

A
DISSERTATION
ON

REALIZATION OF CURRENT MODE AREA SPEED EFFICIENT ANALOG TO DIGITAL CONVERTER

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This is certified that the dissertation entitled “**Realization of Current Mode Area Speed Efficient Analog to Digital Converter**” is a work of **Mr. Yashpal Singh** (University Roll No- 8581) a student of Delhi College of Engineering. This work is completed under my direct supervision and guidance and forms a part of master of engineering (Electronics and communication) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted to any other Institute/University for the award of any other degree to the best of my knowledge.

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ABSTRACT

The growth of analog IC design has been impeded by the process technologies which are mostly optimized for digital applications only. With the evolution of submicron technologies such as 0.18 micron and 0.13 micron, the supply voltages have been reduced to 1.8 Volts and lower. This makes it difficult to design a voltage mode CMOS circuits with high linearity and wide dynamic range. Recently, current mode circuits have become a viable alternative for future applications because of their inherent advantages over voltage mode circuits.

The System on Chip (SoC) technology is highly on demand for digital signal processing applications and wireless systems where it has the ability to provide high speed together with the minimum hardware. In SoC designs, analog and digital building blocks are generally integrated at the same chip. In this case, there should be some interfaces between them. Analog to Digital Converters (ADCs) are the most commonly used mixed-signal modules which transfer analog blocks output data to digital gates. ADCs are one of the major modules in CMOS sensors where they act as the interface between the sensed environment which has analog data and the sensing network which is usually a digital system. They are also used as interfaces for DSP systems, communication networks and multimedia systems.

In this project Current Mode comparator and Area Speed Efficient A/D (Analog to Digital) Converter has been studied and implemented using 0.18um TSMC CMOS VLSI technology. The verification of various modules has been carried out using PSPICE simulations. The configuration generates 4-bit digital output, for a given input current signal, in two stages, generating 2-bits per stage, with reduced time delay. The realized Analog to Digital Converter (ADC) is suitable for high speed current mode operations as appreciable reduction in delay is seen in overall operation as the critical module, current comparator, used is highly efficient in terms of speed of processing.

TABLE OF CONTENTS

Certificate	ii
Acknowledgement	iii
Abstract	iv
Table of Contents...	v
Tables	vii
List of Figures.....	viii
1 INTRODUCTION	1 - 2
1. Introduction	1
2. Organization of Dissertation	2
2 Different types of ADC	3 - 15
2.1. Introduction	3
2.2. ADC Characteristics	3
2.3. ADC Architectures.....	9
3 CMOS Current Mode Comparators	16 - 30
3.1 Introduction.....	16
3.2 Basic Current Mirror.....	16
3.3: Simple Current Mirror.....	18
3.4: Conventional Current Comparator.....	20
3.5: Different Current Comparator Circuits.....	21
3.5.1: Basic CMOS current comparator	21
3.5.2: Cascode Current comparator with inverter output stages	22
3.5.3: Conventional Current Comparator	22
3.6: Time Delay and Slew Rate of different Comparators.....	25
3.7: Simulation Results	26
4. Encoder	31 - 40

4.1: Introduction	31
4.2: Digital IC Technologies and Logic-Circuit Families	31
4.3: Designing of CMOS-Logic Gate Circuits	33
4.4 Truth Table Encoder	35
4.5: Encoder Circuit	36
4.6: Simulation Results.....	38
5. DAC and Current Steering	41 – 54
5.1 Introduction	41
5.2 Basic Operation.....	41
5.3 Practical Operation.....	42
5.4 DAC Types.....	43
5.5 DAC Performance.....	46
5.6 DAC Ckt.....	47
5.7 Current Steering	49
5.8 Simulation Results.....	51
6. ADC (Analog to Digital Converter)	55 –73
6.1 Introduction	55
6.2 ADC Step Size	55
6.3 Values of all Currents in the ASEADC Block Diagram.....	56
6.4 Reference Current for Stage I.....	58
6.5 ADCM Operation.....	59
6.6 SIMULATION Steps.....	61
6.7 Simulation Results.....	62
7. CONCLUSIONS	73
References	74
CMOS Technology Model Parameter	

TABLES:

Table 4.1 Truth Table Encoder Output

Table 5.1 DAC Output with respect to Encoder output

Table 6.1 Iref & Iconst

Table 6.2 For Reference Current

Table 6.3 Constant Currents for Calculating Reference Currents for Stage – II

Table 6.4 B3 & B2 Output with respect to Comp

Table 6.5 Step Calculate for DAC output

LIST OF FIGURES

Fig 2.1 Flash ADC

Fig 2.2 SAR ADC

Fig 2.3 Dual Slope ADC

Fig. 2.4 Pipeline ADC

Fig. 2.5 Algorithm ADC

Fig 3.1. Block representation of a Current Mirror

Fig 3.2 Simple current mirror structure

Fig 3.3 Basic CMOS current Comparator

Fig. 3.4 Current comparator with inverter output stages

Fig 3.5 Conventional Comparator

Fig 3.6 Chang Comparator

Fig 3.7 Comp1 for 2uA Simple Current mode Comparator When $I_{ref} > I_{in}$.

Fig 3.8 Comp1 for 2uA Simple Current mode Comparator when $I_{ref} < I_{in}$

Fig 3.9 Combine Current Comparator Output

Fig 3.10 Cascode Current Comparator

Fig 3.11 Chang Conventional Comparator Output

Fig 4.1 CMOS Network

Fig 4.2 CMOS Encoder Ckt.

Fig 4.2 CMOS Encoder Ckt.

Fig 4.3 Encoder output 1 (01)

Fig 4.4 Encoder output 2 (10)

Fig 4.5 Encoder output 3(11)

Fig 5.1 Ideally Sample Signal

Fig. 5.2 Piecewise Constant Output of a Conventional DAC Ckt

Fig 5.3 Weighted type DAC

Fig 5.4 R-2R Ladder Network

Fig 5.5 DAC Ckt.

Fig 5.6 DAC Ckt. When both current are tied.

Fig 5.7 Current Steering

Fig 5.8 DAC 2uA/8 out put w.r.t to 7.5/30 Input Current.

Fig 5.9 DAC 4uA/16 out put w.r.t to 15/60uA Input Current.

Fig 5.10 DAC 6/24uA out put w.r.t to 22.5uA/90 Input Current.

Fig 5.11 DAC 6/24uA out put w.r.t to 22.5uA/90 Input Current.

Fig 6.1 Area Speed Efficient Analog to Digital Convertor

Fig 6.2 ADC Bit Change Output1 0000 - 0001 bit

Fig 6.3 ADC Bit Change Output1 0001 - 0000 bit

Fig 6.4 ADC Bit Change Output1 0000 - 1100 bit

Fig 6.5 ADC Bit Change Output1 1000 - 0100 bit

Fig 6.6 ADC Bit Change Output1 1000 - 1100 bit

Fig 6.7 ADC Bit Change Output1 1100 - 0000 bit

Fig 6.8 ADC Bit Change Output1 1100 - 0100 bit

Fig 6.9 ADC Bit Change Output1 1111 - 0000 bit

Fig 6.10 ADC Bit Change Output1 0000 - 1111 bit

Fig 6.11 ADC Bit Change Output1 1111 - 0001 bit