A
DISSERTATION
ON

REALIZATION OF CURRENT MODE AREA SPEED EFFICIENT ANALOG TO DIGITAL CONVERTER

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENT
FOR THE AWARD OF THE DEGREE OF

MASTER OF ENGINEERING
(ELECRONICS AND COMMUNICATION)

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CERTIFICATE

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This is certified that the dissertation entitled **"Realization of Current Mode Area Speed Efficient Analog to Digital Converter"** is a work of **Mr. Yashpal Singh** (University Roll No- 8581) a student of Delhi College of Engineering. This work is completed under my direct supervision and guidance and forms a part of master of engineering (Electronics and communication) course and curriculum. He has completed his work with utmost sincerity and diligence.

The work embodied in this major project has not been submitted to any other Institute/University for the award of any other degree to the best of my knowledge.

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ABSTRACT

The growth of analog IC design has been impeded by the process technologies which are mostly optimized for digital applications only. With the evolution of submicron technologies such as 0.18 micron and 0.13 micron, the supply voltages have been reduced to 1.8 Volts and lower. This makes it difficult to design a voltage mode CMOS circuits with high linearity and wide dynamic range. Recently, current mode circuits have become a viable alternative for future applications because of their inherent advantages over voltage mode circuits.

The System on Chip (SoC) technology is highly on demand for digital signal processing applications and wireless systems where it has the ability to provide high speed together with the minimum hardware. In SoC designs, analog and digital building blocks are generally integrated at the same chip. In this case, there should be some interfaces between them. Analog to Digital Converters (ADCs) are the most commonly used mixed-signal modules which transfer analog blocks output data to digital gates. ADCs are one of the major modules in CMOS sensors where they act as the interface between the sensed environment which has analog data and the sensing network which is usually a digital system. They are also used as interfaces for DSP systems, communication networks and multimedia systems.

In this project Current Mode comparator and Area Speed Efficient A/D (Analog to Digital) Converter has been studied and implemented using 0.18um TSMC CMOS VLSI technology. The verification of various modules has been carried out using PSPICE simulations. The configuration generates 4-bit digital output, for a given input current signal, in two stages, generating 2-bits per stage, with reduced time delay. The realized Analog to Digital Converter (ADC) is suitable for high speed current mode operations as appreciable reduction in delay is seen in overall operation as the critical module, current comparator, used is highly efficient in terms of speed of processing.

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