Chapter 1

Introduction

The System on Chip (SoC) technology is highly on demand for digital signal processing applications and wireless systems where it has the ability to provide high speed together with the minimum hardware. In SoC designs, analog and digital building blocks are generally integrated at the same chip. In this case, there should be some interfaces between them. Analog to Digital Converters (ADCs) are the most commonly used mixed-signal modules which transfer analog blocks output data to digital gates. ADCs are one of the major modules in CMOS sensors where they act as the interface between the sensed environment which has analog data and thee sensing network which is usually a digital system. They are also used as interfaces for DSP systems, communication networks and multimedia systems.

An area speed efficient method for analog to digital conversion is implemented in this thesis. This ADC uses a Digital to Analog Converter (DAC). It is made of a combination of current comparators, DAC, and encoders. The conversion of four bits is performed in two stages. In Chapter 2 different types Analog to Digital Converter have been discussed. This chapter also explains total time required for the conversion by the different ADC Structures. In Chapter 3 various realizations of Current Mode Current Comparator have been described. Simulation results are also included for Slew Rate and Delay Time for different Current Mode Comparator. In Chapter 4 the basic idea about different types of Logic Family is given. An encoder circuit that can accept the current comparator's digital output data and convert it to the corresponding 2-bit digital result is designed. Chapter 5 describes DAC (Digital to Analog Conversion) and the Current Steering for the current distribution to the different comparators in the Second Stage of ADC.

Chapter 6 describes ADC Structure and the operation of the different stages used in the Realization of Area Speed Efficient Analog to Digital Converter (ASEADC). The Simulation Results are included for validation. Chapter 7 describes the Conclusion of the ASEADC.

Chapter 2

Different types of ADC

2.1 Introduction

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device which converts continuous signals to discrete digital numbers. The reverse operation is performed by a digital to-analog converter (DAC).

Typically, an ADC is an electronic device that converts an input analog voltage (or current) to a digital number proportional to the magnitude of the voltage or current. However, some non electronic or only partially electronic devices, such as rotary encoders, can also be considered ADCs. The digital output may use different coding schemes, such as binary, Gray code or two's complement binary.

2.2 ADC Characteristics

- **Resolution**

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or "levels", is usually a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from -128 to 127 (i.e. signed integer), depending on the application.

Resolution can also be defined electrically, and expressed in volts. The minimum change in voltage required to guarantee a change in the output code level is

called the LSB (least significant bit, since this is the voltage represented by a change in the LSB). The resolution Q of the ADC is equal to the LSB voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete voltage intervals:

$$Q = E_{FSR}/N$$

Where

N is the number of voltage intervals,

E_{FSR} is the full scale voltage range, given by,

$E_{FSR} = I_{inmax} - I_{inmin}$

The upper and lower extremes respectively of the current that can be coded.

Normally, the number of current intervals is given by,

$N=2^M$

Where M is the ADC's resolution in bits.

In practice, the useful resolution of a converter is limited by the best signal-to-noise ratio that can be achieved for a digitized signal. An ADC can resolve a signal to only a certain number of bits of resolution, called the effective number of bits (ENOB). One effective bit of resolution changes the signal-to-noise ratio of the digitized signal by 6 dB, if the resolution is limited by the ADC. If a preamplifier has been used prior to A/D conversion, the noise introduced by the amplifier can be an important contributing factor towards the overall SNR.

Response type

- **Linear ADCs**

Most ADCs are of a type known as linear The term linear as used here means that the range of the input values that map to each output value has a linear relationship with the output value, i.e., that the output value k is used for the range of input values from

m (k + b) to m (k + 1 + b),

where m and b are constants/ Here b is typically 0 or -0/5/ When b = 0, the !DC is referred to as mid-rise, and when b = -0/5 it is referred to as mid-tread.

➢ Non-linear ADCs

If the probability density function of a signal being digitized is uniform, then the signal-to-noise ratio relative to the quantization noise is the best possible. Because this is often not the case, it is usual to pass the signal through its cumulative distribution function (CDF) before the quantization. This is good because the regions that are more important get quantized with a better resolution. In the dequantization process, the inverse CDF is needed.

This is the same principle behind the companders used in some tape-recorders and other communication systems, and is related to entropy maximization.

For example, a voice signal has a Laplacian distribution. This means that the region around the lowest levels, near 0, carries more information than the regions with higher amplitudes. Because of this, logarithmic ADCs are very common in voice communication systems to increase the dynamic range of the representable values while retaining fine-granular fidelity in the low amplitude region.

An eight-bit A-law or the μ-law logarithmic ADC covers the wide dynamic range and has a high resolution in the critical low-amplitude region that would otherwise require a 12-bit linear ADC.

➢ Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity is intrinsic to any analog-to-digital conversion. There is also a so-called aperture error which is due to a clock jitter and is revealed when digitizing a time-variant signal (not a constant value).

These errors are measured in a unit called the LSB, which is an abbreviation for least significant bit. In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

➢ Quantization error

Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. The magnitude of the quantization error at the sampling instant is between zero and half of one LSB.

In the general case, the original signal is much larger than one LSB. When this happens, the quantization error is not correlated with the signal, and has a uniform distribution. Its RMS

value is the standard deviation of this distribution, given by . In the eightbit ADC example, this represents 0.113% of the full signal range.

At lower levels the quantizing error becomes dependent of the input signal, resulting in distortion. This distortion is created after the anti-aliasing filter, and if these distortions are above 1/2 the sample rate they will alias back into the audio band. In order to make the quantizing error independent of the input signal, noise with amplitude of 1 quantization step is added to the signal. This slightly reduces signal to noise ratio, but completely eliminates the distortion. It is known as dither.

➢ Non-linearity

All ADCs suffer from non-linearity errors caused by their physical imperfections, causing their output to deviate from a linear function (or some other function, in the case of a deliberately non-linear ADC) of their input. These errors can sometimes be mitigated by calibration, or prevented by testing.

Important parameters for linearity are integral non-linearity (INL) and differential non-linearity (DNL). These non-linearities reduce the dynamic range of the signals that can be digitized by the ADC, also reducing the effective resolution of the ADC.

➢ Sampling rate

The analog signal is continuous in time and it is necessary to convert this to a flow of digital values. It is therefore required to define the rate at which new digital values are sampled from the analog signal. The rate of new values is called the sampling rate or sampling frequency of the converter.

A continuously varying band-limited signal can be sampled (that is, the signal values at intervals of time T, the sampling time, are measured and stored) and then the original signal can be exactly reproduced from the discrete-time values by an interpolation formula. The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal. This is essentially what is embodied in the Shannon-Nyquist sampling theorem.

Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the conversion time). An input circuit called a sample and hold performs this task—in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input. Many ADC integrated circuits include the sample and hold subsystem internally.

➢ Aliasing

All ADCs work by sampling their input at discrete intervals of time. Their output is therefore an incomplete picture of the behavior of the input. There is no way of knowing, by looking at the output, what the input was doing between one sampling instant and the next. If the input is known to be changing slowly compared to the sampling rate, then it can be assumed that the value of the signal between two sample instants was somewhere between the two sampled values. If, however, the input signal is changing rapidly compared to the sample rate, then this assumption is not valid.

If the digital values produced by the ADC are, at some later stage in the system, converted back to analog values by a digital to analog converter or DAC, it is desirable that the output of the DAC be a faithful representation of the original signal. If the input signal is changing much faster than the sample rate, then this will not be the case, and spurious signals called aliases will be produced at the output of the DAC. The frequency of the aliased signal is the difference between the signal frequency and the sampling rate. For example, a 2 kHz sine wave being sampled at 1.5 kHz would be reconstructed as a 500 Hz sine wave. This problem is called aliasing.

To avoid aliasing, the input to an ADC must be low-pass filtered to remove frequencies above half the sampling rate. This filter is called an anti-aliasing filter, and is essential for a practical ADC system that is applied to analog signals with higher frequency content.

Although aliasing in most systems is unwanted, it should also be noted that it can be exploited to provide simultaneous down-mixing of a band-limited high frequency signal (see under sampling and frequency mixer).

➢ Relative speed and precision

The speed of an ADC varies by type. The conversion time is directly proportional to the number of channels. For a successive approximation ADC, the conversion time scales with the logarithm of the number of channels. Thus for a large number of channels, it is possible that the successive approximation ADC is faster than the Wilkinson. However, the time consuming steps in the Wilkinson are digital, while those in the successive approximation are analog. Since analog is inherently slower than digital, as the number of channels increases, the time required also increases. Thus there are competing processes at work. Flash ADCs are certainly the fastest type of the three. The conversion is basically performed in a single parallel step. For an 8-bit unit, conversion takes place in a few tens of nanoseconds.

There is, as expected, somewhat of a tradeoff between speed and precision. Flash ADCs have drifts and uncertainties associated with the comparator levels, which lead to poor uniformity in channel width. Flash ADCs have a resulting poor linearity. For successive approximation ADCs, poor linearity is also apparent, but less so than for flash ADCs. Here, non-linearity arises from accumulating errors from the subtraction processes. Wilkinson ADCs are the best of the three. These have the best differential non-linearity. The other types require channel smoothing in order to achieve the level of the Wilkinson.

2.3 ADC Architectures

These are the most common ways of implementing an electronic ADC:

There are five main types of ADC architectures-

- **Flash-type**
- **Successive approximation**
- **Integrating,**

- Couter Type
- Pipeline,
- Algorithmic

Each has benefits that are the unique to that architecture and span the spectrum high speed and resolution.

➢ Flash –type or Simultaneous ADC

- Flash or the parallel converters have the highest speed of any type of ADC. They utilize one comparator per quantization level *(2N - 1)* and *2N* resistors.

- The reference voltage is divided into 2N values, each of which is fed into comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators.

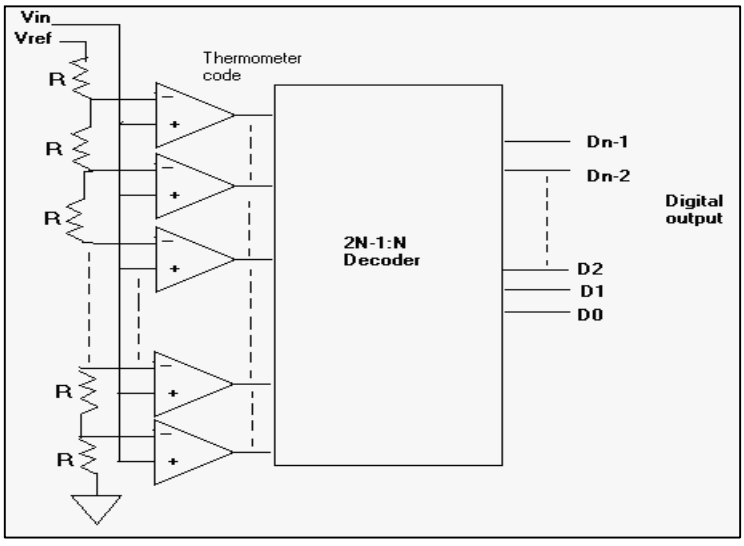

Fig 2.1 Flash ADC

- Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer.

- ❖ Since the number of comparators needed, $2^N - 1$, doubles with each additional bit, requiring a large expensive circuit.
- ❖ ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches on the output (by outputting an out-of-sequence code).

➢ Successive-Approximation Register (SAR) ADC

- ❖ The successive approximation converter basically performs a binary search through all possible quantization levels before converging on final digital answer.

- ❖ An N-bit register controls the timing of the conversion where N is the resolution of the ADC. V_{in} is sampled and compared to the output of the DAC. The comparator output controls the direction of the binary search and the output of the successive approximation register (SAR) is the actual digital conversion.

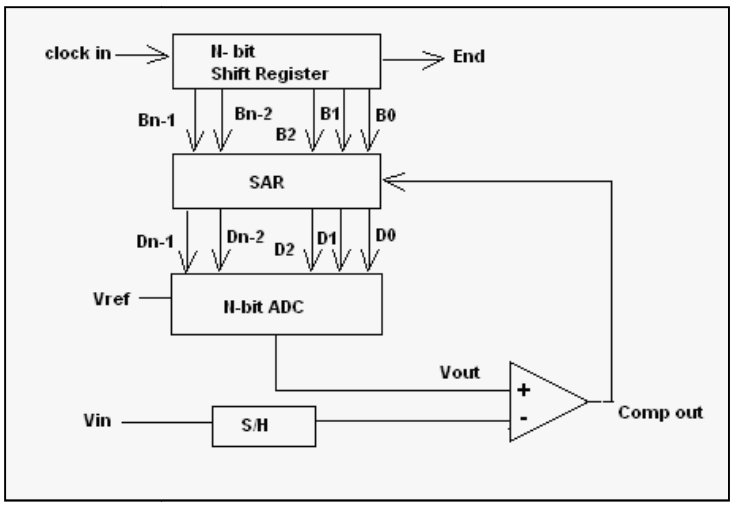

Fig 2.2 SAR ADC

- ❖ The Conversion Time is required by the SAR ADC is: $T = NT_c$

where N is the number of bit, Tc is the time of clock period and T is the total time required by the SAR ADC.

- **Dual Slope ADC**
  - Another type of ADC performs the conversion by the input signal and correlating the integrating time with a digital counter.
  - Known as single and dual-slope ADCs, these types of converters are used in high resolution applications but have relatively slow conversions.
  - However, they are very inexpensive to produce and are commonly found in slow-speed, cost conscious applications.
  - Total charging time taken by the Dual Slope ADC is $2^N T_c$.
  - Total conversion time taken by the Dual Slope ADC is $2NTc + (V_a / V_{ref}) 2^N T_c$.

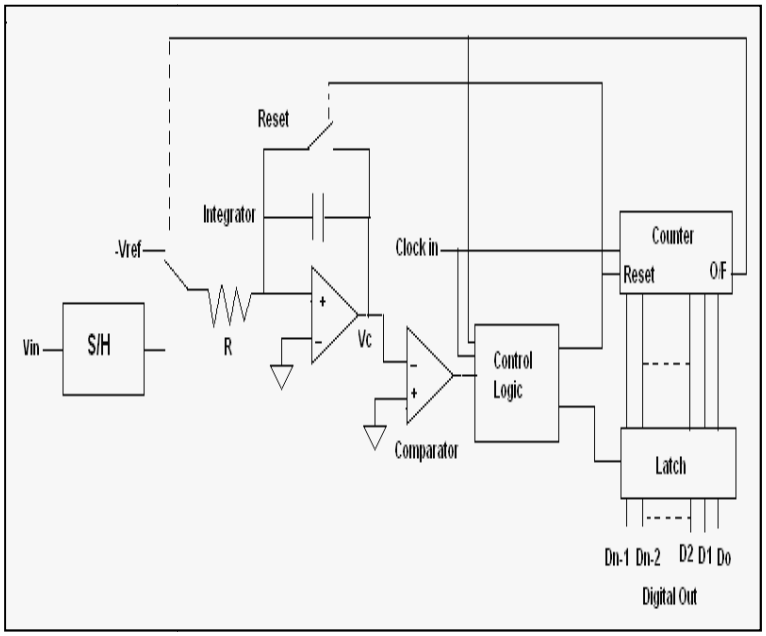

Fig 2.3 Dual Slope ADC

- **Pipeline ADC**

- ❖ The pipeline ADC is an N-step converter, with 1-bit being converted per stage.
- ❖ Able to achieve high resolution (10-13 bits) at relatively fast speeds, the pipeline ADC consists of N-stages connected in series.
- ❖ Each stage contains a 1-bit ADC (a comparator), a sample and hold, a summer and a gain of two amplifier.

A main advantage of the pipeline converter is its high throughput. After an initial delay of N clock cycles, one conversion will be completed per clock cycle. While the residue of the first stage is being operated on by the second stage, the first stage is free to operate on next samples. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions.

The disadvantage is having initial N clock cycle delay before the first digital output appears. The severity of disadvantage is, of course, dependent on the application.

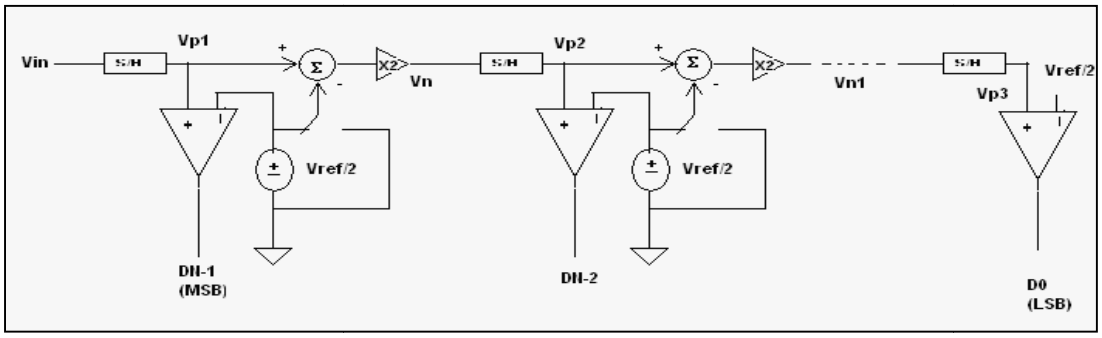

Fig. 2.4 Pipeline ADC

➢ Algorithmic ADC

The algorithmic ADC, also called **cyclic** or **recirculating** converter has been known and utilized in various forms since 1960s.

It was first realized by Hornak in a partially integrated form using a transformer to achieve a gain of two in 1975.

Subsequently Mc. Charles achieved full integration of analog portion of the converter using a metal gate CMOS technology.

The algorithmic ADC consists of an analog signal loop which contains-

- A sample-and-hold amplifier
- A multiply-by-two amplifier
- A comparator
- A reference subtraction circuit.

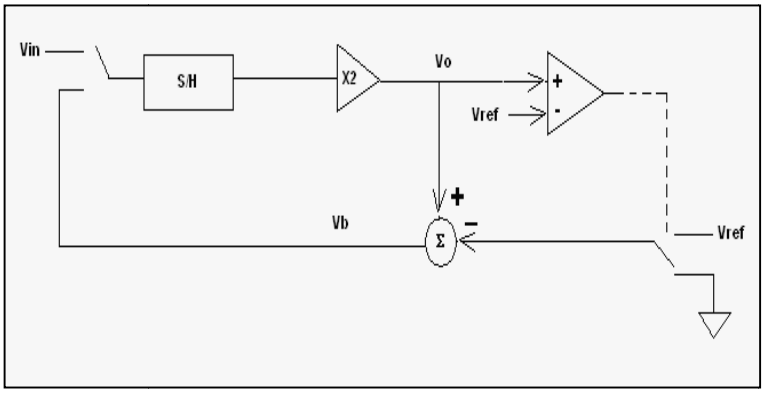

Fig. 2.5 Algorithm ADC

- The operation of the converter consists of first sampling the input signal onto the sample/hold amplifier. This is done by selecting the input signal instead of the loop signal using select switch.
- The input signal is then passed to the multiply-by-two amplifier where it is amplified.
- To extract the digital information from the input signal, the resultant signal, Vo is compared to the reference. If it is larger than the reference, the corresponding bit is set to 1 and the reference is then subtracted off from Vo. Otherwise, this bit is set to 0 and the signal Vo is kept unchanged.
- The resultant signal, denoted by Vb is then transferred, by means of switch back into the analog loop for further processing.

- ❖ This process continues until the desired numbers of bits have been obtained, whereupon a new sampled value of the input signal will be processed. Thus, the digital data comes out from the converter in a serial manner, the MSB first.

The algorithmic ADC can be constructed with very little precision hardware. Its implementation in a monolithic technology can therefore be relatively area-sparing.

It also possesses inherent S/H capability because the S/H amplifier is an integral part of the converter.

It also possesses floating-point operation capability i.e. the input signal can be amplified 2n times before the A/D conversion commences. These properties are very desirable for the design of single-chip complete data acquisition system.

Chapter 3

CMOS Current Mode Comparators

3.1 Introduction

In recent years current-mode signal processing using CMOS technology has gained interest Analog CMOS circuits with small area, high speed and low supply voltage have been designed using this approach. Moreover, it is compatible to digital process, so current mode circuit considered to be alternative to voltage-mode circuit for high speed and low power application as a fundamental component of current mode analog system, current comparator can be use in Analog to Digital converters, oscillators, current to frequency converters, VLSI neural networks and etc. It is a circuit that can compare two values of current applied to them and provide us with a result in logic-1 or logic-0 format.

The desired features of a current comparator include high speed, low input impedance, low power and low supply voltage. Among these requirements, the speed for low current levels is very critical in many situations since it can be the limiting factor of the overall speed of a system. For instance the speed of a current mode Analog to Digital converter is limited by the response time of the comparator at its minimum input current levels for a given possibility of the meta-stability error.

3.2 BASIC CURRENT MIRROR

As the name suggests, a current mirror is expected to perform the similar functions with the electrical current as the plane optical mirror does for the optical signals. Hence a current mirror is a three terminal device whose output current at any instant of time is independent of voltage applied across its

terminals and depends solely on the input current. The output current is the scaled version of the input current. Thus, in other words, **a current mirror reverses the direction of current injected into the low impedance input port and allows its true or scaled version to flow into a high impedance output port**. However the direction of the output current can also be reversed.

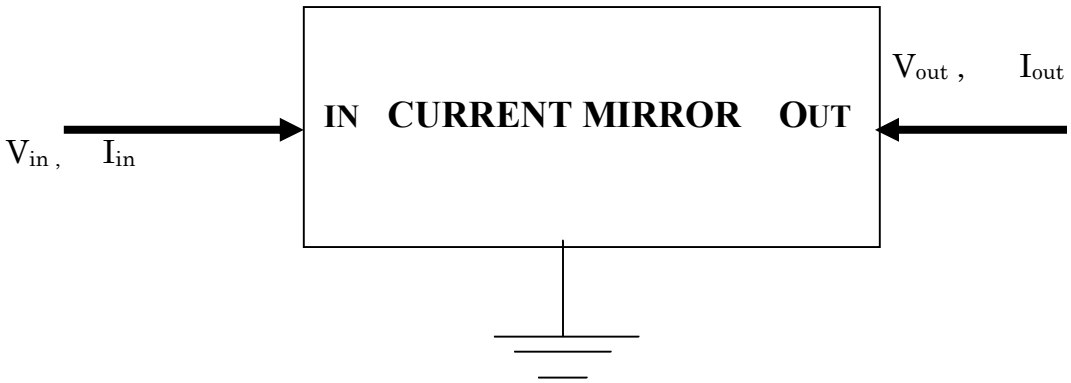

Fig 3.1. Block representation of a Current Mirror

For any high performance system, a current mirror must possess the following characteristics: -

- Current transfer ratio, which is precisely set by the (W/L) ratios, independent of temperature.
- Very high output impedance (high R_{out} and low C_{out}). As a result, the output current is independent of output voltages.
- Low input resistance (R_{in}).
- Low input and output compliance voltages.

Almost all analog circuit structures whether they operate as current mode devices or voltage mode devices, use current mirror in their design. To name a few such devices, following devices are based on the use of the current mirrors.

- Operational amplifiers.

- ❖ Operational trans-conductance amplifiers.
- ❖ Operational trans-resistance amplifiers.
- ❖ Current feedback amplifiers.
- ❖ Current conveyors.
- ❖ Operational floating conveyors.
- ❖ Digital to analog converters.
- ❖ Analog to digital converters.

3.3 Simple Current Mirror

Figure 3.2 shows the basic structure for a current mirror. In no-saturation region the MOSFET is not a good current source. Hence, it is assumed that both the transistors are in saturation region.

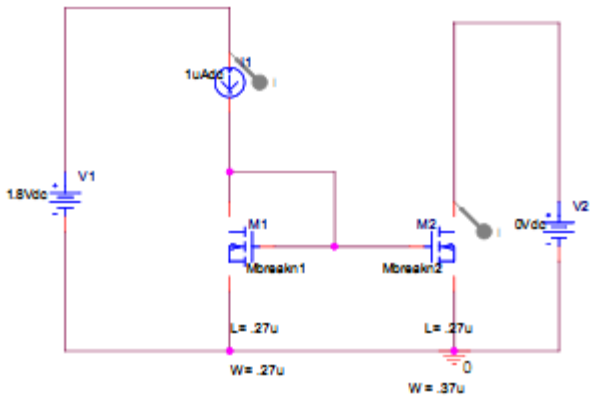

Fig 3.2 Simple current mirror structure

The voltage across the output transistor M2 must be larger than V_{eff} (=V_{GS} -V_T). If the finite output impedance of the transistors are ignored, and it is assumed that both transistors have same size, then M1 and M2 will have same current since they both have same gate source voltage. In the most general case the current transfer function which is defined as the ratio of mirrored current (I_{out}) to the input current (I_{in}) is given by-

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right]\left[\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}}\right]\left[\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right]\left[\frac{K_2}{K_1}\right] \quad (1)$$

Normally, the components of current mirror are processed on the same integrated circuit and all the physical parameters (V_T, K', etc) are identical for both M1 and M2. As a result, the previous equation simplifies to-

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right]\left[\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}\right] \quad (2)$$

If $V_{DS2} = V_{DS1}$, then the above equation further reduces to

$$\frac{Iout}{Iin} = \left[\frac{L_1 W_2}{L_2 W_1}\right] \quad (3)$$

Thus the current transfer ratio is under the control of a circuit designer. However the ideal conditions do not exist and there are three sources of non-idealities in a current mirror. There is finite output impedance and the input impedance is also not zero. These parameters are given as

V_{in} (min) = V_{DS} (sat) + V_T (4)

V_{out} (min) = V_{DS} (sat) (5)

$$R_{in} = \frac{1}{g_{m1}} \quad (6)$$

$$R_{out} = \frac{1}{g_{O2}} = \frac{1}{\lambda I_{DQ2}} \quad (7)$$

There is a tradeoff between output impedance (R_{out}) and output capacitance (C_{out}). Bigger size transistors achieve higher $R_{out,\ which}$ is always desired for a

current mirror. But there will be higher C_{out} associated bigger size transistors, which obviously degenerates the frequency response of a current mirror.

The advantages offered by a simple current mirror include its simple architecture and high output voltage swing capabilities. However, these mirrors are generally plagued with low output impedance characteristics. This low output impedance may not be sufficient for many applications. Thus there is a need to investigate some other circuit structures for the current mirror applications.

3.4 Conventional Current Comparator

A simple current comparator can be designed using current mirrors. But to achieve fast comparison of data in the real time application, we are bound to look for new implementation which can have high frequency operations and less delay time. To get this challenge we first need to have knowledge of the basic current comparator which is shown in the figure below.

In the following circuit current comparator is obtained by using three cascode current mirror two of them are realized using NMOS and one which is appearing in the inverted position uses PMOS. According to the CMOS technology being used appropriate voltage can be selected for VDD . We are considering a supply voltage of 1.8V for further discussion on this circuit.

In conventional current comparator we provide two current values at the reference current position of the current mirror. As shown in the circuit one of the current is the I in which represent analog information obtained from any of the system. For comparing anything we need a reference value, which in our case is a reference current I ref given as input at other node. The output, in the form of voltage value, taken form drain of MOS M3 is obtained on the basis of following relation:

1. if I in> Iref then Vo= 0V

2. if I in< I ref then Vo= 1.8V

These voltage output values can also be inferred as digital output, for which V0 =0 is equivalent to logic-'0' and V0=1 is equivalent to logic-'1'.

To improve the output waveform so obtained we can use inverters after this circuit which picks up the Vo and provide square shaped output waveform.

Although this circuit is capable of providing desired result in the given input range but it is having very large delay which is not acceptable. To overcome delay problems many improved current comparator were then designed, some of them are discussed in the next section.

3.5 Different Current Comparator Circuits

3.5.1 Basic CMOS current comparator

Fig. 3.3 shows the basic CMOS current comparator. Transistors M1, M2 make up the n-type current mirror and M3 and M4 the p-type current mirror. The input current I_{in} and the output current I_{ref} are replicated by the current mirrors at the drains of M2 and M4 are connected together to give the output V_{out}. The output voltage changes from high to low depending on the values of input current and output current.

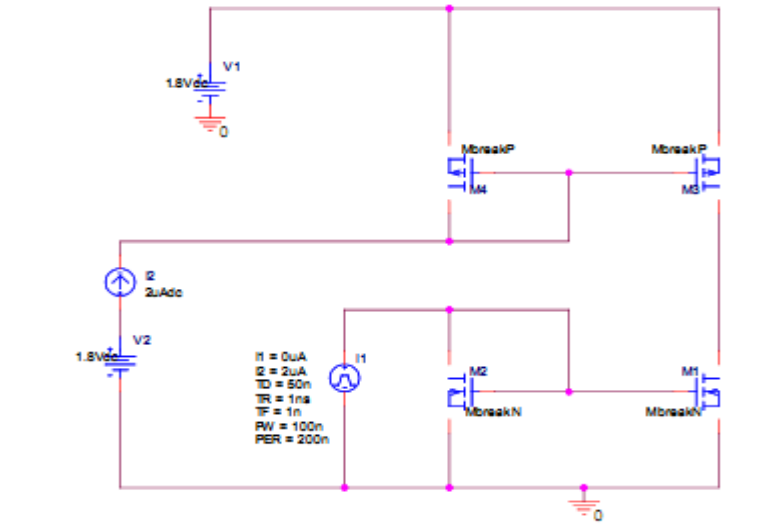

Fig 3.3 Basic CMOS current Comparator

3.5.2 Cascode Current comparator with inverter output stages

In order to obtain better circuit performance, basic current mirrors were replaced by cascode current mirrors. Moreover, to improve the noise margin and to obtain high sensitivity the gain of the current comparator should be high. Three CMOS inverter stages are added to the output stage to achieve full output voltage swing between 0 and 5. Fig. 3.2 shows the current mirror with cascode current mirrors as input stage and three inverters making the output stage.

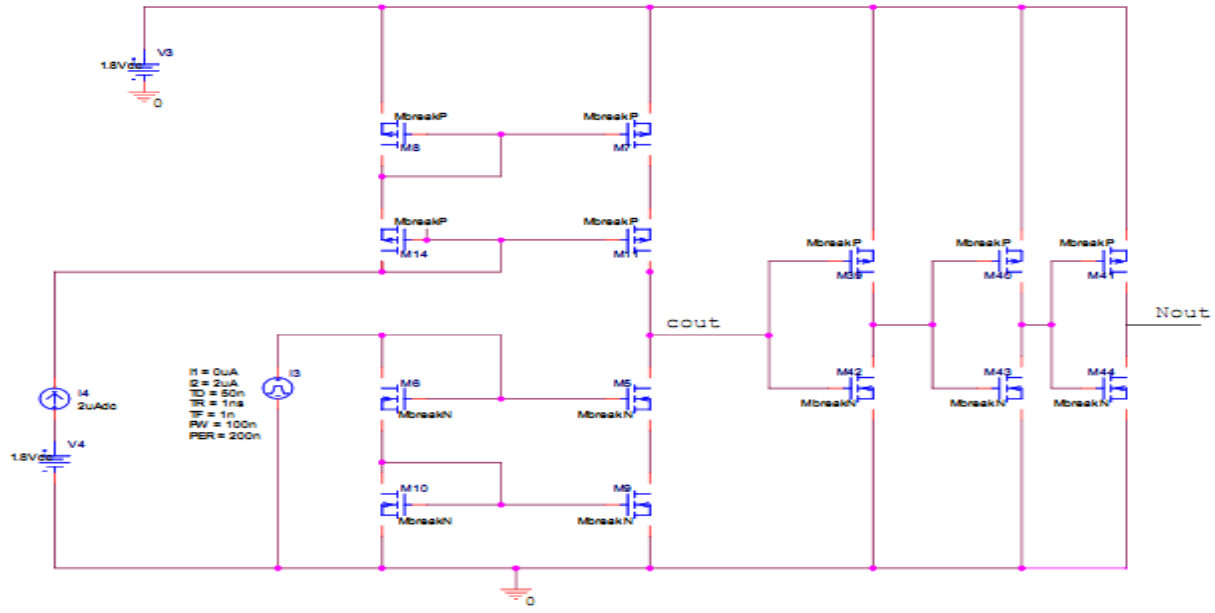

Fig. 3.4 Current comparator with inverter output stages

3.5.3 Conventional Current Comparator

Figure 1a shows a conventional CMOS current-mode comparator. It comprises the threshold current (Ith) generation circuit, which is made up of transistors MP1 and M N1, the mirror pMOS MP2 t hat produces a replica of Ith , the input nMOS MN2 in a diode-connected configuration, and its mirror transistor MN3. The discrepancy between Ith , and the input current Iin ,either becomes the charging current for the output capacitive load CL if the former is greater than the latter, or the discharging current, if the opposite is t rue. As a result, the output voltage Vout will rise to a 'high' logic level if Iin is less than Ith ,and vice

versa. The expression for Ith is derived as follows. B y equating the saturation currents o f M P1 and MN1, their gate potential VG is given by

$$V_g = \frac{V_{dd} - |V_{tp}| \pm \sqrt{\frac{K_{mn1}}{K_{mp}}} V_{th}}{1 + \sqrt{\frac{Kmn1}{Kmp1}}}$$

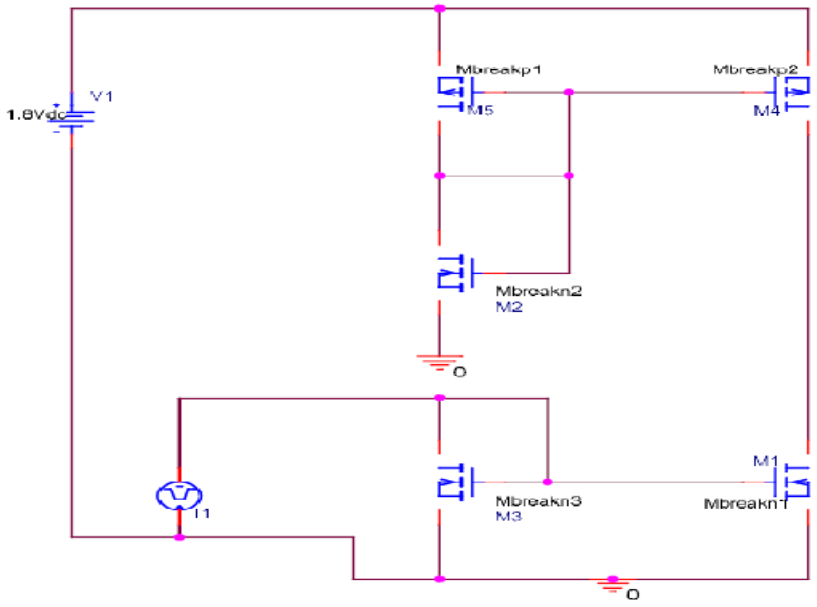

Fig 3.5 Conventional Comparator

where VDD denotes the power supply voltage, while Vtp and Vtn are the pMOS and nMOS threshold voltage, respectively. K is a device parameter defined by

$$Kmn1 = \frac{1}{2}\mu nCox\frac{Wmn1}{Lmn1}$$

The same equation for pMOS.

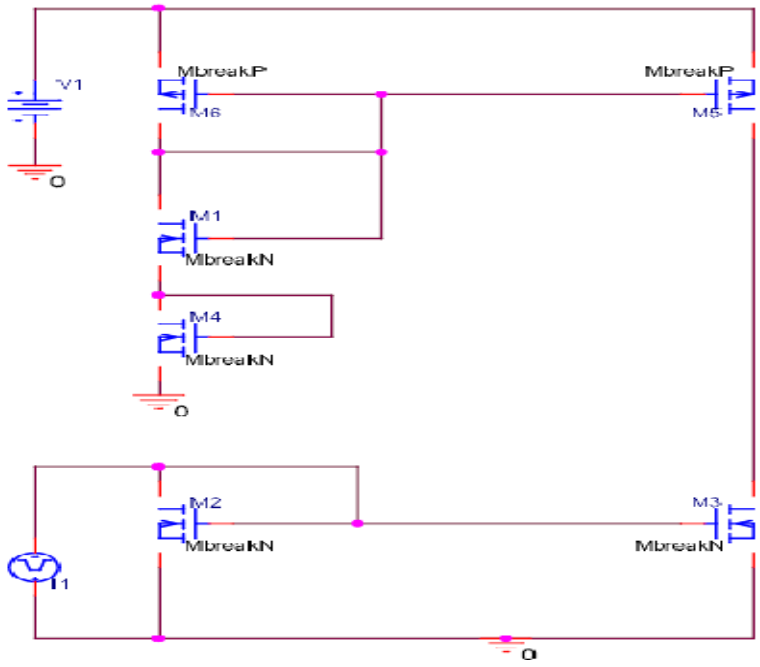

Fig 3.6 Chang Comparator

This conventional current comparator has a major drawback, which is its inability to offer a small-area feature when Ith is low owing to the constraint of minimum channel width. When Ith is low, the area of the comparator is necessarily large, since the aspect ratio will b e less than 1 as shown b y the Cadence Spectre simulation for low Ith .This implies that in order t o achieve a low Ith , the channel length has to be scaled up proportionately. This will inevitably increase the area o f the circuit. As area is one of the most fundamental and critical design parameters for optimum performance, the new current-mode comparator will be a plausible solution t o t his problem.

This intuitive observation is translated into practice by introducing the new current-mode comparator , which in corporates an nMOS device in series with, or beneath the original threshold generation circuit. Figure 3.6 portrays the modified circuit showing the additional nMOS device, MN4, which aids in reducing V GS can be reduced substantially by decreasing V GS , and hence attaining smaller Ith . In fact, more than one nMOS device can be inserted for

even smaller values of I. By examining the threshold current generating circuit, one can observe:

$$V_{DD} = |V_{tp}| + n\,V_{tn}$$

where n denotes the maximum number of nMOS devices that can be coupled into the threshold generation circuit before any of the devices in the threshold generation circuit comes out of saturation mode. The rest of the circuit is practically the same as the conventional circuit.

Extensive simulations have been carried out on the Current Mirror conventional comparator based on 180nm CMOS technologies.

3.6 Time Delay and Slew Rate of different Comparators

Current Mode Comparators	Delay (ns)	Slew Rate (V/us)
Simple Current Comparator	1.656	114.285
Cascode Comparator	0.946	10.526
Modified Conventional Comparator	2.002	0.8771

3.7 Simulation Result:

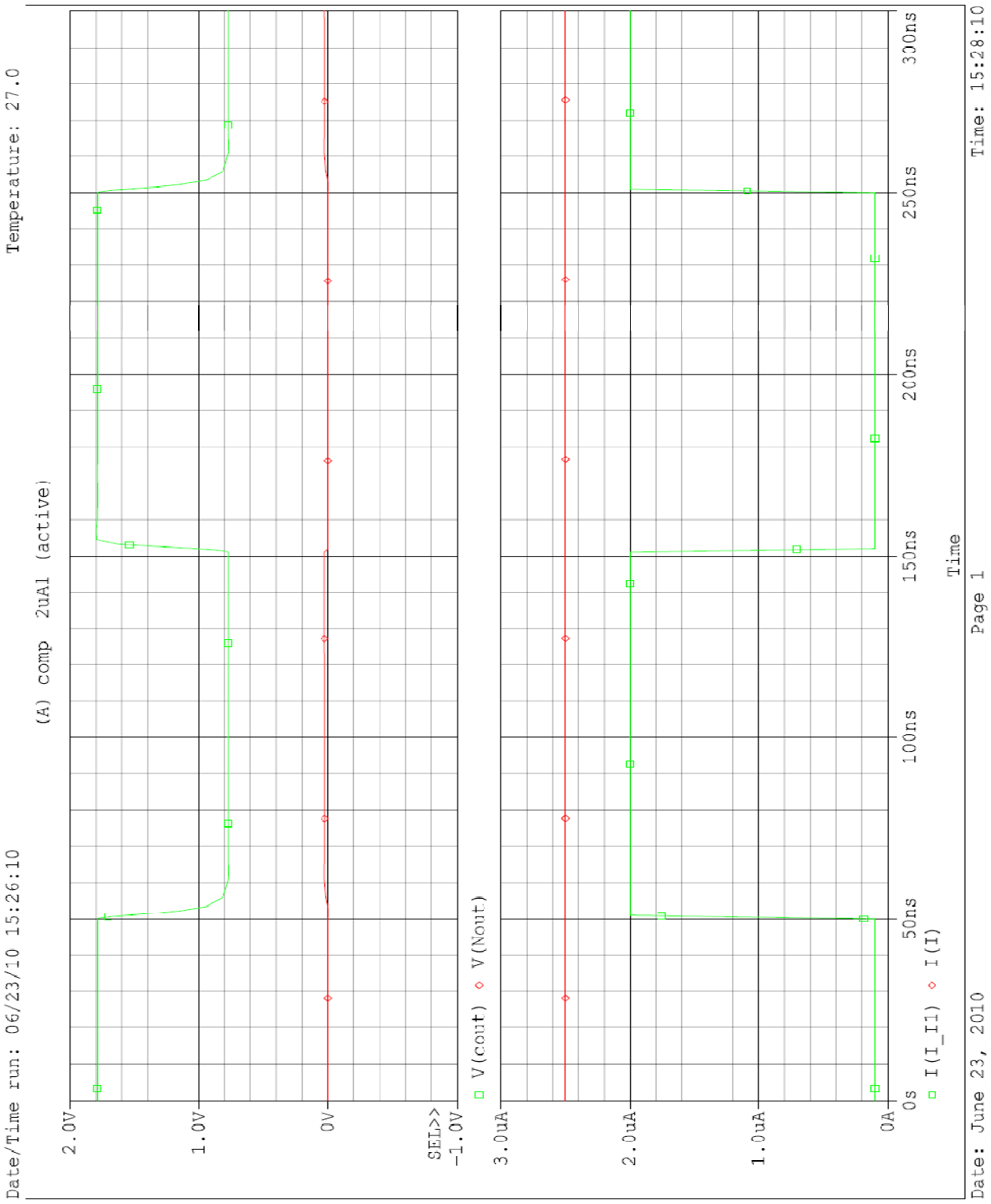

Fig 3.7 Comp1 for 2uA Simple Current mode Comparator When Iref>Iin.

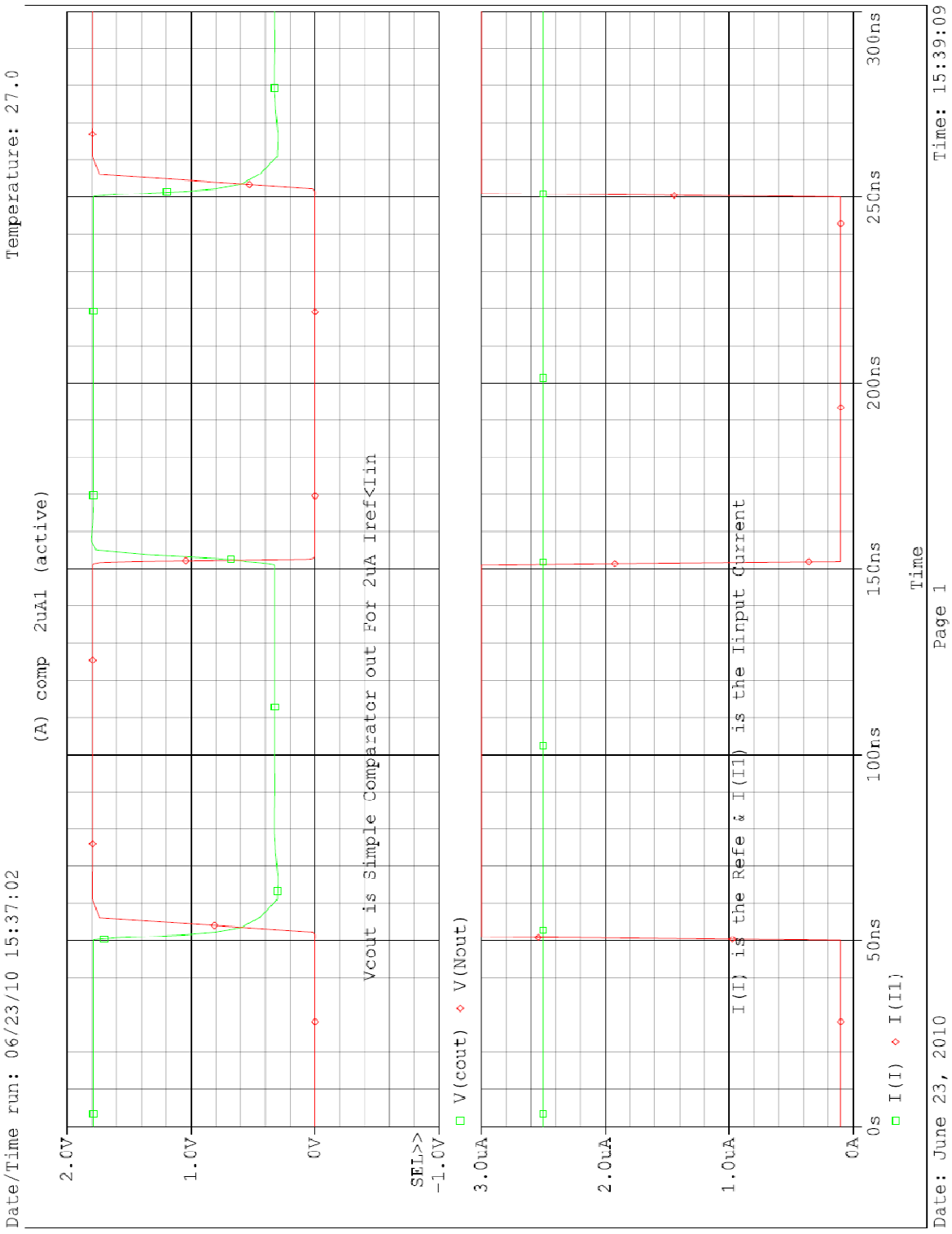

Fig 3.8 Comp1 for 2uA Simple Current mode Comparator when Iref<Iin

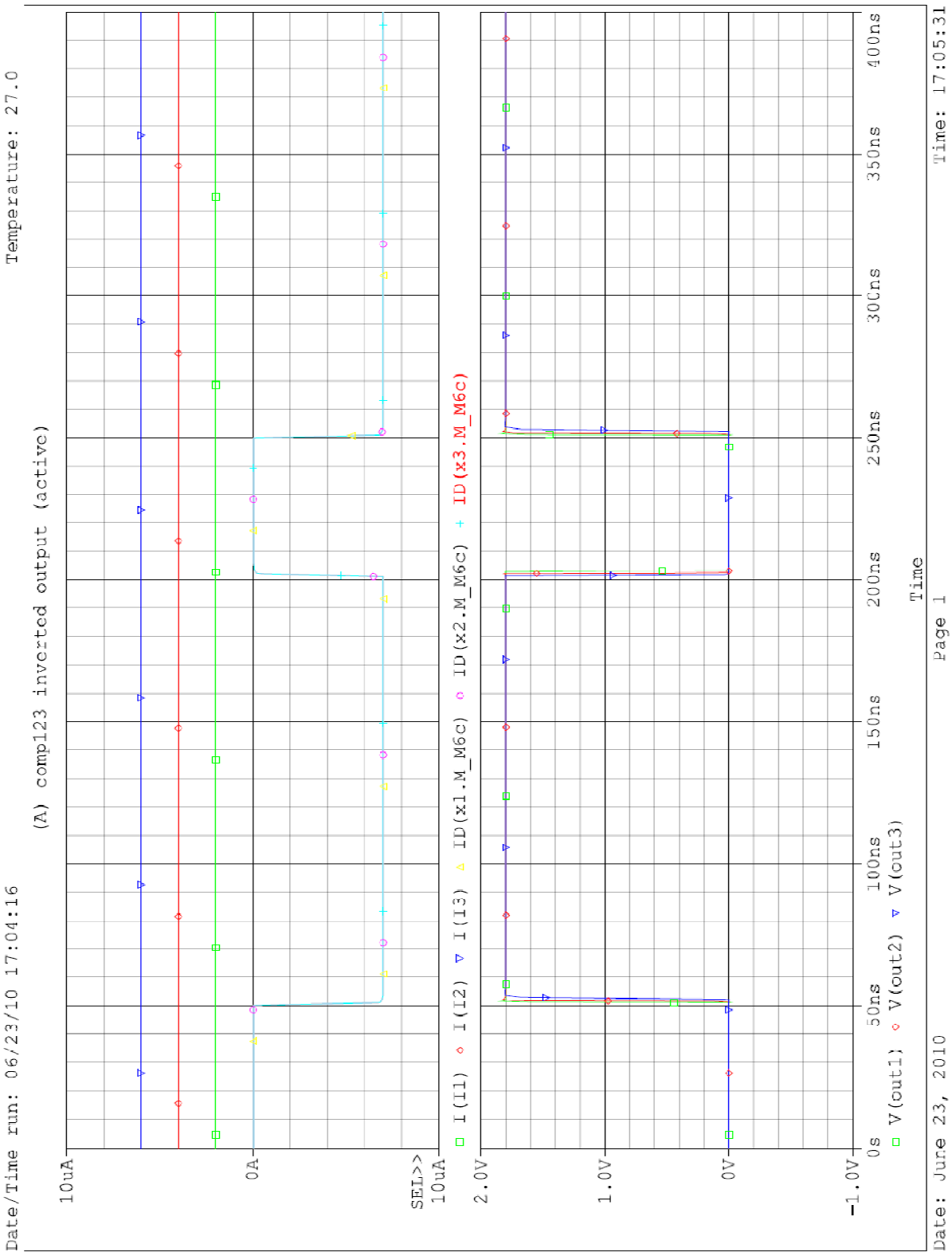

Fig 3.9 Combine Current Comparator Output

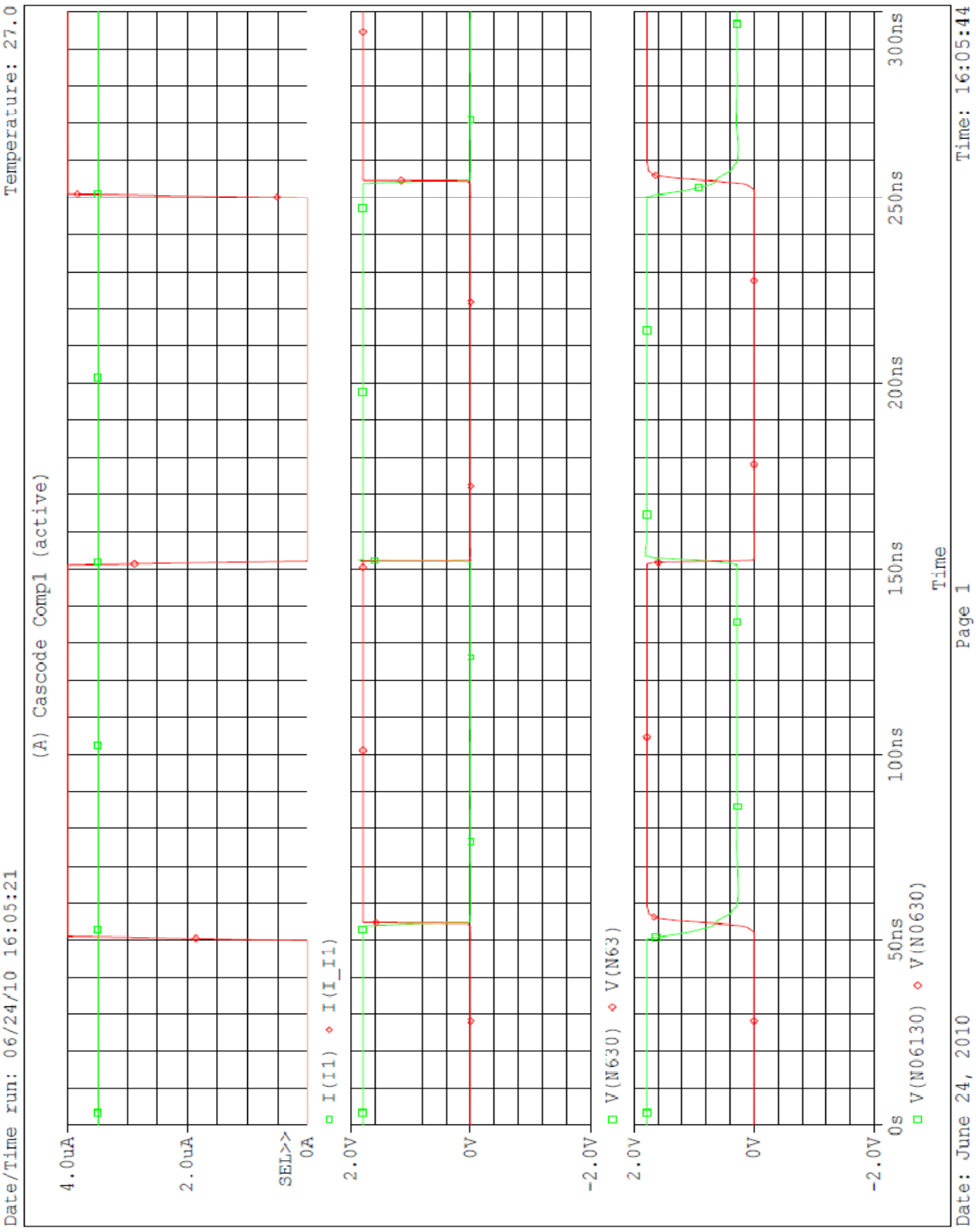

Fig 3.10 Cascode Current Comparator

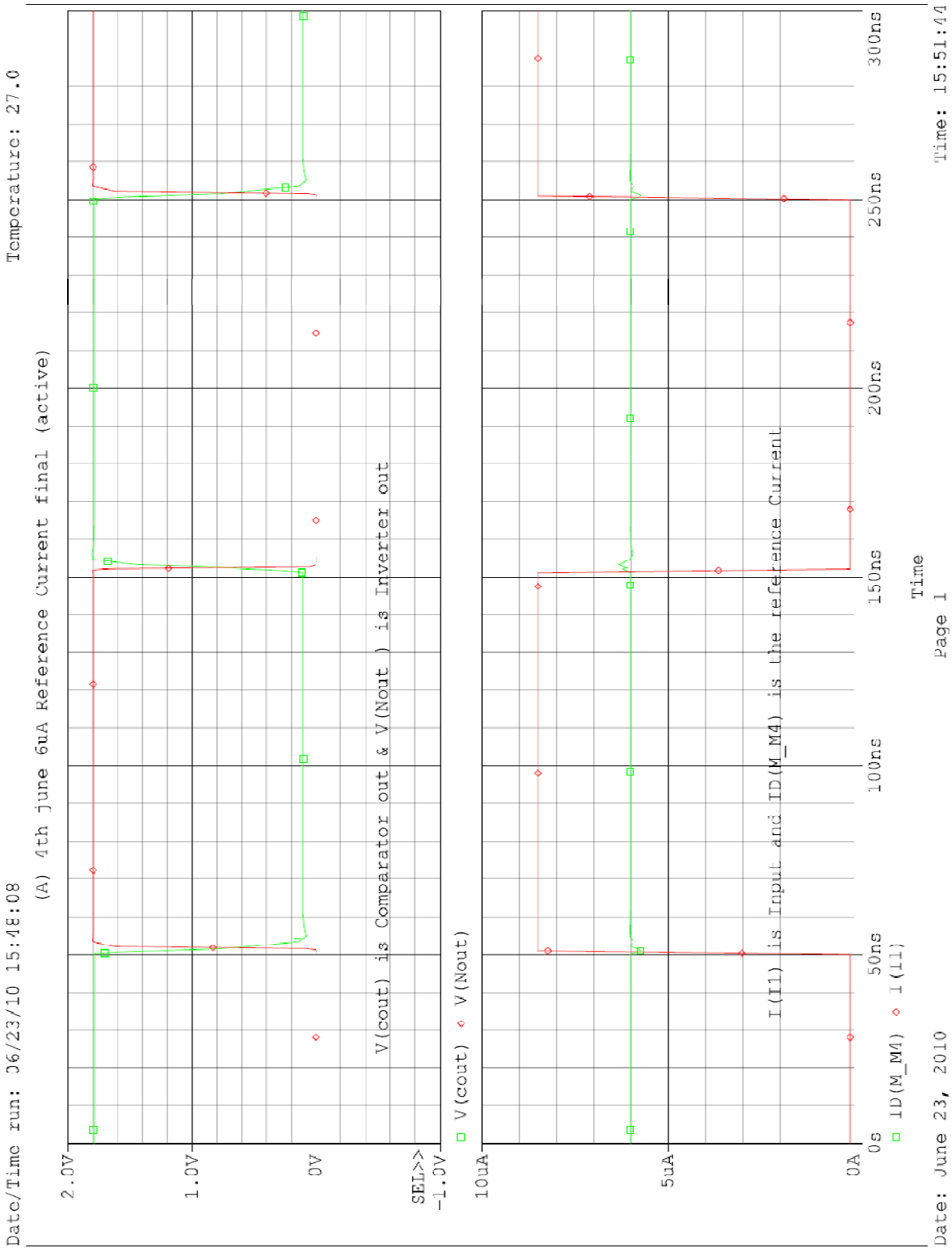

Fig 3.11 Chang Conventional Comparator Output

Chapter 4

Encoder

4.1 Introduction

An encoder is a circuit that converts any decimal digit and/or alphabetic character into the coded representation of those inputs as per the requirement of a particular application to achieve desired results in terms of secured data or compressed or a different representation that is compatible for a given system. In our particular application we require a encoder circuit that can accept the current comparator's digital output data and convert it to the corresponding 2-bit digital result.

4.2 Digital IC Technologies and Logic-Circuit Families

The chart shown in the figure 4.1 shows the major IC technologies and logic-circuit families that are currently in use. Members of each family are made with the same technology, have a similar circuit structure, and exhibit the same basic features. Each logic-circuit family offers a unique set of advantages and disadvantages. In the conventional style of designing systems, one selects an appropriate logic family (e.g. TTL , CMOS, or ECL) and attempts to implement as much of the system as possible using circuit modules (packages) that belong to this family. In this way, interconnection of the various packages is relatively straightforward. If, on the other hand, packages from more than one family are used, one has to design suitable interface circuits. The selection of a logic family is based on such considerations as logic flexibility, speed of operation, availability of complex functions, noise immunity, operating-temperature range, power dissipation and cost.

CMOS Technologies

CMOS is, by a large margin, the most dominant of all the IC technologies available for the digital-circuit design. CMOS has replaced NMOS , which was employed in the early days of VLSI (in the 1970's)/ There are a number of reasons for this development, the most important of which is the much lower power dissipation of CMOS circuits. CMOS has also replaced Bipolar as the technology-of-choice in digital system design, and has made possible levels of integration (or circuit packing densities) and a range of applications, neither of which would have been possible with the bipolar technology. Furthermore, CMOS continues to advance, whereas there

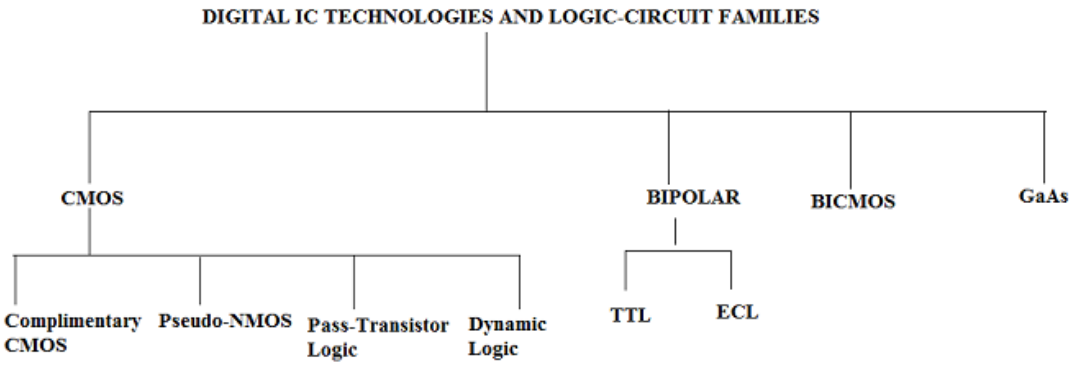

Figure4.1 Digital IC circuit technologies and Logic-circuit Families

appear to be few innovations at the present time in bipolar digital circuits. Some of the reasons for CMOS displacing the bipolar technology in digital applications are as follows:

- CMOS logic circuits dissipate much lesser power than the bipolar logic circuits and thus one can pack more CMOS circuits on a chip than is possible with the bipolar circuits.
- The high input impedance of the MOS transistor allows the designer to use the charge storage as a means for the temporary storage of information in both the logic and memory circuits. This technique cannot be used in bipolar circuits.
- The feature size (i.e. minimum channel length) of the MOS transistor has

decreased dramatically over the years, with some recently reported designs utilizing channel lengths as short as 0.06μm. This permits very tight circuit packing and, corresponding, very high levels of integration.

Of the various forms of CMOS, complimentary CMOS circuits based on the inverter are most widely used. They are available both as small-scale integration (SSI) circuit packages (containing 1-10 logic gates) and medium-scale integrated (MSI) circuit packages (10-100 gates per chip) for assembling digital systems on printed-circuit boards. More significantly, complimentary CMOS is used in VLSI logic (with millions of gates per chip) and memory-circuit design. In some applications, complimentary CMOS is supplemented by one (or both) of two other MOS logic circuit forms. These are pseudo-NMOS, so-named because of the similarity of its structure to NMOS logic, and pass transistor logic. Another type of CMOS logic circuit utilizes dynamic techniques to obtain faster circuit operation, while keeping the power dissipation very low. Dynamic techniques to obtain faster circuit operation, while keeping the power dissipation very low. Dynamic CMOS logic represents an area of growing importance.

Of the various CMOS design techniques described above, we have used the complimentary CMOS circuit design based on the inverter.

4.3 Designing of CMOS-Logic Gate Circuits

A CMOS logic circuit is in effect an extension, or a generalization, of the CMOS inverter. The inverter consists of an NMOS pull-down transistor, and a PMOS pull-up transistor, operated by the input voltage in a complimentary fashion. The CMOS logic gate consists of two networks: Pull- down network (PDN) constructed of NMOS transistors, and the Pull-up network (PUN) constructed of the PMOS transistors. The two networks are operated by the input variables, in a complimentary fashion. Thus, for the three-input gate represented in figure 3.2 the PDN will conduct for all input combinations that require a low output (Y=0) and will then pull the output node down to ground, causing a zero voltage to

appear at the output, Vy=0. Simultaneously, the PUN will be off, and no direct dc path will exist between V_{dd} and ground. On the other hand, all input combinations that call for a high output (Y=1) will cause the PUN to conduct, and the PUN to conduct, and the PUN will then pull the output node up to V_{dd}, establishing an output voltage $V_y = V_{dd}$. Simultaneously, the PDN will be cut off, and again, no dc current path between V_{dd} and ground will exist in the circuit.

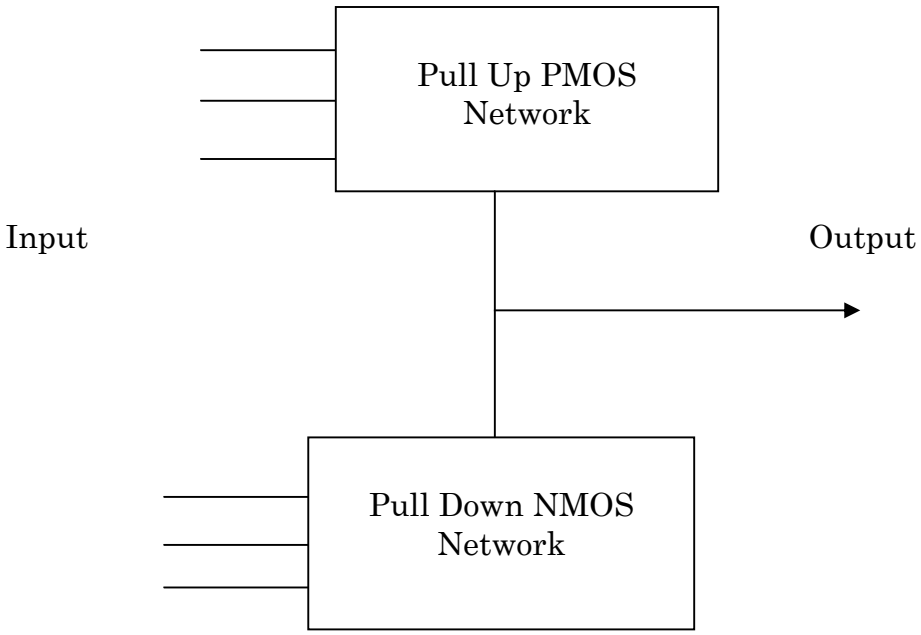

Fig 4.1 CMOS Network

Now since the PDN comprises NMOS transistors, and since an NMOS transistor conducts when the signal at its gate is high, the PDN is activated (i.e. conducts) when the inputs are high. In dual manner, the PUN comprises PMOS transistors, and a PMOS transistor conducts when the input signal at its gate is low; thus the PUN is activated when the inputs are low.

The PDN and PUN utilizes devices in parallel to form an OR function, and devices in series to form an AND function. Here the OR and AND refer to the current flow or conduction.

4.4 Truth Table Encoder

The input-output relationship required to implement the function required in the ADC circuit is shown in the table below (Table 4.1).

Comparator outputs			Encoder Outputs	
C_3	C_2	C_1	B_3, B_1	B_2, B_2
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Table 4.1 Truth Table Encoder Output

Encoder for stage-I will provide outputs B_3 and B_2 for which the Boolean relation can be derived from the truth table and it comes out as:

$B_3 = C1.\ C2$

$B_2 = C1.\ (C2\ \textbf{xnor}\ C3)$

But from table it can be observed that if output of the comparator is 1, i/e/ C1 is '1' then the output of *comparator j that is Cj* would be also '1' because Ij < Ii as long as j < i, consequently the equations can be modified as follows:

B3 = C2

$B2 = C3 + (C1 . C2')$

Similarly encoder at stage-II is responsible for providing the binary output for bit B1 and B0 and this encoding is exactly similar as done at stage-I for B3 and B2 respectively. Thus the equation for encoder at stage-II can be written as follows:

$B_1 = C2$

$B_0 = C3 + (C1. C2')$

4.5 Encoder Circuit

To implement the above mentioned Boolean relation for the encoder circuit pull-up and pull down networks are made from PMOS and NMOS respectively. Final circuit thus obtained is shown below:

A=INVT (C3)

B=INVT (C1)

C=C2.

In this encoder circuit, PMOS M1, M2 and M3 are part of pull up network while NMOS M4, M5 and M6 are part of pull-down network.

This circuit is simulated using CMOS 180nm technology parameters at voltage supply of 1.8V.

The simulation results for the various inputs applied to the encoder are shown in next section.

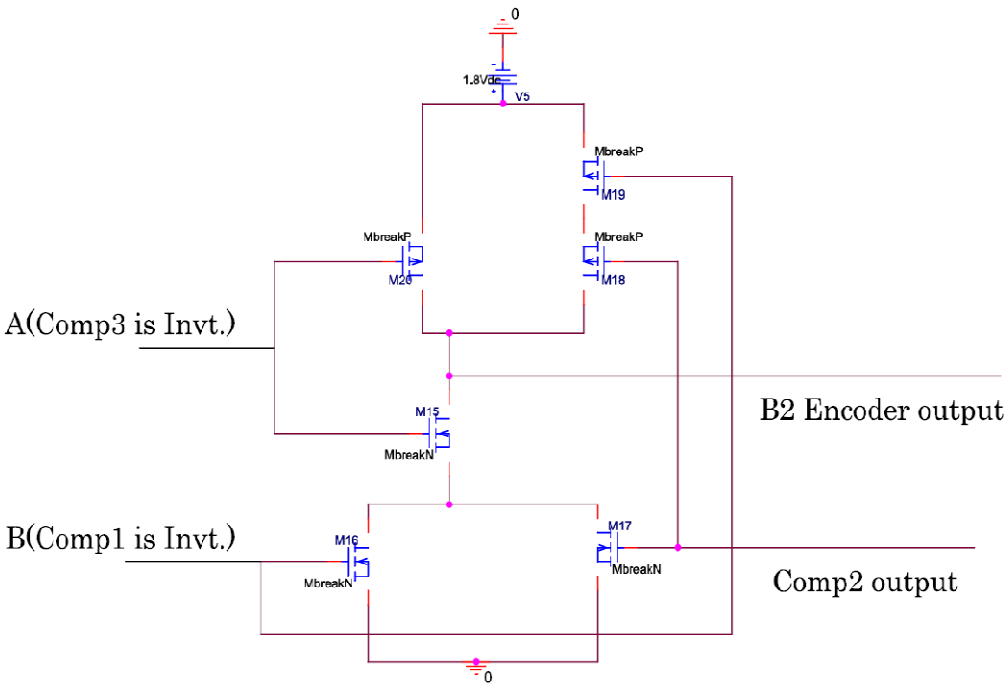

Fig 4.2 CMOS Encoder Ckt.

4.6 Simulation Results:

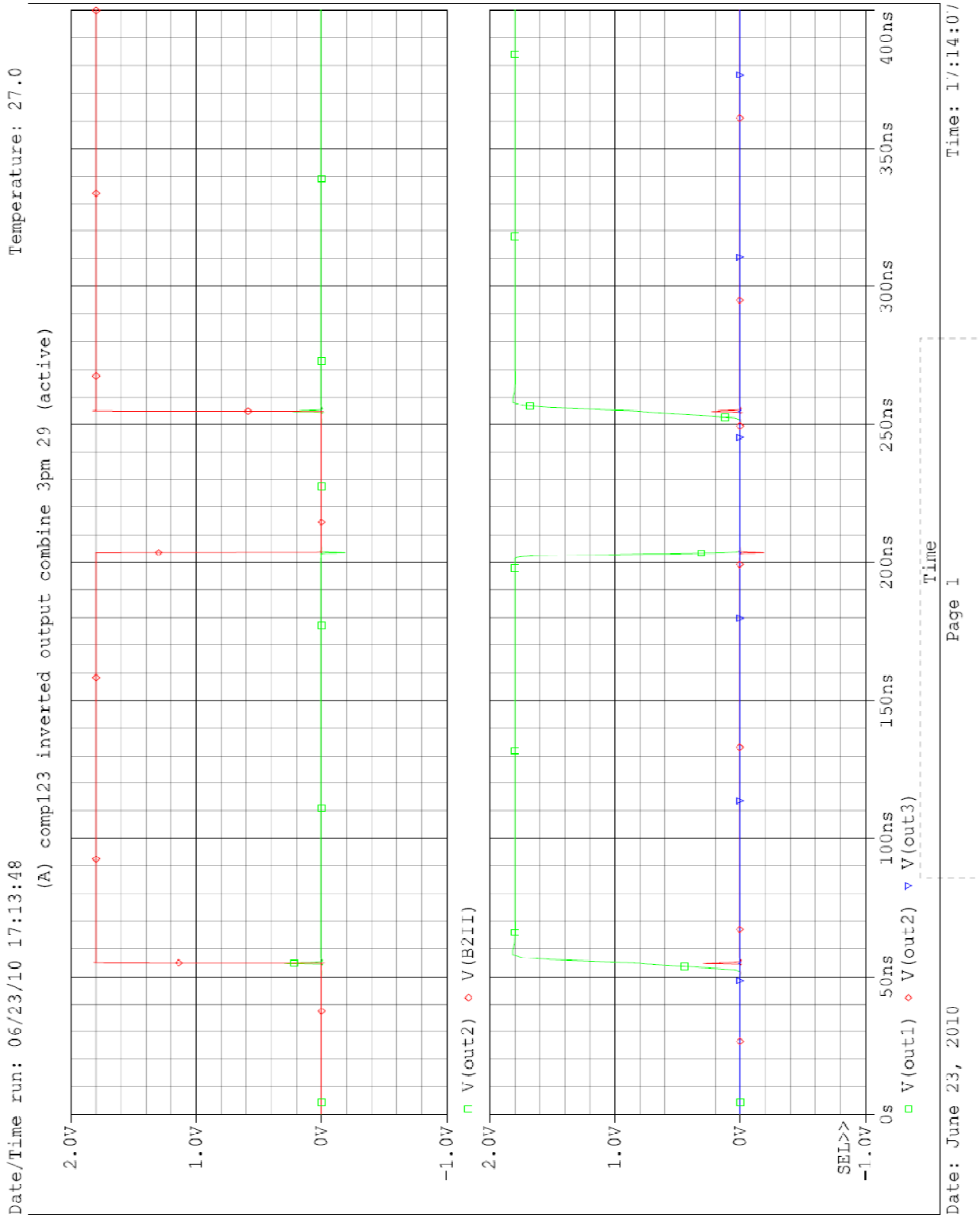

Fig 4.3 Encoder output 1 (01)

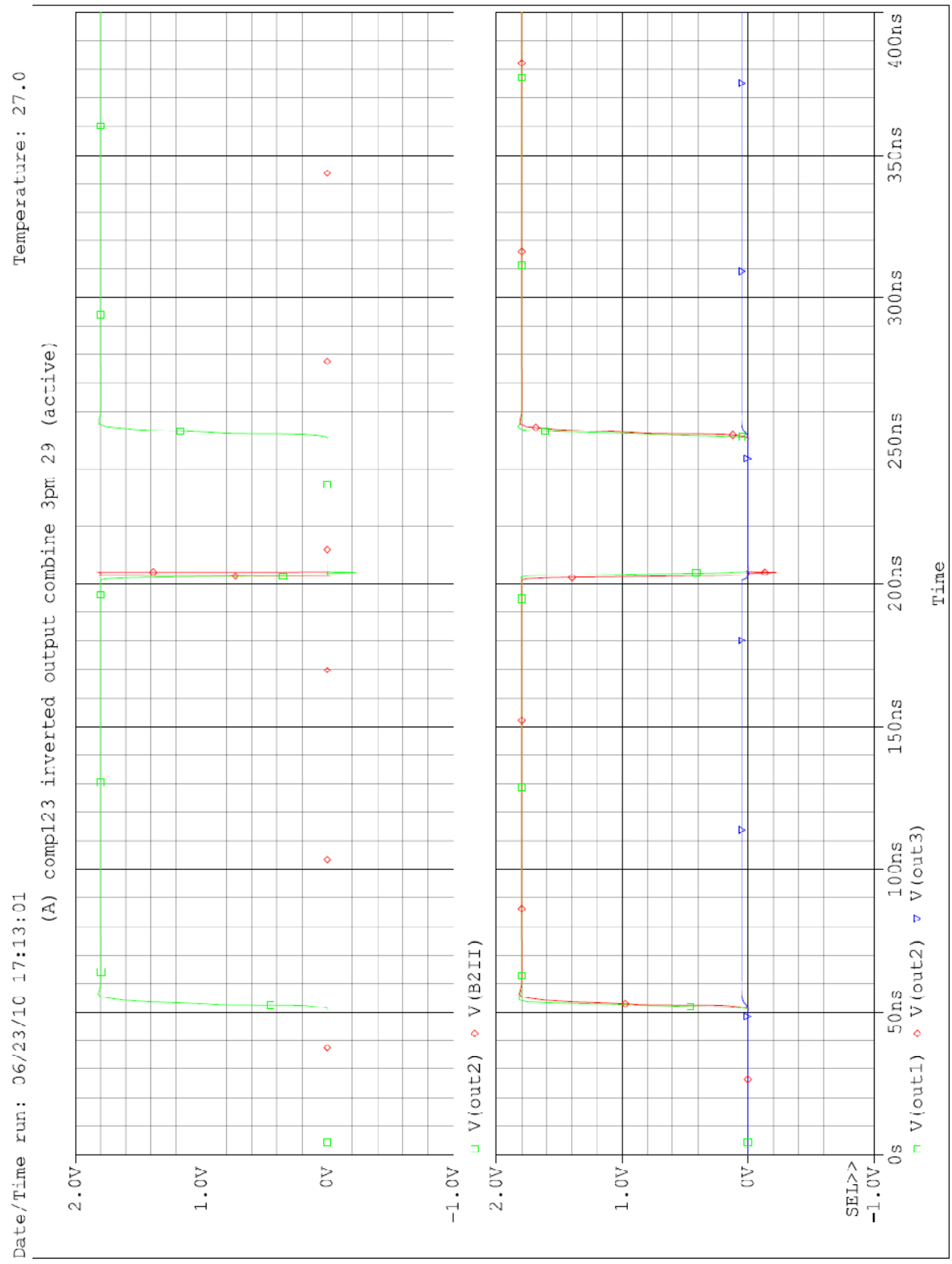

Fig 4.4 Encoder output 2 (10)

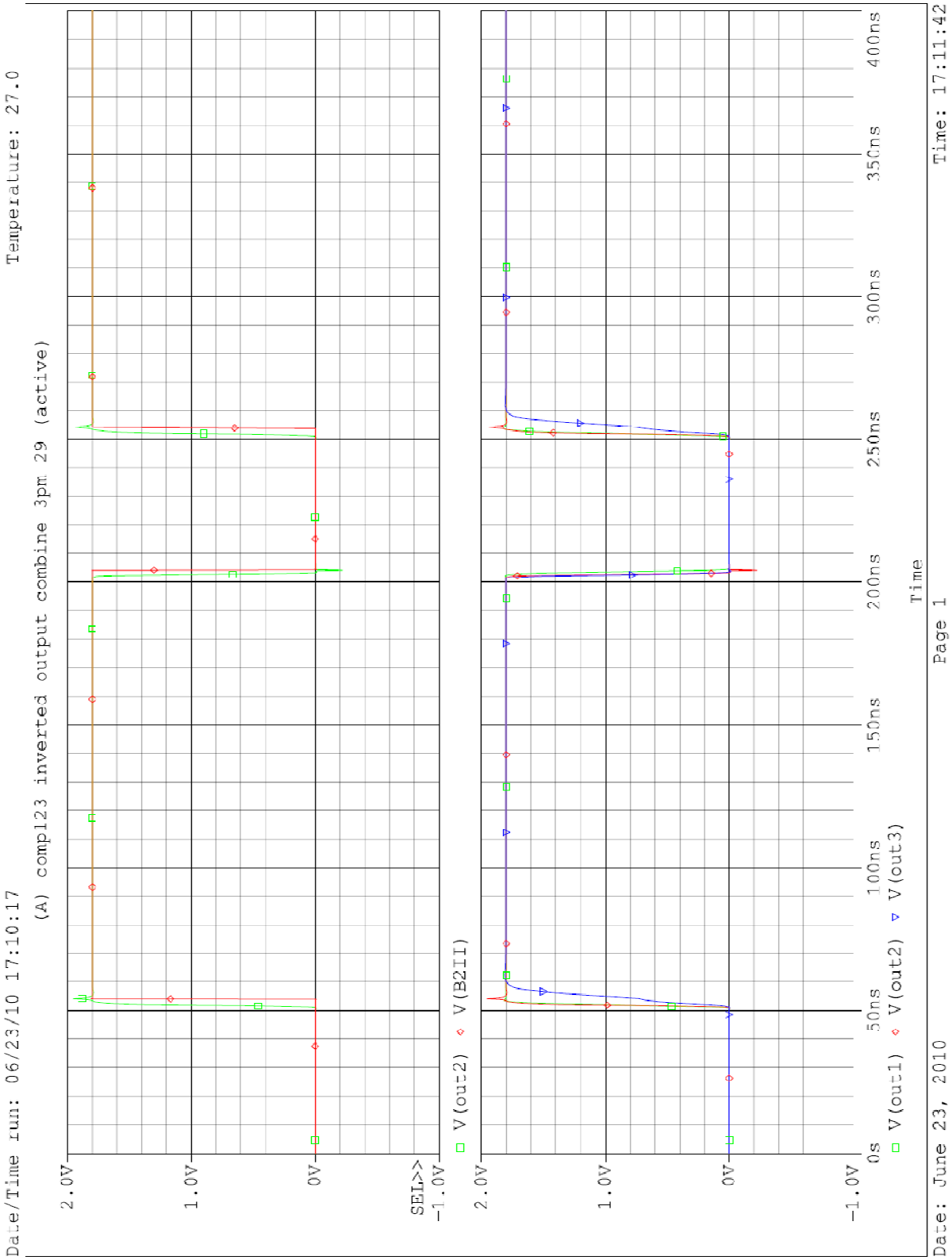

Fig 4.5 Encoder output 3(11)

Chapter 5

DAC & Current Steering

5.1 Introduction

A **digital-to-analog converter** (**DAC** or **D-to-A**) is a device that converts a digital (usually binary) code to an analog signal (current, voltage, or electric charge). An analog-to-digital converter (ADC) performs the reverse operation.

5.2 Basic Operation

A **digital-to-analog converter** (**DAC** or **D-to-A**) is a device that converts a digital (usually binary) code to an analog signal (current, voltage, or electric charge). An analog-to-digital converter (ADC) performs the reverse operation.

An encoder is a circuit that converts any decimal digit and/or alphabetic character into the coded representation of those inputs as per the requirement of a particular application to achieve desired results in terms of secured data or compressed or a different representation that is compatible for a given system. In our particular application we require a encoder circuit that can accept the current comparator's digital output data and convert it to the corresponding 2-bit digital result.

By the Nyquist–Shannon sampling theorem, sampled data can be reconstructed perfectly provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency). However, even with an ideal reconstruction filter, digital sampling introduces quantization error that makes perfect reconstruction practically impossible. Increasing the digital resolution (i.e., increasing the number of bits used in each sample) or introducing sampling dither can reduce this error.

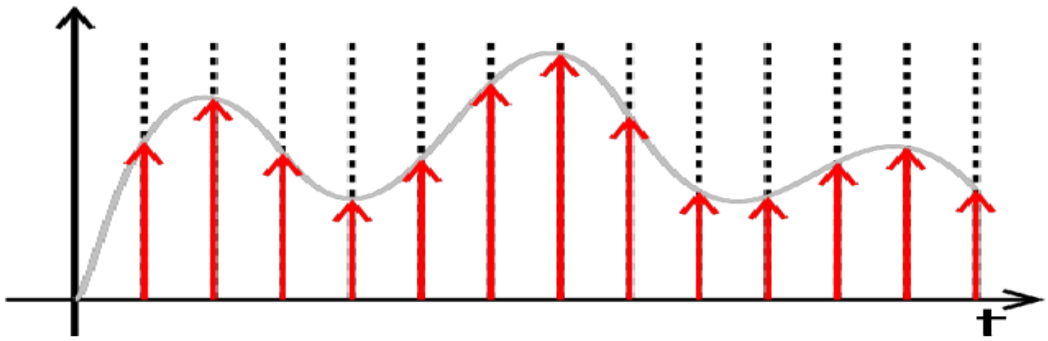

Fig 5.1 Ideally Sample Signal

5.3 Practical Operation

Instead of impulses, usually the sequence of numbers update the analogue voltage at uniform sampling intervals.

These numbers are written to the DAC, typically with a clock signal that causes each number to be latched in sequence, at which time the DAC output voltage changes rapidly from the previous value to the value represented by the currently latched number. The effect of this is that the output voltage is *held* in time at the current value until the next input number is latched resulting in a piecewise constant or 'staircase' shaped output. This is equivalent to a zero-order hold operation and has an effect on the frequency response of the reconstructed signal.

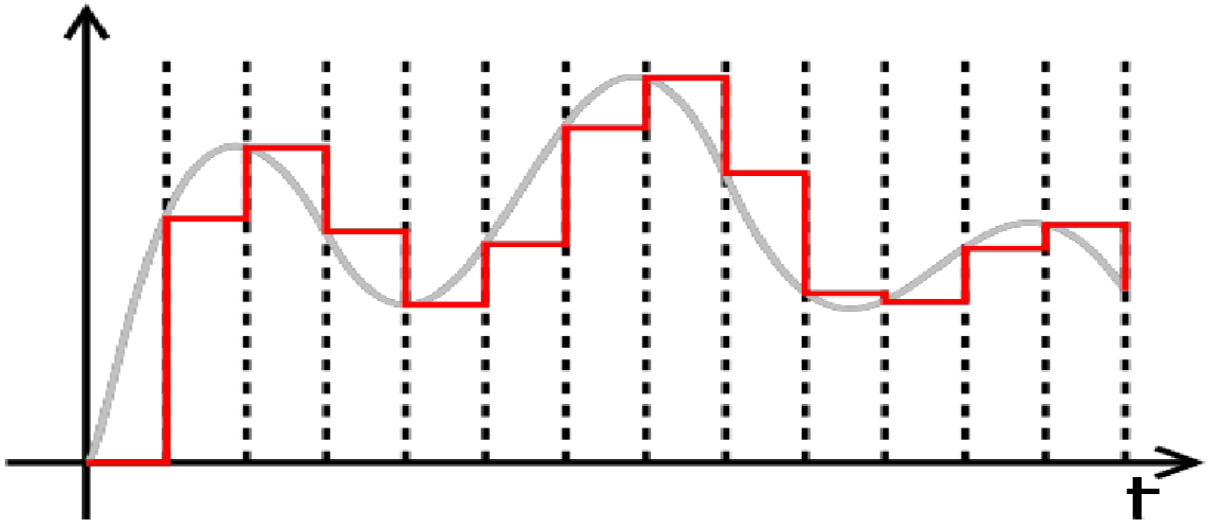

Fig. 5.2 Piecewise Constant Output of a Conventional DAC Ckt.

The fact that practical DACs output a sequence of piecewise constant values or rectangular pulses would cause multiple harmonics above the Nyquist frequency. These are typically removed with a low pass filter acting as a reconstruction filter.

However, this filter means that there is an inherent effect of the zero-order hold on the effective frequency response of the DAC resulting in a mild roll-off of gain at the higher frequencies (often a 3.9224 dB loss at the Nyquist frequency) and depending on the filter, phase distortion. Not all DACs have a zero order response however. This high-frequency roll-off is the output characteristic of the DAC, and is not an inherent property of the sampled data.

5.4 DAC Types

The most common types of electronic DACs are:

- **Pulse-Width Modulator,** the simplest DAC type. A stable current or voltage is switched into a low-pass analog filter with a duration determined by the digital input code. This technique is often used for electric motor speed control, and is now becoming common in high-fidelity audio.

- **Oversampling DACs** or interpolating DACs such as the **Delta-Sigma DAC**, use a pulse density conversion technique. The oversampling technique allows for the use of a lower resolution DAC internally. A simple 1-bit DAC is often chosen because the oversampled result is inherently linear. The DAC is driven with a pulse-density modulated signal, created with the use of a low-pass filter, step nonlinearity (the actual 1-bit DAC), and negative feedback loop, in a technique called delta-sigma modulation. This results in an effective high-pass filter acting on the quantization (signal processing) noise, thus steering this noise out of the low frequencies of interest into the high frequencies of little interest, which is called noise shaping (*very* high frequencies because of the oversampling). The quantization noise at these high frequencies are removed or greatly attenuated by use of an analog low-pass filter at the output (sometimes a simple RC low-pass

circuit is sufficient). Most very high resolution DACs (greater than 16 bits) are of this type due to its high linearity and low cost. Higher oversampling rates can either relax the specifications of the output low-pass filter and enable further suppression of quantization noise. Speeds of greater than 100 thousand samples per second (for example, 192 kHz) and resolutions of 24 bits are attainable with delta-sigma DACs. A short comparison with pulse-width modulation shows that a 1-bit DAC with a simple first-order integrator would have to run at 3 THz (which is physically unrealizable) to achieve 24 meaningful bits of resolution, requiring a higher-order low-pass filter in the noise-shaping loop. A single integrator is a low-pass filter with a frequency response inversely proportional to frequency and using one such integrator in the noise-shaping loop is a first order delta-sigma modulator. Multiple higher order topologies (such as MASH) are used to achieve higher degrees of noise-shaping with a stable topology.

- **Binary-weighted DAC**, which contains one resistor or current source for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision resistors and current sources are expensive, so this type of converter is usually limited to 8-bit resolution or less.

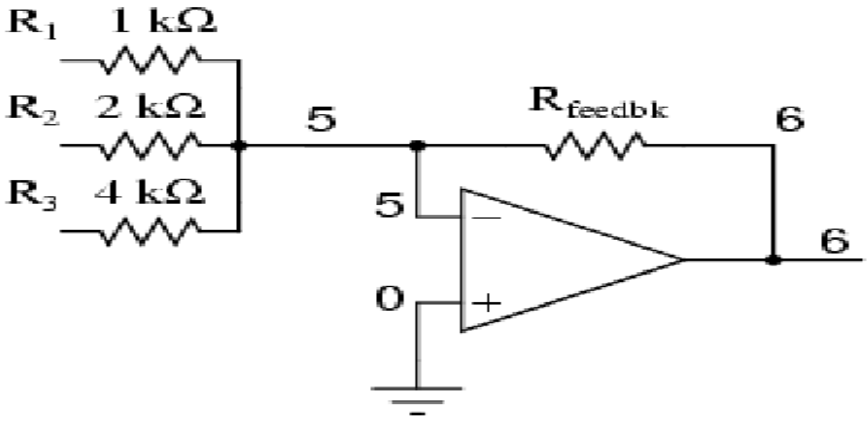

Fig 5.3 Weighted type DAC

- **R-2R ladder DAC** which is a binary-weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued-matched resistors (or current sources). However, wide converters perform slowly due to increasingly large RC-constants for each added R-2R link.

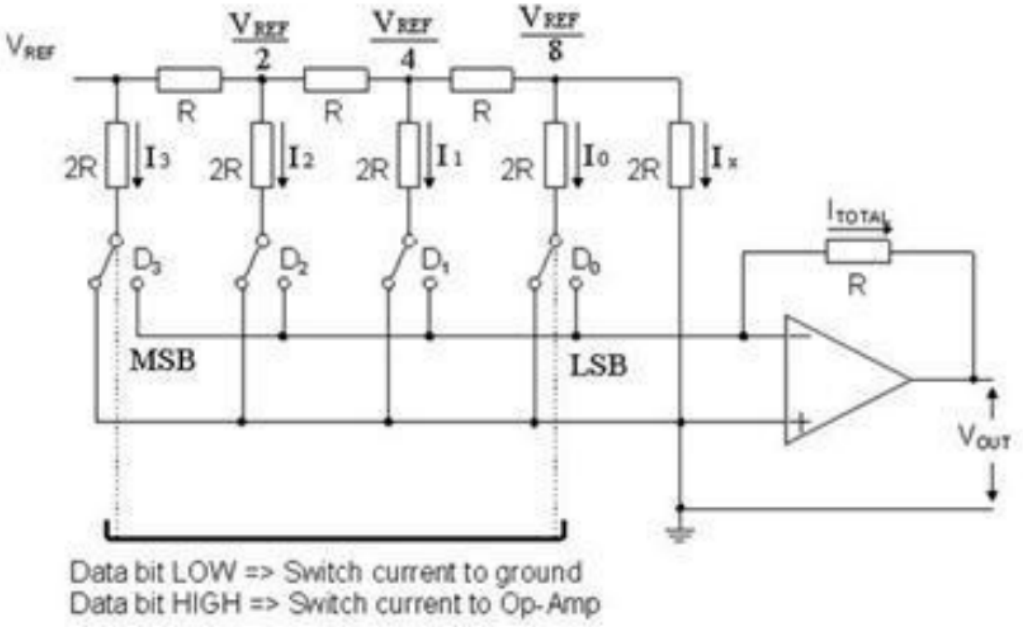

Fig 5.4 R-2R Ladder Network

- **Hybrid DACs**, which use a combination of the above techniques in a single converter. Most DAC integrated circuits are of this type due to the difficulty of getting low cost, high speed and high precision in one device.

- **Segmented DAC**, which combines the thermometer-coded principle for the most significant bits and the binary-weighted principle for the least significant bits. In this way, a compromise is obtained between precision (by the use of the thermo meter coded principle) and number of resistors or current sources (by the use of the binary weighted principle). The full binary-weighted design means 0% segmentation, the full thermometer-coded design means 100% segmentation.

5.5 DAC Performance

DACs are very important to system performance. The most important characteristics of these devices are:

- **Resolution**: This is the number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (21) levels while an 8 bit DAC is designed for 256 (28) levels. Resolution is related to the **effective number of bits** (ENOB) which is a measurement of the actual resolution attained by the DAC.

- **Maximum sampling frequency**: This is a measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem, a signal must be sampled at over twice the frequency of the desired signal. For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DACs that operate at over 40 kHz. The CD standard samples audio at 44.1 kHz, thus DACs of this frequency are often used. A common frequency in cheap computer sound cards is 48 kHz — many work at only this frequency, offering the use of other sample rates only through (often poor) internal re sampling.

- **Monotonicity:** This refers to the ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

- **THD+N**: This is a measurement of the distortion and noise introduced to the sign the DAC. It is expressed as a percentage of the total power of unwanted harmonic

distortion and noise that accompany the desired signal. This is a very important characteristic for dynamic and small signal DAC applications.

- **Dynamic range**: This is a measurement of the difference between the largest smallest signals the DAC can reproduce expressed in decibels. This is usually related DAC resolution and noise floor.

  Other measurements, such as phase distortion and sampling period instability, can also be very important for some applications.

5.6 DAC Ckt.

In this circuit, the digital output signal that is obtained from the encoder circuit is converted into an analog signal for allowing the further conversion of the current signal into the associated lower significant digital signals obtained from the IInd stage of the designed ADC i.e. B1 and B0.

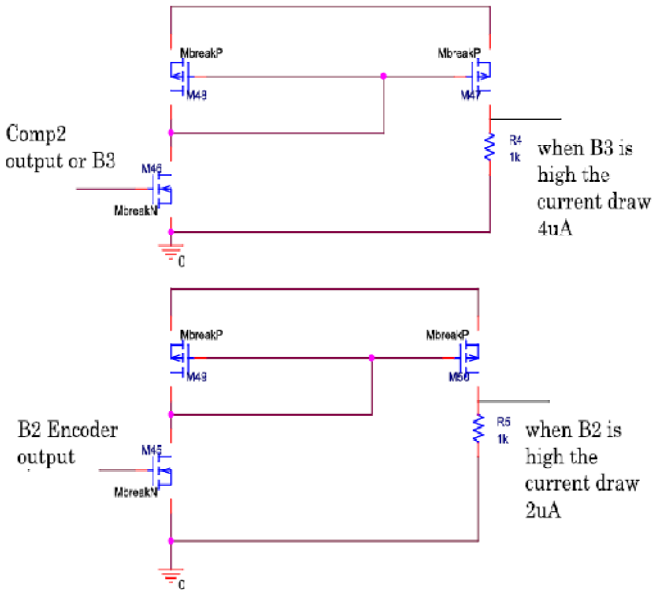

Fig 5.5 DAC Ckt.

Here, the digital signal either B3 or B2 from the output of the encoder of the Ist stage is fed into the DAC as input to the transistor M1. The transistor acts like a

switch. When B3 or B2 received is high then the transistor M1 receives sufficient base drive so as to act as a closed switch, thus allowing the current from the V_{dd} to pass through it to the ground. When the value of B3 or B2 signal received is low then the transistor doesn't receive the sufficient base drive and causes the transistor M1 to act as an open switch.

The transistorsM2, M3, M4 and M5 together make a current mirror circuit that are used to replicate the current that is passing through the drain of M1.Thus when the current is allowed to pass through the drain of M1 due to the transistor M1 acting as a closed switch then this same current is replicated at the output of drain of M5 and in case of the transistor M1 acting as an open switch there is no current present at the output of M5.

The value of the current to be allowed to pass through the drain of M1 on receiving a high B3 or B2 signal is decided by the proper selection of the transistor parameters W and L. For the design of the circuit, the output currents as per the inputs B3 and B2 corresponding to the following table:

DAC Output

B3/B1	B2/B0	DAC Current O/P
0	0	0
0	1	8
1	0	16
1	1	24

Table 5.1 DAC Output w.r.t Encoder output

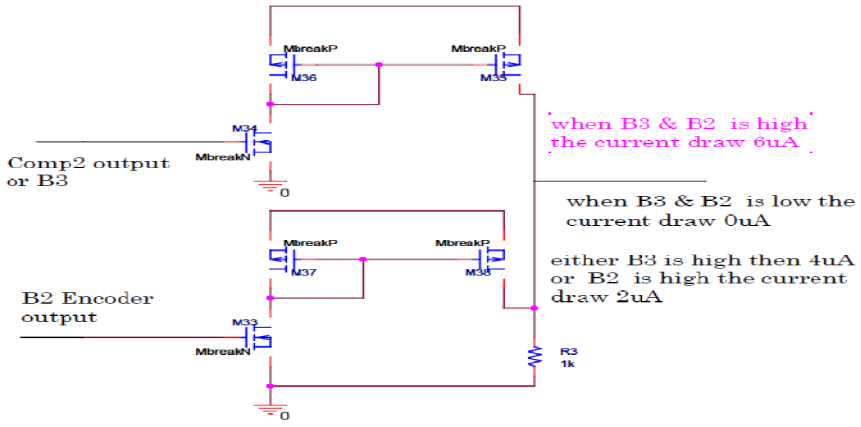

Fig 5.6 DAC Ckt. When both current are tied.

This circuit is simulated using CMOS 180nm technology parameters at voltage supply of 1.8V. The simulation results for the various inputs applied to the encoder are shown in next section.

5.7 Current Steering:

An improved current steering cell for a DAC which eliminates the need for an inverter reduces the noise at the common mode. The cell includes a first and a second current steering MOS transistor of a first polarity type, each having a gate and a pair of current passing terminals. The cell has an input terminal for receiving digital input signals coupled to the gate of the first of the pair of current steering transistors, and a common mode node for receiving an input current coupled to the same one of the pair of current passing terminals of each current steering MOS transistor. The current output terminal of the cell is coupled to the other of the pair of current passing terminals of the first of the current steering MOS transistors. Finally, the cell includes a third MOS transistor of the opposite polarity type to the current steering MOS transistors, having a gate and a pair of current passing terminals for passing a current through the transistor, the gate of the third MOS transistor being coupled to the gate of the first MOS current steering transistor, and the current passing terminals of the third MOS transistor being coupled between the gate of the second MOS current steering

transistor and one of the pair of current passing terminals of the second MOS current steering transistor.

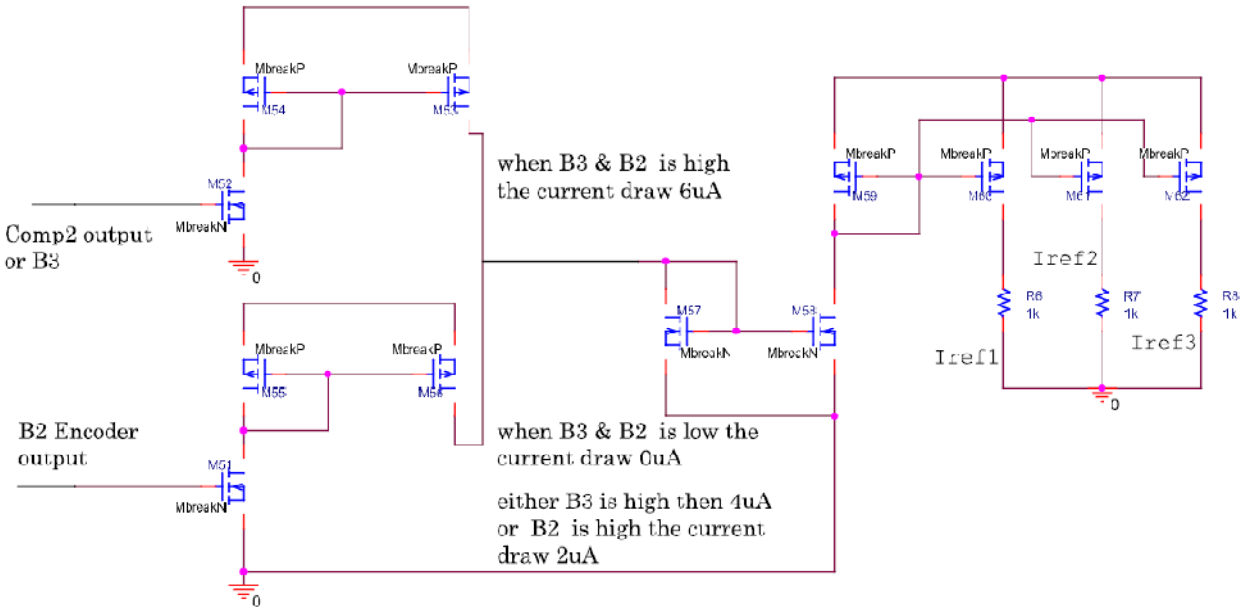

Fig 5.7 Current Steering

5.8 Simulation results

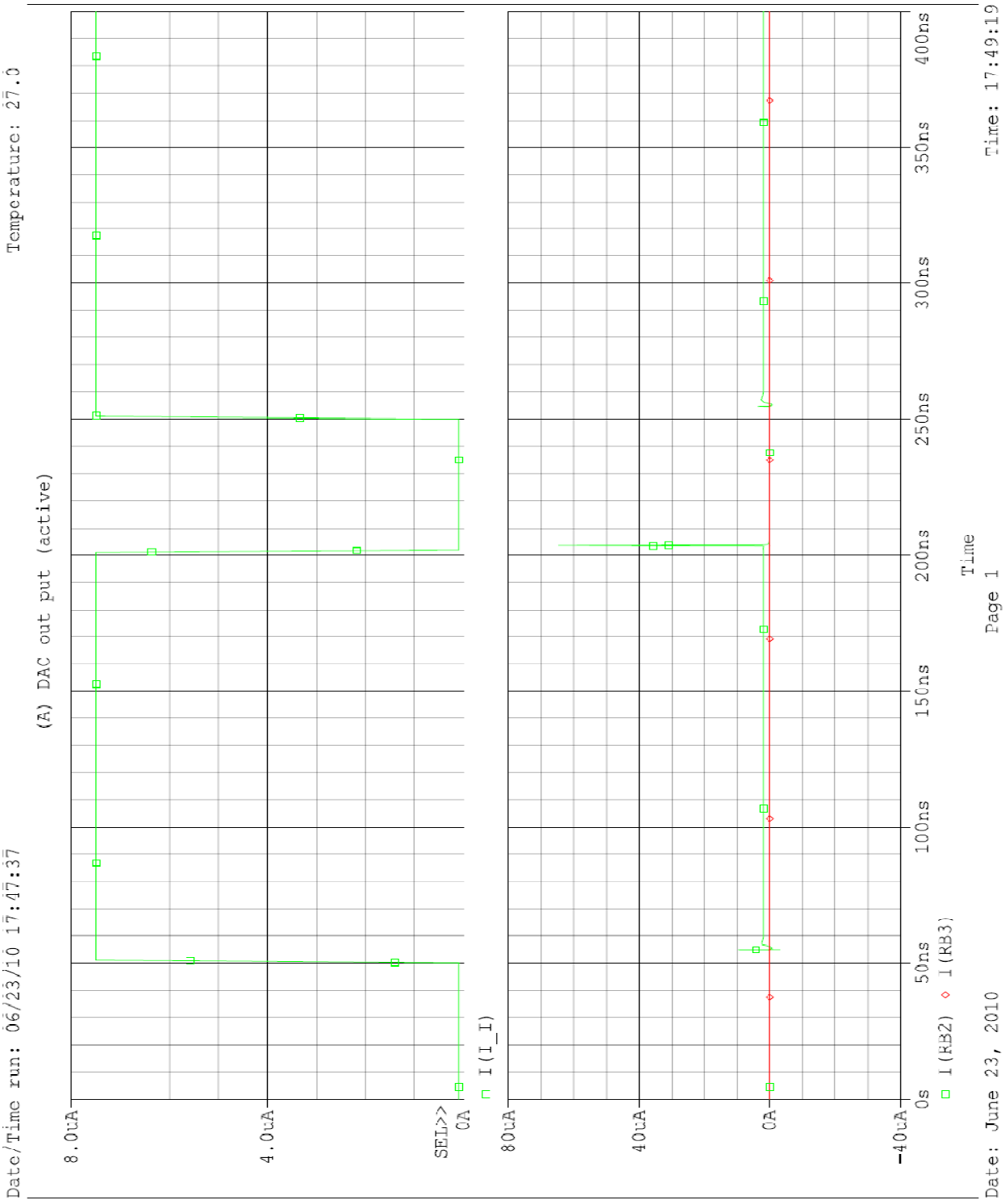

Fig 5.8 DAC 2uA/8 out put w.r.t to 7.5/30 Input Current.

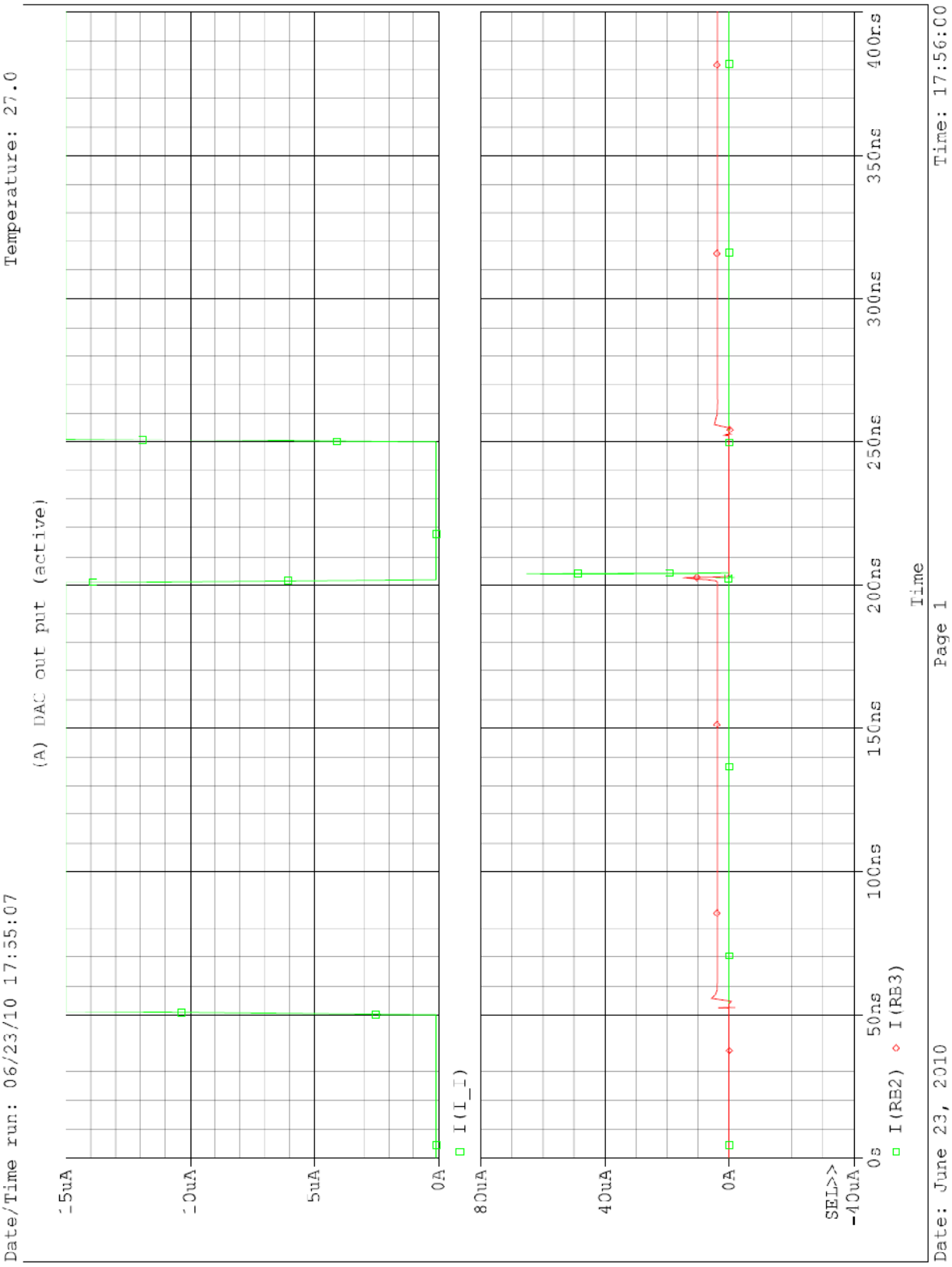

Fig 5.9 DAC 4uA/16 out put w.r.t to 15/60uA Input Current.

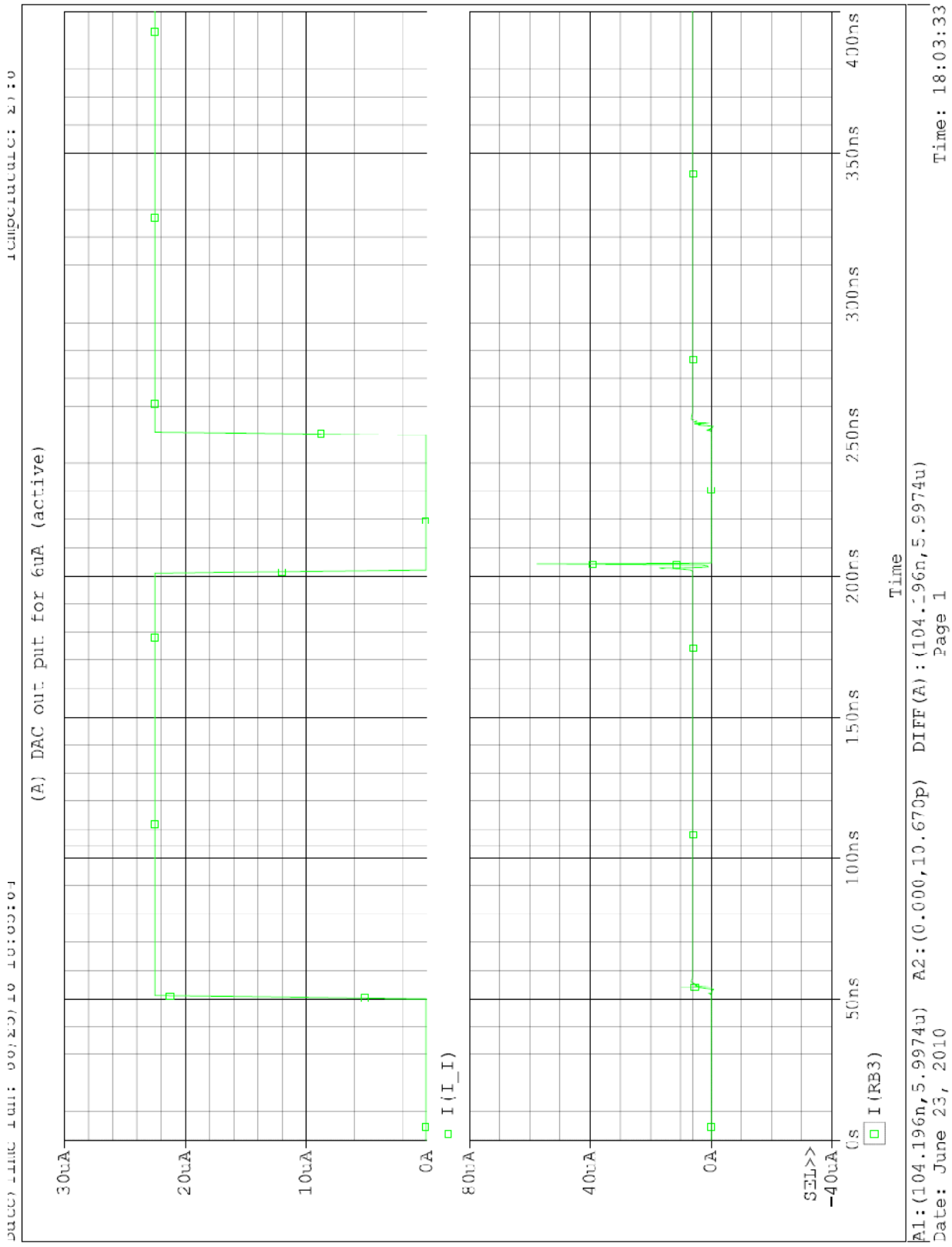

Fig 5.10 DAC 6/24uA out put w.r.t to 22.5uA/90 Input Current.

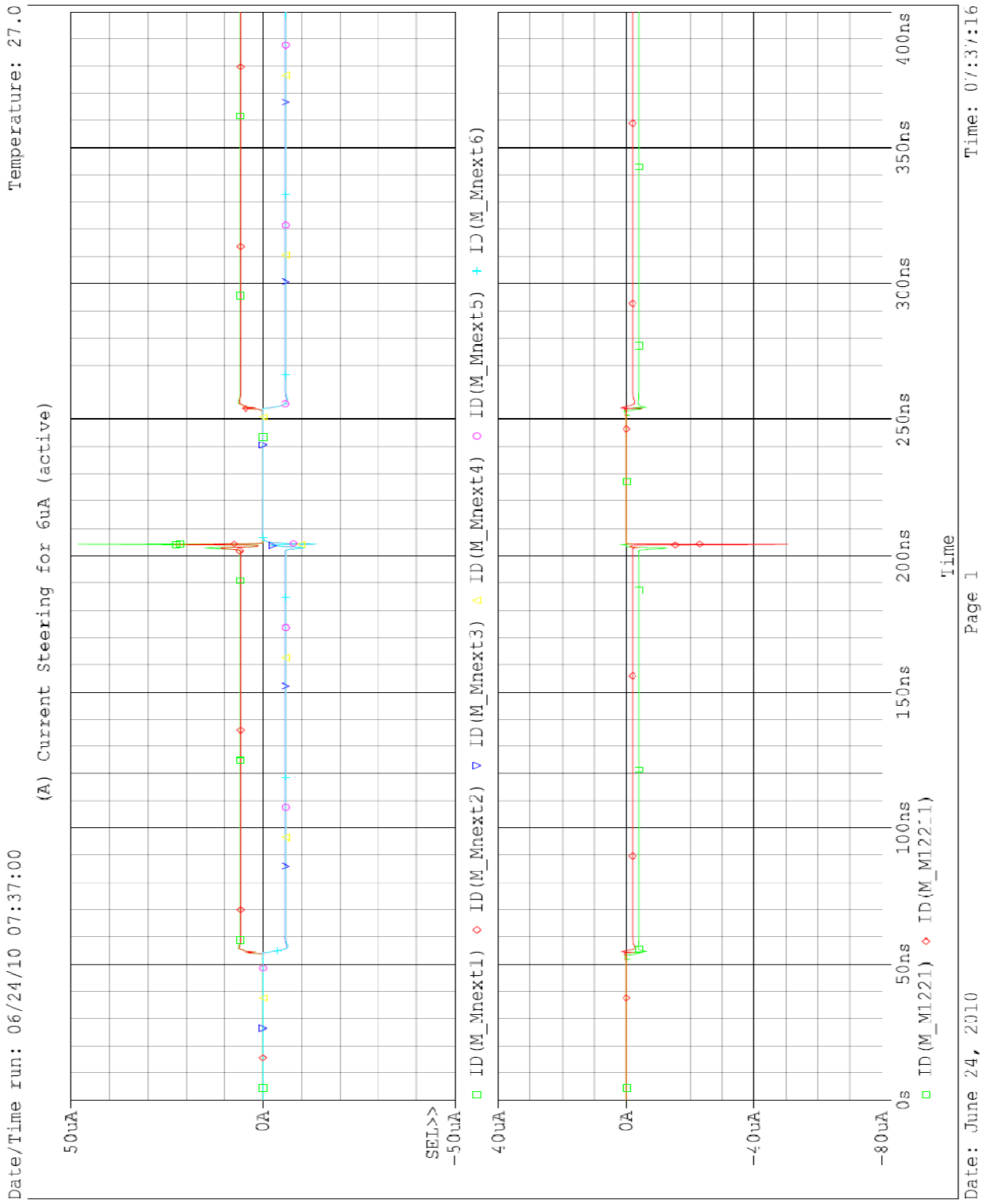

Fig 5.11 DAC 6/24uA out put w.r.t to 22.5uA/90 Input Current.

Chapter 6

ADC

6.1 Introduction

An area speed efficient method for analog to digital conversion is implemented in this thesis. This ASEADC, shown in Fig. 1, uses a Digital to Analog Converter (DAC). It is made of a combination of current comparators, DAC, and encoders. The conversion of four bits is performed in two stages.

6.2 ADC Step Size

In the first stage, most significant bits, $B3$ and $B2$, are generated from the analog input value (input current). The other two bits, $B1$ and $B0$, are produced in the second stage depending on the output values of the first stage. 2-bit generation at the same time decreases the total time of 4-bit conversion. Corresponding to each x-bit in digital output, there will be 2^x levels in analog input. For a 4-bit system with an input current in the range of ($M1$, $M2$), the minimum difference between each two levels, *step*, will be calculated as follows:

$$step = (M2 - M1)/(2^x - 1)$$

$$Step\ Size = 30\text{-}0/15 = 2uA$$

The advantage of using current mirror based comparator over the one in [8] is the reduced circuitry as it does not required current subtractor at input stage.

6.3 VALUES OF ALL CURRENTS IN THE ASEADC BLOCK DIAGRAM

Iref1	Iref2	Iref3
step × 2^2	step × 2^3	step × (2^2 + 2^3)
Iconst1	**Iconst2**	**Iconst3**
step × 2^0	step × 2^1	step × (2^0 + 2^1)

Table 6.1 Iref & Iconst

The ADC being presented here is obtained by cascading all the individual circuit discussed till now. This ADC accepts analog input in the form of current from any transducer or a system and after processing it as per the algorithm provides us with the binary equivalent of that signal information.

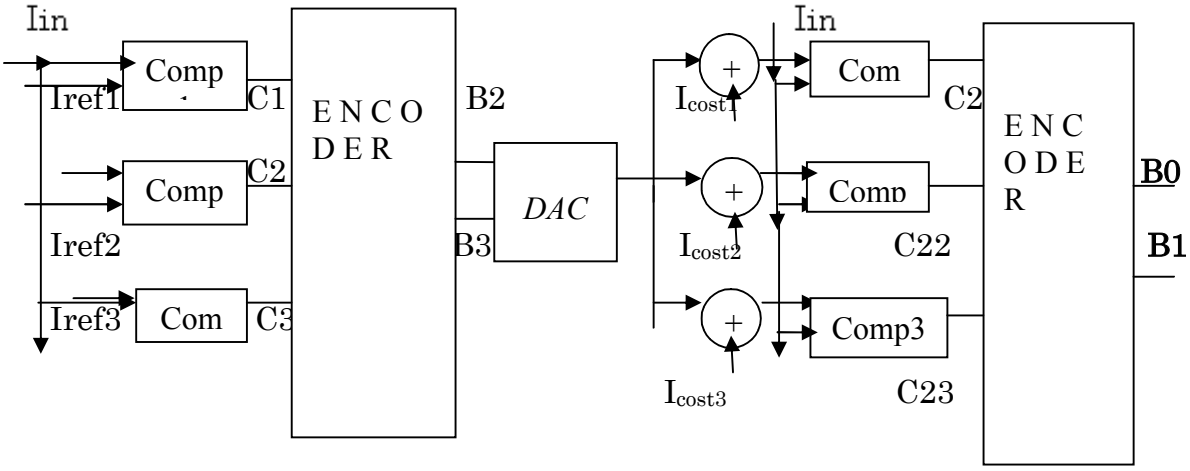

Fig 6.1 Area Speed Efficient Analog to Digital Convertor

The input to an A/D converter varies in a continuous manner between the minimum and maximum value. Using these minimum and maximum levels we divide the whole range into many threshold values which are considered as reference for comparing with the signal and thus help in the evaluation of the digital output. Step size is evaluated as:

$$Xth = \frac{Imax - Imin}{2}$$

Iref1	Iref2	Iref3
8uA	16uA	24uA

Table 6.2 For Reference Current

wheren= number of bit(s) at output. We assume that the input current signal coming from the transducer varies in range from 0μA to 30μA, thus providing threshold values of 2μA, 4μA, 8μA, ..., 30μA.

The proposed converter uses 2 stages, each stage for generating 2-bits. In stage-I input current Iin is compared with reference currents Iref (i=1,2,3) to generate comparator's output i.e- logic-1 or logic-0 when Iref < Iin, or Iin > Iref respectively. These logic outputs are then taken up by the encoder to provide M.S.B.(most significant bits) B3 and B2.

6.4 Reference Current for Stage – I.

For stage-II we first convert bits B3 and B2 to corresponding threshold currents using DAC Digital to Analog Converter) and then the two currents so obtained, 8μA and 16μA, are added and replicated to have three currents of same value using current steering circuit. To each a constant current Iconsti (i=1,2,3)(values given in the table 6.2) is added and the final values so obtained act as reference current for stage-II. Thus after comparing I_{in} and $I_{DAC} + I_{const}$ and encoding the comparator's output we get the remaining two bits LSB (Least Significant Bits) B1 and B0.

I_{const1}	I_{const2}	I_{const3}
2.0uA	4.0uA	6.0uA

Table 6.3 Constant Currents for Calculating Reference Currents for Stage – II

Thus in the presented Analog to Digital Converter the binary equivalent for a given signal is obtained in two successive stages. This requires less no of comparator when compared to parallel conversion procedure. Also this circuit is providing very less delay time and hence can be effectively used in the high speed signal processing applications.

6.5 ASEADC Operation

In the first stage, the analog input, *Iin*, is compared to constant reference currents, *Irefi* , through the current comparators, *Comp.i*, where $i = 1, 2, 3$. The output of *Comp.i* is 1 when *Iin* > *Irefi* and 0 otherwise. Due to the three current comparator outputs, the *Encoder*1 indicates whether each one of *B*3 and *B*2 is 1 or 0.

Comp. 3	Comp. 2	Comp. 1	B3	B2
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Table 6.4 B3 & B2 Output w.r.t Comp

From the above table,

$B3 = Comp.\ 1 \cdot Comp.\ 2$

$B2 = Comp.\ 1 \cdot (Comp.\ 2\ XNOR\ Comp.\ 3)$

From the above table, if the output of *Comp.i* is 1, the output of *Comp.j* would be also 1 because $Ij < Ii$ as long as $j < i$. Thus,

$B3 = Comp.\ 2$

$B2 = Comp.\ 3 + (Comp.\ 1 \cdot Comp.\ 2)$

In the second stage, the DAC generates a current corresponding to the values of *B*3 and *B*2 as follows:

B3B2	DAC output
00	0
01	$step \times 2^2$
10	$step \times 2^3$
11	$step \times (2^2+2^3)$

Table 6.5 Step Calculate for DAC Output

The DAC output current is added to each constant current values, *Iconsti*. The summation result is called the total reference current. The next three parallel current comparators compare the *Iin* to each of these total reference currents. Again, the output of *Comp.i* is 1 if *Iin* is greater than the total reference current.

*Encoder*2 decides the value of *B*1 and *B*0 exactly in the same way as *Encoder*1 does for *B*3 and *B*2, respectively. Thus, the equations of (3) can be rewritten for *Encoder*2 in order to extract *B*1 and *B*0 as follows:

$B1 = Comp.\ 2$

$B0 = Comp.\ 3 + (Comp.\ 1 \cdot Comp.\ 2)$

6.6 SIMULATION Steps

A 4-bit current mode ADC was designed and simulated based on the proposed ADCM. The circuit is designed for a current input between 0μA and 30μA.

The main building blocks of the simulated ADC are current comparator and DAC. The circuits used for these blocks are discussed in the following sub-sessions.

A. Current Comparator

To implement the ADCM, current-mirror current comparators are used. Fig. 3.3 shows the schematic of the employed current comparator.

B. Digital to Analog Converter

In this implementation, a 2-bit DAC is employed which generates a constant current corresponding to the two first converted bits, *B*3 and *B*2. The 2-bit DAC is a parallel combination of two 1-bit current mode DACs.

When the digital input is 1, a certain constant current is produced in the output. The current mirror transistors are weighted so that they can generate 0µA, 8µA, 16µA, and 24µA from digital inputs of 00, 01, 10, and 11, respectively. Fig.5.5 Shows the schematic of the DAC used in the ADCM.

6.7 Simulation Results:

I have verified many simulation results given below in the list and accordingly in the same manner simulation result.

1. Output1 0000 - 0001 bit
2. Output1 0001 - 0000 bit
3. Output1 0000 - 1100 bit
4. Output1 1000 - 0100 bit
5. Output1 1000 -11 00 bit
6. Output1 1100 - 0000 bit
7. Output1 1100 - 0100 bit
8. Output1 1111 - 0000 bit
9. Output1 1111 - 0001 bit
10. Output1 1111 - 0100 bit
11. Output1 1111 - 1000 bit
12. Output1 1111 - 1100 bit
13. Output1 0000 - 1111 bit
14. Output1 0100 - 1000 bit
15. Output1 0100 - 1111 bit

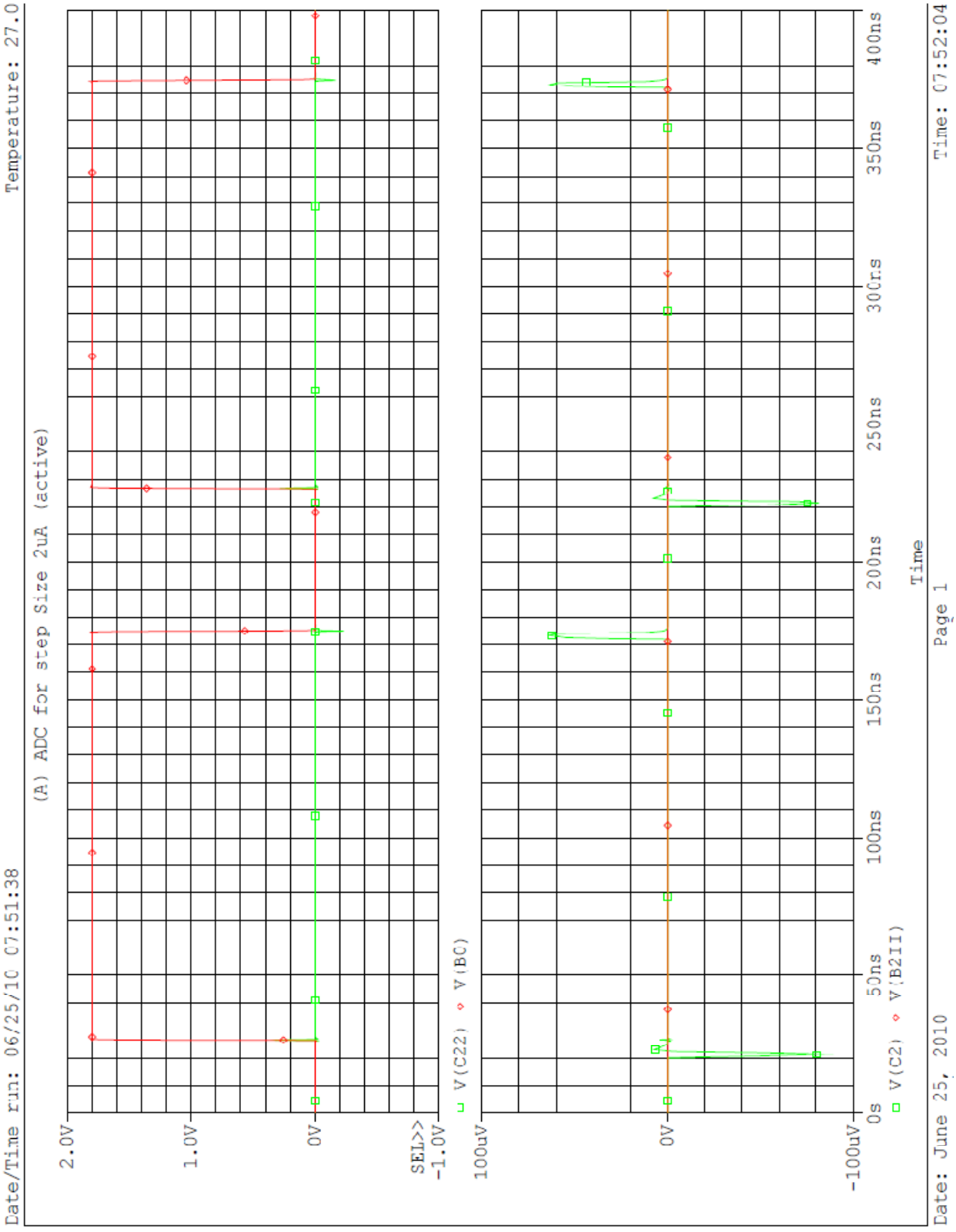

Fig 6.2 ADC Bit Change Output1 0000 - 0001 bit

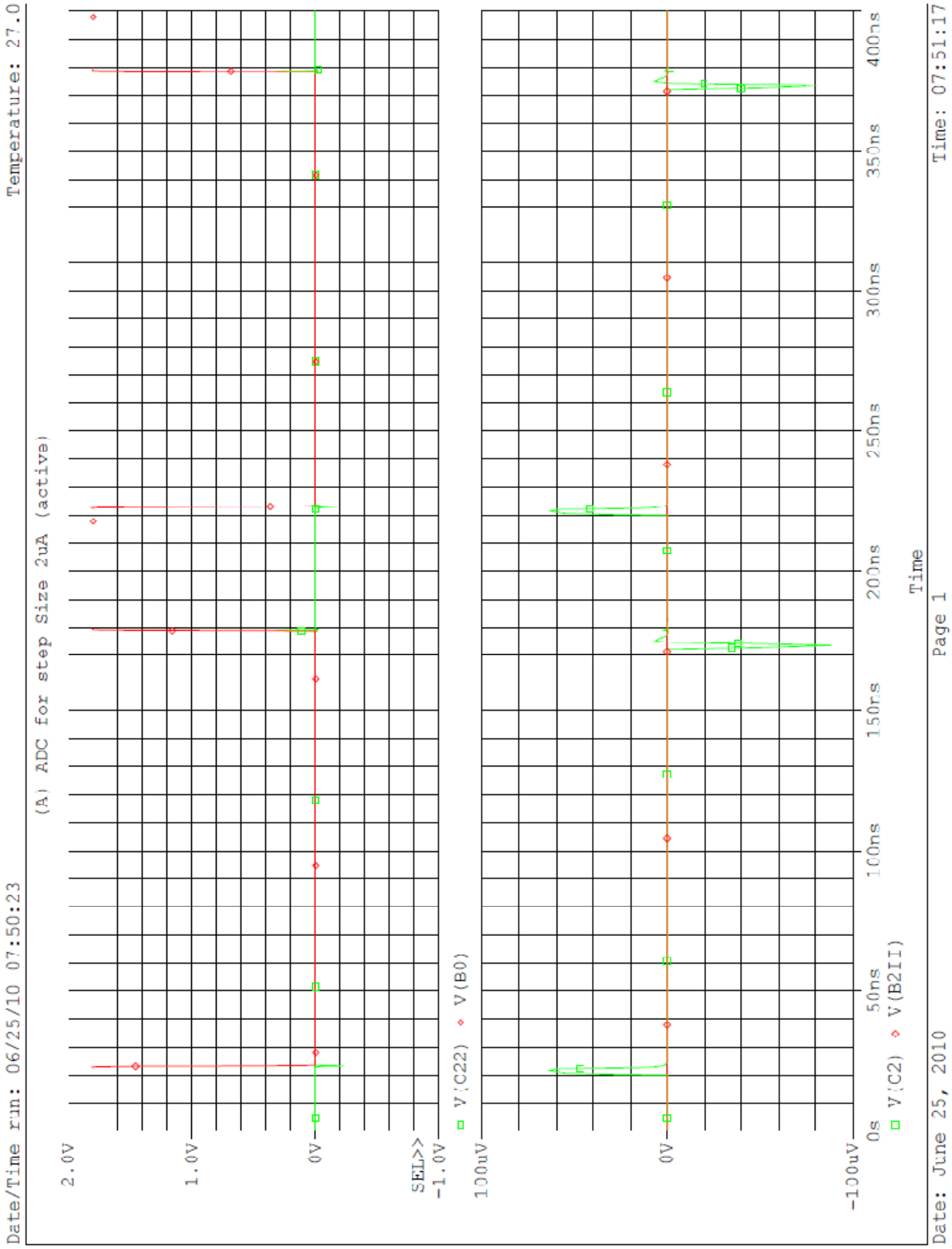

Fig 6.3 ADC Bit Change Output1 0001 - 0000 bit

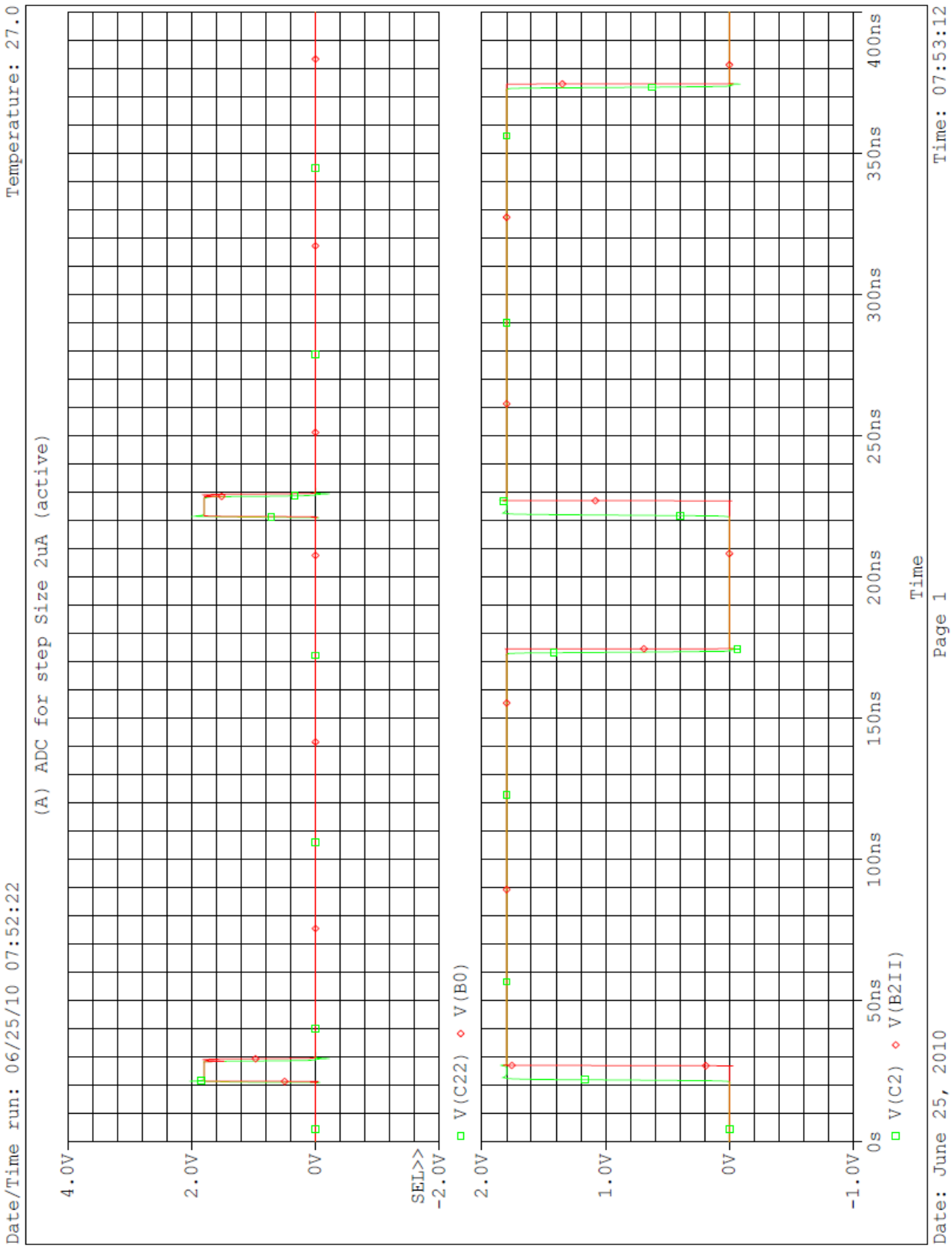

Fig 6.4 ADC Bit Change Output1 0000 - 1100 bit

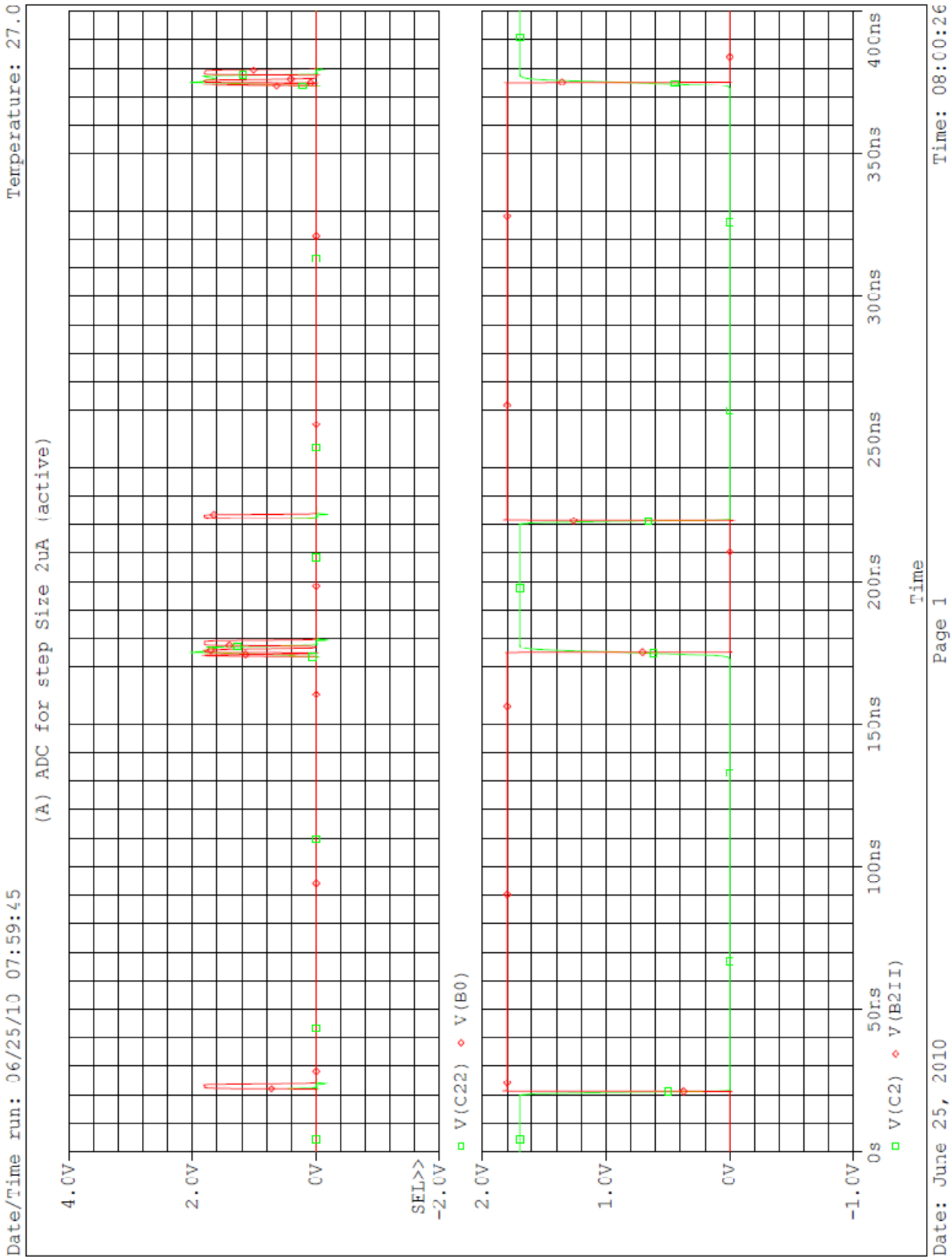

Fig 6.5 ADC Bit Change Output1 1000 - 0100 bit

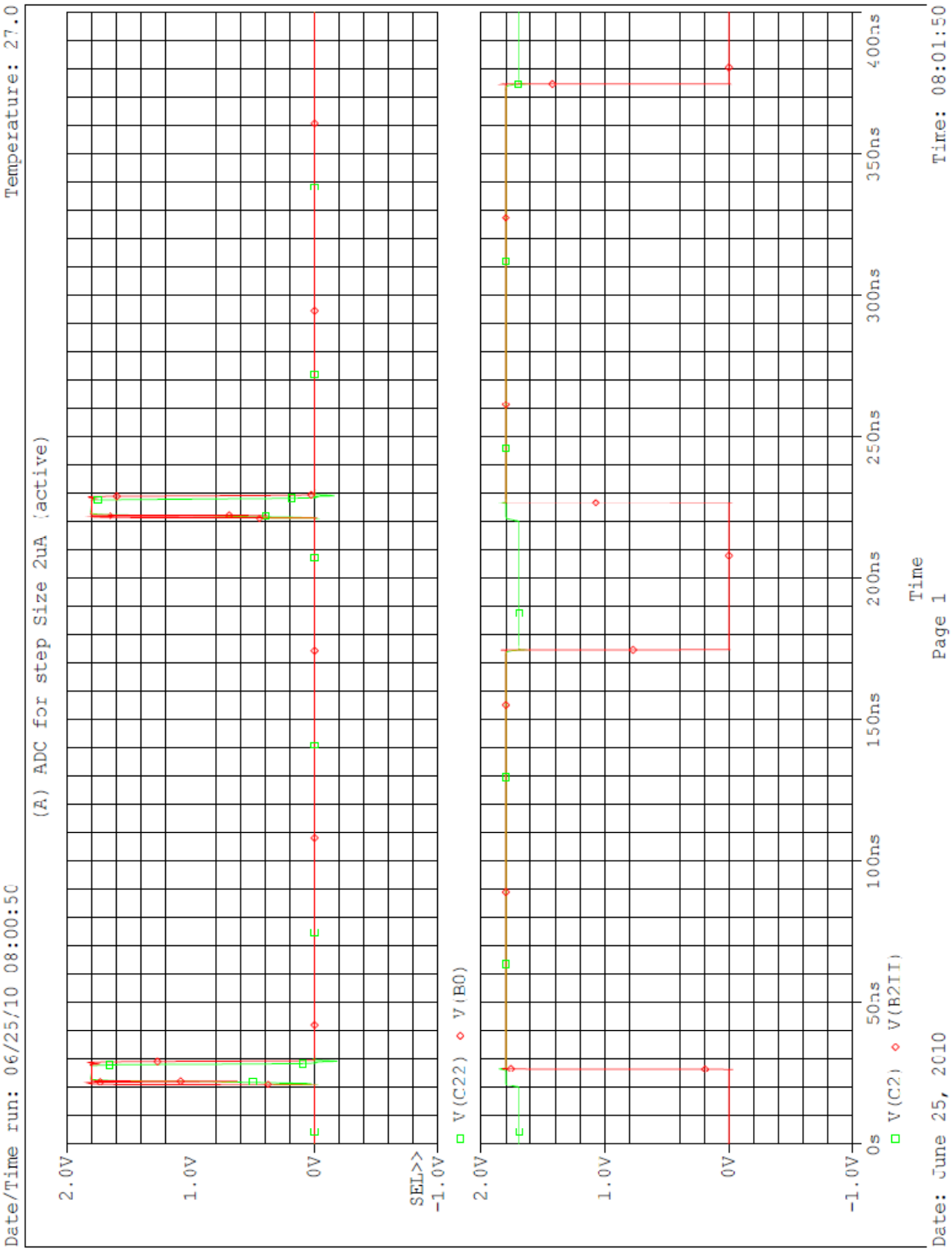

Fig 6.6 ADC Bit Change Output1 1000 - 1100 bit

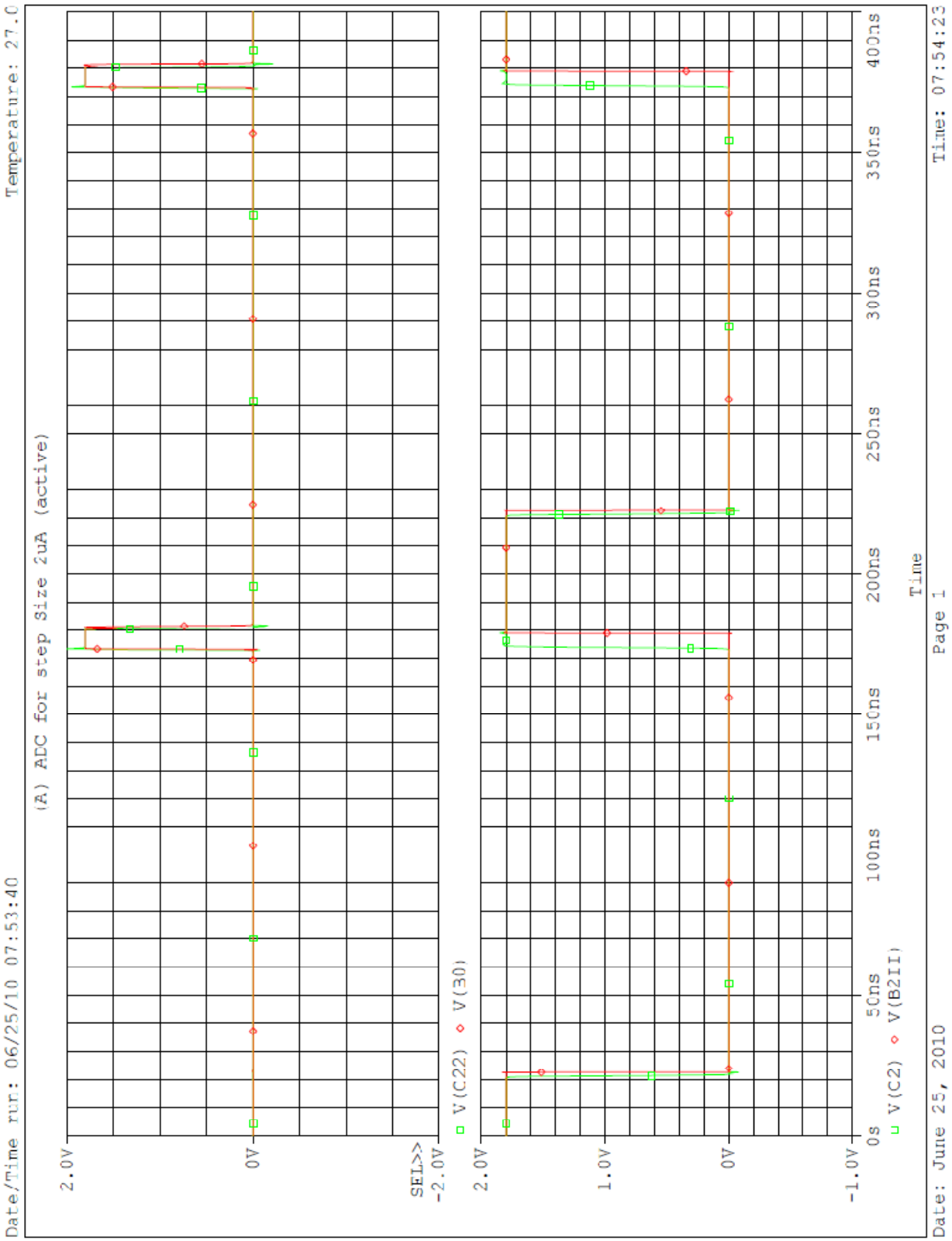

Fig 6.7 ADC Bit Change Output1 1100 - 0000 bit

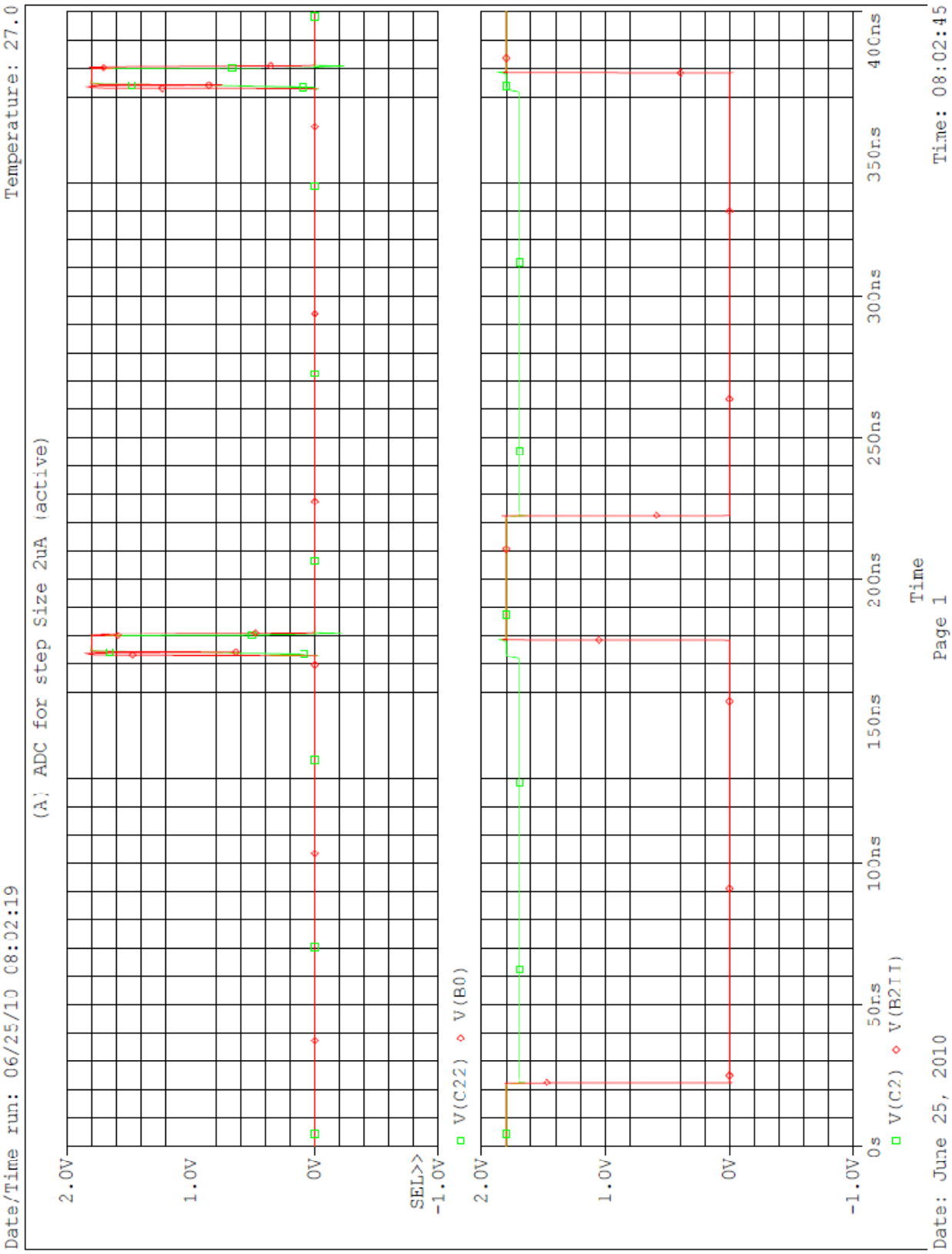

Fig 6.8 ADC Bit Change Output1 1100 - 0100 bit

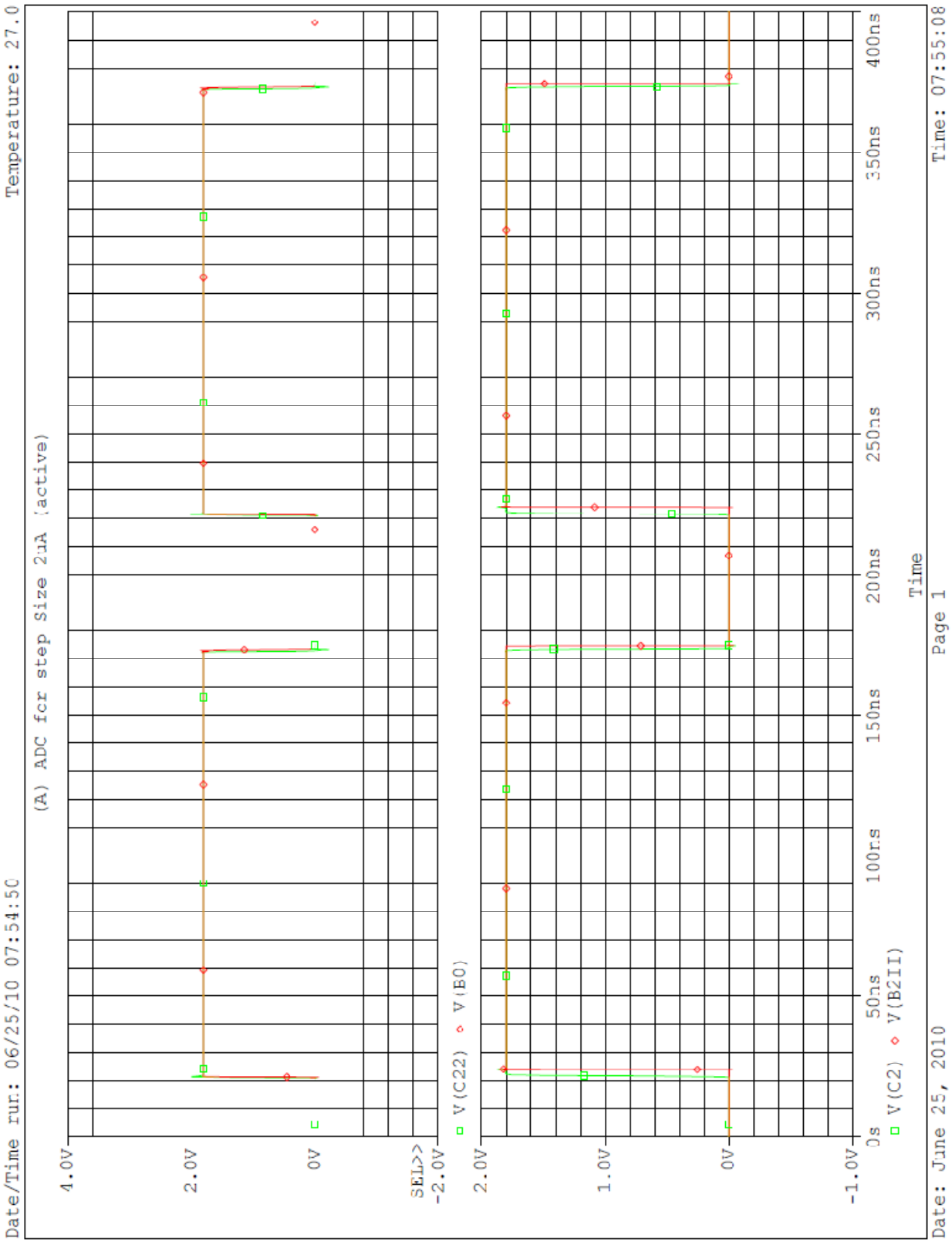

Fig 6.9 ADC Bit Change Output1 1111 - 0000 bit

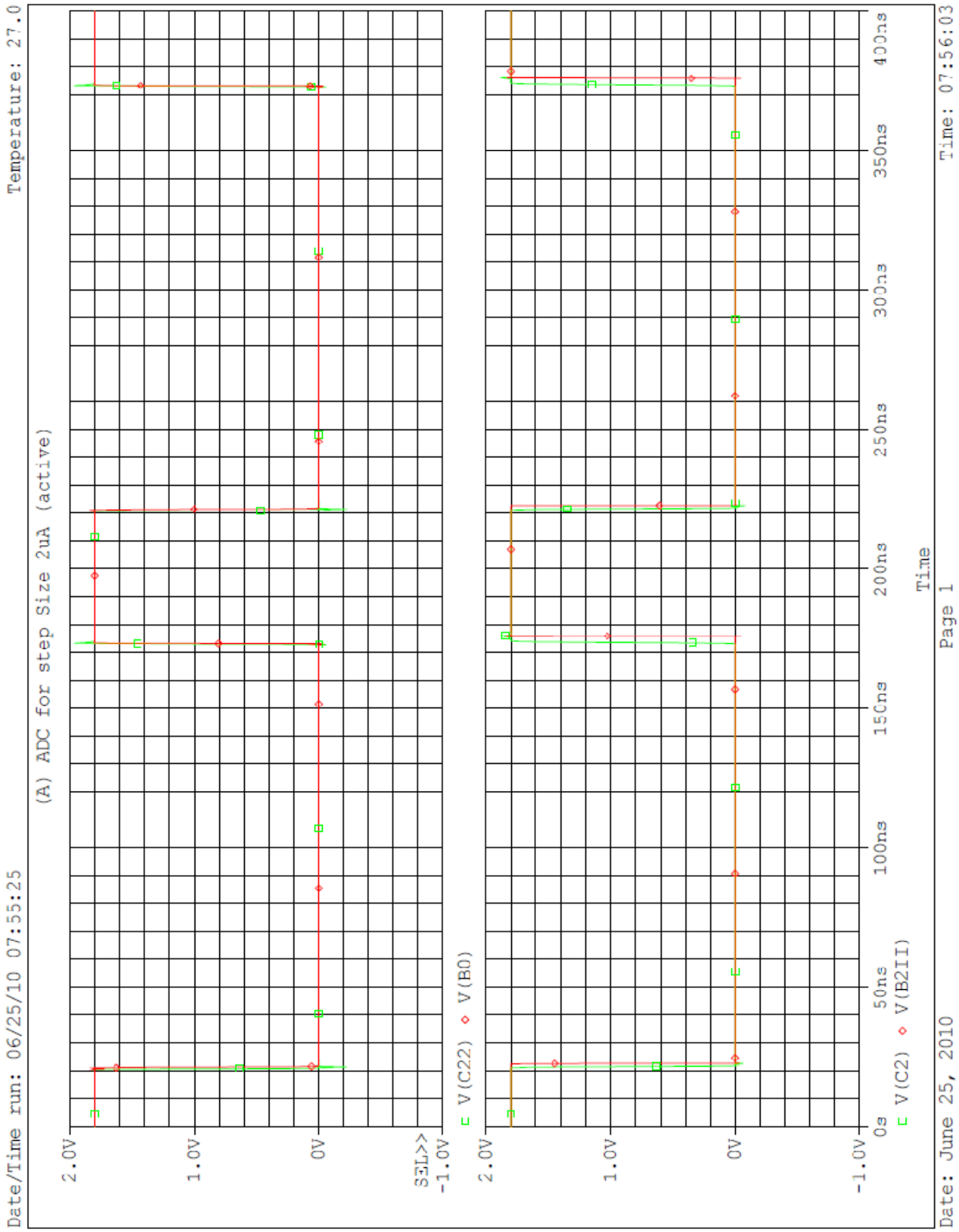

Fig 6.10 ADC Bit Change Output1 0000 - 1111 bit

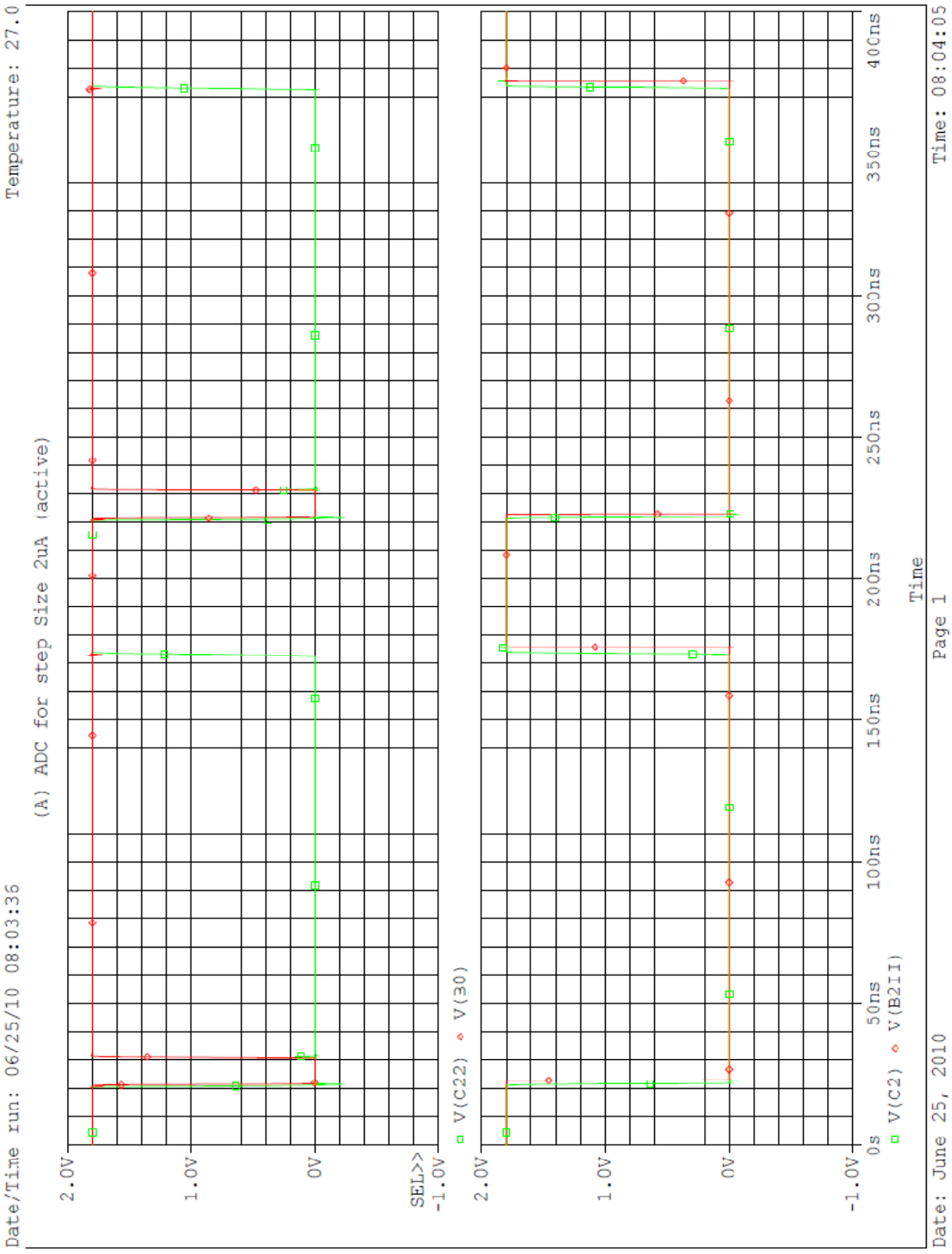

Fig 6.11 ADC Bit Change Output1 1111 - 0001 bit

Chapter 7

Conclusion and future scope

In this project, realization of area speed efficient Analog to Digital Converter (ASEADC), a fast and area efficient method for analog to digital conversion is done. It serves as an efficient alternative in designing current mode ADCs. This method has a parallel configuration and provides two bits at the same time resulting in a high conversion speed. The simulated result shows that characteristics of the designs are in good agreement with the literature. Further, the minimum numbers of gates are used in the implementation of DAC as compared to the other existing structures. This feature makes the implemented ADC less area consuming. A 4 -bit ASEADC is simulated using the 180nm CMOS technology parameters and is giving satisfactory results. A 6-bit ASEADC can be designed using 7 comparators in each the two stages, which is not being implemented in paper.

References

[1]. J. Sarao, and H.H.L. Kwok University of Victoria, Canada.Current Mode Building and Blocks and Their Application in ADC

[2]. D. A. Freitas and K. W. Current, "CMOS current comparator circuit", *Electronics Letters,* Aug. 1983, vo1.28, no.3, pp. 695-697.

[3]. Z.-H. Kong, K.-S. Yeo and C.-H. Chang, Design of an Area efficient CMOS multiple-valued current comparator circuit, IEE Proceedings online no. 041137 doi:10.1049/ip-cds:200 41137 IEE Proc.-Circuits Devices Syst., Vol. 152, No. 2, April 2005

[4]. Sobot, R Current -mode multiple valued logic circuits in digital CMOS technology'. Master's t he sis, Simon Fraser University, Canada, 1996

[5]. Current, K.W.: 'Current-mode CMOS multiple-valued logic circuits,' IEEE J. Solid-State Circuits, 1994, 29, (2) , pp. 95–107

[6]. Chunyan, W., Ahmad, M.O., and Swamy, M.N .S.: 'Low- power current comparator cell for weak current operations'. IEEE Int. Sympon Circuits and Systems, 2001, Vol. 1, pp. 544–547

[7]. Giustolisi, G., Palumbo, G., and Pennisi, S .: 'Resolution of a current mode algorithmic analog-to-digital converter', IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., 2002, 49, (10), pp. 1480–1486

[8]. Golnar Khodabndehloo, Mitra Mirhassani and Majid Ahmadi An Area-Speed Efficient Method for Current Mode Analog to Digital Converters Research Centre for Integrated Microsy stems Electrical and Computer Engineering Department University of Windsor, ON, N9B 3P4 Email: khodaba@u windsor.ca 978-1-4244-3896-9/09/$25.00 ©2009 IEEE.

[9]. H. Traff, *Novel approach to high speed CMOS current comparators* Electronics Letters , Vol. 28, No. 3 , pp. 310-312, 1992.

[10] D. G. Nairn and C. A. T. Salama, *A current mode algorithmic analog to-digital converter* , IEEE International Symposium on Circuits and System s , Vol. 3, pp. 2573-2576, 1988.

[11]. C. Wu and Y. Liow, *New current mode wave-pipelined architectures for high-speed analog -to-digital converters* , IEEE Transactions on Circuits and System s I, Vo l. 51, pp. 25-37, 2004.

[12]. S. Chuenarom and V. Tipsuwarnpron, *Application Techniques for High Performance A DC*, International Symposium on Communications and Information Technologies , pp. 749-752 , 2006.

[13 D. G. Nairn and C. A. T. Salama, *current mode algorithmic analog –to digital converters* , IEEE Journal o f Solid-State Circuits , Vol. 25, No. 4 , pp. 997-1004, 1990.

[14]. M . Conti, P. Crippa, S . Orcioni, C . Turchetti, and S . Scolastr a, *A current mode multilevel memory using flash A /D converters* , T he 6th IEEE International Conference on Electronics , Circuits and System s , Vol. 3 , pp. 1627 - 1630, 1999.

[15]. A . Agarwal, Y. B. Kim , and S. Sonkusale, *Low power current m ode A D C for CMOS sensor IC*, IEEE International Symposium on Circuits and Systems , Vol. 1 , pp. 584-587, 2005.

[16]. R. Dlugosz and K.Iniewski, *Ultra Low Power Current-mode Algorithmic Analog -to-digital Converter Implemented In 0. 18 /s pl mu/m CMOS Technology For Wireless Sensor Network*, Proceedings of the International Conference on Mixed Design of Integrated Circuits and System , pp. 22-24, 2006.

Model Parameter of CMOS 180nm Technology for PSpice

```
.MODEL NMOS NMOS (                          LEVEL   = 7
+ TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17     VTH0    = 0.3750766
+K1      = 0.5842025    K2      = 1.245202E-3   K3      = 1E-3
+K3B     = 0.0295587    W0      = 1E-7          NLX     = 1.597846E-7
+DVT0W   = 0            DVT1W   = 0             DVT2W   = 0
+DVT0    = 1.3022984    DVT1    = 0.4021873     DVT2    = 7.631374E-3
+U0      = 296.8451012  UA      = -1.179955E-9  UB      = 2.32616E-18
+UC      = 7.593301E-11 VSAT    = 1.747147E5    A0      = 2
+AGS     = 0.452647     B0      = 5.506962E-8   B1      = 2.640458E-6
+KETA    = -6.860244E-3 A1      = 7.885522E-4   A2      = 0.3119338
+RDSW    = 105          PRWG    = 0.4826        PRWB    = -0.2
+WR      = 1            WINT    = 4.410779E-9   LINT    = 2.045919E-8
+XL      = 0            XW      = -1E-8         DWG     = -2.610453E-9
+DWB     = -4.344942E-9 VOFF    = -0.0948017    NFACTOR = 2.1860065
+CIT     = 0            CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0            ETA0    = 1.991317E-3   ETAB    = 6.028975E-5
+DSUB    = 0.0217897    PCLM    = 1.7062594     PDIBLC1 = 0.2320546
+PDIBLC2 = 1.670588E-3  PDIBLCB = -0.1          DROUT   = 0.8388608
+PSCBE1  = 1.904263E10  PSCBE2  = 1.546939E-8   PVAG    = 0
+DELTA   = 0.01         RSH     = 7.1           MOBMOD  = 1
+PRT     = 0            UTE     = -1.5          KT1     = -0.11
+KT1L    = 0            KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0            WLN     = 1             WW      = 0
+WWN     = 1            WWL     = 0             LL      = 0
+LLN     = 1            LW      = 0             LWN     = 1
+LWL     = 0            CAPMOD  = 2             XPART   = 0.5
+CGDO    = 6.7E-10      CGSO    = 6.7E-10       CGBO    = 1E-12
```

```
+CJ     = 9.550345E-4    PB     = 0.8          MJ     = 0.3762949
+CJSW   = 2.083251E-10   PBSW   = 0.8          MJSW   = 0.1269477
+CJSWG  = 3.3E-10        PBSWG  = 0.8          MJSWG  = 0.1269477
+CF     = 0              PVTH0  = -2.369258E-3  PRDSW  = -1.2091688
+PK2    = 1.845281E-3    WKETA  = -2.040084E-3  LKETA  = -1.266704E-3
+PU0    = 1.0932981      PUA    = -2.56934E-11  PUB    = 0
+PVSAT  = 2E3            PETA0  = 1E-4         PKETA  = -3.350276E-3   )
*
.MODEL PMOS PMOS (                              LEVEL  = 7
+ TNOM   = 27             TOX    = 4.1E-9
+XJ     = 1E-7           NCH    = 4.1589E17     VTH0   = -0.3936726
+K1     = 0.5750728      K2     = 0.0235926     K3     = 0.1590089
+K3B    = 4.2687016      W0     = 1E-6          NLX    = 1.033999E-7
+DVT0W  = 0              DVT1W  = 0             DVT2W  = 0
+DVT0   = 0.5560978      DVT1   = 0.2490116     DVT2   = 0.1
+U0     = 112.5106786    UA     = 1.45072E-9    UB     = 1.195045E-21
+UC     = -1E-10         VSAT   = 1.168535E5    A0     = 1.7211984
+AGS    = 0.3806925      B0     = 4.296252E-7   B1     = 1.288698E-6
+KETA   = 0.0201833      A1     = 0.2328472     A2     = 0.3
+RDSW   = 198.7483291    PRWG   = 0.5           PRWB   = -0.4971827
+WR     = 1              WINT   = 0             LINT   = 2.943206E-8
+XL     = 0              XW     = -1E-8         DWG    = -1.949253E-8
+DWB    = -2.824041E-9   VOFF   = -0.0979832    NFACTOR = 1.9624066
+CIT    = 0              CDSC   = 2.4E-4        CDSCD  = 0
+CDSCB  = 0              ETA0   = 7.282772E-4   ETAB   = -3.818572E-4
+DSUB   = 1.518344E-3    PCLM   = 1.4728931     PDIBLC1 = 2.138043E-3
+PDIBLC2 = -9.966066E-6   PDIBLCB = -1E-3        DROUT  = 4.276128E-4
+PSCBE1  = 4.850167E10    PSCBE2 = 5E-10         PVAG   = 0
+DELTA  = 0.01           RSH    = 8.2           MOBMOD = 1
+PRT    = 0              UTE    = -1.5          KT1    = -0.11
```

```
+KT1L    = 0           KT2     = 0.022        UA1     = 4.31E-9
+UB1     = -7.61E-18   UC1     = -5.6E-11     AT      = 3.3E4
+WL      = 0           WLN     = 1            WW      = 0
+WWN     = 1           WWL     = 0            LL      = 0
+LLN     = 1           LW      = 0            LWN     = 1
+LWL     = 0           CAPMOD  = 2            XPART   = 0.5
+CGDO    = 7.47E-10    CGSO    = 7.47E-10     CGBO    = 1E-12
+CJ      = 1.180017E-3 PB      = 0.8560642    MJ      = 0.4146818
+CJSW    = 2.046463E-10 PBSW   = 0.9123142    MJSW    = 0.316175
+CJSWG   = 4.22E-10    PBSWG   = 0.9123142    MJSWG   = 0.316175
+CF      = 0           PVTH0   = 8.456598E-4  PRDSW   = 8.4838247
+PK2     = 1.338191E-3 WKETA   = 0.0246885    LKETA   = -2.016897E-3
+PU0     = -1.5089586  PUA     = -5.51646E-11 PUB     = 1E-21
+PVSAT   = 50          PETA0   = 1E-4         PKETA   = -3.316832E-3  )
*
```