Design of Energy-Efficient and Radiation-Tolerant Latches

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by

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CERTIFICATE

This is to certify that the thesis entitled **"Design of Energy-Efficient and Radiation-Tolerant Latches"**, submitted by **Niraj Kumar** (23/PhDECE/01) to the Department of Electronics & Communication Engineering, Delhi Technological University, for the award of the degree of **Doctor of Philosophy** is a record of the original, bona fide research work carried out by him under my supervision and guidance. The thesis has reached the standards fulfilling the requirements of the regulations related to the award of the degree.

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I **Niraj Kumar** hereby certify that the work which is being presented in the thesis entitled **"Design of Energy-Efficient and Radiation-Tolerant Latches"** in partial fulfillment of the requirements for the award of the Degree of **Doctor of Philosophy**, submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from **July 2023 to September 2026** under the supervision of **Prof. Neeta Pandey** and **Dr. Chaudhary Indra Kumar**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

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ABSTRACT

The evolution of modern integrated circuits (ICs) has profoundly transformed human life. Today, ICs play an essential role in critical systems such as medical instruments, self-driving vehicles, aircraft navigation, and satellites. Ensuring the reliability of these systems has therefore become a key concern. One of the most serious concerns for ICs reliability is the occurrence of soft errors (SEs). As semiconductor technology continues to scale down, circuits become increasingly susceptible to such transient faults (TFs). These errors are typically triggered when radiation particles strike the ICs and produce current pulses that disrupt its normal operation. The resulting disturbances can corrupt stored data and, in severe cases, cause system failures. For instance, if SE occurs in a medical device during surgery, it could lead to malfunction and interrupt the procedure. Similarly, an error in the control logic of an autonomous vehicle might result in an accident, or a disturbance in an aircraft's navigation system could compromise flight safety. Even though some malfunctions may be resolved by resetting the system, the downtime during recovery could have critical consequences. In satellite control systems, SE might prevent the satellite from maintaining its orbit, causing it to descend and eventually burn up in the Earth's atmosphere. Therefore, protecting integrated circuits against SEs is crucial for maintaining the reliability and safety of critical applications.

Numerous techniques have been developed to enhance the tolerance of ICs against SEs. Among various circuit components, memory and storage elements such as latches and flip-flops are particularly susceptible to these TFs, as the data stored in them are vital for correct circuit functionality. To overcome above issues, radiation hardened latch by design (RHBD) is used, improving resilience by incorporating redundant feedback paths that store identical data and using a voter circuit to determine the correct output. Several advanced hardened latch architectures have been introduced in recent years, demonstrating strong resistance to SEs and reliable performance under radiation effects. This thesis proposes five novel radiation hardened designs to address this problem. The first proposed design seven transistor Schmitt Trigger (STST) latch against radiation effects involves increasing the capacitance at sensitive nodes by incorporating an additional STST block. It exhibits a high critical charge to power delay area product (PDAP) ratio called (QPAR) due to lower transistor count and node capacitance. The second design four transistor Schmitt Trigger (FTFT) latch is capable of withstanding and recovering from single node

upsets (SNUs) with higher QPAR due to lower transistor count than first proposed design STST. The third design triple node upset radiation hardened latch (TNURH) uses Muller C-elements (MCEs) and capability to recover SNUs, double node upset (DNUs), and triple node upset (TNUs) at all of its sensitive nodes. The QPAR value is high because of its shorter delay (due to wider transmission gate), low power usage (due to clocked MCEs), and compact area. The fourth design cascode Schmitt Trigger and Muller C-element based triple node upset radiation hardened (CSTCE-TNURH) latch, uses STST and MCE to recover SNUs, DNUs, and TNUs. It has higher QPAR than third design TNURH due to less number of transistor used.

The performance and power efficiency of radiation hardened latches utilising complementary metal oxide semiconductor (CMOS) in lower technology nodes deteriorate due to secondary effects and variances in the manufacturing process. As a result, FinFET technology emerges as a viable choice for attaining better performance. Replacing metal oxide semiconductor field effect transistors (MOSFETs) with FinFETs in digital circuit design allows for smaller layouts and improved reliability. FinFETs deliver higher ON currents than MOSFETs of the same size. Moreover, since the channel width in FinFETs can be controlled by varying the fin height, they offer a denser structure compared to planar MOSFETs. To solve secondary effects issue, novel fifth design double node upset radiation hardend Muller C-element and Schmitt Trigger (MCEST) based design is proposed in this thesis. The proposed MCEST latch exhibits robustness against both SNUs and DNUs at its sensitive nodes. It achieves a high critical charge to power delay product (PDP) ratio, due to its reduced node capacitance and lower transistor count. The performance of each of the proposed designs is examined and contrasted in the thesis using standard latch metrics. The proposed designs (2, 3, 4) functionality has been verified by simulations conducted in Cadence Virtuoso utilizing 45 nm CMOS technology. Additionally, 7 nm FinFET model is used to validate the performance of FinFET based latches. Overall, this thesis provides an in-depth study and development of radiation hardened latches with a focus on enhancing stability, improving power consumption, and resilience to SEs. By employing novel circuit strategies and alternate device and performance evaluation through extensive simulations, the findings offer meaningful contributions toward the realization of high-speed, energy-efficient, and dependable memory solutions suitable for low-power and high speed mordern electronic applications.

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Abbreviations

BTI	**B**ias **T**emperature **I**nstability
CFTST	**C**ascode **F**our **T**ransistor **S**chmitt **T**rigger
CGI	**C**lock **G**ated **I**nverter
CG-MCE	**C**lock **G**ated **M**uller **C**-**E**lement
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CNTFET	**C**arbon **N**anotube **F**ield **E**ffect **T**ransistor
CSTCE-TNURH	**C**ascode **S**chmitt **T**rigger and **C**-**E**lement based **T**riple **N**ode **U**pset **R**adiation **H**ardened
CSTs	**C**ascode **S**chmitt **T**riggers
CSTST	**C**ascode **S**even **T**ransistor **S**chmitt **T**rigger
DLEI	**D**ouble **L**evel **E**rror **I**nterception
DNU	**D**ouble **N**ode **U**pset
ECC	**E**rror **C**orrection **C**ode
EHPs	**E**lectron-**H**ole **P**airs
ELTs	**E**nclosed **L**ayout **T**ransistors
FinFET	**Fin** **F**ield-**E**ffect **T**ransistor
FTST	**F**our **T**ransistor **S**chmitt **T**rigger
ICs	**I**ntegrated **C**ircuits
MCE	**M**uller **C**-**E**lement
MCEST	**M**uller **C**-**E**lement based **S**chmitt **T**rigger
MNUs	**M**ultiple **N**ode **U**psets
MOSFETs	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistors

PDP	**P**ower **D**elay **P**roduct
PVT	**P**rocess**V**oltage**T**emperature
Qc	**C**ritical **C**harge
QPAR	**C**ritical **C**harge to **P**ower **D**elay **A**rea **P**roduct **R**atio
RHBD	**R**adiation **H**ardening **B**y **D**esign
SEs	**S**oft **E**rrors
SETs	**S**ingle **E**vent **T**ransients
SEUs	**S**ingle **E**vent **U**psets
SNU	**S**ingle **N**ode **U**pset
ST	**S**chmitt **T**rigger
STST	**S**even **T**ransistor **S**chmitt **T**rigger
TF	**T**ransient **F**ault
TNU	**T**riple **N**ode **U**pset
TNURH	**T**riple **N**ode **U**pset **R**adiation **H**ardened
VTC	**V**oltage **T**ransfer **C**haracteristic

Chapter 1

Introduction

1.1 Motivation

Transient fault (TF) due to soft errors (SEs), sequential circuit designers are in a hard dilemma, while achieving reliable designs with maximum power efficiency. Among different electronic components in every chip, sequential elements (latches/ Flip-Flops) represent up to 50% of the chip area. Sequential elements, highly affect the chip efficiency, performance and reliability. In addition, the power consumption of the clock network, in latches/Flip-Flop approximately more than half of the total chip power consumption. Therefore, efficient implementation of sequential circuits mainly design of latch circuit is of great importance for power efficient and reliable integrated circuits (ICs) design. When a static D-latch is implementing at low technology node and low voltage, it becomes more susceptible to single event upset (SEUs) because of reducing supply voltage, decreasing critical charge, and increasing densities. Therefore, if we want to design a ultra-low power latch in reliability critical or space applications, techniques to tolerate SEU should be applied. Conventionally, Error Correction Code (ECC) is a technique is used to solve this problem. However, when multi-bit upset due to SE occurs, ECC may not be suitable solution because the cost of complicated coding and decoding technique for multi-bit correction is too high. It will bring high complexity and large overhead, as well as degrade the performance of the circuit. To overcome single event multiple nodes upset issues, radiation-hardened by-design (RHBD) techniques are explored in [1]-[96]. The advantage of these techniques is to enhance the tolerance against soft errors in worst cases. Therefore, energy efficient, low cost and radiation hardened latch designs are indispensable for low technology nodes.

1.2 Mechanisms of single-event effects

There are two types of radiation sources present in the atmosphere. First source is cosmic radiation (like protons and heavy ions) in space when hits in a transistor's sensitive area and produces electron hole pairs (EHPs), resulting in SEUs or single event transients (SETs) [1]-[6]. The second source is alpha particles and secondary neutrons produced through cosmic-ray interactions in terrestrial [7]-[15]. The absence of an atmospheric shielding layer in space allows cosmic particles to reach electronic systems with greater intensity. Consequently, the impact of cosmic radiation in space is considerably more severe than at ground level [16]-[22]. Charge collection generally occurs within a few microns of the junction; thus, the collected charge for these events is from 1 to several 100 fC, depending on the type of ion, its trajectory, and its energy over the path through or near the junction [23]. The reverse-biased junction is the most charge-sensitive part of circuits, particularly if the junction is floating or weakly driven [23], [24]. Considering a strike of a high-energy particle on the semiconductor device, the movement of this particle strike consists in three main successive steps: (1) charge deposition (or generation), (2) charge transport and (3) charge collection. Figure 1.1 schematically shows these successive steps in the case of the passage of the energetic charged particle through a reverse-biased n+/p junction [23].

Step 1: Charge generation: When an energetic particle traverses a semiconductor device, it transfers energy to the material and generates a localized charge distribution along its trajectory. This process primarily occurs through ionizing interactions, where energy is imparted to atomic electrons within the semiconductor lattice. The energized electrons subsequently initiate secondary ionization events, resulting in the formation of numerous EHPs throughout the particle track, as illustrated in Figure 1.1(a). Simultaneously, the

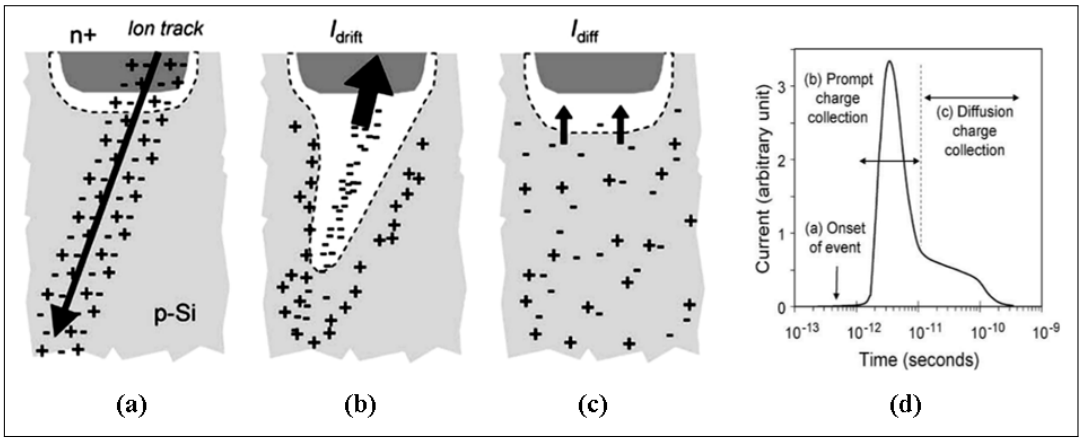


FIGURE 1.1: (a) Charge generation process, (b) and (c) charge transportation process, and (d) current transient process [24].

electric field distribution in the affected region is altered. It leads to the development of a characteristic funnel-shaped potential profile [24].

Step 2: Charge transport: After generation of EHPs, the resulting carriers move through the semiconductor and collected by nearby most sensitive regions of p–n junction. Carrier movement is due to two fundamental processes. First, carriers are driven by drift due to electric field as illustrated in Figure 1.1(b). Secondly, diffusion in electrically neutral regions, as shown in Figure 1.1(c). During this transport process, a portion of the generated carriers may recombine with existing free carriers in the semiconductor lattice, therefore reducing the amount of charge available for collection [24].

Step 3: Charge collection: As the generated carriers reach sensitive regions of the device, the collected charge gives rise to a transient current pulse, as illustrated in Figure 1.1(d). This temporary current disturbance can change the normal operation of the device and may propagate to neighboring circuit elements. Reverse-biased p–n junctions are particularly vulnerable to such events because the depletion-region electric field gives rapid and efficient charge collection. The resulting radiation effects depend on few factors such as magnitude and duration of the transient current pulse as well as the number of circuit nodes affected by the particle strike [24]. When cosmic rays or alpha particles

hit a node, charge accumulates due to drift and diffusion within the transistors, leading to a significant current or voltage at a single vulnerable node, known as a single node upset (SNU). If this significant current or voltage occurs simultaneously, two nodes at a time are called double node upset (DNU). Similarly, if a significant current or voltage occurs simultaneously, three nodes at a time are called triple-node upset (TNU) [25]. The SE due to TF is a significant problem in sequential circuits because internal node glitches can cause bits to flip in memory components like latches and flip-flops [26].

1.3 Functional failure due to soft error

The schematic of a conventional D latch [27] is shown in Figure 1.2. The input signal denoted as D and output signal denoted as Q. The reference latch operates using two clock signals: CLK and its complement NCK (negative clock). It uses three inverters (I1, I2, I3) where I1 and I2 are in the forward path, and I3 is connected in the feedback path. Along with this, the circuit uses two transmission gates (T1 and T2) respectively. The T1 and T2 are connected in feedforward and feedback path respectively.

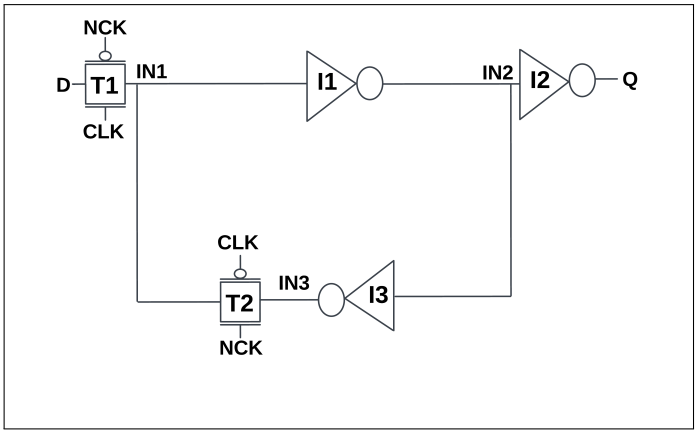


FIGURE 1.2: Schematic of D-latch.

When the CLK is high, the circuit enters the transparent mode. In this mode, the input signal D passes through the forward path to the output Q. In this state, T1 is turned ON,

while T2 is turned OFF, enabling the signal to pass sequentially through inverters I1 and I2, as shown in Figure 1.2. Consequently, any change in the input is immediately reflected at the output. When the NCK is high, the circuit enters the hold mode. During this mode, T1 turns OFF and T2 turns ON, activating the feedback loop formed by T2 and inverter I3 and disconnecting the input from the latch. This feedback path transmission gate T2 and inverter I3 maintain the previous logic state at internal node IN2, confirming that the output Q retains the previous logic value after changing the input D value. Generally, circuit sensitivity against radiation is checked in hold mode. The nodes IN1, IN2, and IN3 are more susceptible to TFs than the other nodes. The experimental data demonstrates that node IN1 has the lowest critical charge (Qc) [23] value among IN1, IN2, and IN3 [27]. Striking of high-energy particles at theses nodes causes the SEs, which change the stored logic state of the node temporarily without permanently damaging the circuit. Hence, the conventional D-latch is extremely vulnerable to SNU, also known as the unhardened D-latch [27]. The SEs were initially taken into account in applications related to nuclear and aerospace engineering [19]. Now, SEs become a significant reliability issue as a result of technological scaling and the previously noted decrease in supply voltage and node capacitance [26]. The statistics presented in [25] indicate that the likelihood of multiple node upsets (MNUs) generally rises with increasing particle energy and scale. Consequently, to produce digital ICs that are extremely dependable, it is required to create storage cells that are resilient to MNUs.

The RHBD refers to circuit and layout design strategies that add tolerance against SEU and MNU without changes in the manufacturing process to create a robust and cost-effective solution for radiation[28]. There are two commonly used techniques used for radiation hardening paths[29]. The first method is layout level hardening which reduce latch-up and minimize the leakage currents. For example, enclosed layout transistors

(ELTs) and guard rings represent the most common techniques employed by today's designers for controlling parasitic conduction paths[29]-[34]. However, the major drawback of layout-level hardening is the significant increase in silicon area [30] [32]. Therefore, this leads to higher fabrication cost and reduced circuit density. In some cases, it also degrades circuit performance due to increased parasitic capacitances [31], [35], [36]. The second method, circuit-level hardening overcomes above discussed drabacks and it generally uses redundancy-based designs such as Muller C-element (MCE) and DICE [37]. Nowadays, researchers only focus on circuit-level hardening with higher noise tolerance without increasing the fabrication cost. The MCE operates as follows. When all the inputs have the same logic value, the output's logic value is the opposite of the inputs logic values. When the logic values of all the inputs differ, then the output is in a high impedance condition and maintains the previous logic value [37]. The clock gating based Muller C-element (CG-MCE) also works like the MCE except that there are extra input signals: CLK and NCK [38]. Figure 1.3 (a) shows the 2-input Muller C-element (2MCE), while Figure 1.3 (b) shows the clock-gated 2-input Muller C-element (CG-2MCE). Figure 1.3 (c) presents the 3-input Muller C-element (3MCE), whereas Figure 1.3 (d) shows the clock-gated 3-input Muller C-element (CG-3MCE). Figure 1.3 (e) depicts the 4-input Muller C-element (4MCE), and Figure 1.3 (f) shows the clock-gated 4-input Muller C-element (CG-4MCE)[39]. However, the major drawback of MCE is that it can tolerate radiation but not recover. On the other hand, DICE [40] fully recovers from radiation. It can change its state only when more than two state nodes are upset at the same time due to the interlocked C-element. Due to interlocked C-element, consuming more power and having a larger delay [40]. Overall, RHBD is a scalable and efficient method of providing radiation tolerance through optimized layout practices, strong circuit architectures, and protection strategies on the node level, but does not require specialized radiation-hardened manufacturing processes.

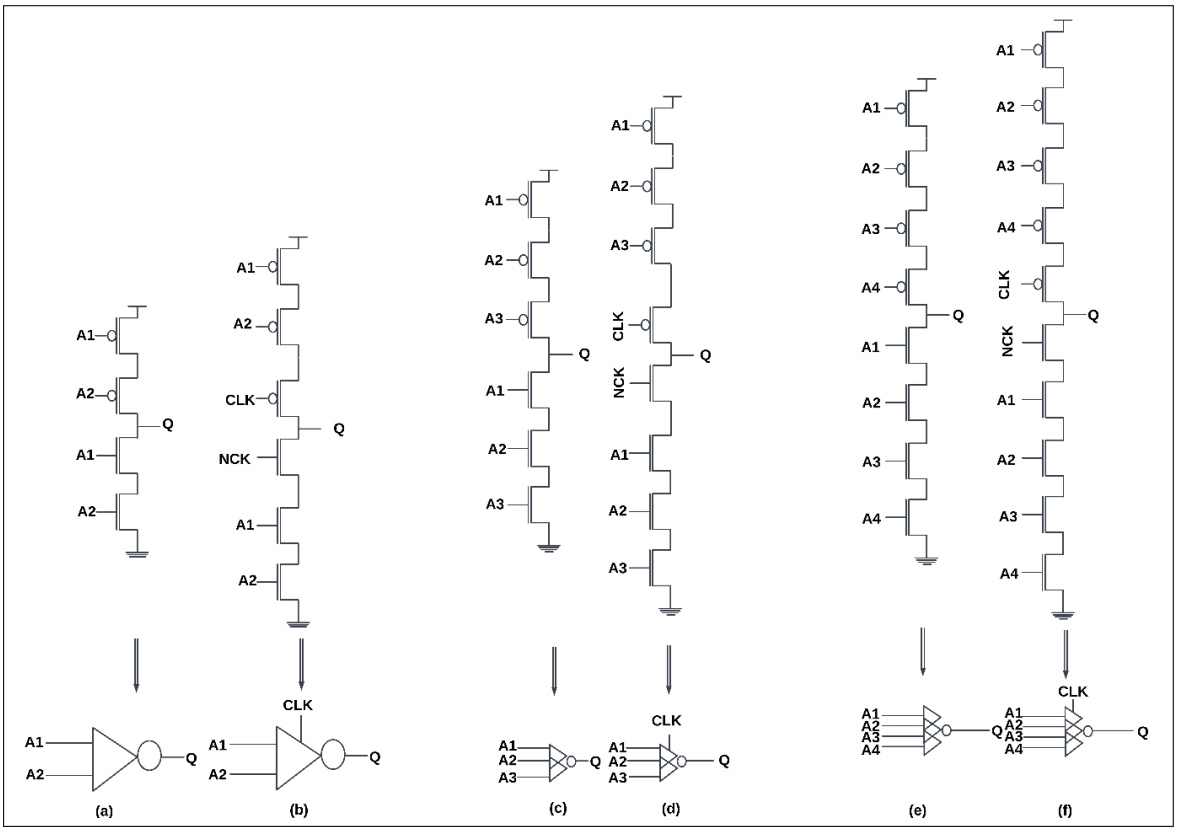


FIGURE 1.3: Schematics of widely used MCEs with different structures: (a) 2MCE, (b) CG-2MCE, (c) 3MCE, (d) CG-3MCE, (e) 4MCE, and (f) CG-4MCE [38], [39].

1.4 Literature review

To address SE issues, various radiation-hardened latch designs have been reported in the literature. Radiation hardened techniques for static D-latch can be classified into three categories:

(1) Single node upset tolerant technique

(2) Double node upset tolerant technique

(3) Triple node upset tolerant technique

In the following sub-section, we discuss radiation-hardened techniques for static D-latch.

1.4.1 Single node upset tolerant technique

The DICE [40] structure stores data across four interconnected nodes and employs redundant feedback paths such that the logic state of each node is controlled by two other nodes. This interlocking configuration ensures that a disturbance at any single node can be corrected by the remaining nodes, thereby preventing an SNU from corrupting the stored data. The TMR latch presented in [41] comprises three identical static latches and a majority voter. It is the most widely used latch in aerospace applications due to its high reliability. The majority of voters and large area overhead are drawbacks of the TMR latch. Compared with traditional redundancy-based techniques TMR [41] and EDAC [40], the DICE architecture provides strong SNU immunity with relatively small area and power overhead. Following the introduction of DICE-based storage elements, several researchers proposed improved latch architectures that aim to enhance SE tolerance while minimizing performance penalties. A redundant feedback path and three MCEs are added to the FERST latch presented in [42] to handle a TF. The data path from input to output contains 2MCE, adding a significant performance cost. In [43] presented hardened latch structures that protect critical feedback nodes through redundancy and error-masking mechanisms. This design included two variants, one optimized for lower cost and another providing higher robustness for safety-critical applications. Further research explored latch architectures optimized for nanoscale complementary metal oxide semiconductor (CMOS) technologies, where SE vulnerability becomes more pronounced. Several hardened latch designs based on Schmitt Trigger and cascode topologies were proposed to increase the Qc required to avoid flip the stored logic state [44]. Increasing the Qc improves radiation tolerance because a larger charge injection is required to disturb the stored data. These designs demonstrated improved noise immunity and enhanced power-delay trade-offs compared with conventional latch architectures [44]. Schmitt Trigger-based latches offer advantages like better noise immunity and sharper transitions at low supply voltages

due to hysteresis behavior. The conventional D latch uses only a single static inverter in the forward path. It has a single threshold voltage, usually about half of the supply voltage. Due to a single threshold, the inverter is susceptible to noise, especially if the input voltage is close to the threshold [45]. On the other side, Schmitt Triggers have two different thresh old voltages: low-to-high switching (higher threshold) and high-to-low switching (lower threshold) [45]. It is a unique hysteretic comparator circuit due to a gap between two distinct thresholds. Due to this property, if any change occurs in the input signal, that change will not be reflected in the output. Only massive, intended changes in the input voltage will alter the output state [45]. Schmitt Trigger-based radiation hardened designs show better noise tolerance, while DICE [40] has a higher power consumption and larger area due to a large number of transistors used. Subsequent work also introduced performance evaluation metrics that simultaneously consider multiple design parameters such as average power (dynamic plus static plus leakage power) [46]–[47] consumption, delay, circuit area, and SE resilience. For instance, researchers have proposed a metric for comparing radiation-hardened latch architectures in terms of Qc, average power, delay, area, and Qc to PDAP ratio (QPAR) [40], [43], [46]–[47]. Using the QPAR metric, several Schmitt Trigger-based latch designs were evaluated and demonstrated improved tolerance to process voltage temperature (PVT) variations compared with traditional CMOS latch structures [40], [43], [46]–[47]. The Schmitt Trigger latch improves robustness by increasing node capacitance, which enhances noise tolerance [46]. It incorporates redundant feedback loops and temporal redundancy was proposed to enhance radiation tolerance while maintaining relatively small power and delay overheads [46]. The SEM latch proposed in [27], is achieved by adding the feedback inverter in the D-latch along with two transistors. The inclusion of inverter and transistors functions as a Schmitt trigger inverter, and because of that, the equivalent gate capacitance of nodes increased [27]. The modified SEM latch (M-SEM) proposed in [27] has two additional inverters are added to the forward

path with gates of transistors to create a Schmitt Trigger comapred to D-latch. After modification to the SEM-latch design Qc increased. The radiation-hardened Schmitt Trigger (ST) latch proposed in [27] swapped inverter I1 of the conventional D-latch with an ST-based inverter . The ST latch will function more slowly because of the Schmitt Trigger's hysteretic properties. A cascode ST latch proposed in [27] to increase the Qc at the node IN1. The only difference between the ST latch [27], and the cascode ST latch proposed is the cascode feedback path. In this latch, the inverter and transmission gate in feedback is replaced by cascode feedback. The cascode architecture allows a greater capability to exit the metastable condition than the transmission gate Without performance deterioration [48]. Furthermore, the Qc is improved in cascode structure. Similarly, HETR-HL [47] latch architecture combines Schmitt Trigger characteristics with duplicated feedback paths to improve SE resilience while maintaining acceptable performance metrics. Recent research has focused on improving radiation tolerance while reducing design complexity and hardware overhead. The HPST [49] latch integrates MCE with dual modular redundancy to achieve higher Qc and lower PDP compared with conventional hardened latch designs. Another approach introduced in [50] is the NST-VB latch, which improves radiation tolerance while reducing temperature sensitivity and power consumption. Further improvements have been achieved through latch architectures incorporating CG-MCEs and memory restorer circuits, which significantly improve the PDP and provide stronger protection against SNUs across multiple technology nodes including in different technology node 65 nm, 32 nm, and 22 nm CMOS technologies [51]. In the VB-ST [51] latch, which increases internal node voltages and noise margins, thereby improving the circuit's resistance to transient radiation disturbances. In SERL [52] latch have been proposed to automatically restore the correct logic state after a transient disturbance while reducing power consumption and circuit area. Other studies have further extended this concept by designing latch architectures that simultaneously mitigate radiation-induced faults and device aging mechanisms such as bias temperature instability (BTI) [53], thereby improving

long-term circuit reliability. Aggressive technology scaling has introduced more severe reliability challenges. In advanced technology nodes, a single radiation particle strike may simultaneously affect two nearby nodes through charge sharing. This phenomenon leads to DNUs, where two circuit nodes are disturbed simultaneously by a single particle strike [54], [55]. Conventional SNU-hardened latch architectures such as DICE may fail under such conditions because their redundancy mechanisms assume that only one node will be affected at a time [56]. To address DNUs, various radiation-hardened latch designs have been reported in the literature.

1.4.2 Double node upset tolerant technique

Several studies have proposed radiation-hardened latch designs based on dual modular redundancy that combine MCE structures to achieve complete recovery against DNUs while enhancing speed and reducing power consumption [56]-[59]. The dual modular redundancy based DNUSH latch presented in [56] is made up of MCEs and inverters to develop multi feedback interlocked loops that preserve accurate data even after the radiation event at the cost of area overhead. Subsequent studies introduced latch architectures based on MCEs, together with high-speed transmission paths and clock-gating techniques, to balance performance and energy efficiency [39]. The LCDNUT [39] latch is built to fully tolerate any DNU using the 3MCE to intercept the accumulation of SEs in the storage module, but the complexity of the circuit is increased. These designs demonstrated significant reductions in power delay product (PDP) and improved robustness under PVT variations [39]. Additional research proposed high-performance latch structures capable of tolerating DNUs while avoiding high-impedance states and maintaining stable operation in radiation environments [57]. More recent studies have focused on reducing hardware complexity while maintaining strong DNU resilience by introducing stacked cross-coupled storage elements and polarity-aware design methodologies [60]. Rule-based latch

design techniques and clock-gating strategies have also been proposed to reduce transistor count and improve energy efficiency while maintaining strong radiation tolerance [61]. Other architectures designed for space electronics employ interlocked feedback loops and specialized logic structures to achieve significant reductions in delay, power consumption, and circuit area while maintaining high reliability in radiation-prone environments [62]. Very recent work has proposed latch designs based on polarity-aware logic and source isolation techniques that reduce the number of sensitive nodes and achieve substantial improvements in power consumption, delay, and area when implemented in advanced CMOS technologies such as 28 nm nodes [63]. The RH-2 presented in [64] has the unique characteristics of a radiation-induced voltage pulse with a good Qc that allows for protection of DNU recovery but at the cost of power delay and area overhead. The HUD-TAL presented in [65] enhances the Qc threshold, resulting in more delay compared to other designs. The DNUCR latch presented in [66] usage of multiple feedback elements complicates the design process and increases verification complexity. The DURMA [67] latch provides robustness and mitigates aging effects, though it incurs a modest area overhead relative to other designs. With the continued scaling of semiconductor technologies, the spacing between circuit nodes has decreased, increasing the likelihood that a single radiation particle may simultaneously disturb multiple nodes. Such an event, when three circuit nodes are affected at the same time, is referred to as a TNUs [59]. Conventional latch hardening schemes designed for SNUs and DNUs disturbances may fail under such conditions because the redundancy mechanisms themselves can become corrupted [59]. To overcome this limitation, researchers have proposed several specialized latch architectures capable of tolerating TNUs. To address TNUs, various radiation-hardened latch designs have been reported in the literature.

1.4.3 Triple node upset tolerant technique

Early approaches incorporated restorer circuits and majority voting mechanisms to restore the correct logic state after a TNU event while improving the PDP [59]. Later designs introduced block-based latch architectures consisting of multiple storage modules interconnected through MCE to enhance fault tolerance with relatively low area overhead [68]. The TNUHL latch presented in [69] consists of five interlocked 4MCE and produces feedback loops that preserve values. This latch is built on multimode redundancy and double-level error interception (DLEI). Although there is no transmission path from input to output and a large number of multi-input MCEs are used, which increases the delay. Subsequent studies proposed modular latch architectures capable of tolerating SNU, DNU, and TNU simultaneously while minimizing performance penalties [70]–[72]. Other designs employ node separation techniques and clock gating mechanisms to reduce charge sharing and improve reliability in radiation-prone environments [72]. Several architectures based on interlocked DICE cells have also been proposed to provide multi-node upset tolerance while maintaining acceptable power-delay trade-offs [73]–[75]. The IHTRL latch presented in [75] consists of a matrix of four CG-MCEs and twelve MCEs that cascade to create a feedback loop and store data. Due to the large number of MCEs, its area, delay, and power consumption are relatively high. More recent studies have introduced optimized TNU-tolerant latch architectures using stacked transistor structures, polarity-aware logic, and heterogeneous interconnection networks to achieve improved radiation resilience with lower power consumption and reduced circuit area [76]–[86]. The LRLPT latch presented in [76] uses a source-drain cross-coupled element (CCE) technique. Due to multiple feedback loops during the transparent phase, it experiences high power consumption and considerable delay. The MCTHSL latch presented in [78] consists of eight transmission gates, fifteen 2MCEs, and one Schmitt Trigger. This latch provides robustness against SEs at the cost of increased power and delay. The TNUCR latch, which was

presented in [81], consists of six inverters and five CG-4MCEs. It has inverters on the feedback path hence more transmission delay. The LCTNUCR latch presented in [81] overcomes the issue of increased transmission delay by replacing the inverter with a CG-4MCE. However, there is a significant area overhead when using multiple 4MCEs. These latch architectures are particularly suitable for high-reliability applications such as satellite systems, aerospace electronics, and nuclear instrumentation where radiation-induced faults are unavoidable [86]–[90]. The TSRL latch presented in [88] incurs a relatively large area overhead due to the complex quadrate interlocking recovery structure using numerous MCEs and CG-MCEs. The TNUSH latch presented in [91] uses nine 2MCEs, six CG-2MCEs, two 3MCEs, and four single-input inverters. This latch provides robustness against SEs at the cost of area overhead. Conventional latch circuits implemented using planar MOSEET technology face several limitations at deep nanoscale nodes, including increased leakage current, short-channel effects, and large PVT variations [92]-[95]. The Fin field effect transistor (FinFET) technology has therefore been investigated due to its improved electrostatic control and reduced leakage current compared with planar CMOS devices [92]. For example, charge-steering latch architectures implemented in 16 nm FinFET technology have demonstrated improved SE hardness by reducing charge collection at sensitive nodes [92]. Similarly, non-volatile magnetic latch architectures integrated with MCE keeper circuits have shown improvements in delay and power consumption while maintaining strong radiation resilience in advanced FinFET technologies [93]. Another promising device technology is the carbon nanotube field effect transistor (CNTFET). The CNTFET devices exhibit high carrier mobility, low leakage current, and extremely high Ion/Ioff ratios, making them suitable for low-power and high-reliability digital circuits [94]. Schmitt Trigger-based CNTFET latch architectures provide improved noise immunity due to hysteresis behavior and demonstrate significant reductions in PDP while increasing the Qc required to flip the stored logic state [94]. Other CNTFET-based radiation-hardened latch architectures demonstrate strong SNU immunity and effective

filtering of single-event transients with minimal area overhead [95]. The latch presented in [96] cannot maintain full DNU tolerance at clock edges due to design limitations, making the latch vulnerable to data latching errors in certain DNU cases. Despite the significant progress achieved in radiation-hardened latch design, several challenges remain unresolved. Many existing latch architectures provide strong protection against SNUs but fail under MNUs conditions. Although several DNUs and TNUs tolerant designs have been proposed, many of these architectures still exhibit one or more limitations, such as high transistor count, increased power consumption, and large delay. Therefore, there remains a need for developing low power, are efficient, and highly reliable latch architectures capable of tolerating MNUs while maintaining high performance and low design complexity.

1.5 Research gaps

In the light of the literature survey, it is noted that low power circuit designing is widely explored due to the increasing high demand for energy-efficient electronic systems. However, low power circuits have always been more susceptible to SE as discussed earlier. To resolve these issue, several resilient latch designs have been reported in literature but they have some limitations. In this respect, following are some technical gaps required to be resolved:

1. Current mitigation designs, such as error-correcting codes and redundancy techniques, can impose substantial power, area, and latency overheads, limiting their applicability in energy-efficient and performance-critical applications. There is a lack of a low-cost single-node upset mitigation circuit that effectively balances area, power, and delay, making it a critical gap in the development of resilient ICs.

2. The complexity of MNUs increases with the scaling of technology nodes, as smaller geometries and higher integration densities make circuits more susceptible to simultaneous errors across multiple nodes in the circuit. Despite ongoing research, there is a notable lack of low-cost, scalable solutions for addressing MNUs while maintaining a balance among area, average power, and delay.

3. Despite significant advancements in radiation-hardened latch designs for conventional CMOS technologies, there remains a lack of comprehensive solutions specifically tailored for emerging nanoscale devices such as FinFET and CNTFET. Most existing hardened latch architectures are optimized for planar CMOS and do not account for the distinct physical, electrical, and radiation response characteristics of FinFET and CNTFET.

   Addressing these gaps is crucial for designing robust ICs for future applications in safety-critical and high-performance domains.

1.6 Research objectives

The work revolves around addressing the identified research gaps through the following objectives:

1. To design and implement a novel Schmitt Trigger-based latch architecture that enhances resilience against Single Node Upsets while achieving improved performance in terms of charge to PDAP ratio (QPAR).

2. To design and analyze a novel radiation-hardened latch architecture by incorporating Schmitt Trigger and Muller C-element mechanisms to enhance overall noise immunity and fault tolerance.

3. To develop a novel latch structure capable of withstanding Triple Node Upsets, with a focus on improving reliability in high-radiation applications such as aerospace and defense systems.

4. To benchmark the proposed novel latch designs against traditional counterparts in FinFET environment, highlighting their improved fault tolerance and optimized trade-offs in power, delay, and area.

1.7 Thesis organization

The thesis is structured into six chapters, the first of which provides an introduction and an overview of the radiation hardened latches. Chapters 2 to 5 focus on the four objectives that were determined through research gaps. The conclusions are drawn in chapter 6, wherein potential avenues for further study are also outlined. An overview of the contents of each chapter is provided below:

Chapter 1:

This chapter presents the background and motivation of the research work. It provides an overview of existing radiation-hardened latch designs reported in the literature. The limitations of these designs are analyzed to identify the existing research gaps. Based on these findings, the objectives of the proposed work are formulated.

Chapter 2:

In this chapter, Four Schmitt Trigger-based radiation-hardened latches are introduced, which successfully overcome the SNU effects and provide improved performance. First, two latches use STST in the forward path and differ in the components used in the feedback path. Similarly, Second, two latches use FTST in the forward path and differ in the

components used in the feedback path. The detailed explanation of the working of the proposed designs is put forward, and their operation is verified through timing waveforms. The performance of the proposed designs in terms of D–Q delay, average power, Qc, area, PDP, and QPAR is evaluated and compared with the considered radiation-hardened latches. The study of supply voltage and temperature variation is conducted to analyze corresponding effect on power and delay. Additionally, the impact of process variations on the performance of the design metrics is evaluated through Monte Carlo analysis.

Chapter 3:

In this chapter, the MCE-based radiation-hardened latch (TNURH) is introduced, which successfully overcomes the TNUs' effects and provides improved performance. The detailed explanation of the working of the proposed design is put forward, and its operation is verified through timing waveforms. The performance of the proposed design in terms of D–Q delay, average power, Qc, area, PDP, and QPAR, is evaluated and compared with the considered radiation hardened latches. The study of supply voltage and temperature variation is conducted to analyze corresponding effect on power and delay. Additionally, the impact of process variations on the performance of the design metrics is evaluated through Monte Carlo analysis.

Chapter 4:

In this chapter, the Schmitt Trigger and MCEs-based radiation-hardened latch (CSTCE-TNURH) is introduced, which successfully overcomes the TNUs' effects and provides improved performance. The detailed explanation of the working of the proposed design is put forward, and its operation is verified through timing waveforms. The performance of the proposed design in terms of D–Q delay, average power, Qc, area, PDP, and QPAR, is evaluated and compared with the considered radiation hardened latches. The study of supply voltage and temperature variation is conducted to analyze corresponding effect on

power and delay. Additionally, the impact of process variations on the performance of the design metrics is evaluated through Monte Carlo analysis.

Chapter 5:

This chapter explores the feasibility of designing a FinFET-based radiation-hardened latch (MCEST) at advanced technology nodes. In the nanometer regime, maintaining reliable circuit performance becomes increasingly challenging due to increased circuit density, reduced Qc, and lowered supply voltage, which make circuits more susceptible to SEs and TFs. Compared to planar metal oxide semiconductor field effect transistors (MOSFETs) of the same size, FinFETs provide higher ON current, which enhances switching performance and overall circuit speed. Additionally, the channel width in FinFETs can be adjusted by varying the fin height, allowing higher circuit density and improved scalability in nanoscale designs. These characteristics make FinFET technology well-suited for advanced latch design, particularly in applications requiring high reliability under scaled voltage and technology conditions. The detailed explanation of the working of the proposed design is put forward, and its operation is verified through timing waveforms. The performance of the proposed design in terms of D–Q delay, average power, Qc, area, PDP, Qc to PDP ratio, is evaluated and compared with the considered radiation hardened latches. The study of supply voltage and temperature variations is conducted to analyze their effects on power and delay. Additionally, the impact of process variations on the performance of the design metrics is evaluated.

Chapter 6:

This chapter summarizes the key contributions made in the field of radiation-hardened latch designs. The chapter also outlines future research directions and highlights the social impact of enhancing the reliability of critical electronic systems.

Chapter 2

Schmitt Trigger Based SNU Radiation Hardened Latches

The results described in this chapter have been published as the following peer-reviewed publication:

* N. Kumar, C. I. Kumar, and N. Pandey, **"High-performance radiation hardened latch using Schmitt Trigger,"** Integration, vol. 104, Feb. 2025, doi: 10.1016/j.vlsi.2025.102478.

* N. Kumar, N. Pandey, and C. I. Kumar **"Schmitt Trigger Based Compact Radiation Hardened Latch,"** 2025 IEEE 4th Int. Conf. Adv. Technol., pp. 1 7, 2025, doi: 10.1109/ICONAT66879.2025.11362702.

2.1 Introduction

The static D-latch is more prone to soft errors (SEs) because of its lesser Qc due to technology scaling and low voltage operation [22]. Terrestrial SEs occur in electronic circuits either from alpha particles originated from packaging or neutron particles from cosmic rays [40]. Due to SEs, changes the logic level of an affected node of a transistor which is in OFF state. The radiation-hardened by design (RHBD) techniques provides best solution to tolerate radiation-induced transient faults (TFs) [21]. From the last decade, vast research in the field of radiation hardened latches against single-node upset (SNU) due to SEs is carried out. Carrying this work forward, first we have proposed an energy efficient seven transistor Schmitt Trigger (STST) radiation hardened latch. The proposed SNU tolerant latch consist of a schmit trigger to enhance SNU tolerance to achieve more robustness compared to the recently reported SNU hardened latches. Further we have proposed an energy efficient four transistor Schmitt Trigger (FTST) tolerant latch. The proposed STST and FTST tolerant latches improve D-Q delay, power, Qc and QPAR as compared to other reported hardened latches.

In Section 2.2, working principle and soft error robustness of the proposed design 1 are presented. Section 2.3 describes the simulation setup for the SNU tolerant designs presented in this chapter. Section 2.4 provides the performance evaluation of proposed design 1. In Section 2.5, working principle, and soft error robustness of the proposed design 2 are presented. Section 2.6 provides the performance evaluation of proposed design 2. Section 2.7 provides a comparison between designs 1 and 2, and Section 2.8 summarizes the findings.

2.2 Proposed design 1

The proposed design 1 presents two radiation-hardened latch designs. The first is STST based latch and the second is cascode seven transistor Schmitt Trigger (CSTST) latch.

2.2.1 Proposed STST latch

The schematic of STST latch is shown in Figure 2.1. It consists of four blocks: transmission gate (T1), STST block, inverter (I1), and inverter (I2) followed by transmission gate (T2). The STST block is placed in the forward path and employs seven transistors, namely M1, M2, M3, M4, M5, M6, and M7, and is significantly achieving radiation hardening. The signal D is the input, and Q is the output in the schematic. The clock signal is referred to as CLK, while the inverted clock signal is labeled NCK. When the CLK is high, the circuit functions in transparent mode, and when the CLK is low, it works in hold mode. When the clock is at logic high, the transmission gate T1 will be on, and T2 will be off, so in this scenario, any change in input at D it will be available at node IN2. The feedback path behaves like an open circuit in transparent mode. In the hold mode, T1 turns off while T2 turns on. In this scenario, input D is not directly connected to output. As the feedback path is activated and the output node Q maintains its previous logic state. The proposed latch effectively works in transparent and hold mode, as shown in Figure 2.2.

Now, we will discuss the TF in the hold mode when positive pulse strikes at node IN1. Let us take logic low at node IN1 and logic high at node IN2. Then node Z is charged, and M7 turns on. Suppose a positive pulse strike at node IN1; consequently, node IN1 goes to logic high from logic low, M5 and M6 will be on. Before changing the logic state at node IN2, charge at node Z must be discharged. In this scenario, IN2 is still logic high, and

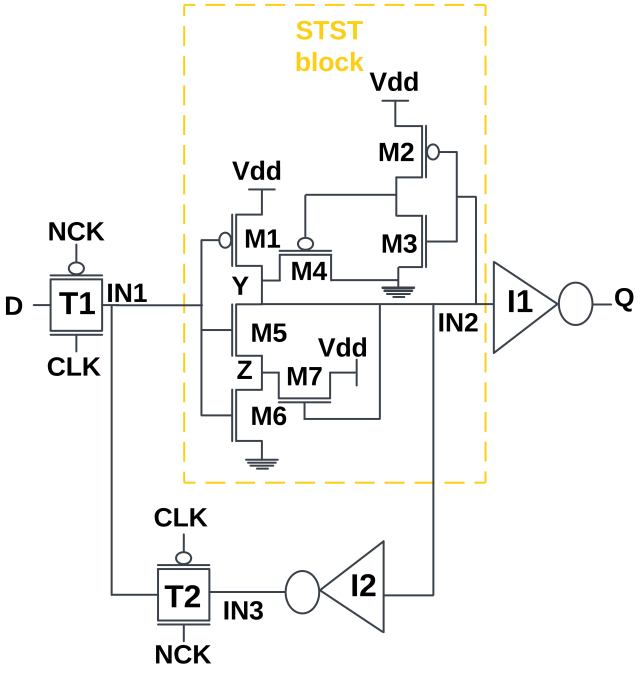


FIGURE 2.1: Schematic of proposed STST latch.

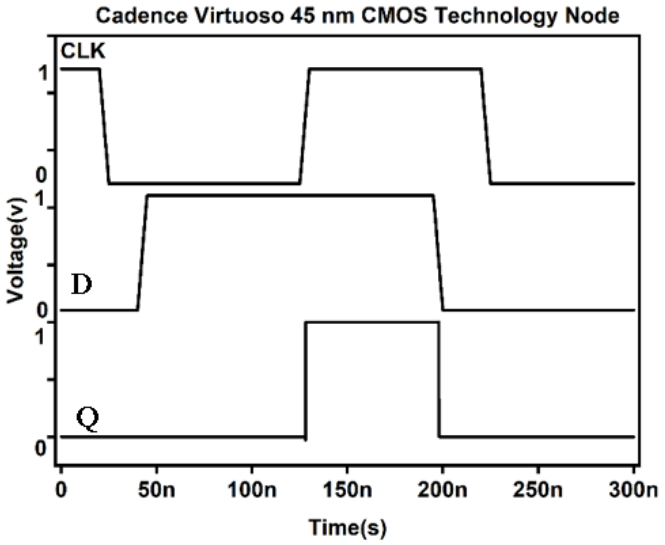


FIGURE 2.2: Simulation results of the STST latch under fault-free case.

enforcing node IN1 to restore the previous state. Now we consider negative pulse strike at node IN1. In this case logic high is assumed at node IN1 while node IN2 rests at logic low. Then node Y is charged, and M3 and M4 turns on. After the TF, node IN1 becomes logic low and M1, M4 will be on, and charge at node Y must be discharged before node

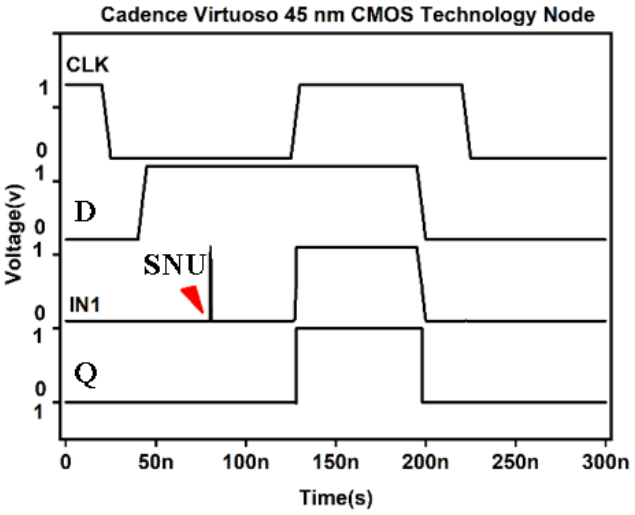


FIGURE 2.3: Simulation results of SNU injection case for STST latch at node IN1.

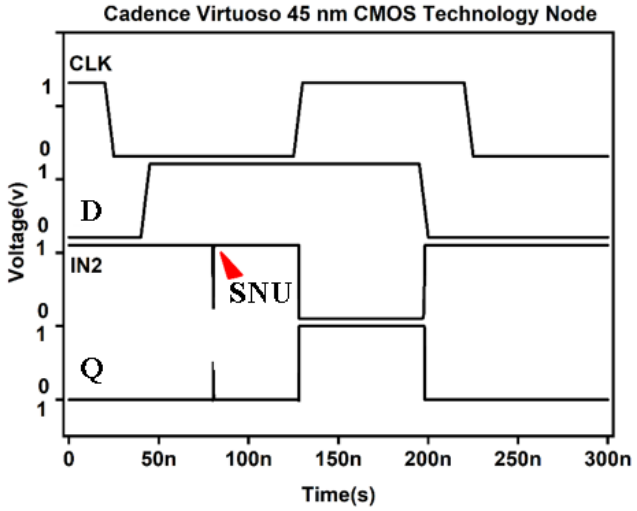


FIGURE 2.4: Simulation results of SNU injection case for STST latch at node IN2.

IN2 can change state. In this scenario, IN2 is still logic low, and the logic of node IN2 forces node IN1 to restore the previous state. The effect of SNU at node IN1 and IN2 of the proposed design is shown in Figures 2.3 and 2.4, respectively. Furthermore, the effect of SNU occurring at node IN1 in the hold mode is not transmitted at the output, thus proving the radiation hardness of the proposed STST latch against SNU.

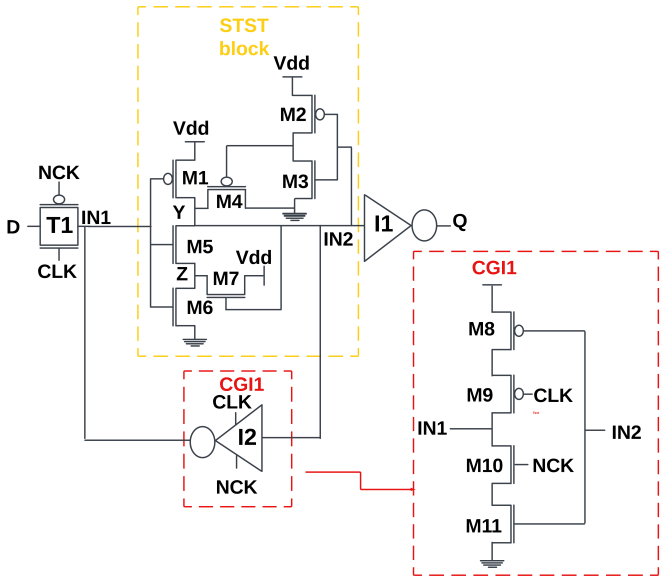


FIGURE 2.5: Schematic of proposed CSTST latch.

2.2.2 Proposed CSTST latch

The schematic of CSTST latch is shown in Figure 2.5. The proposed CSTST design is derived from the STST design with a minor modification. Specifically, the transmission gate and inverter employed in the STST design are replaced with a cascode feedback loop (CGI1). According to [48], cascode architecture demonstrates a superior ability to exit from a metastable state and provides better small signal performance due to reduced Miller effect compared to transmission gate architecture. When CLK is high, and NCK is low, both STST and CSTST latch designs function in the same way. Therefore, the operation is skipped for the sake of brevity. The timing waveform in the fault-free case is shown in Figure 2.6. The output follows the input when the CLK is at logic high (transparent mode) and hold mode when the CLK is at logic low.

The SNU at nodes IN1 and IN2 of the proposed design is shown in Figures 2.7 and 2.8, respectively. Furthermore, the effect of SNU occurring at node IN1 in the hold mode is

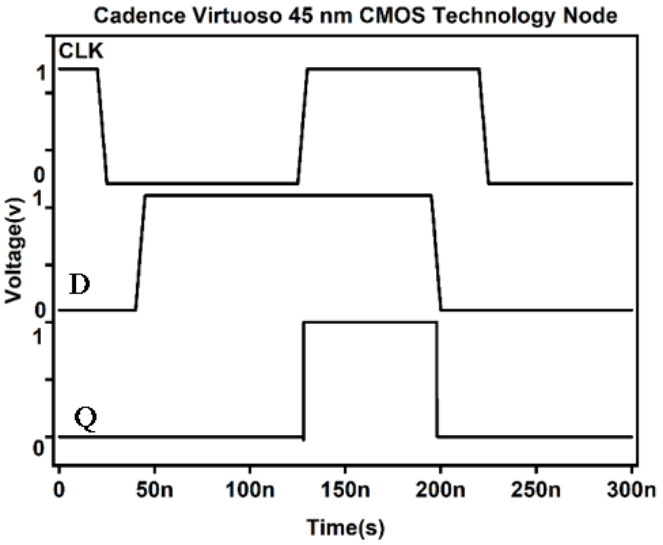


FIGURE 2.6: Simulation results of the CSTST latch under fault-free case.

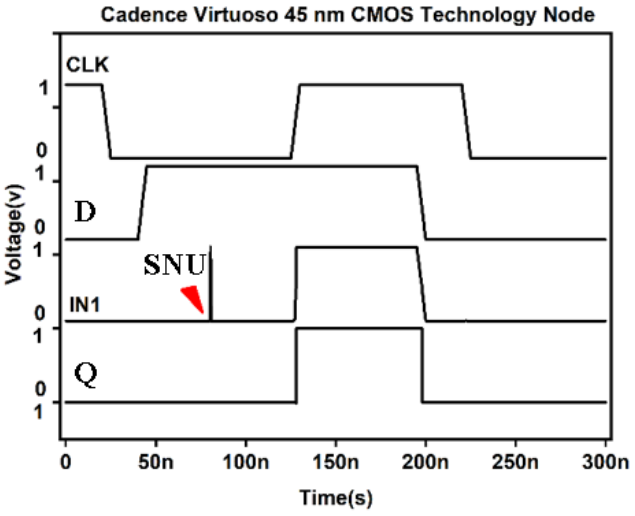


FIGURE 2.7: Simulation results of SNU injection case for CSTST latch at node IN1.

not transmitted at the output, thus showing the radiation hardness of the proposed CSTST latch.

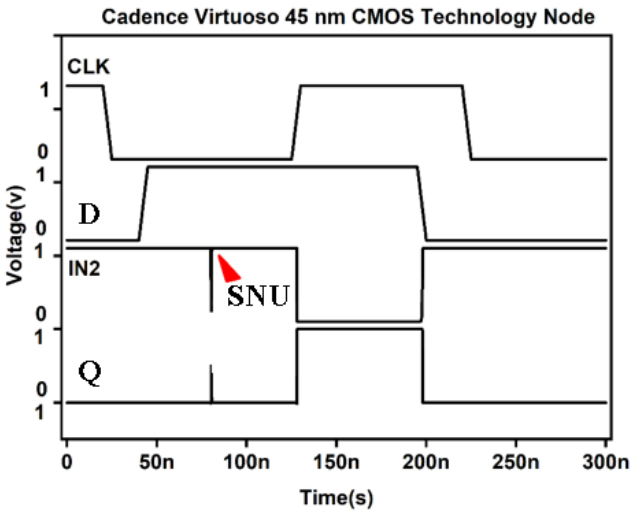


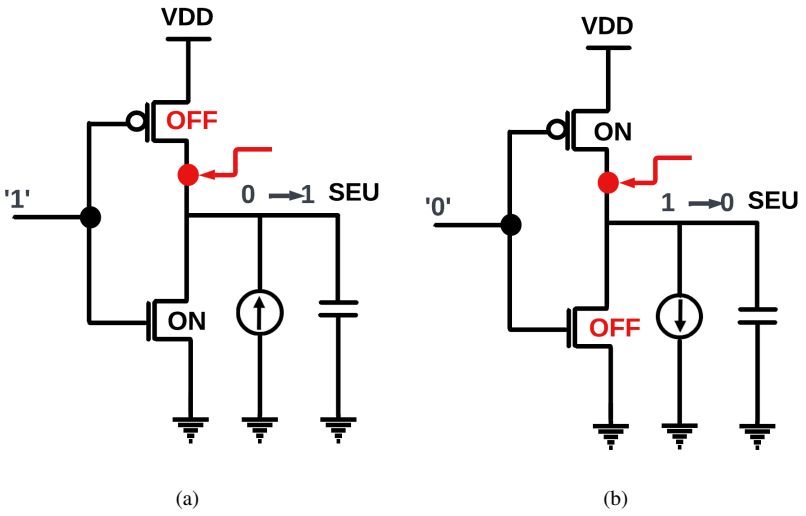
FIGURE 2.8: Simulation results of SNU injection case for CSTST latch at node IN2.

2.3 Simulation setup

All the proposed latches performance in this thesis, is examined in Cadence Virtuoso 45 nm CMOS technology and a 1 V supply voltage at room temperature 27°C and typical process corner. The proposed latches is compared with the other reported latches in terms of D–Q delay, power, Qc, area, PDP, and QPAR. The radiation hardening of proposed and compared latches is examined by injecting a double exponential current source [75] given by (2.1).

$$I(t) = Q\left(e^{-\frac{t}{\tau_2}} - e^{-\frac{t}{\tau_1}}\right) \tag{2.1}$$

where, Q represents the charge accumulated at the node after a strike by high-energy particles; t denotes the fault injection time; τ_2 corresponds to the charge collection time constant, and τ_1 indicates the initial ion-track formation time constant. In the simulation, we have taken τ_2 to be 164 ps and τ_1 to be 50 ps [75]. The direction of the current source is selected to generate a transient pulse that is positive at the PMOS drain (Figure 2.9 (a)) and negative at the NMOS drain and (Figure 2.9 (b)) [75].



(a) (b)

FIGURE 2.9: Transient pulse applied at the drain of (a) PMOS (positive), (b) NMOS (negative).

In order to ensure an equitable comparison, the concept behind choosing the transistor dimensions is voltage transfer characteristic (VTC) curve and the concept of logical effort [45]. Using the idea of logical effort, the transistor sizes for proposed and reported latches were optimized to balance speed and power consumption, ensuring uniform performance across various logic gate configurations derived from the original inverter sizing. The D–Q delay and power are evaluated under PVT conditions. For variability analysis, we have used corner analysis, voltage variation, temperature variation, and Monte Carlo analysis. Simulations are performed for the FF, FS, SF, and SS process corners in order to observe the behavior of the circuits under different scenarios. In addition, the supply voltage is varied from 0.5 V to 1 V, while the temperature range is considered from -25°C to 125°C. These ranges were chosen because practical CMOS circuits, particularly at lower technology nodes, often experience noticeable performance changes with even moderate environmental or process variations. To further examine statistical variability, Monte Carlo simulations with 10,000 runs are carried out using a 5% Gaussian distribution with $\pm 3\sigma$ variation. Variations in transistor width and supply voltage are included during the analysis, since both parameters can influence D-Q delay and power quite significantly.

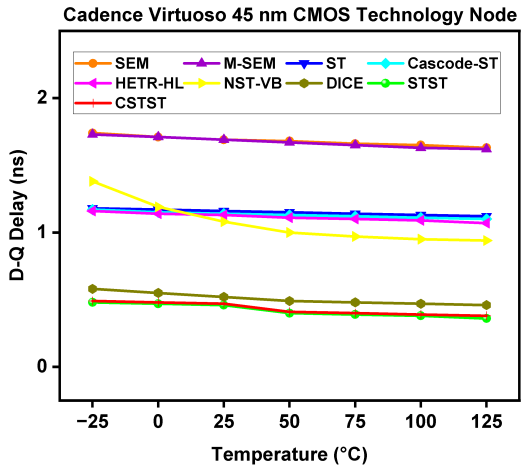


FIGURE 2.10: Temperature variation effect on D-Q delay of proposed STST, CSTST and considered latches.

2.4 Perfomance evaluation

D-Q Delay: The time difference between the input D voltage reaching 50% of its value and the output Q voltage reaching 50% during rising and falling transitions is known as the D–Q delay. The value of D-Q delay for SEM [27], MSEM [27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], DICE [40], and the proposed STST and CSTST are found to be 1.63 ns, 1.69 ns, 1.17 ns, 1.17 ns, 1.14 ns, 1.07 ns, 0.54 ns, 0.46 ns, and 0.47 ns, respectively, and the same is presented in Table 2.1. The results show that the proposed STST and CSTST latches achieve the minimum D-Q delay compared to the reported latches. Moreover, the effects of variations in temperature and supply voltage are also examined, and the results are shown in Figures 2.10 and 2.11, respectively. It can be observed that the proposed designs shows better results in the entire voltage and temperature range as compared to other reported designs.

Power: The power of a latch represents the average power consumed during its switching operation under normal working conditions. The value of power for SEM [27], MSEM

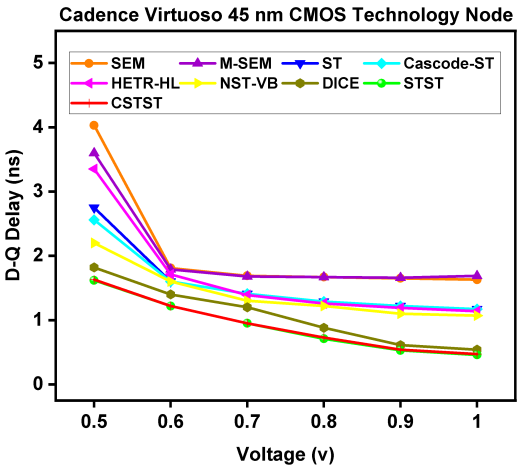


FIGURE 2.11: Voltage variation effect on D-Q delay of proposed STST, CSTST and considered latches.

[27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], DICE [40], and the proposed STST and CSTST are found to be 177.9 nW, 194.1 nW, 28.03 nW, 27.91 nW, 32.49 nW, 25.01 nW, 388.6 nW, 14.04 nW, and 14.07 nW, respectively, and the same is presented in Table 2.1. The results show that the proposed STST and CSTST latches consume significantly lower power compared to the reported latches. Moreover, the effects of variations in temperature and supply voltage are also examined, and the results are shown in Figures 2.12 and 2.13, respectively. It can be observed that the proposed designs shows better results in the entire voltage and temperature range as compared to other reported design.

Critical Charge (Q_c): The Qc is defined as the minimum amount of charge required to change the stored state of a latch due to radiation-induced effects. The value of Qc for SEM [27], MSEM [27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], DICE [40], and the proposed STST and CSTST are found to be 9.85 fC, 9.89 fC, 9.99 fC, 10.59 fC, 10.03 fC, 7.92 fC, 10.55 fC, 10.14 fC, and 11.33 fC, respectively, and the same is presented in Table 2.1. The results show that the proposed CSTST latch achieves the highest Qc compared to the reported latches.

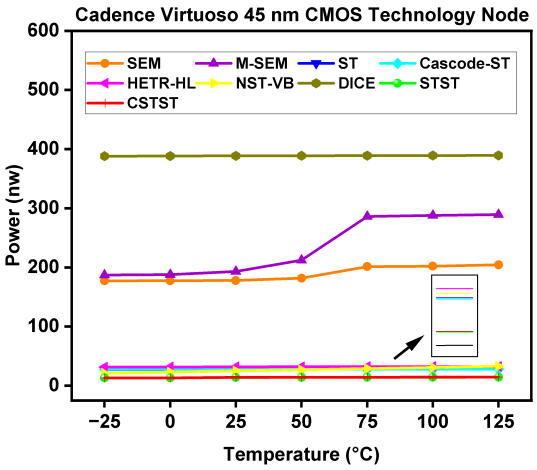


FIGURE 2.12: Effect of temperature variation on the power of proposed STST, CSTST and considered latches

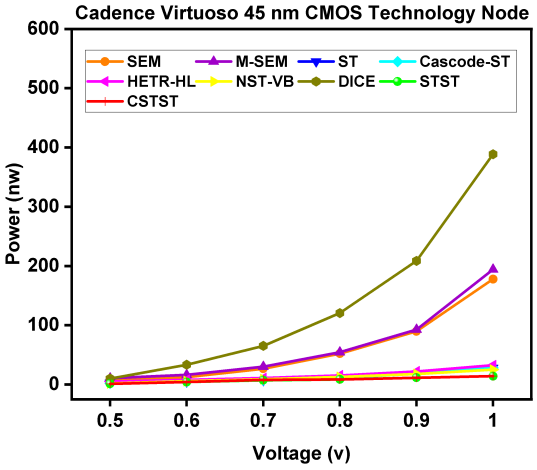


FIGURE 2.13: Effect of supply voltage variation on the power of proposed STST, CSTST and considered latches

Area: The area of a latch represents the total silicon occupied by the transistors used in the circuit layout. The value of area for SEM [27], MSEM [27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], DICE [40], and the proposed STST and CSTST are found to be 6.47 μm^2, 8.45 μm^2, 7.47 μm^2, 7.47 μm^2, 12.40 μm^2, 8.70 μm^2, 9.45 μm^2, 7.58 μm^2, and 7.58 μm^2, respectively, and the same is presented in Table 2.1. The results show that the proposed STST and CSTST latches occupy the lower area compared to

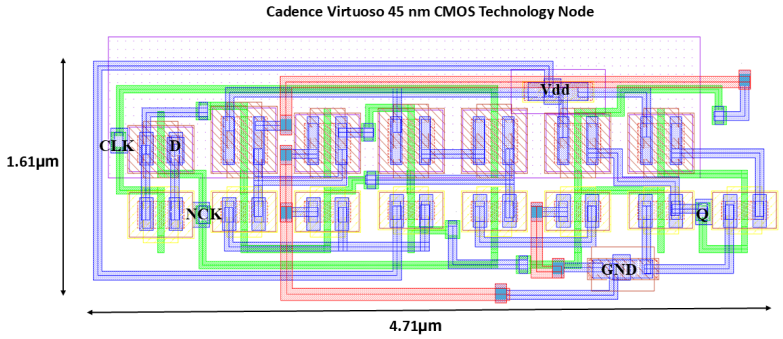


FIGURE 2.14: Layout for proposed CSTST latch.

MSEM [27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], and DICE [40]. The proposed CSTST latch layout is shown in Figure 2.14. After layout implementation, parasitic resistance and capacitance (RC) extraction was performed. The extracted parasitics were then incorporated into the post-layout simulations to evaluate their impact on power, delay, and critical charge. The post-layout results show variations of 8.44%, 15.61%, and 5.92% in power, delay, and critical charge, respectively, for the CSTST latch.

PDP: The PDP value is calculated by simply multiplying the power and D-Q delay for the latch. The value of PDP for SEM [27], MSEM [27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], DICE [40], and the proposed STST and CSTST are found to be 289.98 aJ, 311.50 aJ, 32.79 aJ, 32.79 aJ, 36.49 aJ, 26.76 aJ, 209.84 aJ, 6.46 aJ, and 6.61 aJ, respectively, and the same is presented in Table 2.1. The results show that the proposed STST and CSTST latches significantly lower PDP compared to the reported latches.

QPAR: The QPAR evaluated based on a comprehensive metric Qc to PDAP ratio (QPAR). The value of QPAR for SEM [27], MSEM [27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], DICE [40], and the proposed STST and CSTST are found to be 0.53 $\times 10^{-2}$ m^2/V, 0.37 $\times 10^{-2}$ m^2/V, 4.07 $\times 10^{-2}$ m^2/V, 4.32 $\times 10^{-2}$ m^2/V, 2.22 $\times 10^{-2}$ m^2/V,

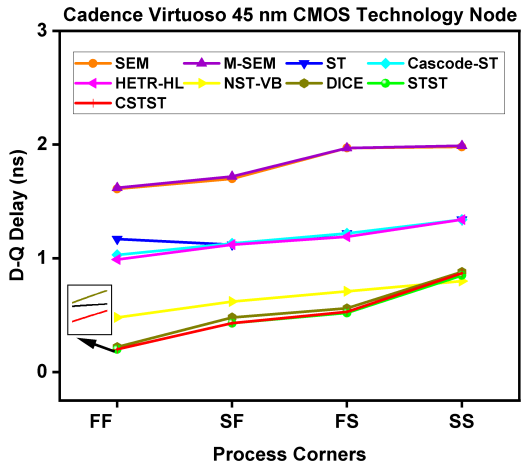


FIGURE 2.15: D-Q delay of proposed STST, CSTST and considered latches at different process corners.

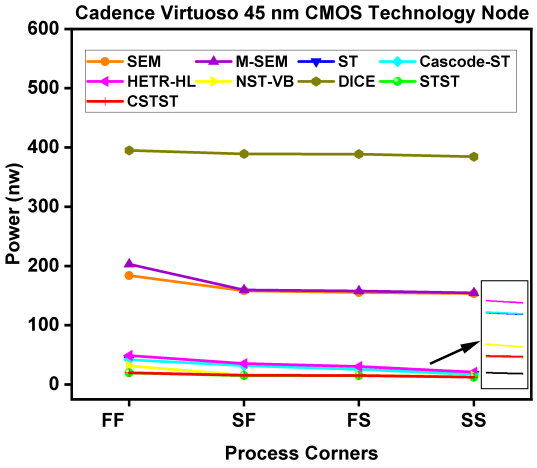


FIGURE 2.16: Power of proposed STST, CSTST and considered latches at different process corners.

3.40 $\times 10^{-2}$ m^2/V, 0.53 $\times 10^{-2}$ m^2/V, 20.20 $\times 10^{-2}$ m^2/V, and 22.57 $\times 10^{-2}$ m^2/V, respectively, and the same is presented in Table 2.1. The results show that the proposed CSTST latch achieves the highest QPAR compared to the reported latches.

Variability Analysis: The impact of various process corners for D-Q delay of all reported and proposed latches is shown in Figure 2.15. Similarly, the impact of various process corners on the power of all reported and proposed latches is shown in Figure 2.16. It

TABLE 2.1: Comparison of proposed STST, CSTST, and considered latches using 45 nm CMOS technology node.

Latches	Q_c **(fC)**	**Power (nW)**	**D-Q Delay (ns)**	**PDP (aJ)**	**Area** (μm^2)	**QPAR** ($\times 10^{-2}$ **m^2/V)**
SEM [27]	9.85	177.9	1.63	289.98	**6.47**	0.53
MSEM [27]	9.89	194.1	1.69	311.50	8.45	0.37
ST [27]	9.99	28.03	1.17	32.79	7.47	4.07
Cascade-ST [27]	10.59	27.91	1.17	32.79	7.47	4.32
HETR-HL [47]	10.03	32.49	1.14	36.49	12.40	2.22
NST-VB [50]	7.92	25.01	1.07	26.76	8.70	3.40
DICE [40]	10.55	388.6	0.54	209.84	9.45	0.53
Proposed STST	10.14	14.04	**0.46**	**6.46**	7.58	20.20
Proposed CSTST	**11.33**	**14.07**	0.47	6.61	7.58	**22.57**

TABLE 2.2: Mean and standard deviation in D-Q delay of proposed STST, CSTST and considered latches.

Latch	**Mean (ns)**	**Standard deviation (ns)**
SEM [27]	1.79	0.15
M-SEM [27]	1.79	0.14
ST [27]	1.17	0.10
Cascade-ST [27]	1.17	0.11
HETR-HL[47]	1.14	0.09
NST-VB [50]	1.12	0.23
DICE [40]	0.53	0.13
Proposed STST Latch	**0.47**	**0.09**
Proposed CSTST Latch	**0.48**	**0.09**

TABLE 2.3: Mean and standard deviation in power of proposed STST, CSTST and considered latches.

Latch	**Mean (nW)**	**Standard deviation (nW)**
SEM [27]	177.5	12.81
M-SEM [27]	194.3	13.83
ST [27]	28.14	3.77
Cacode-ST [27]	28.23	3.80
HETR-HL [47]	33.05	3.40
NST-VB [50]	26.41	6.23
DICE [40]	388.1	4.29
Proposed STST Latch	**14.45**	**0.94**
Proposed CSTST Latch	**14.49**	**0.85**

may be noted that the D-Q delay is lowest for all latches at FF corner, and higher value is observed at SS corner. The power shows the reverse trend i.e. power is lowest at SS corner and highest at FF corner for all latches. Tables 2.2 and 2.3 summarise the mean (μ) and standard deviation (σ) for D-Q delay and power, respectively. Simulation results show that, in comparison to the reported latches, the proposed latches is less sensitive to PVT variations for D-Q delay and power. The standard deviation (σ) in D-Q delay and power for proposed latches remains within 19% and 6% of corresponding mean value.

2.5 Proposed design 2

The proposed design 2 consists two radiation-hardened latches. The first is FTST based latch and the second is cascode four transistor Schmitt Trigger (CFTST) latch.

2.5.1 Proposed FTST latch

Figure 2.17 shows the schematic of the FTST latch. This circuit comprises a total of 12 transistors, including 7 NMOS and 5 PMOS transistors. The proposed design employs four key blocks: FTST block, transmission gate (T1), inverter (I1) in the forward path, and an inverter (I2) followed by transmission gate (T2) in the feedback path. In the forward signal path, the FTST block comprising transistors M1, M2, M3, and M4 is employed. The core hardening mechanism in this design involves enhancing the node capacitance at node IN1 by integrating the FTST block. In this design, D is the input, Q is the output, CLK is the clock signal, and NCK is its complement. When CLK is high, the latch operates in transparent mode; when CLK is low, it works in the hold mode. During the transparent phase, transmission gate T1 is active, while T2 is inactive, allowing the input D connect to output node Q as shown in the Figure 2.18, at this time, the feedback path is

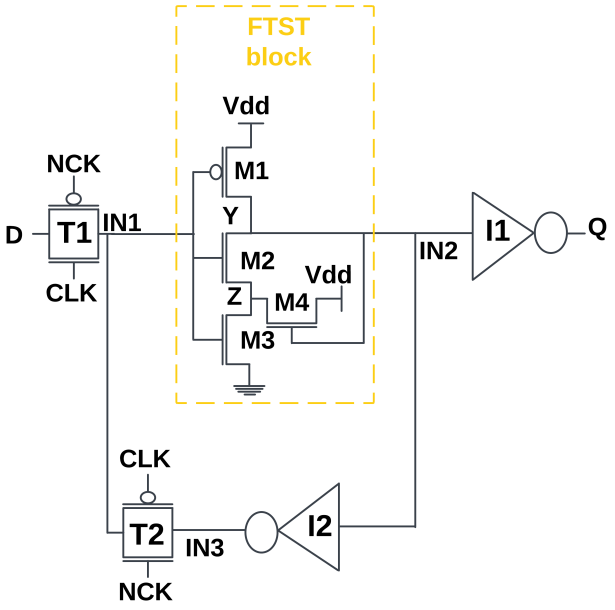


FIGURE 2.17: Schematic of proposed FTST latch.

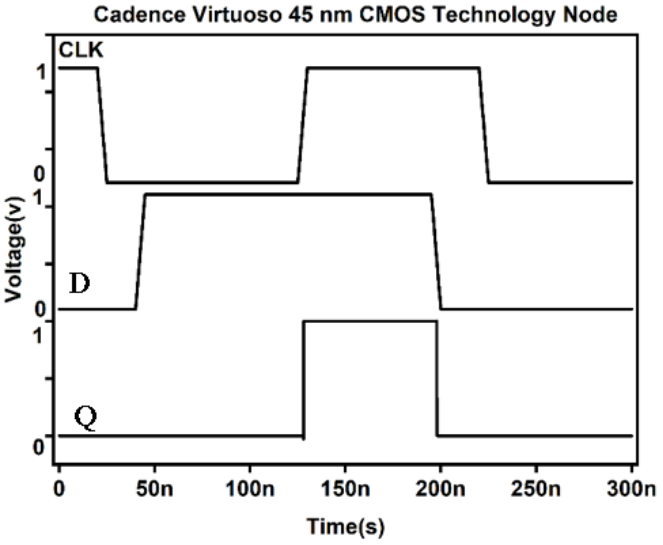


FIGURE 2.18: Simulation results of the FTST latch under fault-free case.

disconnected. Conversely, in hold mode, T1 turns OFF while T2 turns ON, disconnecting the input D from the output Q. However, the feedback loop is now active, hold the output logic state at node Q. It may be noted from Figure 2.18 that the output Q follows input D when CLK is high and retains its previous state otherwise. Now, the latch's behavior

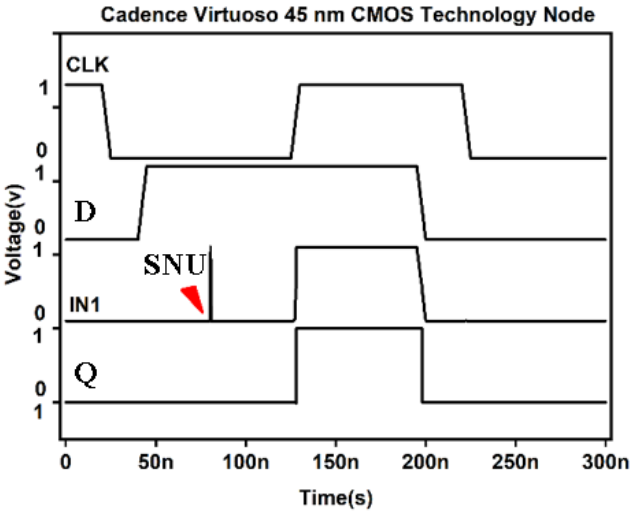


FIGURE 2.19: Simulation results of SNU injection case for FTST latch at node IN1.

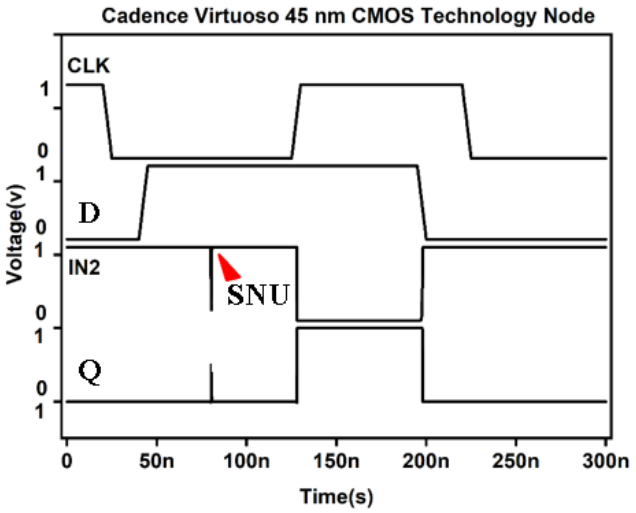


FIGURE 2.20: Simulation results of SNU injection case for FTST latch at node IN2.

under SEs during the hold mode is discussed. Let us assume node IN1 is at logic 0 and node IN2 is at logic 1. In this condition, node Z is charged, and transistor M4 is turned on. If a TF causes node IN1 to switch to logic 1, transistors M2 and M3 will be turned on, and the charge at node Z must be discharged before node IN2 can change its state. The effect of SNU at node IN1 and IN2 of the proposed design is shown in Figures 2.19 and 2.20, respectively. Furthermore, when a SNU occurs at node IN1 during hold mode, it

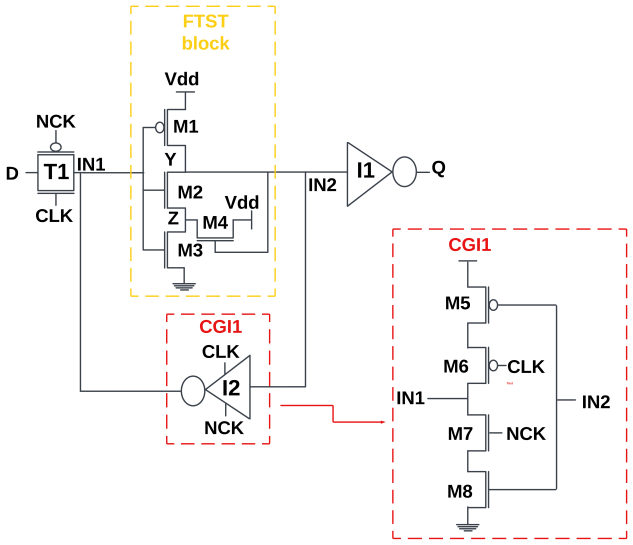


FIGURE 2.21: Schematic of proposed CFTST latch.

does not affect the output, confirming the latch's resilience to radiation-induced faults as shown in Figure 2.19.

2.5.2 Proposed CFTST latch.

Figure 2.21 shows the schematic of CFTST latch. This proposed design uses the same number of transistors as the earlier FTST latch; however, the key difference lies in replacing the transmission gate and inverter with a cascode feedback loop (CGI1). As stated in [48], while the transmission gate setup can mitigate the Miller effect, which can negatively impact performance in small-signal amplifiers, the cascode structure offers enhanced capability to escape metastability compared to its transmission gate-based counterpart. Both FTST and CFTST latches operate similarly when CLK is high and CLK is low. Thus, the operational explanation is not repeated. The corresponding timing diagram is shown in Figure 2.22. When CLK is at logic high, the input is passed to the output; when CLK is low, the output retains its state. Moreover, a SNU at node N1 during the hold phase

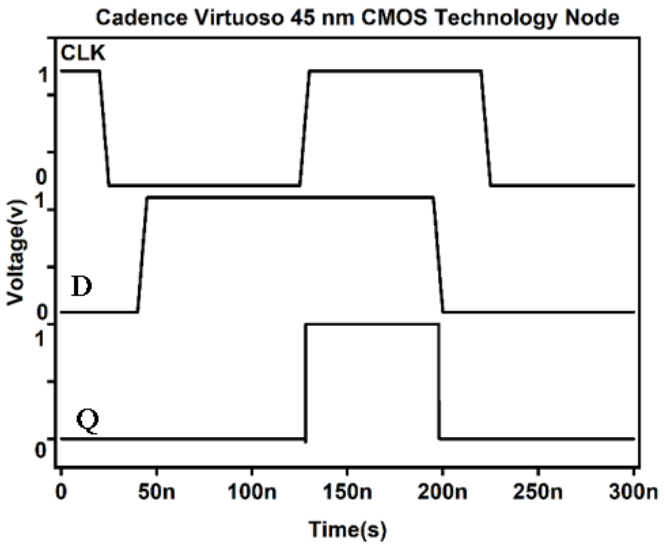


FIGURE 2.22: Simulation results of the CFTST latch under fault-free case.

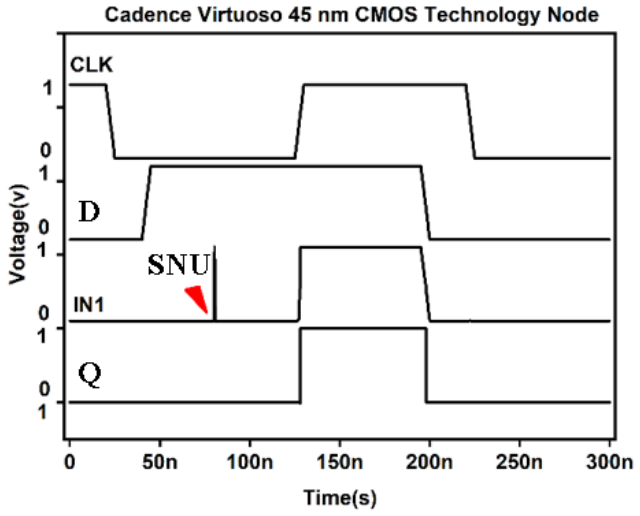


FIGURE 2.23: Simulation results of SNU injection case for CFTST latch at node IN1.

does not affect the output, confirming the radiation-hardened nature of the CFTST latch. The SNU at node IN1 and IN2 of the proposed design is shown in Figures 2.23 and 2.24, respectively. It clearly indicates that the effect of SNU occurring at IN1 is not transmitted to output. Thus, the radiation hardness of CFTST is verified.

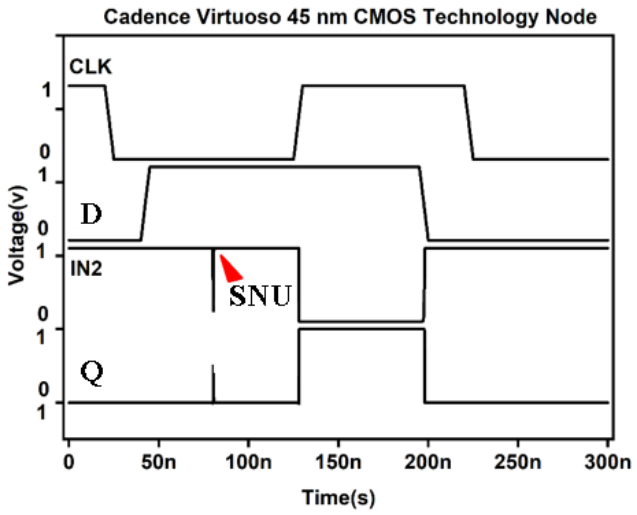


FIGURE 2.24: Simulation results of SNU injection case for CFTST latch at node IN2.

2.6 Performance evaluation

The simulation setup, operating conditions, and evaluation methodology adopted for proposed design 1 are consistently applied to proposed design 2. This ensures a fair performance comparison between the different proposed designs.

D-Q Delay: The value of D-Q delay for SEM [27], M-SEM [27], ST [27], Cacode-ST [27], HETR-HL [47], NST-VB [50], and the proposed FTST and CFTST are found to be 1.63 ns, 1.69 ns, 1.67 ns, 1.67 ns, 1.14 ns, 1.07 ns, 0.40 ns, and 0.41 ns, respectively, and the same is presented in Table 2.4. The results show that the proposed FTST and CFTST latches achieve the minimum D-Q delay compared to the reported latches. Moreover, the effects of variations in temperature and supply voltage are also examined, and the results are shown in Figures 2.25 and 2.26, respectively. It can be observed that the proposed designs shows better results in the entire voltage and temperature range as compared to other reported designs.

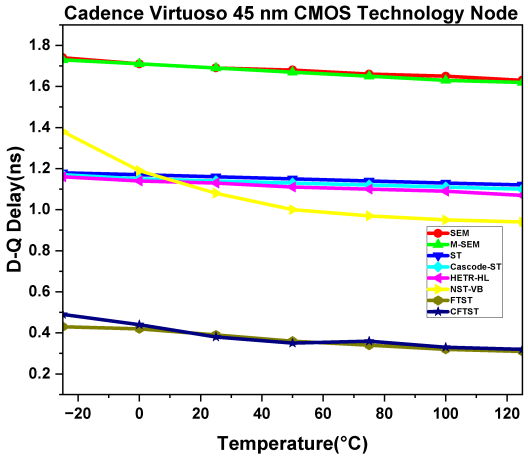


FIGURE 2.25: Effect of temperature variation on the D-Q delay of proposed FTST, CFTST and considered latches.

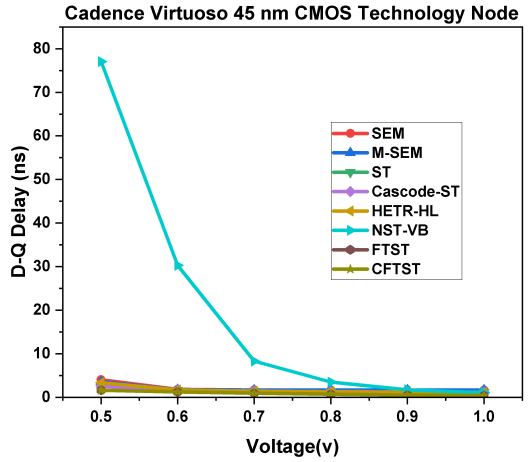


FIGURE 2.26: Effect of supply voltage variation on the D-Q delay of proposed FTST, CFTST and considered latches.

Power: The value of power for SEM [27], M-SEM [27], ST [27], Cacode-ST [27], HETR-HL [47], NST-VB [50], and the proposed FTST and CFTST are found to be 177.9 nW, 194.1 nW, 28.03 nW, 27.91 nW, 32.49 nW, 25.01 nW, 10.59 nW, and 10.61 nW, respectively, and the same is presented in Table 2.4. The results show that the proposed FTST and CFTST latches consume significantly lower power compared to the reported latches. Moreover, the effects of variations in temperature and supply voltage are also examined,

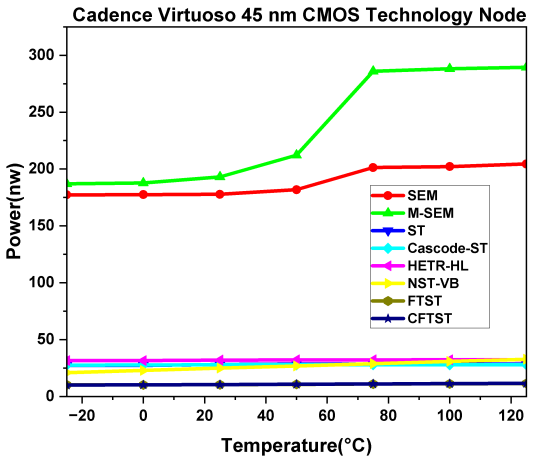


FIGURE 2.27: Effect of temperature variation on the power of proposed FTST, CFTST and considered latches

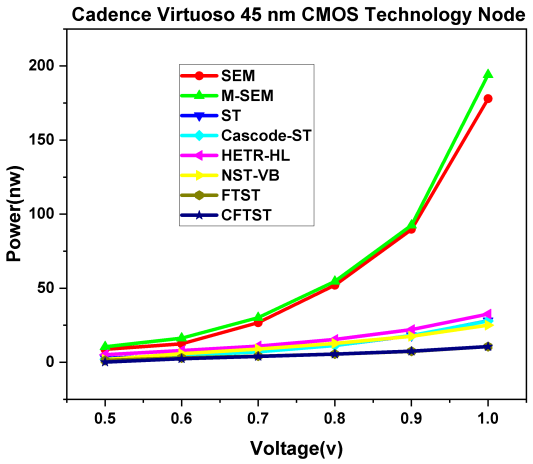


FIGURE 2.28: Effect of supply voltage variation on the power of proposed FTST, CFTST and considered latches.

and the results are shown in Figures 2.27 and 2.28, respectively. It can be observed that the proposed designs shows better results in the entire voltage and temperature range as compared to other reported design.

Critical charge: The value of Qc for SEM [27], M-SEM [27], ST [27], Cacode-ST [27], HETR-HL [47], NST-VB [50], and the proposed FTST and CFTST are found to be 9.85 fC, 9.89 fC, 9.99 fC, 10.59 fC, 10.03 fC, 7.92 fC, 10.09 fC, and 10.93 fC, respectively,

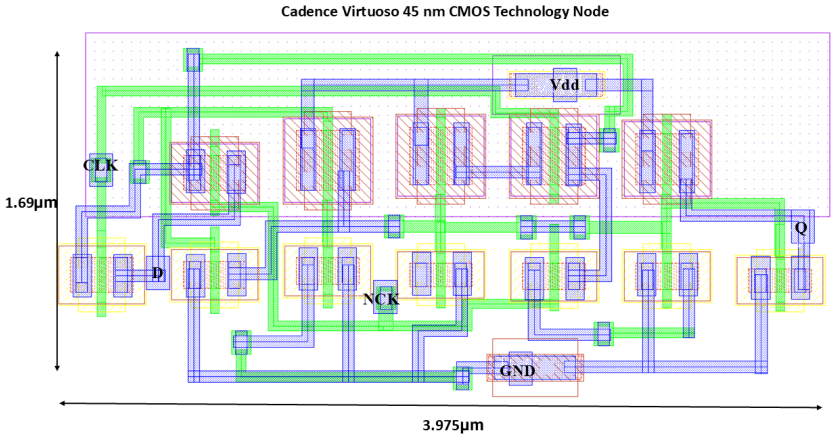


FIGURE 2.29: Layout for proposed CFTST latch.

and the same is presented in Table 2.4. The results show that the proposed CFTST latch achieves the highest Qc compared to the reported latches.

Area: The value of area for SEM [27], M-SEM [27], ST [27], Cacode-ST [27], HETR-HL [47], NST-VB [50], and the proposed FTST and CFTST are found to be 6.47 μm^2, 8.45 μm^2, 7.47 μm^2, 7.47 μm^2, 12.40 μm^2, 8.70 μm^2, 6.72 μm^2, and 6.72 μm^2, respectively, and the same is presented in Table 2.4. The results show that the proposed FTST and CFTST latches occupy the lesser area compared to M-SEM [27], ST [27], Cacode-ST [27], HETR-HL [47], and NST-VB [50]. The proposed CFTST latch layout is shown in Figure 2.29. The post-layout results show variations of 7.72%, 14.52%, and 4.94% in power, delay, and critical charge, respectively, for the CFTST latch.

PDP: The value of PDP for SEM [27], MSEM [27], ST [27], Cascode-ST [27], HETR-HL [47], NST-VB [50], FTST, CFTST are found to be 289.98 aJ, 311.50 aJ, 32.79 aJ, 32.79 aJ, 36.49 aJ, 26.76 aJ, 4.26 aJ and 4.36 aJ respectively and same is presented in Table 2.4. The results show that the proposed FTST and CFTST latches significantly lower PDP compared to the reported latches.

QPAR: The value of QPAR for SEM [27], M-SEM [27], ST [27], Cacode-ST [27],

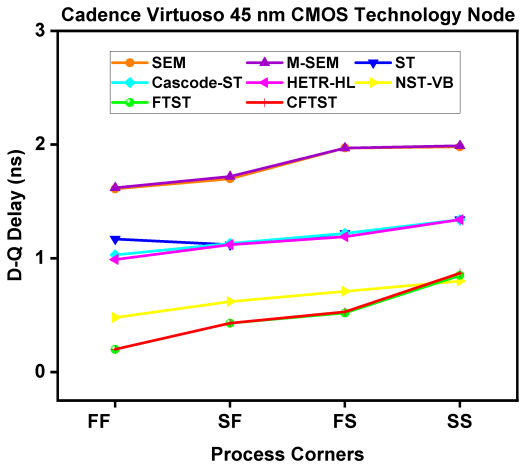


FIGURE 2.30: D-Q delay of proposed FTST, CFTST and considered latches at different process corners.

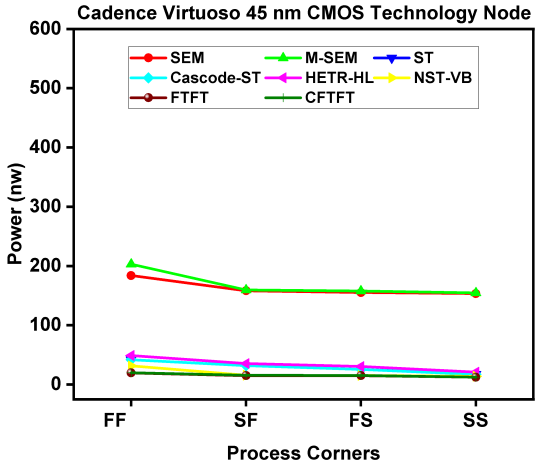


FIGURE 2.31: Power of proposed FTST, CFTST and considered latches at different process corners.

HETR-HL [47], NST-VB [50], and the proposed FTST and CFTST are found to be 0.53 $\times 10^{-2}$ m^2/V, 0.37 $\times 10^{-2}$ m^2/V, 4.07 $\times 10^{-2}$ m^2/V, 4.32 $\times 10^{-2}$ m^2/V, 2.22 $\times 10^{-2}$ m^2/V, 3.40 $\times 10^{-2}$ m^2/V, 35.25 $\times 10^{-2}$ m^2/V, and 37.30 $\times 10^{-2}$ m^2/V, respectively, and the same is presented in Table 2.4. The results show that the proposed FTST and CFTST latches achieve the higher QPAR compared to the reported latches.

Variability Analysis: The impact of various process corners for D-Q delay of all reported

TABLE 2.4: Comparison of proposed FTST, CFTST and considered latches using 45 nm CMOS technology node

Latches	Q_c **(fC)**	**Power (nW)**	**D-Q Delay (ns)**	**PDP (aJ)**	**Area** (μm^2)	**QPAR** ($\times 10^{-2}$ m^2/V)
SEM [27]	9.85	177.9	1.63	289.98	**6.47**	0.53
M-SEM [27]	9.89	194.1	1.69	311.50	8.45	0.37
ST [27]	9.99	28.03	1.67	32.79	7.47	4.07
Cacode-ST [27]	10.59	27.91	1.67	32.79	7.47	4.32
HETR-HL [47]	10.03	32.49	1.14	36.49	12.40	2.22
NST-VB [50]	7.92	25.01	1.07	26.76	8.70	3.40
Proposed FTST	10.09	**10.59**	**0.40**	**4.26**	6.72	35.25
Proposed CFTST	**10.93**	10.61	0.41	4.36	6.72	**37.30**

TABLE 2.5: Mean and standard deviation in D-Q delay of proposed FTST, CFTST and considered latches.

Latch	**Mean (ns)**	**Standard deviation (ns)**
SEM [27]	1.79	0.15
M-SEM [27]	1.79	0.14
ST [27]	1.17	0.10
Cascade-ST [27]	1.17	0.11
HETR-HL[47]	1.14	0.09
NST-VB [50]	1.12	0.23
Proposed FTST Latch	**0.37**	**0.06**
Proposed CFTST Latch	**0.38**	**0.06**

TABLE 2.6: Mean and standard deviation in power of proposed FTST, CFTST and considered latches.

Latch	**Mean (nW)**	**Standard deviation (nW)**
SEM [27]	177.5	12.81
M-SEM [27]	194.3	13.83
ST [27]	28.14	3.77
Cacode-ST [27]	28.23	3.80
HETR-HL [47]	33.05	3.40
NST-VB [50]	26.41	6.23
Proposed FTST Latch	**10.20**	**0.82**
Proposed CFTST Latch	**10.59**	**0.81**

and proposed latches is shown in Figure 2.30. Similarly, the impact of various process corners on the power of all reported and proposed latches is shown in Figure 2.31. It

may be noted that the D-Q delay is lowest for all latches at FF corner, and higher value is observed at SS corner. The power shows the reverse trend i.e. power is lowest at SS corner and highest at FF corner for all latches. Tables 2.5 and 2.6 summarise the mean (μ) and standard deviation (σ) for D-Q delay and power, respectively. Simulation results show that, in comparison to the reported latches, the proposed latches is less sensitive to PVT variation for D-Q delay and power. The standard deviation (σ) in D-Q delay and power for proposed latches remains within 16% and 8% of corresponding mean value.

2.7 Comparison

This section compares the performance of proposed design 1 and design 2 in terms of D–Q delay, power, Qc, area, PDP, and QPAR, and the findings are placed in Table 2.7. The comparison shows that proposed design 2 achieves lower power, reduced D–Q delay, lower PDP, smaller area, and improved QPAR, indicating better radiation tolerance capability. On the other hand, proposed CFTST design 2 exhibits higher Qc. The layouts of the proposed circuits were implemented in 45 nm CMOS, followed by parasitic RC extraction. The extracted parasitics were then included in the post-layout simulations to evaluate their impact on power, D-Q delay, critical charge, and PDP. The post-layout results show variations of 8.24% in power, 15.32% in delay, 5.68% in critical charge, and 24.82% in PDP for STST; 8.44% in power, 15.61% in delay, 5.92% in critical charge, and 25.37% in PDP for CSTST; 7.41% in power, 14.63% in delay, 4.82% in critical charge, and 23.12% in PDP for FTST; and 7.72% in power, 14.52% in delay, 4.94% in critical charge, and 23.36% in PDP for CFTST, respectively.

TABLE 2.7: Performance comparison of proposed (design 1 and design 2) using 45 nm CMOS technology node

Latches	Q_c (fC)	Power (nW)	D-Q Delay (ns)	PDP (aJ)	Area (μm^2)	QPAR ($\times 10^{-2}$ m^2/V)
Design 1 (STST)	10.14	14.04	0.46	6.46	7.58	20.20
Design 1 (CSTST)	**11.33**	14.07	0.47	6.61	7.58	22.57
Design 2 (FTST)	10.09	**10.59**	**0.40**	**4.26**	**6.72**	35.25
Design 2 (CFTST)	10.93	10.61	0.41	4.36	**6.72**	**37.30**

2.8 Summary

This chapter presents two radiation-hardened latches (proposed design 1 and proposed design 2) that can effectively eliminate SNU. The STST (design 1) latch has a lower D-Q delay of 57%, a higher Qc of 28.03%, a lower power of 43.86%, PDP of 75.86%, and a higher QPAR of 494.12% with a decreased area of 12.87% than recently proposed latch NST-VB[50]. The CSTST (design 1) latch, has a cascode feedback loop in place of a transmission gate and inverter with an improved critical charge of 11.74% and QPAR of 11.73% than the STST latch without an area increase. The proposed CSTST latch shows 60.87% and 86.36% lower standard deviation for D-Q delay and power, respectively, compared to the recently reported NST-VB latch [50]. The proposed design 1 is capable of recovering from SNUs but at the cost of more power, larger D-Q delay and area overhead. Therefore, proposed design 2 is offered to solve this issue by reducing the number of transistors. The FTST (design 2) latch has a lower D-Q delay of 62.62%, a higher Qc of 27.40%, a lower power of 57.65%, PDP of 82.76%, and a higher QPAR of 936.76% with a decreased area of 22.76% than recently proposed latch NST-VB[50]. The CFTST (design 2) latch, has a cascode feedback loop in place of a transmission gate and inverter with an improved critical charge of 8.32% and QPAR of 5.82% than the FTST latch without an area increase. The proposed CFTST latch shows 51.02% and 54.97% lower standard deviation for D-Q delay and power, respectively, compared to the recently

reported NST-VB latch [50].

Chapter 3

Muller C- Element Based TNU Hardened Latch

The results described in this chapter have been published as the following peer-reviewed publication:

* N. Kumar, C. I. Kumar, and N. Pandey, **High-performance and robust triple-node-upset radiation hardened latch design,"** AEÜ – Int. J. Electron. Commun., vol. 201, July 2025, 10.1016/j.aeue.2025.155977.

3.1 Introduction

The proposed designs of the previous chapter were capable of tolerating only single-node upsets (SNUs) due to transient fault (TF). Although these designs improved reliability to some extent however, they were unable to recover from triple-node upsets (TNUs), which can significantly affect the robustness and operational reliability of latch circuits in radiation prone environments (cosmic rays and alpha particles). Therefore, there exists a strong requirement for advanced latch design, which is capable of tolerating TNUs while maintaining performance. To overcome this limitation, this chapter presents an muller c-element (MCE) based radiation hardened latch design aimed at improved resilience against TNUs, ensuring higher reliability under severe radiation-induced fault conditions. The proposed design incorporates Multiple MCEs, clock gated muller C-elements (CG-MCEs) to enhance the fault recovery mechanism against TNUs.

The working principle and implementation are presented in Section 3.2. Soft error robustness of the proposed TNU hardened latch is presented in Section 3.3. Performance evaluation is presented in Section 3.4, and Section 3.5 summarizes the findings.

3.2 Proposed design 3

The schematic of the proposed triple node upset radiation-hardened (TNURH) latch is shown in Figure 3.1. The basic building block of the TNURH latch is 4-input Muller C-elements (4MCEs) and clock-gated 4-input Muller C-elements (CG-4MCEs). Both 4MCE and CG-4MCE circuits have the ability to block SEs when a TF occurs at its one

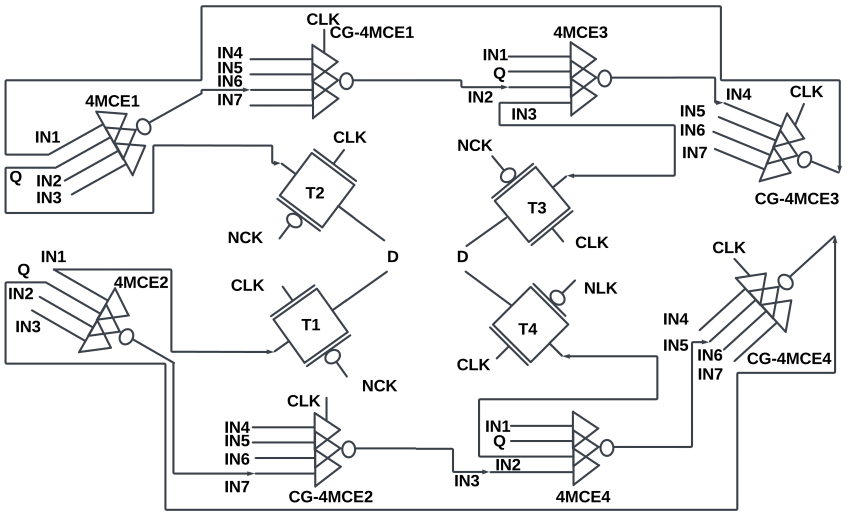


FIGURE 3.1: Schematic of proposed TNURH latch.

of the input nodes. The TNURH latch consists of four transmission gates (T1, T2, T3, and T4), four 4MCEs (4MCE1, 4MCE2 and 4MCE3, 4MCE4) and four CG-4MCEs (CG-4MCE1, CG-4MCE2, CG-4MCE3 and CG-4MCE4). The input and output signals are D and Q, respectively. The CLK and NCK, correspond to a clock signal and a inverted clock signal. When CLK = 1 and NCK = 0, all the transmission gates (T1, T2, T3, and T4) are turned on, and the latch works in a transparent mode. The data transfers from the input D to the output Q through the T2. The CG-4MCEs are disabled in the transparent mode to minimize power and D-Q delay. In the hold mode (CLK = 0 and NCK = 1), all transmission gates (T1, T2, T3, and T4) are turned off. The CG-4MCEs are turned on; therefore, the output of the CG-4MCEs retains the latch state. The simulated waveforms of the proposed TNURH latch in an error-free scenario are shown in Figure 3.2. Let us consider a transparent mode case when CLK = 1, NCK = 0, and D = 1, then all transmission gates (T1, T2, T3, and T4) transmit data to the following respective stages. The logical values of respective internal nodes are IN1 = 1, IN2 = 1, IN3 = 1, IN4 = 0, IN5 = 0, IN6 = 0, IN7 = 0, and output Q = 1. Now, logical state of the four nodes, namely IN4 = 0, IN5 = 0, IN6 = 0, and IN7 = 0, will pass through CG-4MCE4, then output Q of CG-4MCE4 will be in the previous state because CG-4MCE4 is disabled in

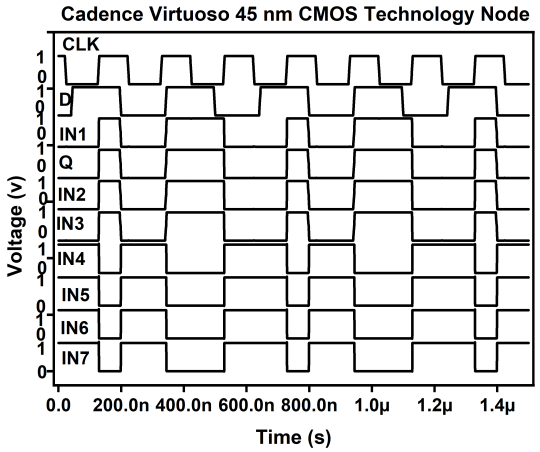


FIGURE 3.2: Simulation waveforms of the fault-free case for the proposed TNURH latch design.

the transparent mode. Similarly, in hold mode case when CLK = 0, NCK = 1, and D=1, then all the transmission gates (T1, T2, T3, and T4) are turned off. The CG-4MCE4 is turned on, which was off in transparent mode; therefore, the output of the CG-4MCE4 retains the latch state, and output Q will remain at logic 1.

The fundamental principle of the soft-error hardening of the proposed latch is described as follows. Assume that a TF happens at one of the internal susceptible nodes (IN1, IN2, IN3, IN4, IN5, IN6, and IN7) and output Q in the hold mode when CLK = 0 and NCK = 1. This TF never changes the latch's output signal since CG-4MCEs can restore the corrupted node's states. The proposed latch retains the output node Q in the correct state when SNU/DNU/TNU are present. The advantage of proposed approach is that it enhances the radiation-hardened ability without any cost of delay, power, and area.

3.3 Fault tolerance and recovery analysis (SNU / DNU / TNU)

In this section, the proposed TNURH latch tolerance and recovery analysis against SNU, DNU, and TNU is analyzed individually for each case. Additionally, we abstract the schematic by using internal nodes of the proposed TNURH latch to analyze the tolerance and recovery, as shown in Figure 3.1. Let us consider a transparent mode case when CLK = 1, NCK = 0, and D = 1, then the output of all transmission gates (T1, T2, T3, and T4) transmit data to the following respective stages. The logical states of respective internal nodes are IN1 = 1, IN2 = 1, IN3 = 1, IN4 = 0, IN5 = 0, IN6 = 0, IN7 = 0, and output Q = 1. Now, we will check the sensitivity of the circuit against TFs in hold mode (CLK = 0 and NCK = 1).

3.3.1 SNU fault tolerance and recovery analysis

In this case, eight possible scenarios exist, which are divided into two cases. Case S1: TF occurs inside 4MCE, and Case S2: TF occurs inside CG-4MCE.

Case S1: In this case, we have considered that one TF occurs at the input of any 4MCE (here we consider 4MCE3). Suppose a TF strikes at node Q, then the logical value of node Q instantly flips from 1 to 0. Now, the internal nodes of 4MCE3 are IN1 = 1, Q = 0, IN2 = 1, and IN3 = 1. However, the output of 4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node Q of CG-4MCE4 is restored at logic 1 because all the inputs of CG-4MCE4 are held at logic 0. Therefore, the correct logic value is restored at node Q. Similarly, SNU fault tolerance and recovery analysis is carried out if TF occurs at other internal nodes like IN1, IN2, and IN3.

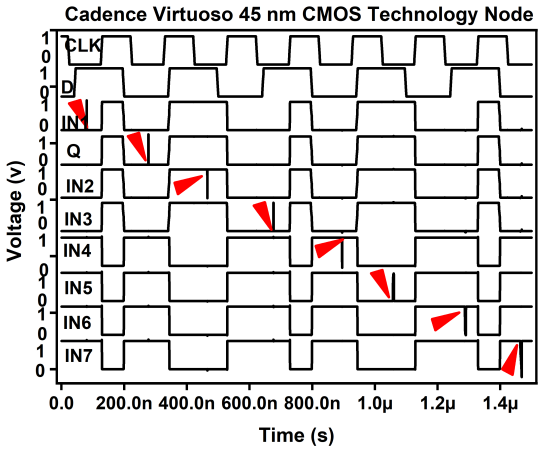


FIGURE 3.3: Simulation waveforms of SNU injections for the proposed TNURH latch design.

Case S2: In this case, we have considered the one TF occurs at the input of any CG-4MCE (here we consider CG-4MCE3). Suppose a TF strikes at node IN4, then the logical value of node IN4 instantly flips from 0 to 1. Now internal nodes of CG-4MCE3 are IN4 = 1, IN5 = 0, IN6 = 0, and IN7 = 0. However, the output of CG-4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node IN4 of 4MCE3 is restored at logic 0 because all the inputs of 4MCE3 are at logic 1. Therefore, the correct logic value is restored at node IN4. Similarly, SNU fault tolerance and recovery analysis is carried out if TF occurs at other internal nodes like IN5, IN6, and IN7. As shown in Figure 3.3, all sensitive nodes can be tolerant and recover. This confirms that the proposed TNURH latch is completely recovering from SNU.

3.3.2 DNU fault tolerance and recovery analysis

In this case, twenty-eight possible scenarios exist, which are divided into three cases. Case D1: two TFs occur inside 4MCE, Case D2: two TFs occur inside CG-4MCE and Case D3: one TF occurs inside 4MCE and one TF occurs inside CG-4MCE.

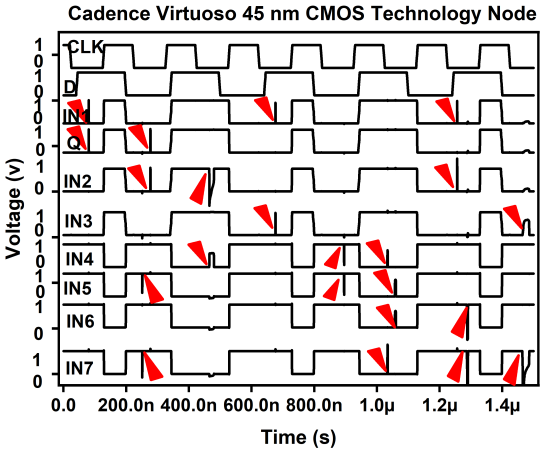


FIGURE 3.4: Simulation waveforms of DNU injections for the proposed TNURH latch design.

Case D1: In this case, we have considered that two TFs occur at the input of any 4MCE (here we consider 4MCE3). Suppose two TFs occur at pairs of nodes IN1 and Q, then IN1 flips from 1 to 0, and Q also flips from 1 to 0. Now, the internal nodes of 4MCE3 are IN1 = 0, Q = 0, IN2 = 1, and IN3 = 1. However, the output of 4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node IN1 of CG-4MCE3 is restored at logic 1 because all the inputs of CG-4MCE3 are at logic 0. The output node Q of CG-4MCE4 is restored at logic 1 because all the inputs of CG-4MCE4 are at logic 0. Therefore, the correct logic value is restored at nodes IN1 and Q, respectively. Similarly, DNU fault tolerance and recovery analysis is carried out if TF occurs at other internal node pairs like (IN1, IN2), (IN1, IN3), (Q, IN2), (Q, IN3), (IN2, IN3).

Case D2: In this case, we have considered that two TFs occur at the input of any CG-4MCE (here we consider CG-4MCE3). Suppose two TFs occur at pairs of nodes IN4 and IN5, then IN4 flips from 0 to 1, and IN5 also flips from 0 to 1. Now, the internal nodes of CG-4MCE3 are IN4 = 1, IN5 = 1, IN6 = 0, and IN7 = 0. However, the output of CG-4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node IN4 of 4MCE3 is restored at logic 0 because all the inputs of 4MCE3 are at logic 1. The output node IN5 of 4MCE4 is restored at logic 0 because all the inputs

of 4MCE4 are at logic 1. Therefore, the correct logic value is restored at nodes IN4 and IN5, respectively. Similarly, DNU fault tolerance and recovery analysis is carried out if TF occurs at other internal node pairs like (IN4, IN6), (IN4, IN7), (IN5, IN6), (IN5, IN7), (IN6, IN7).

Case D3: In this case, we have considered that one TF occurs at the input of any 4MCE (here we consider 4MCE3) and one TF occurs at the input of any CG-4MCE (here we consider CG-4MCE3). In this case, we have taken one internal node from 4MCE3 and another from CG-4MCE3, namely IN2 and IN7, respectively. Suppose TFs occur at pairs of nodes IN2 and IN7, then IN2 flips from 1 to 0, and IN7 also flips from 0 to 1. Now, the internal nodes of 4MCE3 and CG-4MCE3 are IN1 = 1, Q = 1, IN2 = 0, IN3 = 1, IN4 = 0, IN5 = 0, IN6 = 0, and IN7 = 1, respectively. However, the outputs of 4MCE3 and CG-4MCE3 are unaffected due to their fault tolerance and recovery characteristics. The output node IN2 of CG-4MCE1 is restored at logic 1 because all the inputs of CG-4MCE1 are at logic 0. The output node IN7 of 4MCE2 is restored at logic 1 because all the inputs of 4MCE2 are at logic 0. Therefore, the correct logic value is restored at nodes IN2 and IN7, respectively. Similarly, DNU fault tolerance and recovery analysis is carried out if TFs occur at other internal node pairs like (IN1, IN4),(IN1, IN5),(IN1, IN6),(IN1, IN7),(Q, IN4),(Q, IN5),(Q, IN6),(Q, IN7),(IN2, IN4), (IN2, IN6),(IN2, IN7),(IN3, IN4),(IN3, IN5),(IN3, IN6),(IN3, IN7). As shown in Figure 3.4, all sensitive nodes can be tolerant and recover. This confirms that the proposed TNURH latch is completely recovering from DNU.

3.3.3 TNU fault tolerance and recovery analysis

In this case, fifty six possible scenarios exist, which are divided into four cases. Case T1: three TFs occur inside 4MCE, Case T2: three TFs occur inside CG-4MCE and Case

T3: two TFs occur inside 4MCE and one TF occurs inside CG-4MCE. Case S4: one TF occurs inside 4MCE and two TFs occur inside CG-4MCE.

Case T1: In this case, we have considered that three TFs occur at the input of any 4MCE (here we consider 4MCE3). Suppose TFs occur at all considered nodes IN1, Q, and IN2, then IN1 flips from 1 to 0, Q flips from 1 to 0 and IN2 also flips from 1 to 0. Now, the internal nodes of 4MCE3 are IN1 = 0, Q = 0, IN2 = 0, and IN3 = 1. However, the output of 4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node IN1 of CG-4MCE3 is restored at logic 1 because all the inputs of CG-4MCE3 are at logic 0. The output node Q of CG-4MCE4 is restored at logic 1 because all the inputs of CG-4MCE4 are at logic 0. The output node IN2 of CG-4MCE1 is restored at logic 1 because all the inputs of CG-4MCE1 are at logic 0. Therefore, the correct logic value is restored at nodes IN1, Q, and IN2, respectively. Similarly, TNU fault tolerance and recovery analysis is carried out if TFs occur at other internal node triplets like (IN1, Q, IN3),(IN1, IN2, IN3),(Q, IN2, IN3).

Case T2: In this case, we have considered that three TFs occur at the input of any CG-4MCE (here we consider CG-4MCE3). Suppose TFs occur at all considered nodes IN4, IN5, and IN6, then IN4 flips from 0 to 1, IN5 flips from 0 to 1, and IN6 also flips from 0 to 1. Now, the internal nodes of CG-4MCE3 are IN4 = 1, IN5 = 1, IN6 = 1, and IN7 = 0. However, the output of CG-4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node IN4 of 4MCE3 is restored at logic 0 because all the inputs of 4MCE3 are at logic 1. The output node IN5 of 4MCE4 is restored at logic 0 because all the inputs of 4MCE4 are at logic 1. The output node IN6 of 4MCE1 is restored at logic 0 because all the inputs of 4MCE1 are at logic 1. Therefore, the correct logic value is restored at nodes IN4, IN5, and IN6, respectively. Similarly, TNU fault tolerance and recovery analysis is carried out if TFs occur at other internal node triplets like (IN4, IN5, IN7),(IN4, IN6, IN7),(IN5, IN6, IN7).

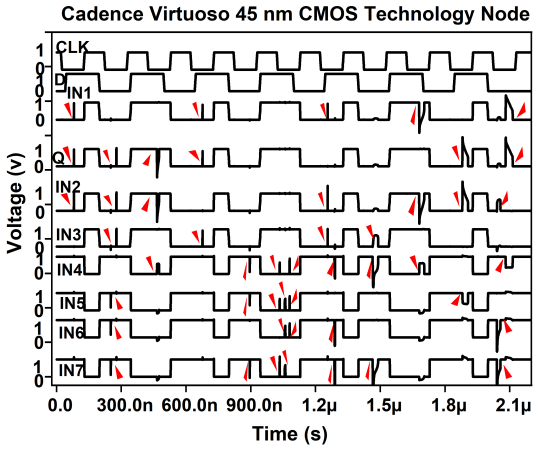


FIGURE 3.5: Simulation waveforms of TNU injections for the proposed TNURH latch design.

Case T3: In this case, we have considered that two TFs occur at the input of any 4MCE (here we consider 4MCE3) and one TF occurs at the input of any CG-4MCE (here we consider CG-4MCE3). Suppose TFs occur at all considered nodes IN1, Q, and IN6, then IN1 flips from 1 to 0, Q flips from 1 to 0, and IN6 also flips from 0 to 1. Now, the internal nodes of 4MCE3 and CG-4MCE3 are IN1 = 0, Q = 0, IN2 = 1 , IN3 = 1, IN4 = 0, IN5 = 0, IN6 = 1, and IN7 = 0, respectively. However, the output of 4MCE3 and CG-4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node IN1 of CG-4MCE3 is restored at logic 1 because all the inputs of CG-4MCE3 are at logic 0. The output node Q of CG-4MCE4 is restored at logic 1 because all the inputs of CG-4MCE4 are at logic 0. The output node IN2 of CG-4MCE1 is restored at logic 1 because all the inputs of CG-4MCE1 are at logic 0. The output node IN6 of 4MCE1 is restored at logic 0 because all the inputs of 4MCE1 are at logic 1. Therefore, the correct logic value is restored at nodes IN1, Q, and IN6, respectively. Similarly, TNU fault tolerance and recovery analysis is carried out if TFs occur at other internal node triplets like (IN1, Q, IN4), (IN1, Q, IN5), (IN1, Q, IN7), (IN1, IN2, IN4), (IN1, IN2, IN5), (IN1, IN2, IN6), (IN1, IN2, IN7), (IN1, IN3, IN4), (IN1, IN3, IN5), (IN1, IN3, IN6), (IN1, IN3, IN7), (Q, IN2, IN4), (Q, IN2, IN5), (Q, IN2, IN6), (Q, IN2, IN7), (Q, IN3, IN4), (Q, IN3, IN5), (Q,

IN3, IN6), (Q, IN3, IN7), (IN2, IN3, IN4), (IN2, IN3, IN5), (IN2, IN3, IN6), and (IN2, IN3, IN7).

Case T4: In this case, we have considered that one TF occurs at the input of any 4MCE (here we consider 4MCE3) and two TFs occur at the input of any CG-4MCE (here we consider CG-4MCE3). Suppose TFs occur at all considered nodes IN1, IN5, and IN6, then IN1 flips from 1 to 0, IN5 flips from 0 to 1, and IN6 also flips from 0 to 1. Now, the internal nodes of 4MCE3 and CG-4MCE3 are IN1 = 0, Q = 1, IN2 = 1, IN3 = 1, IN4 = 0, IN5 = 1, IN6 = 1, and IN7 = 0, respectively. However, the output of 4MCE3 and CG-4MCE3 is unaffected due to its fault tolerance and recovery characteristics. The output node IN1 of CG-4MCE3 is restored at logic 1 because all the inputs of CG-4MCE3 are at logic 0. The output node IN5 of 4MCE4 is restored at logic 0 because all the inputs of 4MCE4 are at logic 1. The output node IN6 of 4MCE1 is restored at logic 0 because all the inputs of 4MCE1 are at logic 1. Therefore, the correct logic value is restored at nodes IN1, IN5, and IN6, respectively. Similarly, TNU fault tolerance and recovery analysis is carried out if TFs occur at other internal node triplets like (IN1, IN4, IN5), (IN1, IN4, IN6), (IN1, IN4, IN7), (IN1, IN5, IN7), (IN1, IN6, IN7), (Q, IN4, IN5), (Q, IN4, IN6), (Q, IN4, IN7), (Q, IN5, IN6), (Q, IN5, IN7), (Q, IN6, IN7), (IN2, IN4, IN5), (IN2, IN4, IN6), (IN2, IN4, IN7),(IN2, IN5, IN6),(IN2, IN5, IN7),(IN2, IN6, IN7),(IN3, IN4, IN5), (IN3, IN4, IN6), (IN3, IN4, IN7), (IN3, IN5, IN6), (IN3, IN5, IN7), (IN3, IN6, IN7). As shown in Figure 3.5, all sensitive nodes can be tolerant and recover. This confirms that the proposed TNURH latch is completely recovering from TNU.

3.4 Performance evaluation

The simulation setup, operating conditions, and evaluation methodology are discussed in Section 2.3, and same is adopted for the proposed Design 3.

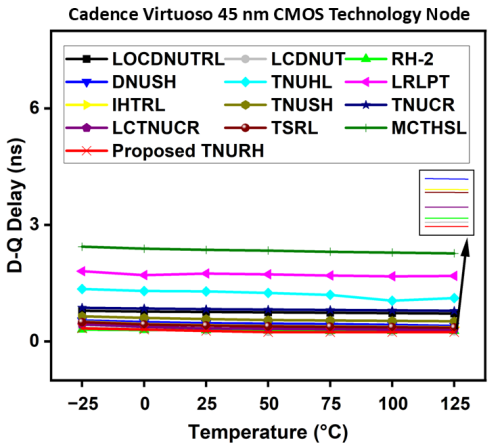


FIGURE 3.6: Effect of temperature variation on the D-Q delay of proposed TNURH and considered latches.

D-Q Delay: The value of D-Q delay for the conventional D-latch [27], DICE [40], FERST [42], ST [27], TMR [41], LOCDNUTRL [57], LCDNUT [39], RH-2 [64], DNUSH [56], TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and the proposed TNURH are found to be 0.47 ns, 0.49 ns, 0.85 ns, 1.07 ns, 1.43 ns, 0.74 ns, 0.28 ns, 0.28 ns, 0.46 ns, 1.27 ns, 1.76 ns, 0.43 ns, 0.57 ns, 0.83 ns, 0.34 ns, 0.43 ns, 2.36 ns, and 0.26 ns, respectively, and the same is presented in Table 3.1. The results show that the proposed TNURH latch achieves minimum D-Q delay compared to the reported latches. Moreover, the effects of variations in temperature and supply voltage are also simulated, and the results are shown in Figures 3.6 and 3.7, respectively. It can be observed that the proposed designs shows better results in the entire voltage and temperature range as compared to the reported latches.

Power: The value of power for the conventional D-latch [27], DICE [40], FERST [42], ST [27], TMR [41], LOCDNUTRL [57], LCDNUT [39], RH-2 [64], DNUSH [56], TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and the proposed TNURH are found to be 0.04 μW, 0.18 μW, 0.12 μW, 0.20 μW, 154.2 μW, 8.44 μW, 0.33 μW, 3.22 μW, 0.54 μW, 1.27 μW, 0.51 μW,

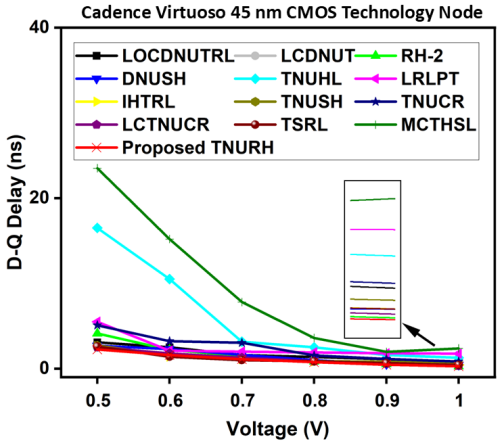


FIGURE 3.7: Effect of supply voltage variation on the D-Q delay of proposed TNURH and considered latches

0.79 μW, 1.11 μW, 1.04 μW, 1.51 μW, 0.78 μW, 6.55 μW, and 0.94 μW, respectively, and the same is presented in Table 3.1. The proposed TNURH latch has a moderate power compared to the TNU latches, such as TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88] and MCTHSL [78]. However, the proposed latch design has high power as compared to LRLPT [76], IHTRL [75], and TSRL [88], but the reported latches have large D-Q delay. Moreover, the effects of variations in temperature and supply voltage are also simulated, and the results are shown in Figures 3.8 and 3.9, respectively. It can be observed that the proposed design shows better results in the entire voltage and temperature range as compared to the reported latches.

Critical Charge: The value of Qc for the conventional D-latch [27], DICE [40], FERST [42], ST [27], TMR [41], LOCDNUTRL [57], LCDNUT [39], RH-2 [64], DNUSH [56], TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and the proposed TNURH are found to be 7.21 fC, 21.23 fC, 18.6 fC, 16.63 fC, 19.61 fC, 26.33 fC, 26.79 fC, 9.14 fC, 28.45 fC, 37.13 fC, 18.48 fC, 28.64 fC, 8.31 fC, 25.89 fC, 36.95 fC, 28.17 fC, 25.87 fC, and 37.6 fC, respectively,

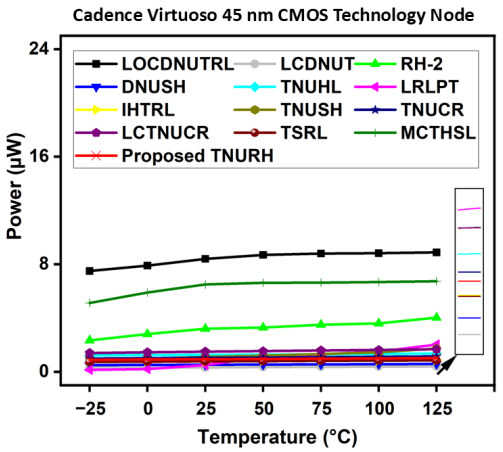


FIGURE 3.8: Effect of temperature variation on the power of proposed TNURH and considered latches.

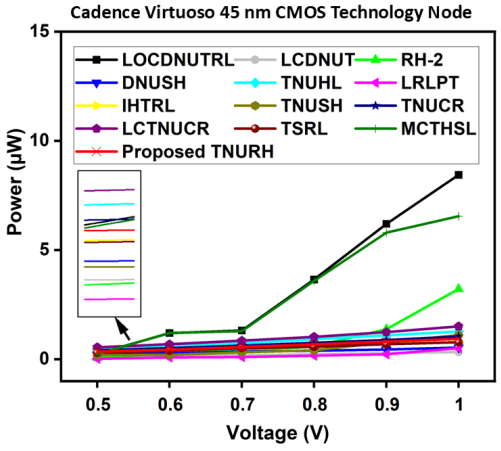


FIGURE 3.9: Effect of supply voltage variation on the power of proposed TNURH and considered latches.

and the same is presented in Table 3.1. The results show that the proposed TNURH latch achieves the highest Qc compared to reported latches.

Area: The value of area for the conventional D-latch [27], DICE [40], FERST [42], ST [27], TMR [41], LOCDNUTRL [57], LCDNUT [39], RH-2 [64], DNUSH [56], TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and the proposed TNURH are found to be 56.5 μm^2, 101.7 μm^2, 135.6 μm^2, 79.1 μm^2, 203.4 μm^2, 248.6 μm^2, 237.3 μm^2, 243.1 μm^2, 339.0 μm^2, 474.6 μm^2,

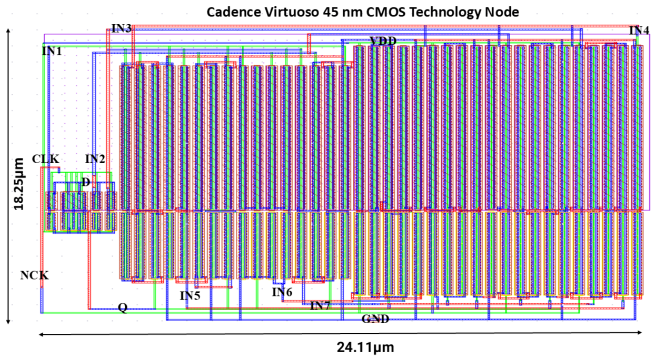


FIGURE 3.10: Layout for proposed TNURH latch.

452.0 μm^2, 460.1 μm^2, 553.7 μm^2, 406.8 μm^2, 689.3 μm^2, 452.4 μm^2, 459.3 μm^2, and 440.01 μm^2, respectively, and the same is presented in Table 3.1. The results show that the proposed TNURH latch occupies second lowest area compared to the TNU latches, such as TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88] and MCTHSL [78]. The proposed TNURH latch layout is shown in Figure 3.10. As reported in the literature [**?**]-[**?**], charge-sharing-induced double-node upsets (DNUs) can be effectively mitigated by increasing the physical separation between sensitive nodes and avoiding closely coupled or shared diffusion regions. For the 130-nm [**?**], 65-nm [98], [**?**] and 32-nm [**?**], technologies, the reported minimum sensitive-node separations are 2 µm, 2.11 µm, and 260 nm, respectively. In the proposed TNURH latch design, the minimum separation between sensitive nodes is 4.62 µm, which is greater than the corresponding values reported in [**?**]-[**?**]. Therefore, the proposed layout provides enhanced physical isolation between sensitive nodes, thereby significantly reducing the likelihood of charge sharing and the resulting double-node or triple-node upset.

PDP: The value of PDP for the conventional D-latch [27], DICE [40], FERST [42], ST [27], TMR [41], LOCDNUTRL [57], LCDNUT [39], RH-2 [64], DNUSH [56], TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and the proposed TNURH are found to be 0.02 fJ, 0.09 fJ, 0.10 fJ, 0.20 fJ, 220.51 fJ, 6.25 fJ, 0.09 fJ, 0.90 fJ, 0.25 fJ, 1.61 fJ, 0.89 fJ, 0.34 fJ, 0.63 fJ, 0.86

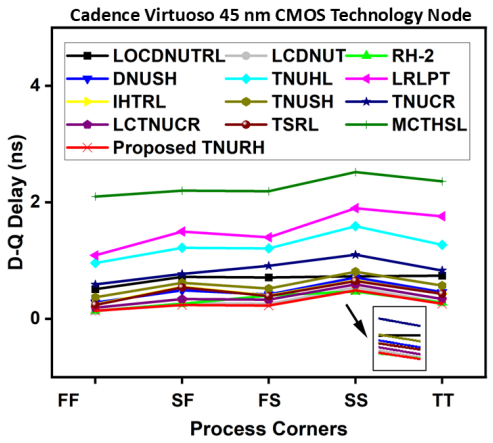


FIGURE 3.11: D-Q delay of proposed TNURH and considered latches at different process corners.

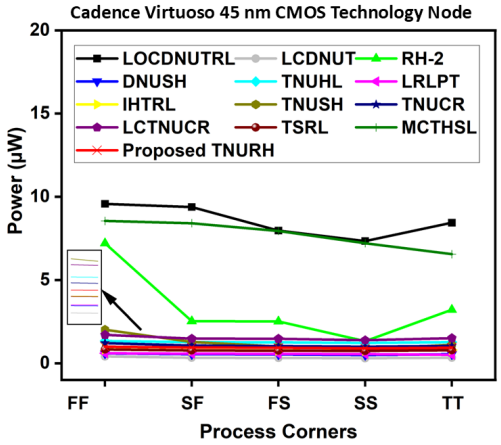


FIGURE 3.12: Power of proposed TNURH and considered latches at different process corners.

fJ, 0.51 fJ, 0.34 fJ, 15.45 fJ, and 0.24 fJ, respectively, and the same is presented in Table 3.1. The results show that the proposed TNURH latch achieves lower PDP compared to the TNU latches, such as TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88] and MCTHSL [78].

QPAR: The value of QPAR for the conventional D-latch [27], DICE [40], FERST [42], ST [27], TMR [41], LOCDNUTRL [57], LCDNUT [39], RH-2 [64], DNUSH [56], TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81],

TABLE 3.1: Comparison of proposed TNURH and considered latches using 45 nm CMOS technology node

Latches	Q_c **(fC)**	**Power** (μ**W**)	**D-Q Delay (ns)**	**PDP (fJ)**	**Area** (μ**m**^{2})	**QPAR** ($\times 10^6$ **m**^{2}**/V**)
D-latch [27]	7.21	0.04	0.47	0.02	56.5	6.8
DICE [40]	21.23	0.18	0.49	0.09	101.7	2.37
FERST [42]	18.6	0.12	0.85	0.10	135.6	1.34
ST [27]	16.63	0.20	1.07	0.20	79.1	0.98
TMR [41]	19.61	154.2	1.43	220.51	203.4	0.001
LOCDNUTRL [57]	26.33	8.44	0.74	6.25	248.6	0.02
LCDNUT [39]	26.79	0.33	0.28	0.09	237.3	1.22
RH-2 [64]	9.14	3.22	0.28	0.90	243.1	0.04
DNUSH [56]	28.45	0.54	0.46	0.25	339.0	0.34
TNUHL [69]	37.13	1.27	1.27	1.61	474.6	0.05
LRLPT [76]	18.48	0.51	1.76	0.89	452.0	0.05
IHTRL [75]	28.64	0.79	0.43	0.34	460.1	0.18
TNUSH [91]	8.31	1.11	0.57	0.63	553.7	0.02
TNUCR [81]	25.89	1.04	0.83	0.86	406.8	0.07
LCTNUCR [81]	36.95	1.51	0.34	0.51	689.3	0.10
TSRL [88]	28.17	**0.78**	0.43	0.34	452.4	0.19
MCTHSL [78]	25.87	6.55	2.36	15.45	459.3	0.003
Proposed TNURH	**37.6**	0.94	**0.26**	**0.24**	**440.01**	**0.35**

TSRL [88], MCTHSL [78], and the proposed TNURH are found to be 6.8 $\times 10^6$ m^2/V, 2.37 $\times 10^6$ m^2/V, 1.34 $\times 10^6$ m^2/V, 0.98 $\times 10^6$ m^2/V, 0.001 $\times 10^6$ m^2/V, 0.02 $\times 10^6$ m^2/V, 1.22 $\times 10^6$ m^2/V, 0.04 $\times 10^6$ m^2/V, 0.34 $\times 10^6$ m^2/V, 0.05 $\times 10^6$ m^2/V, 0.05 $\times 10^6$ m^2/V, 0.18 $\times 10^6$ m^2/V, 0.02 $\times 10^6$ m^2/V, 0.07 $\times 10^6$ m^2/V, 0.10 $\times 10^6$ m^2/V, 0.19 $\times 10^6$ m^2/V, 0.003 $\times 10^6$ m^2/V, and 0.35 $\times 10^6$ m^2/V, respectively, and the same is presented in Table 3.1. The results show that the proposed TNURH latch achieves the highest QPAR compared to the TNU latches, such as TNUHL [69], LRLPT [76], IHTRL [75], TNUSH [91], TNUCR [81], LCTNUCR [81], TSRL [88] and MCTHSL [78].

Variability Analysis: The impact of various process corners for D-Q delay of all reported and proposed latches is shown in Figure 3.11. Similarly, the impact of various process corners on the power of all reported and proposed latches is shown in Figure 3.12. It may be noted that the D-Q delay is lowest for all latches at FF corner, and higher value is

TABLE 3.2: Mean and standard deviation in D-Q delay of proposed TNURH and considered latches.

Latch	Mean (ns)	Standard Deviation (ps)
D latch [27]	0.47	19.58
DICE [40]	0.49	77.30
FERST [42]	0.85	23.12
ST [27]	1.08	23.74
TMR [41]	1.40	101.50
LOCDNUTRL [57]	0.74	21.96
LCDNUT [39]	0.28	21.27
RH-2 [64]	0.28	79.01
DNUSH [56]	0.46	34.32
TNUHL [69]	1.27	36.68
LRLPT [76]	1.73	317.25
IHTRL [75]	0.43	30.21
TNUSH [91]	0.57	38.34
TNUCR [81]	0.84	49.86
LCTNUCR [81]	0.34	20.67
TSRL [88]	0.43	30.99
MCTHSL [78]	2.37	69.15
Proposed TNURH	**0.26**	**18.82**

observed at SS corner. The power shows the reverse trend i.e. power is lowest at SS corner and highest at FF corner for all latches. Tables 3.2 and 3.3 summarise the mean (μ) and standard deviation (σ) for D-Q delay and power, respectively. Simulation results show that, in comparison to reported TNU latches, the proposed latch is less sensitive to PVT variation for D-Q delay and power. The standard deviation (σ) in D-Q delay and power for proposed TNURH latch remains within 7.2% and 1.06% of corresponding mean value.

3.5 Summary

In this chapter, a novel highly reliable energy efficient radiation hardened latch is presented. The proposed latch provides SE tolerance by using four transmission gates, four

TABLE 3.3: Mean and standard deviation in power of proposed TNURH and considered latches.

Latch	Mean (μW)	Standard Deviation (ns)
D-Latch [27]	0.04	0.85
DICE [40]	0.18	4.09
FERST [42]	0.12	1.71
ST [27]	0.20	12.59
TMR [41]	154.1	9.32
LOCDNUTRL [57]	8.52	484.34
LCDNUT [39]	0.35	358.2
RH-2 [64]	3.33	673.6
DNUSH [56]	0.53	5.92
TNUHL [69]	1.27	11.59
LRLPT [76]	0.51	22.27
IHTRL [75]	0.78	11.13
TNUSH [91]	1.16	99.98
TNUCR [81]	1.04	21.94
LCTNUCR [81]	1.51	19.68
TSRL [88]	0.78	12.21
MCTHSL [78]	6.6	380.83
Proposed TNURH	**0.94**	**10.06**

4MCEs, and four CG-4MCEs. The proposed latch can recover from any node upsets, such as SNUs, DNUs, and TNUs. The proposed latch effectively, maintain its SE tolerance in the presence of PVT variations. The proposed TNU hardened latch improves the performance in terms of Qc, power, D-Q delay, PDP, area, and QPAR up to 45.35%, 37.75%, 23.53%, 52.94%, 36.17%, and 250% than the recently reported latch MCTHSL [78] at voltage supply = 1V in 45nm CMOS technology. From Monte-Carlo Simulation, we validate the proposed latch works properly under harsh conditions. The proposed latch shows 48.31% and 8.08% lower standard deviation for D-Q delay and power, respectively, compared to recently reported latch MCTHSL [78]. The simulation results support the robustness of the proposed latch against SNU, DNU, and TNU upsets. Therefore, for low power and space applications the proposed radiation hardened latches would be a better choice.

Chapter 4

Hybrid Schmitt Trigger And Muller C-Element Based TNU Hardened Latch

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The results described in this chapter have been published as the following peer-reviewed publication:

* N. Kumar, C. I. Kumar, and N. Pandey, **"High-Performance Cascode Schmitt-Trigger and C-Element based Triple Node Upset Radiation Hardened Latch,"** Microelectronics Reliability, vol. 182, p. 116174, 2026.

4.1 Introduction

The design presented in the previous chapters effectively handles the fault tolerance against triple-node upset (TNU), but at the cost of power, delay, and area overhead. To overcome these limitations, there is a strong need for cost effective latch design, that can tolerate TNU. This chapter presents a hybrid architecture of a radiation hardened latch which incorporates a Schmitt Trigger and muller c-element (MCE) based radiation hardened latch design aimed at improved fault tolerance capability against TNU. The working principle and implementation are presented in Section 4.2. Soft error robustness of the proposed TNU hardened latch is presented in Section 4.3. Performance evaluation is presented in Section 4.4, and Section 4.5 summarizes the findings.

4.2 Proposed design 4

The schematic of the proposed cascode Schmitt Trigger and C-element-based triple-node-upset radiation-hardened (CSTCE-TNURH) latch is shown in Figure 4.1. The CSTCE-TNURH latch is composed of four transmission gates (T1, T2, T3, and T4), three cascode Schmitt triggers (CST1, CST2, CST3), and a clock-gated 3-input Muller C-element (CG-3MCE). The proposed CSTCE-TNURH latch works as follows: when CLK = 1 and NCK = 0, all transmission gates (T1, T2, T3, and T4) are switched on, and the latch works in the transparent mode. In this case, data transmits from the input D to the output Q through T4, while all CGIs and the CG-3MCE remain off to minimize power and D-Q delay. In hold mode (CLK = 0 and NCK = 1), all transmission gates are turned off, and the CGIs

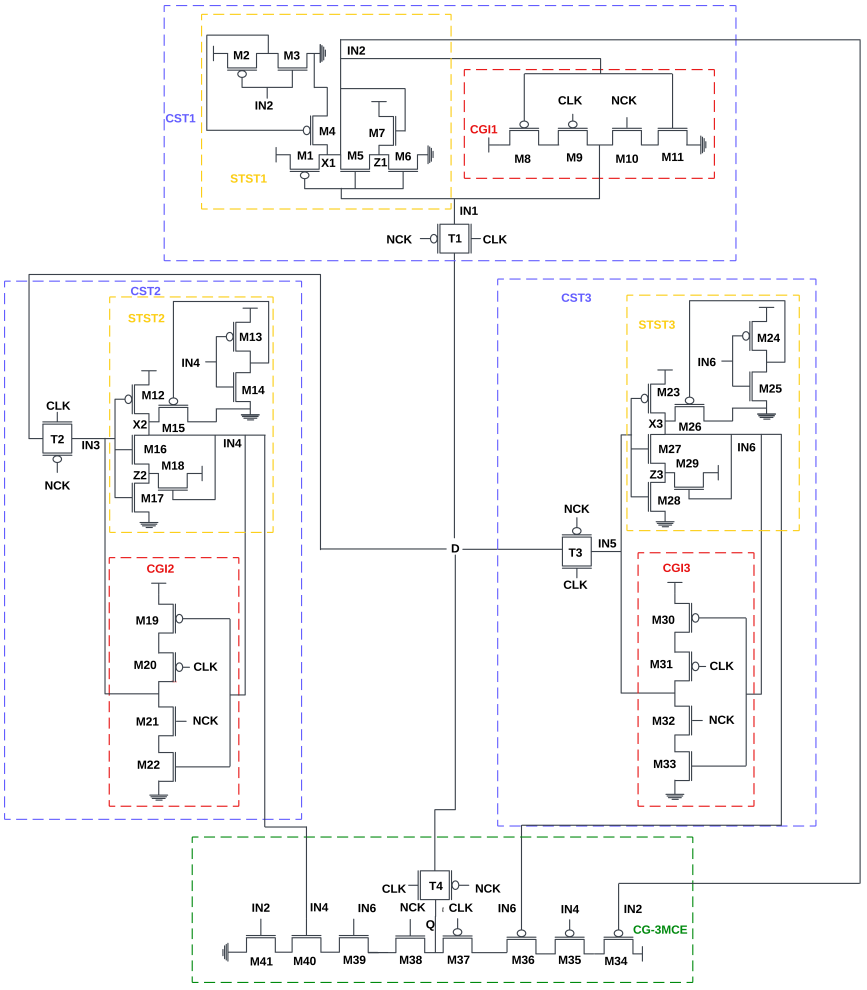

FIGURE 4.1: Schematic of proposed CSTCE-TNURH latch.

along with the CG-3MCE are activated, ensuring that the CG-3MCE output retains the latch's state.

The simulation waveforms of the proposed CSTCE-TNURH latch under error-free conditions are shown in Figure 4.2. In transparent mode (CLK = 1, NCK = 0, D = 1), all transmission gates (T1, T2, T3, and T4) are turned on, allowing data to propagate from the input D to the output Q through T4. In this case, the logic value at the internal nodes are IN1 = 1, IN3 = 1, and IN5 = 1. These values pass through CST1, CST2, and CST3, respectively, resulting in IN2 = 0, IN4 = 0, and IN6 = 0. Since CLK = 1, the CG-3MCE remains disabled and the correct logic is stored at node Q. In hold mode (CLK = 0, NCK

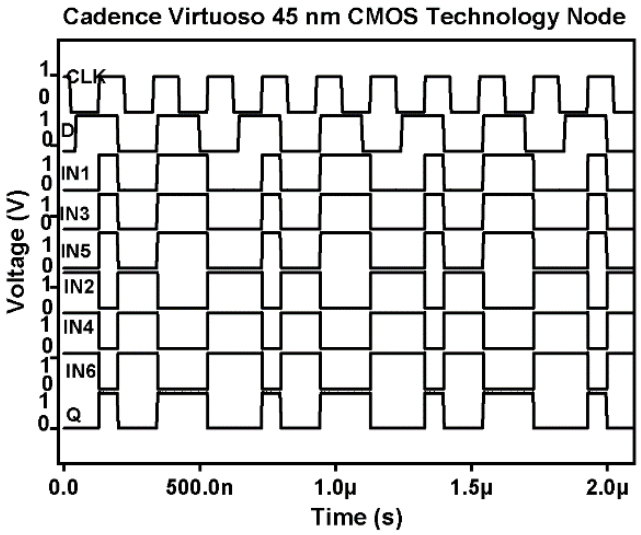

FIGURE 4.2: Simulation results of the CSTCE-TNURH latch design in Fault-free scenario.

= 1, D = 1), all transmission gates are turned off, while the CGIs and CG-3MCE are activated. The CG-3MCE output maintains the latch state, keeping output node Q at logic 1.

4.3 Fault tolerance and recovery analysis (SNU / DNU / TNU)

In this section, the proposed CSTCE-TNURH latch tolerance and recovery analysis against SNU, DNU, and TNU is analyzed individually for each case. Additionally, we abstract the schematic by using internal nodes of the proposed CSTCE-TNURH latch to analyze the tolerance and recovery, as shown in Figure 4.1. First, consider the transparent mode with CLK = 1, NCK = 0, and D = 1. In this case, all transmission gates (T1, T2, T3, and T4) pass data to their respective subsequent stages, resulting in internal node values of IN1 = 1, IN2 = 0, IN3 = 1, IN4 = 0, IN5 = 1, IN6 = 0, and output Q = 1. Next, we analyze the circuit's radiation-hardening behavior in hold mode (CLK = 0, NCK = 1).

4.3.1 SNU fault tolerance and recovery analysis

In this case, seven possible scenarios exist, which are divided into two cases. Case S1: TF occurs inside CSTs, and Case S2: TF occurs inside CG-3MCE.

Case S1: In this case, we have considered that one TF occurs at the input of any CSTs (here we consider CST1). Let us assume positive pulse strikes the internal node IN1. If IN1 is initially at logic 0 and IN2 at logic 1, transistor M7 charges node Z1 to logic 1. A positive pulse at IN1 forces it to logic 1, turning on M5 and M6. The stored charge at Z1 must be discharged before IN2 can change state. Since IN2 remains at logic 1, it forces IN1 back to its previous logic value by CGI1. For a negative pulse at IN1, if IN1 is initially at logic 1 and IN2 at logic 0, transistor M2 is on. A negative pulse causes IN1 drop to logic 0, and transistor M1 charges node X1 to logic 1. The stored charge at X1 must be discharged through M4, as M3 is on, hence IN2 remains at logic 0. However, IN2 is still at logic 0, restoring IN1 to its original state by CGI1. CST2 and CST3 work similarly to recover IN3 and IN5. For a TF on IN2, if IN1 is at logic 1 and IN2 at logic 0, a positive pulse changes IN2 to logic 1, activating M3 and M4, which discharge node X1 and restore SN2 to logic 0. For a negative pulse, if IN1 is at logic 0 and IN2 at logic 1, the pulse forces IN2 to logic 0, but with IN1 at logic 1, M1 charges node X1, restoring IN2 to logic 1. CST2 and CST3 similarly restore IN4 and IN6. However, due to CST1 fault-tolerant and recovery capabilities, its output remains unaffected, and the correct logic value is restored at IN1. The same SNU fault tolerance and recovery behavior is observed when TF occurs at other internal nodes, such as IN3 or IN5.

Case S2: In this case, we have considered that one TF occurs at the input of CG-3MCE. If a TF strikes IN4, its logic value changes from 0 to 1. At this point, the internal nodes of CG-3MCE are IN2 = 0, IN4 = 1, and IN6 = 0. Although the altered value of IN4 reaches the input of CG-3MCE, the outputs of both CG-3MCE and CST2 remain unaffected due

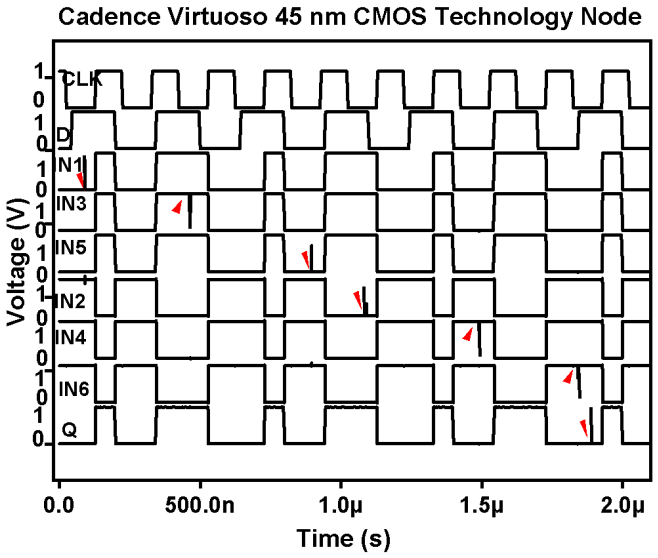

FIGURE 4.3: Simulation results of SNU injection cases for the proposed CSTCE-TNURH latch design.

to their fault-tolerant and recovery features described earlier. Furthermore, if a TF was injected at the output node Q. In this case, output Q is restored by inputs (SN2, SN4, SN6) of a CG-3MCE, which is uncorrupted due to CSTs. Therefore, output node Q will retain its original state. Similar fault tolerance is seen when TF affects other internal nodes like IN2 or IN6. As shown in Figure 4.3, all internal nodes in the proposed CSTCE-TNURH latch are capable of tolerating and recovering from faults, demonstrating complete immunity to SNU events.

4.3.2 DNU fault tolerance and recovery analysis

In this case, twenty-one possible scenarios exist, which are divided into three cases. Case D1: two TFs occur inside CSTs, Case D2: two TFs occur inside CG-3MCE and Case D3: one TF occurs inside CSTs and one TF occurs inside CG-3MCE.

Case D1: In this case, we have considered that two TFs occur at the input of any CSTs (here we consider CST1). If TFs occur at both IN1 and IN3, their logic values change

from 1 to 0. Due to the fault-tolerant and recovery capabilities of CST1 and CST2, as previously described, their outputs remain unaffected, and the correct logic levels are restored at IN1 and IN3. Similar DNU fault tolerance and recovery behavior is observed when TFs occur at other node pairs, such as (IN1, IN5) and (IN3, IN5).

Case D2: In this case, we have considered that two TFs occur at the input of CG-3MCE. If TFs affect IN2 and IN4, both change from logic 0 to logic 1. At this point, the internal nodes of CG-3MCE are IN2 = 1, IN4 = 1, and IN6 = 0. Although the altered values reach CG-3MCE inputs, the outputs of CG-3MCE, CST1, and CST2 remain unchanged due to their fault-tolerance and recovery mechanisms described earlier. As a result, IN2 and IN4 are restored to their correct logic values. Similar fault tolerance is seen for other node pairs such as (IN2, IN6) and (IN4, IN6).

Case D3:: In this case, we have considered that one TF occurs at the input of any CSTs (here we consider CST1) and one TF occurs at the input of CG-4MCE. If a TF occurs at both IN5 and IN6, IN5 flips from logic 1 to 0, and IN6 flips from logic 0 to 1. These incorrect values are applied to the inputs of CST3 and CG-3MCE, but due to their inherent fault-tolerant and recovery features described earlier, their outputs remain unaffected, restoring IN5 and IN6 to their correct values. Furthermore, if a TF is injected at the internal node SN2 and the output node Q. In this case, the internal node IN2 is restored by CST1, and the output Q is restored by inputs (IN2, IN4, IN6) of a CG-3MCE, which is uncorrupted due to CSTs. Therefore, IN2 and Q will retain their original state. Similar recovery behavior occurs for other node pairs, including (IN1, IN2), (IN1, IN4), (IN1, IN6), (IN3, IN2), (IN3, IN4), (IN3, IN6), (IN5, IN2), (IN5, IN4), (IN1, Q), (IN3, Q), (IN4, Q), (IN5, Q), and (IN6, Q). As shown in Figure 4.4, all internal nodes of the proposed CSTCE-TNURH latch exhibit tolerance and recovery from DNU events, confirming its complete immunity against DNU.

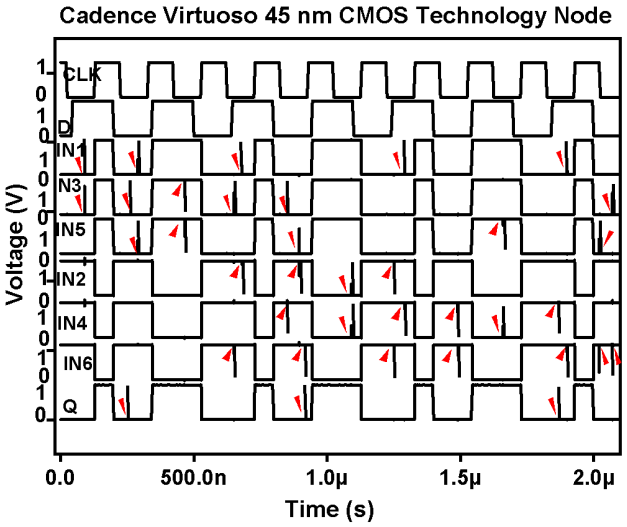

FIGURE 4.4: Simulation results of DNU injection cases for the proposed CSTCE-TNURH latch design.

4.3.3 TNU fault tolerance and recovery analysis

In this case, thirty-five possible scenarios exist, which are divided into four cases. Case T1: three TFs occur inside CSTs, Case T2: three TFs occur inside CG-3MCE and Case T3: two TFs occur inside CSTs and one TF occurs inside CG-3MCE. Case T4: one TF occurs inside CSTs and two TFs occur inside CG-3MCE.

Case T1: In this case, we have considered that three TF occurs at the input of any CSTs (here we consider CST1). If TFs occur simultaneously at IN1, IN3, and IN5, each will change from logic 1 to logic 0. These incorrect values are then propagated to the inputs of CST1, CST2, and CST3. However, the outputs of (CST1, CST2, and CST3) remain unaffected due to their fault-tolerant and recovery features described earlier and the correct logic states are restored at IN1, IN3, and IN5.

Case T2: In this case, we have considered that three TFs occur at the input of CG-3MCE. If a TF strikes all three nodes, their values flip from logic 0 to logic 1, making IN2 = 1, IN4 = 1, and IN6 = 1. These incorrect values are propagate to the inputs of CG-3MCE.

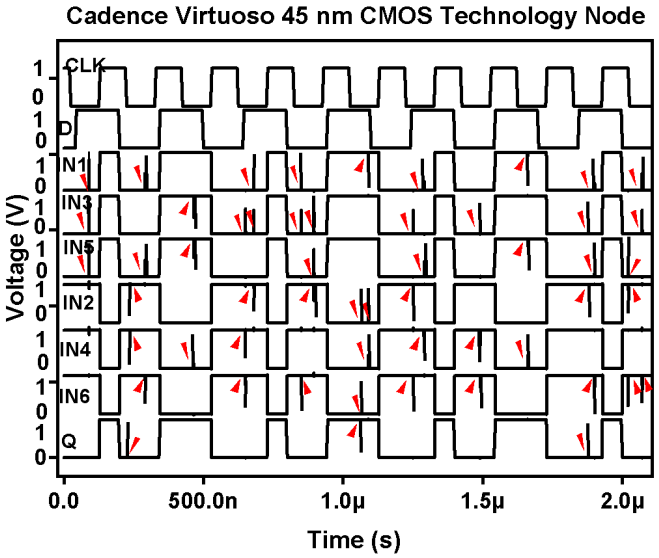

FIGURE 4.5: Simulation results of TNU injection cases for the proposed CSTCE-TNURH latch design.

However, the outputs of (CG-3MCE, CST1, CST2, and CST3) remain unaffected due to their fault-tolerant and recovery features described earlier and the original logic values are restored at IN2, IN4, and IN6.

Case T3: In this case, we have considered that two TFs occur at the input of any CSTs (here we consider CST1) and one TF occurs at the input of CG-3MCE . If TFs hit IN1, IN3, and IN2, then IN1 and IN3 change from logic 1 to logic 0, while IN2 changes from logic 0 to logic 1. These incorrect values propagate to CST1, CST2, and CG-3MCE. Despite this, the outputs of all three blocks remain unchanged due to their fault tolerance and recovery characteristics described earlier, restoring the correct logic levels at IN1, IN3, and IN2. The same TNU analysis applies if TFs occur at other node triplets such as (IN1, IN3, IN4), (IN1, IN3, IN6), (IN1, IN5, IN2), (IN1, IN5, IN4), (IN1, IN5, IN6), (IN3, IN5, IN2), (IN3, IN5, IN4), and (IN3, IN5, IN6).

Case T4: In this case, we have considered that one TF occurs at the input of any CSTs (here we consider CST1) and two TFs occur at the input of CG-3MCE. If TFs strike these nodes, IN1 flips from logic 1 to logic 0, while IN2 and IN4 flip from logic 0 to logic 1.

The incorrect values are delivered to the inputs of CST1 and CG-3MCE. Yet, the outputs of CST1, CST2, CST3, and CG-3MCE remain unaffected due to their fault tolerance and recovery features described earlier, restoring the correct logic at IN1, IN2, and IN4. Furthermore, if a TF is injected at the internal nodes (IN2, IN4) and the output node Q. In this case, the internal nodes IN2 and IN4 are restored by CST1 and CST2, respectively, and the output Q is restored by inputs (IN2, IN4, IN6) of a CG-3MCE, which remains uncorrupted due to CSTs. Therefore, IN2, IN4, and Q will retain their original state. Similar TNU analysis holds for other node triplets, including (IN1, IN2, IN6), (IN1, IN4, IN6), (IN3, IN2, IN4), (IN3, IN2, IN6), (IN3, IN4, IN6), (IN5, IN2, IN4), (IN5, IN2, IN6), (IN5, IN4, IN6), (IN1, IN2, Q), (IN1, IN3, Q), (IN1, IN4, Q), (IN1, IN5, Q), (IN1, IN6, Q), (IN2, IN3, Q), (IN2, IN5, Q), (IN2, IN6, Q), (IN3, IN4, Q), (IN3, IN5, Q), (IN3, IN6, Q), (IN4, IN5, Q), (IN4, IN6, Q), and (IN5, IN6, Q). As shown in Figure 4.5, all sensitive nodes can be tolerant and recover. This confirms that the proposed CSTCE-TNURH latch is completely recovered from TNU.

4.4 Performance evaluation

The simulation setup, operating conditions, and evaluation methodology are discussed in Section 2.3, adopted for the proposed Design 4.

D-Q Delay: The value of D-Q delay for the conventional D-latch [27], DICE [40], TMR [41], RH-2 [64], LOCDNUTRL [57], IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], TNURH (design 3) and the proposed CSTCE-TNURH are found to be 0.47 ns, 0.49 ns, 1.43 ns, 0.28 ns, 0.74 ns, 0.43 ns, 0.57 ns, 1.27 ns, 0.83 ns, 0.34 ns, 0.43 ns, 2.36 ns, 0.26 and 0.17 ns, respectively, and the same is presented in Table 4.1. The results show that the proposed CSTCE-TNURH latch achieves the minimum D-Q delay compared to the reported latches. Moreover, the

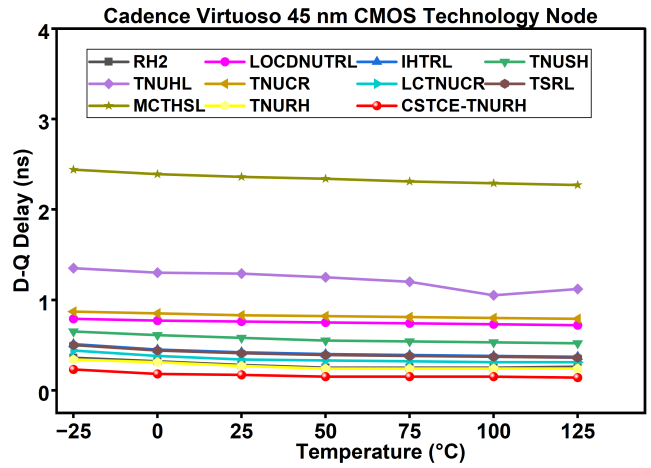

FIGURE 4.6: Temperature variation effect on the D-Q delay of proposed CSTCE-TNURH and considered latches.

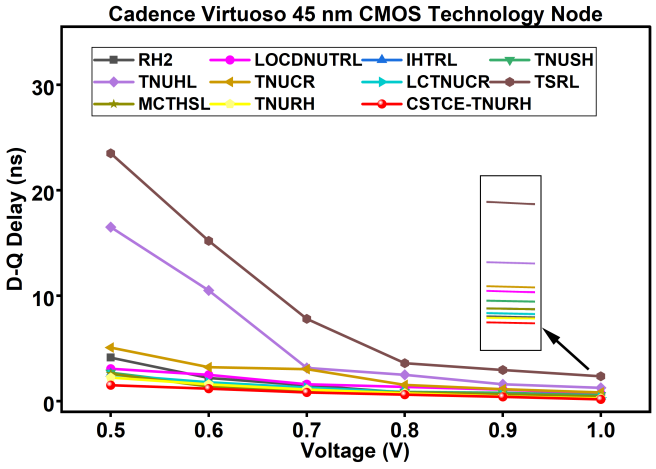

FIGURE 4.7: Voltage variation effect on the D-Q delay of proposed CSTCE-TNURH and considered latches.

effects of variations in temperature and supply voltage are also simulated, and the results are shown in Figures 4.6 and 4.7, respectively. It can be observed that the proposed designs shows better results in the entire voltage and temperature range as compared to the reported latches.

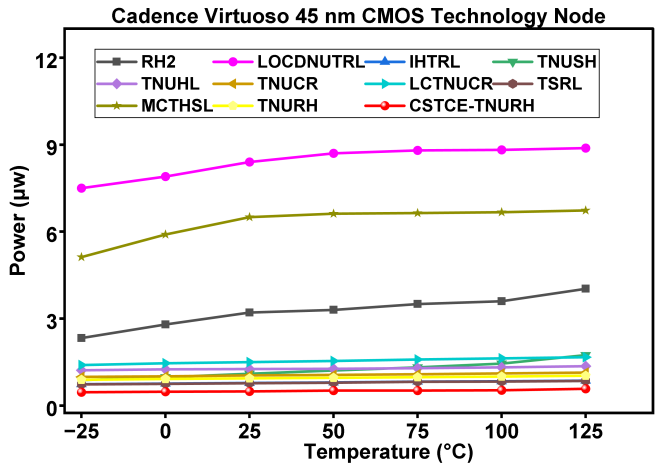

FIGURE 4.8: Temperature variation effect on the power of proposed CSTCE-TNURH and considered latches.

Power: The value of power for the conventional D-latch [27], DICE [40], TMR [41], RH-2 [64], LOCDNUTRL [57], IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], TNURH (design 3) and the proposed CSTCE-TNURH are found to be 0.04 μW, 0.18 μW, 154.2 μW, 3.22 μW, 8.44 μW, 0.79 μW, 1.11 μW, 1.27 μW, 1.04 μW, 1.51 μW, 0.78 μW, 6.55 μW, 0.94 μW, and 0.51 μW, respectively, and the same is presented in Table 4.1. The results show that the proposed CSTCE-TNURH latch consumes lower power compared to the TNU latches, such as IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and TNURH (design 3). Moreover, the effects of variations in temperature and supply voltage are also simulated, and the results are shown in Figures 4.8 and 4.9, respectively. It can be observed that the proposed design shows better results in the entire voltage and temperature range as compared to the reported latches.

Critical Charge: The value of Qc for the conventional D-latch [27], DICE [40], TMR [41], RH-2 [64], LOCDNUTRL [57], IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], TNURH (design 3) and the proposed CSTCE-TNURH are found to be 7.21 fC, 21.23 fC, 19.61 fC, 9.14 fC, 26.33 fC, 28.64 fC, 8.31 fC, 37.13 fC, 25.89 fC, 36.95 fC, 28.17 fC, 25.87 fC, 37.6 fC and 39.2 fC,

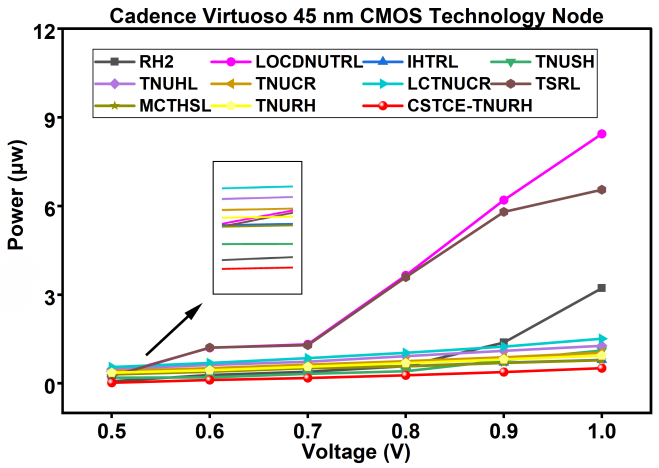

FIGURE 4.9: Voltage variation effect on the power of proposed CSTCE-TNURH and considered latches.

respectively, and the same is presented in Table 4.1. The results show that the proposed CSTCE-TNURH latch achieves the highest Qc compared to reported latches.

Area: The value of area for the conventional D-latch [27], DICE [40], TMR [41], RH-2 [64], LOCDNUTRL [57], IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], TNURH (design 3) and the proposed CSTCE-TNURH are found to be 56.5 μm^2, 101.7 μm^2, 203.4 μm^2, 243.1 μm^2, 248.6 μm^2, 460.1 μm^2, 553.7 μm^2, 474.6 μm^2, 406.8 μm^2, 689.3 μm^2, 452.4 μm^2, 459.3 μm^2, 440.01 μm^2, and 258.73 μm^2, respectively, and the same is presented in Table 4.1. The results show that the proposed CSTCE-TNURH latch occupies smaller area compared to the TNU latches, such as IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and TNURH (design 3). The proposed CSTCE-TNURH latch layout is shown in Figure 4.10. In the proposed CSTCE-TNURH latch design, the minimum separation between sensitive nodes is 5.87 µm, which is greater than the corresponding values reported in [**?**]-[**?**].

PDP: The value of PDP for the conventional D-latch [27], DICE [40], TMR [41], RH-2

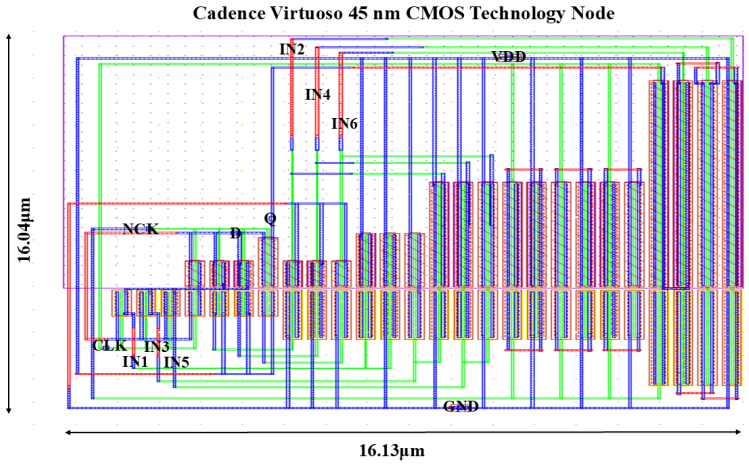

FIGURE 4.10: Layout for proposed CSTCE- TNURH latch.

[64], LOCDNUTRL [57], IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], TNURH (Design-3), and the proposed CSTCE-TNURH are found to be 0.02 fJ, 0.09 fJ, 220.51 fJ, 0.90 fJ, 6.25 fJ, 0.34 fJ, 0.63 fJ, 1.61 fJ, 0.86 fJ, 0.51 fJ, 0.34 fJ, 15.45 fJ, 0.24 fJ, and 0.09 fJ, respectively, as presented in Table 4.1. The results show that the proposed CSTCE-TNURH latch achieves lower PDP compared to the TNU latches, such as IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and TNURH (design 3).

QPAR: The value of QPAR for the conventional D-latch [27], DICE [40], TMR [41], RH-2 [64], LOCDNUTRL [57], IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], TNURH (Design-3), and the proposed CSTCE-TNURH are found to be 6.8 $\times 10^6$ m^2/V, 2.37 $\times 10^6$ m^2/V, 0.001 $\times 10^6$ m^2/V, 0.04 $\times 10^6$ m^2/V, 0.02 $\times 10^6$ m^2/V, 0.18 $\times 10^6$ m^2/V, 0.02 $\times 10^6$ m^2/V, 0.05 $\times 10^6$ m^2/V, 0.07 $\times 10^6$ m^2/V, 0.10 $\times 10^6$ m^2/V, 0.19 $\times 10^6$ m^2/V, 0.003 $\times 10^6$ m^2/V, 0.35 $\times 10^6$ m^2/V, and 1.68 $\times 10^6$ m^2/V, respectively, and the same is presented in Table 4.1. The results show that the proposed CSTCE-TNURH latch achieves the highest QPAR compared to the TNU latches, such as IHTRL [75], TNUSH [91], TNUHL [69], TNUCR [81], LCTNUCR [81], TSRL [88], MCTHSL [78], and TNURH (design 3).

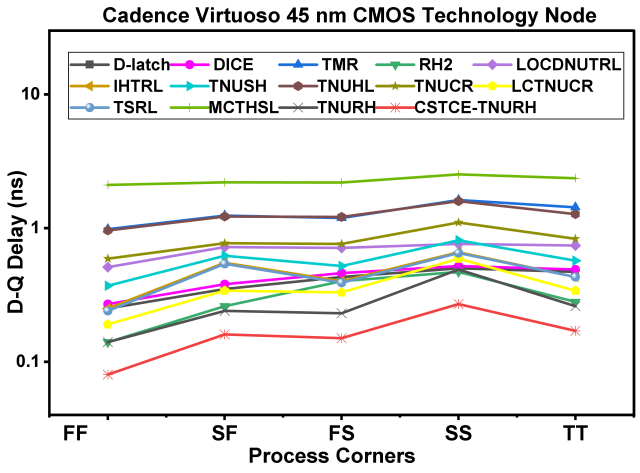

FIGURE 4.11: D-Q delay for proposed CSTCE-TNURH and considered latches with different process corner variations.

Variability Analysis: The impact of various process corners for D-Q delay of all reported and proposed latches is shown in Figure 4.11. Similarly, the impact of various process corners on the power of all reported and proposed latches is shown in Figure 4.12. It may be noted that the D-Q delay is lowest for all latches at FF corner, and higher value is observed at SS corner. The power shows the reverse trend i.e. power is lowest at SS corner and highest at FF corner for all latches. Tables 4.2 and 4.3 summarise the mean (μ) and standard deviation (σ) for D-Q delay and power, respectively. Simulation results show that, in comparison to TNU reported latches, the proposed latch is less sensitive to PVT variation for D-Q delay and power. The standard deviation (σ) in D-Q delay and power for proposed CSTCE-TNURH latch remains within 6.48% and 2.08% of corresponding mean value.

4.5 Summary

In this chapter, a novel highly reliable energy efficient radiation hardened latch is presented. The proposed latch provide the SE tolerance by using four TGs, three CSTs, and

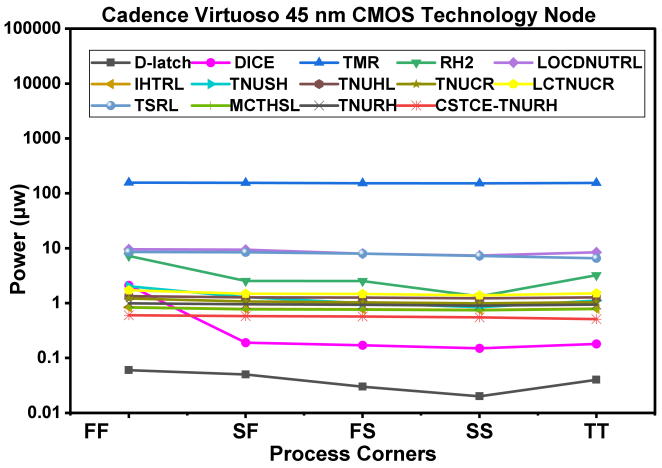

FIGURE 4.12: Power for proposed CSTCE-TNURH and considered latches with different process corner variations.

TABLE 4.1: Comparison of proposed CSTCE-TNURH and considered latches using 45 nm CMOS technology node

Latches	Q_c **(fC)**	**Power** (μ**W**)	**D-Q Delay (ns)**	**PDP (fJ)**	**Area** (μ**m**^{2})	**QPAR** ($\times 10^6$ **m**^{2}**/V**)
D-latch [27]	7.21	0.04	0.47	0.02	56.5	6.8
DICE [40]	21.23	0.18	0.49	0.09	101.7	2.37
TMR [41]	19.61	154.2	1.43	220.51	203.4	0.001
RH-2 [64]	9.14	3.22	0.28	0.90	243.1	0.04
LOCDNUTRL [57]	26.33	8.44	0.74	6.25	248.6	0.02
IHTRL [75]	28.64	0.79	0.43	0.34	460.1	0.18
TNUSH [91]	8.31	1.11	0.57	0.63	553.7	0.02
TNUHL [69]	37.13	1.27	1.27	1.61	474.6	0.05
TNUCR [81]	25.89	1.04	0.83	0.86	406.8	0.07
LCTNUCR [81]	36.95	1.51	0.34	0.51	689.3	0.10
TSRL [88]	28.17	0.78	0.43	0.34	452.4	0.19
MCTHSL [78]	25.87	6.55	2.36	15.45	459.3	0.003
TNURH*	37.6	0.94	0.26	0.24	440.01	0.35
Proposed CSTCE-TNURH	**39.2**	**0.51**	**0.17**	**0.09**	**258.73**	**1.68**

* TNURH latch belongs to Proposed Design-3.

CG-3MCEs. The proposed latch can recover from any node upsets, such as SNUs, DNUs, and TNUs. The proposed latch effectively, maintain its SE tolerance in the presence of PVT variations. From simulations, we have shown that the proposed TNU hardened latch improves the performance in terms of Qc, power, D-Q delay, PDP, area, and QPAR up to 51.53%, 92.14%, 92.80%, 99.42%, 43.67%, and 55900% than the recently reported

TABLE 4.2: Mean and standard deviation in D-Q delay of proposed CSTCE-TNURH and considered latches.

Latch	Mean (ns)	Standard Deviation (ps)
D-latch [27]	0.47	19.58
DICE [40]	0.49	77.30
TMR [41]	1.4	101.50
RH-2 [64]	0.28	79.01
LOCDNUTRL [57]	0.74	21.96
IHTRL [75]	0.43	30.21
TNUSH [91]	0.57	37.99
TNUHL [69]	1.27	36.68
TNUCR [81]	0.84	49.86
LCTNUCR [81]	0.34	20.67
TSRL [88]	0.42	30.99
MCTHSL [78]	2.37	69.15
TNURH*	0.26	18.82
CSTCE-TNURH	**0.17**	**11.02**

* TNURH latch belongs to Proposed Design-3.

TABLE 4.3: Mean and standard deviation in power of proposed CSTCE-TNURH and considered latches.

Latch	Mean (μW)	Standard Deviation (ns)
D-latch [27]	0.04	0.85
DICE [40]	0.18	4.06
TMR [41]	154.1	9.32
RH-2 [64]	3.33	673.6
LOCDNUTRL [57]	8.52	484.34
IHTRL [75]	0.78	11.13
TNUSH [91]	1.16	98.95
TNUHL [69]	1.27	11.59
TNUCR [81]	1.04	21.94
LCTNUCR [81]	1.51	19.68
TSRL [88]	0.78	12.21
MCTHSL [78]	6.57	380.83
TNURH*	0.94	10.06
CSTCE-TNURH	**0.51**	**10.64**

* TNURH latch belongs to Proposed Design-3.

latch MCTHSL [78] at voltage supply = 1V in 45nm CMOS technology. From Monte-Carlo Simulation, we validated the proposed latch works properly under harsh conditions. The proposed latch shows 84.06% and 97.21% lower standard deviation for D-Q delay and power, respectively, compared to recently reported latch MCTHSL [78]. The simulation results support the robustness of the proposed latch against SNU, DNU, and TNU upsets. Therefore, for low power and space applications the proposed CSTCE-TNURH latch would be a better choice compared to other reported latches.

Chapter 5

FinFET Based Latch Design

The results described in this chapter have been published as the following peer-reviewed publication:

* N. Kumar, N. Pandey, and C. I. Kumar, **"High Performance Double Node Upset Radiation Hardened Latch in 7 nm FinFET,"** 2025 10th Int. Conf. Commun. Electron. Syst., pp.589–594, 2025, doi: 10.1109/ICCES67310.2025.11337000.

5.1 Introduction

In the previous chapters, radiation-hardened latch designs were proposed in the complementary metal–oxide–semiconductor (CMOS) technology. Previously proposed latch design enhances the reliability at the cost of D-Q delay, power, and area overhead. To address this limitation, this chapter uses FinFET technology over CMOS technology. The FinFET occupies lesser area as compared to the CMOS counterpart. The FinFETs offer higher ON currents compared to metal–oxide–semiconductor field-effect transistors (MOSFETs) of the same size.[93]. The FinFET channel width changed by varying fin height; thus, FinFET is far more denser than the planar MOSFET [92]. The FinFET has a number of important benefits over MOSFETs in the nanoscale range, including as higher transconductance, low power, and increased robustness under process, voltage, temperature (PVT) fluctuations. Additionally, FinFET has a very low temperature effect on threshold voltage, leading to a much higher temperature tolerance than MOSFET. Therefore, FinFET technology is used to get beyond these limitations of MOSFET in the nanoscale level. In this chapter, we proposed a double-node upset (DNU) hardened latch in FinFET technology.

The working principle and implementation are presented in Section 5.2. Soft error robustness of the proposed DNU hardened latch is presented in Section 5.3. Performance evaluation is presented in Section 5.4, and Section 5.5 summarizes the findings.

5.2 Proposed design 5

The schematic of the proposed Muller C-element with a Schmitt Trigger (MCEST) tolerant latch is shown in Figure 5.1. The MCEST latch is composed of three transmission gates (T1, T2, T3), two tolerant circuits (TC1 and TC2) and a clock-gated 2-input Muller C-element (CG-2MCE). The operation of TC1 is as follows: The TC1 design is structured into six blocks: four transistor Schmitt Trigger (FTST1), 2MCE1, transmission gate T1, inverter CGI1 in forward path, and an inverter CGI2 and CGI3 in feedback path. In forward path, the FTST1 block comprising transistors M1, M2, M3, and M4 is employed. The core hardening mechanism in this design involves enhancing the capacitance at the susceptible node by integrating the FTST1. In this configuration, D is the input, Q is the output, CLK is the clock signal, and NCK is its complement. When CLK is at logic 1 or high, latch works in transparent mode; when CLK is at logic 0, it switches to hold mode. During the transparent phase, the data propagates through the FTST1 and CGI1, while CGI2 and CGI3 remain inactive. Once the input data D stabilizes at nodes X3 and X4, it is transferred to the output IN2 through the 2MCE1 composed of transistors M5, M6, M7, and M8. In this mode, SNU occurring at node IN1 passes through FTST1 and CGI1, subsequently appearing at nodes X3 and X4, respectively. Now, let us consider if CLK = 0, the value stored at IN2 is maintained through CGI2 and CGI3. Let us assume node IN1 is at logic 0 and node X3 is at logic 1. In this condition, node X2 is charged, and transistor M4 is turned on. If a TF causes node IN1 to switch to logic 1, transistors M2 and M3 will be turned on, and the charge at node X2 must be discharged before node X3 can change states. Therefore, when a particle strike affects node IN1, the resulting TF is suppressed by the FTST1. Now consider, if an TF occurs at IN2, a transient pulse is generated at node X4 due to CGI3 feedback, while node X3 preserves its previous voltage. As a result, the inputs of the 2MCE1 differ, preventing fault propagation, and the transient pulse

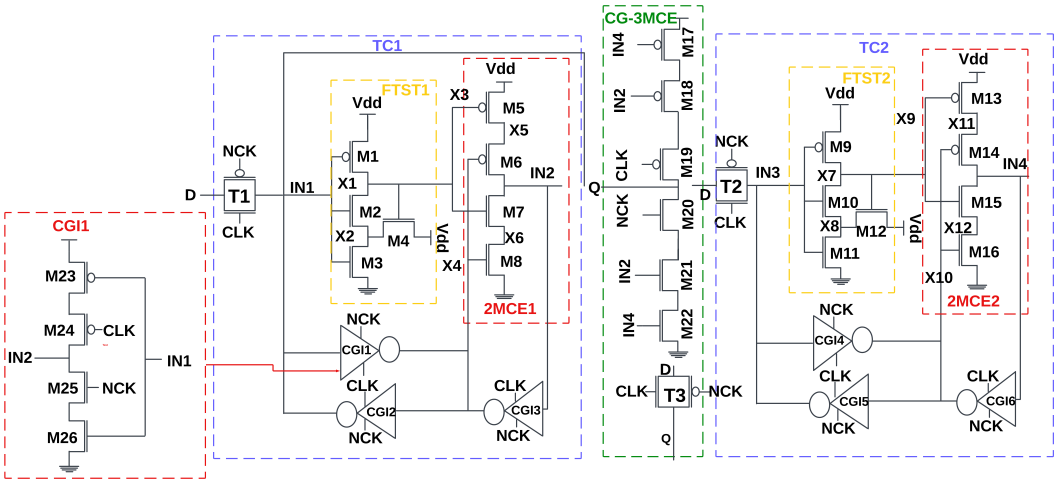

FIGURE 5.1: Schematic of proposed MCEST latch.

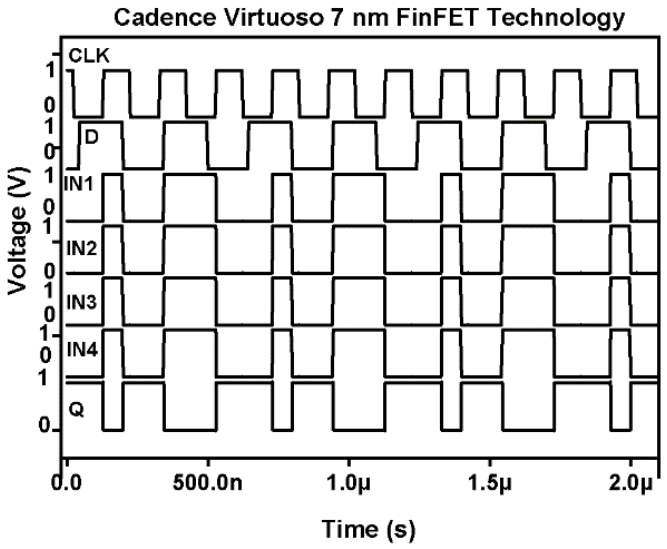

FIGURE 5.2: Simulation waveforms of the fault-free case for the proposed MCEST latch design.

eventually dissipates at IN2. Moreover, TFs at other internal nodes such as X3, X4, X5, and X6 do not cause output inversion in either clock state. This resilience is attributed to transistors (M5, M6, M7, M8), which ensure that the 2MCE1 latches new data only when both inputs are identical. similarly, TC2 restore IN3 and IN4. The MCEST latch functions as follows: When the clock signal is high (CLK = 1) and its complement is low (NCK = 0), transmission gates T1, T2, and T3 are all activated, putting the latch into its transparent state. In this mode, data passes from the D to Q via T3, and the CG-2MCE are

disabled to reduce both power and D-Q delay. During the hold mode (with CLK = 0 and NCK = 1), each transmission gate is deactivated while CG-2MCE turn on, which ensures the CG-2MCE output maintaining the previously stored latch state. Figure 5.2 shows the latch operation in error-free conditions.

5.3 Fault tolerance and recovery analysis (SNU / DNU)

In this section, the proposed MCEST latch tolerance and recovery analysis against SNU, and DNU is analyzed individually for each case. Additionally, we abstract the schematic by using internal nodes of the proposed MCEST latch to analyze the tolerance and recovery, as shown in Figure 5.1. First, looking at the transparent mode with CLK at 1, NCK at 0, and D at 1, all transmission gates (T1, T2, T3) transmit data to the next stage, resulting in node values of IN1, IN2, IN3 and IN4 are logic 1. Now, we discuss the circuit's behavior in hold mode when CLK = 0 and NCK = 1 under the influence of the radiation.

5.3.1 SNU fault tolerance and recovery analysis

In this case, four possible scenarios are exist, which are divided into two cases. Case S1: TF occurs inside FTST1, and Case S2: TF occurs inside CG-2MCE.

Case S1: In this case, we have considered that one TF occurs at the input of any FTSTs (here we consider FTST1). Suppose a TF occurs at node IN1, causing its logical value to flip from 1 to 0. In this scenario, the internal nodes IN1, IN2, IN3, and IN4 are at 0, 1, 1, and 1, respectively. Although the incorrect value at IN1 is propagated to FTST1 inputs, the output of FTST1 remains unaffected, as explained earlier. In a similar way, SNU fault tolerance analysis can be performed when SEs occur at other internal nodes, such as IN3.

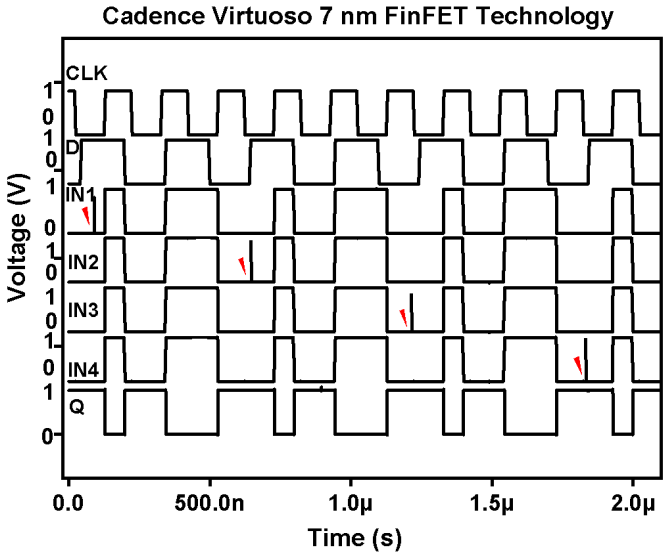

FIGURE 5.3: Simulation waveforms of SNU injections for the proposed MCEST latch design.

Case S2: In this case, we have considered that one TF occurs at the input of CG-2MCE. If a TF occurs at node IN2, the logical state of node IN2 changes from 1 to 0. In this scenario, the internal nodes IN1, IN2, IN3, and IN4 are at 1, 0, 1, and 1, respectively. Although the incorrect value of IN2 is propagated to the inputs of CG-2MCE, the output remains unaffected because of its inherent fault-tolerant properties discussed earlier. Similarly, SNU fault tolerance analysis can be performed when SEs affect other internal nodes, such as IN4. As shown in Figure 5.3, each sensitive node of the MCEST latch exhibits fault tolerance and recovery ability. These findings confirm that the proposed MCEST latch is tolerant under SNU conditions.

5.3.2 DNU fault tolerance and recovery analysis

In this case, six possible scenarios exist, which are divided into three cases. Case D1: two TFs occur inside FTST1, Case D2: two TFs occur inside CG-2MCE and Case D3: one TF occurs inside FTST1 and one TF occurs inside CG-2MCE.

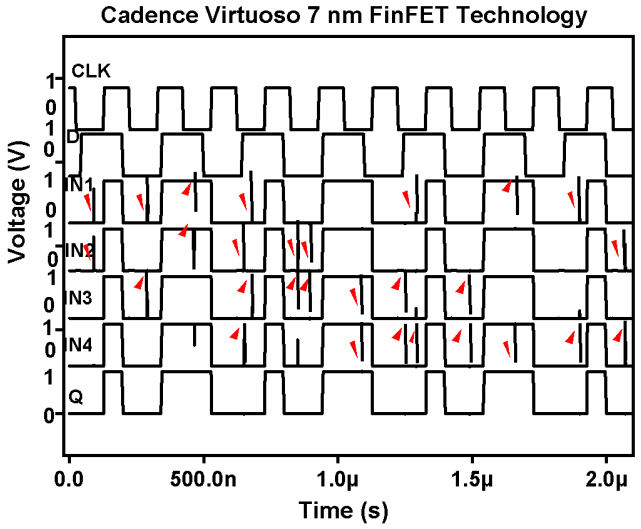

FIGURE 5.4: Simulation waveforms of DNU injections for the proposed MCEST latch design.

Case D1: In this case, we have considered that two TFs occur at the input of any FTSTs (here we consider FTST1). Suppose TFs occur at nodes IN1 and IN3, causing their states change logic 1 to logic 0. Under this condition, the internal nodes of FTST1 are IN1 = 0, IN2 = 1, IN3 = 0 and IN4 = 1. Although erroneous values at IN1 and IN3 are propagated to the inputs of both ST1 and FTST2, their outputs remain unaffected due to the fault-tolerant characteristics discussed earlier.

Case DN2: In this case, we have considered that two TFs occur at the input of CG-2MCE. When TFs occur at nodes IN2 and IN4, their values flip logic 1 to logic 0. As a result, the internal nodes of CG-2MCE are IN1 = 1, IN2 = 0, IN3 = 1 and IN4 = 0. Although erroneous values at IN2 and IN4 are propagated to the inputs of CG-2MCE, the outputs remain unchanged due to the fault-tolerant characteristics previously discussed.

Case DN3: In this case, we have considered the one TF occurs at the input of any FTSTs (here we consider FTST1) and one TF occurs at the input of CG-2MCE. Let us consider a scenario where TFs occur at nodes IN1 and IN4, causing the value of IN1 and IN4 flips logic 1 to logic 0. Under this condition, the susceptible nodes for FTST1 and CG-2MCE

are IN1 = 0, IN3 = 1, IN2 = 1 and IN4 = 0. Although these erroneous values at IN1 and IN4 are propagated to the inputs of FTST1 and CG-2MCE, their outputs remain unaffected due to the fault-tolerant features discussed earlier. Similarly, DNU fault tolerance analysis can be performed when SEs impact other internal node combinations, such as (IN1, IN2), (IN3, IN2), and (IN3, IN4). As shown in Figure 5.4, every sensitive node of the MCEST latch exhibits tolerance capability. These results confirm that the proposed MCEST latch is fully tolerant against DNU events.

5.4 Performance evaluation

The same simulation setup, operating conditions, and evaluation methodology adopted for design 1 are used in this chapter 5 as well. However, in the previous chapter, where the circuits were implemented using 45 nm CMOS technology, the proposed MCEST design in chapter 5 is implemented using 7 nm FinFET technology to achieve improved performance, reduced power, and enhanced scalability.

D-Q Delay: The value of D-Q delay for DICE [40], TMR [41], CHARGE-STEERING [92], LATCH [93], LATCH [96], LOCDNUTRL [57], RH-2 [64], DNUSH [56], HUDTAL [65], DNUCR [62], DURMA [67], and the proposed MCEST are found to be 1190.7 ps, 23680.7 ps, 122.1 ps, 329.3 ps, 23880.1 ps, 0.6 ps, 0.49 ps, 1.92 ps, 2.1 ps, 1.87 ps, 1.05 ps, and 0.41 ps, respectively, and the same is presented in Table 5.1. The results show that the proposed MCEST latch achieves the minimum D-Q delay compared to reported latches. Moreover, the effects of variations in temperature and supply voltage are also simulated, and the results are shown in Figures 5.5 and 5.6, respectively. It can be observed that the proposed designs shows better results in the entire voltage and temperature range as compared to the reported latches.

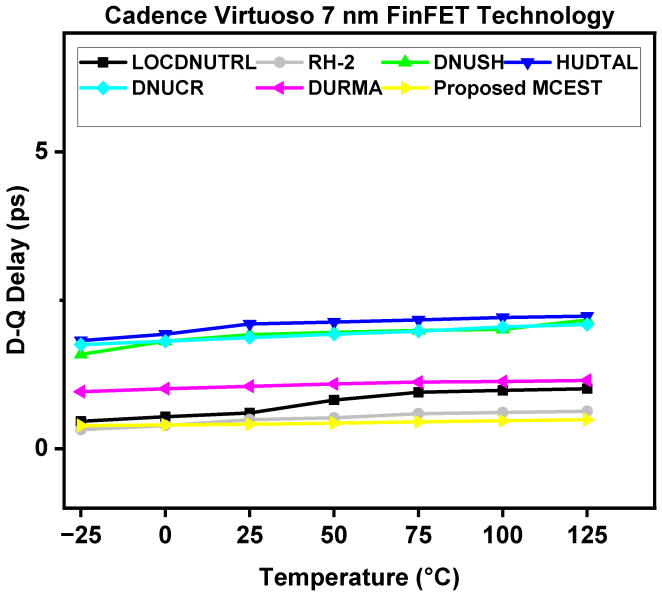

FIGURE 5.5: Temperature variation effect on D-Q delay of proposed MCEST and considered latches.

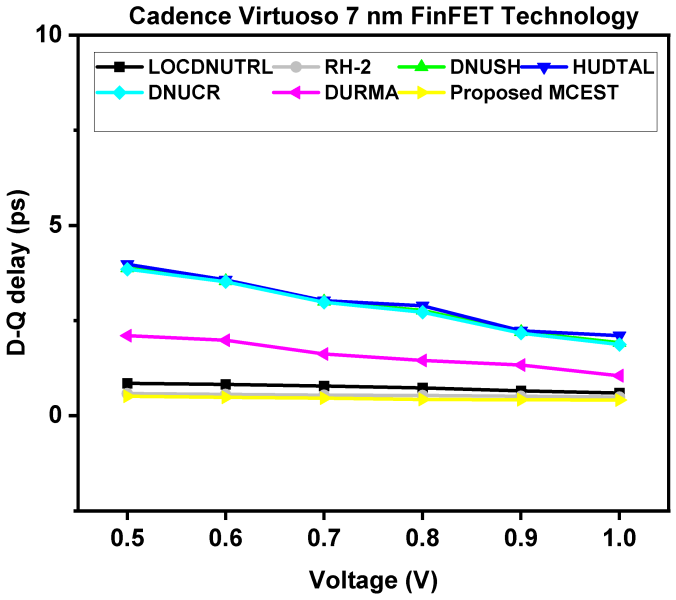

FIGURE 5.6: Voltage variation effect on D-Q delay of proposed MCEST and considered latches.

Power: The value of power for DICE [40], TMR [41], CHARGE-STEERING [92], LATCH [93], LATCH [96], LOCDNUTRL [57], RH-2 [64], DNUSH [56], HUDTAL

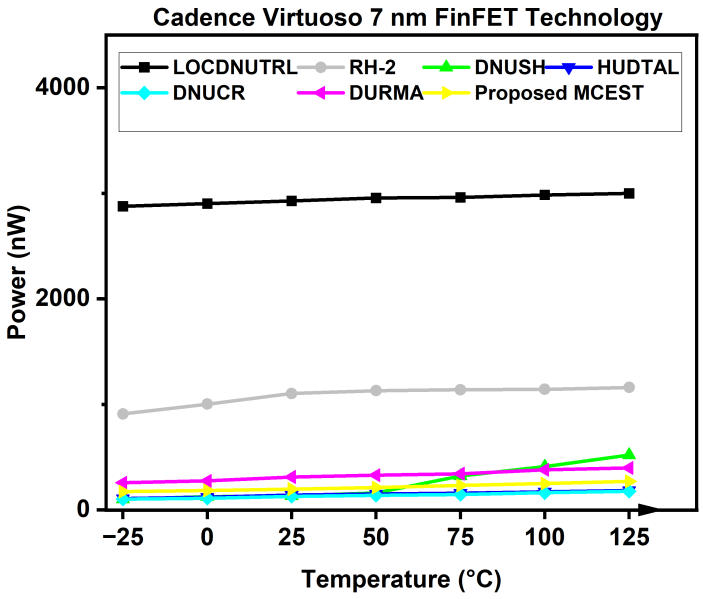

FIGURE 5.7: Temperature variation effect on power of proposed MCEST and considered latches.

[65], DNUCR [62], DURMA [67], and the proposed MCEST are found to be 653.24 nW, 12960.5 nW, 78.08 nW, 110.2 nW, 29.66 nW, 2927.1 nW, 1103.2 nW, 132.1 nW, 141.5 nW, 129.1 nW, 311.7 nW, and 198.2 nW, respectively, and the same is presented in Table 5.1. The results show that the proposed MCEST latch consumes moderate power compared to reported DNU radiation-hardened latches such as LOCDNUTRL [57], RH-2 [64], DNUSH [56], HUDTAL [65], DNUCR [62], and DURMA [67]. However, the proposed latch design has high power as compared to DNU based latches such as DNUSH [56], HUDTAL [65], DNUCR [62], but the reported latches have large D-Q delay. Moreover, the effects of variations in temperature and supply voltage are also simulated, and the results are shown in Figures 5.7 and 5.8, respectively. It can be observed that the proposed design shows better results in the entire voltage and temperature range as compared to the reported latches.

Critical Charge: The value of Qc for DICE [40], TMR [41], CHARGE-STEERING [92], LATCH [93], LATCH [96], LOCDNUTRL [57], RH-2 [64], DNUSH [56], HUDTAL

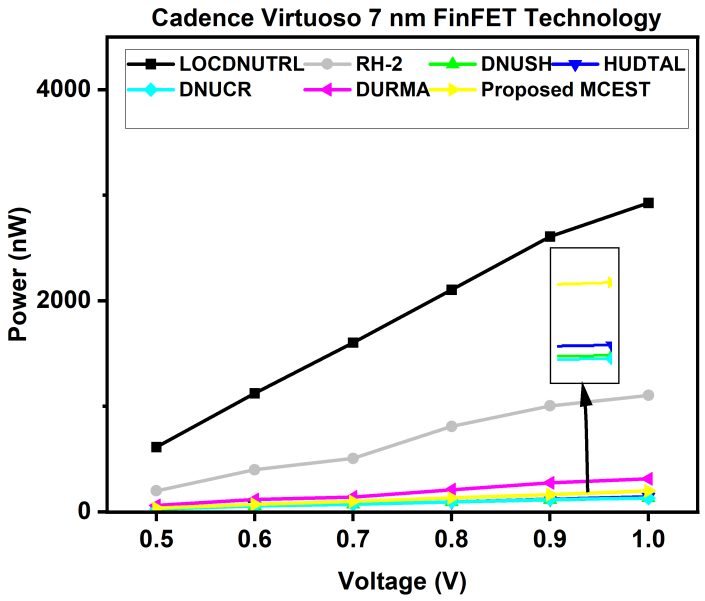

FIGURE 5.8: Voltage variation effect on power of proposed MCEST and considered latches.

TABLE 5.1: Comparison of proposed MCEST and considered latches using 7 nm FinFET technology node

Latch	Q_c **(fC)**	**Power (nW)**	**D-Q Delay (ps)**	**PDP (zJ)**	Q_c**/PDP (V^{-1})**
DICE [40]	1.02	653.24	1190.7	778015.67	1.3110
TMR [41]	0.73	12960.5	23680.7	306907944.4	0.00023
CHARGE-STEERING [92]	0.09	78.08	122.1	9531.77	9.4421
LATCH [93]	0.46	110.2	329.3	36277.86	12.6799
LATCH [96]	1.39	29.66	23880.1	707724.36	1.9640
LOCDNUTRL [57]	3.14	2927.1	0.6	1756.26	1787.89
RH-2 [64]	2.77	1103.2	0.49	540.57	5124.23
DNUSH [56]	3.42	132.1	1.92	253.63	13484.21
HUDTAL [65]	3.05	141.5	2.1	297.15	10264.18
DNUCR [65]	3.51	**129.1**	1.87	241.42	14538.98
DURMA [62]	3.24	311.7	1.05	327.28	9899.78
Proposed MCEST	**3.98**	198.2	**0.41**	**81.18**	**49026.85**

[65], DNUCR [62], DURMA [67], and the proposed MCEST are found to be 1.02 fC, 0.73 fC, 0.09 fC, 0.46 fC, 1.39 fC, 3.14 fC, 2.77 fC, 3.42 fC, 3.05 fC, 3.51 fC, 3.24 fC, and 3.98 fC, respectively, and the same is presented in Table 5.1. The results show that the proposed MCEST latch achieves the highest Qc compared to the reported latches.

PDP: The value of PDP for DICE [40], TMR [41], Charge-Steering [92], Latch [93], Latch [96], LOCDNUTRL [57], RH-2 [64], DNUSH [56], HUDTAL [65], DNUCR [62], DURMA [67], and the proposed MCEST are found to be 778015.67 zJ, 306907944.4 zJ, 9531.77 zJ, 36777.86 zJ, 707724.36 zJ, 1756.26 zJ, 540.57 zJ, 253.63 zJ, 297.15 zJ, 241.42 zJ, 327.28 zJ, and 81.18 zJ, respectively, and the same is presented in Table 5.1. The results show that the proposed MCEST latch achieves a lowest PDP compared the reported radiation-hardened latches.

Q_c/PDP: The value of Q_c/PDP for DICE [40], TMR [41], Charge-Steering [92], Latch [93], Latch [96], LOCDNUTRL [57], RH-2 [64], DNUSH [56], HUDTAL [65], DNUCR [62], DURMA [67], and the proposed MCEST are found to be 1.3110 V^{-1}, 0.0023 V^{-1}, 9.4421 V^{-1}, 12.6799 V^{-1}, 1.9640 V^{-1}, 1787.89 V^{-1}, 5124.23 V^{-1}, 13484.21 V^{-1}, 10264.18 V^{-1}, 14538.98 V^{-1}, 9899.78 V^{-1}, and 49026.85 V^{-1}, respectively, and the same is presented in Table 5.1. The results indicate that the proposed MCEST latch achieves the highest value of Q_c/PDP compared to the reported radiation-hardened latches.

Variability Analysis: The impact of various process corners for D-Q delay of all reported and proposed latches is shown in Figure 5.9. Similarly, the impact of various process corners on the power of all reported and proposed latches is shown in Figure 5.10. It may be noted that the D-Q delay is lowest for all latches at FF corner, and higher value is observed at SS corner. The power shows the reverse trend i.e. power is lowest at SS corner and highest at FF corner for all latches.

5.5 Summary

The proposed MCEST latch demonstrates the ability to tolerate from SNU and DNU at the sensitive nodes. It incorporates MCEs and a Schmitt Trigger circuit. Simulation results show significant performance enhancements, with improvements of up to 60.95%,

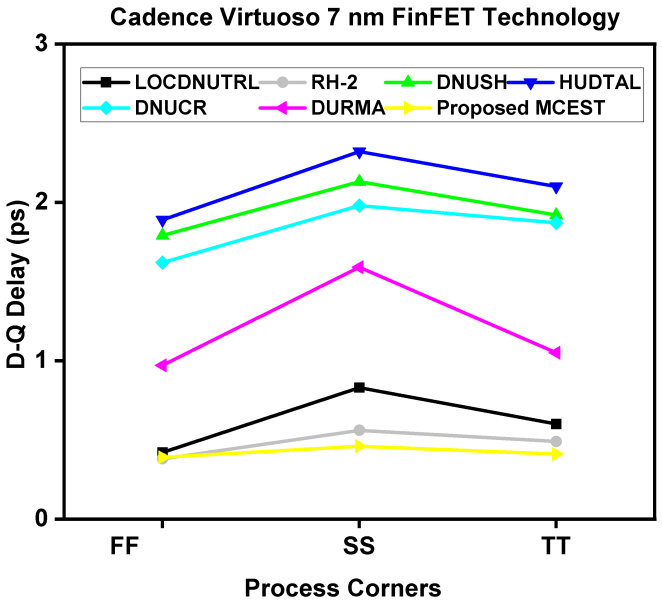

FIGURE 5.9: D-Q delay of proposed MCEST and considered latches at different process corners.

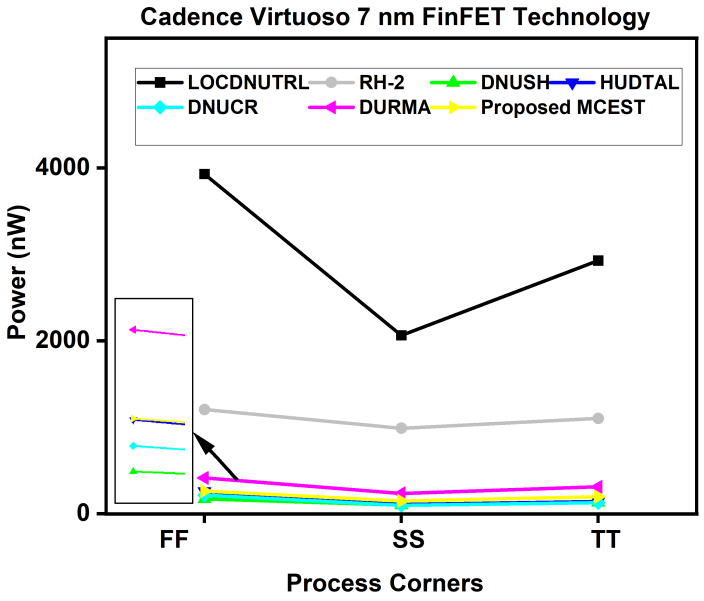

FIGURE 5.10: Power of proposed MCEST and considered latches at different process corners.

36.41%, 22.84%, 75.20%, and 395.25% in D-Q delay, power, Qc, PDP, and Qc to PDP ratio, respectively, when compared to the most recently reported latch DURMA [67]. The

proposed MCEST design features a fastest path due to transmission gate (T3), which improves the recovery time from SEs and greatly reduces delay. Additionally, it uses CG-2MCE, to achieve low power and reducing transistor count to save area. Furthermore, due to the highest Qc to PDP ratio, the proposed radiation-hardened latches are an excellent choice for space applications. The MCEST latch performs better across the entire voltage and temperature range for various parameters like power and delay.

Chapter 6

Conclusion and Future Scope

This thesis provides a thorough analysis of several radiation hardened designs, each of which is tailored to meet the needs of an application. The proposed designs aim to address the limitations of the radiation-hardened latches and FinFET-based designs. By overcoming these limitations, the proposed designs seek to improve energy efficiency, stability, and reliability. In addition to summarizing the primary findings, this chapter puts forward possible avenues for future research, development of radiation hardened designs and societal impact.

6.1 Summary of work done

Chapter 1 provides an introduction, motivation and a brief overview of the conventional D-latch architecture. After an assessment of the available radiation hardened latch designs, research gaps are identified and objectives are established. Finally, the thesis organization is provided. In space and terrestrial, energetic particles are the main source of latch soft errors (SEs). Therefore, improving their radiation-hardened performance requires reducing the probability of single-node upset (SNU). In order to address this, Chapter 2 presents two radiation hardened latches (proposed design 1 and proposed design 2) based on a Schmitt Trigger. Using a Schmitt Trigger, it enhances circuit robustness by its superior noise tolerance capability. The proposed design 1 is capable of recovering from SNU but at the cost of power consumption, delay, and area overhead. Therefore, proposed design 2 is offered to solve this issue. By reducing the number of transistors proposed design 2 reduces the cost and makes an energy-efficient design. The performance of the proposed designs 1 and 2 is compared with reported radiation hardened latches using Cadence Virtuoso simulations at 45 nm CMOS technology. The comparison in Table 6.1 shows that the QPAR of the proposed design 2 (CFTST) latch is 65.26% higher than the proposed design 1 (CSTST) latch, indicating improved radiation tolerance capability.

The latch designs discussed in the chapter 2 could withstand only SNU. Although these designs improved reliability of the circuits, they were unable to handle triple-node upset (TNU). Therefore, a latch structure with higher fault tolerance capability is required to ensure reliable operation under TNU. To solve this problem, chapter 3 (design 3) presents a radiation-hardened latch using muller c-elements (MCEs) for improved tolerance against TNU. The proposed design incorporates Multiple MCEs and clock gated muller c-element (CG-MCEs) to enhance the fault recovery mechanism against SNUs, DNUs, and TNUs. The proposed design 3 (TNURH) latch incorporates a high-speed transmission path (through faster and wider transmission gate T2). This approach significantly reduces D-Q delay and improves recovery time from TNU faults. The CG-4MCEs technique in a TNURH latch reduces power at the cost of area overhead. The latch design proposed in chapter 3 successfully improved tolerance against TNUs. However, this improvement resulted in higher power, increased D-Q delay, and larger area overhead. To achieve a better trade-off between reliability and design efficiency, a more cost-effective latch structure is required. To leverage the advantage of Schmitt Trigger and MCEs, a hybrid latch design 4 (CSTCE-TNURH) is presented in chapter 4. It improves tolerance against TNUs while reducing performance overheads. The number of transistors used in design is reduced, which makes the proposed CSTCE-TNURH latch more area efficient and cost-effective compared to the reported radiation hardened latches. The comparison in Table 6.1 confirms that the proposed CSTCE-TNURH latch achieves approximately 380% higher QPAR than the TNURH latch, showing significantly enhanced radiation tolerance capability.

The previous chapters (2, 3, 4) were 45 nm CMOS based latch designs that improved reliability against radiation. However, they suffered from several limitations such as larger area overhead, reduced scalability, and increased sensitivity to PVT variations at nanoscale dimensions. In addition, MOSFET based designs face challenges such as short-channel

effects and degraded performance as technology scales down. To overcome these drawbacks, FinFET technology has been adopted to propose DNU latch design 5 (MCEST) in chapter 5. Due to its compact structure and higher device density, FinFET technology provides better efficiency compared to CMOS technology.

TABLE 6.1: Comprehensive comparison of the radiation-hardened latch circuits

Latch	TC/ Device	ST/ MCE	SE Tolerance	Power	D–Q Delay	Q_c (fC)	PDP (aJ)	Area (μm^2)	QPAR
DICE	18/ CMOS	N/Y	SNU	388.60 nW	0.54 ns	10.55	209.84 aJ	9.45	0.0053
SEM	12/ CMOS	Y/N	SNU	177.90 nW	1.63 ns	9.85	289.98 aJ	6.47	0.0053
M-SEM	16/ CMOS	Y/N	SNU	194.10 nW	1.69 ns	9.89	328.03 aJ	8.45	0.0037
ST	14/ CMOS	Y/N	SNU	28.03 nW	1.17 ns	9.99	32.80 aJ	7.47	0.0407
HETR-HL	18/ CMOS	Y/Y	SNU	32.49 nW	1.14 ns	10.03	37.04 aJ	12.40	0.0222
NST-VB	14/ CMOS	N/Y	SNU	25.01 nW	1.07 ns	7.92	26.76 aJ	8.70	0.0340
FTST	**12/ CMOS**	**Y/N**	**SNU**	**10.59 nW**	**0.40 ns**	**10.09**	**4.24 aJ**	**6.72**	**0.3525**
CFTST	**12/ CMOS**	**Y/N**	**SNU**	**10.61 nW**	**0.41 ns**	**10.93**	**4.35 aJ**	**6.72**	**0.3730**
STST	**15/ CMOS**	**Y/N**	**SNU**	**14.04 nW**	**0.46 ns**	**10.14**	**6.46 aJ**	**7.58**	**0.2020**
CSTST	**15/ CMOS**	**Y/N**	**SNU/DNU/TNU**	**14.07 nW**	**0.47 ns**	**11.33**	**6.61 aJ**	**7.58**	**0.2257**
TNURH	**80/ CMOS**	**N/Y**	**SNU/DNU/TNU**	**0.94 μW**	**0.94 ns**	**37.60**	**883.60 aJ**	**440.01**	**0.35**
CSTCE–TNURH	**62/ CMOS**	**Y/Y**	**SNU/DNU/TNU**	**0.51 μW**	**0.51 ns**	**39.20**	**260.10 aJ**	**258.73**	**1.68**
MCEST	**52/ FinFET**	**Y/Y**	**SNU/DNU**	**198.2 nW**	**0.41 ps**	**3.98**	**81.26 zJ**	**–**	**–**

TC–Transistor Count, **Y**–Yes, **N**–No.

The salient features in terms of block level comparison and key performance parameters of proposed designs and benchmark latches, namely DICE, SEM, M-SEM, ST, HETR-HL, and NST-VB, under identical operating conditions (VDD = 1V, 45 nm CMOS (except for MCEST)) are summarized in Table 6.1. It may be observed that

- The proposed SNU latches FTST, CFTST, STST, CSTST outperform in comparison to benchmark circuits (DICE, SEM, M-SEM, ST, HETR-HL, and NST-VB) in terms of power, delay, PDP and QPAR. The critical charge is maximum for CSTST among proposed and benchmark circuits.

- The proposed designs TNURH and CSTCE-TNURH can handle SNU, DNU and TNU. These designs use more circuitry for handling more sensitive nodes which

results in more power and larger footprints. However, these designs have better QPAR among all considered designs.

- The performance of proposed FinFET based design MCEST is better CMOS based designs in terms of delay and PDP.

6.2 Future scope

Based on the research work presented in this thesis, a number of directions for future work have been identified.

1. The proposed latch designs in this thesis have been implemented using 45 nm CMOS and 7 nm FinFET technologies. Future research may focus on implementing and optimizing these designs in advanced technology nodes, such as 5 nm, 3 nm, and gate-all-around field-effect transistor (GAAFET) technologies, to further improve performance in terms of area and power consumption.

2. The present work primarily addresses fault tolerance against SNUs, DNUs, and TNUs. Future research may focus on designing latch architectures capable of recovering higher orders of MNUs caused by high-energy particle strikes in deeply scaled semiconductor technologies.

3. The radiation hardening methods proposed for latch circuits may be continued to design radiation-hardened flip-flops, registers and sequential logic blocks used in complex digital systems and processors.

4. The concepts of hardening against SE proposed in this thesis may be extended to design radiation-hardened SRAM cells and memory arrays to improve data reliability in radiation-prone environments.

6.3 Societal impact

Among different electronic components in every chip, sequential circuits (latches/ Flip-Flop/SRAM) represent up to 50% of the chip area. Sequential circuits, highly affect the chip efficiency, performance and reliability. In addition, the power consumption of the clock network, in latches/ Flip-Flop approximately more than half of the total chip power consumption. Therefore, efficient implementation of latches is of great importance for energy efficient and reliable ICs design. The societal impact of radiation-hardened latch designs extends beyond semiconductor reliability to the critical services enabled by modern ICs systems. These circuits are essential for guaranteeing the dependable operation of satellites and communication infrastructure that support weather forecasting, GPS navigation, disaster management and connectivity in remote regions. Therefore, they directly support to national development initiatives such as Digital India, smart agriculture, and environmental monitoring. By enabling robust and uninterrupted operation in radiation-prone environments, radiation-hardened systems enhance public safety, strengthen communication networks, and promote inclusive technological growth. High-altitude avionics, military electronic system, and defence infrastructure are continuously exposed to TF induced disturbances that can degrade system reliability. Radiation hardened latches help mitigate TF induced SEs, thereby guaranteeing reliable operation of essential electronic systems. Consequently, reliability of air traffic control is improved, and enhanced national security capabilities. Therefore, the proposed low-power and high-performance latch architectures enhance data integrity, system safety, and operational reliability under harsh environmental conditions. ———————————————————

References

[1] M. Alioto, "Ultra-low power vlsi circuit design demystified and explained: A tutorial," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 3–29, 2012.

[2] B. Warneke, M. Last, B. Liebowitz, and K. S. Pister, "Smart dust: Communicating with a cubic-millimeter computer," *Computer*, vol. 34, no. 1, pp. 44–51, 2001.

[3] R. Sharpeshkar, "Ultra low power bioelectronics: Fundamentals, biomedical applications, and bio-inspired system," 2010.

[4] W. Weber, J. Rabaey, and E. H. Aarts, *Ambient intelligence*. Springer Science & Business Media, 2005.

[5] S. M. Amin and B. F. Wollenberg, "Toward a smart grid: power delivery for the 21st century," *IEEE power and energy magazine*, vol. 3, no. 5, pp. 34–41, 2005.

[6] G. Bell, "Bell's law for the birth and death of computer classes," *Communications of the ACM*, vol. 51, no. 1, pp. 86–94, 2008.

[7] Y. Lee, G. Chen, S. Hanson, D. Sylvester, and D. Blaauw, "Ultra-low power circuit techniques for a new class of sub-mm 3 sensor nodes," in *IEEE Custom Integrated Circuits Conference 2010*. IEEE, 2010, pp. 1–8.

[8] M. Armand and J.-M. Tarascon, "Building better batteries," *nature*, vol. 451, no. 7179, pp. 652–657, 2008.

[9] M. H. Ghaed, G. Chen, R.-u. Haque, M. Wieckowski, Y. Kim, G. Kim, Y. Lee, I. Lee, D. Fick, D. Kim *et al.*, "Circuits for a cubic-millimeter energy-autonomous wireless intraocular pressure monitor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 12, pp. 3152–3162, 2013.

[10] T. Karnik and P. Hazucha, "Characterization of soft errors caused by single event upsets in cmos processes," *IEEE Transactions on Dependable and secure Computing*, vol. 1, no. 2, pp. 128–143, 2004.

[11] G. E. Moore *et al.*, "Cramming more components onto integrated circuits," 1965.

[12] N. H. Weste and D. Harris, *CMOS VLSI design: a circuits and systems perspective*. Pearson Education India, 2015.

[13] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted mosfet's with very small physical dimensions," *IEEE Journal of solid-state circuits*, vol. 9, no. 5, pp. 256–268, 2003.

[14] M. T. Bohr and I. A. Young, "Cmos scaling trends and beyond," *Ieee Micro*, vol. 37, no. 6, pp. 20–29, 2017.

[15] E. N. Shauly, "Cmos leakage and power reduction in transistors and circuits: process and layout considerations," *Journal of Low Power Electronics and Applications*, vol. 2, no. 1, pp. 1–29, 2012.

[16] I. R. Committee *et al.*, "International roadmap for devices and systems (irds)," 2018.

[17] WikiChip, "Wikichip," https://en.wikichip.org/, accessed: 2021-01-01.

[18] C. I. Kumar and A. Bulusu, "Design and analysis of energy efficient self correcting latches considering metastability," in *2018 14th Conference on Ph. D. Research in Microelectronics and Electronics (PRIME)*. IEEE, 2018, pp. 101–104.

[19] R. C. Baumann *et al.*, "Soft errors in advanced semiconductor devices-part i: the three radiation sources," *IEEE Transactions on device and materials reliability*, vol. 1, no. 1, pp. 17–22, 2001.

[20] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Transactions on nuclear Science*, vol. 50, no. 3, pp. 583–602, 2003.

[21] E. Normand, "Single event upset at ground level," *IEEE transactions on Nuclear Science*, vol. 43, no. 6, pp. 2742–2750, 1996.

[22] T. C. May and M. H. Woods, "Alpha-particle-induced soft errors in dynamic memories," *IEEE transactions on Electron devices*, vol. 26, no. 1, pp. 2–9, 1979.

[23] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Transactions on Device and materials reliability*, vol. 5, no. 3, pp. 305–316, 2005.

[24] C. Hsieh, P. C. Murley, and R. O'brien, "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices," *IEEE electron device letters*, vol. 2, no. 4, pp. 103–105, 2005.

[25] Y. Bentoutou and M. Djaifri, "Observations of single-event upsets and multiple-bit upsets in random access memories on-board the algerian satellite," in *Proceedings of the IEEE Nuclear Science Symposium Conference Record*, Oct. 2008, pp. 2568–2570.

[26] N. Cohen, T. S. Sriram, N. Leland, D. Moyer, S. Butler, and R. Flatley, "Soft error considerations for deep-submicron cmos circuit applications," in *IEDM Technical Digest*, Dec. 1999, pp. 315–318.

[27] S. Lin, Y.-B. Kim, and F. Lombardi, "Design and performance evaluation of radiation hardened latches for nanoscale cmos," *IEEE transactions on very large scale integration (VLSI) systems*, vol. 19, no. 7, pp. 1315–1319, 2010.

[28] J. W. Gambles, K. J. Hass, and S. R. Whitaker, "Radiation hardness of ultra low power cmos vlsi," in *11th NASA Symposium on VLSI Design*, 2003, pp. 1–6.

[29] A. Giraldo, A. Paccagnella, and A. Minzoni, "Aspect ratio calculation in n-channel mosfets with a gate-enclosed layout," *Solid-State Electronics*, vol. 44, no. 6, pp. 981–989, 2000.

[30] A. Giraldo, "Evaluation of deep submicron technologies with radiation tolerant layout for electronics in lhc environments," *Ph. D. Thesis at the University of Padova*, 1998.

[31] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Floria, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro *et al.*, "Radiation tolerant vlsi circuits in standard deep submicron cmos technologies for the lhc experiments: practical design aspects," *IEEE Transactions on Nuclear Science*, vol. 46, no. 6, pp. 1690–1696, 1999.

[32] L. Chen and D. M. Gingrich, "Study of n-channel mosfets with an enclosed-gate layout in a 0.18/spl mu/m cmos technology," *IEEE Transactions on Nuclear Science*, vol. 52, no. 4, pp. 861–867, 2005.

[33] L. Chen, "Radiation tolerant design with 0.18-micron cmos technology, ph.d. dissertation, dept. electrical and computer engineering, university of alberta, edmonton, ab, canada," 2004.

[34] L. Rockett, "An seu-hardened cmos data latch design," *IEEE Transactions on Nuclear Science*, vol. 35, no. 6, pp. 1682–1687, 1988.

[35] S. Whitaker, J. Canaris, and K. Liu, "Seu hardened memory cells for a ccsds reed-solomon encoder," *IEEE Transactions on nuclear science*, vol. 38, no. 6, pp. 1471–1477, 1991.

[36] D. Bessot and R. Velazco, "Design of seu-hardened cmos memory cells: the hit cell," in *RADECS 93. Second European Conference on Radiation and its Effects on Components and Systems (Cat. No. 93TH0616-3)*. IEEE, 1993, pp. 563–570.

[37] J. E. Knudsen and L. T. Clark, "An area and power efficient radiation hardened by design flip-flop," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3392–3399, 2006.

[38] Z. L. et al., "A high-performance and low-cost single-event multiple-node-upsets resilient latch design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 12, pp. 1867–1877, 2022.

[39] A. Yan, C. Lai, Y. Zhang, J. Cui, Z. Huang, J. Song, J. Guo, and X. Wen, "Novel low cost, double-and-triple-node-upset-tolerant latch designs for nano-scale cmos," *IEEE Transactions on Emerging Topics in Computing*, vol. 9, no. 1, pp. 520–533, 2018.

[40] T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron cmos technology," *IEEE Transactions on nuclear science*, vol. 43, no. 6, pp. 2874–2878, 1996.

[41] M. M. Ghahroodi, E. Ozer, and D. Bull, "Seu and set-tolerant arm cortex-r4 cpu for space and avionics applications," in *Proc. of the Workshop on Manufacturable and Dependable Multi-core Architectures at Nanoscale*, 2013.

[42] M. Fazeli, A. Patooghy, S. G. Miremadi, and A. Ejlali, "Feedback redundancy: A power efficient seu-tolerant latch design for deep sub-micron technologies," in *37th Annual IEEE/IFIP International Conference on dependable systems and networks (DSN'07)*. IEEE, 2007, pp. 276–285.

[43] M. Omana, D. Rossi, and C. Metra, "Latch susceptibility to transient faults and new hardening approach," *IEEE Transactions on Computers*, vol. 56, no. 9, pp. 1255–1268, 2007.

[44] S. Lin, Y.-B. Kim, and F. Lombardi, "Soft-error hardening designs of nanoscale cmos latches," in *2009 27th IEEE VLSI Test Symposium*. IEEE, 2009, pp. 41–46.

[45] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital integrated circuits*. Prentice hall Englewood Cliffs, 2002, vol. 2.

[46] S. Shirinzadeh and R. N. Asli, "A novel soft error hardened latch design in 90nm cmos," in *The 16th CSI International Symposium on Computer Architecture and Digital Systems (CADS 2012)*. IEEE, 2012, pp. 60–63.

[47] R. Niaraki Asli and S. Shirinzadeh, "High efficiency time redundant hardened latch for reliable circuit design," *Journal of Electronic Testing*, vol. 29, no. 4, pp. 537–544, 2013.

[48] L.-S. Kim and R. W. Dutton, "Metastability of cmos latch/flip-flop," *IEEE Journal of solid-state circuits*, vol. 25, no. 4, pp. 942–951, 1990.

[49] Z. Huang, H. Liang, and S. Hellebrand, "A high performance seu tolerant latch," *Journal of Electronic Testing*, vol. 31, no. 4, pp. 349–359, 2015.

[50] A. P. Shah, N. Gupta, and M. Waltl, "High-performance radiation hardened nmos only schmitt trigger based latch designs," *Analog Integrated Circuits and Signal Processing*, vol. 109, no. 3, pp. 657–671, 2021.

[51] C. I. Kumar and A. Bulusu, "High performance energy efficient radiation hardened latch for low voltage applications," *Integration*, vol. 66, pp. 119–127, 2019.

[52] A. K. Samal, S. Kumar, and A. Mukherjee, "Design of single node upset resilient latch for low power, low cost and highly robust applications," in *2023 IEEE International Test Conference in Asia (ITC-Asia)*. IEEE, 2023, pp. 1–5.

[53] F. Xia, J. Zhang, J. Ali, C. Zhang, X. Wen, and A. Yan, "Srbml: A single-event-upset recoverable and bti-mitigated latch design for long-term reliability enhancement," in *2024 IEEE International Test Conference in Asia (ITC-Asia)*. IEEE, 2024, pp. 1–5.

[54] A. Yan, Z. Huang, M. Yi, X. Xu, Y. Ouyang, and H. Liang, "Double-node-upset-resilient latch design for nanoscale cmos technology," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 6, pp. 1978–1982, 2017.

[55] A. Yan, K. Yang, Z. Huang, J. Zhang, J. Cui, X. Fang, M. Yi, and X. Wen, "A double-node-upset self-recoverable latch design for high performance and low power application," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 2, pp. 287–291, 2018.

[56] S. Kumar and A. Mukherjee, "A highly robust and low-power real-time double node upset self-healing latch for radiation-prone applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 29, no. 12, pp. 2076–2085, 2021.

[57] H. Xu, L. Zhou, H. Liang, Z. Huang, C. Sun, and Y. Ning, "High-performance double-node-upset-tolerant and triple-node-upset-tolerant latch designs," *Electronics*, vol. 10, no. 20, p. 2515, 2021.

[58] Y. Bai, X. Chen, X. Zhou, Y. Yin, and Y. Zhang, "Double-node-upset self-recoverable latch design for wide voltage range application," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 71, no. 3, pp. 1411–1415, 2023.

[59] C. I. Kumar and B. Anand, "A highly reliable and energy-efficient triple-node-upset-tolerant latch design," *IEEE transactions on nuclear science*, vol. 66, no. 10, pp. 2196–2206, 2019.

[60] Y.-M. Kang, J.-J. Park, G.-H. Kim, I.-J. Chang, and J. Kim, "Low-complexity double-node-upset resilient latch design using novel stacked cross-coupled elements," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 9, pp. 3619–3623, 2023.

[61] S. Hatefinasab, A. Medina-Garcia, D. P. Morales, E. Castillo, and N. Rodriguez, "Rule-based design for low-cost double-node upset tolerant self-recoverable d-latch," *IEEE Access*, vol. 11, pp. 1732–1741, 2023.

[62] S. Kumar and A. Mukherjee, "Low cost and high performance double-node upset resilient latch for low orbit space applications," *International Journal of Circuit Theory and Applications*, vol. 52, no. 5, pp. 2534–2549, 2024.

[63] Q. Zhao, H. Wang, L. Tian, S. Zhao, S. Zhang, L. Hao, X. Li, S. Lu, C. Peng, Z. Lin *et al.*, "A low overhead double-node-upset self-recoverable latch based on polarity design and source isolation technology," *International Journal of Circuit Theory and Applications*, vol. 53, no. 11, pp. 6665–6674, 2025.

[64] J. Guo, S. Liu, X. Su, C. Qi, and F. Lombardi, "High-performance cmos latch designs for recovering all single and double node upsets," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 57, no. 6, pp. 4401–4415, 2021.

[65] G. Qiu, D. Bi, Z. Hu, and Z. Zhang, "A novel high-speed ultralow power double-node-upsets tolerant automotive latch design," *International Journal of Circuit Theory and Applications*, vol. 53, no. 9, pp. 5498–5506, 2025.

[66] S. Kumar and A. Mukherjee, "Low cost and high performance double-node upset resilient latch for low orbit space applications," *International Journal of Circuit Theory and Applications*, vol. 52, no. 5, pp. 2534–2549, 2024.

[67] A. Yan, C. Hu, J. Li, N. Bai, Z. Huang, T. Ni, G. Patrick, and X. Wen, "Cost-optimized double-node-upset-recovery latch designs with aging mitigation and algorithm-based verification for long-term robustness enhancement," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2025.

[68] A. Yan, X. Feng, Y. Hu, C. Lai, J. Cui, Z. Chen, K. Miyase, and X. Wen, "Design of a triple-node-upset self-recoverable latch for aerospace applications in harsh radiation environments," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 56, no. 2, pp. 1163–1171, 2019.

[69] A. Watkins and S. Tragoudas, "Radiation hardened latch designs for double and triple node upsets," *IEEE Transactions on Emerging Topics in Computing*, vol. 8, no. 3, pp. 616–626, 2017.

[70] H. Xu, C. Sun, L. Zhou, H. Liang, and Z. Huang, "Design of a highly robust triple-node-upset self-recoverable latch," *IEEE Access*, vol. 9, pp. 113 622–113 630, 2021.

[71] H. Xu, C. Zhang, R. Ma, Z. Huang, S. Ye, H. Sun, Y. Dai, X. Chen, and Y. Tang, "A low-power triple-node-upset recovery hardened latch based on triple modular redundancy," *International Journal of Circuit Theory and Applications*, 2025.

[72] Z. Huang, D. Cao, J. Cui, Y. Lu, H. Liang, Y. Ouyang, T. Ni, and Z. Li, "Design of node separated triple-node-upset self-recoverable latch," *Microelectronics Journal*, vol. 114, p. 105111, 2021.

[73] A. Yan, K. Qian, J. Cui, N. Cui, T. Ni, Z. Huang, and X. Wen, "A sextuple cross-coupled dual-interlocked-storage-cell based multiple-node-upset self-recoverable latch," in *2021 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*. IEEE, 2021, pp. 1–6.

[74] A. Yan, Z. He, J. Zhou, J. Cui, T. Ni, Z. Huang, X. Wen, and P. Girard, "Dual-modular-redundancy and dual-level error-interception based triple-node-upset tolerant latch designs for safety-critical applications," *Microelectronics Journal*, vol. 111, p. 105034, 2021.

[75] Z. Huang, H. Wang, Y. Ang, H. Liang, Y. Ouyang, and T. Ni, "A high-speed and triple-node-upset recovery latch with heterogeneous interconnection," *Microelectronics Journal*, vol. 118, p. 105290, 2021.

[76] A. Yan, S. Song, Y. Chen, J. Cui, Z. Huang, and X. Wen, "A low-cost and robust latch protected against triple node upsets in nanoscale cmos based on source-drain cross-coupled inverters," in *2022 IEEE 22nd International Conference on Nanotechnology (NANO)*. IEEE, 2022, pp. 215–218.

[77] Y. Lu, G. Hu, J. Wang, H. Wang, L. Yao, H. Liang, M. Yi, and Z. Huang, "A low power-consumption triple-node-upset-tolerant latch design," *Journal of Electronic Testing*, vol. 38, no. 1, pp. 63–76, 2022.

[78] A. Yan, Z. Lin, Y. Xu, N. Bai, J. Cui, Z. Huang, T. Ni, P. Girard, and X. Wen, "Triple-node-upset recovery high-impedance-state insensitive and single-event-transient filtering latch for aerospace applications," *IEEE Transactions on Aerospace and Electronic Systems*, 2025.

[79] A. Yan, Z. Li, S. Huang, Z. Zhai, X. Cheng, J. Cui, T. Ni, X. Wen, and P. Girard, "Sclcrl: Shuttling c-elements based low-cost and robust latch design protected against triple node upsets in harsh radiation environments," in *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*. IEEE, 2022, pp. 1257–1262.

[80] H. Xu, C. Liu, R. Ma, H. Liang, Z. Huang, J. Zhou, and S. Zhu, "A triple-node-upset self-recoverable design based on schmitt-triggers and c-elements," *Microelectronics Reliability*, vol. 144, p. 114977, 2023.

[81] S. Cai, C. Xie, Y. Wen, W. Wang, F. Yu, and L. Yin, "Four-input-c-element-based multiple-node-upset-self-recoverable latch designs," *Integration*, vol. 90, pp. 11–21, 2023.

[82] Z. Huang, H. Wang, D. Ma, H. Liang, Y. Ouyang, and A. Yan, "Low overhead and high stability radiation-hardened latch for double/triple node upsets," *Journal of Electronic Testing*, vol. 39, no. 3, pp. 289–301, 2023.

[83] H. Xu, L. Tang, R. Ma, H. Liang, Z. Huang, T. Ni, J. Li, and X. Ai, "A cost-effective and highly robust triple-node-upset self-recoverable latch design based on dual-output c-elements," *Microelectronics Journal*, vol. 153, p. 106422, 2024.

[84] L. Hao, L. Tian, H. Wang, S. Zhao, Q. Zhao, C. Peng, C. Dai, Z. Lin, and X. Wu, "A low-cost and triple-node-upset self-recoverable latch design with low soft error rate," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 33, no. 4, pp. 1108–1117, 2025.

[85] H. Xu, J. Li, R. Ma, H. Liang, C. Liu, S. Wang, and X. Wen, "A low-area overhead and low-delay triple-node-upset self-recoverable design based on stacked transistors," *IEEE Transactions on Device and Materials Reliability*, vol. 24, no. 2, pp. 302–312, 2024.

[86] C. Peng, L. Tian, L. Hao, Q. Zhao, C. Dai, Z. Lin, and X. Wu, "High-performance latch designs of double-node-upset self-recovery and triple-node-upset tolerance for aerospace applications," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 60, no. 5, pp. 6550–6561, 2024.

[87] Q. Zhao, Q. Liu, X. Zhang, L. Hao, X. Li, S. Zhang, C. Peng, Z. Lin, and X. Wu, "A high-performance and high-robustness triple-node-upset tolerant latch based on redundant-node hardening," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 2025.

[88] Y. Bai, X. Chen, Y. Yang, X. Zhou, and Y. Zhang, "Triple-node-upset self-recoverable latch design for aerospace applications," *Microelectronics Reliability*, vol. 154, p. 115338, 2024.

[89] E. Paparsenos and Y. Tsiatouhas, "Radiation-hardened latch design with triple-node-upset recoverability," *AEU-International Journal of Electronics and Communications*, vol. 187, p. 155539, 2024.

[90] X. Chen, Y. Bai, H. Cai, C. Zhu, X. Zhou, Y. Zhang, and W. Liu, "Low-overhead triple-node-upset self-recoverable latch design for ultra-dynamic voltage scaling application," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 71, no. 6, pp. 2632–2645, 2024.

[91] S. Kumar and A. Mukherjee, "A triple-node upset self-healing latch for high speed and robust operation in radiation-prone harsh-environment," *Microelectronics Reliability*, vol. 139, p. 114857, 2022.

[92] B. Narasimham, K. Chandrasekharan, J. K. Wang, K. Ni, B. L. Bhuva, and R. D. Schrimpf, "Charge-steering latch design in 16 nm finfet technology for improved soft error hardness," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 353–358, 2016.

[93] F. Razi, M. H. Moaiyeri, and R. Rajaei, "Design of an energy-efficient radiation-hardened non-volatile magnetic latch," *IEEE Transactions on Magnetics*, vol. 57, no. 1, pp. 1–10, 2020.

[94] M. Moghaddam, M. H. Moaiyeri, and M. Eshghi, "Design and evaluation of an efficient schmitt trigger-based hardened latch in cntfet technology," *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 1, pp. 267–277, 2017.

[95] S. Shakeel and N. Alam, "Cntfet based radiation hardened latch," *Australian Journal of Electrical and Electronics Engineering*, vol. 18, no. 3, pp. 199–208, 2021.

[96] S. Wang and K. Namba, "C-element-based latch for flip-flops: Complete snu and partial dnu tolerance and resilience to soft errors around clock edges," in *2025 1st International Conference on Consumer Technology*, 2025, pp. 1–4.

[97] O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm cmos technology," *IEEE Transactions on nuclear science*, vol. 53, no. 6, pp. 3253–3258, 2006.

[98] O. Chertkow, A. Pescovsky, L. Atias, and A. Fish, "A novel low power bitcell design featuring inherent seu prevention and self correction capabilities," *Journal of Low Power Electronics and Applications*, vol. 5, no. 2, pp. 130–150, 2015.

[99] S. Pal, D. D. Sri, W.-H. Ki, and A. Islam, "Highly stable low power radiation hardened memory-by-design sram for space applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 6, pp. 2147–2151, 2020.

[100] Y. Q. Aguiar, F. Wrobel, J.-L. Autran, P. Leroux, F. Saigné, A. D. Touboul, and V. Pouget, "Analysis of the charge sharing effect in the set sensitivity of bulk 45 nm standard cell layouts under heavy ions," *Microelectronics Reliability*, vol. 88, pp. 920–924, 2018.

List of Publications

Journals

* N. Kumar, C. I. Kumar, and N. Pandey, **"High-performance radiation hardened latch using Schmitt trigger,"** Integration, vol. 104, Feb. 2025, doi: 10.1016/j.vlsi.2025.102478.

* N. Kumar, C. I. Kumar, and N. Pandey, **High-performance and robust triple-node-upset radiation hardened latch design,"** AEÜ – Int. J. Electron. Commun., vol. 201, July 2025, 10.1016/j.aeue.2025.155977.

* N. Kumar, C. I. Kumar, and N. Pandey, **"High-Performance Cascode Schmitt-Trigger and C-Element based Triple Node Upset Radiation Hardened Latch,"** Microelectronics Reliability, vol. 182, p. 116174, 2026.

Presentations and proceedings in International/National Conferences

* N. Kumar, N. Pandey, and C. I. Kumar **"Schmitt Trigger Based Compact Radiation Hardened Latch,"** 2025 IEEE 4th Int. Conf. Adv. Technol., pp. 1 7, 2025, doi: 10.1109/ICONAT66879.2025.11362702.

* N. Kumar, N. Pandey, and C. I. Kumar, **"High Performance Double Node Upset Radiation Hardened Latch in 7 nm FinFET,"** 2025 10th Int. Conf. Commun. Electron. Syst., pp.589–594, 2025, doi: 10.1109/ICCES67310.2025.11337000.

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High-performance radiation hardened latch using Schmitt trigger

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ARTICLE INFO

Keywords:
Transient fault
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Single event upset
Radiation hardening

ABSTRACT

This paper presents a novel 45 nm CMOS radiation-hardened latch design for low-voltage applications. This paper focusses on the Schmitt trigger-based latch, which enhances robustness through increased node capacitance, providing better noise tolerance. While other types of latch designs uses redundant nodes for radiation hardening but faces reliability issues in modern technologies. This work presents two transient fault-tolerant latch designs based on a seven-transistor Schmitt trigger (STST). The proposed latch circuits are designed and implemented under the 45 nm CMOS technology node. The proposed latch provides the single event upset (SEU) tolerance using the STST latch to hold the correct state. The proposed designs for making STST latch radiation hardened is to increase the node capacitance at susceptible nodes by adding an STST block. The first design STST latch has a lower delay of 57%, a higher critical charge of 28.03%, a lower power of 43.86%, a lower power delay product (PDP) of 75.86%, and a higher critical charge to power delay area product ratio (QPAR) of 494.12% with a decreased area of 12.87% than recently proposed latches. The second design, the cascode seven-transistor Schmitt trigger (CSTST) latch, has a cascode feedback loop in place of a transmission gate and inverter with an improved critical charge of 11.74% and a higher critical charge to power delay area product ratio (QPAR) of 11.73% than the STST latch without an area increase.

1. Introduction

Nowadays, electronic gadgets require low-power VLSI (very large-scale integration) circuits. The applications of low-power VLSI circuits are biomedical devices, wearable devices, pollution monitoring devices, etc. [1]. These application of devices comes up with some challenges, like battery life, size of technology node, and supply voltage. Since battery technology growth is slower than CMOS (Complementary Metal–Oxide–Semiconductor) technology, researchers are putting their efforts into reducing the size of the technology node [2,3]. As the size of the technology node and supply voltage decreases day by day, VLSI circuits are more vulnerable to transient faults (TFs) due to reduced charge stores at circuit nodes [4]. When a high-energy cosmic radiation and alpha particle hits in a transistor's sensitive area and produces electron–hole pairs (EHPs), a transient fault (TF) occurs [5–7]. Consequently, a substantial current/voltage develops at that node when the electric field quickly collects the carriers. A soft error (SE) occurs when a TF delivered from a combinational logic circuit is stored in a memory unit as a single event upset (SEU) [7]. A soft error is a significant problem in sequential circuits because node faults can cause data to flip in memory parts [8]. The D-latch is highly vulnerable to SEU when high-energy particles strike. One effective method to reduce TF is radiation hardening by design (RHBD). A dual interlocked cell (DICE) proposed in [9] uses several redundant nodes for storage to achieve a radiation-hardened design. DICE can withstand transient faults without increasing transistor width or node capacitance. Researchers found the DICE cell unreliable in modern technologies [10]. On the other side, the Schmitt trigger-based radiation-hardened latches proposed in [11] increases the node capacitance to increase the circuit's hardness. This paper mainly focused on a Schmitt trigger-based radiation-hardened design because of better noise tolerance than other designs.

The remaining sections are arranged as follows. In Section 2, the previous hardened latch designs are reported. In Section 3, the proposed structure, working principle, and transient fault resilience are presented. Section 4 provides Simulation Results and Comparison. Process variation effects are presented in Section 5, and Section 6 concludes this paper.

2. Previous hardened latches

The schematic of a traditional D-latch [12] is shown in Fig. 1. The input and output signals are 'd' and 'q', respectively. The D-latch uses two clocks, CLK and NCK, corresponding to a clock signal and a negative clock signal. There are three inverters (I1, I2, and I3) in

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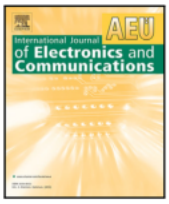

Regular paper



High-performance and robust triple node upset radiation hardened latch design

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Triple-node upset
Self-recover

ABSTRACT

As the technology node of transistors continues to scale down, integrated circuits are more vulnerable to multiple-node-upset (MNU), like double-node upset (DNU) and triple-node upset (TNU). This paper presents a novel 45 nm CMOS triple-node upset radiation-hardened (TNURH) latch for high performance applications. The latch consists of transmission gates (TGs), four input C-Elements (FICEs), and clock gating-based four input C-Elements (CGFICEs). The proposed latch can self-recover from any node upsets, such as single-node upsets (SNUs), double-node upsets (DNUs), and triple-node upsets (TNUs). According to simulation results, the proposed TNURH latch improves the performance results in terms of average power, D–Q delay, CLK-Q delay, power delay product (PDP), area, and power delay area product (PDAP) up to 37.75%, 23.53%, 0.046%, 52.94%, 36.17%, and 69.61% than the recently reported latch. Furthermore, the process, voltage, and temperature (PVT) variations and the Montecarlo (MC) simulations show that the proposed TNURH latch effectively handles the variations.

1. Introduction

Low-power CMOS (Complementary Metal Oxide Semiconductor) circuits are becoming essential for electronic devices. Low-power CMOS circuits are used in the Internet of Things (IoT), biomedical devices, pollution monitoring devices, and other applications [1]. Designing CMOS circuits with reduced area, delay, and power consumption is challenging for designers and manufacturers [2]. As the size of CMOS technology scales down, circuits are more susceptible to transient faults (TFs) due to reduced charge stores at circuit nodes [3]. When alpha particles or cosmic rays strike susceptible nodes of circuits, they produce electron–hole pairs (EHPs), leading to an unexpected transient pulse or disturbance known as a transient fault (TF) or, sometimes called soft error (SE) [4]. A single event transient (SET) is the term used to describe TF for combinational logic circuits [5]. Single event upsets (SEU) occur when the TF transmitted by the combinational logic circuit is stored in the memory element [6]. Single-node upsets (SNU), double-node upsets (DNU), and triple-node upsets (TNU) are examples of TF. When alpha particles or cosmic rays strike, a charge is collected at that node through drift and diffusion operations in transistors, and there is a voltage spike in single susceptible nodes called SNU. However, if a voltage spike occurs, two nodes at a time are called DNU. Similarly, if a voltage spike occurs, three nodes at a time are called TNU [7]. This encourages us to create highly reliable circuits that are resistant to transient faults, particularly for electronic gadgets in extreme radiation conditions. Recent TNU latches meet the stringent requirements of radiation-sensitive applications by balancing resilience against radiation-induced errors with efficient use of power, area, and speed through the use of advanced design strategies such as polarity-based configurations, self-recovery techniques, and stacked transistor arrangements. At present, the most effective method for solving the TNU is radiation hardened by design (RHBD). Without altering the design flow, the RHBD technique is widely used. Fault tolerance is achieved by the RHBD approach at the cost of increased area overhead, delay, and power consumption [8]. Due to the extensive use of latch/flip-flop in digital systems, researchers are now focusing on developing radiation-hardened latch/flip-flop. In this paper, we present a triple-node upset (TNU) resilient latch for applications in radiation-rich and energy-sensitive environments. The main contributions and unique features of our work are as follows:

1. Reliable State Preservation During TNUs: The proposed design uses an innovative transistor-level configuration to ensure that the correct logic state is preserved even when exposed to triple-node upsets. This robust performance exceeds that of existing latch designs, enhancing data integrity in challenging environments.

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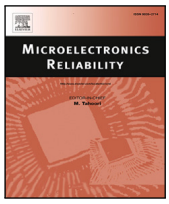

Research paper



High-performance cascode Schmitt-Trigger and C-element based triple node upset radiation hardened latch

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ABSTRACT

As integrated circuits (ICs) technology scales down, ICs are susceptible to multiple node upsets (MNUs), including double node upsets (DNUs) and triple node upsets (TNUs). This paper presents a novel 45 nm CMOS cascode Schmitt trigger and Muller C-element based triple node upset radiation hardened latch (CSTCE-TNURH), developed for high-speed and low-power applications. The latch architecture uses transmission gates (Ts), cascode Schmitt triggers (CSTs), and a clock-gated three-input C-element (CGTICE). The proposed latch features a high-speed data path for reduced D–Q delay, clock-gating for lower power consumption, and a reduced transistor count for smaller area. Simulation results confirm the latch's robustness, showing performance improvements over the most recently reported MCTHSL (Yan et al., 2025) latch up to 92.14% in average power, 92.80% in D–Q delay, 99.42% in PDP, 43.67% in area, 99.67% in PDAP, 51.53% in critical charge (Qc), and 55900% in Qc-to-PDAP ratio. Furthermore, process corner and Monte Carlo (MC) simulations confirm the latch's resilience to process, voltage, and temperature (PVT) variations under harsh conditions. Monte Carlo simulations show that the proposed latch achieves 84.15% and 97.19% lower standard deviations in D-Q propagation delay and power consumption than the most recent MCTHSL (Yan et al., 2025) latch.

1. Introduction

Nowadays, integrated circuits (ICs) require low-power consumption circuits. The applications of low-power ICs are in medical equipment, wearable devices, aerospace, pollution monitoring devices, automobiles, etc. [1–3]. These applications face several challenges: supply voltage, battery life, and technology node size. Since the advancement in battery technology growth is slower than the progress in complementary metal–oxide–semiconductor (CMOS) technology, researchers are focusing on reducing the size of the technology node [4]. As the size of the CMOS technology node and supply voltage scale down, circuits are more susceptible to transient faults (TFs) due to less charge stored at circuit nodes [5]. When a high-energy cosmic radiation and an alpha particle strike at the transistor's sensitive area and generate electron–hole pairs (EHPs). Due to this, a transient fault (TF) occurs, which is known as a soft error (SE) [6]. For combinational logic circuits, TF is referred to as a single event transient (SET) [7] while single event upsets (SEU) occur when the TF is delivered from a combinational logic circuit to a sequential circuit [8]. When cosmic rays or alpha particles hit a node, charge accumulates due to drift and diffusion within the transistors, leading to a significant current or voltage at a single vulnerable node, known as a single-node upset (SNU). If this significant current or voltage occurs simultaneously, two nodes at a time are called double node upset (DNU). Similarly, if a significant current or voltage occurs simultaneously, three nodes at a time are called triple-node upsets (TNU) [9]. Radiation hardening by design (RHBD) is the most effective way to overcome soft errors. However, its robustness can still be significantly influenced by manufacturing defects. The STAHL [10] reported that undetected manufacturing defects can substantially reduce single-event upset (SEU) resilience and introduced the Post-Test Vulnerability Factor (PTVF) to quantify this degradation. In addition, HIDER [11] presents defect-aware hardened latch architectures that achieve both high defect detectability and strong SEU tolerance. These findings highlight that manufacturing defects can easily compromise the soft-error tolerance capability of hardened latches if defect coverage is not adequately addressed. To overcome radiation-hardened issues, a dual interlocked cell (DICE) proposed in [12] uses multiple redundant nodes for storage to achieve a radiation-hardened design. The DICE can tolerate transient faults without increasing transistor width or node capacitance. Researchers observed that DICE cells are unreliable in modern technologies [13]. Conversely, the Schmitt trigger-based radiation-hardened latches proposed in [14] enhance circuit robustness by increasing the node capacitance and its superior noise tolerance capability.

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Schmitt Trigger Based Compact Radiation Hardened Latch

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***Abstract*—Nanoscale circuits are more vulnerable to transient faults or soft errors because the charge stored at their sensitive nodes is significantly reduced. As a result, modern designs strictly mandate that these circuits be able to withstand soft errors. In this paper, a novel 45nm CMOS radiation-hardened latch design is proposed. Using a four-transistor Schmitt trigger (FTST), two different kinds of soft error-tolerant latch designs are presented in this paper. Simulation results demonstrate the robustness of the proposed FTST latch by improving the performance results in terms of average power, D-Q delay, critical charge, power delay product (PDP), area, and charge-to-power-delay-area product ratio (QPAR) up to 57.65%, 62.62%, 27.40%, 82.76%, 22.76%, and 936.76% then the recently reported latch. In comparison to the FTST, the second type of proposed cascode four-transistor Schmitt trigger (CFTST) latch has an enhanced critical charge and QPAR 8.32% and 5.82%, respectively.**

***Index Terms*—Single node upset, Radiation hardening, Schmitt trigger, Soft error, Low power.**

I. Introduction

The emergence of nanotechnology from explorative to industrial applications has pushed researchers to extensively examine the circuits and look into intricate details [1]. The scaling has resulted in miniaturized devices and a nature consequence of this is smaller nodal capacitances. Couple with this, supply voltages are also decreased, which ultimately reduces the charge stores at circuit nodes, making circuits more vulnerable to transient faults (TFs'), referred to as soft errors (SEs') [2,3]. Electronic circuits on Earth experience terrestrial soft errors due to the presence of either neutron particles from cosmic rays or alpha particles from packing. However, most causes of the soft error in space are heavy ions, protons, and electrons. When a high-energy particle hits a transistor's sensitive area and produces electron-hole pairs (EPs), a soft error happens [4]. A reverse-biased transistor's drain/source diffusion gathers these charge carriers. As a result, the transistor that has been turned off momentarily begins to conduct, altering the logic level of the impacted node [5]. This causes a glitch at the node, which leads to a transient fault (TF) and could cause a soft error or system failure [6]. One node flip in the latch is called single node upset (SNU).

Sequential circuits enable soft errors due to their intrinsic nature of storing the state of the system [7]. A soft error can significantly increase the sensitivity of a traditional static reference latch. The most effective way to withstand soft errors is to use radiation hardening by design (RHD). The widespread usage of latch/flip-flop in digital systems has attracted the attention of researchers towards designing radiation-hardened latch/flip-flop. The radiation-hardened latch design is the primary subject of this article. Firstly, examine previous radiation-hardened latches.

This is how the rest of the article is structured. Section 2 explains the existing hardened latch, Section 3 describes the proposed latch's operation, implementation, and soft-error resilience. The simulation and comparison using cadence 45-nm CMOS technology are presented in Section 4. Section 5 explains Process variation analysis. Section 6 discusses the conclusions and the observations that were made.

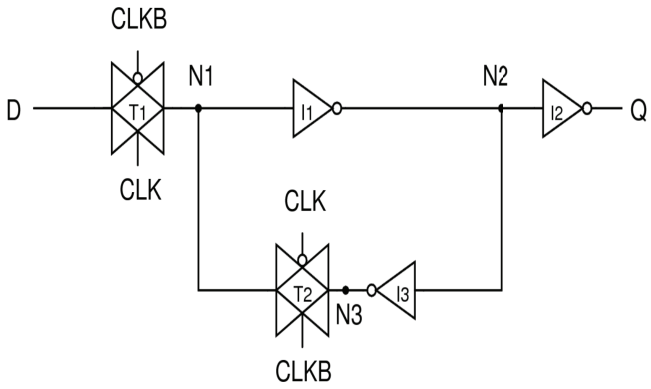

Fig. 1. Refrence Latch.

II. Overview of Existing Hardened Latch

A popular latch circuit, known as the Reference latch [8] in this paper, is depicted in Figure 1. The reference latch utilizes two transmission gates, one placed in the forward path(T1) and the other in the feedback path(T2). In addition, the latch contains three inverters, namely, I1, I2, and I3: I1 and I2 are in the forward path, while I3 is placed in the feedback path. The signals CLK and CLKB represent the clock and its complement, respectively. When CLK is at a high logic level, the latch functions in transparent mode; when CLK is at a logic low level, it works in hold mode. Typically, radiation sensitivity is evaluated during the hold mode. Among all

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High Performance Double Node Upset Radiation Hardened Latch in 7 nm FinFET

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***Abstract*—Soft errors in sequential circuits are more likely to occur when circuit density increases, the minimum charge needed to change a node's state (critical charge) decreases, and voltage levels drop. To overcome these issues, radiation-hardened circuit designs are required to self-recover from soft errors. This work introduces a new radiation-hardened latch design in 7 nm FinFET technology that integrates a Muller C-element with a Schmitt trigger (MCEST). Simulation results show significant performance enhancements, with improvements of up to 60.95%, 0.0009%, 36.41%, 22.84%, 75.20%, and 395.25% in d-to-q delay, clk-to-q delay, power, critical charge (Q_c), power-delay product (PDP), and critical charge to PDP ratio, respectively, when compared to the most recently reported latch. The MCEST latch performs better across the entire voltage and temperature range for various parameters like power and delay.**

***Index Terms*—Double node upset, Soft error, Radiation hardening, Low power, Schmitt trigger.**

I. Introduction

Today's electronic devices need integrated circuits (ICs) that have low power consumption. Wearable technology, environmental monitoring devices, biomedical gadgets, and space applications are examples of low-power ICs [1]. Battery life, supply voltage, and technology node size are issues with these device applications. The CMOS technology is growing more quickly than battery technology; therefore, researchers are working to scale down the size of the technological node [1]. Using FinFET rather than MOSFET in digital circuits can achieve smaller circuits with higher reliability [2]. Compared to MOSFETs of the same size, FinFETs offer higher ON currents [3]. The FinFET channel width changed by varying fin height; thus FinFET is far denser than the planar MOSFET [4]. When transistor sizes decrease, circuits are more susceptible to soft errors (SEs) because circuit nodes have smaller charge storage [5]. When cosmic rays or alpha particles impact vulnerable circuit nodes, Electron-hole pairs (EHPs) are created. This results in an unexpected disturbance known as soft error (SE) or transient fault (TF) [6]. Since node faults can result in data change in memory components, a TF is a major issue in sequential circuits [7]. Soft errors in sequential circuits are more likely to occur when circuit density increases, the minimum charge needed to change a node's state (critical charge) decreases, and voltage levels drop [8]. When alpha particles or cosmic rays hit transistors, resulting in a voltage spike at a single vulnerable node, known as an SNU. If the voltage spike happens simultaneously at two nodes, it is referred to as a DNU [9].

At present, radiation hardened by design (RHBD) is the most efficient approach to tackling the DNU. The RHBD approach is extensively utilised without changing the design flow [10]. The dual interlocked cell (DICE) latch presented in [5] achieves a radiation-hardened (RH) by utilising multiple redundant nodes for storage. The researchers found that under modern technologies field, the DICE latch is unreliable [1]. Conversely, the Schmitt trigger (ST) based RH latches presented in [1] increase the node capacitance to enhance the design robustness. ST based RH designs offer improved noise immunity, whereas the DICE architecture [5] incurs higher power consumption and occupies more area due to its large transistor count. Due to its superior noise tolerance compared to other designs, the ST with Muller C-element (MCE) based radiation-hardened device is the primary focus of this work.

The following is the remaining sections. Section 2 presents existing RH designs. The proposed latch architecture, operation, and transient fault resilience presented in section 3. simulations and cost of the comparison table are discussed in Section 4. Section 5 presents process, voltage, and temperature (PVT) change, while Section 6 will conclude this paper.

II. Existing Hardened Latch

The DICE latch presented in [5] is capable of switching states only if more than two state nodes are simultaneously disturbed. The TMR latch [6] consists a majority voter. But, significant area overhead is the main limitation of the TMR latch. The latch presented in [2] requires a pulse generator, providing additional delay. The inclusion of additional blocks in latch presented in [3] leads to higher circuit complexity and greater energy consumption during data backup. The latch presented in [4] cannot maintain full DNU tolerance at clock edges due to design limitations, making the latch vulnerable to data latching errors in certain DNU cases. The LOCD-NUTRL latch [8] uses two single node upset self-recovery cells, utilizing MOS transistors for pull-up and pull-down operations, enabling rapid correction of particle strike-induced logic errors; however, it consumes more power. The RH-2 latch presented in [9] generates a radiation-induced voltage

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PLAGIARISM VERIFICATION

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Department: Electronics and Communication Engineering

Co-Supervisor: Dr. Chaudary Indra Kumar

Department: Electrical Engineering

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SUMMARY

Detail-oriented researcher with a Ph.D. in VLSI, focused on the design of energy-efficient and radiation-tolerant latches for space applications. Expertise in Digital Electronics, Digital IC Design, CMOS Layout, and Radiation-Hardened Circuits.

SKILLS

- EDA Tools: ***Cadence Virtuoso***, H-Spice, LT-Spice.
- Physical Design: **RTL-to-GDSII**, FP, PP, PLC, CTS, Routing, STA, TC, DRC/LVS, PPA.
- HDL Languages: Verilog, Icarus Verilog, Verilator VHDL, Xilinx Vivado, FPGA
- Simulation & Analysis: MATLAB, PSPICE, LabVIEW, LaTeX, Origin
- Programming: C, C++.

ACHIEVEMENTS

- Completed Ph.D. **in 3 years**.
- **Three SCIE**-indexed journal papers and two international conference papers.
- Received three Research Excellence Awards.
- GATE Qualified: 2017–2021 **(five consecutive years)**.
- **NCC 'C'** Certificate Holder.

EXPERIENCE

National Yunlin University of Science and Technology, TAIWAN.

Postdoc in VLSI (pursuing), **Remote**. **July 2026 – Present**

Assistant Professor (VLSI/ECE) ***May 2026 – Present***

K.R. Mangalam University, Gurugram, India

- Delivered lectures, tutorials, and labs in Digital Electronics and VLSI
- Conducted laboratory sessions using **Cadence Virtuoso** and Xilinx Vivado, FPGA.

Industry Exposure: RTL to GDS-II Internship ***July 2026 — Present***

NIELIT – Noida, India, **Remote**

- Gained hands-on experience in the complete ASIC **RTL-to-GDSII** Physical Design flow, including RTL synthesis, floorplanning, power planning, placement, CTS, routing, STA, timing closure, DRC/LVS, and chip implementation using industry-standard EDA tools.

Industry Exposure: VLSI Design Internship ***Sep 2022 — Feb 2023***

Maven Silicon - Bengaluru, India, **Remote**

Developed practical skills in RTL design using Verilog HDL, simulation, synthesis, timing analysis, and FPGA prototyping following industry-standard VLSI design practices.

Guest Faculty (ECE/VLSI) ***Mar 2026 – May 2026***

Lloyd Institute of Engineering & Technology, Greater Noida, India

- Delivered lectures, tutorials, and labs in Digital Electronics and VLSI

EDUCATION

Delhi Technological University (DTU) ***2023 — 2026***

Delhi, India | Ph.D. in VLSI

Thesis: Design of Energy-Efficient and Radiation-Tolerant Latches.

Institute of Radio-physics and Electronics ***2017 — 2019***

Calcutta, India | M.Tech. in VLSI Design (7.93)

Project: Implementation of DCT using FPGA.
Designed and implemented 1D-DCT architecture in Verilog with a pipelined structure.

CERTIFICATIONS AND LICENSES

- Advanced VLSI Design – Maven Silicon, Centre of Excellence in VLSI (Blended Learning Course), Completed: 25 Feb 2023.
- One-Week Faculty Development Program on 'Advancements and Challenges in VLSI Design and Nanoscale Devices'.
- 5G and Beyond: What is Next? – Department of Electrical Engineering, IIT Kanpur (Short Course), Completed: 14 December 2022.

HOBBIES AND INTERESTS

- Chess, Music
- Innovative approach to circuit design.
- Strong research aptitude and academic integrity.
- Excellent problem-solving and mentoring abilities.

WEBSITES AND SOCIAL LINKS

- LinkedIn: https://www.linkedin.com/in/niraj-pathak-5766b810a/
- ORCID: https://orcid.org/0009-0002-8453-2495

LANGUAGES

English

- Verified using MATLAB and implemented on Xilinx Spartan-3 FPGA at 34.435 MHz.

Institute of Radio-physics and Electronics, Calcutta ***2014 — 2017***

Calcutta, India | B.Tech in ECE in Electronics & Communication / Radiophysics (7.47)

Project: Fabrication and Study of Metal-Semiconductor Contacts.

- Fabricated metallic contacts using photolithography, metallization, and etching.

Atma Ram Sanatan Dharma College, University of Delhi ***2011 — 2014***

Delhi, India | B.Sc. (Hons.) in Electronics (75.33%)
- Graduated with First Class Honours in B.Sc. Electronics.

RESEARCH PUBLICATIONS

1. **N. Kumar**, C. I. Kumar, and N. Pandey, "High-performance radiation-hardened latch using Schmitt trigger," Integration, the VLSI Journal, 2025.

   Available: https://doi.org/10.1016/j.vlsi.2025.102478 **(SCIE)**
2. **N. Kumar**, C. I. Kumar, and N. Pandey, “High-performance and robust triple-node-upset radiation-hardened latch design,” AEÜ – Int. J. Electron. Commun., vol. 201, July 2025.

   Available: https://doi.org/10.1016/j.aeue.2025.155977 **(SCIE)**
3. **N. Kumar**, C. I. Kumar, and N. Pandey, "High-performance cascode Schmitt-trigger and C-element-based triple node upset radiation-hardened latch," Microelectronics Reliability, vol. 182, p. 116174, 2026. [Online]. Available: https://doi.org/10.1016/j.microrel.2026.116174. **(SCIE)**
4. **N. Kumar**, N. Pandey, and C. I. Kumar, “High Performance Double Node Upset Radiation Hardened Latch in 7 nm FinFET,” 2025 10th Int. Conf. Commun. Electron. Syst., pp. 589–594, 2025.

   Available: https://doi: 10.1109/ICCES67310.2025.11337000.
5. **N. Kumar**, N. Pandey, and C. I. Kumar, “Schmitt Trigger Based Compact Radiation Hardened Latch,” 2025 IEEE 4th Int. Conf. Adv. Technol., pp. 1–7, 2025, doi: 10.1109/ICONAT66879.2025.11362702.

   Available: https://doi.org/10.1109/ICONAT66879.2025.11362702