Design, Modeling and Characterization of Interleaved Multiport Power Converters for Battery Charging and Discharging Applications

A Thesis Submitted
In Partial Fulfillment of the Requirements
for the Degree of

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by

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I NISHANT KUMAR (2K20/PHDEE/13) hereby certify that the work which is being presented in the thesis entitled **"Design, Modeling, and Characterization of Interleaved Multiport Power Converters for Battery Charging and Discharging Applications"** in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the Department of Electrical Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from August 2020 to July 2026 under the supervision of Dr. Mayank Kumar, Assistant Professor. The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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Certified that **Nishant Kumar (2K20/PHDEE/13)** has carried out his research work presented in this thesis entitled **"Design, Modeling, and Characterization of Interleaved Multiport Power Converters for Battery Charging and Discharging Applications"** for the award of **Doctor of Philosophy** from Department of **Electrical Engineering**, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student himself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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ABSTRACT

The increasing integration of renewable energy sources, electric vehicles (EVs), energy storage systems, and other high-power DC loads has created a growing need for efficient, reliable, and dynamically stable power conversion systems for DC microgrids. In particular, battery charging, hydrogen electrolyzers, and hybrid energy storage applications require converters capable of handling high current with reduced ripple, high efficiency, low semiconductor stress, and effective thermal utilization. Conventional single-phase converters often face limitations in these applications due to high current stress, increased conduction losses, and comparatively large input and output current ripple. Interleaved and multiport DC–DC converter configurations provide attractive solutions by distributing power among multiple phases and enabling coordinated power transfer between different sources, storage devices, and loads.

This thesis presents the modeling, characterization, design, and control of interleaved and multiport DC–DC converters for high-current charging, renewable-energy integration, and battery–supercapacitor hybrid energy storage applications. Initially, an n-phase interleaved buck converter (*n*PIBC) is investigated considering practical circuit parasitics. A generalized state-space model is developed from the detailed analysis of a three-phase interleaved buck converter (TPIBC), and the steady-state and small-signal characteristics are derived using the state-space averaging technique. The influence of source resistance, inductor resistance, capacitor equivalent series resistance, semiconductor voltage drops, and other non-ideal parameters on converter dynamics and stability is analyzed. Comparative assessment of single-phase, two-phase, and three-phase configurations demonstrates the advantages of interleaving in terms of current ripple, stability, current sharing, and conduction losses. The analytical results are validated experimentally using a laboratory prototype.

The dynamic and time-domain characteristics of the TPIBC are further investigated for constant-power, constant-current, and resistive loads. Analytical expressions are developed for input-current, output-current, and inductor-current ripple under overlapping and non-overlapping duty-ratio conditions and for both continuous and discontinuous conduction modes. The effects of duty ratio, load condition, operating region, and number of phases on converter losses and ripple characteristics are established. These results provide useful design guidelines for selecting the DC-bus voltage, duty ratio, and converter operating region to achieve reduced ripple and

improved efficiency in high-current applications such as battery charging and electrolyzers.

For applications requiring bidirectional power transfer, a three-phase interleaved bidirectional resonant converter (TPIBRC) is developed for EV battery charging and discharging. The proposed converter combines multiphase interleaving with resonant operation to reduce current ripple and distribute the converter current among the phases while enabling soft-switching operation. A control strategy based on pulse-width and frequency modulation is developed to regulate power flow and output voltage over a varying DC-bus voltage. The proposed converter is designed for a 72-V battery system supplied from a 360-V DC bus, and its operation is verified through simulation with zero-voltage-switching operation.

The thesis further proposes a four-port DC–DC converter for battery–supercapacitor energy storage (FPDCBSS) to integrate renewable energy sources, battery storage, supercapacitor storage, and the DC bus through a reduced-component power conversion structure. Averaged and small-signal models are developed for different operating states and are employed for controller design and stability analysis. A coordinated power-management strategy assigns slowly varying power demands to the battery while directing rapid transient power components to the supercapacitor. This reduces high-frequency battery current stress and improves the dynamic response of the DC bus. Robust controller parameters are determined considering converter operating variations, and the proposed concept is validated through simulation and experimental testing of a 100-W prototype.

Overall, the thesis establishes a systematic framework for the modeling, parasitic-aware characterization, ripple and loss analysis, stability assessment, control design, and experimental validation of interleaved buck converter and multiport DC–DC converters. The results demonstrate that appropriate selection of the number of phases, duty ratio, operating region, resonant characteristics, and power-sharing strategy can significantly improve converter performance. The developed converter configurations and analytical methodologies provide practical design guidelines for renewable-energy-based DC microgrids, EV charging and discharging infrastructure, hydrogen electrolyzers, and battery–supercapacitor hybrid energy storage systems.

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LIST OF ABBREVIATIONS

PV	Photovoltaic
DG	Distributed Generation
BESS	Battery Energy Storage System
HESS	Hybrid Energy Storage System
SESS	Supercapacitor Energy Storage System
BSCES	Battery–Supercapacitor based Energy Storage System
EV	Electric Vehicle
IBC	Interleaved Buck Converter
VRM	Voltage Regulator Module
HFT	High-Frequency Transformers
CBC	Classical Buck Converter
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
PM	Phase Margin
GM	Gain Margin
*n*PIBC	*n*-phase Interleaved Buck Converter
TPIBC	Three-phase Interleaved Buck Converter
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
FC	Fast Charging
PWM	Pulse Width Modulation
SSA	State Space Averaged
MSO	Mixed Signal Oscilloscope
TR	Theoretical Results
ER	Experimental Results

ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
SSRC	Soft Switching Resonant Converter
BDC	Bidirectional Converter
DAB	Dual Active Bridge
HV	High Voltage
SRC	Series Resonant Converter
PRC	Parallel Resonant Converter
SPRC	Series-Parallel Resonant Converter
TPRC	Three Port Resonant Converter
TPIBRC	Three-phase Interleaved Bidirectional Resonant Converter
PI	Proportional-Integral
HF	High Frequency
CBC	Classical Buck Converter
SPV	Solar Photovoltaic
MPC	Multiport Converter
ESS	Energy Storage System
FPDCBSS	Four-Port DC-DC Converter for Battery-Supercapacitor-based ESSs
MPPT	Maximum Power Point Tracking

LIST OF SYMBOLS

v_S	Source voltage
v_O	Output voltage
v_{SWx}	x^{th} branch switch ON voltage drop for *n*PIBC
v_{Dx}	x^{th} branch diode voltage drop for *n*PIBC
sw_x	x^{th} branch switch for *n*PIBC
D_x	x^{th} branch diode for *n*PIBC
L_x	x^{th} branch inductor for *n*PIBC
C	Filter capacitor for *n*PIBC
R_S, R_C	ESR of source, ESR of filter capacitor for *n*PIBC
R_O	Load Resistance
R_{Lx}	ESR of xth branch inductor for *n*PIBC
i_S	Source current for *n*PIBC
i_x, i_{Lx}	Current through x^{th} branch switch and inductor for *n*PIBC
I_{Lx}	Average inductor current through x^{th} branch for *n*PIBC
$\triangle i_{Lx}$	Inductor ripple current through x^{th} branch for *n*PIBC
i_C	Current through filter capacitor for *n*PIBC
i_O	Output current for *n*PIBC
I_O	Average output current for *n*PIBC
$\triangle i_O$	Output ripple current *n*PIBC
i_{load}	Load current for *n*PIBC
f_s	Switching frequency for *n*PIBC
f_{ri}	Effective ripple frequency for *n*PIBC
d	Duty ratio of individual switches during turn-on for *n*PIBC
R_1, R_2, R_3	Regions of Operations for TPIBC
v_{oa}	Average output voltage
d_a	Discharging time duty ratio under DCM for TPIBC
Δi_S	Input ripple current for TPIBC
P_{Sw}	Switching power loss of each switch for TPIBC

t_r	Switch turn-on time of each switch for TPIBC
t_f	Switch turn-off time of each switch for TPIBC
$i_{Lx\,min}$	Minimum value of inductor current ripple for TPIBC
$i_{Lx\,max}$	Maximum value of inductor current ripple for TPIBC
E_{Sw}	Switching energy loss of each switch for TPIBC
P_{CR}	Conduction loss of individual switches due to on state resistance for TPIBC
P_{CVS}	Conduction loss of individual switches due to v_{SW} for TPIBC
P_{CVD}	Conduction loss of individual switches due to v_D for TPIBC
P_{CER}	Conduction loss due to ESR of each inductor (R_L) for TPIBC
P_{loss}	Total loss of TPIBC
P_L	Fixed Power Load
L_r, C_r	Resonant tank inductor and capacitor
L_m	Magnetising inductance
S_1, S_2, S_3, S_4	Input active full bridge switches for TPRC
P_1, P_2, P_3	Output ports for TPRC
D_1, D_2, D_3, D_4	Diode full bridge corresponding to P1 for TPRC
D_5, D_6, D_7, D_8	Diode full bridge corresponding to P2 for TPRC
D_9,D_{10},D_{11},D_{12}	Diode full bridge corresponding to P3 for TPRC
L_{O1}, L_{O2}, L_{O3}	Parallel inductor corresponding to P1, P2, P3 respectively for TPRC
L_P	Equivalent parallel inductance
L_S	Equivalent series inductance
$V_{ab,f}$, $V_{cd,f}$	Fundamental component of voltage of equivalent circuit of TPRC
R_F	Full load resistance
V_B	Base voltage
Z_B	Base impedance
i_B	Base current
δ	Input Pulse width

f_r	Resonant Frequency
F	Normalized switching frequency
M	Gain
Q	Quality factor
λ	Normalized inductance
R_{ac}	AC equivalent resistance
S_{P1x}, $S_{P3x,}$ S_{P2x}, S_{P4x}	Input active full bridge switches of xth branch for TPIBRC
S_{S1x}, $S_{S3x,}$ S_{S2x}, S_{S4x}	Secondary side active full bridge switches of P1 of xth branch for TPIBRC
D_{5x}, $D_{6x,}$ D_{7x}, D_{8x}	Diode full bridge corresponding to P2 of xth branch for TPIBRC
D_{9x}, $D_{10x,}$ D_{11x}, D_{12x}	Diode full bridge corresponding to P3 of xth branch for TPIBRC
Φ	Phase shift angle between the two sides switch bridges
V_{cxPeak}	Peak resonant tank capacitor voltage
i_{sxPeak}	Series tank peak current
$v_{S,nom}$	Nominal input voltage
$v_{S,min}$	Minimum input voltage
$v_{S,max}$	Maximum input voltage
V_{PV}	Solar PV voltage for FPDCBSS
i_{in}	Solar PV generated current for FPDCBSS
i_B	Battery current for FPDCBSS
i_{SC}	Supercapacitor current for FPDCBSS
i_O	Load current for FPDCBSS
L_S	Input port inductance for FPDCBSS
L_B	Battery port inductance for FPDCBSS
L_{SC}	Supercapacitor port inductance for FPDCBSS
S_S	Input port switch for FPDCBSS

S_1, S_2	Switches for hybrid battery supercapacitor-based operation for FPDCBSS
S_b	Switch integrating load with BSCES for FPDCBSS
V_{SC}	Supercapacitor voltage for FPDCBSS
V_{bat}	Battery voltage for FPDCBSS
C_O, C_b, C_C	Filter capacitor across load and battery and capacitance of supercapacitor for FPDCBSS
R_O, R_B, R_{SC}	Load resistance and battery and SC internal resistance for FPDCBSS
P_L, P_{LF}, P_{HF}	Total load, low frequency and high frequency component of load for FPDCBSS
P_B, P_{SC}	Battery and supercapacitor reference power for FPDCBSS
K_p , K_i	Proportional gain and Integral gain of controllers for FPDCBSS
f_{LPF}	Low pass filter for FPDCBSS
i_{LF_ref}	Low frequency reference current(for battery) for FPDCBSS
i_{HF_ref}	High frequency reference current(for SC) for FPDCBSS
r_{LS}, r_{LB}, r_{LSC}	ESR of inductance for input port, battery port and SC port for FPDCBSS
r_{Co}, r_{Cb}, r_{Cc}	ESR of Filter capacitor across load and battery and ESR of supercapacitor for FPDCBSS

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Chapter 1

Introduction

The traditional power generation system requires the power plant generating units, together with large-scale transmission and distribution networks, to distribute electricity to consumers. However, concern about greenhouse gas emissions have raised due to the rapid use of fossil fuels like coal, gasoline, etc. and the increasing need for energy [1]-[3]. These difficulties have led the world's transition to clean, sustainable energy production. Renewable energy sources, particularly solar photovoltaic (PV) and wind energy systems [1], have emerged as attractive alternatives to conventional fossil fuel-based power generation. Their adoption is further supported by the availability of abundant natural resources and declining installation costs [3]. The distributed generation (DG) is being adopted widely across the world to cope up with energy demand for DC microgrid, the electrification of transportation, and other applications. These DG have contributed to a sharp increase in the demand for highly efficient power electronic conversion systems that can provide reliable and flexible energy management.

1.1 Distributed Generation and the Transition Towards Sustainable Energy Systems

DG is becoming an essential component of contemporary electrical power systems. A DG process generates electricity in close proximity to the point of consumption by using relatively small-scale production units. Renewable energy sources that can be integrated into the distribution network or used as localized energy systems include fuel cells, PVs, wind energy, and small-scale hydroelectric systems. Among these technologies, solar PV generation has attracted a lot of attention due to its modularity, scalability, ease of installation, and applicability for both grid-connected and free-standing applications [4], [5].

The available renewable energy sources are naturally intermittent such as PV electricity is based on temperature and solar irradiation, whereas wind energy output is influenced by wind speed and environmental conditions. As a result, the instantaneous power

generated by renewable sources may not always be adequate for the power needed by the related loads. This mismatch may cause variations in DC-bus voltage, power flow, and system operating conditions [6], [7]. Therefore, the effective integration of distributed renewable energy sources depends on power converters and energy storage devices [7]. Energy storage systems (ESSs) are capable of absorbing excess energy during periods of high renewable energy generation and producing power during periods of low generation. By serving as the electrical link between renewable energy sources, storage devices and loads, power electronic converters provide voltage conversion, current regulation, regulated power transmission, and bidirectional energy flow [8].

The development of DC based energy systems has also increased due to the growing usage of renewable energy sources. PV arrays, batteries, supercapacitors, electric cars, data servers, electrolyzers, and many more contemporary sources, storage devices, and loads are either intrinsically DC or internally demand DC power [9]-[12]. Consequently, DC microgrids has become the best method for integration of DG, energy storage, and modern electrical loads. For renewable energy-based DC microgrids and their related applications to be implemented successfully, efficient, small and dependable DC-DC power converters must be developed. In high-current applications, where minimal current ripple, high efficiency, decreased semiconductor stress, and efficient thermal management are required, this requirement of such converter becomes very crucial [12].

1.2 DC Microgrid for Renewable Energy Integration and Power Management

A DC microgrid, shown in Fig. 1.1 is a small-scale power system that connects electrical loads, ESS, and dispersed energy sources via a single DC bus [6]-[7]. Unlike traditional AC distribution systems, DC microgrids eliminate needless AC–DC and DC–AC conversion stages by directly integrating several connected DC sources and loads [13]. The PV generation with wind turbine generation along with battery ESS (BESS), supercapacitors, grid interfaces, electric vehicle (EV) charging stations, hydrogen electrolyzers, data centers, and other DC demands can all be found in a typical renewable-energy-based DC microgrid [10], [14], [15]. Power is transferred between these components via the common DC bus, which serves as the central energy-transfer interface [15].

Various kinds of power-flow scenarios could arise, depending on the availability of renewable energy and load demand. The excess energy can be used to charge the battery and/or supercapacitor when renewable energy generation exceeds the instantaneous load requirement [15]. The ESS can cover the shortfall and keep the DC-bus voltage stable at times when renewable power is insufficient. In a similar manner, the ESS can offer temporary power backup during abrupt changes in load demand [15]-[17].

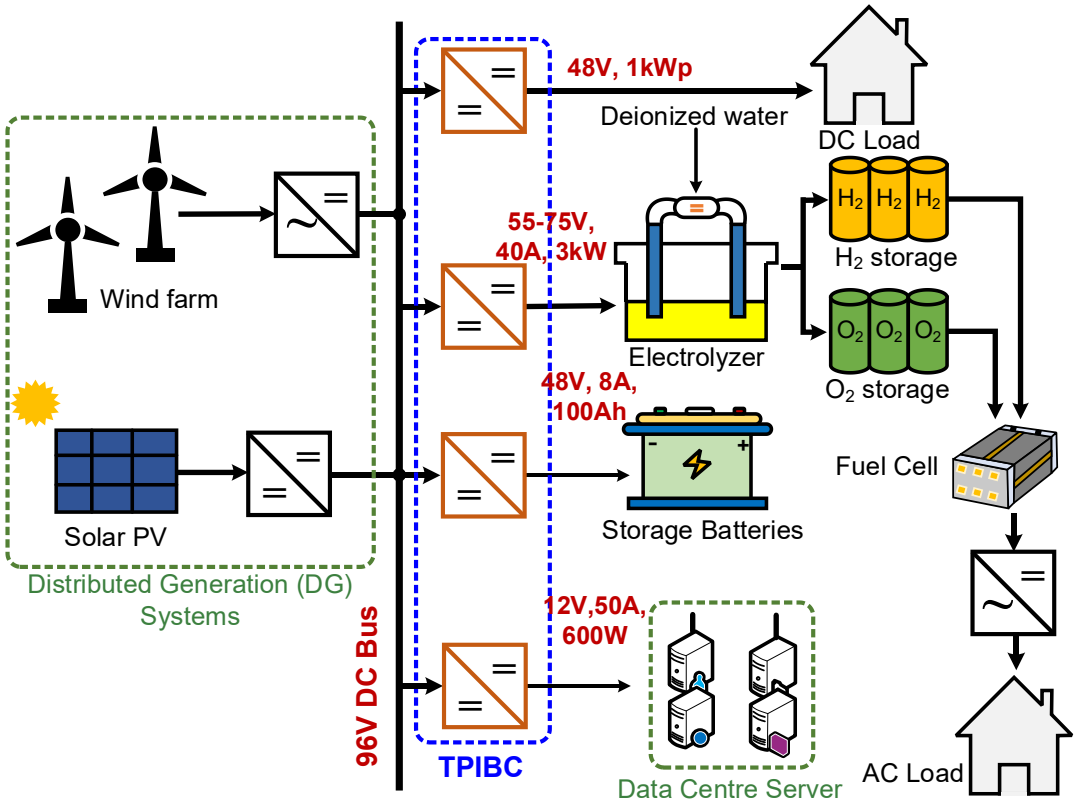


Fig. 1.1 Schematic block diagram of a renewable energy-based DG system connected with constant power, constant current, and constant voltage loads.

Thus, one of the most crucial parts of a DC microgrid is the power electronic converter. Voltage conversion, current and voltage regulation, power flow control, and bidirectional energy transfer between the DC bus and energy storage devices are all made possible by it. Additionally, the converter must continue to function steadily in the face of changes in source voltage, load demand, and energy storage circumstances [10], [11], [18], [19].

DC microgrids are especially appealing for applications like renewable energy systems, data centers, communications systems, EV charging infrastructure, and hydrogen production because of the growing number of DC loads and suppliers. However, the related converters must meet different electrical requirements for these applications. As a result, when designing the controlled converters, the properties of the loads and energy storage devices must be carefully taken into account [15]-[17].

1.3 DC Microgrid Loads and their Electrical Characteristics

The voltage-current characteristics of the loads linked to a DC microgrid can differ significantly as shown in Fig. 1.2. DC loads can be generically categorized as constant-voltage, constant-current, constant-power, and resistive loads from the perspective of power converter modeling and control [20], [21]. Converter operation, current ripple, dynamic response, and system stability are all directly impacted by the properties of the associated load. Because the ripple behavior of high-current interleaved converters depends not only on the duty ratio and converter settings but also on the type of connected load, this consideration becomes more crucial [22], [23].

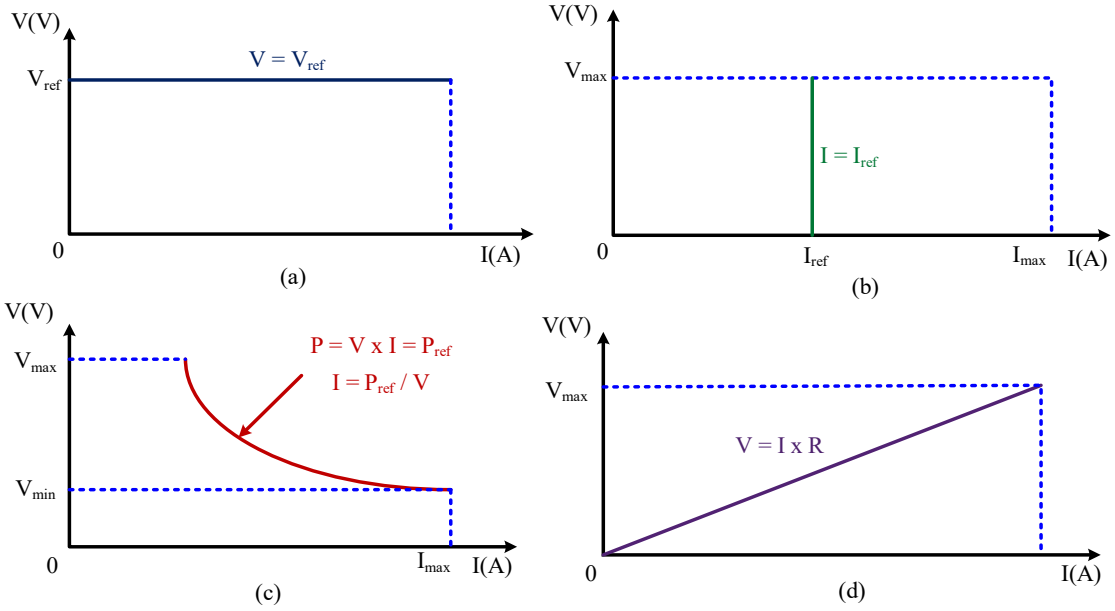


Fig. 1.2 V-I characteristics of common DC load types (a) constant voltage load, (b) constant current load, (c) constant power load, and (d) resistive load.

1.3.1 Constant-Voltage Loads

A constant voltage load throughout its operational range, aims to keep its terminal voltage roughly constant. Properly regulated DC-bus loads and regulated electronic systems are two examples. In spite of changes in input voltage, load demand, and outside disruptions, the power converter serving a constant-voltage load must maintain the necessary voltage. For dependable operation, precise voltage management and sufficient closed-loop stability are crucial.

1.3.2 Constant-Current Loads

A constant current load throughout its operational range, draws roughly the same amount of current. Certain electrochemical loads and battery charging circumstances may show traits of constant-current functioning. For these kinds of applications, the converter needs to precisely control the output current while operating steadily across the necessary voltage range. Because of excessive ripple can increase losses and negatively impact the performance and longevity of the linked energy storage device, it is crucial to take current ripple into account.

1.3.3 Constant-Power Loads

A constant-power load attempts to maintain approximately constant power consumption, expressed as $P = V \times I$ or $I = P / V$ .Therefore, a decrease in the DC-bus voltage results in an increase in the load current. This characteristic produces a negative incremental impedance and can introduce additional challenges in the stability of DC microgrids and their associated power converters. Constant-power behaviour is particularly relevant to regulated electronic loads, data servers, DC power supplies, and tightly controlled power electronic systems. Consequently, the interaction between constant-power loads and converter dynamics must be considered in the design of stable DC power systems**.**

1.3.4 Resistive Loads

For resistive load $I = V / R$ *or* $P = V^2 / R$**.** Resistive loads are commonly used in fundamental converter analysis because of their simple mathematical representation. They are useful for deriving steady-state and small-signal models and for evaluating voltage

and current ripple. The available DC microgrids generally accommodates a combination of various kinds of loads. Thus, converter modeling and performance analyses based on resistive loads only may not completely provide practical operating conditions.

1.3.5 Battery Charging and Discharging as a Dynamic DC Load/Source.

The nature of battery for changing electrical functioning from charging to discharging and vice versa based on the required direction of power flow, they represent a special feature in DC microgrids [11]. During charging, the battery serves as a regulated energy-consuming load; during discharging, it powers the DC bus. The charging and discharging process requires accurate current control and bidirectional power conversion [11]. High charging currents and sudden changes in power consumption can put battery cells under a lot of stress. Furthermore, strong current ripple and multiple high-current charge-discharge cycles may accelerate battery degradation. These characteristics promote the use of hybrid ESSs (HESS), which combine batteries and high-power-density supercapacitors [12], [15].

1.4 ESS for DC Microgrids

The ESS has become an essential part of DC microgrid to create balance between load demand and renewable energy generation. They meet transient power needs, provide energy during times of inadequate generation, and compensates for variations in renewable power generation [15].

1.4.1 Battery ESS (BESS)

Batteries can provide average power demands over extended periods of time because of their comparatively high energy density. Lithium-ion batteries are especially appealing for EVs, DC microgrids, and renewable energy applications because of its high energy density [22]. Batteries, however, have slower electrochemical kinetics and a relatively low power density. Regular high-current charging and discharging can hasten aging by raising thermal and electrochemical stress [23]. As a result, relying solely on batteries to react to sudden, sharp changes in power could shorten their lifespan.

1.4.2 Supercapacitor ESS (SESS)

Supercapacitors have exceptional charge-discharge life cycle, low internal resistance, quick charge-discharge capability, and a very high-power density. They can absorb and supply short-duration transient power because of these qualities [23]. But compared to batteries, supercapacitors have a far lower energy density. As such, they are typically not appropriate for fulfilling long-term energy needs on their own.

1.4.3 Battery–Supercapacitor based ESS (BSCES)

The development of BSCES has been driven by the complimentary features of supercapacitors and batteries. The battery provides the average or low-frequency portion of the load power in a BSCES, while the supercapacitor reacts to sudden, high-frequency power demands [14], [15]. Battery current stress, high-frequency battery current variations, needless charge-discharge cycling, transient response, and possibly battery longevity can all be decreased with such coordinated operation. However, appropriate power electronic converters and control techniques are needed for the successful combination of battery and supercapacitor storage. Bidirectional power flow, DC-bus voltage maintenance, power-sharing coordination, and stability in the face of fluctuations in load demand and renewable generation are all requirements for the converter [22], [23].

1.5 Emerging Applications of DC Microgrids

High-performance DC–DC converters are needed for various kind of applications brought about by the growing use of DC microgrids and renewable energy systems. Among these, data centers, hydrogen electrolyzers, and electric car charging are significantly high-power DC applications [9]-[12].

The need for reliable and powerful EV charging infrastructure has grown dramatically due to the quick electrification of transportation. High power transfer capacity, precise voltage and current control, minimal charging-current ripple, high conversion efficiency, and reliable operation are all necessary for fast-charging systems [10], [11]. The charging converter has a major impact on batteries life, temperature stress and charging efficiency. High-current charging systems thus require converter topologies that can distribute the charging current among multiple semiconductor devices while maintaining low output-current ripple [24], [25]. The dependence on conventional grid electricity can be further

reduced by combining PV power with energy storage devices and renewable-energy-based EV charging stations. However, the intermittent nature of renewable energy raises additional need for energy storage and coordinated power management. The high-current capability, current-sharing features, ripple cancellation, and modular scalability of interleaved converters make them appealing for EV charging [26]-[28]. Additionally, multiport converter (MPC) architectures offer chances to incorporate energy storage devices and renewable energy sources into a single power conversion framework.

It has been widely acknowledged that hydrogen generated from renewable energy sources is a crucial step toward low-carbon energy systems. Electrolyzers often run at high current levels and need controlled DC power. As a result, the DC–DC converter that powers an electrolyzer needs to deliver a high output current with minimal current ripple [29]. The lifespan and functionality of electrochemical systems can be adversely affected by excessive current ripple. Because interleaved buck converter (IBC) divides the total output current throughout several converter phases and can greatly lower the resulting output-current ripple, IBCs are especially appealing for such applications However, the duty ratio and operating region affect an interleaved converter's ripple characteristics. Thus, choosing appropriate operating conditions requires thorough characterization of continuous and discontinuous conduction modes as well as overlapping and non-overlapping working zones [30].

Numerous electronic loads in modern data centers and high-performance computer systems necessitate dependable and superior DC power. Energy efficiency can be increased and needless power conversion stages can be eliminated with direct DC distribution. Over certain operational ranges, data servers and regulated electronic systems may display constant-power characteristics. Because of the negative incremental impedance connected to constant-power operation, their integration into DC microgrids may result in extra stability issue [20]. As a result, dynamic interactions between converters, DC buses, and constant-power loads must be carefully taken into account when designing power converters for data center applications.

1.6 DC–DC Power Converters for DC Microgrid Applications

The DC–DC converters are essential parts of DC microgrids because distributed energy sources, energy storage devices, and loads typically operate at various voltage levels. The converter allows controlled power transfer between various system components and offers the necessary voltage conversion. A DC–DC converter can carry out voltage step-up, step-down, bidirectional energy conversion, galvanic isolation, or multiport power management, depending on the application. DC–DC converters can broadly be classified into non-isolated, isolated, and MPC configurations [31].

1.6.1 Non-Isolated DC–DC Converters

Non-isolated DC-DC converters often offer a compact size, high power density, and relatively easy control because they do not use a high-frequency transformer. Buck, boost, buck–boost shown in Fig. 1.3 and their derivative configurations are examples of common topologies. Applications which need high-current step-down conversion are especially well suited for the buck converter. Nevertheless, a traditional single-phase buck converter encounters increased semiconductor current stress, higher current ripple, increased thermal stress, and increased passive component needs as the output current rises. The usage of *n*-phase interleaved converter topologies is strongly motivated by these constraints.

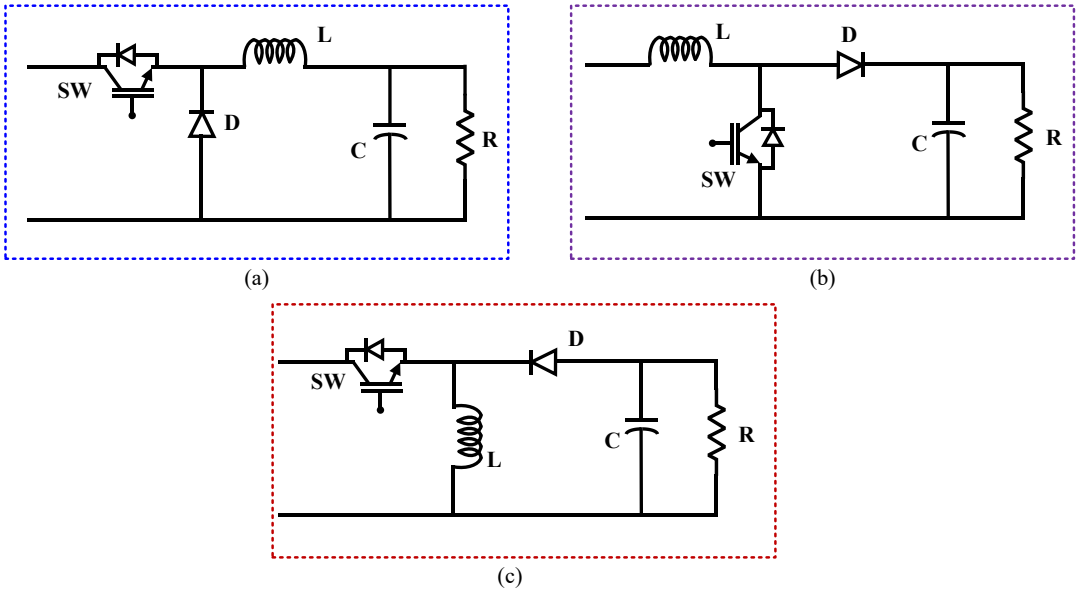


Fig. 1.3 Non-isolated DC-DC converter topology (a) Buck, (b) Boost, and (c) Buck-boost.

1.6.2 Isolated DC–DC Converters

High-frequency transformers (HFT) are used in isolated DC–DC converters to offer adjustable voltage conversion ratios and galvanic isolation. Flyback, forward, full-bridge shown in Fig. 1.4, half-bridge, phase-shifted full-bridge, and resonant converters are examples of common isolated DC-DC converter topologies. As switching frequency and power levels rise, hard-switched converters may encounter higher switching losses, Electromagnetic Interference (EMI),, and semiconductor thermal stress. By using the interaction between inductive and capacitive components to create soft-switching circumstances, resonant converters overcome some of these drawbacks.

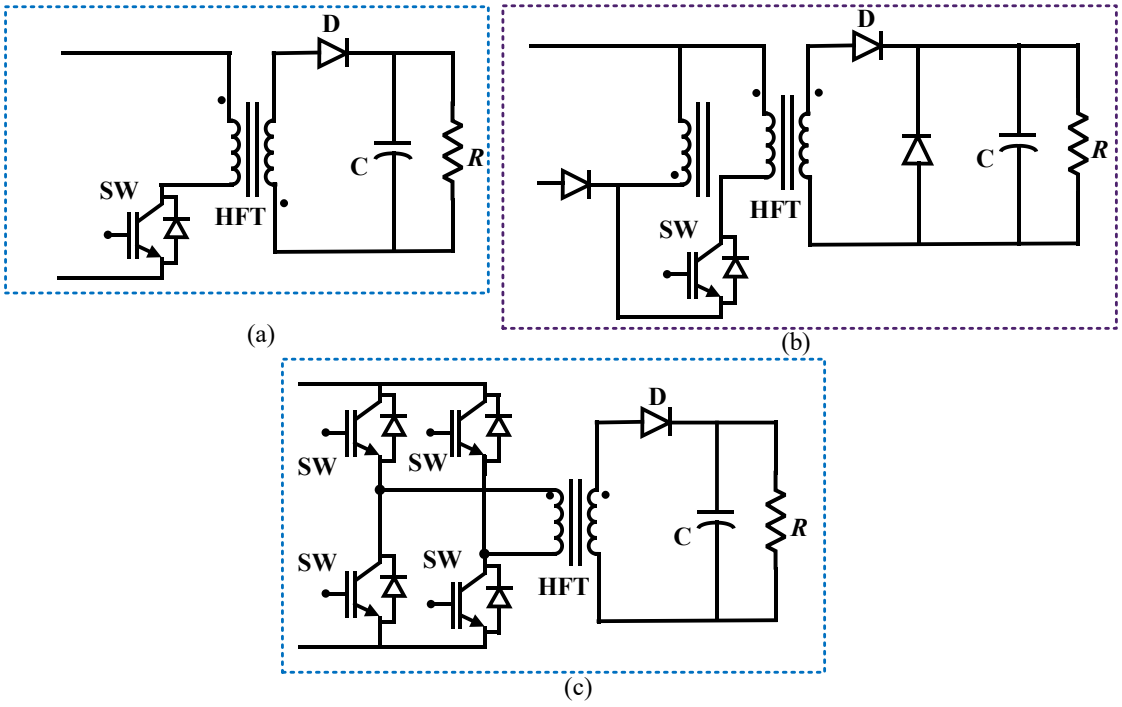


Fig. 1.4 Isolated DC-DC converter topology (a) Flyback, (b) Forward, and (c) Full bridge.

1.6.3 Multiport DC–DC Converters

A single power conversion interface for many sources, storage devices, and loads is offered by multiport DC–DC converters. When compared to systems that use different converters for every energy source, multiport architectures can lower: the quantity of switching devices, the number of power conversion stages, the number of components, the size and volume of the system, and conversion losses [31]. For integrating solar power, batteries, supercapacitors, and DC loads, MPCs are appealing. Nevertheless, extra

difficulties with power-flow coordination, converter modeling, control interaction, and stability are brought about due to the existence of multiple ports. When bidirectional energy transfer between several storage devices and the shared DC bus is necessary, these difficulties become more serious.

1.7 Interleaved DC–DC Converters for High-Current Applications

In high-current applications, the IBCs have become a viable remedy for the drawbacks of Classical Buck Converter (CBC). Multiple parallel converter phases operating at the same switching frequency with the proper phase displacement between respective parallel phases. The optimal phase displacement, θ of the switching signals for an *n*-phase interleaved converter is $\theta = 360^{0} / n$. Ripple components produced by particular converter branches are partially or totally cancelled by the phase-shifted operation. Consequently, the resulting input and output current ripple can be significantly decreased [24], [25].

The principal advantages of interleaving include reduced input and output current ripple, improved current sharing among converter phases, reduced current stress on individual semiconductor devices, improved thermal distribution, increased effective ripple frequency, reduced filter component requirements, improved transient performance and modular scalability and increased power capability [25]. These advantages make IBCs attractive for renewable energy interfaces, battery charging systems, EV charging, Voltage Regulator Modules (VRMs), electrolyzers, data centers, telecommunication systems, and other high-current applications. However, the number of phases and the duty ratio have a significant impact on an interleaved converter's performance. Individual phase currents may operate in non-overlapping intervals or overlap, depending on the operational duty ratio. As a result, the output-current ripple that results are not constant over the whole duty-ratio range [32]. This duty-ratio-dependent behavior is particularly important for high-current charging applications, where the converter may need to operate over a wide input-voltage range while maintaining a regulated output voltage [33]. Therefore, comprehensive assessment of interleaved converters across different operating regions and generalized modeling are essential for the optimal converter design.

1.8 Influence of Circuit Parasitics on Converter Performance

The practical power converters having several non-ideal components cannot be ignored, despite the fact that ideal converter models are useful for understanding fundamental operating principles. These include source resistance, inductor winding resistance, capacitor equivalent series resistance (ESR), diode forward voltage drops, semiconductor switch voltage drops, parasitic inductances and capacitances. These parasitic elements affect the converter's voltage conversion ratio, conduction losses, efficiency, damping, frequency response, transient behavior, and closed-loop stability [34].

The impact of parasitic elements should be taken into account in high-current applications. Even relatively small parasitic resistances can cause large voltage drops and conduction losses when high currents flow through the converter. Additionally, parasitic components affect the individual phase currents along with changing current sharing and affect ripple cancellation in interleaved converters. The ESR of inductors and capacitors can alter the damping characteristics of the converter, while semiconductor switch and diode voltage drops impact the effective conversion ratio.

Therefore, the behavior of real-world converters may not be correctly represented by mathematical models created just under ideal assumptions. Accurately forecasting steady-state and dynamic behavior and creating controllers that continue to function well under realistic operating conditions depend on the inclusion of pertinent parasitic components in the converter model [34].

1.9 Research Motivation and Problem Statement

Many renewable energy sources, energy storage devices, and a variety of electrical loads operating under changing loading and environmental circumstances are common components of modern energy systems. As a result, the effectiveness, controllability, power density, and dependability of the related DC-DC converters have a significant impact on these systems' performance. Conventional single-phase converters have various practical challenges due to the growing need for high-current and high-power applications. Large current stress, bulky passive components, increased output current ripple, and challenging thermal control are all experienced by semiconductor switches [33]. These restrictions lower converter efficiency, raise system costs, and lower overall

dependability. As a result, during the past 20 years, converter topologies that can distribute current over several power processing routes have drawn a lot of research interest.

One of the best ways to get around these restrictions is to use interleaved DC-DC converters. Interleaving reduces input and output current ripple through ripple cancellation while distributing the load current among many branches by running multiple identical converter phases in parallel with evenly phase-shifted switching signals [35]. Smaller passive filter components can be used without compromising performance because the effective ripple frequency rises in direct proportion to the number of phases. As a result, interleaved converters perform better than traditional single-phase converters in terms of efficiency, thermal distribution, transient responsiveness, EMI and power density. Even while interleaving significantly enhances converter performance, a number of less-than-ideal aspects still have an impact on practical implementations. The ESR of inductors and capacitors, conduction losses, source resistance, and voltage drop in switching devices are examples of circuit parasitics that have a substantial impact on steady-state operation, converter efficiency, transient responsiveness, and closed-loop stability [36]. Therefore, the mathematical modeling considering the actual parasitic value of components is essential for realistic converter analysis and subsequent designing of converter.

The IBCs are suitable for high current and low voltage output applications with reduced output ripple current [37]. However, the operation of IBC at particular duty ratio in overlapping and non-overlapping mode under continuous conduction mode (CCM) and discontinuous conduction mode (DCM) for optimum output with low ripple value is a matter of investigation and attention.

In addition to high-current interleaved converters, the EV charging system and renewable energy systems have raised the interest in resonant converter technology. Unlike the pulse-width-modulated converters, which have mostly hard switching operation, resonant converters utilize the intrinsic resonance between inductive and capacitive components to accomplish the soft switching as the zero-voltage switching (ZVS) and zero-current switching (ZCS) greatly reduce switching losses, device stress, and EMI [38]. These resonant converters are attractive for high-frequency and high-power charging applications to justify the installation cost. Furthermore, many battery packs can

now be charged simultaneously while maintaining balanced current sharing and high conversion efficiency by optimal designing of interleaved multiport resonant converters.

Advanced and reliable energy storage technologies are becoming more and more necessary as renewable energy source have started occupying place in various energy sectors to cater the energy requirement. The lithium-ion batteries have gained interest in industrial and EV sector for having a high energy density; however, the lithium-ion batteries degrade more quickly when exposed to repeated high-current transients. Thus, a high-power density is required to be used along with the battery cater the high transient current. Supercapacitors is a better choice for complementing the battery as have a comparatively low energy density but a very high-power density and outstanding cycling capabilities. Effective power sharing, better transient response, longer battery life, and increased system reliability [15], [22] are all made possible by integrating these complimentary storage technologies into a BSCES.

The implementation of BSCES require multiple converters as proposed in previous literatures. However, multiple converter implementation increases the installation cost and control complexity increases. Therefore, a MPC topology that can control power flow between batteries, supercapacitors, renewable energy sources, and DC loads is required. Compared to conventional multi-stage converter architectures, used for conversion of voltage for various equipment, MPCs decrease the number of components, limit conversion stages, boost efficiency, and simplify the overall system architecture. However, the increased interaction between multiple energy ports makes converter modeling and controller design much more difficult, requiring sophisticated mathematical models and reliable control strategies that can sustain stable operation under variable operating conditions and parameter uncertainties [15].

The expected steady state behavior of the converter is deviated due to change in component condition and intrinsic parasitic values with change in temperature and other working conditions causes significant difficulty in the practical application of converters. The frequent power converter performance degradation is the outcome of traditional controller design that is dependent on nominal system characteristics when converter parameters deviate from their nominal values. Robust control techniques that ensure stability over a certain range of uncertainty in the system characteristics are essential for

reliable operation in real-time applications Kharitonov's theorem [39] with uncertainty analysis-based frequency-domain design approaches provide better means to construct controllers that retain adequate stability margins under realistic operating conditions.

Through the methodical creation of sophisticated converter topologies, thorough mathematical modeling approaches, and reliable controller design processes, the research described in this thesis tackles these issues. The article examines how operational duty ratio affects converter performance under various conduction areas, starting with generalized modeling of *n*-phase IBCs with circuit parasitics. Interleaved multiport resonant converters that are appropriate for charging infrastructure are then created and examined. Building on these advancements, a unique four-port DC-DC converter that combines battery storage, supercapacitor storage, and PV generating is suggested for hybrid energy storage applications. In order to guarantee dependable converter operation despite parameter uncertainties, robust decoupled controller design techniques based on state-space modeling, frequency-domain analysis, and Kharitonov's theorem are finally established.

The presented research contributes toward the systematic development of high-efficiency, high-power-density, and dependable power conversion systems that are appropriate for novel applications such as DC microgrids, hybrid energy storage (HES) systems, renewable energy integration, and EV charging stations.

1.10 Research Objectives

The primary objective of this research is to develop and investigate advanced interleaved and multiport DC–DC converter architectures and control strategies for renewable energy systems, high-current charging infrastructure, and battery-supercapacitor hybrid energy storage applications.

The main objectives of the thesis are described as follows:

- To develop and characterize interleaved power converters considering parasitic effects for battery charging and discharging applications.
- To investigate the effects of duty ratio and operating regions on the performance of interleaved converters and identify optimal operating conditions.
- To develop mathematical models of multiport battery-supercapacitor power conversion systems and analyze their dynamics, stability, and power-sharing behavior.

- ❖ To design and validate control strategies for battery-supercapacitor HES systems to achieve stable operation, effective power management, and enhanced dynamic performance.

1.11 Scope of the Research

The research methodology adopted in this thesis includes theoretical analysis, converter topology building, mathematical modeling, controller design, simulation studies and experimental validation. A hierarchical foundation for the development of cutting-edge DC-DC converters for renewable energy and BSCES based applications is established by the adopted methodology. Further each chapter has its own importance for implementation of power converter for various different applications which guarantees that each stage of the research provides the necessary foundation for the renewable energy-based power converter applications.

A detailed assessment of the existing literature on interleaved DC-DC converters, MPC topologies, operating-region analysis, generalized converter modeling, HES systems, and applicable control algorithms was the first step in the research process. The identification of current research gaps in the areas of simplified converter designs, generalized mathematical modeling, converter operating-region characterization and controller design was made possible by this review. The problem statement and study objectives were developed based on these observations.

The first approach was creation of a generalized state-space averaged mathematical model for an *n*-phase IBC which was the main goal of the technical investigation's initial effort. In order to effectively depict converter dynamics under realistic operating conditions, the model integrates the circuit parasitic features of the components of converter. After establishing the various applicable converters basic operational characteristics through steady-state analysis, control-oriented transfer functions appropriate for controller design and stability analysis were obtained using small-signal linearization.

The second step was to review the characteristics of three-phase IBC (TPIBC) under different operating conditions. Analytical investigations were carried out for both non-overlapping and overlapping operating regions in CCM and DCM. The effect of change in duty ratio and operating region on current ripple, converter dynamics, voltage

regulation, and system performance was systematically evaluated. The worked out analytical framework presents the generalized design guidelines for IBCs operating under practical conditions.

The third stage concentrated on creating sophisticated converter topologies for renewable energy applications, building on the generalized converter concept. In order to increase conversion efficiency through soft-switching operation, lower switching losses, and improve current sharing among converter phases, an interleaved multiport resonant DC-DC converter was first created. In order to combine PV generation, battery energy storage, supercapacitor energy storage, and a regulated DC bus into a single converter structure, a unique four-port DC-DC converter was later created. The suggested converter architecture facilitates coordinated bidirectional power flow among several energy sources, lowers the number of components, and increases power density.

The development of the controller for the suggested HES system was the focus of the next study. Using frequency-domain approaches, a decoupled proportional-integral (PI) control scheme was created to assign high-frequency transient power to the supercapacitor and low-frequency power changes to the battery. Converter uncertainties were included in the mathematical model to guarantee dependable operation under realistic parameter variations, and Kharitonov's uncertainty theorem was used to identify robust controller gain regions that could maintain closed-loop stability for all allowable parameter variations.

To assess both steady-state and dynamic performance, the suggested mathematical models, for various converter topologies, with and without control strategy were implemented in the MATLAB simulation software. Under a variety of operating situations, such as source fluctuations, load disturbances, and parameter uncertainties, extensive simulation studies were carried out. The various performance criteria inclusive of the converter efficiency, voltage control, current ripple, transient responsiveness, and power-sharing capabilities were analyzed and compared with conventional converter topologies in order to highlight the advantages of the proposed methods.

Lastly, laboratory-scale hardware implementations were used to experimentally validate the various interleaved converter prototypes and with and without control algorithms. Theoretical predictions and simulation findings were contrasted with

experimental measurements of converter voltage, current, efficiency, transient responsiveness, and power-sharing performance. The strong agreement between analytical, modeling, and experimental studies shows that the established converter topologies and robust control method are practically applicable for renewable energy and HES applications. It also validates the validity of the suggested models.

1.12 Major Contributions of the Thesis

The following describes the thesis main contributions to achieving the aforementioned objectives:

1. The development of a generalized mathematical model for *n*-phase IBC having the circuit parasitic components and its effect has been carried out. It offers more accurate representation of practical converters behaviour than previous ideal converter models because of consideration of effects of passive component resistances and converter non-idealities. The generalized state-space model can be utilized for describing any number of converter phases and hence forms the basis for steady-state, dynamic, and small-signal investigations.
2. The performance of IBCs in various operating regions has been thoroughly characterized. The behaviour of the converter has been examined analytically for both continuous and discontinuous conduction modes, as well as non-overlapping and overlapping switching regions. Duty ratio's impact on current ripple, current sharing, output voltage characteristics, converter efficiency, and operational bounds has been methodically determined, offering helpful design recommendations for real-world multiphase converter systems.
3. The unidirectional multiport resonant and bidirectional interleaved multiport resonant DC-DC converter has been developed for infrastructure related to charging and discharging such as EV charging station. The combination of interleaved and multiport feature with fast switching semiconductors operating at high frequency (HF) helps to achieve lower current ripple, better current sharing, soft-switching operation, and increased power density. In addition to lowering the number of HF transformers, the converter architecture allows for modular expansion for multiport charging applications.

4. A non-isolated multiport DC–DC converter having four ports for incorporating PV source, BESS system, SESS and fluctuating DC load. The suggested converter maintains self-governing solar power extraction while facilitating coordinated bidirectional power flow between the battery, supercapacitor, and DC bus. In comparison to conventional numerous converter setups for same application, the suggested topology minimizes conversion stages, lowers hardware complexity, and increases the system efficiency by combining various power ports into a single converter structure.
5. The mathematical modeling of suggested MPC has been done using control-oriented state-space averaged and small-signal approaches. The dynamic interactions between the solar source, battery, supercapacitor, and DC bus under various operating modes for various states of operation are accurately described by these models. The provided analytical methodology offers a methodical basis for controller synthesis, stability assessment, and converter analysis.
6. A controller design has been developed for the four-port DC-DC converter for battery-supercapacitor-based ESSs (FPDCBSS). The controller employs frequency-segregation based power sharing, in which the battery responds to the load's low-frequency power demand while the supercapacitor compensates for relevant high-frequency power transient requirements. This coordinated control method extends battery service life time and also reducing battery current stress, enhancing transient response, and regulating DC-bus voltage.
7. The recommended FPDCBSS structure and controller designs are validated by simulation modeling and hardware implementation. The hardware results demonstrate how well the suggested converters and control strategies reduce implementation costs when compared to the classical method, including increased efficiency, stable power sharing, robust operation under parameter uncertainties, and extended battery lifetime for BSCES. They also validate the accuracy of the developed mathematical models that are steady state and small signal modes.

The chronological description discusses about the contribution of the work done for a comprehensive framework for the design, modeling, analysis, and implementation of various appropriate DC-DC converters for various applications including EV charging

systems, battery charging infrastructure, BSCES applications, renewable energy integration, and DC microgrids. The various proposed approaches provide useful design methods for high-efficiency, high-power-density, and robust power electronic conversion systems in addition to the highlighted problems with conventional power converter topologies.

1.13 Organization of the Thesis

The thesis is organized into eight chapters, each of which contains the following information:

Chapter 1 provides an overview of the proposed study along with the background and reasons why various DC-DC converter types are required in hybrid energy storage and renewable energy applications. It highlights the importance of interleaved converter technology, identifies existing research gaps, formulates the issue statement, outlines the objectives and scope of the study, explains the research process, highlights the main contributions of the thesis, and provides the thesis with a general framework.

Chapter 2 presents the published literature on interleaved DC-DC converters, ripple reduction methods, generalized converter modeling, resonant converter technologies, hybrid battery-supercapacitor ESSs, MPC architectures, and control design strategies being thoroughly reviewed. The chapter establishes the reason for the suggested work provided in the next chapters, critically evaluates the existing research, and points out current limits.

Chapter 3 provides with generalized mathematical model of an *n*-phase IBC with applicable circuit parasitic components. Generalized converter equations and control-oriented transfer functions are derived using state-space averaged modeling, steady-state analysis, and small-signal modeling techniques. Subsequent converter analysis and controller design are built upon the given analytical framework.

Chapter 4 examines the TPIBC working properties under various operating situations. Both non-overlapping and overlapping working regions in DCM and CCM are thoroughly characterized. Generalized design guidelines for multiphase interleaved converters are provided by an analytical evaluation of the impact of operating area on TPIBC dynamics, ripple characteristics, and overall performance.

Chapter 5 presents an interleaved multiport resonant DC-DC converter for renewable energy applications being developed and analyzed. In order to improve conversion efficiency, lower switching losses, improve current sharing, and boost power density, the suggested converter architecture combines the benefits of interleaving and resonant power conversion. The converter performance is assessed using mathematical analysis, modeling studies, and experimental validation.

Chapter 6 presents a state of art four-port DC-DC converter for battery-supercapacitor-based ESSs. The converter combines the DC bus, battery storage, supercapacitor storage, and PV generation into a single converter architecture. To illustrate the efficacy of the suggested converter, comprehensive operating principles, mathematical modeling, power-flow analysis, simulation results, and experimental verification are provided.

Chapter 7 proposes a reliable decoupled PI control approach for the suggested battery supercapacitor-based ESS. Battery and supercapacitor power sharing is coordinated using frequency-domain power allocation, and resilient controller gain regions that can sustain closed-loop stability under parameter uncertainties are found using Kharitonov's uncertainty theorem. Simulation and experimental research under a range of operating situations are used to validate the suggested controller.

Chapter 8 presents the conclusions of the thesis and outlines potential directions for future research.

Chapter 2

Literature Review

2.1 Introduction

The significance of modern power electronic converter systems has grown drastically due to the quick growth of renewable energy sources, EVs, energy storage technologies, and DC-based electrical loads. In order to increase energy efficiency, decrease conversion stages, and make it easier to integrate energy storage with increasing demand for DC loads [4]. DG based on PV sources, wind energy, fuel-cell, and other renewable energy sources is increasingly being integrated with DC microgrids. DC-DC converters act as the primary interface in these systems between loads, storage devices, and renewable energy sources [6].

Power converters with high efficiency, high power density, low input and output current ripple, reduced semiconductor stress, and reliable operation under various operating conditions are required due to the growing demand for high-power EV charging, hydrogen production through electrolyzers, data centers, and other high-power DC applications [9], [10]. The high-power application using CBC has significant current stress and increasing conduction losses. IBC have gained attention for its phase-shifted switching operation can minimize the resulting input and output current ripple. However, the number of phases, duty ratio, switching method, operating region, and circuit factors have a significant impact on interleaving benefits. The steady-state and dynamic properties of the converter are further changed by the existence of parasitic elements [34]. Reliable design and control thus depend on precise modeling and characterization of realistic interleaved converters.

Multiport and bidirectional DC-DC converters have become come up with the options for combining various energy sources and storage devices together for various applications. Specifically, the combination of battery and supercapacitor energy storage offers complimentary features: the supercapacitor gives high power density and quick dynamic response, while the battery delivers high energy density [22], [23]. Therefore, to

coordinate power flow across renewable sources, batteries, supercapacitors, and DC loads, appropriate power electronic interfaces are needed.

The main research in this thesis progress with examination of individual converter features to the creation and management of integrated multiport energy conversion systems. The characteristics and modeling of interleaved converters, operating-region characterization, ripple current and current-sharing analysis, resonant and soft-switching conversion system, MPC topologies, and battery-supercapacitor HESS devices are major research theme.

2.2 Distributed Generation and DC Microgrid Applications

The growing use of renewable energy sources has made DG a crucial component of modern electrical power systems. Decentralized energy generation has been made possible using PV systems, wind energy systems, fuel cells, and other distributed energy resources, which also lowers transmission losses.

Power electronic interfaces are necessary for the integration of DG systems in order to control power flow, regulate voltage, and preserve power quality. Giri et al. used a Lorentzian norm adaptive filter to study power quality enhancement in a DG system based on a solitary squirrel-cage induction generator [1]. Their research shows how crucial sophisticated control and filtering methods are for preserving power quality in dynamic and nonlinear operational environments. DC microgrid development has also been aided by the growing use of DG based on renewable energy. When the system has a lot of DC sources, storage devices, and DC loads, DC microgrids are very appealing. DC microgrids can lower the number of conversion stages related to DC loads and renewable energy sources when compared to AC systems.

Meng *et al.* presented a review of control strategies for DC microgrids and discussed the challenges associated with voltage regulation, current sharing, power management, and system stability [17]. Ye et al. examined low-frequency resonance suppression in a DC microgrid enabled by DAB converters and showed that the stability of the entire DC system is significantly influenced by the terminal characteristics of integrated converters [40].

Another significant reason propelling the growth of DC power infrastructure is the growing electrification of transportation. Infrastructure for charging EVs is a major

obstacle to their adoption in India, according to Nair et al. [2]. Therefore, high-performance power electronic converters that can handle large charging power while keeping acceptable efficiency and power quality are necessary for the development of scalable and efficient charging infrastructure.

An enhanced power-quality onboard integrated charger with less switching stress was proposed by Gupta et al. [3]. The study emphasizes how crucial it is to lower semiconductor stress in EV charging applications while preserving the necessary power quality. DC microgrids are becoming more and more important for data centers, hydrogen generation, and other high-power DC uses in addition to EV charging. Converters that can handle high current with minimal ripple and good reliability are needed for these applications. Investigating interleaved converter architectures is strongly motivated by this demand.

2.3 DC–DC Power Conversion for High-Power Applications

DC–DC converters are essential parts of ESSs, DC microgrids, EV charging systems, and renewable energy systems. DC–DC converters can be generically classified as either isolated or non-isolated, depending on the necessary isolation and voltage conversion ratio. Non-isolated converters such as buck, boost, and buck–boost converters are generally characterized by relatively simple structures and high efficiency. However, conventional single-phase converters can experience high current stress at elevated power levels.

When low-voltage, high-current loads are supplied via a high-voltage DC bus, high step-down conversion is very crucial. As a result, several high step-down converter designs have been proposed. A transformer less interleaved high step-down conversion-ratio converter with minimal switch voltage stress was created by Pan et al. [41]. A high-efficiency non-isolated converter with an extremely high step-down conversion ratio was also studied by Kirshenboim and Peretz [42].

High step-up converters are frequently needed for renewable energy applications in order to connect low-voltage PV sources to high-voltage DC busses. For distributed PV generation, Li et al. looked into an interleaved high step-up zero-voltage-transition converter with an integrated transformer voltage-doubler cell [43].

These investigations show that modified converter structures can achieve high step-up and high step-down conversion. However, the inclusion of additional switching devices, coupled inductors, or auxiliary components may result in a more complex circuit.

In order that the storage device must both absorb and deliver energy, bidirectional conversion is also crucial in ESSs. A multiphase, modular, bidirectional, triple-voltage DC–DC converter for fuel cell and hybrid car applications was proposed by Su and Tang [44]. These structures show how bidirectional conversion can be used for energy storage and vehicle applications.

Therefore, in addition to voltage gain, efficiency, current ripple, switching losses, device stress, power density, and control complexity must all be taken into account when choosing a converter topology.

2.4 Interleaved DC–DC Converter Topologies

The main advantages of interleaving include current sharing among semiconductor devices, reduced input-current ripple, reduced output-current ripple, lower current stress per phase, improved thermal distribution, increased effective ripple frequency, reduced filter requirements and improved scalability for high-power operation. These characteristics have made interleaved converters attractive for battery chargers, EV charging systems, renewable energy interfaces, electrolyzers, and DC microgrids.

The switching strategy for interleaved converter has a direct influence on current sharing and ripple cancellation. Saito et al. investigated IBCs based on winner-take-all switching [33]. The work demonstrates the importance of appropriate switching control in achieving desired phase operation. Unequal phase currents in interleaved converters can lead to thermal imbalance and put more strain on individual semiconductor components. For reliable operation, current-sharing control is consequently important.

A current-sharing approach for a three-phase series-capacitor buck converter operating across a broad output voltage range was examined by Chen et al. [45]. The significance of maintaining balanced phase currents when converter operation extends over a broad voltage range is demonstrated by their study.

When practical parasitic components are taken into account, the problem of current sharing becomes more important because variations in parasitic resistance and inductance might result in uneven current distribution.

The IBC is one of the most widely studied topologies for high-current step-down applications. Lee et al. investigated an IBC with low switching losses and an improved step-down conversion ratio [46]. The proposed approach demonstrates the possibility of improving both conversion ratio and switching performance through topology modification.

IBC with continuous input current, incredibly low output-current ripple, minimal switching losses, and an enhanced step-down conversion ratio was proposed by Esteki et al. [32]. The study shows how IBCs can be used in applications that need high current and stringent ripple requirements. A high-efficiency interleaved ultra-high step-down DC–DC converter with extremely minimal output current ripple was proposed by Amiri and Farzanehfard [47]. Applications where a high-voltage DC bus must feed low-voltage loads can benefit from such high step-down topologies.

These advancements demonstrate that IBCs can produce better voltage and current characteristics. Nevertheless, a lot of suggested topologies either involve additional components or complex switching techniques.

An enhanced interleaved buck-boost converter was modeled, analyzed, and implemented by Rana et al. [48]. Such topologies are appealing for variable-voltage renewable energy sources and storage systems because they can accomplish both step-up and step-down conversion. For distributed PV generation, Li et al. suggested an interleaved high step-up ZVT converter with an integrated transformer voltage-doubler cell [43]. This paper shows how to attain high voltage (HV) gain while enhancing converter performance by using interleaving and soft-switching approaches.

In PV systems, where the source voltage can be significantly lower than the necessary DC-bus voltage, the development of high-gain interleaved converters is very pertinent. High-gain converters, however, have the potential to increase circulating current, voltage stress, and control complexity. Converter selection must therefore take into account all operational requirements rather than just voltage gain.

2.5 Ripple Reduction and Current-Sharing Techniques

When designing high-current power converters, current ripple is a crucial factor. Conduction losses, EMI, capacitor stress, and battery current stress are all increased by excessive ripple.

Analytical time-domain expression for the net ripple generated by parallel interleaved converters were obtained by Johnson and Krein [49]. Their research focuses on the connection between phase operation and generated current ripple. In asymmetric interleaved multiphase DC–DC converters, Schuck and Podgurski studied ripple minimization using harmonic elimination [50]. Beyond traditional interleaving, the study shows that proper phase and switching arrangement can further reduce ripple. For high-power applications, Lu et al. studied coupled inductors in an interleaved multiphase three-level DC–DC converter [51]. Although their design adds more complexity, coupled inductors can enhance magnetic use and offer extra ripple reduction.

A passive filter building block for input or output current ripple cancellation was proposed by Nag et al. [52]. These methods show that phase interleaving can be enhanced by passive networks to further minimize current ripple. Active ripple cancellation methods for spur reduction in DC–DC converters were studied by Liu, Liao and Kuo [53]. Although it may make control more complicated, active ripple cancellation can improve ripple performance.

The literature therefore indicates that ripple reduction can be achieved through phase-shifted interleaving, harmonic elimination, coupled magnetic components, passive ripple cancellation; and active ripple cancellation. However, ripple cancellation is strongly dependent on the duty ratio and operating region. This observation motivates the detailed operating-region analysis developed in the present thesis.

2.6 Modeling of DC–DC and Interleaved Power Converter

Maksimovic *et al.* provided a comprehensive discussion of modeling and simulation methods for power electronic converters [54]. Davoudi *et al.* investigated numerical state-space average-value modeling of pulse width modulation (PWM) DC–DC converters operating in both continuous and discontinuous conduction modes [5].

Pavlovic *et al.* developed simplified averaged models suitable for controller design and microgrid simulation [55]. Such models are computationally efficient and useful for

system-level studies. However, conventional averaged models generally neglect switching-frequency dynamics and may not accurately represent behavior near switching transitions.

For multiphase interleaved buck, boost, and buck–boost converters, including transient, steady-state, and switching dynamics, Azer and Emadi created a generalized state-space average model [56]. Because the number of phases directly affects phase interactions, dynamic response, and current ripple, generalized modeling approaches are crucial. A generalized model for an n-phase converter offers a methodical framework for assessing converter performance without creating an entirely separate model for every phase number.

The impacts of digital control and switching might not be adequately captured by continuous-time averaged models. A general method for sampled-data modeling of power electronic circuits was created by Verghese et al. [57]. When the controller is implemented digitally, discrete-time models are especially crucial since converter stability is impacted by sampling, computation delay, and modulation. Discrete-time maps for the analysis of bifurcations and chaos in DC–DC converters were studied by Di Bernardo and Vasca [58]. Their research shows that discrete-time and nonlinear phenomena could play a significant role in converter operation. A unified state-space model of constant-frequency current-mode-controlled power converters running in CCM was discussed by Smithson and Williamson [59]. M. Kumar and R. Gupta investigated stability and sensitivity analysis of uniformly sampled DC–DC converters considering circuit parasitics [34]. Their work demonstrates that parasitic components can significantly affect converter stability and sensitivity.

2.7 Soft-Switching Resonant DC–DC Converters

High-frequency operation is attractive because it reduces the size of passive components and boosts power density. Hard switching, however, raises EMI and switching losses. Soft-switching techniques overcome these limitations by achieving ZVS or ZCS.

Bhat studied the design and analysis of resonant converters of the LCL type [60]. An LCL resonant converter with PWM control was further studied by Raju and Doradla [61].

A design process for optimizing an LLC resonant converter for wide output voltage range operating was shown by Beiranvand et al. [62].

Applications requiring high switching frequency and efficiency are especially drawing attention to resonant converters. However, their voltage gain is highly dependent on resonant-tank settings and switching frequency, making control more difficult. A bidirectional soft-switching series-resonant converter for DC microgrid ESSs was presented by Wu et al. [63]. A bidirectional resonant DC–DC converter appropriate for a broad voltage gain range was studied by Shen et al. [64]. A bidirectional series-resonant DC/DC converter that is extremely effective across a broad battery voltage range was presented by Bai et al. [28]. Estima and Cardoso analyzed the efficiency of drivetrain topologies for electric and hybrid vehicles [65]. Onar, Kobayashi, and Khaligh proposed a fully directional universal power electronic interface for EV, HEV, and PHEV applications [66].

These investigations show that resonant conversion is appropriate for energy storage uses. However, it is possible to accomplish soft switching, current sharing, and ripple reduction all at once by combining resonant conversion with interleaving.

2.8 Multiport and Bidirectional DC–DC Converters

MPCs provide a means of integrating multiple sources, storage devices, and loads through a common power conversion system. Compared with independent converters, multiport architectures can reduce, converter count, passive components, conversion stages, system volume and overall cost. However, multiport systems are dynamically coupled, and changes in one port may influence the operation of other ports.

S. K. Mishra *et al.* investigated a switched-boost-action-based MPC [67]. O. Ray *et al.* proposed an integrated dual-output converter [68]. Vettuparambil *et al.* developed a MPC interfacing solar PV modules and energy storage with a DC microgrid [69]. This work is particularly relevant to renewable-energy-based DC microgrids. Aravind *et al.* reviewed multiport non-isolated DC–DC converters and their control techniques for renewable-energy applications [31]. The review demonstrates the increasing importance of multiport architectures in renewable energy systems.

Surulivel *et al.* proposed a four-port converter with bidirectional ports and a common ground for PV hybrid ESSs [70]. More recently, Mondal *et al.* investigated a three-phase five-port partially isolated DC–DC converter for DC-powered commercial buildings [71], while Murugan *et al.* developed a high step-down bidirectional MPC [72].

2.9 Battery Supercapacitor based ESSs

Battery and supercapacitor technologies have complementary characteristics. Batteries offer high energy density, relatively high energy capacity and suitability for long-duration energy supply whereas supercapacitors offer high power density, rapid charge/discharge, high life cycle and excellent transient response.

Emadi *et al.* provided an overview of hybrid electric and fuel-cell vehicle power system architectures [73]. Lahyani *et al.* investigated battery/supercapacitor combinations in UPS applications [74]. Kollimalla *et al.* proposed a control strategy for battery and supercapacitor storage systems [15]. These studies demonstrate that hybrid storage can reduce battery stress and improve system performance.

Mesbahi *et al.* developed an advanced model of a hybrid ESS (HESS) integrating lithium-ion batteries and supercapacitors for EV applications [75]. Reddy *et al.* proposed a battery–supercapacitor HESS for EV operation over a wide ambient temperature range [76]. Bai *et al.* investigated optimal HESS design for improving battery lifetime in plug-in hybrid EVs [77]. Sadeq *et al.* investigated optimal control strategies for maximizing HESS performance while considering vehicle topography [78]. C. Jia *et al.* developed real-time model predictive control using linear parameter-varying models for battery–supercapacitor HESS [79]. These advanced control techniques can improve power-sharing performance, but they may require higher computational complexity.

Bandwidth-based control provides a relatively simple alternative. Shahverdi *et al.* investigated a bandwidth-based control strategy for a series hybrid EV with light energy storage [80]. As battery and supercapacitor are ideally suited to low-frequency and high-frequency power components, respectively, the frequency-based power allocation concept is especially appealing for BSCES. Fixed bandwidth control, however, does not always yield the best results. Furthermore, the control design needs to account for parameter uncertainty and converter dynamics.

2.10 Control and Stability of Interconnected Converter Systems

Dynamic interactions are introduced when several power electronic converters are integrated into a single DC bus. A converter that is stable on its own could cause instability when connected to another converter.

Vettuparambil *et al.* proposed a MPC interfacing PV modules and energy storage with a DC microgrid [14]. Surulivel *et al.* proposed a four-port converter with bidirectional ports for PV HESSs [70]. D. Rojas *et al.* investigated the control of a four-port DC–DC converter for PV systems integrating batteries and supercapacitors [81]. These studies directly demonstrate the potential of four-port converter architectures for integrating renewable energy and hybrid energy storage. However, the dynamic coupling among PV, battery, supercapacitor, and DC-bus voltage requires a coordinated control strategy.

He *et al* investigated unified frequency-domain small-signal stability analysis for interconnected converter systems [82]. Their work emphasizes the importance of considering interactions among converter subsystems. Nonlinear control has also been investigated for interleaved converters. Echalih *et al.* studied nonlinear control design and stability analysis of a single-phase half-bridge interleaved buck shunt active power filter [83]. Repecho *et al.* investigated a fixed-switching-frequency interleaved sliding-mode eight-phase synchronous buck converter [84]. Such approaches provide strong robustness but may involve increased implementation complexity.

2.11 Research Gaps Identified in the Literature

After the thorough review of the literature, it is identified that significant advancements have been made in the development of interleaved DC–DC converters, mathematical modeling methodologies, HESS, and multiport power conversion architectures. However, still a number of significant research gaps, sustain.

First, a significant portion of the described work is dedicated to converter topology, voltage conversion ratio, ripple reduction and switching-loss reduction. The impact of practical circuit parasitics on the dynamic properties and phase margin (PM) and gain margin (GM) of multiphase interleaved converters has not been thoroughly studied, despite the fact that these contributions enhance converter performance.

Second, system-level simulation and controller design frequently employ traditional averaged models. However, simplified models, could overlook parasitic resistances and

other nonidealities that might drastically alter the PM and GM, damping characteristics, converter poles, and zeros. Therefore, to accurately forecast converter behavior, a thorough mathematical model that is parasitic incorporated is essential.

Third, steady-state performance, ripple cancellation, current sharing, or efficiency are typically highlighted in current research on multiphase and interleaved converters. The comprehensive characterization of the impact of parasitic factors on the dynamic behavior of interleaved converters under various operating conditions has received relatively less attention.

Fourth, the coordinated interaction between the BSCES, multiport/interleaved DC–DC converter, and DC bus dynamics continues to be an important research area, despite the fact that BSCES have been thoroughly studied for EVs, renewable energy systems, and DC microgrids. More research is needed, specifically on how converter nonidealities affect power-sharing and closed-loop stability.

Fifth, simplified converter models are used in the development of several current HESS control techniques. When parasitic components, parameter uncertainties, operating-point fluctuations, and many switching states are taken into account at the same time, such techniques might not accurately depict the real converter dynamics.

Lastly, a comprehensive framework that integrates dynamic characterization, parasitic-aware modeling of interleaved converters, HES integration, and coordinated control for battery and supercapacitor systems is required. The study described in this thesis is motivated by these gaps.

Chapter 3

Design and Characterization of *n*-Phase IBC with Circuit Parasitic

3.1 Introduction

High-efficiency, compact, and high-power-density DC–DC converters are in great demand due to the growing use of renewable energy systems, EVs, ESSs, telecommunication power supply, and high-performance computing. Because of its straightforward circuit design, ease of control, and high efficiency, the buck converter has been widely used among many converter topologies whenever a regulated step-down DC voltage is needed [1]. The traditional single-phase buck converter, however, faces a number of practical drawbacks when the output current demand rises, such as increased current stress on semiconductor devices, increased current ripple, larger passive components, higher thermal stress, and decreased dynamic performance. These restrictions worsen in high-current applications including distributed power architectures, battery charging systems, VRMs and EV power converters [2].

The idea of interleaving has been widely used in contemporary power electronic converters to get around these problems. Multiple identical buck converter cells connected in parallel make up an IBC, where each phase runs at the same switching frequency but is phase-shifted with respect to neighboring phases. The ripple currents generated by specific converter branches are either entirely or partially cancelled by the phase-shifted operation. As a result, the converter's overall input and output current ripple is much decreased, enabling the use of smaller inductors and capacitors while also enhancing transient response and converter efficiency. Additionally, the decreased ripple current improves heat distribution across semiconductor components, lowers EMI, and boosts converter dependability. These advantages have established interleaved converters as one of the preferred converter topologies for medium- and high-power DC–DC conversion applications [3].

The fast-charging infrastructure involves state of art battery technology, motors, and drives applications with HV and high current output converters with a proper charging

algorithm for lithium-ion battery packs, which are widely used in EVs [3]. IBCs, with their simple design structure and low control complexity, are beneficial to use in situations that require high output current with a low ripple and step-down conversion ratio [33]. The benefits of interleaved converters are as follows: *(i)* reduces the filter requirement due to increased output ripple multiplicity [35]; *(ii)* there is a significant reduction in the required rating of the inductor and input/output capacitor [85]; *(iii)* the transient response of the system is faster for a shift in load [48]. The interleaving technique is used for many applications, ranging from low-power VRMs to high-power converters for applications in renewable energy integration, energy storage, communication networks, data centers, transportation electrification, and smart-home devices [44], [46], [82].

The battery charging systems require converters that can supply high charging currents with little current ripple, the fast expansion of battery-powered EVs has speed up research on interleaved converters [44]. Reduced warmth, increased charging efficiency, and longer battery life are all directly improved by lower charging ripple. Additionally, interleaved converters' modular design allows for simple power scalability by adding more phases without significantly altering the converter's overall architecture [32], [46], [83]. As a result, multiphase IBCs are now appealing options for energy storage applications, data-center power supply, renewable energy interfaces, onboard chargers, off-board rapid chargers, and aerospace power systems.

Practical converters always include a number of non-ideal features that significantly affect their steady-state and dynamic behavior, even though the ideal operation of IBCs has been widely documented in the literature [56]. The ESR of capacitors and inductors, internal resistance of the input source, on-state voltage drop of semiconductor switches, and forward voltage drop of freewheeling diodes are some examples of these non-idealities [16]. These parasitic components increase power losses, change converter dynamics, lower voltage gain, change damping properties, and have an impact on the closed-loop system's PM and GM. Inaccurate mathematical models and controller designs that diverge from real-world converter behavior are thus frequently the consequence of ignoring these parasitic elements.

Sample-data modeling and state-space averaged (SSA) modeling are the most widely used modeling techniques for switched-mode power converters, according to reports [16].

By analyzing the converter over individual switching intervals, sample-data models accurately capture switching behavior. Nevertheless, they frequently result in mathematically complex expressions that offer little physical insight into converter dynamics [57]-[59]. By employing averaged continuous-time equations to represent the converter, the state-space averaging technique, on the other hand, removes high-frequency switching components. While maintaining the dominant low-frequency dynamics needed for controller design and stability analysis, this greatly streamlines mathematical analysis [86], [87]. The state-space averaging technique has become one of the most used modeling techniques for switching power converters because of these benefits.

Previous studies have mostly concentrated on modeling two-phase IBCs or traditional buck converters. Although these studies offer insightful information about how converters work, they do not create a generic mathematical framework that can incorporate useful circuit parasitics and be applied to an arbitrary number of interleaved phases. Additionally, there are still not many thorough analytical studies that explain how parasitic components affect PM, voltage gain, and converter characteristics. For systematic converter design and controller development across a wide variety of power ratings, generalized modeling of *n*-phase IBC (*n*PIBC) therefore becomes crucial.

This chapter presents the SSA model, including steady state and small signal modeling for *n*PIBC with circuit parasitic. The circuit parasitic components include the internal resistance of the supply voltage, the ESR of the inductor, the ESR of the capacitor, the switch on-state voltage drop, and the diode forward voltage. The effect of changes in the number of phases, passive components, and variable circuit parasitic on characteristics and system stability has been analyzed. The TPIBC has been designed, and a prototype has been developed considering the requirements of 2-wheeler and 3-wheeler charging at 48V and 60V, respectively.

3.2 Operation Principle of IBC

The interleaving can be used to increase the power handling capacity, lower current ripple and improve overall converter performance. In order to maintain a fixed phase displacement between the gate signals of neighboring converter phases, the technique entails connecting several identical converter cells in parallel and running them with the same switching frequency. An IBC reduces the electrical and thermal stresses on

individual semiconductor devices by distributing the load current among multiple parallel branches, in contrast to a traditional single-phase buck converter that processes the entire load current through a single switching branch.

The coordinated switching of several converter phases forms the basis of an IBC's operation. The gate pulses are equally phase-shifted throughout a single switching period, yet each phase functions as a separate buck converter.

The inductor current waves produced by distinct phases are dispersed uniformly during a single switching time because the converter branches function sequentially rather than simultaneously. The average current components are added while the alternating ripple components partially cancel each other when these branch currents are joined at the output node. As a result, compared to a comparable single-phase converter running at the same switching frequency, the converter shows noticeably less input and output current ripple.

The interleaving idea has a number of significant benefits. First, as the number of converter phases increases, the current handled by each phase drops proportionately, improving heat distribution and lowering conduction losses. Second, smaller passive filter components can be used because the effective ripple frequency seen at the output increases with the number of phases. Lastly, by merely adding more converter phases without altering the fundamental converter topology, the modular design of the converter enables power scaling. IBCs are one of the most popular topologies for high-current power conversion applications because of these features.

The fundamental mechanisms responsible for the improved performance of interleaved converters are discussed in the following subsections.

3.2.1 Ripple Cancellation Mechanism:

The reduction of current ripple through the phenomena of ripple cancellation is the main benefit of interleaving. The output current ripple in a traditional buck converter is equivalent to the ripple generated by the single filter inductor whereas *n*PIBC, shown in Fig. 3.1 is made up of $x = 1$ to n inductors with phase-shifted ripple currents. Depending on the duty cycle and number of converter phases, the ripple components are either entirely or partially eliminated when these separate inductor currents are added together.

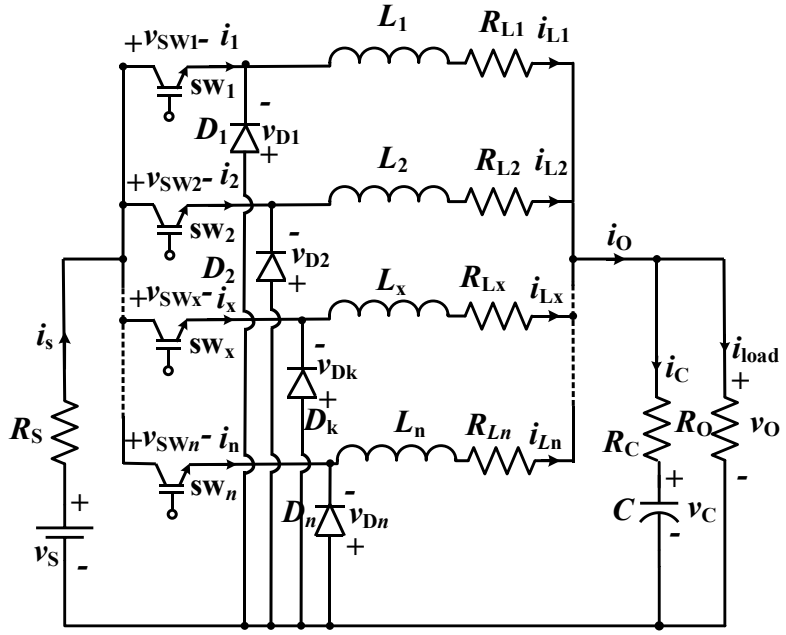


Fig. 3.1 Circuit diagram of *n*PIBC with circuit parasitic.

For an *n*PIBC, the output current is expressed as

$$i_O(t) = \sum_{x=1}^{n} i_{Lx}(t) \tag{3.1}$$

where, $i_{Lx}(t)$ denotes the current flowing through the kth inductor.

Each inductor current consists of an average component and a ripple component,

$$i_{Lx}(t) = I_{Lx} + \Delta i_{Lx}(t) \tag{3.2}$$

where, I_{Lx} is the average inductor current and $\Delta i_{Lx}(t)$ represents the ripple current.

Substituting the above expression into the output current equation yields

$$i_O(t) = \sum_{x=1}^{n} I_{Lx}(t) + \sum_{x=1}^{n} \Delta i_{Lx}(t) \tag{3.3}$$

When put together, the ripple components tend to cancel each other out since they are evenly phase displaced by $360^O/n$. Consequently, the net ripple current is much lower than the ripple current generated by each individual converter branch. Complete cancellation of dominant ripple harmonics may happen under specific duty-cycle conditions, producing an output current that is nearly ripple-free. In addition to lowering the output voltage ripple and increasing converter efficiency, the decrease in ripple current also

reduces the current passing through the output capacitor. Additionally, the reduced ripple current extends the service life of passive components.

3.2.2 Effective Switching Frequency:

The increase in the effective ripple frequency seen at the converter output is another significant feature of the interleaving approach. The phase-shifted operation results in the switching events of individual phases being uniformly dispersed over the switching period, even if each converter phase works at the same switching frequency fs. Consequently, the output ripple appears at a frequency equal to

$$f_{ri} = n \times f_S \tag{3.4}$$

where, f_{ri} is the effective ripple frequency, f_S is the switching frequency of each converter phase, and n is the total number of interleaved phases.

The energy storage components can function more efficiently due to the rise in ripple frequency. Smaller inductors and output capacitors can be used to maintain the same output voltage ripple specification since the ripple period lowers as the number of phases increases. Higher power density and lower converter volume are directly impacted by this decrease in passive component size.

3.2.3 Current Sharing:

Another crucial aspect of interleaved converters is current sharing. The entire load current is split among all phases since identical converter branches are linked in parallel. Each converter phase carries an equal amount of the load current under balanced operating conditions and identical component values. The total output current is given by, (3.1). For balanced operation,

$$I_{L1} = I_{L2} = \cdots = I_{Ln} = \frac{I_O}{n} \tag{3.5}$$

As a result, as the number of converter phases increases, the current stress on each power semiconductor device and magnetic component lowers. A number of useful benefits result from the decrease in branch current. First, because there is less current passing through each switch, semiconductor devices have lower conduction losses. Second, a longer component lifetime and increased dependability are the outcomes of a

more even distribution of thermal dissipation throughout the converter phases. Lastly, current sharing keeps the necessary converter power rating while enabling the use of devices with lower current ratings. However, due to differences in parasitic resistances, semiconductor properties, and inductance values, perfect current sharing is not always possible in real-world converters. As a result, current-balancing strategies are frequently used to guarantee that converter branches receive an equal amount of current.

3.3 Two-phase IBC with Circuit Parasitics

The impact of component losses and non-ideal features is ignored in the ideal. Nevertheless, the steady-state and dynamic performance of practical IBCs is greatly impacted by a number of parasitic components. These parasitic components must be included in the converter model in order to produce a mathematical model that faithfully captures the real-world converter. As the most basic multiphase arrangement, the two-phase IBC serves as the foundation for expanding the study to converters with more phases. Consequently, before extending the concept to an arbitrary number of phases, a thorough mathematical model of the two-phase converter incorporating circuit parasitics is first discussed.

3.3.1 Circuit Configuration

IBC operates on principle of operation nearly identical to the traditional buck converter. The two-phase IBC circuit diagram in Fig. 3.2 (a) shows various parasitic components of Two-Phase IBC with resistive load (R_O); the source voltage is v_s; the two vertical branches have the forward voltage drops of the diodes (v_{D1}, v_{D2}) and the two horizontal branches have switch on voltage drops (v_{SW1}, v_{SW2}). The ESRs of the source voltage and filter capacitor are denoted by Rs and Rc, respectively; the ESRs of the filter inductors of the two branches of the interleaved converter are denoted by R_{L1} and R_{L2}. The parasitic values are regarded as constant during the switching period.

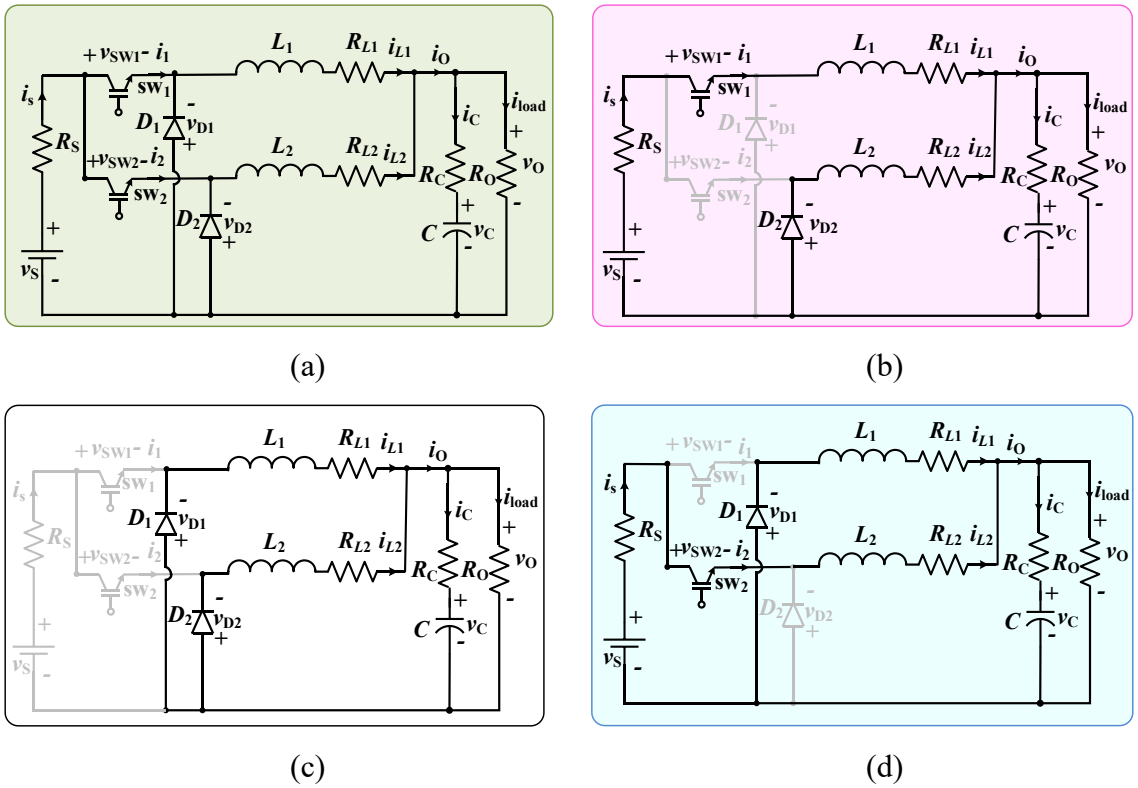


Fig. 3.2 Two-phase IBC with circuit parasitic (a) circuit diagram (b) Mode 1 operation (c) Mode 2 and Mode 4 operation (d) Mode 3 operation.

Two-phase IBC operates in four modes, as shown in Fig. 3.2 (b)–(d). In mode-1, SW_2 is in the off-state while SW_1 is turned on. In this mode, energy is stored in inductor L_1 and the current flowing through it, i.e., i_{L1}, grows. When switch SW_2 is switched off, the energy of inductor is released through diode D_2, which lowers the current i_{L2}. v_{SW1} across switch SW_1 and v_{D2} across diode D_2 are the on-state voltage drops, respectively. In mode-2, the current i_{L1} and i_{L2} decreases switches SW_1 and SW_2 switched off and the energy is released to load through diodes D_1 and D_2. v_{D1} and v_{D2} are parasitic voltage drops. In mode 3, SW_1 is in the off-state while switch SW_2 is turned on. In this mode, energy is stored in the inductor L_2 as the current, i_{L2} flowing through it increases. When switch SW_1 is switched off, the energy held in inductor i_{L1} is released through diode D_1, which causes the current i_{L1} to drop. In this mode of operation, the voltage drops v_{SW2} across the switch SW_2 and v_{D1} across diode D_1 are taken into account. The operation in mode-4 is as mode-2.

3.3.2 Mathematical Modeling of Two-phase IBC

The switching circuit is described over a specified switching period using state space analysis. The SSA model is constructed and subsequently linearized about the operational point during a single switching cycle, and the descriptive set of equations is determined. The following is the state space equation during a switching cycle:

$$\frac{dx(t)}{dt} = \dot{x}(t) = \mathbf{A}_k x(t) + \mathbf{B}_k u(t) \tag{3.6}$$

$$y(t) = \mathbf{C}_k x(t) + \mathbf{D}_k u(t) \tag{3.7}$$

Equation (3.6) represents the state equation with state variable $x(t)$ ε $R^{m\times1}$ and input variable $u(t)$ ε $R^{p\times1}$, whereas equation (3.7) represents the output equation with output as $y(t)$ ε $R^{q\times1}$, where m, p, and q represent the different states variables, input variables, and output variables, respectively. The designed circuits, input, output, and direct transmission matrices for the kth switching mode are represented by the matrices A_k ε $R^{m\times m}$, B_k ε $R^{m\times p}$, C_k ε $R^{q\times m}$, and D_k ε $R^{q\times p}$. The four switching configurations for two-phase IBC are represented by k = 1 to 4. Branch current i_{L1}, i_{L2}, and filter capacitor voltage v_C are the state variables in the two-phase IBC with circuit parasitic depicted in Fig. 3.2(a); source voltage v_S, voltage drops v_{SW1}, v_{SW2}, and v_{D1}, v_{D2} are regarded as input variables; the voltage v_O is output variable. Switches SW_1 and SW_2 have duty ratios of d_1 and d_3, respectively. In the duty ratio, the duration of mode-2 and mode-4 operation is represented as d_2 and d_4, respectively. Additionally, the following relationship is taken into consideration to lessen the complexity of mathematical derivations:

$$d_1 = d_3 = d, \text{ and } \quad d_2 = d_4 = (1/2 - d) \tag{3.8}$$

The averaging of the state matrices for two-phase IBC system can be expressed as follows:

$$\begin{aligned} A &= (A_1 + A_3)d + (A_2 + A_4)(1/2 - d); \\ B &= (B_1 + B_3)d + (B_2 + B_4)(1/2 - d); \\ C &= (C_1 + C_3)d + (C_2 + C_4)(1/2 - d); \\ D &= (D_1 + D_3)d + (D_2 + D_4)(1/2 - d). \end{aligned} \tag{3.9}$$

TABLE 3.1

PARAMETERS OF FOUR MODES OF OPERATION OF TWO-PHASE IBC WITH CIRCUIT PARASITIC.

Sl. No.	Modes	Parameters
a.	Mode 1	$A_1=\begin{bmatrix} \frac{-1}{L_1}\left(R_S+R_{L_1}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_{L_2}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}$; $B_1=\begin{bmatrix} \frac{1}{L_1} & \frac{-1}{L_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ $C_1=\begin{bmatrix} \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix}$; $D_1=[0 \quad 0 \quad 0 \quad 0 \quad 0]$;
b.	Mode 2	$A_2=\begin{bmatrix} \frac{-1}{L_1}\left(R_{L_1}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_{L_2}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}$; $B_2=\begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ $C_2=\begin{bmatrix} \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix}$; $D_2=[0 \quad 0 \quad 0 \quad 0 \quad 0]$;

Sl. No.	Modes	Parameters
c.	Mode 3	$A_3=\begin{bmatrix} \frac{-1}{L_1}\left(R_{L_1}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_S+R_{L_2}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}$ $B_3=\begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 \\ \frac{1}{L_2} & 0 & \frac{-1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$ $C_3=\begin{bmatrix} \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix}; \quad D_3=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix};$
d.	Mode 4	$A_4=A_2; \quad B_4=B_2; \quad C_4=C_2; \quad D_4=D_2$
e.	Two-Phase IBC SSA Model	$A=\begin{bmatrix} \frac{-1}{L_1}\left(R_S d+R_{L_1}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_S d+R_{L_2}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix};$ $B=\begin{bmatrix} \frac{d}{L_1} & \frac{-d}{L_1} & 0 & \frac{-(1-d)}{L_1} & 0 \\ \frac{d}{L_2} & 0 & \frac{-d}{L_2} & 0 & \frac{-(1-d)}{L_2} \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix};$ $C=\begin{bmatrix} \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix}; \quad D=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix}.$

Where, $R_{OC}=R_O+R_C$

Equations (3.6), (3.7), (3.8) and (3.9) determines the state, input, output, and direct transmission parameters for said converter. Tables 3.1 represents the SSA model matrices. Accordingly, the transfer functions general expression can be derived as:

$$\mathrm{S}X(S) = \mathrm{A}X(S) + \mathrm{B}U(S) \tag{3.10}$$

$$X(S) = (\mathrm{SI\text{-}A})^{-1}\ \mathrm{B}U(S) \tag{3.11}$$

$$Y(S) = \mathrm{C}(\mathrm{SI\text{-}A})^{-1}\ \mathrm{B}U(S) \tag{3.12}$$

$$G(S) = \mathrm{C}(\mathrm{SI\text{-}A})^{-1}\ \mathrm{B} \tag{3.13}$$

Therefore, after finding out the parameters *A*, *B* and *C,* using (3.13) provide the transfer function for two-phase IBC with circuit parasitics

3.4 TPIBC and *n*PIBC with Circuit Parasitics

The basic knowledge of interleaved converter operation is provided by the two-phase IBC covered in the preceding section. However, a number of real-world uses, such as high-current VRMs, renewable energy interfaces, telecommunication power supply, and electric car battery chargers, require output currents greater than what two converter phases can provide. By dispersing the load current among a greater number of converter cells and concurrently enhancing ripple cancellation and thermal performance, increasing the number of interleaved branches offers an efficient option.

The next level of complexity among different multiphase configurations is represented by the TPIBC, which is a crucial intermediate topology for creating a generic mathematical model that may be applied to *n*PIBC. The TPIBC architecture offers better dynamic response, lower current stress per switching device, higher effective ripple frequency, and better ripple cancellation than the two-phase converter. It is especially appropriate for medium- and high-power battery charging systems because of these features. Practical three-phase interleaved converters, like two-phase converters, have a number of non-ideal features, such as source resistance, semiconductor voltage dips, and the ESR of inductors and capacitors. To effectively forecast converter behavior under realistic operating conditions, these parasitic factors must be included in the mathematical model since they alter the converter dynamics. As a result, the generalized *n*-phase converter model is derived from the state-space model developed in this section, which incorporates all important parasitic elements.

At least one converter branch constantly transmits energy to the output during steady-state operation. As a result, compared to a two-phase converter, the combined output current shows noticeably less ripple. Additionally, the input current becomes smoother due to the regular distribution of switching transitions during the switching duration, which lowers EMI and increases converter efficiency. The incorporation of parasitic resistances modifies the voltage applied across each inductor and introduces additional damping into the converter dynamics. These effects are explicitly considered during the state-space modelling presented in the subsequent subsections.

3.4.1 Circuit Configuration

The per-phase working principle of the IBC is nearly identical to that of the simple buck converter. Fig. 3.3 (a) depicts the schematic circuit of *n*PIBC at resistive load (R_O), where each branch resembles a CBC with different components that are switch, diode, and inductor, with circuit parasitic for all the branches, and it is considered a constant such as the on-state switch voltage drop (v_{SWx}), the forward voltage drops of diodes (v_{Dx}), and the ESR for filter inductor (R_{Lx}), respectively, of the xth branch of the interleaved converter, where $x = 1, 2, \ldots, n$. The source voltage is v_S; the capacitor voltage is v_C; and the output voltage is v_O, respectively. The ESR of the supply voltage and filter capacitor are represented by R_S and R_C, respectively.

In this section, the complete state space analysis is presented for TPIBC with parasitic variables and then generalized to *n*PIBC. Fig. 3.3 (b) represents TPIBC with parasitic variables, which comprises three sets of switches with inductors and freewheeling diodes coupled to a common filter capacitor (C) with parasitic resistance (R_C) and load (R_O). The TPIBC operates in six different modes of operation, as shown in Fig. 3.3 (c)–(f), and the respective waveforms are presented in Fig. 3.4.

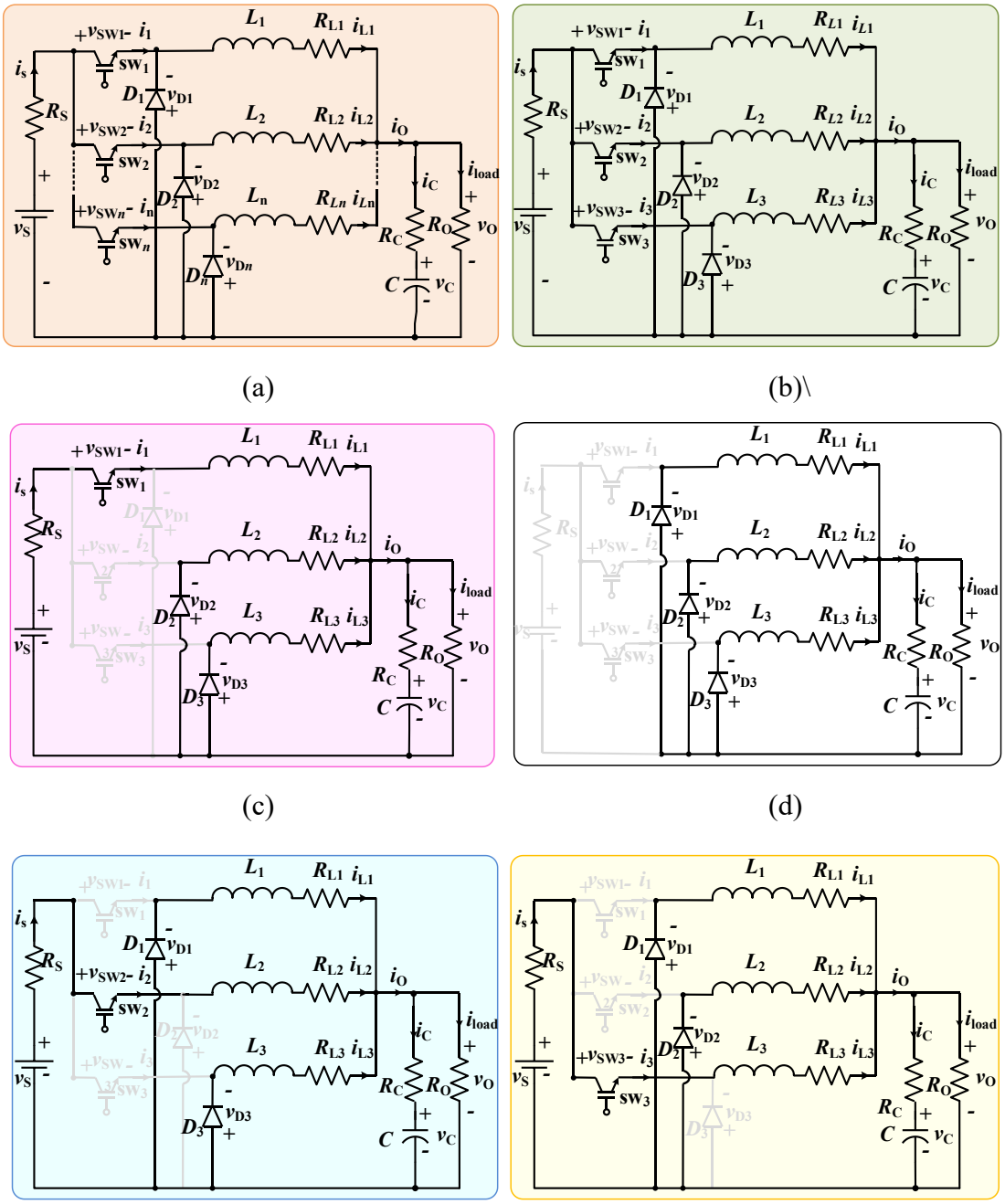


Fig. 3.3 Circuit diagram with circuit parasitic for (a) *n*PIBC; (b) TPIBC; (c) TPIBC in mode M1; (d) TPIBC in freewheeling modes M2, M4, and M6; (e) TPIBC in mode M3; and (f) TPIBC in mode M5.

In mode M1, the first branch switch SW_1 is triggered, and the other switches SW_2 and SW_3 are kept inactive. The voltage drops across SW_1, i.e., v_{SW1}, and the resultant voltage appears across the parasitic inductor L_1 along with the load, which stimulates the rise in

inductor current, i.e., $i_{L1,}$ and energy stored in inductor L_1. As the remaining switches SW_2 and SW_3 are switched off, the freewheeling diodes D_2 and D_3 allow to release the stored energy in the inductors L_2 and $L_{3,}$ resulting in the inductor currents i_{L2} and i_{L3} decreasing. The voltages v_{D1}, $v_{D2,}$ and v_{D3} are the voltage drops across diodes D_1, $D_{2,}$ and D_3, respectively. In mode M2, M4 M6 all the switches $SW_{1,}$ $SW_{2,}$ and SW_3 are switched-off, and all the freewheeling diodes D_1, $D_{2,}$ and D_3 are allowed to release the accumulated energy in the inductors L_1, $L_{2,}$ and $L_{3,}$ resulting in a drop in inductor current $i_{L1,}$ $i_{L2,}$ and i_{L3}, respectively. In modes M3 and M5, the second branch switch SW_2 and the third branch switch SW_3 are triggered, respectively, and the behavior of the circuit is similar to that in mode M1. In modes M4 and M6, the operation is similar to M2. In all six modes of operation, there is loss of energy and voltage drop due to the ESR of filter inductors (R_{L1}, $R_{L2,}$ and R_{L3}), filter capacitors (R_C), and internal resistance of the source voltage (R_s).

3.4.2 Mathematical Modeling of TPIBC

The state space model for the TPIBC circuit with parasitic variables is presented in this section. The switching circuit is described via state-space analysis over a switching period. A state space averaged (SSA) model is developed for one switching cycle, which is then linearized further around the operational point and necessitates the descriptive set of equations. The state space equation for one switching cycle is expressed as equation (3.6) and (3.7) and the matrices are derived as explained in previous section for the kth switching configuration, where k = 1 to 2n, where the total number of switching configurations for n-PIBC is 2n.

Referring to the TPIBC having parasitic components as shown in Fig. 3.3 (b), current for filter inductors are i_{Lx}, where x= 1 to 3 and voltage for filter capacitor is v_C are the state variables; input voltage v_S, switches voltage drops v_{SWx}, where x= 1 to 3, and diodes conduction voltage drops v_{Dx}, where x= 1 to 3 are the input variables; and the voltage across the load v_O is taken as the output variable. The value $d_{1,}$ $d_{2,}$ $d_{3,}$ $d_{4,}$ $d_{5,}$ and d_6 are considered as a duty ratio for the six modes of operation M1, M2, M3, M4, M5, and M6 of TPIBC, respectively.

$$d_1 + d_2 + d_3 + d_4 + d_5 + d_6 = 1 \qquad 3.14$$

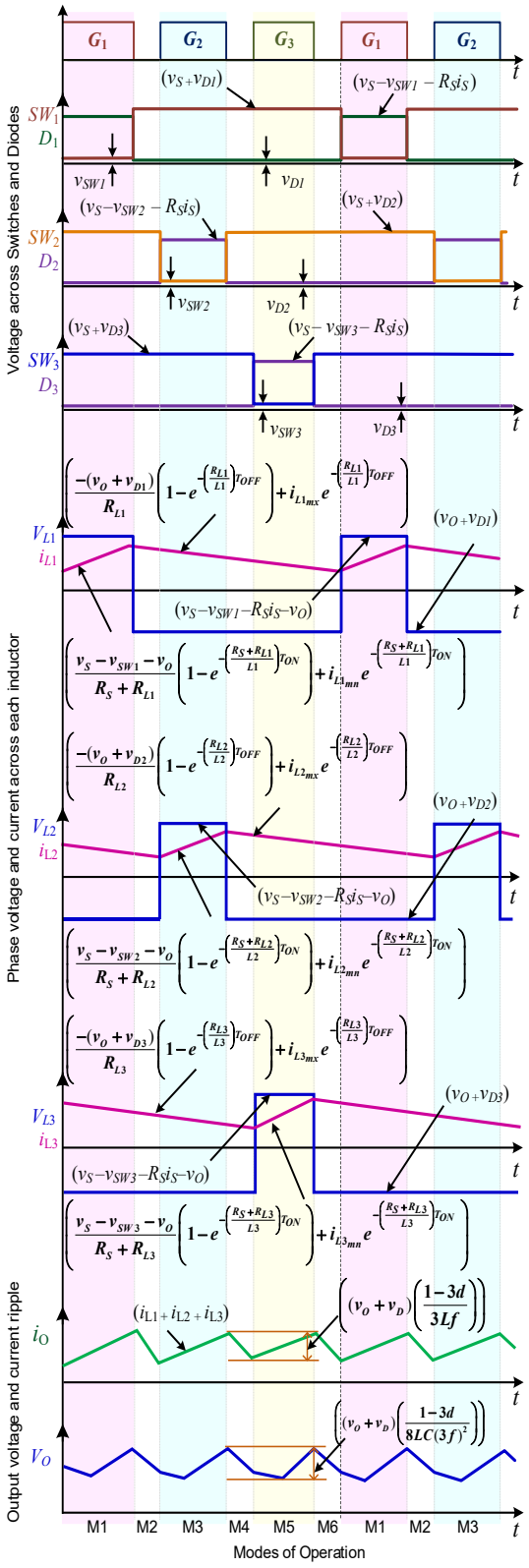


Fig. 3.4 Characterization of input and output variables in different modes of operation for TPIBC.

Therefore, the averaging of the state matrices of TPIBC system can be expressed as follows:

$$\begin{aligned} A &= A_1d_1 + A_2d_2 + A_3d_3 + A_4d_4 + A_5d_5 + A_6d_6; \\ B &= B_1d_1 + B_2d_2 + B_3d_3 + B_4d_4 + B_5d_5 + B_6d_6; \\ C &= C_1d_1 + C_2d_2 + C_3d_3 + C_4d_4 + C_5d_5 + C_6d_6; \\ D &= D_1d_1 + D_2d_2 + D_3d_3 + D_4d_4 + D_5d_5 + D_6d_6; \end{aligned} \quad 3.15$$

Duty ratio of individual switch during turn-on and turn-off is considered as d and (1-d), respectively; therefore, TPIBC during switch-on is d for modes M1, M3, M5 and written as follows:

$$d_1 = d_3 = d_5 = d \quad 3.16$$

During modes M2, M4, and M6, all the switches are off and the energy freewheel through diodes (i.e., with the consideration of the duty time period of the individual switch $dT_s \leq T_s/n$; where T_s is the switching period) and the duty ratio can be defined as follows:

$$d_2 = d_4 = d_6 = \left(\frac{1}{3} - d\right) \quad 3.17$$

Equations (3.6), (3.7) and (3.14) to (3.17) are applicable in the estimation of the state, input, output, and direct transmission matrices for TPIBC having parasitic components operating in the six modes of switching up to duty ratio 1/3. The various switching matrices in Table 3.2 is the SSA model for TPIBC are determined in the same manner as for two-phase IBC in previous section.

3.5 Steady State and Small Signal Analysis for *n*PIBC

The steady state model for *n*PIBC is yield from (3.10) and (3.11) by changing the minuscule to majuscule and the derivative terms to zero, as shown below:

$$\dot{X} = AX + BU = 0 \quad 3.18(a)$$

$$Y = CX \quad 3.18(b)$$

The steady state variables are as represented as X, U and Y, where X = States, U = Input and Y = Output.

TABLE 3.2

PARAMETERS OF SIX MODES OF OPERATION AND SSA MODEL OF TPIBC WITH CIRCUIT PARASITIC

Sl. No.	Modes	Parameters
a	Mode 1	$A_1=\begin{bmatrix} \frac{-1}{L_1}\left(R_S+R_{L_1}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_{L_2}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_3}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(R_{L_3}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}; B_1=\begin{bmatrix} \frac{1}{L_1} & \frac{-1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \begin{pmatrix} C_1=\begin{bmatrix} \frac{R_OR_C}{R_{OC}} & \frac{R_OR_C}{R_{OC}} & \frac{R_OR_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix} \\ D_1=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{pmatrix}$
b	Mode 2	$A_2=\begin{bmatrix} \frac{-1}{L_1}\left(R_{L_1}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_{L_2}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_3}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(R_{L_3}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}; B_2=\begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \begin{pmatrix} C_2=\begin{bmatrix} \frac{R_OR_C}{R_{OC}} & \frac{R_OR_C}{R_{OC}} & \frac{R_OR_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix} \\ D_2=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{pmatrix}$
c	Mode 3	$A_3=\begin{bmatrix} \frac{-1}{L_1}\left(R_{L_1}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_S+R_{L_2}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_3}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(R_{L_3}+\frac{R_OR_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}; B_3=\begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ \frac{1}{L_2} & 0 & \frac{-1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \begin{pmatrix} C_3=\begin{bmatrix} \frac{R_OR_C}{R_{OC}} & \frac{R_OR_C}{R_{OC}} & \frac{R_OR_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix} \\ D_3=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{pmatrix}$
d	Mode 4	$A_4=A_2;\quad B_4=B_2;\quad C_4=C_2;\quad D_4=D_2$

TABLE 3.2

PARAMETERS OF SIX MODES OF OPERATION AND SSA MODEL OF TPIBC WITH CIRCUIT PARASITIC

e	Mode 5	$A_5=\begin{bmatrix} \frac{-1}{L_1}\left(R_{L_1}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_{L_2}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_3}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(R_S+R_{L_3}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}; B_5=\begin{bmatrix} 0 & 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ \frac{1}{L_3} & 0 & 0 & \frac{-1}{L_3} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \begin{pmatrix} C_5=\begin{bmatrix} \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix} \\ D_5=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{pmatrix}$
f	Mode 6	$A_6 = A_2;\quad B_6 = B_2;\quad C_6 = C_2;\quad D_6 = D_2$
TPIBC SSA Model		$A=\begin{bmatrix} \frac{-1}{L_1}\left(R_S d+R_{L_1}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_S d+R_{L_2}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_3}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(R_S d+R_{L_3}+\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_3}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}; B=\begin{bmatrix} \frac{d}{L_1} & \frac{-d}{L_1} & 0 & 0 & \frac{-(1-d)}{L_1} & 0 & 0 \\ \frac{d}{L_2} & 0 & \frac{-d}{L_2} & 0 & 0 & \frac{-(1-d)}{L_2} & 0 \\ \frac{d}{L_3} & 0 & 0 & \frac{-d}{L_3} & 0 & 0 & \frac{-(1-d)}{L_3} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \begin{pmatrix} C=\begin{bmatrix} \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix} \\ D=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \end{pmatrix}$

where, $R_{OC} = R_O + R_C$

Thus, X and Y has been derived as shown below:

$$X = -A^{-1}BU \tag{3.19}$$

$$Y = -CA^{-1}BU \tag{3.20}$$

Any system's controller is designed with an intent to handle the small signal portion. Deviation from the defined steady state operating point can be identified using small signal analysis. This exercise may help determine the improvement of stability of the closed-loop system. The input-output equilibrium in the *n*PIBC with circuit parasitic is disrupted by a small perturbation near the operating point. The remaining input parameters are in a stable state, but the input supply (v_S) and output voltage (v_O) are disturbed around their typical values. The phenomenon is represented by the following equation:

$$v_S = V_S + \hat{v_S};\ \text{where}\ \frac{\hat{v_S}}{V_S} << 1 \hat{v_S} \tag{3.21}$$

$$v_O = V_O + \hat{v_O};\ \text{where}\ \frac{\hat{v_O}}{V_O} << 1 \tag{3.22}$$

where, the steady state value and perturbed values are represented as V_X and $\hat{v}_X$ respectively. The disturbed system is required to be brought back to equilibrium therefore controller reacts to change duty ratio by small amount and hence states change as follows:

$$d = D + \hat{d};\ \text{where}\ \frac{\hat{d}}{D} << 1 \tag{3.23}$$

$$x = X + \hat{x};\ \text{where}\ \frac{\hat{x}}{X} << 1 \tag{3.24}$$

where, the steady state duty ratio is *D* and and state variable is *X*. $\hat{d}$ is the deviation in duty ratio to bring equilibrium in system and $\hat{x}$ is states parameters deviation. Substituting the derived parameters from (3.21), (3.22), (3.23), (3.24) in (3.6), (3.7) and taking steady state equation (3.13) and omitting the perturbed parameters product the dynamic response of the of *n*PIBC can be stated as follows:

$$\dot{\hat{x}} = A\hat{x} + B\hat{v}_S + E\hat{d} \tag{3.25}$$

$$v_O = C\hat{x} + F\hat{d} \tag{3.26}$$

$$\text{Where, } E = \left(\sum_{i=1}^{n} A_{2i-1} - A_{2i}\right)X + \left(\sum_{i=1}^{n} B_{2i-1} - B_{2i}\right)U \tag{3.27}$$

$$F = \left(\sum_{i=1}^{n} C_{2i-1} - C_{2i}\right)X \tag{3.28}$$

where, E ϵ $R^{m\times1}$, F ϵ $R^{q\times1}$, and X and U are state variable and input variables in steady state respectively. The small signal matrices for *n*PIBC has been presented in Table 3.3. For TPIBC (n = 3), applying the Laplace transform to (3.25) and (3.26) and further simplifying, we get,

$$\left.\frac{\hat{v}_O(s)}{\hat{v}_S(s)}\right|_{\hat{d}(s)=0} = C(SI - A)^{-1}B \tag{3.29}$$

$$\left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{v}_S(s)=0} = C(SI - A)^{-1}E + F \tag{3.30}$$

The transfer function for the disturbance appears in the supply voltage of TPIBC with $\hat{d} = 0$ is defined for a system as given in (3.29) and transfer function for the disturbance appears in the duty ratio of TPIBC with $\hat{v}_S = 0$ is defined for system given in (3.30). The steady-state voltage gain and transfer function for TPIBC are derived and presented in Table 3.4 This section's steady-state and small-signal analysis lay the mathematical groundwork for comprehending the dynamic behavior of the suggested *n*PIBC. The small-signal model describes the connection between changes in the duty ratio and the associated changes in the state variables and output voltage, whereas the steady-state model gives the operating point around which the converter dynamics are linearized. The generated small-signal transfer functions are especially helpful for assessing the converter's transient performance and frequency response. Additionally, the development and application of suitable control measures are based on these analytical models.

TABLE 3.3

SMALL SIGNAL MODEL OF N-PHASE IBC WITH CIRCUIT PARASITIC

$$A = \begin{bmatrix} \frac{-1}{L_1}\left(R_S d + R_{L_1} + \frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \cdots & \frac{-1}{L_1}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_1}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(R_S d + R_{L_2} + \frac{R_O R_C}{R_{OC}}\right) & \cdots & \frac{-1}{L_2}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_2}\left(\frac{R_O}{R_{OC}}\right) \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ \frac{-1}{L_n}\left(\frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_n}\left(\frac{R_O R_C}{R_{OC}}\right) & \cdots & \frac{-1}{L_n}\left(R_S d + R_{L_n} + \frac{R_O R_C}{R_{OC}}\right) & \frac{-1}{L_n}\left(\frac{R_O}{R_{OC}}\right) \\ \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \cdots & \frac{1}{C}\left(\frac{R_O}{R_{OC}}\right) & \frac{-1}{C}\left(\frac{1}{R_{OC}}\right) \end{bmatrix}; E = \begin{bmatrix} \frac{1}{L_1}(V_S + V_{D_1} - V_{SW_1} - R_S I_{L_1}) \\ \frac{1}{L_2}(V_S + V_{D_2} - V_{SW_2} - R_S I_{L_2}) \\ \vdots \\ \frac{1}{L_n}(V_S + V_{D_n} - V_{SW_n} - R_S I_{L_n}) \\ 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{d}{L_1} & \frac{-d}{L_1} & 0 & \cdots & 0 & \frac{-(1-d)}{L_1} & 0 & \cdots & 0 \\ \frac{d}{L_2} & 0 & \frac{-d}{L_2} & \cdots & 0 & 0 & \frac{-(1-d)}{L_2} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & 0 & \vdots & \vdots & \ddots & 0 \\ \frac{d}{L_n} & 0 & 0 & \cdots & \frac{-d}{L_n} & 0 & 0 & \cdots & \frac{-(1-d)}{L_n} \\ 0 & 0 & 0 & \cdots & 0 & 0 & 0 & \cdots & 0 \end{bmatrix}; \begin{cases} C = \begin{bmatrix} \frac{R_O R_C}{R_{OC}} & \frac{R_O R_C}{R_{OC}} & \cdots & \frac{R_O R_C}{R_{OC}} & \frac{R_O}{R_{OC}} \end{bmatrix} \\ D = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & \cdots & 0 \end{bmatrix} \\ F = 0 \end{cases}$$

where, $R_{OC} = R_O + R_C$

TABLE 3.4

TRANSFER FUNCTIONS AND VOLTAGE GAIN FOR TPIBC WITH CIRCUIT PARASITIC

$$\left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{v}_S(s)=0} = \frac{V_S}{C\left(\frac{L_1L_2L_3}{L_1L_2+L_2L_3+L_3L_1}\right)S^2+\frac{1}{R_O}\left(\frac{L_1L_2L_3}{L_1L_2+L_2L_3+L_3L_1}\right)S+1} \tag{3.31}$$

$$\left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{v}_S(s)=0} = \frac{R_O\left[\begin{array}{c}[CR_CL_2L_3S^3+\{L_2L_3+CR_C(L_2R_{L_3}+L_3R_{L_2}+L_2R_Sd+L_3R_Sd)\}S^2+\{L_2R_{L_3}+L_3R_{L_2}+L_2R_Sd+L_3R_Sd+CR_C(R_S^2d^2+R_{L_2}R_{L_3}+\\ R_{L_2}R_Sd+R_{L_3}R_Sd)\}S+R_S^2d^2+R_{L_2}R_{L_3}+R_{L_2}R_Sd+R_{L_3}R_Sd](V_S+V_{D_1}-V_{SW_1}-R_SI_{L_1})+[CR_CL_1L_3S^3+\{L_1L_3+CR_C(L_1R_{L_3}+L_3R_{L_1}\\ +L_1R_Sd+L_3R_Sd)\}S^2+\{L_1R_{L_3}+L_3R_{L_1}+L_1R_Sd+L_3R_Sd+CR_C(R_S^2d^2+R_{L_1}R_{L_3}+R_{L_1}R_Sd+R_{L_3}R_Sd)\}S+R_S^2d^2+R_{L_1}R_{L_3}+R_{L_1}R_Sd\\ +R_{L_3}R_Sd](V_S+V_{D_2}-V_{SW_2}-R_SI_{L_2})+[CR_CL_1L_2S^3+\{L_1L_2+CR_C(L_1R_{L_2}+L_2R_{L_1}+L_1R_Sd+L_2R_Sd)\}S^2+\{L_1R_{L_2}+L_2R_{L_1}+L_1R_Sd+\\ L_2R_Sd+CR_C(R_S^2d^2+R_{L_1}R_{L_2}+R_{L_1}R_Sd+R_{L_2}R_Sd)\}S+R_S^2d^2+R_{L_1}R_{L_2}+R_{L_1}R_Sd+R_{L_2}R_Sd](V_S+V_{D_3}-V_{SW_3}-R_SI_{L_3})\end{array}\right]}{\left[\begin{array}{c}CL_1L_2L_3(R_O+R_C)S^4+\{L_1L_2L_3+C(L_1L_2+L_2L_3+L_1L_3)R_OR_C+C(L_1L_2R_{L_3}+L_1L_3R_{L_2}+L_2L_3R_{L_1})(R_O+R_C)+C(L_1L_2+L_2L_3+L_1L_3)(R_O+R_C)R_Sd\}S^3\\ +\{(L_1L_2R_{L_3}+L_1L_3R_{L_2}+L_2L_3R_{L_1})+(L_1L_2+L_2L_3+L_1L_3)(R_O+R_Sd)+C(L_1+L_2+L_3)R_Sd(R_CR_Sd+R_OR_Sd+2R_OR_C)+C(L_1R_{L_2}R_{L_3}+L_2R_{L_1}R_{L_3}+\\ L_3R_{L_1}R_{L_2})(R_O+R_C)+C(L_1R_{L_2}+L_2R_{L_1}+L_1R_{L_3}+L_3R_{L_1}+L_2R_{L_3}+L_3R_{L_2})(R_OR_C+R_CR_Sd+R_OR_Sd)\}S^2+\{(L_1+L_2+L_3)R_Sd(2R_O+R_Sd)+\\ (L_1R_{L_2}R_{L_3}+L_2R_{L_1}R_{L_3}+L_3R_{L_1}R_{L_2})+(L_1R_{L_2}+L_2R_{L_1}+L_1R_{L_3}+L_3R_{L_1}+L_2R_{L_3}+L_3R_{L_2})(R_O+R_Sd)+C(R_O+R_C)R_S^3d^3+CR_C(R_{L_1}+R_{L_2}+R_{L_3}+3R_O)R_S^2d^2\\ +CR_O(R_{L_1}+R_{L_2}+R_{L_3})R_S^2d^2+C(R_O+R_C)(R_{L_1}R_{L_2}R_{L_3})+C(R_{L_1}R_{L_2}+R_{L_1}R_{L_3}+R_{L_2}R_{L_3})(R_OR_C+R_CR_Sd+R_OR_Sd)+2CR_C(R_{L_1}+R_{L_2}+R_{L_3})R_OR_Sd\}S\\ +R_S^3d^3+3R_OR_S^2d^2+R_{L_1}R_{L_2}R_{L_3}+(R_{L_1}R_{L_2}+R_{L_1}R_{L_3}+R_{L_2}R_{L_3})(R_O+R_Sd)+(R_{L_1}+R_{L_2}+R_{L_3})R_Sd(2R_O+R_Sd)\end{array}\right]} \tag{3.32}$$

$$\frac{V_O}{V_S} = \frac{R_O\left[\begin{array}{c}[d-\frac{1}{V_S}\{V_{D_1}(1-d)+V_{SW_1}d\}](R_{L_2}+R_Sd)(R_{L_3}+R_Sd)+[d-\frac{1}{V_S}\{V_{D_2}(1-d)+V_{SW_2}d\}](R_{L_3}+R_Sd)(R_{L_1}+R_Sd)\\ +[d-\frac{1}{V_S}\{V_{D_3}(1-d)+V_{SW_3}d\}](R_{L_1}+R_Sd)(R_{L_2}+R_Sd)\end{array}\right]}{R_S^3d^3+(R_{L_1}+R_{L_2}+R_{L_3}+3R_O)R_S^2d^2+R_{L_1}R_{L_2}R_{L_3}+(R_{L_1}R_{L_2}+R_{L_1}R_{L_3}+R_{L_2}R_{L_3})(R_O+R_Sd)+2(R_{L_1}+R_{L_2}+R_{L_3})R_OR_Sd} \tag{3.33}$$

3.6 Performance Evaluation of the *n*PIBC

The steady-state and dynamic behavior of the suggested *n*PIBC are fully represented by the mathematical models created in the earlier sections. However, a thorough analysis of the converter performance under various operating conditions is necessary to determine the generated models' actual utility. As a result, this section provides a methodical evaluation of the suggested converter's performance through analytical research and simulation experiments. The analysis focuses on how frequency response, stability, ripple characteristics, and battery charging performance are affected by the number of interleaved phases and circuit parasitics.

The single-phase buck converter, two-phase IBC, and TPIBC are designed for a power level of 384 W to 600 W, where the input voltage v_S = 200 V, the output voltage v_O = 48 V or 60 V, the load resistance R_O = 6 Ω, and the switching frequency is 20 kHz. The designed values of circuit components are considered ideal (without parasitic) and with parasitic for the analysis of the converters. The results of TPIBC are presented in comparison with single-phase buck converter and two-phase IBC without parasitics. The value of circuit components for single-phase buck converter, two-phase IBC, and TPIBCs are L = 2.85mH and C = 8.33μF, $L_1 = L_2$ = 1425μH and C = 2.85μF, and $L_1 = L_2 = L_3$ = 950μH and C = 1.02μF, respectively**.** During the experimental testing, the utmost care was taken to ensure that the designed values of branch inductors, L_x, and their parasitic values, R_{Lx}, were equal; however, there were slight variations; the nearest values of circuit parasitics have been considered for analysis, which is based on design and availability. The designed value of TPIBC with circuit parasitic is presented in Table 3.5.

3.6.1 Frequency-Domain Characteristics

A DC–DC converter's frequency response offers important details about its stability and dynamic behavior. Specifically, the open-loop transfer function's gain crossover frequency, phase crossover frequency, GM, and PM are crucial markers for assessing the converter's closed-loop stability and transient response.

TABLE 3.5

PARAMETERS OF TPIBC WITH CIRCUIT PARASITIC

Parameters	Inductor ($L_1 \approx L_2 \approx L_3$)	Capacitor (C)	ESR of Source (R_S) / Inductor ($R_{L1} \approx R_{L2} \approx R_{L3}$) / Capacitor ($R_C$)	On-state switch voltage drop, $V_{SW1} \approx V_{SW2} \approx V_{SW3}$	On-state diode voltage drop, $V_{D1} \approx V_{D2} \approx V_{D3}$
TPIBC with parasitic-I	≈ 960μH	2 μF	0.15Ω / 0.105Ω / 0.2Ω	0.497V	0.442V
TPIBC with parasitic-II			0.65Ω / 0.45Ω / 0.7Ω		

To examine the influence of the number of interleaved phases on converter dynamics, the frequency responses of the single-phase, two-phase, and TPIBC are obtained under identical operating conditions. Fig. 3.5 shows the bode plot of a non-parasitic single-phase buck converter, two-phase IBC, and TPIBC, which is plotted using the equations presented in [16] and (3.31) taking the same rating of inductance and capacitance as TPIBC and at d = 0.24. The graph shows that the GM is infinity for all three cases. However, the PM of a single-phase buck converter is maximum and that of TPIBC is minimum, whereas the gain crossover frequency increases for TPIBC. However, for the design purpose of a particular rating converter, the ratings of the inductor and capacitor for a single-phase buck converter are higher compared to TPIBC.

As per the designed values of components of single-phase, two-phase, and TPIBC, and with derived expressions, the bode plot is depicted in Fig. 3.6. This represents that all three non-parasitic converters have almost equal phage margins, whereas the gain crossover frequency increases for TPIBC.

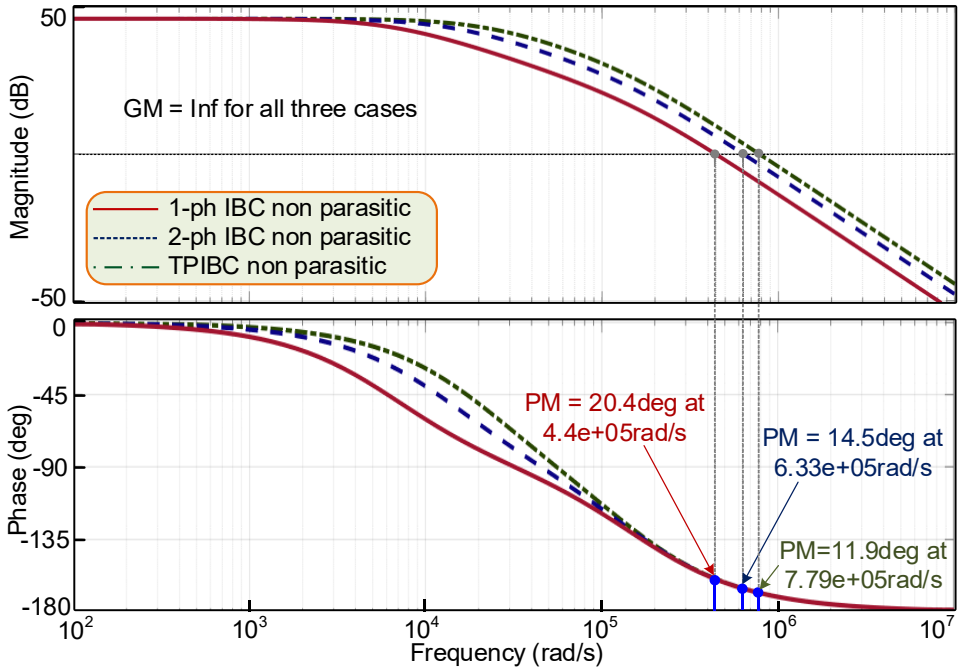


Fig. 3.5 Single-phase buck converter, two-phase IBC, and TPIBC without circuit parasitic for the same value of inductance and capacitance at $d = 0.24$.

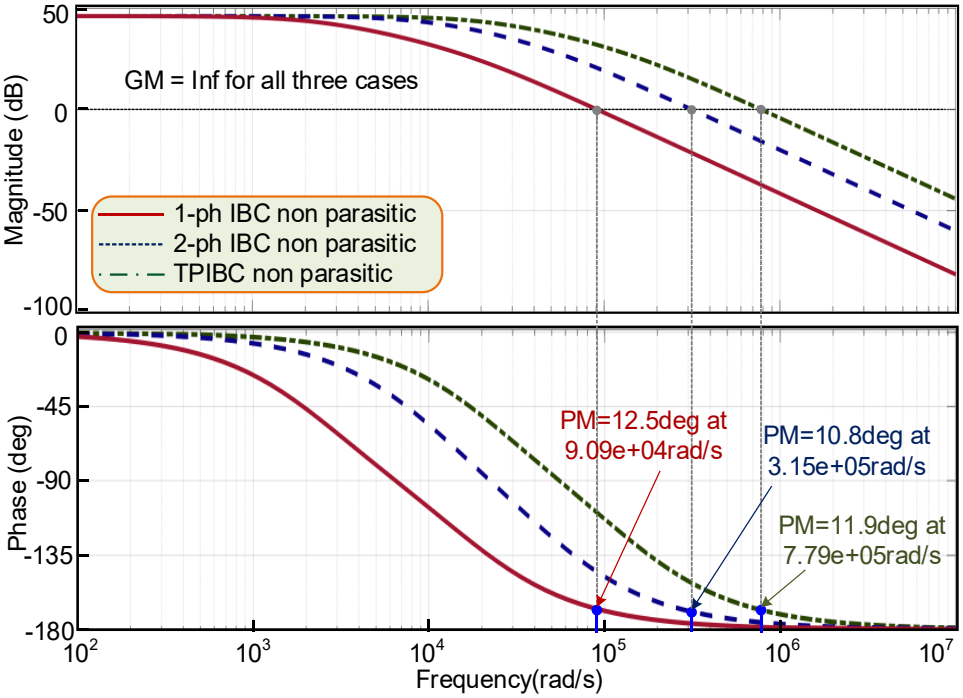


Fig. 3.6 Single-phase buck converter, two-phase IBC, and TPIBC without circuit parasitics for the designed values of inductance and capacitance at $d = 0.24$.

3.6.2 Effect of Circuit Parasitics

Practical component circuit parasitics have a major impact on a DC–DC converter's PM and GM. Ideal converter models do not accurately reflect the dynamic properties of real-world converters, although being helpful for comprehending the fundamentals of operation.

The various circuit components used for the design of TPIBC have non-ideal circuit parasitic properties, and they may vary with the change in designed value, make, and operating conditions. The parasitic variables have been changed by changing the size of inductor and capacitor and adding a series resistance of 0.5Ω to the source for high parasitic TPIBC. The parasitic voltage drops for switches and diodes are considered same for the low parasitic and high parasitic conditions. The bode plot as per the derived transfer function and designed values for TPIBC non-parasitic, low-parasitic, and high parasitic is shown in Fig. 3.7. The PM increases with an increase in parasitic values for approximately the same gain crossover frequency.

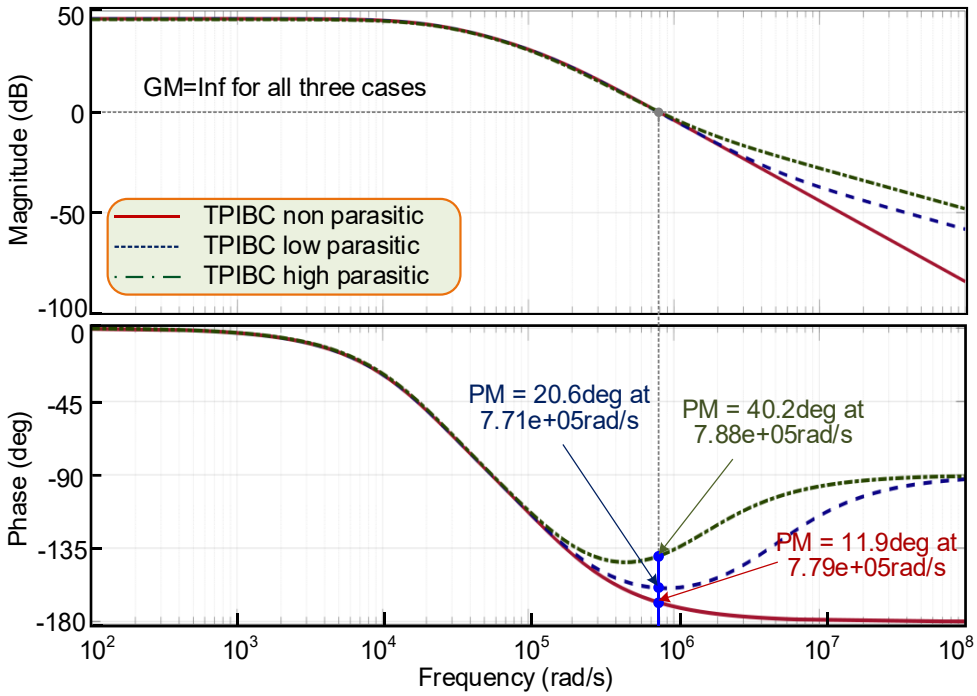


Fig. 3.7 TPIBC with and without circuit parasitic at $d = 0.24$.

3.6.3 Effect of Filter Capacitance

One of the most important passive parts of a buck converter is the output filter capacitor, which directly affects the converter's dynamic stability, transient responsiveness, and output voltage ripple. The output capacitor in an IBC locates the dominating poles and zeros in the control-to-output transfer function in addition to smoothing the combined inductor current. As a result, choosing the right filter capacitance is crucial to attaining enough stability and dynamic performance. The PM with respect to the output filter capacitor has been plotted in Fig. 3.8, which shows that the PM for both the ideal single-phase buck converter and ideal TPIBC drops with a rise in the rating of the filter capacitor.

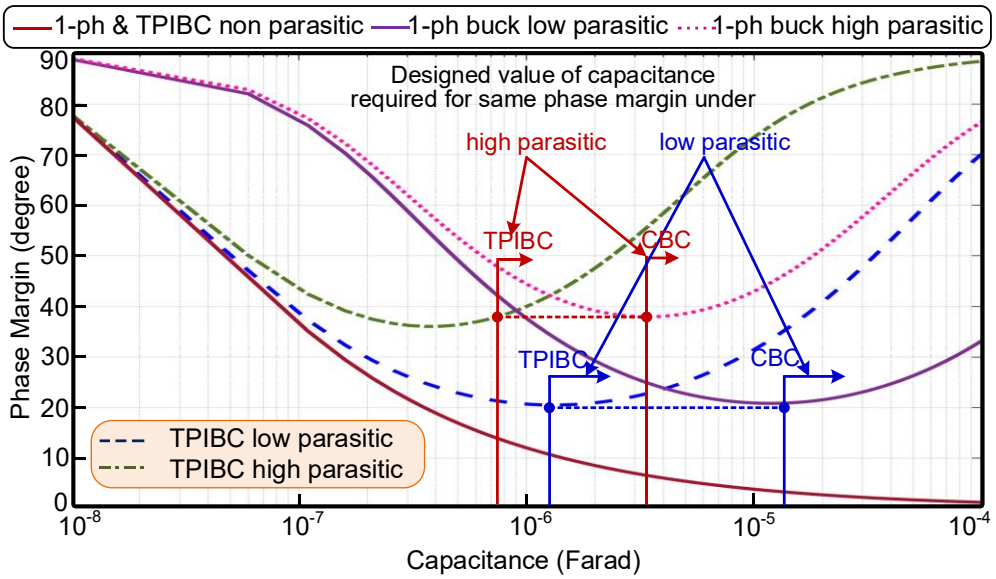


Fig. 3.8 PM for single-phase buck converter (ideal, low parasitic, and high parasitic) and TPIBC (ideal, low parasitic, and high parasitic) for varying capacitance, at $d = 0.24$.

The PM initially drops with an increase in the value of the filter capacitor and thereafter starts increasing for low and high values of parasitic for the single-phase CBC and TPIBC. However, the PM of high parasitic TPIBC starts increasing prior to low parasitic TPIBC and buck converter with circuit parasitic. Thus, in practical terms, TPIBC can be operated at a higher PM with lower values of filter capacitance in comparison to CBC. In all cases, the PM becomes almost constant at higher values of the filter capacitor.

3.6.4 Effect of Circuit Parasitic on Voltage Gain

The voltage gain of TPIBC as derived in (3.33) with circuit parasitic is plotted with varying duty rations in Fig. 3.9. The voltage gain drops with the rise in supply ESR R_S and ESR of the branch inductors $R_{Lx,}$ and it is untrammeled by the ESR of the filter capacitor R_C. The effect of internal resistance of source is significant at a higher side-duty ratio. The effect of ESR of branch inductor R_{Lx} is constant for all duty ratios. The effect of diode voltage drop (v_{Dx}) is maximum at low duty ratio and nominal at high duty ratio, whereas the effect of on-state switch voltage drop (v_{SWx}) is nominal at low duty ratio and maximum at higher duty ratio.

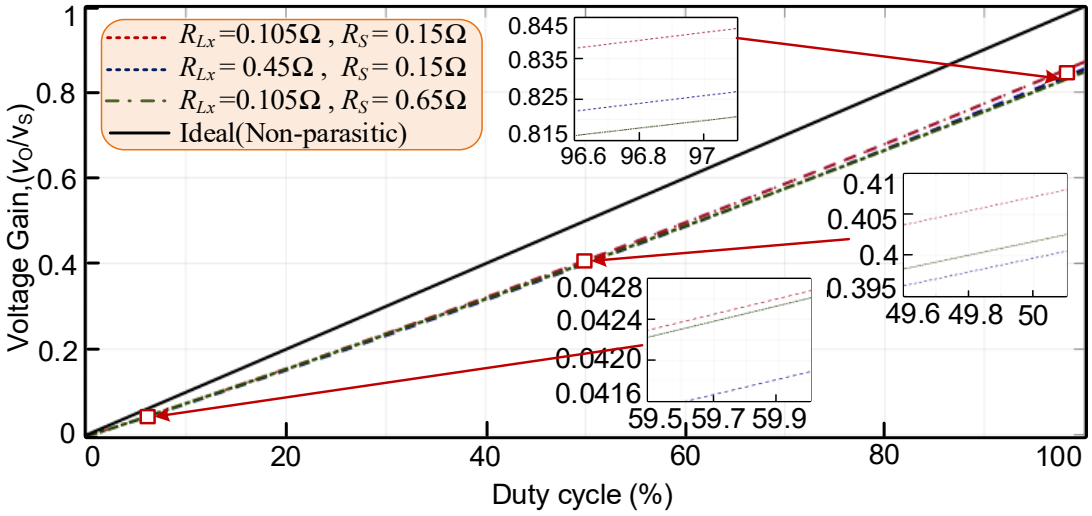


Fig. 3.9 Voltage gain of TPIBC for variation in duty cycle for various values of parasitic variables.

3.6.5 Ripple Characteristics and Battery Performance

It is quite apparent that the ripple voltage reduces with an increase in the value of the filter capacitor for CBC and TPIBC. Fig. 3.10 shows that the PM for non-parasitic CBC and TPIBC reduces with a reduction in the ripple voltage, whereas for both parasitic CBC and parasitic TPIBC, the PM reduces initially with a reduction in the ripple voltage and starts increasing the PM.

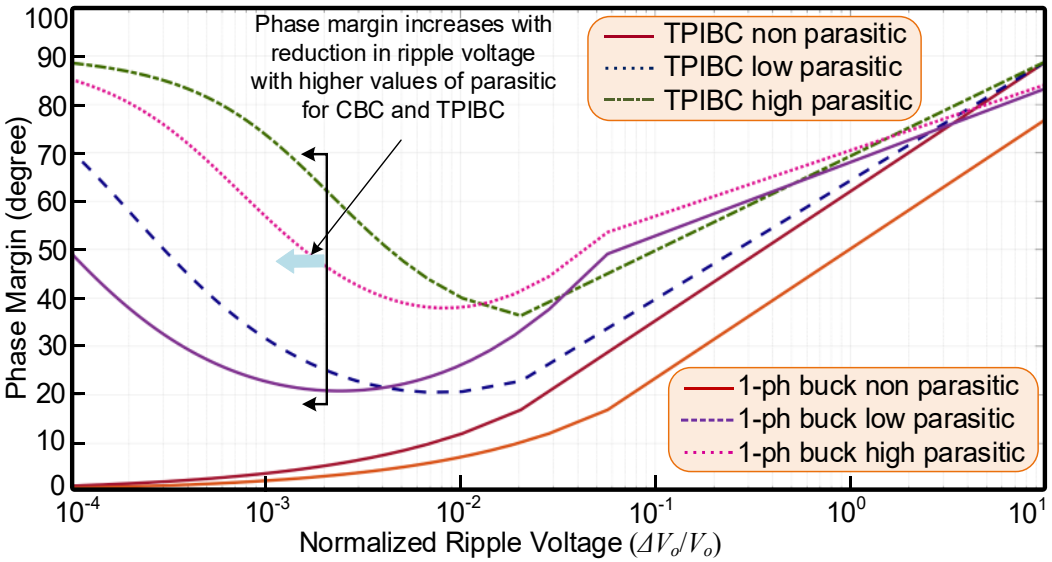


Fig. 3.10 PM with respect to normalized ripple voltage for single-phase buck converter (ideal, low parasitic, and high parasitic) and TPIBC (ideal, low parasitic, and high parasitic) for varying capacitance, at $d = 0.24$.

The TPIBC is simulated for the same value of ESR for each branch inductor, such as R_{Lx} = 0.105Ω, and for different values of ESR for each branch inductor, such as R_{L1}=0.105Ω, R_{L2} = 0.25Ω, and R_{L3} = 0.45Ω, respectively. In the prior case of the same ESR for all inductors, the value of the source current was the same for all three phases, whereas when the ESR for all inductors was different, the low ESR inductor allowed a higher current through it and the high ESR inductor allowed a lower current through it, as shown in Fig. 3.11. This behavior of TPIBC with circuit parasitic reduces the i^2R loss compared to a single-phase buck converter with circuit parasitic due to the nature of self-detecting low resistance paths for higher current.

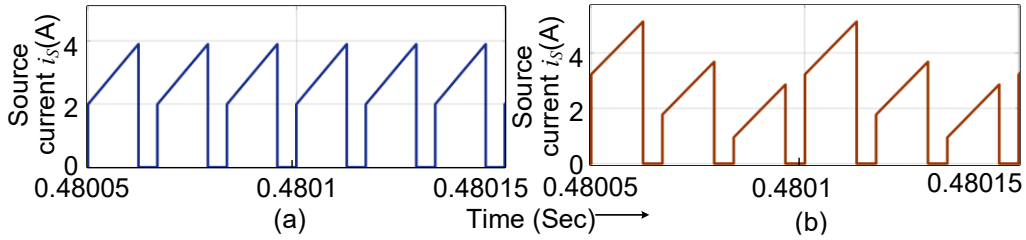


Fig. 3.11 Source current for TPIBC with parasitic (a) same value of ESR for branch inductor, R_{Lx}= 0.105Ω (b) different value of ESR for branch inductor, R_{L1} = 0.105Ω, R_{L2} = 0.25Ω, R_{L3} = 0.45Ω.

The simulation results for TPIBC with parasitic and without parasitic are shown in Fig. 3.12. It is seen that the values are reduced with parasitic in TPIBC. There is a nominal reduction in the ripples of inductor current and output current due to parasitic but there is a considerable reduction in the ripples of input current, capacitor current, and output voltage in parasitic TPIBC compared to non-parasitic TPIBC.

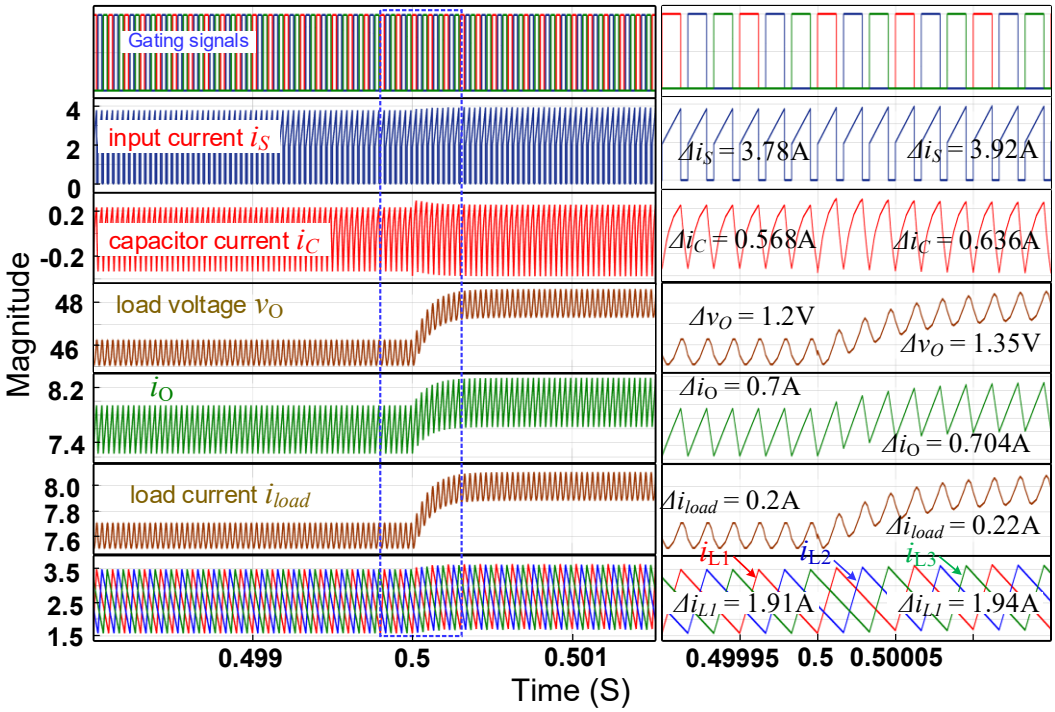


Fig. 3.12 Simulation waveforms for TPIBC with parasitic and without parasitic at d = 0.24.

The proposed ratings of the interleaved converter are aimed at being used as a charger, particularly for batteries of 2-wheeler and 3-wheeler EVs with batteries of 48V and 60V, respectively. The significant advantage of the proposed TPIBC can be analyzed by replacing the resistive load and parallel capacitor with a battery, as presented in Figs. 3.13 (a) and (b). The equivalent circuit model of a battery is shown in Fig. 3.13 (C), which comprises the combined resistance R_{ic} and R_{ct}, and the electric double layer capacitance (C_{ed}) [24]. As the switching frequency of the converter is quite high, i.e., in the order of killo-Hz, the majority of current flows through the low capacitive reactance, X_{Ced} = $1/(2\pi fC_{ed})$, and current flowing through R_{ct} is negligible and (R_{eff} = R_{ic}). The charging current, i_O, comprises the average dc component, I_O, and the ripple component, Δi_O. The

average dc current is utilized for charging the battery, whereas the ripple component causes $\Delta i^2_O R_{eff}$ loss and the resulting enhancement of heating in the battery. Therefore, the ripple component is stressed to be minimized in the charger in order to lower the loss and deterioration of the battery.

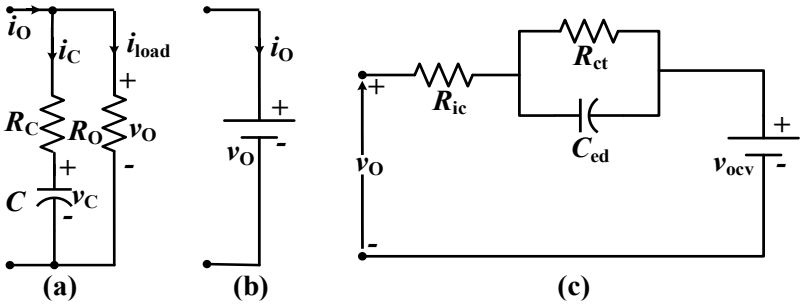


Fig. 3.13 (a) Resistive load (R_O) in parallel to the parasitic capacitor, (b) battery load, (c) equivalent circuit model (ECM) of battery.

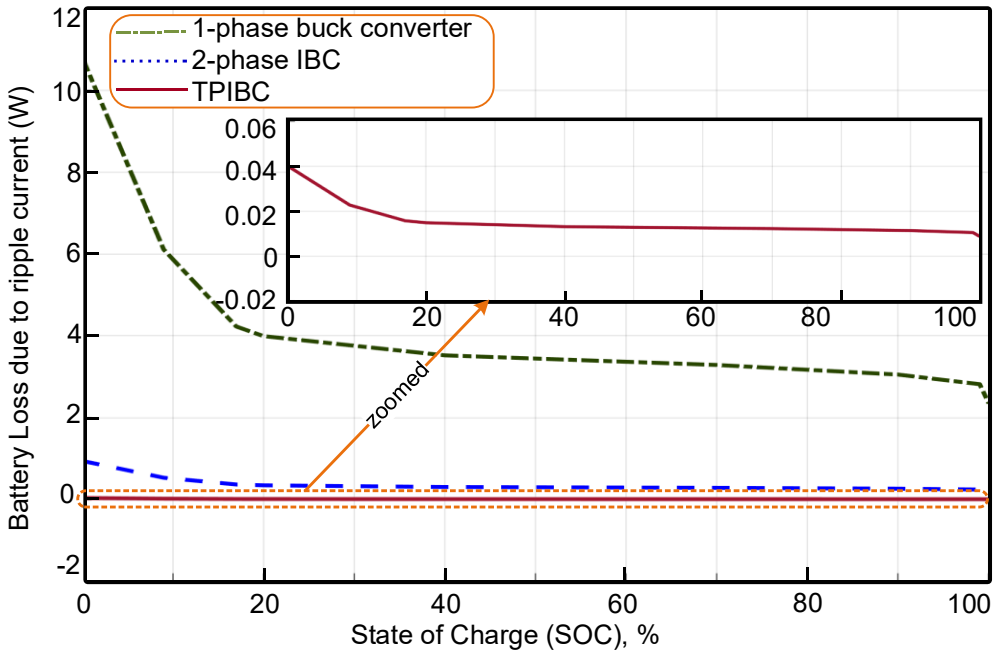


Fig. 3.14 Battery losses due to charger ripple current for 1-phase buck converter, 2-phase IBC and TPIBC with change in SOC for 48V battery.

All the batteries are provided with a battery manual showing the variation of open circuit voltage (v_{OCV}) with the change in state of charge (SOC) of the battery. The 48V battery parameters are used, where charging voltage is kept at 58.4V and v_{OCV} varies from

40V to 54.4V for 0% to 100% SOC. The effect of interleaving for reduction in the ripple current and further losses is demonstrated in Fig. 3.14. It is quite apparent that at a low SOC of the battery, the losses due to ripple current are apparently high for the CBC and lower for the TPIBC. However, the losses reduce with increasing SOC and the higher open circuit voltage of the battery.

3.7 Experimental Validation

A laboratory-scale TPIBC prototype was created in accordance with the design parameters given in the preceding sections in order to verify the suggested analytical model and simulation findings. A direct comparison between theoretical predictions and practical findings was made possible by the prototype's design, which allowed it to function under the same electrical conditions as those taken into account in the analytical and simulation studies.

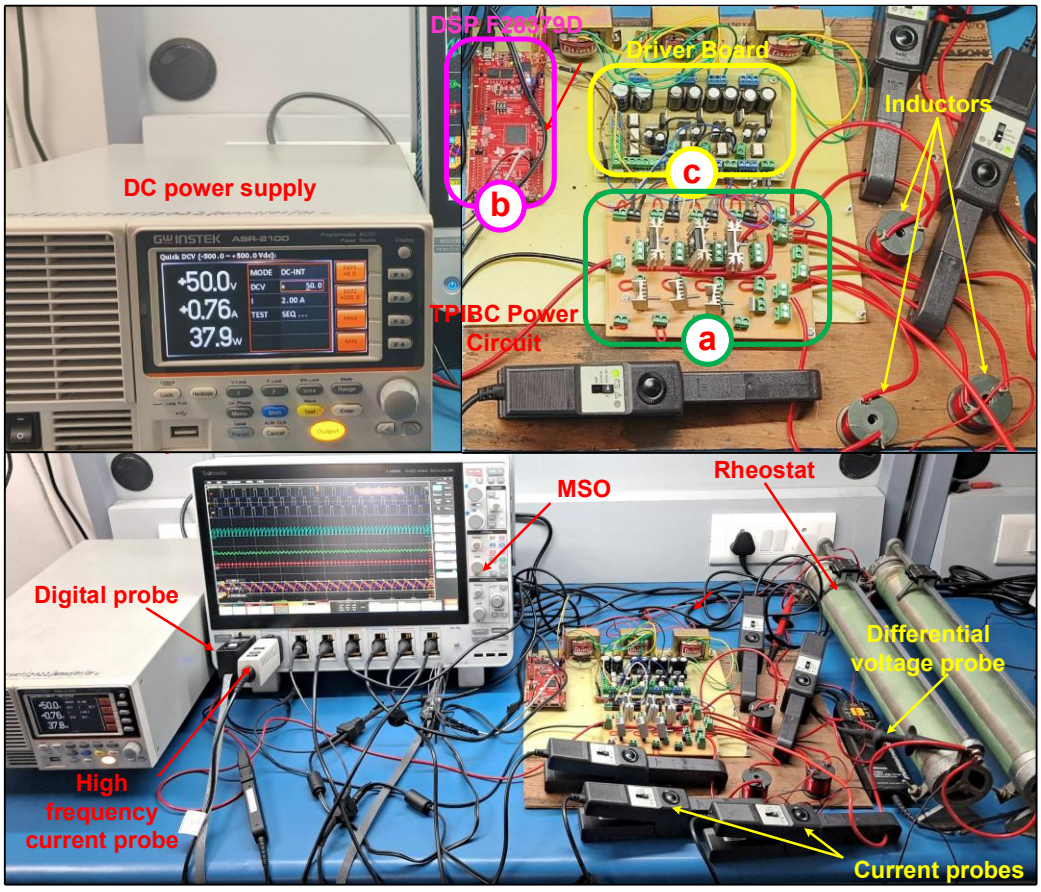


Fig. 3.15 Experimental setup for TPIBC.

A TPIBC prototype is developed, scaling down the voltage rating to 1/4th of the rating specified, such that with the input voltage fixed at 50V, the variable output voltage from 12V to 15V is obtained, changing the duty ratio from 24% to 30%, respectively. The experimental prototype shown in Fig. 3.15 comprises mainly three stages, such as (a) the power stage, comprising power MOSFETs IRFP260N, power diodes RHRP30120, and other components, including a designed toroidal inductor using ferrite core and copper wire and capacitor; (b) the controller stage of the microcontroller LAUNCHXL-F28379D for gating pulse generation; and (c) the driver circuitry and other measuring devices, such as a mixed signal oscilloscope, differential voltage probe, and current probes.

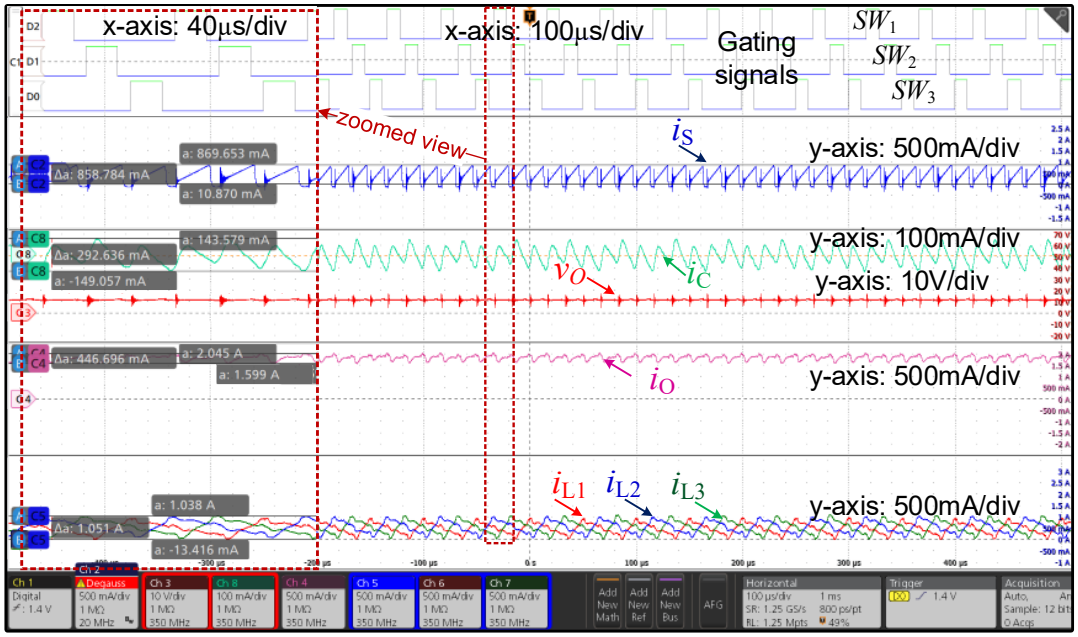


Fig. 3.16 Gate pulse, source current, capacitor current, output voltage, output current, and three-phase currents (top to bottom) at low parasitic for TPIBC at $d = 0.24$.

The results are captured for i) low parasitic value ESR of source, inductor, and capacitor at $d = 0.24$ (Fig. 3.16) and $d = 0.3$ (Fig. 3.17), respectively, and ii) high parasitic value ESR of source, inductor, and capacitor at $d = 0.24$ (Fig. 3.18), respectively, as given in Table 3.5. Figs. 3.16 and 3.17 show the phase current of each phase of TPIBC at $d = 0.24$ has a lower ripple than $d = 0.3$, though all the other ripple components reduce for $d = 0.3$ compared to $d = 0.24$, which implies that all the ripple other than phase current ripple reduces for duty ratio near 1/n^{th} duty ratio. From Figs. 3.16 and 3.18, it is apparent that the values for various parameters reduce for high parasitic TPIBC due to a drop in the

ESR of the source, inductors, and capacitor with switches and diodes compared to low parasitic TPIBC at the same duty ratio $d = 0.24$.

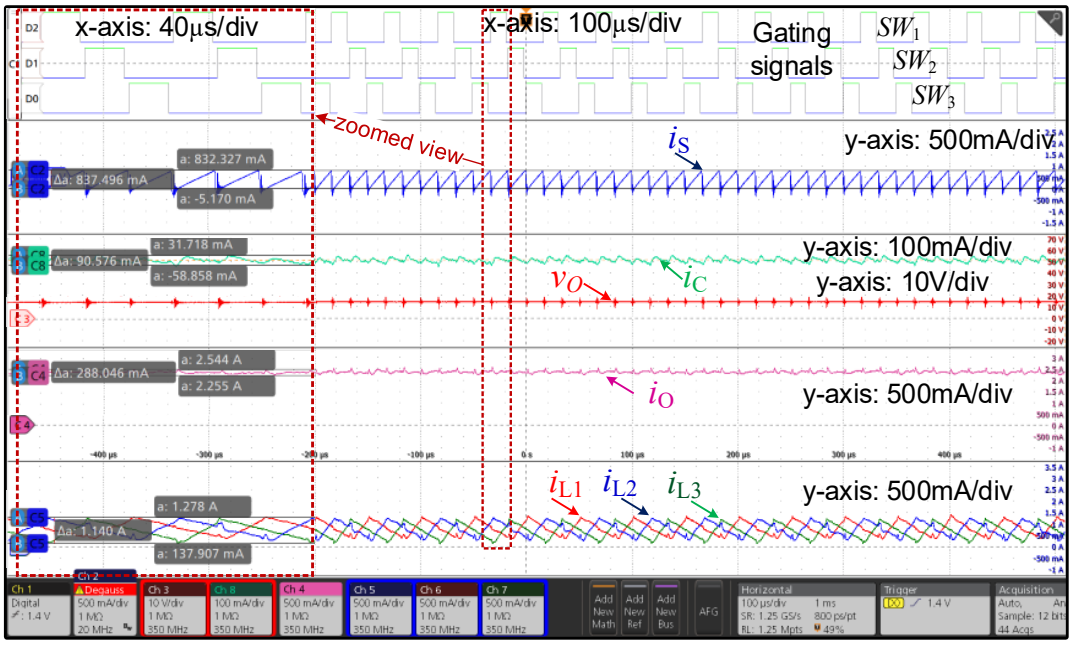


Fig. 3.17 Gate pulse, source current, capacitor current, output voltage, output current, and three-phase currents (top to bottom) at low parasitic for TPIBC at $d = 0.30$.

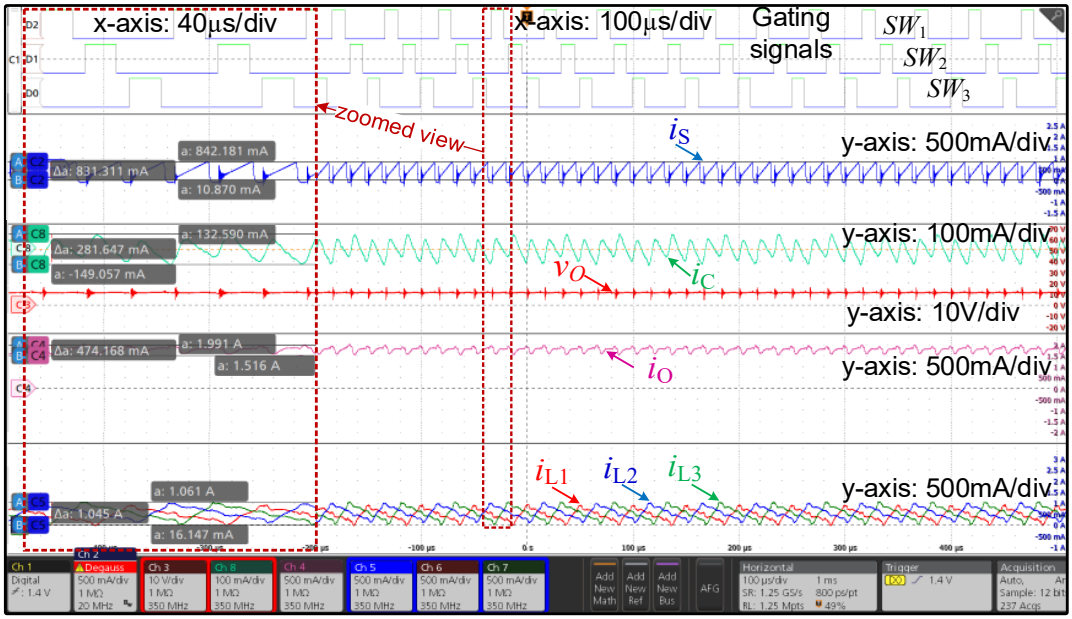


Fig. 3.18 Gate pulse, source current, capacitor current, output voltage, output current, and three-phase currents (top to bottom) at high parasitic for TPIBC at $d = 0.24$.

The experiment has been performed with a 50V input supply voltage. With respect to (3.33), the expected output voltages without circuit parasitic are 12V at $d = 0.24$ and 15V at $d = 0.3$, but due to the existence of circuit parasitic, the output voltage is lower than expected, i.e., 11.8V and 11.2V at $d = 0.24$ for low parasitic and high parasitic values in TPIBC, respectively. The results are in good agreement with derived mathematical relations. The outcomes are well aligned with the derived mathematical relations.

3.8 Conclusion

The state space analysis, including steady state and small signal analysis for *n*-phase IBC with parasitic components, is presented. The comparative analysis with the designed parameters of single-phase buck converters, two-phase IBC, and TPIBC has been presented. The variation in PM with respect to circuit parasitics and the change in filter capacitance around the designed values are presented for TPIBC. The ripple reduces with an enhanced number of phases and becomes nominal for a high capacitance value for the buck converter. The parasitic parameters in a circuit, like the ESR of the source, the ESR of the inductor, and the ESR of the capacitor, the forward voltage drop of diodes, and the on-state switch voltage drop, are considered for the establishment of mathematical relations. This enhances concordance with the experimental data. It is essential to take into account the converter's dynamic properties while building the control loop for a certain application. As a result, the suggested approach is appropriate because it offers a simple means of understanding parasitic IBC dynamics. The TPIBC with circuit parasitic is more stable, and i^2R loss is reduced compared to a single-phase buck converter with circuit parasitic.

Chapter 4

Impact of Operating Duty Ratio on the Performance of IBC under Different Operating Regions

4.1 Introduction

Recent advancements in power electronics provide state-of-the-art techniques for the various aspects of power utility developments. Power converters are used in low- to high-power applications such as mobile chargers, dc drives, front-end rectifiers, EV charging, electrolyzers for hydrogen generation, etc. Green hydrogen generation from renewable energy resources has the potential to achieve the solution for global warming issues and limit the net carbon emissions. The hydrogen electrolyzer requires a high-current output dc-dc converter [88]. In EVs, the cost of the ESS is a major concern. Therefore, reducing the output current ripple of the charging converter is crucial to maintaining the lifespan of the EV battery with improved charging efficiency.

The IBC are suitable for high current, low voltage output with reduced current output ripple and are a potential solution for electrolyzers and charging applications, as shown in chapter 1. Thus, depending on the input dc bus voltage and application power rating, the IBC operates in a range of duty ratios in overlapping or non-overlapping mode. Therefore, reducing the output current ripple of the converter is crucial for all ranges of step-down voltages with high charging currents for versatile and optimal utilization. Thus, with a regulated dc output, an optimally designed converter with negligible output current ripple is the principal research area of concern.

The classic way to reduce output ripple components is to increase the size of the filter inductor and capacitor. However, this method not only increases the size and weight of the converter due to the large energy-storing elements but also affects its transient behavior and increases the loss components. There are various methods in the literature [47], [50], [51], [53] to reduce the ripple current for various dc-dc converter topologies. A common way to lower inductor current ripple is to use the interleaved multi-phase converter branches and change the phase of gate pulses for different branches.

Interleaving techniques make the dc-dc converter more efficient, reducing input output ripple, providing redundancy, and increasing the current capability with similarly rated switches. Applications with lower voltage gain and high current gain, such as VRMs for processing units, battery charging, smart grid networks, and electrolyzers, utilize IBCs [9], [29], [32], [41], [52]. Both fixed and variable output voltage applications utilize the IBCs. The green hydrogen electrolyzer application requires high power with minimum ripple current. Non-isolated topologies are good for selection and are attractive for low-power electrolyzers due to their simple structure and high-power density [9]. Turn ratio in [32], implements the high step-down gain of non-isolated topologies based on coupled inductors. In [29], [41], two-phase IBC is proposed, and a high step-down conversion ratio is to be obtained only for duty ratios less than 0.5 with CCM. A new IBC is proposed to step down the high dc bus voltage application, which is limited to 50% of the duty cycle, as the converter is operated in CCM with lower current stress [46]. The switched-capacitor-based converter is used to improve conversion efficiency but results in a high rise in transient current and conduction loss [43].

In a high-frequency cascaded buck converter, the switching operation would have a narrow duty cycle and a short switch-on time. Under such conditions, the average switching stress value is very high, which is equal to the input voltage for a large switch-off period [45]. Thus, high-input and low-output voltage systems reduce the efficiency of IBCs [89]. If the conversion ratio is higher, the lower-side transistor will be required to handle a significant amount of high current and voltage stress. Furthermore, a series capacitor buck converter's duty ratio doubling effect has a limited range for voltage regulation [42]. In various IBC branches, there is high ripple inductor current due to the use of smaller inductors. The higher ripple current of the branches results in a high ripple input current for IBC [90]. Thus, if the ripple inductor current is higher, a larger inductor and capacitor are required. Also, for various applications, the output ripple current and voltage need to be well within the specified tolerance limit. Thus, the optimal phase-shift modulation is required for ripple cancellation in the IBC. However, all the analysis considers the resistive load and not the constant power load when studying the effect of ripple inductor current in the design of the IBC.

The interleaving of converters helps in achieving ripple cancellation by using the method of phase-shifting in the switching operation of the parallel converter, such that when the current ripples are summed together at the output, the ripple reduces [49], [91]. Thus, due to the interleaving of the buck converter (i.e., IBC), it observes a significant reduction in ripple current, further leading to a reduction in the size of the output LC filter nd an improvement in the dynamic response and power handling capability [48], [92]. The IBC also has the advantage of reducing component stress because it allows for power sharing between each phase of interleaved branches [84]. So, a constant power load and a high duty ratio would allow for high-frequency operation, which would further reduce the size of the filter component used to design the converter. In ideal conditions, IBC is expected to operate with equal sharing of power through the interleaved branches; however, the parasitic component imbalance causes unbalanced power flow through phases in CCM. Studying the behaviour of the IBC at a higher duty ratio is crucial, especially when the IBC operates in DCM due to a reduction in the output current magnitude.

The calculation of switching loss is critical for a realistic estimation of junction temperature as well as determining the power converter's efficiency [92]. Because IBC has many switches, it's important to find the best duty ratio operating region to get the least amount of switching loss for both fixed resistive and constant power loads. The CCM and DCM of branch inductor current have quite a high effect on switching losses and vary depending on the application power, constant power load, and operating duty region.

In order to understand and analyse the impact of variation in the duty ratio for IBCs, a TPIBC is designed for a fixed resistance load and constant power load with variation in the duty ratio for different operating regions. The main contribution of the chapter is to develop the analytical relations and provide the solutions to identify the region of operation with reduced current ripple and switching loss for fixed resistive load, constant power load, and high current load applications.

4.2 Operating Regions of TPIBC

The operational duty ratio has a significant impact on a TPIBC performance. The duty ratio of a multiphase converter also controls the overlap between the switching intervals of neighboring converter phases, unlike a traditional single-phase buck converter where

the duty ratio mainly controls the output voltage. As a result, changes in the duty ratio alter the converter's dynamic behavior, ripple cancellation mechanism, and current conduction sequence.

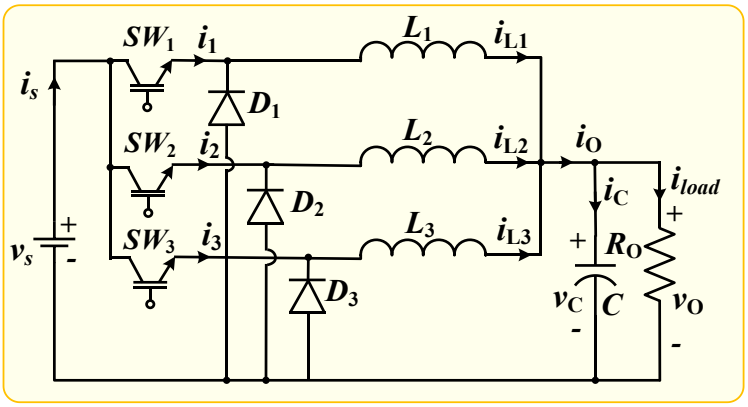


Fig. 4.1 Basic circuit diagram of TPIBC

The operating principle of IBCs is similar to the CBC with certain synchronized operations of parallel branches. Fig. 4.1 shows the structure of TPIBC. The TPIBC mainly comprises a source voltage (v_s) connected to three switches SW_1, SW_2, and SW_3 of three inductor branches comprising L_1, L_2, and L_3, respectively. The freewheeling diodes are D_1, D_2, and D_3.

4.2.1 Classification of Operating Regions of TPIBC

A TPIBC's switching behavior is constantly changing depending on the operational duty ratio. The amount of overlap between neighboring gate pulses varies as the duty ratio rises from zero to unity because the three converter phases are uniformly displaced by one-third of the switching time. This variance results in distinct switching sequences and, as a result, distinct ripple characteristics.

In TPIBC, with respect to complementary switching between switches and respective freewheeling diodes, a total of eight configurations is possible. which can further reduce to four possible modes with the consideration that all three-phases are symmetrical. The characterization of all four modes (i.e., M_0, M_1, M_2, and M_3) is presented in Figs. 4.2 (a)–(d). Three operating regions for TPIBC are defined, where the duty ratio ranges for region-1 (R_1), region-2 (R_2), and region-3 (R_3) are $0 \leq d < 1/3$, $1/3 \leq d < 2/3$, and $2/3 \leq d \leq 1$, respectively [24], as given in Table 4.1.

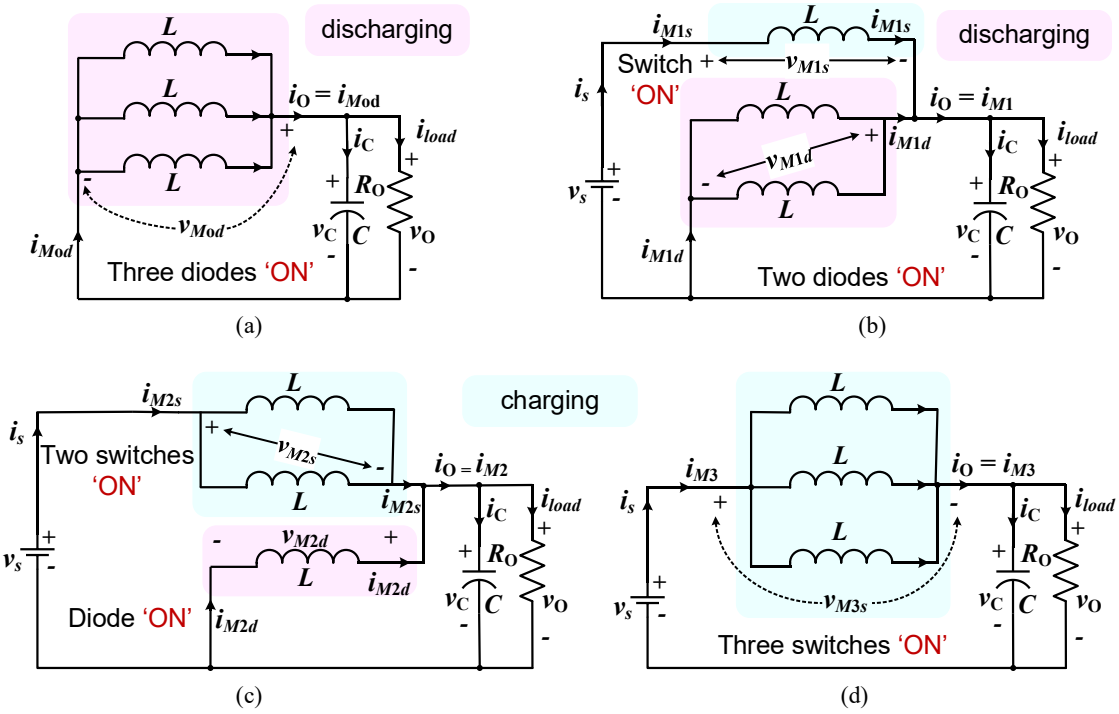


Fig. 4.2 Different modes of operation with combination of ON and OFF conditions of switches and diodes in CCM (a) mode M_0: all switches OFF, (b) mode M_1: one switch ON, (c) mode M_2: two switches ON, and (d) mode M_3: three switches ON.

TABLE 4.1

DIFFERENT OPERATING REGION FOR TPIBC

Range of Duty	Region	Modes and Duration (for TPIBC $n = 3$)	
$0 < d < 1/3$	R_1	M_1	M_0
		dT_s	$\{(1/n)-d\}T_s$
$1/3 < d < 2/3$	R_2	M_2	M_1
		$\{d-(1/n)\}T_s$	$\{(2/n)-d\}T_s$
$2/3 < d < 1$	R_3	M_3	M_2
		$\{d-(2/n)\}T_s$	$\{(3/n)-d\}T_s$

4.2.1.1 Region 0 < D < 1/3

In this operating region each TPIBC phase's conduction interval is less than one-third of the switching duration. As a result, only one TPIBC phase conducts during each switching interval, and the gate pulses of neighboring phases do not overlap. This region

is therefore referred to as the non-overlapping operational region. Only the phase-shifted sum of the individual inductor currents can cause ripple cancellation since the converter phases conduct individually.

4.2.1.2 Region 1/3 < D < 2/3

Adjacent converter phases start to conduct simultaneously for a portion of the switching cycle when the duty ratio surpasses one-third. As a result, two converter phases concurrently transmit energy to the output during an overlapping conduction interval. When compared to Region I, the interaction between the overlapping phase currents greatly alters the ripple characteristics and produces better ripple cancellation.

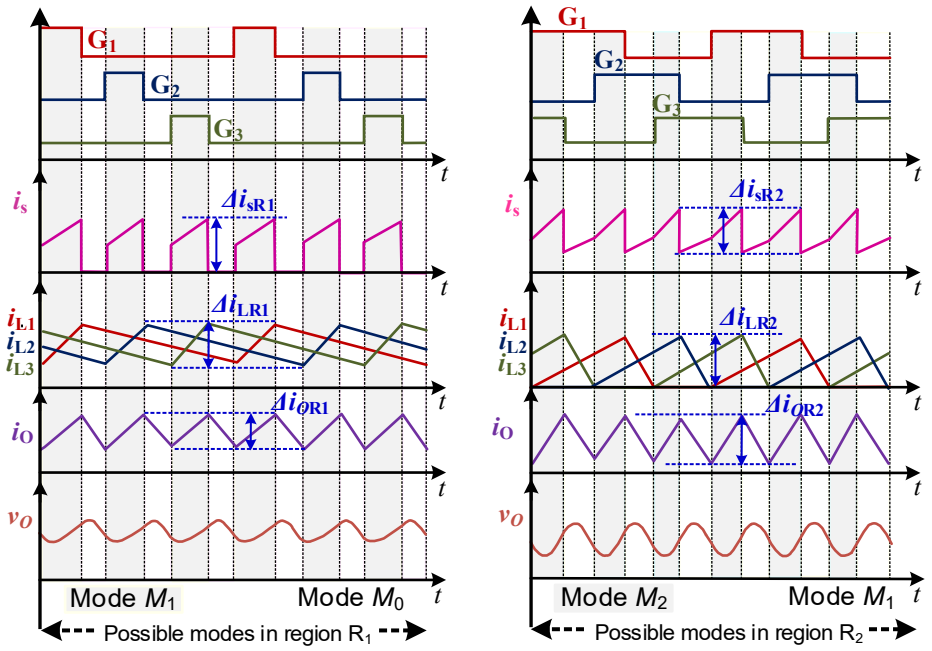
4.2.1.3 Region 1/3 < D < 2/3

When the duty ratio rises above two-thirds, there is enough overlap between neighboring gate pulses for all three converter phases to operate simultaneously for a portion of the switching period. As a result, the converter functions under a distinct conduction pattern that is marked by significant branch current overlap. The ripple characteristics are very different from those seen in the earlier operational regions, even though current sharing is still balanced.

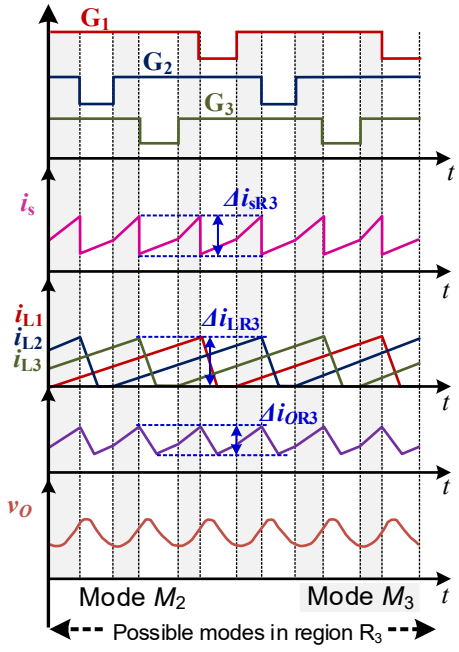
The transition boundaries between neighboring operational regions are represented by the duty ratios D=1/3 and D=2/3. Because they correlate to modifications in the switching sequence and ripple cancellation process, these duty ratios are especially important. These transition points are very desirable operating points for battery charging and other high-performance power conversion applications because they significantly reduce the source current ripple, capacitor current ripple, and output voltage ripple, as will be shown later in this chapter.

4.2.2 Current Conduction Mechanism

The three TPIBC phases' switching sequence and the matching overlap between their conduction intervals control the TPIBC's current conduction mechanism. Throughout the switching cycle, the converter maintains balanced power transmission among the three branches due to the uniform phase displacement of 120°.



(a) (b)



(c)

Fig. 4.3 Characterization of TPIBC under different operating regions(a) R_1: 0 <d< 1/3, (b) R_2: 1/3 <d< 2/3, and(c) R_3: 2/3 <d< 1.

However, various operating areas have different current pathways because the number of concurrently conducting phases varies with the operating duty ratio.

Each region consists of two operating modes, such as R_1 having M_0 (i.e., all switches are OFF) and M_1(i.e., one switch is ON) modes, R_2 having M_1 and M_2(i.e., two switches are ON) modes, and R_3 having M_2 and M_3(i.e., all the three switches are ON) modes for TPIBC, as given in Table 4.2. Further, in this chapter, symmetrical parallel configurations (i.e., $L_1 = L_2 = L_3 = L$) are considered, and the respective four modes of operations (i.e., M_0, M_1, M_2, and M_3) are discussed to get the optimal region of operation. The respective waveforms for different regions under all four modes are presented in Fig. 4.3. The charging and discharging of respective inductor currents are also presented in Table 4.2.

TABLE 4.2

TPIBC CURRENT CHARACTERISTICS UNDER POSSIBLE OPERATING MODES

Operating regions	Switching States						Charging / discharging			Operating modes	Operating regions
	Sw_1	Sw_2	Sw_3	D_1	D_2	D_3	L_1	L_2	L_3		
R_1	OFF	OFF	OFF	ON	ON	ON	↓	↓	↓	M_0	
	OFF	OFF	ON	ON	ON	OFF	↓	↓	↑	M_1	R_2
	OFF	ON	OFF	ON	OFF	ON	↓	↑	↓		
	ON	OFF	OFF	OFF	ON	ON	↑	↓	↓		
R_3	OFF	ON	ON	ON	OFF	OFF	↓	↑	↑	M_2	
	ON	OFF	ON	OFF	ON	OFF	↑	↓	↑		
	ON	ON	OFF	OFF	OFF	ON	↑	↑	↓		
	ON	ON	ON	OFF	OFF	OFF	↑	↑	↑	M_3	

Calculation of the time duration of M_2 during R_2 and R_3 is presented in Fig.4.4 for TPIBC as follows:

$$\Delta t_{M_2}\big|_{R_2} = \left(d - 1/3\right)T_s;\ \ \Delta t_{M_2}\big|_{R_3} = \left(1-d\right)T_s \qquad 4.1$$

where, d is the duty ratio and $T_s = 1/f_s$ is the switching period.

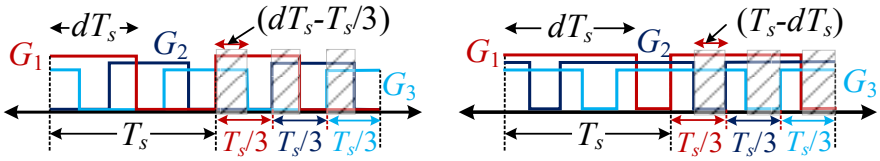


Fig. 4.4 Duration of mode M_2 under region of operation (a) R_2, and (b) R_3.

4.3 Analytical Relation for TPIBC under CCM and DCM for Different Region

Considering the same phase difference between the operating switches, mathematical relations for the characterization of the waveforms in different regions of operation can be developed with respect to the duty ratio for TPIBC. The average output voltage v_{oa} with ideal circuit components under CCM can be written as $d\times V_s$, and under DCM for buck converter, if charging and discharging time is $d\times T_s$ and $d_a\times T_s$ then output voltage can be written as follows:

$$v_{oa} = \frac{v_s d}{d + d_a} \tag{4.2(a)}$$

Further for TPIBC, the average value of output current $i_o|_{avg}$ is the sum of phase inductor currents and it can be written as follows:

$$i_O\big|_{avg} = 3\times i_L\big|_{avg} = \frac{3}{2}\Delta i_L(d + d_1) = \frac{v_{oa}}{R_O} \tag{4.2(b)}$$

$$\Delta i_L = \frac{v_{oa}\times d_a T_S}{L} \tag{4.2(c)}$$

$$d_a^{\,2} + d\times d_a = \frac{2L}{3R_O T_S} = \frac{2Lf_s}{3R_O} \tag{4.2(d)}$$

$$d_a = \frac{-d \pm \sqrt{d^2 + \left(8f_s L/3R_O\right)}}{2} \tag{4.2(e)}$$

Substituting (4.2e) in (4.2a), the average output voltage (v_{oa}) under DCM can be written as follows:

$$v_{oa} = \frac{2v_s d}{d + \sqrt{d^2 + \left(8f_s L/3R_O\right)}} \quad \forall \text{ DCM} \tag{4.3}$$

4.3.1 Region R_1 ($0 < d < 1/3$):

The behavior of output current i_o depends on the continuous and discontinuous conduction of per-phase inductor currents i_L. With respect to the output current i_o, this region can be divided into three sub-regions, such as *(i) SR*-I: both i_o and i_L are continuous under M_0 and M_1 modes of operation and the value of Δi_o can be derived as (4.5); *(ii) SR*-II: i_o is continuous and i_L is discontinuous; and *(iii) SR*-III: both i_o and i_L are discontinuous. The values of Δi_o under regions *SR*-II and *SR*-III can be derived as (4.7), where the negative values of $\Delta\psi_1$, $\Delta\psi_2$, $\Delta\psi_3$ are considered zero. The characterization of output current i_o under regions *SR*-II and *SR*-III with respect to inductor currents is shown in Fig. 4.5.

$$\Delta i_{M_1S} = \frac{d\left(v_s - v_{oa}\right)}{f_S L}; \quad \Delta i_{M_1d} = \frac{2 \times v_{oa} d}{f_S L}; \tag{4.4}$$

$$\Delta i_{OR_1} = \Delta i_{M_1S} - \Delta i_{M_1d} = \Delta i_{M_0d} = \frac{dv_s\left(1-3d\right)}{f_S L} \quad \forall \text{CCM}. \tag{4.5}$$

$$d' = d\left(v_S - v_{oa}\right)/v_{oa}; \tag{4.6}$$

$$\Delta i_{OR_1} = \begin{cases} \Delta\psi_1, \ \forall \dfrac{2}{3} < d' \le \left(1-d\right) \& \, d_1 = d; \\ \Delta\psi_1 + \Delta\psi_2, \forall \dfrac{2-3d}{3} < d' \le \dfrac{2}{3} \begin{cases} d_1 = d + d' - 2/3, \\ d_2 = \left(2-3d'\right)/3; \end{cases} \\ \Delta\psi_2, \forall \dfrac{1}{3} < d' \le \dfrac{2-3d}{3} \& \, d_2 = d; \\ \Delta\psi_2 + \Delta\psi_3, \forall \dfrac{1-3d}{3} < d' \le \dfrac{1}{3} \& \begin{cases} d_2 = d + d' - 1/3, \\ d_3 = \left(1-3d'\right)/3; \end{cases} \\ \Delta\psi_3, \forall d' \le \dfrac{1-3d}{3} \& \, d_3 = d. \end{cases} \tag{4.7(a)}$$

where,

$$\Delta\psi_1 = \frac{v_s - 3v_{oa}}{f_S L} d_1; \Delta\psi_2 = \frac{v_s - 2v_{oa}}{f_S L} d_2; \Delta\psi_3 = \frac{v_s - v_{oa}}{f_S L} d_3 \tag{4.7(b)}$$

The input current ripple Δi_S can be calculated with consideration of lossless TPIBC under CCM, DCM and the ripple in the inductor currents in any region Δi_L within the individual phase can be written as in (4.8) and (4.9), respectively.

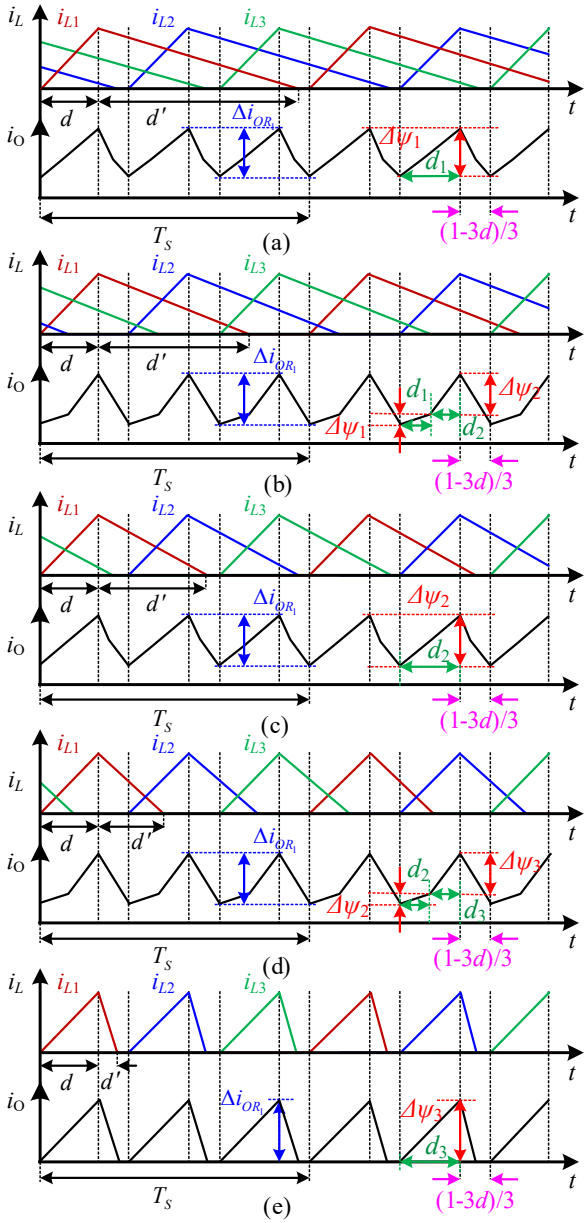


Fig. 4.5 Characterization of TPIBC output current i_o with respect to each phase inductor current i_{L1}, i_{L2}, and i_{L3} under region R_1 and sub-regions *SR*-II and *SR*-III for DCM of operation with (a), (b), (c), (d), and (e) representing all the five possible durations of the inductor discharging period.

The critical value of inductor L_{CR1}can be designed for continuous output current Δi_o in region R_1, and the performance of the converter at fixed average output voltage and with range of charging power level using TPIBC can be evaluated in (4.10) and (4.11), respectively. The critical value of inductor L_c' can be designed for continuous inductor

current i_L in any region can be written as in (4.12). Whereas, due to the overlapping modes of inductor charging regions in R_2 and R_3, the output currents Δi_O in both the modes are continuous.

$$\Delta i_{SR_1} = v_s d\left(\frac{1}{3R_O} + \frac{(1-d)}{2f_S L}\right) \quad \forall \text{ CCM;} \tag{4.8(a)}$$

$$\Delta i_S = \frac{d\left(v_s - v_{oa}\right)}{f_S L}, \ \forall \text{all regions under DCM of } i_L. \tag{4.8(b)}$$

$$\Delta i_L = \frac{d\left(v_s - v_{oa}\right)}{f_S L}, \ \forall \text{all regions in CCM or DCM.} \tag{4.9}$$

$$L_{CR_1} \geq \underbrace{\frac{\left(v_s - v_{oa}\right)d}{v_{oa}}}_{d' \geq (1/3-d),\ \forall \text{continuous } \Delta i_{OR_1}} \times \frac{R_O}{2f} = \frac{(1-3d)R_O}{6f_s}, \ \forall \text{ CCM} \tag{4.10}$$

$$P_{oR_1} \geq \frac{{v_{oa}}^2(1-3d)}{6f_S L_{CR_1}} \quad \forall \text{ CCM} \tag{4.11}$$

$$L_C' \geq \frac{3(1-d)R_O}{2f_s} \quad \forall \text{ continuous inductor current} \tag{4.12}$$

4.3.2 Region R_2 ($1/3 < d < 2/3$):

In this region the switches operate in overlapping condition under M_1 and M_2 modes of operation during continuous inductor currents. The value of Δi_o is derived and presented in (4.14). Similar to the region R_1, the relation for Δi_{oR2} is derived with respect to discontinuous value of inductor currents and the value of d' as given in (4.15). The negative values of $\Delta\gamma_1$, $\Delta\gamma_2$, and $\Delta\gamma_3$ are considered to be zero. The characterization of output current i_o under region *SR*-II with respect to inductor currents is shown in Fig. 4.6.

$$\Delta i_{M_2S} = \frac{2\left(d-1/3\right)\left(v_s - v_{oa}\right)}{f_S L}; \Delta i_{M_2d} = \frac{v_{oa}\left(d-1/3\right)}{f_S L}; \tag{4.13}$$

$$\Delta i_{OR_2} = \begin{matrix} = \left|\Delta i_{M_2S} - \Delta i_{M_2d}\right| \\ = \left|\Delta i_{M_1d} - \Delta i_{M_1S}\right| \end{matrix} = \frac{v_s\left(d-1/3\right)\left(2-3d\right)}{f_S L}. \tag{4.14}$$

$$\Delta i_{OR_2} = \begin{cases} \Delta\gamma_1, \forall \dfrac{1}{3} < d' \le (1-d) \,\&\, d_1 = d - 1/3; \\ \Delta\gamma_1 + \Delta\gamma_2, \forall \dfrac{2-3d}{3} < d' \le \dfrac{1}{3} \,\&\, \begin{cases} d_1 = d + d' - 2/3, \\ d_2 = (1-3d')/3; \end{cases} \\ \Delta\gamma_2 + \Delta\gamma_3, \forall d' \le \dfrac{2-3d}{3} \,\&\, \begin{cases} d_2 = d - 1/3, \\ d_3 = d + d' - 2/3; \end{cases} \end{cases} \quad \text{4.15(a)}$$

where,

$$\Delta\gamma_1 = \frac{2v_s - 3v_{oa}}{f_S L} d_1; \Delta\gamma_2 = \frac{2(v_s - v_{oa})}{f_S L} d_2; \Delta\gamma_3 = \frac{v_s - v_{oa}}{f_S L} d_3 \quad \text{4.15(b)}$$

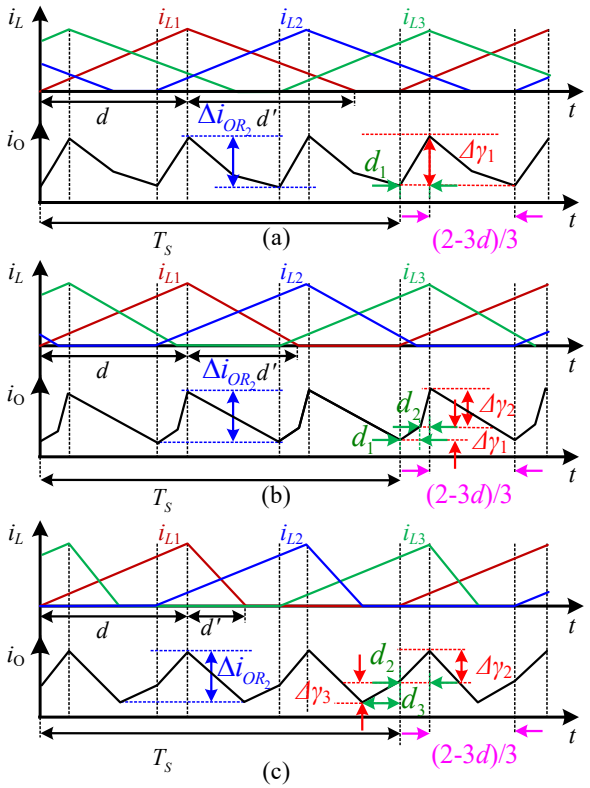


Fig. 4.6 Characterization of output current i_o with respect to each phase inductor current i_{L1}, i_{L2}, and i_{L3} under region R_2 and sub-region *SR*-II for DCM operation with (a), (b), and (c) representing all the three possible durations of the inductor discharging period.

4.3.3 Region R3 (2/3 <*d*< 1):

In this region the switches operate in overlapping condition under M_2 and M_3 modes of operation during continuous inductor currents. The value of Δi_o is derived and presented in (4.17). Similar to the region R_1, the relation for Δi_{oR3} is derived with respect to discontinuous values of inductor currents and the value of d' as given in (4.18). The negative values of $\Delta\varepsilon_1$, $\Delta\varepsilon_2$, are considered to be zero. The characterization of output current i_o under region *SR*-II with respect to inductor currents is shown in Fig. 4.7.

$$\Delta i_{M_2S} = \frac{2v_S(1-d)^2}{f_S L};\ \Delta i_{M_2d} = \frac{v_{oa}(1-d)}{f_S L}; \tag{4.16}$$

$$\Delta i_{OR_3} = \left|\Delta i_{M_3S}\right| = \left|\Delta i_{M_2S} - \Delta i_{M_2d}\right| = \frac{v_S(1-d)(3d-2)}{f_S L}. \tag{4.17}$$

$$\Delta i_{OR_3} = \Delta\varepsilon_1 + \Delta\varepsilon_2,\ \forall d' \le (1-d)\ \&\ \begin{cases} d_1 = d - 2/3, \\ d_2 = 1-(d+d'); \end{cases} \tag{4.18(a)}$$

$$\Delta i_{OR_3} = \Delta\varepsilon_1 + \Delta\varepsilon_2,\ \forall d' \le (1-d)\ \&\ \begin{cases} d_1 = d - 2/3, \\ d_2 = 1-(d+d'); \end{cases} \tag{4.18(b)}$$

The average values of currents can also be calculated in DCM and CCM with respect to derived current ripples. The performance of TPIBC can be evaluated for the same load with a different duty ratio. The derived results are able to design and develop the TPIBC with respect to minimum current ripples and to reduce the total loss components.

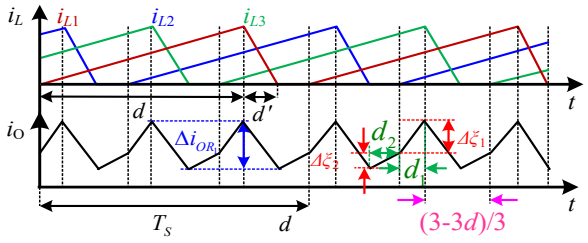


Fig.4.7 Characterization of output current i_o with respect to each phase inductor current i_{L1}, i_{L2}, and i_{L3} under region R_3 and sub-regions *SR*-II for DCM operation.

4.4 Output Ripple Current for various types of Loads.

4.4.1 Resistive Load

The variation of output ripple current with respect to change in duty ratio for resistive load is plotted in Fig. 4.8 for single-phase buck converter using $\Delta i_O = dv_s(1\text{-}d)/f_sL$ and TPIBC under CCM for regions R_1, R_2, and R_3 using equation (4.5), (4.14) and (4.17), respectively. It shows that the peak ripple current for single-phase buck converter is much higher than TPIBC. Also, the ripple current for TPIBC is maximum in the mid operating region of the duty, i.e., $d = l/(2\times n)$ and minimum in transition operating region of the duty, i.e., $d = l/n$ where l = 1, 2, 3 for TPIBC.

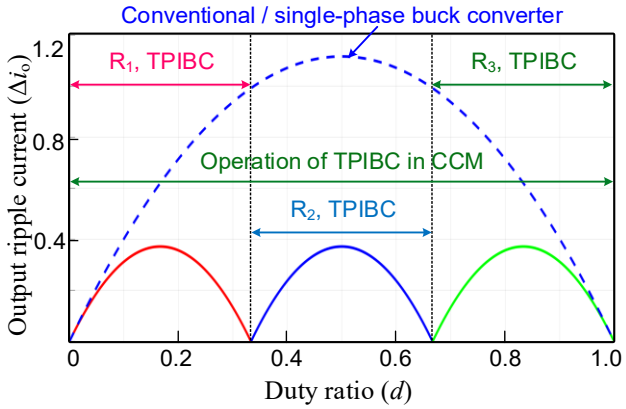


Fig. 4.8 Characterization of output ripple current(Δi_O) with respect to duty ratio (d) under different operating regions for buck converter and TPIBC with resistive load and CCM branch inductor current.

4.4.2 Constant Power Load

The two different cases of variation of output ripple current with respect to change in duty ratio for constant power loads of 37.5 W and 12.5 W are shown in Figs. 4.9 and 4.10, respectively. Since the operation is performed from a lower duty to a higher duty ratio for TPIBC, i.e., ideally the voltage gain is from zero to one, the small power ratings (i.e., constant power loads of 37.5 W and 12.5 W are selected to meet the current rating of the semiconductor switches during experimental results at lower duty. It is observed that the variation of ripple current in CCM i.e., black dotted lines in Figs. 4.9 and 4.10 in any region of operation is similar to the resistive load i.e., Fig. 4.8, whereas in DCM the variation of output current ripple changes in comparison to CCM with variation in duty, and it also depends upon the power rating of constant power. load.

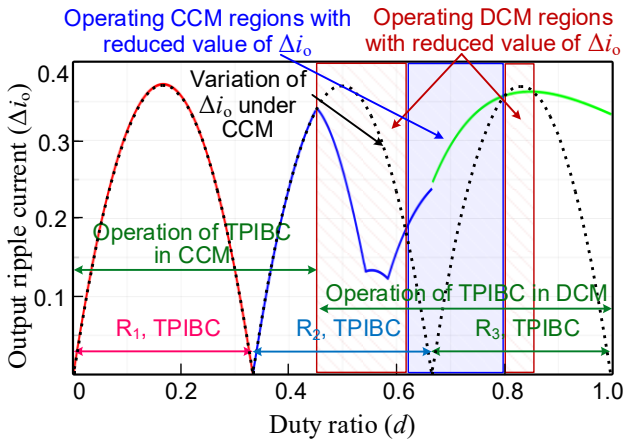


Fig. 4.9 Characterization of output ripple current(Δi_O) with respect to duty ratio (d) under different operating regions for TPIBC at constant output power of 37.5 W in CCM and DCM of branch inductor currents.

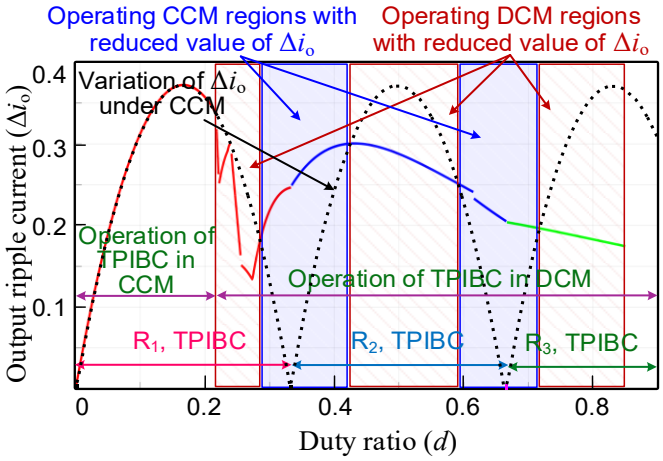


Fig. 4.10 Characterization of output ripple current(Δi_O) with respect to duty ratio (d) under different operating regions for TPIBC at constant output power of 12.5 W in CCM and DCM of branch inductor currents.

4.5 TPIBC Loss and Efficiency Analysis

Loss estimation is a critical aspect in evaluating the performance and efficiency of TPIBC, especially under various regions of operation. Among the different types of losses, conduction loss and switching loss are the most significant contributors to the overall power loss in the system. Switching losses are associated with the dynamic behavior of power switches during turn-on and turn-off transitions, and influenced by factors such as switching frequency, voltage, and current slew rates. On the other hand, conduction losses

primarily arise due to the resistive elements in the circuit, such as the on-state resistance of high-frequency switches and the ESR of inductors and capacitors, and they are directly related to the rms value of current flowing through these components. The efficiency of the converter depends on the balance between switching and conduction losses, which vary with changes in load conditions, duty cycle, and input / output voltage levels. A comprehensive loss calculation under these varying operational regions is essential for optimal converter design and thermal management, ensuring high efficiency and reliable performance.

4.5.1 Switching loss of individual switches

To reduce the size of circuit passive components and improve the performance of the converters, the high switching frequency operation of the converter is chosen. Whereas, due to the increase in switching frequency, the switching losses of the converter play a dominant role in the total losses of the converter. The estimation of switching loss is essential for the prediction of junction temperature and the overall efficiency of the power converter. The switching diagram of each IGBT of the proposed TPIBC is shown in Fig. 4.11, where t_r and t_f are the rise-time and fall-time during turn-on and turn-off of the switch, respectively. The maximum voltage across the switch is $V_{Sw} \approx v_S$.

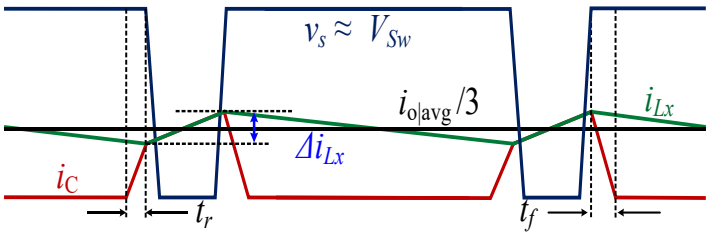


Fig. 4.11 Switching behavior and loss calculation.

The range of branch inductor current magnitude is varied between $i_{Lx\ min}$ and $i_{Lx\ max}$, as shown in Fig. 4.11. The switching power loss (P_{Sw}) with respect to turn-on and turn-off time can be calculated for the xth branch of the inductor current of TPIBC, where x= 1, 2, and 3 for TPIBC. Fig. 4.11 shows the transition of voltage from V_S to 0 during turn-on (t_r) and from 0 to V_S during turn-off (t_f). The inductor current through each switch remain approximately constant and varies between minimum inductor current, $i_{Lx\ min}$ at turn-on and maximum inductor current at turn-off, $i_{Lx\ max}$ can be written for TPIBC as follows:

$$i_{L_{x\min}} = \left(\frac{i_O|_{avg}}{3} - \frac{\Delta i_{Lx}}{2} \right); \text{ and } i_{L_{x\max}} = \left(\frac{i_O|_{avg}}{3} + \frac{\Delta i_{Lx}}{2} \right) \quad 4.19$$

Switching energy loss (E_{Sw}) during switching transition is the integral of instantaneous power during the transition that during turn-on switching energy loss (E_{Sw_ON}) and turn-off switching energy loss (E_{Sw_OFF}) as follows:

$$E_{Sw_ON} = \int_0^{t_r} v_S \left(1 - \frac{t}{t_r}\right) \left(\frac{i_O|_{avg}}{3} - \frac{\Delta i_{Lx}}{2} \right) dt \quad 4.20(a)$$

$$E_{Sw_ON} = v_S \left(\frac{i_O|_{avg}}{3} - \frac{\Delta i_{Lx}}{2} \right) \left(\frac{t_r}{2} \right) \quad 4.20(b)$$

$$E_{Sw_OFF} = \int_0^{t_f} v_S \left(1 - \frac{t}{t_f}\right) \left(\frac{i_O|_{avg}}{3} + \frac{\Delta i_{Lx}}{2} \right) dt \quad 4.21(a)$$

$$E_{Sw_OFF} = v_S \left(\frac{i_O|_{avg}}{3} + \frac{\Delta i_{Lx}}{2} \right) \left(\frac{t_f}{2} \right) \quad 4.21(b)$$

The switching power loss (P_{Sw}) can be calculated using energy loss per switching cycle as follows:

$$P_{Sw} = f_S \times \left(E_{Sw_ON} + E_{Sw_OFF} \right) \quad 4.22(a)$$

$$P_{Sw} = \frac{v_S}{2} f_S \left(\left(\frac{i_O|_{avg}}{3} - \frac{\Delta i_{Lx}}{2} \right) \times t_r + \left(\frac{i_O|_{avg}}{3} + \frac{\Delta i_{Lx}}{2} \right) \times t_f \right) \quad 4.22(b)$$

$$P_{Sw} = \frac{v_S}{2} f_S \left(\left(\frac{2i_O|_{avg} - 3\Delta i_{Lx}}{6} \right) \times t_r + \left(\frac{2i_O|_{avg} + 3\Delta i_{Lx}}{6} \right) \times t_f \right) \quad 4.22(c)$$

$$P_{Sw} = \frac{v_S \times f_S}{12} \times \left\{ 2\, i_O|_{avg} \left(t_f + t_r \right) + 3\Delta i_{Lx} \left(t_f - t_r \right) \right\} \quad 4.22(d)$$

$$P_{Sw} = \frac{v_S \times i_O|_{avg} \times f_S}{6} \left(t_f + t_r \right) + \underbrace{\frac{v_S \times \Delta i_{L_x} \times f_S}{4} \left(t_f - t_r \right)}_{\text{loss component due to ripple}} \quad 4.22(e)$$

$$\text{where, } \Delta i_{L_x} = \frac{\left(v_S - v_{oa} \right) v_{oa}}{v_S f_S L} \quad 4.23$$

The individual switching loss of TPIBC is plotted with respect to variation in duty ratio using (4.22), as shown in Figs. 4.12(a) and 4.12(b) at 37.5W and 12.5W with constant power loads, respectively. It can be seen that the switching loss reduces with an increase in duty ratio, and there is further reduction in switching losses after transitioning from the CCM to the DCM mode of operation in various operating regions.

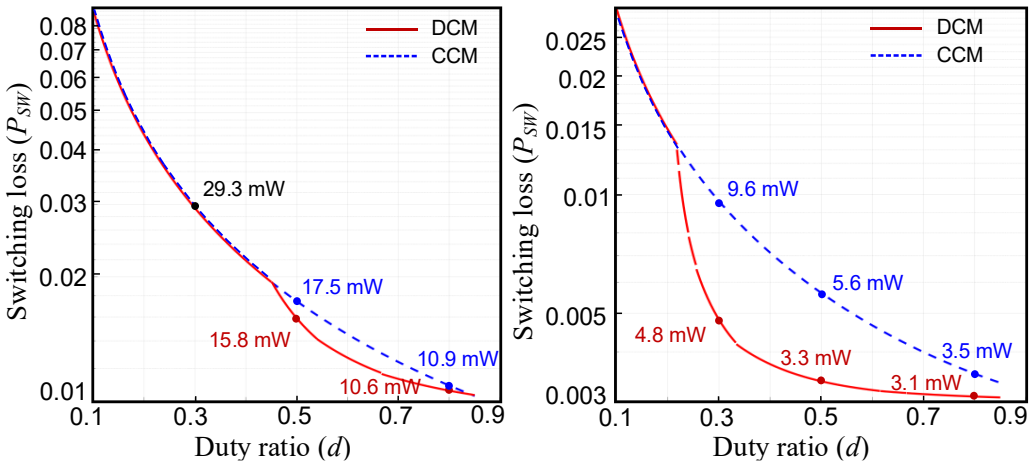
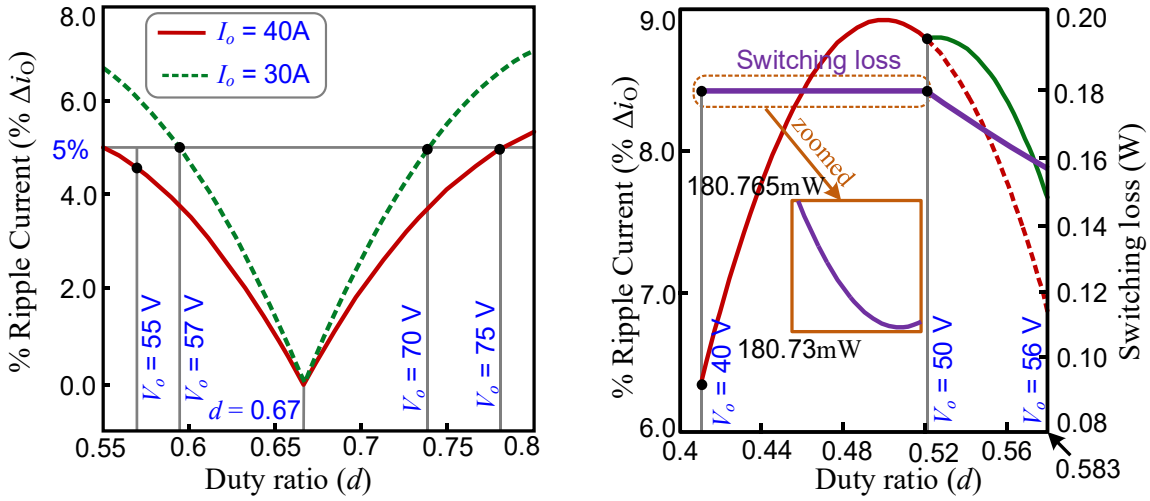


Fig. 4.12 Variation in individual switching loss (P_{Sw}) with respect to duty ratio for TPIBC under different operating region for constant power loads at (a) 37.5W and (b) 12.5W.

Figs. 4.13 (a) and (b) represent the percentage output current ripple of TPIBC for the applications shown Chapter 1 i.e., electrolyzer for hydrogen generation at 55V-75V, constant current of 40A, and peak power of 3 kW, and battery charging at 48 V nominal, 8A maximum charging current, 100Ah, respectively. Since the dc power quality, i.e., current ripple for the electrolyzer, is less than 5% to lower the energy consumption of the electrolyzer and optimize the aging [7], therefore the duty range is selected as 0.573 to 0.781 for a voltage range of 55V to 75V from the 96V input dc bus voltage at peak power of 3kWp. For the safe limit of output current ripple, the TPIBC is designed and the value of inductor L_{elect} = 180µH is used. The same converter can be used for a 2.1kWp peak power application under a safe limit of output current ripple with the modified range of duty ratio and respective voltage range of 57V to 70V. The characteristics of percentage output current ripple for electrolyzers at 3kWp and 2.1kWp are presented in Fig. 4.13 (a) in red and dotted green, respectively. Fig. 4.13 (b) shows the behavior of percentage ripple

current with constant current charging of battery from 40V-50V range and constant power from 50V-56V duty range.



(a) (b)

Fig. 4.13 Variation of percentage output current ripple (%Δi_o) with respect to duty ratio for TPIBC under different operating regions for (a) electrolyzer at constant current ratings of 40A and 30A, (b) battery charging with constant current charging at 8A and constant power of 375 W.

4.5.2 Conduction Loss of individual switches:

In a TPIBC, the interleaving technique helps to distribute the current across multiple phases, thereby reducing ripple current and minimizing conduction losses. Each individual switches conduct for the time equal to duty cycle and the current through each switch is equal to the branch inductor current, i_{Lx} which is a triangular waveform oscillating around the average output current with peak-to-peak ripple as given in (4.19). The rms value of current over conduction period $d \times T_S$.

$$i^2_{xrms} = d\left(\frac{\left(i_O|_{avg}\right)^2}{9} + \frac{\left(\Delta i_{Lx}\right)^2}{12}\right) \qquad 4.24(a)$$

$$i^2_{xrms} = d \times \left(i_O|_{avg}\right)^2 \left(\frac{1}{9} + \frac{1}{12}\left(\frac{\Delta i_{Lx}}{i_O|_{avg}}\right)^2\right) \qquad 4.24(b)$$

The conduction loss of individual switches (P_{CR}) due to on state resistance (R_{SW_ON}) is expressed as follows:

$$P_{\mathrm{CR}} = R_{\mathrm{SW_ON}} \times d \times \left(i_O \big|_{avg} \right)^2 \left(\frac{1}{9} + \frac{1}{12} \left(\frac{\Delta i_{Lx}}{i_O \big|_{avg}} \right)^2 \right) \tag{4.25}$$

The conduction loss of individual switches (P_{CVS}) due to on-state voltage of the switch (v_{SW}) is expressed as follows

$$P_{\mathrm{CVS}} = \frac{d \times i_O \big|_{avg} \times v_{SW}}{3} \tag{4.26}$$

The conduction loss of individual diodes (P_{CVD}) due to on state voltage drop (v_{D}) is expressed as follows:

$$P_{\mathrm{CVD}} = \frac{\left(1-d\right) \times i_O \big|_{avg} \times v_D}{3} \tag{4.27}$$

Similarly, the conduction loss due to ESR of inductor (R_{L}) of each branch of TPIBC is expressed as follows:

$$P_{\mathrm{CER}} = R_L \times d \times \left(i_O \big|_{avg} \right)^2 \left(\frac{1}{9} + \frac{1}{12} \left(\frac{\Delta i_{Lx}}{i_O \big|_{avg}} \right)^2 \right) \tag{4.28}$$

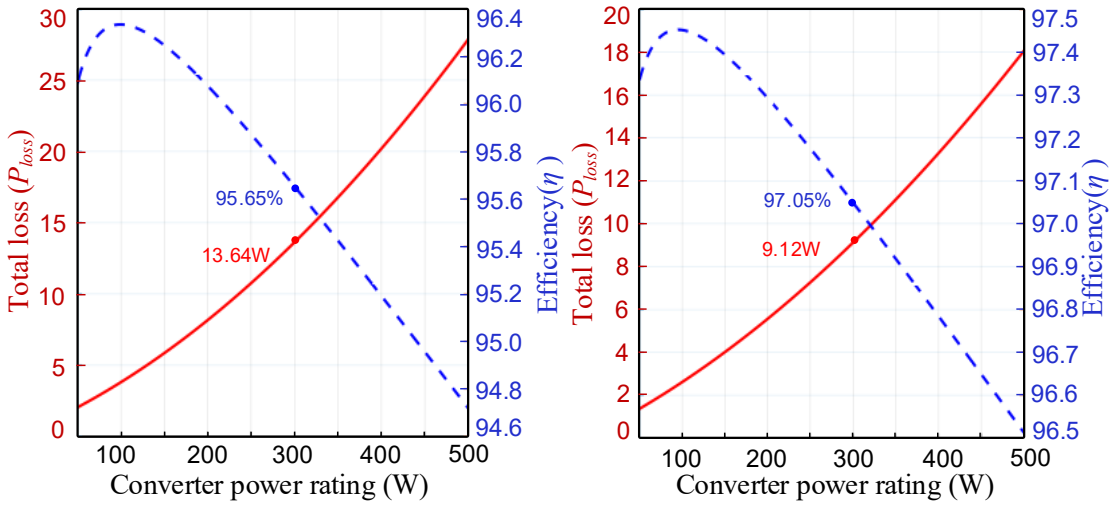
Thus, total loss of TPIBC (P_{loss}) and efficiency (η) can be written as follows:

$$P_{loss} = 3 \times (P_{Sw} + P_{\mathrm{CR}} + P_{\mathrm{CVS}} + P_{\mathrm{CVD}} + P_{\mathrm{CER}}) \tag{4.29}$$

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \% \tag{4.30}$$

Considering the value of ESR of inductors, R_{L}= 0.45Ω, power IGBT on-state resistance, $R_{\mathrm{SW_ON}}$ = 0.08Ω, forward voltage drop v_{SW} = 1.5V and power diode forward voltage drop v_D =1.3V, input voltage fixed at v_S = 96V with duty ratio d = 0.78, the total power loss and efficiency of TPIBC for has been plotted with respect to varying output power and it is seen that for 300W output power, the total losses in TPIBC is 13.64W (i.e., 95.65 % efficiency) at d = 0.57 and 9.12W (i.e., 97.05% efficiency) at d = 0.78, as shown

in Fig. 4.14. It is evident that for same power output the losses and efficiency changes with change in region of operation.



(a) (b)

Fig. 4.14 Variation in total loss (P_{loss}) with respect to output power for TPIBC under different operating individual region (a) R_2: $d = 0.58$ and (b) R_3: $d = 0.78$.

4.6 Experimental Validation

A laboratory prototype setup for TPIBC is developed for performance evaluation under fixed output load power and fixed resistive load at different duty ratios. The analytical results are tested at a 50-V input supply voltage.

Fig. 4.15 depicts the experimental setup of TPIBC, comprising three main stages: (a) the power stage, which includes power IGBTs K75T60A, power diodes RHRP30120, energy transfer ferrite bobbin core inductors connected in each phase, and a filter capacitor; (b) the digital signal processing board LAUNCHXL-F28379D, which provides the gating pulse; and (c) the driver circuitry, designed to supply power IGBTs. The various devices for measuring circuit characteristics are used, such as differential voltage probes, current probes, and a mixed signal oscilloscope (MSO) to capture the waveforms.

The circuit is tested for the fixed load powers, i.e., P_L = 37.5W and 12.5W at a switching frequency of 20kHz under normal circuit operation in non-overlapping and overlapping conditions. Accordingly, the circuit components are calculated such that the values of inductors $L_1 = L_2 = L_3 = 560\mu H$ and $C = 1.86\mu F$. Ideally, the designed value of inductors is exactly equal, and the ESR is negligible. Whereas, during the hardware

design, it was carefully investigated that the designed values of phase branch inductors (L_x) and their parasitic ESR (R_{Lx}) have a slight variation [34]. However, the nearest values of branch inductors have been considered for the analysis, which is based on design and availability. Also, the other circuit parasitic components, such as on-state voltage drops across the switches and diodes, are considered ideal.

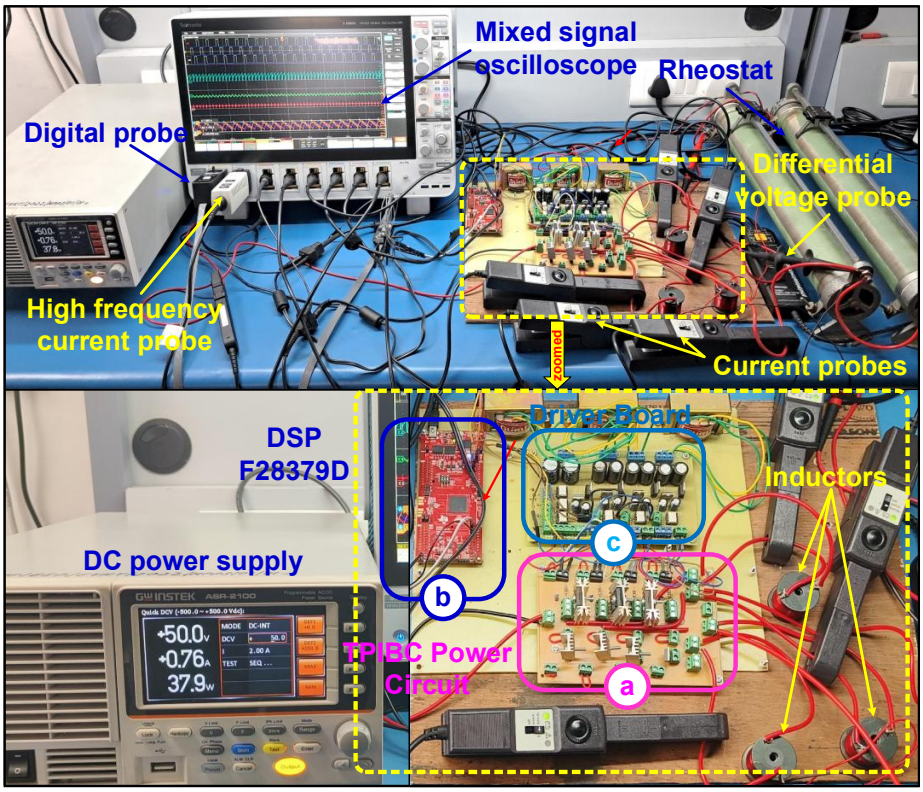


Fig. 4.15 Experimental setup for TPIBC.

Figs. 4.16 and 4.17 show the simulation results of TPIBC for the same parameter mentioned above. Fig. 4.16 shows the simulation result for the designed TPIBC being operated for varying duty ratio with fixed resistive load for $R_O = 6\Omega$ and Fig. 4.17 shows the simulation result for varying duty ratio with fixed power $P_L = 37.5$W. It is seen that voltage and current vary linearly for fixed resistive load and non-linear for fixed power load.

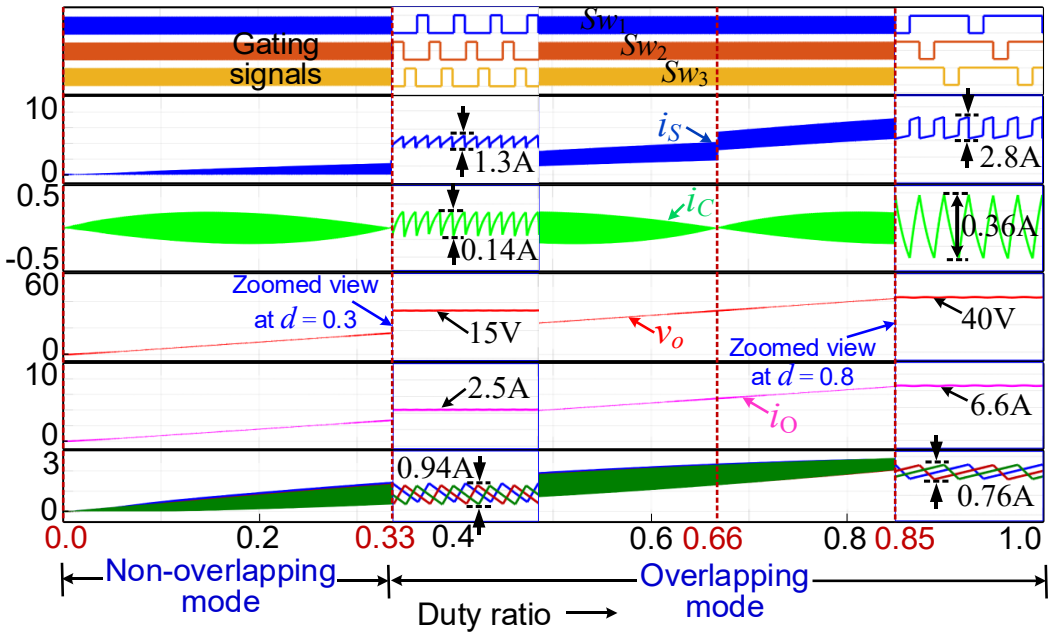


Fig. 4.16 Simulation result of TPIBC with respect to varying duty ratio at fixed resistive load $R_O = 6\Omega$.

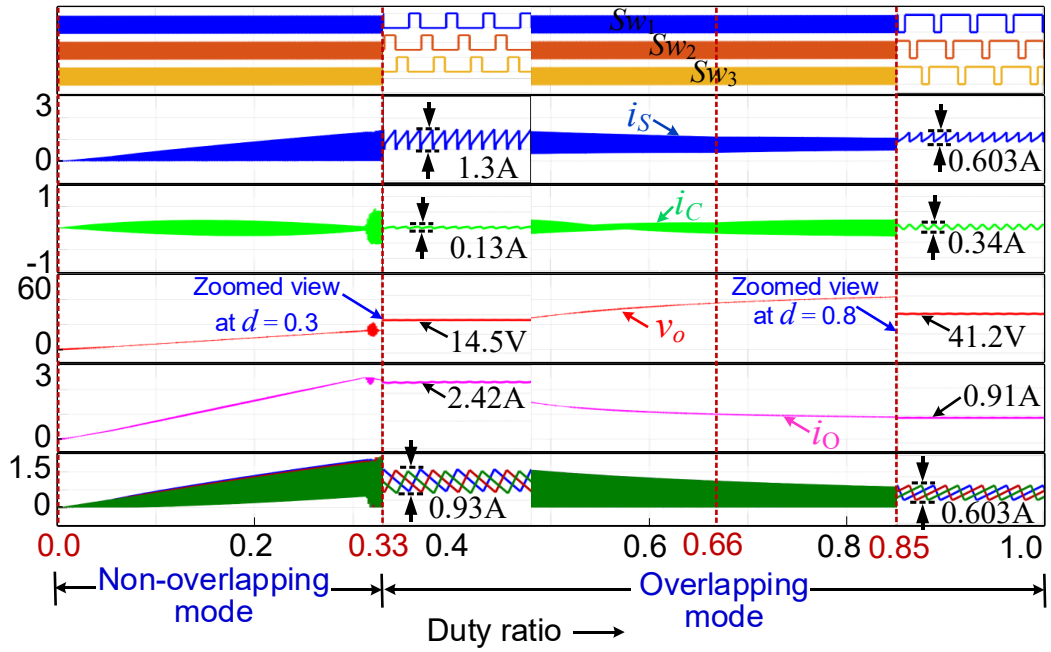


Fig. 4.17 Simulation result of TPIBC with respect to varying duty ratio at constant power load $P_L = 37.5$W.

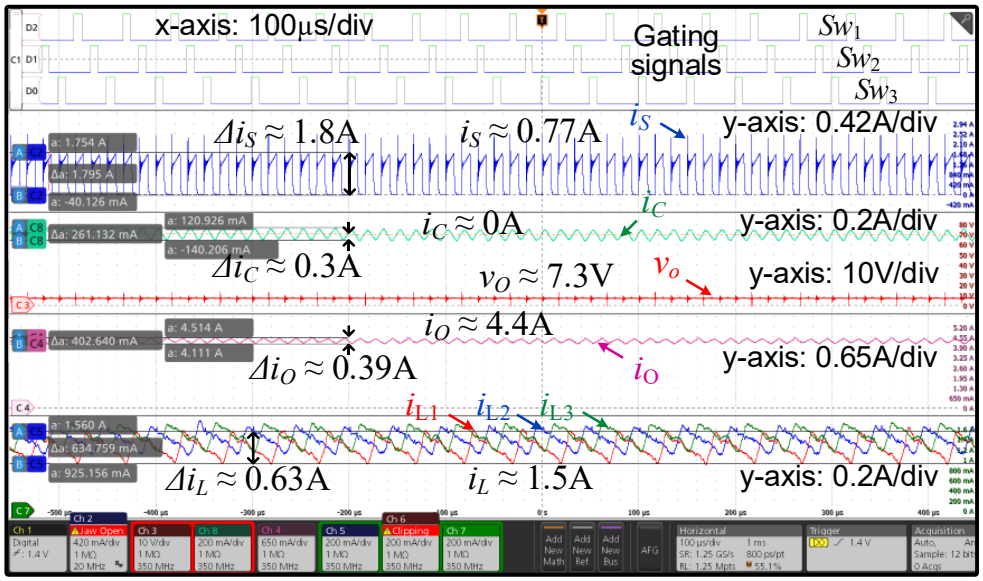


Fig. 4.18 Performance evaluation of TPIBC with constant power load P_L = 37.5W under different operating region R_1 at d = 0.16.

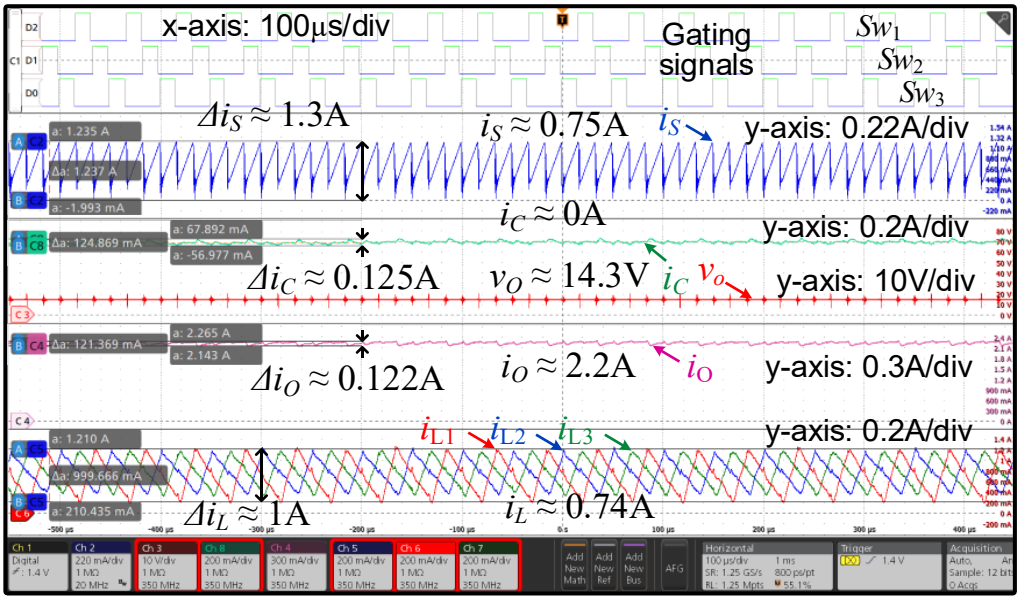


Fig. 4.19 Performance evaluation of TPIBC with constant power load P_L = 37.5W under different operating region R_1 at d = 0.3.

Fig. 4.18 to Fig. 4.21 shows the behaviour of TPIBC with constant power load of P_L = 37.5W at different duty regions ranging from d = 0.16 in region R_1 to d = 0.83 in region, R_3. The result in Fig. 4.18 shows that the value of v_{oa} is equal to $d \times v_s$ for CCM and higher than $d \times v_s$ for DCM from Fig. 4.21. The duty ratio to evaluate the performance of TPIBC

is chosen such that it is in the centre of all three regions of operation, i.e., 0.16 (within the non-overlapping region $0 \leq d \leq 1/3$), 0.5 (within the overlapping region $1/3 \leq d \leq 2/3$), and 0.83 (within the overlapping region $2/3 \leq d \leq 1$).

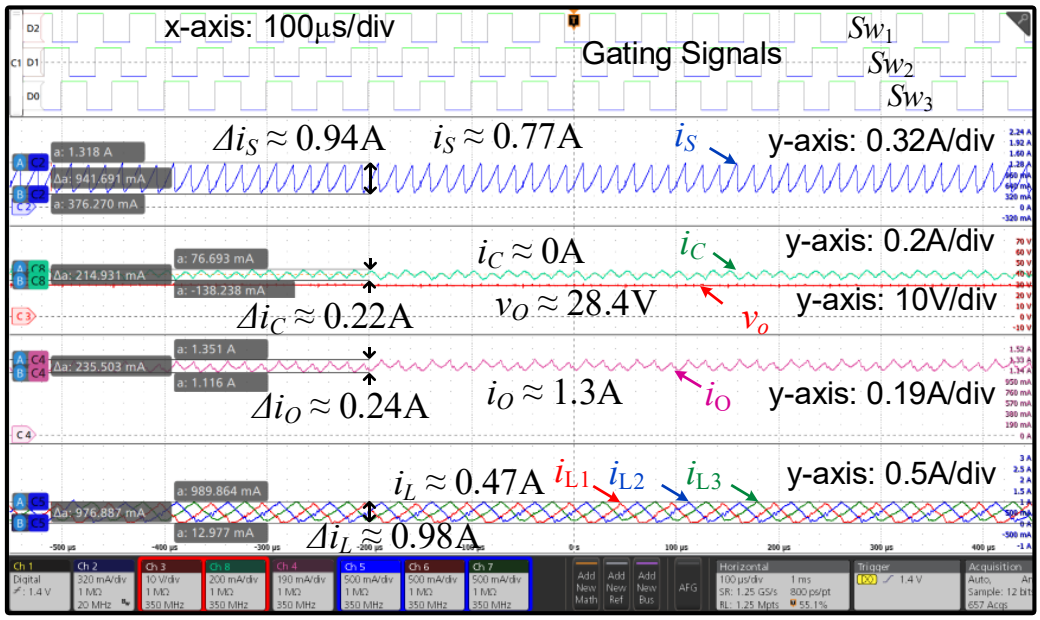


Fig. 4.20 Performance evaluation of TPIBC with constant power load P_L = 37.5W under different operating region R_2 at d = 0.5.

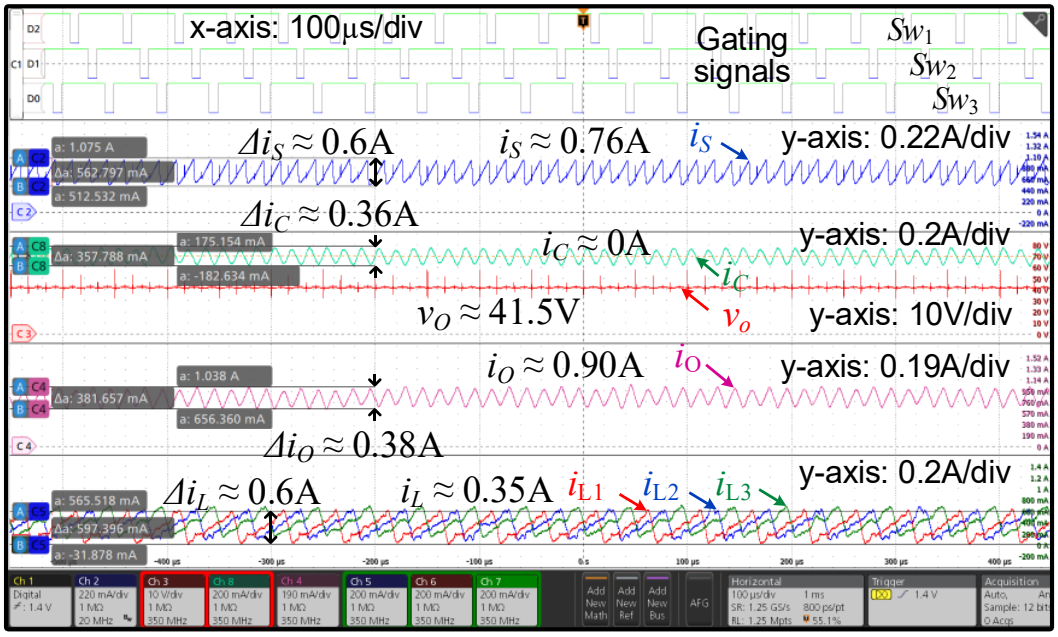


Fig. 4.21 Performance evaluation of TPIBC with constant power load P_L = 37.5W under different operating region R_3 at d = 0.83.

The behaviour of the output current ripple shown in Fig. 4.18 is similar to the analytical results presented in Fig. 4.9 under CCM and DCM of operation with same system parameters such that at d = 0.16, $\Delta i_O \approx$ 0.39A, at d = 0.3, $\Delta i_O \approx$ 0.122A, at d =0.5, $\Delta i_O \approx$ 0.24A, at d = 0.83, $\Delta i_O \approx$ 0.38A. In Figs. 4.18, 4.20 and 4.21, the values of Δi_O are 0.39A, 0.24A, and 0.38A, respectively, which is nearly equal to 10%, 20%,and 40% of their average output currents in the respective regions. Fig. 4.19 shows the operation of TPIBC at d = 0.3 in CCM. The output voltage is approximately equal to $d \times v_s$ and the value of $\Delta i_O \approx 0$. Fig. 4.20 and Fig. 4.22 are captured at d = 0.5 at different power levels i.e., P_L= 37.5W and 100 W, respectively. It shows that the percentage value of output ripple current, Δi_O with respect to output current, i_O is 18% in the DCM at P_L= 37.5W which is higher than Δi_O 10% of i_O under CCM at P_L = 100W.

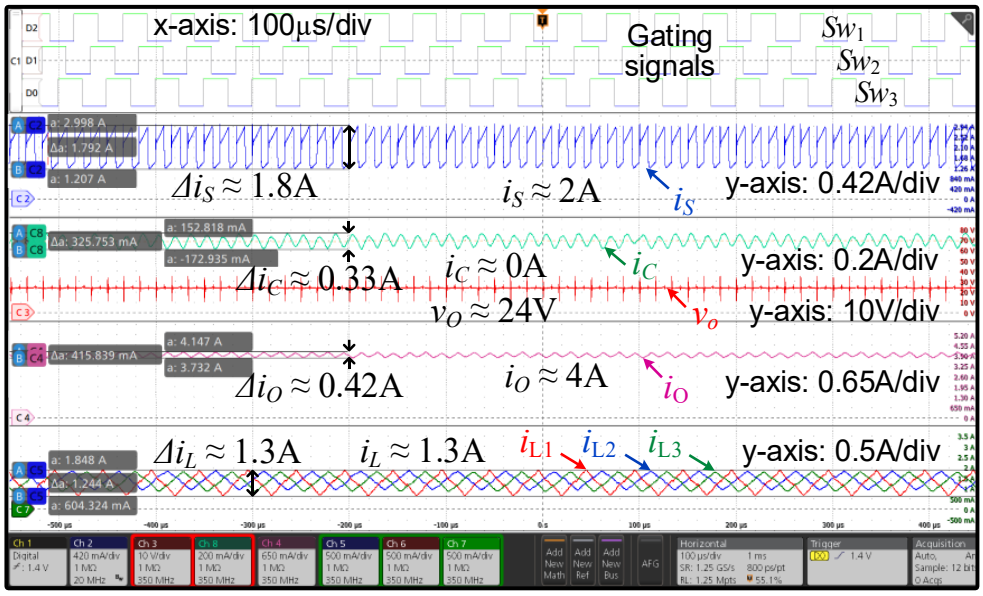


Fig. 4.22 Performance evaluation of TPIBC under different operating region R_2 with load power P_L = 100W at d = 0.5.

Fig. 4.23 shows the characteristics of TPIBC with continuous change of duty, i.e., $0 \leq d \leq 0.85$ at fixed load resistances with zoomed view of overlapping and non-overlapping modes at d = 0.3 and 0.8, respectively to have similarity with the simulation result shown in Fig. 4.16. It is apparent that $\Delta i_C \approx 0.36$ nearly maximum value of at centre of the region operation at duty d = 0.8 and $\Delta i_C \approx 0.14$ nearly minimum value of at end of the region of operation.

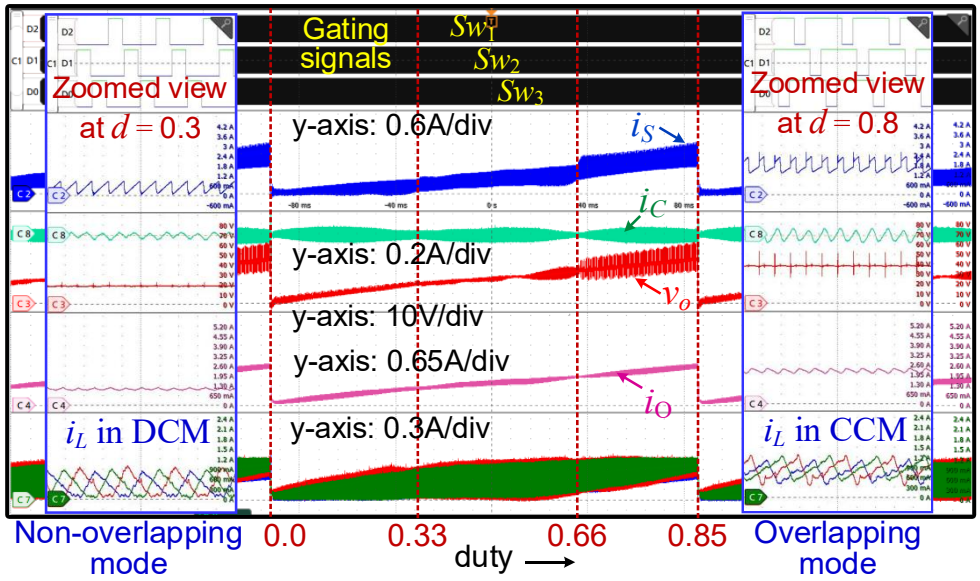


Fig. 4.23 Characterization of TPIBC at continuous change in duty ratio with fixed load resistance.

From Fig. 4.16 and Fig. 4.23, it is seen that the inductor ripple current increases with increase in duty ratio in region R_1, remains maximum and nearly constant with increase in duty ratio in region R_2 and decreases with increase in duty ratio in region R_3. The inductor ripple current, $\Delta i_L \approx 0.94$A at $d = 0.3$ end of region R_1 and $\Delta i_L \approx 0.76$A at $d = 0.8$ mid of region R_3.

Fig. 4.24 shows the switching loss behaviour of switch SW_2 at constant load power of 37.5W with different duty ratio. The captured results can be validated with the derived result presented in (4.22) and Fig. 4.12. Table 4.3 shows the validation of the theoretical results (TR) with respect to the experimental results (ER). The ERs are in good agreement to the derived TRs with minor difference, which is due to the presence of circuit parasitics.

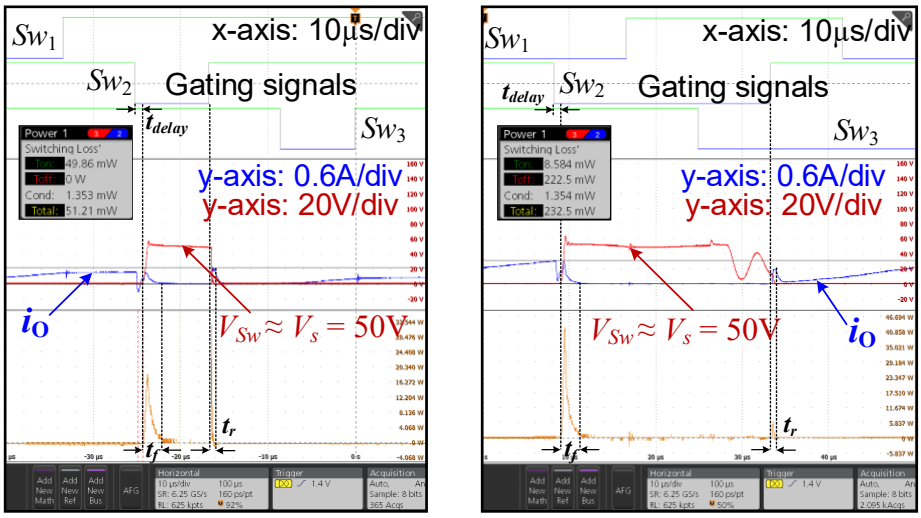


Fig. 4.24 Switching loss characteristics of SW_2 at constant load power of 37.5W with different duty ratio (a) d = 0.8, and (b) d = 0.5.

Table 4.3

BEHAVIOR OF TPIBC UNDER DIFFERENT OPERATING REGIONS AND LOADS

Parameters		P_L(W)	Δi_s(A)	Δi_L(A)	Δi_o(A)	i_s (A)	i_L(A)	i_o (A)	v_o(V)
d =0.16	TR	37.5	1.868	0.6	0.372	0.75	1.563	4.688	8
CCM	ER		1.80	0.63	0.39	0.77	1.50	4.40	7.30
d =0.50	TR		1.005	1.005	0.262	0.754	0.458	1.373	27.48
DCM	ER		0.94	0.98	0.24	0.77	0.47	1.30	28.40
d =0.83	TR		0.603	0.603	0.368	0.75	0.299	0.896	41.87
DCM	ER		0.60	0.60	0.38	0.76	0.35	0.90	41.50
d =0.16	TR	12.5	0.821	0.6	0.372	0.25	0.521	1.563	8
CCM	ER		0.81	0.61	0.38	0.26	0.51	1.60	7.30
d =0.3	TR	37.5	1.302	0.938	0.134	0.75	0.833	2.5	15
CCM	ER		1.30	1.00	0.12	0.75	0.74	2.20	14.30
d =0.5	TR	100	2.271	1.116	0.372	2.00	1.333	4	25
CCM	ER		1.80	1.30	0.42	2.00	1.30	4	24

4.7 Conclusion

This paper presents a time-domain characterization and performance analysis of current ripple behaviour, loss due to turn-on and turn-off conditions of the switch, and total converter loss for TPIBC at constant power and fixed resistance loads. The TPIBC has been designed for high-output current applications requiring reduced current ripple, such as electrolyzers and battery storage, to lower energy consumption and optimize aging. The presented analytical relations provide a solution for designing the dc bus voltage and, consequently, for selecting the duty ratio with respect to the load profile and application power rating, ensuring enhanced system performance in terms of reduced current ripple, switching losses, and total converter loss. The behavior of TPIBC varies with non-overlapping and overlapping switching signals, CCM and DCM of inductor current, and different load profiles. The derived relations also help to design the TPIBC parameters to operate under CCM and DCM of operation. The switching losses reduces with rise in duty ratio and further reduces for transition from CCM to DCM operation for constant power load. The percentage output current ripple rises with respect to output current from region-1 (R_1) to region-3 (R_3), and from CCM to DCM for constant power load. The value of Δi_L remains the same for a particular duty ratio irrespective of the change in output power.

Chapter 5

Multiport Interleaved Resonant Converter

5.1 Introduction

The development of sophisticated power electronic converters for high-power energy conversion applications has been greatly expedited by the quick electrification of transportation networks and the growing use of renewable energy sources. Highly efficient bidirectional power conversion systems that can transmit energy with high dependability, low losses, and superior power quality are necessary for EVs, BESS, renewable energy systems, and DC microgrids. Because of its uncomplicated control and simple architecture, conventional hard-switched DC–DC converters have been widely used in various applications. it is predicted that 11–13 million EVs will be sold in India annually, with electric two-wheelers leading the way with a projected penetration rate of 35–40%. To overcome the charging energy requirement, the installation of renewable-based fast charging (FC) stations is needed [64].

There are number of drawbacks of hard-switching techniques have been revealed by the ongoing demand for higher power density, higher switching frequency, and improved conversion efficiency. These drawbacks include increased switching losses, severe EMI, and high thermal stress experienced by semiconductor devices. By leveraging the inherent resonance between inductive and capacitive components to enable soft-switching operation, resonant power conversion has become a viable way to get around these restrictions. Resonant converters significantly lower switching losses and increase overall converter efficiency by minimizing the overlap between the switch voltage and current during switching transitions, in contrast to traditional pulse-width modulation (PWM) converters. Resonant converters can function at much higher switching frequencies with less device stress and electromagnetic emissions when ZVS or ZCS is achieved [93]. As a result, resonant converter topologies are becoming more and more appealing for medium and high-power applications that need high conversion efficiency and small converter structures.

A converter with multiple output port with interleaved feature could be used for higher charging current. The benefit of multiport output is the use of lower components leading to the lower cost and high-power density is achieved. The constraint with increase in number of ports is design and power flow controlling. In order to remove this constraint multiple transformers are connected together at output in [94]-[101]. However, it leads to higher cost and lower power density due to increase in volume. MPCs are generally designed for bidirectional power flow capability but for higher power rating used in the charging station unidirectional MPC should be used to reduce cost, volume and control complexity. The interleaved front-end converters are used in [65]-[66]. Using such converters provides the wide range of options for battery charging of different rating with fast and slow charging capability.

The interleaving of converter discussed in [65]-[66] achieves high output current. To decrease switching losses and further reduce the converter size, weight, and volume, converter switches must be operated in soft switching mode, but due to variation in the loading, the soft switching resonant converter (SSRC) designing is challenging task. The SSRC are discussed in [60]-[61], [65]-[66].

The bidirectional converters (BDCs) are available in isolated and non-isolated, where the LLC converters, CLLC converters [94], dual active bridge (DAB) converters [95] are some isolated BDCs used in many industrial applications. The transformer used in these BDCs help to achieve HV gain using high turn ratio but lack to achieve high efficiency with HV gain. The BDCs in [63], [77] and [96] can achieve higher efficiency for the designated voltage range but require higher turn ratio to achieve higher voltage gain which leads to design complexity of the transformer and higher copper loss and further the switching stress for HV side is large. The use of multiphase currents helps to achieve high output current and, hence, equivalent power with a lesser-voltage gains by reducing the turn ratio of transformer windings [38].

In [60]-[62], it discusses the resonant converters with soft switching mode. The resonant converter is classified depending on the configuration As renewable energy sources have fluctuating voltage output due to continuous change of irradiance, the dc-dc converter linked to EV charging systems has to be operated in soft switching for a range of input voltage variation [62].

Among the various resonant converters CLL resonant converter has the benefit of series and parallel resonant converters both. These converters have a wide range of ZVS operation of the primary switches and has the advantage of ZCS for the diode rectifier on the secondary side with pulse width control for load voltage regulation [94]. The range of frequency selection for variable frequency control for the resonant converter is required to be selected cautiously as the increased losses at higher frequency above the resonant frequency and increase in component size such as magnetics and filters at light loads when operated at lower frequency below the resonant frequency which results in low power density design of converter.

This chapter provides a thorough characterization of interleaved multiport resonant converters for charging and discharging infrastructure. The resonant converter topology and its working concept are first introduced in this chapter. A thorough analysis of the bidirectional interleaved multiport resonant converter follows the presentation of the modeling, operational features, and design process of the unidirectional interleaved multiport resonant converter. The usefulness of the suggested converter topologies for high-efficiency charging and discharging applications is demonstrated through discussion of the operating modes, resonance characteristics, design considerations, and simulation tests.

5.2 Resonant Converter Topology and Operation

Resonant converters use the inherent resonance between inductive and capacitive components to achieve soft-switching operation, in contrast to traditional PWM converters, which function by hard-switching semiconductor devices. Resonant converters greatly lower switching losses, limit EMI and increase converter dependability by permitting the switching transitions to take place at either zero voltage or zero current. For battery charging systems, renewable energy interfaces, data centers, EV charging infrastructure, and other high-power applications needing compact and effective power conversion, resonant converters are becoming more and more appealing due to these features [61].

The configuration of the resonant inductors and capacitors inside the resonant tank is the primary distinction between resonant converter topologies. The converter's voltage gain characteristics, circulating current, soft-switching range, control approach, and

appropriateness for bidirectional operation are all directly impacted by the arrangement of these passive components. As a result, throughout the past few decades, many resonant converter topologies have been proposed, each of which has unique benefits based on the intended use. The most frequent resonant converter configurations used in isolated DC–DC power conversion are the Series Resonant Converter (SRC), Parallel Resonant Converter (PRC), LLC Resonant Converter, CLL Resonant Converter, and CLLC Resonant Converter [99].

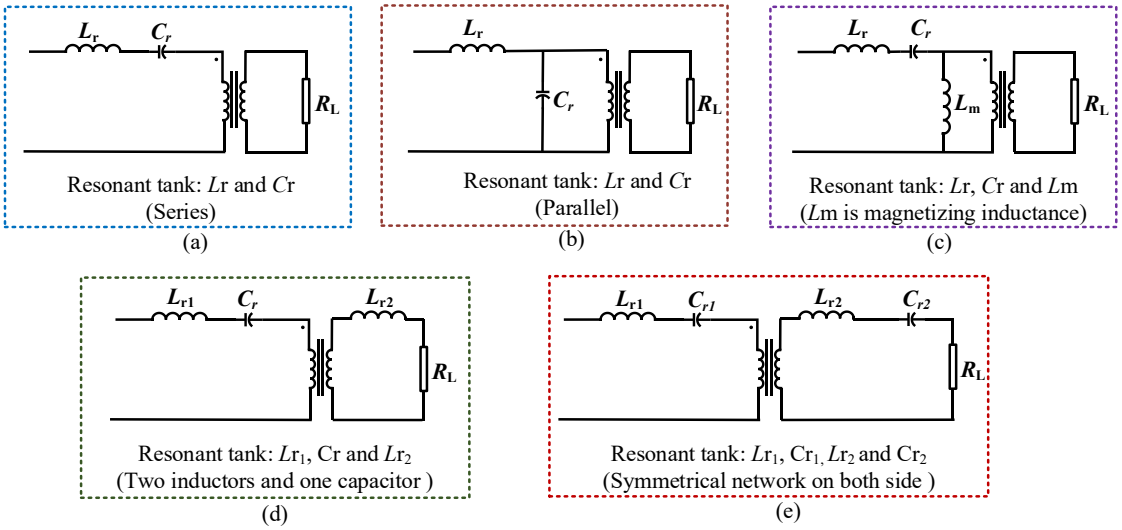


Fig. 5.1 Classification of resonant converter topologies as per resonant tank configurations (a) SRC, (b) PRC, (c) LLC, (d) CLL, and (e) CLLC

5.2.1 Series Resonant Converter

One of the earliest resonant converter topologies created for isolated high-frequency power conversion is the SRC. The resonant tank is made up of a resonant inductor (L_r) and resonant capacitor (C_r) linked in series with the high-frequency transformer's primary winding, as shown in Fig. 5.1(a). The output voltage is controlled by adjusting the switching frequency around the resonant frequency, while the resonant network acts as a frequency-dependent impedance.

***Operating Principle*:**

A bridge inverter is first used to transform the DC input voltage into a high-frequency square-wave signal. The series resonant tank, where electrical energy constantly oscillates between the resonant inductor and resonant capacitor, is subjected to this high-frequency

stimulation. The inductive and capacitive reactance's cancel each other out at the resonant frequency, which minimizes tank impedance and maximizes power transfer via the transformer to the secondary-side rectifier. The transmitted power is decreased as the switching frequency is raised above resonance because the resonant current falls. On the other hand, operating below resonance raises the resonant current, albeit too much circulating current might lower converter efficiency. The converter can accomplish ZCS, which reduces switching losses, because the resonant current naturally drops to zero during each switching cycle.

The SRC has a straightforward resonant construction, superior high-frequency performance, and built-in soft-switching functionality. However, because the output voltage is highly dependent on the load impedance, the converter shows poor voltage regulation under light-load conditions. Additionally, a comparatively large switching-frequency variation is necessary to maintain output voltage regulation, which increases control complexity and decreases efficiency under various operating situations.

5.2.2 Parallel Resonant Converter

To get over the SRC's limitations in light-load control, the PRC was developed. As seen in Fig. 5.1(b), this topology has the L_r connected in series with the power transfer line and the C_r connected in parallel with the load. The resonant capacitor may directly sustain the output voltage thanks to the parallel configuration, which enhances voltage regulation across a larger load range.

***Operating Principle*:**

Similar like the SRC, the inverter transforms the incoming DC voltage into a high-frequency AC voltage before applying it to the resonant tank. As power is sent to the output via the high-frequency transformer, the resonant inductor and capacitor constantly exchange energy. Even while operating with a light load, the output voltage is comparatively steady since the resonant capacitor is linked in parallel with the load. By altering the switching frequency, which changes the resonant tank impedance and hence controls the resonant current, the output power may be adjusted.

The continuous cycling of resonant current across the parallel capacitor causes greater conduction losses during heavy-load operation, even though the PRC offers better light-load voltage regulation than the SRC. The resonant components are subjected to more

heat stress due to the increased circulating current, which also lowers converter efficiency. As a result, the PRC is less appealing for contemporary high-power charging applications where decreased conduction losses and high efficiency are crucial.

5.2.3 LLC Resonant Converter

By integrating a L_r, C_r and transformer magnetizing inductance (L_m) inside the resonant tank, the LLC resonant converter incorporates the advantageous features of both the SRC and PRC. One of the most popular resonant topologies for switched-mode power supplies, battery chargers, and isolated DC-DC converters is the LLC converter because of its exceptional efficiency and broad soft-switching range.

***Operating Principle*:**

The resonant tank is excited by the high-frequency inverter. Energy is alternately stored in the capacitor and resonant inductance throughout each switching cycle before being sent to the output rectifier via the transformer. The converter may display two resonant frequencies and greatly expand the ZVS operating region thanks to the magnetizing inductance's additional resonant channel. By adjusting the switching frequency around the resonant frequency while preserving effective resonant energy transfer, output voltage regulation is accomplished.

Excellent conversion efficiency, low switching losses, broad load regulation flexibility, and high-power density are all offered by the LLC converter. However, the presence of several resonant frequencies makes resonant tank construction more difficult and necessitates careful resonant parameter optimization to guarantee stable operation across the intended operating range. Furthermore, further circuit modifications and complex control schemes are frequently needed to sustain bidirectional functioning utilizing the LLC topology.

5.2.4 CLL Resonant Converter

An additional resonant inductor, L_{r2} along with L_{r1} and C_r is employed in place of the transformer magnetizing inductance, L_m used in the LLC converter in the CLL resonant converter, an alternate resonant topology. As a result, the resonant tank has two resonant inductors and one resonant capacitor, allowing for more design flexibility and better resonant characteristic control. Because of these characteristics, the CLL converter is

especially well-suited for interleaved converter designs and high-power isolated converters.

***Operating Principle*:**

The CLL resonant tank is driven by a high-frequency excitation produced by the inverter during operation. Power is transferred to the output stage via the high-frequency transformer via a sinusoidal resonant current created by the alternating storage and release of energy by the resonant inductors and capacitor. By adjusting the switching frequency in relation to the resonant frequency, the output voltage can be controlled. By carefully choosing the resonant components, the resonant behavior may be precisely controlled because the resonant inductors are independent of the transformer magnetizing inductance. Additionally, ZVS is made possible over a wide working range by the resonant current's natural depletion of the switch output capacitances prior to device turn-on.

The CLL topology provides more magnetic design flexibility, lower semiconductor current stress, less circulating current, and easier integration with interleaved converter topologies when compared to the LLC converter. Additionally, the converter has good compatibility with various multiport architectures and a high conversion efficiency. For charging and discharging infrastructures that need high efficiency, balanced current sharing, and scalable power capability, these features make the CLL resonant converter especially appealing.

5.2.5 CLLC Resonant Converter

By adding resonant inductors and capacitors on both sides of the isolation transformer shown in Fig 5.1(e), the CLLC resonant converter expands the CLL topology and creates a symmetrical resonant tank. The CLLC converter is especially well-suited for bidirectional DC–DC power conversion since this configuration allows for almost identical resonance properties during both forward and reverse power transfer.

***Operating Principle*:**

The converter uses high-frequency switching to stimulate the symmetrical resonant network. The primary-side bridge serves as the inverter and the secondary-side bridge as the rectifier during forward power flow. The two bridges' operational responsibilities are switched during reverse power flow. The resonant properties are nearly the same in both operating directions because of the symmetrical arrangement of the resonant components.

As a result, throughout a broad operating range, effective bidirectional energy transfer can be accomplished while preserving ZVS.

The CLLC converter has symmetrical voltage gain characteristics, high conversion efficiency, and outstanding bidirectional performance. Nevertheless, the extra resonant inductors and capacitors raise the number of converter components, making resonant parameter optimization more difficult and the design more complex. These elements make practical realization more difficult and raise implementation costs, especially for high-power modular converter systems.

The CLL resonant converter provides an efficient balance between converter simplicity, resonant tank flexibility, soft-switching capabilities, lower circulating current, and high conversion efficiency among the various resonant converter topologies. Additionally, its resonant construction allows for balanced current sharing and modular power expansion while maintaining excellent operational efficiency, making it ideal for interleaved and multiport implementations. The CLL resonant topology has been used in this study to construct the suggested interleaved multiport resonant converters because of these benefits.

5.3 Unidirectional Multiport Resonant Converter

The proposed multiport output series resonant interleaved DC-DC converter with unidirectional power flow capability of different ports at particular voltage level. Having a multiport structure reduces the requirements of multiple HF transformer resulting the cost and volume of the system decreases in comparison with the same number of individual chargers. A control method using PWM and frequency modulation is obtained to control the output voltage and power for the three port converters. The interleaved output of the three ports helps to obtain low ripple peak current for HF transformer secondary side and high charging current obtained.

5.3.1 Modeling and Characterization

The circuit diagram of three-port resonant converter (TPRC) with capacitive filter is presented in Fig. 5.2. The converter comprises mainly of source voltage v_S, input active full bridge with switches S_1, S_2, S_3 and S_4 and output three ports with diode full bridge; D_1, D_2, D_3, D_4 corresponding to output port-1; D_5, D_6, D_7, D_8 corresponding to output port-2;

and D_9, D_{10}, D_{11}, D_{12} corresponding to output port-3, respectively. The input and output of TPRC is linked by LC resonant tank with capacitor, C_r and inductor, L_r and HF transformer having magnetizing inductance and negligible leakage inductance. In order to utilize magnetizing inductance L_m of the HF transformer as part of the parallel inductor, the inductor L_{O1}, L_{O2}, L_{O3} are kept on the secondary side ports P_1, P_2 and P_3 that of HF transformer respectively where, L_{O1}, L_{O2}, L_{O3} are equal and equivalent parallel inductance including L_m is L_P.

The equivalent circuit of the Fig. 5.2 referred to the primary / input side of the HF transformer after performing the analysis for simplification is shown in the Fig. 5.3, where $V_{ab,f}$ and $V_{cd,f}$ represents the fundamental component of voltage. The output voltage of the secondary ports is considered equal such that $V_{c_1d_1} = V_{c_2d_2} = V_{c_3d_3} = V_{cd}$. All switches S_1, S_2, S_3 and S_4 at primary side of the converter consists of standard MOSFET with anti-parallel diodes and snubber capacitor connected in parallel.

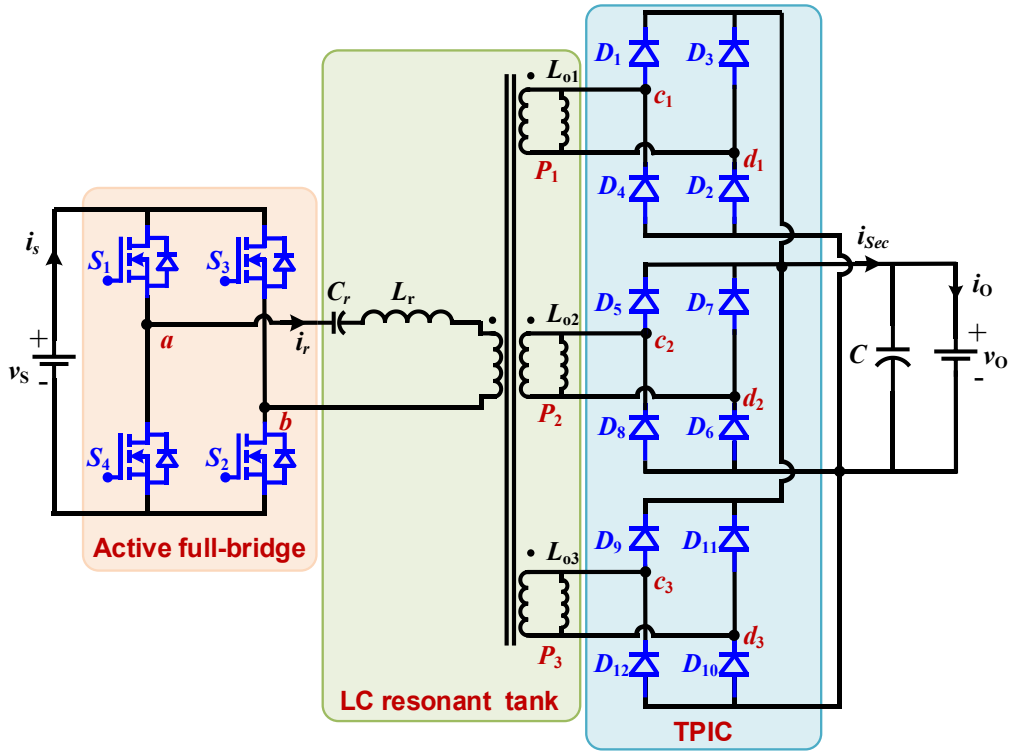


Fig. 5.2 Resonant TPRC circuit diagram.

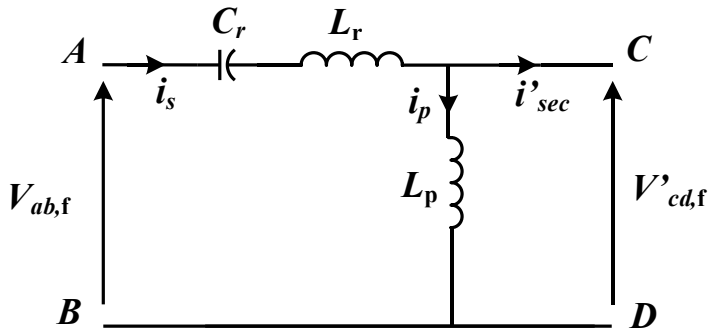


Fig. 5.3 Simplified three-port LC resonant tank circuit.

The output power of the resonant TPRC is controlled by modified gating scheme by changing the input pulse width, δ and also regulating the number of interleaved ports in operation from three to one and vice-versa. The pulse width δ of voltage V_{ab} is controlled by changing the angle α. The gating signal to the switches S_2 and S_4 is reduced by angle α which is then summed up with switches S_1 and S_3 respectively. Thus, the gating signal for S_1, S_3 are wider than S_2, S_4. The output port bridge diodes are working for 50% duty cycle like a diode bridge rectifier. The capacitor used in series LC resonant tank is significant in reducing dc current component arising due to asymmetry of the bridge's voltage drop, etc. and avoids the transformer saturation. In the LC resonant tank when the voltage across the capacitor is at peak, current through the tank is zero and when the voltage across the capacitor is zero, current through resonant tank is at peak.

5.3.2 Steady state Equivalent Circuit Analysis

The CLL resonant tank converter is analyzed using approximate ac circuit analysis [13]. In approximate equivalent circuit analysis, all harmonics component except fundamental component are neglected for both voltage and current. All components such as switches, diodes and capacitor are taken to be ideal. The HF transformer has magnetizing inductance, which is considered as parallel inductor; and the leakage inductance at primary side and secondary side for all the three-port outputs are neglected.

All the components and parameters are referred to the primary side from the secondary side. The load resistance R_o, output current i_o, output voltage v_o are transferred to the primary side of HF transformer and is denoted as R'_o, i'_o, and v'_o, respectively. The ac component of current i_{sec} in secondary side is referred to the primary side denoted as i'_{sec}.

There are two equivalent circuit analysis done for voltage source load and resistive load with capacitive filter. Any of the analysis could be applied to either of the load because resistive load resistance can be regarded as equivalent load resistance of voltage source load with power $P_0 = v_0'^2/R'_F$, $R'_0 = R'_F$ for full load as R'_F is the full load resistance referred to primary side. For design purpose all equations are presented in normalized form with the base values.

$$V_B = v_S; Z_B = R'_F; i_B = V_B / Z_B \tag{5.1}$$

where, v_s is the dc bus voltage or input voltage. The converter voltage gain is given as follows:

$$M = v'_0 / v_S = v'_0 / V_B \tag{5.2}$$

The ratio of switching frequency to resonant frequency is the normalized switching frequency

$$F = \omega_s / \omega_r = f_s / f_r \tag{5.3}$$

where, $f_r = \omega_r /2\pi$ is the resonant frequency of the series tank circuit and also $\omega_r = 1/\sqrt{(L_S C_S)}$ and $f_s = \omega_s /2\pi$ is the required switching frequency.

The normalized value of series and parallel reactance are given as follows:

$$X_{S,pu} = X_s / Z_B; \quad X_{P,pu} = X_P / Z_B \tag{5.4}$$

$$\text{where, } X_{s,pu} = X_{L_S,pu} + X_{C_S,pu}$$

$$X_{L_S,pu} = \frac{\omega_S L_S}{R'_F} = \left(\frac{\omega_r L_S}{R'_F}\right)\left(\frac{\omega_S}{\omega_r}\right) = Q \times F \tag{5.5}$$

where Q is the quality factor of series resonant circuit. Similarly,

$$X_{C_S,pu} = -Q / F \tag{5.6}$$

The normalized inductance is given as follows:

$$\lambda = L_S / L_P \tag{5.7}$$

The equivalent circuit in Fig. 5.3 is used for the analysis in which CLL-tank circuit separated by fundamental component of two voltage sources V_{ab} and V'_{cd} (referred to primary side) across the terminals *AB* and *CD* are used in the analysis respectively.

The normalized fundamental component of two voltage source V_{ab} and V'_{cd} in [14] is given as follows:

$$V_{ab,\mathrm{f},pu} = (2/\pi)\times(1-cos\delta) \tag{5.8}$$

$$V'_{cd,\mathrm{f},pu} = (4M/\pi) \tag{5.9}$$

By using the principle of superposition, the normalized primary side series tank current is as follows:

$$i_{s,pu} = \left(\frac{V_{ab,\mathrm{f},pu} - V'_{cd,\mathrm{f},pu}}{X_{S,pu}}\right) \tag{5.10}$$

Simplifying (5.10),

$$i_{s,pu} = \left(\frac{2}{\pi Q(F-\frac{1}{F})}\right)\left[(1-cos\delta)-2M\right] \tag{5.11}$$

The normalized current through parallel inductor L_p is

$$i_{p,pu} = \left(\frac{4M}{\pi X_{p,pu}}\right) = \left(\frac{4M\lambda}{\pi QF}\right) \tag{5.12}$$

Thus, using (5.11) and (5.12) and simplifying normalized interleaved secondary side current referred to primary side is given as follows:

$$i'_{sec,pu} = \left(\frac{2}{\pi Q(F-\frac{1}{F})}\right)[(1-\cos\delta)-2M(1+K)] \tag{5.13}$$

where,

$$K = \lambda(1-1/F^2) \tag{5.14}$$

The expression for peak current in series tank can be obtained from (5.11) as follows:

$$i_{S_{Pk},pu} = \left(\frac{2}{\pi Q(F - \frac{1}{F})} \right) \sqrt{\left[(1 - cos\delta)^2 + 4M^2 - 4M(1 - cos\delta) \right]} \quad 5.15$$

The peak voltage of tank capacitor is given by

$$V_{C_{Pk},pu} = \left(\frac{2}{\pi Q(F^2 - 1)} \right) \sqrt{\left[(1 - cos\delta)^2 + 4M^2 - 4M(1 - cos\delta) \right]} \quad 5.16$$

$$i'_{sec_{Pk},pu} = \left(\frac{2}{\pi Q\left(F - 1/F\right)} \right) \sqrt{[(1 - \cos\delta)^2 + 4M^2(1 + K)^2 - 4M(1 + K)(1 - \cos\delta)]} \quad 5.17$$

The peak secondary current referred to primary side is obtained from (5.13) given as in (5.17). The instantaneous power transferred from primary side to secondary side or vice-versa can be evaluated from either side. Here the instantaneous power is calculated taking product of voltage, $V'_{cd,\mathrm{f,pu}}$ and current, $i'_{sec,\mathrm{pu}}$ in the secondary side referred to the primary side.

$$P_{pu} = \left(\frac{8M}{\pi^2 Q(F - \frac{1}{F})} \right) [(1 - \cos\delta) - 2M(1 + K)] \quad 5.18$$

In the Fig. 5.3 all the components voltage and current in secondary side are shown referred to primary side. In the secondary bridge, output voltage v'_{O} is considered to be constant, the input voltage V'_{cd} is square wave with positive and negative peak of amplitude v'_{O}. Thus, rms value of input voltage and current fundamental component, for secondary side rectifier across terminal CDis given as:

$$V'_{cd,\mathrm{f},r} = \left(\frac{2\sqrt{2}}{\pi} v'_O \right) \quad 5.19$$

$$i'_{sec,r} = \left(\frac{\pi}{2\sqrt{2}} i'_O \right) \quad 5.20$$

The ac equivalent resistance R_{ac} for the replacement of diode bridge, filter capacitor and load resistance block is obtained by considering only fundamental component [14] dividing the rectifier voltage and current and expressed as

$$R_{ac} = \left(8/\pi^2\right) R'_O \quad \text{where, } R'_O = R_O / n^2 \tag{5.21}$$

The normalized form of ac equivalent resistance is

$$R_{ac,pu} = \left(\frac{8R'_O}{\pi^2 R'_F}\right) \tag{5.22}$$

where $R'_O = R'_F$ for full load. The rms value of the fundamental component of voltage across terminal *AB* is expressed as

$$V_{ab,f,r} = \left(\frac{\sqrt{2}}{\pi} v_S\right)(1-\cos\delta) \tag{5.23}$$

The phasor equivalent circuit model with primary voltage taken as the reference voltage. Thus, voltage gain in the impedance network can be expressed as

$$\frac{V'_{cd,f,r}}{V_{ab,f,r}} = \left|\frac{R_{ac,pu} \parallel jX_{p,pu}}{X_{s,pu} + R_{ac,pu} \parallel jX_{p,pu}}\right| \tag{5.24}$$

Comparing equation (5.19) and (5.23) we get converter voltage gain as

$$M = \frac{v'_O}{v_S} = \frac{1-\cos\delta}{2}\frac{V_{cd,f,r}}{V_{ab,f,r}} \tag{5.25}$$

Simplifying the expression for equation (5.24), we get

$$M = \frac{(1-\cos\delta)/2}{\sqrt{\left(1+\lambda\frac{1}{\left(1-F^2\right)}\right)^2 + \left(\frac{\pi^2}{8}Q\left(F-\frac{1}{F}\right)\right)^2}} \tag{5.26}$$

From (5.26) it is interpreted that gain, *M* is dependent on gating scheme for change in, load quality factor *Q*, normalized switching frequency *F* and normalized inductance λ.

5.3.3 Design Trade Off

Converter gain is addition of two blocks the resonant tank and the transformer. The resonant tank gain is variable depending on the load, frequency and inductance whereas the transformer gain is fixed depending on the ration of primary to secondary and also transformer ideally does not amplify or dampen the signal, it is only responsible to change the output voltage level. The input voltage of the converter is expected to have variations and as the transformer gain is fixed to keep constant output voltage the tank must compensate. Therefore, if input voltage is lower than the specified value tank has to amplify the signal producing the maximum resonant tank gain and if the input voltage is higher than the specified value, then the tank has to dampen the signal producing minimum resonant tank gain.

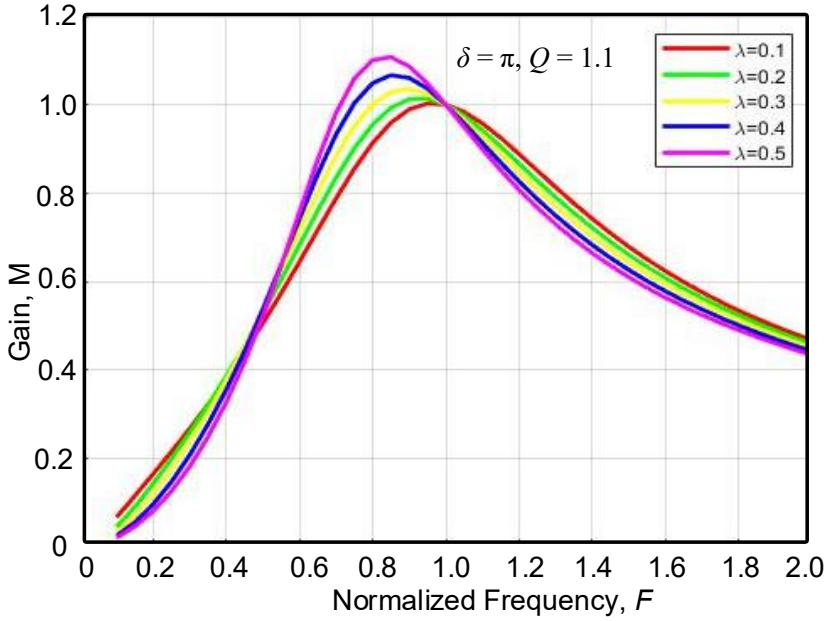


Fig. 5.4 Plot for gain (M) with respect to normalized frequency (F) for varying normalized inductance (λ).

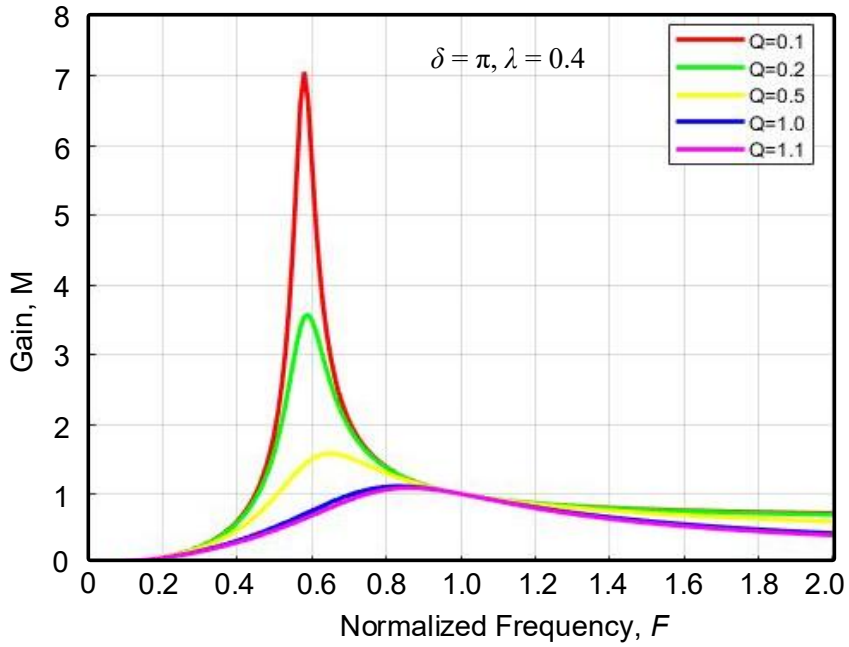


Fig. 5.5 Plot for gain (M) versus normalized frequency (F) for varying quality factor (Q).

Fig. 5.5 shows the plot for gain with respect to normalized frequency for various value of Q depending on load. Gain is proportional to frequency but their relationship depends on the operating region. Gain control is done by the modulating switching frequency. Gain is inversely proportional to switching frequency in inductive region and directly proportional in capacitive region. Accordingly entering capacitive region could provoke instability in the control loop and damage the switching MOSFET. Since stable control for all loads are required therefore, for worst case scenario of overloading, Q = 1.1 is considered. Depending on the value of gain required the minimum and maximum switching frequency range is selected in the inductive region for stable operation. Such as minimum switching frequency for maximum gain and maximum switching frequency for minimum gain. Also, the power output could be controlled by the changing the switching frequency higher the resonant frequency and modified gating scheme.

The plot in Fig. 5.4 is used to determine the value of normalized inductance, higher normalized inductance indicates higher gain and wider input range. The converter is always operated with such switching frequency so as to operate in inductive region and achieve ZVS soft switching for all the primary side switches of the converter with constant output voltage.

Fig. 5.6 shows the plot for gain, M with respect to quality factor (Q) for various value of normalized frequency (F) depending on switching frequency. This presents that with decrease in the value of quality factor increment in gain is faster for lower values of normalized frequency (F).

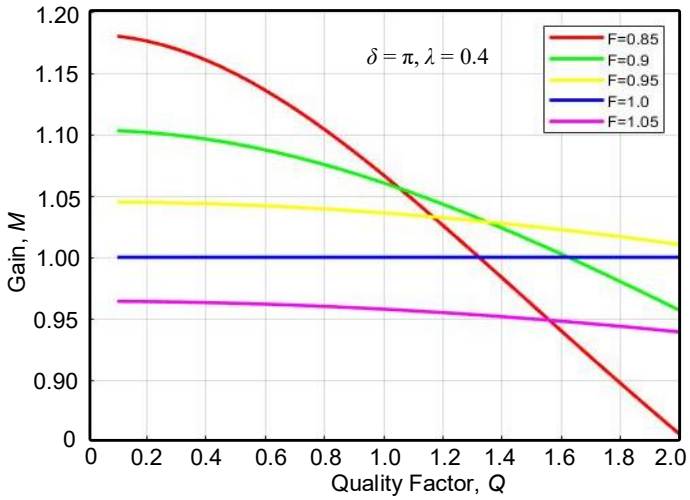


Fig. 5.6 Plot for gain, M with respect to quality factor, Q for varying normalized frequency, F.

The specifications for the CLL-type front end resonant converter design are as follows: primary side or input nominal voltage $v_{S,nom}$= 480V and deviation in input voltage is considered such as $v_{S,max}$=510V and $v_{S,min}$=460V, full load output power is 3.3kW, output voltage required (v_O) = 48V, maximum average output current ($i_{O.max}$) = 68.75A, resonant frequency (f_r) = 50kHz. Considering the transformer ratio (n) = 10 and input voltage range, the value of M_{max}= 1.04 and M_{min}= 0.94. From Fig. 5.6. the minimum and maximum required normalized frequency F_{min}= 0.96 and F_{max} =1.05 respectively. From Fig. 5.4. for the given range of gain, the minimum required normalized inductance is determined as, λ = 0.4. The converter is designed for worst condition at δ = π with maximum load, Q = 1.1. The full load resistance is $R_F = v_O^2/P_O$ = 0.6981Ω, therefore R'_F = 69.81Ω. From (1) base values V_B= 480V, Z_B= 69.81Ω and I_B= 6.875A. Using (5.2) to (5.7), the tank parameters can be calculated as L_r=244.45 µH, C_r= 0.0414 µF, L_P= 611.125 µH. It is to be noted that L_P includes the magnetizing inductance of the HF transformer. Therefore, depending on the value of magnetizing inductance of the HF transformer the value of L_{O1}, L_{O2}, L_{O3}, placed on secondary side of HF transformer is calculated.

5.3.4 Simulation Results and Discussion

The CLL-type multiport resonant designed converter in previous section is simulated using MATLAB simulation software. The power transfer of the converter is controlled by varying the switching frequency, f_S and pulse width, δ. The simulation is done for (a) maximum gain, M_{max} and minimum normalized frequency, F_{min} (b) unity gain and unity normalized frequency (c) minimum gain and maximum normalized frequency. All the simulation waveforms are presented for full load and pulse width of switches of the primary side converter operated at 50% duty cycle i.e $\delta = \pi$.

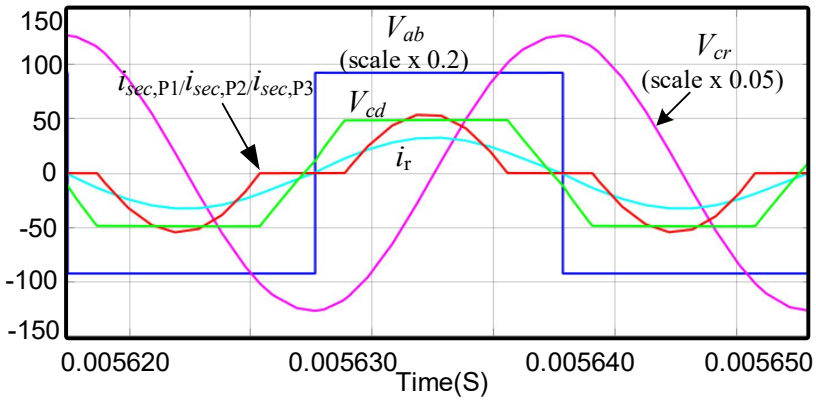


Fig. 5.7 Waveforms for full load FC such as all the primary switches operate in ZVS soft switching when gain, M_{max}=1.04, normalized frequency, F_{min}=0.96 for v_S = 460V and f_S= 48kHz.

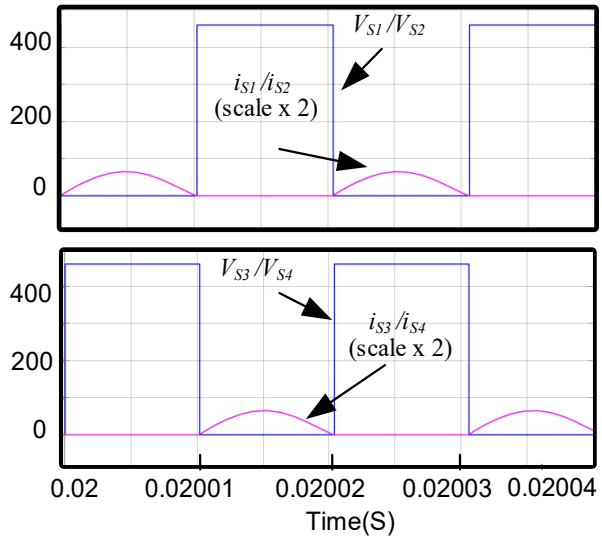


Fig. 5.8 Switching waveforms for primary side switches for full load FC at v_S = 460V and f_S= 48kHz.

Fig. 5.7 shows the simulation results for minimum source voltage, $v_S = 460$V, such that gain, M_{max}=1.04 and minimum frequency, f_S= 48kHz having F_{min} =0.96. The resonant tank current, i_r is almost in-phase with the primary voltage, V_{ab} which allows ZVS operation of primary side switches as shown in Fig. 5.8. The tank capacitor voltage V_{cr} is in resonance with the tank current, i_r. The secondary voltage of HF transformer for each port P_1, P_2 and P_3 is V_{cd} and secondary port output current of individual port is $i_{sec,P1}$, $i_{sec,P2}$and $i_{sec,P3}$.

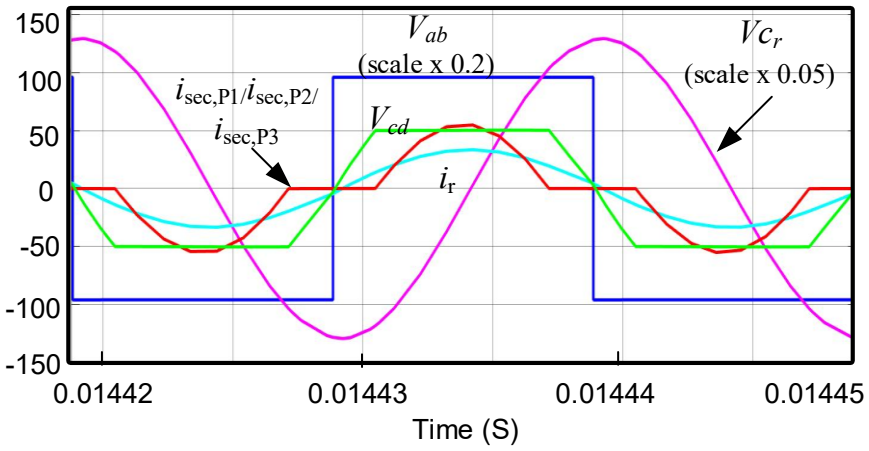


Fig. 5.9 Waveforms for full load FC such as all the primary switches operate in ZVS soft switching when gain, M_{nom}=1, normalized frequency, F_{nom}=1 for for v_S = 480V and f_S= f_r =50kHz.

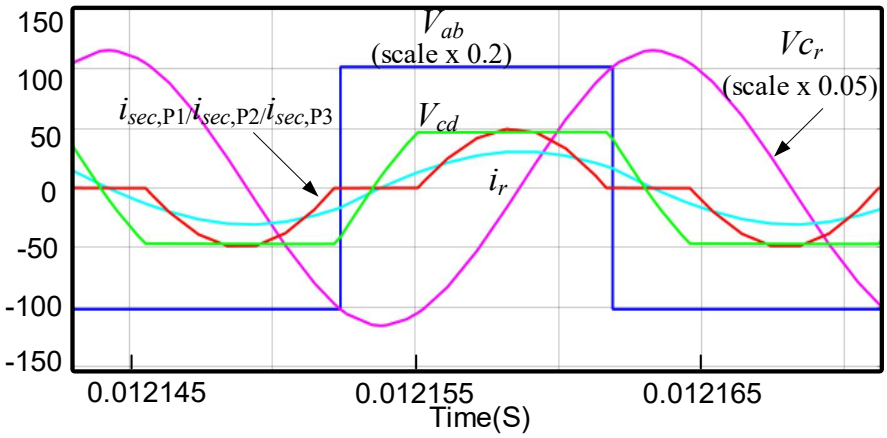


Fig. 5.10 Waveforms for full load FC such as all the primary switches operate in ZVS soft switching when gain, M_{min}=0.94, normalized frequency, F_{max}=1.05 for v_S = 510V and f_S= 52.5kHz.

The simulation results for nominal source voltage v_S = 480V, such that gain, M=1 and resonant frequency, f_S= f_O =50kHz having F= 1 is shown in the Fig. 5.9 and simulation results for maximum source voltage v_S = 510V, such that gain, M_{min}= 0.94 and maximum frequency, f_S =52.5kHz having F_{max} = 1.05 is shown in the Fig. 5.10 and ZVS soft switching is shown in Fig. 5.11. Hence, all the switches in three different operations are operating in ZVS soft switching as presented in Table5.1.

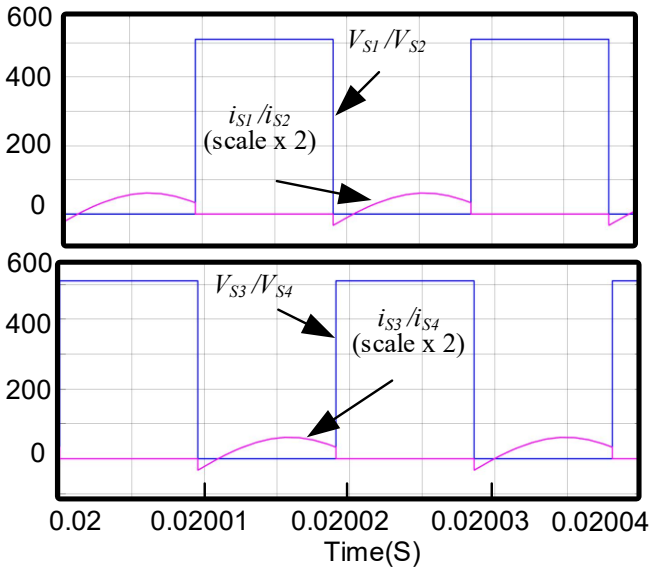


Fig. 5.11 Switching waveforms for primary side switches for full load FC at v_S = 510V and f_S= 52.5kHz.

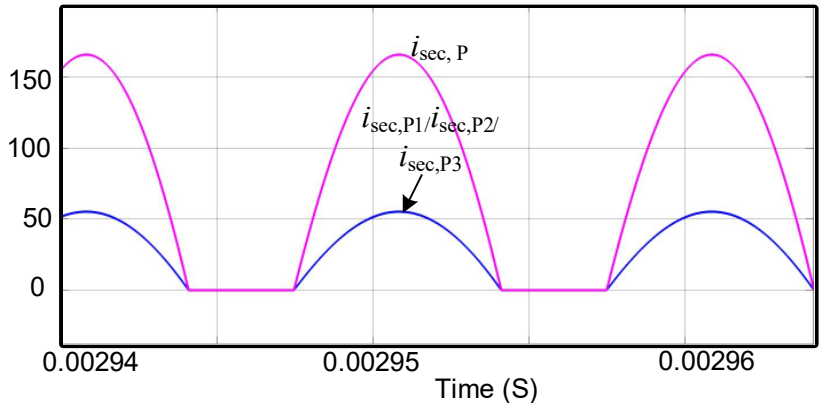


Fig. 5.12 Waveforms of secondary side ripple current for each output port having peak current of 55A approx. and for combined output port having peak current of 165A approx. respectively.

The total current of the interleaved output port is the sum of individual output port current of secondary side such that $i_{sec,P} = i_{sec,P1} + i_{sec,P2} + i_{sec,P3}$. Fig. 5.12 shows the individual port output current and interleaved port output current and it is interpreted that the peak current of single output is three times the individual port peak current.

TABLE 5.1

RESULT COMPARISON

Parameters	**Results**		
Input voltage, v_S	480 V	460V	510V
Switching frequency, f_S	50kHz	48kHz	52.5kHz
Gain, M	1	1.04	0.94
Normalized Frequency, F	1	0.96	1.05
Soft Switching Primary Side Switches.	All the switches are operating in ZVS soft switching.		

5.4 Bidirectional Interleaved Multiport Resonant Converter

A three-phase interleaved bidirectional resonant converter (TPIBRC), is shown in Fig. 5.13(a), for charging EVs at various charging levels from varying dc bus voltages integrated with DG from renewable sources. Each of the three input ends has been fed at a 1/3rd phase difference at a specified range of duty ratio, and the output end is linked to a multiport HF transformer at the ideally fixed voltage for high current with minimal ripples to promote the FC of EVs. The converter is designed for operation in a bidirectional mode with FC and slow discharging of the vehicle. The component design of the converters is based on the applicable load requirement or capacity of the EV.

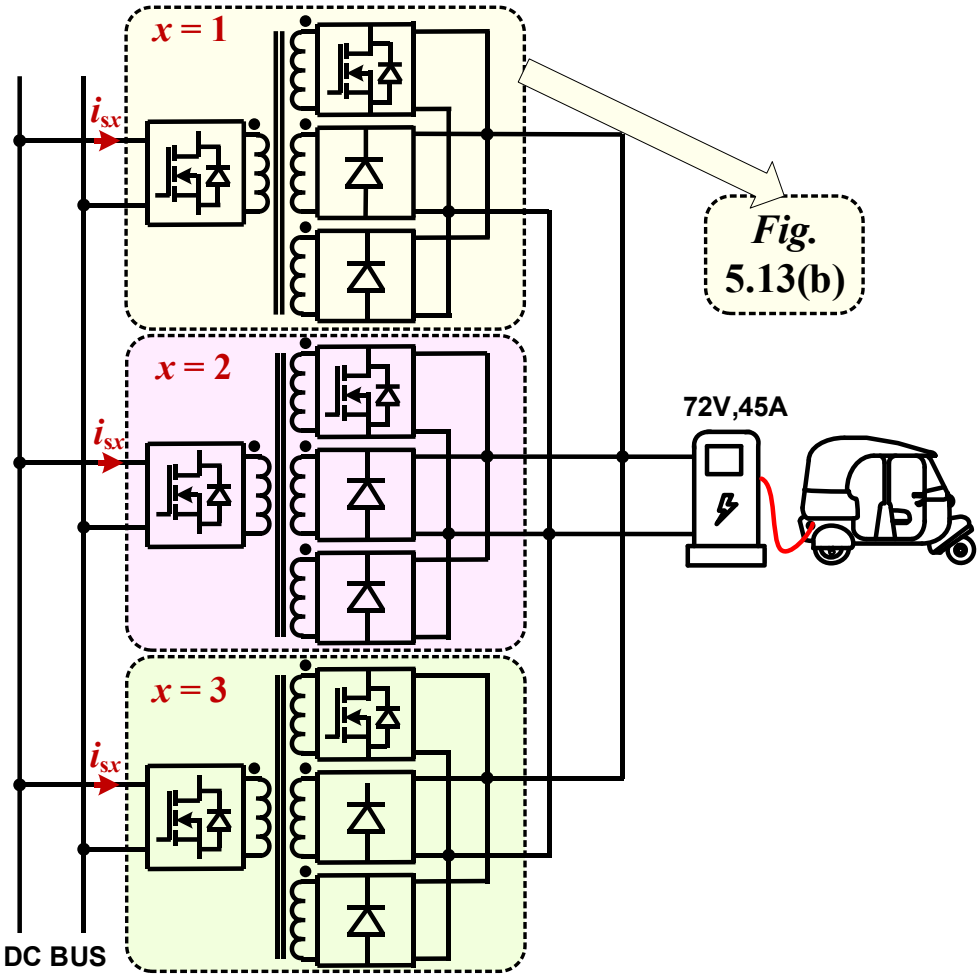


Fig. 5.13 (a) DC bus fed front-end interleaved bidirectional resonant converter with 3.3kW capacity.

5.4.1 Modeling and Characterization

The interleaved branches of front-end interleaved resonant dc-dc converter having common input dc source and combined output filter capacitor is presented in Fig. 5.13(b). The given circuit has the active full bridge input with switches S_{P1}, S_{P2}, S_{P3} and S_{P4} and output three ports where port 1 is active full bridge with switches S_{S1}, S_{S2}, S_{S3} and S_{S4} having antiparallel diode D_1, D_2, D_3, D_4 and other two ports with diode full bridge having diodes D_5, D_6, D_7, D_8 for output port 2 and D_9, D_{10}, D_{11}, D_{12} for output port 3 respectively. Each interleaved branch input bridge and output bridges are linked by multiport HF transformer with capacitor, C_r and inductor, L_r as LC resonant tank. In order to regulate the value of equivalent parallel inductor, L_P as per design requirement and use magnetizing

inductance L_m, the inductor L_{S1}, L_{S2}, L_{S3} are housed correspondingly on each interleaved branch ports P_1, P_2 and P_3 where, L_{S1}, L_{S2}, L_{S3} are equal and the leakage inductance of HF transformer is considered to be negligible. The equivalent LC resonant tank circuit, referred to the primary / input side of the HF transformer, is presented in Fig. 5.14.

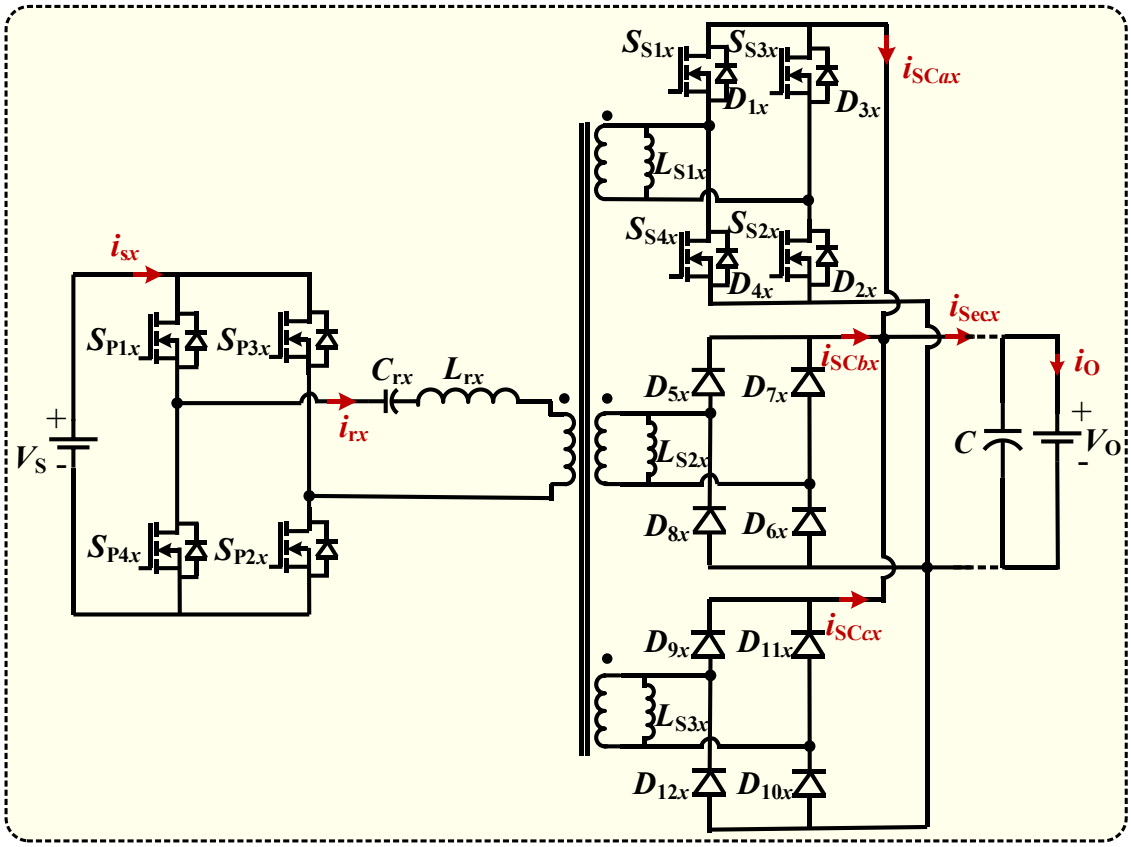


Fig. 5.13 (b) circuit diagram of each branch of front-end interleaved resonant converter.

The input voltage of each interleaved branch is V_{AB}, and the output voltage of each secondary port of each interleaved branch is equal that is, V_{CD}. All switches S_{Pux} at primary side and all switches S_{Sux} at port 1 of secondary side of xth interleaved branch of converter where $u = 1$ to 4 comprise of the MOSFET switch, which has embedded snubber capacitor connected with anti-parallel diodes. The pulse width, δ is controlled by altering the angle α. The gating signal to the primary bridge bottom switches S_{P2x} and S_{P4x} is reduced by angle α, which is then summed up with primary bridge top switches $S_{P1x}$and S_{P3x}, respectively. Thus, the gating signal for S_{P1x}, S_{P3x} are wider than S_{P2x}, S_{P4x}. The secondary side bridges ports work at 50% duty cycle.

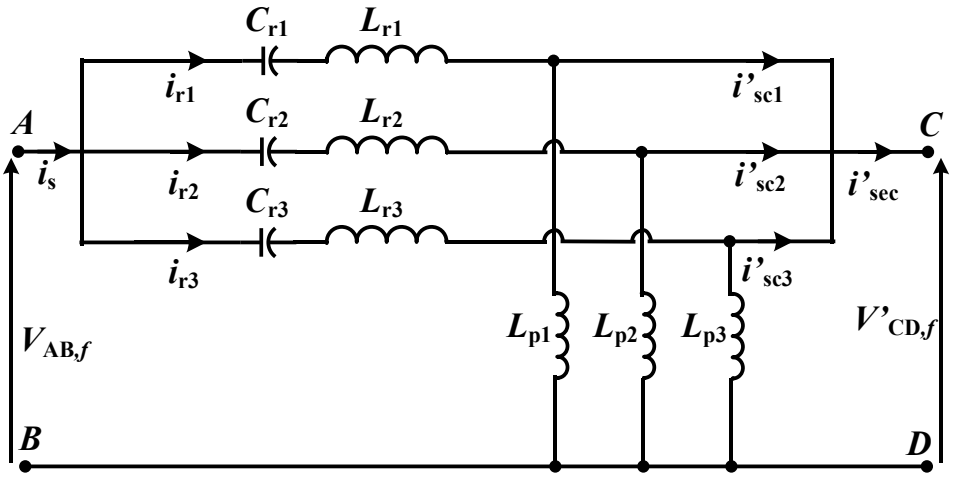


Fig. 5.14 Simplification of *LC* resonant tank of front-end interleaved three-port output resonant converter.

The power transfer between the dc bus bar to dc load is regulated using modifying the phase shift angle Φ between the two sides switch bridges S_{Sux} of port 1 and S_{Pux} respectively, by altering the switching frequency, f_S and state of the art gating pulse by altering switch gate pulse width, δ for each interleaved branch and also restricting the operative output ports on secondary side of HF transformer to one for secondary to primary power transfer and vice-versa for FC and slow discharging. The use of a capacitor in a series *LC* resonant tank avoids the transformer saturation by significantly reducing DC current components that results from voltage drop asymmetry of the bridge, etc. Each of front-end three-phase interleaved branches are operated at a phase shift of 120° for the high output current along with significant ripple cancellation.

5.4.2 Steady state Equivalent Circuit Analysis

The proposed TPIBRC has three interleaved branches having a CLL series resonant tank at the input side of the multiport transformer, and each circuit is analyzed by taking into account only the fundamental components of voltage and current and neglecting all harmonics components known as approximate AC circuit analysis [15]. Although there are parasitic components present in switches, diodes, inductors, and capacitors, these are taken to be ideal to reduce the complexity of the derivation. The secondary side parallel inductors and the magnetizing inductance of the HF transformer for each branch have

been considered equivalent parallel inductors, and the leakage inductance of the transformer is being neglected, as shown in Fig. 5.14.

The equivalent circuit is simplified considering all the parameters and components of secondary side referred to the primary side of respective HF transformer for each interleaved branch and denoted as R'_o, i'_o, v'_o for the load resistance R_o, output current i_o and output voltage v_o respectively. The ac component of load side current, i_{sec} referred to the dc bus bar side is denoted as i'_{sec}. Considering the fixed voltage DC load and capacitive filter resistive load, the two equivalent circuit analysis done which could be applicable to any load with power $P_o = v_o'^2/R'_F$, $R'_o = R'_F$ where R'_F being resistance on full load when referred to bus bar side. Considering the applicable analysis objective, all equations are represented in per unit using the base value for normalization as in [12], the equations (5.27) to (5.33) has been referred from [12] to proceed with analysis.

Fig. 5.14 represents the equivalent circuit in which each branch CLL-tank circuit separates the two voltage sources V_{AB} across the terminals AB and V'_{CD} across the terminal's CD referred to dc bus side. Also, V'_{CD} is phase-shifted by Φ from V_{AB}. The two-voltage source V_{AB} and V'_{CD} is represented in the normalized fundamental component as follows:

$$V_{AB,f,pu} = \left(2/\pi\right)\left(1 - cos\delta\right)\sin(\omega_S t) \tag{5.27}$$

$$V'_{CD,f,pu} = \left(4M/\pi\right)\sin(\omega_S t - \phi) \tag{5.28}$$

The series tank current of each xth interleaved branch (where $x = 1, 2, 3$) for the primary side in normalized is obtained using the principle of superposition as follows:

$$i_{S_x,pu} = \left(\frac{V_{AB,f,pu} - V'_{CD,f,pu}}{X_{S,pu}}\right) \tag{5.29}$$

From (5.27), (5.28) and (5.29), it can be written as follows:

$$i_{S_x,pu} = \left(\frac{2}{\pi Q\left(F-\frac{1}{F}\right)}\right)\times\left[\left(1 - cos\delta\right)\cos(\omega_S t) - 2M\cos\left(\omega_S t - \phi\right)\right] \quad 5.30$$

$$V_B = V_S; Z_B = R'_F; i_B = V_B / Z_B$$

Each parallel inductor, L_{PX} current in normalized form is

$$i_{P_x,pu} = \left(\frac{4M}{\pi X_{P,pu}}\right) = \left(\frac{4M\lambda}{\pi QF}\right)\cos(\omega_S t - \phi) \quad 5.31$$

Thus, subtracting expression (5.31) for each parallel inductor current from respective series tank current expression (5.30) and simplifying, the load side current referred to the dc bus side of each *m* nos. of port (*m = a, b, c*) of each interleaved branch can be obtained, and it is given as follows:

$$i'_{SC,mx,pu} = \left(\frac{2}{\pi Q\left(F-\frac{1}{F}\right)}\right)\times\left\{(1-\cos\delta)\cos(\omega_S t) - 2M\cos(\omega_S t - \phi)(1+K)\right\} \quad 5.32$$

where,

$$K = \lambda\left(1 - 1/F^2\right) \quad 5.33$$

Evaluating (5.30) and (5.32) at $\omega_S t = 0$ and ϕ, the following soft-switching conditions for the two bridges is obtained:

$$i_{S_X,pu}(0) < 0 \quad 5.34$$

for each interleaved branch primary side switches ZVS operation, and

$$i'_{SC_{mx},pu}(\phi/\omega) > 0 \quad 5.35$$

for each port of each interleaved branch secondary side switches ZVS operation.

The condition could be further expressed as follows:

$$\frac{2(2M\cos\phi-(1-\cos\delta))}{\pi Q\left(F-\frac{1}{F}\right)}<0 \tag{5.36}$$

$$\frac{2(2M(1+K)-(1-\cos\delta)\cos\phi)}{\pi Q\left(F-\frac{1}{F}\right)}>0 \tag{5.37}$$

The Zero Voltage Switching (ZVS) condition is determined at extreme condition considering $\delta=\pi$ and therefore the expression to obtain the full ZVS range for each interleaved branches primary and secondary bridges is

$$\cos\phi=\min\left(\frac{1}{M},M(1+K)\right) \tag{5.38}$$

The above condition as in (5.38) for soft switching could be satisfied by taking the value of both 1/M and M(1+K) as greater than 1 since the max value of cos is 1. To satisfy ZVS condition, in primary side M should be less than 1 and to satisfy ZVS condition in secondary side the value of K and hence, should be selected correctly.

The peak current in series tank of each interleaved branch obtained from (5.30) can be expressed as

$$i_{S_{xPeak},pu}=\left(\frac{2}{\pi Q\left(F-\frac{1}{F}\right)}\right)\times\sqrt{\left[(1-cos\delta)^2+4M^2-4M(1-cos\delta)\cos\phi\right]} \tag{5.39}$$

The peak voltage of tank capacitor in series tank of each interleaved branch is given by

$$V_{C_{xPeak},pu}=\left(\frac{2}{\pi(F^2-1)}\right)\times\sqrt{\left[(1-cos\delta)^2+4M^2-4M(1-cos\delta)\cos\phi\right]} \tag{5.40}$$

The peak output port current referred to dc bus side is of each port of each interleaved branch obtained from (5.32) given as follows:

$$i'_{\mathrm{SC},mx_{Peak},pu} = \left(\frac{2}{\pi Q\left(F - \frac{1}{F} \right)} \right) \times \frac{}{\sqrt{[(1-\cos\delta)^2 + 4M^2(1+K)^2 - 4M(1+K)(1-\cos\delta)\cos\phi]}} \quad 5.41$$

The total load side current referred to dc bus side is given by

$$i'_{\mathrm{sec},pu} = i'_{\mathrm{SC},1,pu} + i'_{\mathrm{SC},2,pu} + i'_{\mathrm{SC},3,pu} \quad 5.42$$

where,

$$\begin{aligned} i'_{\mathrm{SC},1,pu} &= i'_{\mathrm{SC},a1,pu} + i'_{\mathrm{SC},b1,pu} + i'_{\mathrm{SC},c1,pu} \\ i'_{\mathrm{SC},2,pu} &= i'_{\mathrm{SC},a2,pu} + i'_{\mathrm{SC},b2,pu} + i'_{\mathrm{SC},c2,pu} \\ i'_{\mathrm{SC},3,pu} &= i'_{\mathrm{SC},a3,pu} + i'_{\mathrm{SC},b3,pu} + i'_{\mathrm{SC},c3,pu} \end{aligned} \quad 5.43$$

The dc bus side to load side instantaneous power P_{PS} is calculated taking voltage, $V'_{CD,f,\mathrm{pu}}$ times the current, $i'_{\mathrm{sec,pu}}$ product [15] such that each output port current of each secondary branch is equal and further simplifying the output power is expressed as follows:

$$P_{\mathrm{PS},pu} = mx\left(\frac{4M}{\pi^2 Q\left(F - \frac{1}{F} \right)} \right)(1-\cos\delta)\sin\phi \quad 5.44$$

The secondary to primary side instantaneous power P_{SP} where, only one output port of each interleaved branch is active is expressed as follows:

$$P_{\mathrm{SP},pu} = x\left(\frac{4M}{\pi^2 Q\left(F - \frac{1}{F} \right)} \right)(1-\cos\delta)\sin\phi \quad 5.45$$

A square wave with peak amplitude v'_{O} represents the fundamental component load voltage $V'_{\mathrm{CD},f}$. Thus, rms value of load voltage fundamental component, across terminal CD and current referred to dc bus sideis given as follows:

$$V'_{\mathrm{CD},f,r} = \left(\frac{2\sqrt{2}}{\pi} v'_O\right) \tag{5.46}$$

$$i'_{\mathrm{sec},r} = \left(\frac{\pi}{2\sqrt{2}} i'_O\right) \tag{5.47}$$

The circuit is analyzed replacing the filter capacitor and load resistance, R_O by ac equivalent resistance R_{ac} which is obtained taking into consideration only fundamental component [14] of voltage divided by current expressed as

$$R_{ac} = \left(8/\pi^2\right) R'_O \text{ where, } R'_O = R_O / n^2 \tag{5.48}$$

The ac equivalent resistance in normalized form is

$$R_{ac,pu} = \left(\frac{8R'_O}{\pi^2 R'_F}\right) \tag{5.49}$$

Where $R'_O = R'_F$ is the output resistance referred to primary side at full load. The expression for the fundamental component of rms voltage across terminal AB:

$$V_{\mathrm{AB},f,r} = \left(\frac{\sqrt{2}}{\pi} v_S\right)(1\text{-}\cos\delta) \tag{5.50}$$

The input bus voltage is reference voltage in phasor form Thus, impedance network voltage gain can be expressed as

$$\frac{V'_{\mathrm{CD},f,r}}{V_{\mathrm{AB},f,r}} = \left| \frac{R_{ac,pu} \times jX_{P,pu}}{X_{S,pu} + R_{ac,pu} \times jX_{P,pu}} \right| \tag{5.51}$$

Comparing equation (5.46) and (5.50) we get each port each interleaved branch voltage gains as follows:

$$M = \frac{v'_O}{V_S} = \frac{1-\cos\delta}{2} \frac{V_{CD,f,r}}{V_{AB,f,r}} \tag{5.52}$$

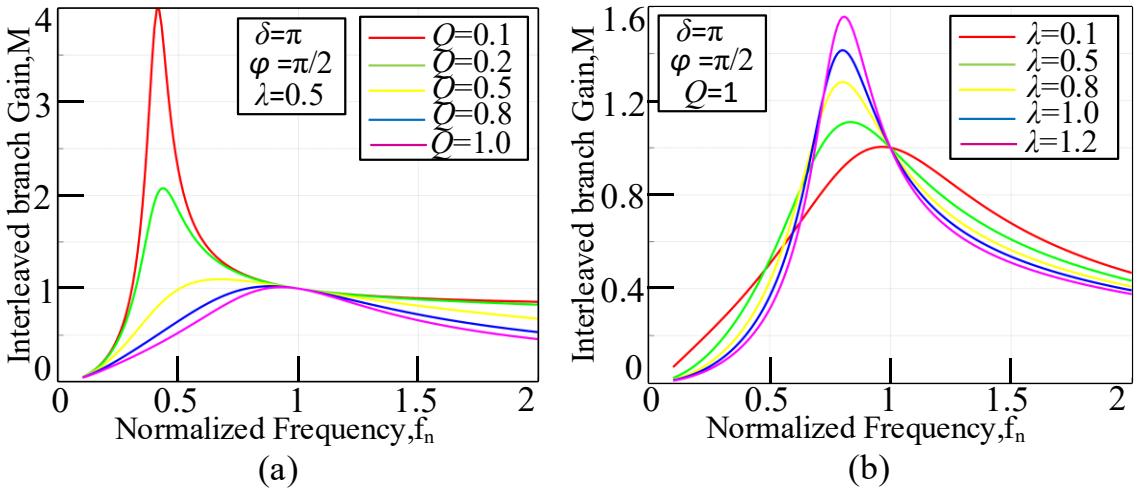
Using equation (5.52) simplification of (5.51), we get

$$M = \frac{(1-\cos\delta)\,\mathrm{Sin}\,\phi/2}{\sqrt{\left(1+\lambda\frac{1}{(1-F^2)}\right)^2+\left(\frac{\pi^2}{8}Q\left(F-\frac{1}{F}\right)\right)^2}} \qquad 5.53$$

The expression in (5.53) shows the relationship of gain, M for each port each interleaved branch is dependent on the modified gating for varying pulse width δ, phase shift Φ, normalized frequency F, Load Quality factor Q, and normalized inductance λ.

5.4.3 Design Trade Off

Each interleaved branch gain is summation of CLL resonant tank gain and the transformer. The gain contribution of resonant tank is dependent on the value of load, resonant and switching frequency, tank inductance and capacitance whereas gain contribution of transformer is constant contingent upon the transformer turn ratio and it contributes for only change in voltage level and does not amplify the signal. The front-end input voltage level of each interleaved branch is same and expected to vary depending on the variation in bus voltage, the transformer turn ratio being fixed for obtaining fixed output voltage at output port of each interleaved branch the resonant tank of each interleaved branch must compensate. Thus, as the variation in input voltage for each branch is same the tank value must be identical to compensate for the variation such that if the level of bus voltage is high or low than the nominal value then tank is to compensate accordingly by changing the gain of resonant tank. The derived mathematical results in previous section have to be utilized for obtaining design curves to get the tank and turn ratio values for each multi output port interleaved branch of the TPIBRC.



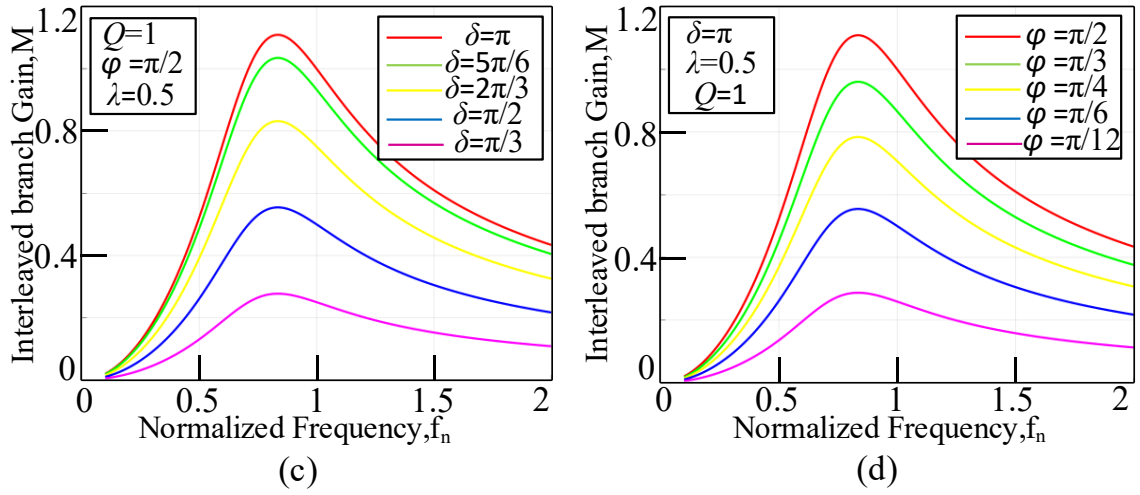


Fig. 5.15 Variation of interleaved branch Gain, *M* corresponding to normalized frequency, *F* for a) various quality factor, *Q* b) various normalized inductance, *λ* c) various gate pulse, *δ* d) various phase shift, *Φ*.

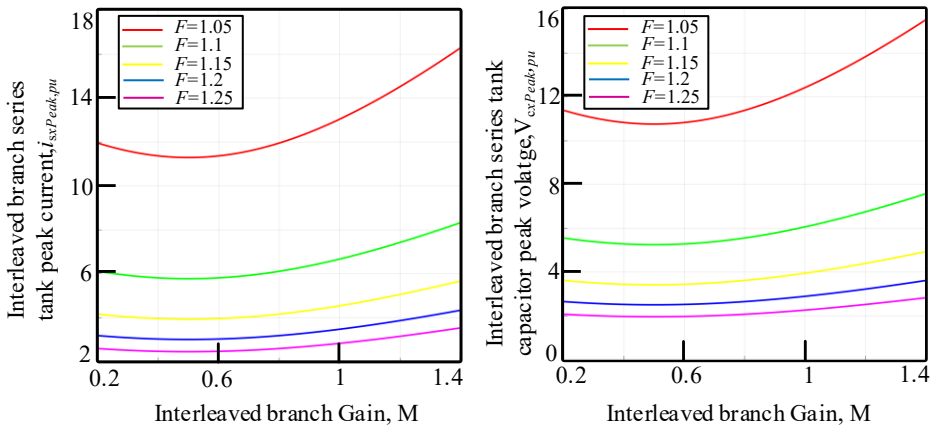


Fig. 5.16 (a) Variation of interleaved branch series tank peak current, i_{sxPeak} versus interleaved branch Gain, (b)Variation of interleaved branch series tank capacitor voltage, V_{cxPeak} versus interleaved branch Gain *M* for varying normalized frequency, *F*.

The design curve provides all the parameters required to selected including converter gain M for each branch, normalized switching frequency F and hence tank component for each branch, normalized inductance λ and hence the parallel inductance value of each branch, and quality factor Q depending upon the loads. Fig. 5.15 shows the plot for interleaved branch Gain, *M* corresponding to normalized frequency, *F* a) for various value

of quality factor, Q depending on load. It is inferred that there is large inductive operative region for light load condition and lower inductive operating region for full load condition. The inductive region is stable operating region as gain reduces with increase in normalized frequency and could be used to control gain by controlling switching frequency.

The capacitive region is unstable region as the gain reduces with reduction in normalized frequency leading to the state of instability leading to maloperation of the converter. The state of stable operation is the necessity for all range of loads thus the extreme worst case of full load is considered such that Q=1.0. b) for various value of normalized inductance, λ depending on resonant tank series inductance, L_{sx}. It is seen that the operating region is larger for large value of series inductance, but as the normalized inductance is lower there is lower magnetizing current leading to higher efficiency, thus a trade-off is required for high operating region and efficiency. c) and d) for various values of gate pulse, δ and phase shift, Φ which shows that the value of gain decreases with decrease in gate pulse, δ and phase shift, Φ respectively and thus used to control the power output depending upon the load requirement.

The switching frequency of converter is kept such as each interleaved branch operates in corresponding inductive region and the ZVS soft switching is achieved for all primary switches and constant output voltage is achieved with high efficiency. Also, from Fig. 5.16 shows variation of interleaved branch series tank peak current, i_{sxPeak} and tank capacitor voltage, V_{cxPeak} versus interleaved branch Gain M respectively for varying normalized frequency, F it is seen that as the normalized frequency and hence the switching frequency increases the tank peak current and peak voltage reduces for wide range of gain, M. Hence, it is advantageous to operate in the region of higher operating frequency and lower gain, M subjected to system requirement. The converter is operated at such switching frequency such as each interleaved branch operates in inductive region and the ZVS soft switching and constant output voltage is achieved with high efficiency.

The following are the design requirements for the CLL-type TPIBRC: DC busbar or source ideal voltage, $v_{S,nom}$= 360V, and input voltage deviation is taken into account such as $v_{S,max}$ = 370V and $v_{S,min}$ = 350V, maximum output power is 3.3kW at constant output voltage, v_O = 72V, max output current, i_O = 45A, resonant frequency, f_r = 50kHz. The multiport transformer primary secondary turn ratio is considered as, n:1:1:1 = 5:1:1:1 and

input voltage range, the value of M_{max}= 1.03 and M_{min}= 0.97. Considering the range of required gain at worst case condition of full load that is Q= 1, δ= π and Φ= π/2, the min and max operating normalized frequency is obtained from Fig. 3 such that F_{min}= 0.93 and F_{max} = 1.08 respectively and the critical value of normalized inductance is taken as, λ=0.5. The full load resistance is $R_F = v_O^2/P_O$=1.6Ω, therefore R'_F =40Ω. From equation (5.27) to (5.33) of [12] the base values V_B=360V, Z_B=40Ω and I_B=9A and the tank parameters of each interleaved branch can be calculated as L_{rx}=127 μH, C_{rx}=0.0795 μF, L_{px}=254 μH. Noteworthy, is the fact thatL_{mx} and L_{rx} also comprise of the magnetizing and leakage inductance respectively of each multiport HF transformer. Therefore, contingent of the magnetizing inductance the value of series tank inductance, L_S and L_{S1}, L_{S2}, L_{S3}, connected parallel on load side is calculated. The three interleaved branch are phase shifted by 120^0.

5.4.4 Simulation Results and Discussion

The previous section design parameters are used to simulated the proposed TPIBRC in MATLAB. In order to control power transfer from either side of TPIBRC is done by regulating the switching frequency, f_S phase shift, Φ and pulse width, δ. Considering full load and each interleaved branch primary side switches pair operating for 50% duty cycle with phase shift of 120^0 from each interleaved branch the results are captured. The simulation result in Fig. 5.17(a)-(c) shows that at input voltage v_S=360V and switching frequency, f_S being equal to resonant frequency, f_r at 50kHz all the resonant tank capacitor voltage, $V_{Cr,x}$ and current, $i_{r,x}$ of each branch of TPIBRC is in resonance such that the voltage is minimum when current is at peak and current is minimum when voltage is at peak. The primary and secondary voltage is shown as $V_{AB,x}$ and $V_{CD,x}$ for each branch respectively and output current of each secondary port of each branch is shown as $i_{sc,mx}$. As the TPIBRC has multiport transformer, the high current output of i_{sec}=45A is achieved compared to single port output and due to front end interleaving of three branches the ripple current is reduces to large extent as shown in simulation result Fig. 5.17(d). The individual port output current of each interleaved branch is $i_{sc,mx}$ and each interleaved branch output current is $i_{sc,x}$ and the output current of converter is i_{sec}.

Fig.5.18 shows that each primary side switches of interleaved branches operate in ZVS soft switching and hence reducing the switching losses and increasing the efficiency.

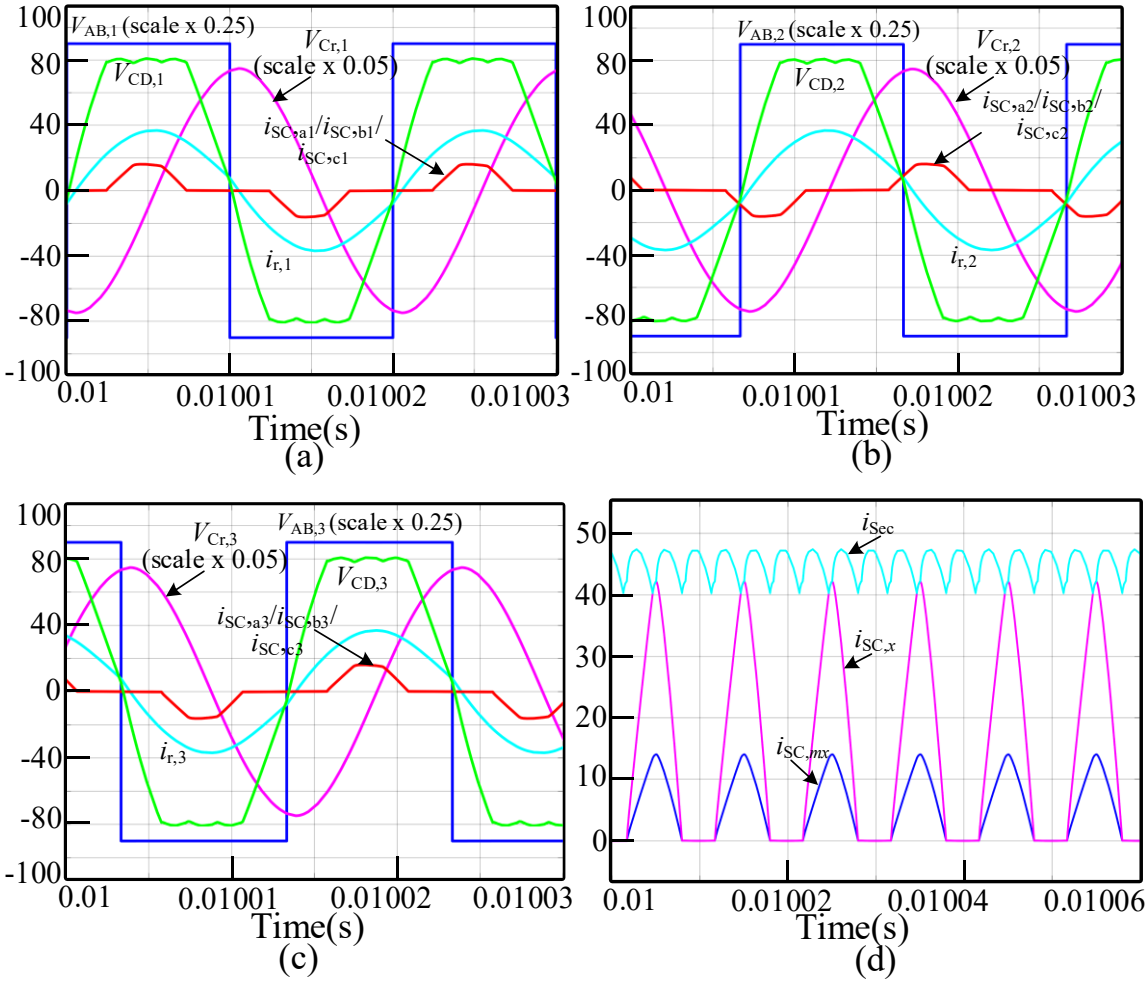


Fig. 5.17 TPIBRC waveforms for full load FC such as all the primary switches operate in ZVS soft switching when gain, M_{nom}=1, normalized frequency, F_{nom}=1 for v_S = 360V and f_S= f_r =50kHz.for (a) 1st branch (b) 2nd branch (c) 3rd branch (d) Simulation waveform of secondary ripple current for each output port and combined output.

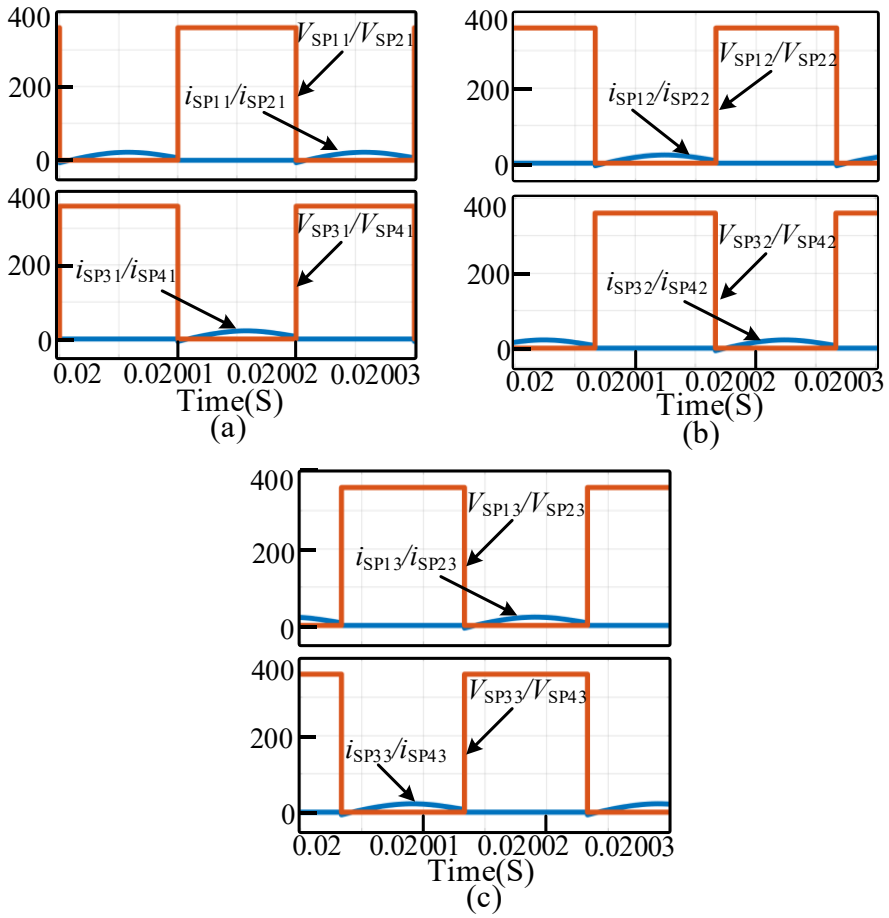


Fig. 5.18 Soft switching primary side switches switching waveform of all interleaved branches for v_S = 360V and f_r =f_S= 50kHz (a) 1st branch, (b) 2nd branch, and (c) 3rd branch.

5.5 Conclusion

An extensive analysis of interleaved multiport resonant converters designed for high-power charging and discharging infrastructures was provided in this chapter. The basic features of resonant converter topologies were first examined, emphasizing the benefits, drawbacks, and working principles of the SRC, PRC, LLC, CLL, and CLLC resonant converters. Because of its streamlined resonant tank, lower circulating current, enhanced soft-switching capability, and compatibility with interleaved multiport architectures, the CLL resonant topology was determined to be the best option for the suggested converter based on the comparative evaluation.

The unidirectional and bidirectional interleaved multiport resonant converters were then designed and characterized. In order to distribute the output current among several converter branches and significantly lessen the current stress on individual semiconductor

devices and transformer windings, the suggested converter configurations use three-phase interleaving in conjunction with multiport HFTs. The suggested architecture lowers the peak current handled by each transformer port to about one-third when compared to traditional single-port converters. This leads to decreased conduction losses, better thermal performance, smaller transformers, and increased overall power density.

The switching sequences, resonant energy transfer methods, and design considerations of the suggested converters were used to analyze their operational characteristics. Modified switching tactics, such as switching frequency variation and proper regulation of the primary and secondary bridge switching patterns while preserving operation in the inductive area, were demonstrated to efficiently regulate converter output power. All primary-side switches effectively accomplish ZVS throughout a broad working range by making sure the switching frequency stays higher than the resonant frequency. This reduces switching losses and boosts conversion efficiency.

The efficacy of the suggested converter topologies under realistic operating conditions was further confirmed by the simulation studies. The 3.3 kW unidirectional interleaved resonant converter maintained a regulated 48 V output appropriate for high-current fast-charging applications while exhibiting stable operation over an input voltage range of 460–510 V. Comparably, over an input voltage range of 350–370 V with a regulated 72 V output, the 3.3 kW TPIBRC accomplished effective charging and controlled discharging performance. The success of the suggested resonant tank design and switching approach was confirmed by the fact that all interleaved branches in both converter configurations maintained soft-switching operation.

Chapter 6

Modeling of Four-Port DC-DC Converter for Battery-Supercapacitor-Based System

6.1 Introduction

The reduction in grid dependency and the intermittent nature of solar PV (SPV) sources have increased the need for the reliable integration of HES systems to ensure efficient energy management and effective handling of dynamic load conditions. Although batteries offer high energy density, their performance and lifecycle are reduced under dynamic load conditions with high-power requirements during transient events. BSCES systems provide an effective solution for energy management with improved transient performance. The selection of converter topologies for the integration of BSCES, along with control strategies for power sharing, bidirectional power flow, and maintaining system stability under varying operating conditions, is a primary concern of HES systems [73]-[76].

6.1.1 Need for Battery–Supercapacitor HESS

The converter topologies with BSCES systems are reported in the literature [102]-[103]. The selection of the converter topology also depends on the application, such as EV applications [73], [75], renewable energy integrations (REI) [71], [103], etc. A conventional BSCES system for light EV (LEV) is shown in Fig. 6.1 (a).

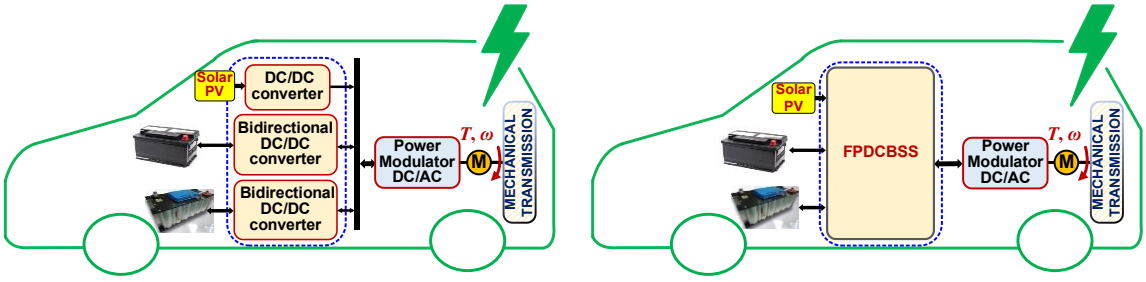


Fig. 6.1 Light EV propulsion system with (a) conventional BSCES converter topology and (b) proposed FPDCBSS topology.

6.1.2 Motivation for the Development of Multiport DC–DC Converters

The primary concern of the on-board converter topologies is cost effectiveness, reduced size and high efficiency for increasing the vehicle milage. The MPC topologies provide the solution with reduced number of switching devices with improved efficiency with effective coordination of power flow between multiple input-output ports [67]-[68]. In [67], a simplified switched-boost-action-based MPC topology with reduced switch count and bidirectional power flow capability for coordinating the load power demand with the input source and battery is presented. By reducing the number of conversion stages and switch counts, it improves efficiency with decreases switching losses. A bidirectional high step-down three-switch MPC with wide voltage conversion capability, reduced component count, and effective load-voltage regulation is presented in [72].

The literature has documented a variety of control strategies for controlling the power sharing between the load and ESSs [14], [80]. State-machine and rule-based controllers [80] are easy to design, but they frequently show little flexibility when the load circumstances change quickly. Although intelligent methods like fuzzy logic, neural networks, and optimization-based energy management systems [31] have shown better power allocation skills, they often need large amounts of processing power, training data, or precise system models. To improve dynamic performance and robustness, advanced control techniques like sliding mode control, adaptive control, and model predictive control [22] have also been studied; however, their implementation complexity and computational burden greatly increase for real-time implementations.

Frequency-decoupling-based [15], [23] control has become one of the more appealing energy management techniques for BSCES systems. With this method, the supercapacitor compensates for the high-frequency transient component of the load power demand while the battery handles the low-frequency component. The battery can supply the average energy demand while the SC can react to abrupt power variations, which successfully takes advantage of the complementing qualities of both storage devices [14]. As a result, there is a considerable decrease in battery current stress, charge-discharge cycling, and thermal degradation, which extends battery life and increases system reliability. Due to its simplicity, ease of implementation, and excellent dynamic performance, low-pass and high-pass filter based control structures have been effectively used for HES system

applications in a number of studies [15].The need for sophisticated energy storage technologies that can provide high power density, quick transient response, and extended operating lifetime has grown dramatically due to the growing use of renewable energy sources and the quick electrification of transportation networks. Lithium-ion batteries are frequently used as the main energy storage source in EVs, DC microgrids and other applications due to their high energy density among the current energy storage technologies. However, batteries are prone to accelerated aging under frequent high-current charging and discharging circumstances, have a limited power density, and have relatively slow electrochemical kinetics. Supercapacitors, on the other hand, exhibit remarkable power density, quick charge-discharge capability, and superior cycling durability. However, their capacity to independently meet the long-duration energy requirements of electric propulsion systems is limited by their comparatively low energy density. As a result, neither technology alone can meet the dynamic power needs found in real-world EV applications.

6.1.3 Objectives and Scope of Converter Modeling

By combining the complementing qualities of both storage devices, BSCES have become an efficient way to get around these restrictions. In a HESS, the supercapacitor makes up for short-term power fluctuations brought on by quick acceleration, regenerative braking, and abrupt load changes, while the battery is mostly in charge of meeting the average energy demand over long periods of time. The reliability of EV powertrains and DC microgrid etc. is increased, battery longevity is increased, thermal stress is decreased, and overall system efficiency is greatly improved by such coordinated operation.

HES systems employing batteries and supercapacitor have attracted significant attention due to their ability to improve system lifetime and dynamic response [28], [78]. MPC topologies enable effective power flow management among different energy sources and storage elements. The common-ground configuration simplifies the converter structure [70]. In addition, fewer conversion stages result in improved efficiency, reduced switching losses, and lower system cost, making these converters suitable for off-grid solar and LEV applications.

The control-oriented modeling of FPDCBSS is presented in this chapter. The MPC architecture for a LEV is shown in Fig. 6.1 (b). It provides independent control of power flow across three of its four ports while maintaining overall power balance.

6.2 Classification of Power-Converter Configurations for HESS

The power-converter interface plays an important role in determining the power-sharing capability, dynamic performance, efficiency, and controllability of a battery–supercapacitor HESS. Since the battery and supercapacitor have complementary characteristics, the converter configuration should allow their individual characteristics to be utilized effectively. Depending on the electrical connection of the storage elements with the DC bus and the location of the power electronic interface, HESS converter topologies can be broadly classified as passive, semi-active, series-active, parallel-active, isolated-active, and multi-level active configurations, as shown in Fig. 6.2.

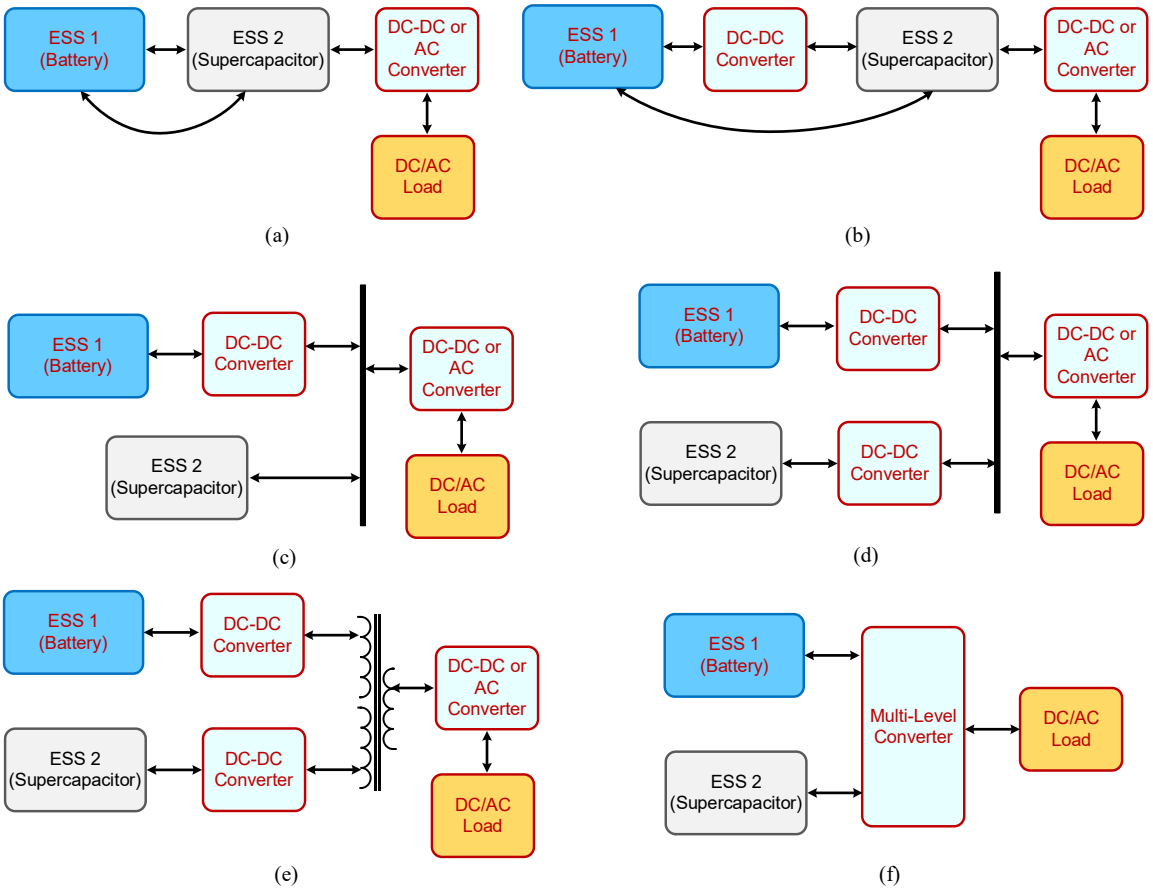


Fig. 6.2 Classification of HESS power-converter topologies: (a) passive, (b) semi-active, (c) series-active, (d) parallel-active, (e) isolated-active, and (f) multi-level active.

6.2.1 Passive HESS Configuration

In the passive configuration shown in Fig. 6.2 (a), the battery and supercapacitor are directly connected to the DC bus without dedicated DC–DC converters. Consequently, the power contribution of the two storage elements is mainly determined by their terminal voltage characteristics and internal impedances. The principal advantage of this configuration is its simple structure and low component count. Since no dedicated converter is required for either storage element, the associated switching losses, control requirements, and hardware complexity can be reduced. However, independent control of the battery and supercapacitor currents is not possible.

6.2.2 Semi-Active HESS Configuration

The semi-active configuration shown in Fig. 6.2 (b) introduces a bidirectional DC–DC converter between one storage element and the DC bus, while the other storage element remains directly connected to the bus. The addition of a converter provides controlled power flow for one of the storage elements and improves the operating flexibility compared with the passive configuration. The converter can regulate the current or voltage of the actively controlled storage device and thereby improve DC-bus voltage regulation and energy utilization. However, the storage element directly connected to the DC bus remains strongly dependent on the bus voltage and does not have independent power-flow control.

6.2.3 Series-Active HESS Configuration

In the series-active configuration, shown in Fig. 6.2 (c), the converter associated with one storage element is connected in series with the other storage element or with the DC power path. The converter therefore controls the voltage contribution of the actively interfaced storage unit while the remaining storage element participates directly in the main power path. The series connection can provide an effective means of regulating the combined storage voltage and controlling the contribution of the actively interfaced device. It can also reduce the power processed by the converter under suitable operating conditions because the converter may process only a portion of the total system power.

6.2.4 Parallel-Active HESS Configuration

The parallel-active configuration shown in Fig. 6.2 (d) employs separate bidirectional DC–DC converters for the battery and supercapacitor. Both storage elements are therefore actively interfaced with the DC bus. This arrangement provides independent control of battery and supercapacitor currents and is particularly suitable for coordinated power management. The battery can be assigned to supply the relatively slow-varying or average component of the load power, whereas the supercapacitor can respond to rapid changes in power demand. Such power sharing can reduce high-frequency current variations in the battery and consequently reduce unnecessary battery stress.

6.2.5 Isolated-Active HESS Configuration

The isolated-active configuration shown in Fig. 6.2 (e) incorporates HF transformer-based power conversion to provide galvanic isolation between the storage elements and the DC bus. The use of a high-frequency transformer provides electrical isolation and enables a wide voltage-conversion ratio. Such configurations are attractive when the storage voltage and DC-bus voltage differ significantly or when isolation is required by the application. Bidirectional isolated DC–DC converters can also provide controlled power transfer in both charging and discharging directions.

6.2.6 Multi-Level Active HESS Configuration

The multi-level active configuration shown in Fig. 6.2 (f) employs multiple semiconductor switching levels to process the energy between the storage system and the DC load or bus. Multilevel structures can reduce the voltage stress experienced by individual semiconductor devices and can improve the quality of the converter voltage waveform. These characteristics make multilevel configurations attractive for medium- and high-power applications. They can also provide improved scalability and facilitate operation at higher DC-bus voltage levels.

6.2.7 Comparative Discussion and Selection of HESS Configuration

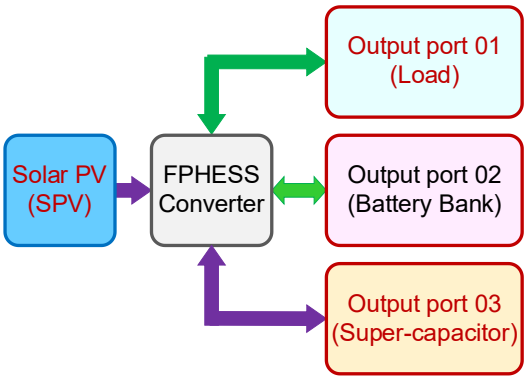
The six configurations shown in Fig. 6.2 provide different levels of controllability and hardware complexity. The passive configuration offers the simplest implementation but provides limited control over individual storage currents. The semi-active configuration

improves controllability by actively interfacing one storage element. The series-active configuration provides controlled voltage contribution while potentially reducing the power processed by the converter under appropriate operating conditions. The parallel-active configuration provides independent control of both storage devices but requires separate converter stages. The isolated-active configuration provides galvanic isolation and flexible voltage conversion, whereas the multi-level active configuration is particularly suitable for higher voltage and power applications. For the battery–supercapacitor system considered in this thesis, the complementary dynamic characteristics of the two storage devices need to be exploited through coordinated power sharing. The battery is intended to provide the relatively slow-varying component of the power demand, while the supercapacitor is required to respond rapidly to transient variations. Therefore, independent control of the two storage ports is desirable. Although a parallel-active configuration can provide this functionality, it requires separate bidirectional converter stages for the battery and supercapacitor. This increases the number of semiconductor devices and passive components and results in multiple power-processing stages. These limitations motivate the investigation of a multiport converter-based HESS architecture, in which the source, battery, supercapacitor, and DC load can be integrated through a common power-conversion structure. Accordingly, the subsequent section presents the converter topology developed in this work. The proposed configuration aims to retain the required bidirectional power-flow capability and coordinated battery–supercapacitor power sharing while reducing the number of active switching devices and simplifying the overall power-conversion structure.

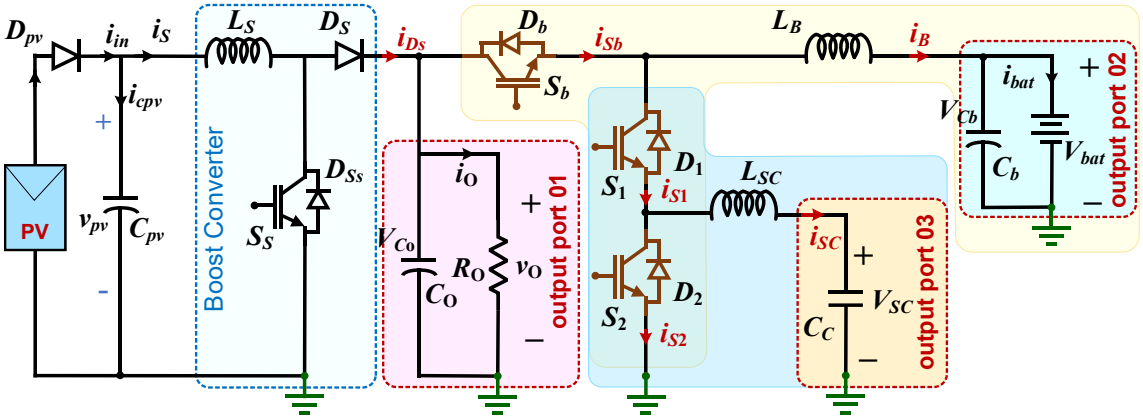
6.3 Configuration of the Proposed Four-Port DC–DC Converter

The block diagram of the proposed FPDCBSS system is shown in Fig. 6.3 (a). It is designed to manage energy flow between the SPV source, battery, SC, and load. The circuit diagram of the proposed converter is shown in Fig. 6.3 (b); it comprises an SPV-side simple boost converter for maximum power point (MPP) tracking connected with a MPC for BSCES. The SPV source is acting as the primary energy source. The converter has three output ports with bidirectional power flow capability, such as output port 01 for a medium voltage load, i.e., output port 01; for a battery load, i.e., output port 02; and for

an SC load, i.e., output port 03. The FPDCBSS-based converter has SPV MPP tracking control using a boost converter and DC bus voltage regulation control using BSCES.



(a)



(b)

Fig. 6.3 Proposed four-port DC-DC converter for battery-supercapacitor-based storage (FPDCBSS): (a) block diagram and (b) schematic circuit diagram.

The FPDCBSS consists of four active switches, S_S, S_b, S_1, and S_2, for the integration of SPV, battery, SC, and load. The switching states are coordinated such that each storage element can operate either in buck mode (charging) or boost mode (discharging), enabling bidirectional power flow. In boost mode energy is transferred from energy storage elements to DC bus V_O, and in buck mode of operation the energy is stored by the energy storage elements. The FPDCBSS operates under several distinct states depending on the availability of SPV energy and the load demand. The semiconductor switch SS operates independently for SPV power harvesting, providing maximum power to the DC bus V_O.

6.3.1 PV Source (SPV) Port

The main renewable energy source, the PV array, is connected to the converter's first input port interprated as SPV-side of converter. When there is enough solar energy available, the PV system transforms solar irradiance into electrical energy and powers the DC bus. A PV array's output voltage and power fluctuate constantly throughout the day because they are dependent on solar irradiation and cell temperature. As a result, the converter needs to be able to handle large fluctuations in the input power while still operating steadily.

To maximize energy extraction from the solar panels, the PV source in actual renewable energy systems often functions under Maximum Power Point Tracking (MPPT) management. In order to ensure that the PV array works at its maximum power point even when environmental conditions change, the MPPT algorithm continuously modifies the converter operating point. The four-port converter controls the power transfer between the PV array and the common DC bus, even though the MPPT algorithm establishes the PV source's reference operating voltage operating in boost mode through switch S_S and diode D_S.

The PV source provides most of the load power during times of high sun irradiation. Depending on their respective levels of charge and the chosen energy management method, any extra energy produced over the instantaneous load need is used to charge the battery and/or the supercapacitor. On the other hand, the battery and supercapacitor make up for the power shortfall by meeting the necessary load demand when solar power is insufficient because of cloud cover or decreased irradiance.

The converter's operating mode is directly impacted by the PV source's dynamic behavior. As a result, PV voltage fluctuations are taken into account as one of the external disturbances enabling BSCES operation in buck or boost mode of operation.

6.3.2 Battery Port (Port 02)

The BESS and the common DC bus are connected via the second port of the suggested converter. The battery provides the average component of the load power and serves as the main long-term energy storage device. Because of its high energy density, the battery can store excess renewable energy for later use and maintain power delivery for long periods of time.

An inductor, L_B and a bidirectional switching configuration that permits both charging through S_b D_1, D_2 and discharging through S_1, S_2, D_b are used to link the battery port to the converter. The converter uses the buck mode to transmit energy from the DC bus to the battery during times of surplus solar generation, charging the battery. On the other hand, the converter runs in boost mode, enabling the battery to discharge and supply energy to the DC bus, when the available PV power is inadequate to meet the load demand.

Despite having a high energy density, batteries' electrochemical dynamics are slower than those of supercapacitors. Rapid cycles of charging and discharging raise internal temperature, mechanical stress, and electrochemical aging, all of which hasten battery deterioration. Consequently, the battery is purposefully tasked with providing only the low-frequency or slowly fluctuating portion of the load power in the suggested hybrid ESS. The supercapacitor handles high-frequency transient power needs, which lowers battery current ripple and greatly extends battery life.

One of the principle state variables taken into account in the mathematical model is the battery current, i_B which is also the main regulated variable in the robust controller design described in the following chapter.

6.3.3 Supercapacitor Port (Port 03)

The SESS is linked to the converter's third port. In contrast to batteries, supercapacitors have minimal internal resistance, nearly infinite charge-discharge cycles, a very high power density, and a very quick charging and discharging capabilities. These features allow the supercapacitor to react to abrupt power variations in the DC system extremely instantly.

Controlled bidirectional power flow is made possible by the supercapacitor's link with the converter via its own inductor, L_{SC} and bidirectional switching configuration. The converter enables the supercapacitor to drain quickly through S_2, D_1, D_b in order to support the DC bus during abrupt drops in solar power or sudden rises in load demand. Similarly, the converter captures excess energy by charging the supercapacitor through S_b, S_1, D_2 when the transient load demand drops or extra renewable power becomes available.

The supercapacitor is not designed to provide long-duration power support because it has a much lower energy density than the battery. Rather, its main purpose is to lessen the dynamic stress placed on the battery, decrease DC bus voltage variations, and adjust for high-frequency power transients. The hybrid energy storage approach used in this study is based on the complementary relationship between the battery and supercapacitor.

The converter state-space model explicitly represents the supercapacitor current,i_{SC} which is the second key controlled variable for designing the control method.

6.3.4 Regulated DC Load Port (Port 1)

The regulated DC load that the converter supplies is represented by the first port. The suggested converter is designed as a generalized DC power interface that can provide a wide range of DC applications, in contrast to application-specific converter models. Therefore, an EV traction system, a DC microgrid, a charging station powered by renewable energy, an industrial DC distribution network, a telecommunication power supply, a data center, or any regulated DC power system requiring continuous and stable voltage could be represented by the load connected to the common DC bus.

The converter's principal goal is to keep the DC bus voltage at its designated reference value in spite of changes in load demand, storage device operating circumstances, and renewable energy generation. Regardless of disruptions in the hybrid ESS, maintaining a steady DC bus voltage guarantees dependable operation of the linked load.

The solar source alone, the battery alone, the supercapacitor alone, or any combination of these sources may provide the load power, depending on the operating conditions. The suggested converter maximizes the use of renewable energy sources and reduces needless battery stress by continually coordinating the power supply of each source to meet the load demand.

An equivalent resistive load, R_O linked across the DC bus voltage, v_O is used to represent the load in mathematical modeling. While still being applicable to a wide range of realistic DC loads, this generalized model makes the derivation of the converter equations simpler.

6.4 Principle of Opeartion

The goal of the proposed four-port DC–DC converter is to enable effective and coordinated power exchange between the regulated DC load, BESS, SESS, and PV source. The converter must constantly control the direction and quantity of power flow while preserving a steady DC bus voltage because renewable energy sources are intermittent and practical DC loads are dynamic. The suggested converter concurrently controls several energy ports with different electrical characteristics and operating needs, in contrast to traditional two-port converters, where power transfer takes place between only one source and one load.

The converter's working principle is based on the controlled switching of semiconductor devices that use PWM to manage the charging and discharging of the inductive energy storage elements. Bidirectional energy transfer between the battery, supercapacitor, and common DC bus is made possible by the converter's ability to function in both buck and boost modes by suitably modifying the duty cycles of the active switches. Because of its bidirectional capabilities, the converter can adjust to constantly shifting operating conditions, including variations in solar irradiation, load demand, and the energy storage devices' state of charge.

The suggested converter is made to take advantage of the complementing energy storage properties of the battery and the supercapacitor by coordinating power management. The battery provides the average or slowly fluctuating portion of the load power due to its high energy density, while the supercapacitor compensates for abrupt transient power needs due to its high power density and quick dynamic response. The battery's operating lifetime is extended, system stability is improved, total converter efficiency is increased, and battery current stress is greatly reduced by such coordinated operation.

The instantaneous balance between the available PV power, the load power demand, and the energy stored in the battery and supercapacitor determines the power flow among the four ports from the standpoint of converter operation. The extra energy is used to charge the battery and/or supercapacitor whenever the solar source produces enough power to meet the load demand. On the other hand, the battery and supercapacitor provide the stored energy to make up for the power shortfall during times when solar generation

is insufficient. As a result, the converter minimizes needless battery cycling and maximizes the use of renewable energy sources while guaranteeing continuous power delivery.

The converter operation is divided into six different operating states in order to correctly depict these different operating circumstances. Different current routes, switching sequences, and power flow methods occur from each operational state, which corresponds to a distinct combination of battery and supercapacitor charging or draining conditions. The system's instantaneous energy balance and the control signals produced by the energy management algorithm determine which operating state is best.

The operational analysis in this chapter takes into account, that operating in CCM, the converter guarantees that the inductor currents stay constant during the switching cycle. When developing mathematical models, conduction losses, switching losses, and leakage currents are ignored because the semiconductor switches and diodes are initially considered to be perfect. With consistent inductance and capacitance values throughout the operating range, the passive components are regarded as linear and time-invariant. The use of the state-space averaging technique is justified by the assumption that the switching frequency is significantly higher than the converter's main dynamic frequencies. The DC bus capacitor is big enough to keep the output voltage almost constant during each switching cycle.

These presumptions maintain the prevailing dynamic properties needed for controller design while significantly simplifying the mathematical analysis. The accuracy of the converter model can then be increased by incorporating practical non-idealities into simulation studies.

6.5 Mathematical Modeling of the Proposed Four-Port DC–DC Converter

An accurate mathematical model that can describe the dynamic interaction between the solar source, BESS, SESS, and regulated DC load is necessary to build an efficient control strategy for a multiport power converter. Direct analysis of the proposed four-port converter using its instantaneous switching equations is computationally and mathematically challenging because it is a switched nonlinear system whose operating states constantly change based on the switching sequence of the semiconductor devices.

In order to correctly depict the converter dynamics and greatly simplify the ensuing controller design, an averaged mathematical model is created in this chapter.

Finding the dynamic link between the converter inputs, state variables, and output variables is the main goal of mathematical modeling. Converter stability, transient responsiveness, controllability, observability, and small-signal behavior can all be systematically analyzed with the help of such a model. Moreover, the transfer functions utilized in the robust controller design described in the following chapter are derived analytically from the mathematical model.

The detailed description of various states depending on the operation of S_b, S_1 and S_2 are characterized under different operating conditions and presented as follows:

6.5.1 State-I Operation ($P_{SPV} < P_O$):

The transient condition under *state*-I of operation arises due to sudden increase in the load demand, i.e., SPV power P_{SPV} is less than sudden load power P_O demand. In this state both the battery and SC operate in boost mode of operation to supply power to the DC bus to meet high load demand conditions. The switches S_1 and S_2 act as the active energy transfer switches, and the diodes D_b and D_1 operate in order to regulate current, as depicted in the switching and current characteristics diagram in Fig. 6.4 and Table 6.1. The detailed current path under all three modes (i.e., modes M_1, M_2, and M_3) is presented in Fig. 6.5 to relate the characteristics presented in Table 6.1, where T is the switching period.

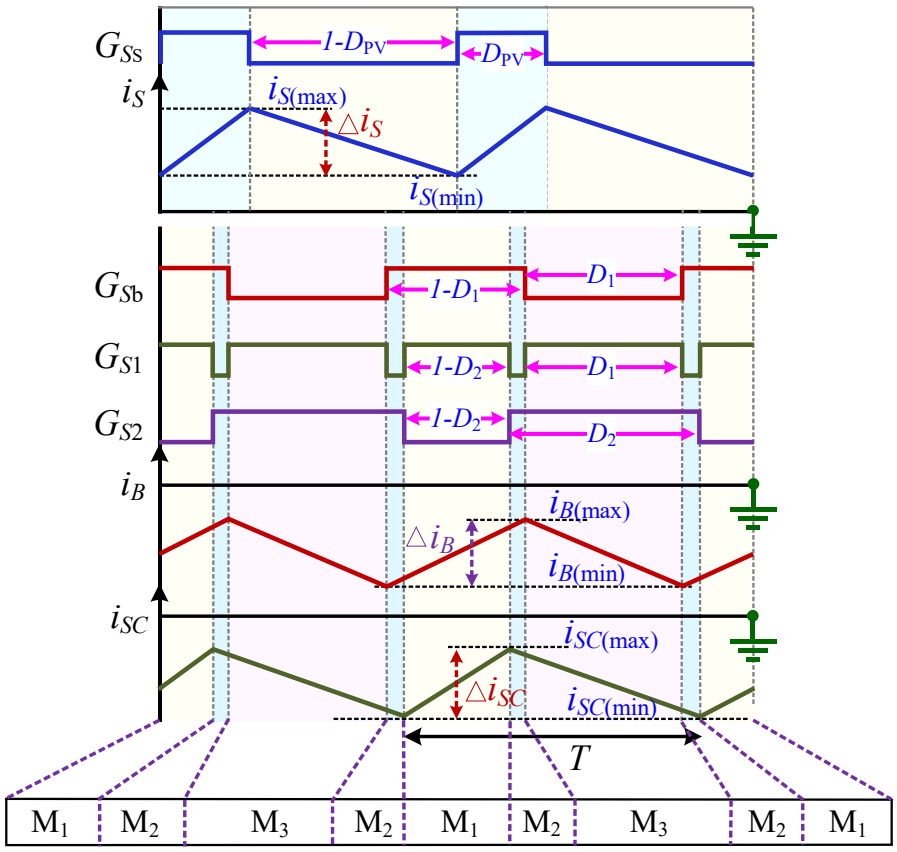


Fig. 6.4 Switching pattern and current characteristics of the FPDCBSS under *State*-I operation.

TABLE 6.1

POSSIBLE MODES UNDER TRANSIENT CONDITIONS UNDER STATE-I

Mode	**Duration**	**Current Characteristics**	**Active Switches**
M_1	$(1-D_2)\times T$	$i_B \downarrow, i_{SC} \downarrow$	D_1, D_b
M_2	$\{(D_2-D_1)/2\}\times T$	$i_B \downarrow, i_{SC} \uparrow$	D_b, S_2
M_3	$D_1\times T$	$i_B \uparrow, i_{SC} \uparrow$	S_1, S_2

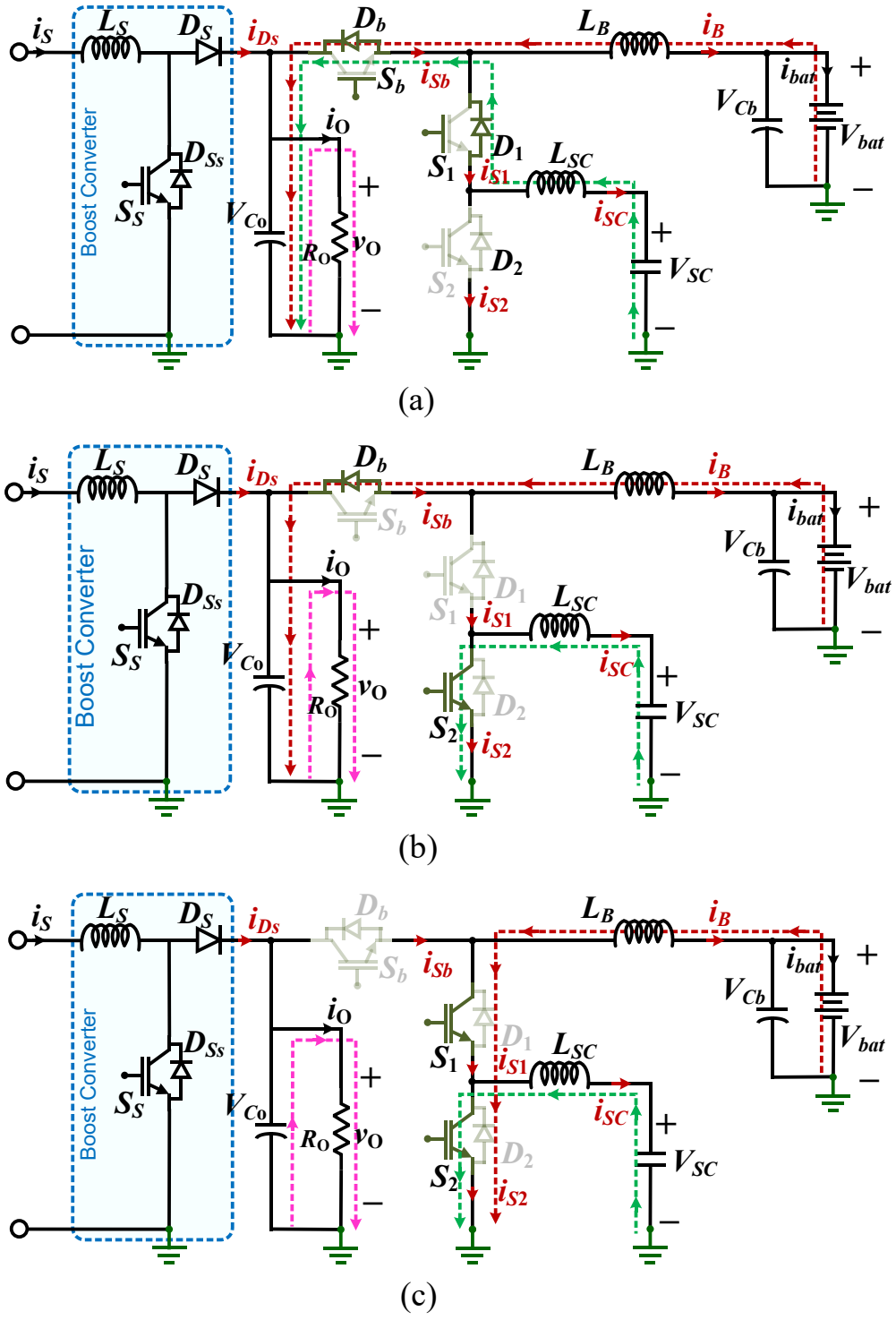


Fig. 6.5 Equivalent circuits illustrating the operating modes of the FPDCBSS in *state*-1: (a) M_1, (b) M_2, and (c) M_3.

6.5.1.1 *Steady-state analysis of FPDCBSS converter during state-I:*

The battery and SC operate in boost mode and steady-state voltage gain expression, which can be written as follows:

$$v_O = \frac{V_B}{1-D_1} = \frac{V_{SC}}{1-D_2} \tag{6.1}$$

The state-space averaged (SSA) model is obtained within one complete switching period (T) with the consideration that the system is linearized around the operating point. The state space equation can be written as follows [34], [104]:

$$\frac{dx(t)}{dt} = \dot{x} = \mathbf{A}_K x(t) + \mathbf{B}_K u(t) \tag{6.2(a)}$$

$$y(t) = \mathbf{C}_K x(t) + \mathbf{D}_K u(t) \tag{6.2(b)}$$

where $\mathbf{A}_K$, $\mathbf{B}_K$, $\mathbf{C}_K$, and $\mathbf{D}_K$ show the state, input, output, and direct transmission matrices for different states K (i.e., K = S1, S2, S3, S4) and the operating modes within the state, i.e., $M_i = M_1, M_2, \ldots, M_{12}$. In *state*-I, the state variable $x(t)$ is defined as $[i_B, i_{SC}, v_{Co}]^T$, i.e., the current through battery side inductors i_B, SC side inductors i_{SC} and voltage across DC bus capacitor v_{Co} are the state variables, and battery voltage v_B and SC voltage v_{SC} are the input variables, and the voltages across load v_o, battery current i_B, and SC current i_{SC} are the output variables. In steady state, (6.2 a) and (6.2 b) can be rewritten as follows:

$$\dot{\mathrm{X}} = \mathbf{A}_K \mathrm{X} + \mathbf{B}_K \mathrm{U} = 0 \Rightarrow \mathrm{X} = -\mathbf{A}_K^{-1}\mathbf{B}_K \mathrm{U} \tag{6.3(a)}$$

$$\mathrm{Y} = \mathbf{C}_K \mathrm{X} + \mathbf{D}_K \mathrm{U} \Rightarrow \mathrm{Y} = (-\mathbf{C}_K \mathbf{A}_K^{-1}\mathbf{B}_K + \mathbf{D}_K)\mathrm{U} \tag{6.3(b)}$$

The averaging of the state matrices $\mathbf{A}_{S1}$ and input matrices $\mathbf{B}_{S1}$ within the *state*-I of the FPDCBSS with respect to three switching modes can be derived and is given as follows:

$$A_{S1}=\begin{bmatrix} 0 & 0 & -(1-d_1)/L_B \\ 0 & 0 & -(1-d_2)/L_{SC} \\ (1-d_1)/C_O & (1-d_2)/C_O & -1/R_O C_O \end{bmatrix};$$

$$B_{S1}=\begin{bmatrix} 1/L_B & 0 \\ 0 & 1/L_{SC} \\ 0 & 0 \end{bmatrix};\ C_{S1}=\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix};\ D_{S1}=\begin{bmatrix} 0 \end{bmatrix}. \quad 6.4$$

6.5.1.2 ***Small-signal analysis of FPDCBSS converter during state-I:***

Using the state-space model obtained for *state*-I, the system dynamics are linearized around a nominal operating condition through small-signal perturbation analysis. In this approach, the state variables, input variables, and control variables are expressed as the combination of a steady-state component and a small-signal variation, as follows:

$$x = X + \hat{x};\quad u = U + \hat{u};\quad d = D + \hat{d} \quad 6.5$$

Where x, u, and d are the state variable, input, and duty ratio ($d \equiv d_1, d_2$); X, U, and D are the steady-state values of state variable, input, and duty ratio ($D \equiv D_1, D_2$); and $\hat{x}, \hat{u},$ and $\hat{d}$ are the perturbations around the steady-state values.

Substituting perturbed variables into averaged equations and neglecting higher-order terms gives the small-signal model expressed as follows for p^{th} state, where p = 1, 2, 3, 4:

$$\dot{\hat{x}}_{Sp} = A_{Sp}\hat{x} + B_{Sp}\hat{u} + E_{1Sp}\hat{d}_1 + E_{2Sp}\hat{d}_2 \quad 6.6$$

Further, for p^{th} state (6.6) can be written using Laplace transform as follows:

$$\hat{Y}(s) = C(SI - A_{Sp})^{-1}\left[B_{Sp}\hat{U}(s) + E_{1Sp}\hat{d}_1(s) + E_{2Sp}\hat{d}_2(s)\right] \quad 6.7$$

The transfer function (TF) is obtained by considering one perturbation input at a time while setting all other perturbations zero. Thus, the TF of battery current $\hat{i}_B$ with respect

to duty ratio $\hat{d}_1$ keeping all other perturbations $\hat{U}$ and $\hat{d}_2$ equal to zero, i.e., $G_{i_B d_1|Sp}\big|_{\hat{d}_2=\hat{U}=0}$, and similarly, the TF of SC current $G_{i_{SC} d_2|Sp}\big|_{\hat{d}_1=\hat{U}=0}$ and output voltage $G_{v_O d_2|Sp}\big|_{\hat{d}_1=\hat{U}=0}$ can be written as in (6.8), (6.9), and (6.10), respectively.

$$G_{i_B d_1|Sp} = G_{i_B d_1|Sp}\big|_{\hat{d}_2=\hat{U}=0} = \hat{i}_B(s)\big/\hat{d}_1(s) = C_{Sp}(SI - A_{Sp})^{-1}E_{1Sp} \tag{6.8}$$

$$G_{i_{SC} d_2|Sp} = G_{i_{SC} d_2|Sp}\big|_{\hat{d}_1=\hat{U}=0} = \hat{i}_{SC}(s)\big/\hat{d}_2(s) = C_{Sp}(SI - A_{Sp})^{-1}E_{2Sp} \tag{6.9}$$

$$G_{v_O d_2|Sp} = G_{v_O d_2|Sp}\big|_{\hat{d}_1=\hat{U}=0} = \hat{v}_O(s)\big/\hat{d}_2(s) = C_{Sp}(SI - A_{Sp})^{-1}E_{2Sp} \tag{6.10}$$

Further, for *state*-I, the values of E_{1S1} and E_{2S1} can be derived and written as follows:

$$E_{1S1} = \begin{bmatrix} \dfrac{v_O}{L_B} & 0 & \dfrac{-I_B}{C_O} \end{bmatrix}^T ; E_{2S1} = \begin{bmatrix} 0 & \dfrac{v_O}{L_{SC}} & \dfrac{-I_{SC}}{C_O} \end{bmatrix}^T \tag{6.11}$$

From (6.8), (6.9), (6.10), and (6.11), it can be further rewritten as in (6.12), (6.13), and (6.14), respectively. It can be seen from Fig. 6.3 that the duty (1-D_2) is responsible only for the response time ratio of SC; therefore, the value should be minimal with respect to battery response duty (1-D_1). Therefore, the term associated with (1-D_2) can be neglected, also $i_O = (1-D_1)i_B$, and (6.12) can be rewritten as (6.15). Similarly, (6.13) can be rewritten as (6.16); and (6.14) can be rewritten as (6.17) and further with respect to (6.16) it can be rewritten as (6.18).

$$G_{i_B d_1}\big|_{S1} = \frac{\left(\dfrac{v_O}{L_B}s^2 + \dfrac{v_O}{R_O L_B C_O}s + \dfrac{v_O(1-D_2)^2}{L_{SC}L_B C_O} + \dfrac{(1-D_1)}{L_B C_O}i_B s\right)}{\left(s^3 + \dfrac{1}{R_O C_O}s^2 + \left(\dfrac{(1-D_2)^2}{L_{SC}C_O} + \dfrac{(1-D_1)^2}{L_B C_O}\right)s\right)} \tag{6.12}$$

$$G_{i_{SC} d_2}\big|_{S1} = \frac{\left(\dfrac{v_O}{L_{SC}}s^2 + \dfrac{v_O}{R_O L_{SC} C_O}s + \dfrac{v_O(1-D_1)^2}{L_{SC}L_B C_O} + \dfrac{(1-D_2)}{L_{SC}C_O}i_{SC} s\right)}{\left(s^3 + \dfrac{1}{R_O C_O}s^2 + \left(\dfrac{(1-D_2)^2}{L_{SC}C_O} + \dfrac{(1-D_1)^2}{L_B C_O}\right)s\right)} \tag{6.13}$$

$$G_{v_O d_2}\big|_{S1} = \frac{\left(-\dfrac{i_{SC}}{C_O}s^2 + \dfrac{v_O(1-D_2)}{L_{SC}C_O}s\right)}{\left(s^3 + \dfrac{1}{R_O C_O}s^2 + \left(\dfrac{(1-D_2)^2}{L_{SC}C_O} + \dfrac{(1-D_1)^2}{L_B C_O}\right)s\right)} \tag{6.14}$$

$$G_{i_B d_1}\Big|_{S1} = \frac{\left(v_O C_O s + \frac{2v_O}{R_O}\right)}{\left(L_B C_O s^2 + \frac{L_B}{R_O} s + (1-D_1)^2\right)} \tag{6.15}$$

$$G_{i_{SC} d_2}\Big|_{S1} = \frac{\left(v_O C_O s + \frac{2v_O}{R_O}\right)}{\left(L_{SC} C_O s^2 + \frac{L_{SC}}{R_O} s + (1-D_2)^2\right)} \tag{6.16}$$

$$G_{v_O d_2}\Big|_{S1} = \frac{\left(-\frac{v_O L_{SC}}{R_O(1-D_2)} s + v_O(1-D_2)\right)}{\left(L_{SC} C_O s^2 + \frac{L_{SC}}{R_O} s + (1-D_2)^2\right)} \tag{6.17}$$

$$G_{v_O i_{SC}}\Big|_{S1} = \frac{\hat{v}_O(s)}{\hat{i}_{SC}(s)} = \frac{\left(R_O(1-D_2)\left(1 - \frac{L_{SC}}{R_O(1-D_2)^2} s\right)\right)}{\left(R_O C_O s + 2\right)} \tag{6.18}$$

6.5.2 State-II Operation ($P_{PV} > P_O$):

The transient condition under *state*-II of operation arises due to sudden decrease in the load demand. In this state both the battery and SC operate in buck mode of operation to receive power from the DC bus to maintain bus voltage. The switches S_1 and S_b act as the active energy transfer switches, and the diodes D_1 and D_2 operate in order to regulate current, as depicted in the switching and current characteristics diagram in Fig. 6.6 and Table 6.2. The detailed current path under all three modes (i.e., modes M_4, M_5, and M_6) is presented in Fig. 6.7 to relate the characteristics presented in Table 6.2, where T is the switching period.

TABLE 6.2

POSSIBLE MODES UNDER TRANSIENT CONDITIONS UNDER STATE-II

Mode	Duration	Current Characteristics	Active Switches
M_4	$(1-D_2) \times T$	$i_B \uparrow, i_{SC} \uparrow$	S_b, S_1
M_5	$\{(D_2 - D_1)/2\} \times T$	$i_B \uparrow, i_{SC} \downarrow$	S_b, D_2
M_6	$D_1 \times T$	$i_B \downarrow, i_{SC} \downarrow$	D_1, D_2

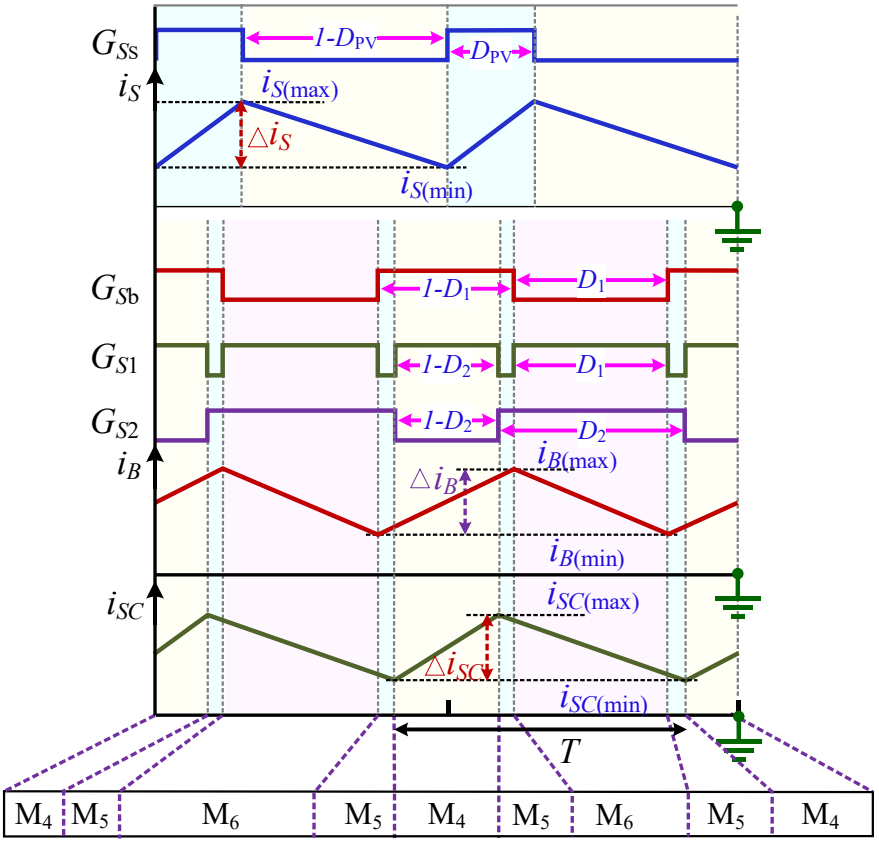
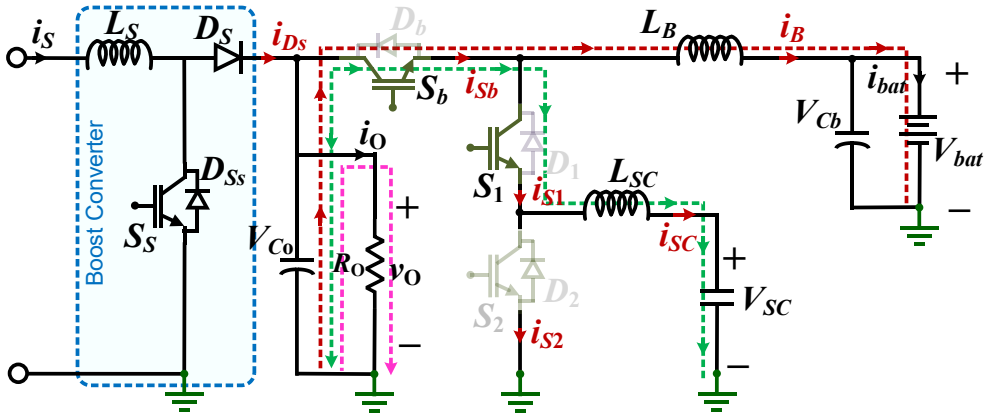


Fig. 6.6 Switching pattern and current characteristics of the FPDCBSS under *State*-II operation.



(a)

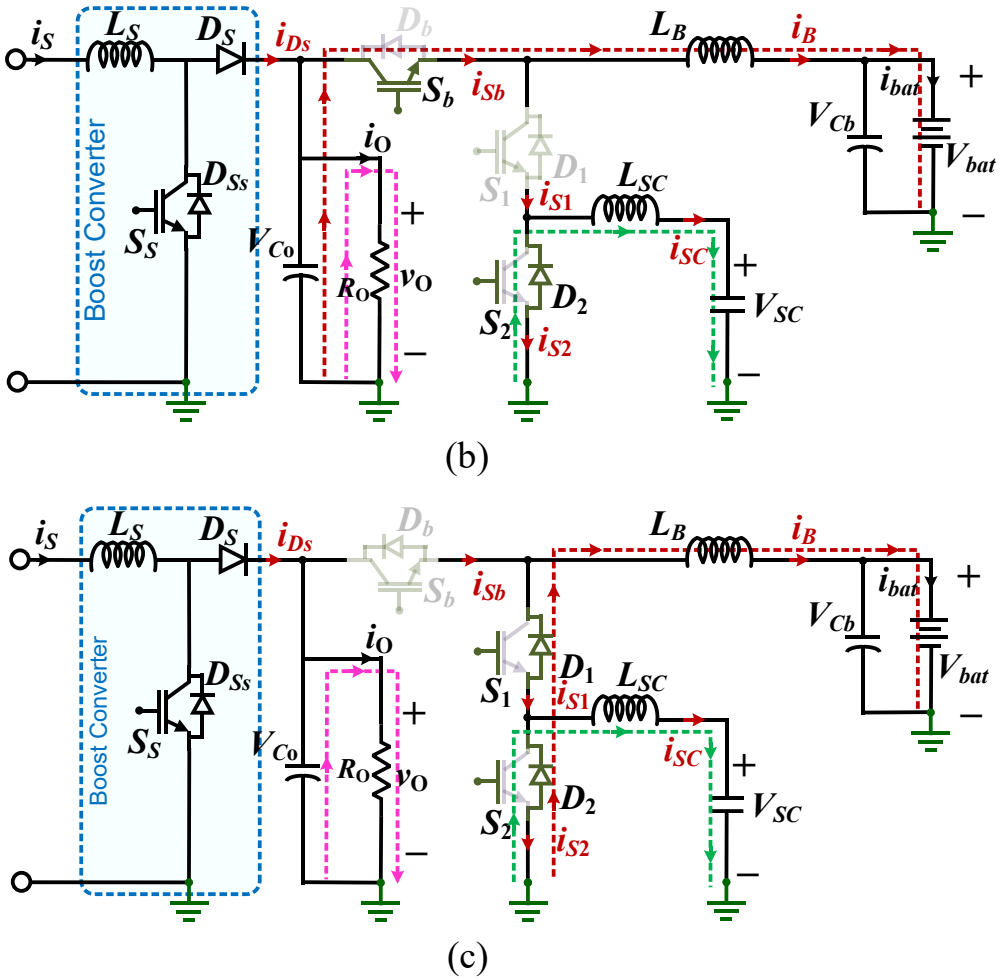


Fig. 6.7 Equivalent circuits illustrating the operating modes of the FPDCBSS in *state*-II: (a) M_4, (b) M_5, and (c) M_6.

6.5.2.1 *Steady-state analysis of FPDCBSS converter during state-II:*

In *state*-II, the state variable is defined as $[i_B, i_{SC}, v_{Co}, v_{SC}]^T$, where, v_{Cb} and v_{SC} are the voltages across battery side capacitor and SC, respectively. The battery and SC operate in buck mode (i.e., charging) and steady-state voltage gain expression can be written as follows:

$$V_{bat} = v_O\left(1-D_1\right), \quad V_{SC} = v_O\left(1-D_2\right) \tag{6.19}$$

The averaging of the state matrices $\mathbf{A}_{S2}$ and input matrices $\mathbf{B}_{S2}$ within the *state*-II of the FPDCBSS with respect to three switching modes (i.e., M_4, M_5, and M_6) can be derived and is given as follows*:*

$$A_{S2}=\begin{bmatrix} 0 & 0 & -1/L_B & 0 \\ 0 & 0 & 0 & -1/L_{SC} \\ 1/C_b & 0 & -1/R_BC_b & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC}C_C \end{bmatrix}; \quad 6.20$$

$$B_{S2}=\begin{bmatrix} (1-d_1)/L_B & (1-d_2)/L_{SC} & 0 & 0 \end{bmatrix}^T;\ C_{S2}=\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ D_{S2}=\begin{bmatrix} 0 \end{bmatrix}$$

6.5.2.2 *Small-signal analysis of FPDCBSS converter during state-II:*

Using the state-space model obtained for *state*-II, the system dynamics are linearized around a nominal operating condition through small-signal perturbation analysis as done for *state*-II. Further, for *state*-II, the values of E_{1S2} and E_{2S2} can be derived and written as follows:

$$E_{1S2}=\begin{bmatrix} \frac{-v_O}{L_B} & 0 & 0 & 0 \end{bmatrix}^T; E_{2S2}=\begin{bmatrix} 0 & \frac{-v_O}{L_{SC}} & 0 & 0 \end{bmatrix}^T \quad 6.21$$

Similar to *state*-I, the TFs for *state*-II can be derived and presented as follows:

$$G_{i_Bd_1}\big|_{S2}=\left(sv_OC_b+Vc_O/R_B\right)\Big/\left(s^2L_BC_b+sL_B/R_B+1\right) \quad 6.22$$

$$G_{i_{SC}d_2}\big|_{S2}=\left(sV_{SC}C_C+v_O/R_{SC}\right)\Big/\left(s^2L_{SC}C_C+sL_{SC}/R_{SC}+1\right) \quad 6.23$$

$$G_{v_{bat}d_1}\big|_{S2}=v_O\Big/\left(s^2L_BC_b+sL_B/R_B+1\right) \quad 6.24$$

$$G_{v_{SC}d_2}\big|_{S2}=v_O\Big/\left(s^2L_{SC}C_C+sL_{SC}/R_{SC}+1\right) \quad 6.25$$

6.5.3 *State*-III *Operation:*

The transient condition under *state*-III of operation arises due to charging of the SC and discharging of the battery to balance with the reference voltages. In this state the battery operates in boost mode and SC operates in buck mode of operation. The switches

S_b, S_1, and S_2 act as the active energy transfer switches, and the diodes D_b and D_2 operate to regulate current, as depicted in the switching and current characteristics diagram in Fig. 6.8 and Table 6.3. In *state*-III, three modes, M_7, M_8, and M_9, occur. The detailed current path under all three modes (i.e., modes M_7, M_8, and M_9) is presented in Fig. 6.9 to relate the characteristics presented in Table 6.3, where T is the switching period.

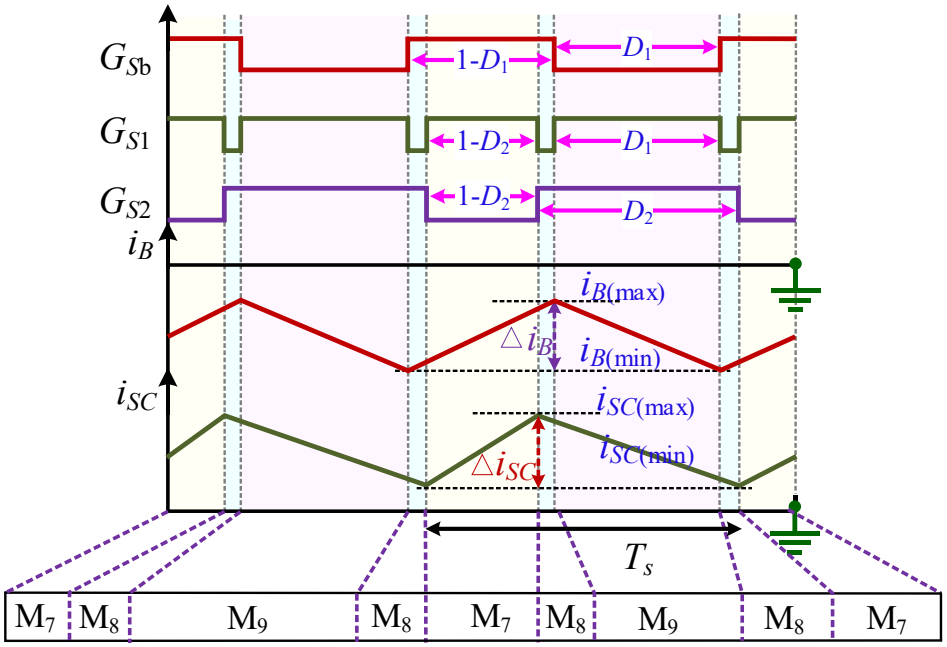


Fig. 6.8 Switching pattern and current characteristics of the FPDCBSS under *State*-III operation.

TABLE 6.3

POSSIBLE MODES UNDER TRANSIENT CONDITIONS UNDER STATE-III

Modes	Duration	Current Characteristics	Active Switches
M_7	$(1-D_2)\times T$	$i_B \downarrow, i_{SC} \uparrow$	S_b, S_1, D_b
M_8	$\{(D_2-D_1)/2\}\times T$	$i_B \downarrow, i_{SC} \downarrow$	D_b, D_2
M_9	$D_1\times T$	$i_B \uparrow, i_{SC} \downarrow$	S_1, S_2, D_2

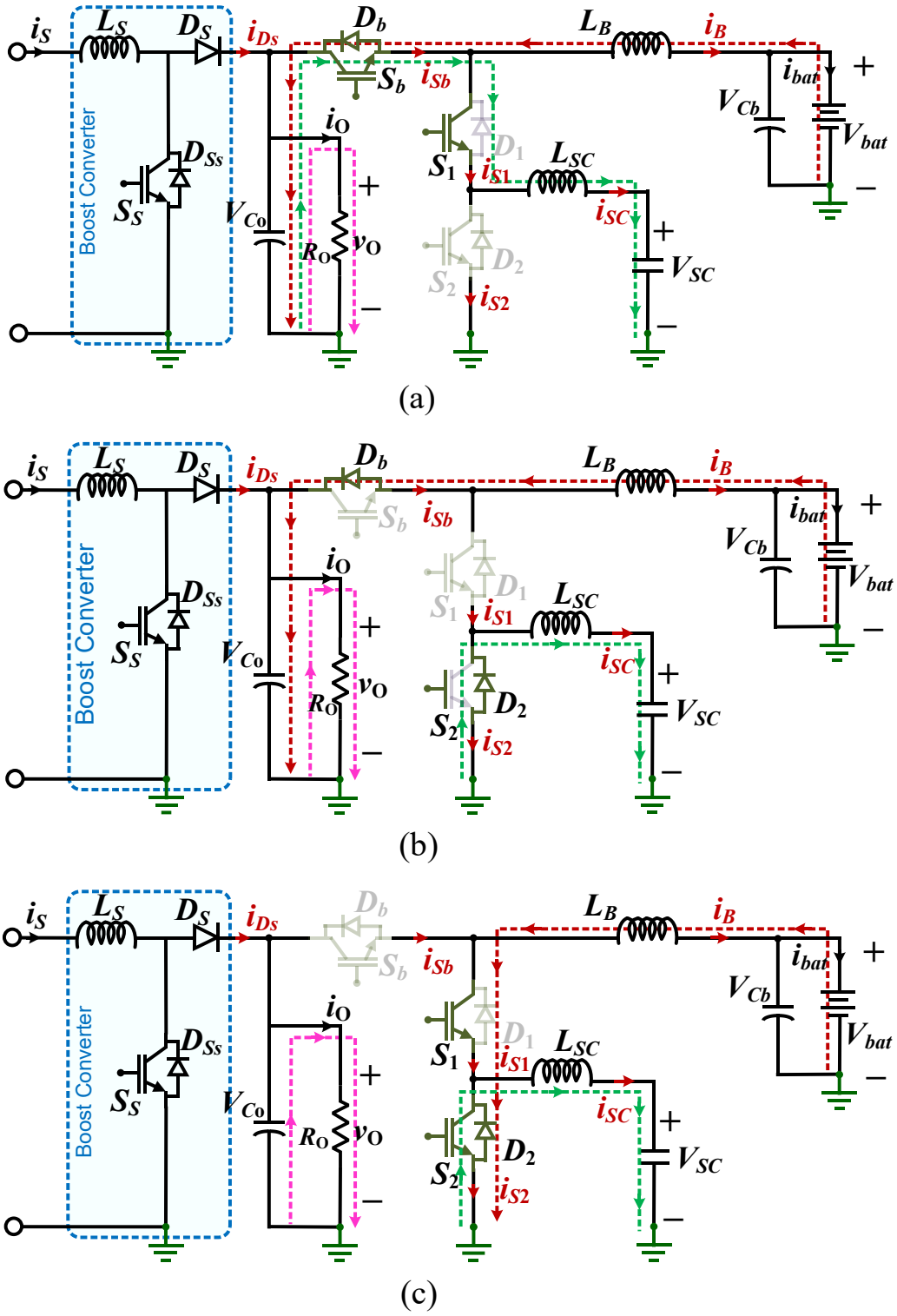


Fig. 6.9 Equivalent circuits illustrating the operating modes of the FPDCBSS in *state*-III: (a) M_7, (b) M_8, and (c) M_9.

6.5.3.1 *Small-signal analysis of FPDCBSS converter during state*-III*:*

In *state*-III, the state variable is defined as $[i_B, i_{SC}, v_{Co}, v_{SC}]^T$ and input is V_{bat}. The averaging of the state matrices $\mathbf{A}_{S3}$ and input matrices $\mathbf{B}_{S3}$ within the *state*-III of the FPDCBSS with respect to three switching modes (i.e., M_7, M_8, and M_9) can be derived and is given as follows:

$$A_{S3}=\begin{bmatrix} 0 & 0 & \dfrac{-(1-d_1)}{L_B} & 0 \\ 0 & 0 & \dfrac{(1-d_2)}{L_{SC}} & \dfrac{-1}{L_{SC}} \\ \dfrac{(1-d_1)}{C_O} & -\dfrac{(1-d_2)}{C_O} & \dfrac{-1}{R_O C_O} & 0 \\ 0 & \dfrac{1}{C_C} & 0 & \dfrac{-1}{R_{SC}C_C} \end{bmatrix}; \quad 6.26$$

$$B_{S3}=\begin{bmatrix} 1/L_B & 0 & 0 & 0 \end{bmatrix}^T;$$

$$E_{1S3}=\begin{bmatrix} \dfrac{v_O}{L_B} & 0 & \dfrac{-I_B}{C_O} & 0 \end{bmatrix}^T; E_{2S3}=\begin{bmatrix} 0 & \dfrac{-v_O}{L_{SC}} & \dfrac{I_{SC}}{C_O} & 0 \end{bmatrix}^T$$

Similar to *state*-I, the TFs for *state*-III can be derived and presented in (6.27), (6.28), and (6.29).

6.5.4 *State*-IV *Operation:*

The transient condition under *state*-IV of operation arises due to discharging of the SC and charging of the battery to balance with the reference voltages. In this state the battery operates in buck mode and SC operates in boost mode of operation. The switches S_b, and S_2 act as the active energy transfer switches, and the diodes D_b, D_1, and D_2 operate to regulate current, as depicted in the switching and current characteristics diagram in Fig. 6.10 and Table 6.4. In *state*-IV, three modes, M_{10}, M_{11}, and M_{12}, occur. The detailed current path under all three modes (i.e., modes M_{10}, M_{11}, and M_{12}) is presented in Fig. 6.11 to relate the characteristics presented in Table 6.4, where T is the switching period.

$$G_{i_B d_1}\Big|_{S3} = \frac{\left(s^3 C_O C_C R_{SC} + s^2\left(C_O + \frac{2C_C R_{SC}}{R_O}\right) + s\left(\frac{2}{R_O} + \frac{C_O R_{SC}}{L_{SC}}\right) + \frac{2R_{SC}}{L_{SC} R_O}\right) v_O}{s^4 C_O C_C R_{SC} L_B + s^3\left(C_O L_B + \frac{C_C R_{SC} L_B}{R_O}\right) + s^2\left(C_C R_{SC}(1-D_1)^2 + \frac{L_B}{R_O} + \frac{C_O R_{SC} L_B}{L_{SC}}\right) + s\left((1-D_1)^2 + \frac{R_{SC} L_B}{R_O L_{SC}}\right) + \frac{R_{SC}(1-D_1)^2}{L_{SC}}} \quad (6.27)$$

$$G_{i_{SC} d_2}\Big|_{S3} = \frac{-s^3 C_O C_C R_{SC} v_O + s^2\left(\frac{C_C {V_{SC}}^2}{v_O} - \frac{C_C R_{SC} v_O}{R_O} - C_O v_O\right) + s\left(-\frac{v_O}{R_O} + \frac{{V_{SC}}^2}{R_{SC} v_O}\right)}{s^4 C_O C_C R_{SC} L_{SC} + s^3\left(C_O L_{SC} + \frac{C_C R_{SC} L_{SC}}{R_O}\right) + s^2\left(C_C R_{SC}(1-D_2)^2 + \frac{L_{SC}}{R_O} + C_O R_{SC}\right) + s\left((1-D_2)^2 + \frac{R_{SC}}{R_O}\right)} \quad (6.28)$$

$$G_{v_O i_{SC}}\Big|_{S3} = \frac{\left(s^3 C_C L_{SC} + s^2\left(\frac{L_{SC}}{R_{SC}} + C_C R_{SC}\right) + 2s\right) V_{SC}}{\left(-s^3 C_O C_C R_{SC} v_O + s^2\left(\frac{C_C {V_{SC}}^2}{v_O} - \frac{C_C R_{SC} v_O}{R_O} - C_O v_O\right) + s\left(-\frac{v_O}{R_O} + \frac{{V_{SC}}^2}{R_{SC} v_O}\right)\right)} \quad (6.29)$$

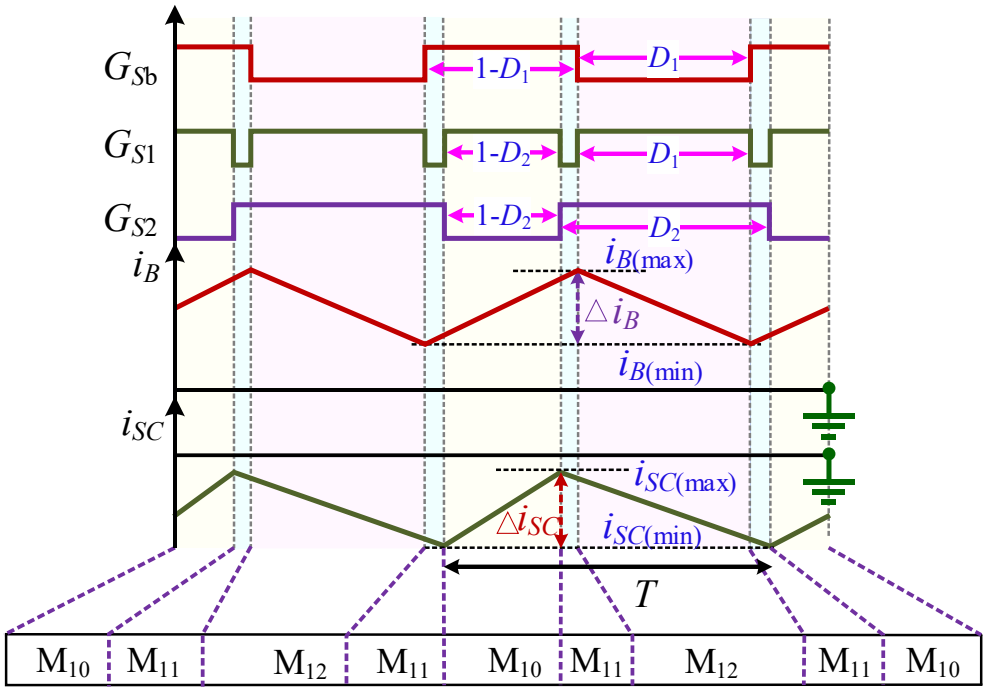


Fig. 6.10 Switching pattern and current characteristics of the FPDCBSS under *State*-IV operation.

TABLE 6.4

POSSIBLE MODES UNDER TRANSIENT CONDITIONS UNDER STATE-IV

Modes	**Duration**	**Current Characteristics**	**Active Switches**
M_{10}	$(1\text{-}D_2)\times T$	$i_B \uparrow, i_{SC} \downarrow$	S_b, D_b, D_1
M_{11}	$\{(D_2–D_1)/2\}\times T$	$i_B \uparrow, i_{SC} \downarrow$	S_b, S_2
M_{12}	$D_1\times T$	$i_B \downarrow, i_{SC} \uparrow$	S_2, D_1, D_2

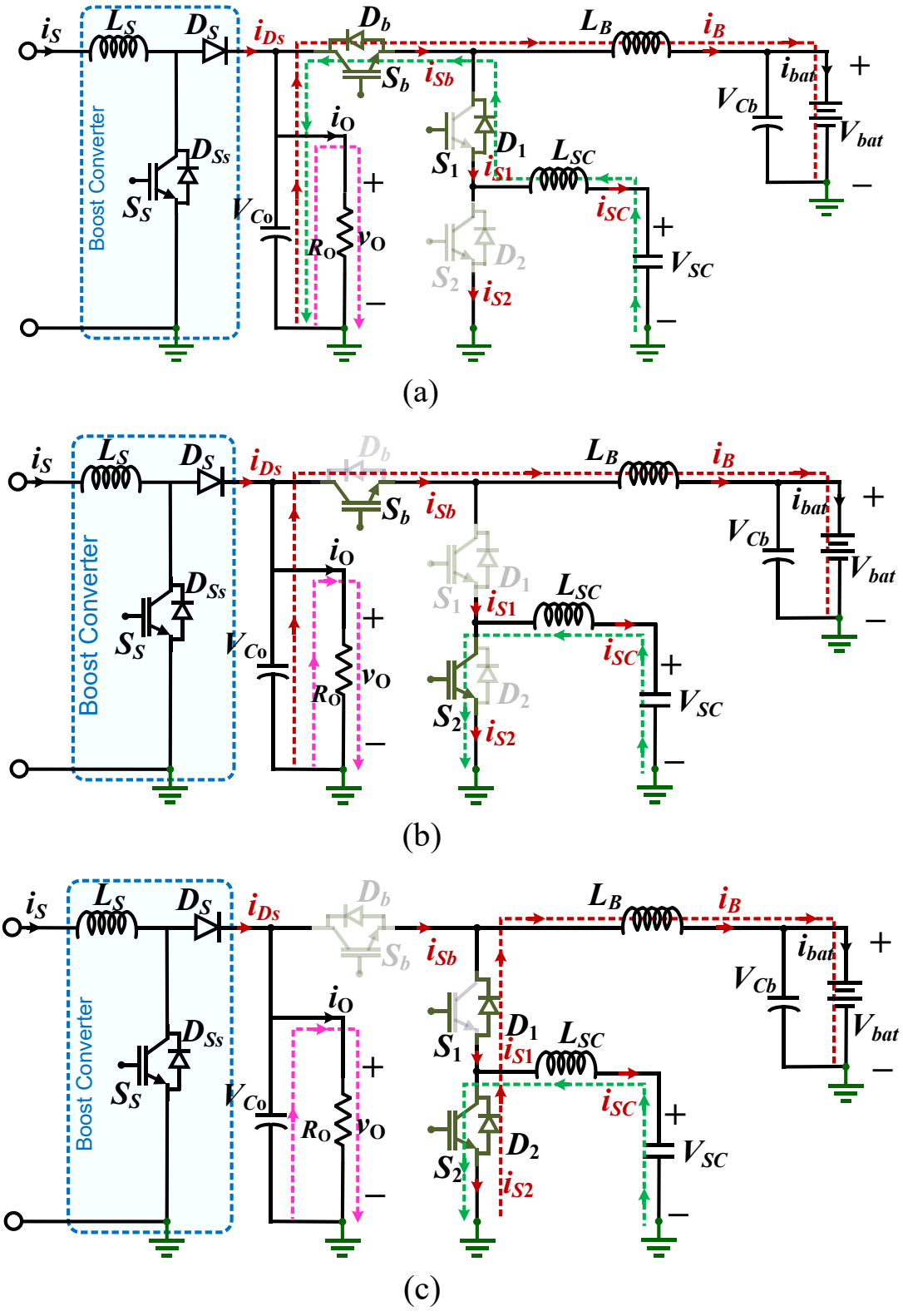


Fig. 6.11 Equivalent circuits illustrating the operating modes of the FPDCBSS in *state*-IV: (a) M_{10}, (b) M_{11}, and (c) M_{12}.

6.5.4.1 *Small-signal analysis of FPDCHESS converter during state-*IV *operation:*

In *state*-IV, the state variable is defined as $[i_B, i_{SC}, v_{Co}, v_B]^T$ and input is V_{SC}. The averaging of the state matrices $\mathbf{A}_{S4}$ and input matrices $\mathbf{B}_{S4}$ within the *state*-IV of the FPDCBSS with respect to three switching modes (i.e., M_{10}, M_{11}, and M_{12}) can be derived and is given as follows:

$$A_{S4}=\begin{bmatrix} 0 & 0 & \dfrac{(1-d_1)}{L_B} & -\dfrac{1}{L_B} \\ 0 & 0 & -\dfrac{(1-d_2)}{L_{SC}} & 0 \\ -\dfrac{(1-d_1)}{C_O} & \dfrac{(1-d_2)}{C_O} & -\dfrac{1}{R_O C_O} & 0 \\ \dfrac{1}{C_b} & 0 & 0 & -\dfrac{1}{R_B C_b} \end{bmatrix}; \qquad 6.30$$

$$B_{S4}=\begin{bmatrix} 0 & 1/L_{SC} & 0 & 0 \end{bmatrix}^T;$$

$$E_{1S4}=\begin{bmatrix} \dfrac{-v_O}{L_B} & 0 & \dfrac{I_B}{C_O} & 0 \end{bmatrix}^T; E_{2S4}=\begin{bmatrix} 0 & \dfrac{v_O}{L_{SC}} & \dfrac{-I_{SC}}{C_O} & 0 \end{bmatrix}^T$$

Similar to *state*-I, the TFs for *state*-IV can be derived as presented in (6.31), (6.32), and (6.33).

6.5.5 *State-*V *and State-*VI *Operation:*

In both operating states, the average power transfer through SC is zero, where the battery is discharging during *state*-V and charging during *state*-VI. In *state*-V, the modes of operation include M_1, M_2, M_3, M_7, M_8, and M_9, which have already been covered in *state*-I and *state*-III; while in *state*-VI, the modes of operation are M_4, M_5, M_6, M_{10}, M_{11}, and M_{12}, which have already been covered in *state*-II and state-IV, as shown in Figs. 6.12 and 6.13, respectively.

$$G_{i_{SC}d_2}\Big|_{S4} = \frac{\left(s^3 C_O C_b R_B + s^2\left(C_O + \frac{2C_b R_B}{R_O}\right) + s\left(\frac{2}{R_O} + \frac{C_O R_B}{L_B}\right) + \frac{2R_B}{L_B R_O}\right) v_O}{s^4 C_O C_b R_B L_{SC} + s^3\left(C_O L_{SC} + \frac{C_b R_B L_{SC}}{R_O}\right) + s^2\left(C_b R_B (1-D_2)^2 + \frac{L_{SC}}{R_O} + \frac{C_O R_B L_{SC}}{L_B}\right) + s\left((1-D_2)^2 + \frac{R_B L_{SC}}{R_O L_B}\right) + \frac{R_B (1-D_2)^2}{L_B}} \quad (6.31)$$

$$G_{i_b d_1}\Big|_{S4} = \frac{-s^3 C_O C_b R_B v_O + s^2\left(\frac{C_b {V_{bat}}^2}{v_O} - \frac{C_b R_B v_O}{R_O} - C_O v_O\right) + s\left(-\frac{v_O}{R_O} + \frac{{V_{bat}}^2}{R_B v_O}\right)}{s^4 C_O C_b R_B L_B + s^3\left(C_O L_B + \frac{C_b R_B L_B}{R_O}\right) + s^2\left(C_b R_B (1-D_1)^2 + \frac{L_B}{R_O} + C_O R_B\right) + s\left((1-D_1)^2 + \frac{R_B}{R_O}\right)} \quad (6.32)$$

$$G_{v_O i_{SC}}\Big|_{S4} = \frac{-s^3 C_b L_B L_{SC} R_B \frac{{v_O}^2}{V_{SC}} + s^2\left(C_B L_B R_B R_O V_{SC} - L_B L_{SC} \frac{{v_O}^2}{V_{SC}}\right) + s\left(L_B R_O V_{SC} - L_{SC} R_B \frac{{v_O}^2}{V_{SC}}\right) + R_B R_O V_{SC}}{\left(s^3 C_O C_b R_B + s^2\left(C_O + \frac{2C_b R_B}{R_O}\right) + s\left(\frac{2}{R_O} + \frac{C_O R_B}{L_B}\right) + \frac{2R_B}{L_B R_O}\right) v_O} \quad (6.33)$$

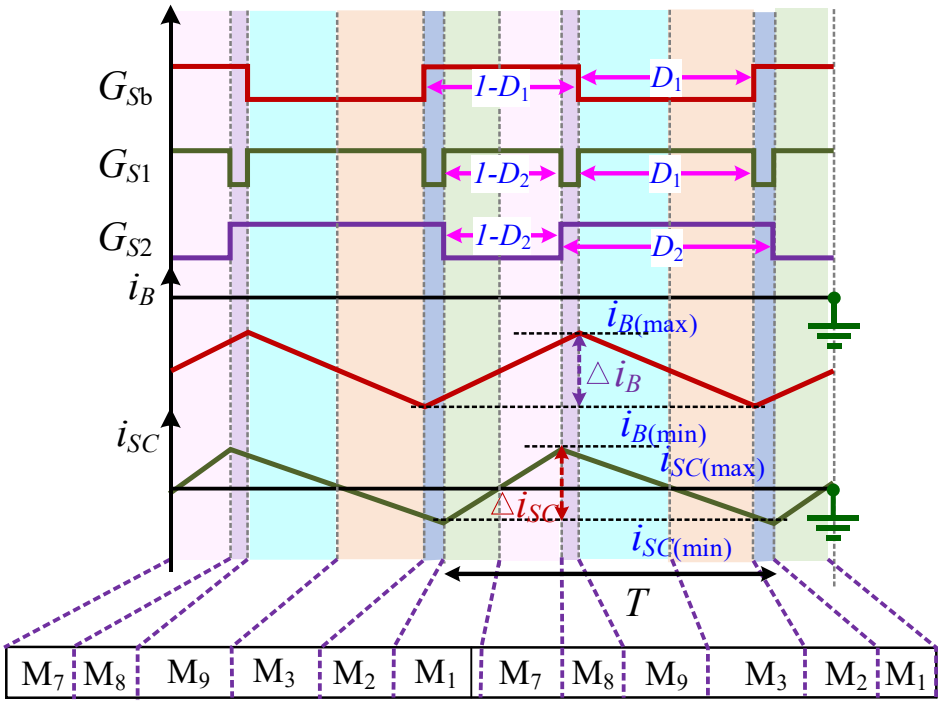


Fig. 6.12 Switching pattern and current characteristics of the FPDCBSS under *State*-V operation.

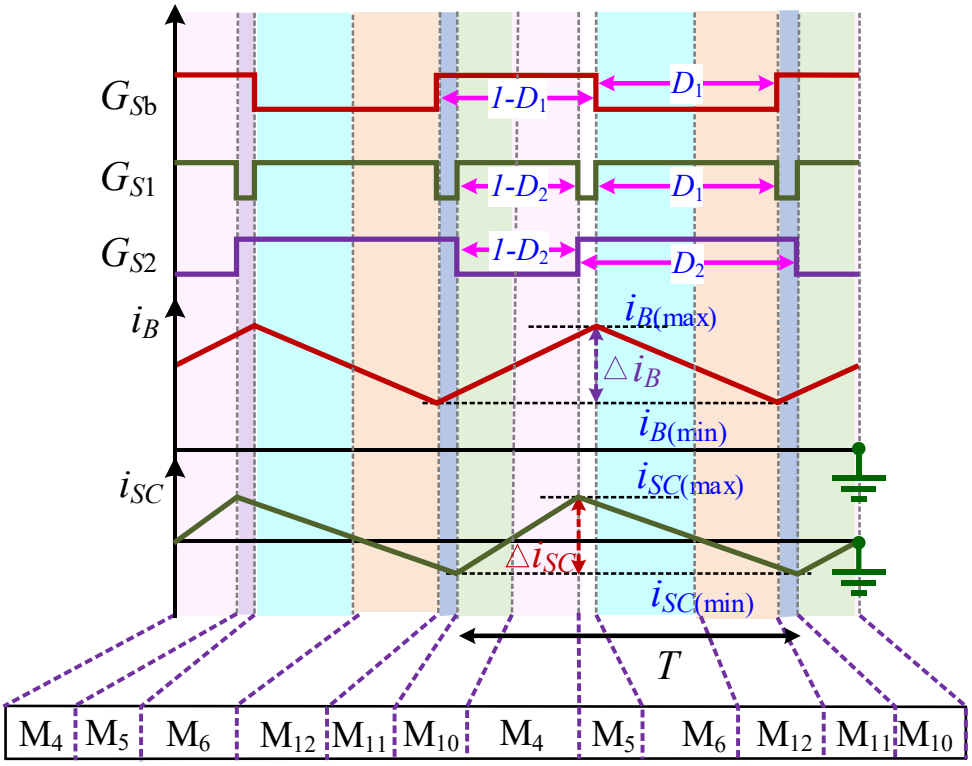


Fig. 6.13 Switching pattern and current characteristics of the FPDCBSS under *State*-VI operation.

6.6 Simulation Results and Discussion

The FPDCBSS converter and its coordinated control strategy discussed in the previous sections are evaluated for effectiveness under two representative operating conditions, i.e., changes in solar irradiation and variation in load, using the parameters given in Table 6.5, with the load voltage fixed at 105 V, as shown in Figs. 6.14 and 6.15, respectively.

TABLE 6.5

DESIGN PARAMETERS OF FPDCBSS

Parameters	**Values**
Output port voltages: v_O, V_{bat}, and V_{SC}	105 V, 48 V, and 36 V
Inductors: L_S, L_B, and L_{SC}	560 µH, 560 µH, and 300 µH
Capacitors: C_O, C_b, and C_C	470 µF, 100 µF, and 3.1 F
Power $P_{o\max}$ / load resistance R_O	600 W / 16Ω-384Ω
Switching frequency f_S	20 kHz

Figs. 6.14 and 6.15 show the steady-state and dynamic performance of the FPDCBSS under six operating states with a step change in solar irradiance at a fixed load and a step change in load at a fixed irradiance, respectively. The six states contain four transient states (i.e., States I, II, III, and IV) and two steady states (i.e., States V and VI). Refer to *state*-IV where due to sudden decrease in solar irradiation SC starts to operate in boost mode with certain current to feed the DC bus whereas the battery continues to charge from the bus by operating in buck mode. *State*-VI shows steady-state operation where only battery is charging and SC remains dormant. *State*-I shows both battery and SC operates in boost mode to feed the load. *State*-V shows steady state operation where only battery is discharging and SC remains dormant. *State*-III is the transient state when battery is still discharging whereas SC is charging and then shifts to *state*-I. The deficit power required by the load is instantaneously supplied by the SC for transient compensation, while the battery transitions into reduction in battery charging current, i_B or reversing from charging

to discharge(-i_B) mode to supply sustained average power. The bus voltage remains regulated at its reference value, demonstrating that the voltage regulation loop and BSCES control scheme operate in coordinated fashion. The SC current returns toward zero in steady-state conditions, confirming that it primarily handles dynamic components rather than steady-state energy transfer.

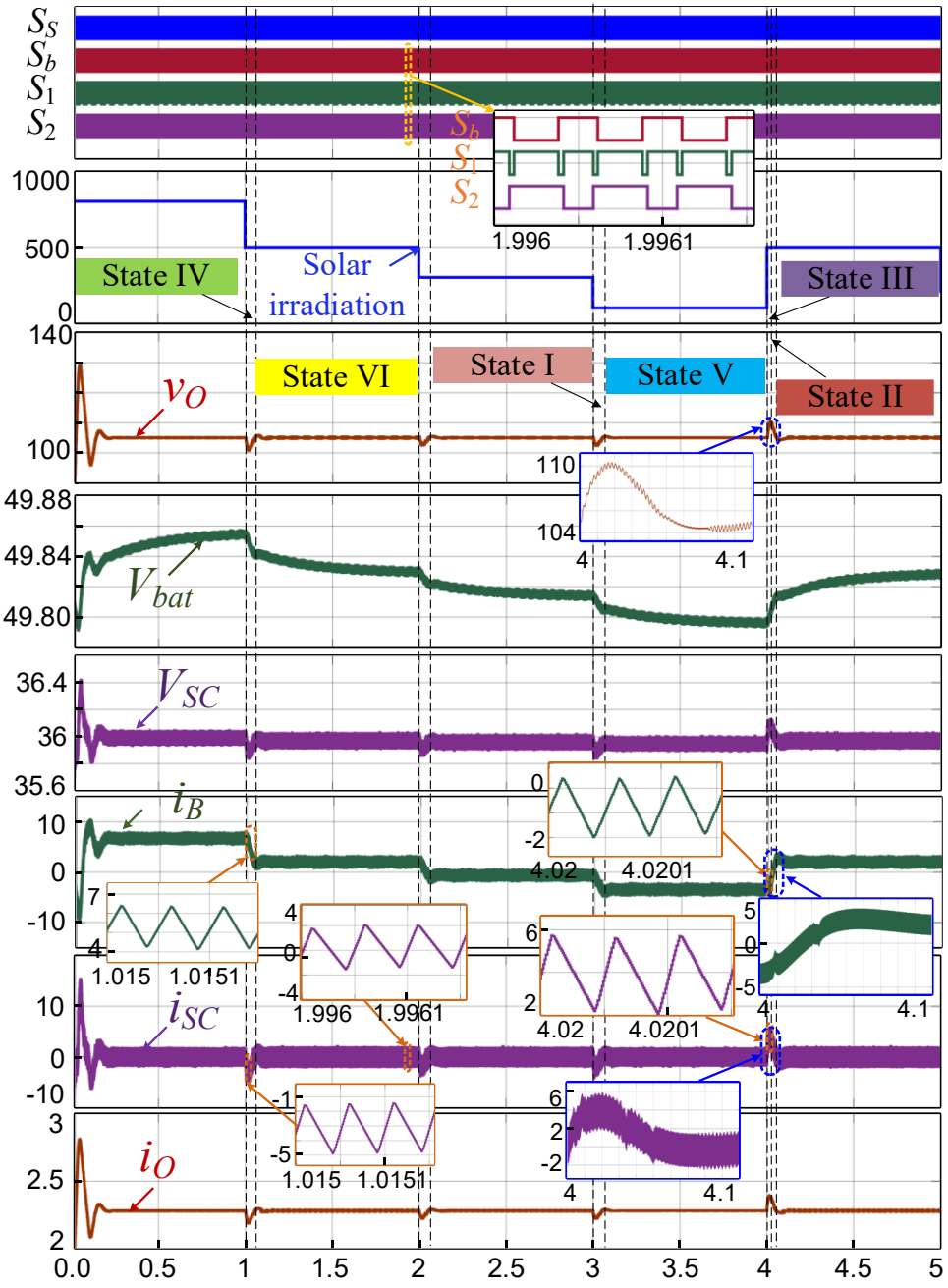


Fig. 6.14 Steady-state and dynamic performance of the FPDCBSS under six operating states with a step change in solar irradiance at a fixed load.

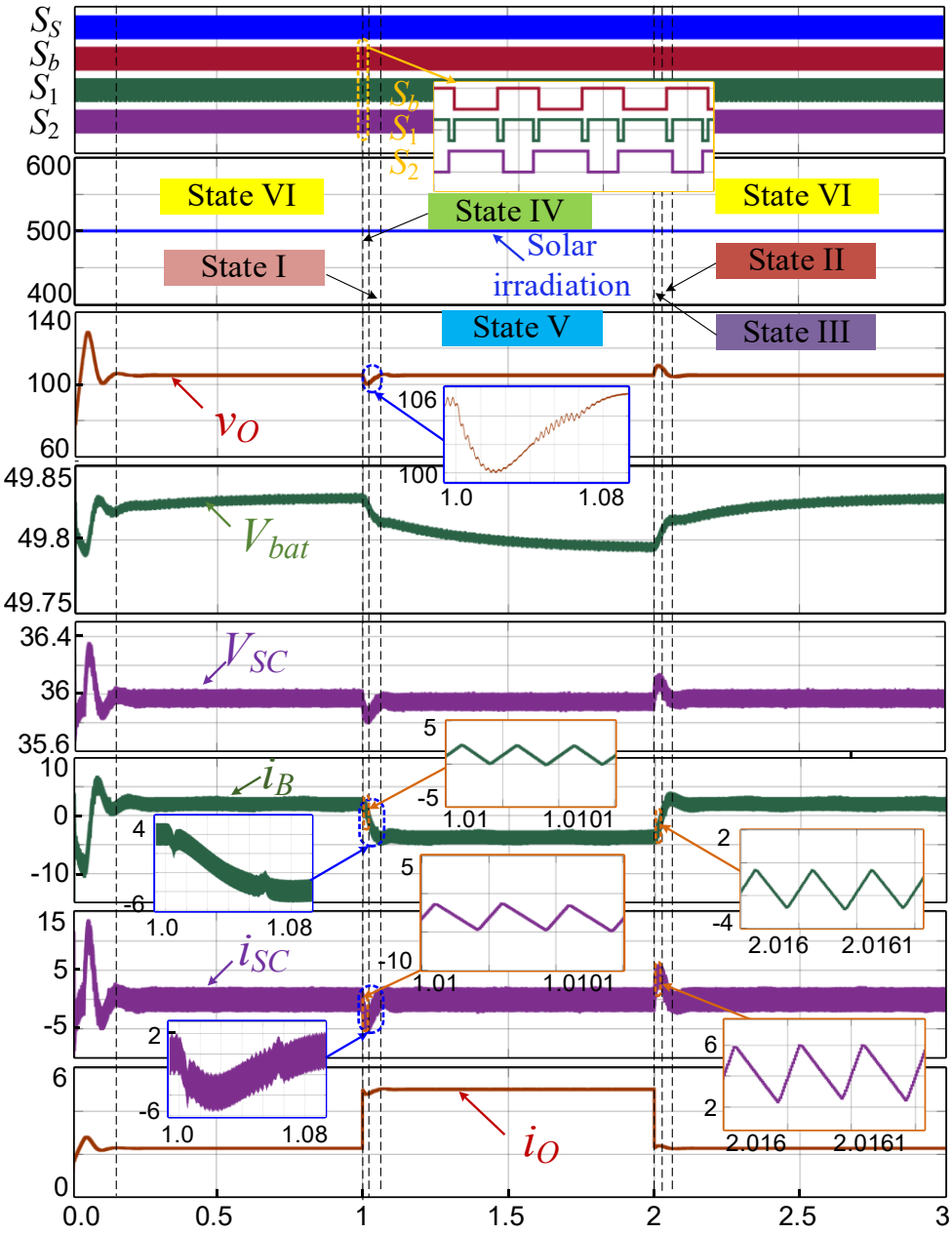


Fig. 6.15 Steady-state and dynamic performance of the FPDCBSS under six operating states with a step change in load at fixed solar irradiance.

6.7 Conclusion

Several significant dynamic features of the suggested converter are revealed by the calculated transfer functions. Through the same DC bus, the battery and supercapacitor loops are dynamically connected. Therefore, unless suitable decoupling techniques are used, a disturbance in one storage device affects the dynamic response of the other. The

dynamics of the computed transfer functions show that the interplay between the storage inductors and the DC-link capacitor largely controls the converter's behavior. The converter's inherent frequency, damping ratio, and transient response are all determined by the pole placements. The possible controller bandwidth and stability margins are directly impacted by these features. Additionally, during controller design, the zeros that appear in the numerator polynomials have an impact on the converter's phase response and, consequently, the achievable PM.

The derived transfer functions are used for stability analysis performed in the next chapter and controller design based on the design parameters.

Chapter 7

Controller Design for Battery-Supercapacitor based Storage System

7.1 Introduction

The need for sophisticated energy storage technologies that can provide high power density, quick transient response, and extended operating lifetime has grown dramatically due to the growing use of renewable energy sources and the quick electrification of transportation networks [2]. Lithium-ion batteries are frequently used as the main energy storage source in EVs, DC microgrids and other applications due to their high energy density among the current energy storage technologies [5]-[7]. However, batteries are prone to accelerated aging under frequent high-current charging and discharging circumstances, have a limited power density, and have relatively slow electrochemical kinetics [15], [22]-[23]. Supercapacitors, on the other hand, exhibit remarkable power density, quick charge-discharge capability, and superior cycling durability. However, their capacity to independently meet the long-duration energy requirements of electric propulsion systems is limited by their comparatively low energy density. As a result, neither technology alone can meet the dynamic power needs found in real-world EV applications [74]-[75].

By combining the complementing qualities of both storage devices, BSCES have become an efficient way to get around these restrictions. In a HESS, the supercapacitor makes up for short-term power fluctuations brought on by quick acceleration, regenerative braking, and abrupt load changes, while the battery is mostly in charge of meeting the average energy demand over long periods of time [22]. The reliability of EV powertrains and DC microgrid etc. is increased, battery longevity is increased, thermal stress is decreased, and overall system efficiency is greatly improved by such coordinated operation.

7.1.1 Need for Robust Control in BSCES

While there are significant performance benefits to combining battery and supercapacitor technology, there are also significant control issues. It is challenging to independently regulate battery and supercapacitor current due to the significant coupling across converter states caused by the dynamic interactions between the storage devices via the shared DC bus [79]. The controller design process is further complicated by changes in the generation of renewable energy, load disturbances, converter parameter uncertainties, and nonlinear operating conditions [104]. Because the control actions of one storage element affect the dynamics of the other, conventional proportional-integral (PI) controllers, when built independently for each storage device, frequently fail to offer sufficient performance [105]. Degraded stability margins, poor transient response, and unwanted current oscillations may result from this.

This study uses a decoupled robust control technique for the BSCES in order to address these problems. The suggested controller divides the frequency content of the load demand so that the supercapacitor makes up for high-frequency transient power and the battery only manages the low-frequency energy component. Each energy source can have an independent controller design thanks to this frequency-domain power distribution, which also reduces interference between storage devices. In order to guarantee appropriate closed-loop performance in the face of parameter changes, modeling uncertainties, and external disruptions, robust control methods are also integrated.

7.1.2 Controller Objectives

The small-signal mathematical model of the suggested hybrid energy storage converter created in the preceding chapter serves as the foundation for the controller development discussed in this chapter. Controller synthesis uses linearized transfer functions that relate the battery current and supercapacitor current to their corresponding duty-cycle control signals [106]. The foundation for choosing controller parameters that meet stability and dynamic performance criteria is frequency-domain analysis, which includes Bode plots, gain crossover frequency, PM, and bandwidth allocation [107].

The suggested approach introduces explicit bandwidth segregation between the battery and supercapacitor control loops, in contrast to traditional coupled controller topologies documented in the literature. In order to reject high-frequency disruptions and prevent

abrupt changes in current that hasten battery deterioration, the battery control loop is purposefully built with a comparatively small bandwidth. On the other hand, to guarantee quick correction of transient power needs, the supercapacitor controller is given a much larger bandwidth. The hybrid storage dynamics may be effectively decoupled thanks to this hierarchical allocation, which also maintains closed-loop robustness across a broad operating range [39], [107].

7.2 Robust Decoupled Controller Architecture for Battery-Supercapacitor based HESS

In the BSCES, the battery is utilized to mitigate the low-frequency transients and average power requirement, whereas the SC provides the capability to overcome the high-frequency transient conditions because of its high-power density and fast charge-discharge characteristics. To achieve effective power sharing, the SC current control loop is designed with a higher bandwidth than the battery current control loop, enabling it to respond quickly to sudden power variations while allowing the battery to meet the slower-varying load demand. In addition, the output voltage control loop is designed with a bandwidth approximately one-tenth that of the inner current control loops, ensuring proper cascaded operation, minimizing interaction between the control loops, and maintaining stable system performance.

The control strategy presented in [15] is extended for the FPDCBSS system as shown in Fig. 7.1. The current demand is separated into low-frequency and high-frequency components in Fig. 7.1 (a), which are assigned to the battery and the SC, respectively, for coordinated power management. The control scheme employs a low-pass filter (f_{LPF}) to generate i_{LF_ref} for the battery and the complementary i_{HF_ref} (i_{SC_ref}) for the SC, while the battery and SC current errors (i_{B_err} and i_{SC_err}) are processed by PI controllers, which are subsequently combined with logic-gate circuitry to derive the appropriate gating signals G_{Sb}, G_{S1}, and G_{S2} for FPDCBSS. The controller parameters are designed for the control strategy presented in Figs. 7.1 (b) and (c) to guarantee smooth operation without altering the controller structure during mode shifts, even though the FPDCBSS operates under six distinct operating states that correspond to different power transfer modes.

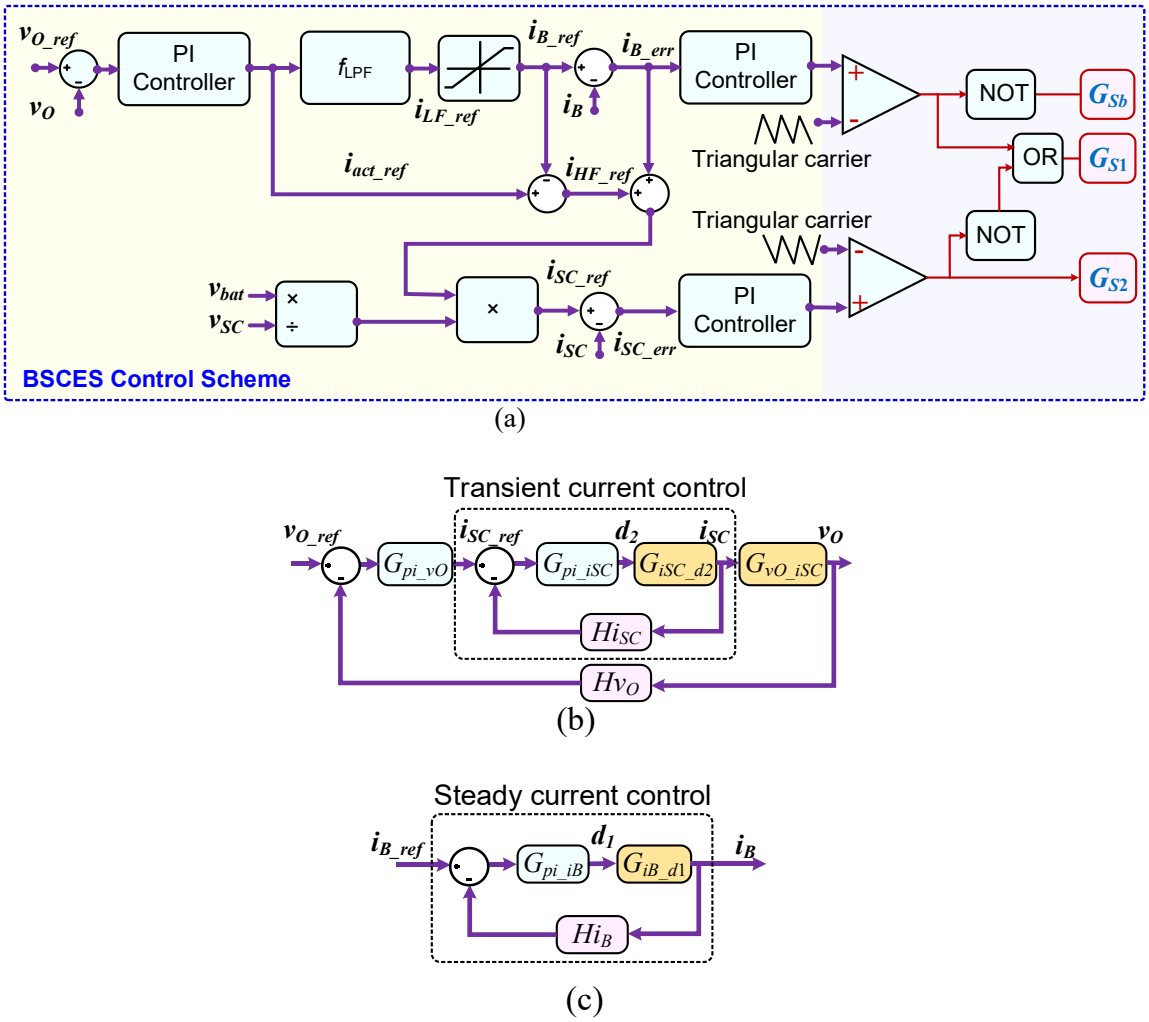


Fig.7.1 Control strategy for FPDCBSS system.

The DC-link voltage controller serves as the outer loop, while the SC current control loop functions as the inner loop, as illustrated in Fig. 7.1 (b). Additionally, the battery current controller block diagram, shown in Fig. 7.1 (c), operates independently from the SC controller and is responsible solely for controlling the battery current.

The controller is designed to guarantee the closed-loop stability of the FPDCBSS converter under all operating conditions. As shown in Fig. 7.1, the battery current plant G_{iB_d1}, the supercapacitor current plant G_{isc_d2}, and the output voltage plant G_{vo_d2} are employed for the design of the inner current controllers and the outer voltage controller, respectively. The pole-zero plots corresponding to *states*-I, II, III, and IV are presented in Fig. 7.2. as per the parameter defined in Table 7.1.

TABLE 7.1

DESIGN PARAMETERS OF FPDCBSS

Parameters	Values
Output port voltages: v_O, V_{bat}, and V_{SC}	90-110 V, 48 V, and 36 V
Inductors: L_S, L_B, and L_{SC}	560 µH, 560 µH, and 300 µH
ESR of Inductors: r_{LS}, r_{LB}, and r_{LSC}	320 mΩ, 320 mΩ, and 250 mΩ
Capacitors: C_O, C_b, and C_C	470 µF, 100 µF, and 3.1 F/21.6 V
ESR of Capacitors: r_{Co}, r_{Cb}, and r_{Cc}	200 mΩ, 100 mΩ, and 50 mΩ
Power $P_{o\max}$ / load resistance R_O	120 W / 100Ω-384Ω
Switching frequency f_S	20 kHz

From the stability analysis, it is observed that controller design is primarily required for *states*-I, III, and IV, whereas *state*-II corresponds to the buck-mode operation and exhibits stable open-loop dynamics. Since *state*-V has the same operating characteristics as *state*-I, the controller designed for *state*-I is directly applicable to *state*-V. Similarly, *state*-VI represents the battery charging (buck-mode) operation and also exhibits stable dynamics. Therefore, controller design and stability analysis are focused on *state*-I, III, and IV.

Instead of depending just on nominal operating values, controller settings are designed taking into account uncertainties in the converter parameters to ensure robust performance under realistic operating situations. The converter poles and zeros are directly impacted by these uncertainties, which in turn have an impact on the overall stability margins. Thus, the open-loop transfer functions $G_{i_{SC}d_2}, G_{i_B d_1}, G_{v_O d_2}, G_{v_O i_{SC}}\big|_{S1}$ derived in previous chapter are examined over the specified uncertainty range to for appropriate robust controller design using Kharitonov's theorem and bandwidth segregation technique.

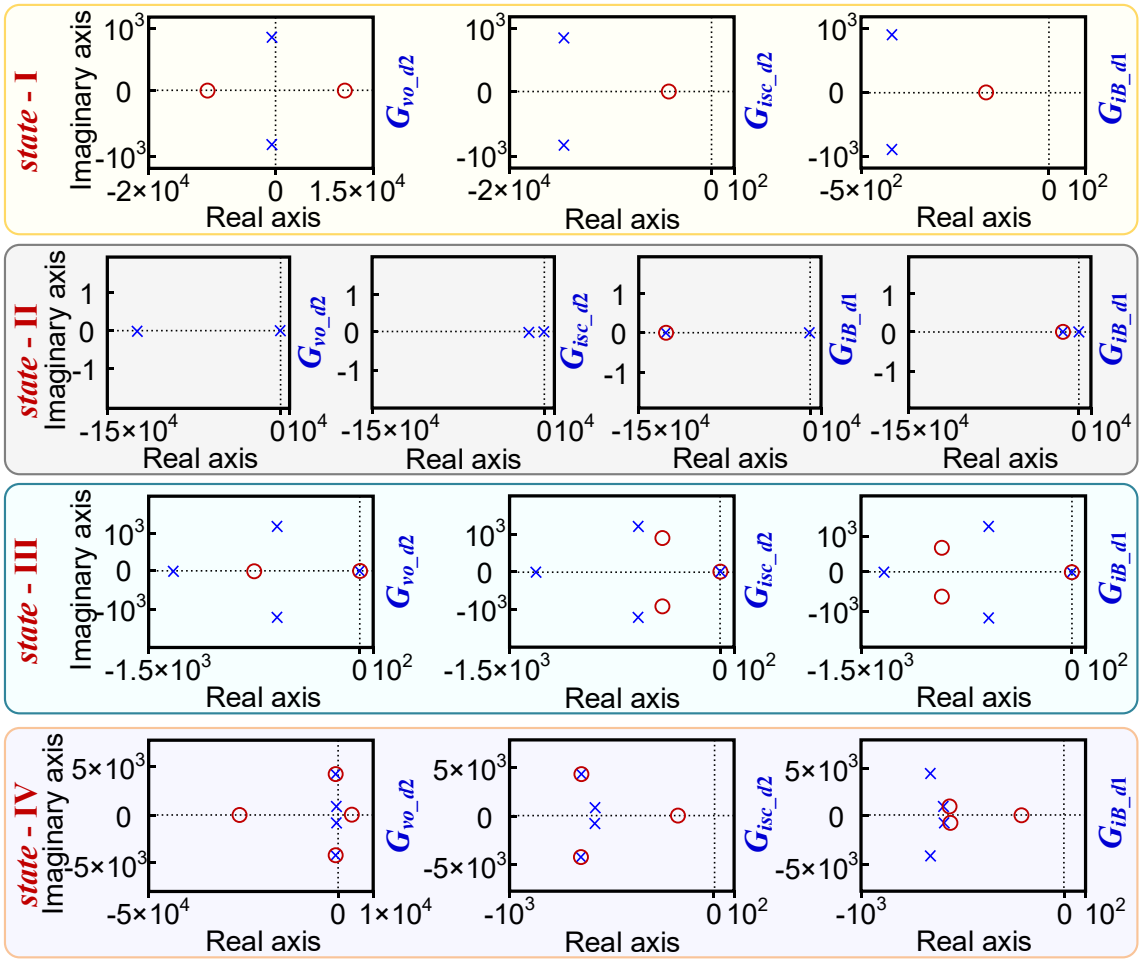


Fig. 7.2 Pole-zero plots of the transfer functions of the FPDCBSS in *states* I-IV under nominal operating conditions.

7.3 Kharitonov's Theorem and the Sixteen Kharitonov Plants

The various circumstances manufacturing tolerances, component age, operating temperature, and fluctuating loading circumstances, the precise values of system parameters are rarely known in real-world engineering systems. As a result, the plant's transfer function belongs to a family of uncertain models whose coefficients vary within predetermined intervals rather than being represented by a single deterministic model. These systems are frequently called interval systems.

Consider a transfer function with uncertainty,

$$G(s) = \frac{N(s)}{D(s)} \tag{7.1}$$

Where, $N(s) = b_m s^m + b_{(m-1)} s^{(m-1)} + \ldots\ldots + b_0$ 7.2

and $D(s) = a_n s^n + a_{(n-1)} s^{(n-1)} + \ldots\ldots + a_0$ 7.3

It is expected that each coefficient varies independently within predetermined limitations.

$$a_i \in [a_i^-, a_i^+], \quad b_i \in [b_i^-, b_i^+] \tag{7.4}$$

An infinite number of potential transfer functions result from this. It is computationally hard to assess the stability of any potential plant, especially for high-order systems. By reducing the infinite stability problem to the study of a finite number of specifically built plants, Kharitonov's theorem offers a sophisticated solution.

The numerator and denominator of the polynomial is written as

$$N(s) = \sum_{i=0}^{m} b_i s^i \quad \text{where, } b_i^- \le b_i \le b_i^+ \tag{7.5}$$

$$D(s) = \sum_{i=0}^{n} a_i s^i \quad \text{where, } a_i^- \le a_i \le a_i^+ \tag{7.6}$$

The resulting transfer function is a member of an infinite family since each coefficient can independently take on any value within its interval. The objective of robust controller design is to guarantee closed-loop stability for every member of this family.

7.3.1 Kharitonov Polynomials

The Kharitonov polynomials are four specifically designed edge polynomials that are obtained from an interval polynomial family by methodically choosing the unknown coefficients' lower and upper bounds in a predetermined alternating sequence. These four polynomials are essential to robust stability analysis because they reflect the important boundary instances of the entire interval family.

For denominator polynomial *D*(s) the four Kharitonov polynomials are,

$$
\begin{aligned}
N_1(s) &= a_0^- + a_1^- s + a_2^+ s^2 + a_3^+ s^3 + \cdots \\
N_2(s) &= a_0^+ + a_1^+ s + a_2^- s^2 + a_3^- s^3 + \cdots \\
N_3(s) &= a_0^+ + a_1^- s + a_2^- s^2 + a_3^+ s^3 + \cdots \\
N_4(s) &= a_0^- + a_1^+ s + a_2^+ s^2 + a_3^- s^3 + \cdots
\end{aligned}
\tag{7.7}
$$

Similarly, four Kharitonov numerator polynomials are obtained from the interval numerator. Thus, we have the numerator and denominator polynomials as N_1, N_2, N_3, N_4 and D_1, D_2, D_3, D_4 respectively.

Kharitonov's theorem shows that stability verification of these four edge polynomials is sufficient to assess the stability of the entire interval polynomial family, rather than examining an infinite number of potential polynomials. This amazing feature ensures solid mathematical guarantees while drastically reducing the computational complexity of robust stability analysis.

7.3.2 Sixteen Kharitonov Plants' Formation

Every Kharitonov polynomial in the numerator is combined with every Kharitonov polynomial in the denominator considering that the transfer function has uncertainty in both numerator and denominator. This leads to 4 × 4 = 16 plants vertex plant.

The sixteen plants are,

$$
\begin{aligned}
P_{11}(s) &= \frac{N_1(s)}{D_1(s)}; P_{12}(s) = \frac{N_1(s)}{D_2(s)}; P_{13}(s) = \frac{N_1(s)}{D_3(s)}; P_{14}(s) = \frac{N_1(s)}{D_4(s)} \\
P_{21}(s) &= \frac{N_2(s)}{D_1(s)}; P_{22}(s) = \frac{N_2(s)}{D_2(s)}; P_{23}(s) = \frac{N_2(s)}{D_3(s)}; P_{24}(s) = \frac{N_2(s)}{D_4(s)} \\
P_{31}(s) &= \frac{N_3(s)}{D_1(s)}; P_{32}(s) = \frac{N_3(s)}{D_2(s)}; P_{33}(s) = \frac{N_3(s)}{D_3(s)}; P_{34}(s) = \frac{N_3(s)}{D_4(s)} \\
P_{41}(s) &= \frac{N_4(s)}{D_1(s)}; P_{42}(s) = \frac{N_4(s)}{D_2(s)}; P_{43}(s) = \frac{N_4(s)}{D_3(s)}; P_{44}(s) = \frac{N_4(s)}{D_4(s)}
\end{aligned}
\tag{7.8}
$$

These sixteen transfer functions represent the sixteen Kharitonov plants or sixteen vertex plants.

One of the extreme realizations of the uncertain system is represented by each Kharitonov plant. The Kharitonov coefficient pattern is used to choose the numerator and denominator coefficients from either their minimum or maximum limits. As a result, each plant represents a distinct set of worst-case parameter values. In the transfer function space, the sixteen plants successfully delineate the edge of the uncertainty region. The

area surrounded by these vertex plants contains any actual plant created by parameter modifications. Consequently, it is anticipated that a controller will retain stability and acceptable performance for each intermediate plant within the uncertainty bounds if it works adequately for all sixteen plants.

7.4 Bandwidth Segregation in BSCES

A battery and a supercapacitor are operated in combination to exploit their respective advantages. While the supercapacitor has a high power density and can provide or absorb huge transient currents during abrupt changes in load circumstances, the battery has a high energy density and is the main energy source for meeting the average power requirement. Despite sharing a DC bus, the two storage devices have very different electrochemical properties, dynamic responses, and operational capacities. Therefore, to guarantee that each storage device contributes in accordance with its intrinsic features, a suitable power management approach is necessary.

One of the most popular energy management strategies for HESS is bandwidth segregation. This method's basic idea is to use frequency-domain filtering techniques to separate the overall load power demand into low-frequency and high-frequency components. Because of its high energy density and comparatively sluggish dynamic reaction, the battery is allocated the low-frequency component, which represents the slowly fluctuating average power demand. On the other hand, because of its superior power density, quick charge-discharge capability, and extended cycle life, the supercapacitor is assigned the high-frequency component, which corresponds to quick transient power fluctuations. Bandwidth segregation improves the overall performance and dependability of the HESS while allowing both energy storage devices to function within their ideal dynamic regions by dividing the power demand based on its frequency content.

7.4.1 Principle of Bandwidth Segregation

The idea behind bandwidth segregation stems from the fact that power consumption for particular application consists of many frequency components. The needed power varies considerably during steady-state requirement and is mostly composed of low-frequency components. However, high-frequency power transients are introduced over

brief periods of time by events including source power variation and abrupt load disturbances.

Mathematically, the total load power can be expressed as,

$$P_L(t) = P_{LF}(t) + P_{HF}(t) \tag{7.9}$$

where,

$P_L(t)$ represents the total load power,

$P_{LF}(t)$ denotes the low-frequency component,

$P_{HF}(t)$ represents the high-frequency component.

A low-pass filter (LPF) is used to obtain the low-frequency component, and the filtered output is subtracted from the total load power to obtain the high-frequency component. Thus,

$$P_{LF}(s) = H_{LPF}(s)P_L(s) \tag{7.10}$$

$$P_{HF}(s) = P_L(s) - P_{LF}(s) \tag{7.11}$$

The rapidly fluctuating transient power and the slowly fluctuating energy demand are successfully separated by the low-pass filter. As a result, the supercapacitor makes up for the quick power swings while the battery provides the average energy needs for the application.

7.4.2 Frequency Characteristics of Battery and Supercapacitor

Because of their electrochemical architectures, batteries and supercapacitors have essentially different operating properties. Although the battery has a comparatively high energy density, its internal electrochemical reaction rates and diffusion processes limit its power capacity. Regular exposure to high current transients shortens battery life, raises temperature, and speeds up internal deterioration. As a result, batteries are better suited to meeting gradually changing power requirements. Supercapacitors, on the other hand, have a high power density and incredibly low internal resistance, allowing for quick charging and discharging with little degradation. Over millions of charge-discharge cycles, they

can safely endure repeated high-current pulses. Supercapacitors are therefore perfect for managing abrupt load changes, regenerative braking energy, and transient power needs.

The complementary characteristics of the two storage devices make bandwidth segregation a natural and efficient power-sharing strategy.

7.4.3 Filter-Based Power Allocation

Frequency-selective filters are the main tool used to implement bandwidth segregation. First-order low-pass filters are frequently used due to their simplicity and convenience of use. The transfer function for it is given by,

$$H_{LPF}(s) = \frac{\omega_C}{s + \omega_C} \tag{7.12}$$

where, ω_c is the cutoff angular frequency. (7.13)

The battery and supercapacitor reference power becomes,

$$P_B(s) = H_{LPF}(s) P_L(s) \tag{7.14}$$

$$P_{SC}(s) = (1 - H_{LPF}(s)) P_L(s) \tag{7.15}$$

The frequency boundary between battery and supercapacitor functioning is established by the cutoff frequency. The battery is responsible for components below the cutoff frequency, whereas the supercapacitor supplies components above the cutoff frequency.

The power sharing performance is directly affected by cut off frequency appropriate selection of cut off frequency is essential. While very high cutoff frequency selection makes the battery react to quick transients resulting into shortening its operating lifetime,selection of a very low cutoff frequency puts more strain on the supercapacitor.

7.5 Design of PI controller for FPDCBSS

A proportional-integral (PI) controller is added to the control loop in order to overcome the drawbacks of the uncompensated system. The PI controller's transfer function is provided by

$$C(s) = K_P + \frac{K_i}{S} \tag{7.16}$$

Where, K_p is the proportional gain and K_i is the integral gain.

While the integral term adds a pole at the origin to remove steady-state error and enhance low-frequency tracking ability, the proportional term raises the total loop gain and speeds up responsiveness. By boosting the low-frequency gain, enhancing the phase characteristics around the crossover frequency, and expanding the system bandwidth, these two control operations collectively alter the system's frequency response. In order to provide sufficient PM, GM, and bandwidth segregation between the battery and supercapacitor current control loops, the PI controller settings are designed taking into account uncertainties in the converter parameters to ensure robust performance under realistic operating situations, such as $V_{SC} \in [30, 42]$, $V_{bat} \in [42, 54]$, and $R_O \in [100, 384]$. The nominal values of the converter system parameters are presented in Table 7.1, where ESR of capacitors and inductors are also considered during modeling of the FPDCBSS.

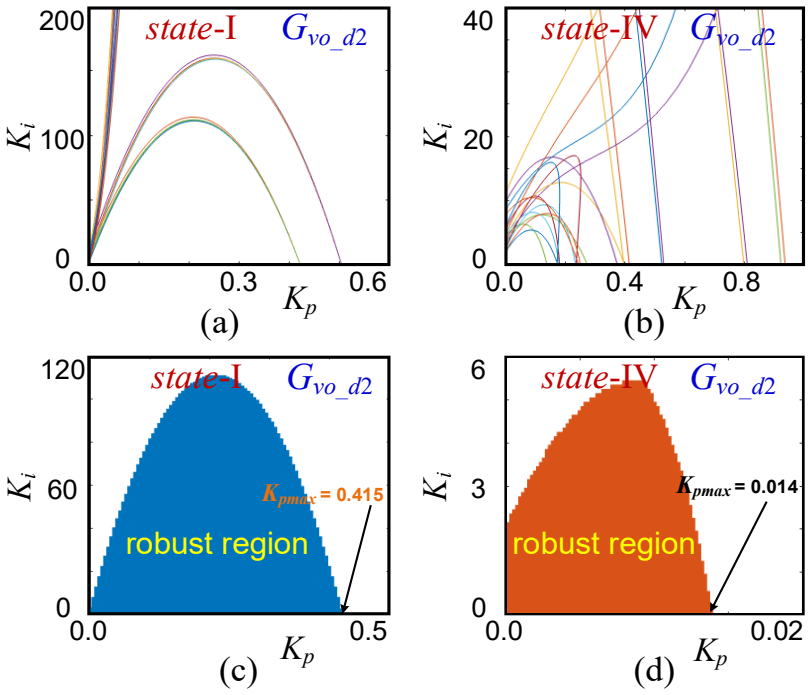


Fig. 7.3 Boundary loci of the Kharitonov 16-plant family for G_{vO_d2} (a) *state*-I, (b) *state*-IV, and the corresponding robust stability regions in the K_p and K_i plane for (c) *state*-I and (d) *state*-IV.

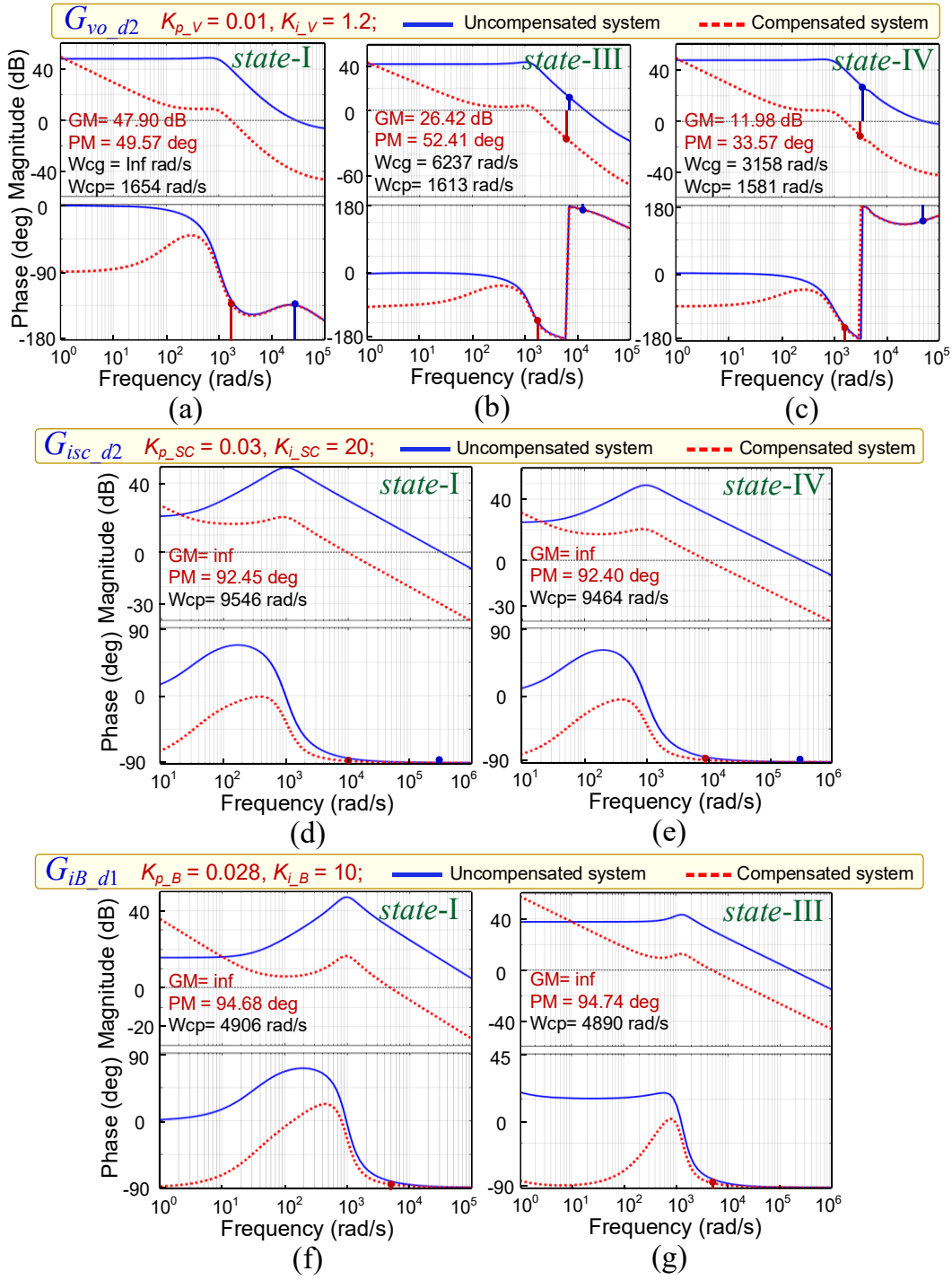


Fig. 7.4 Bode plots of the cascaded control architecture under different operating states, comparing the uncompensated plant and the PI-compensated open-loop response for output voltage controller $Gvod_2$: (a) state-I, (b) state-III, (c) state-IV; the supercapacitor

current controller $Gi_{sc}d_2$: (d) state-I, (e) state-IV; and the battery current controller $Gi_{B}d_1$: (f) state-I and (g) state-III.

Further, to ensure robust stability under parameter variations, the 16 Kharitonov plants are obtained in the K_p - K_i plane, as shown in Figs. 7.3 (a)-(d). The corresponding robust stability regions in the K_p and K_i plane for under *state*-I and *state*-IV are presented in Figs. 7.3 (c) and (d), respectively for G_{vO_d2}. The controller parameters are selected using the robust region given under *state*-IV to make the FPDCBSS stable under all the operating states and designed system parameter uncertainties.

The controller gains are chosen such that the guaranteed GM (> 6 dB) and guaranteed PM (> 30°) can be achieved. Based on the robust stability region, the optimal PI controller gains are selected using the analytical modeling approach *such as* $K_{p,SC} = 0.03$, $K_{i,SC} = 20$, $K_{p,B} = 0.028$, $K_{i,B} = 10$, $K_{p,V} = 0.01$, $K_{i,V} = 1.2$. The bode plots of uncompensated and compensated plants for output voltage, SC, and battery controller (i.e., Gv_Od_2, $Gi_{sc}d_2$, Gi_Bd_1) are plotted for the respective states as shown in Fig. 7.4.

It can be clearly seen from the results that the phase crossover frequency of the SC current controller ($\omega_{cp_sc} \approx 9500$ rad/s) is approximately twice that of the battery current controller ($\omega_{cp_B} \approx 4900$ rad/s) and nearly six times that of the output voltage controller ($\omega_{cp_Vo} \approx 1600$ rad/s), thereby ensuring the desired hierarchical bandwidth separation for stable cascaded control design. It shows that the SC current loop possesses the highest bandwidth to compensate for rapid power transients, the battery current loop operates at an intermediate bandwidth to regulate the slowly varying power demand, and the voltage loop is designed with the lowest bandwidth to ensure voltage regulation and stable interaction between the cascaded control loops.

The compensated frequency responses exhibit an increased PM with the desired crossover frequencies, resulting in improved transient response and enhanced closed-loop stability. The step responses of the FPDCBSS under sudden increase and decrease in load power demand is shown in Fig. 7.5, further validate the control strategy. It shows that during transient conditions, the SC immediately supplies or absorbs the transient power, whereas the battery current changes gradually to meet the steady-state power requirement.

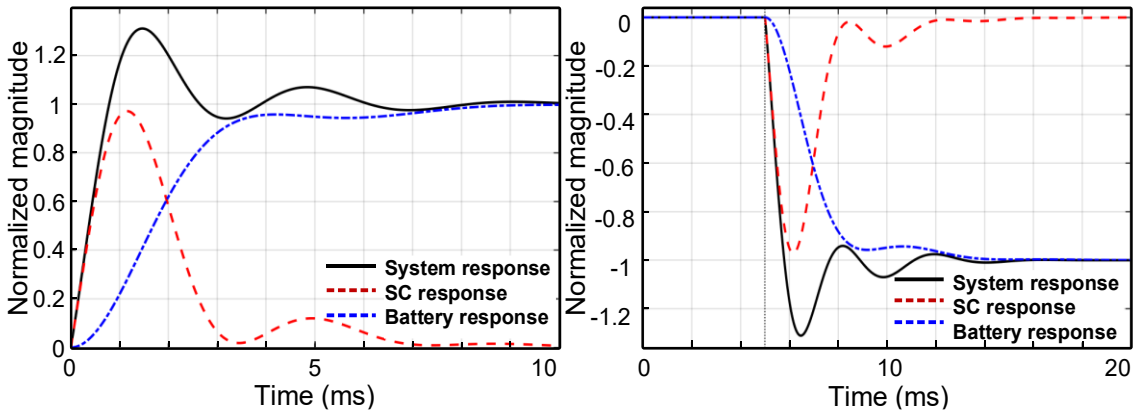


Fig. 7.5 Step response of the FPDCBSS for sudden changes in load power demand: (a) load power increase and (b) load power decrease.

7.6 Comparative Transient Analysis of Different ESS under Active Configurations

The performance of a HESS depends not only on the converter topology and controller but also on the manner in which the power demand is distributed between the available storage elements. In a BSCES, the battery is generally intended to supply the relatively slow-varying component of the power demand, whereas the supercapacitor is utilized to accommodate rapid variations and transient components. This complementary operation can reduce the high-frequency current component experienced by the battery and thereby improve the dynamic response of the DC bus.

To further demonstrate the importance of this power-sharing mechanism, two cases are considered. The first case corresponds to the proposed BSCES configuration. The second case replaces the supercapacitor with another battery and employs with the same controller. The same controller gains are maintained for the comparative simulations so that the observed differences primarily reflect the effect of the storage configuration and power-segregation strategy.

A step variation in the solar PV operating condition is applied at approximately 1 s, resulting in a transient response in the DC-bus voltage and storage currents. The corresponding source voltage, DC-bus voltage, battery current, supercapacitor current, and load current are examined for both the cases.

7.6.1 Battery–Supercapacitor Configuration

The response of the battery–supercapacitor configuration is shown in Fig. 7.6. Before the disturbance, the system operates under a nearly steady operating condition, with the battery supplying the dominant low-frequency component of the required power while the supercapacitor remains available to respond to rapid variations.

At approximately 1 s, a change in the source/bus operating condition produces a noticeable transient in the DC-bus voltage. The bus voltage initially decreases from its pre-disturbance value and subsequently recovers toward its steady-state operating value. The transient is accompanied by a corresponding variation in the battery and supercapacitor currents.

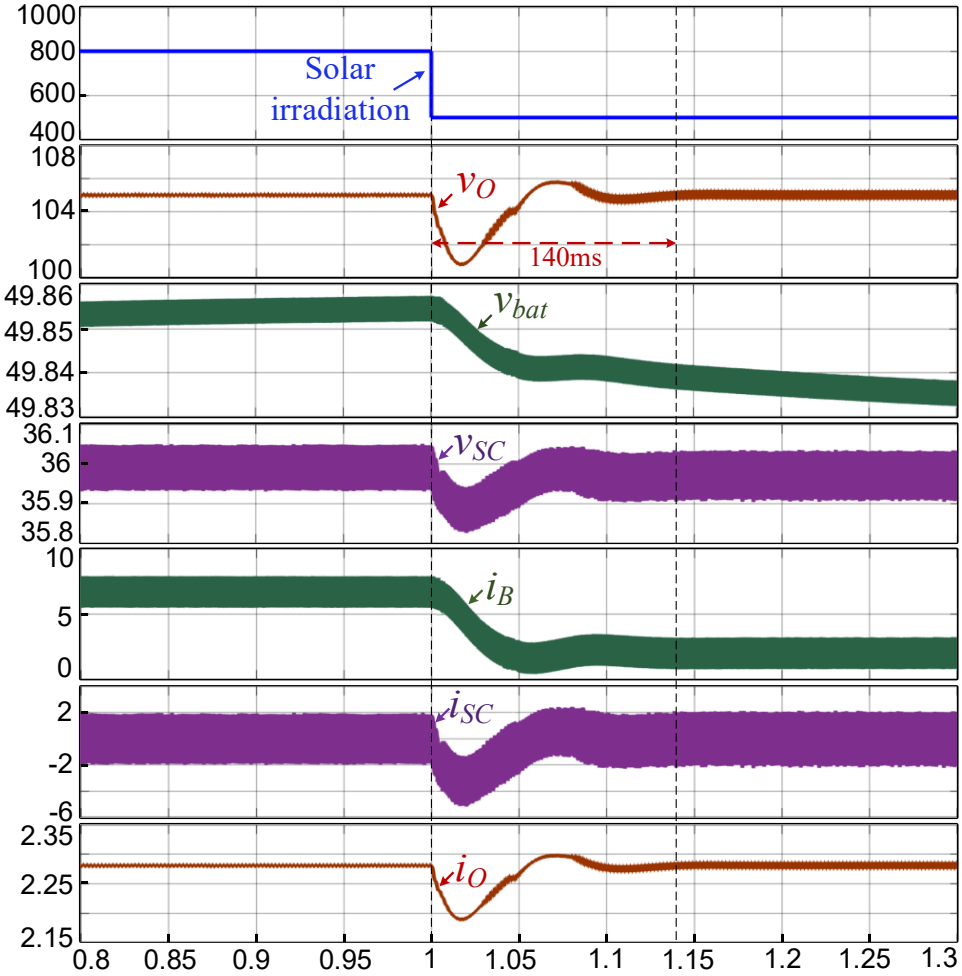


Fig. 7.6 Simulation response of the BSCES under a sudden change in solar irradiation.

A significant feature of this response is the rapid variation in the supercapacitor current immediately following the disturbance. The supercapacitor current changes rapidly in both magnitude and direction during the transient interval, demonstrating its ability to absorb or supply short-duration power. In contrast, the battery current changes more gradually and settles to a comparatively smooth value after the transient. This behavior demonstrates the complementary characteristics of the two storage elements. The battery current therefore primarily represents the relatively slow component of the power demand, whereas the supercapacitor provides rapid compensation during the transient. After the transient interval, the supercapacitor current returns toward its normal operating range while the battery resumes the major portion of the steady-state power contribution.

The load current also exhibits a transient corresponding to the applied disturbance. Despite this change, the DC-bus voltage returns toward its regulated value within 140 ms, indicating satisfactory regulation of the proposed energy-storage system.

7.6.2 Battery-Battery Configuration

The second simulation considers a battery–battery configuration as shown in Fig. 7.7. In this configuration, both the ports are connected with battery energy storage with same controller parameters.

Following the disturbance at approximately 1 s, the DC-bus voltage experiences a transient deviation and subsequently returns toward its steady-state value. The battery current changes significantly during this interval, while the current associated with the second storage unit responds to the transient component of the power demand. The transient current response of the second storage element demonstrates that frequency-based power segregation can direct rapid power variations away from the primary energy-storage path. The load current also exhibits a transient corresponding to the applied disturbance. Despite this change, the DC-bus voltage returns toward its regulated value within 190 ms when both the energy storage elements are batter with same controller gains, indicating slow regulation with respect to HESS system.

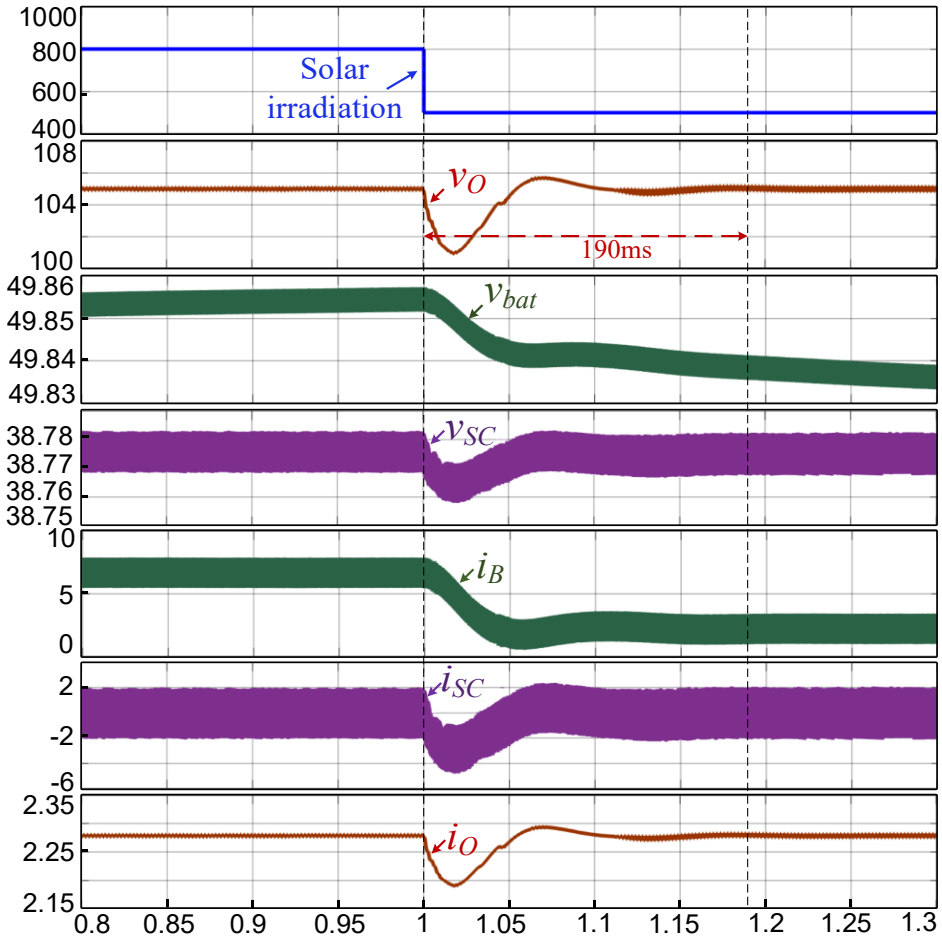


Fig. 7.7 Simulation response of the battery–battery ESS under a sudden change in solar irradiation.

7.7 Experimental validation

Fig. 7.8 shows the experimental setup, which is developed in the laboratory to test the FPDCBSS topology in real time. The setup is tested with input supply voltage of 36V with fixed bus voltage of 48V; the voltage of output port-2 (i.e., connected with battery) is 24V, and the voltage at output port-3 (i.e., connected with SC) is 18V. The values of the inductors are $L_S = L_B = 560\mu H$ and $L_{SC} = 300\mu H$. The dSPACE microlab box is used to operate and test the FPDCBSS. Hall-effect current sensors (ACS712) are used to measure the input current connected at the input port that is source, the battery current connected at the output port-2, and the SC current connected at the output port-3, so that it can be given to the controller. The voltage sensors LV25-P are used to measure the input voltage,

load voltage, V_{bat}, and V_{SC}. The results are captured using mixed MSO, where are the channels are clearly labeled.

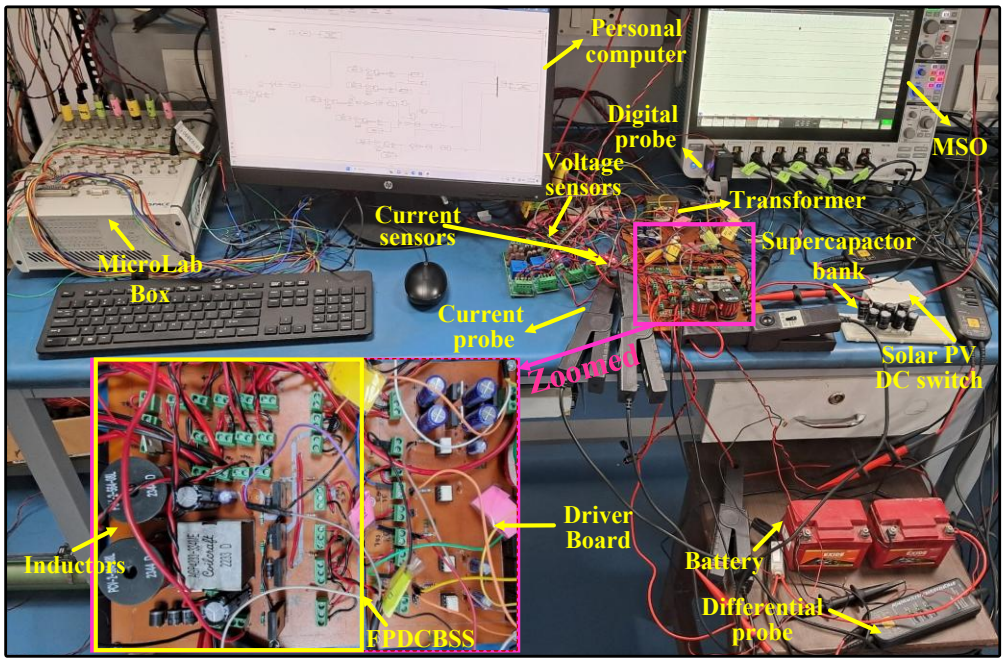


Fig. 7.8 Experimental setup of FPDCBSS.

The experimental results shown in Fig. 7.9 verifies system behavior during transient and steady-state conditions. The dc bus voltage remains regulated around 48V, confirming effective closed-loop control of the boost stage and coordinated switching of the four-port converter. Even during transient disturbances, the bus deviation is minimal, indicating strong dynamic response. The input supply voltage V_{PV} varies from 0V to 35.7 V, the dc bus voltage v_O varies from 0V to 47.9V, the voltage probe connected after the switch and battery voltage V_{bat} varies from 0V to 25V, the SC voltage V_{SC} varies from 0V to 17.3V. The battery initially discharges when the circuit is turned on; however, under steady-state conditions, it begins charging with a current of 380 mA (*note*: the measured battery current in all the experimental results is scaled by a factor of 10 because of the current probe configuration.) Since the load consumes most of the available power, only a small charging current flows into the battery. During transient intervals, the SC absorbs or supplies sudden current demand. Once steady state is reached, SC current settles to zero with negligible oscillation, proving stability of controller implementation.

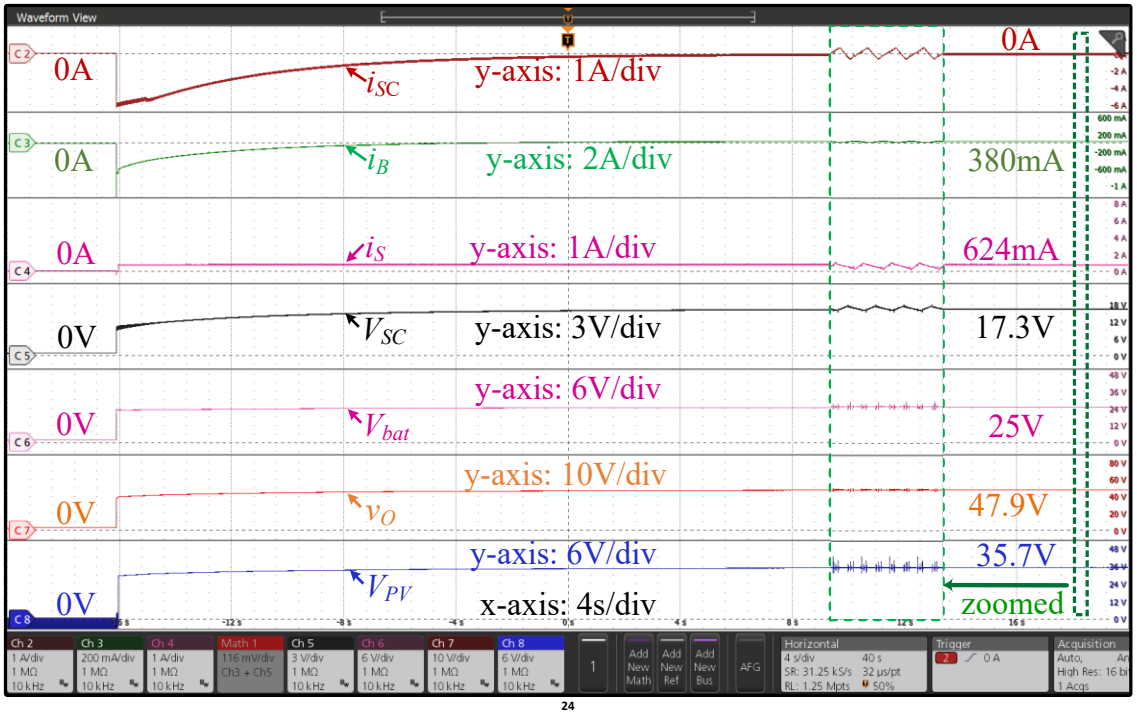


Fig. 7.9 Performance validation of FPDCBSS under transient and steady-state conditions.

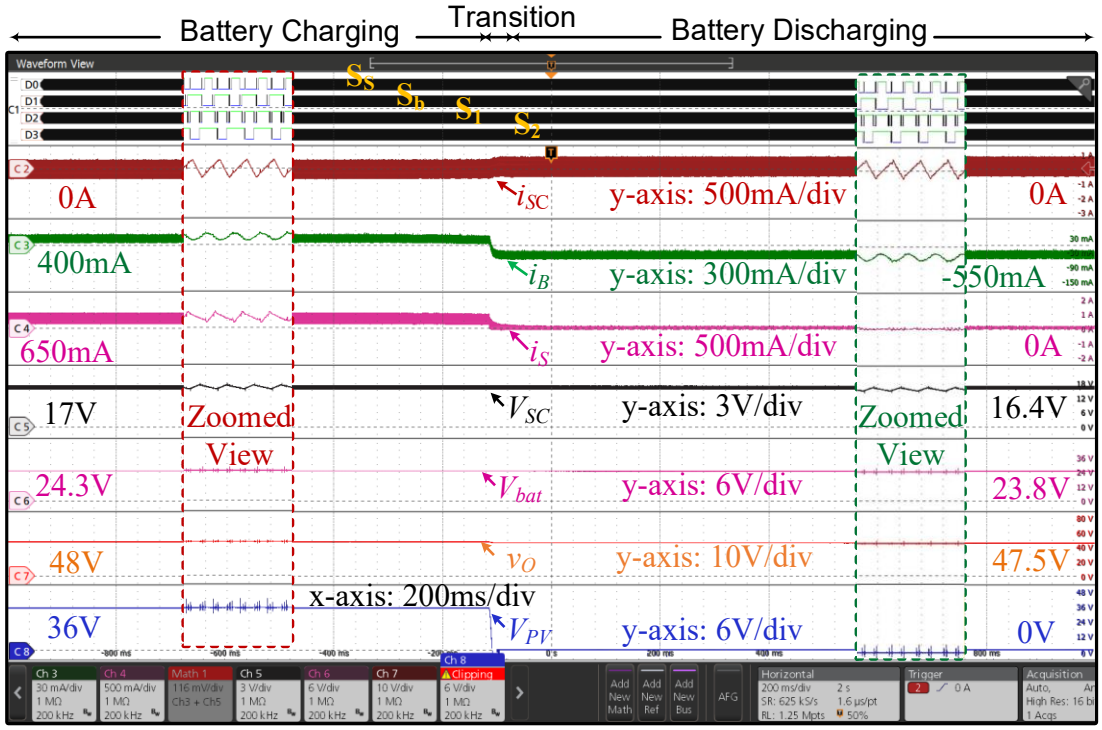


Fig. 7.10 Experimental validation of FPDCBSS under transient and steady-state conditions with charging to discharging conditions.

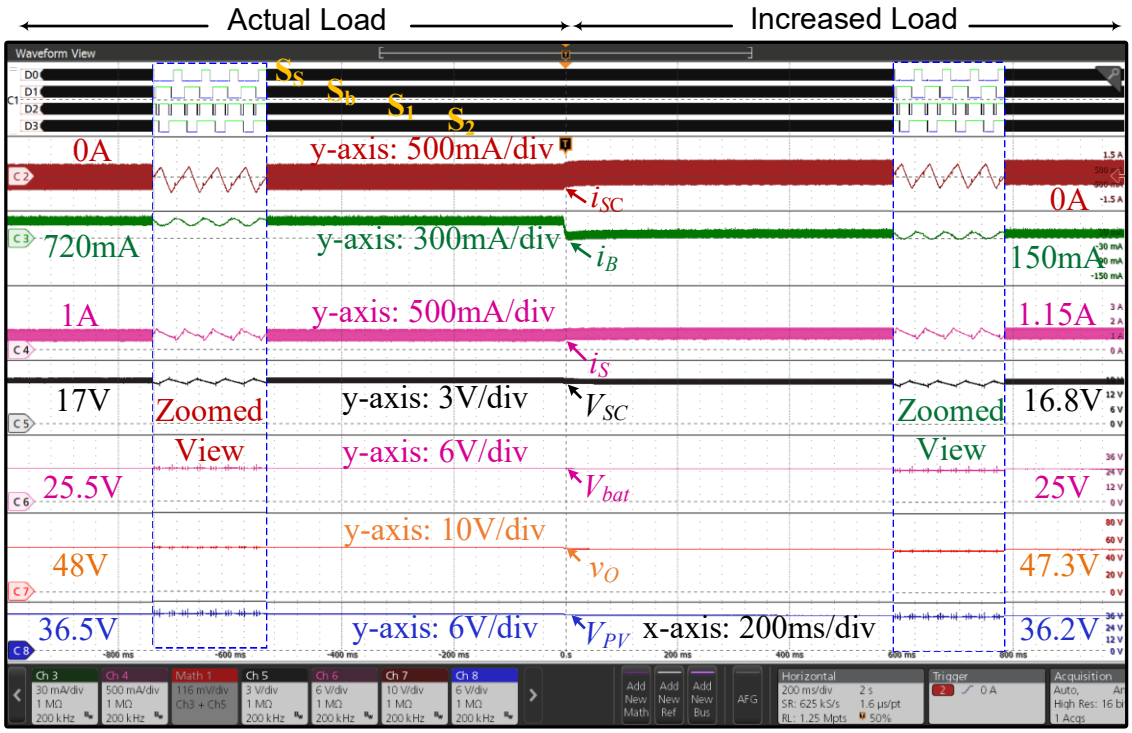


Fig. 7.11 Experimental validation of FPDCBSS under transient and steady-state conditions with load changes from 120Ω to 60Ω.

Fig. 7.10 shows the battery operating in bidirectional mode that is charging and discharging mode of operation. In battery charging mode surplus PV power is utilized to charge the battery while maintaining bus voltage regulation. The charging current is smooth, indicating proper PWM modulation and filtering. The discharging mode occurs when PV power reduces or load increases, the battery supports the dc bus. The direction change of battery current confirms seamless bidirectional power flow through switches S_b and S_1-S_2 and corresponding diodes. Importantly, the transition between charging and discharging occurs without bus voltage fluctuation, demonstrating coordinated multiport control. The results shown in Fig. 7.11 validates dynamic load performance, the battery current changes more gradually, whereas the SC current responds rapidly during load step change, the bus voltage remains regulated at fixed voltage. The SC handles high-frequency transient components, the battery supplies average power and the PV port provides primary generation power. The hardware results clearly demonstrate proper energy management among PV, load, battery, and SC ports.

7.8 Conclusion

The FPDCBSS maintains a constant dc bus voltage with a reduced switch count compared to conventional HES systems that require three separate dc-dc converters. The common-ground four-port topology enables bidirectional power flow among the input source, battery, SC, and load using a single power conversion stage, resulting in reduced component count and improved power conversion efficiency. The averaged and small-signal models are developed to design the controller under different operating states. The controller parameters are selected using Kharitonov-based robust stability analysis to satisfy the specified gain and PM requirements under converter parameter variations. The coordinated control strategy provides power sharing by allowing the SC to respond to transient power demand, while the battery supplies the steady-state power requirement, thereby reducing battery stress and improving the dynamic response of the system. Experimental results obtained from the 100 W prototype validate stable operation, effective dc bus voltage regulation, and satisfactory performance under variations in input power and load conditions. The reduced switch count, coordinated control, and bidirectional operating capability of the FPDCBSS enable its application in REI, EV, and other BSCES systems.

Chapter 8

Conclusion, Future Scope and Societal Impact

8.1 Introduction

The DC microgrid based on renewable energy generation, ESS and DC load has promoted the demand for DC-DC power converters. However, these power converters are utilized to interface the sources, storage devices, and loads have a significant impact on the performance of such systems. In addition to supplying the necessary voltage and current, the converter must function effectively, react fast to variations in power consumption, and maintain stability under a variety of operating circumstances.

The described work done in this thesis was done to achieve a broader goal beginning with the characterization of *n*PIBC having circuit parasitic and further steady state and small signal analysis for observing the effect of ESR of branch inductor, source and filter capacitor and voltage drop across switches and diodes on behavior of various *n*PIBC that is CBC, Two-phase IBC and TPIBC. Further the change in PM and GM has been investigated for change in parasitic and number of phases of *n*PIBC. The behavior of converter ripple current was analyzed for different number of phases for battery charging application. Subsequently, the investigation of non-overlapping and overlapping under CCM and DCM mode of operation for TPIBC was carried out. The effect of CCM and DCM on output ripple current and switching and conduction loss was reviewed. Further, ZVS soft switching TPRC TPIBRC has been modeled with high charging current and low output ripple current application such as EV charging.

The research has also considered the use of a battery–supercapacitor hybrid ESS. A FPDCBSS with robust control architecture has been developed for various application. The six states of operation comprising of twelve modes of operation has been analyzed. After the mathematical modeling the transfer function has been developed for robust controller design using Kharitonov's theorem

The main findings of the research are presented in this chapter. The conclusions are followed by the possible directions for future work and the societal impact of the research has been presented.

8.2 Conclusion

The research work presented in this thesis has investigated the modeling, characterization, analysis, and control of interleaved and multiport power converters for battery charging, energy storage, and DC microgrid applications. The state-space analysis, including steady-state and small-signal modeling, has been developed for an *n*-phase IBC considering practical circuit parasitic components. A comparative stability analysis has been carried out for a conventional single-phase buck converter, a two-phase IBC, and TPIBC using the designed converter parameters. The influence of circuit parasitics and variations in filter capacitance around the designed operating values has also been investigated through the corresponding phase-margin analysis. The results demonstrate that increasing the number of interleaved phases significantly reduces the input and output current ripple, while a sufficiently high filter capacitance further minimizes the ripple. The developed mathematical model incorporates important practical non-idealities, including the ESR of the source, inductor, and capacitor, together with the forward voltage drop of the diodes and the on-state voltage drop of the switches. The inclusion of these parasitic parameters improves the agreement between the analytical results and experimental observations and provides a more realistic representation of the converter dynamics. The analysis further confirms that the dynamic characteristics of the converter must be considered while designing the control loop for a particular application. In this regard, the proposed modeling approach provides a simple and effective means of understanding the influence of parasitic components on the dynamics and stability of interleaved converters. Among the investigated configurations, the TPIBC with circuit parasitics exhibits improved stability and reduced i^2R losses compared with the single-phase buck converter with parasitic components. The analysis also establishes that an *n*-phase IBC is preferably operated below the 1/n duty-cycle region to achieve effective ripple cancellation and improved operating performance.

The time-domain characterization of the TPIBC has further been presented to investigate the current-ripple behavior, turn-on and turn-off switching losses, and total converter losses under constant-power and fixed-resistance load conditions. The TPIBC is particularly suitable for high-output-current applications, including electrolyzers and battery energy-storage systems, where reduced current ripple can contribute to lower

energy losses and improved battery life. The analytical relationships developed in the study provide useful guidelines for selecting the DC-bus voltage and corresponding duty ratio according to the load profile and required power rating. These relations enable the converter parameters to be selected for improved performance in terms of current ripple, switching losses, and total converter losses. The operating behavior of the TPIBC is found to depend significantly on the switching-signal characteristics, including overlapping and non-overlapping switching intervals, as well as on the CCM and DCM of the inductor current and the nature of the connected load. The derived expressions also provide a systematic basis for designing the converter to operate in either CCM or DCM. For a constant-power load, the switching losses decrease with an increase in duty ratio and further decrease when the converter transitions from CCM to DCM. However, the percentage output-current ripple increases with output current from region-1 (R1) to region-3 (R3) and also increases during the transition from CCM to DCM. It is also observed that the magnitude of the inductor current ripple, Δi_L remains unchanged for a particular duty ratio even when the output power is varied.

A fast-charging TPIBRC has also been investigated for high-current applications requiring high current gain and low current ripple. The proposed converter enables FC through multiple ports employing HFTs and three-phase interleaved branches, while slow discharging can be achieved through a single high-frequency transformer port with the same interleaved structure. The simulation results demonstrate the suitability of the proposed TPIBRC for efficient soft-switching operation. The output power can be controlled through modified switching of the front-end interleaved bridges, phase shifting between the primary and secondary bridges, and variation of the switching frequency while maintaining the resonant frequency of the individual interleaved tanks. The converter is operated in the inductive region, where the switching frequency is higher than the resonant frequency, enabling ZVS operation of the switches. The use of three interleaved branches also reduces the transformer size because the current handled by each individual port is approximately one-third of that required in a corresponding single-port configuration. The proposed TPIBRC has been designed for variable input voltage and constant secondary-side voltage, and the MATLAB-based simulation results confirm that the switches in all three interleaved branches operate under ZVS conditions.

Finally, a FPDCBSS has been developed for the coordinated integration of the input source, battery, supercapacitor, and load. The proposed topology maintains a regulated DC-bus voltage while requiring fewer switches than conventional HESS based on three separate DC–DC converters. The bidirectional power flow between BSESS and load is achieved by its common-ground four-port configuration, which curb the requirement of separate converters for all storage system and load resulting into reduction in number of components and increases total power-conversion efficiency. To achieve a robust controller design and dynamic analysis, averaged and small-signal models have been carried out for the various operating modes. The desired gain and phase-margin specifications under uncertain converter parameters is obtained for closed loop control using Kharithnov-based robust stability analysis. While the battery provides mainly steady-state power requirement, the coordinated energy-management ensures the supercapacitor to react to HF transient power demands. This synchronized power-sharing method enhances the system's overall transient response and reduces the battery's stress from high-frequency current.

Stable operation, efficient DC-bus voltage control, and acceptable performance under changes in input power and load conditions are confirmed by an experimental validation prototype. Overall, the suggested FPDCBSS is a promising solution for renewable energy integration, EV charging, and battery–supercapacitor energy-storage applications due to its fewer switches, bidirectional power-flow capability, coordinated battery–supercapacitor power sharing, and control design. Collectively, the outcomes of this thesis demonstrate that accurate consideration of parasitic effects, appropriate selection of the interleaved converter operating region, reduction of current ripple, soft-switching operation, and coordinated hybrid energy-storage control are essential for developing efficient, stable, and reliable power conversion systems for next-generation DC energy application.

8.3 Future Scope of work

The use of SiC and GaN semiconductor devices can be investigated in future implementations of the proposed converters. Higher switching frequencies may allow further reduction in passive component size and improve power density. However, higher-frequency operation also makes parasitic inductances, switching transients, EMI, and

layout-related effects more significant. Therefore, future research can extend the parasitic modeling approach developed in this thesis to high-frequency wide-bandgap converter systems.

The modular structure of interleaved converters provides an opportunity for fault-tolerant operation. Future work can investigate the behavior of the converter when one phase or one switching device fails. A suitable control strategy may allow the remaining phases to continue operation at reduced power. Such a feature would be valuable for applications where uninterrupted operation is important, including EV charging stations, data centers, renewable-energy systems, and critical DC microgrids.

The proposed converter and HESS structure can be extended to EV charging stations. Future research can investigate the use of the supercapacitor for handling short-duration high-power charging demands while the battery or grid supplies the average power requirement. The system can also be extended to bidirectional EV charging and vehicle-to-grid operation. In such a system, the vehicle battery itself can become part of the energy management system, providing additional flexibility to the DC microgrid.

The present research focuses mainly on converter dynamics and power sharing. Future work can include detailed battery aging and degradation models. The energy management system can be designed to consider both the state of charge and state of health of the battery. The controller could then select the battery and supercapacitor power contribution in a way that not only meets the instantaneous power demand but also minimizes battery degradation. This would be particularly useful for EV applications, where battery lifetime is an important concern.

The HESS can potentially be used to improve the stability of the DC bus during sudden changes in constant-power load demand. Further research is required to investigate the interaction between the negative incremental impedance of constant-power loads and the dynamic behavior of the battery and supercapacitor converters.

8.4 Societal Impact

The importance of the research presented in this thesis extends beyond the development and analysis of power electronic converters. The technologies investigated in this work are closely connected with several major changes taking place in the energy and transportation sectors. The power converters that could effectively handle variable energy

generation system are necessary for shifting to DG from conventional electric power generation. Due to their inherent intermittent nature, solar and wind energy integration into the electrical grid requires appropriate energy storage and regulation system. The integration and use of renewable energy can be enhanced by the proposed converter and HESS methods examined in this thesis. The requirement for frequent AC–DC and DC–AC power conversion can also be decreased by the development of effective DC microgrids. Various applications where a large number of sources, storage devices, and loads are intrinsically DC has the benefit.

The need for reliable, powerful charging infrastructure will rise as EVs become more common. Hybrid energy storage can offer further assistance during abrupt changes in power demand, and interleaved converters can help manage high charging currents while lowering current ripple. Thus, this study also help in EV charging application. The possible decrease in battery stress is another significant advantage. The battery can be protected from rapid current fluctuations by enabling the supercapacitor to manage high-power transients. This could help batteries last longer and require fewer replacements. This may also lessen the long-term environmental effects of battery production and disposal.

The integration of renewable energy with electrolyzers also promotes green hydrogen production. Hydrogen can serve as a long-duration potential energy source and can support the energy requirement sectors where direct electrification is difficult.

The increased uses of renewable energy, better BESS management, increased converter efficiency can achieve lower energy losses and greenhouse gas emissions which is better from environmental perspective. Economically, the development of green hydrogen, EVs, energy storage, and renewable energy can create scope for employment, research, and manufacturing.

Therefore, the potential contribution of this research is creation of clean, reliable and efficient energy systems for a wider influence. The work has applications in renewable energy, electric mobility, energy storage, DC microgrids, and future sustainable energy infrastructure, though its main focus is converter modeling and control.

8.5 SDG Mapping of the Research

The research reported in this thesis is mapped chapter-wise to the SDGs for which a meaningful and demonstrable linkage is supported by the research objectives, methodologies, analyses, findings, and intended applications. The mapping below identifies the relevant research contribution and states its strength as Strong, Moderate, or Weak. The mapping is evidence-based and is intended to complement societal-impact discussion.

The most direct linkages are with SDG 7 (Affordable and Clean Energy) and SDG 9 (Industry, Innovation and Infrastructure), because the thesis develops and evaluates converter architectures and control methods for renewable-energy integration, energy storage, high-current conversion, and reliable DC power systems. Links to SDG 11 and SDG 13 are indirect and application-oriented, through potential deployment in EV charging, DC microgrids, and renewable-energy systems; they are therefore assigned a Moderate contribution strength.

S. No.	SDG Number / Official Title / Coloured SDG Logo	Research Work – Chapter-wise / Research Publication-wise Relevance	Strength of Contribution
1	SDG 7 AFFORDABLE AND CLEAN ENERGY 	Chapters 1–2 establish the renewable-energy, DC-microgrid, and energy-storage context. Chapters 5–7 investigate interleaved/multiport conversion, PV–battery–supercapacitor integration, bidirectional power flow, and coordinated energy management. Chapter 8 consolidates the findings. These contributions provide converter-level methods relevant to integrating renewable sources and storage efficiently; the thesis does not itself establish a quantified increase in renewable generation or energy access.	**Strong**

2	**SDG 9 INDUSTRY, INNOVATION AND INFRASTRUCT -URE** 	Chapters 3–4 develop and characterize parasitic-aware n-phase interleaved buck converters and examine operating regions, ripple, losses, and stability. Chapter 5 develops and analyzes interleaved multiport resonant converter configurations, including soft-switching operation for high-current charging. Chapters 6–7 present a four-port PV/battery/supercapacitor converter and robust control design, supported by simulation and experimental validation. These are direct engineering contributions to power-conversion technology and enabling infrastructure.	**Strong**
3	**SDG 11 SUSTAINABLE CITIES AND COMMUNITIE S** 	Chapters 1–2 discuss DC microgrids and EV charging as application contexts. Chapters 5–7 develop converter and hybrid-storage methods potentially applicable to EV charging infrastructure and renewable-energy-based DC systems. This linkage is application-oriented: the thesis provides enabling power-electronic technology but does not evaluate a deployed city-scale system or measure urban sustainability outcomes.	**Moderate**
4	**SDG 13 CLIMATE ACTION** 	Chapters 1–2 motivate renewable-energy integration and reduced dependence on conventional fossil-fuel-based electricity. Chapters 5–7 study converter architectures and hybrid energy storage that can facilitate the use of PV generation and support energy management. The contribution to climate action is indirect and enabling; the thesis does not quantify avoided emissions or conduct a life-cycle carbon assessment.	**Moderate**

8.6 Summary

The present research demonstrates that ideal models are not always sufficient to represent the behavior of practical converters, particularly when the converter has to function in uncertain situations. Therefore, effect of circuit parasitic components for *n*PIBC has been demonstrated. Further the effect of operating regions under CCM and DCM for TPIBC has been analyzed and its consequences for various applications has been reviewed. The modeling and characteristics of isolated DC-DC soft switching converter EV charging application has been carried out.

The BESS and SESS combination provides another important step toward developing flexible and reliable BSESS. The complementary characteristics of the two storage devices can be effectively utilized by assigning segregated power demand through low pass filter to the appropriate ESS. The BSESS can cater both the energy required for sustained operation and the rapid power response needed during transient conditions. As a result, the work highlights several crucial aspects of modern power converters including interleaved converter, resonant converter and multiport power converters using mathematical modeling, small-signal analysis, simulation and hardware implementation.

The future development of this research toward experimental validation, adaptive control, battery aging analysis, renewable-energy integration, EV charging, electrolyzer systems, fault-tolerant operation, and intelligent energy management can further improve the practical value of the work.

In conclusion, the detailed research and analysis in this thesis contributes to the ongoing development of power converters for various application including EV charging, electrolyzers, data centres and DC microgrids, these are capable of meeting the energy demand for changing landscape. The work provides a foundation for further research into reliable and efficient converter-based energy systems and supports the broader movement toward renewable energy integration, sustainable transportation, improved energy storage, and resilient DC power system.

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Appendix A

THEORETCAL RESULTS

The detailed theoretical derivations whose results has been given in main chapters has been presented in this appendix.

A.1 Supporting Mathematical Derivation for Practical *n*PIBC with Circuit Parasitic

The state space formation for chapter 3 considers the practical TPIBC rather than an ideal converter. The circuit includes the source resistance inductor ESRs, capacitor ESR, switch voltage drops, and diode forward-voltage drops.

Thus, for *n* branches define,

$$x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{Ln} \\ v_C \end{bmatrix} \tag{A1.1}$$

The total source current is

$$i_S = i_{L1} + i_{L2} + .. + i_{Ln} \tag{A1.2}$$

The output voltage is not exactly equal to the ideal capacitor voltage when capacitor ESR is considered. From the capacitor branch,

$$v_O = v_C + R_C i_C \tag{A1.3}$$

Since,

$$i_C = i_S - i_O \tag{A1.4}$$

and

$$i_O = v_O / R_O \tag{A1.5}$$

Substituting into A1.3 and simplifying, we get

$$v_O = \frac{R_O}{R_C + R_O} v_C + \frac{R_O R_C}{R_O + R_C} i_S \qquad \text{A1.6}$$

Therefore,

$$v_O = \frac{R_O}{R_{OC}} v_C + \frac{R_O R_C}{R_{OC}} (i_{L1} + i_{L2} + ... + i_{Ln}) \qquad \text{A1.7}$$

Equation (A1.7) is particularly important because it explains why the output equation of the practical converter contains both the capacitor voltage and the inductor-current terms.

A.1.1 Differential Equation of an Individual Converter Phase

Let s_x represent the switching state of phase x:

$$S_x = \begin{cases} 1, \text{ Switch ON} \\ 0, \text{ Switch OFF} \end{cases} \qquad \text{A1.8}$$

For phase x, the source-side voltage is affected by the source ESR. Therefore,

$$v_{S,\text{eff}} = v_S - R_S i_S \qquad \text{A1.9}$$

When the switch of phase x is ON,

$$Lx \frac{di_{Lx}}{dt} = v_S - R_S i_S - v_{SWx} - R_{Lx} i_{Lx} - v_O \qquad \text{A1.10}$$

Hence,

$$\frac{di_{Lx}}{dt} = \frac{v_S - R_S i_S - v_{SWx} - R_{Lx} i_{Lx} - v_O}{Lx} \qquad \text{A1.11}$$

When the switch is OFF, the inductor current freewheels through the diode. The source is isolated from that branch and the diode forward voltage appears in the current path:

$$\frac{di_{Lx}}{dt} = \frac{-v_O - v_{Dx} - R_{Lx} i_{Lx}}{Lx} \qquad \text{A1.12}$$

These two equations form the basic electrical relations from which the switching state equations used in Chapter 3 are obtained.

A.1.2 Capacitor Differential Equation

Applying KCL at the output node gives and substituting A1.7, we get

$$C\frac{dv_C}{dt} = i_{L1} + i_{L2} + ... + i_{Ln} - R_O v_O \qquad \text{A1.13}$$

After substituting, we get

$$\frac{dv_C}{dt} = \frac{R_O(i_{L1} + i_{L2} + ... + i_{Ln}) - v_C}{C} \qquad \text{A1.14}$$

A.1.3 Unified Switching State Equations

Equations (A1.11), (A1.12), and (A1.14) can be combined using the switching variable s_x.

$$\frac{di_{Lx}}{dt} = \frac{1}{L_x}\frac{[S_x(v_S - R_S i_S - v_{SWx} - v_O) + (1 - S_x)(-v_{Dx} - v_O) - R_{Lx} i_{Lx}]}{C} \qquad \text{A1.15}$$

Together with

$$\frac{dv_C}{dt} = \frac{R_O i_S - v_C}{C(R_O + R_C)} \qquad \text{A1.16}$$

the complete switching model can be written as

$$\dot{x} = f(x, u, s) \qquad \text{A1.17}$$

This is the fundamental equation from which the individual state-space matrices are generated.

A.1.4 Switching Modes of the TPIBC under Non-Overlapping

For the non-overlapping operating region of the three-phase converter, the six switching configurations can be represented as

$$\begin{array}{lll} M_1 : (1,0,0) & M_2 : (0,0,0) & M_3 : (0,1,0) \\ M_4 : (0,0,0) & M_5 : (0,0,1) & M_6 : (0,0,0) \end{array} \qquad \text{A1.18}$$

Thus, each switching configuration generates a different set of differential equations.

For example, during M_1,

$$\frac{di_{L1}}{dt} = \frac{v_S - R_S i_S - v_{SW1} - R_{L1} i_{L1} - v_O}{L_1} \quad \text{A1.19}$$

$$\frac{di_{L2}}{dt} = \frac{-v_{D2} - R_{L2} i_{L2} - v_O}{L_2} \quad \text{A1.20}$$

$$\frac{di_{L3}}{dt} = \frac{-v_{D3} - R_{L3} i_{L3} - v_O}{L_3} \quad \text{A1.21}$$

During the all-freewheeling condition,

$$\frac{di_{L1}}{dt} = \frac{-v_{D1} - R_{L1} i_{L1} - v_O}{L_1} \quad \text{A1.22}$$

$$\frac{di_{L2}}{dt} = \frac{-v_{D2} - R_{L2} i_{L2} - v_O}{L_2} \quad \text{A1.23}$$

$$\frac{di_{L3}}{dt} = \frac{-v_{D3} - R_{L3} i_{L3} - v_O}{L_3} \quad \text{A1.24}$$

Similar equations are obtained for M_3 and M_5 by replacing the conducting phase.

A.1.5 Conversion to State-Space Form

For each switching configuration (M_k), the differential equations can be rearranged into the standard form

$$\begin{aligned} \dot{x} &= A_k x + B_k u \text{ and} \\ y &= C_k x + D_k u \end{aligned} \quad \text{A1.25}$$

Here, for practical TPIBC

$$x = [i_{L1} \quad i_{L2} \quad i_{L3} \quad v_C]^T \quad \text{A1.26}$$

and the input vector contains the source and semiconductor voltage-drop quantities considered in the practical model:

$$u = [v_S \quad v_{SW1} \quad v_{SW2} \quad v_{SW3} \quad v_{D1} \quad v_{D2} \quad v_{D3}]^T \quad \text{A1.27}$$

The output is

$$y = v_O \quad \text{A1.28}$$

The matrices A_k, B_k, C_k, and D_k therefore represent the physical circuit behavior of the kth switching state. Chapter 3 defines these matrices for the individual switching configurations and subsequently performs their averaging.

For Ideal TPIBC,

$$R_S = 0; R_{Lk} = 0; R_C = 0; v_{SWk} = 0; v_{Dk} = 0 \qquad \text{A1.29}$$

A.2 Supporting Mathematical Derivation of the FPDCBSS Model

The mathematical model of the proposed FPDCBSS is developed in Chapter 6 using state-space averaging. The purpose of this appendix is to present the intermediate equations from which the state-space matrices are obtained. The derivation begins with the basic inductor voltage equations and capacitor current equations for each operating state and subsequently develops the averaged state equations.

For the derivation, the principal state variables are the battery-side current i_B, supercapacitor-side current i_{SC}, DC-bus or load voltage v_O, battery-side capacitor voltage V_B, and supercapacitor voltage V_{SC}, depending on the operating state.

A.2.1 State-I: Battery and Supercapacitor Discharging

State-I occurs when the available PV power is insufficient to meet the load demand and there is sudden increase in load demand. Both the battery and supercapacitor operate in boost mode and supply energy to the DC bus. The final thesis identifies M_1, M_2 and M_3 as the three switching modes associated with this state.

The state vector is

$$x = \begin{bmatrix} i_B & i_{SC} & v_O \end{bmatrix}^T ; u = \begin{bmatrix} V_{bat} \\ V_{SC} \end{bmatrix} \qquad \text{A2.1}$$

The averaged inductor equation for the battery path is obtained from the volt-second balance as,

Applying, KVL and KCL for Mode M_1, we get

$$\frac{di_B}{dt} = \frac{-v_O}{L_B} + \frac{V_{bat}}{L_B} \tag{A2.2}$$

$$\frac{di_{SC}}{dt} = \frac{-v_O}{L_{SC}} + \frac{V_{SC}}{L_{SC}} \tag{A2.3}$$

$$\frac{dv_{Co}}{dt} = \frac{i_B}{C_O} + \frac{i_{SC}}{C_O} - \frac{v_O}{R_O C_O} \tag{A2.4}$$

Therefore, the state space matrices for mode M_1 are written as,

$$A_1 = \begin{bmatrix} 0 & 0 & -1/L_B \\ 0 & 0 & -1/L_{SC} \\ 1/C_O & 1/C_O & -1/R_O C_O \end{bmatrix}; B_1 = \begin{bmatrix} 1/L_B & 0 \\ 0 & 1/L_{SC} \\ 0 & 0 \end{bmatrix} \tag{A2.5}$$

$$C_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}; D_1 = \begin{bmatrix} 0 \end{bmatrix}$$

Applying, KVL and KCL for Mode M_2, we get

$$\frac{di_B}{dt} = \frac{-v_O}{L_B} + \frac{V_{bat}}{L_B} \tag{A2.6}$$

$$\frac{di_{SC}}{dt} = \frac{V_{SC}}{L_{SC}} \tag{A2.7}$$

$$\frac{dv_{Co}}{dt} = \frac{i_B}{C_O} - \frac{v_O}{R_O C_O} \tag{A2.8}$$

Therefore, the state space matrices for mode M_2 is written as,

$$A_2 = \begin{bmatrix} 0 & 0 & -1/L_B \\ 0 & 0 & 0 \\ 1/C_O & 0 & -1/R_O C_O \end{bmatrix}; B_2 = \begin{bmatrix} 1/L_B & 0 \\ 0 & 1/L_{SC} \\ 0 & 0 \end{bmatrix} \tag{A2.9}$$

$$C_2 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}; D_2 = \begin{bmatrix} 0 \end{bmatrix}$$

Applying, KVL and KCL for Mode M_3, we get

$$\frac{di_B}{dt} = \frac{V_{bat}}{L_B} \quad \text{A2.10}$$

$$\frac{di_{SC}}{dt} = \frac{V_{SC}}{L_{SC}} \quad \text{A2.11}$$

$$\frac{dv_{Co}}{dt} = -\frac{v_O}{R_O C_O} \quad \text{A2.12}$$

Therefore, the state space matrices for mode M_3 is written as,

$$A_3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -1/R_O C_O \end{bmatrix}; B_3 = \begin{bmatrix} 1/L_B & 0 \\ 0 & 1/L_{SC} \\ 0 & 0 \end{bmatrix} \quad \text{A2.13}$$

$$C_3 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}; D_3 = \begin{bmatrix} 0 \end{bmatrix}$$

Therefore, the average state space matrices of FPDCBSS in state-I operation can be expressed as follows:

$$A_{S_1} = \begin{bmatrix} 0 & 0 & -(1-d_1)/L_B \\ 0 & 0 & -(1-d_2)/L_{SC} \\ (1-d_1)/C_O & (1-d_2)/C_O & -1/R_O C_O \end{bmatrix}; \quad \text{A2.14}$$

$$B_{S_1} = \begin{bmatrix} 1/L_B & 0 \\ 0 & 1/L_{SC} \\ 0 & 0 \end{bmatrix}; C_{S_1} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}; D_{S_1} = \begin{bmatrix} 0 \end{bmatrix}$$

A.2.2 State-II: Battery and Supercapacitor Charging

State-II occurs when the available PV power exceeds the instantaneous load requirement along with sudden decrease in load demand. In this state, both storage elements absorb energy from the DC bus. The switching modes *M*4, *M*5 and *M*6 form the complete switching sequence.

For this state, the state variables used by the displayed mathematical model are

$$x = \begin{bmatrix} i_B & i_{SC} & V_{bat} & V_{SC} \end{bmatrix}^T ; u = \begin{bmatrix} v_s \end{bmatrix} \quad \text{A2.15}$$

The averaged inductor equation for the battery path is obtained from the volt-second balance as,

Applying, KVL and KCL for Mode M_4, we get

$$\frac{di_B}{dt} = \frac{v_O}{L_B} - \frac{V_{bat}}{L_B} \quad \text{A2.16}$$

$$\frac{di_{SC}}{dt} = \frac{v_O}{L_{SC}} - \frac{V_{SC}}{L_{SC}} \quad \text{A2.17}$$

$$\frac{dv_{Cb}}{dt} = \frac{i_B}{C_b} - \frac{V_{bat}}{R_B C_b} \quad \text{A2.18}$$

$$\frac{dv_{Cc}}{dt} = \frac{i_{SC}}{C_C} - \frac{V_{SC}}{R_{SC} C_C} \quad \text{A2.19}$$

Therefore, the state space matrices for mode M_4 are written as,

$$A_4 = \begin{bmatrix} 0 & 0 & -1/L_B & 0 \\ 0 & 0 & 0 & -1/L_{SC} \\ 1/C_b & 0 & -1/R_B C_b & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC} C_C \end{bmatrix}; \; B_4 = \begin{bmatrix} 1/L_B & 1/L_{SC} & 0 & 0 \end{bmatrix}^T; \quad \text{A2.20}$$

$$C_4 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; D_4 = \begin{bmatrix} 0 \end{bmatrix}$$

Applying, KVL and KCL for Mode M_5, we get

$$\frac{di_B}{dt} = \frac{v_O}{L_B} - \frac{V_{bat}}{L_B} \tag{A2.21}$$

$$\frac{di_{SC}}{dt} = -\frac{V_{SC}}{L_{SC}} \tag{A2.22}$$

$$\frac{dv_{Cb}}{dt} = \frac{i_B}{C_b} - \frac{V_{bat}}{R_B C_b} \tag{A2.23}$$

$$\frac{dv_{Cc}}{dt} = \frac{i_{SC}}{C_C} - \frac{V_{SC}}{R_{SC} C_C} \tag{A2.24}$$

Therefore, the state space matrices for mode M_5 are written as,

$$A_5 = \begin{bmatrix} 0 & 0 & -1/L_B & 0 \\ 0 & 0 & 0 & -1/L_{SC} \\ 1/C_b & 0 & -1/R_B C_b & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC} C_C \end{bmatrix}; \; B_5 = \begin{bmatrix} 1/L_B & 0 & 0 & 0 \end{bmatrix}^T; \tag{A2.25}$$

$$C_5 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; D_5 = \begin{bmatrix} 0 \end{bmatrix}$$

Applying, KVL and KCL for Mode M_6, we get

$$\frac{di_B}{dt} = -\frac{V_{bat}}{L_B} \tag{A2.26}$$

$$\frac{di_{SC}}{dt} = -\frac{V_{SC}}{L_{SC}} \tag{A2.27}$$

$$\frac{dv_{Cb}}{dt} = \frac{i_B}{C_b} - \frac{V_{bat}}{R_B C_b} \tag{A2.28}$$

$$\frac{dv_{Cc}}{dt} = \frac{i_{SC}}{C_C} - \frac{V_{SC}}{R_{SC} C_C} \tag{A2.29}$$

Therefore, the state space matrices for mode M_6 is written as,

$$A_6 = \begin{bmatrix} 0 & 0 & -1/L_B & 0 \\ 0 & 0 & 0 & -1/L_{SC} \\ 1/C_b & 0 & -1/R_B C_b & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC} C_C \end{bmatrix}; \; B_6 = \begin{bmatrix} 0 & 0 & 0 & 0 \end{bmatrix}^T; \quad \text{A2.30}$$

$$C_6 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; D_6 = \begin{bmatrix} 0 \end{bmatrix}$$

Therefore, the average state space matrices of FPDCBSS in state-II operation can be expressed as follows:

$$A_{S2} = \begin{bmatrix} 0 & 0 & -1/L_B & 0 \\ 0 & 0 & 0 & -1/L_{SC} \\ 1/C_b & 0 & -1/R_B C_b & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC} C_C \end{bmatrix}; \quad \text{A2.31}$$

$$B_{S2} = \begin{bmatrix} (1-d_1)/L_B & (1-d_2)/L_{SC} & 0 & 0 \end{bmatrix}^T; \; C_{S2} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; D_{S2} = \begin{bmatrix} 0 \end{bmatrix}$$

A.2.3 State-III: Battery Discharging and Supercapacitor Charging

State-III occurs when the available PV power is less than load demand along with sudden decrease in load demand. In this state, Battery supplies to DC bus and SC absorb energy from the DC bus. The switching modes *M*7, *M*8 and *M*9 form the complete switching sequence.

For this state, the state variables used by the displayed mathematical model are

$$x = \begin{bmatrix} i_B & i_{SC} & v_O & V_{SC} \end{bmatrix}^T; u = \begin{bmatrix} V_{bat} \end{bmatrix} \quad \text{A2.32}$$

The averaged inductor equation for the battery path is obtained from the volt-second balance as,

Applying, KVL and KCL for Mode M_7, we get

$$\frac{di_B}{dt} = \frac{-v_O}{L_B} + \frac{V_{bat}}{L_B} \tag{A2.33}$$

$$\frac{di_{SC}}{dt} = \frac{v_O}{L_{SC}} - \frac{V_{SC}}{L_{SC}} \tag{A2.34}$$

$$\frac{dv_{Co}}{dt} = \frac{i_B}{C_O} - \frac{i_{SC}}{C_O} - \frac{v_O}{R_O C_O} \tag{A2.35}$$

$$\frac{dv_{Cc}}{dt} = \frac{i_{SC}}{C_C} - \frac{V_{SC}}{R_{SC} C_C} \tag{A2.36}$$

Therefore, the state space matrices for mode M_7 are written as,

$$A_7 = \begin{bmatrix} 0 & 0 & -1/L_B & 0 \\ 0 & 0 & 1/L_{SC} & -1/L_{SC} \\ 1/C_O & -1/C_O & -1/R_O C_O & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC} C_C \end{bmatrix}; \; B_7 = \begin{bmatrix} 1/L_B & 0 & 0 & 0 \end{bmatrix}^T; \tag{A2.37}$$

$$C_7 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; D_7 = \begin{bmatrix} 0 \end{bmatrix}$$

Applying, KVL and KCL for Mode M_8, we get

$$\frac{di_B}{dt} = \frac{-v_O}{L_B} + \frac{V_{bat}}{L_B} \tag{A2.38}$$

$$\frac{di_{SC}}{dt} = -\frac{V_{SC}}{L_{SC}} \tag{A2.39}$$

$$\frac{dv_{Co}}{dt} = \frac{i_B}{C_O} - \frac{v_O}{R_O C_O} \tag{A2.40}$$

$$\frac{dv_{Cc}}{dt} = \frac{i_{SC}}{C_C} - \frac{V_{SC}}{R_{SC}C_C} \tag{A2.41}$$

Therefore, the state space matrices for mode M_8 are written as,

$$A_8 = \begin{bmatrix} 0 & 0 & -1/L_B & 0 \\ 0 & 0 & 0 & -1/L_{SC} \\ 1/C_b & 0 & -1/R_O C_O & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC}C_C \end{bmatrix}; \; B_8 = \begin{bmatrix} 1/L_B & 0 & 0 & 0 \end{bmatrix}^T; \tag{A2.42}$$

$$C_8 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; D_8 = \begin{bmatrix} 0 \end{bmatrix}$$

Applying, KVL and KCL for Mode M_9, we get

$$\frac{di_B}{dt} = \frac{V_{bat}}{L_B} \tag{A2.43}$$

$$\frac{di_{SC}}{dt} = -\frac{V_{SC}}{L_{SC}} \tag{A2.44}$$

$$\frac{dv_{Co}}{dt} = -\frac{v_O}{R_O C_O} \tag{A2.45}$$

$$\frac{dv_{Cc}}{dt} = \frac{i_{SC}}{C_C} - \frac{V_{SC}}{R_{SC}C_C} \tag{A2.46}$$

Therefore, the state space matrices for mode M_9 is written as,

$$A_9 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/L_{SC} \\ 0 & 0 & -1/R_O C_O & 0 \\ 0 & 1/C_C & 0 & -1/R_{SC}C_C \end{bmatrix}; \; B_9 = \begin{bmatrix} 1/L_B & 0 & 0 & 0 \end{bmatrix}^T; \tag{A2.47}$$

$$C_9 = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ D_9 = \begin{bmatrix} 0 \end{bmatrix}$$

Therefore, the average state space matrices of FPDCBSS in state-III operation can be expressed as follows:

$$A_{S3} = \begin{bmatrix} 0 & 0 & \frac{-(1-d_1)}{L_B} & 0 \\ 0 & 0 & \frac{(1-d_2)}{L_{SC}} & \frac{-1}{L_{SC}} \\ \frac{(1-d_1)}{C_O} & -\frac{(1-d_2)}{C_O} & \frac{-1}{R_O C_O} & 0 \\ 0 & \frac{1}{C_C} & 0 & \frac{-1}{R_{SC} C_C} \end{bmatrix}; \quad \text{A2.48}$$

$$B_{S3} = \begin{bmatrix} 1/L_B & 0 & 0 & 0 \end{bmatrix}^T;\ C_{S3} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ D_{S3} = \begin{bmatrix} 0 \end{bmatrix}$$

A.2.4 State-IV: Battery Charging and Supercapacitor Discharging

State-IV occurs when the available PV power is surplus than load demand along with sudden increase in load demand. In this state, Battery absorbs power from DC bus and SC provides power to DC bus to meet sudden increase in load demand. The switching modes $M10$, $M11$ and $M12$ form the complete switching sequence.

For this state, the state variables used by the displayed mathematical model are

$$x = \begin{bmatrix} i_B & i_{SC} & v_O & V_{bat} \end{bmatrix}^T; u = \begin{bmatrix} V_{SC} \end{bmatrix} \quad \text{A2.49}$$

The averaged inductor equation for the battery path is obtained from the volt-second balance as,

Applying, KVL and KCL for Mode M_{10}, we get

$$\frac{di_B}{dt} = \frac{v_O}{L_B} - \frac{V_{bat}}{L_B} \quad \text{A2.50}$$

$$\frac{di_{SC}}{dt} = \frac{-v_O}{L_{SC}} + \frac{V_{SC}}{L_{SC}} \quad \text{A2.51}$$

$$\frac{dv_{Co}}{dt} = -\frac{i_B}{C_O} + \frac{i_{SC}}{C_O} - \frac{v_O}{R_O C_O} \quad \text{A2.52}$$

$$\frac{dv_{Cb}}{dt} = \frac{i_B}{C_b} - \frac{V_{bat}}{R_B C_b} \quad \text{A2.53}$$

Therefore, the state space matrices for mode M_{10} are written as,

$$A_{10} = \begin{bmatrix} 0 & 0 & 1/L_B & -1/L_B \\ 0 & 0 & -1/L_{SC} & 0 \\ -1/C_O & 1/C_O & -1/R_O C_O & 0 \\ 1/C_b & 0 & 0 & -1/R_B C_b \end{bmatrix}; \; B_{10} = \begin{bmatrix} 0 & 1/L_{SC} & 0 & 0 \end{bmatrix}^T; \quad \text{A2.54}$$

$$C_{10} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}; \; D_{10} = \begin{bmatrix} 0 \end{bmatrix}$$

Applying, KVL and KCL for Mode M_{11}, we get

$$\frac{di_B}{dt} = \frac{v_O}{L_B} - \frac{V_{bat}}{L_B} \quad \text{A2.55}$$

$$\frac{di_{SC}}{dt} = \frac{V_{SC}}{L_{SC}} \quad \text{A2.56}$$

$$\frac{dv_{Co}}{dt} = -\frac{i_B}{C_O} - \frac{v_O}{R_O C_O} \quad \text{A2.57}$$

$$\frac{dv_{Cb}}{dt} = \frac{i_B}{C_b} - \frac{V_{bat}}{R_B C_b} \quad \text{A2.58}$$

Therefore, the state space matrices for mode M_{11} are written as,

$$A_{11}=\begin{bmatrix} 0 & 0 & 1/L_B & -1/L_B \\ 0 & 0 & 0 & 0 \\ -1/C_b & 0 & -1/R_O C_O & 0 \\ 1/C_b & 0 & 0 & -1/R_B C_b \end{bmatrix};\ B_{11}=\begin{bmatrix} 0 & 1/L_{SC} & 0 & 0 \end{bmatrix}^T;$$

$$C_{11}=\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ D_{11}=\begin{bmatrix} 0 \end{bmatrix} \quad \text{A2.59}$$

Applying, KVL and KCL for Mode M_{12}, we get

$$\frac{di_B}{dt}=\frac{-V_{bat}}{L_B} \quad \text{A2.60}$$

$$\frac{di_{SC}}{dt}=\frac{V_{SC}}{L_{SC}} \quad \text{A2.61}$$

$$\frac{dv_{Co}}{dt}=-\frac{v_O}{R_O C_O} \quad \text{A2.62}$$

$$\frac{dv_{Cb}}{dt}=\frac{i_B}{C_b}-\frac{V_{bat}}{R_B C_b} \quad \text{A2.63}$$

Therefore, the state space matrices for mode M_{12} are written as,

$$A_{12}=\begin{bmatrix} 0 & 0 & 0 & -1/L_B \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -1/R_O C_O & 0 \\ 1/C_b & 0 & 0 & -1/R_B C_b \end{bmatrix};\ B_{12}=\begin{bmatrix} 0 & 1/L_{SC} & 0 & 0 \end{bmatrix}^T; \quad \text{A2.64}$$

$$C_{12}=\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ D_{12}=\begin{bmatrix} 0 \end{bmatrix}$$

Therefore, the average state space matrices of FPDCBSS in state-IV operation can be expressed as follows:

$$A_{S4}=\begin{bmatrix} 0 & 0 & \frac{(1-d_1)}{L_B} & -\frac{1}{L_B} \\ 0 & 0 & -\frac{(1-d_2)}{L_{SC}} & 0 \\ -\frac{(1-d_1)}{C_O} & \frac{(1-d_2)}{C_O} & -\frac{1}{R_O C_O} & 0 \\ \frac{1}{C_b} & 0 & 0 & -\frac{1}{R_B C_b} \end{bmatrix}; \quad \text{A2.65}$$

$$B_{S4}=\begin{bmatrix} 0 & 1/L_{SC} & 0 & 0 \end{bmatrix}^T;\ C_{S4}=\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix};\ D_{S4}=\begin{bmatrix} 0 \end{bmatrix}$$

A.2.5 State-V and State-VI

State-V and State-VI are the steady state when the SC remains dormant. All the modes of these states are covered under above four states.

Appendix B

EXPERIMENTAL SET-UP

The experimental investigations presented in this thesis were carried out using laboratory-scale power-electronic prototypes developed for the validation of the analytical and simulation results. The experimental hardware was developed progressively according to the requirements of the different converter configurations investigated in Chapters 3, 4, 6, and 7. The experimental systems mainly consist of the power conversion stage, digital controller, gate-driver/interface circuit, input power supply, passive components, electrical load, voltage and current measurement circuits, and a mixed-signal oscilloscope.

The hardware implementation was intended to verify the practical operation of the proposed converter topologies and to compare the measured waveforms with the corresponding analytical and simulation results. Particular attention was given to the measurement of converter input current, individual phase currents, output current, output voltage, battery current, supercapacitor current, and DC-bus voltage.

The TPIBC prototypes described in Chapters 3 and 4 were implemented using three interleaved power-converter branches. The Chapter 3 prototype was implemented using IRFP260N power MOSFETs, RHRP30120 power diodes, three 560-µH branch inductors, a filter capacitor, and a LAUNCHXL-F28379D controller. The Chapter 4 prototype used K75T60A power IGBTs, RHRP30120 power diodes, three 560-µH branch inductors, a filter capacitor, a LAUNCHXL-F28379D controller, and a dedicated gate-driver circuit.

The FPDCBSS experimental system described in Chapters 6 and 7 was developed as a low-power four-port experimental prototype integrating the input source, battery, supercapacitor, and DC load. The prototype was operated using a dSPACE microlab box-based control system, ACS712 current sensors, LV25-P voltage sensors, a driver board, and electrical measurement equipment.

B.1 Electrical Power Circuit of TPIBC (Chapter 3 & Chapter 4)

The power stage, comprising power MOSFETs IRFP260N or power IGBTs K75T60A, power diodes RHRP30120, and other components, including a designed ferrite bobbin core inductor and copper wire and capacitor.

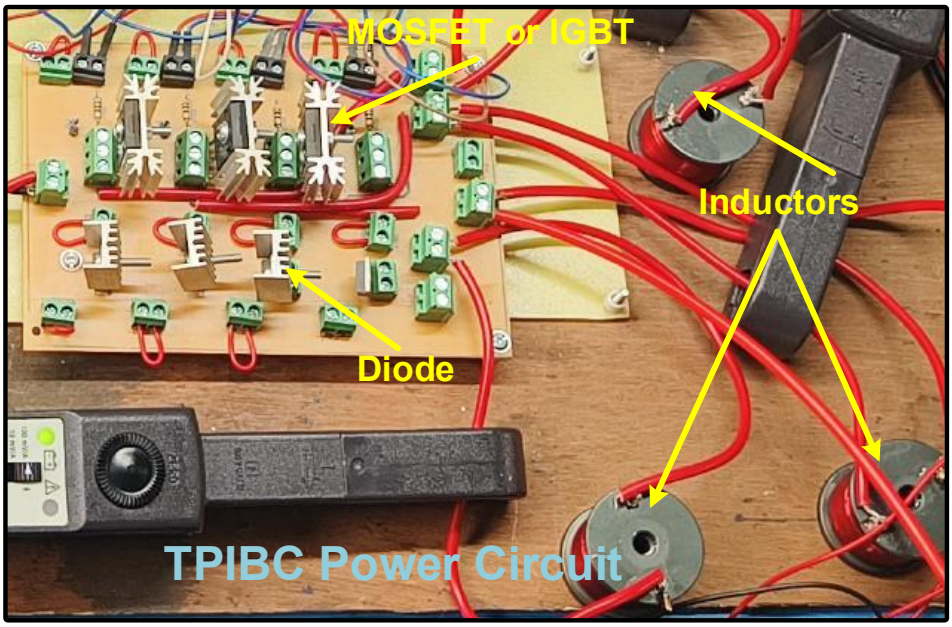
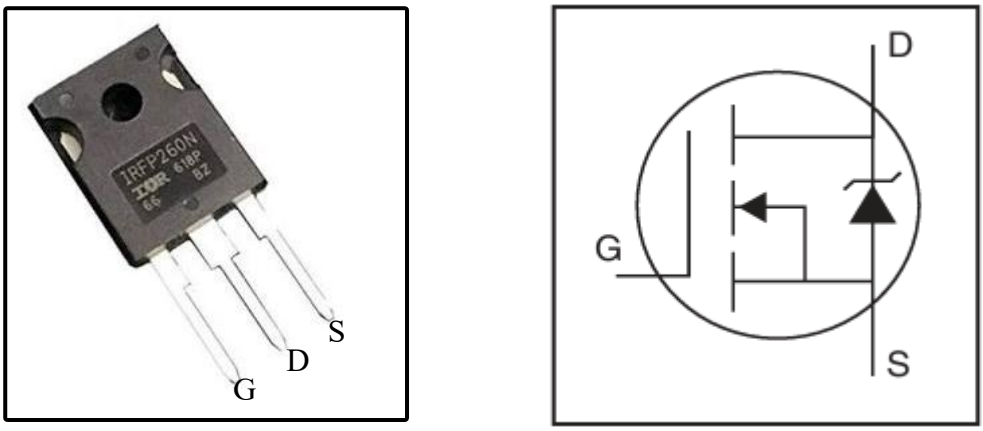


Fig. B.1 Electric Power Circuit of TPIBC.

B.1.1 POWER MOSFETs IRFP260N

The IRFP260N is an N-channel power MOSFET designed for high-current, high-voltage applications. The power MOSFET IRFP260N and circuit symbol is shown in Fig. B.2. It features a low $R_{DS}(on)$ of 0.04 Ω, allowing efficient switching with minimal heat generation. With a maximum drain-source voltage of 200 V and continuous drain current up to 50 A, it suits power supplies, motor drivers, and inverters. The device's fast switching capability reduces losses in high-frequency circuits. Its robust thermal performance, combined with a TO-247 package, ensures reliable operation under demanding conditions. Proper gate drive is essential to maximize efficiency and prevent overheating. The rating of IRFP260N switch is shown in Table B.1.



(a) (b)

Fig. B.2 (a) Power MOSFET IRFP260N (b) Circuit symbol.

TABLE B.1

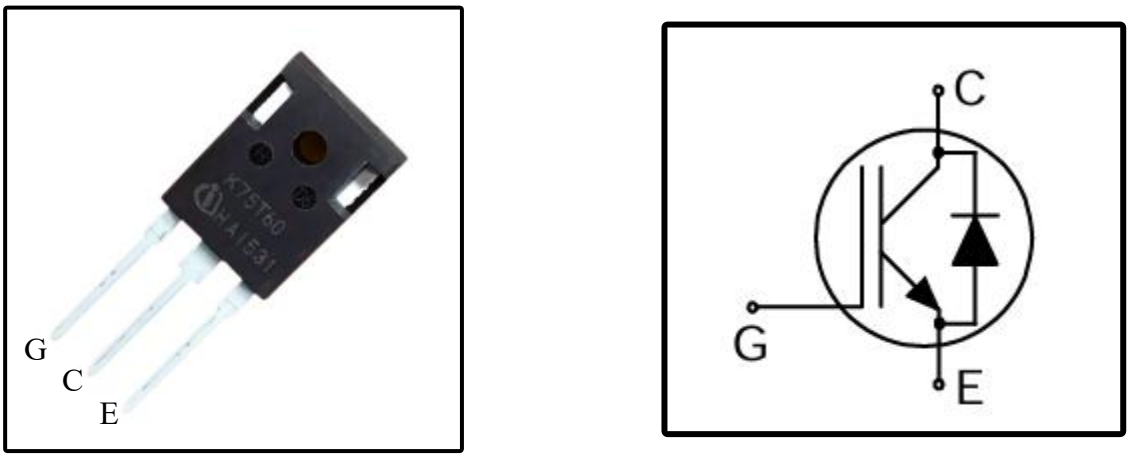
DEVICE RATINGS OF MOSFET IRFP260N SWITCHES

Parameters	Numerical Value
Continuous Drain Current, I_D (@25°C)	50 A
Pulsed Drain Current, I_{DP} (@25°C)	200A
Maximum Power Dissipation, P_{tot} max	300 W
Gate to source voltage, V_{GS}	+/- 20V
Drain-Source Voltage, V_{DS}	200 V

B.1.2 POWER IGBTs K75T60A

The K75T60 / K75T60A Datasheet is an N-channel power Insulated-Gate Bipolar Transistor (IGBT). The power IGBTs K75T60A and circuit symbol is shown in Fig. B.3. The K75T60A IGBT is a high-efficiency 600V IGBT with a 75A current rating, designed for demanding power applications. Featuring TO-247 packaging, this high-power IGBT ensures superior thermal management and low switching losses, making it ideal for solar inverters and industrial power systems. Its robust design enhances energy efficiency and

performance in solar power conversion The rating of K75T60 switch is shown in Table B.2.



(a) (b)

Fig. B.3 (a) Power IGBT K75T60 (b) Circuit symbol.

TABLE B.2

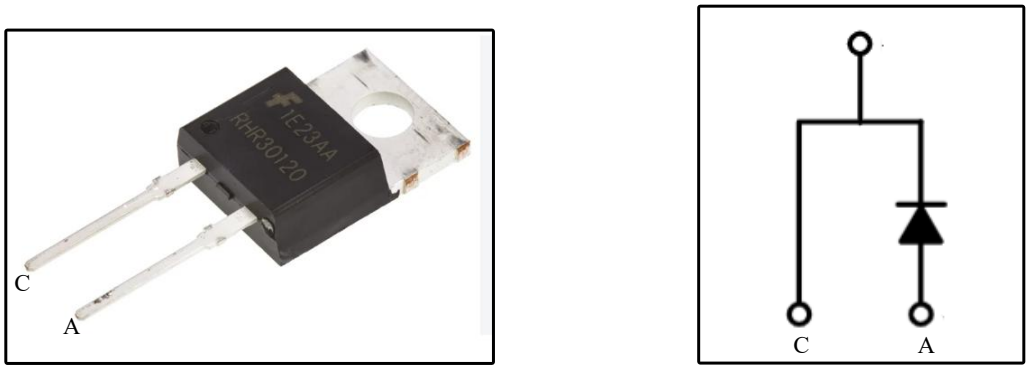
DEVICE RATINGS OF IGBT K75T60 SWITCHES

Parameters	Numerical Value
DC collector current, I_C	75 A
Pulse Collector Current, Icp	225A
Maximum Power Dissipation, P_{tot} max	428 W
Gate to Emitter voltage, V_{GE}	+/- 20V
Collector to Emitter Voltage, V_{CE}	600 V

B.1.3 POWER DIODEs RHRP30120

The RHRP30120 is a hyperfast diode with soft recovery characteristics. The power diodes RHRP30120 and circuit symbol is shown in Fig. B.4. It has the half recovery time of ultrafast diodes and is silicon nitride passivated ion implanted epitaxial planar construction. These devices are intended to be used as freewheeling/ clamping diodes and diodes in a variety of switching power supplies and other power switching applications.

Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors. The rating of RHRP30120 diode is shown in Table B.3.



(a) (b)

Fig. B.4 (a) Power Diode RHRP30120 (b) Circuit symbol.

TABLE B.3

DEVICE RATINGS OF RHRP30120 DIODE

Parameters	Numerical Value
Hyperfast Recovery, t_{rr}	85ns
Average Forward Current, I_F	30A
Max Forward Voltage, V_F	3.2V
Reverse Voltage, R_V	1200V
Maximum Power Dissipation, P_D	125W

B.2 Driver Circuit of TPIBC (Chapter 3 & Chapter 4)

The multi-channel isolated IGBT gate-driver board used to drive the power switches of TPIBC is shown in Fig. B.5. TLP350 gate-driver optocoupler is the main component of the driver board to provide optical isolation between the PWM/control circuit and the IGBT gate triggering circuit. The other components used in the driver circuit of TPIBC includes gate-emitter pull-down resistor, gate-drive supply capacitors, terminal blocks,

diodes, gate resistor, electrolytic capacitors, small ceramic/electrolytic capacitors and isolated power-supply sections.

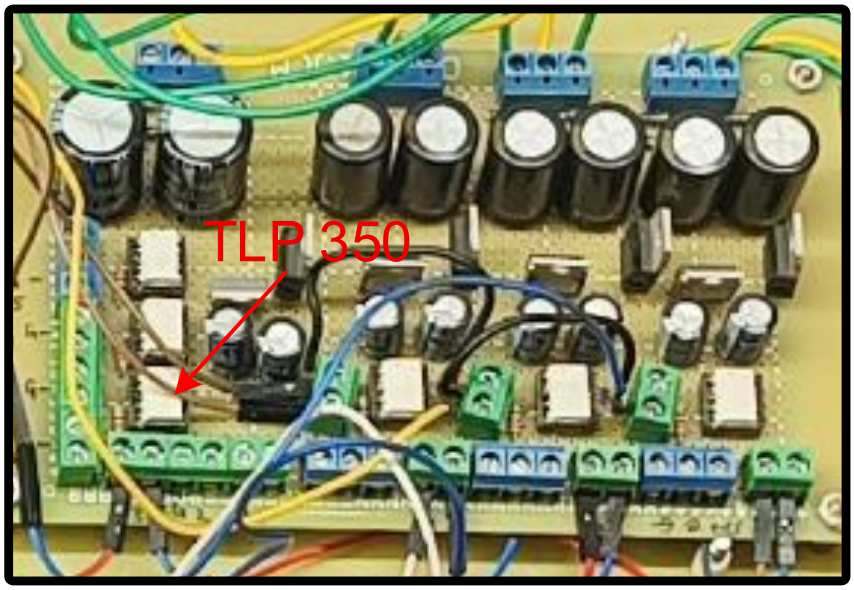


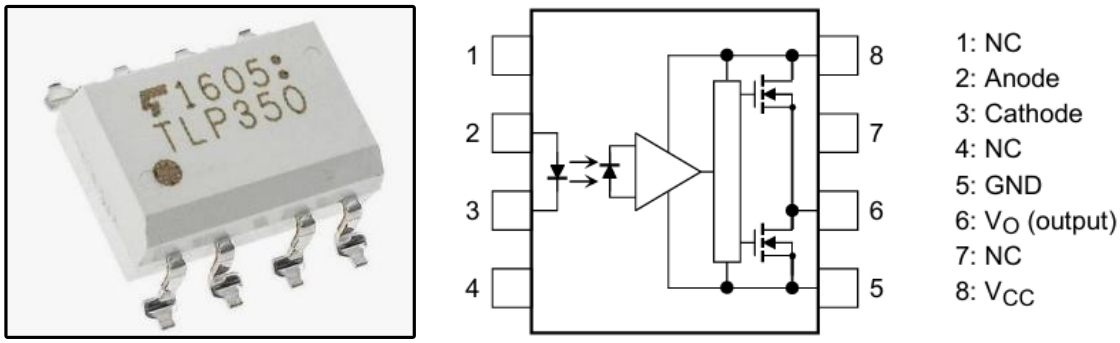
Fig. B.5 Gate driver board of TPIBC.

B.2.1 TLP 350

The TLP350 is an optically isolated gate-driver IC manufactured by Toshiba. It contains an infrared LED on the input side and a high-speed photo-IC/output stage on the isolated side. It is specifically intended for driving IGBTs and power MOSFETs.

Its basic operation can be represented as:

PWM from controller → LED input of TLP350 → optical isolation → output driver → gate of IGBT.



(a) (b)

Fig. B.6 (a) TLP 350 (b) Pin Configuration.

The TLP350 has a totem-pole output, meaning that it can actively source current to charge the IGBT gate and sink current to discharge it. Toshiba specifies a maximum peak output current of ±2.5 A, with a recommended supply range of 15–30 V. Its specified isolation voltage is 3750 Vrms, and the device has a common-mode transient immunity specification of ±15 kV/µs. The rating of TLP 350 is shown in Table B.4.

TABLE B.4

DEVICE RATINGS OF TLP 350

Parameters	Numerical Value
Peak output current, I_O	±2.0 A (max)
Guaranteed performance over temperature	−40 to 100°C
Supply current, I_{CC}	2 mA (max)
Power supply voltage, V_{CC}	15 to 30 V
Threshold input current, I_{FLH}	5 mA (max)
Switching time (tp_{LH}/tp_{HL})	500 ns (max)
Common mode transient immunity	15 kV/µs
Isolation voltage	3750 Vrms

B.3 Digital Signal Processing Board LAUNCHXL-F28379D (Chapter 3 & Chapter 4)

The digital signal processing board LAUNCHXL-F28379D is used for PWM generation to provide pulse for switches of TPIBC. The Texas Instrument LAUNCHXL-F28379D shown in Fig. B.7 described as the digital controller/PWM generation unit used to implement the converter control and generate switching pulses for the MOSFET / IGBT gate-driver circuit. The LAUNCHXL-F28379D is a development and control platform based on Texas Instruments' TMS320F28379D C2000 Delfino™ real-time microcontroller. It is designed for high-speed real-time control applications such as digital

power conversion, motor drives, renewable-energy systems, and electric-vehicle power electronics. The board provides the required computational capability, PWM generation, analog measurement interfaces, and communication peripherals for implementing the control algorithm of the proposed converter. For the experimental converter developed in this thesis, the LAUNCHXL-F28379D is particularly important because the switching signals are generated digitally using its enhanced pulse-width modulation (ePWM) peripherals. The PWM modules allow accurate control of switching frequency, duty ratio, phase displacement and dead-band, which are essential for the operation of the interleaved converter configurations investigated in this work.

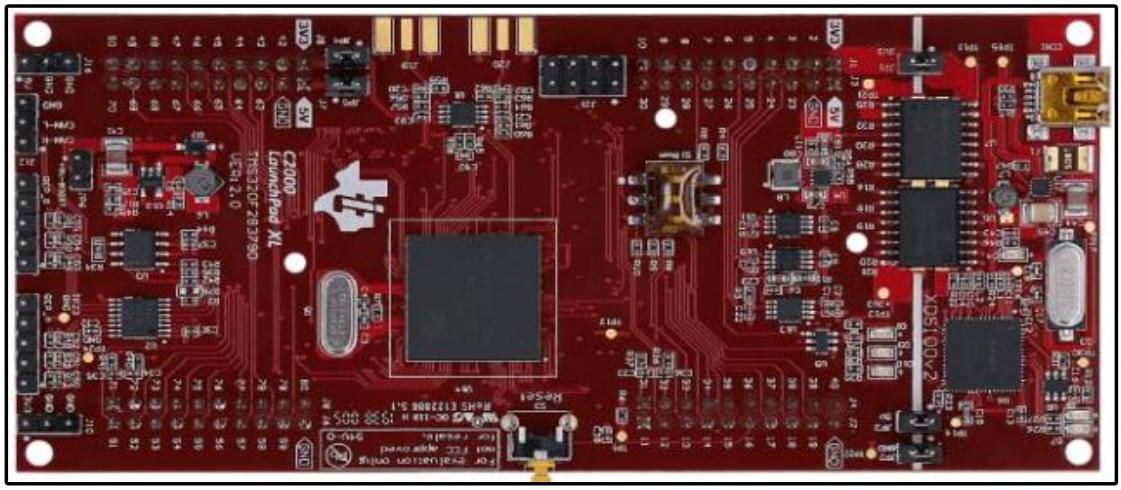


Fig. B.7 Digital signal processing board LAUNCHXL-F28379D.

B.4 Electrical Power circuit of FPDCBSS (Chapter 6 & Chapter 7)

The fabricated electrical power circuit board of the proposed FPDCBSS is shown in Fig. B.8. The board provides the power-stage interconnection for the PV source, battery, supercapacitor, and common DC-bus ports. The power circuit incorporates the required semiconductor switching devices, high-frequency diodes, inductors, capacitors, resistive components, and terminal connectors for implementing the proposed converter. The two large magnetic components visible on the right side of the board are used as the power inductive elements, for PV source and battery whereas the central inductive element and associated semiconductor devices form part of the supercapacitor power-conversion arrangement. The electrolytic capacitors provide DC-link and local energy filtering, and the mounted diodes and switching devices establish the required current paths for the

different operating modes of the FPDCBSS. Separate terminal blocks are provided for the PV, battery, supercapacitor, and load/DC-bus connections, while additional terminals are provided for voltage and current sensing. The board also includes dedicated connections for the battery and supercapacitor inductor currents, as indicated by the markings on the PCB. The fabricated board was subsequently integrated with the gate-driver and control circuits for experimental validation of the proposed FPDCBSS. The power IGBTs K75T60A, power diodes RHRP30120 is used as described in previous sections.

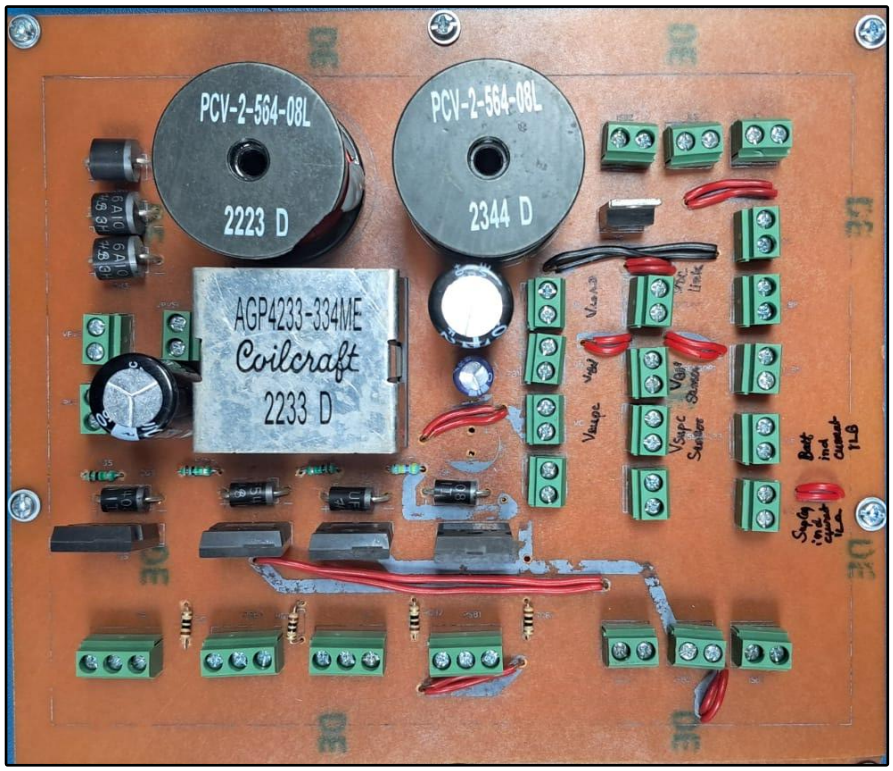


Fig. B.8 Fabricated FPDCBSS power circuit board.

B.5 Gate driver circuit for FPDCBSS (Chapter 6 & Chapter 7)

The fabricated gate driver circuit board for the proposed FPDCBSS is shown in Fig. B.9. The same TLP350 gate-driver optocoupler as described earlier is used to provide optical isolation between the PWM/control circuit and the IGBT gate triggering circuit. The other components used in the driver circuit of TPIBC includes gate-emitter pull-down resistor, gate-drive supply capacitors, terminal blocks, diodes, gate resistor, electrolytic capacitors, small ceramic/electrolytic capacitors and isolated power-supply sections.

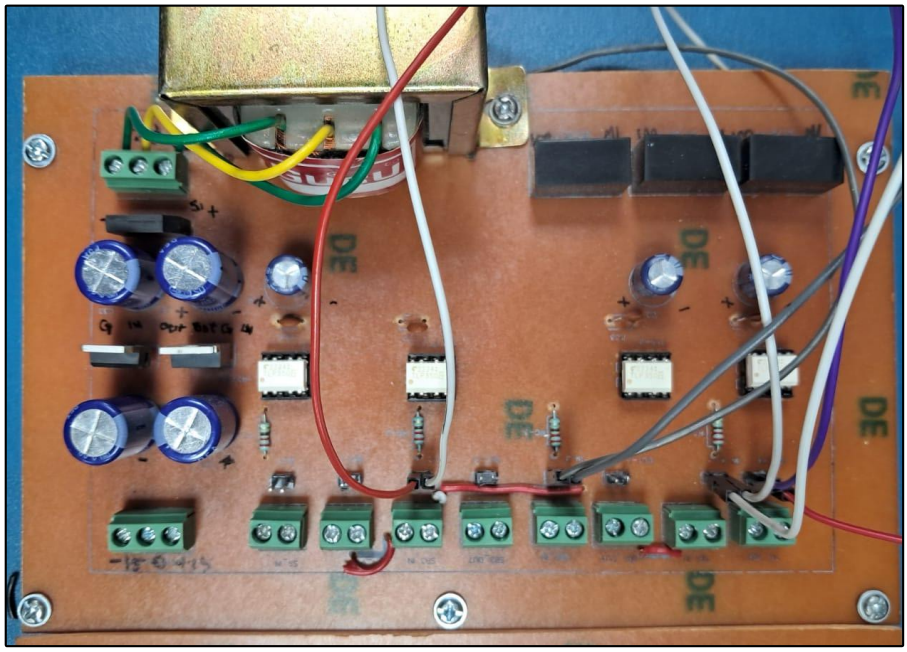


Fig. B.9 Gate driver circuit board for FPDCBSS.

B.6 Real-Time Digital Control(Chapter 6 & Chapter 7)

The FPDCBSS control system has been implemented using a dSPACE MicroLab Box based control system. The controller receives the measured voltage through LV25-P voltage transducer and measured current through ACS712 Hall Effect sensors feedback signals and generates the switching commands required for the converter. The basic control path is measurement of parameters followed by the digital control algorithm and PWM generation. This arrangement allows the control algorithm developed in Chapters 6 and 7 to be implemented in real time.

B.6.1 dSPACE MicroLab Box

The dSPACE MicroLabBox shown in Fig. B.10 is a compact real-time control and rapid-prototyping platform used for the development, testing, and experimental validation of power-electronic control systems. In the proposed experimental setup, it can be used as the real-time control unit for the FPDCBSS, where measured voltage and current signals are acquired from the power circuit and processed in real time to generate the required switching signals. . The measured signals from the voltage and current sensors are supplied to the analog input channels of the MicroLab Box. These signals are processed by the control algorithm implemented using MATLAB/Simulink and dSPACE Control

Desk. Based on the measured DC-bus voltage, battery current, supercapacitor current, and other feedback variables, the controller determines the required duty ratios or control commands for the converter switches.

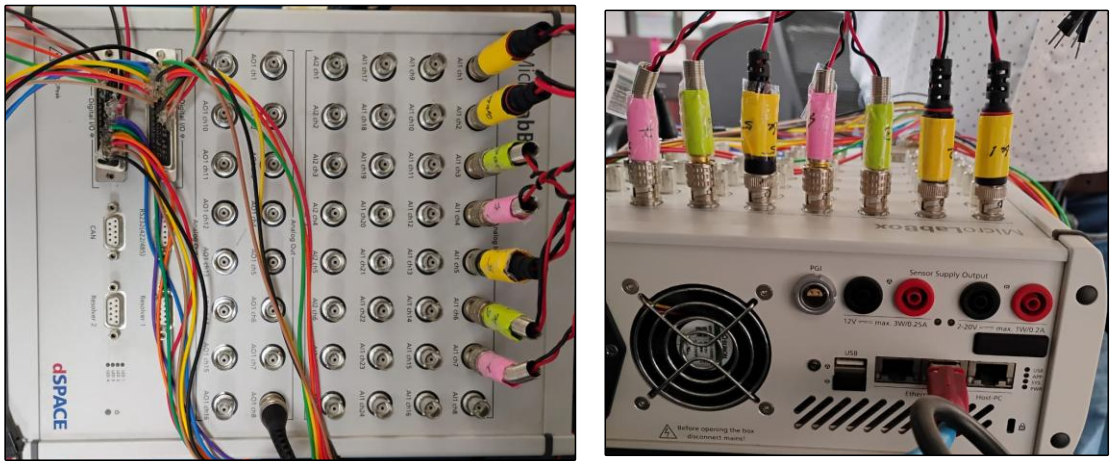
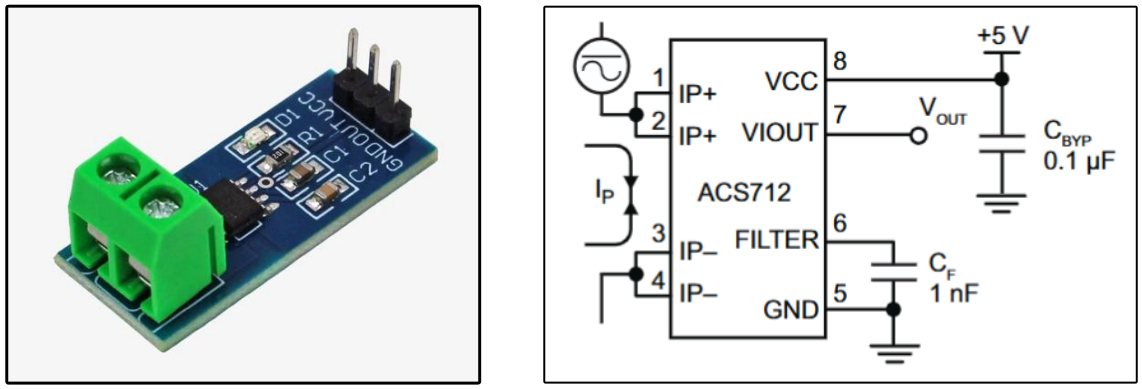


Fig. B.10 dSPACE MicroLab Box.

B.6.2 ACS712 Current Sensor

The ACS712 is a popular, Hall-effect-based linear current sensor IC (and breakout module) shown in Fig. B.11 designed for measuring both AC and DC currents while providing galvanic isolation between the load path and the logic controller. The operating principle for operating ACS712 is current passing through the internal copper conduction path generates a magnetic field. The integrated Hall IC converts this magnetic field into a proportional analog voltage. The rating of ACS712 Hall Effect current sensor is shown in Table B.5.



(a) (b)

Fig. B.11 (a) ACS712 Hall effect current sensor (b) PIN configuration.

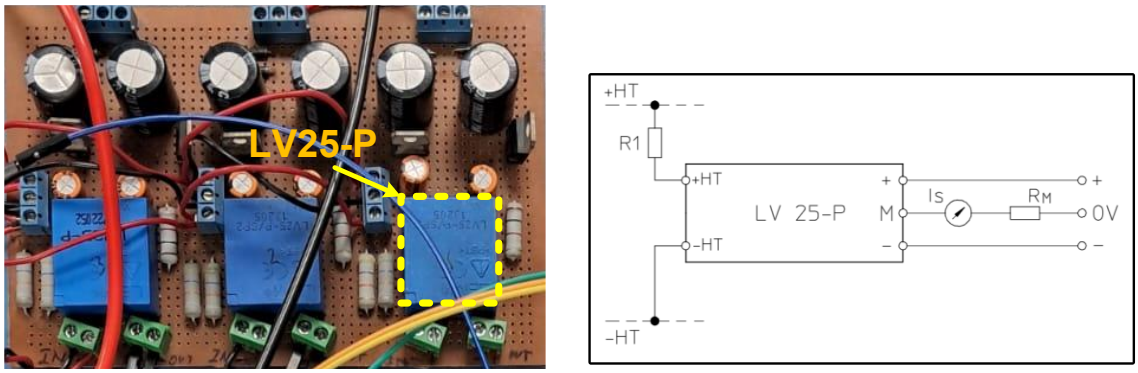
TABLE B.5

DEVICE RATINGS OF ACS712 CURRENT SENSOR

Parameters	Numerical Value
Supply Voltage, V_{CC}	5 V
Supply Current, I_{CC}	8 mA
Output Zener Clamp Voltage, V_Z	8.3 V
Output Resistance, R_{OUT}	1 Ω
Primary Conductance Resistance, R_{PRI}	1.2 mΩ
Output Capacitance Load, C_{LOAD}	10 nF
Output Resistive Load, R_{LOAD}	4.7kΩ

B.6.2 LV 25-P voltage sensors

The custom-designed PCB shown in Fig. B.12 serves as a multi-channel signal conditioning and isolation interface based on LEM LV25-P Hall-effect closed-loop voltage transducers. It is configured to measure high DC or AC voltages while maintaining galvanic isolation between the primary high-voltage side and the secondary low-voltage measurement system (e.g., microcontroller/DSP ADCs). The rating of LV25-P voltage sensor is shown in Table B.6.



(a) (b)

Fig. B.12 (a) LV25-P Hall effect voltage sensors (b) Connection diagram

TABLE B.6

DEVICE RATINGS OF LV25-P VOLTAGE SENSOR

Parameters	**Numerical Value**
Primary nominal RMS current, I_{PN}	10 mA
Primary current, measuring range, I_P	0 to ± 14 mA
Secondary nominal RMS current, I_{SN}	25 mA
Current consumption, I_C	10+I_S mA
Supply voltage, V_C	± 12 to 15 V

List of Publications

Following are the publications in journals and conferences out of this research work.

❖ Publications in National/International Journals

[1] **Kumar, N.,** Kumar, M., "Modeling and characterization of *n*-phase interleaved buck converter with circuit parasitic for battery charging applications," *Electrical Engineering*, vol. 107, pp. 5329–5339 (2025). https://doi.org/10.1007/s00202-024-02347-2.

[2] **Kumar, N.,** Kumar, M., "Impact of Operating Duty on Performance of IBC under Different Operating Regions with Ripple Characterization," IETE Journal of Research, vol. 72(4), pp. 1051–1066 (2026). https://doi.org/10.1080/03772063.2025.2593533.

Under Review:

N. Kumar, M. Kumar, "Control-oriented modeling of four-port dc-dc converter for battery-supercapacitor-based system," *IEEE Transactions on Transportation Electrification*.

Patent:

System and Method for Managing Power Flow in a Hybrid Energy Storage System, *Indian Patent*, Application Filed Number: **202611089328.**

❖ Publications in National/International Conferences

[1] **N. Kumar** and M. Kumar, "Characterization of Two-phase Interleaved Buck Converter with Circuit Parasitic," IEEE Delhi Section Conference (DELCON), New Delhi, India, pp. 1-6, 2022. doi: 10.1109/DELCON54057.2022.9753235.

[2] **N. Kumar** and M. Kumar, "Multiport Interleaved Resonant DC-DC Converter for Off-Board Electric Vehicle Charging Application," IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Jaipur, India, pp. 1-6, 2022. doi: 10.1109/PEDES56012.2022.10079998.

[3] **N. Kumar** and M. Kumar, "Three-Phase Interleaved Bidirectional Resonant Converter for Charging / Discharging Infrastructure," IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Mangalore, India, pp. 1-6, 2024. doi: 10.1109/PEDES61459.2024.10961831.

CURRICULUM VITAE

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PROFESSIONAL PROFILE

Electrical engineering professional with experience in power systems and research, currently serving as Assistant Manager (Technical) at Delhi Transco Limited, a Government of NCT of Delhi undertaking. Research interests include renewable-energy-based DC microgrids, interleaved DC–DC converters, battery–supercapacitor hybrid energy storage, converter modelling, control, stability, and EV charging applications.

PROFESSIONAL QUALIFICATIONS

The author has received the B.Tech degree in Electrical Engineering from West Bengal University of Technology (WBUT), Kolkata, India in the year 2013 with CGPA 8.74 and the M.Tech degree in Power and Energy Systems from National Institute of Technology Karnataka (NITK), Surathkal, Mangalore, India in the year 2017 with CGPA 7.32. He is a doctoral student in the Department of Electrical Engineering, Delhi Technological Unveristy (DTU), Delhi, India and carried out the research reported in the thesis under the supervision of Dr. Mayank Kumar. Assistant Professor, Department of Electrical Engineering, DTU.

PROFESSIONAL EXPERIENCE

- Assistant Manager (Technical), Delhi Transco Limited (DTL), Government of NCT of Delhi Undertaking — currently serving.
- Professional and research exposure in electrical power systems, power electronics, renewable-energy integration, energy storage, and EV charging systems.

RESEARCH & TECHNICAL INTERESTS

- Interleaved DC–DC converters; battery charging/discharging; converter modelling and small-signal analysis.
- Battery–supercapacitor hybrid energy storage systems; multiport converters; robust control and stability analysis.
- Renewable-energy-based DC microgrids, distributed generation, EV charging infrastructure, and power management.

RESEARCH ACHIEVEMENTS

- Qualified GATE in 2015 and 2017.
- Selected for the Commendable Research Award, Delhi Technological University (DTU), for a published research article in the Springer Electrical Engineering.