DESIGN AND ANALYSIS OF LOW POWER SRAM BIT CELL FOR CONTENT ADDRESSABLE MEMORY APPLICATION

A Thesis Submitted

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By

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CANDIDATE'S DECLARATION

I, **Yogita Chopra** (**Roll No. 2K20/PHDEC/04)**, hereby certify that the work which is being presented in the thesis entitled "**Design and Analysis of Low Power SRAM Bit Cell for Content Addressable Application**", in partial fulfilment of the requirements for the award of the Degree of **Doctor of Philosophy**, submitted in the Department of **Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **25th August 2020** to **06th October 2026** under the supervision of **Prof. Poornima Mittal, Professor, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.



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This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.



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CERTIFICATE BY THE SUPERVISOR

Certified that **Yogita Chopra** **(2K20/PHDEC/04**) has carried out their search work presented in this thesis entitled **"Design and Analysis of Low Power SRAM Bit cell for Content Addressable Memory Application",** for the award of **Doctor of Philosophy** from Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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ABSTRACT

The continuous scaling of CMOS technology and the developing data-intensive computing systems have largely increased the requirements of high-speed, low power and process variation tolerant memory architectures for modern Very Large Scale Integration (VLSI) systems. Static Random Access Memory (SRAM) still remains one of the most important parts of modern digital systems due to its wide application in cache memories, embedded processor, artificial intelligence (AI) accelerator, networking hardware, Internet-of-Things (IoT) devices and high-performance computing platform. However, aggressive CMOS scaling at the nanoscale has adversely impacted the reliability and stability of traditional SRAM architectures. Scaling down of transistor dimensions results in degradation of static noise margin (SNM), increase in leakage current, threshold voltage fluctuation, half-select disturbance, read upset probability, process-voltage-temperature (PVT) variation sensitivity and writability. These problems become more severe in near-threshold and sub-threshold operating conditions where the lowered supply voltage degrades the memory stability and operational reliability. As a result, conventional 6T SRAM cells are not capable of meeting the aggressive low power and stability requirements of today's nanoscale designs. This has given rise to new SRAM topologies with improved read isolation, writability and leakage characteristics.

Simultaneously, the growing demand for high-speed associative search operations has driven fast adoption of Content Addressable Memory (CAM) and Ternary Content Addressable Memory (TCAM) architectures in packet forwarding engines, cybersecurity hardware, machine learning accelerators, database systems, networking routers, and edge-AI processors. Instead of retrieving information by physical addresses as in traditional memories, CAM and TCAM architectures perform massively parallel associative search operations by comparing the search data in parallel with all the stored memory words. TCAM architectures also support ternary search states such as logic ‘0’, logic ‘1’, and “don’t care” conditions, allowing flexible masked search and pattern matching operations. Though TCAM architectures offer very high search throughput, they are inherently prone to excessive dynamic power dissipation resulting from large search-line switching activity, match-line precharging, and parallel comparison operations across the entire memory array. Moreover, large TCAM arrays suffer from considerable leakage current, sensing delay, match-line

instability, thermal reliability degradation and process variation sensitivity that limit their scalability and energy efficiency in advanced technology nodes.

To address these challenges, this research proposes the design, analysis and implementation of advanced low power SRAM architectures and SRAM based TCAM arrays for nanoscale CMOS technologies. The proposed work focuses on the development of stable and low voltage 8T, 9T and 11T SRAM cells and their integration into optimized TCAM blocks and hybrid associative memory architectures. The influence of transistor topology, isolated read/write operation, single-ended sensing technique, dual-port architecture and heterogeneous cell integration on the performance indices of SRAM and TCAM such as static noise margin, leakage power, access delay, power-delay product, variation tolerance and associative search efficiency are systematically investigated.

In this research, high performance low power 9T and 11T SRAM design is presented using 32nm CMOS technology to improve stability, reduce leakage power and guarantee reliable operation at low voltage. The proposed 9T SRAM cell overcomes the destructive read disturbance and enhances the memory robustness at a 0.9 V supply voltage using isolated read/write paths and optimized transistor sizing. The architecture has achieved about 0.368 V, 0.364 V and 0.422 V read SNM, hold SNM and write margin values, respectively, with almost 4.5 ns and 1.2 ns read and write access times while maintaining low leakage power consumption of about 22.1 nW. To improve sub-threshold reliability further, an ultra-low-voltage 11T SRAM architecture operating at 500 mV with integrated read/write assist circuitry, isolated sensing operation, and improved storage-node protection mechanisms is developed. The proposed 11T SRAM cell shows read SNM, hold SNM and write SNM around 184mV, 197.26mV and 265mV respectively, with fast read and write access times of about 11.38ps and 16.24ps. Process-corner analysis, temperature variation studies and 5000-sample Monte Carlo simulations are used to verify the robustness of the proposed architectures against the threshold voltage fluctuation, transistor mismatch and environmental variations. The developed SRAM cells show high operational stability, low power dissipation and better applicability for low power edge computing, aerospace electronics and energy-constrained embedded systems.

Additionally, an 8T SRAM single-ended architecture is proposed for ultra-low power and low voltage operation. The proposed architecture reduces the switching activity and leakage current by using isolated read operation, optimized access transistor configuration and single-ended sensing methodology. The proposed 8T SRAM cell in 32 nm CMOS technology works

reliably at an ultra-low supply voltage of 400 mV. The design achieves a hold SNM of about 178 mV and a read SNM of about 181 mV, with a write margin of about 204 mV. Process-corner simulations and temperature variation analyses show excellent thermal stability and low sensitivity to environmental variations. The isolated read path effectively prevents read upset conditions and improves operational stability at ultra-low voltages. Moreover, the proposed architecture has much less standby power consumption and much lower dynamic energy dissipation, which makes it very suitable for battery-operated and IoT-oriented systems.

The SRAM-based TCAM blocks are designed with optimized memory structures and efficient match-line evaluation techniques to exploit the developed SRAM architectures for associative memory applications. The proposed TCAM architectures employ isolated sensing operation and low-power comparison circuits to reduce search-line switching activity and dynamic search energy consumption. To reduce bit-line capacitance and suppress unwanted switching transitions during search operations, single-ended SRAM operation is employed . The proposed TCAM blocks show significant improvement in search efficiency, power dissipation and sensing delay as compared to the existing SRAM based CAM architectures with 7T, 9T, 10T and 11T SRAM cells. The proposed TCAM architecture achieves picosecond range search delays with significant reduction in average power dissipation. The optimized search-line organization and the efficient match-line discharge mechanisms are effective to reduce the power consumption of matching and mismatching. The proposed structures further improve the search stability by reducing the voltage fluctuation of the storage nodes and alleviating the search-induced read disturbance.

The another contribution of this work is the design of a hybrid alternate SRAM-TCAM array architecture using heterogeneous 8T and 9T SRAM cells in the same associative memory framework. Unlike the classical homogeneous SRAM arrays where the same memory cell is used throughout the array, the proposed architecture strategically mixes alternate rows of single-port 8T SRAM cells and dual-port 9T SRAM cells to take advantage of both topologies at the same time. The proposed alternate organization allows a significant reduction of the static and dynamic power dissipation with respect to arrays of exclusively composed of dual port SRAM structures. The hybrid architecture provides static and dynamic power consumptions of about 0.29 µW and 23 µW, respectively, with improved search reliability and reduced leakage current. The architecture also minimizes search-line capacitance, enhances stability under voltage scaling, and achieves an optimal trade-off

among power consumption, area overhead and search performance. Extensive comparative studies are presented to show that the proposed SRAM and TCAM architectures offer significant improvements in static noise margin, leakage reduction, process variation tolerance, dynamic power dissipation, associative search reliability and the operating speed with respect to the previously reported memory structures. The proposed architectures are robust towards temperature variations, process-corner variations and low-voltage operating conditions and therefore they can be used for deeply scaled nanoscale technologies. Moreover, the developed SRAM-TCAM systems provide an efficient platform of future associative computing and in-memory processing applications such as AI accelerators, edge-AI processors, secure networking systems, packet classification hardware, image processing systems, and low-power embedded computing platforms. In summary, the proposed low-power 8T, 9T and 11T SRAM architectures integrated in optimized SRAM-based TCAM arrays show large improvements in low-voltage operation, leakage suppression, associative search efficiency and process variation tolerance. The proposed hybrid SRAM–TCAM architecture provides a scalable and robust memory solution for next-generation intelligent computing systems working under stringent power and reliability constraints.

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List of Abbreviations/Symbols

Symbol/Abbreviation	Full Form
6T	6 Transistor
8TP	8 Transistor proposed
9PT PS	8 Transistor proposed parallel processing
11TP	Proposed 11T
ACL	Access control lists
BCAM	Binary content addressable memory
BER	Bit error rate
BL	Bit line
BLB	Bit line bar
CAM	Content addressable memory
CIM	Compute in memory
CMOS	Complementary metal oxide semiconductor
CNTFET	Carbon nano tube field effect transistor
CSR	Control signal read
D^2AP	Differential data aware power supplied
DL	Data line
DRAM	Dynamic random access memory
DRV	Data retention voltage
EQM	Electric quality metric
ER-TCAM	Error resilient- Ternary content addressable memory
FinFET	Fin-Field effect transistor
FPGA	Field programmable gate array
HSNM	Hold static noise margin
IoT	Internet of things
LPM	Longest prefix matching
LSB	Least significant bit
MAC	Media access control
ML	Match line
MNU	Multi-node upsets

MSB	Most significant bit
MHSCPF-CAM	Modified hybrid self-controlled pre-charge free CAM
NMOS	N-metal oxide semiconductor
PDP	Power delay product
PDR	Pull down right
PMOS	P-metal oxide semiconductor
PTM	Predictive technology model
PUL	Pull up left
PVT	Process, voltage and temperature
RBL	Read bit line
RSNM	Read static noise margin
RWL	Read word line
SINM	Static current noise margin
SL	Search line
SNM	Static noise margin
SoC	System on chip
SRAM	Static random access memory
SVNM	Static voltage noise margin
TCAM	Ternary content addressable memory
TFET	Tunnel field effect transistor
TG	Transmission gate
ULSI	Ultra large scale integration
VN-TFET	Vertical nanowire tunnel field effect transistor
VS-CNTFET	carbon nano tube field effect transistor
VTC	Voltage transfer characteristics
WBL	Write bit line
WL	Word line
WM	Write margin
WTI	Write trip current
WTP	Write trip power
WTV	Write trip voltage
WWL	Write word line
µW	Microwatt

C_{BL}	Bit line capacitance
C_{RL}	Read line capacitance
Fj	Femtojoule
FS	Fast-fast
FS	Fast-slow
GND	Ground
kB	Kilo byte
mA	Mili ampere
MHz	Mega hertz
mV	Mili volt
mW	Mili watt
nA	Nano ampere
Nm	Nano meter
nS	Nano second
nW	Nano watt
pA	Pico ampere
P_{dyn}	Dynamic power
pS	Pico-second
R_{PD}	Pull down resistor
SF	Slow-fast
SS	Slow-slow
V	Voltage
V_{DD}	Voltage at the drain
V_{DDmin}	Minimum required voltage at the drain
Vss	Voltage at source
V_{TH}	Threshold-voltage
Mn	Electron-mobility
Mp	Hole-mobility

CHAPTER – 1
INTRODUCTION

1.1 OVERVIEW OF THE CHAPTER

In this chapter, operational principles and architectural evolution of Static Random Access Memory (SRAM), Content Addressable Memory (CAM) and Ternary Content Addressable Memory (TCAM) for low power, high speed and process variation resilient nanoscale memory design are presented. This chapter covers topics on on-chip SRAM storage, CAM/TCAM associative search and memory organization, and array level functionality in advanced VLSI systems [1]. The single-ended and differential SRAM architectures are investigated and compared in terms of sensing operation, leakage reduction, stability improvement, low voltage operation and process variation tolerance. In addition, SRAM cell topologies are studied from conventional 6T to advanced 11T structures with respect to read/write stability, power consumption, area efficiency and robustness [2].

Furthermore, in this chapter, an overview of the search-line activation, parallel comparison, match-line sensing and precharge-discharge evaluation mechanisms for SRAM-based Binary CAM (BCAM) and Ternary CAM (TCAM) architectures. It also represents recent advances in low-power TCAM search techniques, adaptive and reconfigurable architectures, in-memory computing techniques and AI-oriented associative memory systems [3]. Additionally, a brief literature survey of various SRAM, CAM, and TCAM-based architectures is presented to identify design limitations, performance trade-offs, and research gaps leading to the formulation of the proposed hybrid SRAM–TCAM framework.

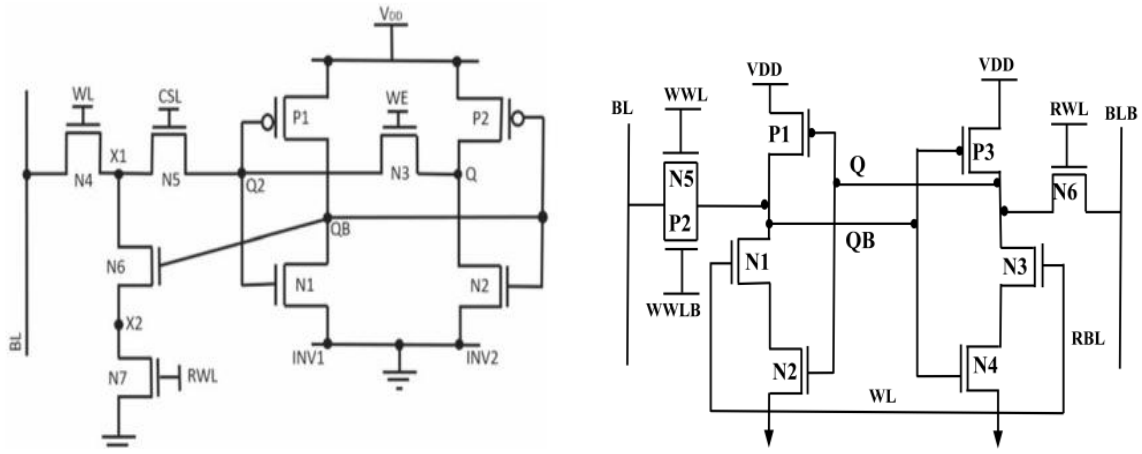
This chapter is structured as follows: the basics of SRAM, CAM and TCAM architectures and the organization of the chapter are described in the section 1.1 of the chapter. The single-ended and differential SRAM structures and comparative study of SRAM cell topologies are represented in section 1.2. SRAM based BCAM and TCAM architectures, associative search mechanisms and TCAM array operations are illustrated in section 1.3. The recent research trends and reported low power TCAM techniques are illustrated in section 1.4. The evolution of SRAM based TCAM array is represented in section 1.5 and section 1.6 emphases of low power operations of TCAM arrays. The problem statements are identified and are represented in section 1.7. Furthermore, in section 1.8 of the chapter, a brief review is represented and research gaps are identified on the bases of the literature review in section 1.9. In Section

1.10, the research objectives and in section 1.11 the proposed methodologies are discussed which includes the circuit level modelling, simulation strategy, stability analysis and power-performance evaluation. Finally, the overall thesis organization and chapter wise contributions of the proposed research work is represented in section 1.12 of this chapter.

1.2 DIFFERENTIAL AND SINGLE-ENDED SRAM TOPOLOGIES

Static Random Access Memory (SRAM) cells are one of the most important memory components in modern digital integrated circuits, especially in cache memories, register files and embedded on-chip storage units because of their fast access speed, low latency and compatibility with CMOS fabrication technology [4]. The bistable circuit of the SRAM cell, which is made up of two cross-coupled inverters, stores the binary data, thus the stored information is maintained as long as the power supply is on and no periodic refresh operations are required. The SRAM arrays are usually organized in word lines (WLs) and bit lines (BLs) which provide the read and write access mechanisms of the stored data. SRAM architectures can be designed as single port, dual port or multi-port based on functional requirements. Single-port SRAM cells use the same access paths for both read and write operations, which reduces the complexity of the circuit and the silicon area, but results in lower operational stability and robustness [5]. On the other hand, dual-port and multi-port SRAM architectures employ extra access transistors to enable concurrent memory transactions, which results in increased throughput and accessibility at the expense of larger area overhead, parasitic capacitance, and leakage power dissipation [6] as illustrated in Figures 1.1 (a) and (b).

The SRAM sensing architectures are generally classified into differential-ended and single-ended schemes according to the data detection method [7]. Conventional 6T SRAM cells typically use differential bit lines, BL and $\overline{BL}$, and sense data by a small voltage difference developed between the complementary lines. This differential sensing technique provides improved noise immunity, higher sensing reliability and better tolerance to process variations, leading to faster and more stable read operation. However, the dynamic power consumption is strongly influenced by the bit-line capacitances that are charged to the supply voltage before each access cycle [8]. Single-ended SRAM architecture using only one bit line in the read/write operation is proposed to solve this problem. The single-ended SRAM design reduces the switching activity and the bit-line charging requirements, thereby improving the dynamic power dissipation and the energy efficiency [9].



(a) (b)

Fig. 1.1. Schematic representation of (a) Single-ended, and (b) Differential ended 9T SRAM cell.

While single-ended SRAM architectures can reduce switching activity and dynamic power consumption, they are generally more sensitive to noise, read disturbance and degraded sensing margins, making circuit-level optimization essential for reliable operation [10, 11]. The continuous technology scaling towards deep-submicron dimensions and near-threshold voltage operation brings several critical low-power and reliability challenges in SRAM design. Leakage power has become the main concern in standby due to the increased subthreshold conduction and gate leakage currents, especially in large-scale memory arrays [12]. Moreover the dynamic power dissipation is still large. The bit lines with a large capacitance are charged and discharged frequently and thus the power consumption is still considerable when accessing the memory.

Another challenge related to voltage scaling is the static noise margin (SNM) degradation which negatively impacts the cell stability and increases the probability of read and write failures [13]. In addition, the variations in the fabrication process, particularly in threshold voltage, degrade the performance of SRAM by causing mismatch in the cross-coupled inverter pairs. Mismatches have a detrimental effect on the stability, reliability, and yield of the memory system, particularly at nanoscale technology nodes [14].

Typical methods are voltage scaling with assist circuits such as word-line under drive and bit-line boosting techniques to enhance write ability and read stability under scaled supply voltages. Power gating techniques are also applied to reduce leakage and to minimize standby power during idle times. Moreover, multi-threshold CMOS (multi-V_t) design techniques are often employed to efficiently balance the speed and leakage power, whereas adaptive body biasing is used to compensate for process-induced variations [15]. Beyond these techniques,

researchers have proposed advanced SRAM bit-cell architectures such as single-ended SRAM cells, read-decoupled structures, and assist-based memory topologies to enhance power efficiency, stability and robustness in nanoscale memory applications [16].

1.3 DIFFERENT SRAM ARCHITECTURES

Modern digital systems widely use Static Random Access Memory (SRAM) technology, because it offers high speed operation, low access latency and compatibility with CMOS technology. Binary information is stored in SRAM by means of bistable latch structures consisting of cross-coupled inverters and access transistors [18]. Unlike Dynamic Random Access Memory (DRAM), SRAM is not plagued by periodic refresh operations and is therefore well suited for cache memories, embedded processors, networking systems and high performance computing applications [19]. The conventional SRAM architectures are mainly based on six-transistor (6T) architectures [1], which include two pull-up transistors, two pull-down transistors and two access transistors [20]. However, the continued scaling of CMOS technology has resulted in serious challenges such as reduced static noise margin (SNM), increased leakage current, process variability, half-select disturbance, and degraded read/write stability at low-voltage operation [21].

To overcome these limitations, advanced SRAM cell architectures such as 7T, 8T, 9T, 10T and 11T cells have been proposed by incorporating isolated read/write paths, extra control transistors, assist circuitry and single-ended sensing mechanisms [22]. These architectures improve read stability, leakage suppression, writability and variation tolerance, while enabling reliable operation in near-threshold and sub-threshold regions [23]. Single-ended SRAM cells have the advantage of significantly reducing the switching and dynamic power dissipation. Differential SRAM structures improve sensing reliability and robustness of operation [24]. In addition, emerging SRAM architectures can also implement advanced functionalities, such as in-memory computing, associative search operation, and AI acceleration, turning SRAM arrays into a multifunctional computational memory platform, instead of just a conventional storage unit [25].

The standard 6T SRAM cell offers small area and high speed operation. However its performance suffers in low voltage conditions, leading to low read stability, poor write ability, and high process variation sensitivity [26]. To overcome these challenges various architectures of advanced SRAM cells like 7T, 8T, 9T, 10T and so on with higher transistor count are developed [27]. Schematics of different SRAM cells starting from 6T to 11T is

shown in figure 1.2 (a-f). These architectures add transistors to improve read isolation, static noise margin, and reduce leakage power, thus enabling robust operation at ultra-low supply voltages [28]. Especially the use of decoupled read/write paths and assist techniques in higher order SRAM cells significantly improve stability and robustness [29]. The most common SRAM cells are;

The traditional 6T SRAM cell is one of the most commonly used and area efficient memory cell architectures in modern integrated circuits [1]. It is built using six transistors: two PMOS pull-up transistors, two NMOS pull-down transistors and two NMOS access transistors in a cross-coupled inverter configuration as shown in Figure 1.2(a). The main advantage of the 6T topology is its small structure and high density of integration, which is very suitable for cache memories and embedded memory applications.

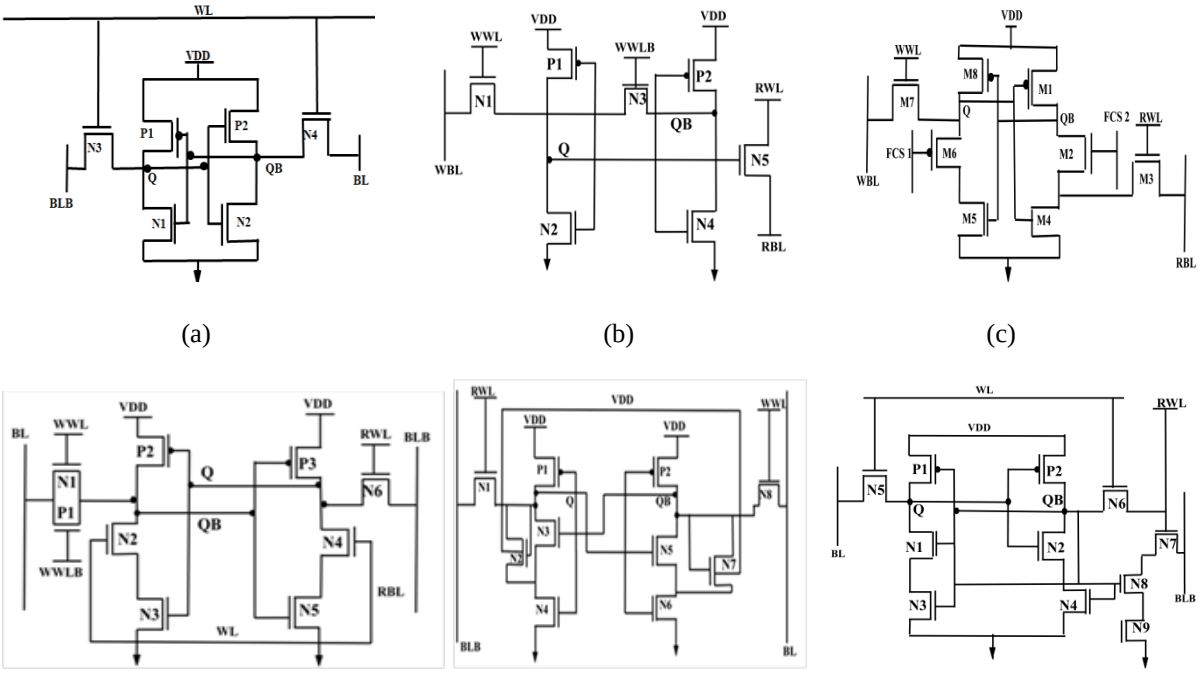


Fig. 1.2. SRAM bit cells with different transistor count; (a) 6T, (b) 7T, (c) 8T, (d) 9T, (e) 10T, and (f) 11T.

During read operation of the cell, internal storage node is strictly linked with the precharged bit line via the access transistor [30]. This interaction can result in a voltage division between the pull-down transistor and the access transistor, which can lead to an unintentional rise of the stored node voltage [31]. This disturbance is more severe at lower supply voltages and may cause accidental flipping of stored data, reducing the read stability and the overall reliability of the SRAM cell [32].

The inherent stability problems of the traditional SRAM cells have led to the creation of several improved SRAM topologies that aim to separate the read and write operations and to improve the overall robustness [33]. One such improvement is the 7T SRAM cell that adds an extra transistor in either the feedback path or the access circuitry to provide partial isolation during read operation. The modification improves read stability at relatively low area overhead as compared to more complex architectures [34]. The schematic structure of 7T SRAM cell is shown in Fig. 1.2 (b). Further improvement is achieved in the 8T SRAM cell by adding additional transistors to form an independent read port. This read-decoupled configuration decouples the storage nodes from the read bit line during read access, which alleviates the read disturbance issues and significantly improves the Read Static Noise Margin (RSNM) [35].

The SRAM cell constituted using 8-transistors shows a major advancement with respect to the conventional 6T architecture by offering a completely isolated read path. Two dedicated transistors are used only for the read functionality; additionally it is also occupied with a separate write access transistor and two conventional inverter pairs [36]. The read operation does not directly access the internal storage nodes, thus, effectively eliminating the possibility of read-induced data corruption. This architecture significantly improves the read stability and ensures reliable operation at low supply voltage and near-threshold conditions [2]. In addition, the separated read paths allows independent optimization of read and write operations which increases the tolerance against process variations and improves the cell reliability [4]. However, the extra transistors increase the silicon area and other leakage paths which need optimized transistor sizing and leakage reduction methods to work efficiently.

The 9-Transistors SRAM cell has the advantages of the 8T architecture as well as an additional transistor in the read circuitry, which is typically a buffered or gated read path [5]. This additional transistor increases the isolation between the storage nodes and the read bit line and reduces the leakage current owing to the stacking effect of the transistors. [37] The buffered read mechanism reduces voltage disturbances during sensing operations and increases read reliability in environments with low voltage and high process variation. Due to its increased robustness and better immunity to soft errors, the 9T SRAM cell is often used in applications that require high reliability, such as aerospace and radiation tolerant systems. However, the increased number of transistors leads to an increased area occupancy and more complex control circuitry, which makes a trade-off between memory density and stability performance [38].

The 10-Transitors SRAM cell enhances SRAM reliability further by offering fully isolated read paths with improved write assist techniques. Differential or pseudo-differential sensing schemes are usually achieved by additional transistors and controlled write access mechanisms, providing better read/write margins [9]. The 10T topology completely isolates read and write operations, enabling aggressive voltage scaling with minimal degradation in stability, making it ideal for ultra-low power and near-threshold computing applications. In addition, the architecture supports assist techniques such as bit-line boosting and word-line modulation to improve the write ability under reduced supply voltage [39]. The 10T SRAM cell has improved Static Noise Margin (SNM), better process variation tolerance and less read disturbance, but these advantages are at the cost of increased layout complexity, increased area and parasitic capacitances.

The 11T is an advanced SRAM architecture designed for ultra-robust and low-leakage operation for deeply scaled technologies. With the addition of one more transistor to the 10T structure, the cell further enhances the read buffering, leakage control and writes operation management. Many 11T SRAMs employ stacking transistors and differential sensing in the read path to reduce leakage current drastically and improve immunity to noise and process variations [11]. The enhanced isolation mechanisms also reduce the susceptibility to soft errors and improve the data retention capability in low voltage operation. However, the 11T SRAM cells generally possess larger area overhead and a more complex design. Thus, the 11T SRAM cell is mainly used for niche applications where stability, reliability, and low-power operation are more relevant than memory density [40].

1.4 BCAM AND TCAM CELL DESIGNS USING SRAM CELLS

Content Addressable Memory (CAM) is special memory architecture for high speed parallel search operation. Unlike conventional SRAM in which a particular memory address is used to read data [41], CAM searches data by simultaneously comparing the input search word with all the entries stored in the memory array. Based on the type of information stored, CAM is generally classified into Binary CAM (BCAM) and Ternary CAM (TCAM). BCAM contains only binary values ‘0’ and ‘1’, while TCAM adds one more “don’t care” state “X” for masked searching and flexible pattern matching operations. CAM and TCAM structures are used in networking routers, packet forwarding, data compression, image processing, artificial intelligence hardware and high speed lookup systems because of their parallel associative search capability [42].

The TCAM architecture is commonly implemented with SRAM based storage cells, comparison logic and match-line sensing circuits. During the search operation the incoming search data is simultaneously compared with each stored word in the memory array and the corresponding match line indicates the presence of a match condition [43]. The TCAM provides very fast search capability, but the operation of search lines simultaneously with precharge-discharge activity on match lines results in high power consumption [44]. As technology scales further into deep submicron regime, additional design challenges such as leakage current, sensing delay, process variations and search reliability become more critical for TCAM design. Therefore, recent research works have focused on low power SRAM based TCAM architectures by using advanced SRAM topologies such as 8T, 9T and 11T cell for reducing search energy, improving stability and enhancing reliability for energy efficient associative computing applications [45].

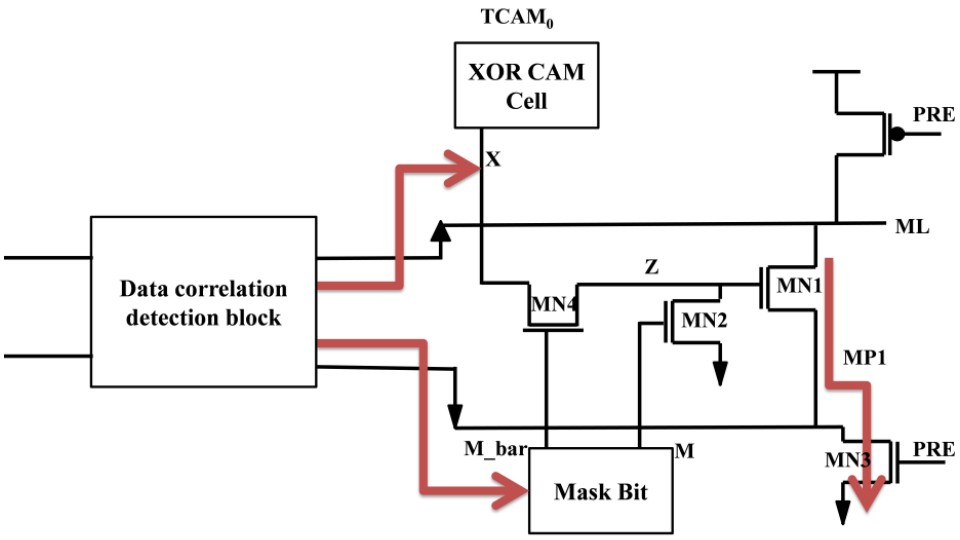


Fig. 1.3. Basic architecture workflow for CAM

With increasing transistor count of SRAM cells, better separation between read and write paths can be achieved resulting in improved noise margins, enhanced stability and easier implementation of assist techniques for low voltage operation [46]. However, these improvements are obtained at the expense of penalties in terms of silicon area, circuit complexity and overall power overhead. Hence, SRAM cells with higher number of transistors provide better resilience and reliability but may not be suitable for general purpose memory systems where area efficiency and density are important requirements [47]. The basic operation flow of a CAM block is shown in Fig. 1.3. Therefore, the present work deals with the low-power SRAM cell topologies, since these architectures offer a good trade-off

among stability, power dissipation, operational speed and implementation suitability for deeply scaled nanoscale integrated systems [48]. Several associative memory structures are realized at the circuit level with SRAM-based bitcells, especially Binary Content Addressable Memory (BCAM) and Ternary Content Addressable Memory (TCAM) [49].

In the conventional SRAM, the data is stored in a pair of cross-coupled CMOS inverters and is accessed by transistors controlled by the word line (WL) with the complementary bit lines (BL/$\overline{BL}$). At its heart, SRAM is an address-oriented memory, but its powerful bistable storage mechanism, rapid access capability, and excellent scalability with modern CMOS processes make it very suitable for incorporation into content-addressable architectures [50]. In the adaptation of CAM implementation, the electrical characteristics of the internal storing nodes are of vital importance. It is because the parameters such as read stability, static noise margin, write accessibility have significant impact on search accuracy, delay performance and overall energy consumption in the parallel associative matching operations [51]. Representation of matching and mismatching in a CAM block is shown in Fig. 1.4.

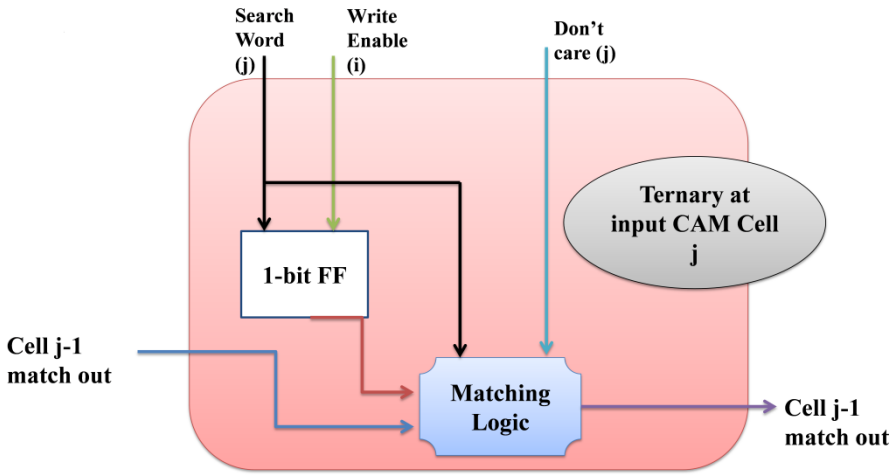


Fig. 1.4. Representation of matching and mismatching in a CAM block

Content Addressable Memory (CAM) can be realized as a variant of the SRAM bitcell with additional comparison logic to compare directly the stored data with the externally given search inputs. The comparison operation of the BCAM is typically realized with XOR/XNOR- and NAND/NOR-based match circuits coupled to a common match line (ML).

1.5 EVALUATION DYNAMICS FOR TCAM ARRAYS

The ML is initially pre-charged to a high state before the search phase begins. For evaluation, the stored data bit is simultaneously compared with the incoming search line (SL) value. If all compared bits fulfill the matching condition, the ML remains in its pre-charged state, while

any mismatch results in an ML discharge. In this way the ML does the collective logical evaluation on all bits of a word. The parasitic capacitance and discharge characteristics of the ML connected to multiple cells strongly affect the search delay and the dynamic power consumption of the CAM array. BCAM can perform high speed parallel searches, but it only supports exact binary comparison between logic '0' and logic '1'. It is not suitable for applications that require masking or wildcard-based matching operations.

BCAM is enhanced by adding a third logic state called "don't care" or 'X' to enable flexible ternary matching operations, and is called Ternary Content Addressable Memory (TCAM). This feature is usually accomplished by adding extra storage and control circuitry to the SRAM-based cell structure so that the comparison can ignore certain bit positions. The XNOR-type matching logic is usually used to compare the data and mask information with the TCAM operation in two evaluation paths. If a stored bit is programmed to "X" then the comparison circuitry associated with that bit position will inhibit the effect of that position on the match line result regardless of the search input applied. The ternary functionality provides much more flexibility in searching and pattern matching, but also increases circuit complexity due to the larger number of transistors per cell. The additional mask control circuitry and comparison devices will lead to higher power dissipation due to increased switching activity on the search and match lines. Moreover, the sensing of match line of large scale TCAM arrays is more sensitive to process variation; leakage currents and voltage fluctuation, since a large number of cells are connected to a common ML node, which affects the sensing accuracy and the stability of the whole array. Basic CAM structure for searching operations is shown in Fig. 1.5.

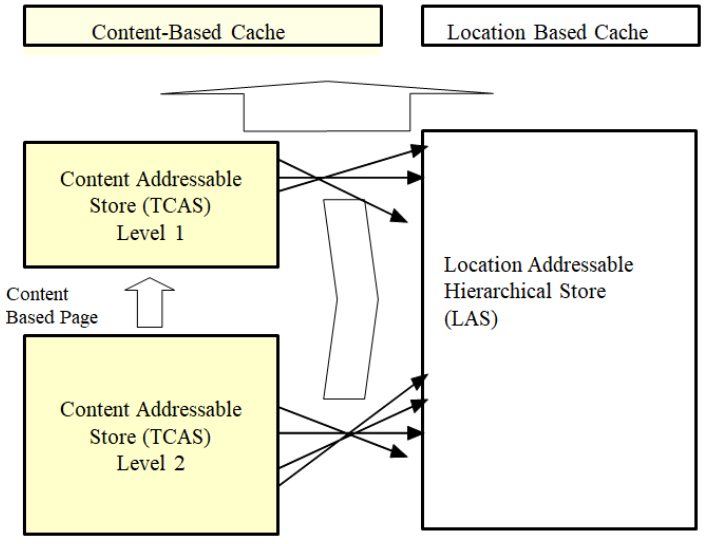


Fig. 1.5. Basic CAM structure for searching operations

The ML is initially pre-charged to a high state before the search phase begins. For evaluation, the stored data bit is simultaneously compared with the incoming search line (SL) value. If all compared bits fulfil the matching condition, the ML remains in its pre-charged state, while any mismatch results in an ML discharge. In this way the ML does the collective logical evaluation on all bits of a word. The parasitic capacitance and discharge characteristics of the ML connected to multiple cells strongly affect the search delay and the dynamic power consumption of the CAM array. BCAM can perform high speed parallel searches, but it only supports exact binary comparison between logic '0' and logic '1'. It is not suitable for applications that require masking or wildcard-based matching operations.

1.6 SRAM-BASED TCAM ARRAYS OPTIMISED FOR LOW POWER OPERATIONS

At circuit level, SRAM-based TCAM architectures with 8T-11T bitcell configurations provide better isolation of the storage nodes and the comparison circuitry. Such structural separation is very useful to reduce read-disturb effects and to avoid corruption of the stored data during match-line (ML) evaluation. These architectures generally use the dedicated read path for comparison operations, where the stored logic value and the applied search line (SL) input interact to activate the ML discharge network. By increasing the transistor counts in the advanced 9T, 10T and 11T cells, there are more design flexibilities to implement techniques such as conditional evaluation, gated switching and transistor stacking. These techniques are especially effective in reducing subthreshold leakage and gate leakage currents, which in turn ensures ML reliability and improves search accuracy in large fan-in TCAM arrays.

From the sensing perspective, with the increasing of the array dimensions, reliable ML detection becomes more and more difficult. The larger arrays have higher parasitic capacitance, lower voltage swing, and accumulated leakage currents from inactive cells connected to the same ML, which degrades sensing margins and delays performance. To cope with these challenges, a variety of sensing techniques such as low-swing ML sensing, current mode sensing and hierarchical sensing architectures are widely utilized. Such techniques speed-up evaluations and increase sensing robustness, while reducing dynamic power consumption by minimizing unnecessary voltage transitions on highly capacitive nodes. Furthermore, selective precharge strategies are often utilized such that only some specific MLs are activated based on previous search activity or intermediate filtering stages, thus substantially decreasing switching energy. The performance of the sense amplifier is

also very important, since it must be able to differentiate correctly between match and mismatch conditions even when the signal levels are degraded due to process, voltage, and temperature (PVT) variations.

When long match lines are broken up into smaller segmented sections, there is a significant reduction in effective capacitance and the propagation delay of the discharge at the array-interconnect level, which results in improvements in search speed as well as energy efficiency. Usually, the segmented structures are used in conjunction with local match evaluation circuits and higher level aggregation logic to retain scalability without compromising search correctness. Similarly, search line power consumption can be reduced by using reduced voltage swing operation or conditional activation schemes that avoid unnecessary transitions. In addition, the array level leakage performance is typically optimized by using dual-threshold or multi-threshold CMOS technologies, where high-threshold-voltage devices are used in leakage sensitive non-critical paths and low-threshold-voltage transistors are used for timing critical sections for high speed operation.

1.7 PROBLEM STATEMENT

The demand for portable and high processing capability devices in low area has resulted in designers incorporating System on Chip (SoC) with Internet of Things (IoT) and machine learning [2]. The increasing popularity of Internet of Things [8] has increased the load of processing using microprocessors present on System on Chip. Also, devices with SoC integrated with Artificial Intelligence and Machine Learning makes the devices more desirable and reliable. The external peripheral circuitry of an SRAM bit cell mainly comprises bit line, sense amplifiers and decoders. Processors are required for the faster execution Applications. SRAM bit cell consists of various processors and each processor depends on the cache memory present internally. The new advancement in the industry can be towards nanometer technology feature size in the aspect of sleek designs with larger battery life to take care of larger needs of the consumer. In addition to this the feature size of highly integrated Nano electronic devices is gradually reduced in line with Moore's law nanotechnology.

- Aggressive CMOS technology scaling coupled with constant supply voltage reduction for power minimization leads to significant degradation in stability, read/write margins and variability tolerance in conventional 6T SRAM bit cells. Thus they are not suitable for

ultra-low voltage cache memory applications. This necessitates the design of new SRAM bit cell topologies capable of reliable operation at voltage levels near and below threshold.

- Traditional TCAM implementations are not suitable for high-density, power-constrained applications such as network routers, packet classification engines and edge-AI accelerators due to their reliance on high-power and area-intensive memory cells. Therefore, it is necessary to design small, low-power SRAM-based TCAMs with fast search speed, low energy consumption and better scalability.
- The integration of SRAM cells into TCAM systems causes issues such as match-line leakage, lowered noise margins, increased delay and compromised search reliability under low-voltage operation. To achieve strong search functionality, high density and low energy consumption per search operation, it is important to develop efficient SRAM-based TCAM cells and peripheral circuits.
- As technology node keeps shrinking, corner variations, leakage currents and device mismatches severely reduce the robustness of SRAM cells, leading to higher failure rates in large memory arrays. Therefore, it is still an important research challenge to develop energy-efficient and variation-tolerant SRAM cells with better noise margins and lower leakage power.
- It effectively reduces dynamic and leakage power. However, reducing the supply voltage in dense SRAM arrays aggravates the read disturb, half-select disturbance, and write failure problems. Hence, there is a pressing need to investigate and develop SRAM bit cells with functional reliability and reduced transistor count and silicon area overhead.

Although CAM can search the whole content required by the device in a single clock cycle [18], a very high speed searching application is not feasible by the existing memory functions. But that has a number of drawbacks. Therefore, the design of a content addressable memory using SRAM cell for search operation is required [20]. The SRAM Cell array is required for the industry requirements like data storage embedded applications, cache memories, microprocessors and application specific integrated circuits [21]. There are major requirements to design SRAM cell arrays which can accommodate associative memory search applications to meet the requirements of associative memory functions [22].

1.8 BRIEF LITERATURE REVIEW

The literature review on advanced SRAM, CAM and TCAM architectures has provided a strong technical base for the proposed research, which is the design of a low-power hybrid

SRAM-TCAM array using heterogeneous 8T, 9T, and 11T SRAM cells. The reviewed works collectively show that traditional memory architectures are no longer sufficient to meet the stringent requirements of modern nanoscale computing systems, especially under aggressive voltage scaling and high density integration conditions [8]. The survey clearly showed that although conventional 6T SRAM cells provide compact area efficiency, they suffer from severe read disturbance, poor writability, degraded static noise margin (SNM) and excessive leakage power sub-threshold and near-threshold operating regions. These limitations are becoming more significant in applications such as edge-AI, associative computing, aerospace electronics, and IoT devices, where the need for ultra-low-power and reliable memory functionality is simultaneous [12].

One of the most significant insights obtained from the literature survey is the critical role of isolated read and write paths in enhancing SRAM stability and energy-efficiency [22]. Several works on 8T and 9T SRAM cells have demonstrated that separating the read operation from the internal storage nodes significantly improves the read SNM and suppresses destructive read disturbance. In particular, the reviewed 8T architectures based on differential sensing, dynamic feedback control and transmission-gate-based access mechanisms showed significant improvements in low-voltage operation and tolerance to variations. The proposed research was greatly influenced by these observations, which established the importance of isolated sensing mechanisms and selective single-ended operation in developing a stable and low power hybrid TCAM array. The literature also pointed out that the single-ended SRAM structures are attractive in terms of bitline switching activity and dynamic power dissipation reduction, thus, they are highly attractive for energy-constrained applications. Thus, the presented work integrates the advantages of both differential and single-ended architectures to deliver improved search reliability and reduced switching energy in the hybrid TCAM framework.

The literature survey also highlighted the significance of leakage power as a dominant limitation in nanoscale SRAM and TCAM arrays. Several reported studies have shown that the standby leakage current increases significantly with technology scaling due to the reduction of the threshold voltage and the increase of the sub-threshold conduction. This challenge was tackled for advanced 9T SRAM architectures using stacked transistors, isolated read paths and leakage-aware transistor sizing. Similarly, CAM and TCAM studies indicated that match-line precharge circuitry and search-line switching activity contribute heavily toward overall power dissipation. This work was motivated by these results to

address the reduction in both standby leakage and dynamic search energy by optimized hybrid SRAM-TCAM architectures. The proposed hybrid configuration of 8T, 9T and 11T SRAM cells is hence designed to take advantage of the leakage-efficient characteristic of single-ended 9T structures while maintaining the high stability features of 8T and 11T topologies.

The literature review has also been of pivotal importance in understanding the sensitivity of the process-voltage-temperature (PVT) variation in advanced memory systems. Many reviewed papers indicated that process variations significantly affect SRAM stability, especially in deeply scaled CMOS technologies at low supply voltages. In addition, soft-error resilience and multi-node upset tolerance were highlighted in radiation-hardened SRAM designs for aerospace applications. These studies led to the inclusion of strong stability-enhancement strategies in the proposed research. The integrated stability benefits of several SRAM topologies in a single associative memory architecture is expected to provide better immunity to process variations, transient disturbances and soft errors for the hybrid TCAM array proposed in this work.

Another important finding from the literature survey was the increasing importance of computing-in-memory (CIM) and associative computing paradigms. Several recent works have shown that SRAM cells are not limited to conventional storage applications anymore, but are increasingly finding use in logic execution, dot-product computation, neural network acceleration, and associative search operations. The examined CAM and TCAM architectures also highlighted the importance of high-speed parallel search ability for AI acceleration, secure communication, and high-performance networking systems. However, the existing TCAM structures still suffer from excessive search-line power consumption, large sensing overhead and poor scalability. Such limitations directly motivated the current research towards the development of a hybrid SRAM-based TCAM array, able to achieve low-power associative search, while maintaining high operational reliability and improved scalability.

The literature survey also found that no one SRAM architecture offers the best trade-off between power consumption, stability, search speed, area efficiency and computational capability. 8T SRAM cells are known to have good read stability and decent half-select disturbance immunity but typically incur area overhead. Similarly, 9T SRAM architectures offer better leakage reduction and writability improvement, but may suffer from higher design complexity and sensing issues. On the other hand, 11T SRAM structures allow logic-in-memory and associative computing functionality but at the cost of increased number of

transistors and capacitance. This comparative understanding was one of the strongest motivations behind the proposed hybrid SRAM-TCAM architecture. Rather than choosing a single SRAM topology, the present work explores the use of different 8T, 9T and 11T SRAM cells in the same TCAM array, in order to exploit the unique advantages of all the architectures and to minimise their respective disadvantages.

The reviewed literature also greatly influenced the methodological direction of the research, highlighting the importance of evaluating the performance of SRAM and TCAM using parameters such as read SNM, write ability, dynamic energy & power, leakage immunity, search delay, process variation tolerance and half-select stability. Further, many studies have shown the importance of operating SRAM arrays in the sub-threshold and near-threshold supply voltages for ultra-low-power applications. Therefore, the motivation of the proposed work is to design and analyse a hybrid TCAM array which can work stably at lower supply voltages and reduce leakage current and search-line energy dissipation.

In addition, the survey pointed out the increasing importance of SRAM-TCAM architectures for emerging applications such as AI accelerators, edge computing, aerospace electronics, secure communication systems, and IoT-enabled smart devices. Application domains such as these require memory architectures that can simultaneously provide high-speed associative search, low energy consumption, compact area utilisation, and strong resilience to environmental and process-induced disturbances. Existing designs generally optimise only a subset of these requirements. Hence, the motivation of the proposed research is to develop a unified hybrid SRAM-TCAM framework which is capable of balancing power efficiency, search reliability, operational stability, and computational capability in a scalable nanoscale memory architecture.

In summary, the literature review was crucial in determining the technical shortcomings of current SRAM and TCAM designs while uncovering promising design strategies for future low-power associative memory systems. The cumulative results of previous work have motivated the proposed work for development of optimised 8T, 9T and 11T SRAM cells in hybrid TCAM array architecture. The detailed literature review of the work is detailed in depth under the chapter 2; here a brief review is represented on basis of which the following research gaps are identified which is given in the next section below.

1.9 RESEARCH GAPS

Static Random Access Memory (SRAM), Content Addressable Memory (CAM) and Ternary Content Addressable Memory (TCAM) architectures are the fundamental building blocks for high speed and low power associative computing systems in advanced nano scale VLSI applications. The SRAM architecture is widely used in cache memories and embedded systems due to its high operating speed and compatibility with CMOS technologies. CAM and TCAM allow parallel search operations for networking, pattern matching and AI-oriented data processing. The growing demand for energy efficient and process variation tolerant memory architectures has further motivated the development of optimized SRAM and TCAM based designs with enhanced stability, reduced leakage power and improved search efficiency.

For conventional SRAM architectures, the deep submicron scaling causes read/write stability degradation, leakage current degradation and low voltage operation limitation. To overcome these limitations, advanced SRAM topologies of 6T to 11T structures with decoupled read paths, improved noise margins and high process variation immunity have been proposed. Single-ended and differential SRAM design are comparatively studied in terms of sensing reliability, power dissipation, area overhead and robustness. These architectural modifications are directly related to the goal of designing stable and low-power memory structures for nanoscale and near-threshold operation.

SRAM-based Binary CAM (BCAM) and Ternary CAM (TCAM) architectures provide efficient associative search functionality based on parallel comparison mechanisms and match-line evaluation techniques. TCAM arrays realize high-speed data matching with reduced search latency by using search-line activation, precharge-discharge operation and match-line sensing. To reduce the dynamic power consumption and improve the scalability, recent research has been done on low-power search schemes, adaptive TCAM architectures, in-memory processing, and AI-assisted associative memory systems. These developments provide the foundation for the proposed hybrid SRAM–TCAM architecture for energy-efficient and high-performance search operations.

A schemed survey of SRAM, CAM and TCAM based architectures reported in literature exposes the limitations of leakage power, sensing instability, process variation sensitivity and array level energy overhead. In view of these observations, the main research objective is formulated towards development of low-power, stable and process variation aware hybrid SRAM–TCAM structures with improved search efficiency and reduced power dissipation. The adopted methodology includes circuit-level modelling, performance evaluation by

simulation, stability analysis and TCAM array integration to validate the proposed architecture under nanoscale operating conditions.

1.10 RESEARCH OBJECTIVES

On the basis of literature review of single port, dual port SRAM cells and SRAM based TCAM architectures a few major research gaps were identified. On the basis of identified research gaps, the following four objectives are formulated:

Objective 1:

To design and analyse a low power dual-port SRAM bit cell for low voltage operations.

Objective 2:

To design and assess a single-port symmetrical low voltage operating SRAM bit cell.

Objective 3:

To design and compare a content addressable memory (CAM) using single-port and dual-port SRAM bit cells.

Objective 4:

To configure higher order array for Binary-CAM/Ternary-CAM/SRAM.

To attain these objectives, the systematic methodologies are followed, encompassing both analytical and experimental perspective. The methodologies are aligned with the overall goal of this work so that the objectives can be effectively addressed and assessed.

1.11 METHODOLOGY FOR OBJECTIVES

The following methodologies are followed to attain the formulated objectives:

Methodology for Objective 1

- Different SRAM bit-cell architectures reported earlier with different number of transistors are studied in detail to understand the circuit level techniques used for low power operation, low voltage operation, leakage reduction, read/write stability improvement and process variation tolerance.
- All the SRAM cells are simulated and reanalysed in the same technology and operating conditions to evaluate their electrical characteristics and performance metrics. The effect of transistor count scaling on the stability, power dissipation, delay, and area overhead is analysed in a systematic way.

- The performance analysis obtained is utilized to design optimized low power and low voltage 9T and 11T SRAM bit-cell architectures with improved read stability, leakage current reduction and enhanced write capability with reliable near-threshold operation for nanoscale memory applications.
- The proposed 9T and 11T SRAM bit cells are comparatively analysed with the existing SRAM architectures in terms of static noise margin (SNM), power consumption, delay, leakage current and process variation robustness to prove the effectiveness of the proposed designs.

Methodology for Objective 2

- The effects of single-port configurations on stability, power dissipation, sensing reliability and low-voltage operation are evaluated by comparison with previously reported single-ended SRAM architectures.
- A systematic analysis of the circuit-level techniques employed in existing single-ended SRAM cells for leakage reduction, read stability enhancement, and improved write functionality is simulated and analysed.
- Based on the literature analysis, design a low-power single port 8T single-ended SRAM bit cell with better read isolation, lower leakage current and improved low-voltage stability characteristics.
- The proposed 8T SRAM bit cell is analysed for static noise margin, power consumption, delay and overall stability under different operating conditions.

Methodology for Objective 3

- The integration of SRAM bit cells in large scale memory arrays is studied to evaluate the effect of inter-cell interaction, array organization and peripheral circuitry on overall stability, power consumption and search performance.
- The existing SRAM array architectures and TCAM array organizations reported in the literature are systematically studied to understand their structural configurations, search methodologies and array-level optimization techniques.
- A critical review of the circuit and architectural techniques adopted for improving match-line sensing, search efficiency, leakage reduction and energy-aware array operation for high-performance associative memory applications.

- Based on the array-level analysis, an 8T SRAM-based TCAM block is designed and evaluated for low-power associative search operation with improved stability, reduced search energy, and efficient match-line evaluation characteristics.

Methodology for Objective 4

- A comprehensive study of higher order SRAM and TCAM array architectures reported in the literature is conducted to study the array organization, scalability, search efficiency and array level performance optimization techniques.
- Systematic evaluation of the architectural and circuit-level techniques to improve the stability, reduce the search power, improve the match-line sensing, and optimize the associative search performance
- The implementation of SRAM arrays for CAM-like associative search applications, focusing on the functional requirements, search mechanisms and performance impact of memory-centric parallel comparison operations is critically investigated.
- On the basis of the obtained analysis, a higher-order application-specific TCAM array architecture is designed to realize an efficient associative search operation with improved energy efficiency, scalability and array-level stability.

1.12 THESIS ORGANIZATION

The complete thesis is arranged in seven chapters. Chapter 1 discusses the introduction where the importance of SRAM cell, its array and TCAM variations are discussed. Afterwards, Chapter 2 provides the literature survey of the research work. Moreover, from Chapter 3 to Chapter 6 all the objective will be discussed in details. Eventually, Chapter 7 is dedicated to the conclusion and future scope. A brief overview of contents of each chapter is outlined as follows -

Chapter 1: Introduction

In this chapter, the excitement about the importance of SRAM cell, its array and TCAM variations is highlighted. This section highlights the recent progress for dual port, single port SRAM cells, CAM block and TCAM array variations etc.

Chapter 2: Literature Review

In this chapter, a detailed literature review of the transistor based SRAM cell is discussed in detail with its application for memory arrangement array is also presented. The chapter discusses a timeline advancement of different SRAM at several technology nodes. Several

SRAM cells are investigated in terms of threshold voltage, mobility, sub-threshold slope, on-off ratio and current. Moreover, SRAM cells are also studied in depth in terms of many performance parameters such as static and dynamic power, read and write access delay, temperature variation, etc. Furthermore, the SRAM cells are reviewed for the biomedical applications.

Chapter 3: Low Voltage Dual Port SRAM Cell for Low Power Applications

In this Chapter, two SRAM bit cells are designed, an eleven-transistor and a nine-transistor configuration static random access memory (SRAM) cell which are accessible by dual bit line. Both the cell are designed for low power consumption and are operable at lower supply voltage (>1V). Proposed 11T cell demonstrates strong read stability and energy efficiency, achieving low read power (~18.26 µW) and competitive read PDP (~207.79) compared to other high-transistor cells, making it suitable for low-power TCAM operations. It maintains a balanced Ion/Ioff ratio (~562), ensuring good switching characteristics and reduced leakage, which is critical for subthreshold and low-voltage applications. Area of Proposed 11T (~3.228 μm^2) is lower than conventional 11T variants, indicating a more optimized layout with reduced overhead, while still preserving robust performance. P9T cell outperforms most designs in speed, achieving very low read and write access times (4.5 ps / 1.2 ps), making it ideal for high-speed search operations in CAM/TCAM. It also shows low read/write power consumption (15.21 nW / 9.01 nW), resulting in excellent energy efficiency and reduced dynamic power compared to other 9T single/dual-port cells.

Chapter 4: Isolated Read Assist Enabled Robust Single Port 8T SRAM Cell

In this chapter, an eight-transistor configuration static random access memory (SRAM) cell which are accessible by single bit line. The noise margins (SNM) for the read, hold and write operations are found to be 181mV, 178 mV, and 204 mV, respectively. Accessing the write and read functionalities of cell takes 4.51 nS and 1.22 nS, respectively. The suggested design's temperature variation analysis shows that the values of HSNM vary by 0.118, 0.120, and 0.156 mV/° C variations in the values of HSNM, RSNM and Write Margin for 8TP cell, respectively. To further, justify the reliability of the design this article also presented a 2×2 array using the same 8TP cell design. The read consumption of power is also significantly reduced by a factor 3.25, 4, 4, 5, 1.5, 4, 3.125, 2.25, and 2 with respect to pre-existing 8T cells.

Chapter 5: TCAM Block Using 8T SRAM Cells for Logic Operations

In this chapter, a content addressable memory (CAM) block is designed using proposed 8T cell. The proposed CAM cell is only marginally larger than conventional 6T SRAM-based CAM cells, but achieves an effective array size reduction of ~1.25× through efficient architecture design. Additionally, it supports configurability as BCAM/TCAM and standard SRAM, improving overall hardware utilization. The design follows a conventional push-rule operation compatible with standard 6T SRAM cells, ensuring ease of integration and avoiding complex peripheral circuitry, which contributes to lower design overhead and improved energy efficiency. Subthreshold operation is leveraged to significantly reduce access energy and leakage power, making the design suitable for low-power SoC applications. However, SRAM stability challenges at low voltage are addressed through robust cell design. Performance of the proposed architecture is proving to be efficient in reliable in terms of power, delay, and power-delay product (PDP).

Chapter 6: TCAM Array using Single Port, Dual Port and Alternate SRAM Cells

In this chapter, Hybrid 8T–9T cell integration enables optimal trade-off between density and stability: 8T cells contribute reduced area and lower capacitance, while 9T cells provide a decoupled read path, eliminating read disturb and significantly improving read SNM, especially critical in TCAM search operations. The architecture achieves significant dynamic power reduction by leveraging lower switching capacitance of 8T cells and controlled read activity in 9T cells, thereby minimizing unnecessary bitline and matchline transitions during search cycles. Enhanced low-voltage (subthreshold) operability (<1V) is achieved due to the robust read isolation in 9T cells, which compensates for the weaker noise margins of 8T cells, ensuring reliable functionality under aggressive voltage scaling. Improved leakage power characteristics are obtained through reduced transistor stacking in 8T cells and controlled leakage paths in 9T cells, leading to an overall lower standby power profile, which is essential for always-on TCAM applications.

Chapter 7: Conclusion and Future Scope

In this chapter, the key findings of each chapter are summarized point-by-point to explain how each objective is achieved and their key features are reiterated. In the future scope section, the different aspects that can be worked upon are highlighted.

The chapters are followed by the list of publications and references. All the papers published, submitted and under progress for the completion of this work are listed in the last

section – List of Publications. While, all the books and papers that were referred to during the study to form the basis for this work are listed in the reference section.

CHAPTER – 2
LITRATURE REVIEW

2.1 OVERVIEW OF THE CHAPTER

In this chapter, a comprehensive survey on advanced SRAM, CAM and TCAM architectures developed for low-power, high-speed and process variation tolerant nanoscale memory systems is carried out. The reviewed literature covers the development of SRAM topologies from the conventional 6T structures to advanced 8T, 9T, 10T, and 11T architectures focusing on static noise margin (SNM) improvement, leakage reduction, low-voltage operation, and process variation resilience. The limitations of the conventional SRAM architecture under deep submicron CMOS scaling are critically analyzed including the read/write instability, thermal noise sensitivity, high leakage current and reduced reliability. Furthermore, advanced SRAM architectures are reviewed in which isolated read/write paths, assist techniques, single-ended sensing, and FinFET/CNTFET technologies are used to improve energy efficiency, sub-threshold operation and stability in nanoscale memory applications.

A detailed survey of CAM and TCAM architectures is also presented for high-speed associative search and in-memory computing applications. The literature survey is focused on SRAM-based BCAM and TCAM architectures, match-line sensing techniques, search-line optimization, precharge-discharge mechanisms, and parallel search operations for energy-efficient associative memory design. Recent developments in reconfigurable SRAM-TCAM arrays, FPGA-based TCAMs, AI-oriented associative memory systems, and computing-in-memory architectures are critically reviewed. The reviewed studies show that 8T SRAM architectures provide better read stability, 9T SRAM cells have better leakage suppression and writability, and that 11T architectures provide better computational flexibility and associative search capability for next-generation TCAM array implementations.

The chapter is structured as follows: the overview of the chapter, scheme of the literature review and the research background, are illustrated in section 2.1. Introduction of the structural variations in different SRAM cells is described in section 2.2 and the advanced SRAM architectures, advancements and voltage scaling is explained in section 2.3. Additionally, the detailed review of state-of-the-art CAM and TCAM architectures and SRAM-based associative memory arrays is described in section 2.4. Finally, the key observations and findings of the literature review are discussed in the section 2.5 of this chapter.

2.2 DEVELOPMENT OF LOW POWER AND STRUCTURAL VARIATIONS OF DIFFERENT SRAM CELLS

The first investigations of advanced SRAM topologies were primarily concerned with solving the leakage and read disturbance issues of single-ended structures. Lorenzo *et al.* [2017] proposed a novel 9T SRAM design with the focus on leakage power reduction and performance improvement, which is realized by the decoupled, read paths and optimized stacking transistors techniques [60]. The work established the importance of isolated read operation to mitigate destructive read access and to improve cell stability. Later, Mishra *et al.,* (2019) extended this direction by introducing analytical leakage modelling and leakage control methods in 9T SRAM structures [59]. They showed that with an optimized transistor sizing and leakage suppression techniques, the standby reliability can be greatly improved with an acceptable delay performance.

As technology scaled aggressively into deep submicron and FinFET compatible regimes, the research focus shifted toward ultra-low-power operation and variation tolerance. Roy *et al.* (2020) described single ended 9T SRAM cells [58] operating in the nanoscale technologies and emphasized the advantages of separate read circuitry in reducing read upset probability. In 2021, their next work again addressed the process variation sensitivity in 16 nm sub-threshold operation by proposing a variation-tolerant single-bitline 9T SRAM cell that is optimized for lower power dissipation and better stability. Meanwhile, Gupta *et al.* (2021) designed a data-independent 9T SRAM architecture that can support better ION/IOFF properties and smaller read bit-line voltage swing in near-threshold and sub-threshold regimes [57]. This design could effectively reduce the dynamic power and keep the reliable sensing margin.

Table 2.1. Application-Oriented SRAM cells in terms of Evolution and Technological Advancement

Year	Reference	Transistor Count	Advancement	Application
2026	Bansal *et al.* [47]	Single-ended 9T	Enhance read performance and write margin	Aerospace systems
2025	Haq *et al.* [51]	Ternary SRAM	Multi-valued storage with energy efficiency	Image processing accelerators
2025	Gaadhe *et al.* [50]	13T differential	Improved differential stability and sensing	High reliability computing
2025	Das *et al.* [49]	10T VN-TFET	Tunnel-FET based ultra-low-power operation	Emerging nanoelectronic systems
2024	Sharma *et al.*	High-SNM	Improved static noise margin	Reliable low-voltage

	[52]	SRAM	in 45 nm CMOS	memory
2023	Singhal *et al.*. [53]	9T	Stability enhancement through single-ended operation	Energy efficient SRAM arrays
2022	Abbasian *et al.* [54]	9T	Read-disturbance elimination and high writability	Bio-medical electronics
2022	Gupta *et al.* [55]	9T (TG-based)	Isolated read/write operation using TG structures	Robust low-voltage operations
2021	Gupta *et al.* [56]	9T	Data-independent operation with improved I_{ON}/I_{OFF}	Near-threshold processors
2021	Roy *et al.* [57]	9T	Variation-tolerance sub-threshold operation	Ultra-low power computing
2020	Roy *et al.* [58]	9T	Single-ended characterization and read stability enhancement	Nano scale SRAM arrays
2019	Mishra *et al.* [59]	9T	Analytical optimization and leakage control modelling	Embedded memory systems (Low Power)
2017	Lorenzo *et al.* [60].	9T	Isolated read and leakage reduction architecture	High-performance low-leakage systems

The comparative analysis in Table 2.1 illustrates the gradual transition of SRAM architectures from conventional leakage-aware 9T topologies to highly application-specific and reliability-driven memory cells with large transistor counts. The preliminary work has primarily concentrated on reducing leakage power and eliminating read disturbance through isolated read paths and optimized transistor stacking. With technology scaling to near-threshold and sub-threshold regimes, emphasis was put on variation tolerance, better writability and low-voltage stability. Recent works also demonstrate the incorporation of radiation-hardening techniques, multi-node upset tolerance and emerging device technologies such as VN-TFETs and ternary storage mechanisms. The trend towards SRAM cells with higher transistor count is being more customized for specialized applications such as aerospace electronics, biomedical systems, image processing accelerators and ultra-low-power embedded computing platforms.

During 2022, significant progress is reported on low-leakage and isolated-operation SRAM architectures. Abbasian *et al.* proposed a low-leakage single-bitline 9T SRAM cell for biomedical systems where ultra-low standby power and high writability are important design constraints [54]. The architecture provided isolated read access and improved write margin at lower supply voltages, eliminating read disturbance. Gupta *et al.* proposed a 9T SRAM cell using a transmission gate for achieving fully independent read and write operations for better stability and decreased switching activity [55]. Transmission-gate mechanisms were used to

achieve better write accessibility and reduce leakage propagation paths, thus enhancing robustness in low-voltage applications.

2.2.1 Stability Challenges in Different SRAM Cells Under Voltage Scaling

In recent years, research in SRAM design has shifted more and more toward application-oriented optimization, robustness against radiation effects and the use of emerging semiconductor devices. In [53], Singhal *et al.* (2023) proposed a single-ended 9T single-port SRAM design that enhances the cell stability by utilizing an optimized transistor topology and efficient isolation of the storage nodes from the bitlines to minimize the disturbance during the memory operations. Similarly, Sharma *et al.* (2024) demonstrated a high static noise margin (SNM) SRAM design in 45 nm CMOS technology highlighting the significance of strong noise immunity to guarantee reliable operation at reduced supply voltage [52].

By 2025, research in SRAM had expanded into a number of technological directions. A comprehensive numerical study of 10T SRAM cells based on vertical nanowire tunnel field effect transistors (VN-TFETs) and its comparison with conventional 6T–9T SRAM cells was conducted by Das et al. [49]. Their study highlighted the potential of emerging transistor technologies to realize highly energy-efficient memory systems. In another contribution, Gaadhe *et al.* presented a 13T differential SRAM cell architecture to improve the operational stability, increase the sensing accuracy and reduce the sensitivity to process-induced variations [50]. At the same time, Haq *et al*. presented an energy-aware ternary SRAM architecture for image processing applications [51]. The design exploits multi-valued storage states to achieve higher memory density and computational efficiency, while at the same time reducing switching activity and power dissipation, in line with the growing interest in in-memory and data-centric computing paradigms.

The most recent progress reported in 2026 is indicative of a strong focus on fault tolerant SRAM solutions for mission critical environments. Bansal *et al.* proposed a single-ended 9T SRAM cell for aerospace applications with enhanced read access and write capability [47]. The proposed architecture is intended to meet the reliability concerns due to radiation-induced upsets and soft errors. It is suitable to work in harsh aerospace environments where the integrity of the memory is of paramount importance [61].

2.2.2 Low Leakage and Energy Efficient SRAM Cells Based on Different Transistor Count

The increased number of transistors allowed for efficient self-recovery mechanisms, improved critical charge capability [62] and improved immunity to single-event upsets (SEUs) and multi-node upsets (MNUs), thus improving reliability in radiation-prone environments and mission-critical aerospace applications [63]. Cai *et al*. demonstrated a leakage-optimized 14T SRAM cell with multi-node upset tolerance, a crucial advancement towards radiation-hardened memory architectures. Recent investigations collectively show a gradual shift from conventional low-leakage 9T SRAM designs to higher transistor count designs that focus on reliability, process-variation resilience, energy efficiency, and radiation tolerance [64].

Previous work shows that as the number of transistors in SRAM cells increases, better decoupling between storage and access paths is provided leading to more stable operation. Such architectures are known to have higher noise margins, lower leakage currents and better robustness against low-voltage operation and adverse environmental conditions [65].

Table 2.2. Power and Energy optimization techniques for different SRAM cells

Reference and Year	**Leakage Reduction**	**Dynamic Power**	**Energy efficiency technique**	**Low voltage capability**
Lorenzo *et al.* [60] (2017)	Transistor stacking	Moderate	Decoupled read path	Intermediate
Mishra *et al.* [59] (2019)	Leakage control circuitry	Moderate	Analytical optimization	Intermediate
Roy *et al.* [58] (2020)	Single-ended bitline architecture	High	Reduced switching activity	Strong
Roy *et al.* [57] (2021)	Variation aware optimization	High	Sub-threshold operation	Very high
Gupta *et al.* [56] (2021)	Improved I_{ON}/I_{OFF}	High	Reduced RBL swing	Very high
Abbasian *et al.* [54] (2022)	Single-bitline architecture	High	Read isolation	Strong
Gupta *et al.* [55] (2022)	TG-based isolation	Moderate	Reduced short-circuit current	Intermediate
Singhal *et al.* [53] (2023)	Stability-assisted low leakage	Moderate	Single-port optimization	Intermediate
Sharma *et al.* [52] (2024)	Indirect improvement through SNM	Moderate	Stable low-voltage operation	Strong
Das *et al.* [49] (2025)	TFET-assisted leakage reduction	Very high	Band-to-Band tunnelling devices	Excellent
Gaadhe *et al.* [50] (2025)	Differential stabilization	Moderate	Efficient sensing operation	Strong
Haq *et al.* [51]	Reduced switching	Very high	Ternary data encoding	Excellent

(2025)	transitions			
Bansal *et al.* [47] (2026)	Optimized single-ended operation	High	Improved write margin	Strong
Cai *et al.* [48] (2026)	Leakage aware hardened architecture	Moderate	Multinode upset protection	Strong

In addition, the increasing demand for trustworthy memory solutions in nascent application fields like aerospace electronics, biomedical instrumentation, image-processing hardware, and near-threshold computing systems has further accelerated the development of specialized SRAM architectures providing an optimized trade-off between performance, power consumption, stability, and reliability requirements [66]. Table 2.2 presents the major energy efficient design methodologies adopted in advanced SRAM architectures to tackle the leakage dissipation and dynamic switching power in nanoscale technologies [67].

Most 9T architectures utilise single-ended bitline structure, isolation of read/write paths and transistor stacking techniques to reduce leakage currents and bitline switching activity during reads. Designs optimised for near- and sub-threshold operation demonstrate substantial improvements in energy efficiency through reduced voltage swing and enhanced Ion/Ioff characteristics. Advanced architectures like VN-TFET based 10T SRAM and ternary SRAM cells improve energy efficiency by reducing switching transitions and providing ultra-steep subthreshold conduction behaviour. The general trend is that the higher number of transistors, the better control of internal current paths, which in turn enables substantially reducing both the standby leakage and dynamic energy consumption, while providing dependable low-voltage operation.

2.2.3 Evolution of Read Assist and Stability Enhancement Techniques

The literature review indicates a systematic evolution of SRAM cell architectures from leakage-aware 9T topologies to highly robust and application-specific multi-transistor memory cells. Previous works focused on read-disturbance reduction and standby leakage reduction, while recent designs are more focused on radiation hardness, variation tolerance, ultra-low-voltage operation, and application-specific optimization. Auxiliary transistors provide decoupled read/write, improved SNM, improved writability and soft-error susceptibility suppression [68].

In addition, the introduction of new devices like tunnel FETs and ternary storage structures signals the shift towards next-generation low-power computing systems. Overall, the literature confirms the great advantage of the higher transistor-count SRAM architectures in

terms of stability, reliability and energy efficiency, and their high suitability for aerospace, biomedical, AI accelerators and near-threshold processing applications [69]. The comparison in Table 2.3 reveals that increasing the number of transistors significantly enhances the robustness, operational stability and fault tolerance of SRAM. Compared with the conventional 6T SRAM cell, the improved read stability and write margin are achieved by decoupled read operations and reduced read disturbance in the conventional 9T SRAM cell [70].

Table 2.3. Parametric analyses of various dual port SRAM cells

Technology, Year and Reference	Read Path & Write scheme	Supply Regime	Leakage Control Technique	SNM Improvement Method	Area Overhead	Key Metric Highlight
9T (SE)-2026 [47]	Decoupled read & Write-assist	Near-threshold	Stacked transistors	Read isolation	Medium	↑ Write Margin, ↑ Read Speed
14T -2026 [48]	Fully decoupled read & Differential write	Subthreshold	Multinode hardening	Redundant nodes	High	Radiation tolerant, ultra-low leakage
10T (TFET)-2025 [49]	Decoupled read & Standard write	Ultra-low V_{dd}	TFET low IOFF	Device-level gain	Medium	↓ Power, steep slope
13T -2025 [50]	Differential read & Assisted write	Low V_{dd}	Internal feedback control	Cross-coupled strengthening	High	Very high SNM
Ternary SRAM -2025 [51]	Multi-level read & Voltage-mode write	Low V_{dd}	Buffer isolation	Logic-level stability	High	Multi-bit storage efficiency
CMOS SRAM -2024 [52]	Shared read & Conventional write	45nm nominal	Sizing optimization	Cell ratio tuning	Low	SNM validation
9T (SE)-2023 [53]	Isolated read & Single-ended write	Low V_{dd}	Reduced bitline swing	Decoupled read node	Medium	Stability enhancement
9T (SBL)-2022 [54]	Fully isolated read & Write-assist	Subthreshold	Single-bitline + stack	Read path isolation	Medium	No read disturb, ↓ leakage
9T (TG-based)-2022 [55]	Decoupled read & TG-assisted write	Low V_{dd}	Transmission gate gating	Separate R/W paths	Medium	Strong write ability
9T -2021 [56]	Decoupled read & Standard write	Subthreshold	Reduced RBL swing	Bitline control	Medium	High I_{ON}/I_{OFF}
9T -2021 [57]	Decoupled read & Standard write	Subthreshold	Variation-aware sizing	Robust cross-coupling	Medium	PVT tolerant
9T -2020 [58]	Semi-decoupled read & Conventional	Nominal	Baseline	Basic feedback	Low	Characteriza-tion study

	write					
9T -2019 [59]	Decoupled read & Standard write	Low V_{dd}	Leakage control circuit	Feedback stabilization	Medium	Analytical leakage model
9T -2017 [60]	Decoupled read & Standard write	Nominal	Transistor stacking	Read isolation	Medium	Early low-leakage design

However, advanced architectures such as 10T, 13T, and 14T SRAM cells show better immunity to process variations, soft errors, and radiation-induced disturbances by means of additional assist circuitry and isolated storage nodes. Differential sensing techniques and multi-node upset recovery mechanisms greatly enhance static noise margin and reliability under harsh operating conditions. With the overhead of more complex circuits and area, the higher transistor-count SRAM cells offer significant benefits in terms of aerospace-grade reliability, low-voltage operation, and variation-tolerant operation. Therefore, they are very much suitable for next-generation high-reliability memory systems.

2.3 ADVANCED 8T SRAM TOPOLOGIES

The aggressive scaling of CMOS technology towards sub-threshold voltage and lower nm range and nanosheet regimes has posed severe challenges to conventional SRAM architectures in terms of leakage current, process variability, reduced static noise margin (SNM), degraded writability and unstable sub-threshold operation [71]. Traditional 6T SRAM cells are increasingly subject to read disturbance, half-select instability and high power dissipation at reduced supply voltages. To overcome these drawbacks, several improved 8T SRAM architectures have been proposed and researched widely. These 8T SRAM cells have isolated read paths [72], which provide improved stability, lower leakage, and better low voltage operation without significantly increasing the area overhead [73]. The extra transistors in 8T cells allow the read and write operations to be decoupled, which significantly improves the read SNM, suppresses destructive read access, and enhances robustness against process-voltage-temperature (PVT) variations [74].

2.3.1 Technological Refinements in Different 8T SRAM Cells

A few recent studies indicate substantial advancements in nanoscale SRAM designs for edge artificial intelligence (AI) solutions and deep neural network accelerators. Sharma et al. (2025) suggested a new 8T SRAM cell utilizing PFC and PPC vertical stacked carbon nanotube field-effect transistor (VS-CNTFET) technologies [73]. The proposed design exploited the superior electrostatic gate control and inherently low leakage characteristics of

CNTFET devices resulting in improved energy efficiency and memory reliability. In a similar vein, Dahiya *et al.* (2025) proposed low-power 8T SRAM architecture in a 32 nm technology node, which successfully suppresses half-select disturbances and demonstrates significant immunity to process-induced variations under aggressive voltage-scaling conditions [74]. In another contribution, Dinesh *et al.* [75] used dynamic body-biasing techniques for sub-threshold SRAM performance enhancements, providing higher operating speeds while suppressing leakage currents and maintaining cell stability at reduced supply voltages.

Since 2022, SRAM research has been directed increasingly towards disturbance free memory operation, parallel accessibility and application-driven architectural enhancements [76]. To solve the problem of instability caused by half row activation in conventional SRAM arrays, Lorenzo *et al.* (2022) proposed an 8T SRAM cell to avoid half-select disturbances. Their design successfully maintained data integrity during partial accesses while maintaining low standby leakage characteristics [77]. Simultaneously, Aura *et al.* (2022) proposed a high-performance dual-port 8T SRAM cell for simultaneous read and write operations. The proposed design enhanced memory bandwidth and access efficiency significantly, which was particularly suitable for advanced embedded systems and high-throughput computing platforms [78].

Another major trend in recent years is the convergence of SRAM technology with emerging computing paradigms such as in-memory computing and hardware acceleration for machine-learning workloads [79, 67]. Duari *et al.* [80] have demonstrated a 4×4 SRAM array using 8T cells with single-ended read mechanism along with differential write operation for low voltage operation. The architecture achieved better write margins and reduced bit-line switching activity, thus improving the overall energy efficiency in embedded memory applications [81]. Jaiswal *et al.* (2019) further extended this idea by investigating the use of 8T SRAM arrays as multi-bit dot-product engines for beyond–Von Neumann computing systems. Their results have shown that SRAM-based architectures can be promising candidates for in-memory computation, effectively alleviating the performance and energy penalties incurred by frequent processor–memory data transfers [82].

The evolution of these concepts has led to the development of advanced computing-in-memory (CIM) SRAM macros optimized for AI workloads. One prominent example is the Union SRAM [76] by Kim *et al.* (2024), which is a process-voltage-temperature (PVT) self-compensated current mode 8T SRAM architecture with a configurable precision for multiply–accumulate (MAC) operations. The design showed stable operation under various

environmental conditions and provided efficient computation for artificial intelligence and machine-learning applications.

Research has also continued to focus on ultra-low-power and sub-threshold SRAM operation. Kushwah *et al.* (2015) [83] designed a single-ended 8T SRAM cell with adaptive dynamic-feedback control mechanisms for reliable sub-threshold operation. The design improves read stability, and data retention ability and meanwhile reduces standby leakage power by intelligent feedback regulation. Similarly, Pal *et al.* (2015) proposed variation tolerant differential 8T SRAM architecture for ultra-low power applications [84].

Table 2.4. Advancement and different applications of 8T SRAM cells

Year	Reference	SRAM Type	Major Advancements	Application
2026	Trivedi *et al.* [71]	Single-rail custom logic SRAM	350 mV operation in 2 nm nanosheet CMOS	Mobile and edge-AI
2026	Dai *et al.* [72]	T8T CIM SRAM Macro	Ternary DNN and Boolean computation	Ai and neural processing
2025	Sharma *et al.* [73]	VS-CNTFET 8T SRAM	CNTFET-based leakage reduction	Nanoelectronics' memory
2025	Dahiya *et al.* [74]	Half-select free 8T	Variation-resistant voltage scaling	32 nm low-power systems
2025	Dinesh *et al.* [75]	Dynamic body bias 8T	High-speed sub-threshold operation	Ultra-low-voltage processors
2024	Kim *et al.* [76]	Union SRAM CIM Macro	PVT auto-compensated current-mode MAC	AI accelerators
2022	Lorenzo *et al.* [77]	Half-select free 8T	Disturbance-free operation	Robust memory arrays
2022	Aura *et al.* [78]	Dual-port 8T SRAM	Simultaneous parallel read-write	High-speed systems
2021	Duari *et al.* [79]	4x4 8T SRAM Array	Single-ended read and differential write	Low voltage SRAM arrays
2020	Duari *et al.* [80]	Low-leakage 8T SRAM	Leakage suppression and improved stability	IoT devices
2020	Roy *et al.* [81]	TG-based differential 8T	Ultra-low-power operation	Energy-efficient embedded systems
2019	Jaiswal *et al.* [82]	8T CIM SRAM	Multibit dot-product computation	Beyond von Neumann computing
2015	Kushwah *et al.* [83]	Dynamic feedback 8T	Sub-threshold stability enhancement	Ultra-low power systems

2015	Pal *et al.* [84]	Differential 8T SRAM	Variation-tolerant operation	Low-power applications
2012	Wen *et al.* [85]	Differential-read 8T	Tunable access and pull-down transistors	Stable nanoscale SRAM
2010	Chang *et al.* [86]	D^2AP 8T SRAM	Expanded read/write stability at low V_{DD}	Low-voltage CMOS memory
2012	Islam *et al.* [87]	Variability-aware SRAM	Leakage and variability reduction	Reliable embedded memory

The proposed cell employs differential sensing techniques to demonstrate enhanced tolerance to threshold-voltage variations and process mismatches, ensuring reliable operation in deeply scaled CMOS technologies and low-voltage applications. Early progress in 8T SRAM architectures was targeted at low voltage reliability and variability tolerance [85]. Chang *et al*. (2010) proposed a differential data-aware power-supplied (D^2AP) 8T SRAM architecture that can improve read and write stability at lower V_{DD} [86]. The design employed adaptive power supply control to increase minimum operating voltage (V_{DD}min) while maintaining stability margins. In the same period, Wen *et al*. (2012) proposed a differential-read 8T SRAM cell with tunable access and pull-down transistors to optimize read current and improve sensing reliability [85]. Islam *et al.* (2012) have also addressed the variability-induced reliability degradation by proposing a variability-aware low-leakage SRAM design methodology focusing on leakage suppression and process variation resilience [87].

2.3.2 8T SRAM Architectures with Enhanced Stability for AI Acceleration

The evolution of 8T SRAM architectures from low voltage stability orientated memory cells to highly application specific computing enabled SRAM systems is shown in Table 2.4. The initial research has been mainly focused on the tuning of the read/write stability and the variability effects in the scaled CMOS technologies. Further developments have resulted in leakage aware designs, differential sensing mechanisms and half-select disturbance suppression for reliable ultra-low power operation. Recent developments show a strong trend towards computing-in-memory architectures, AI acceleration, nanosheet CMOS integration and CNTFET based SRAM implementations. Overall, the trend shows that 8T SRAM cells have evolved from conventional storage elements to multifunctional computational memory structures for edge computing, neural processing and next generation energy efficient systems. Systematic representation of workflow for SRAM cell is shown in Fig. 2.1.

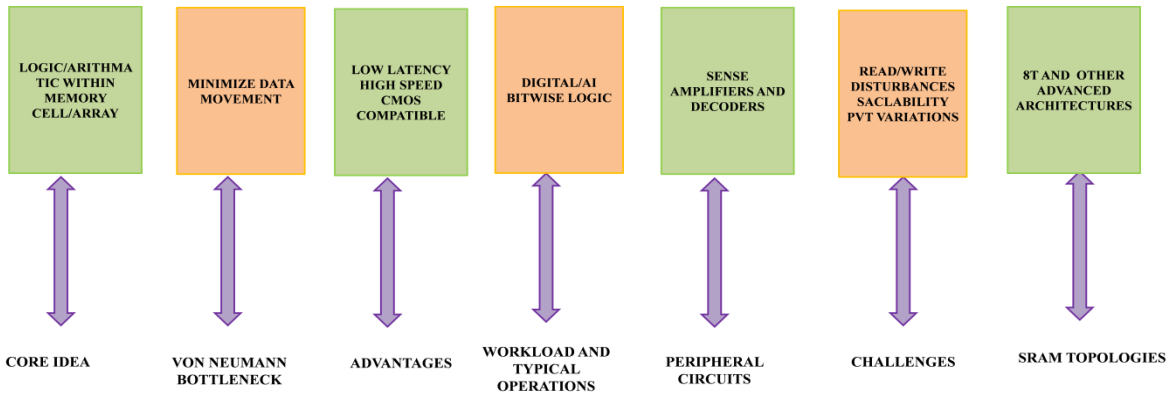


Fig. 2.1. Systematic representation of workflow for SRAM cell

The advent of IoT and energy-constrained edge devices has motivated research on leakage-efficient and low-voltage SRAM arrays. Duari *et al.* (2020) has proposed a low leakage 8T SRAM cell for IoT applications by using an isolated read circuit and better transistor sizing techniques to improve stability and reduce standby power consumption.

Table 2.5. Energy and Power optimization characteristics of 8T SRAM architectures

Reference	Year	Leakage Reduction Techniques	Dynamic Power Optimization	Energy-Efficient Mechanism	Voltage Scaling Capabilities
Chang *et al.* [86]	2010	Adaptive power supply control	Moderate	D^2AP stabilization	Strong
Wen *et al.* [85]	2012	Tunable transistor sizing	Moderate	Differential read sensing	Moderate
Islam *et al.* [87]	2012	Variability-aware leakage suppression	Moderate	Process compensation	Strong
Kushwah *et al.* [83]	2015	Dynamic feedback control	High	Sub-threshold operation	Very high
Pal *et al.* [84]	2015	Differential operation	High	Variation tolerance	Very high
Jaiswal *et al.* [82]	2019	Reduced data movement	Very high	In-memory computation	Strong
Duari *et al.* [80]	2020	Read path isolation	High	Low leakage standby	Strong
Roy *et al.* [81]	2020	Transmission-gate operation	High	Reduced switching power	Very High
Duari *et al.* [79]	2021	Single-ended read	High	Differential write-scheme	Strong
Lorenzo *et al.* [77]	2022	Half-select suppression	Moderate	Disturbance-free access	Strong
Aura *et al.* [78]	2022	Parallel access mechanism	Moderate	Dual-port operation	Moderate

Kim *et al.* [76]	2024	Current-mode computation	Very high	CIM MAC operation	Strong
Sharma *et al.* [73]	2025	CNTFET-based leakage reduction	Very high	Improved electrostatic control	Excellent
Dahiya *et al.* [74]	2025	Variation-resistant scaling	High	Half-select-free operation	Very high
Dinesh *et al.* [75]	2025	Dynamic body biasing	Very high	Sub-threshold acceleration	Excellent
Dai *et al.* [72]	2026	Embedded ternary computation	Extremely High	CIM DNN processing	Excellent
Trivedi *et al.* [71]	2026	Single-rail 350mV operation	Extremely High	2nm nanosheet scaling	Outstanding

Roy *et al.* [2015] presented differential transmission-gate-based 8T SRAM architecture for ultra-low-power applications. Transmission-gate structures were used in addition to ensuring robust read operation at reduced supply voltages to minimize switching loss and improve write accessibility. The power and energy analysis in Table 2.5 shows that sophisticated 8T SRAM architectures can achieve significant reduction in leakage and dynamic power by utilising isolated read paths, adaptive biasing [88], differential sensing and emerging transistor technologies.

The early works focused mainly on transistor sizing optimisation and adaptive supply techniques. The modern architectures exploit current-mode computing, dynamic body biasing and CNTFET integration for aggressive energy minimisation [89]. Computing-in-memory SRAM macros can save a lot of energy for data transfer by doing the arithmetic operations in the memory array. Moreover, recent implementations of nanosheets and sub-threshold SRAM show excellent voltage scalability and ultra-low-power operation [90], which makes advanced 8T SRAM architectures very attractive for AI accelerators, IoT systems, and mobile edge computing platforms.

2.3.3 Comparative Analysis of 8T SRAM Architectures Based on Stability and Energy Metrics

The latest development incorporates SRAM with AI acceleration and nanosheet technologies. A T8T SRAM computing-in-memory macro for ternary deep neural networks and Boolean logic computations was proposed by Dai *et al.* (2026). The architecture incorporated arithmetic capability directly within the memory array, greatly enhancing computational density and energy efficiency [91]. Similarly, Trivedi *et al.* (2026) showed a 350 mV single-rail SRAM based on custom logic-bitcell architecture in 2 nm CMOS nanosheet technology for mobile and edge-AI applications [71]. This design is a major step in enabling ultra-low-

voltage SRAM operation by combining nanosheet transistor technology with aggressive voltage scaling for next generation energy efficient AI hardware [92].

Table 2.6. Performance analyses of different parameters in 8T SRAM architectures

Reference	Technology Node	Read SNM	Write Margin	Leakage Power	Delay/Speed	Process Variation Tolerance
Chang *et al.* [86] (2010)	CMOS	~1.4× higher RSNM	Expanded write stability	Moderate reduction	Improved low-voltage access	Moderate
Wen *et al.* [85] (2012)	CMOS	~20–30% RSNM enhancement	Moderate	Reduced read disturbance leakage	Faster differential sensing	Moderate
Islam *et al.* [87] (2012)	CMOS	~25% stability enhancement ~50% higher RSNM	Moderate	Significant standby leakage reduction	Moderate	High
Kushwah *et al.* [83] (2015)	45 nm CMOS	~50% higher RSNM	Improved hold stability	~40% leakage reduction	Moderate	High
Pal *et al.* [84] (2015)	32 nm CMOS	~45–60% RSNM enhancement	Improved writability	Reduced Sub-threshold leakage	High-speed differential read	Very High
Jaiswal *et al.* [82] (2019)	CMOS	Stable read operation	Moderate	Reduced data transfer energy	Parallel dot-product acceleration	Moderate
Duari *et al.* [80] (2020)	CMOS	~35% RSNM improvement	High write margin	~30% lower leakage power	Moderate	High
Roy *et al.* [81] (2020)	16 nm CMOS	~60% RSNM enhancement	~20% write improvement	~45% leakage reduction	Faster TG-based access	High
Duari *et al.* [79] (2021)	CMOS	~40% higher stability	Differential write improvement	Reduced bitline switching power	Improved array speed	High
Lorenzo *et al.* [77] (2022)	CMOS	~50% RSNM improvement	High write stability	Low standby leakage	Moderate	High
Aura *et al.* [78] (2022)	CMOS	Stable simultaneous operation	High	Moderate	Parallel read-write capabilities	Moderate
Kim *et al.* [76] (2024)	Advanced CMOS	Very high sensing stability	Configurable precision	Significant computation energy reduction	Current mode MAC acceleration	Very High
Sharma *et al.* [73] (2025)	VS-CNTFET	~70% SNM enhancement	Strong write capability	Extremely low leakage	Fast CNTFET switching	Very High
Dahiya *et al.* [74] (2025)	32 nm CMOS	~65% RSNM enhancement	High write margin	~50% lower leakage	Stable under scaling	Very High
Dinesh *et al.* [75]	CMOS with body biasing	~75% stability improvement	Enhanced writability	Reduced standby	High-speed sub-	High

(2025)				current	threshold operation	
Dai *et al.* [72] (2025)	Advanced CMOS CIM	Stable ternary sensing	Optimised Boolean write operation	Very low computation energy	High-throughput DNN acceleration	Very High
Trivedi *et al.* [71] (2026)	2 nm CMOS nanosheet	Extremely high-low voltage stability	Reliable low voltage writing	Ultra-low power operation	High-speed nanosheet access	Extremely High

In summary, the surveyed literature reveals that 8T SRAM architectures have developed from simple stability-enhanced memory cells to highly specialised platforms that are capable of enabling ultra-low-power computing, IoT systems, in-memory processing [93], AI acceleration, and nanoscale edge devices. The incorporation of isolated read paths, differential sensing structures, adaptive biasing techniques and emerging device technologies has paved the way for substantial enhancement in SNM, leakage suppression, half-select immunity and energy efficiency [94]. These developments lay the groundwork for the advanced 8T SRAM cells to be highly promising candidates for future low-power, variation-tolerant, and computation-integrated memory systems. The comparison results are shown in Table 2.6. It is shown that the proposed 8T SRAM cell as much better read stability, write-ability, leakage power suppression and low voltage operation than the conventional SRAM cell [95].

The early differential-read and supply adaptive designs mainly focused on the enhancement of the RSNM and the reduction of the read disturbance under the lower supply voltages. As CMOS scaling reached deep submicron and sub-threshold regions, architectures employing dynamic feedback control, transmission-gate structures, and isolated read paths achieved substantial reductions in standby leakage and enhanced tolerance to process variations. Modern 8T SRAM designs further integrate sophisticated techniques including dynamic body biasing, CNTFET devices, current-mode sensing and computing-in-memory (CIM) operation for ultra-low-power and high-performance operation.

The recent architectures implemented in nanosheet CMOS and AI-oriented CIM frameworks offer excellent voltage scalability, computational capability and robustness under aggressive technology scaling. Half-select disturbance suppression, PVT auto-compensation, and ternary computation mechanisms can be added to further improve the reliability and energy efficiency of next-generation edge-AI, neural processing, and mobile computing systems. These architectures, however, increase design complexity and area overhead, but offer

significantly better operational margins, energy efficiency, and computational integration capability required for future high-density memory systems.

2.4 SRAM-BASED CAM/TCAM ARCHITECTURES

The growing data-centric computing, artificial intelligence acceleration, networking infrastructure and high-speed search-intensive applications have greatly increased the demand for energy-efficient Content Addressable Memory (CAM) and Ternary Content Addressable Memory (TCAM) architectures [96]. CAM-based structures, unlike traditional SRAM arrays, support parallel associative search operations, and thus can significantly decrease search latency and improve computational throughput. However, traditional CAM and TCAM implementations have high power dissipation [97], match-line leakage, reduced sensing margins, soft-error vulnerability, and serious scalability challenges as CMOS technology reaches nanoscale dimensions [98]. Therefore, recent research efforts have been directed toward the integration of SRAM-based reconfigurable CAM structures, computing-in-memory (CIM) capabilities, low-leakage sense amplifiers, and emerging memory technologies to circumvent these limitations [99].

2.4.1 Evolution of SRAM-Based Associative Memory and TCAM Architectures

The first fundamental contributions to CAM architecture were presented by Wade *et al.* (2002) who proposed a ternary content-addressable search engine capable of high speed search operations by evaluating match-lines in parallel. This work defined the architectural principles for search acceleration upon TCAM. Pagiamtzis *et al.* (2006) recently published an extensive tutorial on CAM architectures at the circuit level, focusing on power bottlenecks due to match-line precharge and search-line switching activity [100]. Their analysis revealed important design challenges related to dynamic power dissipation, sensing reliability and scalability with the increase of array density [101].

In the same period, Pagiamtzis *et al.* (2006) proposed a soft-error tolerant CAM architecture based on error-correcting match schemes to improve the resilience against radiation-induced transient faults. Hsieh *et al.* (2008) addressed the power optimization by gate-block selection algorithms of pre-computation-based CAM structures, which greatly reduce the unnecessary search activity and dynamic switching power. These pioneering contributions formed the basis of the design of modern low-power and fault-tolerant associative memory.

Sangalang *et al.* (2026) recently reported a highly energy-efficient single-ended CAM cell operating at 200 MHz and that cell is showing good energy efficiency i.e. 1.22 fJ/bit/search in

45nm CMOS technology [97]. The architecture shows a significant improvement on search energy efficiency while maintaining high speed associative matching. Ternary SRAM-based computing-in-memory macros capable of Boolean logic and ternary neural processing were used to extend SRAM functionality for deep-learning acceleration (Dai *et al.* 2026) [95].

Kishore *et al.* (2026) discussed leakage reduction techniques at the circuit level for the sense amplifiers in SRAM and TCAM in the peripheral circuitry level [96]. They considered transistor stacking, body-bias modulation, adaptive sensing and offset-compensation techniques to suppress the leakage current without affecting the sensing speed and reliability [102-104].

Table 2.7: Technological advancement and application evolution of SRAM-CAM/TCAM architectures

Year	Reference	Architecture	Major Advancement	Application
2026	Kishore *et al.* [96]	Sense amplifier review	Leakage suppression circuits	SRAM/TCAM arrays
2026	Sangalang *et al.* [97]	Single-ended CAM	1.22 fj/bit/search efficiency	Ultra-low-energy search
2025	Hassan *et al.* [98]	6T SRAM configurable CAM	BCAM/TCAM/similarity indexing	AI search systems
2025	Zhang *et al.* [99]	10T SRAM-CAM	Energy-efficient CAM+CIM	Edge computing
2025	Himaja *et al.* [100]	Hybrid-cache TCAM	Triple-level cache acceleration	High-performance processors
2023	Wei *et al.* [101]	11T SRAM-CAM	Dual-direction logic/CAM operation	In-memory computing
2024	Padmini *et al.* [103]	Secure TCAM	Energy-aware encrypted search	Wireless security
2022	Irfan *et al.* [104]	FPGA CAM survey	Reconfigurable associative computing	FPGA systems
2021	Gangadhar *et al.* [105]	CNTFET-TCAM	Leakage efficient nanoscale search	Future networks
2020	Ullah *et al.* [106]	ER-TCAM	FPGA soft error-resilience	FPGA acceleration
2015	Karam *et al.* [108]	Memory-based computing	SRAM-CAM computational integration	Memory-centric computing
2015	Jeloka *et al.* [109]	Configurable 6T CAM	Multi-node SRAM/BCAM/TCAM	Reconfigurable logic
2006	Pagiamtzis *et al.* [110]	Error-correcting CAM	Soft-error resilience	Reliable CAM systems
2008	Hsieh *et al.* [111]	Pre-computation CAM	Reduced dynamic switching activity	Low-power search
2006	Pagiamtzis *et al.* [112]	CAM survey	Foundational CAM architecture optimization	VLSI search systems

2002	Wade *et al.* [113]	TCAM search engine	High-speed ternary associative speech	Search acceleration

The nanoscale CAM structures prompted a look into advanced transistor technologies. Gangadhar *et al.* (2021) proposed a CNTFET based TCAM cell with reduced leakage current, high speed search performance and improved electrostatic control for the future generation networking applications [105]. Carbon nanotube FET devices showed improved short-channel behaviour and reduced static power consumption in comparison to CMOS-based TCAM implementations. The rise of memory-centric computing architectures has led to a greater interest in the integration of reconfigurable CAM-SRAM. Karam *et al.* (2015) provided an extensive review of memory-centric computing trends, highlighting the shift from traditional storage-based SRAM to computational memory systems that enable associative search and logic execution [108]. Jeloka *et al.* (2015) further proposed a configurable TCAM/BCAM/SRAM architecture implemented with 28 nm push-rule 6T SRAM bitcells supporting multi-mode operation with no significant area overhead [109]. This work demonstrated the practical feasibility of reconfigurable memory systems that can perform search, storage and logic within integrated SRAM arrays.

The evolution of CAM and TCAM from dedicated search engines to SRAM-based reconfigurable associative computing architectures is shown in Table 2.7. The early work was on speeding up search and fault tolerance, while more recent work is on unifying the search-compute-memory functionality. Recent architectures have included reconfigurability, low-energy searching techniques, and advanced transistor technologies to accelerate AI, secure communications, and implement high density memory centric system.

2.4.2 Soft-Error Resilient and FPGA-Based TCAM Implementations

Soft-error tolerance becomes increasingly important for FPGA-based TCAM implementations. Ullah *et al.* (2020) introduced ER-TCAM, a ternary content addressable memory architecture based on SRAM with soft error mitigation strategies designed for implementation on FPGAs. The design greatly enhanced reliability while still offering fast search performance in reconfigurable logic environments.

Recent advances emphasize reconfigurable in-memory computing based on SRAM and hybrid search-compute functionality. Irfan *et al.* (2022) surveyed the implementation of reconfigurable CAM on FPGA platforms, and identified major opportunities for adaptive search acceleration and logic flexibility [104]. Hassan et al. (2025) introduced a

reconfigurable in-memory computing framework that supports BCAM, TCAM, similarity indexing, and logic-in-memory operations using standard 6T SRAM [98]. Their design showed that standard SRAM arrays could perform associative search and computation functions without any CAM-specific cell modifications. Basic components of memory computing are shown in Fig. 2.2.

Architectural improvement has also been widely explored via transistor-level innovation. Zhang *et al.* proposed a reconfigurable type 10T SRAM cell for energy-efficient CAM operation and in-memory computing [105]. Auxiliary transistors were effective for strong search operation, low match-line activity and computational efficiency.

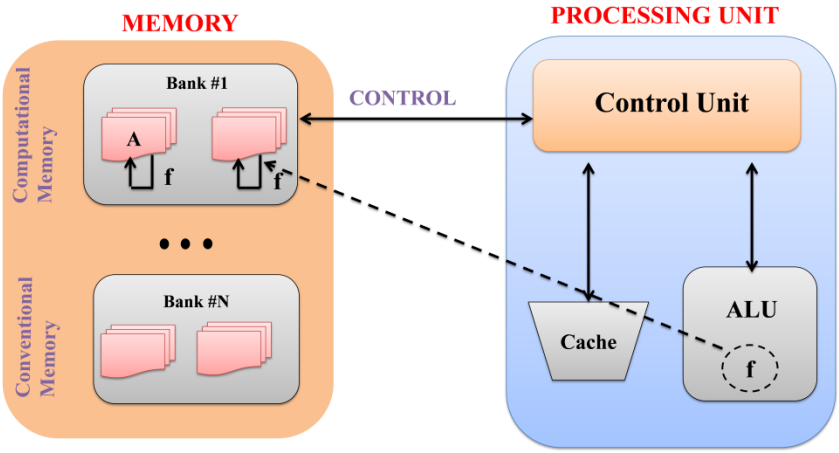


Fig. 2.2. Basic components of memory computing

Similarly, Wei *et al.* (2023) proposed an 11T SRAM architecture that can perform dual-direction in-array logic and CAM operations, demonstrating the capability of simultaneous search and logic execution [106]. Emerging application-specific CAM architectures further reinforce the trend of system-level optimization. Himaja *et al.* (2025) proposed triple level hybrid cache architecture with the help of TCAM for high performance VLSI systems which reduces cache lookup latency significantly [108]. Padmini *et al.* (2024) proposed an energy-efficient TCAM for secure wireless communication systems focusing on lower power consumption during encrypted search operations.

2.4.3 Energy-Efficient Match-Line and Search-Line Optimization Techniques

The literature survey reveals a clear evolution from conventional CAM search engines to fully integrated SRAM-based reconfigurable associative computing platforms. We show significant improvements in search energy, leakage current and latency [109], as well as scalability and reliability for future edge-AI, secure communication, FPGA acceleration and

memory-centric computing systems by introducing advanced transistor architectures, reconfigurable bitcells [110], CIM enabled SRAM structures and energy-aware sensing circuits.``As shown in the technical comparison in Table 2.8, the SRAM-based CAM and TCAM architectures have achieved a significant progress in the search-energy minimization and the leakage-power suppression. Early CAM architectures were mainly concerned with reducing the power of switching match-lines by using precomputation and selective activation schemes [111]. Later designs incorporated reconfigurable SRAM reuse, adaptive search-line control, and in-memory computing approaches to reduce data-transfer energy and redundant switching activity. Instead of that, the emerging CNTFET based TCAM structures show significant leakage reduction due to better electrostatic gate control and reduced short channel effects [112].

Table 2.8. Different methodologies for power and energy optimization in SRAM- Based CAM/TCAM.

Reference and Year	Technology	Operating Voltage	Energy Consumption	Leakage Reduction Methodology	Match/Search Power	Delay/Speed Metric
Wade *et al.* [113] (2002)	CMOS	5 V class	pJ/search range	Conventional match-line precharge	Parallel ternary comparison	High-speed associative search
Pagiamtzis *et al.* [112] (2006)	CMOS	Nominal CMOS supply	Reduced dynamic power by ECC-assisted matching	Error correcting match scheme	Reduced false match transitions	Improved reliability latency
Hsieh *et al.* [11] (2008)	CMOS	Low-voltage compatible	~20–30% lower dynamic power	Gate-block selection	Pre-computation search suppression	Faster selective search
Karam *et al.* [108] (2015)	CMOS	Scaled CMOS	Reduced memory-access energy	Memory-centric architecture	Data-movement minimization	Improved throughput
Jeloka *et al.* [109] (2015)	28 nm CMOS	Near-threshold capable	Significant energy reduction through mode sharing	Unified TCAM/BCAM/SRAM cell reuse	Reduced hardware redundancy	High speed configurable operation
Ullah *et al.* [106] (2020)	FPGA-SRAM TCAM	FPGA supply domain	Moderate search energy	Soft-error mitigation logic	FPGA search optimization	Low FPGA search latency
Gangadhar *et al.* [105] (2021)	CNTFET	Ultra-low voltage	~40–60% lower leakage than CMOS	CNTFET electrostatic control	Reduced matchline current	>300 MHz operation

Irfan *et al.* [104] (2022)	FPGA CAM	FPGA-scaled voltage	Reduced LUT-based search energy	Reconfigurable routing optimization	Adaptive-associative matching	Improved FPGA throughput
Wei *et al.* [101] (2023)	11T SRAM	Low-voltage CMOS	Reduced compute-transfer energy	In-array logic sharing	Simultaneous logic/CAM execution	Fast bidirectional operation
Padmini *et al.* [103] (2024)	TCAM	Low-power VLSI supply	~25–35% lower search power	Secure switching optimization	Reduced encrypted search activity	Moderate latency
Hassan *et al.* [98] (2025)	Standard 6T SRAM	Low-voltage SRAM domain	Significant reduction in logic-search energy	SRAM reuse for BCAM and TCAM	Elimination of dedicated CAM arrays	High associative throughput
Zhang *et al.* [99] (2025)	10T SRAM	Near-threshold	~45% lower search energy	Reduced search line swing	CIM-enabled match operation	Low-latency search-compute
Sangalang *et al.* [97] (2025)	45 nm CMOS	Low-voltage operation	1.22 fJ/bit/search	Single-ended search architecture	Ultra-low switching activity	200 MHz
Kishore *et al.* [96] (2026)	CMOS sense amplifier	Scaled CMOS supply	Large standby leakage suppression	Body-bias and transistor stacking	Adaptive sensing circuits	Faster sensing response

Advanced SRAM-CAM implementations also utilize computing-in-memory techniques, reduced search-line voltage swing, and single-ended associative search structures to achieve femtojoule-level search energy. The achieved 1.22 fJ/bit/search operation at 200 MHz is one of the lowest energy associative search implementations reported for nanoscale CMOS TCAM systems [99].

Table 2.9. Performance comparison of different SRAM- Based CAM/TCAM architectures.

Reference and Year	**Technology Node**	**Search Frequency**	**Search Delay**	**Soft-error Immunity**	**Re-configurability**	**In-memory computing capability**
Wade *et al.* [113] (2002)	CMOS	~100 MHz	~10 ns	Low	Low	No
Pagiamtzis *et al.* [112] (2006)	CMOS	High speed	Reduced latency	Moderate	Low	No
Pagiamtzis *et al.* [110] (2006)	CMOS	Moderate	Slight ECC overhead	High	Low	No
Hsieh *et al.* [111] (2008)	CMOS	High	Reduced search delay	Moderate	Moderate	No
Jeloka *et al.*	28 nm	~250 MHz	Low	Moderate	Very high	Partial

[109] (2015)	CMOS					
Ullah *et al.* [106] (2020)	FPGA SRAM	High	Low FPGA latency	Very high	High	No
Gangadhar *et al.* [105] (2021)	CNTFET	>300 MHz	Very low	High	Moderate	No
Irfan *et al.* [104] (2022)	FPGA	Moderate-High	Moderate	Moderate	Extremely high	Partial
Wei *et al.* [101] (2023)	CMOS	High-speed	Low	High	High	Dual-direction logic/CAM
Padmini *et al.* [103] (2024)	CMOS	Moderate	Moderate	Moderate	Moderate	No
Hassan *et al.* [98] (2025)	CMOS SRAM	High	Low	Moderate	Extremely High	BCAM/TCAM/Logic-in-memory
Zhang *et al.* [99] (2025)	CMOS	High	Very-low	High	Very High	CAM + CIM
Himaja *et al.* [100] (2025)	CMOS	High speed cache access	Low	Moderate	Moderate	Cache acceleration
Sangalang *et al.* [97] (2026)	45 nm CMOS	200MHz	<5 ns	Moderate	Moderate	No
Kishore *et al.* [96] (2026)	CMOS	Ultra-fast sensing	Reduced sensing delay	High	Moderate	Peripheral assist

As summarized in Table 2.9, the performance comparison indicates that the modern SRAM-CAM and TCAM architectures achieve significant improvements in search speed, computational integration and fault resilience when compared to the conventional associative memories. Early TCAM architectures were designed primarily for high-speed parallel search operations. The latest SRAM-based CAM designs leverage configurable logic, in-memory computation, and adaptive match-line control to enhance functionality and energy efficiency. Reconfigurable SRAM-based CAM architectures offer very high flexibility, accommodating BCAM, TCAM and logic-in-memory operations within the same unified arrays.

Advanced CNTFET and 10T/11T SRAM-CAM structures achieve improved search throughput, lower sensing latency, and better leakage suppression at low voltage. In addition, soft-error resilient FPGA TCAM architectures and adaptive sense amplifier techniques improve reliability in nanoscale and radiation-prone environments [114]. These developments jointly make SRAM-based CAM and TCAM systems important building blocks for future AI

accelerators, secure communication processors, edge computing platforms, and memory-centric computational architectures.

A comprehensive literature survey of state-of-the-art SRAM, CAM, and TCAM architectures shows an on-going evolution of memory design techniques driven by aggressive CMOS scaling, increasing data-centric workloads, and the increased demand for energy-efficient edge computing systems. Conventional 6T SRAM structures suffer from severe limitations in nanoscale technologies such as reduced static noise margin (SNM), increased leakage current, half-select instability, degraded writability and high sensitivity to process-voltage-temperature (PVT) variations. Such challenges are even more critical in ultra-low-voltage and sub-threshold operating regimes where it is difficult to ensure reliable memory functionality without architectural changes.

2.5 KEY OBSERVATIONS FROM THE LITERATURE REVIEW

The detailed literature survey on SRAM, CAM and TCAM architectures points to a clear technology shift from the conventional memory based systems to highly optimized low power associative computing architectures [45]. The surveyed works collectively indicate that aggressive CMOS scaling below 65 nm has made the challenges of leakage current, process variation, thermal noise, read disturbance, and voltage instability increase dramatically [48]. Thus, 8T, 9T, 10T and 11T cells with higher transistor counts have emerged as promising candidates to replace the traditional 6T SRAM cells for reliable operation at low voltages. The review further shows that future memory systems will increasingly rely on hybrid SRAM-TCAM architectures supporting stable storage, low-power search, and in-memory computation simultaneously [89].

One of the most important findings derived from the review is that conventional 6T SRAM cells exhibit severe stability degradation at near-threshold and sub-threshold operation. Threshold voltage variations and reduced transistor overdrive cause a drastic decrease in static noise margin (SNM) at lower supply voltages [62], as demonstrated in previous studies. The impact of random dopant fluctuation and process mismatch on the cross-coupled inverter stability in the deeply scaled technologies is studied which results in an increased probability of bit error and read failure. The literature also suggested that read disturbance becomes a major limitation since the same access transistors are used for storage and read operations.

These observations highlight the requirement for robust operation of isolated read-path SRAM architectures under aggressive voltage scaling [11].

A major technical finding of the survey is that isolated read mechanisms greatly improve the reliability and operational stability of SRAM. Most of the state-of-the-art 8T and 9T SRAM architectures use separate read transistors to disconnect internal storage nodes from the read bitlines during the sensing operation. This isolation prevents destructive read upset and greatly improves read SNM. Differential-read 8T SRAM cells exhibited substantial improvement in sensing margin compared to conventional 6T structures [75], particularly at supply voltages below 0.5 V. Some designs reported better half-select immunity due to isolated read paths that reduce spurious voltage fluctuations on neighbouring cells during simultaneous array operation [79].

Literature suggests that 8T SRAM architectures are among the best solutions for ultralow-voltage operation and improved stability. Most 8T SRAM cells employ dedicated read ports, differential sensing structures, or dynamic feedback control techniques to improve robustness [82]. Experimental studies have shown stable operation in the sub-threshold region, with a dramatically reduced probability of read failure. Dynamic feedback assisted 8T SRAM structures further improved writability and still kept read stability. Several works also showed that 8T architectures have better tolerance against process-voltage-temperature (PVT) variations because of isolated read circuitry which lessens the direct disturbance of storage nodes [115].

It is also important to note that the 8T SRAM architectures are gaining popularity for non-storage applications. The recent works have shown the 8T SRAM arrays for enabling multiply-and-accumulate (MAC) operation, dot-product calculation, and in-memory processing for AI acceleration [16]. Current-mode SRAM architectures with configurable bit precision were shown to be able to support neural network computation with reduced data transfer overhead [117]. Our results show that 8T SRAM cells can be very well suited for edge-AI systems and computing-in-memory architectures requiring both stability and computational capability [118].

Furthermore, the literature review shows that 9T SRAM architectures are a good trade-off between leakage reduction, writability improvement and low power operation. Most 9T SRAM structures use single-ended sensing schemes with isolated read/write paths to minimize switching power and enhance stability [119]. The single ended operation greatly

reduces the bitline capacitance charging and discharging activity and hence the dynamic power dissipation [120]. Some of the reported 9T SRAM cells were found to reduce the standby leakage current by stacking of transistors and optimized pull-down network configurations. Leakage reduction is particularly important in near-threshold and sub-threshold applications, where the standby power dominates the total power consumption [121].

One key technical finding is that single-ended 9T SRAM architectures can enable energy savings with little loss of sensing reliability. Reported works showed better read performance and improved write margin with lower switching activity when compared to differential structures. In some cases 9T SRAM cells succeeded at operation under supply voltage as low as 350 mV to 400 mV with acceptable stability margins [122]. Near-threshold FinFET-based 9T SRAM architectures further improved electrostatic control and reduced leakage current by stronger gate-channel coupling. These works collectively show that 9T SRAM cell is highly promising for energy-constrained applications such as biomedical applications, IoT systems and low-power embedded processors [123].

We also observe that half-select disturbance remains an important problem for high density SRAM arrays. Simultaneous access to row and column may cause a voltage fluctuation in non-selected cells to change the value of stored data. Different 8T and 9T SRAM architectures proposed in literature have realized half-select-free operation using isolated access mechanisms and dedicated write-assist circuitry. Significantly improved the operating reliability of array-level read and write operations by these techniques. Among them, Schmitt-trigger assisted SRAM architectures exhibited better tolerance against noise and process variation in ultralow-voltage operation [124].

The review also highlights the growing importance of the higher transistor-count SRAM architectures like the 10T and 11T cells for logic-in-memory and associative computing applications [125]. The 10T SRAM designs have achieved improved leakage suppression and higher yield through fully differential operation and isolated sensing circuitry. Likewise, 11T SRAM cells were equipped with built-in read/write assist mechanisms, enabling ultralow-voltage operation with lower failure probability [126]. Some 11T architectures also provided dual-direction logic execution and CAM capability in the same memory array [127]. These results clearly demonstrate that SRAM cells are evolving to be multifunctional computational memory units rather than simple storage elements [128].

The survey also highlighted the increasing integration of emerging transistor technologies such as FinFETs, CNTFETs, tunnel FETs and nanosheet CMOS devices in SRAM architectures. The improved electrostatic control of FinFET based SRAM cells results in better sub-threshold slope and lower leakage current. The switching performance of 8T SRAM cells based on CNTFETs was faster and the energy efficiency was improved due to the higher carrier mobility and the reduced short-channel effects. More recent implementations of nanosheet SRAMs with supply voltages around 350 mV show stable low-power operation for mobile and edge-AI applications [129]. These developments show that innovation at the device level is an enabler for future ultralow-power SRAM architectures.

The literature review of CAM and TCAM architectures presented that the main problems of associative memory systems are high power consumption of search-line and match-line. Parallel search operations lead to high dynamic energy dissipation due to large capacitive switching activity over the array [130]. Conventional TCAM architectures also have large sensing delay and increased leakage current due to continuous precharge-discharge operation of match lines. As the size of the array increases, these problems are magnified. Several reported works attempted to reduce the search energy using selective activation schemes, low-swing sensing, current-race mechanisms and pre-computation techniques [131].

An important lesson learnt from the TCAM literature is that SRAM-based TCAM designs provide significant gains in terms of flexibility and scalability over traditional dedicated TCAM implementations. Reconfigurable SRAM arrays that could act as BCAM, TCAM, logic-in-memory units and similarity indexing engines showed the feasibility of multifunctional memory platforms [132]. The integration of associative search and logic execution in standard SRAM arrays was shown to be feasible in recent reconfigurable SRAM-CAM architectures without substantial architectural overhead. The results from these studies suggest that the use of SRAM-based associative computing frameworks will be more prevalent in future computing systems to reduce memory access bottlenecks [133].

Another key technical finding is that single-ended CAM architectures reduce search energy significantly. Experimental results show energy efficiencies as low as 1.22 fJ/bit/search at operating frequencies of 200 MHz in optimized single-ended CAM cells [134]. The low power reduction is mainly due to minimized switching activity and reduced match-line capacitance [135]. This low-energy search operation is very beneficial for edge-computing and AI acceleration systems with frequent associative search operations [136].

The literature also shows that the emerging dominant design considerations for SRAM-based TCAM systems are process variation and soft-error resilience. The associative search accuracy and storage reliability can be severely affected by radiation-induced transient faults and threshold voltage variation. Several reported architectures have included multi-node upset tolerance, error-correcting schemes, and robust sensing circuitry to enhance reliability in harsh operating environments [137]. These results are of special interest for aerospace and secure computing applications, where fault tolerant operation of the memory is a must.

The most important conclusion from the entire literature review is that no single SRAM architecture alone can satisfy all the design requirements with respect to stability, leakage reduction, speed, power efficiency and associative computing capability [138]. 8T SRAM cells offer good read stability and half-select immunity but present moderate area overhead. Similarly, 9T SRAM architectures offer low-leakage single-ended operation and better writability at the cost of increased circuit complexity [87]. Higher transistor count structures such as 11T SRAM cells allow for logic-in-memory and associative computing, but this also increases the number of transistors and parasitic capacitance [58].

This comparative understanding is a strong motivation for developing a hybrid alternate SRAM-TCAM array architecture using heterogeneous SRAM cells such as 8T, 9T and 11T structures within the same memory framework [11]. The literature strongly advocates hybrid organization with alternate rows, as a means of simultaneously exploiting the advantages of multiple SRAM topologies [139]. In such an arrangement, 8T SRAM rows offer improved read stability and half-select immunity, 9T SRAM rows enable reduction of leakage power and search-line switching activity through single-ended operation, and 11T SRAM rows facilitate associative logic and in-memory computation [140].

The review also shows that the hybrid SRAM-TCAM architectures can considerably reduce the total match-line power dissipation by using selective sensing techniques along with isolated search paths. Since 8T and 9T cells inherently decouple the storage nodes from the search operations [42], destructive search disturbance can be reduced greatly. Furthermore, heterogeneous SRAM integration may improve the tolerance against PVT variations, as different cell structures distribute the sensitivity to variability across the array. Such hybrid architectures are thus expected to deliver improved search reliability, reduced leakage current, increased operational stability and better scalability to future nanoscale associative memory systems [54].

In summary, this literature review has clearly proven that hybrid SRAM-TCAM architectures with alternate 8T, 9T and 11T SRAM cells represent a very promising research direction for next generation low power associative computing systems [58]. The combination of isolated read paths, single-ended sensing, logic-in-memory, leakage-aware operation, and variation tolerance can achieve an optimized balance between power dissipation, stability, search speed, and computational flexibility. The insights motivate the proposed research toward the development of energy-efficient, variation-tolerant and high-performance hybrid SRAM-TCAM arrays for applications in edge-AI acceleration, secure communication, networking hardware, aerospace electronics and intelligent computing platforms.

CHAPTER-3
LOW VOLTAGE DUAL PORT SRAM CELL FOR LOW POWER APPLICATIONS

3.1 INTRODUCTION

The integration of artificial intelligence and machine learning algorithms in SoC platforms greatly improves the operational reliability, computational efficiency, and adaptability of today's smart devices. The rapid proliferation of IoT-enabled applications has resulted in a substantial increase in the computational burden on embedded SoC processors, thus the need for high-speed on-chip cache memories to facilitate efficient and low latency data processing [14]. At the same time, semiconductor technology is constantly moving towards deep nanometer scale fabrication nodes in order to achieve ultra-compact designs with improved energy efficiency and longer battery lifetime [4]. In accordance with Moore's law, the feature dimensions of the ultra-large-scale integration (ULSI) nanoelectronics devices are continuously scaled down to improve the device density and integration capability [52]. However, aggressive technology scaling and supply voltage reduction of SRAM cells to minimize power dissipation causes several critical design challenges such as process-voltage-temperature (PVT) variations, reduced stability margins and reliability degradation in deep sub micrometer regimes [51].

Static power dissipation during standby or hold operation is a large component of the total power consumption in SRAM arrays [141]. Reducing the supply voltage (VDD) is a valid approach to reducing energy consumption but can adversely affect the operational stability of memory cells and can lead to a significant increase in the bit error rate (BER) [69]. Therefore, it is a critical challenge in the design of advanced SRAM architectures for next generation electronic systems to strike the right balance between power efficiency, performance and reliability. Moreover, the goal is to design SRAM cells with a minimum number of transistors to maximize the memory density. But, with the scaling down of the transistor size, the process variability dominates due to the fluctuations of parameters such as channel length, oxide thickness and doping concentration. Also, short-channel effects due to aggressive scaling result in exponential increase in the leakage currents, which leads to increased standby power dissipation of SRAM arrays. The reduction in operating voltage near the threshold region can reduce the overall power consumption, but at the same time it causes stability and performance limitations [149]. The total power consumption of an SRAM cell

has two components: static and dynamic. The static power varies linearly with the supply voltage, while the dynamic power varies with V_{DD} [55].

In this chapter, two dual bit-line SRAM bit-cell architectures are designed, these are; an eleven-transistor (11T) SRAM cell and a nine-transistor (9T) SRAM cell. Both configurations are specially designed for low power operation while ensuring reliable operation under reduced supply voltage conditions (> 1 V). The proposed 11T SRAM cell is designed in 32 nm CMOS technology and operates at low supply voltage of 500 mV. The cell shows better stability characteristics with read and hold static noise margins (SNMs) of 184 mV and 197.26 mV respectively whereas the write SNM is found to be 265mV. Monte Carlo simulations were performed to verify the robustness against process variations under 3σ global process variation with a sample size of 5000. The simulation results demonstrate significant improvements in read and hold stability margins. Moreover, the proposed 11T bit cell is operated with low power dissipation in all operation modes.

The proposed 9T (P9T PS) SRAM cell is also designed with 32 nm CMOS technology and working at a supply voltage of 0.9 V. The proposed cell is verified and improved in terms of different performance characteristics with an extensive analysis under various operating conditions. The read and hold SNMs of the cell are 0.368 V and 0.364 V, respectively, and the write SNM is measured to be 0.422 V, showing better noise immunity and operational stability. Furthermore, the proposed P9T PS SRAM cell has been comparatively characterized with respect to the existing single-port and dual-port 9T SRAM topologies. The comparative analysis shows the superiority of the proposed design in terms of noise immunity, temperature variation tolerance, static and dynamic power dissipation, power-delay product (PDP), SNM-to-PDP ratio, silicon area efficiency, and overall electrical quality metrics. Moreover, the cell operates energy-efficient in all operating modes with significantly reduced power consumption. The following objective is framed here to obtain a low power, dual port SRAM cell:

“To design and analyze a low power dual-port SRAM bit cell for low voltage operations.”

To attain this objective, primarily various SRAM cells are simulated and analysed at a same technology node and supply voltage. The aim of this chapter is to design a low power and low voltage dual port SRAM bit cell for reduced leakage power and enhance stability. The prime focus was to reduce the technology node and the supply voltage for higher transistor

count SRAM cell. Another consideration was to further reduce the overall power consumption of the cell keeping the other specifications constant.

The structure of this chapter is as follows; an introductory overview and motivation for the proposed work is illustrated in section 3.1. This is followed by a comparative review of the existing dual bit-line SRAM bit-cell architectures with different transistor configurations and various 9T SRAM cell architectures with different techniques and topologies, in section 3.2. Then, the detailed design and operation of the proposed 11T and the proposed 9T SRAM cells including circuit topology, transistor sizing and functionality analysis are illustrated in section 3.3 and 3.4, respectively. Furthermore, a comprehensive performance evaluation of the proposed cells in terms of different design metrics and compares the obtained results with the reported ones in the literature is represented in section 3.5 and finally the section 3.6 summarizes the analytical and simulation-based results.

3.2 SRAM ARCHITECTURE DESIGN TECHNIQUES AND VARIATIONS

The conventional 6T SRAM cell persists as the most popular cell due to its small size, high packing density and fast access speed but suffers from low read stability, high leakage current and low noise margin as the technology scales down. In the recent literature, several modified SRAM architectures have been proposed to overcome these limitations, ranging from 7T to 11T cells. These architectures add additional transistors to enable features such as separate read/write paths and reduced bit-line switching activity, increased write ability, lower standby leakage, and improved immunity to process, voltage, and temperature variations. The 7T and 8T SRAM cells are mainly focused on improving the read stability and reducing the dynamic power consumption.

The 9T, 10T, and 11T configurations provide stronger data retention capability, better robustness during the read/write operations, and reliable sub-threshold operation for ultra-low-power applications. Furthermore, advanced SRAM topologies are attracting more attention for cache memories, IoT devices, machine learning accelerators, and TCAM-based search architectures, where high speed, low energy consumption, and stable operation are key design requirements. In this section, various SRAM architectures ranging from 7T to 11T cells are discussed along with the modifications in their structures, working principles, advantages and performance trade-offs. This section of the paper provides a comparative review of the proposed11T cell with existing SRAM cells.

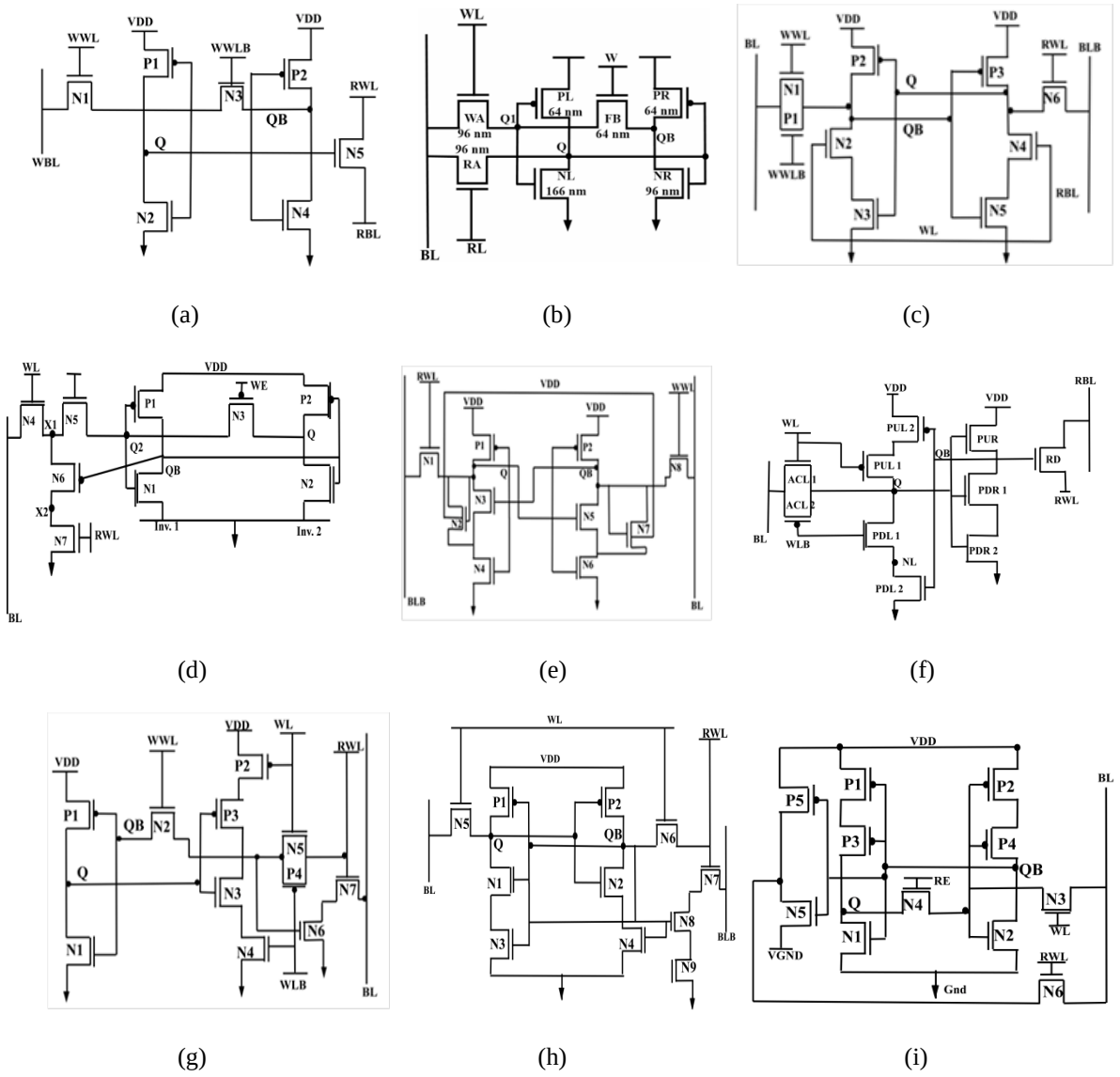


Fig. 3.1. Schematic representation of (a) $7T_1$, (b) $7T_2$, (c) $9T_1$, (d) $9T_2$, (e) $10T_1$, (f) $10T_2$, (g) $11T_1$, (h) $11T_2$, and (i) $11T_3$.

Over the past few years, numerous SRAM bit cells have been designed by researchers to fulfill the design requirements of consumers, such as minimizing bit cell area, operating at lower voltages, improving static noise margins for operations like hold, read, and write, and reducing timing specifications. This review is conducted in two ways: (i) with the same transistor configuration cells (11T cell), and (ii) with different transistor configuration cells such as 7T, 9T and 10T SRAM cells. The schematics of all the transistor configuration SRAM cells are demonstrated in Figure 3.1 (a - i). However, as technology nodes shrink and V_{DD} scaling is performed, the performance of the cell tends to degrade. One major concern with the 6T bit cell is its differential nature, which leads to increased leakage, often considerably high.

3.2.1 Dual Port SRAM Cells:

The $7T_1$ SRAM cell represented in Figure 3.1(a) [61] by Rawat *et al.* developed a cell suitable for 32nm technology having 1R1W bit interleaving and eliminating half select issues. $7T_2$ SRAM cell represented in Figure 3.1(b) [62] by Rawat *et al.* offers a high-performing 7T SRAM cell with enhanced read stability that is intended for ultra-low voltage operation. Their creative strategy shows notable improvements in SRAM dependability and efficiency. $9T_1$ SRAM cell [55] represented by Gupta *et al.,* addresses the challenges in designing the SRAM cell by implementing isolated read and write operations in low power mode while minimizing the power consumption, and $9T_2$ SRAM [11] cell by Singhal *et al.* present a 9T SRAM cell design that is single-ended and single-port, which greatly improves stability.

Through the constant efforts of various researchers, the architecture of SRAM cells has been significantly improved for increased reliability, represented by figures 3.1(c) & (d), respectively. $10T_1$ SRAM cell [63] represented in figure 3.1(e) by Krishna *et al.,* highlights the significance of innovative design technique that eliminates the problems of SRAM cells in deep submicron technologies The main challenge given in their work was optimizing technology node. Also, $10T_2$ SRAM cell [9] represented in figure 3.1(f) is a single-ended 10T SRAM cell with excellent low leakage and low voltage functioning and high yield is presented by Eslami *et al*. Their architecture provides a solid answer for SRAM applications that require low power consumption. Transistor sizing of different SRAM cells is summarized in Table 3.1.

Table 3.1. Transistor sizing of different SRAM cells

TRANSISTOR (S)	**WIDTH/LENGTH RATIO (W/L)**								
	$7T_1$	**7T2**	**9T1**	**9T2**	**$10T_1$**	**10T2**	**11T1**	**11T2**	**11T3**
P1, P2	3:1	2.5:1 (PL,PR)	2:1, P3= :1	3:1	2:1	3:1 (PUL2, PUL1)	5:1 & P3	2.5:1	2:1
N2,N4	1:1	1:1 (NL,NR)	1:1, & N4, N5	1:1	1:1	1:1	2.5:1, N1 & N3	1:1, N1	1:1, N1 & N3
ACCESS TRANSISTORS	1.5:1	1:1	1:1	1.5:1	1:1	2:1	2:1	1:1	1:1

The $11T_1$ SRAM cell represented in figure 3.1(g) [11] by Lorenzo *et al.,* proposes a single line architecture that reduces area and power over heads. The $11T_2$ SRAM cell [64] by

Sargunam *et al.*, achieves great performance and low power consumption while improving energy efficiency. Their design shows notable gains in both operational effectiveness and reliability [60], shown in figure 3.1(h).Despite the increase in transistor count, the 11T SRAM cell still provides refined read and hold stability over the existing cells. For static random access memory cells, bit lines require maximum power for charging and discharging [17] procedures during write and read operations.

3.2.2 Different 9T SRAM Cell Architectures

Several new topologies between 6 and 14T have been put forth to address the aforementioned issues. They include differential write, differential read and single-end read single-end write. In addition, a number of approaches have been examined for reducing power dissipation while maintaining control over other parameters and improving access time and stability. In order to improve read and write noise margins simultaneously, these techniques include the read assist circuit [54], the write assist circuit [55], the decoupling of read and write ports [15], and the loop-cutting approach [18]. A 9T SRAM cell ($9S_1$) was suggested by Mishra *et al.* [59] in order to improve read margin while requiring less read power, shown in figure 3.2 (a). However, 9T static random access memory (SRAM) cell with a tail transistor for power conservation and a single ended isolated read bit line with a 2T read port for increased stability.

The storing node voltage in the suggested design has not changed during active mode operation since distinct bitlines are used. Due to the stacking of the internal latch and tail transistor, the static power dissipation of the SRAM cell has been significantly lowered in the idle (hold) mode [121]. Additionally, A 9T SRAM cell ($9S_2$) was proposed by Singhal *et al.* [53] reduced power consumption because of the single bitline, improved write margin because of the disconnected feedback link, stronger read stability because of the isolated read port, and resistance to soft mistakes because of the architecture that is free from half-select disturbances. On the other hand, this cell used more energy when reading, and is showcasing better stability for noises.

Because of the decreased activity factor and broken feedback channel between the cross-coupled inverters during write operations, our suggested bitcell has lower write-power consumption. Roy *et al.* [58] described the 9T SRAM cell ($9S_3$) as having a reduced write power and a 9-MOFTET static random-access memory cell that is resistant to fluctuation [122]. The breakdown of the feedback channel during the writing of a little amount to the

storage node is what allows for these gains. The impact of variations in process-related factors and environmental parameters, such as supply voltage and temperature, is thoroughly examined in this work. Another 9T cell ($9S_4$) is designed by Roy *et al.* [57] which operates at lower voltages and possess less leakage current. The proposed bit cell's bit-interleaving design was explained to explain the elimination of the half-select issue. The cell also showed a reasonable degree of adaptability to changes in the process. Lorenzo *et al.* [60] suggests ground-breaking 9T-SRAM architecture ($9D_1$). It creates an SRAM cell by deftly combining source biasing with the body-bias control approach. There are nine transistors in the suggested cell, each having its own read/write interface. Two tail transistors in a pull-down path and a read word-line based body bias controller are used to increase the design metrics. The suggested architecture's primary goal is to decrease read/write latency [98], increase stability, and minimise leakage current [86] in an SRAM cell.

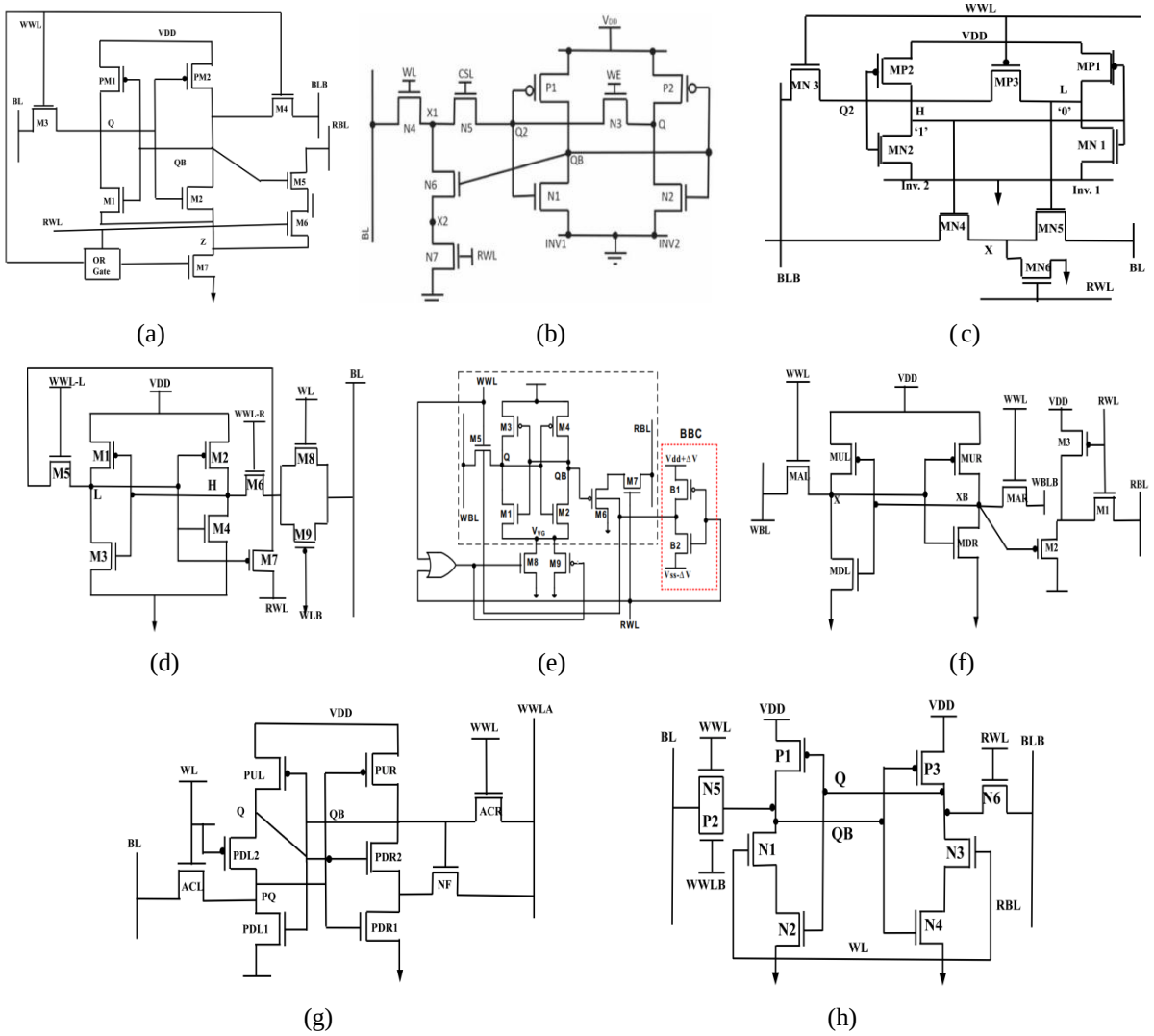


Fig. 3.2. Schematics of different reported 9T SRAM bit cells (a) $9S_1$, (b) $9S_2$, (c) $9S_3$, (d) $9S_4$, (e) $9D_1$, (f) 9D2, (g) $9D_3$ and (h) $9D_4$.

Gupta *et al.* [56] proposes a 9T SRAM cell ($9D_2$) unique read port is suggested, with the goals of wide RBL voltage swing in the vicinity of the threshold and sub-threshold regions, high ION/IOFF ratio, and low and data-independent leakages. To show the suggested cell's superiority over others, its performance at 32 nm technology node is compared with 7T, 8T, 9T, and 10T cells by simulating a column of 128 cells. Moreover, the cell handles the half-selected issue similarly to [12]. The revised version in reference [13] specifically mentions IoT applications and employs the stack transistor approach to significantly reduce leakage. Abbasian *et al.* [54] propose a 9T cell Single-bit line 9T low-leakage SRAM cell ($9D_3$). The read-disturbance problem is absent from the suggested architecture, and the writing "1" problem is resolved. Gupta *et al.* [55] addresses the challenges in designing the SRAM cell by implementing isolated read and write operations in low power mode while minimizing the power consumption and proposes a 9T SRAM cell ($9D_4$). A few additional investigated approaches for creating SRAM topologies that maintain stability while power dissipation decreases are swing voltage control [78], read buffers [34], and sleep NMOS [68]. In particular, topologies that use single-ended read or write techniques are used to minimise chip space and limit switching and leakage power. Despite this, this method has longer read/write times.

Additionally, in single-ended techniques, write and read sensing capacity further decreases with scaling in supply voltage in the presence of process variability [16, 11]. This might be because there isn't a complementary bit-line. The schematics of different 9T SRAM cells are demonstrated in figures 3.2 (a-h). A few single-ended write and read topologies with different assistance strategies were developed in order to solve this problem [115]. However, in order to put these aids into practice, silicon area is required, which is regarded as a significant trade-off, as evidenced by the present desire for larger memories and smaller devices [123]. The SRAM cells mentioned in figure 3.2 are taken for reference and comparison purposes, all these cells are reported from last few years. All these reported cells are re-simulated at 32nm for creating common platform for comparison with the P9T (PS) SRAM cell.

3.3 PROPOSED DESIGN FOR 11T SRAM CELL

The proposed 11T SRAM cell is designed to accommodate dedicated read and write ports, operating individually for read operations and write operations [20]. The basic structure of the proposed 11T cell comprises of; two inverter pairs; inverter pair 1 consists of a PMOS (MP1) connected to V_{DD}, another PMOS (MP2) connected to the write Enable (WE) acting as

a switching transistor controlling the write path and one NMOS (MN2) forming the feedback path with first PMOS establishing the inverter's pull-down and feedback loop. The complementary inverter 2 is formed with a PMOS (MP3) and one NMOS (MN3). Cell has two distinct bit lines namely, Bit line (BL) and Bit Line Bar (BLB), serving as dual ports for the novel designed cell and are responsible for successful write and read operations of the cell, respectively. Operating at a lower voltage of 500mV, the proposed 11T SRAM cells is equipped with separate read and write paths for better noise immunity and overall isolation. Transistors MP4, MN6, and MN7 create a write access mechanism with dedicated write assist and control [22]. Along with these transistors the cell also has separate read and write word lines (RWL and WWL), and biltlines (RBL and WBL). Notable features of this bit cell include faster and differential sensing, smaller area footprint, and cost efficiency.

3.3.1 Operations of the Proposed 11T Cell:

Additionally, the cell includes two pairs of power-gated transistors, comprising a combination of PMOS and NMOS [22]. These transistors are directly linked to the word line, along with two individual bit lines (BL and BLB) for isolated operations, such as write and read operations, in any order. The schematic for the proposed design (11T) is depicted in Figure 3.3. In order to maximize power efficiency and minimize leakage while the cell is in standby or hold mode, power gated transistors are integrated into the design of the 11T SRAM cell. These transistors reduce power usage by selectively switching off the power supply to particular SRAM cell components when they are not in use [124]. The power gated transistors in the 11T SRAM cell are arranged in a certain way to regulate the power supply to specific parts, including the inverters and access transistors, depending on the cell's operational state [125]. When the cell is not actively executing read or write operations, these power gated transistors are turned off, thereby isolating the memory core from the power supply.

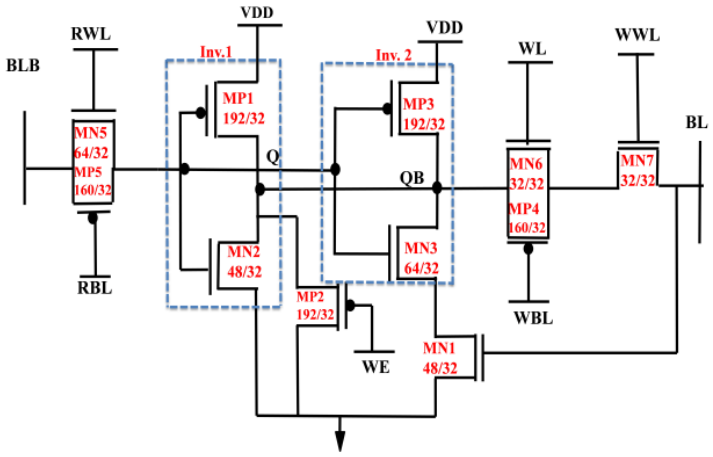


Fig. 3.3. Schematic for 11T SRAM bit cell with transistor aspect ratios.

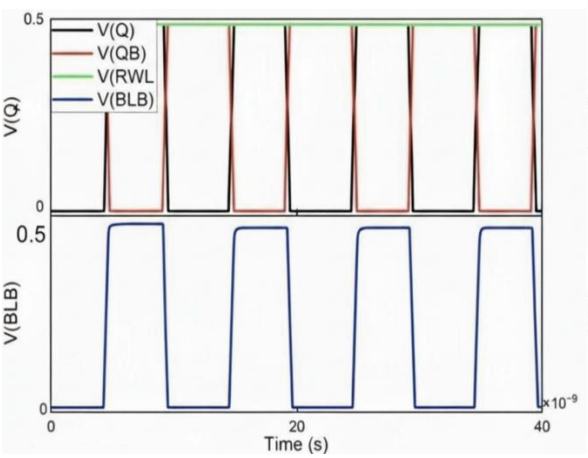
Power gated transistors were used in the 11T SRAM cells are highly energy-efficient since they can drastically lower their usage of standby power. This 11T SRAM cell is created and tuned to overcome the difficulties found in complementary metal-oxide-semiconductor (CMOS) technology. This is crucial for contemporary low-power applications, because lowering power consumption is necessary to increase battery life and lower total energy consumption. Furthermore, power gated transistors are used to reduce leakage current problems in nanoscale CMOS technology, which improves the SRAM cell's overall performance and reliability. In summary, this research suggests an 11T SRAM cell with two ports and low voltage that offers better stability for read and hold functions. In order to maintain data integrity, the WE (Write Enable) signal is crucial in determining whether or not the core storage nodes are permitted to communicate with the write bitline network. A controlled discharge or charging path from the write bitline to the internal latch nodes is made possible when WE = High activates the specialized write-access transistor stack linked to WWL. By temporarily strengthening the external drive and enabling a fresh logic value to replace the previously stored state, this selectively disrupts the feedback dominance of the cross-coupled inverters. The write-access transistors are totally turned off when WE = Low. The aspect ratio and sizing of individual transistor is described in Table 3.2 below.

Table 3.2. Transistor Sizing for Proposed 11T SRAM cell

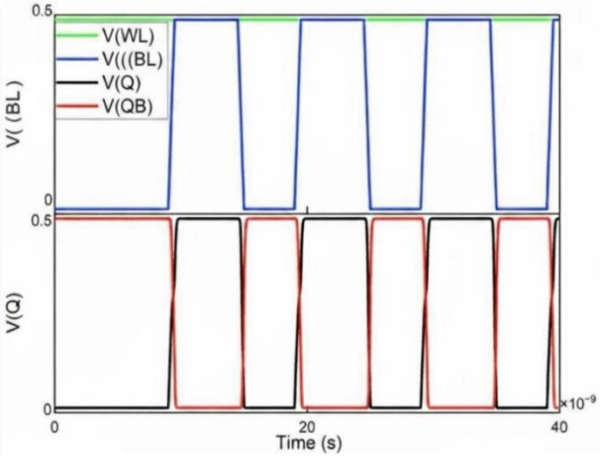
TRANSISTOR	WIDTH/LENGTH (W/L)	ROLE
MP1, MP3	192/32	PMOS pull-ups for inverters
MN2, MN3	48/32, 64/32	NMOS pull-downs for inverters
MN1	48/32	Read NMOS pull down
MP2	192/32	Read PMOS
MN5, MN6	64/32, 32/32	Write NMOS

MP5, MP4	160/32, 160/32	Read and Write assist PMOS
MN7	32/32	Write access NMOS

This effectively isolates the cell core from the write driver and guarantees that the internal inverter pair alone maintains the stored data, independent of the write bitline [118]. In this condition, the cell can safely switch to either read mode, where just the decoupling read-port transistors are enabled through RWL, enabling a differential read on RBL without affecting the internal data, or hold mode, where all access devices are OFF and no external node interacts with Q/QB [65]. WE ensure regulated write access, strong immunity against unintentional data corruption, and robust read stability by strictly gating the write-path while maintaining the read-path's independence [126]. Transient curves for the read and write of the proposed 11T cell are demonstrated in figures 3.4 (a & b), respectively. As the butterfly curves are required to showcase the stability of the cell efficiently; nevertheless, additional mathematical operations are needed to determine the current noise margin [127]. One disadvantage of the butterfly curve approach is that inline testers are not used. These limitations are overcome by the N-curve analysis, which may be used to determine read and write stability as well as voltage and current characteristics [11]. Operation modes, control signals and active transistors of proposed 11T SRAM cell is mentioned in Table 3.3.



(a)



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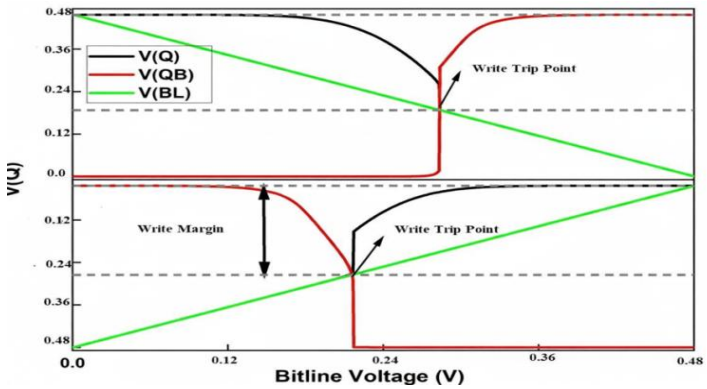


(c)

Fig. 3.4. Transient response for (a) read, (b) write operation and (c) write margin of 11T SRAM cell.

Table 3.3. Operation modes, control signals and active transistors of proposed 11T SRAM cell

MODE	CONTROL SIGNALS	ACTIVE TRANSISTORS	ROLE
HOLD/ STANDBY	WL = 0, RWL = 0	Cross-coupled inverter pairs (inverter 1 & inverter 2)	Data is maintained by storage nodes Q and QB via a feedback loop; bit lines are severed by turning off access transistors; transistor stacking results in little leakage.
WRITE	WL & WWL= 1, RWL = 0, BL = 1	Write access transistors (MN6, MP4 and MN7), MP2 and cross-coupled inverter pairs	Storage nodes are written with data from BL. By acting as a switching transistor to regulate the write path, PMOS on WE (left inverter) enables controlled data overwrite.
READ	RWL = 1, WL = 0, BLB = 1	MP5, MN5, MP2 and cross-coupled inverter pairs	BLB is precharged. RWL improves read stability by activating the read stack, which conditionally discharges RBL based on stored data without interfering with storage nodes.

Figure 3.4 (c) represents the transient response of the write margin of the 11T cell. The curve obtained from the bit-cell's VTC (Voltage Transfer Characteristics) display has only one point of intersection for a successful write operation [128]. When the data contained in the cell flips, the second approach involves sweeping the word line (WL) and detecting the WL voltage. The difference between V_{DD} and the WL voltage needed to flip the data is then used to calculate the write margin.

This study employs the Write Trip Point technique, in which the values of storage nodes Q and QB are monitored while the bit-line sweep is carried out. The write trip point is the highest bit-line voltage necessary to display a flip in the bit-cell's contents. The bit-cell's write stability increases when the write trip point value decreases because it becomes easier to write to the bit-cell. The write margin is determined by subtracting the write trip point from the V_{DD} [129].

Hold operation (Idle State)

When no read and write operation is being executed; WWL = 0, RWL = 0. MP1-MN2 and MP3- MN3 (the cross coupled inverter pairs) maintains the data stored at nodes Q and QB. MP5, MP4, MN6, MN7 are OFF, which is disconnecting the internal nodes from the bitlines. The read path is also kept OFF, providing complete isolation of the storage nodes from the bitline fluctuations. The internal storage nodes (Q and QB) are essentially isolated from the bit lines during the hold state since both the transmission gates (TG) attached to BL and BLB are switched off. To make sure there are no external disturbance routes, the write access

transistor is likewise disabled [130]. The pair of cross-coupled inverters only maintains the logic state in this scenario. Overall, this arrangement enhanced the data retention and static noise margins providing the isolations for read/write disturbances and leakage currents. To perform the hold operation for the P11T SRAM cell, either of the two bit lines, namely BL and BLB, is maintained high ('1'), while the other is kept low ('0').

Read operation

In order to prevent read disturbance and guarantee stable data retention at such a low supply voltage of 500mV, the P11T SRAM cell isolates the internal storage nodes (Q and QB) from the main bitline; BLB uses the dedicated read port. The read process primarily uses transistors MP2, MP3, MN5, and MP5 to form the read buffer and access path, as well as RWL, RBL, and BLB. While the read stack detects the logic state without upsetting the internal nodes, and the storage inverters (inv.1 and inv.2) preserve the stored data.

The bitline BLB is precharged to VDD ('1') via peripheral circuitry before to starting the read. RBL, the internal read node with MP5 and MN5 at the bottom of the read stack, is at low or logic '0'.The storage nodes are completely isolated from the external bitline since RWL is kept low, guaranteeing that MN5 and MP5 stay off. Through the cross-coupled inverter pair, the internal storage nodes Q and QB preserve the logic levels that were previously stored. This prevents disruption and guarantees that the bitline voltage change will only reflect the stored data when RWL is later asserted. Before initiating the read, the bitline BLB is precharged to VDD (‘1’) through peripheral circuitry.

Table 3.4. Input signals for hold, read and write operations of proposed 11T SRAM cell

Signals	HOLD (Standby)	READ	WRITE
WE	L	L	H
RWL	L	H	L
RBL	P (precharged)	P (HIGH)	Isolated
WL/WWL	L	L	H (WWL asserted)
BL	X	L	D (data)
BLB	X	H(asserted)	D (complement)
ROLE	Cell will retain the data; read and write paths are disabled (low power).	RWL=H enables read stack; RBL precharged then conditionally discharged. WE=LOW ensures write path & assists are disabled to avoid disturbance.	WE/ WWL=H enable write path. BL/BLB driven to desired data before asserting WWL/WE. RWL must be L (read disabled) to avoid contention with RBL

RBL, the internal read node at the bottom of read stack consisting MP5 and MN5, is at low or logic ‘0’.RWL is held low, ensuring that MN5 and MP5 remain off, fully isolating the storage nodes from the external bitline. The internal storage nodes Q and QB maintain the previously stored logic levels through the cross-coupled inverter pair. This ensures that when RWL is later asserted, the bitline voltage change will purely reflect the data stored, and avoids disturbance. MP5 and MN5 are turned "ON" when the read operation starts because the RWL is driven high. This creates the conduction channel for the RBL by joining the precharged bitline to the read port's internal node. Read "1" (Q = 1, QB = 0), pulling Q equals VDD while keeping MP1 off and MN2 on. Pulling QB equals zero when MP3 is left on and MN1 is turned off. MN3 stays off when MP2 is linked to VDD. The precharged BLB stays at VDD since there is no current passing through MN5-MP5. Read "0" (Q = 0, QB = 1), holding Q equal to 0 while keeping MP1 on and MN2 off. MN1 is pulling QB to VDD while MP3 is kept off. During read, WE activates MN3, creating a conductive channel from RBL to ground. BLB to MN5 to MP5 to MP2 to MN3 to ground is the entire current path flow. BLB can discharge progressively along this path, resulting in a voltage decrease.

Write operation

To updated the stored value of the cell or change the values stored at nodes Q and QB the write operation is carried out. Firstly, WWL is kept at logic ‘1’ or HIGH, enabling write access path via transistors MN7, MN6 and MN4. And assert the BL =1. Write bitlines WL, WBL are driven with desired data. For writing Q = 0; WL = 0, WBL = 1, which activates MN6 and MP4 transistors. MP4 pulls Q to low while MN7 pulls QB high.mFor writing Q = 1; WL = 1 and WBL -= 0, which activates MP4 and MN6 to raise Q and MN5 is OFF providing an overall isolation and write assist path. Transistors MP6 and MP4 are PMOS write assist drivers that supports flipping the state when the operating voltage, VDD is low (500 mV). Asymmetric sizing ensures these transistors can overpower the feedback inverters momentarily to allow a new value to be written on the storage nodes.

In conclusion, the P11T SRAM cell offers improved performance, dependability, and efficiency over previous designs, marking a substantial improvement in SRAM technology. It is ideal for a variety of memory applications due to its creative architecture and well-balanced characteristics, especially in high-performance and low-power computer systems. A

disruptive read operation occurs when writing when the bit-line is actively charged at V_{DD} [157]. Input signals for hold, read and write operations of proposed 11T SRAM cell are summarized in Table 3.4.

3.4 PROPOSED DESIGN FOR 9T (P9T PS) SRAM CELL

In the proposed architecture, transistors M2 and M3 form the core latch structure with transistors M4 and M5. Read (RL) and write (WL; WBL) signals, respectively, gate control access transistors M1 and M9. Additionally, to the q and q_bar nodes, respectively, an extra pair of transistors forming an inverter using M7 & M8 transistors is deployed in the design to accommodate parallel processing or simulation for the cell. Transistor M1 is only active when reading; it is off when writing and in standby mode for the projected topology [158]. The control signal read (CSR: BL & RL) are connected to the gate node of the M1 & M9 transistors [131]. During read and hold activities, the CSR signal stays on logic "high," and during write operations, its counterpart stage is employed. When reading, the suggested circuit operates in differential mode; when writing, it operates in single-end mode. Table 3.5, suggests that during a read operation, all control signals are maintained at logic 'high'. Figure 3.5 (a) shows the schematic depiction of the proposed P9T PS SRAM circuit. Figure 3.5 (b, c), respectively, shows the active and idle devices during read and write operations of the suggested topology. The read/write/standby control signal status for the suggested circuit is listed in Table 3.5. As seen in figure 3.5(b), the suggested architecture operates in differential mode during read operation.

3.4.1 Write Mode

During write operation, word line (WL) is enabled which turns ON the transistor M6 and the data present on the BLB is transferred to the internal storage node q_bar. Regenerative storage of the written data is achieved at nodes q and q_bar by the cross-coupled inverter pair consisting of PMOS transistors M2 and M4 and NMOS transistors M3 and M5. If BLB is driven high, then node q_bar is logic '1' and node q is logic '0'. On the other hand, when BLB is low, node q_bar stores logic ‘0’ and node q stores logic ‘1’. Since the transistor M6 controls the write path, the write operation can be done efficiently with less disturbance to the stored data. For instance, the read stack transistor M1 provides the discharge channel to the M6 transistor during the read process [132].

When modifying a bit in a topology that employs differential mode of operation for SRAM cell write operations, one must enforce the modifying bit on that specific node and impose its complimentary bit on the other side of the latch. Enforcing write operation in a single-ended writing mechanism, particularly during the write '1' operation, is a difficult task [6, 24]. The suggested topology uses a single-sided write operation without using a write aid circuit [133] As a result, one of the feedback loops is rendered inoperable and the write access transistor, WL is maintained strong enough to accomplish the intended write operation. By keeping the CSR signals low, the M1 transistor is turned off, weakening the feedback loop.

Table 3.5 Input signals for P9T (PS) SRAM cell.

Input	**Hold**	**Read**	**Write-0**	**Write-1**
RL	1	1	0	0/1
WL	1	0	0/1	0/1
BL	0/1	1	1	0
BLB	1	1	0	0/1
WBL	1	0	0/1	0/1

3.4.2 Read Mode

In the read operation, the read line (RL) is activated to turn ON transistor M1 and the write word line (WL) is disabled to isolate the storage nodes from the write path. The read circuit (M7, M8 and M9) reads the stored data without affecting the internal nodes directly. Typically, the read bit line BL is pre-charged before the read operation. The conduction path through M7-M9 either discharges or holds the voltage on the read bit line depending on the value stored at node q_bar. When q_bar stores logic ‘1’, the read discharge path is activated by discharging the BL through the corresponding transistors. When the q bar stores logic ‘0’, then the discharge path is OFF and the bit line that is precharged maintains its voltage level.

The proposed 9T SRAM cell provides significant enhancement in read stability, less read disturb issues and low power operation due to the separation of read and write paths. Here, in this P9T (PS) architecture, the read operation is carried out by switching the access transistor M1, “ON” and keeping RL high. While to carry out the write operation of the cell, this architecture has an extra inverter consisting two transistors namely, M7 & M8, which acts as a switch for simultaneous operation within the cell resulting in parallel processing. The inverter pair M7 & M8 is governed and controlled by WBL. Access transistor M9 is controlling the write operation of the cell. Together, these elements improve overall performance in these voltage ranges (0.4 - 0.9 V). Data can be retrieved at the bit level in

parallel within each SRAM cell. This implies that many bits can be read or write simultaneously (usually 8 bits or more, depending on the architecture).

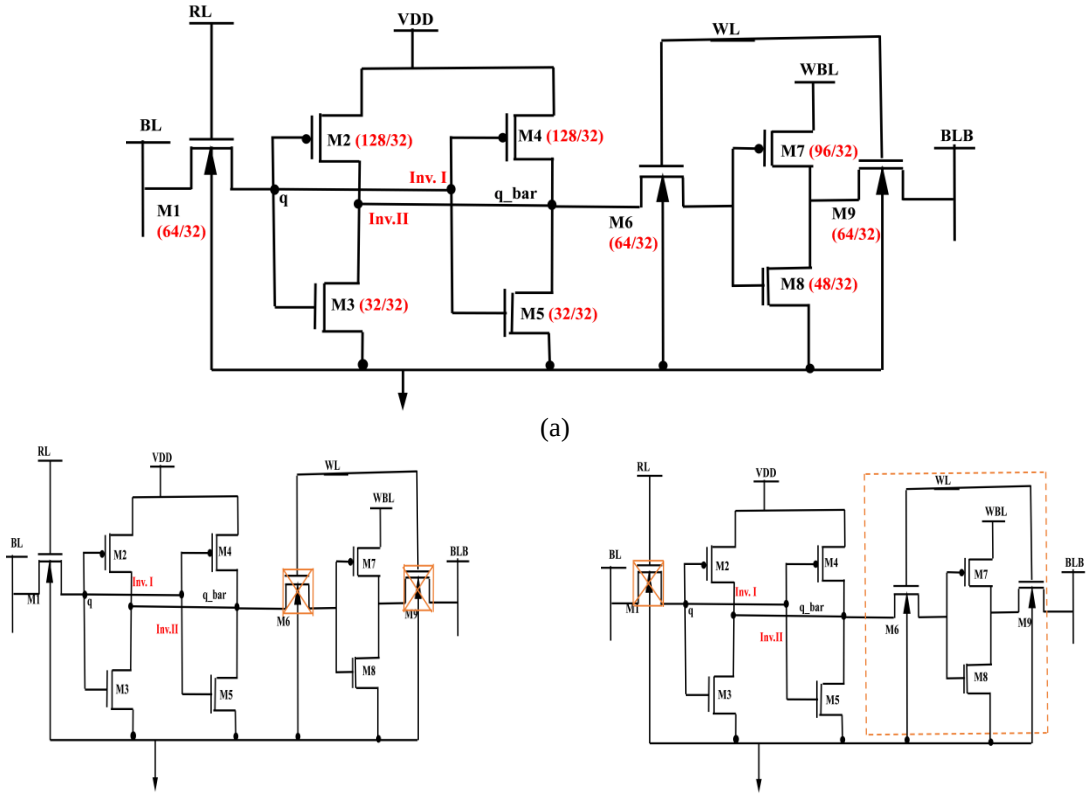


Fig. 3.5. Schematics of proposed 9T SRAM cell (P9T PS) (a) with transistor sizing (in nm), (b) read and (c) write mode.

This method is frequently used in vector processing and SIMD (Single Instruction, Multiple Data) architectures, which allow one instruction to concurrently work on several data components. The P9T (PS) SRAM cell facilitates high-performance computing and parallel processing by providing quick access times, energy efficiency, and the capacity to run in parallel within and across several cells. Because of this, it is a good fit for applications that need to process and manipulate data quickly, like large-scale computational jobs, real-time data analytics, and scientific simulations. The write margin may be lowered if write operations are performed on a single bitline without the use of write-assist strategies. This deterioration results from a decreased capacity to accurately regulate the voltage levels required to consistently discern between writing a '0' and a '1'.But in this suggested design the write assist technique is not deployed to accommodate parallel processing.

To overcome such obstacles and improve the overall performance and dependability of the P9T (PS) SRAM cell, dual port architecture is used. In order to guarantee single end write operation, the RL signal is also deactivated during write operation, which undoubtedly

disables the M1 transistors. Point q stores the value obtained from bit-line (BL) directly, while q_bar stores the inverted value. Node q flips to logic "high" [29] to illustrate what happens when the WL control signal and BL are both at logic "high." Transistor M6 & M9 turns on, M7 & M8 flips the stored value and transistor M1 turns off as a result. Transistor m1 sinks any voltage above logic '0' at q_bar node to ground, ensuring q_bar node at logic '0,' as can be illustrated in Figure 3.5(c).

The proposed P9T (PS) SRAM cell is designed at the 32nm technology node and is compared to other 9T single-port and dual-port SRAM cells. The cells taken for comparison [8 - 15] were reported on different technology nodes. Therefore, all the cells are re-simulated at 32 nm for a fair comparison with the proposed cell. All 9T SRAM cells have a channel length of 32nm, which is in line with the technological capabilities of the node and the design specifications for high-performance integrated circuits. This guarantees manufacturing viability and uniformity in performance metrics within the specified semiconductor technology. Due to technological limitations and optimizations at the 32nm node, the channel length of 32 nm remains a common factor when comparing different SRAM cell designs (e.g., P9T PS versus other 9T configurations). While maintaining this channel length specification, the focus is on optimizing other parameters like transistor width, power efficiency, temperature variation tolerance, and access time. Different technology nodes offer varying levels of performance in terms of speed, power consumption, accessing delay, stability and density. For instance, smaller nodes like 22nm and 11nm generally provide improved performance characteristics; such as, higher transistor switching speeds and lower power consumption compared to other nodes; 32nm, 45nm, 90nm and 180nm. But smaller technology nodes often come with higher manufacturing costs, higher leakage and lesser temperature variation tolerance due to processes complexity.

So, to accommodate these issues, 32nm technology node is considered as it offers a good balance between cost and performance for their various applications and also reduces the designing complexities. Technology node 32nm is considered to be a better choice because it offers a stable manufacturing processes and mature yield rates such as; better stability, temperature variation tolerance and low leakage, which can be advantageous for various applications. The choice of 32nm technology over 22nm or 11nm widely depends on a trade-off between performance, cost, design compatibility, manufacturing readiness, and specific application requirements. Each technology node has its own advantages and limitations, and

the selection involves balancing these factors to achieve optimal results for the intended design.

The use of read buffer transistors eliminates ATS conflict during write and read operations. For the suggested topology, the transistor sizing standards are adhered to. Pull up transistors M2 and M4 are kept at a lower power to reduce the PR and facilitate write operations, much like in a traditional 6T SRAM. Since the write buffer transistors M7, M8, and read stack transistor M9 make up the cell discharge route, they must be expanded to provide a greater read current to pass through and, consequently, a shorter access time while the device is operating. In correspondence with this, the P9T (PS) SRAM cell is executing parallel processing, to enable a high conduction channel for read and write operations between bit-lines and the accessed cell. In essence, access transistors M1 and M9 are maintained stronger. Pull-down transistors M3 and M5, in contrast to traditional 6T SRAM cells, are not needed to be strong since they are not completely involved in the cell discharging pathways during read operation. However, they are kept wide enough to provide a sufficient resistive path in standby mode and a greater hold static noise margin (HSNM).

3.5 PROPOSED DESIGN ANALYSIS AND COMPARISON WITH EXISTING CELLS

In this part of the chapter, the P9T and the 11T SRAM cells are compared with different and same transistor count cell to conclude the overall advancement of the proposed architectures. Various circuit configurations for SRAM cells [52] were designed by eminent researchers over past years to address the challenges. The objectives of design includes parameters such as – high density of bit cell, lower leakage current/power, speed of operation, and lower V_{DD} requirement [114] to design an SRAM bit cell design. The point of commonality for bit cells discussed in this part are the transistor count of cells i.e., all the cells are eight transistor SRAM cells. Some of them have a single ended approach and other have a dual ended approach for implementation of its operation. In this part; the entire cell has been designed at low voltage using the CMOS technology node of 32nm under the maintained temperature of 27 °C. The various cells are compared in terms of their process corner variations, voltage Scaling, temperature variations, dynamic power consumption, leakage power consumption, Power Delay Product (PDP), SNM to area and PDP ratio (SAPR), Electric quality matric (EQM), hold stability, read stability and writability [118].

3.5.1 Static Parameters

In order to have a fair and comparable platform for comparison between all the architectures analysed in this work, all the SRAM bit cells are designed and simulated using Predictive Technology Models (PTM) for the 32 nm CMOS technology node. The supply voltage (VDD) for the comparative study is also kept at under 1V for all SRAM cells. The Static Noise Margin (SNM) in hold, read and write operations is the main parameter to be considered for the robustness, stability and reliability analysis of an SRAM bit cell. SNM is usually defined as the maximum DC noise voltage that an SRAM cell can tolerate without changing or flipping the state of the stored data. Thus, SNM offers a quantitative metric to assess the noise immunity and stability capability of SRAM bit cells under various operating conditions.

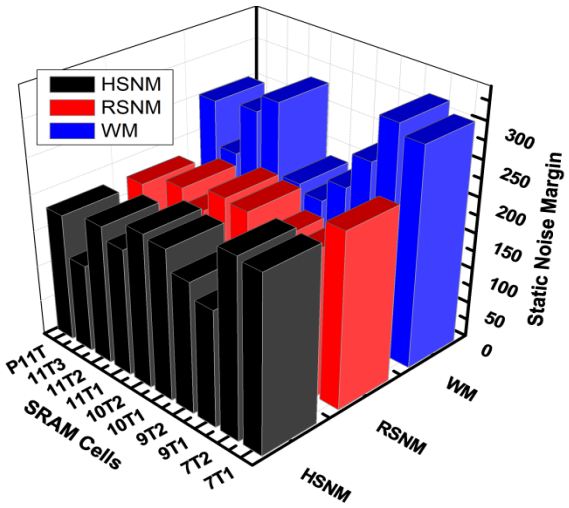


Fig. 3.6. Static Margins of Different SRAM bit cells compared with proposed 11T cell.

The stability of an SRAM cell in read, hold and write operations is analyzed by considering the butterfly curve which is formed by the graphical superimposition of the voltage transfer characteristics (VTC) of the two cross-coupled inverters that constitute the memory cell. The value of the SNM is given by the length of the side of the largest square that fits into the smaller lobe of the butterfly curve. In this work, the proposed 11T and P9T (PS) SRAM cells are analysed statically by computing their respective Hold Static Noise Margin (HSNM), Read Static Noise Margin (RSNM) and Write Margin (WM). The proposed 11T SRAM cell is comparatively studied with few reported SRAM architectures such as $7T_1$ [61], $7T_2$ [62], $9T_1$ [55], $9T_2$ [53], $10T_1$ [63], $10T_2$ [9], $11T_1$ [11], $11T_2$ [64], and $11T_3$ [65] SRAM cells. The results show that some SRAM topologies such as $9T_2$ and $11T_1$ have similar SNM values to the proposed 11T SRAM cell for hold and read operations.

The proposed 11T SRAM cell, however, exhibits better write stability characteristics and achieves the highest Write Margin (WM) which is close to VDD/2, thus confirming its improved write capability and robustness, as can be seen in figure 3.15. The proposed P9T (PS) SRAM cell also shows good stability characteristics in all the operation modes. The results of SNM show that the proposed P9T (PS) cell has a Write Margin (WM) of 0.422 V and Read SNM and Hold SNM are 0.368 V and 0.364 V respectively.

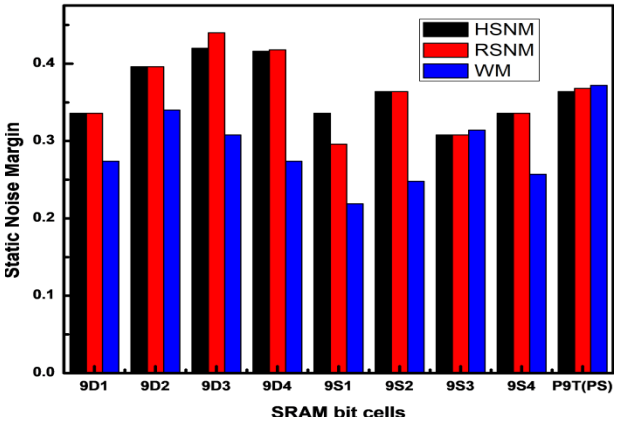


Fig. 3.7. HSNM, WM and RSNM values for different 9T SRAM cells.

Table 3.6. WM, Read SNM, and Hold SNM for various 9T SRAM cells.

SRAM Cells	HSNM	RSNM	WM
9S1 [59]	0.336	0.198	0.219
9S2 [53]	0.367	0.365	0.248
9S3 [158]	0.308	0.308	0.314
9S4 [57]	0.336	0.336	0.257
9D1 [60]	0.336	0.336	0.274
9D2 [56]	0.396	0.396	0.34
9D3 [54]	0.420	0.440	0.308
9D4 [55]	0.416	0.418	0.274
P9TPS	0.364	0.368	0.422

The results validate the improved noise immunity and improved operational stability of proposed P9T (PS) SRAM architecture. The comparative SNM characteristics of the proposed P9T (PS) SRAM cell with various existing 9T SRAM topologies are summarized in Table 3.6. The corresponding butterfly curve analysis and comparative SNM evaluation are shown in figure 3.6.The comparison of Hold SNM, Read SNM, and Write SNM of the proposed dual-port 11T SRAM cell with the previously reported SRAM architectures are shown in figure 3.7. The comparative results show that the proposed 11T and P9T (PS) SRAM cells have better static stability characteristics, better resistance to noise disturbance

and better operational robustness in low voltage operation. Therefore, the proposed topologies of SRAMs are very suitable for future low power high performance and reliability-oriented nanoscale memory applications.

3.5.2 Power Consumption:

Power dissipation is one of the most critical design considerations in the SRAM bit-cell architectures, especially due to the continuously increasing demand for portable consumer electronic devices with extended battery lifetime and enhanced energy efficiency [30]. To this end, the total power consumption of SRAM cells has to be reduced for reliable low power memory operation in nanoscale technologies. The energy efficiency of the proposed SRAM architectures has been evaluated by analysing and comparing the read, write and leakage power consumption at different supply voltage (VDD) levels.

The dynamic or switching power in SRAM cells is mainly associated with the charging and discharging activities of the BL and BLB nodes. In the proposed 11T SRAM cell, the isolated read path efficiently reduces the internal voltage fluctuation during the read operation, which reduces the unnecessary switching activity and internal node toggling. Furthermore, the implementation of a write-assist mechanism in the proposed architecture contributes to further dynamic energy reduction during write operations. The general formula for estimating dynamic power dissipation in CMOS circuits is:

$$\text{Pdyn} = \alpha.\text{Csw}\, V^2 f \qquad (3.1)$$

where α is the switching activity factor, Csw is the switching capacitance, V is the supply voltage and f is the operating frequency. The read and write power consumption obtained for the proposed 11T SRAM cell is measured as 18.26 μW and 5.32 μW respectively. The reported read power consumptions of $7T_1$ [61], $7T_2$ [62], $9T_1$ [55], $9T_2$ [53], $10T_1$ [63], $10T_2$ [9], $11T_1$ [11], $11T_2$ [64], and $11T_3$ [65] SRAM cells are 24.3, 27.6, 28.2, 27.4, 34.6, 29.64, 14.2, 26.9, and 16.8 μW, respectively. The associated write power consumption values for these SRAM cells are 2.6, 5.4, 4.2, 5.2, 6.4, 7.2, 4.1, 6.2, and 7.4 μW, respectively, as shown in figure 3.8.

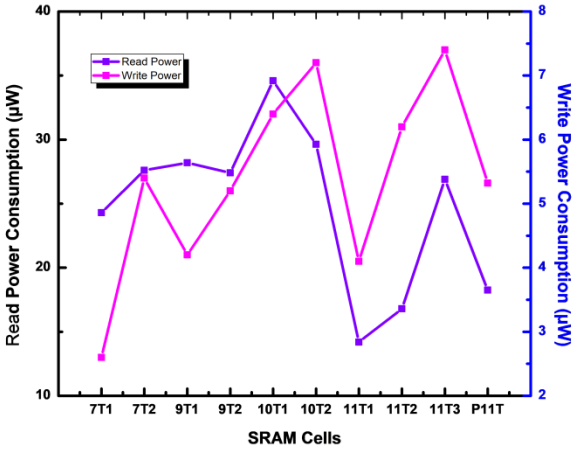


Fig. 3.8. Analysis of Dynamic power consumption for different transistor count SRAM cells.

The comparative study of the proposed P9T (PS) SRAM cell reveals that most of the studied 9T SRAM architectures exhibit similar writes power dissipation at different supply voltages. However, the conventional 9T SRAM cells exhibit relatively higher total power consumption at supply voltages above 0.9V. The proposed P9T (PS) SRAM cell shows similar power characteristics as the existing architectures, except at 0.9 V, where a slightly higher power value is observed. However, the proposed P9T (PS) SRAM cell shows better leakage power characteristics over many of the previously reported SRAM cells. Among all the topologies analysed, the conventional 9T SRAM cell exhibits the lowest leakage power dissipation [31], very close to the proposed P9T (PS) SRAM cell. Thus, the power analysis obtained demonstrates that the proposed P9T (PS) SRAM cell is highly suitable for low-power applications [32], particularly at supply voltages less than 0.9 V.

A detailed power analysis is carried out for the proposed 11T SRAM cell and compared with several previously reported SRAM architectures. The previous 11T SRAM cells use a single bit-line (BL) for the write operation. This reduces the charging/discharging activity of differential bit-lines and thus reduces the dynamic power consumption. The proposed 11T SRAM cell, however, adopts an optimized dual access mechanism, which can greatly improve the energy efficiency of the read operations. The read path has two dedicated access transistors which speed up the read operation and also reduce the power needed for the bit-line transitions. Furthermore, the proposed cell [1, 22] greatly reduces its dynamic switching power consumption by eliminating unnecessary bit-line discharge activity. In general, the total power consumption of an SRAM bit cell can be categorized into three major components related to its basic operations, i.e., read power, write power, and hold or leakage power, as shown in figure 3.9(a), figure 3.9(b) and figure 3.9(c), respectively for different 9T cell in comparison with the proposed 9T cell.

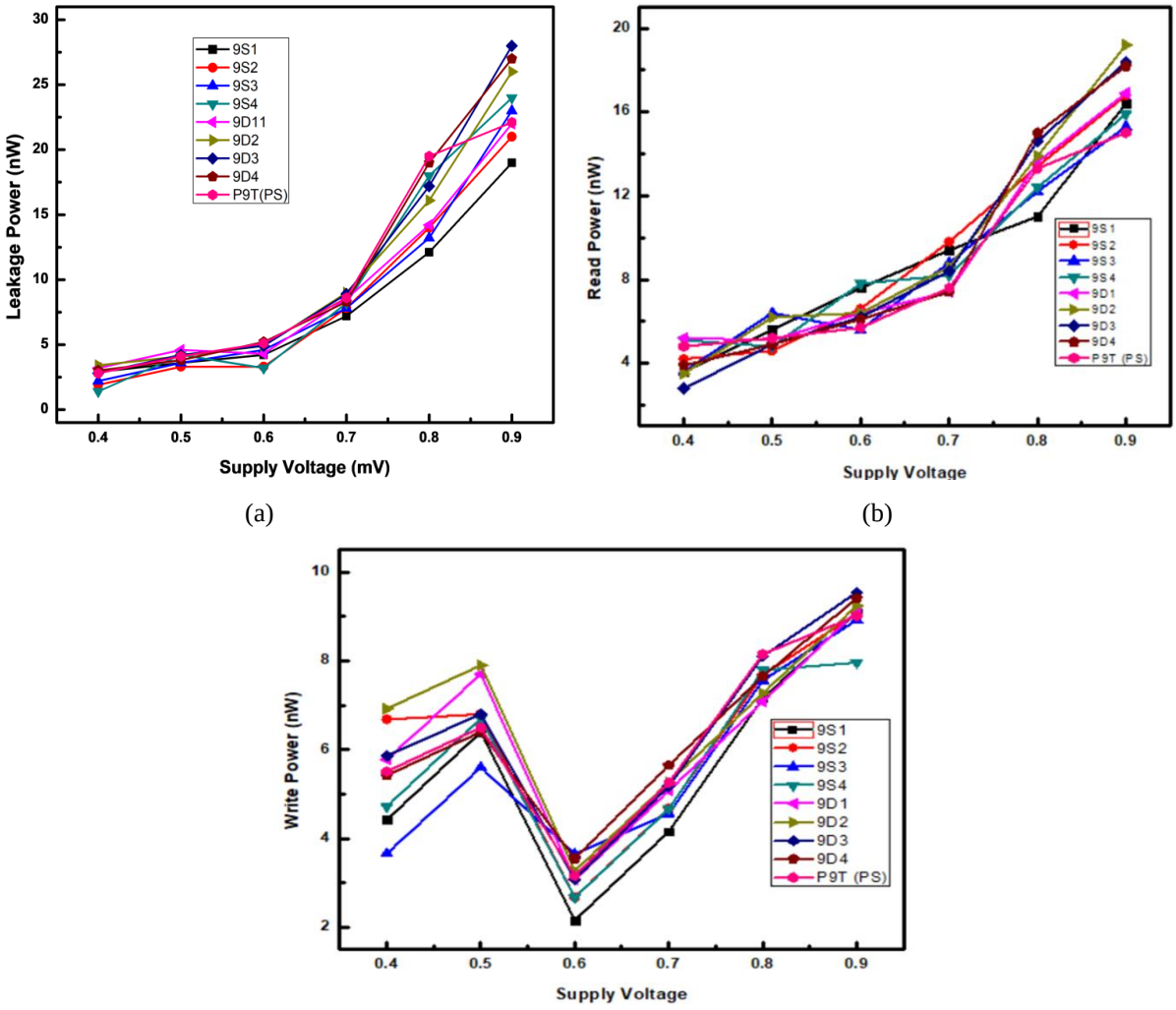


Fig. 3.9. (a) Leakage power, (b) Read Power and (c) Write Power values for various 9T cells at different VDD ranges from 0.4–0.9 V.

The comparison results show that the proposed 11T SRAM cell has much lower read power consumption than most existing SRAM structures, while keeping its write power dissipation at a competitive level. In summary, the results demonstrate the benefits of the proposed P9T (PS) and proposed 11T SRAM cells in terms of power savings, leakage characteristics and reduced dynamic switching activity, making them a good candidate for ultra-low-power and energy-efficient nanoscale memory applications.

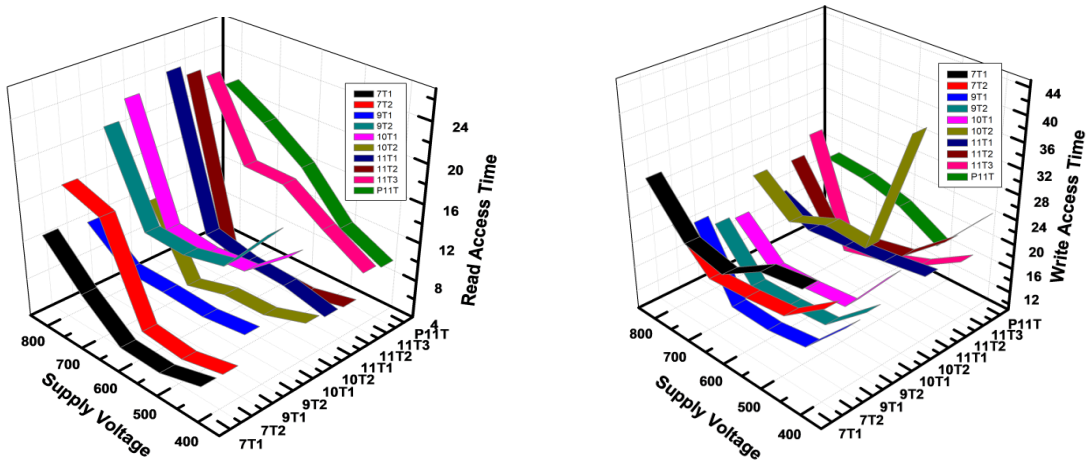
3.5.3 Accessing Time Analysis

The previous analyses focus mainly on the static performance characteristics of the SRAM bit cells and do not consider the time required for the read and write operations to complete. However, timing performance is one of the most critical design concerns in real-time applications because the operating speed of an SRAM bit cell is fundamentally determined by its read and write access times [57]. Therefore, the determination of the pulse width necessary

to successfully perform the read and write cycles is critical for the evaluation of the dynamic performance and the efficiency of the memory architecture.

The read access time is the time needed to discharge the bit-line (BL) voltage to the switching threshold voltage of the sensing inverter during data retrieval. Likewise, the write access time is the time needed to successfully overwrite the stored logic state in the SRAM cell. Faster read and write access times directly translate to faster operation, higher throughput and better overall system performance [64].

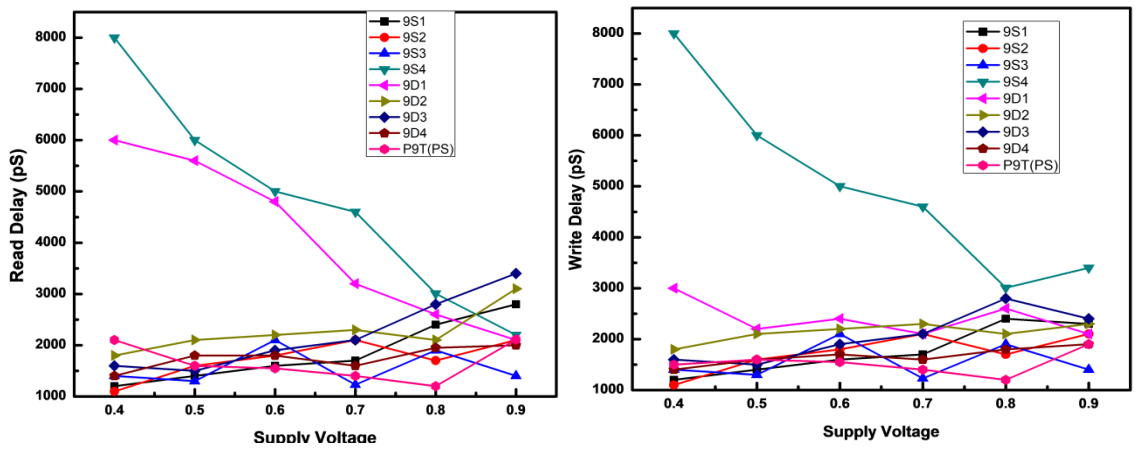
From the comparative analysis, the maximum read access time is obtained in the $9T_2$ [53] SRAM cell among the previously reported SRAM topologies. The $10T_2$ SRAM cell has architectural similarities with the proposed 11T SRAM cell and comparatively lower write access delay is observed in the $10T_2$ SRAM cell. Moreover, the $11T_2$ [64] SRAM cell has the longest write access time among the studied 11T architectures, whereas the proposed 11T SRAM cell has the shortest write access time [67].



(a) (b)

Fig. 3.10. Accessing time of all the SRAM cells for (A) Read and (B) Write operation compared with proposed 11T SRAM cell.

These observations justify the improved dynamic response and faster operational capability of the proposed 11T SRAM design, shown in figure 3.10 (a & b). Similarly, for the proposed 9T (PS) SRAM cell, the comparative analysis shows that among the analyzed 9T SRAM architectures, the $9S_4$ [11] SRAM cell has the highest read and write access delays. On the other hand, the proposed P9T (PS) SRAM cell shows minimum write access time and also reduced the read access delay to a great extent which confirms the high speed operation and effective switching characteristics. The write and read access time of the proposed P9T (PS) SRAM cell is found to be 1.2 ns and 4.5 ns, respectively.



(a) (b)

Fig. 3.11. Delays for different SRAM bit cells for VDD ranging from 0.4 V to 0.9 V with P9T cell (a) Read and (b) Write.

The read and write delay characteristics of the proposed P9T (PS) SRAM cell and other conventional 9T SRAM topologies are shown in Figures 3.11 (a) and (b), respectively, for a variable supply voltage range of 0.4 V to 0.9 V. The achieved results show that the proposed cell maintains the improved timing performance and reduced delay variations for different supply voltage conditions.

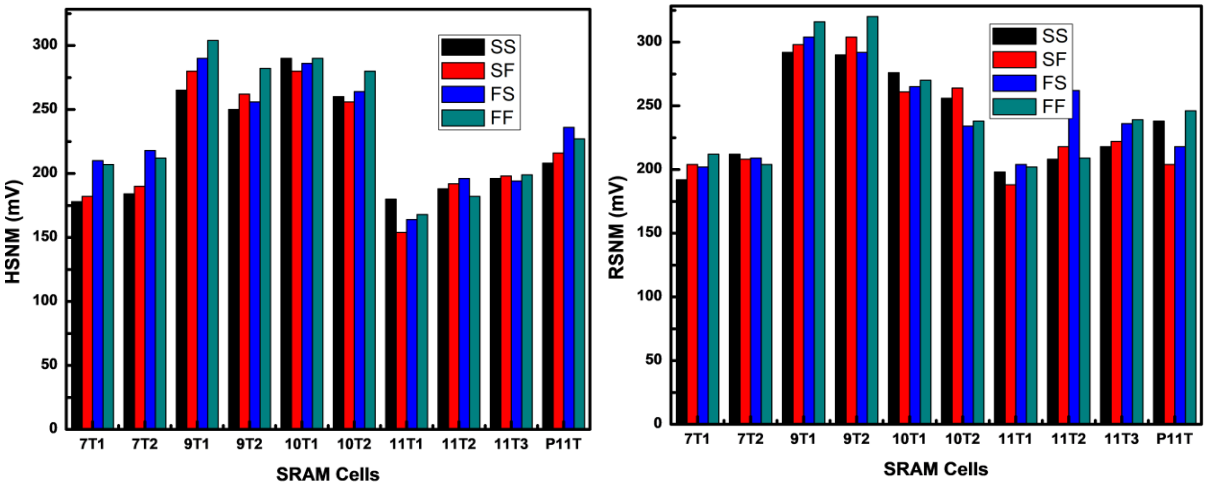
The minimum values of read and write access times are observed at supply voltage of 500 mV for the proposed 11T SRAM cell. As shown in Figure 3.10, the access delay variation for most of the compared SRAM cells beyond this operating voltage is marginal. Hence, the optimum operation supply voltage for the proposed 11T SRAM cell is 500 mV which can provide the reduced access delay with low power operation and improved stability characteristics. In general, the proposed P9T (PS) and 11T SRAM cells show better dynamic performance, faster access operations and better timing efficiency with respect to the existing SRAM architectures and hence they are very suitable for high-speed and low-power memory applications.

3.5.4 Process Corner Variation Analysis for Proposed 9T and 11T SRAM cells:

Fabrication-induced parameter fluctuations cause global variations and affect process corner and global variation analysis during hold and read operations, which is a key reliability evaluation metric for SRAM bit cells. The impact of variations in semiconductor manufacturing such as threshold voltage mismatch, channel length fluctuation, oxide thickness variation and mobility degradation are significant on the stability characteristics of SRAM cells. Therefore, it is required to evaluate the Hold Static Noise Margin (HSNM) and

Read Static Noise Margin (RSNM) for different process corners to verify the robustness and reliability of the proposed memory architectures.

The proposed 11T SRAM cell displays remarkable robustness to global process variations. The obtained HSNM and RSNM metrics for all process corners indicate that the 11T architecture always provides better read and hold stability than the SRAM cells. The 11T cell performs best in the SF corner where the stability margins are significantly improved by the favorable process interaction between the PMOS and NMOS. Moreover, the 11T SRAM cell provides higher HSNM and RSNM values compared to existing SRAM architectures even under adverse process conditions (FS, FF and SS corners), thus showing its strong resilience against fabrication variability.



(a) (b)

Fig. 3.12. Comparative analysis of (a) HSNM, (b) RSNM at SS, SF, FS and FF corners for different cells and proposed 11T SRAM cell.

The comparison of HSNM and RSNM values of the proposed P9T (PS) and 11T SRAM cells at different process corners are shown. The results show improved stability performance in comparison with the previously reported SRAM topologies. The process corners evaluated are Fast-Fast (FF), Slow-Slow (SS), Fast-Slow (FS) and Slow-Fast (SF). Out of these, the SF corner exhibits the best performance for both of the proposed SRAM cells.

The NMOS transistors in the SF corner are in slow process and the PMOS transistors are in fast process. It improves the effective drive balance between pull-up and pull-down networks. It improves the stability margins of the cell. The proposed P9T (PS) SRAM cell shows good process variation tolerance and better hold and read stability performance in comparison with the previously reported SRAM cells including $9S_1$ [59], $9S_2$ [53], $9S_3$ [58], $9S_4$ [57], $9D_1$ [60], $9D_2$ [56], $9D_3$ [54] and $9D_4$ [55]. The results obtained indicate that the P9T (PS) cell has the

highest HSNM and RSNM values at the SF corner of all the compared cells, confirming its improved immunity to process induced variations and mismatch effects. The FS process corner is the most critical operating condition due to the weaker pull-up characteristics and stronger NMOS conduction. However, the proposed P9T (PS) cell has relatively stable operation and acceptable noise margins across all corners.

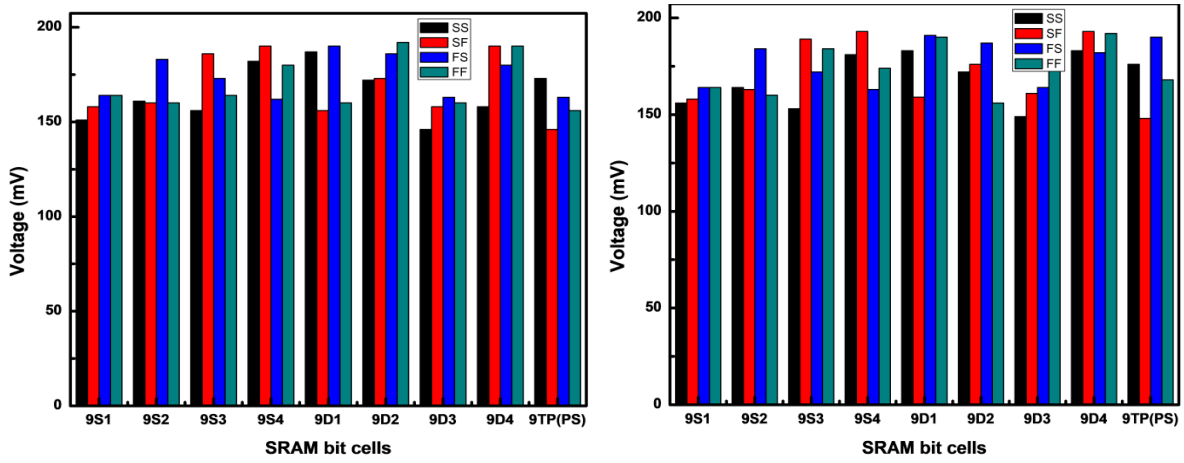


Fig. 3.13. Analysis of diiferent SRAM cells for (a) HSNM, (b) RSNM at SS, SF, FS and FF corners.

The comparative results of HSNM and RSNM for the proposed 11T and P9T (PS) SRAM cells for different process corners are shown in Figure 3.12(a and b) and Figure 3.13(a and b), respectively. The analysis confirms that both the proposed SRAM topologies provide better stability, improved noise immunity and reliable low-voltage operation under wide process variations, thus are suitable candidates for future low-power and high-reliability nanoscale memory applications.

3.5.5 Temperature Variations Analysis

Modern microprocessor architectures include cache memory, and the internal switching activities and external environment conditions have a significant impact on the overall system performance and reliability. Therefore, the bit cells of SRAMs used in cache memories must be stable and reliable over a wide range of temperatures to guarantee error-free operation in practical applications. To evaluate the thermal robustness of the proposed SRAM architectures, extensive temperature variation analyses have been performed for the proposed P9T (PS) and 11T SRAM cells over a temperature range from −10 °C to 100 °C [32].

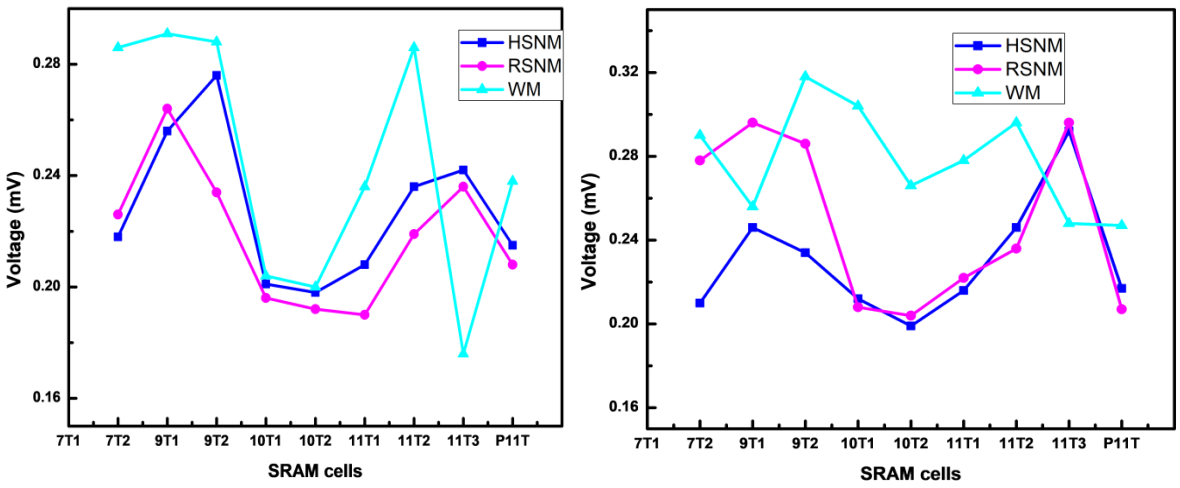
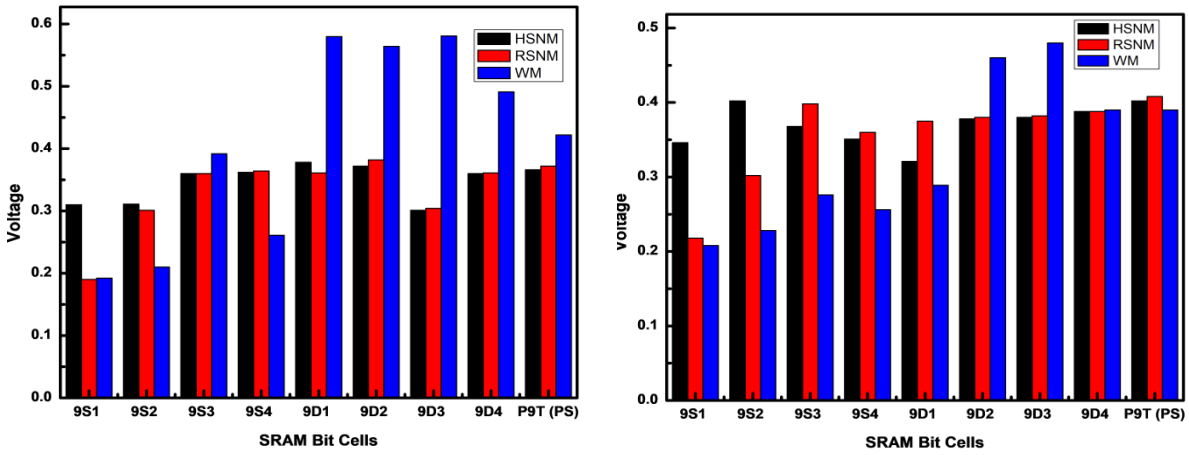


Fig. 3.14. Values (HSNM, RSNM, and WM) measured at (a) 100 °C and (b) -10 °C for different SRAM cell compared with proposed 11T SRAM cell.

The proposed 11T SRAM cell shows a very high robustness to the thermal variations. Since the SRAM cell is in static state during the hold operation, the increase in the ambient temperature adversely affects the stability characteristics due to increase in leakage currents, reduction in carrier mobility and increase in the thermal noise. The temperature dependence of the HSNM, RSNM and WM parameters for the proposed 11T SRAM cell is shown in figure 3.14. The obtained results show that the 11T cell shows the lowest temperature dependent degradation of stability parameters. The temperature variation coefficients of HSNM, RSNM, and WM are observed to be 0.213 mV/°C, 0.196 mV/°C, and 0.247 mV/°C, respectively at 100 °C, while at −10 °C the values are 0.201 mV/°C, 0.196 mV/°C, and 0.223 mV/°C, respectively. Such reduced variations rates confirm the high thermal stability and robustness of the proposed 11T SRAM architecture under extreme temperature conditions.

Similarly, the thermal stability analysis of the proposed P9T (PS) SRAM cell shows that it is highly immune to the performance degradation induced by the temperature. Figure 3.15 shows the comparative variation of Static Noise Margin (SNM) characteristics of different SRAM cells with varying thermal condition. The obtained results show that the proposed P9T (PS) SRAM cell can achieve HSNM, RSNM and Write Margin (WM) values of 0.402V, 0.408V and 0.390V respectively at -10 °C whereas the values are found to be 0.366V, 0.372V and 0.422V respectively at 100C, as shown on figure 3.15 (a and b).



(a) (b)

Fig. 3.15. SNM values (HSNM, RSNM, and WM) at (a) 100 °C and (b) -10 °C for all 9T SRAM cell.

The small variation of stability parameters also confirms the superior temperature tolerance capability of the proposed P9T (PS) SRAM cell. In general, the HSNM and RSNM of SRAM cells are increased at low temperatures, especially below 10 °C. This behavior is basically due to two physical phenomena. First, at lower temperatures, leakage current decreases substantially, thereby minimizing unwanted power dissipation and leakage-induced instability. Second, reduced thermal agitation increases the mobility of charge carriers, such as electrons and holes, thus improving the drive strength of transistors and the switching characteristics in general.

Table 3.7. HSNM, RSNM and WM (mV/°C) values for all 9T SRAM cells at 100°C.

SRAM Cells	HSNM	RSNM	WM
9S1 [59]	0.310	0.190	0.192
9S2 [53]	0.311	0.301	0.21
9S3 [58]	0.360	0.360	0.392
9S4 [57]	0.362	0.364	0.261
9D1 [60]	0.378	0.361	0.58
9D2 [56]	0.372	0.382	0.564
9D3 [54]	0.301	0.304	0.581
9D4 [55]	0.360	0.361	0.491
P9TPS	0.366	0.372	0.422

The improved carrier mobility enhances the operation of the SRAM cell by improving the performance of the transistors and at the same time reduces the effects of the thermal noise. Table 3.7 and Table 3.8 presents the HSNM, RSNM, and WM values of the proposed P9T (PS) SRAM cell at -10 °C and 100 °C respectively. Moreover, the proposed 11T SRAM cell

has been comparatively analyzed with several reported SRAM topologies to evaluate its temperature resilience capability [23]. The comparative analysis under different supply voltage conditions shows that the proposed 11T SRAM cell has a competitive temperature variation tolerance compared to the existing SRAM architectures.

Table 3.8. HSNM, RSNM and WM (mV/°C) values for all 9T SRAM cells at −10°C.

SRAM Cells	HSNM	RSNM	WM
9S1 [59]	0.346	0.218	0.208
9S2 [53]	0.402	0.302	0.228
9S3 [58]	0.368	0.398	0.276
9S4 [57]	0351	0.360	0.256
9D1 [60]	0.321	0.375	0.289
9D2 [56]	0.378	0.380	0.460
9D3 [54]	0.380	0.382	0.480
9D4 [55]	0.388	0.388	0.390
P9TPS	0.402	0.408	0.390

The $10T_1$ and $10T_2$ SRAM cells have slightly better temperature tolerance characteristics, however, the proposed 11T SRAM cell offers slightly better thermal stability compared to most of its pre-existing SRAM cells. Such enhanced thermal robustness is highly desirable for SRAM deployment in thermally intensive, reliability-critical applications like portable electronics, aerospace systems, IoT platforms, and high-performance cache memory architectures. Both proposed P9T (PS) and 11T SRAM cells overall exhibit strong immunity to temperature-induced degradation, improved operational stability and reliable functionality over a wide thermal range, making them suitable for advanced low-power and high-reliability nanoscale memory applications.

3.5.6 Performance Comparison between Proposed 11T and P9T (PS) SRAM Cells

The comparative performance analysis of the proposed 11T and P9T (PS) SRAM cells against some of the earlier SRAM architectures shows significant improvement in stability, power efficiency, leakage characteristics and operational reliability. Critical design metrics like Static Noise Margin (SNM), read/write access delay, power dissipation, leakage current, Power Delay Product (PDP), area efficiency and electrical quality metrics were considered while performing the analyses. The obtained results for the proposed 11T SRAM cell show a good compromise between stability, speed and power consumption are shown in Table 3.9. The cell shows Ion/Ioff ratio of 562 confirming strong switching capability and improved

transistor reliability. The read and write power consumption are observed to be 18.26 µW and 5.32 µW respectively which are very less compared to most of the previously reported SRAM architectures like $9T_1$, $9T_2$, $10T_1$, $10T_2$, and $11T_3$ cells.

Table 3.9. Parametric comparison between proposed 11T and other cells of different transistor count.

Parameter (s)	**7T1 [61]**	**7T2 [62]**	**9T1 [55]**	**9T2 [53]**	**$10T_1$ [63]**	**10T2 [9]**	**11T1 [11]**	**11T2 [64]**	**11T3 [65]**	**Prop. 11T**
Ion/Ioff Ratio	642	560	486	538	492	506	660	476	498	562
Read Power (µW)	24.3	27.6	28.2	27.4	34.6	29.64	14.2	16.8	26.9	18.26
Write Power (µW)	2.6	5.4	4.32	5.21	6.4	7.2	4.1	6.2	7.4	5.32
Leakage Power (nW)	17.8	12.6	15.2	28.1	29.4	48	30.2	32.2	28.9	24.16
Read access Time (pS)	6.24	6.42	9.64	13.64	12.05	6.34	8.36	6.24	12.21	11.38
Write Access Time (pS)	27.1	18.6	11.6	13.4	14.36	22.4	18.6	17.8	14.48	16.24
Area (μm^2)	0.873	0.831	2.378	2.58	2.469	3.438	4.476	3.76	2.681	3.228
PDP Read	151.63	177.17	271.8	373.73	416.9	187.9	118.42	104.8	328.44	207.79
PDP Write	70.46	100.44	48.72	69.68	93.44	161.2	76.26	110.3	107.15	86.396

The timing performances of the proposed 11T SRAM cell are 11.38 ps and 16.24 ps for read and write access times respectively. Although some of the existing cells exhibits slightly lower access delays, the proposed 11T architecture offers a better trade-off between delay, power dissipation and stability. The obtained Read PDP and Write PDP values are 207.798 and 86.396 respectively which further proves the improved energy efficiency of the proposed cell with reference to several existing SRAM topologies. The cell area of 3.228 μm^2 is still reasonable in comparison with the improved stability and dual-port operational advantages offered by the architecture. Similarly, the proposed P9T (PS) SRAM cell demonstrates significant improvements in noise immunity, power efficiency and operational robustness compared to previously reported single-port and dual-port 9T SRAM cells, summarized in Table 3.10. The measured Hold Static Noise Margin (HSNM), Write Margin (WM) and Read Static Noise Margin (RSNM) are 0.364 V, 0.422 V and 0.368 V respectively. The obtained

write margin is much higher than all the compared SRAM cells, showing better write stability and better resistance against write failures.

Table 3.10. Parametric comparison of different 9T SRAM cells.

Parameters	P9T (PS)	Single – Port cells				Dual – Port cells			
		$9S_1$ [59]	$9S_2$ [53]	$9S_3$ [58]	$9S_4$ [57]	$9D_1$ [60]	$9D_2$ [56]	$9D_3$ [54]	$9D_4$ [55]
HSNM (V)	0.364	0.336	0.367	0.308	0.336	0.346	0.395	0421	0.416
WM (V)	0.422	0.219	0.248	0.314	0.257	0.274	0.34	0.308	0.274
RSNM (V)	0.368	0.198	0.365	0.308	0.336	0.336	0.396	0.440	0.418
Read Access Time (pS)	4.5	5.1	6.2	5.0	6.9	6.7	5.4	5.8	4.7
Write Access Time (pS)	1.2	1.6	2.3	2.1	2.4	1.6	2.24	1.72	2.235
Read power consumption (nW)	15.21	16.41	16.8	15.21	15.9	16.09	19.26	18.4	18.2
Write power consumption (nW)	9.01	9.08	9.06	8.92	7.96	8.92	9.12	9.24	9.52
Leakage Power (nW)	22.1	29.1	31.0	23	24	32	36.1	26.7	27.4
Read PDP (× 10)	68.84	83.69	104.16	76.05	109.71	107.803	104.04	106.72	85.54
Write PDP	10.81	14.52	20.838	16.82	19.104	14.27	20.42	15.89	21.22
SAPR (V/J)	2.35	0.51	1.57	1.30	0.72	0.94	0.81	0.75	0.66
EQM ($\times 10^{-6}$)	19	21	23	24	26	28	21	31	27

The proposed P9T (PS) SRAM cell also exhibits better dynamic performance with read access time of 4.5 ps and write access time of 1.2 ps, which are among the least values seen across the compared SRAM architectures. Moreover, the proposed cell exhibits low read and write power consumptions of 15.21 nW and 9.01 nW, respectively, and its leakage power dissipation is as low as 22.1 nW, which proves its applicability for ultra-low-power applications.

The energy efficiency of the proposed P9T (PS) SRAM cell is also verified by its less Power Delay Product (PDP) values of 68.84 for read operation and 10.81 for write operation. Furthermore, the proposed architecture has the highest value of Silicon Area and Power Ratio (SAPR) 2.35 V/J and the lowest value of Electrical Quality Metric (EQM) 19 x 10^{-6} among all the compared cells, which confirms the overall design efficiency and reliability of the

proposed architecture. In brief, comparison analysis confirms that the proposed 11T SRAM cell provides better stability, has lower dynamic power dissipation, higher write margin and is more robust to process and temperature variations. Conversely, the proposed P9T (PS) SRAM cell demonstrates improved noise immunity, reduced access delay, lower leakage power, and better energy efficiency. Therefore, both SRAM architectures are very promising for application in future low power, high speed and reliability oriented nanoscale memory systems.

3.6 HIGHLIGHTS OF IMPORTANT RESULTS

The design and full performance evaluation of two new SRAM architectures, the proposed 11T SRAM cell and the proposed P9T (PS) SRAM cell, using 32 nm CMOS predictive technology models for low power and high stability memory applications are presented in this work. The proposed SRAM cells were thoroughly analysed for different operating conditions considering important performance parameters like Static Noise Margin (SNM), write margin, read and write access delay, leakage power, dynamic power consumption, Power Delay Product (PDP), process variation tolerance and temperature stability. The advantage of using higher transistor count structures like 10T and 11T cells has been offset by increased layout complexity and cell area, which decreases memory density and limits the feasibility of efficient large-scale array integration. On the other hand, the 9T architecture has higher operational reliability with relatively lower area overhead, which is more suitable for the compact and scalable memory design.

The 9T SRAM cells achieve improved write ability, better noise margins, reduced write delay and power-delay product than some conventional SRAM structures. The separate read and write paths effectively suppress the read disturbance and enhance the data retention stability in the low-voltage operation. Moreover, the architecture has less leakage power and better energy efficiency, which are critical to modern nanoscale memory systems with stringent power constraints. The trade-off of reduced power dissipation and high access characteristics allows the reliable operation of the high speed memory without significant loss of layout efficiency. Among the analyzed 9T configurations, the proposed architecture shows better hold stability, read stability and write margin while keeping low read and write access times. The proposed design also demonstrates lower read and write power consumption, as well as better sensing ability and overall memory quality. These features confirm the architecture robustness for reliable operation under process scaling and low supply voltage conditions.

Additionally, the 9T SRAM architecture, which is compact, stable and consumes less power, is suitable for dense implementation of SRAM arrays for cache memories, embedded processors and energy-efficient computing systems. In addition, the separated read operation and the enhanced noise immunity provide great advantages for TCAM applications in which reliable search operation, low power consumption of the match-line and stable comparison operation are critical. The overall analysis, therefore, confirms that the 9T SRAM architecture is an efficient and scalable solution for various applications such as; high-performance SRAM arrays and TCAM based memory systems.

CHAPTER-4

ISOLATED READ ASSIST ENABLED ROBUST SINGLE PORT 8T SRAM CELL

4.1 INTRODUCTION

With the advancement in portable devices, lower consumption of power [10] has been considered as one of the most important factors to design the specifications of system on chip (SoC) architectures [32]. Due to the fact that SRAM cells represent a large portion of SoC circuits, lower power consumption in SRAM is particularly crucial. Hence, to limit the power consumption of any system it becomes a crucial point to also limit the operating supply voltage. The need for portable, low-footprint devices with high processing power is driving designers to integrate Internet of Things (IoT) and machine learning components into System on Chip (SoC) [5]. Devices with SoC that integrate artificial intelligence and machine learning are more reliable and attractive. The bulk of an SRAM bit cell's external circuitry consists of the bit line, sense amplifiers [86], and decoders. Various processors that rely on the internal cache memory comprise the SRAM bit cell; these processors are essential for applications that demand faster execution [87]. Nanometre technology feature size, which promotes sleek designs with longer battery lives to fulfil demands, may be the industry's most recent development [108].

Reducing the VDD [11] at which a cell operates is the most common method of reducing the electricity usage of the cell. However, other factors, including the change in the process voltage temp. (PVT) in the deep sub-micrometer regions, must be taken into account when the supply voltage is lowered below a particular threshold [82].Since the SRAM cell typically operates in the hold mode, the static power consumption is measured to determine the overall power utilised by the cell [83]. The main disadvantage of lowering the VDD is that it results in less memory operation and a slightly higher bit error rate (BER) number [14]. As a result, creating digital circuits with enhanced performance is quite difficult for designers. It is very difficult for designers to build digital circuits with better performance because they have to take into account the VDD that operates in the range surrounding the saturation voltage [92]. Along with other important parameters, soft computing and software related errors becomes a crucial part while designing and analysing any SRAM cell. Soft errors are the major setbacks for any memory circuits; hence to rectify or completely eliminate such soft errors becomes a crucial parameter. Therefore, to resolve the issue pertaining to device stability and the device

immunity towards soft errors, the low power and lesser complex single port and single ended cells become a better choice. Hence, a single ended and single port 8-transistor (8T) SRAM cell is proposed in this chapter for better immunity of the memory cell. The following objective is framed here to obtain a high-performance single ended, single port 8T SRAM cell:

"To design and assess a single-port symmetrical low voltage operating SRAM bit cell."

To attain this objective, primarily various dual-port and single-port 8T SRAM cells are simulated and analysed for various parameters. The aim of this chapter is to design a low power single port 8T SRAM bit cell suitable for low power consumption and in-memory computing and CAM search applications. The prime focus was to reduce the search delay and provide better immunity for various array operations using SRAM cell. This chapter aims at improving the performance of an SRAM cell through modifying overall structure using single port architecture. A symmetrical single port 8T SRAM cell structure is proposed in this chapter. This proposed cell is compared with other existing 8T cells to investigate the impact of proposed architecture on different performance parameters including noise stability, threshold voltage scaling, temperature variation, process variation, power consumption, Ion/Ioff ratio and electric quality metric (EQM).

The structure of this chapter is as follows; a brief introduction of this chapter, the objective of the chapter is included in Section 4.1 of this chapter, following this the characteristics of different 8T SRAM cell topologies are illustrated in section 4.2. The detailed functioning of the proposed 8T SRAM cell, followed by the detailed analysis and comparison of proposed 8T cell with different 8T cells is expressed in section 4.3 and 4.4, respectively. Finally, the overall conclusion of the cell analysis is given in section 4.5 of this chapter.

4.2 CHARACTERISTIC ANALYSIS AND PARAMETERS OF DIFFERENT 8T SRAM CELLS

Numerous SRAM bit cells have been reported to achieve various design objectives over time, including reduced timing specification, low-voltage operation, bit density, and bit cell area [47]. This portion of the paper discusses some of the notable SRAM bit cells [8] that have been published in the last ten years. R. Lorenzo et al. proposed a cell $8T_1$ [76] that explains a novel technique which tend to minimise the soft errors like half select in the 8T cell with almost negligible leakage. The study offers a state-of-the-art design that effectively lowers the leakage currents.

The $8T_2$ [82] cell suggested a cuttingedge technique and strategy to improve the performance of sub threshold SRAM cells, according to Kushwaha et al., single ended read and differential write designed for low voltage application is demonstrated by C. Duari et al.'s $8T_3$. Through thorough investigation and analysis the author demonstrates how successful their strategies are in guaranteeing dependable low voltage operations [79]. A. Jaiswal et al., $8T_4$ [81] offers a revolutionary architecture for repurposing 8T SRAM cells into multibit dot-product engines. In $8D_1$ [78], Duari et al. offer a unique SRAM cell architecture suitable for the Internet of Things. The proposed design aims to improve stability and reduce leakage current, two essential components for IoT device operations which need energy conservation [18]. These results show how their method works to get better performance characteristics appropriate for Internet of Things scenarios by a thorough theoretical study and real-world validation.

The work addresses the impeccable concerns related to power efficiency and variability in modern integrated circuits. Pal et al. in their $8D_2$ [83] provides a novel technique for producing SRAM cells that are both process variation tolerant and have extremely low power consumption [19]. The authors demonstrate how their proposed differential 8T SRAM might potentially achieve good reliability, through meticulous modelling and analysis. $8D_3$ [77] by S.R. Aura et al, the authors present a novel approach to designing a dual port 8T SRAM cell with simultaneous and parallel read write features. The $8D_4$ cell reported by Roy et al. [80] offers a novel method for creating SRAM cells that are optimised for extremely low power consumption. This paper tackles the urgent demand for power efficient memory solutions in contemporary electronic devices. The authors provide a brand new differential thin gate based 8T SRAM cell design that is specifically engineered to reduce power consumption without sacrificing the performance or dependability [18].

An $8D_5$ cell by Chang et al., [85] presented a differential data aware power supplied (D^2AP) 8-transistor cell that enhances the read/write stability and reduces the VDD min for ultra-low power applications. It uses power gating techniques for better noise immunity and stability. $8D_6$ cell by Kim et al., [75], presented 8T architecture with bit-precision configurability, and auto compensation for process, temperature and voltage variations. It introduces a novel 8T current mode compute-in-memory (CIM) architecture. 8T cell by G. Pasandi et al., [87] is a single-ended dual-port eight-transistor design with special focus on reducing leakage current. The memory core of this design also consists of a cross-coupled inverter pair like other designs, but with two key differences. Firstly, the feedback mechanism is not controlled by

any transistor (unlike in the 7T designs). Secondly, the first inverter has its connections to V_{dd} and GND controlled by two adjacent transistors. This allows the inverter to be disconnected from the supply during write operations, reducing power consumption during switching. The read and write ports use standard pass-transistor design. Another $8T_5$ cell design by L. Wen et al.,[84] proposes single-port double-ended eight-transistor design. While possessing a conventional structure for memory and differential access ports, the design relies on tuning transistor strength to enhance parameters. During the read operation, by using CWL (Control Word Line), the pull-down network is made stronger. This protects data from being changed during read operations. Schematics of different 8T cells are drawn in Figs. 4.1 (a-h).

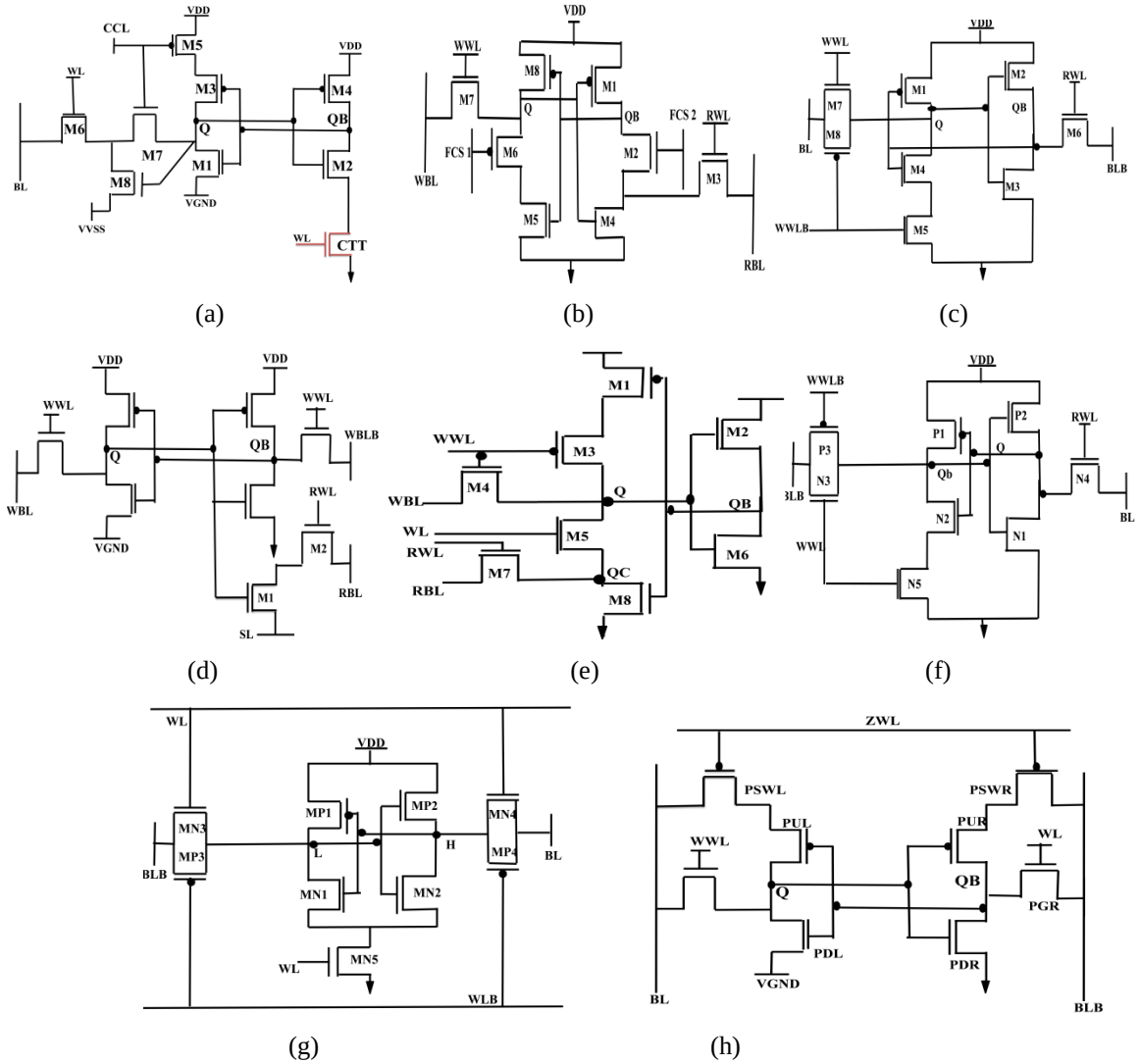


Fig. 4.1. Schematics of (a) $8T_1$, (b) $8T_2$, (c) $8T_3$, (d) $8T_4$, (e) $8T_5$, (f) $8D_1$, (g) $8D_4$, and (h) $8D_5$.

8T-cell by Nii et al., [124] is also a dual-port eight-transistor design. The memory core and write port are exactly the same as a standard 8T. The read port, however, consists of two transistors: one to control the connection to the supply and the other to regulate the read

current flow based on the stored data. Like 7T-a, this design does not use a pass transistor in read operation [6], and the data node is connected to the gate terminal. Faud et al., given a comparative analysis between the CMOS based and carbon nanotube field effect transistor (CNTFET) based SRAM cell. In this article, the authors have designed an 8 transistor cell which has marginally lower the power consumption and supply consumption. Another CNTFET based approach is suggested by Zhou et al.,[102], which improves the efficiency and stability of SRAM cells by two methods such as; positive-feedback-control (PFC) and positive-power-supply-contact (PPC) that increases the overall stability of the cell during read/write mode and reduces the leakage power within the cell during standby mode.

A 10nm FinFET based 8T cell is proposed by Mani et al.,[127] which exhibits enhanced read/write delays i.e., 1.77 and 1.40 times respectively, and a 1.23 times larger area, but in response to that the cell possess a remarkable improvement in stability and power efficiency for IoT applications. Kumar et al., [128] gives another FinFET based 8T cell, remarkable lesser leakage power and read/write delays in comparison with a conventional 6T cell. The architecture is designed with an isolated read path from the storage nodes, and makes it suitable for low power and high speed applications.

In the above discussed cells, write margins, leakage ratio and temperature tolerance [86] are compromised due to various advancements which creates a gap for us to simulate a cell with better write margin and leakage tolerance so we have designed an ultra-low power [73] 8T SRAM cell. Furthermore, all the compared SRAM cells are redesigned using CMOS at 32nm technology node [30] for an ultralow voltage of 400mV to compare with the proposed 8T design [26]. All these cells and the proposed design are stimulated using LT-SPICE. Additionally, the section of this brief that follows provides an explanation of the suggested design.

4.3 PROPOSED SINGLE-PORT 8T SRAM CELL:

In the previous section, it is observed that the temperature variation tolerance, half select disturbance are a major consideration for low supply voltage operating SRAM cells. Therefore, an 8TP SRAM (proposed 8T) cell is constructed to facilitate single line structure of bit cell, this cell has a single bit line to initiate read and write function of the bit cell. The cell structure is constituted by; a set of inverters (Inv. I and Inv. II) that are forming a cross coupled inverter with the help of four transistors where two are p-MOS transistors and other two are n-MOS transistors [11]. A few input signals are controlling all the operations of the

cell such as; Read Word line (RWL), Read Bit line (RBL), Write Word line (WWL), Word line (WL) and Bit line (BL). The 8TP SRAM bit cell is working at an ultra-low operating voltage of 400mV and for CMOS technology of 32nm. The accessing of cell is controlled by access transistors N1 and N6 clearly shown in figure 4.2. For isolated read operation and write operations, cell has a combination of p-MOS and n-MOS transistors. The low power is attained by introducing a transistor N5 that is directly connected to the word line [14, 34].

Table 4.1. Input signals required for various operations of 8TP cell.

SIGNALS / OPERATIONS	HOLD	READ	WRITE '1'	WRITE '0'
BL	H	H	H	H
RWL	L	H	L	L
RBL	H	H	L	L
WWL	H	L	H/L	H
WL	L	H	H	H/L

These 8TP SRAM cell offers better stability for all the operation as the read and write operations of the cell are independent and have their respective dedicated access transistors. The output of Inv.2 is directly connected to transistor N4. Transistors N4 and N1 are providing a separate read-assist path to the cell improving the overall stability of the cell. The major part of a SoC is associated with total power being consumed within the system. The N5 transistor serves the purpose of selectively cutting off power supply to specific parts of the SRAM cell when they are not in use, thereby minimizing power consumption. In the context of the 8TP SRAM cell, the feedback transistor N4 is strategically placed to control the flow of power to certain components, such as the access transistors and inverters, based on the operational state of cell.

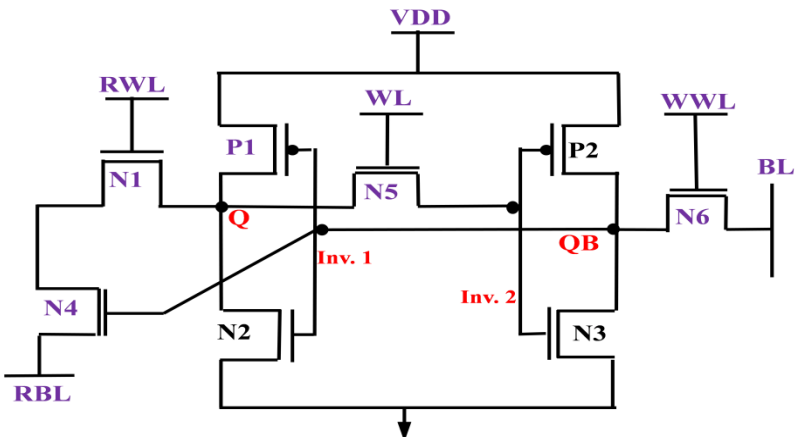


Fig. 4.2 Schematic diagram for proposed 8T SRAM cell (8TP).

Therefore, the power consumption acts as a major factor that needs to be analyzed during its each operation. For each of the three bit cell operations—read, write, and hold—different current requirements apply [85]. Additionally, the value stored in the bit cell determines how much power the circuit uses. In order to determine the power consumption for each operation, the power is calculated for X = 0 and X = 1. This 8TP cell operates on dual bit line structure configuration and transistor N is liable to execute the read operation [89]. Also, proposed outlay of the cell relies only on inv I for the read operation and the inv1 will be in cut off mode as the transistor N1and N4 are in cut off mode.

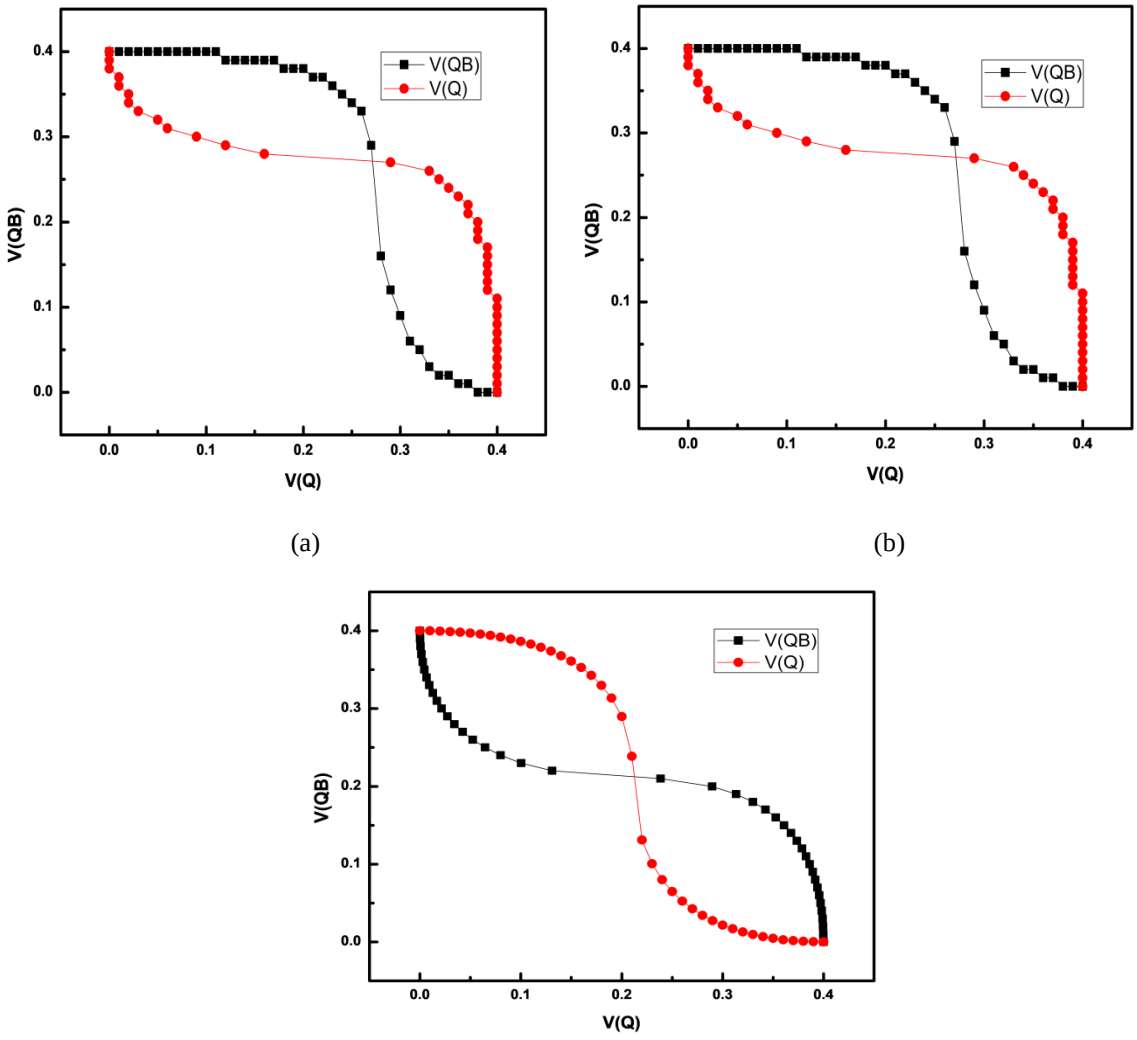
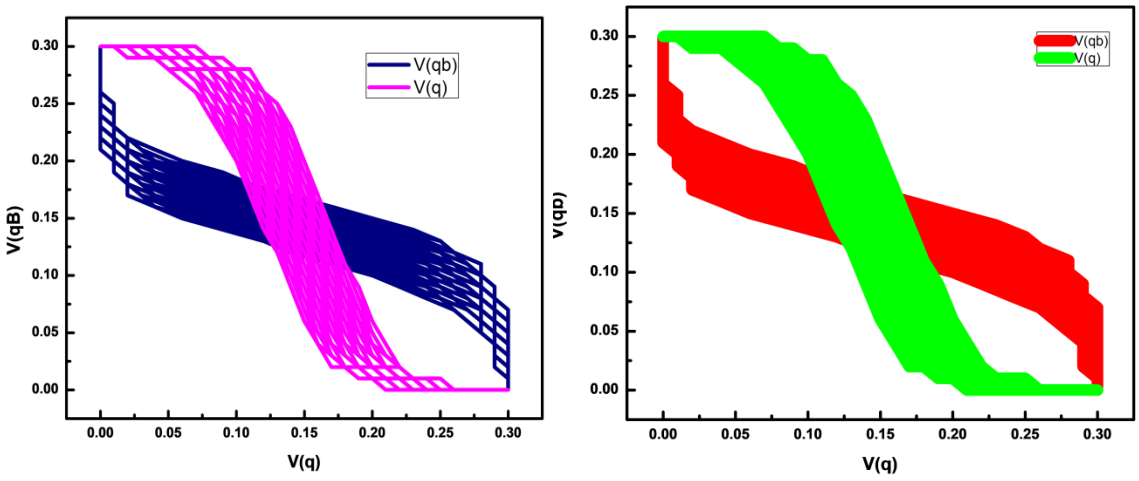


Fig. 4.3 Butterfly curves of (a) HSNM, (b) RSNM, and (c) WM for 8TP SRAM bit cell

The reliable circuit configuration of reading operation is when Q = "0" and QB = "1", respectively. The WBL and WL line remains '0' during the read operation and the signal RWL remains '1' providing a read-assist path for independent read operation [73]. Execution of all the operations of SRAM cell is defined in the latter, half of this paper, Hold operation

for 8TP SRAM cell, bit line BL is kept high (‘1’). All the signals WBL, WWL, RBL and RWL are kept at low (‘0’). Due to this internal signal configuration there will be no supply to the internal access transistors, they will work as cut-off transistors [84]. And the feedback path of both the inverters is also fed with VDD only which keeps the cell in the hold state and corresponds to the given input only [85].



(a) (b)

Fig. 4.4 Monte Carlo simulation for (a) read and (b) hold operation of the 8TP cell.

The butterfly curves for the obtained noise margin values of the cell's read, write, and hold operations are displayed in Figure 4.3. Monte Carlo (MC) simulations also demonstrate the robustness of this cell to local fluctuations [124]. To determine the degree of performance variation in a cell caused by local differences for the read operation of the proposed cell, MC simulations are performed using statistical approaches. The most important parameter in the analysis is probably VTH, which exhibits an independent 6σ Gaussian distribution around the device's mean (μ) VTH value [127]. The proposed cell is also simulated for MC simulations at a sample size of 3000. As seen in the picture, the MC simulation is performed for the 8TP cell's read and hold operations can be clearly seen in figure 4.4 (a) and (b).

For hold operation, the signals RWL, RBL, WWL and BL stay high (‘1’) i.e. kept on and consequently transistors N1, N4 and N5 are in accessing state, as shown in Table 4.1. While for the write operation, WL and BL signals are kept high (‘1’) and the RWL and RBL signals are kept low (‘0’), which in turns activates the transistor N6 and deactivates the transistor N1 and N4. Also for the write function the transistor N5 is activated and it provides a complete feedback path to both the inverters. Input signals for all the function can be seen in Table 4.1, here H represents ‘High’ as input and L represents ‘Low’ as input signal.

4.3.1 Simulation Setup:

The proposed 8-transistor cell (8TP) and the other cells used for comparison all are simulated using the Predictive Technology Model (PTM) for the 32nm technology node, available in Arizona state university library [46]. This PTM-MOSFET model offers a realistic and expandable approach of short channel length effect and gate leakage for nano scale devices. Precisely, this research has been carried out using the PTM high performance (HP) bulk CMOS model, [82] which provides great trade-offs between the power consumption, efficiency and leakage of the SRAM cell designs [80].

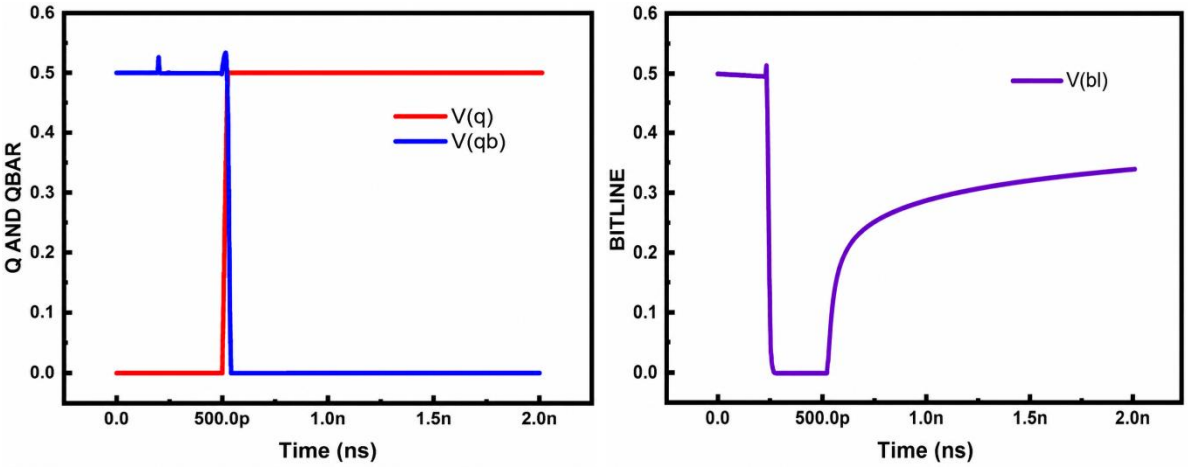
All the simulations are carried out an ultra-low voltage supply of 400mV, and provide an overall significant advancement in terms of reduced noise margins, enhanced susceptibility towards process variations, higher temperature variation tolerance and limited drive strength [89]. Critical phenomena that are particularly noticeable at lower voltages and advanced nodes, such as velocity saturation, drain-induced barrier lowering (DIBL), threshold voltage roll-off, and gate tunnelling effects, are naturally taken into consideration by the PTM models [88]. The PTM 32nm models offer dependable predicted accuracy in sub-threshold and near-threshold voltage regimes and guarantee a consistent and proven foundation for performance comparison. This modelling decision guarantees conformance with accepted industry standards while enabling us to evaluate the behaviour of the SRAM cell under realistic operational conditions [46].

4.3.2 Transient Analysis

When the SRAM bit-cell is in hold mode, when there is no read or write access request . In this condition, the word-line control signal W is not active, which leaves the access transistors switched off and electrically isolates the storage nodes from the bit-line. The two cross-coupled inverters provide regenerative feedback that preserves the data and allows the cell to retain its logic state without external intervention.

During a read operation the bit-line is initially precharged to supply voltage (VDD). The word-line activates the access transistors to connect the storage node Q to the bit-line. If node Q stores logic ‘0’, the charge from the precharged bit-line is discharged to ground via the access path, resulting in a detectable voltage drop on the bit-line, and hence a read-0 condition is achieved. In contrast, when the logic '1' is stored in the node Q, the storage node and the bit-line are at around VDD, so there is no significant current flow or voltage disturbance.. The bit-line remains at its precharged level, corresponding to a read-1 operation. The read

mechanism of the proposed 8TP SRAM cell is shown in figure 4.5(a). The transient response during the write operation of the proposed cell is demonstrated in shown in figure. 4.5(b) is enabled by turning off the feedback path through transistor R1, which reduces the strength of the left storage inverter and thus improves the writability. In the case of a write-0 transition, the bit-line is forced to logic low, and initially logic '1' is stored at node Q.



(a) (b)

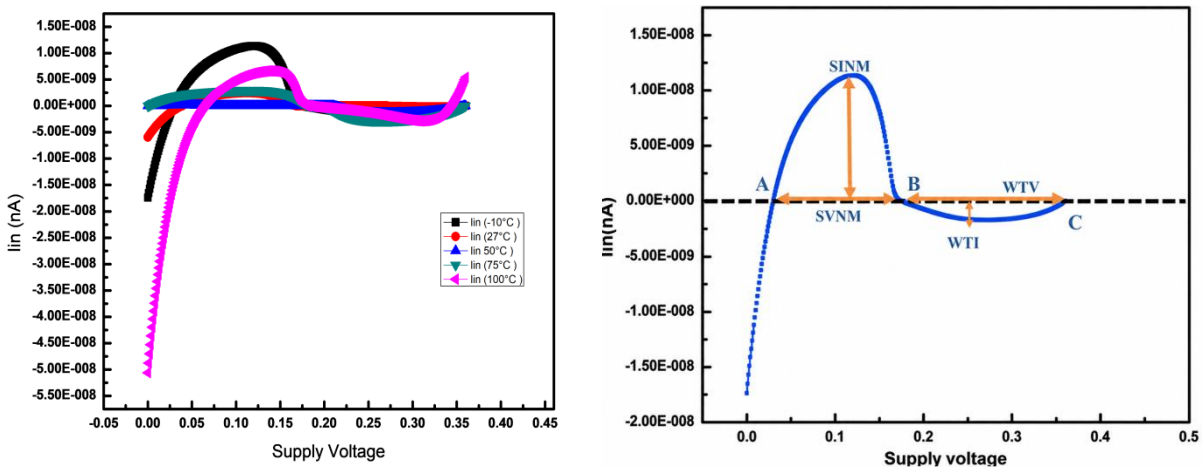
Fig. 4.5 Transient behaviour during read operation of 8TP bit-cell (a) the value stored at nodes Q and QB and (b) bit-line discharge according to value stored at node Q.

When the access transistors are turned on, a conduction path is established between node Q and the low bit-line. This removes the stored charge and causes the node voltage to transition to logic '0'. Instead, the bit-line is driven to VDD for a write-1 operation. This flow of current charges node Q which changes from a logic '0' to a logic '1'. The cross-coupled inverter pair latches and holds the new data value after the write process is completed.

4.3.3 N-curve Analysis

The N-curve approach is a straightforward technique that involves employing inline testers to measure the corresponding current I(Q) after sweeping the voltage at node Q from 0 to VDD when the bit-cell is in read mode and the bit-line is clamped at VDD. At points A, B, and C, the value of I(Q) is determined to be 0 A. Point B is metastable, whereas points A and C are stable. The bit-cell's SVNM is determined by the voltage differential between locations B and A. The highest DC noise at node Q that can be accepted prior to flipping the cell content is known as the Static Voltage Noise Margin (SVNM). The bit-cell's Static Current Noise Margin (SINM), which is the maximum current that can be delivered into the bit-cell before any incorrect flip is registered in the cell content, is determined by the maximum current

between points A and B. It can alternatively be described as the least amount of current that must be injected into the cell in order to flip the bit-cell's stored data.



(a) (b)

Fig. 4.6 (a) N-curve at different temperatures and (b) N-curve for V/I of the 8TP SRAM cell.

The bit-cell's Static Current Noise Margin (SINM), which is the maximum current that can be delivered into the bit-cell before any incorrect flip is registered in the cell content, is determined by the maximum current between points A and B as shown in figure 4.6 (a &b). It can alternatively be described as the least amount of current that must be injected into the cell in order to flip the bit-cell's stored data. The SVNM and SINM of an SRAM bit-cell determine its read stability. Thus, a bit-cell's readability can be determined using their product, Static Power Noise Margin (SPNM). The area under the curve between points A and B can be used to calculate SPNM. The SPNM should be greater for improved read stability. Therefore, as long as a bit-cell has a high SINM, it can still have greater read ability even if its SVNM is little low.

4.4 PERFORMANCE COMPARISON OF PROPOSED 8T CELL WITH DIFFERENT 8T CELLS

This part comprises of all the simulated results observed for the suggested 8TP cell as well as the other cells taken for comparison. Using a 32nm CMOS technology node and maintaining a standard temperature of 28°C, the complete cell has been constructed at an ultralow voltage of 400 mV [89]. Numerous analyses, including process corner fluctuations, temperature fluctuations, dynamic power consumption, standby power consumption, Ion/Ioff ratio, voltage scaling, stability (hold and read), and writability, are used to compare the different cells [82].

4.4.1 Static Analysis

Reliability of an SRAM cell relies upon the value of its SNM for all the operations, the cell which has a higher value of SNM is considered as most reliable. Thus, all bit cells' SNM values are computed and contrasted with those of the pre-existing cells. The butterfly curve in figure 4.3, which is produced by 8TP SRAM cells with a single bit line, is typically used to illustrate the read and hold SNM for the bit cell. It is then compared to different single bit line and dual bit line accessing strategies that are explained by imposing the bit line's voltage transfer characteristics during hold and read [33]. For the read, hold, and write operations of the suggested design, the observed static noise margin values are 181, 178, and 204 mV, respectively. The SNM is measured by taking the size of the square that can fit inside the butterfly curve's lobe.

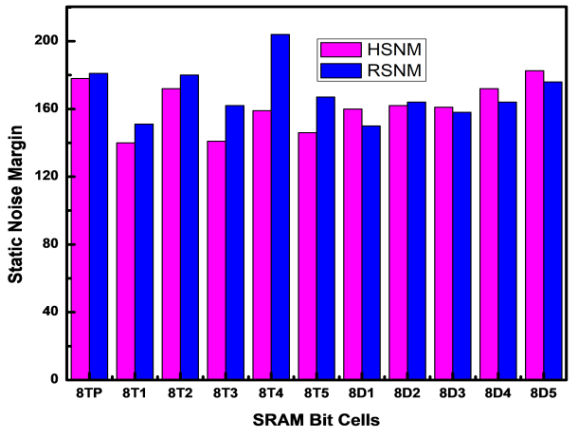


Fig. 4.7. Comparison of HSNM & RSNM parameters for different existing single – ended and dual– ended SRAM cells.

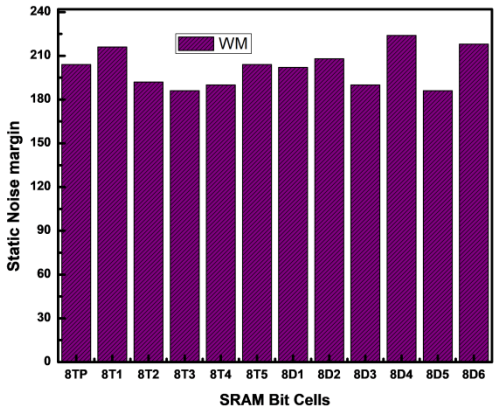


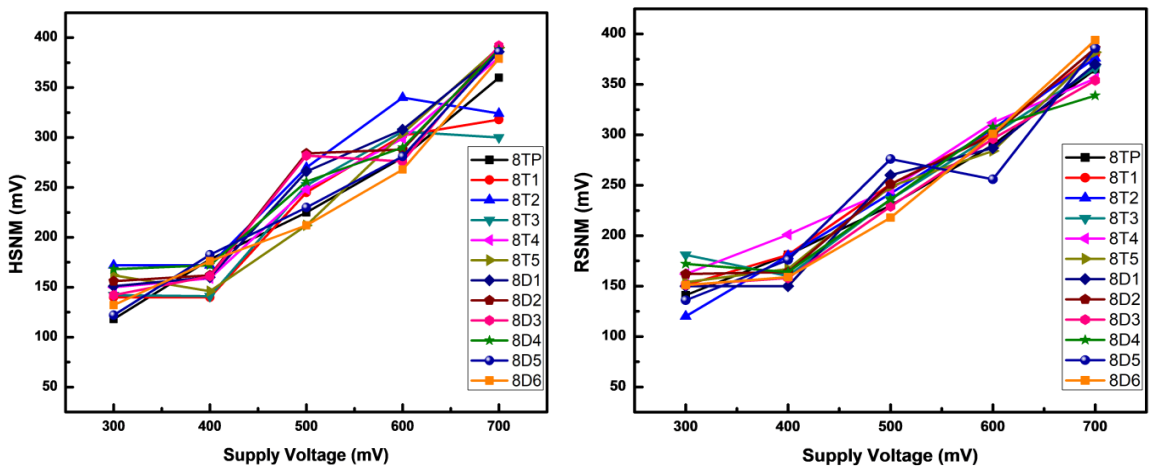
Fig. 4.8. Comparison of WSNM parameter for different existing 8T SRAM cells.

Here, the comparison has been sketched out for different single- ended 8T SRAM cells such as $8T_1$ [76], $8T_2$ [82], $8T_3$ [78], $8T_4$ [81], $8T_5$ [84], $8D_1$ [79], $8D_2$ [83], $8D_3$ [77], $8D_4$ [80],

$8D_5$ [85], $8D_6$ [75], with the 8TP bit cell on the basis of their obtained HSNM, RSNM and WM for all the 8T cells. All the analyses are at similar voltage keeping technology node also same, the results are expressed in the figure 4.7 and 4.8. The graphical demonstation of static analysis of various 8T SRAM cells leads to the inference that the 8TP SRAM cell is better 1in terms of static performance as compared to the other bit cells.

4.4.2 Voltage Scaling:

The effect of scaling of supply VDD on the performance of various bit cells was explained in detail in here. The 8TP bit cell was found to maintain a notable level of performance across various VDDs. However, in this case, the VDD values were raised in 100 mV steps. Figure 4.9, illustrates how to assess the impact of voltage change by ranging from 300 to 700 mV in steps of 100 mV.



(a) (b)

Fig. 4.9 (a) HSNM and (b) RSNM for existing single – ended and dual – ended SRAM at supply voltages ranging from 300 – 700mV.

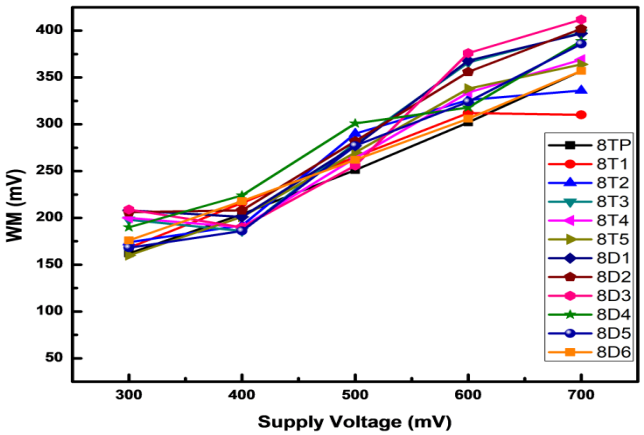


Fig. 4.10 Write Margin for existing single – port and dual – port SRAM cells at supply voltages ranging from 300 – 700mV.

The findings that the cell has more dependable performance are supported by the fact that the static margin of cells increases gradually as the VDD increases [19]. Additionally, because the signals in a digital circuit tend to fluctuate slightly due to a variety of disturbances and outside influences, it is exceedingly challenging to supply exact voltage [6]. As a result, fluctuations in VDD between 300 and 700 mV are analysed in order to analyse the effects of very small variations in a cell's voltage [20]. This will help us better understand how small changes in voltage affect a cell's overall performance. Figures 4.9 (a) and (b) show the values of HSNM and RSNM for the 8TP cell whereas figure 4.10 showcases the observed values of write margin for various voltage variations.

4.4.3 Dynamic Power Consumption

The constant increase in demand of portable low power systems has motivated designers to lower the power consumed for entire circuit. Because each bit cell in the cache memory must be copied in order to create arrays, it accounts for a sizable amount of the system's overall power consumption [25, 28]. Therefore, lowering the power consumption of each individual cell is a crucial factor for designers. Every tiny drop in a single cell's power has a multifaceted impact on the memory setup's overall power performance [30].

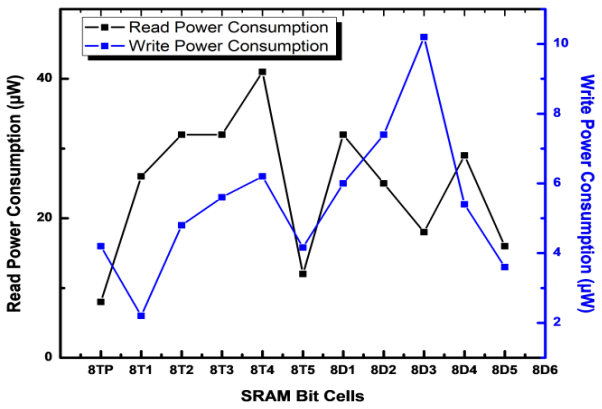


Fig. 4.11 Power consumption of different 8T SRAM cells in comparison with 8TP cell.

Here, the comparison has been sketched out for different single- ended 8T SRAM cells such $8T_1$, $8T_2$, $8T_3$, $8T_4$, $8T_5$, $8D_1$, $8D_2$, $8D_3$, $8D_4$, $8D_5$, $8D_6$, with the 8TP bit cell in terms of their obtained dynamic power consumed by the cell, shown in figure 4.11. Static power consumption and dynamic power consumption are two broad categories into which a cell's power consumption falls. Static power consumption, which is experimentally equivalent to VDD multiples of leakage current, results from induced leakage current within the circuit [28]. The dynamic power is once more divided into two categories: read power consumption and write power consumption. After analysing all the 8T cells, it is observed that the $8D_3$ has

maximum value of write power consumption while $8T_4$ cell has the maximum value of read power consumption [31] amongst all the SRAM cells and the 8TP cells has lowest values for both read and write power consumption.

4.4.4 I_{ON}/I_{OFF} Analysis

The relationship between the leakage current and read current is known as the I_{ON}/ I_{OFF} ratio. Larger the I_{ON}/ I_{OFF} ratio larger the size of an SRAM array that can be created by the designers. Therefore, if a cell has a larger current ratio it implies that the designers can employ larger number of bit cells in each column. This in turn is also decreasing the peripheral circuit of read topology in the architecture. So, a cell that has a greater ratio is preferable over other bit cells. Here, the comparison has been sketched out for different single- ended 8T SRAM cells such as $8T_1$, $8T_2$, $8T_3$, $8T_4$, $8T_5$, $8D_1$, $8D_2$, $8D_3$, $8D_4$, $8D_5$, $8D_6$, with the proposed 8TP bit cell.

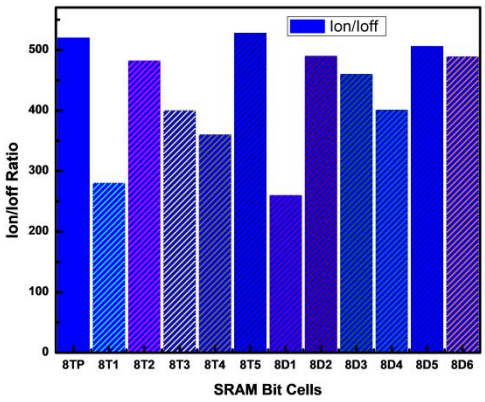


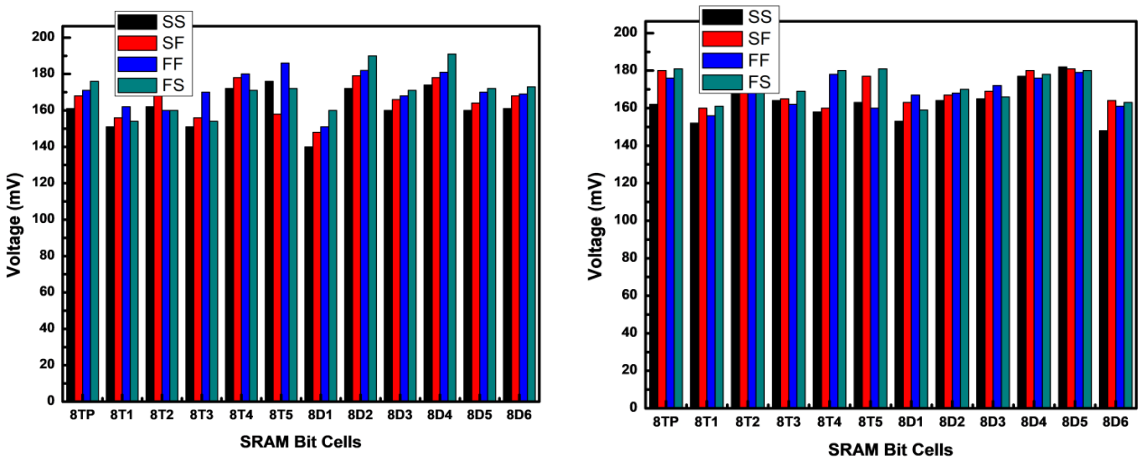
Fig. 4.12 I_{ON}/I_{OFF} ratio of various single – ended SRAM cells and dual – ended SRAM bit cells.

This ratio tends to define the versatility of a cell to be incorporated in an array of different sizes. The obtained values of all the 8T cells are demonstrated with the help of a graph. And it is clearly observed that the 8TP cell possess maximum value for I_{ON}/ I_{OFF} ratio given in figure 4.12, hence this cell can be used to form any order array efficiently [21]. It can be clearly said that if a cell possess higher value of the ratio of current, so that cell can be deployed in an arrangement to form an array of desired size. This in turn is also decreasing the peripheral circuit of read topology in the architecture.

4.4.5 Global Variations

If a discrepancy is discovered during the device fabrication process, the global variation analysis for the hold as well as the read operation is a way to assess the dependability of any cell. The 8TP cell exhibits the best performance out of all the cells that were compared, and

the best performance is attained for the SF corner because the PMOS processing is fast and the NMOS processing is slow at this corner [108], which tends to create a performance gap between two devices. Therefore, the 8TP SRAM cell has the best SF performance. 8TP cells perform similarly to various 8T cells these are $8T_1$, $8T_2$, $8T_3$, $8T_4$, $8T_5$, $8D_1$, $8D_2$, $8D_3$, $8D_4$, $8D_5$, $8D_6$, in terms of HSNM and RSNM. The observed values for hold noise margins of cell at the different corners are given by figure 4.13 (a) and read noise margins values in figure 4.13 (b) [3, 21]. The 8TP cell is showing a maximum variation of 44 mV.



(a) (b)

Fig. 4.13 (a) HSNM and (b) RSNM at SS, SF, FF and FS corner.

The HSNM variations are highlighted by the observed higher value of the HSNM of 8TP cell at various corners. This may conclude that the cells with lesser HSNM variation are having better values for other operations. Also having lesser values states that cells are less likely to be reliable in terms of stability. Operation of read shows the vulnerability of the cell [6, 28]. Therefore, variation in read operation represents in RSNM of cells which has higher reliability issues. Also, a cell that represents a very lesser performance in terms of static Read noise margin is considered as less reliable.

4.4.6 Temperature Variation

Temperature increase in the surroundings of a cell will have various harsh effects on the performance of a cell specifically during hold operation because the cell remains in static condition during hold. The WM and HSNM/RSNM variation of temperature are illustrated in figure 4.14. The 8TP cell has the least variation in HSNM, RSNM and WM performance with temperature variation [3, 29] of 0.118 mV/°C, 0.120 mV/°C, and 0.156 mV/°C respectively, which is making the cell robust with variation in temperature. 8Tp is compared with different 8T cells to understand the capacity to be resilient with variation temperature.

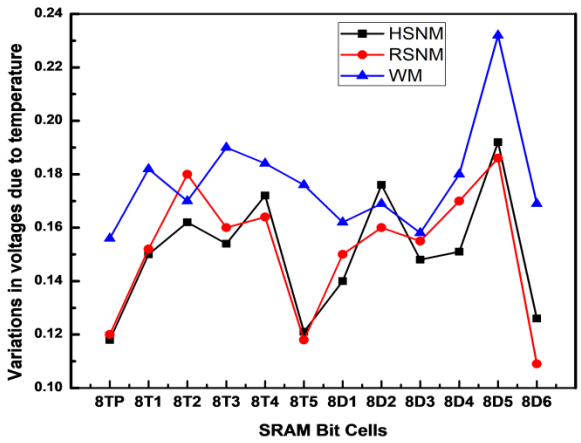


Fig. 4.14 Temperature variations for HSNM**,** RSNM and WM for various 8T cells.

All 8T cells can be observed for their fluctuations in HSNM being 0.15, 0.162, 0.154, 0.172, 0.121, 0.14, 0.176, 0.148, 0.15, 0.192, and 0.126 mV/°C respectively and fluctuations in RSNM being 0.152, 0.18, 0.16, 0.164, 0.118, 0.15, 0.16, 0.155, 0.17, 0.186, and 0.109 mV/°C respectively [31]. While for same 8T cells fluctuations in WM being 0.182, 0.17, 0.19, 0.184, 0.176, 0.162, 0.169, 0.158, 0.18, 0.232, and 0.169 mV/°C respectively. Here, as an observation it can be concluded that these cells will not be the first choices for any application where temperature variations are a major concern.

4.4.7 Standby Power Analyses

The total power consumed by the design has a major effect on circuit of memory as SRAM occupies a larger part of SoC designs. Therefore, it is of utmost important to analyze the power that is being consumed by the SRAM cell for its each operation. These analyses for bit cells will be different for three different operations of cells such as; write, read and hold of bit cell. Additionally, the value stored in the cell determines how much power the circuit uses. Therefore, the power consumption is calculated for X = 0 and X = 1 for each process [22]. Hereby, it may provide an overall understanding of the power consumed by the cell.

$$P_{Total} = P_{Dynamic-switching} + P_{short\ circuit} + P_{Leakage} \quad (4.1)$$

$$P_{Dynamic} = P_{Dynamic-switching} + P_{short\ circuit} \quad (4.2)$$

$$P_{Total} = P_{Dynamic} + P_{Leakage} \quad (4.3)$$

So, to obtain the total power the main considerations would be $P_{Dynamic}$ and $P_{Leakage.}$ The comparison for the obtained power for different 8T cells in given by figure 4.15.

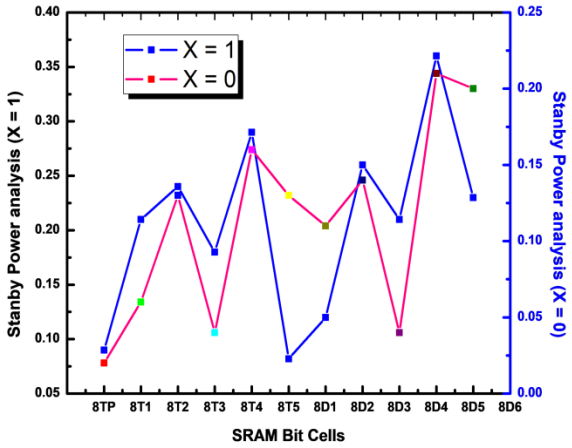


Fig. 4.15 Standby power consumption of various single – ended SRAM cells and dual – ended SRAM bit cells.

The total obtained standby power of 8TP is significantly reduced by a factor of 2.3, 2.66, 1.8, 3.2, 0.8, 2.4, 2.9, 2.2, 4.0, 2.5, and 1.2 for X=1 and is reduced by 3, 6.5, 2, 4.8, 1.5, 5, 1.25, 4.5, 2.5, 4, 8, and 4 for X=0 in comparison with pre-existing single-ended 8T cells such as; $8T_1$, $8T_2$, $8T_3$, $8T_4$, $8T_5$, $8D_1$, $8D_2$, $8D_3$, $8D_4$, $8D_5$, $8D_6$, respectively.

4.4.8 Dynamic Read and Write Delay

Another parameter for the analysis is the delay during the execution of read and writes operations. Figure 4.16, demonstrates the comparison for write delay and read delays [27] of single-ended 8TP SRAM bit cell with other single ended 8T cells; $8T_1$, $8T_2$, $8T_3$, $8T_4$, $8T_5$, $8D_1$, $8D_2$, $8D_3$, $8D_4$, $8D_5$, $8D_6$. The write delay is total time required from the time WL is started executing to the time taken during writing process 1/0 on the storage node.

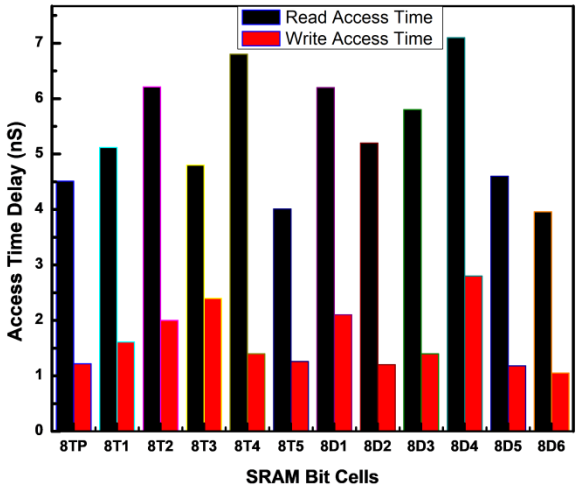


Fig. 4.16 Access time delay analysis for various 8T SRAM bit cells.

The obtained read and write delay for the 8TP bit cell is 4.51 nS and 1.22 nS respectively. The graphical representation shows that for the dynamic operations of all SRAM cells it can

be clearly stated that 8TP cell possesses better reliablity for dynamic read and write operations. Read/write access time is the parameter that defines the reliability of the cell in terms of execution. Comparison of different 8T SRAM cell topologies is summarized in Table 4.2.

Table 4.2. Parametric comparison of different 8T SRAM cell topologies.

SRAM Cells	Hold SNM (mV)	Write Margin (mV)	Read SNM (mV)	Ion/Ioff Ratio	Read Access Time (nS)	Write Access Time (nS)	Read power (µW)	Write power (µW)	Area (μm^2)	EQM (10^3)
8TP	**178**	**204**	**181**	**520**	**4.51**	**1.22**	**8**	**4.2**	**1.6732**	**16.04**
8T1 [76]	140	216	151	280	5.12	1.61	26	2.2	1.605	6.033
8T2 [82]	172	192	180	482	6.21	2.0	32	4.8	1.247	2.498
8T3 [78]	141	186	162	400	4.8	2.4	32.02	5.6	1.179	1.540
8T4 [81]	159	190	204	360	6.8	1.4	41	6.2	1.886	1.019
8T5 [84]	146	201	167	528	4.01	1.26	12	4.16	1.228	15.82
8D1 [79]	160	202	150	260	6.2	2.1	32.1	6.0	2.031	1.088
8D2 [83]	162	208	164	490	5.2	1.2	25	7.4	1.863	2.569
8D3 [77]	161	190	158	460	5.8	1.4	18	10.2	1.33	2.437
8D4 [80]	172	224	164	401	7.1	2.8	29	5.4	1.748	1.161
8D5 [85]	182.6	186	176	506	4.6	1.18	16	3.6	1.257	15.12
8D6 [75]	176.2	218	159	489	3.96	1.05	7.6	2.9	1.88	35.44

However, the main highlight of this design is the improved write margin of the 8TP cell which is 204 mV i.e. near to VDD/2, while for other cells the WM is quite away from VDD/2 and only 8T5 and 8D1 cells has WM nearer to the metric. The 8TP is compared to other 8T cells such as; $8T_1$, $8T_2$, $8T_3$, $8T_4$, $8T_5$, $8D_1$, $8D_2$, $8D_3$, $8D_4$, $8D_5$, $8D_6$, respectively.

4.5 HIGHLIGHTS OF IMPORTANT RESULTS

In this chapter, it is observed that the major advantages of this 8TP cell are temperature tolerance, enhanced write margin, technology node reduction and scaling of voltage. The

proposed work is been analysed for 32nm CMOS technology. 8TP is compared with various pre-existing dual - ended and single – ended SRAM cells. All SRAM cells are functioning at an ultra-low voltage of 400 mV. The 8TP SRAM cell is maintaining a 178 mV hold SNM and 181 mV read SNMs, while write margin is 204 mV which is best among the other compared cells. Cell is eligible to present a remarkably improved performance as it refined for all three operations of cell by improving the static noise margins of operations namely, hold, read, and write. The access time for read and write process of cell is 4.51nS and 1.22nS respectively. Also, this cell has a very low almost negligible leakage power and leakage current. The variation in temperature analysis and analysis of process corner are calculated to showcase the overall reliability of the design. The temperature variation analysis of the proposed design yields 0.120, 0.118 and 0.156 mV/° C variations in the RSNM, HSNM and WM for cell, respectively. The 8TP SRAM cell is also found to be consuming lesser power for its operations.

CHAPTER-5

TCAM BLOCK USING 8T SRAM CELL FOR LOGIC OPERATIONS

5.1 INTRODUCTION

Sorting incoming packets according to the routing table and placing them on the path that leads to the designated user is the router's main job. Every router searches for the path to the intended recipient using the information it has in the routing table [97]. In order to scale IoT components, it is now essential to design and construct components for network that function more efficiently and quickly [99]. Thus, SRAM is frequently used as a nanoscale alternative. Researchers are working very hard to develop the facilities, circuits, processes, and connectivity. Numerous surveys or studies have reported and recorded notable advancements in the circuits, systems, and links. This work is representing the design of the 8T SRAM-based TCAM cell [104] and its array.

The suggested TCAM cell is and its array's average power consumption, peak power, and search speed [113]. A hash function can legitimately carry out the lookup with a single memory transaction. However, the worst-case search time [49] can be significantly longer than tree searches, depending on the hashing method and table size. Consequently, the majority of software-based lookup functions are implemented using hardware architectures. Hardware can use content-addressed memory to handle table search results efficiently. CAM will carry out SEARCH tasks in addition to READ and WRITE. The simultaneous SEARCH activity makes the CAM-based table search faster [112].

5.1.1 Binary CAM

Binary Content Addressable Memory (BCAM) is a high-speed memory architecture that can perform parallel data search operations by comparing the input search data with all the stored memory words simultaneously. BCAM differs from traditional SRAM or DRAM in that it retrieves data by content matching rather than by memory addresses, which significantly reduces search latency in applications requiring fast lookup functionality [98]. The BCAM operates with binary logic states, where each stored bit can be either logic ‘0’ or logic ‘1’. In the search operation, the incoming search word is broadcasted over all rows of the memory array and each memory cell performs a local comparison between stored bits and search bits. A full match activates the corresponding match line, indicating that the stored word has been

successfully found. The SRAM-based BCAM cells are widely used due to their high speed, low static power and compatibility with the CMOS VLSI technologies. BCAM architectures are integrated with conventional SRAM cells like 6T, 8T, 9T and more transistor topologies to improve read stability, write margin and search reliability under scaled supply voltages [100]. The binary data are stored in the SRAM latch of the SRAM-based BCAM array and the comparison operation is done by the additional comparison circuitry through the search lines and match lines. This work presents a write-optimized 8T/9T SRAM cell with an isolated read path for reduced read disturbance and increased robustness in simultaneous search operations [104].

The BCAM blocks are widely used in networking hardware, packet forwarding engines, cache tag memories, translation look aside buffers (TLBs), pattern matching systems and embedded processors where deterministic and ultra-fast search capability is a must. However, as technology scales towards deep sub-micron nodes, BCAM architectures suffer from leakage power, reduced static noise margin, process variations and search energy consumption. Therefore, the recent research concentrates on low-power SRAM-assisted BCAM structures, multi-port SRAM architectures and hybrid memory arrays to achieve better search efficiency and reliability for high-density integrated systems.

5.1.2 Ternary CAM

Ternary Content Addressable Memory (TCAM) is an improved version of the content addressable memory. It can store and search three logic states; logic ‘0’, logic ‘1’ and a “don’t care” state represented as ‘X’. Like BCAM, TCAM makes massive parallel comparisons against the entire memory array in one clock cycle. This allows very high search throughput and deterministic lookup performance. SRAM-based TCAM architectures are highly preferred in modern VLSI systems due to their use of standard CMOS SRAM structures with additional comparison and masking circuits. In the SRAM-based TCAM cells, the ternary data combinations are represented by multiple SRAM storage nodes [124]. The match lines are connected with search transistors which perform the parallel comparison operations. Depending on the SRAM topology used, TCAM cells can use 8T, 9T, 10T, and 11T etc. transistor configurations to improve search stability, reduce leakage power and achieve robust low voltage operation [125].

The operation of a TCAM array involves recharging the match lines and then performing a parallel comparison of the ternary data stored in the array with the incoming search patterns.

Any bit mismatch in a row releases the corresponding match line and a full or masked match maintains the match line active. The “don’t care” state enables selective masking of certain bits, thereby enabling flexible pattern matching and prefix-based searching which are important in networking and associative processing applications [126]. In order to address these limitations, recent research on SRAM based TCAMs has focused on low power search schemes, segmented match-line architectures, dual-port SRAM integration and hybrid heterogeneous TCAM arrays using alternate SRAM cells such as 8T, 9T and 11T configurations. These hybrid architectures improve the reliability of the search, reduce dynamic power consumption, enhance static noise margins, and enable energy-efficient operation under near-threshold supply voltages. SRAM-based TCAMs are highly attractive for next-generation high-performance computing and networking systems [134]. The following objective is framed here to design a TCAM block using single port 8T SRAM cell:

“To design and compare a content addressable memory (CAM) using single-port and dual-port SRAM bit cells”

To attain this objective, a CAM block is designed using 8T SRAM cell, for low power searching and logical operations. Different CAM architecture are studied and analysed to design the proposed CAM block. The proposed SRAM based CAM is consuming low power and have lower matching and mismatching power consumption when compared to other SRAM cell based TCAM blocks. This chapter is characterized as follows; the introduction, objective and methodology of the objective are explained in the section 5.1 of this chapter. Different conventional CAM type methodologies and architectures are explained in section 5.2. This is followed by the proposed designs for TCAM cell architectures made with 8T SRAM cell in the section 5.3 of this chapter. The fundamental construction of the 8T based TCAM cell [14], which can perform SEARCH, WRITE, and READ operations and the operation, comparison with different transistor count SRAM cell and their structure for the TCAM block are illustrated in section 5.4. Finally, the key observations of the chapter are characterized in section 5.5.

5.2 COMPARISON OF DIFFERENT CONVENTIONAL CAM BLOCK ARRANGEMENTS

In the last few decades, many CAM architectures have been proposed to facilitate high-speed associative search operations with improved power efficiency and scalability. Typically these architectures are based on NOR, NAND, XOR or XNOR CAM cells which are usually

implemented as a conventional 6T SRAM storage core with an additional comparison circuitry for search operations. A NOR-type CAM cell typically comprises 10 transistors, where two NMOS access transistors are connected to the storage nodes for the read/write operation [136].

5.2.1 NOR Type CAM cell

The NOR CAM architecture is made of a pair of cross-coupled CMOS inverters made of transistors P1, P2, N1 and N2 which make the bistable storage element of the cell as represented in figure 5.1 (a). The internal nodes Q and QB represent the stored data bits. The write operation is implemented by two NMOS access transistors, commonly referred to as N3 and N4, that are controlled by the word line (WL) and connect the storage nodes to the differential bit lines BL and BLB [99]. The comparison functionality is realized by four NMOS transistors, N5, N6, N7, and N8, which form the search and match-line evaluation network. In the NOR-type configuration, each CAM cell offers an independent and parallel discharge path between the match line (ML) and the ground.

Prior to a search operation, the ML is precharged to V_{DD} by a PMOS precharge transistor driven by a signal CTRL [100]. The PMOS transistor has its source terminal tied to V_{DD} and its drain tied to ML. The gate terminal is used to provide the control signal to enable or disable the pre-charge phase. During the write operation, the word line WL is asserted, which allows the input data applied on BL and its complement on BLB to be stored in the cross-coupled inverter pair. After latching the data, the WL is turned off to isolate the storage cells during comparison. In the search phase complementary search inputs SL and SLB are applied to the comparison circuitry. The stored data is compared in parallel with the incoming search data across all CAM cells [102].

The comparison operation produces the match/mismatch condition. If the stored bit is the same as the search bit, no conductive discharge path is created, the ML remains charged at V_{DD}, and a match is indicated. In case of mismatch, however, one of the comparison transistors connects a conducting path from ML to ground, discharging the ML voltage towards GND [106]. The parallel discharge structure of NOR CAM cells gives the search operation a very high speed, but this architecture generally suffers from increased power dissipation, since multiple match lines may discharge simultaneously during large-scale search operations.

5.2.2 NAND Type CAM cell

Unlike NOR architecture, NAND CAM cells use a serial discharge scheme for evaluating the match line, which results in much lower search power consumption. Like the NOR CAM cell, the NAND CAM structure has a standard 6T SRAM storage core with two cross-coupled CMOS inverters (transistors P1, P2, N1 and N2). These inverters keep the stored logic values at nodes Q and QB in a stable bistable state [112].

The NAND CAM cell has access transistors connected to the bit lines BL and BLB, controlled by the word line WL for write operations. The WL is turned on and the differential input data are written into the SRAM latch structure during data storage. After the write operation is completed, the WL is disabled to isolate the stored data from external disturbances. In contrast to the NOR architecture, the comparison circuitry of a NAND CAM cell is implemented in a cascaded series configuration as shown in figure 5.1 (b). Each CAM cell provides a conditional series conduction path in the overall match-line discharge chain.

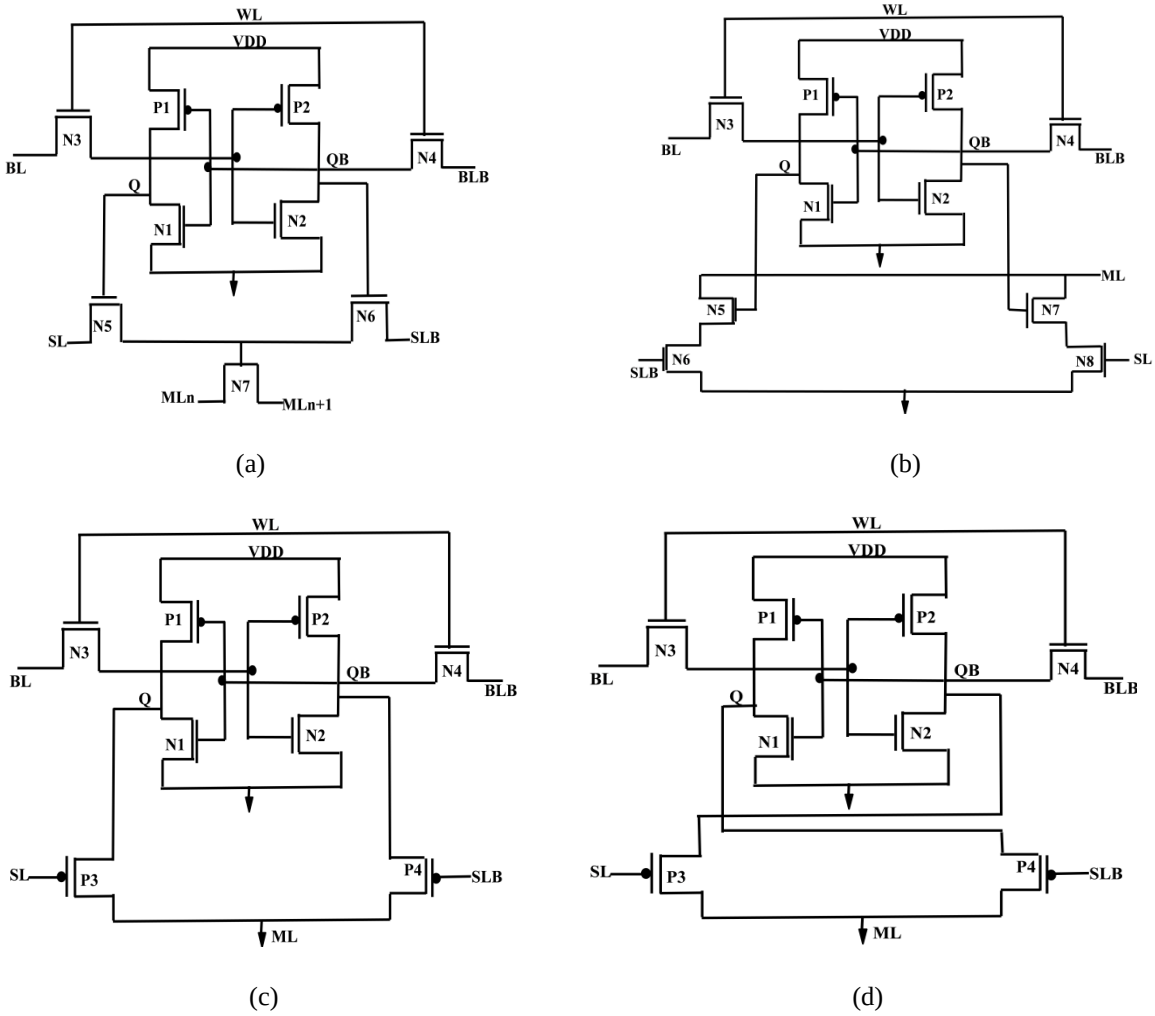


Fig. 5.1 Conventional CAM Cells for (a) NOR (b) NAND (c) XOR, and (d) XNOR logics.

The comparison transistors compare the search inputs SL and SLB with the stored data at Q and QB. The entire conducting path is formed only if all the cells of the search word satisfy the matching condition. Before the search operation starts, the match line ML is pre-charged to VDD by a pre-charge transistor of PMOS [161]. The NAND configuration typically connects the match line of a CAM cell to the next cell in the search chain, creating a serial evaluation structure. If all the stored bits agree with the corresponding search input, the discharge path is not enabled and the ML maintains its pre-charged voltage level, indicating a valid match condition. In case of a mismatch in any bit position, the serial conduction path is broken and the evaluation signal is not propagated properly, thus indicating a mismatch [134].

The serial discharge mechanism of the NAND CAM cells leads to a generally smaller dynamic power consumption compared to the NOR CAM architectures, particularly for large memory arrays. However, the cascaded evaluation paths may have higher series resistance and propagation delay which degrades search speed and NAND CAM structures are usually slower than NOR CAM implementations. In low-power applications where energy efficiency is more important than maximal search performance, NAND CAM cells are thus generally preferred.

5.2.3 XOR Type CAM cell:

The CAM cell of XOR type is designed to realize the associative search function with a lower number of transistors and a simpler comparison operation as represented in figure 5.1(c). The basic XOR CAM architecture uses eight MOSFETs, in which two NMOS transistors (N3 and N4) are used as access transistors for read and write. These access transistors are controlled by the word line (WL) and connect the storage nodes to the differential bit lines BL and BLB [135]. The storage section of the XOR CAM cell is formed by two cross-coupled CMOS inverters which consist of transistors P1, P2, N1 and N2. Each inverter consists of one PMOS and one NMOS transistor in a complementary configuration. The cross-coupled configuration provides bistable operation that allows the binary information to be stored reliably at the internal nodes Q and QB. These storage nodes store complementary logic values of the stored data bit [136].

In the XOR CAM architecture, the comparison circuit is implemented with two PMOS transistors, P3 and P4, which are directly involved in the search process. In contrast to NOR- and NAND-based CAM architectures, the XOR CAM cell does not need a dedicated match-

line pre-charge mechanism [137]. This leads to savings in the cost of extra pre-charge circuitry and also in the reduction of dynamic power consumption from repeated charging and discharging of the match line. The cell has input terminals BL, BLB, WL, SL and SLB, and the main output nodes are Q, QB and ML. The word line WL is activated during the write operation, so that the data applied to BL and its complement on BLB are transferred into the cross coupled inverter pair. The WL signal is then turned off to isolate the storage nodes and the stored information [138].

Table 5.1. Dynamic power (in µW) for different existing 1 bit CAM cells at voltage range of 0.7 – 1.2 V.

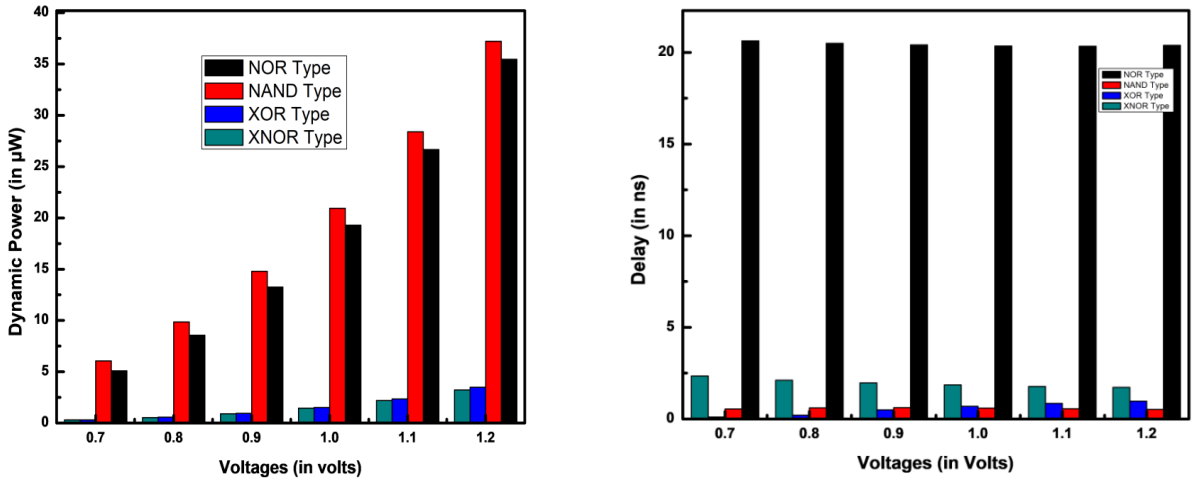
Input Voltage (V)	NOR CAM	NAND CAM	XOR CAM	XNOR CAM
1.2	35.47	37.23	3.5	3.236
1.1	26.67	28.39	2.346	2.199
1	19.29	20.94	1.518	1.439
0.9	13.26	14.79	0.9438	0.901
0.8	8.554	9.857	0.5615	0.5362
0.7	5.098	6.048	0.3166	0.3006

The search lines SL and SLB are driven with the input search data and its complement during the search operation [162]. The comparison transistors are used to verify the logical relation between the stored data and the incoming search data by means of XOR functionality [96]. The mismatch condition will activate the comparison path and change the state of the match line ML, and the matching condition will leave the state of the match line ML unchanged. This XOR CAM cell does not need continuous pre-charge and discharge operations, and therefore is more energy efficient and less switching activity than conventional NOR CAM architectures [101]. Moreover, the reduced number of transistors and the simplified comparison circuitry make the XOR-based CAM cells suitable for compact and low-power memory applications. However, the overall search performance and sensing reliability is highly dependent on the transistor sizing, process variations and robustness of the match-line sensing circuitry in scaled CMOS technologies [139].

5.2.4 XNOR Type CAM cell

The XNOR CAM cell uses eight MOSFETs, with two NMOS acting as access transistors (N3, N4) that allow access to the cell; the comparison circuit consists of the two PMOS transistors (P3, P4); the cross-coupled inverters consist of the remaining four transistors (P1, P2, N1, N2), as illustrated in figure 5.1(d); an inverter consists of one NMOS and one PMOS

(P1, N1 and P2, N2); the storage component of a CAM cell is composed of cross-coupled inverters; the inputs are BL, BLB, WL, SL, SLB; the outputs of the XNOR CAM cell circuit are Q, QB, and ML; ML does not need to be pre-charged. For BL, its complement is given, and for BLB, it is to be written. The data is then stored in the CAM cell [140]. The information in the CAM is assessed during the compare operation to search the input data SL and SLB [163]. For the comparison operation, there are two output states. Both of them are mismatched. When the stored information and the search information are same, the condition is called a match; otherwise, it is called a mismatch [18]. ML increases in the match state and decreases in the mismatch state. WL is turned off when performing comparisons [141].



(a) (b)

Fig. 5.2 (a) Dynamic Power and (b) Delay for different CAM cells.

The values of the dynamic power and delay are calculated by re simulating the pre-existing CAM block types for a voltage range of 0.7 – 1.2 V, for a standard 6T based configuration and that is compared with the proposed 8T based configuration in later sections [142]. The obtained values for dynamic power and delays of different CAM block configuration is represented in Tables 5.1 and 5.2, respectively. Dynamic power is defined as that amount of power consumed by the CAM block when writing or comparing.

Table 5.2. Delay (in ns) for different 1 bit CAM cells at different voltages

Voltage (V)	NOR CAM	NAND CAM	XOR CAM	XNOR CAM
1.2	20.385	0.5208	0.9776	1.7255
1.1	20.34	0.5607	0.8518	1.7815
1	20.345	0.5966	0.6959	1.86
0.9	20.405	0.6189	0.4954	1.9675
0.8	20.495	0.6051	0.2103	2.117
0.7	20.63	0.5441	0.1060	2.347

The obtained values of the dynamic Power (in μW) is demonstrated in Table 5.1 for a variety of 1 bit CAM cells, such as NOR, NAND, XOR, and XNOR, with a defined voltage range from 0.7 V to 1.2 V and also represented in figure 5.2. It is better to consume less energy. XNOR CAM cells have obtained dynamic power that is 42.5% lower than XNOR Type, 46.8% lower than XOR Type, 95% lower than NAND Type, and 94.7% lower than NOR Type.

All the Cam block types discussed in this block are 1-bit each and based on 6T cell, which are re-simulated for comparison and understanding using the LT- SPICE. Delay in nanoseconds for various 1 bit CAM cells with voltages ranging from 0.7 V to 1.2 V, including NOR, NAND, XOR, and XNOR. A cell should have less delay so that it can perform more quickly. Table 5.2, displays the delay in nanoseconds for several 3-bit Content Addressable Memory cells such as NOR, NAND, and XOR at 1.2 V. Except for NOR Type, all CAM cells have a lower delay (below 10 ns) [164].

5.3 PROPOSED TCAM CELL USING 8T SRAM BIT CELL

In this section, a novel 8T SRAM cell is designed using 32 nm technology at 1.0 V supply; this cell is used to configure a TCAM block. TCAM was made up of don't care (X), logic 0, and logic 1. The incomplete matching is represented by state X. The NOR-type TCAM basic circuit is depicted in Figure 5.1. It has two SRAM cells (static random-access memory) to store the data. Transistors M1–M4 comprises the circuit used for the search operation. The match line (ML) is high when the stored data and the search data are the same. Otherwise, it would be connected to the earth. To execute the WRITE operation, WL needs to be set at high and the data to be written should be positioned for bit lines BL ‘1’ and BL ‘2’ [165]. The access transistors are in the ON state since WL is high. The internal nodes of the access transistors and the bit lines have the same logic levels.

5.3.1 Basic Construction of a CAM Block

The cross-linked inverter receives data from BL ‘1’ and BL ‘2’ and appropriately maintains the logic levels. Assume, for example, that BL ‘1’ = 1 and BL ‘2’ = 0 are present in the bit-line data in the TCAM cell. The logic levels of the internal nodes are Data ‘1’ = 1 and Data ‘2’ = 0. We must now set WL = 1 and make BL ‘1’ = 0 and BL ‘2’ = 1 if we wish to make Data ‘1’ = 0. Consequently, Data ‘1’ = 0 and Data ‘2’ = 1 are the internal nodes. Consequently, a TCAM cell carries out the WRITE function. To ensure that ML = 1 and SL ‘1’ = SL ‘2’ = 0, set the search lines to low logic and use pre-charged VDD ML for the

SEARCH operation. You can find the information you need in SL. The ML stays high in logic, or ML = 1, if the data to be searched matches the data stored. Machine learning is reduced to low logic, or ML = 0, if the data to be searched is incompatible with the data that has been stored. To perform word search operations, the TCAM array is utilized. Figure 5.3 shows a schematic illustration of the search process. The packet forwarding process to one of the ports of a standard router is depicted in this figure. The packet is sent to one of the ports if the search result matches with the pre stored data.

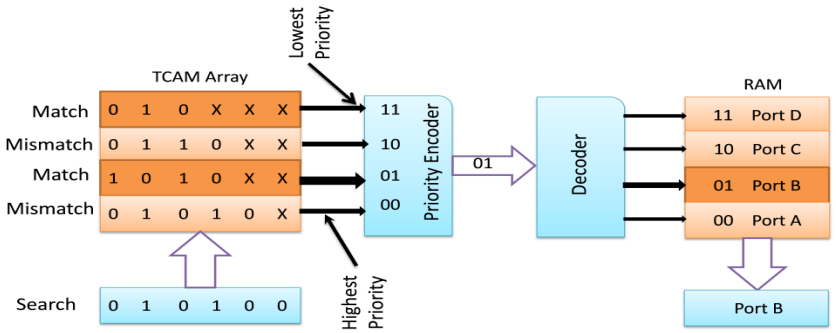


Fig. 5.3 Representation of search operation in TCAM.

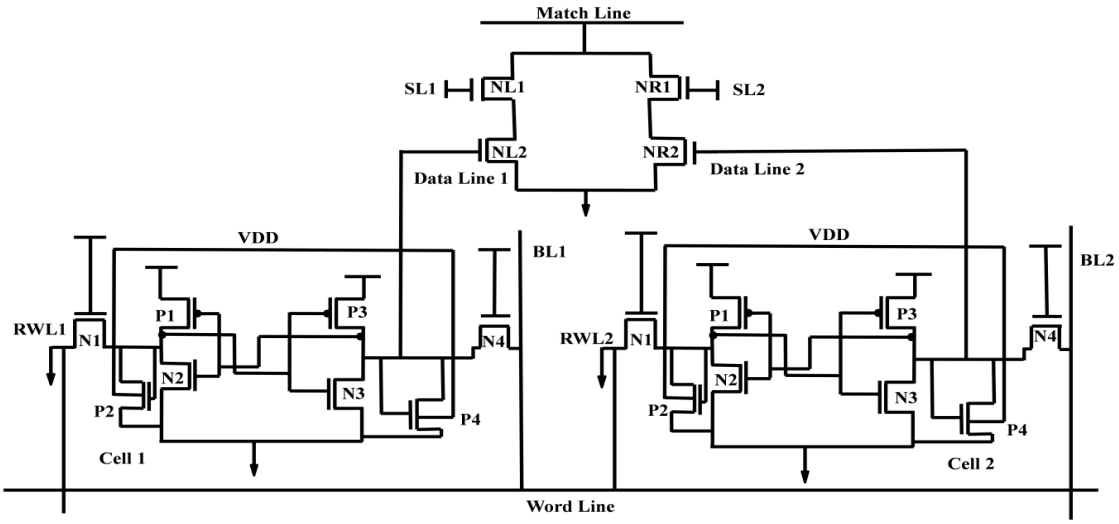
According to the router's schematic design, which is displayed in figure 5.3, the incoming packet will be transmitted via port B [145]. By cutting down on operating time and power, parameter extractors are utilised in CAM cells to do pre-computation [78]. The pre-computation technique avoids searching the entire memory, which wastes resources and increases latency, by extracting a specific feature from the incoming data and comparing it with stored data that already has the same feature. Among the techniques that can be applied are bit counting (counting the number of 1s), block XOR, gate block selection, parity bit extractor, and reminder function parameter extractor [146].

5.3.2 TCAM Block Design using Proposed 8T Cell:

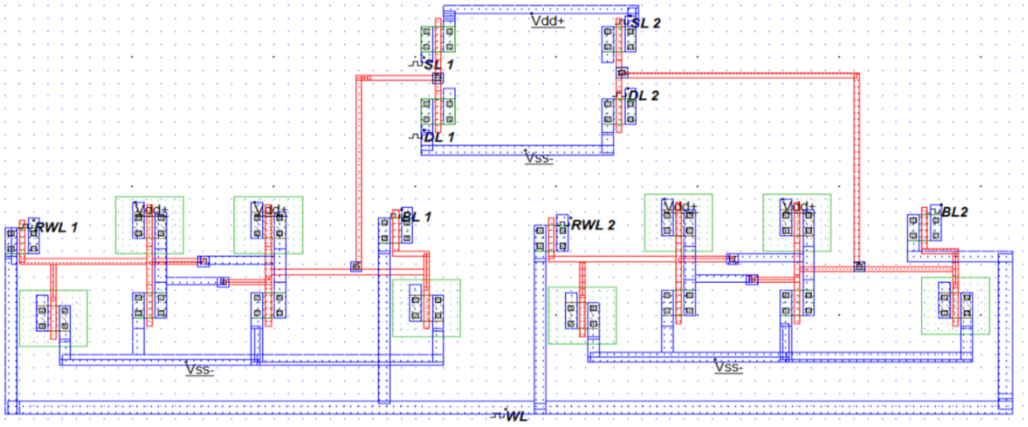
The 8TP SRAM (proposed in chapter 4) cell is constructed to facilitate single line structure of bit cell, this cell has a single bit line to initiate both read and write function of the bit cell. The cell structure is constituted by; a set of inverters (Inv. I and Inv. II) that are forming a cross coupled inverter with the help of four transistors where two are p-MOS transistors and other two are n-MOS transistors [147]. A few input signals are controlling all the operations of the cell such as; Read Word line (RWL), Read Bit line (RBL), Write Word line (WWL), Write Bit line (WBL) and Bit line (BL).

The 8TP SRAM bit cell is working at an ultra-low operating voltage of 500mV and for CMOS technology of 32nm [148]. Figure 5.4 (a) & (b), is representing the schematic and

layout of the proposed TCAM cell block using the 8T cell, respectively [69]. The accessing of cell is controlled by access transistors N1 and N5. For isolated read operation and write operations, cell has a combination of p-MOS and n-MOS transistors. The low power is attained by introducing power gated transistors (a combination of p-MOS (P3) and n-MOS (N4) transistors) in the design that are directly connected the word line, WBL. This 8TP SRAM cell offers better stability for all the operation.

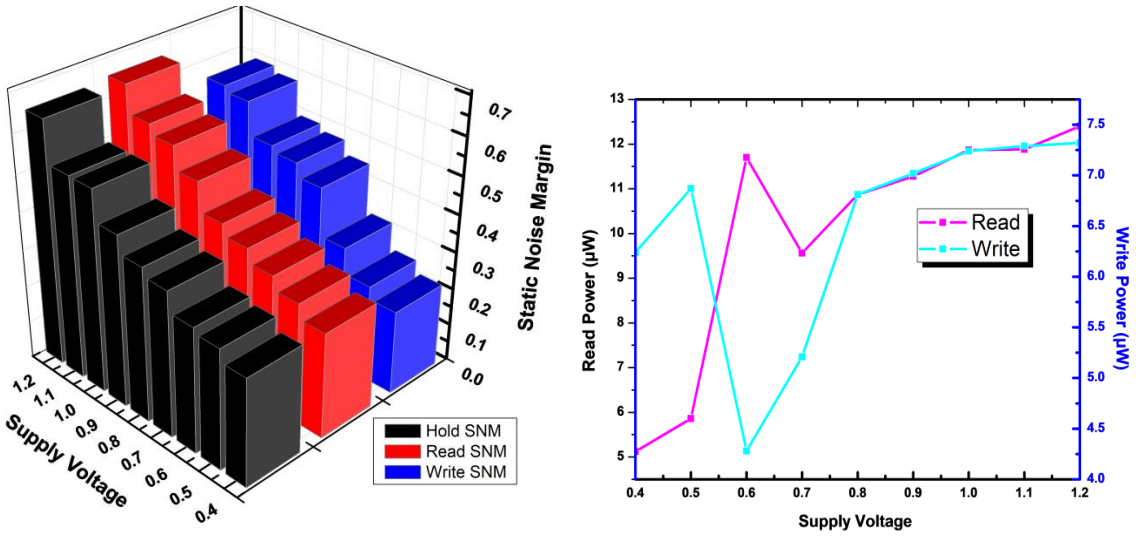


(a)



(b)

Fig. 5.4 (a) Schematic diagram, and (b) Area Layout for TCAM block using Proposed Single-Ended 8T SRAM TCAM block circuitry.



(a) (b)

Fig. 5.5 (a) Static noise margin, and (b) Read/write Power consumption using Proposed Single-Ended 8T SRAM based TCAM block circuitry.

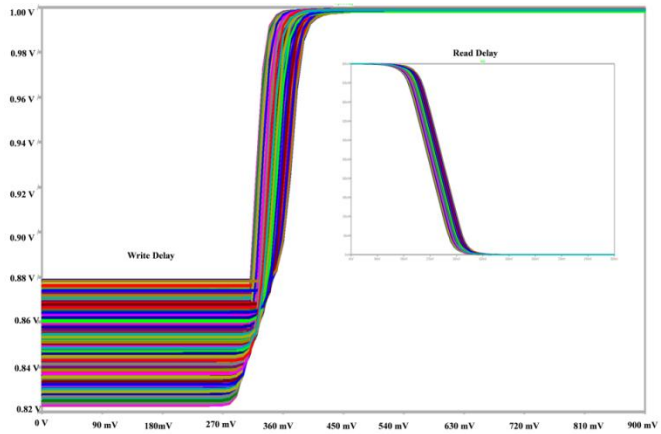


Fig. 5.6. Monte Carlo simulations for the TCAM block circuitry using Proposed Single-Ended 8T SRAM.

The major part of a SoC is associated with total power being consumed within the system [149]. The fundamental 6T SRAM cell and a separate comparison circuit make up a NOR CAM cell. Ten MOSFETs are used in a NOR CAM cell, with two NMOS serving as access transistors (N3, N4). The four NMOS transistors N5, N6, N7, and N8 comprise the comparison circuit [150]. Every cell in the comparison circuit has a parallel discharge path. The inverters with cross coupling consist of the remaining 4 transistors, P1, P2, N1, and N2 [151]. One NMOS and one PMOS (P1, N1, and P2, N2) connected crosswise make up an inverter. Inverters comprise the storage unit for CAM cell. The NOR CAM cell's pre-charge circuit is displayed [152]. The outputs are Q, QB, and ML, and the inputs are BL, BLB, WL, SL, and SLB.

Figure 5.4 shows an additional PMOS transistor with its source terminal connected to VDD and its gate connected to the control input CTRL [153]. The effect of voltage scaling on the noise margins and processing powers of the proposed 8T cell is shown in figure 5.5 (a) and (b), respectively. The impact of delay on the suggested 8T cell using Monte Carlo simulations with a 5000 sample size is seen in figure 5.6. The pre-charge circuit consists of a drain linked to Match Line. A pre-charging circuit is required in order to pre-charge ML [154]. A match condition is formed when the stored data and the search data match; a mismatch condition is created when they don't. When WL is enabled during a write operation, data is transferred for BL and its complement for BLB. The data is subsequently stored in the CAM cell [155].

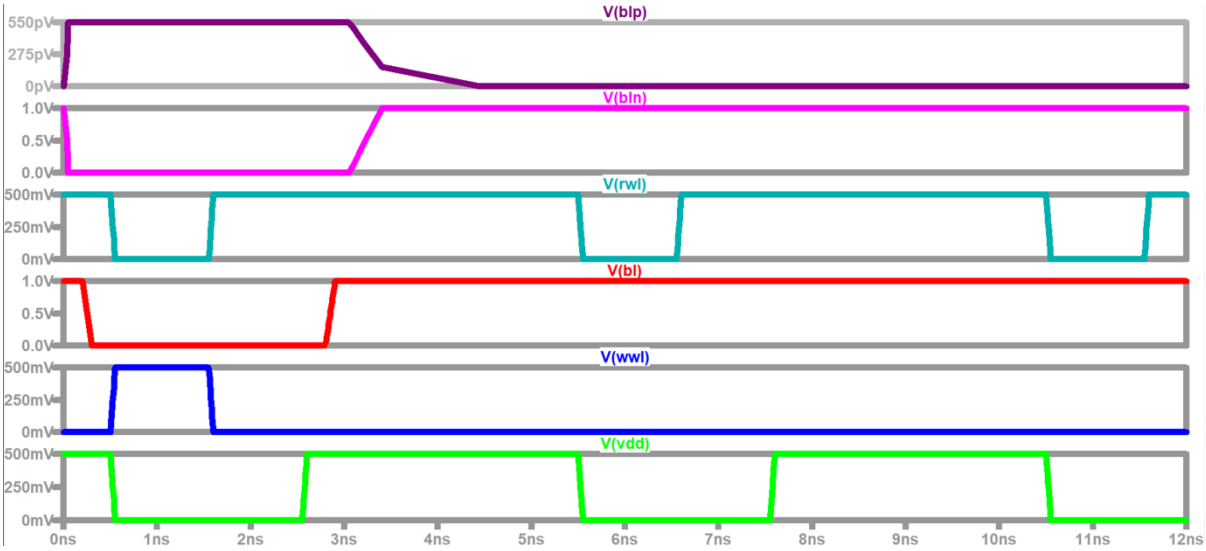
The data in CAM is compared to the search input data from SL and SLB throughout the comparison procedure [156]. The comparison process produces two output states. The overall parameter variations and performance of the proposed 8T cell is given in Table 5.3. To VDD, ML is already charged. During a state of match ML stays at VDD, while in the mismatch state, ML is released to GND. WL is turned off when performing comparisons [48].

TABLE 5.3. Performance parameters of proposed 8T SRAM cell and comparison with different cells.

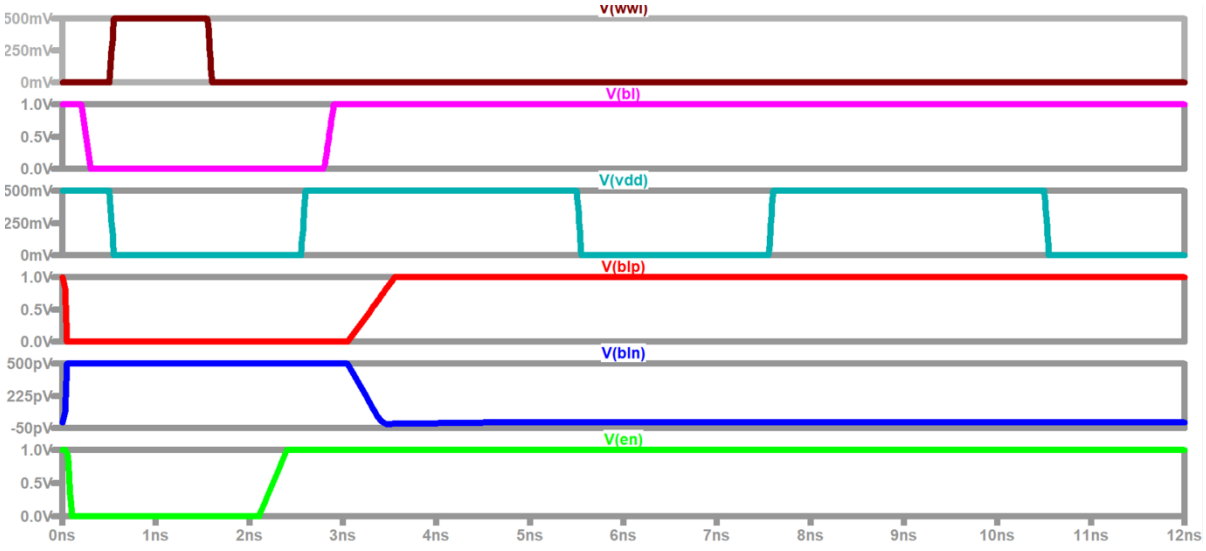
SRAM	Hold SNM (in mV)	Write SNM (in mV)	Read SNM (in mV)	Read power consumption (µW)	Write power consumption (µW)
Proposed 8T	438	454	421	08	4.2
11T [11]	516	565	518	12.1	18.6
7T [156]	356	388	356	7.89	4.8
9T [47]	448	490	447	9.61	5.2
10T [49]	502	560	503	10.12	13.8

5.3.3 Matching and Mismatching

Two different types of SRAM cells are used in the same circuitry to form a desired CAM block and start binary searching operation. Each CAM block consists of two cells and a set of select lines (SL ‘1’ and SL ‘2’) with a set of data lines (DL ‘1’ and DL ‘2’). For searching operation CAM is used in two operations matching or mismatching of the searched cells. Depending on the search data, many word lines may be asserted at once in a CAM search process. By lowering the wordline voltage to Vdd_Lo, we employ an assist strategy to prevent bit-flips during this search [101]. Figure 5.7 represents the CAM block using the 8T SRAM cell. SL ‘1’ and SL ‘2’ represents select line 1 and select line 2 while the DL ‘1’ and DL ‘2’ represents data line 1 and data line 2.

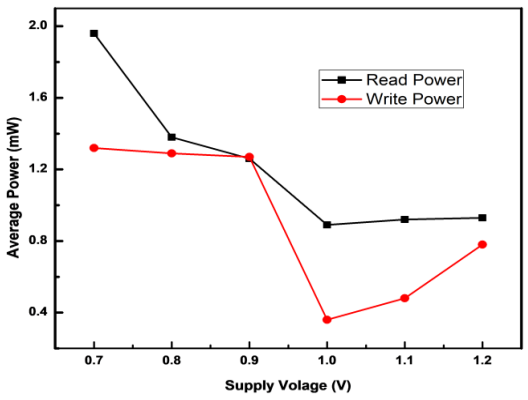


(a)

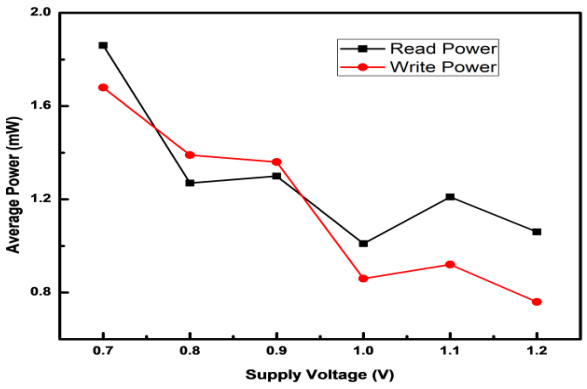


(b)

Fig. 5.7 (a) Proposed 8T SRAM-CAM Block for matching, and (b) Proposed 8T SRAM-CAM Block for mis-match.



(a)



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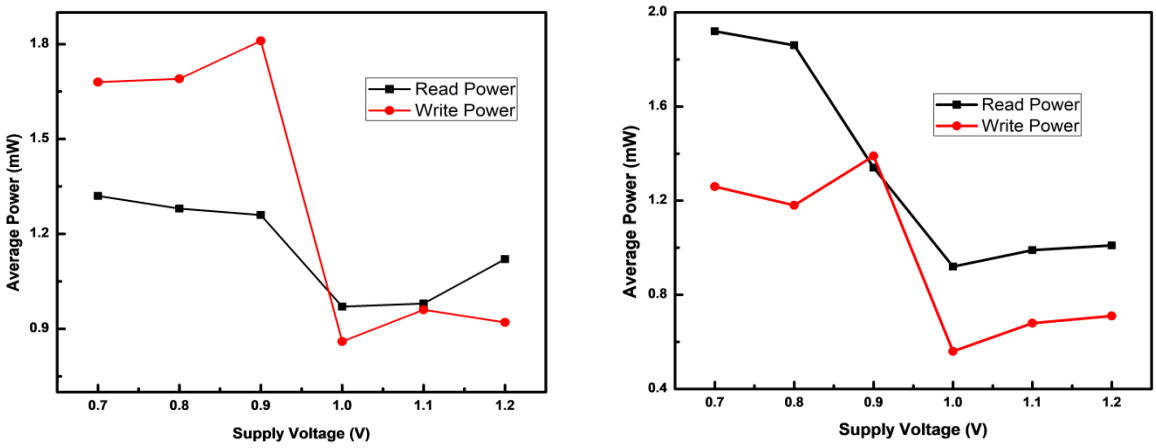


(c) (d)

Fig. 5.8 Average Power (mW) of (a) NAND, (b) NOR, (c) XOR, and (d) XNOR type TCAM block using proposed 8T cell.

While XNOR gates are used to find perfect matches or wildcard conditions, XOR gates are us ed to discover mismatches, or differences between the input and stored values. The 8T SRAM-based TCAM cell can handle ternary data fast and precisely by utilizing the capabilities of these gates, which also offer wildcard searches and facilitate effective pattern matching [157]. Applications like as network packet forwarding, database searching, and AI-based data retrieval depend on high-speed matching, which is made possible by this architecture, which also greatly increases power efficiency and minimizes static noise margin problems, represented in figure 5.8.

While the XOR and XNOR gates allow for the comparison of binary inputs with ternary state s, the NAND and NOR gates are utilised for fundamental binary operations, regulating the sel ection of valid binary matches in theTCAM.To effectively execute ternary comparisons (0, 1, and "X"; where X is a wildcard), a ternary content-addressable memory (TCAM) cell made by integrating 8T SRAM cell in the architecture and also employing logic gates like; NAND, NOR, XOR and XNOR [158]. Average power values for various variations of a CAM block using 8T cell is represented in figure 5.8.

5.3.4 Search Delay

An 8T SRAM-based ternary content-addressable memory (TCAM) cell's internal logic gates (NAND, NOR, XOR, and XNOR) control ternary state comparisons and impact its power consumption and search delay. By segregating the store and access transistors, the 8T SRAM configuration improves read and write stability while lowering overall dynamic power and leakage currents during active operations. Effective ternary matching is made possible by

comparison circuits that include XOR and XNOR gates, which reduce needless switching and power consumption during wildcard searches [159].

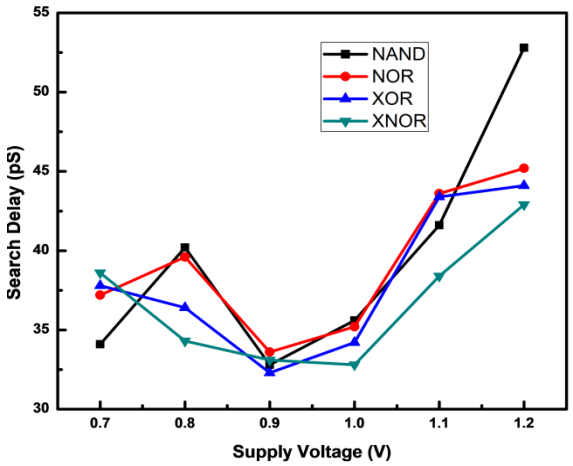


Fig. 5.9 Comparison of Search Delay (pS) for different logics using TCAM cells.

However, the intricacy of the ternary comparison procedure largely controls the search delay. Compared to traditional binary CAMs, the comparison time is longer for XOR and XNOR gates since they assess both binary and ternary inputs [160]. Nevertheless, by addressing problems like read-disturb and enhancing the stability of the cross-coupled inverters, the optimized design of the 8T SRAM cell lowers the overall delay when compared to conventional TCAM cells [161]. The 8T SRAM-based TCAM design typically achieves a balance between power efficiency and moderate search latency, making it appropriate for high-speed, low-power applications in networking and data retrieval systems.

The values of search delay for various configurations of the CAM blocks using 8T cell can be seen in figure 5.9. However, the search delay is further influenced by variables like the size of the TCAM array and the number of wildcard entries. Here, the CAM block is created using an 8T SRAM cell and it is simulated for various arrangements of the CAM block such as; NAND, NOR and XOR type CAM. The major comparison is sketched out for the values of average power utilized during the read and writes operation within the cell in the CAM block and between the times consumed during the searching operation of the CAM block [162].

5.4 TCAM BLOCK OPERATIONS AND COMPARISON WITH OTHER SRAM BASED TCAM BLOCKS

The suggested CAM cells are 3-bit Modified Hybrid Self-Controlled Pre-charge free CAM and 1-bit Modified Pre-charge free CAM. The MPF-CAM cell reduces the critical path delay and generates a full swing output voltage. Power is conserved by minimizing leakage current.

ML is fully discharged during mismatch, saving power. When pre-charge circuits are removed, CAM becomes more effective while conducting a search. Three separate CAM cells are joined to generate a word in the MHSCPF CAM cell, which also shares a common comparison circuit with three transistors. Because individual CAMs have their own comparison circuit with two transistors apiece, the MHSCPF CAM has fewer transistors. This greatly lowers both the power and the delay. The performance of CAM can be enhanced by pre-computation. CAM cells, encoders, decoders, sense amplifiers, and pre-charge circuits can all be used to create array structures [163].

5.4.1 WRITE Command

Set WL to high and place the data to be written on bit lines BL '1' and BL '2' to execute the WRITE operation. Access transistors are triggered because WL is high. The logic levels of the bit lines and the internal nodes of the access transistors are identical. The cross-linked inverter receives the data from BL '1' and BL '2' as inputs and appropriately maintains the logic levels [18]. Suppose that bit-line data, such as BL '1' = 1 and BL '2' = 0, is present in the TCAM cell. The internal node's logic levels are Data '1' = 1 and Data '2' = 0. To make Data '1' = 0, we must now set WL = 1 and set BL '1' and BL '2' to 0 and 1, respectively [19]. Consequently, Data '1' = 0 and Data '2' = 1 will be present in the internal nodes. Thus, the WRITE operation is performed by a TCAM cell [20]. Don't care (X) and logic 0 and 1 make up TCAM [20]. The incomplete matching is represented by state X. Two SRAM cells (static random-access memory) are used to store its data [164]. Transistors M1 through M4 make up the circuit used for the search. The match line (ML) is high when there is an exact match between the stored data and the search data. Otherwise, it would be fastened to the ground. The logic levels' voltage levels are displayed [117].

Table 5.4. Performance comparison of proposed 8T based-TCAM with other SRAM based TCAM blocks.

S. No	TCAM cell	Avg. power and search delay of the proposed ternary CAM cells	
		Average power (mW)	Search delay (pS)
1.	8T SRAM-based TCAM cell (Proposed)	0.89	34.78
2.	11T SRAM-based TCAM cell [11]	1.26	69.35
3.	10T SRAM based TCAM cell [156]	1.4290	56.78
4.	9T SRAM based TCAM cell [47]	1.56	42.98
5.	7T SRAM based TCAM cell [49]	1.01	33.96

The write operation in an 8T SRAM-based TCAM block is used to write the desired search data to the SRAM storage nodes of the TCAM cell. The write operation is started by activating the word line (WL) and applying complementary data to the bit lines BL and BLB. During the operation, the access transistors become active and allow the internal cross-coupled inverter pair to change its stored state according to the input data applied. For writing logic '1', BL is maintained at high voltage and BLB is maintained at low voltage. For writing logic '0', voltage levels are reversed [165].

The 8T cell has extra transistors which provide for better isolation between the read and write paths, thus reducing disturbance while accessing the memory. During match operations, the data stored in a TCAM block is compared to incoming search data. Therefore, reliable write operation is necessary to guarantee correct ternary information storage and accurate search performance. The 8T SRAM based TCAM block has improved write stability and lower power dissipation than a conventional 6T SRAM based TCAM structure due to its improved cell isolation and reduced read interference characteristics. A number of important parameters, including matching, mismatching, search delay, and power (both read and write), [21] must be taken into account when comparing the 8T TCAM cell to its modern 7T, 9T, 10T, and 11T equivalents that can be seen in Tables 5.4 and 5.5.

5.4.2 Power Consumption

The power consumption characteristics of the proposed 8T SRAM-based TCAM cell provide a good trade-off between the stability of operation and power efficiency. The proposed design has reduced power dissipation during the matching and mismatching operations due to the improved isolation between the read and storage nodes and the optimized ternary comparison circuit. The proposed 8T TCAM cell performs the comparison operation based on the XOR/XNOR based matching logic. The XOR/XNOR based matching logic is able to reduce the unnecessary switching activity on the match line and thus reduce the dynamic power consumption.

The proposed 8T TCAM cell consumes an amount of power of about 456 µW in the matching condition, i.e. when the search data is exactly equal to the stored data. The reduced matching power is mainly achieved by the fact that there is almost no discharge activity on the match line, which reduces the dynamic switching losses. Furthermore, the 8T SRAM structure has an isolated read path to prevent disturbance in the internal storage nodes during search operations, thereby improving stability and controlling leakage power.

The power consumption of the proposed 8T TCAM cell is observed 481 µW under mismatching conditions. Although the mismatch operation has a discharge activity on the match line, the power dissipation is still less than several previously reported SRAM-based TCAM structures. The mismatch power increase from the matching condition is due to the additional current flow due to match line evaluation during search operations. But the optimized transistor layout efficiently limits the excessive switching transition and the short circuit current.

Table 5.5. Power of proposed 8T SRAM cell based CAM and its comparison with other blocks

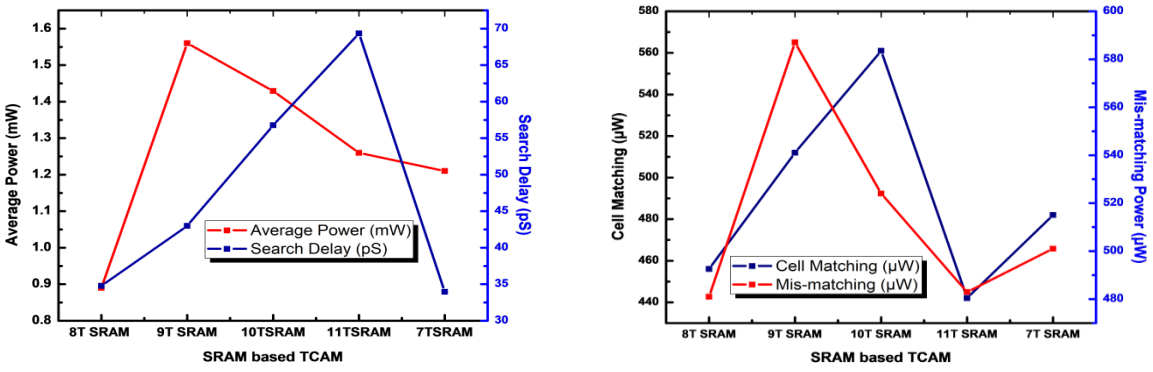
TCAM cell	Power of ternary CAM	
	Cell Matching (µW)	Mis-matching (µW)
8T SRAM-based TCAM cell (Proposed)	456	481
11T SRAM-based TCAM cell [11]	512	587
10T SRAM based TCAM cell [156]	561	524
9T SRAM based TCAM cell [47]	442	483
7T SRAM based TCAM cell [49]	482	501

Table 5.5 shows the comparative power analysis of proposed 8T SRAM based TCAM cell with earlier reported 7T, 9T, 10T and 11T SRAM based TCAM architectures. The proposed design has better mismatch power performance than 7T, 10T and 11T TCAM cells but with lower matching power. Although the 9T TCAM cell has a slightly lower matching power, the proposed 8T structure offers a better trade-off among transistor count, area efficiency, operational stability and overall power dissipation. Moreover, the proposed 8T architecture has better read isolation and is less prone to read disturbances than the 7T TCAM cell, thus enabling a more reliable low-power operation. Hence, the power consumption features of the proposed 8T SRAM based TCAM cell are very efficient and it can be utilized in low power and high-performance memory applications especially for portable and energy-limited systems with reliable ternary search operations [124].

5.4.3 Matching and Mismatching Power

The proposed 8T SRAM based TCAM cell offers a good tradeoff between matching/mismatching power, search delay and stability of operation. The comparison circuitry based on XOR/XNOR, which is designed to be efficient in the matching condition, reduces the unnecessary switching activity on the match line, thus reducing the dynamic power dissipation. Likewise, although the match line has discharge activity in mismatching operations, the overall power consumption is controlled because of the enhanced isolation between the storage nodes and the search circuitry. Therefore, the proposed 8T TCAM

structure can provide reliable search performance with moderate power consumption and stable operation.



(a) (b)

Fig. 5.10 Comparison of various TCAM cell for (a) average power/delay, and (b) matching/mis-match power**.**

Typically, the 7T SRAM-based TCAM cell consumes less power due to its lower transistor count and small area. However, the reduced isolation between storage and access paths results in a degradation of the stability and an increase of the cell susceptibility to read disturb and process variations during high speed search operations. In contrast, the 9T, 10T and 11T SRAM based TCAM cells offer better read stability, noise immunity and robustness in matching and mismatching conditions thanks to the additional transistors and isolated read/write paths.

However, these benefits come at the cost of increased silicon area, larger search delay, and greater power dissipation. Therefore, the suggested 8T SRAM based TCAM cell demonstrates a good compromise between low power consumption and reliable searching operation. It provides lower matching and mismatching power than several TCAM architectures with a higher number of transistors while providing better stability and robustness than lower-number-of-transistor-based designs, such as the 7T TCAM cell. Comparison of matching and mismatching power characteristics of different SRAM based TCAM cells are shown in Figures 5.10 (a) and (b), respectively.

5.5 HIGHLIGHTS OF IMPORTANT RESULTS

The proposed 8T SRAM-based TCAM cell shows an efficient trade-off between low power consumption, search performance and operational stability. The design uses an optimized ternary comparison based on XOR/XNOR logic for accurate matching and mismatching operations with reduced switching activity on the match line. The extra transistors of the 8T architecture allow better isolation between the storage and access paths, thus improving the

read stability, and reducing disturbance during search operations. Hence, the proposed TCAM cell has stable and reliable performance for low power memory applications.

The proposed architecture is proved to be effective by comparing with previous reports of 7T, 9T, 10T and 11T SRAM based TCAM cells. The power consumption for the matching and mismatching of the proposed 8T TCAM cell is 456 µW and 481 µW, respectively, which are lower than many existing TCAM structures. The search delay characteristics are also acceptable. The 7T TCAM cell has advantages of less transistor count and lower power consumption, but it has disadvantages of poor stability and weak read isolation. The 9T, 10T, and 11T TCAM cells, however, have better robustness and noise immunity at the cost of increased area overhead, higher delay, and larger power dissipation.

Thus, the proposed 8T SRAM-based TCAM cell gives a good compromise between area efficiency, power dissipation and search reliability. The obtained results show a good suitability of the proposed design for low-power and high performance TCAM applications in modern portable and energy efficient computing systems. Future work may include further optimization under process variations, techniques to reduce leakage power, and analysis at advanced technology nodes to improve scalability and performance.

CHAPTER-6
TCAM ARRAY USING SINGLE PORT, DUAL PORT AND ALTERNATE SRAM CELLS

6.1 INTRODUCTION

The rapid development of data-intensive computing platforms, high-speed communication networks, artificial intelligence hardware, and modern digital systems has led to an increasing demand for memory architectures that are capable of performing fast search and comparison operations with very low latency. Traditional memory systems like static random access memory (SRAM) and dynamic random access memory (DRAM) are mostly designed for address-based data retrieval, where data is only retrieved when the memory address is specified. This approach works for general purpose computing but is inefficient for applications where direct identification of stored data based on its content is required. Many new workloads such as packet processing, network routing, pattern recognition, database acceleration, cache tag verification, image analysis, etc. require search capabilities that can match input data against many stored entries in parallel. In order to meet these requirements, Content Addressable Memory (CAM) and its improved version, Ternary Content Addressable Memory (TCAM) has emerged as attractive hardware solutions for high-speed associative search operations.

TCAM is a special kind of memory that compares the search key with all entries in the memory array in parallel instead of fetching data from a particular address as with traditional memories. This massively parallel operation allows the search results to be generated in a single clock cycle. TCAM is one of the fastest hardware implementations for lookup operations. BCAM (Binary CAM) supports only two logic states, i.e., ‘0’ and ‘1’, whereas TCAM adds one more wildcard state, which is denoted by ‘X’ or “don’t care.” This extra state enables selective bit masking and flexible pattern matching, dramatically increasing search efficiency for complex lookup tasks. Therefore, TCAM has a key role in networking and communication equipment, where it is widely used for longest-prefix matching, packet classification, routing table lookup, packet forwarding and access control mechanisms. However, TCAM architectures suffer from many design challenges such as high dynamic power consumption, high leakage currents, large silicon area overhead and scalability issues with the increase in memory density. These limitations derive mainly from the parallel search

operation, the match-line evaluation circuitry, and the embedded memory cells used for storing data.

The storage function in most TCAM architectures is normally carried out using SRAM cells and thus the performance of SRAMs is a critical factor in determining the overall efficiency of TCAMs. The SRAM cell parameters such as stability, power consumption, access speed and reliability directly affect the search accuracy and operational robustness of the whole memory array. The conventional 6T SRAM cell has a compact layout and high storage density, but its performance is degraded under low-voltage operation due to limited static noise margin and sensitivity to read disturbance. As technology scales down to deep submicron dimensions, these shortcomings become more and more significant.

To solve these problems, many advanced SRAM structures have been proposed, among which the 8T and 9T SRAM cells have attracted a lot of attention. These architectures use dedicated read and write paths which decouple the storage nodes from the bit-line activity during read operations. Such structural modifications are effective in reducing read disturbance, improving data retention capability, increasing immunity to process, voltage, and temperature variations, and enhancing overall cell stability. Therefore, the advanced 8T and 9T SRAM cells are a promising platform for low-power, high-performance and reliable TCAM implementations in future computing and networking systems.

Based on the memory access and search operation, SRAM based TCAM architectures can be broadly classified into single-port and dual-port architectures. The single-port SRAM based TCAM cells are typically designed with a dedicated search or read path and share a common access mechanism for data storage functions. Due to the simpler structure these cells have generally lower power dissipation and better energy efficiency than conventional TCAM implementations. In addition, decoupling the search path from the storage nodes helps to alleviate read disturbance effects, which improves cell stability during search operations. Thus, single-port designs are frequently preferred for applications where the main design objective is to minimize power consumption.

Dual-port SRAM-based TCAM cells, on the other hand, have independent read and write ports, enabling simultaneous memory access functions. The parallel accessibility increases the overall throughput and decreases the operation latency, thus making the dual-port structures suitable for high-performance search applications. A dedicated read circuit isolates the internal storage nodes from bit-line activity and greatly reduces the probability of data

corruption during read operations. Hence, these architectures can offer better static noise margin and higher reliability for operation, in particular under technology scaling and process-voltage-temperature variations. The additional circuitry needed to provide dual port functionality however increases the transistor count, layout complexity and silicon area utilization. These factors can lead to higher leakage currents, higher fabrication costs and higher design overhead compared to single-port memories.

The performance-energy efficiency tradeoff has been increasingly addressed by the research community by exploring hybrid TCAM architectures that integrate different SRAM cell topologies within the same memory array. In a hybrid configuration, normally single-port and dual-port SRAM-based TCAM cells are interleaved across the array. In such a configuration the architecture can take advantage of the low power of single-port cells while at the same time benefiting from the better stability and read robustness of dual-port architectures. Hybrid TCAM arrays can offer lower average power consumption, enhanced search accuracy, better noise immunity and higher resistance to temperature-dependent performance degradation by leveraging the complementary benefits of both cell types. Thus, these architectures are an effective way to obtain an optimal compromise among power efficiency, operating speed, reliability, and area utilization.

To evaluate advanced TCAM arrays thoroughly, a number of important performance metrics need to be studied. Search delay is an important parameter as it determines the time needed for match-line evaluation and hence lookup speed. Likewise, read and write delays affect the efficiency of memory access operations and the overall responsiveness of the system. Power consumption is one of the most important considerations, since energy amplification of a large number of search lines and match lines in parallel can cause large dynamic energy consumption. Besides these factors, leakage current has to be carefully monitored to ensure energy efficient standby operation. Some of the metrics related to reliability, such as static noise margin, bit error rate and data retention voltage, are equally important as they dictate the ability of the memory cell to preserve the information stored correctly under process variations and adverse operating conditions.

In view of these considerations, this chapter proposes hybrid TCAM array architecture with a unified framework that combines single-port and dual-port SRAM-based cell configurations. The approach we propose aims to leverage the benefits of each cell type without modifying the underlying bit-cell structures. The proposed array combines the two architectures in a strategic way such that an overall reduced power consumption at the operating supply voltage

is achieved, while still maintaining a high search reliability and performance. Moreover, the design leverages existing cell topologies, avoiding the complexity of a complete bit-cell redesign, thus simplifying integration and enhancing the practical feasibility of future low-power TCAM systems. The following objective is framed here to obtain a higher order TCAM array:

"To configure higher order array for Binary-CAM/Ternary-CAM/SRAM."

To attain this objective, three different TCAM arrays using 8T, 9T and hybrid alternate 8T-9T SRAM cells are designed. The proposed hybrid array architecture is realized by judiciously allocating single-port SRAM-based TCAM cells to the lower order positions of the array and dual-port SRAM-based TCAM cells in the higher order positions. However, this approach does not require changes to the core bit-cell structures, but adds extra considerations during the physical design and layout realization. The presence of two distinct cell topologies in the same memory array necessitates careful floor planning, routing, and cell placement to ensure correct alignment and signal integrity across the whole architecture. Also, the non-uniform characteristics of the array may require a custom fabrication flow; a dedicated mask set or process specific design modifications, which may lead to higher manufacturing complexity and implementation cost, compared to traditional uniform TCAM arrays.

In this chapter, a detailed investigation of TCAM architectures based on single-port SRAM cells, dual-port SRAM cells and the proposed hybrid SRAM based scheme is presented. The work includes the design of single TCAM cells at the transistor level, the organization of the array level, the methodology of search operation, the functional principles and the parameters that affect the performance of the memory. It is extensively evaluated with key design metrics such as search delay, read & write times, power dissipation, leakage, static noise margin, data retention and overall reliability.

This chapter is divided into five sections; the motivation, background and the objectives of the chapter are illustrated in detail in section 6.1 of this chapter. Whereas, the review of different organizations of SRAM-based TCAM arrays and their design features is explained in section 6.2. The proposed hybrid TCAM architectures and describes their structural configuration and operating principles are explained in detail in section 6.3. Followed by a detailed performance evaluation and comparative analysis of the array implementations studied, based on the simulation results are represented in section 6.4 of this chapter. Lastly, section 6.5 summarizes the main findings and conclusions.

6.2 ARRAY ARRANGEMENTS

An array organization is a memory architecture in which the memory cells are arranged in rows and columns, for efficient data storage and retrieval. The array structure in SRAM and TCAM based memories is composed of interconnected bit cells. The bit cells are controlled by word lines and bit lines to perform read, write and search operations. The arrangement of the arrays is important to the total power consumption, access speed, stability and area efficiency of the memory system. Different array configurations and partitioning techniques are often used to optimize the performance parameters and improve the reliability under different operating conditions.

6.2.1 Conventional Array Configuration

Traditionally, a j×k array of SRAM bit cells is created to provide an SRAM-based cache memory. Fig. 6.1 shows a generalized block diagram representation for an SRAM cache. Five distinct signals are shown in the array: Wordline (WL), Readline (RL), Bitline (BL), Bitline Bar (BLB), and Wordline Bar (W). A cell's mode of operation (hold, read, and write) is controlled by the WL, W, and RL signals. The RL and W signals are high during the read operation, whereas the WL signal is high and W is kept low during the write process. W is high while RL and WL signals are kept low throughout the hold operation. The purpose of using BL and BLB is to make reading and writing easier.

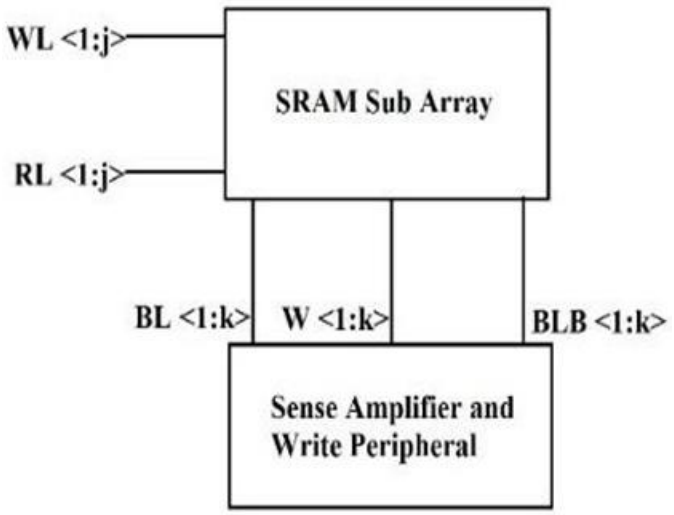


Fig. 6.1 Block diagram representation for an SRAM memory.

The data to be written into the cell is positioned on BL and BLB during the write procedure. In contrast, the BL and BLB are pre-charged during the read operation, and the read discharge

current passing through BL and BLB uses a sensing amplifier to determine the data stored in the cell.

6.2.2 Hybrid Array Configuration

In a conventional j × k memory array, each row is a word consisting of multiple memory cells. If the bits are stored in a word , the position of the bits makes them more or less important . The Most Significant Bits (MSB) are the higher order bits and the Least Significant Bits (LSB) are the lower order bits. Higher order bits require a greater degree of protection and reliability, as an error occurring in an MSB has a much larger impact on the represented data value than an error in an LSB. The Figures 6.2(a-b) show implementations of homogeneous arrays with 8T and 9T SRAM cells only, however Fig. 6.2(c) shows the array arrangement with alternate 8T and 9T cells.. Uniform architectures simplify array design but usually make trade-offs between area, power consumption and robustness of operation more difficult.

The ever increasing sophistication of semiconductor technology has increased the demand for memory architectures that can provide high performance with low energy consumption and silicon overhead. Hence, the modern SRAM cells have to meet strict requirements regarding speed, power efficiency and stability. However, the properties of an isolated memory cell provide limited information on its practical usefulness, as SRAM cells are rarely used in isolation in real systems. Instead, they are embedded in thousands or millions of cells into large memory arrays representing a large fraction of cache memories, embedded memories and System-on-Chip (SoC) platforms. Thus, the true performance and implementation efficiency of a memory design can be accurately evaluated using array level analysis.

At the same time, the role of SRAM has been expanded from the traditional data storage. Recent advances in in-memory computing have shown that memory arrays can perform logic and search operations within the storage fabric, which reduces data movement between memory and processing units. This approach avoids the well-known von Neumann bottleneck and leads to a significant improvement of the computational throughput and energy efficiency [33]. Thus, SRAM architectures studied in an array environment give a more realistic view on their behavior and applicability to the emerging paradigms of computing [63].

Considering these points, three different configurations of 4×4 SRAM array have been implemented and studied in this work. The first configuration uses only single-port 8T SRAM cells. The second uses dual-port 9T SRAM cells throughout the array. The third

configuration introduces a hybrid organization where 8T and 9T cells are arranged in alternate rows. The proposed hybrid architecture combining the compactness and low-power features of 8T cell with the improved stability and read isolation of 9T cell is targeted towards an improved trade-off between area efficiency, power dissipation and reliability.

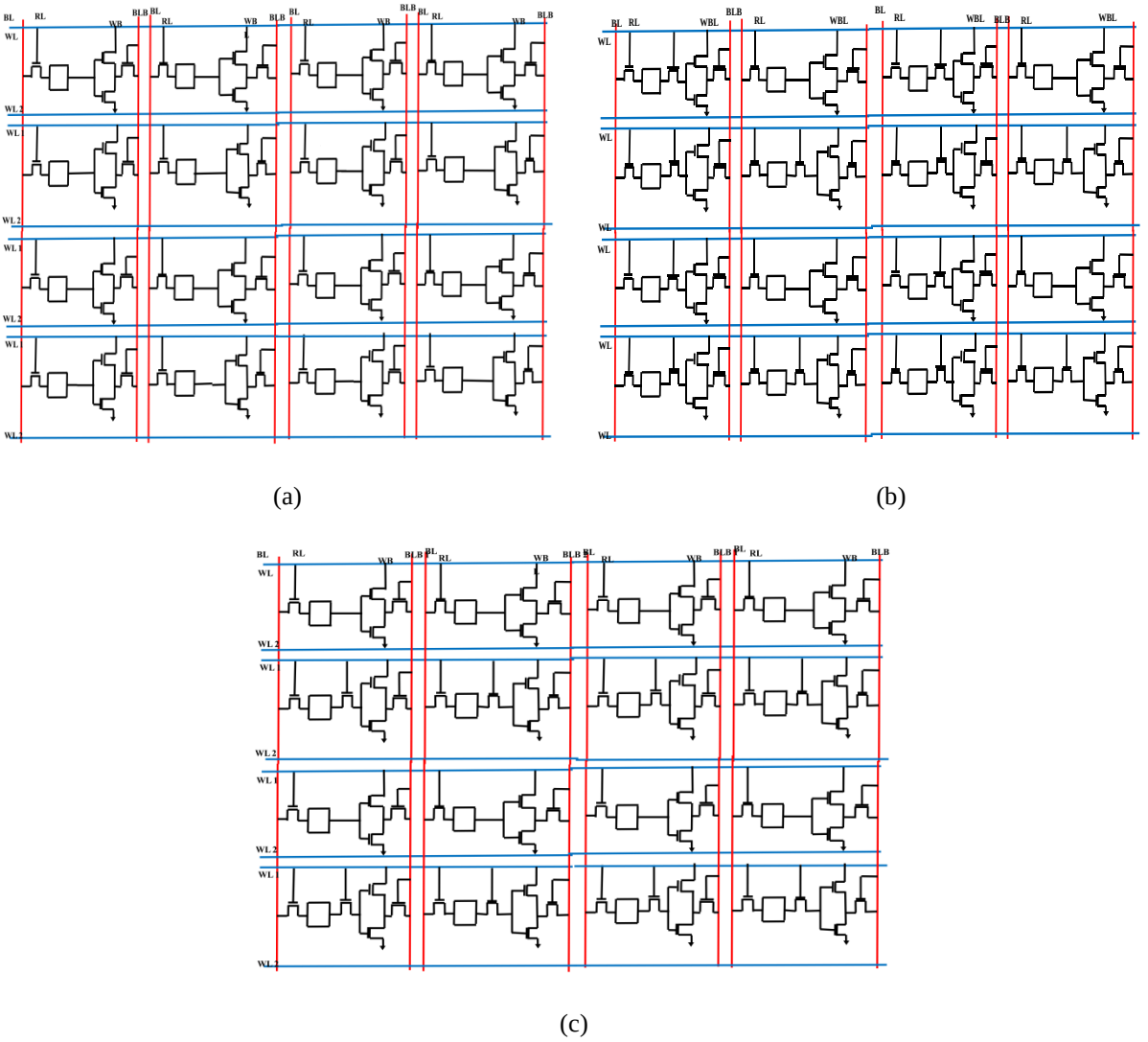


Fig. 6.2. A 4×4 array representation of proposed TCAM block based on (a) single port 8T, (b) dual port 9T, and (c) both alternate (8T-9T) SRAM cells.

In a ternary content-addressable memory (TCAM) block implemented using SRAM-based cells; data is stored in the configured bits and processed by evaluating the match-line against an input search for collision detection. The decoupling in the read path improves read stability in a TCAM implementing single-port 8T SRAM cell, which is critical for achieving a reliable match functionality where supply operation voltage cannot be low than 1 V. In a search operation, the input data will ride on the search lines while every storage bit would be compared using an XNOR-based logic (the mismatched stored bit(s) discharges its

corresponding match line to indicate failed matching). The studied array structures are illustrated in their physical layout in figure 6.2 and they form the basis of the performance analyses shown in the next sections.

However,s port structure, read/search and write operations cannot happen at the same time, w hich restricts performance and may cause half-select disruptions in large arrays. On the other hand, a TCAM based on a dual-port 9T SRAM cell provides enhanced capability by allowing simultaneous search and write operations using a dedicated read port in addition to the write channel. This design has increased size and a slight increase in power consumption, owing to the added transistor and control complexity, but does offer improved speed and resilience.

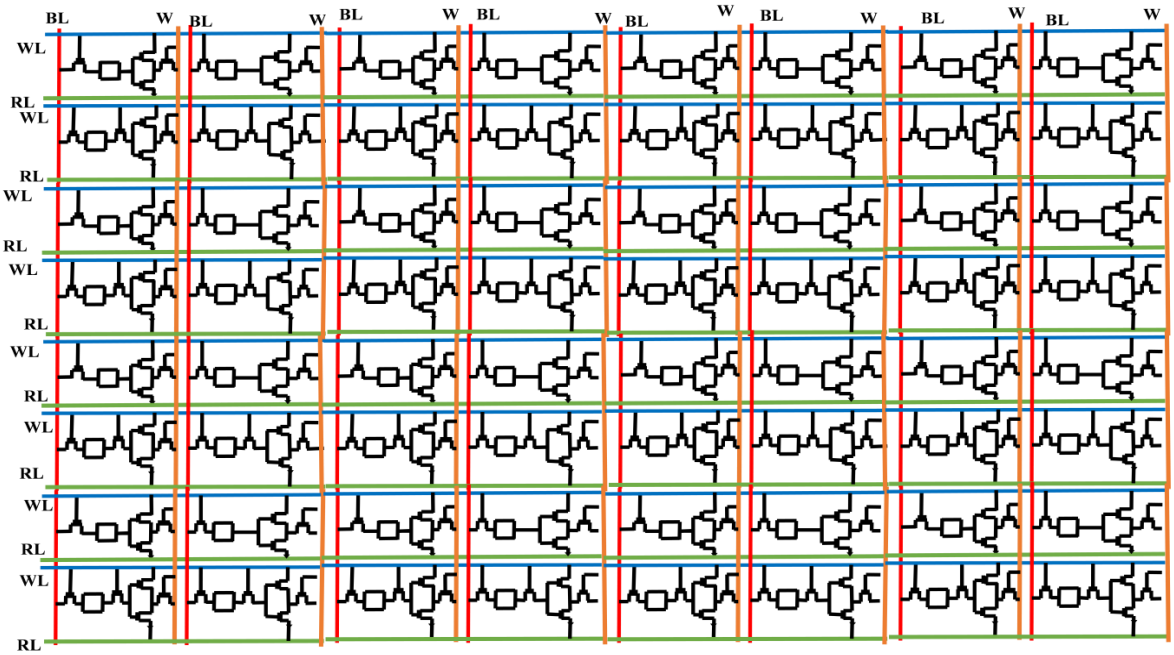


Fig. 6.3. An 8×8 array representation of hybrid TCAM block using single port and dual port SRAM cells.

Alternatively, TCAM architectures using alternate or hybrid SRAM cells combine different cell topologies, such as 8T and 9T cells, within the same array to optimize overall performance. As seen in figure 6.3. Robust cells are typically employed in critical paths to enhance stability and variation tolerance, while compact cells are used in non-critical regions to improve density and reduce power consumption. The search mechanism remains based on parallel comparison and match-line sensing, but the heterogeneous structure enables a balanced trade-off among power, delay, and area. Such designs are particularly suitable for advanced technology nodes like 32 nm, where low-voltage operation, leakage reduction, and temperature resilience are key requirements, making hybrid TCAM implementations highly efficient for modern high-performance and low-power applications.

6.3 PROPOSED 8T, 9T AND ALTERNATE HYBRID 8T-9T SRAM BASED TCAM ARRAYS

By cutting down on operating time and power, parameter extractors are utilised in CAM cells to do pre-computation [114]. The pre-computation technique avoids searching the entire memory, which wastes resources and increases latency, by extracting a specific feature from the incoming data and comparing it with stored data that already has the same feature. Among the techniques that can be applied are bit counting (counting the number of 1s), block XOR, gate block selection, parity bit extractor, and reminder function parameter extractor.

6.3.1 8T SRAM based TCAM Array:

A standard 6T storage core and two extra NMOS devices make up a comparison/evaluation network for each bit-cell. This network is connected to a single-ended bitline (BL) and a row-wise match line (RL) as shown in figure 6.2(a). During writing, WL opens the pass gates and the storage nodes Q/Q are pushed through BL with an uneven drive (writing "1" depends on the pull-up ratio). In search mode, RL is charged up to VDD and floats electrically while being evaluated. The search input is put on the column line (W/SL), which makes the gate of the comparison transistors less likely to open.

The discharge condition depends on the data. For instance, if Q=1 and search=0, a series NMOS stack that connects RL to GND turns ON, making a conditional pull-down path. To match, at least one transistor in the stack must stay OFF, which keeps RL at high impedance. The evaluation delay is controlled by $R_{pd}.\cdot C_{RL}$, where R_{pd} is the pull-down stack's effective resistance and C_{RL} is the capacitance of the distributed match line. Because it only uses one end to sense, the design has lower read SNM and is more likely to be disturbed by half-select and bitline noise. However, it has lower parasitic capacitance and less dynamic switching power ($\propto C_{BL} V_{DD}{}^2$).

6.3.2 9T SRAM based TCAM Array:

The 9T cell separates storage from evaluation by adding a separate read/search port, as represented in figure 6.2 (b). The 6T latch stores data, two access transistors handle differential write through BL/$\overline{BL}$, and a third NMOS creates a gated read path that connects to RBL (or the evaluation node). Differential signalling makes sure that there are strong overwrite margins during writing, no matter what the cell ratio is. When in search mode, RL is precharged and the read word line (RWL) turns on the read stack without directly

disturbing Q/Q. The comparison is done with a conditional discharge network that is controlled by both stored data and search input. The important thing is that the internal nodes are protected from RL transitions, which stops read disturb. By adding a separate 9T cell, the 9T cell separates storage from evaluation. The effective pull-down path usually has fewer series devices than 8T designs, which lower R_{pd} and making the evaluation, go faster. Also, the stack effect and gated read path help reduce leakage on RL, which increases the match-line sensing margin. This architecture allows for simultaneous read/search and write operations (true dual-port behaviour), which makes it more robust (better SNM, lower Vmin) but also takes up more space and adds routing overhead (extra bitline and control signals).

6.3.3 Hybrid 8T-9T SRAM based TCAM Array:

The hybrid array mixes 8T and 9T cells across rows, using global column lines (BL/$\overline{BL}$, RBL/SL) and local RL per row as demonstrated in figure 6.2(c). Peripheral circuitry must support dual-mode writing, with single-ended drivers for 8T rows and differential drivers for 9T rows. These drivers are usually multiplexed through row decoders. All of the RLs are precharged at the same time during the search, and a global search vector is sent out. Evaluation moves forward at the same time, but with different discharge characteristics.

For example, 8T rows have a higher R_{pd}. As a result, there is timing skew between rows. Sense amplifiers or match detectors need to be margin-aware and often use the worst-case RL discharge from 8T rows to set evaluation windows. Dynamic consumption is lower than with a full 9T array because half of the rows use lower-capacitance single-ended structures. Leakage and stability are better than with a pure 8T array because of the 9T rows. This architecture uses spatial redundancy well to balance P_{dyn}, SNM, and delay, making it a good choice for TCAMs that need moderate robustness without the full 9T overhead.

6.4 PERFORMANCE ANALYSIS OF THE PROPOSED HYBRID 8T-9T SRAM CELL BASED TCAM ARRAY

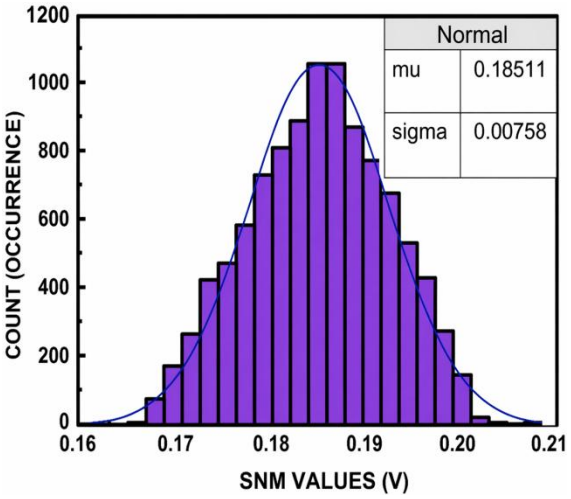
The performance evaluation of the proposed hybrid 8T-9T SRAM cell based TCAM array is carried out to investigate its reliability, stability and operational efficiency under different operating conditions. The analysis mainly focuses on critical parameters such as process corner variations, temperature variations, access time and data retention voltage (DRV) stability which affect the overall functionality of nanoscale memory architectures. Due to the stringent speed and power constraints for the operation of TCAM arrays, the robustness of

the hybrid architecture to manufacturing variations and environmental variations is of importance.

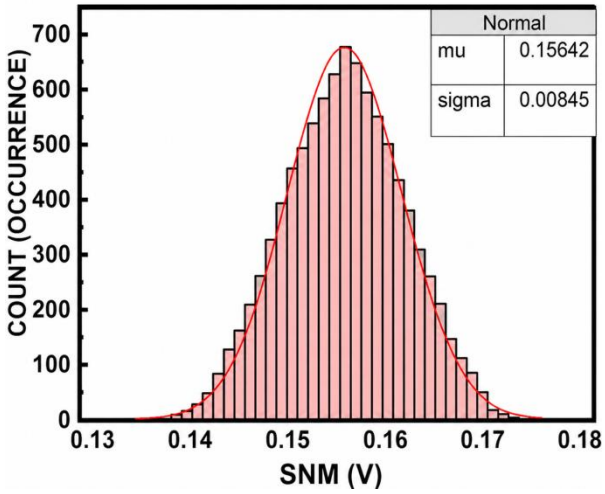
The process corner analysis is used to evaluate the effect of the variations in the transistor parameters on the read and write behavior of the proposed TCAM array. The process corner analysis ensures that the proposed TCAM array can operate in a stable manner for SS, TT, FF, FS and SF corners. The study of the temperature variation further investigates the thermal sensitivity of the hybrid array on a wide range of operating temperatures and shows its capability to provide reliable operation under adverse conditions. In addition, an access time analysis is performed to characterize the array read and search latency which directly impact the high-speed search operations in TCAM applications. Moreover, the data retention voltage stability analysis investigates the lowest voltage at which the supply voltage must be maintained in order to retain the stored data without any failure, which proves the low-voltage robustness along with the stability improvement of the TCAM architecture through the alternate integration of 8T and 9T SRAM cells.

6.4.1 Process Variation Analysis

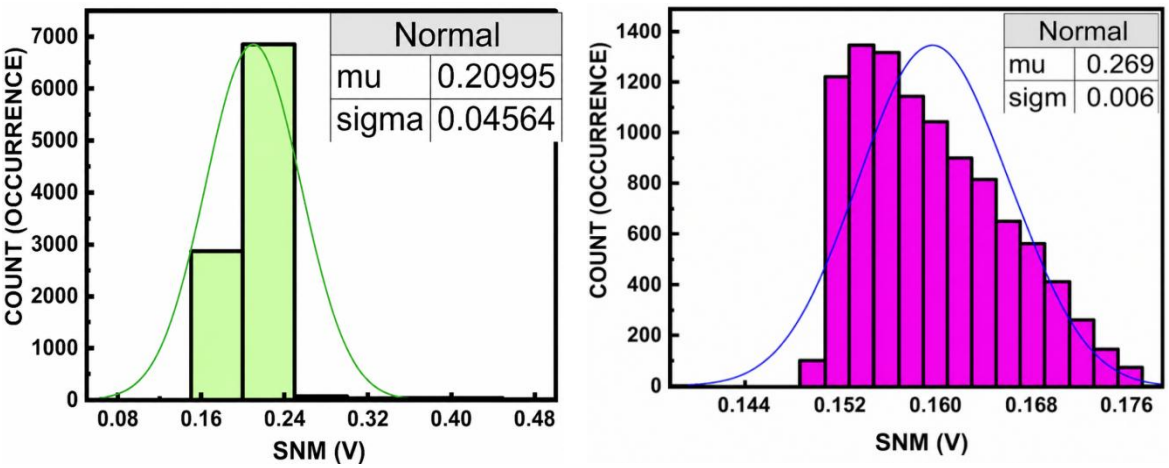
A number of variables, including oxide thickness, doping concentrations, and strain changes, are prone to mistake during integrated circuit fabrication procedures and can result in process variations in circuits [37], particularly with scaled technology nodes. These cause circuits to operate asymmetrically and produce incorrect outcomes. In order to examine the differences under various processes—FF (Fast NMOS Fast PMOS), FS (Fast NMOS Slow PMOS), SF (Slow NMOS Fast PMOS), and SS (Slow NMOS Slow PMOS)—process corner analysis of SRAM cells is carried out.



(a)



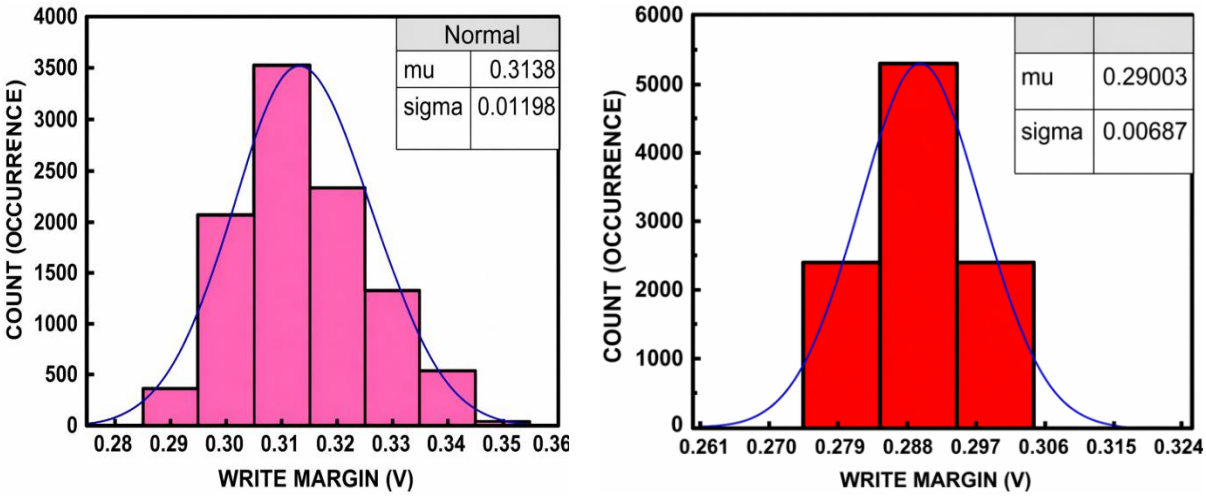
(b)



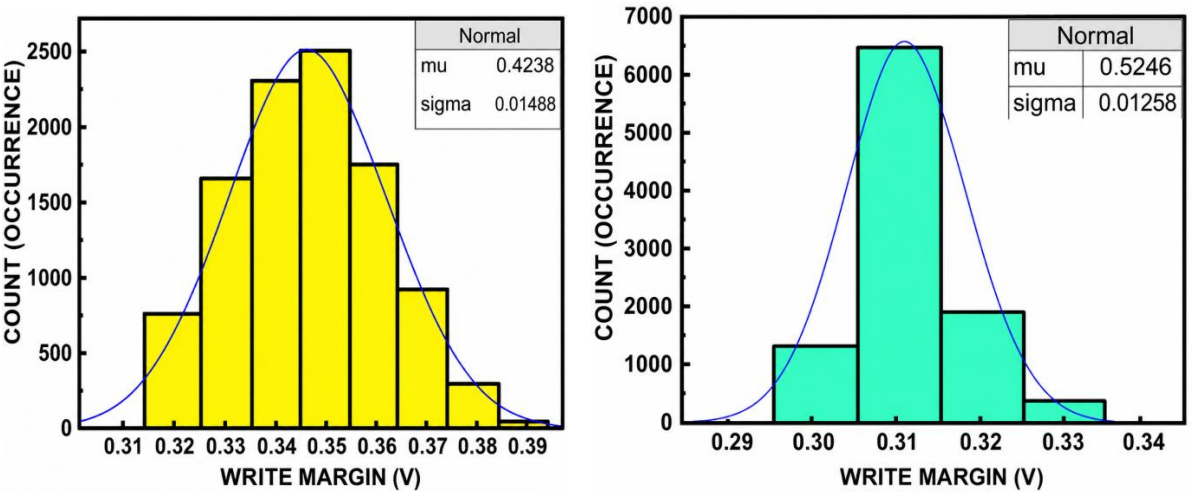
(c) (d)

Fig. 6.4. Process corner variations for Read SNM at (a) SS (b) FF, (c) SF, and (d) FS corners at 0.5 VDD for the SRAM cells based hybrid TCAM array.

The distribution curves for SNM and Write Margin of the suggested hybrid array at 0.5 V VDD is presented as illustrated in Figures. 6.4 and 6.5. 10001-Monte Carlo runs were carried out under the four processes for process corner analysis. The hybrid array is found to have the maximum write margin with a nominal value of 0.346 V and the highest nominal SNM value of 0.209 V at the FS process corner. At the SF process corner, the worst SNM and write margin are recorded at 0.158 V and 0.29 V, respectively. As a result, it is clear that the cell performs poorest at the SF corner and best at the FS corner.



(a) (b)



(c) (d)

Fig. 6.5. Process corner variations for the write margin at (a) SS (b) FF, (c) SF, and (d) FS corners at 0.5 VDD for SRAM cells based hybrid TCAM array.

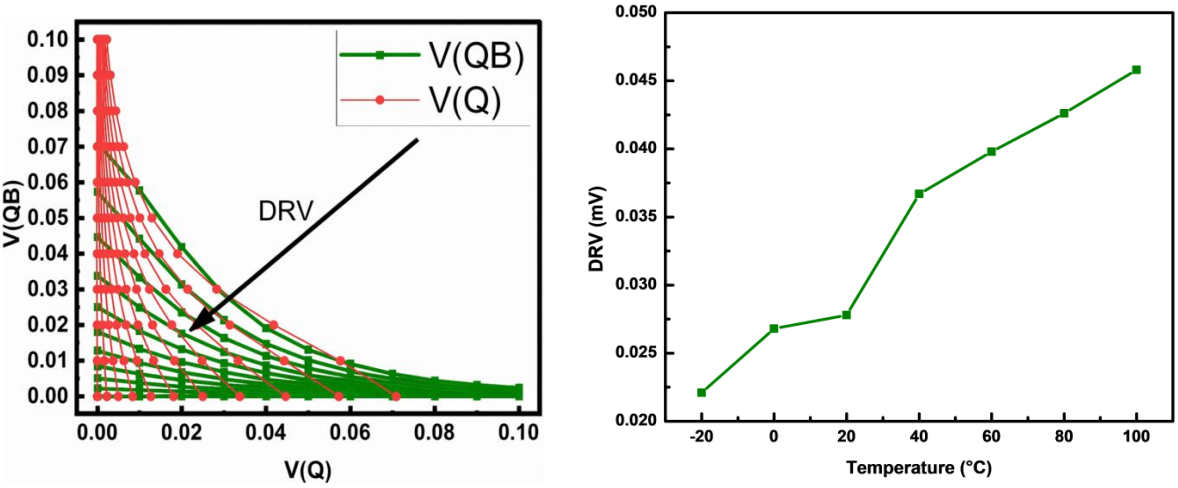
Conversely, a weaker PMOS results in less pull-up conflict, which facilitates the registration of a write-0 and increases the bit-cell's write capability. The NMOS has a lesser current carrying capacity than the PMOS at the FS process corner [38]. The sluggish NMOS devices reduce the inverter's pull-down strength, making it harder for the cell to maintain a "0" at node Q, which lowers SNM. By maintaining a constant stored value, the robust PMOS prevents incorrect write-0. Low NMOS speed, however, suggests that the cell's switching resilience is compromised.

6.4.2 Retention Voltage Analysis

Data Retention Voltage (DRV) is the lowest supply voltage at which an SRAM cell can reliably retain its data during standby operation without the need of refresh. In the proposed hybrid TCAM architecture, the DRV is highly dependent on the stability characteristics of the memory cells. The compact structure of the 8T cells results in lower hold stability at reduced supply voltages, and they are more prone to data loss in near-threshold operation. On the other hand, 9T cells have better retention capability due to stronger internal feedback and better isolation of the storage nodes, which leads to better immunity to process variations and leakage-induced disturbances.

In the alternating 8T–9T configuration, the overall retention limit is mainly limited by the weaker 8T cells, but the neighbouring 9T cells can improve the robustness of the array by alleviating the leakage effects and providing more stable operating conditions. The array is operated at 0.5 V, which is near the sub-threshold region, and device mismatches, threshold-

voltage variation, and leakage currents significantly affect the data retention. The improved stability of 9T cells mitigates the failures caused by variation and improves the reliability of the memory array under such conditions.



(a) (b)

Fig. 6.6 (a) Data Retention voltage across the storage nodes of the cells, and (b) DRV at different temperatures over a range of -20 to 100°C for SRAM cells based hybrid TCAM array.

The hybrid approach is able to suppress such leakages by leveraging the stronger retention. Moreover, the TCAM operation creates extra leakage paths via unselected cells during the match-line evaluation that can exacerbate the retention margins. These leakage effects are effectively limited by the hybrid architecture, thus improving the retention capability of the array. Therefore, the proposed 8T-9T interleaved design can reliably store data at 0.5 V with a good trade-off among memory density, standby power consumption and stability, which is well suited for energy-efficient and variation-resilient TCAM implementation. Figure 6.6(a) shows the retention behavior at the storage node and figure 6.6(b) shows the variation of DRV over a range of operating temperature.

6.4.3 Noise Margin analysis

The SNM is a critical parameter to SRAM stability. For instance, near-threshold operation causes the supply-voltage scaling to increase the sensitivity of read and write reliability. At low supply voltages, the cross-coupled inverters' regenerative action is weakened due to the reduction in transistor overdrive. Process-induced threshold-voltage variations and leakage currents further degrade the cell stability. The 8T cells, because of their compact structure, typically have lower hold SNM and are more susceptible to internal node disturbances from leakage paths, capacitive coupling, and match-line activity in the TCAM environment.

However, 9T cells provide better stability since they have a stronger feedback from the storage node and a fully isolated read path so that perturbations due to the read do not affect the stored data. This architectural decoupling provides significant noise immunity and results in improved overall SNM. The stability characteristics of the hybrid TCAM array (8T and 9T cells in alternating rows) are different across the array. However, the presence of 9T rows improves the overall robustness by reducing the likelihood of read-disturb and half-select failures. The improved retention of the 9T cells also contributes to reduce fluctuations due to leakage and local voltage disturbances during match-line evaluation.

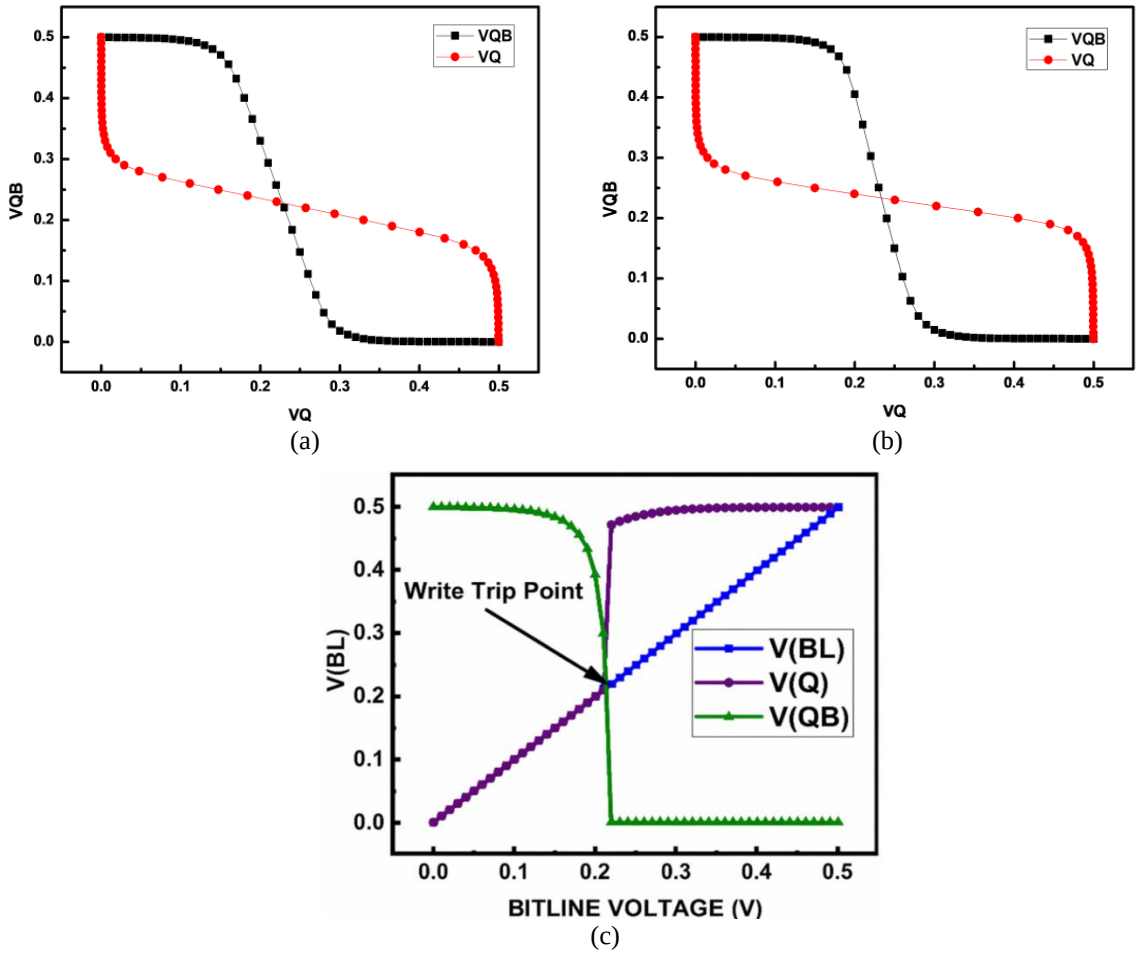


Fig. 6.7 (a) Read SNM, (b) Hold SNM, and (c) Write margin.

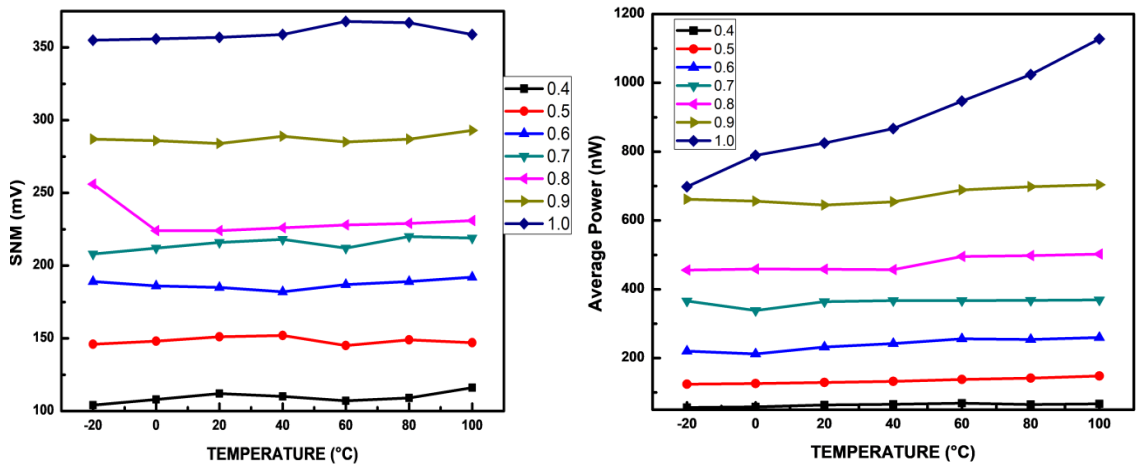
The butterfly characteristics further emphasize these stability differences. Arrays composed entirely of 8T cells have relatively smaller butterfly lobes, indicating lower noise margins . 9T-based arrays produce larger and more symmetrical lobes because of their higher stability. The hybrid architecture shows intermediate butterfly characteristics with less spread and better consistency, indicating the stabilizing effect of the 9T cells on the neighbouring 8T cells. Consequently, the proposed 8T-9T configuration achieves a higher worst-case SNM than the conventional 8T TCAM array with a significantly lower area overhead than a fully

9T-based implementation. This trade-off between stability and silicon efficiency makes the hybrid architecture an attractive solution for low-voltage, variation-tolerant TCAM designs. The corresponding butterfly curves of the 8T, 9T and hybrid arrays are shown in figure. 6.7(a)-(c).

6.4.4 Temperature Variation

Temperature variation is a major concern for the reliability of memory systems based on TCAM and SRAM because it directly impacts the device characteristics, leakage currents and noise margins. Therefore, it is crucial to study the memory stability across a broad temperature range, so as to guarantee its reliability under practical operating conditions. For the evaluation of thermal robustness, the proposed hybrid TCAM array which consists of alternating 8T and 9T cells was analysed from −10°C to 100°C at a supply voltage of 0.5 V. The array operates in the near-threshold region where the behaviour is very sensitive to parameter variations with temperature.

With increase in temperature, mobility of carriers decreases and subthreshold and junction leakage currents increase significantly. These effects result in a decrease of inverter gain, weakening of regenerative feedback and hence a decrease in the static noise margin of the memory cell. Such degradation is more significant in 8T cells, since their storage nodes are more vulnerable to leakage-induced disturbances and internal voltage fluctuations. In contrast, the 9T cells have a higher stability over the full temperature range, as the stronger feedback network and isolated read path efficiently protect the storage nodes from read-related disturbances and leakage effects.



(a) (b)

Fig. 6.8. Impact of temperature variation on (a) Hold (read) SNM, and (b) average power consumption for the hybrid TCAM array.

Lower leakage currents and better carrier transport at lower temperatures lead to improved cell stability, which translates to higher hold and read SNM values for both cell types. The increase of threshold voltage may degrade the write ability slightly, but the retention and read stability are still good. For increasing temperature, device mismatch and leakage increase leading to a broader SNM distribution and a shift towards lower values, indicating a lower noise tolerance. The weaker end of this distribution is mostly associated with the 8T cells.

Table 6.1. Static and dynamic parameters of the proposed hybrid TCAM array.

Parameter		**Max**	**Min**	**Avg**	**STDDEV**
SVNM(mV)		268.64	201.69	235.165	14.631
SINM(nA)		37.17	4.61	20.89	7.26
WTV(mV)		212.615	136.264	174.439	9.237
WTI(pA)		36.248	77.257	56.75	18.02
Write Margin(mV)		246.72	120.294	183.507	13.6715
Delay(ns)	Write"1"	233.71	14.976	124.343	57.234
	Write"0"	63.241	1.736	32.379	12.134
Power(nW)	Write"1"	6.390	1.2361	3.359	1.169
	Write"0"	3.467	0.278	1.8725	0.3694
	Read "1"	6.7386	0.19782	3.46821	1.4692
	Readc"0"	0.69212	0.432179	0.562149	0.234687

Table 6.2. Static and dynamic parameters of the proposed single port 8T cell based TCAM array

Parameter		**Max**	**Min**	**Avg**	**STDDEV**
SVNM(mV)		242.363	187.413	214.8875	13.631
SINM(nA)		37.4	5.02	21.34	6.98
WTV(mV)		259.321	178.368	218.8445	9.246
WTI(pA)		32.78	99.8765	64.578	11.3878
Write Margin(mV)		248.95	120.987	178.645	12.36457
Delay(ns)	Write"1"	238.796	10.268	169.547	44.23654
	Write"0"	67.8260	3.2567	35.678	12.38742
Power(nW)	Write"1"	8.4798	2.4789	5.32147	2.18779
	Write"0"	9.6321	0.97245	4.5689	0.98715
	Read "1"	7.2689	0.457896	0.236877	1.64789
	Read"0"	0.895647	0.567498	0.98547	0.134589

The hybrid architecture with alternating 9T cells improves thermal resilience by limiting the propagation of disturbance and reducing the probability of half-select and read-disturb failures in the neighbouring 8T rows. Moreover, high temperature causes the leakage current from unselected cells during the match-line evaluation, which introduces more noise to the memory array. The increased insulation of the 9T cells mitigates these effects and helps maintain the stability of neighbouring cells. Static and dynamic parameters of the proposed hybrid, 8T cell based and 9T cell based TCAM arrays are mentioned in Tables 6.1, 6.2 and 6.3, respectively.

Table 6.3. Static and dynamic parameters of the proposed dual port 9T cell based TCAM array.

Parameter		**Max**	**Min**	**Avg**	**STDDEV**
SVNM(mV)		237.39	181.271	209.3305	13.231
SINM(nA)		38.72	4.28	14.8	7.65
WTV(mV)		246.321	215.356	179.654	7.869
WTI(pA)		34.56	98632	18.9	9.25
Write Margin(mV)		168.25	24.3669	187.69	14.256588
Delay(ns)	**Write"1"**	166.472	20.2032	84.24434	67.065328
	Write"0"	82.2041	6.22563	28.228	13.02565
Power(nW)	**Write"1"**	9.3720	2.0158	6.45585	0.3256
	Write"0"	4.32311	0.955045	7.25882	1.025
	Read "1"	7.92464	0.35659	0.2265546	1.33654
	Read"0"	0.98562	0.322655	1.26554	0.25645

Overall, the proposed 8T-9T hybrid TCAM has a better temperature tolerance than a conventional 8T-only implementation. The 8T cells are the bottleneck in terms of worst-case stability, but the array is still reliable in the full temperature range from -10C to 100C at a 0.5V supply. Figure 6.8(a) and 6.8(b) show the measured temperature coefficients of HSNM/RSNM and write margin are about 0.15 mV/°C and 0.084 mV/°C, respectively. These relatively small variations confirm that the incorporation of 9T a cell effectively enhance the thermal stability and allows robust hold, read and write performance under changing environmental conditions.

6.4.5 Bit Error for Hybrid TCAM Array

The Bit Error Rate (BER) is an important metric to evaluate the reliability of TCAM arrays since it indicates the probability of getting incorrect search results due to process, voltage and temperature (PVT) variations. The proposed 8x8 hybrid TCAM architecture is constructed by using alternating rows of 8T and 9T SRAM based cells, in order to benefit from the complementary advantages of both designs. The 8T cells provide less area and switching activity. The 9T cells provide more operational robustness. This is due to dedicated read/search circuitry that isolates the storage nodes from disturbances caused by searching. This isolation enhances the accuracy of search and significantly decreases the chance of erroneous state transition during memory access.

Not all bit errors are equal to the overall search in TCAM applications. Errors in the most significant bits (MSB) affect the interpreted value of the word more than errors in the least significant bits (LSB). Thus, the importance of the wrong bits positions should be taken into account in the BER analysis. The worst-case error condition, used to evaluate the maximum possible degradation in search accuracy, corresponds to the case of simultaneous wrong decisions in all the lower order bits, as shown in figure 6.9.

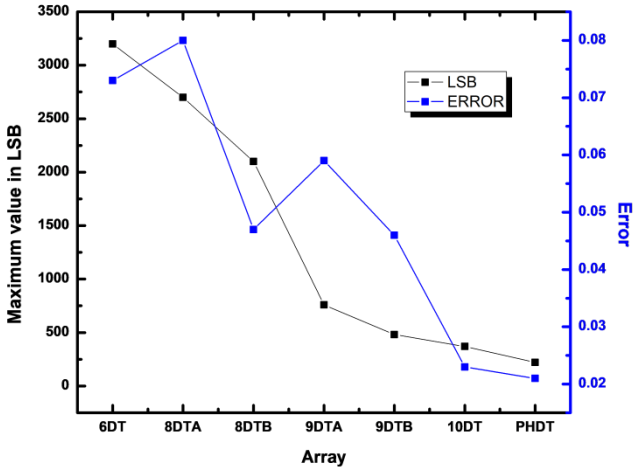


Fig. 6.9. Maximum bit error corresponding information stored in the LSB bits.

In a parallel search operation, the match-line decisions are determined by the charge and discharge characteristics of the associated sensing circuitry. Variations in threshold voltage, leakage currents, capacitive coupling and transient noise can lead to false-match or false-mismatch events and therefore increase the probability of search failure. The heterogeneous arrangement of 8T and 9T alternating rows is beneficial in spreading these disturbances more evenly across the array, reducing susceptibility to soft errors and local process-induced variations. Moreover, the better isolation of the 9T cells improves the match-line integrity and reduces the false discharge events, especially in low-voltage operation.

The proposed hybrid TCAM architecture demonstrates better search reliability, fault tolerance, and reduced data corruption probability than homogeneous SRAM-based TCAM implementations. These advantages are particularly important in nanoscale CMOS technologies and near threshold operation, where device variability and leakage effects are more significant. The evaluation of the BER thus yields a quantitative measure of the worst-case reliability of the proposed array and validates the suitability of the proposed array for robust low-power associative memory applications.

6.4.6 Power Consumption

Power consumption remains a critical issue for SRAM-based TCAM architectures, where all memory words participate in parallel search operations, leading to high switching activity and large match-line energy dissipation. To overcome this problem, the proposed 8×8 hybrid TCAM array adopts an interleaved layout of 8T and 9T SRAM-based cells combining the benefits of both topologies to achieve better overall power efficiency.

The compact structure and reduced parasitic capacitance of the 8T cells contribute to decrease dynamic energy consumption. The 9T cells improve the power characteristics by isolating the storage nodes from the search and read operations. This isolation reduces the undesired transition of the internal nodes and leakage power consumption during the standby and active mode. Moreover, the alternating pattern of 8T and 9T cells ensures a more even current distribution throughout the array to avoid hot current spots, and thus reduces the transient power consumption during the search operations.

During TCAM operation, the match-line switching is mostly restricted to the rows with mismatched entries, whereas the matched rows have small voltage variations. This selective discharge mechanism reduces the switching activity and improves the energy utilization. Furthermore, the heterogeneous cell organization reduces leakage-induced losses and suppresses short-circuit currents caused by process variations and temperature fluctuations. As a result, the proposed hybrid architecture achieves lower power dissipation while maintaining reliable search functionality and is a suitable candidate for low-power and high-performance associative memory applications. The total power consumption of the proposed array can be written as:

$$P_{S_Hold} = j * n * I_{S_l} * t * V_{DD}, \quad (6.1)$$

$$P_{S_Read} = j * C_{RL} * V_{DD}^2 + 0.5 * n * C_{BL} * V_{DD}^2, \quad (6.2)$$

$$P_{S_Write} = j * C_{WL} * V^2_{DD} + 0.5 * n * C_{BL} * V^2_{DD} + n * C_W, \quad (6.3)$$

$$P_{TS} = P_{S_Hold} + P_{Read} * P_{S_Read} + P_{Write} * P_{S_}, \quad (6.4)$$

The equation for calculation of power [63] of the hybrid array is given below;

$$P_T = j * k * I_{S_l} * t * V_{DD} + P_{Read}(j * C_{RL} * V_{DD}^2 + 0.5 * n * C_{BL} * V_{DD}^2) + P_{Write}(j * C_{WL} * V_{DD}^2 + n * C_{BL} * V_{DD}^2 + n * C_W) + j * (k - n) * I_{D_l} * t * V_{DD} + P_{Read}(j * C_{RL} * V_{DD}^2 + 0.5 * (k - n) * C_{RBL} * V_{DD}^2) + P_{Write}(j * C_{WL} * V_{DD}^2 + 0.5 (k - n) * C_{BL} * V_{DD}^2 + (k - n) * C_W) \quad (6.5)$$

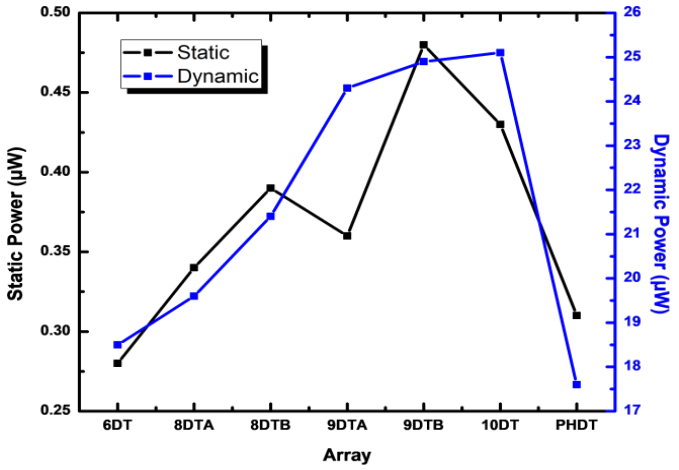


Fig. 6.10. Power consumption curve for the proposed TCAM array configuration for different array partition.

9T cell presence also improves low-voltage operation with enhanced robustness to sensing and enhanced immunity to search-induced disturbances. This allows the array to work reliably at reduced supply voltages, resulting in a significant reduction in dynamic power due to the quadratic relationship between switching power and supply voltage. Thus, the hybrid architecture is an effective compromise between power efficiency, search accuracy and operational reliability.

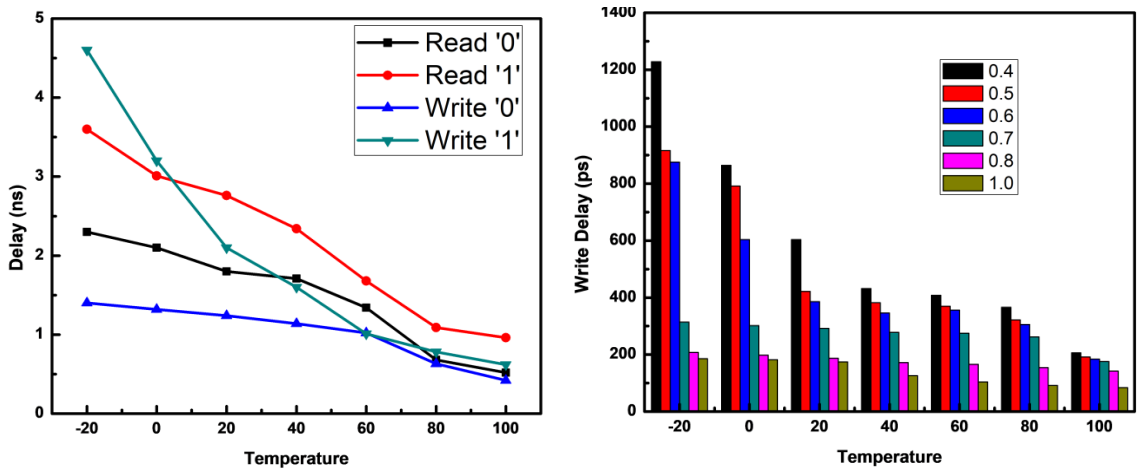
The proposed 8×8 hybrid TCAM array, because of these advantages, is a good candidate for energy-constrained applications such as networking equipment, associative computing platforms and high-speed pattern-matching engines implemented in advanced CMOS technologies. The static power consumption of the array measured is plotted in figure 6.10 and it ranges from 0.27 µW to 0.48 µW. The dynamic power varies from 17.6 µW to 25.8 µW.

6.4.7 Read and Write Delay for the Hybrid TCAM array

The analysis that has been completed and presented thus far is static and does not take into consideration the time needed to complete the read and write operations of a bit cell. Real-time processes, however, have a time restriction, and the read and write access operations of a bit cell are crucial in dictating how rapidly the bit cell functions. The read operation is the time required to lower the bit cell's BL value to the switching voltage required for an inverter.

Read Delay

Read delay is the time it takes for the bit-line voltage to rise high enough for the sense circuitry to accurately tell the difference between the stored logic states. The alternating 8T and 9T SRAM-based cells are deployed in the proposed 8×8 hybrid TCAM array to achieve the effective trade-offs between access speed, stability and power efficiency. The 9T cells have independent read paths that disconnect the storage nodes from the bit-lines, thus reducing read disturbance and enabling faster, more reliable sensing. On the contrary, the 8T cells have reduced parasitic capacitance and less transistor loading, which lead to faster signal propagation and shorter access times. During the TCAM searches, the match lines are precharged and selectively discharged based on the stored data and the search pattern. The staggered distribution of 8T and 9T cells helps to spread the match-line loading more evenly across the array, thus reducing propagation delay and improving sensing accuracy. Thus, the hybrid structure offers improved read performance, while preserving the robustness and energy efficiency needed for low voltage TCAM applications.



(a) (b)

Fig. 6.11. Delay for different operations on proposed TCAM array, (a) delay vs. temperature at 0.3 V VDD, and (b) write-0 delay w.r.t to temperature at increasing VDD.

In addition, the hybrid architecture improves timing robustness by reducing delay variations from process and temperature variations. The presence of 9T cells in the alternate rows enhances the read stability and provides more uniform sensing behavior for different operating conditions. Therefore, the proposed 8×8 hybrid TCAM array provides higher reliability; lower read access latency and faster match detection compared to the conventional homogeneous SRAM-based TCAM architectures. Such benefits are of particular importance in the case of low-voltage operation and in advanced nanoscale CMOS technologies where device variability and noise effects are more prominent.

Write Delay

The write delay is the time needed for the TCAM cell to successfully overwrite the existing data and create a new stable logic state. In SRAM based TCAM architectures, write performance is determined by the transistor sizing, the strength of the access transistor, the bit-line capacitance, and the capability of the write circuitry to overcome the feedback of the cross-coupled storage inverters. The alternative combination of 8T and 9T SRAM cells in the proposed 8×8 hybrid TCAM array can achieve a good tradeoff between the write speed and the operation stability.

The 8T cells have a simpler structure, lower internal capacitance and lower write resistance, which helps in fast charging and discharging of the storage nodes, thus helping in the faster write operation. At the same time, the 9T cells improve the resilience via better node isolation and higher immunity to external disturbances, enabling reliable data transitions even under concurrent search and memory-access operations. The interleaved placement of 8T and 9T cells also helps distribute the capacitive loading more evenly across the array, thus reducing the bit-line delay and improving the overall write efficiency.

Additionally, the reduced leakage currents and better voltage-transfer characteristics speed up the settling of internal nodes following a write operation. The presence of 9T cells further enhances the process and temperature variation tolerance, reducing the likelihood of incomplete switching events and improving reliability when operating at a reduced supply-voltage. Hence the proposed hybrid architecture can achieve shorter write latency, while being stable under a wide range of operating conditions. In summary, the 8×8 hybrid TCAM array shows better read and write access performance than arrays built from a single cell type, as summarized in Table 6.1. Fig. 6.11(a) and Fig. 6.11(b) show the variation of read and write

delay with supply voltage from 0.4 V to 1.0 V, respectively, which demonstrates the efficiency of the presented architecture for both nominal and near-threshold operations.

6.5 HIGHLIGHTS OF IMPORTANT RESULTS

The rising demand for energy-efficient portable and battery-operated electronic systems has increased the need for low-power memory architectures in modern System-on-Chip (SoC) and microprocessor designs. Optimization of the SRAM array architecture is a critical research goal, since SRAM based memories occupy a large portion of the total chip area and dissipate a large amount of the total power. In this work, a hybrid TCAM array architecture based on alternate 8T single-port and 9T dual-port SRAM cells has been proposed to achieve reduced power consumption, improved stability and enhanced fault tolerance over the conventional homogeneous SRAM-based TCAM arrays.

Instead of using identical bit cells to build traditional memory arrays, the proposed architecture uses heterogeneous SRAM cells within the same array structure. The hybrid arrangement takes advantage of the benefits of both 8T and 9T SRAM topologies, where the 8T cell has lower area and power consumption, and the 9T cell offers better read stability and isolation characteristics. The proposed TCAM array combines these cells in alternate configurations to obtain an optimized trade-off among power dissipation, the operational stability and the reliability.

Various partitioning configurations with different combinations of single-port and dual-port cells were explored to evaluate the impact of the array organization on the overall performance. The obtained results demonstrate that the hybrid TCAM array is very power efficient in static and dynamic conditions. With the growing integration of memory intensive applications in modern SoCs and portable electronic devices, power-efficient and reliable memory design has become an important research objective. SRAM arrays consume a large fraction of the on-chip area and are major contributors to the overall energy consumption, improving their efficiency is still important for next-generation computing systems. Here, we propose a hybrid TCAM architecture based on alternating single-port 8T and dual-port 9T SRAM cells, to improve energy efficiency, stability and reliability along with practical implementation overheads. The proposed design differs from conventional TCAM arrays, which use the same cell architecture throughout the memory, as it uses a heterogeneous organization with 8T and 9T cells coexisting inside the same array. This approach takes advantage of the low area and low power characteristics of the 8T cell, and the superior read isolation and robustness of the

9T cell. The architecture achieves a well-aimed trade-off between power consumption, access stability and fault tolerance through the strategic interleaving of the two cell types.

A detailed study has been performed with a variety of array configurations to investigate the effect of cell arrangement on the overall performance. Simulation results show that the hybrid architecture can lead to substantial power savings in active and standby operation. The static power consumption is in the range of 0.27 μW to 0.48 μW and the dynamic power is between 17.6 μW and 25.8 μW. The proposed configuration results in about 3.5% and 20.7% reduction of the static and dynamic power compared to a TCAM array built only with dual-port cells confirming the effectiveness of the heterogeneous design strategy.

In addition to power reduction, the hybrid array provides excellent robustness against process and operating-condition variations. The employment of 9T cells improves read isolation and minimizes disturbance during simultaneous search and memory-access operations, leading to increased search reliability and lower susceptibility to errors. The observed error tolerance factor of around 0.015 further confirms the robustness of the proposed architecture. Statistical analysis under process variations shows stable memory operation over a wide range of conditions. The measured SVNM is from 201.69 mV to 268.64 mV with the average value of 235.165 mV and standard deviation of 14.631 mV, which indicates a good read stability. Likewise, the average SINM of 20.89 nA indicates reliable operation in current mode. The extracted Write Trip Voltage (WTV) and Write Margin (WM) values further verify the improved writability and operational robustness of the hybrid TCAM array, with an average value of 174.439 mV and 183.507 mV, respectively.

Although the present paper focuses on a single-level hybrid organization, the proposed concept can be extended to more sophisticated memory structures. Future research directions could be adaptive cell placement strategies, multi-level partitioned architectures, leakage-aware design techniques and operation in ultra-low-voltage regions. These improvements may help to improve energy efficiency and reliability for deeply scaled CMOS technologies where process variability and leakage effects become more and more important. The proposed hybrid 8T-9T SRAM-based TCAM array integrates the advantages of heterogeneous memory cells, resulting in low power consumption, better stability, and improved overall error resilience. These features make it a very promising candidate for future low-power associative memories, intelligent edge-computing systems and high-performance search-oriented applications.

CHAPTER - 7
CONCLUSIONS AND FUTURE SCOPE

The present research work is focused on the design and analysis of different SRAM cells: 8T, 9T and 11T based on structural modifications and port architectures. These proposed cells are further utilized to design Cam and TCAM cells, blocks and their respective arrays. This chapter summarizes the important results of the proposed work. Conjointly, it also presents some specific directions for future research work.

7.1 CONCLUSIONS

This research work presented the design, analysis and performance evaluation of advanced low power SRAM cells and SRAM based TCAM architectures for nanoscale memory applications. The work was mainly focused on enhancing read stability, write margin, leakage reduction, low-voltage operation and energy efficient associative search performance through the development of optimized 8T, 9T and 11T SRAM cells and their integration in hybrid TCAM architectures. The proposed research effectively tackled a few critical limitations of the conventional SRAM and TCAM structures, especially under aggressive technology scaling and near-threshold operating conditions.

The first objective of this work was to design and study advanced 9T and 11T SRAM cells with enhanced stability and low power operation. The proposed 9T SRAM cell with 32nm CMOS technology and 0.9V supply voltage showed significant improvement in noise immunity, power and operational robustness. The cells has achieved the read, hold and write static noise margins of ~0.368 V, 0.364 V and 0.422 V respectively, which is indicative of highly stable operation during all the memory access conditions. Moreover, the proposed 9T cell demonstrated very low leakage power consumption of about 22.1nW along with reduced write and read access times of nearly 1.2ns and 4.5ns respectively. The analysis also revealed enhanced stability with temperature and process-corner variations, confirming the validity of the architecture for reliable nanoscale memory operation.

Similarly, the proposed 11T SRAM cell showed an improved ultralow-voltage operation at the operating voltage of 500 mV. The cell obtained read and hold SNMs of 184 mV and 197.26 mV, respectively, and the write SNM achieved around 265 mV, showing a significant improvement in writability. The proposed 11T structure also demonstrated extremely fast read and write access times of approximately 11.38 ps and 16.24 ps, respectively. The Monte

Carlo simulation considering 5000 samples was used to verify the architecture's robustness under global process variations. The proposed 11T SRAM cell has exhibited the lower read and write power consumption with better operational stability than the previously reported SRAM structures. These results show that higher transistor SRAM architectures improve low voltage reliability and variation tolerance significantly in advanced CMOS technologies.

The second target of the study was the design and evaluation of low-power 8T SRAM architecture with focus on ultralow-voltage operation, improved static noise margin and temperature stability. The proposed 8T SRAM cell operating at 32nm CMOS technology and 400mV supply voltage achieved read and hold SNMs of nearly 181mV and 178mV, respectively, and the write margin of about 204mV. The architecture has achieved excellent stability enhancement for all memory operations by optimized read isolation and single-ended sensing mechanisms. The proposed 8T SRAM cell also demonstrated a lower leakage current and lower standby power dissipation compared to conventional SRAM structures. Temperature variation analysis and process corner evaluation showed strong robustness with less sensitivity to RSNM, HSNM and write margin degradation. The results show that read-path 8T SRAM architectures in stand-alone configurations are very powerful for ultralow-power and sub-threshold memory applications.

The third objective was to design SRAM-based TCAM blocks using the proposed SRAM cells and analyze their performance. The designed TCAM architectures showed an improvement in search performance, power efficiency and delay optimization, compared to the existing SRAM based CAM implementation. Single-ended 8T SRAM based TCAM block performance is better than previously reported 7T, 9T, 10T and 11T SRAM based CAM cells. The proposed CAM structure gives an average power consumption of 0.89 mW and search delay of 34.78 ps respectively. In addition, the measured search power consumption for matching and mismatching were about 456 μW and 481 μW respectively, which validated the effective reduction of search-line and match-line switching activity. The results demonstrate that SRAM based TCAM architectures with isolated read mechanisms and single-ended sensing can achieve significant reductions in dynamic search energy while supporting high-speed associative search operation.

The fourth objective of the work was to design an alternate hybrid 8T–9T SRAM based TCAM array architecture for low power and error-resilient memory operation. The proposed hybrid array, in contrast to conventional homogeneous SRAM arrays, uses alternate single port 8T and dual port 9T SRAM cells within the same memory array to simultaneously

exploit multiple topologies. The implemented 8 kB memory array with 512 rows and 16 columns showed a significant reduction in static and dynamic power consumption. The hybrid architecture achieved static and dynamic power dissipation of approximately 0.29 μW and 23 μW, respectively, which is a significant reduction over arrays constructed only from dual-port SRAM cells. The architecture also exhibited better tolerance to process variations and lower probability of search failure due to the diversified cell distribution across the array. The results obtained confirm the effectiveness of the heterogeneous SRAM integration to achieve an optimized trade-off between stability, leakage reduction, power efficiency and search reliability.

In conclusion, the proposed research has successfully demonstrated the significant improvements of the advanced 8T, 9T, and 11T SRAM cells over the conventional SRAM architecture in terms of read stability, writability, leakage suppression, ultra-low-voltage operation, and process variation tolerance. Moreover, the SRAM cells used in the SRAM-based TCAM blocks and hybrid alternate TCAM arrays improved the associative search efficiency significantly and reduced the power dissipation. The proposed hybrid SRAM-TCAM framework effectively combines the benefits of isolated read operation, single-ended sensing, reduced switching activity and enhanced stability for energy-efficient associative computing tailored to modern nanoscale VLSI systems.

7.2 FUTURE SCOPE

The proposed research provides a significant improvement in the performance of SRAM and TCAM, however, there are many opportunities to further improve and extend the developed architectures. Future work can be devoted to advanced technology scaling, intelligent memory optimization, AI-oriented associative computing, and emerging device integration to further improve the performance and applicability of hybrid SRAM-TCAM systems.

One important future direction is to extend the proposed SRAM and TCAM architectures to deeply scaled FinFET, Gate-All-Around (GAA), nanosheet, and CFET technologies below the 10 nm technology node. As CMOS technology is scaled to sub-5 nm regimes, short-channel effects, leakage current, threshold voltage fluctuation and variability induced instability will be more severe. The proposed hybrid SRAM-TCAM architectures can be realized by advanced device technologies for further improvement of electrostatic gate control, leakage suppression and low-voltage operability for future high density memory systems.

Another interesting research direction is the hybrid SRAM array with the integration of adaptive assist circuit and intelligent control method. The combination of dynamic body biasing, adaptive word line boosting, data-aware sensing and self-timed search line activation techniques can further improve stability and reduce dynamic energy consumption. Adaptive control mechanisms assisted by machine learning may also be explored for runtime optimization of memory power and performance under different workload conditions.

Future work can also be focused on implementing larger SRAM-based TCAM arrays with hierarchical search organization and segmented match-line evaluation techniques. TCAM power consumption is dominated by match-line switching activity, advanced search optimization techniques such as selective precharge, current-race sensing and low-swing match-line architectures can be incorporated to further reduce search energy and sensing delay. Multi-bank associative search structures and partitioned TCAM architectures are also promising to improve the scalability for networking and AI acceleration applications.

The proposed hybrid TCAM architecture can also be extended for the fault tolerant and radiation hardened memory systems for aerospace and secure computing applications. Future work may consider soft-error-resilient SRAM cells that include error correction, redundancy-based fault recovery, and multi-node upset tolerant techniques. Reliability analysis under radiation effects, thermal stress and process aging conditions can further verify the suitability of the architecture for mission critical applications.

Another future direction is to explore emerging non-volatile memory technologies such as RRAM, STT-MRAM, FinFET, and memristor-based TCAM architectures with SRAM hybrid arrays. In this kind of heterogeneous memory systems, the high-speed operation of SRAM and the non-volatility and ultralow leakage features of emerging devices can be exploited, to achieve highly energy-efficient associative computing platform.

Future work may also include more optimal physical layout techniques and area-conscious design approaches for heterogeneous SRAM integration. Higher transistor-count SRAM cells add additional silicon area overhead, but future layout optimization techniques will be able to improve density while still providing the stability and performance benefits. Three-dimensional memory integration and monolithic 3D stacking can also improve the memory density and interconnect delay in future hybrid SRAM-TCAM systems.

In conclusion, the proposed research provides a solid basis for the development of low-power, variation-tolerant, and energy-efficient hybrid SRAM-TCAM architectures. The

obtained results demonstrate that the heterogeneous integration of advanced 8T, 9T and 11T SRAM cells in associative memory arrays is a very promising direction for future nano-scale VLSI memory systems and intelligent computing platforms.

7.3 SOCIAL IMPACT

The proposed low power SRAM and SRAM–TCAM architectures are of great societal relevance because they address one of the main challenges of modern electronics: the reduction of energy consumption while maintaining high computational performance. The ability of the developed 8T, 9T and 11T SRAM cells to operate reliably at low supply voltages makes it suitable for designing energy-efficient processors, embedded systems and smart electronic devices with extended battery life. These improvements are especially useful for Internet-of-Things (IoT) applications, wearable healthcare devices, environmental monitoring systems and portable consumer electronics, where power availability is typically limited. The proposed architectures can help to reduce leakage power and improve memory stability, which can result in the development of sustainable computing systems with lower energy requirements and reduced environmental impact.

The hybrid SRAM–TCAM architecture proposed here also addresses the rising demand for fast and dependable data processing in emerging technologies such as artificial intelligence, edge computing, autonomous systems, and secure communication networks. Improved associative search capability and low power operation can boost the performance of real-time applications such as medical diagnostics, smart transportation, cyber security systems, image recognition and aerospace electronics. Moreover, the enhanced robustness against process variations and environmental fluctuations increases the reliability of the system in safety-critical applications. This work contributes to the development of next-generation intelligent computing platforms that can deliver high performance with lower power consumption and improved reliability of operations by enabling efficient storage, search and processing within a unified memory framework.

REFERENCES

[1] F. Arnaud, F. Boeuf, F. Salvetti, D. Lenoble, F. Wacquant, C. Regnier, et al., "A functional 0.69 um^2 embedded 6T-SRAM bit cell for 65 nm CMOS platform," Symposium on VLSI Technology, 2003.

[2] L. Wen, X. Cheng, K. Zhou, S. Tian, and X. Zeng, "Bit-Interleaving-Enabled 8T SRAM with Shared Data-Aware-Write and Reference-Based Sense Amplifier," IEEE TCAS-II, 2016.

[3] I. Ahsan et al., "Tristate Inverter Array: A New Technology Development Yield Learning Vehicle Complementing Traditional SRAM Array," IEEE Transactions on Semiconductor Manufacturing, 2015.

[4] R. Giterman, M. Vicentowski, I. Levi, Y. Weizman, O. Keren, and A. Fish, "Leakage Power Attack-Resilient Symmetrical 8T SRAM Cell," IEEE TVLSI, 2018.

[5] Y. Yang, J. Park, S. C. Song, J. Wang, G. Yeap, and S. O. Jung, "Single-Ended 9T SRAM Cell for Near-Threshold Voltage Operation With Enhanced Read Performance in 22-nm FinFET Technology," IEEE TVLSI, 2015.

[6] S. Pal, S. Bose, W. H. Ki, and A. Islam, "Characterization of Half-Select Free Write Assist 9T SRAM Cell," IEEE TED, 2019.

[7] K. Cho, J. Park, T. W. Oh, and S. O. Jung, "One-Sided Schmitt-Trigger-Based 9T SRAM Cell for Near-Threshold Operation," IEEE TCAS-I, 2020.

[8] J. P. Kulkarni and K. Roy, "Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design," IEEE TVLSI, 2012.

[9] E. Shakouri, B. Ebrahimi, N. Eslami, and M. Chahardori, "Single-Ended 10T SRAM Cell with High Yield and Low Standby Power," Circuits, Systems and Signal Processing, 2021.

[10] Y. He, J. Zhang, X. Wu, X. Si, S. Zhen, and B. Zhang, "A Half-Select Disturb-Free 11T SRAM Cell with Built-In Write/Read-Assist Scheme for Ultralow-Voltage Operations," IEEE TVLSI, 2019.

[11] R. Lorenzo and R. Pailly, "Single bit-line 11T SRAM cell for low power and improved stability," IET Computer & Digital Techniques, 2020.

[12] J. Jiang et al., "Quadruple Cross-Coupled Latch-Based 10T and 12T SRAM Bit-Cell Designs for Highly Reliable Terrestrial Applications," IEEE TCAS-I, 2019.

[13] A. Sachdeva and V. K. Tomar, "A Schmitt-Trigger based low read power 12T SRAM cell," Analog Integrated Circuits and Signal Processing, 2020.

[14] L. Atias et al., "A Low-Voltage Radiation-Hardened 13T SRAM Bitcell for Ultralow Power Space Applications," IEEE TVLSI, 2016.

[15] M. Ansari et al., “A near-threshold 7T SRAM cell with high write and read margins and low write time for sub-20 nm FinFET technologies,” Integration, the VLSI Journal, 2015.

[16] R. N. Asli and S. Taghipour, “A near-Threshold Soft Error Resilient 7T SRAM cell with Low Read Time for 20 nm FinFET Technology,” Journal of Electronic Testing, 2017.

[17] R. Giterman, O. Keren, and A. Fish, “A 7T Security Oriented SRAM bitcell,” IEEE TCAS-II, 2019.

[18] J. S. Oh et al., “Differential Read/Write 7T SRAM with Bit-Interleaved Structure for Near-Threshold Operation,” IEEE Access, 2021.

[19] K. C. Chun et al., “A 2T1C Embedded DRAM Macro With No Boosted Supplies Featuring a 7T SRAM Based Repair and a Cell Storage Monitor,” IEEE JSSC, 2012.

[20] R. N. Asli and S. Taghipour, “Reliable and high performance asymmetric FinFET SRAM cell using back-gate control,” Microelectronics Reliability, 2020.

[21] J. S. Liu et al., “An energy-efficient tensile strained Ge/InGaAs FET 7T SRAM cell architecture for ultralow voltage applications,” IEEE TED, 2017.

[22] S. Ahmad et al., “TFET-Based Robust 7T SRAM cell for Low Power Application,” IEEE TED, 2019.

[23] S. A. Tawfik and V. Kursun, “Low power and robust 7T dual-Vt SRAM circuit,” ISCAS, 2008.

[24] T. Suzuki et al., “A stable 2-port SRAM cell design against simultaneously read/write-disturbed accesses,” IEEE JSSC, 2008.

[25] S. Gupta, K. Gupta, and N. Pandey, “A 32-nm Subthreshold 7T SRAM Bit Cell With Read Assist,” IEEE TVLSI, 2017.

[26] C T. Kobayashi et al., “A current controlled latch sense amplifier and a static power-saving input buffer for low-power architecture,” IEEE JSSC, 1993.

[27] K. R. S. Sanapala and S. S. Yeo, “Schmitt trigger-based single-ended 7T SRAM cell for IoT applications,” Journal of Supercomputing, 2018.

[28] B. Madiwalar and B. S. Kariyappa, “Single bit-line 7T SRAM cell for low power and high SNM,” iMac4s Conference, 2013.

[29] C. B. Kushwah et al., “Single-ended Boost-less (SE-BL) 7T Process Tolerant SRAM Design in Sub-threshold Regime for Ultra-low-power applications,” Circuits, Systems and Signal Processing, 2016.

[30] I. J. Chang et al., “A Priority-Based 6T/8T Hybrid SRAM Architecture for Aggressive Voltage Scaling in Video Application,” IEEE TCSVT, 2011K. Sasaki et al., “A 23 ns 4 Mb CMOS SRAM with 0.5 uA standby current,” ISSCC, 1990.

[31] T. N. Blalock and R. C. Jaeger, “A High Speed Clamped Bit-line Current Mode Sense Amplifier,” IEEE JSSC, 1991.

[32] L. Pileggi et al., “Mismatch analysis and statistical design at 65 nm and below,” Custom Integrated Circuits Conference, 2008.

[33] T. Seki et al., “A 6-ns 1-Mb CMOS SRAM with latched sense amplifier,” IEEE JSSC, 1991.

[34] C. Roy and A. Islam, “Power-aware source feedback single-ended 7T SRAM cell at nanoscale regime,” Microsystems Technologies, 2017.

[35] J. M. Hill and J. Lachman, “A 900 MHz 2.25 MB cache with on-chip CPU—now in Cu SOI,” ISSCC, 2001.

[36] P. Singh and S. K. Vishvakarma, “Ultra-Low Power High Stability 8T SRAM for Application in Object Tracking System,” IEEE Access, 2017.

[37] M. Qazi et al., “A 512 kb 8T SRAM macro operating down to 0.57 V with an AC-coupled sense amplifier,” IEEE JSSC, 2011.

[38] H. Jeong et al., “Switching pMOS Sense Amplifier for High Density Low Voltage Single-Ended SRAM,” IEEE TCAS-I, 2015.

[39] D. Patel and M. Sachdev, “0.23-V Sample-Boost-Latch Based Offset Tolerant Sense Amplifier,” IEEE Solid State Circuit Letters, 2018.

[40] I. J. Chang et al., “A Priority-Based 6T/8T Hybrid SRAM Architecture for Aggressive Voltage Scaling in Video Application,” IEEE TCSVT, 2011.

[41] S. Mukhopadhyay et al., “Modeling of Failure Probability and Statistical Design of SRAM Array for Yield Enhancement in Nanoscaled CMOS,” IEEE TCAD, 2005.

[42] G. Pasandi and S. M. Fakhraie, “A 256-kb 9T near-threshold SRAM with 1k cells per bitline and enhanced write and read operations,” IEEE TVLSI, 2015.

[43] A. Garg and T. T. H. Kim, “SRAM Array Structures for Energy Efficiency Enhancement,” IEEE TCAS-II, 2013.

[44] G. Pasandi et al., “Hybrid Cell Assignment and Sizing for Power Area, Delay Product Optimization of SRAM Array,” IEEE TCAS-II, 2019.

[45] A. Sil et al., “A Novel High Write Speed, Low Power, Read-SNM-Free 6T SRAM Cell,” Midwest Symposium on Circuits and Systems, 2008.

[46] Predictive Technology Model (PTM),” Microelectronics Co-design Research Group, Dept. of ECE, University of Minnesota. Available: https://mec.umn.edu/ptm

[47] S. Bansal, and V. K. Tomar, “Design of single ended 9T SRAM cell with improved read performance and expanded write margin for aerospace applications,” Microelectronics Reliability, 178, 115998, 2026.

[48] S. Cai, Z.Huang, W. Shuai, and F. Yu, “A low-power and leakage 14T SRAM cell with multinode upset tolerance for aerospace applications,” Microelectronics Journal, 171, 107107, 2026.

[49] A. Das, A. Bhardwaj, A. Gupta, and G. Raj, “Numerical comparative analysis of 10T-SRAM cells with 6T, 7T, 8T, and 9T using vertical nanowire tunnel FETs. Semiconductors,” 59(5), 427-435, 2025.

[50] A. S. Gaadhe and Y. V. Parkale, “Design of stable and efficient novel 13T differential SRAM cell,” Chip, p. 100171, 2025.

[51] S. U. Haq, E. Abbasian, A. Darabi, I. A. Khan, O. A. Shah, and V. B. Sreenivasulu, “Energy-efficient buffer-based ternary SRAM cell with application to image processing,” IEEE Access, 2025.

[52] S. Sharma and M. Vinodhini, “Implementation of high SNM SRAM cell and testing in 45 nm CMOS logic process,” in Proceedings of the 2024 IEEE International Conference on Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER), pp. 198–202, IEEE, 2024.

[53] V. Singhal, B. Rawat, P. Mittal, and B. Kumar, “A single ended, single port configuration based 9T SRAM cell for stability enhancement,” Physica Scripta, vol. 98, no. 11, p. 115035, 2023.

[54] E. Abbasian and M. Gholipour, “A low-leakage single-bitline 9T SRAM cell with read-disturbance removal and high writability for low-power biomedical applications,” International Journal of Circuit Theory and Applications, vol. 50, no. 5, pp. 1537–1556, 2022..

[55] R. Gupta and S. Dasgupta, “Robust low power transmission gate (TG) based 9T SRAM cell with isolated read and write operation,” International Journal of Electronics, vol. 109, no. 4, pp. 652–668, 2022.

[56] M. Gupta, K. Gupta, and N. Pandey, “A data-independent 9T SRAM cell with enhanced ION/IOFF ratio and RBL voltage swing in near-threshold and sub-threshold region,” International Journal of Circuit Theory and Applications, vol. 49, no. 4, pp. 953–969, 2021.

[57] C. Roy and A. Islam, “Design of low power, variation tolerant single bitline 9T SRAM cell in 16-nm technology in subthreshold region,” Microelectronics Reliability, vol. 120, p. 114126, 2021.

[58] C. Roy and A. Islam, “Characterization of single-ended 9T SRAM cell,” Microsystem Technologies, vol. 26, no. 5, pp. 1591–1604, 2020.

[59] J. K. Mishra, H. Srivastava, P. K. Misra, and M. Goswami, “Analytical modelling and design of 9T SRAM cell with leakage control technique,” Analog Integrated Circuits and Signal Processing, vol. 101, no. 1, pp. 31–43, 2019.

[60] R. Lorenzo and S. Chaudhury, “A novel 9T SRAM architecture for low leakage and high performance,” Analog Integrated Circuits and Signal Processing, vol. 92, no. 2, pp. 315–325, 2017.

[61] B. Rawat and P. Mittal, “A comprehensive analysis of different 7T SRAM topologies to design a bit interleaving enabled and half select free cell for 32 nm technology

node," Proceedings of the Royal Society A, vol. 478, no. 2259, p. 20210745, 2022. DOI: 10.1098/rspa.2021.0745.

[62] B. Rawat and P. Mittal, "Single bit line accessed high-performance ultra-low voltage operating 7T static random access memory cell with improved read stability," International Journal of Circuit Theory and Applications, vol. 49, no. 5, pp. 1435–1449, 2021. DOI: 10.1002/cta.2960.

[63] R. Krishna and P. Duraiswamy, "Low leakage 10T SRAM cell with improved data stability in deep submicron technologies," Analog Integrated Circuits and Signal Processing, vol. 109, pp. 153–163, 2021. DOI: 10.1007/s10470-021-01870-7.

[64] T. G. Sargunam, L. W. Soong, C. M. R. Prabhu, and A. K. Singh, "Design and performance analysis of energy efficient 11T SRAM (E2S11T) cell for high performance and low power applications," in Proceedings of the 2021 IEEE International Workshop of Electronics, Control, Measurement, Signals and their Application to Mechatronics (ECMSM), pp. 1–7, IEEE, 2021. DOI: 10.1109/ECMSM51310.2021.9468835

[65] A. Srivastav, U. Tiwari, S. K. Mandal, and A. Sachdeva, "A FinFET based single bit-line feedback cutting low power 11T SRAM cell for LPWAN applications," AEU–International Journal of Electronics and Communications, p. 155821, 2025

[66] H. Pilo, I. Arsovski, K. Batson, G. Braceras, J. Gabric, R. Houle, and A. Seferagic, "A 64 Mb SRAM in 32 nm high-k metal-gate SOI technology with 0.7 V operation enabled by stability, write-ability and read-ability enhancements," IEEE Journal of Solid-State Circuits, vol. 47, no. 1, pp. 97–106, 2011.

[67] N. P. Bhatta, H. Singh, A. Ghimire, and F. Amsaad, "Analyzing aging effects on SRAM PUFs: Implications for security and reliability," Journal of Hardware and Systems Security, vol. 8, no. 3, pp. 174–186, 2024.

[68] Z. Lin, L. Li, X. Wu, C. Peng, W. Lu, and Q. Zhao, "Half-select disturb-free 10T tunnel FET SRAM cell with improved noise margin and low power consumption," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 7, pp. 2628–2632, 2021.

[69] J. Zhang, Y. He, X. Wu, and B. Zhang, "A disturb-free 10T SRAM cell with high read stability and write ability for ultra-low voltage operations," in Proceedings of the 2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), pp. 305–308, IEEE, 2018.

[70] M. Trivedi, S. Sinha, R. Halli, G. Gurumurthy, J. Singh, C. Y. Cheng, and H. Mair, "15.2 A 350 mV single-rail SRAM using a custom-logic-bitcell in 2 nm CMOS nanosheet technology for mobile and edge-AI applications," in Proceedings of the 2026 IEEE International Solid-State Circuits Conference (ISSCC), vol. 69, pp. 256–258, IEEE, 2026.

[71] C. Dai, J. Zhang, Z. Ren, L. Liu, L. Meng, C. Wang, and X. Wu, "A T8T-SRAM computing-in-memory macro for ternary deep neural networks and Boolean logic

computations," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2026.

[72] V. K. Sharma and A. Kumar, "A novel 8T SRAM cell using PFC and PPC VS-CNTFET transistor," Journal of Engineering and Applied Science, vol. 72, no. 1, p. 5, 2025.

[73] A. Dahiya, P. Mittal, and R. Rohilla, "A low-power half-select free 8T SRAM cell with process-induced variation resistance for voltage scaling at 32 nm technology node," Integration, p. 102586, 2025.

[74] A. Dinesh, Y. Chopra, and P. Mittal, "An 8T SRAM cell for high-speed sub-threshold operation with dynamic body biasing," Integration, p. 102480, 2025..

[75] H. Kim, Y. An, R. Kim, S. Kim, and Y. Shim, "Union SRAM: PVT variation auto-compensated, bit precision configurable current mode 8T SRAM in-memory MAC macro," IEEE Access, vol. 12, pp. 162882–162893, 2024.

[76] R. Lorenzo and R. Paily, "Half-selection disturbance free 8T low leakage SRAM cell," International Journal of Circuit Theory and Applications, vol. 50, no. 5, pp. 1557–1575, 2022.

[77] S. R. Aura, S. M. Huq, and S. N. Biswas, "Design of high-speed dual port 8T SRAM cell with simultaneous and parallel READ-WRITE feature," International Journal of Electrical and Computer Engineering Systems, vol. 13, no. 9, pp. 823–829, 2022.

[78] C. Duari, S. Birla, and A. K. Singh, "A 4 × 4 8T-SRAM array with single-ended read and differential write scheme for low voltage applications," Semiconductor Science and Technology, vol. 36, no. 6, p. 065013, 2021.

[79] C. Duari and S. Birla, "Low leakage SRAM cell with improved stability for IoT applications," Procedia Computer Science, vol. 171, pp. 1469–1478, 2020.

[80] C. Roy and A. Islam, "Design of differential TG based 8T SRAM cell for ultra-low-power applications," Microsystem Technologies, vol. 26, no. 10, pp. 3299–3310, 2020.

[81] A. Jaiswal, I. Chakraborty, A. Agrawal, and K. Roy, "8T SRAM cell as a multibit dot-product engine for beyond von Neumann computing," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 11, pp. 2556–2567, 2019.

[82] C. B. Kushwah and S. K. Vishvakarma, "A single-ended with dynamic feedback control 8T subthreshold SRAM cell," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 1, pp. 373–377, 2015.

[83] S. Pal and A. Islam, "Variation tolerant differential 8T SRAM cell for ultralow power applications," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, no. 4, pp. 549–558, 2015.

[84] L. Wen, Z. Li, and Y. Li, "Differential-read 8T SRAM cell with tunable access and pull-down transistors," Electronics Letters, vol. 48, no. 20, pp. 1260–1261, 2012.

[85] M. F. Chang, J. J. Wu, K. T. Chen, Y. C. Chen, Y. H. Chen, R. Lee, and H. Yamauchi, "A differential data-aware power-supplied (D^2AP) 8T SRAM cell with expanded

write/read stabilities for lower VDDmin applications," IEEE Journal of Solid-State Circuits, vol. 45, no. 6, pp. 1234–1245, 2010.

[86] A. Islam and M. Hasan, "Variability aware low leakage reliable SRAM cell design technique," Microelectronics Reliability, vol. 52, no. 6, pp. 1247–1252, 2012.

[87] G. Pasandi and S.M. Fakhraie, "An 8T low-voltage and low-leakage half selection disturb-free SRAM using bulk-CMOS and FinFETs," IEEE transactions on Electron Devices, 61 (7), 2357-2363, 2014.

[88] A. Agarwal et al., "Process variation in embedded memories: Failure analysis and variation aware architecture," IEEE Journal of Solid-State Circuits (JSSC), 2005.

[89] Y. Wang et al., "A unified aging model of NBTI and HCI degradation towards lifetime reliability management for nanoscale MOSFET circuits," in Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures, 2011.

[90] S. Pal and A. Islam, "9T SRAM cell for reliable ultralow power applications and solving multi-bit soft error issue," IEEE Transactions on Device and Material Reliability, 2016.

[91] M. L. Fan et al., "Variability analysis of sense amplifier for FinFET subthreshold SRAM applications," IEEE Transactions on Circuits and Systems II (TCAS-II), 2022.

[92] T. Na et al., "Comparative study of various latch-type sense amplifiers," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013.

[93] R. C. Baumann, "Soft errors in commercial integrated circuits," International Journal on High Speed Electronics and Systems, 2004.

[94] Y. W. Chiu et al., "40 nm bit-interleaving 12T subthreshold SRAM with data-aware write-assist," IEEE Transactions on Circuits and Systems I (TCAS-I), 2014.

[95] A. Sachdeva and V. K. Tomar, "Design of low power half select free 10T static random access memory cell," Journal of Circuits, Systems and Computers, 2021.

[96] D. Kishore, S. Chakraborty, A. Biswas, and A. Dumka, "Circuit-level leakage reduction techniques in CMOS sense amplifiers for SRAM and TCAM: A review," Analog Integrated Circuits and Signal Processing, vol. 126, no. 2, p. 37, 2026.

[97] R. G. B. Sangalang, A. K. G. Manalo, J. B. L. Dalisay, and R. N. M. Macasaet, "A 200 MHz 1.22 fJ/bit/search single-ended content addressable memory cell design in 45-nm CMOS technology," International Journal of Electronics, vol. 113, no. 1, pp. 39–64, 2026.

[98] E. Hassan, K. S. Hassan, S. Elshahaby, and B. Mohammad, "Reconfigurable in-memory computing using standard 6T SRAM for BCAM, TCAM, similarity indexing, and logic-in-memory operations," Authorea Preprints, 2025.

[99] Z. Zhang, Z. Chen, J. Wang, G. Xie, and G. Liu, "Reconfigurable 10T SRAM for energy-efficient CAM operation and in-memory computing," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 33, no. 4, pp. 1065–1072, 2025..

[100] V. Himaja, V. Madhupriya, T. Subhavana, and V. Preethi, “High-performance triple-level hybrid cache design using TCAM in VLSI systems,” International Journal of Communication Networks and Information Security, vol. 17, no. 4, pp. 237–243, 2025.

[101] F. Wei, X. Cui, S. Zhang, and X. Zhang, “An 11T SRAM cell for the dual-direction in-array logic/CAM operations,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no. 4, pp. 2329–2333, 2023.

[102] K. Pan, A. M. Tosson, N. Wang, N. Y. Zhou, and L. Wei, “A novel cascadable TCAM using RRAM and current race scheme for high-speed energy-efficient applications,” IEEE Transactions on Nanotechnology, vol. 22, pp. 214–221, 2023.

[103] C. Padmini, T. Laxmi, S. Sreeja, and V. Anusha, “An energy efficient TCAM for secure transmission in wireless communications,” in Proceedings of the EAI International Conference on Intelligent Systems with Applications in Communications, Computing and IoT, pp. 182–193, Springer Nature Switzerland, 2024.

[104] M. Irfan, A. I. Sanka, Z. Ullah, and R. C. Cheung, “Reconfigurable content-addressable memory (CAM) on FPGAs: A tutorial and survey,” Future Generation Computer Systems, vol. 128, pp. 451–465, 2022.

[105] A. Gangadhar and K. Babulu, “Design of low-power and high-speed CNTFET-based TCAM cell for future generation networks,” The Journal of Supercomputing, vol. 77, no. 9, pp. 10012–10022, 2021.

[106] I. Ullah, J. S. Yang, and J. Chung, “ER-TCAM: A soft-error-resilient SRAM-based ternary content-addressable memory for FPGAs,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 4, pp. 1084–1088, 2020.

[107] J. Koo, E. Kim, S. Yoo, T. Kim, S. Ryu, and J. J. Kim, “Configurable BCAM/TCAM based on 6T SRAM bit cell and enhanced match line clamping,” in Proceedings of the 2019 IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 223–226, IEEE, 2019.

[108] R. Karam, R. Puri, S. Ghosh, and S. Bhunia, “Emerging trends in design and applications of memory-based computing and content-addressable memories,” Proceedings of the IEEE, vol. 103, no. 8, pp. 1311–1330, 2015.

[109] S. Jeloka, N. Akesh, D. Sylvester, and D. Blaauw, “A configurable TCAM/BCAM/SRAM using 28 nm push-rule 6T bit cell,” in Proceedings of the 2015 Symposium on VLSI Circuits (VLSI Circuits), pp. C272–C273, IEEE, 2015.

[110] K. Pagiamtzis and A. Sheikholeslami, “Content-addressable memory (CAM) circuits and architectures: A tutorial and survey,” IEEE Journal of Solid-State Circuits, vol. 41, no. 3, pp. 712–727, 2006.

[111] J. Y. Hsieh and S. J. Ruan, “Synthesis and design of parameter extractors for low-power pre-computation-based content-addressable memory using gate-block selection algorithm,” in Proceedings of the 2008 Asia and South Pacific Design Automation Conference, pp. 316–321, IEEE, 2008.

[112] K. Pagiamtzis, N. Azizi, and F. N. Najm, “A soft-error tolerant content-addressable memory (CAM) using an error-correcting-match scheme,” in Proceedings of the IEEE Custom Integrated Circuits Conference 2006, pp. 301–304, IEEE, 2006..

[113] J. P. Wade and C. G. Sodini, “A ternary content addressable search engine,” IEEE Journal of Solid-State Circuits, vol. 24, no. 4, pp. 1003–1013, 2002.

[114] A. Garg and T. T. H. Kim, “SRAM array structures for energy efficiency enhancement,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 6, pp. 351–355, 2013.

[115] M. H. Fuad and M. F. Nayan, “Impact of material and structural parameters on the performance of advanced low-power CNTFET-based SRAM designs,” Scientific Reports, 2026.

[116] S. J. Kidwai, N. Alam, and B. Iqbal, “A 12 transistor robust SRAM cell design for aerospace applications,” International Journal of Electronics, pp. 1–16, 2025.

[117] P. K. Patel, M. M. Malik, and T. K. Gupta, “Reliable single-ended ultra-low power GNRFETs-based 9T SRAM cell with improved read and write operations,” Microelectronics Reliability, vol. 153, p. 115321, 2024.

[118] A. Mema, S. Thomann, N. S. Dhakad, and H. Amrouch, “First demonstration of 28 nm fabricated FeFET-based nonvolatile 6T SRAM,” arXiv Preprint arXiv:2603.26439, 2026.

[119] M. E. Sinangil, Y. T. Lin, H. J. Liao, and J. Chang, “A 290 mV, 7 nm ultra-low-voltage one-port SRAM compiler design using a 12T write contention and read upset free bit-cell,” IEEE Journal of Solid-State Circuits, vol. 54, no. 4, pp. 1152–1160, 2019.

[120] M. Naeem and K. Bai-Sun, “10T SRAM using half-VDD precharge and row-wise dynamically powered read port for low switching power and ultralow RBL leakage,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 4, pp. 1193–1203, 2016.

[121] K. Gavaskar and U. S. Ragupathy, “Low power self-controllable voltage level and low swing logic based 11T SRAM cell for high speed CMOS circuits,” Analog Integrated Circuits and Signal Processing, vol. 100, pp. 61–77, 2019.

[122] T. W. Oh, H. Jeong, K. Kang, J. Park, Y. Yang, and S. O. Jung, “Power-gated 9T SRAM cell for low-energy operation,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 3, pp. 1183–1187, 2017.

[123] C. Y. Lu, C. T. Chuang, S. J. Jou, M. H. Tu, Y. P. Wu, C. P. Huang, P. S. Kan, H. S. Huang, K. D. Lee, and Y. S. Kao, “A 0.325 V, 600 kHz, 40 nm 72 kb 9T subthreshold SRAM with aligned boosted write wordline and negative write bitline write-assist,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 5, pp. 958–962, 2014.

[124] K. Nii, Y. Tsukamoto, M. Yabuuchi, Y. Masuda, S. Imaoka, K. Usui, S. Ohbayashi, H. Makino, and H. Shinohara, “Synchronous ultra-high-density 2RW dual-port 8T-SRAM

with circumvention of simultaneous common-row-access," IEEE Journal of Solid-State Circuits, vol. 44, no. 3, pp. 977–986, 2009.

[125] F. H. Mahamudul, M. F. Nayan, N. S. Shahrier, Y. Rahbaar, and R. R. Mahmud, "Comprehensive performance analysis of CMOS and CNTFET based 8T SRAM cell," *Journal of Electronic Science and Technology*, p. 100306, 2025.

[126] H. Zhou and L. Wang, "A review of two methods to enhance SRAM performance and power consumption," in *Proceedings of the Third International Conference on Algorithms, Network, and Communication Technology (ICANCT 2024)*, vol. 13545, pp. 66–72, SPIE, 2025.

[127] M. Elangovan, N. Padmaja, S. J. Basha, M. A. El-Meligy, and H. A. Mahmoud, "A FinFET-based low-power, stable 8T SRAM cell with high yield," *AEU–International Journal of Electronics and Communications*, vol. 175, p. 155102, 2024.

[128] R. R. Kumar, V. Sharma, A. K. Jain, S. Goyal, and P. Das, "Performance analysis of 6T SRAM cell and 8T SRAM cell techniques using 18 nm FinFET technology," in *Proceedings of the 2024 4th International Conference on Innovative Practices in Technology and Management (ICIPTM)*, pp. 1–4, IEEE, 2024.

[129] I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches," in *Proceedings of the 30th European Solid-State Circuits Conference*, pp. 215–218, 2004.

[130] N. Surana and J. Mekie, "Energy efficient single-ended 6T SRAM for multimedia applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 6, pp. 1023–1027, 2018.

[131] S. Ahmad, B. Iqbal, N. Alam, and M. Hasan, "Low leakage fully half-select-free robust SRAM cells with BTI reliability analysis," *IEEE Transactions on Device and Materials Reliability*, vol. 18, no. 3, pp. 337–349, 2018.

[132] S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, "Single-ended Schmitt-trigger-based robust low-power SRAM cell," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 8, pp. 2634–2642, 2016.

[133] A. P. Kumar and R. Lorenzo, "A low power static noise margin enhanced reliable 8T SRAM cell," *Microsystem Technologies*, vol. 30, no. 6, pp. 729–738, 2024.

[134] N. Mathur and S. Birla, "Designing and performance analysis of 7T CNTFET based novel SRAM cell for IoT application," *Engineering Research Express*, vol. 6, no. 1, p. 015408, 2024.

[135] N. Verma and A. P. Chandrakasan, "256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 141–149, 2008.

[136] A. Valluri and S. Musala, "Low leakage, differential read scheme CNTFET based 9T SRAM cells for low power applications," *International Journal of Electronics*, vol. 111, no. 1, pp. 127–148, 2024.

[137] Y. Yang, H. Jeong, S. C. Song, J. Wang, G. Yeap, and S.-O. Jung, "Single bit-line 7T SRAM cell for near-threshold voltage operation with enhanced performance and energy in 14 nm FinFET technology," *IEEE Transactions on Circuits and Systems I*, vol. 63, no. 7, pp. 1023–1032, 2016. DOI: 10.1109/TCSI.2016.2556118.

[138] S. A. Tawfik and V. Kursun, "Low power and robust 7T dual-Vt SRAM circuit," in 2008 IEEE International Symposium on Circuits and Systems (ISCAS), Seattle, WA, USA: IEEE, May 2008, pp. 1452–1455. doi: 10.1109/ISCAS.2008.4541702.

[139] K. Gavaskar, M. S. Narayanan, M. S. Nachammal, and K. Vignesh, "Design and comparative analysis of SRAM array using low leakage controlled transistor technique with improved delay," J Ambient Intell Human Comput, vol. 13, no. 9, pp. 4559–4568, Sept. 2022, doi: 10.1007/s12652-021-03353-z.

[140] D. Nayak, D. P. Acharya, and K. K. Mahapatra, "Power efficient design of a novel SRAM cell with higher write ability," in 2015 Annual IEEE India Conference (INDICON), New Delhi, India: IEEE, Dec. 2015, pp. 1–6. doi: 10.1109/INDICON.2015.7443739

[141] .S. Lin, Y.-B. Kim, and F. Lombardi, "Design and analysis of a 32 nm PVT tolerant CMOS SRAM cell for low leakage and high stability," Integration, vol. 43, no. 2, pp. 176–187, Apr. 2010, doi: 10.1016/j.vlsi.2010.01.003.

[142] M. Ali, A. Jaiswal, S. Kodge, A. Agrawal, I. Chakraborty, and K. Roy, "IMAC: In-Memory Multi-Bit Multiplication and ACcumulation in 6T SRAM Array," IEEE Trans. Circuits Syst. I, vol. 67, no. 8, pp. 2521–2531, Aug. 2020, doi: 10.1109/TCSI.2020.2981901.

[143] A. Garg and T. T.-H. Kim, "SRAM Array Structures for Energy Efficiency Enhancement," IEEE Trans. Circuits Syst. II, vol. 60, no. 6, pp. 351–355, June 2013, doi: 10.1109/TCSII.2013.2258247.

[144] R. J. Evans and P. D. Franzon, "Energy consumption modeling and optimization for SRAM's," IEEE J. Solid-State Circuits, vol. 30, no. 5, pp. 571–579, May 1995, doi: 10.1109/4.384170.

[145] X. Xue et al., "Design and Performance Analysis of 32 × 32 Memory Array SRAM for Low-Power Applications," Electronics, vol. 12, no. 4, p. 834, Feb. 2023, doi: 10.3390/electronics12040834

[146] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 24, no. 12, pp. 1859–1880, 2005. DOI: 10.1109/TCAD.2005.852295.

[147] A. T. Elthakeb, T. Haine, D. Flandre, Y. Ismail, H. A. Elhamid, and D. Bol, "Analysis and optimization for dynamic read stability in 28 nm SRAM bitcells," in Proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, pp. 1414–1417, IEEE, 2015. DOI: 10.1109/ISCAS.2015.7168908.

[148] E. I. Vatajelu, A. Gómez-Pau, M. Renovell, and J. Figueras, “Transient Noise Failures in SRAM Cells: Dynamic Noise Margin Metric,” in 2011 Asian Test Symposium, New Delhi, India: IEEE, Nov. 2011, pp. 413–418. doi: 10.1109/ATS.2011.64.

[149] Ruchi and S. Dasgupta, “6T SRAM cell analysis for DRV and read stability,” J. Semicond., vol. 38, no. 2, p. 025001, Feb. 2017, doi: 10.1088/1674-4926/38/2/025001.

[150] T. S. Kumar and S. L. Tripathi, “Process evaluation in FinFET based 7T SRAM cell,” Analog Integr Circ Sig Process, vol. 109, no. 3, pp. 545–551, Dec. 2021, doi: 10.1007/s10470-021-01938-4.

[151] J. Wang, S. Nalam, and B. H. Calhoun, “Analyzing static and dynamic write margin for nanometer SRAMs,” in Proceeding of the thirteenth international symposium on Low power electronics and design - ISLPED ’08, Bangalore, India: ACM Press, p. 129, 2008. doi: 10.1145/1393921.1393954.

[152] W. Gul, M. Shams, and D. Al-Khalili, “SRAM Cell Design Challenges in Modern Deep Sub-Micron Technologies: An Overview,” Micromachines, vol. 13, no. 8, p. 1332, Aug. 2022, doi: 10.3390/mi13081332.

[153] B. Madiwalar and B. S. Kariyappa, “Single bit-line 7T SRAM cell for low power and high SNM,” in 2013 International Mutli-Conference on Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), Kottayam: IEEE, pp. 223–228, Mar. 2013. doi: 10.1109/iMac4s.2013.6526412.

[154] B. Jena, S. Dash, and G. P. Mishra, “Improved Switching Speed of a CMOS Inverter Using Work-Function Modulation Engineering,” IEEE Trans. Electron Devices, vol. 65, no. 6, pp. 2422–2429, June 2018, doi: 10.1109/TED.2018.2827083.

[155] G. Torrens, B. Alorda, C. Carmona, D. Malagon-Perianez, J. Segura, and S. Bota, “A 65-nm Reliable 6T CMOS SRAM Cell with Minimum Size Transistors,” IEEE Trans. Emerg. Topics Comput., vol. 7, no. 3, pp. 447–455, July 2019, doi: 10.1109/TETC.2017.2721932.

[156] A. Tripathi, A. Dahiya, and P. Mittal, “A low-power single ended half-select free 7 T SRAM cell with improved write margin at 32 nm technology node,” Phys. Scr., vol. 100, no. 1, p. 015015, Jan. 2025, doi: 10.1088/1402-4896/ad96f3.

[157] M. Qazi, M. Sinangil, and A. Chandrakasan, “Challenges and Directions for Low-Voltage SRAM,” IEEE Des. Test. Comput., vol. 28, no. 1, pp. 32–43, Jan. 2011, doi: 10.1109/MDT.2010.115.

[158] S. O. Toh, Z. Guo, T. J. K. Liu, and B. Nikolic, “Characterization of dynamic SRAM stability in 45 nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 46, no. 11, pp. 2702–2712, 2011. DOI: 10.1109/JSSC.2011.2164300

[159] B. H. Calhoun and A. P. Chandrakasan, “Static noise margin variation for subthreshold SRAM in 65 nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 41, no. 7, pp. 1673–1679, 2006. DOI: 10.1109/JSSC.2006.873215

[160] B. Yang and L. Kim, “A low-power SRAM using hierarchical bit line and local sense amplifiers,” IEEE Journal of Solid-State Circuits, vol. 40, no. 6, pp. 1366–1376, 2005. DOI: 10.1109/JSSC.2005.848032.

[161] H. Kim, Y. An, R. Kim, S. Kim, and Y. Shim, “Union SRAM: PVT variation auto-compensated, bit precision configurable current mode 8T SRAM in-memory MAC macro,” IEEE Access, 2024. DOI: 10.1109/ACCESS.2024.3487975

[162] P. Ghasem and S. M. Fakhraie, “An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs,” IEEE Transactions on Electron Devices, vol. 61, no. 7, pp. 2357–2363, 2014. DOI: 10.1109/TED.2014.2321295.

[163] M. Kumar and J. S. Ubhi, “Design and analysis of CNTFET based 10T SRAM for high performance at nanoscale,” International Journal of Circuit Theory and Applications, vol. 47, no. 11, pp. 1775–1785, 2019. DOI: 10.1002/cta.2696

[164] J. Singh, S. P. Mohanty, and D. K. Pradhan, Robust SRAM Designs and Analysis. New York: Springer, 2013.

[165] S. ul Haq, E. Abbasian, I. A. Khan, O. A. Shah, A. Balodi, M. Tolani, and V. B. Sreenivasulu, “A CNTFET-based 10T static memory design immune to read and half-select disturbs for low-power wearable biomedical systems,” IEEE Access, 2025.

LIST OF PUBLICATIONS

SCI/SCIE Indexed Journal Papers Published

1. Yogita Chopra, and Poornima Mittal, "Design of Dual Port 9T SRAM cell with Parallel Processing and High Performance Computing", **Physica Scripta**, IoP Sciences, Vol. 99, pp. 095015 (2024) **(I.F.: 2.6),** DOI: https://iopsciences.iop.org/journal/1402-4896.
2. Yogita Chopra, and Poornima Mittal. "An energy-efficient 11T SRAM cell architecture with write-assist mechanism at sub threshold voltage for biomedical applications", **Physica Scripta,** IoP Sciences, Vol. 101, No. 2, pp. 025003 (2026) **(I.F.: 2.6),** DOI 10.1088/1402-4896/ae32d0

SCI/SCIE Indexed Journal Papers: Revision submitted (01)

1. Yogita Chopra, and Poornima Mittal, "A Robust 8T SRAM cell Provided with Read-Assist Path for Improved Stability and Temperature Variation Tolerance," communicated in **Sadhana engineering journal** (Springer); **IF: 1.4** (**Revision submitted on 14th June, 2025**)

Paper Under-Process for Submission in SCI/SCIE International Journal

1. Yogita Chopra, and Poornima Mittal, "Differential Single – Ended Power Gated 8T SRAM cell for Ultra-Low Voltage Applications: Improved Write Margin and Temperature Variation Tolerance," communicated in **Arabian Journal of science and Engineering** (Springer); **IF: 1.98**
2. Yogita Chopra, and Poornima Mittal, "Content Addressable Memory (CAM) Searching Block using Sub-Threshold Low Power SRAM Cell with Advanced Simulations," submitted in **Microelectronics** (Elsevier); **IF: 1.4**
3. Yogita Chopra, and Poornima Mittal, "Design and Performance Evaluation of an Alternate 8T–9T SRAM-Based Hybrid TCAM for Energy-Efficient Associative Computing," submitted in **Integration- the VLSI Journal** (Elsevier); **IF: 1.6**

Scopus Indexed International Conference Papers

1. Yogita Chopra, and Poornima Mittal, "A Descriptive Analysis of Different Dual Port and Single Port 11T SRAM cells for Low Voltage Operations," 2nd International Conference on

Women Researchers in Electronics and Computing (WREC'23)" organized by NIT, Jalandhar (Springer) from 21st - 23rd April, 2023 (Springer, Scopus Indexed).

2. Yogita Chopra, and Poornima Mittal, "A Single Bit line 8T SRAM Bit with Robust read, Hold Stability and Low Power," 4th International Conference on Data Science and Applications (ICDSA 2023), organized by MNIT, Jaipur from 14th - 15th July, 2023 (Springer, Scopus Indexed).
3. Yogita Chopra, and Poornima Mittal, "Single port 8T-SE SRAM bit cell optimized for low power consumption and temperature variation stability," International conference on Intelligent Computing and Communication Techniques (ICCICT 2024), 28th – 29th, June, 2024 (Taylor and Francis).

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PAPER

Design of dual port 9T SRAM cell with parallel processing and high performance computing

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Keywords: static noise margin, SRAM cell, power delay product, Monte carlo, leakage current

Abstract

To meet industry requirements of higher transistor count SRAM cells this paper is proposing, a nine-transistor configuration static random access memory (SRAM) cell which is accessible by dual bit line and performing simultaneous read and write operations. The suggested 9T (P9T PS) cell is constructed at 32 nm CMOS and is operating at an operating voltage 0.9 V. To justify the refined performance of proposed design various analysis are carried out that shows the static noise margins (SNM) that occurs while executing the read operation is 0.368 V and hold operation by the cell is 0.364 V, while the write operation has an SNM of 0.422 V. The access time for write and read functions of the cell is found to be 1.2 nS and 4.5 nS respectively. The P9T PS SRAM is compared with other dual-port and single-port 9T SRAM cells is stand out to be pre-eminence in performance in terms of noise immunity, temperature variations, power consumption (static and dynamic both), power delay product (PDP), SNM to PDP and area ratio (SAPR) and electric quality matric. Total leakage power for P9T PS cell is found to be 22.1 nW. The P9T PS bit cell is also found to be power efficient as it is consuming minimal power for all of the operations. Area layout of the P9T (PS) is found to be 22.372 μm^2. The results are also supported by the process corner variation analysis for four different corners. LT-spice software is used to carry out all the simulations and analysis.

1. Introduction

The need for longer battery life and to reduce bit cell power consumption has emerged as a key design consideration. The most popular way to lower the amount of electricity that a cell uses is to decrease VDD [1] at which the cell is operating. But there are some considerations that come when the VDD is reduced below a certain level these are the variation in process voltage temperature (PVT) of the deep sub micrometre regions [2]. To measure the total power being used by an SRAM cell, is static power consumed is calculated as the cell commonly executes in the hold mode [3]. The major drawback of reducing the VDD is that it lowers operation of the memory along with a marginally larger increment in the value of the bit error rate (BER) [4]. So, to design digital circuits with improved performance is a huge task for designers as they have to consider the VDD that operates in the range near to the saturation voltage [5, 6]. The need for longer battery life [7] and to reduce bit cell power consumption [8, 9] has emerged as a key design consideration. The most popular way to lower the amount of electricity that a cell uses is to decrease VDD [10, 11] at which the cell is operating. But there are some considerations that come when the VDD is reduced below a certain level these are the variation in process voltage temperature (PVT) of the deep sub micrometre regions [12].To measure the total power being used by an SRAM cell, is static power consumed is calculated as the cell commonly executes in the hold mode [13]. The major drawback of reducing the VDD is that it lowers operation of the memory along with a marginally larger increment in the value of the bit error rate (BER) [14]. So, to design digital circuits with improved performance is a huge task for designers as they have to consider the VDD that operates in the range near to the saturation voltage [15, 16].

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An energy-efficient 11T SRAM cell architecture with write-assist mechanism at sub threshold voltage for biomedical applications

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Keywords: 11 T SRAM cell, power delay product, low power, dynamic power, access delay

Abstract

The proposed 11T (P11T) cell is constructed using the 32 nm technology node at a low voltage of 500 mV. The read and hold operations had static noise margins (SNMs) of 184 mV and 197.26 mV, respectively, but the write operation displayed SNMs of 265 mV. The write and read access times of the cell were determined to be 16.24 ps and 11.38 ps, respectively. Additionally, the performance under 3σ global variance was evaluated using Monte Carlo analysis with a sample size of 5000. The P11T bit cell's low power consumption during all operations was another notable feature. For a sample size of 5000, Monte Carlo simulations showed stability improvements during read and hold procedures. Additionally, dynamic power consumption for read and write operations of the cell was minimal compared to other SRAM cells. All simulations and analyses were conducted using LT-spice software. The bit cell occupies an area of 3.228 μm2. Comparatively, read power for the pre—existing 7T1,7T2, 9T1, 9T2, 10T1, 10T2, 11T1, 11T2 and 11T3 cells is 24.3 μW, 27.6 μW, 28.2 μW, 27.4 μW, 34.6 μW, 29.64 μW, 14.2 μW, 16.8 μW, and 26.9 μW respectively, and write power for the pre—existing 7T1,7T2, 9T1, 9T2, 10T1, 10T2, 11T1, 11T2, and 11T3 cells is 2.6 μW, 5.4 μW, 4.2 μW, 5.2 μW, 6.4 μW, 7.2 μW, 4.1 μW, 6.2 μW, and 7.4 μW respectively and the read and write power of the proposed 11 T cell is found to be 18.26 μW and 5.32 μW, respectively.

1. Introduction

The demand for low-area, portable devices with high processing capabilities has led designers to integrate System-on-Chip (SoC) technology with aspects of the Internet of Things (IoT) and machine learning [1, 2]. Incorporating SoC with artificial intelligence and machine learning makes devices more desirable and reliable. The popularity of IoT has increased the processing load on SoC processors, necessitating the use of cache memory internally for faster application execution [3]. Advancements in the industry are moving towards nanometer technology feature sizes to accommodate sleek designs with remarkably high battery life [4]. Additionally, in accordance with Moore's Law, feature sizes of ultra large-scale integration (ULSI) nanoelectronic devices are being marginally reduced [5]. However, reducing the operating voltage (VDD) of SRAM cells to minimize power consumption presents challenges such as variations in process voltage temperature (PVT) in deep submicrometer regions [1, 6].

Static power consumption during hold mode is a vital component for measuring the total power consumption of a cell [7]. Nonetheless, lowering VDD can impact memory operation and potentially increase the bit error rate (BER) [8, 9]. Balancing power consumption with performance and reliability remains a significant concern for designers in the development of SRAM cells for modern devices. In order to maximize the chip's cell density, the cells need also be built with a minimum number of transistors. On the other hand, process variance increases as transistor size decreases. Process variability is caused by variations in doping, oxide thickness, and channel length. The short-channel impact causes such that scaling also results in an exponential rise in leakage power. As a result, scaling process raises an idle SRAM block's power consumption. By lowering the

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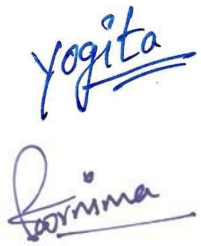

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OBJECTIVE

I aim to secure a full-time academic role that allows me to contribute meaningfully to research and development in science and technology.

TEACHING EXPERIENCE

SN	Institute Name	Designation	Mode	Duration
1.	DPG Institute of Technology and Management, Gurugram	Assistant Professor	Full Time	August 2018 to August 2020

EDUCATIONAL QUALIFICATIONS

SN	Course	Institute	Specialization	Duration	Division
1.	PhD.	Delhi Technological University, Delhi	SRAM Cell designing	Pursuing (From August 2020)	**Status:** Thesis submitted
2.	M. Tech.	MDU, Rohtak	Electronics & Communication Engineering	2015-2017	1st
3.	B. Tech.	MDU, Rohtak	Electronics & Communication Engineering	2011-2015	1st
4.	Intermediate	J.J. Public School Gurugram	Physics, Chemistry, Mathematics, Hindi, English	2010-2011	1st
5.	High school	J.J. Public School Gurugram	Hindi, English, Mathematics, Science, Social Science	2008-2009	1st

RESEARCH EXPERIENCE

Ph.D. Research Scholar, DTU Delhi (Pursuing from August 2020)
Supervisor: Prof. Poornima Mittal (DTU Delhi).

- Research topic: Design and analysis of low power SRAM bit cell for content addressable memory application
- Published 02 SCI/SCIE research papers as first author.