DESIGN AND ANALYSIS OF JUNCTIONLESS NANOWIRE FET AND ITS APPLICATIONS

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By

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CANDIDATE'S DECLARATION

I, **Bharti (2K21/PHDEC/506)**, hereby certify that the work which is being presented in the thesis entitled "**Design and Analysis of Junctionless Nanowire FET and its Applications**", in partial fulfilment of the requirements for the award of the Degree of **Doctor of Philosophy**, submitted in the Department of **Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **01st January 2022** to **08th October 2026** under the supervision of **Prof. Poornima Mittal, Professor, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India.** The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

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CERTIFICATE BY THE SUPERVISOR

Certified that **Bharti (2K21/PHDEC/506**) has carried out her research work presented in this thesis entitled **"Design and Analysis of Junctionless Nanowire FET and its Applications",** for the award of **Doctor of Philosophy** from the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student herself, and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.



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ABSTRACT

The continuous scaling of conventional planar Field Effect Transistors (FETs) has led to severe Short Channel Effects (SCEs), increased leakage current (I_{OFF}), and fabrication complexity, thereby necessitating the exploration of alternative device architectures. Among the emerging devices, Junctionless Nanowire Field Effect Transistors (JL-NWFETs) have attracted considerable attention due to their simplified fabrication process, which eliminates the need for abrupt junction formation by employing uniform doping throughout the source-channel-drain. Despite these advantages, conventional JL-NWFETs suffer from several inherent limitations, including reduced ON-state current (I_{ON}), insufficient volume depletion in the OFF-state, degraded carrier mobility due to heavy doping, and increased susceptibility to SCEs such as Drain Induced Barrier Lowering (DIBL) and I_{OFF}. Addressing these challenges is essential for enabling the practical implementation of JL-NWFETs in future nanoscale electronic systems.

This thesis presents a comprehensive analysis focused on improving the performance of conventional JL-NWFETs through advanced device engineering, analytical modeling, and application-oriented design. Initially, an Improved JL-NWFET (I-JL-NWFET) device is proposed by integrating an oppositely doped Core Shell (CS) configuration with a Dual Material Gate (DMG) and Gate Sidewall Spacer (GSS). The CS structure enhances volume depletion and improves electrostatic control, while the DMG introduces a step in the channel potential, reducing electric field peaks and suppressing SCEs. The incorporation of a GSS further improves fringe field control and reduces leakage current. The proposed device is systematically optimized, revealing that for a core thickness (t_{core}) as half of channel thickness (t_{si}) is optimal, with SiO_2 as the gate oxide, HfO_2 as the spacer material, and a spacer length of 25 nm, which is equal to the source/drain length.

The results demonstrate significant improvements in the proposed I-JL-NWFET performance, including 23.1% increase in I_{ON}, along with a five-order reduction in I_{OFF}, resulting in an impressive I_{ON}/I_{OFF} ratio of approximately 10^6, which is six orders of magnitude higher than that of the conventional JL-NWFET. Additionally, an 88% improvement in Subthreshold Slope (SS) is achieved. To further evaluate the proposed I-JL-NWFET reliability and scalability, the effects of channel length (L_C) scaling, t_{si} variation, and temperature fluctuations on electrical, analog/RF, and linearity performance are systematically analyzed. The optimal L_C and t_{si} are found to be 30 nm and 10 nm, respectively. The variation in drain current (I_{DS}) with temperature

(200 K to 500 K) is limited to 29% in the I-JL-NWFET compared to 31.8% in the JL-NWFET, while SS and DIBL are reduced by 29% and 28%, respectively.

Moreover, performance degradation with temperature is significantly mitigated, with transconductance (g_m) decreasing by 24.4% (compared to 26.7% in JL-NWFET), early voltage (V_{EA}) reducing by 32.9% (compared to 52.72%), and cut-off frequency (f_T) decreasing by only 19.9% (compared to 45.2%). The proposed I-JL-NWFET exhibits reduced sensitivity to scaling and temperature variations, ensuring stable operation under varying conditions. Additionally, linearity metrics such as higher-order transconductance coefficients (g_{m2}) and intermodulation distortion parameters indicate superior behavior at elevated temperatures, making the device suitable for high-frequency and analog applications. Specifically, the peak value of g_{m2} is reduced by 2.53%, 5.45%, 10.74%, and 11.67% at 200 K, 300 K, 400 K, and 500 K, respectively, confirming improved linearity at higher temperatures.

To gain deeper insight into the underlying device physics, initially, two physics-based analytical models are developed for the intermediate I-JL-NWFET architectures, the first device incorporating CS with DMG and the second incorporating device CS with GSS, before analysing the final proposed I-JL-NWFET that integrates CS, DMG, and GSS. These models are formulated by solving the two-dimensional Poisson's equation using appropriate boundary conditions and incorporating the effects of fringe capacitance and spacer permittivity. The analytical models accurately predict important device parameters such as surface potential distribution, electric field profile, threshold voltage (V_T), I_{DS}, I_{OFF}, SS, and DIBL. A strong agreement between analytical and numerical simulation results validates the accuracy and reliability of the proposed models. Furthermore, the models provide valuable insights into the influence of device parameters such as core doping concentration, spacer material, and geometrical scaling, thereby serving as effective design tools for device optimization at nanoscale dimensions.

The scope of this work is further extended to biomedical application circuit-level analysis to establish the practical applicability of the proposed device. A novel biosensor based on the I-JL-NWFET is proposed for the detection of the p53 biomarker associated with Gastrointestinal (GI) cancer. The sensing mechanism is based on the interface charge deduction method within a nanocavity region, enabling label-free and real-time detection. The optimization analysis reveals that the highest sensitivity is achieved when the nanocavity is positioned near the source side of the channel, while the optimum cavity length (L_{cav}) is found to be half of the L_C. Under the optimized device configuration, for a p53 concentration of 1.62 ng/ml corresponding to the

maximum diseased condition, the biosensor achieves an I_{ON}/I_{OFF} sensitivity of 4.60 × 10^9, V_T sensitivity of 0.69, and SS sensitivity of 0.78.

For a p53 concentration of 0.27 ng/ml corresponding to the maximum healthy condition, the device exhibits an I_{ON}/I_{OFF} sensitivity of 2.15 × 10^7, V_T sensitivity of 0.49, and SS sensitivity of 0.88. These results confirm the strong discriminatory capability of the proposed biosensor in effectively distinguishing healthy and diseased states over clinically relevant biomarker concentrations. Further, the influence of structural and environmental parameters, including L_C, t_{core}, temperature, and biomolecule occupancy, is systematically investigated. The analysis demonstrates that the biosensor retains appreciable sensitivity even at shorter L_C, indicating its suitability for highly scaled nanowire biosensor applications.

The temperature analysis confirms robust sensing behaviour over a wide operating temperature range, while the cavity occupancy study shows that maximum sensitivity is achieved at 100% cavity occupancy, emphasizing the importance of complete biomolecular binding within the sensing region. In addition, the incorporation of Repulsive Steric Hindrance (RSH) effects provides a more realistic assessment of biosensor performance by accounting for steric limitations and practical binding constraints, thereby bridging the gap between idealized simulation and practical operation. Moreover, the successful integration of the proposed biosensor with Common Source Amplifier (CSA) read-out circuitry validates its ability to transform biomolecule-induced current variations into detectable voltage signals appropriate for practical sensing applications. The results confirm the suitability of the proposed device for reliable and ultra-sensitive biosensing applications.

Beyond biomedical applications, this thesis also explores the potential of the proposed I-JL-NWFETs circuit-level analysis to establish the practical applicability in electronic applications. A comparative investigation is carried out among the two proposed device structures, device D1 incorporating CS, DMG, and GSS, and device D2 incorporating CS, DMG, along with previously reported architectures, device D3 and D4 based on CS + SMG and the conventional JL-NWFET, respectively. Their n- type and p-type configurations are named as N1, N2, N3, and N4, and p-type devices P1, P2, P3, and P4, respectively. The proposed N1 device demonstrates the minimum I_{OFF} of 9.55 × 10^{-9} μA, indicating highly effective leakage suppression and stronger electrostatic control achieved through the cumulative benefits of CS, DMG, and GSS. Although N2 provides the smallest intrinsic delay (τ) of 1.40 ps due to the absence of GSS architecture, the τ observed in N1 remains very close at 1.43 ps, while still offering considerably lower leakage compared with the existing structures, N3 and N4.

The static performance analysis of the CMOS inverter shows that Inv1, implemented using N1 and P1, achieves the highest noise margins (NM_L = 0.515 V and NM_H = 0.355 V) with improved switching reliability and enhanced static stability. In addition, Inv1 exhibits superior thermal robustness, as reflected by the lowest positive temperature coefficient of propagation delay (τ_P) of 3.96 × 10^{-3} K^{-1} among all considered configurations. However, the presence of GSS in Inv1 introduces additional fringing capacitance, which slightly increases the τ_P of 11.25 ps, average power dissipation (P_{avg}) of 42.70 μW, Power Delay Product (PDP) of 480.87 aJ, and Energy Dealy Product (EDP) of 5404.10 × 10^{-30} Js compared with Inv2 which exhibits corresponding values of 10.85 ps, 40.61 μW, 440.61 aJ, and 4780.61 × 10^{-30} Js, respectively. Nevertheless, both proposed inverter structures (Inv1 and Inv2) continue to outperform the previously reported inverter configurations, Inv3 and Inv4.

The 3-stage Ring Oscillator (RO) analysis demonstrates stable oscillation behavior in the gigahertz range for all proposed configurations of R1, R2, R3, and R4, realized using Inv1, Inv2, Inv3, and Inv4, respectively. Although R2 attains the highest oscillation frequency (f_{osc}) of 15.36 GHz because of its lower τ_P, R1 delivers more reliable overall performance. R1 exhibits the shortest warm-up time of 76.52 ps and the lowest jitter of 0.001 ps, confirming faster startup response and improved frequency stability. Moreover, temperature-dependent analysis shows that R1 possesses the smallest negative temperature coefficient of τ_P of −2.84 × 10^{-3} K^{-1} and the minimum temperature rise of 12.23 K, highlighting its superior thermal stability during high-frequency operation compared to R2, R3, and R4. The supply voltage investigation further indicates that oscillations cannot be sustained at 0.5 V for any configuration. An analytical investigation for Inv1 further reveals that increasing t_{core} results in larger τ_P and reduced f_{osc}, while reducing the t_{core} enhances switching speed and oscillator performance. The analysis identifies t_{core} = 5 nm as the optimum design condition for achieving the best compromise between τ_P and f_{osc}.

At last, this thesis presents a unified framework that combines device innovation, analytical modeling, biosensing applications, and circuit implementation of the proposed I-JL-NWFETs. This research work establishes that the I-JL-NWFET incorporating CS, DMG, and GSS is highly suitable for biomedical sensing applications, whereas the I-JL-NWFET with CS and DMG without GSS offers a better trade-off for high-speed and energy-efficient digital electronics. The outcomes of this research provide valuable guidelines for the design and development of next-generation low-power, high-performance nanoelectronics devices and open new avenues for their integration into advanced sensing platforms.

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List of Abbreviations and Symbols

Abbreviation/Symbol	Full Form
ALD	Atomic Layer Deposition
BJT	Bipolar Junction Transistor
BSA	Bovine Serum Albumin
BHF	Buffered Hydrofluoric Acid
CLM	Channel Length Modulation
COLSA	CO2 Laser Spike Annealing
CSA	Common Source Amplifier
CMOS	Complementary MOS
CT	Computed Tomography
CB	Conduction Band
CS	Core-Shell
DG	Double Gate
DSG	Double Surrounding Gate
DIBL	Drain- Induced Barrier Lowering
DMG	Dual Material Gate
EDP	Energy Delay Product
EOT	Equivalent Oxide Thickness
FE	Ferroelectric
GI	Gastrointestinal
GAA	Gate All Around
GME	Gate Material Engineering
GSS	Gate Sidewall Spacer
GS	Gate Stacked
GC	Graded Channel
HCEs	Hot Carrier Effects
HF	Hydrofluoric Acid
I-JL-NWFET	Improved JL-NWFET
ITCs	Interface Trap Charges
IUPAC	International Union of Pure and Applied Chemistry
JL-NWFETs	Junctionless Nanowire Field Effect Transistors
L-BTBT	Lateral Band-to-Band tunneling
MRI	Magnetic Resonance Imaging
MOSFETs	Metal Oxide Field Effect Transistors
MWA	Microwave Annealing
MLD	Molecular Monolayer Doping
MW	Molecular Weight
NWFETs	Nanowire Field Effect Transistors
PET	Positron Emission Tomography
PDP	Power Delay Product

RDFs	Random Dopant Fluctuations
RIE	Reactive Ion Etching
RE	Recessed
RSE	Repulsive Steric Effect
RSH	Repulsive Steric Hindrance
RO	Ring Oscillator
SHE	Self-Heating Effect
S_E	Sensitivity Error
SCEs	Short Channel Effects
SOI	Silicon-On-Insulator
SMG	Single Material Gate
SPC	Solid Phase Crystallization
S/D	Source/Drain
S.D	Standard Deviation
SE	Steric Effect
SH	Steric Hindrance
SS	subthreshold slope
VSP	Switching Point Voltage
TCAD	Technology Computer-Aided Design
IIP3	Third-order Input Intercept Point
IMD3	Third-order Intermodulation Distortion,
TGF	Transconductance Generation Factor
TMG	Triple Material Gate
VB	Valance Band
VIP2, VIP3	Voltage Intercept Points
VTC	Voltage Transfer Characteristics
ZTC	Zero Temperature Coefficient
ZTC	Zero Temperature Coefficient
ZCP	Zero-Crossover Point
T	Absolute temperature
Al_2O_3	Aluminium oxide
$T_{ambient}$	Ambient temperature
P_{avg}	Average power dissipation
E_g	Bandgap
K	Boltzmann constant,
L_{cav}	Cavity length
$\phi_C(z)$	Central potential
L_C	Channel length
t_{si}	Channel thickness
t_{core}	Core thickness
f_T	Cutoff frequency
C_{dep}	Depletion capacitance
I_{DS}	Drain current

V_{DS}	Drain voltage
V_{EA}	Early voltage
g_c	Effective density of states for electrons
g_v	Effective density of states for holes
E_C	Electric field
m_o	Electron's rest mass
V_{fb}'	Flat-band voltage
t_{ox}	Gate oxide thickness
V_{GS}	Gate voltage
Au	Gold
HfO_2	Hafnium dioxide
NM_H	High-level noise margin
τ_{PHL}	High-to-low output transition delay
n_i	Intrinsic carrier concentration
τ	Intrinsic delay
pI	Isoelectric point
I_{OFF}	Leakage current or OFF-state current
I_{lin}	Linear region drain current
C_L	Load capacitance
μ_e	Low field electron mobility
μ_p	Low field hole mobility
NM_L	Low-level noise margin
τ_{PLH}	Low-to-high output transition delay
T_{max}	Maximum lattice temperature
$Conc._{p53}$	Molar concentration of p53
Mo	Molybdenum
I_{ON}	ON-state current
f_{osc}	Oscillation frequency
f_{osc}	Oscillation frequency
g_d	Output conductance
k	Permittivity or dielectric constant
τ_P	Propagation delay
λ	Represents the scaling length
L_S/L_D	S/D length
I_{sat}	Saturation region drain current
t_{shell}	Shell thickness
SiC	Silicon carbide
I_{Dsub}	Subthreshold current
$\phi_S(z)$	Surface potential
I_{ON}/I_{OFF}	Switching ratio
Ta_2O_5	Tantalum pentoxide
ΔT	Temperature rise

V_T	Threshold voltage
C_{GG}	Total gate capacitance
g_m	Transconductance
m_e	Tunneling mass of electrons
m_h	Tunneling mass of holes

CHAPTER-1

INTRODUCTION

1.1 OVERVIEW OF THE CHAPTER

The continuous evolution of semiconductor technology and the increasing demand for compact, high-speed, and low-power electronic systems have accelerated the transition from conventional planar Metal Oxide Field Effect Transistors (MOSFETs) toward advanced nanoscale transistor architectures. As device dimensions are aggressively scaled, planar FETs suffer from severe Short Channel Effects (SCEs), increased leakage current, threshold voltage degradation, and poor electrostatic gate control, thereby limiting their suitability for future nanoelectronics applications. To address these limitations, cylindrical Nanowire Field Effect Transistors (NWFETs) have emerged as promising alternatives due to their superior gate controllability, excellent carrier confinement, and enhanced scalability. Junctionless Nanowire Field Effect Transistors (JL-NWFETs) have gained significant attention because of their simplified fabrication process, reduced junction formation complexity, improved electrostatic integrity, and low-power operation.

In recent years, extensive research has been carried out to improve the performance of JL-NWFETs through structural engineering approaches for achieving better performance suitable for next-generation integrated circuits and biosensing platforms. Despite these advancements, several performance limitations and design challenges still remain in existing JL-NWFET architectures, particularly in terms of Lateral Band-to-Band tunneling (L-BTBT) during the OFF-state. Recent studies indicate that structural modification techniques can significantly enhance the device-level performance of JL-NWFETs. Furthermore, the increasing demand for highly sensitive biomedical sensors and energy-efficient nanoelectronics systems necessitates the development of advanced JL-NWFET architectures with enhanced electrical and sensing characteristics. Therefore, the present research work focuses on the device-level design and analysis of structurally improved JL-NWFET architectures to achieve enhanced electrostatic integrity, improved electrical performance, and superior sensing capability for future nanoscale electronic applications.

This chapter is systematically arranged into seven sections, starting with an overview of this chapter in Section 1.1. The evolution to the cylindrical FET is presented in Section 1.2. Further, the concept of JL-NWFETs, including the evolution of cylindrical FET structures, working

principle, important device parameters, and their potential applications in modern nanoelectronics systems, are explained in Section 1.3. Thereafter, in Section 1.4, a comprehensive literature review covering various structural enhancement techniques for JL-NWFETs, analytical modeling approaches, biomedical sensing applications, digital circuit implementations, and reliability analyses is discussed. The research gaps are identified in Section 1.5, and the problem statement is formulated in Section 1.6. Subsequently, Section 1.7 outlines the objectives of the proposed research work, while Section 1.8 describes objective-wise methodologies adopted to achieve the intended research objectives. Section 1.9 comprises the thesis organization, providing a brief description of each chapter included in this research work. At last, the summary of the chapter is presented in Section 1.10

1.2 EVOLUTION OF CYLINDRICAL FET

Aggressive scaling of MOSFETs has opened new challenges for advanced nanoelectronics applications that demand superior electrostatic integrity, low power consumption, high integration density, and fabrication feasibility at deeply scaled technology nodes. However, the performance of conventional inversion-mode MOSFETs is increasingly constrained by severe SCEs, dopant-induced variability, and the technological difficulty of forming abrupt Source/Drain (S/D) junctions as the device dimensions approach the sub-nm regime [1].

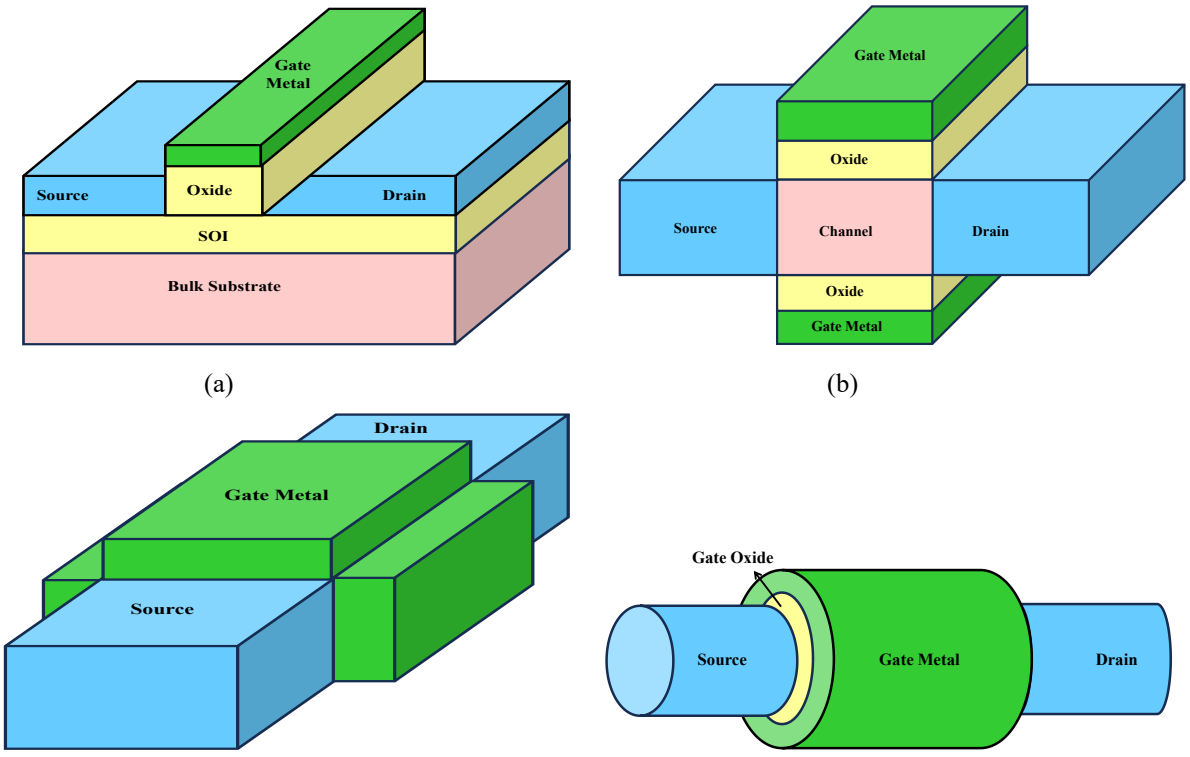


Fig. 1.1 Basic structure of (a) SOI MOSFET, (b) DGFET, (c) FINFET, and (d) Nanowire FET

To overcome these limitations, multi-gate architectures such as Silicon-On-Insulator (SOI) MOSFET [2], Double Gate (DG) FETs [3], FinFETs [4], and cylindrical Nanowire FET (NWFET) [5]. Fig. 1.1 represents the evolution from SOI MOSFET to DGFET, FinFET, and finally to NWFET. Among these architectures, NWFETs are highly promising for extending Complementary MOS (CMOS) scaling due to their excellent gate controllability and enhanced channel confinement [6].

Semiconductor NWFET have been widely studied as nanoscale building blocks for nanoelectronics since they can function as both devices and wires that access the devices. NWFETs are used in various fields of endeavors such as biomedical sensors, biochemical sensors, optical components, fluid mechanics, telecommunication, electronics, power, etc. due to their excellent sensitivity, low cost, and real-time. When analytic molecules bind to a specific recognition molecule at the surface of the nanowire results in excellent sensitivity detection which is attached to their smaller size, and large surface-to-volume ratio, enabling local charge transfer which in turn changes the current due to field effect [7]. NWFET also serve as fundamental building blocks in electronic circuits. They can be used to create high-performance transistors due to their small size and excellent electrical properties. NWFETs can be incorporated into logic gates and digital circuits, enabling the development of smaller and more energy-efficient electronic devices.

1.3 JUNCTIONLESS NANOWIRE FET

Recent advances in semiconductor technology provide the means to explore alternative methods for fabricating transistors, aiming to further reduce their size to increase transistor density and enhance performance. The conventional NWFET uses semiconductor junctions formed by doping atoms into the silicon substrate, creating p-type and n-type regions [8]. The basic structure of NWFET in 3-D and 2-D is portrayed in Fig. 1.2 (a) and (b), respectively, illustrating channel length (L_C), channel thickness (t_{si}), gate oxide thickness (t_{ox}), and S/D length (L_S/L_D). Decreasing the size of such transistors means the junctions will get closer, which becomes very challenging at the lower end of the nanometer scale due to the requirement for extremely high doping concentration gradients [9].

One of the most promising solutions to overcome this issue is JL-NWFET device. The first cylindrical junctionless device was proposed and fabricated in 2013 [10]. Unlike conventional NWFETs, JL-NWFETs do not have a p-n or n-p junction between the source and drain regions, thereby making the fabrication process easier and the device more scalable at lower technology nodes. The 3-D structure of the JL-NWFET is similar to that of the NWFET, as shown in Fig.

1.2 (a). However, the 2-D cross-sectional view of JL-NWFET, depicted in Fig. 1.2 (c), illustrates the uniform n-type doping throughout source, channel, and drain compared to the 2-D view of NWFET in Fig. 1.2 (b), having intrinsic p-type doping in the channel region.

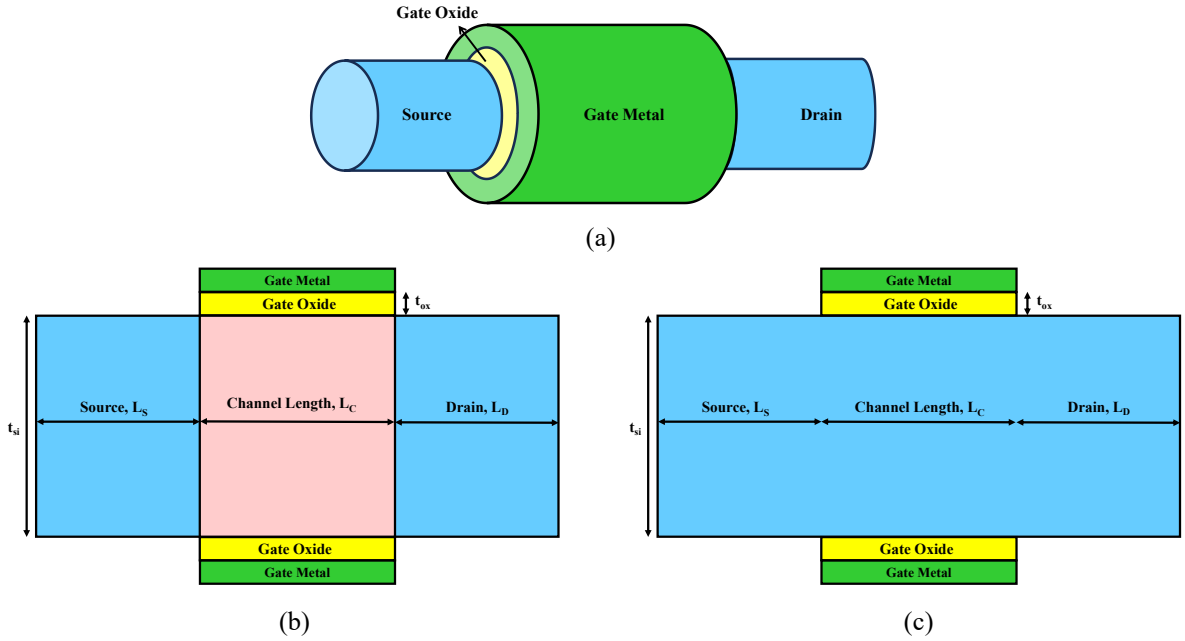


Fig. 1.2 (a) 3-D structure of NWFET and JL-NWFET, (b) 2-D view of NWFET, and (c) 2-D view of JL-NWFET

Due to the absence of a traditional junction, JL-NWFETs can be fabricated using simpler manufacturing processes than traditional FETs. This simplicity can potentially reduce production costs. The operating mechanism of a JL-NWFET differs fundamentally from that of a conventional inversion-mode MOSFET. In a junctionless architecture, the source, channel, and drain are uniformly doped with the same conductivity type, eliminating the formation of p-n junctions and suppressing inversion-layer conduction. As a result, device switching is primarily governed by electrostatic carrier depletion controlled by the gate work-function difference rather than by surface inversion.

1.3.1 Working Principle of JL-NWFET

The conventional JL-NWFET operates in three distinct operating modes, namely, full depletion mode, partial depletion mode, and flat band mode, as illustrated through the 2-D view in Fig. 1.3 (a), (b), and (c), respectively. Unlike conventional inversion-mode NWFET, the JL-NWFET consists of a uniformly and heavily doped semiconductor body extending continuously from source to drain. Since no conventional p-n junctions are present, current transport is governed by the electrostatic depletion and restoration of carriers within the channel

under the influence of the gate electric field. When the gate voltage (V_{GS}) is sufficiently low, the majority carriers are completely depleted from the channel region.

Under this condition, the channel becomes devoid of mobile charge carriers and the device operates in the full-depletion mode, resulting in a very small drain current. As V_{GS} increases, the minimum gate voltage at which a conducting channel starts forming in the middle of the channel is defined as the threshold voltage (V_T). At this point, the device enters the partial-depletion mode, where a reduced carrier concentration remains in the nanowire core and a conductive path begins to develop.

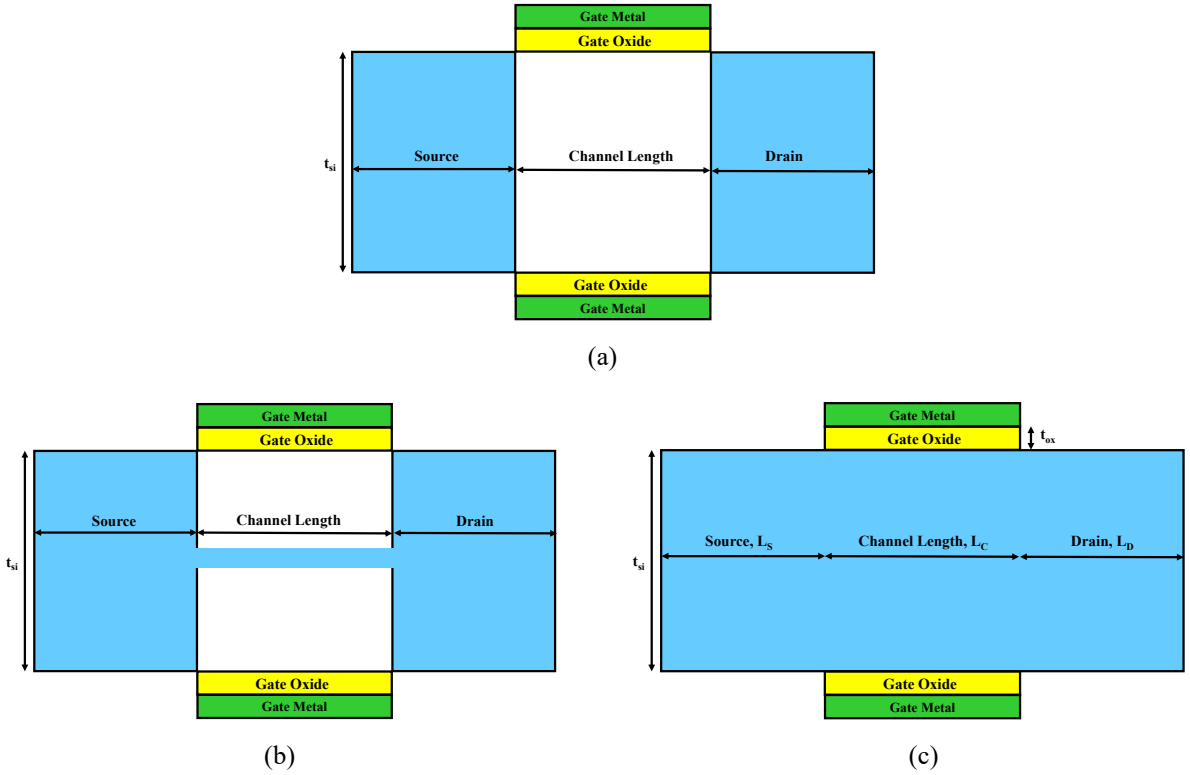


Fig. 1.3 Working mechanism of JL-NWFET in (a) full depletion mode, (b) partial depletion mode, and (c) flat band mode

With further increase in V_{GS}, the flat-band condition is reached, corresponding to minimal band bending and maximum carrier density within the channel. Consequently, a low-resistance conduction path is established between source and drain, enabling strong current conduction [9].

1.3.2 Characteristics parameters of JL-NWFET

The applicability of JL-NWFET for nanoscale applications is determined by means of performance parameters, which are discussed as follows

a. Threshold Voltage (V_T)

The threshold voltage (V_T) of JL-NWFET is the minimum gate voltage at which a conducting channel starts forming at the center of the channel region [9]. It marks the transition of the device from full depletion mode to partial depletion mode.

b. Drain current (I_{DS})

The drain current (I_{DS}) is the output current flowing from drain to source under the influence of applied V_{GS}. It is also called the ON-state current (I_{ON}) at $V_{GS} = V_{DS}$ (drain voltage) [9].

c. Leakage current (I_{OFF})

The leakage current is the drain current flowing in the full depletion mode when the JL-NWFET is in the OFF-state, generally at 0 V_{GS}. Consequently, it is also known as OFF-state current (I_{OFF}). A low leakage current is essential for reducing static power dissipation and improving energy efficiency in low-power applications.

d. I_{ON}/I_{OFF} ratio

The I_{ON}/I_{OFF} ratio is known as the switching ratio as it indicates how effectively the JL-NWFET can switch between its OFF-state and ON-state and vice-versa. A higher ratio is required for JL-NWFET which indicates better switching performance and improved logic operation for digital applications.

e. Transconductance (g_m)

The transconductance (g_m) stands out as a crucial analog metric in assessing devices, as it measures the relationship between the change in current and the variation in V_{GS}. A higher g_m signifies an inherent enhancement in amplification capacity for analog applications. It is defined as the change in drain current with a change in gate voltage. It is formulated as [11]

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \text{ at } V_{DS} = \text{constant} \tag{1.1}$$

f. Subthreshold Slope (SS)

The subthreshold slope (SS) is a measure of how steeply the I_{DS} increases with the V_{GS} in the subthreshold region, representing the device's switching efficiency. It is defined as the change in V_{GS} for every ten-fold increase in I_{DS} and can be expressed as [9]

$$SS = \frac{V_{GS}}{\partial \log_{10}(I_{DS})} \text{ mV/decade} \tag{1.2}$$

It is also one of the critical parameters when analysing the SCEs. A lower value of SS indicates faster switching and stronger gate control over the channel.

g. Drain-Induced Barrier Lowering (DIBL)

The Drain- Induced Barrier Lowering (DIBL) refers to the reduction in the V_T caused by an increase in the V_{DS} [12]. It is also used as a metric to evaluate the SCEs of JL-NWFET. A lower DIBL value indicates better immunity to variation of V_{DS} on channel characteristics and improved electrostatic integrity of the device.

1.3.3 Potential Applications of JL-NWFET

The potential application areas of JL-NWFET are illustrated in Fig. 1.4. JL-NWFETs have attracted considerable attention for a wide range of applications, including low-power electronics, analog/RF circuits, biosensing, memory systems, and flexible electronics. The cylindrical structure of the JL-NWFET provides strong control over channel charge, while the junctionless architecture with uniform doping across the source, channel, and drain regions simplifies fabrication and improves scalability. These features make JL-NWFETs promising candidates for next-generation nanoscale electronic systems. However, despite these advantages, the inherent limitations of conventional JL-NWFETs, such as limited I_{ON}, L-BTBT [13], high I_{OFF}, and various SCEs, can restrict their performance in application-specific environments. Therefore, application-oriented optimization of JL-NWFET in terms of structure, material properties, and geometrical parameters becomes essential.

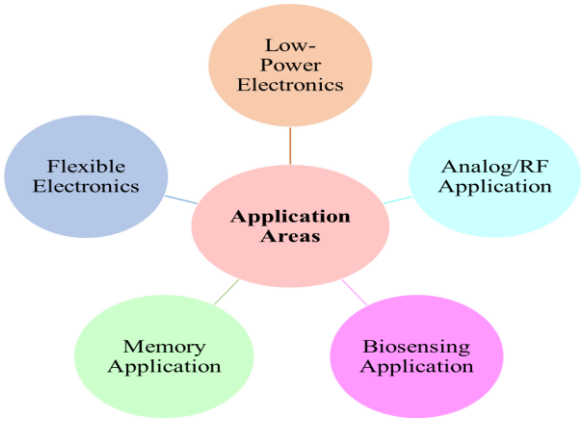


Fig. 1.4 Potential applications of JL-NWFET

For digital and low-power electronic applications, a high I_{ON}/I_{OFF} ratio, low SS, and reduced I_{OFF} are required to achieve efficient switching and low power dissipation. In analog and RF applications, higher g_m, improved output characteristics, and reduced DIBL are desirable for better gain and frequency response. In biosensing applications, low I_{OFF} and high sensitivity

are important for reliable operation, particularly in portable and battery-operated platforms. For memory applications, strong electrostatic control, low standby power consumption, and stable charge retention characteristics are required. Similarly, in flexible electronics, low operating voltage, tolerance to process variations, and energy-efficient operation are important. Hence, structural improvement and performance optimization of JL-NWFETs are necessary to tailor their characteristics according to specific application requirements.

1.4 LITERATURE REVIEW

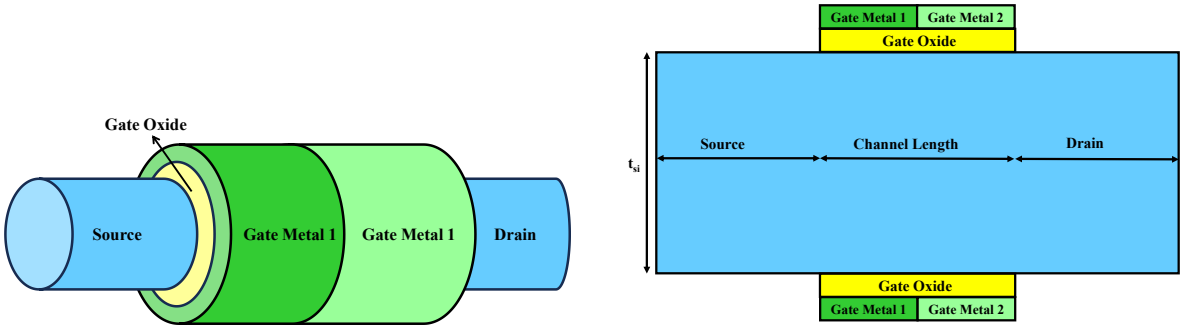
A gradual and noteworthy advancement on the JL-NWFET has been endowed with an advanced device design, especially in the application areas of biomedical and electronics circuits. Over the last few decades, several novel JL-NWFET structures have been proposed to further enhance JL-NWFET device performance and overcome their intrinsic limitations in I_{ON}, V_T tunability, and sensitivity to geometrical variations. These advancements in performance are credited by introducing novel JL-NWFET structures. In this subsection, these novel JL-NWFET are reviewed in terms of their performance parameters, analytical modeling, applications, and reliability.

1.4.1 Structural improvement for JL-NWFET

The device structure in JL-NWFET improves the performance of JL-NWFET. Researchers have proposed different performance enhancement strategies for JL-NWFET in terms of channel, gate material, gate oxide, and the combination of these approaches. Each approach aims to either enhance I_{ON} or reduce I_{OFF}. These structures are discussed in detail in the following sub-sections.

a. Gate Material Engineering (GME) JL-NWFET

The Gate Material Engineering (GME), consist of Dual Material Gate (DMG) [11] and Triple Material Gate (TMG) [14] architectures, has been extensively investigated as an effective structural advancement to overcome low I_{DS} in JL-NWFET. An illustration of DMG JL-NWFET structure in 3-D and 2-D is shown in Fig. 1.5 (a) and (b), respectively. The DMG configuration can be realized through high-dose nitrogen implantation into Molybdenum (*Mo*), forming gate segments with distinct effective work functions [15]. The concept has been further extended to TMG structures, which are fabricated using sequential gate patterning and multiple metal deposition processes [16].



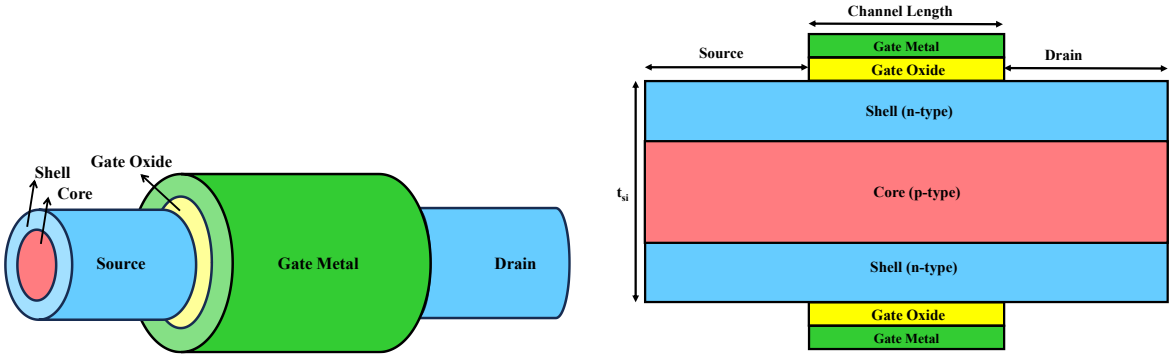
(a) (b)

Fig. 1.5 Structure of Dual Material Gate JL-NWFET in (a) 2-D and (b) 3-D

These GME structures provide enhanced flexibility in electrostatic control while preserving the junctionless nature of the device as compared to the Single Material Gate (SMG).

b. Core-Shell (CS) JL-JL-NWFET

The Core-Shell (CS) JL-NWFET structure whose 3-D and 2-D view is illustrated in Fig. 1.6 (a) and (b), respectively, consists of a central core region within a uniformly doped cylindrical channel. In CS JL-NWFET, the channel is effectively divided the channel into two regions, namely core and shell regions [13, 17]. In conventional JL-NWFET devices, the V_{GS} may not fully deplete carriers in the central region of the nanowire.



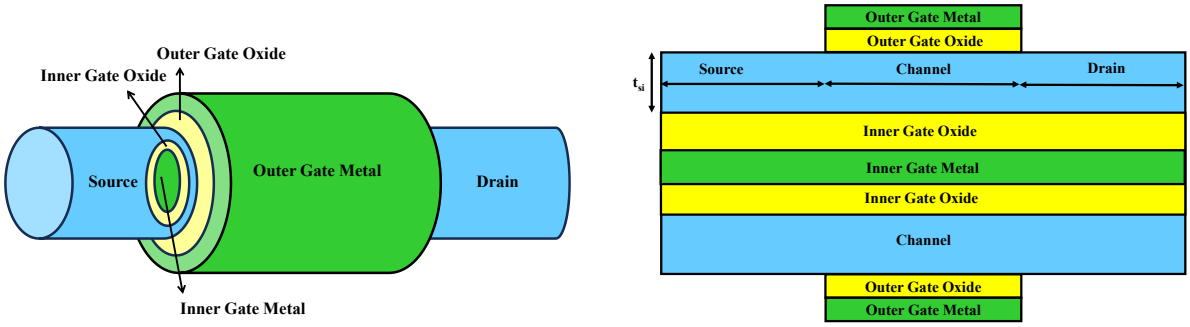
(a) (b)

Fig. 1.6 Structure of Core-Shell JL-NWFET in (a) 2-D and (b) 3-D

The introduction of a core region facilitates improved volume depletion. This structural modification in JL-NWFET increases the source-to-channel potential barrier, thereby reducing the I_{OFF} and enhancing electrostatic gate control. This core can be intrinsic [13], p-type doped [17], or insulating [18]. The feasibility of CS architecture has been demonstrated using a hybrid method incorporating Molecular Monolayer Doping (MLD), Microwave Annealing (MWA), and CO2 Laser Spike Annealing (COLSA) [19].

c. Double Surrounding Gate (DSG) JL-NWFET

The Double Surrounding Gate (DSG) JL-NWFET consists of two concentric cylindrical gates- an inner gate and an outer gate-separated by corresponding inner and outer gate oxide layers [20]. The silicon channel is sandwiched between these oxide layers, forming a coaxial structure that significantly enhances gate coupling. The 3-D and 2-D views of DSG JL-NWFET are presented in Fig. 1.7 (a) and (b), respectively. The presence of the inner gate provides additional electrostatic control over the channel compared to a conventional single surrounding gate structure. This dual-gate configuration ensures efficient depletion of carriers throughout the channel volume, thereby reducing short-channel effects and improving device performance.



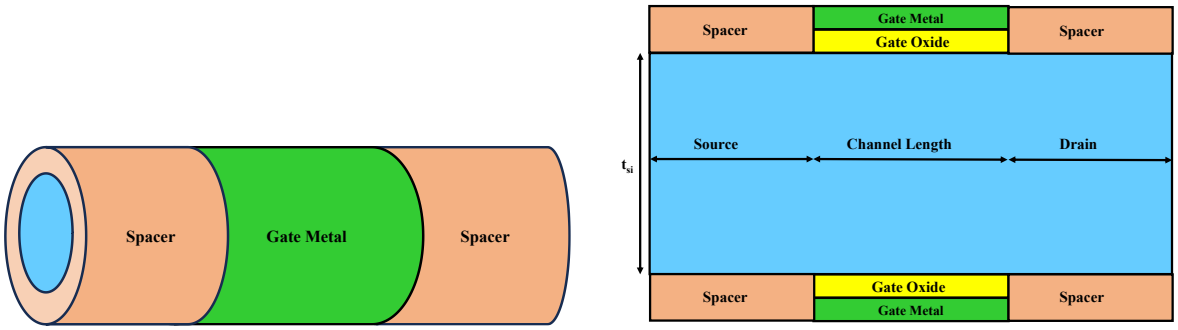
(a) (b)

Fig. 1.7 Structure of Double Surrounding Gate JL-NWFET in (a) 2-D and (b) 3-D

The fabrication feasibility of DSG JL-NWFET devices has been demonstrated by Hanna *et al.* [21].

d. Gate Sidewall Spacer (GSS) JL-NWFET

The Gate Sidewall Spacer (GSS) is an effective technique to enhance electrostatic control in JL-NWFET devices. The incorporation of GSS helps reduce I_{OFF} by enabling fringing electric fields to extend into the ungated regions of the channel, assisting in carrier depletion [22].



(a) (b)

Fig. 1.8 Structure of Gateside Wall Spacer JL-NWFET in (a) 2-D and (b) 3-D

The use of high permittivity (k) material as spacers further intensifies fringing fields, promoting both vertical and lateral depletion of the channel region. This leads to improved suppression of I_{OFF} and enhanced device scalability. The experimental realization of GSS has been achieved using Atomic Layer Deposition (ALD) techniques [23]. The corresponding 3-D and 2-D structures are shown in Fig. 1.8 (a) and (b), respectively.

e. Gate Stacked (GS) JL-NWFET

According to scaling theory, gate oxide thickness must decrease proportionally with channel length. However, aggressive oxide scaling introduces fabrication challenges and increases gate leakage current, thereby exacerbating SCEs. To address these limitations, high-k materials have been introduced as gate insulators. While they reduce I_{OFF}, their relatively low band offsets with silicon and degraded interface quality can lead to increased parasitic effects. To overcome these challenges, a stacked Gate Stacked (GS) structure is proposed whose 3-D and 2-D structure is depicted in Fig. 1.9 (a) and (b), respectively, where a thin Silicon Dioxide (SiO_2) interfacial layer is retained between the silicon channel and the high-k permittivity layer [24].

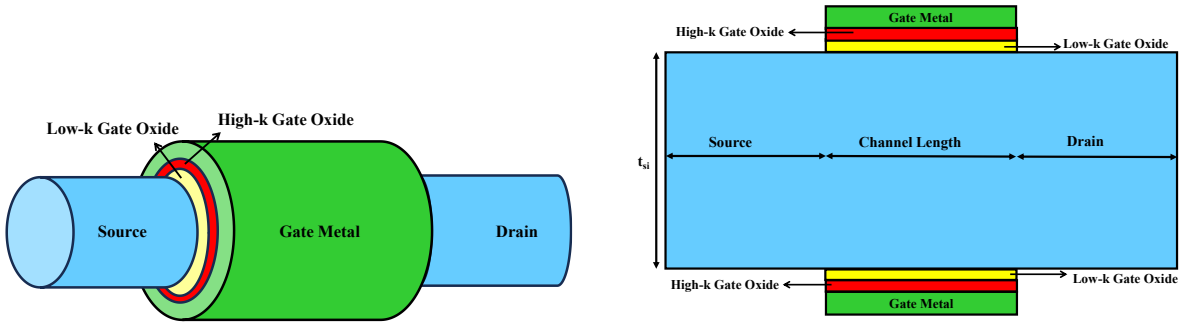


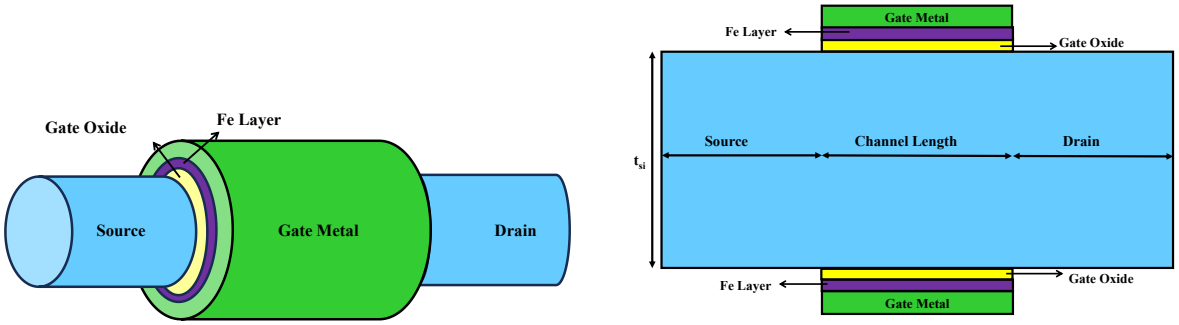
Fig. 1.9 Structure of Gate Stacked JL-NWFET in (a) 2-D and (b) 3-D

The experimental realization of GS architecture is reported in [25]. This configuration preserves interface quality while maintaining a low Equivalent Oxide Thickness (EOT).

f. Ferroelectric (FE) JL-NWFET

In Ferroelectric (FE) JL-NWFET devices, a thin ferroelectric layer is deposited over the conventional gate dielectric [26] as shown in Fig. 1.10 (a) and (b), respectively. Unlike SiO_2 and high-k used as gate oxide material, which exhibit positive capacitance, ferroelectric materials demonstrate negative capacitance behavior. The ferroelectric materials exhibit spontaneous polarization even in the absence of an electric field, and their polarization direction changes under an applied electric field. During polarization switching, the negative

capacitance effect reduces the overall gate capacitance, leading to lower subthreshold swing and reduced leakage current.



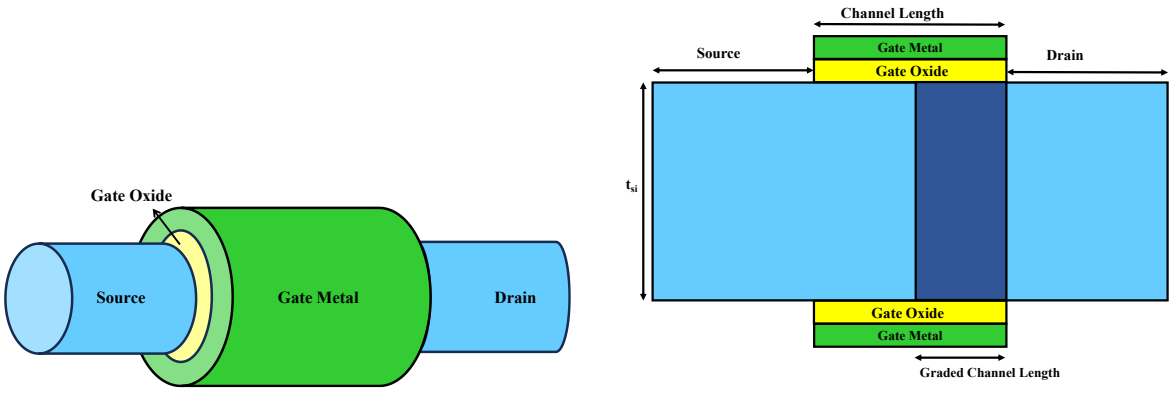
(a) (b)

Fig. 1.10 Structure of Ferroelectric JL-NWFET in (a) 2-D and (b) 3-D

Although Hafnium Dioxide (HfO_2) is conventionally used as a high-*k* gate dielectric, it can exhibit ferroelectric behavior when appropriately doped and processed. The ferroelectric HfO_2-based materials have been reported to be compatible with silicon-based fabrication processes [27].

g. Graded Channel (GC) JL-NWFET

The Graded Channel (GC) JL-NWFET whose 3-D and 2-D view are illustrated in Fig. 1.11 (a) and (b), respectively, incorporates a lateral doping gradient along the channel length. Typically, the channel is divided into two regions: the source-side region with doping similar to the source and the drain-side region with higher doping [28]. The higher doping region is known as graded channel length. This non-uniform doping profile establishes a built-in electric field along the channel, and more importantly, introduces an additional electric field peak at the junction of the two regions.



(a) (b)

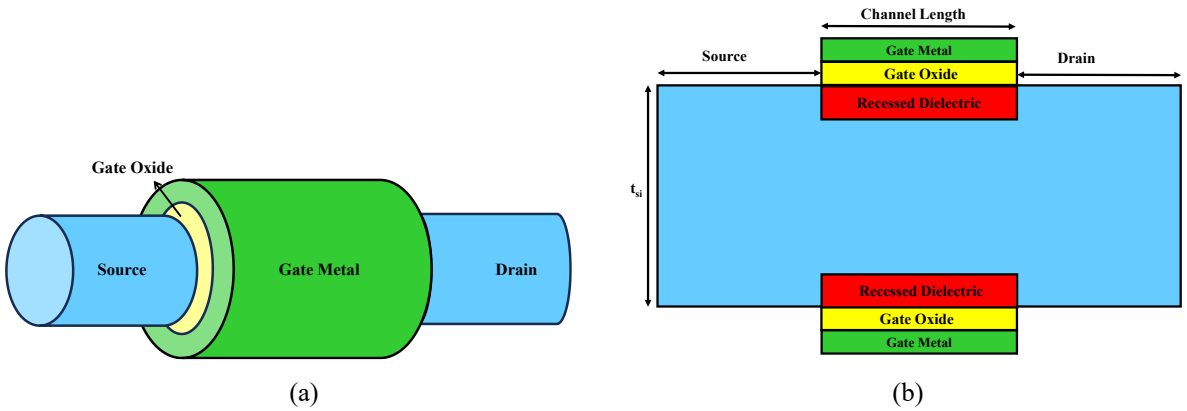
Fig. 1.11 Structure of Graded Channel JL-NWFET in (a) 2-D and (b) 3-D

This field peak accelerates carrier transport, reduces carrier transit time, and suppresses carrier scattering, thereby improving current drivability. As a result, improvements are observed in

drain current, transconductance, and analog/RF performance metrics. From a fabrication perspective, the graded channel can be realized using advanced ion implantation techniques with controlled dose variation to achieve a smooth lateral doping profile [29].

h. Recessed (RE) Source/Drain JL-NWFET

The Recessed (RE) S/D JL-NWFET structure incorporates a recessed dielectric layer beneath the gate oxide in the channel region [30]. The structure of RE JL-NWFET is depicted in Fig. 1.12 (a) and (b), respectively. This modification enhances gate-to-channel coupling and improves electrostatic control over the nanowire. The recessed structure allows the gate electric field to penetrate deeper into the channel, resulting in more uniform carrier depletion in the OFF-state. Additionally, it contributes to reduced effective S/D resistance, thereby improving overall device performance. The fabrication feasibility of RE JL-NWFET structures has been reported in the literature [31].



(a) (b)

Fig. 1.12 Structure of Recessed Source/Drain JL-NWFET in (a) 2-D and (b) 3-D

Table 1.1. Comparison of the electrical parameters of the reported JL-NWFETs

Year	Ref.	Reported JL-NWFET	t_{si} (nm)/ L_C (nm)	I_{ON} (A)	I_{ON}/I_{OFF}	SS (mV/dec)
2012	[11]	DMG	10/40	3.20×10^{-5}	1×10^{3}	64.00
2013	[14]	TMG	10/50	1.60×10^{-5}	-	-
2016	[17]	CS	25/20	1.00×10^{-4}	-	63.00
2016	[20]	DSG	10/30	1.40×10^{-5}	-	68.00
2017	[22]	GSS	10/20	0.80×10^{-5}	1×10^{7}	62.00
2022	[26]	FE	10/20	1.00×10^{-4}	1.7×10^{10}	61.00
2021	[28]	GC	10/30	1.98×10^{-4}	-	-
2023	[30]	RE	10/20	1.15×10^{-5}	4.9×10^{4}	73.63

Table 1.1 presents the performance of reported JL-NWFETs with their reported L_C and t_{si}, over the years has steadily improved with the adoption of advanced device structures. Early designs such as DMG and TMG reported in [11] and [14], respectively, exhibit moderate I_{ON} and

limited performance metrics. With the introduction of CS and GSS structures, significant improvements are achieved in SS and I_{ON}/I_{OFF} ratio, indicating better switching behavior.
The FE-based device reported by Rai *et al*. [26] demonstrates the best overall performance with very high I_{ON} and excellent leakage control. The GC structure reported in [28] achieves the highest I_{ON}, emphasizing the importance of channel engineering. However, Kumar *et al*. [30] reported the RE structure shows relatively degraded SS, suggesting performance trade-offs. Eventually, it is observed that structural innovations enhance device performance, although balancing all parameters remains a challenge.

i. Hybrid JL-NWFET

Many researchers have reported JL-NWFETs that combine two or three basic structural device designs as discussed earlier, to simultaneously enhance electrostatic control and carrier transport. These hybrid approaches aim to overcome the limitations of individual techniques by leveraging their cumulative benefits, resulting in improved performance metrics such as I_{ON}/I_{OFF} ratioand SS. Table 1.2 summarizes the reported hybrid JL-NWFET device structures from recent literature, highlighting their device design and performance improvements. It can be observed that hybrid configurations consistently outperform their single-technique counterparts in terms of switching characteristics and analog/RF performance.

Table 1.2. Comparison of the performance parameters of the reported JL-NWFETs

Year	Ref.	Reported JL-NWFET	t_{si} (nm)/ L_C (nm)	I_{ON} (A)	I_{ON}/I_{OFF}	SS (mV/dec)
2026	[32]	DSG + FE	10/20	-	3.30×10^{5}	67.28
2025	[33]	GSS + GC	10/20	1.00×10^{-5}	1.00×10^{9}	61.00
2025	[34]	FE + RE	10/40	7.61×10^{-6}	6.50×10^{2}	75.62
2025	[35]	GS + FE + RE	10/40	1.66×10^{-6}	2.40×10^{12}	55.99
2024	[36]	DMG + RE	07/30	1.00×10^{-5}	1.00×10^{6}	65.00
2024	[29]	DMG + GC	10/30	1.00×10^{-5}	1.00×10^{7}	68.00
2023	[37]	GS + FE	06/16	7.70×10^{-6}	3.33×10^{5}	72.71
2023	[38]	GS + GC	10/30	1.00×10^{-4}	1.00×10^{10}	61.00
2022	[39]	DSG + GSS + GS	10/20	1.00×10^{-4}	1.00×10^{10}	63.82
2021	[40]	DMG + DSG	10/20	-	2.18×10^{11}	64.32
2021	[41]	DSG + GSS	10/20	-	2.64×10^{11}	64.26
2021	[42]	TMG + DSG	1.50/3.00	1.36×19^{-5}	2.63×10^{9}	59.53
2020	[43]	DMG + GSS + GS	10/30	3.80×10^{-5}	1.60×10^{3}	68.00
2017	[44]	DSG + GSS	10/20	-	1.00×10^{9}	62.60

The performance of JL-NWFET devices, particularly in terms of I_{ON}/I_{OFF} ratio, SS, and electrostatic control, has significantly improved over time through various structural engineering techniques [32]-[44]. Numerous efforts have been reported to enhance these

performance metrics by incorporating different advanced design strategies. Notably, the device reported by Singh *et al*. [35] achieves the highest I_{ON}/I_{OFF} ratio of 2.40×10^{12} along with the lowest SS of 55.99 mV/dec. Moreover, the devices incorporating FE layers consistently show improved SS due to the negative capacitance effect. Additionally, multi-gate and hybrid architectures demonstrate better leakage control and steeper switching characteristics. Consequently, the modern designs outperform earlier ones in terms of efficiency and scalability.

In terms of drive current, higher I_{ON} values are observed in works reported by Mishra *et al*. [38] and Bala *et al*. [39], reaching up to 1.00×10^{-4}, indicating improved current drivability with gate-all-around and multi-gate configurations. However, a higher I_{ON} does not always guarantee a better I_{ON}/I_{OFF} ratio or lower SS, highlighting inherent trade-offs in device design. Earlier works, as reported from 2017 to 2021, mainly utilize DSG, DMG, and GSS combinations, achieving moderate performance with SS around 60 - 65 mV/dec and I_{ON}/I_{OFF} in the range of 10^9 - 10^{11}. Table 1.2 indicates a clear trend toward hybridized device architectures, where combining multiple structural strategies improves performance; however, a trade-off is evident, as designs typically achieve either higher I_{ON} or lower SS, requiring careful optimization to balance both parameters effectively.

1.4.2 Analytical Modeling Strategies of JL-NWFET

The analytical modeling of JL-NWFET devices has evolved from simple Poisson-based formulations for uniformly doped cylindrical structures to understand device electrostatics and derive electrical parameters such as central channel potential (Φ_C), inner channel potential (Φ_i), outer channel potential (Φ_o), channel electric field (E_C), subthreshold current (I_{Dsub}), g_m, V_T, DIBL, I_{DS}, and SS, as conventional equations are not applicable for cylindrical devices. Over the years, various cylindrical structural innovations and modeling strategies have been proposed, primarily based on solving the Poisson equation using either Bessel functions [45, 49, 54, 55, 57, 59] or exponential (1-D) [18, 46-48, 50-53, 56, 58] approaches.

The 1-D Poisson approach assumes that the potential variation is primarily along the channel, leading to an exponential form of the solution. This method offers mathematical simplicity and low computational cost, making it highly suitable for quick estimation of key device parameters. In contrast, the Bessel function-based approach provides a more physically rigorous framework by solving the Poisson equation in cylindrical coordinates, thereby capturing both radial and axial potential variations.

Table 1.3. Comparison of modeling strategies of different existing JL-NWFET

Year	[Ref]	Reported JL-NWFET	Modeling Strategy	Key Parameters derived
2026	[18]	CS + GS	General solution of the 1-D Poisson equation	Φ_C, V_T
2025	[45]	FE	Bessel function solution of the Poisson equation	Φ_C, V_T, SS, I_{DS}
2025	[46]	FE + GS	General solution of the 1-D Poisson equation	Φ_C, V_T, I_{DS}
2023	[47]	CS	General solution of the 1-D Poisson equation	Φ_C, E_C, V_T, I_{Dsub}
2023	[48]	TMG	General solution of the 1-D Poisson equation	V_T, I_{Dsub}, g_m
2022	[49]	GS	Bessel function solution of the Poisson equation	Φ_C, SS
2022	[50]	DMG + GC	General solution of the 1-D Poisson equation	Φ_C, V_T, SS, I_{DS}
2022	[51]	GC	General solution of the 1-D Poisson equation	Φ_C, V_T, I_{Dsub}
2021	[52]	DSG	General solution of the 1-D Poisson equation	Φ_i, Φ_o, V_T, SS, I_{DS}, g_m
2020	[53]	DMG + GS	General solution of the 1-D Poisson equation	Φ_C, V_T, I_{DS}
2016	[54]	DSG	Bessel function solution of the Poisson equation	Φ_i, Φ_o, SS, I_{Dsub}
2016	[55]	DMG-GS	Bessel function solution of the Poisson equation	Φ_C, I_{DS}
2015	[56]	TMG	General solution of the 1-D Poisson equation	Φ_C, E_C, V_T,
2014	[57]	DMG	Bessel function solution of the Poisson equation	Φ_C, I_{Dsub}
2014	[58]	DMG	General solution of the 1-D Poisson equation	Φ_C, V_T
2014	[59]	TMG	Bessel function solution of the Poisson equation	Φ_C, I_{Dsub}

Table 1.3 summarizes the approaches used by the researchers for the various reported JL-NWFETs, which are discussed in subsection 1.1. The majority of the modeling approaches are based on the general solution of the 1-D Poisson equation due to its simplicity and wide applicability. Most reported works focus on deriving the Φ_C, from which the remaining parameters are obtained. Furthermore, the choice of modeling approach depends more on device geometry and analysis requirements rather than structural complexity.

1.4.3 Various Biomedical applications using FET

In biomedical applications, FETs are mainly used for the detection of biomolecules and therefore referred to as biosensors. Their ability to convert biological interactions into measurable electrical signals makes them suitable for early disease diagnosis and real-time monitoring. Table 1.4 presents a comparative overview of different detection approaches, including simulation-based and real-time experimental methods, highlighting the diversity of detectable biomolecules associated with diseases such as cancer, viral infections, and renal disorders. It is observed from Table 1.4 that the simulation-based approaches, such as dielectric modulation and charge deduction, have been widely explored.

The dielectric modulation is being widely applied for detecting a variety of biomolecules, including DNA, proteins, and virus-related markers such as SARS-CoV-2. It is based on the variation in the dielectric constant of biomolecules present in the cavity region; therefore, it is particularly suitable when only the dielectric properties of the biomolecules are known.

Moreover, charge deduction techniques are mainly focused on cancer biomarker detection, including ovarian, breast, and prostate cancer. In this method, detection relies on the charge or concentration difference between healthy and diseased biomolecules, making it suitable when such concentration information is available.

Table 1.4. Comparison of various detection approaches using FET

Year	[Ref]	Detection technique	Biomolecules Detected
2026	[60]	Dielectric Modulation	MCF7-10 A, HS578T, MDA-MD-231, MCF7, and T47D cancer cell line for breast cancer
2024	[61]	Dielectric Modulation	Liver cancer cell line biomolecules for liver cancer
2024	[62]	Dielectric Modulation	Aptes, Gluten, keratin, and Glutin biomolecules
2023	[63]	Charge Deduction	HE4 biomolecules for ovarian cancer
2023	[64]	Charge Deduction	C-erbB-2 biomolecules for breast cancer
2023	[65]	Charge Deduction	PSA biomolecules for prostate cancer
2022	[66]	Dielectric Modulation	DNA, biotin, protein, Aptes biomolecules
2022	[67]	Dielectric Modulation	SARS-CoV-2 biomolecules for COVID-19
2021	[68]	Real-time detection	PSA for prostate cancer
2020	[69]	Real-time detection	NMP22 and CK8 for bladder cancer
2020	[70]	Real-time detection	p53 biomolecules tumour suppressor protein
2019	[71]	Charge Deduction	KIM-I biomolecules for Acute Renal Failure
2018	[72]	Real-time detection	DNA for the hepatitis B virus
2015	[73]	Real-time detection	HE4 biomolecules for ovarian cancer

The experimental real-time detection and simulation-based approaches complement each other in biomolecule detection studies. In 2021, Sajjad *et al.* [73] experimentally demonstrated the detection of HE4 biomolecules for ovarian cancer, which was subsequently analyzed through the Technology Computer-Aided Design (TCAD) simulations by Bhattacharya *et al.* [63] using the charge deduction method. Similarly, Zhang *et al.* [68] experimentally realized a planar FET for PSA biomolecule detection associated with prostate cancer, and this was further supported by Kumar *et al.* [65] in 2023 through TCAD simulations using the same charge deduction method. Together, these experimental validations and simulation studies provide a comprehensive framework for rapid and continuous monitoring of biomarkers, enabling immediate response and dynamic tracking of biological interactions

Table 1.5. Comparison of reported JL-NWFETs for biomolecule detection

Year	[Ref]	Reported JL-NWFET	Biomolecules Detected
2025	[74]	JL-NWFET	Apomyoglobin, Aptes, Glucose oxidas, Gelatin, Gluten, Streptavidin, and Zenin.
2025	[75]	JL-NWFET	Aptes, Keratin, Gelatin, Streptavidin, and Uricase
2025	[76]	TMG + GS	ChOX and Uricase
2025	[77]	GS	Aptes, Ferro-Chrome, Keratin, Streptavidin, Uricase
2024	[78]	JL-NWFET	Aptes, Biotin, Gluten, Keratin, Protein, Streptavidin, and Zein
2024	[79]	TMG	Aptes, Biotin, ChOx, Protein, Streptavidin, Uricase

2023	[80]	DSG	Apomyoglobin, Aptes, Biotin, ChOx, Glucose oxidase, Gelatin, Gluten, Protein, Streptavidin, Uricase, and Zenin.
2022	[81]	TMG + GS	Keratin, Gelatin, Gluten
2021	[82]	DMG	Aptes, Keratin
2021	[83]	DSG	Biotin, DNA, and Hydroprotein
2020	[84]	GS	Aptes, ChOX, Protein, Streptavidin, and Uricase
2019	[85]	DMG	Aptes, Biotin, Protein, and Streptavidin
2018	[86]	JL-NWFET	Aptes, ChOx, Protein, Streptavidin and Uricase
2017	[87]	JL-NWFET	Aptes, Biotin, DNA, Protein, and Streptavidin
2016	[88]	DMG	Aptes, Protein, and Streptavidin

Table 1.5 presents the use of reported JL-NWFET structures for biomolecule detection, showcasing their capability to detect a wide range of proteins, enzymes, and disease markers. It is observed that most reported JL-NWFET-based biosensors are primarily utilized for protein-related biomolecule detection. Additionally, these devices predominantly employ the dielectric modulation method, where sensing is based on variations in the dielectric constant of the target biomolecules. Although JL-NWFETs provide efficient and sensitive detection, their biomedical applicability remains narrower compared to other FET-based approaches, requiring further development to expand their use towards disease-specific diagnostics.

1.4.4 Different digital applications using reported JL-NWFETs

The conventional JL-NWFET compatibility with nanoscale dimensions makes them suitable for implementing high-performance logic circuits. The various device performance improvement designs, such as FE, GME, and GS, etc., are explored to further enhance circuit-level performance. Table 1.6 presents a comparative overview of different reported JL-NWFET structures employed in digital applications, including CMOS inverters, SRAM cells, NAND/NOR gates, and ring oscillators**.**

Table 1.6. Performance comparison of the reported JL-NWFETs for different digital applications

Year	[Ref]	Reported JL-NWFET	Digital applications	Performance parameters
2025	[45]	FE	CMOS Inverter	1. SS = 49 mV/dec 2. V_T = 0.27 V 3. I_{OFF} = 6.2 ×10^5 nA
2025	[89]	JL-NWFET	CMOS Inverter	1. NM_H = 0.5 V, NM_L = 0.4 V 2. V_m = 0.457 V
			6T SRAM	1. RNM = 0.16 V, WNM = 0.45 V 2. HNM = 0.41 V
2025	[90]	JL-NWFET	CMOS Inverter	1. NM_H = 0.37 V, NM_L = 0.36 V 2 τ_P = 6 ps
2024	[91]	JL-NWFET	CMOS Inverter	1. τ_P = 5 ps 2. EDP = 0.31 fJ.ps
			Ring Oscillator	1. t_r = 4 ps 2. t_f = 3.9 ps
2023	[92]	DSG	CMOS Inverter	1. NM_H = 0.43 V, NM_L = 0.46 2. τ_P = 5.6 ns

2023	[93]	FE	CMOS Inverter	1. NM_H = 0.44 V and NM_L= 0.48 2. τ_P = 1.18 ps
			Ring Oscillator	1. f_{osc} = 172.1 GHz
2023	[94]	DMG + GC + GS	CMOS Inverter	1. τ_P = 0.62 ps 2. PDP = 24.75 aJ
			NAND	1. τ_P = 6.03 ps 2. PDP = 240.11 aJ
			NOR	1. τ_P = 6.02 ps 2. PDP = 239.9 aJ
			Ring Oscillator	1. f_{osc} = 23.25 GHz
			6T SRAM	1. RNM = 203.5 mV 2. WNM = 280 mV 3. HNM = 256 mV 4. RAT = 16.10 ps, WAT = 8.10 ps
2022	[95]	TMG + GS + GSS	CMOS Inverter	1. P_{avg} = 4.44 × 10^{-16} W
2021	[40]	DMG + DSG + GSS	CMOS Inverter	1. NM_H = 0. 326 V, NM_L = 0.271 V 2. τ_P = 35 ps.

From the Table 1.6, it is observed that CMOS inverters are the most commonly analyzed digital application across all structures with the performance parameters such as noise margins (NM_H and NM_L), switching voltage (V_m), Energy Delay Product (EDP), Power Delay Product (PDP), propagation delay (τ_P), oscillation frequency (f_{osc}), average power dissipation (P_{avg}), Read Noise Margin (RNM), Write NM (WNM), Hold NM (HNM), Read Access Time (RAT), and Write Access Time (WAT). Furthermore, earlier works from 2021 to 2022 exhibit comparatively higher τ_P and lower performance. Moreover, recent works from 2023 to 2025 show significant performance improvement, particularly in reduced τ_P and enhanced noise margins. Notably, advanced architectures reported in [94] also support multiple circuits such as SRAM, NAND, NOR, and ring oscillators, with better stability. A trade-off is observed between speed and power-related parameters; therefore, careful optimization is required to achieve a balanced device design.

1.4.5 Reliability analysis of JL-NWFET

The temperature variation is a critical factor affecting the performance and reliability of JL-NWFET devices, especially at nanoscale dimensions. The changes in temperature influence carrier mobility, V_T, I_{OFF}, and overall device stability. Various JL-NWFET structures, such as GS, DMG, FE, GC, and RE, are analyzed over a wide temperature range to understand their thermal behavior. Table 1.7 presents a comparative study of reported JL-NWFET highlighting the impact of temperature on the electrical parameters.

From Table 1.7, it is observed that increasing temperature generally degrades device performance across most reported JL-NWFET structures. A common trend is observed in [36, 46] that I_{OFF} increases and a reduction in the I_{ON}/I_{OFF} ratio with increasing temperature. In

several cases reported by Rai *et al.* [26] and Gupta *et al.* [96], g_m and cutoff frequency (f_T) also degrade, indicating reduced high-frequency performance. Additionally, V_T decreases and SS increases with temperature, affecting switching efficiency. However, Kumar *et al.* [30] reported exhibiting minimal noise variation, indicating partial thermal stability.

Table 1.7. Overview of temperature analysis of the reported JL-NWFET

Year	[Ref]	Reported JL-NWFET	Temperature range	Observation
2025	[46]	GS + FE	100 K – 500 K	I_{ON}/I_{OFF} decreases with the increase in temperature.
2025	[36]	DMG + RE	200 K – 500 K	I_{OFF} increases, and I_{ON} decreases with increasing temperature.
2023	[30]	RE	200 K – 500 K	Noise variation is minimal with temperature variation.
2022	[96]	GC	200 K – 500 K	The g_m and f_T are degraded by 6.14%, 0.01%, and when the temperature increases.
2022	[26]	FE	200 K – 400 K	The g_m and f_T degrade with the increase in temperature.
2022	[97]	DSG	200 K – 400 K	The I_{ON} and DIBL are increased by 17.2% and 27.5%, respectively, when the temperature increases.
2021	[98]	GC	300 K – 400 K	The V_T is reduced by 12.3% and the SS is enhanced by 30.6% when the temperature increases.
2015	[99]	DMG	200 K – 500 K	The effect of localized charges decreases with increasing temperature.
2014	[100]	DMG	200 K – 500 K	Interface trap charges change the temperature sensitivity parameter.

The Interface Trap Charges (ITCs) significantly influence the electrical characteristics and reliability of JL-NWFET devices by affecting carrier transport and electrostatic control. These ITCs, present at the oxide-semiconductor interface, can alter V_T, I_{OFF}, and analog/RF performance. The effect of ITCs depends on their polarity (positive or negative) and density. Table 1.8 provides an overview of various reported JL-NWFET structures under different ITC ranges, highlighting their impact on device behavior. The analysis helps in understanding the sensitivity of devices to ITCs and the effectiveness of design techniques in mitigating these effects.

Table 1.8. Comparison of interface trap charges analysis of the reported JL-NWFET

Year	[Ref]	Reported JL-NWFET	ITC range	Observation
2025	[101]	TMG + GS	-5×10^{12} cm^{-2} to 5×10^{12} cm^{-2}	Negative ITCs reduced I_{OFF} by 93.6% and positive ITCs increased it by 1343.5%.

2024	[29]	DMG + GC	-1×10^{13} cm^{-2} to 1×10^{13} cm^{-2}	Analog/RF performance is enhanced under negative ITCs relative to positive ITCs.
2018	[102]	GS	-1×10^{11} cm^{-2} to 1×10^{11} cm^{-2}	The use of ZrTiO4 as high-*k* in GS minimizes the impact of ITCs.
2015	[99]	DMG	-1×10^{16} m^{-2} to 1×10^{16} m^{-2}	The effect of localized charges decreases with increasing temperature.
2014	[100]	DMG	-1×10^{16} m^{-2} to 1×10^{16} m^{-2}	ITC alters the temperature sensitivity parameter.
2014	[103]	JL	0, 5×10^{12}, 1×10^{13} cm^{-2}	ITCs' effect intensifies as the nanowire radius or doping concentration decreases.

From Table 1.8, it is observed that ITCs generally deteriorate device performance, though their impact strongly depends on polarity and density. Negative ITCs tend to reduce I_{OFF}, whereas positive ITCs significantly increase it, leading to degraded performance. Furthermore, Mudidhe *et al.* [29] reported that in the analog/RF applications, negative ITCs are often found to provide better performance compared to positive ITCs. The presence of ITCs also affects parameters such as transconductance, gain, and frequency response, indicating reduced efficiency. In 2018, Suman *et al.* [102] showed that the high-*k* materials and advanced gate structures help in minimizing the impact of ITCs. Additionally, smaller device dimensions and higher doping concentrations increase sensitivity to ITCs. These reports indicate that managing ITCs is essential to ensure stable and reliable JL-NWFET operation, highlighting a trade-off between scaling and device robustness.

1.5 RESEARCH GAPS

Based on the literature review of improvement techniques in existing JL-NWFETs, analytical modeling approaches, biosensor applications, and circuit-level implementations, four major research gaps have been identified, which are as follows:

i. Although JL-NWFETs reduce variability and simplify fabrication by eliminating abrupt junctions and complex doping profiles, a dedicated and comprehensive structure specifically designed to simultaneously mitigate L-BTBT and enhance I_{ON} while maintaining strong electrostatic control is still lacking.

ii. To ascertain the practicality and suitability of the improved device architecture, it is imperative to develop an analytical model. Many reported analytical models primarily focus on the channel region, assuming that conduction occurs only within the gated channel and therefore often neglect the influence of S/D extensions.

iii. The growing demand for user-friendly and rapidly responsive diagnostic devices for various diseases within the field of healthcare has underscored the necessity for enhancing

the structure of nanowires dedicated to disease detection. There is a compelling need to develop and implement a highly efficient and I-JL-NWFET for disease detection.

iv. Most reported works have evaluated improved JL-NWFET structures either for biosensor applications or for specific circuit configurations. However, comprehensive circuit-level analysis to establish the broader applicability of the proposed device architecture remains limited. Therefore, a detailed evaluation of electronic circuit applications is required to validate performance improvements.

1.6 PROBLEM STATEMENT

JL-NWFETs have emerged as promising candidates for next-generation semiconductor devices due to their simple structure, excellent scalability, and compatibility with nanoscale fabrication. Despite these advantages, several critical challenges limit their performance and practical adoption. One major issue is insufficient volume depletion in the OFF-state, which results in higher I_{OFF} and degraded switching characteristics. Additionally, JL-NWFETs often exhibit lower I_{ON} compared to conventional NWFETs, affecting overall device efficiency.

Another significant challenge is the absence of accurate and comprehensive analytical models for these devices. Conventional analytical equations developed for planar MOSFETs are generally not directly applicable to any novel JL-NWFET device structures because of their cylindrical structure with different performance enhancement strategies. This limitation restricts the proper extraction of key parameters such as V_T, SS, and I_{DS}. Therefore, addressing these limitations is essential to enhance the reliability of JL-NWFETs for advanced nanoelectronics applications.

The integration of JL-NWFETs into biomedical and low-power electronic systems introduces additional challenges along with new opportunities. Although cylindrical devices offer high sensitivity due to their high surface-to-volume ratio, their application in biosensing is limited by design constraints and a lack of standardized evaluation methods. Achieving high sensitivity while ensuring compatibility with biological environments remains a critical requirement. Moreover, real-time and accurate detection of biomolecules under practical conditions demands robust and reliable device performance.

At the same time, the increasing demand for low-power portable electronics, IoT systems, and high-speed circuits requires devices with low leakage, high switching speed, and energy efficiency. The conventional device design faces severe SCEs and higher power dissipation at scaled dimensions, making JL-NWFETs a potential alternative. However, a trade-off exists

between achieving high performance and meeting application-specific requirements. Hence, there is a strong need to develop optimized JL-NWFET architectures that can simultaneously improve electronic performance and enable efficient biomedical sensing for future integrated systems.

1.7 OBJECTIVES

The primary goal of this research is to propose a novel Improved JL-NWFET for biomedical and electronics applications. Furthermore, the analytical modeling for the proposed device is required to derive its electrical characteristics and validate the simulation results. To carry out the whole research work, the following four objectives are formulated:

Objective - 1: Design and Structural Analysis of an Improved Junctionless Nanowire FET.

Objective - 2: Analytical Modelling to Extract Performance Parameters for Improved Junctionless Nanowire FET.

Objective - 3: Performance Assessment of Improved Nanowire FET for Biomedical Application.

Objective - 4: Analysis of Electronic Circuit Application using Improved Nanowire FET.

To attain these objectives, a systematic methodology is adopted. The adopted methodology is structured in accordance with the overall aim of this research, enabling effective analysis and assessment of the proposed objectives.

1.8 OBJECTIVE-WISE METHODOLOGY

The following methodologies are followed to attain the formulated objectives:

Methodology for Objective 1

To accomplish Objective 1, a novel device structure, the Improved JL-NWFET, is first proposed and analyzed using SILVACO ATLAS TCAD. The device is initially optimized with respect to core thickness, gate oxide material, spacer material, and spacer length. Subsequently, the proposed Improved JL-NWFET is compared with four other device structures. After optimization, channel length and channel thickness scaling are performed on Improved JL-NWFET and the conventional JL-NWFET to evaluate their impact on electrical, analog/RF, and linearity characteristics. After optimizing the channel dimensions, the effect of temperature variations on electrical, analog, and linearity performance is also investigated.

Methodology for Objective 2

In this objective, analytical models are developed for three different device configurations. First, the Improved JL-NWFET with a CS structure and DMG is considered. Second, the Improved JL-NWFET with a CS and GSS is analyzed. Finally, the Improved JL-NWFET combining CS, DMG, and GSS is modeled. The analytical formulations for all configurations are implemented using MATLAB. Subsequently, the obtained analytical solutions are evaluated for device performance. These results are then compared with simulation outcomes to ensure accuracy and consistency. This comparison validates the effectiveness of the proposed structure.

Methodology for Objective 3

The methodology for this objective consists the utilization of proposed Improved JL-NWFET for the application in biomedical sensing. Initially, the device is optimized with respect to nanocavity length and nanocavity size. Subsequently, p53 biomolecules are selected as the biomarker for gastrointestinal cancer detection based on a comprehensive literature review. The proposed structure is then thoroughly analyzed in terms of sensitivity. In addition, the repulsive steric hindrance effect is incorporated to ensure a more realistic evaluation of biosensor performance. Furthermore, to facilitate practical sensing, the proposed I-JL-NWFET-based biosensor is integrated into a common-source amplifier as the readout circuit.

Methodology for Objective 4

Herein, the objective is to demonstrate the utilization of the proposed Improved JL-NWFET for electronic applications through circuit-level implementation. The CMOS inverter and ring oscillator circuits are designed using the proposed device. The performance of the Improved JL-NWFET-based CMOS inverter is evaluated by analysing its static and dynamic characteristics. Additionally, three-stage ring oscillator circuits are implemented to investigate RF performance. The results obtained from both the CMOS inverter and ring oscillator are compared with three counterpart device architectures to identify the contribution of each design element.

1.9 THESIS ORGANIZATION

The complete thesis is arranged in seven chapters. Primarily, a brief introduction based on the concerned issue and motivation behind the study is included in each chapter. Conjointly, the

key observations are outlined at the end. A concise overview of each chapter is outlined as follows

Chapter 1: Introduction

This chapter introduces the evolution of nanoscale transistor technologies with emphasis on JL-NWFET as a promising alternative to conventional inversion-mode NWFET. The challenges associated with aggressive device scaling, including SCEs, leakage current, reliability, and increased fabrication complexity, are discussed. The problem statement behind developing an Improved JL-NWFET is explained. The literature review, research gaps, research objectives, and organization of the thesis are also outlined in this chapter.

Chapter 2: Structural Analysis of Improved Junctionless Nanowire FET.

This chapter focuses on the design and structural optimization of the Improved JL-NWFET incorporating an oppositely doped CS architecture with DMG and GSS. The impact of core thickness, channel thickness, gate oxide material, spacer material, spacer length, and channel length on device characteristics is systematically investigated. The proposed structure demonstrates improved suppression of DIBL, reduced L-BTBT, enhanced I_{ON}, reduced I_{OFF}, improved SS, and a higher I_{ON}/I_{OFF} ratio.

Chapter 3: Analytical Modelling of Improved Junctionless Nanowire FET.

In this chapter, a surface-potential-based analytical model is developed for Improved JL-NWFET. The analytical formulation is derived to accurately predict device parameters, including surface potential distribution, threshold voltage, and drain current characteristics. The developed model is validated against simulation results under various biasing and structural conditions, showing strong agreement. The model provides physical insight into the role of geometrical and material parameters in mitigating SCEs and improving subthreshold behavior.

Chapter 4: p53 Biomarker Detection for Gastrointestinal Cancer Using Improved Junctionless Nanowire FET.

This chapter extends the proposed Improved JL-NWFET structure for biomedical sensing applications, specifically for label-free detection of the p53 biomarker associated with gastrointestinal cancers. The biosensing mechanism is based on interface charge deduction within a nanocavity region introduced in the device. The influence of nanocavity position, cavity length, core thickness, and channel dimensions on sensitivity is analyzed. The study also evaluates temperature effects and steric hindrance to ensure realistic, practical biosensor performance.

Chapter 5: CMOS Inverter And Ring Oscillator Analysis Using Improved-Junctionless Nanowire FET

This chapter investigates the circuit-level applicability of the proposed Improved JL-NWFET. CMOS inverters are designed and analyzed to evaluate static and dynamic performance metrics. The impact of the CS, high-*k* GSS, and DMG on leakage-delay trade-offs is investigated. Furthermore, a 3-stage ring oscillator is analyzed, demonstrating the applicability of the proposed device for RF applications. The proposed device achieves a balanced compromise between leakage suppression, switching stability, and speed.

Chapter 6: Conclusion, Future Scope, and Social Impact

The major contributions of the present research in accordance with the stated objectives are summarized in this chapter. It highlights the key outcomes related to the structural design, analytical modeling, biomedical sensing application, and circuit-level analysis of the Improved JL-NWFET. The overall performance improvements and applicability of the proposed device are also discussed. In addition, the future scope and social impact of the research work are discussed.

Furthermore, the thesis is followed by the list of publications (published, accepted, and in progress) and the list of references referred to carry out this research work.

1.10 SUMMARY OF THE CHAPTER

From the basic concept and detailed literature review of JL-NWFET presented in this chapter, it is observed that JL-NWFETs offer significant advantages over conventional MOSFETs. Furthermore, previous studies reveal the growing potential of JL-NWFETs in biomedical sensing and digital circuit applications due to their compatibility with nanoscale integration. However, the literature review also indicates that simultaneous optimization of JL-NWFET for biosensing capability and circuit-level applicability remains a major challenge. These observations provide the primary motivation for the present research work. The identified limitations and research gaps establish the need for developing Improved JL-NWFET architectures capable of improved sensing performance and reliable circuit operation. Therefore, the subsequent chapters focus on the design and analytical modeling of improved JL-NWFET structures incorporating advanced structural techniques, followed by detailed TCAD-based performance analysis, biomedical sensing investigation, and circuit-level validation to achieve the proposed research objectives.

CHAPTER-2
STRUCTURAL ANALYSIS OF IMPROVED JUNCTIONLESS NANOWIRE FET

2.1 INTRODUCTION

Despite offering several advantages, JL-NWFETs exhibit drawbacks like low I_{DS} and g_m when compared to conventional NWFETs. Additionally, the implementation of JL-NWFET can lead to unavoidable process challenges, such as Random Dopant Fluctuations (RDFs) resulting in device variation [104]. Furthermore, the n-channel JLT experiences a challenge related to band overlap, which results in L-BTBT of electrons during the OFF-state from the valence band to the conduction band of the channel and drain, respectively [105].

Consequently, this mechanism causes an increase in the number of holes within the n-channel, as electrons are being transported away via tunneling due to L-BTBT. As a consequence of this phenomenon, a parasitic n-p-n Bipolar Junction Transistor (BJT) is triggered, where the source, channel, and drain act as parasitic emitter, base, and collector, respectively. The occurrence of L-BTBT significantly increases the I_{OFF} and induces the parasitic BJT effect in JL-NWFET, necessitating measures to mitigate these issues. The focus of this thesis is to explore the combined advantages of DMG and GSS techniques in an oppositely doped CS JL-NWFET.

Therefore, the following objective is framed here to obtain an Improved Junctionless Nanowire FET:

"Design and Structural Analysis of an Improved Junctionless Nanowire FET."

To realize the desired objective, the methodology includes the following steps: -

- Validation of an experimental NWFET using SILVACO ATLAS.
- Development of a JL-NWFET using the same experimentally realized NWFET device parameters.
- Design an Improved JL-NWFET to improve the performance characteristics.
- Optimization of the proposed Improved JL-NWFET for performance improvement.
- Comparative analysis of the Improved JL-NWFET with the different variants of JL-NWFET.

This chapter is arranged in eight sections, including this introductory section numbered as 2.1. In Section 2.2, the validation of an experimentally realized NWFET through simulation is

presented. Subsequently, in Section 2.3, the conventional JL-NWFET is analyzed by keeping the device parameters identical to those of the NWFET. In Section 2.4, a novel Improved JL-NWFET is introduced along with a possible fabrication process flow. The optimization of material and other device parameters is presented in Section 2.5.

Additionally, the proposed device is compared with other devices in Section 2.6. Thereafter, the impact of channel length scaling and channel thickness scaling are presented in Section 2.7 and 2.8, respectively. Furthermore, after optimizing channel length and channel thickness, the impact of temperature on the Improved JL-NWFET is analyzed in Section 2.9, and the results are compared with JL-NWFET. The summary of the complete research work of this chapter is highlighted in Section 2.9.

2.2 VALIDATION OF EXPERIMENTAL NWFET

Prior to the simulation and analysis of the conventional JL-NWFET, its inherent limitations are first identified by comparing its performance with that of a conventional NWFET. To simulate the NWFET, the experimentally reported NWFET is first calibrated in SILVACO ATLAS [106] to establish the simulation framework. Fig. 2.1 (a) and (b) show a 3-D view and 2-D cross-sectional view of an NWFET whose structural parameters and material are in accordance with the experimental report [8], such as L_C, t_{si}, t_{ox}, channel doping (N_A), and S/D doping (N_D), which are also presented in Table 2.1. The $L_{S/D}$ regions are 25 nm as reported in [17]. The models consist of the field and concentration dependent carrier mobility models to account for the velocity saturation and low field mobility effects, respectively.

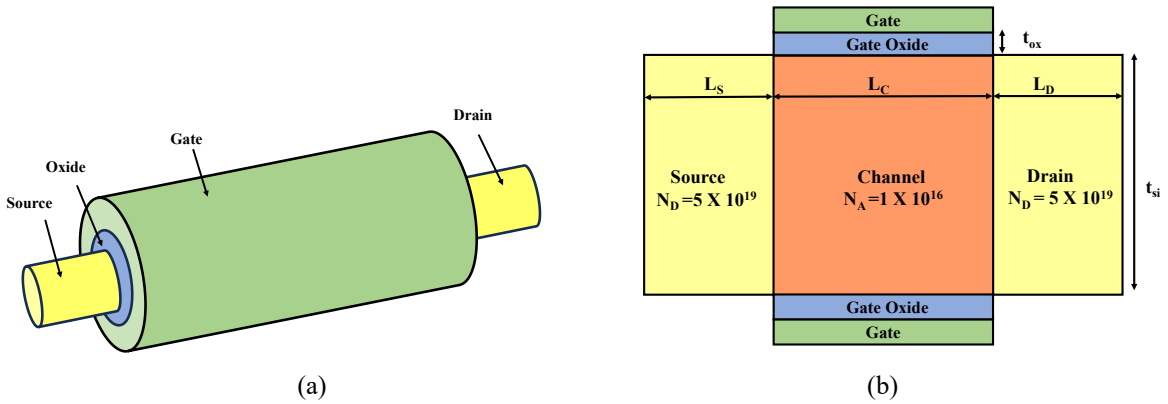


Fig. 2.1 (a) 3-D and (b) 2-D cross-sectional view of NWFET

The Lombardi CVT model to accommodate inversion layer mobility for non-planar devices and the Band Gap Narrowing model for heavily doped regions have been activated. Additionally, the Shockley-Read-Hall and Auger recombination models have been employed to accommodate carrier lifetimes and impact ionization, respectively. Gummel-Newton is

utilized for obtaining numerical solutions. During calibration, the tunneling mass of electrons (m_e) and holes (m_h) are kept to be 0.5 m_o and 0.75 m_o, respectively, where m_o is the electron's rest mass. The effective density of states for electrons (g_c) and holes (g_v) is taken to be 2.2 and 0.67, respectively.

Table 2.1. Device specification for NWFET

Device Parameters		**NWFET**
Channel	Material	Silicon
	Length, L_C (nm)	60
	Thickness, t_{si} (nm)	10
	Doping, N_A (cm^{-3})	1×10^{16}
Gate	Material	Polysilicon
Gate Oxide	Material	SiO_2
	Thickness, t_{ox} (nm)	1
Source/Drain	Material	Silicon
	Length, $L_S/_D$ (nm)	25
	Doping, N_D (cm^{-3})	5×10^{19}

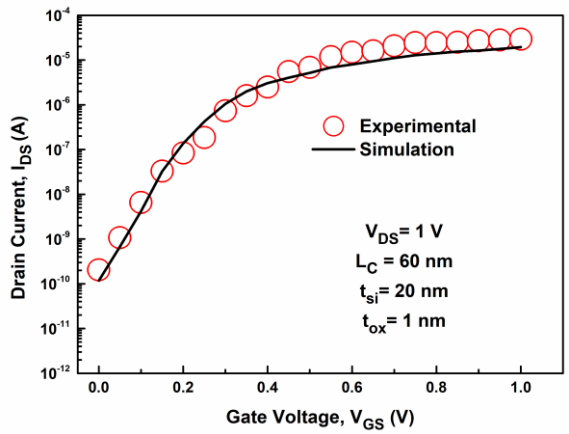


Fig. 2.2 Combined plot for experimental and simulation transfer characteristics of the NWFET

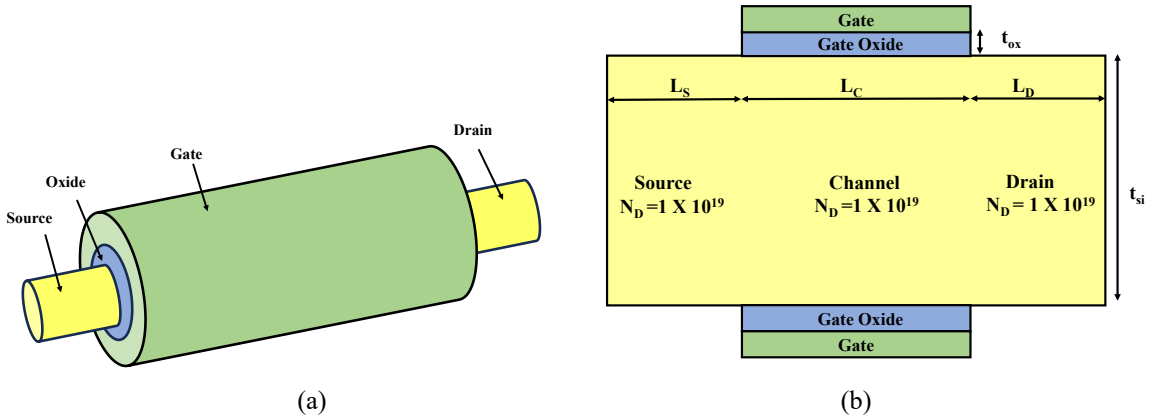
Figure 2.2 depicts a combined plot illustrating the transfer characteristics of NWFET, encompassing both experimental and simulation data. The magnitude of the simulated I_{DS} at $V_{DS} = V_{GS} = 1$ V is 24.1% less than the experimental data. The I_{ON}/I_{OFF} ratio is determined by

$$\frac{I_{ON}}{I_{OFF}} = \frac{I_{DS}\left(V_{DS} = 1V, V_{GS} = 1V\right)}{I_{DS}\left(V_{DS} = 1V, V_{GS} = 0V\right)} \tag{2.1}$$

The I_{ON}/I_{OFF} ratio for both the experimental and simulated data of NWFET is obtained to be approximately 10^5. This calibration ensures close agreement between the experimental and simulated transfer characteristics and provides a reliable reference for subsequent comparison with the JL-NWFET.

2.3 CHARACTERISTICS OF JL-NWFET

For the analysis of JL-NWFET, the structural parameters are kept identical as NWFET. The 3-D and 2-D cross-sectional depiction of JL-NWFET is illustrated in Fig. 2.3. The materials and device parameters for JL-NWFET are shown in Table 2.2. The only difference lies in the uniform n-type doping concentration of 10^{19} cm^{-3} utilized for defining the source, drain, and channel regions [107]. Furthermore, the gate metal in this configuration possesses a high work function of 5.1 eV [17]. To validate the simulation setup for conventional JL-NWFET, the same physical models are such as used as mentioned in subsection 2.1. Additionally, to consider the tunneling of electrons, the non-local BTBT model is utilized.



(a) (b)

Fig. 2.3 (a) 3-D and (b) 2-D cross-sectional view of JL-NWFET

Table 2.2. Device specification for JL-NWFET

Device Parameters		JL-NWFET
Channel	Material	Silicon
	Length, L_C (nm)	60
	Thickness, t_{si} (nm)	10
	Doping, N_D (cm^{-3})	1×10^{19}
Gate	Material	Gold
	Workfunction (eV)	5.1
Gate Oxide	Material	SiO_2
	Thickness, t_{ox} (nm)	1
Source/Drain	Material	Silicon
	Length, $L_{S/D}$ (nm)	25
	Doping, N_D (cm^{-3})	1×10^{19}

A combined transfer characteristics of simulation and experimental work [107] is plotted corresponding to V_{DS} = 1 V in Fig. 2.4. The close agreement between the simulated and experimental results validates the adopted physical models for subsequent JL-NWFET analysis.

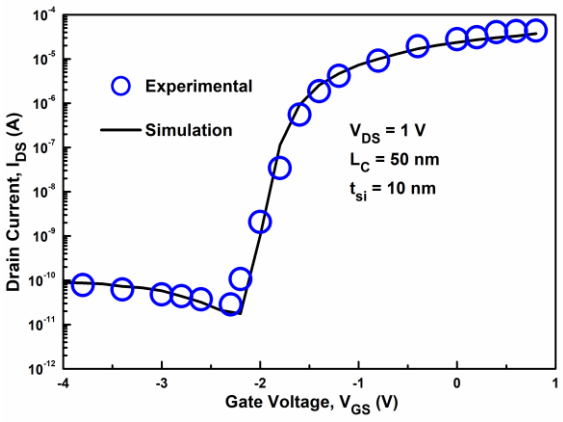


Fig. 2.4 Combined plot of simulation and experimental results of JL-NWFET

Figure 2.5 demonstrates the V_T extraction of JL-NWFET. The V_T corresponds to the V_{GS} of the junctionless structure, where the surface potential reaches its lowest value. One of the methods to determine V_T from the $\sqrt{I_D}$-V_{GS} curve is linear extrapolation [108, 109]. In this approach, the tangent to the $\sqrt{I_D}$-V_{GS} curve is extended to intersect the V_{GS} axis, yielding the value of V_T. Herein, JL-NWFET exhibits a V_T of 0.208 V as illustrated in Fig. 2.5.

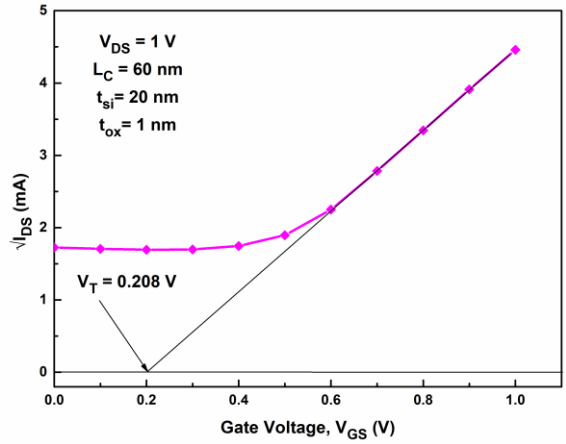
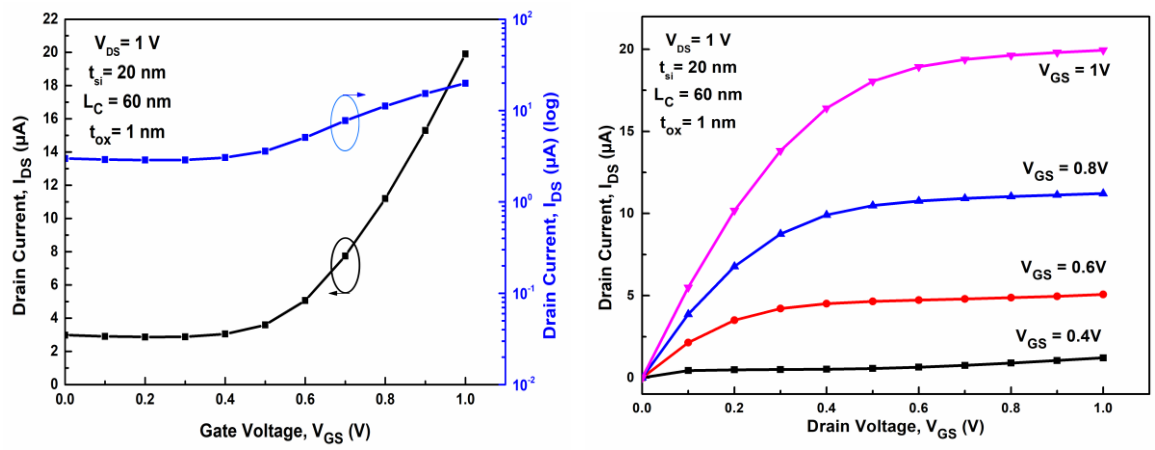


Fig. 2.5 Threshold voltage extraction of JL-NWFET

The transfer characteristics and output characteristics of JL-NWFET are illustrated in Fig. 2.6 (a) and (b), respectively. In Fig. 2.6 (a), the I_{DS} of JL-NWFET is obtained as 19.9 µA at V_{DS} = V_{GS} = 1 V, which is 9.5% and 31.3% less than the simulated and experimental NWFET, respectively. JL-NWFET experiences a reduced I_{ON} due to enhanced series resistance arising from the lightly doped extension regions of the S/D, in contrast to the NWFET. Furthermore, JL-NWFET experiences a significant increase in I_{OFF}, resulting in an unfavourable I_{ON}/I_{OFF} ratio. This outcome arises from the inability to achieve volume depletion despite using a high work function gate metal, thereby causing an enhanced OFF-state leakage current.



(a) (b)

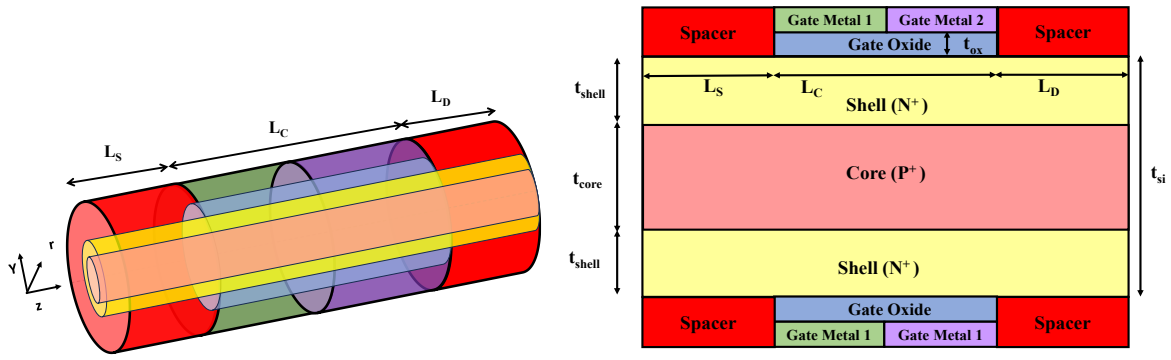
Fig. 2.6 (a) Transfer characteristics and (b) output characteristics of JL-NWFET

In Fig. 2.6 (b), there is a noticeable enhancement in current as the V_{GS} increases. Additionally, the SS is obtained as 541.7 mV/decade for JL-NWFET. Despite the benefits of reducing the thermal budget and simplifying the fabrication process, JL-NWFET offers an unsatisfactory I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, and SS. Consequently, there is a need to improve the structure of JL-NWFETs in a way that achieves both high I_{ON} while reducing I_{OFF} concurrently.

2.4 PROPOSED DEVICE: IMPROVED JUNCTIONLESS NANOWIRE FET

One approach towards improving the OFF-state of JL-NWFET involves the incorporation of an opposite-doped core in the large t_{si}. This strategy facilitates volume depletion during the OFF-state. Additionally, to further improve the JL-NWFET structure to achieve enhanced I_{ON} and reduced I_{OFF}, GME along with a GSS can be employed. The proposed Improved JL-NWFET (I-JL-NWFET), featuring an n-type channel, is analyzed with the inclusion of an equally and oppositely doped core, a high-*k* GSS, and a DMG. Fig. 2.7 (a) and (b) illustrate the 3-D and 2-D cross-sectional views of I-JL-NWFET, respectively.

The novelty in the present work resides in the unique design of the proposed device, which adeptly combines the benefits of three distinct architectures. The first architecture encompasses an oppositely doped core that not only helps in volume depletion but also effectively mitigates the occurrence of parasitic BJT action induced by the L-BTBT in JL-NWFET during the OFF-state. The second architecture involves DMG, which improves carrier transport efficiency and reduces SCEs as compared with the SMG device structure. The third architecture comprises a high-*k* GSS to improve subthreshold characteristics.



(a) (b)

Fig. 2.7 (a) 3-D and (b) 2-D cross-sectional view of Improved JL-NWFET (I-JL-NWFET)

Table 2.3. Device specification for the proposed I-JL-NWFET

Device Parameters		**I-JL-NWFET (This work)**	
Channel	Material	Silicon	
	Length, L_C (nm)	30 (L_{M1})	30 (L_{M2})
	Thickness, t_{si} (nm)	10	
	Doping, N_D (cm^{-3})	1×10^{19}	
Core	Material	Silicon	
	Thickness, t_{core} (nm)	10	
	Doping, N_A (cm^{-3})	1×10^{19}	
Gate	Workfunction (eV)	5.1 (M_1)	4.6 (M_2)
Gate Oxide	Material	SiO_2	
	Thickness, t_{ox} (nm)	1	
Source/Drain	Length, $L_{S/D}$ (nm)	25	
Spacer	Material	HfO_2	
	Length	25	

Unless otherwise stated, the device specifications of the proposed I-JL-NWFET in this subsection follow those listed in Table 2.3. The p-type doped core is doped at a concentration of 10^{19} cm^{-3}. As a result, n-type doped shell, with doping of 10^{19} cm^{-3}, defines the active device layer for I-JL-NWFET. The core thickness (t_{core}) and shell thickness (t_{shell}) are calculated using the relation $t_{si} = (2 \times t_{shell}) + t_{core}$. Moreover, for the DMG structure, the gate metals M_1 and M_2 are characterized by work functions of 5.1 eV and 4.6 eV, respectively. To optimize the performance of I-JL-NWFET, a gate work function difference of 0.5 eV is maintained between M_1 and M_2 [11]. Moreover, the lengths of M_1 (L_{M1}) and M_2 (L_{M2}) are equal, ensuring that $L_C = L_{M1} + L_{M2} = 60$ nm.

Figure 2.8 outlines the possible fabrication process steps for I-JL-NWFET using the integrated process flow reported by Rana *et al.* [110] for cylindrical JL-NWFET and Lee *et al.* [19] for CS architecture. As shown in Fig. 2.8, this process can begin with a p-type SOI wafer. The fin structures are defined using deep ultraviolet lithography, followed by anisotropic pattern

transfer via Reactive Ion Etching (RIE). The resulting silicon fins are transformed into cylindrical nanowires through a prolonged dry oxidation process for 5 hours. Subsequently, the thermally grown oxide is removed using a Buffered Hydrofluoric Acid (BHF) dip, yielding the p-doped silicon core [110].

An undoped amorphous Si film is deposited, followed by Solid Phase Crystallization (SPC) at 600 °C for 24 hours. The active region is defined via E-beam lithography, and the shell thickness is further reduced to the desired dimension through selective thermal reoxidation. For the MLD process, after the Hydrofluoric Acid (HF) dip, Si surfaces are reacted with diethyl 1-propylphosphonate for n-doping. After capping oxide, the samples are annealed by a combination of MWA+COLSA to drive in and re-activate dopants [19]. After the capping oxide removal, gate oxide (SiO_2) was thermally grown on the surface of the NWFET. The DMG can be realized by high-dose nitrogen implantation into *Mo* to form M_1 and M_2 [15].

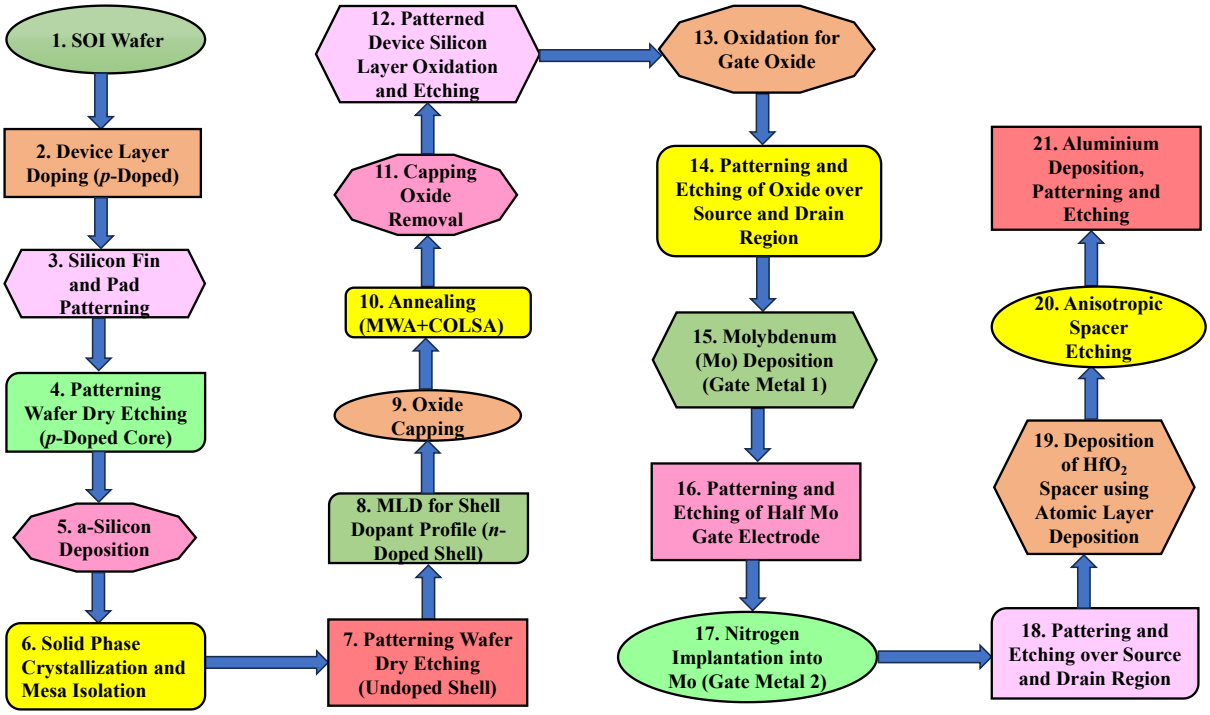


Fig. 2.8 Stepwise possible fabrication process flow of I-JL-NWFET

Thereafter, the ATD is employed to form a GSS [23]. After patterning the gate electrodes, standard metal deposition for contact pads is used. One of the main challenges in the practical fabrication of I-JL-NWFET with high-permittivity spacers might arise in achieving precise etching anisotropy [111]. This is crucial for maintaining uniform gate profiles and ensuring accurate critical dimension control, which directly impacts device performance. Additionally, proper spacer patterning is essential for aligning and separating the gate from the S/D regions, helping to minimize electrical leakage and parasitic effects. The process-induced variations in

conventional JL-NWFET lead to RDFs, which cause fluctuations in the V_T. However, RDFs can be mitigated by using the SDP formed through MLD and MWA as reported in [13].

2.4.1 Optimization of core thickness

The t_{core} is a critical parameter in core-shell structures, and its optimization is essential for tailoring the characteristics of I-JL-NWFET as it impacts the charge transport and carrier confinement within the channel region. Fig. 2.9 (a) and (b) illustrate the transfer characteristics for different t_{core} varying from 4 nm to 12 nm in linear and log scales, respectively. As the t_{core} increases, the I_{DS} decreases in both linear and log scales. This reduction is attributed to the decrease in the active shell thickness, resulting in a reduced area available for carrier movement within the device.

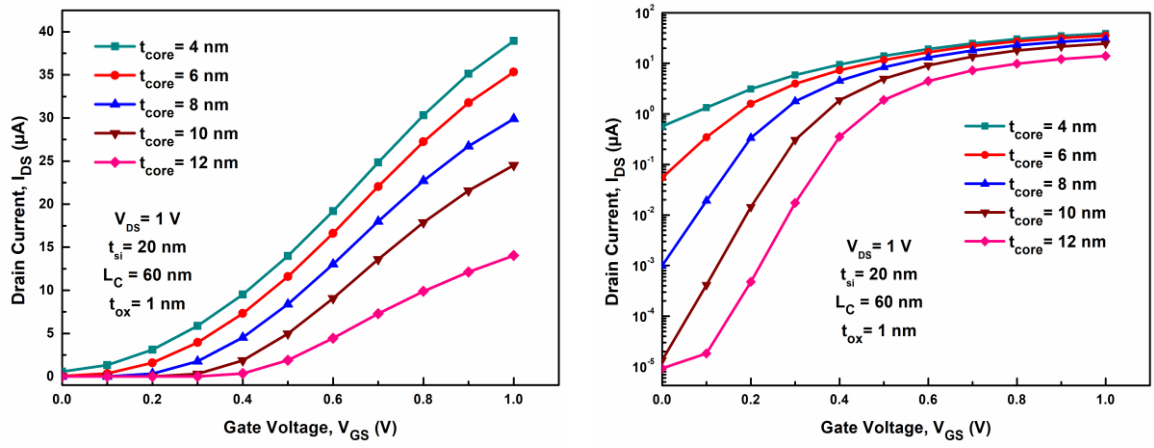


Fig. 2.9 Transfer characteristics of I-JL-NWFET for different t_{core} in (a) linear scale and (b) log scale

Similarly, in Fig. 2.9 (b), the I_{OFF} current degrades with an increase in the t_{core}. This behavior is due to the existence of a p-type core between two n-type shells, facilitating a larger depletion of carriers when the device is in the OFF-state. However, it is observed that the reduction in I_{OFF} current becomes less significant after increasing t_{core} beyond 10 nm. This suggests that increasing t_{core} beyond this point does not have a substantial impact on the I_{OFF} of I-JL-NWFET.

Figure 2.10 depicts the impact of t_{core} variation on the I_{ON}/I_{OFF} ratio and SS. As the t_{core} increases, SS shows a decreasing trend until the t_{core} reaches 10 nm, beyond which SS reaches saturation. In contrast, the I_{ON}/I_{OFF} ratio experiences a significant improvement until the t_{core} reaches 10 nm, after which it decreases marginally. Based on the findings, the optimization of the t_{core} yields an optimal value of 10 nm which is half the value of t_{si}. For further optimization, the t_{core} of I-JL-NWFET is set at 10 nm.

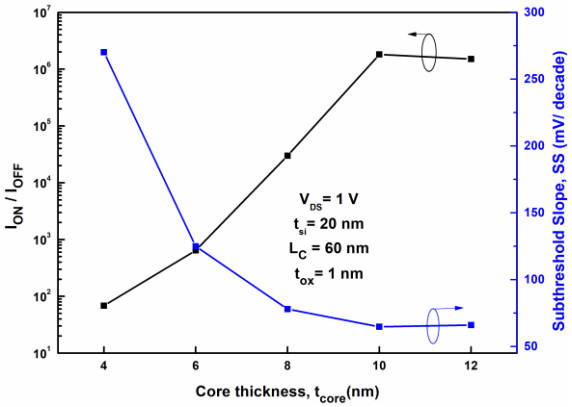
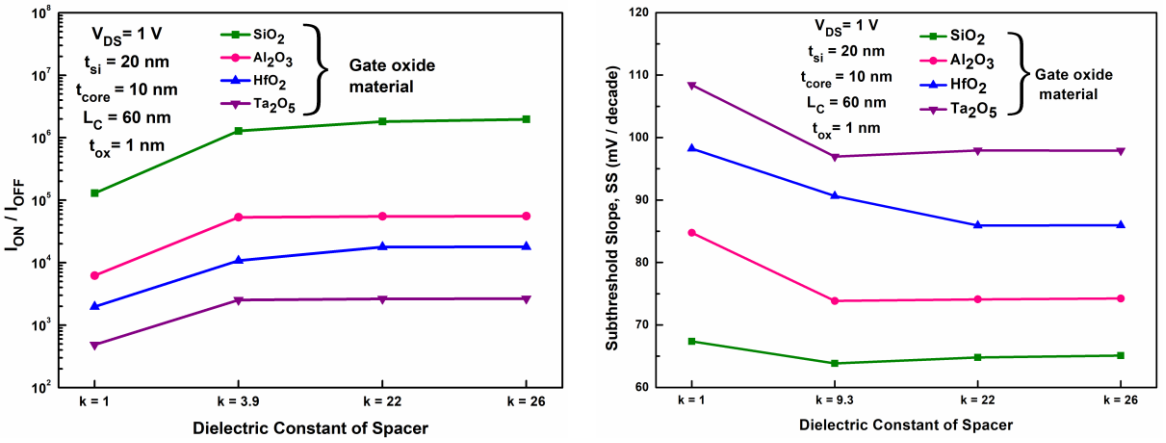


Fig. 2.10 Variation of I_{ON}/I_{OFF} ratio and SS for different t_{core} of Improved JL-NWFET

2.4.2 Optimization of gate oxide material

The choice of gate oxide material in combination with the spacer material is of paramount importance in any device structure. This selection influences various aspects of device performance and characteristics. Herein, different gate oxide materials, such as SiO_2 (k = 3.9), Aluminium oxide (Al_2O_3, k = 9.3), HfO_2 (k = 22), and Tantalum pentoxide (Ta_2O_5, k = 26) are tested in conjunction with different spacer materials such as air (k = 1), SiO_2 (k = 3.9), HfO_2 (k = 22) and Ta_2O_5 (k = 26).



(a) (b)

Fig. 2.11 Variation of (a) I_{ON}/I_{OFF} ratio and (b) SS as a function of different dielectric constants of the spacer for various gate oxide materials of Improved JL-NWFET

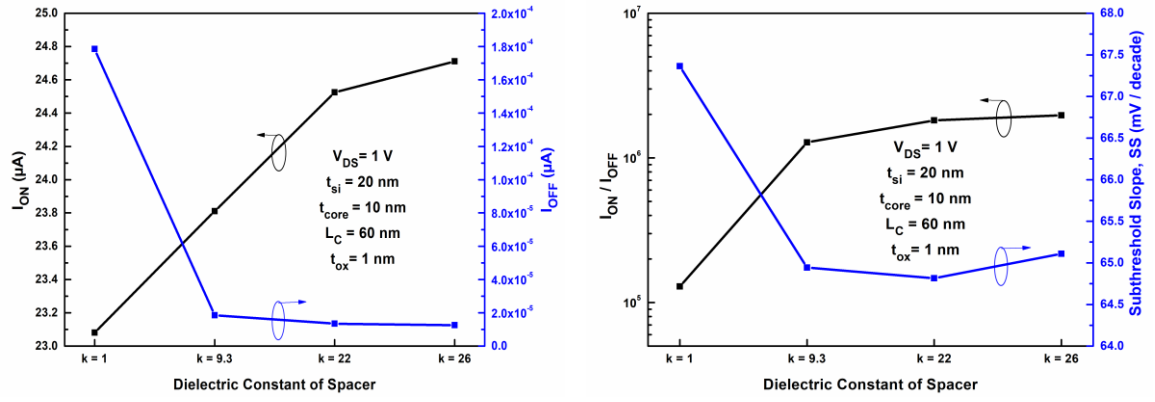
In Fig. 2.11 (a), the I_{ON}/I_{OFF} ratio is plotted as a function of aforesaid spacer dielectric constants (k = 1, 3.9, 22, and 26) for the aforementioned gate oxide materials. A higher I_{ON}/I_{OFF} ratio signifies a better switching capability of any device. It can be observed that the utilization of SiO_2 as the gate oxide yields a superior I_{ON}/I_{OFF} ratio, followed by Al_2O_3, HfO_2, and Ta_2O_5 as the gate oxide for various spacer materials (k = 1, 3.9, 22, and 26). Furthermore, the I_{ON}/I_{OFF} ratio

shows an improvement with an increasing spacer dielectric constant till k = 22 (HfO_2), regardless of the gate oxide material used.

Furthermore, Fig. 2.11 (b) shows the variation of SS as a function of spacer dielectric materials for various gate oxide materials. It is evident that as the spacer dielectric constant increases, there is a reduction in SS, irrespective of the gate oxide material employed. Moreover, the minimum SS is obtained with SiO_2 as the gate oxide, followed by Al_2O_3, HfO_2, and Ta_2O_5 as the spacer dielectric constant increases (k = 1 to 26). The combination of a low-k material as the gate oxide and a high-k material as the spacer is a strategic decision aimed at optimizing I_{ON}/I_{OFF} ratio and SS. A low-k material, SiO_2 (k = 3.9), is known for having a low dielectric constant. This property is advantageous for reducing capacitance and, consequently, increasing I_{ON}/I_{OFF} ratio. On the other hand, a high-k material, like HfO_2 (k = 22), is chosen for the spacer which helps to reduce I_{OFF}. The reduction in OFF-state current contributes to a lower SS.

2.4.3 Optimization of the spacer material

The appropriate choice of spacer material plays a critical role in defining and controlling device performance during the OFF-state. The spacer assists in suppressing SCEs, such as SS degradation and leakage currents. Its proper design and selection are essential for achieving high device performance. For the selection of suitable spacer material among air (k = 1), SiO_2 (k = 3.9), HfO_2 (k = 22), and Ta_2O_5 (k = 26) for I-JL-NWFET, a comparative analysis is investigated. The variation of I_{ON} and I_{OFF} as a function of the spacer material having different dielectric constants is plotted in Fig. 2.12 (a).



(a) (b)

Fig. 2.12 Plots of (a) I_{ON} and I_{OFF} and (b) I_{ON}/I_{OFF} ratio and SS of I-JL-NWFET with different dielectric constants of the spacer

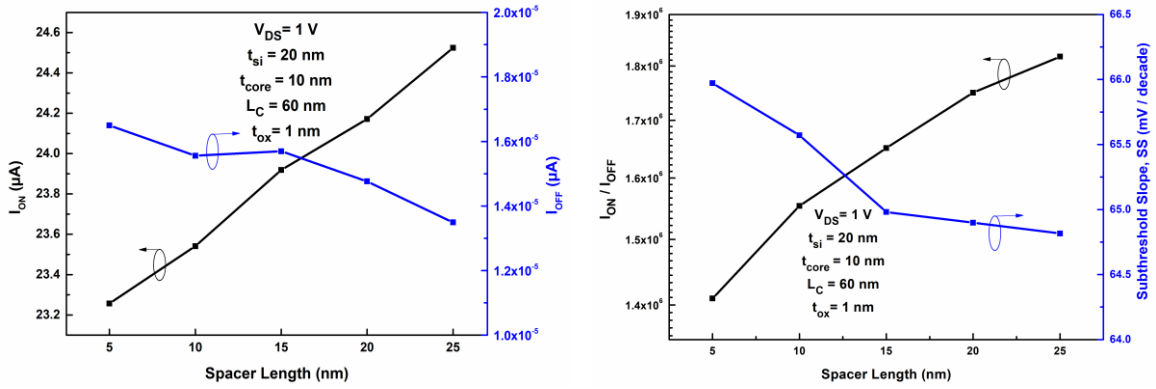
Furthermore, Fig. 2.12 (b) depicts the variation of I_{ON}/I_{OFF} ratio and SS as a function of spacer material having dielectric constants. The introduction of the spacer on both sides of the gate

enhances the fringing electric fields and leads to the depletion of the device beyond the gate edge in the OFF-state [112]. The fringe fields refer to electric fields that extend beyond the edges of the gate. Consequently, I_{OFF} decreases with increasing spacer dielectric constant, and after k = 22, it reaches saturation in Fig. 2.12 (a). In contrast, I_{ON} increases with an increasing spacer dielectric constant.

In Fig. 2.12 (a), the high-k GSS helps to concentrate these electric fields, leading to a more efficient current flow in the ON-state. This trend contributes to the overall increasing trend of the I_{ON}/I_{OFF} ratio depicted in Fig. 2.12 (b). The variation of SS is also plotted in Fig. 2.12 (b) which depicts that as the spacer dielectric constant increases, SS reduces until k = 22 (HfO_2), after which it slightly increases. Henceforth, the choice of HfO_2 as the spacer material with SiO_2 as the gate oxide material further optimizes I-JL-NWFET's characteristics, making it a favorable combination for achieving enhanced device performance.

2.4.4 Optimization of spacer length

The spacer length of the device can impact leakage currents across the gate-channel interface. An optimal spacer length can minimize OFF-state leakage current, contributing to energy efficiency and reducing standby power consumption. Fig. 2.13 (a) displays the I_{ON} and I_{OFF} variation in comparison to spacer length. The variation of the I_{ON}/I_{OFF} ratio and SS as a function of spacer length is plotted in Fig. 2.13 (b).



(a) (b)

Fig. 2.13 Plots of (a) I_{ON} and I_{OFF} and (b) I_{ON}/I_{OFF} ratio and SS of I-JL-NWFET with different spacer lengths

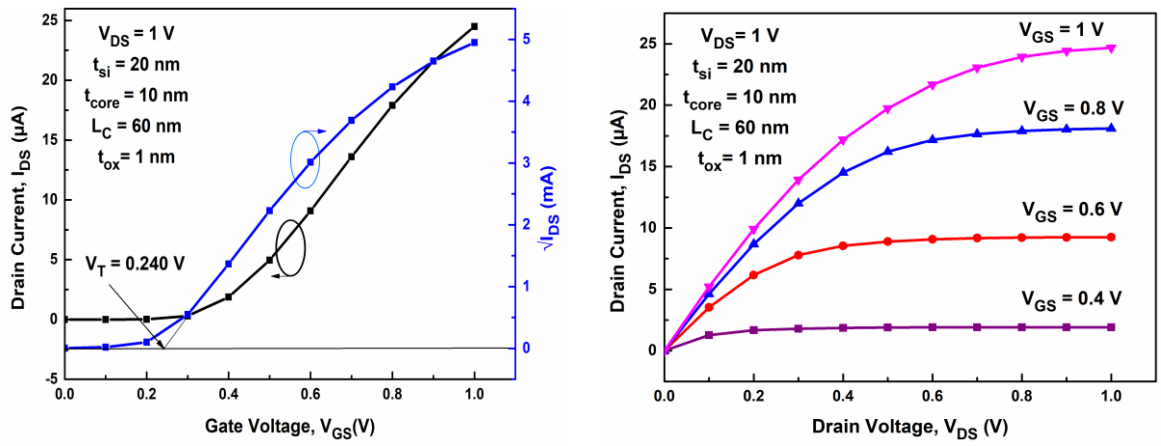
In Fig. 2.13 (a), it is revealed that with increasing spacer length, there is a marginal improvement in the I_{ON}. This improvement is attributed to the reduction in parasitic resistance in the active shell region under the spacer due to fringe fields. The shell layer of I-JL-NWFET beyond the gate edges becomes depleted by adding a high-k GSS. As the spacer length

increases, this depletion region effectively expands, consequently lower I_{OFF}. The maximum I_{ON} and minimum I_{OFF} occur when the spacer length is set at 25 nm.

In Fig. 2.13 (b), it is perceived that as the spacer length increases, there is a significant enhancement in the I_{ON}/I_{OFF} ratio. This means that the device becomes more effective in turning ON and OFF, which is desirable for digital logic applications. The maximum I_{ON}/I_{OFF} ratio is achieved when the spacer length is 25 nm. Contrastingly, as the spacer length increases, there is a slight reduction in the SS. The minimum SS occurs when the spacer length is 25 nm. A smaller SS indicates that the device exhibits a more gradual change in current with increasing gate voltage in the subthreshold region. Eventually, the spacer length is optimized at 25 nm for I-JL-NWFET due to improved I_{ON}/I_{OFF} ratio and SS.

2.4.5 Electrical Characteristics of I-JL-NWFET

After optimization of core thickness, spacer length, gate oxide material, and spacer material, the electrical parameters of I-JL-NWFET are analyzed. Fig. 2.14 (a) demonstrates the transfer characteristics with V_T extraction of I-JL-NWFET. The I_{DS} of I-JL-NWFET is obtained as 24.5 µA at $V_{DS} = V_{GS} = 1$ V. I-JL-NWFET exhibits a V_T of 0.240 V as illustrated in $\sqrt{I_D}$-V_{GS} characteristics in Fig. 2.14 (a). The plot in Fig. 2.14 (b) displays the output characteristics of I-JL-NWFET, showing a significant increase in current as the gate voltage increases.



(a) (b)

Fig. 2.14 (a) Transfer characteristics and (b) output characteristics of I-JL-NWFET

Table 2.4. Performance parameters of JL-NWFET and the proposed I-JL-NWFET

Parameters	V_T (V)	I_{ON} (µA)	I_{OFF} (µA)	I_{ON}/I_{OFF}	SS (mV/decade)
JL-NWFET	0.208	19.9	2.98	6.68	541.7
I-JL-NWFET (This work)	0.240	24.5	1×10^{-5}	1.81×10^{6}	64.8

The extracted performance parameters of JL-NWFET are compared with I-JL-NWFET and succinctly presented in Table 2.4. I-JL-NWFET demonstrates a 23.1% increase in I_{ON} compared to the conventional JL-NWFET. Furthermore, a substantial enhancement is evident in I_{OFF}, which is reduced by an order of 5 in the I-JL-NWFET. As a result, an impressive I_{ON}/I_{OFF} ratio of approximately 10^6 is achieved under the conditions of L_C = 60 nm, t_{si} = 20 nm, and t_{ox} = 1 nm in the I-JL-NWFET. Moreover, an 88% improvement in SS is observed in the I-JL-NWFET compared to the JL-NWFET.

2.5 COMPARATIVE ANALYSIS OF I-JL-NWFET WITH DIFFERENT JL-NWFET STRUCTURES

The enhanced performance of the proposed I-JL-NWFET can be analyzed by comparing it with various structure variants of JL-NWFET. Throughout this section, I-JL-NWFET is labelled as Device D1, whose 2-D cross-sectional view is illustrated in Fig. 2.15 (a) and is systematically evaluated against four comparative architectures, namely D2, D3, D4, and D5, whose 2-D cross-sectional views are illustrated in Fig. 2.15 (b), (c), (d), and (e), respectively. Through a comparative analysis, essential insights into how various nanowire structures affect the performance and behavior of the device characteristics can be understood.

The devices D1, D2, D3, D4, and D5 are designed with identical L_C, t_{ox}, and t_{si} to isolate the impact of individual architectural modifications. Devices D3, D4, and D5 have been previously reported in [17], [13], and [10]. On the other hand, D2 is an intermediate variant of the proposed device, introduced for comparison by excluding the spacer extension, and has not been previously reported. Device D2 incorporates the DMG technique with an oppositely doped core of t_{core} = 10 nm. The gate metals, M_1 and M_2, have work functions of 5.1 eV and 4.6 eV, respectively similar to those of Device D1. This gate configuration allows for enhanced control over the channel conductivity and performance characteristics.

Device D3 is JL-NWFET with an oppositely doped core of t_{core} = 10 nm, similar to Devices D1 and D2. However, it employs an SMG with a work function of 5.1 eV. This gate design provides less electrostatic control over the channel conductivity with a simpler gate structure compared to Devices D1 and D2. The JL-NWFET structure of Device D4 features an intrinsic core t_{core} = 10 nm with an SMG having a work function of 5.1 eV. The intrinsic core means that it is undoped, and the control of channel conductivity primarily relies on the gate potential. The conventional structure of JL-NWFET is labelled as Device D5 in this section. The devices D1,

D2, D3, and D4 have similar dimensions as Device D5, with the following parameters: L_C = 60 nm, t_{si} = 20 nm, $L_{S/D}$ = 25 nm, and t_{ox} = 1 and SiO_2 as the gate oxide material.

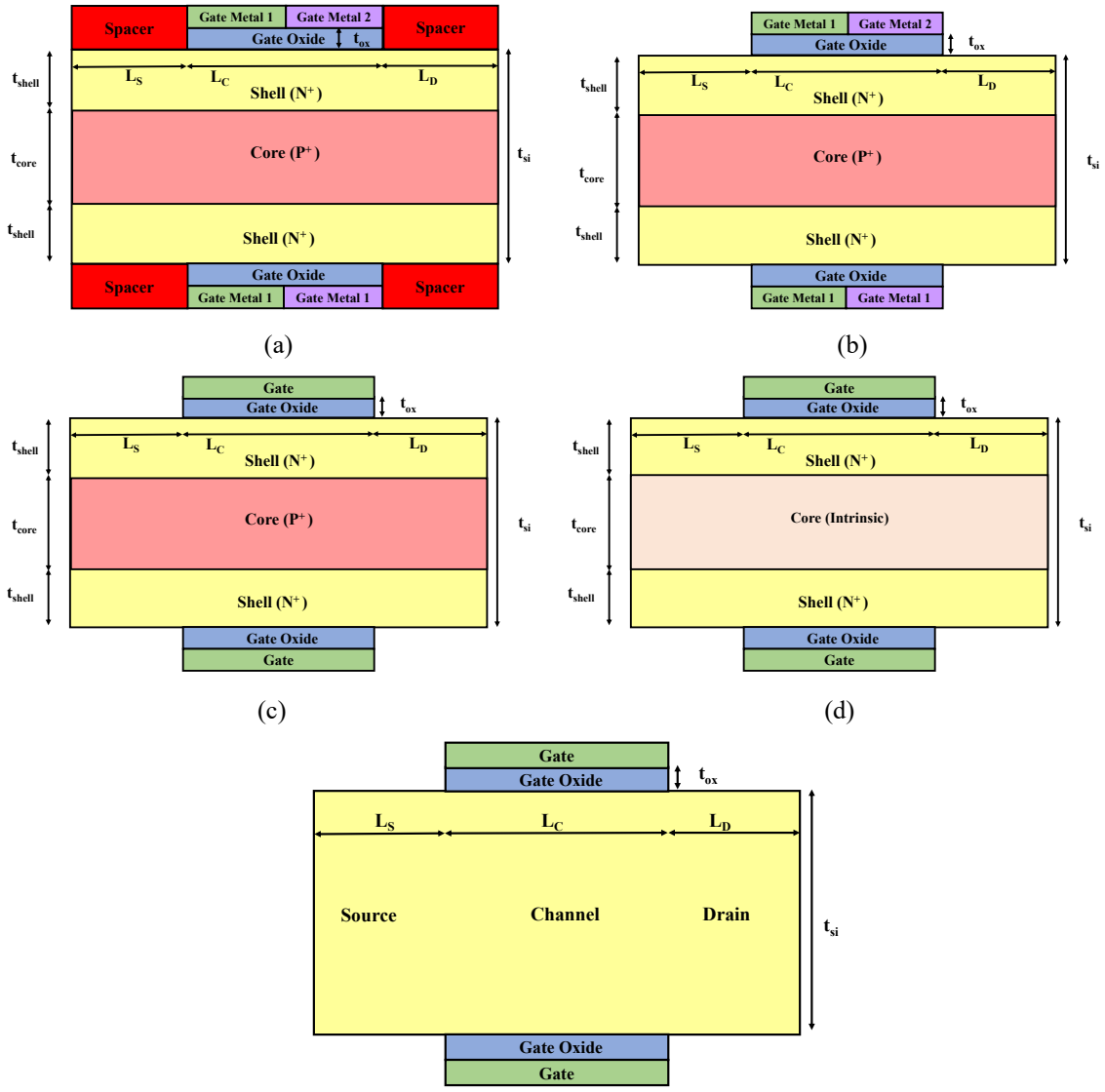


Fig. 2.15 2-D cross-sectional view of (a) Device D1, (b) Device D2, (c) Device D3, (c) Device D4 and (e) Device D5

Figure 2.16 (a) and (b) compare the transfer characteristics of Devices D1, D2, D3, D4, and D5 in linear and logarithm scales, respectively. Fig. 2.16 (a) indicate that Device D1 achieved the highest I_{DS} of 24.5 µA at V_{DS} = V_{GS} = 1 which is 11%, 77%, 54%, and 23% greater than devices D2, D3, D4, and D5, respectively. The reason behind this is that Device D1 incorporates a high-*k* GSS along with DMG, DMG architecture enhances the electric field at the source side, accelerating electrons in the channel, leading to higher I_{DS} whereas a high-*k* GSS reduces parasitic resistance under the spacer region due to the fringe field effect.

Furthermore, the incorporation of only DMG in Device D2 results in an improvement of 60%, 39%, and 11% compared to Devices D3, D4, and D5, respectively.

However, the presence of the core in Devices D3 and D4 reduces the active shell thickness, resulting in increased series resistance and reduced I_{DS} at $V_{DS} = V_{GS} = 1$ by 30% and 20%, respectively, compared to Device D5. The increase in series resistance due to large carrier depletion results in a more significant reduction in I_{DS} for Device D3 due to the presence of an opposite-doped core compared to Device D4 having an undoped core. It can be perceived from Fig. 2.16 (b) that Device D1 exhibits the lowest I_{OFF} ($\sim 10^{-5}$) at $V_{DS} = 1$ V, $V_{GS} = 0$ V as compared to Devices D2, D3, D4, and D5. Device D5 lacks volume depletion, meaning that during the OFF-state, the channel does not get fully depleted. As a consequence, it experiences a large I_{OFF} due to the parasitic BJT phenomenon, which contributes to higher I_{OFF}.

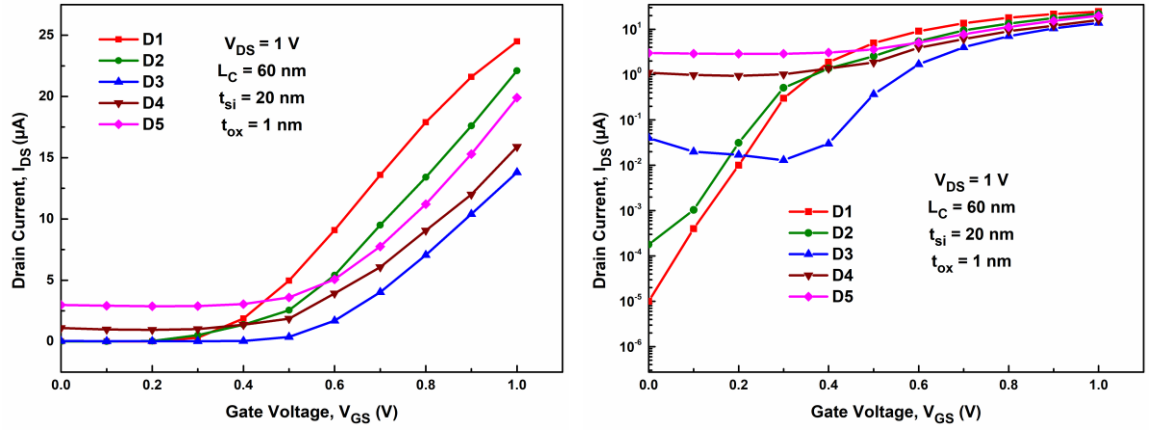


Fig. 2.16 Transfer characteristics comparison of Devices D1, D2, D3, D4, and D5 in (a) linear and (b) log scale

Additionally, Device D4 incorporates an intrinsic core, which means it does not have any additional doping in the core region. As a result, the active channel thickness is reduced, helping to deplete the channel in the OFF-state. This depletion in Device D4 mitigates the parasitic BJT phenomenon, leading to a substantial reduction of 63% in the I_{OFF} compared to Device D5. Device D3 demonstrates a remarkable reduction of 96% and 98% in I_{OFF} compared to devices D4 and D5, respectively. This significant reduction is due to the presence of an oppositely and equally doped p-type core between two n-type shells, leading to substantial carrier depletion.

Furthermore, the recombination of holes from the core and electrons from the shell region contributes to substantial depletion, resulting in an extremely low I_{OFF} in Device D3. When using DMG in Device D2, there is a significant decrease in I_{OFF} compared to Devices D3, D4, and D5. This is because the tunneling width on the drain side becomes larger, which prevents

L-BTBT of electrons from the channel to the drain when in the OFF-state. For Device D1, the incorporation of the high-*k* GSS along with DMG helps in further reduction of I_{OFF} as compared to devices D2, D3, D4, and D5, as the fringing field effect leads to depletion of the region under the high-*k* region in the OFF-state.

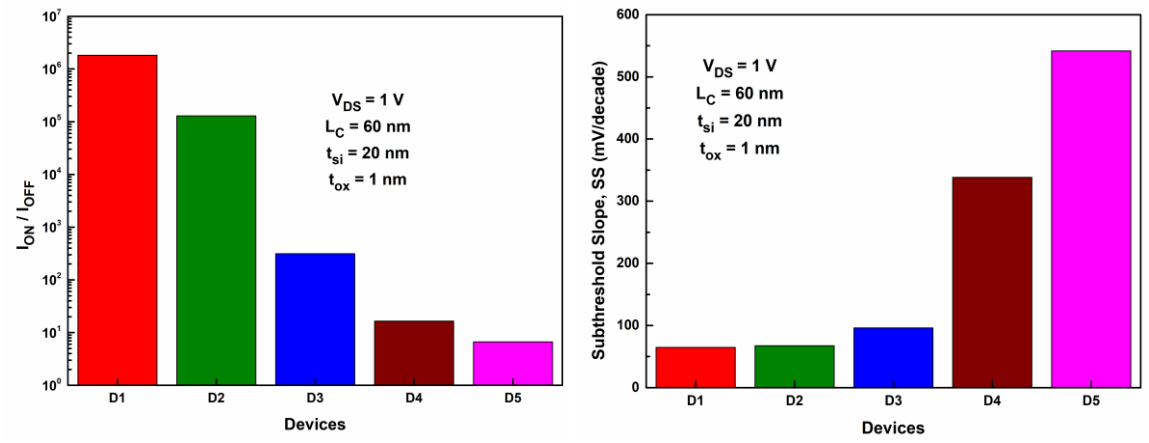


Fig. 2.17 Comparison of (a) I_{ON}/I_{OFF} ratio and (b) SS of Devices D1, D2, D3, D4, and D5

Figure 2.17 (a) and (b) illustrate I_{ON}/I_{OFF} ratio and SS for devices D1, D2, D3, D4, and D5, respectively. It can be perceived from Fig. 2.17 (a) that Device D1 has the highest I_{ON}/I_{OFF} ratio (~ 10^6) followed by Devices D2, D3, D4, and D5. It is portrayed in Fig. 2.17 (b) that the minimum SS is obtained as 64.8 mV/decade in Device D1. Device D1 benefits from DMG and high-*k* GSS techniques, which effectively lower the electric field at the drain side, mitigating SCEs and resulting in a reduced SS as compared to Devices D2, D3, D4, and D5. Device D1 shows significant improvements in SS compared to devices D2, D3, D4, and D5, with enhancements of 3%, 32%, 80%, and 88%, respectively.

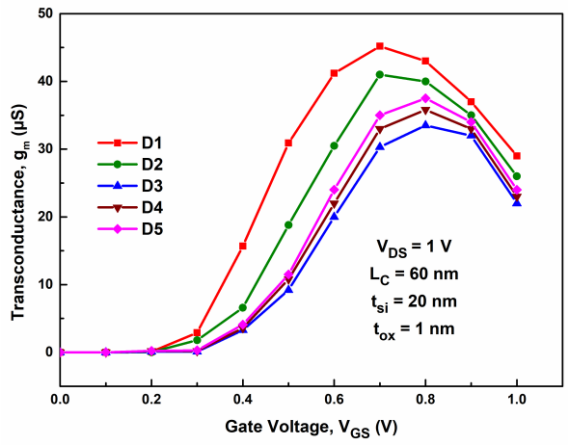


Fig. 2.18 Transconductance comparison of Devices D1, D2, D3, D4, and D5

Fig. 2.18 illustrates the transconductance (g_m) for all five devices. The maximum value of g_m at V_{GS} = 1 V is observed for Device D1 followed by Devices D2, D3, D4, and D5. The result shows significant enrichment of g_m in Device D1 by 11%, 31%, 26% and 20% at V_{GS} = 1 V as compared to Devices D2, D3, D4, and D5, respectively. This trend can be correlated with the fact that in Device D1, maximum g_m is observed due to a DMG and high-k GSS structure that improves carrier transport efficiency by modifying potential and electric field distribution along the channel as comprehensively discussed in the next section.

2.5.1 Devices internal analysis through horizontal cutline

The internal device analysis using horizontal cutline methodology in SILVACO ATLAS allows for a detailed exploration of the working physics of the device. By implementing the cutline analysis on Device D1, D2, D3, D4, and D5, at 1 nm below the oxide-channel interface in the horizontal direction, key device properties such as potential, electric field, and energy band profiles can be extracted and visualized. Fig. 2.19 illustrates a schematic representation of the horizontal cutline location within the Device D1 structure.

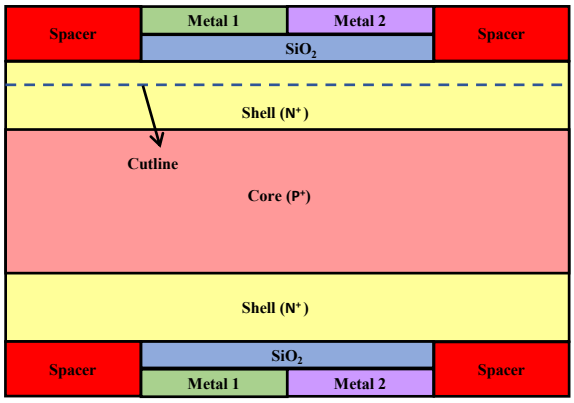
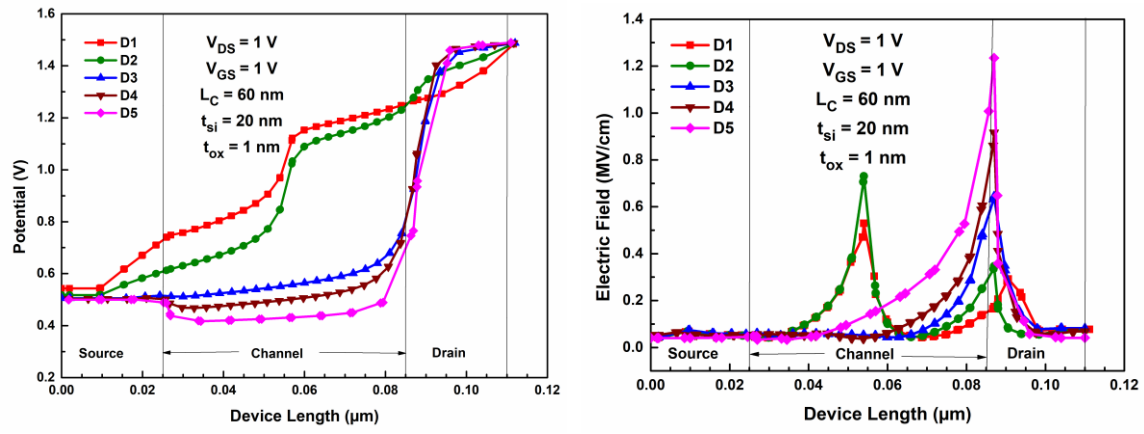


Fig. 2.19 Illustration of cutline taken at 1 nm below oxide-channel interface on Device D1

The potential profiles in ON-state along the device length for Devices D1, D2, D3, D4, and D5 are illustrated in Fig. 2.20 (a). It becomes evident that there is an abrupt transition at the interface of dissimilar gate metals in Devices D1 and D2 due to differences in gate work functions. This sharp transition facilitates a more effective modulation of the electric field in the channel. In contrast, Devices D3, D4, and D5 exhibit a smooth potential distribution from the source to the drain region.

Figure 2.20 (b) depicts the variation of the electric field along the device length of Devices D1, D2, D3, D4, and D5 in ON-state. As a consequence of the potential abruptness, Devices D1 and D2 display two electric field peaks at the M_1 and M_2 interfaces. These additional electric field peaks near the source region result in the accelerated motion of electrons in the channel,

leading to an enhanced drive current. On the other hand, the electric field peak near the drain region in Devices D1, D2, D3, D4, and D5 exhibits a decreasing trend, indicating a suppression SCEs in the same order. Notably, in Device D1, the electric field peak shifts toward the drain region due to fringing lines [113].



(a) (b)

Fig. 2.20 Comparison of (a) potential and (b) electric field distribution along device length of Devices D1, D2, D3, D4, and D5

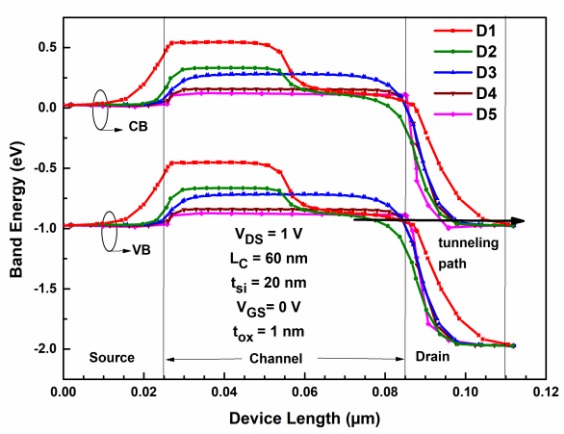


Fig. 2.21 Energy band profile comparison of Devices D1, D2, D3, D4, and D5

The energy band diagram along the device length of Devices D1, D2, D3, D4, and D5 is plotted in Fig. 2.21. Device D5 exhibits the smallest tunneling width, enabling significant tunneling from the channel region to the drain region at the channel-drain interface via the tunneling path. Consequently, this contributes to a large I_{OFF} due to increased leakage current. The incorporation of a heavily doped p-type core in Device D3 results in a larger tunneling width. This is attributed to the enhanced depletion of carriers at the channel-drain interface compared to Device D4, which has an intrinsic core.

Devices D1 and D2 have a higher source-to-channel barrier height compared to Devices D3-D5, as they have an additional electric field peak due to DMG structure. The enhancement of

the barrier is more in Device D1 due to the presence of a high-*k* GSS than in Device D2. This enhancement significantly restricts the movement of charge carriers in the OFF-state as compared to Device D2. Moreover, the lowest electric field peak at the channel-drain interface in Device D1 as compared to Devices D1, D2, D3, D4, and D4 leads to an enlarged tunneling width, inhibiting the triggering of the parasitic BJT phenomenon.

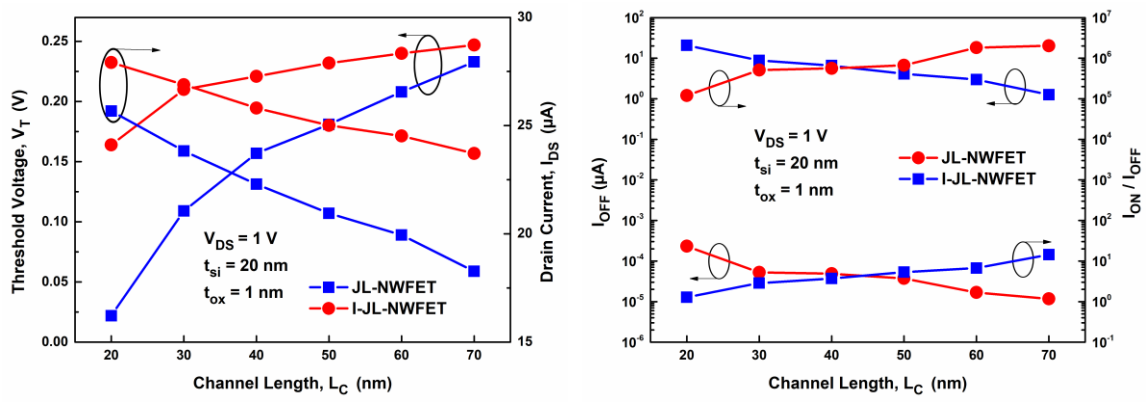
2.6 IMPACT OF CHANNEL LENGTH SCALING ON DEVICE PERFORMANCE

The device scaling represents a fundamental procedure within the semiconductor industry aimed at enhancing the transistor density on the chip. Therefore, it is imperative to assess how device scaling influences the performance of I-JL-NWFET. In this section, the impact of L_C scaling with variations ranging from 70 nm to 20 nm keeping t_{si} = 20 nm, $L_{S/D}$ = 25 nm, and t_{ox} = 1 nm as constant on the electrical, analog/RF and linearity parameters of I-JL-NWFET is analyzed. Furthermore, the results are also compared with that of conventional JL-NWFET.

2.6.1 Impact of channel length scaling on electrical parameters

In this subsection, the impact of L_C on the electrical characteristics such as V_T, I_{DS}, I_{OFF}, SS, and DIBL of I-JL-NWFET and JL-NWFET are analyzed. Fig. 2.22 (a) illustrates the influence of L_C variation on the V_T and I_{DS} of I-JL-NWFET and JL-NWFET. The observed trend in Fig. 2.22 (a) indicates a significant decrease in the V_T for conventional JL-NWFET when scaling down the L_C whereas I-JL-NWFET shows more consistent and lower variations in V_T. Notably, a sudden decline in V_T at an L_C of 20 nm suggests a loss of control of the gate voltage over the channel with a relatively large channel thickness. The I_{DS} for the scaled L_C is plotted in Fig. 2.22 (a) at V_{GS} = 1 V. It corresponds to the maximum I_{ON} of junctionless transistors as they are normally designed so that they operate in flat band condition in the ON-state.

The curve demonstrates that the I_{DS} of both I-JL-NWFET and JL-NWFET increases with the scaling of L_C. The I_{DS} of I-JL-NWFET surpasses that of JL-NWFET as the L_C is scaled down. Additionally, I-JL-NWFET shows enhancement of I_{DS} due to the incorporation of DMG and high-*k* GSS, implying better control over the flow of current through the channel. The impact of L_C variation on the I_{OFF} and I_{ON}/I_{OFF} ratio of I-JL-NWFET and JL-NWFET is illustrated in Fig. 2.22 (b). In the case of JL-NWFET, the I_{OFF} is higher than that of I-JL-NWFET as the L_C is scaled down. This is attributed to inadequate volume depletion in the large channel thickness and the initiation of parasitic BJT effects [105]. Typically, smaller L_C leads to higher I_{OFF}, which can be a concern for power efficiency and heat generation in integrated circuits.



(a) (b)

Fig. 2.22 Plots of (a) threshold voltage and drain current (b) I_{OFF} and I_{ON}/I_{OFF} ratio of I-JL-NWFET and JL-NWFET for different channel lengths

Conversely, I-JL-NWFET shows significantly better I_{OFF} variation at scaled L_C due to the presence of an opposite dope core which helps in volume depletion during OFF-state. Additionally, DMG suppresses SCEs and Hot Carrier Effects (HCEs) more effectively and high-k material in the spacer region helps to deplete the channel beyond the gate edge. However, at a 20 nm channel length, there is a significant increase in the I_{OFF} of I-JL-NWFET, indicating poor electrostatic control of gate voltage. Consequently, the I_{ON}/I_{OFF} ratio of JL-NWFET and I-JL-NWFET decreases with decreasing L_C as portrayed in Fig. 2.22 (b). Besides this, I-JL-NWFET depicts higher I_{ON}/I_{OFF} than JL-NWFET at scaled L_C.

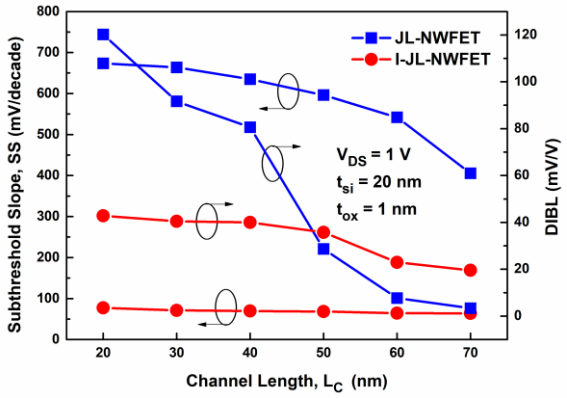


Fig. 2.23 Plots of (a) SS and DIBL of I-JL-NWFET and JL-NWFET for different channel lengths

It can be noted from Fig. 2.23 that SS is lower for I-JL-NWFET than JL-NWFET. In JL-NWFET, the SS rises with the scaling of L_C because of an increase in I_{OFF}. This, in turn, leads to a reduction in the slope of the I_{DS}-V_{GS} characteristics as the device transitions from the OFF-state to the ON-state. On the contrary, I-JL-NWFET shows less variation of SS at scaled L_C, implying improved subthreshold characteristics due to DMG and high-k GSS. The DIBL is expressed as [12]

$$DIBL = \frac{V_T\left(V_{DS} = 0.05V\right) - V_T\left(V_{DS} = 1V\right)}{\left(V_{DS} = 1V\right) - \left(V_{DS} = 0.05V\right)} \text{ mV/V} \tag{2.2}$$

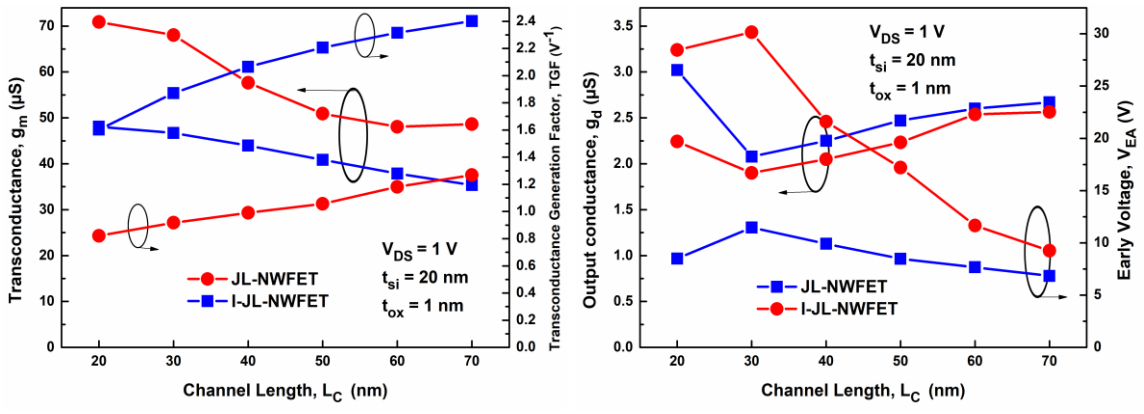
The DIBL is quite severe in JL-NWFET as compared to I-JL-NWFET with scaling of L_C as demonstrated in Fig. 2.23. The reduction in DIBL effect in I-JL-NWFET is due to the presence of the oppositely doped core in the channel and DMG structure. The inclusion of an oppositely doped core decreased the active channel thickness of the I-JL-NWFET, improving gate control effectiveness and reducing the influence of drain voltage on the channel's electrostatics. As a result, the narrow conduction area led to a significant reduction in DIBL [22]. Additionally, the DMG structure aids in mitigating DIBL by providing a screening effect against drain voltage [12].

2.6.2 Impact of channel length scaling on analog/RF parameters

This subsection investigates the impact of L_C on the analog/RF parameters such as transconductance (g_m), Transconductance Generation Factor (TGF), output conductance (g_d), early voltage (V_{EA}), total gate to gate capacitance (C_{GG}) and cut-off frequency (f_T) of the I-JL-NWFET and JL-NWFET.

The TGF holds significance in assessing the power needed to achieve high-speed concerning gate bias. TGF plays a pivotal role in determining how the current can be effectively utilized to attain a desired transconductance. The g_m and TGF are expressed as [113]

$$TGF = \frac{g_m}{I_{DS}} \tag{2.3}$$



(a) (b)

Fig. 2.24 Plots of (a) transconductance and TGF (b) output conductance and early voltage of I-JL-NWFET and JL-NWFET for different channel lengths

Figure 2.24 (a) displays the influence of L_C variation on the g_m and TGF of I-JL-NWFET and JL-NWFET at V_{GS} = 1 V. With the scaling of L_C, the g_m of both I-JL-NWFET and JL-NWFET

increases, with g_m of I-JL-NWFET exceeding that of JL-NWFET. This is attributed to the enhanced I_{DS} in I-JL-NWFET than JL-NWFET as explained in Fig. 2.22 (a). The TGF exhibits a greater decrease in I-JL-NWFET compared to JL-NWFET as L_C is scaled down. The decrease in TGF is mainly attributed to the rising I_{DS} as L_C decreases, which counteracts any potential improvement in g_m.

Generally, analog circuit devices are frequently operated in the saturation region. While I_{DS} typically remains unaffected by V_{DS} in the saturation region, the impact of V_{DS} on channel electrostatics introduces variations in I_{DS}, attributed to short-channel behavior. Hence, to understand the relationship between V_{DS} and I_{DS}, g_d is evaluated. Additionally, the V_{EA} is crucial in the analysis and design of analog circuits, as it helps in determining the intrinsic gain of the device. The g_d and V_{EA} are formulated as follows [113]

$$g_d = \frac{\partial I_{DS}}{\partial V_{DS}} \text{ at } V_{GS} = \text{constant} \tag{2.4}$$

$$V_{EA} = \frac{I_D}{g_d} \tag{2.5}$$

The impact of L_C variation on the g_d and V_{EA} of I-JL-NWFET and JL-NWFET at V_{DS} = 1 V is portrayed in Fig. 2.24 (b). The g_d of I-JL-NWFET reduces more than that of JL-NWFET as on scaling of L_C due to reduced DIBL in I-JL-NWFET than in JL-NWFET as observed in Fig. 2.23. Consequently, reduced g_d increases V_{EA} of I-JL-NWFET than that of JL-NWFET as on scaling of L_C. However, scaling of L_C below 30 nm may increase effect of drain bias leading to increase in g_d and decrease in V_{EA} in both I-JL-NWFET and JL-NWFET.

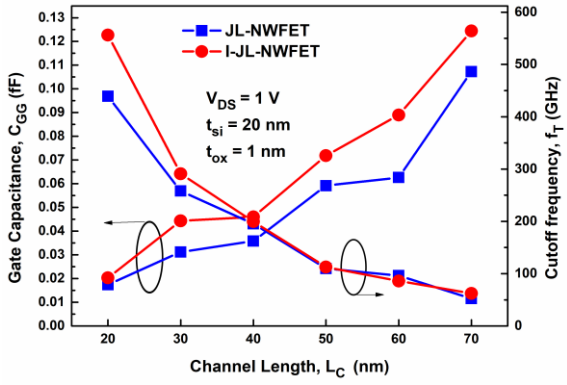


Fig. 2.25 Plots of gate capacitance and cut-off frequency of I-JL-NWFET and JL-NWFET for different channel lengths

The C_{GG} as parasitic capacitance and f_T are important parameters for RF applications. C_{GG} in RF amplifiers may cause RF amplifiers to have low gain due to parasitic loss. The f_T is defined

as the frequency at which the short circuit current gain drops to 0 dB. Mathematically, C_{GG} and f_T are formulated as [114]

$$C_{GG} = C_{GS} + C_{GD} \tag{2.6}$$

$$f_T = \frac{g_m}{2\pi C_{GG}} \tag{2.7}$$

where C_{GS} and C_{GD} are parasitic capacitances between gate-to-source and gate-to-drain terminals, respectively. Fig. 2.25 shows the influence of varying L_C on the C_{GG} and f_T of I-JL-NWFET and JL-NWFET at V_{GS} = 1 V. The increase of C_{GG} of I-JL-NWFET exceeds that of JL-NWFET due to the presence of high-*k* GSS which increases capacitance at any given L_C. Moreover, the observed increase of f_T of I-JL-NWFET than that of JL-NWFET on scaling L_C is mainly due to increase in g_m as observed in Fig. 2.24 (a).

2.6.3 Impact of channel length scaling on linearity parameters

The impact of scaling of L_C on linearity parameters of the I-JL-NWFET and JL-NWFET are analyzed in this subsection. The fundamental parameters, g_{m2} and g_{m3}, are significantly influenced during high-frequency operation, leading to distortion and indicating nonlinearity. To enhance linearity performance, the peak values of g_{m2} and g_{m3} must be as low as possible. The g_{m2} and g_{m3} are expressed as [115]

$$g_{m2} = \frac{\partial^2 I_{DS}}{\partial V_{GS}^2} \tag{2.8}$$

$$g_{m3} = \frac{\partial^3 I_{DS}}{\partial V_{GS}^3} \tag{2.9}$$

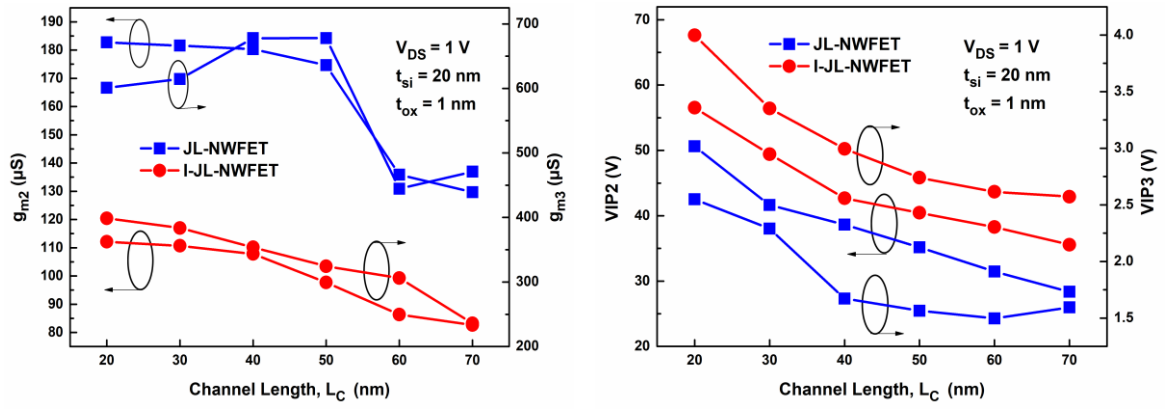
Figure 2.26 (a) depicts the influence of L_C variation on the peak value of g_{m2} and g_{m3} of I-JL-NWFET and JL-NWFET. The peak value of g_{m2} of I-JL-NWFET and JL-NWFET occurs at 0.6 V and 0.7 V, respectively while the peak value of g_{m3} of I-JL-NWFET and JL-NWFET occurs at 0.4 V and 0.5 V, respectively. The peak value of g_{m2} and g_{m3} increases on decreasing L_C due to less V_{GS} control on large channel thickness. Moreover, I-JL-NWFET exhibits low peak value of g_{m2} and g_{m3} than that of JL-NWFET at any given L_C, owing to inclusion of oppositely doped facilitating more effective V_{GS} control over channel region.

The set of metrics employed for evaluating distortion characteristics from DC parameters includes voltage intercept points (VIP2 and VIP3). The VIP2 signifies the extended input gate voltage where the voltage level of the fundamental signal equals that of the second-order harmonic signal. Beyond this crucial voltage, distortion is influenced by the amplitude of the first-order tone. The VIP3 represents the extrapolated input gate voltage at which the voltage

levels of the fundamental and third-order harmonic signals become comparable. For high linearity performance and minimal distortion operation, a higher VIP2 and VIP3 is essential. These metrics can be expressed as follows [115]

$$VIP2 = 4 \times \frac{g_m}{g_{m2}} \tag{2.10}$$

$$VIP3 = \sqrt{24 \times \frac{g_m}{g_{m3}}} \tag{2.11}$$



(a) (b)

Fig. 2.26 Plots of (a) g_{m2} and g_{m3} (b) VIP2 and VIP3 of I-JL-NWFET and JL-NWFET for different channel lengths

Figure 2.26 (b) illustrates the impact of L_C variation on the peak value of VIP2 and VIP3 of I-JL-NWFET and JL-NWFET. The peak value of VIP2 of I-JL-NWFET and JL-NWFET is observed at 0.7 V and 0.8 V, respectively while the peak value of VIP3 of I-JL-NWFET and JL-NWFET is observed at 0.6 V and 0.7 V, respectively. The peak value of VIP2 and VIP3 observed in I-JL-NWFET increases on decreasing L_C due enhancement in g_m that counteracts any increases in g_{m2} and g_{m3}.

The third-order input intercept point (IIP3) denotes the extrapolated input power level at which the powers of first and third-order harmonics become equal. IMD3, representing third-order intermodulation distortion, signifies the extrapolated intermodulation distortion power where the first and third-order intermodulation powers are equal. Eqns. (1.14) and (1.15) are employed to evaluate IIP3 and IMD3, respectively, with R_s assumed to be 50 Ω in analog and RF applications [115]. Achieving a high IIP3 value and a low IMD3 value is desirable for enhancing linear characteristics.

$$IIP3 = \frac{2}{3} \times \left[\frac{g_m}{g_{m3} \times R_S} \right] \tag{2.12}$$

$$IMD3 = \left[\frac{9}{2} \times (VIP3)^2 \times g_{m3} \right] \times R_S \tag{2.13}$$

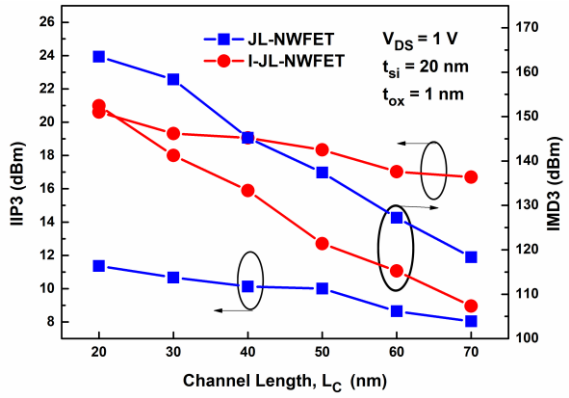


Fig. 2.27 Plots of IIP3 and IMD3 of I-JL-NWFET and JL-NWFET for different channel lengths

Figure 2.27 demonstrates the impact of L_C variation on the peak value of IIP3 and IMD3 of I-JL-NWFET and JL-NWFET. The peak value of IIP3 of I-JL-NWFET and JL-NWFET is observed at 0.8 V and 0.9 V, respectively while the peak value of IMD3 of I-JL-NWFET and JL-NWFET is observed at 0.6 V and 0.7 V, respectively. Due to increasing g_m on decreasing L_C, the peak value of IIP3 in I-JL-NWFET increases than that in JL-NWFET. Furthermore, the peak value of IMD3 of I-JL-NWFET increases on decreasing L_C due to increasing g_{m3} and VIP3. I-JL-NWFET exhibits low peak value of IMD3 compared to JL-NWFET owing to low peak value of g_{m3} in I-JL-NWFET as observed in Fig. 2.26 (a).

At 30 nm of L_C, I-JL-NWFET demonstrates optimal values for I_{OFF}, I_{ON}/I_{OFF}, and DIBL. Consequently, L_C of the I-JL-NWFET is fixed at 30 nm for further analysis in subsequent sections.

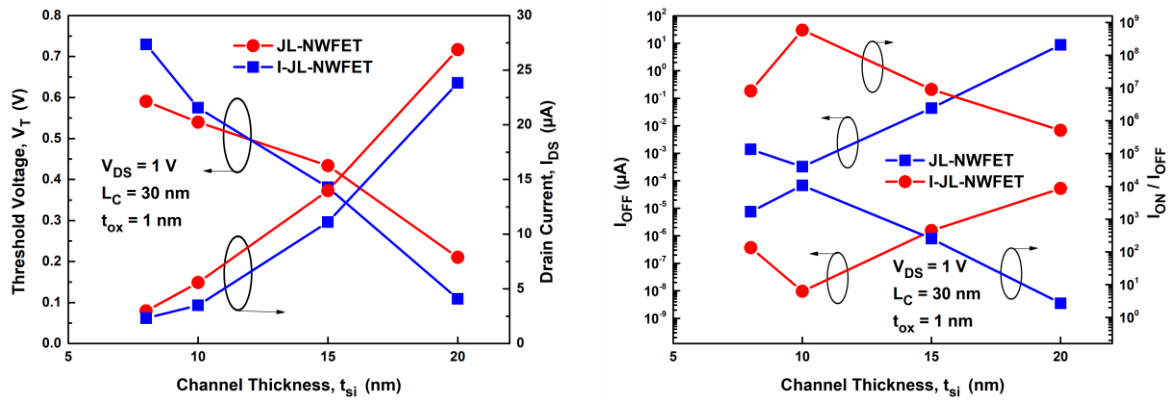
2.7 IMPACT OF CHANNEL THICKNESS SCALING ON DEVICE PERFORMANCE

The design of JL-NWFET is significantly influenced by the t_{si}, a crucial parameter essential for operation in various modes. Furthermore, the key concerns associated with JL-NWFET, namely insufficient volume depletion and leakage current, are strongly dependent on the t_{si} [107]. The impact of t_{si} on the electrical, analog/RF and linearity characteristics of both JL-NWFET and I-JL-NWFET is analyzed by varying it from 20 nm to 8 nm keeping L_C = 30 nm,

$L_{S/D}$ = 25 nm, and t_{ox} = 1 nm constant. Moreover, t_{core} in I-JL-NWFET is varied as half of t_{si} during each scaling of t_{si}.

2.7.1 Impact of channel thickness scaling on electrical parameters

In this subsection, the analysis focuses on the impact of t_{si} on the electrical characteristics of I-JL-NWFET and JL-NWFET, including I_D, V_T, I_{OFF}, SS, and DIBL. The impact of t_{si} scaling results in an increase in V_T for both JL-NWFET and I-JL-NWFET, as depicted in Fig. 2.28 (a). In the case of large t_{si} of JL-NWFET, there is insufficient volume depletion, requiring less gate voltage to turn the transistor ON. I-JL-NWFET exhibits less variation in V_T as t_{si} is scaled, compared to JL-NWFET because of the presence of an opposite doped core that reduces active shell thickness for conduction.



(a) (b)

Fig. 2.28 Plots of (a) threshold voltage and drain current (b) I_{OFF} and I_{ON}/I_{OFF} ratio of I-JL-NWFET and JL-NWFET for different channel thicknesses

Furthermore, as shown in Fig. 2.28 (a), I_{DS} decreases with a reduction in t_{si} for both JL-NWFET and I-JL-NWFET. In the case of JL-NWFET, where bulk conduction occurs, the decrease in cross-sectional area for current flow leads to a decrease in I_{DS}. Conversely, in I-JL-NWFET, which features a DMG, the presence of dual materials enhances carrier mobility. This results in an increase in I_{DS} compared to JL-NWFET, despite the presence of the opposite doped core that reduces the active shell thickness for conduction. Fig. 2.28 (b) illustrate the influence of t_{si} variation on the I_{OFF} and I_{ON}/I_{OFF} ratio.

The higher I_{OFF} in JL-NWFET with a t_{si} of 20 nm is attributed to insufficient volume depletion and the initiation of the parasitic BJT phenomenon. This effect diminishes with the scaling of t_{si}, allowing the gate voltage to more effectively control the channel. However, in I-JL-NWFET, the presence of an oppositely doped core aids in carrier depletion in the OFF-state. Additionally, the utilization of a DMG, including high-k material in the spacer region, further

contributes to reducing I_{OFF} compared to JL-NWFET on the scaling of t_{si}. Both JL-NWFET and I-JL-NWFET experience an increase in I_{OFF} at a t_{si} of 8 nm due to a rise in SCEs. However, it is worth emphasizing that the I_{OFF} recorded for I-JL-NWFET at a t_{si} of 8 nm is comparatively lower than that observed in JL-NWFET under the same conditions. Consequently, I_{ON}/I_{OFF} ratio in I-JL-NWFET is higher than JL-NWFET.

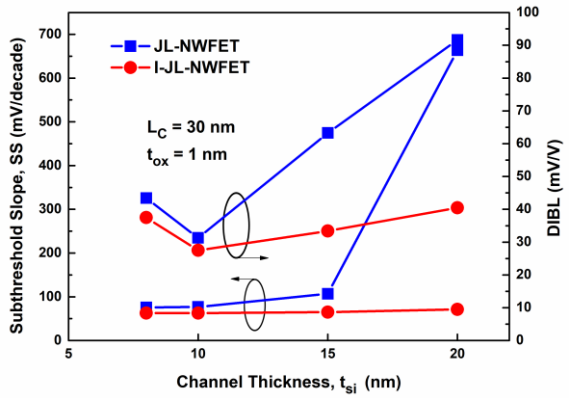


Fig. 2.29 Plots of SS and DIBL of I-JL-NWFET and JL-NWFET for different channel thicknesses

The impact of varying t_{si} on SS and DIBL is shown in Fig. 2.29. The SS in JL-NWFET decreases drastically when t_{si} is scaled due to the significant reduction in the OFF-state current. Additionally, SS also increases since scaling of t_{si} beyond 10 nm increases I_{OFF} in JL-NWFET. However, SS in I-JL-NWFET shows less sensitivity towards scaled t_{si} due to improved I_{OFF} as discussed in Fig. 2.28 (b). Furthermore, decreasing the nanowire t_{si} improves the efficacy of gate control, leading to a diminished impact of the drain voltage on the electrostatics in the channel region. Consequently, the effective gate control provided by the smaller t_{si} markedly reduces DIBL in JL-NWFET till 10 nm of t_{si} beyond which it increases due to reduced control of gate voltage over the channel region, as illustrated in Fig. 2.29. Nevertheless, in the case of I-JL-NWFET, DIBL exhibits less sensitivity on scaling t_{si}. This is attributed to the presence of the core with opposite doping, which effectively reduces the active channel region, and DMG, which improves gate control on the reduced active channel region.

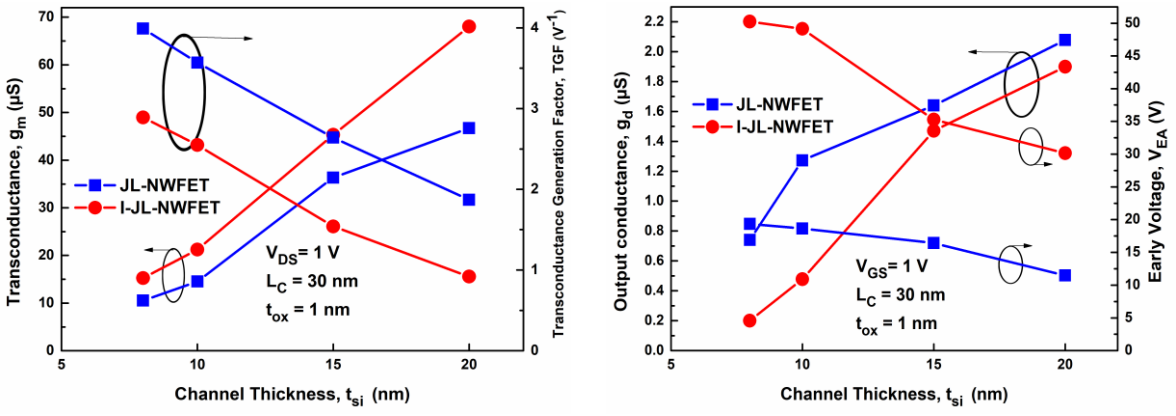
Table 2.5. Performance comparison of the proposed I-JL-NWFET with JL-NWFET and other reported devices

Parameters	Experimental JL-NWFET [9]	Re-S/D-JL-GAA MOSFET [30]	DPGAA MOSFET [116]	JL-NWFET	I-JL-NWFET (This work)
I_{OFF} (A)	1×10^{-15}	9.5×10^{-10}	5.34×10^{-13}	3.25×10^{-10}	9.55×10^{-15}
I_{ON}/I_{OFF}	1×10^{6}	1.2×10^{4}	2.14×10^{8}	1.07×10^{4}	5.83×10^{8}
SS (mV/decade)	64	73.63	69.96	76.83	62.75
DIBL (mV/V)	-	49.47	-	31.30	27.51

Table 2.5 compares the electrical performance of I-JL-NWFET with JL-NWFET, experimental work [9], Recessed Source/Drain Junctionless Gate All Around (Re-S/D-JL-GAA) MOSFET [30] and Dielectric Pocket Gate All Around (DPGAA) MOSFET [116]. It can be observed that I-JL-NWFET showcases higher I_{ON}/I_{OFF}, and less value of I_{OFF}, SS and DIBL when compared to other published work. The superior electrical performance demonstrated by the I-JL-NWFET underscores its viability for various electronic applications.

2.7.2 Impact of channel thickness scaling on analog/RF parameters

The impact of scaling of t_{si} on analog/RF parameters such as g_m, TGF, g_d, V_{EA}, C_{GG} and f_T of the I-JL-NWFET and JL-NWFET is analyzed in this subsection. Fig. 2.30 (a) illustrates the variation of t_{si} on g_m and TGF of I-JL-NWFET and JL-NWFET at V_{GS} = 1 V. The g_m of I-JL-NWFET and JL-NWFET decreases on scaling of t_{si} due to reduction of I_D. Moreover, g_m of I-JL-NWFET surpasses than that of JL-NWFET attributed to enhanced I_{DS} at any given t_{si}, as exhibited in Fig. 2.30 (a).



(a) (b)

Fig. 2.30 Plots of (a) transconductance and TGF (b) output conductance and early voltage of I-JL-NWFET and JL-NWFET for different channel thicknesses

Consequently, TGF of I-JL-NWFET and JL-NWFET increases as t_{si} is scaled down due to reduced I_{DS}. Additionally, I-JL-NWFET exhibits higher TGF compared to JL-NWFET at any given t_{si}, due to DMG structure that increases carrier mobility in the channel. Fig. 2.30 (b) illustrates g_d and V_{EA} of I-JL-NWFET and JL-NWFET at V_{DS} = 1 V on varying t_{si}. The g_d of I-JL-NWFET and JL-NWFET decreases on scaling of t_{si} due to reduction of I_{DS} as observed in Fig. 2.30 (a). Moreover, g_d of I-JL-NWFET is less compared to JL-NWFET at any given t_{si}, attributed due to the enhanced control of V_{GS} compared to V_{DS} on a smaller channel thickness. Consequently, V_{EA} of I-JL-NWFET surpasses that of JL-NWFET due to lower g_d at any given

$t_{si.}$ It is also observed that there is a marginal reduction of g_d below 10 nm of t_{si}, leading to minimal change in V_{EA} of I-JL-NWFET.

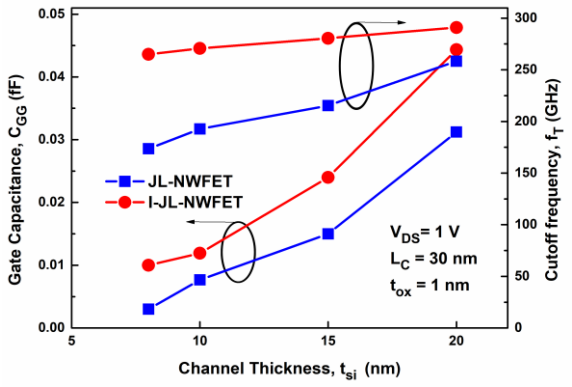


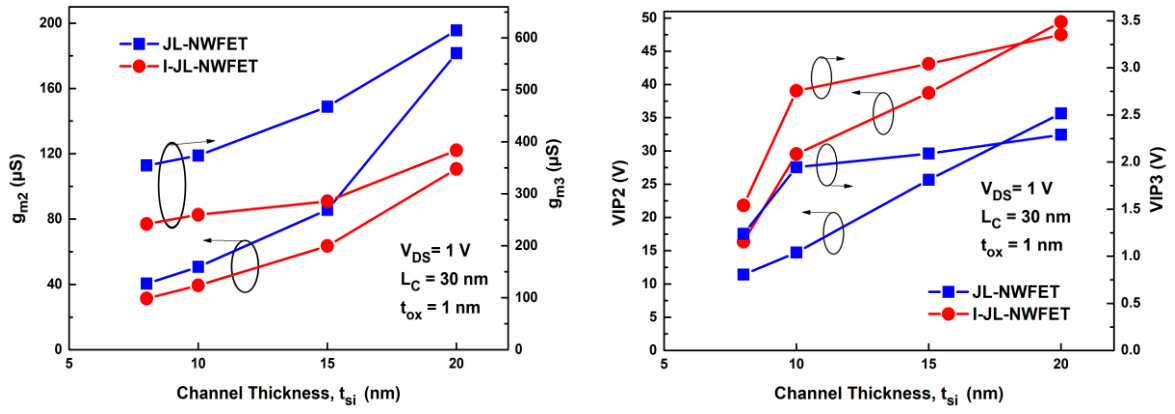
Fig. 2.31 Plots of gate capacitance and cut-off frequency of I-JL-NWFET and JL-NWFET for different channel thicknesses

Figure 2.31 depicts the impact of variation of t_{si} on C_{GG} and f_T of I-JL-NWFET and JL-NWFET at V_{GS} = 1 V. At any given t_{si}, I-JL-NWFET exhibit higher C_{GG} compared to JL-NWFET, primarily because of the inclusion of a high-*k* GSS, which enhances capacitance between gate to source and gate to drain. Furthermore, the noticeable enhancement in f_T of I-JL-NWFET compared to JL-NWFET on scaling t_{si} is predominantly attributed to the increase in g_m, as depicted in Fig. 2.30 (a).

2.7.3 Impact of channel thickness scaling on linearity parameters

The analysis of this subsection focuses on the impact of variation of t_{si} on the linearity parameters of I-JL-NWFET and JL-NWFET, consisting g_{m2}, g_{m3}, VIP2, VIP3, IIP3 and IMD3. Figure 2.32 (a) demonstrates the influence of t_{si} variation on the peak value of g_{m2} and g_{m3} of I-JL-NWFET and JL-NWFET. The peak value of g_{m2} of I-JL-NWFET and JL-NWFET occurs at 0.6 V and 0.7 V, respectively while the peak value of g_{m3} of I-JL-NWFET and JL-NWFET is observed at 0.4 V and 0.5 V, respectively.

On decreasing t_{si}, I-JL-NWFET exhibits lower peak value of g_{m2} and g_{m3} compared to JL-NWFET due to enhanced V_{GS} control over smaller channel leading to reduced harmonic distortion [115]. Fig. 2.32 (b) shows the impact of varying t_{si} on the peak value of VIP2 and VIP3 of I-JL-NWFET and JL-NWFET. The peak value of VIP2 for I-JL-NWFET occurs at 0.7 V, whereas for JL-NWFET, it occurs at 0.8 V. Similarly, the peak value of VIP3 for I-JL-NWFET is observed at 0.6 V, while for JL-NWFET, it is observed at 0.7 V. I-JL-NWFET displays higher peak value of VIP2 and VIP3 compared to JL-NWFET due to lower peak value of g_{m2} and g_{m3}.



(a) (b)

Fig. 2.32 Plots of (a) g_{m2} and g_{m3} (b) VIP2 and VIP3 of I-JL-NWFET and JL-NWFET for different channel thicknesses

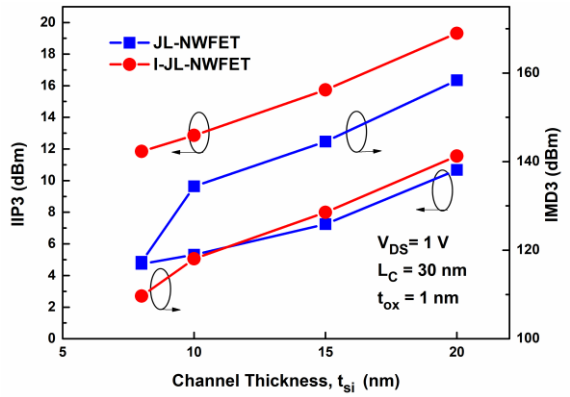


Fig. 2.33 Plots of IIP3 and IMD3 of I-JL-NWFET and JL-NWFET for different channel thicknesses

Figure 2.33 illustrates the impact of t_{si} variation on the peak value of IIP3 and IMD3 of I-JL-NWFET and JL-NWFET. The peak value of IIP3 of I-JL-NWFET and JL-NWFET is observed at 0.8 V and 0.9 V, respectively while the peak value of IMD3 of I-JL-NWFET and JL-NWFET is observed at 0.6 V and 0.7 V, respectively. Due to decreasing g_m on reducing t_{si}, the peak value of IIP3 in JL-NWFET reduces more than that in I-JL-NWFET. Furthermore, the peak value of IMD3 of I-JL-NWFET decreases on reducing t_{si} due to reducing VIP3. Notably, I-JL-NWFET demonstrates a lower peak value of IMD3 compared to JL-NWFET at any given t_{si}, owing to low peak value of g_{m3} in I-JL-NWFET as observed in Fig. 2.32 (a).

I-JL-NWFET exhibits optimum value of I_{OFF}, I_{ON}/I_{OFF} and DIBL at 30 nm of L_C and 10 nm of t_{si}. Moreover, analog/RF and linearity parameters depend on electrical parameters. Therefore, the L_C and t_{si} of I-JL-NWFET are optimized at 30 nm and 10 nm, respectively for subsequent performance analysis.

2.8 TEMPERATURE IMPACT ON DEVICE PERFORMANCE

The temperature dependence analysis of nano-scale devices offers a more profound understanding of the intrinsic performance of the device, allowing for insights into its performance under varying temperature conditions. This section delves into exploring the impact of temperature on the characteristics of electrical, analog/RF, and linearity parameters in I-JL-NWFET and JL-NWFET.

2.8.1 Impact of temperature on electrical parameters

In this subsection, the impact of temperature on I-JL-NWFET and JL-NWFET is analyzed on the electrical characteristics such as I_{DS}, V_T, I_{OFF}, SS and DIBL by varying the temperature from 200 K to 500 K. The dependence of temperature on transfer characteristics of I-JL-NWFET and JL-NWFET in linear and log scales are illustrated in Fig. 2.32 (a) and (b), respectively. As the temperature rises, I_{DS} initially rises at a specific V_{GS} and subsequently declines with further temperature increases. This point is called the Zero Temperature Coefficient (ZTC) at which I_{DS} demonstrates almost no dependence on temperature [117]. Below the ZTC point, an increase in temperature leads to a decrease in V_T, causing an increase in I_D.

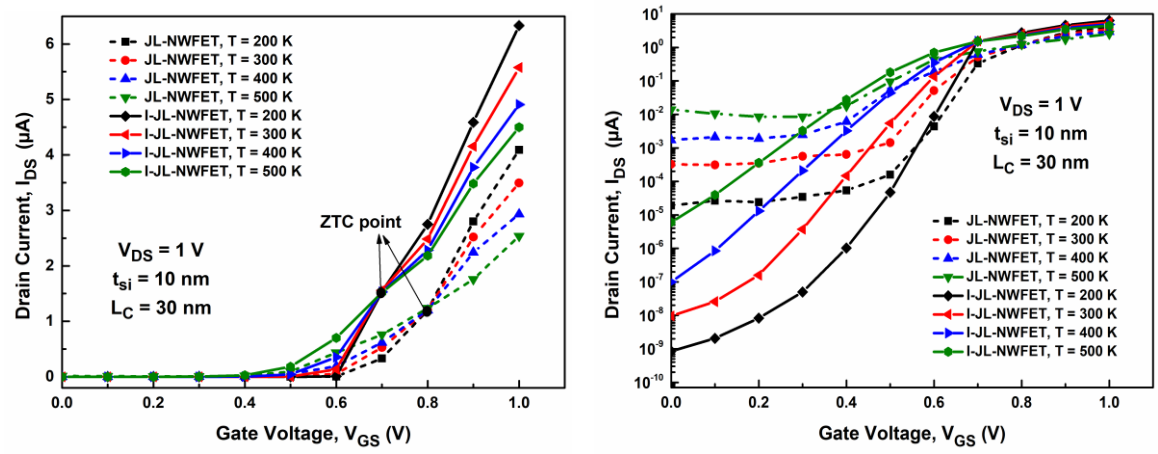


Fig. 2.34 Transfer characteristics of I-JL-NWFET and JL-NWFET for different temperatures in (a) linear scale and (b) log scale

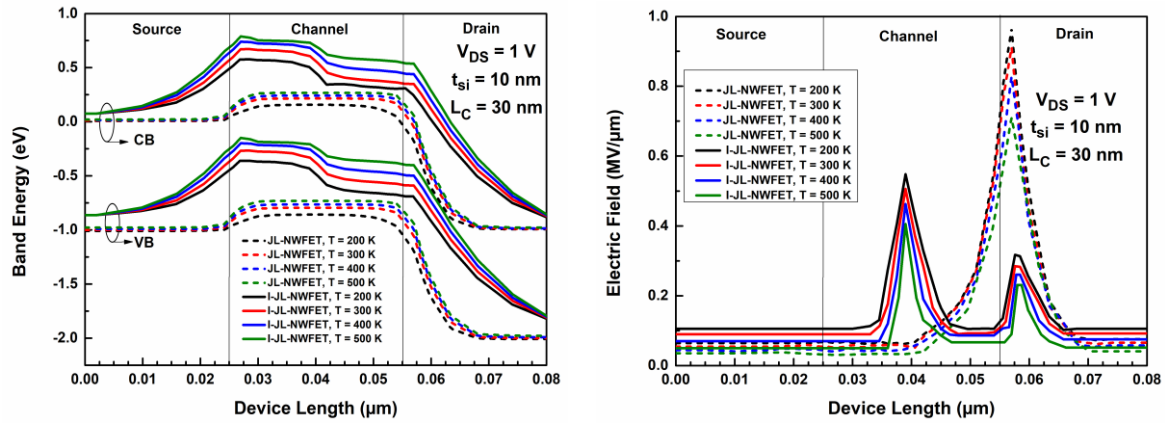
Conversely, beyond the ZTC point, I_{DS} decreases due to a decline in electron mobility with rising temperature. The ZTC of I-JL-NWFET and JL-NWFET are observed at 0.7 V and 0.8 V, respectively. In JL-NWFET, the primary degradation mechanism for electron mobility is phonon scattering, and this effect varies proportionally with $T^{-3/2}$ [117]. However, the I_{DS} (V_{GS} = 1 V) of I-JL-NWFET is comparatively high in comparison to JL-NWFET attributed to the

incorporation of DMG that enhances the current driving capability in the device as observed in Fig. 2.32 (a). Moreover, it is found that the variation of I_{DS} at V_{GS} = 1 V in I-JL-NWFET and JL-NWFET is 29% and 31.8%, respectively with an increase in temperature from 200 K to 500 K.

This underscores the comparatively lower sensitivity of I-JL-NWFET to temperature variations when compared to JL-NWFET. Additionally, I_{OFF} (V_{GS} = 0 V) increases in both I-JL-NWFET and JL-NWFET with an increase in temperature from 200 K to 500 K as depicted in Fig. 2.34 (b). This is attributed to the increases in intrinsic carrier concentration (n_i) which is a dependent factor of temperature and expressed as [118]

$$n_i = \exp\left[\frac{-E_g}{2KT}\right] \tag{2.14}$$

where 'K' is the Boltzmann constant, E_g is bandgap of semiconductor, and 'T' is the absolute temperature. The I_{OFF} in I-JL-NWFET is comparable less in comparison to JL-NWFET due to an oppositely doped core which aids in depleting the channel during the OFF state.



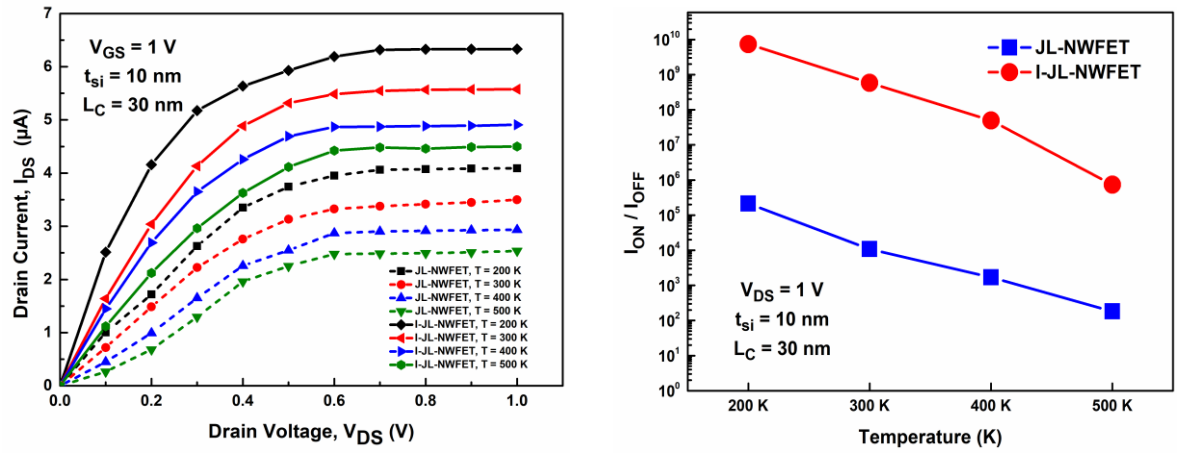
(a) (b)

Fig. 2.35 Plots of (a) energy band and (b) electric field of I-JL-NWFET and JL-NWFET for different temperatures

The variation of Conduction Band (CB) energy and Valance Band (VB) energy along the device length of I-JL-NWFET and JL-NWFET for different temperatures at V_{GS} = 0 V is plotted in Fig. 2.35 (a). As the band gap profile is analyzed below ZTC point of I-JL-NWFET and JL-NWFET, with an increase in temperature, band gap decreases that consequently increases I_{DS}. Moreover, at any given temperature, JL-NWFET exhibits the smallest tunneling width from VB of channel to CB of drain region in comparison to I-JL-NWFET during OFF-state. This mechanism causes parasitic BJT and increases I_{OFF} in JL-NWFET [17]. However, the inclusion of an oppositely doped core widens this tunneling width and enhances source to channel barrier

height that cumulatively decreases I_{OFF} in I-JL-NWFET [17]. Additionally, the employment of two dissimilar gate work functions in the DMG structure results in an abrupt transition, further amplifying the tunneling width of I-JL-NWFET [11].

Figure 2.35 (b) depicts the variation of the electric field along the device length of I-JL-NWFET and JL-NWFET for different temperatures at V_{GS} = 1 V. As the electric field is analyzed above ZTC point of I-JL-NWFET and JL-NWFET, with an increase in temperature, electric decreases, subsequently reducing I_{DS}. At any particular temperature, I-JL-NWFET displays two electric field peaks leading to accelerating electrons in the channel, which consequently enhances I_{DS} as compared to JL-NWFET in ON-state. Furthermore, the peak value of an electric field near drain region in I-JL-NWFET is reduced than that in JL-NWFET due to the lower work function of M_2. This characteristic enables better modulation of the V_{GS} over the channel rather than the V_{DS}, consequently mitigating SCE such as DIBL [11].



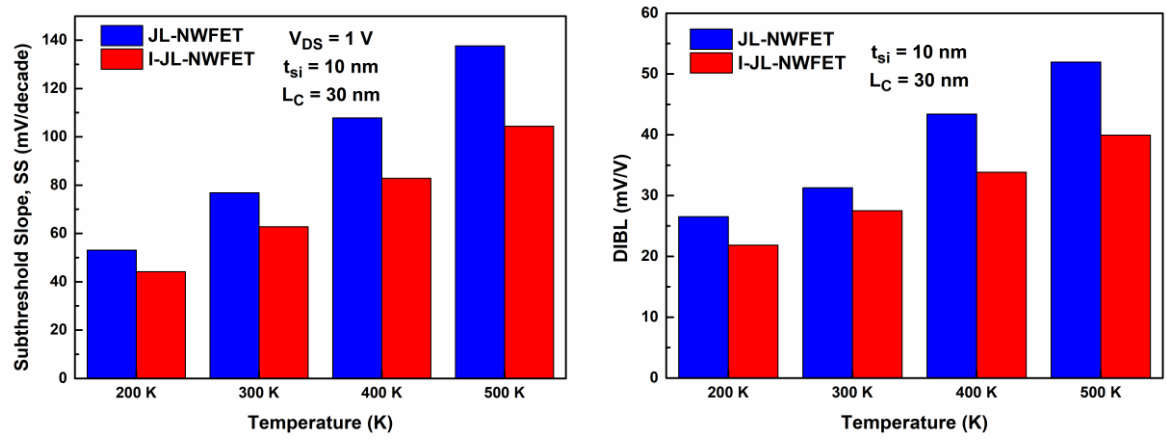
(a) (b)

Fig. 2.36 Plots of (a) output characteristics and (b) I_{ON}/I_{OFF} ratio of I-JL-NWFET and JL-NWFET for different temperatures

Figure 2.36 (a) presents the output characteristics variation of I-JL-NWFET and JL-NWFET with temperature at V_{GS} = 1 V. The I_{DS} of I-JL-NWFET is observed to be higher than that of JL-NWFET. Analysis from Fig. 2.36 (a) reveals that the ZTC for I-JL-NWFET and JL-NWFET occurs at 0.7 V and 0.8 V, respectively. Beyond this ZTC point, I_{DS} decreases with increasing temperature. Consequently, as the output characteristics are plotted beyond their respective ZTC points, the I_{DS} of both devices decreases as temperature rises. Moreover, for any given temperature, the I_{DS} of I-JL-NWFET is observed to be higher than that of JL-NWFET as explained in Fig. 2.34 (b).

The I_{ON}/I_{OFF} ratio of I-JL-NWFET and JL-NWFET at various temperatures is plotted in Fig. 2.37 (b). As discussed in Fig. 2.34 (b), an increase in temperature increases I_{OFF}, consequently decreasing I_{ON}/I_{OFF} ratio in both I-JL-NWFET and JL-NWFET. However, the I_{ON}/I_{OFF} ratio of I-JL-NWFET is notably higher compared to JL-NWFET. The reason behind this is the utilization of DMG architecture and oppositely doped core in I-JL-NWFET, which work synergistically to increase I_{ON} and decrease I_{OFF}, respectively.

The variation of SS and DIBL in I-JL-NWFET and JL-NWFET against increasing temperature is illustrated in Fig. 2.37 (a) and (b), respectively. Notably, the observed variations in SS and DIBL are 29% and 28% less, respectively, in I-JL-NWFET compared to JL-NWFET when the temperature is increased from 200 K to 500 K. This indicates that I-JL-NWFET demonstrates a relatively lower sensitivity to temperature-induced changes in SS and DIBL compared to JL-NWFET over the specified temperature range.



(a) (b)

Fig. 2.37 Plots of (a) SS and (b) DIBL of I-JL-NWFET and JL-NWFET for different temperatures

The SS and DIBL in I-JL-NWFEET vary in a controlled manner with increasing temperature in comparison to JL-NWFET. At any given temperature, the reduced SS observed in I-JL-NWFET is credited to its high I_{ON}/I_{OFF} ratio, indicating superior switching speed compared to JL-NWFET. Furthermore, the DIBL of I-JL-NWFET is less than that of JL-NWFET at a specified temperature range attributed to the presence of the DMG architecture. As discussed in Fig. 2.33 (b), the lower gate work function at the drain side than the source side results in a reduced electric field, allowing for greater control of the V_{GS} over the channel rather than the V_{DS}.

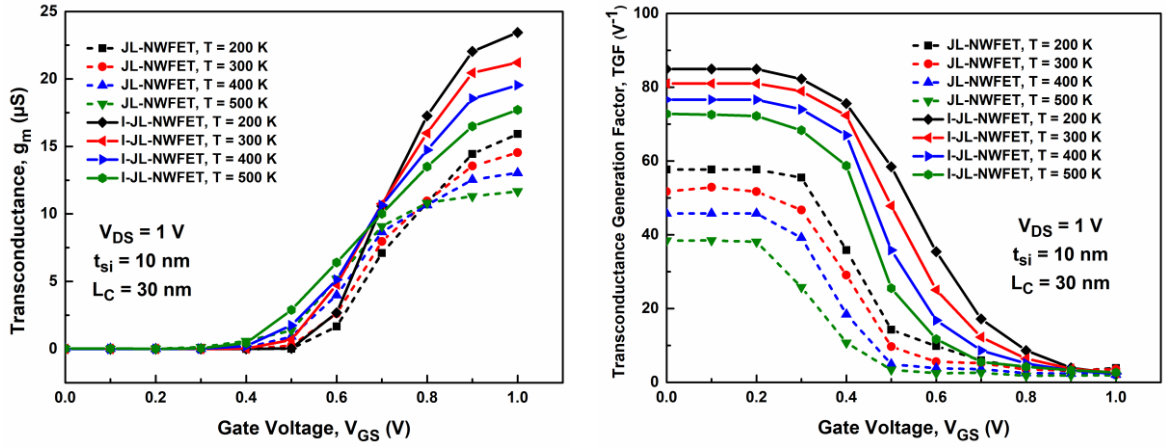
Table 2.6. Effect of temperature on the electrical performance of JL-NWFET and the proposed I-JL-NWFET

Parameters	Devices	200 K	300 K	400 K	500 K
I_{ON}/I_{OFF}	JL-NWFET	2.13×10^5	1.07×10^4	1.70×10^3	1.81×10^2
	I-JL-NWFET	7.40×10^9	5.83×10^8	4.93×10^7	7.37×10^5
SS (mV/decade)	JL-NWFET	53.14	76.83	107.85	137.68
	I-JL-NWFET	44.19	62.75	82.84	104.41
DIBL (mV/V)	JL-NWFET	26.54	31.30	43.40	51.95
	I-JL-NWFET	21.84	27.51	33.84	39.95

Table 2.6 provides a comprehensive comparison of the electrical performance of the I-JL-NWFET with that of JL-NWFET at various temperatures. Notably, the comparison demonstrates that parameters such as I_{ON}/I_{OFF} ratio, SS and DIBL are less susceptible to temperature fluctuations in the I-JL-NWFET when compared to the JL-NWFET.

2.8.2 Impact of temperature on analog/RF parameters

The analog/RF circuits are often sensitive to changes in temperature. An in-depth analysis of temperature variation is vital for ensuring the reliable and consistent performance of the device. This sub-section investigates the impact of temperature on the analog/RF parameters such as g_m, TGF, g_d, V_{EA}, C_{GG}, and f_T of the I-JL-NWFET and JL-NWFET.



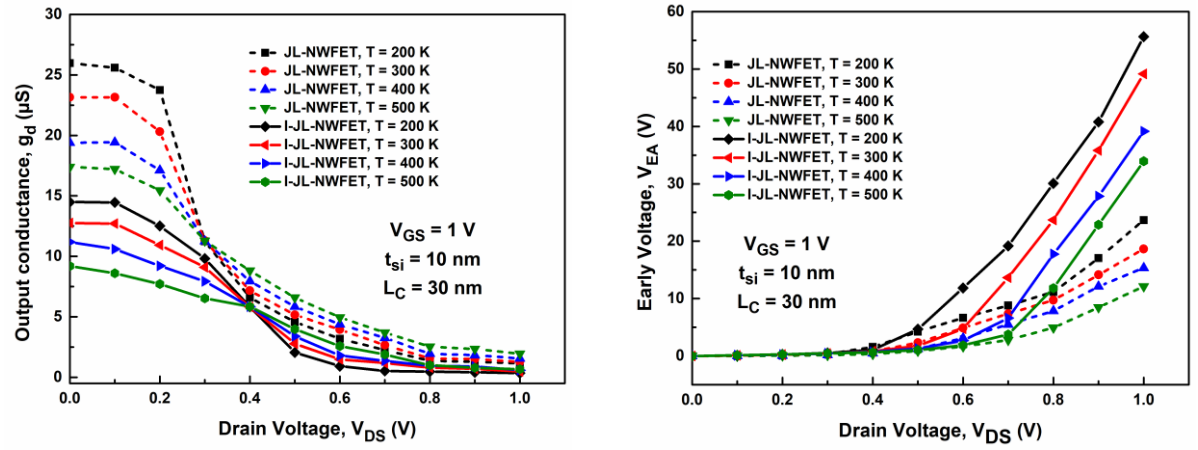
(a) (b)

Fig. 2.38 Plots of (a) transconductance and (b) TGF of I-JL-NWFET and JL-NWFET for different temperatures

Figure 2.38 (a) and (b) exhibit the g_m and TGF variation with respect to V_{GS} at various temperatures, respectively. It is noted from Fig. 2.38 (a) that the g_m of both I-JL-NWFET and JL-NWFET experiences an increase with temperature below ZTC. However, above the ZTC, the trends reverse, possibly attributed to an increase in the rate of scattering events with rising temperatures, as discussed in Fig. 2.34 (a). Furthermore, for a given temperature, the g_m of I-JL-NWFET surpasses that of JL-NWFET owing to DMG architecture. Additionally, there is a decrease of 24.4% in g_m for I-JL-NWFET and 26.7% for JL-NWFET at V_{GS} = 1 V. Fig. 2.38

(b) reveals that in the subthreshold region, the TGF decreases by 14.32% in I-JL-NWFET and 33.40% in JL-NWFET, with an increase in temperature from 200 K to 500 K at V_{GS} = 0 V.

The impact of temperature on g_d and V_{EA} of I-JL-NWFET and JL-NWFET are portrayed in Fig. 2.39 (a) and (b), respectively. At lower V_{DS}, the g_d is primarily influenced by Channel Length Modulation (CLM). Conversely, at higher V_{DS}, the g_d is governed DIBL [113]. CLM represents a SCE whereby the channel length is effectively shortened due to the application of drain bias. This phenomenon is particularly relevant because the output resistance of the device is directly proportional to the channel length. Consequently, when the channel length is shortened due to drain bias, it increases the output conductance.



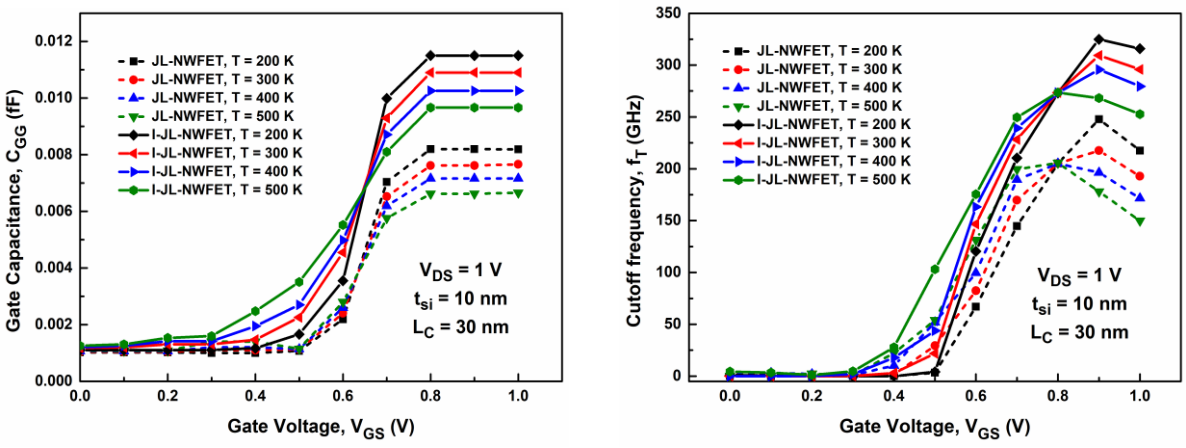
(a) (b)

Fig. 2.39 Plots of (a) output conductance and (b) early voltage of I-JL-NWFET and JL-NWFET for different temperatures

As depicted in Fig. 2.39 (a), it is evident that, at any given temperature, g_d in I-JL-NWFET is lower than JL-NWFET at higher V_{DS}. Additionally, a temperature increase at lower V_{DS} results in a reduction of g_d until a specific V_{DS}, beyond which g_d reverses its trend due to the occurrence of ZTC point and rise in DIBL with the temperature increment. Due to the lowest g_d of I-JL-NWFET at higher V_{DS} at any particular temperature, it attains a superior V_{EA} than that in JL-NWFET as illustrated in Fig. 2.39 (b). The enhanced V_{EA} contributes to an improved intrinsic gain of the device, particularly beneficial for analog amplifiers. Moreover, with the rise in temperature from 200 K to 500 K, V_{EA} decreases 32.9% in I-JL-NWFET and 52.72% in JL-NWFET.

Fig. 2.40 (a) and (b) depict the C_{GG} and f_T as a function of V_{GS} for temperatures ranging from 200 K to 500 K for I-JL-NWFET and JL-NWFET, respectively. From Fig. 2.40 (a), it is perceived that, under low V_{GS}, C_{GG} is predominantly influenced by the depletion capacitance (C_{dep}) [117]. With the rising temperature, the surface potential diminishes, causing an

enhancement in C_{dep}. Conversely, under high V_{GS} conditions, an increase in temperature leads to a reduction in C_{GG}. Notably, I-JL-NWFET exhibits a higher C_{GG} compared to JL-NWFET at any given temperature, attributed to the increased outer fringe capacitance resulting from the utilization of a high-k GSS [113].



(a) (b)

Fig. 2.40 Plots of (a) gate capacitance and (b) cut-off frequency of I-JL-NWFET and JL-NWFET for different temperatures

The behavior of f_T mirrors the trends observed in g_m and C_{GG}. It increases with a temperature rise at lower V_{GS} until a specific V_{GS}, after which it declines with further temperature increases, as demonstrated in Fig. 2.40 (b). For the I-JL-NWFET, the decline in C_{GG} at higher V_{GS} is offset by an improvement in g_m, resulting in a superior f_T compared to the JL-NWFET. Notably, the reduction in f_T is 19.9% in I-JL-NWFET and 45.2% in JL-NWFET when the temperature is elevated from 200 K to 500 K.

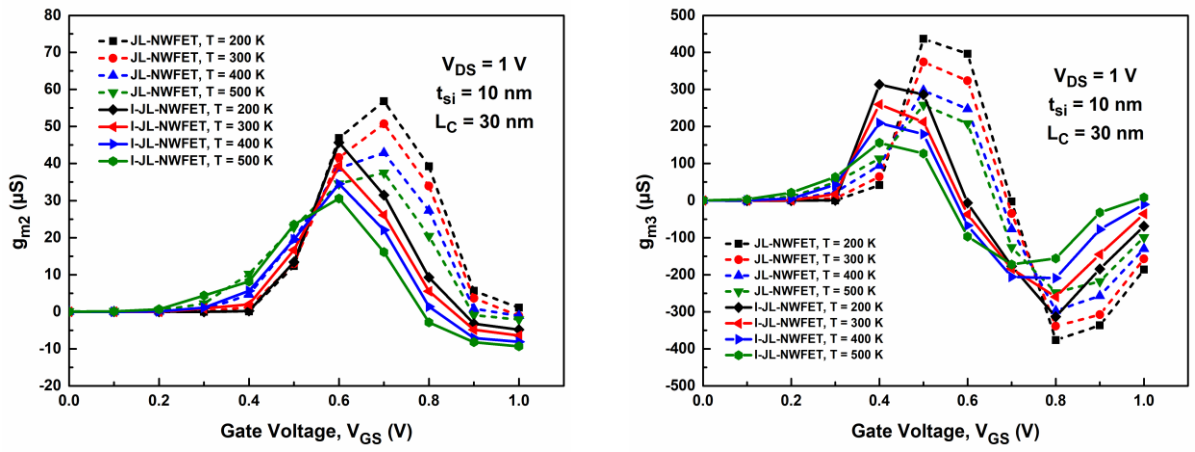
Table 2.7. Effect of temperature on the analog/RF performance of JL-NWFET and the proposed I-JL-NWFET

Parameters	Devices	200 K	300 K	400 K	500 K
g_m (µS)	JL-NWFET	15.92	14.53	13.04	11.67
	I-JL-NWFET	23.43	21.21	19.53	17.70
TGF (V^{-1})	JL-NWFET	57.69	51.69	45.76	38.41
	I-JL-NWFET	84.91	80.98	76.61	72.75
g_d (µS)	JL-NWFET	1.16	1.27	1.56	1.95
	I-JL-NWFET	0.35	0.47	0.59	0.67
V_{EA} (V)	JL-NWFET	23.68	18.65	15.36	12.14
	I-JL-NWFET	55.63	49.14	39.14	33.94
C_{GG} (fF)	JL-NWFET	0.008	0.0070	0.0071	0.006
	I-JL-NWFET	0.011	0.0109	0.0102	0.009
f_T (GHz)	JL-NWFET	217.56	192.75	171.55	149.84
	I-JL-NWFET	315.80	295.80	279.54	252.73

The analog/RF parameters of JL-NWFET and I-JL-NWFET at different temperature are summarized in Table 2.7. The analysis reveals that g_m, TGF, g_d, V_{EA}, C_{GG}, and f_T are less affected by temperature variations in I-JL-NWFET compared to JL-NWFET.

2.8.3 Impact of temperature on linearity parameters

In addition to achieving high speed, contemporary communication systems must ensure minimal signal distortion to assess the device's suitability for analog and RF applications. If a device fails to maintain linearity, the nonlinear components at the output may overwhelm the desired signal. To enhance the linearity of a system, the g_m must remain constant across the input voltage. In this subsection, the effect of temperature on the linearity performance of I-JL-NWFET is analyzed through metrics such as g_{m2}, g_{m3}, VIP2, VIP3, IMD3, and IIP3, and results are compared with JL-NWFET.



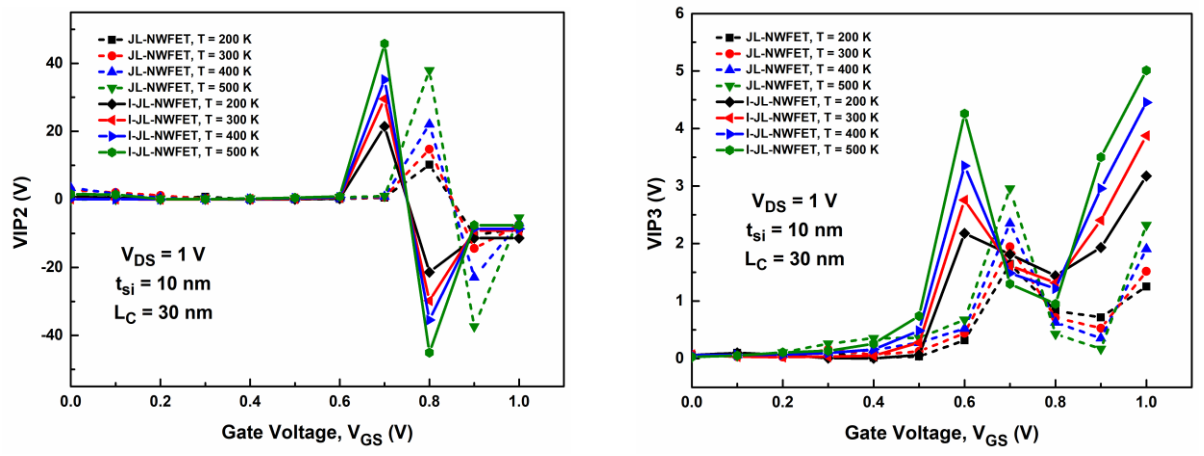
(a) (b)

Fig. 2.41 Plots of (a) g_{m2} and (b) g_{m3} of I-JL-NWFET and JL-NWFET for different temperatures

The effect of temperature on g_{m2} and g_{m3} against V_{GS} of I-JL-NWFET and JL-NWFET are portrayed in Fig. 2.41 (a) and (b), respectively. The g_{m2} decreases as temperature increases in case of both I-JL-NWFET and JL-NWFET as exhibited in Fig. 2.41 (a). Additionally, the peak value of g_{m2} of I-JL-NWFET is reduced by 2.53%, 5.45%, 10.74%, and 11.67% as compared to JL-NWFET at 200 K, 300 K, 400 K and 500 K, respectively, indicating I-JL-NWFET is more linear than JL-NWFET at higher temperature. The linearity of the device is also associated with the flatness of the g_{m3} amplitude. The g_{m3} primarily contributes to the distortion of fundamental amplitude through signals in adjacent bands or intermodulation distortions.

Moreover, the Zero-Crossover Point (ZCP) of g_{m3} should occur at a lower V_{GS} for improved linearity performance [115]. The V_{GS} value at which g_{m3} first crosses the zero axis is defined as ZCP and determines the DC bias point for optimal device operation. Furthermore, in I-JL-

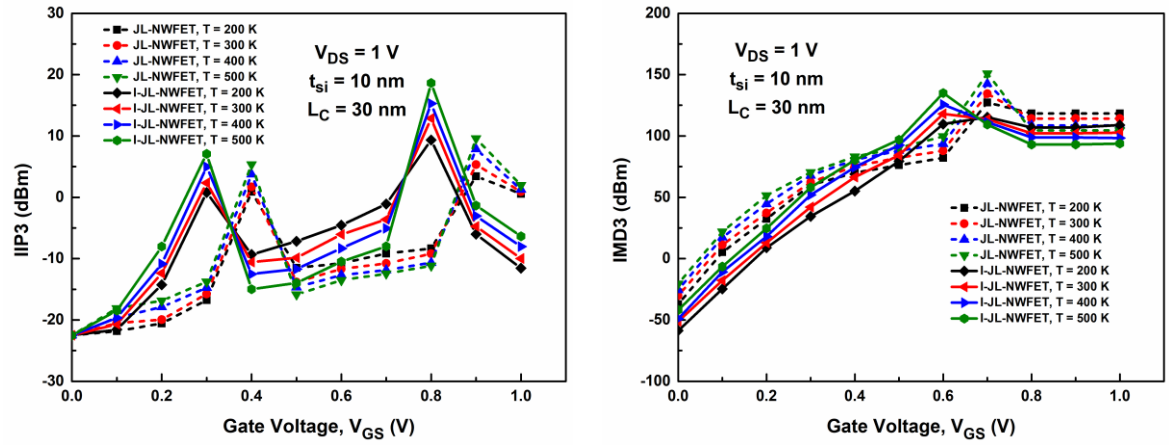
NWFET, ZCP is shifted towards lower V_{GS} compared to JL-NWFET at any given temperature. This shift is advantageous for achieving better linearity and lower distortion in device performance. The influence of temperature on VIP2 and VIP3 of I-JL-NWFET and JL-NWFET are displayed in Fig. 2.42 (a) and (b), respectively.



(a) (b)

Fig. 2.42 Plots of (a) VIP2 and (b) VIP3 of I-JL-NWFET and JL-NWFET for different temperatures

It is observed in Fig. 2.42 (a) that the peak value of VIP2 in I-JL-NWFET exhibits an increase by 2.09 times, 2.0 times, 1.59 times, and 1.20 times compared to that in JL-NWFET as the temperature escalates from 200 K to 500 K. This augmentation is attributed to a reduction in the amplitude of g_{m2} with the rise of temperature. Furthermore, in Fig. 2.42 (b), the peak value of VIP3 in I-JL-NWFET occurs when g_{m3} is zero and shows an increase by 32.3%, 41.7%, 43.1%, and 44% compared to that in JL-NWFET as the temperature increases from 200 K to 500 K.



(a) (b)

Fig. 2.43 Plots of (a) IIP3 and (b) IMD3 of I-JL-NWFET and JL-NWFET for different temperatures

Figure 2.43 (a) and (b) depict the influence of temperature variation on IIP3 and IMD3 of I-JL-NWFET and JL-NWFET as functions of V_{GS}, respectively. The higher IIP3 peak observed in Fig. 2.43 (a) of I-JL-NWFET than of JL-NWFET with rising temperature distinctly indicates enhanced linearity performance as the temperature increases. Additionally, IMD3 of I-JL-NWFET is found to be lower than that of JL-NWFET as depicted in Fig. 2.43 (b). This observation ensures that in the I-JL-NWFET, HCEs have been mitigated, leading to a reduction in both power consumption and distortion of the device.

Table 2.8. Effect of temperature on the linearity performance of JL-NWFET and the proposed I-JL-NWFET

Parameters	Devices	200 K	300 K	400 K	500 K
Peak g_{m2} (µS)	JL-NWFET	56.82	50.75	42.89	37.47
	I-JL-NWFET	45.69	39.34	34.51	30.57
Peak g_{m3} (µS)	JL-NWFET	436.46	373.78	297.22	258.06
	I-JL-NWFET	313.35	259.73	209.30	155.98
Peak VIP2 (V)	JL-NWFET	10.22	14.74	22.05	37.93
	I-JL-NWFET	21.45	29.54	35.15	45.75
Peak VIP3 (V)	JL-NWFET	1.65	1.95	2.35	2.96
	I-JL-NWFET	2.18	2.76	3.35	4.26
Peak IIP3 (dBm)	JL-NWFET	3.42	5.31	7.87	9.60
	I-JL-NWFET	9.34	12.85	15.27	18.62
Peak IMD3 (dBm)	JL-NWFET	127.29	134.39	142.60	150.88
	I-JL-NWFET	109.65	118.04	125.63	134.96

Table 2.8 summarizes the lower temperature variation of the linearity parameter of I-JL-NWFET than that of JL-NWFET. Eventually, for increasing temperature (200 K - 500 K), I-JL-NWFET is more reliable and useful in RF applications than JL-NWFET. Moreover, investigating alternative semiconductor materials with superior thermal stability could mitigate performance degradation at elevated temperatures. Materials like silicon carbide (SiC) have exhibited notable potential in preserving electrical characteristics at high temperatures [119]. It may serve as a potential future substitute for silicon material at high temperatures.

2.9 SUMMARY OF THE IMPORTANT RESULTS

The current chapter is focused on improving the performance of JL-NWFET by identifying its major limitation of L-BTBT and thereby proposing a novel I-JL-NWFET device. The proposed I-JL-NWFET consists of oppositely doped CS, DMG, and high-*k* GSS architecture to improve the device performance. Further, the optimization of I-JL-NWFET reveals that the t_{core} should be half of the L_C, and that a low-*k* material as gate oxide material combined with a high-*k* GSS material provides the best performance. Additionally, spacer length is found to be equal to $L_{S/D}$ length for optimal results.

Subsequently, horizontal cut-line analysis is undertaken to gain deeper insight into device behaviour and the factors contributing to improve the proposed device performance. Furthermore, the performance comparison of I-JL-NWFET with other variants of JL-NWFET demonstrates its superior characteristics. Additionally, the impact of L_C and t_{si} confirms its reliable scalability with reduced SCEs. Finally, the impact of temperature analysis on electrical, analog/RF, and linearity parameters shows robust performance of the proposed I-JL-NWFET against temperature variation. The important outcomes of the chapter are enlisted below.

- Firstly, an NWFET is validated using the SILVACO ATLAS tool by calibrating simulation conditions against the experimental data, and a close agreement is observed between experimental and simulated transfer characteristics.
- The optimization of the proposed I-JL-NWFET shows that for t_{si} of 20 nm, a 10 nm t_{core} is the optimal value, with SiO_2 as gate oxide with HfO_2 as spacer material, and the spacer length of 25 nm is the same as the $L_{S/D}$.
- I-JL-NWFET demonstrates a 23.1% increase in I_{ON} along with a reduction by an order of 5 in I_{OFF} compared to JL-NWFET. Furthermore, an impressive I_{ON}/I_{OFF} ratio of approximately 10^6 is achieved in I-JL-NWFET, which is six orders of magnitude higher than that of JL-NWFET. Moreover, an 88% improvement in SS is observed in the I-JL-NWFET compared to the JL-NWFET.
- During comparative analysis, the proposed I-JL-NWFET (D1) achieved the highest I_{DS} of 24.5 µA, which is 11%, 77%, 54%, and 23% greater than devices D2, D3, D4, and D5, respectively. Device D1 shows significant improvements in SS compared to devices D2, D3, D4, and D5, with enhancements of 3%, 32%, 80%, and 88%, respectively. Additionally, g_m in Device D1 enhances by 11%, 31%, 26% and 20% as compared to Devices D2, D3, D4, and D5, respectively.
- The L_C and t_{si} of the I-JL-NWFET are optimized to 30 nm and 10 nm, respectively. The variation of I_{DS} in I-JL-NWFET and JL-NWFET is 29% and 31.8%, respectively, with an increase in temperature from 200 K to 500 K. The SS and DIBL are 29% and 28% less, respectively, in I-JL-NWFET compared to JL-NWFET over the same temperature range.
- There is a decrease of 24.4% in g_m for I-JL-NWFET and 26.7% for JL-NWFET. Similarly, V_{EA} decreases by 32.9% in I-JL-NWFET and 52.72% in JL-NWFET. The reduction in f_T is 19.9% in I-JL-NWFET and 45.2% in JL-NWFET when the temperature is elevated from 200 K to 500 K.

- The peak value of g_{m2} of I-JL-NWFET is reduced by 2.53%, 5.45%, 10.74%, and 11.67% as compared to JL-NWFET at 200 K, 300 K, 400 K, and 500 K, respectively, indicating I-JL-NWFET is more linear than JL-NWFET at higher temperatures.

The present work demonstrates significant performance enhancement of the JL-NWFET through the proposed I-JL-NWFET by the cumulative benefits of CS, DMG, and GSS architecture, and thereafter optimizing key design parameters. The future research can focus on the incorporation of advanced materials with superior electrical properties and optimized dielectric combinations to further suppress SCEs and I_{OFF}. Additionally, emphasis can be placed on developing improved fabrication techniques to precisely control doping profiles and interface quality, thereby minimizing variability and trap-induced degradation. These advancements can further strengthen the scalability, reliability, and overall performance of next-generation JL-NWFET devices.

CHAPTER-3
ANALYTICAL MODELING OF IMPROVED JUNCTIONLESS NANOWIRE FET

3.1 INTRODUCTION

As the device dimensions are aggressively scaled, improved control over channel potential, suppression of SCEs, and enhancement of current driving capability become increasingly important. However, the cylindrical geometry of JL-NWFETs gives rise to electrostatic behaviour that differs significantly from that of conventional planar transistors. Consequently, analytical expressions developed for planar devices cannot be directly applied to NWFET structures. Therefore, a dedicated cylindrical analytical framework is required to accurately describe the potential distribution, electric field profile, and carrier transport characteristics of such devices. Analytical modelling plays an important role in understanding the underlying device physics and in validating numerical simulation results.

In this thesis, rather than directly developing an analytical model for the proposed I-JL-NWFET incorporating CS, DMG, and GSS architecture, a stepwise analytical approach is adopted. The influence of individual structural modifications to be isolated and examined by considering two architectural features at a time. Initially, analytical modelling is carried out for the JL-NWFET with CS and DMG, followed by the JL-NWFET with CS and GSS. After establishing the physical insight obtained from these intermediate configurations, a comprehensive analytical model of the proposed I-JL-NWFET integrating CS, DMG, and GSS is developed. This systematic approach facilitates a clearer understanding of the contribution of each design element and provides analytical validation of the performance improvements observed in simulation.

As a comprehensive performance analysis of the proposed I-JL-NWFET is presented in Chapter 1 through TCAD simulation, analytical modelling is required to further validate and authenticate the observed performance improvements. The following objective is framed here to obtain an analytical modeling of Improved Junctionless Nanowire FET:

“Analytical Modeling to Extract Performance Parameters for Improved Junctionless Nanowire FET.”

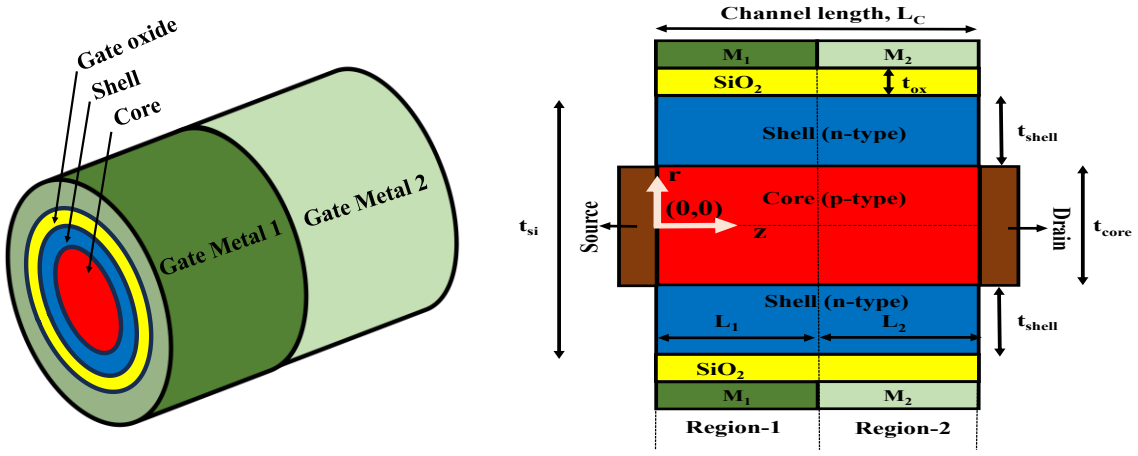
To realize the desired objective, the methodology includes the following steps: -

- First, an analytical model of the JL-NWFET incorporating CS and DMG is developed for the subthreshold region, without considering the influence of S/D length.
- Subsequently, an analytical model of the JL-NWFET with CS and GSS is formulated for all regions of operation, taking into account the effect of S/D length.
- Finally, a comprehensive analytical model of the JL-NWFET integrating CS, DMG, and GSS is developed for all operating regions, with explicit consideration of S/D length.

This chapter is arranged into five major sections, including this introductory section numbered as 3.1. In Section 3.2, an analytical model of the JL-NWFET incorporating CS and DMG is developed for the subthreshold region, without considering the influence of S/D length. Subsequently, in Section 3.3, the analytical model of the JL-NWFET with CS and GSS is formulated across all regions of operation, accounting for the effect of S/D length. In Section 3.4, a comprehensive analytical model of the proposed I-JL-NWFET integrating CS, DMG, and GSS is developed for all operating regions, with explicit consideration of S/D length. The summary of the complete research work of this chapter is highlighted in Section 3.5.

3.2 ANALYTICAL MODELING OF JL-NWFET WITH CS AND DMG

To derive an analytical model for JL-NWFET with CS and GSS (DMG-CS-JL-NWFET), the device is divided into two different regions (region-1 and region-2). Fig. 3.1 (a) and (b) showcase the 3-D and 2-D schematic illustrations of DMG-CS-JL-NWFET, respectively. DMG-CS-JL-NWFET comprises two gate materials, M_1 and M_2 with lengths L_1 and L_2 respectively, such that channel length $L_C = L_1 + L_2$.



(a) (b)

Fig. 3.1 (a) 3-D and (b) 2-D cross-sectional view of DMG-CS-JL-NWFET

For simplicity, the S/D region is assumed to have zero thickness and the S/D contact is located along the left/right side of the silicon channel. The assumption of zero thickness for S/D regions simplifies the modeling complexity by treating these regions as idealized interfaces without spatial extent. Notably, this assumption does not affect the model's accuracy in the current analysis, as no S/D extensions have been considered during the simulations. However, a non-zero S/D thickness plays a critical role in device behavior.

Specifically, the S/D extension region acts as an extension of the channel, helping to weaken SCEs and improving overall device performance [47]. Therefore, considering a non-zero S/D thickness is essential in advanced technology nodes where SCEs are more significant. In this chapter, t_{si} is considered to be greater than 5 nm; therefore, quantum mechanical effects are disregarded [120]. When t_{si} is further scaled below 5 nm, quantum confinement effects become increasingly significant. These effects alter the energy band structure of silicon, leading to an effective widening of the bandgap due to spatial quantization of carriers. This energy bandgap correction would directly impact key device parameters.

3.2.1 Surface Potential and Electric Field Modeling

Assuming the shell region of the channel is completely depleted under the subthreshold regime. The 3-D channel potential in the core region, $\varphi_{core,j}(r, z, \theta)$ and the shell region, $\varphi_{shell,j}(r, z, \theta)$, are symmetric with respect to the θ direction, therefore, $\partial\varphi_{core,j}(r, z, \theta)/\partial\theta = 0$ and $\partial\varphi_{shell,j}(r, z, \theta)/\partial\theta = 0$. Therefore, the potential distributions in the shell and core regions of the channel are obtained by solving the 2-D Poisson's equation in cylindrical coordinates and can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\varphi_{core,j}(r,z)\right)+\frac{\partial^2\varphi_{core,j}(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}},\ j=1,2\ for\ 0\le r\le\frac{t_{core}}{2} \tag{3.1}$$

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\varphi_{shell,j}(r,z)\right)+\frac{\partial^2\varphi_{shell,j}(r,z)}{\partial z^2}=-\frac{qN_d}{\varepsilon_{si}},\ j=1,2\ for\ \frac{t_{core}}{2}\le r\le\frac{t_{shell}}{2} \tag{3.2}$$

where $\varphi_{core,j}(r, z)$ and $\varphi_{shell,j}(r, z)$ are potentials in core and shell regions, respectively, for the jth region (j = 1, 2). The electronic charge, permittivity of silicon, acceptor concentration, and donor concentration are denoted as q, ε_{si}, N_a, and N_d, respectively. The potential distributions along the radial direction in both the core and shell regions are assumed to be parabolic profiles analogous to that developed by [47] and are given as

$$\varphi_{core,j}(r,z)=A_{0j}(z)+A_{1j}(z)r+A_{2j}(z)r^2 \tag{3.3}$$

$$\varphi_{shell,j}(r,z) = B_{0j}(z) + B_{1j}(z)\left(r - \frac{t_{core}}{2}\right) + B_{2j}(z)\left(r - \frac{t_{core}}{2}\right)^2 \tag{3.4}$$

The coefficients A_{0j}, A_{1j}, A_{2j}, B_{0j}, B_{1j}, and B_{2j} are determined using the following boundary conditions [47]

(i) In the core region, the central potential ($\varphi_{Cj}(z)$) is a function of z only. This reflects the symmetry of the core structure and the lack of radial dependence due to the cylindrical geometry and is represented as

$$\varphi_{core,j}(0,z) = \varphi_{Cj}(z) \tag{3.5}$$

(ii) In the shell region, the surface potential ($\varphi_{Sj}(z)$) reflects the influence of the gate voltage on the surface potential, which is a critical factor in determining the device's electrostatic behavior and is given as

$$\varphi_{shell,j}\left(\frac{t_{si}}{2}, z\right) = \varphi_{Sj}(z) \tag{3.6}$$

(iii) The electric field in the centre of the channel region is zero due to symmetry along the z-axis. This ensures consistency with the physical geometry and potential distribution.

$$\left.\frac{\partial \varphi_{core,j}(r,z)}{\partial r}\right|_{r=0} = 0 \tag{3.7}$$

(iv) The electric flux at the interface of the gate oxide and shell region is continuous. This condition ensures that the displacement field remains consistent across the oxide and shell interface, preserving electrostatic continuity.

$$\varepsilon_{si}\left.\frac{\partial \varphi_{shell,j}(r,z)}{\partial r}\right|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}\left(\varphi_{gj} - \varphi_{Sj}(z)\right)}{\frac{t_{si}}{2}\ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)} \tag{3.8}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{\frac{t_{si}}{2}\ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)} \tag{3.9}$$

$$\varphi_{gj} = V_{GS} - V_{fbj} \tag{3.10}$$

$$V_{fbj} = \phi_{Mj} - \phi_{si} \tag{3.11}$$

$$\left.\frac{\partial \varphi_{shell,j}(r,z)}{\partial r}\right|_{r=\frac{t_{si}}{2}} = \frac{C_{ox}\left(\varphi_{gj} - \varphi_{Sj}(z)\right)}{\varepsilon_{si}} \tag{3.12}$$

here, the notations C_{ox}, ε_{ox}, t_{ox}, and ϕ_{si} represent gate oxide capacitance per unit area, gate oxide permittivity, gate oxide thickness and silicon work function. V_{fbj} and ϕ_{Mj} are the flat band voltage and gate work functions for the jth region.

(iv) Continuity in the potential and electric field at core-shell interface. These conditions are critical for maintaining smooth transitions between the core and shell regions.

$$\varphi_{core,j}\left(\frac{t_{core,j}}{2},z\right)=\varphi_{shell,j}\left(\frac{t_{core,j}}{2},z\right) \tag{3.13}$$

$$\left.\frac{\partial\varphi_{core,j}(r,z)}{\partial r}\right|_{r=\frac{t_{core}}{2}}=\left.\frac{\partial\varphi_{shell,j}(r,z)}{\partial r}\right|_{r=\frac{t_{core}}{2}} \tag{3.14}$$

The arbitrary coefficients, A_{0j}, A_{1j}, A_{2j}, B_{0j}, B_{1j}, and B_{2j} are determined using Eqn. 3.5-3.7 and 3.12-3.14 of boundary conditions (i)-(iv) and are derived as

$$A_{0j}(z)=\varphi_{Cj}(z) \tag{3.15}$$

$$A_{1j}(z)=0 \tag{3.16}$$

$$A_{2j}(z)=\frac{\left(4\varepsilon_{si}+C_{ox}\left(t_{si}-t_{core}\right)\right)\varphi_{Sj}(z)-4\varepsilon_{si}\,\varphi_{Cj}(z)-C_{ox}\varphi_{gj}\left(t_{si}-t_{core}\right)}{\varepsilon_{si}t_{si}t_{core}} \tag{3.17}$$

$$B_{0j}(z)=\frac{\left(4\varepsilon_{si}t_{core}+C_{ox}t_{core}\left(t_{si}-t_{core}\right)\right)\varphi_{Sj}(z)+\left(4\varepsilon_{si}\left(t_{si}-t_{core}\right)\right)\varphi_{Cj}(z)-C_{ox}t_{core}\varphi_{gj}\left(t_{si}-t_{core}\right)}{4\varepsilon_{si}t_{si}} \tag{3.18}$$

$$B_{1j}(z)=\frac{\left(4\varepsilon_{si}+C_{ox}\left(t_{si}-t_{core}\right)\right)\varphi_{Sj}(z)-4\varepsilon_{si}\,\varphi_{Cj}(z)-C_{ox}\varphi_{gj}\left(t_{si}-t_{core}\right)}{\varepsilon_{si}t_{si}} \tag{3.19}$$

$$B_{2j}(z)=\frac{\left(-4\varepsilon_{si}-C_{ox}\left(2t_{si}-t_{core}\right)\right)\varphi_{Sj}(z)+4\varepsilon_{si}\,\varphi_{Cj}(z)+C_{ox}\varphi_{gj}\left(2t_{si}-t_{core}\right)}{\varepsilon_{si}t_{si}\left(t_{si}-t_{core}\right)} \tag{3.20}$$

$\varphi_{Sj}(z)$ is written in terms of $\varphi_{Cj}(z)$ by solving Eqns. 3.1 and 3.2 simultaneously using Eqns. 3.3 and 3.4 at $r = t_{core}$ and is given as

$$\varphi_{Cj}(z)=\frac{\left(8\varepsilon_{si}+2C_{ox}t_{si}\right)\varphi_{Sj}(z)-2C_{ox}t_{si}\varphi_{gj}-q(N_a+N_d)t_{core}\left(t_{si}-t_{core}\right)}{8\varepsilon_{si}} \tag{3.21}$$

The second-order differential equation of $\varphi_{Sj}(z)$ is obtained by solving Eqn. 3.2 using Eqns. 3.4 and 3.21, and expressed as

$$\frac{\partial^2\varphi_{Sj}(z)}{\partial z^2}-\frac{\left(\varphi_{Sj}(z)-D_j\right)}{\lambda^2}=0 \tag{3.22}$$

$$D_j=\varphi_{gj}+\frac{qN_dt_{si}}{4C_{ox}}-\frac{qt_{core}(N_a+N_d)}{4C_{ox}} \tag{3.23}$$

$$\lambda^2 = \frac{\varepsilon_{si} t_{si}}{4C_{ox}} \tag{3.24}$$

where λ represents the scaling length of DMG-CS-JL-NWFET. It is observed that λ is the same as that of a conventional Double Gate Junctionless FET [121] without core-shell and DMG architectures. Moreover, D_1 (in region-1) when t_{core} is zero also becomes identical to the long channel surface potential of a conventional Double Gate Junctionless MOSFET [121]. Following the methodology adopted by [58], the generic solution for the second-order differential Eqn. 3.20 for regions 1–2 is expressed as

$$\varphi_{S1}(z) = G_1 e^{z/\lambda} + H_1 e^{-z/\lambda} + D_1 \quad \text{for region-1} \tag{3.25}$$

$$\varphi_{S2}(z) = G_2 e^{z/\lambda} + H_2 e^{-z/\lambda} + D_2 \quad \text{for region-2} \tag{3.26}$$

where arbitrary constants, G_1, H_1, G_2, and H_2, can be determined using the following boundary conditions (v)-(vii). The potential at the source side is assumed to be the built-in potential, $V_{bi} = \frac{KT}{q} \ln\left(1 + \frac{N_d}{n_i}\right)$. K, T, and n_i denote Boltzmann's constant, thermal temperature, and intrinsic concentration, respectively. Additionally, the potential and electric field are assumed to be continuous at the interface between region-1 and region-2, ensuring smooth transitions across the regions [122].

(v) The potential at the source side

$$\varphi_{S1}(z = 0) = V_{bi} \tag{3.27}$$

(vi) The surface potential at the drain side

$$\varphi_{S2}(z = L_C) = V_{bi} + V_{DS} \tag{3.28}$$

(vii) Continuity of the surface potential and electric field at the interface of regions 1 and 2.

$$\varphi_{S1}(z = L_1) = \varphi_{S2}(z = L_1) \tag{3.29}$$

$$\left.\frac{\partial \varphi_{S1}(z)}{\partial r}\right|_{z = L_1} = \left.\frac{\partial \varphi_{S2}(z)}{\partial r}\right|_{z = L_1} \tag{3.30}$$

The G_1, H_1, G_2, and H_2 are determined by solving the abovementioned boundary conditions and obtained as

$$G_1 = P_1 V_{GS} + Q_1 \tag{3.31}$$

$$H_1 = P_2 V_{GS} + Q_2 \tag{3.32}$$

$$G_2 = P_1 V_{GS} + Q_3 \tag{3.33}$$

$$H_2 = P_2 V_{GS} + Q_4 \tag{3.34}$$

where

$$P_1 = \frac{e^{-L_C/\lambda} - 1}{2\ sinh\ (L_C / \lambda)} \tag{3.35}$$

$$P_2 = \frac{1 - e^{L_C/\lambda}}{2\ sinh(L_C / \lambda)} \tag{3.36}$$

$$Q_1 = \frac{V_{DS} + F_1 + F_2 + F_3}{2\ sinh\ (L_C / \lambda)} \tag{3.37}$$

$$Q_2 = \frac{-V_{DS} - F_2 + F_4 + F_5}{2\ sinh\ (L_C / \lambda)} \tag{3.38}$$

$$Q_3 = \frac{V_{DS} + F_1 + F_3 + F_6 e^{-L_C/\lambda}}{2\ sinh\ (L_C / \lambda)} \tag{3.39}$$

$$Q_4 = \frac{-V_{DS} + F_4 + F_5 - F_6 e^{L_C/\lambda}}{2\ sinh\ (L_C / \lambda)} \tag{3.40}$$

$$F_1 = \left(\frac{qN_d t_{si}}{4C_{ox}} - \frac{qt_{core}(N_a + N_d)}{4C_{ox}} - V_{bi} \right)(e^{-L_C/\lambda} - 1) \tag{3.41}$$

$$F_2 = (V_{fb1} - V_{fb2})\ cosh(L_2 / \lambda) \tag{3.42}$$

$$F_3 = V_{fb2} - V_{fb1} e^{-L_C/\lambda} \tag{3.43}$$

$$F_4 = \left(\frac{qN_d t_{si}}{4C_{ox}} - \frac{qt_{core}(N_a + N_d)}{4C_{ox}} - V_{bi} \right)(1 - e^{L_C/\lambda}) \tag{3.44}$$

$$F_5 = V_{fb1} e^{L_C/\lambda} - V_{fb2} \tag{3.45}$$

$$F_6 = (V_{fb1} - V_{fb2})\ cosh(L_1 / \lambda) \tag{3.46}$$

By differentiating the surface potential along the channel length, the lateral electric field distribution can be obtained. It can be written as

$$E_j(z) = -\frac{\partial \varphi_{Sj}(z)}{\partial z} \tag{3.47}$$

$$E_j(z) = -\frac{1}{\lambda}\left(G_j\ e^{z/\lambda} - H_j e^{-z/\lambda} \right) \tag{3.48}$$

3.2.2 Threshold Voltage, Subthreshold Current, DIBL, and Subthreshold Slope Modeling

To determine the V_T, the location (*zmin*) of the minimum surface potential ($\varphi_{S1,min(z)}$) must first be identified. This minimum potential is always found beneath the metal with the highest work function, which is in region-1 (under M_1) [121]. The position of the minimum surface potential (*zmin*) is found by differentiating Eqn. 3.25 and setting the result to zero [121].

$$\left.\frac{d\varphi_{S1}(z)}{dz}\right|_{z=z\min} = 0 \tag{3.49}$$

$$\left.\frac{d\left(G_1 e^{z/\lambda} + H_1 e^{-z/\lambda} + D_1\right)}{dz}\right|_{z=z\min} = 0 \tag{3.50}$$

$$\frac{z\min}{\lambda}\left(G_1\, e^{z\min/\lambda} - H_j e^{-z\min/\lambda}\right) = 0 \tag{3.51}$$

$$z\min = \frac{\lambda}{2}\ln\left(\frac{H_1}{G_1}\right) \tag{3.52}$$

The $\varphi_{S1,min}(z)$ in region-1 can be determined by substituting *zmin* in Eqn. 3.25, which is given as

$$\varphi_{S1,\min}(z)\big|_{z=z\min} = G_1\sqrt{\frac{H_1}{G_1}} + H_1\sqrt{\frac{G_1}{H_1}} + D_1 \tag{3.53}$$

$$\varphi_{S1,\min}(z)\big|_{z=z\min} = 2\sqrt{G_1 H_1} + D_1 \tag{3.54}$$

The V_T of DMG-CS-JLNWFET can be obtained by equating $\varphi_{S1,min}(z)$ to zero for $V_{GS} = V_T$ as shown below

$$2\sqrt{G_1 H_1} + D_1 = 0 \tag{3.55}$$

$$4G_1 H_1 = D_1^2 \tag{3.56}$$

By substituting Eqns. 3.23, 3.31, and 3.32 in Eqn. 3.56 and setting $V_{GS} = V_T$

$$4\left(P_1 V_T + Q_1\right)\left(P_2 V_T + Q_2\right) = \left(V_T - \beta_1\right)^2 \tag{3.57}$$

Where

$$\beta_1 = V_{fb1} - \frac{qN_d t_{si}}{4C_{ox}} + \frac{qt_{core}(N_a + N_d)}{4C_{ox}} \tag{3.58}$$

Solving Eqn. 3.57 for V_T, it can be expressed as

$$V_T = \frac{-N_1 + \sqrt{N_1^2 - N_2}}{N_3} \tag{3.59}$$

where

$$N_1 = 2P_1Q_2 + 2P_2Q_1 + \beta_1 \tag{3.60}$$

$$N_2 = (4Q_1Q_2 - \beta_1^2)N_3 \tag{3.61}$$

$$N_3 = 4P_1P_2 - 1 \tag{3.62}$$

The subthreshold current (I_{sub}) can be obtained by using the channel potential solution and is given as [122]

$$I_{sub} = \frac{\pi t_{si} KT\left(1-e^{-qV_{DS}/KT}\right)}{\int_0^{L_1} \frac{dz}{W_1(z)} + \int_{L_1}^{L_1+L_2} \frac{dz}{W_2(z)}} \tag{3.63}$$

$$W_n(z) = n_i \mu_p \int_0^{t_{core}/2} e^{\left(\frac{q\varphi_{core,j}(r,z)}{KT}\right)} dr + n_i \mu_e \int_{t_{core}/2}^{t_{si}/2} e^{\left(\frac{q\varphi_{shell,j}(r,z)}{KT}\right)} dr \tag{3.64}$$

$$SS = \frac{\partial V_{GS}}{\partial log\left(I_{sub}\right)} \tag{3.65}$$

$$DIBL = \frac{V_T\left(V_{DS}=0.05V\right) - V_T\left(V_{DS}=1V\right)}{\left(V_{DS}=1V\right) - \left(V_{DS}=0.05V\right)} \tag{3.66}$$

here, μ_e and μ_p are hole mobility and electron mobility, respectively. The SS and DIBL can be derived as reported in [9] and [12], respectively.

3.2.3 Validation of Analytical Modeling of JL-NWFET with CS and DMG through Simulation Analysis

Using the derived analytical models, the subthreshold behavior of DMG-CS-JL-NWFET is examined in terms of channel electrostatics surface potential distribution, electric field distribution, I_{sub}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS, and DIBL. Further, the results are also compared with conventional JL-NWFET to highlight the merit of DMG-CS-JL-NWFET. The specifications of conventional JL-NWFET and DMG-CS-JL-NWFET are given in Table 3.1. Unless otherwise stated, the shell doping concentration (N_D) is taken as 1×10^{19} cm^{-3}, the core doping concentration (N_A) is 1×10^{19} cm^{-3}, t_{ox} = 1 nm, and ε_{ox} = 3.9. The V_{DS} is maintained at 1 V, consistent with calibration work (Fig. 2.4). The V_{GS} is set to 0.4 V, which is below the V_T of the DMG-CS-JL-NWFET at L_C = 30 nm, t_{si} = 10 nm, and t_{core} = 0 to 7 nm, ensuring operation in the subthreshold region. It may be noted that t_{core} of 0 corresponds to a conventional DMG-JL-NWFET without a core-shell structure.

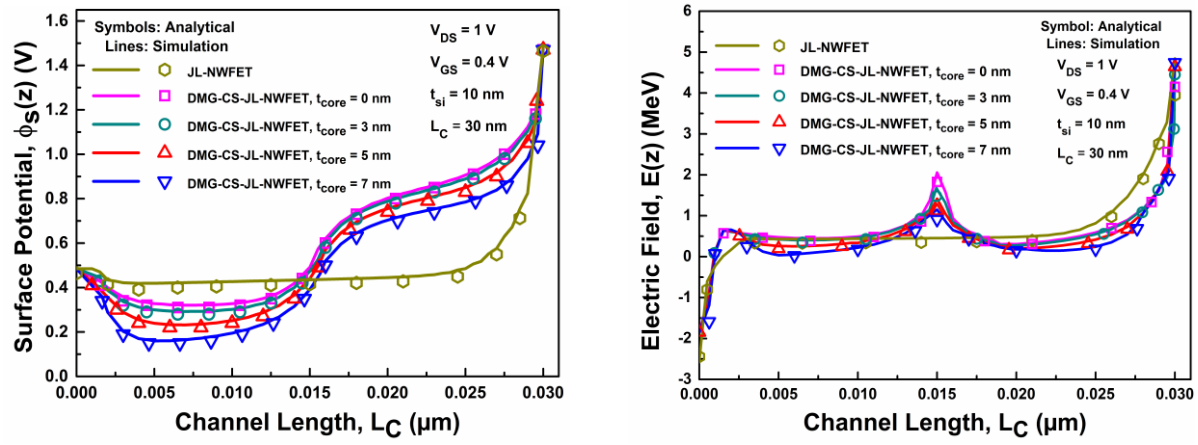
Table 3.1. Device specification for conventional JL-NWFET and DMG-CS-JL-NWFET

Parameters	JL-NWFET	DMG-CS-JL-NWFET	
Channel Thickness, t_{si} (nm)	10	10	
Channel Doping, N_d (cm^{-3})	1×10^{19}	1×10^{19}	
Core Doping, N_a (cm^{-3})	-	1×10^{19}	
Gate Workfunction (eV)	5.1 (ϕ_M)	5.1 (ϕ_{M1})	4.6 (ϕ_{M2})
Gate Oxide permittivity	3.9 (ε_{ox})	3.9 (ε_{ox})	
Gate Oxide Thickness, t_{ox} (nm)	1	1	

Figures 3.2 (a) and (b) illustrate the surface potential ($\phi_S(z)$) and electric field ($E(z)$), respectively, along the L_C of conventional JL-NWFET and DMG-CS-JL-NWFET by varying

t_{core} from 0 nm to 7 nm. The horizontal cut-line for extracting $\phi_S(z)$ and $E(z)$ is set 1 nm beneath the oxide-semiconductor interface. A close agreement is observed between the results obtained from the model and TCAD simulation, with an average deviation of 4.34% and 5.95% in Fig. 3 (a) and (b), respectively. These deviations are primarily due to the approximations used in the analytical model to simplify the equations and numerical precision in TCAD.

It is observed from Fig. 3.2 (a) that as t_{core} increases (0 to 7 nm) in the fixed t_{si} of 10 nm, the position of the minimum surface potential of region-1 shifts downward as compared to that of conventional JL-NWFET. This indicates that fewer dopants are available to screen the penetration of the gate electric field into the shell region, suggesting more efficient gate control over the channel in the subthreshold region. Additionally, a step-change in the $\phi_S(z)$ is observed at the M_1 and M_2 interface, unlike the smooth curve observed in conventional JL-NWFET. This is due to the difference in work function in DMG-CS-JL-NWFET, which enhances carrier transport efficiency in the shell region.



(a) (b)

Fig. 3.2 (a) Surface potential ($\phi_S(z)$) and (b) Electric field ($E(z)$) profile along channel length for conventional JL-NWFET and DMG-CS-JL-NWFET with different t_{core}

Figure 3.2 (b) depicts the electric peak at the interface of the DMG structure in DMG-CS-JL-NWFET, caused by gate work function difference in contrast to no transition curve of conventional JL-NWFET. Increasing t_{core} decreases the electric field peak due to the reduction in the active conduction area, and therefore, a thicker t_{core} (7 nm) reduces the subthreshold current as compared to a thinner t_{core} (3 nm). Furthermore, as t_{core} increases, the electric field decreases at the drain side as compared to conventional JL-NWFET. A high electric field near the drain side may result in the formation of highly energetic "hot carriers", which may cause the HCEs. Consequently, DMG-CS-JL-NWFET exhibits higher reliability against HCE than conventional JL-NWFET.

The surface potential along the L_C of DMG-CS-JL-NWFET is depicted in Fig. 3.3 for different t_{si} while keeping t_{core} as 5 nm. The results from the model and the TCAD simulation show an average deviation of 3.31%. As can be observed from Fig. 3.3, increasing t_{si} shifts the $\phi_S(z)$ upwards, implying reduced gate control over the shell region. This can lead to insufficient volume depletion of the shell region, as the thinner *p*-type core cannot deplete carriers in the thicker *n*-type shell region. Consequently, this results in a higher I_{OFF}. Therefore, a thicker, oppositely, and equally doped core should be used when designing DMG-CS-JL-NWFET in the subthreshold region.

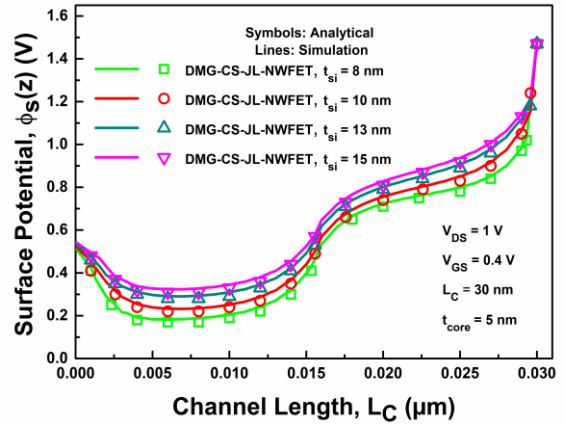


Fig. 3.3 Surface potential ($\phi_S(z)$) profile along channel length for DMG-CS-JL-NWFET with different t_{si}

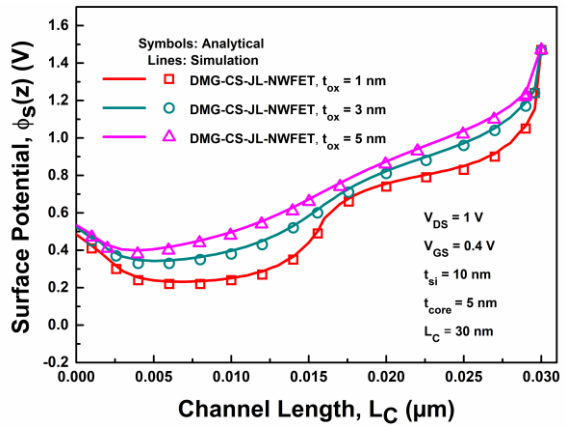
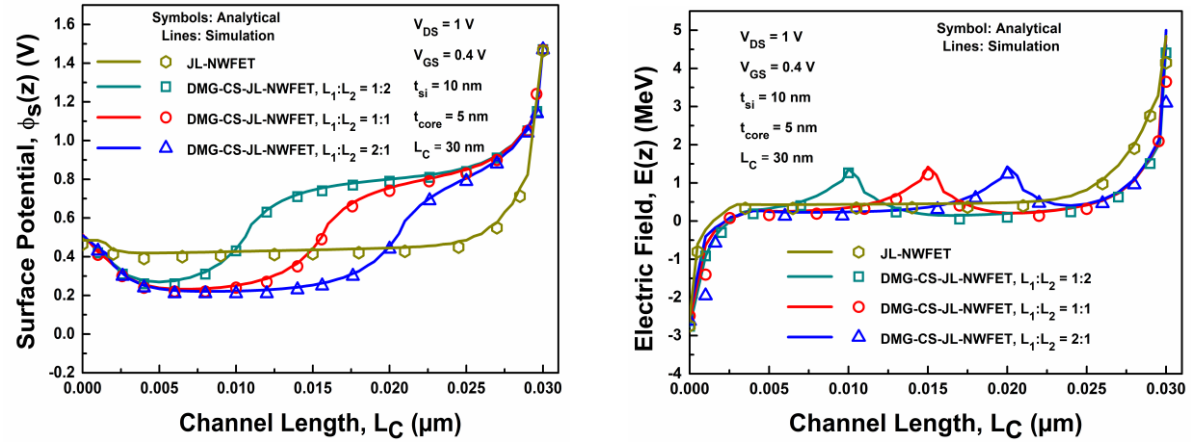


Fig. 3.4 Surface potential ($\phi_S(z)$) profile along channel length for different t_{ox} of DMG-CS-JL-NWFET

The impact of t_{ox} on the surface potential profile of DMG-CS-JL-NWFET is portrayed in Fig. 3.4. A deviation of 3.22% on average is observed in Fig. 3.4 between the results from the model and the TCAD simulation. As t_{ox} increases, C_{ox} decreases (Eqn. 3.9), which further increases the scaling length (λ) of DMG-CS-JL-NWFET (Eqn. 3.24) and the D_j factor in regions 1 and 2 (Eqn. 3.23) that consequently increases $\phi_S(z)$ (Eqn. 3.24 and 3.25). Therefore, $\phi_S(z)$ shifts upwards as t_{ox} increases from 1 nm to 5 nm. A thicker t_{ox} (5 nm) is not preferable because it resists the vertical electric field from the gate electrode penetrating the shell region, resulting

in poor electrostatic integrity. To enhance immunity against SCEs, a thinner t_{ox} (1 nm) should be utilized. However, further scaling down of the gate oxide thickness might lead to a decline in retention properties due to stress-induced leakage current [123].

Figures 3.5 (a) and (b) display surface potential ($\phi_S(z)$) and electric field ($E(z)$) profiles for the conventional JL-NWFET and DMG-CS-JL-NWFET with the influence of L_C ratios (L_1:L_2). Fig. 3.5 (a) shows an average deviation of 4.21% between the analytical results and TCAD simulation. It is observed from Fig. 3.5 (a) that conventional JL-NWFET have a smooth surface potential curve, while a step transition is seen for DMG-CS-JL-NWFET due to dissimilar gate work functions. Furthermore, as the L_1:L_2 ratio in DMG-CS-JL-NWFET increases, the position of minimum surface potential shifts towards the drain side. Moreover, when L_1 is small (L_1: L_2 = 1:2), the minimum surface potential ($\varphi_{S1,min}(z)$) is higher than that when the length of L_1 is large (L_1: L_2 = 2:1). For DMG-CS-JL-NWFET, the V_T is mainly determined by the minimum surface potential (Eqn. 3.54). Therefore, DMG-CS-JL-NWFET with a small ratio of L_1 will exhibit a small threshold V_T compared to a larger ratio of L_1.

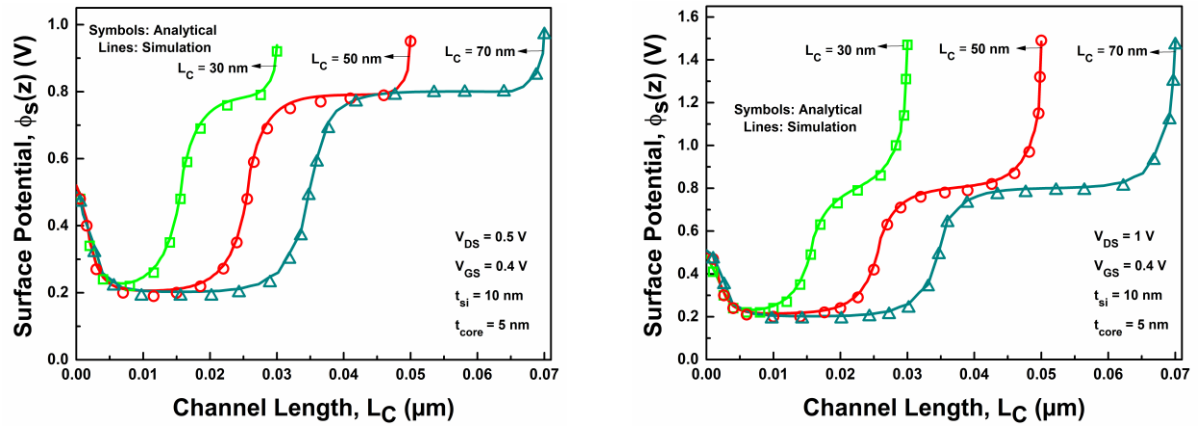


(a) (b)

Fig. 3.5 (a) Surface potential ($\phi_S(z)$) and (b) Electric field ($E(z)$) profile channel length for conventional JL-NWFET and DMG-CS-JL-NWFET with different L_1:L_2 ratios

The results from Fig. 3.5 (b) obtained using the model (Eqn. 3.48) show good agreement with the simulated results, with an average deviation of 5.73%. The electric field peak in Fig. 3.5 (b) is observed in DMG-CS-JL-NWFET due to the corresponding single-step change in the surface potential profile (Fig. 3.5 (a)), in contrast to the absence of an electric field peak in the conventional JL-NWFET. This electric field peak in DMG-CS-JL-NWFET can provide more acceleration to electrons in the channel and improve the efficiency of carrier transportation. It can be clearly seen from Fig. 3.5 (b) that the electric peak shifts towards the drain side as the L_1:L_2 ratios increase (1:2 to 2:1).

A high electric field peak near the drain side may cause HCE. A smaller L_1:L_2 ratio (L_1: L_2 = 1:2) results in a lower V_T, while a higher L_1:L_2 ratio (L_1: L_2 = 2:1) leads to increased HCE. Therefore, an L_1:L_2 ratio of 1:1 is preferred for DMG-CS-JL-NWFET in future practical applications. Fig. 3.6 (a) and (b) show the variation in surface potential of DMG-CS-JL-NWFET at different L_C of 30 nm, 50 nm, and 70 nm with V_{DS} = 0.5 V and 1 V, respectively. The analytical results deviate from TCAD simulation on an average of 4.15% and 5.57% in Fig. 3.6 (a) and (b), respectively. Notably, as L_C decreases (from 70 nm to 30 nm), minimum surface potential under M_1 is pulled upwards, leading to a reduction in V_T. This indicates that a shorter L_C causes V_T to be more influenced by drain bias, resulting in increased SCE such as DIBL.



(a) (b)

Fig. 3.6 Surface potential ($\phi_S(z)$) profile of DMG-CS-JL-NWFET along channel length for L_C = 30 nm, 50 nm, and 70 nm at (a) V_{DS} = 0.5 V and (b) V_{DS} = 1 V

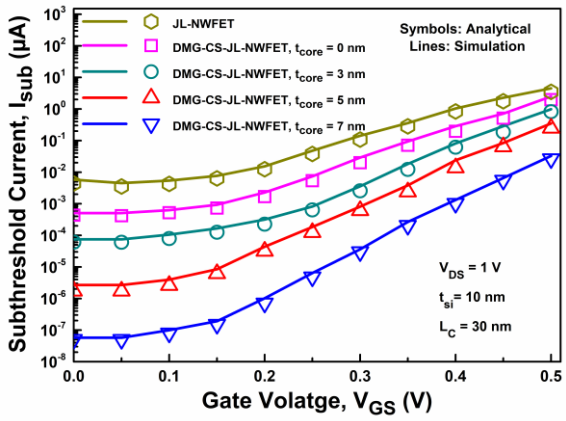


Fig. 3.7 Subthreshold current (I_{sub}) for conventional JL-NWFET and DMG-CS-JL-NWFET with different t_{core}

The subthreshold current (I_{sub}) of conventional JL-NWFET and DMG-CS-JL-NWFET for different t_{core} is shown in Fig. 3.7. A deviation of 19.41% on average is observed in Fig. 3.7 between the results from the model and the TCAD simulation. It is evident that I_{sub} decreases

with increasing t_{core} in comparison to conventional JL-NWFET, which is attributed to the reduction of the shell region where conduction occurs, as also explained in Fig. 3.2 (b). The presence of an oppositely doped core significantly reduces I_{OFF} (at V_{GS} = 0 V) as compared to that of the conventional JL-NWFET.

This is attributed to a thicker t_{core} also leads to the lowest I_{OFF} than a thinner t_{core} due to the fact that a thinner oppositely doped t_{core} may not fully deplete the shell region during the OFF-state. Additionally, I_{sub} significantly decreases when t_{core} exceeds 5 nm, which is half of the channel thickness. It has been demonstrated that for efficient design, a core-shell structure in DMG-JL-NWFET with a t_{core} should be half of t_{si}, as it effectively reduces I_{OFF} with minimal degradation on I_{sub}. However, increasing the t_{core} beyond 50% of t_{si} in DMG-CS-JL-NWFET significantly reduces I_{OFF}, but also leads to a substantial reduction in I_{sub}. Therefore, for t_{si} of 10 nm, a t_{core} of 5 nm is considered to be optimal for DMG-CS-JL-NWFET.

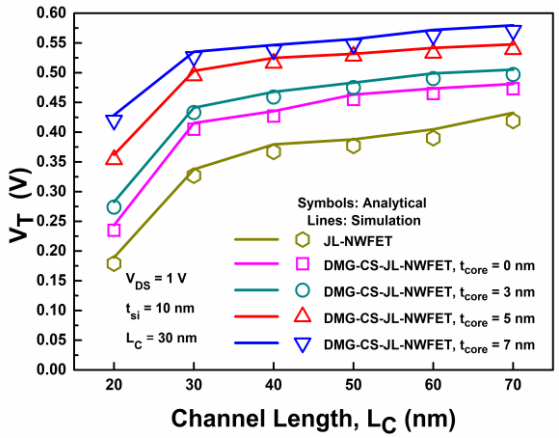
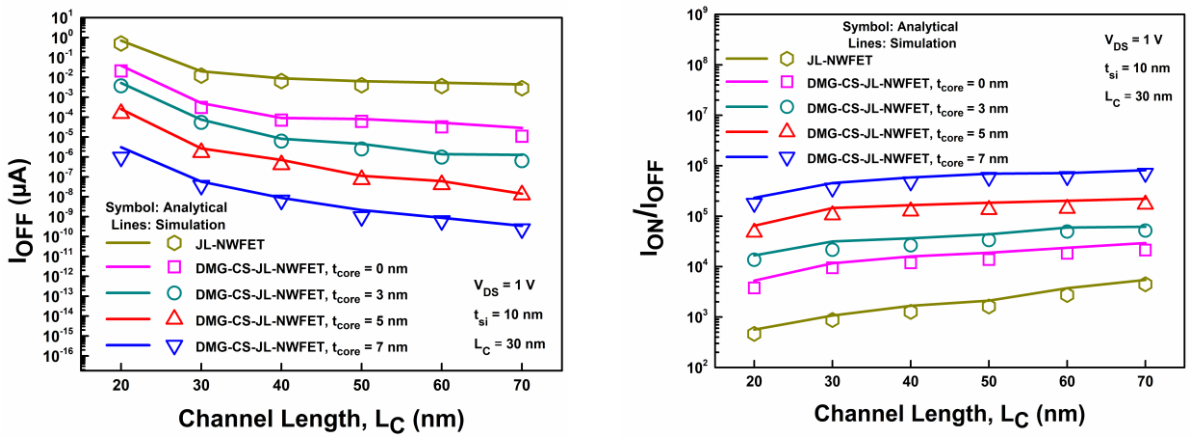


Fig. 3.8 Variation of V_T with L_C for conventional JL-NWFET and DMG-CS-JL-NWFET with different t_{core}

Figure 3.8 presents the impact of L_C scaling (from 70 nm to 20 nm) on V_T of conventional JL-NWFET and DMG-CS-JL-NWFET with different t_{core}. An average deviation of 2.85% is observed in Fig. 3.8 between the analytical result and TCAD simulation. It is observed that V_T decreases on scaling down L_C at any given t_{core}, as already explained in Fig. 3.6 (a) and (b). Additionally, a significant reduction in V_T is noticed at 20 nm of L_C across all t_{core} values, indicating diminished gate control over the channel. For any specific L_C, a thicker t_{core} (7 nm) results in a higher V_T than the conventional DMG-JL-NWFET (with t_{core} = 0) and conventional JL-NWFET. This is due to the fact that a thicker oppositely doped t_{core} facilitates complete depletion of the shell region in the OFF-state, thereafter requiring a higher gate voltage to initiate conduction. Moreover, the complete depletion of carriers in the shell region leads to a reduced I_{OFF}.

The impact of L_C scaling on the I_{OFF} and I_{ON}/I_{OFF} ratio of conventional JL-NWFET and DMG-CS-JL-NWFET for various t_{core} values are depicted in Fig. 3.9 (a) and (b), respectively. The results obtained from the model and TCAD simulation show an average deviation of 14.28% and 22.51% in Fig. 3.9 (a) and (b), respectively. The conventional JL-NWFET exhibits the highest I_{OFF} at any specific L_C. However, I_{OFF} reduces with the increase in oppositely doped t_{core} (ranging from 0 to 7 nm) as fewer carriers are available in the shell region during OFF-state at any given L_C, as also discussed in Fig. 3.7. Moreover, at fixed t_{core}, I_{OFF} rises on decreasing L_C due to an increase in drain voltage control and the decrease in gate voltage control on the channel's electrostatics which is also depicted in Fig. 3.9. However, a thicker t_{core} (7 nm) lessens drain voltage control over the channel compared to a thinner t_{core} (3 nm) or the absence of a core (0 nm).



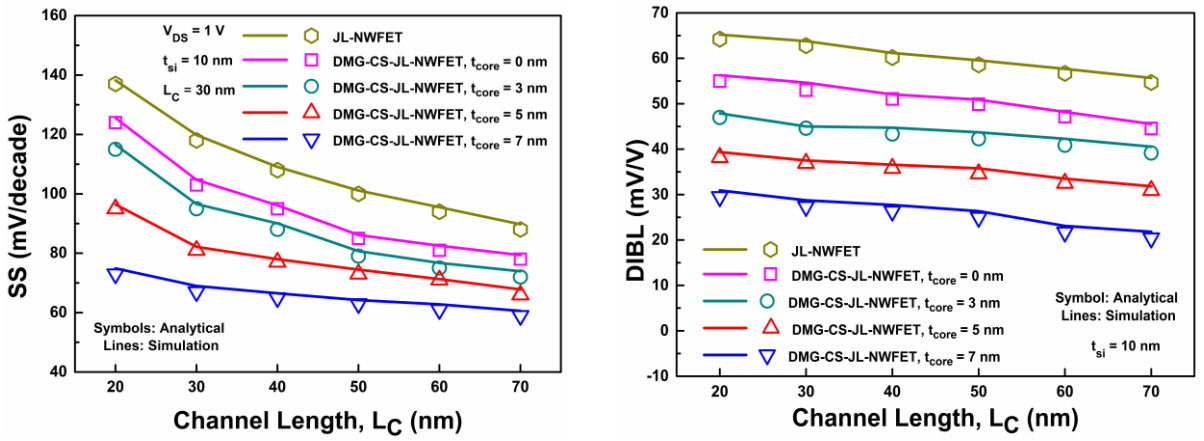
(a) (b)

Fig. 3.9 Variation of (a) I_{OFF} and (b) I_{ON}/I_{OFF} ratio with L_C for conventional JL-NWFET and DMG-CS-JL-NWFET with different t_{core}

It is noted in Fig. 3.9 (b) that DMG-CS-JL-NWFET achieves the highest I_{ON}/I_{OFF} ratio compared to conventional JL-NWFET for any specific L_C. Although increasing t_{core} reduces I_{sub}, as observed in Fig. 3.7, the I_{ON}/I_{OFF} ratio increases with t_{core} due to a significant decrease in I_{OFF}, as observed in Fig. 3.9 (a). Furthermore, the I_{ON}/I_{OFF} ratio for both conventional JL-NWFET and DMG-CS-JL-NWFET decreases when L_C is scaled down from 70 to 20 nm, primarily due to a substantial increase in I_{OFF}, caused by reduced gate voltage control over channel electrostatics. This is also illustrated in Fig. 3.8, where a significant decrease in V_T is observed at smaller L_C.

Figures 3.10 (a) and (b) demonstrate the variation of SS and DIBL with scaling of L_C of conventional JL-NWFET and DMG-CS-JL-NWFET for different values of t_{core}, respectively. The analytical results deviate from TCAD simulation on an average of 2.68% and 2.81% in

Fig. 3.10 (a) and (b), respectively. It is observed that SS is the highest for conventional JL-NWFET and lowest for DMG-CS-JL-NWFET with thicker t_{core} (7 nm) at any given L_C due to reduced I_{OFF}, as can be seen in Fig. 3.9 (a), which makes the slope steeper.



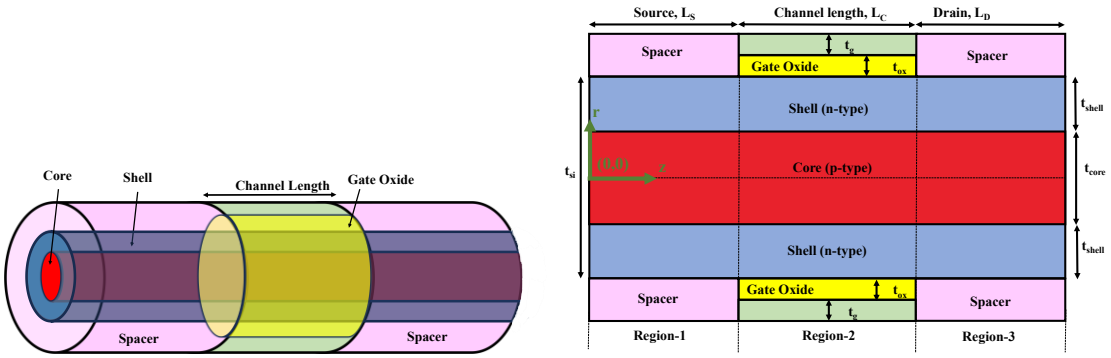
(a) (b)

Fig. 3.10 Variation of (a) SS and (b) DIBL with L_C for conventional JL-NWFET and DMG-CS-JL-NWFET with different t_{core}

Furthermore, SS increases with increasing L_C for both conventional JL-NWFET and DMG-CS-JL-NWFET with fixed t_{core} due to reduced gate voltage control over the channel region and enhancement in I_{OFF}. Fig. 3.10 (b) shows that the DMG-CS-JL-NWFET exhibits lower DIBL than the conventional JL-NWFET for any specific L_C. Increasing t_{core} (from 0 nm to 7 nm) reduces DIBL in the DMG-CS-JL-NWFET due to improved gate control over the shell region of the channel, which minimizes the influence of drain bias. However, DIBL increases with decreasing L_C due to enhanced SCEs in smaller L_C, as discussed in Fig. 3.6 (a) and (b).

3.3 ANALYTICAL MODELING OF JL-NWFET WITH CS AND GSS

The 3-D and 2-D structure of the JL-NWFET with CS and GSS (GSS-CS-JL-NWFET) are depicted in Fig. 3.11 (a) and (b), respectively. The GSS-CS-JL-NWFET consists of three regions: the source extension under the spacer (region-1), the channel region under the gate oxide (region-2), and the drain extension under the spacer (region-3). It may be noted that in GSS-CS-JL-NWFET, $L_{sp} = L_{S/D}$, where L_{sp} is the spacer length. The HfO_2 and SiO_2 are used as the spacer material and gate oxide, respectively.



(a) (b)

Fig. 3.11 (a) 3-D view and (b) 2-D schematic of GSS-CS-JL-NWFET

3.3.1 Surface Potential Modeling

Solving the 2-D Poisson's equation can determine silicon's surface electrostatic potential and electric field distribution. The electrostatic potential in the core and shell region of the channel can be expressed as follows:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\psi_{core,k}(r,z)\right)+\frac{\partial^2\psi_{core,k}(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}}\ for\ 0\le r\le\frac{t_{core}}{2},k=1,2,3 \tag{3.67}$$

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\psi_{shell,k}(r,z)\right)+\frac{\partial^2\psi_{shell,k}(r,z)}{\partial z^2}=\frac{-qN_d}{\varepsilon_{si}}\ for\ \frac{t_{core}}{2}\le r\le\frac{t_{si}}{2},k=1,2,3 \tag{3.68}$$

Here, potential distribution in core and shell region of the channel for the kth region (k = 1, 2, 3), permittivity of silicon, acceptor concentration, electronic charge, and donor concentration are denoted as $\psi_{core}(r,z)$, $\psi_{shell}(r,z)$, ε_{si}, N_a, q, and N_d respectively. The potential distributions along the radial direction in both the core and shell regions are described using the parabolic potential approximation [47] and are expressed as follows

$$\psi_{core,k}(r,z)=Y_{0k}(z)+Y_{1k}(z)r+Y_{2k}(z)r^2 \tag{3.69}$$

$$\psi_{shell,k}(r,z)=Z_{0k}(z)+Z_{1k}(z)\left(r-\frac{t_{core}}{2}\right)+Z_{2k}(z)\left(r-\frac{t_{core}}{2}\right)^2 \tag{3.70}$$

Using the following boundary conditions (viii-xi), the arbitrary coefficients Y_{0k}, Y_{1k}, Y_{2k}, Z_{0k}, Z_{1k}, and Z_{2k} can be determined.

(viii) The central potential ($\psi_{Ck}(z)$) and surface potential ($\psi_{Sk}(z)$) are as follow

$$\psi_{core,k}(0,z)=\psi_{Ck}(z)\ \text{and}\ \psi_{shell,k}\left(\frac{t_{si}}{2},z\right)=\psi_{Sk}(z) \tag{3.71}$$

(ix) The electric field in the center of the core region of the channel is zero by symmetry of channel potential.

$$\left.\frac{\partial \psi_{core,k}(r,z)}{\partial r}\right|_{r=0} = 0 \tag{3.72}$$

(x) The electric field at the surface is continuous.

$$\left.\frac{\partial \psi_{shell,k}(r,z)}{\partial r}\right|_{r=\frac{t_{si}}{2}} = \frac{C_k\left(V_{GS} - V_{fb} - \psi_{Sk}(z)\right)}{\varepsilon_{si}} \tag{3.73}$$

Where V_{fb} signifies the flat band voltage. C_k is the capacitance per unit area for the kth region and is given as

$$C_1 = C_3 = \frac{\left(C_{if} + C_{of}\right)}{\pi t_{si}} \tag{3.74}$$

$$C_2 = \frac{\varepsilon_{ox}}{\frac{t_{si}}{2}\ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)} \tag{3.75}$$

Here, C_1 and C_3 represent fringe capacitance per unit area, which is the combination of inner fringe capacitance per unit width (C_{if}) and outer fringe capacitance per unit width (C_{of}). Generally, C_{of} originates from both gate electrodes through the spacer dielectric, as illustrated in Fig. 3.12. Furthermore, oxide capacitance per unit area and gate oxide permittivity are represented by C_2 and ε_{ox}, respectively, in region-2. C_{if} and C_{of} are expressed as [124]

$$C_{if} = \frac{6\varepsilon_{ox}}{\pi}\ln\left(\frac{t_{ox} + t_{si}sin\delta}{t_{ox}cos\delta + f_{if}L_{sp}sin\delta}\right) \tag{3.76}$$

$$C_{of} = \frac{2\varepsilon_{sp}}{\pi} ln\left(\frac{t_g + t_{ox}}{L_{sp}}\right) \tag{3.77}$$

here, f_{if}, ε_{sp}, t_g, and δ denote tuning parameter, spacer permittivity, gate electrode thickness, and plate angle, respectively.

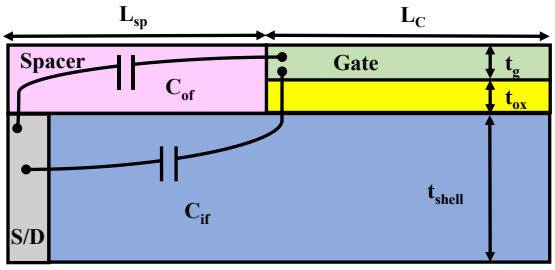


Fig. 3.12 Depiction of outer fringe and inner fringe capacitance of GSS-CS-JL-NWFET

(xi) The potentials and electric fields in the radial direction at the boundary between the core and shell regions must be continuous.

$$\psi_{core,k}\left(\frac{t_{core,k}}{2},z\right)=\psi_{shell,k}\left(\frac{t_{core,k}}{2},z\right) \tag{3.78}$$

$$\left.\frac{\partial\psi_{core,k}(r,z)}{\partial r}\right|_{r=\frac{t_{core}}{2}}=\left.\frac{\partial\psi_{shell,k}(r,z)}{\partial r}\right|_{r=\frac{t_{core}}{2}} \tag{3.79}$$

Using boundary conditions (viii)–(xi), arbitrary coefficients in Eqns. 3.69 and 3.70 are expressed as

$$Y_{0k}(z)=\psi_{Ck}(z) \tag{3.80}$$

$$Y_{1k}(z)=0 \tag{3.81}$$

$$Y_{2k}(z)=\frac{\left(4\varepsilon_{si}+C_k\left(t_{si}-t_{core}\right)\right)\psi_{Sk}(z)-4\varepsilon_{si}\psi_{Ck}(z)-C_k\left(t_{si}-t_{core}\right)\left(V_{GS}-V_{fb}\right)}{\varepsilon_{si}t_{si}t_{core}} \tag{3.82}$$

$$Z_{0k}(z)=\frac{\left(4\varepsilon_{si}t_{core}+C_kt_{core}\left(t_{si}-t_{core}\right)\right)\psi_{Sk}(z)+4\varepsilon_{si}\left(t_{si}-t_{core}\right)\psi_{Ck}(z)-C_kt_{core}\left(t_{si}-t_{core}\right)\left(V_{GS}-V_{fb}\right)}{4\varepsilon_{si}t_{si}} \tag{3.83}$$

$$Z_{1k}(z)=\frac{\left(4\varepsilon_{si}+C_k\left(t_{si}-t_{core}\right)\right)\psi_{Sk}(z)-4\varepsilon_{si}\psi_{Ck}(z)-C_k\left(t_{si}-t_{core}\right)\left(V_{GS}-V_{fb}\right)}{\varepsilon_{si}t_{si}} \tag{3.84}$$

$$Z_{2k}(z)=\frac{\left(-4\varepsilon_{si}-C_k\left(2t_{si}-t_{core}\right)\right)\psi_{Sk}(z)+4\varepsilon_{si}\psi_{Ck}(z)+C_k\left(2t_{si}-t_{core}\right)\left(V_{GS}-V_{fb}\right)}{\varepsilon_{si}t_{si}\left(t_{si}-t_{core}\right)} \tag{3.85}$$

$\psi_{Ck}(z)$ can be written in terms of $\psi_{Sk}(z)$ by solving Eqns. 3.67 and 3.68 simultaneously using Eqns. 3.69 and 3.70 at $r = t_{core}$ and is derived as

$$\psi_{Ck}(z)=\frac{\left(8\varepsilon_{si}+2C_kt_{si}\right)\psi_{Sk}(z)-2C_kt_{si}\left(V_{GS}-V_{fb}\right)-q\left(N_a+N_d\right)t_{core}\left(t_{si}-t_{core}\right)}{8\varepsilon_{si}} \tag{3.86}$$

By using Eqns. 3.70 and 3.86 to solve Eqn. 3.68 at $r = t_{si}/2$, the differential equation for $\psi_{Sk}(z)$ can be represented as:

$$\frac{\partial^2\psi_{Sk}(z)}{\partial z^2}-\frac{\left(\psi_{Sk}(z)-W_k\right)}{\lambda_k{}^2}=0 \tag{3.87}$$

$$\lambda_k{}^2=\frac{\varepsilon_{si}t_{si}}{4C_k} \tag{3.88}$$

$$W_k=V_{GS}+\gamma_k \tag{3.89}$$

$$\gamma_k=\frac{qN_dt_{si}-qt_{core}\left(N_a+N_d\right)}{4C_k}-V_{fb} \tag{3.90}$$

where λ_k represents the scaling length of GSS-CS-JL-NWFET. It may be noted again that the λ_k is the same as that of a conventional Double Gate (DG) JL-MOSFET [121] without core-

shell architecture. Additionally, W_k also matches that of a standard DG-JL-MOSFET [121]. The general solution for the second-order differential Eqn. 3.87 for all three regions is expressed as

$$\psi_{S1}(z) = M_1 e^{z/\lambda_1} + N_1 e^{-z/\lambda_1} + W_1 \tag{3.91}$$

$$\psi_{S2}(z) = M_2 e^{(z-L_S)/\lambda_2} + N_2 e^{-(z-L_S)/\lambda_2} + W_2 \tag{3.92}$$

$$\psi_{S3}(z) = M_3 e^{(z-L_S-L_C)/\lambda_3} + N_3 e^{-(z-L_S-L_C)/\lambda_3} + W_3 \tag{3.93}$$

To solve arbitrary constants, the following boundary conditions are used.

(xii) The surface potential in the region-1 at the source side

$$\psi_{S1}(z=0) = V_{bi} = \frac{KT}{q}\ln\left(1+\frac{N_d}{n_i}\right) \tag{3.94}$$

Where V_{bi}, K, T, and n_i signify built-in potential, Boltzmann constant, thermal temperature, and intrinsic concentration, respectively.

(xiii) The surface potential in the region-3 at the drain side

$$\psi_{S3}(z = L_S + L_C + L_D) = V_{bi} + V_{DS} \tag{3.95}$$

(xiv) At the interface of regions 1–2 and 2–3, the surface potential and electric field exhibit continuity.

$$\psi_{S1}(z = L_S) = \psi_{S2}(z = L_S) \tag{3.96}$$

$$\psi_{S2}(z = L_S + L_C) = \psi_{S3}(z = L_S + L_C) \tag{3.97}$$

$$\left.\frac{\partial \psi_{S1}(z)}{\partial r}\right|_{z=L_S} = \left.\frac{\partial \psi_{S2}(z)}{\partial r}\right|_{z=L_S} \tag{3.98}$$

$$\left.\frac{\partial \psi_{S2}(z)}{\partial r}\right|_{z=L_S+L_C} = \left.\frac{\partial \psi_{S3}(z)}{\partial r}\right|_{z=L_S+L_C} \tag{3.99}$$

M_k and N_k for k = 1, 2, 3 are obtained by solving abovementioned boundary conditions (xii)-(xiv) and expressed as

$$M_1 = \left(1+\frac{\lambda_1}{\lambda_2}\right)\left(\frac{e^{-L_S/\lambda_1}}{2}\right)M_2 + \left(1-\frac{\lambda_1}{\lambda_2}\right)\left(\frac{e^{-L_S/\lambda_1}}{2}\right)N_2 + \left(\frac{e^{-L_S/\lambda_1}}{2}\right)(W_2 - W_1) \tag{3.100}$$

$$N_1 = \left(1-\frac{\lambda_1}{\lambda_2}\right)\left(\frac{e^{L_S/\lambda_1}}{2}\right)M_2 + \left(1+\frac{\lambda_1}{\lambda_2}\right)\left(\frac{e^{L_S/\lambda_1}}{2}\right)N_2 + \left(\frac{e^{L_S/\lambda_1}}{2}\right)(W_2 - W_1) \tag{3.101}$$

$$M_3 = \left(1+\frac{\lambda_3}{\lambda_2}\right)\left(\frac{e^{L_C/\lambda_2}}{2}\right)M_2 + \left(1-\frac{\lambda_3}{\lambda_2}\right)\left(\frac{e^{-L_C/\lambda_2}}{2}\right)N_2 + \frac{(W_2 - W_3)}{2} \tag{3.102}$$

$$N_3 = \left(1-\frac{\lambda_3}{\lambda_2}\right)\left(\frac{e^{L_C/\lambda_2}}{2}\right)M_2 + \left(1+\frac{\lambda_3}{\lambda_2}\right)\left(\frac{e^{-L_C/\lambda_2}}{2}\right)N_2 + \frac{(W_2-W_3)}{2} \tag{3.103}$$

$$M_2 = \frac{(F_1-V_{GS})A-(F_2-V_{GS})C}{AB-CD} \tag{3.104}$$

$$N_2 = \frac{(F_2-V_{GS})B-(F_1-V_{GS})D}{AB-CD} \tag{3.105}$$

$$A = \cosh\left(\frac{L_S}{\lambda_1}\right)+\left(\frac{\lambda_1}{\lambda_2}\right)\sinh\left(\frac{L_S}{\lambda_1}\right) \tag{3.106}$$

$$B = \left[\cosh\left(\frac{L_D}{\lambda_3}\right)+\left(\frac{\lambda_3}{\lambda_2}\right)\sinh\left(\frac{L_D}{\lambda_1}\right)\right]e^{L_C/\lambda_2} \tag{3.107}$$

$$C = \left[\cosh\left(\frac{L_D}{\lambda_3}\right)-\left(\frac{\lambda_3}{\lambda_2}\right)\sinh\left(\frac{L_D}{\lambda_1}\right)\right]e^{-L_C/\lambda_2} \tag{3.108}$$

$$D = \cosh\left(\frac{L_S}{\lambda_1}\right)-\left(\frac{\lambda_1}{\lambda_2}\right)\sinh\left(\frac{L_S}{\lambda_1}\right) \tag{3.109}$$

$$F_1 = V_{bi}+V_{DS}-\gamma_3-(\gamma_2-\gamma_3)\cosh\left(\frac{L_D}{\lambda_3}\right) \tag{3.110}$$

$$F_2 = V_{bi}-\gamma_1-(\gamma_2-\gamma_1)\cosh\left(\frac{L_S}{\lambda_1}\right) \tag{3.111}$$

3.3.2 Threshold Voltage, Drain Current, and Subthreshold Slope Modeling

To derive the V_T for GSS-CS-JL-NWFET, the minimum surface potential ($\psi_{S2,min}(z)$) of the channel region (region-2) is set to zero [121]. The position of minimum surface potential (zmin) is determined by differentiating Eqn. 3.92 and equating the result to zero.

$$\left.\frac{d\psi_{S2}(z)}{dz}\right|_{z=z\min} = 0 \tag{3.112}$$

$$z\min = L_S + \frac{\lambda_2}{2}\ln\left(\frac{Z_2}{Y_2}\right) \tag{3.113}$$

$$\psi_{S2,\min}(z)\big|_{z=z\min} = 2\sqrt{Y_2 Z_2}+W_2 \tag{3.114}$$

By setting $\psi_{S2,min(z)}$ to zero and solving for V_{GS}, the V_T can be determined as

$$V_T = \frac{-(2\alpha_1\alpha_4+2\alpha_2\alpha_3-\gamma_2)+\sqrt{(2\alpha_1\alpha_4+2\alpha_2\alpha_3-\gamma_2)^2-(4\alpha_1\alpha_2-1)(\alpha_2\alpha_4-\gamma_2{}^2)}}{4\alpha_1\alpha_2-1} \tag{3.115}$$

$$\alpha_1 = \frac{AF_1-CF_2}{AB-CD} \tag{3.116}$$

$$\alpha_2 = \frac{C - A}{AB - CD} \tag{3.117}$$

$$\alpha_3 = \frac{BF_2 - DF_1}{AB - CD} \tag{3.118}$$

$$\alpha_4 = \frac{D - B}{AB - CD} \tag{3.119}$$

The subthreshold drain current (I_{sub}) for $0 \leq V_{GS} < V_T$, the drain current in the linear region (I_{lin}) for $V_T \leq V_{GS} < V_{DS} + V_T$, and the drain current in the saturation region (I_{sat}) for $V_{DS} + V_T \leq V_{GS} \leq V_{DD}$ constitute the total I_{DS} of GSS-CS-JL-NWFET. The corresponding expressions for I_{sub} [122], I_{lin} [125, 126], and I_{sat} [125, 126] are as follows

$$I_{sub} = \frac{\pi t_{si} KT\left(1 - e^{-qV_{DS}/KT}\right)}{\int_0^{L_S} \frac{dz}{H_1(z)} + \int_{L_S}^{L_S+L_C} \frac{dz}{H_2(z)} + \int_{L_S+L_C}^{L_S+L_C+L_D} \frac{dz}{H_3(z)}} \tag{3.120}$$

$$H_k(z) = n_i \mu'_p \int_0^{t_{core}/2} e^{\left(\frac{q\psi_{core,k}(r,z)}{KT}\right)} dr + n_i \mu'_e \int_{t_{core}/2}^{t_{si}/2} e^{\left(\frac{q\psi_{shell,k}(r,z)}{KT}\right)} dr \tag{3.121}$$

$$\mu'_p = \frac{\mu_p}{1 + \eta\left(V_{GS} - V_T\right)} \text{ and } \mu'_e = \frac{\mu_e}{1 + \eta\left(V_{GS} - V_T\right)} \tag{3.122}$$

$$I_{lin} = \sum_{k=1}^{3} \left[\frac{\beta_k \left(\left(V_{GS} - V'_T\right) V_{DS} - \frac{1}{2} V_{DS}^2 \right)}{L_k \left(1 - \frac{l_d}{L_k} + \frac{V_{DS}}{L_k E_C} \right)} \right] \tag{3.123}$$

$$I_{sat} = \sum_{k=1}^{3} \left[\frac{\beta_k \left(V_{GS} - V'_T\right) V_{DS,sat}}{L_k \left(1 - \frac{l_d}{L_k} + \frac{V_{DS,sat}}{L_k E_C} \right)} \right] \tag{3.124}$$

$$SS = \frac{\partial V_{GS}}{\partial log_{10}(I_{DS})} \tag{3.125}$$

Here, μ_p is low field hole mobility [125], μ_e is low field electron mobility [125], η is fitting parameter [125], $V'_T = V_T - DIBL$ is the effective threshold voltage [125], $\beta_k = \pi(t_{si} - t_{core})\mu'_e C_k + \pi t_{core}\mu'_p C_k$ is the process parameter, $E_C = \frac{2\,ves}{\mu' e}$ is *the* critical electric field at which electron velocity (v_{es}) saturates [126], l_d is the channel length modulation factor [126], and $V_{DS,sat} = \frac{V_{GS} - V_T}{1 + \frac{V_{GS} - V_T}{L_C E_C}}$ is saturation voltage [126]. Furthermore, the SS is defined as the variation in V_{GS} required for every tenfold increase in I_{DS} and can be expressed as Eqn. 3.125.

3.3.3 Validation of Analytical Modeling of JL-NWFET with CS and GSS through Simulation Analysis

Unless specified otherwise, the N_d is taken as 1×10^{19} cm^{-3}, t_{ox} = 1 nm, gate work function (ϕ_M) =5.1 eV, $L_{sp} = L_{S/D}$ = 25 nm, and ε_{ox} = 3.9. The developed model is first analyzed for the surface potential of GSS-CS-JL-NWFET with the L_C of 30 nm and t_{si} of 10 nm while varying the t_{core} from 0 to 7 nm. Different spacer materials, including air, Al_2O_3, HfO_2, and Ta_2O_5, with permittivity of 1, 9.3, 22, and 26, respectively, are also considered to analyse the effect of fringe capacitance. Furthermore, to see the effect of core doping on the performance of GSS-CS-JL-NWFET, the N_a has been varied from 1×10^{15} cm^{-3} to 1×10^{20} cm^{-3}. Subsequently, the impact of scaling L_C from 70 nm to 20 nm on the device parameters is evaluated.

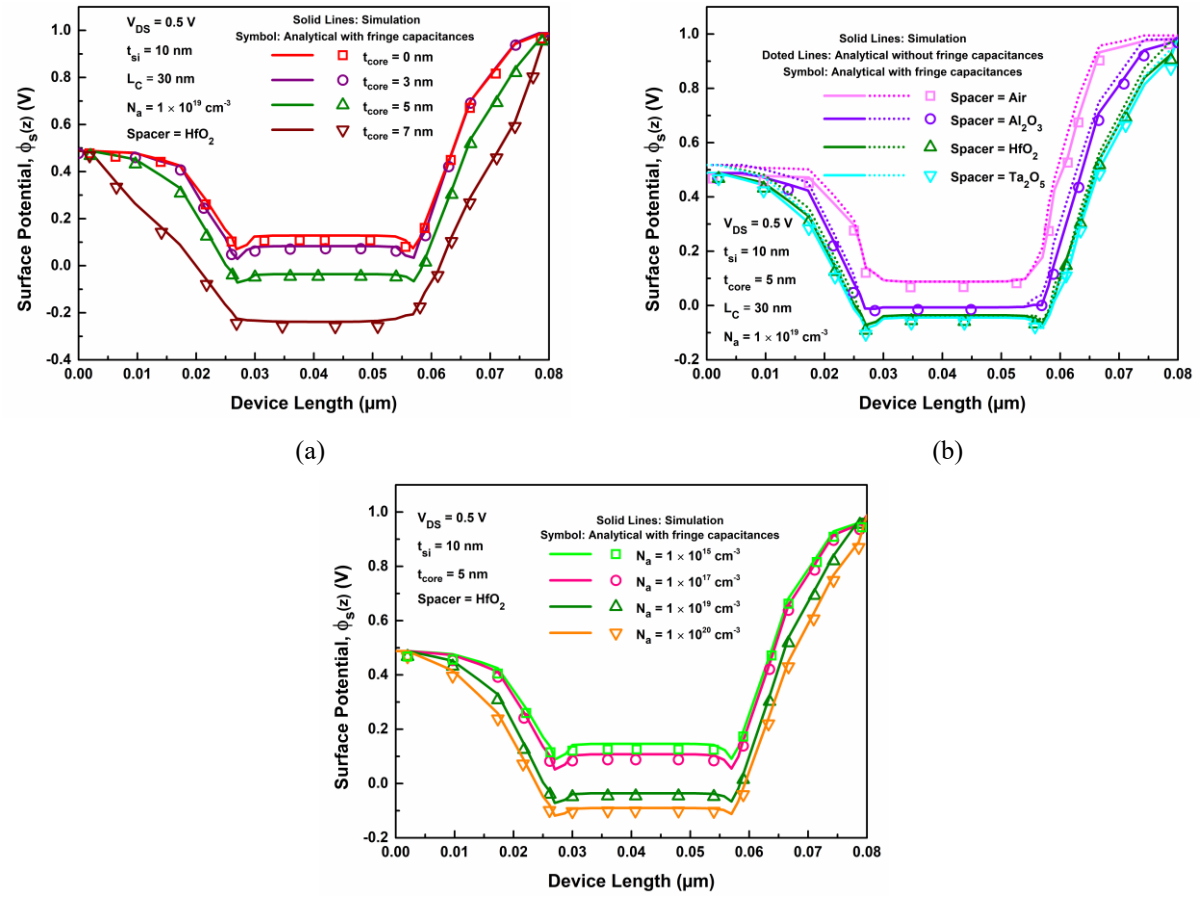


Fig. 3.13 Surface potential ($\phi_S(z)$) profile along device length of GSS-CS-JL-NWFET at V_{GS} = 0 V for different (a) core thicknesses, (b) spacer materials with and without fringe capacitances, and (c) core doping concentrations

Figure 3.13 (a) portrays the surface potential ($\phi_S(z)$) of GSS-CS-JL-NWFET along the device length, with t_{core} varying from 0 nm to 7 nm while maintaining HfO_2 as spacer material in OFF-state (V_{GS} = 0 V). The surface potential is extracted using the horizontal cut-line at 1 nm beneath

the oxide-semiconductor interface during TCAD simulations. A close correlation is observed between the results from the analytical model and the TCAD simulation. It may be noted that zero t_{core} corresponds to a conventional JL-NWFET with a GSS without a core-shell structure.

It is observed from Fig. 3.13 (a) that as t_{core} increases from 0 to 7 nm, with a fixed t_{si} of 10 nm, the minimum surface potential in the channel region (region-2) shifts downward. This implies that fewer dopants are present to shield the gate electric field's penetration into the shell region, indicating enhanced gate control over the shell region. Moreover, the expansion of the oppositely doped t_{core} suppresses the shell region, which serves as the primary conduction area, depleting it in the OFF-state, and consequently reducing leakage current. The surface potential profile of GSS-CS-JL-NWFET at a fixed t_{core} of 5 nm with different spacer materials, in the OFF-state, both with and without consideration of fringe capacitances in the analytical model, is shown in Fig. 3.13 (b).

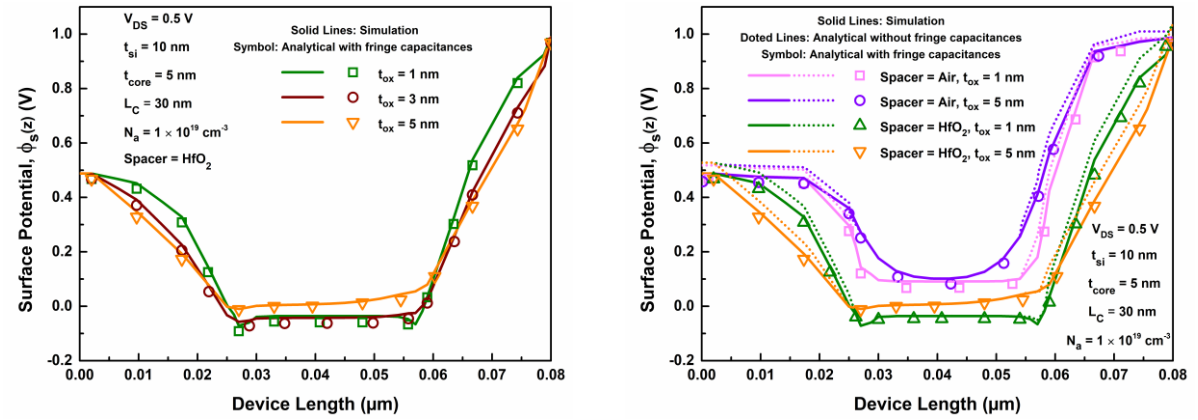
It may be noted that air denotes the absence of spacer material, and the device corresponds to a conventional oppositely doped core-shell JL-NWFET. As observed, the analytical result with the consideration of fringe capacitances aligns well with the simulation result. The spacer having high permittivity (Al_2O_3, HfO_2, Ta_2O_5) shifts the minimum surface potential downward as compared to the air spacer. This effect can be attributed to the fact that a high-permittivity spacer enhances the fringing electric field, leading to increased depletion beyond the channel region during the OFF-state [22]. The vertical electric field experiences fewer carriers, further shifting the surface potential downward.

However, it is also observed that there is no significant further reduction in surface potential when changing the spacer material from HfO_2 to Ta_2O_5. Therefore, the choice of spacer material with a permittivity higher than HfO_2 does not result in substantial performance improvement in terms of surface potential reduction. Besides this, without considering the fringe capacitance effects in the analytical model, the surface potential increases in the S/D extension, deviating from the simulation result. This discrepancy arises because the model does not capture the increased fringing electric field due to fringe capacitance, which can shift the surface potential upward in the S/D extension to match the simulation result.

Furthermore, no significant change in surface potential is observed in the channel region as fringe capacitances only affect the regions beyond the channel, primarily in the S/D extensions. The effect of different p-type core doping on the surface potential profile of GSS-CS-JL-NWFET by varying it from 1×10^{15} cm^{-3} to 1×10^{20} cm^{-3}, with fixed n-type shell doping of 1×10^{19} cm^{-3} in the OFF-state, is demonstrated in Fig. 3.13 (c). The surface potential shifts

upward with decreasing core doping, as a lightly doped core with 1×10^{15} cm^{-3} concentration may not be able to deplete the channel during the OFF-state, and the vertical electric field may not shift the surface potential downward due to the presence of carriers in the shell region. Conversely, a heavily doped core with a concentration of 1×10^{20} cm^{-3} shifts the surface potential downward as it depletes the shell region more effectively.

Figure 3.14 (a) compares the surface potential profile of GSS-CS-JL-NWFET for different t_{ox} at specific t_{core} (5 nm) and spacer (HfO_2) in the OFF-state. The plot indicates that as the t_{ox} increases from 1 nm to 5 nm, the surface potential shifts upwards, suggesting that the vertical electric field from the gate struggles to penetrate the thicker oxide layer, weakening the gate's control over the channel. Fig. 3.14 (b) demonstrates the surface potential profile of GSS-CS-JL-NWFET for different spacers and t_{ox} at fixed t_{core} in the OFF-state. The analytical model that accounts for fringe capacitances closely matches the simulation results, whereas the model without fringe capacitances shows significant deviation.



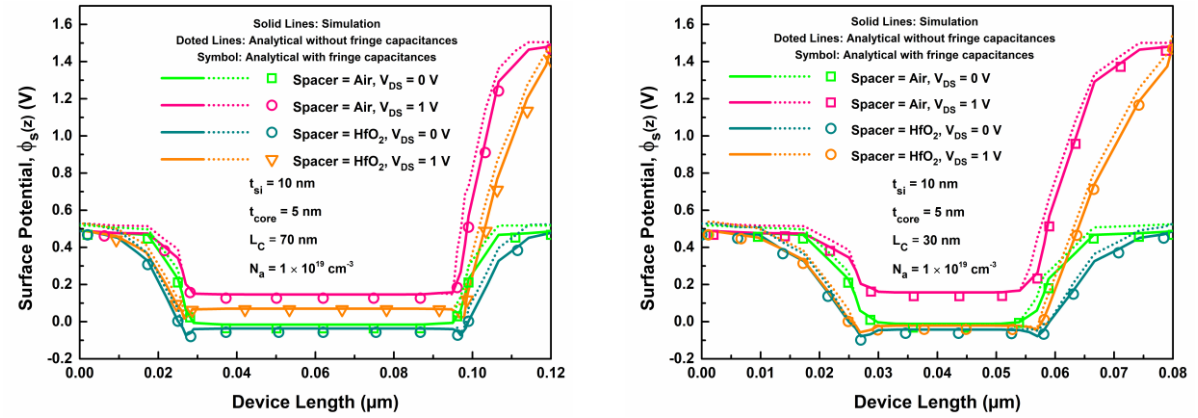
(a) (b)

Fig. 3.14 Surface potential ($\phi_{S(z)}$) profile along device length of GSS-CS-JL-NWFET for different (a) t_{ox} and (b) spacer materials with and without fringe capacitances and t_{ox}

This is due to the fact that the absence of fringe capacitance in the analytical model increases the surface potential in the S/D extension regions. Furthermore, it is observed that at a specific t_{ox}, the high-k GSS (HfO_2) shifts the surface potential downward. This occurs because the high-k GSS over the S/D extension enhances carrier depletion by increasing the fringing electric field, which leads to a downward shift in the surface potential. Although a thin t_{ox} is preferred to improve control, it can also increase leakage current. Therefore, using a high-permittivity spacer along with a thicker t_{ox} is recommended.

To understand the effect of drain bias on the scaling of L_C, the surface potential of GSS-CS-JL-NWFET for different V_{DS} and spacers at L_C of 70 nm and 30 nm are plotted in Fig. 3.15 (a) and

(b), respectively. It is evident from both Fig. 3.15 (a) and (b) that when fringe capacitances are ignored, the analytical model fails to capture the enhanced depletion effect caused by the fringing electric field, leading to a higher surface potential than that observed in the simulation results. Besides this, when V_{DS} increases from 0 V to 1 V with an air spacer, the surface potential rises upward more significantly for the shorter L_C of 30 nm (Fig. 3.15 (b)) compared to the 70 nm. This suggests a greater reduction in V_T for the shorter channel, indicating that the drain bias has a more pronounced effect on shorter L_C with air spacer. Additionally, with a high-k GSS (HfO_2), no significant shift in the minimum surface potential is observed for a given L_C. Moreover, as the L_C is scaled from 70 nm to 30 nm with an HfO_2 spacer, the influence of drain bias on the minimum surface potential is reduced.



(a) (b)

Fig. 3.15 Surface potential ($\phi_S(z)$) profile along device length of GSS-CS-JL-NWFET for different spacer materials and V_{DS} at channel lengths of (a) 70 nm and (b) 30 nm with and without fringe capacitances

Fig. 3.16 (a), (b), and (c) depict the transfer characteristics of the GSS-CS-JL-NWFET for different core thicknesses, spacer materials, and core doping concentrations, respectively. As the t_{core} increases from 0 to 7 nm in Fig. 3.16 (a), with a specific high-k GSS, I_{OFF} decreases drastically by 4 orders of magnitude. This behavior is due to the fact that increasing t_{core} in the oppositely doped core aids in the depletion of carriers in the shell region during the OFF-state. Moreover, a high-permittivity spacer helps in volume depletion beyond the gate region due to an increase in the fringing electric field.

However, increasing t_{core} also decreases I_{ON} at V_{GS} = 1 V, as the shell region, which serves as the conduction area, is reduced. The decrease in I_{ON} is more prominent when t_{core} exceeds more than half of the t_{si}. Fig. 3.16 (b) shows that when considering the fringe capacitances effect in an analytical model, a high-permittivity spacer (Ta_2O_5) reduces I_{OFF} more efficiently than a

low-*k* GSS (Al_2O_3), as a high-permittivity spacer increases gate voltage control over channel electrostatics due to the fringing electric field.

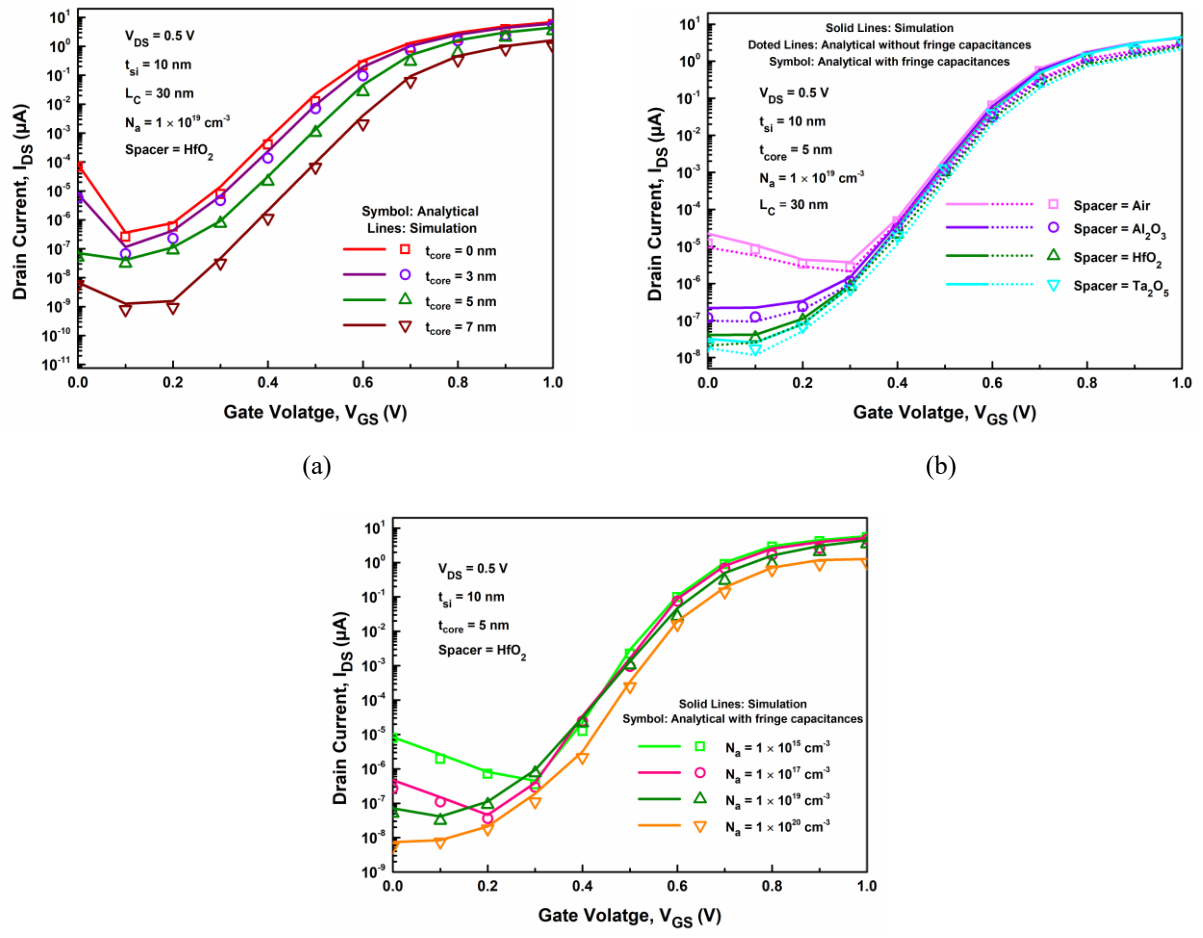


Fig. 3.16 Transfer characteristics of GSS-CS-JL-NWFET for different (a) core thicknesses, (b) spacer materials with and without fringe capacitances, and (c) core doping concentrations

Additionally, no significant decrease in I_{OFF} is observed for Ta_2O_5, therefore, HfO_2 is preferable as spacer material for GSS-CS-JL-NWFET. However, no significant improvement is observed in I_{ON}. Furthermore, the analytical result without fringe capacitances increases the I_{OFF} significantly compared to the simulation result, as the model does not account for the enhanced depletion effect caused by the fringing electric field. Additionally, I_{ON} decreases due to an increase in parasitic resistances in S/D extensions without fringe capacitance consideration in the analytical model. Fig. 3.16 (c) illustrates that as p-type core doping increases from 1×10^{15} cm^{-3} to 1×10^{20} cm^{-3}, I_{OFF} decreases by 3 orders of magnitude due to the effective depletion of carriers in the shell region.

However, a highly doped core with a concentration of 1×10^{20} cm^{-3} degrades the I_{ON} significantly due to an increase in series resistance. The core doping of GSS-CS-JL-NWFET

should be kept equally as the shell region because, beyond 1×10^{19} cm^{-3}, I_{ON} starts to degrade significantly. Therefore, the trade-off between I_{OFF} and I_{ON} should be carefully considered when designing the GSS-CS-JL-NWFET. Although increasing t_{core} decreases I_{OFF}, further increasing t_{core} beyond an optimal value does not provide additional performance benefits. This is because a larger core reduces the effective conduction area in the shell, limiting carrier transport. For t_{si} of 10 nm, a t_{core} of 5 nm is preferable, as increasing t_{core} beyond this point leads to a significant degradation in I_{ON}.

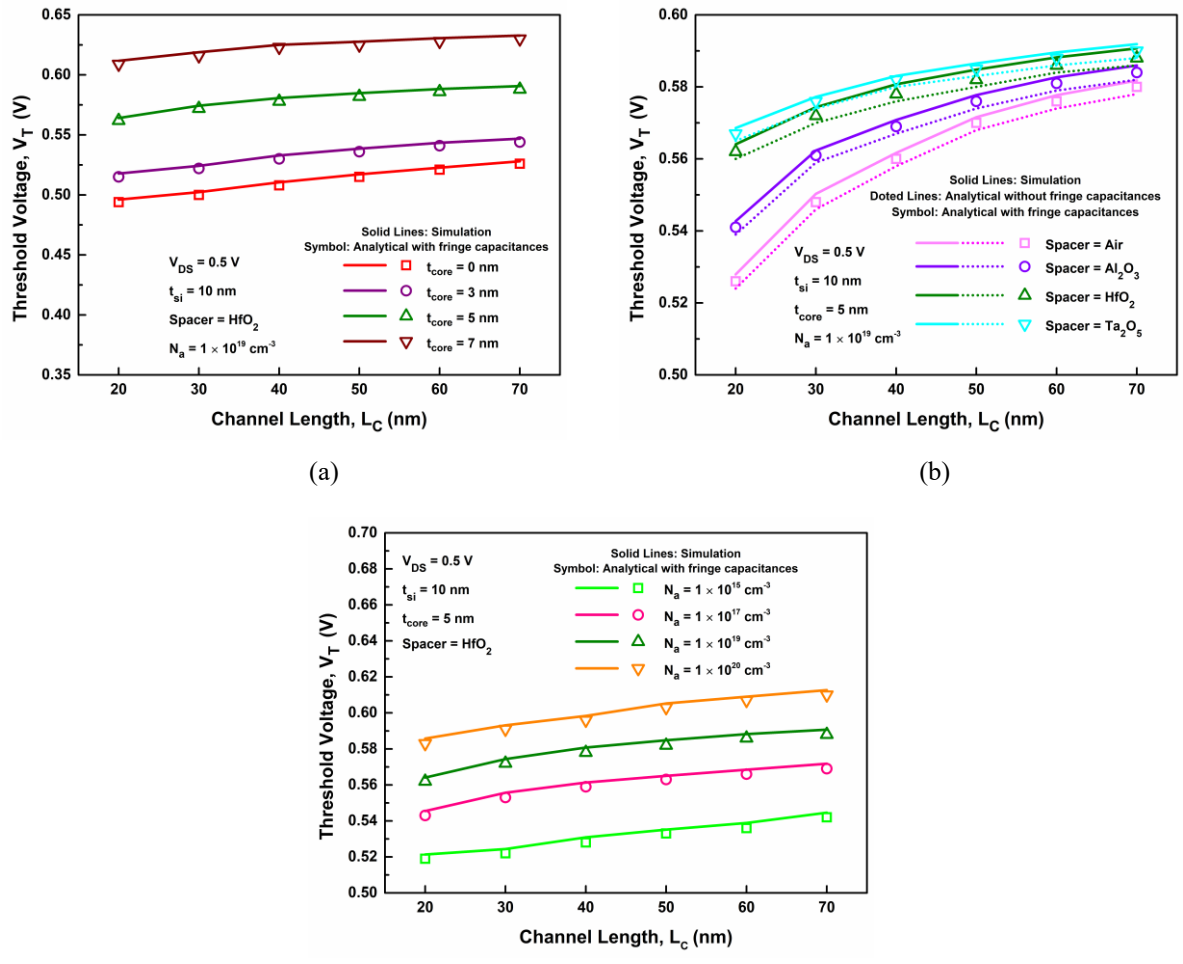


Fig. 3.17 Effect of L_C scaling on V_T of GSS-CS-JL-NWFET for different (a) core thicknesses, (b) spacer materials with and without fringe capacitances, and (c) core doping concentrations

To analyse the effect of L_C scaling on the characteristics of GSS-CS-JL-NWFET, L_C is varied from 70 nm to 20 nm. The dependence of V_T on L_C scaling is illustrated in Fig. 3.17 (a), (b), and (c) for different core thicknesses, spacer materials, and core doping concentrations, respectively. Fig. 3.17 (a) shows that at a given L_C, a wider t_{core} (7 nm) requires a higher V_T compared to a narrower t_{core} (3 nm) or no core. A thicker t_{core} depletes the channel more effectively during the OFF-state, which increases the required V_{GS} to turn the device ON,

leading to a higher V_{GS}. In Fig. 3.17 (b), considering fringe capacitance in the analytical model, higher permittivity spacer materials require a higher V_T, as they help to deplete S/D extension during the OFF-state.

However, the improvement is less pronounced when using Ta_2O_5 compared to HfO_2 as the spacer material. On the other hand, without fringe capacitances, the analytical results decrease than the simulation as the absence of fringe capacitance weakens the coupling between the gate and the shell region, reducing the V_T. Fig. 3.17 (c) depicts that highly doped t_{core} (1×10^{20} cm^{-3}) depleted the shell region more effectively than lightly doped t_{core} (1×10^{15} cm^{-3}), resulting in increased V_T to initiate carrier conduction. In Fig. 3.17 (a), (b), and (c), V_T decreases as L_C is scaled down due to increased SCEs.

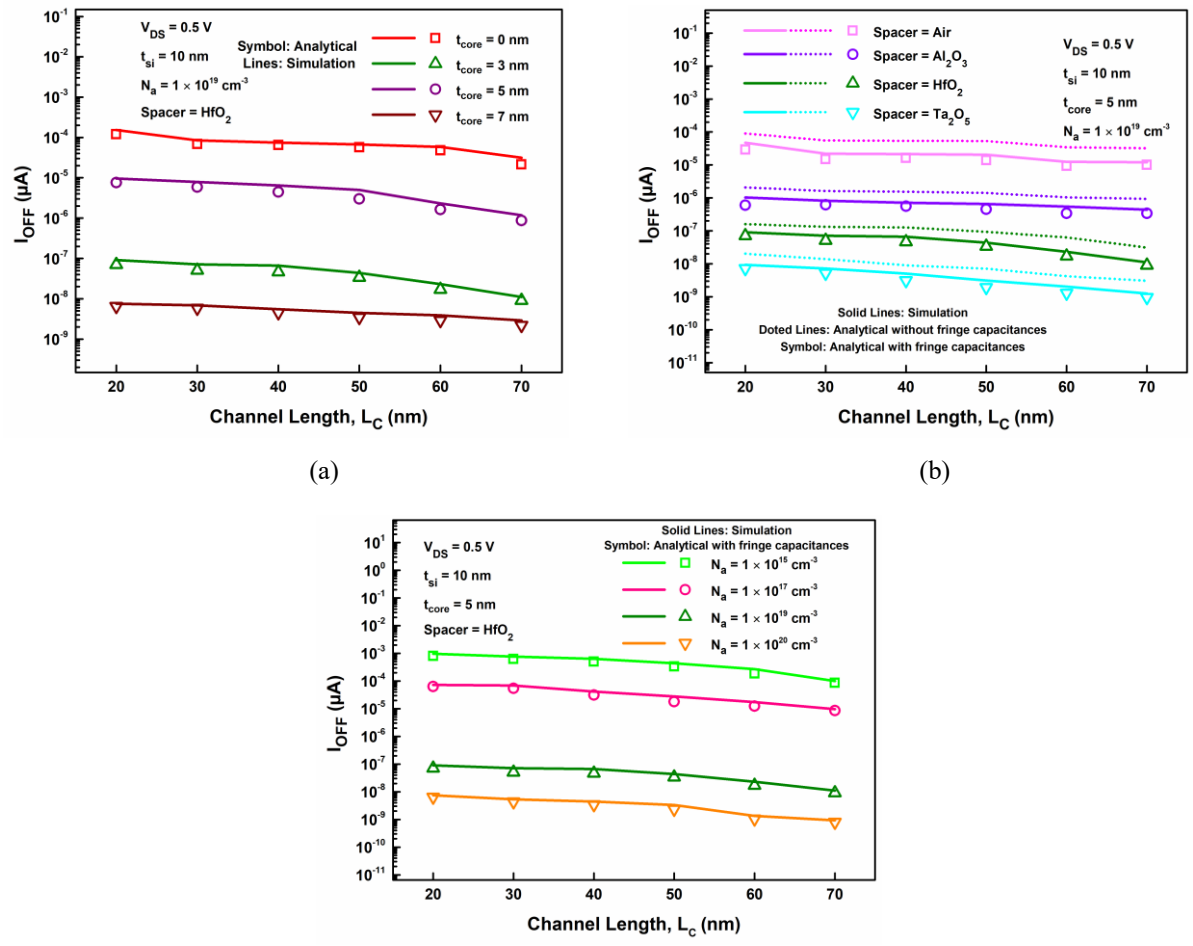
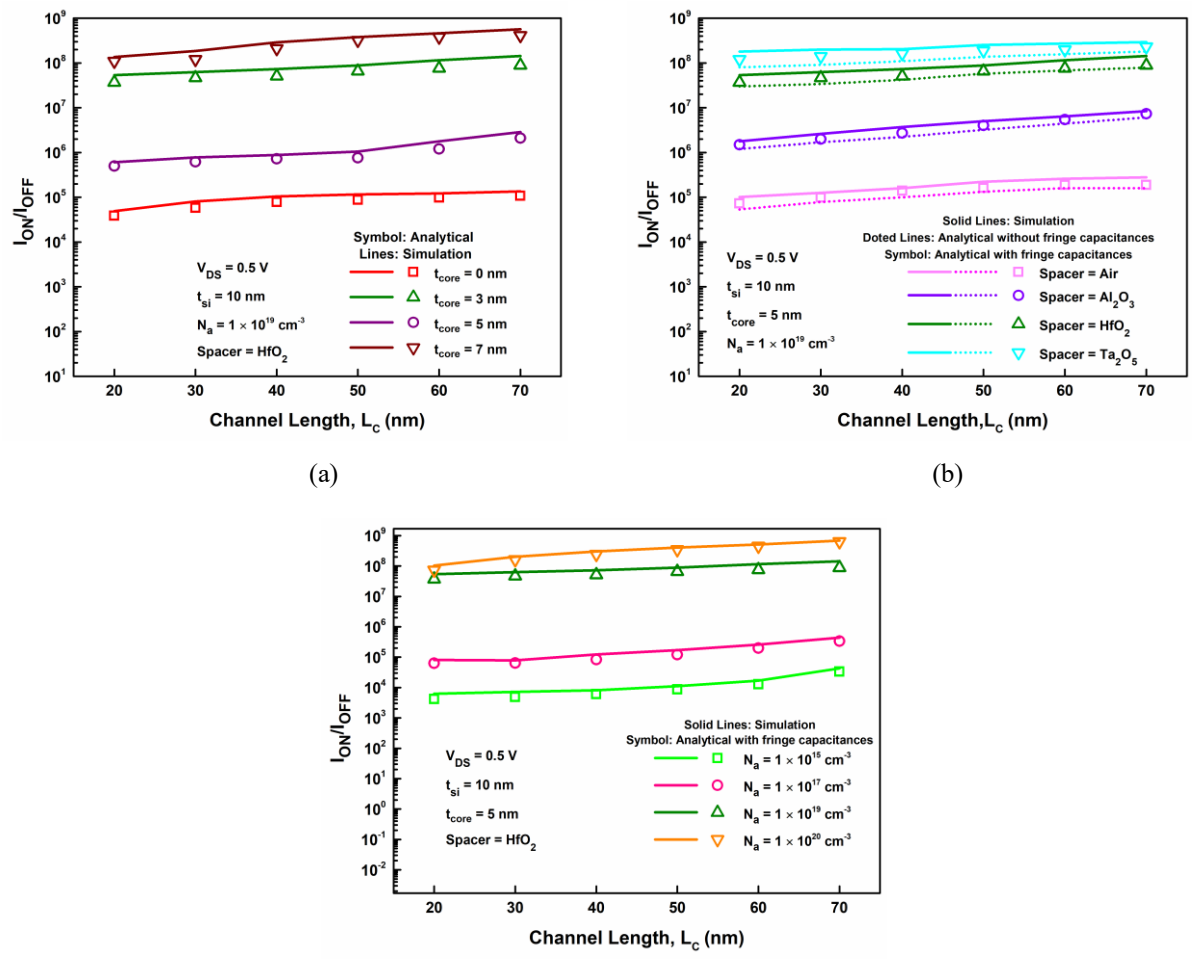


Fig. 3.18 Effect of L_C scaling on I_{OFF} of GSS-CS-JL-NWFET for different (a) core thicknesses, (b) spacer materials with and without fringe capacitances, and (c) core doping concentrations

Figures 3.18 (a), (b), and (c) portray the effect of scaling L_C on I_{OFF} for various core thicknesses, spacer materials, and core doping concentrations, respectively. In Fig. 3.18 (a), increasing t_{core} at fixed L_C reduces I_{OFF}, as discussed previously in Fig. 3.16 (a). Additionally, Fig. 3.18 (b)

shows that by including the fringe capacitances effect in the analytical model, the spacer material with higher permittivity enhances depletion beyond the channel region and reduces I_{OFF} by suppressing unwanted carrier conduction in the OFF-state which was already discussed in Fig. 3.16 (b). Additionally, without the inclusion of fringe capacitance, I_{OFF} increases due to the weaker electrostatic control. This leads to reduced depletion in the S/D extensions, allowing more I_{OFF}. Fig. 3.18 (c) illustrates that a highly doped core (1×10^{20} cm^{-3}) results in reduced I_{OFF} compared to a lightly doped core (1×10^{15} cm^{-3}) due to enhanced carrier depletion. The stronger depletion reduces carrier conduction in the OFF-state, thereby mitigating I_{OFF}. Furthermore, I_{OFF} increases as L_C decreases in Fig. 3.18 (a), (b), and (c) not by orders of magnitude but by noticeable increments due to the enhanced SCEs.



(a) (b)

(c)

Fig. 3.19 Effect of L_C scaling on I_{ON}/I_{OFF} ratio of GSS-CS-JL-NWFET for different (a) core thicknesses, (b) spacer materials with and without fringe capacitances, and (c) core doping concentrations

The influence of L_C scaling on the I_{ON}/I_{OFF} ratio for varying core thicknesses, spacer materials, and core doping concentrations is presented in Fig. 3.19 (a), (b), and (c), respectively. As shown in Fig. 3.19 (a), a thicker t_{core} (7 nm) achieves the highest I_{ON}/I_{OFF} ratio, primarily due to a

significant reduction in I_{OFF} compared to a thinner t_{core} (3 nm) or no core. In Fig. 3.19 (b), the use of a high-permittivity spacer (Ta_2O_5) results in a higher I_{ON}/I_{OFF} ratio compared to an air spacer when the inclusion of fringe capacitance is considered in the analytical model due to reduced I_{OFF}. However, the improvement in the I_{ON}/I_{OFF} ratio when switching from HfO_2 to Ta_2O_5 is relatively less.

Furthermore, without fringe capacitances, I_{ON}/I_{OFF} ratio decreases than the simulation results due to an increase in I_{OFF}, as discussed in Fig. 3.18 (b). Fig. 3.19 (c) demonstrates that the I_{ON}/I_{OFF} ratio increases with increasing core doping due to decreasing I_{OFF} as explained in Fig. 3.18 (c). However, the enhancement in the I_{ON}/I_{OFF} ratio becomes less significant beyond a core doping concentration of 1×10^{19} cm^{-3}, making it an optimal doping level for balancing leakage suppression and ON-state performance. In Fig. 3.19 (a), (b), and (c), the I_{ON}/I_{OFF} ratio decreases with L_C scaling, not by orders of magnitude but by noticeable increments, driven by an increase in I_{OFF}. Additionally, no significant enhancement in I_{ON} is observed with L_C scaling.

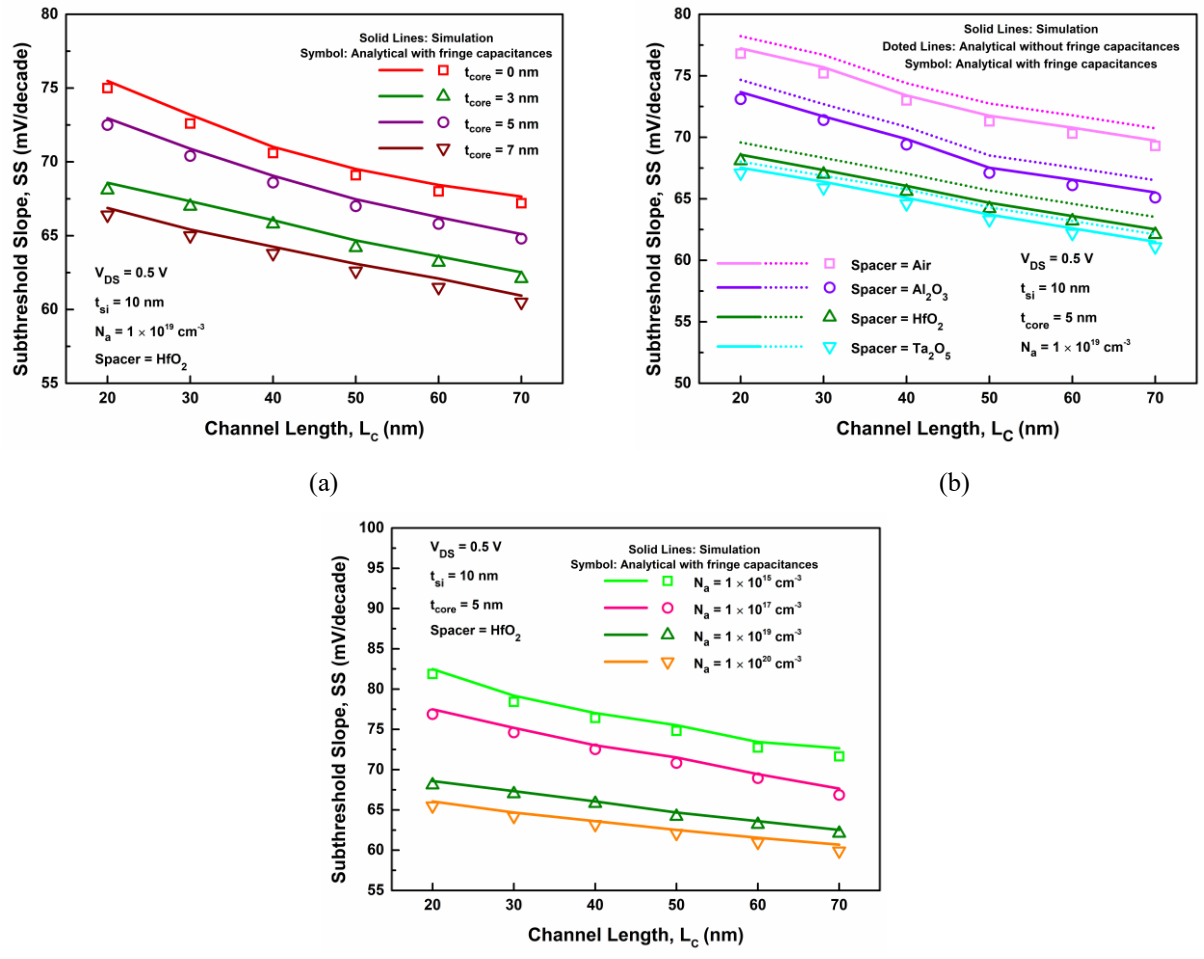


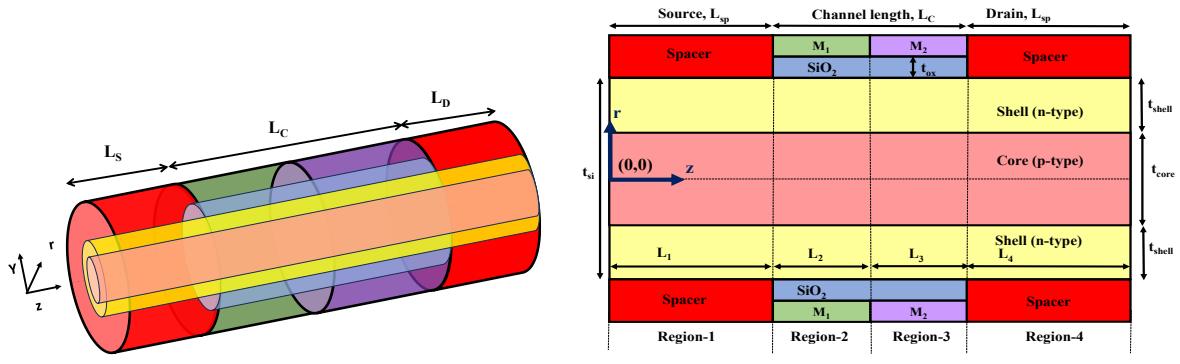
Fig. 3.20 Effect of L_C scaling on SS of GSS-CS-JL-NWFET for different (a) core thicknesses, (b) spacer materials with and without fringe capacitances, and (c) core doping concentrations

Figures 3.20 (a), (b) and (c) compare the SS of GSS-CS-JL-NWFET for different core thicknesses, spacer materials, and core doping concentrations, respectively. A steep SS is desirable to efficiently switch the transistor current by minimizing subthreshold leakage, which helps reduce CMOS standby power dissipation. As shown in Fig. 3.20 (a), the lowest SS is achieved with a thicker t_{core} (7 nm) due to a significant reduction in I_{OFF}, as seen in Fig. 3.18 (a). Fig. 3.20 (b) indicates that considering the effect of fringe capacitance in the analytical model, a high-permittivity spacer material improves SS by depleting the S/D extension, leading to a decrease in I_{OFF}, as discussed in Fig. 3.18 (b).

This mitigated I_{OFF} steepens the slope of the transfer characteristics, bringing SS closer to its ideal value. Moreover, without fringe capacitances, SS increases than its simulation results due to enhanced I_{OFF} as shown in Fig. 3.18 (b). Fig. 3.20 (c) illustrates that at fixed L_C, increasing core doping concentrations leads to an improved SS due to a greater extent of depletion in the shell region that mitigates I_{OFF}. The stronger depletion effect reduces the potential barrier-lowering effect caused by residual carriers, ensuring a sharper turn-on characteristic and better switching efficiency. However, SS increases with the scaling down of L_C in Fig. 3.20 (a), (b), and (c), owing to the rise in I_{OFF}, which reduces the steepness of the transfer characteristics slope.

3.4 ANALYTICAL MODELING OF THE PROPOSED I-JL-NWFET

The 3-D view of the proposed I-JL-NWFET is shown in Fig. 3.21 (a). In 2-D view of I-JL-NWFET as illustrated in Fig. 3.21 (b), the proposed device is divided into four regions, namely, source extension (region–1), channel region with M_1 gate (region–2), channel region with M_2 gate (region–3), and drain extension (region–4) for analytical modeling. Herein, the source extension length and drain extension length are denoted as L_1 and L_4, respectively. Additionally, L_{sp} ($L_{sp} = L_1 = L_4$) signifies the length of S/D extension.



(a) (b)

Fig. 3.21 (a) 3-D view and (b) 2-D schematic of I-JL-NWFET

3.4.1 Surface Potential Modeling

The surface potential distribution of I-JL-NWFET can be derived by solving Poisson's equation. In semiconductor physics, Poisson's equation is applied to model the semiconductor device by solving for the electrostatic potential and electric field distributions within the device. The symmetry of the cylindrical structure of I-JL-NWFET ensures that the potential distribution has no variation with respect to the angular direction in the radial plane. As a result, a 2-D Poisson's equation is sufficient to model the device using appropriate boundary conditions. The potential distributions in the core and shell region are derived from 2-D Poisson's equation in cylindrical coordinates and are given as follows:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\phi_{core,n}(r,z)\right)+\frac{\partial^2\phi_{core,n}(r,z)}{\partial z^2}=\frac{qN_a}{\varepsilon_{si}}\ for\ 0\le r\le\frac{t_{core}}{2},n=1,2,3,4 \tag{3.126}$$

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\phi_{shell,n}(r,z)\right)+\frac{\partial^2\phi_{shell,n}(r,z)}{\partial z^2}=\frac{-qN_d}{\varepsilon_{si}}\ for\ \frac{t_{core}}{2}\le r\le\frac{t_{si}}{2},n=1,2,3,4 \tag{3.127}$$

where, $\phi_{core,n}(r,z)$ and $\phi_{shell,n}(r,z)$ are the potential distribution of the core and shell region, respectively, for region n as shown in Fig. 3.21. The permittivity of silicon, electron charge, acceptor concentration in the core region of the channel, and donor concentration in the shell region of the channel, are denoted as ε_{si}, q, N_a, and N_d, respectively. Using parabolic potential approximation [47], the potential distribution along the radial direction in both the core and shell regions is described as follows:

$$\phi_{core,n}(r,z)=G_{0n}(z)+G_{1n}(z)r+G_{2n}(z)r^2 \tag{3.128}$$

$$\phi_{shell,n}(r,z)=S_{0n}(z)+S_{1n}(z)\left(r-\frac{t_{core}}{2}\right)+S_{2n}(z)\left(r-\frac{t_{core}}{2}\right)^2 \tag{3.129}$$

where the arbitrary coefficients $G_{0n}(z)$, $G_{1n}(z)$, $G_{2n}(z)$, $S_{0n}(z)$, $S_{1n}(z)$, and $S_{2n}(z)$ can be determined from the following boundary conditions (xv)-(xviii):

(xv) Surface potential ($\phi_{Sn}(z)$) in shell region and central potential ($\phi_{Cn}(z)$) in the core region of channel is expressed as

$$\phi_{core,n}(0,z)=\phi_{Cn}(z) \tag{3.130}$$

$$\phi_{shell,n}\left(\frac{t_{si}}{2},z\right)=\phi_{Sn}(z) \tag{3.131}$$

(xvi) The electric field at the center of the core region in the channel is zero.

$$\left.\frac{\partial \phi_{core,n}(r,z)}{\partial r}\right|_{r=0} = 0 \tag{3.132}$$

(xvii) Potentials and electric fields along the radial direction at the interface between the core and shell regions must be continuous.

$$\phi_{core,n}\left(\frac{t_{core,n}}{2}, z\right) = \phi_{shell,n}\left(\frac{t_{core,n}}{2}, z\right) \tag{3.133}$$

$$\left.\frac{\partial \phi_{core,n}(r,z)}{\partial r}\right|_{r=\frac{t_{core}}{2}} = \left.\frac{\partial \phi_{shell,n}(r,z)}{\partial r}\right|_{r=\frac{t_{core}}{2}} \tag{3.134}$$

(xviii) The electric field at the silicon-oxide in the shell region interface is continuous.

$$\left.\frac{\partial \phi_{shell,n}(r,z)}{\partial r}\right|_{r=\frac{t_{si}}{2}} = \frac{C_n\left(V_{GS} - V_{fbn} - \phi_{Sn}(z)\right)}{\varepsilon_{si}} \tag{3.135}$$

here, C_n and V_{fbn} are capacitance per unit area and flat band voltage for the nth region, respectively. In the DMG structure, the flat band voltage in each gate region is directly influenced by the work function of the respective gate material and the work function of silicon (ϕ_{si}). Since the DMG design utilizes two distinct gate materials, M_1 and M_2, the flat band voltages depend on the work functions of M_1 (ϕ_{M1}) and M_2 (ϕ_{M1}).

$$C_2 = C_3 = C_{ox} = \frac{\varepsilon_{ox}}{\frac{t_{si}}{2}\ln\left(1 + \frac{2t_{ox}}{t_{si}}\right)} \tag{3.136}$$

$$C_1 = C_4 = C_{sp} = \frac{\left(C_{if} + C_{of}\right)}{\pi t_{si}} \tag{3.137}$$

$$V_{fb1} = V_{fb2} = \phi_{M1} - \phi_{si} \tag{3.138}$$

$$V_{fb3} = V_{fb4} = \phi_{M2} - \phi_{si} \tag{3.139}$$

where, the notations C_{ox}, ε_{ox}, C_{sp}, C_{if}, C_{of}, and ϕ_{si} represent gate oxide capacitance per unit area, gate oxide permittivity, spacer capacitance per unit area, inner fringe capacitance per unit width, outer fringe capacitance per unit width, and workfunction of silicon, respectively. C_{if} and C_{of} are expressed as [124]

$$C_{if} = \frac{6\varepsilon_{ox}}{\pi}\ln\left(\frac{t_{ox} + t_{si}sin\theta}{t_{ox}cos\theta + f_{if}L_{sp}sin\theta}\right) \tag{3.140}$$

$$C_{of} = \frac{6\varepsilon_{sp}}{\pi} ln\left(\frac{t_g + t_{ox}}{L_{sp}}\right) \tag{3.141}$$

here, f_{if}, L_{sp}, ε_{sp}, t_g, and θ indicate tuning parameter with the value of unity, spacer length, spacer permittivity, gate electrode thickness and plate angle with the value of $\pi/6$, respectively. Fig. 3.22 portrays C_{if} and C_{of} in I-JL-NWFET.

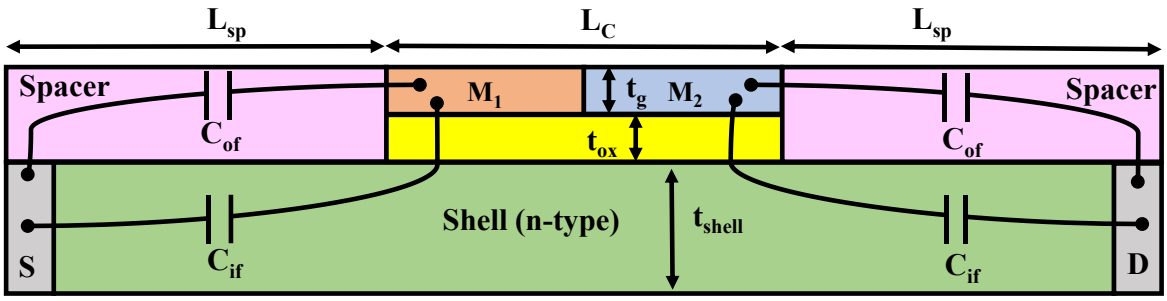


Fig. 3.22 Illustration of inner fringe capacitance (C_{if}) and outer fringe capacitance (C_{of}) in I-JL-NWFET

Using boundary conditions (xvi)–(xix), arbitrary coefficients in Eqns. 3.128 and 3.129 are obtained as

$$G_{0n}(z)=\phi_{Cn}(z) \tag{3.142}$$

$$G_{1n}(z)=0 \tag{3.143}$$

$$G_{2n}(z)=\frac{\left(4\varepsilon_{si}+C_n\left(t_{si}-t_{core}\right)\right)\phi_{Sn}(z)-4\varepsilon_{si}\phi_{Cn}(z)-C_n\left(t_{si}-t_{core}\right)\left(V_{GS}-V_{fbn}\right)}{\varepsilon_{si}t_{si}t_{core}} \tag{3.144}$$

$$S_{0n}(z)=\frac{\left(4\varepsilon_{si}t_{core}+C_nt_{core}\left(t_{si}-t_{core}\right)\right)\phi_{Sn}(z)+4\varepsilon_{si}\left(t_{si}-t_{core}\right)\phi_{Cn}(z)-C_nt_{core}\left(t_{si}-t_{core}\right)\left(V_{GS}-V_{fbn}\right)}{4\varepsilon_{si}t_{si}} \tag{3.145}$$

$$S_{1n}(z)=\frac{\left(4\varepsilon_{si}+C_n\left(t_{si}-t_{core}\right)\right)\phi_{Sn}(z)-4\varepsilon_{si}\phi_{Cn}(z)-C_n\left(t_{si}-t_{core}\right)\left(V_{GS}-V_{fbn}\right)}{\varepsilon_{si}t_{si}} \tag{3.146}$$

$$S_{2n}(z)=\frac{\left(-4\varepsilon_{si}-C_n\left(2t_{si}-t_{core}\right)\right)\phi_{Sn}(z)+4\varepsilon_{si}\phi_{Cn}(z)+C_n\left(2t_{si}-t_{core}\right)\left(V_{GS}-V_{fbn}\right)}{\varepsilon_{si}t_{si}\left(t_{si}-t_{core}\right)} \tag{3.147}$$

To obtain the relationship between $\phi_{Sn}(z)$ and $\phi_{Cn}(z)$, Eqns. 3.126 and 3.127 are solved simultaneously using Eqn. 3.128 and 3.129 at $r = t_{core}$ and is given as

$$\phi_{Cn}(z)=\frac{\left(8\varepsilon_{si}+2C_nt_{si}\right)\phi_{Sn}(z)-2C_nt_{si}\left(V_{GS}-V_{fbn}\right)-q\left(N_a+N_d\right)t_{core}\left(t_{si}-t_{core}\right)}{8\varepsilon_{si}} \tag{3.148}$$

By solving Eqn. 3.127 using Eqns. 3.129 and 3.148 at $r = t_{si}/2$, the differential equation for $\phi_{Sn}(z)$ can be expressed as

$$\frac{\partial^2\phi_{Sn}(z)}{\partial z^2}-\frac{\left(\phi_{Sn}(z)-A_n\right)}{\lambda_n^{\,2}}=0 \tag{3.149}$$

$$A_n=V_{GS}+\alpha_n \tag{3.150}$$

$$\alpha_n = \frac{qN_d t_{si} - qt_{core}\left(N_a + N_d\right)}{4C_n} - V_{fbn} \tag{3.151}$$

$$\lambda_n{}^2 = \frac{\varepsilon_{si} t_{si}}{4C_n} \tag{3.152}$$

where λ_n signifies the scaling length of DMG-ODCS-JL-NWFET for the nth region and is analogous to the scaling length of Double Gate Junctionless FET [121]. It characterizes the potential distribution within the silicon thickness and is determined by the device geometry and boundary conditions. Derived from the electrostatic potential distribution, the scaling length is influenced by the capacitance per unit area and the t_{si}. A smaller λ, achieved by reducing the t_{si}, enhances the gate's electrostatic control over the channel, thereby suppressing SCEs and improving overall device performance. The generic solution for the second-order differential Eqn. 3.149 for regions 1–4 is expressed as

$$\phi_{S1}\left(z\right) = B_1 e^{z/\lambda_1} + D_1 e^{-z/\lambda_1} + A_1 \tag{3.153}$$

$$\phi_{S2}\left(z\right) = B_2 e^{(z-L_1)/\lambda_2} + D_2 e^{-(z-L_1)/\lambda_2} + A_2 \tag{3.154}$$

$$\phi_{S3}\left(z\right) = B_3 e^{(z-L_1-L_2)/\lambda_3} + D_3 e^{-(z-L_1-L_2)/\lambda_3} + A_3 \tag{3.155}$$

$$\phi_{S4}\left(z\right) = B_4 e^{(z-L_1-L_C)/\lambda_4} + D_4 e^{-(z-L_1-L_C)/\lambda_4} + A_4 \tag{3.156}$$

where arbitrary constants, B_n and D_n can be determined using the following boundary conditions (xix)-(xxi)

(xix) The surface potential at the source side

$$\phi_{S1}\left(z=0\right) = V_{bi} \tag{3.157}$$

$$V_{bi} = \frac{KT}{q}\ln\left(1+\frac{N_d}{n_i}\right) \tag{3.158}$$

where V_{bi} is the built-in potential. K, T, and n_i represent the Boltzmann constant, thermal temperature, and intrinsic concentration, respectively.

(xx) The surface potential at the drain side

$$\phi_{S4}\left(z = L_1 + L_C + L_4\right) = V_{bi} + V_{DS} \tag{3.159}$$

(xxi) At the interface of regions 1–2, regions 2–3, and regions 3–4, the surface potential and electric field exhibit continuity.

$$\phi_{S1}\left(z = L_1\right) = \phi_{S2}\left(z = L_1\right) \tag{3.160}$$

$$\phi_{S2}\left(z = L_1 + L_2\right) = \phi_{S3}\left(z = L_1 + L_2\right) \tag{3.161}$$

$$\phi_{S3}\left(z = L_1 + L_C\right) = \phi_{S4}\left(z = L_1 + L_C\right) \tag{3.162}$$

$$\left.\frac{\partial \phi_{S1}(z)}{\partial r}\right|_{z=L_1} = \left.\frac{\partial \phi_{S2}(z)}{\partial r}\right|_{z=L_1} \tag{3.163}$$

$$\left.\frac{\partial \phi_{S2}(z)}{\partial r}\right|_{z=L_1+L_2} = \left.\frac{\partial \phi_{S3}(z)}{\partial r}\right|_{z=L_1+L_2} \tag{3.164}$$

$$\left.\frac{\partial \phi_{S3}(z)}{\partial r}\right|_{z=L_1+L_C} = \left.\frac{\partial \phi_{S4}(z)}{\partial r}\right|_{z=L_1+L_C} \tag{3.165}$$

B_n and D_n are obtained by solving abovementioned boundary conditions and expressed as

$$B_1 = \frac{e^{-L_1/\lambda_1}}{2}\left(B_2\left(1+\frac{\lambda_1}{\lambda_2}\right)+D_2\left(1-\frac{\lambda_1}{\lambda_2}\right)+\left(A_2-A_1\right)\right) \tag{3.166}$$

$$D_1 = \frac{e^{L_1/\lambda_1}}{2}\left(B_2\left(1-\frac{\lambda_1}{\lambda_2}\right)+D_2\left(1+\frac{\lambda_1}{\lambda_2}\right)+\left(A_2-A_1\right)\right) \tag{3.167}$$

$$B_3 = B_2\left(1+\frac{\lambda_3}{\lambda_2}\right)\frac{e^{L_2/\lambda_2}}{2}+D_2\left(1-\frac{\lambda_3}{\lambda_2}\right)\frac{e^{-L_2/\lambda_2}}{2}+\frac{\left(A_2-A_3\right)}{2} \tag{3.168}$$

$$D_3 = B_2\left(1-\frac{\lambda_3}{\lambda_2}\right)\frac{e^{L_2/\lambda_2}}{2}+D_2\left(1+\frac{\lambda_3}{\lambda_2}\right)\frac{e^{-L_2/\lambda_2}}{2}+\frac{\left(A_2-A_3\right)}{2} \tag{3.169}$$

$$B_4 = B_3\left(1+\frac{\lambda_4}{\lambda_3}\right)\frac{e^{L_3/\lambda_3}}{2}+D_3\left(1-\frac{\lambda_4}{\lambda_3}\right)\frac{e^{-L_3/\lambda_3}}{2}+\frac{\left(A_3-A_4\right)}{2} \tag{3.170}$$

$$D_4 = B_3\left(1-\frac{\lambda_4}{\lambda_3}\right)\frac{e^{L_3/\lambda_3}}{2}+D_3\left(1+\frac{\lambda_4}{\lambda_3}\right)\frac{e^{-L_3/\lambda_3}}{2}+\frac{\left(A_3-A_4\right)}{2} \tag{3.171}$$

$$B_2 = \frac{(W_1-V_{GS})\gamma_1-(W_2-V_{GS})\gamma_3}{\gamma_1\gamma_4-\gamma_3\gamma_2} \tag{3.172}$$

$$D_2 = \frac{(W_2-V_{GS})\gamma_4-(W_1-V_{GS})\gamma_2}{\gamma_1\gamma_4-\gamma_3\gamma_2} \tag{3.173}$$

$$W_1 = V_{bi}+V_{DS}+\alpha_4\left(\cosh\left(\frac{L_4}{\lambda_4}\right)-1\right)-\alpha_3\cosh\left(\frac{L_4}{\lambda_4}\right)+\left(\alpha_3-\alpha_2\right)\delta \tag{3.174}$$

$$W_2 = V_{bi}+\alpha_1\left(\cosh\left(\frac{L_1}{\lambda_1}\right)-1\right)-\alpha_2\cosh\left(\frac{L_1}{\lambda_1}\right) \tag{3.175}$$

$$\delta = \cosh\left(\frac{L_3}{\lambda_3}\right)\cosh\left(\frac{L_4}{\lambda_4}\right)+\left(\frac{\lambda_4}{\lambda_3}\right)\left(\sinh\left(\frac{L_3}{\lambda_3}\right)\sinh\left(\frac{L_4}{\lambda_4}\right)\right) \tag{3.176}$$

$$\gamma_1 = \cosh\left(\frac{L_1}{\lambda_1}\right)+\left(\frac{\lambda_1}{\lambda_2}\right)\sinh\left(\frac{L_1}{\lambda_1}\right) \tag{3.177}$$

$$\gamma_2 = \cosh\left(\frac{L_1}{\lambda_1}\right)-\left(\frac{\lambda_1}{\lambda_2}\right)\sinh\left(\frac{L_1}{\lambda_1}\right) \tag{3.178}$$

$$\gamma_3 = \left(1 - \frac{\lambda_3}{\lambda_2}\right)\delta e^{-L_1/\lambda_1} \tag{3.179}$$

$$\gamma_4 = \left(1 + \frac{\lambda_3}{\lambda_2}\right)\delta e^{L_1/\lambda_1} \tag{3.180}$$

3.4.2 Threshold Voltage, DIBL, Drain Current, and Subthreshold Slope Modeling

The V_T of I-JL-NWFET can be obtained by setting the minimum surface potential ($\phi_{S2,min}(z)$) to zero [121]. Moreover, V_T is controlled by M_1 having a larger work function [121]. The $\phi_{S2,min}(z)$ for region 2 is expressed as follows:

$$\phi_{S2,min}(z) = 2\sqrt{B_2 D_2} + A_2 \tag{3.181}$$

By equating $\phi_{S2,min}(z)$ to zero and solving for V_{GS}, the V_T is expressed as:

$$V_T = \frac{-F_1 + \sqrt{F_1^2 - F_2 F_3}}{F_2} \tag{3.182}$$

where

$$F_1 = \frac{2(\gamma_3 - \gamma_1)(W_2\gamma_4 - W_1\gamma_2) + 2(\gamma_2 - \gamma_4)(W_1\gamma_1 - W_2\gamma_3)}{(\gamma_1\gamma_4 - \gamma_3\gamma_2)^2} - \alpha_2 \tag{3.183}$$

$$F_2 = \frac{4(\gamma_3 - \gamma_1)(W_1\gamma_1 - W_2\gamma_3)}{(\gamma_1\gamma_4 - \gamma_3\gamma_2)^2} - 1 \tag{3.184}$$

$$F_3 = \frac{4(W_1\gamma_1 - W_2\gamma_3)(W_2\gamma_4 - W_1\gamma_2)}{(\gamma_1\gamma_4 - \gamma_3\gamma_2)^2} - {\alpha_2}^2 \tag{3.185}$$

Moreover, DIBL denotes the impact of V_{DS} on the V_T and is expressed as [12]

$$DIBL = \frac{V_T(V_{DS} = 0.05V) - V_T(V_{DS} = 1V)}{(V_{DS} = 1V) - (V_{DS} = 0.05V)} \tag{3.186}$$

A cumulative I_{DS} for region n (1–4) comprises subthreshold drain current (I_{sub}) for $0 \le V_{GS} \le V_T$, I_{DS} in linear region (I_{lin}) within $V_T \le V_{GS} \le V_{DS,sat}$, and I_{DS} in saturation region (I_{sat}), for $V_{DS,sat} \le V_{GS} \le V_{DD}$. The expression of I_{sub} [122], I_{lin} [125], and I_{sat} [126] are given as

$$I_{sub} = \frac{\pi t_{si} KT\left(1 - e^{-qV_{DS}/KT}\right)}{N(z)} \tag{3.187}$$

$$N(z) = \int_0^{L_1} \frac{dz}{Q_1(z)} + \int_{L_1}^{L_1+L_2} \frac{dz}{Q_2(z)} + \int_{L_1+L_2}^{L_1+L_C} \frac{dz}{Q_3(z)} + \int_{L_1+L_C}^{L_1+L_C+L_4} \frac{dz}{Q_4(z)} \tag{3.188}$$

$$Q_n(z) = n_i \mu'_p \int_0^{t_{core}/2} e^{\left(\frac{q\phi_{core,n}(r,z)}{KT}\right)} dr + n_i \mu'_e \int_{t_{core}/2}^{t_{si}/2} e^{\left(\frac{q\phi_{shell,n}(r,z)}{KT}\right)} dr \tag{3.189}$$

$$I_{lin} = \sum_{n=1}^{4} \left[\frac{\beta_n \left((V_{GS} - V'_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right)}{L_n \left(1 - \frac{l_d}{L_n} + \frac{V_{DS}}{L_n E_C} \right)} \right] \tag{3.190}$$

$$I_{sat} = \sum_{n=1}^{4} \left[\frac{\beta_n (V_{GS} - V'_T) V_{DS,sat}}{L_n \left(1 - \frac{l_d}{L_n} + \frac{V_{DS,sat}}{L_n E_C} \right)} \right] \tag{3.191}$$

$$\mu'_p = \frac{\mu_{p0}}{1 + \zeta (V_{GS} - V_T)} \tag{3.192}$$

$$\mu'_e = \frac{\mu_{e0}}{1 + \zeta (V_{GS} - V_T)} \tag{3.193}$$

$$\beta_n = \pi (t_{si} - t_{core}) \mu'_e C_n + \pi t_{core} \mu'_p C_n \tag{3.194}$$

$$E_C = \frac{2v_{es}}{\mu'_e}, V_{DS,sat} = \frac{V_{GS} - V_T}{1 + \frac{V_{GS} - V_T}{L_C E_C}} \tag{3.195}$$

$$SS = \frac{\partial V_{GS}}{\partial log_{10}(I_{DS})} \tag{3.196}$$

here, μ'_p, μ'_e, μ_{p0}, μ_{e0}, and ζ represent effective field-dependent hole mobility, effective field-dependent electron mobility, low field hole mobility, and low field electron mobility, respectively [125]. $V'_T = V_T - DIBL$ is the effective threshold voltage [125]. E_C, l_d and $V_{DS,sat}$ are the critical electric field at which electron velocity (v_{es}) saturates, channel length modulation factor, and saturation voltage, respectively [125, 126]. The expression in Eqn 3.196 is used to obtain the SS.

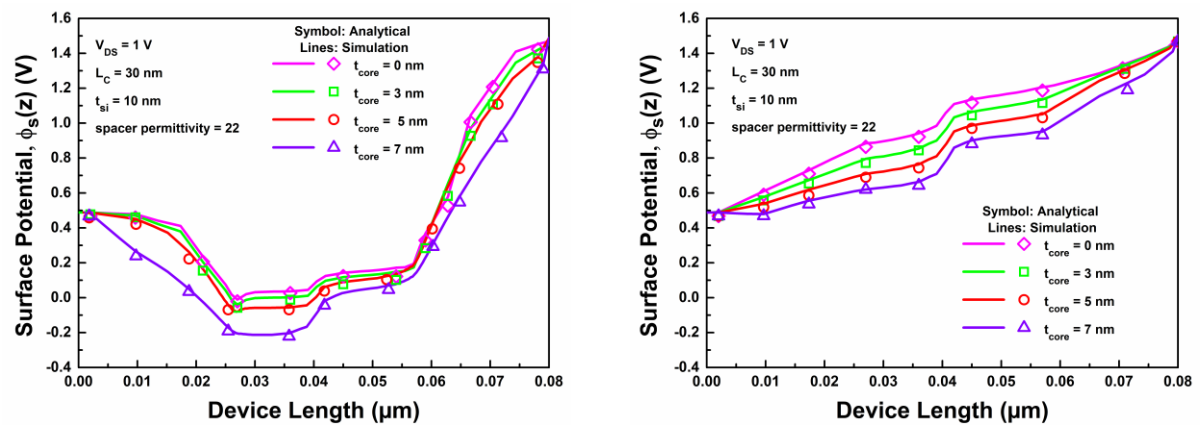
3.4.3 Validation of Analytical Modeling of I-JL-NWFET through Simulation Analysis

Unless otherwise stated, N_a, t_{ox}, L_{sp}, ε_{ox}, ε_{sp}, ϕ_{M1}, ϕ_{M2}, and N_d are kept as 1×10^{19} cm^{-3}, 1 nm, 25 nm, 3.9, 22, 5.1 eV, 4.6 eV, and 1×10^{19} cm^{-3}, respectively. Various spacer materials, such as air, Al_2O_3, HfO_2, and Ta_2O_5, with permittivities of 1, 9.3, 22, and 26, respectively, are also examined to analyse their impact on fringe capacitance. The analysis in this work is conducted at 300 K, and the influence of higher temperatures is not considered. At elevated temperatures, phonon scattering tends to increase, which can reduce carrier mobility and the overall current

drive capability of the I-JL-NWFET. Additionally, leakage current may increase due to enhancement in intrinsic carrier concentration at higher temperatures [118].

The effects of interface charge traps are neglected in the present analysis to maintain focus on these key parameters. Furthermore, the quantization effects are also neglected in the present model as they are insignificant for $t_{si} \geq 7$ nm [120]. The quantization effects become significant for $t_{si} < 7$ nm due to quantum confinement, where the reduction in physical dimensions causes the energy levels of carriers to become discrete rather than continuous. The quantum confinement also changes the effective bandgap, potentially increasing it and affecting the ON-state current and OFF-state current characteristics of the device. While these effects are ignored in the current model to simplify the analysis, their inclusion would require a quantum mechanical treatment of the problem, such as solving the Schrödinger-Poisson equations self-consistently.

Figure 3.23 (a) and (b) illustrate the surface potential ($\phi_S(z)$) along the device length in OFF-state ($V_{GS} = 0$ V) and ON-state ($V_{GS} = 1$ V), respectively, with t_{core} varying from 0 nm to 7 nm while maintaining HfO_2 (permittivity = 22) as spacer material. The data obtained from the proposed model aligns well with the simulation results. The horizontal cut-line to extract the $\phi_S(z)$ is considered at 1 nm below the oxide-semiconductor interface during TCAD simulations. It is important to note that when t_{core} is zero, the device represents a DMG-JL-NWFET with a GSS but without a core-shell structure.



(a) (b)

Fig. 3.23 Surface potential ($\phi_{S(z)}$) profile of I-JL-NWFET along device length for different core thicknesses at (a) $V_{GS} = 0$ V (OFF-state) and (b) $V_{GS} = 1$ V (ON-state)

It is observed from Fig. 3.23 (a) and (b) that the widening of oppositely doped t_{core} causes enhancement in the depletion region within the channel due to the *p-n* junction between equally doped core ($N_a = 1 \times 10^{19}$ cm^{-3}) and shell region ($N_d = 1 \times 10^{19}$ cm^{-3}). This influences the built-

in potential that reduces the $\phi_S(z)$. Furthermore, as t_{core} increases, the shell region undergoes greater depletion, reducing the number of carriers available to block the gate electric field from penetrating the channel, thereby reducing leakage current. This results in a deeper $\phi_S(z)$ in the OFF-state compared to the ON-state. Moreover, due to DMG architecture, step potential is observed in both Fig. 3.23 (a) and (b), which implies enhanced carrier velocity, resulting in improved carrier transport efficiency and an increased drive current [11].

Figure 3.24 (a) and (b) demonstrate $\phi_S(z)$ along the device length in OFF-state and ON-state, respectively, with spacer permittivity varying from 1 to 26 while maintaining t_{core} at 5 nm. It is understood from Fig. 3.24 (a) and (b) that increasing the permittivity of the spacer shifts $\phi_S(z)$ downwards. A higher spacer permittivity reduces the A_1 (region–1) and A_4 (region–4) components, as described in Eqn. 3.150, respectively, which reduces the surface potential (Eqns. 3.153 and 3.156). Fig. 3.24 (a) depicts that during OFF-state, the high-permittivity spacer enhances the fringing electric field, leading to greater depletion beyond the channel and causing the surface potential to decrease as the spacer permittivity increases. In addition, 3.24 (b) shows that during ON-state, the high permittivity spacer diverts part of the electric field into the spacer region, reducing its direct influence on the channel surface.

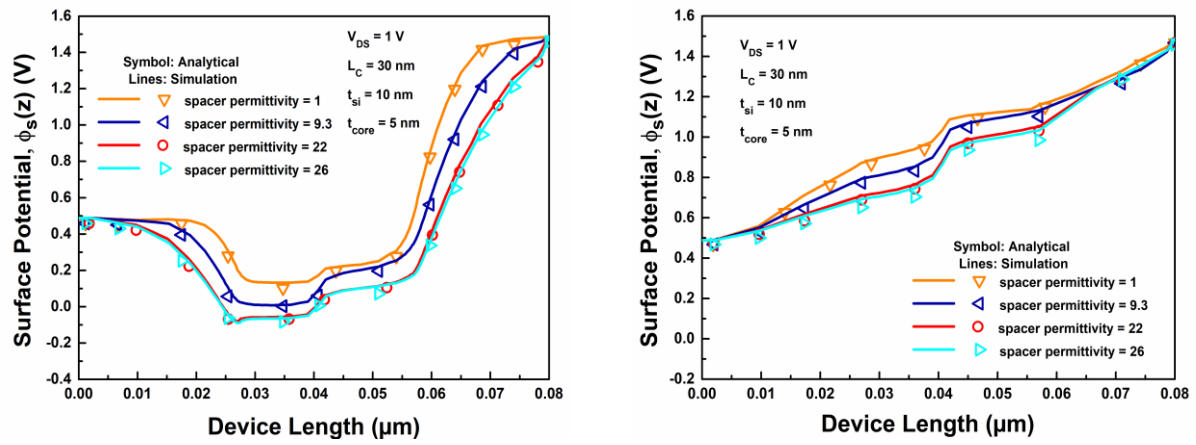


Fig. 3.24 Surface potential ($\phi_{S(z)}$) profile of I-JL-NWFET along device length for different spacer permittivities at (a) V_{GS} = 0 V (OFF-state) and (b) V_{GS} = 1 V (ON-state)

This redistribution lowers the surface potential at the channel. Furthermore, the results also show that increasing the spacer permittivity beyond 22 does not significantly further reduce the surface potential. This may be because the effect of higher permittivity diminishes after a certain point. As the spacer permittivity increases, the electric field strength between two conducting plates decreases, but beyond a threshold, the reduction in surface potential becomes minimal. This is due to the diminishing effectiveness of the dielectric material's ability to

further lower the electric field. Therefore, using a spacer material with a permittivity higher than 22 provides minimal improvement in surface potential reduction during both the OFF-state and ON-state.

The impact of V_{DS} on $\phi_S(z)$ from 0.4 V to 1 V are shown in Fig. 3.25 (a) and (b), respectively, at fixed t_{core} (5 nm) for different V_{GS}. Notably, as V_{GS} increases toward V_T, the shell region transitions from full depletion to partial depletion state. Due to electron accumulation in the shell region, $\phi_S(z)$ shifts upward as V_{GS} increases. DIBL measures how the drain bias affects the V_T (Eqn. 3.186), which is influenced by the minimum $\phi_S(z)$ in the channel (Eqn. 3.181). Notably, at given V_{GS}, the minimum $\phi_S(z)$ remains unaffected under the M_1 region as V_{DS} increases from 0.4 V (Fig. 3.25 (a)) to 1 V (Fig. 3.25 (b)), ensuring better screening from V_{DS}, thereby demonstrating immunity against DIBL.

This clearly indicates that using two different gate materials with distinct work functions in the DMG structure effectively mitigates SCEs. The V_T is influenced by the gate material with a higher work function (M_1), which creates a stronger vertical electric field compared to M_2 (with a lower work function). This stronger vertical field from M_1 reduces the impact of the horizontal electric field. Besides this, the weaker vertical electric field generated by M_2 helps minimize the effects of hot carriers and also prevents it from shifting the $\phi_S(z)$ downward as effectively as M_1.

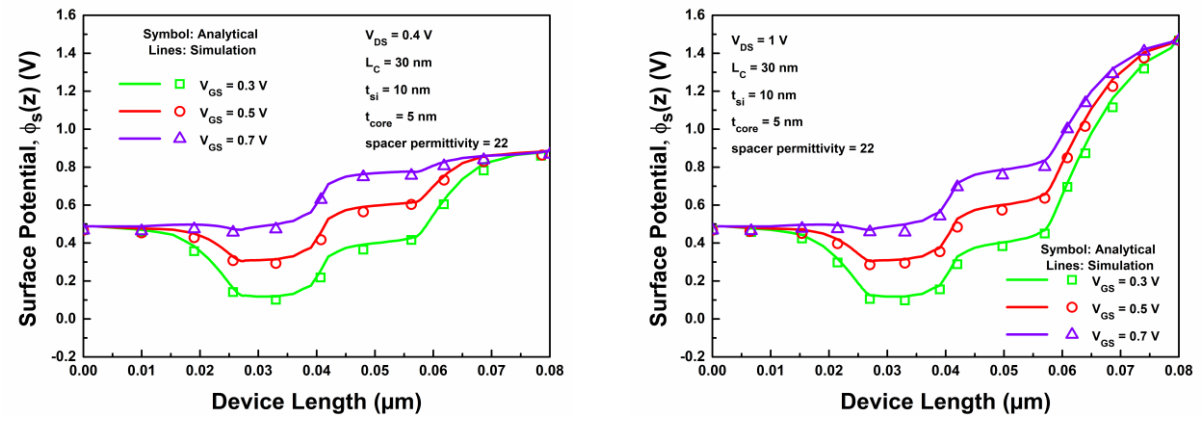
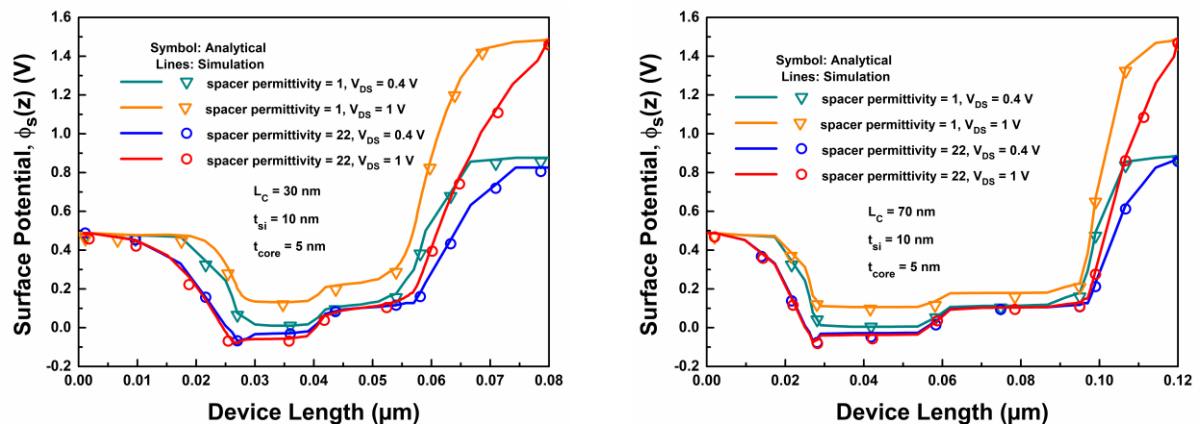


Fig. 3.25 Surface potential ($\phi_{S(z)}$) profile of I-JL-NWFET along device length for different V_{GS} at (A) V_{DS} = 0.4 V and (B) V_{DS} = 1 V

To analyse the effect of drain bias and spacer permittivity on L_C scaling, the variation in $\phi_S(z)$ of I-JL-NWFET in OFF-state at different L_C of 30 nm and 70 nm are presented in Fig. 3.26 (a) and (b), respectively, for different V_{DS} and spacer permittivities.



(a) (b)

Fig. 3.26 Surface potential ($\phi_{S(z)}$) profile of I-JL-NWFET along device length for different V_{DS} and spacer permittivities in OFF-state at L_C of (A) 30 nm and (B) 70 nm

It can be seen that $\phi_{S(z)}$ is more flat for longer L_C (L_C = 70 nm) than shorter L_C (L_C = 30 nm) on varying V_{DS} from 0.4 V to 1 V for unity spacer permittivity. Moreover, the minimum $\phi_{S(z)}$ is pulled up in the region–2, which in turn reduces V_T (Eqn. 3.181) and consequently increases the DIBL effect for the air spacer. Nevertheless, utilizing a high permittivity spacer mitigates the influence of drain bias on the minimum $\phi_{S(z)}$ on decreasing L_C (from 70 nm to 30 nm). This is owing to an enhanced fringing electric field, which experiences fewer carriers, allowing it to penetrate the shell region and lower the $\phi_{S(z)}$ as compared to unity spacer permittivity.

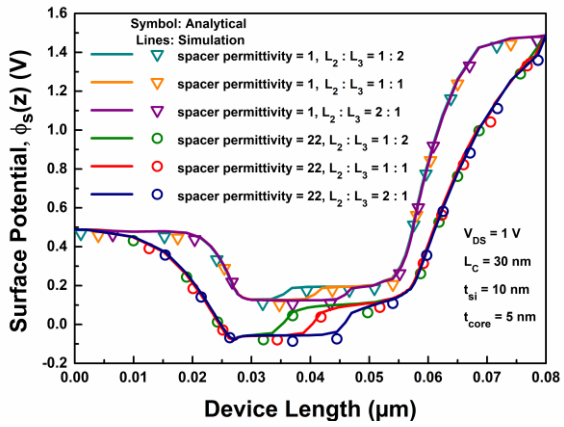


Fig. 3.27 Surface potential ($\phi_{S(z)}$) profile of I-JL-NWFET along device length in OFF-state for different $L_2 : L_3$ ratios

The variation in $\phi_{S(z)}$ of I-JL-NWFET along device length is analyzed for different ratios of L_2:L_3 and plotted in Fig. 3.27 while maintaining a fixed L_C (L_C = 30 nm) for air (permittivity = 1) and HfO_2 (permittivity = 22) spacer. It is observed that at any particular spacer permittivity, as the length of M_1 (L_2) decreases, the minimum $\phi_{S(z)}$ shifts towards the source side, resulting in a smaller V_T. This indicates that DIBL highly depends on channel ratios ($L_2 : L_3$). However, the step transition shifts towards the drain side with decreasing L_3, leading to higher device

reliability against DIBL. Additionally, the downward shift of $\phi_{S(z)}$ is more prominent for a high permittivity spacer compared to when no spacer is present. To balance the trade-off between V_T and DIBL, the ratio of $L_2 : L_3$ in the DMG structure for I-JL-NWFET should be kept at 1:1.

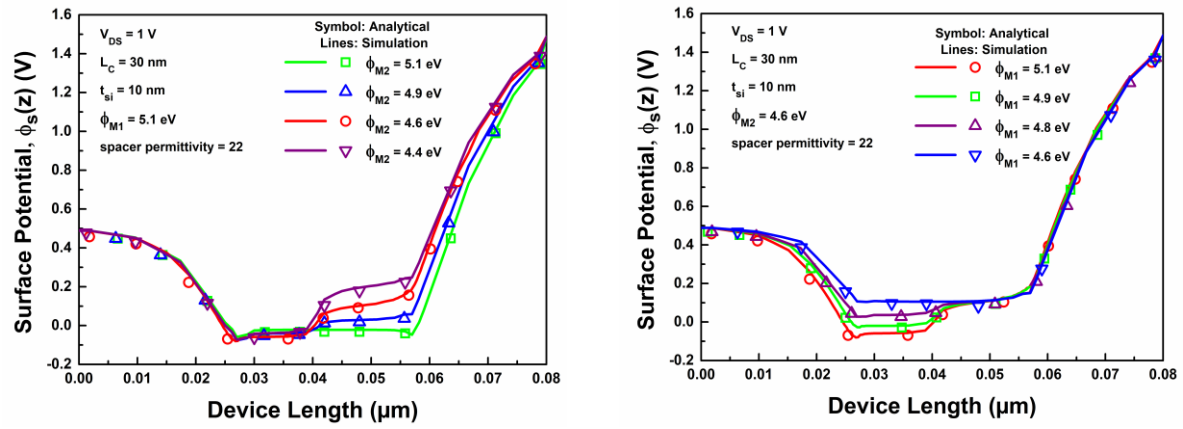
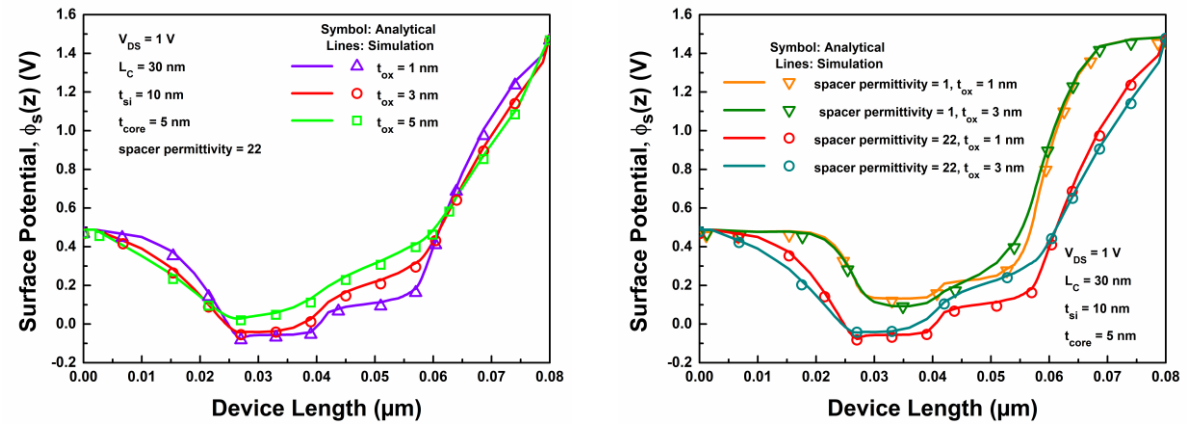


Fig. 3.28 Surface potential ($\phi_{S(z)}$) profile of I-JL-NWFET along device length for different work functions of (a) M_2 gate metal and (b) M_1 gate metal

Figure 3.28 (a) represents the variation in $\phi_{S(z)}$ of I-JL-NWFET along the device length by varying the M_2 work function (ϕ_{M2}) with fixed M_1 work function (ϕ_{M1} = 5.1 eV). A high ϕ_{M1} of 5.1 eV is maintained to ensure sufficient volume depletion during OFF-state in any JL-NWFET. It may be noted that when $\phi_{M1} = \phi_{M2} = 5.1$ eV, I-JL-NWFET exhibits SMG characteristics. As ϕ_{M2} decreases, a step-like variation is observed at the interface of dissimilar M_1 and M_2 caused by the work function difference ($\phi_{M1} - \phi_{M2}$). This step transition creates an electric field peak that enhances carrier mobility in the shell region, thereby increasing I_{ON}. Due to this abrupt change, the minimum $\phi_{S(z)}$ shifts under the M_1 region; therefore, for V_T derivation, only the M_1 region is considered.

This minimum $\phi_{S(z)}$ is screened from V_{DS} variation and thereby mitigates the DIBL effect, as also explained in Fig. 3.25 (a) and (b). A larger work function difference increases carrier transport efficiency. The higher electric field generated by M_1 increases carrier mobility. Besides this, the weaker vertical electric field generated by M_2 minimizes the hot carriers effect near the drain side. Fig. 3.28 (b) demonstrates the variation in $\phi_{S(z)}$ of I-JL-NWFET along the device length when the M_1 work function (ϕ_{M1}) is varied while keeping the M_2 work function (ϕ_{M2}) fixed at 4.6 eV. It is noted that when $\phi_{M1} = \phi_{M2} = 4.6$ eV, I-JL-NWFET behaves as SMG-I-JL-NWFET. As ϕ_{M1} decreases, the minimum $\phi_{S(z)}$ shifts upwards, reducing the device's V_T and causing the gate to lose control over the channel. Therefore, it is always preferable to have $\phi_{M1} > \phi_{M2}$ for the DMG structure.



(a) (b)

Fig. 3.29 Surface potential ($\phi_{S(z)}$) profile of I-JL-NWFET along device length in OFF-state for different (a) gate oxide thicknesses and (b) spacer permittivities

The impact of oxide thickness (t_{ox}) on $\phi_{S(z)}$ with fixed spacer permittivity of 22 is portrayed in Fig. 3.29 (a). It may be noted that as t_{ox} increases, scaling length increases (Eqn. 3.152). Consequently, the electrostatic integrity reduces, leading to an upward shift in the $\phi_{S(z)}$. This is because a thicker t_{ox} is less susceptible to penetration by the electric field from M_1 compared to a thinner t_{ox}. Moreover, the lower work function of M_2 causes a comparatively larger upward shift in $\phi_{S(z)}$ as t_{ox} increases from 1 to 5 nm, thereby degrading the threshold behavior of I-JL-NWFET . Therefore, the effect of M_2 is not considered in the modeling of V_T, as considered in Eqn. 3.181. The $\phi_{S(z)}$ in the OFF-state of I-JL-NWFET for different t_{ox} and spacer permittivities is compared in Fig. 3.29 (b).

In the case of an air spacer, a thicker t_{ox} (3 nm) leads to a reduced gate oxide capacitance, weakening the vertical electric field. Contrarily, a thicker t_{ox}, along with the inclusion of a high permittivity spacer, strengthens the control of the vertical electric field due to an increase in outer fringe capacitance. This enhances the fringing electric field in the S/D extension, allowing the vertical electric field to penetrate more easily into the shell region of the channel, pulling $\phi_{S(z)}$ downward compared to the absence of a spacer. Although a thinner t_{ox} (1 nm) should be used to improve immunity against SCEs, it may result in stress-induced leakage current. Therefore, utilizing a high permittivity spacer along with a thicker t_{ox} helps eliminate gate leakage current while achieving better gate controllability.

Figure 3.30 (a) depicts the transfer characteristics (in logarithm scale) of I-JL-NWFET for different core thicknesses with fixed spacer permittivity. Notably, a wider oppositely doped t_{core} leads to a reduction in I_{ON} at V_{GS} = 1 V, attributed to a decrease in shell thickness (t_{shell}), which serves as the active conduction region. Besides this, an increase in t_{core} from 0 to 7 nm effectively reduces the I_{OFF} by ~3 orders at V_{GS} = 0 V. This significant reduction in I_{OFF} is due

to the cumulative effect of the oppositely doped core that enhances volume depletion, the DMG structure that increases the tunneling width in the OFF-state, and the high permittivity spacer aids in depleting the channel beyond the gate region [22]. Nevertheless, beyond a t_{core} of 5 nm (half the channel thickness, t_{si} = 10 nm), further increases in t_{core} do not significantly impact I_{OFF}.

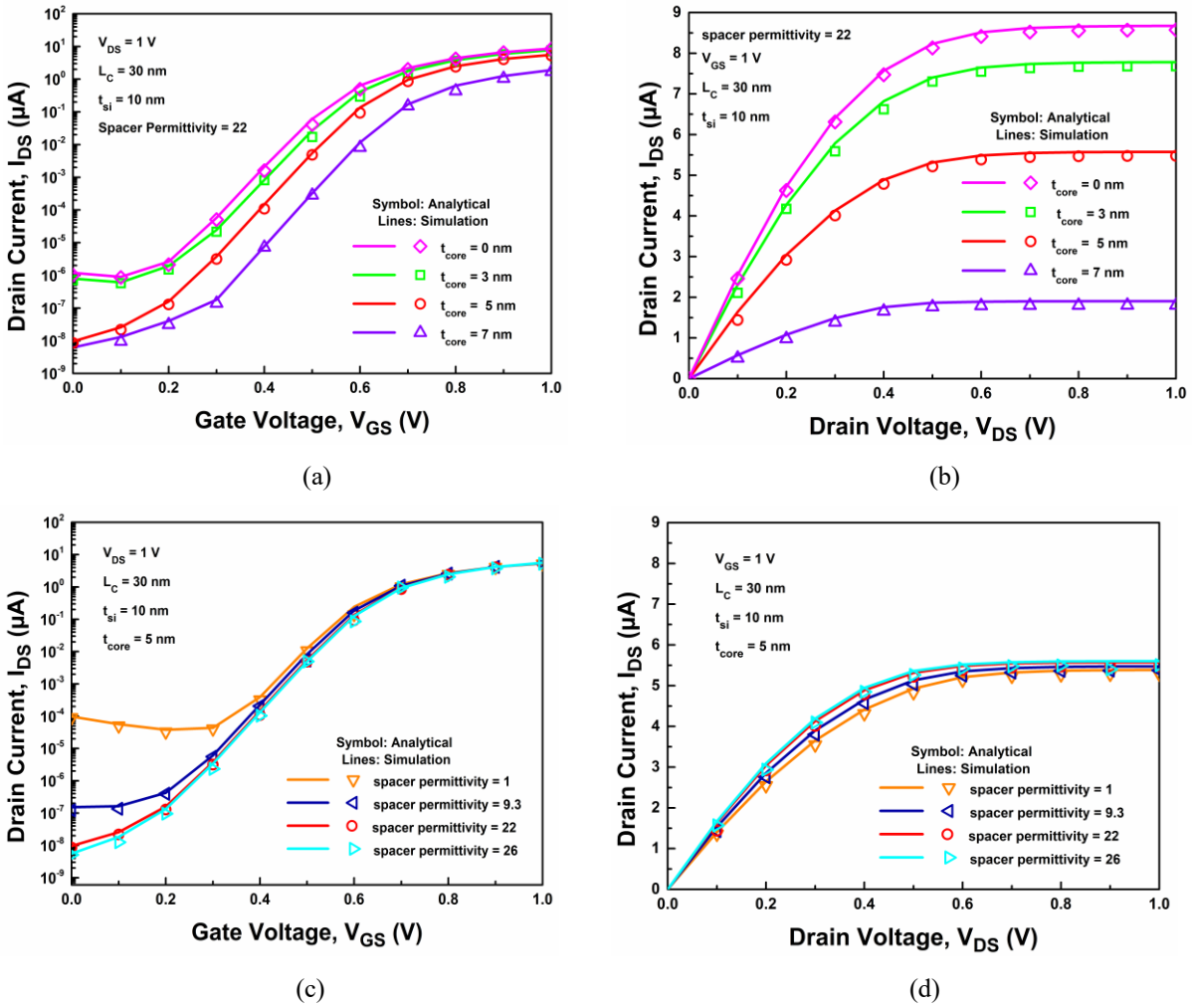


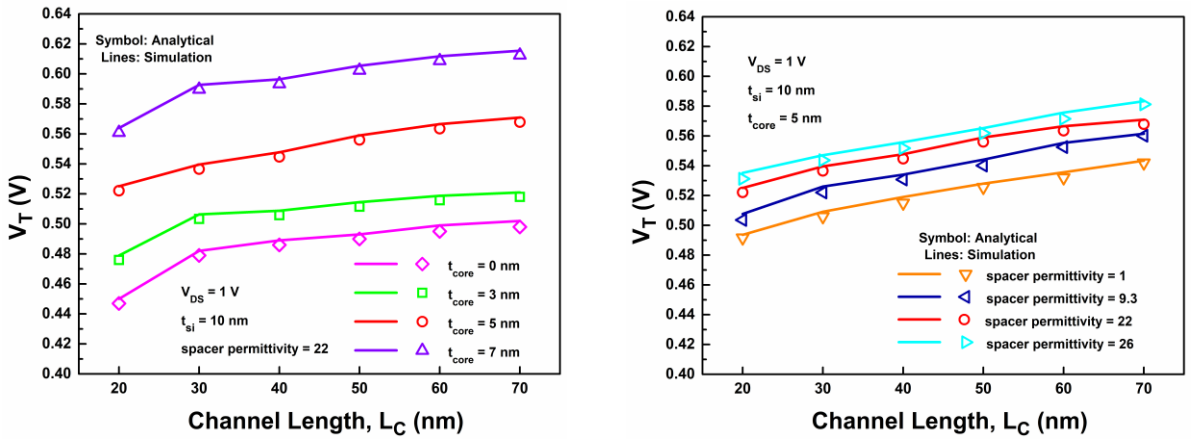
Fig. 3.30 (a) Transfer characteristics and (b) output characteristics for different core thicknesses, (c) transfer characteristics, and (d) output characteristics for different spacer permittivities of I-JL-NWFET

Figure 3.30 (b) portrays the output characteristics (in linear scale) where increasing t_{core} reduces I_{ON} as explained in Fig. 3.30 (a). Therefore, to balance the trade-off between I_{ON} and I_{OFF}, t_{core} should be kept as 50% of the t_{si} in the CS structure. The influence of spacer permittivity on the transfer characteristics (in logarithm scale) and output characteristics (linear scale) of I-JL-NWFET for fixed t_{core} are plotted in Fig. 3.30 (c) and (d), respectively. It is noted from Fig. 3.30 (c) that by increasing the permittivity of the spacer from 1 to 26, I_{OFF} reduces by four orders of magnitude. The dependence of I_{OFF} can be understood from the fact that a high permittivity spacer helps to deplete the channel beyond the gate region. On the other hand, a

slight improvement in I_{DS} is observed in Fig. 3.30 (d) due to the reduction in parasitic resistance in the region under the spacers with increasing spacer permittivity.

To understand the impact of L_C scaling on device parameters, L_C is varied from 70 nm to 30 nm. The influence of L_C scaling on V_T for different core thicknesses and spacer permittivities are illustrated in Fig. 3.31 (a) and (b), respectively. It is evident from Fig. 3.31 (a) that at a particular L_C (L_2 + L_3), with increasing t_{core}, V_T increases, as explained in Fig. 3.23 (a). This is mainly attributed to an oppositely and equally doped core that results in efficient depletion of the shell region. Consequently, a higher voltage is required to initiate conduction, as the channel is completely depleted by a thicker t_{core}, leading to an increase in V_T.

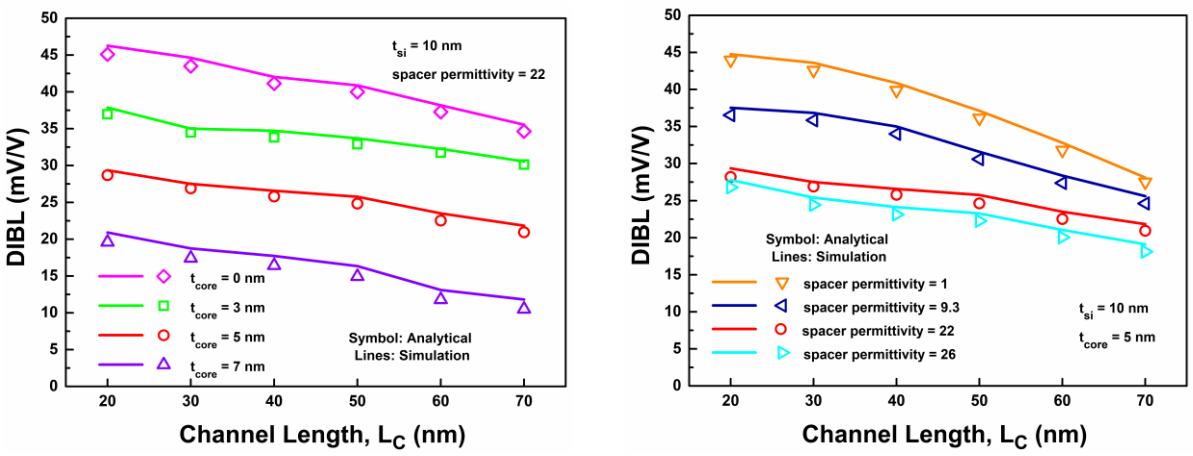
Additionally, V_T decreases with decreasing L_C at any given t_{core} as SCEs become more pronounced, as explained in Fig. 3.26 (a) and (b) for a spacer permittivity of 22. Furthermore, Fig. 3.31 (b) shows that the I-JL-NWFET with a high-permittivity spacer exhibits a higher V_T compared to a low-permittivity spacer for any given L_C. This is because the presence of spacers on both sides of the gate edges improves the OFF-state performance, as also observed in Fig. 3.24 (a). This highlights how the use of high-permittivity spacers in the S/D extension aids in scaling down the L_C.



(a) (b)

Fig. 3.31 Variation of V_T with L_C of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

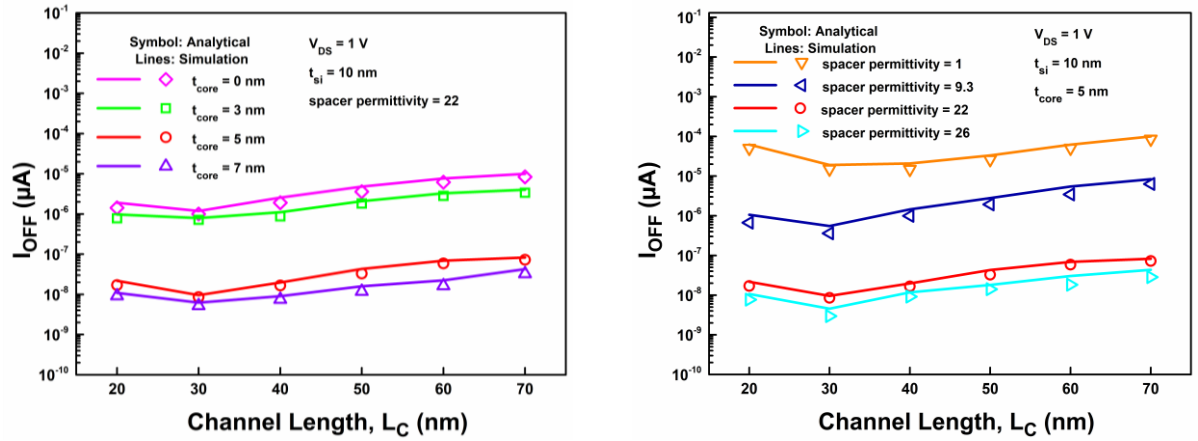
The impact of L_C scaling on DIBL for different core thicknesses and spacer permittivities are demonstrated in Fig. 3.32 (a) and (b), respectively. Fig. 3.32 (a) exhibits that with an increase in the width of the oppositely doped core (0 to 7 nm), the electrostatic integrity is enhanced, thereby, DIBL reduces for a fixed L_C. A wider oppositely doped core enhances electrostatic control, ensuring that the V_{GS} predominantly governs the channel potential while minimizing the impact of external influences such as the V_{DS}.



(a) (b)

Fig. 3.32 Variation of DIBL with L_C of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

Although the combination of DMG architecture and a thicker t_{core} reduces DIBL, scaling down the L_C exacerbates DIBL due to the increasing prominence of the horizontal electric field. Fig. 3.32 (b) shows that DIBL reduces using a high permittivity spacer at a given L_C due to an increase in fringing electric field, as explained in Fig. 3.26 (a) and (b). Although increasing t_{core} and high permittivity spacer reduces DIBL at a given L_C, it increases on decreasing L_C due to an increase in the horizontal electric field. A high DIBL on reducing L_C makes the device's operation more dependent on V_{DS}. This degrades switching characteristics, increases power consumption, and reduces reliability.



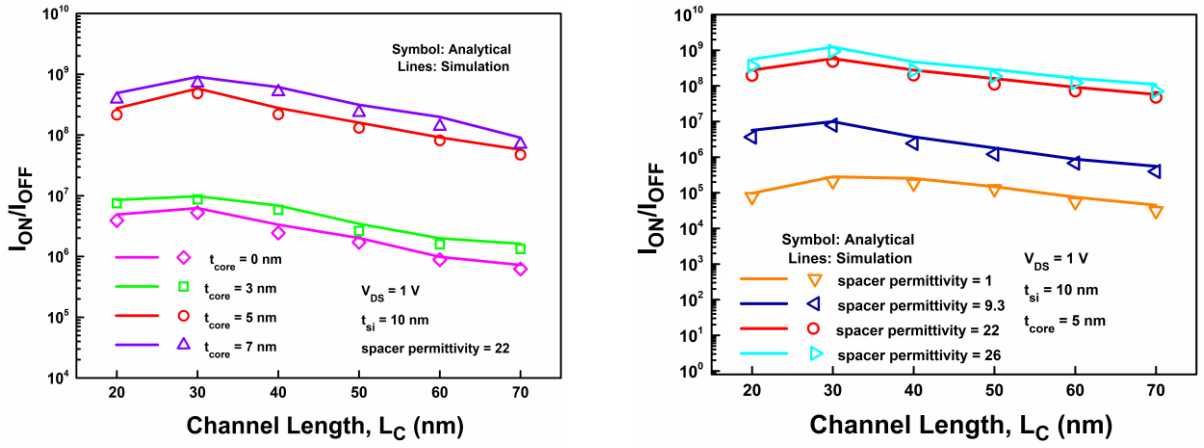
(a) (b)

Fig. 3.33 Variation of I_{OFF} with L_C of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

Figures 3.33 (a) and (b) present how the scaling of L_C affects I_{OFF} for various core thicknesses and spacer permittivities, respectively. In Fig. 3.33 (a), a significant reduction in I_{OFF} is observed when the t_{core} increases from 3 nm to 5 nm. This suggests that a 3 nm t_{core} may not

fully deplete the t_{si} during the OFF-state at the given L_C. However, increasing t_{core} beyond 5 nm still reduces I_{OFF}, but the improvement becomes less pronounced. In Fig. 3.33 (b), I_{OFF} decreases as the spacer permittivity increases from 1 to 26 at a specific L_C, as discussed in Fig. 30 (c). Nevertheless, in Fig. 3.33 (a) and (b), I_{OFF} increases as L_C is scaled down. This is due to the reduced gate control over the channel region and the resulting increase in SCEs.

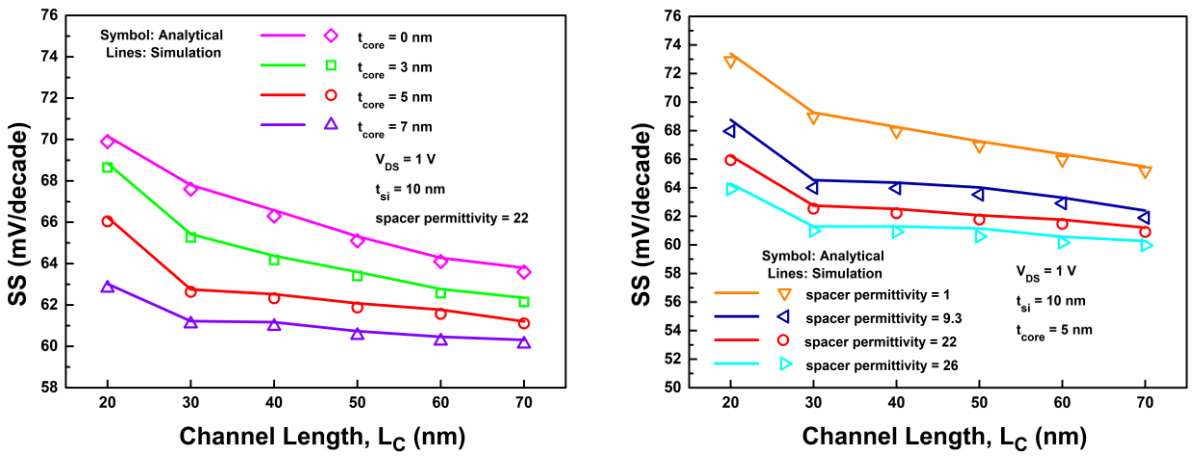
The effect of L_C scaling on the I_{ON}/I_{OFF} ratio for different core thicknesses and spacer permittivities are portrayed in Fig. 3.34 (a) and (b), respectively. A thicker t_{core} and higher permittivity spacer result in the highest I_{ON}/I_{OFF} ratio at a specific L_C, primarily due to a significant reduction in the I_{OFF}. Furthermore, the I_{ON}/I_{OFF} ratio increases less noticeably as L_C decreases in Fig. 3.34 (a) and (b), even though I_{OFF} tends to rise with decreasing L_C. This is attributed to the combined effect of the DMG structure, which enhances the I_{ON}, and the high-permittivity spacer, which lowers parasitic resistance in the spacer region, helping to enhance the overall I_{ON} behavior.



(a) (b)

Fig. 3.34 Variation of I_{ON}/I_{OFF} with L_C of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

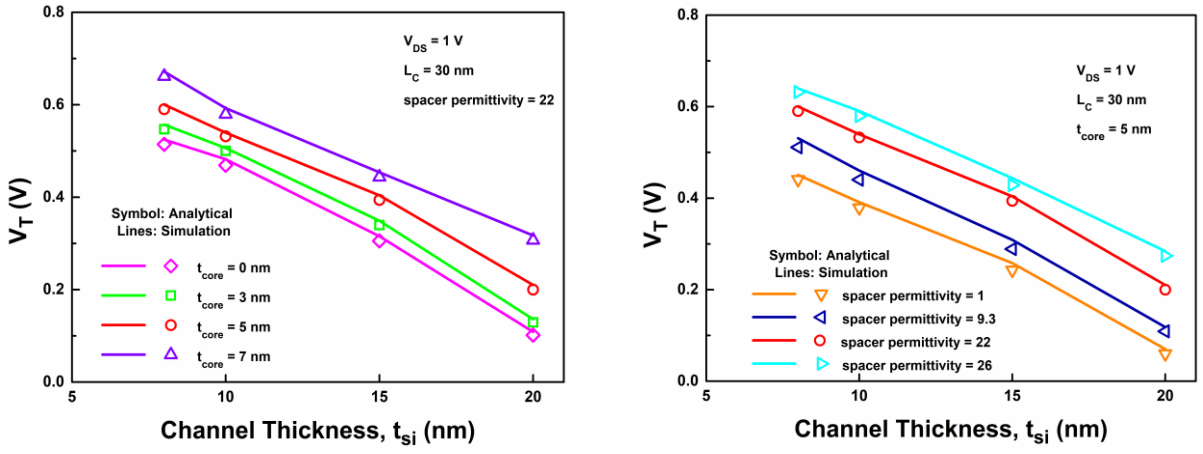
Figures 3.35 (a) and (b) depict the impact of SS for different core thicknesses and spacer permittivities, respectively, on varying L_C. In Fig. 3.35 (a), for any given L_C, a thicker t_{core} (7 nm) results in better SS performance compared to a thinner t_{core} (3 nm) or no core. A thicker oppositely doped core improves volume depletion in the channel, enhancing gate control over the channel potential. This reduces I_{OFF}, also as seen in Fig. 33 (a), leading to a steeper and more desirable transfer characteristic. A minimum SS is crucial because SCEs impair the device's ability to fully switch OFF, resulting in increased I_{OFF} and, consequently, enhancing SS. Analysing the SS of the proposed device at scaled-down channel lengths helps evaluate its effectiveness in suppressing SCEs.



(a) (b)

Fig. 3.35 Variation of SS with L_C of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

Additionally, Fig. 3.35 (b) indicates that SS improves with a higher permittivity spacer compared to a lower one at a specific L_C. This improvement is due to a reduction in the I_{OFF}, also as observed in Fig 33 (b), which can be attributed to enhancement in the fringing electric field in the OFF-state, allowing the gate to deplete the channel more effectively even beyond the physical gate edge. Nevertheless, as L_C is scaled down in Fig. 3.35 (a) and (b), SS tends to increase, primarily due to a rise in I_{OFF}, which worsens the steepness of the transfer characteristics. A higher SS on reducing L_C implies that the device requires a larger swing in V_{GS} to switch between OFF-state and ON-state, which compromises energy efficiency and results in slower transitions. This becomes particularly problematic for scaled devices where low-power operation is critical.

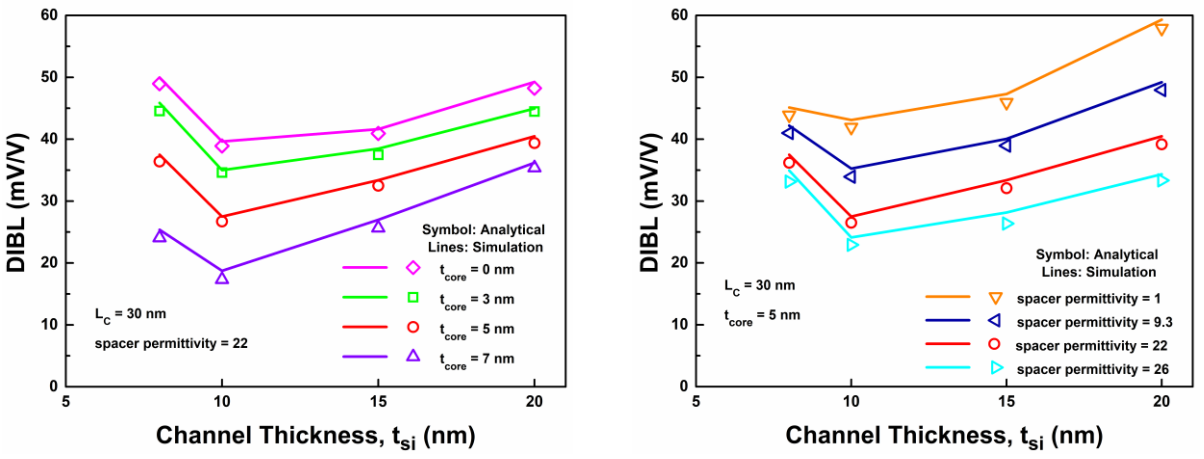


(a) (b)

Fig. 3.36 Variation of V_T with t_{si} of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

In order to investigate the impact of t_{si} scaling on device parameters, t_{si} is varied from 20 nm to 8 nm while maintaining a constant L_C of 30 nm. Fig. 3.36 (a) and (b) illustrate the impact of

t_{si} on V_T for different core thicknesses and spacer permittivities, respectively. It is observed from Fig. 3.36 (a) that V_T increases drastically on scaling t_{si} from 20 nm to 8 nm at any specific t_{core}. In the case of large t_{si}, thinner oppositely doped t_{core} may not deplete the shell region and subsequently require less gate voltage to initiate conduction. When t_{si} is scaled to 10 nm, gate control over the channel improves, and consequent thicker t_{core} (7 nm) required a higher V_T than thinner t_{core} (3 nm) or absence of core. Furthermore, Fig. 3.36 (b) clearly indicates that a high permittivity spacer also aids in volume depletion in large t_{si} (20 nm) when a 5 nm t_{core} is used. However, this may not be sufficient, and a higher V_{GS} is required for conduction. Besides this, as t_{si} is scaled down with fixed t_{core}, the shell region becomes depleted more easily, leading to an increase in V_T.

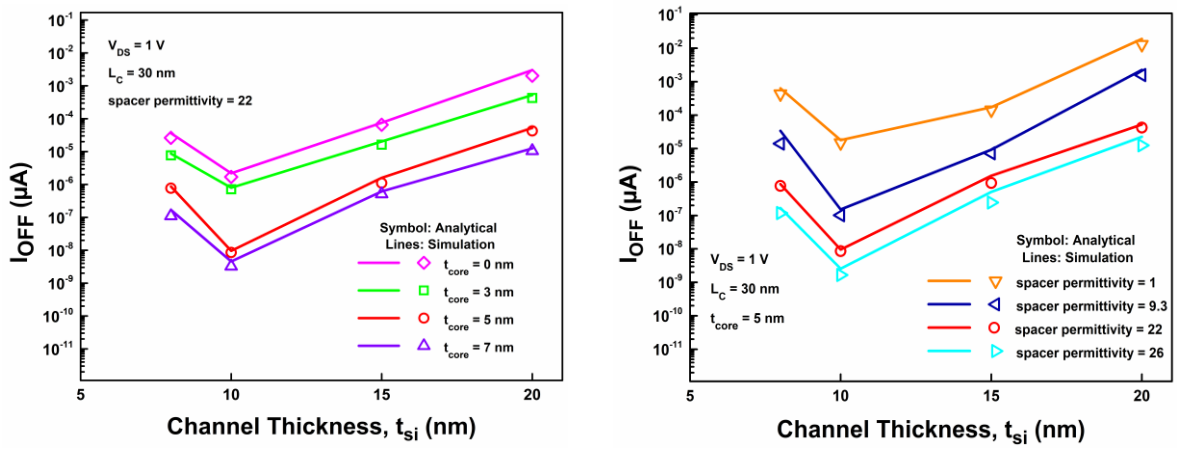


(a) (b)

Fig. 3.37 Variation of DIBL with *tsi* of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

The effect of t_{si} scaling on DIBL for different core thicknesses and spacer permittivities are demonstrated in Fig. 3.37 (a) and (b), respectively. It is observed from Fig. 3.37 (a) that DIBL is improved on the scaling down of t_{si} due to the prominent gate control provided by the smaller area of conduction in the shell region at any t_{core}. Moreover, the degree of improvement in DIBL with t_{si} scaling is prominent for a thicker t_{core} (7 nm) than a thinner t_{core} (3 nm). This is because the reduced shell region due to the thicker oppositely doped t_{core} experiences a less concentrated electric field from the drain to the source, which helps to reduce DIBL compared to the thinner t_{core}. Additionally, Fig. 3.37 (b) reveals that increasing the permittivity of the spacer over S/D extension reduces DIBL, as it helps in increasing the vertical electric field. This strengthens gate control over the channel and reduces the influence of the horizontal electric field from the drain bias. However, when t_{si} is scaled below 10 nm, DIBL increases due to an increase in SCEs.

Fig. 3.38 (a) and (b) compare the I_{OFF} of the I-JL-NWFET with varying t_{si} for different core thicknesses and spacer permittivities, respectively. In Fig. 3.38 (a), it can be observed that scaling down t_{si} leads to a more significant reduction in I_{OFF} when the *p*-type t_{core} is larger compared to when t_{core} is thinner. This is due to the decrease in the *n*-type shell region of the channel, which is more easily depleted as the shell region shrinks. However, when t_{core} exceeds 5 nm, the reduction in I_{OFF} becomes less pronounced on decreasing t_{si}. Fig. 3.38 (b) shows that increasing the spacer permittivity reduces I_{OFF} at fixed t_{si}, but beyond a permittivity of 22, the reduction in I_{OFF} becomes less significant. In both Fig. 3.38 (a) and (b), when t_{si} is reduced from 20 nm to 10 nm, the gate's electrostatic control over the shell region improves, leading to a decrease in I_{OFF}.



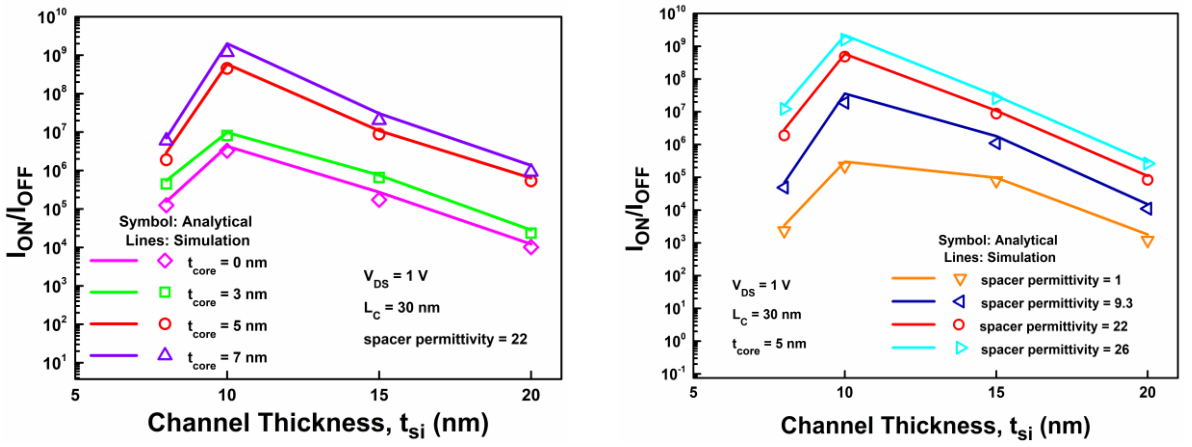
(a) (b)

Fig. 3.38 Variation of I_{OFF} with t_{si} of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

This is due to the presence of an oppositely doped core and a gate-sidewall spacer, which help enhance the gate's control. However, as t_{si} decreases further beyond 10 nm, the device starts to experience stronger SCEs, causing the gate's ability to control the shell region to diminish. This results in an increase in I_{OFF}, which is observed as a ditch in the I_{OFF} curve at t_{si} = 10 nm. The impact of this phenomenon is also evident in the I_{ON}/I_{OFF} ratio, as the increase in I_{OFF} at smaller values of t_{si} = 8 nm negatively affects the device's overall performance. Thus, the ditch at 10 nm of t_{si} reflects a trade-off between enhanced gate control at smaller values of t_{si} and the onset of SCEs, which limit the device's electrostatic integrity.

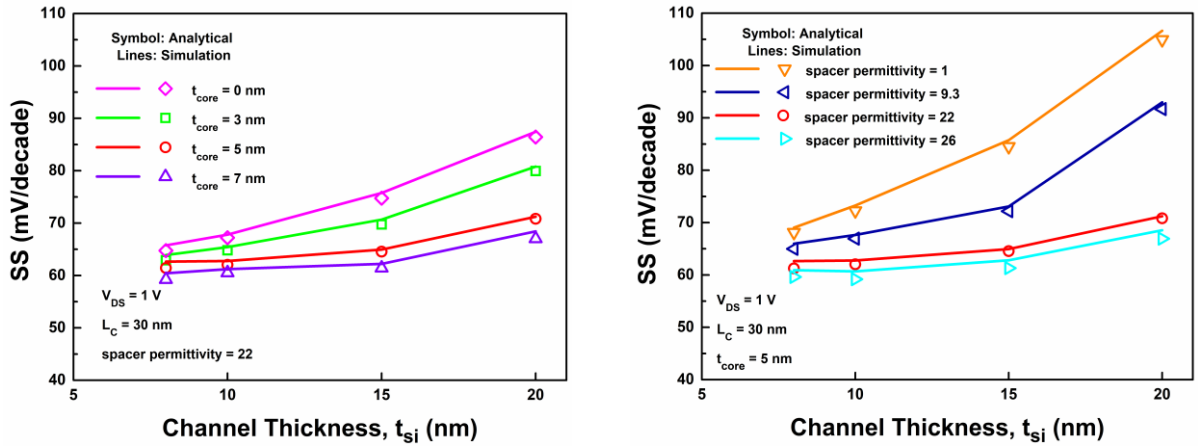
The influence of t_{si} scaling on the I_{ON}/I_{OFF} ratio for different core thicknesses and spacer permittivities are presented in Fig. 3.39 (a) and (b), respectively. The I_{ON}/I_{OFF} ratio in Fig. 3.39 (a) increases as t_{si} decreases until 10 nm at a particular t_{core}, primarily due to a significant decrease in I_{OFF}, as observed in Fig. 38 (a). Furthermore, a high permittivity spacer results in a higher I_{ON}/I_{OFF} ratio compared to a low permittivity spacer at specific t_{si}, as shown in Fig. 3.39

(b). However, the improvement in the I_{ON}/I_{OFF} ratio becomes less significant beyond a permittivity of 22. The I_{ON}/I_{OFF} ratio decreases when t_{si} exceeds 10 nm due to the increase in I_{OFF} in the ultra-thin shell region.



(a) (b)

Fig. 3.39 Variation of I_{ON}/I_{OFF} ratio with t_{si} of I-JL-NWFET for different (a) core thicknesses and (a) spacer permittivities



(a) (b)

Fig. 3.40 Variation of SS with t_{si} of I-JL-NWFET for different (a) core thicknesses and (b) spacer permittivities

The impact of scaling t_{si} on SS for different core thicknesses and spacer permittivities are depicted in Fig. 3.40 (a) and (b), respectively. As t_{si} decreases in Fig. 3.40 (a), the SS reduces at any t_{core} attributed to the higher gate control over a smaller channel that reduces I_{OFF}. Moreover, a thinner oppositely doped t_{core} may fail to sufficiently deplete the shell region, resulting in a higher I_{OFF}. Consequently, the improvement in SS is more significant for a thicker t_{core} (7 nm) compared to a thinner core (3 nm) at any given t_{si}. Besides this, when t_{core} exceeds 5 nm, the improvement in SS becomes less pronounced. Furthermore, in Fig. 3.40 (b), as the permittivity of the spacer increases, SS improves at fixed t_{si} due to steep switching characteristics as I_{OFF} decreases. However, when permittivity exceeds 22, the improvement in

SS becomes less significant. When t_{si} is scaled down, SS improves due to I_{OFF} reduction, as the smaller shell region can be more easily depleted of carriers during the OFF-state, resulting in a steeper slope of the I_{DS}-V_{GS} characteristics.

Table 3.2. Performance comparison of the proposed I-JL-NWFET with other junctionless devices

Parameters	CS CSG JL NMOSFET [47]	DM GAA JL NCFET [127]	JL-Mac. DM CGAA MOSFET [128]	I-JL-NWFET (This work)
Channel Length, L_C (nm)	30	30	30	30 nm
Channel Thickness, t_{si} (nm)	10 (t_{core} = 2 nm)	10	10	10 nm
Drain Voltage, V_{DS} (V)	0.5 V	0.1	0.1	1 V
Gate Work Function (eV)	5.2	4.6 (M_1), 4.4 (M_2)	5.1 (M_1), 4.6 (M_2)	5.1 (M_1), 4.6 (M_2)
Threshold Voltage, V_T (V)	0.11	0.235	0.805	0.52
SS (mV/decade)	-	52	-	62.63
DIBL (mV/V)	12.5	0.07	19	26.90

Table 3.2 compares the analytical values of I-JL-NWFET with CS Channel Surrounding Gate (CSG) JL NMOSFET [47], Dual Material (DM) GAA JL Negative Capacitance (NC) FET [127], and JL-Macaroni (Mac.) DM Cylindrical GAA MOSFET [128]. It is observed that advanced structures in JL devices, operating at different V_{DS}, effectively mitigate SCEs, highlighting their suitability for nanoscale technology nodes.

3.5 SUMMARY OF THE IMPORTANT RESULTS

The current chapter focuses on the analytical investigation of the proposed I-JL-NWFET to validate the electrostatic behaviour of the cylindrical nanowire structures with analytical solutions. Since the electrostatic characteristics of cylindrical JL-NWFETs differ significantly from those of conventional planar devices, analytical formulations developed for planar transistors cannot be directly applied. Therefore, a dedicated cylindrical analytical framework is developed to accurately capture the potential distribution, electric field behaviour, and current transport in the proposed structures. The analytical models are further validated through comparison with TCAD simulation results.

- Firstly, a quasi-analytical model for the DMG-CS-JL-NWFET is developed by solving the two-dimensional Poisson's equation in cylindrical coordinates using the surface potential approach. The analytical results show close agreement with TCAD simulation data over a wide range of device parameters by varying t_{core}, t_{si}, t_{ox}, and L_C.
- The analytical investigation of DMG-CS-JL-NWFET reveals that maintaining the t_{core} equal to half of the t_{si} effectively suppresses I_{OFF} while preserving the I_{sub}. It is further

observed that increasing the t_{core} beyond this optimum value reduces I_{OFF} further but adversely affects the subthreshold conduction.

- A physics-based analytical model for the GSS-CS-JL-NWFET is developed by incorporating fringe capacitance effects. The analytical expressions for surface potential, V_T, I_{DS}, and SS are derived and validated through TCAD simulations, demonstrating good agreement.
- The analysis of GSS-CS-JL-NWFET establishes that the optimum design is achieved when the t_{core} is maintained at half of the t_{si} and the core doping is equal in magnitude but opposite in type to that of the shell region. In addition, the use of a high-permittivity HfO_2 spacer is found to effectively reduce I_{OFF} and improve SS.
- A comprehensive analytical model of the proposed I-JL-NWFET incorporating CS, DMG, and GSS architecture is developed. The surface potential model is utilized to derive the key device parameters such as V_T, DIBL, I_{DS}, and SS.
- The analysis further demonstrates that proper selection of t_{core}, t_{si}, L_C, and spacer permittivity effectively improves electrostatic control over the channel, mitigates DIBL, and enhances subthreshold characteristics.

The present chapter establishes a comprehensive analytical foundation for the proposed I-JL-NWFET by systematically modelling intermediate device configurations prior to the final combined architecture. Moreover, the analytical models not only provide valuable physical understanding of the device behaviour but also serve as effective design guidelines for optimizing future cylindrical I-JL-NWFET. The future research may focus on extending the analytical framework by incorporating interface trap effects, quantum confinement, variability analysis, and advanced channel materials to further improve the accuracy, scalability, and applicability of next-generation JL-NWFET devices.

CHAPTER-4
p53 BIOMARKER DETECTION FOR GASTROINTESTINAL CANCER USING IMPROVED JUNCTIONLESS NANOWIRE FET

4.1 INTRODUCTION

Gastrointestinal (GI) cancer stands among the most prevalent cancers globally and is the second leading cause of cancer-related deaths, accounting for around 700,000 fatalities annually. GI cancers encompass a group of malignant tumours that originate in the gastrointestinal tract and associated digestive organs. These include carcinomas that develop in the oral cavity, esophagus, stomach, liver, bile duct, gallbladder, pancreas, small intestine, and large intestine [129, 130]. Affecting both men and women, GI cancers impose a substantial burden on global health due to their high incidence and associated mortality.

The early symptoms of GI cancer are often subtle or absent, leading to most cases being diagnosed at advanced stages, which significantly limits treatment effectiveness [131]. Early detection and timely intervention are key to improving cure rates, reducing mortality, and enhancing patient's quality of life. Moreover, early-stage cancer treatment typically requires fewer resources and less invasive interventions, thus lowering healthcare costs and easing financial burdens on patients. The p53 tumour suppressor protein is one of the most widely studied and clinically utilized biomarkers in cancer diagnostics [132-134].

Its overexpression has been observed in various GI cancers, and several studies suggest that detecting p53 in serum could serve as a valuable tumour marker [135, 136]. Commonly known as the "guardian of the genome," p53 plays a crucial role in preserving genomic stability [137-139]. It is among the most frequently mutated genes in human cancers, with mutation rates differing by cancer type. Through its regulation of apoptosis and cell cycle arrest, p53 helps eliminate damaged cells, thereby preventing their progression into malignant tumours. Although current diagnostic techniques offer high sensitivity, they come with significant limitations.

The primary diagnostic methods for GI cancer include endoscopy, Magnetic Resonance Imaging (MRI), Computed Tomography (CT), and Positron Emission Tomography (PET) [140-142]. These methods are costly, confined to hospital settings, and require skilled

professionals to operate. This poses a serious challenge for patients in remote or underserved areas, who often lack access to timely and efficient diagnostic services. Consequently, there is a growing demand for rapid, affordable, and accessible diagnostic solutions. In this context, the development of a portable biosensor offers a promising alternative, enabling early detection in a way that is both cost-effective and user-friendly, aligning with the broader medical consensus that accurate diagnosis is the foundation of effective treatment.

The biosensors are analytical devices that detect biomolecules and convert their concentrations into measurable signals, offering rapid and accurate diagnostics, particularly valuable for early cancer detection [143]. Across the world, a wide variety of biosensors have been developed, including electrochemical, organic, capacitive, and optical types [144-148]. Among these, FET-based biosensors have garnered significant interest from the scientific community due to their exceptional sensing capabilities, offering high sensitivity, specificity, and rapid response to target concentrations [149].

The first ion-sensitive FET-based biosensor was introduced by P. Bergveld in 1970 [150]. The FET-based biosensor's compatibility with semiconductor technology enables low-cost production and scalability, making it ideal for mass manufacturing, as also highlighted in the recent studies [60-73]. However, the sensitivity performance metrics of FET-based biosensors are limited by SCEs [151]. Huang *et al.* [152] demonstrated that sensitivity can be further enhanced by improving the electrostatic gate control over the channel in a conventional NWFET having cylindrical structures.

Meanwhile, JL-NWFETs have been designed for bio-sensing applications only for proteins and other biomolecules and not for any cancer detection. Even though JL-NWFET has become a strong alternative to NWFET, it suffers from the major limitations of volume depletion and parasitic BJT phenomenon [13, 17]. Inspired by these advancements in the FET-based detection of biomarkers for cancer detection and the urgent need for GI cancer detection, the current chapter reports the electrical detection of GI cancer biomarker p53, which has not yet been reported in the existing literature using a I-JL-NWFET.

Therefore, the following objective is framed here to utilize the proposed I-JL-NWFET for biomedical application:

"Performance Assessment of Improved Nanowire FET for Biomedical Application."

To realize the desired objective, the methodology includes the following steps: -

- Initially, the p53 biomarker is chosen for cholangiocarcinoma, a type GI cancer, based on available clinical concentrations between healthy and diseased samples, based on the comprehensive literature survey.
- Subsequently, the proposed I-JL-NWFET is utilized for biosensing using SILVACO ATLAS and is systematically optimized in terms of nanocavity position and by varying cavity length. Thereafter, the sensing performance of the optimized device is evaluated using the sensitivities for various healthy and diseased biomarker concentrations.
- Furthermore, the analysis is carried out by examining the influence of temperature variation, cavity occupancy, and repulsive steric hindrance effects to obtain a realistic insight into biosensor behaviour under practical operating conditions.
- Finally, the proposed biosensor is integrated with a readout circuit to convert biomolecule-induced drain current variations into measurable voltage shifts using the MixedMode circuit simulator in SILVACO ATLAS, thereby assessing its suitability for practical biomedical detection applications.

This chapter is organized into four sections, commencing with the introduction in Section 4.1. Section 4.2 covers the device structure and the methodology for GI cancer detection using the I-JL-NWFET. Subsequently, the optimization and performance analysis of the I-JL-NWFET based biosensor are presented in Section 4.3. Eventually, Section 4.4 incorporates the necessary summary.

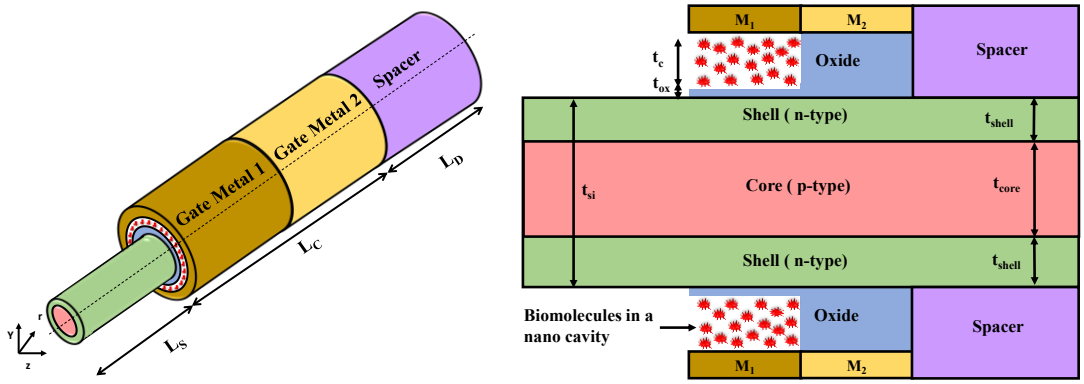
4.2 GI CANCER DETECTION USING PROPOSED I-JL-NWFET

This section presents a comprehensive methodology for the detection of the GI cancer biomarker p53 using the proposed I-JL-NWFET based biosensor. It encompasses detailed descriptions of the device architecture and biomolecular interaction mechanisms, followed by the modeling framework developed to simulate the detection of p53. It may be noted that this chapter is entirely based on TCAD simulations, with experimental procedures from literature used solely as references to ensure realistic modeling parameters and biofunctionalization conditions.

4.2.1 Device Structure of I-JL-NWET based Biosensor

The 3-D and 2-D schematic views of the I-JL-NWFET based biosensor with nanocavity are illustrated in Fig. 4.1 (a) and (b), respectively. The proposed biosensor is used for the sensitivity analysis of the GI cancer biomarker, i.e., p53. The parameters and material used for I-JL-NWFET based biosensor are presented in Table 4.1. The proposed biosensor employed during

the simulation analysis have the L_C of 30 nm, t_{ox} of 1 nm, and t_{si} of 10 nm. An oppositely and equally doped core (p-type, $N_a = 1\times10^{19}$ cm^{-3}) is incorporated in the middle of the channel (n-type, $N_d = 1 \times 10^{19}$ cm^{-3}). In the proposed device, the core is p-type and the shell is n-type, making the device n-type overall. If the core is n-type and the shell is p-type, the device becomes p-type, with hole conduction dominating instead of electron conduction. The inclusion of an oppositely doped p-type core offers an advantage over conventional n-type JL-NWFET, effectively depleting the channel in the OFF-state and reducing the parasitic BJT phenomenon.



(a) (b)

Fig. 4.1 (a) 3-D view and (b) schematic of I-JL-NWFET based biosensor, highlighting the nanocavity region used for biomolecule detection

Table 4.1. Device specification for the proposed I-JL-NWFET based biosensor

Device Parameters		**I-JL-NWFET**	
Channel	Material	Silicon	
	Length, L_C (nm)	15 (L_{M1})	15 (L_{M2})
	Thickness, t_{si} (nm)	10	
	Doping, N_D (cm^{-3})	1×10^{19}	
Core	Material	Silicon	
	Thickness, t_{core} (nm)	10	
	Doping, N_A (cm^{-3})	1×10^{19}	
Gate	Workfunction (eV)	5.1 (M_1)	4.6 (M_2)
Gate Oxide	Material	SiO_2	
	Thickness, t_{ox} (nm)	1	
Source/Drain	Length, $L_{S/D}$ (nm)	25	
Spacer	Material (Drain side only)	HfO_2	
	Length (nm)	25	
Cavity	Length, L_{cav} (nm)	15 nm from the source side	
	Thickness, t_c (nm)	10 nm	

In the p-type device (n-core, p-shell), similar depletion benefits would be obtained, but the device would operate with hole transport, resulting in a lower mobility and potentially reduced ON-state current compared to the n-type version under identical bias conditions. However, in

the I-JL-NWFET-based biosensor, a cavity needs to be created from the source side. As a result, the spacer on the source side is etched away, leaving only the HfO_2 spacer on the drain side. For future experimental realization of I-JL-NWFET, the stepwise possible fabrication process flow is already explained in Fig. 2.8. Additionally, for biosensor implementation using I-JL-NWFET, the nanocavity, which is essential for biosensing functionality, is created by selectively etching the gate spacer on the source side and subsequently removing the underlying gate oxide to expose the sensing region [153].

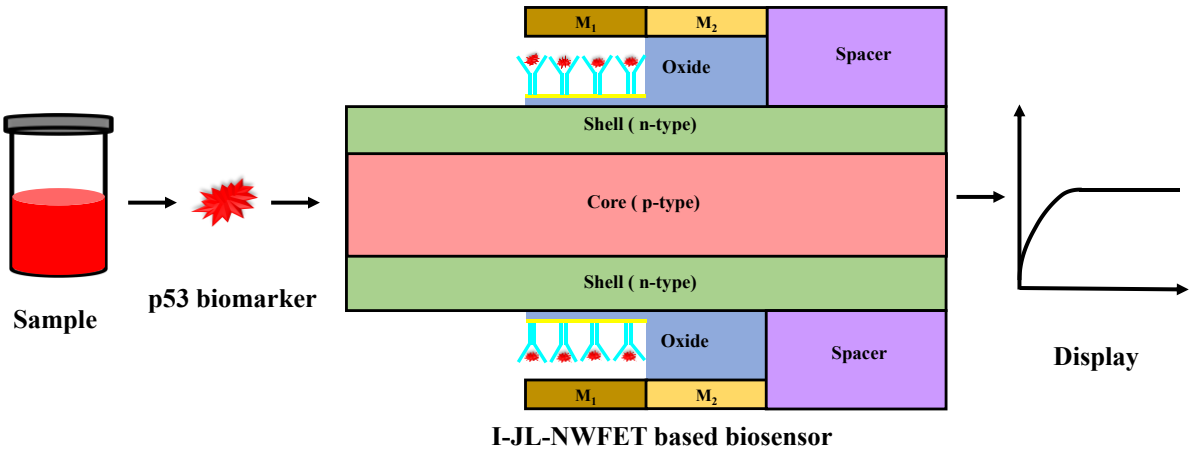


Fig. 4.2 Illustration of the GI cancer detection process using the proposed I-JL-NWFET based biosensor, where the p53 biomarker is selectively captured and identified

The p53 protein molecules typically exhibit a size in the range of approximately 6–8 nm [154]. Accordingly, a nanocavity with a thickness of 10 nm is deemed adequate to facilitate the immobilization of biomolecules for detection purposes using the I-JL-NWFET based biosensor. The proposed I-JL-NWFET based biosensor is optimized for biomolecules up to ~10 nm in their smallest dimension, matching the nanocavity thickness (t_c) to ensure complete immobilization and strong electrostatic coupling with the channel. The smaller species, such as biotin or streptavidin, fall within the 3–5 nm range, can also be detected, with sensitivity influenced by net charge and orientation.

For larger biomolecules, the t_c can be increased to avoid steric hindrance and maintain binding efficiency. The feasibility of fabricating nanocavities with this dimension has been experimentally validated in [153]. To enhance the binding affinity and immobilization efficiency of p53 biomolecules within the cavity region, a total gate stack thickness of 1 nm, comprising a gold (*Au*) coating on SiO_2, is employed [63]. The gold coating was introduced to

enable stable and efficient biofunctionalization via thiol–gold chemistry, which allows covalent attachment of biomolecule linkers followed by immobilization of the p53-specific antibody.

The process flow diagram, illustrated in Fig. 4.2, outlines the sequential steps involved in the detection of p53 biomolecules. The detection mechanism is based on an interface charge deduction strategy. In this method, the effective interfacial charge induced by the presence of p53 biomolecules in blood serum is quantitatively extracted and applied to the interfacial region of the I-JL-NWFET based biosensor. This approach enables the sensitive and label-free detection of p53, facilitating early diagnosis of various GI cancers.

4.2.2 p53 Model and Detection Mechanism

The p53 gene, first described in 1979, was the first tumour-suppressor gene to be identified [155]. The p53 contains 393 amino acids and has a 53 kDa Molecular Weight (MW) with an isoelectric point (pI) of 6.50 [139, 156]. The p53 molecules in the serum will be negatively charged since the pH of blood (pH = 7.4) > pI of p53 [157]. It has been experimentally proven that FET can be used effectively in the detection of p53 protein [70, 158]. For analysing the sensing behavior of the device, charge control can be developed, for which the effective charge due to p53 has to be numerically modeled.

To achieve this, the net charge due to p53 molecules in the blood sample is calculated and applied as a charge at the oxide-channel interface. The physical recognition procedure includes a thin layer of gold-coated SiO_2. The immobilization process follows established biofunctionalization protocols reported in experimental work [70]. Briefly, the gold-coated SiO_2 surface is cleaned and functionalized with a mixed solution of SH-PEG-COOH and SH-PEG (40 μM:2 μM) in PBS 1X (pH 7.4) for one hour at room temperature. The surface is then activated with N-ethyl-N-(3-(dimethylamino)propyl) carbodiimide (EDC) and N-hydroxysuccinimide (NHS) at 0.4 M/0.1 M in PBS 1X (pH 7.4) for 20 min at room temperature.

Subsequently, the device is incubated overnight at 4 °C with the p53-specific capture antibody (PAb1620) at 13 nM in PBS 1X (pH 7.4). Finally, unreacted sites are blocked with Bovine Serum Albumin (BSA) (1 mg/mL in PBS 1X, pH 7.4) to prevent non-specific adsorption. The adsorption of p53 biomolecules onto the sensor surface is not solely governed by electrostatic differences in isoelectric points, but rather by a specific biofunctionalization mechanism that enables selective capture of the target protein. The sensing surface (gold-coated SiO_2) undergoes sequential chemical modification with SH-PEG/SH-PEG-COOH (biomolecule linker), followed by EDC/NHS activation to introduce reactive ester groups.

This allows covalent immobilization of the p53-specific capture antibody (PAb1620) through amide bond formation with the antibody's primary amine groups. The immobilization step is carried out overnight at 4 °C to ensure stable binding. Post-functionalization, non-specific binding sites are blocked with BSA. This procedure ensures that the adsorption of p53 molecules occurs specifically via antigen–antibody binding and not due to non-specific electrostatic interactions. Once the target p53 molecules bind to their immobilized antibodies, the interaction is irreversible under measurement conditions and not in dynamic equilibrium with the solution concentration. This covalent and bio-recognition-based approach confers high specificity to the proposed biosensor rather than making it an ion-sensitive device.

The binding kinetics of p53 biomolecules at the sensing surface are governed by both the bio-analyte concentration in the sample and the dominant transport mechanism. At the low clinical concentrations considered in this work, the transport of p53 molecules from the bulk solution to the functionalized sensing surface is primarily diffusion-limited. Once at the surface, the specific antigen–antibody interaction between p53 and immobilized PAb1620 dominates the binding process, leading to stable, irreversible attachment under measurement conditions. The rate of binding increases with analyte concentration due to the higher probability of molecular encounters, but the binding reaches saturation once all available antibody sites are occupied.

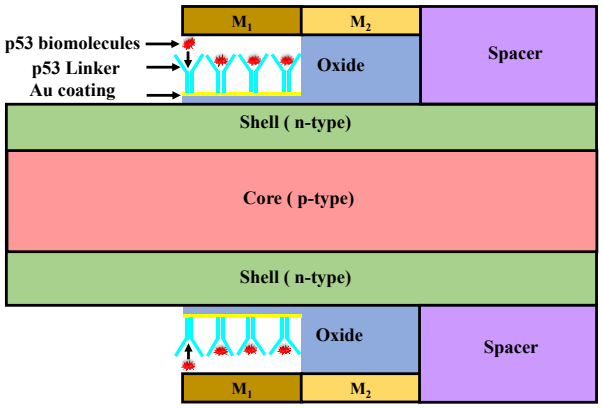


Fig. 4.3 Immobilization of p53 biomolecules at the nanocavity using the target-capturing p53 linker, ensuring selective binding to the target biomarker

These characteristics are incorporated into the numerical modeling by representing the effect of bound p53 molecules as an equivalent fixed interface charge at the oxide–channel interface. The detection process of p53 biomolecules is shown in Fig. 4.3, illustrating the immobilization of p53 biomolecules after binding with the linker PAb1620. After the p53 biomolecules are immobilized with the linkers inside the cavity, the electrostatic characteristics of the I-JL-NWFET change, resulting in the detection of p53 molecules. The proposed biosensor employs

a specific antigen–antibody recognition mechanism, which significantly reduces the influence of the general acidic or alkaline properties of non-target biomolecules.

The surface functionalization with SH-PEG/SH-PEG-COOH and BSA blocking minimizes non-specific adsorption, thereby suppressing pH-related interference from non-target species. Since detection is based on the stable covalent immobilization of p53-specific antibodies and the subsequent binding of p53 molecules, the signal primarily reflects target-specific electrostatic modulation rather than bulk solution pH variations. Further research can extend this work by performing detection studies in controlled acidic or alkaline buffer environments to evaluate device robustness under varying pH conditions.

Such investigations could also explore integrating reference sensors or differential measurement schemes to further eliminate residual pH effects, enabling reliable biosensing in diverse biochemical settings. The linearity in the proposed biosensor is ensured by modeling and measuring the device response over a defined p53 concentration range, where the induced interface charge varies proportionally with analyte concentration, resulting in a consistent modulation of the surface potential and drain current. The specificity is achieved through covalent immobilization of the p53-specific capture antibody (PAb1620) via SH-PEG/SH-PEG-COOH functionalization and EDC/NHS activation, ensuring that only p53 molecules bind effectively.

The selectivity is maintained by blocking unreacted surface sites with BSA, which suppresses non-specific adsorption from other biomolecules. The antigen–antibody binding mechanism, combined with the blocking layer, enables the biosensor to reliably differentiate p53 from non-target proteins, even in complex bio-environments. To investigate the sensing behavior of the proposed device, a numerical model is used to simulate the modulation of interface charge resulting from the presence of p53 molecules. The equivalent interface charge, denoted as Q_{p53} , plays a critical role in modulating the surface potential and consequently the device's electrical response.

The Q_{p53} induced by p53 molecules present in a blood serum sample can be estimated using the following expression [63, 64]

$$Q_{p53} = \left(Conc._{p53} \times q_{p53} \right) \times AvogadroNumber \tag{4.1}$$

where the molar concentration of p53 ($Conc._{p53}$) is calculated by dividing the concentration of p53 by its MW. The obtained $Conc._{p53}$ is multiplied by the net effective charge per p53

biomolecule (q_{p53}), taken as 4e [159], and Avogadro Number, which is 6.023×10^{23}. The serum concentrations of the tumour suppressor protein p53 were investigated for both healthy individuals and patients diagnosed with GI cancer.

Table 4.2. Equivalent charges for p53 concentrations for healthy and diseased persons

Type of Patients	Healthy	Diseased (Cholangiocarcinoma)
Clinically Relevant Biomarker Concentration (Mean ± S.D. (ng/ml)) [160]	0.19 ± 0.08	1.03 ± 0.59
Concentration Range (ng/ml)	0.11 to 0.27	0.44 to 1.62
Equivalent Interface Charges ($\times10^{12}$ q/cm^2)	-5 to -12.27	-20 to -73.63

Specifically, a 100% positivity rate was observed for cholangiocarcinoma, which is a malignancy that originate in the bile ducts. As summarized in Table 4.2, the p53 concentrations are clinically reported in terms of Mean ± Standard Deviation (S.D.), which is 0.19 ± 0.08 ng/ml for healthy individuals and 1.03 ± 0.59 ng/ml for patients with cholangiocarcinoma [160]. This statistical representation presumes a Gaussian distribution, a convention widely adopted in biosensor modeling and biomedical analytics [161]. Utilizing the empirical 68% rule, which states that approximately 68% of measurements lie within ±1 S.D. of the mean, the physiologically relevant concentration range for diseased individuals spans from 0.44 to 1.62 ng/ml.

This range serves as the clinically actionable window for biosensor calibration, ensuring that simulation inputs reflect the biological heterogeneity and patient-to-patient variability present in real-world clinical data. Importantly, relying solely on the mean value for simulations would neglect this inherent variability and lead to oversimplified models that may not account for lower or higher-end responders. Therefore, accounting for the S.D. in the analysis improves the predictive fidelity of the simulation, facilitates the design of more robust biosensing systems, and ensures closer alignment with clinically observed biomarker variability.

In contrast, broader statistical intervals such as the 95% (±2 S.D.) or 99.7% (±3 S.D.) rules, though standard in hypothesis testing, are less suitable for defining biosensor detection ranges, particularly at low concentration regimes. For instance, applying the ±3 S.D. rule to healthy p53 values yields a lower bound of –0.05 ng/ml, which lacks physiological validity, as negative concentrations are not permissible in biological systems. This concern is consistent with guidance from the International Union of Pure and Applied Chemistry (IUPAC) Compendium of Analytical Nomenclature, which stipulates that concentration thresholds must correspond to measurable and physically realizable quantities in analytical chemistry [162].

Consequently, in this work, the mean ± 1 S.D. interval is adopted to define the relevant concentration span of p53 for biosensing simulations. This approach maintains biological realism, captures clinical variability, and allows for accurate estimation of the equivalent interface charge densities, which critically influence the electrostatic behavior and sensitivity of the proposed biosensor system. The calculated charge densities corresponding to these concentrations are also listed in Table 4.2.

4.3 OPTIMIZATION AND PERFORMANCE ANALYSIS OF I-JL-NWFET BASED BIOSENSOR

The performance analysis of the proposed I-JL-NWFET based biosensor is carried out using the SILVACO TCAD. The sensing simulations are based on experimental biofunctionalization and detection protocols reported in literature [70], adapted for p53 detection. The target analyte is the tumour suppressor protein p53, which carries a net negative charge (−4e). The concentration range investigated (0.11–0.27 ng/mL for healthy persons and 0.44–1.62 ng/mL for diseased persons) corresponds to the equivalent interface charge densities listed in Table 4.2. Considering a dry sensing environment during simulations, the nanocavity without p53 biomolecules is modeled as air (k = 1).

The presence of p53 in the nanocavity is represented by applying the calculated interface charges at the oxide–channel interface using Eqn. 4.1 and assigning a dielectric constant of 3.23 [163], thereby replicating the electrostatic influence of immobilized biomolecules. Unless otherwise stated, the temperature is kept at 300 K. Furthermore, the biomolecular cavity is assumed to be fully occupied in the initial subsections to provide a baseline reference. The effect of partial cavity occupancy is analyzed in the subsequent subsection, followed by the influence of repulsive steric hindrance during biomolecule immobilization, addressing practical deviations from the ideal case.

4.3.1 Optimization of I-JL-NWFET based Biosensor

To determine the optimal cavity length (L_{cav}) and cavity side (Source/Drain side) for sensing applications, I-JL-NWFET based biosensor is examined through I_{ON}/I_{OFF} and I_{ON}/I_{OFF} sensitivity. The I_{ON}/I_{OFF} ratio indicates how effectively a device can switch between the OFF-state (V_{GS} = 0) and the ON-state (V_{GS} = 1 V). The dependence of L_{cav} on the I_{ON}/I_{OFF} ratio when the nanocavity is created on the source and drain sides is portrayed in Fig. 4.4 (a) and (b), respectively. In both cases, the I_{ON}/I_{OFF} ratio is consistently higher for the diseased p53 serum concentration range compared to the healthy case. This enhancement is attributed to the

increased negative equivalent interface charge associated with the diseased p53 concentration, which strengthens the electrostatic repulsion of residual channel electrons during the OFF-state, thereby reducing I_{OFF} and enhancing the I_{ON}/I_{OFF} switching ratio.

In Fig. 4.4 (a), as L_{cav} increases from the source side, the I_{ON}/I_{OFF} ratio improves, indicating stronger modulation of the source-side barrier or improved channel control. However, this improvement saturates as L_{cav} extends towards the M_2 gate, suggesting diminishing marginal electrostatic influence. In contrast, Fig. 4.4 (b) shows that increasing L_{cav} from the drain side has little effect until the cavity reaches under the M_1 gate. There, a noticeable increase in I_{ON}/I_{OFF} is observed, which is attributed to the higher work function of M_1. This enhances gate control and more effectively suppresses I_{OFF}, thereby improving the switching behavior.

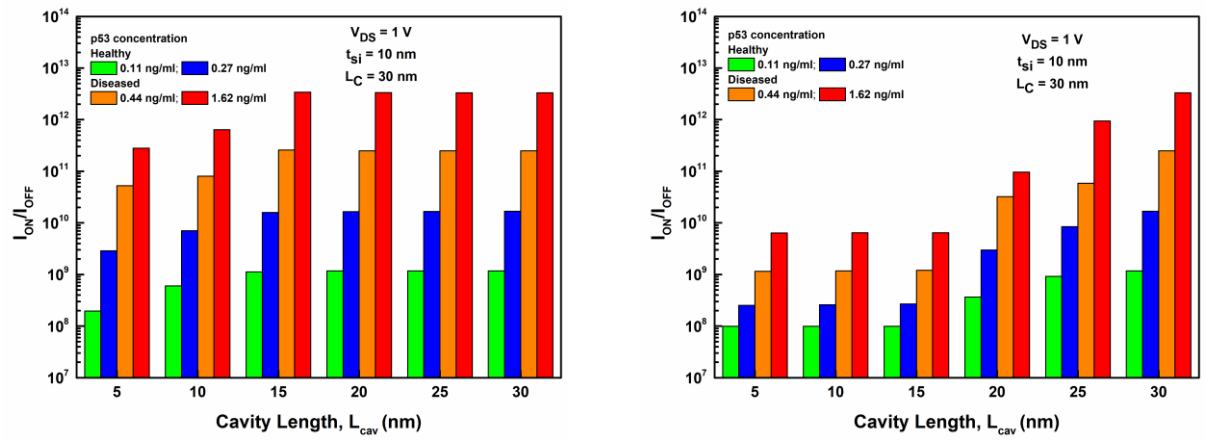


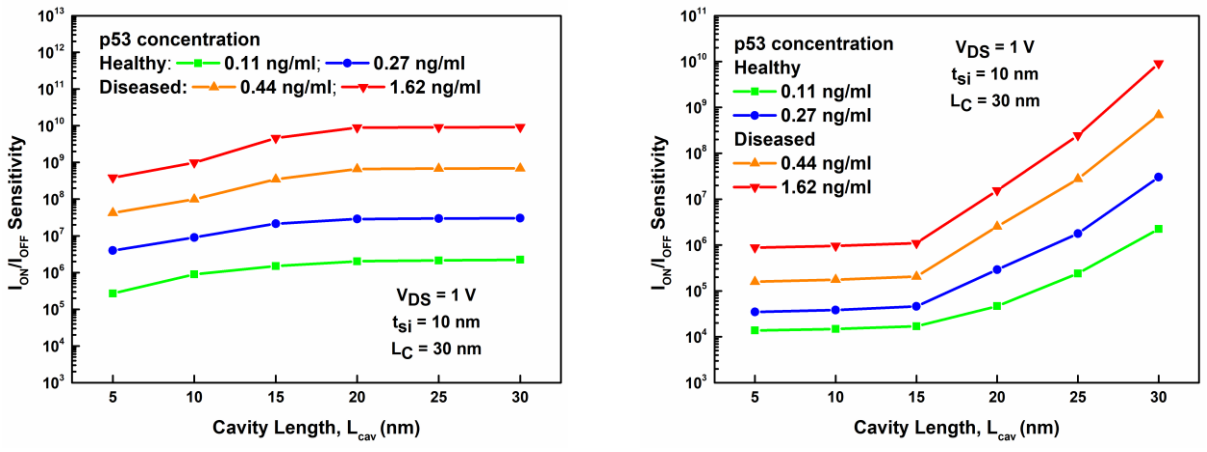
Fig. 4.4 Variation of the I_{ON}/I_{OFF} ratio for different cavity lengths when the cavity is at (a) source side and (b) drain side, illustrating the influence of cavity length on the I_{ON}/I_{OFF} ratio

The sensitivity of a biosensor generally refers to its ability to detect small changes in analyte concentration and produce a measurable response. The I_{ON}/I_{OFF} sensitivity is defined as [63]

$$I_{ON}/I_{OFF}\,Sensitivity = \frac{I_{ON}/I_{OFF}|_{bio}}{I_{ON}/I_{OFF}|_{air}} \tag{4.2}$$

here, $I_{ON}/I_{OFF}|_{bio}$ and $I_{ON}/I_{OFF}|_{air}$ denote the switching ratio on the presence and absence of p53 biomolecules, respectively. As observed from Fig. 4.5 (a) and (b), the I_{ON}/I_{OFF} sensitivity follows the same trend as that of the I_{ON}/I_{OFF} ratio in Fig. 4.4 (a) and (b). When comparing nanocavity placement, the sensitivity is consistently higher when the cavity is positioned at the source side rather than the drain side at any given L_{cav}. At L_{cav} of 15 nm on the source side, the I_{ON}/I_{OFF} sensitivity reaches 4.60×10^9 for diseased and 2.15×10^7, corresponding to the maximum range of diseased and healthy p53 concentrations, respectively (Fig. 4.5 (a)). These

values are over three orders of magnitude higher than the drain-side values (Fig. 4.5 (b)). This quantitative enhancement is attributed to stronger gate control and improved modulation of the tunneling window when the cavity extends under the M_1 gate, effectively suppressing I_{OFF}.



(a) (b)

Fig. 4.5 The I_{ON}/I_{OFF} sensitivity for different cavity lengths when the cavity is at (a) source side and (b) drain side, showing the influence of cavity length and position on sensing performance

The enlarged electrostatic influence at the source side also enhances the modulation of the BTBT window, which further strengthens the biomolecule-induced sensitivity. The I_{ON}/I_{OFF} sensitivity becomes identical when L_{cav} equals the L_C, irrespective of cavity position (Source/Drain). These results clearly indicate that the optimal design for the I-JL-NWFET based biosensor involves placing the nanocavity on the source side, specifically under the M_1 region, with a L_{cav} equal to 50% of the total L_C, corresponding to an aspect ratio (L_{cav}/L_C) of 0.5. These results confirm that source-side placement with optimized L_{cav} maximizes sensitivity by combining enhanced gate–channel electrostatics with stronger BTBT window control and biomolecule-induced charge modulation.

4.3.2 Performance Analysis of the Optimized I-JL-NWFET based Biosensor

This subsection presents a comprehensive evaluation of the electrostatic performance of the optimized I-JL-NWFET based biosensor with L_{cav} of 15 nm with a nanocavity at the source side. The analysis focuses on key device characteristics such as transfer behavior, sensitivity analysis, and electrostatic response under varying biomarker concentrations, specifically targeting the tumour suppressor protein p53.

Fig. 4.6 illustrates the transfer characteristics of the I-JL-NWFET based biosensor for various concentrations of p53 serum proteins, comparing the response between healthy and diseased individuals. The influence of p53 concentration, modeled as an equivalent negative interface

charge, is most pronounced in the subthreshold region. The accumulation of negative charges at the gate dielectric/channel interface electrostatically repels electrons in the uniformly doped n-type channel, thereby enhancing depletion and increasing the potential barrier for carrier injection.

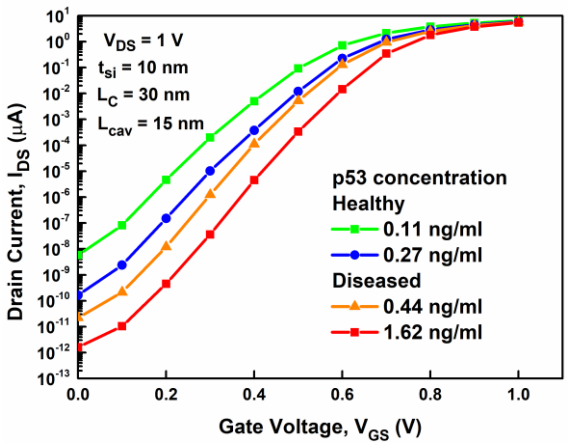


Fig. 4.6 Transfer characteristics for different p53 serum concentrations for varying concentrations of p53 protein, comparing the response for healthy and diseased individuals

Since both the minimum and maximum p53 concentrations in diseased individuals are higher than those in healthy subjects, the corresponding increase in equivalent negative interface charge leads to a greater suppression of the I_{OFF}. This occurs due to the widened energy barrier for BTBT, which significantly reduces BTBT-induced leakage. In contrast, the negative interface charge associated with diseased p53 concentration leads to a reduction in I_{ON} however, this effect is comparatively minimal. This is because the strong gate overdrive in the ON-state effectively re-establishes channel conduction by lowering the potential barrier, thereby partially compensating for the repulsive effect of the additional negative interface charge.

The V_T sensitivity and SS sensitivity for healthy and diseased p53 concentrations are depicted in Fig. 4.7 (a) and (b), respectively. The V_T sensitivity [63] and SS sensitivity [164] are given as

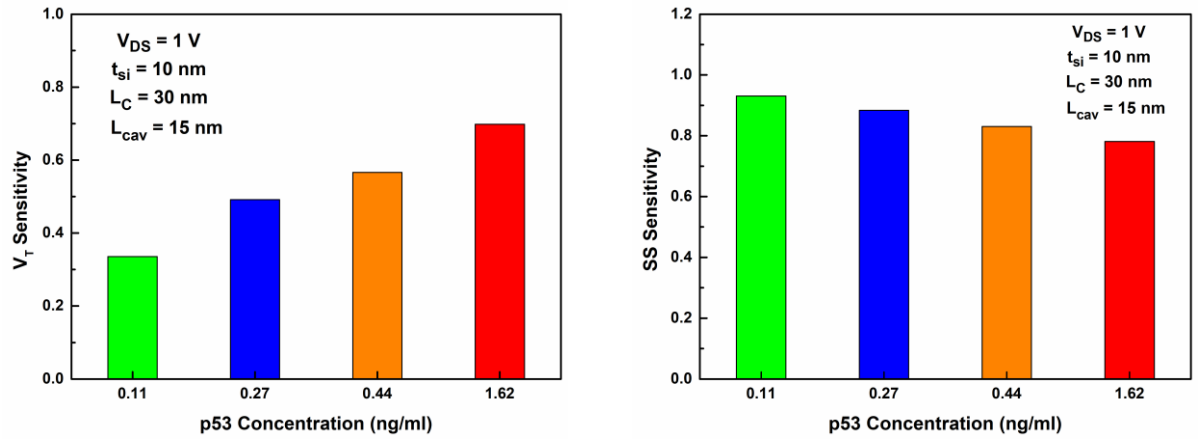
$$V_T Sensitivity = \frac{V_T|_{bio} - V_T|_{air}}{V_T|_{air}} \tag{4.3}$$

$$SSsensitivity = \frac{SS|_{bio}}{SS|_{air}} \tag{4.4}$$

Here, $V_T|_{bio}$, $V_T|_{air}$, $SS|_{bio}$, and $SS|_{air}$ denote V_T and SS of the device in the presence of immobilized p53 biomolecules and in the absence of biomolecules (air-filled cavity), respectively. The presence of negative interface charge modifies the effective flat-band voltage (V_{fb}') and is given as [165]

$$V_{fb}^{'} = V_{fb} - \frac{qN_f}{C_{ox}} \tag{4.5}$$

where V_{fb}, q, N_f, and C_{ox} denote flat band voltage in the absence of interface charge, elementary charge, density of interface charge per unit area, and gate oxide capacitance per unit area, respectively.



(a) (b)

Fig. 4.7 (a) V_T sensitivity and (b) SS sensitivity for healthy and diseased p53 concentrations, demonstrating the device's ability to differentiate disease states

In junctionless transistors, the V_T is strongly dependent on V_{fb}', therefore, an increase in V_{fb}' due to negative interface charges lead to a higher V_T. As a result, V_T sensitivity for a healthy individual lies within the range of 0.33 to 0.49, and increases to 0.56 to 0.69 with elevated p53 concentrations corresponding to the diseased state, as illustrated in Fig. 4.7 (a). Conversely, SS sensitivity decreases with increasing p53 concentration from healthy to diseased conditions as observed in Fig. 4.7 (b). Specifically, the SS sensitivity ranges from 0.93 to 0.88 in healthy individuals and further declines to 0.83 to 0.78 in the diseased state.

This is attributed to a reduction in SS at higher (more negative) p53 concentrations, which arises from a corresponding decrease in I_{OFF}. Since SS is directly influenced by I_{OFF}, lower I_{OFF} in the diseased state leads to improved SS but diminished SS sensitivity compared to the healthy state. Table 4.3 presents the $V_T|_{bio}$, $SS|_{bio}$, V_T sensitivity, and SS sensitivity for healthy and diseased p53 concentrations. The results show that $V_T|_{bio}$ increases and $SS|_{bio}$ decreases with increasing biomolecule concentration. The decrease in $SS|_{bio}$ in the diseased state leads to sharper switching and higher sensitivity, thereby confirming the benefit of low SS in enhancing biosensor performance.

Table 4.3. Comparison of $V_T|_{bio}$, SS$|_{bio}$, V_T sensitivity, SS sensitivity for a range of p53 concentrations of healthy and diseased persons

Parameters	p53 Concentration			
	Healthy		Diseased	
	0.11 ng/ml (Min.)	0.27 ng/ml (Max.)	0.44 ng/ml (Min.)	1.62 ng/ml (Max.)
$V_T\|_{bio}$	0.45	0.50	0.53	0.57
V_T Sensitivity	0.33	0.49	0.56	0.69
SS$|_{bio}$	69.77	66.02	62.27	58.52
SS Sensitivity	0.93	0.88	0.83	0.78

Figure 4.8 (a) and (b) illustrate the surface potential ($\phi_S(z)$) along the device length in the OFF-state and the ON-state, respectively, for different p53 serum concentrations corresponding to healthy and diseased individuals. The surface potential was extracted from a horizontal cut-line positioned 1 nm below the oxide–semiconductor interface in TCAD simulations. Notably, since the nanocavity is confined to the M_1 region, constituting only half the total L_C, the influence of p53-induced interfacial charge modulation is primarily localized within this region.

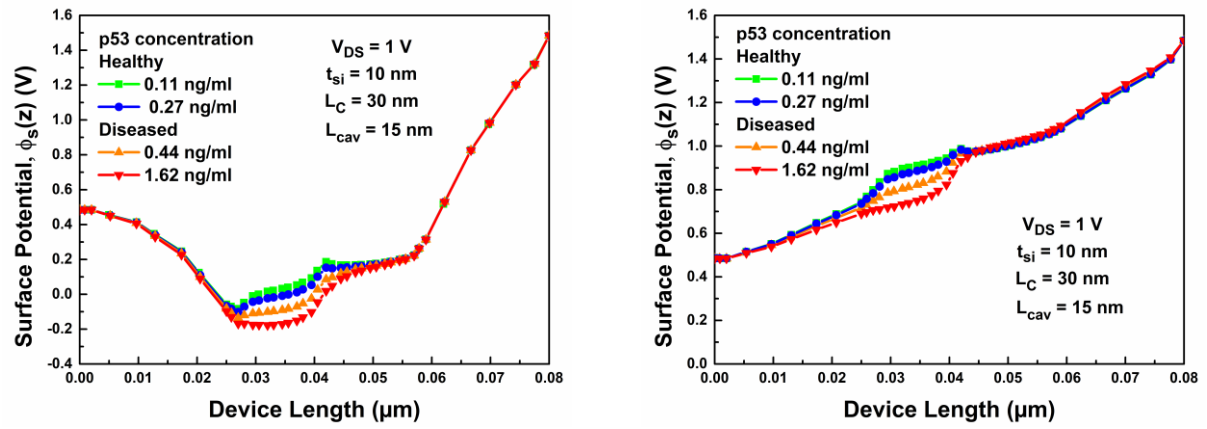


Fig. 4.8 Surface potential ($\phi_S(z)$) profile of I-JL-NWFET based biosensor along device length for different p53 serum concentrations, comparing healthy and diseased conditions at (a) OFF-state and (b) ON-state

It is evident from both Fig. 4.8 (a) and (b) that increasing p53 concentration in diseased conditions results in a downward shift of $\phi_S(z)$, attributable to the accumulation of additional negative charge at the oxide–semiconductor interface. This excess negative charge induces stronger electrostatic repulsion, depleting carriers in the underlying channel region. The downward shift is more pronounced in the OFF-state due to the inherently low carrier density, which limits the screening of vertical gate fields. Consequently, this enhances gate control, further suppresses channel potential, and leads to a reduction in I_{OFF} compared to that under healthy p53 levels, as already observed in Fig. 4.8.

In contrast, during the ON-state, the higher carrier density partially screens the gate field, resulting in a less prominent shift in $\phi_S(z)$. Furthermore, a distinct step-change in $\phi_S(z)$ is observed at the M_1–M_2 interface in both Fig. 4.8 (a) and (b), arising from the work function difference introduced by the DMG architecture, which sharpens electrostatic control and enhances carrier transport efficiency in the shell region. Moreover, the DMG configuration helps to suppress the formation of highly energetic "hot carriers" that typically arise from high electric fields near the drain, thereby improving device reliability against HCEs [11].

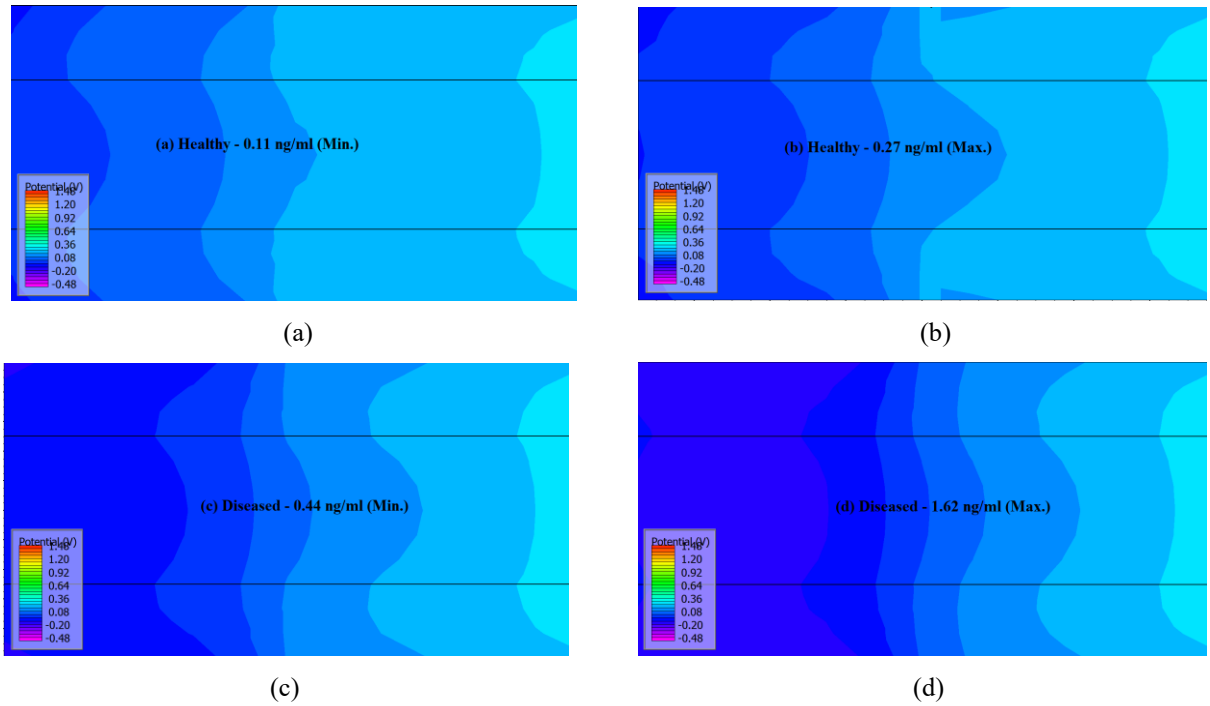
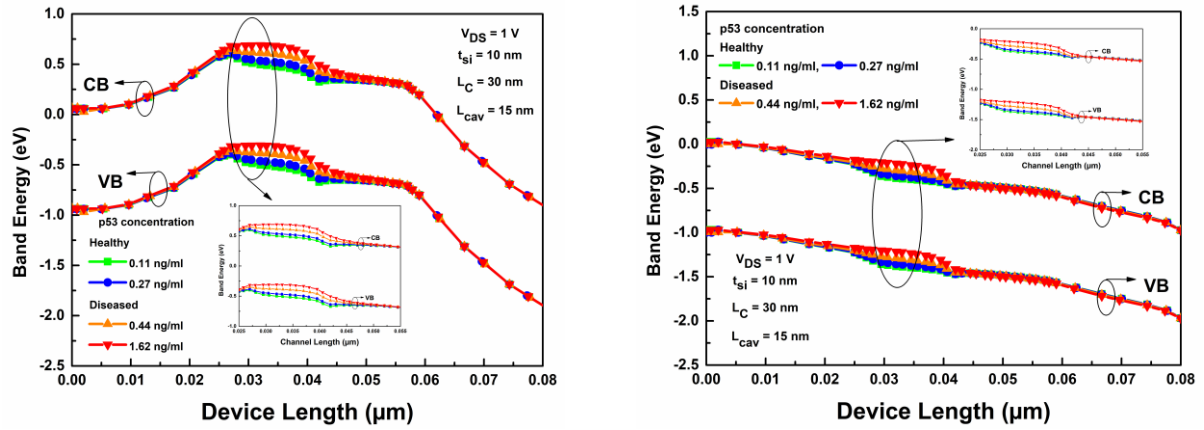


Fig. 4.9 Potential contour for p53 concentration for (a) healthy 0.11 ng/ml (Min.), (b) healthy 0.27 ng/ml (Max.), (c) diseased 0.44 ng/ml (Min.), and (d) diseased 1.62 ng/ml (Max.)

Figures 4.9 (a), (b), (c), and (d) show the potential distribution contours for the different concentrations of the p53 biomarker of healthy and diseased persons in the OFF-state. It is evident from these contours that the potential distribution in the channel region is significantly reduced as the p53 concentration increases, which leads to a reduction in I_{OFF} for higher p53 concentrations, which increases I_{ON}/I_{OFF} sensitivity.

The band energy profile along the I-JL-NWFET based biosensor length for varying serum concentrations of the p53 protein for healthy and diseased persons in the OFF-state and ON-state are presented in Fig. 4.10 (a) and (b), respectively. It is observed from both Fig. 4.10 (a) and (b) that when healthy and diseased p53 protein concentration equivalent negative interface charges are introduced, it affects the energy band profile predominantly within the M_1 region,

where the nanocavity is located. In the OFF-state, the channel is fully depleted due to the absence of gate-induced inversion, and the addition of negative interfacial charge further enhances the electrostatic potential barrier.



(a) (b)

Fig. 4.10 Band energy profile of I-JL-NWFET based biosensor along device length for different p53 serum concentrations for healthy and diseased persons at (a) OFF-state and (b) ON-state

This is reflected in the energy band diagram by an upward shift of both the CB and VB under the M_1 region only. The increased upward band bending deepens the energy barrier for electron conduction, thereby suppressing I_{OFF}. In the ON-state, a strong gate overdrive lowers the CB and VB across the channel to allow carrier accumulation and establish conduction. However, the p53 concentration equivalent charges under the M_1 region partially counteract this gate-induced band modulation. As a result, the CB and VB remain slightly elevated in this region, leading to a marginal reduction in I_{ON}. This effect becomes more apparent with increasing p53 concentration, although the overall impact on I_{ON} remains limited due to the dominant influence of the gate field in the ON-state. This trend is consistent with the transfer characteristics shown in Fig. 4.6.

4.3.3 Impact of Core Thickness on the Sensitivity of the I-JL-NWFET based Biosensor

This subsection examines the impact of t_{core} on I_{ON}/I_{OFF} ratio, V_T, and SS sensitivity of the I-JL-NWFET based biosensor. As a fundamental structural parameter in core-shell architecture, the t_{core} plays a pivotal role in determining gate control over the channel, influencing electrostatic integrity and charge carrier modulation. Variations in t_{core} affect the potential distribution across the device, thereby altering its sensitivity to biomolecular interactions at the sensing surface and directly impacting overall biosensor performance.

Figures 4.11 (a), (b), and (c) demonstrate V_T, I_{ON}/I_{OFF} ratio, and SS sensitivity, respectively, with respect to variations in t_{core} for p53 concentration corresponding to healthy and diseased

individuals. As shown in Fig. 4.11 (a), the V_T sensitivity increases with an increase in t_{core} from 1 nm to 7 nm for both healthy and diseased p53 concentrations. This behavior can be attributed to enhanced volume depletion in the oppositely doped core region. A thicker t_{core} increases the depletion effect, necessitating a higher V_{GS} to initiate conduction in the channel, thereby increasing the V_T. Consequently, the variation in V_T due to p53 equivalent interface charge becomes more pronounced, resulting in greater V_T sensitivity.

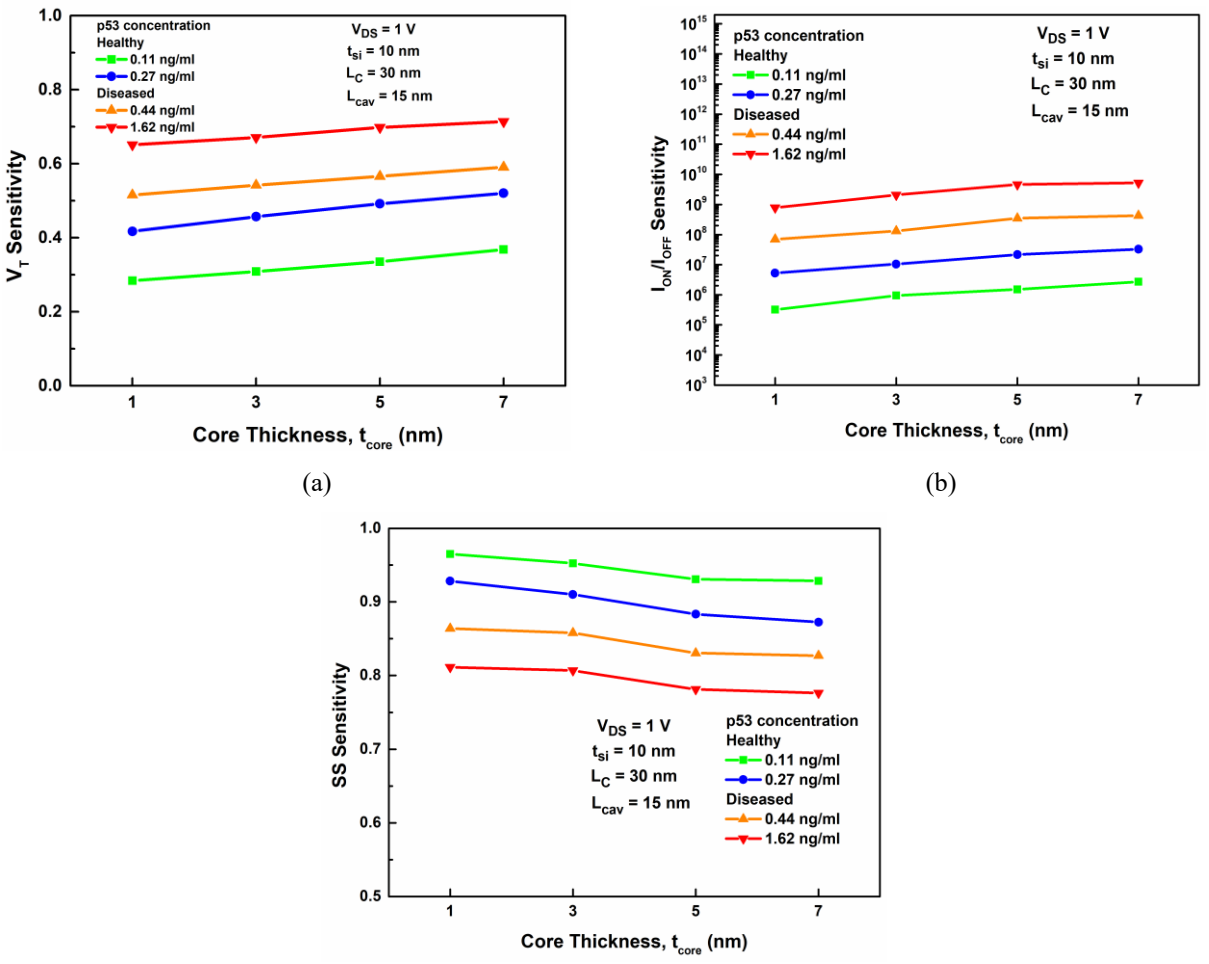


Fig. 4.11 Variation of (a) V_T sensitivity, (b) I_{ON}/I_{OFF} sensitivity, and (c) SS sensitivity on varying core thickness for healthy and diseased p53 concentrations, emphasizing the impact of structural scaling

Additionally, for a fixed t_{core}, the diseased state characterized by a higher p53 concentration exhibits greater V_T sensitivity than the healthy state. This is due to the presence of a larger amount of equivalent negative interface charge, which further elevates V_T by increasing the electrostatic barrier to channel conduction. Fig. 4.11 (b) depicts that I_{ON}/I_{OFF} sensitivity increases with increasing t_{core} at any given p53 concentration. This trend is primarily attributed to a reduction in I_{OFF}, as a thicker core enhances volume depletion within the channel, thereby improving the $I_{ON}/I_{OFF}|_{bio}$ compared to the air-filled cavity. Consequently, the I_{ON}/I_{OFF}

sensitivity is elevated. Furthermore, for a fixed t_{core}, a higher p53 concentration within the cavity leads to a greater accumulation of negative interface charges.

This intensifies the depletion effect and further suppresses I_{OFF}, thereby enhancing the I_{ON}/I_{OFF} sensitivity, as already discussed in Fig. 4.8 (a). As shown in Fig. 4.11 (c), at a given t_{core}, the SS sensitivity is lower for the diseased sample compared to the healthy one. This is due to the fact that the higher negative equivalent interfacial charge associated with elevated p53 concentrations suppresses I_{OFF}, thereby decreasing $SS|_{bio}$ and consequently the SS sensitivity. Additionally, at a fixed p53 concentration, increasing t_{core} further reduces SS sensitivity, as the thicker core enhances volume depletion, leading to a lower I_{OFF} and thus a reduced $SS|_{bio}$ relative to the absence of p53 biomolecules. Beyond a t_{core} of 5 nm, the changes in I_{ON}/I_{OFF} and SS sensitivity become minimal, indicating saturation in performance improvement.

4.3.4 Impact of Channel Length on the Sensitivity of the I-JL-NWFET based Biosensor

The impact of L_C on V_T, I_{ON}/I_{OFF}, and SS sensitivity of the I-JL-NWFET based biosensor is investigated in this subsection. Understanding the L_C dependent electrical behavior provides insight into the device's ability to reliably detect biomolecular interactions at varying concentrations, which is essential for practical biomedical sensing applications. The V_T, I_{ON}/I_{OFF}, and SS sensitivity with respect to variations in Lc for p53 concentration corresponding to healthy and diseased individuals are illustrated in Figs 4.12 (a), (b), and (c), respectively.

As the L_C decreases, the V_T shift ($V_T|_{bio} - V_T|_{air}$) increases at a given p53 concentration as illustrated in Fig. 4.12 (a). This is due to stronger gate control and enhanced influence of biomolecule equivalent charge on the shorter L_C. This larger shift raises the overall V_T sensitivity in the presence of p53 biomolecules. In Fig. 4.12 (b), I_{ON}/I_{OFF} sensitivity decreases as L_C decreases at fixed p53 concentration. This reduction is primarily due to an increase in I_{OFF} resulting from SCEs in shorter L_C. Moreover, the higher negative equivalent interface charge present in diseased samples more effectively suppresses I_{OFF} compared to the healthy case, resulting in relatively lower I_{OFF} and an increase in I_{ON}/I_{OFF} sensitivity in the diseased condition at a given L_C. On the contrary, in Fig. 4.12 (c), the SS sensitivity increases with decreasing L_C at fixed p53 concentration. This is due to the SCEs induced increase in I_{OFF}, which elevates the SS under biomolecular influence.

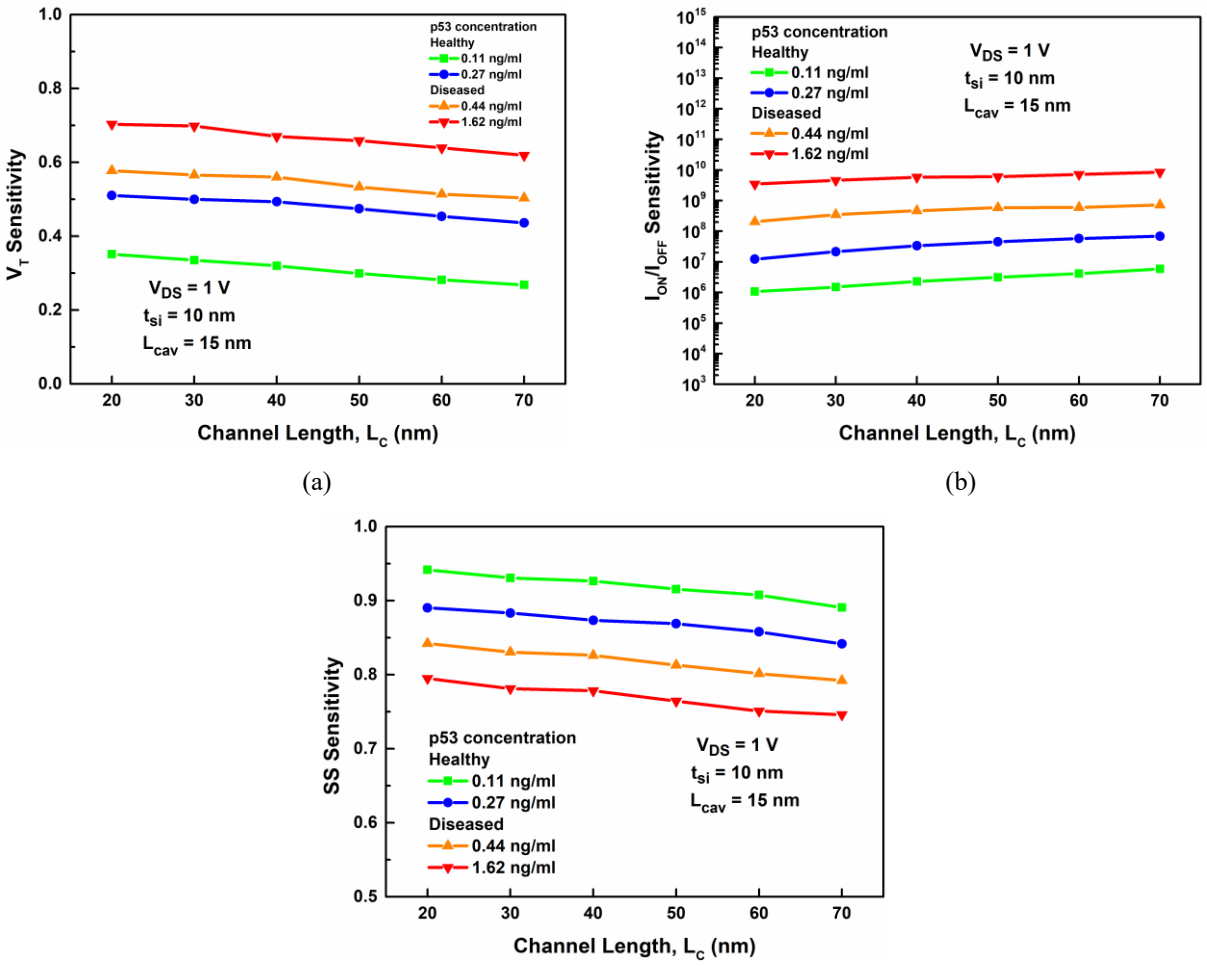


Fig. 4.12 Influence of channel length on (a) V_T sensitivity, (b) I_{ON}/I_{OFF} sensitivity, and (c) SS sensitivity for healthy and diseased p53 concentrations

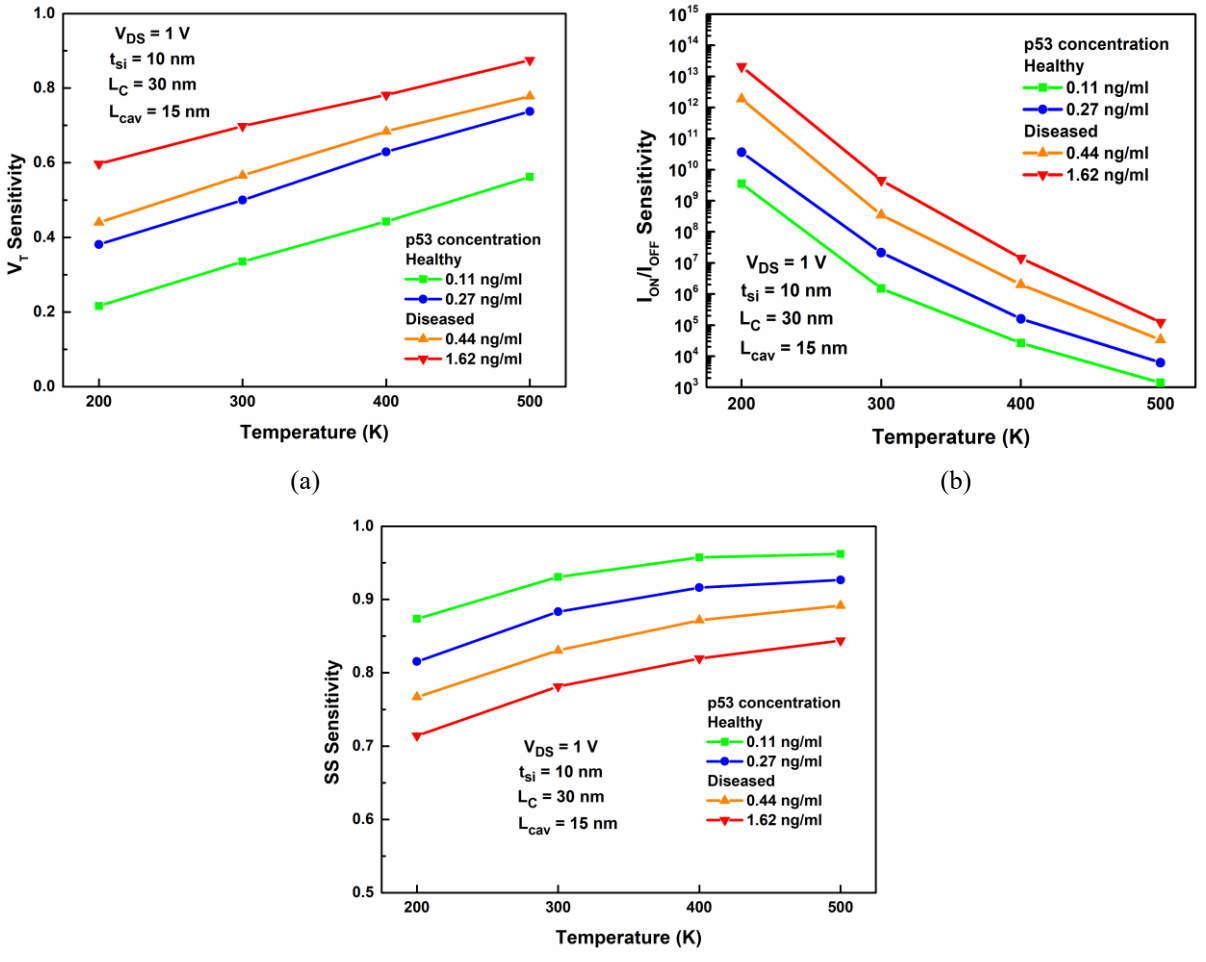
However, at a given L_C, higher concentrations of p53 (associated with diseased conditions) introduce more negative interface charge, which suppresses I_{OFF}, thereby reducing $SS|_{bio}$ and leading to a decrease in SS sensitivity.

4.3.5 Effect of Temperature on the Sensitivity of the I-JL-NWFET based Biosensor

This subsection presents a detailed analysis of how temperature variations (from 200 K to 500 K) influence the sensitivity metrics of the I-JL-NWFET based biosensor, thereby evaluating its operational stability and applicability in practical biomedical scenarios. Comprehending the temperature-dependent behavior of the biosensor response is crucial for achieving consistent performance under diverse physiological and environmental conditions. The temperature-dependent analysis extending up to 500 K is not intended to represent realistic biosensing conditions but rather to evaluate the device's electrical robustness under extreme scenarios. Such boundary simulations are common in device physics to assess performance limits,

reliability, and carrier transport mechanisms. This extended range ensures that the model remains consistent with semiconductor physics, while practical biosensing would still operate under physiological temperatures, where biomolecules are stable.

Figures 4.13 (a), (b), and (c) illustrate the variations in V_T, I_{ON}/I_{OFF}, and SS sensitivity, respectively, as a function of temperature for p53 concentrations corresponding to healthy and diseased conditions. As shown in Fig. 4.13 (a), V_T sensitivity increases with rising temperature at a given p53 concentration. This behavior is attributed to the reduction in electron mobility with temperature, leading to an increase in V_T in both healthy and diseased cases. In junctionless transistors, phonon scattering is the dominant mobility degradation mechanism, and its effect follows a $T^{-3/2}$ dependence [117].



(a) (b)

(c)

Fig. 4.13 Effect of operating temperature variation on (a) V_T sensitivity, (b) I_{ON}/I_{OFF} sensitivity, and (c) SS for healthy and diseased p53 concentrations

The I_{ON}/I_{OFF} sensitivity, shown in Fig. 4.13 (b), decreases with increasing temperature from 200 K to 500 K at fixed p53 levels. This trend is primarily due to the rise in I_{OFF}, which is driven by the temperature-dependent increase in intrinsic carrier concentration (n_i), which is

given by Eqn. 1.16. Conversely, SS sensitivity decreases with increasing temperature, as shown in Fig. 4.13 (c), due to the corresponding rise in I_{OFF}, which degrades SS response.

4.3.6 Effect of Cavity Occupancy on the Sensitivity of the I-JL-NWFET based Biosensor

This subsection investigates the effect of varying cavity occupancy on V_T, I_{ON}/I_{OFF}, and SS sensitivity under both healthy and diseased p53 biomarker concentrations. Understanding these dependencies is essential for optimizing I-JL-NWFET based biosensor performance under partial or incomplete molecular binding conditions, which are often encountered in real-world diagnostic scenarios.

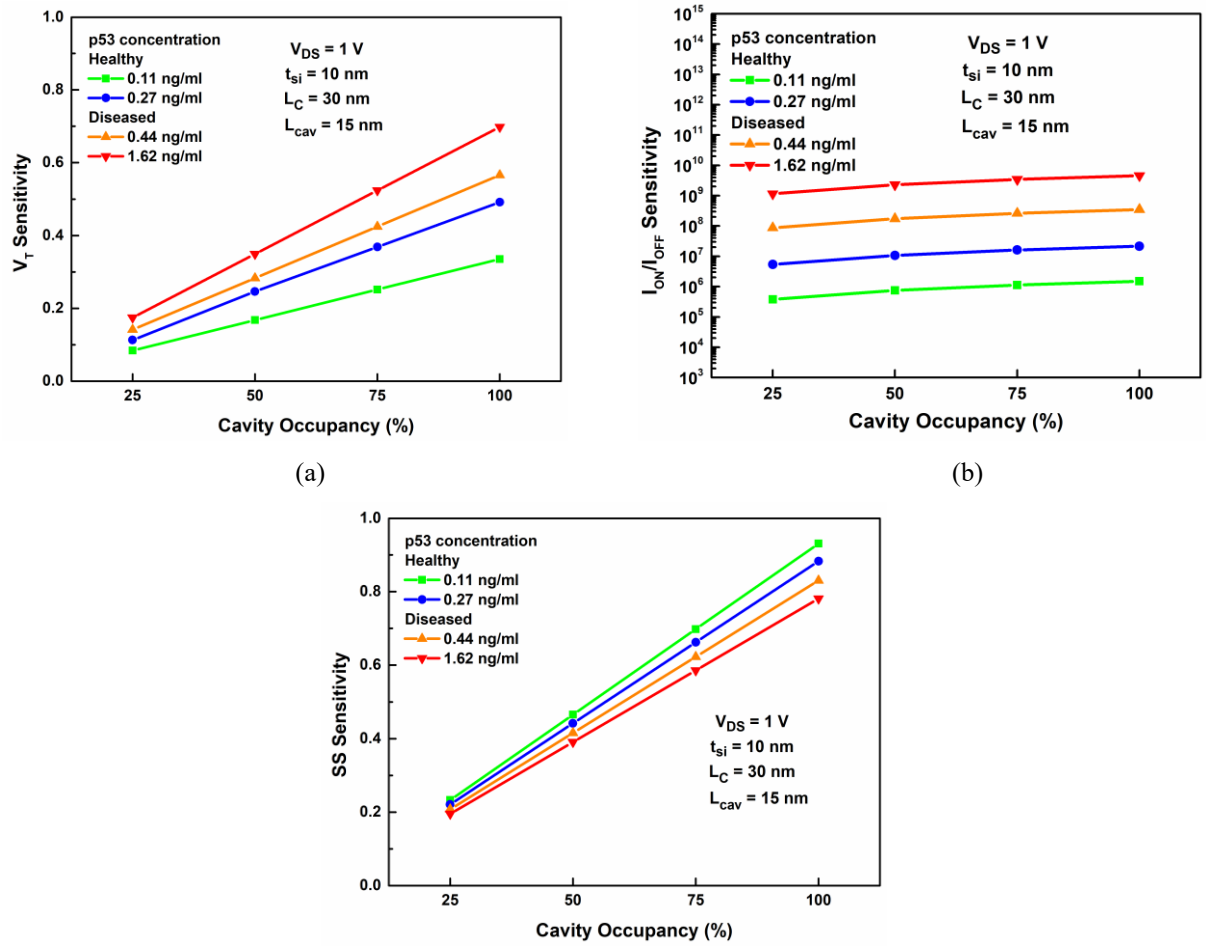


Fig. 4.14 Influence of nanocavity occupancy ratio on (a) V_T sensitivity, (b) I_{ON}/I_{OFF} sensitivity, and (c) SS sensitivity, comparing performance for healthy and diseased p53 concentrations

The V_T, I_{ON}/I_{OFF}, and SS sensitivity with respect to variations in cavity occupancy for p53 concentration corresponding to healthy and diseased individuals are illustrated in Figs. 4.14 (a), (b), and (c), respectively. As cavity occupancy decreases from 100% to 25%, a notable reduction is observed in the sensitivity of V_T, I_{ON}/I_{OFF}, and SS in the I-JL-NWFET based biosensor. This behavior can be attributed to the diminished presence of biomolecular charge

within the sensing cavity, which leads to weaker electrostatic modulation of the channel potential. Specifically, V_T sensitivity in Fig. 4.14 (a) decreases due to a lower net surface charge, which reduces the shift in channel threshold behavior at a given p53 biomarker concentration.

Similarly, the I_{ON}/I_{OFF} sensitivity declines with reduced cavity occupancy as shown in Fig. 4.14 (b), as the smaller biomolecular influence results in less pronounced variation between the ON-state and OFF-state currents. In Fig. 4.14 (c), SS sensitivity also degrades on decreasing cavity filling, since the limited interface charge fails to significantly perturb the subthreshold conduction characteristics. These observations highlight the importance of maximizing cavity occupancy to ensure optimal biosensor performance, particularly in scenarios involving low analyte availability or incomplete molecular capture.

4.3.7 Effect of Repulsive Steric Hindrance on the Sensitivity of the I-JL-NWFET based Biosensor

This subsection investigates the effect of Repulsive Steric Hindrance (RSH) on the sensitivity of the proposed I-JL-NWFET based biosensor. The Repulsive Steric Effect (RSE) arises mainly from interactions between non-bonded atoms or valence electrons, which generate intermolecular repulsion [166]. The Steric Effect (SE) restricts the additional entrance of biomolecules into the sensing cavity and lowers the binding rate of biomolecules with the reaction surface. Moreover, RSE prevents the placement of similar biomolecules in close proximity, thereby requiring adequate spacing between capturing strands depending on biomolecule size.

To account for this phenomenon, the cavity architecture is modified by introducing non-uniform step arrangements with inter-molecular gaps, ensuring a minimum separation of ~5 nm between biomolecules to realistically emulate steric repulsion and minimize unfavourable interactions [167]. By integrating these considerations, the analysis provides a more practical and accurate estimation of the biosensor's sensitivity under steric hindrance-limited conditions. The effect of RSH on the sensitivity parameters of the I-JL-NWFET based biosensor is depicted in Figs. 4.15 (a), (b), and (c) for V_T, I_{ON}/I_{OFF}, and SS sensitivities, respectively, under healthy and diseased p53 concentrations.

When RSH is considered, the V_T sensitivity in Fig. 4.15 (a) decreases because Steric Hindrance (SH) enforces a minimum separation of ~5 nm between biomolecules inside the cavity. This spacing reduces the effective density of immobilized p53 biomolecules, and consequently the equivalent negative charge induced at the gate interface, leading to weaker charge modulation

and a smaller V_T shift. Similarly, the I_{ON}/I_{OFF} sensitivity in Fig. 4.15 (b) decreases since the reduced biomolecule density and spatial constraints increase I_{OFF} current, thereby lowering the I_{ON}/I_{OFF} ratio.

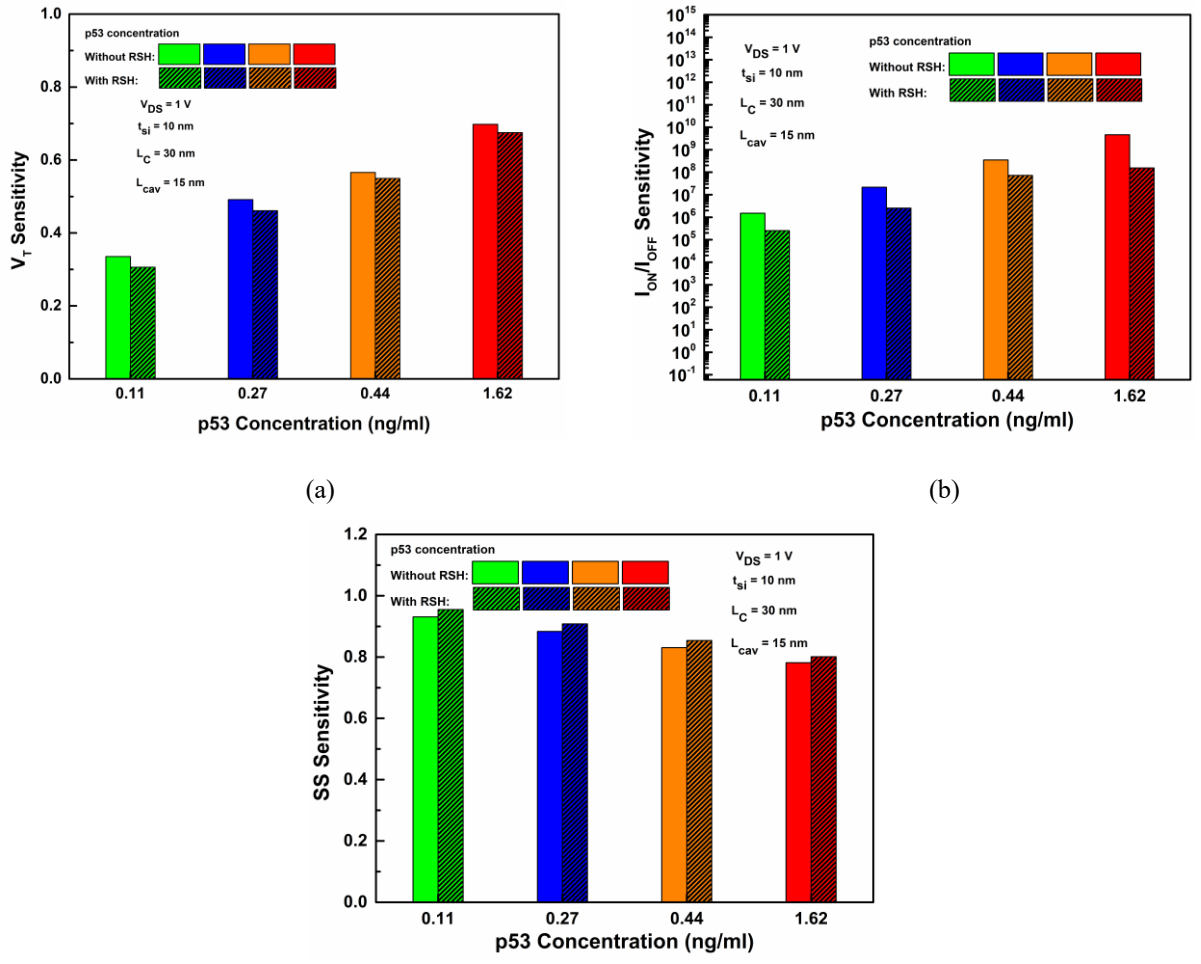


Fig. 4.15 Assessment of repulsive steric hindrance on (a) V_T sensitivity, (b) I_{ON}/I_{OFF} sensitivity, and (c) SS sensitivity for healthy and diseased p53 concentrations

In contrast, the SS sensitivity in Fig. 4.15 (c) increases under RSH, as the rise in I_{OFF} enhances the subthreshold slope of the biomolecule-filled cavity compared to the air-filled reference, resulting in higher SS sensitivity. Overall, RSH degrades V_T and I_{ON}/I_{OFF} sensitivities but improves SS sensitivity compared to the ideal theoretical case of a fully filled cavity, highlighting the necessity of incorporating RSE for a realistic evaluation of biosensor performance. Table 4.4 summarizes the sensitivity error (S_E), where previously published structures that employed SE for sensitivity calculations exhibited inaccuracies of approximately 14%-21%. To address this, the proposed RSH approach is applied and evaluated with respect to the steric SH considerations reported in earlier studies.

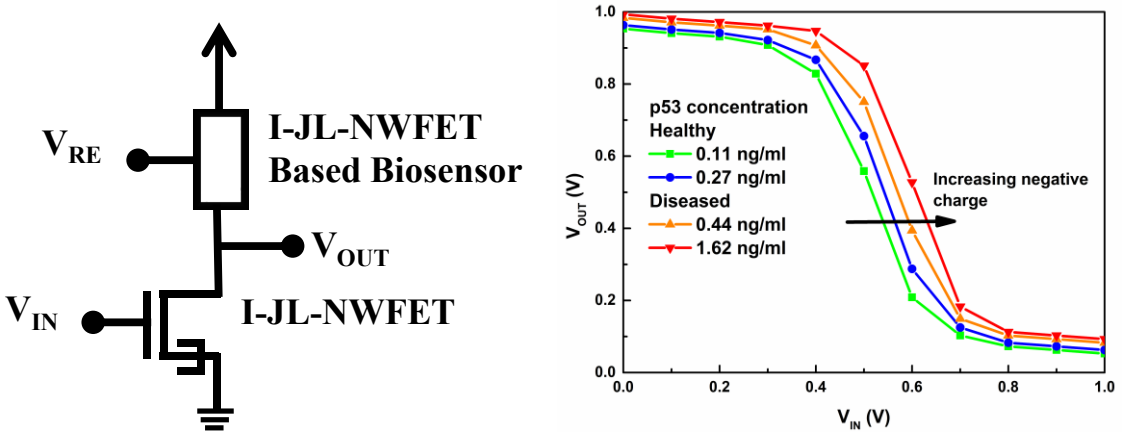
Table 4.4. Sensitivity Error Evaluation in SH and RSH Approach

Reference	Sensitivity		S_E (%)
	S_{SE}	S_{RSE}	
[63]	2.9×10^8	1.54×10^7	19%
[166]	-	-	21%
[167]	6×10^8	5.25×10^9	14%
This work	1.84×10^8	1.55×10^8	18%

The sensitivity error is defined as $S_E(\%) = \left(\frac{S_{RSE} \sim S_{SE}}{S_{RSE}}\right) \times 100$, where S_{RSE} represents the sensitivity obtained using the RSH approach and S_{SE} denotes the SE considering sensitivity [167]. These findings clearly highlight that replacing SE with RSE yields a more accurate and consistent sensitivity evaluation. Therefore, the incorporation of RSE in both the design and analysis stages is necessary to ensure realistic and practically realizable biosensor performance.

4.3.8 Read-Out Circuitry for Biomolecule Detection

To enable practical sensing, a Common Source Amplifier (CSA) is employed as the voltage read-out circuit, as also reported in [63]. The proposed I-JL-NWFET-based biosensor is integrated into the CSA configuration utilizing the I-JL-NWFET, as shown in Fig. 4.16 (a). The I-JL-NWFET is analyzed in Chapter 1, whereas the I-JL-NWFET-based biosensor is introduced in the present Chapter. In the circuit, the proposed biosensor transistor acts as the input device whose electrical characteristics are modulated by the binding of targeted p53 biomolecules inside the nanocavity region.



(a) (b)

Fig. 4.16 (a) Circuit of the CSA incorporating the I-JL-NWFET-based biosensor. (b) Voltage transfer characteristics of the CSA for the detection of p53 biomolecules

The CSA converts these small biomolecule-induced current variations into measurable output voltage shifts (V_{OUT}), thereby providing a reliable voltage-mode read-out, where the applied input voltage (V_{IN}) serves as the V_{GS}. In this circuitry, the reference electrode voltage (V_{RE})

biases the nanocavity region where the targeted p53 biomolecules bind, thereby establishing a baseline electrostatic potential for charge detection [168]. Fig. 4.16 (b) illustrates the Voltage Transfer Characteristics (VTC) of the CSA for targeted p53 detection. The binding of negatively charged p53 molecules induces a positive shift in the VTC, which raises the effective V_T and produces a corresponding rightward shift in the transfer curve.

This shift alters the device transconductance and leads to a measurable change in the CSA output. These results confirm that the CSA not only amplifies the biosensor response but also preserves its discriminatory capability across clinically relevant biomarker concentrations, highlighting its potential for real-time biomedical applications. The benchmarking study presented in Table 4.5 clearly establishes the superiority of the proposed I-JL-NWFET based biosensor over the existing FET based biosensors such as Dual Material Hetero-Structure Charge-Plasma-based Extended Gate (DCE-H) TFET [63], Heterojunction Dopingless (HJ-DL) TFET [64], , Dual Cavity Dielectric Modulated Nanotube (DCDM NT) [164], and BIOFET [169].

Table 4.5. Performance Benchmarking of the V_T Sensitivity and I_{ON}/I_{OFF} Sensitivity of the Proposed Biosensor

FET based Biosensor	V_T **Sensitivity**	I_{ON}/I_{OFF} **Sensitivity**
DCE-HTFET (L_C = 80 nm , L_{cav} = 35 nm, t_c = 15 nm, biomolecule = HE4) [63]	-	2.8 × 106
HJ-DL-TFET (L_C = 50 nm , L_{cav} = 30 nm, biomolecule = C-erB-2) [64]	-	2.48 × 106
DCDM NTTFET (L_C = 25 nm , L_{cav} = 30 nm, t_c = 10 nm, biomolecule = streptavidin) [164]	0.53	-
BIOFET (L_C = 60 nm , L_{cav} = 45 nm, t_c = 6 nm, biomolecule = protein) [169]	0.44	-
I-JL-NWFET (L_C = 30 nm , L_{cav} = 15 nm, t_c = 10 nm, biomolecule = p53) (This work)	0.69	4.60 × 109

The proposed biosensor exhibits a significantly better V_T sensitivity and I_{ON}/I_{OFF} sensitivity as compared to the previously reported FET-based biosensors. This combined improvement in sensitivity highlights the strong potential of the I-JL-NWFET as a next-generation biosensing platform for highly reliable and selective detection of biomolecules such as p53. The nanoscale dimensions of the proposed biosensor are selected to enhance the surface-to-volume ratio, which is critical for maximizing the modulation of channel conductivity by the bound biomolecules. The selected nanometre dimensions are in line with those reported in recent TCAD-based biosensor studies [63, 64, 164, 169], where scaling improves sensitivity without compromising fabrication feasibility.

4.4 SUMMARY OF THE IMPORTANT RESULTS

The current chapter focuses on the development and analysis of I-JL-NWFET based biosensor for label-free electrical detection of the p53 biomarker, which is an important indicator for GI cancers. The sensing mechanism is based on interface charge deduction, wherein equivalent interfacial charges corresponding to clinically relevant p53 concentrations are introduced into the nanocavity region. This approach enables the device to distinguish effectively between healthy and diseased conditions through variations in the electrical characteristics of I-JL-NWFET based biosensor. The device structure is systematically optimized to achieve enhanced sensitivity and reliable detection performance.

Further, the impact of key design parameters including nanocavity position, L_{cav}, L_C, t_{core}, cavity occupancy, and temperature is investigated to obtain deeper insight into biosensor behaviour. Subsequently, the effect of realistic sensing constraints is also examined by incorporating RSH, which provides a more practical evaluation of sensing performance. Additionally, the integration of the proposed biosensor with CSA read-out circuitry is demonstrated to translate biomolecule-induced current variations into measurable voltage shifts. The important outcomes of the chapter are listed below.

- Firstly, the proposed I-JL-NWFET based biosensor is proposed for label-free electrical detection of the p53 biomarker associated with cholangiocarcinoma which is a bile duct cancer, one of the GI cancers. The sensing principle is based on interface charge deduction through equivalent interfacial charges introduced in the nanocavity region corresponding to clinically relevant biomarker concentrations.
- The optimization analysis reveals that the highest sensitivity is achieved when the nanocavity is positioned near the source side of the channel, while the optimum L_{cav} is found to be half of the L_C.
- Under the optimized device configuration, for a p53 concentration of 1.62 ng/ml corresponding to the maximum diseased condition, the biosensor achieves an I_{ON}/I_{OFF} sensitivity of 4.60×10^9, V_T sensitivity of 0.69, and SS sensitivity of 0.78.
- For a p53 concentration of 0.27 ng/ml corresponding to the maximum healthy condition, the device exhibits an I_{ON}/I_{OFF} sensitivity of 2.15×10^7, V_T sensitivity of 0.49, and SS sensitivity of 0.88.
- The obtained results confirm that the proposed biosensor possesses strong discriminatory capability over clinically relevant biomarker concentrations and can effectively differentiate healthy and diseased states.

- The channel scaling analysis demonstrates that the biosensor retains appreciable sensitivity even at shorter channel lengths, indicating its suitability for highly scaled nanowire biosensor applications.
- The temperature analysis shows that the proposed I-JL-NWFET biosensor remains sensitive over a wide operating temperature range, thereby confirming its robust sensing behaviour under varying thermal conditions.
- The cavity occupancy investigation indicates that maximum sensitivity is obtained at 100% cavity occupancy, emphasizing the importance of complete biomolecular binding within the sensing region.
- The incorporation of RSH effects provides a more realistic assessment of biosensor performance by accounting for steric limitations and practical binding constraints, thereby bridging the gap between idealized simulation and practical operation.
- Furthermore, the integration of the proposed biosensor with CSA read-out circuitry successfully converts biomolecule-induced drain current variations into measurable voltage shifts, thereby demonstrating its potential for practical biomedical sensing applications.

The present chapter demonstrates that the proposed I-JL-NWFET based biosensor offers high sensitivity, excellent discrimination capability, and reliable operation for label-free detection of the p53 biomarker. The combined optimization of structural parameters, consideration of practical sensing effects, and successful read-out circuit integration establish the feasibility of the proposed biosensor for future biomedical diagnostic applications. The further research may focus on experimental validation, fabrication feasibility, and performance assessment in complex biological environments to establish the practical applicability and robustness of the proposed sensing platform.

CHAPTER-5
CMOS INVERTER AND RING OSCILLATOR ANALYSIS USING IMPROVED-JUNCTIONLESS NANOWIRE FET

5.1 INTRODUCTION

The device engineering techniques, as discussed in Chapter 1, are widely used to improve JL-NWFET switching characteristics and mitigate SCEs in deeply scaled technologies. These features make the device particularly suitable for high-speed and low-power digital circuit implementations. In Chapter 4, the applicability of the proposed I-JL-NWFET was demonstrated through biomedical sensing applications. The results established that the same device architecture can be effectively extended beyond sensing platforms toward other emerging application domains. In this context, it becomes important to investigate the suitability of the proposed I-JL-NWFET for electronic circuit applications. Therefore, exploring how such engineered devices behave within CMOS logic elements, particularly inverters, becomes essential for evaluating their suitability for future nanoscale circuit platforms.

The CMOS inverter is the fundamental building block of digital logic, with its delay, noise margins, and switching energy dictating the performance of larger systems [89, 90]. Therefore, analysing its switching behavior is essential for assessing the feasibility of integrating I-JL-NWFET technology into complex circuits, as inverter delay directly influences propagation delays in oscillators, counters, and other timing-critical blocks. To further evaluate the practical applicability of emerging nanoscale devices, the Ring Oscillator (RO) serves as a benchmark circuit because its oscillation frequency reflects device delay, drive strength, and capacitive loading. An RO composed of an odd number of cascaded inverters in a feedback loop exhibits a frequency governed by the propagation delay of each stage [91, 93]. Implementing a RO using I-JL-NWFET based CMOS inverter enables assessment of the combined advantages of CS, DMG, GSS techniques, making the architecture well-suited for low-power and energy-constrained applications.

The following objective is framed to explore the broader applicability of the the proposed I-JL-NWFET for electronics applications:

“Analysis of Electronic Circuit Application using Improved Nanowire FET.”

To realize the desired objective, the methodology includes the following steps: -

- Initially, the device-level analysis is carried out for the proposed I-JLNWFET device to investigate the influence of structural modifications on electrostatic control and leakage suppression and the results are compared with the counterpart devices.
- Subsequently, circuit-level analysis is performed using the MixedMode circuit simulator in SILVACO ATLAS through CMOS inverter implementation using the proposed and counterpart devices. The inverter performance is assessed in terms of voltage transfer characteristics, noise margins, and transient switching behaviour.
- Finally, circuit-level RO analysis is carried out using the MixedMode circuit simulator in SILVACO ATLAS by implementing RO configurations using the corresponding proposed I-JL-NWFET with its counterpart JL-NWFET devices. The performance of I-JL-NWFET and counterpart devices are investigated under realistic operating conditions, thereby assessing their suitability for high-speed and low-power nanoscale circuit applications.

This chapter focuses on analysing the performance of the I-JL-NWFET-based CMOS inverter and RO to demonstrate how device-level innovations can significantly influence circuit-level performance. The remaining paper is organized into six sections with Section 5.1 as the introduction. Section 5.2 details the proposed device architecture, the calibration procedure, and the descriptions of the counterpart devices. Section 5.3 presents the device-level performance analysis. In Section 5.4, the static and dynamic characteristics of CMOS inverters based on the I-JL-NWFET and the other considered devices are systematically analyzed. Section 5.5 examines the performance of the RO employing both the proposed and counterpart devices. Finally, Section 5.6 concludes the paper by summarizing the key findings of this chapter.

5.2 DEVICE DESCRIPTION AND SIMULATION SET UP

To evaluate the performance of n-type and p-type I-JL-NWFET devices for circuit-level analysis, comprehensive device simulations are carried out using MixedMode simulator in SILVACO ATLAS. The 3-D and 2-D schematics of both transistor types are presented in Fig. 5.1 (a), (b), (c), and (d), respectively. For the n-type I-JL-NWFET, the L_C, t_{si}, and $L_{S/D}$ are set to 30 nm, 10 nm, and 25 nm, respectively. To compensate for the inherently lower hole mobility in the p-type device, the t_{si} and t_{core} of the p-type I-JL-NWFET are chosen to be twice that of its n-type counterpart [170]. The default mobility values (μ_n = 1000 cm²/Vs and μ_p = 500 cm²/Vs), as specified in the Silvaco user manual, are retained during simulations.

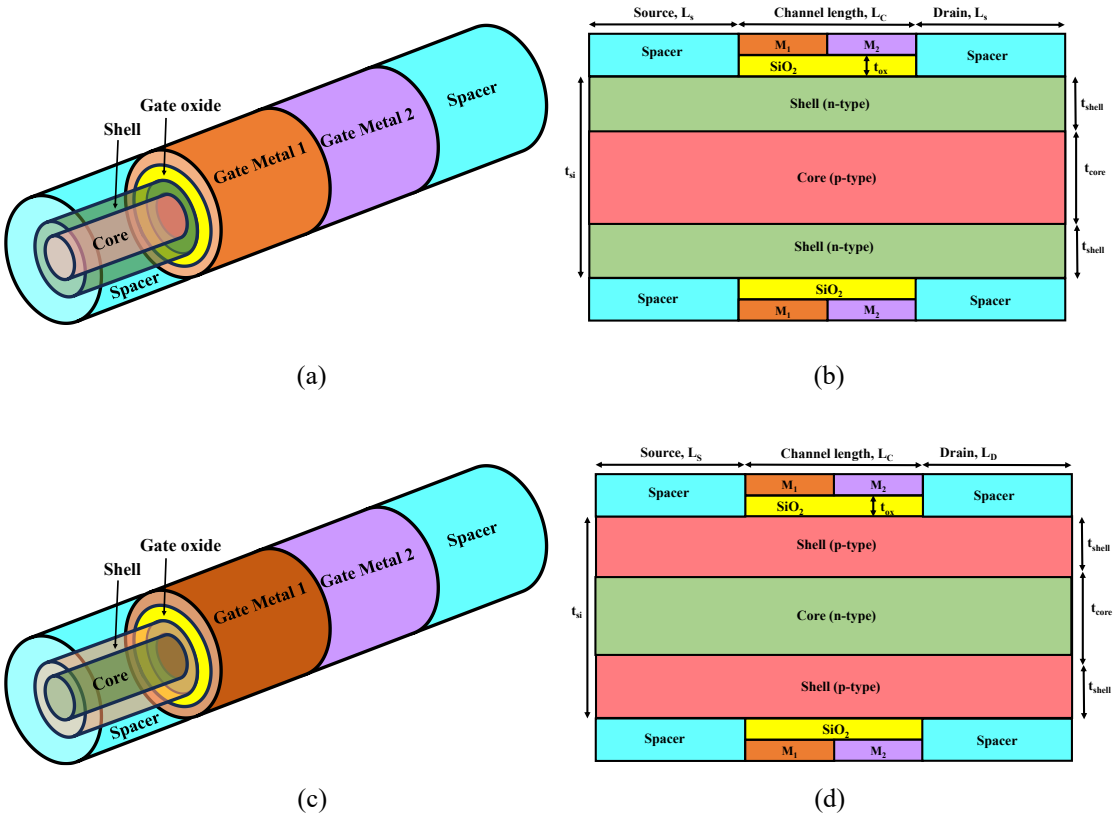


Fig. 5.1 (a) 3-D view, (b) 2-D view of n-type I-JL-NWFET, (c) 3-D view, (d) 2-D view of p-type I-JL-NWFET

The n-type I-JL-NWFET features a uniformly doped shell region with a doping concentration of 1×10^{19} cm^{-3} extending across the source, channel, and drain. Conversely, in the complementary p-type I-JL-NWFET, the shell is p-type doped at 1×10^{19} cm^{-3}, with an n-type core placed centrally within the channel.

In the absence of reported experimental data for cylindrical CS-JLNWFET structures, I-JL-NEFET is calibrated using available experimental JL-NWFET data [107], and the corresponding transfer characteristics are presented earlier in Chapter 2 in Fig. 24. Since experimental I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of non-cylindrical CS-JL FET are available in the literature [19], the calibrated simulation results have been validated against the experimental results, which share similar underlying physics. The comparison is presented in Fig. 5.2 (a), (b), (c), and (d). It is important to note that the primary objective of calibration is to ensure that the simulation environment accurately captures the device's physical behavior. A close agreement between simulation and experimental results is observed, with average deviations of 18.665%, 14.08%, 12.60%, and 10.37% for Fig. 5.2 (a), (b), (c), and (d), respectively. These deviations are primarily attributed to geometrical differences, as the simulated device employs a cylindrical CS architecture, whereas the experimental device is non-cylindrical.

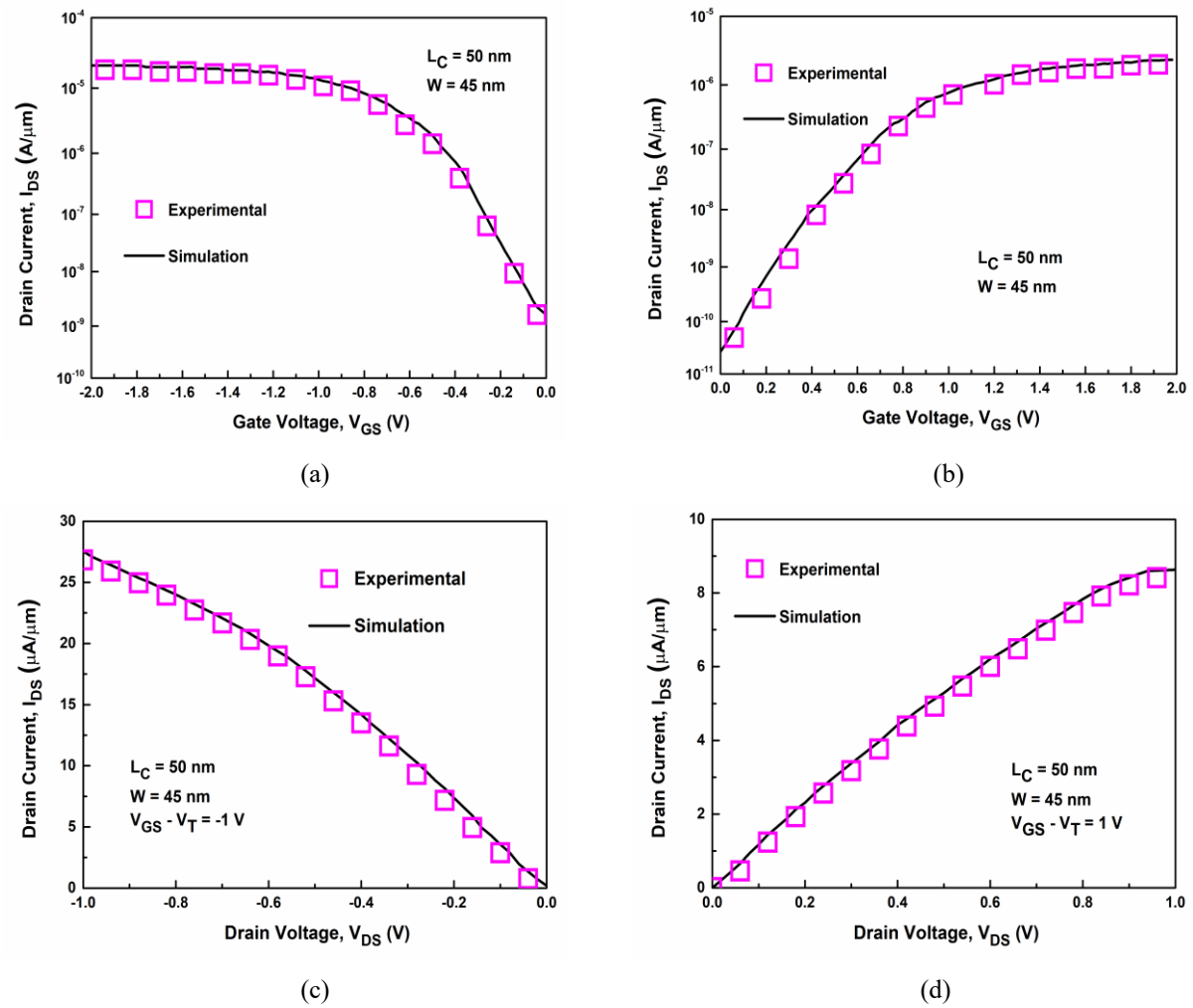


Fig. 5.2 Comparison of simulation and experimental results of (a) p-type transfer characteristics, (b) n-type transfer characteristics, (c) p-type output characteristics, and (d) n-type output characteristics

For comparative analysis, the proposed I-JL-NWFET device is referred to as device D1 in this chapter. It is systematically evaluated against three comparative architectures, namely D2, D3, and D4. The device D2 integrates the DMG and the oppositely doped core but excludes the spacer extension. Device D3 employs an SMG with the oppositely doped core and device D4 represents the conventional JL-NWFET baseline. These comparative devices design corresponds to devices D2, D3, and D5, respectively, as previously used for comparative analysis in Section 2.5 of Chapter 2.

However, it should be noted that in Section 2.5 of Chapter 2, these devices are analysed with L_C = 60 nm and t_{si} = 20 nm, consistent with the experimental NWFET device specifications discussed in Section 2.2. In contrast, in the present chapter, all devices are designed with identical dimensions of L_C = 30 nm and t_{si} = 10 nm, based on the optimized design parameters of I-JL-NWFET obtained in Sections 2.6 and 2.7. The corresponding 3-D and 2-D device

structures are presented in Fig. 5.4 (a), (b) for D2, (c), (d) for D3, and (e), (f) for D4, which illustrate only the n-type configurations.

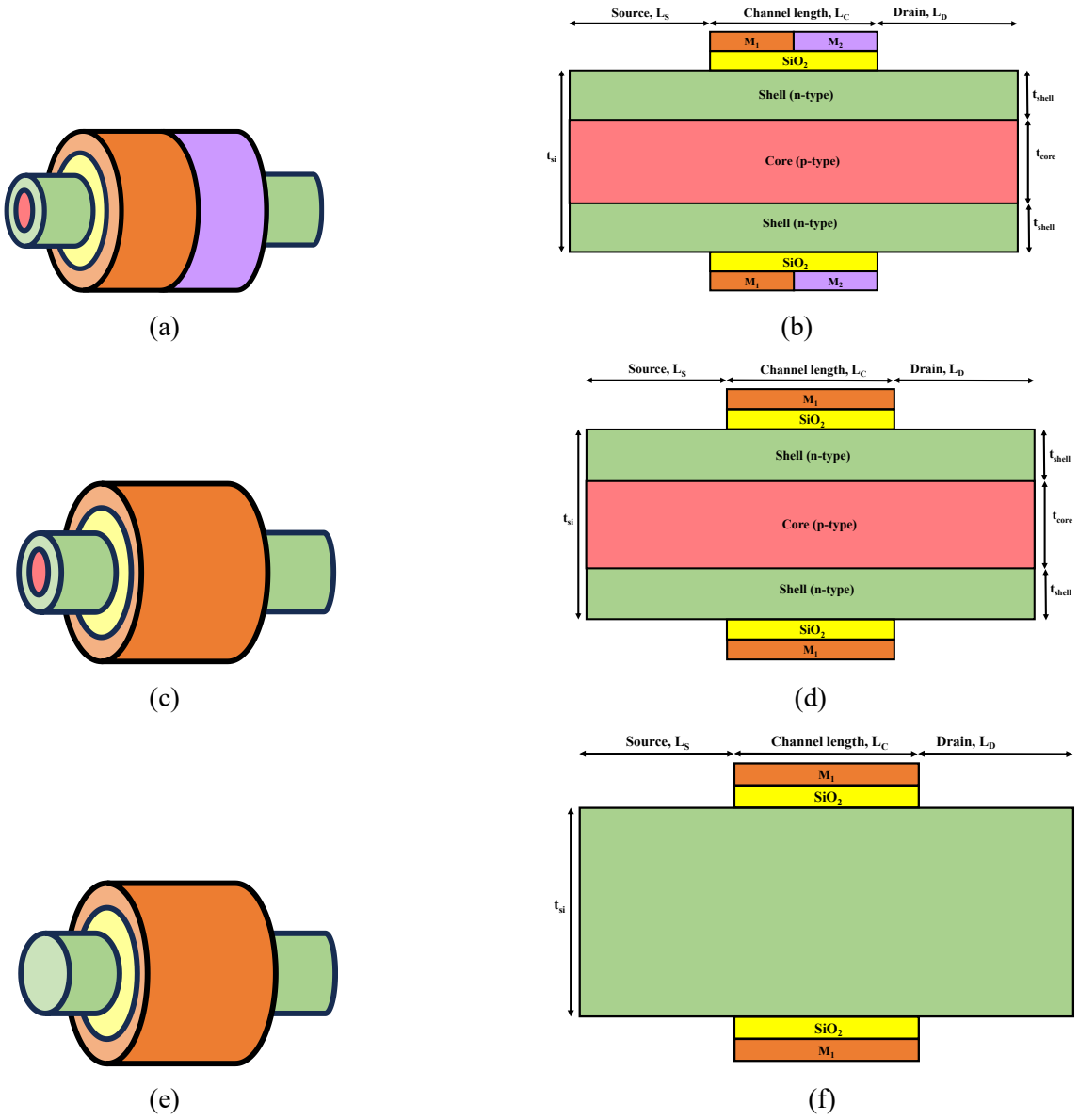


Fig. 5.3 3-D and 2-D structures of devices D2, D3, and D4, where (a, b) correspond to D2, (c, d) to D3, and (e, f) to D4, respectively

Devices D3 and D4 have been previously reported in the literature [17] and [10], respectively. In contrast, D1 represents the proposed architecture of this work, while D2 is an intermediate variant of the proposed I-JL-NWFET device, introduced for comparison by excluding the GSS. Furthermore, each architecture (D1, D2, D3, and D4) is implemented for both n-type and p-type operation. Hereafter, for clarity, the corresponding n-type devices are denoted as N1, N2, N3, and N4, while the corresponding p-type devices are denoted as P1, P2, P3, and P4 in the subsequent sections.

5.3 DEVICE LEVEL ANALYSIS

This section presents a comprehensive device-level evaluation of the proposed I-JL-NWFET device (N1) to elucidate the impact of structural modifications on electrostatic control and leakage suppression. The key metrics including surface potential, energy band profiles, transfer characteristics, and gate capacitance are analyzed and compared with devices N2, N3, and N4. Fig. 5.4 compares the surface potential distribution along the channel in the OFF-state (V_{GS} = 0) for the devices N1, N2, N3, and N4, highlighting the impact of successive architectural modifications on electrostatic control. The conventional JL-NWFET structure (device N4) exhibits a relatively smooth and gradual surface potential variation, indicating weak gate control and a higher susceptibility to SCEs such as DIBL.

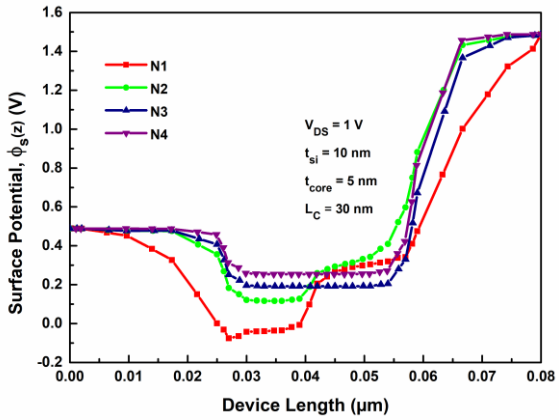


Fig. 5.4 Surface potential profile of devices N1, N2, N3, and N4 in the OFF-state

The introduction of an oppositely doped core in the N3 device causes enhanced depletion in the shell region during the OFF-state, which reduces the carrier concentration available to screen the gate electric field. This allows stronger gate-field penetration into the channel, resulting in a downward shift of the surface potential compared to the conventional N4 device. Device N2 further improves the surface potential profile by incorporating a DMG in conjunction with the oppositely doped core. The DMG introduces a distinct step in the surface potential at the interface of the two gate materials, which reinforces the source-side potential barrier and reduces the lateral electric field toward the drain. As a result, device N2 demonstrates improved immunity to DIBL and enhanced electrostatic integrity relative to N3 and N4.

In the proposed device N1, a more pronounced downward shift in surface potential is observed across the source, channel, and drain regions. The potential step introduced by the DMG, together with the high-permittivity GSS, intensifies the fringing electric field. This enhanced

field promotes stronger depletion extending beyond the channel region, resulting in a further reduction of the surface potential. Overall, the surface potential comparison clearly indicates a progressive improvement from device N4 to N1, confirming that the synergistic integration of an oppositely doped core, DMG, and GSS is crucial for achieving superior electrostatic performance for electronic applications.

The CB and VB energy profiles of devices N1, N2, N3, and N4 under OFF-state bias conditions are demonstrated in Fig. 5.5, providing insight into carrier transport and leakage suppression mechanisms. In device N3, the incorporation of an oppositely doped core increases depletion in the shell region, which elevates the source–channel energy barrier in both the CB and VB compared to a conventional structure without core-shell N4. The upward shift of the CB in N3 hinders carrier injection, thereby reducing I_{OFF}. However, both band profiles remain relatively smooth along the channel, limiting the extent of leakage suppression. Moreover, further improvement is observed in N2, where the addition of a DMG to the oppositely doped core introduces a distinct step in the band profiles near the interface of the two gate materials.

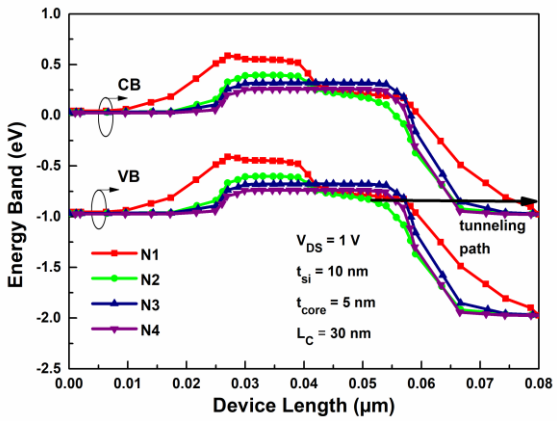


Fig. 5.5 Conduction band and valence band energy profile of devices N1, N2, N3, and N4 in the OFF-state

This step effectively increases the energy barrier at the source side while screening the channel from drain-induced potential modulation. Additionally, the tunneling width toward the drain is increased, which suppresses electron tunneling from the VB to the CB and leads to a reduction in I_{OFF} compared to devices N3 and N4. In N1, which integrates the DMG, oppositely doped core, and high-permittivity GSS, the CB and VB profiles exhibit the highest source-channel energy barrier and the largest tunneling width compared to devices N2 to N4. The spacer-enhanced fringing electric field further strengthens depletion beyond the channel region, resulting in minimal band lowering near the drain. Consequently, device N1 demonstrates the strongest suppression of carrier injection and the lowest I_{OFF} among all the compared devices.

Figure 5.6 compares the total Gate to Gate Capacitance (C_{gg}) as a function of V_{GS} for devices P1, P2, P3, P4, and N1, N2, N3, N4. The conventional JL-NWFET (device N4) exhibits the highest C_{gg}, primarily due to weaker channel depletion in the OFF-state and stronger capacitive coupling between the gate and the conductive channel region. This higher capacitance can adversely impact switching speed and dynamic power consumption. In device N3, the introduction of an oppositely doped core enhances depletion in the shell region, thereby reducing the effective charge density under the gate. As a result, C_{gg} is noticeably reduced compared to N4, reflecting improved electrostatic control and weakened gate-to-channel coupling. Further improvement is observed in device N2, where the incorporation of the DMG modifies the potential distribution along the channel.

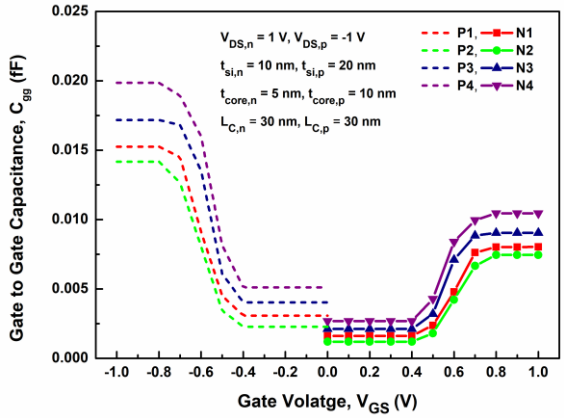


Fig. 5.6 Comparison of Gate to Gate capacitance for devices P1-P4 and N1-N4

The DMG reduces gate–drain capacitive coupling by introducing a potential step near the source side, which limits carrier accumulation toward the drain. Consequently, device N2 demonstrates a lower C_{gg} compared to devices N3 and N4. In the proposed device N1, which integrates the DMG, oppositely doped core, and a high-k GSS, the introduction of the high-permittivity spacer increases the fringe capacitance, leading to a slightly higher C_{gg} compared to Device N2. Although the proposed device N1 exhibits a marginally higher C_{gg} than device N2 due to increased fringe capacitance arising from the high-permittivity spacer, it delivers significantly enhanced electrostatic control and substantially lower leakage current. In contrast, device N2 benefits from the lowest C_{gg} and consequently achieves the minimum intrinsic delay among all devices, indicating superior switching speed.

Furthermore, corresponding p-type devices (P1, P2, P3, and P4) exhibit higher C_{gg} compared to their corresponding n-type devices (N1, N2, N3, and N4), respectively. This increase is attributed to the larger t_{si} and t_{core}, which enhance gate-to-channel capacitive coupling, along with the inherently lower hole mobility requiring stronger charge accumulation. Similar to the

n-type trend, P4 exhibits the highest C_{gg} due to weaker electrostatic control, while P1 and P2 demonstrate relatively lower capacitance compared to P3 and P4, indicating improved channel depletion and better gate control.

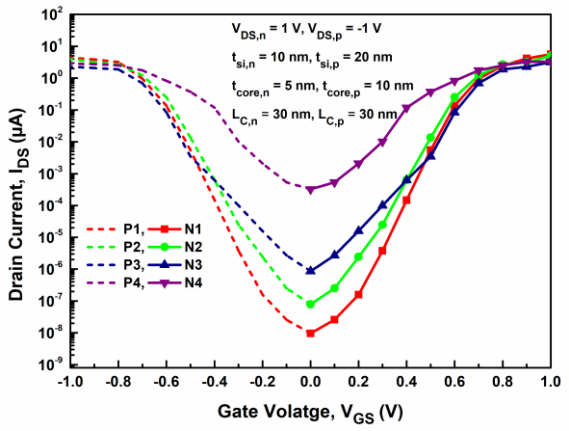


Fig. 5.7 Comparison of transfer characteristics of devices P1-P4 and N1-N4

The transfer characteristics of complementary n-type and p-type devices play a crucial role in determining the voltage transfer characteristics, switching threshold, noise margins, and overall stability of CMOS inverter circuits. Therefore, a detailed analysis of the individual device-level transfer characteristics is essential before proceeding to inverter-level evaluation. In particular, the inclusion of well-matched p-type devices is critical for achieving balanced pull-up and pull-down strengths in complementary logic. Fig. 5.7 illustrates the transfer characteristics for both p-type (P1, P2, P3, and P4) and n-type (N1, N2, N3, and N4) versions of devices D1, D2, D3, and D4, respectively, enabling a clear comparison of SS, I_{OFF}, and V_T control. Devices N4 and P4, which correspond to the conventional JL-NWFET baseline, exhibit the highest I_{OFF} and a relatively degraded SS, reflecting limited electrostatic control of the channel.

Introducing an oppositely doped core with an SMG in devices N3 and P3 leads to a noticeable reduction in I_{OFF} and an improvement in SS, indicating enhanced depletion control in the shell region of the channel. Furthermore, the performance enhancement is observed in devices N2 and P2, where the incorporation of a DMG along with the oppositely doped core results in a steeper SS and suppressed I_{OFF} compared to N3 and P3. This improvement arises from the step-in surface potential introduced by the DMG, which strengthens gate control near the source end and mitigates SCEs. The most pronounced improvement is achieved in devices N1 and P1, which combine the DMG, oppositely doped core, and GSS extension. In the N1 and P1 devices, the transfer characteristics show the lowest I_{OFF} and the sharpest subthreshold transition among all device configurations.

The spacer-assisted DMG effectively reduces fringe-field penetration and enhances electrostatic integrity, leading to superior channel control. Overall, the progressive transition from N4 to N1 and P4 to P1 demonstrates a systematic improvement in subthreshold performance. These results confirm that the combined use of a DMG, oppositely doped core, and GSS is most effective in suppressing leakage current and improving subthreshold characteristics. Table 5.1 presents a comparative summary of the key electrical characteristics of the devices N1-N4 and P1-P4, including V_T, I_{ON}, I_{OFF}, C_{gg}, and intrinsic delay (τ). The intrinsic delay is calculated as [171]

$$\tau = \frac{V_{DD} C_{gg}}{I_{ON}} \tag{5.1}$$

Table 5.1. Characteristics comparison of N1, N2, N3, N4, P1, P2, P3, and P4 devices

Devices	V_T (V)	I_{ON} (μA)	I_{OFF} (μA)	C_{GG} (fF)	τ (ps)
N1	0.56	5.57	9.55×10^{-9}	0.00803	1.43
N2	0.55	4.97	7.89×10^{-8}	0.00746	1.40
N3	0.53	3.16	8.62×10^{-7}	0.00904	2.84
N4	0.50	3.28	3.25×10^{-4}	0.01045	3.04
P1	0.53	4.39	11.95×10^{-9}	0.01526	3.41
P2	0.52	3.93	9.35×10^{-8}	0.01417	3.39
P3	0.50	2.26	10.32×10^{-7}	0.01718	7.52
P4	0.48	2.84	5.25×10^{-4}	0.01986	6.69

While N2 exhibits the lowest intrinsic delay due to its reduced gate capacitance, N1 offers a more balanced performance by combining competitive switching speed with superior leakage suppression and electrostatic integrity. Compared to N1, N2, N3, and N4 devices, corresponding P1, P2, P3, and P4 devices exhibit higher τ and C_{gg}, along with lower I_{ON}, respectively, primarily due to the lower mobility of holes compared to electrons.

5.4 CIRCUIT LEVEL CMOS INVERTER ANALYSIS

This section presents a circuit-level evaluation of the proposed D1 device through CMOS inverter analysis. The key inverter metrics, including VTC, noise margins, and switching behavior, are examined to assess the impact of device-level electrostatic improvements on logic robustness, switching sharpness, and suitability for low-power digital applications. Figure 5.8 portrays the 3-D schematic of CMOS inverters Inv1, Inv2, Inv3, and Inv4, realized using complementary p-type (P1, P2, P3, and P4) and n-type (N1, N2, N3, and N4) devices corresponding to the four architectures considered in this work. Here, C_L denotes the load capacitance of 3fF seen at the output node of the CMOS inverter [172].

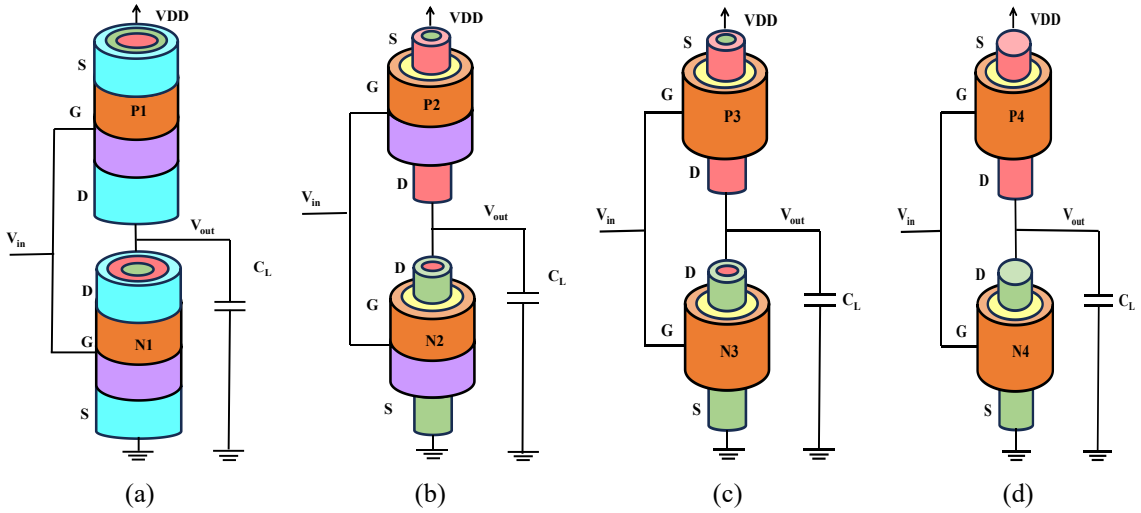


Fig. 5.8 Basic 3-D structures of CMOS inverter (a) Inv1, (b) Inv2, (c) Inv3, and (d) Inv4 realized using complementary n-type (N1, N2, N3, and N4) and p-type (P1, P2, P3, and P4) devices, respectively

The simulation of these circuits is carried out using the ATLAS MixedMode simulator. Fig. 5.9 demonstrates the combined VTCs of CMOS inverters (Inv1, Inv2, Inv3, and Inv4) realized using complementary n-type (N1, N2, N3, and N4) and p-type (P1, P2, P3, and P4), respectively, under identical biasing and geometrical conditions. The slope and position of the VTC curves provide insight into inverter switching behavior, gain, and electrostatic control.

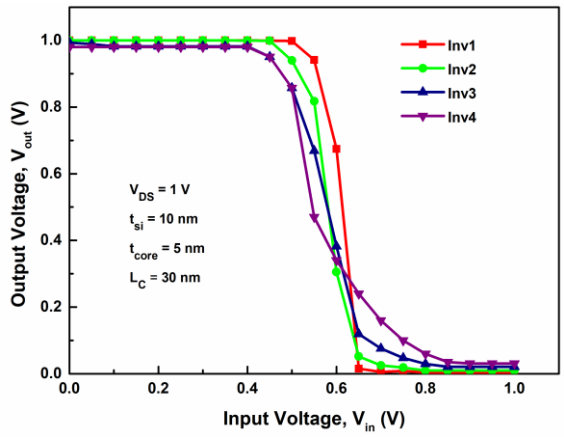


Fig. 5.9 Comparison of voltage transfer characteristics of the CMOS inverters Inv1, Inv2, Inv3, and Inv4

A pronounced rightward shift of the VTC is observed as the device configuration evolves from Inv4 to Inv1, reflecting a gradual increase in the effective V_T due to the cumulative introduction of electrostatic boosters. The Inv4 exhibits the lowest V_T and the most gradual transition between logic levels, indicating weaker gate control and a wider switching region. In Inv3, the incorporation of an oppositely doped core enhances depletion in the shell region, resulting in a higher V_T and a steeper VTC compared to Inv4. The addition of a DMG in Inv2 further increases V_T by introducing a surface potential step near the source, which suppresses early

carrier injection and strengthens source-side electrostatic control. The Inv1 integrates all these features along with a GSS, which depletes the channel beyond the gate region.

Consequently, early channel formation is suppressed, channel inversion is delayed, and a higher input voltage is required to initiate conduction. Together, these effects result in the steepest VTC transition and the most pronounced rightward shift of the inverter switching point in Inv1, demonstrating superior gate control and improved switching behavior. The noise margin quantifies the immunity of a digital circuit to noise disturbances, and higher noise margin values are essential for reliable circuit operation. The noise margins for low and high logic levels are defined as the low-level noise margin (NM_L) and high-level noise margin (NM_H), respectively, and are expressed as [173]

$$NM_H = V_{OH} - V_{IH} \tag{5.2}$$

$$NM_L = V_{IL} - V_{OL} \tag{5.3}$$

where V_{OL} and V_{OH} represent the maximum and minimum output voltages corresponding to logic '0' and logic '1', respectively. The minimum high input voltage and maximum low input voltage are denoted as V_{IH} and V_{IL}, respectively, and are defined by points where slope = -1 in the VTC characteristics.

Figures 5.10 (a), (b), (c), and (d) present the extraction of parameters such as V_{OH}, V_{OL}, V_{IL}, and V_{IH} for the CMOS inverters Inv1, Inv2, Inv3, and Inv4, respectively, which are used to evaluate the noise margins. The extracted parameters required to evaluate the noise margins are summarized in Table 5.2. As observed in Table 5.2, all CMOS inverters achieve a near-ideal V_{OH} of 1 V, indicating strong pull-up capability. However, significant differences are observed in V_{OL}. Inv1 exhibits the lowest V_{OL} owing to the combined effect of the DMG, oppositely doped core, and GSS, which together enhance channel depletion in the OFF state and suppress I_{OFF}. The improved electrostatic control minimizes residual channel charge, ensuring a stronger pull-down operation and resulting in an output voltage very close to ground. Consequently, Inv1 achieves the highest NM_L and a large NM_H, reflecting well-balanced and maximized noise margins.

This superior noise margin performance confirms the strong electrostatic integrity and robust switching behavior of the proposed structure. Inv2 shows slightly reduced noise margins compared to Inv1 due to its relatively higher V_{OL} and narrower transition window. Although the DMG and oppositely doped core improve gate control and suppress SCEs, the absence of spacer extension leads to increased fringe-field coupling and incomplete suppression of I_{OFF}. As a result, the pull-down strength is marginally weakened, causing an increase in V_{OL} and a

reduction in both NM_L and NM_H. Inv3 and Inv4 exhibit progressive degradation in noise margins due to weaker electrostatic control. In Inv3, the use of the SMG with an oppositely doped core improves depletion compared to Inv4; however, the lack of a DMG limits source-side control, resulting in a broader transition region and increased V_{OL}. The Inv4 suffers the most from poor electrostatic integrity, resulting in the highest V_{OL} and the widest transition region.

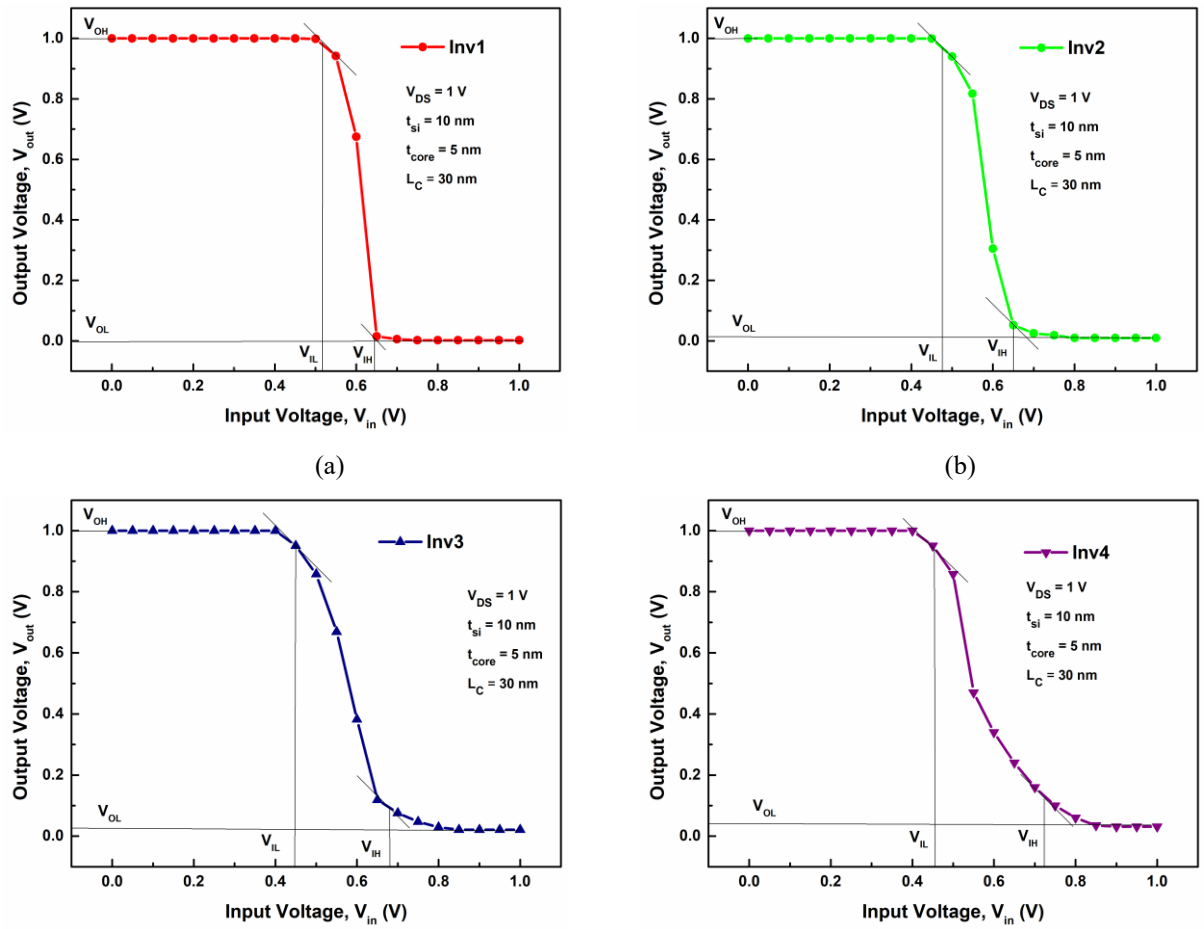


Fig. 5.10 Comparison of voltage transfer characteristics of the CMOS inverters (a) Inv1, (b) Inv2, (c) Inv3, and (d) Inv4

Table 5.2. Extracted static parameters of the CMOS inverters Inv1, Inv2, Inv3, and Inv4

CMOS Inverters	V_{OH} (V)	V_{OL} (V)	V_{IH} (V)	V_{IL} (V)	NM_H (V)	NM_L (V)
Inv1	1	0.002	0.645	0.517	0.355	0.515
Inv2	1	0.009	0.650	0.475	0.350	0.466
Inv3	1	0.021	0.680	0.456	0.320	0.435
Inv4	1	0.031	0.725	0.451	0.275	0.420

Although Inv4 exhibits a moderate NM_L due to its relatively higher V_{OL}, the significantly reduced NM_H and gradual switching behavior severely limit its overall noise immunity. The

transient performance of the CMOS inverter Inv1, Inv2, Inv3, and Inv4 is evaluated in terms of propagation delay, which directly governs both the dynamic power dissipation and the maximum achievable operating frequency of digital circuits. Since the inverter constitutes the fundamental building block of an RO, an accurate assessment of its timing characteristics is essential for predicting RO oscillation frequency and delay behavior. Accordingly, the inverter delay analysis presented in this work forms the basis for the RO-based circuit-level evaluation discussed in the following section.

The propagation delay of a CMOS inverter (τ_P) is defined as the average of the high-to-low and low-to-high transition delays, given by [173]

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} \tag{5.4}$$

where τ_{PHL} represents the delay associated with a high-to-low output transition, and τ_{PLH} corresponds to a low-to-high output transition. Specifically, τ_{PHL} is measured as the time interval between the 50% transition point of the rising input voltage and the 50% transition point of the falling output voltage, while τ_{PLH} is defined as the time interval between the 50% transition point of the falling input voltage and the 50% transition point of the rising output voltage. These delay components collectively determine the effective stage delay used in RO frequency estimation. The τ_{PHL} and τ_{PHL} are given as [173]

$$\tau_{PHL} = \frac{C_L L_C}{\mu_e' C_{ox} \pi \left(t_{si} - t_{core}\right)\left(V_{OH} - V_{T,n}\right)} \left[\frac{2V_{T,n}}{\left(V_{OH} - V_{T,n}\right)} + \ln\left(\frac{4\left(V_{OH} - V_{T,n}\right)}{V_{OH} + V_{OL}} - 1 \right) \right] \tag{5.5}$$

$$\tau_{PLH} = \frac{C_L L_C}{\mu_e' C_{ox} \pi \left(t_{si} - t_{core}\right)\left(V_{OH} - V_{OL} - \left|V_{T,p}\right|\right)} \left[\frac{2\left|V_{T,p}\right|}{\left(V_{OH} - V_{OL} - \left|V_{T,p}\right|\right)} + \ln\left(\frac{2\left(V_{OH} - V_{OL} - \left|V_{T,p}\right|\right)}{V_{OH} - V_{50\%}} - 1 \right) \right] \tag{5.6}$$

$$\text{where, } V_{50\%} = \frac{V_{OL} + V_{OH}}{2} \tag{5.7}$$

The analytical model for the proposed device is developed in Chapter 3, Section 3.4, where $V_{T,n}$ for n-type and $V_{T,p}$ p-type devices are given as follow

$$\left|V_{T,p}\right| = V_{T,n} = \frac{-F_1 + \sqrt{F_1^2 - F_2 F_3}}{F_2} \tag{5.8}$$

$$\text{Where, } F_1 = \frac{2\left(\gamma_3 - \gamma_1\right)\left(W_2\gamma_4 - W_1\gamma_2\right) + 2\left(\gamma_2 - \gamma_4\right)\left(W_1\gamma_1 - W_2\gamma_3\right)}{\left(\gamma_1\gamma_4 - \gamma_3\gamma_2\right)^2} - \alpha_2 \tag{5.9}$$

$$F_2 = \frac{4\left(\gamma_3 - \gamma_1\right)\left(W_1\gamma_1 - W_2\gamma_3\right)}{\left(\gamma_1\gamma_4 - \gamma_3\gamma_2\right)^2} - 1 \tag{5.10}$$

$$F_3 = \frac{4\left(W_1\gamma_1 - W_2\gamma_3\right)\left(W_2\gamma_4 - W_1\gamma_2\right)}{\left(\gamma_1\gamma_4 - \gamma_3\gamma_2\right)^2} - {\alpha_2}^2 \tag{5.11}$$

$$W_1 = V_{bi} + V_{DS} + \alpha_4\left(\cosh\left(\frac{L_4}{\lambda_4}\right) - 1\right) - \alpha_3\cosh\left(\frac{L_4}{\lambda_4}\right) + \left(\alpha_3 - \alpha_2\right)\delta \tag{5.12}$$

$$W_2 = V_{bi} + \alpha_1\left(\cosh\left(\frac{L_1}{\lambda_1}\right) - 1\right) - \alpha_C\cosh\left(\frac{L_1}{\lambda_1}\right) \tag{5.13}$$

$$\gamma_1 = \cosh\left(\frac{L_1}{\lambda_1}\right) + \left(\frac{\lambda_1}{\lambda_2}\right)\sinh\left(\frac{L_1}{\lambda_1}\right),\ \gamma_2 = \cosh\left(\frac{L_1}{\lambda_1}\right) - \left(\frac{\lambda_1}{\lambda_2}\right)\sinh\left(\frac{L_1}{\lambda_1}\right) \tag{5.14}$$

$$\gamma_3 = \left(1 - \frac{\lambda_3}{\lambda_2}\right)\delta e^{-L_1/\lambda_1},\ \gamma_4 = \left(1 + \frac{\lambda_3}{\lambda_2}\right)\delta e^{L_1/\lambda_1} \tag{5.15}$$

$$\alpha_n = \frac{qN_d t_{si} - qt_{core}\left(N_a + N_d\right)}{4C_n} - V_{fbn}\text{, for n-channel device}$$
$$\alpha_n = \frac{-qN_a t_{si} - qt_{core}\left(N_a + N_d\right)}{4C_n} - V_{fbn}\text{, for p-channel device} \tag{5.16}$$

$${\lambda_n}^2 = \frac{\varepsilon_{si} t_{si}}{4C_n} \tag{5.17}$$

where n = 1 (source region), 2 (channel region under M_1), 3 (channel region under M_2), and 4 (drain region). In practical digital systems, input signals exhibit finite rise and fall times, which directly influence inverter switching behavior and timing robustness. When a pulse input with non-zero rise time (τ_{rise}) and fall time (τ_{fall}) is applied, the delay components can be expressed as [173]

$$\tau_{PHL(nonideal)} = \sqrt{\tau_{PHL(ideal)}^2 + \left(0.5\tau_{rise}\right)^2} \tag{5.18}$$

$$\tau_{PLH(nonideal)} = \sqrt{\tau_{PLH(ideal)}^2 + \left(0.5\tau_{rise}\right)^2} \tag{5.19}$$

To evaluate this effect, the transient response of the CMOS inverter Inv1, Inv2, Inv3, and Inv4 is first analyzed under non-ideal input conditions using a 0-1 V pulse waveform with rise and fall times of 10 ps. The corresponding transient waveforms are plotted together and shown in Fig. 5.11. Under non-ideal excitation with finite τ_{rise} and τ_{fall}, inverter Inv2 exhibits the sharpest output transient response, indicating superior switching agility and reduced sensitivity to input slew degradation. This behavior is primarily attributed to the absence of the GSS, which results in lower C_{gg} and enables faster charging and discharging of the output node under realistic input conditions.

The combined effect of the DMG and oppositely doped core in Inv2 further enhances channel modulation, contributing to its steep transient slope. Inverter Inv1, which incorporates the DMG, oppositely doped core, and GSS, exhibits a comparatively smoother transient response

under non-ideal excitation. Although the spacer introduces additional C_{gg}, it significantly improves electrostatic control near the drain-side channel region, thereby enhancing stability and suppressing leakage. As a result, while the transient slope of Inv1 is slightly less abrupt than that of Inv2 under non-ideal input conditions, it remains robust and well-controlled, particularly during the high-to-low transition. Inverters Inv3 (JL-NWFET + CS + SMG) and Inv4 (JL-NWFET) exhibit noticeably slower transient responses and pronounced delay degradation due to inferior electrostatic integrity, higher leakage current, and weaker channel control.

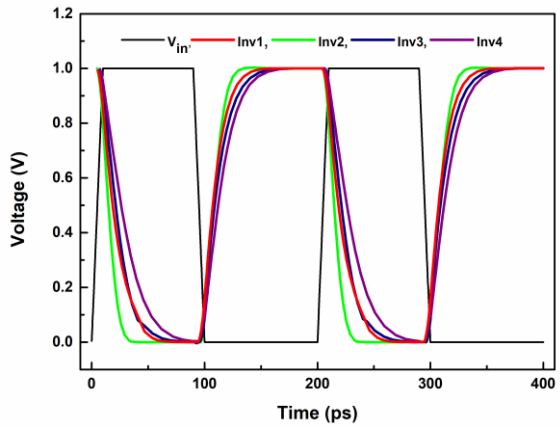


Fig. 5.11 Comparison of transient characteristics of the CMOS inverters Inv1, Inv2, Inv3, and Inv4

To accurately extract propagation delay parameters, the CMOS inverter transient response is next evaluated using an ideal pulse input with a voltage swing of 0-1 V and zero τ_{rise} and τ_{fall} and are plotted in Fig. 5.12 (a), (b), (c), and (d) for CMOS inverters Inv1, Inv2, Inv3, and Inv4, respectively. Under ideal excitation, the pull-down delay is dominated by intrinsic channel control rather than gate capacitance, allowing the DMG-spacer-oppositely doped core configuration in Inv1 to achieve the minimum τ_{PHL}. Inverter Inv2 achieves the minimum τ_{PLH} due to its reduced gate capacitance in the absence of a spacer, which facilitates faster charging of the output node. Consequently, although Inv1 exhibits the lowest τ_{PHL}, inverter Inv2 attains the lowest average propagation delay τ_P, making it more favorable for achieving higher RO oscillation frequencies. Inverters Inv3 and Inv4 exhibit significantly higher τ_{PHL}, τ_{PLH}, and τ_P values due to degraded electrostatic control, increased leakage current, and weaker channel modulation.

A quantitative comparison of the extracted propagation delay parameters under both ideal and non-ideal input conditions is summarized in Table 5.3. As evident from Table 3, all CMOS inverters Inv1, Inv2, Inv3, and Inv4 experience an increase in propagation delay when finite rise and fall times are introduced; however, the delay penalty is least pronounced for Inv1 and

Inv2, confirming their superior resilience to input slew degradation. Notably, Inv2 consistently demonstrates the lowest average propagation delay across both excitation conditions, reinforcing its suitability for high-speed RO-based circuit applications.

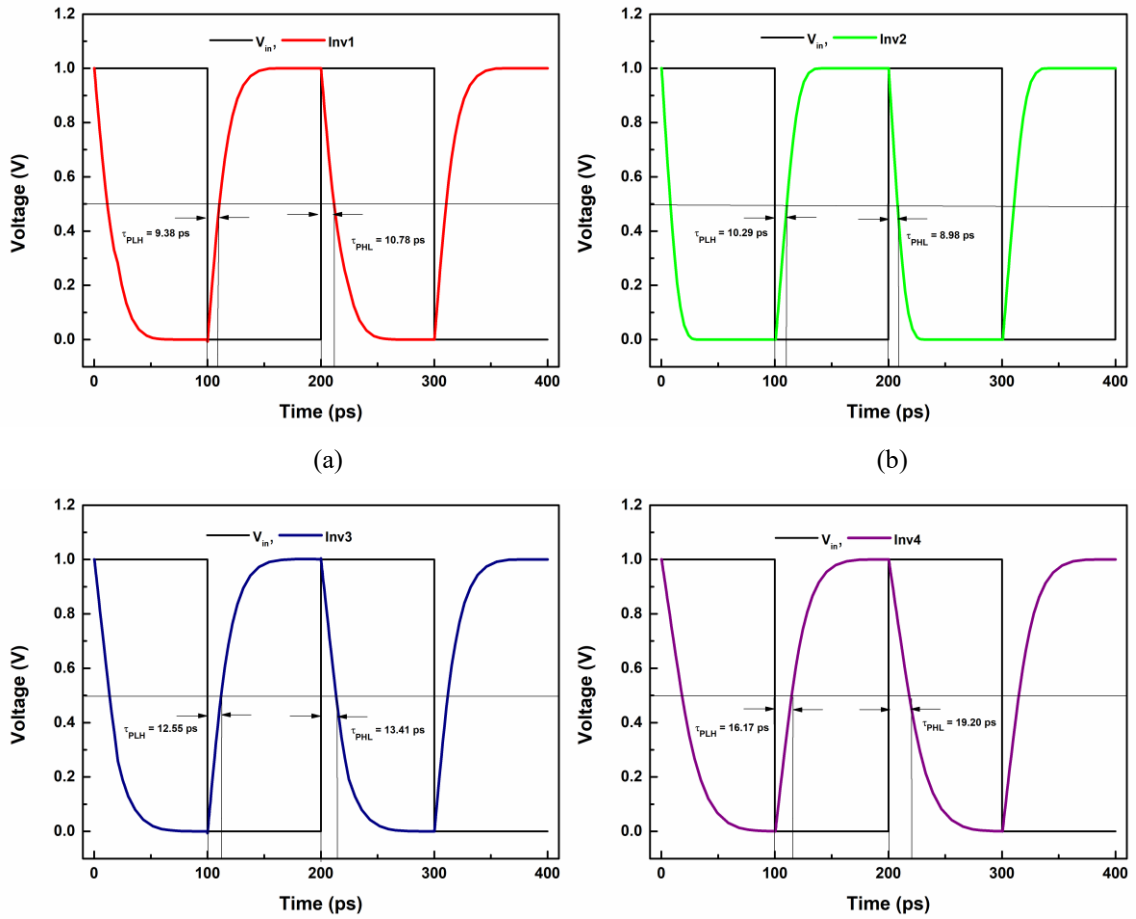


Fig. 5.12 Comparison of transient characteristics of the CMOS inverters (a) Inv1, (b) Inv2, (c) Inv3, and (d) Inv4

Table 5.3. Extracted dynamic parameters of the CMOS inverter Inv1, Inv2, Inv3, and Inv4

CMOS Inverters	Ideal case ($\tau_{rise} = \tau_{fall} = 0$)			Non-Ideal case ($\tau_{rise} = \tau_{fall} = 10$ ps)		
	τ_{PLH} (ps)	τ_{PHL} (ps)	τ_P (ps)	τ_{PLH} (ps)	τ_{PHL} (ps)	τ_P (ps)
Inv1	9.38	10.78	10.08	10.62	11.88	11.25
Inv2	10.29	8.98	9.63	11.44	10.27	10.85
Inv3	12.55	13.41	12.98	13.50	14.31	13.90
Inv4	16.17	19.20	17.68	16.92	19.84	18.38

Table 5.4 presents the comparative performance of CMOS inverters Inv1, Inv2, Inv3, and Inv4 based on τ_P, average power (P_{avg}), Power Delay Product (PDP), and Energy Delay Product (EDP). To use CMOS inverters in high-speed circuits with low power consumption, it is necessary to evaluate both PDP and EDP, where PDP = $P_{avg} \times \tau_P$ and EDP = PDP × τ_P, where, P_{avg} is the average power consumed by a CMOS inverter during operation [173]. It includes

dynamic, short-circuit, and leakage power components. It indicates the circuit's overall power efficiency. Among the designs, Inv2 exhibits minimum PDP and EDP, indicating superior overall energy efficiency and speed performance.

Table 5.4. PDP and EDP Comparison of the CMOS inverter Inv1, Inv2, Inv3, and Inv4

CMOS Inverters	τ_P (ps)	P_{avg} (µW)	*PDP (aJ)*	*EDP* (10^{-30} *Js*)
Inv1	11.25	42.70	480.87	5404.10
Inv2	10.85	40.61	440.61	4780.61
Inv3	13.90	38.70	537.93	7477.22
Inv4	18.38	35.52	652.85	11999.52

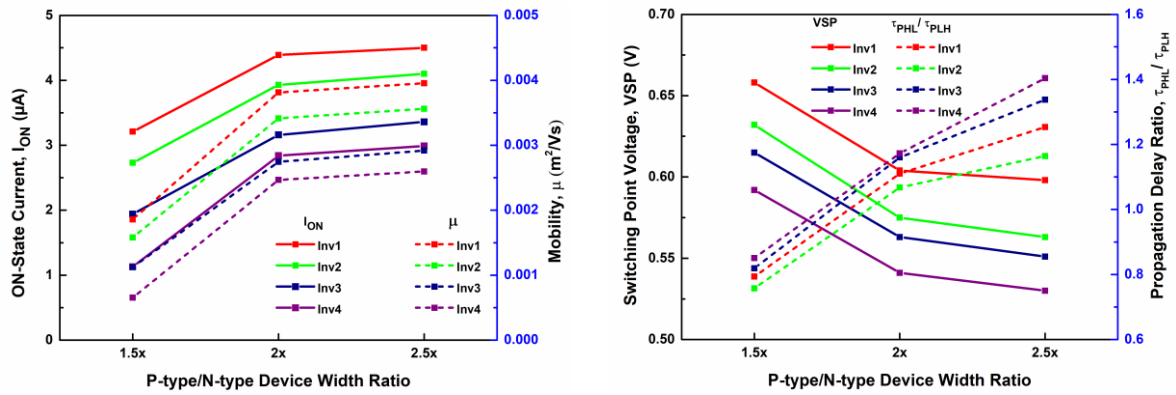
Although Inv1 shows comparable delay, its PDP and EDP are slightly higher than those of Inv2. In contrast, Inv3 demonstrates reduced power consumption but suffers from increased delay, resulting in a higher EDP. Inv4 achieves the lowest power consumption; however, it exhibits the largest delay, leading to the highest PDP and EDP among all configurations. Among the designs, between Inv1 and Inv2. While Inv2 achieves the lowest propagation delay along with minimum PDP and EDP, indicating better speed and energy efficiency, Inv1 offers comparable delay with slightly higher PDP and EDP, suggesting a marginal compromise in energy efficiency.

5.4.1 Effect of P-type Device Width on CMOS Inverter Performance

To achieve balanced inverter operation, the p-type/n-type device sizing ratio was systematically optimized by varying the t_{si} of P1, P2, P3, and P4 from 1.5× to 2.5× relative to their corresponding N1, N2, N3, and N4, respectively. The I_{ON} variation and mobility (μ) with sizing ratio is plotted in Fig. 5.13 (a). At 1.5×, the p-type devices exhibit insufficient drive strength, resulting in lower I_{ON} across all P1, P2, P3, and P4 devices. Increasing the ratio to 2× significantly enhances the I_{ON}, enabling improved pull-up capability and enabling better matching with N1, N2, N3, and N4. A further increase to 2.5× results in only marginal improvement, indicating diminishing returns due to increased parasitic loading. The μ variation in Fig 5.13 (a) further supports this observation.

At 1.5×, the mobility of P1, P2, P3, and P4 remains low, limiting current drivability. Increasing the ratio to 2× yields a substantial improvement, approaching the required strength for balanced operation with N1, N2, N3, and N4. At 2.5×, only a slight increase is observed, confirming mobility saturation effects. The Switching Point Voltage (VSP) and the propagation delay ratio (τ_{PHL}/τ_{PLH}) at different sizing ratios are demonstrated in Fig. 5.13 (b). At 1.5×, the VSP is significantly higher than mid-supply, indicating dominant n-type device behavior. Increasing

the ratio to 2× shifts the VSP closer to the ideal $V_{DD}/2$, achieving improved balance between P1, P2, P3, P4 and N1, N2, N3, N4. At 2.5×, the VSP shifts slightly lower, indicating the onset of n-type device dominance.



(a) (b)

Fig. 5.13 Effect of p-type/n-type device width ratio on (a) ON-state current and mobility, and (b) switching point voltage and propagation delay ratio

However, the shift is minimal compared to the improvement from 1.5× to 2×, reinforcing that 2× provides the most balanced switching condition. Furthermore, the τ_{PHL}/τ_{PLH} ratio at 1.5× is less than 1, indicating slower rise transitions due to weak p-type device dominance. At 2×, the ratio approaches unity, demonstrating near-balanced rise and fall delays. At 2.5×, the ratio exceeds unity significantly, indicating slower fall transitions due to p-type device overdrive. Based on μ, I_{ON}, VSP, and τ_{PHL}/τ_{PLH}, the 2× p-type/n-type device sizing ratio provides the optimal trade-off by ensuring near-equal pull-up and pull-down strengths, symmetric switching, minimal delay skew, and efficient geometry utilization.

5.4.2 Effect of Holes Mobility and Sizing on CMOS Inverter Performance

To evaluate the effectiveness of structural scaling over mobility enhancement, three cases were analyzed as shown in Table 5.5: (i) equal geometry ($t_{si,p} = t_{si,n}$) with default carrier mobility values (μ_n = 1000 cm²/Vs and μ_p = 500 cm²/Vs), (ii) artificial mobility enhancement ($\mu_p = 3\times \mu_n$) with equal geometry, and (iii) structural scaling ($t_{si,p} = 2\times t_{si,n}$) with default carrier mobility values. In Case 1, the inherently lower hole mobility leads to weak p-type (P1, P2, P3, and P4) drive strength compared to n-type (N1, N2, N3, and N4), resulting in reduced I_{ON}, a higher VSP > $V_{DD}/2$, and $\tau_{PHL}/\tau_{PLH} < 1$, indicating slower rising transitions. Although this configuration is physically realistic, it suffers from poor inverter balance and degraded performance.

In Case 2, while I_{ON} improves as mobility is artificially increased to compensate for weaker p-type conduction, it leads to overcompensation, resulting in a left-shifted switching point (VSP

< $V_{DD}/2$) and significant delay imbalance (τ_{PHL}/τ_{PLH} > 1.3), indicating dominant p-type behavior. Moreover, mobility enhancement does not account for capacitance effects and may not be physically realizable, limiting its reliability.

Table 5.5. Comparative analysis of mobility and structural scaling for Inv1, Inv2, Inv3, and Inv4

Cases	Parameters	Inv1	Inv2	Inv3	Inv4
Case 1: $t_{si,p}$ = $t_{si,n}$, μ_p = 500 cm²/Vs, μ_n = 1000 cm²/Vs	I_{ON} (μA)	3.21	2.73	1.94	1.13
	VSP (V)	0.65	0.63	0.61	0.59
	τ_{PHL}/τ_{PLH} ratio	0.79	0.76	0.82	0.85
Case 2: $t_{si,p}$ = $t_{si,n}$, μ_p = 1500 cm²/Vs, μ_n = 1000 cm²/Vs	I_{ON} (μA)	4.21	3.71	2.98	2.67
	VSP (V)	0.56	0.53	0.52	0.50
	τ_{PHL}/τ_{PLH} ratio	1.36	1.29	1.41	1.47
Case 3: $t_{si,p}$ = 2× $t_{si,n}$, μ_p = 500 cm²/Vs, μ_n = 1000 cm²/Vs (This work)	I_{ON} (μA)	4.39	3.93	3.16	2.84
	VSP (V)	0.60	0.57	0.56	0.54
	τ_{PHL}/τ_{PLH} ratio	1.11	1.06	1.16	1.17

In contrast, Case 3 (this work) employs structural scaling, where increasing $t_{si,p}$ enhances the effective drive strength of P1, P2, P3, and P4 devices without altering intrinsic mobility. This results in improved I_{ON}, a switching point close to $V_{DD}/2$, and τ_{PHL}/τ_{PLH} ~1, demonstrating near-symmetric inverter operation. These results clearly demonstrate that structural scaling ($t_{si,p}$ = 2× $t_{si,n}$) provides a more effective and physically consistent approach for achieving balanced inverter performance compared to mobility enhancement, which introduces asymmetry despite marginal current improvement.

5.4.3 Effect of Temperature on CMOS Inverter Performance

In this subsection, the impact of temperature on Inv1, Inv2, Inv3, and Inv4 is analyzed to understand the insights into their performance under varying temperature conditions. The transient response of CMOS inverters (Inv1, Inv2, Inv3, and Inv4) is evaluated by varying the temperature from 300 K to 400 K with 10 ps τ_{rise} and τ_{fall}.

It is evident from Fig. 5.14 (a), (b), (c), and (d) that increasing temperature (300 K to 400 K) results in slower output transitions, indicating an increase in τ_P for all inverter configurations. In any JL-NWFET, the dominant degradation mechanism is phonon scattering, due to which carrier mobility decreases approximately proportional to $T^{-3/2}$ [117]. This reduction in mobility directly lowers the I_{ON}, thereby increasing the charging and discharging time of the load capacitance and degrading switching speed.

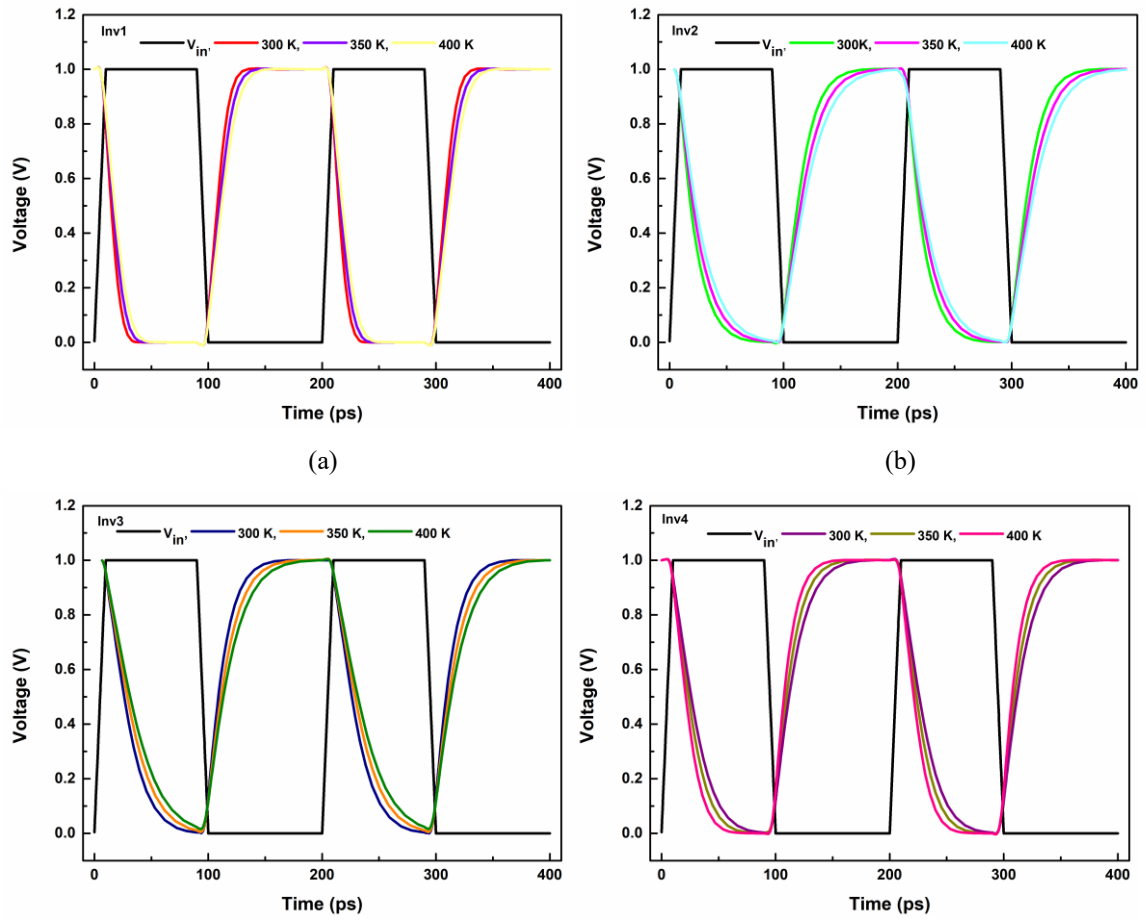


Fig. 5.14 Transient characteristics of the CMOS inverters (a) Inv1, (b) Inv2, (c) Inv3, and (d) Inv4 for different temperatures

Table 5.6. Temperature Coefficient of τ_p for CMOS inverter Inv1, Inv2, Inv3, and Inv4

CMOS Inverters	**τ_P (ps) ($\tau_{rise} = \tau_{fall}$ = 10 ps)**			**Temperature Coefficient (K^{-1})**
	300 K	**350 K**	**400 K**	
Inv1	11.25	13.35	15.71	3.96×10^{-3}
Inv2	10.85	13.05	15.59	4.36×10^{-3}
Inv3	13.9	17.34	20.74	4.92×10^{-3}
Inv4	18.38	22.33	27.99	5.22×10^{-3}

The temperature coefficient of τ_p for CMOS inverters Inv1, Inv2, Inv3, and Inv4 is summarized in Table 5.6. Inverters Inv1, Inv2, Inv3, and Inv4 exhibit a positive temperature coefficient, confirming that τ_P increases with temperature due to mobility degradation. Among all configurations, Inv1 exhibits the lowest temperature coefficient, indicating superior thermal stability, compared to Inv2, Inv3, and Inv4 due to the incorporation of DMG, GSS, and CS architecture, which enhance current drivability and mitigate leakage current, making it comparatively more robust against temperature variations than Inv2, Inv3, and Inv4.

5.4.4 Effect of Load Capacitance on CMOS Inverter Performance

The impact of load capacitance (C_L) on the τ_P of CMOS inverters (Inv1, Inv2, Inv3, and Inv4) is evaluated by varying C_L from 1 fF to 10 fF and is shown in Fig. 5.15. The results clearly show that the τ_P increases with C_L for all inverter configurations. This behavior is due to the increased charging/discharging time associated with higher capacitive loading. Among all architectures, Inv1 and Inv2 exhibit the lowest delay, indicating superior drive capability, whereas Inv3 and Inv4 show significantly higher delay, particularly at larger C_L, due to reduced electrostatic control and drive strength. At low C_L (1-3 fF), the delay difference among Inv1, Inv2, Inv3, and Inv4 is relatively small.

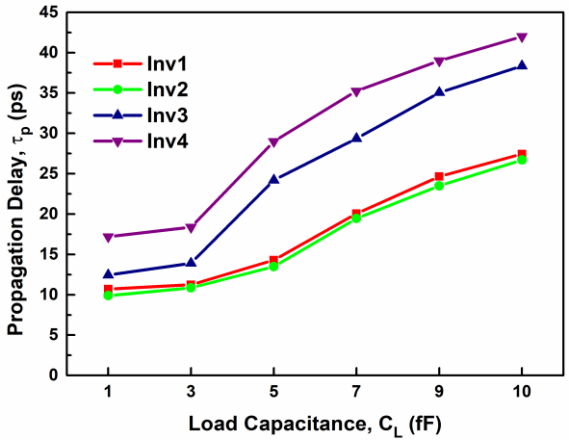


Fig. 5.15 Propagation delay of the CMOS inverters Inv1, Inv2, Inv3, and Inv4 for different load capacitances

As C_L increases beyond 3 fF, the delay degradation becomes more pronounced, especially for Inv3 and Inv4, highlighting their limited current driving capability. It is also observed that the difference in τ_P between Inv1 and Inv2 is relatively small; however, Inv2 exhibits slightly lower delay compared to Inv1. This can be attributed to the absence of the spacer in D2, which reduces the intrinsic parasitic resistance and capacitance, thereby slightly improving the switching speed. In contrast, the presence of the spacer in D1, while beneficial for electrostatic control, introduces additional intrinsic delay.

5.5 CIRCUIT LEVEL RING OSCILLATOR ANALYSIS

The ring oscillator (RO) are widely employed to evaluate the dynamic performance of nanoscale devices at the circuit level, as their oscillation frequency directly reflects the cumulative delay of cascaded inverter stages. In this section, the RO circuits R1, R2, R3, and R4 are implemented using the corresponding CMOS inverters Inv1, Inv2, Inv3, and Inv4, respectively, to further validate the device and inverter-level performance under realistic

switching conditions. The oscillation frequency (f_{osc}) of an N-stage RO is determined by the propagation delay of the individual inverter stages and is expressed as [173]

$$f_{osc} = \frac{1}{2N\tau_P} \tag{5.20}$$

$$f_{osc} = \frac{\mu_e' C_{ox} \pi \left(t_{si} - t_{core}\right)}{NC_L L_C \left\{ \begin{array}{l} \dfrac{1}{\left(V_{OH} - V_{T,n}\right)} \left[\dfrac{2V_{T,n}}{\left(V_{OH} - V_{T,n}\right)} + \ln\left(\dfrac{4\left(V_{OH} - V_{T,n}\right)}{V_{OH} + V_{OL}} - 1 \right) \right] \\ + \dfrac{1}{\left(V_{OH} - V_{OL} - \left|V_{T,p}\right|\right)} \left[\dfrac{2\left|V_{T,p}\right|}{\left(V_{OH} - V_{OL} - \left|V_{T,p}\right|\right)} + \ln\left(\dfrac{2\left(V_{OH} - V_{OL} - \left|V_{T,p}\right|\right)}{V_{OH} - V_{50\%}} - 1 \right) \right] \end{array} \right\}} \tag{5.21}$$

where τ_p denotes the average propagation delay of a single inverter stage and N represents the total number of inverter stages in the RO. In the present work, a 3-stage ring oscillator ($N = 3$) composed of identical inverters is considered.

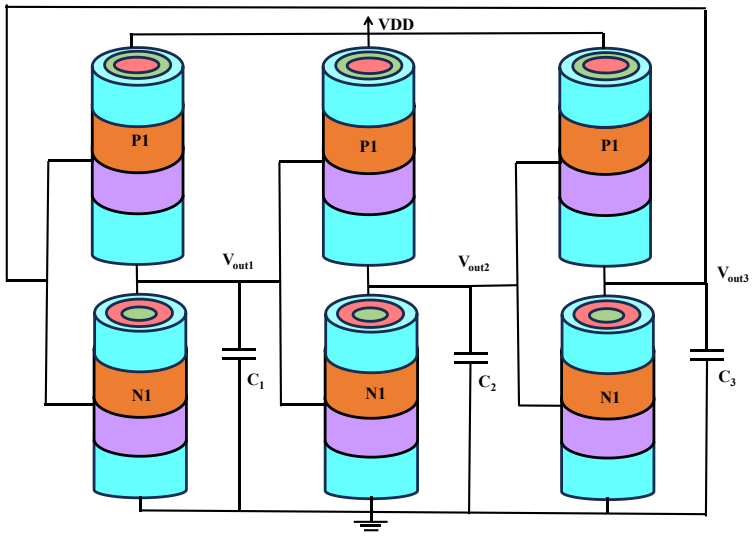


Fig. 5.16 Structure of a 3-stage ring oscillator (R1) realized using CMOS inverter Inv1

A 3-stage RO circuit implemented using inverter Inv1 is illustrated in Fig. 5.16. The load capacitor of $C_1 = C_2 = 3$fF, and $C_3 = 6$fF is taken into account [172, 174]. The corresponding transient oscillation waveforms of R1, R2, R3, and R4 are presented in Fig. 15.7 (a), (b), (c), and (d), respectively. It is observed that the oscillation does not commence immediately upon application of the supply voltage; instead, a finite startup interval is required before sustained oscillations are established. This interval, commonly referred to as the warm-up time, corresponds to the period during which the circuit transitions from its initial condition to steady-state oscillatory operation [175].

After the warm-up time, stable oscillations are generated by the ring oscillator. The outputs of the different stages are phase-shifted by π/N (for an N-stage RO), maintaining equal magnitude while being uniformly distributed in phase. However, due to device-level variations, thermal effects, and noise sources, each inverter stage introduces small timing fluctuations, which accumulate and manifest as jitter in the overall oscillation [175]. This jitter represents the cycle-to-cycle variation in the oscillation period and serves as a key indicator of frequency stability.

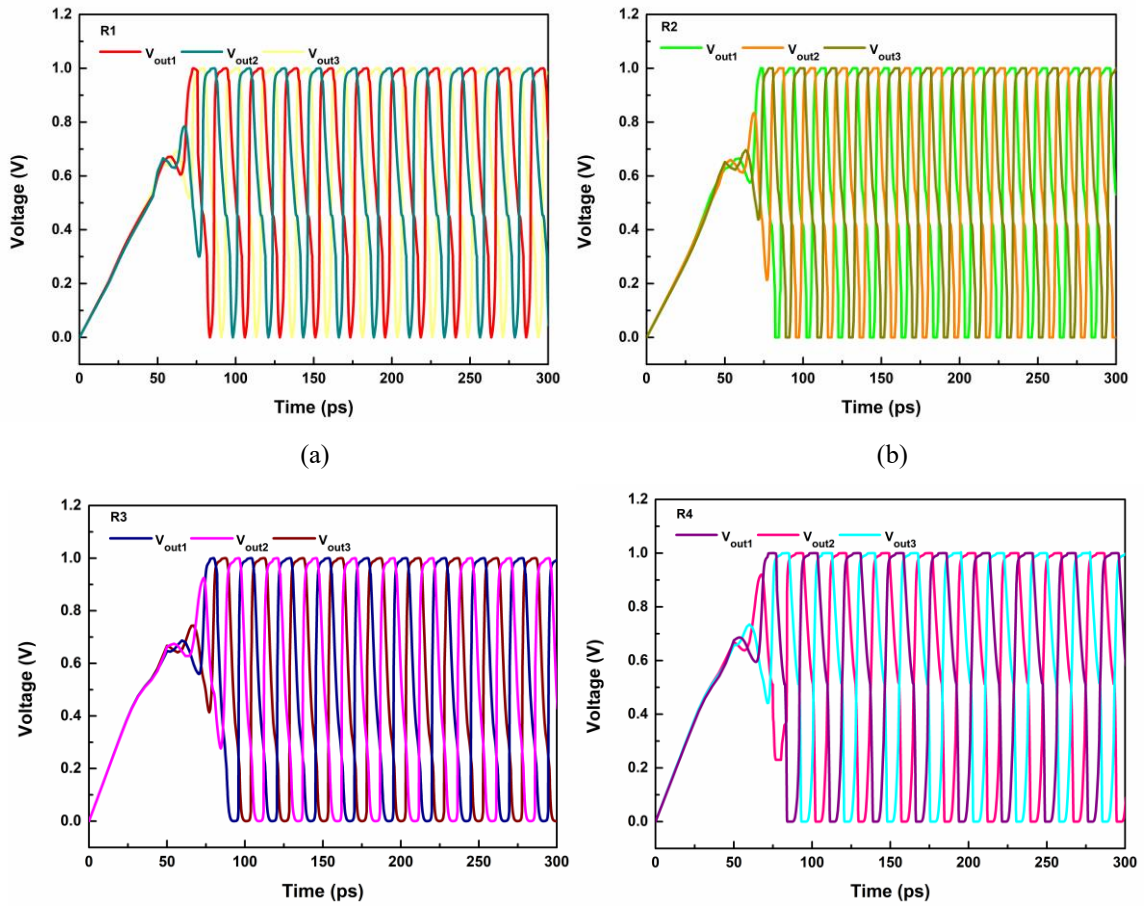


Fig. 5.17 The 3-stage RO output characteristics of (a) R1, (b) R2, (c) R3, and (d) R4

Table 5.7. Comparison of RO R1, R2, R3, and R4 based on f_{osc}, Warm-uptime, and jitter

RO	f_{osc} (GHz)	Warm-up time (ps)	Jitter (ps)
R1	14.81	76.52	0.001
R2	15.36	77.77	0.002
R3	11.99	82.6	0.003
R4	9.06	84.05	0.005

The performance metrics including oscillation frequency, warm-up time, and jitter, are summarized in Table 5.9. The extracted oscillation frequencies f_{osc} are 14.81 GHz, 15.36 GHz, 11.99 GHz, and 9.06 GHz for R1, R2, R3, and R4, respectively. These results confirm that all RO configurations operate in the GHz frequency range, thereby demonstrating the high-speed

switching capability and suitability of the proposed nanoscale devices for high-frequency digital applications. Among the studied structures, R2 achieves the highest oscillation frequency due to its minimum inverter propagation delay, which arises from reduced gate capacitance and enhanced switching speed. The R1 exhibits a slightly lower oscillation frequency than R2; however, it maintains stable oscillation behavior while benefiting from reduced leakage current and improved electrostatic control.

R3 and R4 show comparatively lower oscillation frequencies as a consequence of increased propagation delay and degraded electrostatic integrity. Furthermore, R1 exhibits the lowest warm-up time (76.52 ps) and the minimum jitter (0.001 ps), indicating superior frequency stability and faster startup. R2 shows comparable warm-up time with slightly higher jitter, whereas R3 and R4 exhibit increased warm-up time and larger jitter values, reflecting reduced stability and higher delay variability. The lower jitter in R1 can be attributed to reduced self-heating and improved electrostatic control, which minimizes cycle-to-cycle timing fluctuations. Table 5.7 presents the comparison between analytically derived and TCAD-simulated values of propagation delay and oscillation frequency for the proposed device. The analytical model predicts propagation delay with reasonable accuracy, showing slight underestimation compared to simulation results.

Table 5.8. Comparison between simulated and analytical values of τ_p and f_{osc} for Inv1 (based on proposed D1)

Parameters	Simulated Value	Analytical Value
τ_{PLH} (ps)	10.62	9.95
τ_{PHL} (ps)	11.88	11.10
τ_P (ps)	11.25	10.52
f_{osc} (GHz)	14.81	15.84

Table 5.8 shows the normalized sensitivities of τ_P ($S_{\tau P}$) and f_{osc} (S_{fosc}) taking t_{core} =5nm as the baseline condition using an analytical model. It is observed that increasing the t_{core} results in a significant increase in τ_P and a corresponding decrease in f_{osc}. Conversely, reducing t_{core} improves delay and frequency, but the improvement is relatively moderate. This behavior indicates that device performance is sensitive to variations in t_{core}, particularly for higher values. Hence, t_{core} = 5 provides an optimal trade-off between speed and overall device performance.

Table 5.9. Sensitivity Analysis of τ_P and f_{osc} with respect to core thickness

t_{core} (nm)	τ_P (ps)	$S_{\tau_P} = \frac{\Delta\tau_P/\tau_P}{\Delta t_{core}/t_{core}}$	f_{osc} (GHz)	$S_{\tau_P} = \frac{\Delta f_{osc}/f_{osc}}{\Delta t_{core}/t_{core}}$
3	9.98	-0.128	16.70	-0.136
5	10.52	0	15.84	0
7	11.25	0.174	14.81	-0.163

Fig. 5.18 illustrates the variation of f_{osc} with supply voltage (V_{DD}) for all RO configurations. It is observed that f_{osc} increases monotonically with V_{DD}, which is consistent with the analytical Eqn. 5.21, As V_{DD} increases, the I_{ON} improves, leading to a reduction in τ (Eqn. 5.1) and consequently an increase in f_{osc}. Among all configurations, R2 exhibits the highest f_{osc} across the entire V_{DD} range due to its reduced intrinsic capacitance and faster switching, followed closely by R1, while R3 and R4 show comparatively lower frequencies due to increased delay and weaker electrostatic control.

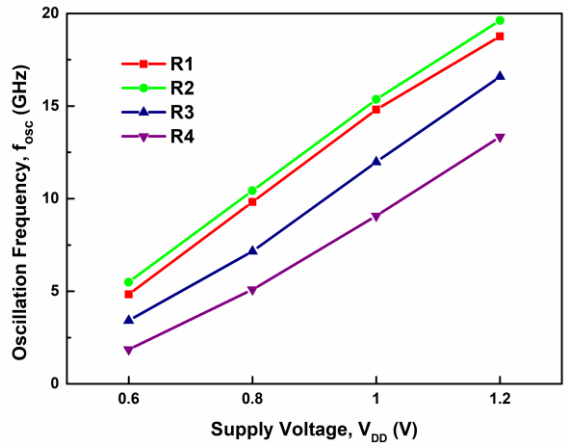


Fig. 5.18 Oscillation frequency of RO R1, R2, R3, and R4 for different supply voltages

In terms of startup reliability, all RO fail to sustain oscillation at 0.5 V, indicating that the minimum V_{DD} lies between 0.5 V and 0.6 V. At $V_{DD} \geq 0.6$ V, oscillations are successfully initiated for all configurations; however, R1 demonstrates more reliable and faster startup compared to R2, whereas R3 and R4 exhibit delayed and less stable oscillations, particularly near the V_T. This behavior is attributed to the insufficient loop gain at lower V_{DD}, where the reduced drive current is unable to overcome losses in the ring, preventing sustained oscillation.

Overall, the RO analysis corroborates the CMOS inverter-level delay results, demonstrating that R2 (based on D2) is well-suited for ultra-high-speed applications due to its slightly higher f_{osc}. In contrast, R1 (based on D1) provides a balanced trade-off between f_{osc}, startup reliability, leakage suppression, and robust electrostatic control. Although R1 exhibits marginally lower speed compared to R2, its improved stability and reliability under varying operating conditions make it a more suitable candidate for low-power, high-performance integrated circuit applications.

5.5.1 Effect of Temperature and Self-Heating Effect on Ring Oscillator

The variation of f_{osc} with temperature is depicted in Fig. 5.19, where f_{osc} decreases with increasing temperature for all RO configurations considered in this work. This degradation is

primarily attributed to reduced carrier mobility and increased τ_p of the Inv1, Inv2, Inv3, and Inv4 inverters at elevated temperatures.

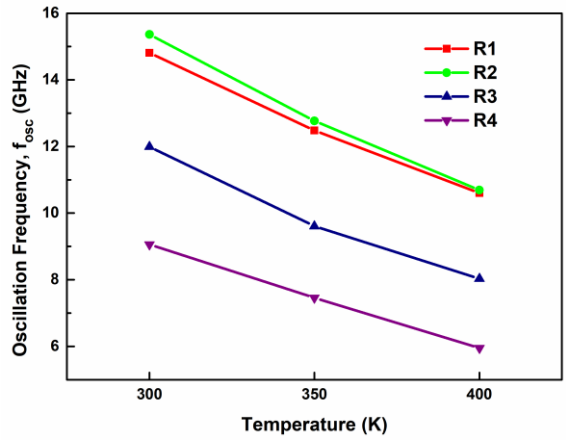


Fig. 5.19 Oscillation frequency of RO R1, R2, R3, and R4 for different temperatures

Table 5.10. Temperature Coefficient of f_{osc} for RO R1, R2, R3, and R4

RO	f_{osc}			Temperature Coefficient (K^{-1})
	300 K	350 K	400 K	
R1	14.81	12.48	10.6	-2.84×10^{-3}
R2	15.36	12.77	10.69	-3.04×10^{-3}
R3	11.99	9.61	8.03	-3.30×10^{-3}
R4	9.06	7.46	5.95	-3.43×10^{-3}

From Table 5.10, the temperature coefficient of f_{osc} is negative for all R1, R2, R3, and R4, confirming the expected inverse dependence of frequency on temperature. Among the RO, R1 exhibit lower magnitude of temperature coefficient, indicating better thermal stability, compared to R2, R3, and R4, with R4 exhibiting the worst temperature sensitivity. Specifically, R1 (based on D1) shows a relatively smaller reduction in frequency (from 14.81 GHz at 300 K to 10.6 GHz at 400 K) compared to R2 (from 15.36 GHz to 10.69 GHz), highlighting the superior robustness of the proposed architecture. The Self-Heating Effect (SHE) induced temperature rise (ΔT) is quantified as the difference between the maximum lattice temperature (T_{max}) during operation and the ambient temperature ($T_{ambient}$) and is given as [176]

$$\Delta T = T_{\max} - T_{ambient} \tag{5.22}$$

Figure 5.20 portrays the global device temperature during RO operation. The T_{max} for R1-R4 are 312.23 K, 313.31 K, 315.67 K, and 318.54 K, respectively, and corresponding ΔT values are 12.23 K, 13.31 K, 15.67 K, and 18.54 K, respectively. This temperature rise directly impacts carrier transport through mobility degradation, leading to an increase in τ_p and a consequent reduction in f_{osc}. Furthermore, R1 (based on D1) exhibits the lowest ΔT (12.23 K) and correspondingly the smallest reduction in frequency (14.81 GHz to 10.6 GHz), whereas R4

(based on D4) shows the highest ΔT (18.54 K) along with the largest degradation in f_{osc} (9.06 GHz to 5.95 GHz). The RO (R2 and R3) based on intermediate structures (D2 and D3) follow a similar trend consistent with their respective temperature rises.

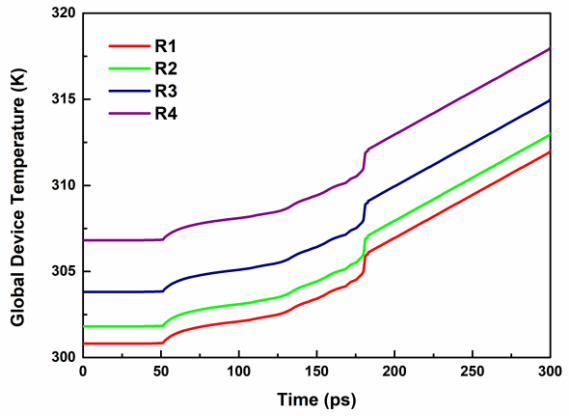


Fig. 5.20 Global device temperature during RO operation

These results confirm that the proposed D1 architecture maintains lower self-heating, reduced delay sensitivity, and better frequency stability compared to the conventional D4, thereby retaining its performance advantage even under elevated thermal operating conditions. A comparison between D1 and D2 further reveals a trade-off, wherein D2 exhibits slightly higher f_{osc} due to reduced τ_p while D1 demonstrates lower self-heating and improved thermal stability, making it a more reliable choice for operation under elevated temperature and thermal stress conditions.

5.5.2 Effect of Load Capacitance on Ring Oscillator

Figure 5.21 demonstrates the impact of C_L on the f_{osc} of RO (R1, R2, R3, and R4) by varying C_L from 1 fF to 10 fF. The results clearly show that f_{osc} decreases with increasing C_L for all configurations. This behavior is attributed to the fact that f_{osc} is inversely proportional to τ_p which increases with higher capacitive loading, as discussed in subsection 5.5.2. Among all architectures, R1 and R2 exhibit higher f_{osc}, indicating faster switching characteristics, whereas R3 and R4 show significantly lower f_{osc}, particularly at larger C_L, due to their degraded electrostatic control. At low C_L (1–3 fF), the difference in f_{osc} among R1, R2, R3, and R4 is relatively small.

However, as C_L increases beyond 3 fF, the degradation in f_{osc} becomes more pronounced, especially for R3 and R4, highlighting their limited ability to drive larger loads. It is also observed that the difference in f_{osc} between R1 and R2 is relatively small; however, R2 exhibits slightly higher frequency compared to R1. This can be attributed to the absence of the spacer in D2, which reduces intrinsic parasitic resistance and capacitance, thereby improving

switching speed. In contrast, the presence of the spacer in D1 introduces additional intrinsic delay, slightly reducing the f_{osc}.

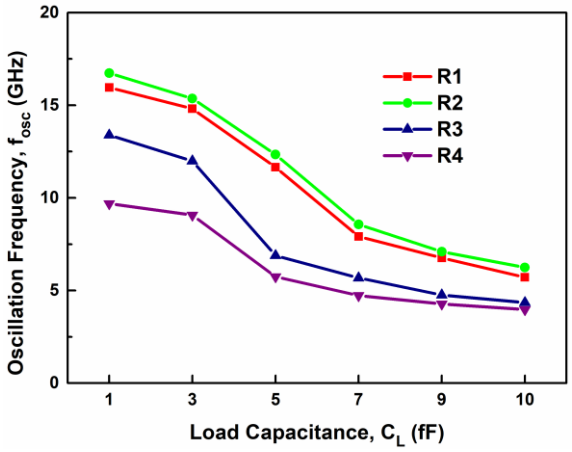


Fig. 5.21 Oscillation frequency of RO R1-R4 for different load capacitance

Table 5.11. State-of-the-art benchmarking of the proposed I-JL-NWFET against previously reported work

Ref	Experimental /Simulation work	Technology node, L_C (nm)		f_{osc} (GHz)	τ_p (ps)	*PDP* *(aJ)*	*EDP* (10^{-30} *Js*)	NM	
		n-type	p-type					NM_H (V)	NM_L (V)
[170]	Experimental	775	275	-	67	-	-	0.53	0.41
[171]	Simulation	30	30	-	1	-	-	-	-
[172]	Simulation	800	800	3.17	52.5	-	-	-	-
[177]	Simulation	55	45	-	2.2	-	-	0.43	0.45
[178]	Simulation	10	10	19.2	5.21	-	-	-	-
[179]	Simulation	130	130	-	0.8	-	-	-	-
[180]	Simulation	20	20	0.91	0.29				
This Work	Simulation	30	30	14.81	11.25	547.87	6163.59	0.355	0.515

Furthermore, a comparative analysis is provided in Table 5.11 to clearly position the proposed work relative to prior art, highlighting its advantages in terms of improved speed, reduced delay, and enhanced energy efficiency. The comparison demonstrates the effectiveness and competitiveness of the proposed device architecture.

5.6 SUMMARY OF THE IMPORTANT RESULTS

The present chapter investigates the circuit-level performance of I-JL-NWFET incorporating CS, DMG and GSS. The analysis is carried out to evaluate how the device-level improvements achieved in the proposed I-JL-NWFET translate into circuit-level benefits in terms of switching characteristics, delay, leakage suppression, and oscillation behavior. Four different device configurations are considered, and their corresponding n-type, p-type at the device level,

CMOS inverter, and RO performances are systematically analyzed. The important outcomes of the chapter are summarized below.

- The proposed N1 (based on I-JL-NWFET comprising CS + DMG + GSS) achieves the lowest I_{OFF} of 9.55 × 10^{-9} µA, which is significantly lower than N2, N3, and N4 This confirms that the combined CS, DMG, and GSS architecture provides the most effective suppression of I_{OFF} and improved electrostatic integrity.
- Among the device architectures, the proposed N2 (comprising CS + DMG) exhibits the lowest τ of 1.40 ps, while N1 (based on I-JL-NWFET comprising CS + DMG + GSS) shows a closely comparable value of 1.43 ps. Both proposed N1 and N2 outperform the reported devices N3 and N4, which exhibit τ of 2.84 ps and 3.04 ps, respectively. This indicates that the proposed architecture maintains high-speed operation with only a marginal delay penalty in exchange for stronger leakage suppression.
- The proposed Inv1 (based on I-JL-NWFET comprising CS + DMG +GSS) demonstrates the highest noise margins, with NM_L = 0.515 V and NM_H = 0.355 V. These values are higher than those of Inv2 (0.466 V, 0.350 V), Inv3 (0.435 V, 0.320 V), and Inv4 (0.420 V, 0.275 V), confirming superior switching robustness and static stability.
- Under non-ideal input conditions, Inv2 (comprising CS + DMG) exhibits the lowest average propagation delay τ_P of 10.85 ps, whereas Inv1 (based on I-JL-NWFET comprising CS + DMG +GSS) achieves 11.25 ps, indicating only a marginal delay penalty despite improved leakage control. Both proposed configurations outperform Inv3 and Inv4, which show delays of 13.90 ps and 18.38 ps, respectively.
- The average p_{avg} of Inv1, Inv2, Inv3, and Inv4 is 42.70 µW, 40.61 µW, 38.70 µW, and 35.52 µW, respectively. Although Inv1 consumes slightly higher power, this increase is accompanied by substantial improvements in leakage suppression, and noise margin.
- Inv2 provides the best energy efficiency, with the lowest PDP of 440.61 aJ and EDP of 4780.61 × 10^{-30} Js. In comparison, Inv1, Inv3, and Inv4 exhibit PDP values of 480.87 aJ, 537.93 aJ, and 652.85 aJ, and EDP values of 5404.10 × 10^{-30} Js, 7477.22 × 10^{-30} Js, and 11999.52 × 10^{-30} Js, respectively.
- Over the temperature range of 300-400 K, the proposed Inv1 exhibits the lowest temperature coefficient of τ_P of 3.96 × 10^{-3} K^{-1}, compared with Inv2 (4.36 × 10^{-3} K^{-1}), Inv3 (4.92 × 10^{-3} K^{-1}), and Inv4 (5.22 × 10^{-3} K^{-1}). This demonstrates the superior thermal robustness of Inv1 resulting from the combined effect of CS, DMG, and GSS.

- The analytical study shows that increasing t_{core} causes a significant increase in τ_P and a corresponding reduction in f_{osc}. Conversely, reducing t_{core} improves speed and f_{osc}. The analysis identifies t_{core} = 5 nm as the optimum design point, providing the best trade-off between delay, f_{osc}, and overall circuit performance.
- The proposed R1 exhibits the lowest warm-up time of 76.52 ps and the minimum jitter of 0.001 ps. In comparison, R2, R3, and R4 show warm-up times of 77.77 ps, 82.60 ps, and 84.05 ps, and jitter values of 0.002 ps, 0.003 ps, and 0.005 ps, respectively. These results confirm faster startup and superior frequency stability for the R1.
- The extracted oscillation frequencies of the three-stage ring oscillators are 14.81 GHz, 15.36 GHz, 11.99 GHz, and 9.06 GHz for R1, R2, R3, and R4, respectively. Although R2 (comprising CS + DMG) achieves the highest f_{osc}, the proposed R1 (based on I-JL-NWFET comprising CS + DMG +GSS) maintains comparable frequency while offering improved stability and startup characteristics.
- In temperature-dependent analysis, R1 shows the smallest magnitude of negative temperature coefficient (-2.84×10^{-3} K^{-1}) compared with R2 (-3.04×10^{-3} K^{-1}), R3 (-3.30×10^{-3} K^{-1}), and R4 (-3.43×10^{-3} K^{-1}). It also exhibits the lowest temperature rise of 12.23 K, whereas R2, R3, and R4 show 13.31 K, 15.67 K, and 18.54 K, respectively, confirming better thermal stability.
- Supply voltage analysis shows that all RO configurations fail to sustain oscillation at 0.5 V, indicating that the minimum operating supply voltage lies between 0.5 V and 0.6 V.

The present chapter demonstrates that the proposed I-JL-NWFET based CMOS circuits provide a balanced circuit-level solution by combining improved electrostatic integrity, strong leakage suppression, robust noise margins, enhanced thermal stability, and stable high-frequency oscillation behavior. Although the inclusion of the GSS introduces a small delay penalty due to increased fringing capacitance, this drawback is effectively compensated by improved switching robustness and reduced leakage current. The results establish the suitability of the proposed I-JL-NWFET for low-power, high-frequency nanoscale CMOS applications. The future work may focus on experimental circuit-level validation, fabrication-oriented variability analysis, and assessment of larger digital building blocks to further establish the practical applicability of the proposed architecture.

CHAPTER - 6

CONCLUSION, FUTURE SCOPE, AND SOCIAL IMPACT

The present research work is focused on the design and analysis of I-JL-NWFET based on structural modifications incorporating the cumulative benefit of CS, DMG, and GSS through TCAD simulation. Additionally, the simulation results are validated by the analytical modeling of the I-JL-NWFET. The proposed device is further utilized to detect GI cancer through the detection of the p53 biomarker. Also, the proposed device demonstrates its potential in electronics applications by realizing a CMOS inverter and a 3-stage ring oscillator. In this chapter, important findings and outcomes of the proposed work are summarized.

This chapter is divided into three sections. Section 6.1 incorporates the overall conclusions of the research work. Furthermore, Section 6.2 discusses possible directions for future research, while Section 6.3 highlights the potential social impact of the proposed work.

6.1 CONCLUSION

The research work begins with the understanding of the evolution from planar FET to cylindrical JL-NWFET. The literature review reveals that the performance enhancement of JL-NWFETs has evolved progressively through continuous structural innovation and optimization strategies. Over the years, researchers have explored various device architectures, including DMG, TMG, CS, GSS, FE, GC, and hybrid configurations. It is observed that hybrid device architectures generally provide superior performance compared to single-structure designs by utilizing the cumulative advantages of multiple engineering techniques. Furthermore, the analytical modeling approaches developed for cylindrical JL-NWFETs demonstrate the importance of accurate electrostatic analysis for understanding nanoscale device behaviour.

In the biomedical domain, FET-based biosensors have shown strong potential for biomolecule detection, yet disease-specific applications using cylindrical JL-NWFET architectures remain comparatively limited. Similarly, circuit-level investigations confirm the applicability of advanced JL-NWFET structures in digital and RF electronics applications. However, comprehensive research work integrating device optimization, analytical validation, biomedical sensing, and circuit-level realization within a unified framework is still limited. Eventually, the literature review establishes that although significant advancements have been achieved in improving JL-NWFET performance, further research is still required to investigate

whether a single optimized JL-NWFET architecture can simultaneously support both biomedical sensing and electronic circuit applications with balanced and reliable performance.

The present research work focuses on the design, analysis, modeling, biomedical sensing application, and circuit-level investigation of the proposed Improved Junctionless Nanowire Field Effect Transistor (I-JL-NWFET). By identifying the major limitations associated with conventional JL-NWFETs, particularly the degradation caused by incomplete volume depletion, and proposes a novel architecture incorporating CS, DMG, and GSS structures improvement strategies. Through systematic TCAD-based investigation, the proposed architecture demonstrates improved electrostatic control, 23.1% increase in I_{ON}, a reduction by an order of 5 in I_{OFF}, and 88% improvement in SS.

Furthermore, the comparative analysis of the proposed device D1 (JL-NWFET + p-type CS + DMG + GSS) and D2 (JL-NWFET + p-type CS + DMG), with pre-existing devices D3 (JL-NWFET + p-type CS + SMG), D4 (JL-NWFET + intrinsic CS), and D5 (JL-NWFET), confirms the superiority of the proposed D1 in terms of electrical and analog/RF. The optimization of structural parameters reveals that the optimum value of t_{core} is achieved when it is maintained at half of t_{si}, with SiO_2 as the gate oxide and HfO_2 as the spacer material, while the optimum spacer length is found to be equal to the $L_{S/D}$ of 25 nm. Furthermore, the L_C and t_{si} of the I-JL-NWFET are optimized to 30 nm and 10 nm, respectively, thereby establishing the importance of proper device dimensioning and dielectric engineering in achieving balanced performance between leakage suppression, current drivability, and thermal reliability.

To further validate the electrostatic behaviour of the proposed I-JL-NWFET, a comprehensive analytical modeling is developed using the surface potential approach in cylindrical coordinates. Initially, the analytical models are formulated for two intermediate proposed devices (JL-NWFET + CS + DMG + GSS) and (JL-NWFET + CS + GSS), and then the final I-JL-NWFET structure. The analytical framework is established by solving the two-dimensional Poisson's equation in cylindrical coordinates using the surface potential approach. The developed analytical framework successfully captures the potential distribution, electric field behaviour, threshold voltage variation, and current transport mechanism of the proposed devices.

The analytical solutions exhibit close agreement with TCAD simulation results over a wide range of device parameters. The analysis further demonstrates that t_{core}, t_{si}, L_C, t_{si} and spacer permittivity play crucial roles in suppressing I_{OFF}, reducing DIBL, and improving subthreshold characteristics. Moreover, the analytical investigation confirms that optimum performance is

achieved when the t_{core} is maintained at half of t_{si}, with the incorporation of DMG for effective DIBL reduction and HfO_2 as the spacer material. In addition to providing a deeper physical understanding of I-JL-NWEET, the analytical framework also establishes effective design guidelines for future nanoscale transistor optimization while reducing dependence on computationally intensive numerical simulations.

The proposed I-JL-NWFET is further extended toward biomedical sensing applications through the development of a label-free biosensor for the detection of the p53 biomarker associated with GI cancer. The sensing mechanism is established through interface charge modulation within the nanocavity region, enabling effective differentiation between healthy and diseased biomarker concentrations through variations in the electrical characteristics of the device. The highest sensitivity is achieved when the nanocavity is positioned near the source side of the channel, while the optimum L_{cav} is found to be half of the L_C. Furthermore, the biosensor structure is systematically optimized by analysing the influence of nanocavity position L_C, t_{core}, cavity occupancy, and temperature on sensing performance.

The investigation demonstrates that proper optimization of structural parameters significantly enhances the sensitivity and discrimination capability of the proposed biosensor, enabling effective differentiation between healthy and diseased samples. Under the optimized device configuration, for a p53 concentration of 1.62 ng/ml corresponding to the maximum diseased condition, the biosensor achieves an I_{ON}/I_{OFF} sensitivity of 4.60×10^9, V_T sensitivity of 0.69, and SS sensitivity of 0.78. Similarly, for a p53 concentration of 0.27 ng/ml corresponding to the maximum healthy condition, the device exhibits an I_{ON}/I_{OFF} sensitivity of 2.15×10^7, V_T sensitivity of 0.49, and SS sensitivity of 0.88, thereby confirming the highly sensitive detection capability of the proposed biosensor toward clinically relevant p53 concentrations.

Additionally, the incorporation of practical sensing considerations by including RSH effects to evaluate the biosensor performance under non-ideal binding conditions. Additionally, the successful integration of the proposed biosensor with CSA read-out circuitry demonstrates the capability of converting biomolecule-induced current variations into measurable voltage responses suitable for practical sensing systems. The analysis confirms that the proposed I-JL-NWFET based biosensor possesses high sensitivity, strong discrimination capability between healthy and diseased samples, and reliable sensing behaviour for label-free biomarker detection.

Finally, the circuit-level applicability of the proposed I-JL-NWFET is investigated through CMOS inverter and 3-stage RO implementations. The comparative analysis of n-type devices

N1, N2, N3, and N4 and p-type devices P1, P2, P3, and P4, corresponding to proposed (JL-NWFET + CS + DMG + GSS) and D2 (JL-NWFET + CS + DMG), with pre-existing devices D3 (JL-NWFET + CS + SMG) and D4 (JL-NWFET), effectively translates into improved circuit-level performance. The static analysis of CMOS inverter reveals that the proposed Inv1 (based on device N1 and P1) exhibits the highest noise margin, strongest leakage suppression, and lowest positive temperature coefficient among all investigated configurations. Although the inclusion of GSS in Inv1 slightly increases the τ, comparable to Inv2 (based on device N2 and P2) and significantly better than the pre-existing Inv3 (based on device N3 and P3) and Inv4 (based on device N4 and P4). Additionally, the dynamic analysis further reveals that the additional fringing capacitance introduced by GSS causes a marginal increase in τ_P, p_{avg}, PDP, and EDP for Inv1 compared to Inv2.

The Inv2 exhibits the lowest PDP of 440.61 aJ, slightly lower than that in Inv1 with 480.87 aJ, while both outperform pre-existing Inv3 and Inv4 with PDP of 537.93 aJ, and 652.85 aJ, respectively. The RO analysis reveals that although R2 (realized using Inv2) achieves the highest f_{osc} of 15.36 GHz due to the lowest τ_P observed in the corresponding CMOS inverter, R1 (realized using Inv1) demonstrates more robust and stable ring oscillator performance. R1 exhibits the lowest warm-up time of 76.52 ps and minimum jitter of 0.001 ps, confirming faster startup behaviour and superior frequency stability compared to pre-existing R3 (realized using Inv3), and R4 (realized using Inv4). Furthermore, in temperature-dependent analysis, R1 shows the smallest negative temperature coefficient of -2.84×10^{-3} K^{-1} along with the lowest temperature rise of 12.23 K, thereby demonstrating enhanced thermal stability and reliable high-frequency operation under varying thermal conditions.

To conclude, the present research work confirms that the I-JL-NWFET incorporating CS, DMG, and GSS is more suitable for biomedical sensing applications due to its superior leakage suppression, enhanced sensitivity, improved stability, and robust thermal performance. However, the inclusion of GSS introduces additional fringing capacitance, leading to a slight increase in propagation delay, PDP, and EDP. Consequently, for digital electronic applications requiring higher speed and better energy efficiency, I-JL-NWFET incorporating CS and DMG without GSS provides a more balanced trade-off between performance and power consumption. Therefore, the present work establishes that the optimized device architecture should be selected based on the target application requirements.

6.2 FUTURE SCOPE

The present work addresses an approach related to improving the JL-NWFET for biomedical and electronics applications through TCAD simulations. However, there are multiple aspects that still need attention, which are ignored during the analysis. The incorporation of physical effects during simulation, such as quantum confinement, interface trap charges, and trap-induced degradation, may provide a more realistic understanding of nanoscale device behaviour. In the proposed work, during temperature analysis, it is observed that as temperature increases, I_{ON} decreases and I_{OFF} increases; however, I-JL-NWFET has the least performance degradation compared to conventional JL-NWFET. Therefore, the current research work can be further extended by exploring advanced semiconductor channel materials with high thermal properties to improve device performance at high temperatures.

The future research may focus on the experimental fabrication and characterization of the proposed I-JL-NWFET and its associated biosensor and circuit architectures to validate the simulated and analytical findings under practical operating conditions. In the biomedical domain, future work may include other disease detection and the development of portable point-of-care diagnostic platforms. Additionally, larger digital building blocks such as SRAM cells, logic circuits, and arithmetic units may be investigated to evaluate the practical large-scale applicability of the proposed I-JL-NWFET architecture.

6.3 SOCIAL IMPACT

The proposed I-JL-NWFET architecture and its associated applications have significant potential to contribute toward the advancement of energy-efficient and sustainable semiconductor technologies. The improved electrostatic integrity, reduced leakage current, enhanced thermal stability, and low-power operation achieved by the proposed device can support the development of environmentally friendly electronic systems with reduced energy consumption. Such improvements are highly beneficial for modern portable electronics, communication systems, computing platforms, and intelligent devices that demand compact size, high performance, and low power dissipation. Furthermore, the development of accurate analytical models contributes to semiconductor education, research advancement, and efficient design optimization of future nanoscale devices.

The biomedical sensing application developed in this research work also possesses strong societal relevance by enabling rapid, label-free, and highly sensitive detection of biomarkers

associated with GI cancer. The early-stage disease diagnosis can significantly improve treatment outcomes, patient survival rates, and healthcare accessibility. The compact and low-power nature of the proposed biosensor may facilitate the development of affordable portable diagnostic systems suitable for real-time health monitoring and point-of-care applications, particularly in resource-limited regions. In addition, the successful circuit-level realization of the proposed architecture may contribute toward reliable high-speed electronics for healthcare, automation, communication, and intelligent technologies. Finally, the present research supports technological advancement in both electronics and biomedical engineering while contributing toward improved healthcare, sustainable energy utilization, and enhanced quality of life.

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Oppositely-Doped Core-Shell Junctionless Nanowire FET: Design and Investigation

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Junctionless Nanowire Field Effect Transistor (JL-NWFET) has garnered significant attention in recent years owing to its simplified fabrication process, achieved through uniform doping across the device. However, JL-NWFET suffers from certain drawbacks, including low drive current, insufficient volume depletion, and lateral band-to-band tunneling. To address these issues, this paper proposes Improved JL-NWFET with an oppositely doped core–shell structure along with a Dual Material gate (DMG) and high-k spacer. Furthermore, Improved JL-NWFET is optimized for parameters such as core thickness, gate oxide material, spacer material, and spacer length. The performance of Improved JL-NWFET is also evaluated in comparison with other structural variants of JL-NWFET. Notably, Improved JL-NWFET showcases an enhancement of 23.1% and 20% in ON-state current (I_{ON}) and transconductance (g_m), respectively when compared to the conventional JL-NWFET. Furthermore, the Subthreshold Slope (SS) experiences an 88% improvement in the Improved JL-NWFET as opposed to the JL-NWFET. Additionally, the OFF-state leakage current (I_{OFF}) undergoes a fivefold reduction, leading to a sixfold increase in the I_{ON}/I_{OFF} ratio compared to the JL-NWFET. Among all the variants of JL-NWFET devices analyzed in this paper, Improved JL-NWFET stands out with its exceptional performance characteristics.
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In recent years, the integrated circuits and information industry has been driven by the desire to improve device performance while reducing device dimensions. This downscaling of planar Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) has led to enhanced functionality, higher device density, and faster switching speeds. However, this conventional scaling of planar transistors has its limitations, particularly in terms of the emergence of Short Channel Effects (SCEs).[1,2] To address the challenges posed by SCEs, researchers have explored various multiple-gate structures.[3–5] Out of all the multigate device structures, the Gate All Around (GAA) MOSFET is considered the most optimal due to its superior gate controllability, higher packaging density, and immunity towards SCEs.[6–8] One of the complexities arising from the adoption of GAA MOSFETs is the formation of confined Source/Drain (S/D) junctions, which involves careful consideration of thermal budget and doping techniques during the fabrication process. Numerous studies have explored flexible organic devices because of their inexpensive manufacturing process at lower temperatures.[9–11] However, these organic devices face reliability issues and are not well-suited for high-speed analog and digital applications.[12] As an alternative to organic devices, silicon-based inorganic semiconductor devices such as Junctionless Transistors (JLTs) have emerged. JLTs do not rely on p-n junctions and instead have uniform doping throughout the source, channel, and drain regions, making the fabrication process more feasible and straightforward.[13–16]

The combination of GAA MOSFET structure and JLT has been demonstrated through experimentation and presented as a Junctionless Nanowire Field Effect Transistor (JL-NWFET).[17] JL-NWFET offers lesser fabrication complications and mitigated SCEs over the inversion mode MOSFET.[18–20] Despite offering several advantages, JLTs exhibit drawbacks like low drive current and transconductance when compared to conventional transistors. Additionally, the implementation of JLTs can lead to unavoidable process challenges, such as Random Dopant Fluctuations (RDFs) resulting in device variation.[21] Furthermore, the n-channel JLT experiences a challenge related to band overlap, which results in Lateral Band-to-Band Tunneling (L-BTBT) of electrons during the OFF-state ($V_{GS} = 0$ V, $V_{DS} = 1$ V) from the Valence Band (VB) to the Conduction Band (CB) of the channel and drain, respectively.[22] Consequently, this mechanism causes an increase in the number of holes within the n-channel, as electrons are being transported away via tunneling due to L-BTBT. As a consequence of this phenomenon, a parasitic n-p-n Bipolar Junction Transistor (BJT) is triggered, where the source, channel, and drain act as parasitic emitter, base, and collector, respectively. The occurrence of L-BTBT significantly increases the OFF-state current (I_{OFF}) and induces the parasitic BJT effect in JLT, necessitating measures to mitigate these issues.

Kumar et al.[23] explore the influence of the Shell Doping Profile (SDP) on enhancing the electrical characteristics of JLT with an intrinsic core. Moreover, the practical implementation of the SDP has been demonstrated through experimental approaches using Molecular Monolayer Doping (MLD) and Microwave Annealing (MWA) methods.[24,25] The combination of the MLD method with MWA for conformal and self-assembled doping has been demonstrated to effectively reduce the impact of RDF, as well as alleviate variations in subthreshold slope and threshold voltage. Additionally, researchers have successfully realized the Ge-Si_xGe_{1-x} Core–Shell (CS) nanowire tunneling field-effect transistor with a Ge core and Si_xGe_{1-x} shell.[26] Sahay et al.[27] investigated the beneficial effects of incorporating a p-type core in JL-NWFET, which helps to mitigate the parasitic BJT phenomenon and reduces I_{OFF}. However, the existence of a core within JL-NWFET results in a diminished effective shell area, thereby decreasing carrier mobility. Therefore, it is imperative to include some modified JL-NWFET structures that can be utilized to achieve high performance.

Numerous studies in the literature have proposed the utilization of Dual Material Gate (DMG) to enhance carrier mobility, ON-state ($V_{GS} = 1$ V, $V_{DS} = 1$ V) current (I_{ON}), and transconductance in comparison to Single Material Gate (SMG) JLT by carefully adjusting the channel potential and electric field distributions along the channel length.[28–31] The DMG architecture involves two gate metals, where the work function of gate metal 1 ($M1$) is higher than that of gate metal 2 ($M2$). Additionally, researchers have extensively investigated the incorporation of a high-dielectric constant (k) spacer on both sides of the gate to further enhance immunity against SCEs.[32–35] The focus of this paper is to explore the combined advantages of gate engineering and spacer techniques in an oppositely doped core–shell JL-NWFET.

This paper has a total of five sections, with Introduction section serving as the introduction. In Validation of Experimental Inversion-Mode Nanowire FET section, the experimental inversion-mode NWFET is validated while Device Structure and Characteristics of JL-NWFET section delves into the analysis of the electrical characteristics of JL-NWFET. Afterwards, Improved Junctionless

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PAPER

Investigating the effect of scaling and temperature on the performance of improved junctionless nanowire FET through simulation analysis

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Keywords: band-to-band tunneling (BTBT), core-shell (CS), dual material gate (DMG), high-k spacer, junctionless nanowire FET (JL-NWFET)

Abstract

An Improved Junctionless Nanowire Field Effect Transistor (I-JL-NWFET) device is proposed in this paper to address the limitations of conventional JL-NWFET. This research paper initially, comprehensively analyzes the impact of channel length (L) and channel thickness (t_{si}) scaling on the electrical, analog/RF, and linearity performance of I-JL-NWFET and JL-NWFET. The results suggest that the specific design features in I-JL-NWFET contribute to a more robust and less sensitive response to variations in scaling compared to its counterpart, JL-NWFET. Furthermore, an exploration into the impact of temperature on the electrical, analog/RF, and linearity performance is also conducted for both I-JL-NWFET and JL-NWFET. The electrical performance of I-JL-NWFET showcases a significantly reduced temperature sensitivity in parameters like drain current (I_D), Subthreshold Slope (SS) and Drain Induced Barrier Lowering (DIBL) compared to JL-NWFET. Subsequently, analyzing the analog/RF performance in the context of parameters such as transconductance (g_m), Transconductance Gain Factor (TGF), output conductance (g_d), early voltage (V_{EA}), total gate capacitance (C_{GG}), and cut-off frequency (f_T) under temperature variation, a lower degree of variability in I-JL-NWFET is observed compared to JL-NWFET. Furthermore, the linearity performance of I-JL-NWFET, assessed through parameters such as second and third-order transconductance (g_{m2}, g_{m3}), second and third-order input voltage intercept points (VIP2, VIP3), and third-order intermodulation distortion (IIP3 and IMD3) is improved at the higher temperature than that of JL-NWFET.

1. Introduction

The primary impetus behind the evolution of transistors towards miniaturization is to achieve higher density and enhanced performance for Integrated Circuit (IC) applications. However, this pursuit of miniaturization also introduces undesirable consequences in the form of adverse Short Channel Effects (SCEs) which impede technological progress [1]. To address these issues, the adoption of multi-gate transistors stands out as a promising solution for future technological advancements [2]. Nevertheless, the need for precise doping profiles at the metallurgical junctions and the necessity of a substantial thermal budget for dopant activation have become increasingly challenging as conventional Metal Oxide Semiconductor Field Effect Transistor (MOSFET) scaled down aggressively in size, which is also pertinent to future Complementary Metal Oxide Semiconductor (CMOS) technology [3].

Recently, Organic Thin-Film Transistors (OTFTs) have garnered significant attention for their commercial viability, primarily attributed to their mechanical flexibility, cost-effective fabrication, and semi-transparent characteristics [4]. Furthermore, leveraging the semiconductor properties of the organic materials used in their

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ORIGINAL RESEARCH ARTICLE

Core–Shell Incorporated Analytical Modeling of a Dual-Material Gate Junctionless Nanowire: Extraction of Subthreshold Characteristics

Bharti[1] · **Poornima Mittal**[1]

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Abstract
The easy fabrication process of a junctionless nanowire field-effect transistor (JL-NWFET) positions it as a promising alternative to the conventional FET. However, the heavy doping required in the JL-NWFET restricts carrier mobility and volume depletion. This paper introduces a dual-material gate (DMG) and a core–shell (CS) structure in the JL-NWFET to address these challenges. Moreover, developing an analytical model is crucial for understanding the intricate details of device physics. A physics-based 2D analytical model for the DMG-CS JL-NWFET is proposed in this paper. Using an analytical model, the subthreshold characteristics of the DMG-CS-JL-NWFET are investigated in terms of surface potential, electric field, threshold voltage, subthreshold drain current, leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio, subthreshold slope, and drain-induced barrier lowering (DIBL). The simulation results obtained with the ATLAS 3D device simulator align with the analytical results. The proposed model can serve as a foundational design guideline for core–shell-incorporated gate-engineered JL-NWFETs.

Keywords Analytical modeling · core-shell · dual-material gate (DMG) · junctionless nanowire FET (JL-NWFET) · surface potential

Introduction

Nanowire field-effect transistors (NWFETs) with cylindrical structures, which are based on inorganic materials, were initially proposed due to their efficient control over the channel region, effectively mitigating short-channel effects (SCEs).[1–3] However, challenges such as achieving an ultra-steep doping profile at the metallurgical junctions and the high thermal budget required for dopant activation limit their potential for aggressive scaling. Concurrently, organic materials for transistors are gaining attention for their commercial viability due to their mechanical flexibility, cost-effective fabrication, and semi-transparency.[4] Nonetheless, instability and degradation of organic materials remain significant challenges that need to be addressed for further advancements in organic transistor technology.[5] To overcome these challenges, junctionless nanowire field-effect transistors (JL-NWFETs) based on inorganic material (mainly silicon), have emerged as a promising technology in advanced semiconductor nodes, benefiting from a streamlined fabrication process that enhances scalability.[6–10] JL-NWFETs have a thin channel with high channel doping (~10^{19} cm^{-3}) and a high-work-function gate electrode (greater than that of silicon), which depletes the channel in the OFF-state, thereby further mitigating SCEs compared to inversion-based nanowires.[7] However, the JL-NWFET faces issues such as random dopant fluctuations (RDF)[9] and parasitic bipolar junction transistor (BJT) effects.[10] Moreover, the high doping concentration in the channel of the JL-NWFET adversely impacts carrier mobility, leading to a reduction in the drive current and transconductance.[11] In addition, threshold voltage fluctuations induced by random dopants are more pronounced than those in inversion-mode transistors, which typically feature a nearly intrinsic channel. This substantial variation in threshold voltage arises in JL-NWFETs due to the heavily doped channel.[8]

Consequently, the core–shell (CS) structure in the channel of a double-gate (DG) JL-FET has demonstrated that incorporating a core in the channel region effectively depletes the channel in the OFF-state and reduces the parasitic BJT phenomenon.[12–14] Additionally, a few studies in

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Analytical Modeling of Oppositely Doped Core-Shell Junctionless Nanowire Transistor Considering Fringe Capacitance and Dual Material Gate

*Bharti and Poornima Mittal**

This paper presents a physics-based analytical solution for junctionless nanowire field effect transistor (JL-NWFET) incorporating an oppositely doped core-shell (ODCS) structure, dual material gate (DMG), and a high permittivity spacer by solving Poisson's equation. The surface potential concept has been used to derive threshold voltage, drain-induced barrier lowering, drain current, and subthreshold slope. The results demonstrate that the cumulative benefits of ODCS, DMG, and high permittivity spacer in conventional JL-NWFET enhance the device performance and mitigate short channel effects (SCEs). Furthermore, the close agreement between the analytical and simulation results for different core thicknesses, spacer permittivities, channel lengths, and channel thicknesses highlights the robustness and reliability of the proposed modeling methodology, offering valuable guidance for device optimization and design refinement in nanoelectronics applications.

1. Introduction

The ease in the fabrication process for junctionless nanowire field-effect transistors (JL-NWFETs), credited to the lack of complex doping profiles and improved short channel effects (SCEs), positions them as promising alternatives to metal oxide semiconductor field effect transistors (MOSFETs).[1–6] JL-NWFETs obviate the necessity for ultra-steep doping profiles in the source/drain (S/D) regions and circumvent the thermal budget required for dopant activation. Despite alleviating many technological hurdles associated with scaling devices, JL-NWFETs still encounter challenges such as insufficient volume depletion,[7] random dopant fluctuations (RDFs),[8] and parasitic bipolar junction transistor (BJT) phenomenon.[9] Moreover, being comprehensively explored and fabricated only as single-unit devices, JL-NWFETs are not gaining significant popularity from a fabrication perspective compared to conventional multigate devices (such as FinFETs). Conventional multigate devices are already well-established in commercial fabrication flows, with significant investment in tooling, processes, and design support, making it harder for junctionless devices to gain acceptance. Recently, the emerging core-shell (CS) architecture in the channel of JL-NWFET has been explored.[10,11] This design incorporates a central core positioned between two shells within the source, drain, and channel regions. Simulation-based studies have explored designs with an intrinsic core[8] and an oppositely doped core[11] combined with highly doped shells. The inclusion of a p-type core in the n-type channel of JL-NWFET helps to realize efficient volume depletion that leads to mitigated OFF-state current. However, the inclusion of a core in the channel reduces the active conduction area, which in turn reduces the ON-state current in ODCS-JL-NWFET.

Many authors suggested the use of gate material engineering architecture as the solution to enhance carrier mobility within the channel.[12–17] In addition, the inclusion of a high permittivity spacer over an S/D extension region can facilitate volume depletion during OFF-state due to the fringing fields through the spacer enhancing the electric field in the S/D extension.[18] Furthermore, fringe capacitance arises due to the capacitance generated by the electric field through the spacer over the S/D extension region.[19] The fringe capacitance play a critical role in digital circuits, as they have a significant influence on propagation delays and power consumption. In analog circuits, these capacitances can lead to negative feedback, which can alter the gain-bandwidth product. The simulation-based study of DMG-incorporated ODCS-JL-NWFET has been reported[20] but they lack analytical modeling to validate the results.

The previously published work has developed analytical models for DG-JL-FET using central potential-based modeling as well as surface potential-based modeling approaches.[21] Li et al.[22] have utilized the central potential method to model gate all around (GAA) JL-NWFET with cylindrical structures. DMG-incorporated JL-NWFET has been modeled using the central potential approach.[13] However, these models often neglect the S/D extension regions. Besides this, charge-based modeling has been reported for advanced JL-NWFETs,[23,24] but key features such as the inclusion of DMG and S/D length have not been explored using this approach. Furthermore, an analytical model for core-shell incorporated JL-NWFET with a single material gate (SMG) has been proposed, employing the central potential concept.[11] Unlike conventional JL-NWFET, where bulk conduction domi-

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RESEARCH

Core–Shell Incorporated Junctionless Nanowire FET based Biosensor for Detection of p53 Biomarker in Gastrointestinal Cancer

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Abstract
The early-stage diagnosis of various Gastrointestinal (GI) cancers is critical for enabling timely clinical intervention and improving patient prognosis. This work presents an electrical biosensing approach for the differentiation and detection of healthy and cholangiocarcinoma conditions by quantifying varying clinical concentrations of the p53 biomarker in blood serum. The proposed sensing platform utilizes a Core–Shell Junctionless Nanowire Field Effect Transistor (CS-JL-NWFET) for the real-time and ultra-sensitive detection of the p53 biomarker. The sensing mechanism is based on interface charge modulation, where equivalent interface charges, representing different concentrations of the p53 biomarker, are introduced into the nanocavity region of the device. This electrostatic modulation influences the device's electrical response, enabling label-free biomarker detection. The performance of the biosensor is systematically evaluated using key sensing parameters, including threshold voltage, switching ratio (I_{ON}/I_{OFF}), and subthreshold slope. The proposed biosensor exhibits high sensitivity in distinguishing clinical p53 concentrations, achieving an I_{ON}/I_{OFF} ratio of 4.60×10^{9} at 1.62 ng/ml, corresponding to the maximum diseased state, and 2.15×10^{7} at 0.27 ng/ml, corresponding to the maximum healthy state, enabling effective differentiation between healthy and cancerous conditions. Furthermore, the impact of variation in core thickness, channel length, temperature, cavity occupancy, and repulsive steric hindrance on the threshold voltage, switching ratio, and subthreshold slope sensitivity is analyzed. The results confirm that device geometry and operational environment critically affect biosensor performance, providing valuable design insights for sensitivity, reliability, and clinical applicability.

Keywords Biosensor · Core–Shell · Gastrointestinal Cancer · Junctionless Nanowire · P53 biomarker · Sensitivity

Introduction

Gastrointestinal (GI) cancer stands among the most prevalent cancers globally and is the second leading cause of cancer-related deaths, accounting for around 700,000 fatalities annually. GI cancers encompass a group of malignant tumours that originate in the gastrointestinal tract and associated digestive organs. These include carcinomas that develop in the oral cavity, esophagus, stomach, liver, bile duct, gallbladder, pancreas, small intestine, and large intestine [1, 2]. Affecting both men and women, GI cancers impose a substantial burden on global health due to their high incidence and associated mortality. The increasing incidence is largely driven by factors such as population growth, aging, and unequal access to quality cancer prevention and treatment services. The early symptoms of GI cancer are often subtle or absent, leading to most cases being diagnosed at advanced stages, which significantly limits treatment effectiveness [3]. Early detection and timely intervention are key to improving cure rates, reducing mortality, and enhancing patient's quality of life. Moreover, early-stage cancer treatment typically requires fewer resources and less invasive interventions, thus lowering healthcare costs and easing financial burdens on patients. The p53 tumour suppressor protein is one of the most widely studied and clinically utilized biomarkers in cancer diagnostics [4–6]. Its overexpression has been observed in various GI cancers, and several studies suggest that detecting p53 in serum could serve as a valuable tumour marker [7, 8]. Commonly known as the "guardian of the genome," p53 plays a crucial role in preserving genomic stability [9–11]. It is among the most frequently mutated

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Analog/RF Performance of Oppositely Doped Core-Shell Junctionless Nanowire FET with Dual Material Gate and High-k Spacer

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***Abstract*— The impact of integrating Dual Material Gate (DMG) and high-k spacer on analog/RF characteristics of Oppositely Doped Core-Shell Junctionless Nanowire FET (ODCS-JLNWFET) is explored in this paper. The primary objective of this analysis is to assess the electrical as well as analog/RF performance of the proposed device (DMG-ODCS-JLNWFET with spacer) using various metrics such as subthreshold slope (SS), transconductance (g_m), switching ratio (I_{ON}/I_{OFF}), Transconductance Generation Factor (TGF), early voltage (V_{EA}), output conductance (g_d), total gate capacitance (C_{GG}), and cut-off frequency (f_T). The performance of DMG-ODCS-JLNWFET with spacer is compared with DMG-ODCS-JLNWFET without spacer, Single Material Gate (SMG) ODCS-JLNWFET with and without spacer. The results demonstrate enhanced electrical and analog/RF performance of the proposed device, offering valuable insights into its potential applications in the analog and digital domains at the nanoscale.**

Keywords*— Core-Shell (CS), Dual material Gate (DMG), Nanowire FET (NWFET), Spacer.

I. INTRODUCTION

The semiconductor research society has been actively working on various fronts to achieve cost-effective, miniaturized, high-speed, and low-power devices. However, as transistors become smaller, Short Channel Effects (SCEs) become more prominent, leading to degraded device performance and reliability [1]. The emergence of advanced transistor designs such as multiple gates Field-Effect Transistors (FETs) has demonstrated their excellence over planar devices when it comes to achieving device scaling [2]. Among various device designs, Gate-All-Around (GAA) FET is notably recognized as the ultimate device structure for downsizing devices [3]. In GAA FET, the gate wraps around the channel on all sides, enhancing electrostatic control of the gate voltage over the channel region. Nevertheless, GAA FET faces challenges in establishing precise connections of Source/Drain (S/D) regions and satisfying the rigorous thermal budget requirements [4].

Extensive research has been conducted on flexible organic devices owing to their cost-effective fabrication process and the ability to operate at lower temperatures. However, these organic devices face reliability issues, rendering them unsuitable for high-speed analog and digital applications [5], [6]. Therefore, Junctionless Nanowire (JLNW) FET, which is a silicon-based inorganic semiconductor device that eliminates the need for a p-n junction, has emerged as a promising alternative [4], [7]. The high doping concentration in JLNWFET device gives rise to several challenges, including reduced carrier mobility leading to low ON-state ($V_{GS} = V_{DS} = 1$ V) current (I_{ON}) and low transconductance. Moreover, the significance of the electron tunneling mechanism becomes pronounced in JLNWFET during the OFF-state [8].

In a recent study, a novel core-shell JLNWFET architecture that utilized conformal shell doping profiles has been experimentally demonstrated [9]. Kumar *et al.* [10] adopted an identical strategy in cylindrical gate JLNWFET to achieve improved electrical characteristics. Furthermore, many researchers have utilized core-shell architecture to enhance JLNWFET performance for diverse applications [11]-[15]. The inclusion of core helps in achieving volume depletion during the OFF state of JLNWFET, thereby reducing leakage current. However, there is a lack of research on enhancing I_{ON} of core-shell based FETs. The incorporation of Dual Material Gate (DMG) structures in comparison to Single Material Gate (SMG) structures has been shown to provide increased drain current, transconductance, and reduced SCEs [16]-[18]. Additionally, the utilization of high-dielectric (k) spacer further boosts the performance of JLNWFET [19]-[22].

This paper proposes an n-type JLNWFET with an oppositely doped core, combining DMG benefits with a high-k spacer. Furthermore, analog/RF performance is thoroughly explored for DMG-ODCS-JLNWFET with spacer and results are compared with those obtained from DMG-ODCS-JLNWFET without spacer, SMG-ODCS-JLNWFET with spacer, and SMG-ODCS-JLNWFET without spacer configurations. This paper comprises four sections starting with Section I as the introduction. Section II provides a description of the parameters of the device structure. Furthermore, Section III presents the results and discussion including a comparative analog and Radio Frequency (RF) analysis of the proposed device with other ODCS-JLNWFET counterpart structures. Finally, Section IV presents a conclusion based on the findings of the analysis.

II. DEVICE STRUCTURE

A 3-D view of the proposed DMG-ODCS-JLNWFET with spacer device is demonstrated in Fig. 1 (a) whereas its 2-D schematic view is represented in Fig. 1 (b). The L_G, t_{ox}, and t_{si} remain set at 60 nm, 1 nm, and 20 nm, respectively, as per the experimental findings in [23].

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Improved Performance of Oppositely Doped Core-Shell Junctionless Nanowire FET Using Gate Material Engineering

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***Abstract*— The impact of work function variation on Dual Material Gate Oppositely Doped Core-Shell Junctionless Nanowire FET (DMG-ODCS-JLNWFET) is explored in this paper. The variation in surface potential, electric field, band energy, drain current (I_D), leakage current (I_{OFF}), subthreshold slope (SS), transconductance (g_m), and switching ratio (I_{ON}/I_{OFF}) are analyzed. The performance of DMG-ODCS-JLNWFET is also compared with Single Material Gate (SMG) ODCS-JLNWFET. The results demonstrate that the proposed device shows significant advancements, boasting improvements of 18.9%, 73.7%, 26.8%, and 10.8% in I_D, I_{OFF}, g_m, and SS respectively when compared to SMG-ODCS-JLNWFET. These noteworthy enhancements underscore the device's exceptional suitability for both analog and digital applications within the confines of nano-scale dimensions.**

Keywords— Core-Shell (CS), Dual material Gate (DMG), Nanowire FET (NWFET), Work function.

I. INTRODUCTION

The notable Short Channel Effects (SCEs) observed at scaled dimensions are a consequence of ineffective gate control and physical restrictions in achieving ultra-scaled dimensions. This has surpassed the capabilities of traditional planar Field Effect Transistors (FET), prompting researchers to redirect their attention towards multiple-gate 3-D topologies, particularly Nanowires FET (NWFET), as the prospective foundation for technologies [1]. However, it faces major hurdles in achieving an ultra-sharp doping gradient at the junction during fabrication [2]. Considerable research efforts have been dedicated to exploring flexible organic devices, primarily due to their cost-effective fabrication process and their capacity to operate effectively at lower temperatures. Despite these advantages, the reliability of organic devices poses a notable challenge, making them less suitable for applications requiring high-speed analog and digital functionalities [3], [4].

Junctionless Nanowire FET (JLNWFET) has emerged as a noteworthy alternative exhibiting a low thermal budget during the manufacturing process due to a lack of p-n junctions [5]. Furthermore, to achieve better electrostatic control of gate voltage over the channel, Junctionless Transistors (JLTs) have also embraced cylindrical architecture [6]. Despite several advantages, the high doping concentration inherent in JLNWFET introduces challenges, notably resulting in reduced carrier mobility, leading to low ON-state current (I_{ON}) and transconductance. Additionally, insufficient volume depletion and electron tunneling during OFF-state contribute to an increase in leakage current. The incorporation of an oppositely doped core within the Core-Shell (CS) architecture of JLNWFET helps in volume depletion in the OFF state which tends to reduce I_{OFF} [7], [8]. In 2014, Lee *et al.* [9] demonstrated the feasibility of CS-JLNWFET marking the first experimental validation of the innovative approach. Previously, multiple researchers have employed Dual Material Gate (DMG) to improve carrier mobility and mitigate the impact of SCEs by altering the channel potential and electric field distributions as compared to Single Material Gate (SMG) devices [10]-[13].

The DMG architecture comprises two gate materials, M_1 and M_2, characterized by distinct work functions Φ_{M1} and Φ_{M2}, with the condition $\Phi_{M1} > \Phi_{M2}$ [10]. To harness the benefits of DMG in conjunction with an oppositely doped core-shell structure, a novel device structure named Dual Material Gate Oppositely Doped Core-Shell (DMG-ODCS) JLNWFET is proposed in this paper. Moreover, the effect of workfunction variation of M_2 (Φ_{M2}) by keeping Φ_{M1} constant, on the performance of the DMG-ODCS-NWFET device. One challenge associated with implementing work function variation in practical device fabrication is the reliance on the DMG approach. This method utilizes a single Reactive Ion Etching (RIE) process to pattern dissimilar gate metals simultaneously, ensuring high selectivity to the ultrathin gate dielectric. An alternative method entails leveraging molybdenum (Mo) as a commonly utilized gate material, with its work function susceptible to adjustment through careful control of nitrogen implantation within the Mo substrate, offering a potential avenue for achieving desired work function variations in devices [14], [15].

This paper is systematized into four sections, commencing with Section I, which serves as the introduction. In Section II, a detailed account of the device structure parameters is presented. Section III is dedicated to presenting the results and facilitating a comprehensive discussion, which includes a comparative analysis between the proposed device and SMG-ODCS-JLNWFET. The final section, Section IV, encapsulates the conclusion drawn from the analysis and findings presented throughout the paper.

II. DEVICE STRUCTURE

The devices are simulated using the SILVACO TCAD simulator [16]. A 3-D view of the proposed DMG-ODCS-JLNWFET device is presented in Fig. 1 (a) whereas its 2-D schematic view is illustrated in Fig. 1 (b). Additionally, a 2-D cross-sectional view of SMG-ODCS-JLNWFET is depicted in Fig. 2. Table I provides the structural parameters of both devices. These parameters are chosen as per experimental work [17]. The channel thickness (t_{si}) of DMG-ODCS-JLNWFET is given as [7]

$$t_{si} = (2 \text{ X } t_{shell}) + t_{core} \quad (1)$$

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Oppositely Doped Core-Shell Junctionless Nanowire FET based Biosensor: Proposal and Optimization

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***Abstract*—Dielectric-Modulated (DM) Field-Effect Transistors (FETs) have garnered considerable attention for their ability to detect biomolecules. This work proposes a novel Oppositely Doped Core-Shell Junctionless Nanowire FET with Dual Material Gate based biosensor for the detection of neutral biomolecules. The proposed biosensor is optimized in terms of cavity position (either on the drain side or the source side) and cavity length. Furthermore, after the cavity position and length are optimized, the sensing capability of the proposed biosensor is evaluated through its electrical parameters. The analysis reveals that the proposed device structure functions as an extremely sensitive and label-free biosensor.**

Keywords—Biosensor, Core-Shell (CS), Dielectric Modulated (DM), Junctionless Nanowire FET (JL-NWFET), Sensitivity.

I. Introduction

The medical healthcare sector is experiencing a notable increase in demand for devices that offer both user-friendliness and swift response times when diagnosing a range of diseases within the human population. In this context, the pivotal objective of medical equipment is to provide precise measurements of health status, promptly identify the onset of diseases, and track their progression over time. Moreover, by swiftly identifying the initial signs of a disease, medical professionals can initiate timely and appropriate interventions, potentially preventing its advancement to more severe stages. Therefore, biosensors play a vital role in this process by serving as sensitive diagnostic tools capable of detecting biomarkers associated with various diseases [1-5]. Furthermore, Field Effect Transistor (FET) based biosensors offer a viable option for the unlabeled detection of biomolecules due to their affordability, scalability, sturdiness, faster response time, heightened sensitivity, and reliable performance [6, 7].

The Dielectric-Modulated (DM) FET detects and monitors biomolecules through cavities or nanogaps in the oxide region, altering the dielectric constant. This change affects electrostatics and transport, modulating electrical characteristics. By tracking these changes, label-free detection is achieved. However, Short Channel Effects (SCEs) significantly reduce the sensitivity, scalability, and energy efficiency of FET-based biosensors [8]. Therefore, Junctionless Nanowire FET (JL-NWFET) based biosensors have been explored by incorporating the DM technique [9-12]. Moreover, JL-NWFET offers a simplified manufacturing process and mitigated SCE over conventional FET [13]. In addition, incorporating the Core-Shell (CS) architecture within the channel of JL-NWFET significantly mitigates tunneling effect as well as parasitic BJT phenomena [14]. Additionally, Gate Material Engineering (GME) has been explored in CS-JL-NWFET which simultaneously improves device mobility and reduces leakage current [15-17].

This work proposes an Oppositely Doped Core-Shell (ODCS) JL-NWFET with Dual Material Gate (DMG) based biosensor for label-free detection of neutral biomolecules. The presence of a neutral biomolecule using the proposed device is detected by introducing the dielectric constant (k) of the targeted neutral biomolecule in the oxide region. The neutral biomolecules namely streptavidin (k = 2.1), biotin (k = 2.63), and keratin (k = 10) are taken into account [18]. Streptavidin is used to detect lipids, nucleic acids, and proteins [19]. Biotin is a form of vitamin B which is essential for skin and nails health [20]. Keratin is a protein that helps to form skin, nails and hair [21]. The proposed device undergoes analysis first with a cavity at the drain side, then with a cavity at the source side, to determine the optimal position for enhancing sensitivity across varying cavity lengths.

The paper is systematized into four sections. Section I provides the introduction. Section II provides detailed device structure parameters. Section III delivers results and facilitates discussion. Section IV summarizes the conclusions drawn from the analysis and findings presented in the paper.

II. Device Structure

A 3-D view of the proposed DMG-ODCS-JL-NWFET based biosensor device is presented in Fig. 1 (a). Fig. 2 (a) and (b) portray the 2-D schematic of DMG-ODCS-JL-NWFET biosensor with a cavity at drain side and source side, respectively. The device parameters of the proposed biosensor are summarized in Table I. The workfunction of gate metal 1 (M1) and gate metal 2 (M2) are kept at 5.1 eV and 4.6 eV, respectively [22]. The length of M1 (LM1) and M2 (LM2) constitute channel length (L) such that L = LM1 + LM2. The channel thickness (tsi) of DMG-ODCS-JL-NWFET is given as [14, 15]

$$t_{si} = (2 \times t_{shell}) + t_{core} \quad (1)$$

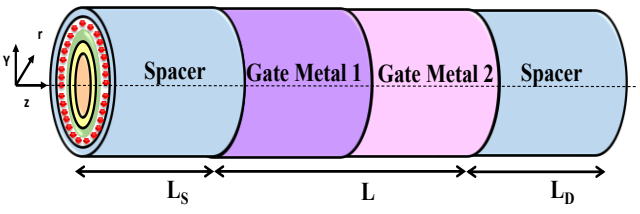

Fig. 1. 3-D view of DMG-ODCS-JL-NWFET biosensor.

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Effect of Interface Trap Charges on Improved Junctionless Nanowire Field Effect Transistor

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***Abstract*— This paper investigates the reliability issues caused by Interface Trap Charges (ITCs) in the Improved Junctionless Nanowire Field Effect Transistor (Improved-JL-NWFET). These fixed localized charges formed at the channel-oxide interface during fabrication due to radiation, stress, process variations, and hot carrier damage, significantly impacting device characteristics. This paper analyzes their effects on key performance parameters and compares results with a conventional JL-NWFET. Both donor (+ve) and acceptor (−ve) ITCs in the channel/gate oxide interface region are examined for their influence on electrical and analog parameters. The results indicate that Improved-JL-NWFET exhibits more immunity against degradation in electrical and analog parameters compared to its conventional counterpart devices in the presence of positive and negative ITCs.**

Keywords— Core-Shell (CS), Dual Material Gate (DMG), Interface Trap Charge (ITC), Junctionless Nanowire FET (JL-NWFET).

I. INTRODUCTION

Nanowire Field-Effect Transistor (NWFET) having cylindrical structure offers enhanced gate control compared to Double-Gate (DG) FETs and FinFETs while effectively mitigating Short Channel Effects (SCEs) [1]. Meanwhile, Junctionless (JL) NWFETs have emerged as strong contenders to conventional junction-based NWFETs, primarily due to their simpler fabrication process [2, 3]. Unlike traditional junction-based NWFET, JL-NWFET does not require highly precise doping profiles in the Source/Drain (S/D) regions, nor do they depend on high-temperature dopant activation. However, JL-NWFET faces challenges such as incomplete volume depletion [4], which results in high leakage current and low drive current [5]. To address these challenges, researchers have investigated innovative structural modifications.

Among them, the Core-Shell (CS) channel structure, which incorporates a central core surrounded by shells in the source, drain, and channel regions, has demonstrated significant potential in minimizing leakage currents in JL-NWFETs [4, 6-7]. However, the CS structure alone does not enhance the device's drive current. To address this limitation, the integration of Dual Material Gate (DMG) configurations with gate sidewall spacers in the core-shell structure, aiming to improve carrier mobility while effectively minimizing leakage current, has been reported [8]. This paper presents an Improved JL-NWFET (Improved-JL-NWFET) that incorporates the combined benefits of CS structure in the channel, a DMG design in gate material with a gate sidewall spacer.

Apart from addressing SCEs, ensuring device reliability is crucial, especially for nanoscale transistors. During fabrication, various charges are introduced into the oxide layer and accumulate at the channel-gate oxide interface, negatively impacting performance. These trap charges originate from process-induced, stress-induced, and radiation-induced damage [9]. Previous research has extensively examined the effects of localized charges on JL Trigate MOSFET [10], Tunnel FET [11], and JL-NWFET [12]. Donor interface traps act as positive localized charges when devoid of electrons, whereas acceptor interface traps function as negative localized charges when filled with electrons [13]. Understanding these charge dynamics is essential for improving the stability and reliability of advanced nanoscale devices.

This paper analyses the performance and reliability issues of Improved-JL-NWFET and its counterparts JL-NWFET and NWFET due to interface trap charges. It is structured into four sections: Section I presents the introduction, while Section II defines the parameters of three devices. Section III presents the results and discussion, including a comparative analysis of Improved-JL-NWFET, JL-NWFET, and NWFET. Finally, Section IV summarizes the key findings from the analysis.

II. DEVICE STRUCTURE

Fig. 1 (a) and (b) present 3-D and 2-D representations of Improved-JL-NWFET, respectively. Fig. 2 (a) illustrates the single 3-D view which is same for both conventional JL-NWFET and NWFET. Furthermore, the 2-D structure for conventional JL-NWFET and NWFET are displayed in Fig. 2 (b) and (c), respectively. The structural parameters of the devices are summarized in Table I. The Improved-JL-NWFET design features a core region with opposite doping (p-type), leading to the formation of a reduced n-type channel known as the shell region. The SiO_2 serves as the gate oxide, while HfO_2 is employed as the gate sidewall spacer [14]. The overall silicon thickness (t_{si}) is determined by the core thickness (t_{core}) and shell (t_{shell}) thicknesses, following the relation $t_{si} = (2 \times t_{shell}) + t_{core}$ [4]. The device simulations are conducted using the SILVACO ATLAS TCAD 3-D device simulator [15]. In the Improved-JL-NWFET structure, t_{core} is set to 10 nm, which is half of t_{si} [16]. The DMG configuration incorporates two gate metals (M_1 and M_2), each extending 15 nm, with a work function difference of 0.5 eV between them [17].

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Steric Hindrance Effect on Core-Shell Junctionless Nanowire FET Based Biosensor Sensitivity for Breast Cancer Detection

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***Abstract*— This work investigates a Core–Shell Junctionless Nanowire (CSJLNW) FET based biosensor incorporating dielectric modulation for breast cancer detection. The proposed device detects the presence of different cell lines of breast cancer, namely, MCF-10A, HS578t, MCF7, and T47D. The investigation focuses on the influence of steric hindrance, where incomplete nanocavity filling by biomolecules affects electrostatic coupling and sensitivity of the proposed biosensor. The simulation results demonstrate that the non-uniform step patterns inside the nanocavity due to the steric hindrance effect significantly modify device parameters, namely threshold voltage, ON-state current, switching ratio, and subthreshold slope. The findings highlight the potential of the proposed biosensor as an ultra-sensitive and label-free system for the early detection of cancer.**

Keywords— Biosensor, Core-Shell (CS), Dielectric Modulated (DM), Junctionless Nanowire (JLNW) FET, Steric Hindrance Effect.

I. INTRODUCTION

Cancer continues to be a public health challenge, with breast cancer being the most diagnosed malignancy in women. It accounts for approximately 11.6% of all diagnosed cancer cases and contributes to around 6% of global deaths due to cancer [1]. An initial and precise diagnosis is therefore crucial for effective treatment and reduction in mortality rates. Currently, X-ray mammography serves as the main method for diagnosis; however, limited accessibility in remote regions and the rising cost of healthcare in developed nations highlight the need for diagnostic techniques that are reliable, affordable, and easy to interpret [2]. The difference between normal and cancerous breast tissues' dielectric properties offers a strong foundation for effective detection. Recent research has reported a permittivity ratio of nearly 2:1 between normal and cancerous tissues [3], with cancerous tissues consistently exhibiting higher permittivity and conductivity in the frequency range of 50–900 MHz [4]. These differences have been further validated through investigations of breast cancer cell lines across a broader spectrum extending from 200 MHz to 13.6 GHz [5]. Such insights into dielectric behavior enable the development of Dielectric Modulated Field Effect Transistor (DM-FET) devices, offering a promising pathway for cost-effective and early breast cancer detection [6].

The DM-FET facilitates label-free detection by introducing nanogaps within the oxide region, where variations in the dielectric constant influence the electrostatics, leading to measurable changes in device behavior. However, conventional FET-based biosensors suffer from Short Channel Effects (SCEs), which degrade the device's sensitivity and reduce its overall energy efficiency [7]. To address these issues, Junctionless Nanowire (JLNW) incorporating DM techniques have been proposed in the literature [8]. JLNWs simplify fabrication and suppress SCE compared to traditional FETs [9]. Moreover, adopting a Core-Shell (CS) channel design in JLNWs further minimizes tunneling and parasitic BJT effects [10], while Gate Material Engineering (GME) improves mobility and reduces leakage [11]. In practical biosensing systems, target biomolecules bind to immobilized receptors inside nanocavities. This binding is often constrained by steric effects caused by molecular crowding, size mismatch, electrostatic interactions, and non-ideal binding efficiency. As sites become occupied, previously bound molecules obstruct further analyte access, leaving the nanogap only partially filled [12, 13]. Such non-uniform attachment produces uneven dielectric changes within the cavity, which ultimately reduces the sensor's sensitivity.

A. Literature Review

Several FET-based biosensors based on DM have been reported for label-free breast cancer detection by exploiting dielectric modulation. Singh *et al.* [14] employed a dopingless negative-capacitance ferroelectric tunnel FET (TFET) with dual nanocavities, achieving ultra-high sensitivity through intrinsic gate voltage amplification. Kaushal *et al.* [15] proposed a thickness-engineered MoS_2 TFET biosensor, demonstrating enhanced sensitivity with increased cavity occupancy. Bitra *et al.* [7] reported a dielectric-modulated step-channel JL-TFET using charge plasma concepts to suppress random dopant fluctuations. Priyadarshani *et al.* [8] utilized a dual-nanocavity JL-FET to sense multiple breast cancer cell lines, highlighting the role of dielectric variation and cavity optimization. However, most existing works assume ideal or uniform cavity filling, with limited analysis of steric hindrance–induced non-uniform biomolecule immobilization, motivating the present study.

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Delhi Technological University, Delhi

B.E. in Electronics and Communication Engineering, 2017

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Journal Publications

1. Bharti and Poornima Mittal, "Oppositely-Doped Core-Shell Junctionless Nanowire FET: Design and Investigation," *ECS Journal of Solid State Science and Technology*, vol. 13, no. 1, pp. 013004-013004, Jan. 2024, doi: 10.1149/2162-8777/ad1c90.
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