ENHANCED PERFORMANCE SCHMITT TRIGGER LOGIC DESIGN

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by

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CANDIDATE'S DECLARATION

I, Bhawanand Jha, hereby certify that the work which is being presented in the thesis entitled "Enhanced Performance Schmitt Trigger Logic Design" in partial fulfillment of the requirements for the award of the Degree of **Doctor of Philosophy**, submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from **July 2019** to **JUNE 2026** under the supervision of **Prof. Rajeshwari Pandey** and **Prof. Kirti Gupta**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Candidate's Signature

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

Signature of Supervisor(s) **Signature of External Examiner**

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CERTIFICATE

This is to certify that Bhawanand Jha (Enrollment No. 2K19/PHDEC/11) has conducted the research work presented in this thesis entitled **"Enhanced Performance Schmitt Trigger Logic Design"** for the award of **Doctor of Philosophy** in the **Department of Electronics and Communication Engineering,** Delhi Technological University, Delhi.

The work embodied in this thesis is an authentic record of the candidate's own research carried out under the supervision of **Prof. Rajeshwari Pandey** and **Prof. Kirti Gupta**. The matter presented in this thesis has not been submitted elsewhere, either in part or in full, to any other university or institute for the award of any degree or diploma, to the best of our knowledge and belief.

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ABSTRACT

Advances in VLSI technology have driven the growth of energy-constrained applications such as healthcare, environmental monitoring, surveillance, and smart agriculture, increasing the need for ultra-low-power circuit techniques. Although CMOS logic is widely used for its low power and reliability, continued scaling has raised chip and power density, making supply-voltage reduction essential. Subthreshold and near-threshold operation support minimum-energy designs, and many systems operate even below this point for greater energy savings. Applications with long standby durations further benefit from aggressive voltage scaling, as standby power dominates their energy use. However, existing CMOS low-voltage techniques face challenges such as high bias requirements, variability, and post-silicon tuning, while reduced supply voltage degrades the on/off current ratio and noise immunity. These limitations highlight the need for logic styles with stronger current ratios and improved noise tolerance. Schmitt Trigger (ST) logic meets these requirements through its inherent hysteresis and leakage-quenching properties, offering better leakage reduction and noise immunity than conventional CMOS for robust low-voltage operation.

Schmitt trigger logic is a better alternative than CMOS logic for operation at lower supply voltages. Different variants of ST logic style with improved performance are available in the literature. In this work, the modified topologies of ST gates are investigated and design enhancements aimed at improving their overall efficiency are proposed. The design of ST gates is oriented towards low voltages at lower technology nodes which results circuits with high delay values. Thus, two novel ST logic styles gates named as three-stage ST (TS ST) and transmission-gate based three-stage ST (TG-TS ST) are put forward. The proposed ST logic gates have improved delay and power in comparison to existing ST logic gates due to reduction in load capacitances.

The use of variable threshold CMOS (VTCMOS) gates with high noise immunity is restricted due to the high leakage current values. The issue has been addressed by integrating variable threshold concept with device stacking in the novel low-leakage Schmitt Trigger style termed Stacked Variable Threshold CMOS (SVTCMOS) ST logic style. This technique effectively suppresses leakage current while enhancing noise robustness. Analytical formulations are developed to characterize the improvement in leakage behaviour and hysteresis response. Simulations validate that the proposed SVTCMOS design offers improved reliability for low-power digital circuits, particularly those where leakage current dominates overall energy consumption.

The issue of degraded noise immunity in dynamic ST gates is addressed by integrating dynamic threshold voltage device along with refined keeper and feedback transistors to achieve both high speed and strong noise tolerance. A dedicated domino ST buffer is designed and analyzed. The results demonstrate improved hysteresis characteristics, stable output behaviour, and enhanced delay performance compared to existing dynamic and static ST buffers. The design also exhibits strong resilience under process and voltage variations.

Finally, to address the process corners and voltage variations introduced by CMOS scaling, the work explores a process-invariant ST logic gate using Carbon Nanotube Field-Effect Transistor (CNTFET) technology. The proposed CNTFET-based ST logic gate exhibits improved consistency and reliability under process corners and voltage variations, highlighting its potential for next-generation nanoelectronics and robust digital interfaces.

Overall, this thesis provides a comprehensive set of ST logic design methodologies covering static, dynamic, low-power, and variation-tolerant domains. The proposed techniques are supported through theoretical analysis, extensive SPICE-level simulations at 45 nm technology node, and variation studies. Additionally, Stanford University's 32 nm CNTFET model is used to validate the performance of CNTFET-based gates. Collectively, these contributions advance the design of high-efficiency and noise-tolerant digital circuits, offering promising applicability in low-power processors, sensor nodes, and emerging nanoscale computing architectures.

The future scope of this work focuses on extending the proposed ST gate designs toward advanced low-power and high-performance VLSI applications. An algorithmic design methodology can be developed to optimize transistor sizing, threshold voltage, and feedback parameters for achieving an effective trade-off between power consumption and speed. Further research can investigate the cascading behaviour of dynamic ST gates by analyzing timing constraints, charge sharing, clock synchronization, and hysteresis effects in multi-stage operations. Such analysis can support the development of reliable pipelined architectures with improved noise immunity and robustness against process and voltage variations.

In addition, the proposed TS ST and TG-TS ST logic styles can be expanded to implement complex combinational and sequential circuits for evaluating their system-level performance in terms of delay, power dissipation, PDP, and signal integrity. Their integration into larger modules such as arithmetic units, control circuits, and pipeline systems can provide insights into scalability and suitability for modern VLSI systems. Furthermore, CNTFET based ST gates can be extended to realize arithmetic circuits including adders, subtractors, multipliers, and ALUs, enabling energy-efficient designs for future nanoelectronic and low-power computing applications.

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Abbreviations

Schmitt Trigger	ST
Dynamic threshold MOS	DTMOS
Variable threshold CMOS	VTCMOS
Pull-down network	PDN
Pull-up network	PUN
Feedback network	FBN
Multiplexer	MUX
Three-stage ST	TS ST
Transmission gate three-stage ST	TG-TS ST
Stacked VTCMOS Schmitt Trigger	SVTCMOS
2 input AND	AND2
2 input OR	OR2
2 input exclusive OR	XOR2
2 input NAND	NAND2
2 input NOR	NOR2
Carbon nanotube field effect transistor	CNTFET
Single-walled CNT	SWCNT

Chapter 1

Introduction

1.1 Background

The advancement in VLSI technology has led to tremendous growth in energy-constrained applications such as healthcare systems, environmental monitoring systems, surveillance systems, and smart agriculture systems [1-5]. The tight energy budget of these applications demands low power circuits and thus has motivated research in this direction. The use of CMOS logic is the driving force behind various large-scale integrations for designing applications due to design ease, negligible static power consumption, and high packing density. However, with the scaling down of the CMOS technology, the integrated circuits have become compact along with increased power density [6-7]. This needs attention for the design of digital circuits to be used in energy-constrained applications. The scaling of supply voltage is adopted to obtain low-power circuits for its quadratic effect on power. Various CMOS design techniques to facilitate operation at low voltage involve optimized transistor sizing [8], dynamic forward biasing schemes [9], near zero threshold transistors [10], body biasing [11] and subthreshold operation are suggested. Out of these, subthreshold operation is mostly preferred since the other techniques suffer from the drawbacks of high bias voltage generation, active variability compensation, or post-silicon tuning. The circuits operating in sub-threshold region mainly focus on operation optimized for minimum energy per operation point. The circuits used in energy-constrained applications however, operate below this point wherein the minimum supply voltage is determined at the instant when active operation gets initiated [12-19]. Further, applications such as environmental monitoring system, wireless sensor network circuits employ circuits with long standby durations such that the standby power consumption dominates the overall energy budget. Therefore, minimizing the supply voltage is a promising solution to achieve significant power reduction.

The operation of CMOS digital circuits at low voltages offers significant power saving but affects the other performance parameters. In the conventional CMOS digital circuits, the transistor's active current (I_{ON}) to leakage current (I_{OFF}) ratio (I_{ON}/I_{OFF}) gets degraded at lower supply voltage due to its exponential dependence on power supply, V_{DD} as given by

$$\frac{I_{ON}}{I_{OFF}} = e^{(V_{DD}/\eta V_T)} \tag{1.1}$$

where η is the sub-threshold ideality factor, and VT is the thermal voltage [20]. The reduced I_{ON}/I_{OFF} ratio limits the supply voltage scaling in CMOS digital circuits as the output fails to attain nominal V_{DD} and GND voltage levels defined for the logic design [21]. Additionally, the digital CMOS circuits become susceptible to noise at lower voltages as the threshold voltage is not aggressively scaled as the supply voltage. This causes degradation of the noise immunity of the circuits. Thus, there is a need for an alternate low-voltage logic style that maintains the optimum I_{ON}/I_{OFF} ratio and exhibits better noise immunity.

The Schmitt trigger (ST) logic style is an amenable solution that addresses the above-mentioned issues. A conventional ST logic gate exhibits a leakage quenching effect that reduces I_{OFF} value and increases the I_{ON}/I_{OFF} ratio, and hysteresis that enhances noise immunity in comparison to a CMOS logic gate [22-58]. A digital gate designed using ST logic is a better alternative than CMOS logic for lower supply voltage operation [28]. Different variants of ST logic style with improved performance are available in the literature [22-78]. In this work, ST logic style is chosen for the implementation of digital logic gates, and different improved structure of ST logic gates are presented for enhanced performance.

1.2 Schmitt Trigger (ST) Logic Style

A conventional ST logic gate consists of three parts, namely a pull-down network (PDN), a pull-up network (PUN), and a feedback network (FBN). The schematic of a conventional ST logic inverter is shown in Fig. 1.1 [26]. The transistors (P1, P2), (N1, N2) and (P3, N3) form the PUN, PDN and FBN, respectively. For a low value of input V_{IN}, transistors (P1, P2) conduct such that the output node V_{OUT} is charged to a high voltage level. Alternatively, for a high value of input V_{IN}, transistors (N1, N2) conduct such that the output node V_{OUT} attains a low voltage level. The presence of feedback in the conventional ST inverter results in two different switching threshold voltages in contrast to a single threshold voltage in CMOS inverter. Also, the feedback transistors result in leakage quenching from the output node, thereby minimizing the output level degradation. Thus, the ST logic gates offer the advantage of reduced leakage current and better noise immunity over CMOS logic gates [22-29].

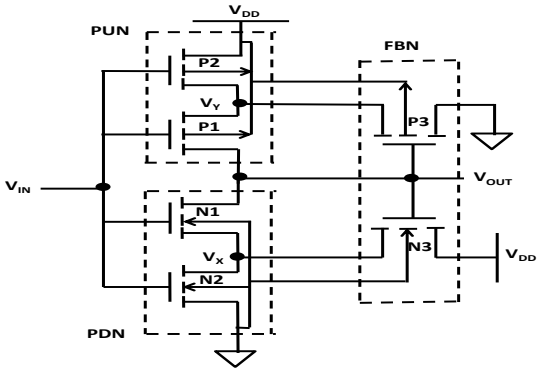


Fig. 1.1 Schematic of a conventional ST logic inverter [26]

The ST logic gates are investigated in the literature as a robust solution for noise-tolerant and low-power digital circuit design [12-82]. Based on a comprehensive study of the available literature on ST logic gates, the work done can be divided into two categories, namely static ST gates and dynamic ST gates. The work done under each category is described further.

Static logic circuits allow versatile implementation of logic functions based on static, or steady-state. A typical static logic gate generates its output corresponding to the applied input voltages after a certain time delay, and preserves its output level as long as the power supply is provided. In the literature, the performance of the conventional ST static gate is reported to be improved in terms of parameters like reduced leakage, improved noise immunity, and I_{ON}/I_{OFF} value. The improved static ST logic style includes leakage control transistor (LECTOR) ST logic style [30], [33], gated leakage transistor (GALEOR) ST logic style [31], [33], feed-forward leakage self-suppression (FFLSSL) ST logic style [33] NMOS-only voltage booster ST logic style (NST) [34], voltage bootstrapping ST (VB-ST) logic style [35], pseudo NMOS ST logic style [33] dynamic threshold ST logic style [36-37], variable threshold CMOS ST logic style (VTCMOS ST) [36], [38].

The authors in [30] applied the LECTOR technique in ST logic style to reduce leakage current in comparison to conventional ST logic style. Two extra leakage-controlled transistors, each in PDN and PUN are added between the output node and the transistor implementing the functionality in PDN and PUN. The effective stacking of transistors reduces the leakage

current, however, it adds extra resistance in the circuit. Another style is based on the gated leakage transistor (GALEOR) technique [31], where gated leakage transistors are connected. This technique also reduces the leakage power, but generates output with reduced voltage swing and increased propagation delay. The feed-forward leakage, self-suppression logic (FFLSSL) stacks additional transistors both in the PDN and PUN. The circuit involves feedback from the output node at different terminals in both PDN and PUN. All three circuits reduce leakage power but suffer from lower noise margin values, thereby exhibiting reduced noise immunity.

An NMOS only voltage booster ST (NST-VB) style is presented in [34]. The circuit replaces the PMOS in the PUN with an NMOS transistor to reduce the effect of negative bias temperature instability in the circuit. The voltage booster arrangement addresses the issues of threshold voltage drops due to the use of NMOS only transistors. The circuit employs the use of another supply which is greater than the power supply of the gate. Also, the circuit has high delay values with an area overhead. These drawbacks are overcome in another circuit presented as a voltage-booster ST (VB-ST) style in [35]. The circuit adds diode connected NMOS and dummy transistor which acts as a capacitor to provide voltage bootstrapping. The circuit exhibits lower hysteresis width due to the absence of a feedback mechanism in the PUN, thereby significantly degrading the noise immunity of VB-ST gates.

Another version of static ST logic style replaces all the PMOS transistors in the PUN with one PMOS transistor, referred to as pseudo NMOS ST logic style [33]. The gate terminal of the PMOS transistor is connected to ground potential and is thus named as Pseudo NMOS. The topology offers advantages like smaller chip areas and high density, but the ratioed logic and the always-on pseudo transistor cause large power consumption, which make its highly unattractive.

The authors in [36], [37] have used the dynamic threshold MOS (DTMOS) technique in ST logic gates. A DTMOS ST inverter replaces normal transistors in a conventional ST inverter with DTMOS transistors. The DTMOS ST logic provides enhanced noise immunity and improved I_{ON}/I_{OFF} ratio by dynamically modulating the threshold voltage of the transistors. When the gate and body terminals are shorted, the effective threshold voltage is reduced during switching, resulting in improved drive capability and sharper switching characteristics. While this technique enhances noise robustness and switching speed, it also leads to increased switching current. Furthermore, the reduced threshold voltage increases susceptibility to leakage, which limits its effectiveness in deeply scaled technologies.

The conventional, LECTOR, GALEOR, FFLSSL, NST-VB, VB-ST, Pseudo NMOS, and DTMOS ST logic styles exhibit hysteresis by using an extra current path that resists the signal transition of the node through the use of current feedback. In all these styles, extra power consumption is unavoidable as the feedback circuit produces extra current in order to maintain the output. In contrast, the use of a voltage feedback path is suggested in [38] to obtain low power ST gates. This design is named the variable threshold CMOS (VTCMOS) ST design. A VTCMOS ST buffer cascades two CMOS inverters in such a manner that the switching threshold voltage of the first inverter is varied by the output of the second inverter. This technique enables robust operation under low-voltage conditions and improves tolerance to noise over the other existing ST gates but with increased I_{OFF} values.

The conventional ST logic style is static with its switching threshold voltage and power consumption dependent on the aspect ratio of the transistors used in the PUN and PDN of the

gate. Another category of ST logic design represents the clocked logic style and is referred to as the dynamic ST logic style. Different structures of dynamic ST logic and their extension to domino ST logic are available in the literature [74], [75]. The domino ST logic style presented in [75-76] operates in the precharge and evaluation phase depending on the driving clock signal. The domino ST logic attains augmented hysteresis but with the drawback of increased dynamic power when compared to static CMOS logic. Another improved domino ST logic styles [76] are presented that are implemented using footer domino technology. The suggested arrangement reduces leakage and static currents than the footless technique and thus is power efficient. Another domino ST logic style further enhances the hysteresis width of the gates, causing the low to high transition at the output node at comparatively high voltages than domino ST1 logic [76]. The domino logic concept has also been extended for the design of no race (NORA) Domino ST logic system for pipelined applications [33] [77].

1.3 Motivation and Scope of Work

A detailed review of prior work indicates that the design of static ST logic gates follows two approaches, based on the feedback characteristics. The existing work in static ST logic gates employing current feedback offers improvements through reduction in leakage current but at the cost of increased delay. Another design uses voltage booster arrangements in ST logic style but further degrades the speed and noise margin. The DTMOS ST gates show speed advantage at the cost of high power consumption and additional fabrication complexity. Thus, there exists a need for an improved static ST logic style which can achieve improved noise margins and speed without much increase in power.

The performance of the existing ST logic gates with voltage feedback shows high noise margins but is limited by the reduced I_{ON}/I_{OFF} values and high delay values. Thus, the realization of static ST logic style with voltage feedback can further be enhanced by exploring design techniques such that leakage current values can be lowered. So, there is a need to design low leakage ST logic gate topologies

The energy-constrained applications require gates with improved noise immunity and speed. Dynamic ST logic gates improve speed over static logic counterparts at the cost of noise immunity. Despite of these advancements, existing dynamic ST logic structures continue to suffer from degraded noise immunity under low-voltage operation and inherent speed–power trade-offs**.** Consequently, the scope of the present work is directed toward enhancing the overall performance of dynamic ST logic**,** with specific emphasis on optimization of speed and noise immunity.

Several studies in the literature emphasize that scaling of MOSFETs into the nanometer regime introduces critical challenges, including short-channel effects, increased leakage, and mobility degradation, all of which adversely impact the performance of CMOS circuits. To address these issues, carbon nanotube FETs (CNTFETs) have been explored as a promising alternative over MOSFETs because it offers near-ballistic transport, high carrier mobility, and reduced leakage currents [78-82]. Hence, incorporating CNTFET devices into ST gate design can be explored for the performance enhancement of ST gates in the nanometer regime.

Motivated by these gaps, the present research aims to formulate well-defined objectives focused on enhancing the performance of ST logic gates through improved circuit design.

1. Design of enhanced performance Schmitt trigger logic gates.

2. Design of low leakage Schmitt trigger logic gates.

3. Design of high performance dynamic Schmitt trigger logic gates.

4. Design of process invariant Schmitt trigger logic gates.

1.4 Organization of the Thesis

Chapter 1: Introduction

This chapter presents the evolution of the Schmitt trigger logic design and its significance in energy-constrained applications. A comprehensive study of the available literature on ST logic is conducted. The key findings are summarized and further analysed to identify the research gaps. Finally, a brief description of the thesis layout is given.

Chapter 2: Existing ST gates

The study of conventional ST logic gates is presented in this chapter. The circuit operations of conventional static and dynamic ST logic gates are explained followed by a description of improvements proposed in the literature on these conventional structures. Various performance parameters related to the ST logic gates are presented along with their mathematical formulation. The realizations of the basic logic gates based on the static and dynamic ST logic styles are also included in this chapter.

Chapter 3: Improved current feedback static Schmitt trigger logic gates

This chapter presents two new ST logic styles with current feedback. A three stage ST logic is introduced to obtain hysteresis. The delay performance of the three stage ST style is further improved by introducing transmission gates in the ST logic style. The functionality of the proposed gates is explained and verified through simulations, along with the performance comparison with existing ST gates. The proposed gates are also tested for their robustness and sensitivity through process corner and voltage variation.

Chapter 4: Improved voltage feedback static Schmitt trigger logic gates

This chapter presents a novel stacked variable threshold CMOS ST logic style. Mathematical formulations related to the improvement in noise immunity and reduction in leakage current values are put forward. The performance of the proposed ST gates is compared with existing counterparts through simulations using 45 nm PTM CMOS technology parameters. The logic is further verified through layout simulations and is tested for its robustness and sensitivity through process corner and voltage variation analysis.

Chapter 5: Modified domino Schmitt trigger logic gates

This chapter delves into the design of dynamic ST logic. A new design approach is introduced in this chapter for the realization of a domino ST logic. The performance of the proposed domino ST logic is evaluated under process variation at different corners. The characterization, like the voltage transfer curve, the effect of change of channel width of the keeper transistor,

and voltage variation on the performance parameters of the proposed logic, is performed. The proposed logic is also tested for its reliability through Monte Carlo analysis.

Chapter 6: CNTFET based Schmitt trigger logic gates

In this chapter, process invariant CNTFET ST logic is presented, and different CNTFET-based logic gates are proposed. The operation is analyzed, and its functionality is verified through simulations. The performances are compared with MOS-based ST logic gates. The effect of variations on the performance parameters is also studied.

Chapter 7: Conclusion and future scope

In this chapter, the presented work is summarized and concluded with a thought on the prospective future scope.

1.5 Conclusion

This chapter has highlighted the growing importance of energy-constrained applications and the need for circuit techniques that enable reliable operation at low supply voltages. The power supply reduction techniques have been explored to facilitate low-voltage operation; however, these techniques suffer from degraded I_{ON}/I_{OFF} values and reduced noise immunity. In this context, ST logic emerges as a promising solution due to its inherent noise immunity and robustness at reduced supply voltages. The fundamental principles of Schmitt trigger operation have been discussed in this chapter to establish the necessary background. Furthermore, the existing research gaps in Schmitt trigger logic design have been presented. Based on these gaps, the research objectives of the present work have been clearly defined, providing a strong foundation for the subsequent chapters of the thesis.

Chapter 2

Existing ST gates

2.1 Introduction

The previous chapter presents a background, motivation, and research objectives for the work on ST gates. This chapter consists of a comprehensive literature survey on ST logic gates categorized as static and dynamic ST logic gates. Building upon these insights, this chapter provides an understanding of the operational principles, design methodologies, and associated performance parameters of ST logic gates.

2.2 Static ST Logic Style

The block diagram of a generic static ST logic gate consists of a pull up network (PUN) and a pull down network (PDN) followed by a feedback network (FBN), as shown in Fig. 2.1. The PDN uses NMOS transistors to implement the logic function, while the PUN utilizes PMOS transistors to implement its dual logic. The FBN consists of a separate PMOS and NMOS transistor pair driven by the output of the gate and provides feedback by connecting the respective source terminal to the PUN and PDN. A ST logic gate offers effective suppression of leakage current that minimizes output level degradation and exhibits hysteresis for improved noise immunity.

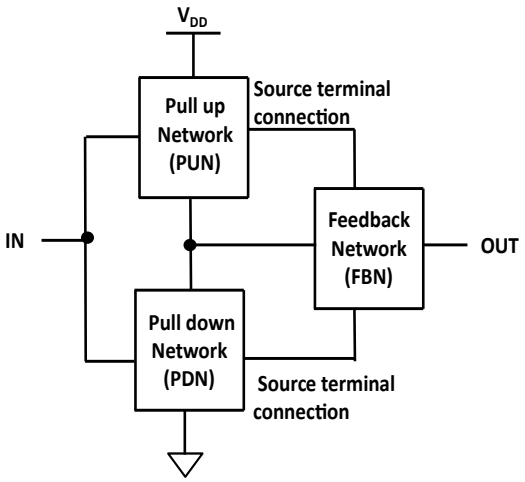


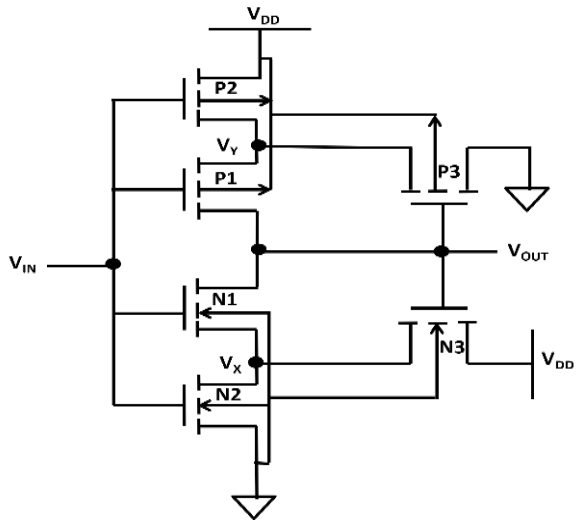
Fig. 2.1 Block diagram of static ST logic gate

2.2.1 Conventional ST logic Inverter

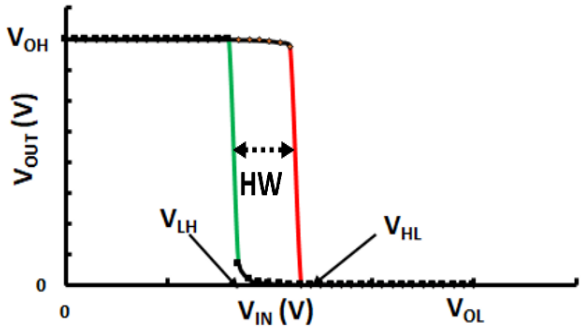
The schematic of a conventional ST logic inverter is shown in Fig. 2.2 (a). The transistors (P1, P2) form the PUN, while the transistors (N1, N2) define the PDN. The output (V_{OUT}) is fed back to these networks through FBN with transistors (P3, N3). For a low value of input V_{IN}, transistors (P1, P2) conduct such that the output node V_{OUT} is charged to a high level V_{OH}. Alternatively, for a high value of input V_{IN}, transistors (N1, N2) conduct and V_{OUT} attains a low level V_{OL}. The presence of feedback in the ST inverter results in two different switching threshold voltages in contrast to a single threshold voltage of a CMOS inverter. Further, for a low input signal V_{IN}, transistor N3 conducts such that the source potential of transistor N1, V_X is increased. This forces drain to source voltage of transistor N1 close to zero and more specifically, gate to source voltage of transistor N1 negative which results in an exponential decrease in the leakage current, I_{OFF}. This causes an effective leakage quenching from the

output node or the redirection of leakage of N1 through N3, which consequently minimizes the output level degradation.

The presence of feedback in the ST inverter results in two different switching threshold voltages in contrast to a single threshold voltage of a CMOS inverter. The corresponding voltage transfer curve (VTC) is shown in Fig. 2.2(b). When V_{IN} is increased from a low to a high voltage level, the input voltage at which the output voltage makes a high-to-low transition is represented as V_{HL}. Similarly, when V_{IN} is decreased from a high to low voltage level, the input voltage at which the output makes a low-to-high transition is represented as V_{LH}. The difference between the V_{HL} and V_{LH} is evaluated as the hysteresis width ($V_{HW} = V_{HL} - V_{LH}$). This voltage window creates a buffer zone that prevents the circuit from switching states due to small or transient noise signals. The larger the hysteresis window, the better immune is the circuit to noise [38]. Thus, ST logic gates exhibit hysteresis and have enhanced noise immunity in comparison to CMOS logic gates [38].



(a)



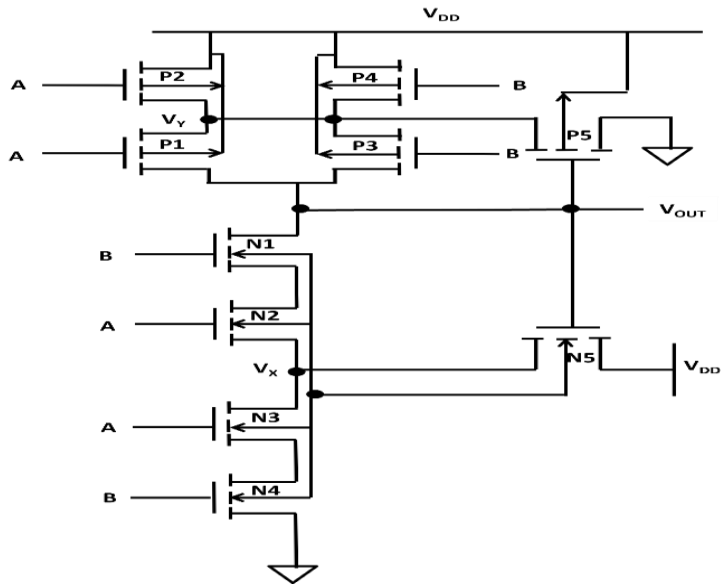
(b)

Fig. 2.2 Conventional ST logic inverter (a) Schematic diagram (b) VTC

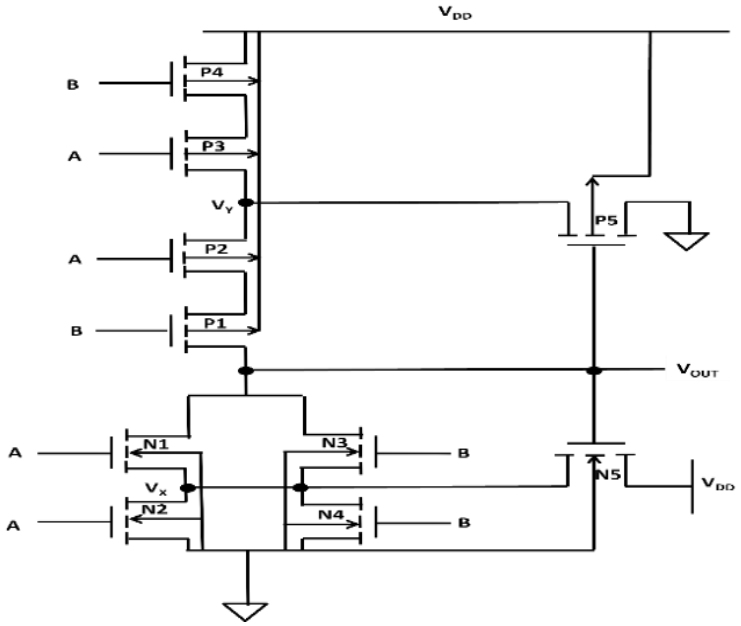
The advantages of conventional ST Logic inverter can be availed by applying the principle to the design of complex functions rather than simple inverting function. The fundamental requirement of a ST logic gate is the existence of a middle node within the PUN and PDN,

which can be connected to the FBN for leakage quenching. Thus, it is evident that the NMOS connected to this node should be conducting when a low value at the output node is required and non-conducting otherwise. The same has to be maintained for PMOS blocks for high output value. Thus, the driving transistors N1, N2, P1, and P2 in the conventional ST inverter are replaced by the corresponding NMOS/PMOS function blocks to allow implementation of any arbitrary block. For example, the realization of a two-input ST NAND (NAND2) gate replaces the PMOS (P1/P2) transistors in PUN with parallel PMOS (P1, P2, P3 and P4) structures. Analogously, the NMOS transistors (N1, N2) in the PDN are replaced with a series-connected NMOS transistors (N1, N2, N3, N4) as shown in Fig. 2.3 (a) The output V_{OUT} in feedback through FBN to node V_X and V_Y for leakage quenching and improvement in noise immunity.

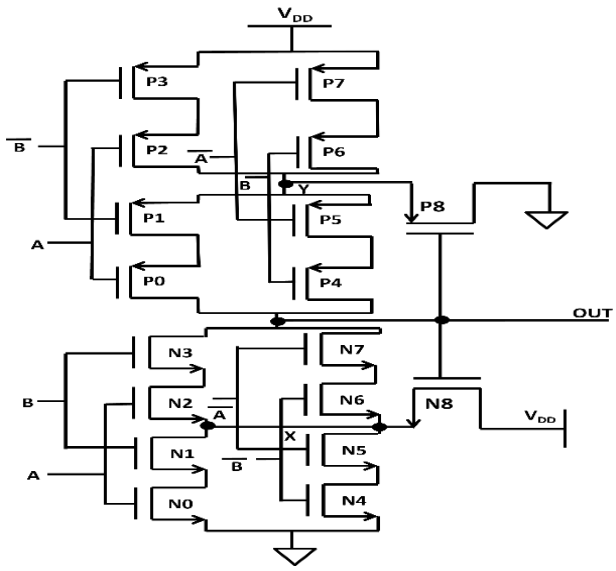
The same principle is applied for the realization of 2-input ST NOR (NOR2) gate as shown in Fig. 2.3(b). The transistors (N1, N2) (P1,P2) in the PDN and PUN of the ST inverter are replaced by parallel NMOS structures (N1, N2, N3, N4) and series connected PMOS structures (P1, P2, P3, P4), respectively. The circuit of a conventional two-input exclusive-OR (XOR2) ST gate is shown in Fig. 2.3 (c). The transistors (N0-N7) in the PDN and its dual in PUN with transistors (P0-P7) implement the XOR2 functionality. Further, transistors N8 and P8 form the feedback network by providing positive feedback in the gate. The additional feedback network offers the advantage of reduced leakage current that avoids the degradation of output voltage levels from their nominal values as well as better noise immunity over CMOS logic gates [26], [28]. For the case when both the inputs have different logic levels, the PUN conducts and a high output voltage is produced at the output node, OUT. In this case, the feedback transistor N8 conducts such that the intermediate node X in the PDN is charged. This causes the gate-source voltage of the inner transistors N2 and N6 to enter the negative region, thereby further reducing their leakage current. For the case when both the inputs are at a high logic level, the PDN transistors conduct such that the output node OUT is discharged and a low voltage level is obtained at the output.



(a)



(b)



(c)

Fig. 2.3 Schematic of conventional ST logic gates (a) NAND2 (b) NOR2 (c) XOR2

2.2.2 Dynamic Threshold MOSFET ST Logic Gate

An improved ST logic style named dynamic threshold MOSFET ST logic (DTMOS ST) gate is proposed in [30-33]. The regular MOSFETs in conventional ST logic gate are replaced with DTMOS transistors. The block diagram of a DTMOS ST logic gate consisting of DTMOS transistors in PUN, PDN and FBN is shown in the Fig. 2.4. The source terminal of DTMOS transistors in FBN is connected to the middle point in PUN and PDN.

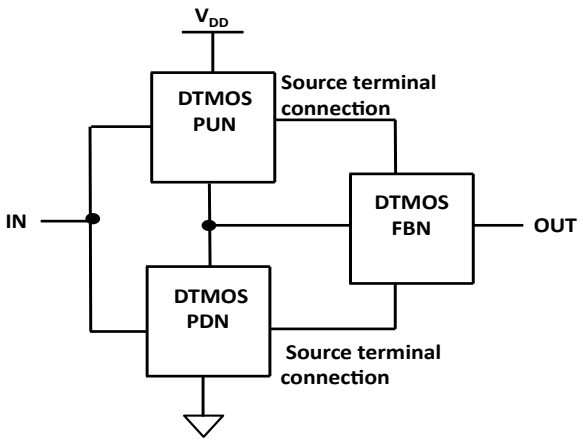
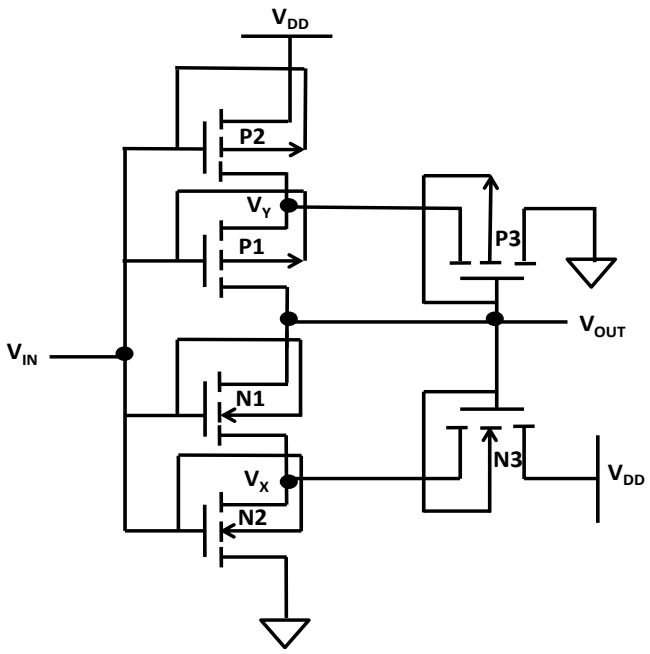


Fig. 2.4 Block diagram of DTMOS ST logic gate

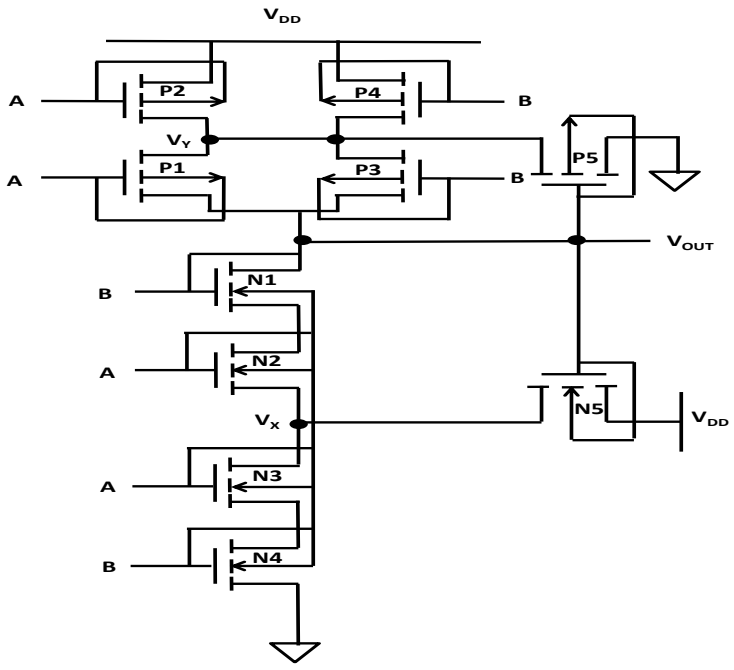
The MOS schematic of a DTMOS ST logic inverter is shown in Fig. 2.5 (a). The PUN consists of DTMOS PMOS transistors (P1, P2), PDN has DTMOS NMOS transistors (N1, N2), along with FBN having DTMOS transistors (P3, N3). The feedback transistors are driven by the output FBN, and the source terminals are connected to the respective middle nodes node V_X and V_Y. When a low logic level is applied at V_{IN}, the PUN is activated, resulting in a high logic level at the V_{OUT} node. The high output voltage turns on transistor N3. Owing to the DTMOS configuration, the threshold voltage of the transistor N3 is reduced, thereby a higher voltage in comparison to conventional static ST inverter is obtained at the source potential of transistor N1. This mechanism leads to an increase in the upper switching threshold voltage with reference to the conventional counterpart. Conversely, when a high logic level is applied at V_{IN}, the lower switching threshold voltage is reduced. This arrangement improves noise immunity and I_{ON}/I_{OFF} value at the cost of increased power consumption.

The same design principle which is followed in conventional static ST gates to realize complex logic functions is applied. The circuit diagrams for NAND2 and NOR2 gates using DTMOS ST logic style are drawn in Fig. 2.5 (b) and (c), respectively.

An improved ST logic named dynamic threshold MOS (DTMOS) ST is suggested in [30-33]. The regular MOSFETs in the conventional ST gate are replaced with DTMOS transistors. The corresponding DTMOS ST XOR2 gate is shown in Fig. 2.5 (d). The PDN and PUN have DTMOS NMOS transistors (N0-N7) and DTMOS PMOS transistors (P0-P7), respectively, along with DTMOS feedback transistors. A DTMOS ST gate has improved delay at the cost of increased switching current and power due to the low threshold voltage observed for DTMOS transistors in the operation of the gate.


VDD
P2
VY
P1
P3
VOUT
VIN
N1
N3
VDD
VX
N2

(a)


VDD
A
P2
P4
B
VY
A
P1
P3
B
P5
VOUT
B
N1
A
N2
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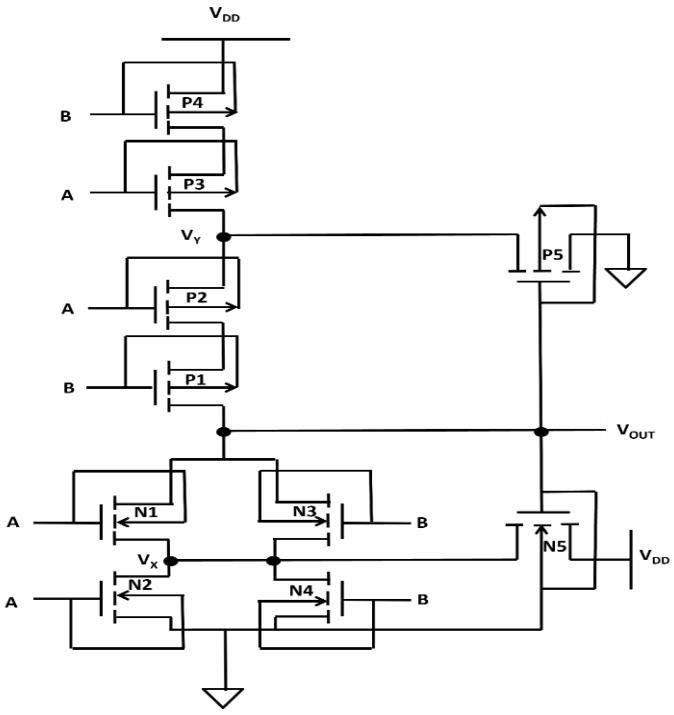
A
N3
B
N4

(b)



(c)

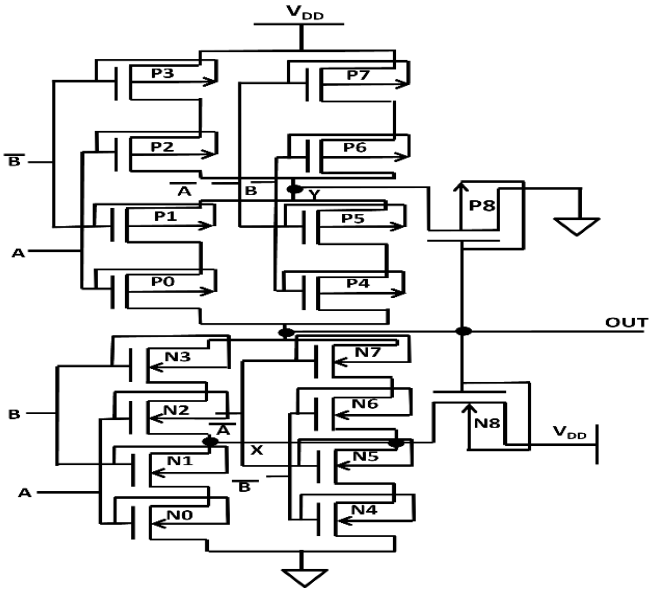


Fig.2.5 Schematic of DTMOS ST gates (a) inverter (b) NAND2 (c) NOR2 (d) XOR2

2.2.3 Variable Threshold CMOS ST Logic Gate

The conventional static ST logic style exhibits hysteresis by introducing an additional current path that opposes the transition of the internal node through current-based feedback. In this approach, extra power consumption is inevitable because the feedback circuitry generates additional current to sustain the output level. In contrast, a voltage-based feedback mechanism

is proposed to achieve low-power ST logic gates. This approach is known as the variable threshold CMOS ST (VTCMOS ST) design. The block diagram of the VTCMOS ST gate consists of two cascaded inverters having the first inverter as a CMOS inverter followed by a DTMOS inverter, as shown in Fig. 2.6. The output of the DTMOS inverter is connected to the substrate terminal of the transistors in the CMOS inverter to obtain hysteresis.

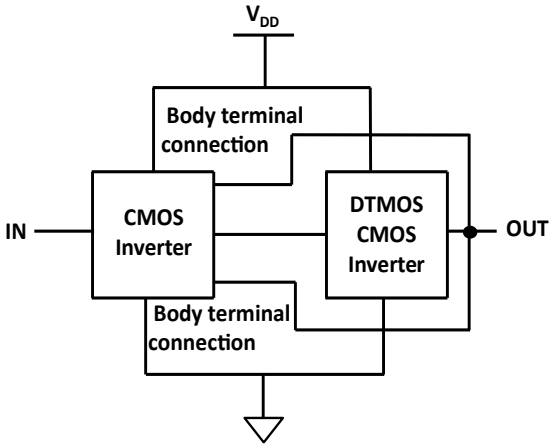


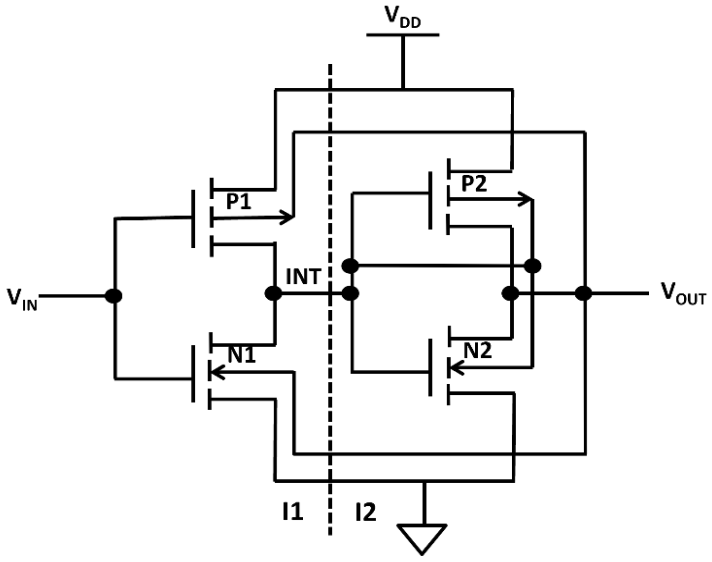
Fig. 2.6 Block diagram of VTCMOS ST logic gate

A VTCMOS ST logic buffer cascades two inverters ((I1: N1, P1), (I2: N2, P2)) in such a manner that inverter I2 controls the substrate of transistors in inverter I1 as shown in Fig. 2.7 (a). The switching threshold voltage of the transistors in I1 is varied by the output of the second inverter. This technique results in significantly improved noise-immune ST gates over the other existing ST gates but with increased I_{OFF} values.

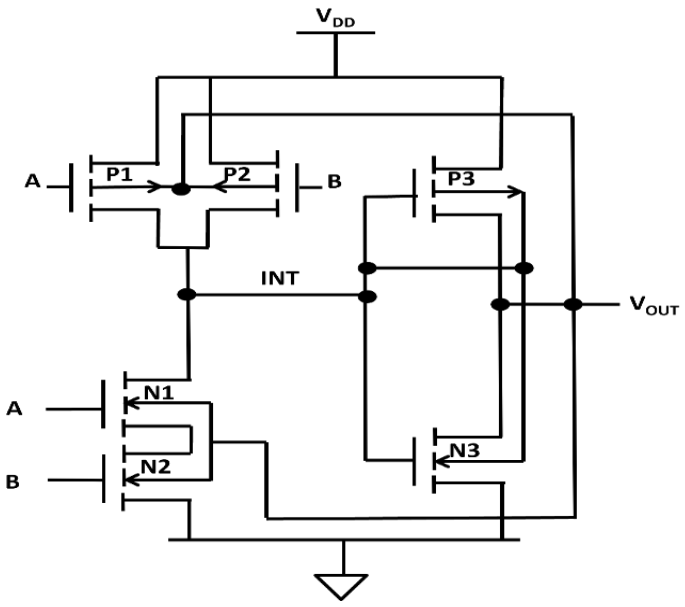
The design principle followed to realize complex functions in VTCMOS ST logic style involves realizing the given functionality in the first stage. The PDN of I1 in the first stage realizes the given functionality, while its dual is implemented in PUN. The first stage is then followed by the DTMOS inverter with its output being fed to the substrate terminals of the transistors in the first stage. By following the same design principle, the circuit diagram of two-input VTCMOS ST NAND2 (VTCMOS NAND2) gate is shown in Fig. 2.7 (b). The first inverter of VTCMOS ST NAND2 gate consists of parallel connected PUN transistors (P1, P2) and series connected PDN transistors (N1, N2) driven by inputs A and B. The second stage is a DTMOS inverter comprising of DTMOS transistors P3 and N3. Similarly, the circuit diagram of a two-input VTCMOS ST NOR2 (VTCMOS ST NOR2) gate is shown in Fig. 2.7 (c). The first stage consists of series connected PUN transistors (P1, P2) and parallel connected PDN transistors (N1, N2). The second stage consists of DTMOS transistors P3 and N3. It is to be noted that the output terminal of the second stage is connected to the substrate terminal of the first stage transistors in both the NAND2 and NOR2 gates.

Another ST logic gate presented in [38-41] incorporates the advantage of the variable threshold technique in ST logic style and is referred to as variable threshold CMOS (VTCMOS) ST logic. The schematic of a VTCMOS ST XOR2 gate is shown in Fig. 2.7 (d). It comprises two stages in which the first stage implements the functionality in PDN (transistors: N0-N3) and its dual in PUN (transistors: P0-P3). It is then followed by a second stage having a DTMOS inverter (N4, P4). It is worth noting that the substrate terminals of transistors in the first stage are controlled by the output of the DTMOS inverter in the second stage. The threshold voltage of the transistors is accordingly varied and thus, the gate is called a VTCMOS ST XOR2 gate.

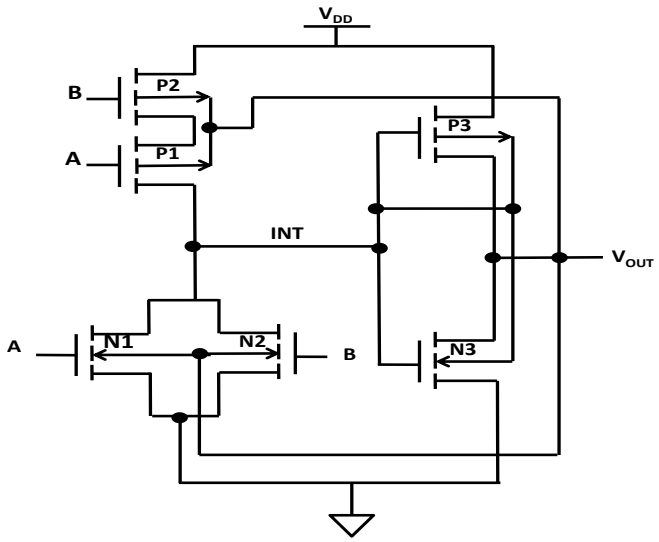
This gate consumes less power at the expense of increased delay when compared to the conventional ST and DTMOS ST XOR2 gates.



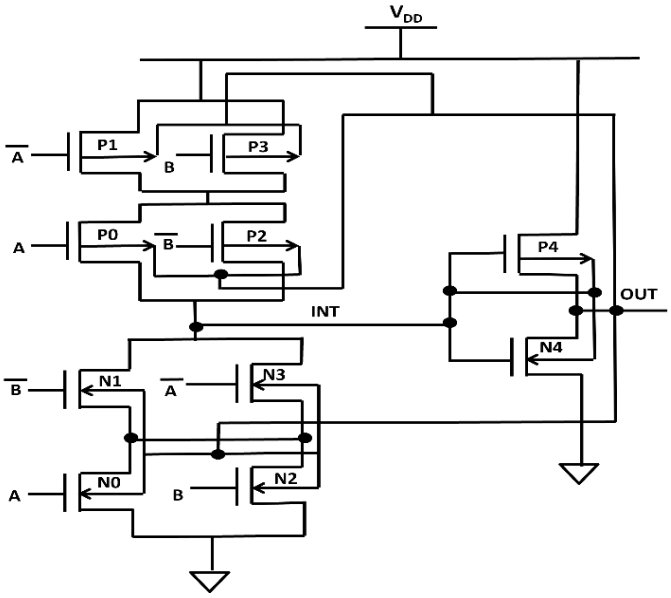
(a)



(b)



(c)



(d)

Fig. 2.7 Schematic of VTCMOS ST logic gates (a) inverter (b) NAND2 (c) NOR2 (d) XOR2

2.3 Performance parameters

In this subsection, different performance parameters associated with a conventional ST logic gate are explained.

2.3.1 Voltage swing

It is defined as the difference between the maximum output voltage (V_{OH}) and the minimum output voltage (V_{OL}) obtained from a gate. The voltage swing (V_{SW}) of a conventional ST inverter (Fig. 2.2 (a)) can be obtained by expressing the output voltage, V_{OUT} as:

$$V_{OUT} = V_{DD} - R_P I_{PUN} \quad (2.1)$$

where R_P is the equivalent resistance of the PUN and I_{PUN} is the total current in the PUN, respectively.

When the input voltage, V_{IN} is low, the transistors (N1, N2) in the PDN are in the cut-off region such that the total current in the PDN, I_{PDN} is zero except for small leakage currents.
The Kirchhoff's current law (KCL) at the output node can be written as,

$$I_{PUN} = I_{PDN} = 0 \quad (2.2)$$

Therefore, by using Eq. (2.1), the output voltage, V_{OH} is calculated as:

$$V_{OUT} = V_{OH} = V_{DD} \quad (2.3)$$

Alternatively, when the input voltage V_{IN} is high, the transistors P1, P2 in the PUN are turned OFF. In this case, the condition mentioned in Eq. (2.1) is satisfied, and then the drain-to-source voltage of the NMOS transistor becomes equal to zero. Consequently, the output voltage of the circuit is calculated as:

$$V_{OUT} = V_{OL} = 0 \quad (2.4)$$

Therefore, the voltage swing of a conventional ST inverter is calculated as

$$V_{SW} = V_{OH} - V_{OL} = V_{DD} \quad (2.5)$$

2.3.2 Hysteresis Width

Hysteresis width (V_{HW}) is defined as the difference between the input switching threshold voltages for rising and falling transitions of the input signal. It quantifies the extent of hysteresis introduced in a circuit to enhance noise immunity and suppress spurious switching due to input fluctuations. The hysteresis width is obtained by performing a DC voltage sweep analysis at the input while monitoring the output transition points. When the input voltage is swept from low logic level to high logic level, the corresponding input voltage at which the output switches state from high logic level to low logic level is represented as V_{HL}. Similarly, for the case when the input voltage is swept from high logic level to low logic level, the input voltage at which the output switches back from low logic level to high logic level is represented as V_{LH}. The hysteresis width is then calculated as the difference between the two switching thresholds as given by:

$$V_{HW} = V_{HL} - V_{LH} \quad (2.6)$$

The V_{HW} determination for the conventional static ST inverter requires calculation of switching threshold voltages. These voltages can be determined by considering the basic circuit as three pairs of CMOS transistors. The first is a standard inverter with transistors N1 and P1, while

transistors N3, N1 and P3, P1 introduce hysteresis by feeding back the output voltage to nodes V_X and V_Y. For circuit analysis, the threshold voltages of all the NMOS and PMOS transistors are assumed to be V_{thn} and V_{thp}, respectively.

Case I: For V_{IN} = 0 V, the two stacked PMOS transistors P1 and P2 are ON with negligible conducting drain current, since NMOS transistors N1 and N2 are OFF and V_{OUT} =V_{DD}. The transistor P3 is OFF and N3 is at the threshold of conduction with $V_X = V_{DD}$-V_{thn}. When V_{IN} rises to V_{thn},N2 starts to turn ON, but N1 is OFF because V_X is greater than V_{thn}. In this condition, both N2 and N3 operate in the saturation region. The saturation current through transistors N2, N3 [1] is expressed as:

$$I_{D,N2} = W_{N2} V_{SAT,N2} C_{OX} \frac{(V_{gs} - V_{thn})^2}{(V_{GS} - V_{thn}) + E_{C,N2} L_{N2}} \tag{2.7}$$

$$I_{D,N3} = W_{N3} V_{SAT,N3} C_{OX} \frac{(V_{gs} - V_{thn})^2}{(V_{GS} - V_{thn}) + E_{C,N3} L_{N3}} \tag{2.8}$$

where $W_{N2}, V_{SAT,N2}, E_{C,N2}, L_{N2}$ and $W_{N3}, V_{SAT,N3}, E_{C,N3}, L_{N3}$ represent the channel width, saturation velocity, critical electric field, and channel length of transistors N2 and N3, respectively.

By equating the drain current of N2 and N3, the potential at node X can be expressed as:

$$V_X = V_{DD} - V_{thn} - R_N \sqrt{\frac{V_{sat,N2} E_{C,N3}}{V_{sat,N3} E_{C,N2}}} (V_{IN} - V_{thn}) \tag{2.9}$$

where $R_N = \sqrt{\frac{W_{N2}}{W_{N3}}}$

Further, increase in V_{IN} causes subsequent decrease in V_X. Thus, the input voltage at which output changes to low voltage, higher switching threshold V_{HL} is computed by equating the current of transistor N1 and the equivalent PMOS transistor (Pe).

$$I_{D,N1} = I_{D,Pe} \tag{2.10}$$

$$W_{N1} V_{SAT,N1} C_{OX} \frac{(V_{gs} - V_{thn})^2}{(V_{GS} - V_{thn}) + E_{C,N1} L_{N1}} = W_{Pe} V_{SAT,p} C_{OX} \frac{(V_{sg} - |V_{thp}|)^2}{(V_{sg} - V_{thp}) + E_{C,P} L_{Pe}} \tag{2.11}$$

where W_{pe} and L_{pe} are the equivalent width and length of series connected P1 and P2 transistors, and $V_{SAT,P}$ and $E_{C,P}, L_{N2}$ are the saturation velocity and critical electric field of the PMOS transistor. By using V_X as given by Eq. (2.9) and with $V_{IN} = V_{HL}$, the above equation is solved for V_{HL} as:

$$V_{HL} = \frac{V_{DD} + V_{tp} + B_1\left(V_{DD} + R_N\sqrt{\frac{V_{sat,N2}E_{C,N3}}{V_{sat,N3}E_{C,N2}}}V_{thn}\right)}{1 + B_1\left(1 + R_N\sqrt{\frac{V_{sat,N2}E_{C,N3}}{V_{sat,N3}E_{C,N2}}}\right)} \quad (2.12)$$

Where $B_1 = \sqrt{\frac{2W_N V_{SAT,N}E_{C,P}}{E_{C,N}W_{Pe}V_{SAT,P}}}$

Similarly, for the case when the input voltage V_{IN} is decreased from V_{DD} to 0V, the input voltage is equal to the lower threshold voltage V_{LH} and is calculated as:

$$V_{LH} = \frac{R_P\sqrt{\frac{V_{SAT,P2}}{V_{SAT,P3}}\frac{E_{C,P3}}{E_{C,P2}}}\left(V_{DD} + V_{thp}\right) + B_2V_{thn}}{\left(1 + R_P\sqrt{\frac{V_{SAT,P2}}{V_{SAT,P3}}\frac{E_{C,P3}}{E_{C,P2}}} + B_2\right)} \quad (2.13)$$

Where $B_2 = \sqrt{\frac{W_{Ne}V_{SAT,N}E_{C,P}}{2E_{C,N}W_PV_{SAT,P}}}$

The difference between the higher switching threshold Eq. (2.12) and the lower switching threshold voltage Eq. (2.13) provides the hysteresis width, which leads to noise immunity of the circuit.

Similarly, the V_{HW} determination for the VTCMOS ST buffer requires calculation of switching threshold voltages, V_{HL} and V_{LH}. For the VTCMOS ST buffer at V_{HL}, the transistors N1 and P1 operate in the saturation region with their substrate to source potential maintained at zero bias and forward bias, respectively. The saturation current through transistors N1 and P1 is equated to calculate the switching threshold voltage, V_{HL}. The saturation current through transistors N1 ($I_{D,N1}$) and P1 ($I_{D,P1}$) [1] is expressed as:

$$I_{D,N1} = W_{N1}V_{SAT,N1}C_{OX}\frac{(V_{gs} - V_{th0,N1})^2}{(V_{GS} - V_{th0,N1}) + E_{C,N1}L_{N1}} \quad (2.14)$$

$$I_{D,P1} = W_{P1}V_{SAT,P1}C_{OX}\frac{(V_{SG} - |V_{th,P1}|)^2}{(V_{DD} - V_{IN} - |V_{th,P1}|) + E_{C,P1}L_{P1}} \quad (2.15)$$

where $W_{N1}, V_{SAT,N1}, E_{C,N1}, L_{N1}$ and $W_{P1}, V_{SAT,P1}, E_{C,P1}, L_{P1}$ represent the channel width, saturation velocity, critical electric field, and channel length of transistors N1 and P1, respectively. The voltage $V_{th0,N1}$ represents the zero substrate bias threshold voltage of transistor N1 and $V_{th,P1}$ is the forward substrate bias threshold voltage of transistor P1.

The two current equations are equated as:

$$I_{D,N1} = I_{D,P1} \tag{2.16}$$

Substituting the values

$$W_{N1}V_{SAT,N1}C_{OX}\frac{(V_{HL}-V_{th0,N1})^2}{(V_{GS}-V_{th0,N1})+E_{C,N1}L_{N1}} = W_{P1}V_{SAT,P1}C_{OX}\frac{(V_{DD}-V_{HL}-|V_{th,P1}|)^2}{(V_{DD}-V_{IN}-|V_{th,P1}|)+E_{C,P1}L_{P1}} \tag{2.17}$$

By solving Eq. (2.17), V_{HL} is calculated as:

$$V_{HL} = \frac{(V_{DD}-|V_{th,P1}|)R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}+V_{th0,N1}}{1+R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}} \tag{2.18}$$

where $R = \sqrt{\frac{W_{P1}}{W_{N1}}}$

Similarly, the lower switching threshold voltage (V_{LH}) is determined during high to low transition in V_{IN}. At V_{LH}, the transistors N1 and P1 operate in the saturation region with their substrate potential maintained at forward bias and zero bias, respectively.

By following the above method, the lower switching threshold V_{LH} is computed as:

$$V_{LH} = \frac{(V_{DD}-|V_{th0,P1}|)R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}+V_{th,N1}}{1+R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}} \tag{2.19}$$

where $V_{th0,P1}$ is the zero substrate bias threshold voltage of transistor P1, and $V_{th,N1}$ is the forward substrate bias threshold voltage of transistor N1. By using Eq. (2.18) and (2.19), the hysteresis width of the VTCMOS ST buffer (V_{HW_VTCMOS}) is computed as:

$$V_{HW_VTCMOS} = V_{HL} - V_{LH} = \frac{(|V_{th0,P1}|-|V_{th,P1}|)R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}+(V_{th0,N1}-V_{th,N1})}{1+R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}} \tag{2.20}$$

2.3.3 Propagation delay

The average propagation delay (τ_d) of a conventional ST inverter defines the average time required for the input signal to propagate through the inverter. It is determined as the average of the two propagation delay times τ_{PHL} and τ_{PLH} defined as the input-to-output signal delay during the high-to-low and low-to-high transition of the output, respectively.

The input and output voltage waveform of a conventional ST inverter is shown in Fig. 2.8. The propagation delay τ_{PHL} is defined as the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage. The τ_{PHL} can be found from Fig. 2.8 as:

$$\tau_{PHL} = t_1 - t_0 \tag{2.21}$$

Similarly, the propagation delay τ_{PLH} is defined as the propagation delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage. The same is marked in Fig. 2.8 as

$$\tau_{PLH} = t_3 - t_2 \tag{2.22}$$

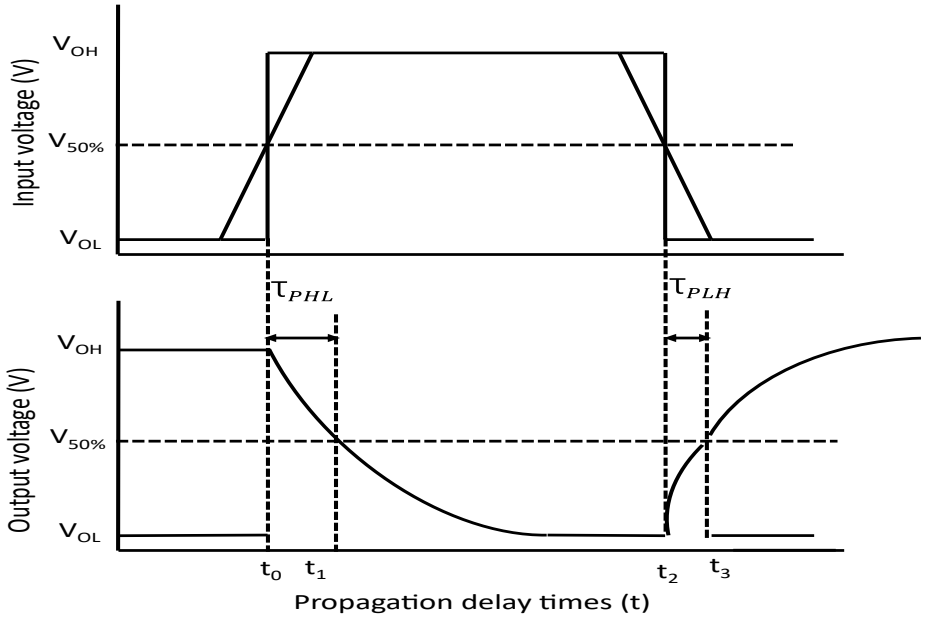


Fig. 2.8 Input and Output voltage waveforms of a conventional ST inverter

Thus, the average propagation delay, τ_d can be compiled as:

$$\tau_d = \frac{\tau_{PHL} + \tau_{PLH}}{2} \tag{2.23}$$

2.3.4 Power Consumption

The steady state power consumption of a conventional static ST inverter is negligible due to fact that both PUN and PDN are never ON simultaneously under static operating conditions. However, there is a small leakage power due to leakage currents. Further, there is another component of power, referred to as dynamic power, during the switching events due to the charging up or charging down of the output load capacitance. The average dynamic power of a conventional ST inverter over one time period (T) can be found as:

$$P_{dyn} = \frac{1}{T}\int_0^T V(t)i(t)dt = C_{load}V_{DD}^2 f \tag{2.24}$$

where C_{load} is the equivalent capacitance connected between the output node of the conventional ST inverter and the ground. The equivalent capacitance is calculated by combining all the capacitances of the ST inverter, as shown in Fig. 2.9. Thus, C_{load} can be expressed as:

$$\begin{aligned} C_{load} = {} & C_{db,N1} + C_{gd,N1} + C_{gs,N1} + C_{sb,N1} + C_{db,P1} + C_{gd,P1} + C_{gs,P1} \\ & + C_{sb,P1} + C_{db,N2} + C_{gd,N2} + C_{db,P2} + C_{gd,P2} + C_{gs,N3} \\ & + C_{gd,N3} + C_{gs,P3} + C_{gd,P3} \end{aligned} \tag{2.25}$$

where C_{db}, C_{gd}, C_{gs}, and C_{sb} are the drain to substrate, gate to drain, gate to source, and source to substrate capacitances associated with the transistors N1 and P1, and C_{db} and C_{gd} are the drain to substrate and gate to drain capacitances of transistors N2 and P2, and C_{gs} and C_{gd} are the gate to source and gate to drain capacitances of transistors N3 and P3.

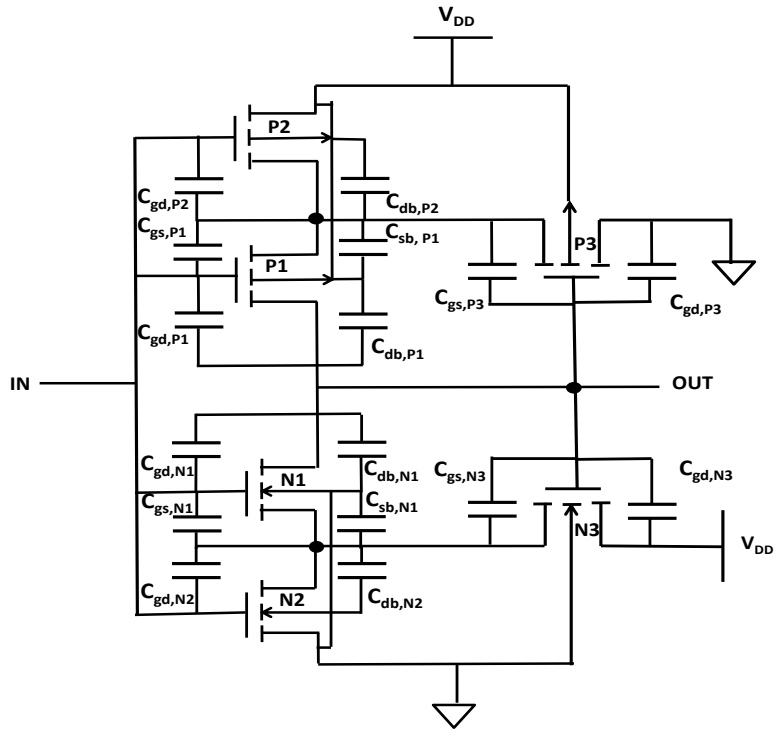


Fig. 2.9 Capacitance associated with each transistor in a conventional ST inverter

2.3.5 Power–Delay Product

Power–Delay Product (PDP) is a performance metric that represents the energy consumed per switching event in a digital circuit. It captures the trade-off between power and speed, making it a widely used parameter for performance evaluation of low-power VLSI circuits.

$$\mathrm{PDP} = \mathrm{P_{dyn}} \times \tau_d \tag{2.26}$$

where P_{dyn} is the dynamic power consumption, and τ_d the propagation delay of the circuit. As power multiplied by time represents energy, PDP has the unit of joules (J).

2.3.6 Leakage Current

In a conventional static ST inverter, for a low value of input $V_{IN,}$ the output node voltage V_{OUT} is high. In this condition, the transistors P1, P2, and N3 conduct and carry the active current (I_{ON}). Also, the transistors N1, N2 and P3 do not conduct such that leakage current (I_{OFF}) exists. The flow of both currents is pictorially represented in Fig. 2.10. The reduction in leakage current in ST gates is derived by finding the ratio of the leakage current through a single transistor equivalent to N1 and comparing it to N1 in the ST inverter.

As N1 is OFF, the leakage current $I_{OFF,\,ST_N1}$ is the subthreshold drain current equation [20] and is given as:

$$\mathrm{I_{OFF,ST_N1}} = \mathrm{I_0 exp}\left(\frac{\mathrm{V_{GS} - V_{th} - \eta V_{DS}}}{\mathrm{nV_T}}\right)\left(1 - \mathrm{exp}\left(\frac{-\mathrm{V_{DS}}}{\mathrm{V_T}}\right)\right) \tag{2.27}$$

where I_0 is a constant dependent on W/L of the transistor, V_{th} is the threshold voltage, η is the drain induced barrier lowering coefficient, n is the subthreshold ideality factor, and V_T is the thermal voltage. By substituting $V_{GS_N1} = -V_X$, $V_{DS_N1} = V_{DD} - V_X$, and neglecting η for the sake of simplification in the above equation, the leakage current through transistor N1 (I_{OFF,ST_N1}) can be expressed as:

$$\mathrm{I_{OFF,ST_N1}} = \mathrm{I_0 exp}\left(\frac{-(\mathrm{V_X + V_{th}})}{\mathrm{nV_T}}\right)\left(1 - \mathrm{exp}\left(\frac{-(\mathrm{V_{DD} - V_X})}{\mathrm{V_T}}\right)\right) \tag{2.28}$$

Similarly, the leakage current through single transistor N1 ($I_{OFF,\,single_N1}$) with $V_{GS}=0$, $V_{DS}=V_{DD}$ can be expressed as:

$$\mathrm{I_{OFF,Single_N1}} = \mathrm{I_0 exp}\left(\frac{-\mathrm{V_{th}}}{\mathrm{nV_T}}\right)\left(1 - \mathrm{exp}\left(\frac{-\mathrm{V_{DD}}}{\mathrm{V_T}}\right)\right) \tag{2.29}$$

Thus, the ratio of leakage currents in the single transistor equivalent to transistor N1 in the conventional ST inverter can be written as:

$$\frac{I_{OFF,Single_N1}}{I_{OFF,ST_N1}} = \frac{\exp\left(\frac{V_X}{nV_T}\right)\left(\exp\left(\frac{V_{DD}}{V_T}\right) - 1\right)}{\left(\exp\left(\frac{V_{DD}}{V_T}\right) - \exp\left(\frac{V_X}{V_T}\right)\right)} \tag{2.30}$$

Further, the node voltage V_X is determined by equating the current flowing through the transistors N2 and N3 in the conventional ST inverter using Eq. (2.27), with $V_{GS_N2} = 0$, $V_{DS_N2} = V_X$, with $V_{GS_N3} = V_{DD}-V_X$, $V_{DS_N3} = V_{DD}-V_X$. It can be approximated as:

$$V_X \approx V_T \ln\left(\frac{I_{0,N2}\exp\frac{V_{DD}}{V_T} + I_{0,N3}}{I_{0,N2} + I_{0,N3}}\right) \tag{2.31}$$

where $I_{0,N2}$ and $I_{0,N3}$ are constants representing the transistor strength of N2 and N3, respectively, and are impacted by the respective W/L ratio. By substituting the value of V_X from Eq. (2.31) in Eq. (2.30), the ratio of leakage current can be approximated as:

$$\frac{I_{OFF,single_N1}}{I_{OFF,ST_N1}} \approx 1 + \frac{I_{0,N2}}{I_{0,N3}} e\exp\left(\frac{V_{DD}}{V_T}\right) \tag{2.32}$$

Hence, it can be seen from the above equation that there is leakage quenching in the ST structure due to the feedback transistor.

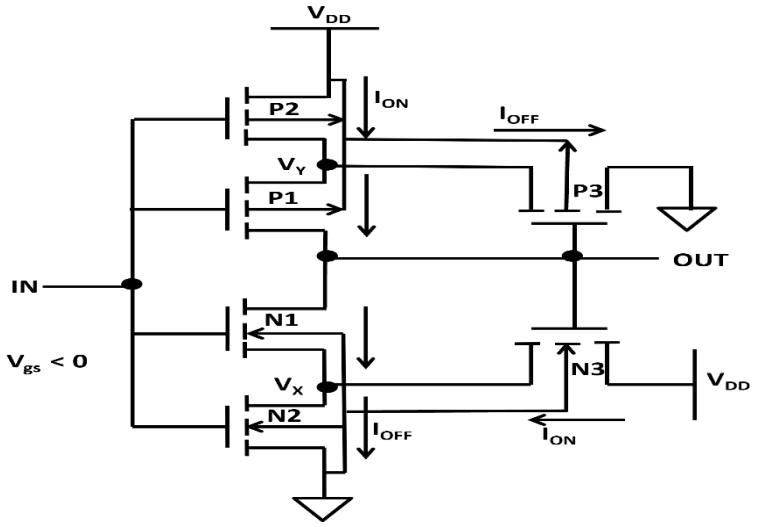


Fig. 2.10 Illustration of I_{ON} and I_{OFF} in a conventional ST inverter

2.4 Design Examples using ST styles

Two design examples, namely a 4:1 multiplexer and a full adder, are considered to verify the effectiveness of the static ST gates [42-43].

a. Multiplexer

A multiplexer is an important part of digital circuits. It is realized in ST logic style by using conventional ST, DTMOS ST, and VTCMOS ST styles. The block diagram of a 4:1

multiplexer (4:1 MUX) with four input lines A, B, C and D and two select lines S_0 and S_1 is shown in Fig. 2.11. It consists of three 2:1 ST MUXs arranged in two stages. The functionality of a 2:1 MUX with input lines A, B, and select line S is expressed as
Out1= $\overline{S_0}A + SB$.

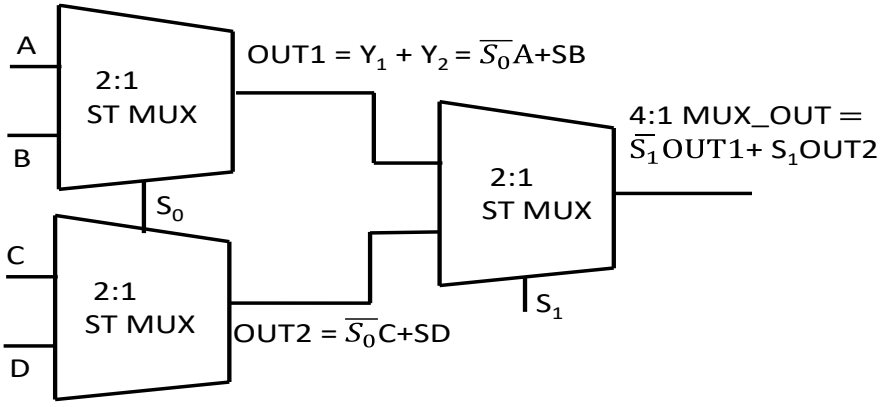
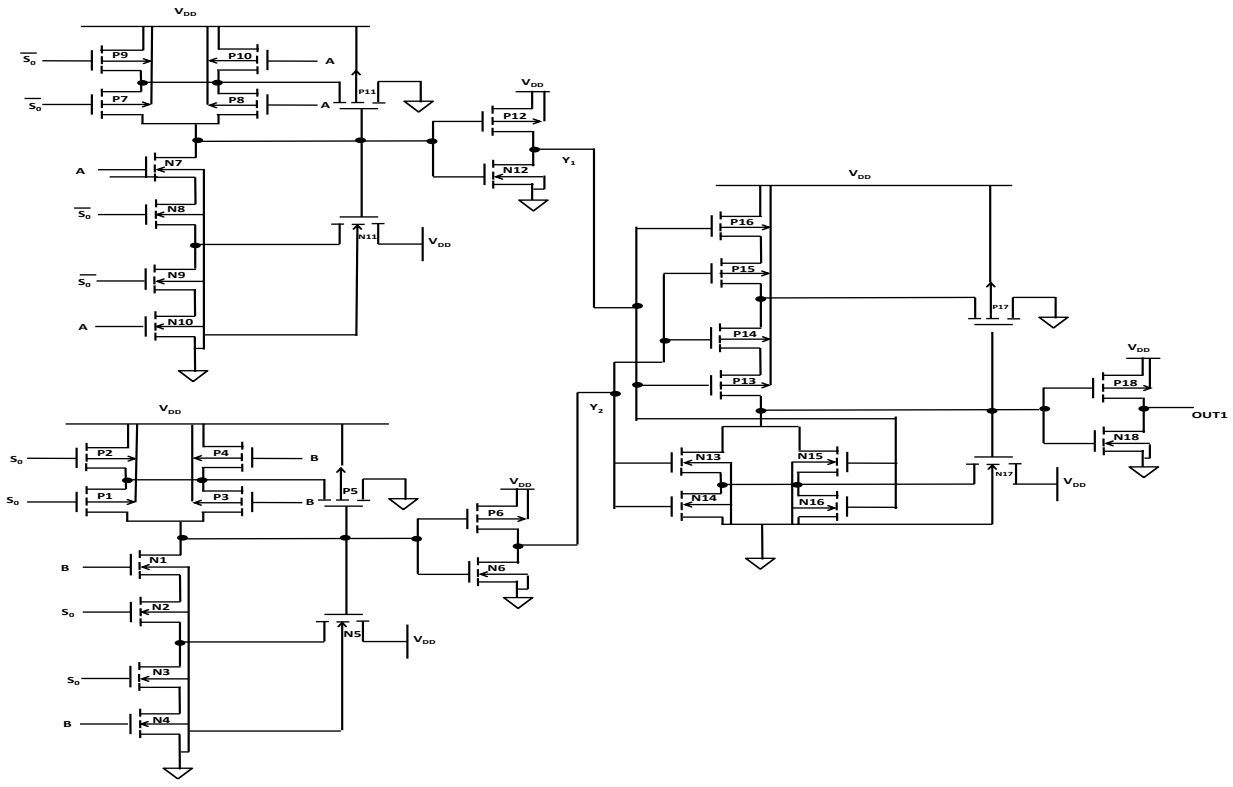
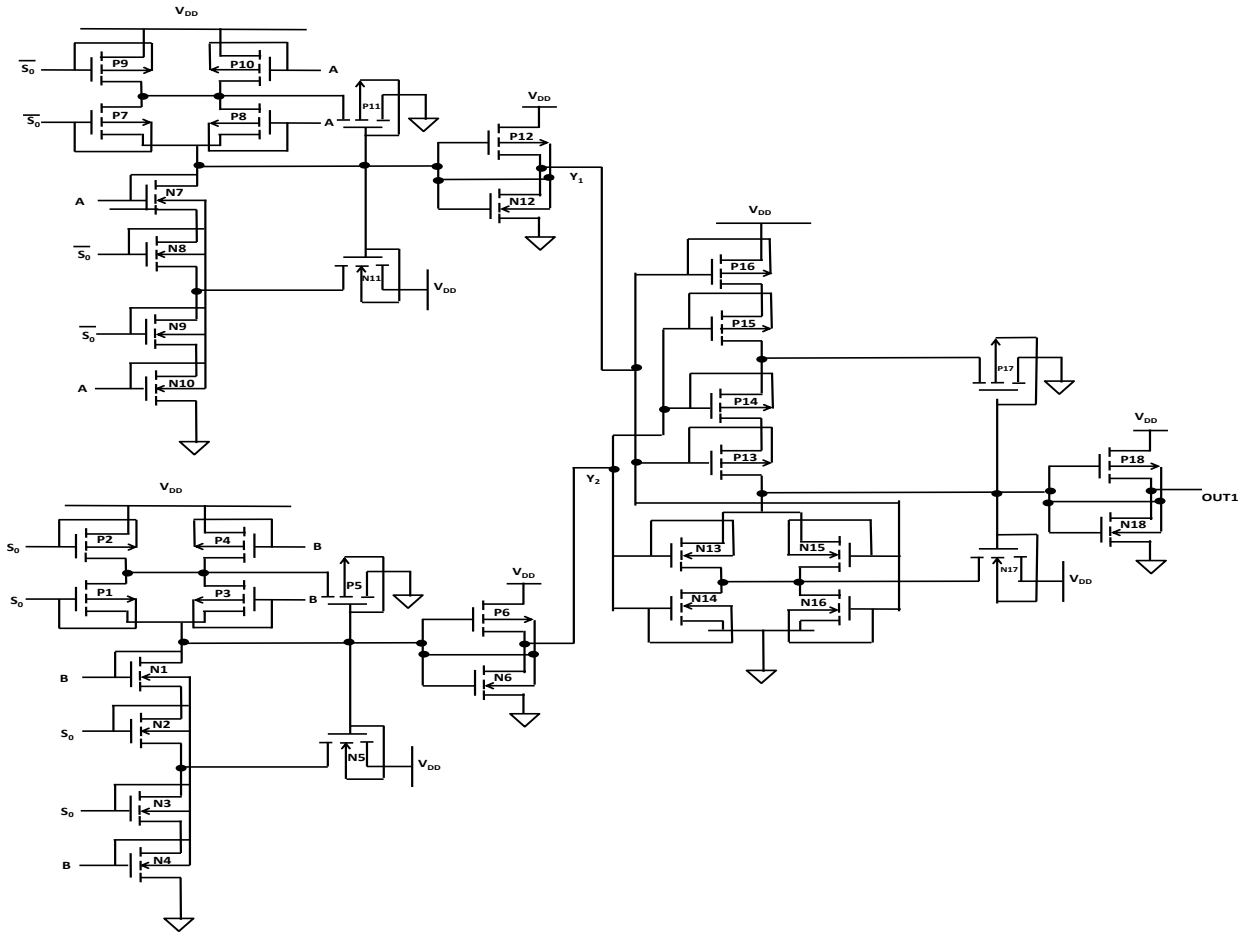


Fig. 2.11 Block diagram of 4:1 MUX

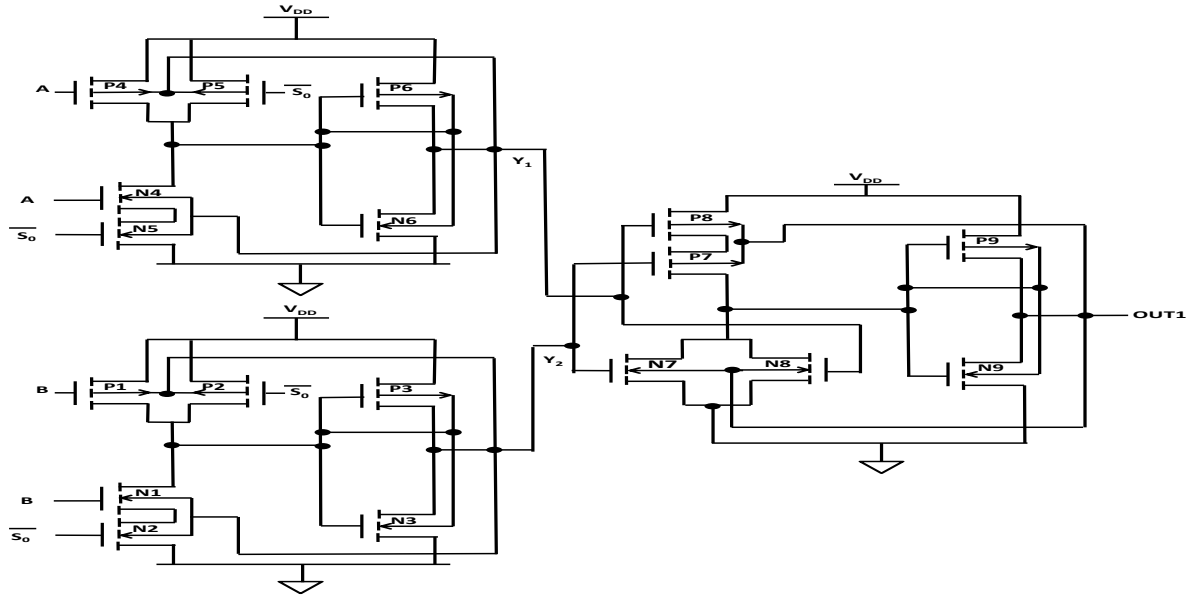
The above equation indicates that two 2-input AND (AND2) gate and one 2-input OR (OR2) gate is required. The complete circuit diagrams for one 2:1 ST MUX realized using conventional ST, DTMOS ST and VTCMOS ST logic styles are shown in Fig. 2.12.



(a)



(b)



(c)

Fig. 2.12 2:1 ST MUX in different static ST logic styles (a) Conventional ST (b) DTMOS ST (c) VTCMOS ST

b. Full Adder

The block diagram of a full adder design is shown in Fig. 2.13. The realization requires two 2-input exclusive-OR gates, two 2-input AND gates, and one 2-input OR gate. The full adder is realized using conventional ST, DTMOS ST, and VTCMOS ST logic styles.

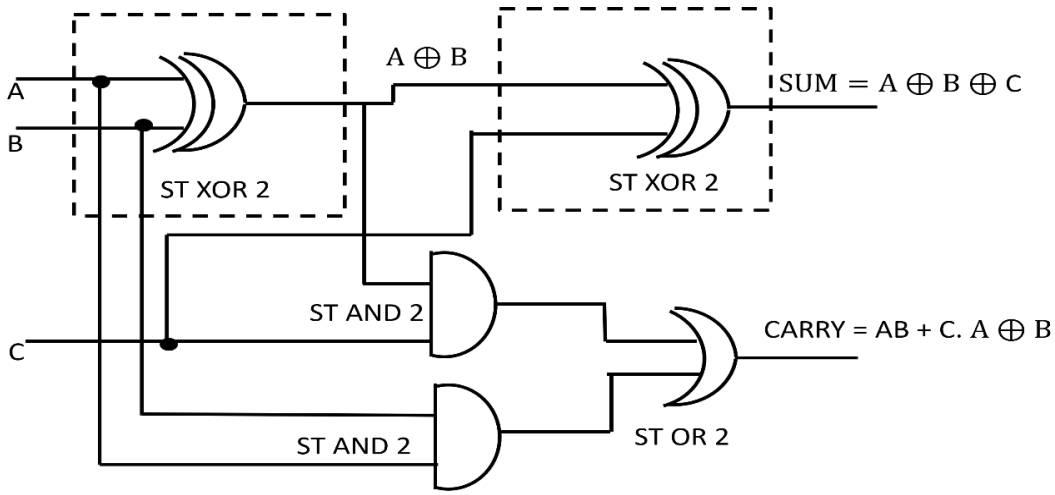


Fig. 2.13 Block diagram of a full adder

The designs of 4:1 MUX and full adder are simulated using 45 nm PTM technology parameters in LTspice simulation. The power supply and load capacitance of the designs are taken as 0.35 V and 100 fF, respectively. The different performance parameters such as hysteresis width (V_{HW}), active current to leakage current ratio (I_{ON}/I_{OFF}), dynamic power (P_{dyn}), and propagation delay (τ_d) are noted, and results are summarized in Tables 2.1 and 2.2, respectively.

The simulated results reveal that the 4:1 VTCMOS ST MUX provides the highest hysteresis width among all the MUXs due to the variable threshold technique. It has 64% more hysteresis width in comparison to the 4:1 DTMOS ST MUX. Also, the I_{ON}/I_{OFF} ratio and propagation delay are improved for the 4:1 DTMOS ST MUX in comparison to the conventional ST and VTCMOS ST MUXs due to the dynamic threshold technique, which leads to reduction in the threshold voltage. With reference to dynamic power, the 4:1 DTMOS ST MUX consumes the highest dynamic power because of extra injection of current through current feedback, which resists change in output due to injection of noise in the input and extra parasitic capacitances. However, the 4:1 VTCMOS ST MUX reduces dynamic power by 63% over the 4:1 DTMOS ST MUX. Further, the VTCMOS ST full adder provides the highest hysteresis width among all the existing full adders. The SUM output of the DTMOS ST full adder has the highest I_{ON}/I_{OFF} value. The propagation delay of the conventional ST adder is the highest, which is the design constraint. The propagation delay of the DTMOS ST adder is comparable with VTCMOS ST adder. The DTMOS ST adder also consumes the highest dynamic power among the existing ST adders, which is another design constraint.

Table 2.1 Performance comparison of different 4:1 ST MUXs

ST styles / Performance comparison	Conventional ST MUX	DTMOS ST MUX	VTCMOS ST MUX
V_{HW} (mV)	58	62	102
I_{ON}/I_{OFF}	955	1970	41
τ_d (ns)	27	9.93	9.87
P_{dyn} (nW)	655	1200	460

Table 2.2 Performance comparison of different ST full adders

ST styles / Performance comparison	Conventional ST Adder	DTMOS ST Adder	VTCMOS ST Adder	Conventional ST Adder	DTMOS ST Adder	VTCMOS ST Adder
	SUM			CARRY		
V_{HW} (mV)	72.1	51.5	102.8	51.2	61.8	92.7
I_{ON}/I_{OFF}	26.5	51	10.2	45.2	95.1	135
τ_d (ns)	15.8	4.4	4.5	10.3	3.4	2.7
P_{dyn} (nW)	72.9	1000	922	389.1	2000	1000

The above results indicate that gate design based on VTCMOS ST logic style offer maximum hysteresis width. The gate design based on DTMOS ST logic style has the highest I_{ON}/I_{OFF} value. The propagation delay of the gate design based on the DTMOS ST logic style is comparable with gate design based on VTCMOS ST logic style. The limitation of gate design based on conventional ST and DTMOS ST logic styles is that it has the highest propagation delay and dynamic power consumption.

2.5 Dynamic ST Logic Styles

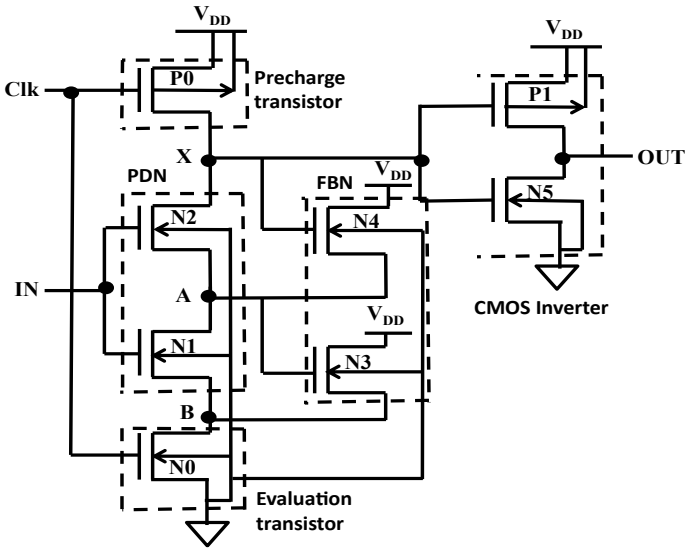
The dynamic ST logic gate is a specialized class of digital gates that incorporates ST functionality within dynamic CMOS logic [74-75]. A dynamic ST gate works on the principle of precharge and evaluate logic depending upon the value of the clock (Clk) signal.

A conventional domino ST logic buffer [76] is shown in Fig. 2.14 (a). It consists of two stages wherein the logic function is implemented in the first stage and the second stage comprises a CMOS inverter. The first stage has a precharge transistor P0 and an evaluation transistor N0. The PDN consists of stacked transistors N1, N2 with their common terminal connected to the FBN N4 transistor. Further, the FBN also has transistor N3 which is connected to the common terminal of N1 and evaluation transistor N0. For a low value of Clk signal, the circuit operates in the precharge phase. In this phase, the dynamic node X is precharged to V_{DD} through P0 while the input IN has no effect as N0 is OFF. Conversely, for a high value of Clk signal, the circuit enters the evaluation phase, the transistors N0 and P0 are ON and OFF, respectively,

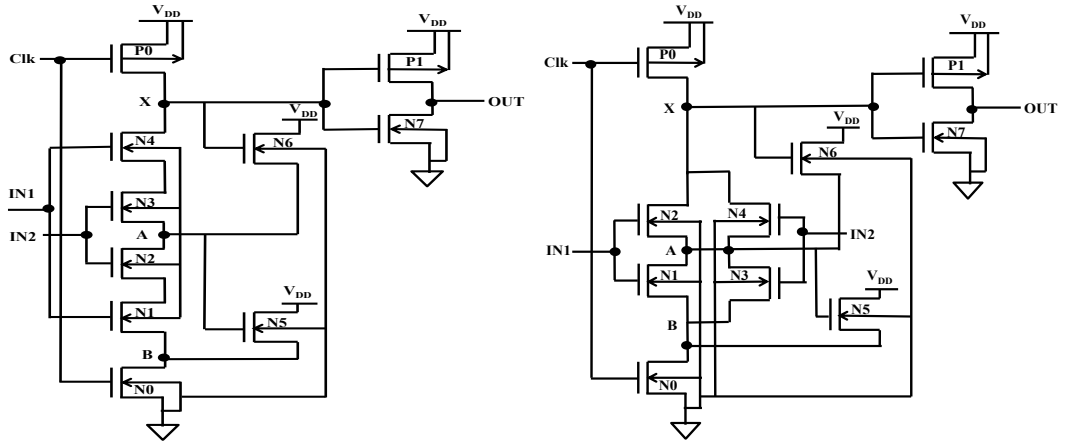
and the gate gets evaluated according to the applied input. The conventional domino ST logic gate offers an improvement in speed at the cost of increased power consumption in comparison to its static counterpart. The advantages of the conventional domino ST logic buffer can be availed by applying the principle to the design of complex functions rather than simple buffer function. The two inputs domino ST logic AND2 and domino ST logic OR2 gates are shown in Fig. 2.14 (b) and (c). The difference between the domino ST logic AND2 gate and the domino ST logic buffer lies in the PDN, while the remaining structure remains the same. The PDN consists of four transistors N1, N2, N3, and N4 are connected in the series. In the precharge phase, the dynamic node X is precharged to V_{DD} through P0 while the inputs IN1 and IN2 have no effect as PDN is OFF. Conversely, for a high value of Clk signal, the circuit enters the evaluation phase, the PDN transistors are ON and P0 is OFF, such that the gate is evaluated according to the input.

The PDN of a two inputs domino ST logic OR2 gate consists of four transistors, in which transistors N1 and N2 are connected in parallel with transistors N3 and N4, respectively. In the precharge phase, the dynamic node X is precharged to V_{DD} through P0 while the inputs IN1 and IN2 have no effect as PDN is OFF. Conversely, for a high value of Clk signal, the circuit enters the evaluation phase, the PDN transistors are ON, and P0 is OFF, such that the gate gets evaluated according to the input.

The other two modified structures domino ST1 logic and domino ST2 logic buffers, are shown in Fig. 2.15 (a) and Fig. 2.15 (b), respectively, wherein the FBN is modified by introducing a keeper transistor. The domino ST1 logic buffer lowers the power consumption, while the domino ST2 logic buffer improves noise immunity in comparison to the conventional ST domino logic buffer.

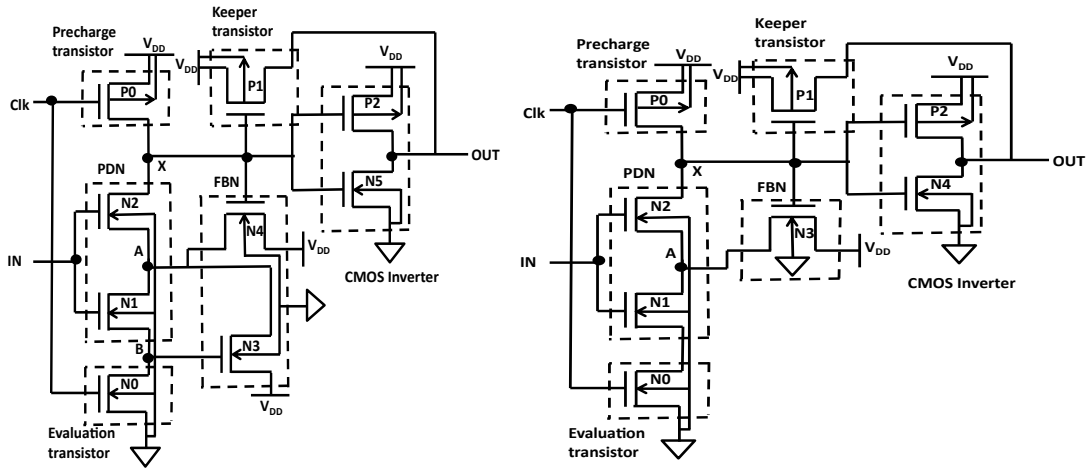


(a)



(b) (c)

Fig. 2.14 Domino ST logic gates (a) Conventional domino ST buffer (b) Domino ST AND2 (c) Domino ST OR2



(a) (b)

Fig. 2.15 Schematic of domino ST logic buffers (a) Domino ST1 [76] (b) Domino ST2 [76]

Despite these developments, challenges related to noise immunity degradation and speed-power trade-offs still persist in existing ST logic structures. Therefore, performance enhancement of the ST logic remains the focus of the work presented in this thesis.

2.6 Conclusion

This chapter presents basic concepts related ST logic gates. The operation of both static and dynamic ST gates and associated performance parameters are discussed. The improved form for both categories of gates is presented. The approach to realizing different logic functions in static as well as dynamic ST logic gates is elaborated. Lastly, the implementations of two design examples, namely the 4:1 multiplexer and full adder are presented, and a performance comparison in support of theoretical propositions is put forward.

Chapter 3

Improved Current Feedback Static Schmitt Trigger Logic Gates

3.1 Introduction

A comprehensive review of prior research reveals that the design of static ST logic gates has primarily evolved along two major approaches based on the type of feedback employed, namely current feedback and voltage feedback techniques. This chapter is devoted to static ST gates with current feedback. The conventional work for static ST logic gates employing current feedback offers ST gates with reduced leakage current, but at the cost of increased delay. Another approach incorporates voltage booster arrangements within the ST logic framework to further improve speed and power consumption, but degrades noise immunity. Alternatively, DTMOS ST gates demonstrate improved noise immunity, however, they suffer from high power consumption and additional fabrication complexity. Thus, there is a need to design conventional ST logic gates having current feedback that can overcome the power delay tradeoff, along with improved noise immunity. Two new static ST logics having current feedback are presented in this chapter to address the mentioned issues.

3.2 Proposed Three-Stage ST Logic Style

The first proposed ST logic style employs three stages and feedback and is thus referred to as three-stage ST (TS ST) logic style. It implements the required functionality in the first stage, which is then followed by two inverter stages. The output of the third stage is fed back to the first stage. The TS ST logic style is based on the recent ST topology presented in [44], which is used to implement relaxation oscillators. The same is extended and investigated for the implementation of the digital ST gates.

3.2.1 Operation and Analysis

A two-input TS ST exclusive-OR (TS ST XOR2) gate is chosen to explain the proposed TS ST logic style. The complete MOS schematic of the proposed TS ST XOR2 gate is shown in Fig. 3.1. The PDN of the first stage connects transistors (N0-N3) for exclusive-OR functionality. Conversely, the PUN connects transistors (P0-P3) to implement the inverse of the given functionality. It is then followed by two CMOS inverters (N4, P4) and (N5, P5) with a feedback connection from the output node (OUT) to the first stage output to introduce hysteresis in the gate.

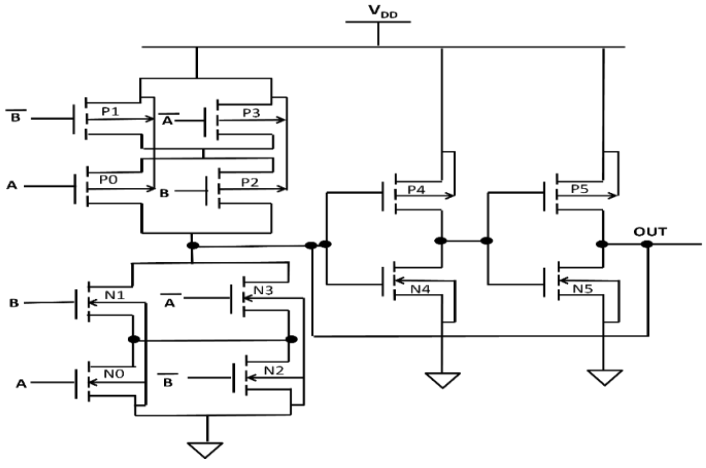


Fig. 3.1 Schematic of the proposed two-input TS ST XOR2 gate

The operation of the proposed TS ST XOR2 gate for different input combinations is explained below:

Case I: When both the inputs A and B are at a low logic level:

In the PDN, transistors N2, N3 are ON, while in the PUN, transistors P1, P3 are OFF, allowing the node OUT to discharge through the current path established from node OUT to ground (GND). The node OUT is thus discharged to GND so that high and low voltage levels are obtained at the output of the second and third inverter respectively.

Case II: When input A is at low logic level and B is at high logic level:

In this case, the transistors N1 and N3 are ON while the transistors N0 and N2 are OFF. This condition in the PDN does not allow a current path to be formed between the node OUT and GND. Further, in the PUN, the series connected transistors P0 and P1 conduct, and the node OUT is charged to a high potential. Thus, the output of the second inverter acquires a low voltage level and subsequently a high level is obtained at the output of the third inverter.

Case III: When input A is at high logic level and B is at low logic level:

For this input combination, a charging path from the power supply to node OUT gets established as transistors P2 and P3 are ON, and N1 and N3 are OFF. This condition charges node OUT to a high voltage level and the output of the second inverter attains a low voltage level accordingly.

Case IV: When input A and B are at the high logic level:

In this case, a current path to discharge the node OUT is formed as the transistors N0 and N1 are ON and no path from the power supply is formed since transistors P0 and P2 are OFF. Thus, the node OUT is discharged and a high voltage level is obtained at the output of the second inverter.

The existence of hysteresis in the proposed TS ST XOR2 gate is elaborated by considering that the inputs A and B are maintained at low and high voltage levels, respectively. In this initial condition, the node OUT is maintained at a high voltage level as explained above in case II. The input B is now allowed to make a high-to-low transition. As the voltage at input B continues to decrease, a high-to-low transition begins to occur at node OUT. However, during the initial phase of the high-to-low transition at the node OUT of the first stage, positive feedback from the inverter in the third stage becomes active. The transistor P5 is ON, which reinforces a high output voltage at the output node, OUT of the first-stage inverter. This causes an increase in the switching threshold voltage V_{HL} during the high-to-low transition, as the discharge of the output node takes additional time. Similarly, the proposed TS ST XOR2 gate leads to a decrease in switching threshold voltage V_{LH} for a low-to-high transition at the node OUT. Therefore, it exhibits stronger hysteresis, which leads to an increase in the noise immunity of the gate.

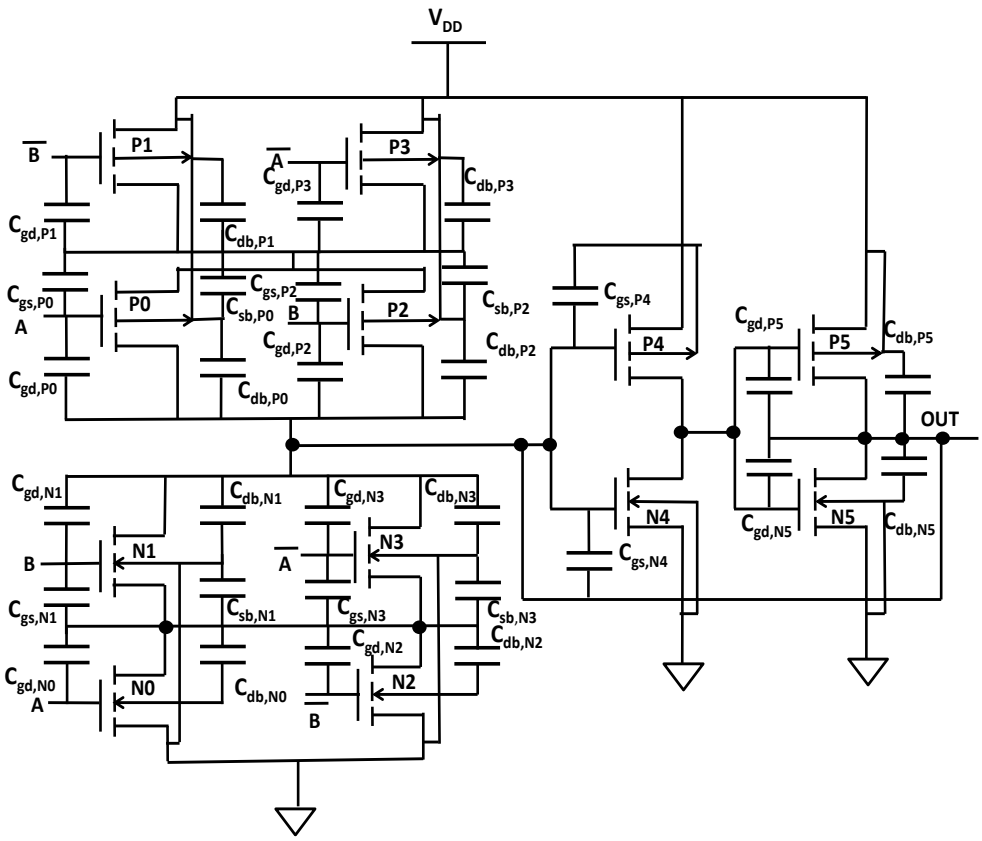


Fig. 3.2 Parasitic capacitances in proposed TS ST XOR2 gate

It is worth mentioning that the proposed TS ST XOR2 gate realizes the given functionality in the first stage. Thus, for a complex logic function of n-input variables, there will be at least 2n transistors in the first stage, which will directly increase the parasitic capacitance at the output node. The increased capacitance has adverse effects on delay and power consumption values. For the proposed TS ST XOR2 gate, the total load capacitances $C_{TS\ ST}$ at the output node OUT are illustrated in Fig. 3.2 and can be expressed as:

$$\begin{aligned} C_{TS\ ST} = {} & C_{db,N0} + C_{gd,N0} + C_{db,P0} + C_{gd,P0} + C_{db,N1} + C_{gd,N1} + C_{db,P1} + \\ & C_{gd,P1} + C_{db,N2} + C_{gd,N2} + C_{db,P2} + C_{gd,P2} + C_{db,N3} + C_{gd,N3} + C_{db,P3} + \\ & C_{gd,P3} + C_{gs,N4} + C_{gs,P4} + C_{db,N5} + C_{gd,N5} + C_{db,P5} + C_{gd,P5} + C_{gs,P0} + \\ & C_{sb,P0} + C_{gs,N1} + C_{sb,N1} + C_{gs,P2} + C_{sb,P2} + C_{gs,N3} + C_{sb,N3} \end{aligned} \quad (3.1)$$

where C_{db} and C_{gd} are the drain to substrate terminal and gate to drain terminal capacitances, respectively, of transistors N0, P0, N1, P1, N2, P2, N3, P3, N5, and P5, C_{gs} is the gate to source capacitance of transistors N1, N3, N4, P0, P2 and P4, and C_{sb} is the source to substrate capacitance of the transistors N1, N3, P0, and P2.

3.2.2 Simulation Results

In this section, the functionality of the proposed TS ST XOR2 gate is verified through simulations. Thereafter, the performance of the proposed XOR2 gate is compared with conventional ST (Fig. 2.3 (c)), DTMOS ST (Fig. 2.5 (d)), and VTCMOS ST (Fig. 2.7 (d)) XOR2 gates. The performance parameters such as transistor count, hysteresis width (V_{HW}),

propagation delay (τ_d), dynamic power (P_{dyn}), and power delay product (PDP) are considered. All the gates are simulated in LTspice using 45 nm PTM CMOS technology parameters with supply voltage and load capacitance of 0.4 V and 2 fF, respectively. The proposed TS ST XOR2 gates are implemented by using the transistors having the mentioned aspect ratio as listed in Table 3.1

Table 3.1: Aspect ratio of transistors in XOR2 gates designed in different ST styles

Transistors / ST styles	Aspect ratio of NMOS transistors	Aspect ratio of PMOS transistors
Conventional ST [26]	N0-N7=4, N8=1	P0-P7=16, P8=2
DTMOS ST [37]	N0-N7=4, N8=1	P0-P7=16, P8=2
VTCMOS ST [38]	N0-N3=2, N4=2	P0-P3=8, P4=8
Proposed TS ST	N0-N3=2, N4=2, N5=1	P0-P3=8, P4=8, P5=2

I. Functional Verification

The proposed TS ST XOR2 gate is implemented, and the simulated waveform is shown in Fig. 3.3. It can be observed that when both the inputs are at a high logic level (V_{DD} = 0.4 V), a low logic level (= 0 V) is obtained as the output voltage at the OUT node. Similarly, a low logic voltage level is obtained at node OUT when both the inputs are at a low logic level. Further, it can also be verified that when the two inputs in the proposed TS ST XOR2 gate differ, then a high output voltage is observed at the OUT node. Thus, the proposed TS ST XOR2 gate conforms to the functionality for all input combinations.

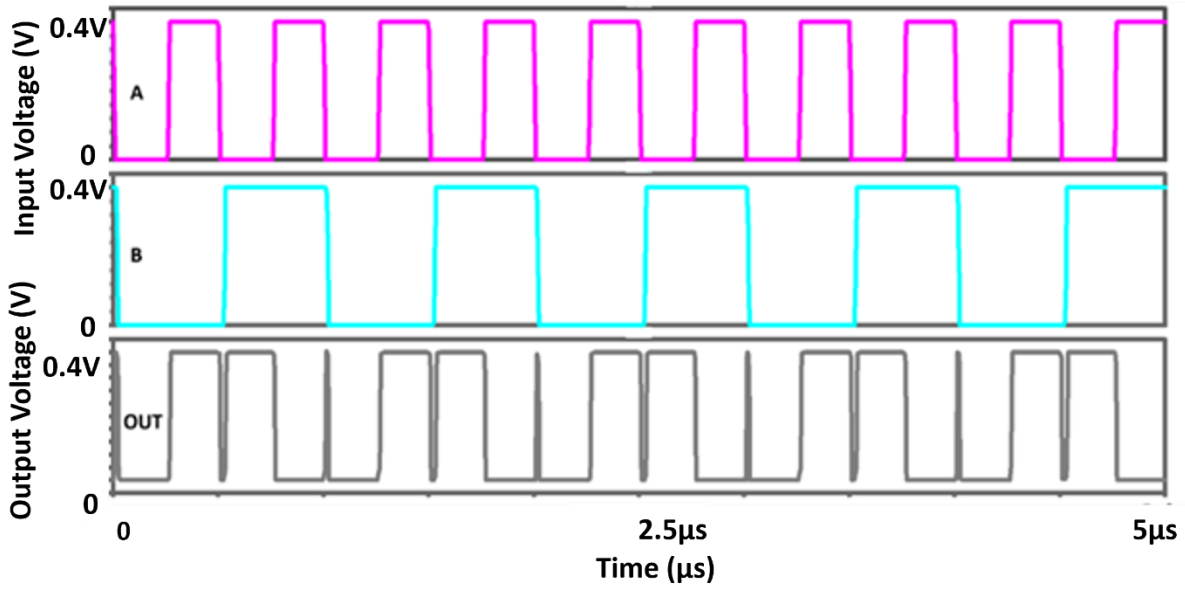


Fig. 3.3 Transient response of the proposed TS ST XOR2 gate

II. Performance Comparison

The values of various performance parameters obtained from the simulation results for the proposed and existing ST logic style based XOR2 gates are listed in Table 3.2. The following observations can be drawn from the results:

- The noise immunity of an ST gate is generally measured in terms of hysteresis width. The hysteresis width of the proposed TS ST XOR2 gate is increased by 855 %, 889 %, and 145 % over conventional ST, DTMOS ST, and VTCMOS ST gates, respectively. The increase in hysteresis width is observed due to the positive feedback from the third stage that increases/decreases the switching threshold voltages.
- The results for delay indicate that the proposed TS ST XOR2 gate is the slowest among all and exhibits an increase in delay values by 20 %, 125 %, and 65 % in comparison to conventional, DTMOS, and VTCMOS ST XOR2 gates, respectively. The cascade of three stages in the proposed TS ST XOR2 gate has led to increase in propagation delay.
- The proposed TS ST XOR2 gate consumes the lowest dynamic power and offers a power saving of 14 %, 82 %, and 43 % in comparison to conventional ST, DTMOS ST, and VTCMOS ST gates, respectively.
- The PDP of the proposed TS ST XOR2 gate is reduced by 60 % and 6 % in comparison to DTMOS ST and VTCMOS ST XOR2 gates, respectively, due to the combined effect of low delay and power consumption values. However, the proposed TS ST XOR2 gate shows a marginal increase in PDP by 3 % with respect to the conventional ST XOR2 gate.

The effect of scaling from 45 nm to 32 nm is studied for the proposed and existing XOR2 gate topologies. The obtained results at 32 nm technology node are summarized in Table 3.2. It is found that the propagation delay of conventional ST and TS ST XOR2 gates is reduced by 1.6 % and 15.4 %, respectively, due to reduced channel length, which shortens carrier transit time and lowers parasitic capacitances. However, the propagation delay at the lower technology node is increased by 15 % and 5.6 % for DTMOS and VTCMOS ST XOR2 gates due to the dynamic body biasing mechanism that causes a delay in threshold voltage adjustment, which initially restricts current flow during switching. Thus, standard logic gates with fixed body bias benefit more directly from scaling, since their threshold voltages do not dynamically limit the switching behaviour. The dynamic power of conventional ST, DTMOS ST, and VTCMOS ST XOR2 gates at the 32 nm technology node reduces by 33 %, 57 %, and 79 %, respectively, while it is comparable for the TS ST XOR2 gate due to the involvement of three stages. Thus, the PDP reduction is observed for all the gates by 34.4 %, 51 %, 78.2 %, and 13.3 % for conventional ST, DTMOS ST, VTCMOS ST, and TS ST XOR2 gates, respectively, at the 32 nm technology node. The V_{HW} of conventional ST, DTMOS ST, VTCMOS ST, and TS ST gates is reduced by 4.8 %, 63.6 %, 26.3 %, and 20.5 %, respectively. The reduction in hysteresis width leads to reduction in noise immunity because the ST gates become less regenerative and more susceptible to noise due to increased short-channel effects.

Table 3.2: Performance comparison of ST XOR2 gates

ST styles / Performance comparison	Conventional ST XOR2 [26]	DTMOS ST XOR2 [37]	VTCMOS ST XOR2 [38]	Proposed TS ST XOR2
Results at 45 nm CMOS Technology node				
Transistor count	18	18	10	12
τ_d (ns)	5.32	2.85	3.88	6.42
P_{dyn} (nW)	2.85	14	4.33	2.45
PDP ($x10^{-18}J$)	15.16	39.9	16.8	15.72
V_{HW} (mV)	29	28	112.74	276.97
Area $(um)^2$	8.69	9.70	8.58	9.55
Results at 32 nm CMOS Technology node				
τ_d (ns)	5.23	3.3	4.1	5.43
P_{dyn} (nW)	1.90	5.92	0.89	2.51
PDP ($x10^{-18}J$)	9.93	19.53	3.66	13.62
V_{HW} (mV)	27.6	10.19	83	220

3.3 Proposed Transmission Gate Three-Stage ST Logic Style

The proposed TS ST logic presented in Section 3.2 achieves significant improvement in noise immunity at the cost of the propagation delay. To address this issue, a new logic style that integrates transmission gate (TG) in TS ST logic is proposed in this section. The new style is referred to as transmission gate three-stage ST (TG-TS ST) logic style.

3.3.1 Operation and Analysis

The proposed TG-TS ST logic gate employs transmission gates (TG) to realize a logic function and feeds the intermediate output to the TS ST gate. The schematic of the proposed two-input TG-TS ST exclusive-OR (TG-TS ST XOR2) gate is shown in Fig. 3.4. The corresponding TG network comprises two TGs (TG1:N0, P0) and (TG2: N1, P1), and its output X further drives the TS ST inverter.

The operation of the proposed TG-TS ST XOR2 gate for different input combinations is explained.

Case I: When both the inputs A and B are at low logic level:

For this case, TG1 is in high impedance state while TG2 conducts such that complement of the logic level at B which is high is transferred to intermediate node X. The high voltage of node X drives the first inverter followed by second inverter and a low logic level is produced at the third inverter output OUT.

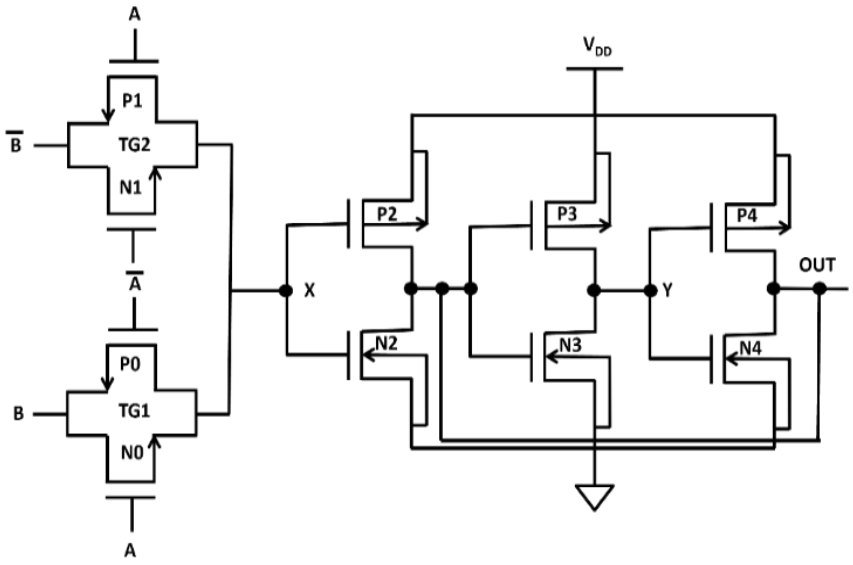


Fig. 3.4 Schematic of the proposed two-input TG-TS ST XOR2 gate

Case II: When input A is at the low logic level and B is at the high logic level:

In this case, TG1 is in a high impedance state while TG2 transfers a low voltage level at node X. The low voltage of node X turns ON transistor P2 in the first stage inverter, which produces a high logic level at the OUT node. This further turns ON transistor N3 and provides a low voltage at node Y.

Case III: When input A is at the high logic level and B is at the low logic level:

In this case, TG1 conducts while TG2 is in a high impedance state. Under this condition, a low logic level is produced as the output of the TG network at node X. This input voltage when fed to the inverter, turns ON transistor P2 and produces a high voltage, which further turns ON transistor N3. A low logic level is obtained at node Y, which turns the transistor P4 ON and provides a high logic level at the output node OUT.

Case IV: When inputs A and B are at the high logic level:

For this case, TG1 conducts, and TG2 does not conduct. This condition makes a high logic level of input B available at node X, which provides low logic at the OUT output node.

The parasitic capacitances are computed to analyse the effect on delay performance. The total capacitances at node OUT ($C_{TG\text{-}TS\ ST}$) by considering the associated parasitic capacitances of different transistors in the proposed TG-TS ST gate, are drawn in Fig. 3.5. The same can be expressed as:

$$C_{TG-TS\ ST} = C_{bd,N2} + C_{gd,N2} + C_{bd,P2} + C_{gd,P2} + C_{gs,N3} + C_{gs,P3} + C_{bd,N4} + C_{gd,N4} + C_{bd,P4} + C_{gd,P4} \quad (3.2)$$

where C_{bd} and C_{gd} are the body to drain terminal and gate to drain terminal capacitances of the transistors N2, P2, N4, and P4, respectively, and C_{gs} is the gate to source terminal capacitance across transistor N3.

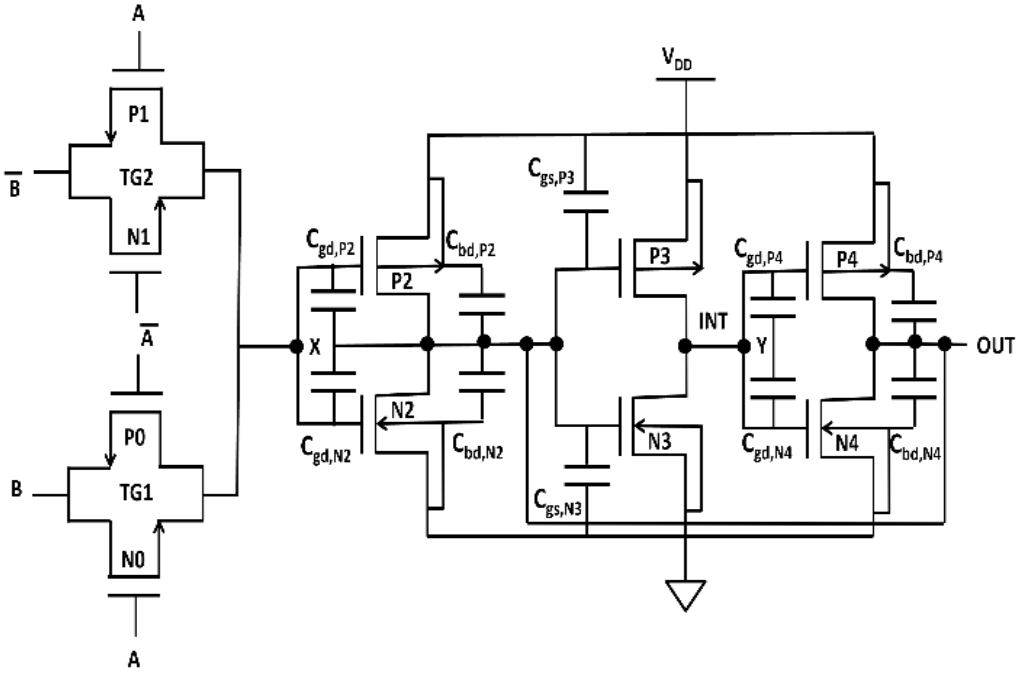


Fig. 3.5 Parasitic capacitances at node OUT in the proposed TG-TS ST XOR 2 gate

3.3.2 Simulation Results

In this section, the functionality of the proposed TG-TS ST XOR2 gate is verified through simulations. Thereafter, the performance of the proposed XOR2 gate is compared with conventional ST, DTMOS ST, and VTCMOS ST XOR2 gate counterparts. The performance parameters such as transistor count, hysteresis width (V_{HW}), propagation delay (τ_d), dynamic power (P_{dyn}), and power delay product (PDP) are considered. All the gates are simulated in LTspice using 45 nm PTM CMOS technology parameters with a supply voltage and load capacitance of 0.4 V and 2 fF, respectively. The proposed TG-TS ST XOR2 gates are implemented by using transistors having the mentioned aspect ratio as listed in Table 3.3.

Table 3.3: Aspect ratio of transistors in XOR2 gates designed in different ST styles

Transistors / **ST styles**	**Aspect ratio of NMOS transistors**	**Aspect ratio of PMOS transistors**
Conventional ST [26]	N0-N7=4, N8=1	P0-P7=16, P8=2
DTMOS ST [37]	N0-N7=4, N8=1	P0-P7=16, P8=2
VTCMOS ST [38]	N0-N3=2, N4=2	P0-P3=8, P4=8
Proposed TG-TS ST	N0-N3=2, N4=1	P0-P3=8, P4=2

I. Functional Verification

The observed simulation waveform for the proposed TG-TS ST XOR2 gate is shown in Fig. 3.6. It can be observed that when both the inputs are at a high logic level (V_{DD} = 0.4 V), a low logic level (= 0 V) is obtained as the output voltage at the OUT node. Similarly, a low logic voltage level is obtained at node OUT when both the inputs are at a low logic level. Further, it can also be verified that when the two inputs in the proposed ST XOR2 gates differ, then a high output voltage is observed at the OUT node. Thus, the proposed TG-TS ST XOR2 gate conforms to the functionality for all input combinations.

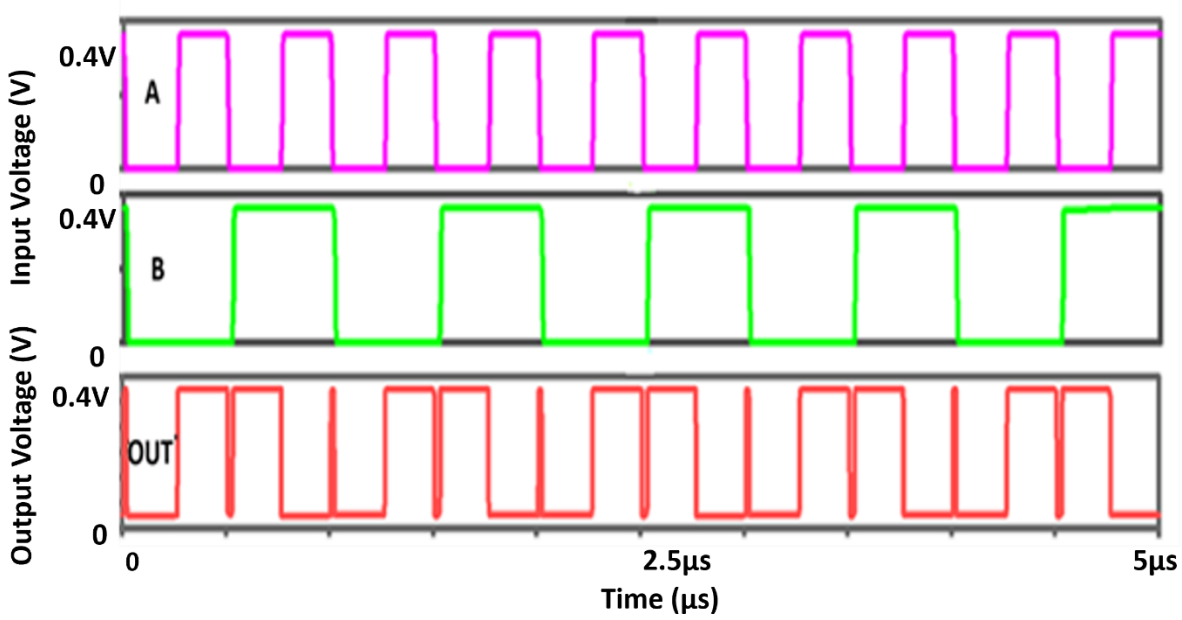


Fig. 3.6 Transient response of the proposed TG-TS ST XOR2 gate

II. Performance Comparison

The values of different performance parameters are noted from the simulation results and are listed in Table 3.4. The following observations can be drawn from the results:

- The proposed TG-TS ST XOR2 gate achieves a significant reduction of 40 % and 18 % in delay values in comparison to conventional and VTCMOS XOR2 gates, respectively. The delay advantage can be attributed to the reduced capacitance at the output node, OUT of the proposed TG-TS ST XOR2 gate. It demonstrates the superior switching performance of the TG-based design due to the reduced resistance and improved signal driving capability introduced by the transmission gates. Thus, the proposed TG-TS ST XOR2 proves to be more efficient in terms of propagation delay. However, the proposed TG-TS ST XOR2 gate has 12 % increased delay value in comparison to the existing DTMOS ST XOR2 gate. The dynamic threshold voltage technique in the DTMOS ST XOR2 gate results in a high dynamic power, which reduces the delay. However, the fabrication of DTMOS adds to the fabrication cost as well as increases power. Thus, the proposed TG-TS ST XOR2 gate can effectively replace the DTMOS ST gate without an increase in cost and power.

- The proposed TG-TS ST XOR2 gate consumes the lowest dynamic power and offers a power saving of 32 %, 86 %, and 55 % in comparison to conventional ST, DTMOS ST, and VTCMOS ST XOR2 gates, respectively. The proposed TG-TS ST XOR2 gate integrates transmission gates with the three-inverter ST logic, which offers the advantage of decreasing capacitance at the output node.
- The PDP of the proposed TG-TS ST XOR2 gate gets reduced by 59 %, 84 %, and 63 %, in comparison to conventional ST, DTMOS ST, and VTCMOS ST XOR2 gates, respectively, due to the combined benefit of low propagation delay and power consumption values.
- The hysteresis width of the proposed TG-TS ST XOR2 gate is increased by 389 %, 406 %, and 26 % over conventional ST, DTMOS ST, and VTCMOS ST XOR2 gates, respectively.

The effect of scaling from 45 nm to 32 nm technology node is as follows: The simulation results for the proposed and existing ST XOR2 gates at 32 nm technology node are listed in Table 3.4. It is observed that the propagation delay of all the gates decreases due to reduction in load capacitances, except for a few, as a result of technology scaling. The propagation delay of conventional ST and TG-TS ST XOR2 gates reduces by 1.6 % and 3.7 %, respectively, due to reduced channel length, which shortens carrier transit time and lowers parasitic capacitances. The dynamic power of conventional ST, DTMOS ST, VTCMOS ST, and TG-TS ST XOR2 gates at the 32 nm technology node reduces by 33 %, 57 %, 79 % and 67 %, respectively. Thus, the PDP reduction of 34.4 %, 51 %, 78.2 %, and 68.6 % is observed for conventional ST, DTMOS ST, VTCMOS ST, and TG-TS ST XOR2 gates, respectively, at the 32 nm technology node. The hysteresis width of conventional ST, DTMOS ST, VTCMOS ST, and TG-TS ST XOR2 gates reduce by 4.8 %, 63.6 %, 26.3 %, and 14.7 %, respectively. The reduction in hysteresis width leads to reduction in noise immunity because the ST gates become less regenerative and more susceptible to noise due to increased short-channel effects.

Table 3.4 Performance comparison of ST XOR2 gates

ST styles / **Performance comparison**	**Conventional ST XOR2 [26]**	**DTMOS ST XOR2 [37]**	**VTCMOS ST XOR2 [38]**	**Proposed TG-TS ST XOR2**
Results at 45 nm CMOS Technology node				
Transistor count	18	18	10	10
τ_d (ns)	5.32	2.85	3.88	3.19
P_{dyn} (nW)	2.85	14	4.33	1.95
PDP (x10^{-18}J)	15.16	39.9	16.8	6.22
V_{HW} (mV)	29	28	112.74	141.91
Results at 32 nm CMOS Technology node				
τ_d (ns)	5.23	3.3	4.1	3.07
P_{dyn} (nW)	1.90	5.92	0.89	0.64
PDP (x10^{-18}J)	9.93	19.53	3.66	1.95
V_{HW} (mV)	27.6	10.19	83	121

3.4 Overall Performance Comparison

In this section, the performances of the proposed TS ST and TG-TS ST XOR2 gates are compared with conventional ST, DTMOS ST, and VTCMOS ST XOR2 gates. The performance parameters such as transistor count, hysteresis width voltage (V_{HW}), propagation delay (τ_d), dynamic power (P_{dyn}), and power delay product (PDP) are considered. All the gates are simulated in LTspice using 45 nm PTM CMOS technology parameters with supply voltage and load capacitance of 0.4 V and 2 fF, respectively. The effect of process variation at different corners on the performance is also studied.

The values of different performance parameters are noted from the simulation results and are listed in Table 3.5. The following observations can be drawn from the results:

- The results for propagation delay indicate that the proposed TG-TS ST XOR2 gate shows reduced delay values by 40 %, 18 %, and 50 % in comparison to conventional, VTCMOS, and proposed TS-ST XOR2 gates, respectively. The delay advantage can be attributed to the reduced capacitance at the output node of the proposed TG-TS ST XOR2 gate. The simulation waveform shown in Fig. 3.7 presents a delay comparison between the TS ST and the TG-TS ST XOR2 gates. It is observed that the duration of low-to-high and high-to-low transitions at the output is significantly lower in the TG-TS ST XOR2 gate as compared to the TS ST XOR2 gate. This reduction in transition time reduces the propagation delay of the proposed TG-TS ST XOR2 gate. It demonstrates the superior switching performance of the TG-based design, due to the reduced resistance and improved signal driving capability introduced by the transmission gates. Therefore, the proposed TG-TS ST XOR2 gate proves to be more efficient in terms of reduced propagation delay. However, the proposed TG-TS ST XOR2 gate has a 12 % increased delay value in comparison to the existing DTMOS ST XOR2 gate. The dynamic threshold voltage technique in the DTMOS ST XOR2 gate results in a high switching current, which reduces the delay. However, the fabrication of DTMOS adds to the fabrication cost as well as increases power. Thus, the proposed TG-TS ST XOR2 gate can replace the DTMOS ST XOR2 gate without an increase in cost and power.

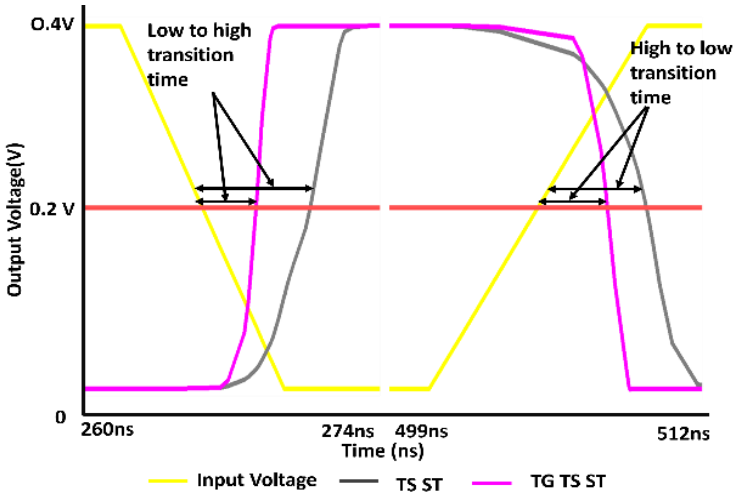


Fig. 3.7 Transition time comparison of the proposed TS ST and TG-TS ST XOR2 gates

- The proposed TG-TS ST XOR2 gate consumes the lowest dynamic power and offers a power saving of 32 %, 86 %, 55 %, and 20 % in comparison to conventional ST, DTMOS ST, VTCMOS ST, and proposed TS ST XOR2 gates, respectively. The proposed TG-TS ST XOR2 gate integrates transmission gates with the three-inverter ST logic, which infers the advantage. The proposed circuit efficiently reduces dynamic power consumption by decreasing capacitance at the output node.
- The PDP of the proposed TG-TS ST XOR2 gate is reduced by 59 %, 84 %, 63 %, and 60 % in comparison to conventional ST, DTMOS ST, VTCMOS ST, and proposed TS ST XOR2 gates, respectively, due to the combined benefit of lower delay and power consumption values.
- The hysteresis width of the proposed TS ST XOR2 gate is increased by 855 %, 889 %, 145 %, and 95% over conventional ST, DTMOS ST, VTCMOS ST, and TG-TS ST XOR2 gates, respectively. The hysteresis width comparison of the proposed TS ST XOR2 and TG-TS ST XOR2 gates is also shown in Fig. 3.8. The effect of a change in the width of feedback transistors (P4, N4) of TG-TS ST XOR2 gate on hysteresis width is shown in Fig. 3.9. It is observed that the value of the switching threshold voltage V_{LH} decreases with an increase in the width of the feedback transistor P4, and the value of the switching threshold voltage V_{HL} increases with an increase in the width of the feedback transistor N4. A similar trend for the switching threshold is observed for the TS ST XOR2 gate and is not shown for the sake of brevity.

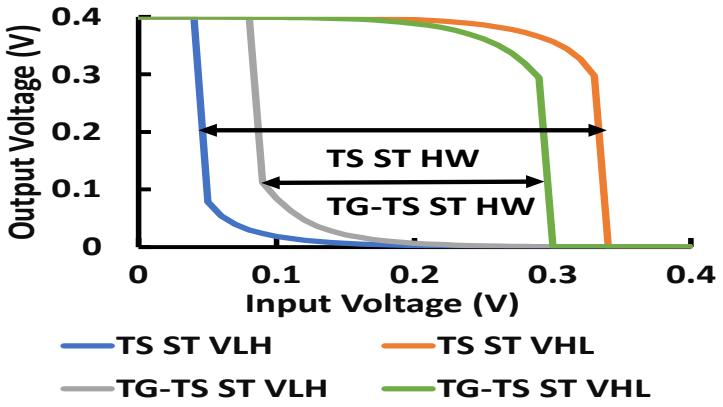
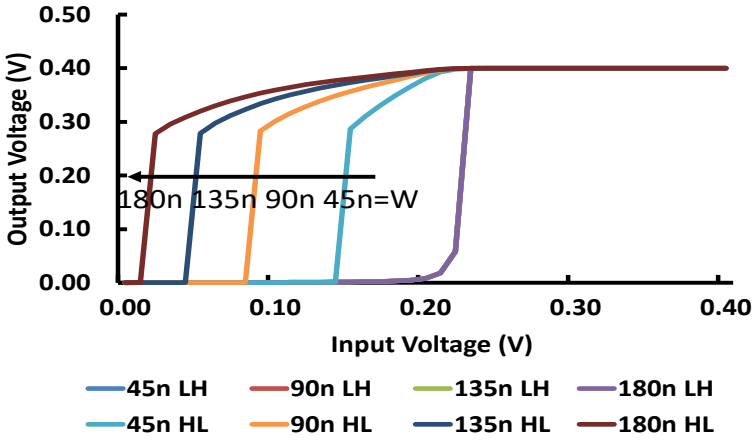
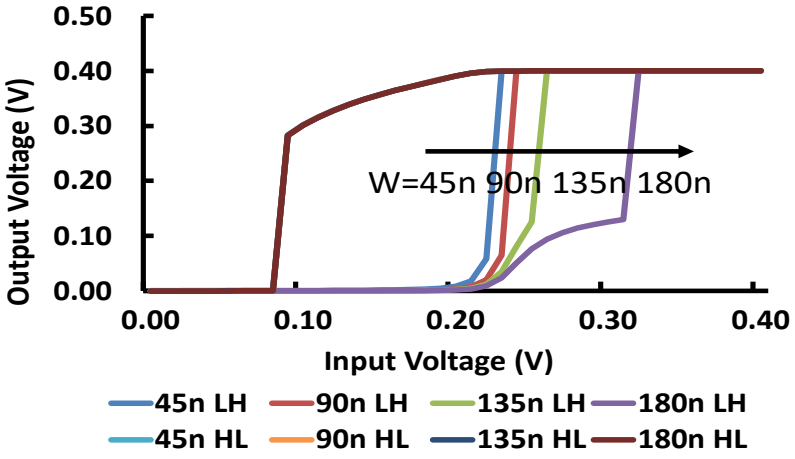


Fig. 3.8 Hysteresis width comparison of the proposed TS ST and TG-TS ST XOR2 gates



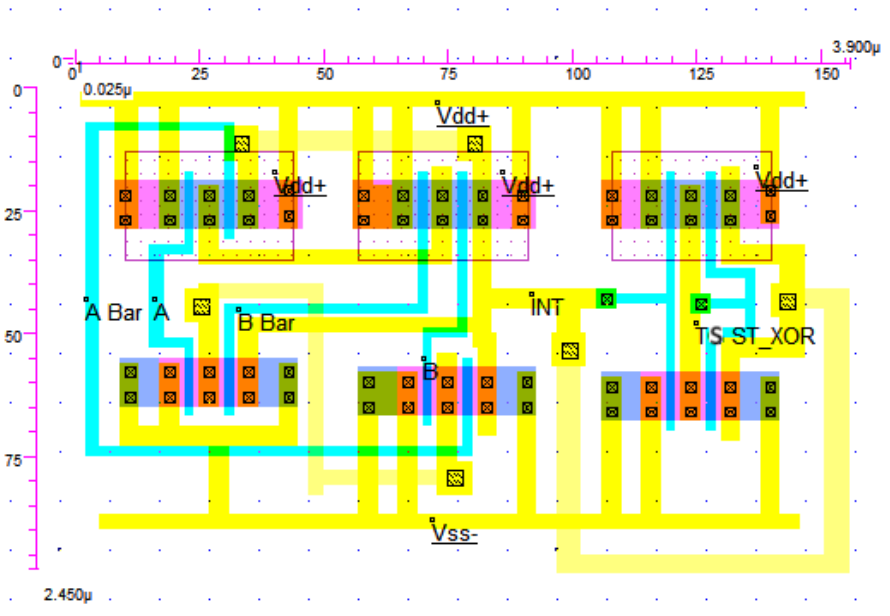
(a)



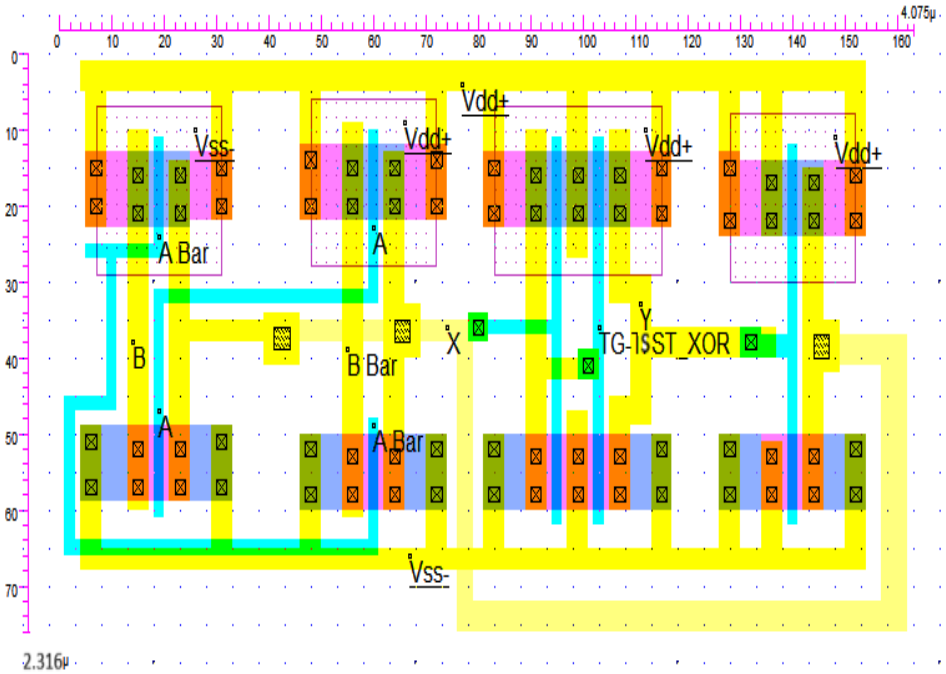
(b)

Fig. 3.9 Effect of change in width of feedback transistor in TG-TS ST XOR2 gate (a) Low to high (V_{LH}) (b) High to low transition (V_{HL})

The layout of the proposed TS ST XOR2 and TG-TS ST XOR2 gates is shown in Fig. 3.10. It is observed that the VTCMOS ST XOR2 gate consumes the lowest area among all, as listed in Table 3.5. The proposed TG-TS ST XOR2 gate occupies less area than the DTMOS ST XOR2 gate and is comparable in area to the TS ST XOR2 gate. The post-layout simulation results show an increase in propagation delay, dynamic power, and PDP compared with the schematic-level simulation results due to the extracted parasitic capacitances and resistances associated with the physical layout, as shown in Table 3.5.



(a)



(b)

Fig. 3.10 Layout design of proposed XOR2 gates using (a) TS ST (b) TG-TS ST

The simulation results for the proposed and existing ST XOR2 gates at the 32 nm technology node are listed in Table 3.5. The effect of scaling from 45 nm to 32 nm is as follows: It is observed that the propagation delay of all the gates decreases due to a reduction in load capacitances, except for the DTMOS ST and VTCMOS ST XOR2 gates. The propagation delay of conventional ST, TS ST, and TG-TS ST XOR2 gates reduces by 1.6 %, 15.4 %, and 3.7 %, respectively, due to reduced channel length, which shortens carrier transit time and lowers parasitic capacitances. However, the propagation delay increases for the DTMOS and VTCMOS ST XOR2 gates by 15 % and 5.6 % due to the dynamic substrate biasing mechanism, which causes propagation delay in threshold voltage adjustment, which initially restricts current flow during switching. Thus, standard logic gates with fixed substrate bias benefit more directly from scaling, since their threshold voltage does not dynamically limit the switching behaviour. The dynamic power of conventional ST, DTMOS ST, VTCMOS ST, and TG-TS ST XOR2 gates at the 32 nm technology node is reduced by 33%, 57%, 79%, and 67%, respectively, while it is comparable for the TS ST XOR2 gate. Thus, the PDP reduction is observed for all the gates by 34.4 %, 51 %, 78.2 %, 13.3 %, and 68.6 % for conventional ST, DTMOS ST, VTCMOS ST, TS ST, and TG-TS ST XOR2 gates, respectively, at the 32 nm technology node. The hysteresis width of conventional ST, DTMOS ST, VTCMOS ST, TS ST, and TG-TS ST XOR2 gates is reduced by 4.8 %, 63.6 %, 26.3 %, 20.5 %, and 14.7 %, respectively. The reduction in hysteresis width leads to a reduction in noise immunity because the ST gates become less regenerative and more susceptible to noise due to increased short-channel effects.

Table 3.5: Performance comparison of ST XOR2 gates at different technology nodes

ST styles / Performance comparison	Conventional ST XOR2 [26]	DTMOS ST XOR2 [37]	VTCMOS ST XOR2 [38]	Proposed TS ST XOR2	Proposed TG-TS ST XOR2
Results at 45 nm CMOS Technology node					
Transistor count	18	18	10	12	10
τ_d (ns)	5.32	2.85	3.88	6.42	3.19
P_{dyn} (nW)	2.85	14	4.33	2.45	1.95
PDP ($x10^{-18}J$)	15.16	39.9	16.8	15.72	6.22
V_{HW} (mV)	29	28	112.74	276.97	141.91
Area $(um)^2$	8.69	9.70	8.58	9.55	9.43
	Post Layout				
τ_d (ns)	5.90	3.10	4.15	6.80	3.54
P_{dyn} (nW)	3.12	15.2	4.95	2.75	2.2
Results at 32 nm CMOS Technology node					
τ_d (ns)	5.23	3.3	4.1	5.43	3.07
P_{dyn} (nW)	1.90	5.92	.89	2.51	.64
PDP ($x10^{-18}J$)	9.93	19.53	3.66	13.62	1.95
V_{HW} (mV)	27.6	10.19	83	220	121

The effect of process corner variation on the proposed ST XOR2 gates is analysed and compared with existing ST XOR2 gates. The results for various performance parameters across different design corners (TT, FF, SS, SF, and FS; T: Typical, F: Fast, S: Slow) are summarized in Table 3.6. The proposed TG-TS ST XOR2 gate reflects the lowest deviation in hysteresis width at the FF and SS corners. It also exhibits the lowest variation in delay at the FF, SF, and FS corners, except for the DTMOS ST XOR2 gate at the SS corner. In contrast, the VTCMOS ST XOR2 gate shows the highest deviation in propagation delay at the FF, SF, and FS corners. Furthermore, the proposed TG-TS ST XOR2 gate shows the lowest dynamic power deviation at the SS and SF corners, while the conventional ST XOR2 gate exhibits the highest deviation at the FF, SS, and SF corners.

Effect of Supply Voltage Variation

The effect of variation in supply voltages on the propagation delay of existing and proposed TS ST and TG-TS ST XOR2 gates is illustrated in Fig. 3.11(a). Along with the original graph, a modified graph is also included for clear visibility. As the supply voltage is varied from low to high, it is observed that the propagation delay decreases. The proposed TG-TS ST XOR2 gate shows the lowest propagation delay with respect to conventional ST, VTCMOS ST, and TS ST XOR2 gates. The conventional ST and DTMOS ST XOR2 gates show reduction in propagation delay with respect to an increase in supply voltage, except for VTCMOS ST, TS ST and TG-TS ST XOR2 gates. The VTCMOS ST, TS ST, and TG-TS ST XOR2 gates show reduction in propagation delay with increase in supply voltage from 0.2 V to 0.6 V due to drive current increases exponentially with V_{dd} in the subthreshold and near threshold region, and

increase in delay with an increase in supply voltage from 0.6 V to 0.8 V due to current growth becoming quadratic/linear.

The effect of supply voltage variations on dynamic power dissipation is shown in Fig. 3.11(b). Along with the original graph, a modified graph is also combined for clear visibility. The ST gates show an increase in dynamic power consumption due to an increase in supply voltage. The proposed TG-TS ST XOR2 gate exhibits the lowest dynamic power dissipation among all ST gates.

The effect of supply voltage variations on noise immunity is depicted in Fig. 3.11(c). It also shows an increase in noise immunity with respect to an increase in supply voltage due to stronger feedback. It is observed that the DTMOS ST, VTCMOS ST, TS ST, and TG-TS ST XOR2 gates exhibit a slight decrease in noise immunity at higher supply voltages (0.6 V to 0.8 V) due to substrate bias limits.

Table 3.6: Performance comparison of ST XOR2 gates at different design corners

ST styles / **Performance comparison**	**Conventional ST XOR2 [26]**	**DTMOS ST XOR2 [37]**	**VTCMOS ST XOR2 [38]**	**Proposed TS ST XOR2**	**Proposed TG-TS ST XOR2**
TT					
Transistor count	18	18	10	12	10
τ_d (ns)	5.32	2.85	3.88	6.42	3.19
P_{dyn} (nW)	2.85	14	4.33	2.45	1.95
PDP (x10^{-18}J)	15.16	39.9	16.8	15.72	6.22
V_{HW} (mV)	29	28	112.74	276.97	141.91
Area (um)^2	8.69	9.70	8.58	9.55	9.43
FF					
τ_d (ns)	3.88	2.23	2.75	4.84	2.65
P_{dyn} (nW)	12.4	16	13	3.86	2.55
PDP (x10^{-18}J)	48.11	32.80	10.06	18.68	6.75
V_{HW} (mV)	29	27.5	92.9	256.98	141.84
SS					
τ_d (ns)	6.7	3.3	5.57	10.61	4.8
P_{dyn} (nW)	7.9	9.48	4.3	0.995	1.9
PDP (x10^{-18}J)	52.90	31.28	23.95	10.55	9.12
V_{HW} (mV)	37.3	30	120	287.2	145
SF					
τ_d (ns)	4.80	3.09	3.20	7.50	2.97
P_{dyn} (nW)	4.92	8.5	2.9	3.10	1.97
PDP (x10^{-18}J)	23.61	26.26	9.28	23.25	5.85
V_{HW} (mV)	32	28.5	105	240	153
FS					

τ_d (ns)	4.75	2.90	3.15	7.30	2.95
P_{dyn} (nW)	5.60	9.2	4.65	3.35	4.0
PDP ($x10^{-18}$J)	26.6	26.6	14.64	24.45	11.8
V_{HW} (mV)	35	29	107	260	155

T: Typical, F: Fast, S: Slow

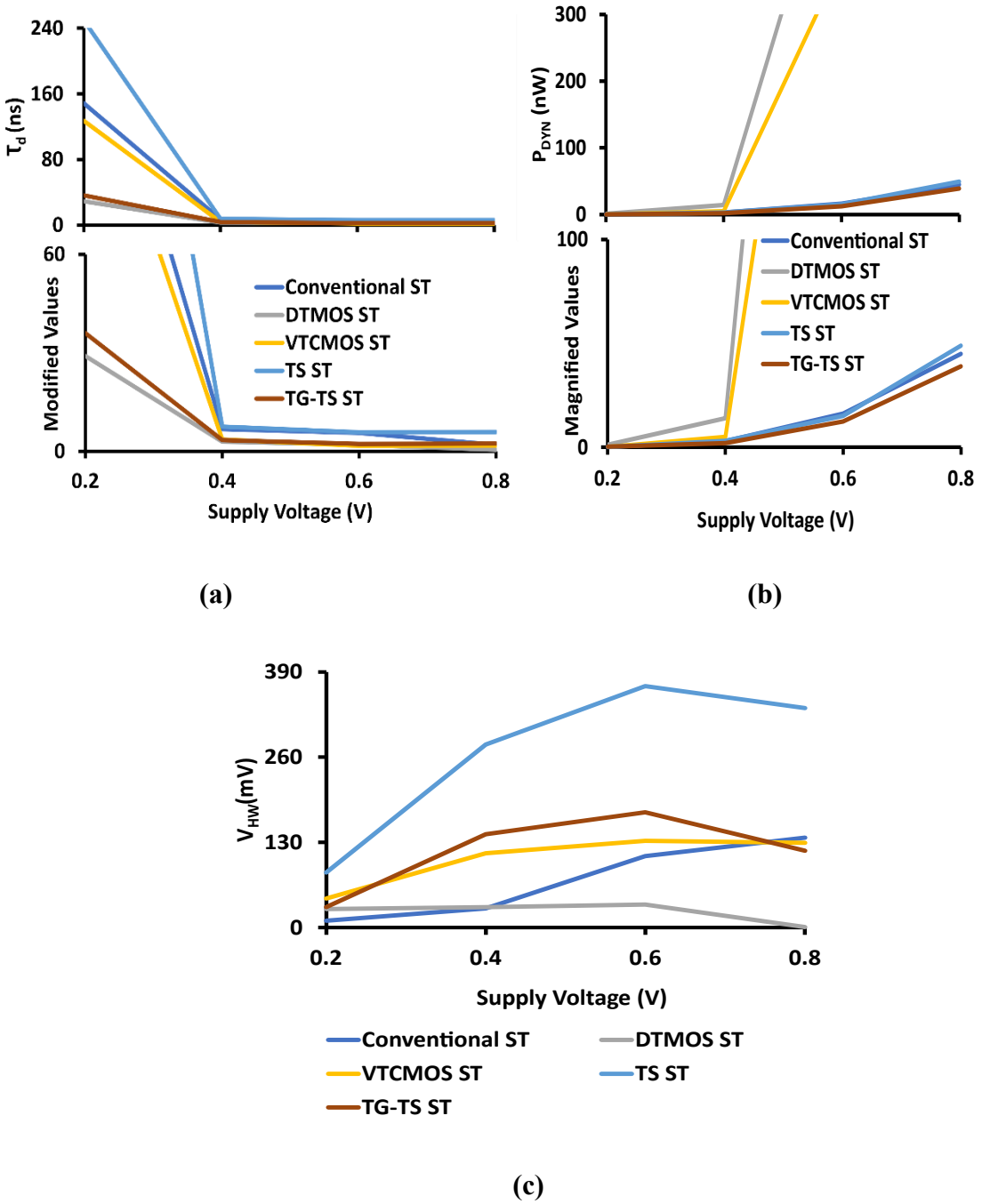


Fig. 3.11. Effect of supply voltage variation on performance parameters of ST XOR2 gates (a) τ_d (b) P_{dyn} (c) V_{HW}

3.5 Design Examples using Proposed ST Logic Styles

A 4:1 multiplexer (MUX) is taken as a design example. The block diagram of the 4:1 MUX employs two 2:1 ST MUXs in the first stage, which are followed by one 2:1 ST MUX in the second stage, as shown in Fig. 3.12. The design of 4:1 TS ST and TG-TS ST MUXs is shown in Fig. 3.13. The same design is extended for the existing ST logic style. All the MUXs are simulated, and the results of different performance parameters are listed in Table 3.7. It is observed that the proposed 4:1 TG-TS ST MUX shows a reduction in propagation delay of 49 %, 9 %, 19 %, and 71 % with respect to 4:1 conventional ST, DTMOS ST, VTCMOS ST, and TS ST MUXs, respectively. Furthermore, compared to the 4:1 conventional ST, DTMOS ST, and TS ST MUXs, the proposed 4:1 TG-TS ST MUX gate decreases dynamic power consumption by 92 %, 55 %, and 84 %, respectively. Hence, the proposed 4:1 TG-TS ST MUX has the lowest dynamic power consumption among all the MUXs except the VTCMOS ST MUX. Additionally, the proposed 4:1 TS ST and TG-TS ST MUXs offer the highest and second-highest immunity among all the MUXs. The proposed 4:1 TG-TS ST MUX achieves an improvement of 599 %, 956 %, and 120 % in comparison to 4:1 conventional ST, DTMOS ST, and VTCMOS ST MUXs, respectively. The process corners analysis also confirms the superiority of the proposed ST MUXs over conventional ST MUXs.

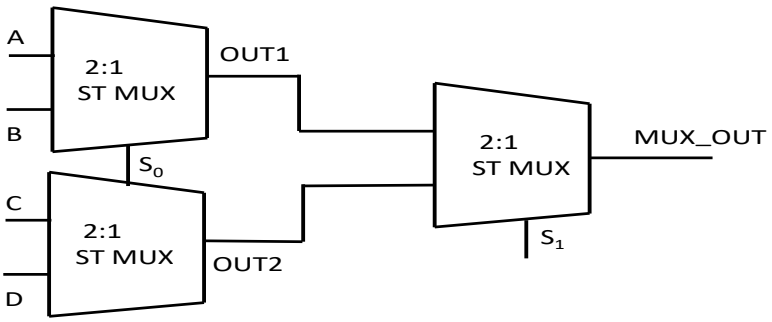
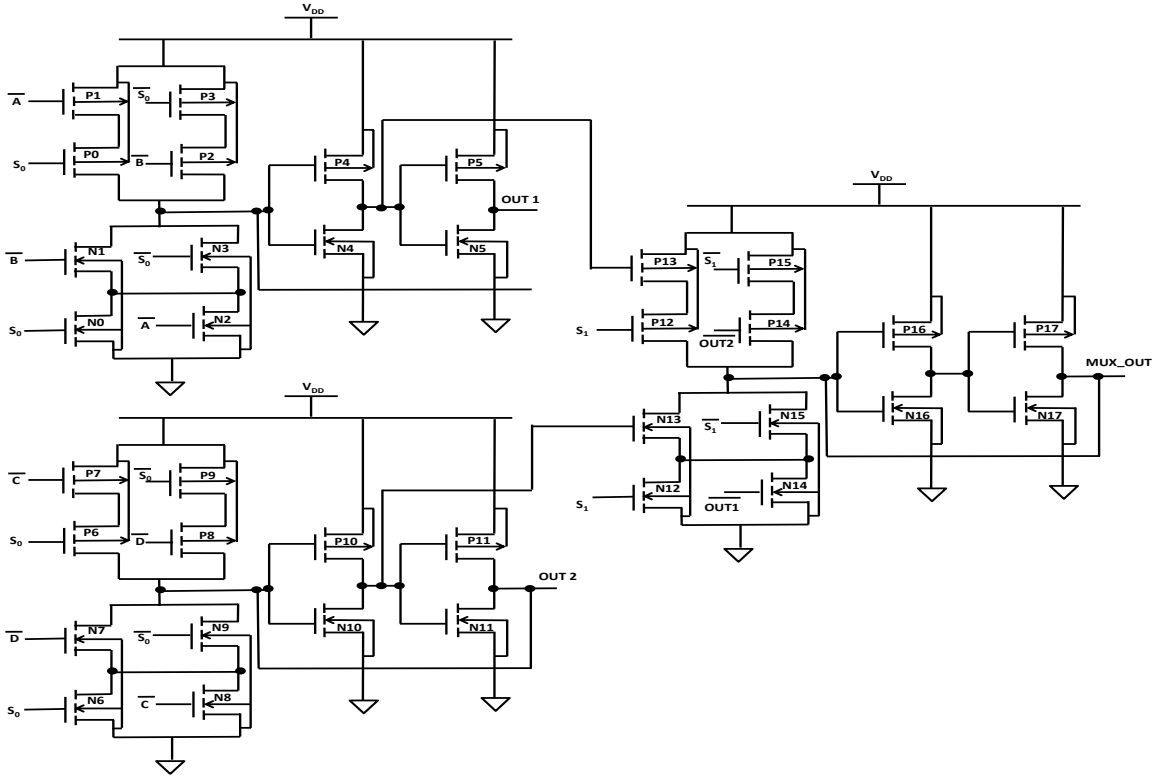
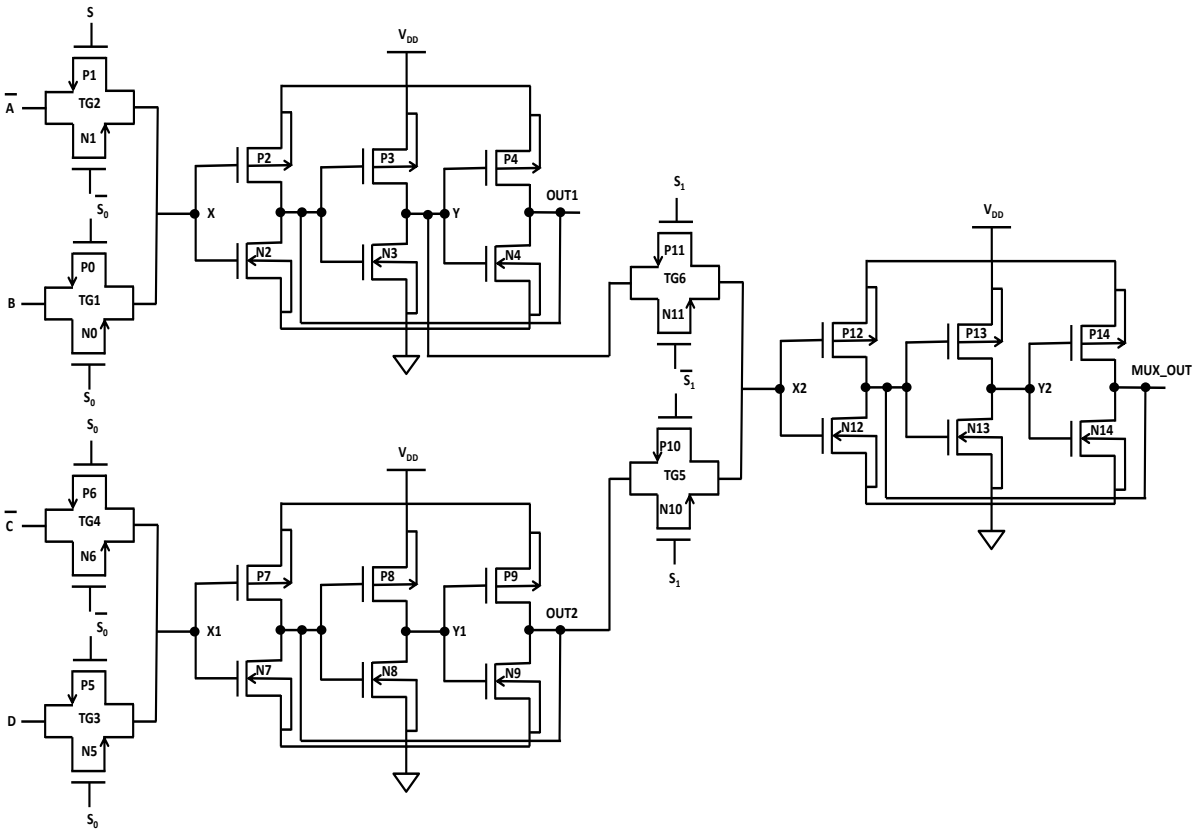


Fig. 3.12 Block diagram of 4:1 MUX



(a)



(b)

Fig. 3.13 Realization of 4:1 ST MUXs in different styles (a) TS ST (b) TG-TS ST

Table 3.7 Performance comparison of 4:1 ST MUXs

ST styles / Performance comparison	Conventional ST MUX [26]	DTMOS ST MUX [37]	VTCMOS ST MUX [38]	Proposed TS ST MUX	Proposed TG-TS ST MUX
	TT				
Transistor count	54	54	30	36	30
τ_d (ns)	9.04	5.11	5.77	15.94	4.63
P_{dyn} (nW)	113	20.48	2.4	57	9.2
PDP ($x10^{-18}J$)	1021	104.6	13.8	909	43
V_{HW} (mV)	29.3	19.4	92.9	267	205
	FF				
τ_d (ns)	5.74	3.59	3.61	8.21	2.67
P_{dyn} (nW)	221	78	5.9	217	26
PDP ($x10^{-18}J$)	1269	280	21.2	1782	69.4
V_{HW} (mV)	19.51	29.3	82.4	236.5	176.4
	SS				

τ_d (nS)	14.82	7.4	8.66	17.01	7.86
P_{dyn} (nW)	60	54	11.72	66	16.3
PDP ($x10^{-18}J$)	889.2	400	101.4	1123	128.11
V_{HW} (mV)	29.7	61	103	287	234
	SF				
τd (ns)	8.9	8.2	5.2	13.5	7.5
P_{dyn} (nW)	41.53	28.23	12.57	105	10.15
PDP ($x10^{-18}J$	370	231	65	1417	76.12
V_{HW} (mV)	29.71	29.79	87.81	275	195.74
	FS				
τ_d (ns)	8.1	7.5	4.69	15.5	7.2
P_{dyn} (nW)	74.63	29.14	8.16	98	15
PDP ($x10^{-18}J$)	605	219	38	1519	108
V_{HW} (mV)	28.85	20.06	92.94	275	206.24

3.6 Conclusion

This chapter presents two logic styles, namely TS ST logic and TG-TS ST logic with current feedback. The TS ST logic style has three stage inverter with positive feedback, and the second logic style is implemented by integrating transmission gates with the TS ST logic style. Both logic styles are investigated for the implementation of XOR2 functionality. The two proposed ST XOR2 gate designs are simulated using CMOS PTM 45nm technology node parameters. The performance of the proposed TS ST XOR2 and TG-TS ST XOR2 gates is compared with the existing ST XOR2 gates. It is found that the proposed TS ST XOR2 gate provides the highest noise immunity, followed by the proposed TG-TS ST XOR2 gate. The proposed TG-TS ST XOR2 gate has the lowest dynamic power consumption compared to existing ST XOR2 gates. Additionally, the proposed 4:1 TG-TS ST XOR2 multiplexer provides the lowest propagation delay and second highest noise immunity among all existing multiplexers. Further, the reliability of the proposed TS ST and TG-TS ST XOR2 gates is verified by process corner and voltage variation analysis, which confirms the effectiveness of the proposed ST logic styles among all design schemes. Overall, the proposed TG-TS ST logic gates are most suitable for low power, high performance, and high noise immune digital circuit design.

Chapter 4

Improved Voltage Feedback Static Schmitt Trigger Logic Gates

4.1 Introduction

The previous chapter deals with the comprehensive study of static ST with current feedback, which overcomes the power delay tradeoff issues. This chapter is devoted to static ST gates with voltage feedback. The existing work for static ST logic gates employing voltage feedback offers improvements in noise immunity, but at the cost of increased leakage current. The positive feedback transistors, connected in a voltage feedback configuration, create additional conduction paths or raise the effective drive strength of the pull-up/pull-down networks even in the steady-state condition. This results in higher leakage currents through the feedback transistors. Therefore, a new static logic style is proposed to overcome the leakage current issues, along with improved noise immunity.

4.2 Proposed Stacked VTCMOS Schmitt Trigger Logic Style

The conventional VTCMOS ST logic style cascades two stages such that the switching threshold voltage of transistors in the first stage is varied by the output of the second inverter. This arrangement improves noise margin at the cost of increased I_{OFF} values. The leakage current is reduced in the proposed ST logic style by introducing stacking in the PDN of the first stage. The proposed style is thus named as stacked VTCMOS ST logic and is referred to as the SVTCMOS ST logic style. The block diagram of the proposed SVTCMOS ST logic gate is shown in Fig. 4.1. It consists of PUN and PDN in the first stage, wherein the stacking of transistors is adopted in function realization. The subsequent output is then followed by a DTMOS inverter. The output V_{OUT} is connected to the body terminals of the transistors in the PUN and stacked PDN of the first stage. The stacked PDN transistors are a series connection of NMOS transistors. This arrangement increases the path resistance from output to ground, leading to a reduction in the leakage current values.

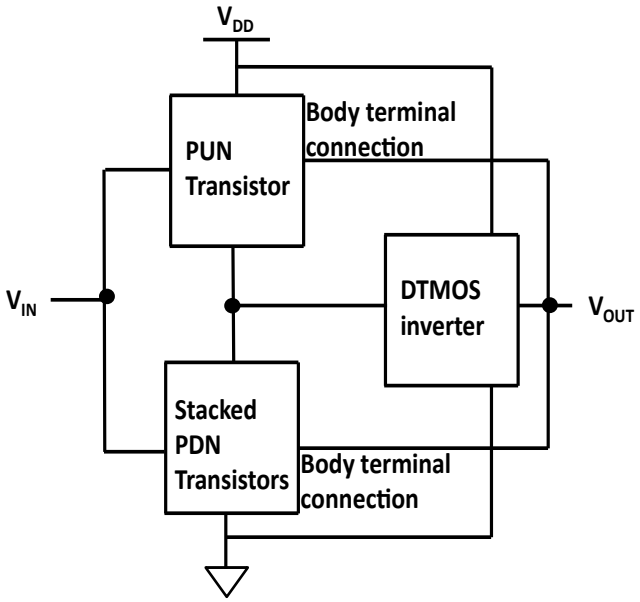


Fig. 4.1 Block diagram of the proposed SVTCMOS ST logic gate

4.2.1 Operation and Analysis

The schematic of the proposed SVTCMOS ST buffer with two inverters (SI1, SI2) is shown in Fig.4.2. The first inverter, SI1, has stacked transistors (N1, N2) in PDN, and transistor P1 forms PUN. This is followed by a second stage DTMOS inverter, SI2, consisting of transistors N3 and P2. The output of SI2 is connected to the substrate terminal of transistors in SI1. For a low value of input voltage V_{IN}, transistor P1 turns ON, charging intermediate node INT to a high voltage level. This high voltage turns ON transistor N3 such that the buffer attains a low output voltage level. Alternatively, for a high value of input voltage V_{IN}, both N1 and N2 conduct such that the node INT gets discharged to a low voltage level, and a high voltage level is obtained at the output of the SVTCMOS ST buffer.

The existing VTCMOS logic style has high leakage current value (I_{OFF}), thus suffers from degraded I_{ON}/I_{OFF} values. The proposed SVTCMOS logic style introduces stacking of transistors and integrates its advantages with the technique of variable threshold voltage for overall performance improvement. The stacking of transistors in the PDN of the style increases the effective series resistance and leads to significant leakage current reduction. This arrangement is beneficial for applications where leakage power becomes a dominant concern [45]. Additionally, the stacking along with variable threshold technique results in improved noise immunity due to increase in hysteresis width in comparison to the existing VTCMOS ST gates. This can be explained by considering a low to high transition at V_{IN} in the proposed SVTCMOS ST buffer. For the initial value of low voltage level at V_{IN}, the transistors N1, N2 maintain a zero substrate bias. However, substrate-source junction of transistor P1 is forward biased, forcing the threshold voltage to drop such that transistor P1 continues to maintain a high logic level at the INT node. Also, the stacking of transistors in PDN increases the effective resistance and requires more current to discharge the INT node. Hence, V_{IN} has to go much higher to maintain the necessary current to discharge the node. Therefore, the presence of forward bias substrate effect in P1 along with stacking of transistors increases the V_{HL} in the proposed SVTCMOS ST buffer in comparison to the existing VTCMOS ST buffer. Thus, the proposed SVTCMOS ST buffer has high hysteresis width leading to enhanced noise immunity.

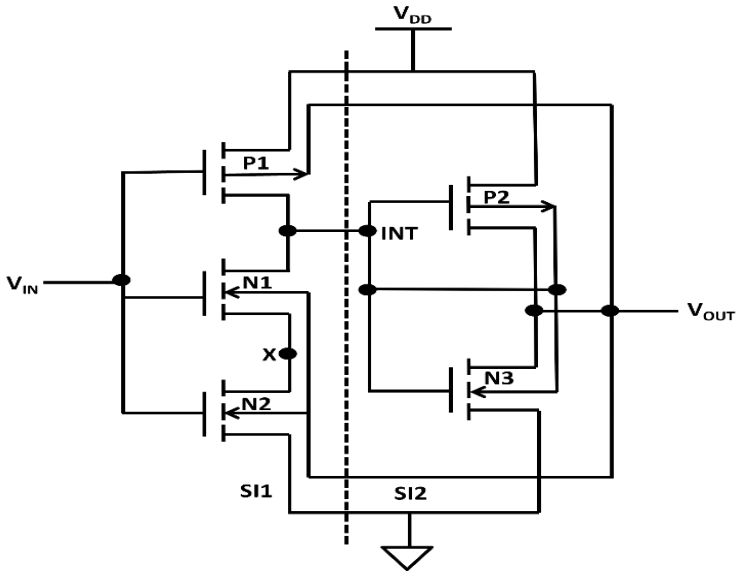


Fig. 4.2 Schematic of the proposed SVTCMOS ST buffer

A mathematical model to support the theoretical propositions is presented further.

I. Noise Immunity Improvement

The noise immunity is evaluated in terms the hysteresis width (V_{HW}) computed as the difference between two switching threshold voltages, V_{HL} and V_{LH}. For the proposed SVTCMOS ST buffer at V_{HL}, the transistors N1 and P1 operate in the saturation region with their substrate to source potential maintained at zero bias and forward bias, respectively. The switching threshold voltage, V_{HL} is calculated by equating the saturation current through transistors N1 and P1. The saturation current through transistors N1 ($I_{D,N1}$), P1 ($I_{D,P1}$) [1] is expressed as:

$$I_{D,N1} = W_{N1} V_{SAT,N1} C_{OX} \frac{(V_{gs} - V_{th0,N1})^2}{(V_{GS} - V_{th0,N1}) + E_{C,N1} L_{N1}} \tag{4.1}$$

$$I_{D,P1} = W_{P1} V_{SAT,P1} C_{OX} \frac{(V_{SG} - |V_{th,P1}|)^2}{(V_{DD} - V_{IN} - |V_{th,P1}|) + E_{C,P1} L_{P1}} \tag{4.2}$$

where $W_{N1}, V_{SAT,N1}, E_{C,N1}, L_{N1}$ and $W_{P1}, V_{SAT,P1}, E_{C,P1}, L_{P1}$ represent the channel width, saturation velocity, critical electric field, and channel length of transistors N1 and P1, respectively. The voltage $V_{th0,N1}$ represents the zero substrate bias threshold voltage of transistor N1, $V_{th,P1}$ is the forward substrate bias threshold voltage of transistor P1, and V_{X1} is the source potential of transistor N1.
The two current equations are equated as:

$$I_{D,N1} = I_{D,P1} \tag{4.3}$$

Substituting the values from Eq. (4.1) and (4.2) into Eq. (4.3) results:

$$W_{n1} V_{SAT,N1} C_{OX} \frac{(V_{HL} - V_{X1} - V_{th0,N1})^2}{(V_{GS} - V_{th0,N1}) + E_{C,N1} L_{N1}} = W_{P1} V_{SAT,P1} C_{OX} \frac{(V_{DD} - V_{HL} - |V_{th,P1}|)^2}{(V_{DD} - V_{IN} - |V_{th,P1}|) + E_{C,P1} L_{P1}} \tag{4.4}$$

By solving Eq. (4.4), V_{HL} is calculated as:

$$V_{HL} = \frac{(V_{DD} - |V_{th,P1}|) R \sqrt{\frac{V_{SAT,P1} E_{C,N1}}{V_{SAT,N1} E_{C,P1}}} + V_{X1} + V_{th0,N1}}{1 + R \sqrt{\frac{V_{SAT,P1} E_{C,N1}}{V_{SAT,N1} E_{C,P1}}}} \tag{4.5}$$

where $R = \sqrt{\frac{W_{P1}}{W_{N1}}}$

Similarly, the lower switching threshold voltage (V_{LH}) is determined during high to low transition in V_{IN}. At V_{LH}, the transistors N1 and P1 operate in the saturation region with their substrate potential maintained at forward bias and zero bias, respectively. By following the above method, the lower switching threshold V_{LH} is computed as:

$$V_{LH} = \frac{(V_{DD} - |V_{th0,P1}|)R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}} + V_{X2} + V_{th,N1}}{1 + R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}} \quad (4.6)$$

where $V_{th0,P1}$ is the zero substrate bias threshold voltage of transistor P1, $V_{th,N1}$ is the forward substrate bias threshold voltage of transistor N1, and V_{X2} is the source potential of transistor N1. By using Eq. (4.5) and (4.6), the hysteresis width of the proposed SVTCMOS ST buffer ($V_{HW_SVTCMOS}$) is computed as:

$$V_{HW_SVTCMOS} = V_{HL} - V_{LH}$$
$$= \frac{(|V_{th0,P1}| - |V_{th,P1}|)R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}} + (V_{X1} - V_{X2}) + (V_{th0,N1} - V_{th,N1})}{1 + R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}} \quad (4.7)$$

The accuracy of the above model is validated through SPICE simulations of the SVTCMOS ST buffer with a power supply of 0.4 V and value of R ranging from 1.4 to 2.4. The plots of the simulated and predicted values of hysteresis width, $V_{HW_SVTCMOS}$ are shown in Fig. 4.3. A maximum error of 18 % is observed for hysteresis width. It is found that there is close agreement between the simulated and the predicted values of the parameters for all the operating conditions.

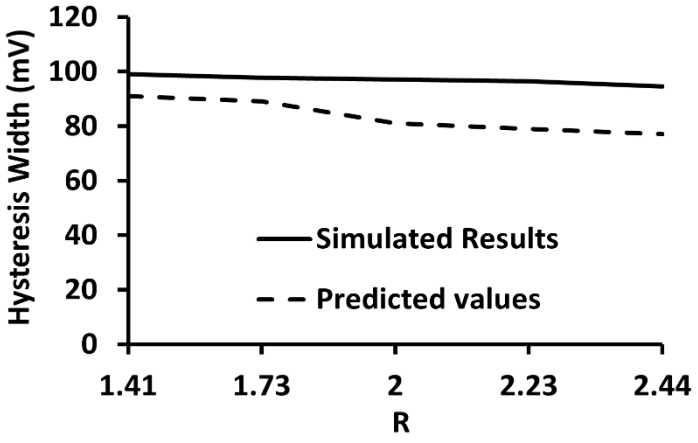


Fig. 4.3 Simulated vs predicted values of a hysteresis width, $V_{HW_SVTCMOS}$ of the SVTCMOS ST buffer

Analogously, the hysteresis width (V_{HW_VTCMOS}) for the existing VTCMOS ST buffer is derived in Chapter 2 and is rewritten below:

$$V_{HW_VTCMOS} = V_{HL} - V_{LH} = \frac{(|V_{th0,P1}| - |V_{th,P1}|)R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}} + (V_{th0,N1} - V_{th,N1})}{1 + R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}}} \quad (4.8)$$

The comparison reveals that the hysteresis width of the proposed SVTCMOS ST buffer ($V_{HW_SVTCMOS}$) is enhanced by $(V_{X1} - V_{X2})/(1 + R\sqrt{\frac{V_{SAT,P1}E_{C,N1}}{V_{SAT,N1}E_{C,P1}}})$ over the hysteresis width of the VTCMOS ST buffer (V_{HW_VTCMOS}). The results validate the improvement in hysteresis through the proposed SVTCMOS ST buffer.

II. Reduction in Leakage Current (I_{OFF})

The design of the SVTCMOS ST buffer employs stacking of transistors. The effect of this modification is analysed to determine the leakage current through N1 represented as ($I_{OFF,SVTCMOS_N1}$) for the case when it is driven by low value of input voltage V_{IN}. As N1 is OFF, the leakage current $I_{OFF,\ SVTCMOS_N1}$ is the subthreshold drain current equation [20] and is given as:

$$I_{OFF,SVTCMOS_N1} = I_0 \exp\left(\frac{V_{GS} - V_{th} - \eta V_{DS}}{nV_T}\right)\left(1 - \exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (4.9)$$

where I_0 is a constant dependent on W/L of transistor N1, V_{th} is the threshold voltage, η is drain induced barrier lowering coefficient, n is the subthreshold ideality factor, and V_T is the thermal voltage. By substituting V_{GS_N1} = -V_X, V_{DS_N1}= V_{DD} -V_X, V_{GS_N2} = 0, V_{DS_N2} = V_X and neglecting η for the sake of simplification in the above equation, the leakage current through transistors N1 ($I_{OFF,\ SVTCMOS_N1}$) and N2 ($I_{OFF,\ SVTCMOS_N2}$) can be expressed as:

$$I_{OFF,SVTCMOS_N1} = I_{0,N1} \exp\left(\frac{-(V_X + V_{th})}{nV_T}\right)\left(1 - \exp\left(\frac{-(V_{DD} - V_X)}{V_T}\right)\right) \quad (4.10)$$

$$I_{OFF,SVTCMOS_N2} = I_{0,N2} \exp\left(\frac{-V_{th}}{nV_T}\right)\left(1 - \exp\left(\frac{-V_X}{V_T}\right)\right) \quad (4.11)$$

Further, the node voltage V_X is determined by equating the current flowing through stacked transistors N1 and N2 in the proposed SVTCMOS ST buffer.

$$I_{OFF,\ SVTCMOS_N1} = I_{OFF,\ SVTCMOS_N2}$$

$$I_{0,N1}\exp\left(\frac{-(V_X+V_{th})}{nV_T}\right)\left(1-\exp\left(\frac{-(V_{DD}-V_X)}{V_T}\right)\right)=I_{0,N2}\exp\left(\frac{-V_{th}}{nV_T}\right)\left(1-\exp\left(\frac{-V_X}{V_T}\right)\right) \quad (4.12)$$

where $I_{0,N1}$ and $I_{0,N2}$ are constant dependent on the aspect ratio of N1 and N2 respectively. The node voltage V_X by considering $n\approx 1$ can be approximated:

From Eq. (4.12),

$$V_X = V_T \ln\left(\frac{I_{0,N1}\exp\frac{V_{DD}}{V_T}+I_{0,N2}\exp\frac{V_{DD}}{V_T}}{I_{0,N2}\exp\frac{V_{DD}}{V_T}+I_{0,N1}}\right) \quad (4.13)$$

The accuracy of the above model is validated through SPICE simulations of the proposed SVTCMOS ST buffer with a power supply V_{DD} ranging from .3V to .5V. The plots of the simulated and predicted values of $I_{OFF,SVTCMOS_N1}$is shown in Fig. 4.4. A maximum error of 19% is observed, which indicates a close agreement between the simulated and the predicted values for all the operating conditions. Similarly, for the existing VTCMOS ST buffer, the leakage current through transistor N1 ($I_{OFF,\ VTCMOS_N1}$) with V_{GS}=0, V_{DS}=V_{DD} is expressed as:

$$I_{OFF,VTCMOS_N1} = I_{0,N1}\exp\left(\frac{-V_{th}}{nV_T}\right)\left(1-\exp\left(\frac{-V_{DD}}{V_T}\right)\right) \quad (4.14)$$

Thus, the ratio of leakage currents in the existing and proposed ST buffers can be written as:

$$\frac{I_{OFF,VTCMOS_N1}}{I_{OFF,SVTCMOS_N1}} = \frac{\left(\exp\left(\frac{V_{DD}}{V_T}\right)-1\right)\left(\exp\frac{V_X}{nV_T}\right)}{\exp\left(\frac{V_{DD}}{V_T}\right)-\exp\left(\frac{V_X}{V_T}\right)} \quad (4.15)$$

By substituting the value of V_X from Eq. (4.13) in Eq. (4.15), the ratio of leakage currents is approximated as:

$$\frac{I_{OFF,VTCMOS_N1}}{I_{OFF,SVTCMOS_N1}} \approx 1+\frac{I_{0,N1}}{I_{0,N2}} \quad (4.16)$$

$$I_{OFF,SVTCMOS_N1} \approx \frac{I_{OFF,VTCMOS_N1}}{1+\frac{I_{0,N1}}{I_{0,N2}}} \quad (4.17)$$

The above equation clearly indicates that the proposed SVTCMOS ST buffer has reduced leakage current as compared to the VTCMOS ST buffer. The leakage current reduction in the proposed SVTCMOS ST buffer depends on the W/L ratio of transistors N1 and N2, which in turn relies on $I_{0,N1}/I_{0,N2}$.

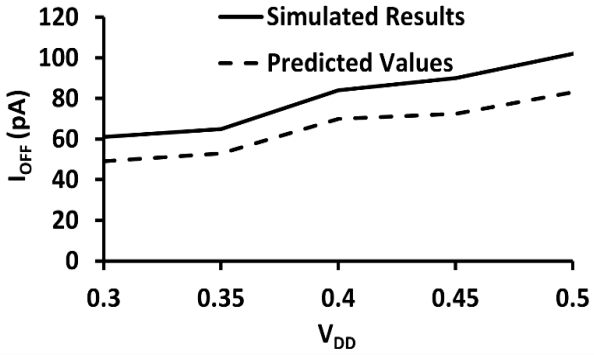


Fig. 4.4 Simulated vs predicted values for the I_{OFF} values of the proposed SVTCMOS ST logic buffer

The scheme for realizing two input gates in the SVTCMOS ST logic style requires replacing the transistors (N1, N2) and P1 in the SVTCMOS ST buffer with their corresponding PDN and PUN. The schematics of the SVTCMOS ST based AND2 and OR2 logic gates are presented in Fig. 4.5. The inverted functionalities such as NAND2 and NOR2 gates can be obtained from the same circuit by utilizing the output from the V_{INT} node. In the proposed SVTCMOS AND2 gate (Fig. 4.5 (a)), the inputs A and B drive the series-connected transistor pairs (N1, N2) and (N3, N4) in the PDN, respectively, while they drive two parallel transistors (P1, P2) in the PUN. The second stage controls the substrate of the first stage as in the SVTCMOS ST buffer. The modelling of the proposed SVTCMOS AND2 gate can be done by analysing the change in the output node due to a transition in one or both the inputs. The case of single input transition can be analysed in a manner similar to the SVTCMOS ST buffer. However, if the change in output occurs due to transition in both the inputs, then in this condition, the four transistors in series can be replaced by two transistors with doubled channel length, and the two transistors in parallel can be replaced by a single transistor having twice the channel width. Thus, the effective value of R' for the proposed SVTCMOS ST AND2 gate with $W_N' = \frac{W_{N1}}{2}$ and $W_P' = 2W_{P1}$ is computed as:

$$R' = \sqrt{\frac{W_P'}{W_N'}} = \sqrt{\frac{4W_{P1}}{W_{N1}}} = 2R \tag{4.18}$$

In the case of the proposed SVTCMOS ST OR2 gate (Fig. 4.5 (b)), the inputs A and B drive the parallel connected transistors (N1, N2) and (N3, N4) respectively while they drive two series transistors (P1, P2) in the PUN. The second stage controls the substrate of first stage as in SVTCMOS ST buffer. The two parallel NMOS transistors in the proposed SVTCMOS OR gate can be replaced by single transistor having doubled channel width and two PMOS transistors in series can be replaced by single transistor having doubled channel length. The

effective value of R'' for the SVTCMOS ST OR2 gate with $W_N'' = 2W_{N1}$ and $W_P'' = \frac{W_{P1}}{2}$ is computed as:

$$R'' = \sqrt{\frac{W_P''}{W_N''}} = \sqrt{\frac{W_{P1}}{4W_{N1}}} = \frac{R}{2} \tag{4.19}$$

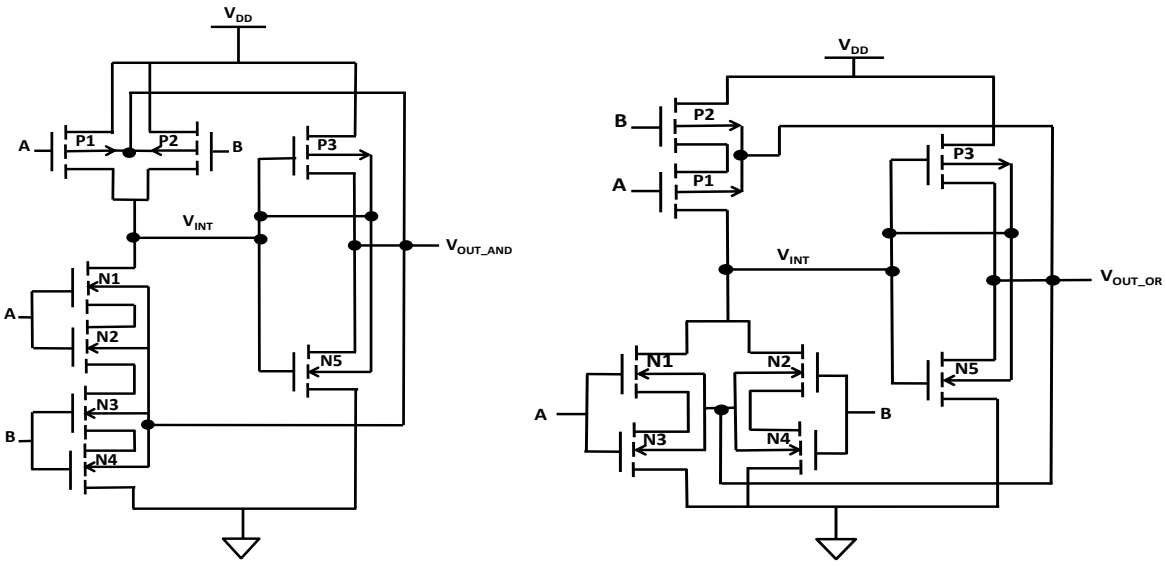


Fig. 4.5 Proposed SVTCMOS ST gates (a) AND2 (b) OR2

4.2.2 Simulation Results

The performance of the proposed SVTCMOS ST gates is compared with their counterparts designed using conventional ST and other existing ST logic styles, namely DTMOS ST and VTCMOS ST gates. For conventional ST and DTMOS ST gates, a dynamic threshold inverter is connected at the output for logical equivalence with VTCMOS ST and SVTCMOS ST styles [38]. The aspect ratio of the transistors taken in the simulation of buffers is listed in Table 4.1. All the buffers are simulated in LTspice using 45 nm PTM CMOS technology parameters with supply voltage and load capacitance of 0.4 V and 100 fF, respectively. The effect of process variation at different corners and power supply on the performance of all the buffers is also studied. The simulation results at different process corners are summarized in Table 4.2. The results at the 32 nm CMOS technology node are also listed in Table 4.3.

Table 4.1 Aspect ratio of different transistors in ST buffers

Transistors / **ST styles**	**W/L of NMOS transistors**	**W/L of PMOS transistors**
Conventional ST [28]	N1=2, N2=4, N3=2	P1=8, P2=8, P3=3
DTMOS ST [37]	N1=2, N2=4, N3=2	P1=8, P2=8, P3=3
VTCMOS ST [40]	N1=2, N2=2	P1=2, P2=1.4
Proposed SVTCMOS	N1=2, N2=1, N3=2	P1=8, P2=1.4

Table 4.2 Performance comparison of ST buffers at different process corners

ST styles / Performance comparison	Typical Corner			
	Conventional ST [28]	**DTMOS ST [37]**	**VTCMOS ST [40]**	**Proposed SVTCMOS ST**
V_{HW} (mV)	37.36	47.77	92.78	99.14
I_{OFF} (pA)	11	5.5	637.66	84
P_{dyn} (µW)	.45	2.9	1.86	.66
τ_d (ns)	24.16	8.08	9.87	24.13
PDP (10^{-15}J)	11.79	23.65	18.35	16.02
Area $(\mu m)^2$	2.78	2.74	1.56	1.79
	Post layout results			
τ_d (ns)	24.9	8.75	10.3	24.85
P_{dyn} (µW)	.50	3.2	2.1	.72
	Fast corner			
V_{HW} (mV)	43.59	78.09	71.48	80.05
I_{OFF} (pA)	2.20	6.8	2300	190
P_{dyn} (uW)	1.03	4.31	3.20	1.14
τ_d (ns)	12.69	6.30	6.14	12.71
	Slow corner			
V_{HW} (mV)	18.16	37.9	103.48	109.45
I_{OFF} (pA)	3.93	2.25	224.11	69.33
P_{dyn} (uW)	0.23	1.91	1.23	.47
τ_d (ns)	49.5	10.81	18.96	48

T:Typical, F:Fast, S:Slow

The following observations can be drawn from the simulation results at typical design corner.

- The noise immunity of ST buffers is analysed in terms of their respective hysteresis width (V_{HW}). It can be observed that DTMOS ST buffer has better V_{HW} than conventional ST buffer due to dynamic threshold technique that results in higher V_{HL} value and lower V_{LH} value in comparison to conventional ST buffer. The VTCMOS ST buffer has improved V_{HW} over DTMOS ST buffer as the turn-ON voltage of each transistor at zero body bias is greater than normal transistor in other buffers. Further, the proposed SVTCMOS ST buffer obtained maximum V_{HW} improvement of 165 %, 107 %, and 7 % over conventional ST, DTMOS ST and VTCMOS ST, respectively. Additionally, the noise immunity is also investigated by the noise spectral density curve shown in Fig. 4.6. The noise spectral density of the proposed SVTCMOS ST logic buffer is the lowest among all the existing buffers for the entire frequency range, indicating that the proposed SVTCMOS ST logic provides ST gate with the highest noise immunity. Further, the proposed SVTCMOS ST buffer significantly reduces the I_{OFF} value by 87 % compared to the VTCMOS ST logic buffer. By considering improvements in V_{HW} simultaneously, it can be stated that the proposed SVTCMOS ST buffer provides an improved noise margin with reduced I_{OFF} values. The other existing conventional and DTMOS ST buffers, though, have reduced I_{OFF}

value but fail to provide high noise immunity and hence are not preferred in logic gate design.

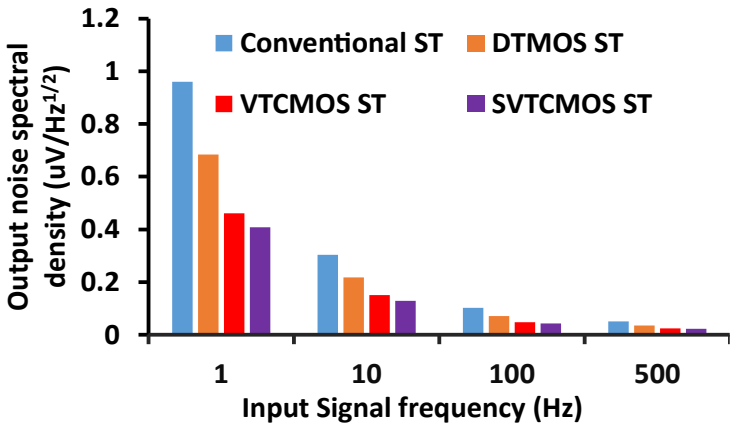


Fig. 4.6 Output noise spectral density of ST logic buffers at different frequencies

- The DTMOS ST buffer has the highest dynamic power consumption as it employs a current feedback path to enhance noise immunity. The proposed SVTCMOS ST buffer in contrast, shows dynamic power reduction of 77 % and 64 % as compared to DTMOS ST and VTCMOS ST buffers, respectively, whereas it is comparable with the conventional ST buffer. The stacking of transistors reduces the I_{OFF} values in the proposed SVTCMOS ST buffer by increasing the turn-ON voltage of each transistor at zero bias conditions. The proposed SVTCMOS ST buffer has a comparable propagation delay with conventional ST buffer, except for DTMOS ST and VTCMOS ST buffers. Further, the proposed SVTCMOS ST buffer shows a decrease in PDP value by 32 % and 12.6 % in comparison to DTMOS ST and VTCMOS ST buffers, as listed in Table 4.2. In addition, the dynamic power and propagation delay of the SVTCMOS ST logic buffer are compared due to variations in the W/L ratio of transistor N2 as shown in Fig. 4.7. The decreasing trend of the W/L ratio shows a reduction in dynamic power and an increase in propagation delay due to decreased dynamic power values.

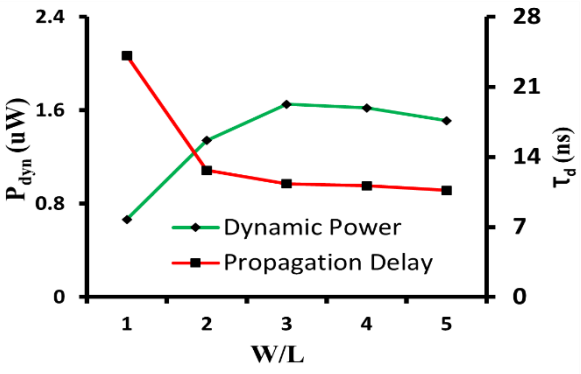


Fig. 4.7 Effect of change in W/L ratio of the transistor (N2) on dynamic power and propagation delay in the proposed SVTCMOS ST buffer

The layout of all the buffers is drawn on MICROWIND, and the occupied area is mentioned under Typical design in Table 4.2. The layout of VTCMOS ST and proposed SVTCMOS ST logic buffers is shown in Fig. 4.8. It is observed that the proposed SVTCMOS ST buffer consumes the least area, except for the VTCMOS ST buffer. The area of the SVTCMOS ST buffer reduces by 35 % and 34 % in comparison to the conventional ST and DTMOS ST buffers. The post layout results show that the propagation delay and dynamic power consumption increase due to increase in parasitic capacitances. So, careful transistor placement, sizing, and routing have been done to minimize the parasitic effects.

The effect of process variation at different corners and power supply on the performance of all the buffers is studied. The results are listed in Table 4.2. It is observed that all the buffers exhibit correct functionality at all design corners, and their corresponding voltage transfer characteristics (VTC) are shown in Fig. 4.9. Like typical corner, the same trend in improvement for hysteresis width is noticed at fast and slow corners, except for the VTCMOS ST buffer (fast corner) from Table 4.2. The worst and best possible case at a fast corner is observed for the DTMOS ST and conventional ST buffers, respectively, whereas at a slow corner, they are spotted for the conventional ST and proposed SVTCMOS ST buffers, respectively. The effect of process variation at fast and slow corners on I_{OFF} and dynamic power is maximum for the conventional ST buffer, whereas it is minimum for the proposed SVTCMOS ST logic buffer. As far as propagation delay is concerned, the effect of process variation at fast and slow corners is maximum for the conventional ST buffer and minimum for the DTMOS ST logic buffer. Moreover, all ST buffers have a lower propagation delay at the fast corner and a higher propagation delay at the slow corner in comparison with the typical corner. The high-speed benefit at the fast corner results from the lowering of the threshold voltage of NMOS and PMOS transistors. Similarly, the high threshold voltage of NMOS and PMOS transistors at the slow corner results in low speed. In the case of the slow corner, the propagation delay of the conventional ST, DTMOS ST, VTCMOS ST, and proposed SVTCMOS ST logic buffers increases by 47 %, 22 %, 38 %, and 47 %, respectively, in comparison to the typical corner, while the corresponding percentage decrease of 104 %, 34 %, 92 % and 98 % is observed at the fast corner.

Table 4.3 Performance comparison of ST buffers at different technology nodes

ST gates / **Performance comparison**	**Conventional ST [28]**	**DTMOS ST [37]**	**VTCMOS ST [40]**	**Proposed SVTCMOS ST**
	45nm			
V_{HW} (mV)	37.36	47.77	92.78	99.14
I_{OFF} (pA)	11	5.5	637.66	84
P_{dyn} (µW)	.45	2.9	1.86	.66
τ_d (ns)	24.16	8.08	9.87	24.13
	32 nm			
V_{HW} (mV)	27.99	28.6	53.5	57.3
I_{OFF} (pA)	15	6.85	813.3	94
P_{dyn} (µW)	0.33	1.32	.94	0.35
τ_d (ns)	32	11.72	11.33	35

The performance of the ST logic buffers using 32 nm PTM technology parameters in LTspice is listed in Table 4.3. The SVTCMOS ST buffer shows maximum V_{HW} improvement of 104 %, 100 %, and 7 % over conventional ST, DTMOS ST, and VTCMOS ST, respectively. Further, the SVTCMOS ST buffer achieves significant I_{OFF} reduction by 88.4 % in comparison to the existing VTCMOS ST buffer. The SVTCMOS ST buffer shows dynamic power reduction of 73 % and 62 % as compared to DTMOS ST and VTCMOS ST buffers, respectively, whereas it is comparable to a conventional ST buffer. The SVTCMOS ST buffer has increased propagation delay values in comparison to DTMOS ST and VTCMOS ST buffers. The performance trends observed are consistent with those obtained using the 45 nm technology.

Effect of Supply Voltage Variation

The effect of supply voltage variation on V_{HW}, I_{OFF}, dynamic power, and propagation delay is shown in Fig. 4.10. The original graph shown for I_{OFF} in Fig. 4.10 (b) has been magnified for the sake of clear visibility. Overall, it is observed that there is a decrease in hysteresis width, I_{OFF}, dynamic power, and an increase in propagation delay with decrease in supply voltage.

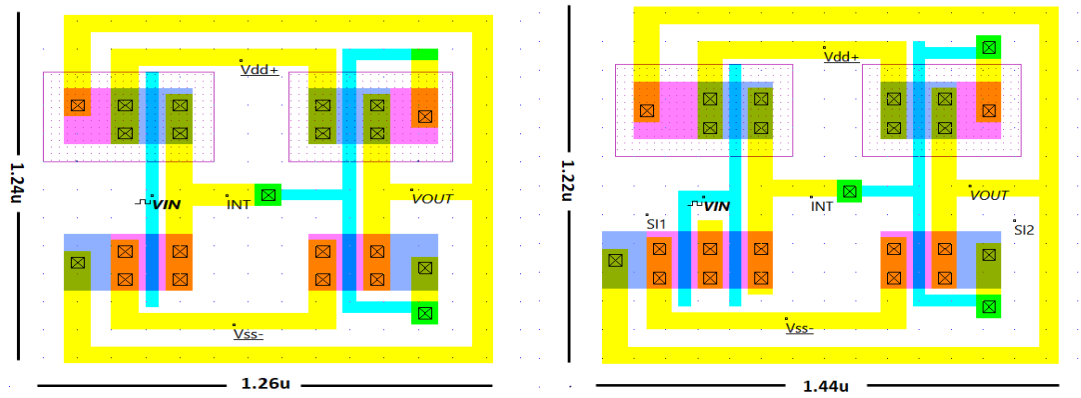


Fig. 4.8 Layout of ST buffers (a) VTCMOS (b) SVTCMOS

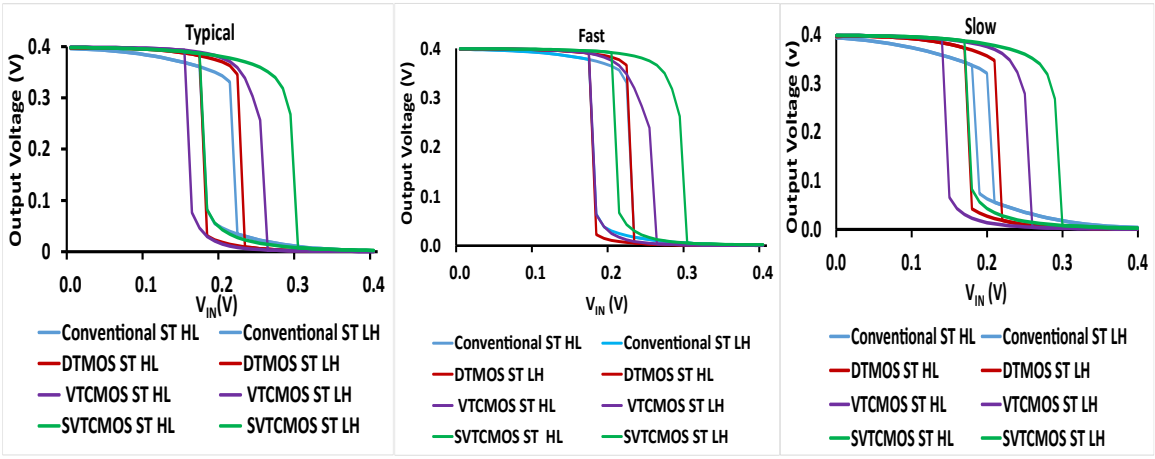


Fig. 4.9 VTC of ST buffers at different process corners

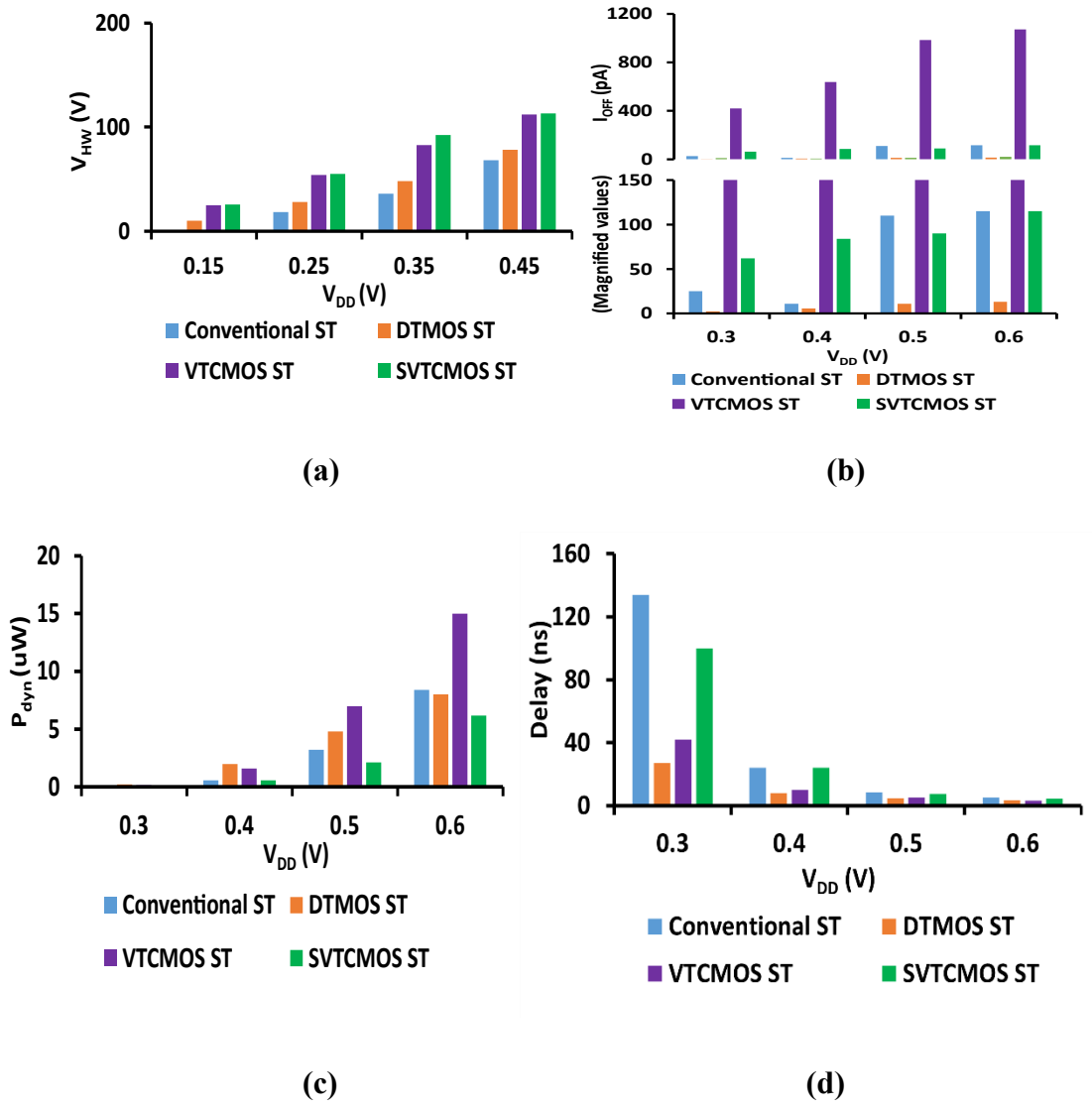


Fig. 4.10 Performance measurements with respect to variations in supply voltage (a) V_{HW} (b) I_{OFF} (c) P_{dyn} (d) τ_d

- The OR2 and AND2 functionality are realized in existing VTCMOS and proposed SVTCMOS ST logic styles. It is observed that a reduction of 50 % in the I_{OFF} value is obtained in the proposed SVTCMOS ST OR2 gate at the cost of 7 % increase in propagation delay, while the other parameters, V_{HW}, and dynamic power remain comparable with the VTCMOS OR2 gate. Further, the V_{HW} of the proposed SVTCMOS ST OR2 gate exhibits less process variation than the VTCMOS ST OR2 gate at typical and fast corners. The VTC at different process corners for ST OR2 gates is shown in Fig. 4.11. Also, the I_{OFF} of the proposed SVTCMOS ST OR2 gate has less process variation than the VTCMOS ST OR2 gate with comparable switching current and propagation delay variation. Similar results analysis is confirmed for the AND2 gate for the result listed in Table 4.4. Hence, it is verified that the proposed SVTCMOS ST logic style leads to the design of low leakage ST gates with high noise immunity with less variations.

Table 4.4: Performance comparison of logic gates at different process corners

ST styles / Performance comparison	Style (ST OR2)					
	Typical		Fast		Slow	
	VTCMOS	SVTCMOS	VTCMOS	SVTCMOS	VTCMOS	SVTCMOS
V_{HW} (mV)	93.13	90.84	72.06	80.48	103.72	110.08
I_{OFF} (pA)	281.44	141	1000	365	98	107
P_{dyn} (uW)	.74	.79	1.09	1.18	.46	.46
τ_d (ns)	12.89	13.85	7.4	7.95	24.88	25.99
	Style (ST AND2)					
V_{HW} (mV)	92.75	94.27	74	84	103.33	111.62
I_{OFF} (pA)	291.76	594	774.67	749	191.15	637
P_{dyn} (uW)	1.94	1.50	3.17	2.60	1.28	.79
τ_d (ns)	11.13	11.83	6.82	7.065	20.90	22.30

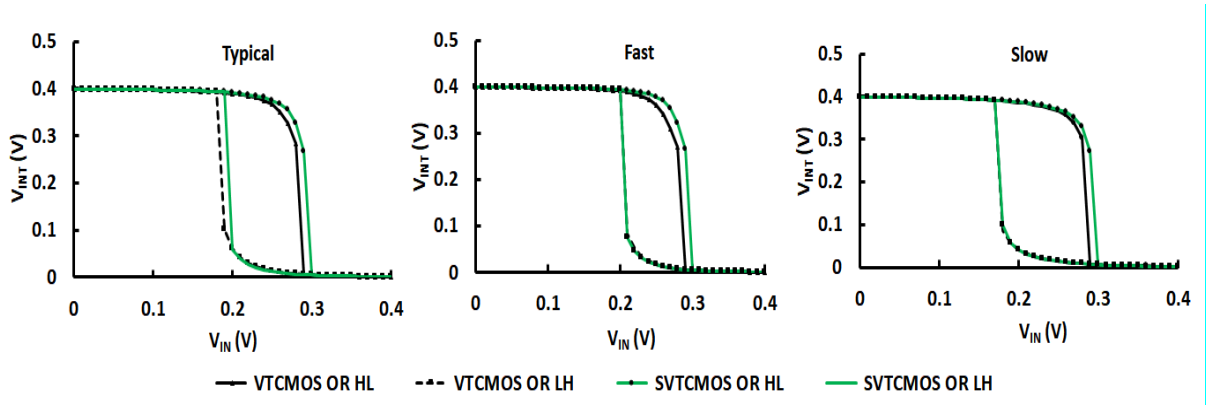
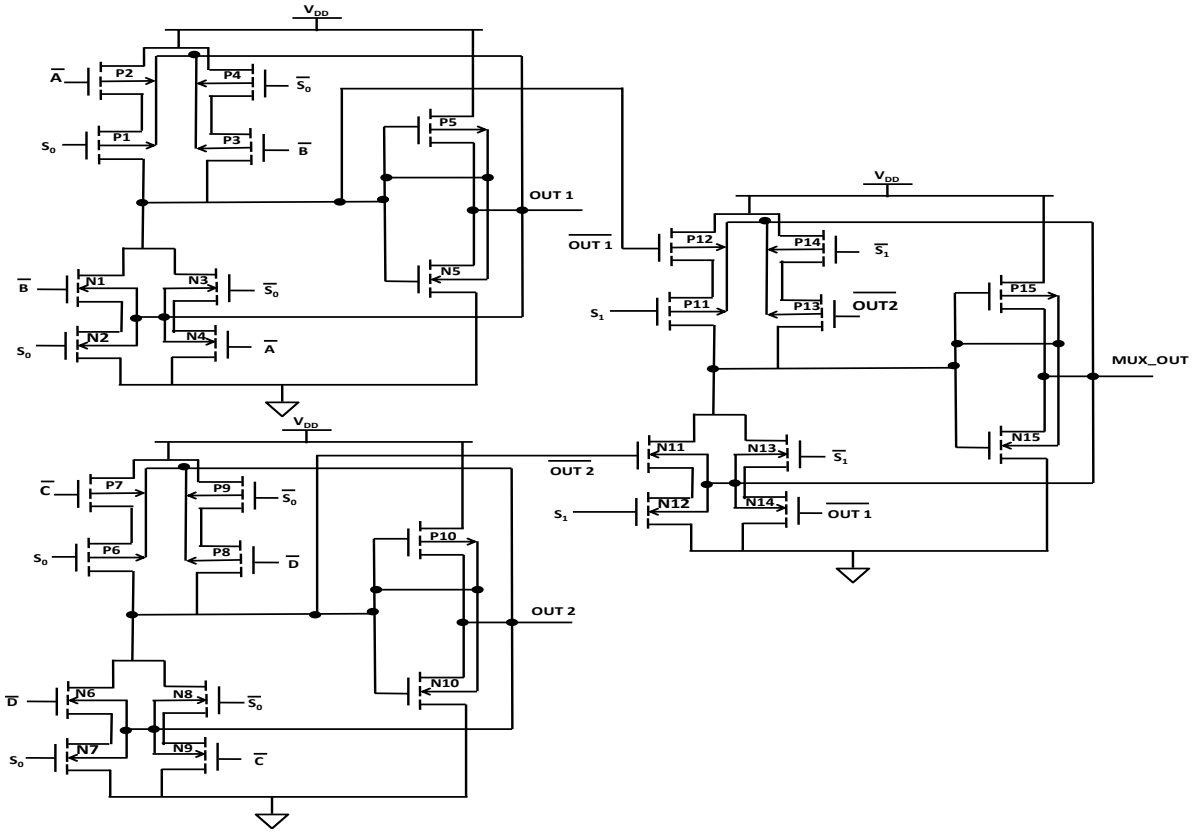


Fig. 4.11 Voltage transfer curve at different process corners for VTCMOS and proposed SVTCMOS ST OR2 gates

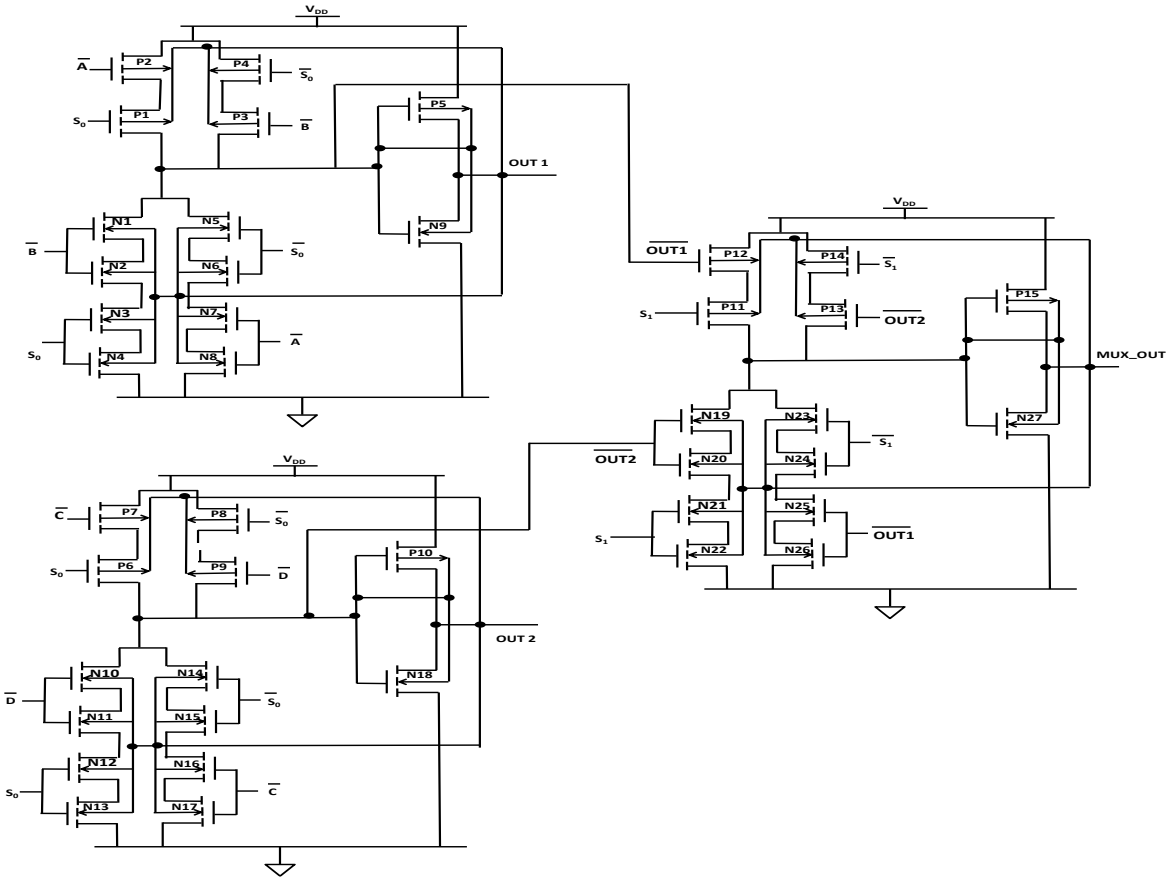
4.3 Design Example using Proposed SVTCMOS ST logic style

4:1 ST MUX

A 4:1 ST MUX is taken as a design example. All the MUXs are simulated in LTspice using 45 nm PTM CMOS technology parameters with a supply voltage and load capacitance of 0.4 V and 100 fF, respectively. The block diagram of the 4:1 MUX is shown in Fig. 3.12. The design employs two 2:1 MUXs in the first stage, which is followed by one 2:1 ST MUX in the second stage. The design of 4:1 VTCMOS and SVTCMOS ST MUXs is shown in Fig. 4.12. Both MUXs are simulated and the results of different performance parameters are listed in Table 4.5. The proposed SVTCMOS ST MUX decreases leakage current and dynamic power consumption by 83 % and 64 %, respectively, in comparison to the 4:1 VTCMOS ST MUX. Furthermore, the proposed SVTCMOS ST MUX has a higher hysteresis width than the VTCMOS ST MUX. It is observed that the VTCMOS ST MUX shows an optimum solution for the propagation delay.


VDD
A
P2
P4
S0
P1
S0
P3
B
P5
OUT 1
B
N1
N3
S0
N2
S0
N4
A
N5
VDD
OUT 1
P12
P14
S1
S1
P11
P13
OUT2
P15
MUX_OUT
N11
N13
S1
OUT 2
S1
N12
N14
OUT 1
N15
VDD
C
P7
P9
S0
S0
P6
P8
D
P10
OUT 2
D
N6
N8
S0
S0
N7
N9
C
N10

(a)


VDD
A
P2
P4
S0
S0
P1
P3
B
P5
OUT 1
B
N1
N5
N9
S0
N2
N6
N3
N7
A
S0
N4
N8
VDD
OUT1
P12
P14
S1
S1
P11
P13
OUT2
P15
MUX_OUT
N19
N23
S1
OUT2
N20
N24
N21
N25
S1
OUT1
N22
N26
N27
VDD
C
P7
P8
S0
S0
P6
P9
D
P10
OUT 2
D
N10
N14
N18
S0
N11
N15
N12
N16
C
S0
N13
N17

(b)

Fig. 4.13 Realization of 4:1 ST MUXs in different styles (a) VTCMOS ST (b) SVTCMOS ST

Table 4.5 Performance comparison of 4:1 ST MUX

ST styles / Performance comparison	VTCMOS	SVTCMOS
V_{HW} (mV)	108	115
I_{OFF} (pA)	1550	250
P_{dyn} (µW)	5	1.9
τ_d (ns)	21	42

4.4 Conclusion

This chapter is devoted to the design of improved static ST gates with voltage feedback. It presents a low leakage stacked variable threshold CMOS (SVTCMOS) ST logic style. The proposed SVTCMOS ST logic style integrates the stacking of transistors with the variable threshold voltage technique. Mathematical derivations are presented, which show reduction in leakage current and enhancement in hysteresis width with reference to the VTCMOS ST logic style. Simulations are performed using LTspice at 45 nm PTM CMOS technology node for different logic gates. The mathematical results are also validated through simulation results. It is observed that the proposed SVTCMOS ST buffer shows a reduction of 87 % and 64 % in leakage current and dynamic power, respectively, along with an increase of 7 % in hysteresis width with respect to the existing VTCMOS ST logic buffer. Further, a 4:1 MUX is designed and simulated using the SVTCMOS ST logic buffer. It is observed that the proposed 4:1 SVTCMOS ST MUX shows a significant decrease in the leakage current and dynamic power in comparison to the VTCMOS ST MUX. The 4:1 SVTCMOS ST MUX also has more noise immunity than the VTCMOS ST MUX. The process corner and voltage variation analysis results indicate more robustness towards variation in comparison to existing ST logic counterparts. Thus, the proposed SVTCMOS ST logic gate is applicable for the energy constrained applications.

Chapter 5

Modified Domino Schmitt Trigger Logic Gates

5.1 Introduction

The previous chapter deals with the comprehensive study of static ST with voltage feedback, which reduces leakage current by maintaining improved noise immunity. This chapter is devoted to the dynamic CMOS ST logic gate. The dynamic CMOS ST logic gate is a specialized class of digital gates that incorporates the Schmitt trigger functionality within dynamic CMOS logic. The dynamic ST gates are preferred over static ST logic gates due to the high speed obtained at the cost of degraded noise immunity. In this chapter, the focus is to enhance the performance of domino ST logic gates in terms of speed and noise immunity. The use of dynamic threshold MOSFET (DTMOS) in PDN is suggested and the performance of new DTMOS ST gates is analysed and compared with the existing dynamic ST gates. A brief discussion on DTMOS is presented, which is followed by detailed discussion and analysis of the proposed style.

5.2 DTMOS Technique

A dynamic threshold voltage MOSFET (DTMOS) is a transistor that has a buried oxide built on silicon wafer. High doses of arsenic and boron for source/drain terminals and polysilicon gate implants are used to create NMOS and PMOS with N+ and P+ poly gates, respectively. It is suitable for ultra-low voltage (0.6 V and below) in VLSI circuits [36], [46]. The device can have four terminals or three terminals layout. A four terminal layout provides separate source, drain, gate, and substrate (body) contacts, which allows operation in both standard and DTMOS modes. The schematic of a four-terminal DTMOS is shown in Fig. 5.1 (a). For DTMOS mode, the gate terminal is tied to the substrate as illustrated through the cross-section of a DTMOS shown in Fig. 5.1 (b). This is achieved through three terminal layout wherein hard local gate-substrate connections are fabricated, as illustrated in Fig. 5.1 (c). The connection results in a forward-biased substrate-source junction in DTMOS, in contrast to the reverse-biased substrate-source junction in a standard MOSFET. The forward bias substrate-source junction results in the threshold voltage drop. For an N-DTMOS, the threshold voltage (V_{th0_ND}) [68] with substrate-bias set to zero is given as:

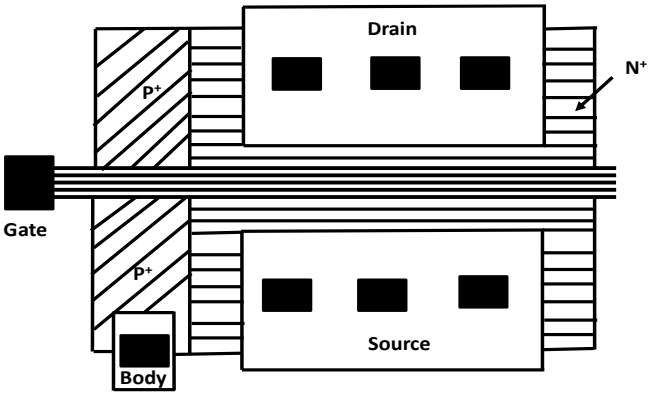
$$V_{th0_ND} = 2\phi_B + V_{FB} + \frac{\sqrt{2\epsilon_S q N_a 2\phi_B}}{C_{OX}} \tag{5.1}$$

where V_{FB} is the flat band voltage, $2\phi_B$ is the inversion layer potential, ϵ_S is Si permittivity, q is the electron charge, N_a is the channel doping, and C_{ox} is the gate oxide capacitance.

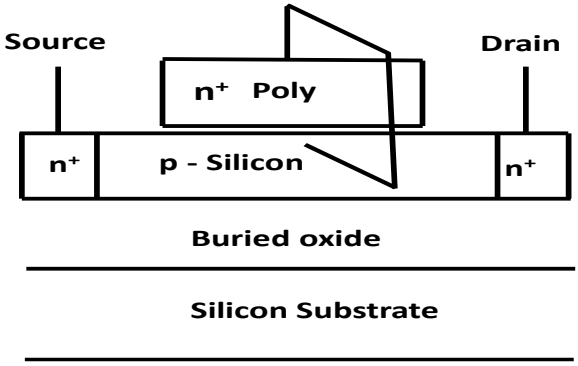
When the substrate-source junction is forward-biased, the corresponding threshold voltage is given as:

$$V_{th_ND} = 2\phi_B + V_{FB} + \lambda\sqrt{2\phi_B - V_{BS}} \tag{5.2}$$

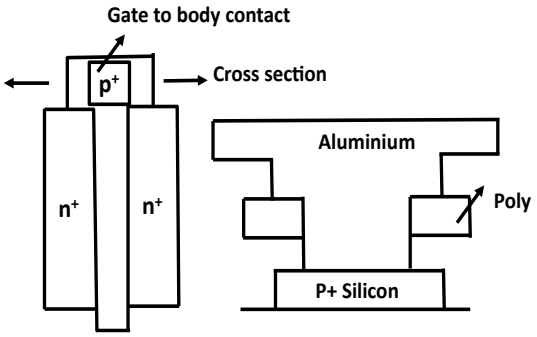
where $\lambda = \sqrt{2\epsilon_S q N_a} / C_{ox}$



(a)



(b)



(c)

Fig. 5.1 (a) Schematic of the body (substrate) contact DTMOS (b) Cross section of a DTMOS (c) Gate-to-substrate connection by using aluminium to short the poly gate to the p^+ region [68]

It may further be noted that the lowering of threshold voltage in DTMOS does not come at the expense of higher leakage current because at $V_{GS}=V_{BS}=0$, the DTMOS and the standard MOSFET have the same threshold voltage, consequently, they have the same leakage current. However, the voltage drop in DTMOS results in higher drain current, resulting in high dynamic power and faster switching. It has been observed that the increase in dynamic power is marginal as compared to speed enhancement [68]. Thus, the use of DTMOS for the design of domino ST logic gates is carried out.

5.3 Proposed Domino ST Logic Style

The dynamic ST logic gate is a specialized class of digital gates that incorporates the Schmitt trigger functionality within a dynamic logic style. A dynamic ST gate is clock-driven and works on the principle of precharge and evaluate logic. A domino ST logic gate is an improved form of a dynamic ST gate, which facilitates direct cascading of dynamic ST gates. A Domino ST logic gate consists of two stages, wherein the first stage implements the logic function and the second stage employs a CMOS inverter. The block diagram of the proposed domino ST logic gate is shown in Fig. 5.2. The first stage consists of a precharge transistor, an evaluation transistor, and PDN that realizes the functionality by using DTMOS. It also consists of a feedback network (FBN) to obtain hysteresis and a weak keeper transistor for the purpose of maintaining a high potential at the dynamic node. The second stage is a CMOS inverter to avoid malfunction due to the direct cascading of the first stage only. The proposed domino ST logic aims to improve the speed and noise immunity in comparison to its existing counterparts.

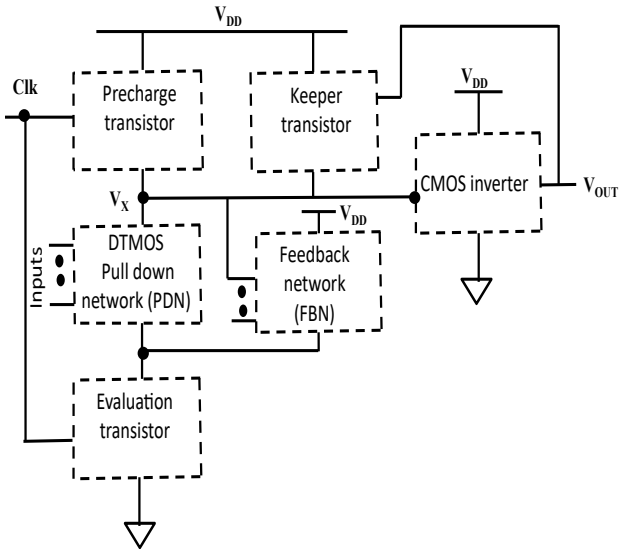


Fig. 5.2 Block diagram of domino ST logic gate

5.3.1 Operation and Analysis

The schematic of the proposed domino ST logic buffer is shown in Fig. 5.3. The first stage has a precharge transistor (P0), an evaluation transistor (N0), and a PDN with a DTMOS transistor N1. The FBN has a transistor N2, and P1 is used as a weak keeper transistor. The second stage is a CMOS inverter. The operation of the gate is controlled by the clock (Clk) signal. During the precharge phase (Clk = 0), the precharge transistor P0 is ON and the evaluation transistor N0 is OFF, such that dynamic node X gets precharged to V_{DD} due to the formation of a conducting path from V_{DD}. This further produces a low output at the domino output node OUT of the proposed buffer. The keeper transistor P1 turns ON and provides an alternate conducting path with low current values from the power supply to dynamic node X. Additionally, the high voltage at node X turns ON transistor N2 such that node A, which is also the source of transistor N1 attains a high potential. Thus, the drain and source terminals of transistor N1 are almost at the same potential, which limits current flow across it and helps in maintaining a strong one at node X. This ensures that a strong zero is maintained at the output node OUT of the proposed domino ST buffer. Conversely, during the evaluation phase (Clk = V_{DD}), P0 is OFF and N0

conducts such that the output gets evaluated depending on the value of IN. For a low value of IN, dynamic node X remains at high potential and a low output voltage level is obtained at the domino output OUT. The keeper transistor which is ON in this condition also helps to maintain a strong one voltage level at the dynamic node X during the evaluation phase as the precharge transistor is turned OFF. Further, the ON feedback transistor N2 raises the voltage at node A and limits the current flow between node X and internal nodes. This ensures strong one at dynamic node X and availability of strong zero at domino output node OUT. It is to be noted that since the transistor N2 is in weak conduction and N0 is ON, there exists a weak conduction path leading to a slight increase in power during this input condition. However, for the high value of input IN, the substrate-source junction of DTMOS N1 gets forward biased. This results in lowering of the threshold voltage of DTMOS N1 (in accordance with Eq. 5.2). The decrease in threshold voltage helps quick discharge of the dynamic node X and results in speed enhancement.

The keeper transistor P1 further enhances the noise immunity and thus makes the circuit more robust against noise and voltage fluctuations. This can be explained by considering the low logic level at the IN terminal of the proposed gate. When IN is at a low logic level, the dynamic node X and the domino output OUT are expected to be high and low logic levels, respectively. Since initially the OUT is at a low logic level, it turns ON the keeper transistor P1. During a low-to-high transition at IN, it is expected that dynamic node X to have a transition from high-to-low. The transistor N1 tries to lower the potential of node X, but the weak keeper transistor pulls it up to a high logic level. Hence, IN has to go much higher to maintain the necessary current to discharge node X. Thus, the presence of a keeper transistor increases the switching threshold of the circuit and hence the noise margin.

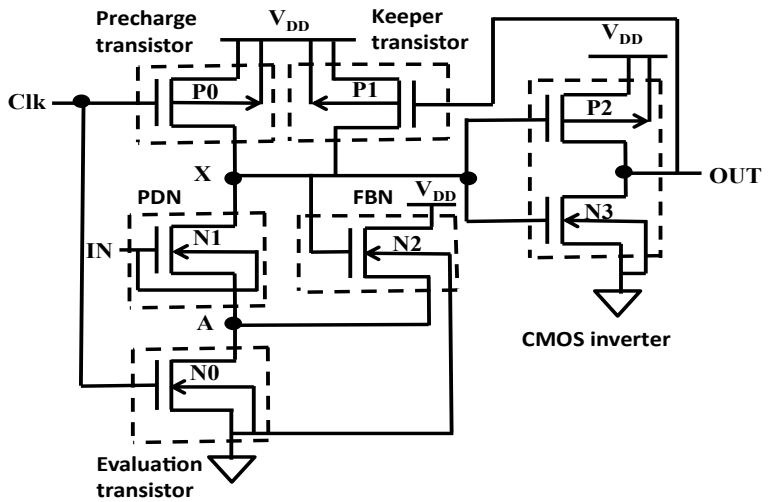


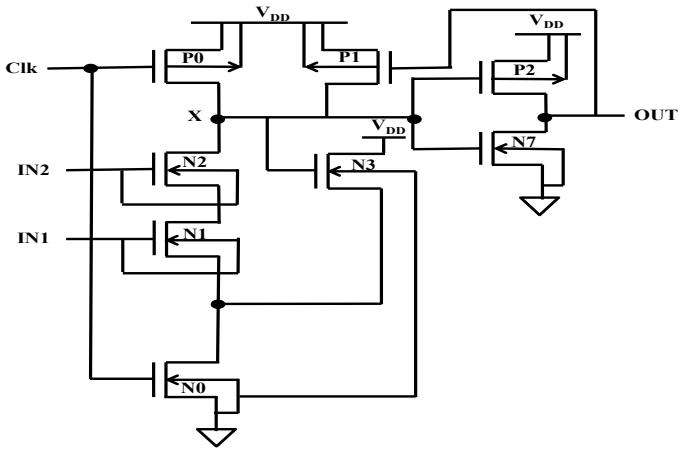
Fig. 5.3 Circuit diagram of the proposed domino ST logic buffer

The proposed domino ST logic style is inherently extensible to complex logic functions because the conventional NMOS transistors in the pull-down network are replaced by DTMOS transistors. The precharge transistor, keeper transistor, FBN, and a CMOS inverter of a domino ST gate remain identical to the proposed domino ST buffer. The DTMOS transistor of a DTMOS ST gate ensures the core advantages of the domino ST buffer, lowering the threshold

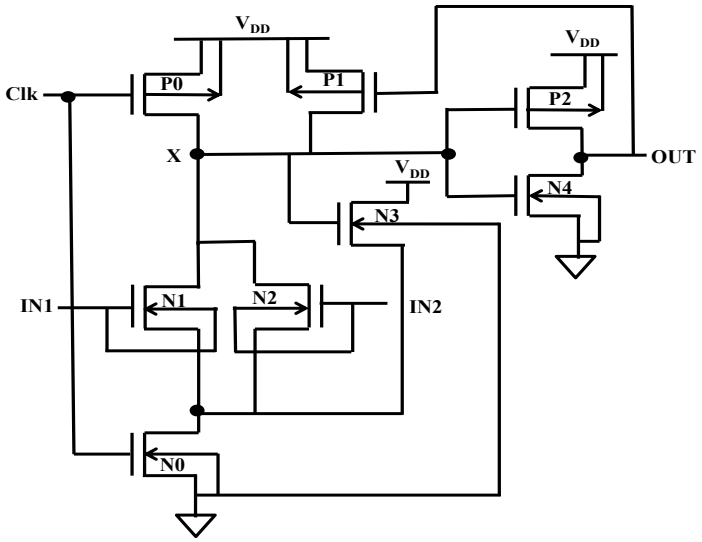
voltage during evaluation for faster discharge and improving noise margins for enhanced noise immunity.

The proposed 2-input domino ST AND2 gate implements the AND2 functionality by employing series-connected DTMOS NMOS transistors N1 and N2 in the PDN as shown in Fig. 5.4 (a). The transistor N2 is controlled by input IN2, which has its drain terminal at dynamic node X and source terminal at the drain terminal of N1. The transistor N1 is controlled by input IN1, which has its drain terminal at the source terminal of N2 and source terminal at the drain of the evaluation transistor N0. During the precharge phase (Clk = 0), the precharge transistor P0 is ON and the evaluation transistor N0 is OFF such that dynamic node X gets precharged to V_{DD} due to the formation of a conducting path from V_{DD}. This further produces a low output at the domino output node OUT of the proposed 2-input domino ST AND2 gate. However, during the evaluation phase (Clk = 1), transistors N1 and N2 must turn ON simultaneously to discharge the dynamic node X by activating the series conduction path. Despite the presence of series resistance, dynamic threshold voltage reduction in DTMOS enables faster switching. All other elements, such as keeper transistor P1 and feedback transistor N3 provide the same benefits as offered for the proposed domino ST logic buffer. This configuration preserves the full noise-tolerance benefits of hysteresis and feedback while benefiting from DTMOS speed in the critical discharge path.

The proposed 2-input domino ST OR2 gate modifies the PDN to realize OR2 logic through parallel-connected DTMOS NMOS transistors N1 and N2 as shown in Fig. 5.4 (b). Transistors N1 and N2 are connected by inputs IN1 and IN2, and their drain terminals are directly connected at the dynamic node X and source terminals at the drain of the evaluation transistor, forming low-resistance parallel branches. During the precharge phase (Clk=0), the precharge transistor P0 is ON and the evaluation transistor N0 is OFF such that dynamic node X gets precharged to V_{DD} due to the formation of a conducting path from V_{DD}. This further produces a low output at the output node OUT of the proposed 2-input domino ST OR2 gate. During the evaluation phase (Clk=1), the discharge at dynamic node X occurs if IN1 or IN2 (or both) are at high voltage level. The role of the keeper transistor P1 and feedback transistor N3 remain identical to the proposed domino buffer.



(a)



(b)

Fig. 5.4 Proposed domino ST logic gates (a) AND2 (b) OR2

5.3.2 Simulation Results

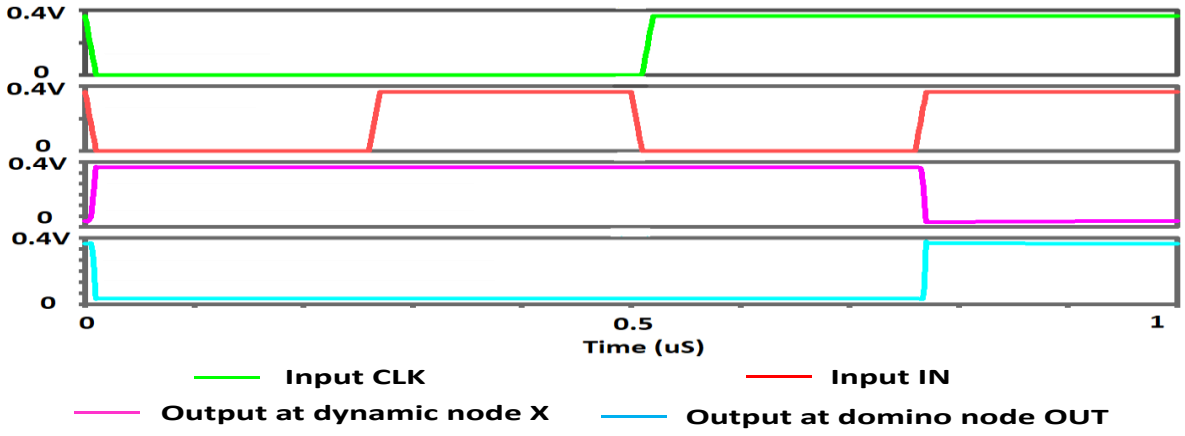
The performance of the proposed domino ST logic buffer is compared with conventional ST, DTMOS ST, VTCMOS ST, conventional domino ST, domino ST1 logic (Fig.2.15 a) [76], and domino ST2 (Fig. 2.15 b) [76] logic buffers, respectively. The performance parameters, such as transistor count, hysteresis width (V_{HW}), propagation delay (τ_d), dynamic power (P_{dyn}), leakage power (P_{leak}), and power delay product (PDP) of ST buffers are measured. An inverter with an NMOS to PMOS width-to-length ratio of 2:3 is connected at the output of conventional ST and DTMOS ST logic inverters to ensure logical equivalence [38]. All the buffers are simulated through LTspice using aspect ratios of the transistors as mentioned in Table 5.1 and 45 nm PTM CMOS technology parameters with a supply voltage and a load capacitance of 0.4 V and 2 fF, respectively. The effect of process variation at different corners and supply voltage on the performance of the buffers is also studied.

I. Functional Verification

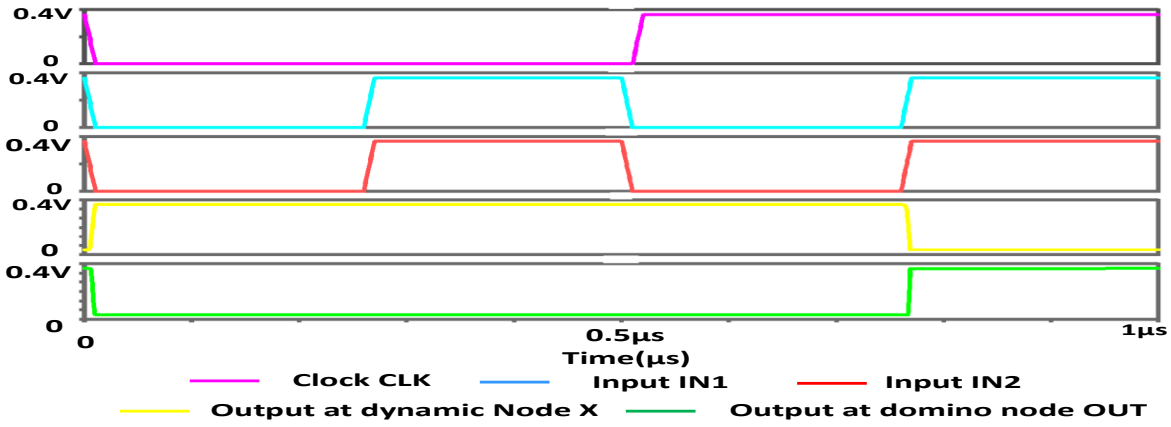
The simulation outputs of the proposed domino ST logic buffer, domino ST AND2 gate and domino ST OR2 gate are shown in Fig. 5.5. It can be observed that during the precharge phase, dynamic node X is precharged to a high logic level (= 0.4 V) and the domino output node OUT is maintained at a low logic level (=0 V). Further, in the evaluation phase, for a low value of IN, the dynamic node X maintains a high logic level while the domino node OUT is at a low logic level. Also, for a high value of IN, the dynamic node X and domino node OUT are maintained at low and high output voltage levels, respectively.

Table 5.1: Aspect ratio of transistors in different ST buffers

Aspect ratio / ST styles	Aspect ratio of NMOS transistors used	Aspect ratio of PMOS transistors used
Conventional ST [26]	N1= 2, N2=2, N3=2	P1=2, P2=8, P3=2
DTMOS ST [37]	N1= 2, N2=2, N3=2	P1=2, P2=8, P3=2
VTCMOS ST [70]	N1=2 , N2=2	P1=8, P2=3
Conventional Domino ST [76]	N0=2, N1=2, N2=2, N3=2, N4=2, N5=2	P0=8, P1=3
Domino ST1[76]	N0=2, N1=2, N2=2, N3=2, N4=2, N5=2	P0=8, P1=1, P2=3
Domino ST2 [76]	N0=2, N1=2, N2=2, N3=2, N4=2	P0=8, P1=1, P2=3
Proposed Domino ST Logic buffer	N0=2, N1=2, N2=2, N3=2	P0=8, P1=1, P2=3



(a)



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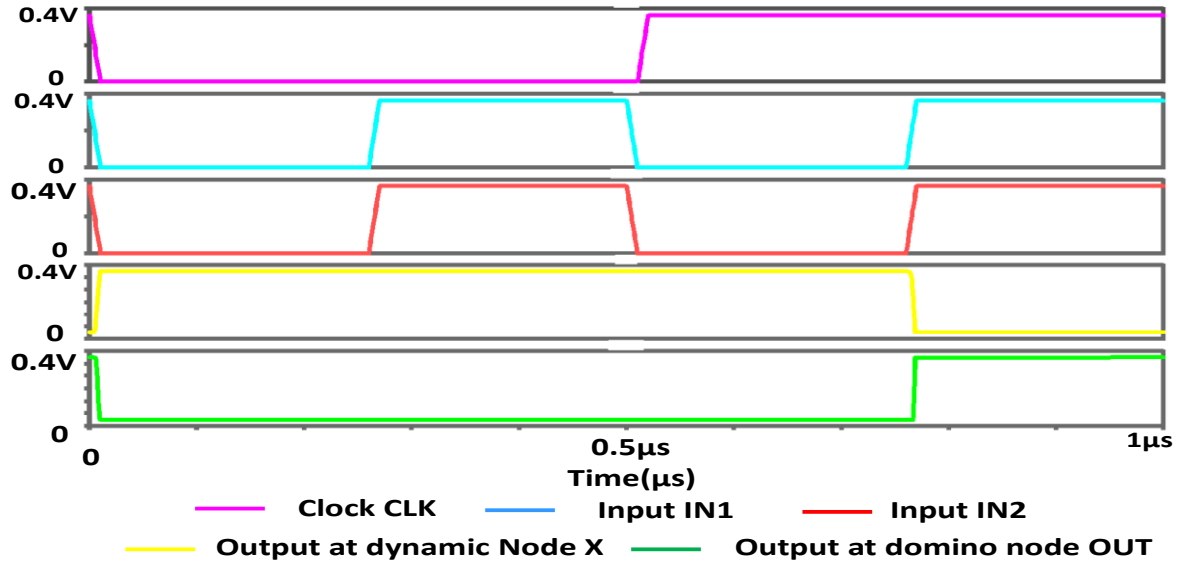


(c)

Fig.5.5 Transient response of the proposed domino ST logic gates (a) Buffer (b) AND2 (c) OR2

Further, for the sake of comparison, the performance parameters of various ST logic styles at different process corners obtained through simulation have been tabulated in Table 5.2

Table 5.2 Performance comparison of ST buffers at different process corners

ST styles / Performance comparison	Conventional ST [26]	DTM OS ST [37]	VTCM OS ST [40]	Conventional Domino ST [76]	Domino ST1 [76]	Domino ST2 [76]	Proposed Domino ST logic
Transistor Count	8	8	6	8	9	8	7
TT Corner							
V_{HW} (mV)	58.4	68.5	93	48.4	48.4	49	161.3
τ_d (ns)	4.97	3.20	2.76	3.53	3.99	3.90	3.26
P_{dyn} (nW)	0.75	1.09	0.62	0.28	0.21	0.44	0.31
PDP (10^{-18} J)	3.70	3.48	1.71	0.98	0.83	1.70	1.01
P_{leak} (nW)	0.37	38.8	39.2	0.28	0.21	0.21	0.28
Area $(um)^2$	5.13	5.26	4.28	4.71	4.92	4.75	3.66
Post layout							
τ_d (ns)	5.2	3.27	2.84	3.60	4.3	3.96	3.28
P_{dyn} (nW)	0.82	1.17	0.68	0.29	0.23	0.46	0.315
FF Corner							
V_{HW} (mV)	58.06	58.31	73.4	38.42	37.9	38	148.4
τ_d (ns)	3.71	2.86	1.92	2.75	2.87	2.80	2.40
P_{dyn} (nW)	0.83	48	0.31	0.65	0.86	0.54	0.29
P_{leak}	1.48	41.2	41.24	1.08	0.87	0.91	1.08

SF Corner							
V_{HW} (mV)	67.43	67.6	90.7	37.2	36.63	37.2	177.1
τ_d (ns)	4.94	3.26	2.35	4.04	4.06	3.99	3.39
P_{dyn} (nW)	1	0.82	0.19	0.02	0.06	0.37	0.15
P_{leak}	1.016	40.6	40	0.652	0.776	0.77	0.64
FS Corner							
V_{HW} (mV)	58	70	93	48	46	54	105
τ_d (ns)	5.69	3.56	1.94	3.99	3.56	3.61	2.92
P_{dyn} (nW)	0.53	1.05	0.10	0.78	0.69	0.65	0.37
P_{leak}	0.70	37	39.2	0.53	0.15	0.19	0.57
SS Corner							
V_{HW} (mV)	67.4	68	111	67.06	57.88	67	161.9
τ_d (ns)	4.62	3.90	3.86	4.62	5.02	5	4.22
P_{dyn} (nW)	0.57	0.07	0.18	0.46	0.43	0.43	0.47
P_{leak}	0.12	37	38	0.11	0.08	0.075	0.10

(T: Typical transistor; F: Fast transistor; S: Slow transistor)

The following observations can be drawn from the simulation results:

- The proposed domino ST logic buffer improves V_{HW} by 176 %, 135 %, 73 %, 233 %, 233 %, and 229 % in comparison to the conventional ST, DTMOS ST, VTCMOS ST, conventional domino ST, domino ST1, and domino ST2 buffers, respectively. The action of the keeper transistor P1 results in a favourable effect on the switching threshold voltage during the transition. In addition to this, the impact of the increase in channel width of the keeper transistor P1 on the V_{HW} for the proposed domino ST logic buffer is analysed, and the results are plotted in Fig. 5.6. It is observed that V_{HW} increases with an increase in the channel width. Also, the increase is more pronounced when dynamic node X takes high to low transition in comparison to the low to high transition.
- It is observed that the proposed domino ST logic buffer has reduced τ_d value by 34 %, 7.6 %, 18.2 %, and 16.4 % in comparison to conventional ST, conventional domino ST, domino ST1, and domino ST2 buffers, respectively. The use of a DTMOS transistor in PDN to realize the logic function results in lowering the propagation delay value. However, the proposed buffer has a higher τ_d value than DTMOS ST and VTCMOS ST buffers, as these static ST buffers dynamically control the threshold voltage of all the transistors in the buffer by using a dynamic and variable threshold voltage technique, in contrast to PDN transistors in the proposed circuit. The effect of technology scaling on τ_d of the proposed and Domino ST buffers, as depicted in Fig. 5.7, reveals a decreasing trend in τ_d with technology scaling.
- The proposed domino ST logic buffer offers P_{dyn} reduction by 58 %, 71.5 %, 50 %, and 29.5 % in comparison to conventional ST, DTMOS ST, VTCMOS ST, and domino ST2 buffers, respectively. It thus consumes lower P_{dyn} than all the existing buffers except the conventional domino ST and domino ST1 buffers. The use of DTMOS transistors in PDN increases the dynamic power marginally in comparison to conventional domino ST and domino ST1 buffers, as their presence increases the driving current during a switching event.
- The proposed domino ST buffer has a lower P_{leak} value by 24.3 %, 99 %, and 99.2 %, in comparison to conventional ST, DTMOS ST, and VTCMOS ST buffers, respectively. However, increase of 33 % and 33 % is observed with reference to domino ST1 and domino ST2 buffers due to leakage through feedback transistor N2.

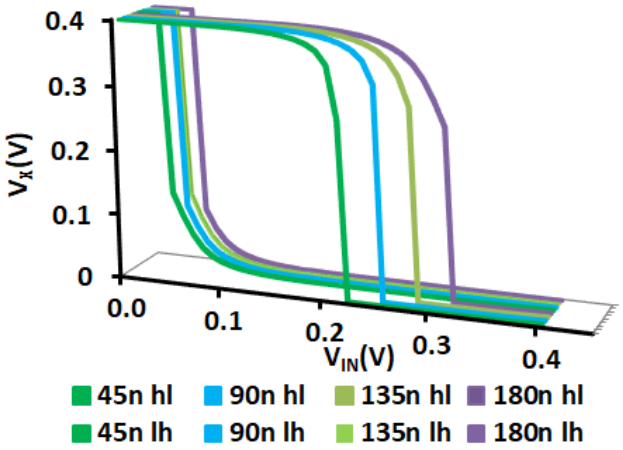


Fig. 5.6 Effect of channel width of keeper transistor P1 on V_{HW} in the proposed domino ST logic buffer

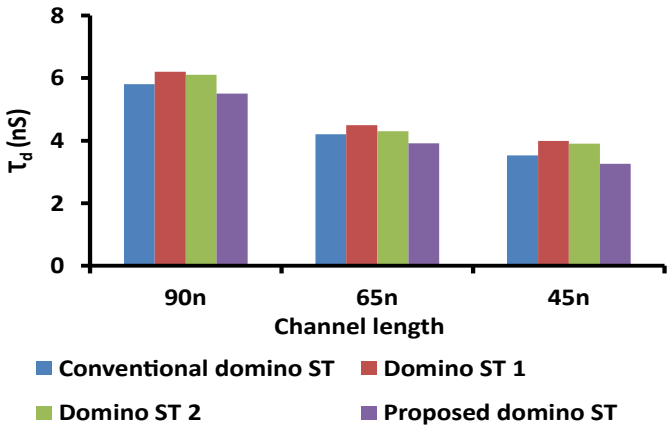


Fig. 5.7 Effect of technology scaling on τ_d of domino ST logic buffers

- The simulation results for PDP indicate that the proposed domino ST logic buffer provides a PDP value lower than all except for conventional domino ST and domino ST1 buffers due to a dominant reduction in their power consumption.

- The layout of all the buffers is drawn and the layout of the proposed domino ST logic buffer is shown in Fig. 5.8. The results indicate a low area requirement by the proposed domino ST logic buffer by 28 %, 30.4 %, 14.5 %, 22.2 %, 25.6 % and 23 % in comparison to conventional ST, DTMOS ST, VTCMOS ST, conventional domino ST, domino ST1 and domino ST2 logic buffers, respectively. This reduction is attributed to the low transistor count in the proposed domino ST logic buffer. The post layout simulation results show that τ_d and P_{dyn} increase due to increase in extracted parasitic capacitances. So, design rules are followed to minimize the extracted parasitic capacitances as far as possible.

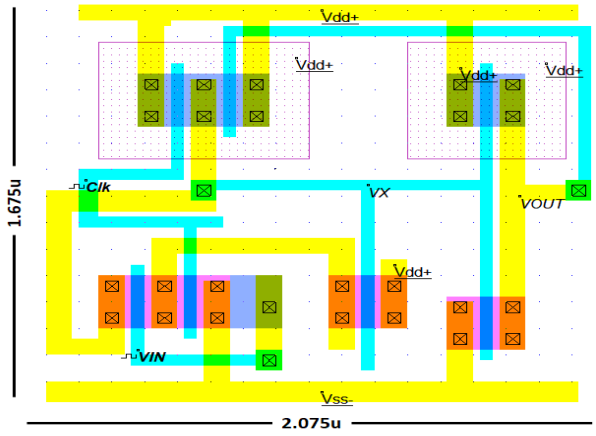
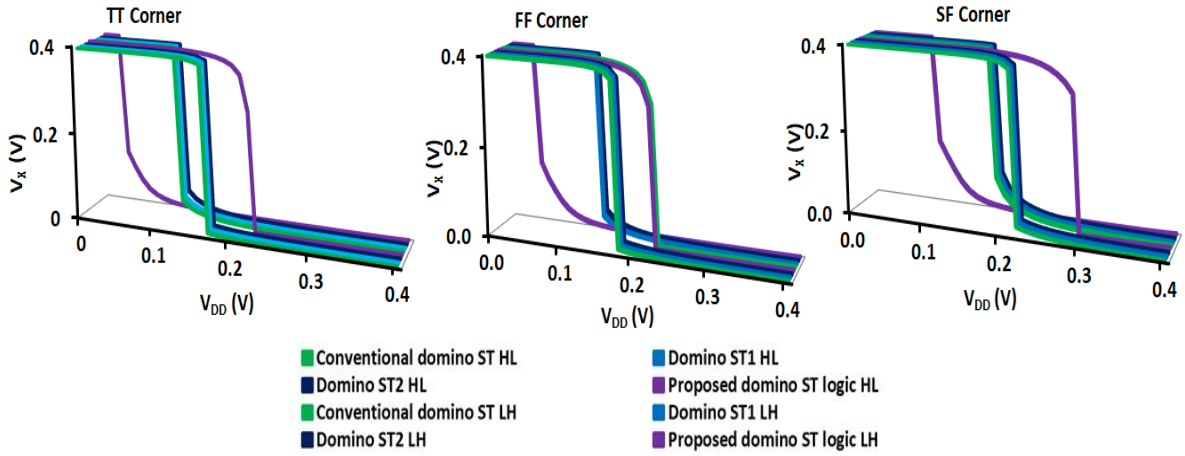


Fig. 5.8 Layout of the proposed domino ST logic buffer

The impact of process variations at different design corners (TT, FF, SF, FS, and SS; TT: Typical NMOS, Typical PMOS; FF: Fast NMOS, Fast PMOS; SF: Slow NMOS, Fast PMOS, FS: Fast NMOS, Slow PMOS, SF; Slow NMOS, Fast PMOS) is studied, and the results are appended in Table 5.2. The VTC of domino ST logic buffers is shown in Fig. 5.9. From process corner analysis, it is observed that the proposed domino ST logic buffer achieves the highest V_{HW} at all corners, maintaining the same trend as in a typical corner. In FF and FS corners, it provides the lowest τ_d among all buffers except the VTCMOS ST buffer, and in the SS and SF corners, it achieves the lowest value except the DTMOS ST and VTCMOS ST buffers. The proposed domino ST buffer demonstrates the lowest P_{dyn} at the FF corner and is lower than all except conventional domino ST and domino ST1 buffers in the SF corner, DTMOS ST and VTCMOS ST in the FS corner, and DTMOS ST and VTCMOS ST in the SS corner. Furthermore, the SF corner provides the lowest P_{leak}, while the FF and FS corners have lower P_{leak} than all except conventional domino ST, domino ST1, and domino ST2 buffers. It is surpassed only by domino ST1 and domino ST2 buffers in the SS corner. Overall, the proposed domino ST logic buffer shows the same performance trend as the typical corner without performance deviation.



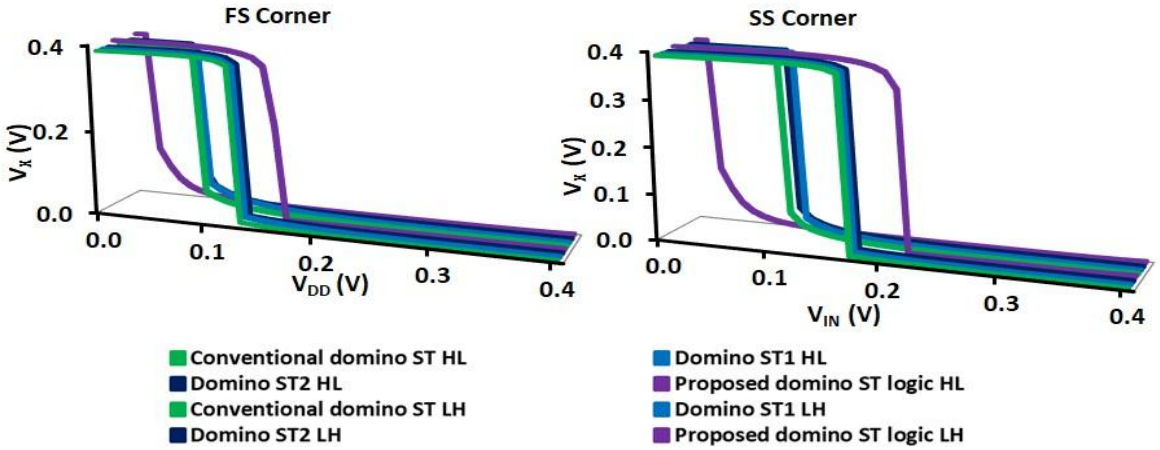


Fig. 5.9 VTC of domino ST logic buffers

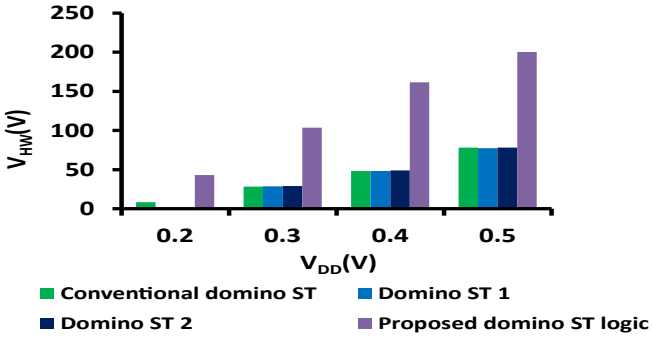
The performance of the proposed domino ST AND2 and OR2 gates is compared with conventional domino ST, domino ST1 [76], and domino ST2 [76] AND2 and OR2 gates, respectively. The performance parameters such as V_{HW}, τ_d, P_{dyn}, P_{leak}, and PDP of ST gates are measured. All the gates are simulated in LTspice using 45nm PTM CMOS technology parameters with a supply voltage and a load capacitance of 0.4 V and 2 fF, respectively. It is observed that the proposed domino ST AND2 gate increases V_{HW} by 238 %, 239 %, and 234 % in comparison to conventional domino ST, domino ST1, and domino ST2 AND2 gates, respectively. It remains approximately the same with the domino ST buffers due to feedback and the keeper transistors are unchanged in domino ST AND2 and OR2 gates. The τ_d of the proposed domino ST AND2 gate decreases by 10 %, 19 %, and 17.3 % in comparison to conventional domino ST, domino ST1, and domino ST2 AND2 gates due to the use of a DTMOS transistor in the PDN of the proposed domino ST AND2 gate. The P_{dyn} of the proposed domino ST gate decreases by 28 % with respect to the domino ST2 AND2 gate and increases by 13.7 % and 50 % in comparison to conventional ST and domino ST1 AND2 gates. The proposed domino ST AND2 gate increases leakage power by 3.8 %, 42 %, and 50 % in comparison to conventional domino ST, domino ST1, and domino ST2 AND2 gates due to the use of DTMOS transistor in the PDN of the proposed domino ST gate. Further, the proposed domino ST OR2 gate increases V_{HW} by 226 %, 219 %, and 213 % in comparison to conventional domino ST, domino ST1, and domino ST2 OR2 gates, respectively. The τ_d of the proposed domino ST OR2 gate decreases by 2.5 %, 15 %, and 14.5 % in comparison to conventional domino ST, domino ST1, and domino ST2 OR2 gates, respectively. The proposed domino ST OR2 gate has lower τ_d than the proposed domino ST AND2 gate due to the parallel combination of transistors in the PDN of the domino ST OR2 gate, which decreases the overall resistance. The P_{dyn} of the proposed domino ST OR2 gate decreases by 29 % with respect to the domino ST2 OR2 gate and increases by 9.6 % and 47.8 % in comparison to the conventional domino ST and domino ST1 OR2 gates, respectively. The P_{leak} of the proposed domino ST OR2 gate increases by 3.4 %, 36 %, and 42.8 %, in comparison to conventional domino ST, domino ST1, and domino ST2 OR2 gates, respectively. The proposed domino ST AND2 and OR2 gates provide significant improvement in noise immunity and speed over existing domino ST gates at the cost of increase in the leakage power.

Table 5.3: Performance comparison of ST AND2 and OR2 gates

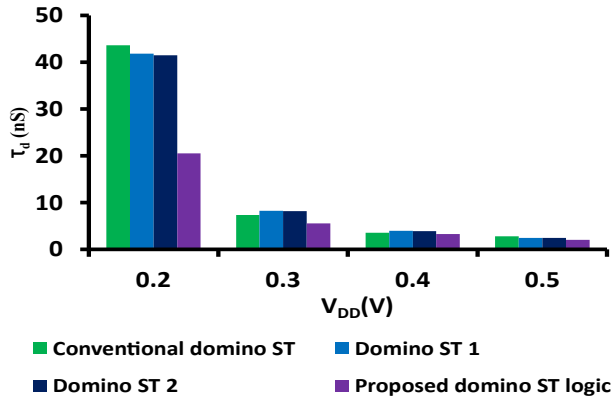
ST styles / Performance comparison	Conventional Domino ST [76]	Domino ST1 [76]	Domino ST2 [76]	Proposed Domino ST logic
	AND2			
V_{HW} (mV)	47	46.90	47.50	159
τ_d (ns)	3.88	4.30	4.21	3.48
P_{dyn} (nW)	0.29	0.22	0.46	0.33
PDP (10^{-18} J)	1.13	0.94	1.93	1.15
P_{leak} (nW)	0.26	0.19	0.18	0.27
	OR2			
V_{HW} (mV)	50	51	52	163
τ_d (ns)	3.14	3.63	3.58	3.06
P_{dyn} (nW)	0.31	0.23	0.48	0.34
PDP (10^{-18} J)	.97	.83	1.72	1.04
P_{leak} (nW)	0.29	0.22	0.21	0.30

II. Effect of Supply Voltage Variation

Fig. 5.10 represents the effect of supply voltage variations on V_{HW}, τ_d, P_{dyn}, and P_{leak}. The decrease in supply voltage leads to a decrease in V_{HW}, P_{dyn}, and P_{leak}, while τ_d increases.



(a)



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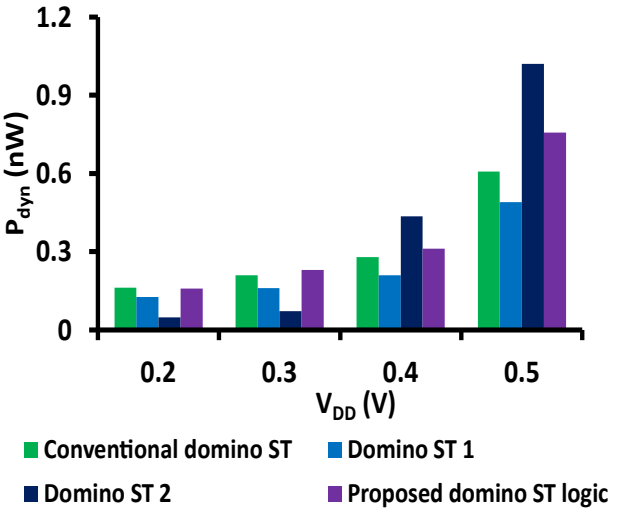

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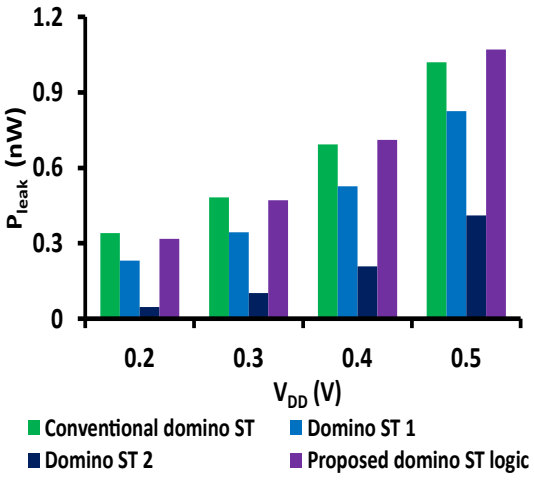


(d)

Fig 5.10 Effect of variations in supply voltage on domino ST logic buffers (a)V_{HW} (b) τ_d (c) P_{dyn} (d) P_{leak}

5.4 Design Example using Proposed Domino ST Logic Style

A 4:1 MUX is taken as a design example. The block diagram of 4:1 domino MUX is shown in Fig. 5.11. The S0, S1 and Clk are the select lines and clock signal of the domino MUX. The design of 4:1 conventional domino ST, domino ST1, domino ST2, and proposed domino ST MUXs is shown in Fig. 5.12. The design employs two 2:1 ST MUXs in the first stage, which is followed by one 2:1 ST MUX in the second stage. The MUXs are simulated and the results of different performance parameters are listed in Table 5.4. All the MUXs are simulated in LTspice using 45 nm PTM CMOS technology parameters with a supply voltage and a load capacitance of 0.4 V and 2 fF, respectively. The proposed domino ST logic MUX improves V_{HW} by 230 %, 226 %, and 217 % in comparison to the conventional domino ST, domino ST1, and domino ST2 MUXs, respectively, due to the keeper transistors in the proposed MUX. It is observed that the proposed domino ST logic MUX has reduced the τ_d value by 3 %, 16 %, and 13.6 % in comparison to conventional domino ST, domino ST1, and domino ST2 MUXs, respectively, due to the use of a DTMOS transistor in the PDN of the proposed MUX. The proposed domino ST logic MUX offers P_{dyn} reduction by 25% in comparison to the domino ST2 MUX. Thus, it consumes lower P_{dyn} except for the conventional domino ST and domino ST1 MUXs. Further, the simulation results indicate that the proposed domino ST logic MUX reduces the PDP value by 35.2 % in comparison to the domino ST2 MUX, except for conventional domino ST and domino ST1 MUXs. The P_{leak} of the proposed domino ST MUX increases by 1.4 %, 30.7 % and 36 % in comparison to the conventional domino ST, domino ST1, and domino ST2 MUXs, respectively. Hence, the proposed domino ST MUX is most suitable for high immunity and speed at the cost of increase in the leakage power.

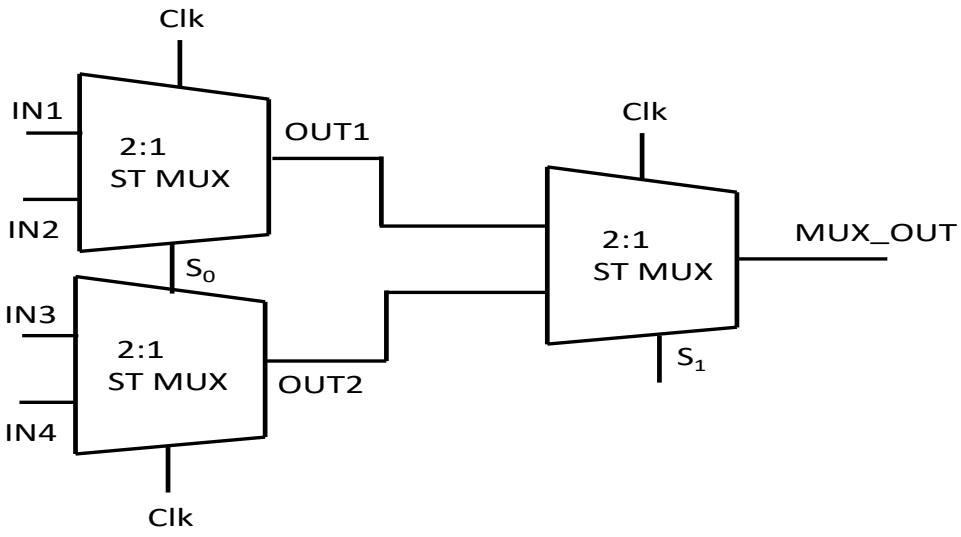
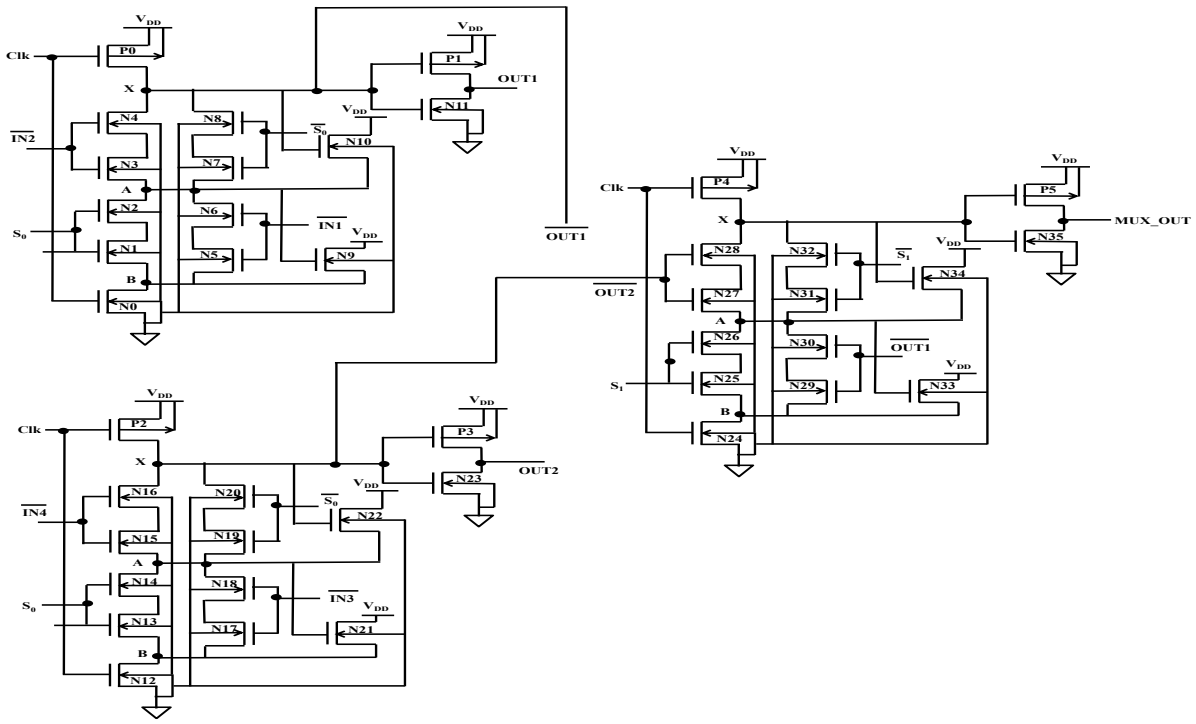
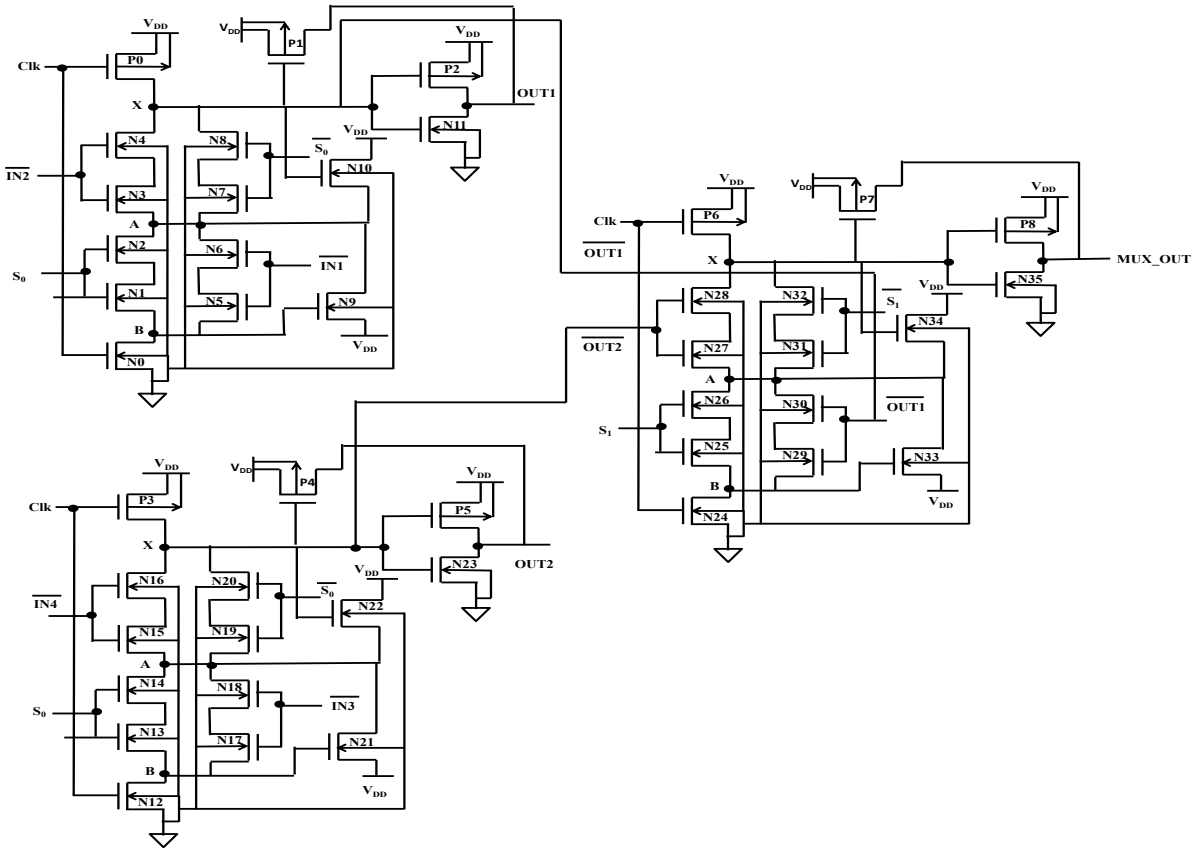


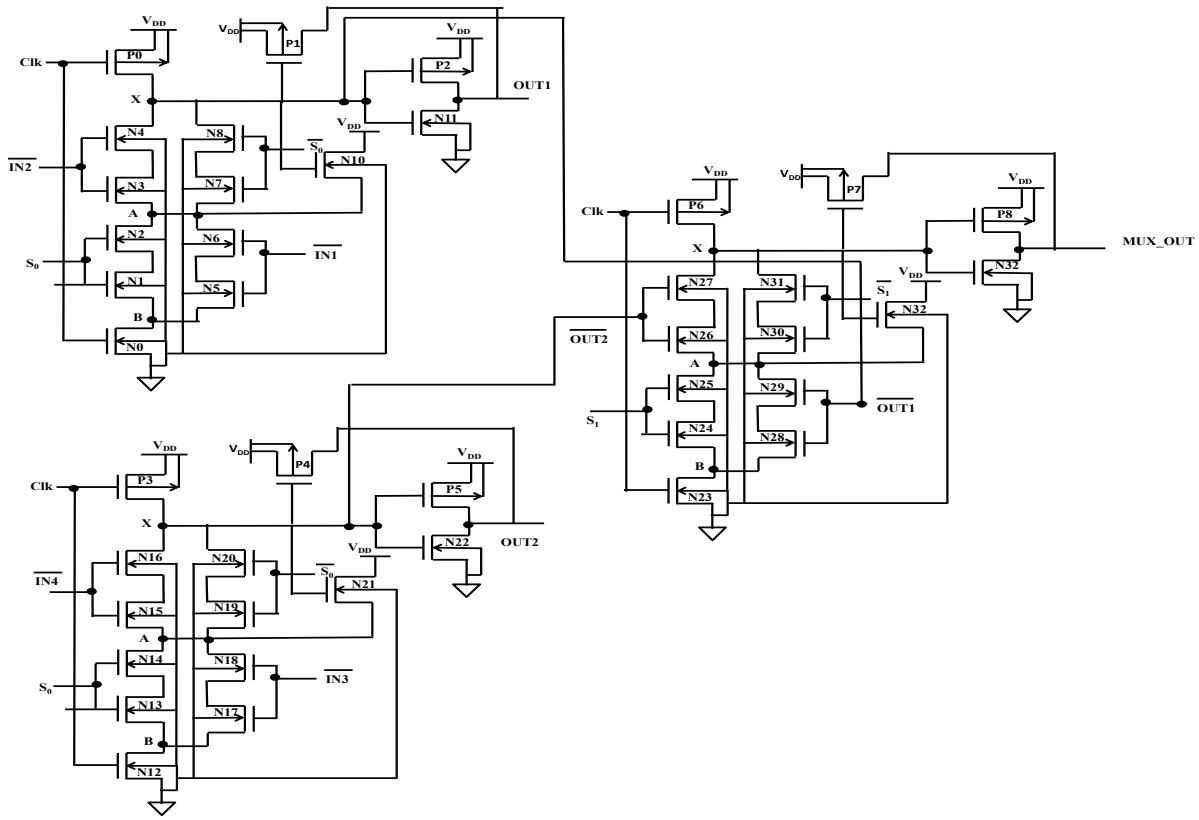
Fig. 5.11 Block diagram of 4:1 domino MUX


Clk
IN2
S0
IN4
S1
MUX_OUT
OUT1
OUT2
X
A
B
VDD
P0
P1
P2
P3
P4
P5
P6
P7
P8
N0
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
N12
N13
N14
N15
N16
N17
N18
N19
N20
N21
N22
N23
N24
N25
N26
N27
N28
N29
N30
N31
N32
N33
N34
N35
IN1
IN3

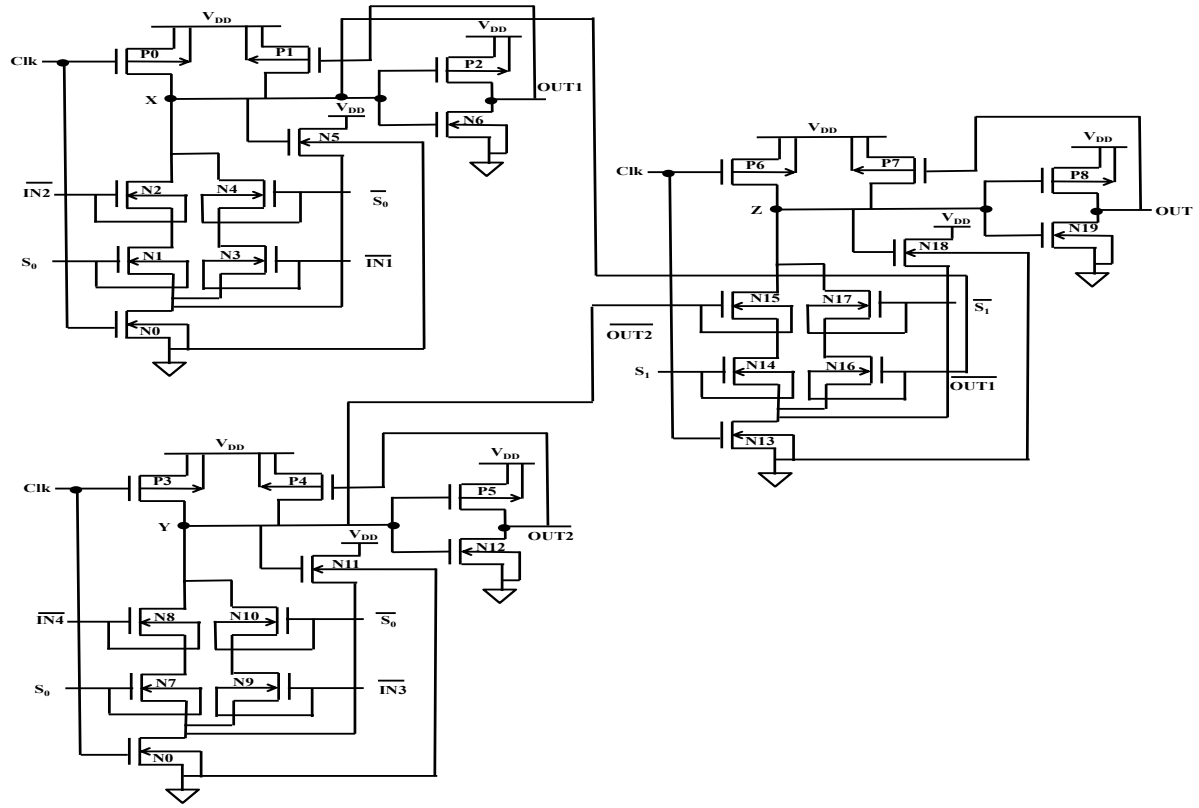
(a)


Clk
IN2
S0
IN4
S1
MUX_OUT
OUT1
OUT2
X
A
B
VDD
P0
P1
P2
P3
P4
P5
P6
P7
P8
N0
N1
N2
N3
N4
N5
N6
N7
N8
N9
N10
N11
N12
N13
N14
N15
N16
N17
N18
N19
N20
N21
N22
N23
N24
N25
N26
N27
N28
N29
N30
N31
N32
N33
N34
N35
IN1
IN3

(b)


Clk
P0
P1
P2
OUT1
X
N4
N8
N11
N10
N3
N7
A
N2
N6
N1
N5
B
N0
P3
P4
P5
N16
N20
N22
N21
N15
N19
N14
N18
N13
N17
N12
OUT2
P6
P7
P8
MUX_OUT
N27
N31
N32
N26
N30
N25
N29
N24
N28
N23
OUT1

(c)


Clk
P0
P1
P2
OUT1
X
N5
N6
N2
N4
N1
N3
N0
P3
P4
P5
Y
N11
N12
OUT2
N8
N10
N7
N9
P6
P7
P8
OUT
Z
N18
N19
N15
N17
N14
N16
N13
OUT2
OUT1

(d)

Fig. 5.12 Realization of 4:1 domino ST MUXs in different styles (a) Conventional (b) Domino ST1 (c) Domino ST2 (d) Proposed domino ST

Table 5.4 Performance comparison of 4:1 domino ST MUXs

ST styles / Performance comparison	Conventional Domino ST [76]	Domino ST1 [76]	Domino ST2 [76]	Proposed Domino ST logic
V_{HW} (mV)	50	50.5	52	165
τ_d (ns)	6.5	7.5	7.3	6.3
P_{dyn} (nW)	0.8	0.6	1.2	0.9
PDP (10^{-18} J)	5.2	4.5	8.76	5.67
P_{leak} (nW)	.67	.52	.50	.68

5.5 Conclusion

This chapter focus on the domino ST logic style, which works on the principle of precharge and evaluate logic. The proposed domino ST logic incorporates two stages, wherein the first stage implements the logic function using dynamic threshold MOS transistors and and the second stage employs a CMOS inverter. A modified keeper and feedback transistors are employed improved performance. Different domino ST logic gates based on the proposed domino ST logic style are designed and simulated using CMOS PTM 45 nm technology node parameters. It is observed from the simulation results that the proposed domino ST logic buffer provides maximum reduction in propagation delay by 18.2 %, and maximum increase in hysteresis width by 233 % in comparison to domino ST1 and conventional domino ST buffers, respectively. Overall, the proposed domino ST logic buffer provides the highest speed and noise immunity among all the buffers. The proposed domino ST logic buffer also has the lowest area in comparison to existing ST logic buffers. The proposed domino ST AND2, OR2 and 4:1 ST MUXs provide significant improvement in the noise immunity and speed among all the existing domino ST gates at increase in the leakage power. Further, the reliability of the proposed domino ST gates is verified by process corner and voltage variation analysis, which confirms the effectiveness of the proposed styles among all design styles. The improved domino ST logic gate is applicable for noise immune and high speed dynamic circuit design applications.

Chapter 6:

CNTFET Based Schmitt Trigger Logic Gates

6.1 Introduction

The conventional design of ST gates is primarily based on planar silicon MOSFET technology. To achieve higher integration density and improved circuit performance, continuous scaling of MOSFET dimensions has been pursued in accordance with Moore's Law. However, as device dimensions shrink into the nanometer regime, several critical challenges emerge, including severe short-channel effects, increased leakage currents, and mobility degradation. These non-idealities adversely impact circuit performance and reliability, thereby limiting the scalability of traditional ST gate designs. Consequently, there is a growing need to explore alternative device technologies for ST gates. In this context, carbon nanotube field-effect transistors (CNTFETs) have gained significant attention as a promising replacement for conventional MOSFETs owing to their high carrier mobility, near-ballistic transport, and superior current driving capability [78-82]. CNTFETs have been widely investigated across various application domains such as nanoelectronics, high-performance computing, low-power digital circuits, and biomedical implantable devices. Therefore, this chapter examines the implementation of ST gates using CNTFET technology. The previously proposed three-stage Schmitt trigger (TS ST) logic is extended by incorporating CNTFETs. The objective is to exploit the excellent transport properties of CNTFETs at the 32 nm node to achieve better hysteresis characteristics, reduced propagation delay, and lower dynamic power compared to the MOSFET-based TS ST design.

6.2 CNTFET Preliminaries

Carbon nanotubes (CNTs) are extremely fine and distinctive structures that offer notable advantages over many other nanomaterials, due to their exceptional mechanical, electrical, and chemical characteristics. When a graphene sheet is rolled at a specific angle, it forms a carbon nanotube. The direction and manner in which the graphene sheet is rolled, a single-walled CNT (SWCNT) can show either metallic or semiconducting behaviour. This distinct feature is characterized by the chirality vector, denoted by an integer pair (m, n), known as the chiral vector. A CNT acts as a metal when n = m or n – m = 3i**,** where *i* is an integer; otherwise, it functions as a semiconductor [78-79].

A carbon nanotube field effect transistor (CNTFET) is a device that consists of parallel semiconducting CNTs which are either grown or transferred onto a substrate. A typical device configuration of a MOSFET-like carbon nanotube FET (CNTFET), comprising the drain, gate, source, and substrate, is illustrated in Fig. 6.1 [80]. The CNTs are placed in the channel region, which remains undoped, while the two adjoining regions are heavily doped to form the source and drain extensions and/or interconnects between neighbouring devices. The gate voltage modulates the conductivity of the undoped channel. The CNTFETs enable ballistic or near-ballistic transport under low voltage bias due to the remarkably long mean free path (around 1 μm) for elastic scattering.

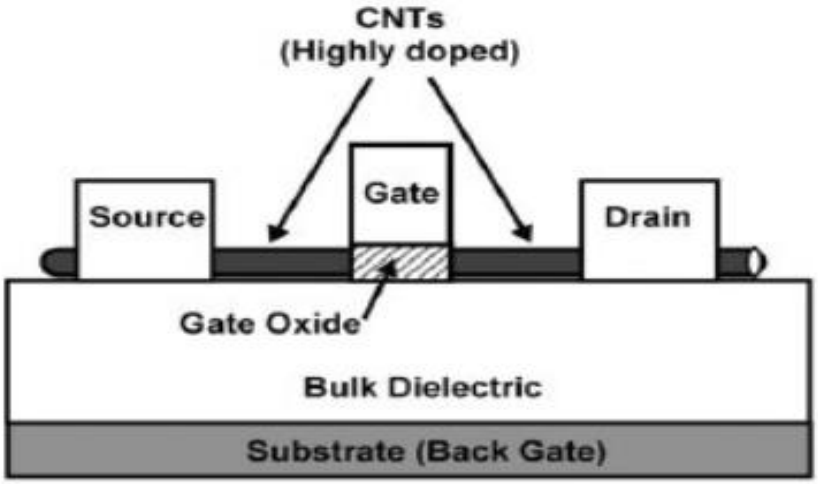


Fig. 6.1 CNTFET Structure [80]

The operational behaviour of both p-type FET and n-type FET is largely similar. The diameter of a carbon nanotube (CNT), denoted as D_{CNT} is a fundamental parameter in CNTFET design and is given by:

$$D_{CNT} = \frac{Ch}{\pi} \tag{6.1}$$

where Ch represents the chirality vector, which is a key device-level parameter. Chirality defines the manner in which a graphene sheet is rolled to form a cylindrical carbon nanotube. It is expressed as:

$$Ch = a\sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{6.2}$$

where a = 0.249 nm is the lattice constant, and n_1 and n_2 are integers that determine the structure of the CNT. Furthermore, the threshold voltage of a CNTFET is inversely proportional to the diameter of the nanotube and is given by [81]:

$$V_{th} = \frac{0.42}{D_{CNT}} \tag{6.3}$$

Thus, chirality indirectly influences the threshold voltage through its effect on the CNT diameter, making it a critical parameter in CNTFET design.

6.3 Proposed CNTFET Three-stage ST Logic Style

The proposed CNTFET three-stage ST logic style **(**CNTFET TS ST logic style) is designed by replacing the MOSFET transistors in the TS ST logic style previously introduced in Chapter 3 with CNTFETs. The proposed CNTFET TS ST logic style employs three stages and a feedback

connection. It implements the required functionality in the first stage, which is then followed by two inverter stages. The output of the third stage is fed back to the first stage.

6.3.1 Operation and Analysis

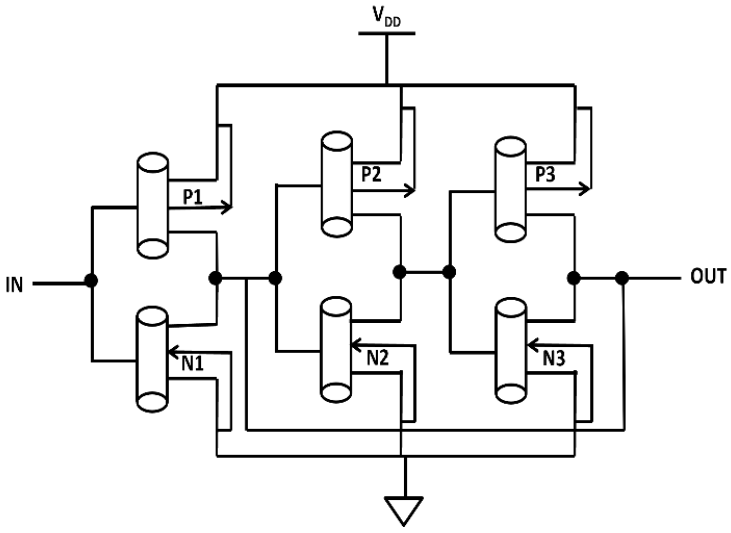
The complete schematic of the proposed CNTFET TS ST logic inverter is shown in Fig. 6.2. The first stage of the proposed CNTFET TS ST logic inverter comprises of a PDN with transistor N1 and a PUN with transistor P1. It is then followed by two CNTFET inverters (N2, P2) and (N3, P3) with a feedback connection from the output node (OUT) to the first stage output to introduce hysteresis in the circuit. The operation of the novel CNTFET TS ST inverter for different input combinations can be explained as:

Case I: When the input is at a low logic level:

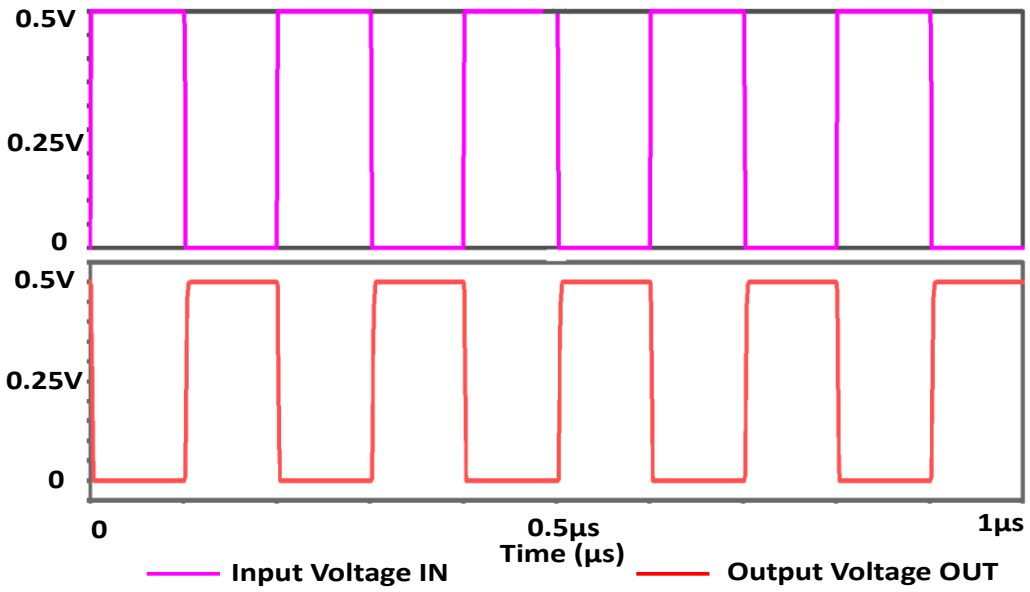
In the PUN, transistor P1 conducts, while in the PDN, transistor N1 is OFF. In this condition, the node OUT is charged through the current path established from the supply voltage to node OUT so that a low voltage level is obtained at the output of the second inverter.

Case II: When the input is at the high logic level:

In this case, the transistor N1 is ON while the transistor P1 is OFF. This condition in the PDN allows a current path to be formed between the node OUT and GND. Further, in the PUN, the transistor P1 does not conduct, and the node OUT is discharged to a low potential. Thus, the output of the second inverter acquires a high voltage level. The functionality of the novel CNTFET TS ST inverter has been verified and is represented in Fig.6.2 (b).



(a)



(b)

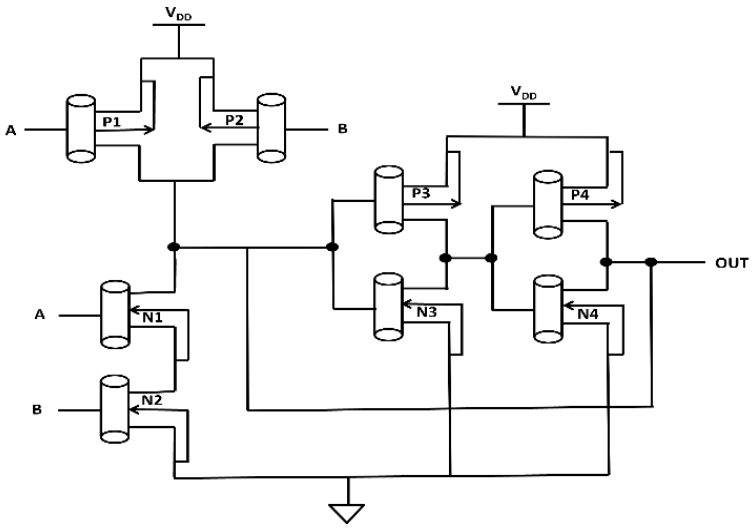
Fig. 6.2 Schematic of inverter (a) Proposed CNTFET TS ST (b) Transient response

The proposed CNTFET TS ST logic gate topology can be extended to realize multi-input logic functions such as NAND2/AND2, NOR2/OR2, XOR2/XNOR2 by modifying the first-stage PUN and PDN and retaining the cascaded three-inverter ST feedback structure. This approach ensures that hysteresis width advantage along with improvements in speed and power consumption.

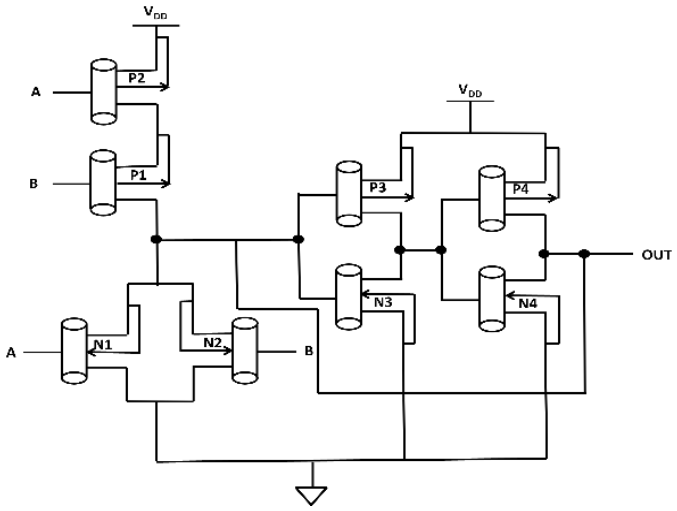
The scheme for realizing two input gates in the CNTFET TS ST logic style requires replacing the transistors N1 and P1 in the proposed CNTFET TS ST logic inverter with their corresponding PDN and PUN in the first stage inverter. The schematics of the two-input CNTFET TS ST NAND2, NOR2, and XOR2 logic gates are presented in Fig. 6.3. In the proposed CNTFET TS ST NAND2 gate (Fig. 6.3 (a)), the inputs A and B drive the series-connected transistor pairs (N1, N2) in the PDN, while they drive two parallel transistors (P1, P2) in the PUN. This is followed by the two stages as in the TS ST inverter.

The inputs A and B in the proposed CNTFET TS ST NOR2 gate (Fig. 6.3(b)) drive the parallel-connected transistors (N1, N2) in the PDN and two series transistors (P1, P2) in the PUN of the first stage. This is followed by two stages, with the output of the third stage being feedback to obtain hysteresis.

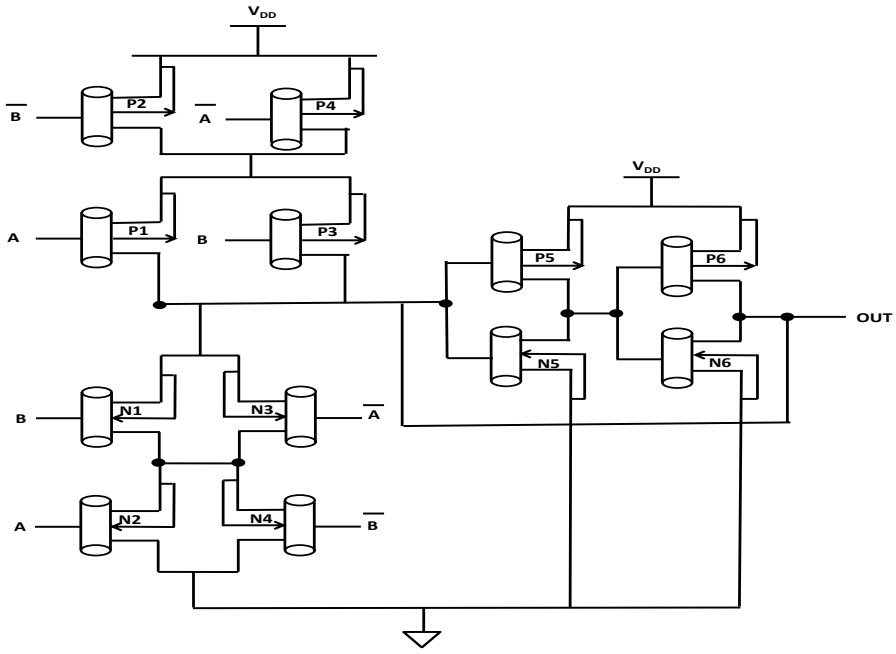
The inputs A and B in the proposed CNTFET TS ST XOR2 gate (Fig. 6.3(c)) drive the series-connected parallel transistor pairs (N1, N3) and (N2, N4) in the PDN and series-connected parallel transistor pairs (P1, P3) and (P2, P4) in the PUN of the first stage. This is followed by the two stages, with the output of the third stage being feedback to obtain hysteresis.


V_{DD}
A
P1
P2
B
V_{DD}
P3
P4
OUT
A
N1
N3
N4
B
N2

(a)


V_{DD}
A
P2
V_{DD}
B
P1
P3
P4
OUT
N3
N4
A
N1
N2
B

(b)



(c)

Fig.6.3 Schematic of the proposed CNTFET TS ST logic gates (a) NAND2 (b) NOR2 (c) XOR2

6.3.2 Simulation Results:

The performance of the proposed CNTFET TS ST logic gates is compared with the existing MOSFET-based TS ST logic counterparts. The performance parameters such as hysteresis width (V_{HW}), propagation delay (τ_d), and power dissipation (P_{dyn}) and power delay product (PDP) are considered. The TS ST logic gates are simulated using 32 nm PTM CMOS technology parameters, and the CNTFET TS ST logic gates are simulated using 32 nm CNTFET technology parameters with a supply voltage and load capacitance of 0.5 V and 10 fF, respectively. The simulation results are summarized in Table 6.1. It is observed that the CNTFET TS ST inverter obtains better V_{HW} by 19 % in comparison to the TS ST inverter. This happens because the threshold voltage of CNTFETs is tunable by choosing an optimum value of CNT diameter/chirality. In a three-stage structure, each CNTFET stage produces stronger regenerative feedback than silicon devices. Further, the CNTFET TS ST inverter decreases τ_d and P_{dyn} by 11 % and 12.5 %, respectively, in comparison to the TS ST inverter because CNTFET has higher carrier mobility and lower parasitic capacitances than Si-devices.

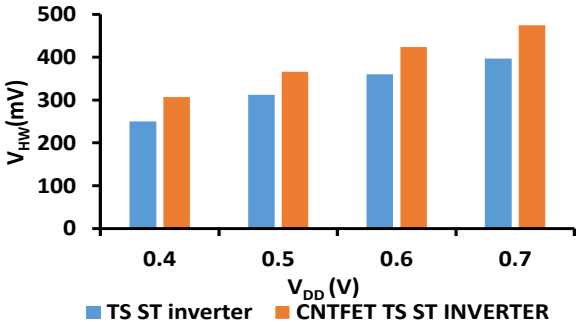
The effect of voltage variation on the performance of all the inverters is also studied and shown in Fig. 6.4. A decreasing trend in V_{HW} and V_{dyn} is observed with decrease in supply voltages. Further, it is observed that the τ_d increases with the corresponding decrease in supply voltage.

The CNTFET TS ST inverter maintains a consistent performance due to its unique one-dimensional material properties and near-ballistic transport behaviour over the MOSFET-based design for the process corner analysis (FF, TT, and SS). The CNTFET TS-ST inverter improves V_{HW} by 18 % and 20 %, reduces τ_d by 9 % and 11.4 %, and lowers P_{dyn} by 13 % and 10.6 % across FF and SS corners, respectively, compared to its MOSFET counterpart. Particularly, even in the worst-case SS corner, the CNTFET version exhibits better robustness in V_{HW} and τ_d, demonstrating superior immunity to process variations.

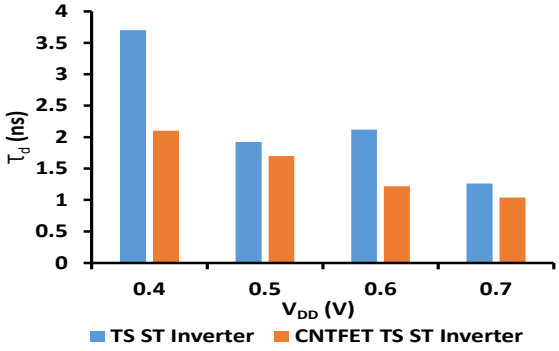
Table 6.1: Performance comparison of the TS ST and proposed CNTFET TS ST logic inverters

ST gates / Performance comparison	TS ST inverter	Proposed CNTFET TS ST inverter
TT		
V_{HW} (mV)	309	368.6
τ_d (ns)	1.92	1.70
P_{dyn} (nW)	8.10	7.2
PDP (10^{-18} J)	15.55	12.24
FF		
V_{HW} (mV)	335	395
τ_d (ns)	1.55	1.41
P_{dyn} (nW)	9.2	8
PDP (10^{-18} J)	14.26	11.28
SS		
V_{HW} (mV)	285	342
τ_d (ns)	2.80	2.48
P_{dyn} (nW)	7.5	6.7
PDP (10^{-18} J)	21	16.61

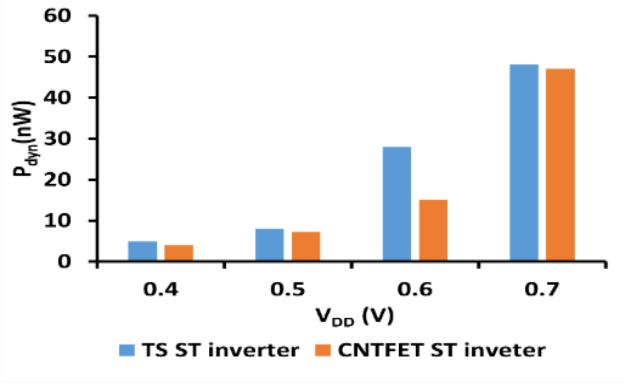
T: Typical, F: Fast, S: Slow



(a)



(b)



(c)

Fig. 6.4 Effect of voltage variations on performance parameters of TS ST and proposed CNTFET TS ST logic inverters

The performance of the proposed CNTFET TS ST NAND2 and NOR2 gates is further compared with the existing MOSFET-based TS ST NAND2 and NOR2 gates. The performance parameters such as V_{HW}, τ_d, and P_{dyn} are considered. The same simulation conditions as taken for the inverter are considered. The simulation results are summarized in Table 6.2. The CNTFET TS ST NAND2 gate has better V_{HW} than the TS ST NAND2 gate. The CNTFET TS ST NAND2 gate increases V_{HW} by 19.5 % in comparison to the TS ST NAND2 gate. In addition, the CNTFET TS ST NAND2 gate decreases τ_d and P_{dyn} by 13 % and 12.6 %, respectively, in comparison to the TS ST NAND2 gate because CNTFET has higher carrier mobility and lower parasitic capacitances than MOSFET devices. Moreover, the CNTFET TS ST NOR2 gate provides increase in V_{HW} by 20 %, and decrease in τ_d and P_{dyn} by 11% and 13%, respectively, with respect to the TS ST NOR2 gate. The CNTFET TS ST NAND2 gate has higher τ_d than the CNTFET TS ST NOR2 gate due to an increase in the path resistance between output and ground. In contrast, the CNTFET TS ST NOR2 gate achieves faster discharge and lower τ_d than the CNTFET TS ST NAND2 gate. Further, the CNTFET TS ST XOR2 gate increases V_{HW} by 19.2 % in comparison to the TS ST XOR2 gate. The CNTFET TS ST XOR2 gate decreases τ_d and P_{dyn} by 13.3 % and 21 % in comparison to the TS ST XOR2 gate. It is observed that the trend of improvement in the performance parameter is the same for the inverter.

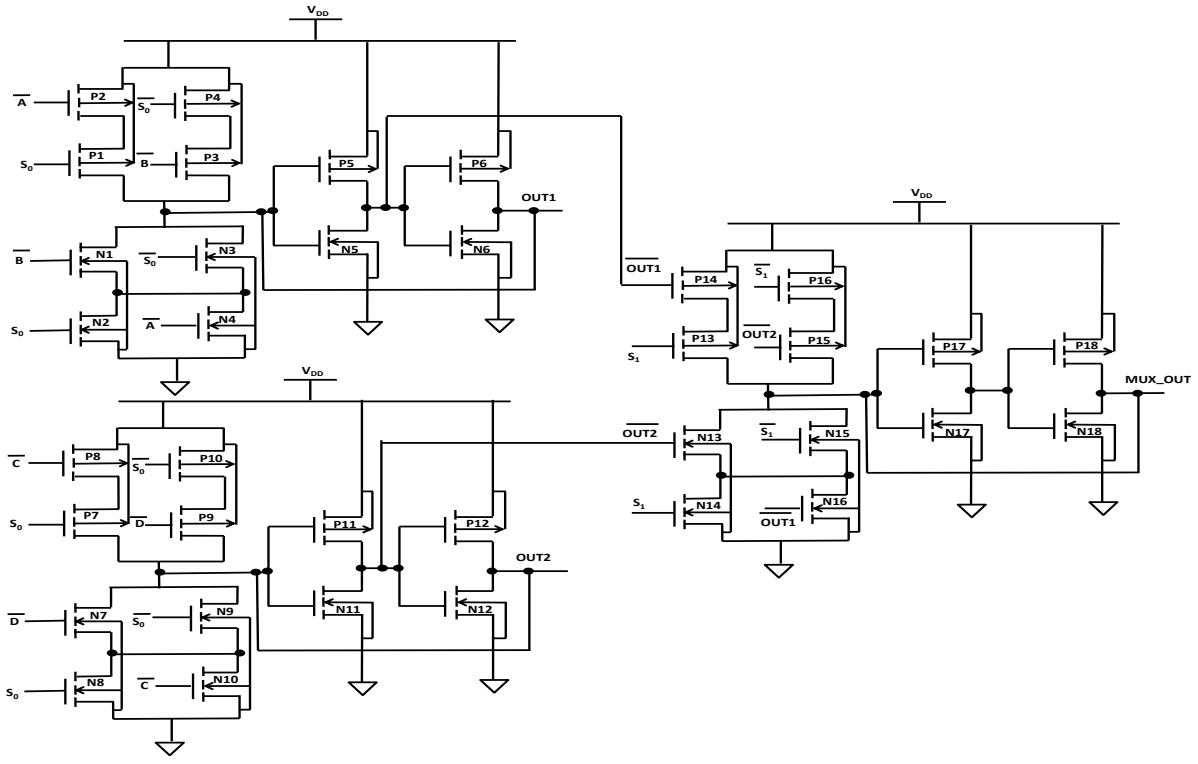
Table 6.2: Performance comparison of the TS ST and proposed CNTFET TS ST gates

ST styles / **Performance comparison**	**MOSFET TS ST**	**Proposed CNTFET TS ST**
NAND2		
V_{HW} (mV)	307	367
τ_d (ns)	2.12	1.85
P_{dyn} (nW)	7.9	6.9
PDP (10^{-18} J)	16.74	12.76

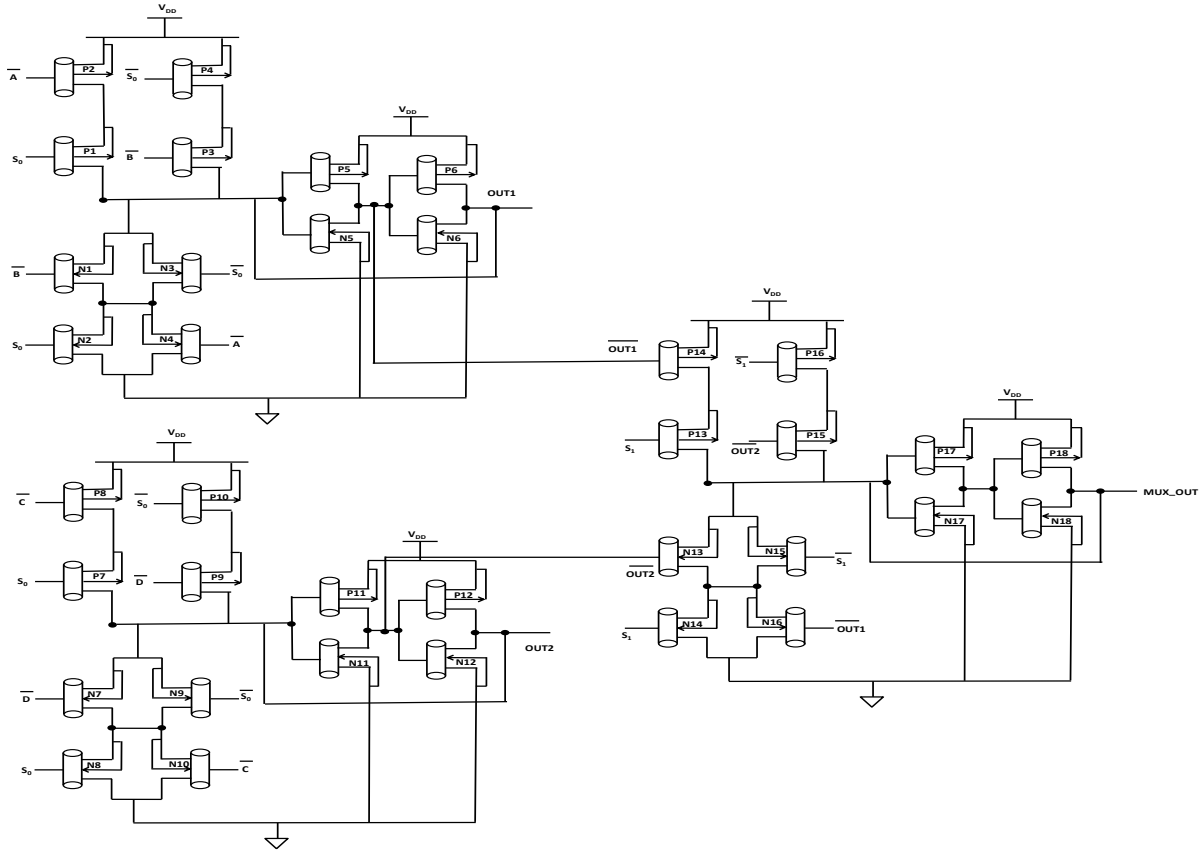
NOR2		
V_{HW} (mV)	312	374
τ_d (ns)	1.85	1.65
P_{dyn} (nW)	8.4	7.3
PDP (10^{-18} J)	15.54	12.04
XOR2		
V_{HW} (mV)	311	371
τ_d (ns)	3	2.60
P_{dyn} (nW)	14	11
PDP (10^{-18} J)	42	28.6

6.4 Design Example using proposed CNTFET TS ST logic style

A 4:1 MUX is taken as a design example. The block diagram of 4:1 MUX is taken as shown in Fig. 3.12. The design of a 4:1 TS ST and proposed CNTFET TS ST MUXs is shown in Fig. 6.5. The design employs two 2:1 MUXs in the first stage, which is followed by one 2:1 MUX in the second stage. The MUXs are simulated, and the results of different performance parameters are listed in Table 6.3. The 4:1 TS ST MUX is simulated using 32 nm PTM CMOS technology, and the 4:1 CNTFET TS ST MUX is simulated using 32 nm CNTFET technology parameters with the same simulation setup. The proposed 4:1 CNTFET TS ST MUX improves V_{HW} by 23 % in comparison to the 4:1 TS ST MUX. It is observed that the proposed 4:1 CNTFET TS ST MUX has reduced the τ_d value by 17 % in comparison to the 4:1 TS ST MUX. The proposed 4:1 CNTFET TS ST MUX offers P_{dyn} reduction by 18 % in comparison to the 4:1 TS ST MUX.



(a)



(b)

Fig.6.5 Realization of 4:1 MUXs in different styles (a) TS ST (b) CNTFET TS ST

Table 6.3: Performance comparison of the TS ST and proposed 4:1 CNTFET TS ST MUXs

ST styles / Performance comparison	TS ST MUX	Proposed CNTFET TS ST MUX
V_{HW} (mV)	307	375
τ_d (ns)	7	5.8
P_{dyn} (nW)	26	21.4
PDP (10^{-18} J)	182	124

6.5 Conclusion

In this chapter, the CNTFET are introduced in TS ST logic style to enhance performance at lower technology node. The CNTFET TS ST logic gates are implemented by replacing MOSFET transistors in the TS ST logic style with CNTFET transistors. Different CNTFET TS ST logic gates and their performance are compared with the existing MOSFET-based TS ST logic counterparts. It is observed from the simulation results that the proposed CNTFET TS ST inverter increases hysteresis width by 19 %, and reduces propagation delay and dynamic power by 11% and 12.5%, respectively, in comparison to the MOSFET-based TS ST inverter. Further, it is confirmed that the CNTFET TS ST AND2, OR2 and MUX provide better noise

immunity, speed, and power consumption in comparison to existing counterparts. Further, the reliability of the proposed CNTFET gates is verified by process corner and voltage variation analysis, which confirms the effectiveness of the proposed style among all the designs. The proposed CNTFET TS ST gates are suitable for digital circuit design at lower technology nodes.

Chapter 7

Conclusion and Future Scope

This chapter summarizes the major findings in this thesis and outlines possible future work that can be developed based on the basic ideas presented here.

7.1 Summary of work done in this thesis

Chapter 1: Introduction

The first chapter presents the background, motivation, and objectives of the research work. The motivation for this work arises from the increasing demand for low-power circuits in modern energy-constrained applications. Various power supply reduction techniques are explored to support low-voltage operation, however, these techniques exhibit degraded I_{ON}/I_{OFF} characteristics and reduced noise immunity. In this regard, ST logic has emerged as a promising approach due to its inherent noise immunity and robust performance under reduced supply voltage conditions. The fundamental concepts of ST logic gate operation are discussed to provide the necessary background for the proposed work. In addition, research gaps in the existing ST logic design are identified. Based on these research gaps, the objectives of the present work are clearly formulated, thereby establishing a strong foundation for the subsequent chapters of the thesis.

Chapter 2: Existing ST Gates

This chapter presents a comprehensive study of ST logic gates, including both static and dynamic implementations. The operational principles, design methodologies, and associated performance parameters of ST logic gates are discussed in detail. Furthermore, the improved forms of static and dynamic ST logic gates are presented for enhanced performance under low-voltage operation. The realization of various logic functions using static as well as dynamic ST logic gates is also elaborated. In addition, the implementations of two important design examples, namely the 4:1 MUX and full adder, are demonstrated. Finally, a comparative performance analysis is presented to validate the theoretical propositions and highlight the effectiveness of the proposed ST logic approaches.

Chapter 3: Improved Current Feedback Static Schmitt Trigger Logic Gates

This chapter presents the design and analysis of static ST logic gates based on current feedback techniques. Existing current feedback ST logic gates are reviewed, highlighting their advantages in leakage reduction along with limitations such as increased delay, degraded noise immunity, higher power consumption, and fabrication complexity. To address these challenges, two novel static ST logic styles, namely TS ST logic and TG-TS ST logic, are proposed. The TS ST logic employs a three-stage inverter with positive feedback, whereas the TG-TS ST logic integrates transmission gates with the TS ST logic structure to achieve improved circuit performance. Both proposed logic styles are investigated for the implementation of XOR2 functionality and simulated using CMOS PTM 45 nm technology parameters. The performance of the proposed TS ST XOR2 and TG-TS ST XOR2 gates is compared with existing ST XOR2 gates in terms of noise immunity, dynamic power consumption, propagation delay, and PDP. The results demonstrate that the proposed TS ST XOR2 gate achieves the highest noise immunity, while the proposed TG-TS ST XOR2 gate exhibits the lowest dynamic power consumption among all considered designs. Furthermore,

the proposed 4:1 TG-TS ST XOR2 multiplexer provides the lowest propagation delay along with the second-highest noise immunity compared to existing multiplexer designs. In addition, process corner and voltage variation analyses have been carried out to verify the reliability and robustness of the proposed logic styles. Overall, the proposed TG-TS ST logic gates are found to be highly suitable for low-power, high-performance, and noise-immune digital circuit applications.

Chapter 4: Improved Voltage Feedback Static Schmitt Trigger Logic Gates

This chapter presents the design and analysis of improved static ST logic gates employing voltage feedback techniques. Existing voltage feedback based ST logic gates are reviewed, highlighting their enhanced noise immunity along with the drawback of increased leakage current caused by additional conduction paths through the positive feedback transistors. To address these limitations, a novel SVTCMOS ST logic style is proposed. The proposed SVTCMOS ST logic combines transistor stacking with the variable threshold voltage technique to achieve reduced leakage current while maintaining improved noise immunity. Mathematical analyses are put forward to demonstrate the reduction in leakage current and enhancement in hysteresis width compared to the existing VTCMOS ST logic style. The proposed logic gates are simulated using LTspice with 45 nm PTM CMOS technology parameters, and the theoretical results are validated through simulation outcomes. The results indicate that the proposed SVTCMOS ST buffer achieves significant reductions in leakage current and dynamic power, along with improved hysteresis width compared to the conventional VTCMOS ST buffer. Furthermore, a 4:1 SVTCMOS ST multiplexer is designed and analyzed, demonstrating lower leakage current, reduced dynamic power consumption, and enhanced noise immunity in comparison to the VTCMOS ST multiplexer. In addition, process corner and voltage variation analyses confirm the robustness and reliability of the proposed logic style. Overall, the proposed SVTCMOS ST logic gates are found to be highly suitable for energy-constrained and noise-tolerant digital circuit applications.

Chapter 5: Modified Domino Schmitt Trigger Logic Gates

This chapter presents the design and analysis of dynamic CMOS ST logic gates with emphasis on improving speed and noise immunity. Dynamic ST logic gates, which operate on the principle of precharge and evaluation, have been studied as high-speed alternatives to static ST logic gates. To enhance the performance of conventional domino ST logic, the use of DTMOS transistors in the pull-down network has been proposed. A brief overview of DTMOS operation has been presented, followed by the detailed design and analysis of the proposed domino ST logic style. The proposed domino ST logic consists of two stages, where the first stage realizes the logic functionality using DTMOS based dynamic circuitry and the second stage employs a CMOS inverter. In addition, modified keeper and feedback transistors have been incorporated to improve circuit performance. Various logic gates based on the proposed domino ST logic style have been designed and simulated using CMOS PTM 45 nm technology parameters. The simulation results demonstrate that the proposed domino ST logic buffer achieves significant reduction in propagation delay and substantial enhancement in hysteresis width compared to existing domino ST logic buffers. Furthermore, the proposed domino ST logic gates exhibit enhanced noise immunity, improved speed and reduced area among the considered designs, although with a slight increase in leakage power. The proposed domino ST AND2, OR2, and 4:1 ST MUXs also provide considerable improvements in speed and noise immunity compared to conventional domino ST gates. In addition, process corner and voltage variation analyses

confirm the robustness and reliability of the proposed design approach. Overall, the proposed domino ST logic style is found to be highly suitable for high-speed and noise immune dynamic digital circuit applications.

Chapter 6: CNTFET based Schmitt Trigger Logic Gates

This chapter presents the implementation and analysis of ST logic gates using CNTFET to overcome the limitations associated with conventional planar silicon MOSFET-based ST gate designs at nanometer-scale technology nodes. In this regard, CNTFETs are investigated due to their superior carrier mobility, near-ballistic transport characteristics, and enhanced current driving capability, that makes them suitable for low-power and high-performance digital circuit applications. The previously proposed three-stage Schmitt trigger (TS ST) logic style is extended using CNTFET technology by replacing MOSFET transistors with CNTFET devices. Various CNTFET-based TS ST logic gates are designed and analyzed at the 32 nm technology node, and their performance is compared with the corresponding MOSFET-based TS ST logic gates. Simulation results demonstrate that the proposed CNTFET TS ST inverter achieves enhanced hysteresis width along with reduced propagation delay and dynamic power consumption compared to the MOSFET-based TS ST inverter. Furthermore, the proposed CNTFET TS ST AND2, OR2, and MUX gates exhibit improved noise immunity, higher speed, and lower power consumption relative to existing counterparts. In addition, process corner and voltage variation analyses confirm the robustness and reliability of the proposed CNTFET-based designs. Overall, the proposed CNTFET TS ST logic gates are found to be highly suitable for low-power, high-performance, and reliable digital circuit design at advanced technology nodes.

Chapter 7: Conclusion and Future Scope

The proposed TS ST, TG-TS ST, SVTCMOS ST, domino ST, and CNTFET-based TS ST logic styles have been designed and analyzed for different logic functions including buffers, AND2, OR2, XOR2, and 4:1 MUXs. The simulation results obtained using CMOS PTM technology parameters demonstrate significant improvements in terms of noise immunity, leakage current, propagation delay, dynamic power consumption, and PDP compared to existing ST logic counterparts. Furthermore, process corner and voltage variation analyses confirm the robustness and reliability of the proposed logic styles under different operating conditions. The incorporation of CNTFET technology further extends the applicability of ST logic gates toward advanced nanometer technology nodes by achieving enhanced speed, reduced power consumption, and improved hysteresis characteristics.

Overall, the presented work establishes efficient ST logic design approaches suitable for energy-constrained, high-speed, and noise-tolerant digital systems. In addition, this chapter outlines potential future research directions, including the exploration of advanced device technologies, optimization of ST logic architectures, investigation of emerging low-power design techniques, and the implementation of complex VLSI systems using the proposed ST logic styles.

7.2 Future Scope

The research work done in thesis is devoted to the design of ST logic gates for low-power, high-performance, and noise-immune digital circuit applications. The study comprehensively

investigates both static and dynamic ST logic gate design methodologies employing current feedback and voltage feedback techniques. Various limitations associated with existing ST logic styles, such as increased leakage current, degraded noise immunity, power-delay tradeoff, and fabrication complexity, have been identified and addressed through the development of novel ST logic structures. Some of the avenues for future work that can be taken up are

1. An algorithmic design methodology can be systematically developed for the proposed ST gates to achieve an optimal trade-off between low power consumption and high-speed performance. This approach involves defining structured design steps, including transistor sizing, threshold voltage tuning, and feedback network optimization, to control switching characteristics and hysteresis behaviour. Design parameters such as load capacitance, supply voltage scaling, and feedback strength can be algorithmically adjusted to meet target specifications.
2. The cascading behaviour of dynamic ST gates can be systematically analyzed to understand signal propagation, timing constraints, and the impact of hysteresis on successive stages. Key aspects such as charge sharing, clocking scheme, noise immunity, and signal integrity must be carefully evaluated to ensure reliable operation when multiple dynamic ST stages are connected in sequence. Based on this analysis, the proposed dynamic ST gates can be effectively extended to realize pipelined architectures.

3. The applicability of the proposed TS ST and TG-TS ST logic styles can be further investigated by extending their implementation to complex combinational and sequential circuits. This enables a comprehensive evaluation of their impact on system-level performance metrics, including noise immunity, propagation delay, power consumption, and power delay product. Moreover, integrating these logic styles into larger architectures such as arithmetic units, control logic, and pipelined systems can reveal their potential advantages in enhancing robustness against process and voltage variations. Such exploration will provide deeper insights into their scalability and suitability for low-power and high-performance VLSI design.

4. The work on CNTFET-based ST gates can be extended to develop arithmetic circuits such as adders, subtractors, multipliers, and arithmetic logic units (ALUs), which serve as fundamental building blocks in energy-constrained applications.

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