

STUDY AND DESIGN OF HIGH PERFORMANCE SAR-ADC

**A Thesis Submitted
in Partial Fulfillment of the Requirements
for the Degree of**

DOCTOR OF PHILOSOPHY

by

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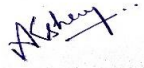
June, 2026

Acknowledgement

I supremely thank the Almighty God for the opportunities and abilities He has endowed in me that have enabled me to come this far.

I take the opportunity to humbly submit my heartfelt appreciation to **Prof. Neeta Pandey** from the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, and **Prof. Maneesha Gupta** from the Department of Electronics and Communication Engineering, Netaji Subhas University of Technology, Delhi, for steering me this far in the scholarly research work. Their immense contribution and rare dedication in providing much-needed guidance are worth much honor. They are my continual source of inspiration in the face of monumental challenges in research. They are academic giants under whose watch I am molded into a seasoned research scholar. They have been of great help in the successful completion of my research work. I extend my sincere regards to **Prof. Neeta Pandey**, HOD ECE department, DTU, for her constant support. I wish to express my gratitude towards the DRC chairperson and the esteemed faculty members for their valuable time and efforts throughout this journey.

My appreciation also goes to my colleagues in the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, for their constant encouragement and motivation. I also thank my family and friends for their continual prayers, encouragement and support throughout this research period.


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CANDIDATE'S DECLARATION

I **Akshay Mann** hereby certify that the work which is being presented in the thesis entitled "**Study and Design of High Performance SAR-ADC**" in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the Department of Electronics and Communication Engineering, Delhi Technological University, is an authentic record of my own work carried out during the period from January 2021 to April 2026 under the supervision of **Prof. Neeta Pandey**, Professor in the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India, and **Prof. Maneesha Gupta**, Professor in the Department of Electronics and Communication Engineering, Netaji Subhas University of Technology, Delhi, India.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other institute.

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This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

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ABSTRACT

The rapid advancement of modern electronic systems has significantly increased the demand for efficient interfaces bridging continuously varying physical signals and digital processing architectures. Modern applications such as Internet of Things (IoT) infrastructures, wireless sensing systems, wearable medical devices, biomedical instrumentation, industrial control platforms, environmental monitoring networks, autonomous systems, and portable electronics rely on continuous acquisition of analog data and its subsequent processing in digital environments. As a result, Analog-to-Digital Converters (ADCs) have become one of the fundamental components of modern mixed-signal integrated systems. The performance of an ADC directly affects the overall accuracy, speed, reliability and energy efficiency of the entire electronic system. Consequently, the optimization of ADC architectures for achieving superior performance and lower energy consumption has become a major focus in integrated circuit design.

Among various ADC architectures, Successive Approximation Register (SAR) ADC has emerged as the most attractive solutions for medium-to-high resolution applications owing to its simplified architecture, digital-friendly implementation and excellent energy efficiency. Unlike pipeline ADCs that require power-hungry operational amplifiers or flash ADCs that require a large number of comparators, SAR ADC architectures perform conversion by progressively refining the digital estimate of the input signal using a comparator, Capacitive Digital to Analog Converter (CDAC) and successive approximation control. These advantages make SAR ADCs highly suitable for low-power applications operating under strict energy constraints. However, despite their inherent efficiency, conventional SAR ADCs still face several performance limitations. Comparator delay, DAC switching energy, capacitor area, settling time, power, energy efficiency and SAR control overhead significantly influence the achievable speed, resolution and power consumption of the converter. Furthermore, continued CMOS technology scaling introduces additional challenges such as reduced voltage headroom, increased leakage currents, device mismatch and degraded analog circuit performance.

Motivated by these challenges, this thesis presents a comprehensive investigation of advanced circuit and architectural techniques aimed at improving the performance of SAR ADCs while maintaining low power consumption and high conversion efficiency. The work begins with a detailed study of ADC fundamentals, performance parameters and existing literature survey. Important SAR ADC performance metrics including resolution, sampling rate, conversion time, Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SNDR), Spurious-Free Dynamic Range (SFDR), Effective Number of Bits (ENoB), Differential Nonlinearity (DNL), Integral Nonlinearity (INL) and Figure of Merit (FoM) are examined to establish the theoretical framework for evaluating converter performance. A comprehensive study is then conducted covering advanced mixed signal circuit techniques including conventional comparator architectures, DAC switching algorithms, capacitor array optimization techniques, SAR logic implementations and hybrid ADC architectures. Through this survey, several research gaps are identified, particularly in comparator design, switching energy reduction, control logic optimization and high-speed hybrid conversion methodologies.

To address the limitations of conventional comparators, the thesis proposes and investigates multiple comparator architectures employing different circuit enhancement techniques. Initially, self-cascode based comparator architectures are developed to improve voltage gain and regenerative behavior while maintaining low static power dissipation. The self-cascode structure effectively increases output resistance and enhances amplification without requiring additional power consuming stages. Subsequently, shared-charge reset mechanisms and auxiliary inverter techniques are introduced to reduce comparison delay and accelerate the regeneration process. These methods improve the charging and discharging characteristics of internal nodes, thereby enhancing comparator speed and reducing energy consumption. Furthermore, Dynamic Threshold MOS (DTMOS)-based comparator architectures are proposed to enable reliable low-voltage operation. By dynamically connecting the gate and body terminals of transistors, the threshold voltage is adaptively controlled during circuit operation, resulting in improved current drivability, faster decision making, and enhanced sensitivity under reduced supply voltages. Detailed circuit-level simulations are performed to evaluate propagation delay, power consumption and energy efficiency. Comparative analysis among all proposed comparator architectures identifies the most suitable design for integration into low-power SAR ADC systems.

Building upon the optimized comparator structure, a low-power 10-bit SAR ADC architecture is designed and implemented. The proposed ADC incorporates a bootstrap switch to improve sampling linearity and minimize signal-dependent resistance variations. The bootstrap circuit ensures a nearly constant gate-source voltage across the sampling transistor, thereby reducing distortion and enhancing input signal fidelity. In addition, a modified split-capacitor DAC architecture is employed to reduce total capacitance and silicon area. The capacitor array is segmented into coarse and fine sections, significantly lowering the overall capacitor requirement while preserving conversion accuracy. To further improve energy efficiency, a V_{cm} -based switching methodology is adopted. Unlike conventional switching techniques that repeatedly connect capacitors between reference voltages, the proposed approach utilizes the common-mode voltage as an intermediate reference level, thereby reducing charge redistribution energy. An additional energy-optimized switching strategy is developed to minimize unnecessary capacitor transitions during successive approximation, resulting in substantial reductions in DAC switching energy and dynamic power consumption.

To overcome the speed limitations associated with conventional SAR conversion, a novel Hybrid Flash-SAR ADC architecture is proposed. The hybrid architecture integrates the advantages of flash and SAR conversion techniques to simultaneously achieve high conversion speed with reduced power consumption. In the proposed design, a 4-bit flash ADC front-end performs coarse quantization of the input signal and generates the four most significant bits (MSBs). The flash stage utilizes multiple comparators operating in parallel, enabling instantaneous determination of the coarse digital code. Rest six least significant bits (LSBs) are then resolved by a SAR ADC back-end employing a segmented split-capacitor DAC and asynchronous control logic. By pre-determining the MSBs through flash conversion, thereby decreasing the total number of successive approximation cycles required for conversion, resulting in lower conversion latency and higher sampling speed.

A dedicated output encoding and bit-concatenation architecture is also developed for the hybrid converter. The thermometer-coded outputs generated by the flash ADC are converted into binary format using a thermometer-to-binary encoder. These encoded MSBs are synchronized using D flip-flops and combined with the LSBs generated by the SAR ADC through an output assembler block. The resulting architecture produces a complete 10-bit

digital output while ensuring proper timing synchronization between the flash and SAR conversion stages. Furthermore, asynchronous SAR logic is employed to eliminate unnecessary clock cycles and reduce conversion delay, enabling faster operation compared with conventional synchronous SAR controllers.

Extensive simulation studies are carried out using Cadence Virtuoso in a CMOS technology environment to validate the proposed architectures. The performance of individual circuit blocks, including the comparator, DAC, SAR logic, encoder and hybrid conversion system, is thoroughly analyzed. Static performance evaluation includes DNL and INL measurements to assess converter linearity. Dynamic performance is evaluated using FFT based analysis from which SNDR, SFDR, Total Harmonic Distortion (THD) and ENOB are extracted. Power consumption, switching energy, conversion delay and energy efficiency are also investigated in detail. Comparative analysis against conventional switching techniques such as monotonic switching, Vcm-based switching and split capacitor switching demonstrates significant reductions in switching energy achieved by the proposed methodology. Similarly, the proposed hybrid architecture exhibits improved conversion speed while maintaining low power operation compared with traditional SAR ADC designs.

The research contributions presented in this thesis provide improvements at both circuit and system levels. At the circuit level, novel comparator architectures based on self-cascode, shared-charge, auxiliary inverter and DTMOS techniques enhance speed, sensitivity and energy efficiency. At the architectural level, the proposed split-capacitor DAC, energy-efficient switching methodology, asynchronous SAR logic and Hybrid Flash-SAR conversion approach collectively reduce power consumption, switching energy and conversion latency. These contributions provide a systematic foundation for developing next-generation ADC architectures with improved energy efficiency and enhanced performance.

The outcomes of this research have significant practical relevance for modern electronic systems operating under stringent energy constraints. The proposed ADC architectures are particularly suitable for IoT sensor nodes, wearable health-monitoring devices, biomedical instrumentation, wireless communication transceivers, environmental monitoring platforms, smart industrial systems and battery-powered portable electronics. Furthermore, the developed methodologies provide a foundation for future investigations into ultra-low-

voltage operation, advanced CMOS technology scaling, adaptive calibration techniques, artificial intelligence-assisted data conversion systems and high-speed mixed-signal integrated circuits. Consequently, the work presented in this thesis contributes toward the development of energy-efficient and sustainable electronic systems capable of supporting the growing demands of future digital technologies.

List of Publications

SCI/SCIE Indexed Journal Papers Accepted/Published

1. **Akshay Mann**, Neeta Pandey, Maneesha Gupta, “Novel high-speed low-power comparators imbibing self-cascode preamplifier technique,” *AEU - International Journal of Electronics and Communications*, vol. 185, 2024, pp. 155429. ISSN: 1434-8411. DOI: <https://doi.org/10.1016/j.aeue.2024.155429>
2. **Akshay Mann**, Neeta Pandey, Maneesha Gupta, “Energy efficient high-speed dynamic comparators using shared charge logic and auxiliary inverter technique,” *AEU - International Journal of Electronics and Communications*, vol. 195, 2025, pp. 155787. ISSN: 1434-8411. DOI: <https://doi.org/10.1016/j.aeue.2025.155787>
3. **Akshay Mann**, Neeta Pandey, Maneesha Gupta, “High-Speed, Power Efficient 10-bit Hybrid Flash–SAR ADC with Non-binary Segmented DAC and Asynchronous Control,” in *AEU - International Journal of Electronics and Communications*, vol. 211, 2026, pp. 156304. DOI: <https://doi.org/10.1016/j.aeue.2026.156304>

Scopus Indexed International Conference Papers

1. **Akshay Mann**, Neeta Pandey, Maneesha Gupta, “Design of DTMOS Based Preamplifier for Low Power and High Speed Comparator,” *2025 IEEE International Conference on Interdisciplinary Approaches in Technology and Management for Social Innovation (IATMSI)*, Gwalior, India, 2025, pp. 1–5. DOI: 10.1109/IATMSI64286.2025.10985249.
2. **Akshay Mann**, Neeta Pandey, Maneesha Gupta, “Capacitor Splitting Based DAC Switching for Reduced Energy and Power Consumption in SAR ADCs,” *IEEE International Conference on Computing, Communication and Networks and Telecommunications (ICCNT 2025)*, 2025. (Published).

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List of Abbreviations

IoT	Internet of Things
ADC	Analog to Digital Converter
SAR	Successive Approximation Register
DAC	Digital to Analog Converter
CDAC	Capacitive Digital to Analog Converter
CMOS	Complementary Metal Oxide Semiconductor
LSB	Least Significant Bit
MSB	Most Significant Bit
FFT	Fast Fourier Transform
SNR	Signal to Noise Ratio
SNDR	Signal to Noise and Distortion Ratio
THD	Total Harmonic Distortion
SFDR	Spurious Free Dynamic Range
ENoB	Effective Number of Bits
DNL	Differential Non Linearity
INL	Integral Non Linearity
FoM	Figure of Merit
dB	Decibels
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
DTMOS	Dynamic Threshold-voltage MOS
OTA	Operational Transconductance Amplifier

SC	Switched Capacitor
PVT	Process, Voltage, Temperature
PC1	Proposed Comparator 1
PC2	Proposed Comparator 2
PC3	Proposed Comparator 3
PC4	Proposed Comparator 4
PC5	Proposed Comparator 5
PC6	Proposed Comparator 6
PDP	Power Delay Product
MATLAB	Matrix Laboratory
SDG	Sustainable Development Goal

Chapter 1

Introduction

Modern electronic systems increasingly rely on efficient interfaces between the physical world and digital processing platforms. Most signals originating from real-world environments—such as temperature, pressure, light intensity, sound waves, biomedical signals and wireless communication signals—exist in analog form [1-3]. However, modern computing, signal processing, and communication systems operate predominantly in the digital domain due to their superior robustness, programmability and scalability. Consequently, an essential component of any mixed-signal system is the Analog-to-Digital Converter (ADC) which transforms continuous-time analog signals into corresponding digital values that can be processed, stored and analyzed by digital systems [4, 21].

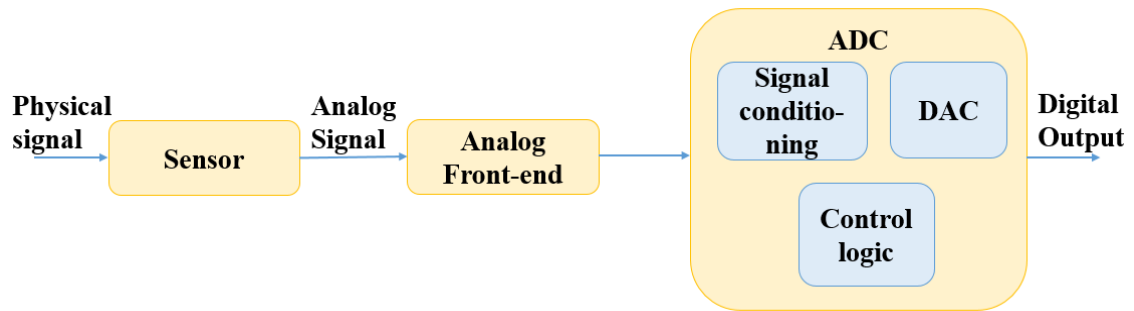


Fig.1.1 Energy constrained sensing and data acquisition system

ADCs are essential components in numerous modern electronic and communication systems including wireless communication systems, sensor networks, biomedical instrumentation, automotive electronics, industrial monitoring systems, and portable consumer devices [1, 4, 5]. The overall precision, operating speed, and energy efficiency of a system are significantly affected by the performance characteristics of the ADC. This

results in designing of high-performance ADC architectures that have become a key research area in mixed-signal integrated circuit design [22].

Over the years, numerous ADC architectures have been introduced to satisfy the varying performance demands of contemporary electronic applications. These architectures are designed to satisfy different combinations of sampling speed, resolution, power consumption, and implementation complexity, depending on the target application. Some of the most commonly used ADC architectures include Flash ADCs, Pipeline ADCs, Sigma-Delta ADCs and SAR ADCs [2, 3, 6-8, 14, 15]. Each of these architectures employs a different conversion mechanism and therefore offers unique advantages and limitations.

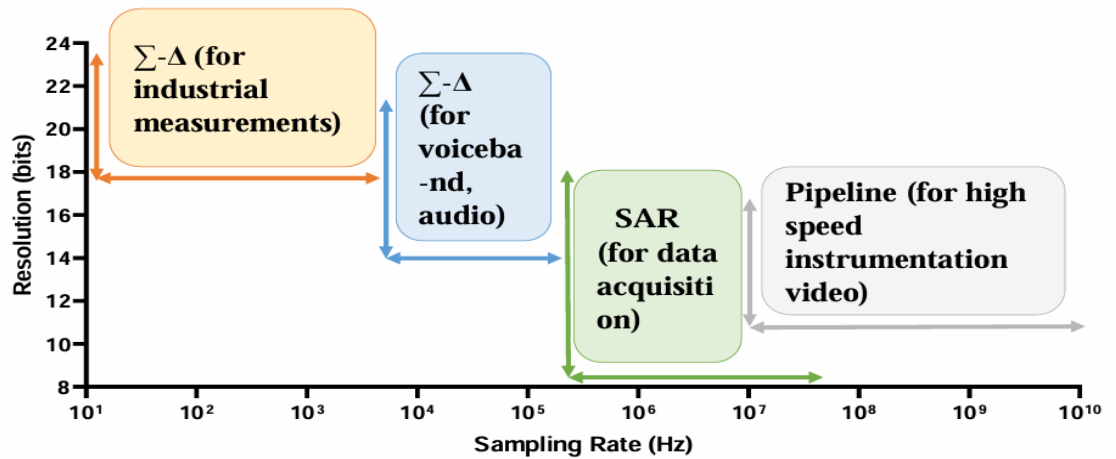


Fig.1.2 Resolution vs. Sampling Rate comparison of ADC architectures

Flash ADCs represent one of the earliest and fastest converter architectures. In this technique, the input signal is concurrently evaluated against multiple reference voltage levels through a parallel network of comparators [7, 9-12]. For an N-bit resolution, a flash ADC requires $2^N - 1$ comparators along with a resistor ladder network to generate the reference levels [13]. This parallel comparison enables extremely high conversion speeds with minimal latency, making flash ADCs suitable for applications such as high-speed data communication, radar systems and high-frequency instrumentation [14, 18].

However, the exponential increase in comparator count with resolution leads to significant drawbacks, including large silicon area, high static power consumption, increased input capacitance and severe mismatch issues [2, 7]. Consequently, flash ADCs are generally limited to low-resolution designs, typically in the range of 4–8 bits.

Pipeline ADCs offer an effective compromise between conversion speed and resolution by dividing the overall conversion process into multiple sequential stages [16, 17]. Each stage determines a few bits of the digital output and produces a residue signal, which is then amplified and forwarded to the next stage for additional conversion. This staged conversion mechanism allows pipeline ADCs to achieve moderate to high resolutions while maintaining relatively high sampling rates [2, 8]. As a result, pipeline architectures are generally used in applications like wireless communication receivers, digital video systems and high-speed imaging devices. Nevertheless, pipeline ADCs depend extensively on high-accuracy analog building blocks, including operational amplifiers, residue amplifiers and precisely matched capacitors. These components introduce significant power consumption and design complexity, especially in advanced CMOS processes, where lower supply voltages increase the difficulty of designing high-gain amplifiers [19, 23].

Sigma-Delta ADCs follow a fundamentally different conversion principle based on oversampling and noise-shaping techniques [14, 15]. In these ADCs, the input signal is sampled at a frequency much greater than the Nyquist rate and quantization noise is pushed toward higher frequencies through the use of feedback loops and digital filtering. This technique enables sigma-delta ADCs to provide exceptionally high resolution and superior linearity, making them ideal for precision measurement, audio processing and instrumentation systems [8, 18]. However, the reliance on oversampling and digital filtering introduces latency and limits the achievable conversion speed. Therefore, sigma-delta converters are typically restricted to low-bandwidth applications where high resolution is more important than high sampling rates.

Among these architectures, SAR ADC has become increasingly popular because of its efficient balance among power consumption, resolution and implementation complexity [1, 20-23]. SAR ADCs carry out the conversion operation through a binary search method that progressively identifies each bit of the output code. A typical SAR ADC architecture includes a bootstrap switch, comparator, capacitive digital-to-analog converter (DAC) and SAR control circuitry. Since SAR ADCs rely primarily on passive charge redistribution rather than power-hungry amplification stages, they are inherently energy-efficient [5, 24]. Furthermore, their largely digital implementation allows them to scale effectively with modern CMOS technologies. These features make SAR ADCs highly appropriate for low-power applications, including IoT sensor nodes, wearable devices, biomedical monitoring equipment and portable communication systems.

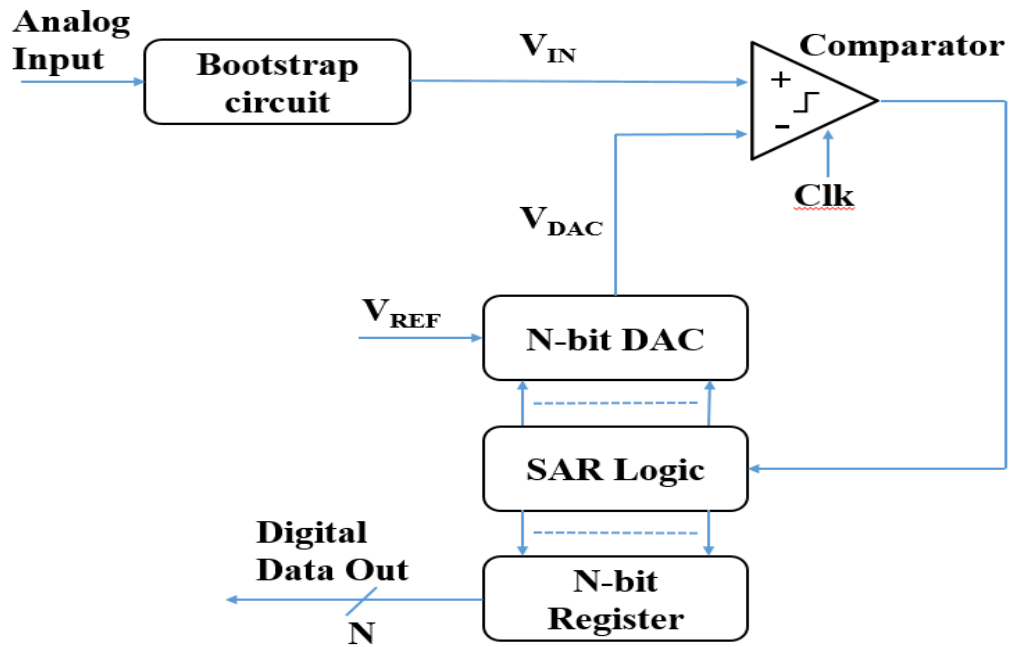


Fig.1.3 Basic architecture of N-bit SAR ADC

Despite the inherent advantages of SAR ADC architectures, achieving simultaneously high conversion speed, low power consumption, and high resolution remains a significant design challenge [21, 23]. The performance of a SAR ADC largely depends on the

effectiveness and optimization of its key building blocks, including the comparator, CDAC and SAR logic [25-27, 35]. Each of these components contributes directly to the conversion speed, energy consumption, and accuracy of the converter and any inefficiency within these blocks can limit the achievable performance of the entire system.

The comparator acts as the primary decision-making component in a SAR ADC, determining the sign of the voltage difference between the sampled input signal and the reference voltage produced by the DAC at every conversion stage. Because the comparator operates repeatedly during each conversion cycle, its propagation delay and power consumption have a major effect on the converter's overall speed and energy efficiency. Conventional dynamic comparator architectures, such as the StrongARM latch and double-tail latch comparators, often suffer from several limitations including input-referred offset voltage, metastability issues and kickback noise [28, 30-32]. Device mismatch in the input differential pair can introduce offset errors, which degrade the precision of the conversion operation. Additionally, during regeneration phase of the comparator, large voltage transitions at internal nodes can propagate back to the input terminals, generating kickback noise that disturbs the stored charge on the sampling capacitor [21, 24]. These effects become more pronounced in scaled CMOS technologies where supply voltages are reduced and transistor mismatch increases.

Another major contributor to SAR ADC power consumption is the CDAC [29]. In conventional binary-weighted DAC architectures, the capacitor array must maintain precise ratios between capacitors to accurately generate reference voltages corresponding to different digital codes [7]. As the converter resolution becomes higher, the size of the capacitor array increases exponentially, leading to greater silicon area consumption and higher parasitic capacitance effects. Furthermore, during the successive approximation process, the capacitors undergo frequent switching between reference voltage levels and ground, leading to significant switching energy consumption [33, 34]. This continuous switching operation can contribute significantly to the overall power consumption of the SAR ADC. Additionally, large capacitor arrays create longer settling durations because of

increased RC time constants, thereby restricting the maximum attainable sampling rate of the converter.

The SAR logic also has a vital role in defining the efficiency of the conversion operation. It executes the binary search algorithm used to generate the final digital output code. Conventional synchronous SAR logic architectures rely on a global clock signal to coordinate each comparison step, which may introduce unnecessary idle periods between operations [35, 36]. This can reduce the effective conversion speed and increase the energy consumed per conversion cycle. Moreover, the interaction between the comparator, DAC switching network and control logic must be carefully synchronized to avoid timing errors and ensure accurate bit decisions. Any inefficiency in the SAR logic, such as excessive switching activity or poor timing management, can increase digital power consumption and reduce overall system performance [37, 39].

In addition to these circuit-level challenges, technology scaling introduces further complications such as reduced supply voltage, increased leakage currents, device mismatch and parasitic effects, all of which affect the performance of SAR ADC building blocks [38, 40]. These limitations highlight the need for innovative design techniques that improve comparator speed and accuracy, reduce DAC switching energy and capacitor count, and optimize SAR logic for faster and more energy-efficient operation.

Therefore, significant research efforts are directed toward developing advanced comparator architectures, energy-efficient DAC switching algorithms, and optimized SAR control schemes to improve the overall performance of SAR ADCs [3, 10, 17]. Enhancements in these critical circuit blocks can facilitate the development of SAR ADC architectures that offer high speed, low power consumption and high resolution for modern mixed-signal applications. Moreover, as CMOS technology scales toward deep submicron nodes, analog circuit design faces additional challenges such as reduced supply voltage, increased leakage currents, device mismatch and higher sensitivity to noise and parasitic effects [2, 31]. These challenges require innovative circuit techniques and

architectural improvements to maintain high performance while minimizing power consumption.

In this context, the development of high-performance SAR ADC architectures with improved comparator structures, optimized DAC switching techniques and efficient control logic has become an active area of research [18, 19, 51, 75]. This thesis concentrates on the analysis and design of high-speed, energy-efficient SAR ADC architectures, with special attention given to enhancing comparator performance and optimizing DAC switching techniques while maintaining compatibility with advanced CMOS technologies.

1.1 Motivation

The rapid advancement of portable electronic devices, wireless communication systems and sensor-based monitoring platforms has created an increasing demand for high-performance and energy-efficient data conversion systems [1-4]. Modern applications such as IoT networks, wearable health monitoring devices, environmental sensing systems and biomedical implants require continuous acquisition and processing of analog signals while operating under strict power constraints [1, 5]. In several such applications, the energy budget is highly constrained since the systems operate using compact batteries or energy-harvesting sources, including thermoelectric generators, solar cells and vibration-based energy harvesters [2, 6].

Under such conditions, minimizing power consumption becomes a critical design objective. Among all the components present in a typical signal acquisition chain, including sensors, analog front-end circuits, microcontrollers and communication modules, ADC frequently accounts for a considerable share of the overall system power consumption [5, 7]. Hence, improving the energy efficiency of ADC architectures is essential for extending battery life and enabling long-term autonomous operation of portable devices.

Another important motivation for developing high-performance SAR ADCs arises from the increasing demand for higher sampling speeds and improved signal resolution. Emerging applications such as software-defined radio, wireless communication receivers, high-speed imaging systems and real-time sensor networks require ADCs capable of processing signals at high data rates while maintaining low power consumption [8, 9]. However, attaining both high-speed operation and low power consumption at the same time is difficult because of the fundamental trade-offs involved in ADC design architectures. Among various ADC architectures, SAR ADCs offer a promising solution because of their simple architecture and inherently low power consumption [1, 10, 11]. The absence of operational amplifiers in the signal path significantly reduces static power dissipation, making SAR ADCs suitable for energy-constrained applications. Furthermore, the use of capacitive charge redistribution allows efficient implementation of the DAC with minimal active circuitry [12, 13].

Despite these advantages, several challenges still limit the performance of conventional SAR ADCs. One of the primary limitations arises from the comparator, which is responsible for making multiple decisions during each conversion cycle. Because the comparator is triggered multiple times during the conversion process, its delay and power dissipation greatly affect the overall speed and energy efficiency of the ADC [20, 22]. Traditional comparator structures, including the StrongARM latch and double-tail dynamic comparator, often experience limitations such as high input-referred offset, kickback noise and elevated power consumption when operating at high frequencies [20, 21, 24, 31, 32].

Another significant challenge arises from the CDAC switching technique, which accounts for a major share of the dynamic power dissipation in SAR ADCs [37, 40]. Conventional binary-weighted switching schemes require large capacitor arrays and involve significant switching energy during each conversion cycle. This not only raises power consumption but also results in larger silicon area and longer settling time [38].

In addition to these circuit-level challenges, technology scaling introduces further complexities in mixed-signal circuit design. As CMOS technologies move toward smaller feature sizes, supply voltages are reduced to maintain device reliability [2, 31]. While lower supply voltages help reduce power consumption, they also limit voltage headroom and degrade the performance of analog circuits such as comparators and reference generators. Device mismatch, leakage currents and substrate noise also become more prominent in scaled technologies, making it increasingly difficult to maintain high accuracy and speed [21, 26, 31].

These challenges provide strong motivation for investigating new comparator architectures, energy-efficient DAC switching techniques and improved SAR control strategies that can enhance the overall performance of SAR ADCs [41, 42]. By developing innovative circuit techniques and optimizing the architecture of the converter, it is possible to achieve significant improvements in speed, energy efficiency, and reliability.

Therefore, the primary motivation of this research is to explore and design high-performance SAR ADC architectures capable of achieving low power consumption, high conversion speed and improved energy efficiency while operating reliably in modern CMOS technologies [17-19]. The proposed work focuses on improving key circuit blocks of the SAR ADC—particularly the comparator and DAC switching scheme—to enable efficient data conversion for next-generation mixed-signal systems.

1.2 SAR ADC Performance Parameters

1.2.1 Terms

Several basic terms are generally used to describe the operation and ADC performance characteristics, including SAR ADCs. Understanding these terms is essential for evaluating and comparing different converter architectures.

Resolution:

Resolution is a key parameter that defines the precision and quantization capability of an

Analog-to-Digital Converter (ADC) [1, 2]. It indicates the minimum change in the analog input signal that can be identified and converted into a corresponding digital output code. In simple terms, resolution specifies how finely the input voltage range is divided into discrete digital levels. An ADC with higher resolution can detect smaller variations in the input signal, resulting in more accurate digital representation.

The resolution of an ADC is generally specified by the number of bits (N) used to represent the digital output. In an N-bit ADC, the complete analog input range is partitioned into 2^N discrete quantization levels [1, 3], with each level corresponding to a unique digital code. As the bit resolution increases, the number of quantization levels grows exponentially, enabling more precise representation of the analog input signal.

The voltage difference between two adjacent quantization levels is known as LSB or quantization step size. The LSB defines the minimum variation in the input voltage that causes a one-bit change in the digital output code of the ADC. It can be calculated as:

$$LSB = \frac{V_{FS}}{2^N} \quad (1.1)$$

where V_{FS} is the full-scale input voltage range of the ADC.

For instance, a 10-bit ADC divides the input range into $2^{10}=1024$ discrete levels. If the full-scale input range is 1 V, the corresponding LSB size is approximately 0.976 mV, indicating that the converter can ideally detect voltage variations as small as this amount

Higher resolution ADCs provide more accurate digital representations of analog signals but generally require more complex circuitry, increased conversion time, and higher power consumption. In SAR ADC architectures, resolution directly affects the number of comparison cycles required during the conversion process. Specifically, an N-bit SAR ADC requires N successive comparison operations to determine the final digital output code [4, 5].

In summary, resolution is a key performance parameter that determines the accuracy and precision of an ADC, and increasing the resolution improves the ability of the converter to detect small variations in the input signal. However, achieving higher resolution requires careful design considerations to manage noise, power consumption and circuit complexity.

Sampling Rate:

The sampling rate, also known as the sampling frequency (f_s), indicates the number of times per second a continuous-time analog signal is captured or sampled by an analog-to-digital converter [1, 2]. It determines how frequently the signal is captured and therefore directly influences the ability of the converter to accurately reconstruct the original analog waveform in the digital domain.

According to the Nyquist–Shannon sampling theorem, the sampling frequency must be at least twice the maximum frequency component of the input signal to prevent loss of information during sampling [2, 3]. Mathematically, this condition is expressed as:

$$f_s \geq 2 f_{max} \quad (1.2)$$

where f_{max} represents the highest-frequency component present in the input signal. The frequency $2f_{max}$ is commonly referred to as the Nyquist rate. If the sampling frequency falls below the Nyquist rate, a phenomenon known as aliasing occurs, in which higher frequency components of the input signal are incorrectly mapped into lower frequency components in the sampled signal [2, 4]. This results in distortion that cannot be removed once the signal has been digitized.

In practical implementations, the sampling frequency is typically selected well above the Nyquist rate to ensure a safety margin and ease the design requirements of anti-aliasing filter [1, 5]. The sampling rate also determines the highest input signal bandwidth that the

ADC can accurately convert, making it a critical specification in applications such as communication systems, imaging systems and real-time data acquisition platforms.

Conversion Time:

Conversion time is the total duration required by an ADC to convert a sampled analog input signal into its equivalent digital output code [1, 6]. It represents the interval between the instant when analog input is sampled and the time at which the digital output data becomes available.

In SAR ADC, the conversion process is performed using a binary search algorithm [6, 7]. The converter identifies each output bit in sequence, starting from MSB and continuing towards LSB. At every stage, the comparator determines whether the sampled input signal is higher or lower than the reference voltage produced by DAC.

For an N-bit SAR ADC, the conversion process typically need N comparison cycles, meaning that the conversion time can be approximated as:

$$T_{conv} = N * T_{cycle} \quad (1.3)$$

where T_{cycle} represents the time required for one comparison cycle, including DAC settling and comparator decision time.

The overall conversion time is therefore influenced by several factors, including [8]:

- Comparator decision delay
- DAC settling time
- Propagation delay of SAR logic
- Clock frequency of the ADC

Minimizing the conversion time is essential for achieving higher sampling rates, especially in high-speed applications. Consequently, significant research efforts focus on improving

comparator speed, reducing DAC settling time, and optimizing SAR logic architecture to accelerate the conversion process [9].

Quantization:

Quantization is the procedure of converting a continuous range of analog input amplitudes into a limited number of discrete digital levels [1, 2]. Since an ADC has a limited number of output codes determined by its resolution, the continuous input signal amplitude must be rounded to the closest available digital level. Since the input signal may not exactly match one of the discrete quantization levels, the ADC must approximate the input value to the nearest level. This approximation introduces an error known as quantization error [2, 3], which represents the deviation between the true analog input value and its quantized digital equivalent. In an ideal ADC, the quantization error remains limited within the following range:

$$-\frac{1}{2}LSB \leq e_q \leq +\frac{1}{2}LSB \quad (1.4)$$

Although quantization is an unavoidable aspect of analog-to-digital conversion, increasing the ADC resolution by using more bits decreases the quantization step size and consequently enhances conversion accuracy [1, 4].

Quantization Noise:

The inaccuracy produced during quantization can be represented as a noise component called quantization noise. In theoretical studies, this noise is commonly modeled as a uniformly distributed random signal that is uncorrelated with the input signal [2, 5]. Such an assumption enables the quantization error to be analyzed as an additive noise source within the conversion process. For an ideal ADC with uniformly distributed quantization error, the mean square value of the quantization noise can be expressed as:

$$P_q = \frac{LSB^2}{12} \quad (1.5)$$

where P_q represents the quantization noise power.

Quantization noise establishes a fundamental constraint on the maximum SNR attainable by an ADC and understanding it is therefore critical in the design of high-performance ADC architectures, as it determines the ultimate resolution and accuracy that the converter can achieve.

1.2.2 Dynamic Characteristics

Dynamic characteristics describe the behavior and performance of an ADC when the signal varies with time. Unlike static parameters, which are evaluated using constant or slowly varying input signals, dynamic characteristics are measured using time-varying signals such as sinusoidal, modulated or broadband signals. These parameters provide insight into how accurately the ADC can digitize real-world signals that change continuously over time.

In practical systems such as wireless communication receivers, biomedical instrumentation, radar systems and sensor interfaces, the input signals are rarely static. Instead, they consist of dynamic waveforms that contain multiple frequency components. Therefore, assessing the dynamic performance of an ADC is important for determining its effectiveness in signal processing applications [1, 2].

Dynamic performance metrics are generally evaluated using frequency-domain analysis, typically through FFT of the digital output sequence [2-4, 9]. By applying a pure sinusoidal input signal and observing the spectral components of the ADC output, it is possible to quantify the distortion, noise, and linearity characteristics of the converter. Various key parameters are employed to evaluate the dynamic performance of ADCs.

Signal-to-Noise Ratio (SNR)

The Signal-to-Noise Ratio (SNR) is a fundamental dynamic performance parameter used to assess the quality of an ADC. It is defined as the ratio of the desired signal power to the total noise power within the specified frequency range. In simple terms, SNR indicates how accurately the ADC maintains the original input signal while reducing the impact of noise generated during the conversion process.

Mathematically, the quantization process introduces noise that limits the achievable dynamic performance of the ADC [3, 4]. Consequently, SNR is quantified as:

$$SNR = 10 \log_{10} \left(\frac{P_{signal}}{P_{noise}} \right) dB \quad (1.6)$$

where P_{signal} represents the power of the fundamental input signal, and P_{noise} denotes the total noise power within the system bandwidth, excluding harmonic distortion components. In ADC characterization, SNR is commonly evaluated by applying a pure sinusoidal signal to the converter input and performing FFT on the resulting digital output samples. The fundamental input frequency appears as the primary peak in the frequency spectrum, whereas the other spectral components correspond to noise arising from quantization effects, thermal noise, circuit imperfections and clock jitter. The measured SNR is obtained from the ratio of the fundamental signal power to the total integrated noise power floor.

For an ideal N-bit ADC, the maximum achievable SNR is mainly constrained by quantization noise, which results from the finite number of quantization levels in the converter. By assuming that the quantization error is uniformly distributed within $\pm 1/2$ LSB and behaves as white noise, the theoretical SNR is given by:

$$SNR = 6.02 * N + 1.76 dB \quad (1.7)$$

where N is the resolution of the ADC in bits. This expression indicates that the SNR increases linearly with the number of bits in the converter. In particular, every extra bit of resolution increases the theoretical SNR by nearly 6 dB, effectively doubling the signal-to-noise power ratio. For example:

- An 8-bit ADC ideally provides approximately 49.9 dB SNR
- A 10-bit ADC ideally provides approximately 61.9 dB SNR
- A 12-bit ADC ideally provides approximately 74 dB SNR

However, practical ADCs rarely achieve the ideal SNR due to various non-ideal factors present in real circuits. These factors include thermal noise from resistive elements, comparator noise, capacitor mismatch, clock jitter, switching noise in the DAC array, and substrate coupling effects [5, 6-9]. In SAR ADCs, the noise contributions from the sampling network, comparator regeneration process and capacitive DAC switching significantly influence the achievable SNR. A higher SNR value indicates that the desired signal is significantly stronger than the background noise, resulting in improved signal fidelity and a more precise digital representation of the analog input signal. Consequently, achieving a high SNR is essential in applications including wireless communication receivers, high-resolution sensor interfaces, medical instrumentation, and high-speed data acquisition systems.

In the design of high-performance SAR ADCs, improving SNR requires careful optimization of several circuit blocks, including the sampling capacitor network, comparator architecture, reference voltage stability and DAC switching scheme. Reducing noise contributions and improving circuit linearity can enhance dynamic performance and lead to higher effective resolution.

Signal-to-Noise-and-Distortion Ratio (SNDR)

The Signal-to-Noise-and-Distortion Ratio (SNDR) is an important dynamic performance metric used to assess the accuracy and linearity of ADC under time-varying input

conditions. Unlike SNR, which considers only the noise components present in the system, SNDR accounts for both random noise and nonlinear distortion components that arise during the analog-to-digital conversion process. Consequently, SNDR offers a more complete and practical evaluation of ADC performance under real operating conditions [1, 4].

SNDR is defined as the ratio of the fundamental signal power to the combined power of all unwanted spectral components, including noise and harmonic distortion, within the specified frequency range. Mathematically, SNDR can be expressed as

$$SNDR = 10 \log_{10} \left(\frac{P_{signal}}{P_{noise} + P_{distortion}} \right) dB \quad (1.8)$$

where P_{signal} represents the power of the fundamental input signal, P_{noise} represents the total noise power excluding harmonic components and $P_{distortion}$ represents the power contained in harmonic distortion components generated by nonlinearities in the ADC.

In practical testing environments, SNDR is generally determined through spectral analysis methods. A sinusoidal input signal is applied to the ADC, and the resulting digital output samples are analyzed using FFT to generate the frequency spectrum. The fundamental frequency component appears as the dominant peak in the spectrum, while the remaining spectral components represent noise and distortion. The SNDR is subsequently obtained by comparing the power of the fundamental frequency component with the total power of all remaining spectral components within the ADC bandwidth.

Harmonic distortion components arise due to nonlinearities in the ADC circuitry, including imperfections in the comparator, capacitor mismatch in the DAC array, finite settling errors and switching nonidealities [6, 7]. These nonlinear effects generate harmonics at integer multiples of the input frequency, such as $2f_{in}$, $3f_{in}$, and higher-order components. These harmonics contribute to the distortion power and therefore degrade the SNDR value.

SNDR is particularly important because it directly determines ENOB of the ADC, which represents the practical resolution achieved by the converter under dynamic conditions.

Total Harmonic Distortion (THD)

Total Harmonic Distortion (THD) is a significant dynamic performance metric used to assess the linearity characteristics of an ADC. It measures the extent to which harmonic components are generated when a pure sinusoidal input signal is provided to the converter. Ideally, when a sinusoidal signal is digitized by a perfectly linear ADC, the output spectrum should contain only the fundamental frequency component corresponding to the input signal. However, due to various circuit non-idealities present in practical ADC implementations, extra frequency components emerge in the output spectrum at integer multiples of the fundamental frequency [1-4]. These components are known as harmonic distortion components.

The primary sources of harmonic distortion in ADCs include nonlinearities in the comparator, mismatch in the capacitive DAC array, finite settling errors in the switching network, non-ideal reference voltages and device-level nonlinear behavior of transistors in scaled CMOS technologies. These nonlinearities distort the shape of the reconstructed waveform and introduce spectral components at frequencies such as $2f_{in}$, $3f_{in}$, $4f_{in}$, and so on, where f_{in} represents the fundamental input signal frequency.

Total Harmonic Distortion quantifies the cumulative effect of these harmonic components relative to the fundamental signal. Mathematically, THD is defined as the ratio of the combined power of all harmonic components to the power of the fundamental frequency component. It is commonly expressed in decibels (dB) and can be calculated as [2]

$$THD = 10 \log_{10} \left(\frac{P_2 + P_3 + P_4 + \dots + P_n}{P_1} \right) \quad (1.9)$$

Where P_1 represents the power of the fundamental signal component, and $P_2, P_3, P_4, \dots, P_n$ represent the power of the second, third, fourth and n th order harmonic components, respectively.

In practical measurement procedures, THD is typically determined using frequency-domain analysis. A sinusoidal test signal is supplied to the ADC, and the resulting digital output samples are processed using FFT. The resulting spectrum displays the fundamental frequency component as the dominant peak, while harmonic distortion components appear at multiples of the input frequency [6-8]. The THD is then calculated by summing the power of the significant harmonic peaks and comparing it to the fundamental signal power.

A lower THD value indicates better linearity and reduced distortion, meaning that the ADC more accurately preserves the shape and spectral purity of the input signal. Conversely, a high THD value indicates significant nonlinear distortion, which can degrade signal quality and introduce interference in communication systems or measurement errors in precision instrumentation.

In the design of high-performance SAR ADCs, minimizing THD requires careful attention to several design aspects, including accurate capacitor matching in the DAC array, high-gain and low-offset comparator design, optimized switching algorithms, and symmetrical layout techniques to reduce parasitic mismatches. Additionally, ensuring sufficient settling time in the DAC and minimizing reference voltage fluctuations can significantly improve harmonic performance.

THD is especially significant in applications such as wireless communication receivers, high-resolution data acquisition systems, audio processing equipment, and precision instrumentation, where high signal fidelity and spectral purity are essential [4]. Therefore, optimizing THD alongside other dynamic parameters such as SNR and SNDR is important for achieving high overall performance in modern ADC architectures.

Spurious-Free Dynamic Range (SFDR)

Spurious-Free Dynamic Range (SFDR) is a key dynamic performance parameter used to evaluate the spectral purity of an ADC. It measures the ability of the converter to distinguish a desired signal from unwanted spurious spectral components generated during the conversion process. SFDR is defined as the ratio of the amplitude of the fundamental signal component to the amplitude of the largest spurious spectral component appearing in the output spectrum. [2, 8].

Mathematically, SFDR can be expressed as

$$SFDR = 20 \log_{10} \left(\frac{A_{signal}}{A_{spur}} \right) dB \quad (1.10)$$

where A_{signal} represents the amplitude of the fundamental input signal and A_{spur} represents the amplitude of the largest unwanted spurious component in the spectrum.

The spurious components, commonly referred to as spurs, may arise from several sources including harmonic distortion, intermodulation distortion, clock feedthrough, switching transients in the DAC, capacitor mismatch, and nonlinearities in the comparator or other circuit elements. These spurs appear at frequencies different from the fundamental frequency and can significantly degrade the quality of the digitized signal.

In practice, SFDR is typically measured using frequency-domain analysis. A sinusoidal input signal is applied to the ADC, and the digital output samples are processed using FFT to obtain the output spectrum. The fundamental signal appears as the dominant peak at the input frequency f_{in} , while harmonic distortion components appear at integer multiples such as $2f_{in}$, $3f_{in}$, and so forth. Other spurious tones may also appear due to nonlinear circuit behavior or interference. The SFDR is determined by identifying the largest spur in the spectrum and determining the ratio between the amplitude of the fundamental component and that of the spur signal [5].

Unlike SNR and SNDR, which consider the total integrated noise and distortion power, SFDR focuses specifically on the worst-case spectral component. This makes SFDR particularly important in applications where a single unwanted tone can interfere with signal detection or corrupt adjacent communication channels.

A higher SFDR value indicates superior spectral purity, meaning that the ADC produces fewer unwanted spurious tones and can accurately represent the input signal without introducing strong interfering components. Conversely, a low SFDR indicates significant distortion or interference in the output spectrum.

SFDR is especially critical in applications such as wireless communication receivers, radar systems, spectrum analyzers and high-speed data acquisition systems, where unwanted spectral components can degrade system performance by interfering with neighboring frequency channels. In these systems, the ADC must maintain a large dynamic range so that weak signals can be detected even in the presence of strong nearby signals [1].

In SAR ADC design, improving SFDR requires minimizing nonlinear distortion and reducing switching-induced artifacts. Techniques such as precise capacitor matching in the DAC array, optimized DAC switching algorithms, high-gain low-offset comparator design, and careful layout techniques to minimize parasitic coupling can significantly improve SFDR performance. Additionally, ensuring stable reference voltages and minimizing clock jitter are important factors in maintaining high spectral purity.

Overall, SFDR is an essential parameter for evaluating the dynamic linearity of an ADC and is widely used alongside other performance metrics such as SNR, SNDR, THD, and ENOB to characterize the dynamic behavior of high-performance data converters.

Effective Number of Bits (ENOB)

The Effective Number of Bits (ENOB) is an important dynamic performance metric used to evaluate the practical resolution of an ADC. While the nominal resolution of an ADC

is determined by the number of bits used for representing the digital output, the actual performance of the converter is often degraded by various non-ideal effects such as thermal noise, quantization noise, circuit nonlinearities, comparator offset, capacitor mismatch, reference voltage fluctuations and clock jitter. As a result, the effective resolution achievable in real operating conditions is usually lower than the theoretical resolution specified by the converter design [1].

ENoB provides a quantitative measure of the usable resolution of an ADC by considering the combined effects of distortion present in the output signal. It is derived from the SNDR, which includes both random noise components and harmonic distortion effects. By comparing the measured SNDR with the theoretical signal-to-noise ratio of an ideal converter, ENoB indicates the number of bits that effectively participate in accurate signal conversion. The relationship between ENoB and SNDR is given by

$$ENoB = \frac{SNDR - 1.76}{6.02} \quad (1.11)$$

where SNDR is expressed in decibels (dB), 1.76 dB represents the offset constant associated with quantization noise in an ideal converter and 6.02 dB corresponds to the increase in signal-to-noise ratio obtained for each additional bit of resolution.

This equation shows that each additional effective bit improves the SNDR by approximately 6 dB. Conversely, any reduction in SNDR due to noise or distortion results in a corresponding decrease in ENoB.

For example, if a converter has a measured SNDR of 62 dB, the effective number of bits can be calculated as

$$ENoB = \frac{62 - 1.76}{6.02} \approx 10 \text{ bits} \quad (1.12)$$

This indicates that although the ADC may be designed as a higher-resolution converter, its effective performance corresponds to that of an ideal 10-bit ADC under the given operating conditions.

ENoB is typically determined through spectral analysis using FFT of the digital output signal when a sinusoidal input is applied [3]. From the FFT spectrum, the SNDR is calculated by comparing the power associated with the fundamental signal component with the combined power of noise and distortion components. The ENoB value is then derived using the relationship above.

This parameter is widely used as a comprehensive performance indicator because it captures the combined influence of multiple dynamic error sources in the converter. In high-performance SAR ADCs, factors such as capacitor mismatch in the DAC array, comparator noise, switching transients, and incomplete DAC settling can reduce SNDR and therefore lower the effective resolution [5].

Improving ENoB in SAR ADC architectures requires careful optimization of several design aspects, including high-accuracy capacitor arrays, low-noise comparator circuits, efficient DAC switching schemes, and stable reference voltage generation. Proper layout techniques and calibration methods are also commonly employed to mitigate mismatch and reduce distortion.

Overall, ENoB provides a practical and widely accepted metric for assessing the real-world performance of ADCs. Unlike nominal resolution, which only reflects the theoretical capability of the converter, ENoB directly reflects the usable precision of the ADC when operating under realistic signal conditions, making it a critical parameter in applications such as communication systems, precision measurement equipment, sensor interfaces and high-speed data acquisition systems [8].

1.2.3 Static Characteristics

Static characteristics describe the performance of an ADC when the input signal is constant or slowly varying with time. Unlike dynamic parameters, which evaluate the behavior of the converter under rapidly changing signals, static characteristics focus on the accuracy, linearity, and precision of the conversion process. These parameters provide insight into how closely the ADC digital output accurately matches the corresponding analog input value under steady-state conditions [1].

In static performance evaluation, the input voltage is gradually varied across the full operating range of the ADC, and the resulting digital output codes are observed. By analyzing the relationship between the applied input voltage and the generated digital codes, it is possible to identify deviations from ideal behavior caused by circuit imperfections. These deviations can arise from factors such as comparator offset, capacitor mismatch in the DAC array, finite reference voltage accuracy, switching errors, and parasitic effects in the circuit implementation [3, 4].

The primary objective of static characterization is to evaluate the linearity and accuracy of the ADC transfer function. In an ideal ADC, the transfer characteristic follows a perfectly linear correspondence between the analog input voltage and the resulting digital output code [5]. However, practical ADCs often exhibit deviations from this ideal linear behavior due to device mismatches and circuit non-idealities.

Various key parameters are utilized to characterize the static performance of ADCs, including offset error, gain error, DNL and INL. Each of these parameters provides information about specific types of errors that may occur during the conversion process.

Offset Error

Offset error is one of the fundamental static performance parameters used to evaluate the accuracy of an ADC. It represents the difference between the actual ADC transfer

characteristic and the ideal transfer characteristic at the lower end of the input voltage range. In simpler terms, offset error indicates the amount by which the input voltage must deviate from zero in order to produce the first transition in the digital output code [2].

In an ideal ADC, the first transition between digital output codes should occur when the input voltage reaches half of the LSB above the minimum input voltage. This ensures that the quantization intervals are symmetrically distributed around each digital code. However, due to practical circuit imperfections, the actual transition point may shift either above or below this ideal value. This shift is referred to as offset error [3].

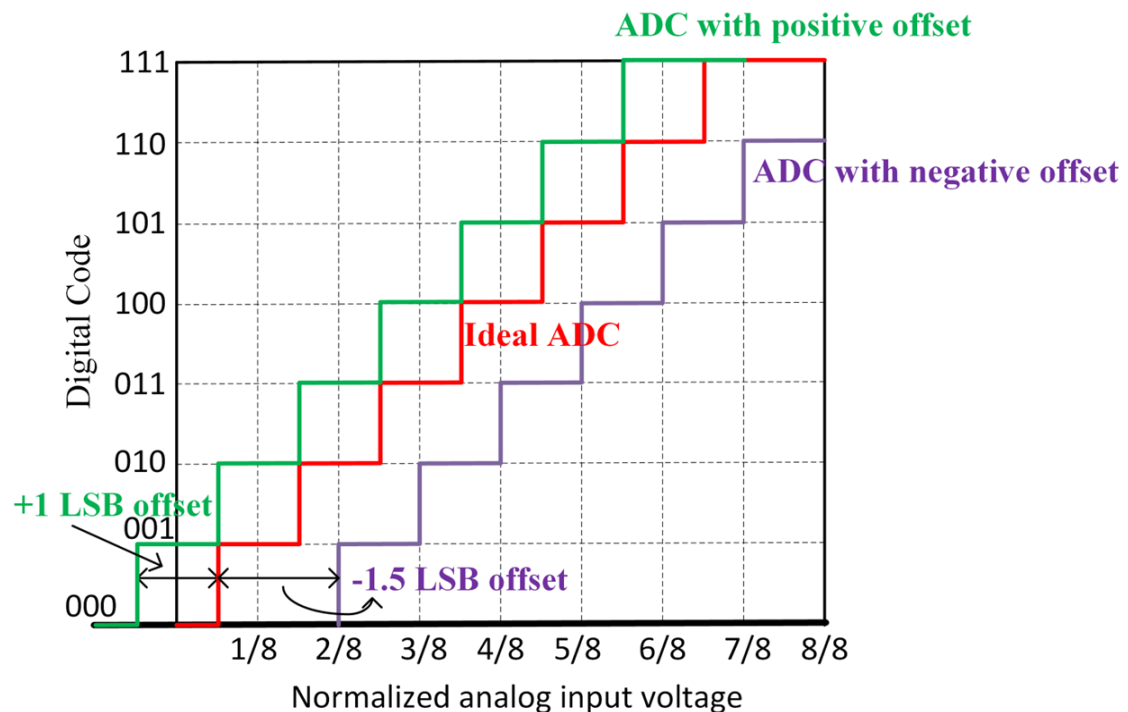


Fig. 1.4 Positive and Negative Offset Error

Mathematically, Offset error is defined as the deviation between the actual and ideal transition voltages corresponding to the first code transition. It is typically expressed in units of LSB or sometimes in volts [5].

$$\text{Offset Error} = V_{\text{actual transition}} - V_{\text{ideal transition}} \quad (1.13)$$

Where $V_{\text{actual transition}}$ represents the measured input voltage at which the first code transition occurs, and $V_{\text{ideal transition}}$ represents the ideal transition voltage (normally equal to $\frac{1}{2}$ LSB).

Offset error in an ADC can be classified into positive offset error and negative offset error depending on the direction of the shift of the transfer characteristic relative to the ideal response.

Offset error occurs when the first code transition point deviates from its ideal position, which ideally should occur at $\frac{1}{2}$ LSB above the minimum input voltage. Due to imperfections in the comparator, reference voltage circuitry, or capacitor mismatches in the DAC, the transition point may shift either toward higher or lower input voltage values [7].

Offset error introduces a constant shift in the entire ADC transfer curve without affecting its slope. This means that all digital codes are displaced by the same amount along the input voltage axis. As a result, although the spacing between quantization levels remains unchanged, the digital output codes no longer correspond exactly to the correct input voltage levels.

Several circuit-level factors contribute to offset error in practical ADC implementations. One of the major sources is comparator offset voltage, which arises due to mismatch between the transistors in the differential input pair of the comparator. Even small mismatches in transistor dimensions or threshold voltages can lead the comparator to switch at input voltage levels that differ slightly from the intended values. Other contributing factors include reference voltage inaccuracies, parasitic capacitances in the sampling network, charge injection during switching and mismatches in the capacitive DAC array [8].

In SAR ADC architectures, offset error is particularly influenced by the comparator design, since the comparator determines the decision threshold during each conversion step. If the comparator exhibits a significant offset voltage, the comparison results may shift consistently, leading to systematic errors in the digital output codes.

Although offset error affects the absolute accuracy of the converter, it is often considered a correctable error. Calibration techniques such as digital offset calibration, auto-zeroing, and chopping techniques can be used to compensate for offset errors [9]. In many systems, offset error is also removed during post-processing by subtracting the measured offset from the digital output.

From a system perspective, minimizing offset error is important in applications demanding high measurement precision, such as sensor interfaces, instrumentation systems, biomedical signal acquisition, and precision control systems. Careful device matching, symmetrical layout techniques, and low-offset comparator design are commonly used to reduce offset error in high-performance ADCs.

Overall, offset error gives a systematic deviation of the ADC transfer characteristic at the zero-input condition, and its reduction is essential for achieving accurate analog-to-digital conversion in precision electronic systems.

Gain Error

Gain error is an important static performance parameter used to evaluate the accuracy of an ADC. It denotes the difference in the slope of the actual ADC transfer characteristic compared to the ideal characteristic after compensating for the offset error. In other words, gain error indicates how much the scaling of the input to output relationship differs from the ideal conversion behavior.

In an ideal ADC, the digital output codes increase linearly with the voltage across the entire input range. The slope of this transfer curve is determined from the ratio of the full-

scale input voltage range to the total number of quantization levels (2^n). Under ideal operating conditions, the maximum digital output code is obtained precisely when the input signal attains the full-scale reference voltage [4].

However, in practical implementations, various circuit non-idealities can cause the slope of the actual transfer function to differ slightly from the ideal slope. This deviation results in a scaling error, meaning that the digital output values do not accurately represent the input voltage across the entire range. This error is referred to as gain error [6].

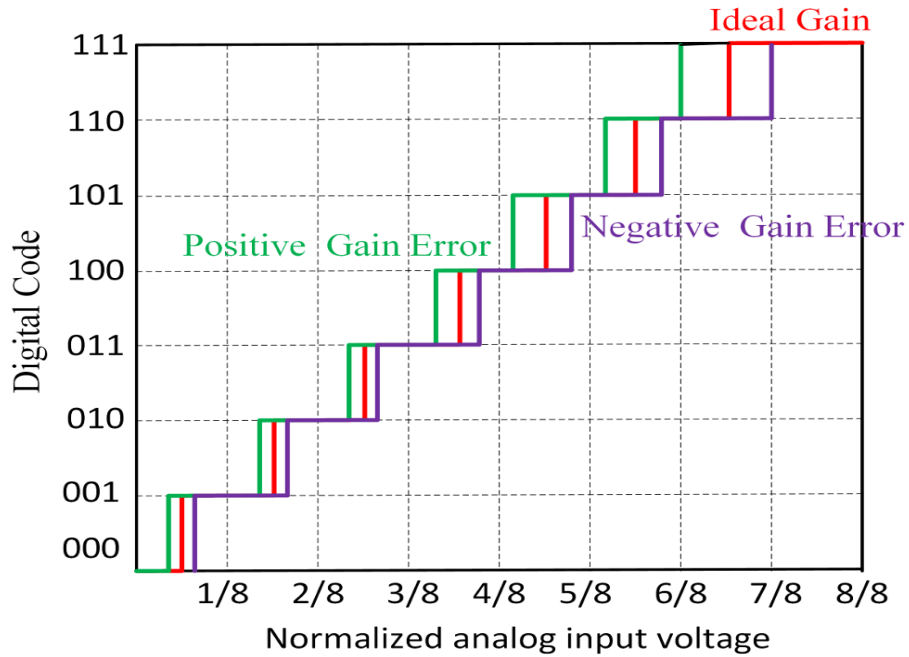


Fig. 1.5 Positive and Negative Gain Error

Gain error is typically measured after correcting for offset error so that the comparison between the ideal and actual transfer characteristics reflects only the difference in slope. Mathematically, gain error can be expressed as [7]

$$\text{Gain Error} = \frac{V_{\text{actual full-scale}} - V_{\text{ideal full-scale}}}{V_{\text{ideal full-scale}}} \quad (1.14)$$

where $V_{\text{actual full-scale}}$ represents the input voltage corresponding to the maximum digital output code in the practical ADC, and $V_{\text{ideal full-scale}}$ represents the ideal full-scale input voltage.

Gain error is often expressed in LSB units, percentage of full scale or in millivolts (mV) depending on the specific format used in the ADC characterization [2]. In an ideal ADC, the digital output codes increase linearly with the input voltage and the maximum digital output code is reached exactly when the input voltage reaches the full-scale reference voltage. However, due to practical circuit non idealities such as reference voltage inaccuracies, capacitor mismatch in the DAC array, comparator gain limitations, and circuit parasitics, the slope of the transfer characteristic may become either steeper or flatter than the ideal slope [5, 6]. Depending on the direction of deviation, gain error can be classified as either positive gain error or negative gain error.

Several circuit-level factors contribute to gain error in practical ADC designs. One major source is inaccuracy in the reference voltage, since the reference voltage defines the full-scale range of the converter. Any variation in the reference voltage directly affects the slope of the transfer characteristic. Another common source is mismatch in the CDAC array [7], particularly in SAR ADC architectures. Capacitor mismatches alter the effective weighting of each bit, which leads to deviations in the overall conversion gain.

Other contributing factors include finite settling errors in the DAC switching network, temperature variations affecting device parameters, and non-ideal behavior of analog front-end circuits such as amplifiers or sampling networks [8, 9]. These effects can collectively cause the transfer function to stretch or compress relative to the ideal characteristic.

In the graphical representation of the ADC transfer function, gain error appears as a tilt in the transfer curve, meaning that the slope differs from the ideal slope even though the first

transition point is aligned after offset correction. As the input voltage increases toward full scale, the deviation between the ideal and actual curves becomes progressively larger.

Unlike nonlinear errors such as INL and DNL, gain error is generally considered a systematic error and can often be corrected using calibration techniques. Many modern ADC systems employ digital gain calibration, where the output codes are scaled using correction factors to compensate for gain mismatch. Proper reference voltage design, accurate capacitor matching, and careful circuit layout can also help reduce gain error during the design stage.

In high-accuracy applications such as instrumentation systems, sensor interfaces, biomedical measurement equipment and high-resolution data acquisition systems, minimizing gain error is essential for maintaining accurate signal conversion across the entire input range. Therefore, careful design of the reference generation circuit, CDAC network and sampling circuitry is required to ensure minimal gain deviation [9].

Overall, gain error reflects the difference in the scaling factor between the ideal and actual ADC transfer functions, and its reduction is necessary to achieve high accuracy in analog-to-digital conversion systems.

Differential Non-Linearity (DNL)

Differential Non-Linearity (DNL) is an important static performance parameter used to evaluate the linearity of an ADC. It measures the variation of the actual step size between two neighboring digital output codes relative to the ideal step size of one LSB [5]. In an ideal ADC, each quantization step corresponds exactly to one LSB of the input voltage range. However, due to circuit non-idealities and component mismatches, the original step width may differ slightly from this ideal value.

DNL therefore measures how uniformly the analog input range is divided into quantization intervals [6]. If the quantization steps are not uniform, certain codes may represent larger

or smaller voltage intervals than expected, which leads to inaccuracies in the conversion process.

Mathematically, DNL can be expressed as

$$DNL = \frac{V_{actual\ step} - V_{ideal\ step}}{V_{LSB}} \quad (1.15)$$

where $V_{actual\ step}$ represents the measured voltage difference between two consecutive code transition points, $V_{ideal\ step}$ represents the ideal step width equal to one LSB, and V_{LSB} denotes the least significant bit voltage.

When the value of DNL is zero, the step size exactly matches the ideal LSB width. A positive DNL value signifies that the actual code step is greater than one LSB, while a negative DNL value indicates that the step size is less than one LSB [9, 10].

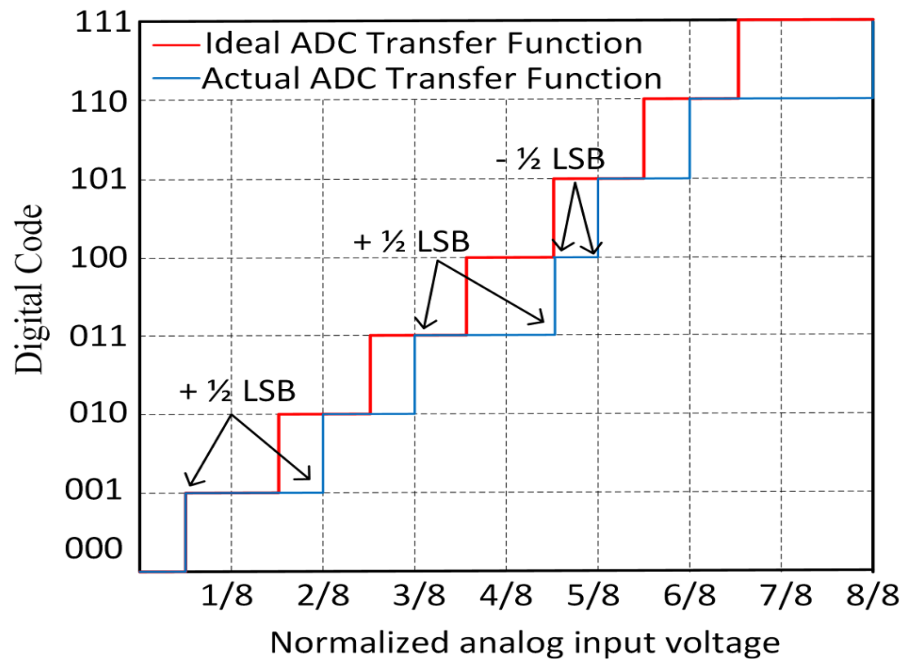


Fig. 1.6 ADC Transfer Function with DNL Error

The magnitude of DNL provides insight into the uniformity of the ADC transfer characteristic. If the DNL value lies within the range -1 LSB to $+1$ LSB, the ADC is considered monotonic, meaning that the output codes increase sequentially without skipping any codes [2, 4]. However, if the DNL value exceeds ± 1 LSB, it may lead to the occurrence of missing codes, where certain digital output values never appear for any input voltage. Missing codes degrade the resolution and accuracy of the converter and are generally undesirable in precision applications.

Several circuit-level factors contribute to DNL errors in practical ADC implementations. In SAR ADC architectures, one of the most significant contributors is capacitor mismatch in the CDAC array. Since each capacitor represents a specific binary weight, any mismatch alters the effective voltage step produced during the successive approximation process. This mismatch results in non-uniform quantization intervals, which directly manifests as DNL error [6].

Other sources of DNL include comparator offset, charge injection during switching, parasitic capacitances in the sampling network, incomplete DAC settling and variations in the reference voltage. These factors disturb the ideal voltage division during the conversion process and lead to irregular spacing between code transitions [15, 28].

DNL is typically measured using a slow ramp input signal or a histogram testing method, where the input voltage is varied across the full-scale range, and the frequency of occurrence of each digital output code is measured. By analyzing the distribution of output codes, it is possible to determine whether certain codes appear more frequently (indicating larger step widths) or less frequently (indicating smaller step widths) [16].

Maintaining low DNL is essential in applications demanding high linearity performance and precision, such as instrumentation systems, sensor interfaces, communication receivers, and high-resolution data acquisition systems. In high-performance SAR ADC designs, DNL errors can be minimized through techniques such as accurate capacitor

matching, layout symmetry, calibration methods, and optimized DAC switching schemes [17].

Overall, DNL provides an important measure of the local linearity of the ADC transfer function, reflecting how evenly the analog input range is quantized into discrete digital output codes.

Integral Non-Linearity (INL)

Integral Non-Linearity (INL) is an important static performance parameter used to evaluate the overall linearity of an ADC. It measures the variation of the actual ADC transfer characteristic from the ideal straight-line relationship between the analog input voltage and the corresponding digital output code [1-4]. Unlike DNL, which measures the variation in step size between successive digital codes, INL represents the cumulative deviation of the transfer curve over the entire input range.

In an ideal ADC, the digital output codes increase linearly with the input voltage, producing a perfectly straight transfer curve when plotted against the analog input signal. However, practical ADC implementations exhibit deviations from this ideal behavior due to various circuit imperfections such as capacitor mismatch, comparator offset, incomplete DAC settling, parasitic capacitances, switching nonlinearities and variations in the reference voltage [35]. These imperfections cause the transfer characteristic to bend or shift away from the ideal straight-line characteristics, resulting in INL error.

Mathematically, INL is defined as the deviation between the actual transition point of a particular code and the corresponding transition point predicted by the ideal transfer curve. This deviation is typically expressed in units of LSB and can be written as

$$INL_k = \frac{V_{actual}(k) - V_{ideal}(k)}{V_{LSB}} \quad (1.16)$$

where $V_{\text{actual}}(k)$ represents the measured input voltage associated with the k^{th} code transition, $V_{\text{ideal}}(k)$ represents the ideal transition voltage of that code determined from the ideal transfer characteristic, and V_{LSB} is the voltage value corresponding to one LSB.

INL is usually evaluated using either the endpoint method or the best-fit line method. In the endpoint method, the ideal straight line is drawn between the first and last transition points of the ADC transfer curve [22-25]. In the best-fit method, a least-squares line is fitted through all transition points to minimize the overall error. The INL value is then determined as the maximum deviation of any code transition from this reference line.

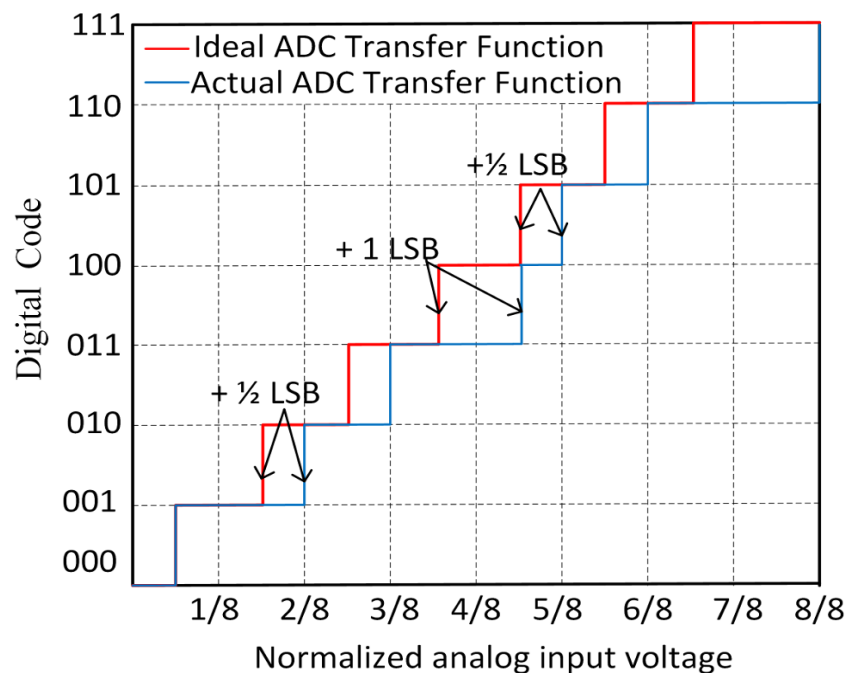


Fig. 1.7 ADC Transfer Function with INL Error

A smaller INL value indicates that the ADC transfer characteristic closely follows the ideal linear behavior. Conversely, a large INL value indicates significant nonlinearity in the converter, which can degrade the accuracy of signal representation. Unlike offset and gain errors, which are systematic and often correctable through calibration, INL errors are

more complex because they arise from distributed nonlinearities across the entire conversion range [17].

In SAR ADC architectures, INL is strongly influenced by the matching accuracy of the CDAC array. Since each capacitor represents a binary weight in the successive approximation process, even small mismatches can accumulate and produce nonlinearities in the output transfer curve. Additionally, comparator decision errors and incomplete DAC settling during high-speed operation can further contribute to INL degradation [19].

The impact of INL becomes particularly significant in applications that demand high accuracy and precision, such as instrumentation systems, medical devices, industrial measurement equipment and high-resolution data acquisition systems. Large INL values can introduce distortion into the reconstructed signal and decrease the effective accuracy of the converter.

Therefore, minimizing INL is a critical objective in the design of high-performance SAR ADCs. Techniques such as capacitor layout optimization, common-centroid layout structures, calibration algorithms, digital correction techniques and improved comparator design are often employed to reduce nonlinearity and improve the overall accuracy of the converter [9, 20, 21].

Overall, INL provides a comprehensive evaluation of the global linearity of the ADC transfer function, capturing the cumulative effects of all nonlinear error sources present in the converter.

Monotonicity

Monotonicity is an important static characteristic of an ADC that describes the behavior of the digital output codes with respect to changes in the analog signal. An ADC is said to be monotonic if its digital output code either increases or remains constant when the input voltage increases [2, 3]. In other words, the output of the converter must never decrease

when the input signal increases. This property ensures that the ADC produces a non-decreasing transfer characteristic over the entire input voltage range.

In an ideal ADC, the transfer function consists of a staircase-shaped curve where each step corresponds to a quantization level [5, 20]. As the input voltage increases, the output code transitions sequentially from one level to the next higher level. Therefore, the digital output always moves in the forward direction without reversing. Monotonicity guarantees that the conversion process maintains a consistent relationship between the analog input signal and the digital output code [18].

In practical ADC implementations, monotonic behavior is strongly related to DNL performance. If the DNL of every code is greater than -1 LSB, the ADC is guaranteed to be monotonic. However, if the DNL becomes less than -1 LSB, the step size between adjacent codes may become negative, leading to a situation where the output code decreases even though the input voltage increases. This phenomenon results in non-monotonic behavior and may cause instability in signal processing systems [2, 4].

Monotonicity is particularly important in applications where the ADC is used in closed-loop control systems, digital feedback loops or measurement systems [18, 20, 48]. In such systems, a non-monotonic converter can introduce unpredictable behavior because a small increase in the input signal may produce a lower digital output value. This can cause oscillations or instability in control loops and degrade system reliability.

In SAR ADC architectures, monotonicity is largely influenced by the accuracy of the CDAC array, since the DAC generates the reference voltages used for comparison during the successive approximation process [40, 43]. If capacitor mismatches are large, the voltage steps generated during the conversion process may not follow the correct binary weighting, resulting in irregular step sizes. This can lead to negative DNL values and consequently violate the monotonic property.

Other factors that can affect monotonicity include comparator offset, switching charge injection, parasitic capacitances, and incomplete DAC settling during high-speed operation [39, 44]. Careful design techniques are therefore required to ensure monotonic behavior in high-resolution SAR ADCs.

To maintain monotonicity, designers often employ precision capacitor matching, common-centroid layout techniques, calibration methods, and optimized DAC switching algorithms [9, 18, 34, 44]. These approaches help maintain uniform step sizes and prevent code reversal during the conversion process.

Monotonicity is often considered a minimum requirement for reliable ADC operation, especially in systems where the converter output is directly used for control or decision-making processes. Even if other linearity parameters such as INL and DNL are not perfect, maintaining monotonic behavior ensures that the ADC produces stable and predictable conversion results [4, 7].

Overall, monotonicity guarantees that the ADC transfer function remains non-decreasing throughout the input range, thereby preserving the accurate relationship between the analog input signal and the corresponding digital output code. This characteristic is essential for ensuring reliable operation in a wide range of analog-to-digital conversion applications.

1.2.4 Figure of Merit (FoM)

The Figure of Merit (FoM) is a widely used performance metric that enables quantitative comparison of different ADC architectures in terms of energy efficiency and conversion performance [23]. Since ADCs may operate at different resolutions, sampling rates, and power levels, direct comparison of parameters such as power consumption alone does not provide a fair assessment of performance [24]. Therefore, the FoM serves as a normalized performance metric that accounts for the relationship between power consumption, resolution, and sampling frequency.

In modern mixed-signal systems, particularly those used in wireless communication devices, sensor interfaces, biomedical electronics and IoT platforms, minimizing energy consumption while maintaining high accuracy is a key design objective [37, 48]. FoM provides a convenient method to evaluate how efficiently an ADC converts analog signals into digital data with respect to energy usage.

Several FoM formulations have been proposed in the literature, among which the Walden FoM and the Schreier FoM are the most commonly used metrics for evaluating ADC performance.

Walden Figure of Merit

The Walden Figure of Merit is widely used for evaluating energy in Nyquist-rate ADCs, particularly SAR and flash ADC architectures [37, 51]. This metric represents the energy consumed per conversion step, providing a direct measure of how much energy the converter requires to resolve one quantization level.

The Walden FoM is defined as

$$FoM_{walden} = \frac{Power}{2^{ENoB} * f_s} \quad (1.17)$$

where Power represents the total power consumed by ADC, ENoB denotes the effective number of bits, f_s is the sampling frequency.

The term 2^{ENoB} corresponds to the total number of quantization levels in the converter, and therefore the denominator represents the total number of conversion steps processed/second. The Walden FoM therefore quantifies the energy required to perform a single quantization step.

The units of Walden FoM are typically expressed in Joules per conversion-step, and in modern low-power ADC designs the values are usually reported in femto-Joules per conversion-step (fJ/conversion-step) [23, 53].

A lower Walden FoM value indicates higher energy efficiency, meaning that the ADC consumes less energy to perform each conversion operation. Over the past decades, advances in CMOS technology and circuit design techniques have enabled continuous improvement in Walden FoM, particularly for SAR ADC architectures, which are known for their excellent power efficiency [51].

Schreier Figure of Merit

Another important performance metric used for ADC comparison is the Schreier Figure of Merit, which incorporates both dynamic range and power efficiency into a single parameter. Unlike the Walden FoM, which focuses primarily on energy per conversion step, the Schreier FoM evaluates the trade-off between signal quality and power consumption [23].

The Schreier FoM is defined as

$$FoM_{schreier} = SNDR + 10 \log_{10} \left(\frac{f_s}{Power} \right) \quad (1.18)$$

where SNDR represents the signal-to-noise-and-distortion ratio, f_s denotes the sampling frequency, Power represents the power consumption of the ADC.

The Schreier FoM is expressed in decibels (dB) and provides a measure of how effectively the ADC achieves high dynamic performance relative to its power consumption. In contrast to the Walden FoM, higher Schreier FoM values indicate better performance, as they correspond to higher signal quality achieved with lower power consumed [53].

This metric is particularly useful when evaluating high-resolution converters, where maintaining high SNR while minimizing power consumption is critical.

Importance of FoM in Modern ADC Design

In recent years, the rapid growth of energy-constrained electronic systems such as wearable devices, implantable medical sensors, wireless sensor networks, and edge-computing nodes has significantly increased the demand for ultra-low-power ADC architectures [44-47]. In such applications, the energy efficiency of the data conversion process directly impacts battery life and overall system reliability.

SAR ADCs have become one of the most power-efficient architectures for medium-resolution and moderate-speed applications. This is primarily due to their charge-redistribution DAC structure, absence of high-power operational amplifiers, and highly digital implementation, which allows them to benefit from CMOS technology scaling [48, 50].

Modern SAR ADC designs aim to achieve extremely low FoM values through several architectural and circuit-level techniques, including [48, 49]:

- energy-efficient DAC switching schemes,
- optimized comparator architectures,
- asynchronous SAR logic,
- capacitor array scaling,
- reference voltage optimization,
- calibration techniques to improve linearity without increasing power consumption.

By minimizing switching energy, improving comparator efficiency and reducing digital control overhead, designers can significantly improve the FoM of SAR ADCs while maintaining high SNDR and ENOB performance.

1.3 Literature Survey

The continuous evolution of modern electronic technologies has greatly accelerated the deployment of intelligent and interconnected systems across a broad range of applications. In particular, the widespread adoption of IoT devices, wearable healthcare monitors, portable sensor nodes, and edge-computing platforms has created a growing need for efficient data acquisition systems [48]. These applications rely on electronic interfaces that can accurately capture analog signals from physical environments—such as temperature, pressure, biological activity, and environmental parameters—and convert them into digital data suitable for processing, storage, or transmission. Consequently, the development of energy-efficient and high-precision signal conversion circuits has become essential to support the reliable operation of such systems while maintaining minimal power consumption [21, 52]. As a result, ADCs have become one of the most critical components in mixed-signal integrated circuits. In many IoT and sensor-oriented systems, the ADC serves as the main interface between real-world analog signals and digital processing circuits, making its performance critical to overall system operation. As a result, there is a growing need for ADC architectures capable of providing high resolution, low power consumption, compact silicon area, and dependable performance under low supply voltages in advanced CMOS technologies [1, 54].

Analog-to-digital conversion plays a central role in numerous applications including wireless communication systems, biomedical instrumentation, environmental monitoring, industrial automation and portable consumer electronics [48]. In these systems, physical quantities such as temperature, pressure, sound and electromagnetic waves are initially transformed into electrical analog signals by sensors. These analog signals must then be digitized accurately so that they can be processed, stored, or transmitted by digital systems. Over the past several decades, significant research efforts have been devoted to developing ADC architectures that meet increasingly demanding requirements in terms of conversion speed, resolution, power efficiency, and integration density [48, 55].

Among the various ADC architectures, SAR ADC has emerged as one of the most attractive solutions for moderate-to-high resolution applications requiring excellent power efficiency. The SAR ADC architecture offers several advantages including simple circuit structure, scalability with CMOS technology, and reduced dependence on power-hungry analog blocks such as operational amplifiers [47, 60]. As a result, SAR ADCs have become widely adopted in IoT devices, sensor interfaces, and battery-powered electronic systems. Continuous advancements in circuit techniques and digital calibration methods have further enhanced the performance capabilities of SAR ADCs, enabling them to achieve higher sampling rates and improved energy efficiency.

1.3.1 Comparators

In SAR ADC, the comparator serves as the primary decision-making circuit responsible for generating the digital output bits during each conversion cycle [41]. Since a SAR ADC performs multiple comparison operations—typically equal to the number of bits in the converter resolution—the comparator is activated repeatedly during each conversion process. Consequently, the energy consumed by the comparator accumulates over multiple comparison cycles and becomes a major contributor to the overall power dissipation of the ADC. In low-power applications such as IoT devices, wireless sensor networks, biomedical monitoring systems, and portable instrumentation, where energy efficiency is a primary design objective, optimizing the comparator architecture is essential for improving the overall performance of the ADC [46].

In many practical SAR ADC implementations, the comparator alone may account for a substantial portion of the total power dissipation, sometimes approaching 40–60% of the overall converter power budget [47]. This high contribution arises because the comparator must operate at high speed while maintaining sufficient sensitivity to detect very small voltage differences generated by the capacitive DAC. Furthermore, the comparator must exhibit low input-referred noise, minimal offset voltage, and robust operation across process, voltage, and temperature (PVT) variations [48, 65]. These requirements create

significant design challenges, particularly in modern CMOS technologies where supply voltages continue to decrease due to technology scaling.

One of the most widely used comparator architectures in high-speed ADC design is the Strong ARM latch comparator [31, 32, 66, 67], originally introduced in the early 1990s as a sense-amplifier-based comparator for high-speed digital circuits. This architecture has gained widespread popularity due to its high-speed regenerative operation, compact structure and zero static power consumption, as it relies entirely on dynamic operation controlled by a clock signal [21–23]. The Strong ARM latch is composed of a differential input stage followed by cross-coupled regenerative transistors that quickly amplify the input voltage difference to full digital output levels [31].

Despite its advantages, the conventional Strong ARM comparator suffers from several limitations when applied to modern low-power SAR ADC architectures. One major drawback is that the Strong ARM structure employs a single-stage architecture, in which the input differential pair and the regenerative latch operate simultaneously without sufficient electrical isolation [48, 68-70]. As a result, the regenerative switching activity in the latch stage directly affects the input stage, leading to undesirable effects such as kickback noise, which can disturb the sampled input signal stored in the capacitive DAC. Additionally, the absence of isolation between stages increases switching losses and may result in higher dynamic power consumption, particularly under low-speed or low-voltage operating conditions [20, 24]. These limitations have motivated researchers to investigate alternative comparator architectures that offer improved energy efficiency and reduced noise coupling.

To overcome these challenges, the double-tail dynamic comparator architecture was proposed as an enhancement over the traditional Strong ARM latch [27, 28, 68, 77, 109, 113]. In this structure, the comparator is divided into two distinct stages: a preamplifier stage and a regenerative latch stage. The preamplifier stage amplifies the small differential input voltage while minimizing the effects of noise and kickback interference. The

amplified signal is then fed to the regenerative latch stage, which rapidly resolves the comparison decision through positive feedback regeneration [27, 28]. By separating the amplification and regeneration processes, the double-tail comparator improves input sensitivity and reduces the loading effect on the input signal source.

Although the double-tail architecture provides improved performance compared to single-stage designs, it still exhibits certain limitations. In many implementations, both the preamplifier and latch stages are activated simultaneously during the evaluation phase [48, 82, 84]. This simultaneous operation may result in suboptimal energy utilization, since the preamplifier may consume power even when the latch stage has already resolved the comparison decision. Furthermore, the performance of double-tail comparators can degrade under ultra-low supply voltage conditions, where reduced transistor overdrive limits the achievable gain and regeneration speed. These constraints become particularly significant in medium- to high-resolution SAR ADCs implemented in advanced technology nodes [31–33].

In response to these challenges, extensive research efforts have focused on developing improved comparator architectures that balance speed, power efficiency, and circuit complexity. Many modern designs employ two-stage comparator structures, where the preamplifier suppresses input-referred noise and reduces switching activity in the latch stage, while the regenerative latch ensures rapid decision-making [41, 87, 95]. Different circuit techniques have been studied to enhance the performance of the preamplifier stage. For instance, the use of cascode differential amplifier structures has been explored to increase the gain of the preamplifier by optimizing the overdrive voltage of the input transistors [43, 103, 108, 113, 129]. Higher gain allows the comparator to resolve smaller input voltage differences more quickly; however, this improvement typically results in higher static power consumption [41].

Similarly, several studies have proposed low-voltage double-tail comparator structures that incorporate additional transistors in the preamplifier stage to enhance gain and

improve speed performance [81, 88, 98, 115, 120, 126, 131, 135, 141]. While these designs can achieve reduced decision delay, they also increase circuit complexity, silicon area, and overall energy consumption [42, 44]. Other approaches have explored bulk-driven techniques to improve low-voltage operation by modifying the effective threshold voltage of input transistors [66, 67, 126]. For example, time-domain bulk-driven offset cancellation methods adjust the tail transistor parameters to improve comparator gain and speed characteristics. However, such methods typically require auxiliary circuits such as charge pumps and phase detectors, which increase design complexity and power overhead, limiting their suitability for high-frequency operation [42, 102, 123, 137].

Calibration-based techniques have also been investigated to mitigate comparator offset and improve accuracy. Methods such as weight-biasing calibration dynamically adjust the effective input threshold of the comparator to compensate for mismatch-induced offsets. While these techniques can significantly improve comparison accuracy, they often introduce additional digital control circuitry and calibration overhead, thereby increasing energy consumption and implementation complexity [29, 54–57, 109].

Beyond improvements in the preamplifier stage, several techniques focus on reducing power consumption within the regenerative latch stage. One approach involves the use of SR-latch-based regenerative comparators, where cross-coupled transistors provide strong positive feedback to accelerate the regeneration process while maintaining relatively low power consumption [43, 58, 144]. Another approach involves current-recycling techniques, in which bias currents are reused across multiple stages of the comparator to improve energy efficiency [33, 44, 153, 157]. Although these techniques can reduce average power consumption, the inclusion of additional latch stages may introduce extra delay and degrade the overall comparison speed [27,29].

Other design strategies combine the preamplifier and latch stages using multiplexing or hybrid structures, allowing certain circuit blocks to remain inactive during specific phases of operation in order to reduce average power consumption [45, 58, 64, 80, 90, 160, 164].

However, this integration may introduce additional delay in the signal path and adversely affect the overall comparison speed.

For applications requiring extremely low input-referred noise, some researchers have proposed multi-stage comparator architectures that employ two preamplifier stages followed by a regenerative latch [48, 73-76]. These designs provide improved sensitivity and faster decision speed but generally consume significantly higher power due to the increased number of active analog stages.

High-speed performance enhancement techniques have also been explored in the literature. For instance, peaking techniques using negative impedance converters can emulate negative capacitance in the preamplifier stage, effectively increasing bandwidth and accelerating the comparator decision process. While such approaches improve speed performance, they introduce additional circuitry that increases overall power consumption and design complexity [38–48].

More recently, advanced comparator designs have incorporated dynamic-time current-mode architectures that utilize switched-feedback inverters and clock-shaping circuits to dynamically regulate the power consumption during the comparison process [80, 82, 166, 170]. These designs aim to achieve the best compromise between speed and energy efficiency by controlling the timing of regenerative feedback. However, the additional circuit blocks required for clock shaping and feedback control increase implementation complexity and may present challenges in terms of scalability and layout optimization [68–69].

Overall, the existing literature demonstrates that comparator design inherently involves a trade-off among power consumption, speed, circuit complexity, and robustness under low-voltage operation. While numerous techniques have been proposed to improve specific performance metrics, achieving simultaneous optimization of all these parameters remains a challenging task. These limitations highlight the need for the development of novel

comparator architectures capable of providing high speed, low power consumption, reduced offset, and improved noise immunity, particularly for next-generation SAR ADCs designed for energy-constrained IoT and edge-sensing applications.

1.3.2 DAC Switching Algorithms and Capacitor Architectures

In a SAR ADC, CDAC plays a fundamental role in defining the energy efficiency, area consumption and linearity performance of the overall converter. The CDAC generates reference voltages during the successive approximation process by redistributing charge across a capacitor array. Because this charge redistribution occurs repeatedly for every bit decision in the conversion cycle, the DAC often becomes the dominant contributor to the total power dissipation and silicon area of the SAR ADC [6, 14]. Consequently, the design of efficient DAC architectures and switching algorithms has become one of the most active research areas in SAR ADC development.

Traditional SAR ADC implementations rely on binary-weighted capacitor arrays [16, 17], where the capacitor values follow a geometric progression proportional to powers of two. For an N-bit converter, the largest capacitor in the array typically has a value proportional to $2^N - 1$ times the unit capacitor. As the ADC resolution increases, the value of the largest capacitor rises exponentially. This exponential scaling leads to several practical challenges. First, the large capacitors occupy a substantial silicon area, increasing the overall chip size and fabrication cost. Second, large capacitive loads introduce significant parasitic capacitances and routing capacitance, which degrade the settling behavior of the DAC output. Third, the large capacitor array increases the impact of thermal noise, commonly represented by the kT/C noise limit, thereby constraining the minimum capacitor size that can be used in low-noise designs [1, 2].

Another important drawback of conventional binary-weighted DAC architectures is the high switching energy consumed during the charge redistribution process. In each conversion cycle, multiple capacitors are switched between reference voltage nodes and ground, resulting in substantial charge transfer. This repeated charging and discharging

process consumes significant dynamic power. Furthermore, switching large capacitors generates reference-dependent voltage glitches and transient disturbances, which require additional settling time before accurate comparator decisions can be made. Consequently, the DAC switching operation can restrict the highest attainable sampling rate of the SAR ADC.

Capacitor mismatch also represents a major challenge in binary-weighted DAC arrays. Manufacturing variations in capacitor dimensions and dielectric properties introduce mismatch between capacitors that ideally should have precise binary ratios. Such mismatches cause deviations in the DAC output voltage, which in turn introduce nonlinear errors such as DNL and INL [19]. These nonlinearities degrade the accuracy of the converter and may lead to missing codes in severe cases. To mitigate these effects, designers often rely on careful layout methods such as common-centroid configuration, capacitor trimming, or digital calibration methods. Nevertheless, the presence of large capacitors and parasitic elements continues to impose limitations on DAC performance.

To address these limitations, numerous energy-efficient DAC switching algorithms have been introduced over the past decade. These algorithms aim to minimize the total charge transfer during the conversion process while maintaining accurate digital approximation. One of the earliest improvements over the conventional switching scheme is the monotonic switching algorithm [21, 65, 92], which significantly reduces switching energy by ensuring that capacitors switch in only one direction during the conversion process. In this approach, large capacitors are not toggled between opposite reference voltages, thereby avoiding unnecessary charge redistribution and reducing energy consumption. Monotonic switching has become widely adopted in practical SAR ADC designs due to its simplicity and moderate energy savings.

Further improvements have been achieved through the introduction of non-binary and redundant switching techniques [25, 39, 59, 61-63]. In non-binary architectures, the capacitor array does not strictly follow binary weighting; instead, redundancy is

introduced in the DAC structure to relax matching requirements and tolerate comparator errors. By allowing slight inaccuracies during intermediate comparison steps, non-binary DAC structures reduce the need for precise capacitor ratios and enable faster convergence of the successive approximation process. Redundant switching schemes extend this concept by incorporating additional capacitors or redundant bits that provide flexibility in the approximation sequence, thereby improving tolerance to noise and mismatch effects [78, 79].

More aggressive switching schemes have also been proposed to achieve near-complete switching energy reduction. These approaches carefully reuse stored charge and avoid resetting capacitors to ground between successive conversion cycles. Techniques such as charge-reuse switching [24, 52, 132, 161], reference recycling [81] and reset-energy elimination [103, 149] can reduce the total switching energy by a large percentage compared to conventional charge redistribution methods. In some advanced implementations, these techniques have enabled SAR ADCs to achieve extremely low energy per conversion step, making them highly suitable for energy-constrained applications.

In addition to switching algorithm optimization, significant research efforts have been directed in improving the capacitor topology of the DAC array. One common approach involves the use of split-capacitor DAC structures [25, 38, 40, 83, 85, 91, 94, 105], in which the large capacitor array is divided into multiple smaller sub-arrays connected through attenuation capacitors. This technique reduces the size of the largest capacitor while maintaining the overall resolution of the converter. By reducing the physical size of the capacitor array, split-capacitor DACs significantly decrease silicon area and parasitic capacitance, thereby improving both energy efficiency and conversion speed.

Another widely adopted architecture is the split-array DAC [116, 122, 130, 143, 152, 162, 169], where the MSB capacitors and LSB capacitors are implemented in separate sub-arrays. These sub-arrays may be connected through bridging capacitors or scaling

capacitors to achieve the desired binary weighting. Split-array architectures scale well with increasing resolution because they prevent the largest capacitor from becoming excessively large. Additionally, these structures facilitate improved matching through optimized layout techniques and calibration methods [18,47].

More advanced capacitor structures have also been introduced to further reduce switching energy. For example, semi-resting DAC architectures maintain the charge stored in large capacitors during intermediate conversion steps, thereby avoiding unnecessary switching activity [59]. Similarly, semi-recovery DAC structures reuse charge from previous conversions to reduce the total energy required for subsequent operations. These techniques have demonstrated extremely low energy consumption, achieving femto-Joule energy per conversion step in specialized low-power implementations [48].

Additional energy savings can be achieved through charge-sharing reset techniques, where charge that would normally be dissipated to ground during reset operations is partially recovered and reused in subsequent cycles. These charge-recovery approaches further improve energy efficiency by minimizing the net charge transfer in the DAC network [71, 72].

Despite these advancements, the design of DAC switching schemes and capacitor architectures involves several important trade-offs. Algorithms that achieve significant switching-energy reduction often require more complex control logic and precise timing coordination, which can increase digital power consumption and design complexity. Similarly, split or redundant capacitor arrays may introduce additional calibration requirements to maintain acceptable DNL and INL performance. Therefore, the overall effectiveness of a DAC architecture depends on careful co-optimization of switching algorithms, capacitor layout, comparator design, and SAR logic.

Application requirements also influence DAC design choices. For example, ultra-low-power wearable biosensor systems typically prioritize minimal energy per conversion step

and low supply voltage operation rather than extremely high sampling rates [50]. In such applications, designers often employ small-capacitance DAC arrays combined with simplified switching algorithms that minimize dynamic energy consumption.

Overall, the most energy-efficient SAR DAC implementations integrate several complementary techniques, including optimized switching algorithms, capacitor splitting strategies, charge reuse mechanisms and careful layout design to manage mismatch and parasitic effects. By combining algorithmic innovations with improved capacitor architectures, modern SAR ADCs can achieve significant reductions in power consumption while maintaining high accuracy and scalability for next-generation mixed-signal systems.

1.3.3 SAR Logic and System-Level Considerations

While the analog building blocks such as the comparator and CDAC form the core of the conversion process in a SAR ADC, the SAR logic plays an equally important role in determining the overall efficiency, speed and reliability of the converter. The SAR logic orchestrates the entire conversion process by controlling the switching sequence of the DAC, managing comparator evaluation cycles and storing intermediate decision results. Although SAR logic is implemented using digital circuitry, its performance has a major impact on the dynamic power consumption, timing accuracy, and throughput of the ADC [20, 23, 58]. As the resolution and operating speed of SAR ADCs increase, the impact of SAR logic on overall system performance becomes increasingly pronounced.

In a conventional SAR ADC, the conversion process follows a binary search algorithm in which each bit of the digital output is determined sequentially [60, 86, 93]. The SAR logic first assigns a trial value to the MSB and instructs the DAC to produce the corresponding reference voltage. The comparator then evaluates whether the sampled input voltage is greater or smaller than the DAC output, after which the SAR logic updates the digital code accordingly. This iterative procedure continues from the MSB down to the LSB, requiring N comparison steps for an N -bit ADC. Although this approach is conceptually simple and

highly efficient for moderate sampling rates, it introduces certain limitations as converter resolution and speed increase.

One of the primary challenges associated with SAR logic is the dynamic power consumption caused by switching activity within the digital control circuitry [96, 99, 100]. During each conversion cycle, multiple digital signals toggle as the SAR logic updates the register contents and controls DAC switching operations. As the sampling frequency increases, the switching activity within the SAR logic also increases, leading to higher dynamic power dissipation. Furthermore, inefficiencies in the design of the state machine controlling the SAR logic can result in unnecessary transitions or redundant clock cycles, which further increase energy consumption per conversion.

Another important consideration is the precise timing coordination required between the comparator, DAC and SAR logic [48]. After each bit decision, the DAC output must settle to a stable voltage level before the comparator performs the next comparison. If the SAR logic advances to the next decision step before the DAC has fully settled, incorrect comparator decisions may occur, leading to conversion errors. Conversely, if excessive settling time is allocated, the overall conversion speed is unnecessarily reduced. Therefore, the SAR logic must carefully synchronize comparator evaluation, DAC settling and register updating operations to ensure both accuracy and efficiency.

As the resolution of the SAR ADC increases, the complexity of the SAR logic also increases. Higher resolution converters require a larger number of decision cycles, which places more stringent requirements on clock generation, signal synchronization and timing margins. Moreover, the logic circuitry must be robust enough to handle metastability conditions that may arise when the comparator decision occurs near the switching threshold [115]. If metastability is not properly handled, the SAR logic may incorrectly interpret comparator outputs, resulting in erroneous digital codes. Consequently, robust SAR logic design is essential to ensure reliable operation across different PVT conditions.

At the architectural level, the design of SAR logic directly influences how efficiently improvements in comparator and DAC design translate into overall ADC performance. Traditional SAR controllers rely on single-bit-per-cycle conversion, where each bit decision requires one complete comparator evaluation [107]. While this approach minimizes hardware complexity, it limits the maximum achievable sampling rate because the total conversion time is proportional to the ADC resolution. To address this limitation, several advanced SAR logic techniques have been proposed.

One such technique is the multi-bit-per-cycle SAR architecture, where multiple bits are resolved during a single comparison cycle [97, 101, 111, 127]. For example, 2-bit-per-cycle SAR ADCs determine two bits simultaneously by using multiple comparators or more complex decision logic. This approach significantly decreases the number of necessary comparison cycles, thereby improving conversion speed and increasing the effective conversion speed of the converter [51]. However, the implementation of multi-bit-per-cycle architectures requires more sophisticated comparator arrangements and additional digital control circuitry, which may increase design complexity and power consumption.

Another important architectural enhancement involves the use of hybrid ADC architectures, where SAR conversion is combined with other conversion techniques to improve performance [35, 89, 97, 119, 133, 138, 150, 163]. For example, Flash–SAR hybrid architectures employ a small flash ADC stage to determine the most significant bits of the input signal, followed by SAR logic that resolves the remaining lower bits. By performing coarse quantization using a flash stage, the number of SAR comparison cycles can be reduced, thereby improving conversion speed. However, the integration of flash and SAR architectures introduces additional design challenges, including comparator matching, thermometer-to-binary decoding, and synchronization between parallel and sequential conversion stages.

In addition to speed improvement techniques, modern SAR ADCs also incorporate redundancy and calibration mechanisms to enhance accuracy and robustness. Redundant DAC encodings allow the SAR logic to tolerate certain comparator decision errors without affecting the final conversion result [40, 78, 86]. Such redundancy relaxes capacitor matching requirements and improves linearity performance, although it increases the complexity of the control logic and requires additional digital processing.

Another important concept is comparator-aware SAR control [101, 112, 118], where the SAR logic dynamically adapts the timing of comparison operations based on the behavior of the comparator. For example, when the comparator input difference is small, the regeneration process may take more time to resolve the decision. In such cases, the SAR logic can extend the evaluation time to avoid metastability errors. Conversely, when the input difference is large, the decision can be completed more quickly, allowing the SAR logic to proceed to the next step sooner. This adaptive timing strategy helps optimize the trade-off between speed and reliability while reducing unnecessary power consumption [60, 61].

At extremely high sampling rates, particularly in gigahertz-range SAR ADCs, system-level considerations become even more critical. In such designs, the comparator, sampling network, DAC switching circuitry, and SAR logic must be co-designed to ensure precise timing alignment. Issues such as clock distribution delay, comparator regeneration timing, and input sampling accuracy become dominant design constraints. Advanced clocking strategies [104], pipeline-assisted SAR structures [73, 75, 170] and asynchronous SAR logic [64, 65] have been explored to address these challenges.

On the opposite end of the design spectrum, SAR ADCs intended for low power applications such as IoT sensor nodes, wearable biomedical devices and energy-harvesting systems, prioritizing minimal energy consumption per conversion rather than maximum speed [37, 39, 88, 93, 117, 121, 125, 134, 136, 140]. In these systems, the SAR logic is often optimized for energy efficiency through techniques such as asynchronous control

logic, reduced switching activity, simplified state machines, and voltage-scaled digital circuits. Additionally, small-capacitor DAC arrays and low-power comparators are employed to further reduce energy consumption per sample [66, 67, 72–76].

Despite the numerous advancements in comparator design, DAC switching algorithms, and SAR logic, several challenges remain in achieving the simultaneous optimization of speed, power efficiency, area, and accuracy. The interaction among these building blocks creates fundamental performance bottlenecks that limit the scalability of SAR ADC architectures in advanced CMOS technologies. In particular, achieving high conversion speed without significantly increasing power consumption remains a major challenge in the design of next-generation SAR ADCs.

These limitations highlight the need for new circuit-level and architectural innovations that can improve the performance of SAR ADCs while maintaining energy efficiency. Specifically, there is a strong motivation to develop improved comparator architectures with enhanced sensitivity and reduced power consumption, more efficient DAC structures that reduce capacitor count and switching energy, and optimized SAR logic capable of supporting high-speed operation with minimal power overhead.

1.3.4 Hybrid ADC Architectures: Bridging Speed and Power Efficiency

As the demand for high-performance data conversion continues to grow in modern electronic systems, the limitations of conventional ADC architectures have driven the development of hybrid data converter architectures that combine the advantages of multiple conversion techniques [48]. While SAR ADCs are widely recognized for their excellent energy efficiency and moderate speed, their sequential bit-cycling operation inherently limits the achievable sampling rate in very high-speed applications [20]. Conversely, architectures such as Flash ADCs offer extremely high conversion speed but suffer from exponential growth in comparator count, large silicon area, and high power consumption [9]. Hybrid ADC architectures have therefore emerged as an attractive

solution to bridge the performance gap between high-speed conversion and energy efficiency.

Hybrid ADCs integrate two or more conversion techniques within a single architecture in order to exploit their complementary advantages. Among the various hybrid approaches proposed in the literature, Flash–SAR ADCs, Pipeline–SAR ADCs, and multi-step SAR architectures are the most widely studied. These architectures aim to increase conversion speed while maintaining the low power characteristics that make SAR ADCs attractive for modern mixed-signal systems.

One of the most widely adopted hybrid architectures is the Flash–SAR ADC, which combines a coarse flash conversion stage with a fine SAR conversion stage [89, 97, 107, 112, 119]. In this architecture, a low-resolution flash ADC is used to find the MSBs of the input signal. Since flash converters perform comparisons simultaneously using parallel comparators, the MSB determination occurs very rapidly. Once the coarse conversion is completed, the remaining LSBs are resolved using a SAR conversion process. This hybrid strategy significantly reduces the number of SAR comparison cycles required to finish the conversion, thereby increasing the overall sampling rate of the converter.

The Flash–SAR approach provides several advantages. First, the flash front-end reduces the number of sequential SAR cycles, which directly improves conversion speed. Second, since the flash stage typically resolves only a few MSBs, the number of required comparators remains relatively small compared to a full flash ADC implementation. Third, the SAR stage continues to benefit from the energy efficiency of CDAC switching, preserving the low-power features of SAR ADC architectures. However, the integration of a flash front-end also introduces new design challenges, including comparator offset matching, thermometer-to-binary encoding, and synchronization between parallel flash decisions and sequential SAR logic [127, 133, 142, 150, 159, 167].

Another important hybrid architecture is the Pipeline–SAR ADC, which combines the pipeline conversion principle with SAR sub-converters. In traditional pipeline ADCs, each stage resolves a small number of input bits and forwards the residue signal to the next stage for further refinement. However, conventional pipeline stages rely heavily on operational amplifiers to perform residue amplification, which significantly increases power consumption and limits scalability in low-voltage CMOS technologies. To overcome these limitations, modern designs replace traditional pipeline stages with SAR-based residue converters. In a Pipeline–SAR ADC, each stage carries out a partial SAR conversion and produces a residue voltage that is transferred to the following stage. This approach significantly reduces the need for high-power operational amplifiers while maintaining high throughput [73, 75].

Pipeline–SAR architectures provide a favorable balance between speed and power efficiency. Since different pipeline stages operate concurrently, the overall throughput can be significantly higher than that of a traditional SAR ADC [170]. At the same time, use of SAR-based stages allows designers to leverage capacitive DAC structures and dynamic comparators, which are inherently energy efficient. Nevertheless, pipeline-based architectures require careful management of inter-stage residue amplification, calibration, and digital correction techniques to maintain high linearity performance.

In addition to Flash–SAR and Pipeline–SAR architectures, several multi-step and multi-bit-per-cycle SAR ADC architectures have been proposed to enhance conversion speed [106, 114]. In these architectures, multiple bits are resolved during each comparison cycle rather than determining one bit at a time. For example, a 2-bit-per-cycle SAR ADC determines two bits simultaneously by comparing the input signal against multiple reference levels. By resolving multiple bits per cycle, the overall number of comparison cycles needed for conversion is reduced, leading to faster operation. However, this improvement often requires additional comparators or more complex reference generation schemes, which may increase circuit complexity and power consumption.

Another promising direction involves time-interleaved SAR ADC architectures, where multiple SAR ADC cores operate in parallel to increase the effective sampling rate. In this technique, each ADC core samples the input signal at a fraction of the overall sampling rate, and their outputs are interleaved to produce a high-speed digital data stream. Time-interleaving enables very high sampling rates without requiring extremely fast individual converters [35, 54-57, 72, 76]. However, this approach introduces challenges related to channel mismatch, timing skew, offset mismatch and gain mismatch, which must be carefully corrected using calibration techniques.

Hybrid architectures have also been explored to support adaptive and reconfigurable ADC systems. In such designs, the converter dynamically adjusts its resolution or operating mode depending on the application requirements [77, 80, 112]. For example, in wireless communication systems, the ADC may operate at high speed with moderate resolution during data reception, while switching to a lower sampling rate and higher resolution during signal monitoring. Reconfigurable hybrid architectures allow a single converter to support multiple operating modes, improving system flexibility and energy efficiency.

Despite the numerous advantages offered by hybrid ADC architectures, their design also involves several trade-offs. The integration of multiple conversion techniques increases architectural complexity and often requires sophisticated digital calibration and control logic. Additional comparator circuits and reference generation networks may increase power consumption if not carefully optimized. Furthermore, maintaining synchronization between different conversion stages is critical to ensure accurate and reliable operation.

Nevertheless, hybrid architectures represent an important direction in modern ADC research, particularly for applications that require both high sampling speed and energy efficiency. By intelligently combining the strengths of multiple conversion techniques, hybrid ADCs can achieve performance levels that are difficult to realize using a single architecture alone.

In the context of low-power sensing systems and Internet-of-Things applications, the challenge is to develop hybrid architectures that maintain the energy efficiency of SAR ADCs while extending their speed capabilities. Recent research trends therefore focus on hybrid designs that minimize additional circuitry, reduce comparator count, and maintain compact capacitor arrays. These efforts aim to achieve high-performance ADC solutions capable of supporting the increasing data-rate demands of modern mixed-signal systems.

Consequently, the exploration of hybrid ADC architectures offers valuable understanding into overcoming the inherent speed limitations of conventional SAR ADCs. By integrating architectural innovations with improved circuit techniques, hybrid converters play a crucial role in advancing the performance of next-generation data conversion systems.

1.4 Research Gaps

The rapid expansion of IoT platforms, wearable biomedical devices, portable sensing nodes, wireless sensor networks, and edge-computing systems has significantly increased the demand for compact and energy-efficient data acquisition circuits. In such systems, the ADC serves as a critical interface between real-world analog signals and digital processing systems. The performance of the ADC directly determines the overall accuracy, power consumption, latency, and signal integrity of the system. Consequently, the development of high-performance and low-power ADC architectures has become an important research focus in modern mixed-signal integrated circuit design.

Among the various ADC architectures, SAR ADC has emerged as one of the most attractive solutions for medium-resolution and moderate-speed applications. SAR ADCs provide an excellent balance between resolution, conversion speed, circuit complexity, and energy efficiency. Their architecture primarily relies on capacitive charge redistribution, dynamic comparators, and digital control logic, making them highly compatible with modern CMOS technology scaling. As a result, SAR ADCs are widely used in low-power sensing systems, biomedical instrumentation, wireless communication devices, and embedded signal processing platforms.

Despite their advantages, achieving simultaneous improvements in speed, resolution, and power efficiency remains a challenging task in SAR ADC design. The overall performance of a SAR ADC is heavily dependent on the efficiency of its main building blocks, including the comparator, CDAC and SAR logic. Each of these components imposes particular design limitations that affect the scalability and performance of the converter. Consequently, several research gaps still exist in the optimization of these fundamental blocks, particularly for operation in modern low-voltage CMOS technologies.

1.4.1 Research Gap in Comparator Design

One of the most critical components in a SAR ADC is the comparator, which executes the decision-making operation during each bit comparison cycle. In a typical N-bit SAR ADC, the comparator is activated N times during each conversion process. Therefore, its delay, input-referred noise, offset voltage, and metastability characteristics directly influence the achievable resolution, SNR and maximum sampling rate of the converter.

Dynamic comparators are widely used in SAR ADC architectures because they consume negligible static power and can achieve high operating speeds. Several comparator topologies have been proposed in the literature, including StrongARM latch comparators [31], double-tail dynamic comparators [27, 30], auxiliary-inverter comparators [42, 108, 129], and body-biased comparator structures [67, 95, 154]. These designs attempt to improve speed, reduce noise, or minimize offset voltage through various circuit techniques such as regenerative latching, adaptive biasing, and offset calibration.

However, many of these techniques introduce additional transistors, intermediate nodes, or auxiliary circuits, which increase parasitic capacitance and layout complexity. These additional parasitic effects can degrade the regeneration speed of the latch and increase dynamic power consumption. Furthermore, offset reduction techniques often require

calibration loops or digital correction circuitry, which increases area overhead and system complexity [66, 98, 109].

Another significant challenge arises when comparators operate under low supply voltage conditions, which are common in modern deep-submicron CMOS technologies [110, 124]. Reduced supply voltage limits the available voltage headroom for transistor operation, weakening the regenerative gain of the latch stage. This leads to longer decision times and increases susceptibility to metastability, particularly when the input differential voltage is small. Additionally, thermal noise and device mismatch become more dominant at low supply voltages, further degrading comparator accuracy.

The regeneration process in dynamic comparators also introduces kickback noise, which propagates back to the DAC output and disturbs the sampled input signal. This phenomenon can significantly degrade conversion accuracy, especially in high-resolution SAR ADCs where the voltage difference between adjacent codes is extremely small.

Therefore, there exists a clear need for novel comparator architectures that simultaneously achieve:

- i. High decision speed
- ii. Robust operation under low supply voltages
- iii. Low power consumption

Developing such comparators without relying on extensive calibration circuitry remains an important research challenge in modern SAR ADC design.

1.4.2 Research Gap in DAC Switching Techniques

Another important component in SAR ADC architectures is the CDAC, which generates reference voltages during the successive approximation process. The DAC typically

occupies the largest silicon area in the converter and contributes significantly to the overall power dissipation.

In conventional SAR ADC designs, the DAC is implemented using a binary-weighted capacitor array [21, 52, 105, 148, 165]. While this approach provides a straightforward implementation of the charge-redistribution algorithm, it introduces several limitations. As ADC resolution increases, the capacitor sizes grow exponentially, resulting in large silicon area and increased parasitic capacitances. For example, a 10-bit binary-weighted DAC requires a capacitor ratio of 512:1 between the largest and smallest capacitors.

The high total capacitance of the DAC array increases switching energy consumption during each conversion cycle. Every time the capacitor array is reconfigured during the successive approximation process, charge is redistributed between capacitors and reference voltage nodes. This repeated switching process results in significant dynamic power dissipation.

In addition to increased power consumption, large capacitor arrays also introduce settling time limitations. The DAC output voltage must settle to a stable value before the comparator performs the next comparison. Large capacitances slow down this settling process, thereby limiting the maximum achievable sampling rate.

To address these challenges, several energy-efficient switching schemes have been studied in the literature, including:

- i. Monotonic switching techniques
- ii. Vcm-based switching algorithms
- iii. Split capacitor arrays

Although these approaches significantly reduce switching energy, they often introduce additional circuit complexity. Some techniques require multiple reference voltages, while others rely on redundant capacitor arrays that increase layout complexity and calibration

requirements. Furthermore, many reported DAC switching schemes are evaluated under nominal operating conditions, with limited analysis of reliable performance under PVT variations.

Therefore, an important research gap exists in the development of simple, scalable DAC architectures that can simultaneously achieve:

- i. Reduced switching energy
- ii. Smaller capacitor arrays
- iii. Improved linearity performance
- iv. Robust operation under PVT variations
- v. Minimal circuit complexity

1.4.3 Research Gap in SAR Logic

While significant research attention has been devoted to comparator and DAC design, the SAR logic has received comparatively less focus. The SAR logic governs the timing and sequencing of the conversion process, coordinating the operation of the DAC switching network and comparator decisions.

Conventional SAR ADCs employ synchronous control logic, where each comparison cycle is triggered by a global clock signal. Although this approach simplifies timing control, it introduces several limitations. High-frequency clock distribution networks consume significant dynamic power, especially in high-speed SAR ADCs [29, 98, 130]. Additionally, synchronous operation requires conservative timing margins to ensure correct operation across PVT variations, which may reduce conversion speed and energy efficiency.

Recent research has explored asynchronous SAR logic architectures, where the next comparison cycle is triggered immediately after the comparator decision becomes available [96, 106, 118, 124]. This approach eliminates unnecessary clock cycles and can

significantly reduce conversion time. However, asynchronous designs often require more complex control circuits and are sensitive to variations in comparator delay.

Another important limitation of conventional SAR logic is the lack of adaptive behavior. Most existing SAR controllers operate with fixed timing schedules regardless of input signal conditions [55, 89, 151]. In practice, the comparator may resolve some decisions much faster than others, depending on the input voltage difference. Fixed-timing control therefore results in wasted idle time and unnecessary energy consumption.

Furthermore, the interaction between SAR logic and comparator metastability is not fully addressed in many existing designs [48]. If the comparator requires additional regeneration time for small input differences, the SAR logic may incorrectly interpret the output if sufficient timing margin is not provided. Current solutions often rely on conservative timing design or additional calibration circuits, which increase power consumption and circuit complexity.

Thus, there remains significant scope for developing energy-aware and adaptive SAR logic architectures that can dynamically adjust their operation based on comparator behavior and input signal conditions.

1.4.4 Research Gap in Hybrid SAR ADC Architectures

Hybrid ADC architectures, particularly Flash–SAR converters, have been studied to overcome the speed limitations of conventional SAR ADCs [107, 127, 138]. In these architectures, a flash converter carries out a coarse quantization of the input signal, while a SAR converter resolves the remaining lower bits. This technique reduces the number of SAR comparison cycles and improves conversion speed.

However, hybrid architectures introduce additional design challenges. The flash front-end requires multiple comparators and reference ladders, which increase static and dynamic

power consumption. Comparator offset mismatch and reference ladder inaccuracies may also degrade conversion accuracy.

Moreover, many existing hybrid architectures focus primarily on improving speed, with less emphasis on overall energy efficiency. As a result, hybrid ADCs often consume significantly more power than pure SAR ADCs at moderate sampling rates.

Therefore, there is a need for energy-efficient hybrid architectures that maintain the low-power characteristics of SAR ADCs while improving conversion speed.

1.5 Problem Statement

The continuous development of modern electronic techniques has significantly enhanced the adoption of intelligent and interconnected systems such as IoT devices, wearable healthcare monitors, wireless sensor networks and portable embedded platforms. These applications rely on compact and energy-efficient data acquisition circuits capable of accurately capturing physical signals from the surrounding environment. In such systems, ADCs serve as a critical bridge between the analog sensing domain and digital processing units. By converting continuous-time analog signals generated by sensors into discrete digital representations, ADCs enable further processing, storage and communication of data. Consequently, the overall performance of the ADC—including its resolution, conversion speed and power consumption—influences on the efficiency, reliability and operational lifetime of the entire electronic system.

Among the various ADC architectures, SAR ADC has emerged as suitable solutions for low-power and moderate-resolution applications. SAR ADCs offer several advantages including simple architecture, excellent energy efficiency, scalability with CMOS technology, and compatibility with low supply voltages. These characteristics make SAR ADCs particularly attractive for battery-operated and energy-constrained applications where minimizing power consumption is critical. However, despite these advantages,

achieving simultaneously high speed, high resolution, and low power dissipation remains a significant challenge in SAR ADC design.

The overall performance of a SAR ADC is greatly influenced by the efficiency and coordination of its primary building blocks, including the comparator, CDAC and SAR logic. Each of these components introduces specific limitations that restrict the achievable performance of the converter. Consequently, improving SAR ADC performance requires a comprehensive design approach that addresses the limitations of these blocks simultaneously.

One of the most critical challenges arises from the comparator circuit, which performs the decision-making operation during each bit comparison cycle of the SAR algorithm. The comparator must detect extremely small voltage differences between the sampled input signal and the DAC output voltage. Therefore, its performance parameters—such as delay, input-referred noise, offset voltage, metastability behavior and power consumption—directly affect the achievable resolution, SNR and maximum sampling rate of the ADC. Conventional dynamic comparator architectures, including StrongARM and double-tail comparators, have been widely used due to their high speed and low static power consumption. However, these designs suffer from several drawbacks when implemented in modern low-voltage CMOS technologies. Reduced supply voltage limits the available voltage headroom for transistor operation, weakening the regenerative gain of the latch and increasing susceptibility to noise and offset. Additionally, many advanced comparator techniques require additional circuitry for offset calibration, auxiliary amplification, or bias control, which increases power consumption, circuit complexity, and silicon area. These limitations highlight the need for novel comparator architectures capable of providing high-speed operation, reduced noise, and low power consumption while maintaining reliable performance at low supply voltages.

Another important challenge in SAR ADC design arises from the CDAC switching network, which is responsible for generating reference voltages during the successive

approximation process. In conventional SAR ADCs, the DAC is implemented using binary-weighted capacitor arrays. While this approach simplifies the implementation of the charge redistribution algorithm, it leads to exponential growth in capacitor size as the resolution increases. For example, in a 10-bit SAR ADC, the largest capacitor must be 512 times larger than the smallest unit capacitor. Such large capacitor arrays occupy significant silicon area and introduce large parasitic capacitances that degrade settling speed. Furthermore, frequent switching of these capacitors during each conversion cycle leads to considerable dynamic power consumption. Although various energy-efficient switching algorithms have been proposed to reduce DAC switching energy, many of these techniques introduce additional reference voltages, redundant capacitor structures, or complex switching control schemes. These solutions increase design complexity and may negatively affect linearity performance, particularly in the presence of capacitor mismatch. Therefore, there is a strong need to develop DAC architectures and switching techniques that reduce switching energy, minimize capacitor count, and maintain high linearity while remaining simple and robust for practical implementation.

Besides the comparator and DAC, the SAR logic has a significant role in defining the conversion speed and energy efficiency of the ADC. The SAR logic manages the sequence of DAC switching actions and comparator decisions necessary for implementing the binary search algorithm. Conventional SAR ADC typically employ synchronous control logic driven by a global clock. However, high-frequency clock distribution introduces significant dynamic power consumption and limits scalability for high-speed operation. Furthermore, the fixed timing of synchronous SAR logic often results in inefficient use of comparator decision time, since the logic must assume worst-case delays to guarantee correct operation. As a result, unnecessary idle periods may occur between comparison cycles, increasing overall conversion time and energy consumption. While asynchronous and multi-bit-per-cycle SAR logic architectures have been proposed to improve speed and efficiency, these approaches often introduce complex control circuits and increased sensitivity to process, voltage, and temperature variations. Consequently, there remains a need for energy-efficient SAR logic architectures that reduce digital switching activity,

support high-speed operation, and maintain robust timing coordination with the comparator and DAC circuits.

Another limitation in conventional SAR ADC architectures is the inherent trade-off between conversion speed and power efficiency. The sequential nature of the SAR algorithm requires one comparison per bit, which limits the maximum achievable sampling rate for high-resolution converters. Hybrid architectures such as Flash–SAR ADCs have been introduced to improve speed by combining coarse flash conversion with fine SAR quantization. However, these architectures typically introduce additional comparators and reference networks, which increase static and dynamic power consumption. Moreover, many existing hybrid designs prioritize speed improvements without adequately addressing overall energy efficiency. Therefore, there is a need for hybrid SAR ADC architectures that enhance conversion speed while preserving the low-power advantages of conventional SAR designs.

Based on the above challenges, it becomes evident that achieving a high-performance SAR ADC requires a holistic design approach that simultaneously addresses the limitations of the comparator, DAC and SAR logic blocks. Improvements in one component alone are often insufficient to achieve significant system-level performance enhancement. Instead, coordinated optimization of these building blocks is necessary to achieve improvements in speed, resolution, power efficiency, and silicon area.

1.6 Research Objectives

The primary objective of this research is to develop a novel high-performance SAR ADC architecture by addressing the key design limitations associated with its core building blocks. The specific objectives of the work are as follows:

1. **To design an enhanced performance comparator for application in Analog to Digital Converters (ADC)** with improved speed, reduced input-referred noise,

and robust metastability characteristics suitable for low-voltage, high-resolution ADC applications.

2. **To design a Digital to Analog Converter (DAC) circuit with reduced number of capacitors for improving delays and overall ADC footprint** in order to minimize switching energy, improve settling behavior, reduce conversion delay and decrease the overall silicon area of the ADC.
3. **To design a power efficient Successive Approximation Register (SAR) logic for application in ADC** that minimizes switching activity and dynamic power consumption while ensuring fast and reliable bit-by-bit decision sequencing.
4. **To design a novel high performance SAR ADC**, and to demonstrate improvements in speed, resolution, power efficiency and footprint through detailed simulation, analysis, and performance benchmarking against state-of-the-art designs.

1.7 Thesis Organization

This thesis is organized into six chapters, each focusing on different aspects of low-power and high-performance SAR ADC design techniques and hybrid ADC architectures.

Chapter 1 presents the introduction and background of Analog-to-Digital Converters (ADCs), with particular emphasis on Successive Approximation Register (SAR) ADCs. The chapter discusses the motivation behind the research, important SAR ADC performance parameters, literature survey, identified research gaps, problem statement, research objectives and overall thesis organization.

Chapter 2 provides a comprehensive review of prior work on advanced mixed-signal circuit techniques used in SAR ADC design. The chapter discusses self-cascode structures, DTMOS-based techniques, cross-coupled regenerative latch architectures, shared-charge reset techniques, auxiliary inverter methods, capacitive DAC switching

schemes and SAR control strategies. Different design trade-offs related to power consumption, speed, silicon area and circuit complexity are also analyzed.

Chapter 3 focuses on the proposed comparator architectures developed in this research work. Multiple comparator topologies based on self-cascode structures, shared-charge logic, auxiliary inverter techniques and DTMOS operation are presented and analyzed. Their operating principles, circuit implementation and performance improvements are discussed in detail along with comparative evaluation results.

Chapter 4 presents the design and implementation of a low-power SAR ADC architecture. The chapter introduces the proposed methodology, including split-capacitor DAC architecture, bootstrap sampling switch, V_{cm} -based switching technique and energy-optimized switching strategy. Simulation results related to switching energy, static linearity, dynamic performance, and power consumption are also discussed.

Chapter 5 presents the proposed Hybrid Flash-SAR ADC architecture developed to achieve improved conversion speed and energy efficiency. The chapter explains the integration of flash ADC and SAR ADC blocks, asynchronous SAR logic, segmented DAC structure and hybrid conversion methodology. Detailed simulation results including FFT analysis, linearity analysis, switching energy comparison and overall performance evaluation are presented and discussed.

Chapter 6 presents the conclusions, future research directions, and social impact of the proposed work. The chapter summarizes the major contributions and performance improvements achieved through the proposed comparator architectures and SAR ADC techniques. In addition, possible future enhancements such as AI-assisted calibration, advanced CMOS technology scaling, ultra-low-voltage operation and high-speed time-interleaved architectures are discussed. The chapter also highlights the potential social impact of energy-efficient ADC systems in applications such as IoT devices, wearable

healthcare systems, biomedical instrumentation, wireless communication, environmental monitoring and sustainable low-power electronic systems.

Chapter 2

Prior Work on Advanced Mixed-Signal Circuit Techniques

2.1 Scope of the Chapter

This chapter presents a comprehensive review of prior work on advanced mixed-signal circuit techniques that are widely employed in the design of energy-efficient and high-performance data converters, particularly SAR ADCs. The primary objective of this chapter is to establish a strong theoretical and practical foundation by critically examining various circuit-level and architectural innovations reported in the literature, without focusing on specific implementations from this thesis.

The chapter begins by discussing device and circuit level enhancement techniques such as the self-cascode structure and DTMOS-based configurations, which are primarily aimed at improving intrinsic gain, reducing leakage and enabling reliable operation at ultra-low supply voltages. These techniques are particularly relevant in modern CMOS technologies where reduced voltage headroom poses significant design challenges.

Subsequently, the chapter explores comparator design methodologies, including the cross-coupled regenerative latch structure, shared-charge reset technique, auxiliary inverter-based enhancements, and the conventional dynamic comparator. These approaches are examined in terms of their influence on key performance metrics such as offset voltage, decision speed, power consumption, and noise immunity, which are critical in finding overall efficiency of SAR ADCs.

The discussion then transitions to CDAC architectures, covering a range of switching schemes such as binary-weighted structures, monotonic switching, V_{cm} -based techniques and split-capacitor configurations. Emphasis is placed on understanding how these

techniques influence switching energy, linearity, capacitor area, and settling behavior, thereby affecting the overall ADC performance.

Further, the chapter reviews SAR logic and control strategies, including conventional sequential logic, binary search algorithms, and asynchronous control techniques. These methods are evaluated based on their ability to optimize conversion speed, reduce digital power consumption, and simplify timing requirements.

Additionally, the chapter includes a review of conventional comparator architecture, highlighting their operating principles, regenerative behavior and inherent limitations regarding delay, energy and power. This discussion provides a baseline for understanding the performance improvements achieved by advanced comparator techniques presented in later sections.

Finally, the chapter consolidates the insights gained from the reviewed techniques by presenting a detailed analysis of design trade-offs, focusing on power, speed, area and circuit complexity. Key observations are drawn to highlight the limitations of existing approaches and to identify potential research gaps that motivate the work presented in subsequent chapters of this thesis.

Overall, this chapter serves as a critical survey of existing mixed-signal design methodologies, providing a structured understanding of the challenges and opportunities in the development of low-power, high-resolution SAR ADC systems.

2.2 Self-Cascode Technique

The self-cascode transistor is a widely adopted technique for overcoming the gain and output resistance limitations of short-channel MOS transistors in low voltage analog and mixed-signal designs [113]. It is realized by vertically stacking two transistors of the same polarity, with their gates shorted together and an internal node formed between them, as

shown in Fig. 2.1. Typically, the upper device (M2) is designed with a larger aspect ratio than the lower device (M1), i.e.,

$$m = \frac{\beta_2}{\beta_1} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} > 1 \quad (2.1)$$

For correct operation, both devices must remain in conduction, which imposes the conditions $V_G - V_X - V_T > 0$ and $V_G - V_S - V_T > 0$, ensuring that M2 operates in saturation or linear region and M1 remains in linear region over a wide output voltage range. This biasing arrangement is fundamental to achieving the desired enhancement in output resistance without significantly increasing the minimum required drain–source voltage.

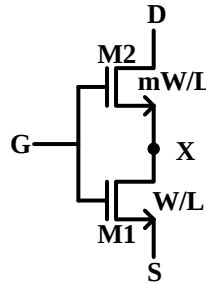


Fig. 2.1 Self cascode structure NMOS transistor

The operation of the self-cascode structure can be understood by analyzing the voltage distribution across the two transistors. Since M1 has a smaller aspect ratio, it develops a relatively small voltage drop across its drain-source terminals, effectively acting as a source degeneration element. This stabilizes the intermediate node voltage and allows M2 to experience a higher effective drain voltage, ensuring that it remains in saturation or linear region. As a result, variations in the output voltage at node D are largely absorbed

by M2, while the channel of M1 remains relatively unaffected. This significantly reduces channel-length modulation effects, leading to a substantial increase in output resistance.

From a large-signal perspective, the drain current of the composite device can be derived by equating the currents through M1 and M2. Since M1 works in the triode region, the current exhibits a quasi-linear dependence on the intermediate node voltage V_X , whereas M2 follows the square-law behavior characteristic of saturation. Solving the resulting equations yields an equivalent current expression that resembles that of a single transistor with an effective transconductance parameter $\beta_{eq} = \frac{\beta_1\beta_2}{\beta_1 + \beta_2}$. When $\beta_2 \gg \beta_1$, this simplifies to $\beta_{eq} \approx \beta_1$, indicating that the current driving capacity of the composite device is governed primarily by the smaller transistor. This is an important insight, as it implies that the gain improvement achieved by the structure does not come from increased transconductance, but rather from a substantial reduction in output conductance.

The small-signal model, shown in Fig. 2.2, further highlights the advantages of the self-cascode configuration. The lower transistor M1 can be approximated as a source degeneration resistance $r_{s,eff} \approx 1/g_{m1}$, which introduces local feedback and stabilizes the voltage at the intermediate node. As a result, variations in the drain voltage are attenuated before reaching the channel of M2, effectively suppressing channel length modulation. The overall output resistance can therefore be written as $r_{o,eff} \approx (1 + g_{m2}r_{o2})r_{o1}$, which, under practical design conditions, approaches $(m+1)r_o$ for large m . This substantial increase in output resistance directly translates into higher intrinsic gain $A_v = g_m * r_o$, making the structure particularly attractive for gain-critical stages.

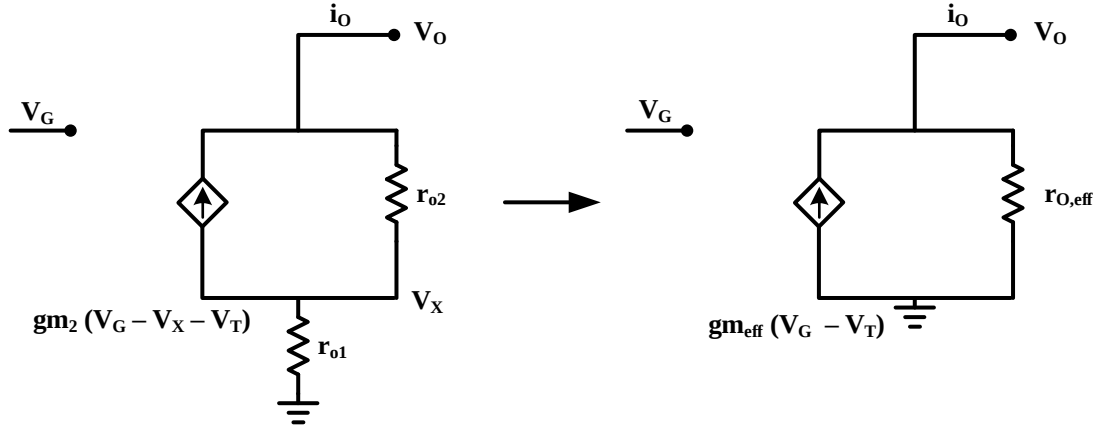


Fig. 2.2 Small-signal model of self-cascode transistor

A key advantage of the self-cascode over the conventional cascode lies in its voltage headroom requirement. In a traditional cascode, both transistors must remain in saturation, requiring a minimum voltage of approximately $V_{DSAT1} + V_{DSAT2}$, which becomes prohibitive in low-supply designs. In contrast, the self-cascode allows the lower device to operate in the linear region with a very small V_{DS1} , resulting in an overall saturation voltage nearly equal to that of a single transistor.

In terms of device sizing and layout, the composite structure offers an interesting trade-off between effective channel length and silicon area. Increasing the scaling factor m effectively increases the equivalent channel length, thereby improving output resistance, but also leads to larger parasitic capacitances at the internal node. These capacitances, particularly the gate to drain capacitance of M2, introduce additional poles in the frequency response and transfer the dominant pole to lower frequencies. Consequently, while the DC gain improves, the unity-gain bandwidth and overall speed are reduced. Analytical and simulation studies show that the transition time increases with m , highlighting a fundamental gain–bandwidth trade-off inherent to the structure.

From an application standpoint, the self-cascode composite transistor is particularly useful in current mirrors, where high output impedance is essential for accurate current

replication. By replacing a single transistor with a composite pair, the mirror exhibits reduced gain error and improved linearity without requiring additional voltage headroom. Similarly, in differential amplifiers and operational transconductance amplifiers (OTAs), the structure can be used to enhance gain while maintaining compatibility with low supply voltages. It is also advantageous in biasing networks and analog front-end circuits, such as those used in data converters, where power efficiency and area constraints are critical.

Overall, the self-cascode technique provides a robust and scalable solution for enhancing analog performance in modern CMOS technologies. By exploiting device stacking with asymmetric sizing and controlled region of operation, it achieves a significant improvement in output resistance and intrinsic gain, while preserving low-voltage operation and moderate area overhead. This makes it a key building block in designing of energy-efficient, high performance analog and mixed signal integrated circuits.

2.3 DTMOS-based Technique

The continuous compression of CMOS technologies and the consequent decrease in supply voltage have introduced substantial challenges in designing of high performance circuits, particularly due to the degradation of intrinsic gain, reduced voltage headroom, and limited signal swing. In this context, advanced device-level techniques such as DTMOS structure has emerged as effective solutions to sustain analog performance under low-voltage conditions [90, 102]. The DTMOS technique exploits the body terminal of MOS transistors as an active control node, enabling dynamic modulation of the threshold voltage through body biasing. By forward-biasing the body–source junction, the threshold voltage is reduced, which in turn enhances the effective overdrive voltage and improves current drive capability. The increasing the body bias significantly reduces the threshold voltage while increasing the drain current [135, 147].

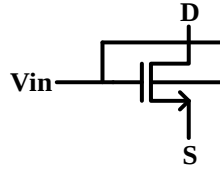


Fig. 2.3 DTMOS based NMOS transistor

The DTMOS-based NMOS shown in the Fig. 2.3 represents a modified MOS device configuration in which the gate and body (substrate) terminals are joined together, enabling adaptive threshold voltage control during operation. In this structure, the input V_{in} is employed simultaneously to both the gate and the body of the NMOS transistor, the gate and body terminals are connected together to dynamically control the threshold voltage, while the drain functions as the output node and the source is maintained at an appropriate reference potential determined by the circuit operation. Unlike a conventional NMOS transistor where the body is fixed (usually tied to ground), the DTMOS configuration allows the body potential to follow the gate voltage, thereby dynamically modulating the threshold voltage through the body effect.

When V_{in} increases, both the gate to source voltage V_{GS} and the body to source voltage V_{BS} increase simultaneously. Since the body is forward-biased with reference to the source, the threshold voltage V_{TH} is reduced according to the body effect relation. This reduction effectively increases the overdrive voltage ($V_{GS} - V_{TH}$), resulting in a higher drain current for the same input voltage compared to a conventional NMOS. Consequently, the DTMOS device exhibits enhanced transconductance and improved current driving capability, which is particularly beneficial in low-voltage operation where maintaining sufficient overdrive is challenging.

Overall, the DTMOS-based transistor provides an effective technique for enhancing device performance under low supply voltage conditions by dynamically lowering the threshold voltage during conduction while maintaining low leakage in the OFF state. This

makes it particularly useful in power constraint analog circuits, such as low-voltage comparators, SAR ADCs, and biomedical sensor interfaces.

In addition to amplifiers, the DTMOS technique proves highly beneficial in comparator and quantizer design, particularly in delta-sigma modulators operating at sub-1 V supply levels. One of the primary limitations in low-voltage systems is the restricted overlap between output voltage range of amplifiers and input range of subsequent stages, such as comparators. By employing the body terminal as the signal input in PMOS transistors, the DTMOS-based comparator achieves a rail-to-rail input range, effectively eliminating the need for additional level-shifting circuitry. Furthermore, the dynamic functioning of the comparator reveals a balance between input resolution and speed, as smaller differential inputs increase the decision delay due to reduced current imbalance in the input pair. Also, the transconductance of DTMOS is the addition of body transconductance (g_{m_b}) and gate transconductance (g_{m_g}), which supports gain enhancement. It is to be emphasized that in DTMOS, the threshold voltage changes dynamically with the applied voltage signal. Therefore, when the signal increases threshold voltage reduces and during signal reduction, threshold voltage increases. This is due to the fact that V_{sb} is changing dynamically with applied signal which thereby is changing the threshold voltage.

Despite its advantages, there are several practical limitations of the technique including the implementation of an NMOS DTMOS layout which requires triple-well technology to enable independent body biasing, which results in an increase in the overall silicon area. Additionally, the body terminal exhibits larger parasitic capacitances due to well structures, making it unsuitable for high-frequency signal paths. Care must also be taken to limit the forward body bias to avoid excessive junction currents. Nevertheless, when judiciously applied, DTMOS offers a powerful means of improving low-voltage analog performance by enabling threshold voltage reduction, extended input range, and simplified circuit topologies.

2.4 Cross-Coupled Regenerative Latch Structure

The cross-coupled regenerative latch is a nonlinear, positive-feedback-based circuit topology that serves as the core decision-making element in high-speed comparators, sense amplifiers, and bistable memory elements [120]. Its operation relies on the rapid amplification of a small differential input into a full logic-level output through regenerative action. Structurally, the latch consists of two identical branches forming a differential pair, where each output node is connected to the gate of the opposite transistor, creating a cross-coupled loop [129]. This configuration establishes a bistable system with two stable equilibrium points, corresponding to logic ‘0’ and ‘1’, and one metastable point where both outputs are equal.

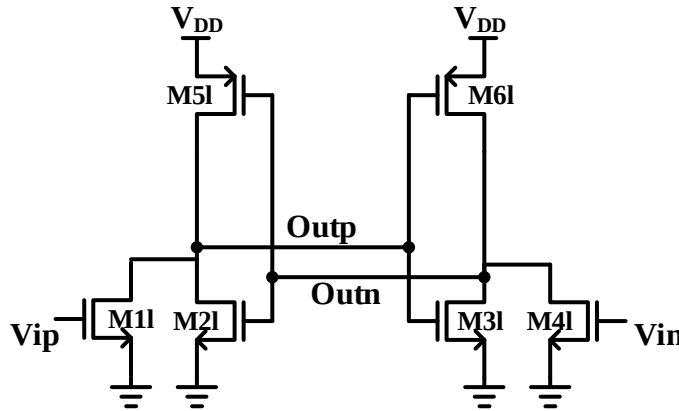


Fig. 2.4 Cross coupled regenerative latch

The cross-coupled regenerative latch shown in the Fig. 2.4 is a fundamental decision-making circuit widely used in dynamic comparators and sense amplifiers because of its capability to rapidly amplify small differential inputs into full-swing digital outputs through positive feedback [137]. The structure consists of two symmetrical branches formed by PMOS transistors M5l and M6l connected to V_{DD} , and NMOS input transistors M1l, M2l, M3l, and M4l connected to ground. The nodes Outp and Outn serve as both output nodes and internal feedback nodes, which are cross-coupled such that the output of each branch controls the opposite branch. The inputs V_{ip} and V_{in} are employed at the

gates of the NMOS transistors, creating a differential current path that initiates the regeneration process.

During operation, when a small differential input voltage is applied ($V_{ip} \neq V_{in}$), one side of the latch begins to conduct slightly more current than the other. For instance, if $V_{ip} > V_{in}$, transistor M1l (and corresponding branch) conducts more strongly, pulling the Outp node slightly toward ground. This small voltage drop at Outp reduces the gate voltage of the opposite PMOS transistor M6l, causing it to turn ON more strongly and pull Outn toward V_{DD} . As Outn rises, it further suppresses conduction in the left branch while enhancing conduction in the right branch, creating a strong positive feedback loop. This regenerative action continues exponentially, rapidly driving one node (Outn) to V_{DD} and the other node (Outp) to ground.

The key feature of this latch is the cross-coupling between Outp and Outn, which ensures that any small initial imbalance is reinforced and amplified. The regeneration speed depends on the effective transconductance of the transistors and capacitance at output nodes, with faster operation achieved for higher g_m and lower parasitic capacitance. This structure inherently exhibits bistable behavior, meaning it has two stable states corresponding to logic '0' and '1', and one unstable metastable state when both outputs are equal. If the input difference is very small, the latch may temporarily remain in this metastable state before resolving to one of the stable states due to noise or mismatch.

Additionally, the PMOS transistors M5l and M6l act as active loads, providing pull-up action, while the NMOS transistors form the pull-down network controlled by the input signals. The symmetry of the circuit is critical to minimize offset and ensure accurate comparison. Any mismatch between transistors or parasitic capacitances at Outp and Outn can introduce input-referred offset voltage, affecting precision.

The regeneration process can be described mathematically by examining the differential voltage ΔV . Under small-signal conditions, the rate of change of this differential voltage follows an exponential relationship:

$$\frac{d(\Delta V)}{dt} = \frac{gm}{C_l} * \Delta V \quad (2.2)$$

which leads to

$$\Delta V(t) = \Delta V(0) * e^{\frac{t}{\tau}} \quad (2.3)$$

where $\tau = C_l/gm$

Here, gm represents the effective transconductance of the latch transistors, and C_l is the total capacitance at each output, including parasitic capacitances. This equation highlights that the latch behaves as an exponential amplifier, where the regeneration speed is determined by the ratio gm/C_l . A higher transconductance or lower node capacitance results in faster decision time, which is critical in high-speed data converters.

An important characteristic of the regenerative latch is its metastability behavior. If the input voltage is extremely small or zero, the latch may remain in a quasi-stable state for a finite time before resolving to one of the stable states due to noise or mismatch. The resolution time in such cases increases logarithmically with decreasing input difference, which imposes a fundamental limit on comparator speed and accuracy. This is particularly critical in high-resolution ADCs, where the input difference near decision boundaries is very small.

Non-idealities such as device mismatch, thermal noise, and flicker noise introduce an input-referred offset voltage, which determines the minimum detectable signal. Mismatch in threshold voltage, mobility, or transistor dimensions between the two branches causes asymmetry in the regenerative process, biasing the latch toward one output state. To mitigate these effects, careful layout methods such as common-centroid placement, inter-

digitation, and symmetric routing are employed. Additionally, preamplifier stages are often placed before the latch to amplify the input signal and reduce the impact of latch offset and kickback noise [153, 157].

From a power perspective, the regenerative latch is highly efficient because it consumes dynamic power only during the evaluation phase, with negligible static current in steady states. This makes it particularly suitable for low power and high speed applications such as SAR ADCs, where the comparator is activated only during bit decision cycles.

In scaled CMOS technologies, reduced supply voltage and limited overdrive voltage degrade the transconductance g_m , thereby increasing regeneration time. To address this, advanced techniques such as body biasing (DTMOS) or self-cascode structures can be incorporated to enhance effective transconductance and improve latch sensitivity under low-voltage conditions.

In summary, the cross-coupled regenerative latch operates as a high-gain, nonlinear amplifier that exploits positive feedback to achieve rapid signal amplification and binary decision-making. Its performance is governed by the interplay between transconductance, load capacitance, device matching, and parasitic effects, making it a critical component in the design of high speed, low power analog systems.

2.5 Shared-Charge Reset Technique

In dynamic latch comparators, the reset phase plays a crucial role in establishing proper initial conditions for accurate and fast regeneration during evaluation. Conventionally, the output nodes are either completely charged to V_{dd} or discharged to ground, which results in large voltage swings and increased power consumption. To overcome this limitation, a shared-charge reset technique is illustrated in Fig. 2.5, where a pass transistor (S_c) is introduced between the two output nodes [103].

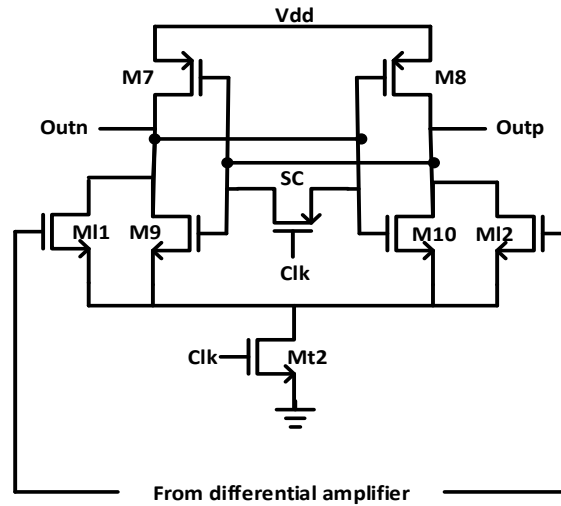


Fig. 2.5 Shared charge logic in cross couple latch

During first phase ($\text{Clk} = 0$), the transistor Mt2 is OFF, eliminating static current flow. At the same time, the reset transistors initialize internal nodes, and the shared-charge transistor becomes active, shorting the output nodes Outp and Outn . Since one of these nodes is typically at a higher voltage and the other at a lower voltage from the previous evaluation cycle, charge redistribution occurs between them. As a result, both output nodes settle to an intermediate voltage level, approximately around $V_{\text{dd}}/2$, instead of being driven to full rail voltages.

When the circuit enters the second phase ($\text{Clk} = 1$), the same Mt2 is ON and the reset transistors turn OFF. The differential input signal causes the internal nodes to discharge at different rates, generating a voltage difference that triggers the regenerative latch. Unlike conventional designs, the regeneration in this architecture begins from a mid-level voltage rather than rail-to-rail conditions, significantly reducing the required voltage swing. This leads to faster decision-making and lower dynamic power consumption.

The shared-charge technique offers multiple advantages. First, it reduces delay by minimizing the voltage excursion required during regeneration. Second, it lowers power consumption by avoiding full charging and discharging of output nodes. Third, it

simplifies clocking requirements, as the use of NMOS tail transistors eliminates the need for complementary clock signals. Overall, the shared charge reset technique redefines the conventional notion of reset in dynamic comparators by transitioning from full-state initialization to charge-preserving preconditioning [149]. By positioning the latch near its metastable point prior to evaluation, it enables faster regeneration, reduced energy dissipation, and improved overall performance, making it a highly effective strategy for modern low voltage, high speed analog systems like SAR ADCs and other data conversion interfaces.

2.6 Auxiliary Inverter Technique

The auxiliary inverter technique is an advanced enhancement introduced in the latch stage of a dynamic comparator to significantly improve regeneration speed by increasing both the initial differential voltage and the effective transconductance of the latch [49, 108]. Unlike traditional designs where intermediate transistors do not contribute to the latch transconductance during regeneration, this auxiliary inverter pair actively participates in both the early and later phases of the decision process.

Fig. 2.6 illustrates the schematic of the proposed comparator incorporating an auxiliary inverter pair within a double-tail architecture. The primary objective of this design is to reduce the latch regeneration time by effectively increasing the equivalent transconductance of the regenerative stage. To achieve this, additional transistors forming auxiliary inverters (M_{r1} – M_{r4}) are introduced at the output nodes. These auxiliary inverters act as voltage-dependent current sources and sinks, providing additional drive strength during the regeneration phase without introducing significant capacitive loading [129].

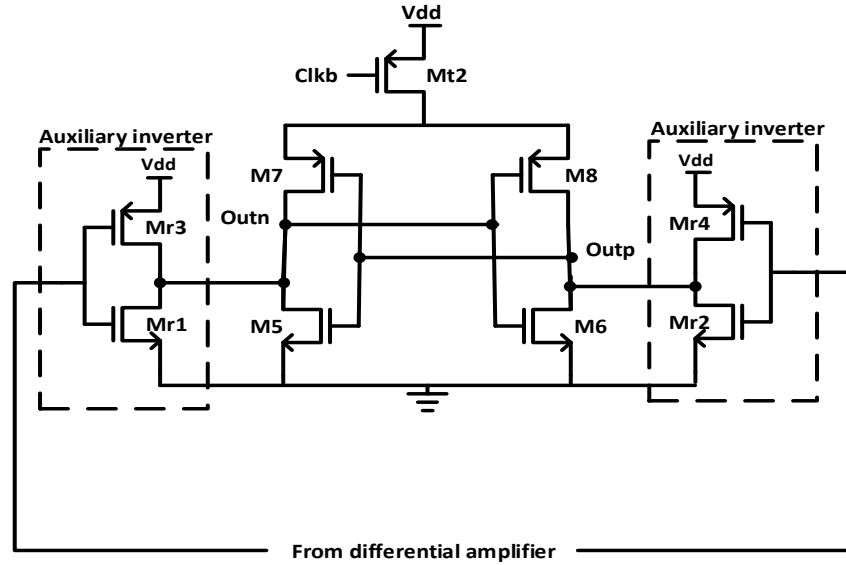


Fig. 2.6 Auxiliary inverter pair technique

During first stage ($\text{Clk} = 0$), Mt2 is turned OFF, ensuring zero static current. Internal nodes are precharged to V_{dd} , and the auxiliary inverter is initialized such that the NMOS devices (Mr1 , Mr2) are ON while the PMOS devices (Mr3 , Mr4) remain OFF. This establishes proper initial conditions at the output nodes without unnecessary switching activity.

When the circuit enters second stage ($\text{Clk} = 1$), the tail transistor is turned ON. As regeneration begins, the auxiliary inverter pair actively assists the latch operation. Specifically, one inverter branch provides additional pull-up current while the other provides pull-down current, depending on the polarity of the differential input. For example, when one output node starts discharging, the corresponding NMOS device in the auxiliary inverter strengthens the discharge path, while the complementary PMOS device assists in charging the opposite node. This dual action enhances the effective regeneration current and accelerates the transition of output nodes toward rail voltages.

Unlike conventional latch structures, where regeneration relies solely on cross-coupled feedback, this design benefits from additional current boosting through the auxiliary

inverter pair, resulting in faster voltage amplification and reduced delay. Importantly, this improvement is achieved without requiring multi-phase clocking or introducing significant parasitic capacitance at the output nodes [157].

Other benefit of this technique is to preserve the low static power nature of dynamic comparators, as the auxiliary inverter operates only during the evaluation phase and does not introduce continuous current paths. However, careful design considerations are necessary, including proper sizing of the auxiliary transistors to balance speed improvement against increased parasitic capacitance and potential mismatch-induced offset.

Overall, the auxiliary inverter technique enhances comparator performance by acting as a dynamic gain booster and current accelerator within the latch stage, simultaneously increasing the effective transconductance and initial differential voltage. This results in faster regeneration, improved sensitivity to small input signals, and reduced delay, making it usable for high speed and high resolution ADC applications in modern CMOS technologies.

2.7 Capacitive DAC Techniques

The capacitive Digital-to-Analog Converter (CDAC) is a fundamental component in SAR ADCs, playing a dual role of sampling the input and generating reference voltages during the conversion process. Its design critically influences the complete performance of the ADC in terms of power dissipation, area, linearity and conversion speed. As SAR ADCs are broadly adopted in low power and medium to high resolution applications, the optimization of CDAC architecture has been a major focus in mixed-signal circuit design.

In conventional implementations, the CDAC is realized using an array of binary-weighted capacitors, which enables straightforward charge redistribution to approximate the input signal. However, this approach often leads to significant switching energy, large total capacitance, and increased silicon area, especially for higher resolution designs.

Additionally, capacitor mismatch and parasitic effects can degrade linearity, resulting in errors like DNL and INL.

To address these limitations, several advanced switching techniques and structural modifications have been described in the literature. These include energy-efficient switching schemes such as monotonic switching and V_{cm} -based switching, which aim to reduce switching power and improve settling behavior. Furthermore, architectural innovations like the split-capacitor technique help in minimizing the total capacitance and area without significantly compromising accuracy.

This section provides an overview of various capacitive DAC techniques, focusing on their operating principles, advantages, and inherent trade-offs. The discussion highlights how different switching strategies and capacitor configurations impact key performance metrics such as energy efficiency, linearity, and implementation complexity, thereby guiding the selection of suitable CDAC architectures for modern low-power SAR ADC designs.

2.7.1 Conventional Binary-Weighted Capacitor Structures

Figure 2.7 illustrates a 5-bit binary-weighted CDAC commonly used in SAR ADCs for generating analog reference voltages during the conversion process [6, 19]. The DAC consists of a comparator, an array of capacitors whose values are scaled in binary ratios such as C , $C/2$, $C/4$, $C/8$ and so on. Each capacitor is connected through a switch network that allows its top plate to be selectively connected either to the positive reference voltage (V_{refp}) or the negative reference voltage (V_{refn}). The bottom plates of all capacitors are connected together to form the DAC output node, which is interfaced with the comparator input.

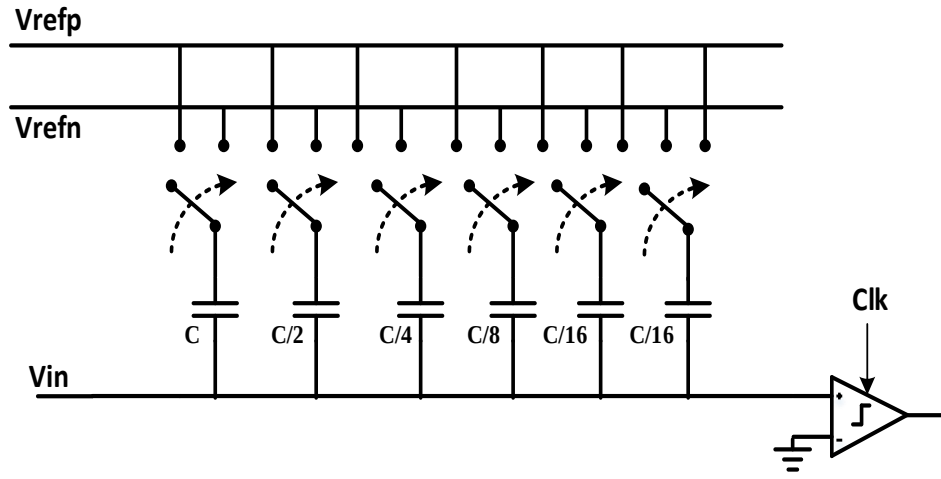


Fig. 2.7 5-bit binary weighted DAC

During the sampling phase, the capacitor array samples the input signal V_{in} . In the subsequent conversion phase, the SAR logic controls the switches sequentially from the MSB capacitor to the LSB capacitor. Depending on the comparator output, each capacitor is switched either to V_{refp} or V_{refn} , thereby redistributing charge within the capacitor array. Since the capacitor values follow binary weighting, each capacitor contributes a voltage proportional to its binary significance. The largest capacitor C represents the MSB and contributes the highest voltage step, while smaller capacitors provide progressively finer voltage adjustments.

The output voltage generated by the capacitive DAC is determined by charge conservation and can be expressed as:

$$V_{DAC} = \sum_{i=1}^N b_i * \frac{C_i}{C_{total}} * V_{ref} \quad (2.4)$$

where b_i represents the digital control bit, C_i is the corresponding capacitor value and C_{total} is the total capacitance of the array.

The binary-weighted DAC offers simple implementation and accurate binary search operation in SAR ADCs. However, for higher resolutions, the largest capacitor value increases exponentially, leading to larger silicon area, higher switching energy, and increased sensitivity to capacitor mismatch and parasitic capacitances [48]. Another important limitation is mismatch between capacitors, which introduces errors in the DAC output. Since the accuracy of the CDAC directly determines the linearity of the ADC, any deviation in capacitor ratios leads to DNL and INL. The most significant errors arise from mismatch in the largest capacitors, as they contribute the highest weight. From an energy perspective, the conventional binary-weighted switching scheme is inefficient because it involves large voltage swings across capacitors during each bit cycle. This has led to the development of improved switching techniques such as monotonic switching, V_{cm} -based switching and split capacitor arrays, which reduce switching energy and total capacitance while maintaining accuracy. Despite these drawbacks, the conventional binary-weighted CDAC remains an important reference architecture due to its conceptual simplicity, ease of analysis, and direct mapping between digital codes and analog output.

2.7.2 Monotonic Switching Technique

The monotonic switching technique is an energy-efficient capacitor switching strategy employed in SAR ADCs to minimize dynamic power consumption and simplify charge redistribution in the capacitive DAC, while maintaining accurate conversion [21, 92]. Unlike the conventional binary-weighted switching scheme—where capacitors are repeatedly toggled between V_{ref} and ground, leading to large switching energy—the monotonic approach ensures that the DAC output voltage evolves in a single direction throughout the conversion process, thereby eliminating redundant charge/discharge cycles. This technique is fundamentally based on principle of charge conservation, but modifies the initial conditions and switching sequence to reduce energy dissipation.

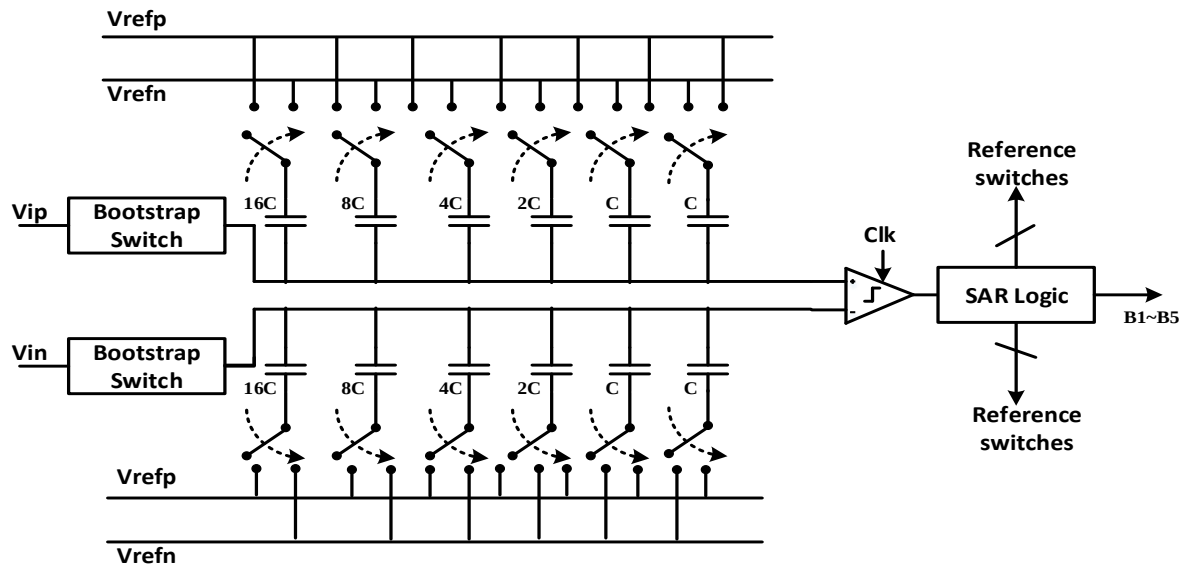


Fig. 2.8 Monotonic DAC switching scheme in 5-bit SAR ADC

Figure 2.8 illustrates a monotonic switching CDAC used in a fully differential 5-bit SAR ADC architecture. The DAC consists of two symmetrical capacitor arrays connected to the positive and negative comparator inputs. Each array contains binary-weighted capacitors ($16C$, $8C$, $4C$, $2C$, C , C), controlled by switches that connect the capacitor top plates either to V_{refp} or V_{refn} . The inputs V_{ip} and V_{in} are sampled through bootstrap switches to improve sampling linearity and reduce signal-dependent switch resistance.

During the sampling stage, the input differential signal is sampled on the capacitor arrays while all bottom plates are initially connected to a common reference level. After sampling, the SAR conversion process begins. Unlike the conventional binary-weighted DAC, where capacitors may switch repeatedly between V_{refp} and V_{refn} , the monotonic switching scheme ensures that capacitor switching occurs in only one direction during the conversion process. Typically, all capacitors are initially connected to one reference voltage, and during successive approximation, selected capacitors are switched monotonically toward the opposite reference depending on the comparator decision.

The conversion starts with MSB. Based on the comparator output, the corresponding capacitor in one DAC branch remains unchanged while the capacitor in the opposite

branch is switched. Subsequent capacitors are then switched sequentially according to SAR logic decisions. Since only either side of the differential DAC actively switches during each comparison cycle, the total switching activity and charge redistribution energy are significantly reduced.

The monotonic switching technique offers several important advantages:

- Reduced switching energy: Since capacitors switch only once in a single direction, unnecessary charging/discharging is avoided.
- Lower power consumption: Reduced switching activity directly lowers dynamic power.
- Improved common-mode stability: The differential structure helps maintain a relatively constant common-mode voltage during conversion.
- Reduced capacitor stress and noise: Smaller voltage transitions reduce switching noise and improve linearity.

In summary, the monotonic switching technique represents a significant improvement over conventional binary-weighted switching by reducing energy consumption, simplifying switching operations, and improving speed through reduced voltage transitions. By ensuring that the DAC output evolves in a single direction during conversion, it eliminates redundant charge redistribution and enables highly efficient SAR ADC implementations suitable for modern low-power, high-performance applications.

2.7.3 Vcm-Based Switching Technique

The Vcm-based switching technique is an advanced and highly energy-efficient capacitor switching method used in SAR ADCs to significantly reduce switching energy, improve linearity, and maintain a stable common-mode voltage at the comparator input. This technique modifies both the sampling scheme and the reference voltage levels used during conversion, thereby addressing key limitations of conventional and monotonic switching methods [104]. In contrast to traditional approaches where capacitors are switched

between V_{ref} and ground, the V_{cm} -based technique utilizes a common-mode reference voltage V_{cm} (typically $V_{ref}/2$) as a central operating point, which plays a crucial role in minimizing voltage swings and energy consumption.

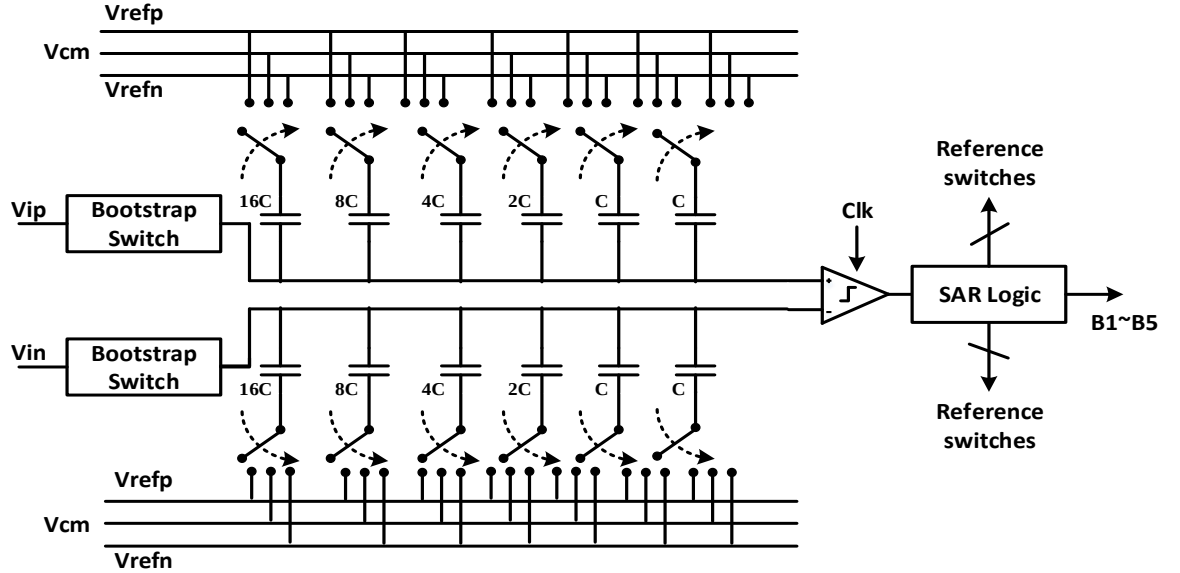


Fig. 2.9 V_{cm} -based DAC switching scheme for 5-bit SAR ADC

Figure 2.9 illustrates a V_{cm} -based capacitive DAC switching scheme used in a fully differential 5-bit SAR ADC architecture [114]. In this approach, an additional reference level, namely the common-mode voltage (V_{cm}), is introduced along with the conventional reference voltages V_{refp} and V_{refn} . The DAC consists of two symmetrical binary-weighted capacitor arrays connected to the differential comparator inputs. Each capacitor can be selectively switched among V_{refp} , V_{refn} and V_{cm} through the SAR-controlled switching network.

During the sampling stage, the inputs V_{ip} and V_{in} are sampled onto the capacitor arrays through bootstrap switches, which help maintaining constant switch resistance and improve linearity. Initially, most capacitor bottom plates are connected to the common mode voltage V_{cm} , which establishes a balanced common-mode condition across the differential DAC outputs.

In successive approximation phase, the SAR logic controls capacitor switching based on comparator decisions. Unlike conventional binary-weighted switching, where capacitors transition directly between V_{refp} and V_{refn} , the V_{cm} -based scheme performs switching around the common-mode voltage. Typically, the first comparison is carried out without consuming DAC switching energy because the capacitor arrays are already initialized around V_{cm} . In subsequent bit cycles, selected capacitors are switched between V_{cm} , V_{refp} , and V_{refn} depending on the comparator output.

An important benefit of this approach is that the voltage swing across the capacitor array is significantly reduced. Since many capacitor transitions occur between V_{cm} and one reference level instead of full-scale transitions between V_{refp} and V_{refn} , the overall switching energy decreases substantially. In addition, maintaining the DAC output around a constant common-mode level improves comparator stability and reduces common-mode disturbance during conversion [125].

The V_{cm} -based DAC switching technique provides several important benefits:

- Significant reduction in switching energy
- Lower dynamic power consumption
- Improved common-mode stability
- Reduced switching noise and better linearity
- Smaller voltage transitions across capacitors

However, the V_{cm} -based switching technique also introduces certain design complexities. It requires precise generation and control of the common-mode voltage, as any deviation in V_{cm} directly affects conversion accuracy. Additionally, the switching logic is more complex compared to monotonic schemes, and careful timing is required to ensure correct charge redistribution [146].

In summary, the V_{cm} -based switching technique represents a highly optimized approach for SAR ADCs, offering substantial reductions in switching energy, improved speed, and

enhanced comparator performance through common-mode stabilization. By leveraging a mid-level reference voltage and symmetric switching operations, it overcomes the limitations of earlier techniques and is widely adopted in modern low-power, high-performance ADC designs.

2.7.4 Split Capacitor Technique

The split capacitor technique is a widely adopted optimization of the conventional binary-weighted CDAC in SAR ADCs, developed to overcome the exponential growth of capacitance, area, and switching energy associated with high-resolution designs [25]. In a conventional N-bit binary-weighted CDAC, the total capacitance scales as $C_{\text{total}} = (2^N - 1)C$, making it impractical for resolutions beyond 10–12 bits due to large silicon area, increased parasitic effects, and slower settling.

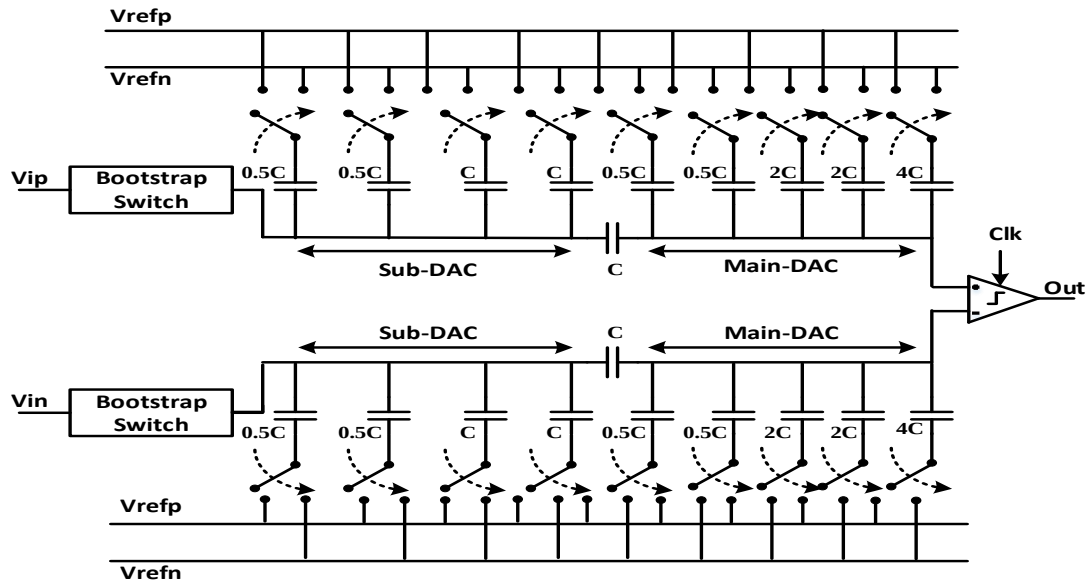


Fig. 2.10 Split capacitor DAC technique for 5-bit SAR ADC

The split capacitor approach addresses this by partitioning the capacitor array into two sub-arrays—an MSB array (Main-DAC) and an LSB array (Sub-DAC)—connected through an attenuation (bridge) capacitor, thereby preserving the required binary

weighting while drastically reducing the total capacitance [38, 40]. Figure 2.10 illustrates a split-capacitor DAC architecture employed in a 5-bit fully differential SAR ADC. The split-capacitor technique divides the DAC into two smaller sections: a Main-DAC responsible for the Most Significant Bits (MSBs) and a Sub-DAC responsible for the Least Significant Bits (LSBs). Both sections are connected through a bridge capacitor C , which scales the contribution of the sub-DAC to maintain correct binary weighting.

In the shown architecture, the Main-DAC contains larger capacitors such as $4C$, $2C$, C and $0.5C$ which generate coarse voltage steps corresponding to higher-order bits. The Sub-DAC contains smaller capacitors used to resolve lower-order bits with finer voltage resolution. The bridge capacitor between the two arrays ensures that the voltage contribution from the sub-DAC is attenuated appropriately before reaching the comparator input. The differential implementation uses two identical capacitor arrays connected to the positive and negative comparator inputs, thereby improving common-mode noise rejection and linearity.

During the sampling phase, the analog input signals V_{ip} and V_{in} are sampled onto the capacitor arrays through bootstrap switches, which improve sampling linearity by maintaining nearly constant switch resistance. During the successive approximation phase, the SAR logic sequentially controls the capacitor switching between V_{refp} and V_{refn} . The Main-DAC first resolves the MSBs through larger voltage transitions, while the Sub-DAC subsequently refines the conversion by generating smaller voltage steps for the LSBs.

The primary advantage of the split-capacitor DAC is the significant reduction in total capacitance compared to a conventional binary-weighted array. Instead of requiring very large capacitor ratios, the architecture achieves equivalent binary weighting through capacitive attenuation [83, 85, 116, 122]. This leads to:

- Reduced silicon area

- Lower switching energy and dynamic power consumption
- Improved DAC settling speed
- Reduced RC delay
- Lower loading on the comparator input

However, the technique introduces several critical design challenges. The precision of the DAC heavily depends on the precise value of the bridge capacitor. Any mismatch or parasitic capacitance at the intermediate node (between MSB and LSB arrays) can introduce gain errors, leading to INL and DNL degradation. Another important consideration is the parasitic capacitance at the bridge node, which can be comparable to the LSB capacitors and hence significantly affect performance. Shielding techniques, dummy structures, and careful routing are essential to minimize these parasitics.

In summary, the split capacitor technique provides an elegant solution to the scalability limitations of conventional CDACs by reducing capacitance, power, and area while maintaining resolution through capacitive attenuation. Despite the added design complexity and sensitivity to parasitics, it remains a highly effective and widely used approach in modern SAR ADCs, particularly for applications requiring a balance between high resolution, low power, and compact silicon implementation.

2.8 SAR Logic and Control Techniques

The SAR logic forms the digital backbone of a SAR ADC, orchestrating the step-by-step conversion of the analog input into a corresponding digital output. It governs the timing and sequence of operations, including sampling, bit-wise comparison, DAC switching and final code generation. The efficiency of the SAR logic directly impacts the total speed, power consumption, and robustness of the converter, making it a critical component in mixed-signal system design.

In its basic form, SAR logic implements a binary search algorithm to iteratively coincide on the digital representation of the input signal. This process involves setting and resetting bits based on comparator decisions, requiring precise synchronization between the digital control circuitry, the capacitive DAC, and the comparator. Traditionally, this functionality has been realized using synchronous sequential logic driven by a global clock, which simplifies design but may introduce limitations in terms of speed and power efficiency due to clock distribution and unnecessary switching activity.

To overcome these challenges, various advanced SAR control techniques have been developed. These include optimized sequential logic implementations, efficient binary search algorithms, and asynchronous control schemes that eliminate the need for a high-frequency global clock. Asynchronous approaches, in particular, offer significant advantages in reducing power consumption and improving conversion speed by allowing each bit decision to proceed immediately after the comparator resolves, rather than waiting for a fixed clock edge.

This section presents an overview of different SAR logic and control methodologies, emphasizing their operational principles and design trade-offs. The discussion focuses on how these techniques influence timing complexity, energy efficiency, scalability, and ease of integration, providing a foundation for selecting appropriate control strategies in modern low-power and high-performance SAR ADC architectures.

2.8.1 Conventional Sequential Logic Techniques

The conventional sequential logic technique used in SAR ADCs forms the digital backbone responsible for controlling the bit-wise approximation process and coordinating the interaction between the comparator and the capacitive DAC [35, 36]. In this approach, the SAR logic is typically implemented using a chain of flip-flops, shift registers, and combinational control circuits that operate synchronously with a clock signal. The conversion process follows a binary search algorithm, where each bit is resolved

sequentially starting from MSB to LSB. At the beginning of the conversion cycle, the SAR register is initialized, usually by setting the MSB to logic '1' while keeping all other bits at '0'. This digital code is applied to the CDAC, generating a corresponding analog voltage that is compared with the sampled input signal using a comparator.

Based on the comparator output, the SAR logic determines whether the trial bit should be retained or cleared. If the DAC output is less than the input signal, the bit remains set; otherwise, it is reset to zero. This decision is stored in a flip-flop corresponding to that bit position. The logic then shifts to the next bit, repeating the process until all bits are resolved. The sequential nature of this technique ensures that only one comparison is performed per clock cycle, leading to a total conversion time of N clock cycles for an N -bit ADC. The control logic also generates timing signals required for sampling, DAC switching, and comparator evaluation, ensuring proper synchronization between analog and digital blocks.

From an implementation perspective, dynamic or static D flip-flops are commonly used to store bit decisions, while a shift register mechanism propagates the control signal across bit positions [96]. A finite state machine (FSM) may also be employed to manage the overall conversion sequence, including reset, sampling, and evaluation phases. While this conventional sequential approach is simple, robust, and easy to design, it introduces limitations in terms of speed and power efficiency. Since each bit decision requires a separate clock cycle, the overall conversion speed is constrained, making it less suitable for high-speed applications. Additionally, the repeated clocking of flip-flops and control circuitry contributes to dynamic power consumption.

Despite these limitations, the conventional sequential SAR logic remains widely used due to its deterministic operation, low hardware complexity, and ease of integration. It provides a reliable framework for moderate-speed and medium-resolution ADCs, particularly in applications where simplicity and accuracy are prioritized over ultra-high speed. Advances in SAR logic design, such as asynchronous and event-driven techniques,

have been proposed to overcome the speed and power limitations of conventional sequential logic while retaining its fundamental operating principles.

2.8.2 Binary Search Implementation

The binary search implementation in SAR ADCs is the fundamental algorithm that enables efficient and systematic conversion of an analog input signal into its corresponding digital representation [106]. This technique operates by successively narrowing down the range in which the input signal lies, using a divide-and-conquer approach analogous to a binary search in digital systems [118]. At the start of the conversion process, the sampled analog input is held constant, and the SAR logic initializes the MSB to logic ‘1’, while all other bits are set to ‘0’. This digital code is applied to the capacitive DAC, generating an analog voltage equal to half of the reference voltage ($V_{ref}/2$). The comparator then compares this DAC output with the input signal V_{in} . If $V_{in} > V_{DAC}$, the MSB is retained; otherwise, it is reset to ‘0’.

Following this decision, the SAR logic proceeds to the next bit, setting the second most significant bit (MSB-1) to ‘1’ while keeping the previously decided MSB unchanged. The DAC now generates a new analog voltage corresponding to the updated digital code and updates the analog estimate according to the second-bit weight. This process continues iteratively for each subsequent bit, with each step halving the remaining error range. At the i^{th} step, the DAC output represents the sum of previously determined bits plus a trial contribution of $V_{ref}/2^i$. The comparator decision determines whether this contribution should be retained or removed, thereby refining the estimate of the input signal.

Mathematically, after N comparison cycles for an N -bit ADC, the final digital output D satisfies:

$$V_{DAC} = V_{ref} * \frac{D}{2^N} \approx V_{in} \quad (2.5)$$

where D is the digital approximation of the input signal. The error after each step is reduced by a factor of two, ensuring convergence within N clock cycles. This makes the binary search algorithm highly efficient, as it achieves full resolution with a linear number of steps relative to the number of bits.

From a circuit perspective, the implementation of binary search relies on tight coordination between the SAR register, DAC and comparator. The SAR logic generates control signals to switch the capacitor array, while the comparator provides a single-bit decision at each step. The simplicity of this algorithm allows for low hardware complexity and deterministic operation, which is a key advantage over other ADC architectures. However, the sequential nature of the process limits the maximum conversion speed, as each bit must be resolved before proceeding to the next.

Despite this limitation, binary search remains the cornerstone of SAR ADC operation due to its excellent balance between speed, power efficiency and accuracy. It is particularly well-suited for medium-to-high resolution applications where moderate sampling rates and low power consumption are required, such as in biomedical devices, IoT sensors, and portable electronics.

2.8.3 Asynchronous Control Techniques

The asynchronous control technique in SAR ADCs is an advanced timing strategy that eliminates the dependence on a global high-frequency clock for bit cycling, thereby improving speed and reducing power consumption [124]. Unlike conventional sequential logic, where each bit decision is synchronized to a fixed clock period, the asynchronous approach allows each conversion step to proceed after finishing previous comparator decision. This is achieved using event-driven control logic, where the comparator output itself triggers the next stage of the SAR operation. As a result, the conversion time becomes data-dependent rather than being constrained by a worst-case clock period, leading to faster average conversion speed.

In an asynchronous SAR architecture, the comparator generates a “ready” or “done” signal once it completes the comparison between the input signal and the DAC output. This signal is used to activate the SAR logic, which updates the corresponding bit and reconfigures the DAC for the next comparison. Instead of using flip-flops driven by a global clock, the design typically employs dynamic latches, delay elements, and handshaking circuits to propagate control signals through the bit cycles. Each stage operates only when required, thereby reducing unnecessary switching activity and dynamic power consumption. The absence of a high-speed clock also simplifies clock distribution and minimizes clock-related issues such as skew and jitter.

From a timing perspective, the total conversion time in an asynchronous SAR ADC is given by the sum of individual bit decision times:

$$T_{conv} = \sum_{i=1}^N (t_{comp,i} + t_{logic,i} + t_{DAC,i}) \quad (2.6)$$

where t_{comp} , t_{logic} , and t_{DAC} represent the comparator decision time, logic delay, and DAC settling time for each bit, respectively. Since each stage proceeds immediately after the previous one completes, the overall conversion time is optimized, especially when the comparator resolves quickly for large input differences in early bit cycles.

One of the major advantages of asynchronous control is its energy efficiency. Because the circuit operates in an event-driven manner, power is consumed only when transitions occur, avoiding the constant toggling associated with synchronous clocked systems. This makes it highly suitable for low-power applications such as IoT devices, biomedical sensors and portable electronics. Additionally, asynchronous operation can improve robustness to PVT variations, as the timing automatically adapts to the actual circuit conditions.

However, the design of asynchronous SAR logic introduces challenges, including increased circuit complexity, sensitivity to noise and glitches, and the need for careful timing coordination to avoid metastability or race conditions. Handshaking circuits and

delay matching must be carefully designed to ensure reliable operation [139, 145]. Despite these challenges, asynchronous control techniques have gained significant attention in modern SAR ADC designs due to their ability to achieve higher speed and lower power consumption compared to conventional synchronous approaches, making them highly attractive for advanced low-voltage and high-performance applications.

2.9 Conventional Comparator

After discussing the various device-level enhancement techniques, DAC switching methodologies and SAR control strategies, it is important to examine the operation of the conventional comparator architecture that forms the fundamental decision-making block in most SAR ADC systems. Understanding the structure, operation and limitations of the conventional comparator provides a useful reference for evaluating the performance improvements achieved by the advanced comparator techniques discussed in subsequent chapters.

The conventional comparator architecture consists of two primary stages, namely the preamplifier stage and the latch stage, as shown in Fig. 2.11, which operate sequentially to convert a small analog input difference into a full-scale digital output. The preamplifier stage functions as an input sensing and amplification block, while the latch stage performs the final decision through regenerative positive feedback. The operation of the preamplifier stage is divided into two distinct phases: pre-charge and evaluation. During its first phase ($\text{Clk} = 0$), the PMOS transistors M3c and M4c are turned ON, charging the parasitic or explicit capacitances at nodes P and Q (denoted as C_P and C_Q) to the supply voltage V_{dd} . As these nodes are precharged to a high level, the subsequent static latch stage is initialized accordingly. Specifically, the NMOS transistors M1l and M4l in the latch turn ON, which discharges the output nodes Out_p and Out_n to ground, thereby ensuring a well-defined initial condition. Simultaneously, the PMOS transistors M6l and M7l are turned ON, while M5l, M8l, and the NMOS devices M2l and M3l remain OFF, maintaining symmetry and preventing any unintended regeneration during this phase.

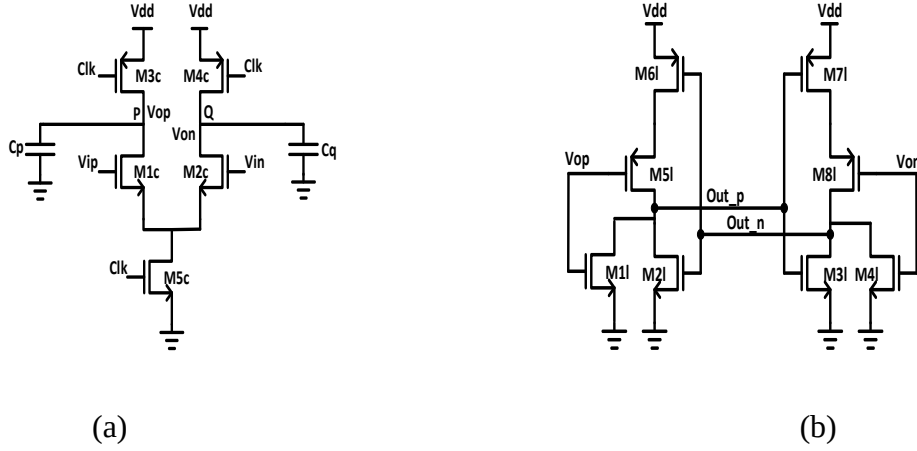


Fig. 2.11 Conventional comparator stages (a) preamplifier and (b) static latch

When the clock transitions to its second phase ($\text{Clk} = 1$), the preamplifier enters its active amplification mode. The PMOS precharge devices are turned OFF, and the nodes V_{op} and V_{on} begin to discharge from V_{dd} toward ground through the NMOS input transistors $M1c$ and $M2c$. The discharge rates of these nodes depend on the input voltages V_{ip} and V_{in} , such that a differential voltage is gradually developed between V_{op} and V_{on} . This voltage difference, although initially small, is crucial because it serves as the input to the latch stage. The preamplifier thus converts the input voltage difference into a time or voltage difference at its output nodes. The gain of the preamplifier stage can be approximated as [128]

$$A_v(\text{Preamp}) = \frac{\Delta V_o}{\Delta V_i} \approx \frac{g_{m1,c,2,c} \cdot (V_{dd} - V_{oen})}{I_{cm}} \quad (2.7)$$

where $g_{m1,c,2,c}$ is the transconductance of transistor $M1c$ or $M2c$, $V_{oen} = |V_{op} - V_{on}|$, is the output level to enable cross coupled latch and I_{cm} is the common mode current drawn from the capacitances if placed on nodes P and Q. This expression indicates that the gain is directly proportional to the transconductance and available voltage headroom, and inversely proportional to the common-mode current.

The latch stage, which follows the preamplifier, operates based on strong positive feedback. Once a sufficient differential voltage is developed at V_{op} and V_{on} , the cross-coupled transistors in the latch are triggered, initiating regeneration. One output node is rapidly driven toward V_{dd} while the other is pulled toward ground, resulting in a full logic-level output. An important advantage of this two-stage architecture is that the preamplifier isolates the input from the latch, thereby significantly reducing kickback noise caused by rapid switching in the regenerative stage [155, 156]. This isolation improves accuracy and allows operation over a wide input common-mode range, which is particularly beneficial in high-speed ADC applications.

However, despite these advantages, the presence of a static latch introduces certain limitations. Since the latch continuously consumes current, it leads to increased static power consumption, which is undesirable for low-power applications such as IoT systems [158]. Moreover, the speed of the comparator is constrained by the gain and bandwidth of the preamplifier, as well as the delay associated with initiating regeneration in the latch. The requirement of sufficient preamplifier gain to overcome latch offset further increases power consumption and limits scalability at low supply voltages. Consequently, while the conventional comparator provides good noise isolation and robustness, its speed–power trade-off motivates the use of dynamic latch-based architectures in modern low-power and high-speed designs [168].

The physical implementation of the conventional comparator was carried out using Cadence Virtuoso on 180 nm technology and the corresponding layout is shown in the Fig. 2.12 with area of 168 mm^2 . The layout design ensures symmetry between differential paths to minimize mismatch and offset, with careful placement of transistors and routing to balance parasitic capacitances at critical nodes. Proper common-centroid techniques and matching strategies are typically employed to reduce systematic variations, which is essential for maintaining comparator accuracy in high-speed applications.

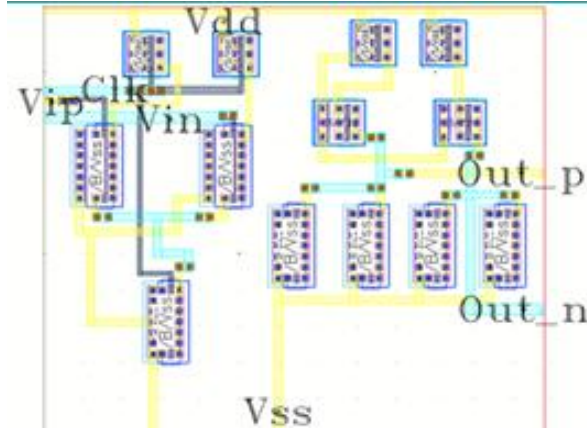


Fig. 2.12 Layout of conventional comparator

The transient analysis of the conventional comparator, as depicted in Fig. 2.13, illustrates the dynamic switching behavior of the circuit across the pre-charge and evaluation phases, highlighting the evolution of internal node voltages and output transitions. During the pre-charge phase, both output nodes are initialized to a known state, ensuring symmetric starting conditions. As the clock transitions to the evaluation phase, a small differential input voltage causes unequal discharge rates at the preamplifier output nodes, which is subsequently amplified by the latch stage through regenerative feedback. The transient waveform clearly demonstrates how a small input difference is translated into a full-swing digital output, with one node transitioning toward V_{dd} and the other toward ground. Based on the simulation results, the conventional comparator exhibits a delay of approximately 353 ps and a power consumption of 135 μW , indicating a moderate-speed operation with relatively higher power dissipation due to the presence of static current paths and the requirement of sufficient preamplifier gain.

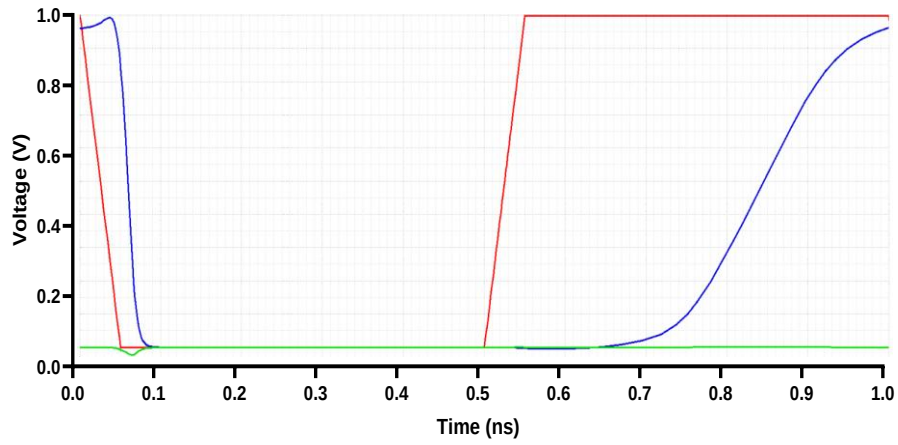
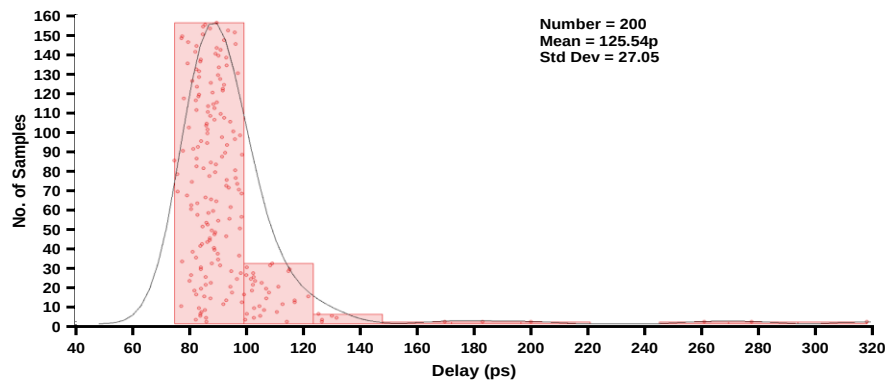
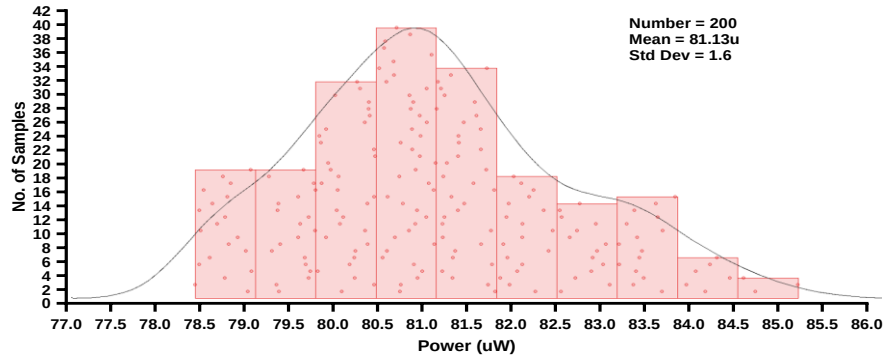


Fig. 2.13 Transient analysis of Conventional comparator

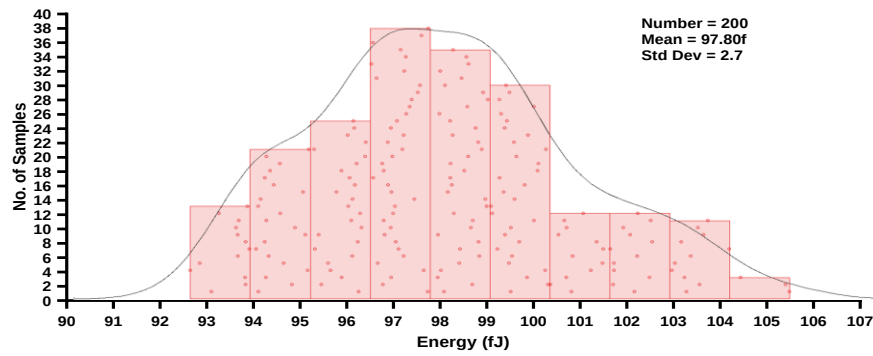
To further evaluate the robustness of the design, Monte Carlo simulations (shown in Fig. 2.14) were performed with 200 samples to analyze the statistical variations in delay, power, and energy consumption.



(a)



(b)



(c)

Fig. 2.14 Monte-Carlo simulations for (a) delay, (b) power and (c) energy for Conventional Comparator

The results exhibit a random distribution of these performance parameters due to process variations such as threshold voltage fluctuations, mobility variations, and mismatch in device dimensions. The spread in delay and power reflects the sensitivity of the comparator to device-level non-idealities, while the energy distribution provides insight into overall efficiency under variability. Such statistical analysis is crucial in assessing the reliability and yield of the design, particularly for large-scale integration in ADC systems, where consistent performance across process corners is required. Overall, the results indicate that while the conventional comparator demonstrates functional correctness, its

variability and relatively higher delay and power consumption motivate the need for more optimized dynamic comparator architectures.

2.10 Summary of Techniques and Design Trade-offs

The advanced mixed-signal circuit techniques discussed in this chapter collectively address the fundamental challenges associated with low-voltage operation, high-speed conversion, and energy-efficient design in modern SAR ADC architectures. Each technique targets a specific bottleneck within the signal chain, including device-level limitations, comparator regeneration delay, DAC switching energy, and control logic inefficiencies. However, these improvements are inherently interdependent, and the adoption of any particular technique introduces trade-offs in terms of power consumption, speed, silicon area, and design complexity. Therefore, a system-level perspective is essential to evaluate how these techniques interact and to determine an optimal design strategy.

At the device level, techniques such as self-cascode and DTMOS aim to enhance transistor performance under constrained supply voltages. The self-cascode structure effectively increases output resistance by redistributing the drain-source voltage across two series-connected devices, thereby reducing channel-length modulation and improving intrinsic gain. This is particularly advantageous in analog front-end circuits where gain enhancement is critical. However, the presence of an internal node introduces additional parasitic capacitance, which can limit bandwidth and slow down transient response. In contrast, the DTMOS technique dynamically modulates the threshold voltage by tying the gate and body terminals, resulting in increased transconductance and improved current drive at low supply voltages. While this enables operation in sub-1V regimes, its applicability is constrained by the forward-biasing of the body-source junction, which can introduce leakage currents and reliability concerns in bulk CMOS processes.

At the circuit level, comparator performance is primarily dictated by the efficiency of the regenerative latch. The cross-coupled regenerative latch structure provides exponential amplification of small differential inputs through positive feedback, making it a key component in high-speed comparators. Enhancements such as the shared-charge reset technique and auxiliary inverter-based technique focus on improving the initial conditions and effective transconductance of the latch, respectively. The shared-charge reset technique reduces delay by preconditioning output nodes to an intermediate voltage level, thereby minimizing the time required to enter the regeneration phase. This also reduces dynamic power consumption by avoiding full voltage swings during reset. However, its performance is sensitive to capacitor matching and charge redistribution accuracy. The auxiliary inverter technique, on the other hand, introduces additional dynamic current paths that boost the effective transconductance during regeneration, leading to faster decision-making. This improvement comes at the cost of increased parasitic loading and potential design complexity in ensuring stable operation across process variations.

In the DAC domain, the conventional binary-weighted capacitor array provides a straightforward implementation of charge redistribution but suffers from exponential growth in capacitance with increasing resolution, leading to larger area, higher switching energy, and slower settling. To mitigate these issues, several optimized switching techniques have been developed. The monotonic switching technique reduces energy consumption by ensuring unidirectional switching of capacitors, thereby eliminating redundant charge/discharge cycles. The Vcm-based switching technique further improves energy efficiency by maintaining the DAC output around a constant common-mode voltage, significantly reducing voltage swings and improving comparator stability. However, it requires precise generation of the common-mode reference and introduces additional control complexity. The split capacitor technique addresses the scalability issue by dividing the DAC into MSB and LSB sub-arrays connected through an attenuation capacitor, thereby reducing total capacitance and area. While effective, this approach is highly sensitive to parasitic capacitances at the bridge node, which can degrade linearity and necessitate calibration.

From a digital control perspective, SAR logic plays a crucial role in determining conversion speed and energy efficiency. Conventional sequential logic provides a simple and deterministic implementation but is limited by clock dependency, resulting in fixed conversion time and increased dynamic power due to continuous clock switching. The binary search algorithm ensures efficient convergence to the input signal value in N steps for an N -bit ADC, forming the core operational principle of SAR conversion. Asynchronous control techniques enhance performance by eliminating the global clock and allowing each bit decision to occur immediately after the previous one, thereby reducing average conversion time and power consumption. However, asynchronous designs introduce challenges related to timing synchronization, metastability, and increased circuit complexity.

2.10.1 Performance Trade-offs (Power, Speed, Area, Complexity)

The optimization of mixed-signal circuits requires careful balancing of multiple performance parameters, each of which is influenced by the chosen design techniques. Power consumption is predominantly determined by switching activity in the DAC and dynamic operation of the comparator and control logic. Techniques such as monotonic and V_{cm} -based switching significantly reduce switching energy by minimizing voltage transitions, while asynchronous control further reduces power by eliminating unnecessary clock toggling. However, these techniques may increase design overhead and require additional circuitry for control and reference generation.

Speed is largely governed by comparator regeneration time, DAC settling time, and control logic delay. Techniques that enhance the initial differential voltage or effective transconductance of the latch, such as shared-charge reset and auxiliary inverter methods, directly reduce comparator delay. Asynchronous SAR logic further improves speed by removing the constraint of fixed clock cycles. Nevertheless, increasing speed often requires higher bias currents or more complex circuit structures, which can negatively impact power efficiency.

Area is primarily dominated by the capacitive DAC and layout considerations. The conventional binary-weighted DAC suffers from large area due to exponential capacitor scaling, whereas the split capacitor technique significantly reduces area by partitioning the array. However, reduced capacitance increases sensitivity to mismatch and parasitic effects, requiring more sophisticated layout techniques and, in some cases, calibration circuitry.

Complexity increases with the adoption of advanced techniques. While conventional architectures are relatively simple and robust, techniques such as asynchronous control, auxiliary inverter enhancement, and V_{cm} -based switching introduce additional design challenges, including precise timing control and sensitivity to process variations. Thus, achieving optimal performance requires a careful trade-off between simplicity and functionality.

2.10.2 Key Observations from Existing Techniques

The comprehensive review of existing mixed-signal circuit techniques reveals that the performance of SAR ADCs is strongly dependent on the optimization of three major building blocks: the comparator, capacitive DAC and SAR logic. From the study of comparator architectures, it is observed that conventional dynamic comparators suffer from reduced gain, increased delay and degraded robustness under low-voltage operation. Techniques such as self-cascode structures improve voltage gain by increasing effective output resistance, thereby accelerating differential signal development and reducing comparator delay. Similarly, DTMOS-based approaches enhance transconductance through dynamic threshold modulation, making them highly suitable for ultra-low-voltage applications. However, DTMOS techniques may require careful body-bias management to avoid latch-up and excessive leakage in scaled technologies.

The analysis of regenerative latch architectures indicates that the regeneration speed of a comparator is highly influenced by the effective transconductance and initialization

conditions of the latch. Conventional cross-coupled latches provide strong positive feedback but often consume higher switching energy due to full rail-to-rail charging and discharging. The shared-charge reset technique reduces unnecessary voltage swings during reset by equalizing output node voltages prior to regeneration, thereby lowering delay and power consumption. Likewise, the auxiliary inverter technique enhances the regenerative strength of the latch by providing additional current drive, resulting in faster latch operation without introducing significant capacitive loading.

The study of capacitive DAC techniques demonstrates that conventional binary-weighted capacitor arrays become inefficient at higher resolutions due to exponentially increasing capacitance, leading to larger silicon area, higher switching energy, and increased sensitivity to mismatch and parasitic capacitances. To overcome these limitations, monotonic switching techniques reduce switching activity by ensuring unidirectional capacitor transitions during conversion. Similarly, Vcm-based switching schemes minimize voltage swing across capacitors by introducing a common-mode reference voltage, thereby achieving substantial energy savings and improved common-mode stability. Furthermore, split-capacitor architectures effectively reduce total capacitance and DAC area while maintaining binary-weighted functionality through capacitive attenuation.

The review of SAR logic and control techniques indicates that conventional synchronous sequential logic suffers from clock distribution overhead and increased power consumption at higher sampling rates. Binary search algorithms provide efficient successive approximation conversion; however, overall conversion speed remains limited by global clock dependency. In contrast, asynchronous SAR control techniques eliminate unnecessary clock cycles by enabling event-driven operation, thereby reducing power consumption and improving conversion speed.

Overall, the literature survey reveals that significant improvements in ADC performance can be achieved through the combined optimization of comparator gain, latch regeneration

dynamics, DAC switching energy and SAR control logic. However, existing techniques often optimize only one performance parameter at the expense of others, leading to trade-offs among speed, power consumption, area, complexity and robustness. These observations highlight the need for integrated design methodologies capable of simultaneously improving energy efficiency, speed, and low-voltage operation, which forms the primary motivation for the proposed work presented in subsequent chapters.

Chapter 3

Key Innovations in Comparator Architecture

This chapter presents a detailed investigation of several innovative comparator architectures developed to enhance the overall performance of SAR ADC systems. The proposed designs incorporate advanced circuit-level techniques including self-cascode structures, shared-charge reset mechanisms, auxiliary inverter-assisted regeneration and DTMOS-based operation. Each technique is introduced with the objective of improving specific performance parameters such as comparison speed, regenerative gain, power efficiency, and reliable low-voltage operation. Self-cascode configurations are explored to enhance effective output resistance and strengthen regeneration without increasing power overhead. Shared-charge techniques are employed to reduce internal node transition delay and improve comparison efficiency, while auxiliary inverter structures accelerate regenerative action and reduce decision latency. Furthermore, DTMOS-based architectures dynamically adjust transistor threshold voltage during operation to improve current driving capability and enable efficient operation under reduced supply voltages.

3.1 Design Motivation and Performance Metrics

The design of high-performance comparators is a critical aspect in the development of energy-efficient and high-speed mixed-signal systems, particularly in SAR ADCs. The comparator serves as the decision-making element that determines each bit during the conversion process, and its performance precisely impacts the entire speed, power consumption, resolution and accuracy of the ADC. A key challenge in comparator design is achieving an optimal trade-off among delay, power consumption, energy efficiency, and accuracy. The total delay of a comparator is primarily composed of two components: the preamplifier delay, which governs the rate of development of the input differential voltage, and the latch regeneration delay [120], which determines how quickly the comparator output resolves to a full digital level. In conventional designs, the preamplifier stage often

suffers from limited gain due to low output resistance and limited transconductance. Similarly, the latch stage, while capable of strong positive feedback, may exhibit increased regeneration delay if the initial differential input is insufficient, leading to metastability and degraded speed performance.

Power consumption is another critical design constraint, especially in battery-operated and IoT-based systems [93]. In comparator circuits, power is consumed through both static and dynamic components, where static power arises from bias currents in preamplifier stages and dynamic power is due to charging and discharging of internal capacitances during switching. Therefore, achieving low power consumption while maintaining high speed and accuracy requires careful optimization of both preamplifier and latch stages. Energy efficiency, often quantified in terms of energy per comparison, is closely related to both delay and power consumption. Reducing delay without increasing power, or reducing power without significantly affecting delay, leads to improved energy efficiency. Additionally, robust design methodologies must also ensure stable operation across process corners and temperature variations while maintaining low standard deviation in performance metrics.

To address aforementioned challenges, this chapter brings forward six new comparator architectures (PC1–PC6) based on progressive design innovations. With an aim of increasing gain, a self cascode structure is introduced in preamplifier stage of PC1 – PC4 while remaining two architectures bring in DTMOS in preamplifier stage. Further, to speed up latch regeneration shared-charge logic and auxiliary inverter-based approaches are used and overall energy efficiency is improved through dynamic operation and reduced switching activity. By systematically exploring these techniques, the proposed comparator architectures aim to achieve an improved balance among speed, power, and accuracy, making them suitable for next-generation low-voltage, high-speed SAR ADC applications.

3.2 Self-Cascode Based Comparator Architectures (PC1 and PC2)

This section shows the design, its implementation and performance evaluation of the two proposed comparator architectures, namely Proposed Comparator 1 (PC1) and Proposed Comparator 2 (PC2), developed to enhance the speed and energy efficiency of conventional comparator topologies for low-voltage SAR ADC applications. The motivation behind these designs' stems from the limited preamplifier gain, higher delay, and suboptimal power efficiency of conventional two-stage comparators under scaled supply voltages. To overcome these issues, both proposed comparators employ a self-cascode structure in place of the traditional differential pair, thereby increasing the effective output resistance and transconductance of the input stage to achieve higher gain and faster differential voltage development. While PC1 combines this enhanced preamplifier with a static latch to maintain robust regeneration and structural simplicity, PC2 further improves energy efficiency by integrating a dynamic latch, which eliminates static current paths and enables faster regenerative action through clock-controlled operation. Detailed analytical modeling of the proposed architectures is carried out by deriving the delay contributions of both preamplifier and latch stages, thereby establishing the relationship between circuit parameters, parasitic capacitances, and overall comparator speed.

3.2.1 Circuit Design and Operation

The proposed methodology focuses on improving comparator performance by modifying the preamplifier stage of a conventional two-stage comparator. The circuit schematics of Proposed Comparator 1 (PC1) and Proposed Comparator 2 (PC2) are placed as Fig. 3.1 and Fig. 3.2 respectively. PC1 and PC2 use proposed self-cascode based preamplifier wherein differential pair is formed by self-cascode structure ((M1s, M3s), ((M2s, M4s)). The PC1 and PC2 differ in the latch configurations. The former uses static latch while the latter relies on dynamic latch.

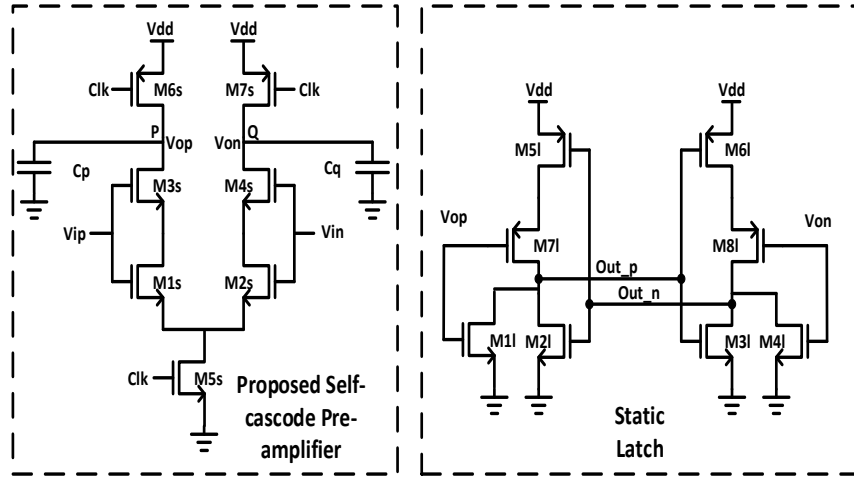


Fig. 3.1 Proposed comparator 1 (PC1) using self cascode preamplifier with static latch

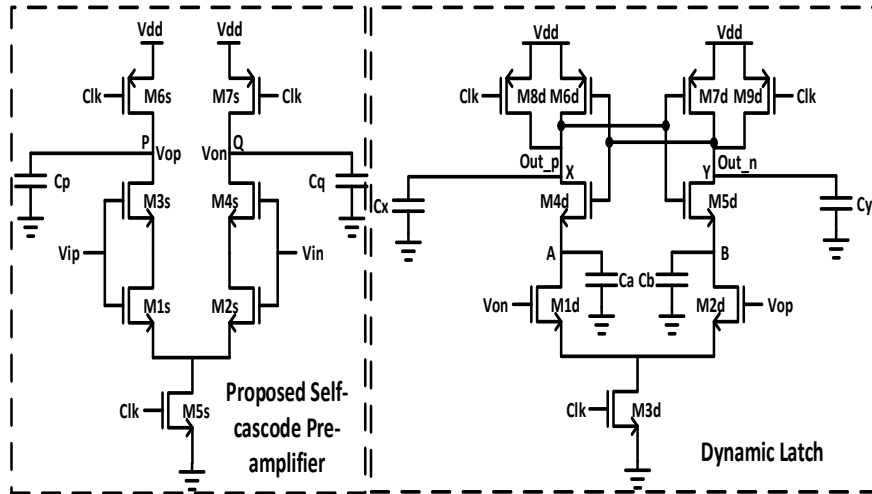


Fig. 3.2 Proposed comparator 2 (PC2) using self cascode preamplifier with dynamic latch

The preamplifier in both PC1 and PC2 is dynamic in nature, and works in sampling ($\text{Clk}=0$) and evaluation phases ($\text{Clk}=1$). For $\text{Clk}=0$, both transistors M6s and M7s are turned on and charge capacitors at nodes P and Q (C_p and C_q) to Vdd. Subsequently when $\text{Clk}=1$, C_p and C_q are discharged from Vdd to ground at different instants proportional to input voltage Vip and Vin. Therefore, an input dependent differential voltage is created

between V_{op} and V_{on} , which drive the latch stage for final output. The gain of the preamplifier stage can be expressed as follows,

$$A_v(Preamp) = \frac{\Delta V_o}{\Delta V_i} \approx \frac{g_{m1s_3s_2s_4s} \cdot (V_{dd} - V_{oen})}{I_{cm}} \quad (3.1)$$

where $g_{m1s_3s_2s_4s}$ represent equivalent trans-conductances of transistor (M1s, M3s) or (M2s, M4s), V_{oen} is the output level to enable cross coupled latch and I_{cm} is the current in common mode configuration pulled out from the differential pair transistors. It is to be emphasized here that the gain of self cascode stage used in proposed comparator is much higher than simple differential pair used in preamplifier of conventional comparator [19].

The PC1 employs static latch comprising of differential input pair (M1l-M4l) and cross-coupled transistor pairs (M2l-M3l and M7l-M8l) that stores and maintains its output state using continuous feedback, typically implemented with cross-coupled inverters. It does not rely on clocked pre-charge or evaluation phases and can hold its state indefinitely as long as power is supplied. Static latches offer good noise immunity and stable operation but generally consume higher static power due to continuous current flow.

The PC2 used dynamic latch which is formed by differential pair M1d-M2d, two cross coupled pairs, M4d-M5d and M6d-M7d and two pre-charge switches M8d-M9d. During first phase ($Clk=0$), transistors M6s and M7s are turned on and charge the capacitors at nodes P and Q (C_p and C_q) to V_{dd} . Also, PMOS transistors M8d and M9d of dynamic latch are turned on charging capacitors C_x and C_y at nodes X and Y respectively to V_{dd} , which turns on NMOS transistors M4d and M5d. In addition, the outputs enabled in self cascode preamplifier turns both NMOS transistors M1d and M2d of dynamic latch. Sequentially, PMOS transistors M7d, M8d and NMOS transistor M3d are off.

During evaluation phase ($Clk = 1$), V_{op} and V_{on} node capacitance of self cascode preamplifier discharges from V_{dd} to ground in a different time rate proportional to the magnitude of each input voltage V_{ip} and V_{in} . Therefore, an input dependent differential voltage is formed between output terminals, operating the transistors of dynamic latch

such that to regenerate one of the output node of latch to logic high while other remains at logic low.

Delay analysis

The delay analysis of the proposed comparators is carried out by decomposing it into two fundamental components, namely the preamplifier delay (t_{pre}) and the latch regeneration delay.

Preamplifier delay

As PC1 and PC2 use same preamplifier stage, the delay calculations remain same for both comparators. In pre-charge phase, the tail transistor M5s remains off and the PMOS transistors M6s-M7s connected to the supply are turned on, charging the intermediate nodes P and Q to V_{dd} . This ensures proper initialization of the circuit with equal node voltages. In pre-charge phase, the circuit schematic of preamplifier may be viewed as Fig. 3.3(a). When the clock transitions to the second phase ($Clk = 1$), the pre-charge transistors are switched off and the current path through the self-cascode differential pair is activated. The circuit schematic of preamplifier in evaluate phase may be viewed as Fig. 3.3(b). Consequently, the capacitances at nodes P (C_p) and Q (C_q), respectively begin to discharge at rates determined by the voltages V_{ip} and V_{in} , leading to the development of a differential voltage between the two nodes. The KCL at nodes P and Q may be written as

$$-C_p \frac{d(V_{dd} - V_{op})}{dt} = g_{m_{1s3s}}(V_{ip}) \quad (3.2)$$

$$-C_q \frac{d(V_{dd} - V_{on})}{dt} = g_{m_{2s4s}}(V_{in}) \quad (3.3)$$

where $g_{m_{1s3s}}$ and $g_{m_{2s4s}}$ are the equivalent transconductances of M1s, M3s and M2s, M4s respectively.

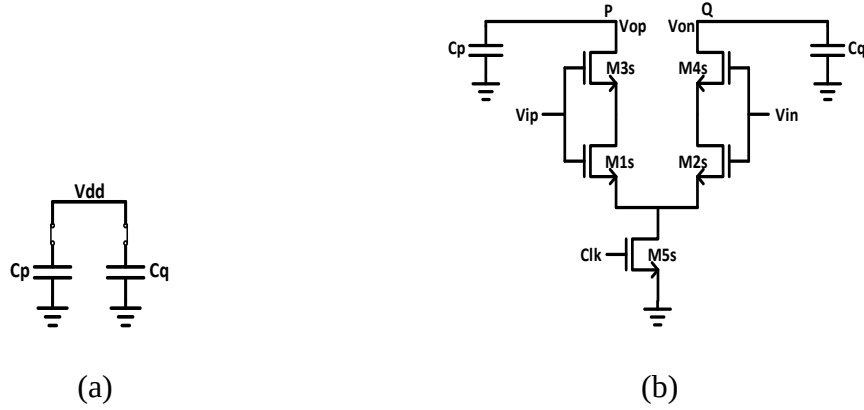


Fig. 3.3 Preamplifier operation phases: (a) precharge, (b) amplification

Integrating and combining (3.2) and (3.3), we get

$$C_{pq} \frac{(V_{op} - V_{on})}{t_{pre}} = g_{m_{eq_s}} (V_{ip} - V_{in}) \quad (3.4)$$

where $C_{pq} = C_p = C_q$, and t_{pre} is the decision time of preamplifier. Equation (3.4) gives correlation between the differential output voltage and input voltage difference. It is clear that the output voltage grows proportionally with time and is directly influenced by the equivalent transconductance and load capacitance.

Since the tail current is constant, therefore,

$$|V_{op} - V_{on}| \approx \left\{ \frac{g_{m_{eq_s}} (|V_{ip} - V_{in}|)}{C_{pq}} \right\} * t_{pre} \quad (3.5)$$

where $g_{m_{eq_s}}$ denotes the equivalent transconductance of M1s-M4s. This analysis highlights that the enhanced transconductance provided by the self-cascode structure accelerates the discharge process, thereby reducing the preamplifier decision time. As a result, the first stage produces a sufficiently large differential signal more rapidly, which subsequently reduces the regeneration time required by the latch stage and contributes to the overall reduction in comparator delay.

Latch delay

The second stage of PC1 is realized using a static latch configuration, implemented through two cross-coupled NOR gates, following the methodology reported in prior work. This latch structure provides regenerative feedback by interconnecting the outputs of each NOR gate to the input of the other, while the second input of each gate serves as the enabling signal for triggering the decision process. Specifically, transistors M1l,M2l,M5l ,M7l constitute the first NOR gate (NOR1), whereas transistors M3l,M4l,M6l,M8l form the second NOR gate (NOR2). The latch produces two complementary outputs, Out_p and Out_n, which represent the final digital decision of the comparator. During operation, once a sufficient differential voltage is developed at the preamplifier output, it is applied to inputs of the latch. The cross-coupled structure ensures that even a small input difference is rapidly amplified through positive feedback, forcing one output node to transition to logic high while the other is driven to logic low. The switching behavior of the latch can be analyzed using transient response, where propagation delay corresponds to the time required for the outputs to transition between logic states following an input event. The total parasitic capacitance at output nodes Out_n and Out_p can be viewed as lumped capacitances at these nodes and may written as [48]:

$$[C_{out_n} = C_{gb,M2l} + C_{gb,M5l} + C_{db,M3l} + C_{db,M4l} + C_{db,M8l} + C_{sb,M8l} + C_{db,M7l}] \quad (3.6)$$

$$[C_{out_p} = C_{gb,M3l} + C_{gb,M8l} + C_{db,M1l} + C_{db,M2l} + C_{db,M5l} + C_{sb,M5l} + C_{db,M6l}] \quad (3.7)$$

where C_{gb} , C_{db} and C_{sb} corresponds to gate to bulk, drain to bulk and source to bulk capacitances of respective transistors.

In this context, the delay of the static latch is strongly influenced by the parasitic capacitances present at the output nodes. These capacitances, which arise from gate-to-bulk, drain-to-bulk and source-to-bulk junctions of the constituent transistors, can be collectively modeled as lumped capacitances at nodes Out_p and Out_n. The charging and discharging of these effective capacitances determine the speed of voltage transition at the

output nodes and hence directly impact the propagation delay of the latch. Therefore, accurate estimation of these parasitic components is essential for precise delay modeling and overall performance evaluation of the comparator.

Assuming the static latch is initially reset and its inputs are applied as $V_{op} = 1$ and $V_{on} = 0$, therefore, the lowest to highest and highest to lowest propagation delays (τ_{PLH_Latch} and τ_{PHL_Latch} linked with node Out_n are given respectively as:

$$\tau_{PLH_Latch} = \tau_{PLH_out_n} + \tau_{PHL_out_p} \quad (3.8a)$$

and

$$\tau_{PHL_Latch} = \tau_{PHL_out_n} + \tau_{PLH_out_p} \quad (3.8b)$$

Finally, the overall delay of PC1 can be expressed as:

$$t_{total_pc1} = t_{pre} + (\tau_{PLH_Latch} + \tau_{PHL_Latch})/2 \quad (3.9)$$

The PC2 uses dynamic latch and its delay may be formulated by writing KCL at nodes X and node Y of Fig. 3.2, which are given in (3.10) and (3.11) respectively.

$$C_x \frac{dV_{out_p}}{dt} = g_{m11_d} (V_{out_n} - V_{on} - V_t) \quad (3.10)$$

$$C_y \frac{dV_{out_n}}{dt} = g_{m12_d} (V_{out_p} - V_{op} - V_t) \quad (3.11)$$

where V_{out_p} and V_{out_n} correspond to voltages at node X and Y.

Combining equations (3.10) and (3.11), we get

$$C_{xy} \frac{d(V_{out_p} - V_{out_n})}{dt} = g_{m_{eq_d}} (V_{out_n} - V_{out_p} + V_{op} - V_{on}) \quad (3.12)$$

Also, writing summing currents at node A and B from Fig. 3.2:

$$-C_a \frac{dV_{on}}{dt} = +\Delta I + C_x \frac{dV_{out_p}}{dt} \quad (3.13)$$

$$-Cb \frac{dV_{op}}{dt} = -\Delta I + Cy \frac{dV_{out_n}}{dt} \quad (3.14)$$

Integrating the sides of (3.13) and (3.14) and merging the resulting equations gives:

$$Cxy \frac{d(V_{out_p} - V_{out_n})}{dt} + gm_{eq_d}(V_{out_p} - V_{out_n}) \left(1 - \frac{Cxy}{Cab}\right) = gm_{eq_d} \frac{2\Delta I.t}{Cab} \quad (3.15)$$

where gm_{eq_d} represents equivalent transconductance of transistors M4d and M5d, $Cxy = Cx = Cy$ is the identical capacitance at node X and Y, $Cab = Ca = Cb$ is the identical capacitance at node a and b. Equation (16) represents a differential equation and solving the same, the delay of the dynamic latch can be written as:

$$t_{latch_pc2} = \frac{0.69 * Cxy}{gm_{eq_d} \left(1 - \frac{Cxy}{Cab}\right)} \quad (3.16)$$

The delay expression of the dynamic latch clearly indicates the influence of internal node capacitances on the regeneration process. In particular, the presence of capacitances Ca and Cb introduces a degeneration effect, which effectively slows down the regeneration by increasing the time constant of the latch. Therefore, the degeneration caused by the capacitors Ca and Cb raises t_{latch_pc2} by a factor of $\left(1 - \frac{Cxy}{Cab}\right)$. As this ratio increases, the effective transconductance driving the regeneration is reduced, thereby increasing t_{latch} . Hence, the capacitive loading at intermediate nodes plays a crucial role in evaluating the speed of the dynamic latch and should be minimized during the design and layout. Finally, the overall delay of PC 2 can be expressed as:

$$t_{total_pc2} = t_{pre} + t_{latch} \quad (3.17)$$

This relation highlights that any improvement in the preamplifier gain or reduction in latch capacitances directly contributes to faster overall comparator operation. Meanwhile, the output voltages V_{out_p} and V_{out_n} of dynamic latch varies according to the values of V_{op} and V_{on} and finally brings one output back to V_{dd} while allowing other to fall to zero. This regenerative action ensures full-swing digital outputs and enables high-speed

decision making, thereby making the proposed comparator highly efficient for low-power and high-speed applications.

3.2.2 Performance Evaluation

The design of proposed comparator architectures is validated through extensive simulations carried out in a 180 nm CMOS technology using the Cadence Virtuoso design. Post-layout simulations are performed to evaluate key indicators such as gain, delay, power dissipation, energy efficiency and robustness under process variations. The results are also compared with the conventional comparator to establish the effectiveness of the proposed methodology.

The first level of analysis focuses on the preamplifier stage, where the impact of the self-cascode structure is assessed against the conventional differential pair. The gain of proposed self-cascode preamplifier stage is compared with the conventional design through AC analysis.

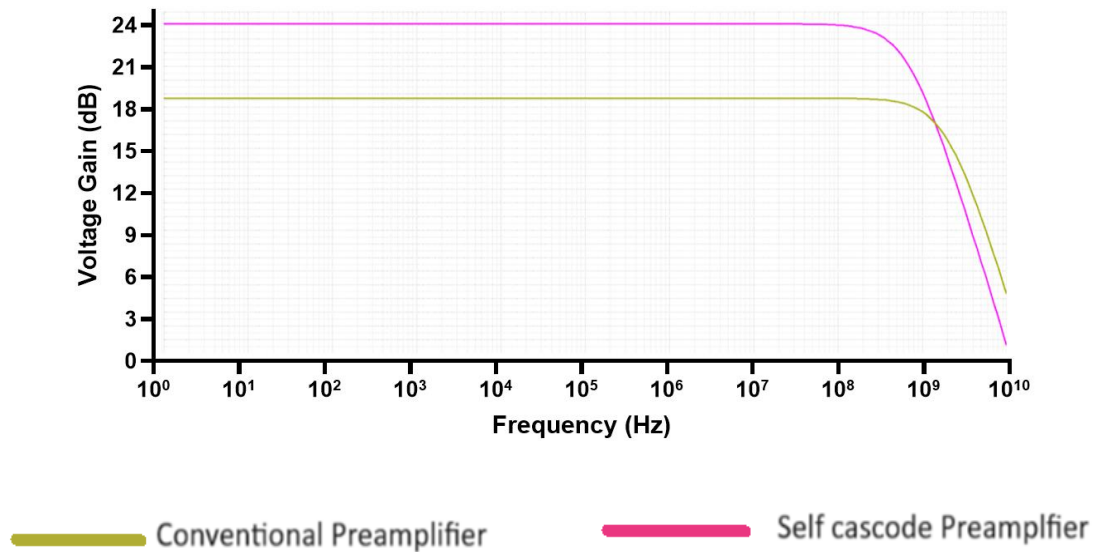


Fig. 3.4 Gain comparison of conventional preamplifier and proposed self cascode preamplifier

The AC response is depicted in Fig. 3.4 which indicates that the proposed self-cascode preamplifier exhibits a significantly higher gain across a wide frequency range compared to the conventional design. This improvement is attributed to the increased output resistance and enhanced transconductance of the self-cascode configuration. Further the delay and average power dissipation of the proposed self-cascode preamplifier is compared with the conventional design. The timing waveform for delay and average power consumption are shown in Fig. 3.5 and 3.6 respectively. It is found that the delay of self-cascode preamplifier is ~ 25 ps in contrast to ~ 72 ps for conventional preamplifier, clearly highlighting the improvement. Additionally, the average power consumption of the proposed self-cascode preamplifier consumes approximately $16 \mu\text{W}$, whereas the conventional preamplifier exhibits a higher power consumption of about $29 \mu\text{W}$. These results clearly demonstrate that the proposed preamplifier achieves both higher speed and lower power consumption, primarily due to faster development of the differential output voltage.

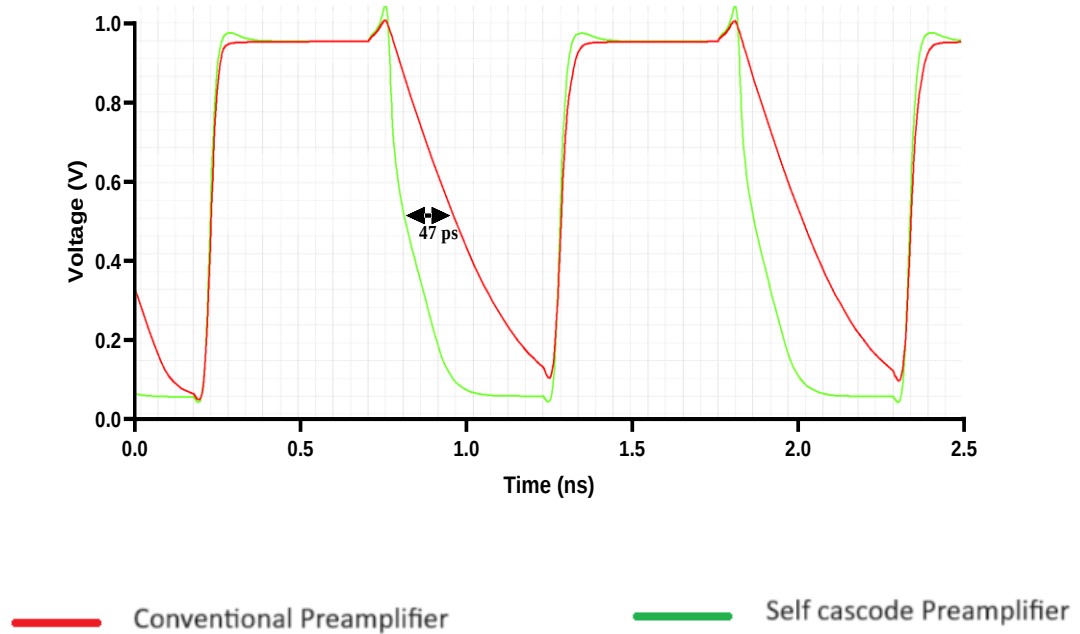


Fig. 3.5 Timing waveforms for self cascode and conventional preamplifiers

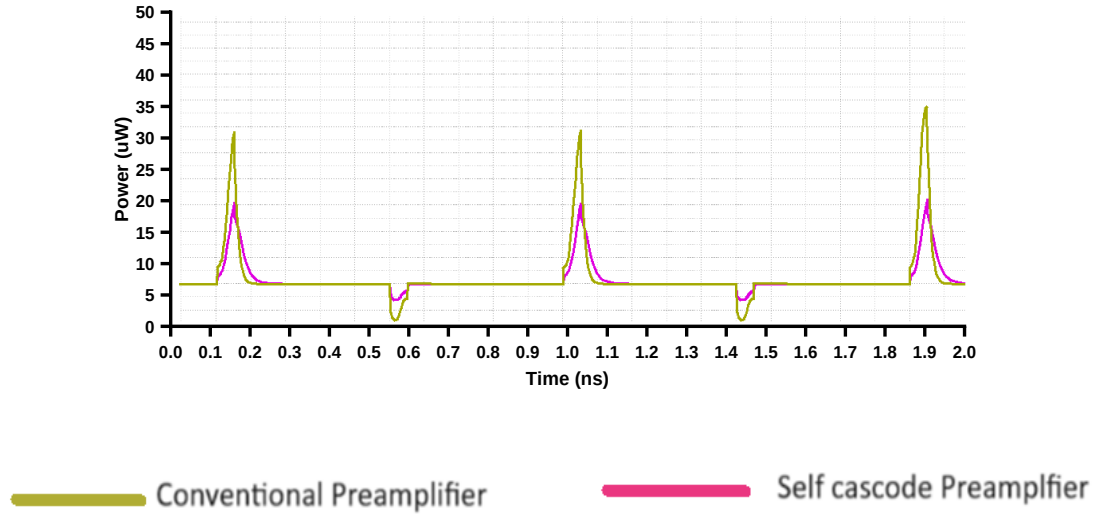


Fig. 3.6 Power consumption of proposed self cascode and conventional preamplifiers

The layouts of the proposed comparator architectures were implemented using Cadence Virtuoso, as illustrated in Fig. 3.7, to evaluate the practical silicon area and layout feasibility of the designs. The measured active areas indicate that Proposed Comparator 1 (PC1) occupies approximately $162 \mu\text{m}^2$, while Proposed Comparator 2 (PC2) requires a slightly smaller area of about $154 \mu\text{m}^2$.

Despite incorporating architectural enhancements such as the self-cascode preamplifier and optimized latch configurations, the layout results show a minimal increase in active area indicating that performance improvements are achieved without significant silicon area penalty. Notably, PC2 achieves a marginal reduction in area compared to PC1, primarily due to the use of a dynamic latch structure, which eliminates certain transistors associated with static biasing and simplifies the overall layout.

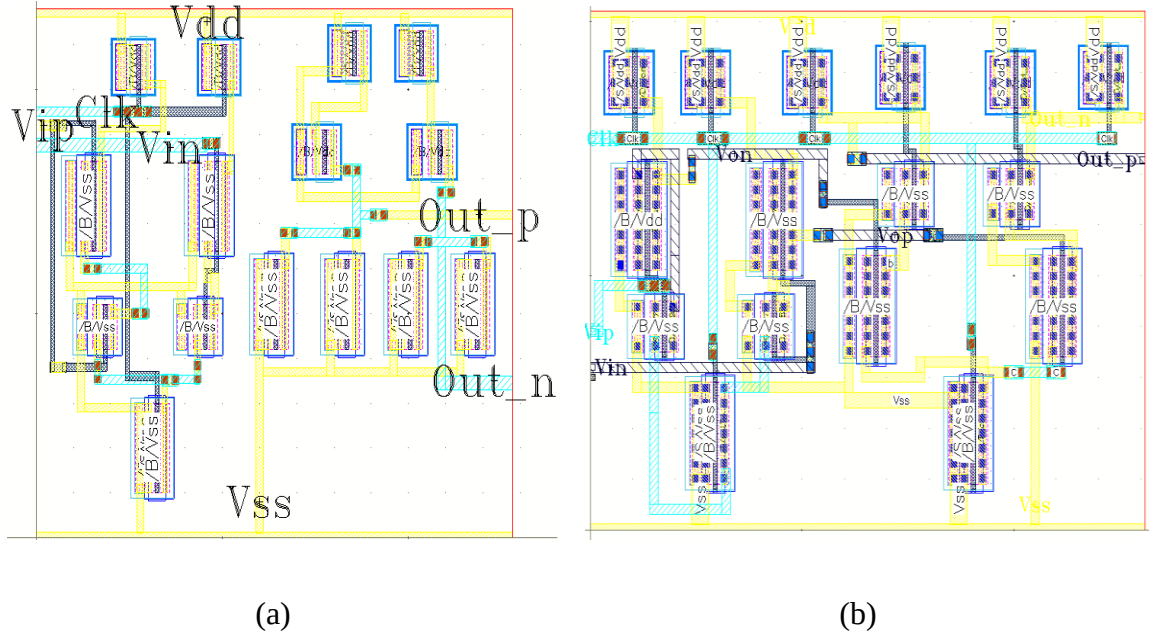
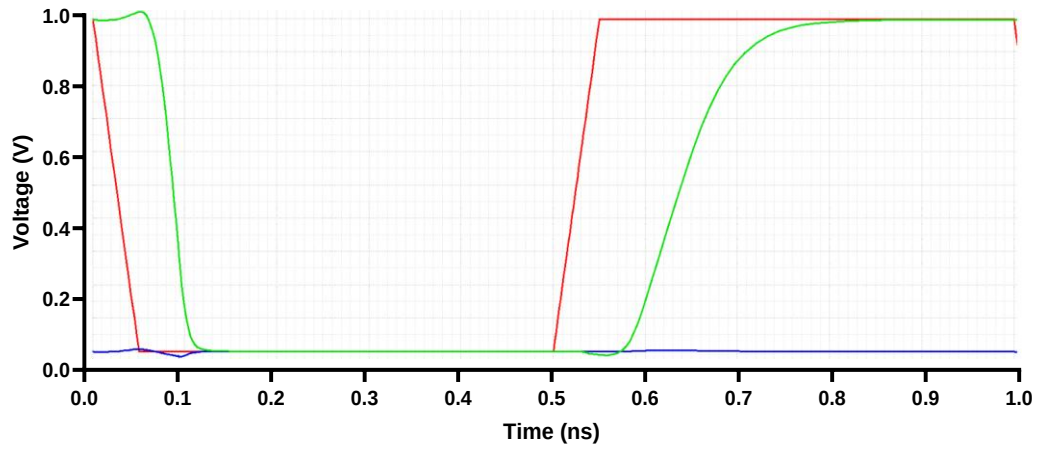


Fig. 3.7 Layout of (a) Proposed comparator 1 (PC1) (b) Proposed comparator 2 (PC2)

The complete proposed comparator structures were evaluated using transient simulations with a ramp input signal. One input is swept upto 1V while the other is held at a fixed reference voltage (500 mV). Post-layout simulation results provide a realistic evaluation of circuit evaluation in terms of delay, power and energy performance.



(a)

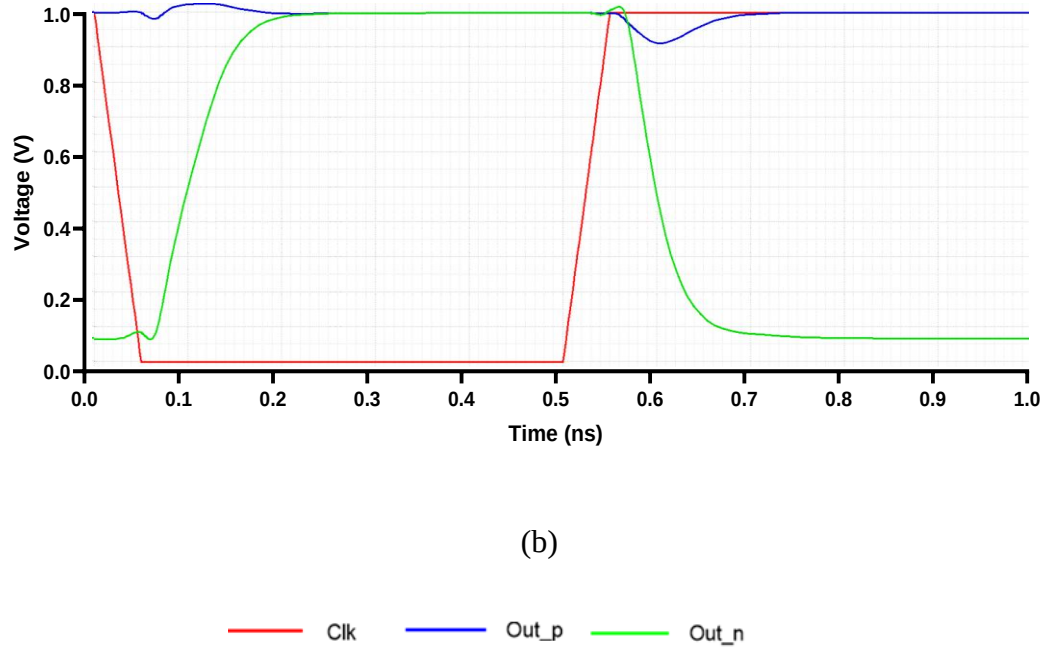
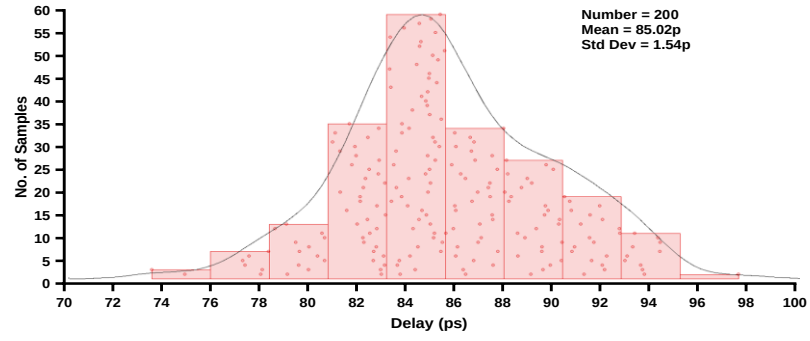
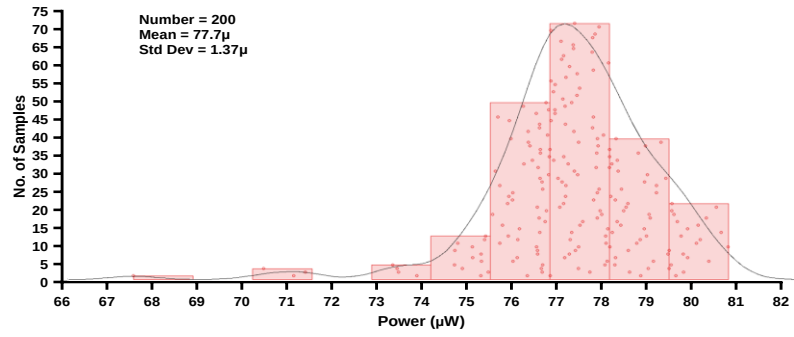


Fig. 3.8. Transient analysis of (a) Proposed comparator 1 (PC1) and (b) Proposed comparator 2 (PC2)

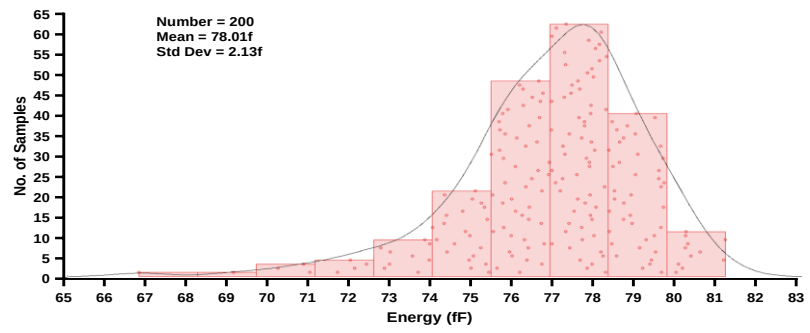
From the transient waveforms shown in Fig. 3.8 (a) and (b), analogues to Proposed Comparator 1 (PC1) and Proposed Comparator 2 (PC2), the key performance metrics are extracted and analyzed. PC1 exhibits a delay of approximately 304 ps, power consumption of 130 μW , and energy consumption of 116 fJ/conversion. In comparison, PC2 demonstrates improved performance with a reduced delay of 220 ps, lower power consumption of 110 μW , and energy consumption of 111 fJ/conversion. These results clearly indicate that PC1 achieves a significant improvement over the conventional comparator due to the enhanced gain provided by the self-cascode preamplifier, which accelerates the development of the differential input signal and reduces decision time. Furthermore, PC2 achieves additional performance gains by incorporating a dynamic latch structure, which eliminates static current paths and enhances regenerative action..



(a)

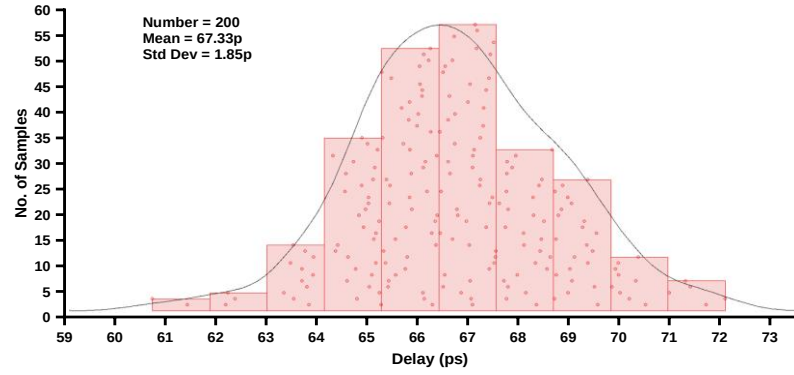


(b)

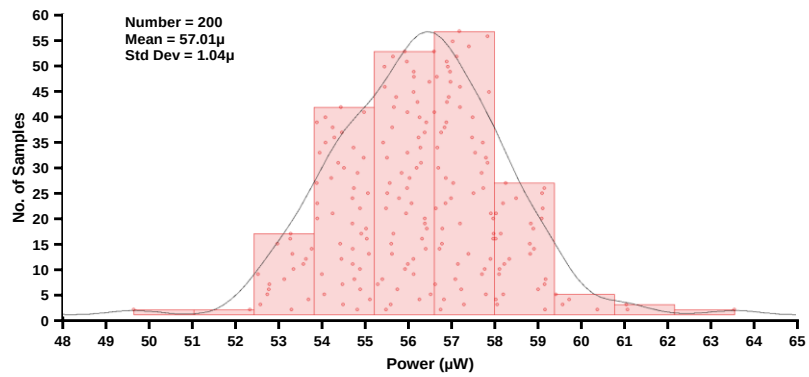


(c)

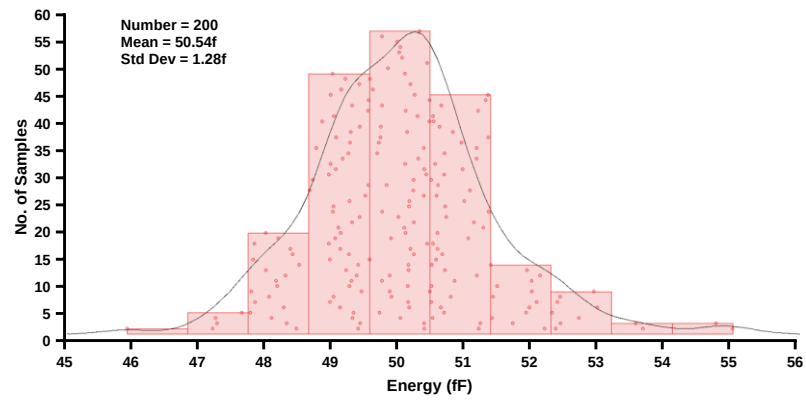
Fig. 3.9 Monte-Carlo simulation for (a) delay, (b) power and (c) energy for Proposed Comparator 1 (PC1)



(a)



(b)



(c)

Fig. 3.10 Monte-Carlo simulation for (a) delay, (b) power and (c) energy for Proposed Comparator 2 (PC2)

To evaluate the robustness of the proposed comparator architectures against process variations, Monte Carlo simulations with 200 samples are performed, as shown in Figs. 3.9 and 3.10 for PC1 and PC2, respectively. The statistical analysis reveals that both proposed comparators demonstrate lower mean delay and power consumption compared to the conventional design, indicating improved performance consistency. Additionally, the standard deviation of key parameters is reduced, which reflects enhanced stability and reduced sensitivity to device mismatch and process variations. For instance, the mean delay decreases significantly from approximately 353 ps in the conventional comparator to about 220 ps in Proposed Comparator 2, highlighting the effectiveness of the proposed design in achieving faster operation. Similarly, the energy consumption not only decreases but also exhibits lower variation, confirming improved reliability across different process conditions. These results validate that the proposed comparator architectures maintain consistent performance and are well-suited for practical fabrication scenarios where process variations are inevitable.

Table 3.1: Comparative Analysis of Proposed Comparators with recent works

Parameter Reference	Technology (nm)	Supply voltage (V)	Clock Frequency(GHz)	Power Consumption(uW)	Delay (ps)	Energy (fJ/conv)	Active Area (μm^2)
[27]	180	1.2	0.5	329	550	660	392
[41]	180	1.2	0.5	109	388	110	-
[45]	180	1.8	0.5	-	-	162	150
[103]	180	1.8	2	148	212	-	533
Conventional Comparator	180	1.2	0.5	135	353	132	168
Proposed Comparator 1 (PC1)	180	1.2	0.5	130	304	116	162
Proposed Comparator 2 (PC2)	180	1.2	0.5	110	220	111	154

The performance comparison presented in Table 3.1 provides a comprehensive evaluation of the proposed comparator architectures against recent reported works and the conventional comparator under similar operating conditions in 180 nm CMOS technology. It is observed that prior works exhibit relatively higher delay and energy consumption, with delays ranging from 388 ps to 550 ps and energy values as high as 660 fJ/conversion, indicating limitations in achieving an optimal balance between speed and energy efficiency. Although some designs report lower power, they often compromise in delay or operate at different supply voltages and frequencies, making them less suitable for balanced high-speed applications.

The conventional comparator, while maintaining moderate power consumption of 135 μ W, suffers from a relatively high delay of 353 ps and energy consumption of 132 fJ/conversion, which restricts its suitability in high-speed SAR ADC systems. In contrast, the proposed designs demonstrate clear and consistent improvements. Proposed Comparator 1 (PC1) reduces the delay to 304 ps while maintaining comparable power consumption (130 μ W) and achieving lower energy (116 fJ/conversion), validating the effectiveness of the self-cascode preamplifier in enhancing gain and accelerating decision-making. More notably, Proposed Comparator 2 (PC2) achieves the best overall performance, with a significant reduction in delay to 220 ps, along with lower power consumption (110 μ W) and energy (111 fJ/conversion). This improvement highlights the advantage of combining a high-gain self-cascode preamplifier with a dynamic latch, which enhances regeneration speed while eliminating static current paths. Additionally, the active area of the proposed comparators remains competitive, with PC2 occupying only 154 μm^2 , which is smaller than both the conventional comparator and several prior designs.

3.3 Shared-Charge Logic and Auxiliary Inverter Based Comparators (PC3 and PC4)

This section presents the design and comprehensive evaluation of Proposed Comparator 3 (PC3) and Proposed Comparator 4 (PC4), which are advanced dynamic comparator architectures developed to enhance the energy efficiency and speed of comparator operation beyond the previously proposed static and dynamic latch structures. Both comparator architectures employ the self-cascode preamplifier topology introduced in the earlier section to enhance front-end gain and accelerate differential voltage development; however, their key distinction lies in the latch-stage optimization. PC3 integrates a shared-charge logic dynamic latch, wherein a charge-sharing reset mechanism is introduced between the latch output nodes during the precharge phase to exploit residual charge from the previous cycle and initialize both outputs near an intermediate potential rather than full rail voltages. This reduces the voltage swing required during regeneration and consequently lowers both latch delay and dynamic energy consumption.

Building upon this concept, PC4 further augments the latch stage by incorporating auxiliary inverter pairs into the shared-charge logic dynamic latch structure. These auxiliary inverters increase the effective transconductance of the regenerative latch, thereby strengthening positive feedback and accelerating the charging/discharging of output nodes during the evaluation phase. Analytical delay modeling shows that the latch delay is inversely proportional to the effective latch transconductance, and therefore the auxiliary inverter-assisted topology of PC4 achieves substantially lower regeneration time than PC3 by increasing the overall regenerative drive strength.

Extensive post-layout simulations confirm the efficacy of the proposed architectures. PC3 achieves a delay of substantial improvement over conventional dynamic comparators due to the shared-charge logic mechanism. PC4 further improves the delay, owing to the enhanced regeneration provided by the auxiliary inverter pair. Monte Carlo analyses

confirm the robustness of both designs, indicating resilience against fabrication mismatches and environmental fluctuations. Although PC4 incurs slightly higher power and area overhead than PC3 due to the auxiliary inverter circuitry, it offers the best overall speed and FoM, setting it highly appropriate for ultra-high-speed ADC applications. Conversely, PC3 provides the lowest energy consumption and power dissipation, rendering it more attractive for ultra-low-power systems where energy efficiency is prioritized over absolute speed.

3.3.1 Circuit Design and Operation

The architecture of Proposed Comparator 3 (PC3) incorporates a self-cascode preamplifier followed by an optimized dynamic latch employing shared-charge reset logic, as illustrated in Fig. 3.11. The principal motivation behind this latch modification is to exploit residual charge stored at the output nodes during the previous comparison cycle, thereby reducing unnecessary full-swing charging/discharging and improving both delay and energy efficiency.

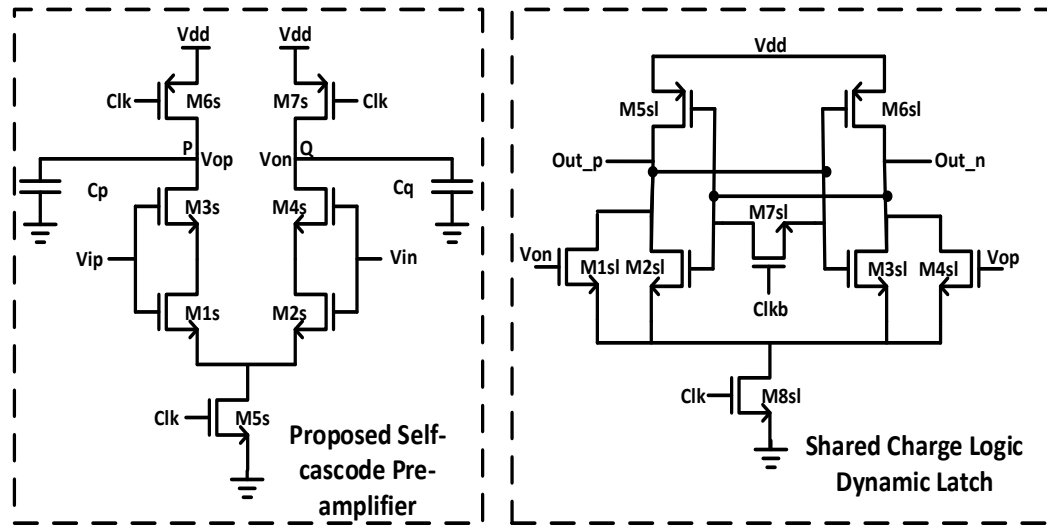


Fig.3.11 Proposed comparator 3 (PC3) using shared charged logic

In contrast to conventional latch implementations, the PMOS reset transistors used in earlier static latch structures are replaced with a single tail-controlled regenerative path to

reduce transistor count and increase the effective regeneration current. Furthermore, an NMOS pass transistor (M7sl) is inserted between the complementary latch output nodes to realize the shared-charge mechanism. This transistor becomes active during the reset/precharge phase and allows redistribution of charge between the two output nodes, such that the latch outputs equalize toward an intermediate voltage rather than being forced to opposite rail voltages. As a result, both output nodes begin the subsequent evaluation cycle from approximately half-supply potential, substantially reducing the voltage excursion required during regeneration.

During precharge phase, the tail transistors of both the preamplifier and latch remain turned off, thereby eliminating static current paths and ensuring zero static power dissipation. Simultaneously, the preamplifier output nodes V_{op} and V_{on} are charged to V_{dd} , which activates the intermediate latch transistors connected to these nodes. Under this condition, the shared-charge transistor between the latch outputs turns on and facilitates charge redistribution between Out_p and Out_n . Since one of the output nodes typically retains a high voltage while the other remains low from the preceding comparison cycle, this charge-sharing process equalizes the node voltages toward nearly $V_{dd}/2$. This intermediate initialization state significantly reduces the regeneration distance required in the subsequent comparison cycle and therefore lowers latch delay.

When the clock transitions to next phase ($Clk=1$), the tail transistors are activated, and the self-cascode preamplifier begins discharging V_{op} and V_{on} at rates determined by the differential input voltages V_{ip} and V_{in} . As the voltage difference between the preamplifier outputs develops, one of the latch input transistors gradually turns off when its gate to source voltage declines below threshold, thereby initiating the regenerative action of the latch. The cross-coupled inverter pairs provide strong positive feedback, rapidly amplifying the differential input and forcing one output node toward V_{dd} while discharging the complementary node to ground. Since the latch outputs commence regeneration from an initial voltage near mid-supply rather than rail-to-rail extremes, the required transition time is substantially reduced. This shared-charge assisted initialization improves both the

regeneration speed and switching energy of the latch compared to conventional dynamic latch structures. Consequently, PC3 achieves lower delay and reduced energy per conversion while maintaining robust dynamic operation, which is aptly suitable for low voltage, high speed comparator applications.

The delay of shared charge logic latch in PC3 is calculated using the methodology given in [40] and found as

$$t_{latch_pc3} = \frac{C_L}{g_{m_{eq_d1}}} \ln \frac{V_{dd}/2}{|V_{op} - V_{on}|} \quad (3.18)$$

where $g_{m_{eq_d1}} = g_{m_{M2sl-M3sl}} + g_{m_{M5sl-M6sl}} + g_{m_{M1sl-M4sl}}$ is the effective trans-conductance of shared charge logic dynamic latch and C_L corresponds to the load capacitance.

The architecture of Proposed Comparator 4 (PC4) extends the shared-charge dynamic latch concept of PC3 by incorporating auxiliary inverter pairs (M1ai, M9ai) and (M4ai, M10ai) into the latch stage to further accelerate regenerative action and reduce latch delay, as illustrated in Fig. 3.12.

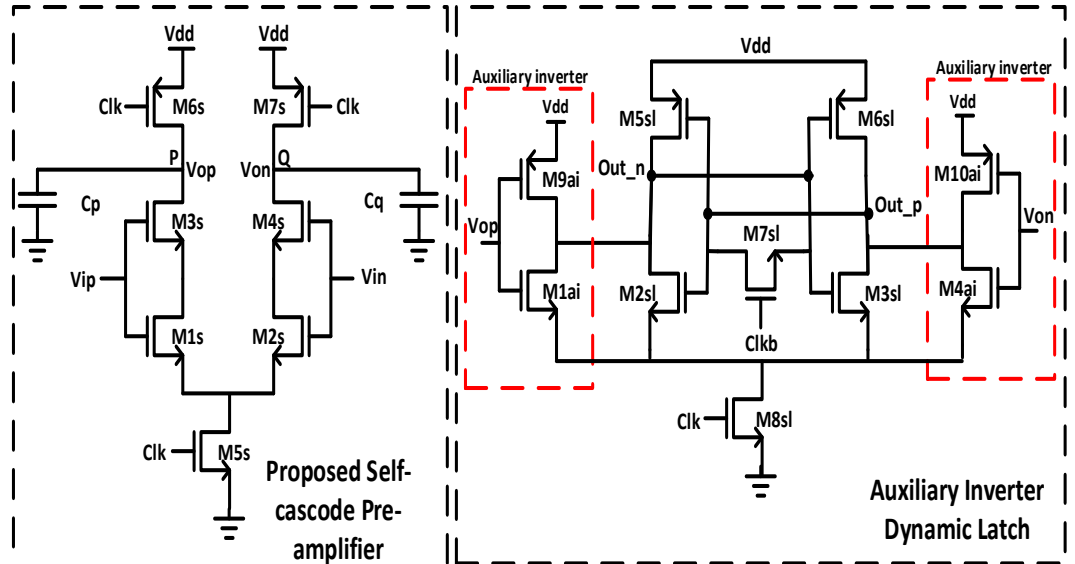


Fig.3.12 Proposed comparator 4 (PC4) using auxiliary inverter technique

The fundamental objective of this modification is to increase the effective transconductance of the latch network, thereby supporting the positive feedback mechanism responsible for regeneration. These auxiliary inverters provide supplementary charging and discharging paths during regeneration, enabling faster transition of the output nodes without introducing significant capacitive loading at the output terminals. As a result, the delay of the latch is reduced substantially while preserving energy efficiency.

During the first phase ($\text{Clk}=0$), the tail transistors of both the self-cascode preamplifier and dynamic latch remain turned off, ensuring zero static current dissipation. Simultaneously, the PMOS precharge transistors charge the preamplifier output nodes V_{op} and V_{on} to V_{dd} , thereby initializing the differential outputs. At this instant, the lower NMOS transistors of the auxiliary inverter branches are turned on, while the corresponding PMOS devices remain off, thus preparing the latch outputs for the subsequent regeneration cycle. This configuration establishes proper initial conditions at the latch nodes without introducing unnecessary switching activity.

When the clock transitions to the second phase ($\text{Clk}=1$), the tail transistors of the preamplifier and latch are activated, and the self-cascode preamplifier begins discharging V_{op} and V_{on} at rates proportional to the applied differential inputs. If, for example, $V_{ip} > V_{in}$, the node V_{op} discharges more rapidly than V_{on} , thereby generating a sufficient differential voltage at the latch input nodes. This differential voltage activates the regenerative latch, and the auxiliary inverter pairs simultaneously assist in the charging and discharging of Out_p and Out_n . In particular, as the corresponding latch input node discharges, the tail transistor of the latch behaves as an effective current source, while the auxiliary inverter transistors provide additional drive current to accelerate the transition of the output node toward the supply rail. The complementary output node is discharged correspondingly through the regenerative feedback network. Finally, the total delay of proposed comparator 3 (PC3) can be expressed as:

$$t_{total_pc3} = t_{pre} + t_{latch_pc3} \quad (3.19)$$

The delay of dynamic latch with auxiliary inverter used in PC4 is given by [21]

$$t_{latch_pc4} = \frac{C_L}{gm_{eq_d2}} \ln \frac{V_{dd}/2}{|V_{op} - V_{on}|} \quad (3.20)$$

where $gm_{eq_d2} = gm_{M1ai-M4ai} + gm_{M2sl-M3sl} + gm_{M5sl-M6sl} + gm_{M9ai-M10ai}$ is the effective transconductance of the latch which includes shared charge logic as well as auxiliary inverter concepts. The total delay of proposed comparator 2 can be expressed as:

$$t_{total_pc4} = t_{pre} + t_{latch_pc4} \quad (3.21)$$

The inclusion of auxiliary inverter pairs increases the effective transconductance of the latch, thereby accelerating the regeneration process and reducing delay compared to the shared-charge dynamic latch used in PC3. Since these inverters are incorporated within the regenerative path without adding significant capacitive load at the output nodes, the improvement in speed is achieved with only a slight increase in power and energy. As a result, PC4 provides a better delay-performance trade-off while still maintaining high energy efficiency.

3.3.3 Performance Evaluation

The proposed comparator architectures were verified and evaluated using post-layout simulations in Cadence Virtuoso with a 180 nm CMOS technology at a 1 V supply voltage. These simulations were carried out to validate circuit functionality and to accurately extract key performance parameters such as delay, power consumption and energy per conversion. The final layouts of PC3 and PC4, presented in Fig. 3.13(a) and Fig. 3.13(b), occupy 149.5 μm^2 and 156 μm^2 , respectively. The slightly larger area of PC4 is due to the inclusion of auxiliary inverter circuitry; however, the increase is only 4.3%. This indicates that the proposed architectural improvements achieve significant performance gains with negligible area overhead.

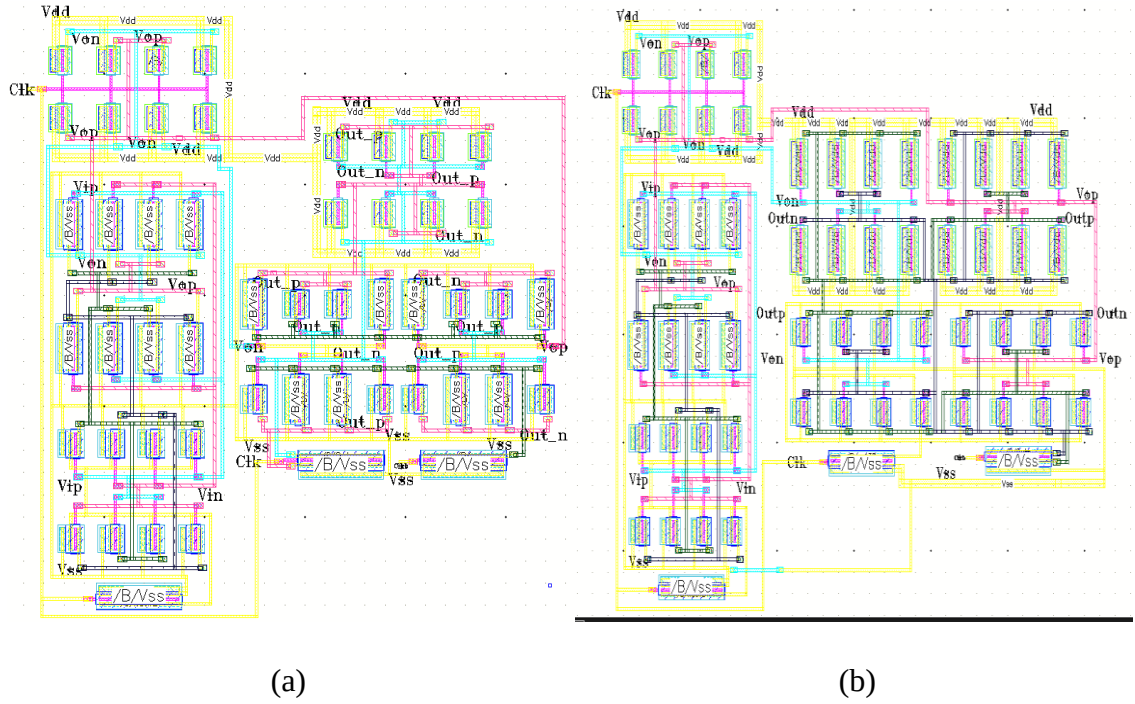
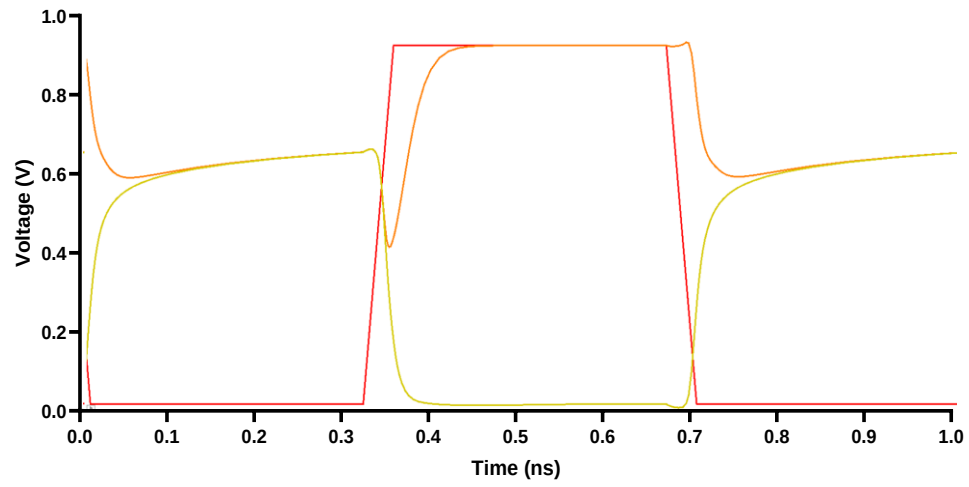


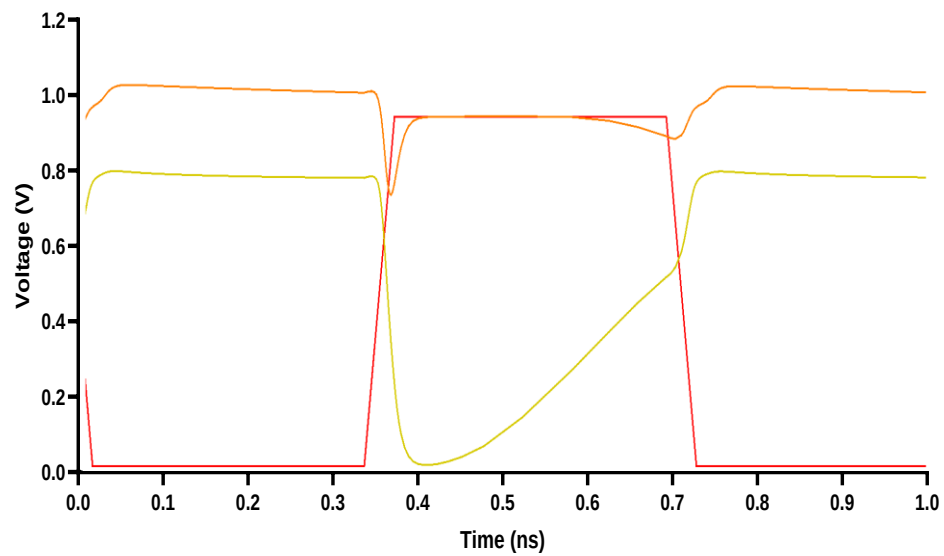
Fig. 3.13. Layout of (a) Proposed comparator 3 (PC3) and (b) Proposed comparator 4 (PC4)

Post-layout transient evaluations were performed to evaluate the dynamic performance of the proposed comparator architectures by applying a ramp input signal (0–1 V) to one input while keeping the other input fixed at a 500 mV reference. The comparator switches when the ramp crosses the reference, enabling extraction of key metrics such as delay, power and energy. The transient responses of PC3 and PC4, shown in Figs. 3.14(a) and 3.14(b), illustrate their switching and regeneration behavior under identical conditions.

It is observed that PC3 achieves a delay of 146.2 ps, power consumption of 107.1 μ W, and energy of 110.2 fJ/conversion. Further improvement is observed in PC4, where the addition of auxiliary inverter pairs reduces the delay to 123.3 ps, while power and energy increase slightly to 114.1 μ W and 115.2 fJ/conversion, respectively. This indicates that the auxiliary inverter-assisted regeneration enhances latch transconductance and accelerates output transitions. Although PC4 shows a modest increase in power, the significant reduction in delay making it appropriate for high speed applications.



(a)



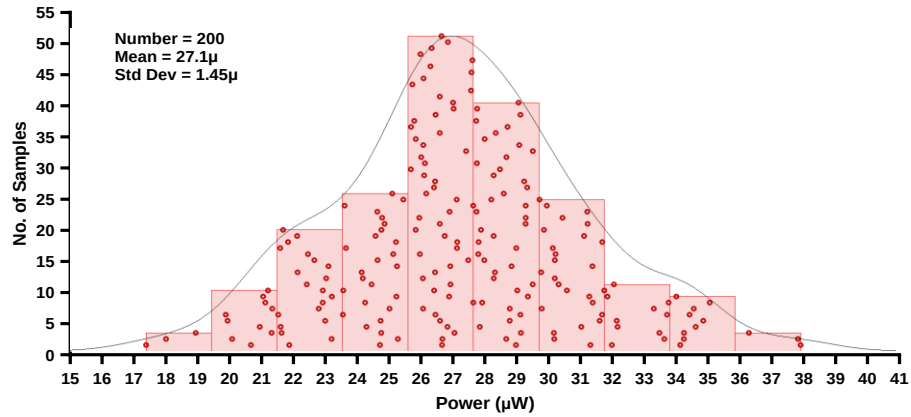
(b)

clk Out_p Out_n

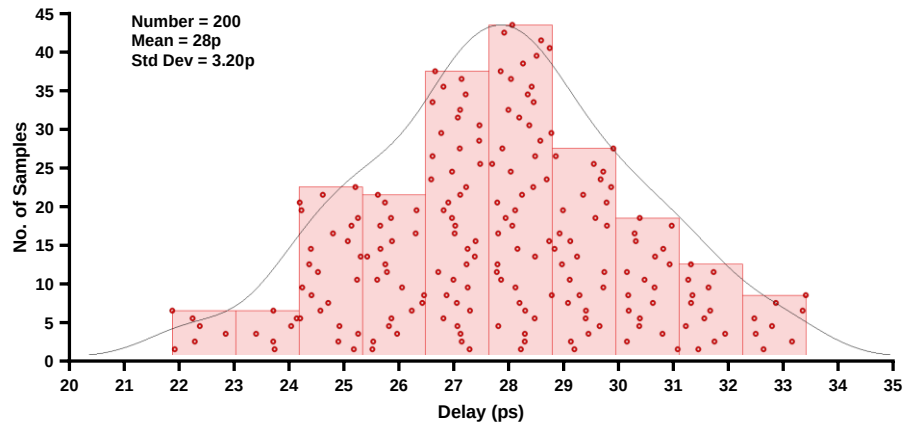
Fig. 3.14. Transient analysis of (a) Proposed comparator 3 (PC3) and (b) Proposed comparator 4 (PC4)

Figures 3.15 and 3.16 present the Monte Carlo simulation analysis for the proposed comparator architectures, showing the statistical variation in power, delay and energy per conversion over 200 samples for PC3 and PC4, respectively. These simulations assess robustness against device mismatch and process variations encountered in fabrication. The results indicate that both designs exhibit tightly clustered distributions around their mean values, demonstrating strong immunity to variability.

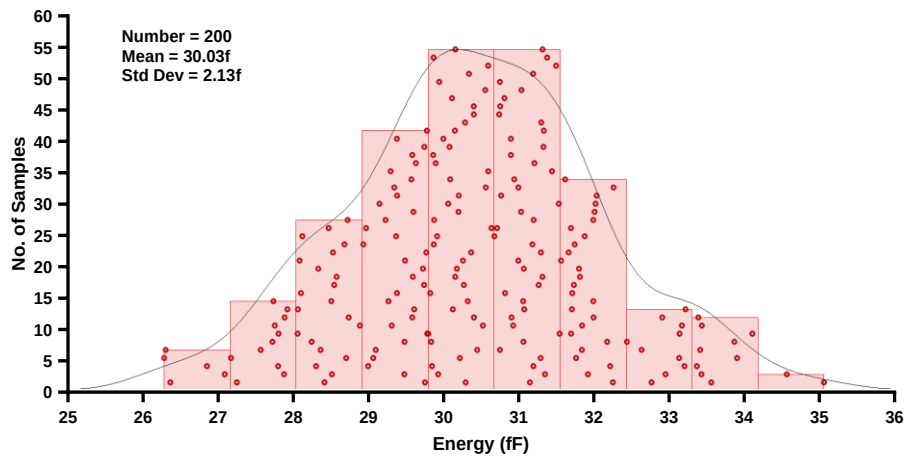
For PC3, the narrow spread in all performance metrics confirms that the shared-charge dynamic latch provides stable and predictable operation under variations. Similarly, PC4 maintains a compact distribution despite the inclusion of auxiliary inverter-based enhancement, indicating that improved regeneration does not compromise robustness. The overall reduction in standard deviation across parameters suggests that the combination of self-cascode preamplifier and optimized latch design improves tolerance to threshold voltage shifts, mobility variations, and mismatch effects.



(a)

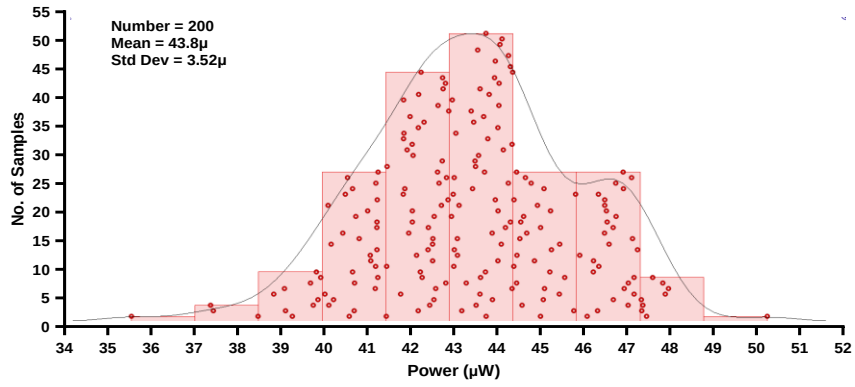


(b)

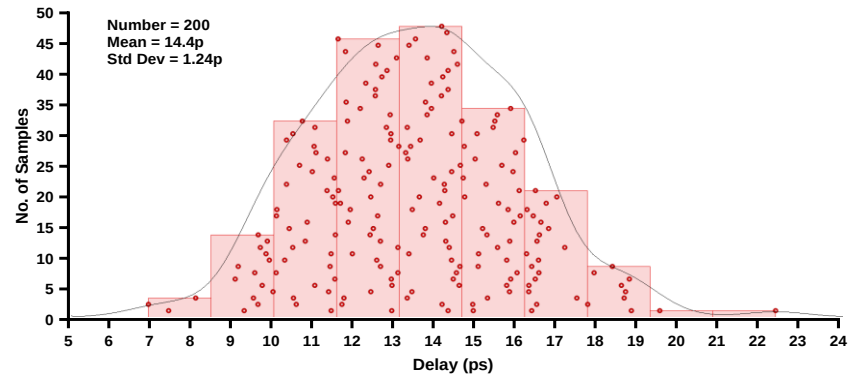


(c)

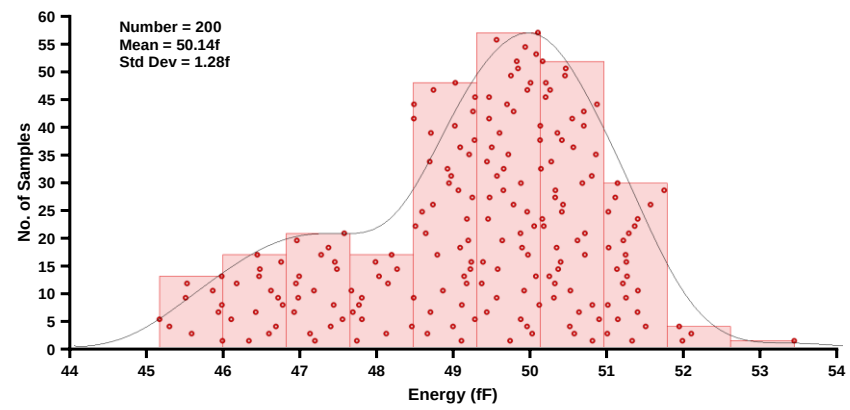
Fig. 3.15 Monte-Carlo simulations for (a) power, (b) delay and (c) energy for Proposed Comparator 3 (PC3)



(a)



(b)



(c)

Fig. 3.16 Monte-Carlo simulations for (a) power, (b) delay and (c) energy for Proposed Comparator 4 (PC4)

The comparative performance analysis presented in Table 3.2 demonstrates the effectiveness of the proposed comparator architectures, PC3 and PC4, relative to previously reported dynamic comparator designs implemented across similar CMOS technology nodes and operating conditions. It is evident that many state-of-the-art comparators reported in literature exhibit either higher propagation delay, increased power dissipation, or inferior energy efficiency, thereby limiting their suitability for modern low-voltage and high-speed ADC applications.

Table 3.2: Comparative analysis of Proposed Comparators with recent works

Parameter Reference	Technology (nm)	Supply voltage (V)	Clock Frequency(GHz)	Power Consumption(μ W)	Delay (ps)	PDP (fJ)	Energy (fJ/conv)	Active Area (μ m ²)
[30]	180	1.2	1	133	100	13.3	-	-
[109]	90	1	1	90	200	18	109	150
[70]	180	1	1	32.62	51.76	1.69	32.6	58.32
[113]	90	1	0.5	20.39	167.6	3.41	-	54.03
[84]	180	1	0.5	188.9	46.4	8.76	-	-
[103]	180	1	1	16.52	72.09	1.2	-	-
[98]	180	1	1	171	672	47.65	165	168
	180	1	1	137	601	114.9	138	162
	180	1	1	117	161	36.6	119	154
Proposed Comparator 3 (PC3)	180	1.2	0.5	65	195.2	19.5	57.1	149.5
	180	1	1	107.1	146.2	39.5	110.2	149.5
	180	1.8	2	69	109	82.3	71.1	149.5
Proposed Comparator 4 (PC4)	180	1.2	0.5	66.5	156	7.15	64.1	156
	180	1	1	114.1	123.3	24.2	115.2	156
	180	1.8	2	74	84.1	18.8	74.4	156

In comparison, the proposed designs consistently achieve a superior balance among delay, power and energy across multiple supply voltages and clock frequencies. Specifically, PC3 demonstrates strong energy-efficient performance, achieving 57.1 fJ/conversion at 1.2 V and 0.5 GHz with a delay of 195.2 ps, while operating at only 65 μ W, indicating the effectiveness of the shared-charge dynamic latch in reducing switching energy and improving overall efficiency. At higher operating conditions of 1 V and 1 GHz, PC3 maintains competitive performance with 146.2 ps delay, 107.1 μ W power, and 110.2 fJ/conversion, confirming robust scalability across different operating points.

Further performance enhancement is observed in PC4, where the incorporation of auxiliary inverter-assisted regeneration significantly improves speed. At 1.2 V and 0.5 GHz, PC4 achieves a reduced delay of 156 ps, corresponding to nearly 20% improvement over PC3 under comparable conditions, while maintaining similar power consumption of 66.5 μ W and energy of 64.1 fJ/conversion. Under more aggressive operating conditions of 1.8 V and 2 GHz, PC4 achieves its best performance with a minimum delay of 84.1 ps, while dissipating 74 μ W and consuming 74.4 fJ/conversion, demonstrating excellent high-speed capability. Although PC4 incurs a modest increase in power and area relative to PC3 due to the inclusion of auxiliary inverter circuitry, the substantial delay reduction and improved power-delay product justify this overhead for high-speed applications.

From the active area perspective, both proposed comparators maintain compact layouts with silicon footprints below 160 μm^2 , which are competitive with or better than several prior-art implementations. Overall, the results validate that PC3 provides an optimized solution for energy-constrained applications requiring low-power operation, whereas PC4 offers superior speed and power-delay performance for high-speed ADC systems. The comparative data thus confirms that the integration of shared-charge logic and auxiliary inverter-assisted regeneration enables the proposed comparator architectures to outperform conventional and previously reported designs in terms of delay, energy efficiency and FoM, making them highly suitable for advanced low-voltage SAR ADC implementations.

3.4 DTMOS-Based Comparator Architectures (PC5 and PC6)

This section presents Proposed Comparator 5 (PC5) and Proposed Comparator 6 (PC6), which utilize a DTMOS-based preamplifier to improve performance under ultra-low supply voltage conditions. Unlike earlier self-cascode designs, these comparators replace the conventional input transistors with DTMOS devices [147], where the gate and body are shorted. This configuration dynamically lowers the threshold voltage during conduction, resulting in higher transconductance, reduced delay and reliable low-voltage operation without additional static power.

In PC5, the DTMOS preamplifier is combined with a static latch, providing enhanced gain and stable decision-making. In PC6, the static latch is replaced to dynamic latch, removing static current paths and further reducing power and energy consumption while improving regeneration speed. Analytical results show that the higher transconductance of DTMOS reduces preamplifier delay.

Simulation results verify the efficacy of the proposed designs and Monte Carlo analysis demonstrates robust performance with low sensitivity to process variations. Comparative analysis shows that the proposed DTMOS-based comparators achieve better delay, power and energy performance than several existing designs, while operating at lower supply voltage.

3.4.1 Circuit Design and Operation

The proposed methodology for PC5 and PC6 is based on enhancing the front-end amplification capability of the comparator through the incorporation of a Dynamic Threshold MOS (DTMOS)-based preamplifier, followed by two alternative latch-stage implementations to optimize the speed–power trade-off. As illustrated in Figs. 3.17 and 3.18, the conventional preamplifier input transistors are replaced by DTMOS devices in which the gate and body terminals are electrically shorted. This dynamic body-biasing

arrangement enables the threshold voltage to vary with the input signal, thereby reducing the threshold voltage during conduction and increasing it during the OFF state. Such dynamic threshold modulation enhances the effective transconductance of the input transistors while maintaining low leakage current, making the architecture particularly advantageous for ultra-low-voltage operation.

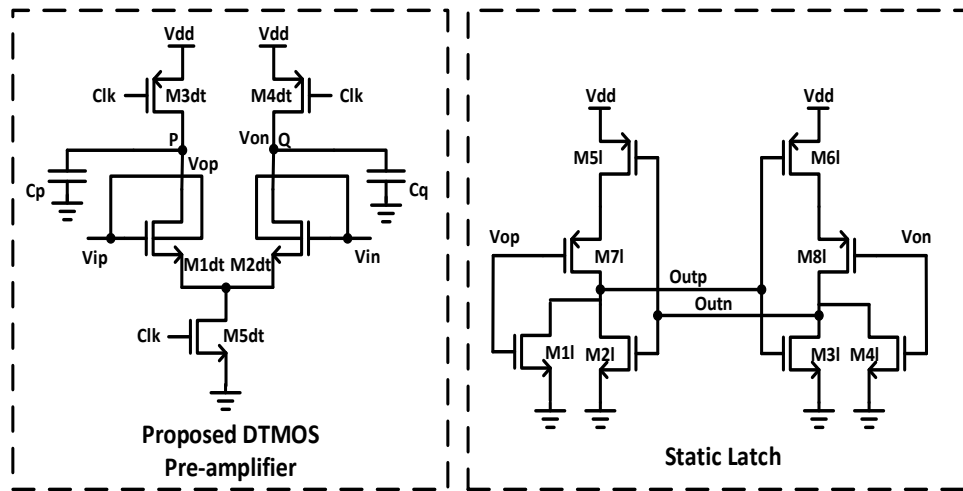


Fig.3.17 Proposed Comparator 5 (PC5) using DTMOs preamplifier with static latch

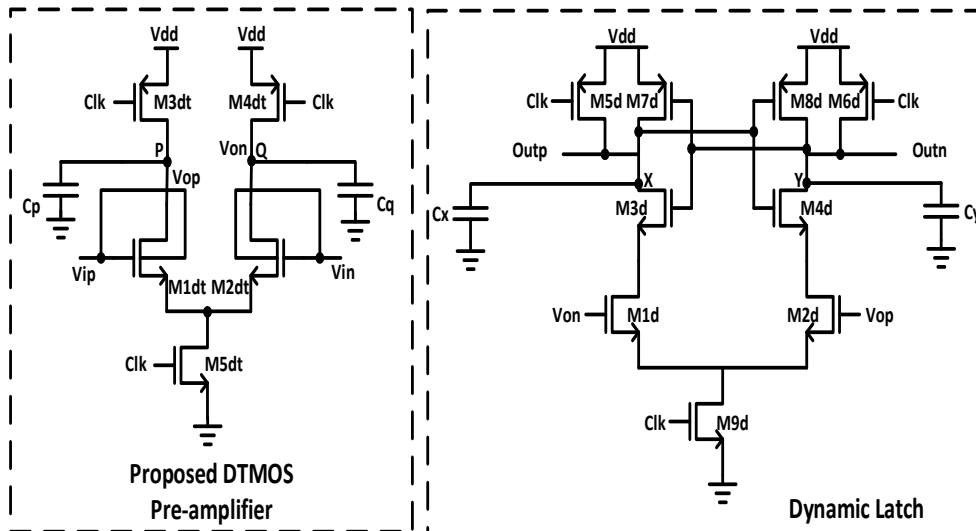


Fig.3.18 Proposed Comparator 6 (PC6) using DTMOs preamplifier with dynamic latch

The gain of the DTMOS-based preamplifier is governed by the transconductance of the input devices and is expressed as:

$$Av(Preamp) = \frac{\Delta V_o}{\Delta V_i} \approx \frac{gm_{1s,2s}(V_{dd}-V_{oen})}{I_{cm}} \quad (3.22)$$

where $gm_{1s,2s}$ is the trans-conductance of transistor M1s or M2s, $V_{oen} = |V_{op} - V_{on}|$, is the output level to enable cross coupled latch and I_{cm} is the current in common mode configuration drawn from the capacitances if placed on nodes P and Q.

Also, for MOSFET to work in saturation region, drain current is expressed as [9]:

$$I_D = \frac{\mu_n C_{ox} W (V_{GS} - V_t)^2 (1 + \lambda V_{DS})}{2 * L} \quad (3.23)$$

For DTMOS device, $gm_{1s,2s}$ can be expressed by differentiating I_D w.r.t. V_{GS} as [9]:

$$I_D = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_n C_{ox} W (V_{GS} - V_t)(1 + \lambda V_{DS})}{L} * \frac{1}{1 + \frac{\gamma}{2 * \sqrt{V_{SB} + \phi_f}}} \quad (3.24)$$

Since the threshold voltage of a DTMOS device decreases dynamically during conduction, the actual transconductance of the input pair becomes higher than that of conventional MOS transistors. This occurs due to body-bias induced threshold modulation, which increases the sensitivity of drain current to gate voltage. As a result, the preamplifier achieves higher voltage gain and produces a larger differential output ($V_{op}-V_{on}$) for a given input signal. Additionally, the enhanced transconductance helps in reducing and stabilizing the common-mode current, improving the robustness of the preamplifier under low-voltage operation.

Delay analysis

To analyze the delay of two proposed comparators, in PC5, the DTMOS preamplifier is followed by a static latch, where the delay is governed by the average propagation delays of the complementary outputs which provides stable operation and reliable regeneration. Further, in PC6, the static latch is replaced with a dynamic latch, whose delay depends on

the regenerative transconductance and internal node capacitances. This latch offers stronger positive feedback, faster regeneration and eliminates static current paths, thereby reducing both delay and power consumption. The overall preamplifier delay is primarily determined by the rate at which the load capacitances at V_{op} and V_{on} are discharged during the evaluation phase.

Therefore, the pre-amplifier delay can be written as:

$$t_{pre_dtmos} \approx \frac{C_{eff} |V_{op} - V_{on}|}{gm_{1s,2s} |V_{ip} - V_{in}|} \quad (3.25)$$

Higher $gm_{1s,2s}$ provides lesser delay.

For PC5, delay for second stage is expressed as :

$$t_{slatch} = \frac{\tau_{PLH} + \tau_{PHL}}{2} \quad (3.26)$$

where τ_{PLH} and τ_{PHL} are lowest to highest and highest to lowest propagation delays associated with either output nodes Out_p / Out_n respectively.

Similarly, for PC6, delay for second stage is written as:

$$t_{dlatch} \approx \frac{C_{xy} |Out_p - Out_n|}{gm_{eqd} |V_{op} - V_{on}|} \quad (3.27)$$

Analytical delay modeling shows that the preamplifier delay is inversely proportional to the effective transconductance of the DTMOS devices and directly proportional to the load capacitance. Due to the higher transconductance achieved through DTMOS operation, the preamplifier can generate the required differential output voltage more rapidly, thereby reducing the time needed to activate the latch stage. This results in an overall improvement in comparator speed.

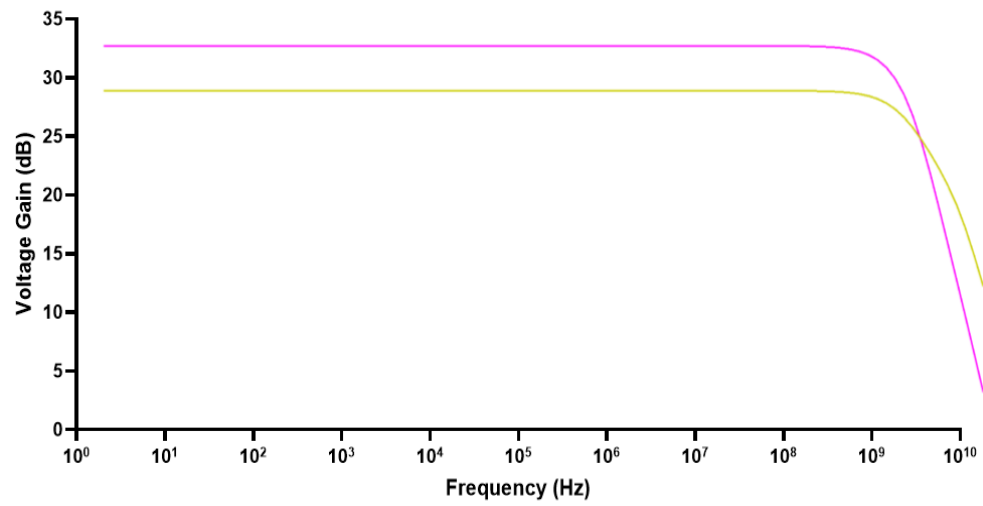
Thus, the proposed approach improves performance under low-voltage conditions by combining DTMOS-based gain enhancement with optimized latch architectures. PC5 focuses on stable and energy-efficient operation using a static latch, while PC6 prioritizes

high speed and low power through a dynamic latch. This approach effectively explores the trade-offs between static and dynamic latch designs while leveraging DTMOS advantages for ultra-low-voltage, high-speed comparator applications.

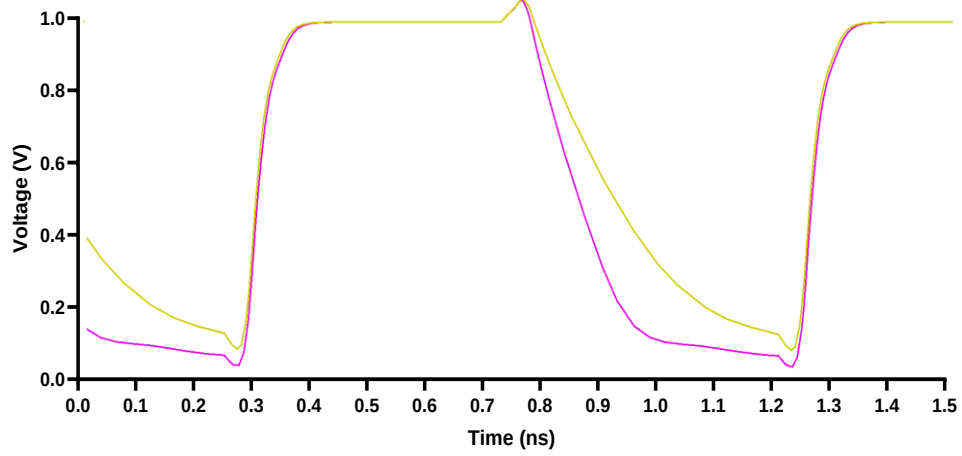
3.4.2 Performance Evaluation

The performance of the proposed DTMOS-based comparator architectures was validated through extensive simulations in Cadence Virtuoso using a 180 nm CMOS technology operating at a reduced 0.6 V supply and 1 GHz clock frequency, targeting ultra-low-voltage and high-speed applications. Both designs were evaluated in terms of preamplifier gain, delay, total comparator delay, power consumption, power delay product (PDP) and energy per conversion.

To isolate the benefit of the DTMOS approach, the preamplifier was first analyzed independently. AC analysis was performed by applying a 0.6 V_{pp} differential input while keeping the other input at a fixed DC level. The results show that the DTMOS preamplifier achieves nearly 25% higher voltage gain compared to a conventional design, confirming improved transconductance due to dynamic threshold modulation (as shown in Fig. 3.19(a)). In addition, transient analysis indicates around 50% reduction in preamplifier delay (shown in Fig. 3.19 (b)), validating that the increased transconductance effectively reduces the charging and discharging time constants. These results confirm that the DTMOS configuration significantly enhances both gain and speed under low-voltage operation.



(a)



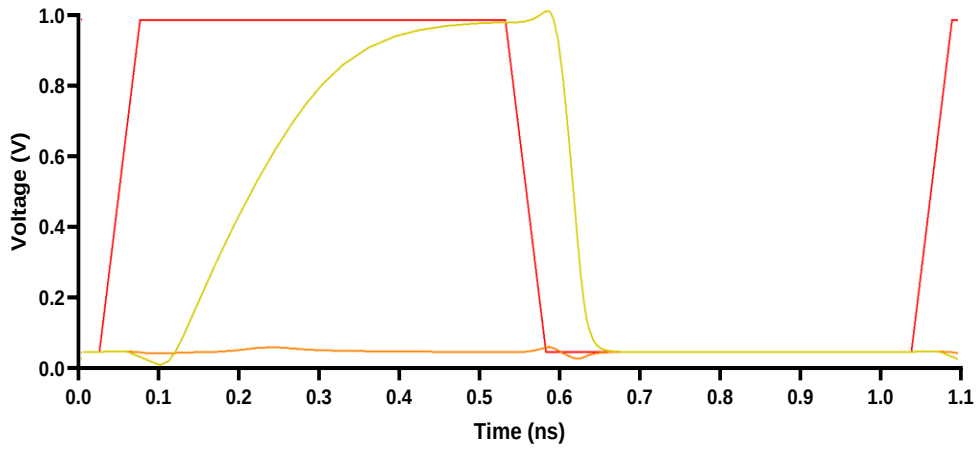
(b)

— Conventional Preamplifier — DTMOS based Preamplifier

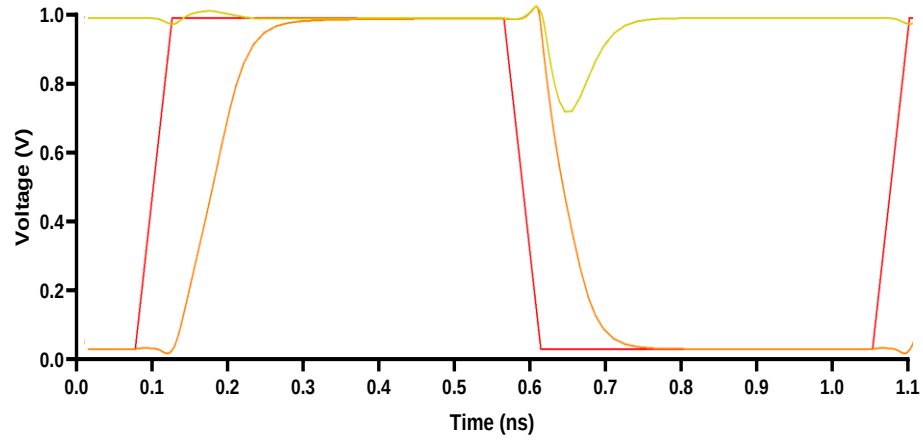
Fig. 3.19. Comparison of (a) Gain and (b) Delay of conventional and DTMOS based Pre-amplifiers

Following the preamplifier characterization, the complete comparator architectures PC5 and PC6 were evaluated through transient simulations by applying a 0.6 V ramp input to one terminal while keeping the other input fixed at a 300 mV reference, representing practical comparison conditions. The transient responses, presented in Fig. 3.20(a) and Fig. 3.20(b), indicate that PC5 achieves a delay of 110.4 ps, whereas PC6 further reduces the delay to 90 ps, demonstrating the advantage of combining a DTMOS preamplifier with a dynamic latch for faster regeneration.

In terms of power consumption, PC5 dissipates 37 μW , while PC6 consumes only 30.6 μW , showing that the dynamic latch in PC6 reduces average power by eliminating static current paths. The corresponding PDP is improved from 4.1 fJ in PC5 to 2.8 fJ in PC6, indicating better energy-delay efficiency. Similarly, the energy per conversion decreases from 34.2 fJ/conversion in PC5 to 29.2 fJ/conversion in PC6, confirming that PC6 provides the better overall performance in terms of speed, power and energy efficiency from PC5.



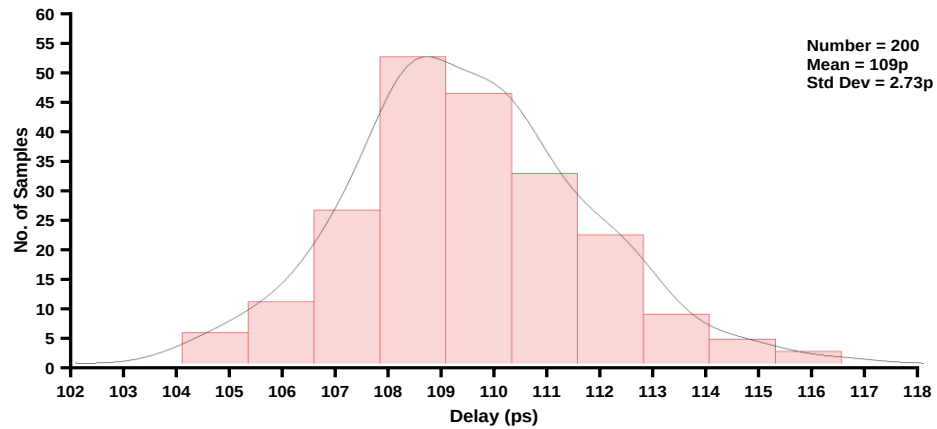
(a)



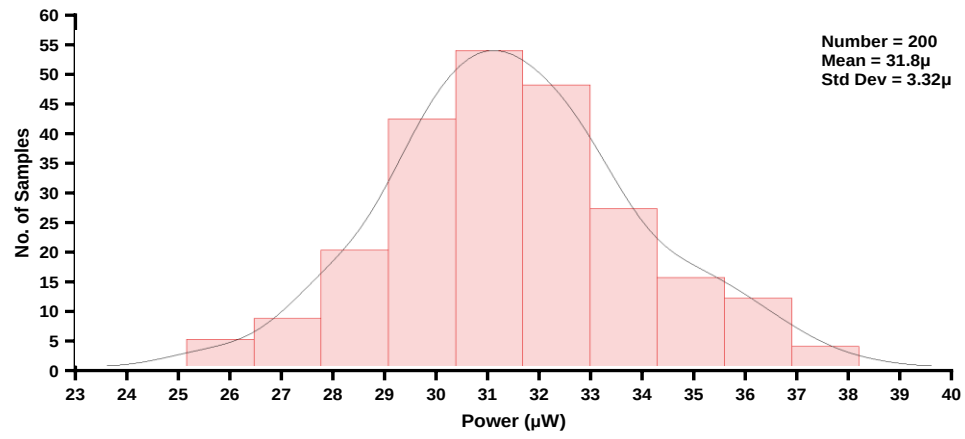
(b)

Fig. 3.20 Transient analysis of (a) Proposed Comparator 5 (PC5) and (b) Proposed Comparator 6 (PC6)

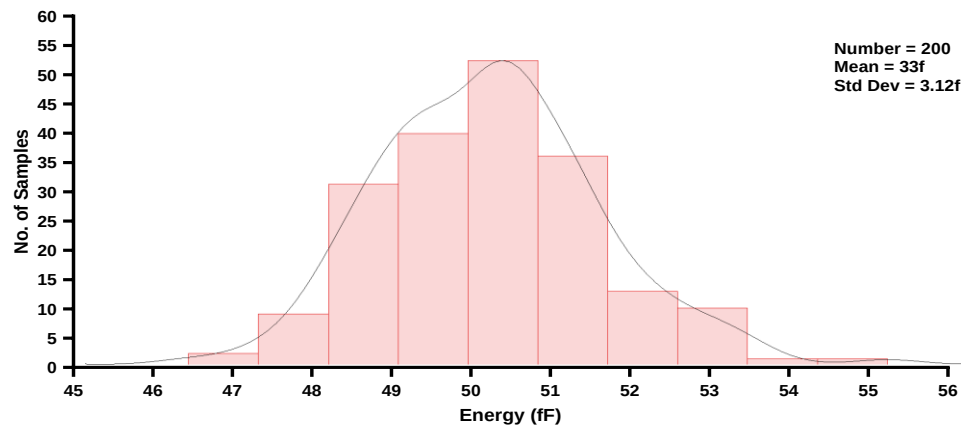
To further assess robustness, Monte Carlo simulations with 200 samples were performed for both comparator architectures, and the statistical distributions of delay, power, and energy are shown in Figs. 3.21 and 3.22.



(a)

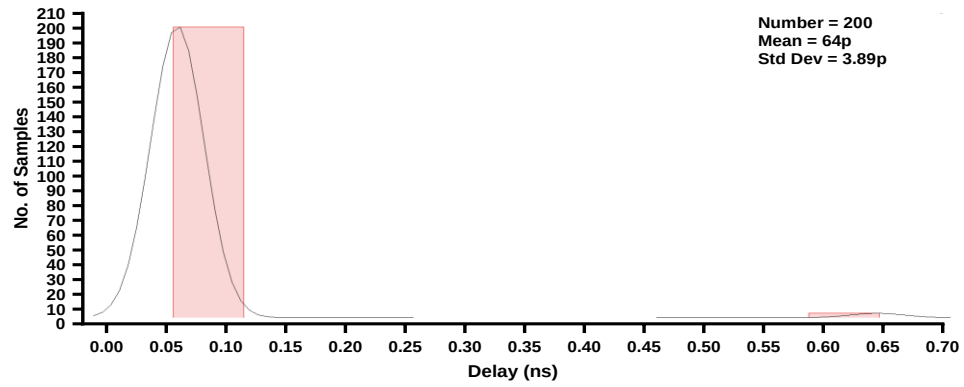


(b)

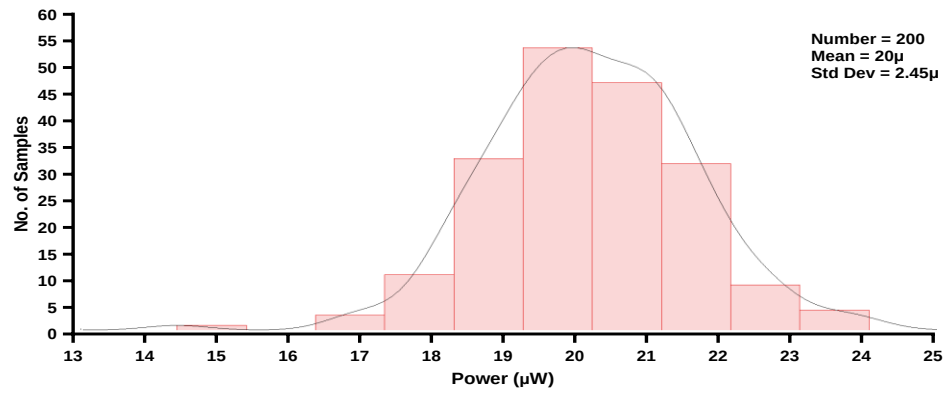


(c)

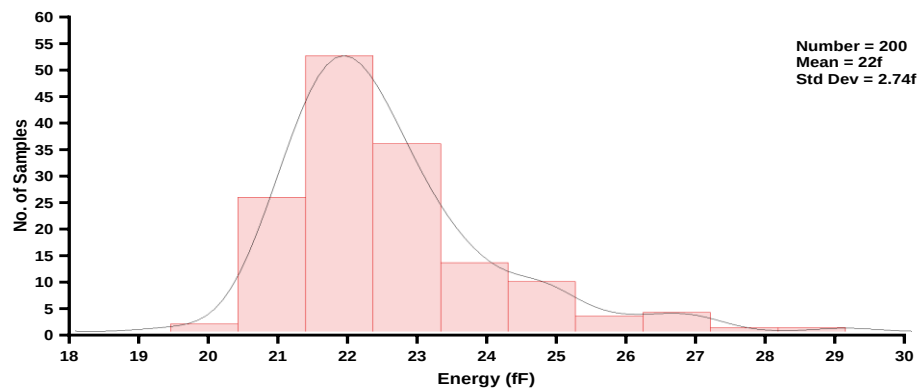
Fig.3.21. Monte Carlo simulation for (a) Delay (b) Power and (c) Energy for PC5



(a)



(b)



(c)

Fig.3.22 Monte Carlo simulation for (a) Delay (b) Power and (c) Energy for PC6

Overall, the simulation results demonstrate that the DTMOS preamplifier significantly improves gain and speed at low supply voltage, while the dynamic latch in PC6 further enhances delay, power and energy performance. Consequently, PC6 emerges as the most efficient architecture among the proposed DTMOS-based comparators.

The comparative analysis presented in Table 3.3 evaluates the execution of the proposed DTMOS-based comparator architectures (PC5 and PC6) against recent state of the art designs implemented in similar CMOS technologies.

Table 3.3: Comparative Analysis of DTMOS based comparators with recent works

Reference \ Parameter	Technology (nm)	Supply voltage (V)	Clock Frequency (GHz)	Power Consumption (uW)	Delay (ps)	PDP (fJ)	Energy (fJ/conv)
[67]	55	1	2	109.1	82.68	9.024	121
[69]	90	1	1	57	72	4.1	52
[103]	90	0.8	1	0.33	240	0.08	-
[30]	180	1.2	1	133	100	13.3	-
[32]	180	1	1	32.62	51.76	1.69	32.6
[68]	180	1	1	16.52	72.1	1.2	-
Proposed Comparator 5 (PC5)	180	0.6	1	37	110.4	4.1	34.2
Proposed Comparator 6 (PC6)	180	0.6	1	30.6	90	2.8	29.2

The results demonstrate that the proposed comparators achieve highly competitive performance while operating at minimized supply voltage of 0.6 V, making them well-suited for ultra-low-voltage applications. Specifically, PC5 achieves a delay of 110.4 ps,

power consumption of 37 μW , PDP of 4.1 fJ, and energy of 34.2 fJ/conversion, which is analogous to or better than several existing designs operating at higher supply voltages.

Further improvement is observed in PC6, which reduces the delay to 90 ps, lowers power consumption to 30.6 μW , and achieves a superior PDP of 2.8 fJ with 29.2 fJ/conversion energy. This highlights the effectiveness of combining a DT MOS preamplifier with a dynamic latch, enabling better speed and energy efficiency. Although some reported designs achieve lower delay, they often operate at higher voltages or consume more power, making them less efficient in terms of overall energy performance.

The ability of PC5 and PC6 to maintain strong performance at 0.6 V confirms the effectiveness of the DT MOS technique in overcoming threshold voltage limitations in low-voltage operation. Overall, the proposed designs achieve an improved balance between delay, power and energy efficiency, making them highly suitable for ultra-low-power SAR ADCs and IoT-based mixed-signal systems.

3.5 Comparison

This section presents the design, analysis, and performance evaluation of six proposed comparator architectures, categorized into three groups based on the underlying circuit enhancement techniques and latch topologies. The first group, comprising PC1 and PC2, introduced the self-cascode preamplifier technique combined with static and dynamic latch configurations, respectively. The second group, PC3 and PC4, further enhanced dynamic comparator performance through shared-charge logic dynamic latch and auxiliary inverter-assisted regeneration, along with self-cascode preamplifier technique. The final group, PC5 and PC6, employed a DT MOS-based preamplifier with static and dynamic latch configurations to facilitate ultra-low-voltage operation.

Table 3.4 Comparison of Performance of Proposed Comparators

Parameter Reference	Technology (nm)	Supply voltage (V)	Clock Frequency (GHz)	Power Consumption (uW)	Delay (ps)	Energy (fJ/conv)	Active Area (um ²)
Proposed	180	1.2	0.5	130	304	116	162
Comparator 1 (PC1)	180	1	1	137	601	138	162
Proposed	180	1.2	0.5	110	220	111	154
Comparator 2 (PC2)	180	1	1	117	161	119	154
Proposed	180	1.2	0.5	65	195.2	57.1	149.5
Comparator 3 (PC3)	180	1	1	107.1	146.2	110.2	149.5
Proposed	180	1.2	0.5	66.5	156	64.1	156
Comparator 4 (PC4)	180	1	1	114.1	123.3	115.2	156
Proposed Comparator 5 (PC5)	180	0.6	1	35.4	105	34.2	168
Proposed Comparator 6 (PC6)	180	0.6	1	30.6	90	29.2	156

The comparative results summarized in Table 3.4 demonstrate a clear progression in comparator performance across the proposed architectures. Among the self-cascode based comparators, PC2 outperforms PC1 due to the adoption of a dynamic latch, reducing delay from 304 ps to 220 ps and lowering power consumption from 130 μ W to 110 μ W at 1.2 V supply. In the second category, the introduction of shared-charge logic and auxiliary inverter-assisted latches in PC3 and PC4 provides further performance enhancement, with PC4 achieving the best delay of 156 ps at 1.2 V while maintaining moderate power

consumption of 66.5 μW , demonstrating the effectiveness of improved latch regeneration. The final category based on DTMOS preamplifiers exhibits the most significant enhancement in low-voltage performance, where PC5 and PC6 successfully operate at 0.6 V supply, substantially lower than the other architectures. Among all six designs, PC6 achieves the best overall energy efficiency, consuming only 29.2 fJ/conversion while maintaining the minimum delay of 90 ps and low power consumption of 30.6 μW , thereby demonstrating the superiority of combining DTMOS gain enhancement with dynamic latch regeneration.

In addition to speed and power improvements, the proposed comparator architectures maintain compact active area footprints, ranging from 149.5 μm^2 to 168 μm^2 , indicating that the performance enhancements are achieved without significant silicon area penalty. A systematic performance trend can also be observed from the comparative data: enhancement of preamplifier gain consistently reduces delay, while the transition from static to dynamic latch structures lowers power and energy consumption. Furthermore, latch-level optimizations such as shared-charge logic and auxiliary inverter-assisted regeneration improve regeneration speed, whereas DTMOS implementation extends the operating range toward ultra-low-voltage applications.

Overall, the results of this chapter confirm that the proposed comparator architectures successfully address the limitations of conventional comparator designs through progressive circuit-level innovations. The self-cascode technique offers an effective means of improving gain and delay under nominal supply voltages, the shared-charge and auxiliary inverter-based latch techniques provide enhanced dynamic performance for high-speed applications, and the DTMOS-based preamplifier enables robust operation at aggressively scaled supply voltages. Depending on application requirements, PC3 and PC4 are well suited for moderate-to-high-speed energy-efficient ADC systems, whereas PC5 and PC6, particularly PC6, emerge as the most promising candidates for ultra-low-power, low-voltage SAR ADC implementations in IoT, biomedical and portable electronic applications.

3.6 Summary

The analysis executed in this chapter demonstrate that the proposed comparator architectures (PC1–PC6) achieve substantial improvements in speed, power consumption, energy efficiency, and robustness compared to conventional designs. These improvements are primarily driven by systematic enhancements at both the preamplifier and latch stages, where techniques such as self-cascode gain boosting, shared-charge logic, auxiliary inverter-assisted regeneration and DTMOS-based operation have been effectively integrated.

The use of self-cascode structures in PC1 and PC2 significantly enhances the intrinsic gain of the preamplifier by increasing output resistance, enabling faster development of the input differential signal and reducing the burden on the latch stage. This directly results in reduced propagation delay and improved sensitivity. Furthermore, the transition from a static latch in PC1 to a dynamic latch in PC2 highlights an important design trade-off: while static latches provide robustness and stable operation, dynamic latches eliminate static current paths and achieve superior energy efficiency and speed.

In the case of PC3 and PC4, the incorporation of shared-charge logic and auxiliary inverter-based latch enhancement leads to notable performance improvements. The shared-charge mechanism minimizes unnecessary voltage swings during regeneration, thereby reducing both switching energy and delay. In PC4, the addition of auxiliary inverters strengthens the regenerative feedback, significantly accelerating the latch operation and resulting in the lowest delay among the mid-voltage designs.

For ultra-low-voltage operation, PC5 and PC6 utilize DTMOS-based preamplifiers, which dynamically adjust the threshold voltage to enhance transconductance and gain at reduced supply levels. This enables reliable and high-speed operation even under low-voltage conditions. Among these, PC6, which combines DTMOS with a dynamic latch, achieves superior overall performance in terms of delay, power, and energy efficiency.

Across all architectures, Monte Carlo analyses indicate improved robustness, with reduced variability in delay and power consumption. This is largely attributed to higher preamplifier gain and faster latch regeneration, which reduce sensitivity to device mismatch and process fluctuations. Additionally, the area overhead introduced by advanced techniques remains minimal, ensuring practical feasibility for integrated circuit implementation.

From a system-level perspective, the proposed comparators facilitate higher sampling rates, reduced energy per conversion, and improved robustness, making them highly suitable for modern SAR ADC applications. While PC1 and PC3 provide a balanced trade-off with better stability and reliability, PC2 and PC4 achieve improved speed and energy efficiency. Among all designs, PC6 delivers the best overall performance in terms of delay, power, and energy. Overall, the results demonstrate that co-design of the preamplifier and latch stages, along with targeted architectural enhancements, effectively overcomes the limitations of conventional comparators and enables optimized performance for low-voltage, high-speed, and energy-efficient mixed-signal systems.

Chapter 4

Low Power ADC

This chapter presents the design and implementation of a low-power SAR ADC architecture incorporating multiple energy-efficient circuit techniques. The proposed methodology focuses on reducing dynamic switching energy, minimizing capacitor area, improving sampling linearity and enhancing overall conversion efficiency. A split-capacitor DAC structure is modified and adopted to reduce total capacitance and silicon overhead while preserving conversion resolution. To further reduce power consumption, a V_{cm} -based switching approach and an optimized switching methodology are introduced to minimize unnecessary capacitor transitions during charge redistribution. A detailed explanation of the proposed ADC architecture, circuit implementation and operating principles are provided. Simulation-based performance evaluation is presented through transient analysis, switching energy comparison, static linearity analysis and dynamic performance characterization. The obtained results demonstrate the effectiveness of the proposed low-power techniques in achieving improved energy efficiency while maintaining acceptable conversion accuracy and system performance.

4.1 Introduction

The growing requirement for battery-operated compact electronics, wireless sensor networks, biomedical implants and IoT devices has intensified the need for low power and high resolution ADCs capable of operating under stringent energy constraints. Among the various ADC architectures, SAR ADC has emerged as standout solutions for medium resolution and moderate-speed applications due to its inherently low power consumption, scalable digital-friendly architecture, and compatibility with deep-submicron CMOS technologies [36]. In a SAR ADC, the CDAC constitutes a dominant portion of the overall power dissipation, primarily due to repetitive capacitor charging and discharging during the bit-cycling process. As converter resolution increases, the number and size of

capacitors in the DAC array grow exponentially, leading to higher switching energy, larger silicon area, increased settling time, and degraded overall energy efficiency. Consequently, optimization of DAC switching energy has become a critical design objective in modern SAR ADC architectures.

Conventional charge-redistribution DAC switching techniques require substantial switching energy because the capacitor array undergoes full-scale transitions during successive approximation cycles. Numerous switching algorithms have been put forward in literature to mitigate this issue, including monotonic switching [21], V_{cm} -based switching [104] and split-capacitor arrays [116]. While these approaches reduce switching energy to varying extents, many suffer from trade-offs such as increased capacitor count, larger digital control complexity or degraded linearity. Therefore, there remains a strong need for an energy-efficient DAC switching methodology that simultaneously minimizes switching power, capacitor array size, and circuit complexity while preserving high linearity and conversion accuracy.

To address these challenges, this chapter presents a low-power SAR ADC architecture employing an optimized DAC switching methodology based on capacitor splitting, monotonic switching and V_{cm} -assisted reference switching techniques. The proposed approach significantly reduces the effective DAC switching energy by minimizing high-weight capacitor transitions and lowering the total capacitance requirement of the DAC array while maintaining a steady common-mode voltage during resolution. Furthermore, the ADC integrates a high-speed dynamic comparator to complement the low-energy DAC architecture and ensure rapid bit decisions during the successive approximation process. By combining capacitor splitting with an energy-optimized switching algorithm, the proposed SAR ADC aims to achieve improved power efficiency, reduced switching energy, enhanced linearity, and compact silicon area. The methodology and performance evaluation presented in this chapter demonstrate the applicability of the proposed structure for next-generation low-power mixed-signal systems targeting IoT and portable sensing applications.

4.2 Proposed Methodology

4.2.1 Proposed SAR ADC Architecture

The proposed structure is designed to achieve low power absorption, reduced switching energy, and improved conversion linearity by combining a fully differential split-capacitor DAC structure with V_{cm} -based switching and bootstrap sampling techniques. The generalized architecture is shown in Fig. 4.1. The converter mainly consists of bootstrap switches, differential capacitive DAC arrays ((DACp and DACn), a dynamic regenerative comparator, SAR logic and reference switching circuitry. The complete architecture operates on the principle of successive approximation, where the input signal in analog form is converted into output in digital form through iterative comparison and charge redistribution.

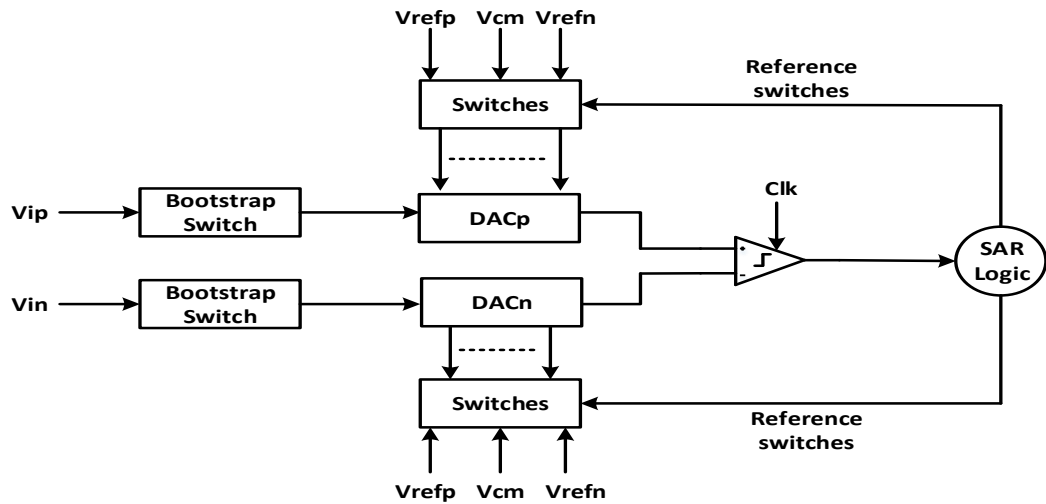


Fig. 4.1 Generalized N bit SAR ADC architecture

The ADC employs a fully differential topology to improve immunity against supply noise and common-mode disturbances. Two alike capacitor arrays are employed for the positive and negative signal paths, namely DACp and DACn. These arrays generate differential DAC voltages that are applied to the comparator inputs during each conversion cycle.

Compared to single-ended architectures, the differential implementation provides improved noise rejection, better linearity, and enhanced robustness under low-voltage operation.

4.2.2 Bootstrap Switch

The analog input sampling stage utilizes the bootstrap switch circuit shown in Fig. 4.2. In conventional MOS sampling switches, the ON resistance varies with the input signal amplitude because the gate-to-source voltage changes dynamically during sampling [48]. This variation introduces nonlinear distortion and degrades ADC accuracy. To eliminate this problem, the proposed bootstrap circuit dynamically boosts the gate voltage of the sampling transistor during the first phase. The bootstrap circuit consists of capacitors C1, C2 and C3 along with clock-controlled transistors M1–M12. During the next phase, the bootstrap capacitors are charged with supply voltage. When the clock enters the sampling phase, the stored charge raises the gate voltage of the sampling transistor above V_{dd} , thereby maintaining an approximately constant gate-to-source voltage (V_{GS}). As a result, the ON resistance of the sampling switch remains nearly constant across the entire input voltage range. This significantly improves sampling linearity and enables reliable operation under low supply voltage conditions.

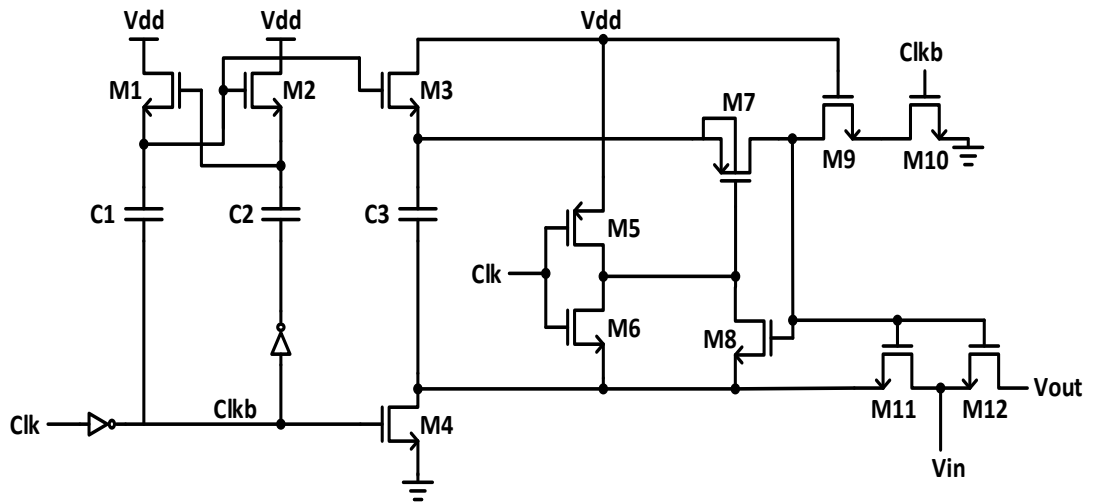


Fig. 4.2 Bootstrap Switch

4.2.3 Vcm-based Switching Network

The proposed DAC also incorporates a Vcm-based switching technique to further minimize switching energy. In conventional switching methods, capacitor bottom plates are switched directly between Vrefp and Vrefn, resulting in large voltage transitions and high dynamic power consumption. In the proposed approach, an additional common-mode reference voltage Vcm is introduced along with Vrefp and Vrefn. During the initialization phase, most capacitor bottom plates are connected to Vcm, which establishes a balanced common-mode condition across the differential DAC outputs. During bit cycling, only selected capacitors are switched between the reference voltages according to the SAR logic decisions. Since many switching transitions occur between Vcm and Vrefp or Vrefn instead of full-scale transitions between the two reference voltages, the total switching energy is substantially reduced.

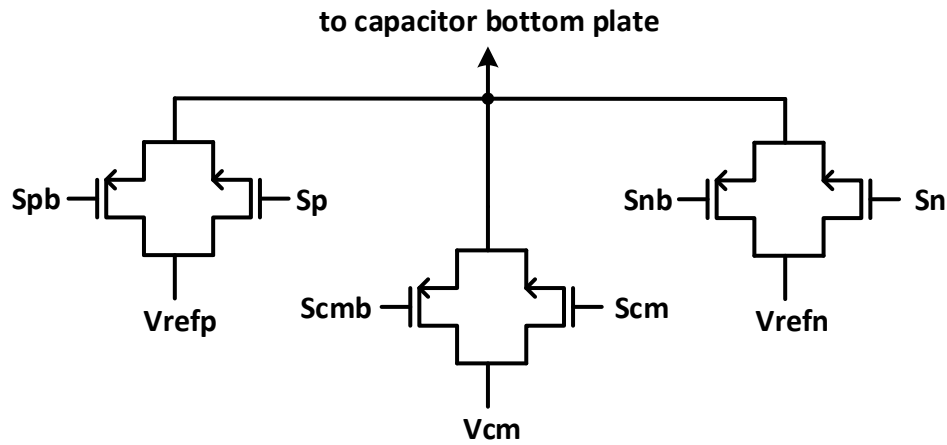


Fig. 4.3 Vcm-based switching network

The reference switching network used for capacitor bottom-plate switching is shown in Fig. 4.3. Each capacitor bottom plate is connected to Vrefp, Vcm and Vrefn through CMOS transmission gates controlled by complementary SAR logic signals. Transmission gates are used instead of single MOS switches to avoid threshold voltage loss and maintain low ON resistance over the entire signal range. During each conversion cycle, the SAR

logic activates the appropriate transmission gate, thereby connecting the capacitor to the required reference voltage. This switching structure ensures accurate charge redistribution, improved switching linearity, and reduced signal-dependent errors.

4.2.4 Split-Capacitor DAC

To minimize the total capacitance and switching energy of the DAC, the proposed converter utilizes a modified split capacitor DAC architecture (as shown in Fig. 4.4). In conventional binary weighted capacitor arrays, the capacitor size increases exponentially with ADC resolution, resulting in large silicon area and increased settling time. To overcome these limitations, the proposed design divides the DAC into multiple capacitor branches consisting of high-capacitance, low-capacitance, and unit-capacitance sections. Instead of using a bridge capacitor, a unit capacitance is employed towards unit-capacitance section and all the capacitors are arranged in binary-weighted form to preserve accurate charge redistribution during successive approximation.

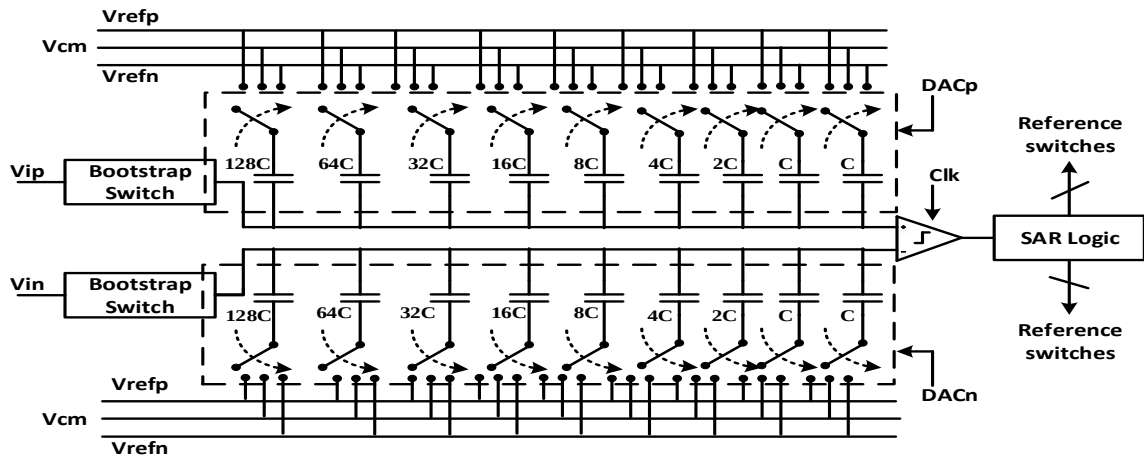


Fig. 4.4 Realized 10-bit SAR ADC

By implementing this modified capacitor splitting scheme, the effective total DAC capacitance is significantly reduced without affecting the overall resolution of the ADC. This reduction in capacitance directly decreases switching power, silicon area and delay, thereby improving both energy efficiency and conversion speed.

4.2.4 Proposed Energy-optimized Switching Methodology

The proposed DAC switching methodology, shown in Figs. 4.5, 4.6 and 4.7, operates through an energy-optimized multi-phase charge redistribution process specifically designed to minimize switching activity and reduce overall DAC energy consumption during SAR conversion. The comparator used during the switching process is dynamic triggered with Clk. The conversion cycle begins with the acquisition and first-bit decision phase (Fig. 4.5) during which the analog differential signal is send on the top plates of all DAC capacitors through transmission-gate switches controlled by the sampling clock. In this phase, the bottom plates of the high and low capacitor banks are placed to the lowest voltage V_{refn} (0), while the unit capacitor branches are biased at the common-mode voltage V_{cm} ($1/2$).

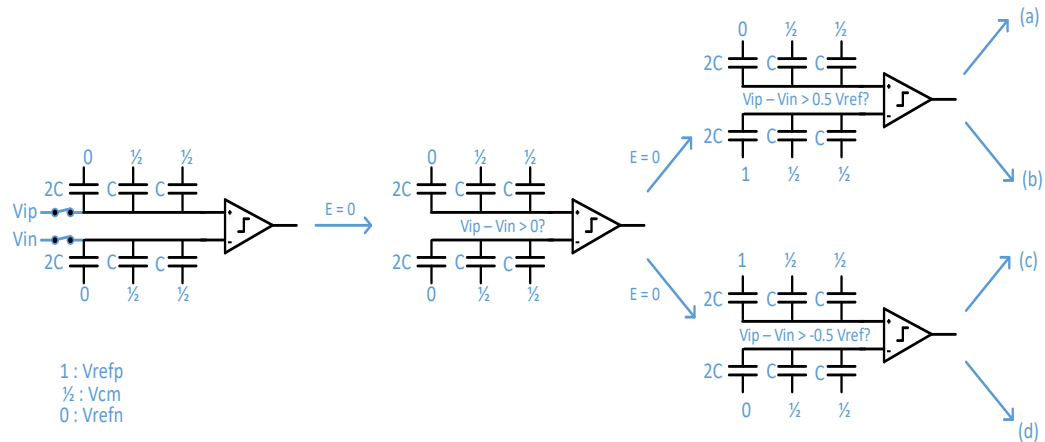


Fig. 4.5 Switching mechanism of the SAR ADC with 4-bit resolution for acquisition and first bit resolution

Since the initial comparison is done immediately after sampling without requiring any DAC capacitor transition, the MSB is resolved minus incurring switching energy. This zero-energy first-bit decision significantly improves the energy efficiency of the proposed SAR ADC assimilated with conventional switching schemes where the DAC array undergoes a full-scale transition for MSB determination.

Following the MSB decision (Fig. 4.6), the second $(N-2)^{\text{th}}$ bit decisions are executed using a monotonic differential switching strategy. For each subsequent bit y , the switching action is determined by the previously resolved bit D_{y-1} . Based on this decision, one of the capacitor arrays (DACp or DACn) remains unchanged while the corresponding capacitor in the opposite array transitions from $V_{\text{refn}}(0)$ to $V_{\text{refp}}(1)$. All remaining capacitors preserve their existing switching states. This one-sided differential switching approach minimizes unnecessary capacitor transitions and assures that the common mode voltage of the DAC outputs remains nearly steady throughout the process, thereby reducing comparator offset sensitivity and improving linearity. The dynamic switching energy associated with each of these intermediate bit decisions is analytically represented by

$$E_y = \left\{ (1 - 2D_{y-1}) \sum_{x=1}^{y-1} (2D_x - 1) 2^{N-y-x-2} \right\} C V_{\text{ref}}^2 \quad (4.1)$$

which depends on the previous comparator decisions and the binary weighting of the switched capacitor. This formulation confirms that the proposed switching algorithm substantially lowers switching energy relative to conventional binary-search DAC switching methods.

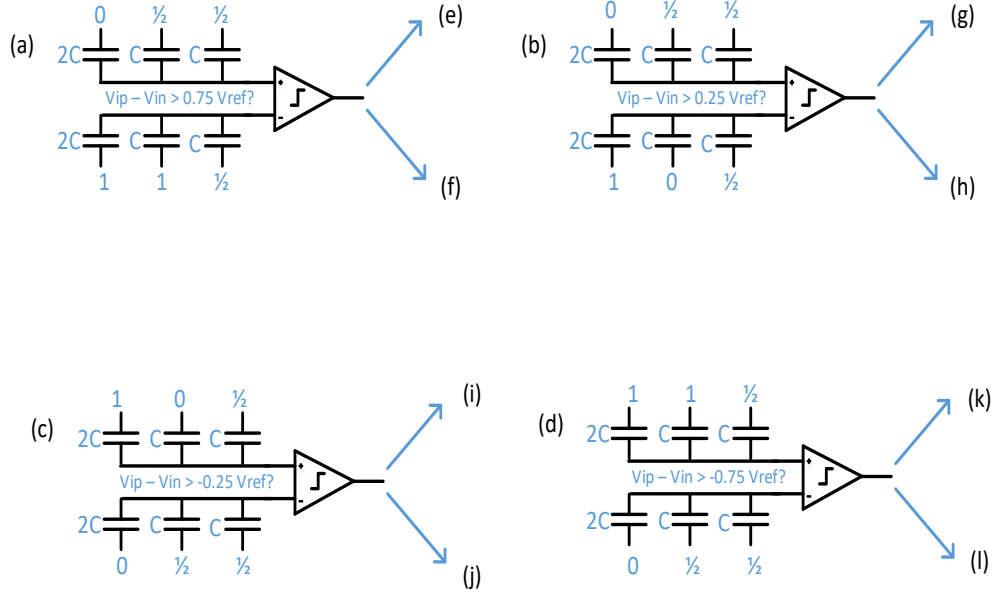


Fig. 4.6 Switching procedure for 2nd to (N-2)th bit decisions

During the penultimate (N-1)th bit decision, the proposed architecture exploits the unit capacitor branch and the additional common-mode reference voltage V_{cm} to achieve higher effective resolution without increasing DAC array size. In this step, the first unit capacitor in the lower-voltage DAC branch transitions from V_{cm} to either V_{refp} or V_{refn} , established from former determined bit D_{N-2} . The introduction of V_{cm} as an intermediate reference voltage enables tri-level switching, effectively improving voltage resolution while avoiding the need for larger binary-weighted capacitor arrays. The associated switching energy for this phase is described by

$$E_{N-1} = \left\{ 1 - 2D_{N-2} \sum_{x=1}^{N-2} (2D_x - 1) 2^{N-x-1} \right\} C V_{ref}^2 \quad (4.2)$$

which remains significantly lower than that of conventional switching due to the reduced voltage swing of the unit capacitor branch.

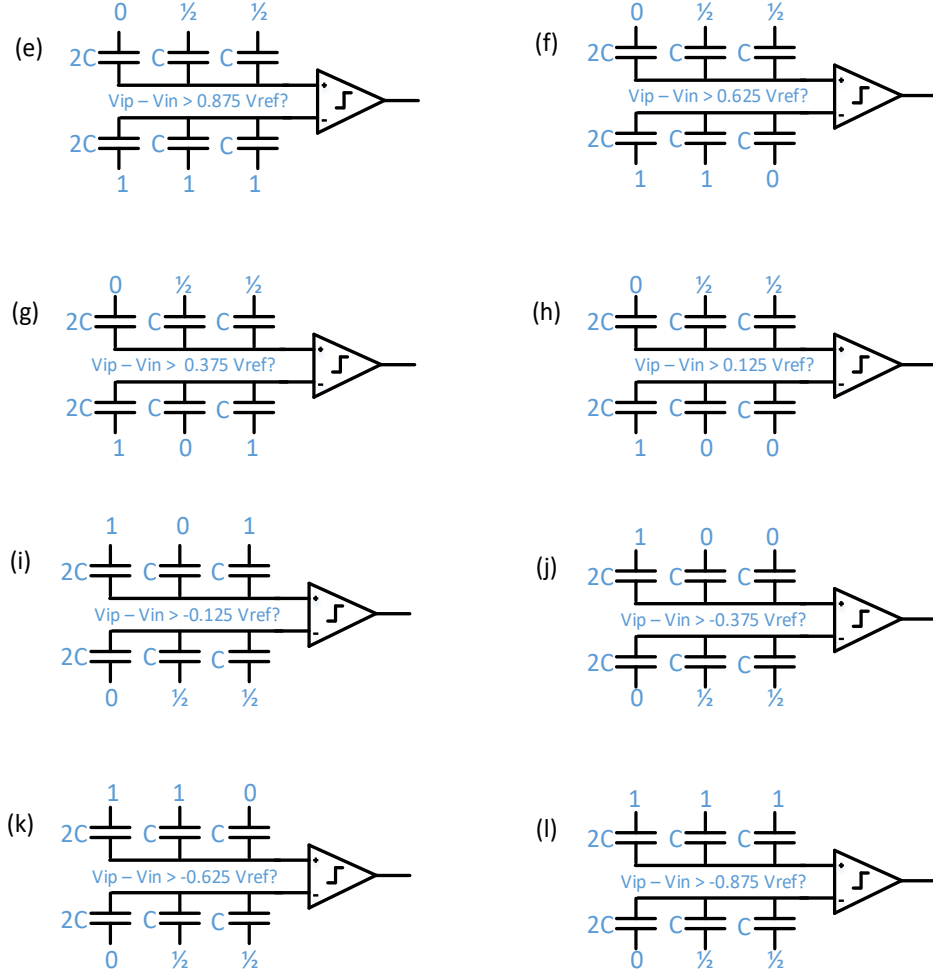


Fig. 4.7 Switching procedure for (N-1)th and (N)th bit decision

In the final (Nth) bit decision (Fig. 4.7), the last remaining unit capacitor is toggled between V_{cm} and the appropriate reference voltage to resolve LSB. The comparator then performs the final comparison and generates the last decision bit D_N . Since only the smallest capacitor in the DAC array is switched during this phase, the corresponding energy consumption is minimal, as expressed by

$$E_N = D_{N-1} \left\{ \sum_{x=1}^{N-2} (1 - D_x) 2^{N-x-1} \right\} C V_{ref}^2 \quad (4.3)$$

By carefully controlling the sequence of unit-capacitor switching in the final two conversion cycles, the proposed architecture achieves fine-resolution voltage quantization with negligible incremental energy overhead.

Assuming a uniform distribution of input codes, the average DAC switching energy over all possible conversion cycles is represented by

$$E_{avg} = \left\{ \sum_{y=2}^{N-1} 2^{N-y-2} - 2^{N-2y-1} \right\} C V_{ref}^2 \quad (4.4)$$

which demonstrates that the proposed switching technique attains substantial energy lessening by minimizing high-weight capacitor transitions and exploiting common-mode assisted switching. This optimized combination of split-capacitor architecture, monotonic differential switching, V_{cm} -assisted tri-level reference generation and zero-energy MSB decision enables the proposed SAR ADC to achieve significantly lower switching energy, reduced DAC capacitance, improved linearity, and enhanced power efficiency compared to conventional and previously reported DAC switching techniques.

The operation of the ADC begins with the first phase (sampling), during which the differential signals V_{ip} and V_{in} are sampled on the top plates of capacitor arrays through the bootstrap switches controlled by the sampling clock Clk . After completion of this phase, the switches are turned OFF, and the sampled charge is held on the capacitor arrays. The SAR logic then initiates the conversion phase by performing a binary search operation to determine each output bit sequentially from MSB to LSB. During each comparison cycle, the SAR logic updates the switching states of the DAC capacitors, thereby generating the corresponding analog reference voltage. This DAC generated voltage is equated with the sampled input voltage through the dynamic regenerative comparator, where its output determines whether the selected DAC voltage is higher or lower than the input, and SAR logic updates the corresponding bit accordingly. This process continues iteratively until all 10 bits are resolved.

4.3 Results

The implementation of the proposed low power SAR ADC architecture employing the energy-optimized DAC switching technique was thoroughly evaluated through circuit-level simulations on 180 nm CMOS technology. The ADC operates at a 1 V supply voltage with a sampled frequency of 20 MS/s, targeting low-power and moderate-resolution applications. The evaluation focuses on key performance metrics including switching energy, power consumption, linearity (INL/DNL), spectral performance (SNDR, SFDR, ENOB) and overall FoM.

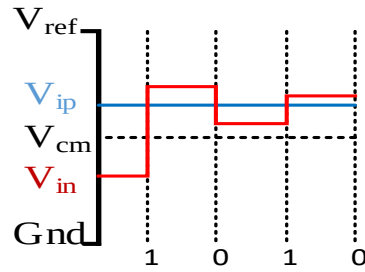


Fig. 4.8 Output waveform of proposed DAC circuit

4.3.1 DAC Transient Response and Switching Energy Comparison

The transient response of the DAC switching mechanism, illustrated in Fig. 4.8, confirms correct operation of the proposed switching sequence and validates the effectiveness of the charge redistribution process. The blue waveform represents the sampled input voltage V_{ip} , while the red waveform represents the DAC output voltage V_{in} generated during the bit-by-bit conversion process. Initially, the DAC output starts from ground potential and is subsequently adjusted according to the SAR logic decisions. During each comparison cycle, the DAC output either increases or decreases toward the input signal level depending on the comparator output. The digital sequence shown below the waveform represents the corresponding bit decisions obtained during the conversion process. A detailed comparison of switching energy across different DAC switching techniques (e.g.

conventional, Vcm- based, monotonic and set and down), as shown in Fig. 4.9, indicates that the proposed Vcm-based, split-capacitor monotonic switching scheme achieves a significant reduction in energy consumption. The average switching energy is measured to be approximately $65 \text{ CV}_{\text{ref}}^2$, which corresponds to a 74.5% reduction compared to conventional switching techniques. This substantial improvement highlights the effectiveness of minimizing high-weight capacitor transitions and utilizing intermediate reference levels to reduce overall energy dissipation.

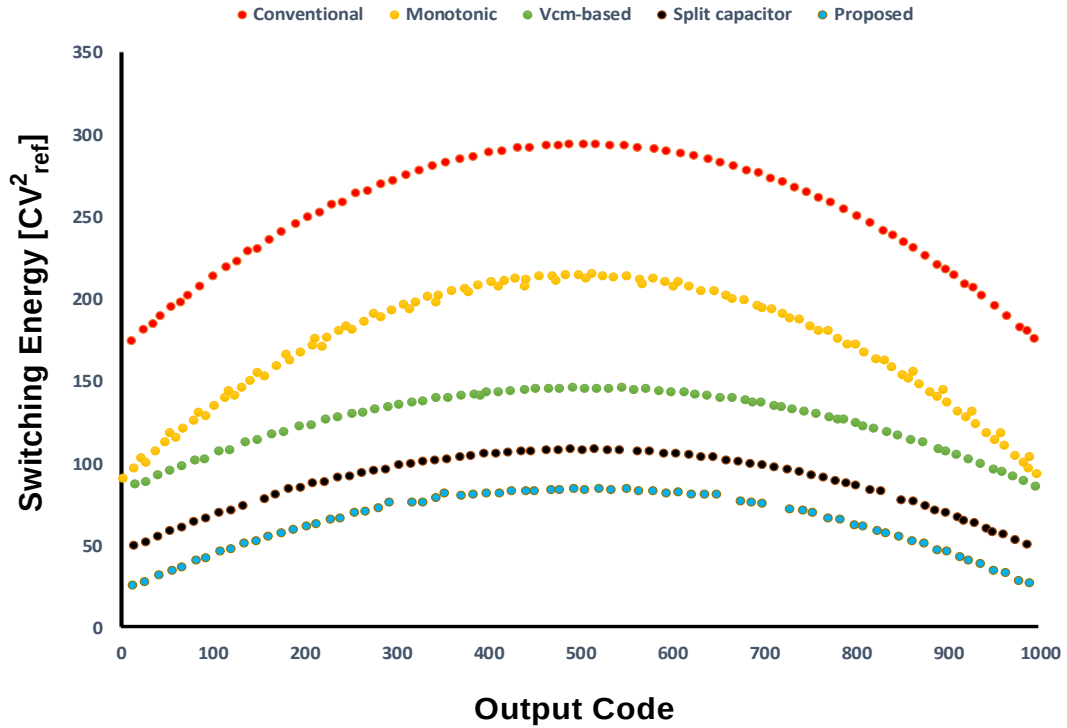
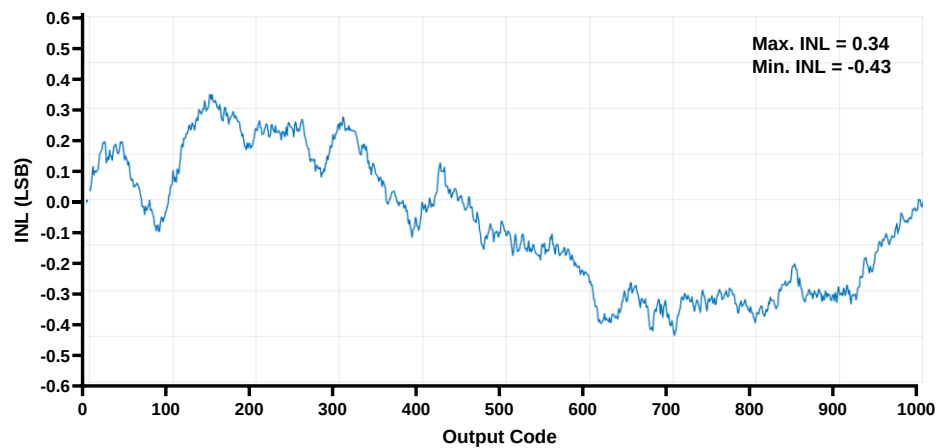


Fig. 4.9 Comparison of switching energy in various DAC switching methods

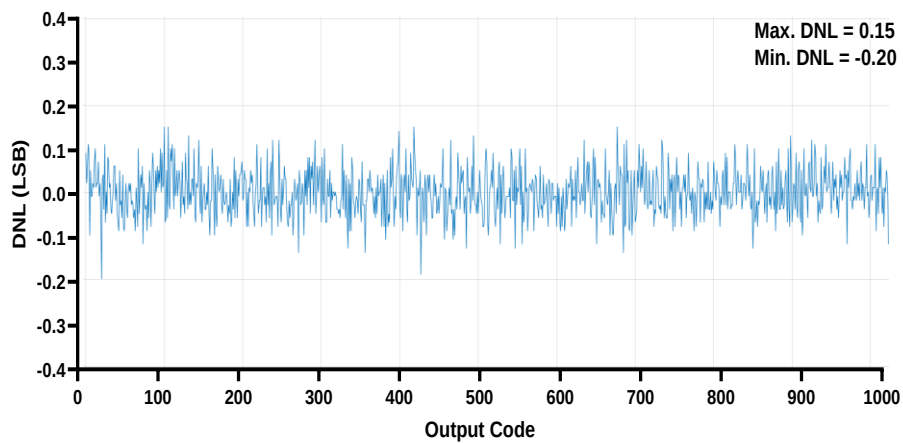
4.3.2 Static Linearity and Power Consumption Analysis

The static performance of the ADC was evaluated through linearity analysis, with simulations conducted at a 1 V supply, 20 MHz sampling frequency and 1.56 MHz input signal rate. The INL and DNL characteristics are presented in Fig. 4.10(a) and Fig. 4.10(b),

respectively. The measured INL ranges between -0.43 LSB and +0.34 LSB, while the DNL varies between -0.20 LSB and +0.15 LSB, both remaining well within the acceptable limit of ± 1 LSB. These results confirm that the proposed ADC maintains good static linearity and satisfies accuracy requirements for high-resolution applications, as compared to the state of art works.



(a)



(b)

Fig. 4.10 (a) INL (b) DNL of SAR ADC

In terms of power performance, the overall power dissipation of the ADC is calculated to be 53.20 μ W, demonstrating the low-power nature of the proposed architecture. The energy efficiency is further quantified using FoM, defined as the ratio of power consumption to the product of sampling rate and effective resolution. The proposed ADC accomplishes FoM of approximately 3.11 fJ/conversion-step, indicating superior energy efficiency in contrast to prevailing SAR ADC designs.

4.3.3 Dynamic Performance Analysis

The dynamic performance of the proposed ADC was analyzed using FFT of the output spectrum, as shown in Fig. 4.11. The ADC achieves SNDR of 60.85 dB and SFDR of 76 dB, comparable to ENOB of 9.74 bits. These results prove that the proposed design maintains high spectral purity and resolution under nominal operating conditions.

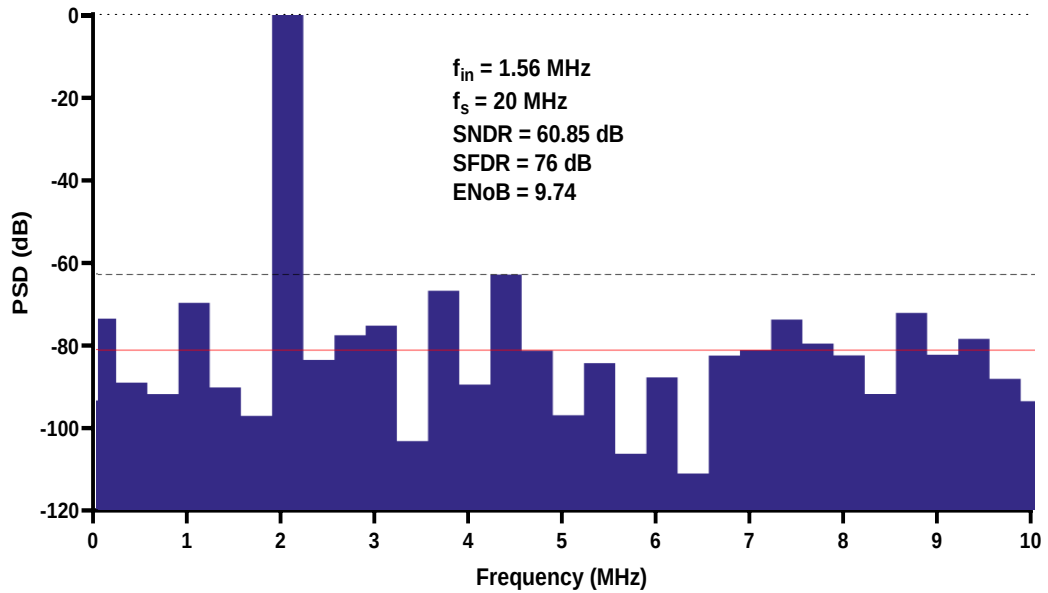


Fig. 4.11 FFT of SAR ADC

In the proposed architecture, the DAC switching network remains the dominant power consumer, followed by dynamic comparator and SAR logic, as shown in Fig. 4.12. Based

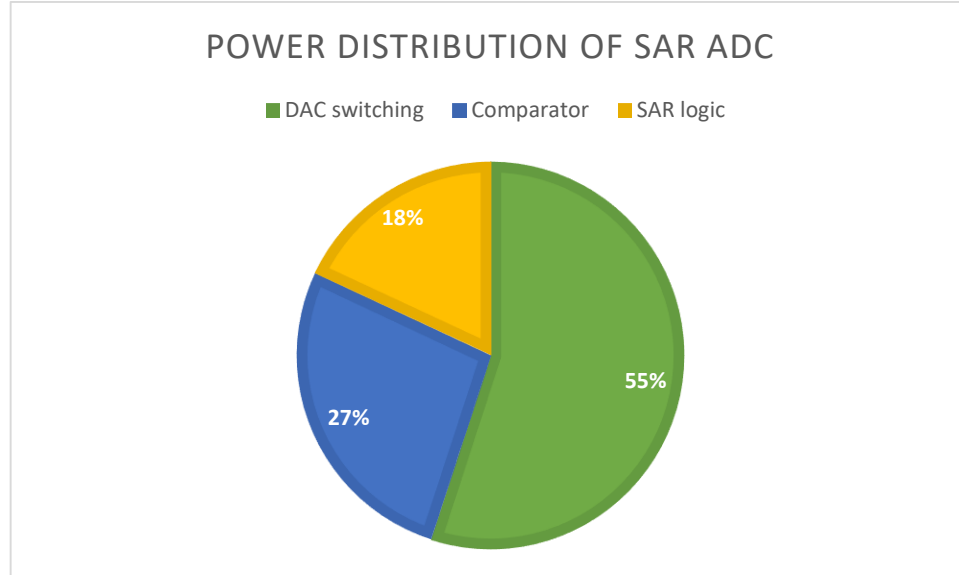


Fig. 4.12 Power Distribution of SAR ADC

on the simulation results, approximately 55% of the total power is consumed by the DAC switching, 27% by the comparator and rest 18% by asynchronous SAR logic. On the other side, a conventional synchronous SAR ADC typically exhibits a higher DAC power contribution because of larger binary capacitor arrays and higher switching activity. The split capacitor architecture and optimized switching methodology considerably reduces DAC energy. Additionally, the asynchronous logic minimizes unnecessary clock transitions, resulting in a lower overall power consumption than the conventional architecture.

The comparative performance analysis presented in Table 4.1 evaluates the proposed SAR ADC against several state-of-the-art designs implemented in similar 180 nm CMOS technology, highlighting its effectiveness in achieving a superior balance between power, energy efficiency and resolution. It is evident that prior works either operate at higher supply voltages or incur significantly higher power consumption to achieve comparable resolution and dynamic performance. For instance, designs reported in [39] and [26] consume substantially higher power of 5760 μW and 589 μW , respectively, while

achieving lower or comparable ENOB values. Similarly, although some designs such as [122] achieve slightly higher ENOB of 9.97 bits, they operate at much lower sampling rates (0.2 MS/s), which limits their applicability in moderate-speed systems.

In contrast, the proposed SAR ADC operates at a sampling rate of 20 MS/s with a 1 V supply, achieving an ENOB of 9.74 bits, which is highly competitive among the compared designs. The dynamic performance metrics, including SNDR of 60.85 dB and SFDR of 76 dB, demonstrate that the proposed architecture maintains high spectral purity and signal fidelity. Furthermore, the static linearity performance, with INL and DNL confined within ± 1 LSB, confirms accurate conversion characteristics comparable to or better than existing techniques.

Table 4.1: Performance comparison of SAR ADC with recent works

Parameter Reference	Technology (nm)	ADC precision (bits)	Frequency for sampling (MS/s)	Operating Voltage (Volt)	SNDR (dB)	SFDR (dB)	ENOB (bits)	INL (LSB, 10^{-2})	DNL (LSB, 10^{-2})	Power Consumption(μ W)	FoM (fJ/conv. step)
[26]	180	8	50	1.2	48.16	52.41	7.7	52	70	589	56.65
[39]	180	10	70	1.8	58.26	64.87	9.39	18.7	19	5760	179.9
[50]	180	10	1	1	57.81	68.63	9.31	16	15	15.25	24.03
[122]	180	10	0.2	1	61.77	78.06	9.97	26	33	4.45	22.2
Proposed Work	180	10	20	1	60.85	76	9.74	34	15	53.20	3.11

A key highlight of the proposed work is its considerably improved energy efficiency, as reflected by FoM of 3.11 fJ/conversion-step, which is substantially lower than all referenced works. This improvement is primarily attributed to the optimized DAC switching methodology that reduces switching energy by minimizing capacitor transitions

and leveraging V_{cm} -based switching. Additionally, the total power consumption of 53.20 μW is considerably lower than most high-speed counterparts, demonstrating the effectiveness of the proposed design in achieving low-power operation without compromising performance.

Overall, the comparison clearly establishes that the proposed SAR ADC achieves an optimal trade-off among speed, resolution, power, and energy efficiency, outperforming existing designs particularly in terms of FoM. This makes the proposed architecture highly suitable for energy-constrained, moderate-speed applications such as IoT devices, wearable systems, and portable sensing platforms, where both power efficiency and conversion accuracy are critical design requirements.

4.4 Summary

The results obtained from the proposed SAR ADC architecture clearly demonstrate that the integration of an energy-optimized DAC switching technique with a fully differential charge redistribution framework leads to substantial improvements in power efficiency, linearity, and overall converter performance. The primary contributor to these enhancements is the decrease in switching energy in CDAC, which traditionally dominates the overall power dissipation in SAR ADCs. By employing a combination of V_{cm} -based switching, capacitor splitting and monotonic charge redistribution operation, the proposed methodology effectively minimizes the number of high-weight capacitor transitions during the conversion process. This directly reduces the dynamic power consumption linked with repeated charging and discharging of large capacitive nodes, which is reflected in the significant reduction in average switching energy.

One of the key observations from the results is the elimination of switching energy during the MSB decision phase, achieved through the top-plate sampling technique. Since no capacitor transition occurs during this initial comparison, a considerable portion of energy consumption is avoided at the outset of the conversion cycle. Furthermore, during

subsequent bit decisions, the use of one-sided monotonic switching ensures that only one branch of the differential DAC undergoes voltage transition while the other remains unchanged. This not only reduces switching activity but also upholds a nearly constant common-mode voltage at the comparator input, thereby improving comparator stability and reducing offset-related errors. The introduction of V_{cm} as an intermediate reference level in later conversion stages further enhances energy efficiency by reducing voltage swing during capacitor switching, particularly for lower-weight capacitors.

The capacitor splitting technique plays a crucial role in reducing the overall DAC capacitance without degrading resolution. By dividing the capacitor array into high, low, and unit capacitor branches, the design achieves a reduction in total capacitance and hence switching energy, while still maintaining accurate charge redistribution. This approach also contributes to reduced silicon area and improved settling behavior of the DAC, which is essential for high-speed operation. Importantly, the use of split capacitors does not introduce significant mismatch errors due to the parasitic capacitance associated with bottom plate node, as evidenced by the measured INL and DNL values, which remain well within ± 0.5 LSB. This confirms that the proposed architecture maintains high static accuracy despite aggressive energy optimization. Additionally, for large scale manufacturing and high yield operation, background digital calibration or capacitor mismatch calibration is beneficial to compensate for process induced capacitor variations and maintain linearity.

From a dynamic performance perspective, the achieved SNDR of 60.85 dB and SFDR of 76 dB indicate that the proposed ADC preserve good spectral performance and low distortion levels. The corresponding ENOB of 9.74 bits demonstrates that the energy-efficient switching scheme does not compromise effective resolution. Additionally, the low power consumption of 53.20 μ W combined with FoM of 3.11 fJ/conversion-step highlights the superior energy efficiency of the proposed design compared to existing techniques. This improvement in FoM is particularly significant, as it reflects the

combined benefits of reduced switching energy, efficient comparator operation and optimized DAC architecture.

Another important feature of the proposed design is its suitability for low voltage and moderate-speed applications. Operating at a 1 V supply and 20 MS/s sampling rate, the ADC achieves a favorable trade-off between speed and energy consumption, making it ideal for applications such as IoT nodes, wearable electronics, and biomedical sensing systems. Unlike some prior works that achieve higher resolution or lower energy at the cost of reduced sampling rate or increased circuit complexity, the proposed architecture maintains a practical trade-off across all performance metrics.

However, certain design trade-offs must also be acknowledged. The implementation of tri-level switching and multiple reference voltages (V_{refp} , V_{refn} , and V_{cm}) introduces additional complexity in reference generation and switching control circuitry. Careful design of reference buffers and switching networks is required to ensure accurate voltage levels and avoid additional power overhead. Therefore, the proposed SAR ADC architecture successfully addresses the key limitations of conventional designs by reducing DAC switching energy, minimizing capacitance, and maintaining high linearity and dynamic performance. The combination of advanced switching techniques and optimized circuit design results in a highly energy-efficient ADC with competitive resolution and speed. These characteristics make the proposed ADC a strong candidate for next-generation low-power mixed-signal systems, particularly in applications where energy efficiency is of paramount importance.

Chapter 5

Hybrid Flash-SAR ADC

This chapter presents the design and implementation of a low-power and high-speed Hybrid Flash-SAR ADC architecture intended to improve conversion efficiency while minimizing energy consumption. The proposed architecture employs a 4-bit flash ADC front-end and a 6-bit SAR ADC back-end to realize overall 10-bit conversion resolution. To improve overall energy efficiency, the proposed architecture incorporates a segmented split-capacitor DAC combined with an optimized V_{cm} -based switching methodology. A detailed description of the proposed methodology, circuit implementation, operating sequence and performance evaluation of the Hybrid Flash-SAR ADC are provided. Comprehensive simulation results are provided and comparative analysis demonstrates that the proposed Hybrid Flash-SAR architecture successfully achieves improved conversion speed with reduced switching energy and lower overall power consumption compared with conventional SAR ADC implementations.

5.1 Introduction

The growing demand for high speed data acquisition in modern techniques such as wireless communication systems, imaging sensors and high-performance data converters has driven the need for ADC architectures that simultaneously achieve high sampling rates, low power consumption, and moderate-to-high resolution. Conventional ADC architectures, including flash [9] and SAR converters [20], present inherent trade-offs in this regard. Flash ADCs offer extremely high conversion speed due to their parallel comparison mechanism; however, their exponential growth in comparator count with increasing resolution effects in excessive power being consumed and vast silicon area. In contrast, SAR ADCs are widely recognized for their excellent energy efficiency and compact implementation, but their sequential bit-by-bit conversion process inherently limits achievable sampling speed, especially for higher resolution designs.

To overcome these limitations, hybrid Flash-SAR ADC architectures have emerged as an effective solution by combining the advantages of both architectures [89]. In such systems, a low-resolution flash front-end is employed to rapidly resolve the MSBs, thereby significantly reducing conversion latency, while a SAR-based back-end performs fine quantization of the leftover LSBs with efficient energy. This partitioning enables a substantial improvement in overall conversion speed without incurring the full power and area penalties associated with high-resolution flash ADCs. However, existing hybrid approaches often face challenges related to switching energy in the DAC, synchronization complexity between flash and SAR stages, and inefficient timing control due to global clock dependency, which limit their scalability and efficiency at higher operating frequencies.

Recent advancements in ADC design have focused on optimizing individual building blocks such as comparators, DAC switching schemes and SAR logic. While techniques such as Vcm-based switching [168], capacitor splitting [169] and non-binary DAC architectures [40] have demonstrated reduced switching energy, they often introduce increased design complexity or additional circuit overhead. Similarly, conventional synchronous SAR logic relies on a fixed clock period, which must accommodate worst-case delay conditions, thereby limiting speed and energy efficiency. To address this, asynchronous SAR control techniques have been explored, where each conversion step is initiated dynamically based on finishing of the previous operation, enabling faster bit cycling and reduced unnecessary power consumption.

Motivated by these challenges, here the work presents a 10-bit hybrid Flash-SAR ADC architecture that integrates multiple design optimizations to achieve high speed and energy efficient operation. The intended architecture employs a 4-bit flash stage for coarse resolution and a 6-bit SAR stage for fine resolution, along with a non-binary segmented DAC to reduce switching energy and capacitor size. Additionally, an asynchronous multi-phase SAR logic eliminates the need for a global clock, thereby improving conversion speed and reducing control overhead. A dynamic comparator is further incorporated to

enhance low-voltage operation and reduce delay. Through this co-optimization of architecture, DAC switching, and control logic, the proposed hybrid ADC aims to achieve an optimal balance between speed, power and accuracy, making it appropriate for next-generation high speed and energy efficient mixed-signal systems.

5.2 Proposed Methodology

Figure 5.1 illustrates the conventional fully differential SAR ADC architecture. The ADC comprises of bootstrap switches, differential CDAC arrays (DAC_p and DAC_n), a dynamic comparator, SAR logic and an encoder block. Throughout sampling phase controlled by Clk_s the differential inputs V_{pi} and V_{ni} are tested onto the capacitor arrays through bootstrap switches, which provide improved linearity by maintaining nearly constant switch resistance. The DAC arrays generate differential reference voltages through charge redistribution based on the switching decisions provided by the SAR logic. The DAC arrays generate differential reference voltages through charge redistribution based on the switching decisions provided by the SAR logic.

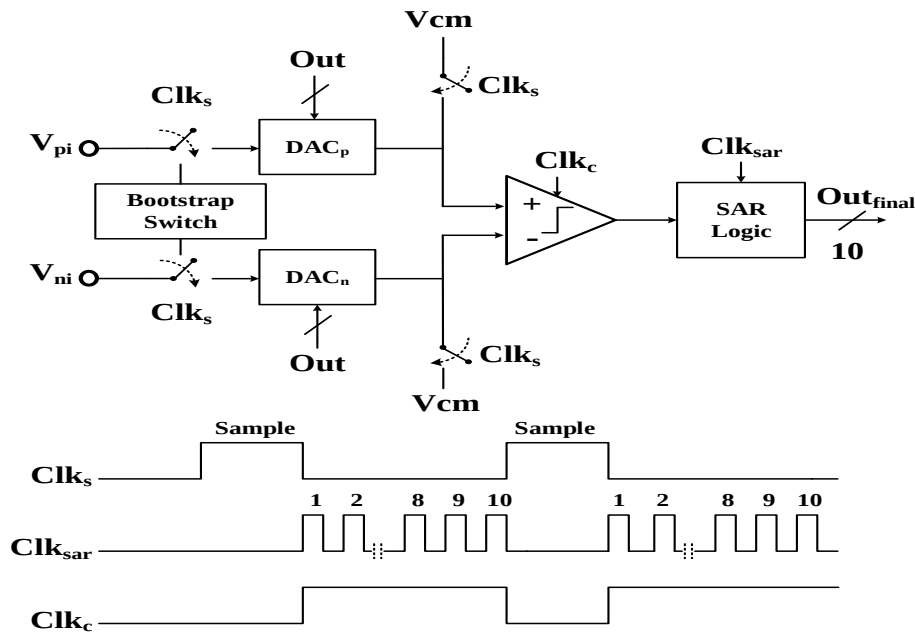


Fig.5.1 Conventional SAR architecture

The comparator, activated by clock Clk_c , compares the differential DAC outputs and produces the decision bit for each conversion cycle. The SAR logic performs the binary search operation sequentially from MSB towards LSB using clock Clk_{sar} and updates the DAC switching states accordingly. Finally, the encoder block assembles the generated bits to produce the final 10-bit digital output $\text{Out}_{\text{final}}$. The timing waveforms shown below the architecture illustrate the synchronization between the sampling clock, SAR clock and comparator clock during the conversion process.

5.2.1 Proposed Hybrid Flash-SAR ADC Architecture

The proposed hybrid Flash-SAR ADC structure combines the high speed operation of Flash ADCs with energy efficiency and better resolution capability of SAR ADCs to realize a low-power and high-performance 10-bit converter. The suggested hybrid Flash-SAR ADC are shown in Fig. 5.2, while the detailed transistor-level implementation of the complete 10-bit ADC is instantiated in Fig. 5.3. The proposed architecture mainly consists of bootstrap switches, a segmented CDAC structure, flash logic, a dynamic comparator, SAR logic and an output encoder. By partitioning the conversion operation between Flash and SAR stages, the architecture significantly improves conversion speed while maintaining reduced switching energy and low power consumption. The converter employs a fully differential structure to improve immunity against supply noise and common-mode disturbances. Differential input signals V_{pi} and V_{ni} are sampled through bootstrap switches controlled by the sampling clock Clk_s .

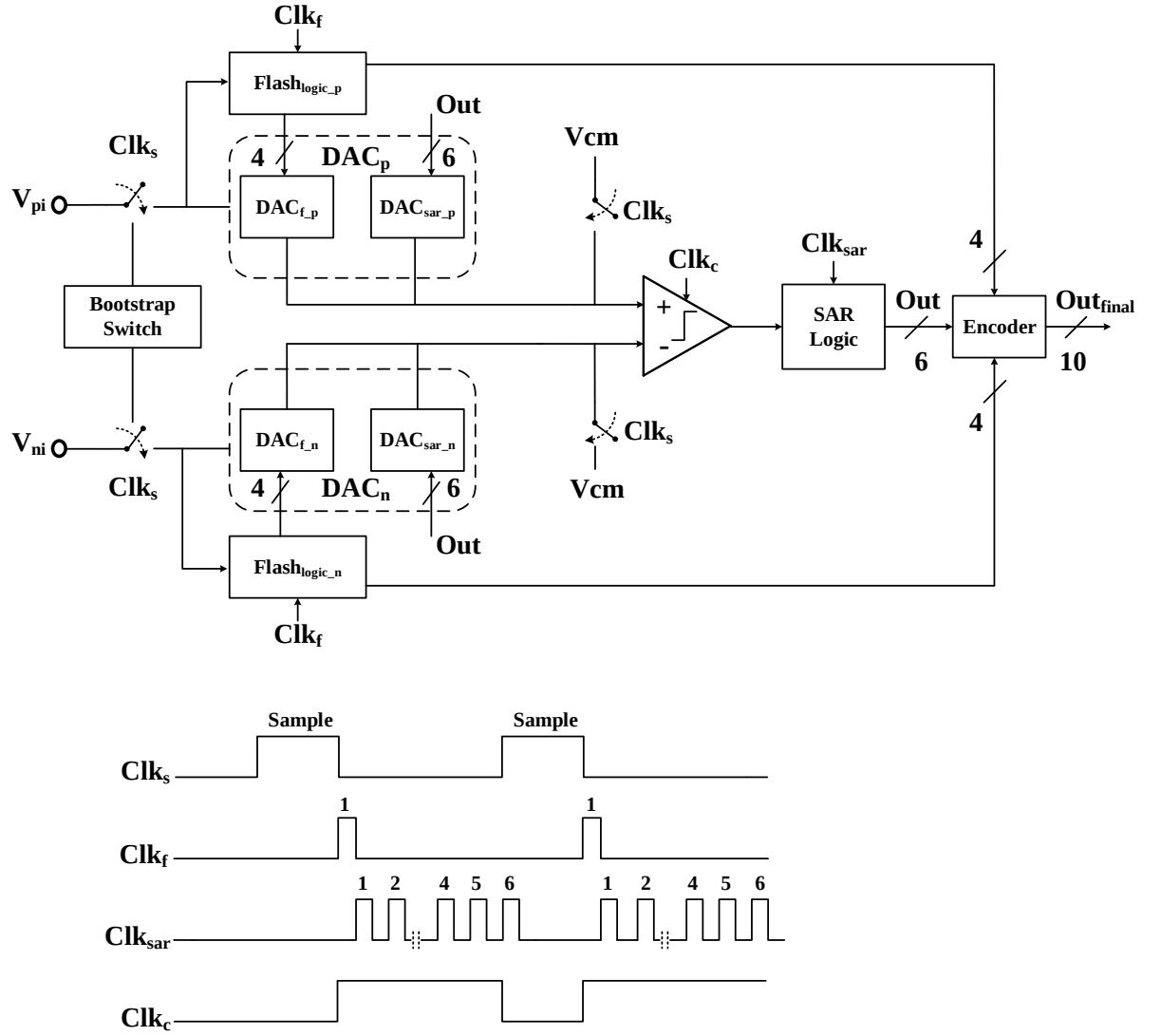


Fig.5.2 Proposed Hybrid flash SAR ADC

The bootstrap switch asserts a nearly constant gate to source voltage throughout the sampling transistor during sampling phase, thereby reducing ON-resistance variation and improving sampling linearity. This enables accurate signal acquisition even under low-voltage operation and high sampling frequencies.

5.2.2 Flash ADC and Vcm-based Switching Technique

The proposed hybrid structure (as shown in Fig. 5.2) divides the conversion process into two stages, in contrast to a conventional SAR ADC, where all 10 bits are resolved sequentially. The upper 4 bits are resolved employing a Flash ADC stage, while the leftover 6 bits are resolved using SAR conversion. This noticeably minimizes the total number of SAR comparison cycles and therefore improves overall conversion speed. The DAC architecture employed in the proposed converter is based on a segmented split-capacitor structure combined with Vcm-based switching. As shown in Fig. 5.3, the DAC is divided into two sections corresponding to Flash and SAR operations. The MSB section associated with the Flash ADC uses larger capacitors to perform coarse quantization, while the SAR section employs smaller capacitors for fine-resolution conversion of the lower 6 bits. The capacitors are arranged in binary-weighted fashion to maintain accurate charge redistribution during successive approximation. Capacitor segmentation significantly reduces total DAC capacitance, switching energy and silicon area in contrast to conventional binary-weighted arrays.

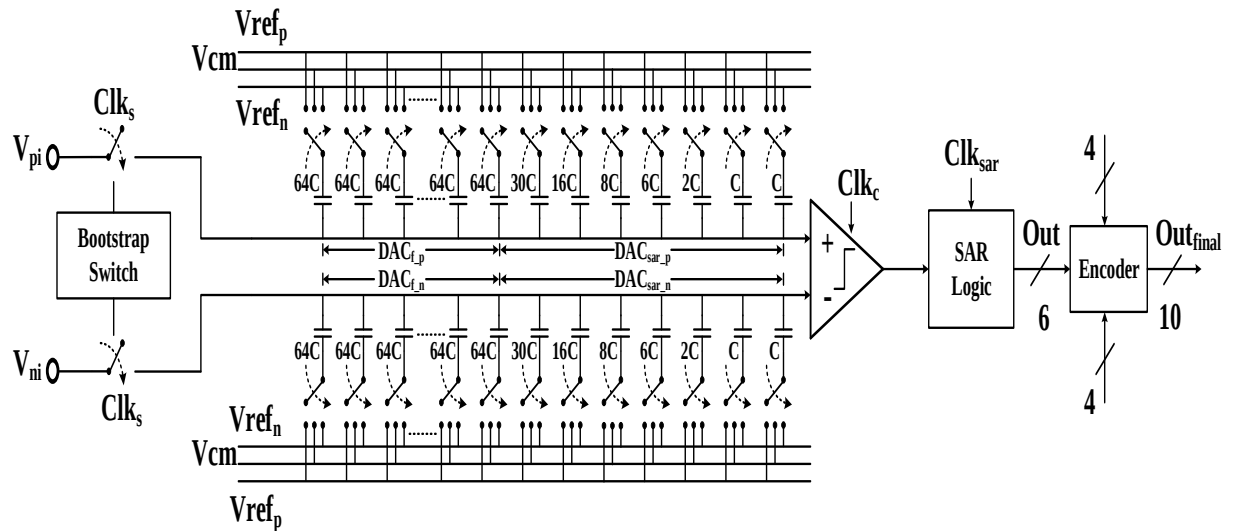


Fig.5.3 Detailed architecture of complete 10-bit ADC

The Flash ADC section comprises of 15 parallel comparators, as shown in Fig. 5.4, which simultaneously compare the sampled input signal against multiple reference levels generated by a local capacitive DAC network [9]. Each comparator produces a decision corresponding to one quantization threshold. The outputs of the Flash comparators collectively configure a thermometer code, which is subsequently altered into a 4-bit binary output using a thermometer-to-binary encoder. Though a single ended version is shown for minimalism, a differential architecture is executed.

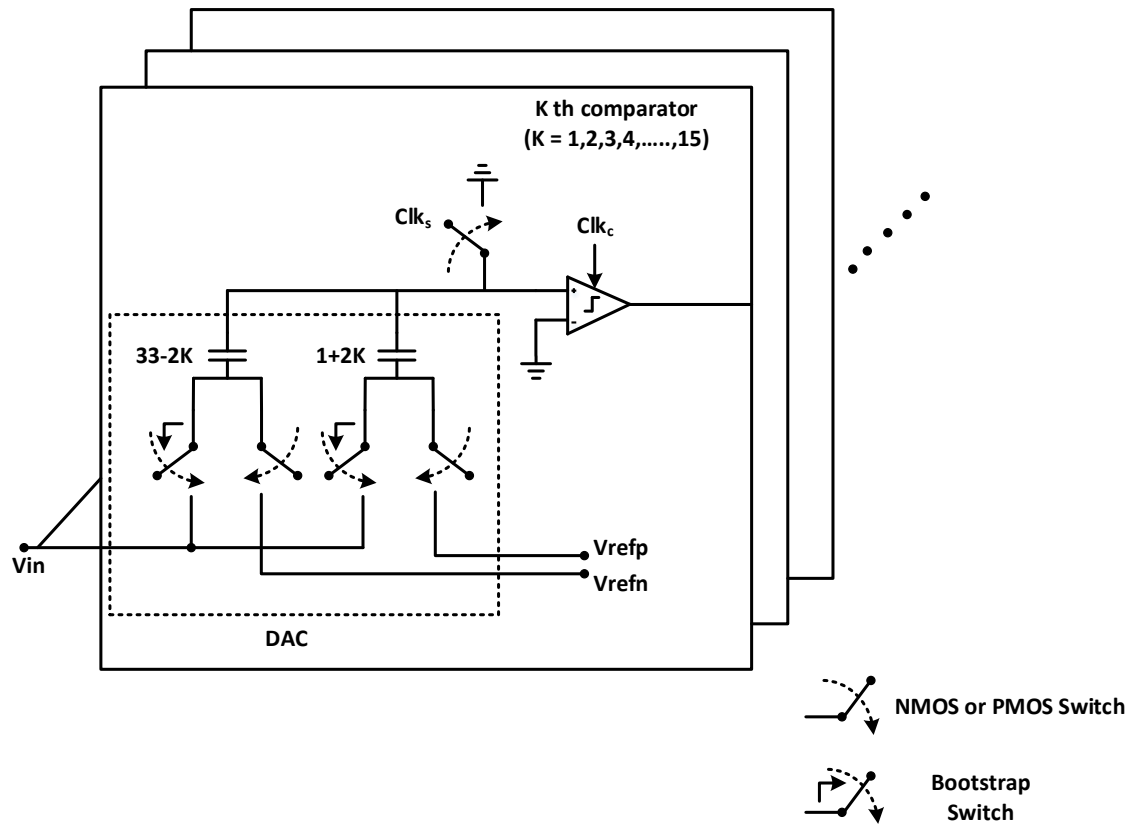


Fig. 5.4 Implementation of 4 bit Flash ADC (a single ended variant is shown for minimalism)

In addition to improve energy efficiency, the proposed DAC uses V_{cm} -based switching methodology. In conventional DAC switching schemes, capacitors switch directly between V_{refp} and V_{refn} , resulting in large voltage transitions and higher dynamic power

consumption. In the proposed structure, an additional common-mode source voltage V_{cm} is added. During initialization, most capacitor bottom plates are connected to V_{cm} , thereby establishing balanced common-mode conditions across the differential DAC outputs. During conversion, only selected capacitors are switched among V_{refp} , V_{cm} and V_{refn} according to the SAR logic decisions. Since many switching operations occur between V_{cm} and one reference level rather than full-scale transitions, the total switching energy is substantially reduced.

The conversion process begins with the sampling phase when Clk_s is enabled. During this interval, the differential input is sampled on top of capacitor arrays through the bootstrap switches. After sampling is completed, the Flash ADC stage is activated using clock Clk_f . The Flash comparators immediately resolve the 4 MSBs through parallel comparison, thereby providing coarse quantization of the input signal. These 4-bit outputs are simultaneously applied to the segmented DAC structure to generate an initial approximation voltage for the SAR stage.

Following Flash conversion, the SAR logic controlled by Clk_{sar} resolves the remaining 6 LSBs using successive approximation. During each SAR cycle, the DAC generates a new voltage based on the comparator decision. The regenerative comparator assimilate the sampled signal with the DAC generated voltage and produces the corresponding decision bit. This process proceeds iteratively till all lower 6 bits are determined. Because the Flash stage already resolves the coarse quantization levels, the SAR stage requires fewer conversion cycles than a conventional 10-bit SAR ADC, thereby improving conversion speed significantly.

A dynamic comparator is used in the proposed structure which operates dynamically. The advantage of using this comparator is that it boosts the overall performance by providing higher transconductance and faster regeneration under low supply voltage conditions. The comparator evaluates the differential voltage between DAC outputs and rapidly regenerates the decision through positive feedback. Dynamic operation eliminates static

current paths during idle conditions, thereby reducing overall power consumption. The timing sequence shown in Fig. 5.2 demonstrates the synchronization among sampling clock Clk_s , Flash clock Clk_f , comparator clock Clk_c and SAR clock Clk_{sar} , ensuring proper coordination between Flash and SAR conversion stages. To operate the comparator at a lower supply voltage of 0.6 V, a reconfigurable switched-capacitor (SC) voltage scaling circuit, as shown in Fig. 5.5, is employed to step down the available 1 V supply [171]. The circuit utilizes flying capacitors and clock-controlled switches to transfer and redistribute charge between capacitors during alternate clock phases, thereby generating a lower output voltage without using inductors. By configuring the capacitive charge-sharing network appropriately, an output voltage of 0.6 V is obtained from the 1 V supply. The generated low-voltage supply is then applied to the comparator, enabling low-power operation while maintaining adequate gain and regenerative performance.

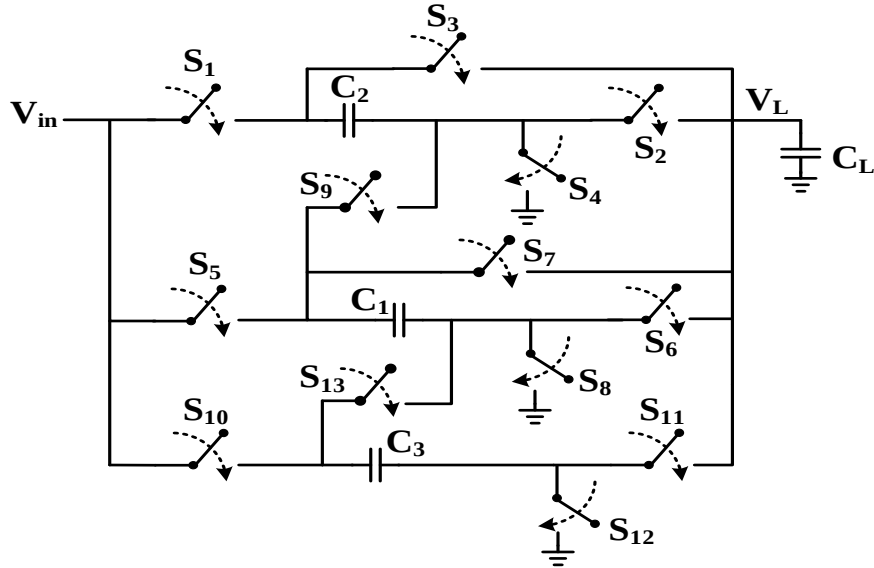


Fig. 5.5 Reconfigurable Switched-Capacitor (SC)

5.2.3 Hybrid Conversion using Encoder and SAR Logic

Figure 5.6 illustrates the output encoder and bit concatenation architecture employed in the hybrid Flash-SAR ADC. The design combines the outputs generated by the flash ADC

and SAR ADC stages to produce the final 10-bit digital output word. The flash ADC generates a thermometer-coded output (C0–C15), which is converted into a 4-bit binary representation (F3–F0) using a thermometer-to-binary encoder. These four bits represent MSBs of the final digital output. Simultaneously, the SAR ADC generates the remaining six LSBs, denoted as S5–S0, through successive approximation conversion.

For reliable concurrence between the coarse flash resolution stage and fine SAR conversion stage, D flip-flops are employed at the outputs of both the encoder and SAR logic blocks. The D flip-flops act as temporary storage and timing synchronization elements, capturing the digital outputs at the active edge of the corresponding clock signals Clk_f and Clk_{sar} . This prevents timing mismatches, reduces the possibility of metastability and ensures stable transfer of data to the output assembly stage. The use of clocked D flip-flops also improves overall timing reliability by aligning the outputs of both conversion stages before final bit concatenation.

The synchronized outputs are then applied to the output assembler block, which performs bit concatenation by combining the 4-bit flash output with the 6-bit SAR output to generate the complete 10-bit digital word $\text{Out}_{\text{final}}$. In the final assembled output, bits D9–D6 correspond to the flash ADC output, while bits D5–D0 are obtained from the SAR ADC stage. This architecture enables efficient integration of coarse flash conversion and fine SAR conversion, thereby achieving high-speed operation while maintaining low power consumption and reduced hardware complexity.

Overall, the proposed methodology integrates high-speed Flash conversion, energy-efficient SAR operation, segmented split-capacitor DAC architecture, V_{cm} -based switching, bootstrap sampling, dynamic comparison and efficient output encoding into a unified hybrid ADC framework. The combined architecture significantly improves conversion speed while reducing switching energy, power dissipation and DAC area. Consequently, the proposed hybrid Flash-SAR ADC provides an effective balance

between speed, resolution, and energy efficiency, making it highly suitable for modern mixed-signal, portable, wireless and high-speed data acquisition applications.

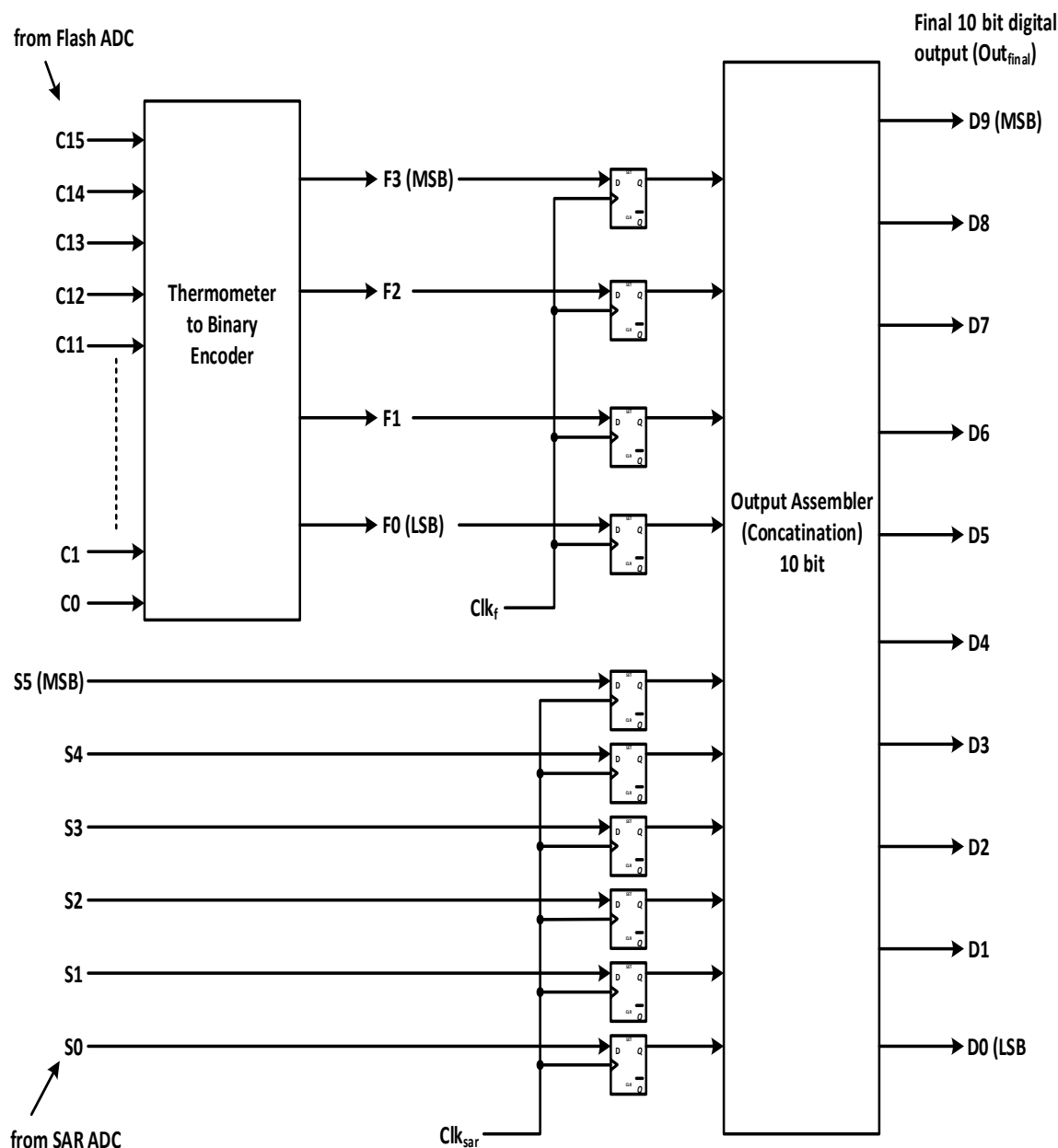


Fig. 5.6 Output Encoder and Bit Concatenation Structure of Proposed Hybrid Flash SAR ADC

The total switching energy in a CDAC of a SAR ADC is fundamentally resolved by the voltage swing and the effective capacitance switched during conversion. For a N-bit SAR ADC, the total energy is expressed as [1]

$$E_{total} = \sum_{i=1}^N C_i * V^2 \quad (5.1)$$

where C_i represents the capacitance switched at bit i and V is the effective voltage transition.

In the hybrid ADC, the conversion process is divided into a 4 bit flash stage and a 6 bit SAR stage. The flash ADC resolves the 4 MSBs; therefore, the flash DAC accuracy requirement corresponds only to the coarse quantization level rather than the full 10-bit resolution. This relaxes matching and settling constraints and reduces switching energy.

The flash ADC resolving MSBs contributes a small additional energy given by

$$E_{flash} \approx (2^4 - 1)V_{refp}^2 C_i \quad (5.2)$$

where V_{refp} is the reference source voltage, C_i the effective switched capacitance per comparator. Because the flash front-end performs coarse quantization with limited resolution, the effective switched capacitance is considerably smaller than that of the SAR capacitive DAC array. The flash comparators consume energy primarily through single-event dynamic charging of internal nodes, whereas the SAR stage repeatedly redistributes charge across the capacitor array during multiple bit decisions. As a result, the accumulated switching energy of the SAR DAC dominates the total conversion energy, while the flash-stage energy contribution remains comparatively small.

The SAR CDAC implements $N_{SAR} = 6$ useful bits. Let the non-binary capacitor weights be

$$C_{NB,i=1 \text{ to } 6} = \{C_{30}, C_{16}, C_8, C_6, C_2, C_1\} \quad (5.3)$$

The total switched capacitance of the SAR array is calculated as [24]

$$C_{total} = \sum_{i=1}^6 C_{NB,i} \quad (5.4)$$

Using V_{cm}–based, monotonic, modified split capacitor DAC scheme, the mean switching energy of the SAR array can be approximated as

$$E_{SAR} \approx \alpha \left[\sum_{i=1}^6 C_{NB,i} \right] V_{refp}^2 \quad (5.5)$$

where $\alpha = 0.38$, an empirical reduction factor capturing V_{cm}–based, monotonic, modified split-capacitor switching technique and is calculated by running transient analysis simulation of one full conversion cycle and recording the capacitor switching events [1,48]. Therefore, the total switching energy for the complete hybrid DAC array is given as

$$E_{total} = E_{flash} + E_{SAR} \quad (5.6)$$

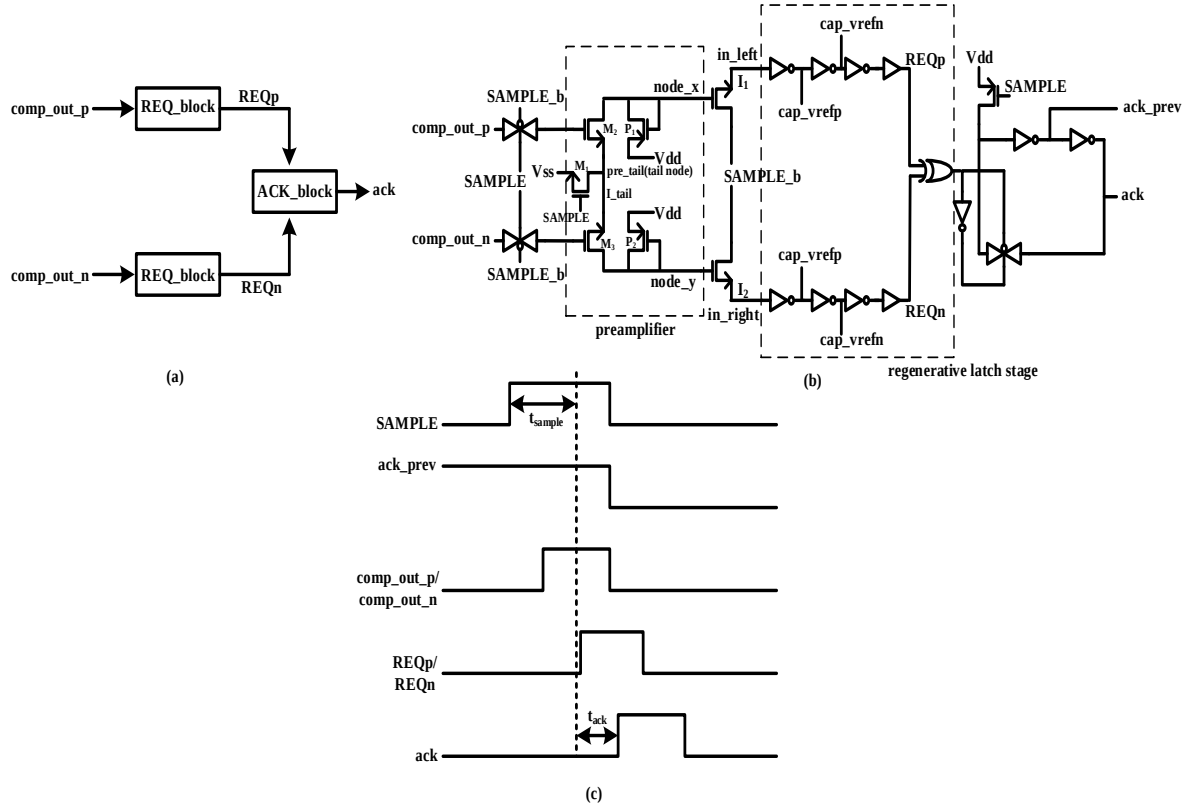


Fig.5.7 Proposed SAR logic (a) Block diagram (b) Schematic and (c) Timing diagram

The proposed hybrid Flash-SAR ADC further incorporates an asynchronous multi-phase SAR logic, as illustrated in Fig. 5.7, to enhance conversion speed and energy efficiency by eliminating the dependence on a global clock. The architecture operates based on event-driven signal propagation, where each bit decision cycle is completed through three sequential phases: pre-amplification, regeneration and asynchronous handshake. This approach enables adaptive timing, ensuring that each transformation step proceeds instantaneously after finishing the former one, thereby avoiding unnecessary idle clock periods and improving overall throughput.

During the pre-amplification phase, the assertion of the SAMPLE signal activates the transmission gates and turns on the tail transistor M1, which establishes the tail current I_{tail} through the differential inputs of the comparator. The differential input voltage ($V_{pi} - V_{ni}$), created by the DAC, is implemented to the comparator inputs, producing a corresponding differential current that develops a small voltage difference between internal nodes $node_x$ and $node_y$. This stage provides initial voltage gain while isolating the input from disturbances caused by latch regeneration. The preamplifier gain determines the magnitude of the developed differential voltage, which can be expressed as

$$\Delta V_{node} \approx A_{v,pre} * (V_{pi} - V_{ni}) \quad (5.7)$$

where $A_{v,pre}$ is the intrinsic gain of preamplifier.

Importantly, the tail current is only active during this phase and is subsequently turned off to reduce static power consumption, thereby improving energy efficiency.

Following a controlled sampling interval, the circuit transitions to the regeneration phase, where the SAMPLE signal is de-asserted, disabling the tail current and effectively freezing the developed differential voltages at the preamplifier output nodes. At this point, isolation switches connect these nodes to a cross-coupled regenerative latch composed of NMOS and PMOS transistors. The latch introduces strong positive feedback, exponentially

amplifying the small differential input voltage to full rail-to-rail logic levels at the internal outputs. The regenerative speed is governed by the latch time constant, which carries inverse relation with the effective transconductance of the latch devices and direct relation with the parasitic capacitance at the internal nodes, expressed as

$$t_{reg} \approx \frac{C_{node}}{g_{m,eq}} \quad (5.8)$$

where C_{node} is the effective capacitance at each latch node and $g_{m,eq}$ is the equivalent transconductance of the cross-coupled NMOS/PMOS devices. This regenerative mechanism ensures rapid and reliable bit resolution even for small input differences.

Once the latch outputs settle, the system enters the asynchronous handshake phase, which replaces conventional clock-driven control with a self-timed signaling mechanism. The resolved latch outputs are buffered to generate request signals REQp and REQn, which are processed by an edge-detection circuit to produce an acknowledgment signal ack. This acknowledgment indicates the completion of the current comparison cycle and triggers the SAR logic to update the DAC configuration for the next bit decision. Simultaneously, the acknowledgment signal resets the internal nodes and prepares the comparator for the subsequent conversion step. The total delay associated with each bit decision is therefore composed of sampling, regeneration, and acknowledgment delays, given by

$$t_{bit} = t_{sample} + t_{reg} + t_{ack} \quad (5.9)$$

where t_{ack} represents acknowledgment propagation delay.

This event-driven asynchronous operation ensures that each bit cycle consumes power only when active, thereby significantly reducing dynamic power consumption compared to synchronous designs that rely on a continuously running clock. Moreover, the absence of a global clock allows the system to operate at a speed determined by actual circuit conditions rather than worst-case timing assumptions, leading to improved efficiency and faster conversion rates. The coordinated interaction between the SAMPLE signal,

regenerative latch outputs, and handshake signals (REQp, REQn, and ack) forms a robust local control loop that enables deterministic, high-speed, and energy-efficient SAR conversion. Consequently, the integration of asynchronous SAR logic with the hybrid Flash-SAR structure plays an important role in achieving the entire performance improvements in the proposed ADC design.

5.3 Results

The performance of the proposed 10-bit hybrid Flash-SAR ADC was validated through detailed post-layout simulations implemented in a 180 nm CMOS technology operating at a 1 V supply voltage, targeting high-speed and energy-efficient conversion. The ADC was excited using a fully differential sinusoidal input with a peak to peak amplitude of 1 V_{pp} centered around a common mode voltage of 0.5 V, ensuring proper utilization of the available signal swing under low-voltage operation. Dynamic performance metrics were extracted using FFT analysis at input frequencies of 1 MHz and 10.2 MHz, with a high sampling rate of 200 MS/s, thereby validating the suitability of the proposed architecture for high speed applications.

All constituent building blocks of the ADC, including the flash front-end, segmented DAC, asynchronous SAR logic, and dynamic comparator, were designed at the transistor level and verified through post-layout extracted simulations in the Cadence Virtuoso environment. The inclusion of parasitic effects in post-layout simulations ensures accurate estimation of real silicon performance, particularly in terms of delay, power consumption, and linearity. In addition, behavioral verification using Spectre and MATLAB co-simulation was performed to validate the functional correctness of the SAR algorithm, DAC switching sequence, and digital output generation under various input conditions.

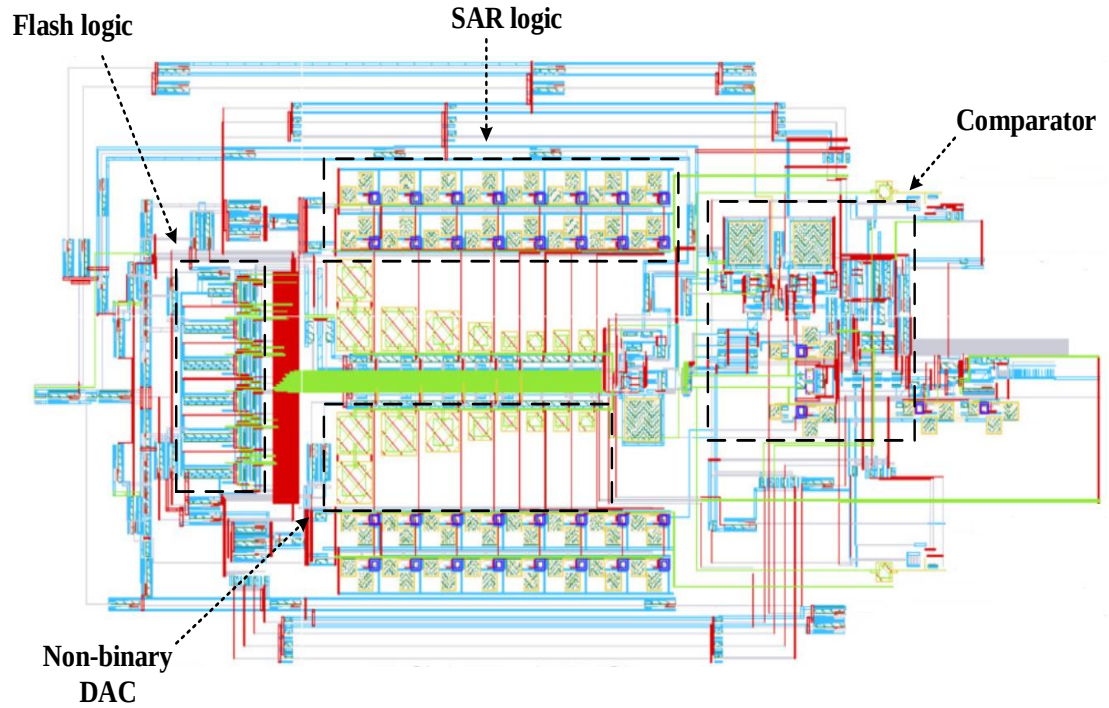
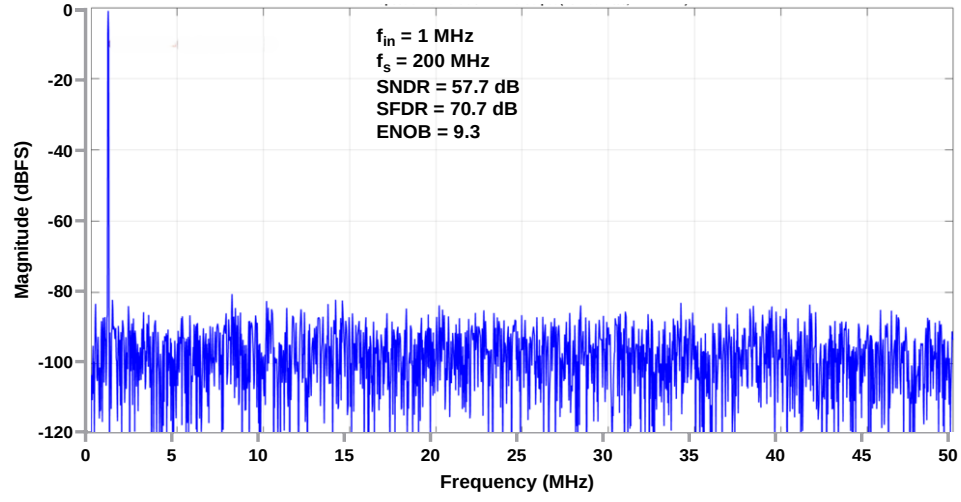
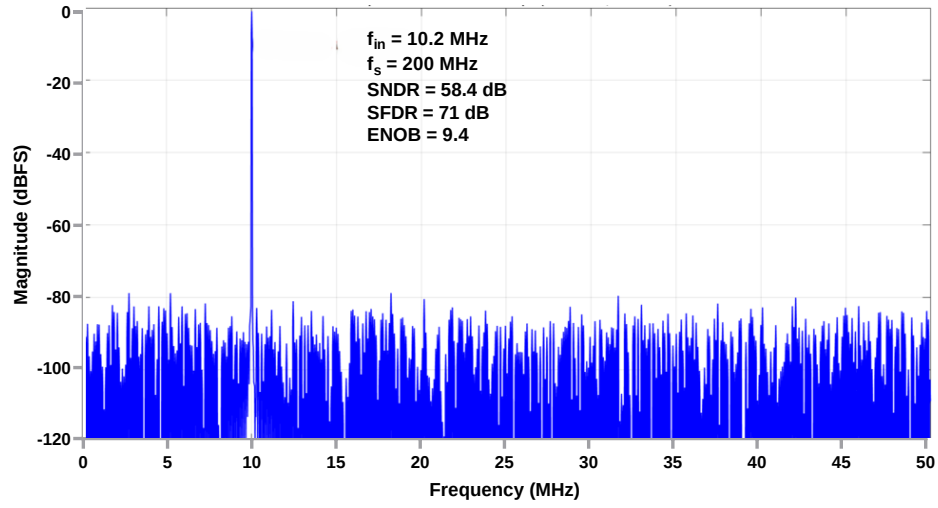


Fig. 5.8 Layout of proposed 10-bit hybrid Flash SAR ADC

The layout of the proposed ADC is shown in Fig. 5.8, with an overall active core area of approximately 0.045 mm^2 , excluding I/O pads. The area is primarily dominated by the capacitive DAC array, which is expected due to its role as the main charge storage and redistribution element in SAR-based architectures. The application of a segmented and non-binary DAC structure significantly decreases the capacitor count compared to conventional binary-weighted implementations, thereby contributing to area efficiency while maintaining high resolution.



(a)



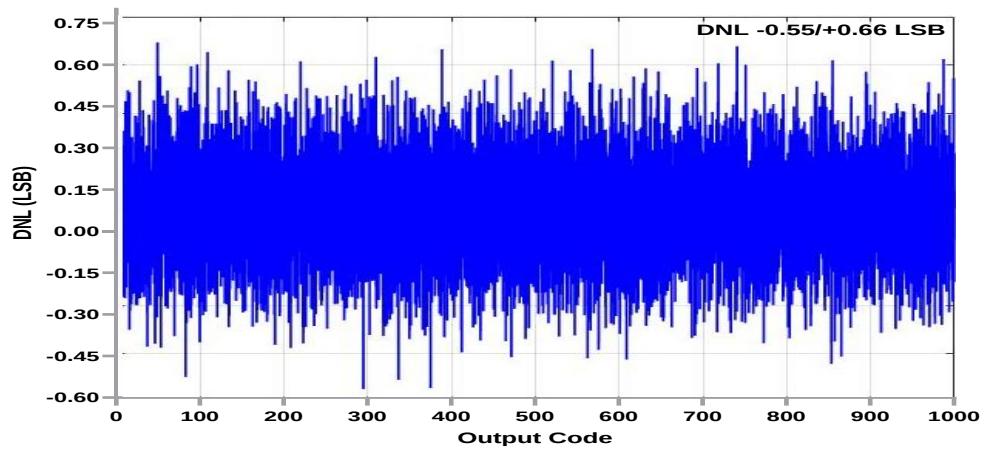
(b)

Fig. 5.9 FFT spectra at event rate of (a) 1 MHz and (b) 10 MHz

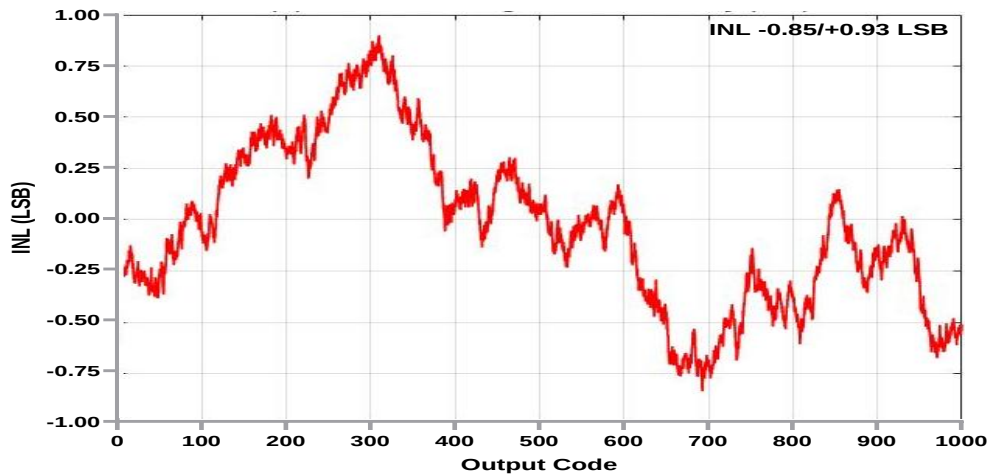
5.3.1 Dynamic Performance Analysis

The dynamic behavior of the proposed hybrid Flash-SAR ADC is further validated through FFT analysis, where the output spectra for frequencies of 1 MHz and 10.2 MHz

at input (as depicted in Fig. 5.9(a) and (b)) exhibit minimal harmonic distortion and negligible spurious tones. The ADC achieves SNDR of 58.4 dB and SFDR of 71 dB, corresponding to ENOB of 9.4 bits. These results demonstrate that the proposed structure maintains high spectral purity and consistent dynamic performance even at high sampling rates, confirming the effectiveness of the hybrid conversion scheme and asynchronous timing in minimizing distortion and noise coupling.



(a)



(b)

Fig. 5.10 Simulated (a) DNL and (b) INL

5.3.2 Static Linearity Analysis

In terms of static behavior, the linearity characteristics of the ADC were evaluated by the results as shown in Fig. 5.10(a) and (b). The DNL is observed to lie within -0.55 to +0.66 LSB, while the INL ranges from -0.85 to +0.93 LSB across the entire output code range. These values remain within acceptable limits of ± 1 LSB and confirm that the proposed ADC maintains good static linearity and satisfies accuracy requirements for high-resolution applications, as compared to the state of art works. The improved linearity can be attributed to the combination of thermometer-coded MSB DAC and optimized non-binary LSB DAC, which together reduce large capacitor switching errors and enhance matching tolerance.

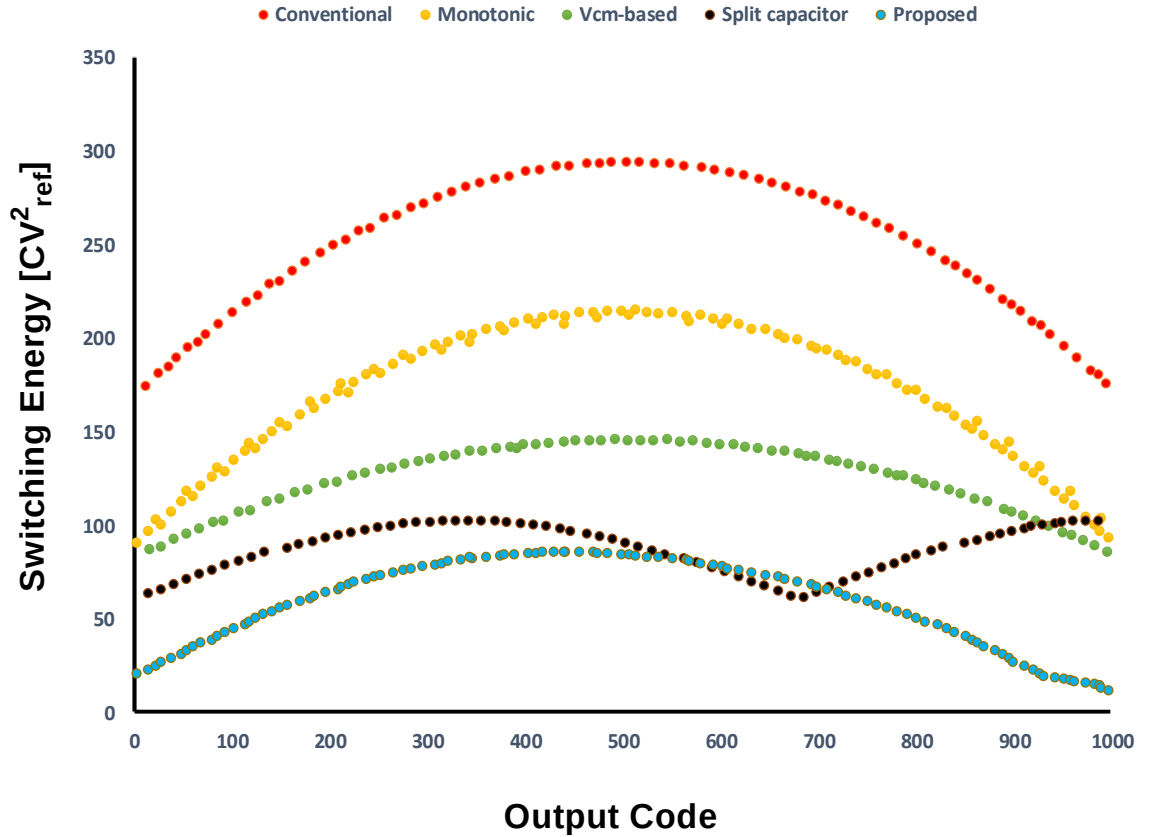


Fig. 5.11 Switching Energy vs Output code

5.3.3 Switching Energy and Power Consumption Analysis

Figure 5.11 presents the switching energy variation with output code for different DAC switching techniques used in SAR ADC architectures. Apart from the proposed switching methodology, the graph compares the energy characteristics of the conventional, monotonic, V_{cm} -based and split capacitor switching schemes. The conventional switching technique exhibits the highest switching energy across almost the entire output code range. This is because large capacitor transitions occur repeatedly between V_{refp} and V_{refn} during successive approximation, resulting in substantial charge redistribution and dynamic power consumption. The V_{cm} -based switching technique significantly reduces switching energy compared to the conventional approach by introducing a common-mode reference voltage V_{cm} . Instead of full-scale voltage transitions between the reference voltages, many capacitor switching operations occur between V_{cm} and either V_{refp} or V_{refn} . This reduction in voltage swing lowers dynamic switching energy and improves common-mode stability. However, despite the improvement, the energy consumption remains relatively high due to the larger number of capacitor transitions involved during the conversion process. The monotonic switching scheme proposed further improves energy efficiency by optimizing the capacitor switching sequence and reducing unnecessary switching activity during bit cycling. Compared to the V_{cm} -based method, this approach achieves lower average switching energy because fewer capacitors undergo large voltage transitions during successive approximation. Nevertheless, the energy still increases near mid-scale output codes due to increased capacitor activity associated with MSB transitions. The split capacitor switching method demonstrates lower switching energy than conventional switching techniques by reducing some redundant capacitor transitions and partially optimizing DAC charge redistribution. However, abrupt energy variations and spikes can be observed in certain output code regions due to non-uniform switching behavior and irregular capacitor transitions.

The switching energy versus output code plot of the proposed scheme confirms a significant average energy reduction of approximately 57.5% compared to conventional

binary-weighted switching schemes. This improvement is primarily achieved through the use of non-binary segmented DAC architecture, which minimizes effective capacitance switching, along with Vcm-based switching, which reduces voltage swing across the capacitors. Additionally, the asynchronous SAR logic eliminates redundant clock-driven switching events, further contributing to reduced energy consumption. Overall, the comparative analysis clearly shows that existing switching methods attempt to reduce DAC switching energy through different charge redistribution strategies, voltage initialization schemes and switching optimizations.

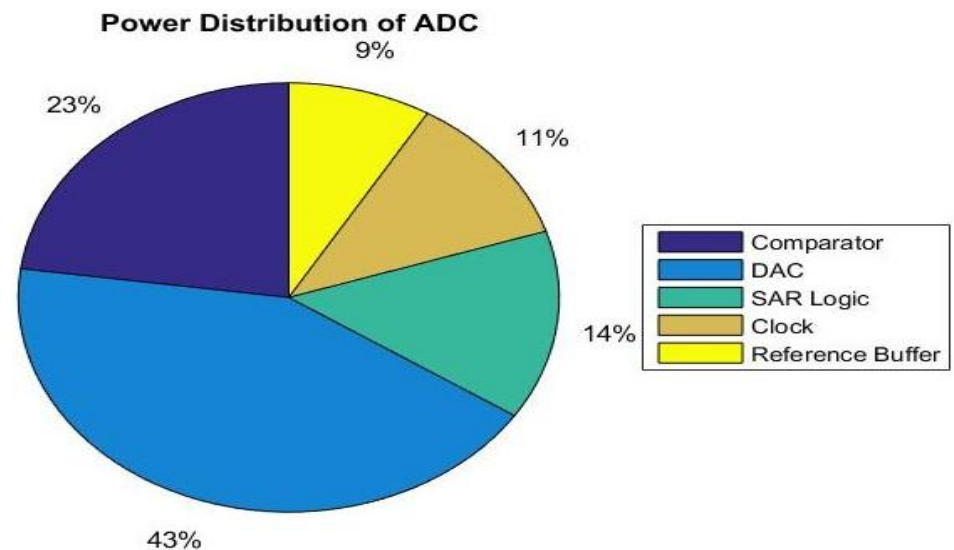


Fig. 5.12 Power Distribution of proposed 10-bit hybrid flash SAR ADC

The power distribution analysis, depicted in Fig. 5.12, reveals that the DAC and comparator together account for nearly 66% of the total power consumption, highlighting their dominant role in determining overall ADC efficiency. The remaining power is consumed by the flash front-end and asynchronous SAR logic, which operate efficiently due to event-driven activation and reduced switching overhead. This balanced power distribution demonstrates that the proposed design effectively optimizes the most power-critical blocks while maintaining high-speed operation.

Table 5.1: Performance comparison of hybrid flash SAR ADC with recent works

Parameter Reference	Architecture	Technology (nm)	Resolution (bits)	Frequency for sampling (MS/s)	Operating Voltage (Volt)	SNDR (dB)	SFDR (dB)	ENoB (bits)	INL(LSB)	DNL (LSB)	Power Consumption(mW)	FoM (fJ/conv. step)	Area (mm ²)
[142]	Flash-SAR	65	10	50	1.2	-	68.81	8.84	0.62	1.63	8.3	-	-
[150]	Flash-SAR	28	6	1000	0.9	35.56	40.81	5.61	-0.75 / +1.10	-0.38 / +0.47	2.33	47.7	-
[167]	Flash-SAR	130	10	32	1	56.7	69.2	9.13	-	-	340	29.7	0.2
[35]	SAR	110	14	5	1.2	-	101.6	12.4	-0.92 / +1.03	-0.30 / +0.50	1.054	14.1	-
[48]	SAR	180	10	80	1.8	56.2	70.6	-	-	-	2.61	-	1.61
[62]	SAR	180	10	0.12	1	58.26	67.4	9.39	0.6	0.77	0.03	36.89	0.13
[79]	SAR	180	10	1	1	57.81	68.63	9.31	0.161	0.152	1525	24.03	0.057
[93]	SAR	180	10	70	1.8	58.26	64.87	9.39	-0.53 / +0.63	-0.6 / +0.6	5.8	123.5	-
[116]	SAR	180	10	100	1	58.58	70.1	9.4	+0.62	+0.45	3.5	31.1	-
Proposed Work	Flash-SAR	180	10	200	1	58.4	71	9.4	-0.85 / +0.93	-0.55 / +0.66	2.3	20.9	0.045

The comparison Table 5.1 presents a performance evaluation of the proposed Hybrid Flash-SAR ADC against previously reported ADC architectures in terms of technology node, resolution, sampling frequency, operating voltage, dynamic performance, linearity, power consumption, FoM and silicon area. From the comparison, it can be observed that the proposed architecture achieves a balanced improvement across multiple performance parameters while maintaining low implementation complexity and energy consumption.

The proposed work is implemented in 180 nm CMOS technology and achieves 10-bit resolution at a sampling frequency of 200 MS/s, which is higher than most of the reported 180 nm SAR ADC implementations listed in the Table. Compared with conventional SAR architectures operating at lower sampling frequencies such as 0.12 MS/s, 1 MS/s, 70 MS/s, and 100 MS/s, the proposed converter demonstrates a substantial increase in conversion speed while preserving conversion accuracy. From a dynamic performance perspective, the proposed ADC achieves an SNDR of 58.4 dB and SFDR of 71 dB, indicating effective suppression of distortion and good spectral purity. The achieved ENOB of 9.4 bits confirms that the converter maintains performance close to ideal 10-bit operation. Compared with previously reported works, the proposed architecture provides competitive SNDR and SFDR values despite operating at a significantly higher sampling frequency. The proposed converter achieves INL within $-0.85/+0.93$ LSB and DNL within $-0.55/+0.66$ LSB, both remaining within the acceptable ± 1 LSB limit for monotonic ADC operation. These results indicate that the proposed segmented DAC architecture and switching methodology maintain accurate code transitions and minimize conversion errors. Power consumption analysis also shows that the proposed architecture dissipates only 2.3 mW, which is considerably lower than several earlier implementations despite achieving higher conversion speed. The FoM further confirms the energy efficiency of the proposed design achieved is 20.9 fJ/conversion-step and is lower than several existing architectures reporting FoM values of 47.7 fJ/conversion-step, 36.89 fJ/conversion-step, 31.1 fJ/conversion-step, and 123.5 fJ/conversion-step, demonstrating improved energy utilization per conversion operation.

Overall, the combined dynamic, static, and energy performance results confirm that the proposed hybrid Flash-SAR ADC achieves an excellent trade-off among high sampling speed, low power consumption, reduced switching energy, and high linearity, making it a highly efficient solution for next-generation high-speed and energy-constrained mixed-signal applications.

5.4 Summary

The complete evaluation of the proposed hybrid Flash-SAR ADC clearly demonstrates that the co-optimization of architecture, DAC switching strategy, comparator design, and control logic leads to a significant improvement in speed–power–accuracy trade-offs compared to conventional ADC implementations. The hybrid partitioning of the conversion process into a flash-based coarse stage (4 MSBs) and a SAR-based fine stage (6 LSBs) effectively addresses the fundamental limitation of sequential SAR conversion. By resolving the most significant bits in a single cycle using the flash front-end, the overall conversion latency is substantially reduced, while the SAR stage ensures energy-efficient fine quantization. This architectural synergy enables high sampling rates without incurring the exponential power and area penalty typically associated with full flash ADCs.

A key contributor to the improved energy efficiency is the implementation of a non-binary segmented DAC combined with V_{cm} -based switching. Unlike conventional binary-weighted DACs, which require large capacitor arrays and result in significant switching energy, the proposed segmentation strategy reduces the effective capacitance and relaxes matching constraints. The use of thermometer coding for MSBs minimizes glitch energy and mismatch-induced errors, while the non-binary LSB DAC reduces switching activity and improves tolerance to parasitic capacitances. The observed reduction of approximately 57.5% in switching energy confirms the effectiveness of this approach. Additionally, initializing DAC operation around the common-mode voltage reduces voltage swing, which not only lowers dynamic power consumption but also improves settling behavior and reduces comparator kickback noise.

The incorporation of asynchronous SAR logic represents another significant advancement in the proposed design. Unlike conventional synchronous SAR architectures that rely on a fixed clock period determined by worst-case delay, the asynchronous approach enables event-driven conversion, where each bit decision is triggered immediately upon completion of the previous operation. This eliminates unnecessary waiting time, reduces

idle power consumption and allows the ADC to operate at a speed determined by actual circuit conditions. The handshake-based control mechanism ensures reliable operation while maintaining deterministic timing, thereby improving both speed and energy efficiency. However, this approach introduces additional design complexity in terms of handshake signal generation and synchronization, which must be carefully managed to avoid timing hazards and metastability issues. It is also to be emphasized in case of extreme PVT variations that the propagation delay of digital logic and regeneration time of comparator are mainly affected. In asynchronous SAR ADC, each comparison automatically triggers the subsequent conversion only after the previous comparison has completed. Therefore, unlike synchronous SAR ADC that rely on a fixed clock period, the asynchronous one inherently adapts to delay variations caused by PVT changes. Under slow process corners or low supply voltages, the conversion time increases slightly, whereas under fast process corners, the conversion time decreases accordingly. Therefore, asynchronous control logic improves timing robustness and minimizes timing violations across a wide range of operating conditions.

The dynamic comparator further enhances the overall performance by providing higher transconductance and faster regeneration under low supply voltage conditions. The improved comparator speed directly contributes to reduced decision time per bit, which is critical in achieving the high sampling rate of 200 MS/s. Moreover, the reduced kickback noise and improved sensitivity of the comparator support better accuracy and linearity, as reflected in the measured INL and DNL values. The fact that linearity metrics remain within ± 1 LSB despite aggressive optimization of speed and energy indicates that the proposed architecture successfully balances performance without compromising precision.

From a system-level perspective, the power distribution analysis indicates that the DAC and comparator dominate total power consumption, accounting for approximately 66% of the overall power. This highlights that further improvements in ADC efficiency would primarily depend on optimizing these two blocks. The flash front-end, although

contributing additional power due to parallel comparators, remains efficient because it operates only for coarse quantization. Similarly, the asynchronous SAR logic contributes relatively less power due to its event-driven operation, validating its applicability for energy efficient and high speed designs.

The robustness of the proposed ADC across temperature variations further confirms its practical viability. Minimal degradation in SNDR and ENOB indicates that the combined effects of non-binary DAC, asynchronous control, and comparator provide stable operation under PVT variations. This robustness is particularly important for real-world applications such as wireless communication and sensor interfaces, where environmental conditions can vary significantly.

Despite the demonstrated advantages, certain trade-offs must be acknowledged. The integration of multiple advanced techniques—such as hybrid architecture, non-binary segmentation, and asynchronous control—introduces increased design complexity and verification effort. Careful layout design is required to manage parasitic effects in the DAC, and precise timing coordination is essential in asynchronous logic to ensure correct operation. Additionally, the flash front-end, while improving speed, introduces comparator offset considerations that may require calibration in higher-resolution implementations.

In conclusion, the proposed hybrid Flash-SAR ADC successfully overcomes the limitations of conventional architectures by combining parallel coarse conversion, energy-efficient fine quantization, and adaptive timing control. The achieved performance—characterized by high sampling rate, low energy consumption, good linearity, and strong robustness—demonstrates that the proposed design provides an effective solution for next-generation high-speed, low-power mixed-signal systems, specifically in applications such as wireless transceivers, imaging systems and high-performance data acquisition platforms.

Chapter 6

Conclusions, Future Directions and Social Impact

This chapter presents the overall conclusions drawn from the research work carried out in this thesis and discusses possible future extensions and broader societal impact of the proposed techniques. The research focused on improving the performance of SAR ADCs through innovations at both circuit and architectural levels. The primary objective was to achieve low power consumption, improved conversion speed, enhanced energy efficiency and reliable operation under modern CMOS technology constraints while maintaining acceptable conversion accuracy. A major contribution of this thesis is the development and evaluation of multiple comparator architectures aimed at improving speed and energy efficiency. Another important contribution of this work is the development of a low-power SAR ADC architecture incorporating energy-efficient DAC design techniques. To further overcome speed limitations associated with traditional SAR conversion, a Hybrid Flash-SAR ADC architecture was proposed and implemented. Comprehensive simulation-based validation was performed to evaluate the effectiveness of the proposed architectures. The results confirmed that the proposed techniques collectively contribute toward improving speed, reducing switching losses, lowering energy consumption and enhancing overall converter performance.

6.1 Conclusions

This thesis presents a comprehensive investigation into the design and optimization of energy efficient, high-speed SAR and hybrid ADC architectures, with a particular focus on comparator innovation, DAC switching techniques, SAR logic and system-level enhancements. The work systematically addresses key limitations of conventional ADC designs through circuit-level and architectural advancements, resulting in improved performance across multiple metrics including delay, power consumption, energy efficiency, linearity, and robustness.

In Chapter 2, prior work on advanced mixed-signal circuit techniques relevant to SAR ADC design is systematically reviewed to establish the foundation for the proposed architectures. The chapter examines key gain enhancement methods such as self-cascode and DTMOS techniques, highlighting their role in improving transconductance and enabling low-voltage operation. Various latch structures, including cross-coupled regenerative latches, shared-charge reset mechanisms, and auxiliary inverter-based designs, were analyzed in terms of regeneration speed, energy efficiency, and stability, along with the limitations of conventional comparator architectures. The study further explores capacitive DAC techniques, including binary-weighted arrays, monotonic switching, Vcm-based switching and split-capacitor structures, emphasizing their impact on switching energy, area, and complexity. Additionally, SAR logic and control strategies, such as sequential logic, binary search algorithms, and asynchronous control techniques, are discussed with respect to speed and power optimization. The chapter concludes with a comparative analysis of these approaches in terms of power, delay, area, and design complexity, leading to key observations and identification of research gaps that motivate the proposed innovations in subsequent chapters.

In Chapter 3, a set of six novel comparator architectures (PC1–PC6) were developed using progressive design techniques such as self-cascode technique which increases gain, shared-charge logic, auxiliary inverter-assisted regeneration and DTMOS-based operation. In particular, the DTMOS approach plays a crucial role in enabling ultra-low-voltage operation. The results demonstrate that increasing preamplifier gain and improving latch regeneration significantly reduces comparator delay while enhancing sensitivity. Among the proposed designs, dynamic latch-based comparators, particularly PC2, PC4 and PC6, achieved superior performance in terms of energy-delay trade-off, while static latch configurations offered better robustness and simpler timing. Overall, the DTMOS-based comparators effectively overcome threshold voltage limitations in scaled CMOS technologies, enabling reliable, high-speed, and energy-efficient operation at reduced supply voltages.

Chapter 4 introduced a low-power SAR ADC architecture employing an optimized DAC switching strategy based on V_{cm} -assisted switching, monotonic charge redistribution, and capacitor splitting techniques. The proposed approach significantly reduced DAC switching energy while maintaining high linearity and accuracy. The ADC achieved excellent performance metrics, including low power consumption, FoM and acceptable INL/DNL characteristics, demonstrating its suitability for energy-constrained applications.

In Chapter 5, a hybrid Flash-SAR ADC architecture was proposed to overcome the speed limitations of conventional SAR ADCs. By integrating a flash front-end for coarse conversion with a SAR-based fine conversion stage, along with a non-binary segmented DAC and asynchronous SAR logic, the proposed design achieved high sampling rates while maintaining energy efficiency. The use of asynchronous control eliminated unnecessary clock overhead, while the comparator and optimized DAC switching further enhanced performance. The results confirmed that the hybrid architecture achieves a favorable balance among speed, power and resolution, making it suitable for high-performance data conversion systems.

Overall, the thesis establishes that co-design of comparator, DAC SAR logic is crucial for getting an optimized ADC performance. The proposed techniques successfully address the trade-offs inherent in conventional designs and provide scalable solutions for low-voltage, high-speed and energy-efficient mixed-signal systems.

6.2 Future Directions

The proposed comparator architectures and low-power ADC systems establish a foundation for further advancements in energy-efficient mixed-signal integrated circuit design. Although the developed architectures demonstrate improvements in conversion speed, switching energy and power efficiency, several opportunities remain for extending

their performance and applicability in future electronic systems. The following research directions can be explored:

1. Migration to advanced CMOS technology nodes

Future work can focus on implementing the proposed comparator and ADC architectures in advanced CMOS technologies such as 65 nm, 45 nm, 28 nm, and FinFET-based processes. Technology scaling can provide improvements in speed, area efficiency, and dynamic power reduction. However, challenges associated with lower supply voltages, leakage currents, process variation and device mismatch must be addressed through adaptive analog design techniques.

2. Ultra low power ADC design for energy constrained systems

Further optimization can target sub-threshold and near-threshold circuit operation to enable ADC functionality under extremely limited energy budgets. Such architectures may support battery-less devices, energy harvesting systems, wireless sensor nodes, and long-lifetime IoT platforms, where minimizing energy per conversion becomes a primary objective.

3. Intelligent calibration and digital assistance techniques

Future research can integrate digital background calibration, adaptive offset correction and self-calibration algorithms to compensate for comparator offset, capacitor mismatch and process variations. The use of digital assistance can improve linearity, increase robustness and maintain converter accuracy under varying operating conditions.

4. AI-assisted mixed signal design optimization

Artificial intelligence and machine learning techniques can be incorporated to automate transistor sizing, comparator optimization, switching sequence selection and power-performance trade-off analysis. AI-driven optimization may significantly reduce design complexity and accelerate development of high-performance ADC architectures.

5. High speed time-interleaved hybrid ADC architectures

The proposed Hybrid Flash-SAR structure can be extended into time-interleaved conversion systems to achieve multi-channel operation and significantly higher effective sampling rates. Future studies may investigate timing synchronization, channel mismatch calibration and digital correction methods for ultra-high speed applications.

6. Advanced DAC switching and capacitor reduction techniques

Additional improvements can be achieved by developing adaptive switching algorithms, capacitor compression methods, and charge-recycling architectures to further minimize DAC switching energy and silicon area. These techniques can improve overall ADC FoM while preserving conversion accuracy.

7. Fully asynchronous and event-driven ADC architectures

Future implementations may explore clock-independent conversion mechanisms that activate circuit blocks only when required. Such asynchronous architectures can reduce unnecessary switching activity and improve energy efficiency for variable-rate sensing applications.

8. Hardware fabrication and experimental validation

The proposed architectures can be extended beyond simulation through post-layout verification, fabrication and silicon measurement. Experimental validation will provide insight into parasitic effects, process variation, reliability and real-world performance under practical operating environments.

9. Integration with smart sensing and edge computing systems

Future ADC systems can be co-designed with edge processing units, embedded intelligence and adaptive sensing platforms to support real-time data acquisition with reduced communication overhead and improved energy utilization.

10. Sustainable and green electronics design

Future research may investigate energy-aware circuit methodologies, adaptive power management, and environmentally sustainable semiconductor design approaches to support long-term development of low-power electronic systems.

Overall, these future directions provide opportunities to extend the proposed work toward next-generation ADC systems that offer higher speed, lower power consumption, improved scalability and enhanced compatibility with emerging intelligent and sustainable electronic applications.

6.3 Social Impact

The proposed research on low-power comparator architectures and energy-efficient ADC systems supports multiple Sustainable Development Goals (SDGs) through advancements in sustainable electronic design and intelligent data conversion. By reducing power consumption and improving energy utilization, the proposed architectures contribute to SDG 7 (Affordable and Clean Energy) through the development of energy-efficient electronic systems. Their application in wearable devices, biomedical monitoring, and healthcare instrumentation supports SDG 3 (Good Health and Well-being) by enabling reliable and long-duration operation of medical sensing platforms. The proposed Hybrid Flash-SAR ADC and optimized mixed-signal architectures also align with SDG 9 (Industry, Innovation and Infrastructure) by promoting advanced semiconductor technologies and efficient digital infrastructure. Furthermore, the deployment of low-power sensing systems in smart monitoring applications contributes to SDG 11 (Sustainable Cities and Communities), while reduced energy demand and improved circuit efficiency indirectly support SDG 12 (Responsible Consumption and Production) and SDG 13 (Climate Action) by lowering resource utilization and environmental impact. Overall, the proposed work contributes toward the development of sustainable, energy-aware and scalable electronic systems for future technological applications.

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