

COMPARATIVE ANALYSIS OF VOLTAGE-MODE SENSE AMPLIFIERS WITH MODIFIED DECAP-ASSISTED PRECHARGE TECHNIQUE

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IN

VLSI DESIGN AND EMBEDDED SYSTEM

SUBMITTED

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I, **Mithun**, Roll No. **2K24/VLS/19** student of **M. Tech (VLSI Design & Embedded systems)**, hereby declare that the project Dissertation titled “**Comparative Analysis of Voltage-Mode Sense Amplifiers with Modified Decap-Assisted Pre-charge Technique**” which is submitted by me to the Department of **Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **2024** to **2026** under the supervision of **Prof. Poornima Mittal**.

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COMPARATIVE ANALYSIS OF VOLTAGE-MODE SENSE AMPLIFIERS WITH MODIFIED DECAP- ASSISTED PRECHARGE TECHNIQUE

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ABSTRACT

Static Random Access Memory (SRAM) is one of the most important memory components used in modern digital systems such as microprocessors, cache memory, mobile devices and embedded applications because of its high speed, low latency and reliable performance. During the read operation of SRAM a very small voltage difference is generated between the bit-lines. This small signal cannot be directly detected by digital circuits. therefore, a sense amplifier is required to sense and amplify the signal into a full logic level. The performance of the sense amplifier plays a significant role in determining the speed, power consumption, stability and reliability of the SRAM system. As CMOS technology continues to scale down, designing an efficient sense amplifier becomes more challenging due to reduced sensing margin, increased leakage current, process variations and higher bit-line capacitance.

Several voltage-mode sense amplifiers such as Cross-Coupled Voltage Sense Amplifier (CCVSA), Latch-Type Sense Amplifier (LTSA), Transmission-Gate Sense Amplifier (TGSA), Parallel Latch-Type Sense Amplifier (PLTSA) and Decoupled Inverter Pair Sense Amplifier (DIPSA) have been proposed in previous research works. Each architecture provides different advantages and limitations in terms of delay, power consumption and stability. Some designs offer high sensing speed but consume more power while others provide low power consumption at the cost of increased delay. Therefore, there is a need for a sense amplifier that can achieve a better balance between speed, power efficiency and stable operation under different operating conditions.

In this work, a Modified Decap-Assisted Sense Amplifier (MDASA) is proposed to improve sensing performance in SRAM applications. The proposed architecture uses decoupling capacitors and parallel transistor paths to provide additional charge support to the bit-lines and improve drive strength during sensing operation. Initially the decoupling capacitors are charged using control signals and during sensing the stored charge is transferred to the bit-lines to provide an initial voltage boost. A cross-coupled positive feedback structure is used to amplify the small voltage difference rapidly and generate a stable digital output. The use of parallel transistor paths further enhances sensing speed and reduces sensitivity to bit-line capacitance variations.

The proposed MDASA and other conventional sense amplifiers are simulated using LTspice in 45 nm CMOS technology under uniform operating conditions. The supply voltage is varied from 0.7 V to 1.2 V and bit-line capacitance is varied from 50 fF to 250 fF. Performance analysis is carried out based on important parameters such as delay, power consumption, leakage current and Power-Delay Product (PDP).

The proposed MDASA achieves simulation results that show the lowest delay among all compared sense amplifiers indicating the fastest sensing performance. The design also shows an improved Power-Delay Product which represents better energy efficiency. Although CCVSA provides the lowest power consumption and leakage current, MDASA achieves a better overall trade-off between speed, power and stability. The proposed architecture also demonstrates stable operation under varying supply voltages and bit-line capacitance conditions. Therefore, the proposed MDASA is highly suitable for high-speed and energy-efficient SRAM applications in modern VLSI systems.



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MTech: VLSI Design and Embedded System

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LIST OF SYMBOLS, ABBREVIATIONS AND NOMENCLATURE

Abbreviation/Symbol	Description
SRAM	Static Random Access Memory
WL	Word Line
BL	Bit Line
BLB	Bit Line Bar
CCVSA	Cross Coupled Voltage Sense Amplifier
LTSA	Latch Type Sense Amplifier
PLTSA	Parallel Latch Type Sense Amplifier
MDASA	Modified Decap-Assisted Sense Amplifier
DIPSA	Decoupled Inverter Pair Sense Amplifier
TGSA	Transmission Gate Sense Amplifier
CTRL1	ControlSignal 1
CTRL2	ControlSignal 2
SE	Sense Enable
CTRL	Control Signal
VPC	Pre-charge signal
PDP	Power-Delay Product

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CHAPTER - 1

INTRODUCTION

This chapter gives an overview of SRAM sense amplifiers and their significance in modern VLSI designs. The chapter discusses various issues involved in SRAM reading processes, including low sensing margin, higher leakage current, increased bit-line capacitance, and process variations in scaled CMOS technology. This chapter also explains different types of voltage mode sense amplifiers, like CCVSA, LTSA, TGSA, PLTSA, and DIPSA, along with their drawbacks in terms of time delay, power dissipation, and sensing capability. Further, the modified Decap-assisted sense amplifier (MDASA) has been introduced as a solution to enhance sensing performance, energy efficiency, and stability for SRAM memories. A sense amplifier is an essential component in memory architectures that senses the voltage difference and amplifies this difference to make full logic levels. As only a voltage difference appears on the bit-lines during the reading process of memory cells, this voltage difference can't be sensed by the digital circuits. Thus, it is necessary to use a sense amplifier to sense and amplify this small voltage difference effectively and quickly.

Static Random Access Memory (SRAM) finds application in many areas such as processors, cache memory, communication systems, and personal electronic devices due to their high speed and lower access time. A very small voltage difference is generated on the bit lines during the reading process in SRAM; therefore, sensing of this small signal must be done accurately. The sensing margin becomes very small, leakage current, and bit-line capacitance become larger with scaling down of CMOS technology. Larger bit-line capacitance results in higher sensing delay and power consumption and makes the SRAM performance slower and not energy efficient. Hence, there is an increased need for designing an improved sense amplifier that will enable faster sensing, less power consumption, and stable performance. A Modified Decap-Assisted Sense Amplifier (MDASA) architecture is designed and proposed to solve the above problems.

Different sections have been considered for this chapter. Section 1.1 highlights the motivation for carrying out the proposed study along with the necessity for an effective design of the sense amplifier. Objectives of the research have been highlighted in section 1.2. Section 1.3 discusses the methodology adopted to conduct performance analysis of the various sense amplifiers. The rest of the chapters of this thesis focus on the proposed architecture, simulation, performance analysis, comparison, and conclusion of the proposed study.

1.1 Motivation

As per continuous scaling down of the CMOS technology, it has become very difficult to implement a suitable sense amplifier in the case of SRAM cells in VLSI circuits. When the process of reading takes place in the SRAM cell, the difference between the voltages on the bit lines is extremely small. This phenomenon becomes

more critical with lowering supply voltage and this leads to slowing down of sensing and instability in sensing process. Moreover, there is a high bit line capacitance and leakage current. All these phenomena degrade the performance of SRAM cell in terms of power dissipation, delay, stability and reliability. A number of different voltage-mode sense amplifiers such as CCVSA, LTSA, TGSA, PLTSA and DIPSA have already been introduced. However, these sense amplifiers suffer from certain limitations. The sense amplifiers designed by certain authors offer fast sensing but consume high power. Whereas others sense amplifiers consume low power but exhibit slow operating speed and high delay. The main aim of this paper is to design an optimal sense amplifier that could offer a fast sense amplification process while consuming low power. Therefore, a novel approach of Modified Decap-assisted Sense Amplifier is suggested here.

1.2 Objective

Designing and analyzing of a suitable voltage-mode sense amplifier for SRAM application is the aim of this thesis. In this proposed thesis, the aim will be to achieve fast sensing operation, reduction in power consumption, as well as obtaining reliable operational characteristics. Some of the objectives which form the aims of this work are presented below. Analyze different voltage-mode sense amplifier structures like CCVSA, LTSA, TGSA, PLTSA, DIPSA based on delay, power consumption, leakage current, and sensing stability. Design a Modified Decap-Assisted Sense Amplifier (MDASA) with the use of decoupling capacitors and parallel transistor paths in order to boost the sensing speed and also to provide reduced sensitivity to changes in bit-line capacitance. Analyze the performance of the proposed MDASA structure against other sense amplifier structures under various values of supply voltage and bit-line capacitance using LTspice in 45nm CMOS technology by analyzing parameters like delay, power consumption, and Power-Delay Product (PDP).

1.3 Methodology

Different types of voltage mode sense amplifiers like CCVSA, LTSA, TGSA, PLTSA, DIPSA and the Proposed MDASA have been designed and investigated in this paper for use in SRAM memory designs. In the Proposed MDASA architecture, the use of decoupling capacitors and parallel transistor paths makes the sense amplifier faster and more stable. All the circuits are designed and simulated in the 45 nm CMOS technology by using LTSpice. The performance characteristics of all the sense amplifiers have been tested in similar operational environments so that a comparison between them may be made. Varying the power supply from 0.7 V to 1.2 V and the bit line capacitance from 50 fF to 250 fF, different sense amplifier performances concerning different performance metrics such as sensing time, energy requirement, leakage phenomenon and Power-Delay Product (PDP) are investigated.

1.4 Report Organization

The dissertation report is organized into six chapters. The first chapter consists of the introduction, motivation, objectives, methodology and an overall overview of the research work. The second chapter includes the review of literature on the sense amplifier circuit architectures that have been previously reported and mentions the gaps in the current designs. The third chapter includes the discussion about working principle and comparative performance of various conventional voltage-mode sense amplifiers. The fourth chapter elaborates on the proposed Modified Decap-Assisted Sense Amplifier (MDASA). This chapter gives details about the architecture of MDASA, working principle, advantages and applications. Chapter 5 shows the simulation results of the proposed sense amplifier in different conditions. Chapter 6 give conclusion and idea of future scope of modified Decap-Assisted Sense Amplifier.

CHAPTER 1 – This Chapter describes the introduction of SRAM memory, the use of sense amplifier in modern VLSI circuitry and the problem and objectives involved in the study to be undertaken.

CHAPTER 2 – This Chapter deals with the basic terminology relating to CMOS technology, the concept of SRAM memory and the working principles of sense amplifiers.

CHAPTER 3 – This Chapter focus on various conventional voltage mode sense amplifiers including LTSA, DIPSA, CCVSA, TGSA and PLTSA. Their performances in respect of delay, power consumption, leakage current and Power-Delay Product (PDP) are discussed here.

CHAPTER 4 – This Chapter describes the proposed Modified Decap-Assisted Sense Amplifier (MDASA). The basic idea of circuit design along with its working principles, benefits, application and other notable features are included here.

CHAPTER 5 –This Chapter discusses the simulation process of the proposed MDASA sense amplifier. Performances of the MDASA in comparison with conventional sense amplifiers are analyzed here in respect of delay, power consumption, leakage current and PDP.

CHAPTER 6 – This Chapter provides a brief conclusion of the research work along with important findings and suggestions for further improvements.

Finally, the list of publications contingent to the work carried out in this report is attached. Afterword, the detailed list of references is presented which is used to refer and site the previous research work to explore the directions for our present work.

CHAPTER -2

LITERATURE REVIEW

2.1 Introduction

Literature review is important for appreciating the evolution, advancements, and problems encountered during the design of SRAM sense amplifiers. As CMOS technology continues to improve, memories are being designed using advanced technology nodes with reduced voltages. While technology scaling has resulted in improved density and performance, it is also accompanied by several challenges that hinder reliable operation, such as increased leakage current, decreased sensing margins, and increased process variation, among others. In addressing these problems, different sensing schemes have been introduced from traditional cross-coupled voltage sense amplifiers to fast current mode sensing and decoupled latches, among others. The current chapter reviews these existing solutions and analyzes their weaknesses and design trade-offs before discussing the proposed architecture.

The chapter consists of two sections that give an overview about the prior work carried out in the area of SRAM sense amplifiers and limitations in these areas. Section 2.1 gives an overview about the introductory part of the literature review, where the issues faced due to scaling of the CMOS technology have been highlighted. Sections 2.2.1 to 2.2.4 give a description of voltage-mode sense amplifiers like CCVSA, LTSA, TGSA, and DIPSA with their respective working and advantages. Sections 2.2.5 to 2.2.7 discuss advanced SRAM cells, comparators and current-mode sensing techniques. Finally, section 2.3 deals with the limitations of the sense amplifiers and section 2.2 deal with Previous reported work.

2.2 Previous year work

2.2.1 Review of Cross-Coupled and Conventional Voltage-Mode Sense Amplifiers

Kalaiselvi, S., and R. Chandrasekaran [1] examined the basic performance tradeoffs that arise for standard CCVSA circuits using a typical 180 nm CMOS technology. The main objective was to study the correlation between the size of the transistors, sensing time delay, and chip overhead associated with the implementation of such circuits. It can be seen from the research that there is considerable loss of performance as well as evaluation time with reduced voltages.

Divya and P. Mittal [2] Purposed The Architecture of a sense amplifier is developed with reference to low power consumption and high efficiency in Static RAM. It has been compared extensively with other existing methodologies involving current mode and voltage mode latches. As a result, it is found that this architecture decreases dynamic power consumption because of minimum charging of internal nodes.

Gupta and Sharma [3] have carried out an analysis on cross coupled circuits for deep sub-micron technologies with their work on CCVSA configuration designed using 28nm CMOS Technology. It provides a full analysis of the weaknesses that exist in normal architectures due to the presence of short channel effects, leakage current, and threshold voltage variation during manufacturing. They demonstrate how the mismatch in devices results in reduction in sensing margin at small node sizes.

2.2.2 Review of Latch-Type Sense Amplifiers (LTSA)

Keerthiga and Mohanraj [4] have undertaken an exhaustive performance benchmarking of Latch-Type Sense Amplifiers (LTSA). They studied how subsequent scaling leads to a reduction in the charge/discharge time of the latching nodes. Their study empirically illustrates the increasing effects of parasitic capacitance from the bit lines, which demonstrates that traditional latch designs require much longer activation periods under sub-micron technology.

A. Kumar and S. K. Singh [5] migrated latch-type architectures into multi-gate device topologies by designing a low-power sensing network in 22 nm FinFET technology. Their research proves that the superior channel-gate electrostatic control inherent to FinFET structures successfully mitigates the subthreshold leakage and drain-induced barrier lowering (DIBL) common in planar CMOS layouts. The design achieves rapid latching speeds and stable rail-to-rail digital swing over varying capacitive bit-line configurations.

M. Revathi and A. Shanthi [6] introduced an architectural modification to the classic latch-type sense amplifier operating at the 90 nm node to achieve dual benefits of high speed and reduced energy consumption. By integrating specialized isolation transistors between the highly loaded bit-lines and the internal sensing latch nodes, their modified circuit limits the redundant discharge of the bit-lines, thereby drastically minimizing the overall energy-delay product (EDP).

This novel circuit is proposed by R. Pandey and S. Agarwal [7] designed a modified latch type sensing amplifier architecture suited for 16 nm FinFET technology. They used a novel biasing scheme to ensure high-speed operation along with minimizing leakage current. The paper clearly illustrates the limitation of the setup time overhead and voltage noise margin during power supply variation.

S. Daniel, M. Eisse, K. Eric, V. T. Ed, and N. Bram [8] interface was achieved The most significant innovation in the design of ultra-fast memory interface by who invented a Double-Tail Latch-Type Voltage Sense Amplifier. The novel technique employed by them to separate the input tracking functionality from latching functionality in terms of multi-tails guarantees that there will not be any node contention within the circuit. This innovative circuit offers setup/hold time of only 18 ps therefore, it is suitable for use in multi-gigahertz processor cores.

2.2.3 Review of Transmission-Gate Sense Amplifiers (TGSA)

According to P. Singh, A. Kumar, R. Kumar, and R. K. Singh [9] the effectiveness of pass-transistor logic in the area of memory peripheral design was tested using a transmission gate-based sense amplifier (TGSA). By taking advantage of the properties of the full-swing nature of NMOS and PMOS transistors working in parallel, the current drive capabilities for both states of evaluation could be made uniform.

P. K. Mishra and R. K. Singh [10] have scaled transmission gate circuits down to an extremely advanced 12nm technological node for studying the operational limits of such circuits in ultra-low voltage ranges. This work deals with maintaining reliable sensing behavior while employing extremely scaled down supply voltages (close to subthreshold levels). The suggested circuit exploits the concept of adaptive body biasing in order to mitigate severe performance degradation caused by process threshold voltage variations.

2.2.4 Review of Decoupled Inverter Pair Sense Amplifiers (DIPSA)

A. Dahiya, P. Mittal, and R. Rohilla [11] have developed the Decoupled Inverter Pair Sense Amplifier (DIPSA) for the 45nm CMOS technology that aims to address the problems associated with the conventional cross-coupled architecture. The new approach isolates the highly capacitive bit lines from the fast-switching internal latches right after detection of the signal. It makes it impossible for the bit lines to discharge unnecessarily, thus increasing the amplification rate and reducing active power.

Das and Chakraborty [12] have further evolved the decoupled inverter pair architecture to the extreme sub-10 nm regime using FinFET-based fabrication at 7 nm. In particular, this investigation focuses on the process-related mismatch and wide parameter variability issues arising from nanoscale fabrication. Leveraging the benefits of high drive-current characteristics of FinFETs, the proposed design ensures high mismatch immunity and low offset voltage values.

Dahiya A., Mittal P., and Rohilla R. [13] developed on their earlier decoupled study to come up with a modified decoupled sense amplifier suitable for low-voltage differential SRAM arrays. An effective technique is used to improve charge sharing and feedback such that the discharge of the output node is hastened during the evaluation period.

2.2.5 Review of Advanced SRAM Cells, Comparators and Interconnects.

A. Dahiya, V. Singhal, and P. Mittal [14] took the optimization approach to the memory core itself by designing a process-variation-tolerant 9T SRAM cell architecture. It is noteworthy that the proposed circuit has built-in write-assist capability in addition to a separate read path. Read disturbance is no longer an issue since it is ensured that the voltage difference on the read path will not affect the data

in the storage nodes.

Jindal E., Singh D., Kumar C., Mittal P. [15] devised a highly accurate and low power-consuming comparator architecture in 45 nm CMOS technology, which can be used for deep learning-based computing systems hardware accelerators. Even though designed specifically for mathematical acceleration, the architecture itself is based on high-gain regenerative circuits similar to sense amplifiers. There is much to learn from this paper regarding lowering offset voltages and designing differential tracking loops.

2.2.6 Review of Current-Mode Sensing and Hierarchical Routing Techniques

Seeninck E., P.J.V. Beers, and H. Ontro [16] proposed sophisticated methods for current mode that could be applied in VLSI circuits. It was shown that while the time response for voltage mode increases exponentially due to high capacitances of the bit lines, the time delay in current mode sensing technique is not influenced by bit line capacitance.

B. D. Yang and L. S. Kim [17] proposed A very efficient and low power consumption SRAM cell using a bit line hierarchical layout along with sense amplifiers which are located locally. By subdividing the lengthy and high capacitance global bit lines into small sized and less capacitance local bit lines, no charging needs to take place for huge line parasitics.

C. Chiu-Chiao, L. H. Chin, and Y. Tall [18] presented Layout of a novel fast-sense amplifier specifically designed to address the issue of sensing very small currents from non-volatile Flash memories. The authors describe the problem of sensing extremely small currents from Flash memories and design a fast sense amplifier which is highly immune to noise.

J. S. Wang and L. Hong-Yu [19] a new current-mode sense amplifier was invented that is tailor-made for use in low-voltage and limited energy consumption SRAM operations. The invention makes use of an active current mirror feedback mechanism that controls the bit line swing to the smallest possible value during the read time period.

2.2.7 Comparative Studies, Subthreshold Circuits and Material Analyses

Kishore, C., & Kumar, A. [20] conducted a comprehensive comparison between the top three voltage-mode sense amplifier architectures (namely, CCVSA, LTSA and TGSA) in terms of their performance through 45nm CMOS technology. The two researchers provided an elaborate assessment of all these designs under similar environmental and operating conditions. The results from their analysis distinctly identify the areas of superiority for each one of these designs.

A. Hemaprabha and K. Vishwa [21] The authors have provided an extensive study on memory sensing techniques spanning different epochs and technology nodes. The

classification by the authors clearly distinguishes between voltage mode and current mode block based on essential factors like scalability of power supply, Power Delay Product (PDP), and layout complexity.

P. K. Pal and R. K. Nagaria [22] investigated ultra-low energy regions through the creation of a MOS-only sub-threshold voltage reference circuit specifically developed to ensure stability during operation under very broad temperature variations. The designed circuit does not incorporate bulky area-occupying passive elements like resistors; instead, it employs sub-threshold transistor properties in order to create a stable voltage reference that is required to bias external blocks within low-power circuits.

R. Selvakumar, M. L. Kumar and S. R. Gopal [23] executed a material-level and physical-layer analysis detailing the severe high-degree variability found in modern thin CMOS manufacturing layers. The authors mapped how physical fluctuations in thin-film oxide layers induce random channel doping variations directly shifting the threshold matching profiles of the delicate matched-transistor pairs within SRAM current sense amplifiers.

A. K. Pathrikar and R. S. Deshpande [24] investigated local optimization techniques for circuit synthesis that were specifically designed for generating power-efficient sense amplifiers that operate very quickly. The approach utilizes custom sizing techniques for appropriately scaling the peripheral transistors' widths and thereby reducing parasitic input capacitance without compromising transconductance, which is necessary for fast latch triggering times.

Y. Moisiadis, I. Bouras and A. Arapoyanni [25] have proposed topologies for level restoration that are suitable for application in the low-power reduced swing interconnect environment. The emphasis of their approach is on the fast restoration of low-voltage signals back to full CMOS logic voltage levels. Such a tracking approach yields very useful structures for weak signal distribution on heavily loaded VLSI global buses.

2.3 Research Gap

The Difficulty in Realizing High Sensing Speed and Low Dynamic Power Consumption Simultaneously One of the significant difficulties associated with sense amplifier design in SRAM circuits is designing such a device that will work at high sensing speed while consuming a relatively low amount of dynamic power. Typically, devices designed to work fast have good current driving ability, which makes them consume more dynamic power and produce more leakage current when operating in a standby mode. In addition, since low-power designs work to limit current flows, they reduce sensing speeds and delays in memory read operations. The Problems Associated with Working at a Reduced Supply Voltage Advanced CMOS technologies have to operate at a lower supply voltage in order to reduce dynamic power consumption and improve battery life of portable devices. Lower supply voltage levels make the transistors switch slower, thus reducing their effectiveness

when working in a low-swing regime. As a consequence, such sense amplifiers need more time to sense relatively smaller voltage swings created in SRAM cells. Low-voltage levels increase error risks and decrease the overall stability and reliability of memory systems.

High Parasitic Capacitance for the Bit-Line in SRAM Memories Since there are multiple memory cells coupled through long bit-lines, a high parasitic capacitance appears in the memory array of SRAM memories. The process of reading the memory contents involves first charging/discharging the high capacitors before reading out the contents from the memory. This increases sensing time, hence making the memory perform poorly. High bit-line parasitic capacitance makes the memory consume more power since more charge needs to be stored and discharged.

Sensitive to Fabrication/Process Mismatches Many existing sense amplifiers are quite sensitive to fabricating and process mismatches. Minor changes to the fabrication process, such as variations in transistor parameters, will adversely affect the performance of the sense amplifier. In some cases, this could result in poor sensing due to mismatches in the transistors that form the sense amplifier.

Comparison Problem Related to Fair Performance Comparing previous architectures of the sense amplifier poses a problem in many cases because of the fact that each study use different supply voltage levels whereas some other researches use different CMOS processes or values of the bit-lines capacitor. Hence, due to such a condition, fair comparisons cannot be made on the basis of the delay time, power dissipation or PDPs of the devices. This causes a lot of confusions regarding the choice of the most efficient structure. Requirement for the Advanced Design as a consequence of the inefficiencies of the conventional sense amplifiers, the development of the improved design becomes absolutely necessary in order to make the sensing fast, power efficient and reliable. The new design must be able to operate effectively and reliably at low voltages. In addition, the new design must minimize the impact of bit-line capacitor and operate successfully under different process or environment conditions.

CHAPTER - 3

CHARACTERISTICS COMPARISON OF DIFFERENT VOLTAGE MODE SENSE AMPLIFIERS

3.1 Introduction

This chapter provides a thorough analysis of several different types of sense amplifiers that are widely used in SRAM arrays. Peripheral circuits in the context of high-speed memory systems have an extremely important role when it comes to determining system performance metrics. Prior to designing an advanced sense amplifier system, it is crucial to investigate the operation of conventional sense amplifier designs under normal operational conditions.

In order to lay a strong base, first in this chapter the basic structure and working principle of a common 6T SRAM cell will be described in detail. Analysis of bit line discharge behaviour during the read operation of a memory cell is important to understand the operation of the sense amplifier. In addition to the memory array structure analysis, in this chapter a total of five conventional sense amplifier structures will be investigated. This includes Latch-Type Sense Amplifier, Decoupled Inverter Pair Sense Amplifier, Cross-Coupled Voltage Sense Amplifier, Transmission-Gate Sense Amplifier and Parallel Latch-Type Sense Amplifier.

Each type of topology is then tested and simulated in similar operational conditions using the design software. Through this, it will be possible to analyze their respective circuit diagrams, internal node signal transitions, and input/output timing waveforms. The analysis of all these different variables will enable the chapter to establish a baseline for the evaluation of some of the important metrics in wireless systems such as signal sensing delays, power consumption during dynamic operations, leakage current while in standby, and the power-delay products.

The performance analysis of sense amplifiers with the use of various voltage mode sense amplifiers will be discussed in this chapter in different sections. Introduction and significance of the analysis of conventional sensing circuits will be presented in section 3.1. Structure and operation of the typical 6T SRAM cell will be explained in section 3.2. Principles and significance of sense amplifiers in memory cells will be discussed in section 3.3. Different types of differential sense amplifiers like, LTSA, DIPSA, CCVSA, TGSA and PLTSA with respect to their operation and other characteristics will be discussed in section 3.4. Performance comparison of these sense amplifiers with regard to delay, power dissipation, leakage current and Power Delay Product (PDP) will be done in section 3.5.

3.2 Static Random Access Memory

Static Random Access Memory (SRAM) is a type of volatile semiconductor memory that retains its stored data as long as electrical power is continuously supplied to the

circuit. One of the greatest advantages of SRAM is its exceptional operational speed. It operates at virtually the same speed as modern digital logic circuits and central processing units (CPUs). In addition to its high-speed performance, SRAM is highly valued because it consumes a minimal amount of leakage power when it is in standby mode. Because of these superior characteristics, SRAM is heavily utilized to build high-speed storage links such as cache memory systems (L1, L2 and L3 caches) directly within or close to the main processing cores.

Modern high-performance computing systems strictly require memory architectures that can execute operations rapidly while maintaining excellent energy efficiency. This section covers the fundamental concepts of SRAM which serves as the core foundation for memory array peripherals. In memory systems the sense amplifier and the SRAM cell work in close cooperation. In fact, the operational characteristics of the SRAM cell directly dictate the performance requirements of the sense amplifier. In this work, a comprehensive comparative analysis of different cross-coupled sense amplifiers connected to a standard 6T SRAM cell is explored and simulated. To properly analyze the design and behavior of a sense amplifier it is essential to first master the basic concept layout and operation of the underlying SRAM cell. The basic circuit schematic of a standard 6T SRAM cell structure is illustrated in Fig. 3.1.

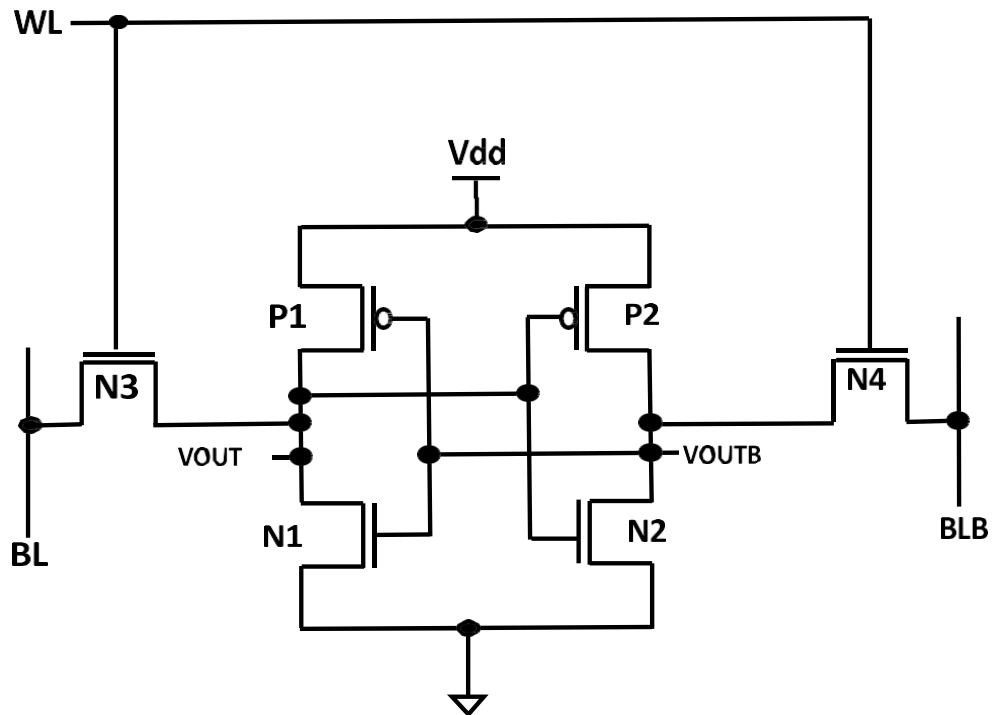


Fig. 3.1 Schematic of 6T SRAM

At its core, a standard SRAM cell functions similarly to a bistable latch or a flip-flop circuit. Binary data representing either a logic "0" or a logic "1" is securely stored on the internal storage nodes of this cross-coupled inverter latch structure. A conventional 6T SRAM cell is constructed using exactly six Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs). Among these six devices four transistors are configured to form two back-to-back CMOS inverters. These inverters create a positive feedback loop that holds and locks the stored data bit indefinitely provided the power remains on. The remaining two transistors function as access or pass transistors. These access devices act as controlled switches that connect the internal storage nodes of the cell to the external heavily loaded bit-lines (BL and BLB). The entire SRAM memory cell can be selectively accessed for a read or write operation only when the control signal on the Word Line (WL) is driven to a high voltage state which turns on these pass transistors.

3.3 Sense Amplifier

A Voltage Mode Sense Amplifier (VMSA) is an important peripheral component used in high-speed SRAM to detect and amplify small voltage differentials that exist on the bit-lines during reading operations. During the accessing of a particular memory cell, a small voltage differential will be created on one of the heavily loaded bit-lines via the transistors of the cell. Since the bit-lines run all the way up to the memory column, they have a high parasitic capacitance that results in the slow discharging of this differential. In other words, it is both time consuming and energy inefficient.

In order to save time and energy, a particular memory cell is only permitted to create a small differential voltage drop between the two complimentary bit-lines. As such, the voltage differentials are very weak and measure only a few millivolts. Such small voltages cannot easily be detected using normal digital logic components; thus, it is imperative that a voltage mode sense amplifier is utilized to detect and amplify the signal.

The Voltage-mode sense amplifier senses the minute voltages that are produced on the bit-line due to the reading process in SRAM. These amplifiers have cross-coupled transistors that help to amplify the signal within a short while. At the beginning, when the sense amplifier is still in the pre-charge mode, the bit-lines as well as the internal nodes are brought to an equal voltage level.

During the process of reading, a tiny voltage is created by the SRAM cell on the bit-lines based on the information stored in the cell. Once the voltage difference becomes large enough, the sense amplifier triggers by way of an external control signal, whereupon the internal latch circuit amplifies the signal and generates a logic zero or one.

3.4 Differential Sense Amplifier Topologies

Differential Sense Amplifiers are often employed in SRAM memory systems in order to amplify small voltage differences which occur during the process of reading. The device operates using two complementing bit-lines, namely Bit-Line (BL) and Bit-Line Bar (BLB). Each of them contains different logic signals that make it possible for the circuit to detect stored information more precisely. In the case of a common memory read sequence, both bit-lines receive a charge of maximum supply voltage levels. Once the cell of interest gets addressed through the word line and activated, its inner circuit starts drawing current from either of the bit-lines and discharging it. At the same time, the other bit-line will stay unchanged in its initial voltage level because no action will be taken regarding it. Thus, there occurs a small difference between BL and BLB voltages in an analog form. The job of the differential sense amplifier is to act as a detector that converts a tiny voltage difference into a full-scale digital signal.

3.4.1 Latch Type Sense Amplifier

The purpose of the LTSA is to distinguish the very slight difference between the voltages on the two complementary bit-lines and produce the digital output accordingly. The functioning of the LTSA is enabled by a signal called 'Sense Enable' or SE. The figure of the latch-type sense amplifier (LTSA) shown in fig. 3.2 is a popular example of voltage mode sense amplifier used in 6T SRAM memory cell array. The basic structure of the LTSA includes two CMOS inverters which are interconnected in the form of a cross couple, where the input of one of the inverters is connected to the output of another inverter, thus forming the latch. The input terminals of the latch circuit are connected to the bit-lines of SRAM using the NMOS access transistors.

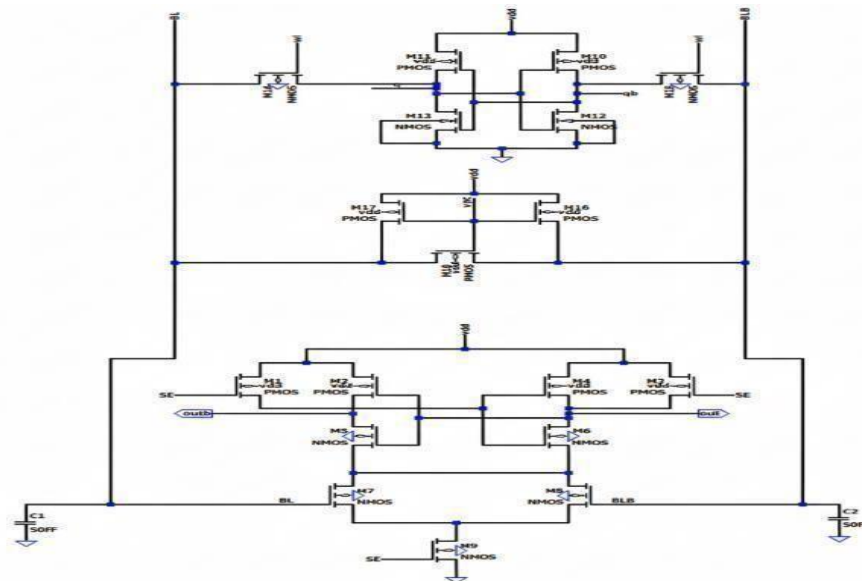


Fig. 3.2 Schematic of Latch Type Sense Amplifier

The LTSA operation can be described through the use of two states. The first is the standby state in which no read operation is taking place, meaning that the Sense Enable (SE) signal is at zero volts. In this case, the enable transistors are off, effectively isolating the cross-coupled latch from the power rail. This causes the cross-coupled latch to be idle hence not utilizing any power. It also makes sure that there is no interference with the bit-lines that have been pre-charged

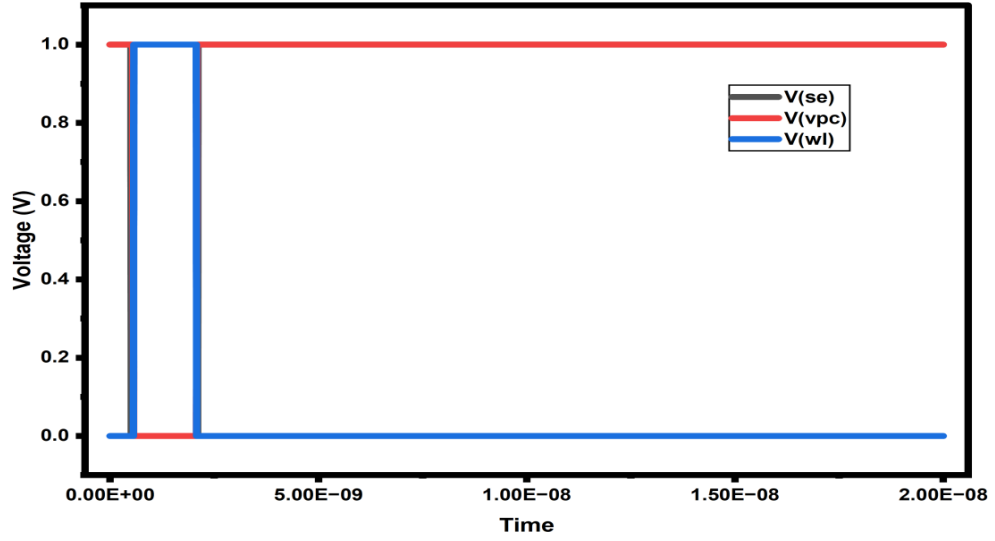


Fig. 3.3 Input Signal Waveform of LTSA

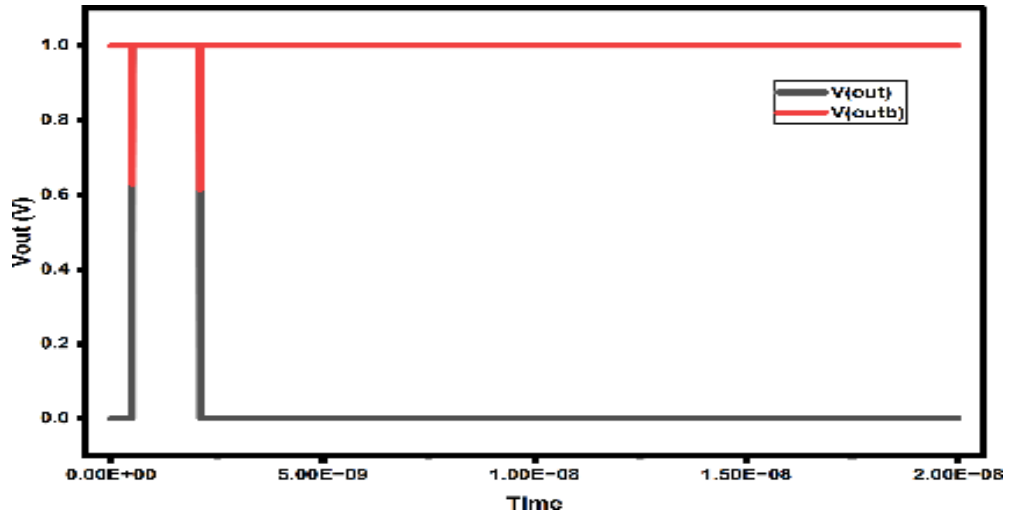


Fig. 3.4 Output Signal Waveform of LTSA

In the read process, however, the behaviour of the LTSA varies since the sense amplifier moves into its sensing stage. This means that there will be a slight difference in voltage between the BL and the BLB since one of the bit lines is now

discharging from the SRAM cell being used for the read process. Once there is enough difference between the two bit lines, the SE signal switches to “High”, activating the latch circuitry.

Once activated, the cross-coupled inverters start amplifying the small input differences due to positive feedback. Since the voltage difference is slight, the node with the slightly higher voltage goes towards the positive power rail, while the other node is driven down towards the ground. This converts the weak signal input into either a logic "0" or "1".

3.4.2 Decoupled Inverter Pair Sense Amplifier

The Decoupled Inverter Pair Sense Amplifier (DIPSA) is a voltage mode sensing scheme that aims to improve the performance of the SRAM sense amplifier by minimizing the impact of high capacitance on the bit-lines on the internal latch. Unlike typical sense amplifiers where the bit-lines are coupled directly to the latch circuit, DIPSA employs isolation transistors, typically fabricated using PMOS transistors, for separating the latch from the bit-lines once the sensing process starts. This separation makes it easier to achieve higher amplification rates while minimizing dynamic power dissipation. The overall working principle of the DIPSA circuit can be analyzed based on various operating phases as well as transient simulation results. The DIPSA circuit schematic is provided in Fig. 3.5

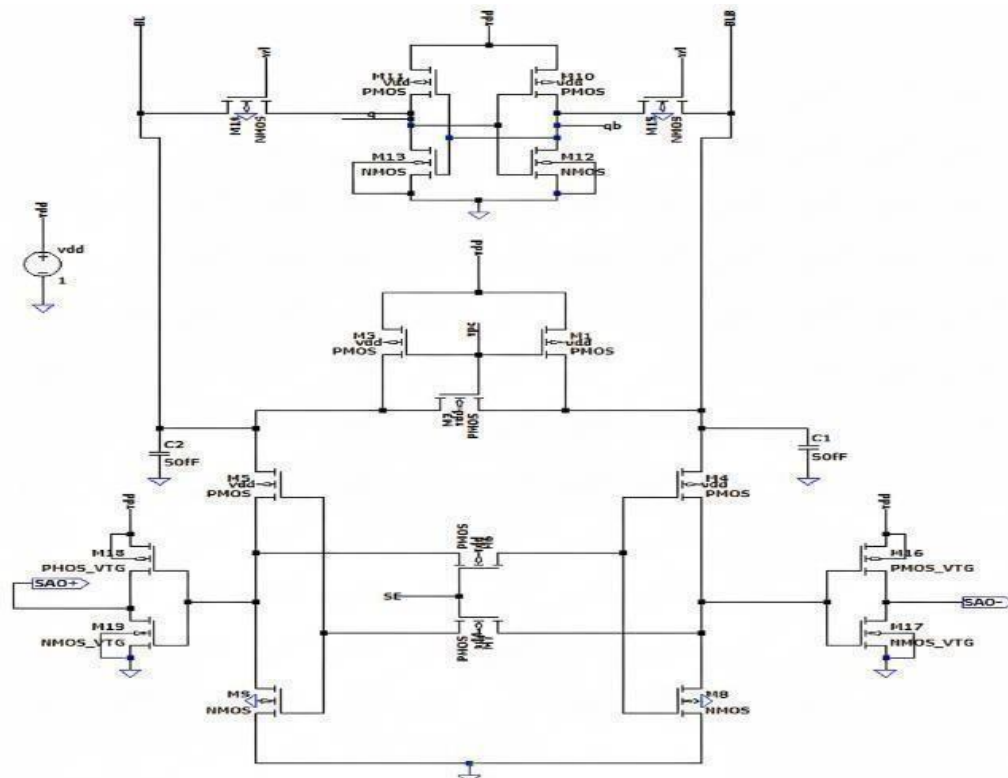


Fig. 3.5 Schematic of Decoupled inverted pair Sense Amplifier

The functioning of the DIPSA can be illustrated in terms of different stages. At the first stage, both BL and BLB bit-lines and internal sensing nodes are charged to the supply voltage (VDD) level. This happens because of the presence of the PRE signal which activates the PMOS pre-charge transistor. It is crucial that bit-lines should have the same voltage, otherwise, an output error will occur due to the mismatch before sensing operations. Once pre-charging is done, the signal of PRE turns high to remove the path of pre-charge. Now the selected SRAM cell causes a slight voltage difference between BL and BLB.

The next stage is a stage of sensing and amplification. At this stage, SAE signal is activated causing enabling of the sense amplifier and connecting the internal latch with the bit-lines through decoupling switches. Latch circuit is developed using the cross coupled PMOS and NMOS transistors. There will be some imbalances within the latch circuit due to even the smallest voltage difference on the bit-lines. Due to the positive feedback action, one node of the latch circuit quickly approaches the level of VDD while the other node goes to the level of GND.

The output stage involves passing the amplified signal to the succeeding circuit blocks. The output pins are connected via buffer inverters built using CMOS technology. These buffer circuits play an important role in preventing the internal latches from being influenced by the external load capacitances or noises. Buffering enhances the driving capability and minimizes the propagation delay. The working of the circuit is analyzed via transient analysis using simulation software. The simulation reveals that the two bit lines have the same voltage value as VDD before reading data. Once the process begins, one bit line discharges slowly in order to create the voltage difference necessary for sensing.

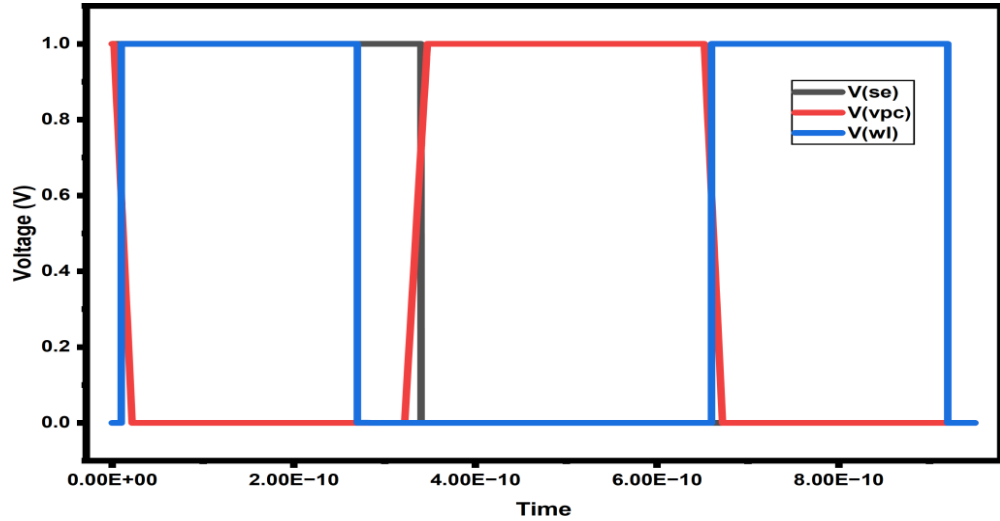


Fig. 3.6 Input Signal Waveform of DIPSA

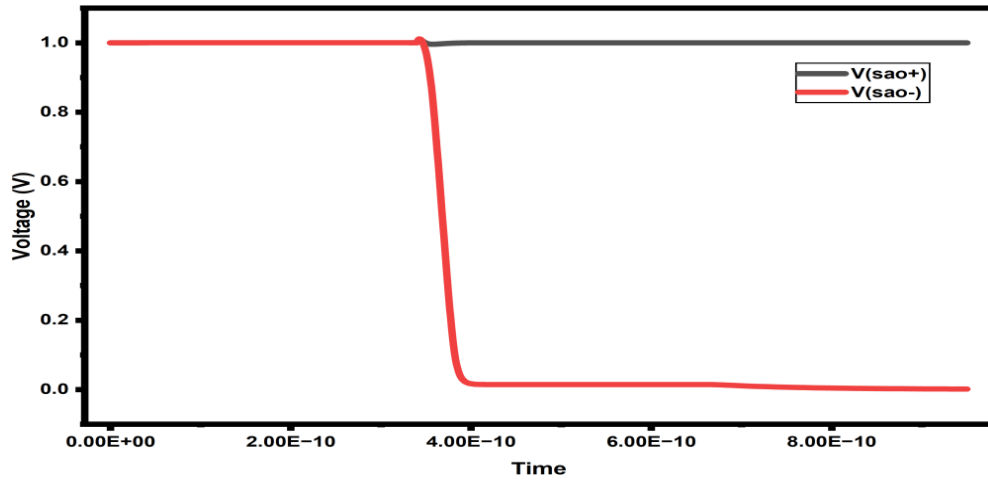


Fig. 3.7 Output Signal Waveform of DIPSA

In transient analysis, one of the significant events is the time at which the SAE signal goes high, thus triggering the sense amplifier. During this time, there is a very fast swing between the two internal nodes of the latch to be either high or low. One node reaches VDD potential while the other swings toward ground potential. Also, the output signals, SAO+ and SAO-, demonstrate fast changes and digital output voltages. It can be deduced that the switches have been able to disconnect the internal latch from the bit-line capacitance.

3.4.3 Cross Coupled Voltage Sense Amplifier

The Cross Coupled Voltage Sense Amplifier (CCVSA) is one of the easiest and the most widely used voltage mode sense amplifiers in standard 6T SRAM designs shown in Fig. 3.8. Because of its easy construction, this scheme is ideal for use in high density memory arrays where compactness and lesser leakage currents play an important role in the design of the circuit. The CCVSA comprises of two CMOS inverters that are interconnected in a cross coupled way such that the output of one inverter serves as the input of the other and vice versa. This creates a latch network that remains stable till the time a slight voltage difference exists at the input terminals. After this voltage difference is established in the circuit, the network is able to amplify the small signal at the input terminals to a full digital signal via positive feedback.

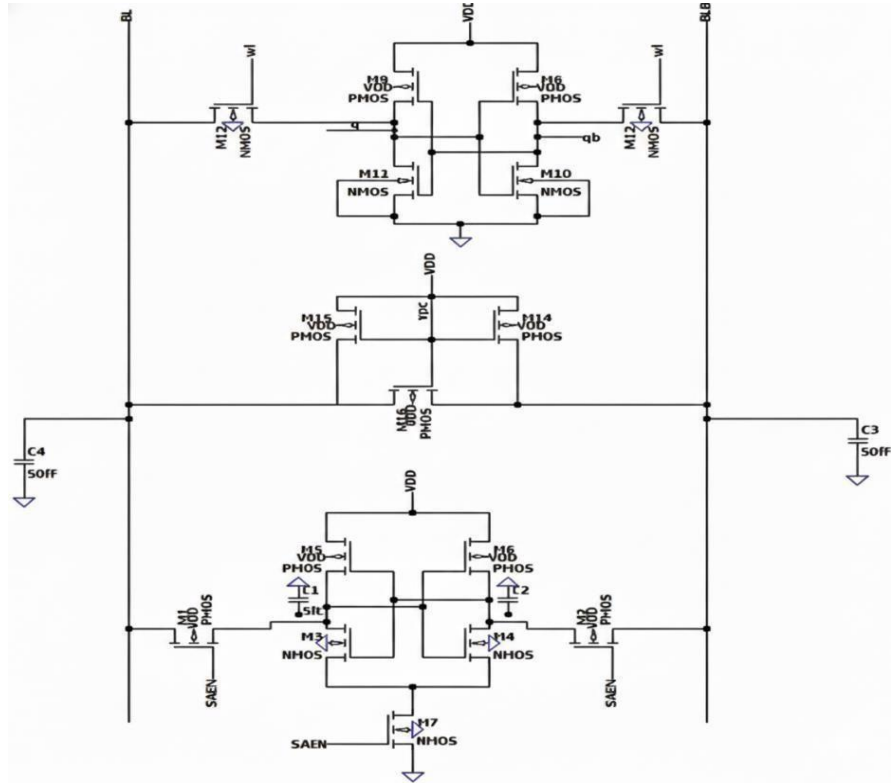


Fig. 3.8 Schematic of Cross Coupled Voltage Sense Amplifier

When the read cycle begins, the word line of the 6T SRAM cell goes high, and the access transistors become ON. Thus the cell begins discharging either one of the complementary bit lines depending upon the state of the stored information, whereas the other bit line stays near the supply voltage level. There is thus an incremental voltage difference developed between the bit lines. Because of direct connection of the bit lines with the cross coupled latch, there will be a corresponding increment in the voltages applied to the two input nodes of the inverter. Because of this, one of the input nodes gets lower than the other one. This disrupts the stable state of the latch, and the regenerative feedback cycle starts producing digital outputs.

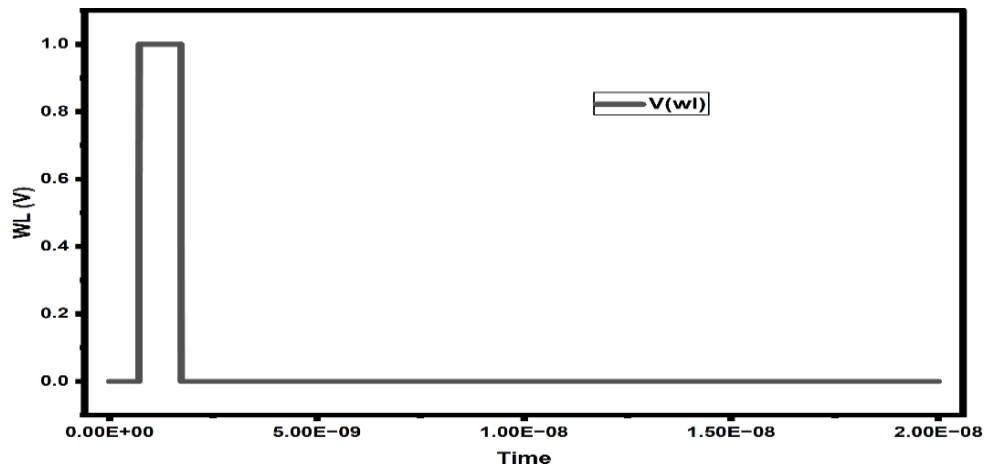


Fig. 3.9 Input Signal Waveform of CCVSA

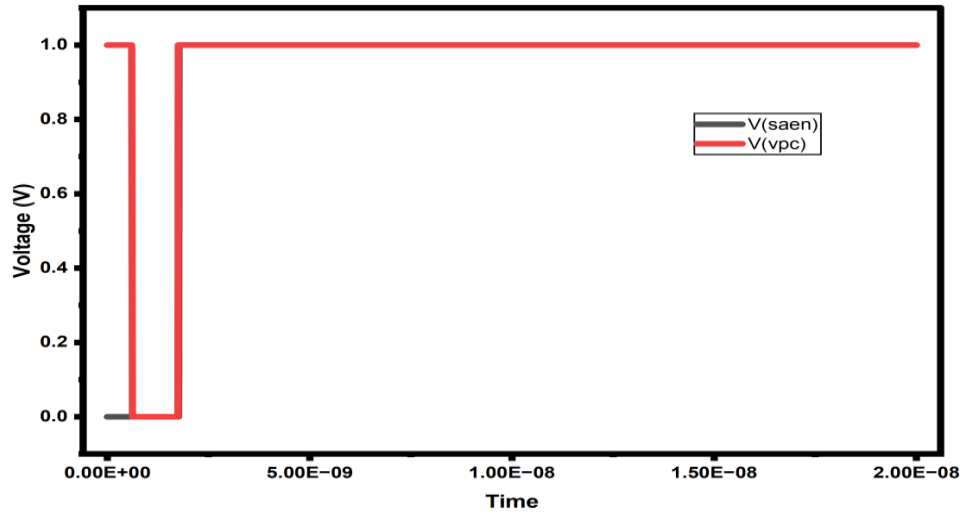


Fig. 3.10 Input Signal Waveform of CCVSA

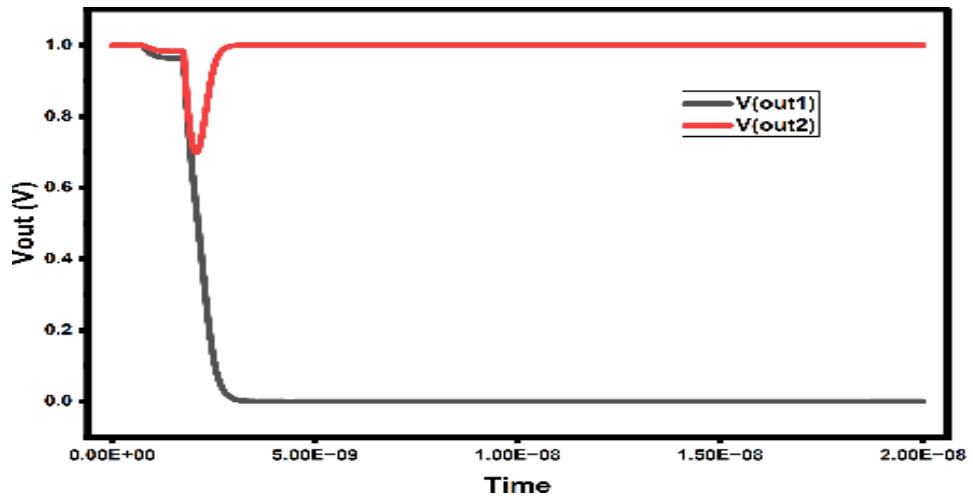


Fig. 3.11 Output Signal Waveform of CCVSA

Once there is a difference in the small voltage between the inputs of the circuits, the cross coupled inverter circuit starts the sensing process by generating a positive feedback. If there is low input voltage on any node, the corresponding output will try moving toward VDD, whereas the second output will try moving towards ground voltage level. As both inverters are linked, a huge voltage difference develops very quickly due to positive feedback. Ultimately, either of the outputs gets the logic “1” state and another output gets the logic “0” state. Through this way, the small signal generated by bit lines can be amplified into digital signal.

3.4.4 Transmission Gate Sense Amplifier

The Transmission-Gate Sense Amplifier (TGSA) is a voltage-based sense amplifier technique employed in 6T SRAM memories that help enhance the accuracy of the

signal and sensing operations. According to the TGSA design, each bit-line is coupled to the internal latch through a CMOS transmission gate. The construction of a transmission gate entails putting together one NMOS and one PMOS transistor in parallel fashion. In the process of operation of the TGSA, the first step involves pre-charging both bit-lines BL and BLB with the supply voltage level VDD. The stage involves keeping the transmission gates on so that there would be a disconnect between the internal latch and memory bit-lines. Isolation will ensure that there is no interference in the form of noise during standby mode.

When reading operations are performed, the selected SRAM cell will discharge the bit-line and generate a small voltage difference across the BL and BLB lines. Once this voltage difference crosses the threshold voltage level for sensing, the Sense Amplifier Enable (SAEN) control signal turns on the transmission gates. As a result, the voltage levels on the bit-lines are transferred to the internal latch nodes through the transmission gates. Due to the capability of CMOS transmission gates to transmit both logic “0” and logic “1” equally well, the signal transmission becomes more reliable when compared to using NMOS pass transistor circuits. The schematic of the TGSA is shown in Fig. 3.12.

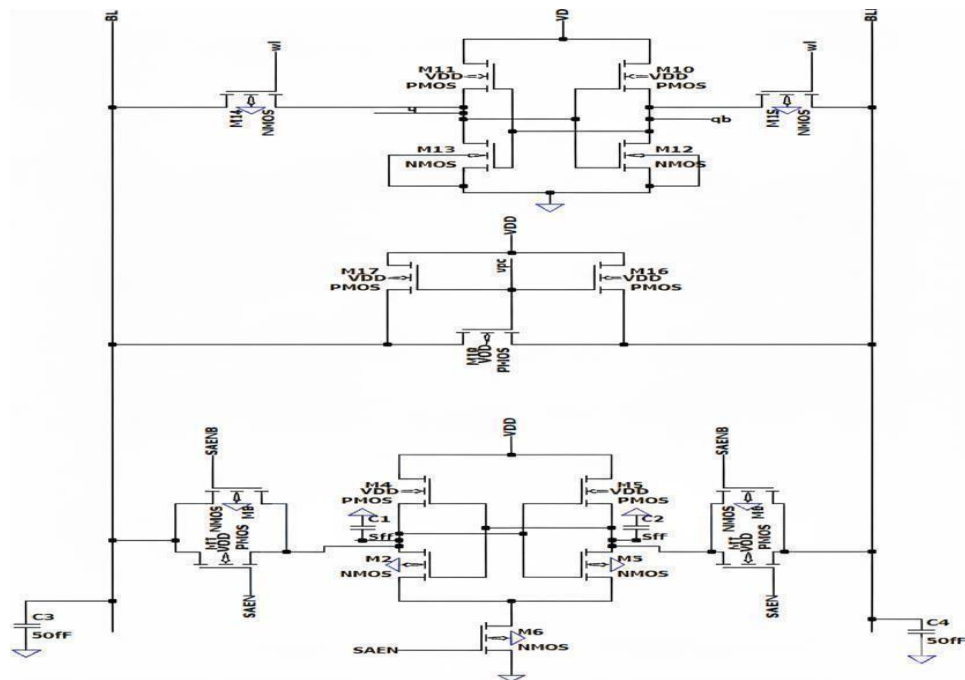


Fig. 3.12 Schematic of TGSA

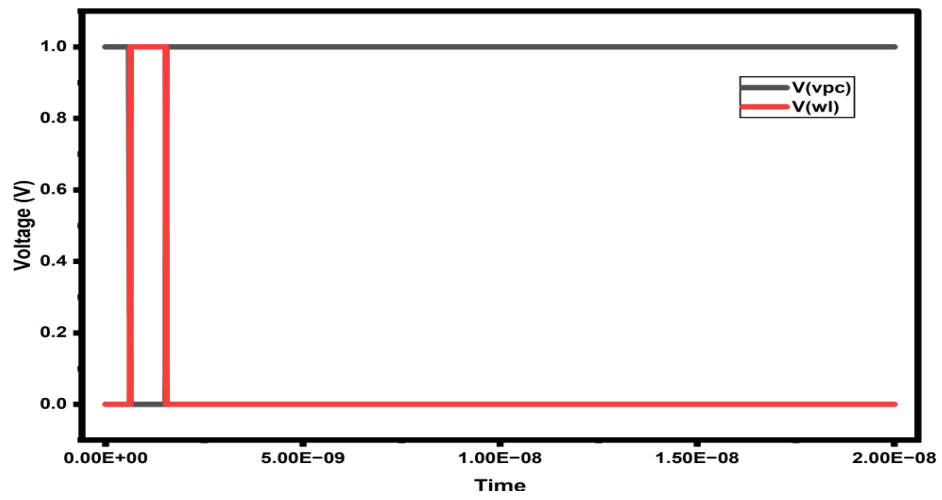


Fig. 3.13 Input Signal Waveform of TGSA

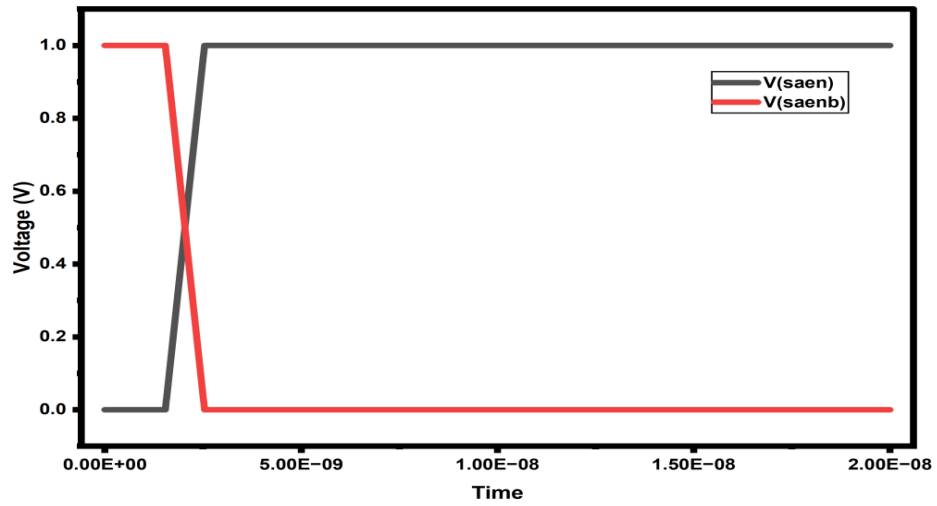


Fig. 3.14 Input Signal Waveform of TGSA

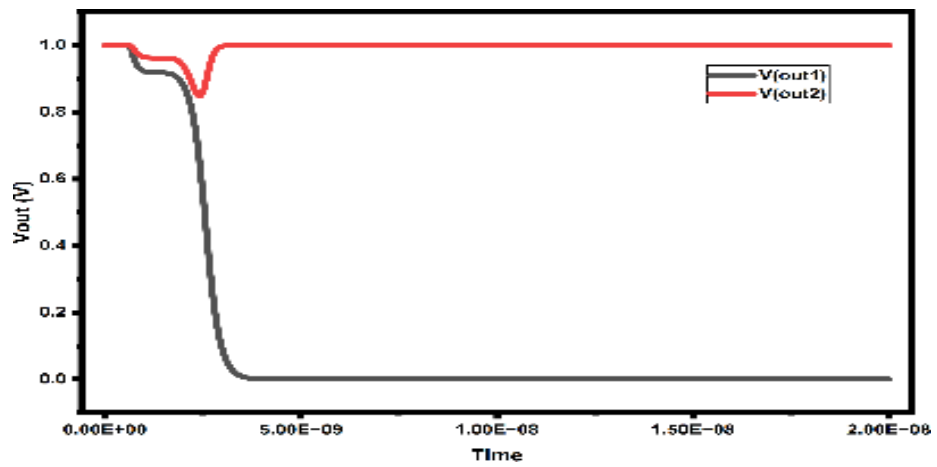


Fig. 3.15 Output Signal Waveform of TGSA

The last stage of TGSA function involves the amplification and output generation stage. The small voltage difference will cause the trigger on the internal latch when received by the transmission gate. It triggers the positive feedback action of the circuit and hence causes a fast transition of the node with higher voltage toward logic 1 or V_{dd} and the other node toward logic 0 or ground state. Hence, the weak input voltage is amplified to generate a digital output.

After amplification, the latch circuit holds the stored data in the output nodes. After reading is complete, the control signal switches off the transmission gate and thus disconnects the internal latch from the bit-lines. In this case, the TGSA goes back to standby mode to carry out the next operation. Hence, TGSA acts like a cross coupled-latch that is enhanced with the use of CMOS transmission gates.

3.4.5 Parallel Latch Type Sense Amplifier

The Parallel Latch-Type Sense Amplifier (PLTSA) is an upgraded voltage sense amplifier in the SRAM memory system that performs faster sensing and minimizes bit-line capacitance effects. Traditional latch-type sense amplifiers suffer from slow sense operation due to their large bit-line capacitance that remains connected to the latch circuitry. In order to solve the above drawback, the PLTSA employs extra parallel transistors connecting bit-lines and the internal latch circuit.

The working of the PLTSA starts by entering its pre-charge phase wherein the SE signal stays low. The above step ensures that no operation takes place since the cross coupled latch and parallel transistors remain in an inactive mode at this stage. In other words, the above steps ensure that the sense amplifier circuitry stays isolated from the memory bit-lines. The schematic of the PLTSA is shown in Fig. 3.16.

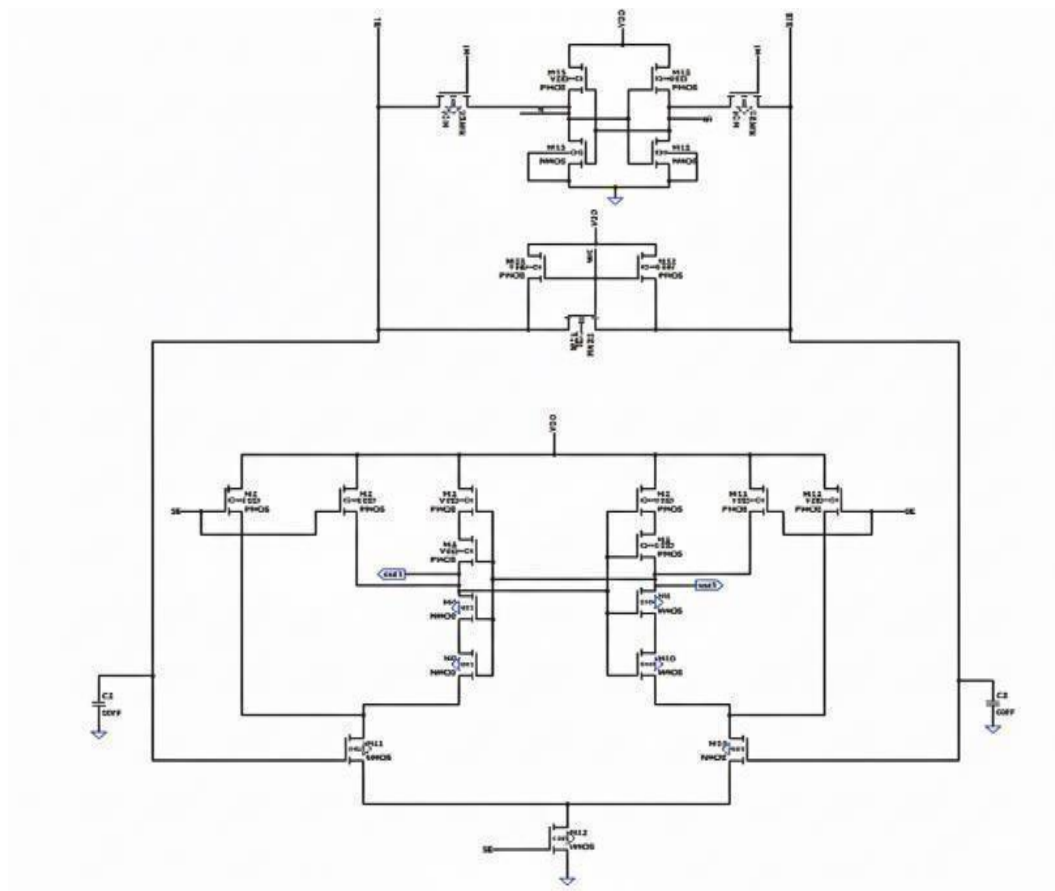


Fig. 3.16 Circuit Schematic of PLTSA

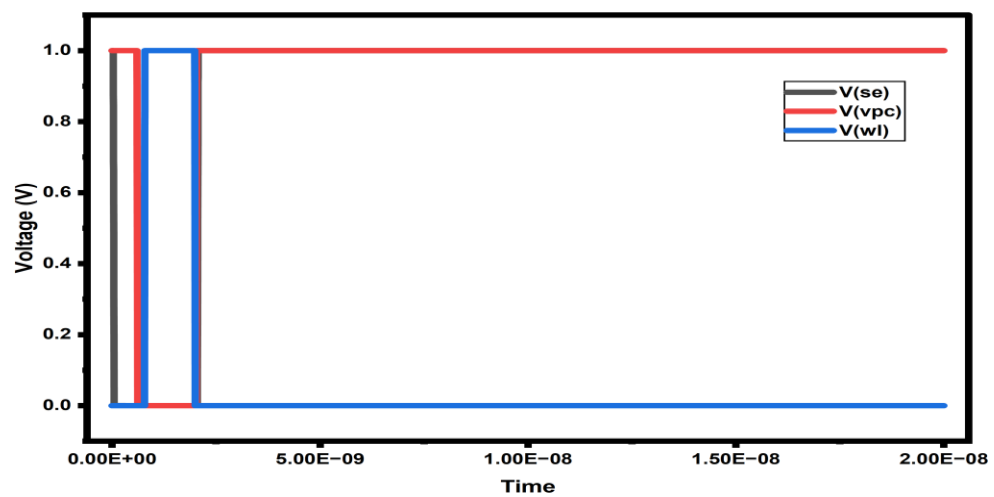


Fig. 3.17 Input Signal Waveform of PLTSA

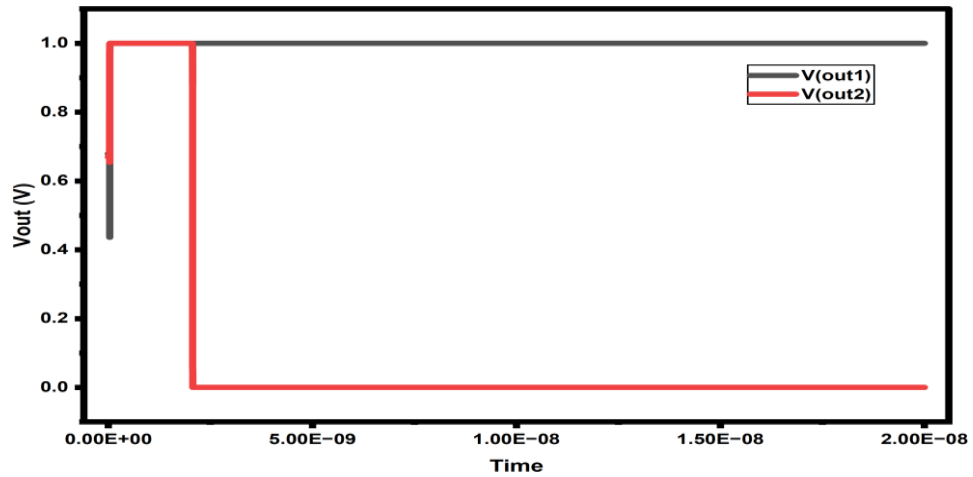


Fig. 3.18 Output Signal Waveform of PLTSA

In the PLTSA, its dynamic sensing starts as the word line of the selected SRAM cell turns into a HIGH state. As a result, the memory cell begins to discharge either the complementary bit lines depending upon the data stored in it. At this point in time, the internal latch circuit is almost isolated from the bit lines so that the loading caused by the large bit line capacitance can be reduced. After a certain time delay, the Sense Enable (SE) signal turns HIGH, thus activating the cross coupled latch along with the parallel transistors path. These transistors couple the voltages present on BL and BLB onto the latch inputs without directly coupling the large bit line capacitance.

At this point the latch amplifier takes advantage of positive feedback to drive the slight voltage differential. This happens because the internal node that connects to the more positively charged bit-line has quicker charge boosting capability due to the parallel connection of the extra transistors, thus making the circuit move out of balance. At this stage, one internal node reaches VDD level, while the other node reaches ground level creating a digital output. Once sensing is complete, the latch preserves the output while the SE signal turns off and is ready for the new memory cycle. Because the parallel transistors function only during the sensing phase, there is no power consumption and the PLTSA is very fast and efficient.

3.5 Comparison Table of Existing Sense Amplifiers at 1 V and 50 fF Bit-Line Capacitance

To evaluate the performance of these different architectures fairly, all five voltage-mode sense amplifiers were simulated under identical operating conditions. The measured performance parameters including sensing delay, power consumption, Power-Delay Product (PDP) and standby leakage current are summarized in Table 3.1

Table 3.1 Performance parameters comparison of conventional sense amplifiers.

Sense Amplifier	Delay (ns)	Power (μ W)	PDP (fJ)	Leakage Current (pA)
DIPSA	0.368	59.64	21.947	84.80
TGSA	2.00	6.09	12.18	15.88
CCVSA	1.58	3.26	5.157	11.84
LTSA	1.54	13.19	20.31	15.88
PLTSA	1.28	6.60	8.448	20.62

The simulation data presented in Table 3.1 reveals distinct performance variations among the five traditional sense amplifier architectures.

DIPSA Performance: DIPSA operates with the fastest speed recording a tiny sensing delay of just 0.368 ns. This high speed occurs because its internal design disconnects the switching nodes from the large bit-line capacitance. However this high performance demands massive energy. It consumes the highest power at 59.64 μ W and generates an extremely large standby leakage current of 8480 pA. This poor energy profile pushes its Power-Delay Product (PDP) to the highest value of 21.947 fJ.

CCVSA Performance: CCVSA proves to be the most efficient design for saving power and minimizing leakage. It draws the minimum active power of only 3.26 μ W and exhibits a very low standby leakage current of 11.84 pA. Thanks to these low values, it achieves the best (lowest) overall PDP of 5.157 fJ, even though its speed is relatively slow with a delay of 1.58 ns.

TGSA and LTSA Performance: TGSA is the slowest circuit in the group taking 2.00 ns to sense the signal, but it maintains a moderate power profile of 6.09 μ W. the conventional LTSA requires 1.54 ns to complete its evaluation and draws a higher active power of 13.19 μ W, which results in a high PDP of 20.31 fJ.

PLTSA Performance: PLTSA successfully achieves a well-balanced compromise between speed and energy conservation. By employing parallel transistor tracks it speeds up evaluation to a delay of 1.28 ns, making it faster than LTSA, CCVSA and TGSA. Concurrently, it restricts its active power to a conservative 6.60 μW and keeps leakage low at 20.62 pA, yielding a highly competitive PDP of 8.448 fJ.

CHAPTER - 4

MODIFIED DECAP-ASSISTED SENSE AMPLIFIER (MDASA)

4.1 Introduction

Several different sense amplifier designs have been suggested for the implementation in SRAM memories, however the design of an amplifier operating both fast and with low power consumption is a challenging issue. With the scaling of CMOS technology and decreased supply voltage, a traditional sense amplifier becomes slow and less reliable for read operations. Decreased supply voltage decreases driving capabilities of transistors, which results in increased sensing time. Additionally, large bit-lines of memories lead to large capacitances and therefore, to degraded performance of circuits. In order to solve aforementioned issues, this chapter suggests a new design of sense amplifier - the Modified Decap-Assisted Sense Amplifier (MDASA). The goal of the MDASA design is to provide a sense amplifier, which would be fast enough with relatively low power dissipation and reliable in low-voltage regimes.

The MDASA design uses small internal capacitors that can hold some amount of charges in the pre-charge period. In the sensing operation these small capacitors provide extra charges to the latch circuit which can speed up the transistors and increase the sensing operation. The parallel paths through transistors also contribute to the quick transfer of the small voltage difference between bit-lines into the latch. Thus, using capacitors and parallel paths does not require continuous current consumption in the stand-by mode but is only required for the sensing time. So the proposed design results in lower PDP values. This chapter will analyze in more detail the circuit structure, operation of transistors in the MDASA and all different stages of its work. Finally LTspice simulation results will be given in order to compare the suggested circuit performance with traditional designs.

The current chapter introduces the proposed Modified Decap-Assisted Sense Amplifier (MDASA), and discusses the concept of the proposed MDASA along with its advantages. Section 4.1 describes the research problem and gives an introduction about the proposed MDASA architecture. The performance requirements for next generation sense amplifiers are described in Section 4.2. These include the need for high sensing sensitivity, minimum propagation delay, low power consumption during standby, and immunity against capacitive loading. Section 4.3 highlights some of the drawbacks related to traditional low voltage sensing concepts, including excessive area overhead, voltage threshold loss, slower latching speed, complex circuitry, and susceptibility to noise. Section 4.4 describes the architecture of the proposed MDASA, which includes the circuit structure, transistor placement, capacitor placements, and output generation circuitry. Section 4.5 elaborates on the complete functioning process of the MDASA, including the phases of pre-charge, bit-line

development, decap-assisted activation, differential amplification and output generation. Section 4.6 outlines some of the major benefits offered by the proposed architecture, including reduced delay and Power-Delay Product (PDP). The practical applications of the designed circuit for high-speed cache memories, portable electronic devices, artificial intelligence accelerators, Internet of Things (IoT) technology, biomedical sensors, and automotive electronics are described in section 4.7. Lastly, section 4.8 describes the important observation made from this research and how the direct connection of the decoupling capacitors to the bit-lines makes it possible to attain high speed and low power dissipation at the same time.

4.2 Performance Requirement of Next-Generation Sense Amplifiers

Before exploring the detailed circuit diagram of the proposed architecture it is essential to analyze the strict performance requirements that modern sensing networks must satisfy. As semiconductor technology scales down to nanoscale levels, memory circuits must meet very harsh design rules. A sense amplifier is no longer just a simple helper circuit. It is a critical component that determines the speed and power budget of the entire processor chip. To operate successfully inside modern high-density memory arrays a next-generation sense amplifier must satisfy several primary performance conditions simultaneously.

4.2.1 High Sensing Sensitivity

In the SRAM read operation, the memory cell produces only a small differential voltage across the bit-lines prior to the actual sensing process. Such a small signal tends to be quite small and hard to discern. This is why the modern sense amplifier needs to have high sensitivity in order to properly discriminate the small differential voltage. In the case where the sensing ability is low, the circuit would generate an erroneous output data. Besides that, the sense amplifier needs to maintain stability throughout its operation; that means it shouldn't be sensitive to mismatch effects in transistor characteristics.

4.2.2 Minimum Propagation Delay

Propagation delay is an important parameter that determines how quickly data can be read from memory. It is the time required for the sense amplifier to convert a small input voltage difference into a complete digital output signal. Modern processors require very fast memory access for high-speed operation. Therefore the transistors inside the sense amplifier must switch quickly and provide strong current driving capability. If the sensing circuit takes more time to respond the overall memory performance becomes slower and reduces processor speed.

4.2.3 Low Standby Power Overhead

Modern portable devices, such as smartphones, smartwatches, and laptops, spend a massive amount of time in an idle or standby state. Even when a device is not actively running an application the memory chip remains powered on to preserve the stored

data. During this idle time, transistors naturally suffer from subthreshold leakage currents, which constantly drain battery life. A next-generation sense amplifier must incorporate advanced gating techniques to completely shut off internal current paths when data is not being read. Minimizing this static power consumption is crucial for extending the battery life of modern electronics.

4.2.4 Immunity to Capacitive Loading

In a high-density memory chip, hundreds of individual SRAM cells are stacked vertically in a single column, and all of them share the same pair of long bit-lines. These long metal wires possess a massive amount of parasitic capacitance. When the sense amplifier activates this heavy capacitive load behaves like a heavy weight that slows down the internal switching speed of the transistors. A truly efficient sense amplifier must find a way to isolate its internal switching nodes from this massive external capacitance. Achieving high immunity to loading ensures that the memory maintains its ultra-fast speed regardless of how large or long the memory column becomes.

4.3 Limitations of Conventional Low-Voltage Sensing Techniques

Traditional voltage-mode sense amplifiers rely on basic design adjustments to handle scaling challenges. Designers usually try to solve memory reading problems by changing transistor sizes adding simple isolation switches or increasing internal bias currents. However, when these conventional circuits operate under low supply voltages, these simple techniques create new engineering bottlenecks. Simply modifying old structures is no longer enough for advanced memory chips because fixing one performance parameter always ruins another.

4.3.1 Transistor Sizing and Area Overhead

The most common way to increase the speed of a slow sense amplifier is to increase the width of its internal transistors. While wider transistors provide higher current drive strength they create two massive issues in low-voltage layouts. First, larger transistors require a much bigger silicon area, which increases manufacturing costs and reduces the density of the memory chip. Second, expanding transistor sizes heavily inflates the internal input capacitance of the amplifier. This extra capacitance loads down the memory lines causing the initial bit-line discharge to become even slower and defeating the original purpose of sizing up the devices.

4.3.2 Threshold Voltage Drops and Slow Latching

In cases where the supply voltage (V_{DD}) is lowered in order to lower power consumption, the sense amplifier transistors become weak since the threshold voltage does not drop as fast. Therefore, the circuit will have low driving capability, leading to a slow sense operation. In the case of cross coupled latches that use positive feedback, the feedback mechanism starts working later on compared to other mechanisms. This makes the sense amplifier operate slowly.

4.3.3 Complexity of Isolation Networks

Most of the normal sense amplifier circuits make use of isolation switches in between the bit lines and the internal latch in order to decrease the influence of the capacitance present on the bit lines. Even though this is an effective approach in minimizing capacitive loads, it makes the circuit more complicated. The added switches need precise control and timings in order for their correct functioning. If not timed correctly, the circuit may be unable to respond to the input signal. The presence of additional switches also causes voltage drop at low supply voltage.

4.3.4 Dynamic Noise and Sensitivity Mismatch

Conventional low-voltage sensing techniques are highly vulnerable to process-voltage-temperature (PVT) variations and random manufacturing mismatches. In advanced, small-scale CMOS technologies even a tiny physical variation between two side-by-side transistors creates a significant threshold voltage mismatch. In a standard cross-coupled amplifier operating at low voltages, this mismatch creates a large internal offset voltage. Because the input signal from the SRAM cell is already very weak, this offset noise can easily overpower the actual data signal causing the sense amplifier to make a false binary decision and flip the data incorrectly.

4.4 Modified Decap-Assisted Sense Amplifier (MDASA)

The Modified Decap-Assisted Sense Amplifier (MDASA) is a modified sense amplifier that relies on the improved circuit design that enhances the sensing time of memories. In MDASA, there is the direct connection of bit lines BL and BLB to decoupling capacitors within the circuit. The decoupling capacitors function with parallel transistors to minimize the impact of bit line capacitance. Therefore, the sense amplifier performs faster sensing and improves performance during the read cycles of memories. The complete circuit structure and node connections of the proposed MDASA are shown in Fig. 4.1.

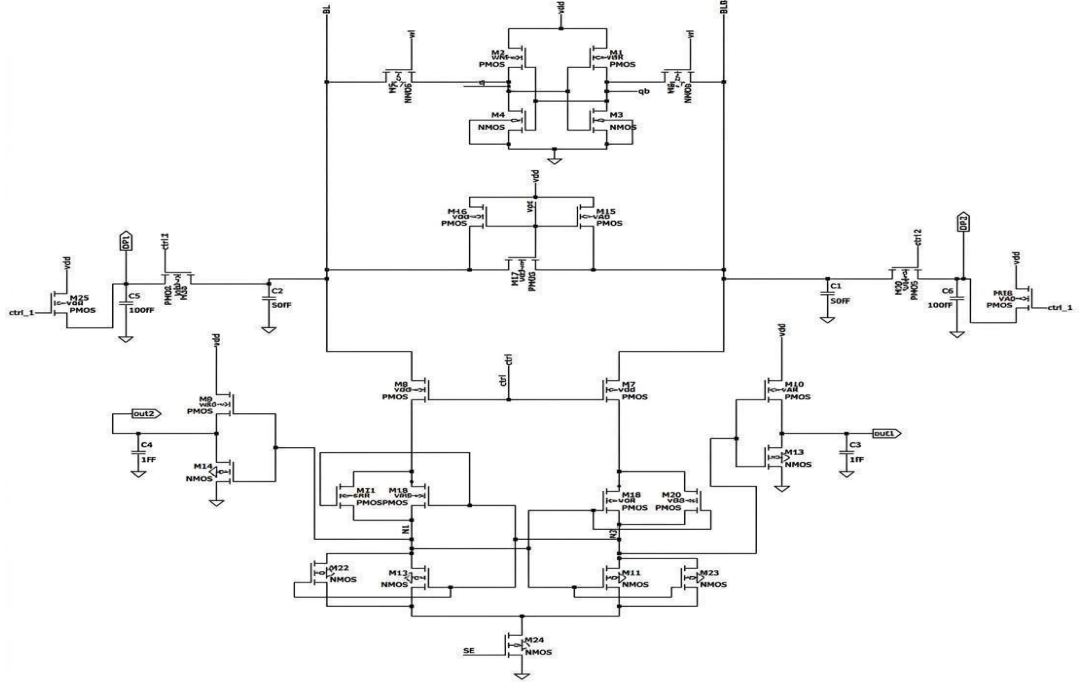


Fig. 4.1 Schematic of MDASA

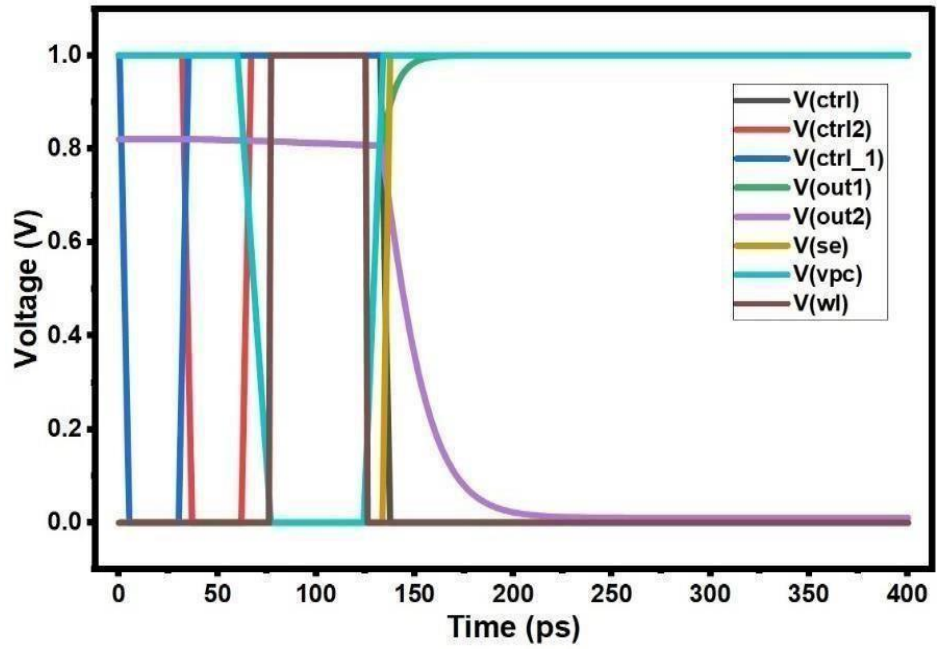


Fig. 4.2 Transient Response of Modified Decap-Assisted Sense Amplifier

4.4.1 Core Regenerative Latch Network

In the core of the proposed circuit lies a cross-coupled latch circuit composed of two inverters made using CMOS technology. The latch circuit includes two PMOS transistors and two NMOS transistors that assist in switching the circuit on from VDD level to ground level. One inverter circuit is connected with the input of another inverter circuit in such a way that each circuit gets its input from another inverter. This makes the circuit form a very powerful positive feedback system. A switch is placed close to the ground connection to prevent unnecessary loss of power due to leakage current.

4.4.2 Direct Bit-Line and Decoupling Capacitor Interconnection

Another significant aspect about the MDASA is the direct relationship between the decoupling capacitors and the bit-lines BL and BLB. Decoupling capacitors are created by employing tiny MOS transistors to minimize space usage on the chip. In the pre-charge phase, these capacitors charge up using the charge from the bit-lines. When the sense phase begins, the already charged up decoupling capacitors aid the sensing process due to their ability to facilitate the tiny voltage generated in the bit-lines.

4.4.3 Parallel Transistor Paths and Driving Strength Boost

For faster sensing operation, the MDASA makes use of extra NMOS and PMOS transistors in parallel. The effect of using additional parallel transistors is that there are many parallel current paths made along with the connection paths of the decoupling capacitors. Once the sense enable input is asserted high, the parallel transistors conduct and give rise to good amount of current in the circuit. The circuit thus works more effectively for sensing the voltage difference.

4.4.4 Evaluation Nodes and Output Buffer Isolation

The MDASA consists of two internal sensing nodes, which are called the true sensing node and the complementary sensing node. These sensing nodes get the voltage difference of the bit-lines helped by capacitors, and assist in creating the final output signal digitally. The final output signals go through buffer inverters in order to protect the internal circuit from noise caused externally, as well as large output capacitance. This helps keep the internal latch insulated from external data lines and maintains strong and fast output signals.

4.5 Working of MDASA

The function of the suggested MDASA circuit involves various stages of operations. Each stage works properly in a proper order following clock and enable signals. In the course of operation, the circuit will be engaged in performing operations related to sensing, boosting, and amplification, etc., one after another. The decoupling capacitor and parallel transistor path will assist the circuit to detect data effectively.

4.5.1 Pre-charge Phase

the initiation of the active reading process, complementary bit-lines BL and BLB are pre-charged to the complete supply voltage VDD. During this idle stage, the main sense amplifier stays disconnected from the circuit since it is not needed at this stage, and moreover, it might cause any wastage of energy as well as disturb the memory cells stored data. Concurrently, control signal #1, i.e., CTRL1, is switched on to create a charging path between internal decoupling capacitors and power lines. Through this, decoupling capacitors can be charged up with electrical energy.

4.5.2 Bit-line Development Phase

The bit-line development stage begins when the word line WL of the selected SRAM cell gets activated and goes high. This activation results in the connection of the storage nodes of the SRAM cell with the pre-charged bit-lines using the access transistors. Depending on the data content in the cell, one of the bit-lines will start discharging gradually towards ground, whereas the other will remain at VDD.

4.5.3 Decap-Assisted Activation Phase

When there is an initial voltage difference on the bit line, the circuit enters into decap assisted activation mode that is the primary focus of this particular design. The control signal CTRL1 is OFF at this instant, allowing the decoupling capacitors to be disconnected from the power source. The other control signal, CTRL2 then turned ON. The result of turning ON the control signals results in the release of stored energy in the decoupling capacitors to the sense node path. The proximity of the decoupling capacitors to the sense node path allows for the charging of the voltage.

4.5.4 Differential Amplification Phase

The cross-coupled latch design becomes operational when the first voltage differential is boosted. The presence of a smaller voltage differential within the system leads to an unequal distribution of currents, hence disrupting the symmetry of the electrical connection and initiating the process of positive feedback. As a result, the node having a slightly higher voltage will go from the previous state to logic level 1 while the remaining node falls to logic level 0. For this purpose, the parallel transistors get activated and offer several low impedance paths for current flow within the circuitry system.

4.5.5 Output Generation Phase

In the last stage of the circuit, the process of output generation starts wherein the stored binary value is fed into the output circuit. The differential outputs from the sensing nodes are fed into two buffer inverters for output generation. The output buffer inverters have mainly two roles. Firstly, they ensure a high amount of current is supplied to create well-defined transition levels in the output signal. Secondly, they ensure isolation of the cross coupled latch from any external disturbance.

Following full amplification of the bit line voltage difference, the output values become stable.

4.6 Advantages of the Proposed MDASA Architecture

The combination of local decoupling capacitors and parallel transistor paths provides the proposed MDASA with several important advantages compared to conventional voltage mode sensing designs.

- 1. Low Propagation Delay:** By utilizing the local charge injection from the decoupling capacitors, the internal nodes receive an instant voltage boost. This forces the cross- coupled latch to break its electrical balance almost immediately drastically cutting down the time it takes to generate a digital output.
- 2. Superior Energy Efficiency (Optimized PDP):** Even though the architecture incorporates extra transistors and capacitors, it operates purely through transient switching. Because these components only draw power during brief switching intervals and consume zero direct current (DC) during steady states, the massive reduction in delay easily compensates for the minor power overhead. This results in a highly optimized Power-Delay Product (PDP).
- 3. High Immunity to Bit-Line Capacitance:** In large memory columns long metal wires create heavy parasitic capacitive loading. The parallel transistor network in the MDASA acts as a smart isolation barrier that prevents this heavy external load from directly weighing down the internal switching latch, ensuring high speed regardless of the memory column size.
- 4. Robust Low-Voltage Stability:** When the supply voltage (VDD) is lowered to save battery life, conventional latches become sluggish and unstable. The MDASA maintains robust operation under aggressive voltage scaling because the local capacitors stabilize the internal nodes and prevent local voltage sags during active evaluation.
- 5. Reduced Sensitivity to Process Variations:** Random manufacturing variations in nanoscale CMOS technology often cause threshold voltage mismatches between transistors. The additional charge provided by the decoupling capacitors expands the differential sensing margin preventing external noise or device mismatches from flipping the data incorrectly.

4.7 Applications of the MDASA

Due to its high tracking speed, low voltage requirements, and excellent energy efficiency, the proposed MDASA is highly suitable for a wide variety of modern VLSI systems. Its primary applications include:

- 1. High-Speed CPU Cache Memories:** Modern microprocessors rely heavily on ultra- fast Level 1 (L1), Level 2 (L2) and Level 3 (L3) internal cache arrays. Because

the MDASA executes rapid rail-to-rail transitions within a fraction of a nanosecond, it can easily match the high clock frequencies of modern central processing units.

2. Low-Power Mobile and Portable Electronics: Smartphones, smartwatches, tablets, and laptops require memory architectures that drastically limit power consumption to extend battery life. The MDASA is an ideal candidate for these devices because of its low standby leakage current and optimized energy consumption during active read cycles.

3. Deep Learning and Artificial Intelligence Accelerators: Hardware accelerators used for AI and deep learning handle very large amounts of data continuously and need fast memory access along with high processing bandwidth. The MDASA supports these high density workloads by delivering clean stable and fast signal outputs even under heavy data traffic.

4. Internet of Things (IoT) and Biomedical Sensors: IoT edge devices and wearable health monitors operate in energy-constrained environments often running on small batteries or harvested ambient energy. The robust low-voltage functionality of the MDASA allows memory blocks to operate reliably at near-subthreshold voltage limits.

5. High-Density Automotive Electronics: Advanced Driver Assistance Systems (ADAS) and autonomous driving chips require memory components that offer absolute data reliability under varying temperatures and environmental noise. The high noise immunity and stable output characteristics of the MDASA ensure safe and error-free memory operations in automotive processing cores.

4.8 The Key Observation of the Work

In all the previously considered conventional sense amplifiers (such as LTSA, CCVSA or DIPSA) it is not possible for a circuit to be both fast and have low power consumption; one has to give up on one of them, if one needs the other. This study shows that by connecting internal decoupling capacitors directly to the bit-lines, the system is capable of catching and boosting a small signal locally. Since the capacitors as well as transistor networks connected to them act as temporary switches, a tremendous current boost is achieved during evaluation phase without continuous current consumption while idle. The main result of this study is achieving unusually small propagation delays with great energy efficiency and low leakage at the same time.

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CHAPTER – 5

COMPARISON OF DESIGNED SENSE AMPLIFIER MDASA WITH OTHER EXISTING SENSE AMPLIFIERS

5.1 Introduction

In recent times, sense amplifiers have become a crucial component in digital circuits and SRAM memory circuits. On reading the information from a storage cell, a very small difference voltage appears on the bit line which is very long and heavily loaded. The sense amplifiers are used to identify the slight voltage difference and convert it to either 0 or 1 binary signals. With the reduction in process technologies to nanometer levels, there arise many issues in designing an effective sense amplifier due to factors such as transistor mismatch, higher leakages and reduced speed, particularly with lower supply voltages. To solve the above issues and design an improved sense amplifier, MDASA is designed and tested in this thesis. This novel circuit is intended to achieve improved speed, reduced power dissipation and reliable signal detection. Though the design of the circuit is good on paper, it needs to compare itself against existing designs to validate the claims made by its designer. Hence the need for performance evaluation arises.

The key purpose of this chapter is the comparative analysis between the MDASA proposed circuit design and other existing sense amplifiers designs. To ensure fairness in comparison the design parameters remain the same for each circuit. The simulation will be done using the same 45 nm CMOS technology, same range of supply voltage, same temperature and the same bit line capacitance for every design. Using the same parameters allows the accurate measurement of the difference in performance of MDASA. The performance of each sense amplifier will be tested using three parameters. Firstly the sensing delay time will be compared, which measures the speed of operation of the circuit. Secondly power consumption will be analyzed, which includes active and leakage power. Thirdly, Power Delay Product of the circuit will be calculated, which determines the energy efficiency of the circuit.

In this chapter, the analysis of the performance of the newly designed MDASA scheme will be discussed systematically. Initially, Sections 5.2 & 5.3 deal with the performance analysis of the electrical properties in terms of delay and power consumption of MDASA along with comparison against other designs at constant bit line capacitance, i.e., 50fF under various voltage supplies. Secondly, Sections 5.4 & 5.5 deal with power efficiency and standby analysis respectively through evaluation of power delay product and leakage current, respectively. Further, Sections 5.6 & 5.7 are dedicated to scalability analysis of MDASA circuit as a result of increase in bit line capacitance from 50fF to 250fF. Lastly, Sections 5.8 & 5.9 deal with performance analysis in terms of speed and energy of the circuit under various operating conditions.

5.2 Delay Analysis Under Supply Voltage Variation at 50fF Bit-Line Capacitance

This section presents a detailed comparative evaluation of the sensing delay for the proposed MDASA against five existing sense amplifier topologies: DIPSA, TGSA, CCVSA, LTSA and PLTSA. The simulations were carried out by varying the supply voltage from 0.7V to 1.2V while keeping the bit-line load capacitance strictly fixed at a standard value of 50fF. The captured quantitative data is organized below in Table 5.1.

5.1 Delay Analysis under Supply Voltage Variation at 50fF Bit-Line Capacitance

Sense Amplifier	Delay (ns)			
	0.7V	0.9V	1V	1.2V
MDASA	0.07485	0.0704	0.06835	0.06639
DIPSA	0.390	0.3639	0.368	0.3513
TGSA	2.21	2.1	2	1.90
CCVSA	1.80	1.63	1.58	1.50
LTSA	1.58	1.561	1.54	1.53
PLTSA	1.27	1.28	1.28	1.26

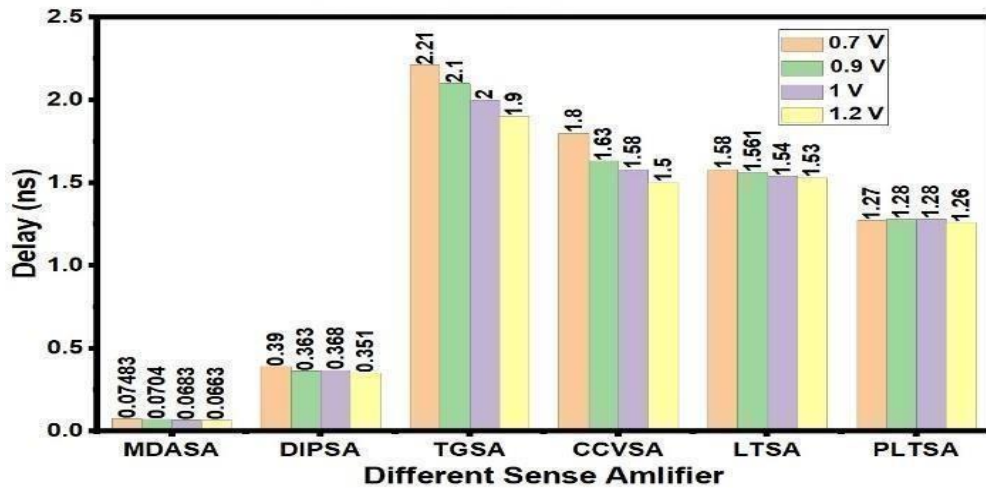


Fig. 5.1 Delay Comparison of Various Sense Amplifiers with Supply Voltage Variation

1. Overall Performance Superiority of MDASA: The proposed MDASA exhibits the lowest sensing delay across the entire supply voltage spectrum (0.7V to 1.2V). For instance, at the nominal operating voltage of 1.0V, the MDASA achieves an ultra-fast sensing delay of just 0.06835 ns. Compared to the slowest architecture (TGSA at 2.0 ns) and even the closest competing architecture (DIPSA at 0.368 ns) the MDASA operates significantly faster. This massive speed boost proves that the internal modifications made to the MDASA allow it to evaluate bit-line signals much quicker than conventional designs.

2. Impact of Supply Voltage Scaling on Delay: As the supply voltage increases from 0.7V to 1.2V, a universal trend is observed where the sensing delay decreases for almost all designs. This happens because a higher supply voltage increases the gate- to-source voltage of the internal transistors. This higher voltage boosts the driving current allowing the transistors to charge and discharge the output nodes at a faster rate. For example, the delay of CCVSA drops from 1.80 ns to 1.50 ns and TGSA drops from 2.21 ns to 1.90 ns.

3. Ultra-Low Voltage Robustness (At 0.7V): Ultra-low-voltage operation at 0.7V implies that the circuit can operate with ultra-low voltage which makes it capable of reducing energy consumption. In normal circumstances, circuits operating at ultra-low voltage have poor performance due to the slow behavior of transistors, resulting from their operating at near-threshold voltage. Nevertheless, the presented MDASA copes well with this situation. The slight increase in delay time to 0.07485ns indicates good speed retention capabilities of the circuit. Conventional circuits such as TGSA and CCVSA have high delay times of 2.21ns and 1.80ns respectively, making them unsuitable for use in applications requiring high speed and low power consumption.

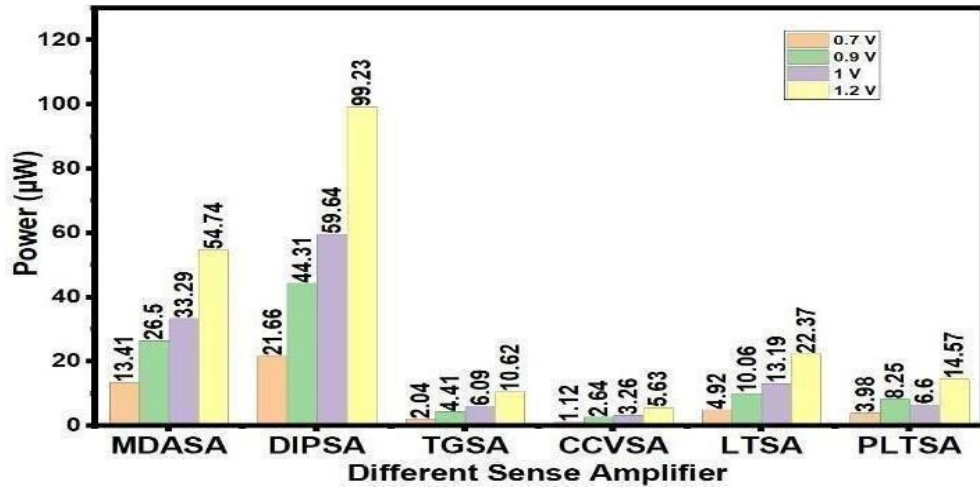
4. Stability and Performance Consistency: From these findings, it has been proven that MDASA exhibits stable delay characteristics as compared to variations in voltages. There are very minimal changes in delays, ranging between 0.008ns at different ranges of voltages, from 0.7V up to 1.2V. It means that the performance is maintained despite the application of different voltages. However, conventional designs exhibit unstable delays or have no increase in speed in terms of delays. For instance, PLTSA remains stable, maintaining a delay of around 1.27ns-1.28ns. It means that its speed will not be improved with an increase in voltage application.

5.3 Power Analysis Under Supply Voltage Variation at 50fF Bit-Line Capacitance

This section evaluates the total power consumption of the proposed MDASA and compares it with the five existing sense amplifier designs (DIPSA, TGSA, CCVSA, LTSA and PLTSA). The power dissipation for all circuits was measured across a supply voltage range of 0.7V to 1.2V while maintaining a constant bit-line load capacitance of 50fF. The recorded data from these simulations is summarized below in Table 5.2.

Table 5.2: Power Consumption (μW) Comparison at 50fF Bit-Line Capacitance

Sense Amplifier	Power (μW)			
	0.7V	0.9V	1V	1.2V
MDASA	13.41	26.50	33.29	54.74
DIPSA	21.66	44.31	59.64	99.23
TGSA	2.04	4.41	6.09	10.62
CCVSA	1.12	2.64	3.26	5.63
LTSA	4.92	10.06	13.19	22.37
PLTSA	3.98	8.25	6.60	14.57

**Fig. 5.2** Power Comparison of Various Sense Amplifiers with Supply Voltage Variation

1. The Core Trade-off Between Speed and Power: A direct comparison with the delay data from Section 5.2 shows a classic VLSI design trade-off. While the proposed MDASA operates exponentially faster than conventional architectures like CCVSA and TGSA, it consumes more power. For example, at a nominal 1.0V supply, MDASA consumes 33.29 μW whereas CCVSA consumes only 3.26 μW . This happens because MDASA uses specialized, high-speed latching mechanisms that draw more current to pull the output nodes to full rail-to-rail logic levels instantly.

2. Massive Power Savings Compared to DIPSA: Even though MDASA consumes more power than the slow conventional circuits, it achieves outstanding energy efficiency when compared to DIPSA which is its only real competitor in terms of sub-

nanosecond speed. Across the entire voltage range, MDASA cuts power consumption almost in half compared to DIPSA. At 1.2V, DIPSA spikes up to a massive 99.23 μW while MDASA consumes only 54.74 μW . This proves that MDASA is heavily optimized to deliver high-speed performance without suffering from the extreme power penalties seen in other advanced topologies.

3. Impact of Supply Voltage Scaling on Power: For every sense amplifier in the table power consumption increases rapidly as the supply voltage scales up from 0.7V to 1.2V. In digital CMOS circuits, dynamic power consumption is directly proportional to the square of the supply voltage. Consequently, as VDD increases, charging the internal capacitances demands drastically more energy. For instance, the power of MDASA increases from 13.41 μW at 0.7V to 54.74 μW at 1.2V.

4. Low-Voltage Power Efficiency: When operating at a low-power constraint of 0.7V, MDASA drops its power footprint down to just 13.41 μW . Combined with the fact that it maintains an ultra-low delay of 0.07485 ns at this specific voltage, operating the MDASA at 0.7V serves as an ideal sweet spot for battery-powered or energy- constrained applications.

5.4 Power-Delay Product Analysis Under Supply Voltage Variation at 50fF Bit-Line Capacitance

This section evaluates the Power-Delay Product (PDP) of the proposed MDASA and compares it with the five existing sense amplifier topologies. The PDP serves as a primary figure of merit in energy-efficient VLSI design, as it mathematically combines both operational speed and power consumption to reflect the overall energy efficiency per cycle. The PDP values were calculated across a supply voltage range of 0.7V to 1.2V with a fixed bit-line capacitance of 50fF. The quantitative results are organized below in Table 5.3.

Table 5.3: Power-Delay Product (fJ) Comparison at 50fF Bit-Line Capacitance

Sense Amplifier	PDP (fJ)			
	0.7V	0.9V	1V	1.2V
MDASA	1.003	1.866	2.273	3.634
DIPSA	8.46	16.084	21.947	34.861
TGSA	4.508	9.261	12.18	20.178
CCVSA	2.016	4.303	5.157	8.445
LTSA	7.78	15.69	20.31	34.22
PLTSA	5.05	10.56	8.448	18.35

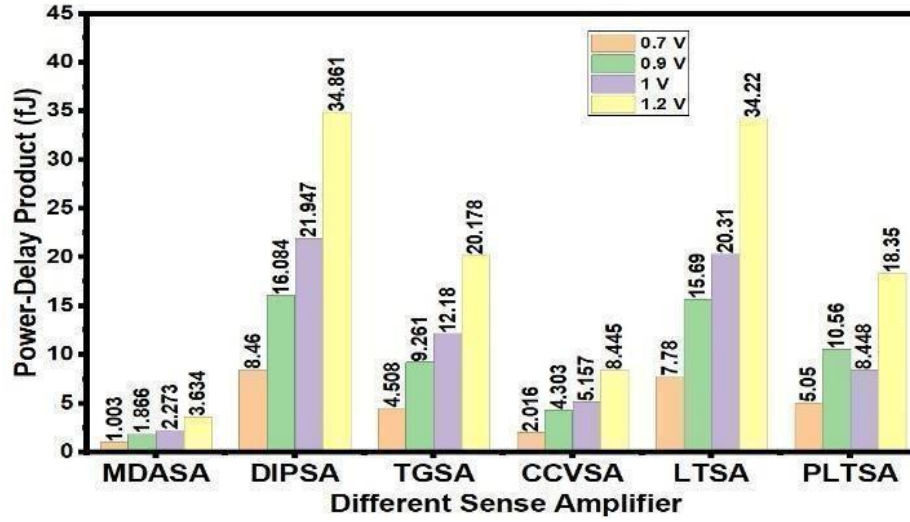


Fig. 5.3 Power–Delay Product Comparison of Sense Amplifiers Under Supply Voltage Variation

1. Absolute Energy Efficiency of MDASA: MDASA circuit has the least power delay product throughout the entire range of supply voltage values varying from 0.7V to 1.2V. For instance, its power delay product at 1.0V voltage is just 2.273 fJ. This is significantly smaller when compared to other high-speed design DIPSA with its power delay product of 21.947 fJ at 1.0V. Despite that MDASA utilizes more raw power than other traditional circuit such as CCVSA, the latter's exceptionally fast performance leads to lesser energy consumption per switching cycle. That is why MDASA emerges as the most energy efficient circuit design.

2. Impact of Supply Voltage Scaling on Energy: As the supply voltage rises from 0.7V to 1.2V, there is also an increase in the PDP for all circuits. The reason behind this is that power increases exponentially with voltage while speed increases linearly due to the decreasing delay. The PDP of the MDASA circuit for instance rises from 1.003 fJ at 0.7V to 3.634 fJ at 1.2V. It clearly illustrates an increasing trend which indicates that circuits should be operated at lower voltages for energy conservation.

3. Exceptional Performance in Ultra-Low Voltage Domain (0.7V): The proposed MDASA works extremely well when the supply voltage used is extremely low at 0.7V to provide an impressive power delay product value of 1.003 fJ. When compared to conventional systems, MDASA is far better at this voltage level. While the power delay products of LTSA and DIPSA are 7.78 fJ and 8.46 fJ respectively, MDASA can operate well under near threshold operation conditions without using a lot of energy.

4. Comparative Advantage Over Existing Topologies: Based on energy efficiency ranking of the results, it is found that MDASA and CCVSA are the most energy-efficient circuit designs among the circuits evaluated. Others include TGSA, PLTSA, LTSA, and DIPSA which are all very high on their power-delay product. Therefore, they take a lot more energy to work. Take the case of DIPSA for instance, at 1.2V it takes almost 9 times the amount of energy MDASA takes to operate. It takes almost 35 fJ while MDASA takes about 3.634 fJ per operation.

5.5 Leakage Current Analysis Under Supply Voltage Variation at 50fF Bit-Line Capacitance

In this section, comparison of the standby leakage current of the suggested MDASA is performed against five different sense amplifier circuits that exist in the literature. In smaller-sized transistors, as they approach nanometer dimensions, sub threshold leakage and gate oxide leakage become the main sources of power dissipation, particularly when the memory is in idle state. For comparing the leakage currents of all sense amplifiers, their supply voltages were varied between 0.7V to 1.2V while maintaining the bit line capacitor constant at 50fF. The simulation results for this idle condition are presented in Table 5.4.

Table 5.4: Standby Leakage Current (pA) Comparison at 50fF Bit-Line Capacitance

Sense Amplifier	Leakage Current (pA)			
	0.7V	0.9V	1V	1.2V
MDASA	29.84	38.48	40.83	50.98
DIPSA	23.50	55.03	84.80	215.60
TGSA	12.88	16.84	15.88	22.2
CCVSA	10.02	12.83	11.84	17.32
LTSA	12.91	16.95	15.88	23.23
PLTSA	15.67	20.26	20.62	26.84

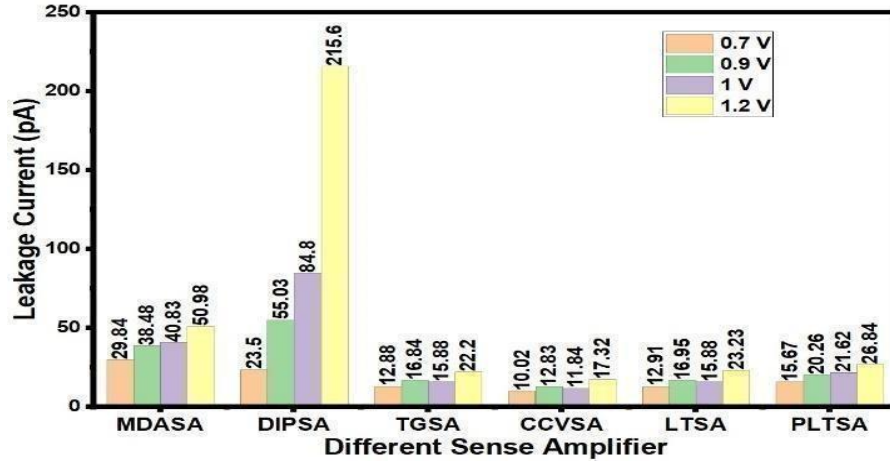


Fig. 5.4 Leakage Current Comparison of Different Sense Amplifiers at Various Supply Voltage Variation

1. The Major Success of MDASA over DIPSA: The most important finding is the comparison between MDASA and DIPSA. Both are advanced, high-speed architectures but DIPSA fails heavily in power saving, wasting a massive 21,560 pA at 1.2V. The proposed MDASA keeps leakage extremely low at just 50.98 pA under the exact same condition. This means MDASA provides modern high-speed performance while successfully eliminating the massive standby power waste seen in other recent designs.

2. A Fair Trade-off with Basic Conventional Circuits: Traditional circuits like CCVSA and TGSA maintain the absolute lowest leakage numbers (around 11 pA to 15 pA at 1.0V) because they use a very minimal number of transistors. The proposed MDASA shows a slightly higher leakage (40.83 pA at 1.0V) than these oldest models. However, this tiny increase in picoamperes is a highly acceptable engineering trade-off because MDASA operates exponentially faster and saves much more total energy when active.

3. Universal Impact of Supply Voltage Scaling: For every single sense amplifier in the table, the leakage current increases steadily as the supply voltage grows from 0.7V to 1.2V. This occurs because higher voltage increases the drain-to-source stress across the turned-off transistors forcing more unwanted current to leak through. For example, the leakage of MDASA increases from 29.84 pA at 0.7V to 50.98 pA at 1.2V.

4. Ideal for Standby-Heavy Devices: At an ultra-low supply voltage of 0.7V, the MDASA drops its static power loss to a negligible 29.84 pA. This proves that the proposed design is exceptionally reliable for battery-operated systems such as smartphones or IoT sensors where the memory remains in idle/standby mode for long intervals and demands a minimal power drain.

5.6 Impact of Bit-Line Capacitance on Power Consumption

increasing the value of bit-line capacitance from 50fF to 250fF results in increased power dissipation of most sense amplifier circuits due to increased energy required to charge greater capacitance loads. As we can see in the table 5.5. For instance, for 1.0V supply voltage, the power consumed by the proposed MDASA increases from 33.43 μ W for 50fF to 41.81 μ W for 250fF and the power dissipated by its chief competitor – DIPSA – rises from 59.64 μ W to 71.70 μ W. On the other hand, the traditional designs of TGSA and CCVSA exhibit the reverse behavior since their power dissipation decreases as the value of bit-line capacitance increases. This is caused by poor response speed of such designs under heavy loading conditions.

Table 5.5 Impact of Bit-line Capacitance on Power Consumption

CBL (fF)	Voltage (V)	Power Consumption (μ W) of Different Sense Amplifiers					
		MDASA	DIPSA	TGSA	CCVSA	LTSA	PLTSA
50	0.7	12.75	21.66	2.09	1.12	4.92	3.98
	0.9	26.68	44.31	4.41	2.68	10.06	8.25
	1	33.43	59.64	6.09	3.26	13.19	6.63
	1.2	56.6	99.23	10.62	5.63	22.37	14.57
75	0.7	13.63	22.77	1.90	1.06	5.51	4.28
	0.9	28.95	47.56	4.17	2.27	11.11	4.87
	1	35.2	64.62	5.79	3.12	13.33	11.59
	1.2	62.89	109.35	10.02	5.43	24.13	19.72
100	0.7	14.11	23.33	1.77	1.03	6.09	4.57
	0.9	30.27	49.25	3.94	2.16	12.46	5.41
	1	38.2	67.25	5.50	2.99	15.4	12.17
	1.2	66.5	114.83	9.77	5.24	23.90	20.62
250	0.7	15.65	24.34	1.282	0.75	8.92	5.95
	0.9	32.90	52.98	2.93	1.673	17.07	8.20
	1	41.81	71.70	4.16	2.34	21.76	9.95
	1.2	73.98	124.3	6.36	4.23	36.09	25.69

Raising the supply voltage from 0.7V to 1.2V brings about a significant increase in power dissipation for all sense amplifier architectures in the above table. Power dissipation in a digital circuit is proportional to the square of the supply voltage. Therefore, an increase in voltage will cause a rise in power dissipation very quickly in all the test cases. Compared to the other architecture, the proposed MDASA architecture is highly power efficient compared to the DIPSA architecture in all the test cases. With 250fF capacitance and a supply voltage of 1.2V, the power dissipation by DIPSA and MDASA is 124.35 μ W and 73.98 μ W, respectively.

5.7 Impact of Bit-Line Capacitance on Delay

The data in the table 5.6 shows that as the bit-line capacitance increases from 50fF to 250fF, the sensing delay of most amplifiers increases because larger capacitance creates a heavier load that takes more time to charge and discharge. For example, at a

fixed supply voltage of 1.0V, the delay of DIPSA increases from 0.358 ns (at 50fF) to 0.412 ns (at 250fF) while the conventional TGSA slows down from 2.00 ns to 2.02 ns. In contrast, the proposed MDASA shows outstanding resistance to this capacitive loading effect. At 1.0V, its delay changes by less than 0.004 ns (from 0.067 ns to 0.0706 ns) proving that its internal architecture is highly stable and does not degrade significantly when attached to long, heavily loaded memory bit-lines.

Table 5.6 Impact of Bit-line Capacitance on Delay

CBL (fF)	Voltage (V)	Delay (ns) of Different Sense Amplifiers					
		MDASA	DIPSA	TGSA	CCVSA	LTSA	PLTSA
50	0.7	0.07485	0.3908	2.1	1.80	1.58	1.27
	0.9	0.07044	0.3639	2.0	1.63	1.56	1.28
	1	0.067	0.358	2.0	1.58	1.54	1.28
	1.2	0.066	0.351	1.90	1.50	1.53	1.26
75	0.7	0.0757	0.410	2.22	1.80	1.58	1.28
	0.9	0.0713	0.374	2.05	1.62	1.56	1.28
	1	0.069	0.367	2.00	1.56	1.54	1.27
	1.2	0.067	0.359	1.91	1.48	1.53	1.27
100	0.7	0.0763	0.427	2.23	1.79	1.58	1.28
	0.9	0.0722	0.383	2.04	1.62	1.56	1.28
	1	0.069	0.373	2.00	1.56	1.54	1.27
	1.2	0.067	0.365	1.92	1.47	1.53	1.27
250	0.7	0.0772	0.507	2.29	1.76	1.58	1.31
	0.9	0.0737	0.424	2.02	1.62	1.56	1.25
	1	0.0706	0.412	2.00	1.36	1.54	1.24
	1.2	0.0688	0.396	1.94	1.47	1.53	1.28

The increase in the value of supply voltage from 0.7V to 1.2V decreases the sensing delay for all test cases as increased voltage means increased driving current which switches the transistor on and off much faster. In terms of total analysis, it can be stated that the performance of MDASA is superior to all other circuits as it shows the minimum value of sensing delay under all test cases. If we consider the minimum value of supply voltage which is 0.7V along with maximum value of the load of 250fF, then both the traditional circuits take more time for sensing with delay values 2.29ns and 1.76ns for TGSA and CCVSA respectively. However, MDASA senses at a very fast speed of just 0.0772ns which means that MDASA is about 29 times faster than TGSA.

5.8 Delay Variation of MDASA at Different Decoupling Capacitor Values and Different Supply Voltages

To study how the proposed design behaves under different conditions the circuit is tested with various operating settings. Table 5.7 shows how the sensing delay of the MDASA changes when the supply voltage and decoupling capacitor values are varied over different ranges.

1. Impact of Supply Voltage: The primary observation is that the sensing delay drops steadily as the supply voltage increases from 0.7 V to 1.2 V. For example, at a fixed capacitor value of 50 fF, the delay decreases from 75.51 ps at 0.7 V down to 66.28 ps at 1.2 V. This performance boost occurs because a higher supply voltage increases the driving current of the transistors, allowing them to switch states much faster.

Table 5.7: Delay variation of MDASA under varying supply voltages and decoupling capacitances

Supply Voltage (V)	Delay (ps) at Different Decoupling Capacitor			
	50 fF	75 fF	100 fF	250 fF
0.7	75.51	74.63	74.85	74.93
0.9	70.47	70.21	70.56	70.43
1.0	68.69	68.67	68.54	68.44
1.2	66.28	66.16	66.16	66.16

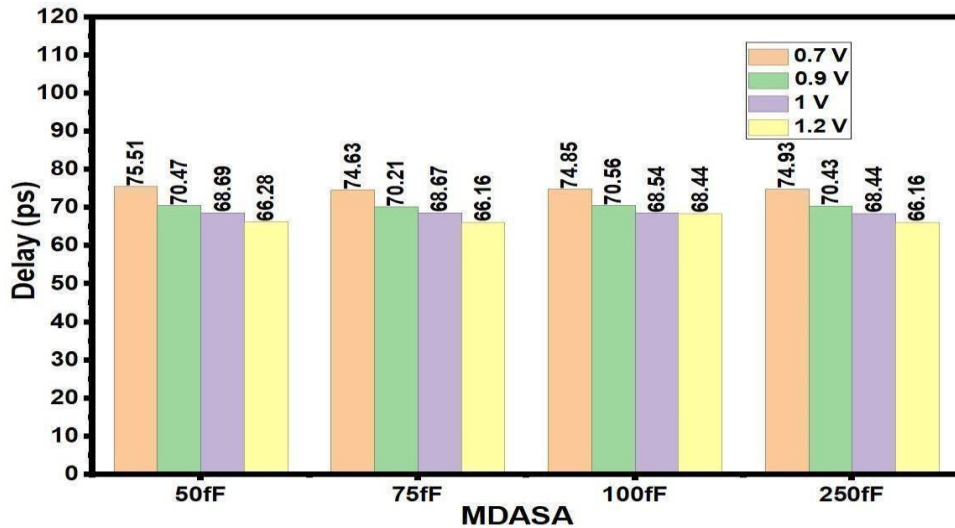


Fig. 5.5 Delay Comparison of MDASA with Varying Decoupling Capacitor Value

2. Impact of Supply Voltage: The primary observation is that the sensing delay drops steadily as the supply voltage increases from 0.7 V to 1.2 V. For example, at a fixed capacitor value of 50 fF, the delay decreases from 75.51 ps at 0.7 V down to 66.28 ps at 1.2 V. This performance boost occurs because a higher supply voltage

increases the driving current of the transistors, allowing them to switch states much faster.

3. Effect of Values for Decoupling Capacitors: On analyzing the results obtained one can see that there is hardly any difference in the sensing delay if the decoupling capacitor value is increased from 50 fF to 250 fF. For instance, when the voltage is set to 1.0 V, the sensing delay varies very slightly from 68.69 ps for 50 fF to 68.44 ps for 250 fF. In a similar way, the sensing delay is not affected if the voltage is kept at 1.2 V.

4. Key Technical Result: This result proves that the MDASA is highly stable and robust. This indicates that high performance is obtained from this circuit even if low capacitance values such as 50 fF or 75 fF are used. The use of higher capacitance, 250 fF, will not increase the speed of operation. Therefore, small capacitors should be preferred for saving on chip area.

5.9 Power Variation of MDASA at Different Decoupling Capacitor Values and Different Operating Voltages

In order to analyze the energy efficiency of the proposed architecture, the energy consumption of the circuit is analyzed by varying different parameters. The behavior of the energy consumption pattern is observed first, before proceeding further into the analysis of data. Table 5.8 illustrates the variation in active energy consumption of the MDASA with variations in supply voltage and decoupling capacitors.

Table 5.8: Power Variation of MDASA at Different Decoupling Capacitor Values and Different Operating Voltage

Supply Voltage (V)	Power (μ W) at Different Decoupling Capacitor			
	50 fF	75 fF	100 fF	250 fF
0.7	13.14	12.74	12.75	12.78
0.9	26.50	26.56	26.60	26.68
1.0	33.29	33.38	33.43	33.53
1.2	54.74	54.88	76.69	55.17

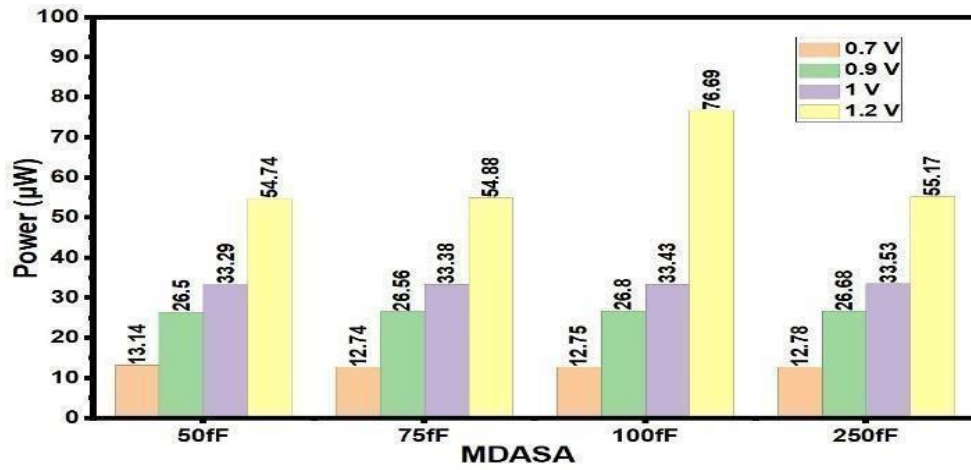


Fig. 5.6 Power Variation of MDASA at Different Decoupling Capacitor Values and Operating Voltage

1. Observation on Scaling of Supply Voltage: The key observation here is that power dissipation becomes high when there is a change in supply voltage from 0.7 V to 1.2 V. For instance, when the value of capacitance is 50 fF, the active power dissipated changes from 13.14 μ W to 54.74 μ W respectively from 0.7 V to 1.2 V.

2. Impact of Increase in Size of Decoupling Capacitor: From the above observations made for voltages of 0.7 V, 0.9 V, and 1.0 V, it is clear that there is negligible increase in power dissipation when the size of decoupling capacitor increases from 50 fF to 250 fF. The negligible increase in power dissipation reveals that decoupling capacitors are used only to store the charges.

3. Analysis of 1.2 V Spike: At the highest voltage of 1.2V, it can be seen that there is a spike in the power level of 76.69 μ W when the capacitance reaches 100 fF. The sudden surge may indicate an abrupt rise in the internal switching activities of the IC or a brief period of instability in operation at that particular voltage and capacitance level. Following this event, the power level drops off and stabilizes to around 55.17 μ W for a maximum of 250 fF capacitive load.

CHAPTER – 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

A modified decap-assisted sense amplifier MDASA is presented in this paper for faster and more energy-efficient SRAMs. It employs decap capacitors and parallel transistor paths for improved performance in SRAM sense operations. The performance of the MDASA design was analyzed and compared with those of other sense amplifiers such as DIPSA, TGSA, CCVSA, LTSA and PLTSA under various voltage conditions and bit-line capacitor values. From the simulation results obtained it can be noted that MDASA has much shorter sensing delay than other sense amplifiers architectures. The reduced sensing delay is a result of the charge assistance offered by decaps and better current drive by the parallel transistor network.

The MDASA architecture is also found to have reliable performance in different conditions. The sensing delay is almost unaffected despite the increase in the bit line and decap capacitor values. In respect to power consumption, the MDASA design is relatively moderate when compared to very high speed sense amplifiers such as DIPSA. While the power consumed is somewhat high in comparison with other low-power SRAMs, its performance cannot be overlooked considering the great improvements in speed made.

This architectural framework has proved its robustness and reliability at modern CMOS process technologies. Its sensing capabilities are maintained at the varying voltage and capacitance levels making it very useful in the practical implementation of SRAM systems. Decoupling capacitors ensure that the stability of the sensing nodes is ensured while lowering unwanted oscillations. When compared to the standard sense amplifiers MDASA has a better speed-power-stability tradeoff. For this reason MDASA is ideal for use in low-power devices cache memory and high-speed VLSI circuits.

6.2 Future Scope

While the proposed MDASA design shows excellent performance improvements, there are several promising ways to expand this research work in the future:

- 1. Silicon Layout Implementation:** The entire process of this analysis has been carried out using the simulation process of schematic design only. Further research can be done by implementing this circuit on a silicon chip to observe its performance in a practical environment.

2. SRAM Array Implementation: In this paper, we have considered only the sense amplifier block for evaluation. It will be worthwhile to extend this investigation to integrating MDASA in complete SRAM memory arrays, like 1Kb or 64Kb arrays, to observe its behavior in association with row decoders.

3. Advances in Transistor Technologies: The circuit has been modeled using conventional bulk CMOS technology. In future studies, we may consider modeling the MDASA circuit using new generation transistors such as FinFET or Gate all around FETs. The use of newer transistors will enhance speed and reduce energy consumption even more.

4. Automation with Machine Learning: Future work can use automated Machine Learning (ML) optimization algorithms to instantly tune the sizes of the internal transistors in the MDASA finding the absolute perfect balance between power, speed, and chip area automatically.

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LIST OF PUBLICATIONS

1. Mithun and P. Mittal, "Comparative Analysis of Sense Amplifier Designs at 45nm, 32nm and 22nm Technology Nodes," in *8th International Conference on Energy Systems Drives and Automations (ESDA)*, Bhubaneswar, India, Dec. 2025, Paper ID: 84, in press.



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Paper Title: Comparative Analysis of Sense Amplifier Designs at 45nm, 32nm, and 22nm Technology Nodes

Dear Mithun Tyagi

We are pleased to inform you that your paper has been accepted for presentation as Offline/Online in ESDA2025 which will be held during 27th (Offline) and 28th (Online) December 2025 in any Hotel, Bhubaneswar, Odisha, India. Hotel's name and address will be given later. After doing registration, the revised paper should be sent to esda.conference@gmail.com as a MS Word version. The paper's name should be as example: '84-ESDA2025-V2'. Please, don't send to multiple emails.

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Some papers from previous conferences, ESDA2019, ESDA2020, ESDA2021, ESDA2022, ESDA2023, ESDA2024 have been published in **SCIE indexed journals**, while other papers are published in **Lecture Notes in Electrical Engineering (LNEE) by Springer-Nature**, which is **SCOPUS indexed**.

2. Mithun and P. Mittal, "Comparative Analysis of Voltage-Mode Sense Amplifiers with Modified Decap-Assisted Precharge Technique," in *17th International Conference on Science and Innovative Engineering 2026 (ICSIE 2026)*, Apr. 2026, Paper ID: ICSIEDR2604167, ISBN: 978-81-69206-38-9.



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CURRICULUM VITAE/BRIEF PROFILE

MITHUN

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Education

Degree	Institute	CGPA/%
M. Tech(VLSI)	Delhi Technological University, New Delhi	8.26 CGPA
B.TECH(ECE)	G L Bajaj Institute of Technology, Gr Noida	8.2 CGPA
12 TH	R S M School, New Delhi	81%
10 TH	R S M School, New Delhi	8 CGPA

Academic Project

6T SRAM Layout

Designed a 6-transistor (6T) SRAM cell layout using Cadence Virtuoso in 90nm CMOS technology, ensuring proper cell symmetry. Performed Design Rule Check (DRC) to verify compliance with fabrication constraints and conducted Layout Vs Schematic (LVS) comparison to ensure functional accuracy between schematic and layout. Extracted parasitic resistance and capacitance (RC) using Assura.

Tools Used: Cadence Virtuoso

Decoupled Inverter Pair Sense Amplifier

Designed a sense amplifier at 22nm technology node to improve performance by reducing delay and minimizing power-delay product (PDP). Simulated the design using industry-standard tools and compared the results with other conventional sense amplifier architectures. The proposed design showed better performance in terms of speed and energy efficiency, making it suitable for high-speed, low-power memory applications.

Tools Used: LT SPICE

COURSES AND RESEARCH WORK

Course name: Hardware Modelling using Verilog by Prof. Indranil Sengupta (IIT KHARAGPUR)

Course name: Digital IC Design by Prof. Janakiraman by IIT madras

Course name: VLSI Design Flow- RTL to GDS by Prof. Sneha Saurabh (IIIT Delhi)

Research Paper: Titled “Comparative Analysis of Sense Amplifier Design at Different Technology Node” in ESDA Conference (2025).

Research Paper: Titled “Comparative Analysis of Voltage-mode Sense Amplifiers with Modified Decap-Assisted Pre-charge technique “ in ICSIE Conference (2026).

Poornima Mittal

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