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Fault-Tolerant Design and Robust Control of Multiport DC–DC Converters with Reduced Current Ripple for Standalone PV–BES Systems

**A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of**

DOCTOR OF PHILOSOPHY

By

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(Roll No. 2K20/PHDEE/505)**

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I, Md. Modassir Masoom, hereby certify that the work which is being presented in the thesis titled "**Fault-Tolerant Design and Robust Control of Multiport DC–DC Converters with Reduced Current Ripple for Standalone PV–BES Systems**" in partial fulfilment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the Department of Electrical Engineering, Delhi Technological University is an authentic record of my work carried out during the period from 12-01-2021 to 20-05-2026 under the supervision of Prof. Narendra Kumar and Dr. Mayank Kumar. I have not submitted the matter presented in the thesis for the award of any other degree from this or any other institute.

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Md. Modassir Masoom

Abstract

The increasing penetration of renewable energy systems, battery energy storage systems, and electric vehicles (EVs) has accelerated the demand for efficient, reliable, and fault-tolerant power electronic interfaces capable of handling multidirectional power flow with enhanced dynamic performance. In this context, multiport DC–DC converters have emerged as a promising solution for integrating photovoltaic (PV) sources, battery energy storage systems, and multiple DC loads within a unified power conversion framework. However, conventional converter architectures are often constrained by high current ripple, increased semiconductor stress, limited fault-tolerant capability, poor dynamic response under non-minimum phase (NMP) conditions, and reduced robustness against parameter uncertainties and operating disturbances. Furthermore, maintaining stable converter operation under varying source conditions, load dynamics, and semiconductor fault scenarios remains a significant challenge in modern EV and renewable energy applications.

This thesis presents the modelling, analysis, design, and experimental validation of advanced non-isolated time-multiplexed multiport DC–DC converter architectures with fault-tolerant capability, reduced current ripple, soft-switching operation, and robust controller design for sustainable energy and light electric vehicle applications. Initially, a robust voltage-mode controlled time-multiplexed DC–DC multiport converter is investigated under non-minimum phase operating conditions. A systematic controllability analysis based on switched linear system (SLS) theory is carried out, and a robust PI controller is designed using the stability boundary locus method in conjunction with Kharitonov's theorem to ensure stable closed-loop operation under structured uncertainties and external disturbances. The proposed controller effectively improves disturbance rejection capability, voltage regulation performance, and system robustness under varying source and load conditions.

Subsequently, a tri-port fault-tolerant modular DC–DC converter with soft-switching capability is developed to achieve improved efficiency, modularity, and reliability. The proposed topology incorporates switched-boost action with time-multiplexed operation to regulate multiple output ports while enabling bidirectional battery charging and discharging operation. The integration of zero-voltage switching

(ZVS) and zero-current switching (ZCS) techniques significantly reduces switching losses and semiconductor stress. In addition, modular stackable architecture and closed-loop switching reconfiguration enable reliable fault-tolerant operation under open-circuit switch fault conditions. Detailed mathematical modelling and design analysis are carried out to characterize converter operation under various operating conditions.

Further, a solar PV-fed fault-tolerant four-port DC-DC converter is presented for light electric vehicle applications. The proposed converter integrates PV source, battery energy storage system, medium-voltage DC load, and low-voltage auxiliary load within a single non-isolated multiport architecture. The interleaved structure and phase-shifted control strategy effectively reduce battery charging current ripple and improve current sharing capability while enhancing converter reliability. The converter employs maximum power point tracking (MPPT), switched-boost operation, and time-multiplexing control to achieve coordinated multiport power management and bidirectional power flow operation. Detailed analysis of current ripple characteristics and converter operation under healthy and fault conditions is presented.

Finally, a comprehensive modelling and robust controller design framework for a non-isolated time-multiplexed multiport fault-tolerant (TMMFT) converter is developed considering parasitic elements and non-ideal operating conditions. Large-signal, averaged, and small-signal models are derived for different operating states, and controllability analysis is carried out using graph-theoretic principles and switched linear system modelling. Robust controller synthesis based on the stability boundary locus approach and Kharitonov's theorem is implemented to ensure stable operation under parameter uncertainties and open-circuit switch fault conditions. Sensitivity and complementary sensitivity analyses are carried out to validate robustness and disturbance rejection capability under healthy and faulty operating scenarios.

The proposed converter topologies and control strategies are experimentally validated using laboratory-scale prototypes implemented with real-time digital control hardware. Experimental investigations confirm reduced current ripple, improved voltage regulation, enhanced fault-tolerant capability, robust dynamic performance, effective disturbance rejection, and reliable operation under varying operating conditions. The outcomes of this research establish the suitability of the proposed

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multiport converter architectures for next-generation renewable energy systems, battery energy storage systems, and electric vehicle charging applications requiring high efficiency, reliability, and operational resilience.

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List of Abbreviations

ADC	Analog to Digital Converter
BES	Battery Energy Storage
CCCV	Constant Current Constant Voltage
CE	Characteristics Equation
CIS	Cyclic Invariant Subspace
CCM	Continuous Current Mode
CMC	Current Mode Control
DCR	Direct Current Resistance
DC	Direct Current
DIDO	Dual Input Dual Output
DPP	Differential Power Processing
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ESS	Energy Storage System
EV	Electric Vehicle
GM	Gain Margin
LEVs	Light Electric Vehicles
LHP	Left Hand Plane
LPRM	Load Power Reference Mode
LVDC	Low Voltage Direct Current
MI-MPC	Multi-Inductor Multiport Converter
MPC	Multiport Converters
MPPT	Maximum Power Point Tracker
MSO	Mixed Signal Oscilloscope
MVDC	Medium Voltage Direct Converter
NMP	Non-Minimum Phase
OCSF	Open-circuit Switch Fault
OLTF	Open-loop Transfer Function
PI	Proportional Integral
PM	Phase Margin

PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Storage
RHP	Right Hand Plane
RPR	Robust Proportional Region
SCSF	Short-Circuit Switch Fault
SDG	Sustainable Development Goal
SIDO	Single Input Dual Output
SI-MPC	Single Inductor Multiport Converter
SISO	Single Input Single Output
SLS	Switched Linear System
SMC	Sliding Mode Controller
SSA	State Space Analysis
SSM	Small-Signal Model
SSOLTF	Small Signal Open Loop Transfer Function
TFs	Transfer Functions
VMC	Voltage Mode Control
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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Chapter 1

INTRODUCTION

1.1 General

The global energy landscape is undergoing a rapid transition toward decarbonization, driven by stringent climate targets and the need to reduce greenhouse gas emissions. The transportation sector, being one of the largest contributors to emissions, is witnessing a paradigm shift from internal combustion engine vehicles to electric vehicles (EVs) [1]-[10]. This electrification of mobility introduces new challenges to the existing power infrastructure, particularly in terms of increased electrical demand, peak load stress, and grid stability. In this context, renewable energy integration, especially solar photovoltaic (PV) systems, plays a crucial role in ensuring a sustainable and clean energy supply. Solar PV is particularly attractive due to its modularity, scalability, and high availability in countries like India, which receive abundant solar irradiance throughout the year. The integration of solar PV with EV charging infrastructure leads to the concept of solar-powered EV charging systems, which offer a promising pathway toward carbon-neutral transportation. However, the intermittent nature of solar energy and the dynamic charging requirements of EVs necessitate the development of advanced power electronic interfaces and energy management strategies. This forms the core motivation of the present research.

1.2 Introduction to DC-DC Converters

The rapid growth of renewable energy systems, electric mobility, data centres, energy storage systems, and modern DC microgrids has significantly increased the demand for efficient power conversion technologies. Among the various power electronic interfaces, DC-DC converters play a pivotal role in regulating and conditioning electrical power between sources, storage systems, and loads. These converters primarily convert an available DC voltage to a regulated output voltage suitable for a particular application while maintaining high efficiency, reliability, and dynamic performance.

The increasing penetration of renewable energy sources and battery-integrated systems has further accelerated the development of advanced converter topologies capable of handling bidirectional power flow, wide voltage conversion ratios, and

multiport energy management. Renewable energy sources, such as solar PV, exhibit inherent intermittency due to varying irradiance and environmental conditions. Consequently, efficient power electronic interfaces are necessary to ensure stable voltage regulation, maximum power extraction, and reliable integration with energy storage and load systems. In this context, DC-DC converters serve as the primary energy-processing stage, bridging the gap between fluctuating renewable energy sources and regulated DC loads. Furthermore, integrating energy storage systems with DC microgrids and EV charging infrastructure requires converters with enhanced controllability, reduced current ripple, high power density, and improved reliability.

Conventional DC-DC converters are broadly classified into isolated and non-isolated topologies depending on the requirement of galvanic isolation, as shown in Figure 1.1. Non-isolated converters, such as buck, boost, buck-boost, Ćuk, SEPIC, and Zeta converters, are widely preferred in low- and medium-power applications due to their reduced component count, compact design, lower cost, and higher efficiency. Among these, boost-derived converter structures are widely employed in renewable energy and EV applications due to their ability to achieve high voltage gain from low-voltage sources, such as PV panels and battery systems. However, conventional converter structures suffer from several limitations, including high current ripple, increased switching stress, limited voltage gain, and reduced efficiency at high switching frequencies. To address these challenges, several advanced techniques such as interleaving, switched-capacitor cells, coupled inductors, voltage multiplier structures, resonant networks, and soft-switching approaches have been incorporated into converter design. In high-power and medium-voltage applications, isolated converter topologies employing high-frequency transformers provide galvanic isolation, improved safety, and higher voltage conversion capability.

The switching behavior of power semiconductor devices considerably influences converter efficiency and dynamic performance. Conventional hard-switched converters experience significant switching losses, voltage overshoot, electromagnetic interference (EMI), and thermal stress at high switching frequencies. To overcome these limitations, soft-switching techniques such as zero-voltage switching (ZVS) and zero-current switching (ZCS) are increasingly incorporated into modern converter structures. Soft-switching converters minimize switching losses by

ensuring commutation under either zero-voltage or zero-current conditions, thereby improving efficiency, reducing device stress, and enabling high-frequency operation with smaller passive components. Interleaved soft-switched converter architectures further contribute to current ripple minimization, thermal stress reduction, and enhanced power handling capability [11]-[17].

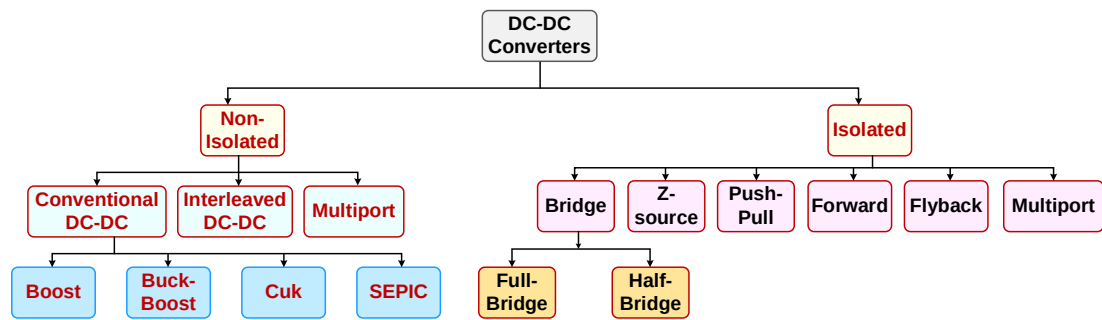


Figure 1.1 Classification of DC-DC converter topologies.

1.3 Multiport DC-DC Converters in Sustainable Energy Systems

The evolution toward MPDCs has enabled the integration of multiple energy sources, storage elements, and loads within a unified architecture, thereby improving power density, system integration, and energy management capability [18]-[25]]. These converters are particularly suitable for PV-EV systems and DC microgrids, where coordinated control of multiple ports is essential. Multiport converters (MPCs) have emerged as a transformative technology, critically improving the cost, size, weight, and efficiency of the system. These converters, which can connect to multiple energy sources and storage systems, are important for making the best use of energy and distributing it evenly. This has a direct effect on how long LEVs last (i.e., improvements in battery charging and discharging cycles) and how well they work. Recent studies emphasize the strategic role of MPCs in effectively managing fluctuating power demands and extending battery life. Bidirectional MPCs enable seamless energy transitions between propulsion and auxiliary systems, boosting energy conservation and vehicle range [26]-[29]. Moreover, advanced MPC architectures integrate renewable energy sources into LEVs, reducing grid power dependency and enhancing the overall energy autonomy of vehicles. Lastly, the capability of MPCs to provide voltage regulation across various subsystems of LEVs further ensures the reliability and safety of these vehicles [30], [31], [57].

1.4 Fault Tolerant Operation of DC-DC Converter

The increasing penetration of renewable energy systems, electric vehicles (EVs), aerospace power systems, DC microgrids, railway electrification, telecommunications infrastructure, and distributed energy storage systems has significantly increased the importance of reliable power electronic converters. Among these, DC-DC converters are among the most critical energy-processing stages due to their ability to regulate voltage, manage bidirectional power flow, and interface with multiple energy sources and storage units. However, the extensive utilization of high-frequency semiconductor switching devices in modern converter topologies exposes these systems to various reliability concerns associated with thermal stress, overcurrent, overvoltage, switching transients, gate driver malfunction, and component ageing. Consequently, the occurrence of faults in power electronic converters has become a major challenge affecting the operational continuity, safety, efficiency, and lifespan of modern electrical energy conversion systems.

In practical operating conditions, semiconductor switches are subjected to repetitive thermal cycling, large current stress, parasitic oscillations, and harsh environmental conditions, which significantly increase the probability of device failure. Statistical reliability studies of power electronic systems indicate that semiconductor devices and associated solder joints account for a substantial share of converter failures. Open-circuit switch faults (OCSFs) [30]-[32],[34], [37], [39] and short-circuit switch faults (SCSFs) [33] are the most common failure modes in semiconductor switches. Among these, OCSFs are comparatively less destructive in the initial stage but can severely deteriorate converter performance by introducing asymmetrical operation, increased current ripple, unbalanced voltage stress, harmonic distortion, and overload conditions on healthy devices. On the other hand, SCSFs may cause catastrophic damage if appropriate protection mechanisms are not in place. Therefore, the development of fault-tolerant DC-DC converters capable of maintaining uninterrupted operation under faulty conditions has become a major research focus in modern power electronics.

The growing dependence on DC microgrids and renewable energy systems further intensifies the need for converter reliability. In photovoltaic energy conversion systems, electric vehicle charging stations, battery energy storage systems, and hybrid

renewable power architectures, any interruption in power flow may result in severe operational and economic consequences. Conventional converter shutdown following a semiconductor fault is often undesirable because it reduces system availability and affects load continuity. In mission-critical applications such as electric propulsion systems, aerospace systems, traction drives, data centres, and medical power supplies, uninterrupted operation under fault conditions is essential. Consequently, fault-tolerant operation has emerged as an indispensable requirement in the design of modern DC-DC converters.

Fault-tolerant operation in DC-DC converters generally involves three major functions: fault detection, fault identification or localization, and post-fault reconfiguration or compensation control. The primary objective of fault diagnosis is to detect the occurrence of a fault within the minimum possible time before it propagates into severe damage. Once the faulty device is identified, the converter is reconfigured through redundant paths, modified switching strategies, or inherent circuit redundancy to maintain regulated power transfer. The effectiveness of a fault-tolerant converter depends largely on the fault detection speed, reliability of fault localization, transient response during reconfiguration, and the converter's capability to sustain acceptable voltage and current regulation under post-fault operation.

Various fault-diagnosis techniques have been developed for DC-DC converters, using both hardware-based and computational approaches. Time-domain and frequency-domain signal analysis methods are widely employed for identifying abnormal converter behavior under faulty conditions. Diagnostic variables such as inductor voltage, inductor current slope, capacitor voltage, diode voltage signature, DC-link current derivative, magnetic near-field waveform, and switching state information are commonly used for fault detection [30], [37], [66], [70]. Among these methods, diode-voltage-based and inductor-voltage-based techniques have attracted considerable attention due to their fast detection capabilities and relatively low implementation complexity. Model-based fault diagnosis methods employing state estimators, observer-based techniques, and switched linear system models have also been proposed to improve fault localization accuracy. However, these methods often require accurate converter modeling, increased computational burden, and sophisticated digital processing hardware.

The advancement of interleaved, multiphase, and multiport converter structures has further introduced new opportunities and challenges in fault-tolerant converter design. Interleaved converter configurations are extensively utilized to reduce input current ripple, improve thermal distribution, increase power density, and enhance converter efficiency. The inherent modularity and parallelism of such topologies provide improved fault-handling capability, as healthy phases can continue operating even after the failure of one converter leg. Similarly, multiport DC-DC converters integrating renewable energy sources, batteries, and loads within a unified structure require enhanced reliability due to the complexity of coordinated power transfer among multiple ports. Therefore, recent research efforts have focused on developing reconfigurable, inherently fault-tolerant converter architectures capable of sustaining regulated operation under single-switch and multiple-switch faults [38]-[42].

In modern fault-tolerant converter architectures, redundancy techniques are broadly classified into module-level redundancy, switch-level redundancy, and inherent circuit redundancy. Conventional redundancy methods employ additional semiconductor switches or converter legs to replace faulty components during post-fault operation. Although effective, these methods increase converter size, cost, control complexity, and conduction losses. To overcome these limitations, reconfigurable converter structures and time-multiplexing control approaches have recently been developed to achieve fault tolerance using existing converter components without significantly increasing hardware complexity. Such approaches improve converter reliability while maintaining reduced component count, high efficiency, and compact structure [43]-[47].

Another important aspect of fault-tolerant converter operation is maintaining converter performance under fault conditions. Faults often result in increased current ripple, degraded voltage regulation, unequal current sharing, additional stress on healthy devices, and reduced conversion efficiency. Therefore, modern fault-tolerant converter designs incorporate interleaving techniques, switched-boost actions, robust control strategies, and optimized modulation methods to mitigate the impact of faults on converter dynamics.

Therefore, the development of fault-tolerant DC-DC converters with reliable post-fault operation, reduced current ripple, enhanced voltage regulation, and uninterrupted power transfer has become a fundamental requirement for modern power electronic systems. The increasing adoption of renewable energy systems, electric transportation, and hybrid energy storage architectures necessitates advanced converter topologies that maintain high reliability and operational continuity even under semiconductor fault conditions. These requirements motivate ongoing research toward efficient, compact, and reconfigurable fault-tolerant DC-DC converter architectures with improved robustness, efficiency, and dynamic performance.

1.5 Closed-Loop Control of Multiport DC-DC Converters

Common techniques such as proportional-integral (PI) control, state feedback, model predictive control (MPC), and sliding mode control (SMC) are often employed to achieve the desired transient and steady-state responses. Complementing these methods, fault-tolerant control and time-multiplexed power-processing strategies further broaden the operational envelope of multiport systems by accommodating switch failures, reducing ripple, and preserving regulation in reconfigured converter states [48], [49]. Similar limitations appear in hierarchical multiport architectures, where PI-based local controllers ensure acceptable steady-state regulation but do not address the deterioration of stability margins under device aging, abrupt load disturbances, or intensified port interactions [50].

Achieving optimal performance in DC-DC multiport converters demands a rigorous approach to controllability analysis and robust controller design [51]-[53]. These converters exhibit complex dynamic behavior in response to variations in input sources, output demands, and load conditions, necessitating accurate and responsive control mechanisms. This process entails a thorough evaluation of the system's state-space representation within the framework of a switched linear system (SLS), the development of a small-signal model (SSM), and the implementation of control strategies capable of preserving system stability across diverse operating conditions. Widely adopted methods such as PI control, state-feedback, and model predictive control are typically utilized to ensure both superior transient performance and steady-state regulation.

11 Current mode control (CMC) inherently suffers from inner-loop instability when the duty cycle exceeds 50%, irrespective of the specific DC-DC converter topology employed [54]. Conversely, voltage mode control (VMC) does not impose such duty cycle constraints. However, in boost converter applications, VMC exhibits limited dynamic performance due to the emergence of a right-half-plane (RHP) zero in the transfer function. This RHP zero imposes a fundamental restriction on the achievable closed-loop bandwidth leading to a slower transient response. Consequently, achieving high-performance regulation in non-minimum phase (NMP) boost converters while operating near the RHP zero constraints presents significant control challenges under VMC schemes.

Efficient operation of multi-output power electronic converters requires coordinated control among different ports to effectively manage the power flow, as presented in [55]-[58]. This coordination is typically achieved through cooperative feedback control mechanisms.

The stabilization and closed-loop control of the converter can also be achieved using an H_∞ -controller. However, this approach inherently involves a higher-order design, which poses practical implementation challenges. Although model order reduction techniques can be applied to obtain a lower-order version, the resulting controller often compromises robustness and may lead to degraded performance [12], [59]. Utilizing lower-order controllers is a viable option for converter stabilization to ensure effective regulation. Lower-order controllers, such as PI/PID controllers, are easier to implement. The elementary PI controller may not offer enough stability and robustness for more complex converter systems. The robust PI type controller is a suitable option for DC-DC converter control due to its stability and robustness against plant parameter variability.

In [60], [61], such as the robust multiple-frequency voltage-mode design for DC-DC boost converters, have improved disturbance rejection and robustness by optimizing controller gains across a wide frequency range. Similarly, low-frequency current-mode control with overshoot suppression has achieved superior transient performance and reduced output voltage deviation during dynamic conditions. However, these methodologies remain focused on single-output converters with limited adaptability to multiport architectures.

Advanced control strategies have been proposed to enhance the stability of DC-DC boost converters. Among these, integral sliding mode control with disturbance observation (ISMC-DO) and continuous non-singular terminal sliding mode control (CTSMC) exhibit strong robustness and dynamic performance. However, these methods involve complex controller design, higher computational demand, sensitivity to parameter variations, and challenges in real-time implementation [62], [63]. Recent advancements in DC-DC converter control strategies for microgrid and renewable energy applications. VMCs have been optimised for stability and robustness, addressing non-minimum phase issues and enabling efficient voltage regulation using reduced-order state-space models and frequency-domain techniques. The SLS theory, introduced in [17], [64], [65] provides a framework to model the dynamic behaviour of power converters, facilitating theoretical analysis in power electronics.

1.6 Objectives of the Work

- 1) Characterization and design of standalone solar PV-based electric vehicle charging with reduced current ripple.
- 2) Design, control and characterization of current ripple behaviour of electric vehicle charging system with non-isolated DC-DC converter.
- 3) Design, control and characterization of current ripple behaviour of electric vehicle charging system with bidirectional DC-DC resonant converter.
- 4) Modelling, analysis and control of soft-switched interleaved boost converter for battery energy storage system.

1.7 Outline of the Chapters

The thesis is organized in seven chapters followed by appendices.

Chapter 1 presents the general introduction of the thesis, beginning with an overview of the research domain and motivation. It includes a detailed introduction to DC-DC converters, followed by the role of multiport DC-DC converters in sustainable energy systems, and fault-tolerant operation of DC-DC converters, particularly in solar PV and electric vehicle applications. The chapter further discusses the control aspects of multiport converters and concludes with clearly defined objectives of the work. **Chapter 2** provides a comprehensive literature review on multiport DC-DC converter topologies and robust controller design techniques. It critically examines modular,

interleaved, and soft-switched converter structures along with conventional and advanced control strategies, including robust and nonlinear control methods, highlighting their advantages, limitations, and research gaps.

Chapter 3 presents the non-isolated time-multiplexed tri-port DC-DC converter. This chapter includes the dynamic modelling of the converter under non-ideal conditions and a detailed analysis of its operating principles under different modes of operation. Large-signal, averaged, and small-signal models are developed for each operating mode. The chapter further investigates the need for controllability analysis and presents structural, state and output controllability using switched linear system theory. A robust controller design is developed based on Kharitonov's theorem and stability boundary locus method, including systematic selection of controller gains and sensitivity analysis. The proposed system is validated through experimental analysis covering controllability verification, dynamic performance, mode transitions, and controller effectiveness.

Chapter 4 focuses on the tri-port soft-switched modular DC-DC converter with reduced current ripple for energy storage systems (ESS). The proposed modular converter topology is presented along with its operating principles under different states of operation. Time-domain analysis is carried out for each state, and the design of the resonant inductor and capacitor is discussed to achieve ZVS and ZCS conditions. The chapter includes the identification of soft switching regions and boundary conditions. The controller operation is explained for different operating modes, and detailed experimental results are presented under charging, discharging and open-circuit switch fault (OCSF) conditions to demonstrate reduced current ripple.

Chapter 5 presents the standalone solar PV-fed time-multiplexed fault-tolerant four-port DC-DC converter. The chapter describes the proposed converter topology and its operation under multiple operating states corresponding to different PV and load conditions. Detailed steady-state analysis, current ripple characterization for input, battery and auxiliary ports, and small-signal stability analysis are carried out for each state under ideal conditions. The chapter also investigates the behavior of the converter under OCSF conditions. Frequency-domain analysis using Bode plots is presented to evaluate system stability. The design of the input capacitor PV side is derived using large-signal, averaged, and small-signal models. The controller operation for different

states is discussed, followed by experimental validation under both healthy and fault conditions, including efficiency and comparative performance analysis.

Chapter 6 deals with the robust controller design for time-multiplexed multiport DC-DC converters. The chapter presents averaged small signal modelling under non-ideal conditions for different operating states. A switched linear system model is developed, and detailed controllability analysis, including structural, state, and output controllability, is performed. Robust controller design is carried out for both healthy and open-circuit switch fault conditions using stability boundary locus and Kharitonov's theorem. The selection of controller gains and sensitivity analysis are discussed in detail. The proposed control strategy is validated through experimental results, including controllability validation, dynamic response analysis, and comparative performance evaluation under different operating conditions.

Chapter 7 summarizes the main conclusions of the research work and outlines the future scope. Some theoretical derivations and detailed descriptions of the experimental setup used for laboratory prototype development are presented in the Appendix.

Chapter 2

LITERATURE REVIEW

2.1 General

A literature review is a fundamental component of scientific research, providing a systematic and critical assessment of the existing knowledge base in a specific research domain. It involves a comprehensive evaluation of previously reported studies, technical developments, and research findings to establish a clear understanding of the current state of the art. Through detailed analysis and synthesis of the available literature, the review identifies prevailing research trends, methodological approaches, technical limitations, and unexplored areas requiring further investigation. Such an analytical framework not only establishes the research context but also facilitates the identification of critical gaps and challenges within the field. Consequently, a well-structured literature review provides a strong foundation for the proposed research, guiding the formulation of objectives, methodologies, and future advancements in the area of study.

2.2 Literature Survey

2.2.1 DC-DC Converter Topologies for PV Applications

In recent years, considerable research has been dedicated to the circuit topology and modeling of the multiport power converters.

K. Suresh, C. Bharatiraja, et al., [72] proposed a non-isolated dual-input dual-output multiport converter for electric vehicle applications, capable of integrating multiple energy sources with different voltage levels. The topology enables simultaneous buck-boost operation and bidirectional power flow, ensuring efficient energy management. A small-signal model and state-space analysis were developed to study the dynamic behavior, and a coordinated control strategy was implemented to regulate power flow among ports.

Yusuke Sato, Masatoshi Uno, et al., [25] proposed a non-isolated multiport converter integrating PWM and phase-shift switched capacitor techniques, enabling independent regulation of PV, battery, and load. The topology reduces switch count and introduces dual control variables (duty cycle and phase shift), with detailed modelling of gain characteristics and soft-switching boundaries.

Santanu K. Mishra, Khirod Kumar Nayak, et al., [23] introduced a switched-boost action-based multiport converter using time-multiplexing control. The topology enables multiple regulated outputs with reduced switch count and supports CCCV battery charging and automatic mode transition between renewable sources and storage systems.

Olive Ray, Santanu Mishra, et al., [61] introduced an integrated dual-output converter, i.e., single input multiple output (SIMO) topology, capable of generating both step-up and step-down outputs using shared switching devices. The converter achieves reduced component count, improved cross-regulation, and high efficiency, with detailed steady-state and dynamic analysis supported by experimental validation.

Xiaoquan Zhu, Bo Zhang, et al., [63] proposed an extended switched-boost DC-DC converter using switched-capacitor and switched-inductor cells to achieve high voltage gain. The topology provides high step-up conversion without extreme duty ratios, reduces voltage stress on switches, and supports modular expansion for higher gain applications.

Wentao Jiang, Xinan Zhang, et al., [73] investigated the large-signal stability of interleaved boost converters under constant power load conditions and proposed a nonlinear disturbance observer-based sliding mode control strategy. A generalized state-space model was developed to ensure stable DC bus voltage and robust dynamic performance.

Zakariya M. Dalala, Jih-Sheng Lai, et al [74] presented a bidirectional CLLLC resonant converter for battery charging applications, achieving soft-switching, i.e., ZVS operation for improved efficiency. A comprehensive modelling and controller design methodology was developed considering load variations, ensuring stable operation across a wide operating range.

P. Prabhakaran, Vivek Agarwal, et al., [75] developed a four-port DC-DC converter for PV-fuel cell hybrid systems in bipolar DC microgrids, featuring a single-inductor structure and reduced component count. The converter includes small-signal modelling for multiple operating modes and ensures efficient voltage regulation and power sharing.

Ruihua Shen, Henry Shu-Hung Chung, et al., [76] proposed the use of a nonlinear inductor in DC distribution systems to enhance both small-signal and large-signal stability. The approach ensures stable operation under constant power loads without requiring complex control schemes, validated experimentally.

Hao Zhang, Dachu Dong, et al., [28] presented a systematic topology derivation framework for multiport DC-DC converters based on voltage-type ports. The work establishes a generalized methodology for deriving converter structures and analyzing power flow paths, supported by modelling and experimental validation.

Ahmed Amr Saafan, Vinod Khadkikar, et al., [77] introduced a bidirectional multiport DC-DC converter for DC microgrid applications, which reduces multiple power conversion stages and enhances system efficiency. The proposed topology employs state-space averaging and small-signal modelling for dynamic analysis, along with a frequency response-based controller design to regulate DC-link voltage and ensure stable operation under varying renewable energy conditions.

Shaik Reddi Khasim, C. Dhanamjayulu, et al., [19] developed a single-inductor multiport converter for electric vehicle applications, enabling hybridization of solar PV and battery sources. The converter achieves dual-input dual-output functionality with reduced component count, and detailed state-space modelling for different operating modes was carried out to analyze charging and discharging behavior.

Sathish Kumar Kollimalla, Mahesh Kumar Mishra, et al., [13] proposed a novel control strategy for hybrid energy storage systems (battery-supercapacitor) to manage power fluctuations in renewable energy systems. The control method allocates low-frequency power to batteries and high-frequency power to supercapacitors, thereby improving system response and reducing battery stress, validated through experimental results.

2.2.2 DC-DC Converter Topologies for EV Applications

Hongfei Wu, Yan Xing, et al., [20] proposed a family of non-isolated three-port converters (TPCs) for standalone renewable energy systems integrating renewable sources, battery storage, and load ports within a unified power conversion structure. The proposed converter topologies achieve single-stage power conversion between

any two ports, resulting in reduced component count, improved efficiency, compact structure, and enhanced power management capability for renewable energy applications.

2 Azuka Affam, Yonis M. Buswig, et al., [24] presented a comprehensive review of multiple-input DC-DC converter topologies for hybrid electric vehicles and renewable energy systems. The study classified converters into electrically connected, electromagnetically connected, and magnetically connected structures, highlighting their suitability for integrating multiple renewable sources and energy storage devices while reducing converter count, system cost, and control complexity.

11 Md. Safayatullah, Mohamed Tamasas Elrais, et al., [78] reviewed advanced power converter topologies and control methods for electric vehicle fast-charging applications. The work emphasized the significance of multiport converters, bidirectional DC-DC converters, and high-power fast charging architectures for achieving high efficiency, reduced charging time, improved reliability, and integration of renewable energy sources with EV charging infrastructure.

34 Siddhant Kumar and Adil Usman, [79] presented a review of converter topologies for battery charging applications in plug-in hybrid electric vehicles (PHEVs). The study investigated bidirectional AC-DC and DC-DC converter configurations employed in battery charging systems, emphasizing efficient power transfer, battery management compatibility, and improved charging performance for hybrid electric vehicle applications.

78 G. K. Naveen Kumar and Arun Kumar Verma, [80] proposed a two-stage onboard EV charger employing an interleaved bridgeless buck–boost power factor correction (PFC) converter followed by an LLC resonant converter. The interleaved structure improves input current shaping, reduces harmonic distortion, and enables high-power-factor operation over a wide input-voltage range, while enhancing converter reliability and efficiency for low-voltage EV charging applications.

Anjanee Kumar Mishra and Taehyung Kim, [81] introduced an economical light plug-in electric vehicle (LPEV) charging system based on an integrated single-stage DC-DC converter. The proposed topology performs multifunctional operations, including

MPPT control, PFC operation, propulsion support, and regenerative braking, using fewer components, thereby improving the compactness, efficiency, and cost-effectiveness of the charging architecture.

Klemen Drobnic, Gabriele Grandi, et al. [82] proposed a grid-tied modular three-phase interleaved converter for EV fast-charging applications. The modular interleaved architecture achieves ripple-free charging current, reduced current stress, and improved thermal distribution, while enabling high-power, fast charging with enhanced efficiency and scalability.

Cuili Chen, Zhongbao Wei, et al., [83] reviewed charging optimization techniques for lithium-ion batteries in electric vehicles. The study analyzed various charging strategies including CCCV, model predictive control, and intelligent charging algorithms aimed at reducing charging time, minimizing battery degradation, and improving charging efficiency under fast-charging conditions.

Alakshyender Singh, Jitendra Gupta, et al., [84] presented the design and control of a two-stage battery charger for low-voltage electric vehicles using a high-gain bridgeless buck-boost PFC AC-DC converter followed by an isolated Ćuk DC-DC converter. The charger achieves high power factor, wide voltage conversion capability, and effective implementation of CC and CV charging modes with reduced control complexity.

Rong-Jong Wai and Jun-Jie Liaw, [21] proposed a high-efficiency isolated single-input multiple-output bidirectional converter for power storage systems and EV-related applications. The converter utilizes coupled inductors and soft-switching operation to achieve bidirectional power transfer, reduced voltage stress, multiple regulated output voltages, and improved efficiency under different operating conditions.

M. Imran Shahzad, Shahid Iqbal, et al., [85] developed an interleaved LLC resonant converter with cascaded voltage-doubler rectifiers for plug-in electric vehicle battery charging. The converter achieves a wide output-voltage range, high efficiency, and reduced switching losses through resonant soft-switching and interleaving techniques, making it suitable for deeply depleted battery charging applications.

Seonghye Kim and Feel-Soon Kang, [86] proposed a multifunctional onboard battery charger for plug-in electric vehicles capable of performing onboard charging, vehicle-

to-grid (V2G) operation, and auxiliary battery charging using a unified converter structure. The topology shares semiconductor devices and passive components among different functions, thereby reducing converter size, weight, and system complexity.

Robson Mayer, Menaouar Berrehil El Kattel, et al., [87] introduced a **multiphase interleaved bidirectional DC-DC converter with coupled inductors for electrified vehicle applications**. The converter achieves reduced current ripple, lower switching stress, improved current sharing, and high efficiency over wide operating ranges while supporting bidirectional power transfer for EV energy storage systems.

Arihant Swaminathan and Malavika Kovili, [88] reviewed different power electronic converter topologies and control strategies employed in electric vehicles. The work discussed the role of DC-DC converters, inverters, regenerative braking systems, and advanced control techniques in improving EV efficiency, reliability, and dynamic performance.

Haoqing Cai, Min Chen, et al., [89] investigated **charging current ripple suppression techniques for battery energy storage converters under distorted grid conditions**. The proposed control strategy effectively suppresses harmonic current ripple during charging operation, thereby improving battery lifespan, charging quality, and converter performance in EV charging systems.

2.2.3 Modular and Soft-Switched Interleaved Converters

Xiaoquan Zhu, Jintao Hou, et al., [90] proposed a modular input-independent output-series (IIOS) multiport DC-DC converter for MVDC integration of distributed DC units. The topology enables direct interfacing of multiple sources to MVDC without intermediate stages, significantly reducing system complexity and cost. A power-balancing LC branch is introduced to mitigate submodule voltage mismatch, while ZVS is achieved for all switches, enhancing efficiency and stable multiport operation under varying load conditions.

Chengsong Wei, Xiaoquan Zhu, et al., [91] introduced a modular single-stage IIOS converter with resonant voltage balance bus (RVBB) for PV-based MVDC systems. The proposed topology ensures self-voltage balancing among submodules and achieves **ZVS turn-on for switches and ZCS turn-off for diodes, resulting in reduced**

switching losses and improved dynamic response. The architecture enables efficient single-stage energy conversion with enhanced modular scalability.

Sivakrishna Karpana, Suman Maiti, et al., [92] developed a non-isolated soft-switched multiport converter for distributed PV systems integrated with energy storage. The converter supports distributed MPPT and differential power processing, allowing independent control of PV sources while maintaining high efficiency. The topology achieves soft-switching operation with reduced component count, validated experimentally on a laboratory prototype.

Abdulgafor Alfares, Brad Lehman, et al., [93] proposed a modular Cuk-based DC-DC converter for MVDC applications with soft-switching characteristics utilizing transformer leakage inductance. The design eliminates bulky electrolytic capacitors, improves reliability, and supports bidirectional power flow. The modular configuration enables flexible series/parallel connection for high-voltage and high-power applications.

Enhui Chu, Jianqun Bao, et al., [94] presented an interleaved two-switch forward converter with passive auxiliary resonant circuit, achieving ZVS and ZCS for all switches. The interleaved structure enhances power density, reduces circulating current, and mitigates voltage stress, while improving efficiency and reliability through soft-switching operation.

Syed Waqar Azeem, Muhammad Ehab, et al., [95] proposed a zero-voltage zero-current-switching (ZVZCS) full-bridge converter for MVDC systems, employing a dual-transformer configuration to achieve soft-switching across a wide load range. The topology ensures reduced switching losses and optimized power transfer, validated through a 3-kW prototype for renewable energy integration.

Tao Zeng, Zhen Wu, et al., [96] introduced a high step-up interleaved soft-switching converter with input-current ripple cancellation and improved voltage gain using switched-capacitor structures. The converter achieves ZVS for switches and ZCS for diodes, significantly reducing switching losses and improving efficiency in PV applications.

Tao Li, Leila Parsa, et al., [36] developed a modular soft-switching DC-DC converter with fault-tolerant capability based on input-parallel-output-series (IPOS) configuration. The converter achieves ZVS for primary switches and ZCS for secondary devices, while interleaving reduces ripple and improves current sharing. The modular design ensures scalability, redundancy, and uninterrupted operation under fault conditions.

Rasha Kassem, Nagwa Ibrahim, et al., [97] proposed an enhanced multiphase interleaved boost converter with soft-switching operation for PV applications. The converter achieves ZVS and ZCS switching, reduced current ripple, and high efficiency ($\approx 98\%$), with improved voltage gain using coupled inductors and a dual-loop control strategy.

2

Rasoul Faraji, Hosein Farzanehfard, et al., [98] introduced a fully soft-switched multiport DC-DC converter with high integration, enabling multiple power flow paths with shared components. The topology employs multiple soft-switching techniques to ensure ZVS/ZCS under all operating modes, resulting in improved efficiency and reduced component count.

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Shanshan Zhao, Yu Chen, et al., [38] proposed a modular multilevel DC-DC converter (MMDC) with inherent bipolar operation capability for MVDC grids. The modular structure enables independent power regulation of multiple ports, high scalability, and enhanced reliability through partial-load operation under fault conditions.

Nishant Kumar, Mayank Kumar, et al., [100] developed a multiport interleaved resonant DC-DC converter for EV fast charging applications. The interleaved architecture reduces current ripple and improves power density, while achieving ZVS over a wide input range using resonant operation.

Shanshan Zhao, Yu Chen, et al., [117] proposed a modular multilevel DC-DC converter with three-port bidirectional operation, enabling independent power control among MVDC and LVDC ports. The converter achieves efficient power flow regulation with reduced circulating power and improved scalability, validated experimentally.

Jayamurugan Mookkan, Saravanan Kaliyaperumal, et al., [118] proposed a modular buck-boost-based multiport bidirectional converter for hybrid EV applications. The converter supports bidirectional power flow, multiple operating modes, and efficient energy management, with a modular architecture enabling flexible integration of PV, battery, and load systems.

2.2.4 Fault-Tolerant Converter Topologies, Operation & Applications

Praneeth Kumar Pedapati, Allamsetty Hemachander, et al., [27] proposed a reconfigurable multiport DC-DC converter topology capable of handling single and multiple switch faults. The design incorporates reconfiguration-based fault tolerance, ensuring uninterrupted power supply and regulated output voltage under fault conditions. The topology supports both open-circuit and short-circuit fault handling, validated through experimental results.

Hanyu Wang, Xuejun Pei, et al., [29] proposed a general fault-tolerant operation strategy for modular series-parallel DC-DC converters, incorporating both fault diagnosis (FD) and post-fault reconfiguration (PFR). The fault detection is achieved using the relationship between inductor voltage and gate signals, enabling fast and low-cost fault identification without additional sensors. A generalized reconfiguration scheme is developed for different converter structures, ensuring smooth hot-swapping and uninterrupted operation under switch fault conditions.

Fernando Bento, Antonio J. Marques Cardoso, et al., [32] presented a fault diagnosis and fault-tolerant operation method for interleaved DC-DC boost converters, focusing on OCSF detection using time-domain analysis of converter variables. A simplified diagnostic algorithm independent of duty cycle is proposed, along with a reconfiguration strategy to maintain converter operation under faulty conditions, experimentally validated on a multi-phase prototype.

Sairaj V. Dhople, Ali Davoudi, et al., [40] introduced a unified reliability assessment framework for multiphase DC-DC converters in PV systems using Markov-based reliability modelling. The study integrates steady-state converter models with stochastic failure analysis, enabling accurate estimation of system reliability and mean

time to failure. The work highlights the influence of component stresses, switching frequency, and capacitor ratings on converter reliability.

Rishabh Bansal, Rushiv Bansal, et al., [31] introduced a time-multiplexed switched-boost multiport converter with enhanced reliability, utilizing boost-side interleaving to reduce input current ripple and improve thermal performance. The converter achieves a fault tolerance index (FTI) of 100% under open-circuit faults and supports CCCV battery charging with bidirectional power flow, validated through detailed performance analysis and experimentation.

Rushiv Bansal, Rishabh Bansal, et al., [58] developed a fault-tolerant multiport bidirectional DC-DC converter with reduced current ripple, employing interleaving and time-multiplexing control. The converter provides step-up/down voltage gain with bidirectional capability and ensures fault tolerance against semiconductor failures. A switched linear system-based small-signal model and robust controller design using stability boundary locus are presented, along with detailed current ripple characterization and experimental validation.

Taehyung Kim, Hyung-Woo Lee, et al., [67] proposed a fault detection and compensation control scheme for modified boost DC-DC converters, enabling continued operation under OCSF conditions. A fault detection index-based method combined with mixed switching control strategy is implemented using a DSP controller, ensuring reliable operation in renewable energy systems with integrated storage.

20 Hadi Givi, Ebrahim Farjah, et al., [68] developed a switch and diode fault diagnosis technique for non-isolated DC-DC converters using diode voltage signature analysis. The method enables rapid detection of open-circuit and short-circuit faults within one switching cycle, improving converter monitoring and reliability without requiring complex sensing mechanisms.

26 Mayank Kumar, [69] presented a time-domain characterization and detection method for open-circuit switch faults in H-bridge converters, employing analytical modelling and Fourier-based analysis of switching states. The proposed method enables accurate

identification of fault location and type, improving system reliability and operational safety in multilevel power converter applications.

Goutham Selvaraj, Amin Rahnema Sadat, et al., [71] presented an improved fault-tolerant power converter for EV propulsion systems, integrating fault-tolerant control (FTC) in both DC-DC and inverter stages. The proposed topology reduces the number of bypass components while enabling continuous motor operation under OCSFs. The effectiveness of the control strategy is validated using real-time hardware-in-the-loop (HIL) implementation with DSP control.

2.2.5 Controller and Robust Control Design

Harish Karneddi, Deepak Ronanki, et al., [16] proposed a predictive control-based bidirectional battery charger capable of operating over a wide voltage range with smooth transition between buck and boost modes. The predictive control strategy minimizes zero-crossing distortion and enhances dynamic performance under both grid-to-vehicle (G2V) and vehicle-to-grid (V2G) modes. The controller demonstrates improved transient response and power quality, validated through experimental implementation on a dSPACE-controlled SiC-based prototype.

Farzin Asadi, [102] introduced a robust control framework for DC-DC converters based on Kharitonov's theorem, enabling stability analysis under interval parametric uncertainties. The work establishes that conventional PI controllers can be transformed into robust controllers through proper gain selection, ensuring stability against input voltage and load disturbances. The methodology provides a systematic approach for designing controllers with guaranteed robustness margins.

Sija Gopinathan, V. S. Rao, et al., [14] developed a controllability-based controller design for switched inductor-capacitor high-gain converters using SLS modeling. A robust PI controller is designed using the stability boundary locus method combined with Kharitonov's theorem, ensuring stable operation under disturbances. The controller achieves a defined robust performance region (RPR) and is experimentally validated using hardware implementation.

Guidong Zhang, Peiwei Heng, et al., [52] presented a comprehensive controllability analysis of high-order DC-DC converters using SLS theory, addressing the challenges

associated with increased system order and multiple dynamic states. The study establishes structural, state, and output controllability conditions, providing a theoretical foundation for systematic controller design in multicell converters, validated through experimental studies.

Mummadi Veerachary, Priyabrata Shaw, et al., [12] proposed a robust voltage-mode controller design for fifth-order boost converters using a contoured robust Bode plot technique. The controller ensures robust voltage regulation under load and input perturbations, and analytical conditions for guaranteed stability are derived. Experimental validation confirms improved dynamic and steady-state performance.

Laxmidhar Senapati, Anup Kumar Panda, et al., [50] proposed a PI-Lead compensator for SIMO Cuk converters to mitigate cross-coupling and cross-regulation issues. The controller effectively decouples multiple outputs and improves transient response under parameter uncertainties. The performance is validated through simulation and hardware prototype implementation.

Mummadi Veerachary, [59] introduced a digital controller design based on Tchebyshev polynomial approach for fifth-order boost converters. The method identifies the complete stabilizing region in the discrete-time domain, enabling optimal controller gain selection through constrained optimization. The controller demonstrates improved voltage regulation and reduced current ripple under perturbations.

Mummadi Veerachary, B. Krishna Mohan, et al., [102] developed a robust digital voltage-mode controller (DVMC) using discrete-time modeling techniques. The controller satisfies robust stability criteria based on sensitivity functions, ensuring voltage regulation under disturbances. The design is validated experimentally, demonstrating robustness over a wide operating range.

Isac Daimary, Rajib Jana, et al., [54] proposed a sliding mode control (SMC) strategy for multiport converters to mitigate cross-coupling and cross-regulation effects. The controller enhances transient performance and ensures robust voltage regulation across multiple outputs, validated through hardware experimentation.

Mayank Kumar, et al., [17] analyzed the stability and sensitivity of digitally controlled DC-DC converters considering parasitic effects, highlighting the impact of sampling

frequency and circuit non-idealities on system stability. The study provides analytical guidelines for robust digital controller design and is validated using FPGA-based implementation.

7 Nikhil Kumar, Mummadi Veerachary, et al., [104] proposed a robust controller design based on stability boundary locus and Kharitonov's theorem for high-gain boost converters exhibiting RHP zero characteristics. The method defines a robust stability region ensuring gain and phase margins, and validates controller robustness experimentally under parameter variations.

Maraka Israyelu, Sashidhar S., et al., [65] developed a state-space modeling approach incorporating circuit parasitics for high-gain converters, enabling accurate prediction of dynamic behavior and stability characteristics. The study highlights the importance of accounting for non-ideal effects in controller design and validates the results through simulation and hardware experimentation.

2.2.6 Identified Research Areas

- 1) Enhanced reliability and fault-tolerant capability are essential to meet the growing demands of PV-integrated EV charging systems, ensuring continuous and stable operation under dynamic conditions and potential component failures.
- 2) Need for enhanced robust control strategies to ensure resilience against component failures, parameter variations, and dynamic EV charging conditions, highlighting a gap in reliable converter operation.
- 3) Need for an optimized topology and control strategy to achieve low current ripple in multiport, time-multiplexed converters under dynamic PV-EV conditions, without reliance on bulky passive components or limited interleaving.
- 4) Need for reliable soft-switching across wide operating ranges in multiport, bidirectional systems to improve efficiency and reduce switching losses.

Chapter 3

NON-ISOLATED TIME-MULTIPLEXED TRI-PORT DC-DC CONVERTERS

3.1 General

A power converter with a single input source and multiple outputs at different voltage levels is known as a single-input multiple-output converter. However, as in many applications, the same port works as both input and output (e.g., battery or grid interfaced ports), they are defined as a multiport converter (MPC), as depicted in Figure 3.1. The outputs of this class of converter can either be higher or lower than the supply voltage, depending on the application. Some of the explored applications for these converters are on-chip supplies for consumer electronic devices, power supplies for consumer appliances, renewable energy integration in homes and electric vehicles. MPCs can be isolated type or non-isolated type, as classified in Figure 3.2. Isolated-type MPC uses a transformer with multiple secondary windings to interface with multiple loads. In this case, only one of the outputs is tightly regulated, and the rest of the outputs are coupled through extra secondary windings. Non-isolated MPCs have no galvanic isolation between different ports. However, depending on the number of inductors, they can be further categorized into single-inductor MPC (SI-MPC) or multiple-inductor MPC (MI-MPC).



Figure 3.1 Block diagram of an MPC.

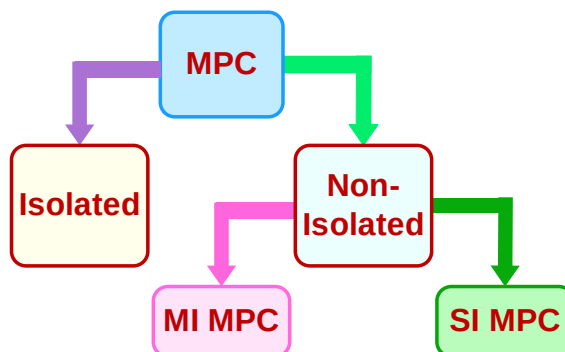


Figure 3.2 Classifications of different MPCs.

There are three different ways in which a boost topology can be customized to supply multiple outputs:

The first method uses a charge-sharing approach using individual switches to distribute inductor energy to different capacitors. This method of generating multiple outputs uses the concept of charge sharing [74]. The schematic of a two-output boost topology using this approach is shown in Figure 3.3. The inductor is charged for DT_s time period using the switch S_1 , and in the subsequent $(1-D)T_s$ interval, the rest of the switches S_3 , S_2 , etc., are turned ON sequentially, where D is the duty ratio and T_s is switching time period. Therefore, the charge is shared between output capacitors C_{01} , C_{02} , etc., respectively. This topology, its analysis, and associated operational issues are extensively reported in the literature [106]-[108]. As all the outputs are coupled to the same switch node in this class of MPCs, the outputs exhibit significant cross-regulation. The dynamics of these converters are also poor.

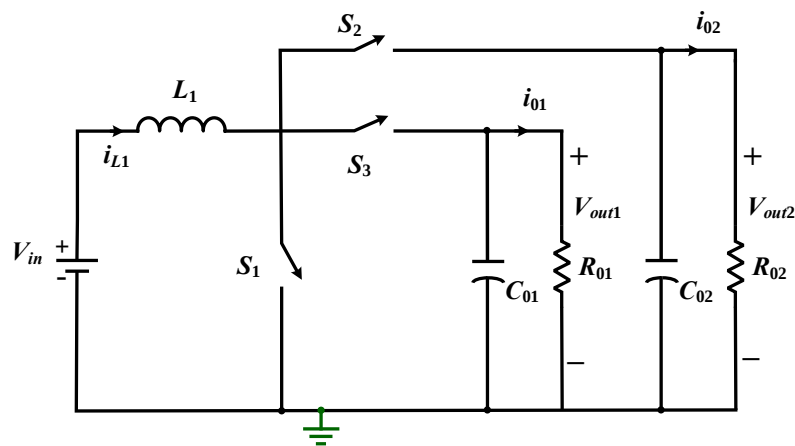


Figure 3.3 SI-MPC converter with one supply and two outputs.

The second method of developing a MPC combines two converters with similar front ends to generate two outputs using only one controlled switch as shown in Figure 3.4.

A method proposed in [109] combines various converters based on their front end. If the front ends of two converters are similar, then the rest of the converter parts are just combined to this front end to realize an MPC. Figure 3.4 shows three configurations of MPCs based on a boost converter. Figure 3.4(a) shows a boost converter combined with a Cuk converter, whereas Figures 3.4(b) and (c) show the boost topology combined with SEPIC and current source converter, respectively. In all the cases, the advantage is a reduction in the number of active switches. This leads to

lower part count, a reduction in driver circuits, and simpler controller implementation. However, this topology has the disadvantage that both outputs cannot be regulated at the same time due to the presence of one controllable switch.

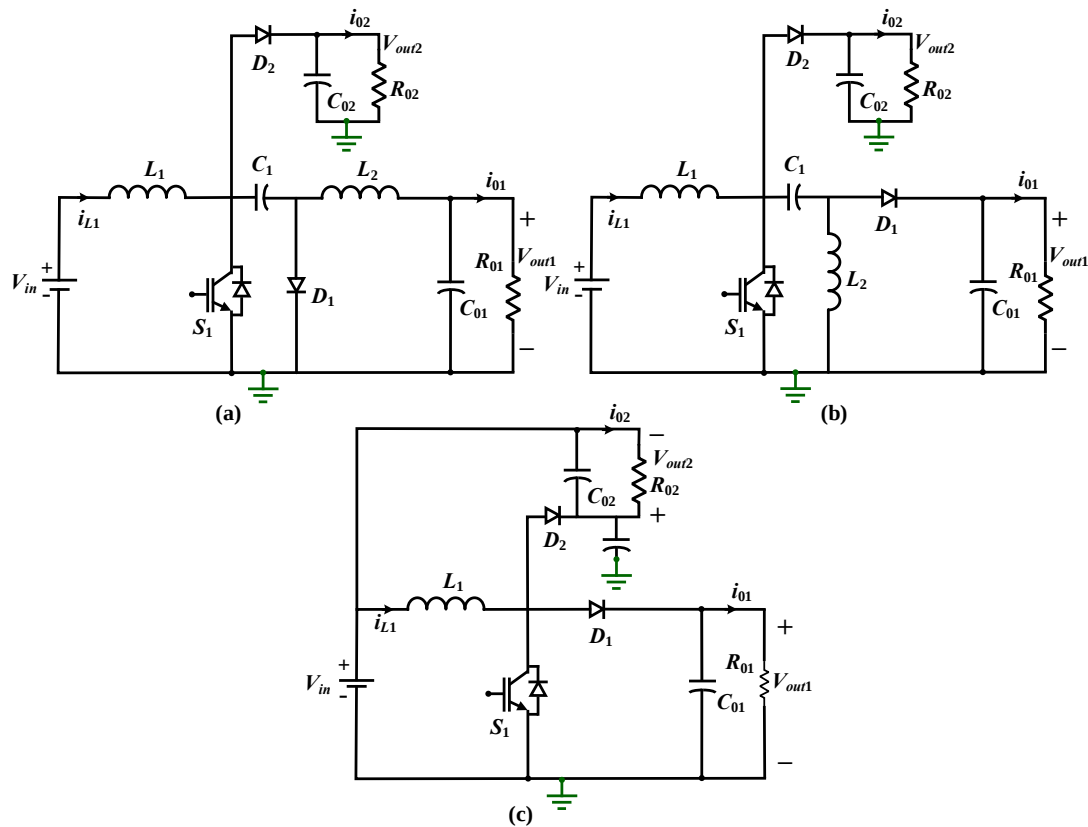
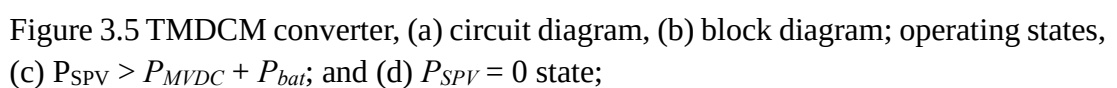


Figure 3.4 Multi-output boost topologies based on mix-match approach. (a) Boost and Cuk topology. (b) Boost and SEPIC topology. (c) Boost and current source topology.

This chapter presents the third method, where a non-isolated time-multiplexed DC-DC multiport (TMDCM) converter architecture devised for dual-output voltage regulation, delivering medium-voltage DC (MVDC) and low-voltage DC (LVDC) for auxiliary subsystems operating on the same ground. The proposed controller design employs the stability boundary locus method together with Kharitonov's theorem to analytically design the robust controller gain limits for time-multiplexed switching scenarios, in which both switches of the same leg operate concurrently. The time-multiplexed switching methodology enhances efficiency and integration.

The TMDCM converter operates in CCM, where the associated modeling and controller design can become analytically intensive, often prompting the neglect of parasitic elements for controllability. Such simplifications yield an idealized, lossless representation that facilitates preliminary analysis and highlights the fundamental operating principles of the converter. However, for accurate prediction of practical behavior, the inclusion of parasitic resistances and non-idealities is essential. Incorporating these effects enables a more faithful characterization of both steady-state and transient responses, thereby improving the reliability of the dynamic model. Accordingly, parasitic components are explicitly considered in this work to develop a comprehensive and realistic representation of the TMDCM converter.

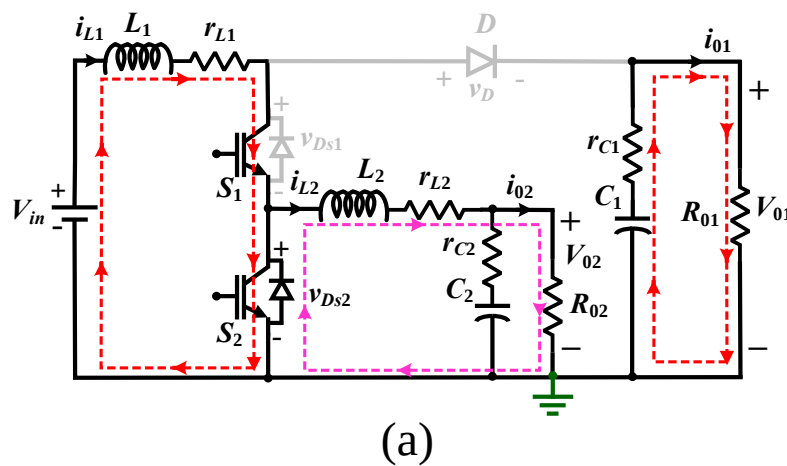


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respectively. The objective of the time-multiplexed MPC topology is to preserve the fundamental dynamic behavior of the converter while minimizing the number of active switches required to achieve multiple output ports.

3.2.1 Mode A Operation Under Non-Ideal Conditions

Figures 3.6(a), (b), and (c) show the equivalent circuit of TMDCM for *mode A* operation under different operating intervals of the converter. The gating signals for the TMDCM converter, G_{s1} and G_{s2} are illustrated in Figure 3.7(a) where d_1 (i.e., $d_1 = D_1 + \hat{d}_1$) and d_2 (i.e., $d_2 = D_2 + \hat{d}_2$) are the controlled signals. The detailed explanation of the TMDCM converter circuit is provided in [23] and [55]. To implement a TMDCM converter topology, the conventional boost operation is initiated by simultaneously turning on the switches S_1 and S_2 , which enables time-multiplexing control. In Figure 3.7(b), the voltage gains at output port-1 (i.e., V_{o1}/V_{in}) of the converter against steady-state duty ratios D_1 and D_2 under different parasitic resistances (r_{L1} , r_{c1}) and load (R_{o1}) conditions are plotted. The ideal gain trajectory $1/(1-D_1)$ serves as a reference, while practical gains vary significantly due to non-idealities. Colored gain zones indicate how parasitic and loading affect performance, such as lower gain with lower resistive loads and higher gain with higher resistive loads. The surface demonstrates the performance across multiple conditions, highlighting the converter's sensitivity to component variations.



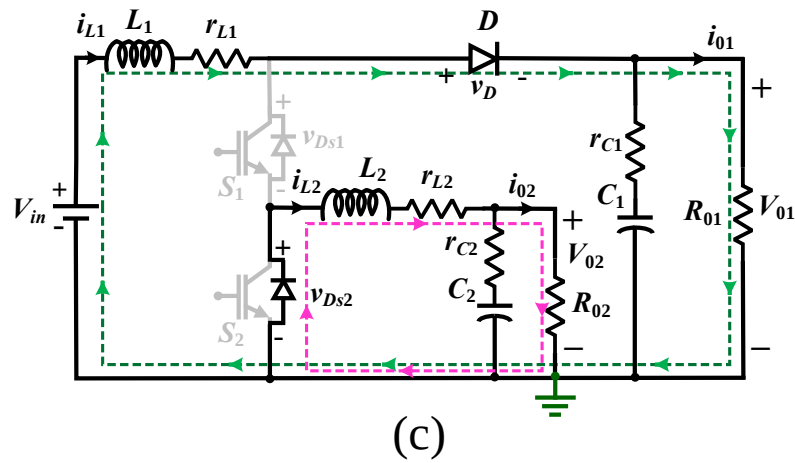
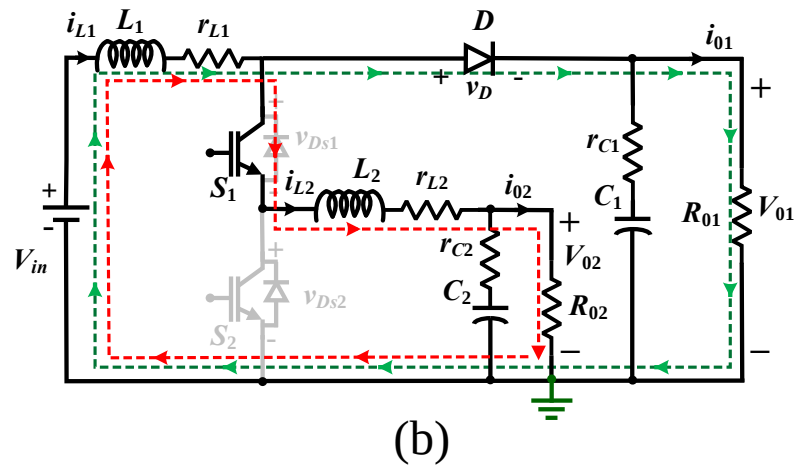
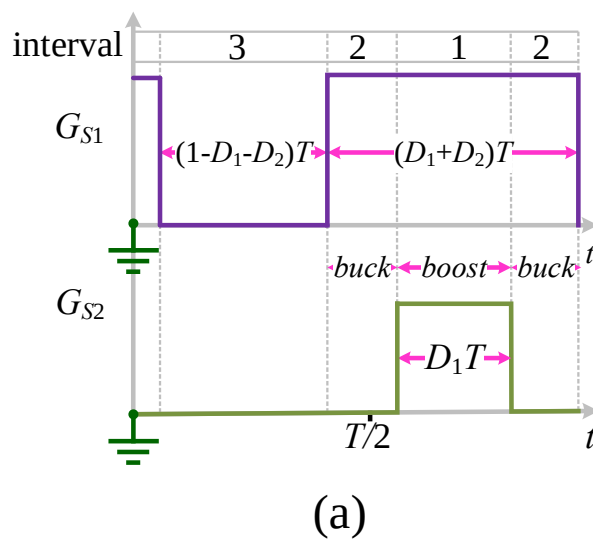


Figure 3.6 TMDCM converter under mode A operation for (a) interval 1, (b) interval 2, and (c) interval 3.



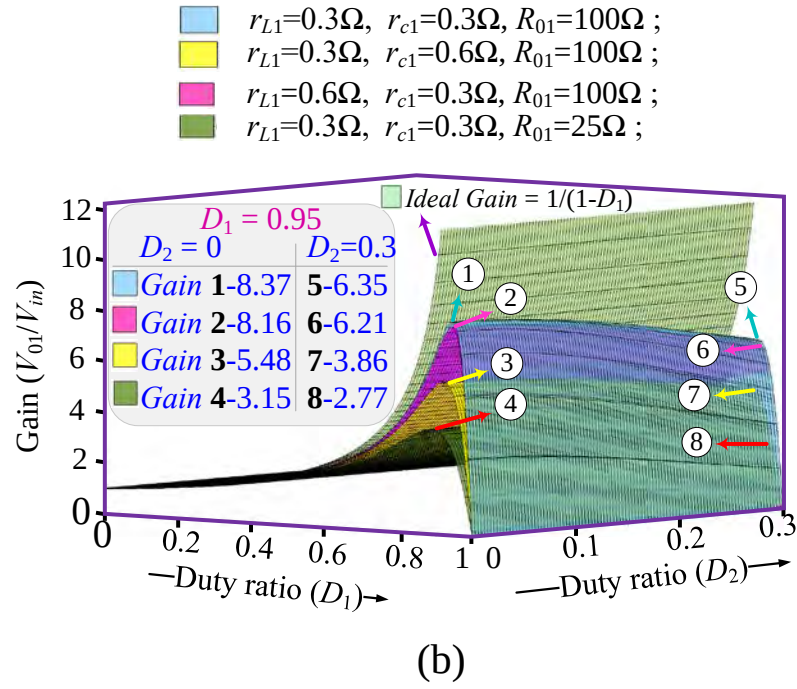


Figure 3.7 Performance analysis of the TMDCM with circuit parasitic under mode A operation (a) switching logic, and (b) voltage gain (V_{01}/V_{in}) characteristics.

3.2.2 Mode B Operation Under Non-Ideal Conditions

Figure 3.8(a) and Figure 3.9(b) show the equivalent circuit of TMDCM for *mode B* operation under different operating intervals of the converter. The gating signals, G_{s1} and G_{s2} are illustrated in Figure 3.9(a) where d_{1b} (i.e., $d_{1b} = \mathbf{D}_{1b} + \hat{\mathbf{d}}_{1b}$) and d_2 (i.e., $d_2 = \mathbf{0}$) are the controlled signals of the switch S_2 and S_1 , respectively.

To implement this operation, the input supply is to be considered as turned *off*, and the conventional boost operation is initiated from the battery side by turning on and *off* the switches S_2 . Figure 3.9(b) illustrates the variation of the voltage gains at output port-1 (i.e., V_{01}/V_{bat}) with respect to the boost duty ratio D_{1b} , where the dashed curve represents the ideal boost gain $1/(1-D_{1b})$ and the solid curves correspond to the practical gain under different parasitic resistance (r_{L2}, r_{c1}) and load conditions. At lower duty ratios, the practical and ideal gains remain closely aligned; however, as D_{1b} approaches unity, the practical gain deviates significantly from the ideal case due to the increasing influence of parasitic elements and load-dependent effects. The maximum observed gain is approximately 8.68 at $D_{1b} = 0.95$, whereas the minimum

gain falls near 5.89, highlighting the performance degradation under non-ideal conditions. This analysis clearly demonstrates that while the theoretical boost converter predicts infinite gain at very high duty ratios, real-time factors such as parasitic resistances and load influence constrain the achievable gain, particularly in high duty ratio operation.

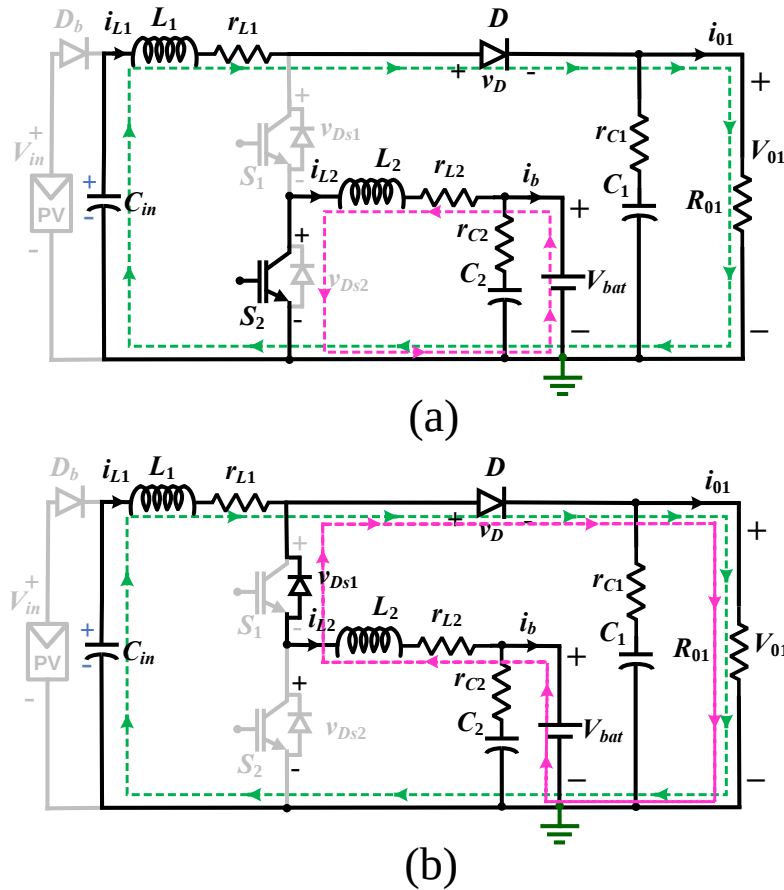
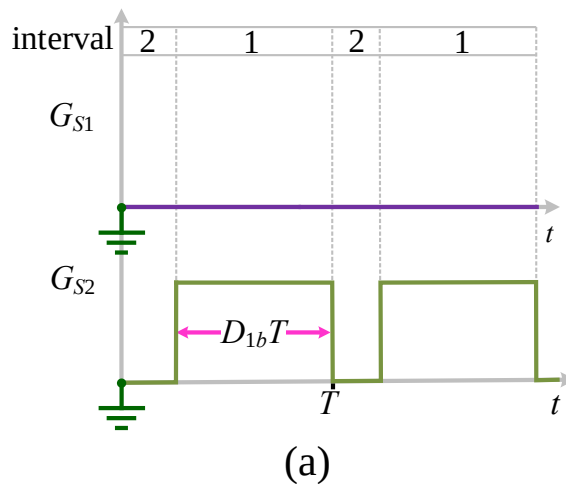


Figure 3.8 TMDCM converter under mode B operation for (a) interval 1, (b) interval 2.



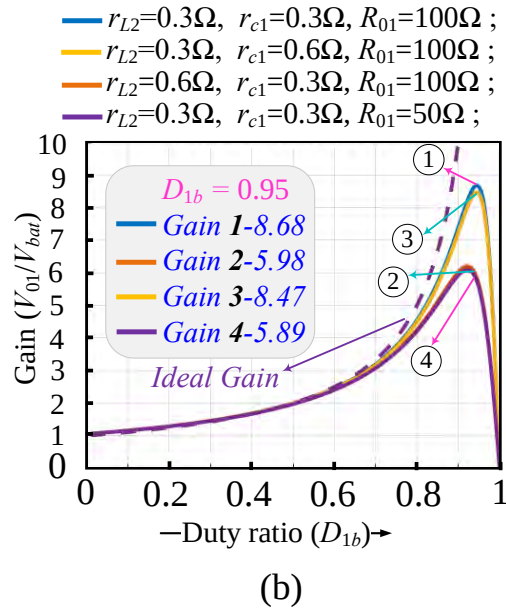


Figure 3.9 Performance analysis of the TMDCM with circuit parasitic under *mode B* operation (a) switching logic, and (b) voltage gain curve (V_{01}/V_{bat}).

3.3 Controllability Analysis of TMDCM Converter

For robust controller development, a thorough control-oriented analysis of the TMDCM converter is imperative. In the context of power electronic converters, controllability evaluation is conventionally segmented into three key categories: (i) *structural controllability*, (ii) *state controllability*, and (iii) *output controllability* [14], [52]. These classifications provide critical insights into the system's dynamic response and facilitate informed controller synthesis under diverse operational conditions. A detailed exposition of these controllability aspects, structured proposition-wise, has been comprehensively addressed in [52]. A comprehensive understanding of the converter's controllability is fundamental to accurately evaluating, refining, and guaranteeing its control performance from a control systems standpoint [104]. In this regard, the TMDCM converter topology is systematically analyzed using a SLS model, which provides a rigorous analytical foundation for capturing the converter's dynamic behavior across multiple switching states.

$$\frac{dx(t)}{dt} = \dot{x}(t) = \mathbf{A}_k x(t) + \mathbf{B}_k u(t) \quad (3.1a)$$

$$y(t) = \mathbf{C}_k x(t) + \mathbf{D}_k u(t) \quad (3.1b)$$

The dynamic behavior of power converters with switching actions is typically investigated using an SLS approach (3.1) for both the operation. In this formulation $x(t)|_A = [i_{L1}, i_{L2}, v_{C1}, v_{C2}]^T$, $x(t)|_B = [i_{L1}, i_{L2}, v_{C1}, v_{Cin}]^T$, $x(t)|_A, x(t)|_B \in \mathbb{R}^{n \times 1}$, $A_k \in \mathbb{R}^{n \times n}$, $B_k \in \mathbb{R}^{n \times p}$, $u(t)|_A = [v_{in}, v_{ss1}, v_{ss2}, v_{Ds2}, v_D]^T$, $u(t)|_B = [v_{bat}, v_D, v_{ss2}, v_{Ds1}]^T$, $u(t)|_A, u(t)|_B \in \mathbb{R}^{p \times 1}$, $C_k \in \mathbb{R}^{q \times n}$ and $D_k \in \mathbb{R}^{q \times p}$, $k \in \{1, 2, \dots, N\}$ represent the system's state, input, and output matrices corresponding to its two output ports for *mode A* and one output port for *mode B*, respectively, with n, p, q , and N denoting the number of state variables, inputs, outputs, and total switching modes, respectively. The averaged small-signal model of the converter is presented in [55] with circuit parasitic for *mode A* operation, whereas all the state switching state matrices without circuit parasitic for both *modes* are presented in [52]. For accurate controller design, the model presented in [23] is extended by incorporating practical parasitic, including the voltage drops across switches and diodes presented in (A.1), thereby offering a more realistic representation of the system behavior under actual operating conditions.

3.3.1 Structural Controllability

Structural controllability implies that input variables influence state variables either directly or indirectly. This property is analyzed using graph theory, typically represented by the matrix $[A|B]$. In SLS, it is evaluated using the large-signal averaged model as follows:

$$\left[\sum_{k=1}^N \Gamma_k A_k \mid \sum_{k=1}^N \Gamma_k B_k \right] \quad (3.2)$$

where Γ_k signifies mode-wise switching sequence.

As illustrated in Figure 3.10, state and input variables are represented in black and magenta, respectively. Green and blue lines depict current-to-current and current-to-voltage dependencies. A vertex denotes a state variable, while a directed edge signifies influence between variables. The direction of the arrow indicates that the source state or input variable affects the destination state variable. This interconnection suggests that future states are influenced by present states or inputs. The resulting graph forms a 'tree,' where input variables serve as the 'root.' If all state variables are

controllable through the *root*, excluding the *root* itself system is structurally controllable.

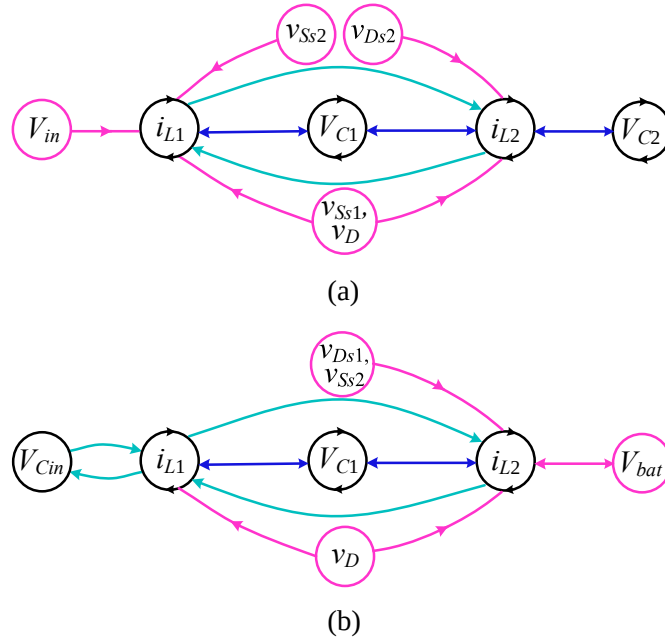


Figure 3.10 Structural controllability with circuit parasitic under (a) *mode A*, and (b) *mode B*.

3.3.2 State Controllability

A state vector $x \neq 0$ is deemed controllable if, over a finite time interval $[0, t_{finite}]$, there exists a switching sequence Γ and a continuous input $u(t)$ that can drive the system from an initial condition $x(0) = x_0$ to the $x(t_{finite}) = 0$, where zero vector represents stable operating point achieved within finite time period t_{finite} . This condition ensures that the system possesses adequate control authority to steer any arbitrary non-zero state to the target point within time t_{finite} . Thus, system (3.1) is considered state controllable if every state vector $x \neq 0$ satisfies this criterion [52]. For a matrix $A \in \mathbb{R}^{n \times n}$ and a subspace $z \in \mathbb{R}^{n \times n}$. The cyclic invariant subspace (CIS) of A with respect to z , denoted as $A|z$, is defined as follows:

$$\langle A|z \rangle = \sum_{k=1}^n A^{k-1} z \quad (3.3a)$$

For an SLS shown in (3.1), the linear subspace sequence is expressed as follows:

$$z_1 = \sum_{k=1}^N \langle A_k | B_k \rangle, z_2 = \sum_{k=1}^N \langle A_k | z_1 \rangle, \dots, z_n = \sum_{k=1}^N \langle A_k | z_{n-1} \rangle \quad (3.3b)$$

Proposition 1: (satisfactory state) If the state of the system (3.1) exhibits controllability, then $\text{rank}(z_1) = n$.

Proposition 2: (essential state) If the state of the system (3.1) exhibits controllability, then $\text{rank}(z_n) = n$.

Based on (3.3b), the decision matrix z_1 corresponding to a state-controllable system for *modes A* (i.e., $z_1|_A$) and *mode B* (i.e., $z_1|_B$) is determined as follows:

$$\begin{aligned} z_1|_A &= \langle A_1 | B_1 \rangle + \langle A_2 | B_2 \rangle + \langle A_3 | B_3 \rangle \\ &= B_1 + A_1 B_1 + A_1^2 B_1 + A_1^3 B_1 + B_2 + A_2 B_2 + \\ &\quad A_2^2 B_2 + A_2^3 B_2 + B_3 + A_3 B_3 + A_3^2 B_3 + A_3^3 B_3 \end{aligned} \quad (3.3c)$$

$$\begin{aligned} z_1|_B &= \langle A_1 | B_1 \rangle + \langle A_2 | B_2 \rangle = B_1 + A_1 B_1 + A_1^2 B_1 + A_1^3 B_1 + B_2 \\ &\quad + A_2 B_2 + A_2^2 B_2 + A_2^3 B_2 \end{aligned} \quad (3.3d)$$

From (3.3c), $z_1|_A$ is calculated for *mode A* as $1 \times 10^{14} [1.0881 \ -0.9632 \ -1.2761 \ -5.1142]^T$. Similarly, the other CIS sequences are calculated as $z_2|_A = 1 \times 10^{25} [-0.1646 \ -2.0030 \ -0.0033 \ -0.8000]^T$, $z_3|_A = 1 \times 10^{36} [0.0286 \ -1.3582 \ 0.2161 \ 4.5657]^T$, $z_4|_A = 1 \times 10^{47} [0.1775 \ 0.3769 \ 0.1934 \ 5.9991]^T$ and from (3.3d), $z_1|_B$ is calculated for *mode B* as $1 \times 10^{14} [-2.8367 \ -0.2275 \ -0.3493 \ 2.1054]^T$. Similarly, $z_2|_B = 1 \times 10^{25} [-4.2622 \ 0.2142 \ 0.8148 \ -9.0736]^T$, $z_3|_B = 1 \times 10^{37} [0.2389 \ 0.0234 \ 0.1860 \ -1.9757]^T$, $z_4|_B = 1 \times 10^{48} [1.6192 \ -0.0313 \ 0.0206 \ -0.0998]^T$.

According to **Proposition 2**, for *mode A* operation $\text{rank}(z_4|_A) = \text{rank}(z_3|_A) = \text{rank}(z_2|_A) = \text{rank}(z_1|_A)$. The column vectors $A_1^3 B_1, A_2^3 B_2, A_3^3 B_3$, and $A_3^2 B_3$ in (3.3c) are linearly independent. Hence, $z_1 = \text{span}(A_1^3 B_1, A_2^3 B_2, A_3^3 B_3, A_3^2 B_3)$, i.e., $z_1|_A = 4$. Similarly, for *mode B* operation $\text{rank}(z_4|_B) = \text{rank}(z_3|_B) = \text{rank}(z_2|_B) = \text{rank}(z_1|_B)$.

The column vectors $A_1^3 B_1, A_1^2 B_1, A_2^3 B_2$ and $A_2^2 B_2$ in (3.3d) are linearly independent. Hence, $z_1|_B = \text{span}(A_1^3 B_1, A_1^2 B_1, A_2^3 B_2, A_2^2 B_2)$, i.e., $z_1|_B = 4$. Additionally, the remaining CIS sequences

are calculated as $z_1|_A$ and $z_1|_B$ which satisfies **Propositions 1** and **2**, that is, $z_1|_{A,B} = 4$ and $z_n|_{A,B} = 4$. Therefore, the system is state controllable.

3.3.3 Output Controllability

In an SLS, output controllability refers to the system's capability to drive its output vector to any specified final value within a finite time span, by applying a suitable control input and switching sequence [52]. A system described by (3.1) is deemed output controllable if, for any initial state $x_0 \in \mathbb{R}^{n \times 1}$, desired final output $y_f \in \mathbb{R}^{q \times n}$, and an arbitrary initial control function $u_0(t)$, there exists a continuous control input $u(t)$ such that the output transitions from $x(0) = x_0$ to $y(t_{finite}) = y_f$, within a finite time t_{finite} .

Proposition 3: The state of the system (3.1) exhibits output controllability if $c_k z_n = \mathbb{R}^q$.

In *mode A* operation, there are three switching states and order $n = 4$ and $q = 1$. The computation of $C_1 z_4|_A$, $C_2 z_4|_A$ and $C_3 z_4|_A$ as 1.9277×10^{46} , 1.3314×10^{46} and 2.4587×10^{46} , respectively, for the 1st output variable, and for the 2nd output variable, all the modes are the same, so $C_{02} z_4$ is 5.9924×10^{47} . Similarly, in *mode B* operation, there are two switching states and order $n = 4$ and $q = 1$. The computation of $C_1 z_4|_B$ and $C_2 z_4|_B$ as 5.0488×10^{47} and 5.1425×10^{47} , respectively, for the 1st output variable. Hence, the system satisfies **Proposition 3**. Therefore, the system is output controllable.

3.4 Motivation for Robust Control Under Structured Uncertainties

Modern power electronic systems, particularly those associated with renewable energy integration and electric vehicle charging applications, are inherently subjected to parametric variations and structured uncertainties arising from both internal and external factors. These uncertainties are not purely stochastic; rather, they exhibit identifiable patterns linked to system parameters such as inductance, capacitance, parasitic resistances, switching delays, and operating point variations.

Conventional linear controllers, designed around a fixed operating point, often fail to guarantee satisfactory performance when subjected to such structured deviations. Even advanced control strategies relying on precise system modeling tend to degrade under model plant mismatch, especially in high-frequency switched

systems where unmodeled dynamics and parasitic effects become significant. This limitation is particularly critical in DC-DC converters, where small parameter deviations can lead to:

- i. degradation in transient response
- ii. increased steady-state error
- iii. potential instability under extreme operating scenarios

Structured uncertainties, unlike unstructured disturbances, possess a known configuration but uncertain magnitude, making them suitable inputs for systematic robust control design. For instance, variations in converter inductance due to magnetic saturation or temperature effects can be bounded but not precisely predicted. Similarly, switching device non-idealities introduce repeatable yet uncertain perturbations in system dynamics.

The motivation for employing robust control methodologies lies in their ability to ensure guaranteed stability and performance within a predefined uncertainty set. and in this chapter, it has been considered that Kharitonov's law is particularly relevant in this context, as they explicitly account for worst-case scenarios rather than nominal conditions. In power electronic converters, robust control facilitates:

- i. maintenance of regulation accuracy across wide input/output variations
- ii. preservation of dynamic performance under parameter drift
- iii. immunity against external disturbances and load transients
- iv. reliable operation in the presence of modeling inaccuracies

Furthermore, the increasing adoption of multi-port and bidirectional DC-DC converter systems introduces higher-order dynamics and stronger coupling between subsystems. This complexity amplifies the sensitivity of the system to structured uncertainties, thereby necessitating control strategies that can handle multi-variable interactions and coupled dynamics without compromising stability margins.

In summary, the integration of renewable energy sources, energy storage systems, and advanced power electronic converters creates a highly dynamic and uncertainty-prone environment. The adoption of robust control under structured uncertainties is therefore not merely an enhancement but a necessity to ensure reliable, efficient, and stable operation of next-generation standalone EV charging systems.

3.4.1 Robust Controller Design

The small-signal model (SSM) given in [14] is used to derive the open-loop transfer functions (OLTF) $\hat{v}_{C1}/\hat{d}_1$, $\hat{v}_{C2}/\hat{d}_2$ for *mode A* and $\hat{v}_{C1}/\hat{d}_{1b}$ for *mode B* operations, respectively. Utilizing the system parameters with direct current resistance (DCR) of L_1 and L_2 as 0.1Ω and 0.3Ω , and equivalent series resistance (ESR) of rc_1 and rc_2 as 0.3Ω . The steady-state values obtained from the experimental setup for both modes of operation, such as duty cycles, corresponding inductor currents, voltages, and load resistances for *mode A* operation, are as follows: $D_1 = 0.667$, $D_2 = 0.208$, $I_{L1} = 2.58$ A, $I_{L2} = 0.8784$ A, $V_{01} = 67.7$ V and $V_{02} = 13.18$ V, with corresponding load resistances $R_{01} = 100 \Omega$ and $R_{02} = 15 \Omega$. Whereas for *mode B* operation $D_{1b} = 0.667$, $I_{L1} = 0$ A, $I_{L2} = -2.095$ A and $V_{01} = 69.76$ V, with corresponding load resistances $R_{01} = 100 \Omega$. The decrease in steady-state voltages is due to system DCR and ESR. Based on these parameters and operational conditions, the transfer functions (TFs) are derived as per [64] and are expressed in (3.4a), (3.4b) and (3.4c) for *mode A* and *mode B*, respectively, as follows:

$$\left. \frac{\hat{v}_{C1}(s)}{\hat{d}_1} \right|_{\hat{v}_{in}, \hat{d}_2=0} = \frac{-0.7721s^4 + 8336s^3 + 3.946 \times 10^7 s^2 + 1.386 \times 10^{11} s + 3.547 \times 10^{14}}{s^4 + 1675s^3 + 1.073 \times 10^7 s^2 + 3.93 \times 10^9 s + 1.829 \times 10^{12}} \quad (3.4a)$$

$$\left. \frac{\hat{v}_{C2}(s)}{\hat{d}_2} \right|_{\hat{v}_{in}, \hat{d}_1=0} = \frac{2.012 \times 10^4 s^3 + 6.778 \times 10^8 s^2 + 2.474 \times 10^{11} s + 1.222 \times 10^{14}}{s^4 + 1675s^3 + 1.073 \times 10^7 s^2 + 3.93 \times 10^9 s + 1.829 \times 10^{12}} \quad (3.4b)$$

$$\left. \frac{\hat{v}_{C1}(s)}{\hat{d}_{1b}} \right|_{\hat{v}_{bat}=0} = \frac{-0.6266s^4 + 3.793 \times 10^3 s^3 + 1.068 \times 10^7 s^2 + 1.017 \times 10^{11} s + 3.685 \times 10^{14}}{s^4 + 1657s^3 + 2.007 \times 10^7 s^2 + 7.965 \times 10^9 s + 1.854 \times 10^{12}} \quad (3.4c)$$

The closed-loop control logic is given in Figure 3.11. The open-loop poles reside in the LHP of the s-plane, confirming the inherent stability of the OLTF. The boost-mode operation, on the other hand, shows non-minimum phase behaviour because of the presence of a RHP zero [17], [64]. As a result, PI compensation is necessary to make sure that the closed-loop system stays stable. conventional controller design depends on a plant model with parameters that are readily apparent. However, in real-world implementations, achieving an exact match between the theoretical model and the physical system is seldom feasible due to inherent discrepancies and parameter variations. Consequently, system uncertainties must be

explicitly considered, requiring adaptations to the nominal plant model to accurately capture these deviations and ensure the controller's robustness.

Figures 3.11(a) and (c) illustrate boost operating modes of the converter in *port* 1 and buck operating modes in *port* 2 during resistive load, CCCV mode for battery charging, respectively, under structured uncertainties in the input voltage V_{in} and the load resistance R_{01} for *mode A* operation. Whereas Figure 3.11(b) demonstrates boost operation under structured uncertainties in the battery voltage V_{bat} and the load resistance R_{01} for *mode B* operation. The load resistance R_{01} is varied within a range of $50\ \Omega$ to $200\ \Omega$, with $100\ \Omega$ is selected as the nominal value for the plant model. Likewise, the input voltage V_{in} and battery voltage V_{bat} is considered within the bounds of 22 V to 40 V and 22 V to 26 V, respectively, while 24 V serves as the nominal operating point for both *modes*.

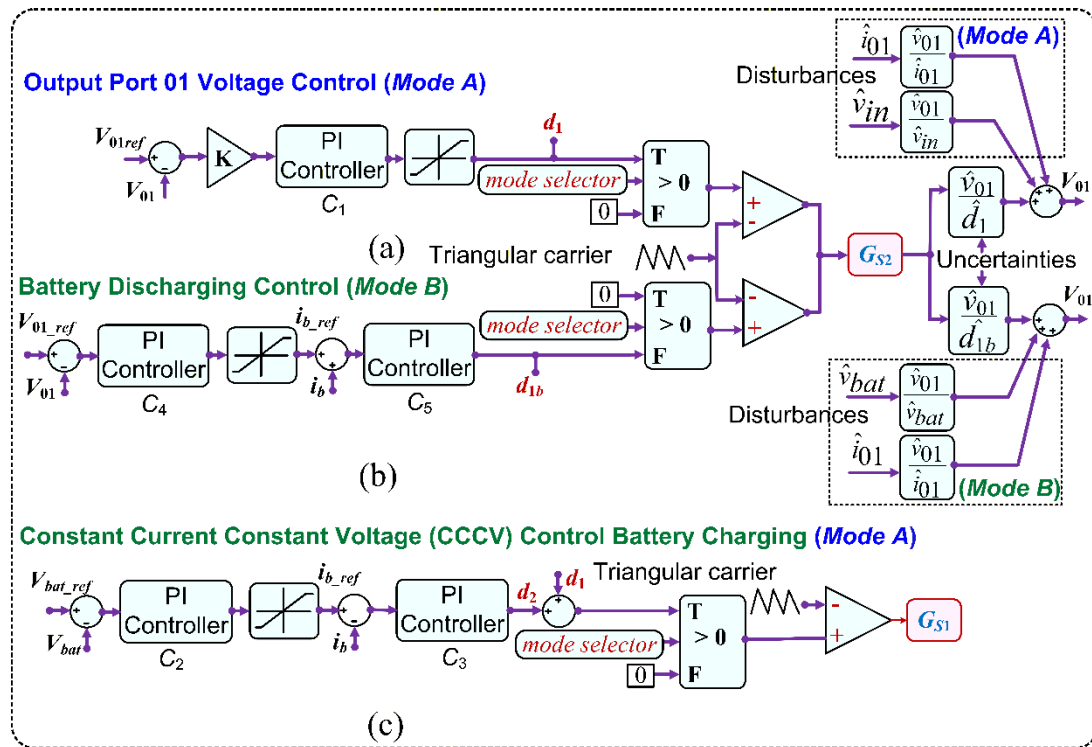


Figure 3.11 Closed-loop control of TMDCM converter.

3.4.1.1 Kharitonov's Theorem

System uncertainties cause the coefficients of the plant's TFs to fluctuate within defined bounds. Consequently, controller design must account for the most adverse

operating conditions to guarantee reliable system performance. To address this, the stability boundary locus method is employed to delineate the permissible range of PI controller parameters. Kharitonov's theorem [103] also provides a strong and mathematically elegant framework for dealing with the limited variability of interval transfer functions that come from parametric uncertainties. The theorem asserts that an interval polynomial representing an infinite family of possible plant models is Hurwitz stable if and only if a certain group of four Kharitonov polynomials is stable. Consider, for instance, an interval polynomial corresponding to the plant under analysis is as follows: -

$$P = q_0 + q_1 s^1 + \dots + q_m s^m + \dots q_r s^r, q_m \in [q_m^-, q_m^+] \quad (3.5)$$

In this case, the polynomial coefficients $[q_m^-, q_m^+]$ depend on the system's uncertainties and can change within set minimum and maximum limits. As per Kharitonov's theorem, the interval polynomial P defined in (3.5) is deemed stable if the following four specifically constructed Kharitonov polynomials (3.6) are Hurwitz stable [15], [104].

$$\begin{aligned} P_1(s) &= q_0^- + q_1^- s^1 + q_2^+ s^2 + q_3^+ s^3 + q_4^- s^4 + q_5^- s^5 + q_6^+ s^6 + q_7^+ s^7 + q_8^- s^8 \dots \\ P_2(s) &= q_0^+ + q_1^+ s^1 + q_2^- s^2 + q_3^- s^3 + q_4^+ s^4 + q_5^+ s^5 + q_6^- s^6 + q_7^- s^7 + q_8^+ s^8 \dots \\ P_3(s) &= q_0^+ + q_1^- s^1 + q_2^- s^2 + q_3^+ s^3 + q_4^+ s^4 + q_5^- s^5 + q_6^- s^6 + q_7^+ s^7 + q_8^+ s^8 \dots \\ P_4(s) &= q_0^- + q_1^+ s^1 + q_2^+ s^2 + q_3^- s^3 + q_4^- s^4 + q_5^+ s^5 + q_6^+ s^6 + q_7^- s^7 + q_8^- s^8 \dots \end{aligned} \quad (3.6)$$

The interval plant is considered as,

$$G_{ij}(s) = \frac{num_G^i(s)}{den_G^j(s)}, \quad (i, j = 1, 2, 3, 4) \quad (3.7)$$

In this context, num_G^i and den_G^j represent the Kharitonov's polynomials for the numerator and denominator of the nominal plant transfer function, respectively. A controller $C = Num_c / Den_c$ will stabilise the aforementioned interval plant family if and only if it concurrently stabilises 16 Kharitonov's plants (3.7) according to Routh-Hurwitz stability criteria. The concurrent stabilisation of 16 interval plants will provide a sufficient condition for robust stability. This attribute will be utilised for the synthesis

of the robust controller by mapping 16 plants onto the controller parameter plane in the next heading.

$$\left(den_G^i \times Den_C\right) + \left(num_G^i \times Num_C\right) = 0. \quad (3.8)$$

$$K_p \Big|_{\hat{v}_{C1}/\hat{d}_1} = \frac{0.7721\omega^8 + 1.72 \times 10^7 \omega^6 - 5.119 \times 10^{14} \omega^4 + 3.335 \times 10^{21} \omega^2 - 6.488 \times 10^{26}}{0.5961\omega^8 + 1.304 \times 10^8 \omega^6 - 1.301 \times 10^{15} \omega^4 - 8.786 \times 10^{21} \omega^2 + 1.258 \times 10^{29}} \quad (3.9a)$$

$$K_i \Big|_{\hat{v}_{C1}/\hat{d}_1} = \frac{1294\omega^8 + 6.307 \times 10^{10} \omega^6 - 7.493 \times 10^{17} \omega^4 + 1.394 \times 10^{24} \omega^2 - 2.535 \times 10^{23}}{0.5961\omega^8 + 1.304 \times 10^8 \omega^6 - 1.301 \times 10^{15} \omega^4 - 8.786 \times 10^{21} \omega^2 + 1.258 \times 10^{29}} \quad (3.9b)$$

$$K_p \Big|_{\hat{v}_{C1}/\hat{d}_{1b}} = \frac{0.6266\omega^8 - 8.18 \times 10^6 \omega^6 - 3.829 \times 10^{14} \omega^4 + 6.604 \times 10^{21} \omega^2 - 6.832 \times 10^{26}}{0.3926\omega^8 + 2.778 \times 10^7 \omega^6 - 1.119 \times 10^{15} \omega^4 + 2.471 \times 10^{21} \omega^2 + 1.358 \times 10^{29}} \quad (3.9c)$$

$$K_i \Big|_{\hat{v}_{C1}/\hat{d}_{1b}} = \frac{1038\omega^8 + 1.27 \times 10^{10} \omega^6 - 6.957 \times 10^{17} \omega^4 + 2.935 \times 10^{24} \omega^2 - 1.885 \times 10^{23}}{0.3926\omega^8 + 2.778 \times 10^7 \omega^6 - 1.119 \times 10^{15} \omega^4 + 2.471 \times 10^{21} \omega^2 + 1.358 \times 10^{29}} \quad (3.9d)$$

3.4.1.2 Stability Boundary Locus

This method maps the imaginary axis of the complex s-plane onto the controller dimension space, as described in [104]. The technique involves solving the characteristic equation across a range of frequencies ω , generating the stability boundary locus $L(K_p, K_i, \omega)$. This boundary effectively demarcates the region within the K_p - K_i design space where the closed-loop system is robustly stable. Optimal tuning of the proportional and integral gains is carried out based on the TFs formulations for both *modes* given in (3.4a), (3.4b), and (3.4c), which are frequency-dependent, and further evaluated using (3.5), (3.6), (3.7), and (3.8) to generate (3.9a), (3.9b), (3.9c) and (3.9d). The robust stability region shown in Figure 3.12(a) and Figure 3.13(a) are derived using the 16-plant extension of Kharitonov's theorem, accounting for parametric uncertainties in input voltage V_{in} (ranging from 22 V to 40 V) and load resistance R_{01} (spanning 50 Ω to 200 Ω) for *mode A* operation, whereas for *mode B* battery voltage V_{bat} (ranging from 22 V to 26 V) and load resistance R_{01} span same as *mode A*. The intersection of the stability regions for all 16 Kharitonov plants defines the robust performance region for the controller. Additionally, Figure 3.12(b) and Figure 3.13(b), Figure 3.12(c) and Figure 3.13(c), and Figure 3.12(d) and Figure 3.13(d), illustrate the Bode response of the uncompensated and compensated transfer

functions from (3.4a) and (3.4c), the Nyquist plot of the compensated system, and the closed-loop step response, respectively, for both operating *modes*.

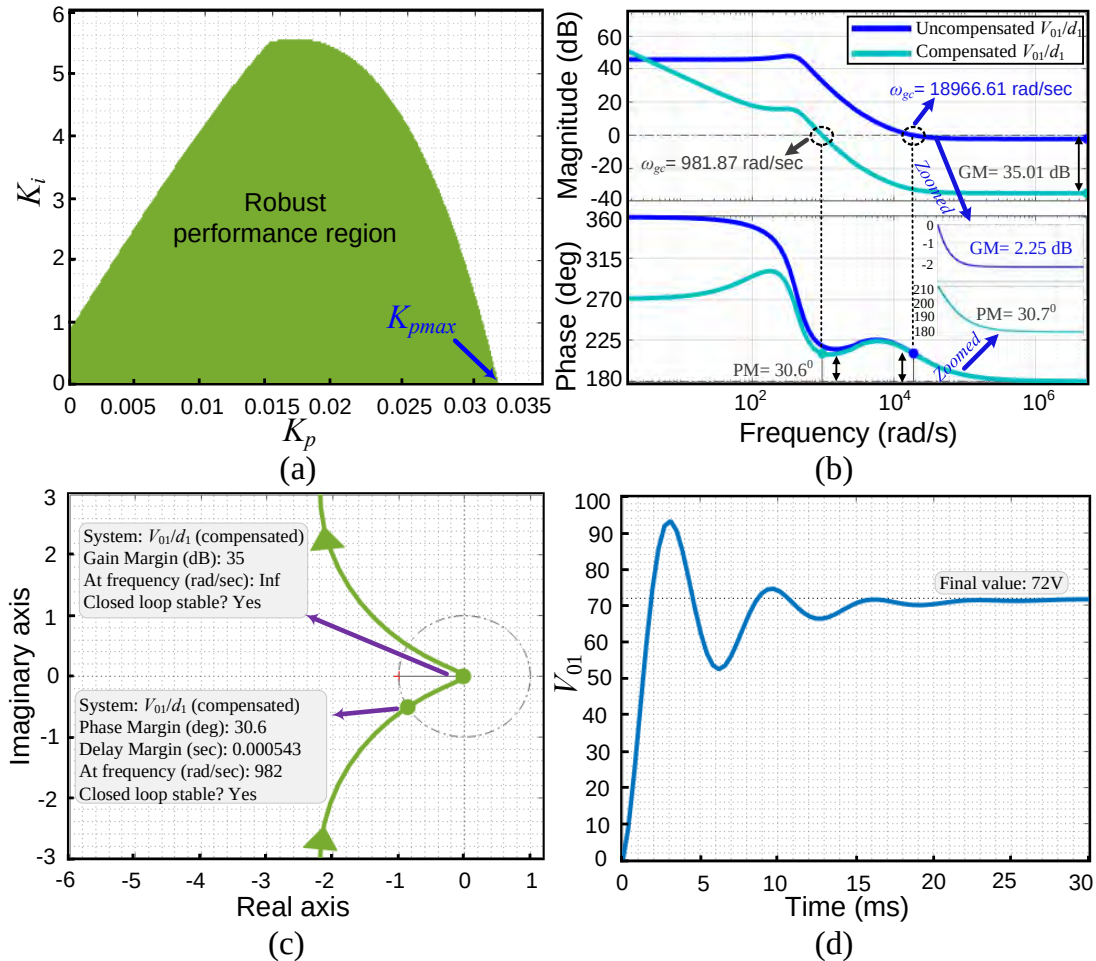
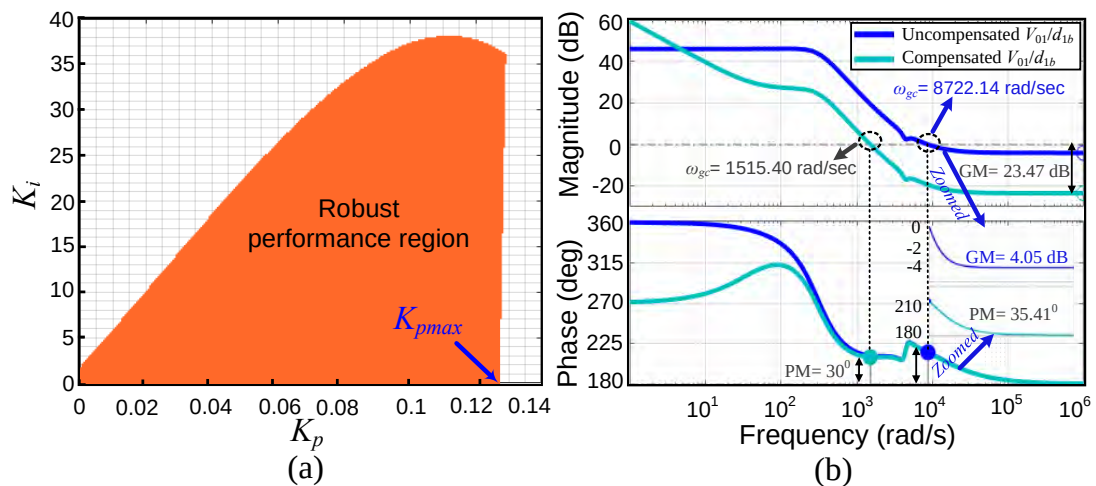


Figure 3.12 Performance analysis in the frequency domain for *mode A* using (a) robust stable boundary locus, (b) Bode plots of the uncompensated and compensated systems, (c) Nyquist plot, and (d) step response of the closed-loop system.



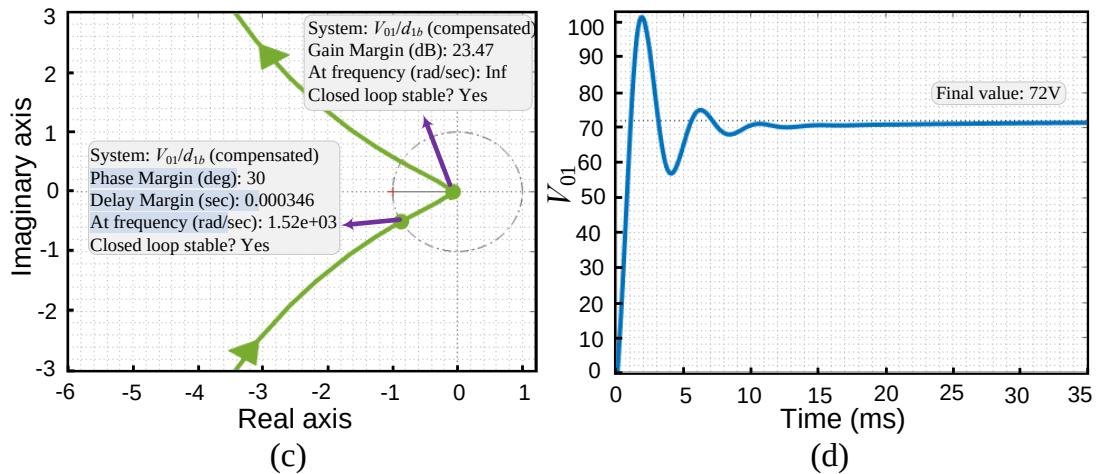
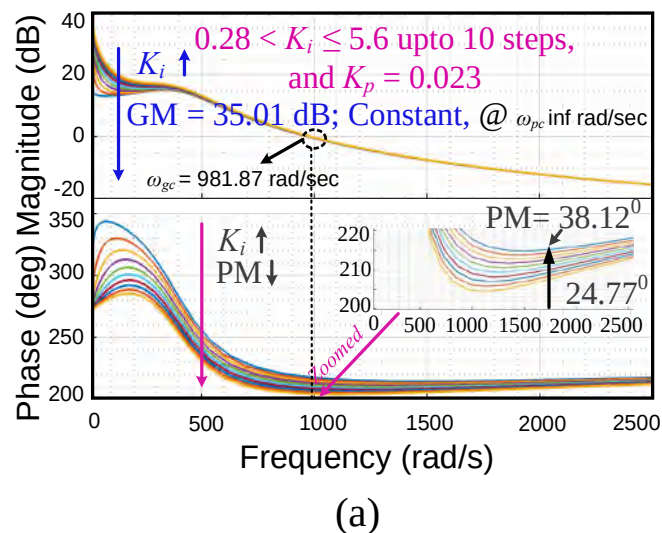


Figure 3.13 Performance analysis in the frequency domain for *mode B* using (a) robust stable boundary locus, (b) Bode plots of the uncompensated and compensated

3.4.1.3 Selection of K_p and K_i

Figure 3.12(a) and Figure 3.13(a) present the robust stability locus for the controller parameter space, where the proportional gain K_p varies from 0 to a maximum value of 0.034 and 0 to a maximum value of 0.13 and the integral gain K_i ranges from 0 to 5.6 and 0 to 38 for *mode A* and *mode B*, respectively. Within this region, the optimal combination of K_p and K_i values is identified through frequency-domain analysis as illustrated in Figures 3.14(a), (b) and Figure 3.15(a), (b).



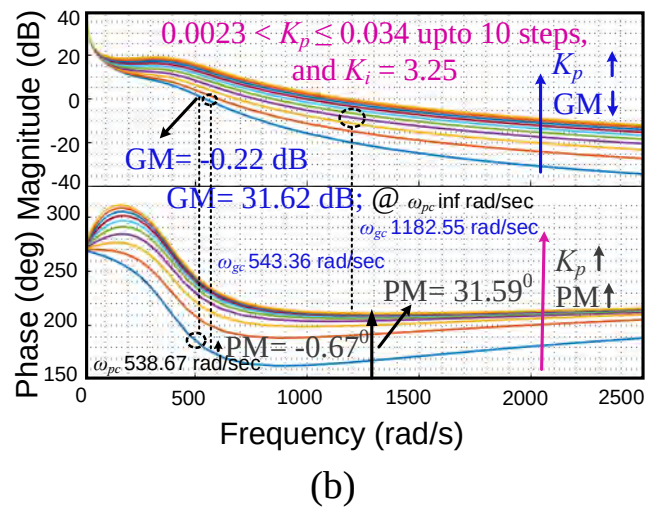


Figure 3.14 Selection of K_p - K_i value using frequency domain analysis for *mode A* with (a) $K_p = 0.023$, K_i variable, and (b) $K_i = 3.25$, K_p variable.

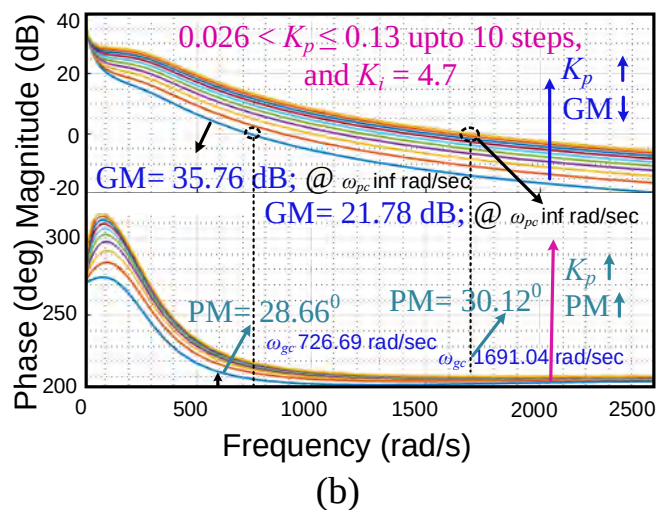
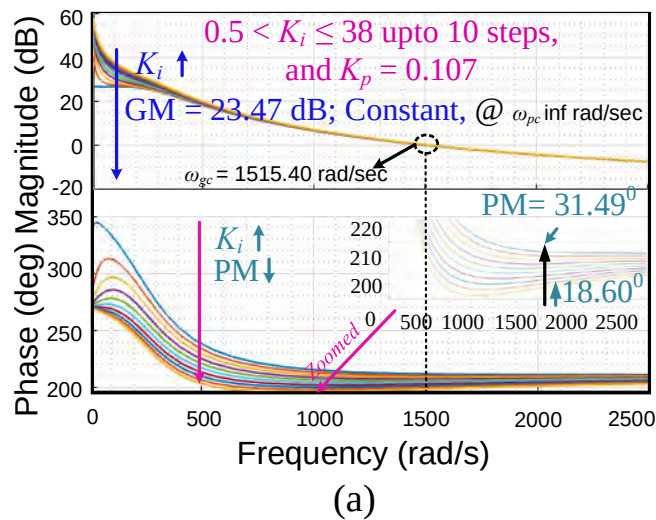


Figure 3.15 Selection of K_p - K_i value using frequency domain analysis for *mode B* with (a) $K_p = 0.107$, K_i variable, and (b) $K_i = 4.7$, K_p variable.

For *mode A*, in Figure 3.14(a), for controller C_1 , K_p is fixed at 0.023 while K_i is varied up to 10 steps. The analysis reveals that increasing K_i results in a decreasing phase margin (PM), while the gain margin (GM) remains nearly constant at 35.01 dB, with the phase crossover frequency (ω_{pc}) approaching infinity. The maximum observed PM is 38.12° at $K_i=0.28$ and the minimum PM is 24.77° at $K_i=5.6$. A suitable operating point is selected where PM exceeds 30° which occurs at $K_i=3.25$ corresponding to a gain crossover frequency (ω_{gc}) of 981.87 rad/s indicating robust stability. Further, in Figure 3.14(b), keeping $K_i=3.25$ fixed and varying K_p up to 10 steps is presented. In this case, both PM and GM are observed to vary, i.e., with increasing K_p , resulting in PM increases while GM decreases. The maximum GM is 46.94 dB at ω_{pc} approaching infinity, and the minimum GM is -0.22 dB at 538.67 rad/s. Similarly, the PM varies from a maximum of 31.59° at 1182.55 rad/s to a minimum of -0.67° at 543.36 rad/s. The occurrence of negative PM and GM at certain values signifies system instability. Therefore, the coinciding stable region identified in both analyses, where robust performance and stability are achieved, is selected. The final controller parameters are thus chosen as $K_p = 0.023$ and $K_i = 3.25$. For *mode B*, in Figure 3.15(a), for controller C_5 , K_p is fixed at 0.107 while K_i is varied up to 10 steps. The analysis remains similar to the previous mode, while the GM remains nearly constant at 23.47 dB with the ω_{pc} approaching infinity. The maximum observed PM is 31.49° at $K_i=0.5$, and the minimum PM is 18.60° at $K_i=38$. The suitable operating point is selected where PM is 30° , which occurs at $K_i=4.67$, corresponding to a ω_{gc} of 1515.40 rad/s, indicating robust stability. In Figure 3.15(b), keeping $K_i=4.67$ fixed and varying K_p up to 10 steps is presented. The analysis reveals similar performance to the previous mode. The maximum and minimum GM are 35.76 dB and 21.78 dB at ω_{pc} approaching infinity. Similarly, the PM varies from a maximum of 30.12° at 1691.04 rad/s to a minimum of 28.66° at 726.69 rad/s. The final controller parameters are thus chosen as $K_p = 0.107$ and $K_i = 4.7$.

3.4.1.4 Sensitivity Analysis

Figures 3.16(a) and (b) illustrate the sensitivity and complementary sensitivity functions of the developed robust controller for the chosen K_p and K_i values in both operating modes, i.e., mode *A* and mode *B* using (3.10a) and (3.10b) in response to

fluctuations in source voltage 22-40 V and load resistance 50-200 Ω [2]. The maximum values of sensitivity ($|S(s)|$) and complementary sensitivity ($|T(s)|$) functions derived from the plots are 1.9 and 1.8 for *mode A* and *mode B*, respectively. As a result, the suggested controller exhibits significant robustness while still providing satisfactory dynamic performance.

$$|S(s)| = \left| \frac{1}{1 + \hat{v}_{C1}(s)/\hat{d}_1} \right| \quad (3.10a)$$

$$|T(s)| = \left| \frac{\hat{v}_{C1}(s)/\hat{d}_1}{1 + \hat{v}_{C1}(s)/\hat{d}_1} \right| \quad (3.10b)$$

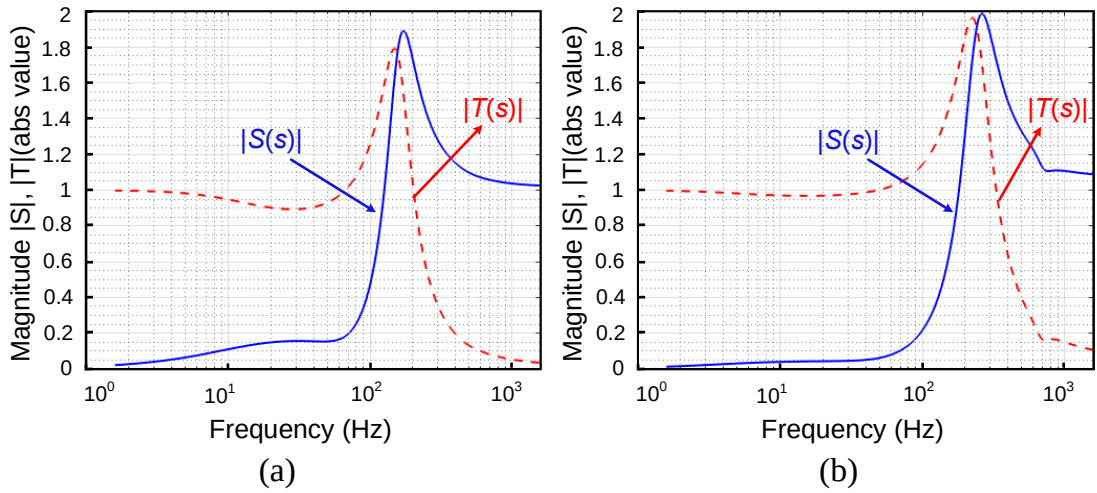


Figure 3.16 Sensitivity and complementary function for (a) *mode A* and (b) *mode B*.

3.5 Experimental Validations

The experimental validation illustrates the dynamic behaviour and efficacy of the proposed TMDCM converter across diverse operating conditions. This section contains a thorough examination and conversation about the results. An experimental prototype was developed to test the converter's effectiveness, with a peak power of 100 W and a switching frequency of 20 kHz, as shown in Figure 3.17. The input voltage V_{in} is realized using the GW INSTEK ASR-2100, a programmable AC/DC source. System control and power management are executed using TI F28379D controller. Voltage and current feedback are precisely measured using LV25-P voltage sensors and ACS712 Hall-effect current sensors, respectively, enabling accurate signal acquisition for closed-loop control. It confirms the controllability, dynamic response,

and overall performance of the TMDCM converter. This section provides a comprehensive analysis and interpretation of the obtained results. The used parameters are illustrated in Table 3.1. Experimental outcomes are presented in Figure 3.18 to Figure 3.21. Channel 1 exhibits a switching pulse G_{s1} and G_{s2} of the system, whereas channels 2, 3 and 4 are i_{L2} , i_{01} , and i_{L1} , respectively. The channels 5, 6 and 7 show voltages of port 01, input, and port 02, respectively.

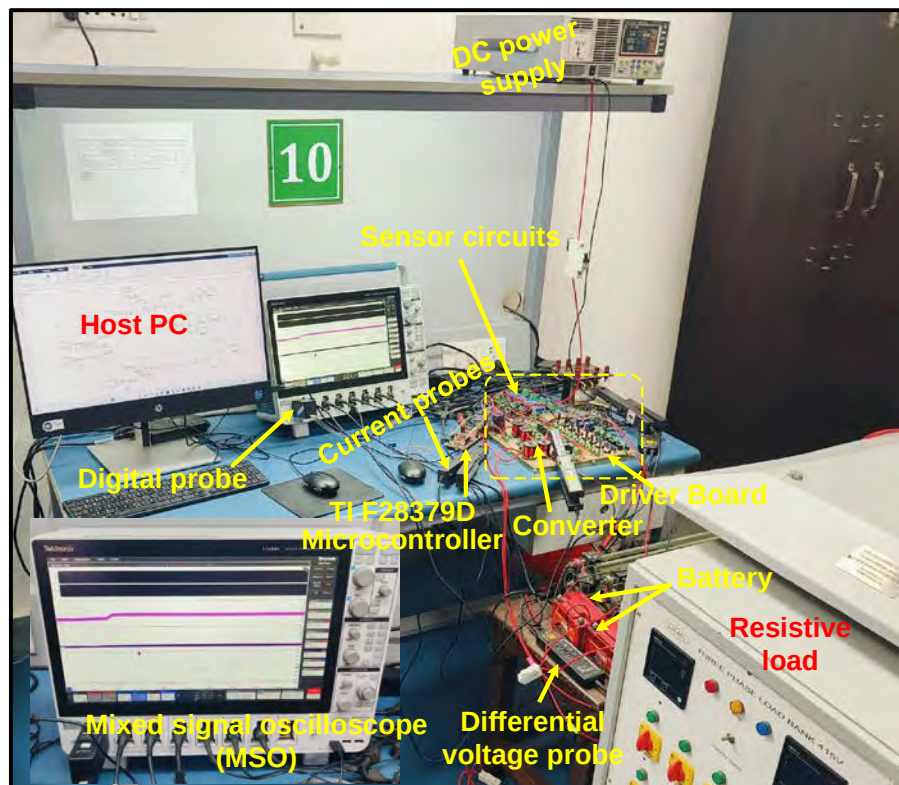


Figure 3.17 Experimental setup for TMDCM converter

Table 3.1
SYSTEM SPECIFICATIONS

Parameters		Values Used	
		Port 02: Resistive load	Port 02: Battery
Ref. Figure		Figure 3.18 & Figure 3.19	Figure 3.20 & Figure 3.21
V_{02}		$R_{02} = 15 \Omega / V_{02} = 15 \text{ V}$	24 V nominal
V_{01}		72 V – 96 V	
Inductor	L_1 / r_{L1}	1.0 mH / 0.1 Ω	
	L_2 / r_{L2}	560 μH / 0.3 Ω	
Capacitor	C_{in} / r_{Cin}	100 μF / 0.3 Ω	
	C_1 / r_{C1}	220 μF / 0.3 Ω	
	C_2 / r_{C1}	100 μF / 0.3 Ω	
Switching frequency		20 kHz	

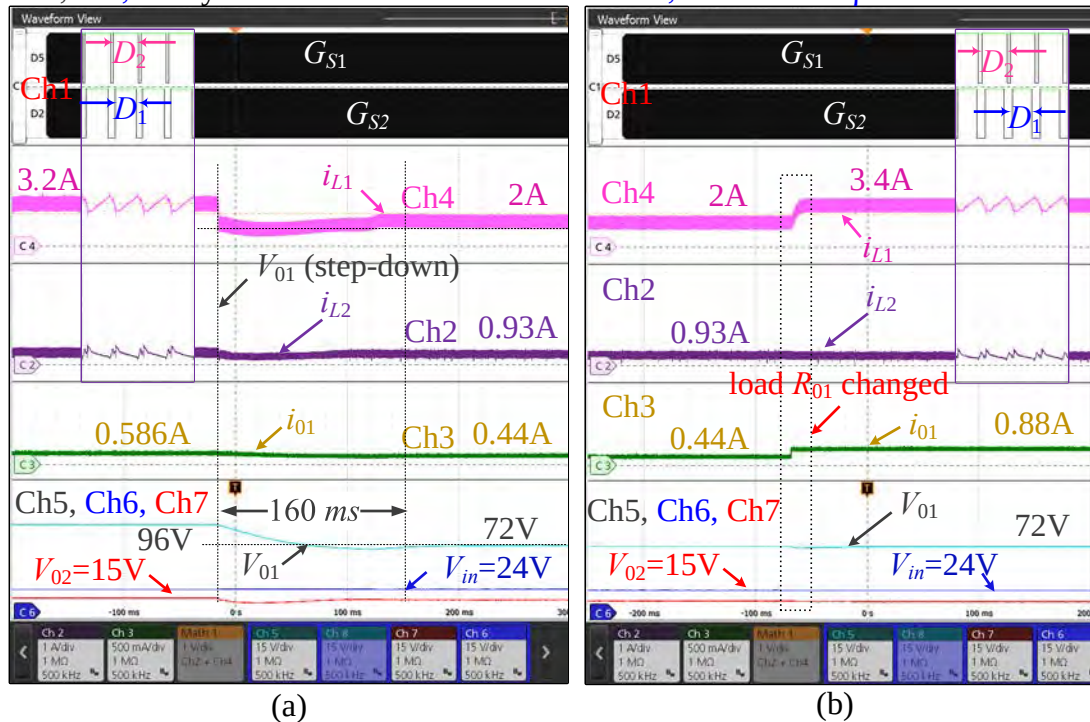
3.5.1 Experimental Analysis of Structure Controllability

It can be verified by varying the duty ratio and the input voltage of the system, in Figure 3.18(a), Figure 3.19, Figure 3.18(c), Figure 3.21(a), Figure 3.21(b) and Figure 3.18(d), respectively, voltage V_{01} is stepped down from 96V to 72V and stepped up from 72V to 96V, V_{02} is stepped up from 15V to 20V for *mode A* and for *mode B*, V_{01} is stepped up from 48V to 72V; and input voltage V_{in} is stepped down from 40V to 30V for *mode A*, respectively. These analysis shows that variations in V_{in} or the duty ratio directly led to corresponding changes in the state variables i_{L1} , i_{L2} , V_{01} , and V_{02} . This confirms that the system's structural controllability is maintained, with the output variables responding predictably to controlled changes in the input and switching parameters.

3.5.2 Experimental Analysis of State Controllability

It can be verified by changing the input and controlling the output voltage, V_{01} and V_{02} . In Figure 3.18(d), it can be seen that on changing the input voltage V_{in} from 40V to 30V, the output voltages V_{01} and V_{02} also change but restore back to 80V and 15V, respectively, as set. This shows that it is state-controllable.

Ch1: Digital out; Ch2: y-axis: 1A/div; Ch3: y-axis: 0.5A/div; Ch4: y-axis: 1A/div; Ch5, Ch6, Ch7: y-axis: 15V/div x-axis: 100ms/div, zoomed: 200μs/div



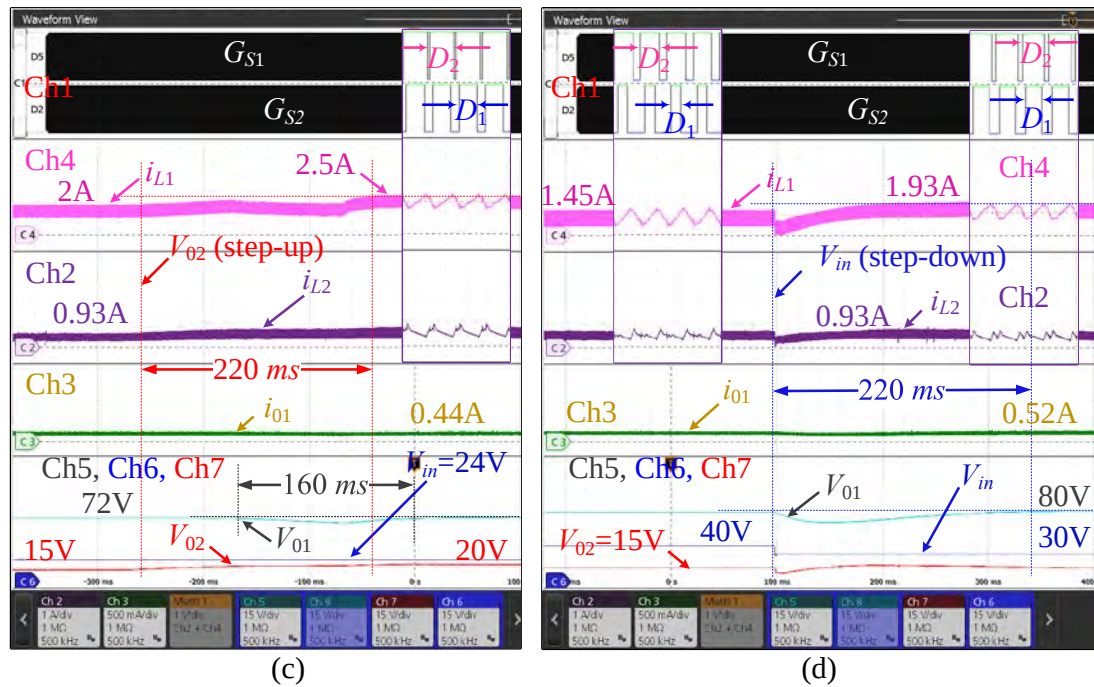


Figure 3.18 Experimental analysis of controllability and system dynamics for *mode A* with $K_p = 0.023$ and $K_i = 3.25$ for (a) step-down in V_{01} from 96V to 72V, (b) load R_{01} halved, (c) step-up in V_{02} from 15V to 20V and (d) step-down in V_{in} from 40V to 30V.

3.5.3 Experimental Analysis of Output Controllability

It can be verified by changing the load R_{01} . In Figure 3.18(b), Figure 3.21(c) and Figure 3.19(fourth sub-interval dynamics), the load R_{01} is halved, due to which a slight disturbance can be seen in V_{01} , but it restores to its reference value as set by the proper controlling technique. This shows that it is output controllable.

3.5.4 Experimental Analysis of System Dynamics for Mode A Operation

Figure 3.18 and Figure 3.19 show performance analysis of the system for two sets of K_p and K_i , and based on that, experimental verification is done for the selection of these parameters. In Figure 3.19(a) and Figure 3.18(a) V_{01} is stepped up and down from 72V to 96V and vice-versa, respectively. The average inductor and load current i_{L1} , i_{L2} , and i_{01} are 2A, 0.93A and 0.44, respectively. The input voltage V_{in} is considered as 24V. In Figure 3.18 and Figure 3.19(a), $K_p = 0.023$ and $K_i = 3.25$ have been selected. Figure 3.19(a) and Figure 3.18(a) show the stepped up and down of V_{01} , the settling time (t_s) is equal to ≈ 160 ms for i_{L1} and V_{01} , whereas for the same operating condition as shown in Figure 3.19(b), keeping K_p the same and $K_i = 0.28$, the t_s is ≈ 1.52 s, which shows that the second case is much slower than the first case. In Figures 3.18(c) and

(d), the dynamics of change in V_{02} and V_{in} are analyzed. V_{02} is stepped up from 15V to 20V, and V_{in} is stepped down from 40V to 30V, respectively. Due to the change in V_{02} , the t_s is $\approx 220\text{ ms}$ for i_{L1} , i_{L2} and V_{02} , while V_{01} settled down in $\approx 160\text{ ms}$. And due to a change in V_{in} , it takes $\approx 220\text{ ms}$ for all the state variables to settle down. So, based on experimental dynamical comparative analysis given in Figure 3.18 and Figure 3.19(a), the faster response, fewer oscillations and minimum maximum overshoot, $K_p=0.023$ and $K_i=3.25$ have been chosen, which is within the boundary condition for a robust system as in Figure 3.12(a).

Ch1: Digital out; Ch2: y-axis: 1A/div; Ch3: y-axis: 0.5A/div;
Ch4: y-axis: 1A/div; Ch5,Ch6,Ch7: y-axis: 15V/div

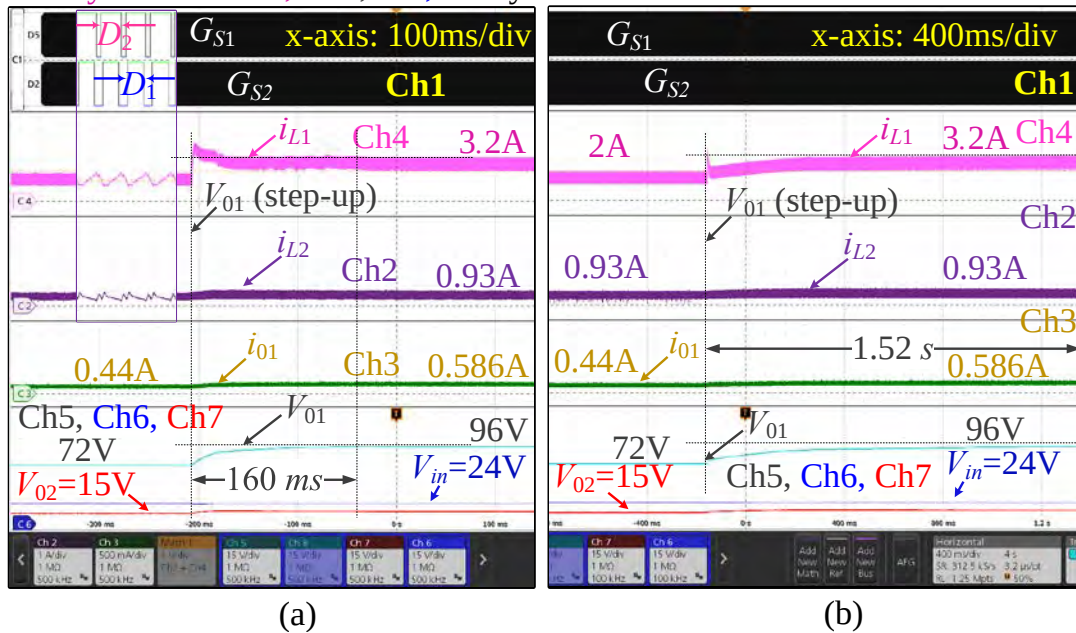


Figure 3.19 Experimental comparison of system dynamics for *mode A* operation for a step-up in V_{01} from 72V to 96V with (a) $K_p=0.023$ and $K_i=3.25$, (b) $K_p=0.023$ and $K_i=0.28$.

3.5.5 Experimental Analysis of System Dynamics for Mode Transition and Mode B Operation

Figure 3.20 illustrates the experimental dynamic performance of the proposed system across four operating intervals: turn-on, mode transition (*A* to *B*) and a step-down in V_{01} accompanied by a load change. During the turn-on dynamic, the reference input is set to $V_{in} = 40\text{V}$. The MVDC bus voltage V_{01} rises and settles at 72 V with a settling time of $t_s \approx 160\text{ ms}$. In this charging phase, the inductor current i_{L2} increases to

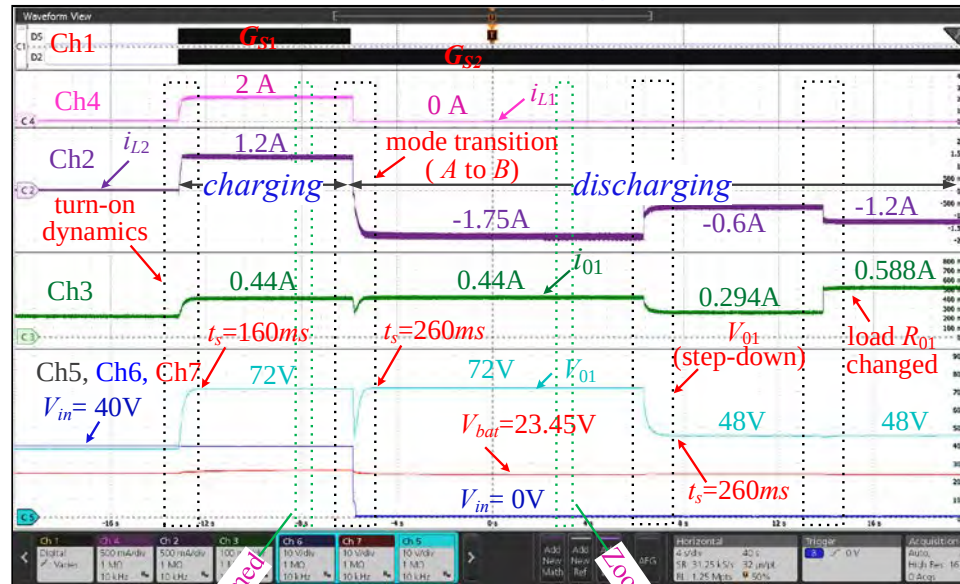
1.2 A, while i_{L1} has an average current of 2 A during conduction and drops to zero during transition. The load current i_{01} stabilizes at 0.44 A, confirming voltage regulation.

In the mode transition dynamic (A to B), the converter switches to discharging mode with a settling time of $t_s \approx 260ms$. In this instance, i_{L2} reverses polarity, initially reaching -1.75 A and thereafter stabilizing around -0.6 A throughout the ensuing step-down dynamic interval. This indicates that the battery is discharging in a regulated manner. The bus voltage V_{01} remains at 72 V, and the load current is consistently 0.44 A, indicating that the transition from charging to discharging is functioning effectively. In the step-down dynamic, the input source is removed (i.e., $V_{in} = 0V$), the battery voltage $V_{bat} = 23.45 V$, and the bus reference voltage decreases from 72 V to 48 V. The mechanism sustains consistent regulation at 48 V during the settling period. Simultaneously, halving the load resistance R_{01} increases i_{01} from 0.294 A to 0.588 A, prompting the battery to discharge in order to maintain the DC bus in *mode B*. These results confirm that the converter maintains robust operation with smooth transitions, accurate bus voltage regulation, and reliable dynamic response. The measured settling times of ~160 ms, 260 ms, and 340 ms for the turn-on, mode transition, and step-down dynamics, respectively, validate the proposed topology's effectiveness under practical transient conditions.

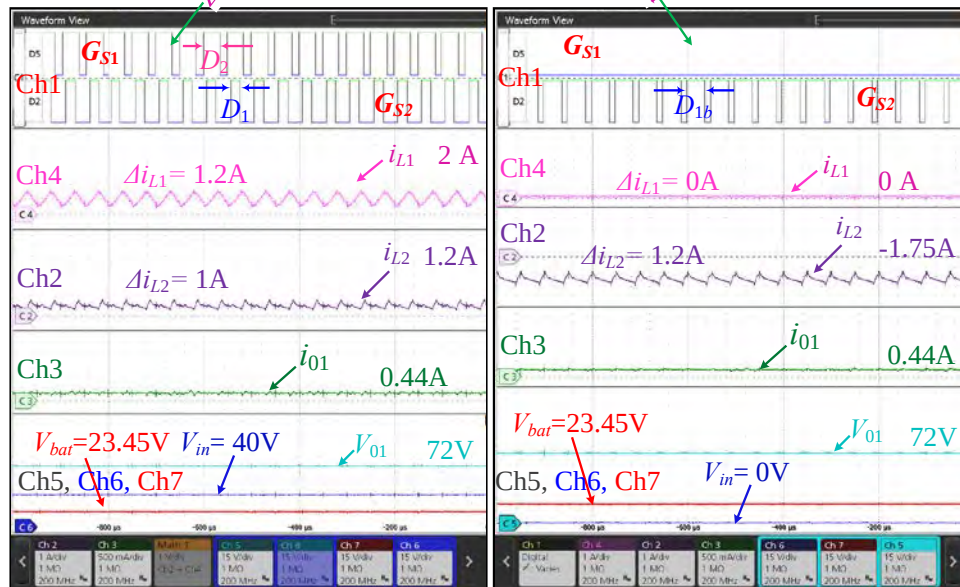
Figures 3.21(a) and (b) show the comparative analysis of the system for two sets of K_p and K_i , for *mode B* operation and based on that, experimental verification is done 0.44, respectively. The battery voltage V_{bat} is considered as 24V. In Figures 3.21(a), $K_p = 0.107$ and $K_i = 4.67$, have been selected. Figure 3.21(a) and Figure 3.20(third interval dynamic) for the selection of these parameters. In Figures 3.21(a) and (b) V_{01} is stepped up from 48V to 72V. The average inductor and load current i_{L1} , i_{L2} , and i_{01} are 0A, -1.35A and show the stepped up and down of V_{01} , the settling time (t_s) is equal to $\approx 260 ms$ for i_{L2} and V_{01} , whereas for the same operating condition as shown in Figure 3.21(b), keeping K_p the same and $K_i = 0.5$, the t_s is $\approx 3.6s$, which shows that the second case is much slower than the first case. So, based on experimental dynamical comparative analysis given in Figures 3.21(a) and (b), the faster response, fewer oscillations and minimum maximum overshoot, $K_p = 0.107$ and $K_i = 4.67$ have

been chosen, which is within the boundary condition for a robust system as in Figure 3.13(a).

- (a) Ch1: Digital out; Ch2: y-axis: 0.5A/div; Ch3: y-axis: 0.1A/div; Ch4: y-axis: 0.5A/div; Ch5,Ch6,Ch7: y-axis: 10V/div, x-axis: 4s/div
(b,c) Ch1: Digital out; Ch2: y-axis: 1A/div; Ch3: y-axis: 0.5A/div; Ch4: y-axis: 1A/div; Ch5,Ch6,Ch7: y-axis: 15V/div, x-axis: 200 μ s/div (Zoomed version)



(a)

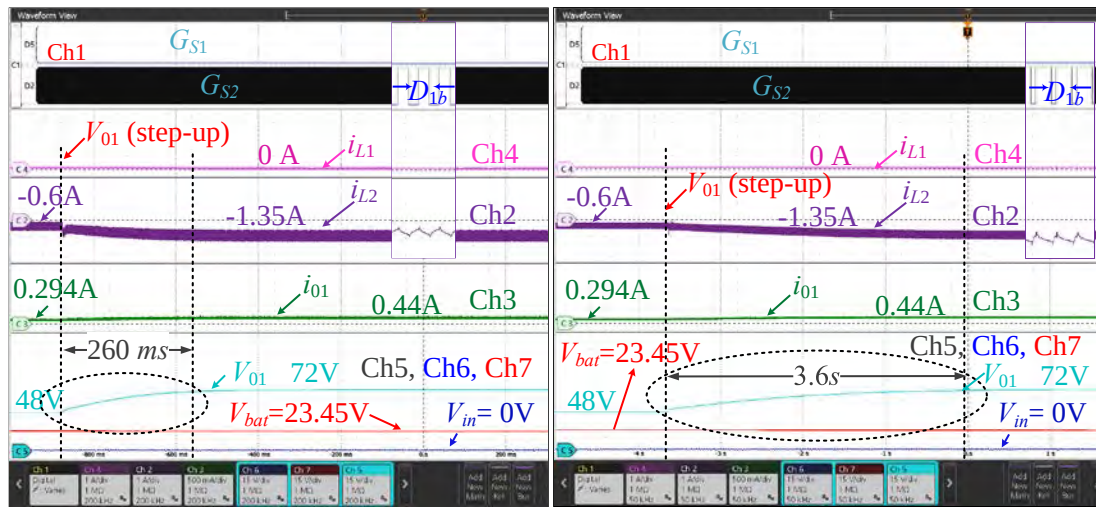


(b)

(c)

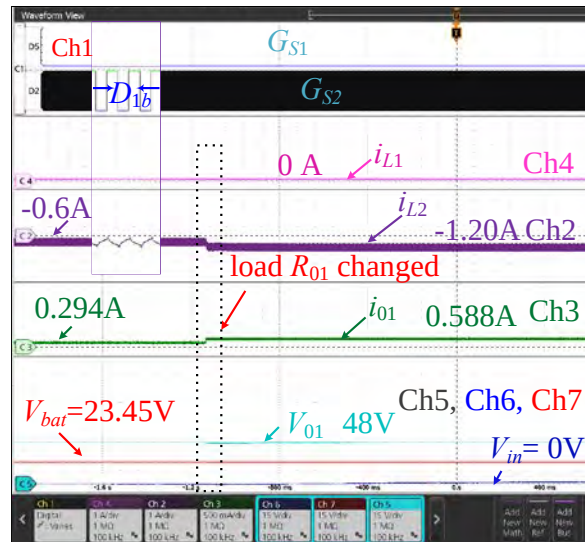
Figure 3.20 Experimental analysis of system, (a) turn-on dynamic, mode transition (A to B), step-down in V_{01} from 72V to 48V and load R_{01} halved during discharging (*mode B*), (b) zoomed version of the charging, and (c) zoomed version of the discharging during mode transition (A to B).

Ch1: Digital out; Ch2: y-axis: 1A/div; Ch3: y-axis: 0.5A/div; Ch4: y-axis: 1A/div; Ch5, Ch6, Ch7: y-axis: 15V/div, x-axis: (a, c = 200, 400 ms/div, b = 1s/div), zoomed: 200 μ s/div



(a)

(b)



(c)

Figure 3.21 Experimental analysis of comparison, controllability and system dynamics for *mode B* with (a) $K_p = 0.107$ and $K_i = 4.67$, (b) $K_p = 0.107$ and $K_i = 0.5$ for a step-up in V_{01} from 48V to 72V, and (c) load R_{01} halved.

3.5.6 Performance Analysis of the Controller

The dynamic comparison of the controller with optimized and arbitrary PI parameters within the robust region for both *mode A* and *mode B* operations is shown in Table 3.2. It shows that the proposed controller exhibits superior transient characteristics, including a lower percentage overshoot, faster rise time, and reduced settling time, when compared to the classical PI controller. It achieves a well-damped response with minimal overshoot and improved dynamic tracking in *mode A*, whereas

for *mode B*, it ensures faster stabilization and enhanced voltage regulation under sudden load perturbations.

Table 3.2
PERFORMANCE COMPARISON OF THE CONTROLLER WITH OPTIMIZED AND ARBITRARY
PI PARAMETERS WITHIN THE ROBUST REGION

Mode	Controller	Parameter	Peak Overshoot	Rise Time	Settling Time	Ref. Figure
<i>Mode A</i>	$K_p = 0.023, K_i = 3.25$ Robust PI controller	V_{01}	$\approx 2\text{-}3\%$	$\approx 0.14\text{s}$	$\approx 0.16\text{s}$	Figure 3.19(a)
		i_{L1}	$\approx 8\text{-}12\%$			
	$K_p = 0.023, K_i = 0.28$ PI controller	V_{01}	$\approx 1\text{-}2\%$	$\approx 1.32\text{s}$	$\approx 1.52\text{s}$	Figure 3.19(b)
		i_{L1}	$\approx 5\text{-}10\%$			
<i>Mode B</i>	$K_p = 0.107, K_i = 4.67$ <i>Robust PI controller</i>	V_{01}	$\approx 4\text{-}5\%$	$\approx 0.23\text{s}$	$\approx 0.26\text{s}$	Figure 3.21(a)
		i_{L1}	$\approx 10\text{-}12\%$			
	$K_p = 0.107, K_i = 0.5$ PI controller	V_{01}	$\approx 2\text{-}3\%$	$\approx 3.2\text{s}$	$\approx 3.6\text{s}$	Figure 3.21(b)

3.5.7 Comparative Analysis of the System

A detailed comparative analysis of the proposed time-multiplexed robust PI controller with the recent research outcomes has been incorporated in Table 3.3.

Table 3.3
COMPARISON OF THE PROPOSED CONTROLLER WITH RESPECT TO DIFFERENT PARAMETERS AND
METHODOLOGIES

Comparison Parameters	[60]	[61]	[101]	[99]	[104]	Proposed
Methodology (controller)	Integral sliding mode	Continuous nonsingular terminal sliding mode	Hybrid model predictive control	Classical PI	Robust PI	Time-multiplexed Robust PI
Non-isolated Topology used in the cited reference	DC-DC boost converter	DC-DC boost converter	DC-DC boost converter	DC-DC interleaved converter	High-gain boost DC-DC converter	DC-DC multiport converter
	No.	0	0	1	0	1
	Bidirectional	1	1	2	1	2
No. of Ports	Unidirectional	1	1	3	1	3
	Total	1	1	3	1	3
Mitigates uncertainties	Yes	No	No	No	Yes	Yes
Control complexity	Medium	High	High	Low	Medium	Medium
No. of Isolated Drivers	1	1	1	2	1	2
Current feedback	Phase current	Phase current	Phase current	Phase current (during charging)	NA	Phase current (during charging)
Voltage feedback	Output voltage	Output voltage	Output voltage	Output voltage	Output voltage	Output voltage
Robust	No	Yes	No	No	Yes	Yes

3.6 Conclusions

This chapter presents the controllability and dynamic behavior of the TMDCM converter, with a thorough inclusion of all pertinent parasitic elements and structured uncertainty. Structural controllability is methodically examined through a graph-theoretical approach, confirming that the converter topology meets the criteria for

complete state structure and output controllability within the specified operational conditions. Additionally, a robust single-loop voltage-mode PI controller presented in this work exhibited satisfactory closed-loop performance under structured uncertainties for a time-multiplexed switched-boost converter exhibiting a right-half-plane (RHP) zero. The robust control strategy is formulated using the stability boundary locus technique, augmented by Kharitonov's theorem, an intriguing application in the context of systems affected by parametric uncertainties. It also ensuring CCCV battery charging and stable DC bus voltage regulation. Thereby, enhancing system resilience and regulated power flow at both the output ports.

Chapter 4

TRI-PORT SOFT-SWITCHED MODULAR DC-DC CONVERTER WITH REDUCED CURRENT RIPPLE FOR ESS

4.1 General

Under equal current-sharing conditions, interleaved boost converters distribute current among phases, reducing current stress and enabling medium- to high-power operation [110]. However, the switch peak inverse voltage remains comparable to that of the conventional boost converter, leading to similar switching losses. The zero-voltage switching (ZVS) and zero-current switching (ZCS)-based soft-switched interleaved boost converters combine the benefits of ZVS and ZCS techniques with interleaving to attain higher power levels with improved efficiency [96], [111]. The soft-switched interleaved converter topologies are used for applications such as data centers, renewable energy systems (RESs) [97], [112] and electric vehicles (EVs) [113].

The transition from single-input single-output (SISO) DC-DC converters to multiport DC-DC converters (MPDC), emphasizing the benefits of reduced component count and improved power density [114]. The MPDCs are designed to integrate into RES with various energy sources [23], [64], [115]. These converters play a critical role in mitigating the inherent intermittency of RESs while ensuring reliable and efficient power delivery. In [92], a soft-switched non-isolated multiport converter is proposed for distributed photovoltaic (PV) systems with integrated energy storage. The topology enables the interfacing of multiple PV strings and an energy storage unit within a unified architecture, employing maximum power point tracking (MPPT) and differential power processing (DPP) to enhance energy utilization. Soft-switching is achieved across all semiconductor devices, resulting in reduced switching losses and improved conversion efficiency. An interleaved two-switch forward dc-dc converter with both ZVS and ZCS capability is presented in [94]. The design employs a coupled inductor and a passive auxiliary resonant network to reduce switching stress and improve the dynamic response and efficiency of the main power switches. Furthermore, in [116], an interleaved bidirectional DC-DC converter incorporating a shared auxiliary soft-switching network is proposed for voltage balancing and

controlled power flow in energy storage applications, such as hybrid electric vehicles and renewable energy systems. The converter achieves ZVS for the main power switches and ZCS for the auxiliary switches and diodes.

In [100], a soft-switched MPDC architecture is introduced to enable unidirectional power transfer among multiple ports for power sharing with a reduced component count. Modular DC-DC converters are indispensable for medium voltage DC (MVDC) systems; however, each class of solutions addresses only a subset of the required performance attributes. Input-independent, series-output-based MPDCs have demonstrated effectiveness for single-stage MVDC integration with reduced system complexity. Nevertheless, their practical deployment is constrained by submodule voltage imbalance and the absence of inherent fault-tolerant capability, particularly under power mismatch and port-level fault conditions [90], [91].

Fault-tolerant cascaded DC-DC converters reported in the literature emphasize short-circuit tolerance and continued operation of healthy submodules, particularly in PV applications [33]. Nevertheless, these topologies typically rely on hard-switched operation, resulting in increased switching losses, higher device stress, and reduced efficiency at high switching frequencies. Similarly, modular multilevel DC-DC converters and their multiport or bipolar extensions reported in [38] and [117] offer high scalability and redundancy; however, they suffer from structural complexity, dependence on centralized magnetic components, narrow soft-switching regions, and limited suitability for compact multiport implementations. As a result, existing modular multilevel DC-DC based solutions do not simultaneously satisfy the requirements of multiport operation, fault tolerance, bidirectional power flow, and wide-range soft switching.

The soft-switching techniques have been demonstrated in [95] for high-gain full-bridge DC-DC converters for MVDC systems, significantly reducing switching losses and improving efficiency. However, these converters are predominantly two-port architectures and are not readily extendable to modular multiport configurations with inherent fault tolerance. Likewise, bidirectional multiport converters developed for lower-voltage applications prioritize power-flow flexibility but lack MVDC scalability and comprehensive protection mechanisms [118].

This chapter introduces a non-isolated, soft-switched tri-port fault-tolerant modular DC–DC (TPFTMDC) converter that employs time-multiplexing control of semiconductor switching devices to enable multiple output ports with a reduced device count, bidirectional power-flow capability, and enhanced fault-tolerant operation.

4.2 Proposed Modular Multiport Converter

The circuit topology of the proposed TPFTMDC converter is presented in Figure 4.1, depicting a n -phase modular interleaved multiport soft-switched converter with two output ports that provide both step-up (i.e., output port 01) and step-down (i.e., output port 02) voltage gain capability. The operation of the proposed converter is discussed for two states: *state I*, where power flows from the source to both output ports; and *state II*, where the source is absent, and power flows from output port 02 to output port 01. A non-isolated tri-port converter with soft-switching capability at the higher-voltage port regulates the MVDC bus voltage and controls battery charging and discharging to satisfy load power requirements. It exhibits bidirectional operation, wherein the battery is charged in buck mode during input supply while maintaining MVDC voltage regulation; conversely, in the absence of the input source, the battery discharges in boost mode to sustain the load demand and preserve the output voltage.

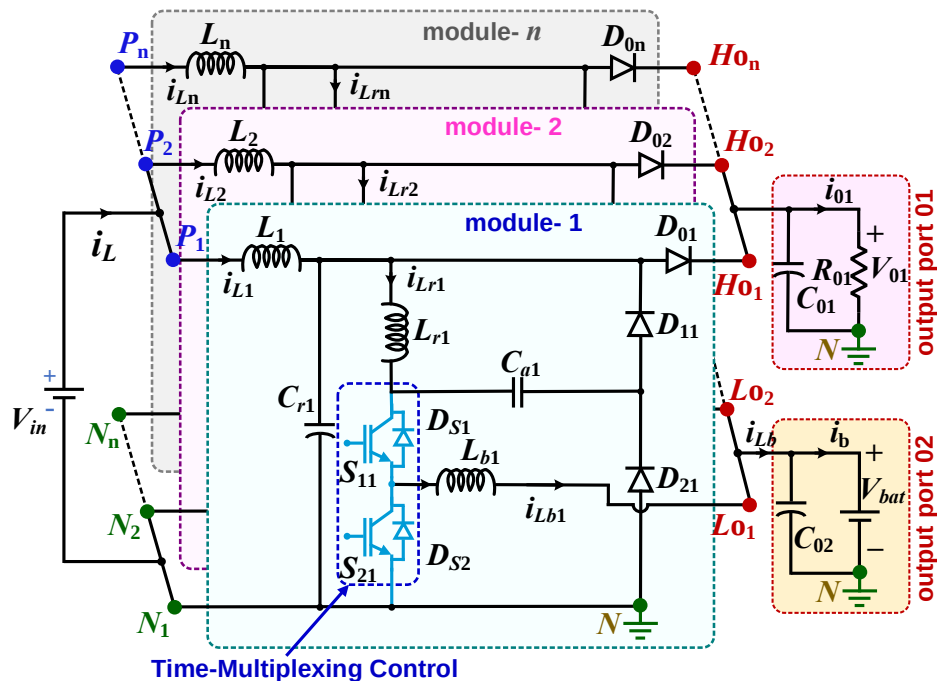


Figure 4.1 Circuit topology of the proposed TPFTMDC converter.

4.3 Operating Principle of the Converter

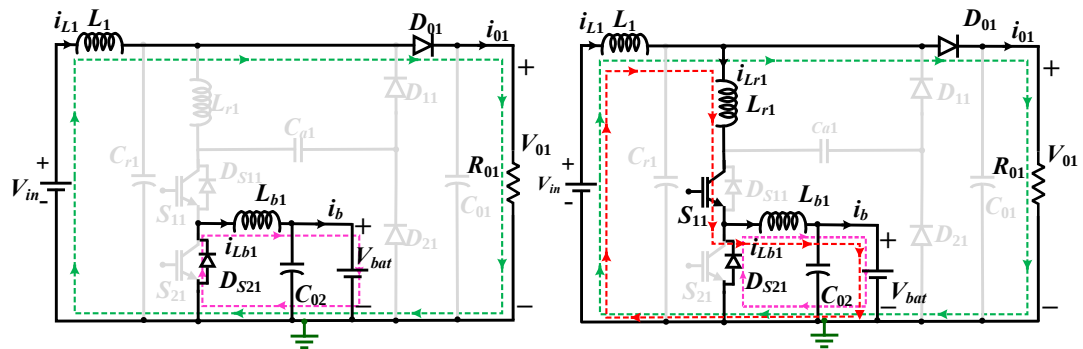
4.3.1 State I Operation

The main features of the proposed converter are its soft-switching capability at the higher-voltage output port and its modularity, which can be extended to an n -stack configuration for higher power ratings. *The proposed circuit is explained for a two-phase TPFTMDC converter.* The main circuit consists of inductors L_1 , L_2 , L_{b1} , and L_{b2} , along with capacitors C_{01} and C_{02} , and diodes D_{01} and D_{02} . The auxiliary circuit that facilitates ZVS and ZCS comprises inductors L_{r1} and L_{r2} , bipolar auxiliary capacitors C_{a1} and C_{a2} , electrolytic resonant capacitors C_{r1} and C_{r2} , and diodes D_{11} , D_{21} , D_{12} , and D_{22} . Switches S_{11} and S_{21} exhibit a phase shift of 180° in relation to S_{12} and S_{22} , respectively. The converter features two voltage level ports: V_{01} (i.e., output port 01 with step-up) and V_{bat} (i.e., output port 02 with step-down for battery charging/discharging).

The switching logics of S_{11} and S_{21} are achieved through a time-multiplexing control technique that employs a switched boost action method. Analysis of modes is conducted on the single-module circuit, specifically module-1, utilizing phase-shifting to achieve a modular circuit that replicates comparable results. The main inductor currents are i_{L1} and i_{Lb1} , whereas the resonant current is i_{Lr1} , accompanied by the respective resonant voltages V_{Ca1} and V_{Cr1} . Switch currents and voltages are represented as i_{S11} , i_{S21} , and V_{S11} , V_{S21} , respectively, accompanied by gating pulses G_{S11} and G_{S21} . The steady-state switching key waveforms under *state I (S-I)*, with respect to the duty ratios D_1 and D_2 for a single stack, are classified into 11 operating modes, as shown in Figure 4.2. The circuit configuration for *state I* operation based on these switching modes is shown in Figure 4.3.

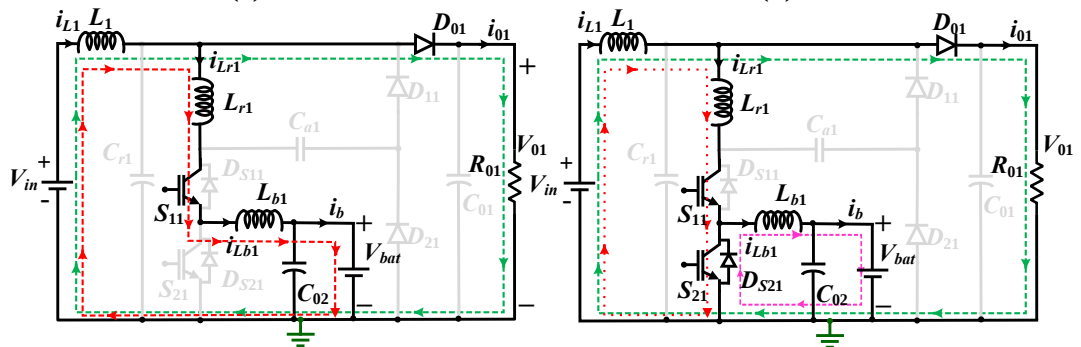


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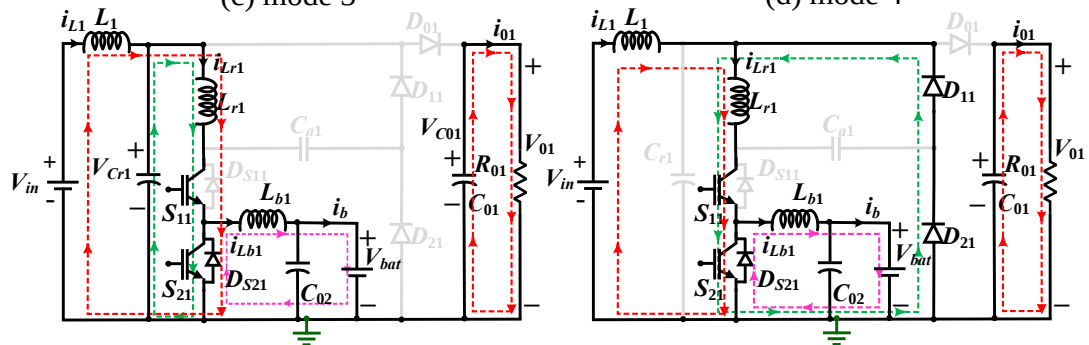
(a) mode 1

(b) mode 2



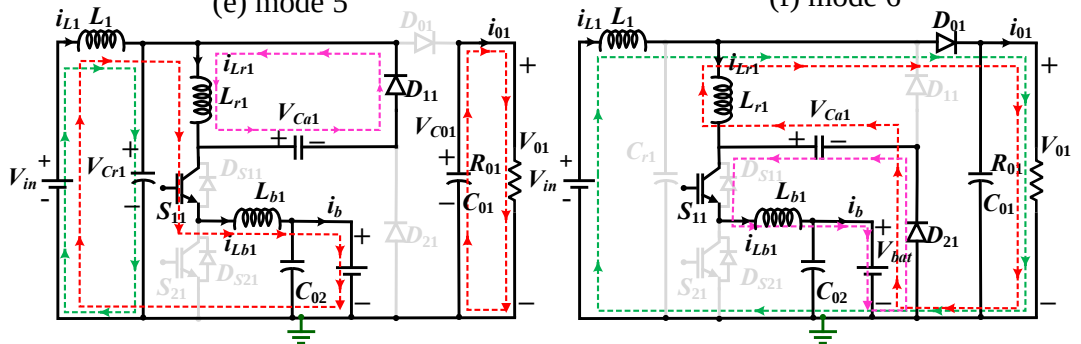
(c) mode 3

(d) mode 4



(e) mode 5

(f) mode 6



(g) mode 7

(h) mode 8

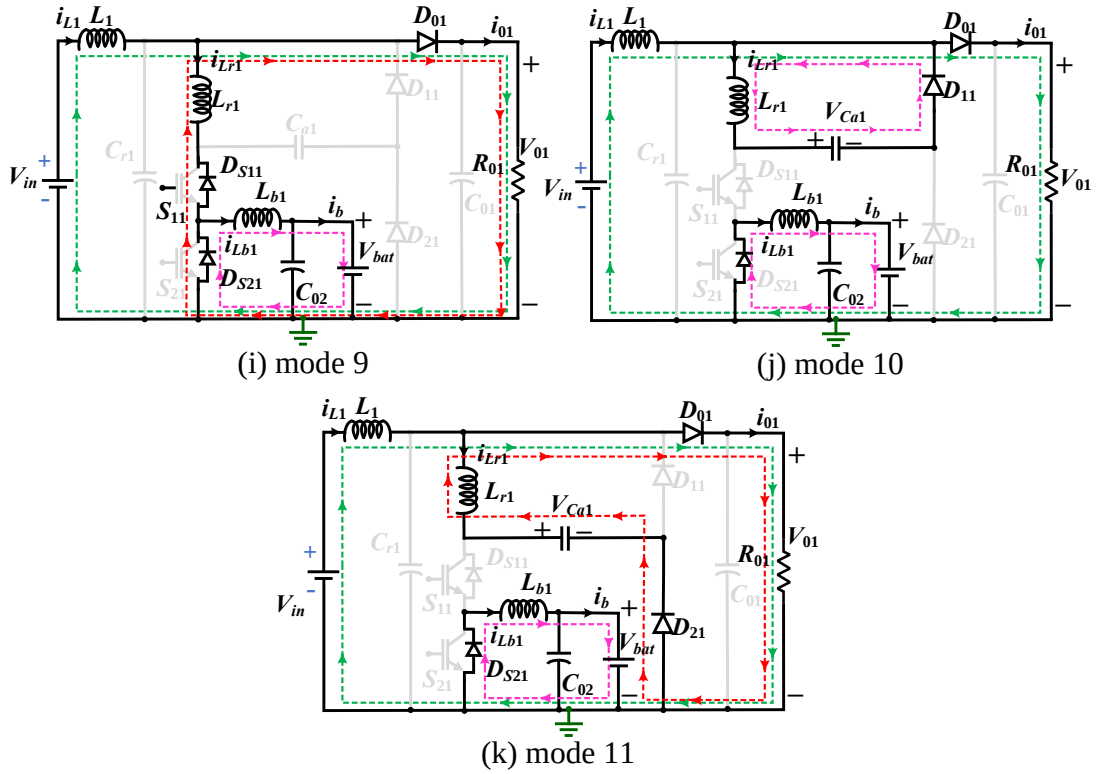


Figure 4.3 Circuit operation of module-1 of the proposed TPFTMDC converter during the charging state (i.e., *state-I*) under (a) mode-1, (b) mode-2, (c) mode-3, (d) mode-4, (e) mode-5, (f) mode-6, (g) mode-7, (h) mode-8, (i) mode-9, (j) mode-10, and (k) mode-11.

4.3.1.1 Time-Domain Analysis of the Converter

Mode 1 ($t_0 \leq t < t_1$), Figure 4.3(a): During this period, it is assumed that inductors L_1 and L_{b1} are initially charged and resulting the voltages are $-(V_{01}-V_{in})$ and $-V_{bat}$, respectively, and the inductor current decreases linearly under steady-state conditions. The detailed analysis for both the *states* and *modes* are presented in the Appendix (A.2.1) and (A.2.2), respectively.

$$i_{L1}^{S-I}(t) = i_{L1}^{S-I}(t_0) - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_1) = I_1^{S-I}, \quad (4.1a)$$

$$i_{Lb1}^{S-I}(t) = i_{Lb1}^{S-I}(t_0) - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_1) = I_{b1}^{S-I}, \quad (4.1b)$$

$$i_{Lr1}^{S-I}(t) = 0, \quad v_{Cr1}^{S-I}(t) = V_{01}, \quad v_{Ca1}^{S-I}(t) = 0. \quad (4.1c)$$

Mode 2 ($t_1 \leq t < t_2$), Figure 4.3(b): During this interval, turn-on of S_{11} clamps the corresponding node to ground potential. This abrupt change in the node voltage forces the inductor L_{b1} to release its stored energy, initiating discharge. As a result, the current in L_{b1} decreases during this interval, ensuring that it remains compatible with the resonant inductor L_{r1} before the converter transitions to the subsequent operating mode.

$$i_{L1}^{S-I}(t) = I_1^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_2) = I_2^{S-I}, \quad (4.2a)$$

$$i_{Lb1}^{S-I}(t) = I_{b1}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_2) = I_{b2}^{S-I}, \quad (4.2b)$$

$$i_{Lr1}^{S-I}(t) = \frac{V_{01}}{L_{r1}} \times t, \quad v_{Cr1}^{S-I}(t) = V_{01}, \quad v_{Ca1}^{S-I}(t) = 0. \quad (4.2c)$$

Mode 3 ($t_2 \leq t < t_3$), Figure 4.3(c): During this interval, the switching characteristics and current path of inductor L_1 exhibit similar operation with respect to the previous mode with the inductor currents i_{Lr1} and i_{Lb1} being equal. Consequently, the principles of circuit theory remain intact when two current sources are connected in series and L_{b1} charges to its maximum value i_{Lb1max} .

$$i_{L1}^{S-I}(t) = I_2^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_3) = I_3^{S-I}, \quad (4.3a)$$

$$i_{Lb1}^{S-I}(t) = I_{b2}^{S-I} + \left(\frac{V_{01} - V_{bat}}{L_{r1} + L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_3) = I_{Lb1max}^{S-I}, \quad (4.3b)$$

$$i_{Lr1}^{S-I}(t) = i_{Lb1}^{S-I}(t), \quad v_{Cr1}^{S-I}(t) = V_{01}, \quad v_{Ca1}^{S-I}(t) = 0. \quad (4.3c)$$

Mode 4 ($t_3 \leq t < t_4$), Figure 4.3(d): During this interval, both switches S_{11} and S_{21} are switched-on and inclusion of inductor L_{r1} facilitates S_{21} in attaining ZCS. The voltage across inductor L_{r1} is equivalent to the output voltage V_{01} . Consequently, the inductor L_1 discharges linearly to i_{L1min} , while the inductor L_{b1} discharges to the battery.

$$i_{L1}^{S-I}(t) = I_3^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_4) = I_{L1min}^{S-I}, \quad (4.4a)$$

$$i_{Lb1}^{S-I}(t) = I_{Lb1max}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_4) = I_{b3}^{S-I}, \quad (4.4b)$$

$$i_{Lr1}^{S-I}(t) = I_{Lb1\max}^{S-I} + \frac{V_{01}}{L_{r1}} \times t, \quad i_{Lr1}^{S-I}(t_4) \approx I_{L1\min}^{S-I} + I_{Lb1\max}^{S-I} = I_{Lr}^{S-I}. \quad (4.4c)$$

Mode 5 ($t_4 \leq t < t_5$), Figure 4.3(e): During this interval, the switching characteristics are similar to those of the previous mode, except that D_{01} is reverse-biased. Hence, the resonant capacitor C_{r1} resonates through L_{r1} and i_{L1} is assumed constant. Consequently, the output capacitors C_{01} discharge through the load R_{01} .

$$i_{L1}^{S-I}(t) \approx I_{L1}^{S-I}(t_4) \approx I_{L1}^{S-I}(t_5) \approx I_{L1\min}^{S-I}, \quad (4.5a)$$

$$i_{Lb1}^{S-I}(t) = I_{b3}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_5) = I_{b4}^{S-I}, \quad (4.5b)$$

$$i_{Lr1}^{S-I}(t) = I_{Lr}^{S-I} + \frac{V_{01}}{Z_{r1}} \times \sin(\omega_{r1}t), \quad \omega_{r1} = 1/\sqrt{L_{r1}C_{r1}}, \quad (4.5c)$$

$$Z_{r1} = \sqrt{L_{r1}/C_{r1}}, \quad v_{Cr1}^{S-I}(t) = V_{01} \cos(\omega_{r1}t), \quad v_{Ca1}^{S-I}(t) = 0. \quad (4.5d)$$

Mode 6 ($t_5 \leq t < t_6$), Figure 4.3(f): During this interval, the auxiliary diodes D_{11} and D_{21} become active when the voltage across the resonant capacitor V_{cr1} discharges to zero in the previous mode. The resonant inductor current i_{Lr1} divides into two distinct components: one flows through diodes D_{11} and D_{21} , while the other contributes to the main inductor current i_{L1} . In this phase, inductor L_{b1} reaches its minimum discharge level $i_{Lb1\min}$.

$$i_{L1}^{S-I}(t) = I_{L1\min}^{S-I} + \left(\frac{V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_6) = I_{L1\max}^{S-I}, \quad (4.6a)$$

$$i_{Lb1}^{S-I}(t) = I_{b4}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_6) = I_{Lb1\min}^{S-I}, \quad (4.6b)$$

$$i_{Lr1}^{S-I}(t) = I_{Lr}^{S-I} + \frac{V_{01}}{Z_{r1}} = I_{rp}^{S-I}, \quad (4.6c)$$

$$v_{Cr1}^{S-I}(t) = 0, \quad v_{Ca1}^{S-I}(t) = 0. \quad (4.6d)$$

Mode 7 ($t_6 \leq t < t_7$), Figure 4.3(g): During this interval, the switch S_{21} is off under ZVS, while switch S_{11} remains active. This mode consists of three current loops: the first loop is V_{in} - L_1 - L_{r1} - L_{b1} - V_{bat} , the second loop is L_1 - C_{r1} - V_{in} ; and the third loop is L_{r1} - C_{a1} - D_{11} , which leads to the occurrence of the second resonance. The V_{cr1} is energized to its peak output voltage V_{01} . The analytical expressions are derived using

the inverse Laplace transform based on the convolution theorem. In the convolution integral, t denotes the time at which the response is evaluated, whereas τ is the integration variable representing a previous time instant at which the input was applied to the system.

$$i_{L1}^{S-I}(t) \approx i_{L1}^{S-I}(t_6) \approx i_{L1}^{S-I}(t_7) \approx I_{L1\max}^{S-I}, \quad (4.7a)$$

$$i_{Lb1}^{S-I}(t) = I_{Lb1\min}^{S-I} - \frac{1}{L_{b1}} \left(V_{bat} \times t - L_{r1} I_{rp}^{S-I} - \int_0^t v_{Cr1}^{S-I}(\tau) d\tau + L_{r1} i_{Lr1}^{S-I}(t) \right), \quad (4.7b)$$

$$\omega_{a1} = 1/\sqrt{L_{r1}C_{a1}}, \quad Z_{a1} = \sqrt{L_{r1}/C_{a1}}, \quad i_{Lb1}^{S-I}(t_7) = I_{b5}^{S-I}, \quad (4.7c)$$

$$i_{Lr1}^{S-I}(t) = I_{rp}^{S-I} \cos(\omega_{a1}t) + \omega_{a1} \int_0^t i_{Lb1}^{S-I}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau, \quad (4.7d)$$

$$v_{Cr1}^{S-I}(t) = \frac{1}{C_{r1}} \left(i_{L1\max}^{S-I} \times t - \int_0^t i_{Lb1}^{S-I}(\tau) d\tau \right), \quad (4.7e)$$

$$v_{Ca1}^{S-I}(t) = I_{rp}^{S-I} Z_{a1} \sin(\omega_{a1}t) - \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-I}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau. \quad (4.7f)$$

Mode 8 ($t_7 \leq t < t_8$), Figure 4.3(h): During this interval, the auxiliary capacitor C_{a1} is discharged through L_{r1} and L_{b1} . The energy is transferred from C_{a1} to L_{r1} and L_{b1} until the capacitor C_{a1} fully discharges to zero.

$$i_{L1}^{S-I}(t) = I_{L1\max}^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_8) = I_4^{S-I}, \quad (4.8a)$$

$$i_{Lb1}^{S-I}(t) = I_{b5}^{S-I} + \frac{1}{L_{b1}} \left((V_{01} - V_{bat}) \times t - L_{r1} i_{Lr1}^{S-I}(t) \right), \quad (4.8b)$$

$$i_{Lr1}^{S-I}(t) = \frac{\left(V_{ca1}^{S-I} \Big|_{t_7} - V_{01} \right) \sin(\omega_{a1}t)}{Z_{a1}} - \omega_{a1} \int_0^t i_{Lb1}^{S-I}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau, \quad (4.8c)$$

$$v_{Ca1}^{S-I} \Big|_{t_7} = I_{rp}^{S-I} Z_{a1} - \frac{1}{C_{a1}} \int_0^{\pi/2\omega_{a1}} i_{Lb1}^{S-I}(\tau) \sin(\omega_{a1}\tau) d\tau, \quad (4.8d)$$

$$v_{Ca1}^{S-I}(t) = V_{01} - \left(V_{01} - v_{Ca1}^{S-I} \Big|_{t_7} \right) \cos(\omega_{a1}t) - \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-I}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau = V_{c1}^{S-I}, \quad (4.8e)$$

$$v_{Cr1}^{S-I}(t) = V_{01}, \quad i_{Lb1}^{S-I}(t_8) = I_{b6}^{S-I}, \quad i_{Lr1}^{S-I}(t_8) = I_{r1}^{S-I}. \quad (4.8f)$$

Mode 9 ($t_8 \leq t < t_9$), Figure 4.3(i): During this interval, the reverse current of i_{Lr1} activates the antiparallel diode of switches S_{11} and S_{21} and discharges through the current loop L_{r1} - D_{01} - R_{01} - D_{S11} - D_{S21} until it reaches zero. Then, it enters *mode 2* for ($t_9 \leq t < t_{10}$) and *mode 3* for ($t_{10} \leq t < t_{11}$) before transitioning to the mode 10.

$$i_{L1}^{S-I}(t) = I_4^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_9) = I_5^{S-I}, \quad (4.9a)$$

$$i_{Lb1}^{S-I}(t) = I_{b6}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_9) = I_{b7}^{S-I}, \quad (4.9b)$$

$$i_{Lr1}^{S-I}(t) = I_{r1}^{S-I} - \frac{V_{01}}{L_{r1}} t, \quad v_{Cr1}^{S-I}(t) = V_{01}, \quad v_{Ca1}^{S-I}(t) = 0. \quad (4.9c)$$

Mode 10 ($t_{11} \leq t < t_{12}$), Figure 4.3(j): During this interval, the switches S_{11} and S_{21} are turned off. The L_{r1} resonates in the loop L_{r1} - C_{a1} - D_{11} , transferring maximum energy to C_{a1} , while L_{b1} discharges to the battery.

$$i_{L1}^{S-I}(t) = I_3^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_{12}) = I_6^{S-I}, \quad (4.10a)$$

$$i_{Lb1}^{S-I}(t) = I_{Lb1\max}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_{12}) = I_{b8}^{S-I}, \quad (4.10b)$$

$$i_{Lr1}^{S-I}(t) = i_{Lb1\max}^{S-I} \cos(\omega_{a1}t), \quad v_{Cr1}^{S-I}(t) = V_{01}, \quad (4.10c)$$

$$v_{Ca1}^{S-I}(t) = i_{Lb1\max}^{S-I} Z_{a1} \sin(\omega_{a1}t). \quad (4.10d)$$

Mode 11 ($t_{12} \leq t < t_{13}$), Figure 4.3(k): During this interval, the auxiliary capacitor C_{a1} resonates within the D_{21} - C_{a1} - L_{r1} - D_{01} loop and the energy is transferred from C_{a1} to L_{r1} until the capacitor C_{a1} fully discharges to zero and enters in *mode 9* ($t_{13} \leq t < t_{14}$).

$$i_{L1}^{S-I}(t) = I_6^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad (4.11a)$$

$$i_{Lb1}^{S-I}(t) = I_{b8}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad (4.11b)$$

$$i_{Lr1}^{S-I}(t) = \left(i_{Lb1\max}^{S-I} - \frac{V_{01}}{Z_{a1}} \right) \sin(\omega_{a1}t), \quad (4.11c)$$

$$v_{Ca1}^{S-I}(t) = V_{01} - \left(V_{01} - i_{Lb1\max}^{S-I} Z_{a1} \right) \cos(\omega_{a1}t), \quad v_{Cr1}^{S-I}(t) = V_{01}. \quad (4.11d)$$

4.3.2 State II Operation

The input supply is absent, so the switches S_{11} and S_{12} are kept permanently off, resulting in the battery operates under boost mode to maintain the dc-bus voltage and providing power to the loads connected at MVDC. This case falls under *SISO*, with the battery functioning as a source. In *state II* (*S-II*), a total of six modes can be observed, as illustrated in the steady-state waveforms depicted in Figure 4.4. Figure 4.5 illustrates all six modes along with their operational principles.

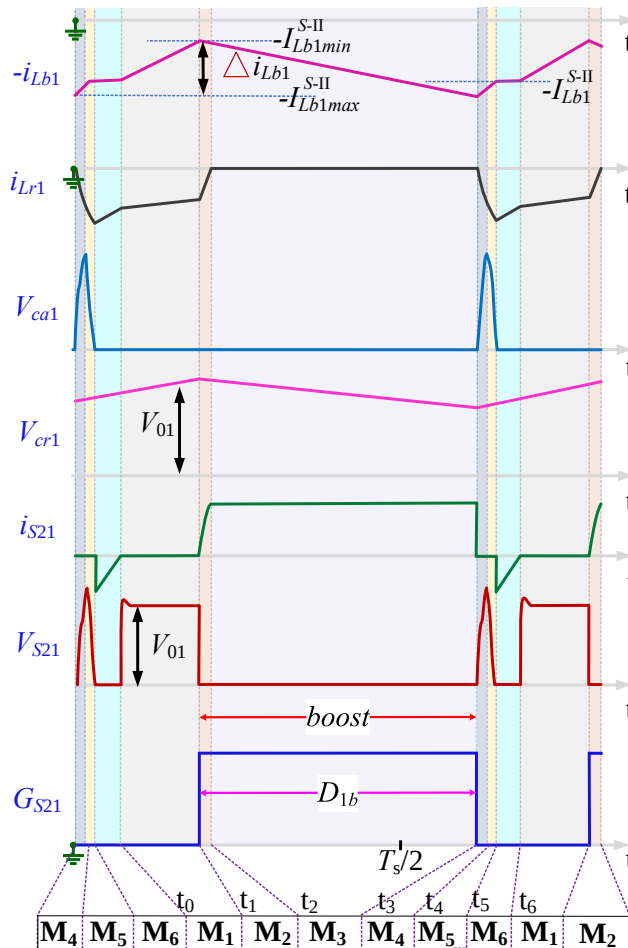


Figure 4.4 The steady-state switching key waveform of module-1 of the proposed TPFTMDC converter during the discharging state (i.e., *state-II*).

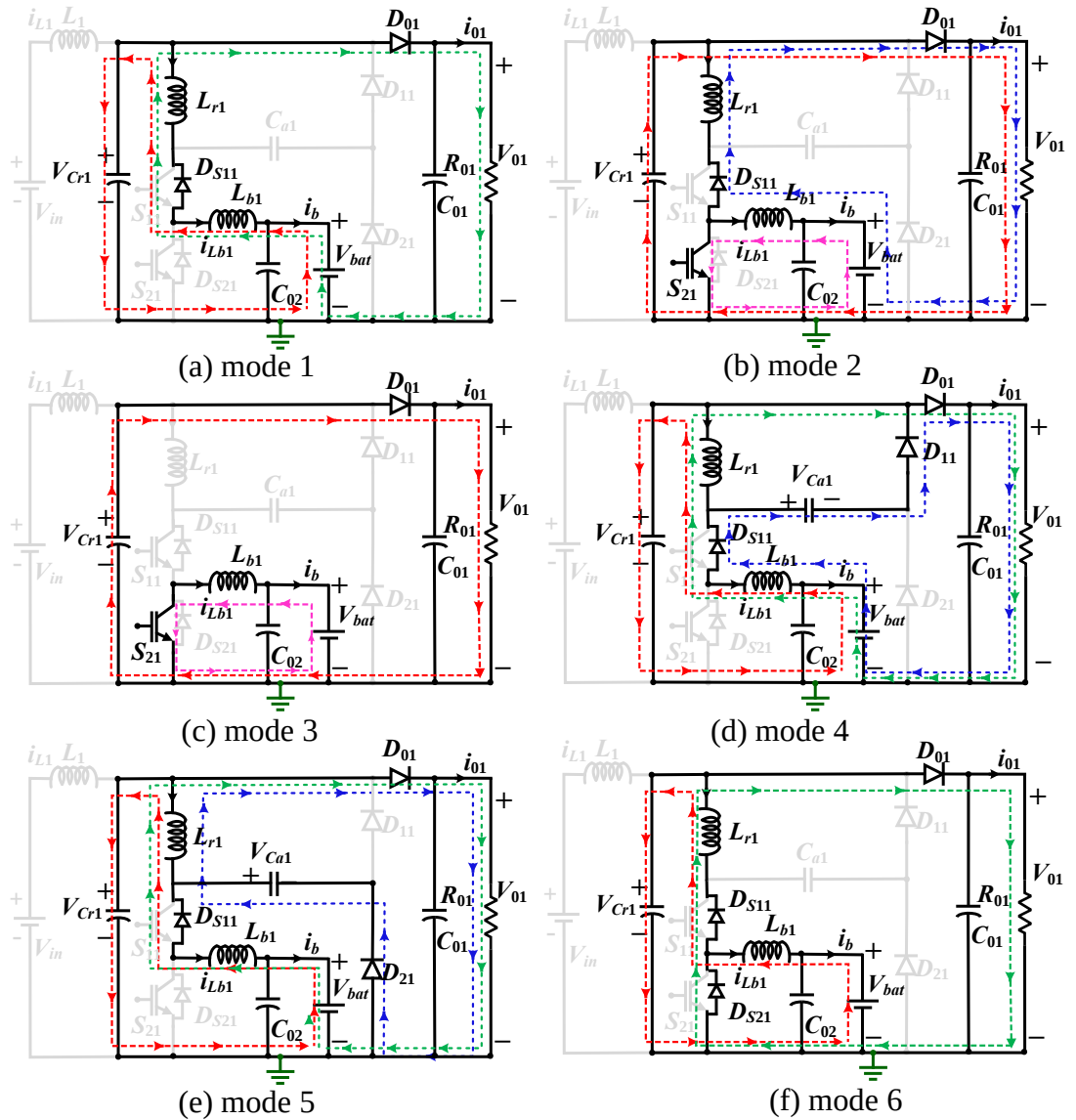


Figure 4.5 Circuit operation of module-1 of the proposed TPFTMDC converter during the discharging state (i.e., state-II) under (a) mode-1, (b) mode-2, (c) mode-3, (d) mode-4, (e) mode-5, and (f) mode-6.

4.3.2.1 Time-Domain Analysis of the Converter

Mode 1 ($t_0 \leq t < t_1$), Figure 4.5(a): During this interval, the switch S_{21} is off, resulting in the diodes D_{01} and D_{S11} being forward-biased. Consequently, the inductor L_{b1} discharges to $-i_{Lb1min}$ through L_{r1} to the load R_{01} and charges the capacitor C_{r1} .

$$i_{Lb1}^{S-II}(t) = i_{Lb1}^{S-II}(t_0) + \left(\frac{V_{bat} - V_{01}}{L_{r1} + L_{b1}} \right) \times t, \quad i_{Lr1}^{S-II}(t) = i_{Lb1}^{S-II}(t), \quad (4.12a)$$

$$v_{Ca1}^{S-II}(t) = 0, \quad i_{Lb1}^{S-II}(t_1) = i_{Lr1}^{S-II}(t_1) = -I_{Lb1min}^{S-II}. \quad (4.12b)$$

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Mode 2 ($t_1 \leq t < t_2$), Figure 4.5(b): During this interval, the switch S_{21} is on, and the diode D_{S11} is still forward biased. So, the L_{r1} discharges to zero through the load R_{01} and L_{b1} charges linearly through the two current loops $L_{r1}-D_{01}-R_{01}-D_{S11}$ and $V_{bat}-L_{b1}-S_{S21}$, respectively.

$$i_{Lb1}^{S-II}(t) = -I_{Lb1min}^{S-II} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-II}(t_2) = I_{b1}^{S-II}, \quad (4.13a)$$

$$i_{Lr1}^{S-II}(t) = -I_{Lb1min}^{S-II} - \left(\frac{V_{01}}{L_{r1}} \right) \times t, \quad i_{Lr1}^{S-II}(t_2) = 0, \quad v_{Ca1}^{S-II}(t) = 0. \quad (4.13b)$$

Mode 3 ($t_2 \leq t < t_3$), Figure 4.5(c): During this interval, the switching characteristics exhibit similarities to the previous mode. The capacitor C_{r1} discharges to the load while L_{b1} continues to charge to its maximum value $-i_{Lb1max}$.

$$i_{Lb1}^{S-II}(t) = I_{b1}^{S-II} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-II}(t_3) = -I_{Lb1max}^{S-II}, \quad (4.14a)$$

$$i_{Lr1}^{S-II}(t) = 0, \quad v_{Ca1}^{S-II}(t) = 0. \quad (4.14b)$$

Mode 4 ($t_3 \leq t < t_4$), Figure 4.5(d): During this interval, the switch S_{21} is turned off under ZVS. The input acts as a current source, and parallel resonance occurs between L_{r1} and C_{a1} .

$$i_{Lb1}^{S-II}(t) = -I_{Lb1max}^{S-II} + \left(\frac{V_{01} - V_{bat}}{L_{b1}} \right) \times t - \frac{L_{r1}}{L_{b1}} i_{Lr1}^{S-II}(t), \quad (4.15a)$$

$$i_{Lr1}^{S-II}(t) = \omega_{a1} \int_0^t i_{Lb1}^{S-II}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau, \quad (4.15b)$$

$$v_{Ca1}^{S-II}(t) = \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-II}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau, \quad (4.15c)$$

$$i_{Lr1}^{S-II}(t_4) = \omega_{a1} \int_0^{\pi/2\omega_{a1}} i_{Lb1}^{S-II}(\tau) \cos(\omega_{a1}\tau) d\tau, \quad i_{Lb1}^{S-II}(t_4) = I_{b2}^{S-II}, \quad (4.15d)$$

$$v_{Ca1}^{S-II}(t_4) = \frac{1}{C_{a1}} \int_0^{\pi/2\omega_{a1}} i_{Lb1}^{S-II}(\tau) \sin(\omega_{a1}\tau) d\tau. \quad (4.15e)$$

Mode 5 ($t_4 \leq t < t_5$), Figure 4.5(e): During this interval, the auxiliary capacitor C_{a1} discharges through L_{r1} .

$$i_{Lb1}^{S-II}(t) = i_{b2}^{S-II} + \frac{(V_{01} - V_{bat}) \times t}{L_{b1}} + \frac{L_{r1}}{L_{b1}} i_{Lr1}^{S-II}(t_4) - \frac{L_{r1}}{L_{b1}} i_{Lr1}^{S-II}(t), \quad (4.16a)$$

$$i_{Lr1}^{S-II}(t) = i_{Lr1}^{S-II}(t_4) \cos(\omega_{a1}t) - \left(\frac{V_{01} - v_{Ca1}^{S-II}(t_4)}{Z_{a1}} \right) \sin(\omega_{a1}t) + \omega_{a1} \int_0^t i_{Lb1}^{S-II}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau, \quad (4.16b)$$

$$v_{Ca1}^{S-II}(t) = V_{01} - (V_{01} - v_{Ca1}^{S-II}(t_4)) \cos(\omega_{a1}t) - Z_{a1} i_{Lr1}^{S-II}(t_4) \sin(\omega_{a1}t) + \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-II}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau, \quad (4.16c)$$

$$i_{Lr1}^{S-II}(t_5) = I_{r1}^{S-II}.$$

Mode 6 ($t_5 \leq t < t_6$), Figure 4.5(f): During this interval, the reverse current of i_{Lr1} activates the antiparallel diode of switch S_{21} and discharges through the current loop L_{r1} - D_{01} - R_{01} - D_{S11} - D_{S21} .

$$i_{Lb1}^{S-II}(t) = I_{b1}^{S-II}(t) \approx -I_{Lb1\max}^{S-II} \quad (4.17a)$$

$$i_{Lr1}^{S-II}(t) = I_{r1}^{S-II} - \left(\frac{V_{01}}{L_{r1}} \right) \times t, \quad v_{Ca1}^{S-II}(t) = 0. \quad (4.17b)$$

4.4 Design of the Resonant Inductor and Capacitor

The resonant auxiliary capacitor C_{a1} affects the ZVS condition of the switch. In mode 7, the ZVS condition has been achieved for the switch S_{21} , and it is assumed that the current flow through the L_{r1} - C_{a1} - D_{11} should be large enough for the resonance. Generally, the snubber capacitance is selected to be 10 times the parasitic capacitance. However, the value of the capacitance of C_{a1} is more than 20 times the output capacitance of the switch S_{21} , i.e., $C_{a1} > 20 \times C_{oes_S21}$. It is charged by L_{r1} and is about double the main inductor current during the switch's turn-off.

In mode 5, the i_{Lr1} is derived in (4.5c). The duration of resonance between L_{r1} and C_{r1} constitutes approximately one-fourth of the total resonant period. The rising time of the i_{Lr1} typically constitutes 10% of the minimum on-time of the switch. However, to satisfy the ZVS condition, the i_{Lr1} rising time is set to 50% of the minimum on-time in this article. In (4.18), it represents the combination of the energy-domain and time-domain constraints during modes 4 and 5, respectively. In mode 4, the i_{Lr1} rises linearly with time, and in mode 5, during a quarter of the resonant cycle, it supports at least the minimum inductor current ($I_{L1\min}$) for the discharge of C_{r1} . In mode 7, C_{r1} and C_{a1} are in series, as seen from the S_{21} side of the switch. So, the switch

S_{21} voltage V_{S21} can be represented as (4.23). Now, applying the charge conservation law across the switch yields (4.24), and the effective capacitance C_{S1} as given in (4.25).

$$t_5 - t_3 = \frac{L_{r1}}{V_{01}} I_{L1\min}^{S-I} + \frac{T_{r1}}{4} < 0.5 D_{\min} T_s \quad (4.18)$$

Where $T_{r1} = 2\pi/\omega_{r1}$, $T_s = 1/f_s$, $D_{\min}$ = minimum duty cycle. From (4.18), C_{r1} is designed as follows:

$$C_{r1} > \frac{D_{\min}^2}{\pi^2 L_{r1} f_s^2} + \frac{4L_{r1} \left(I_{L1\min}^{S-I} \right)^2}{\pi^2 V_{01}^2} - \frac{4D_{\min} I_{L1\min}^{S-I}}{\pi^2 V_{01} f_s} \quad (4.19)$$

Since $4D_{\min} I_{L1\min}^{S-I} / \pi^2 V_{01} f_s \ll D_{\min}^2 / \pi^2 L_{r1} f_s^2$, therefore, (4.19) can be rewritten as follows:

$$C_{r1} > \frac{D_{\min}^2}{\pi^2 L_{r1} f_s^2} + \frac{4L_{r1} \left(I_{L1\min}^{S-I} \right)^2}{\pi^2 V_{01}^2} \quad (4.20)$$

$$i_{Lr1}^{S-I}(t_5) = I_{rp}^{S-I} = I_{L1\min}^{S-I} + I_{Lb1\max}^{S-I} + \frac{V_{01}}{Z_{r1}} = I_{rm}^{S-I} + \frac{V_{01}}{Z_{r1}},$$

$$\text{where } I_{rm}^{S-I} = I_{L1\min}^{S-I} + I_{Lb1\max}^{S-I}.$$

$$L_{r1} = \left(V_{01} / \left(I_{rp}^{S-I} - I_{rm}^{S-I} \right) \right)^2 C_{r1} \quad (4.21)$$

From (4.20) and (4.21), C_{r1} can be calculated as follows:

$$C_{r1} > \frac{D_{\min} \left(I_{rp}^{S-I} - I_{rm}^{S-I} \right)}{\pi V_{01} f_s} \left/ \sqrt{1 - 4 \left(I_{L1\min}^{S-I} \right)^2 / \pi^2 \left(I_{rp}^{S-I} - I_{rm}^{S-I} \right)^2} \right. \quad (4.22)$$

From (4.21) and by the energy conservation law across the switch S_{21} within *state-I* mode 7, the resonant inductor L_{r1} can be designed as given in (4.26):

$$V_{S21}(t) = V_{Ca1}(t) + V_{Cr1}(t) \quad (4.23)$$

$$V_{Cr1}(t) = \frac{C_{r1}}{C_{r1} + C_{a1}} V_{S21}(t) \quad (4.24)$$

$$C_{s1} = C_{r1} C_{a1} / (C_{r1} + C_{a1}), \quad V_{01} - V_1 \approx 0.96 \times V_{01} \quad (4.25)$$

$$L_{r1} < \left\{ 0.96 \times V_{01} \left(2 \frac{C_{s1}}{C_{a1}} - 1 \right) \right/ \frac{I_{rp}}{C_{a1}} \sqrt{C_{s1}} \right\}^2 \quad (4.26)$$

4.4.1 Boundary Condition for the ZVS and ZCS Region

A ψ_{ZVS} feasibility index in (4.27) is defined as the ratio of the selected resonant capacitor C_{r1} to the minimum required resonant capacitance C_{r1_min} obtained from (4.22). As shown in Figure 4.6(a), the values less than unity indicate ZVS operation.

$$\psi_{ZVS}(D_1) = \frac{C_{r1}}{C_{r1_min}(D_1)} \quad (4.27)$$

A ψ_{ZCS} feasibility index is defined as the ratio of the resonant half-cycle duration to the available switch-off time. Thus, the ZCS condition can be achieved as given in (4.28). Figure 4.6(b) shows that the design ensures a ZCS region greater than unity over the normal operating duty range.

$$\psi_{ZCS}(D_1) = \frac{(1-D_1)T_s}{\pi\sqrt{L_{r1}C_{r1}}} \quad (4.28)$$

In Figure 4.6(c), when D_1 is fixed in (4.27), the variation in load R_{01} changes the output and input currents without affecting the switching timing. Consequently, the ZVS condition, which depends on the available commutation current, is load dependent and degrades under light-load operation. In contrast, the ZCS condition is governed solely by the resonant half-cycle duration and the available off-time, and is therefore independent of the load resistance.

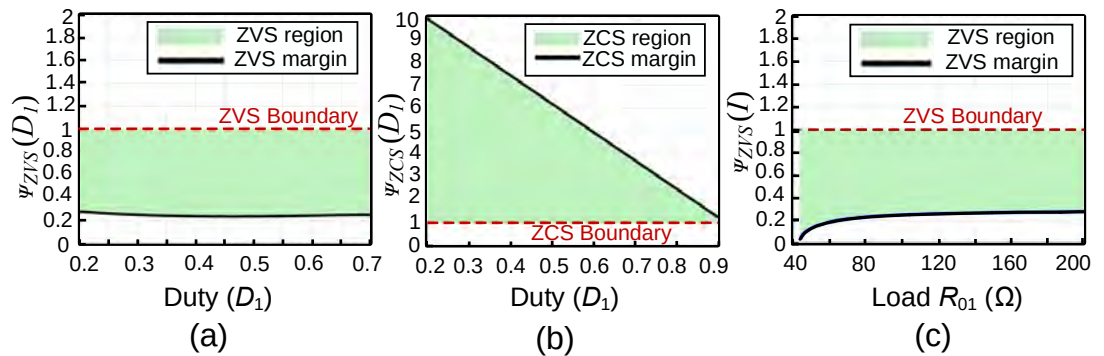


Figure 4.6 Boundary condition of ZVS and ZCS region, (a) ZVS region for a change in duty ratio D_1 , (b) ZVS region for a change in load R_{01} , and (c) ZCS region for a change in duty ratio D_1 .

4.5 Controller Operation

The proposed converter control operation is bifurcated for two distinct operational *states*. The regulation of both the 48V and 12V outputs is achieved with

the use of TI-F28379D launch pad microcontroller. The boost output V_{01} is controlled to maintain a 48V output voltage using a PI controller (C_1). The step-down output (V_{bat}) interfaces with a battery and is regulated by inner and outer loop controls C_2 and C_3 . The control is implemented using a CCCV battery charging method, as illustrated in Figure 4.7. The outputs from both controllers are processed by digital PWM controllers. The phase-shift (Φ) between the carrier signals for an n -module TPFTMDC converter is $360^\circ/n$. With two module TPFTMDC converter, G_{S11} and G_{S12} exhibit an 180° phase shift, which regulates the battery output and the DC-link, respectively. A circuit for state selection alternates control between *state I* and *state II* depending on the magnitude of the input voltage.

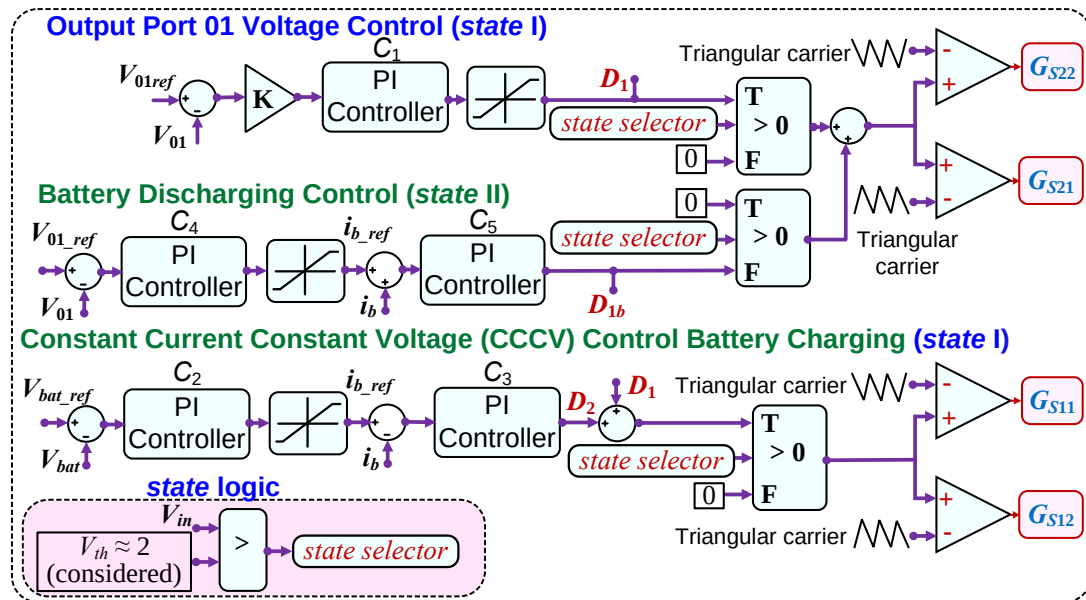


Figure 4.7 Closed-loop control of proposed TPFTMDC converter.

4.6 Experimental Validation

The experimental validation determines the dynamic behavior and performance of the proposed TPFTMDC converter under various operating *states*. Figure 4.8 shows the experimental setup developed in the laboratory to test the proposed topology in real time. It has been tested with an input supply voltage of 24V and variable output voltages at output ports 01 and 02. The specified values of circuit parameters, aligned with the mathematical relations established in Sections 4.3.1 and 4.3.2, along with the utilized values of circuit parameters, are presented in Table 4.1. The microcontroller TI-F28379D is used for generating the PWM gating signals and

3

testing the proposed TPFTMDC converter. Two current sensors (ACS712) are used to measure the battery current at the output port 02 in both directions: one during charging mode control and the other during discharging mode. All voltage and current measurements presented here correspond to the polarities depicted in Figure 4.1, except for the battery current, which is reversed. A positive battery current indicates the battery is charging, whereas a negative current indicates it is discharging. The experimental findings are illustrated in Figure 4.9 to Figure 4.15. The proposed converter is analysed under both healthy operating conditions and scenarios involving open-circuit switch faults (OCSF). The findings are subsequently detailed and analysed in three distinct sub-sections as follows:

Table 4.1
SYSTEM PARAMETERS

Parameters		Values used
DC input / bus voltages (V_{in} / V_{01} / V_{02})		24V / 48V / 12V
Inductors	L_1, L_2, L_{b1}, L_{b2}	560 μ H
	$L_{r1} = L_{r2}$	33 μ H
Capacitors	$C_{a1} = C_{a2}$ / $C_{r1} = C_{r2}$	1 nF / 50 nF
	C_{01}, C_{02}	100 μ F, 10 μ F
IGBT switch IKP06N60T	I_C, V_{CE}, C_{OSS}	6 A, 600 V, 28 pF
Load resistance / Battery voltage (R_{01} / V_{bat})		90 Ω / 12 V
Switching frequency (f_s)		20 kHz

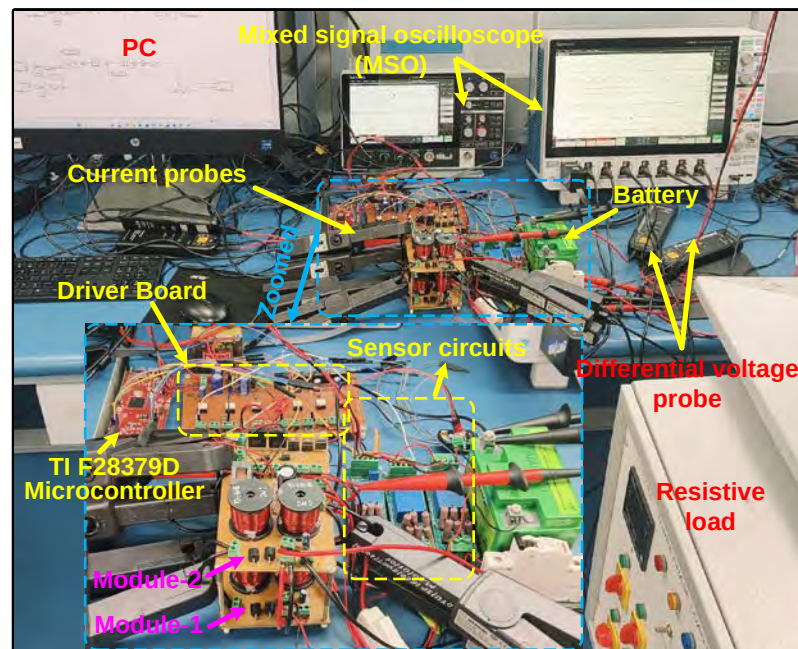


Figure 4.8 Experimental setup of the proposed TPFTMDC converter.

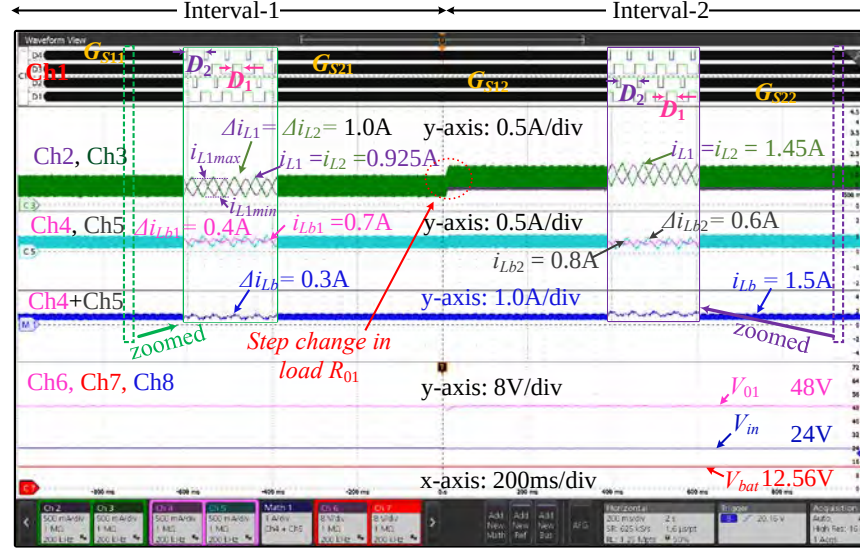
4.6.1 Under State I Operation (Charging)

The charging of the battery with step-down voltage gain capability at the output port 02 is tested under healthy conditions, as shown in Figure 4.9. A single battery with a nominal voltage of 12V is connected for charging and discharging under these conditions. The results have been taken for two intervals. In interval-1, the test was conducted at nominal load (i.e., load resistance R_{01}), and in interval-2, load resistance is $R_{01}/2$ to demonstrate dynamic changes and resonance conditions. Figure 4.9(a) shows the characterization and analysis of the ZVS and ZCS of the switch S_{21} , which is responsible for controlling the DC bus voltage at output port 01.

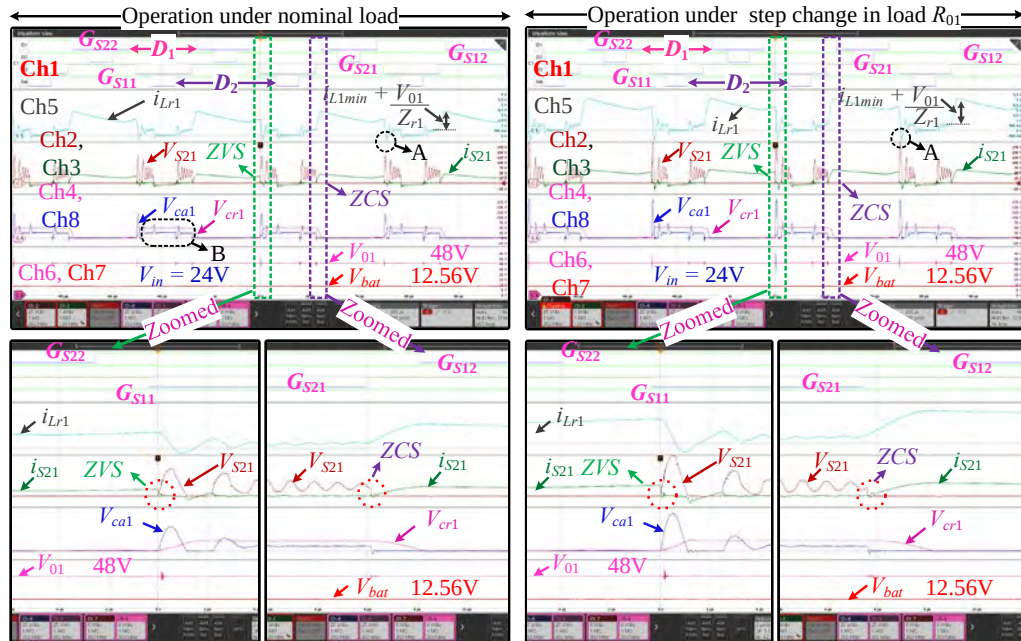
In Figure 4.9, channel 1 of the oscilloscope shows the digital PWM. The duty ratios D_1 and D_2 are associated with the G_{S11} and G_{S21} , and the phase shifts of them are associated with G_{S12} and G_{S22} , respectively. In Figure 4.9(a), channels 2 and 3 shows the input currents, with an average value of $i_{L1} = i_{L2} = 0.925$ A for interval-1 and 1.45 A for interval-2 and an input ripple current of $\Delta i_{L1} = 0$ A, whereas in Figure 4.9(b) and Figure 4.9(c) it shows turn-off ZVS of switch S_{21} and turn-on ZCS of switch S_{21} , respectively, for module 1. The areas circled as A and B in Figure 4.9(b) illustrate that the current in L_{r1} is more than twice the main inductor current i_{L1} , that it should decline below zero, and the capacitor C_{a1} voltage is charging, respectively. This mismatch in v_{Ca1} is caused by the switch's output capacitance. Channels 4 and 5 shows the phase currents of the battery, with average values of $i_{Lb1} = 0.7$ A and $i_{Lb2} = 0.8$ A. Channel m1 shows the mathematical addition of the battery phase currents, i.e., $i_{Lb1} + i_{Lb2} = i_{Lb} = 1.5$ A, and also battery ripple current of $\Delta i_{Lb} = 0.3$ A for both intervals. Channels 6 and 7 are the output port 01 voltage, i.e., $V_{01} = 48$ V and the battery voltage, i.e. $V_{bat} = 12.56$ V, respectively. Figure 4.9(b) and Figure 4.9(c) show the resonant inductor L_{r1} current (i_{Lr1}) and C_{r1} voltage (v_{Cr1}), respectively, for module 1. Channel 8 in Figure 4.9(a) is the input voltage, i.e., $V_{in} = 24$ V, whereas in Figure 4.9(b) and Figure 4.9(c), show the auxiliary capacitor voltage v_{Ca1} for module 1.

In Figure 4.10(a), the characterization of the step change in output voltage V_{01} has been captured to demonstrate the dynamic change and resonance condition. The input currents, with an average value of $i_{L1} = i_{L2} = 0.80$ A for the interval-1 and 1.10 A for the interval-2. Figure 4.10(b) and Figure 4.10(c) show turn off ZVS of switch S_{21} and turn on ZCS of switch S_{21} for this condition, respectively, for module 1. The phase

currents of the battery, with an average value of $i_{Lb1} = 0.48$ A and $i_{Lb2} = 0.52$ A and a battery ripple current of $\Delta i_{Lb} = 0.3$ A for both intervals. The sum of the battery phase current $i_{Lb1} + i_{Lb2} = i_{Lb} = 1.0$ A. The output port 01 voltage, i.e., $V_{01} = 48$ V for the interval-1 and 60 V for the interval-2, and the battery voltage, i.e., $V_{bat} = 12.69$ V.



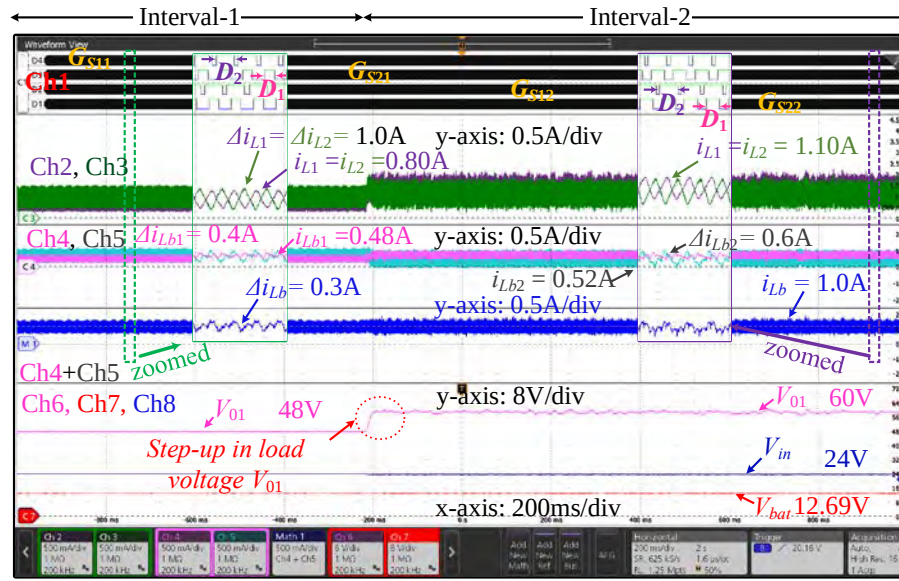
(a)



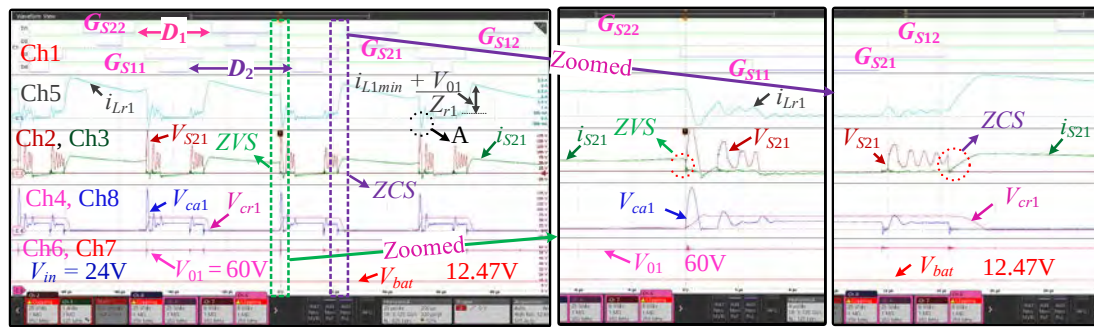
(b)

(c)

Figure 4.9 Experimental results of the proposed TPFTMDC converter under healthy operation, with load varying from nominal R_{01} to $R_{01}/2$: (a) steady-state waveforms; ZVS and ZCS characteristics of switch S_{21} in module 1 at (b) nominal load R_{01} , and (c) half load resistance $R_{01}/2$.



(a)



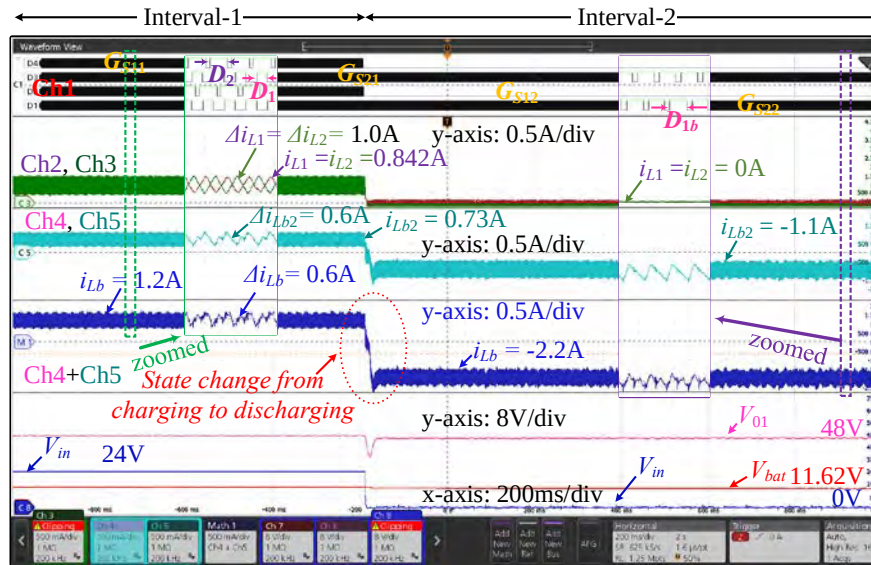
(b)

Figure 4.10 Experimental results of the proposed TPFTMDC converter under healthy operation for a step change in V_{01} from 48 V to 60 V: (a) input / output currents of the boost and battery sides, and (b) ZVS and ZCS of switch S_{21} at $V_{01} = 60$ V.

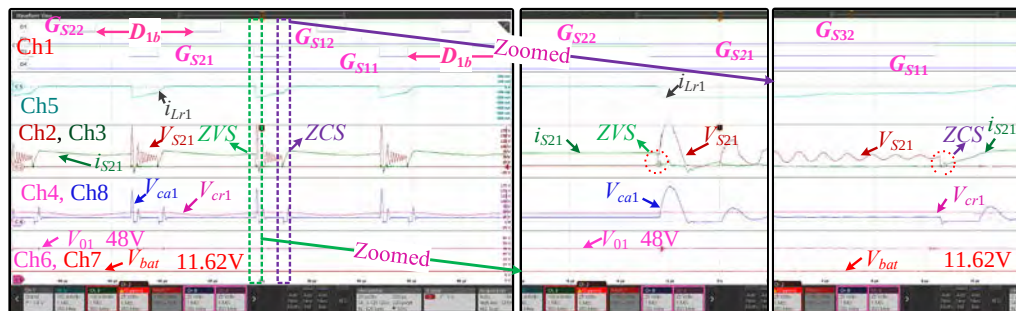
4.6.2 Under State II Operation (Discharging)

In Figure 4.11, the characterization of the state change from *state* I to II (i.e., from charging to discharging) has been captured to demonstrate the dynamic change and resonance condition. The input currents, with an average value of $i_{L1} = i_{L2} = 0.842$ A for the interval-1 and 0 A for the interval-2 and an input ripple current of $\Delta i_{L1} = \Delta i_{L2} = 1$ A and 0 A for the intervals-1 and 2, respectively. The battery current has an average value of $i_{Lb} = 1.2$ A for the interval-1 and $i_{Lb} = -2.20$ A for the interval-2, with a battery ripple current of $\Delta i_{Lb} = 0.6$ A for both intervals. Figure 4.12 shows the characterization of the step change in load R_{01} during discharging. The battery current has an average value of $i_{Lb} = -2.28$ A in the interval-1 and $i_{Lb} = -4.5$ A in the interval-2, with a battery

ripple current of $\Delta i_{Lb} = 0.3 \text{ A}$ in both intervals. In Figure 4.13, the characterization of the step change in output voltage V_{01} has been captured during discharging to demonstrate the dynamic change. The battery current has an average value of $i_{Lb} = -2.24 \text{ A}$ in the interval-1 and $i_{Lb} = -1.667 \text{ A}$ in the interval-2, with $\Delta i_{Lb} = 0.3 \text{ A}$ in both intervals. The output port 01 voltage, i.e., $V_{01} = 48 \text{ V}$ and 36 V for intervals 1 and 2, respectively, and the battery voltage, i.e., $V_{bat} = 11.47 \text{ V}$.



(a)



(b)

Figure 4.11 Experimental results of the proposed TPFTMDC converter under healthy operation for a transition from *state* I to *state* II (battery charging to discharging): (a) input/output waveforms of the boost and battery sides for both states, and (b) ZVS and ZCS of switch S_{21} at $V_{01} = 48 \text{ V}$.

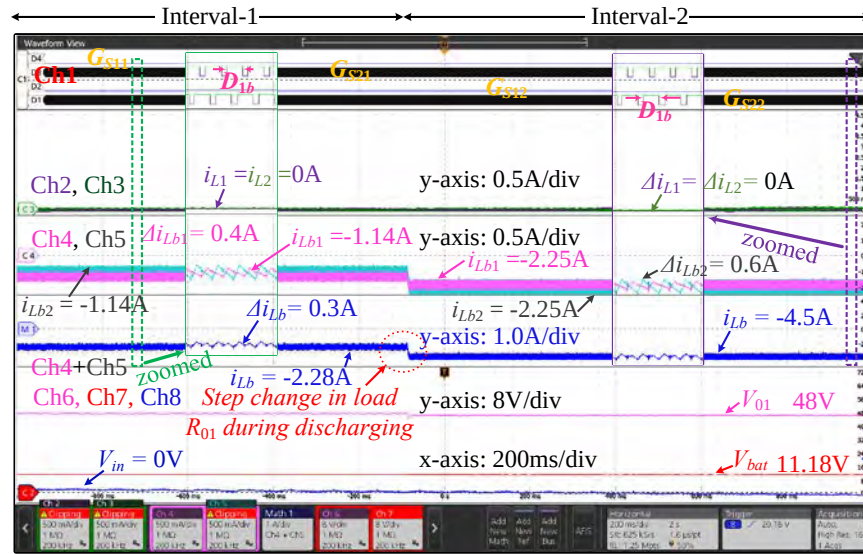


Figure 4.12 Experimental results of the proposed TPFTMDC converter under healthy operation from nominal load to a load change in R_{01} during state II operation (discharging).

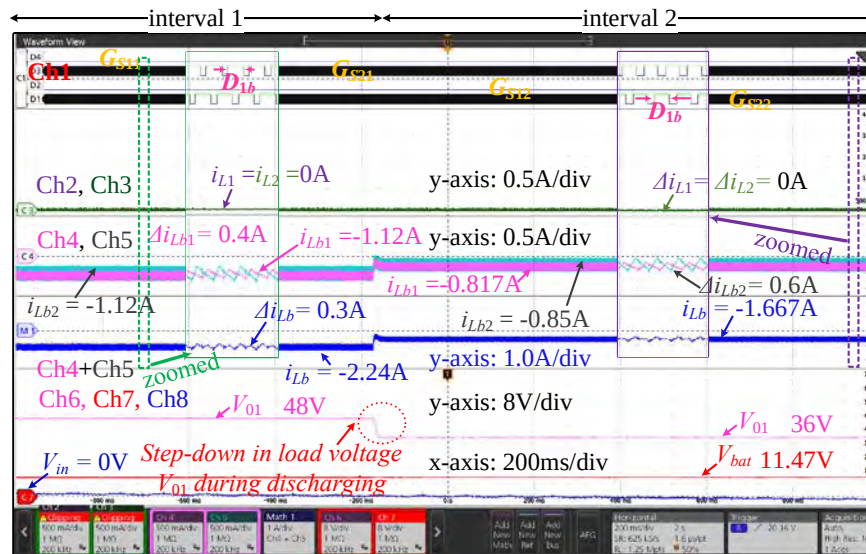


Figure 4.13 Experimental results of the proposed TPFTMDC converter under healthy operation for a step change in V_{01} from nominal voltage $V_{01} = 48V$ to $V_{01} = 36V$ for a state II operation (discharging).

4.6.3 Under Open Circuit Switch Fault Condition

Figure 4.14 presents the characterization of the OCSF in S_{11} and S_{21} (unhealthy condition), demonstrating the fault-tolerant capability of the proposed TPFTMDC converter under both steady-state and dynamic conditions. The input currents, with an average value of $i_{L1} = i_{L2} = 0.925A$ for the interval-1 and $i_{L1} = 0A$, $i_{L2} = 1.85A$ for the

interval-2 (i.e., under OCSF condition) and an input ripple current of $\Delta i_L = 0$ A and 1 A for the intervals 1 and 2, respectively. Channel m_1 in this case has been taken as the sum of input current i.e. $i_{L1} + i_{L2} = i_L = 1.85$ A, to demonstrate the ripple cancellation due to interleaving. The phase currents of the battery, with an average value of $i_{Lb1} = i_{Lb2} = 0.75$ A for the interval-1 and $i_{Lb1} = 0$ A and $i_{Lb2} = 1.5$ A for the interval-2 and a battery ripple current of $\Delta i_{Lb} = 0.3$ A and 0.6 A for the intervals 1 and 2, respectively. The redistribution of current ensures uninterrupted power transfer despite the failure of multiple switch OCSF condition. Moreover, the interleaving effect effectively reduces overall current ripple, validating the robustness of the proposed fault-tolerant design.

In Figure 4.15, the characterization of the step change in output voltage V_{01} has been captured for only one module, i.e., the switches S_{11} and S_{21} are permanently off, and the input/output connection has been disconnected from the second stack to demonstrate the dynamic change. The input currents have an average value of $i_{L2} = 1.60$ A for interval-1 and 2.2 A for interval-2, and an input ripple current of $\Delta i_{L1} = 1$ A for both intervals. The phase currents of the battery have an average value of $i_{Lb2} = 1$ A and a battery ripple current of $\Delta i_{Lb1} = 0.6$ A for both intervals. The output port-01 voltage, i.e., $V_{01} = 48$ V and 60 V for intervals 1 and 2, respectively, with $V_{bat} = 12.89$ V.

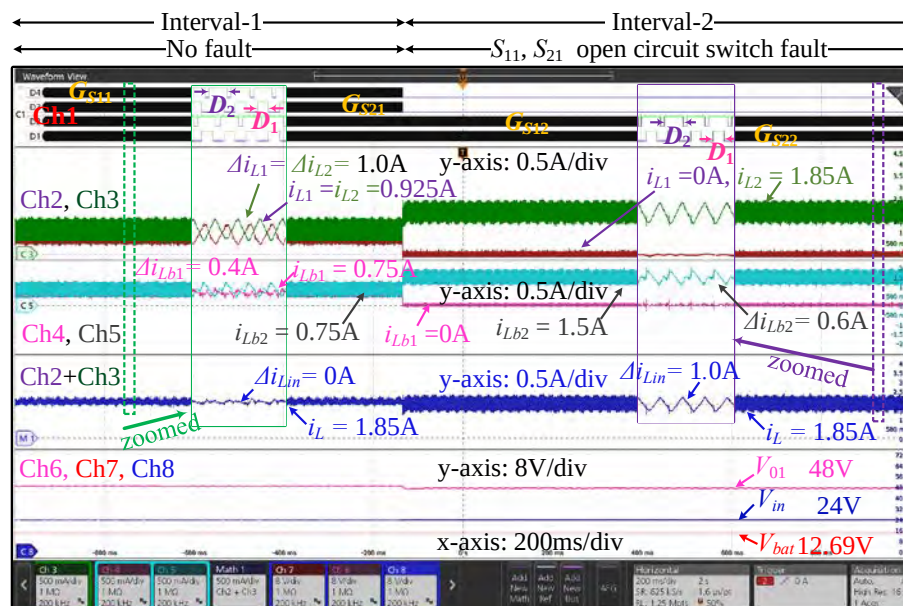


Figure 4.14 Experimental results of the proposed TPFTMDC converter from healthy operation to OCSF in S_{11} and S_{21} (unhealthy condition).

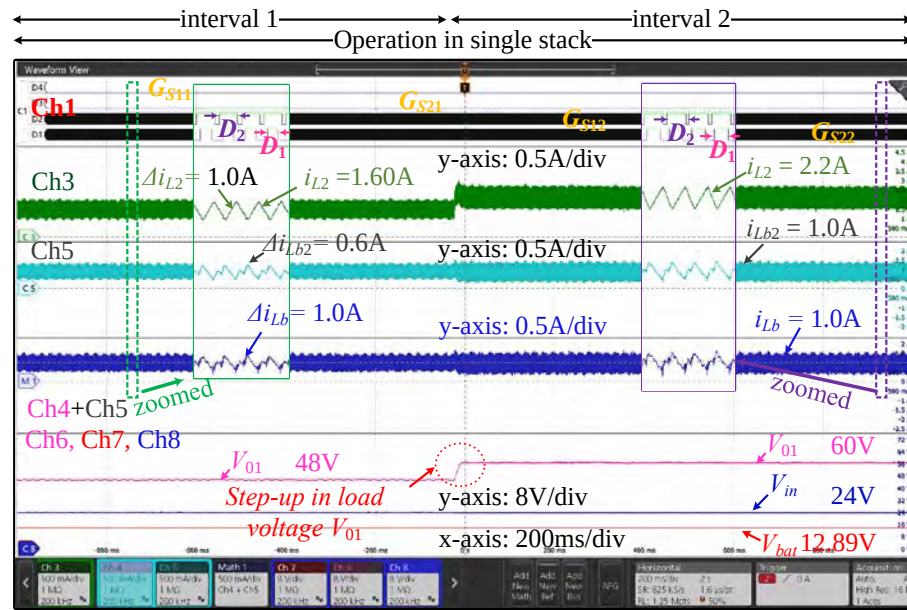


Figure 4.15 Experimental results of the proposed TPFTMDC converter (single module) for a step change in V_{01} from 48 V to 60 V.

4.7 Conclusions

The chapter presents a novel TPFTMDC soft-switched multiport converter; it also presents a detailed design procedure and operational functionality of the proposed converter. The modular design minimizes both input and battery current ripple, reduces the size of passive components, and enhances current capacity while improving fault-tolerant capability. Time-multiplexing control reduces the number of semiconductor devices required relative to the total number of ports and increases system redundancy, thereby enhancing reliability. The mathematical model for each mode has been developed for both operational states based on the time frame. The design of the resonant components has been thoroughly examined. A ZVS and ZCS region has been plotted with respect to the selected parameters for varying load and duty cycle. It also provides fault tolerance against OCSFs. The control strategy has been developed to regulate power distribution among the various ports while simultaneously upholding CCCV battery charging, ensuring a stable boosted dc bus voltage, and improving the resilience of DC power availability. The proposed architecture efficiently manages DC bus voltages across various operating states at all output ports.

Chapter 5

STANDALONE SOLAR PV-FED TIME MULTIPLEXED FAULT-TOLERANT FOUR-PORT DC-DC CONVERTER

5.1 General

11 DC-DC converters are extensively used in a wide range of industrial applications, including renewable energy systems, ships, aeroplanes, and automobiles powered by electricity. With increasing levels of pollution, climate change, rapid increase in the cost of fuel, and the escalation of global warming issues, energy transition and e-mobility technologies have gained attention for research and sustainable development. Consequently, automobile manufacturers have begun producing environmentally friendly electric vehicles (EVs) and hybrid electric vehicles (HEVs). The principal components of these kinds of vehicles are the motor drive system and battery pack design with charge/discharge parameters. In which an effective converter topology with respect to power ratings of the EVs motor to propel the different drive cycles and motoring and regenerative operation, and the charge/discharge current profile of the battery pack are the major areas of concern [119].

3 The DC-DC converter topologies are important for achieving optimal power management in three-wheeler (3-W) and four-wheeler (4-W) light electric vehicle (LEV) systems because they efficiently regulate and control the flow of electrical energy. The application of multiphase buck converters in LEVs, emphasizing their ability to handle high currents and manage higher power requirements while minimizing thermal stress and improving overall system efficiency, is crucial for supporting the performance demands of modern EVs [87]. Advanced converter designs, such as interleaved and multiphase configurations, have gained attention for their ability to reduce ripple, improve thermal performance, and increase converter robustness under variable load conditions [79], [80], [81], [120]. Figure 5.1(a) presents the propulsion system of the LEVs with integrated solar PV. It shows the converter architecture that connects energy supplies to vehicle drive trains and auxiliary loads. Figure 5.1(b) shows the proposed four-port fault-tolerant DC-DC (FPFTDC) non-isolated power converter for low-voltage and LEV applications.

Multiport converters (MPCs) have emerged as a transformative technology, critically improving the cost, size, weight, and efficiency of the system. These converters, which can connect to multiple energy sources and storage systems, are important for making the best use of energy and distributing it evenly. This has a direct effect on how long LEVs last (i.e., improvements in battery charging and discharging cycles) and how well they work. Recent studies emphasize the strategic role of MPCs in effectively managing fluctuating power demands and extending battery life. Bidirectional MPCs enable seamless energy transitions between propulsion and auxiliary systems, boosting energy conservation and vehicle range [20], [21], [26], [27], [28]. Moreover, advanced MPC architectures integrate renewable energy sources into LEVs, reducing grid power dependency and enhancing the overall energy autonomy of vehicles [24]. A solar-fed switched boost single input multiple output (SIMO) converter is demonstrated in [23]. Such systems not only increase energy throughput, but they also contribute to reducing the carbon footprint. Lastly, the capability of MPCs to provide voltage regulation across various subsystems of LEVs further ensures the reliability and safety of these vehicles [18].

The demand for reliability and uninterrupted operation has prompted significant interest in fault-tolerant converter topologies. These converters are specifically designed to maintain functionality even when one or more components fail, thereby ensuring continuous operation. Recent studies have demonstrated the benefits of fault-tolerant converters in LEVs, where the redundancy in their design can significantly mitigate the risks associated with component failures [29], [32], [67]. One key advancement is the development of a fault-tolerant multiphase converter, which not only provides redundancy but also evenly distributes the load among the phases, thereby reducing the impact of a single-phase failure. Moreover, the introduction of fault-tolerant interleaved converters has been found to effectively increase system reliability while also improving power density is a critical factor in the compact spaces of LEVs [37], [40], [66], [68]. Additionally, the implementation of modular converter designs allows for easy isolation and replacement of faulty modules, minimizing downtime and maintenance requirements [30], [39], [70].

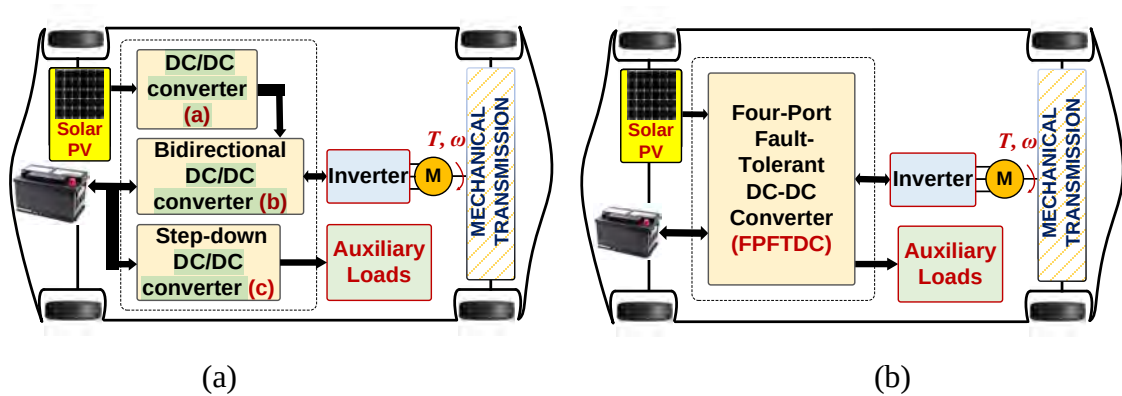


Figure 5.1 Light electric vehicle propulsion system with (a) conventional power converter topology and (b) proposed FPFTDC converter.

Solar PV-based multifunctional converters are pivotal in enhancing the energy autonomy of LEVs by efficiently integrating renewable energy. These converters facilitate optimal energy conversion from photovoltaic panels to EV batteries, thereby extending the driving range without external charging. They also support auxiliary vehicle functions and improve overall energy management [19], [121], [122]. In [123], a high-voltage boosting transformer less inverter for rooftop PV microgrid integration, featuring high voltage gain and leakage current suppression, is presented. In [124], two innovative pulse width modulation (PWM) strategies i.e., enhanced level-shifted PWM and enhanced phase-shifted PWM, are proposed to improve the efficiency and power quality in the solar PV applications. Recent developments include converter efficiency and compactness advancements, which are critical for the constrained space within LEVs. These systems not only boost the vehicle's sustainability by reducing reliance on non-renewable power sources but also enable innovative functionalities such as bidirectional charging, contributing to smarter energy networks [72], [125].

The charging infrastructure significantly influences EV functionality and adoption; it has three levels of charging: *level 1* is low power, with single-phase ac charging less than 3.5 kW or dc charging less than 15 kW; *level 2* is a medium power, with three-phase ac charging less than 22 kW; and *level 3* is a high power, with dc fast charging greater than 22 kW, which lets the batteries be charged quickly. Compatibility with various connectors, including CHAdeMO, CCS, and proprietary systems like Tesla superchargers, is crucial for operational flexibility and user convenience [126]-[128]. These systems shape not only charging efficiency and vehicle range but also

battery longevity and health, underscoring their critical role in sustainable transportation evolution. Charging current ripple has drawbacks, as do larger average charge currents, which require more energy to maintain battery charge. In [89], a strategy to effectively suppress charging current ripple in a three-level T-type converter under distorted grid conditions is presented. A novel control strategy for off-board DC fast charging is designed and presented in [82] to provide a ripple-free output current.

This chapter presents a non-isolated FPFTDC converter. It possesses the ability to control the maximum power point (MPP) and regulate the DC bus voltage for two distinct outputs, namely medium voltage DC (MVDC) and low voltage DC (LVDC) levels, suitable for motor loads and auxiliary low voltage DC loads, respectively. The proposed converter has implemented time-multiplexing control of the semiconductor switching devices to enable output ports with reduced switches and fault-tolerant capability. Additionally, it incorporates a bidirectional feature for charging and discharging the EV battery.

5.2 Proposed Solar PV Fed Fault Tolerant Multiport Converter

The block diagram of the proposed FPFTDC converter is depicted in Figure 5.2(a). A non-isolated four-port converter is designed with MPP control, dc bus voltage regulation of the LVDC and MVDC output ports, and a battery charging/discharging control algorithm to maintain the load power requirement with respect to solar PV power generation and energy storage system. Figure 5.2(b) shows the circuit diagram of the proposed FPFTDC converter. The two-phase interleaved boost converter topology is used on the solar PV side for MPP tracking with reduced solar PV current ripple Δi_{in} and therefore, the size of the capacitor C_{pv} reduces. The design calculation of PV side capacitor is presented in the next heading. The converter has an MVDC (output port 01, i.e., V_{01}) and two LVDC (output port 02 and output port 03, i.e., V_{02} and V_{bat} , respectively) ports. An LVDC output port is connected to a load, whereas the other is connected to battery energy storage (BES), which regulates the dc bus voltages. The carrier signal used for G_{Sbb1} and G_{Sbb2} is 180° phase-shifted compared to the carrier signal used in G_{Sb1} and G_{Sb3} , whereas the modulation of G_{Sb2} depends on the time-multiplexing control of the switched boost action of leg 1. Further, the switching signals G_{Sbb1} , G_{Sbb2} , and G_{Sb1} , G_{Sb3} are complementary in nature. The possible 'states' of the proposed converter is shown in Figure 5.3.

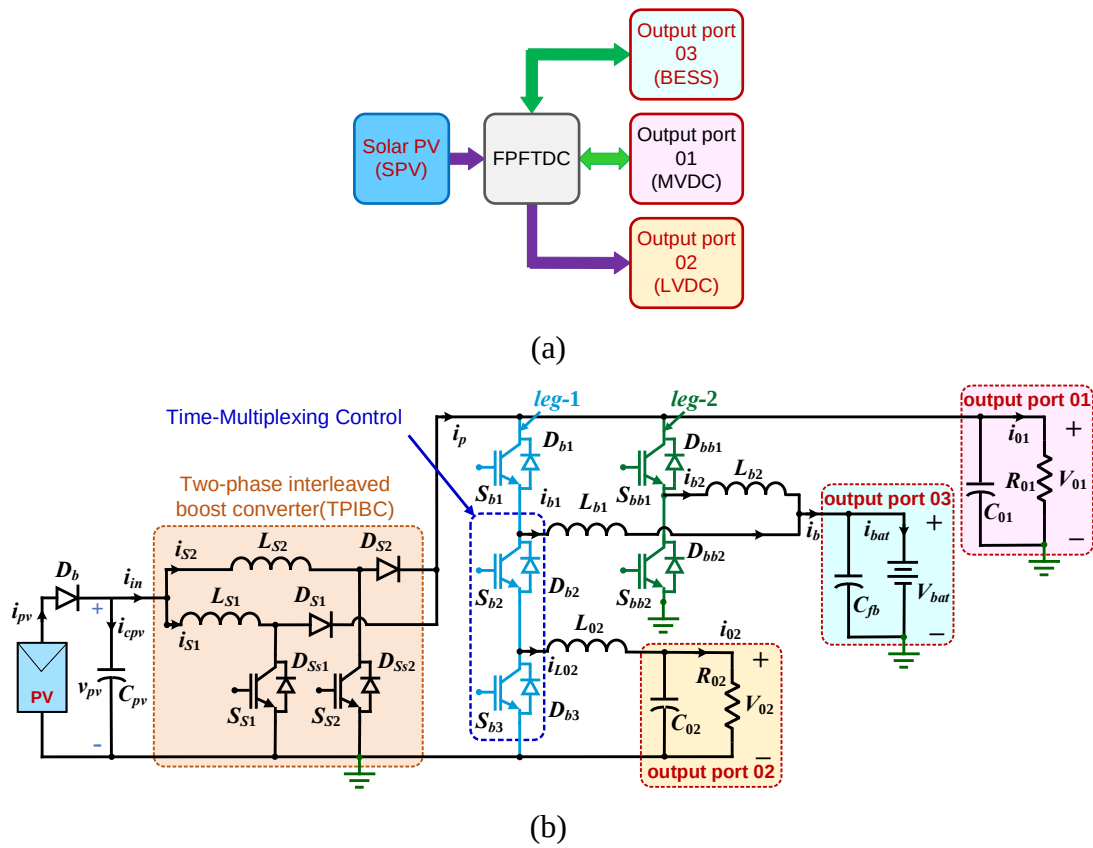


Figure 5.2 Proposed four-port fault-tolerant DC-DC (FPFTDC) converter (a) block diagram, and (b) schematic diagram.

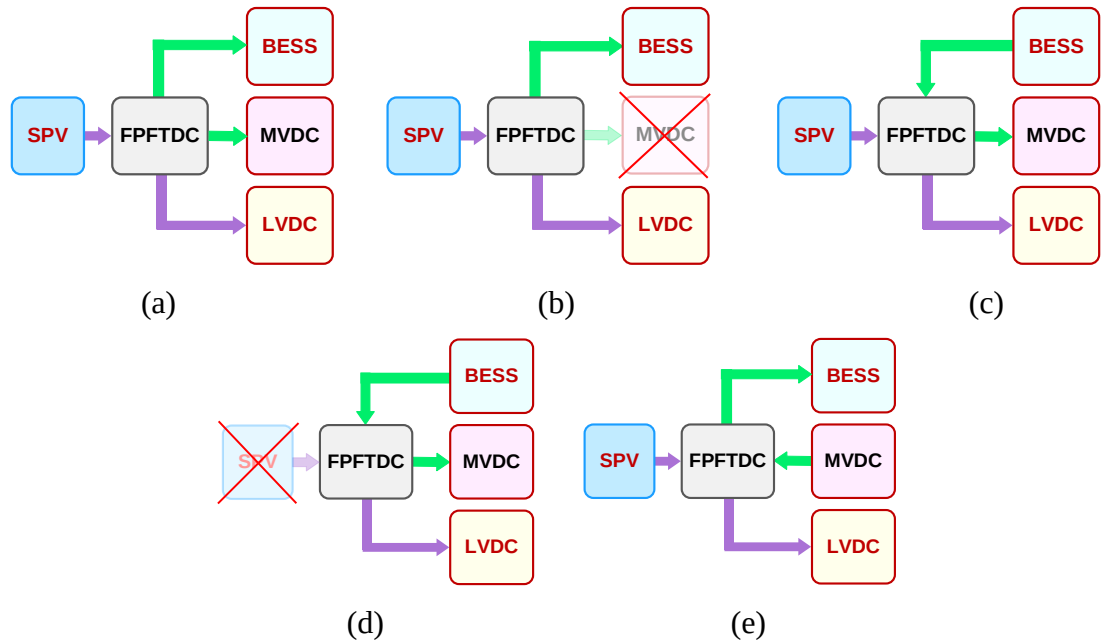


Figure 5.3 Operating states of the proposed FPFTDC converter when (a) $P_{SPV} > P_{MVDC} + P_{LVDC}$ and MPP state; (b) $P_{SPV} > P_{LVDC}$ with EV in rest under MPP and LPRM state; (c) $P_{SPV} < P_{MVDC} + P_{LVDC}$ and MPP state; (d) $P_{SPV} = 0$ state; (e) $P_{SPV} > P_{LVDC}$ with regenerative braking and MPP state.

The solar PV side input converter is a conventional two-phase interleaved boost converter (TPIBC), which is shown in Figure 5.2(b) under the shaded region. The different values of duty ratio (D_1), decide two different regions of operations under continuous conduction mode (CCM), i.e., (a) non-overlapping mode and (b) overlapping mode, as shown in Figure 5.4. Due to phase interleaving, high-frequency operation, and higher duty application under MPP tracking, the input current behavior of the TPIBC is considered mainly in CCM, and the detailed behavior of TPIBC is presented in Table 5.1. Where L_{s1} and L_{s2} are the phase inductors of TPIBC, V_{pv} is the solar PV voltage, and T is the switching period. It can be seen that the input current ripple in any mode decreases with the phase interleaving. Mathematically, it is presented in the next heading.

The proposed converter is enabled with bidirectional functionality, i.e., during surplus PV-generated power, both legs of the converter charge the battery in buck mode of operation with voltage regulation of the MVDC port, which reduces the battery charging current ripple. Similarly, during deficit PV-generated power, the battery discharges under boost mode to fulfill the power demands of loads and maintain the voltage at both the output ports using both legs of the proposed converter. The MPP control of solar PV is achieved using two semiconductor switches, S_{s1} and S_{s2} , of the interleaved boost converter with a 180° phase shifted carrier. The overall system is fault-tolerant; a fault in any semiconductor switch causes the converter to behave like a conventional converter, and the FPFTDC behavior remains intact.

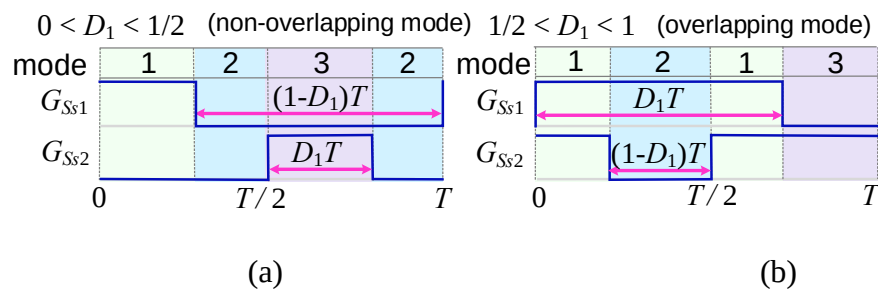


Figure 5.4 TPIBC switching pattern for (a) $0 < D_1 < 1/2$, and (b) $1/2 < D_1 < 1$.

Table 5.1
INPUT CURRENT DERIVATIVES (di_{in}/dt) WITH MODES OF OPERATION AND SWITCHING STATES IN TPIBC

Duty Region	Modes	Duration	Current Derivative ($di_{s1}/dt + di_{s2}/dt$)	Current Characteristics	Active Switches
$0 < D < 1/2$	mode 1	$D_1 T$	$V_{pv}/L_{s1} + (V_{pv} - V_{01})/L_{s2}$	$i_{s1} \uparrow, i_{s2} \downarrow$	S_{s1}, D_{s2}
	mode 2	$(1 - 2D_1)T$	$(V_{pv} - V_{01})(1/L_{s1} + 1/L_{s2})$	$i_{s1} \downarrow, i_{s2} \downarrow$	D_{s1}, D_{s2}
	mode 3	$D_1 T$	$V_{pv}/L_{s2} + (V_{pv} - V_{01})/L_{s1}$	$i_{s1} \downarrow, i_{s2} \uparrow$	D_{s1}, S_{s2}
	Gain		$V_{01}/V_{pv} = 1/(1 - D_1)$		
$1/2 < D < 1$	mode 1	$(2D_1 - 1)T$	$V_{pv} \times (1/L_{s1} + 1/L_{s2})$	$i_{s1} \uparrow, i_{s2} \uparrow$	S_{s1}, S_{s2}
	mode 2	$(1 - D_1)T$	$V_{pv}/L_{s1} + (V_{pv} - V_{01})/L_{s2}$	$i_{s1} \uparrow, i_{s2} \downarrow$	S_{s1}, D_{s2}
	mode 3	$(1 - D_1)T$	$V_{pv}/L_{s2} + (V_{pv} - V_{01})/L_{s1}$	$i_{s1} \downarrow, i_{s2} \uparrow$	D_{s1}, S_{s2}
	Gain		$V_{01}/V_{pv} = 1/(1 - D_1)$		

5.3 Operating Principle of the Converter Under Ideal Conditions

5.3.1 State-I Operation

The block diagram of *state-I* is shown in Figure 5.3(a). In *state-I*, solar PV has generated surplus power compared to the load power demand at *output port 01* and *output port 02*. The system is considered with a 24V nominal battery voltage with 15V LVDC and 60V MVDC ports. It has six different modes of operation that are possible under a steady state. The switching logic waveforms with battery current characteristics and circuit operations for different modes are shown in Figure 5.5 and Figure 5.6, respectively. Both the input and battery sides interleaving of inductors are used. The corresponding gating pulses G_{Ss1} , G_{Ss2} and G_{Sbb1} , G_{Sb1} are 180° phase-shifted. The proposed converter consists of two legs, i.e., *leg-1* with three switches S_{b1} , S_{b2} , and S_{b3} , while *leg-2* with two switches S_{bb1} and S_{bb2} . With bidirectional power flow capability, the converter can seamlessly transfer energy between multiple sources and loads, enhancing system flexibility and energy efficiency. Furthermore, time multiplexing of the buck side switches optimizes converter performance while minimizing switching losses. It maintains both the DC-link bus voltages and performs battery charging with CCCV. The operation of the converter, the individual current characteristics, and the active switching states are summarized with respect to the active modes of operation in Table 5.2.

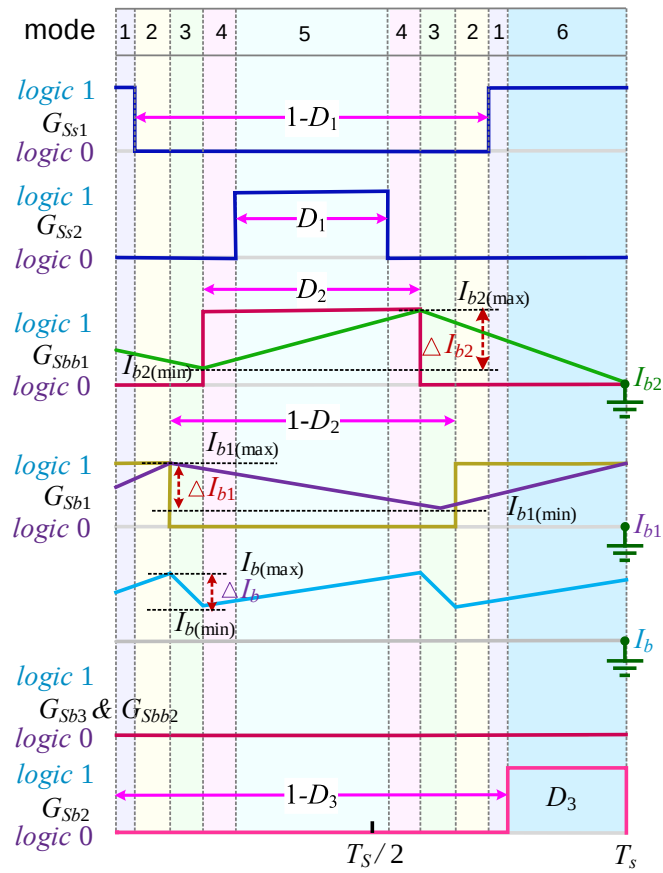
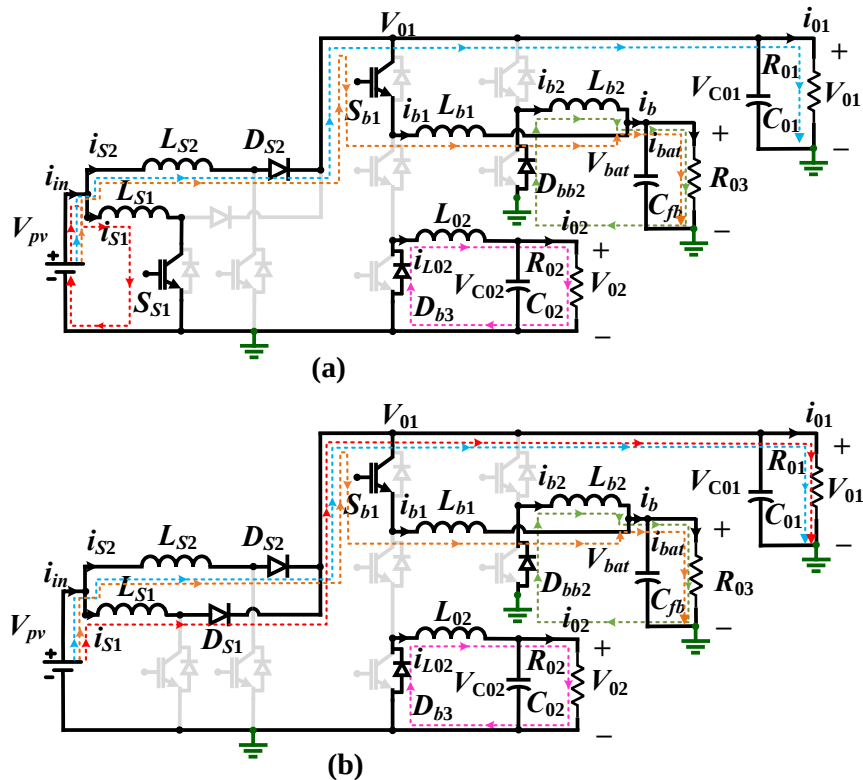


Figure 5.5 Switching and current characteristics for *state I* operation.



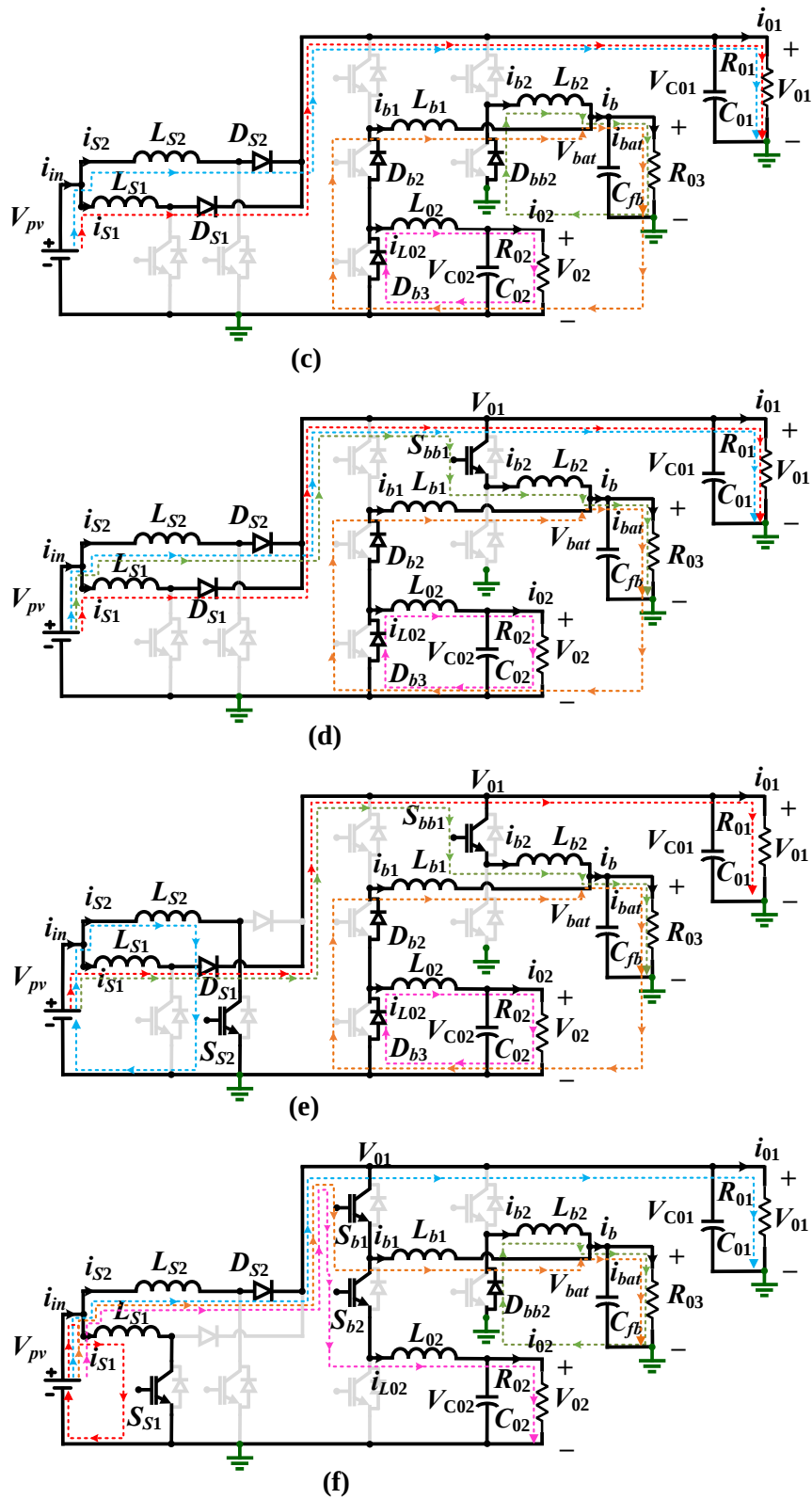


Figure 5.6 Equivalent circuits operation for *state-I* during (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5, and (f) mode 6.

Table 5.2
POSSIBLE MODES UNDER HEALTHY CONDITIONS DURING STATE-I & STATE-II

Modes	Duration	Current Characteristics	Active Switches
mode 1	$(D_1 - D_3) \times T$	$i_{s1} \uparrow, i_{s2} \downarrow, i_{b1} \uparrow, i_{L_{02}} \downarrow, i_{b2} \downarrow$	$S_{s1}, D_{s2}, S_{b1}, D_{b3}, D_{bb2}$
mode 2	$(D_2 - D_1) \times T$	$i_{s1} \downarrow, i_{s2} \downarrow, i_{b1} \uparrow, i_{L_{02}} \downarrow, i_{b2} \downarrow$	$D_{s1}, D_{s2}, S_{b1}, D_{b3}, D_{bb2}$
mode 3	$(1 - 2D_2) \times T$	$i_{s1} \downarrow, i_{s2} \downarrow, i_{b1} \downarrow, i_{L_{02}} \downarrow, i_{b2} \downarrow$	$D_{s1}, D_{s2}, D_{b2}, D_{b3}, D_{bb2}$
mode 4	$(D_2 - D_1) \times T$	$i_{s1} \downarrow, i_{s2} \downarrow, i_{b1} \downarrow, i_{L_{02}} \downarrow, i_{b2} \uparrow$	$D_{s1}, D_{s2}, D_{b2}, D_{b3}, S_{bb1}$
mode 5	$D_1 T$	$i_{s1} \downarrow, i_{s2} \uparrow, i_{b1} \downarrow, i_{L_{02}} \downarrow, i_{b2} \uparrow$	$D_{s1}, S_{s2}, D_{b2}, D_{b3}, S_{bb1}$
mode 6	$D_3 T$	$i_{s1} \uparrow, i_{s2} \downarrow, i_{b1} \uparrow, i_{L_{02}} \uparrow, i_{b2} \downarrow$	$S_{s1}, D_{s2}, S_{b1}, S_{b2}, D_{bb2}$

5.3.1.1 Steady-State Analysis

The steady-state voltage at output port 01 can be derived under CCM using volt-second balance across L_{s1} . The duty ratio D_1 is the optimized fraction of time from MPP control when S_{s1} is turned ON. Thus, the relation can be written for *state-I* operation of the proposed converter as follows:

$$V_{01} = \frac{V_{pv}}{1 - D_1} \quad (5.1)$$

Using volt-second balance across L_{b1} , voltage V_{bat} can be derived when S_{b1} is turned-on for $D_2 T$ time period, given as follows:

$$V_{bat} = V_{pv} \left(\frac{D_2}{1 - D_1} \right) \quad (5.2)$$

Using volt-second balance across L_{02} , voltage V_{02} can be derived when S_{b2} is turned-on for $D_3 T$ time period, given as follows:

$$V_{02} = V_{pv} \left(\frac{D_3}{1 - D_1} \right) \quad (5.3)$$

Using ampere-second balance and assuming the converter is lossless, the average values of currents during *state-I* at output port-2 ($i_{L_{02}avg|S-I}$), port-3 ($i_{bavg|S-I}$), and the input current (i.e., $i_{inavg|S-I} = i_{s1avg} + i_{s2avg}$) can be written as follows:

$$i_{L02_{avg}} \Big|_{S-I} = I_{02} = \left(\frac{D_3}{1-D_1} \right) \frac{V_{pv}}{R_{02}} \quad (5.4)$$

$$i_{b_{avg}} \Big|_{S-I} = i_{b1_{avg}} + i_{b2_{avg}} = \left(\frac{D_2}{1-D_1} \right) \frac{V_{pv}}{R_{03}} \quad (5.5)$$

$$i_{in_{avg}} \Big|_{S-I} = i_{S1_{avg}} + i_{S2_{avg}} = \frac{i_{01_{avg}} + D_2 i_{b_{avg}} + D_3 i_{L02_{avg}}}{1-D_1}, \quad (5.6)$$

$$\text{where, } i_{01_{avg}} = \frac{V_{01}}{R_{01}}.$$

5.3.1.2 Characterization of Current Ripple

The value of input current ripple can be calculated with respect to interleaved inductor currents as follows:

$$\Delta i_{S1} \Big|_{charging} = \left| \frac{V_{pv} D_1 T}{L_{S1}} \right|, \quad \Delta i_{S2} \Big|_{discharging} = \left| \frac{-V_{pv} D_1 T}{L_{S2}} \right| \quad (5.7)$$

$$K_{L1} = D_1 T V_{pv} \left(\frac{1}{\min(L_{S1}, L_{S2})} - \frac{1}{\max(L_{S1}, L_{S2})} \right) \quad (5.8a)$$

$$K_{D1} = \begin{cases} \left(\frac{1-2D_1}{1-D_1} \right) \frac{D_1 T V_{PV}}{\max(L_{S1}, L_{S2})} & \forall D_1 < 0.5 \\ \frac{(2D_1-1) T V_{PV}}{\max(L_{S1}, L_{S2})} & \forall D_1 \geq 0.5 \end{cases} \quad (5.8b)$$

$$\Delta i_{in} = K_{L1} + K_{D1} \quad (5.8c)$$

where K_{Lj} and K_{Dj} are the ripple current magnitude at different switching states and at the same switching states of interleaved branch semiconductor devices, considering one switching state transition, respectively, where $j = 1, 2, \dots, 5$.

The value of the current ripple at the output ports 3 and 2 can be calculated as follows:

$$\Delta i_{b1} \Big|_{charging} = \frac{(V_{01} - V_{bat}) D_2 T}{L_{b1}} = \left(\frac{1-D_2}{1-D_1} \right) \left(\frac{V_{pv}}{L_{b1}} \right) D_2 T \quad (5.9a)$$

$$\Delta i_{b2}|_{discharging} = \frac{-V_{bat}(1-D_2)T}{L_{b2}} = -\left(\frac{1-D_2}{1-D_1}\right)\left(\frac{V_{pv}}{L_{b2}}\right)D_2T \quad (5.9b)$$

$$K_{L2} = D_2TV_{pv}\left(\frac{1-D_2}{1-D_1}\right)\left(\frac{1}{\min(L_{b1}, L_{b2})} - \frac{1}{\max(L_{b1}, L_{b2})}\right) \quad (5.10a)$$

$$K_{D2} = \begin{cases} \left(\frac{1-2D_2}{1-D_1}\right)\frac{D_2TV_{pv}}{\max(L_{b1}, L_{b2})} & \forall D_2 < 0.5 \\ \left(\frac{1-D_2}{1-D_1}\right)\frac{(2D_2-1)TV_{pv}}{\max(L_{b1}, L_{b2})} & \forall D_2 \geq 0.5 \end{cases} \quad (5.10b)$$

$$\Delta i_b = K_{L2} + K_{D2} \quad (5.10c)$$

$$\Delta i_{L_{02}} = \left|\frac{V_{01}-V_{02}}{L_{02}}D_3T\right| = \left|\frac{V_{pv}D_3T}{L_{02}}\left(\frac{1-D_3}{1-D_1}\right)\right| \quad (5.11)$$

From (5.8c) and (5.10c), it can be seen that the input current ripple and the battery-side input current ripple depend on D_1 and D_2 . The relation of K_{D1} and K_{D2} also depends on the range of the respective duty. By selecting identical values for the interleaving inductors L_{S1} , L_{S2} , and L_{b1} , L_{b2} , the values of K_{L1} and K_{L2} become zero. Figure 5.7 is plotted with consideration of identical values of inductors L_{S1} , L_{S2} , and using (5.7) and (5.8). Figure 5.7(a) shows the input current ripple (Δi_{in}) with respect to D_1 with and without the interleaved branch. In this scenario, the boost-side output voltage (V_{01}) is kept constant at 60V. With interleaving on the boost side, the Δi_{in} reduces to zero at duty $D_1 = 0.5$. Figure 5.7(b) shows the Δi_{in} with respect to the D_1 with and without interleaving while maintaining a constant input voltage of 40V. The plot indicates that the Δi_{in} reaches zero (minimum) when $D_1 = 0.5$, and it also shows that as $D_1 \geq 0.5$, the Δi_{in} rises but significantly less than without the interleaved branch.

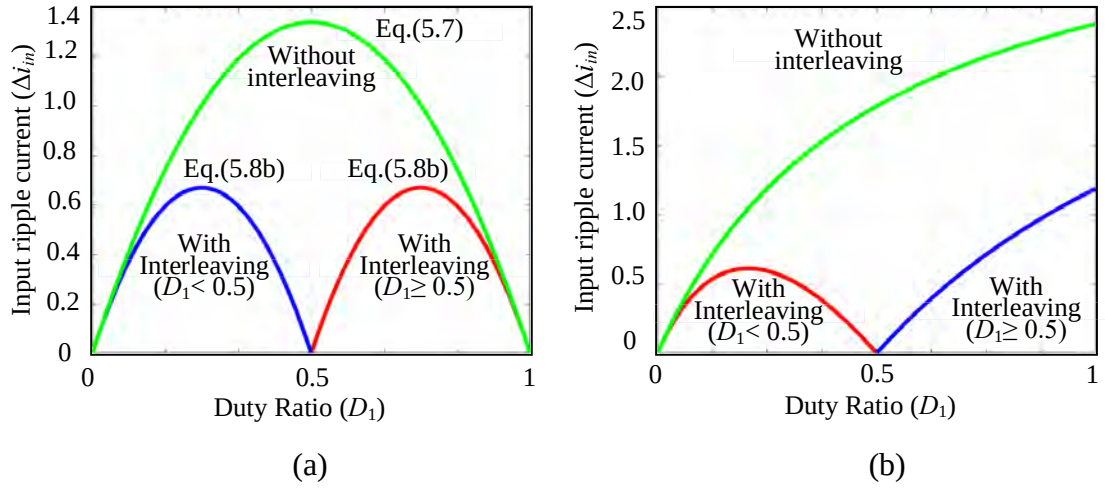


Figure 5.7 Input ripple current (Δi_{in}) with respect to change in the duty D_1 with (a) constant output voltage and (b) constant input voltage.

5.3.1.3 Small-Signal Stability Analysis

With the consideration of the same inductance in each corresponding interleaved branch, the phase-shifted duty with identical width is used, and a generalized reduced-order model for the n -phase interleaved converter can be derived with respect to the following:

$$L_{seq} \frac{di_{in}}{dt} = v_{pv} - (1 - D_1)v_{01}, \quad (\text{solar PV side converter}) \quad (5.12a)$$

$$L_{beq} \frac{di_{bat}}{dt} = D_2 v_{01} - v_{bat}, \quad (\text{battery side converter}) \quad (5.12b)$$

$$\text{where, } i_{in} = \sum_{i=1}^n i_{si}, \quad i_b = \sum_{i=1}^n i_{bi}; \quad (5.13)$$

$$\frac{1}{L_{seq}} = \sum_{i=1}^n \frac{1}{L_{si}}, \quad \frac{1}{L_{beq}} = \sum_{i=1}^n \frac{1}{L_{bi}}.$$

The state space representation for each *state* has been presented in Appendix (A.3). Whereas, the small-signal transfer functions of the converters are obtained by applying small perturbations to the output voltages ($\hat{v}_{c01}$, $\hat{v}_{c02}$, $\hat{v}_{bat}$), input voltage ($\hat{v}_{pv}$), input current ($\hat{i}_{in}$), battery current ($\hat{i}_b$), LVDC load currents ($\hat{i}_{L02}$), and corresponding duty ratio ($\hat{d}_1$, $\hat{d}_2$, $\hat{d}_3$) around their steady-state operating points. The state variable and input variable are defined as in (5.14). Further taking the value of the system parameters given in Table 5.3 and the steady-state values that occurred in the

experimental results, such as duty ratio, respective currents, voltages, and load resistances, are taken as $D_1 = 0.33$, $D_2 = 0.438$, $D_3 = 0.25$, $I_{in} = 1.74\text{A}$, $I_b = 1.05\text{A}$, $I_{L02} = 0.333\text{A}$, $V_{01} = 60\text{V}$, $V_{bat} = 26.3\text{V}$, $V_{02} = 15\text{V}$, and $R_{01} = 100\Omega$, $R_{02} = 45\Omega$, $R_{03} = 25\Omega$, respectively. The small signal open-loop transfer function (*SSOLTF*) can be derived as [17], [122], [129] and written below as (5.15a), (5.15b), and (5.15c).

$$\hat{x}_1(t) = \begin{bmatrix} \hat{i}_{in} & \hat{i}_b & \hat{i}_{L02} & \hat{v}_{c01} & \hat{v}_{c02} & \hat{v}_{bat} \end{bmatrix}^T, \quad \hat{u}_1(t) = \hat{v}_{pv} \quad (5.14)$$

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_1} \right|_{\hat{v}_{pv}, \hat{d}_2, \hat{d}_3=0} = \frac{-1582s^5 + 1.233 \times 10^8 s^4 - 3.354 \times 10^{10} s^3 + 4.763 \times 10^{16} s^2 + 9.86 \times 10^{18} s + 4.641 \times 10^{23}}{s^6 + 4231s^5 + 3.702 \times 10^8 s^4 + 1.317 \times 10^{11} s^3 + 4.131 \times 10^{15} s^2 + 2.343 \times 10^{17} s + 5.159 \times 10^{21}} \quad (5.15a)$$

$$\left. \frac{\hat{v}_{c02}(s)}{\hat{d}_3} \right|_{\hat{v}_{pv}, \hat{d}_1, \hat{d}_2=0} = \frac{6 \times 10^8 s^4 + 2.405 \times 10^{12} s^3 + 2.155 \times 10^{17} s^2 + 6.639 \times 10^{18} s + 3.095 \times 10^{23}}{s^6 + 4231s^5 + 3.702 \times 10^8 s^4 + 1.317 \times 10^{11} s^3 + 4.131 \times 10^{15} s^2 + 2.343 \times 10^{17} s + 5.159 \times 10^{21}} \quad (5.15b)$$

$$\left. \frac{\hat{v}_{bat}(s)}{\hat{d}_2} \right|_{\hat{v}_{pv}, \hat{d}_1, \hat{d}_3=0} = \frac{2.143 \times 10^{10} s^4 + 4.807 \times 10^{12} s^3 + 2.465 \times 10^{17} s^2 + 7.603 \times 10^{18} s + 3.095 \times 10^{23}}{s^6 + 4231s^5 + 3.702 \times 10^8 s^4 + 1.317 \times 10^{11} s^3 + 4.131 \times 10^{15} s^2 + 2.343 \times 10^{17} s + 5.159 \times 10^{21}} \quad (5.15c)$$

Table 5.3
SYSTEM SPECIFICATIONS

Parameters		Designed Values	Mathematical Relations Used / Remarks	Values Used
DC bus voltages (V_{01} / V_{02})		Selected for 3-wheeler application		60V / 15V
Battery Voltage (V_{bat}) / Capacity (Ah)		--		24V / 8Ah
Inductors	L_{s1} / L_{s2}	566 μH	(5.7), $\Delta i_{s1} = \Delta i_{s2} = 1.4\text{A}$, Figure 5.17	560 μH
	L_{b1} / L_{b2}	533 μH	(5.9), $\Delta i_{b1} = 1.4\text{A}$, Figure 5.17	560 μH
	L_{02}	950 μH	(5.11), $\Delta i_{L02} = 0.6\text{A}$	1.0 mH
Capacitors	C_{pv}	99.2 μF	(5.42), $\zeta = 0.06$ and $R_{mpp} = 14\Omega$	100 μF
	C_{01}	226 μF	$i_{01\text{avg}} = 4\text{A}$, $\Delta v_{C01} = 0.5\%$ of 60V	220 μF
	C_{fb}	22.8 μF	$i_{b\text{avg}} = 1\text{A}$, $\Delta v_{Cfb} = 4\%$ of 24V	22 μF
	C_{02}	83.38 μF	$i_{02\text{avg}} = 1\text{A}$, $\Delta v_{C02} = 1\%$ of 15V	100 μF
Switching frequency		--		20kHz

5.3.2 State-II Operation

The block diagram of *state-II* is shown in Figure 5.3(b). During *state-II*, the load at output port 01 is disconnected, and the solar PV-side converter operates either in MPP mode (if battery SoC < 100%) or in load power reference mode (LPRM). The solar PV supplies its energy to the remaining two output ports, i.e., output ports 02 and 03. The FPFTDC operates as a single-input dual-output (SIDO) converter. It has six modes, as shown in Table 5.2 above. The modes of operation are similar to *state-I* operation, and the auxiliary load and the battery share the power generated by PV.

5.3.2.1 Steady-State Analysis

The steady-state voltage conversion ratio for all the outputs is similar as *state I*, except the average current across the circuit ($i_{inavg}|_{S-II}$) changes, which is given as follows:

$$i_{inavg}|_{S-II} = i_{S1avg} + i_{S2avg} = \frac{1}{1-D_1} \left(D_2 i_{bavg} + D_3 i_{L02avg} \right) \quad (5.16)$$

5.3.2.2 Small-Signal Stability Analysis

In this *state* of operation, the MVDC load is disconnected, resulting in a decrease in the steady-state current. The remaining constraints are similar to the *state-I* of the dynamic model. The *SSOLTF* can be derived as (5.17a), (5.17b), and (5.17c).

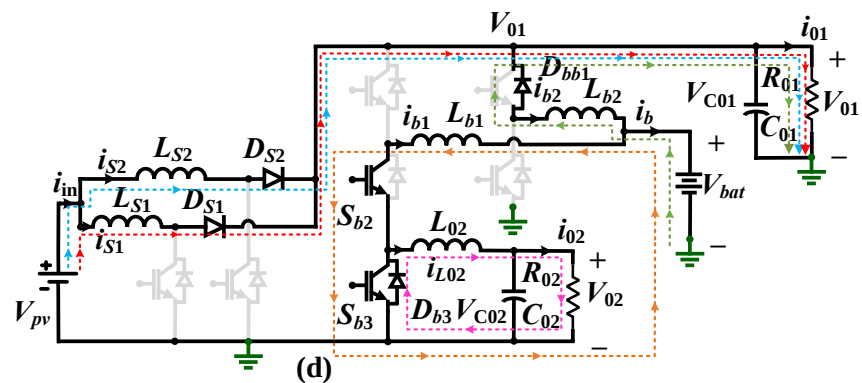
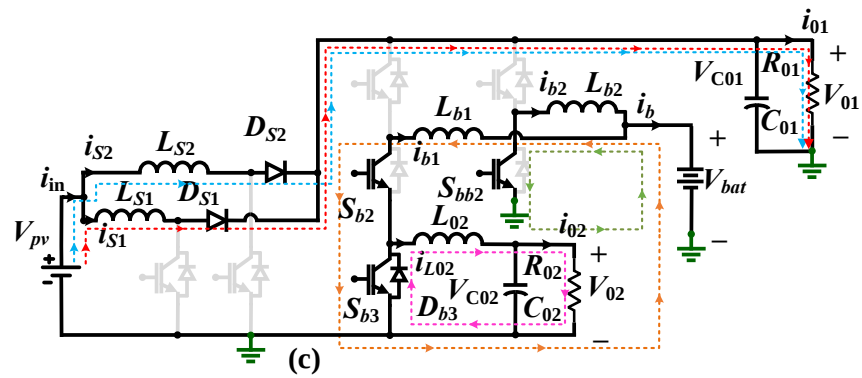
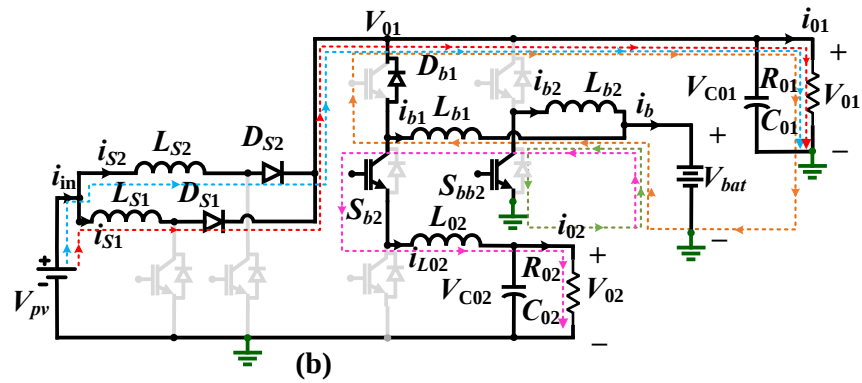
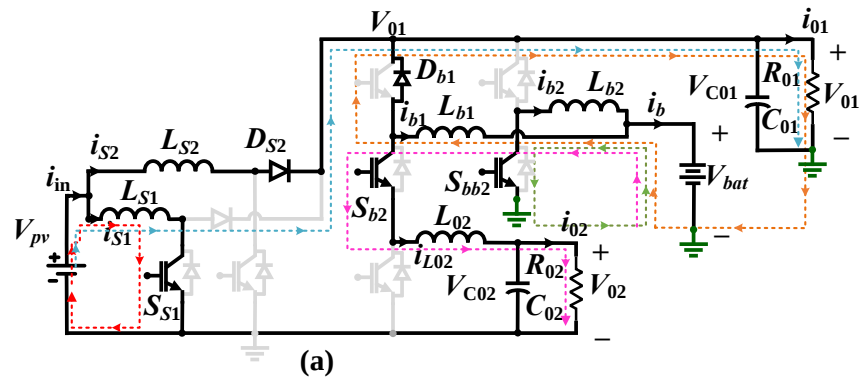
$$\frac{\hat{v}_{c01}(s)}{\hat{d}_1} \bigg|_{\hat{v}_{pv}, \hat{d}_2, \hat{d}_3=0} = \frac{-1073s^5 + 1.254 \times 10^8 s^4 + 1.538 \times 10^{11} s^3 + 4.769 \times 10^{16} s^2 + 1.168 \times 10^{19} s + 4.641 \times 10^{23}}{s^6 + 4222s^5 + 3.702 \times 10^8 s^4 + 1.283 \times 10^{11} s^3 + 4.13 \times 10^{15} s^2 + 2.018 \times 10^{17} s + 5.159 \times 10^{21}} \quad (5.17a)$$

$$\frac{\hat{v}_{c02}(s)}{\hat{d}_3} \bigg|_{\hat{v}_{pv}, \hat{d}_1, \hat{d}_2=0} = \frac{6 \times 10^8 s^4 + 2.399 \times 10^{12} s^3 + 2.155 \times 10^{17} s^2 + 4.691 \times 10^{18} s + 3.095 \times 10^{23}}{s^6 + 4222s^5 + 3.702 \times 10^8 s^4 + 1.283 \times 10^{11} s^3 + 4.13 \times 10^{15} s^2 + 2.018 \times 10^{17} s + 5.159 \times 10^{21}} \quad (5.17b)$$

$$\frac{\hat{v}_{bat}(s)}{\hat{d}_2} \bigg|_{\hat{v}_{pv}, \hat{d}_1, \hat{d}_3=0} = \frac{2.143 \times 10^{10} s^4 + 4.733 \times 10^{12} s^3 + 2.464 \times 10^{17} s^2 + 6.864 \times 10^{18} s + 3.095 \times 10^{23}}{s^6 + 4222s^5 + 3.702 \times 10^8 s^4 + 1.283 \times 10^{11} s^3 + 4.13 \times 10^{15} s^2 + 2.018 \times 10^{17} s + 5.159 \times 10^{21}} \quad (5.17c)$$

The block diagram of *state*-III is shown in Figure 5.3(c). Solar PV power decreases due to any of the following conditions: partial shading, clouds, buildings, trees, or dust. It can destabilize the DC-bus voltage. During this condition, the battery maintains the DC-bus voltage, and the PWM signals to S_{b1} and S_{bb1} are removed. This case serves a similar dual-input and dual-output (DIDO) condition, where the solar and the battery act as inputs, and output ports 01 and 02 are the outputs. In *state*-III, a total of six modes is possible as shown in the steady-state waveforms, presented in Figure 5.8. All the six modes and their operation principle are depicted in Figure 5.9, and the current characteristics are summarized in Table 5.4.





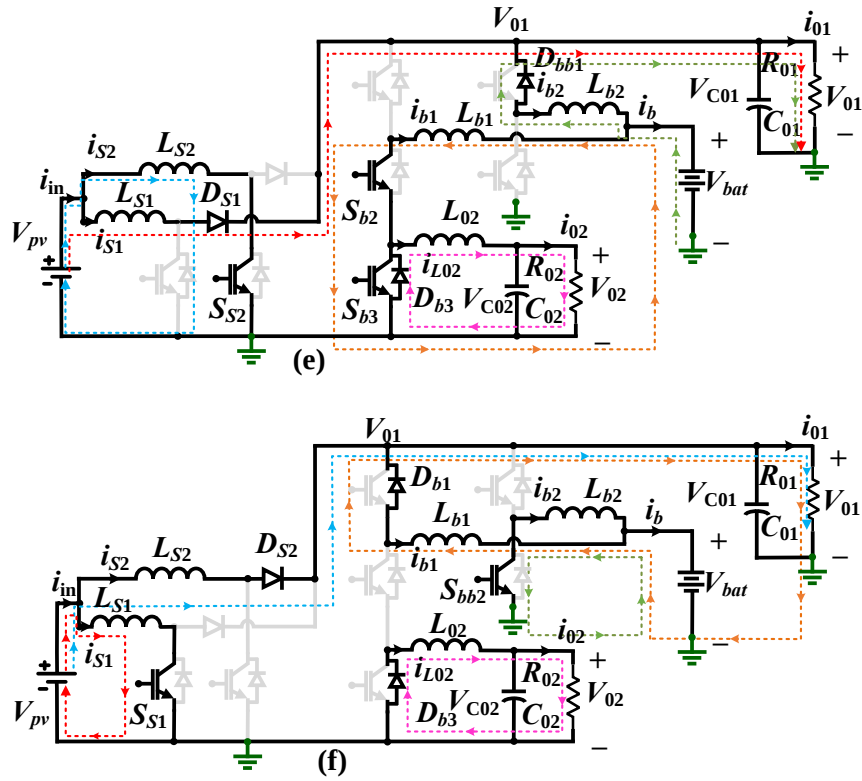


Figure 5.9 Equivalent circuits operation for *state-III* during (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5, and (f) mode 6.

Table 5.4
POSSIBLE MODES UNDER HEALTHY CONDITIONS DURING STATE-III

Modes	Duration	Current Characteristics	Active Switches
mode 1	$(D_1 + D_3 - 1) \times T$	$i_{s1} \uparrow, i_{s2} \downarrow, i_{b1} \downarrow, i_{L02} \uparrow, i_{b2} \uparrow$	$S_{s1}, D_{s2}, S_{b2}, S_{bb2}, D_{b1}$
mode 2	$(1 - D_1 - D_2) \times T$	$i_{s1} \downarrow, i_{s2} \downarrow, i_{b1} \downarrow, i_{L02} \uparrow, i_{b2} \uparrow$	$D_{s1}, D_{s2}, S_{b2}, S_{bb2}, D_{b1}$
mode 3	$(2D_2 - 1) \times T$	$i_{s1} \downarrow, i_{s2} \downarrow, i_{b1} \uparrow, i_{L02} \downarrow, i_{b2} \uparrow$	$D_{s1}, D_{s2}, S_{b2}, S_{b3}, S_{bb2}$
mode 4	$(1 - D_1 - D_2) \times T$	$i_{s1} \downarrow, i_{s2} \downarrow, i_{b1} \uparrow, i_{L02} \downarrow, i_{b2} \downarrow$	$D_{s1}, D_{s2}, S_{b2}, S_{b3}, D_{bb1}$
mode 5	$D_1 T$	$i_{s1} \downarrow, i_{s2} \uparrow, i_{b1} \uparrow, i_{L02} \downarrow, i_{b2} \downarrow$	$S_{s2}, D_{s1}, S_{b2}, S_{b3}, D_{bb1}$
mode 6	$(1 - D_3) \times T$	$i_{s1} \uparrow, i_{s2} \downarrow, i_{b1} \downarrow, i_{L02} \downarrow, i_{b2} \uparrow$	$D_{s2}, S_{s1}, D_{b1}, D_{b3}, S_{bb2}$

5.3.3.1 Steady-State Analysis

The steady-state voltage at output port 01 can be derived under CCM using volt-second balance across L_{S1} . The relation can be written for *state-III* operation of the proposed converter as follows:

$$V_{01} = \frac{V_{pv}}{1-D_1} = \frac{V_{bat}}{1-D_2} \quad (5.18)$$

Using volt-second balance across L_{02} , the voltage V_{02} can be derived as follows:

$$V_{02} = \left(\frac{D_3 - D_2}{1 - D_1} \right) V_{pv} = \left(\frac{D_3 - D_2}{1 - D_2} \right) V_{bat} \quad (5.19)$$

Using ampere-second balance and assuming the converter is lossless, the average values of currents during *state-III* at output port-2 ($i_{L02avg}|_{S-III}$) can be written as follows:

$$i_{L02avg}|_{S-III} = I_{02} = \left(\frac{D_3 - D_2}{1 - D_1} \right) \frac{V_{pv}}{R_{02}} = \left(\frac{D_3 - D_2}{1 - D_2} \right) \frac{V_{bat}}{R_{02}} \quad (5.20)$$

5.3.3.2 Characterization of Current Ripple

The value of the current ripple at the output ports 3 and 2 can be calculated as follows:

$$\Delta i_{b1}|_{charging} = \frac{(V_{01} - V_{bat})}{L_{b1}} \times D_2 T = \left(\frac{V_{bat}}{L_{b1}} \right) \frac{D_2^2}{(1 - D_2)} T \quad (5.21a)$$

$$\Delta i_{b2}|_{discharging} = - \left(\frac{V_{bat}}{L_{b2}} \right) (1 - D_2) T \quad (5.21b)$$

$$K_{L3} = V_{bat} T \left(\frac{2D_2 - 1}{1 - D_2} \right) \left(\frac{1}{\min(L_{b1}, L_{b2})} - \frac{1}{\max(L_{b1}, L_{b2})} \right) \quad (5.22a)$$

$$K_{D3} = \begin{cases} \left(\frac{1 - D_2}{D_2} \right) \frac{(1 - 2D_2) V_{bat} T}{\max(L_{b1}, L_{b2})} & \forall D_2 < 0.5 \\ (2D_2 - 1) \frac{V_{bat} T}{\max(L_{b1}, L_{b2})} & \forall D_2 \geq 0.5 \end{cases} \quad (5.22b)$$

$$\Delta i_b = K_{L3} + K_{D3} \quad (5.22c)$$

$$\Delta i_{L02} = \left| \frac{V_{bat} T (D_3 - D_2)}{L_{02}} \left(\frac{1 - D_3 + D_2}{1 - D_2} \right) \right| \quad (5.23)$$

5.3.3.3 Small-Signal Stability Analysis

In this *state* of operation, the PV and the battery act as an input source, and the system order is reduced to five. The perturbed state variables in *state*-III are $\hat{i}_{in}, \hat{i}_b, \hat{i}_{L02}, \hat{v}_{c01}, \hat{v}_{c02}$. Since this state operates under load sharing, the steady-state values of the duty ratio, current, and voltage change based on the available solar PV power to maintain constant power to all loads. An experimental case is considered for analysis, and the steady-state values are $D_1 = 0.33$, $D_2 = 0.706$, $D_3 = 0.956$, $I_{in} = 1.18A$, $I_b = -1.074A$, and $V_{bat} = 17.6V$. The *SSOLTF* can be derived as (5.24a), (5.24b), and (5.24c).

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_1} \right|_{\hat{v}_{pv}, \hat{v}_{bat}, \hat{d}_2, \hat{d}_3=0} = \frac{-500s^4 + 1.298 \times 10^8 s^3 + 2.387 \times 10^{10} s^2 + 1.299 \times 10^{15} s + 443.5}{s^5 + 231.3s^4 + 1.178 \times 10^7 s^3 + 4.869 \times 10^8 s^2 + 1.725 \times 10^{13} s + 0.1053} \quad (5.24a)$$

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_2} \right|_{\hat{v}_{pv}, \hat{v}_{bat}, \hat{d}_1, \hat{d}_3=0} = \frac{-673.6s^4 + 7.076 \times 10^7 s^3 + 9.021 \times 10^9 s^2 + 5.727 \times 10^{14} s - 46.96}{s^5 + 231.3s^4 + 1.178 \times 10^7 s^3 + 4.869 \times 10^8 s^2 + 1.725 \times 10^{13} s + 0.1053} \quad (5.24b)$$

$$\left. \frac{\hat{v}_{c02}(s)}{\hat{d}_3} \right|_{\hat{v}_{pv}, \hat{v}_{bat}, \hat{d}_1, \hat{d}_2=0} = \frac{6 \times 10^8 s^3 + 3.45 \times 10^9 s^2 + 1.838 \times 10^{15} s + 139.3}{s^5 + 231.3s^4 + 1.346 \times 10^7 s^3 + 8.601 \times 10^8 s^2 + 3.063 \times 10^{13} s - 0.1912} \quad (5.24c)$$

5.3.4 State-IV Operation

The block diagram of *state*-IV is shown in Figure 5.3(d). In this *state*, solar insolation is unavailable, and therefore, the value of solar PV-generated power, PSPV, is 0. The battery maintains the DC-bus voltage and delivers power to the loads connected at the MVDC and LVDC output ports. This case is under SIDO, and the battery serves as a source. In *state*-IV, a total of four modes is possible, as shown in the steady-state waveforms presented in Figure 5.10. All four modes and their operation principle are depicted in Figure 5.11, and the current characteristics are summarized in Table 5.5.

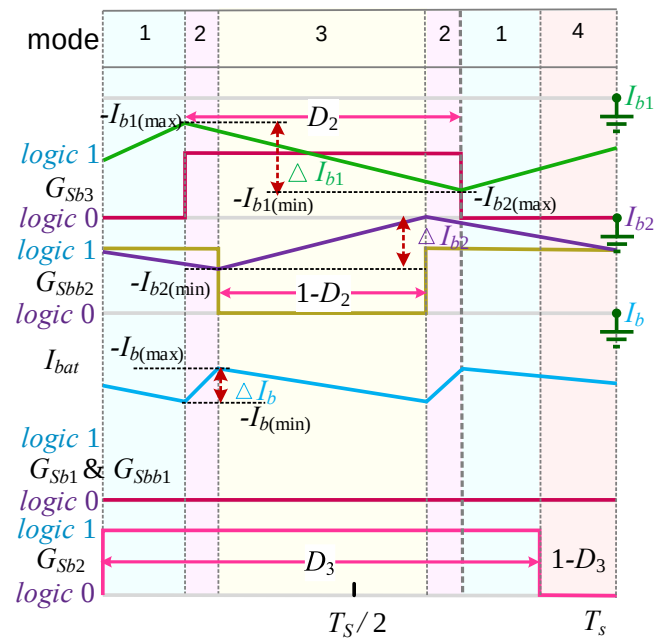
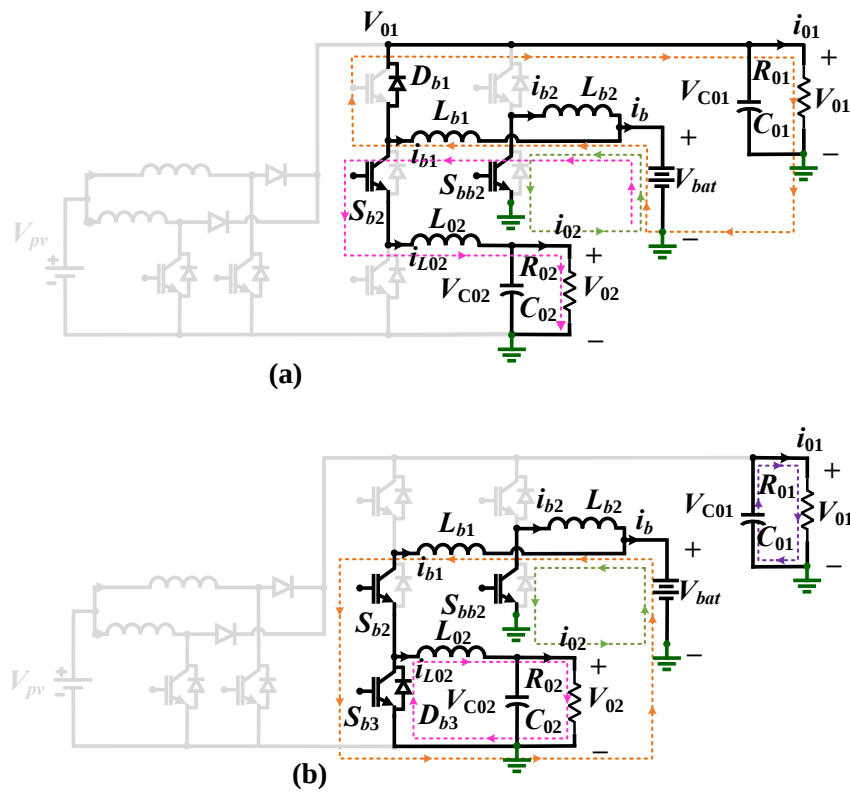


Figure 5.10 Switching and current characteristics for *state-IV* operation.



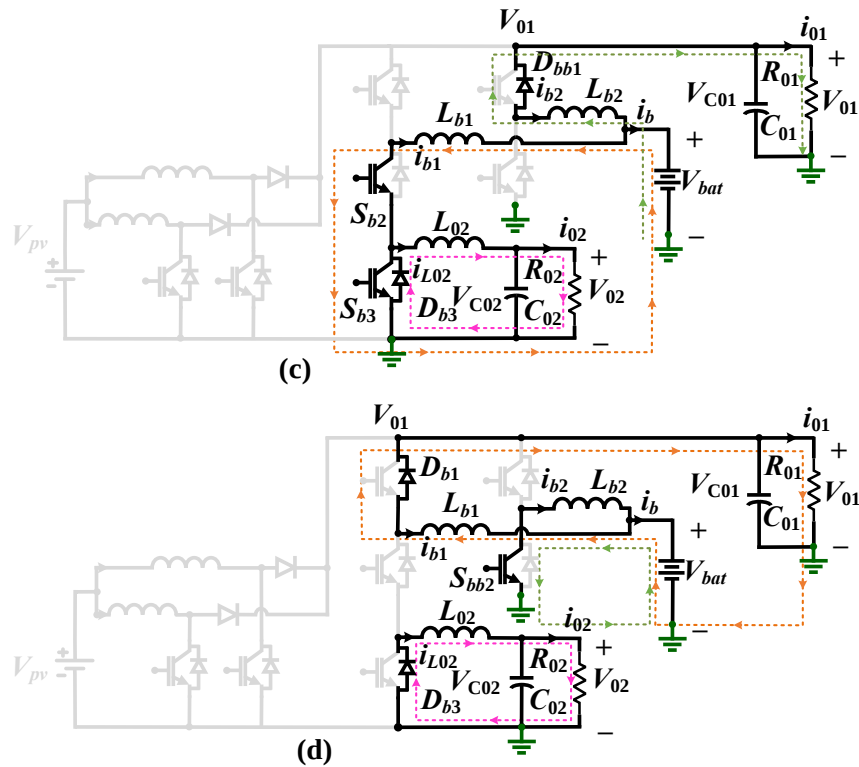


Figure 5.11 Equivalent circuits operation for *state-IV* during (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

Table 5.5

POSSIBLE MODES UNDER HEALTHY CONDITIONS DURING STATE-IV

Modes	Duration	Current Characteristics	Active Switches
mode 1	$(D_3 - D_2) \times T$	$i_{b1} \downarrow, i_{L_{02}} \uparrow, i_{b2} \uparrow$	D_{b1}, S_{b2}, S_{bb2}
mode 2	$(2D_2 - 1) \times T$	$i_{b1} \uparrow, i_{L_{02}} \downarrow, i_{b2} \uparrow$	S_{b2}, S_{b3}, S_{bb2}
mode 3	$(1 - D_2) \times T$	$i_{b1} \uparrow, i_{L_{02}} \downarrow, i_{b2} \downarrow$	S_{b2}, S_{b3}, D_{bb1}
mode 4	$(1 - D_3) \times T$	$i_{b1} \downarrow, i_{L_{02}} \downarrow, i_{b2} \uparrow$	D_{b1}, D_{b3}, S_{bb2}

5.3.4.1 Steady-State Analysis

The steady-state voltage at the output port 01 can be derived in CCM using the volt-second balance across L_{b1} . The battery behaves as a source during *state-IV*. Thus, the relation can be written for the output voltage at the MVDC port of the proposed converter as follows:

$$V_{01} = \frac{V_{bat}}{1 - D_2} \quad (5.25)$$

Using volt-second balance across L_{02} , the voltage at auxiliary load buck output voltage can be written as follows:

$$V_{02} = \left(\frac{D_3 - D_2}{1 - D_2} \right) V_{bat} \quad (5.26)$$

Using the ampere-second balance and assuming the converter is lossless, the average values of current during *state-IV* at output port-2 ($i_{L02avg}|_{S-IV}$) can be written as follows:

$$i_{L02avg}|_{S-IV} = I_{02} = \left(\frac{D_3 - D_2}{1 - D_2} \right) \frac{V_{bat}}{R_{02}} \quad (5.27)$$

5.3.4.2 Characterization of Current Ripple

The value of battery current ripple can be calculated with respect to the change in interleaved inductor currents i_{b1} and i_{b2} as follows:

$$\Delta i_{b1}|_{charging} = \frac{-V_{bat}}{L_{b1}} \times D_2 T \quad (5.28a)$$

$$\Delta i_{b2}|_{discharging} = \frac{V_{01} - V_{bat}}{L_{b2}} \times (1 - D_2) T = \left(\frac{V_{bat}}{L_{b2}} \right) D_2 T \quad (5.28b)$$

$$K_{L4} = D_2 V_{bat} T \left(\frac{1}{\min(L_{b1}, L_{b2})} - \frac{1}{\max(L_{b1}, L_{b2})} \right) \quad (5.29a)$$

$$\Delta i_b = K_{L4} + K_{D3} \quad (5.29b)$$

The value of current ripple at the port connected with auxiliary loads is given as follows:

$$\Delta i_{L02} = \left| \frac{V_{01} - V_{02}}{L_{02}} \times (D_3 - D_2) T \right| = \left| \frac{V_{bat} T}{L_{02}} \left(\frac{1 - (D_3 - D_2)}{1 - D_2} \right) \right| \quad (5.30)$$

5.3.4.3 Small-Signal Stability Analysis

In this *state* of operation, only the battery serves as an input source, i.e., PSPV = 0; hence, the system order is reduced to four. The perturbed state variables in *state-III* are $\hat{i}_b, \hat{i}_{L02}, \hat{v}_{c01}, \hat{v}_{c02}$. An experimental case is considered for the analysis, and the steady-state values are $D_2=0.5967$, $D_3=0.8467$, $I_{in}=1.08A$, $I_b=-1.6945A$, and $V_{bat}=24.2V$, respectively. The *SSOLTF* can be derived as (5.31a) and (5.31b).

$$\left. \begin{array}{l} \hat{v}_{c01}(s) \\ \hat{d}_2 \end{array} \right|_{\hat{v}_{bat}, \hat{d}_3=0} = \frac{-1238s^3 + 9.193 \times 10^7 s^2 + 8.112 \times 10^9 s + 7.856 \times 10^{14}}{s^4 + 231.3s^3 + 1.059 \times 10^7 s^2 + 2.209 \times 10^8 s + 5.281 \times 10^{12}} \quad (5.31a)$$

$$\left. \begin{array}{l} \hat{v}_{c02}(s) \\ \hat{d}_3 \end{array} \right|_{\hat{v}_{bat}, \hat{d}_2=0} = \frac{6 \times 10^8 s^2 + 4.698 \times 10^9 s + 3.169 \times 10^{14}}{s^4 + 231.3s^3 + 1.059 \times 10^7 s^2 + 2.209 \times 10^8 s + 5.281 \times 10^{12}} \quad (5.31b)$$

5.3.5 State-V Operation

The block diagram of *state-V* is shown in Figure 5.3(e). During regenerative braking, the motor acts as a generator, and the converter can supply regenerative power to the BES, enabling bidirectional operation of the FPFTDC and improving system efficiency compared to the unidirectional feature of the conventional converter topology. During *state-V*, the energy transfer period during regenerative braking is very small, and therefore, power transfer from solar PV during this state is negligible. The steady-state key waveforms are shown in Figure 5.12, along with the battery ripple current analysis. The active switches and current characteristics are presented in Table 5.6. This state also supports battery charging in CCCV, and there are four modes in this state.

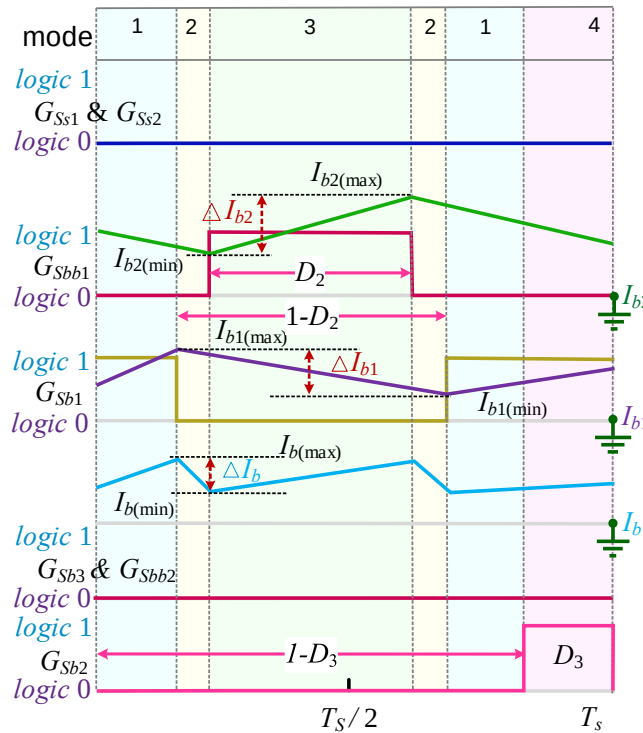


Figure 5.12 Switching and current characteristics for *state-V* operation

Table 5.6
POSSIBLE MODES UNDER HEALTHY CONDITIONS DURING STATE-V

Modes	Duration	Current Characteristics	Active Switches
mode 1	$(D_2 - D_3) \times T$	$i_{b1} \uparrow, i_{L02} \downarrow, i_{b2} \downarrow$	S_{b1}, D_{b3}, D_{bb2}
mode 2	$(1 - 2D_2) \times T$	$i_{b1} \downarrow, i_{L02} \downarrow, i_{b2} \downarrow$	D_{b2}, D_{b3}, D_{bb2}
mode 3	$D_2 T$	$i_{b1} \downarrow, i_{L02} \downarrow, i_{b2} \uparrow$	D_{b2}, D_{b3}, S_{bb1}
mode 4	$D_3 T$	$i_{b1} \uparrow, i_{L02} \uparrow, i_{b2} \downarrow$	S_{b1}, S_{b2}, D_{bb2}

5.3.5.1 Steady-State Analysis

The steady-state voltages at the output ports 03 and 02 can be derived in CCM using the volt-second balance across L_{b1} and L_{02} , respectively. During regenerative braking, output port 01 acts as a source. Thus, the output voltage at output port 03 and port 02 of the FPFTDC converter can be written as follows:

$$V_{bat} = D_2 \times V_{01}; \quad V_{02} = D_3 \times V_{01} \quad (5.32)$$

Using the ampere-second balance and assuming the converter is lossless, the average values of current during *state-V* at output port-2 ($i_{L02avg}|_{S-V}$) can be written as follows:

$$i_{L02avg}|_{S-V} = I_{02} = \frac{D_3 V_{01}}{R_{02}} \quad (5.33)$$

5.3.5.2 Characterization of Current Ripple

The value of battery current ripple can be calculated with respect to the change in interleaved inductor currents i_{b1} and i_{b2} as follows:

$$\Delta i_{b1}|_{charging} = \frac{V_{01} - V_{bat}}{L_{b1}} \times D_2 T = \frac{(1 - D_2) D_2 T V_{01}}{L_{b1}} \quad (5.34a)$$

$$\Delta i_{b2}|_{discharging} = \frac{-V_{bat}}{L_{b2}} \times (1 - D_2) T = -\frac{(1 - D_2) D_2 T V_{01}}{L_{b2}} \quad (5.34b)$$

$$K_{L5} = (1 - D_2) T V_{01} \left(\frac{1}{\min(L_{b1}, L_{b2})} - \frac{1}{\max(L_{b1}, L_{b2})} \right) \quad (5.35a)$$

$$K_{D5} = \begin{cases} (1-2D_2) \frac{D_2 TV_{01}}{\max(L_{b1}, L_{b2})} & \forall D_2 < 0.5 \\ (2D_2 - 1) \frac{(1-D_2) TV_{01}}{\max(L_{b1}, L_{b2})} & \forall D_2 \geq 0.5 \end{cases} \quad (5.35b)$$

$$\Delta i_b = K_{L5} + K_{D5} \quad (5.36)$$

The value of the current ripple at the port connected with auxiliary loads is given as follows:

$$\Delta i_{L_{02}} = \left| \frac{V_{01} - V_{02}}{L_{02}} \times D_3 T \right| = \left| \frac{(1-D_3) D_3 TV_{01}}{L_{02}} \right| \quad (5.37)$$

5.4 Frequency Domain Analysis of the Converter Using Bode Plot with Respect to the States of Operation

Figures 5.13(a), (b), (c) and (d) are the Bode plot $\hat{v}_{c01}/\hat{d}_1$, $\hat{v}_{c01}/\hat{d}_2$, $\hat{v}_{c02}/\hat{d}_3$ and $\hat{v}_{bat}/\hat{d}_2$, respectively. Since the DC-DC boost converter has a non-minimum phase transfer function due to the right half plane open-loop zero [17], [73], hence PI compensation is used to make the system stable. The Bode plot of the boost side $\hat{v}_{c01}/\hat{d}_1$ and $\hat{v}_{c01}/\hat{d}_2$ with and without the PI compensator is shown in Figures 5.13(a) and (b), respectively. In Figure 5.13(a), marked in green, blue and red are *state-I*, *state-II* and *state-III*, respectively and in Figure 5.13(b), marked in green and red are *state-III* and *state-IV*, respectively, where ω_{gc} is the gain crossover frequency. The negative gain margin (GM) and phase margin (PM) of the system are without PI compensation. Using PI compensator $G = k_p + k_i/s$, the plots are marked in similar colors in Figure 5.13(a), which indicates the GMs are 0.3 dB, 4.4 dB, 6.1 dB and PM is 90° at the gain cross-over frequency (ω_{gc}) of 7 rad/s. Figure 5.13(b) shows the GM 1.42 dB, 12.9 dB, and PM is 90° at the ω_{gc} of 2 rad/s and 7 rad/s, respectively. The difference in GM values is due to the change in steady-state gain, and changing the gain does not affect the phase plot. Figures 5.13(c) and (d) show the buck outputs for the auxiliary load and the battery. The system is stable, and the GM is infinite for all the states.

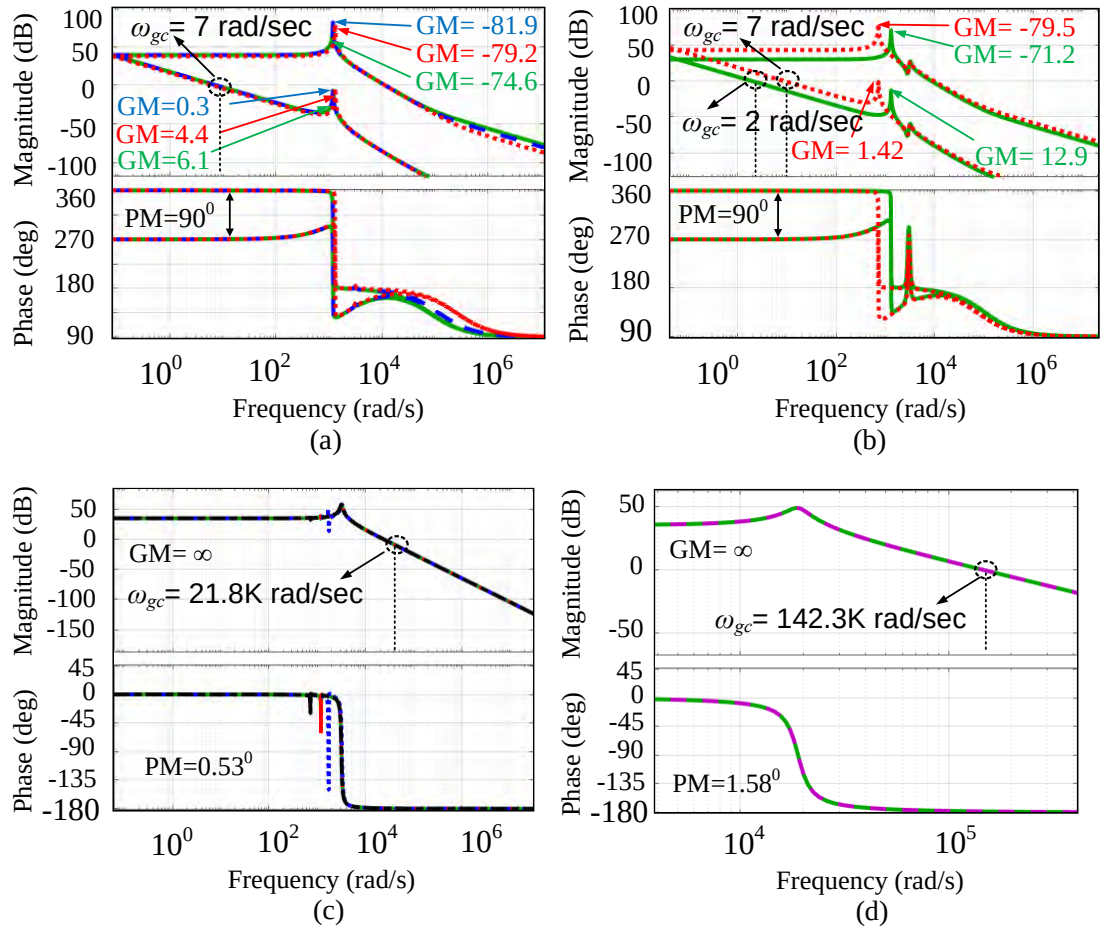


Figure 5.13 Frequency domain analysis of the FPFTDC converter using Bode plot with respect to states of operations for (a) $\hat{v}_{c01}/\hat{d}_1$, (b) $\hat{v}_{c01}/\hat{d}_2$, (c) $\hat{v}_{c02}/\hat{d}_3$ and (d) $\hat{v}_{bat}/\hat{d}_2$.

5.5 Input Capacitor Design (C_{pv})

The PWM to the switches S_{S1} and S_{S2} are 180° phase-shifted, which produces only three modes of operation as shown in Figure 5.4 and Table 5.1. During *mode 1*, only switch S_{S1} is turned-on and switch S_{S2} is turned-off with a duty ratio D_1 . During *mode 2*, both the switches are turned-off with a duty ratio of $(1-2D_1)$ and during *mode 3*, switch S_{S2} is turned-on and switch S_{S1} is turned-off with a duty ratio of D_1 . The state space representation and SSM of single-diode PV modules have been carried out for the designing of the input capacitor (C_{pv}) and has been presented in Appendix (A.3.1), where the state and input vector can be written as follows:

$$x(t) = \begin{bmatrix} i_{S1} & i_{S2} & v_{pv} \end{bmatrix}^T, \quad u(t) = v_{C01} \quad (5.38)$$

The following mathematical relation can be written during mode 1 to mode 3:

$$i_{in} = i_{S1} + i_{S2} = i_{pv} - i_{Cpv} \quad (5.39)$$

$$\dot{i}_{S1}(t) = \left(\frac{v_{pv}(t)}{L_{S1}} \right), \dot{i}_{S2}(t) = \left(\frac{v_{pv}(t) - v_{C01}}{L_{S2}} \right), \quad (5.40a)$$

$$\dot{v}_{pv}(t) = - \left(\frac{v_{pv}(t)}{C_{pv}R_i} + \frac{(i_{S1} + i_{S2})}{C_{pv}} \right) \quad (5.40b)$$

where the negative sign of PV current denotes that the load is a source, and R_i is the input source resistance. The averaged large signal model of the system can be defined, and using the final state-space linearized equation for small signal modelling by applying perturbations to each variable, the transfer function can be written as follows:

$$\frac{\hat{v}_{pv}(s)}{\hat{d}_1(s)} = \frac{-v_{C01}}{L_{seq}C_{pv}s^2 + \frac{L_{seq}}{R_i}s + 1} \quad (5.41)$$

$$\text{where, } L_{seq} = \frac{L_{s1}L_{s2}}{L_{s1} + L_{s2}}$$

The above transfer function is a second-order system, now, after solving for C_{pv} , it can be written as follows:

$$C_{pv} = \frac{L_{seq}}{4(R_{mpp})^2 \zeta^2} \quad (5.42)$$

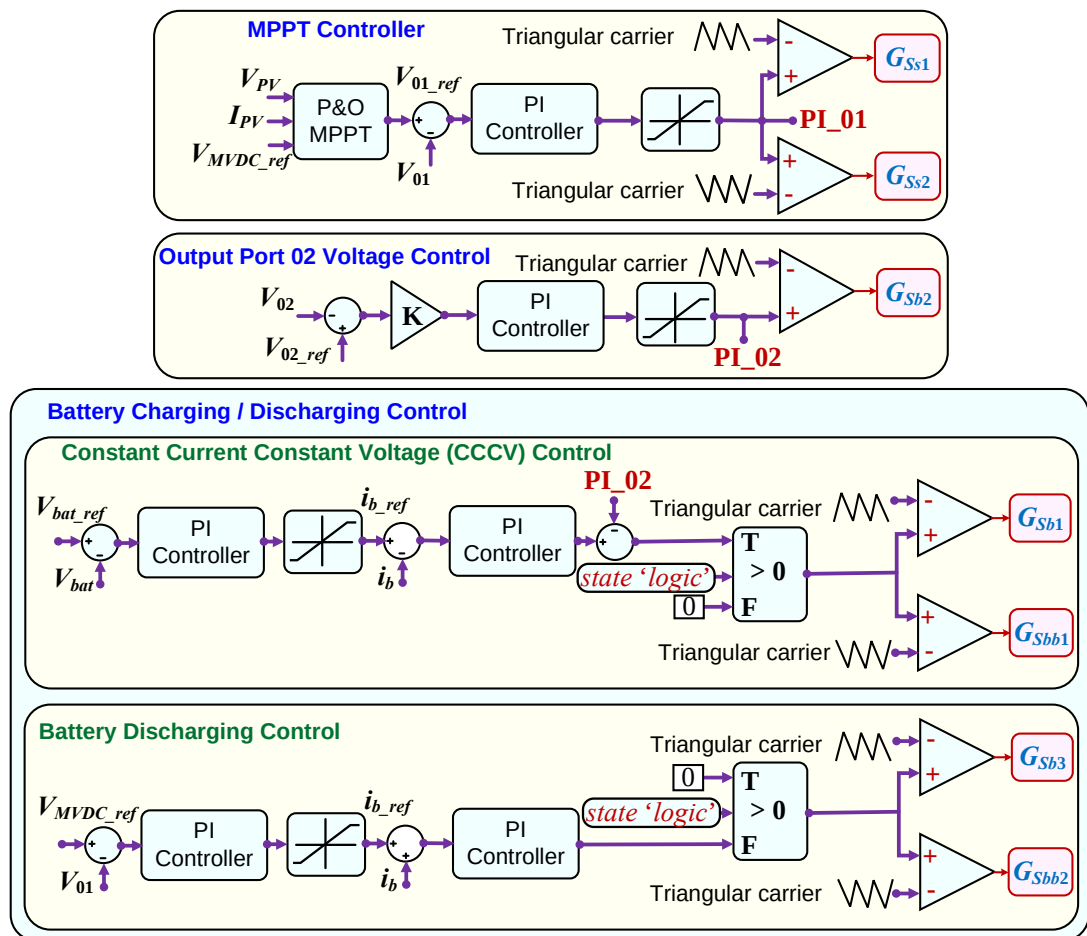
where $R_i = R_{mpp}$ at the maximum power point and ζ is the damping coefficient. It can be concluded from (5.42) that the input capacitor is mainly dependent on the inductor (L_{seq}), R_{mpp} and ζ . However, the above equation is similar to the generalized formula for input capacitors to any irradiance, but due to the interleaving of inductors, the generalized formula is replaced by the equivalent inductance for the n -phase connected in parallel. The lower the input capacitor value, the better the efficiency and transient response.

5.6 Control Strategy for Different States of Operation

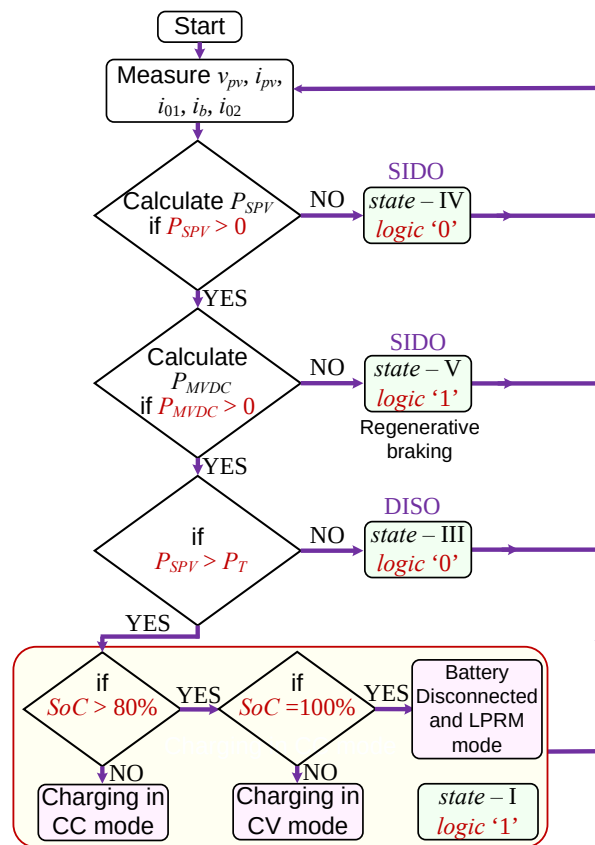
The system comprises two 55 W peak series-connected monocrystalline solar PV panels, which generate a maximum of 80 W of solar PV power. A 24 V, 8 Ah battery

setup is used for energy storage. Solar PV power generation uses perturb-and-observe (P&O) MPP control. The objective of the control technique shown in Figure 5.14(a) is to maintain the DC bus voltages V_{01} ($= MVDC$) and V_{02} while charging the battery using the CCCV method. The system is designed so that during the generation of 75% of the peak installed solar PV power, it can supply power to all *ports*. Two operational states are possible in this condition, i.e., *state-I* and *state-II*. During these two states, the operation switches S_{b3} and S_{bb2} are permanently off. It contains two voltage control loops: MPP control for dc bus voltage V_{01} , switched-boost action control for dc bus voltage V_{02} , and a dual-loop PI controller for battery charging. The outer loop control generates an error signal from the battery reference voltage (V_{bat_ref}) and the battery actual voltage (V_{bat}), and then feeds it to the PI controller with constant-current limitation to generate the battery reference current (i_{b_ref}). The inner loop control generates an error signal using i_{b_ref} and the actual current of the battery (i_b). Further, it is fed to the PI controller to generate the duty cycle. Since *state-I* and *state-II* are operational, time-multiplexing is done between the switches S_{b1} and S_{b2} and the final duty cycle is passed through the comparator block to generate the PWM for the switch S_{b1} and its 180° phase-shifted pulse is given to the switch S_{bb1} .

The flowchart for the control logic for state selection is shown in Figure 5.14(b). When the solar PV power is zero, the system operates under *state-IV*. If solar PV power is greater than zero during the braking mode (i.e., if $P_{MVDC} < 0$) of the vehicle, the regenerative power is fed back to the system using *state-V*, and during motoring mode (i.e., if $P_{MVDC} > 0$) and the input power (P_{pv}) is greater than the net output power P_T ($= P_{bat} + P_{02} + P_{MVDC}$), then *state-I* and *state-II* operate, and if not, then *state-III*. The SoC of the battery is determined based on the actual voltage of the battery used in the system. During *state-IV*, the S_{b1} and S_{bb1} switches are kept permanently off. In this state, dual-loop PI controllers are also used for discharging the battery. In the outer control loop, an error signal is generated from the DC-bus reference voltage (V_{MVDC_ref}) and V_{01} , and then fed to the PI controller to generate i_{b_ref} . The inner loop control generates an error signal from i_{b_ref} and i_b , which is then fed to the PI controller to generate the duty cycle.



(a)



(b)

Figure 5.14 Control strategy for FPFTDC converter (a) switching control technique, and (b) flowchart control logic for state selection.

5.7 Experimental Validation

The experimental results show the characteristics of the proposed FPFTDC converter in different operating conditions. The verification and discussion are presented in detail in this section. To validate the proposed FPFTDC converter, a prototype is developed as shown in Figure 5.15. The prototype uses a TI F28379D control board for power management and control. The F28379D is a dual-core architecture-enabled real-time processor to implement the complex control algorithms often required in digital power applications. It includes twelve enhanced PWM channels and high-speed ADCs, allowing the precise generation of switching pulses essential for modulating power converters. The ePWM channels are synchronized with other peripherals, supporting high-frequency switching applications. Voltage and current measurements are taken using LV25-P and ACS712 hall-effect sensors, respectively. All voltage and current measurements shown here align with the

polarities indicated in Figure 5.2, except the battery current, which is reversed. Positive battery current indicates charging, while negative indicates discharging. Experimental results are presented in the Figure 5.16 to Figure 5.21, and the comparative efficiency curve analysis with respect to different loads for each state is given in Figure 5.22. The designed values of circuit parameters with respect to mathematical relations derived in heading 5.2, and the used values of circuit parameters are listed in Table 5.3.

The proposed converter is characterized in healthy operating conditions and OCSF conditions. Further, the results are also presented and discussed in two sub-headings as follows:

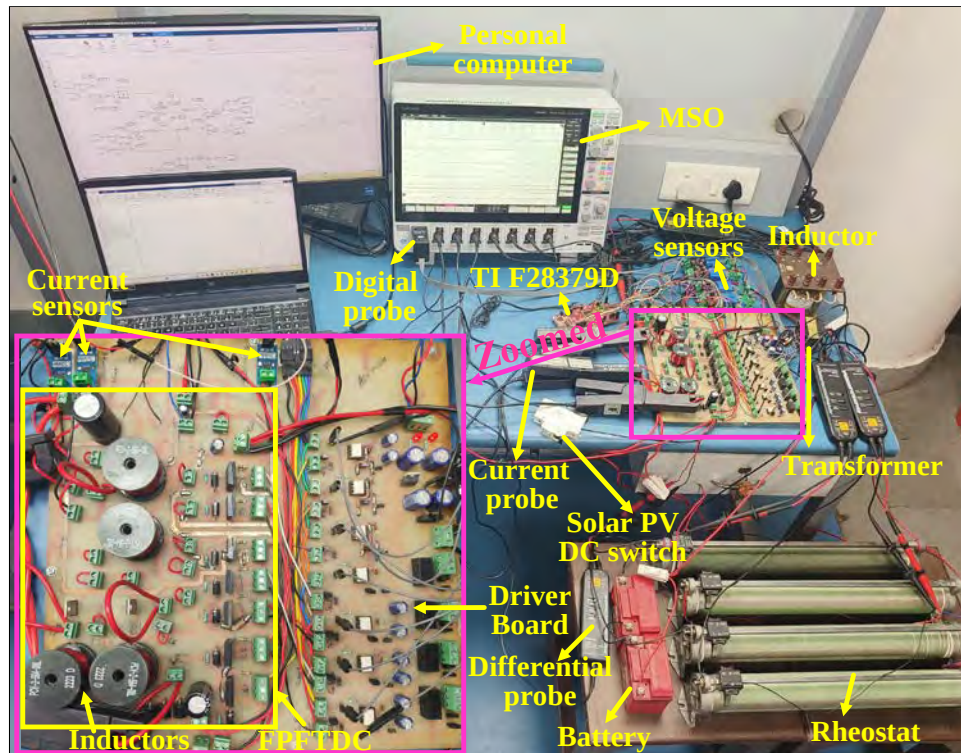


Figure 5.15 Experimental setup for the proposed FPFTDC converter.

5.7.1 Under Healthy Conditions

Figure 5.16, the experimental results for the normal operation of the FPFTDC converter are shown. In *state-I* operation, solar PV supplies power to all the ports. Figure 5.16(a) shows all the four-port voltages and inductor currents. *Channel 1* of the oscilloscope shows a digital switching pulse for all the switches. During charging switch S_{b3} , S_{bb2} is kept permanently off. *Channels 2* and *4* show the boost side inductors (L_{s1} and L_{s2}) currents i_{s1} and i_{s2} , respectively. *Channels 5* and *6* show dc bus voltages,

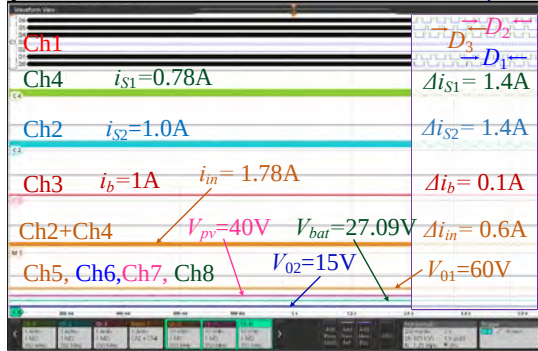
i.e., $V_{01} = 60\text{V}$ and auxiliary load dc bus voltage $V_{02} = 15\text{V}$, respectively. *Channel 7* exemplifies solar PV voltage $V_{pv} = 40\text{V}$. Two 55 W peak mono-crystalline modules are connected in series with MPP voltage $V_{mpp} = 20.528\text{V}$ and MPP current $I_{mpp} = 2.9242\text{A}$ at standard test conditions. *Channel m_1* is the math addition for the input current $i_{s1} + i_{s2} = i_{in}$, with an average current of 1.78A and an input ripple current of $\Delta i_{in} = 0.6\text{A}$. *Channels 8 and 3* show battery voltage V_{bat} and battery current i_b , respectively. Two batteries, each of 12V, 4Ah, are connected in series and charge in CC mode. During this state, the battery is charged with a constant current of 1A, and the voltage increases to 27.09V. In *state-II* operation, Figure 5.16(b), the load at port 01 is removed, which does not affect the DC-link voltage V_{01} . In this *state* the charging current i_b of the battery is increased to 2.2A to maintain the converter to run in CCM. The battery ripple current Δi_b is increased to 0.3A due to the change in the steady-state value of the battery voltage V_{bat} and the average battery current.

Figure 5.16(c) shows *state III* operation, where load demand is higher than the solar PV power. The load sharing is done between the solar PV and the battery. *Channel 4* of the oscilloscope shows i_{pv} ; *channels 2, 3, and m_1* are the inductor currents i_{b1} , i_{b2} , and math addition battery current $i_b = i_{b1} + i_{b2}$, respectively. In this *state*, the PV current i_{pv} is 0.5A, and the battery current is negative with an average value of -1.5A. *Channels 5, 6, and 8* are the DC bus voltages V_{01} , V_{02} , and V_{bat} , respectively.

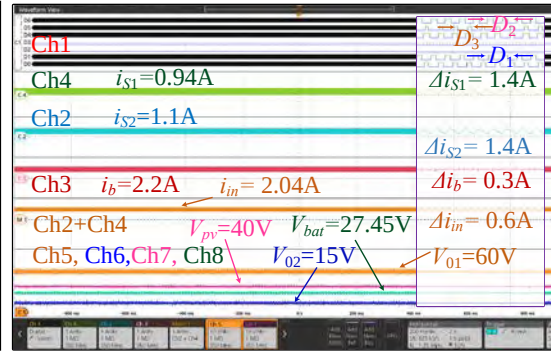
Figure 5.16(d) shows *state-IV* operation. *Channels 2, 3, and 4* are the inductor currents i_{b1} , i_{b2} and the battery current, respectively. *Channels 5, 6, and 8* are the DC bus voltages V_{01} , V_{02} and V_{bat} , respectively. The negative polarity of the battery current shows that the battery is discharging with an average current of -2.5A. The battery ripple current Δi_b and voltage V_{bat} are 0.6A and 18.1V, respectively.

Figures 5.16(e) and (f) show the state transition from *state-II* to *state-I*, and *state-III* to *state-IV* under healthy condition, respectively. During the *state-II* to *state-I* transition, load at output port 01 increases and the input current increases from 1.68A to 2.11 while all the other constraints remain analogous to *state-I* operation. Whereas during *state-III* to *state-IV* transition, the solar and the battery current fulfil the required load demands.

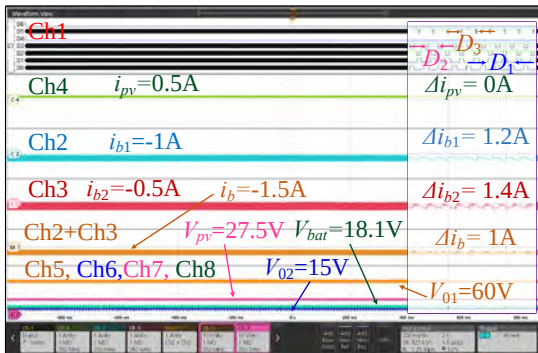
Ch1: Digital out; Ch2: y-axis: 1A/div; Ch3: y-axis: 1A/div; Ch4: y-axis: 1A/div; Ch5, Ch6, Ch7, Ch8: y-axis: 10V/div, x-axis: 200ms/div, zoomed: 200μs/div



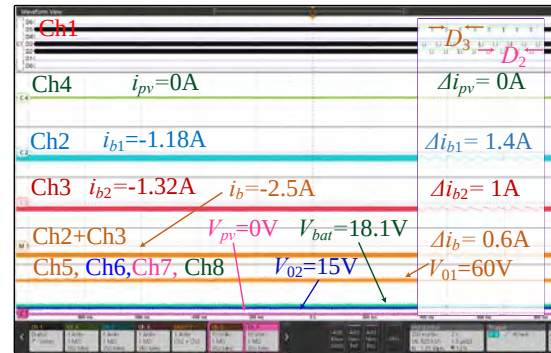
(a)



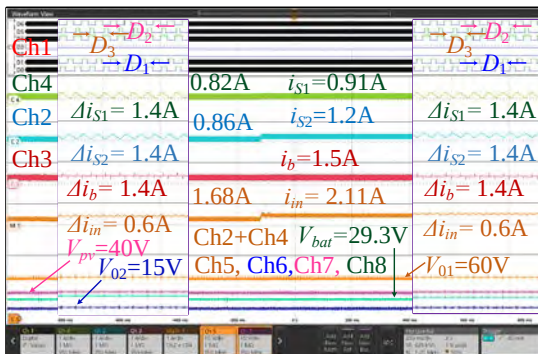
(b)



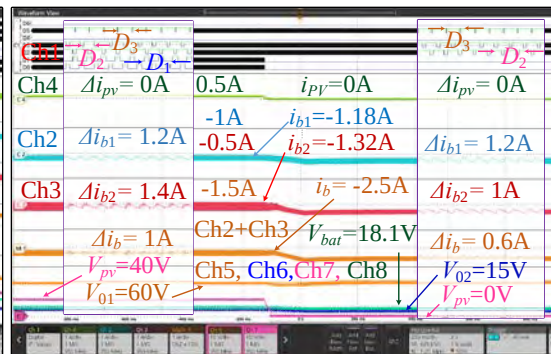
(c)



(d)



(e)



(f)

Figure 5.16 Experimental results of proposed FPFTDC converter under healthy operation during (a) state-I, (b) state-II, (c) state-III, (d) state-IV, and state transition from (e) state-II to state-I, (f) state-III to state-IV.

5.7.2 Under Open Circuit Switch Fault Conditions

The proposed FPFTDC converter is fault-tolerant under OCSF conditions. The OCSFs are considered with healthy antiparallel diodes. The single switch faults are

created in S_{s1} , S_{s2} , S_{b1} , S_{b2} , S_{bb1} , S_{bb2} , and S_{b3} , and the reliable operation of the converter is tested with identical circuit parameters and similar test conditions.

In Figure 5.17, the results are taken in two stages, with and without the S_{bb1} switch fault. For the first stage without fault, the battery ripple current Δi_b is 0.5A with the interleaving of the inductors L_{b1} and L_{b2} , and for the second stage with fault, Δi_b is 1.5A when only *leg-1* operates. It can be seen that when the battery is charged with interleaved inductors, the battery ripple current is reduced. In contrast, the ripple current increases when the interleaving section has been removed. In both cases, it can be seen that the average battery current remains the same at 1.05A and the DC bus voltages are maintained. The discharging of the inductor L_{b2} is done through the switch S_{bb2} and diode D_{bb1} , respectively. Hence, the fault in switch S_{bb1} does not change the operating modes and remains the same as a healthy condition of operation.

Under OCSFs in S_{s1} and S_{bb1} conditions: In *state-I operation* (Figure 5.18), the average current across inductor L_{s1} is 0A, and the total input current is supplied through inductor L_{s2} . The results indicate that the input ripple current has increased from 0.6A to 1.2A, and its average current is 1.67 while keeping the battery current with and without fault, and the DC bus voltages are maintained at set values. Hence, it can be inferred from the result below that if any of the interleaved switches undergo a fault situation, the converter is fault-tolerant.

Figure 5.19 is captured for *state-I* in three different conditions, i.e., healthy operation, OCSF at S_{s1} , S_{bb1} and S_{b2} simultaneously, and OCSF with no load at output port 01. Since the load at output port 01 is removed, other conditions remain the same as in the previous stage. Hence, the input current is reduced to 1.16A from 1.62A to maintain the power flow balance, and in this stage, the net input power is transferred to the battery charging while maintaining the DC bus voltage V_{01} to set values.

For the *state-II operation* (Figure 5.20), in this state also, results have been taken for three stages, such as operating analogously to the *state-I* without any fault; a fault has been given to switch S_{s1} and S_{bb1} at the same time, load R_{01} is removed; and other conditions remain the same as in the previous stage; hence, the input current is reduced to 1.18A from 1.86A to maintain the power flow balance. The net input power is transferred to the battery charging as well as the auxiliary load while maintaining the DC bus voltages V_{01} and V_{02} to set values.

For the *state-IV* operation (Figure 5.21): *Channels 2, 3, and 4* are the inductor currents i_{b1} , i_{b2} and battery current, respectively. *Channels 5, 8, and 7* are the dc bus voltages V_{01} , V_{02} and V_{bat} , respectively. The negative polarity of battery currents denotes that the battery is discharging. In this state, results were obtained for two stages, with and without the S_{bb2} switch fault. In the first stage, when there is no fault, the battery average and ripple current are -1.66A and 0.3A, respectively and for the second stage, the battery average current is the same as in the previous stage, but the battery ripple current Δi_b has been increased from -0.3A to -1.2A while maintaining the DC bus voltages V_{01} and V_{02} to set values.

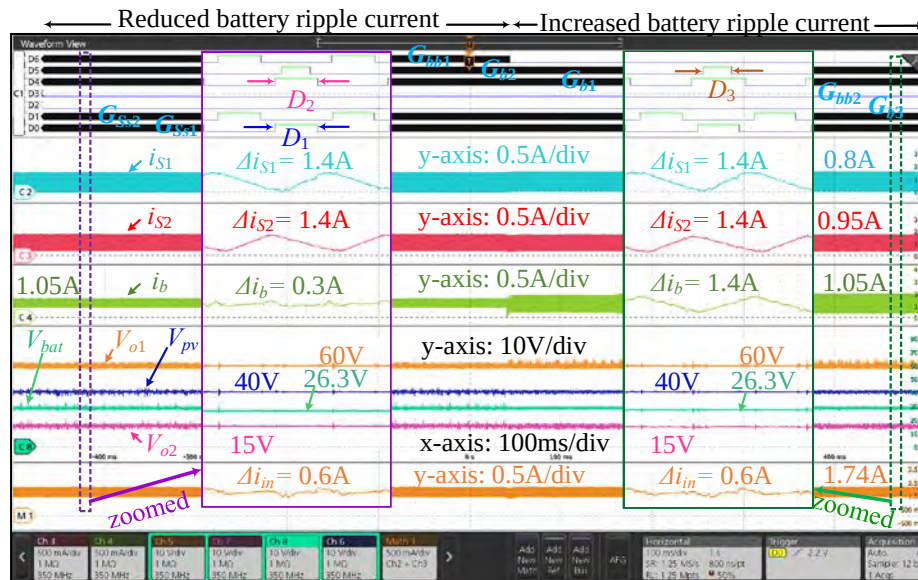


Figure 5.17 Experimental output waveforms for *state-I* operation with reduced battery current ripple and switch S_{bb1} fault during charging.

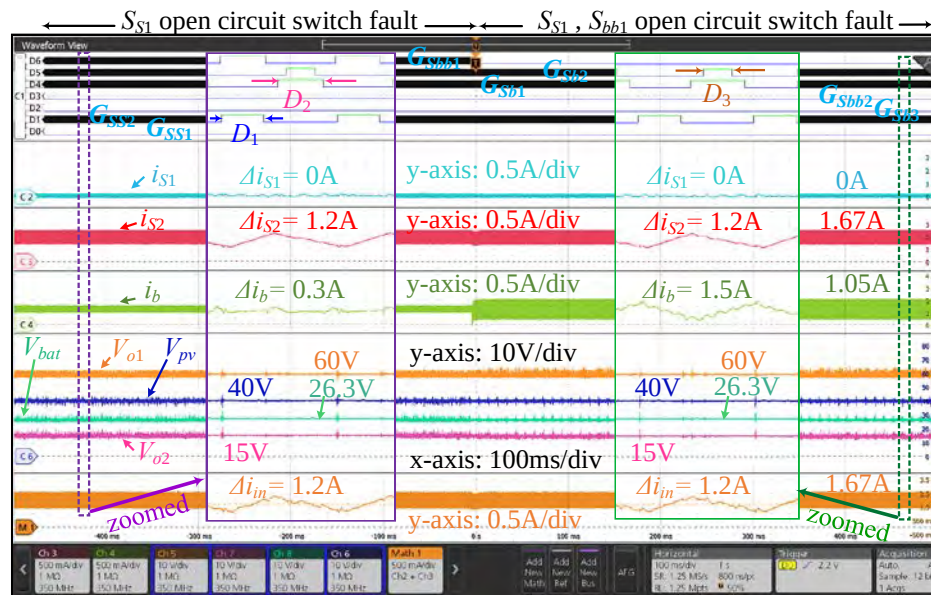


Figure 5.18 Experimental output waveforms for *state-I* operation with open circuit switch faults in S_{S1} and S_{bb1} .

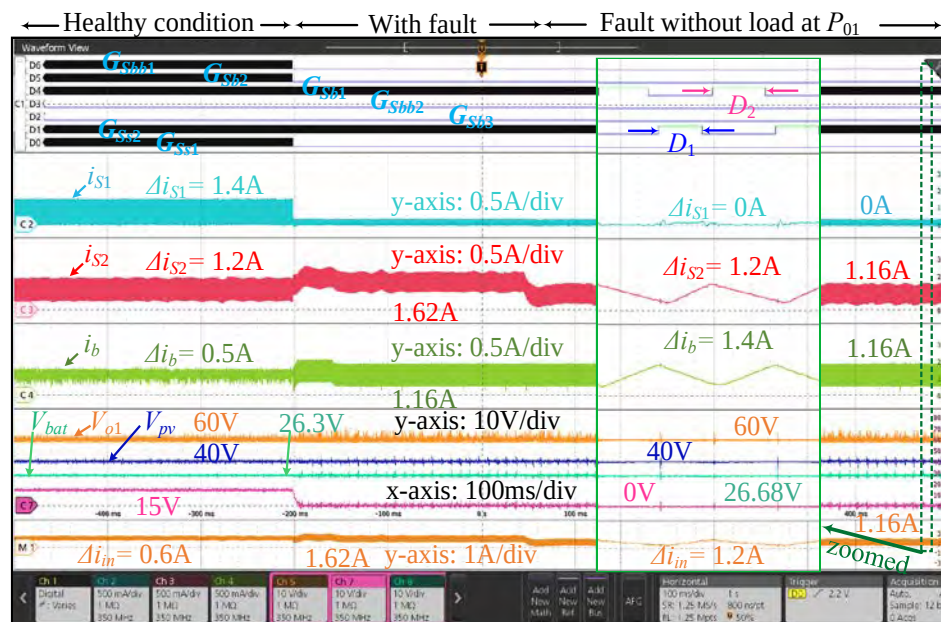


Figure 5.19 Experimental output waveforms for *state-I* operation with open circuit switch faults in S_{S1} , S_{bb1} and S_{b2} , with load and no-load at *port 01*.

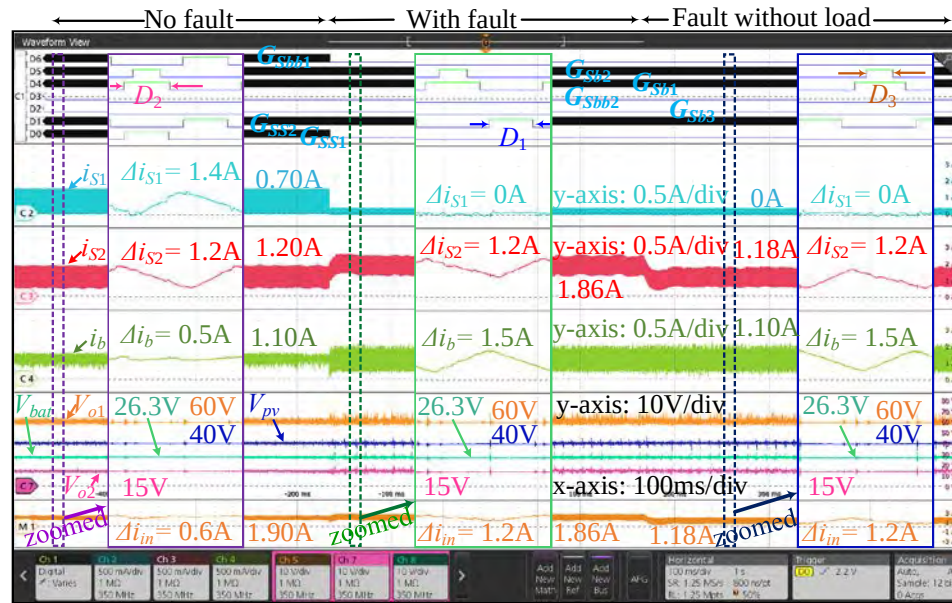


Figure 5.20 Experimental output waveforms for *state-II* operation with open circuit switch faults in S_{S1} and S_{bb1} , with load and no-load at *port 02*.

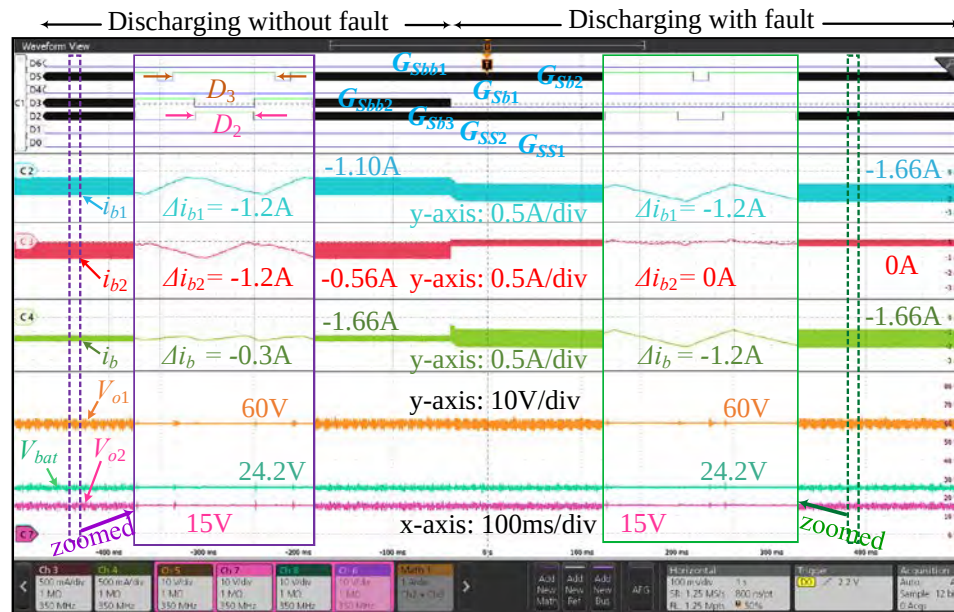


Figure 5.21 Experimental output waveforms for *state-IV* operations with an open circuit switch fault in S_{bb2} .

5.7.3 Efficiency Analysis of the Proposed Converter

The prototype of FPFTDC was developed in the lab and tested at low power under healthy and OSCF conditions. The overall efficiency of the converter is calculated with respect to the ratio of total output power to the total input power within the respective *state* of operation and presented in Figure 5.22.

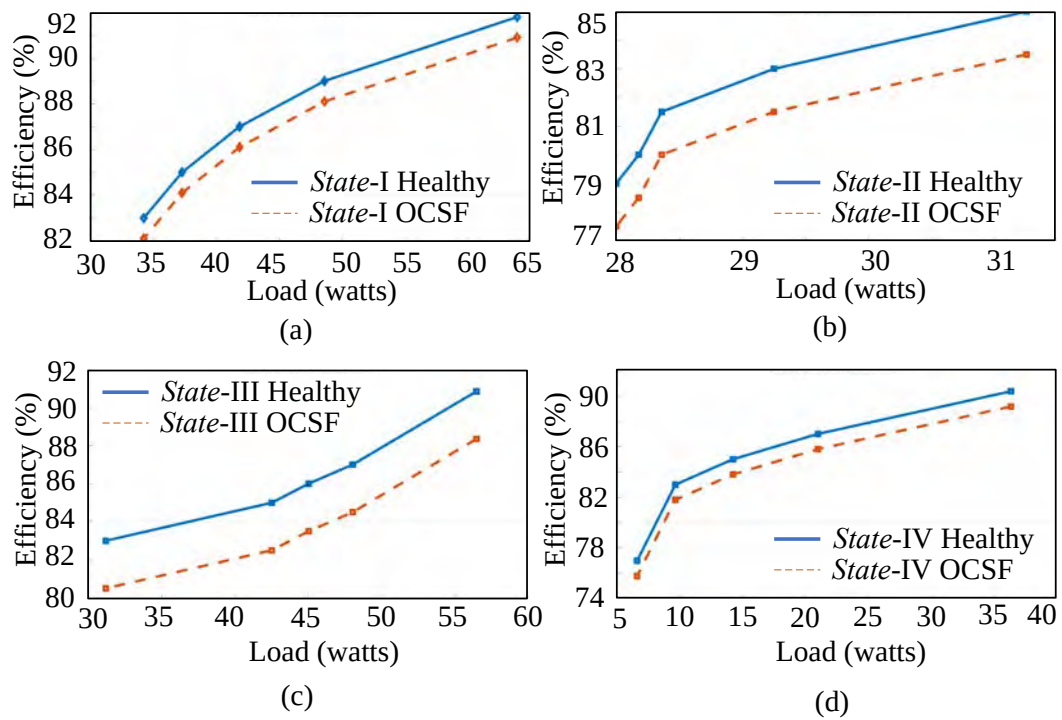


Figure 5.22 Performance comparison of the proposed converter under healthy and OCSF conditions during (a) *state-I*, (b) *state-II*, (c) *state-II* and (d) *state-IV*.

5.7.4 Comparative Analysis of the System

A qualitative and quantitative assessment of the proposed FPFTDC topologies with the various research outcomes presented in the literature in the similar category is presented in Table 5.7. The power density of the converter is defined with respect to operating frequency. The proposed designs demonstrate superior performance, offering solar operation at *MPP*, multiple states, multiple switch fault tolerance, and a number of required isolated drivers and bidirectional ports, which are distinct advantages over other topologies.

Comparison Parameters		[29]	[32]	[76]	[27]	[121]	[26]	[28]	[72]	[19]	Proposed	
Number of Components	Switch	Normal Mode	1,1,1	3	2	3	3	3	4	3	4	4
		Reconfigured	0	0	1	3	1	0	0	0	0	3
			Total	3	3	3	6	4	3	4	3	4
	Diode	2,2,2	3	1	1	1	5	3	2	2	4	2
	Inductor	Normal Mode	1,1,1	1	2	2	1	1	3	2	1	3
		Reconfigured	0	2	0	0	0	0	0	0	0	2
Total			3	3	2	2	1	1	3	2	1	5
Fault Tolerance	Capacitor	2,2,2	2	2	1	3	3	2	3	2	4	
	Single switch	S_{w1}, S_{w2}, S_{w3}	S_{w1}, S_{w2}, S_{w3}	S_{w1}	S_{w1}, S_{w2}, S_{w3}	S_{w1}	NR	NR	NR	NR	S_{s1}, S_{s2}, S_{b3} S_{b2}, S_{bb1}, S_{bb2}	
	Multiple switch	No	Yes	No	Yes	No	NR	NR	NR	NR	Yes	
	Number of Operating States	4	1	1	1	1	2	4	5	2	5	
Type of Switch Faults Addressed	OC/SC	OC/SC	OC	OC	OC/SC	NR	NR	NR	NR	NR	OC	
Control complexity	Medium	Medium	Medium	Simple	NR	Complex	Complex	Simple	Simple	Medium	Medium	
Power Flow Type	Separate	Separate	Separate	Shared	Shared	Shared	Shared	Shared	Shared	Shared	Shared	
SPV (At MPP)	No	No	No	No	No	Yes	No	Yes	No	Yes	Yes	
Voltage Restrictions	$V_o > V_{in}$	$V_o > V_{in}$	$V_o > V_{in}$	$V_o > V_{in} > V_b$	$V_o > V_{in} > V_b$	$V_o < V_{in} < V_b$	$V_o > V_{in} > V_b$	$V_o > V_{in} > V_b$	$V_o > V_{o1} > V_{in}$	$V_{in} < V_b$	$V_{o1} > V_{pv} > V_b > V_{o2}$	
No. of Isolated Driver	3	1	2	2	3	3	2	4	2	4	4	
No. of Ports	Bidirectional	0	0	1	1	1	1	1	2	1	2	
	Unidirectional	2	2	2	2	2	2	2	2	3	2	
	Total	2	2	3	3	3	3	3	4	4	4	
Efficiency	Healthy condition	91.10	93.90	92.67	93.70	89.90	90.00	93.60	98.20	NR	*91.80	
(%)	OCSF condition	90.30	93.60	92.71	93.66	NA	NA	NA	NA	NR	*90.90	
Power Density	High	High	Low	Moderate	Moderate	Moderate	Moderate	Moderate	Moderate	Low	Moderate	
Cost	Low	Low	High	High	Medium	Low	Low	High	Medium	Medium	Medium	

5.8 Conclusions

This chapter presents the design and operation of a novel solar PV-fed FPFTDC multifunctional converter. The interleaved nature of the circuit reduces battery current ripple and the size of the solar PV-side capacitor with increased current capability. It also provides fault-tolerant capability against OCSFs. The detailed analysis of fault-

28 tolerant behavior is discussed. The steady-state analysis and mathematical equations for input current ripple are derived for all the states of operation based on the duty cycle, normalized input voltage, and voltage gain. The time-multiplexing control reduces the number of semiconductor devices with respect to the total number of ports and redundancy in the system to improve reliability. The control strategy is designed to manage power for renewable sources like PV systems through P&O MPP and CCCV battery charging while also ensuring a stable, boosted DC bus voltage and enhancing the resilience of DC power availability. The proposed architecture effectively regulates the DC bus voltages across all operating states and all the output ports.

Chapter 6

ROBUST CONTROLLER DESIGN FOR TIME MULTIPLEXED MULTIPORT DC-DC CONVERTERS

6.1 General

The increasing integration of solar PV systems demands efficient, reliable, and robust DC-DC converters with fast transient response to maintain voltage regulation and stability under rapid irradiance variations. The time-multiplexed converters offer significant advantages by dynamically allocating resources among multiple ports, enabling effective interfacing of diverse energy sources and storage units with a reduced number of semiconductor devices. Furthermore, incorporating multifunctional features enhances the converter's adaptability for varied operating scenarios, such as load sharing and bidirectional power flow management with energy storage systems [11], [23] [72, [130].

Fault-tolerance is an indispensable feature in advanced converter designs to ensure uninterrupted and reliable operation during component failures. In [27], fault-tolerant capabilities are integrated through reconfigurable circuit design and control algorithms to reroute the power flow and maintain system stability. In instances of switch faults such as OCSFs, the converter modifies its power distribution approach to prevent system shutdown [35], [58], [69], [70]; under such conditions, there is a requirement for control methodologies that explicitly address uncertainty, dynamic coupling, and wide operating-range variations, rather than relying solely on nominal linearized design models.

In the literature, converter performance is mostly reported under ideal conditions; however, the ESR of each component considerably influences the converter response. Nonideal variables, including load resistance, the capacitance-to-inductance ratio, and parasitic characteristics, significantly affect the dynamic behaviour of converters [12], [59], [103]. These characteristics may lead to adverse effects such as overshoots and oscillations in switching waveforms. This necessitates evaluating the system state-space dynamics, deriving SSMs, and designing controllers to ensure stability across all operating scenarios while accounting for parasitic effects [56], [105]. The limitations are reported regarding robustness, component count, and

dynamic performance of high-gain dc–dc boost converters in [15] and multiport converters in [75], [77], [132]. for flexible power integration with dc microgrids. The SLS theory [133] provides a framework to model the dynamic behavior of converters, facilitating theoretical analysis in power electronics.

In [14], [53],[103], the controllability analysis, disturbance-observer-based feedback control for accurate voltage regulation, stabilization, and robustness under load variations, as well as the controller design of the converter, are emphasized, demonstrating its ability to deliver consistent performance under variable conditions. In [14], graph-theoretic methods are integrated with SLS theory to establish necessary and sufficient conditions for controllability, emphasizing structural controllability and revealing the influence of converter topology on reachable state dynamics. In [52], SLS controllability is analyzed using state-space formulations, where the cyclic invariant subspace approach streamlines controllability assessment by reducing computational complexity.

The literature on the controllability of single-stage multicell DC-DC converters has been limited in recent years, with most control strategies still relying heavily on trial-and-error methods. This paper introduces a non-isolated time-multiplexed multiport fault-tolerant (TMMFT) DC-DC converter architecture, designed to achieve both maximum power point (MPP) tracking and dual-output voltage regulation. Figure 6.1(a) illustrates the circuit diagram of the TMMFT converter with circuit parasitic, and the various operational states of the converter are depicted in 1(b), where *state I* signifies that solar power (P_{SPV}) is greater than load demand and MPP state; *state II* signifies P_{SPV} is greater than load demand with vehicle is in rest under MPP and load power reference mode (LPRM) state; *state III* signifies, P_{SPV} is less than load demand and MPP state; and *state IV* signifies P_{SPV} is not available. It efficiently delivers medium-voltage dc (MVDC) and low-voltage dc (LVDC) loads.

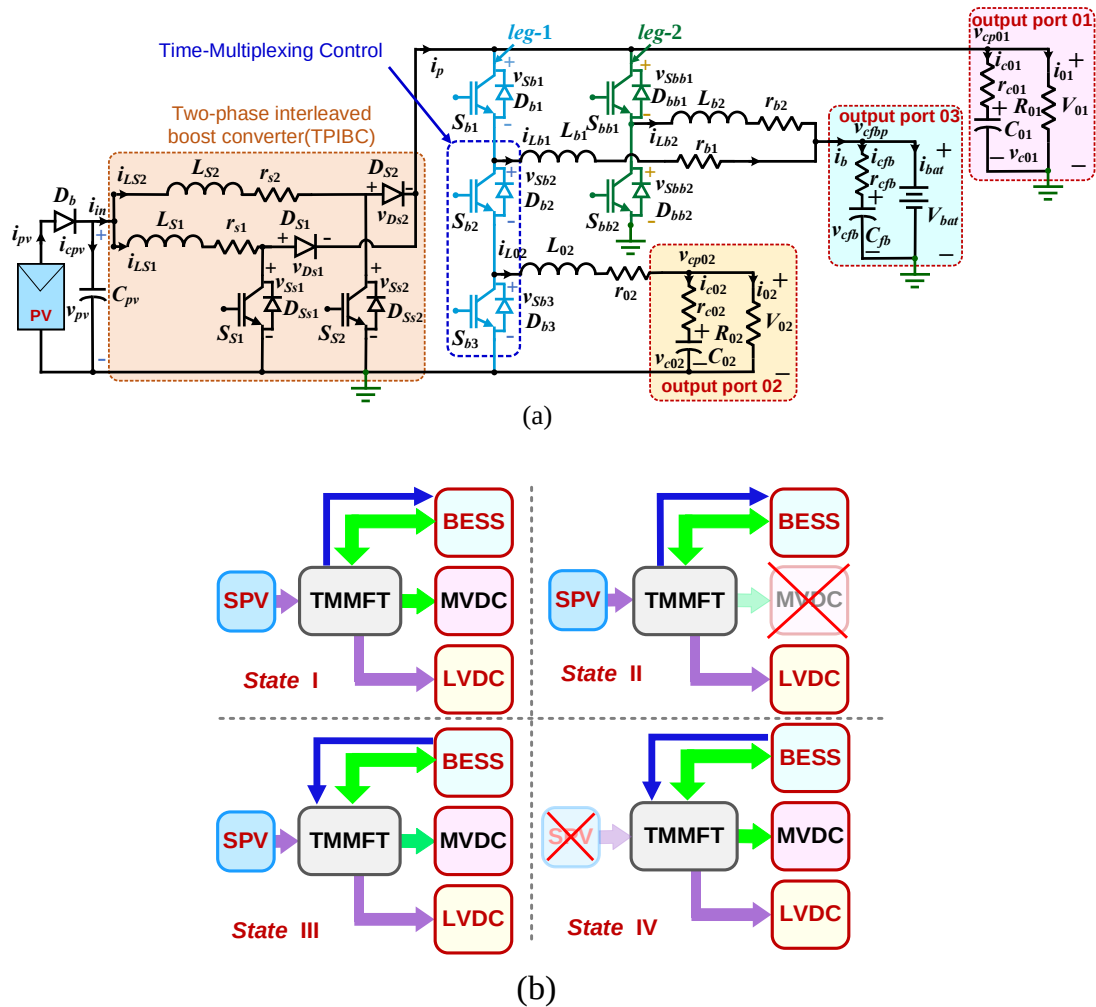


Figure 6.1 Time-multiplexed multiport fault-tolerant (TMMFT) dc-dc converter (a) schematic diagram, and (b) operating states.

6.2 Controllability Analysis of TMMFT Converter

The controllability analysis of power electronic converters is typically categorized into three fundamental components: (i) *structural controllability*, (ii) *state controllability*, and (iii) *output controllability* [14], [52] as discussed in **Chapter 3**. It provides the system behaviour under varying control strategies. It is explained in [14] thoroughly proposition-wise for each classification. The converter control performance can be accurately evaluated, modified, and assured only when its controllability is thoroughly understood [52]. In this context, the controllability of the proposed converter topology is rigorously assessed through an SLS model as given in (6.1), which offers a robust analytical framework for evaluating the system's dynamic behaviour under various switching configurations.

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$$\dot{x}(t) = \mathbf{A}_j x(t) + \mathbf{B}_j u(t); \quad y(t) = \mathbf{C}_j x(t) + \mathbf{D}_j u(t) \quad (6.1)$$

where, $x(t) \in \mathbb{R}^{n \times 1}$, $u(t) \in \mathbb{R}^{p \times 1}$ represent state, input variables; $\mathbf{A}_j \in \mathbb{R}^{n \times n}$, $\mathbf{B}_j \in \mathbb{R}^{n \times p}$, $\mathbf{C}_j \in \mathbb{R}^{1 \times n}$, $\mathbf{D}_j \in \mathbb{R}^{1 \times p} \quad \forall j \in \{1, 2, \dots, N\}$ represent state, input, output, and direct transmission matrices; n , p , and j represent the number of states, inputs, and modes, respectively.

6.2.1 Switched Linear System Model

State-I: The state space averaged (SSA) model for the switching modes from 1 to 6 of [64] under state-I (Γ_{S-I}) is derived and given in (6.2), the SSA model can be written for $x = [i_{Ls1}, i_{Ls2}, i_{Lb1}, i_{Lb2}, i_{L02}, v_{C01}, v_{C02}, v_{Cfb}]^T$ and $u = [v_{pv}, v_{Ss1}, v_{Ss2}, v_{Sb1}, v_{Sb2}, v_{Sbb1}, v_{Ds1}, v_{Ds2}, v_{Db2}, v_{Db3}, v_{Dbb2}]^T$; where, $i_{Ls1}, i_{Ls2}, i_{Lb1}, i_{Lb2}, i_{L02}$ are respective inductor currents; $v_{C01}, v_{C02}, v_{Cfb}$ respective voltage across the capacitors; v_{pv} is the input voltage; and $v_{Ss1}, v_{Ss2}, v_{Sb1}, v_{Sb2}, v_{Sbb1}, v_{Ds1}, v_{Ds2}, v_{Db2}, v_{Db3}, v_{Dbb2}$ are the respective voltage drop across semiconductor devices as given in Figure 6.1(a). After performing the averaging process over the defined switching period (T) as expressed in (6.2), the averaged small signal models (ASSM) are presented in (A4.14). This derivation is based on the introduction of small perturbations around the steady-state operating point of the duty cycles D_1, D_2, D_3 and the input voltage V_{pv} . Here, D_1, D_2, D_3 and V_{pv} represent the steady-state values, while $\hat{d}_1, \hat{d}_2, \hat{d}_3$ and $\hat{v}_{pv}$ correspond to their respective perturbed components. These perturbations induce small variations in the state variables and output responses of the system, which are given in (6.3).

$$\Gamma_{S-I} \equiv \left\{ \begin{array}{l} (A_1, B_1, C_1, (D_1 - D_3)T), (A_2, B_2, C_2, (D_2 - D_1)T), \\ (A_3, B_3, C_3, (1 - 2D_2)T), (A_4, B_4, C_4, (D_2 - D_1)T), \\ (A_5, B_5, C_5, D_1T), (A_6, B_6, C_6, D_3T) \end{array} \right\} \quad (6.2)$$

$$\begin{aligned} x &= X + \hat{x}, \quad u = U + \hat{u}, \quad v_{C01} = V_{01} + \hat{v}_{C01}, \\ v_{C02} &= V_{02} + \hat{v}_{C02}, \quad \text{and } v_{Cfb} = V_{bat} + \hat{v}_{Cfb}. \end{aligned} \quad (6.3)$$

With respect to (6.1) and (6.3), the SSM can be derived. Further, neglecting the steady-state DC-term and the 2nd-order term, it can be written as follows:

$$\hat{\dot{x}} = A\hat{x} + B\hat{u} + E_k\hat{d}_k \quad (6.4)$$

$$\hat{y} = C_k\hat{x} + D\hat{u} + F_k\hat{d}_k \quad (6.5)$$

where $E_k \in \mathbb{R}^{n \times 1}$, $F_k \in \mathbb{R}^{1 \times 1}$, $\forall k \in \{1, 2, 3\}$; k is the number of outputs at output ports. A , B , C , D , E and F are ASSM of *state-I* with circuit parasitic given in (A4.14) in the Appendix.

State-II: The SSA can be yielded from the *state I* after putting R_{01} equal to infinity, whereas it is open-circuited in hardware implementation. It will further deduce that the $G_1 = r_{C01}$ remaining analysis is similar to the previous state.

State-III: The SSA model for switching modes 1 to 6 under state-III (Γ_{S-III}) is derived and given in (6.6); the SSA model can be written for $x = [i_{Ls1}, i_{Ls2}, i_{Lb1}, i_{Lb2}, i_{L02}, v_{C01}, v_{C02}]^T$ and $u = [v_{pv}, v_{bat}, v_{Ss1}, v_{Ss2}, v_{Sb2}, v_{Sb3}, v_{Sbb2}, v_{Ds1}, v_{Ds2}, v_{Db1}, v_{Db3}, v_{Dbb1}]^T$.

$$\Gamma_{S-III} = \left\{ \begin{array}{l} (A_1, B_1, C_1, (D_1 + D_3 - 1)T), (A_2, B_2, C_2, (1 - D_2 - D_1)T), \\ (A_3, B_3, C_3, (2D_2 - 1)T), (A_4, B_4, C_4, (1 - D_2 - D_1)T), \\ (A_5, B_5, C_5, (D_1)T), (A_6, B_6, C_6, (1 - D_3)T) \end{array} \right\} \quad (6.6)$$

State-IV: The SSA model for switching modes 1 to 4 under state-IV (Γ_{S-IV}) is derived and given in (6.7); the SSA model can be written for $x = [i_{Lb1}, i_{Lb2}, i_{L02}, v_{C01}, v_{C02}]^T$ and $u = [v_{bat}, v_{Sb2}, v_{Sb3}, v_{Sbb2}, v_{Db1}, v_{Db3}, v_{Dbb1}]^T$.

$$\Gamma_{S-IV} = \left\{ \begin{array}{l} (A_1, B_1, C_1, (D_3 - D_2)T), (A_2, B_2, C_2, (2D_2 - 1)T), \\ (A_3, B_3, C_3, (1 - D_2)T), (A_4, B_4, C_4, (1 - D_3)T) \end{array} \right\} \quad (6.7)$$

The ASSMs are derived from the mathematical relations (6.6) and (6.7) over the defined switching period and presented in (A4.21) and (A4.27), respectively. The notations for all the state variables and state models are kept the same as *state I*; only the final matrices change.

6.2.2 Controllability Analysis

6.2.2.1 Structural Controllability of TMMFT Converter

The controllability assessment methodology discussed in **Chapter 3** is extended in this chapter for the proposed SLS-based converter model under different

operating conditions. Using a mode-wise averaged large signal model [A|B] can be formulated, and based on this, a structural controllability graph can be plotted as in Figure 6.2 using graph theory. In Figure 6.2(a) to Figure 6.2(d), the state and input variables are marked in black and magenta, respectively, forming *vertices*, while the connecting arcs are *directed edges*. The orientation of the directing arrow signifies that the state variable of the source vertex can induce an alteration in the state variable of the destination vertex. This indicates that the subsequent state variable may be affected by the previous state variable or input variable. The structural graph shown in Figure 6.2(a) to Figure 6.2(d) is referred to as a *tree*, with input variables (u) designated as its *root*. If all state variables in the *tree* are directly or indirectly influenced and regulated by the *root*, excluding the *root* itself, the system is structurally controllable.

6.2.2.2 State Controllability of TMMFT Converter

As mentioned in **Chapter 3**, the system (6.1) is considered controllable if every state vector $x \neq 0$ satisfies this criterion [52]. For a matrix $A \in \mathbb{R}^{n \times n}$ and $w \in \mathbb{R}^{n \times n}$ (i.e., linear subspace), the CIS of A with respect to w (i.e., $A|w$) is defined as follows:

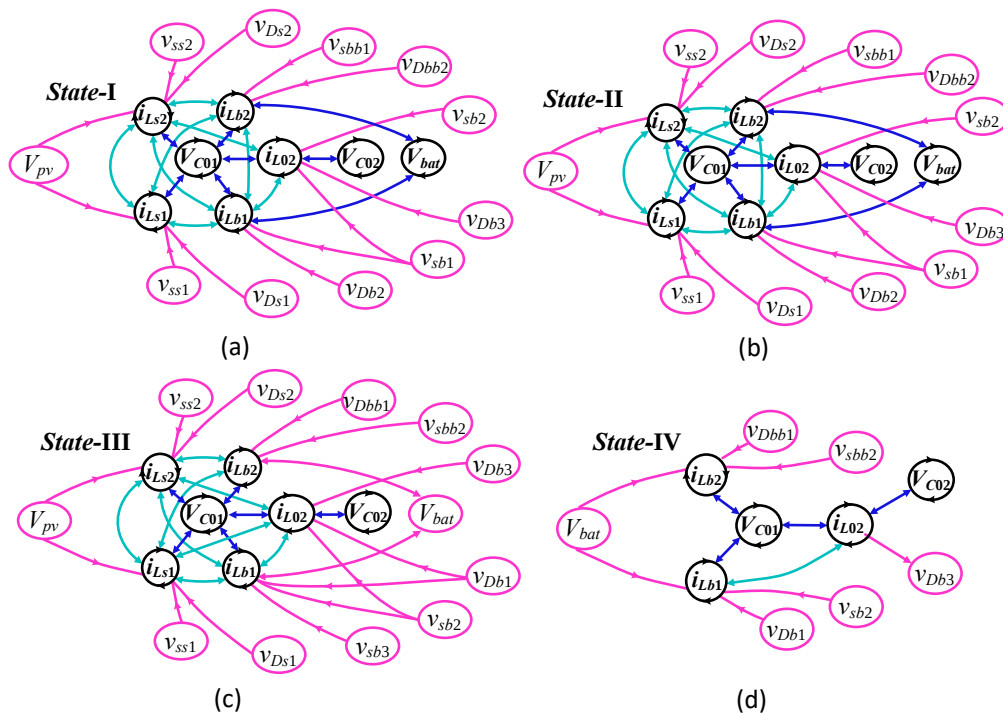


Figure 6.2 Structural controllability of TMMFT dc-dc converter for (a) *state I*, (b) *state II*, (c) *state III*, and (d) *state IV*.

$$\langle A|w \rangle = \sum_{j=1}^n A^{j-1}w \quad (6.8)$$

For an SLS shown in (6.1), the linear subspace sequence is expressed as follows:

$$w_1 = \sum_{j=1}^N \langle A_j | B_j \rangle, w_2 = \sum_{j=1}^N \langle A_j | w_1 \rangle, \dots, w_n = \sum_{j=1}^N \langle A_j | w_{n-1} \rangle \quad (6.9a)$$

Proposition 1: (sufficient condition) If the state of the system (6.1) exhibits controllability, then $\text{rank}(w_1) = n$.

Proposition 2: (necessary condition) If the state of the system (6.1) exhibits controllability, then $\text{rank}(w_n) = n$.

Using (6.9a), the decision matrix w_1 for a state controllable system for *state I* and *state II* are calculated as follows:

$$\begin{aligned} w_1 &= \langle A_1 | B_1 \rangle + \langle A_2 | B_2 \rangle + \langle A_3 | B_3 \rangle + \langle A_4 | B_4 \rangle + \langle A_5 | B_5 \rangle + \langle A_6 | B_6 \rangle \\ &= B_1 + A_1 B_1 + A_1^2 B_1 + A_1^3 B_1 + A_1^4 B_1 + A_1^5 B_1 + A_1^6 B_1 + A_1^7 B_1 \\ &\quad + B_2 + A_2 B_2 + A_2^2 B_2 + A_2^3 B_2 + A_2^4 B_2 + A_2^5 B_2 + A_2^6 B_2 + A_2^7 B_2 \\ &\quad + B_3 + A_3 B_3 + A_3^2 B_3 + A_3^3 B_3 + A_3^4 B_3 + A_3^5 B_3 + A_3^6 B_3 + A_3^7 B_3 \\ &\quad + B_4 + A_4 B_4 + A_4^2 B_4 + A_4^3 B_4 + A_4^4 B_4 + A_4^5 B_4 + A_4^6 B_4 + A_4^7 B_4 \\ &\quad + B_5 + A_5 B_5 + A_5^2 B_5 + A_5^3 B_5 + A_5^4 B_5 + A_5^5 B_5 + A_5^6 B_5 + A_5^7 B_5 \\ &\quad + B_6 + A_6 B_6 + A_6^2 B_6 + A_6^3 B_6 + A_6^4 B_6 + A_6^5 B_6 + A_6^6 B_6 + A_6^7 B_6 \end{aligned} \quad (6.9b)$$

From (6.9b), w_1 is calculated for *state-I* as, $1 \times 10^{34} [0.0018 \ 0.0015 \ -1.1026 \ -1.1040 \ -0.0005 \ 0.0002 \ -0.0013 \ -0.7678]^T$. Similarly, the other CIS sequences are calculated as, $w_2 = 1 \times 10^{65} [0.0052 \ 0.0070 \ -0.5001 \ -0.4983 \ -0.0010 \ -0.0126 \ -0.0005 \ 2.4995]^T$; $w_3 = 1 \times 10^{96} [0.0386 \ 0.0515 \ -1.6061 \ -1.5932 \ -0.0074 \ -0.1037 \ -0.0009 \ 24.5315]^T$; $w_4 = 1 \times 10^{128} [0.0021 \ 0.0028 \ -0.0134 \ -0.0127 \ -0.0004 \ -0.0060 \ 0.0001 \ 1.5534]^T$; $w_5 = 1 \times 10^{158} [0.0088 \ 0.0117 \ 0.3012 \ 0.3041 \ -0.0017 \ -0.0272 \ 0.0008 \ 7.5516]^T$; $w_6 = 1 \times 10^{190} [0.0024 \ 0.0032 \ 0.3065 \ 0.3073 \ -0.0005 \ -0.0086 \ 0.0005 \ 2.7233]^T$; $w_7 = 1 \times 10^{220} [-0.0015 \ -0.0020 \ 1.9697 \ 1.9692 \ 0.0003 \ -0.0062 \ 0.0028 \ 4.7005]^T$; $w_8 = 1 \times 10^{251} [-0.0076 \ -0.0102 \ 0.9694 \ 0.9668 \ 0.0015 \ 0.0170 \ 0.0011 \ -2.9163]^T$.

According to the **Proposition 2**, the $\text{rank}(w_8) = \text{rank}(w_7) = \text{rank}(w_6) = \text{rank}(w_5) = \text{rank}(w_4) = \text{rank}(w_3) = \text{rank}(w_2) = \text{rank}(w_1)$. The column vectors

$A_1^7 B_1, A_2^7 B_2, A_3^7 B_3, A_4^7 B_4, A_5^7 B_5, A_6^7 B_6, A_4^6 B_4$ and $A_6^6 B_6$ in (6.9b) are linearly independent. Hence, $w_1 = \text{span}(A_1^7 B_1, A_2^6 B_2, A_3^7 B_3, A_4^7 B_4, A_5^7 B_5, A_6^7 B_6, A_4^6 B_4, A_6^6 B_6)$, i.e., $w_1 = 8$. Additionally, the other CIS sequences are also computed as w_1 , which satisfies **Propositions 1** and **2**, i.e., $w_1 = 8$ and $w_n = 8$. Therefore, *state I* is state-controllable.

Similarly, for *state II*, the CIS sequences can be calculated as mentioned in *state I* above. The rank of the decision matrix is the same as *state I*; hence, *state II* is state-controllable.

Similarly, for *state III*, the decision matrix is similar to previous states, but the order of the matrix has been reduced to $n = 7$ due to two source inputs, i.e., solar PV (V_{pv}) and battery (V_{bat}). So, omitting the 8th-order term from (6.9b) for each mode yields a decision matrix for *state III*. The CIS sequences can be calculated as mentioned in *state I* and *state II* above. The column vectors $A_1^6 B_1, A_2^6 B_2, A_3^6 B_3, A_4^6 B_4, A_5^6 B_5, A_6^6 B_6, A_4^5 B_4$ are linearly independent. Hence, $w_1 = \text{span}(A_1^6 B_1, A_2^6 B_2, A_3^6 B_3, A_4^6 B_4, A_5^6 B_5, A_6^6 B_6, A_4^5 B_4)$ i.e., $w_1 = 7$. Similarly, the other CIS sequences can also be computed as w_1 , which satisfies **Propositions 1** and **2**, i.e., $w_1 = 7$ and $w_n = 7$. Therefore, *state III* is state-controllable.

Similarly, for *state IV*, there are only four modes of operation, and the order of the matrix is $n = 5$ due to one input source, i.e., battery (V_{bat}). So, omitting the 6th, 7th and 8th order terms from (6.9b) for each mode yields a decision matrix for *state IV*. The CIS sequences can be calculated as $1 \times 10^{18} [0.2460 \ 0.0591 \ -0.0964 \ 0.4486 \ -2.2588]^T$. Similarly, the other CIS sequences are calculated as, $w_2 = 1 \times 10^{32} [0.2505 \ 0.0171 \ 1.3956 \ 0.2594 \ -9.1609]^T$; $w_3 = 1 \times 10^{47} [0.0734 \ 0.0010 \ 1.1177 \ 0.0459 \ -2.3379]^T$; $w_4 = 1 \times 10^{61} [0.1575 \ 0.0018 \ 5.3875 \ -0.0900 \ -0.5821]^T$; $w_5 = 1 \times 10^{76} [-0.0159 \ -0.0004 \ 1.8359 \ -0.1415 \ 3.5979]^T$. The column vectors $A_1^4 B_1, A_2^4 B_2, A_3^4 B_3, A_4^4 B_4$ and $A_1^3 B_1$ are linearly independent. Hence, $w_1 = \text{span}(A_1^4 B_1, A_2^4 B_2, A_3^4 B_3, A_4^4 B_4, A_1^3 B_1)$, i.e., $w_1 = 5$. Similarly, the other CIS sequences are also computed as w_1 , which satisfies **Propositions 1** and **2**, i.e., $w_1 = 5$ and $w_n = 5$. Therefore, *state IV* is state-controllable.

6.2.2.3 Output Controllability of TMMFT Converter

Output controllability in an SLS refers to the system's ability to steer its output vector to any desired final value within a finite time interval, using an appropriate combination of switching sequences and control inputs [52]. A system represented by (6.1) is considered output controllable if, for any initial state $x_0 \in \mathbb{R}^{n \times 1}$, $y_f \in \mathbb{R}^{q \times n}$ and an arbitrary initial control function $u_0(t)$, there exists a continuous control input $u(t)$ that drives the system such that the output evolves from $x(0) = x_0$ to $y(t_{finite}) = y_f$, where t_{finite} is a finite time horizon, and q is the total number of outputs.

Proposition 3: The state of the system (1) exhibits output controllability if $C_j w_n = \mathbb{R}^q$.

In *states* I and II, there are six modes and order $n = 8$ and $q = 1$. The computation of $C_1 w_8$, $C_2 w_8$, $C_3 w_8$, $C_4 w_8$, $C_5 w_8$ and $C_6 w_8$ are as follows: -2.7606×10^{250} , -2.7834×10^{250} , 1.1608×10^{249} , -2.7757×10^{250} , -2.7453×10^{250} , and -2.7650×10^{250} , respectively for first output variable. For the second and third output variables, all the modes are the same, so $C_{02} w_8$ and $C_{03} w_8$ are 1.5655×10^{248} and -2.3078×10^{251} , respectively. For *state* II, the computation of $C_1 w_8$, $C_2 w_8$, $C_3 w_8$, $C_4 w_8$, $C_5 w_8$ and $C_6 w_8$ are as follows: -2.7583×10^{250} , -2.7812×10^{250} , 1.1662×10^{249} , -2.7735×10^{250} , -2.7429×10^{250} , and -2.7627×10^{250} , respectively for first output variable. For the second and third output variables, all the modes are the same, so $C_{02} w_8$ and $C_{03} w_8$ are 1.5646×10^{248} and -2.3054×10^{251} , respectively. In *state* III, there are six modes and order $n = 7$ and $q = 1$. The computation of $C_1 w_7$, $C_2 w_7$, $C_3 w_7$, $C_4 w_7$, $C_5 w_7$ and $C_6 w_7$ are as follows: -2.3124×10^{155} , -1.6884×10^{155} , -3.0781×10^{155} , -3.0790×10^{155} , -4.2449×10^{155} , and -3.1997×10^{155} , respectively for first output variable. For the second output variable, all the modes are the same, so $C_{02} w_7$ is 1.0518×10^{157} . In *state* IV, there are four modes and order $n = 5$ and $q = 1$. The computation of $C_1 w_5$, $C_2 w_5$, $C_3 w_5$ and $C_4 w_5$ are as follows: 68540×10^{75} , -1.4105×10^{75} , -1.4094×10^{75} and -1.3628×10^{75} , respectively for first output variable. For the second output variable, all the modes are the same, so $C_{02} w_5$ is 4.1212×10^{76} . Hence, all the *states* satisfy **Proposition 3**. Therefore, it is output controllable.

6.3 Robust Controller Design

The increasing deployment of standalone photovoltaic PV-based electric vehicle charging systems has created a strong demand for converter architectures

capable of simultaneously handling multiple energy ports, bidirectional power flow, and high operational reliability. In such applications, the power interface must coordinate the PV source, energy storage unit, load terminal, and auxiliary charging/discharging paths within a single compact topology. A four-port fault-tolerant DC-DC converter provides an effective solution by enabling integrated power management with reduced conversion stages, improved efficiency, and enhanced flexibility under varying operating conditions.

Despite these advantages, multiport converter systems are inherently sensitive to structured uncertainties arising from parameter deviations and switching non-idealities. These uncertainties typically originate from inductance tolerance, capacitor aging, parasitic resistance variation, battery internal impedance change, and fluctuations in PV operating conditions due to irradiance and temperature variations. Since these perturbations are associated with identifiable system parameters, they constitute structured uncertainties whose locations in the mathematical model are known, while their exact magnitudes remain uncertain.

The control challenge becomes more significant in a four-port converter because the system dynamics vary according to the active power-flow mode. In the proposed topology, four operating states are defined to satisfy different energy management requirements. Each state represents a distinct switching configuration and corresponding power transfer mechanism. Therefore, the converter behaves as a multi-mode nonlinear system, where plant dynamics, control objectives, and disturbance sensitivity change from one operating state to another. To ensure high-performance operation across the full operating range, dedicated robust controllers have been developed for each major operating mode, except *state III*, which corresponds to the load-sharing condition. In this mode, independent controller synthesis is not required because the operating mechanism is inherently realized through the coordinated interaction of *states I* and *IV*.

This mode-dependent behavior makes conventional fixed-gain controllers inadequate, since a controller tuned for one state may exhibit degraded transient response, poor disturbance rejection, or insufficient stability margins in another state. In power electronic converters operating at high switching frequency, such

performance deterioration can lead to excessive current ripple, voltage regulation error, loss of efficiency, thermal stress, and, in severe cases, instability.

The motivation for applying robust control methodologies is to guarantee closed-loop stability and desired dynamic performance despite these structured uncertainties and mode transitions. Robust control design explicitly considers bounded parameter variation and worst-case operating conditions rather than relying solely on nominal plant models. An additional and critical motivation is the requirement for fault-tolerant operation under OCSF conditions. In practical converters, semiconductor switches are among the most failure-prone components due to thermal cycling, overvoltage stress, and repetitive switching operation. An *OCSF* can significantly alter current paths and converter dynamics, leading to reduced power transfer capability or abnormal voltage stress if not properly managed. Accordingly, the system analysis has been carried out under two principal operating conditions:

6.3.1 Under Healthy Conditions

The operation of the TMMFT converter is defined as healthy when it operates normally with all switching devices functioning. The steady-state switching characteristics under healthy conditions are presented in **Chapter 5**. Robust controllers are designed to ensure accurate voltage/current regulation, fast transient response, and stable operation across all applicable states.

6.3.1.1 System Design

The SSM obtained in (A4.14) for *state I* operation is used to derive the open-loop transfer functions (OLTF) $\hat{v}_{C01}/\hat{d}_1$, $\hat{v}_{bat}/\hat{d}_2$ and $\hat{v}_{C02}/\hat{d}_3$, respectively. Utilizing the system parameters with ESRs specified in Table 6.1, and the steady-state values obtained from the experimental setup such as duty cycles, corresponding inductor currents, voltages, and load resistances the following steady state nominal values are considered: $D_1 = 0.333$, $D_2 = 0.438$, $D_3 = 0.25$, $I_{Ls1} = 0.8039$ A, $I_{Ls2} = 0.8527$ A, $I_{Lb1} = 0.5324$ A, $I_{Lb2} = 0.4681$ A, $I_{L02} = 0.3056$ A, $V_{01} = 59.04$ V, $V_{bat} = 25.01$ V, $V_{02} = 13.75$ V, with corresponding load resistances $R_{01} = 100$ Ω , $R_{02} = 45$ Ω , and $R_{03} = 25$ Ω . The decrease in steady-state voltages is due to system ESRs. Based on these parameters and operational conditions, the TFs are derived as per [64] and are expressed in (6.10). Similarly, for *state II*, in the absence of MVDC load with steady-state parameters I_{Ls1}

= 0.3620 A, $I_{Ls2} = 0.4110$, and the rest of the parameters are similar to *state* I. The TFs are derived and presented in (6.11). In *state* III under load sharing, the SSM obtained in (A4.21) is used to derive TFs and presented in (6.12). The experimental data at steady-state conditions are considered as: $D_1 = 0.5416$, $D_2 = 0.6$, $D_3 = 0.85$, $I_{Ls1} = 1.0556$ A, $I_{Ls2} = 1.1235$ A, $I_{Lb1} = -0.3146$ A, $I_{Lb2} = -0.2860$ A, $I_{L02} = 0.3081$ A, $V_{01} = 58.1006$ V, $V_{bat} = 24$ V, $V_{02} = 13.8608$ V, with corresponding load resistances $R_{01} = 50 \Omega$ and $R_{02} = 45 \Omega$. In *state* IV under battery discharging, the SSM obtained in (A4.27) is used to derive the TFs and presented in (6.13). The experimental data at steady-state conditions are considered as: $D_2 = 0.5967$, $D_3 = 0.8366$, $I_{Lb1} = -0.8701$ A, $I_{Lb2} = -0.7822$ A, $I_{L02} = 0.3064$ A, $V_{01} = 57.63$ V, $V_{bat} = 24.2$ V, $V_{02} = 13.78$ V, with corresponding load resistances $R_{01} = 100 \Omega$ and $R_{02} = 45 \Omega$.

The closed-loop control for output port-1 is shown in Figure 6.3. The *state logic* for the state selection of different operating states is given in [64]. The OLTFs of all states are presented in (6.10) -(6.13), with open-loop poles in the left half of the *s*-plane, indicating a stable system. However, the boost operating side exhibits non-minimum phase behaviour due to a right-half plane (RHP) open-loop zero [73], necessitating PI compensation for stability. System uncertainties are included with the nominal plant to reflect real-time variations and ensure robust performance. Figure 6.3 shows boost operation considering uncertainties in load R_{01} , input voltage (V_{pv}), and battery voltage (V_{bat}). The minimum, maximum, and nominal limits for load R_{01} , input voltage V_{pv} , and battery voltage V_{bat} are considered as [50, 200, 100] Ω , [38, 42, 40] V, and [18, 26, 24.2] V, respectively.

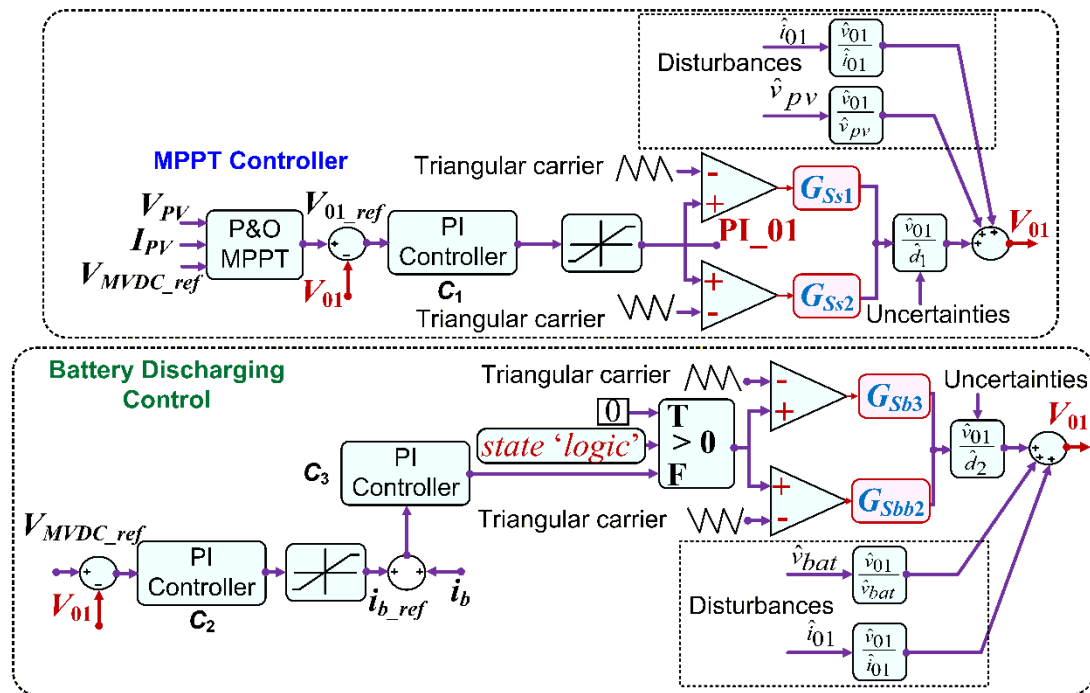


Figure 6.3 Closed-loop control of output port-1 of the TMMFT converter under disturbances and uncertainties.

Table 6.1
SYSTEM SPECIFICATIONS

Parameters		Designed Values
DC bus voltages (V_{01} / V_{02})		60 V / 15 V
Battery voltage (V_{bat}) / capacity (Ah)		24 V / 8 Ah
Inductors	$L_{s1} \approx L_{s2} \approx L_{b1} \approx L_{b2}$ / $r_{s1} \approx r_{s2} \approx r_{b1} \approx r_{b2}$	560 μ H / 0.32 Ω
	L_{02} / r_{02}	1.0 mH / 0.33 Ω
Capacitors	$C_{pv}/C_{01}/C_{02}/C_{fb}$	100/220/100/22 μ F
	$(r_{cpv}/r_{c01}/r_{c02}/r_{cfb})$	(0.33/0.33/0.33/0.27) Ω
Switches and diodes drop		0.7 V / 0.4 V
Switching frequency		20 kHz

6.3.1.2 Stability Boundary Locus

The stability boundary locus method evaluates controller parameters by solving the characteristic equation (CE) at each frequency ω , enabling identification of stable K_p , K_i regions [15], [104]. Using this approach, the locus denoted as $l(K_p, K_i, \omega)$ facilitates the identification of stable controller parameter regions. The values of K_p and K_i are designed for optimal TFs using (6.10), (6.11), and (6.13) in terms of ω , which is given in (6.14), (6.15), and (6.16), respectively.

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_1} \right|_{s-I|\hat{v}_{pv},\hat{d}_2,\hat{d}_3=0} = \frac{-0.4955s^8 + 3.62 \times 10^4 s^7 + 2.72 \times 10^8 s^6 + 1.60 \times 10^{13} s^5 + 8.87 \times 10^{16} s^4 + 3.13 \times 10^{20} s^3 + 8.47 \times 10^{23} s^2 + 9.79 \times 10^{26} s + 3.57 \times 10^{29}}{D_{num_S-I}} \quad (6.10a)$$

$$\left. \frac{\hat{v}_{c02}(s)}{\hat{d}_3} \right|_{s-I|\hat{v}_{pv},\hat{d}_1,\hat{d}_2=0} = \frac{1.733 \times 10^4 s^7 + 7.22 \times 10^8 s^6 + 1.132 \times 10^{13} s^5 + 2.329 \times 10^{17} s^4 + 5.647 \times 10^{20} s^3 + 7.66 \times 10^{23} s^2 + 6.74 \times 10^{26} s + 2.35 \times 10^{28}}{D_{num_S-I}} \quad (6.10b)$$

$$\left. \frac{\hat{v}_{bat}(s)}{\hat{d}_2} \right|_{s-I|\hat{v}_{pv},\hat{d}_1,\hat{d}_3=0} = \frac{6.31 \times 10^4 s^7 + 2.12 \times 10^{10} s^6 + 7.35 \times 10^{13} s^5 + 3.36 \times 10^{17} s^4 + 6.78 \times 10^{20} s^3 + 8.37 \times 10^{23} s^2 + 7.02 \times 10^{26} s + 2.41 \times 10^{29}}{D_{num_S-I}}$$

Where,

$$D_{num_S-I} = s^8 + 9237s^7 + 3.92 \times 10^8 s^6 + 1.36 \times 10^{12} s^5 + 5.91 \times 10^{15} s^4 + 1.18 \times 10^{19} s^3 + 1.44 \times 10^{22} s^2 + 1.19 \times 10^{25} s + 4.07 \times 10^{27} \quad (6.10c)$$

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_1} \right|_{s-II|\hat{v}_{pv},\hat{d}_2,\hat{d}_3=0} = \frac{-0.2319s^8 + 3.91 \times 10^4 s^7 + 3.78 \times 10^8 s^6 + 1.65 \times 10^{13} s^5 + 9.06 \times 10^{16} s^4 + 3.17 \times 10^{20} s^3 + 8.52 \times 10^{23} s^2 + 9.81 \times 10^{26} s + 3.57 \times 10^{29}}{D_{num_S-II}} \quad (6.11a)$$

$$\left. \frac{\hat{v}_{c02}(s)}{\hat{d}_3} \right|_{s-II|\hat{v}_{pv},\hat{d}_1,\hat{d}_2=0} = \frac{1.737 \times 10^4 s^7 + 7.24 \times 10^8 s^6 + 1.13 \times 10^{13} s^5 + 2.33 \times 10^{17} s^4 + 5.65 \times 10^{20} s^3 + 7.66 \times 10^{23} s^2 + 6.76 \times 10^{26} s + 2.36 \times 10^{29}}{D_{num_S-II}} \quad (6.11b)$$

$$\left. \frac{\hat{v}_{bat}(s)}{\hat{d}_2} \right|_{s-II|\hat{v}_{pv},\hat{d}_1,\hat{d}_3=0} = \frac{6.31 \times 10^4 s^7 + 2.12 \times 10^{10} s^6 + 7.34 \times 10^{13} s^5 + 3.36 \times 10^{17} s^4 + 6.76 \times 10^{20} s^3 + 8.35 \times 10^{23} s^2 + 7.02 \times 10^{26} s + 2.42 \times 10^{29}}{D_{num_S-II}}$$

Where,

$$D_{num_S-II} = s^8 + 9232s^7 + 3.92 \times 10^8 s^6 + 1.36 \times 10^{12} s^5 + 5.9 \times 10^{15} s^4 + 1.17 \times 10^{19} s^3 + 1.44 \times 10^{22} s^2 + 1.2 \times 10^{25} s + 4.09 \times 10^{27} \quad (6.11c)$$

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_1} \right|_{s-III|\hat{v}_{pv},\hat{v}_{bat},\hat{d}_2,\hat{d}_3=0} = \frac{-0.6498s^7 + 2.387 \times 10^4 s^6 + 1.56 \times 10^8 s^5 + 5.94 \times 10^{11} s^4 + 1.74 \times 10^{15} s^3 + 2.40 \times 10^{18} s^2 + 1.4 \times 10^{21} s + 2.84 \times 10^{23}}{D_{num_S-III}} \quad (6.12a)$$

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_2} \right|_{s-III|\hat{v}_{pv},\hat{v}_{bat},\hat{d}_1,\hat{d}_3=0} = \frac{-0.0873s^7 + 2.86 \times 10^4 s^6 + 1.74 \times 10^8 s^5 + 6.04 \times 10^{11} s^4 + 1.61 \times 10^{15} s^3 + 2.11 \times 10^{18} s^2 + 1.18 \times 10^{21} s + 2.32 \times 10^{23}}{D_{num_S-III}} \quad (6.12b)$$

$$\left. \frac{\hat{v}_{c02}(s)}{\hat{d}_3} \right|_{s-III|\hat{v}_{pv},\hat{v}_{bat},\hat{d}_1,\hat{d}_2=0} = \frac{1.752 \times 10^4 s^6 + 6.38 \times 10^8 s^5 + 1.88 \times 10^{12} s^4 + 2.76 \times 10^{15} s^3 + 2.53 \times 10^{18} s^2 + 1.22 \times 10^{21} s + 2.28 \times 10^{23}}{D_{num_S-III}}$$

Where,

$$D_{num_S-III} = s^7 + 3968s^6 + 1.74 \times 10^7 s^5 + 3.93 \times 10^{10} s^4 + 5.25 \times 10^{13} s^3 + 4.51 \times 10^{16} s^2 + 2.12 \times 10^{19} s + 3.90 \times 10^{21}$$

(6.12c)

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_2} \right|_{s=IV|\hat{v}_{bat}, \hat{d}_3=0} = \frac{-0.3925s^5 + 1.82 \times 10^4 s^4 + 8.75 \times 10^7 s^3 + 3.41 \times 10^{11} s^2 + 9.53 \times 10^{14} s + 5.55 \times 10^{17}}{s^5 + 2405s^4 + 1.25 \times 10^7 s^3 + 1.66 \times 10^{10} s^2 + 1.14 \times 10^{13} s + 4.00 \times 10^{15}}$$

(6.13a)

$$\left. \frac{\hat{v}_{c02}(s)}{\hat{d}_3} \right|_{s=IV|\hat{v}_{bat}, \hat{d}_2=0} = \frac{1.738 \times 10^4 s^4 + 6.06 \times 10^8 s^3 + 8.94 \times 10^{11} s^2 + 6.45 \times 10^{14} s + 2.31 \times 10^{17}}{s^5 + 2405s^4 + 1.25 \times 10^7 s^3 + 1.66 \times 10^{10} s^2 + 1.14 \times 10^{13} s + 4.00 \times 10^{15}}$$

(6.13b)

$$K_p \left(\frac{\hat{v}_{c01}}{\hat{d}_1} \right) \Big|_{S-I} = \frac{0.4955\omega^{16} - 2.568 \times 10^8 \omega^{14} + 4.01 \times 10^{15} \omega^{12} + 1.228 \times 10^{25} \omega^{10} - 2.392 \times 10^{32} \omega^8 + 1.229 \times 10^{39} \omega^6 + 5.698 \times 10^{44} \omega^4 - 3.108 \times 10^{51} \omega^2 - 1.453 \times 10^{57}}{D_{num} \Big|_{K_S-I}}$$

(6.14a)

$$K_i \left(\frac{\hat{v}_{c01}}{\hat{d}_1} \right) \Big|_{S-I} = \frac{4577\omega^{16} + 1.839 \times 10^{12} \omega^{14} - 1.183 \times 10^{21} \omega^{12} + 1.315 \times 10^{29} \omega^{10} - 2.2 \times 10^{36} \omega^8 + 1.151 \times 10^{43} \omega^6 - 1.432 \times 10^{49} \omega^4 + 4.262 \times 10^{54} \omega^2 - 3.987 \times 10^{54}}{D_{num} \Big|_{K_S-I}}$$

Where,

$$D_{num} \Big|_{K_S-I} = 0.2455\omega^{16} + 1.579 \times 10^9 \omega^{14} - 1.169 \times 10^{18} \omega^{12} + 2.297 \times 10^{26} \omega^{10} - 1.713 \times 10^{33} \omega^8 - 2.162 \times 10^{40} \omega^6 + 1.693 \times 10^{47} \omega^4 + 3.544 \times 10^{53} \omega^2 + 1.274 \times 10^{59}$$

(6.14b)

$$K_p \left(\frac{\hat{v}_{c01}}{\hat{d}_1} \right) \Big|_{S-II} = \frac{0.2319\omega^{16} - 7.332 \times 10^7 \omega^{14} - 3.238 \times 10^{16} \omega^{12} + 1.286 \times 10^{25} \omega^{10} - 2.411 \times 10^{32} \omega^8 + 1.221 \times 10^{39} \omega^6 + 5.743 \times 10^{44} \omega^4 - 3.11 \times 10^{51} \omega^2 - 1.458 \times 10^{57}}{D_{num} \Big|_{K_S-II}}$$

(6.15a)

$$K_i \left(\frac{\hat{v}_{c01}}{\hat{d}_1} \right) \Big|_{S-II} = \frac{2141\omega^{16} + 3.178 \times 10^{12} \omega^{14} - 1.346 \times 10^{21} \omega^{12} + 1.351 \times 10^{29} \omega^{10} - 2.225 \times 10^{36} \omega^8 + 1.156 \times 10^{43} \omega^6 - 1.437 \times 10^{49} \omega^4 + 4.264 \times 10^{54} \omega^2 - 4.00 \times 10^{54}}{D_{num} \Big|_{K_S-II}}$$

Where,

$$D_{num} \Big|_{K_S-II} = 0.05378\omega^{16} + 1.701 \times 10^9 \omega^{14} - 1.188 \times 10^{18} \omega^{12} + 2.288 \times 10^{26} \omega^{10} - 1.701 \times 10^{33} \omega^8 - 2.153 \times 10^{40} \omega^6 + 1.683 \times 10^{47} \omega^4 + 3.534 \times 10^{53} \omega^2 + 1.273 \times 10^{59}$$

(6.15b)

$$K_p \left(\frac{\hat{v}_{c01}}{\hat{d}_2} \right) \Big|_{S-IV} = \frac{0.3925\omega^{10} + 3.886 \times 10^7 \omega^8 - 9.213 \times 10^{14} \omega^6 + 5.859 \times 10^{21} \omega^4 - 3.229 \times 10^{26} \omega^2 - 2.22 \times 10^{33}}{D_{num} \Big|_{K_S-IV}}$$

(6.16a)

$$K_i \left(\hat{v}_{c01} / \hat{d}_2 \right) \Big|_{S-IV} = \frac{18200\omega^{10} - 5.69 \times 10^{11} \omega^8 + 5.034 \times 10^{18} \omega^6 - 1.084 \times 10^{25} \omega^4 + 6.336 \times 10^{30} \omega^2 - 3.814 \times 10^{30}}{D_{num} \Big|_{K-S-IV}} \quad (6.16b)$$

Where,

$$D_{num} \Big|_{K-S-IV} = 0.1541\omega^{10} + 3.998 \times 10^8 \omega^8 - 5.507 \times 10^{15} \omega^6 - 3.015 \times 10^{22} \omega^4 + 5.295 \times 10^{29} \omega^2 + 3.075 \times 10^{35}$$

The stability region given in Figure 6.4 and Figure 6.5 are plotted using Kharitonov's 16 plant theorem. The region in Figures 6.4(a) and (b) is generated by taking uncertainty as mentioned above, while Figures 6.5(a), (b) and (c) illustrate the robust performance region (RPR) obtained by including $\pm 10\%$ variations in the values of L_{s1} , L_{s2} and C_{01} for *states* I and II, and L_{b1} , L_{b2} and C_{01} for *state* IV, respectively. Since *state* III corresponds to a load-sharing mode, and its controller parameters are similar to those of *states* I and IV, a separate robustness analysis for this state is not required, and its performance is implicitly covered within the derived RPRs. As shown in Figure 6.5(a), the RPRs of *states* I and II overlap; however, the admissible region for *state* I is considerably smaller, as highlighted in the zoomed view in Figure 6.5(b). Selecting K_p - K_i pairs from this narrow region led to slow the system dynamics. Therefore, for the first three states, the controller gains are selected without incorporating inductor and capacitor uncertainties. In contrast, for *state* IV, the gain values are intentionally increased after evaluating the effect of parameter uncertainties, ensuring sufficient robustness during the battery discharging mode, as shown in Figure 6.5(c). The intersection of the stability regions corresponding to all 16 Kharitonov plants defines the controller's RPR. Any selection of K_p and K_i within this region ensures robust stability of the system across the entire range of modelled uncertainties. Controller C_1 regulates the output voltage V_{01} during operating *state* I and *state* II. The controller design plots are individually generated for the corresponding plants (6.10a) and (6.11a), as shown in Figure 6.5(a). The common intersecting region in Figure 6.5(a) is utilized to determine suitable values for the K_p and K_i , ensuring robust performance across both operating conditions.

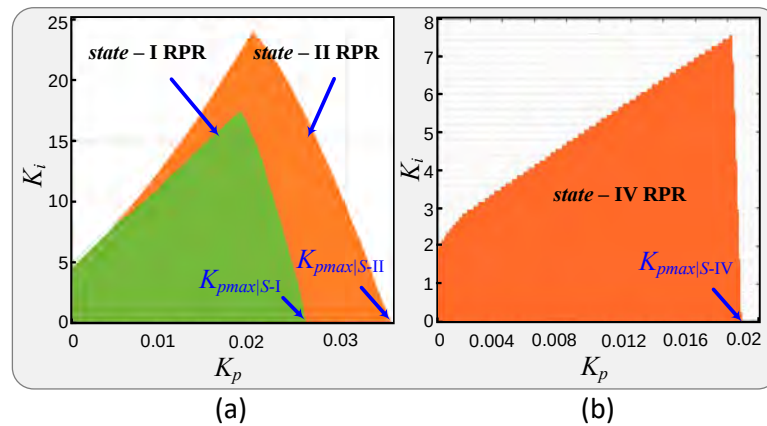


Figure 6.4 Kharitonov's 16-plant overlapped robust stable boundary locus for (a) *state I*, *state II*, (b) robust stable boundary locus for *state IV*, under healthy conditions.

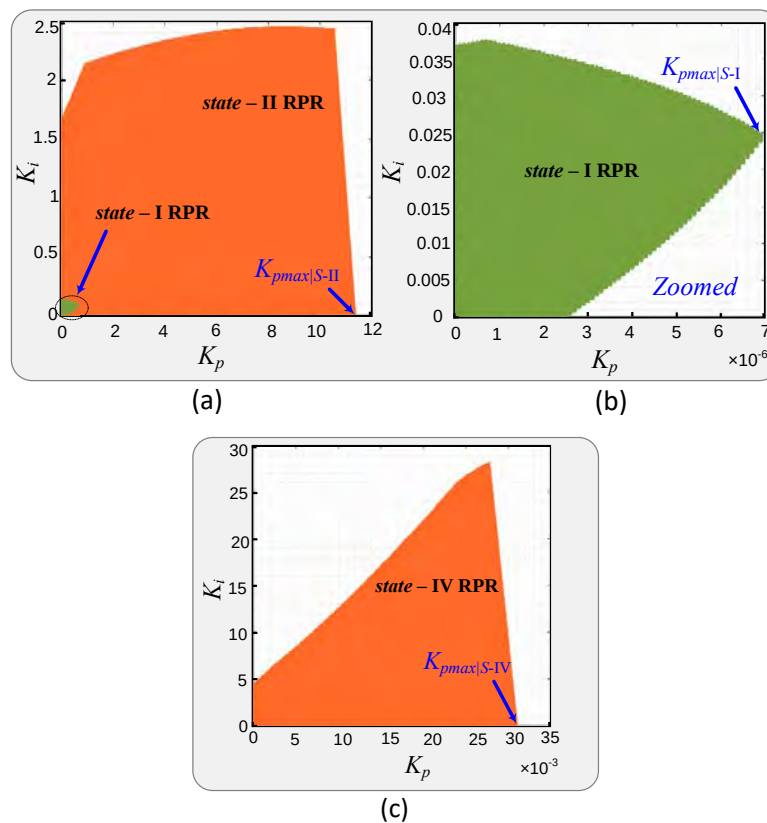


Figure 6.5 Kharitonov's 16 plant overlapped robust stable boundary locus for (a) *state I*, *state II*, by taking uncertainties including L_{S1} , L_{S2} and C_{01} , (b) robust stable boundary locus for *state I*, by taking uncertainties including L_{S1} , L_{S2} and C_{01} , zoomed version (c) robust stable boundary locus for *state IV*, by taking uncertainties including L_{b1} , L_{b2} and C_{01} , under healthy conditions.

Figures 6.6(a) and (b) present the Bode plots of the OLTFs. The solid lines represent uncompensated systems, whereas dashed lines depict the compensated

response of the designed PI controller. Blue, cyan, and magenta curves correspond to *states* I, II, and III in Figure 6.6(a), respectively, while in Figure 6.6(b), blue and cyan denote *states* III and IV, respectively. The compensation significantly improves phase margins (PMs) and stabilizes the system across varying operating points. PMs for the compensated systems increase to 36.9° , 37.3° , and 41.7° , while the corresponding gain margins (GMs) reach to 38.6 dB, 41 dB, and 47.6 dB for *state* I, *state* II, and *state* III in Figure 6.6(a), respectively. Further, PMs increase from 45.7° and 47° to 60.7° and 81° for *state* III and *state* IV, respectively. The observed rightward shift in gain crossover frequencies (ω_{gc}) indicates broader system bandwidth, implying faster transient responses and improved dynamic characteristics across all evaluated operating conditions.

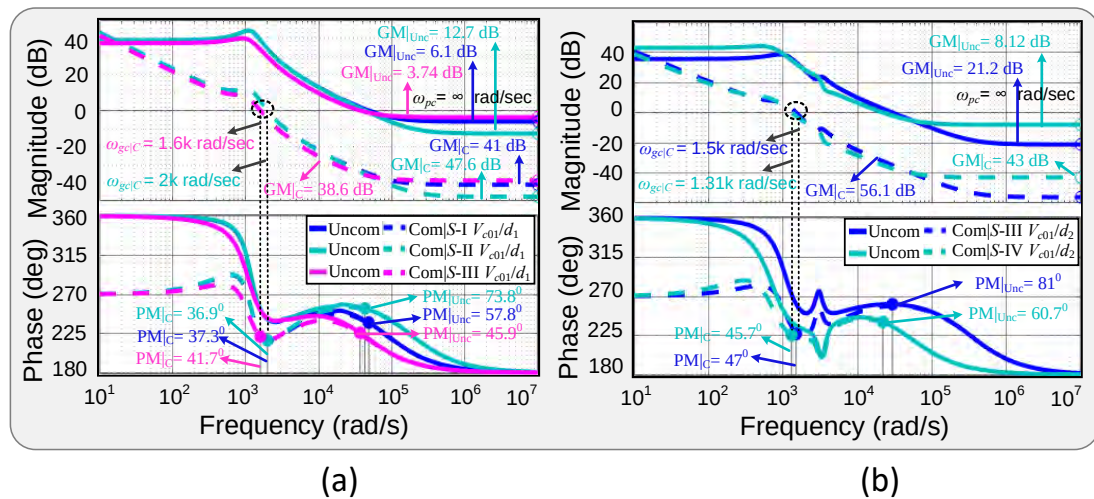


Figure 6.6 Comparative performance analysis in the frequency domain under healthy conditions, (a) Bode plots for *state* I, *state* II, and *state* III of the TFs $\hat{v}_{c01}/\hat{d}_1$, (b) Bode plots *state* III and *state* IV of the TFs $\hat{v}_{c01}/\hat{d}_2$.

Figures 6.7(a) and (b) show the Nyquist plots for the compensated transfer functions corresponding to the frequency-domain analysis of Figures 6.6(a) and (b). In both plots, the system trajectories maintain a safe distance from the critical point $(-1, 0)$, validating closed-loop stability under the Nyquist criterion. The provided delay margins further confirm adequate damping and robust stability. Also, the zoomed-in view in each plot shows clarity on system trajectories near the ω_{gc} .

Figure 6.8(a) to Figure 6.8(d) present a comparative step-response analysis of the conventional and proposed PI controllers under three distinct gain selection

7

strategies. *Case-1*: the PI gains are selected on a heuristic trial-and-error basis, with fixed values $K_p = 0.1$ and $K_i = 150$ applied uniformly across all operating states. *Case-2*: the controller gains are chosen from the RPR obtained by incorporating $\pm 10\%$ variations in inductors L_{s1} , L_{s2} and capacitor C_{01} for *states* I and II, and in L_{b1} , L_{b2} and C_{01} for *state* IV. Accordingly, the gains are set as $K_p = 3 \times 10^{-6}$ and $K_i = 0.03$ for the first three states, and $K_p = 0.018$ and $K_i = 15$ for *state* IV. *Case-3*: corresponds to the optimized PI gains selected from the nominal RPR regions shown in Figures 6.4(a) and (b).

In all cases, the output voltage V_{01} accurately tracks the 60 V reference. For case 1, the response exhibits a faster rise time but is accompanied by pronounced overshoot and a relatively short settling duration. In case 2, the system response is

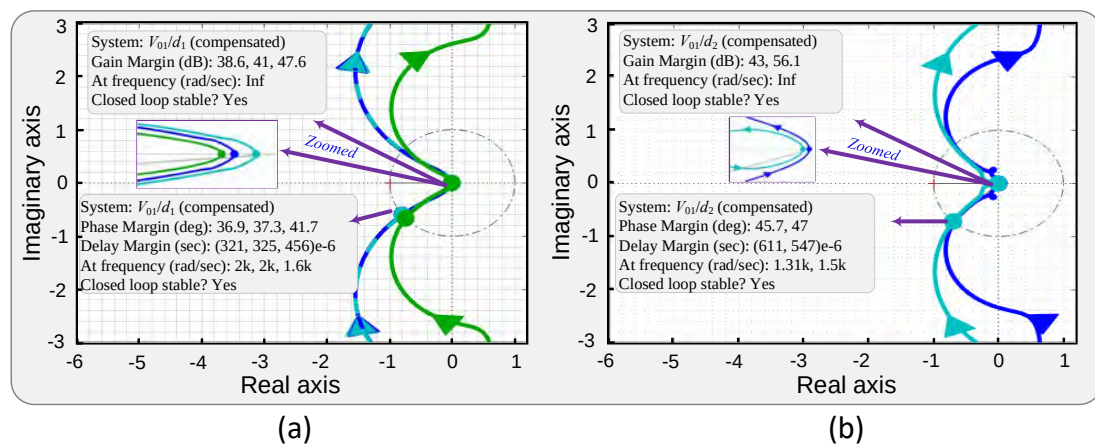
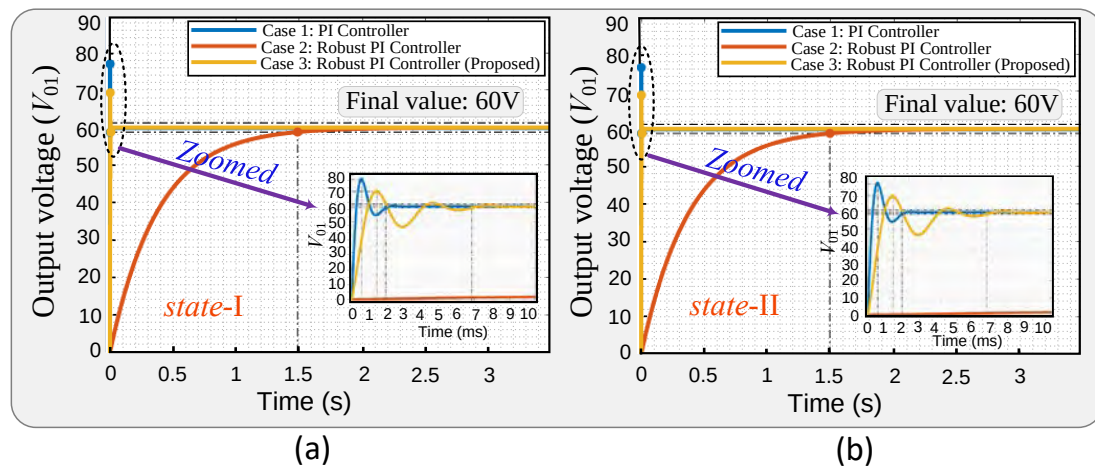


Figure 6.7 Comparative performance analysis in the frequency domain under healthy conditions, (a) Nyquist plots for *state* I, *state* II, and *state* III of the TFs $\hat{v}_{c01}/\hat{d}_1$, (b) Nyquist plots for the *state* III and *state* IV of the TFs $\hat{v}_{c01}/\hat{d}_2$.



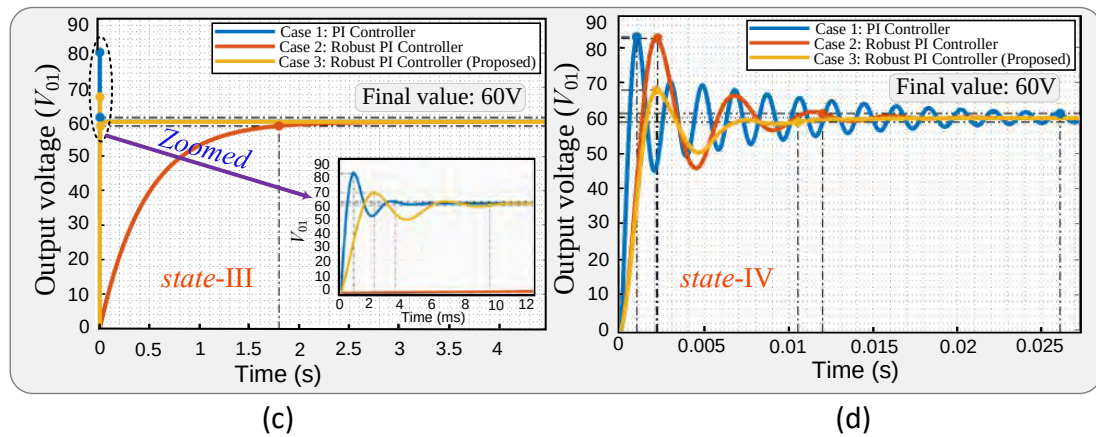


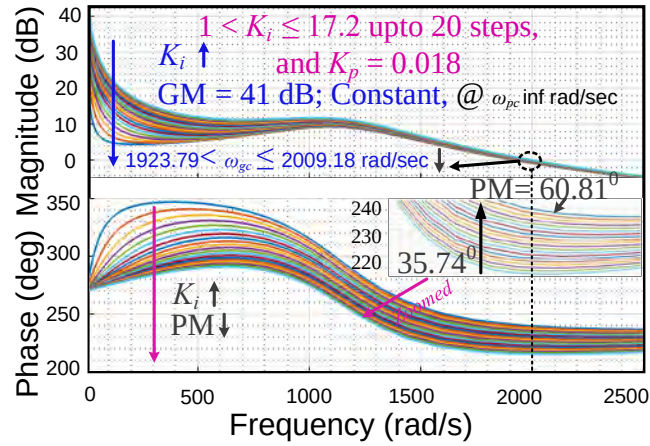
Figure 6.8 Comparative analysis of the step response for the conventional and proposed PI controllers of the TFs $\hat{v}_{c01}/\hat{d}_1$, and $\hat{v}_{c01}/\hat{d}_2$ for (a) *state I*, (b) *state II*, (c) *state III*, and (d) *state IV*.

nearly critically damped for the first three operating states, resulting in significantly slower dynamics compared to cases 1 and 3, while *state IV* exhibits a comparatively higher overshoot. In contrast, the proposed controller (case 3) achieves minimal overshoot, fast rise time, and short settling duration, as evident from the zoomed-in responses, which can be further validated through experimental results. The well-damped responses demonstrate that the controller not only stabilizes the system but also ensures excellent transient performance. These results confirm the effectiveness of the proposed PI compensation strategy in delivering precise voltage regulation and fast dynamic response.

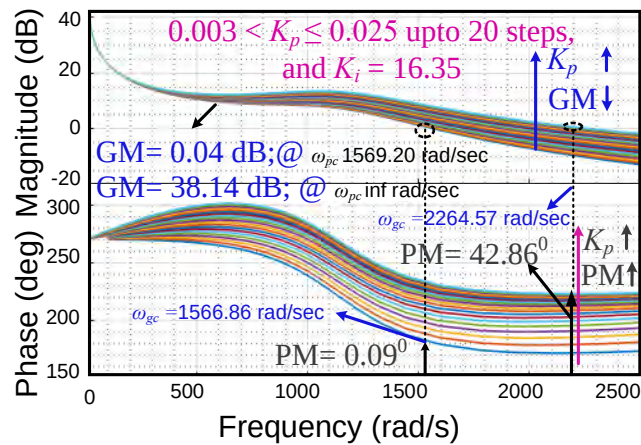
6.3.1.3 Selection of K_p and K_i

From Figure 6.4(a), it can be seen that the RPR region of *state I* lie over the RPR region of *state II*, so the selection of K_p - K_i parameters for the controller C_1 can be done independently of the RPR of *state I*, since it is the common intersection of these two *states*, and K_p - K_i selection for the controller C_3 can be done from the RPR of *state IV*, as given in Figure 6.4(b). Within the range of K_p and K_i as given in Figures 6.4(a) and (b), the optimal combination of K_p and K_i values is identified through frequency-domain analysis as shown in Figures 6.9(a), (b) for *state I* and Figures 6.9(c), (d) for *state IV*. In Figures 6.9(a) and (c), K_p is fixed at 0.018 while K_i is varied up to 20 steps. The analysis reveals that increasing K_i results in a decreasing PM, while

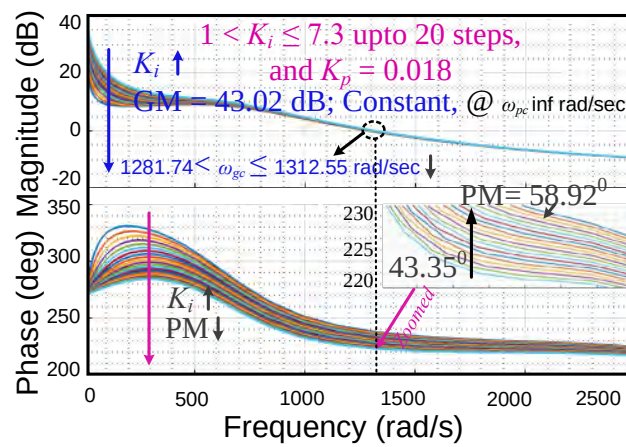
the GM remains nearly constant at 41 dB and 43.02 dB for *states* I and IV, respectively, with ω_{pc} approaching infinity.



(a)



(b)



(c)

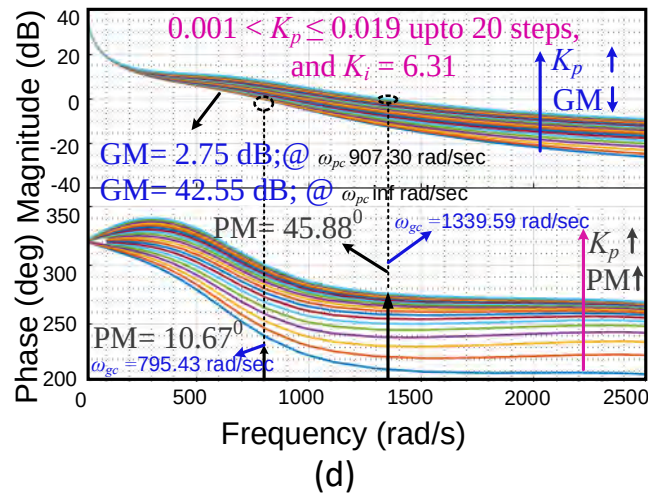


Figure 6.9 Selection of K_p - K_i value using frequency domain analysis with (a) $K_p = 0.018$, K_i variable, and (b) $K_i = 16.35$, K_p variable for *state I*, (c) $K_p = 0.018$, K_i variable, (d) $K_i = 6.31$, K_p variable for *state IV*

6.3.1.4 Sensitivity analysis

Figure 6.10(a) to Figure 6.10(d) present the sensitivity and complementary sensitivity characteristics for all operating *states*, with the selected parameters of K_p - K_i values derived from (6.17) and (6.18), where $i = 1$ for *states I*, II, and III, and $i = 2$ for *state IV*. For *state I* (Figure 6.10(a)), the peak values of $|S(s)|$ and $|T(s)|$ are 1.667 and 1.635, respectively. In *state II* (Figure 6.10(b)), these values decrease slightly to 1.645 and 1.620, respectively. In *state III* (Figure 6.10(c)), it exhibits a further reduction, with peak values of 1.591 and 1.413, respectively. *State IV* (Figure 6.10(d)) demonstrates the lowest peaks, with $|S(s)| = 1.471$ and $|T(s)| = 1.311$. Since $|S(s)| < 2$ is widely considered a robustness criterion [104], all four *states* satisfy this requirement. Moreover, the decreasing value of $|T(s)|$ highlights improved attenuation of high-frequency disturbances and enhanced system stability.

$$|S(s)| = \left| \frac{1}{1 + (\hat{v}_{c01}(s)/\hat{d}_i)} \right| \quad (6.17)$$

$$|T(s)| = \left| \frac{(\hat{v}_{c01}(s)/\hat{d}_i)}{1 + (\hat{v}_{c01}(s)/\hat{d}_i)} \right| \quad (6.18)$$

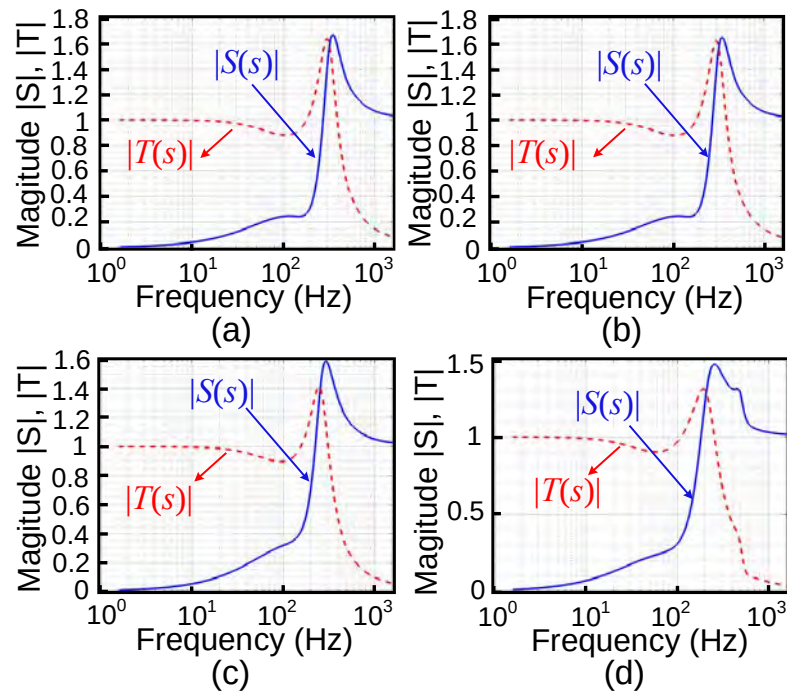


Figure 6.10 Sensitivity and complementary function under healthy conditions for (a) *state I*, (b) *state II*, (c) *state III*, and (d) *state IV*.

6.3.2 Under Open Circuit Switch Fault Conditions

The converter experiences an OCSFs, resulting in modified switching sequences and altered state-space dynamics. Under this condition, the fault-tolerant capability of the converter, together with robust control action, enables continued operation with acceptable performance degradation. By separating the study into healthy and OCSF scenarios, the practical resilience of the proposed converter can be comprehensively evaluated under both nominal and faulted environments. The steady-state switching characteristics under OCSF conditions are shown in Figure 6.11.

6.3.2.1 System Design

The SSMs are derived following the same procedure as in the healthy operating condition, by introducing faults in switches S_{S1} and S_{bb1} for *state I* and in S_{bb2} for *state IV*, respectively. These models are subsequently used to obtain the corresponding OLTFs $\hat{v}_{C01}/\hat{d}_1$ and $\hat{v}_{C01}/\hat{d}_2$. In *state I*, the perturbed state variables are $[i_{Ls2}, i_{Lb1}, i_{L02}, v_{C01}, v_{C02}, v_{Cfb}]^T$. The experimental data at steady-state conditions are considered as follows: $D_1 = 0.333$, $D_2 = 0.438$, $D_3 = 0.25$, $I_{Ls2} = 1.6355$ A, $I_{Lb1} = 0.9846$ A, $I_{L02} = 0.3026$ A, $V_{01} = 58.398$ V, $V_{bat} = 24.614$ V, $V_{02} = 13.62$ V, with corresponding load

resistances $R_{01} = 100 \, \Omega$, $R_{02} = 45 \, \Omega$, and $R_{03} = 25 \, \Omega$. Based on these parameters and operational conditions, the TFs that are derived are expressed in (6.19). Similarly, for *state* IV, the perturbed state variables are $[i_{Lb1}, i_{L02}, v_{C01}, v_{C02}]^T$. The experimental data at steady-state conditions are considered as follows: $D_2 = 0.5967$, $D_3 = 0.8467$, $I_{Lb1} = -1.597 \, \text{A}$, $I_{L02} = 0.3032 \, \text{A}$, $V_{01} = 56.83 \, \text{V}$, and $V_{02} = 13.65 \, \text{V}$, with corresponding load resistances $R_{01} = 100 \, \Omega$ and $R_{02} = 45 \, \Omega$. The TFs are derived and presented in (6.20).

6.3.2.2 Stability Boundary Locus

Using Kharitonov's theorem, the locus $l(K_p, K_i, \omega)$ facilitates the identification of stable controller parameter regions. The values of K_p and K_i are designed for optimal TFs using (6.19) and (6.20), respectively, in terms of ω , as given in (6.21) and (6.22). The RPR given in Figure 6.12(a) to Figure 6.12(d) are plotted using Kharitonov's 16-plant theorem. The regions in Figures 6.12(a) and (b) are generated by taking uncertainty as mentioned above, while Figures 6.12(c) and (d) illustrate the RPR obtained by including $\pm 10\%$ variations in the inductors L_{s2} and capacitor C_{01} for *state* I and L_{b1} and C_{01} for *state* IV, respectively. As shown in Figure 6.12, due to the OCSF condition, the $K_p - K_i$ range has been increased from their healthy condition operations. It is evident from the given Figure 6.4, Figure 6.5 and Figure 6.12 that the selected $K_p - K_i$ gain in healthy conditions lies within the RPR of the OCSF conditions. So, due to the OCSF, there is no impact on the controller gain as selected.

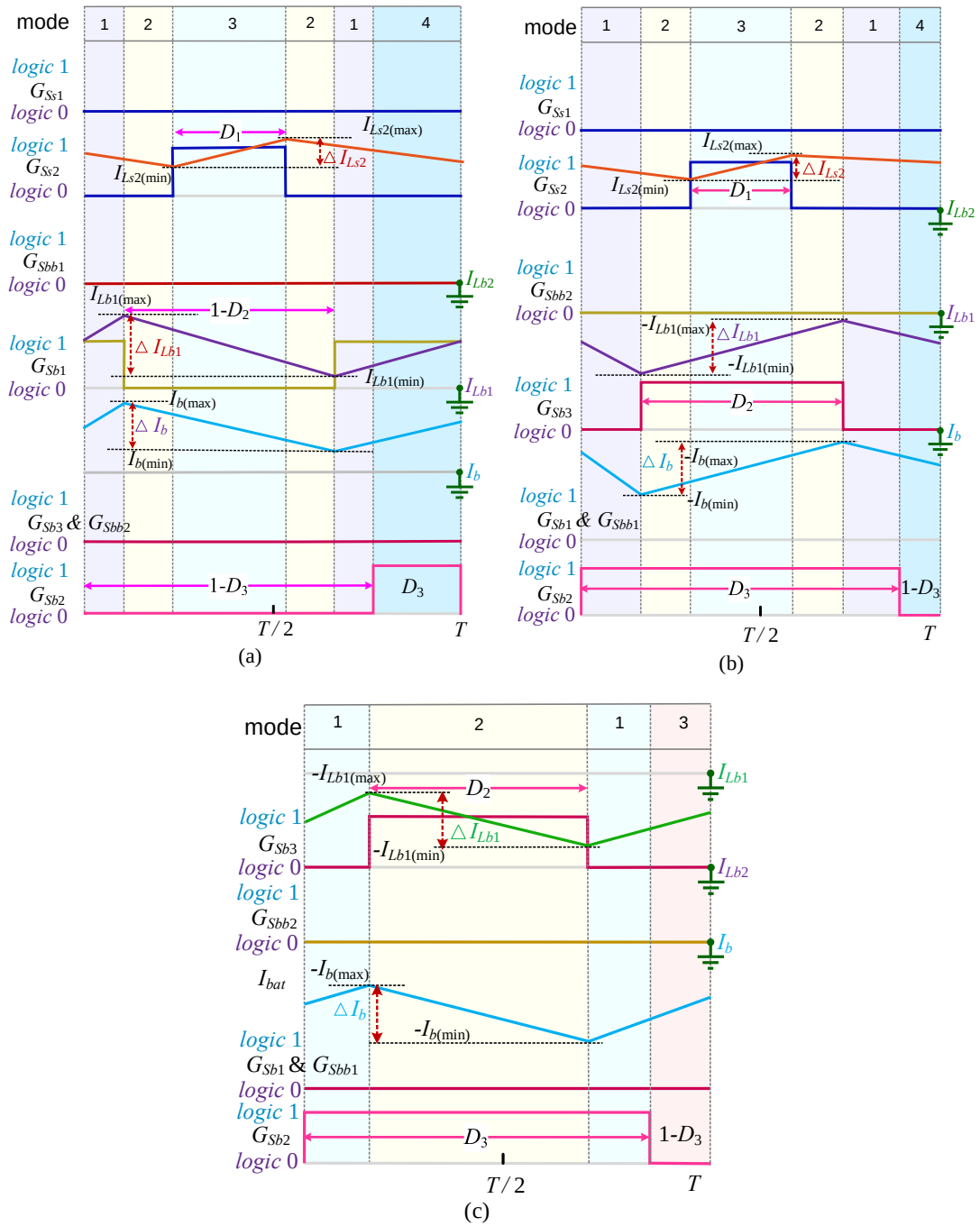


Figure 6.11 Switching characteristics under OCSF conditions for (a) state I, (b) state III, and (c) state IV operation.

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_1} \right|_{s=1, \hat{v}_{pv}, \hat{d}_2, \hat{d}_3=0} = \frac{-0.4892s^6 + 1.59 \times 10^4 s^5 + 7.91 \times 10^7 s^4 + 3.91 \times 10^{12} s^3 + 1.49 \times 10^{16} s^2 + 4.65 \times 10^{19} s + 1.105 \times 10^{23}}{s^6 + 7046s^5 + 2.01 \times 10^8 s^4 + 3.94 \times 10^{11} s^3 + 2.14 \times 10^{15} s^2 + 1.79 \times 10^{18} s + 1.31 \times 10^{21}} \quad (6.19)$$

$$\left. \frac{\hat{v}_{c01}(s)}{\hat{d}_2} \right|_{s=IV|\hat{v}_{bat}, \hat{d}_3=0} = \frac{-0.3870s^4 + 6010s^3 + 2.47 \times 10^7 s^2 + 1.27 \times 10^{11} s + 3.58 \times 10^{14}}{s^4 + 1654s^3 + 1.10 \times 10^7 s^2 + 7.88 \times 10^9 s + 2.70 \times 10^{12}} \quad (6.20)$$

$$K_p \left(\frac{\hat{v}_{c01}}{\hat{d}_1} \right) \Big|_{s=I} = \frac{0.4892\omega^{12} - 1.311 \times 10^8 \omega^{10} + 4.08 \times 10^{15} \omega^8 + 1.379 \times 10^{24} \omega^6}{-2.897 \times 10^{31} \omega^4 + 1.732 \times 10^{38} \omega^2 - 1.446 \times 10^{44}} \Big/ D'_{num} \Big|_{K-S-I} \quad (6.21a)$$

$$K_i \left(\frac{\hat{v}_{c01}}{\hat{d}_1} \right) \Big|_{s=I} = \frac{3447\omega^{12} + 3.644 \times 10^{11} \omega^{14} - 1.355 \times 10^{20} \omega^8 + 6.804 \times 10^{27} \omega^6}{-7.028 \times 10^{34} \omega^4 + 1.978 \times 10^{41} \omega^2 - 6.084 \times 10^{40}} \Big/ D'_{num} \Big|_{K-S-I}$$

Where,

$$D'_{num} \Big|_{K-S-I} = 0.2393\omega^{12} + 3.297 \times 10^8 \omega^{10} - 1.327 \times 10^{17} \omega^8 + 1.455 \times 10^{25} \omega^6 - 1.237 \times 10^{32} \omega^4 - 1.137 \times 10^{39} \omega^2 + 1.222 \times 10^{46} \quad (6.21b)$$

$$K_p \left(\frac{\hat{v}_{c01}}{\hat{d}_2} \right) \Big|_{s=IV} = \frac{0.3870\omega^8 + 1.045 \times 10^7 \omega^6 - 3.711 \times 10^{14} \omega^4 + 3.006 \times 10^{21} \omega^2 - 9.66 \times 10^{26}}{0.1498\omega^8 + 5.52 \times 10^7 \omega^6 - 1.193 \times 10^{15} \omega^4 - 1.563 \times 10^{21} \omega^2 + 1.279 \times 10^{29}} \quad (6.22a)$$

$$K_i \left(\frac{\hat{v}_{c01}}{\hat{d}_2} \right) \Big|_{s=IV} = \frac{640\omega^8 + 3.771 \times 10^{10} \omega^6 - 7.858 \times 10^{17} \omega^4 + 2.82 \times 10^{24} \omega^2 - 3.424 \times 10^{23}}{0.1498\omega^8 + 5.52 \times 10^7 \omega^6 - 1.193 \times 10^{15} \omega^4 - 1.563 \times 10^{21} \omega^2 + 1.279 \times 10^{29}} \quad (6.22b)$$

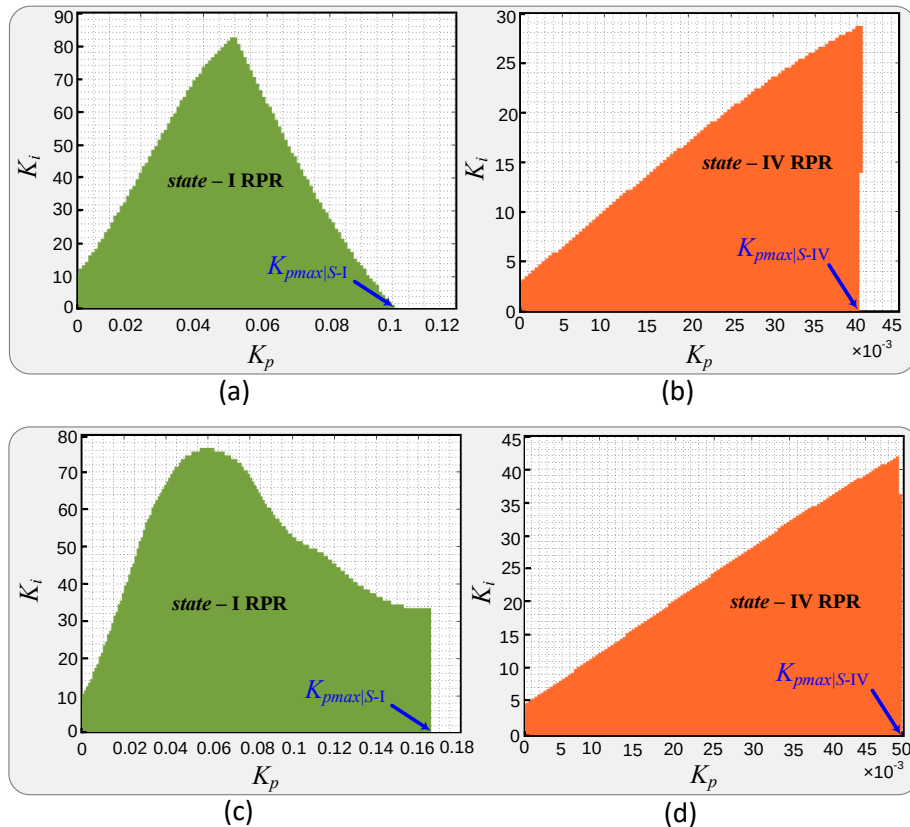


Figure 6.12 Comparative performance analysis in the frequency domain under *OCSF* condition Kharitonov's 16 plant robust stable boundary locus for (a) *state I*, (b) *state IV*, (c) *state I*, by taking uncertainties including L_{S2} and C_{01} , and (d) *state IV*, by taking uncertainties including L_{b1} and C_{01} .

6.3.2.3 Sensitivity analysis

Figure 6.13(a) to Figure 6.13(d) present the sensitivity and complementary sensitivity characteristics for all operating *states* under the OCSF condition, similar to the healthy condition. For *state* I, the peak values of $|S(s)|$ and $|T(s)|$ are 1.744 and 1.575, respectively, as shown in Figure 6.13(a). In *state* II, these values decrease slightly to 1.719 and 1.566, respectively (Figure 6.13(b)). In *state* III, a further reduction with peak values of 1.663 and 1.4, respectively (Figure 6.13(c)), and *state* IV demonstrates the lowest peaks, with $|S(s)| = 1.524$ and $|T(s)| = 1.289$, as shown in Figure 6.13(d). Since $|S(s)| < 2$ for all operating states under the OCSF condition, the selected controller gains ensure stable and robust control performance without significantly affecting the system operation.

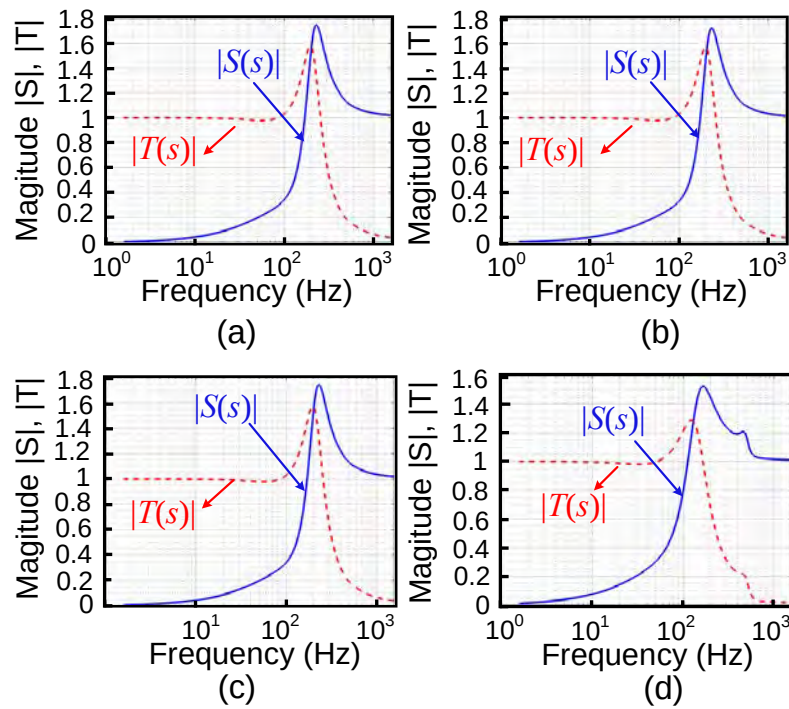


Figure 6.13 Sensitivity and complementary function under *OCSF* conditions for (a) *state* I, (b) *state* II, (c) *state* III, and (d) *state* IV.

6.4 Experimental Validation

The experimental validation demonstrates the dynamic behavior and performance of the proposed TMMFT converter under various operating scenarios. A detailed analysis and discussion of the results are presented. To validate the results, a

prototype of the TMMFT converter has been developed, as shown in the previous chapter, Figure 5.15. The experimental results are illustrated in Figure 6.14, Figure 6.15, Figure 6.16 and Figure 6.17. The nominal design parameters of the circuit components utilized in the prototype are summarized in Table 6.1. The performance evaluation of the proposed converter is carried out under both healthy and OCSF conditions. The corresponding experimental and analytical results are systematically presented and discussed in the following sub-headings:

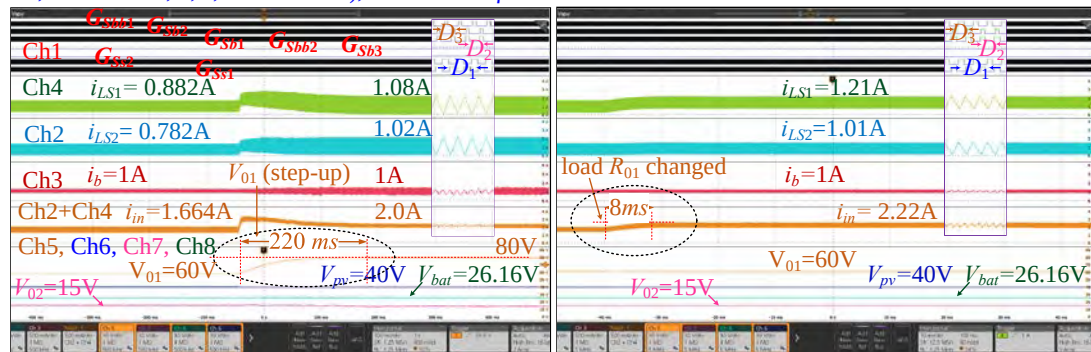
6.4.1 System Controllability Validation

Figures 6.14(a), (c), (d), and (e) illustrate the structural controllability assessment for *state* I, *state* II, *state* III, and *state* IV under healthy conditions, and Figures 6.15(a) and (c) illustrate *state* I and *state* IV under OCSF conditions of the 80W-120W prototype system. *Channel* 1 always represents digital signals. The experimental waveforms were captured using a mixed-signal oscilloscope (MSO) with eight channels. Except for Figure 6.16(a) and Figure 6.17(a), the *channel* assignments in all figures follow the same convention as illustrated in Figure 6.14(a). In Figure 6.15(a) and Figure 6.17(a), the channel numbers are assigned differently and are explicitly labelled in the respective figures for clarity. A step change in V_{01} from 60 V to 80 V results in an adjustment of the corresponding duty ratio from 0.333 to 0.5. The changes in switching logic control directly influence the system state variables, confirming their sensitivity to the control logic. The structural controllability is further validated by interrupting the input power supply, thereby forcing a transition from *state* III to *state* IV under nominal and OCSF in switch S_{bb2} conditions, as presented in Figures 6.16(a) and (b), respectively. This input variation causes noticeable changes in the steady-state values of the corresponding state variables. The designed controller adjusts the system state trajectory, thereby experimentally confirming the structural controllability of the converter.

Further, Figures 6.17(a) and (b) demonstrate state controllability under healthy and multiple OCSF conditions in switches S_{S1} and S_{bb2} . In both cases, the state and output variables are restored to their steady-state values by adjusting the duty ratio after a small transient oscillation. These dynamic responses confirm that the state variables can be driven back to their set values through appropriate control logic. Similarly, Figure 6.17(b) shows the load variation under OCSF condition, the results

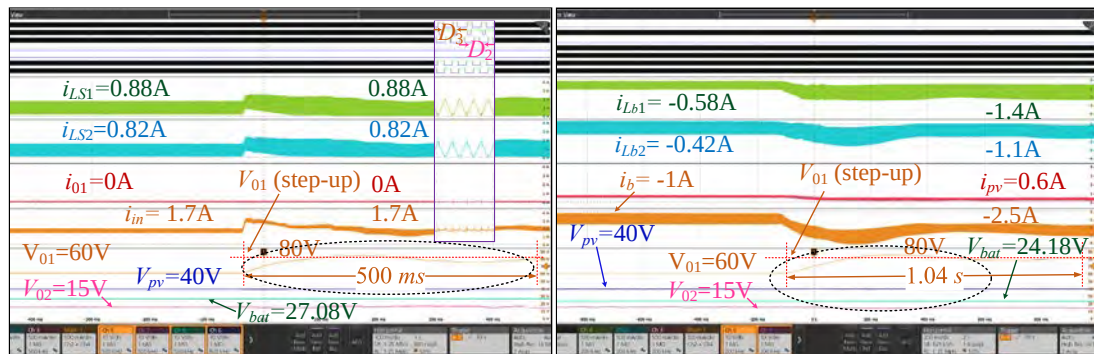
verify the robust dynamic performance of the designed controller. Figures 6.14(b), Figure 6.14(f) show the variation in load R_{01} and Figure 6.17(a) shows the variation in input supply under healthy conditions, whereas Figure 6.15(b), Figure 6.16(b) and Figure 6.17(b) under OCSF condition. In all the cases, the output voltage V_{01} is dipped at the point of change, but restores itself to its set value due to output control, thereby substantiating the *output controllability* of the converter experimentally. Based on the controllability analysis, it is experimentally verified that the system *state I*, *state II*, *state III*, and *state IV* exhibit *structural*, *state*, and *output controllability*. However, in practical power converter applications, the primary control objective is to maintain a regulated output voltage. Therefore, *output controllability* becomes critically important. Given that all four *states* are output controllable, it is feasible to design an appropriate controller tailored to ensure stable and accurate output voltage regulation.

Ch1: Digital out; Ch4,Ch2,Ch3, m1: y-axis: 0.5A/div; Ch5,Ch6,Ch7,Ch8: y-axis: 10V/div, x-axis:(a, c=100ms/div, b=10ms/div, d, e, f=200ms/div), zoomed: 200 μ s/div



(a)

(b)



(c)

(d)

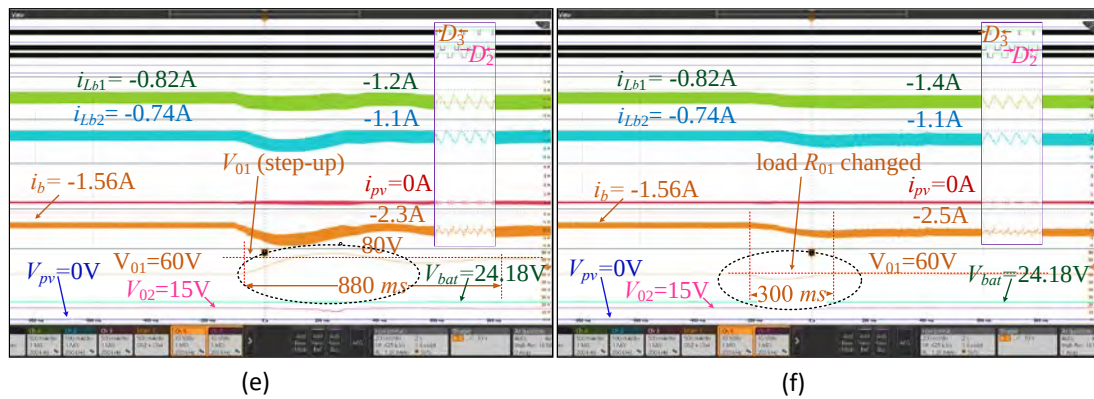


Figure 6.14 Experimental analysis of controllability and system dynamics under healthy conditions for (a) step-up in V_{01} from 60V to 80V (*state I*), (b) load R_{01} halved (*state I*), (c) step-up in V_{01} from 60V to 80V (*state II*), (d) step-up in V_{01} from 60V to 80V (*state III*), (e) step-up in V_{01} from 60V to 80V (*state IV*), and (f) load R_{01} halved (*state IV*).

6.4.2 System Dynamics Validation

6.4.2.1 TMMFT Converter Under Healthy Conditions

In Figure 6.14, the experimental results for the healthy operation of the TMMFT converter are shown. During the *state I* operation, the solar PV source delivers power to all four ports of the converter. Figure 6.14(a) illustrates the corresponding voltage profiles across each port and the associated inductor current waveforms. *Channel 5* in Figure 6.14(a) and *channel m1* in Figure 6.14(b) illustrate a step change in the dc bus voltage V_{01} from 60 V to 80 V and a load change R_{01} for *state I*, with measured settling times (t_s) of approximately 220 ms for V_{01} and 8 ms for the input currents. Similarly, Figures 6.14(c), (d), and (e) depict a step change in V_{01} from 60 V to 80 V for *state II*, *state III*, and *state IV* with a measured t_s of 500ms, 1.04s and 880ms, respectively. Figure 6.14(f) demonstrates a dynamic load change in R_{01} for *state IV*, where a minor disturbance in V_{01} settles within 300 ms.

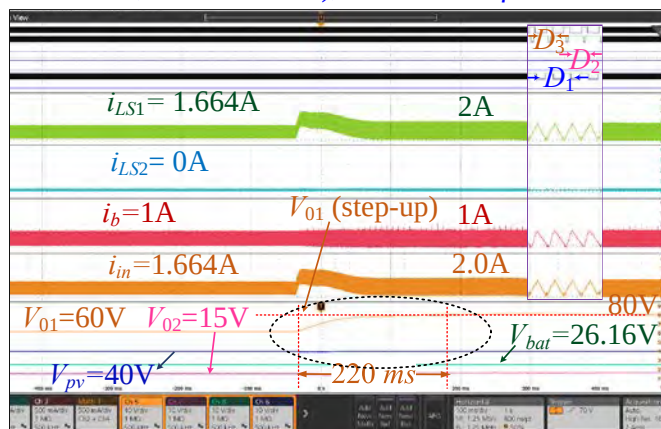
Figure 6.16(a) illustrates the transition from *state III* to *state IV* operation, corresponding to a condition where the load demand exceeds the available power from the solar PV source. Under this scenario, power sharing is established between the solar PV and the battery. During *state III*, the PV contributes 0.5 A, and the battery delivers a discharge current with an average of -1.5A. As the system transitions to *state IV*, the battery discharge current increases to an average of -2.5 A. The negative value of the battery current confirms the discharging operation. The state change for these

conditions has been achieved by switching *off* the PV supply. The settling time (t_s) for battery discharging current and V_{01} is approximately 100ms.

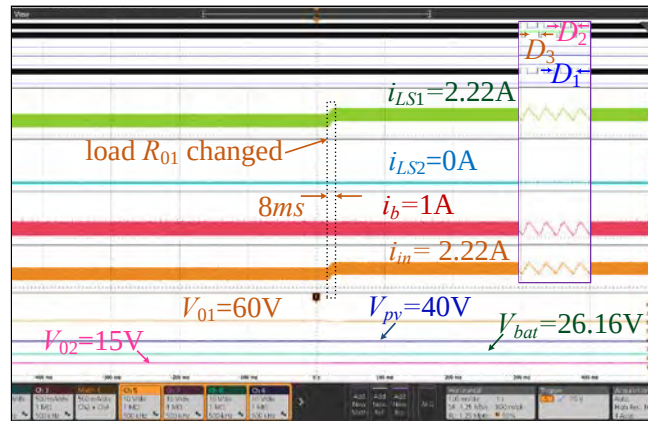
6.4.2.2 TMMFT Converter Under OCSF Conditions

The proposed TMMFT converter exhibits fault-tolerant operation under OCSF conditions. These faults are analyzed considering that all antiparallel diodes remain operational. Single-switch faults, as well as multi-switch faults, are deliberately introduced in switches S_{S1} , S_{b1} , S_{bb1} , and S_{bb2} . The converter's performance is evaluated under identical circuit parameters and consistent testing conditions to validate the controller's robustness and reliability under fault scenarios. Figure 6.15(a) to Figure 6.15(c), Figure 6.16(b), and Figures 6.17(a) and (b) illustrate the system response under a fault in switch S_{S1} - S_{b1} and S_{S1} - S_{bb1} for *state* I and a fault in switch S_{bb2} for *state* IV. The comparative analysis of the system dynamics as shown in Figures 6.14(a), (b), and (e) with Figure 6.15(a) to Figure 6.15(c) without and with fault, respectively, showcases similar dynamics, i.e., the impact of OCSF is negligible on the system dynamics of the TMMFT converter. Figure 6.17(b) illustrates the transition from *state* III to *state* IV operation during a fault in switch S_{bb2} , since the result of this *state* is based on real-time, the PV current and loading conditions of the system are different from a healthy condition to capture the power sharing from PV as well as the battery. The settling time (t_s) for battery discharging current and V_{01} is approximately 500ms.

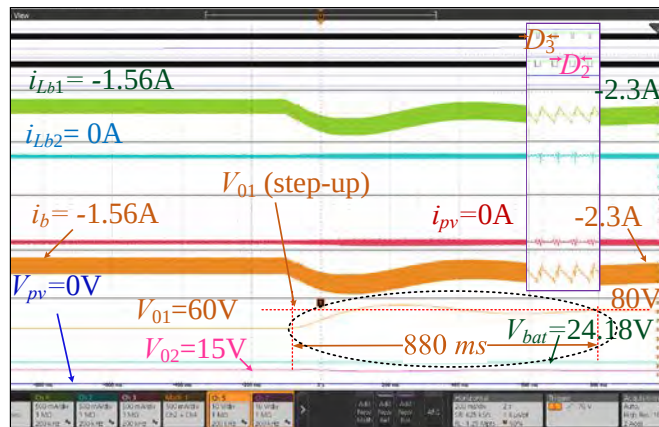
Ch1: Digital out; Ch4,Ch2,Ch3, m1: y-axis: 0.5A/div;
Ch5,Ch6,Ch7,Ch8: y-axis: 10V/div, x-axis:(a, b =
100ms/div, c = 200ms/div), zoomed: 200μs/div



(a)



(b)



(c)

Figure 6.15 Experimental analysis of controllability and system dynamics under OCSF conditions for (a) step-up in V_{01} from 60V to 80V (fault in switch S_{S1} and S_{b1} for *state* I), (b) load R_{01} halved (fault in switch S_{S1} and S_{b1} for *state* I), (c) step-up in V_{01} from 60V to 80V (fault in switch S_{bb2} for *state* IV).

Ch1: Digital out; Ch4, Ch2, Ch3, m1: y-axis: 1A/div & 0.5A/div (without & with fault); Ch5, Ch6, Ch7, Ch8: y-axis: 10V/div, x-axis: 200ms/div & 2s/div (without & with fault); zoomed: 200μs/div

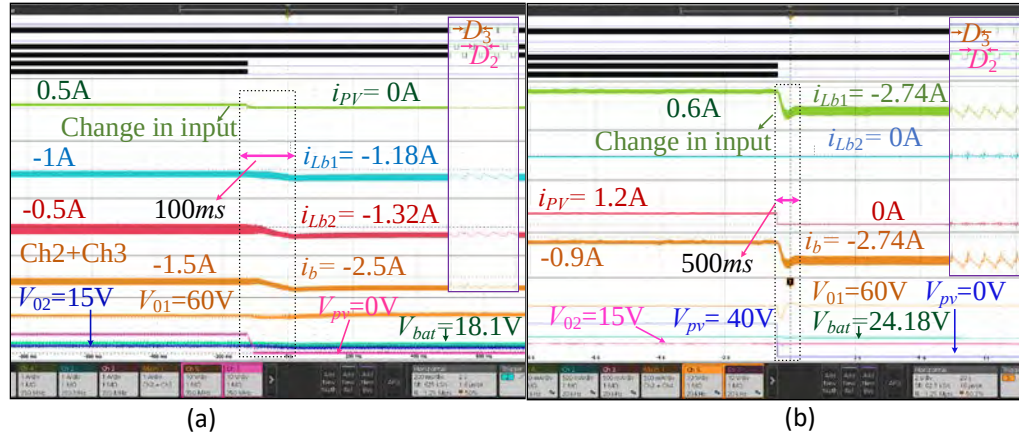


Figure 6.16 Experimental validation for dynamic response to show the state transitions from *state III* to *IV* under (a) nominal operation and (b) OCSF in switch S_{bb2} .

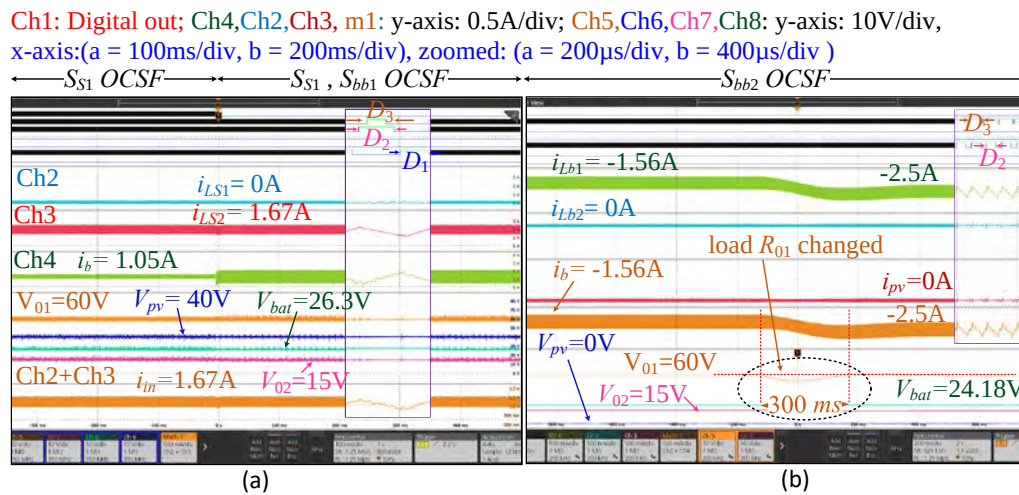


Figure 6.17 Experimental analysis of controllability and system dynamics under OCSF conditions for (a) multi-switch failure (fault in switches S_{s1} and S_{bb1} for *state I*), (b) load R_{01} halved (fault in switch S_{bb2} for *state IV*).

6.4.3 Comparative Analysis of the System

The TMMFT prototype is developed in the laboratory, and a robust PI controller is designed and validated under both healthy and OCSF conditions. Table 6.2 presents a comparative analysis of the proposed control strategy and its effectiveness across key performance categories, including the number of output ports, bidirectional capability, and fault-tolerant operation, in comparison with related works reported in the literature. Compared to existing controller designs, the proposed

approach demonstrates improved performance by providing robust control while accounting for system uncertainties, multiple operating states, load variations, and multiple switch fault tolerance.

Table 6.2
PERFORMANCE COMPARISON OF THE PROPOSED CONTROL STRATEGY FOR TMMFT
WITH STATE-OF-THE-ART METHODS

Ref.	Method	Application	Single / Multiple fault tolerance	Number of operating states	Bi / Uni directional ports	Mitigates uncertainty / Robust
[48]	Hybrid MPC	NR	NR / NR	1	3 / 2	No / No
[49]	SMC	Electronic devices	NR / NR	1	0 / 4	Yes / No
[50]	PI-lead Compensator	EV auxiliary supply	NR / NR	1	0 / 3	No / No
[14]	Robust PI Control	RESs	NR / NR	1	0 / 2	Yes / Yes
[72]	PI Control	DC μ grid, EVs	NR / NR	5	2 / 2	No / No
[31]	Robust PI Control	LEV s	S_1, S_2, S_3, S_4 / Yes	2	1 / 2	Yes / Yes
Proposed	Robust PI Control	LEV s	$S_{S1}, S_{S2}, S_{b3}, S_{b2}, S_{bb1}, S_{bb2}$ / Yes	4	1 / 3	Yes / Yes

RESs-Renewable energy systems, LEV-Light electric vehicles, NR-Not reported

6.4.4 Summary Of Transient Responses

The time-domain performance of the system under the designed robust PI controller, evaluated for both healthy and OCSF conditions, is summarized in Table 6.3 in terms of settling time and percentage undershoot/overshoot for each operating *state*. The consistency in transient behavior across all states, despite variations in operating points and switching configurations, demonstrates that the controller effectively preserves closed-loop damping and stability margins.

Table 6.3
SUMMARY OF TRANSIENT RESPONSES

Step change		Voltage reference			Load change			Input change
Output	Performance parameters	ΔV_{MIDC_ref} (60 to 80) V			ΔR_{01} (100 to 50) Ω			Δi_{pv} (0.5, 1.2 to 0) A
V_{01}	Healthy conditions Figure 6.14 and Figure 6.16(a)	I	II	III	IV	I	IV	III
		<0.1%	$\approx 3-5\%$	$\approx 3-5\%$	$\approx 5-8\%$	<0.1%	$\approx 7-9\%$	$\approx 2-3\%$
		$\approx 0.22s$	$\approx 0.5s$	$\approx 1.04s$	$\approx 0.88s$	$\approx 0.08s$	$\approx 0.30s$	0.1s
	OCSF conditions Figure 6.15, Figure 6.16(b) and Figure 6.17(b)	<0.1%	NR	NR	$\approx 5-8\%$	<0.1%	$\approx 7-9\%$	$\approx 10-15\%$
		$\approx 0.22s$	NR	NR	$\approx 0.88s$	$\approx 0.08s$	$\approx 0.30s$	0.5s

6.5 Conclusions

In this chapter, a comprehensive SLS model of the TMMFT converter was developed by incorporating the effects of parasitic components. The structural controllability of the system was systematically examined using both the SLS formulation and graph theory, and it was analytically verified that the TMMFT converter satisfies the conditions of output controllability under the defined operating conditions. The SSM corresponding to operating states I-IV were derived, and the dynamic behaviour of the associated transfer functions was validated through experimental results. Furthermore, the sensitivity and complementary sensitivity characteristics were analysed under both healthy and OCSF conditions, confirming robust stability and effective disturbance attenuation. In addition, the dynamic performance of the converter under OCSF conditions was investigated to assess its fault-tolerant capability. Moreover, a robust controller design approach based on the stability boundary locus method in combination with Kharitonov's theorem was presented to address system parameter uncertainties. The PI controller gains derived using this method were experimentally validated and shown to ensure stable and robust closed-loop performance.

Chapter 7

MAIN CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The introduction of time-multiplexing control significantly reduces the number of active switches while maintaining high modularity, scalability, and improved system redundancy, leading to enhanced reliability. The proposed converter topologies achieve reduced current ripple, improved power density, and optimized passive component utilization, thereby enhancing overall system efficiency. Furthermore, the converters exhibit inherent fault-tolerant capability, particularly under open-circuit switch faults (OCSF), with validated stable operation and controlled power redistribution during faults. A detailed characterization of current ripple has been analytically investigated for each operating state by considering duty cycle variation, voltage gain, and operating modes, thereby enabling improved passive component design and enhanced current quality.

In addition, the incorporation of soft-switching operation, including ZVS and ZCS, over a wide operating range minimizes switching losses and improves converter efficiency, making the proposed system suitable for high-frequency applications. Robust controller design methodologies based on the stability boundary locus technique combined with Kharitonov's theorem have also been systematically developed to guarantee closed-loop stability and disturbance rejection under parametric uncertainties. The proposed control strategy effectively integrates CCCV battery charging, DC bus voltage regulation, and coordinated multiport power-flow management, thereby ensuring seamless operation across different operating modes and loading conditions.

Moreover, a unified modeling and control framework for time-multiplexed multiport DC-DC converters has been successfully developed by incorporating parasitic effects and structured uncertainties to accurately represent practical converter dynamics. The proposed converter architectures demonstrate complete structural controllability, which has been verified through graph-theoretic analysis and SLS modeling, thereby ensuring reliable regulation of both state and output variables under all operating conditions. Comprehensive SSM together with experimental validation

further confirms the dynamic performance, robustness, and reliability of the proposed system under both healthy and fault conditions. Consequently, the developed converter architectures ensure robust DC power availability and are highly suitable for renewable energy integration, electric vehicle charging, and DC microgrid applications.

7.2 Future Scope of the Work

The future scope of the proposed research includes integrating AI/ML-based fault diagnosis and predictive maintenance techniques for real-time health monitoring and intelligent fault management. Further enhancement of converter performance can be achieved by exploring wide-bandgap semiconductor devices such as SiC and GaN, which can significantly improve switching frequency, conversion efficiency, and thermal performance. In addition, the implementation of distributed and decentralized control architectures for large-scale multiport systems and DC microgrids represents an important direction for achieving scalable and flexible energy management. The optimization of magnetic component design and thermal management techniques can further improve converter power density and overall system compactness.

Moreover, future investigations may focus on cyber-physical security aspects of digitally controlled multiport converters to ensure resilient, secure operation in smart grid environments. The proposed architectures can also be extended toward hybrid energy system integration involving photovoltaic (PV) sources, fuel cells, batteries, and supercapacitors combined with intelligent energy management strategies for enhanced reliability and sustainable operation.

7.3 Sustainable Development Goals

The proposed research significantly contributes to several Sustainable Development Goals (SDGs) by developing advanced, reliable, and energy-efficient multiport power conversion systems. In alignment with *SDG 3 - Health & Well-being*, the developed converter architectures provide uninterrupted power supply for critical applications such as healthcare systems, thereby enhancing the reliability of life-saving infrastructure. In the context of *SDG 7 - Affordable & Clean Energy*, the proposed systems enable efficient integration of renewable energy sources, improve energy efficiency, and reduce power losses in modern power systems.

Furthermore, the proposed research supports *SDG 8 - Decent Work & Economic Growth* by reducing operational costs and improving system efficiency, thereby supporting industrial productivity and economic development. With respect to *SDG 9 - Industry, Innovation & Infrastructure*, the developed fault-resilient power conversion systems contribute to robust, innovative infrastructure by reducing system complexity while enhancing reliability and operational flexibility. In addition, the proposed architectures align with *SDG 10 - Reduced Inequalities* by enhancing rural electrification through resilient DC microgrids, thereby improving energy accessibility in underserved and remote communities.

The research also contributes to *SDG 11 - Sustainable Cities & Communities* by developing reliable electric vehicle charging infrastructure and smart energy systems that support sustainable urban mobility and smart city development. Moreover, the proposed converter systems support *SDG 13 - Climate Action* by facilitating low-carbon energy systems through renewable energy integration, improved conversion efficiency, and reduced emissions from energy and transportation sectors. Collectively, the proposed work promotes sustainable energy utilization, resilient power infrastructure, and environmentally responsible technological advancement for future smart grid and DC microgrid applications.

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Appendix-A

THEORETICAL RESULTS

This appendix presents the essential theoretical derivations utilized throughout the main chapters of the thesis.

A.1 State-space Modeling and Small-signal Analysis Under Different Operating Modes for TMDCM converter

The proposed converter operates under two distinct switching intervals, namely *mode A* and *mode B*, corresponding to different switching states within one switching cycle. These operating *modes* serve as the basis for deriving the converter state equations and dynamic mathematical models. For each mode, the equivalent circuit configuration is analyzed considering the conduction states of the semiconductor devices and the associated energy transfer paths. Based on the converter operation in *mode A* and *mode B*, as given in Figures 3.6 and 3.8, respectively, the large-signal state equations are formulated using Kirchhoff's voltage and current laws. Subsequently, the averaged state-space model is derived over one complete switching period to represent the converter dynamics under CCM operation. Furthermore, small-signal perturbation and linearization techniques are employed around the steady-state operating point to obtain the small-signal model, which is utilized for controllability analysis, transfer function derivation, and robust controller design.

For *Mode A* operation, the state equations are given below:

$$\left. \begin{aligned} V_{L1} &= L_1 \frac{di_{L1}}{dt} = V_{in} - r_{L1}i_{L1} - V_{SS1} - V_{SS2} \\ V_{L2} &= L_2 \frac{di_{L2}}{dt} = -v_{cp02} - r_{L2}i_{L2} - V_{DS1} \\ i_{c01} &= -i_{01}, \forall D_1T \end{aligned} \right\}, \text{ interval } 1 \quad (\text{A.1a})$$

$$\left. \begin{aligned} V_{L1} &= L_1 \frac{di_{L1}}{dt} = V_{in} - r_{L1}i_{L1} - V_D - v_{cp01} \\ V_{L2} &= L_2 \frac{di_{L2}}{dt} = v_{cp01} - r_{L2}i_{L2} - V_{SS1} - v_{cp02} \\ i_{c01} &= i_{L1} - i_{L2} - i_{01}, \forall D_2T \end{aligned} \right\}, \text{ interval } 2 \quad (\text{A.1b})$$

$$\left. \begin{aligned} V_{L1} &= L_1 \frac{di_{L1}}{dt} = V_{in} - r_{L1}i_{L1} - V_D - v_{cp01} \\ V_{L2} &= L_2 \frac{di_{L2}}{dt} = -v_{cp02} - r_{L2}i_{L2} - V_{DS1} \\ i_{c01} &= i_{L1} - i_{01}, \quad \forall (1 - D_1 - D_2) \times T \end{aligned} \right\}, \text{ interval } 3 \quad (\text{A.1c})$$

$$i_{c02} = i_{L2} - i_{02} \quad (\text{A.2})$$

$$v_{cp01} = r_{c1}C_1 \frac{dv_{c1}}{dt} + v_{c1} \quad (\text{A.3})$$

$$v_{cp02} = r_{c2}C_2 \frac{dv_{c2}}{dt} + v_{c2} \quad (\text{A.4})$$

For *Mode B* operation, the state equations are given below:

$$\left. \begin{aligned} V_{L1} &= L_1 \frac{di_{L1}}{dt} = v_{cin} - r_{L1}i_{L1} - V_D - v_{cp01} \\ V_{L2} &= L_2 \frac{di_{L2}}{dt} = -v_{cbat} - r_{L2}i_{L2} + V_{SS2} \\ i_{cin} &= -i_{L1}, \quad i_{c01} = i_{L1} - i_{01}, \quad \forall D_{1b}T \end{aligned} \right\}, \text{ interval } 1 \quad (\text{A.5a})$$

$$\left. \begin{aligned} V_{L1} &= L_1 \frac{di_{L1}}{dt} = v_{cin} - r_{L1}i_{L1} - V_D - v_{cp01} \\ V_{L2} &= L_2 \frac{di_{L2}}{dt} = -v_{cbat} - r_{L2}i_{L2} - V_{DS1} - V_D \\ i_{cin} &= -i_{L1}, \quad i_{c01} = i_{L1} - i_{L2} - i_{01}, \quad \forall (1 - D_{1b}) \times T \end{aligned} \right\}, \text{ interval } 2 \quad (\text{A.5b})$$

$$\text{where, } i_{01} = \frac{v_{cp01}}{R_{01}}, \quad i_{02} = \frac{v_{cp02}}{R_{02}} \quad (\text{A.6})$$

$$i_{cin} = C_{in} \frac{dv_{cin}}{dt} \quad (\text{A.7})$$

$$i_{c01} = C_1 \frac{dv_{c1}}{dt} \quad (\text{A.8})$$

$$i_{c02} = C_2 \frac{dv_{c2}}{dt} \quad (\text{A.9})$$

The system matrix orders are as follows:

- (i). *Mode A*: Four state variables.
- (ii). *Mode B*: Four state variables.

The state-space representation for *Mode A* operation is as follows:

(i). State equation: $\hat{\dot{x}} = \mathbf{A}\hat{x} + \mathbf{B}\hat{u} + \mathbf{E}\hat{d}_1 + \mathbf{F}\hat{d}_2$

(ii). Output equation: $y(t) = \mathbf{C}\hat{x}(t) + \mathbf{D}\hat{u}(t) + \mathbf{G}_1\hat{d}_1 + \mathbf{G}_2\hat{d}_2$

Where the matrices A, B, C and D represent the system, input, output, and direct transmission matrices, and E, G are the state variables at steady-state for the input and output equations.

State Variables and Input Vectors for Mode A:

(i). State vector: $x(t)|_A = [i_{L1}, i_{L2}, v_{C1}, v_{C2}]^T$

(ii). Input vector: $u(t)|_A = [v_{in}, v_{Ss1}, v_{Ss2}, v_{Ds2}, v_D]^T$

The small-signal model for this mode is given below:

$\hat{\dot{x}} = \mathbf{A}\hat{x} + \mathbf{B}\hat{u} + \mathbf{E}\hat{d}_1 + \mathbf{F}\hat{d}_2;$

$$\begin{bmatrix} \hat{\dot{i}}_{L1} \\ \hat{\dot{i}}_{L2} \\ \hat{\dot{v}}_{C1} \\ \hat{\dot{v}}_{C2} \end{bmatrix} = \begin{bmatrix} N_1 & \frac{r_{e1}d_2}{L_1} & -\frac{r_{e1}(1-d_1)}{L_1 r_{C1}} & 0 \\ \frac{r_{e1}d_2}{L_2} & -N_2 & \frac{r_{e1}d_2}{L_2 r_{C1}} & -\frac{r_{e2}}{L_2 r_{C2}} \\ \frac{r_{e1}(1-d_1)}{r_{C1}C_1} & -\frac{r_{e1}d_2}{r_{C1}C_1} & -\frac{r_{e1}}{r_{C1}R_{01}C_1} & 0 \\ 0 & \frac{r_{e2}}{r_{C2}C_2} & 0 & -\frac{r_{e2}}{r_{C2}R_{02}C_2} \end{bmatrix} \hat{x}(t) + \begin{bmatrix} \frac{1}{L_1} & -\frac{1}{L_1}d_1 & -\frac{1}{L_1}d_1 & 0 & -\frac{1}{L_1}(1-d_1) \\ 0 & -\frac{1}{L_2}d_2 & 0 & -\frac{1}{L_2}(1-d_2) & \frac{1}{L_2}d_2 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_{Ss1} \\ \hat{v}_{Ss2} \\ \hat{v}_{Ds2} \\ \hat{v}_D \end{bmatrix}$$

$$\begin{aligned}
 & + \begin{bmatrix} \frac{v_D}{L_1} - \frac{v_{Ss1}}{L_1} - \frac{v_{Ss2}}{L_1} + \frac{r_{e1}I_{L1}}{L_1} + \frac{r_{e1}V_{01}}{r_{C1}L_1} \\ 0 \\ -\frac{r_{e1}I_{L1}}{r_{C1}C_1} \\ 0 \end{bmatrix} \begin{bmatrix} \hat{d}_1 \end{bmatrix} \\
 & + \begin{bmatrix} \frac{r_{e1}I_{L2}}{L_1} \\ \frac{v_D}{L_2} - \frac{v_{Ss1}}{L_2} + \frac{v_{Ds2}}{L_2} + \frac{r_{e1}I_{L1}}{L_2} - \frac{r_{e1}I_{L2}}{L_2} + \frac{r_{e1}V_{01}}{r_{C1}L_2} \\ -\frac{r_{e1}I_{L2}}{r_{C1}C_1} \\ 0 \end{bmatrix} \begin{bmatrix} \hat{d}_2 \end{bmatrix}
 \end{aligned}
 \tag{A.10}$$

and $y(t) = \mathbf{C}\hat{x}(t) + \mathbf{D}\hat{u}(t) + \mathbf{G}_1\hat{d}_1 + \mathbf{G}_2\hat{d}_2$

$$\begin{bmatrix} \hat{v}_{C1} \\ \hat{v}_{C2} \end{bmatrix} = \begin{bmatrix} r_{e1}(1-d_1) & -r_{e1}d_2 & \frac{r_{e1}}{r_{C1}} & 0 \\ 0 & r_{e2} & 0 & \frac{r_{e2}}{r_{C2}} \end{bmatrix} \hat{x}(t) + (-I_{L1}r_{e1}) \begin{bmatrix} \hat{d}_1 \end{bmatrix} + (-I_{L2}r_{e1}) \begin{bmatrix} \hat{d}_2 \end{bmatrix}
 \tag{A.11}$$

$$\begin{aligned}
 \text{where, } r_{e1} &= \frac{R_{01}r_{C1}}{R_{01} + r_{C1}}, \quad r_{e2} = \frac{R_{02}r_{C2}}{R_{02} + r_{C2}}, \quad N_1 = \frac{-(r_{L1} + r_{e1}(1-d_1))}{L_1}, \\
 N_2 &= \frac{(r_{L2} + r_{e2} + r_{e1}d_2)}{L_2}
 \end{aligned}
 \tag{A.12}$$

State Variables and Input Vectors for Mode B:

(i). State vector: $x(t)|_B = [i_{L1}, i_{L2}, v_{c1}, v_{cin}]^T$

(ii). Input vector: $u(t)|_B = [v_{bat}, v_D, v_{Sb2}, v_{Ds1}]^T$

The small-signal model for this mode is given below.

$$\hat{\dot{x}} = \mathbf{A}\hat{x} + \mathbf{B}\hat{u} + \mathbf{E}\hat{d}_b;$$

$$\begin{bmatrix} \hat{\dot{i}}_{L1} \\ \hat{\dot{i}}_{L2} \\ \hat{\dot{v}}_{C1} \\ \hat{\dot{v}}_{Cin} \end{bmatrix} = \begin{bmatrix} N_1 & \frac{-r_{e1}(1-d_b)}{L_1} & -\frac{r_{e1}}{L_1 r_{C1}} & \frac{1}{L_1} \\ \frac{r_{e1}(1-d_b)}{L_2} & -N_2 & \frac{r_{e1}(1-d_b)}{L_2 r_{C1}} & 0 \\ \frac{r_{e1}}{r_{C1} C_1} & -\frac{r_{e1}(1-d_b)}{r_{C1} C_1} & -\frac{r_{e1}}{r_{C1} R_{01} C_1} & 0 \\ \frac{-1}{C_{in}} & 0 & 0 & 0 \end{bmatrix} \hat{x}(t) + \begin{bmatrix} 0 & -\frac{1}{L_1} & 0 & 0 \\ -\frac{1}{L_2} & -\frac{1}{L_2}(1-d_b) & \frac{1}{L_2}d_b & -\frac{1}{L_2}(1-d_b) \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{bat} \\ \hat{v}_D \\ \hat{v}_{Sb2} \\ \hat{v}_{Ds1} \end{bmatrix} + \begin{bmatrix} \frac{r_{e1} I_{L2}}{L_1} \\ \frac{r_{e1} I_{L2}}{L_2} - \frac{r_{e1} I_{L1}}{L_2} + \frac{r_{e1} V_{01}}{r_{C1} L_2} + \left(-\frac{v_{Ds1}}{L_2} - \frac{v_D}{L_2} + \frac{v_{Sb2}}{L_2} \right) \\ \frac{r_{e1} I_{L2}}{r_{C1} C_1} \\ 0 \end{bmatrix} \hat{d}_b \quad (\text{A.13})$$

$$\text{and } y(t) = \mathbf{C}\hat{x}(t) + \mathbf{D}\hat{u}(t) + \mathbf{G}_1 \hat{d}_b$$

$$\begin{bmatrix} \hat{v}_{C1} \end{bmatrix} = \begin{bmatrix} r_{e1} & -r_{e1}(1-d_b) & \frac{r_{e1}}{r_{C1}} & 0 \end{bmatrix} \hat{x}(t) + (I_{L2} r_{e1}) \hat{d}_b \quad (\text{A.14})$$

$$\text{where, } r_{e1} = \frac{R_{01} r_{C1}}{R_{01} + r_{C1}}, r_{e2} = \frac{R_{02} r_{C2}}{R_{02} + r_{C2}}, N_1 = \frac{-(r_{L1} + r_{e1} + r_{Cin})}{L_1},$$

$$N_2 = \frac{(r_{L2} + r_{e1}(1-d_b))}{L_2} \quad (\text{A.15})$$

A.2 Time-domain Analysis of the TPFTMDC Converter

A.2.1 Mode-wise Analysis for State I Operation

The switching characteristics and operating modes in this state are shown in Figure 4.2 and Figure 4.3, respectively. Based on the operating modes, the time-domain analysis has been performed.

1) For mode 1

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (A2.1a)$$

Now, taking the Laplace transform and considering the initial conditions.

$$\begin{aligned} \Rightarrow L_1 \left[sI_{L1}^{S-I}(s) - I_{L1}^{S-I}(0^+) \right] &= \frac{V_{in}}{s} - \frac{V_{01}}{s} \\ \Rightarrow sL_1 I_{L1}^{S-I}(s) - L_1 I_{L1}^{S-I}(0^+) &= \frac{V_{in}}{s} - \frac{V_{01}}{s} \\ \Rightarrow I_{L1}^{S-I}(s) &= \frac{V_{in}}{s^2 L_1} - \frac{V_{01}}{s^2 L_1} + \frac{I_{L1}^{S-I}(0^+)}{s} \end{aligned} \quad (A2.1b)$$

Now, after performing the inverse Laplace transform.

$$\begin{aligned} \Rightarrow i_{L1}^{S-I}(t) &= \left(\frac{V_{in}}{L_1} - \frac{V_{01}}{L_1} \right) \times t + i_{L1}^{S-I}(t_0) \\ \Rightarrow i_{L1}^{S-I}(t) &= i_{L1}^{S-I}(t_0) - \left(\frac{V_{01} - V_{in}}{L_1} \right) t \\ i_{L1}^{S-I}(t) &= i_{L1}^{S-I}(t_0) - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_1) = I_1^{S-I} \end{aligned} \quad (A2.1c)$$

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \quad (A2.2a)$$

Now, taking the Laplace transform of (A2.2a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow L_{b1} \left[sI_{Lb1}^{S-I}(s) - I_{Lb1}^{S-I}(0^+) \right] &= -\frac{V_{bat}}{s} \\ \Rightarrow sL_{b1} I_{Lb1}^{S-I}(s) - L_{b1} I_{Lb1}^{S-I}(0^+) &= -\frac{V_{bat}}{s} \\ \Rightarrow I_{Lb1}^{S-I}(s) &= -\frac{V_{bat}}{s^2 L_{b1}} + \frac{I_{Lb1}^{S-I}(0^+)}{s} \end{aligned} \quad (A2.2b)$$

Now, after performing the inverse Laplace transform.

$$\begin{aligned} \Rightarrow i_{Lb1}^{S-I}(t) &= -\frac{V_{bat} \times t}{L_{b1}} + i_{Lb1}^{S-I}(t_0) \\ \Rightarrow i_{Lb1}^{S-I}(t) &= i_{Lb1}^{S-I}(t_0) - \frac{V_{bat} \times t}{L_{b1}} \end{aligned}$$

$$i_{Lb1}^{S-I}(t) = i_{Lb1}^{S-I}(t_0) - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_1) = I_{b1}^{S-I}, \quad (A2.2c)$$

2) For mode 2

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (A2.3a)$$

In (A2.3a) and (A2.4a), only the initial condition changes remaining are analogous to (A2.1c) and (A2.2c).

$$i_{L1}^{S-I}(t) = i_{L1}^{S-I}(t_0) - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_1) = I_1^{S-I}, \quad (A2.3b)$$

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \quad (A2.4a)$$

$$i_{Lb1}^{S-I}(t) = I_{b1}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_2) = I_{b2}^{S-I}, \quad (A2.4b)$$

$$L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} = V_{01} \quad (A2.5a)$$

Now, taking the Laplace transform of (A2.5a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow L_{r1} \left[s I_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] &= \frac{V_{01}}{s} \\ \Rightarrow s L_{r1} I_{Lr1}^{S-I}(s) - L_{r1} I_{Lr1}^{S-I}(0^+) &= \frac{V_{01}}{s} \\ \Rightarrow I_{Lr1}^{S-I}(s) &= \frac{V_{01}}{s^2 L_{r1}} + \frac{I_{Lr1}^{S-I}(0^+)}{s}, \quad I_{Lr1}^{S-I}(0^+) = 0, \\ \Rightarrow I_{Lr1}^{S-I}(s) &= \frac{V_{01}}{s^2 L_{r1}} \end{aligned} \quad (A2.5b)$$

Now, after performing the inverse Laplace transform.

$$i_{Lr1}^{S-I}(t) = \frac{V_{01}}{L_{r1}} \times t \quad (A2.5c)$$

3) For mode 3

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (A2.6a)$$

In (A2.6a), only the initial condition changes remaining are analogous to (A2.1c).

$$i_{L1}^{S-I}(t) = I_2^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_3) = I_3^{S-I}, \quad (\text{A2.6b})$$

$$i_{Lr1}^{S-I}(t) = i_{Lb1}^{S-I}(t), \quad (\text{A2.7a})$$

$$\begin{aligned} \Rightarrow (V_{01} - v_{Lr1}^{S-I}(t)) - V_{bat} &= L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} \\ \Rightarrow \frac{di_{Lb1}^{S-I}(t)}{dt} &= \left(\frac{V_{01} - V_{bat}}{L_{b1}} \right) - \frac{L_{r1}}{L_{b1}} \frac{di_{Lr1}^{S-I}(t)}{dt} \\ \Rightarrow \frac{di_{Lr1}^{S-I}(t)}{dt} &= \left(\frac{V_{01} - V_{bat}}{L_{b1}} \right) - \frac{L_{r1}}{L_{b1}} \frac{di_{Lr1}^{S-I}(t)}{dt}, \text{ by (A2.7a)} \\ \Rightarrow (L_{b1} + L_{r1}) \frac{di_{Lr1}^{S-I}(t)}{dt} &= (V_{01} - V_{bat}) \end{aligned} \quad (\text{A2.7b})$$

Now, taking the Laplace transform and considering the initial conditions.

$$\begin{aligned} \Rightarrow (L_{b1} + L_{r1}) \left[s I_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] &= \frac{(V_{01} - V_{bat})}{s} \\ \Rightarrow I_{Lr1}^{S-I}(s) &= \frac{I_{Lr1}^{S-I}(0^+)}{s} + \left(\frac{V_{01} - V_{bat}}{L_{b1} + L_{r1}} \right) \times \frac{1}{s^2} \end{aligned} \quad (\text{A2.7c})$$

Now, after performing the inverse Laplace transform.

$$i_{Lr1}^{S-I}(t) = i_{Lb1}^{S-I}(t) = I_{b2}^{S-I} + \left(\frac{V_{01} - V_{bat}}{L_{r1} + L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_3) = I_{Lb1\max}^{S-I}, \quad (\text{A2.7d})$$

4) For mode 4

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (\text{A2.8a})$$

In (A2.8a), only the initial condition changes remaining are analogous to (A2.1c).

$$i_{L1}^{S-I}(t) = I_3^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_4) = I_{L1\min}^{S-I}, \quad (\text{A2.8b})$$

$$L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} = V_{01} \quad (\text{A2.9a})$$

Now, taking the Laplace transform of (A2.9a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow L_{r1} \left[sI_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] &= \frac{V_{01}}{s} \\ \Rightarrow sL_{r1}I_{Lr1}^{S-I}(s) - L_{r1}I_{Lr1}^{S-I}(0^+) &= \frac{V_{01}}{s} \\ \Rightarrow I_{Lr1}^{S-I}(s) &= \frac{V_{01}}{s^2 L_{r1}} + \frac{I_{Lr1}^{S-I}(0^+)}{s}, \\ \Rightarrow I_{Lr1}^{S-I}(0^+) &= I_{Lr1}^{S-I}(t_3) = I_{Lb1\max}^{S-I}, \\ \Rightarrow I_{Lr1}^{S-I}(s) &= \frac{I_{Lb1\max}^{S-I}}{s} + \frac{V_{01}}{s^2 L_{r1}} \end{aligned} \quad (\text{A2.9b})$$

Now, after performing the inverse Laplace transform.

$$i_{Lr1}^{S-I}(t) = I_{Lb1\max}^{S-I} + \frac{V_{01}}{L_{r1}} \times t, \quad i_{Lr1}^{S-I}(t_4) \approx I_{L1\min}^{S-I} + I_{Lb1\max}^{S-I} = I_{Lr}^{S-I}. \quad (\text{A2.9c})$$

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \quad (\text{A2.10a})$$

Now, taking the Laplace transform of (A2.10a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow L_{b1} \left[sI_{Lb1}^{S-I}(s) - I_{Lb1}^{S-I}(0^+) \right] &= -\frac{V_{bat}}{s} \\ \Rightarrow sL_{b1}I_{Lb1}^{S-I}(s) - L_{b1}I_{Lb1}^{S-I}(0^+) &= -\frac{V_{bat}}{s} \\ \Rightarrow I_{Lb1}^{S-I}(s) &= -\frac{V_{bat}}{s^2 L_{b1}} + \frac{I_{Lb1}^{S-I}(0^+)}{s}, \\ \Rightarrow I_{Lb1}^{S-I}(0^+) &= I_{Lb1}^{S-I}(t_3) = I_{Lb1\max}^{S-I}, \\ \Rightarrow I_{Lb1}^{S-I}(s) &= \frac{I_{Lb1\max}^{S-I}}{s} - \frac{V_{bat}}{s^2 L_{b1}} \end{aligned} \quad (\text{A2.10b})$$

Now, after performing the inverse Laplace transform.

$$i_{Lb1}^{S-I}(t) = I_{Lb1\max}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_4) = I_{b3}^{S-I}, \quad (\text{A2.10c})$$

5) For mode 5

$$i_{L1}^{S-I}(t) \approx I_{L1}^{S-I}(t_4) \approx I_{L1}^{S-I}(t_5) \approx I_{L1\min}^{S-I} \quad (\text{A2.11})$$

$$\Rightarrow i_{Lr1}^{S-I}(t) = -i_{Cr1}^{S-I}(t) + i_{L1}^{S-I}(t)$$

$$\Rightarrow i_{Lr1}^{S-I}(t) = -C_{r1} \frac{dv_{Cr1}^{S-I}(t)}{dt} + I_{L1\min}^{S-I}, \quad \text{by (A2.11)}$$

$$\because v_{Lr1}^{S-I}(t) = v_{Cr1}^{S-I}(t),$$

differentiating above

$$\Rightarrow \dot{v}_{Lr1}^{S-I}(t) = \dot{v}_{Cr1}^{S-I}(t),$$

$$\Rightarrow i_{Lr1}^{S-I}(t) = -C_{r1} \frac{dv_{Lr1}^{S-I}(t)}{dt} + I_{L1\min}^{S-I}, \quad (\text{A2.12a})$$

$$\Rightarrow i_{Lr1}^{S-I}(t) = -C_{r1} L_{r1} \frac{d^2 i_{Lr1}^{S-I}(t)}{dt^2} + I_{L1\min}^{S-I},$$

$$\because \omega_{r1} = \frac{1}{\sqrt{L_{r1} C_{r1}}},$$

$$\Rightarrow \frac{d^2 i_{Lr1}^{S-I}(t)}{dt^2} + \omega_{r1}^2 i_{Lr1}^{S-I}(t) = \omega_{r1}^2 I_{L1\min}^{S-I}$$

Now, taking the Laplace transform of (A2.12a) and considering the initial conditions.

$$\Rightarrow \left[s^2 I_{Lr1}^{S-I}(s) - s I_{Lr1}^{S-I}(0^+) - i_{Lr1}^{S-I}(0^+) \right] + \omega_{r1}^2 I_{Lr1}^{S-I}(s) = \frac{\omega_{r1}^2 I_{L1\min}^{S-I}}{s}$$

$$\Rightarrow (s^2 + \omega_{r1}^2) I_{Lr1}^{S-I}(s) = s I_{Lr1}^{S-I}(0^+) + i_{Lr1}^{S-I}(0^+) + \frac{\omega_{r1}^2 I_{L1\min}^{S-I}}{s}$$

$$\Rightarrow I_{Lr1}^{S-I}(s) = \frac{s I_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{r1}^2} + \frac{i_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{r1}^2} + \frac{\omega_{r1}^2 I_{L1\min}^{S-I}}{s(s^2 + \omega_{r1}^2)}$$

$$\because I_{Lr1}^{S-I}(0^+) = I_{Lr1}^{S-I}(t_4), \quad \text{by (A2.9c)}$$

and $i_{Lr1}^{S-I}(0^+) = \frac{V_{01}}{L_{r1}}$, initial capacitor voltage ($v_{Cr1}^{S-I}(t)$) drives the current slope

$$\Rightarrow I_{Lr1}^{S-I}(s) = \frac{s I_{Lr1}^{S-I}(s)}{s^2 + \omega_{r1}^2} + \frac{V_{01}}{L_{r1} \omega_{r1}} \left(\frac{\omega_{r1}}{s^2 + \omega_{r1}^2} \right) + \left(\frac{1}{s} - \frac{s}{s^2 + \omega_{r1}^2} \right) I_{L1\min}^{S-I}$$

$$\because \omega_{r1} = \frac{1}{\sqrt{L_{r1} C_{r1}}}, Z_{r1} = \sqrt{\frac{L_{r1}}{C_{r1}}}, \quad \text{and putting (A2.9c) below}$$

$$\therefore I_{Lr1}^{S-I}(s) = \frac{s I_{L1\min}^{S-I}}{s^2 + \omega_{r1}^2} + \frac{s I_{Lb1\max}^{S-I}}{s^2 + \omega_{r1}^2} + \frac{V_{01}}{Z_{r1}} \left(\frac{\omega_{r1}}{s^2 + \omega_{r1}^2} \right) + \left(\frac{1}{s} I_{L1\min}^{S-I} - \frac{s}{s^2 + \omega_{r1}^2} I_{L1\min}^{S-I} \right)$$

$$\Rightarrow I_{Lr1}^{S-I}(s) = \frac{sI_{Lb1\max}^{S-I}}{s^2 + \omega_{r1}^2} + \frac{V_{01}}{Z_{r1}} \left(\frac{\omega_{r1}}{s^2 + \omega_{r1}^2} \right) + \frac{1}{s} I_{L1\min}^{S-I} \quad (\text{A2.12b})$$

Now, after performing the inverse Laplace transform.

$$\begin{aligned} i_{Lr1}^{S-I}(t) &= I_{L1\min}^{S-I} + I_{Lb1\max}^{S-I} \cos(\omega_{r1}t) + \frac{V_{01}}{Z_{r1}} \sin(\omega_{r1}t) \\ \because \cos(\omega_{r1}t) &\ll 1 \\ \Rightarrow i_{Lr1}^{S-I}(t) &= I_{L1\min}^{S-I} + I_{Lb1\max}^{S-I} + \frac{V_{01}}{Z_{r1}} \sin(\omega_{r1}t) \end{aligned} \quad (\text{A2.12c})$$

$$\begin{aligned} i_{Lr1}^{S-I}(t) &= I_{Lr}^{S-I} + \frac{V_{01}}{Z_{r1}} \sin(\omega_{r1}t) \\ \because v_{Lr1}^{S-I}(t) &= v_{Cr1}^{S-I}(t) = L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} \\ \Rightarrow v_{Cr1}^{S-I}(t) &= \frac{d \left(I_{Lr}^{S-I} + \frac{V_{01}}{Z_{r1}} \sin(\omega_{r1}t) \right)}{dt} \end{aligned} \quad (\text{A2.13})$$

$$v_{Cr1}^{S-I}(t) = V_{01} \cos(\omega_{r1}t)$$

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \quad (\text{A2.14a})$$

In (A2.14a), only the initial condition changes remaining are analogous to (A2.10b).

$$i_{Lb1}^{S-I}(t) = I_{b3}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_5) = I_{b4}^{S-I}, \quad (\text{A2.14b})$$

6) For mode 6

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} \quad (\text{A2.15a})$$

$$\begin{aligned} \Rightarrow L_1 \left[sI_{L1}^{S-I}(s) - I_{L1}^{S-I}(0^+) \right] &= \frac{V_{in}}{s} \\ \Rightarrow sL_1 I_{L1}^{S-I}(s) - L_1 I_{L1}^{S-I}(0^+) &= \frac{V_{in}}{s} \\ \Rightarrow I_{L1}^{S-I}(s) &= \frac{V_{in}}{s^2 L_1} + \frac{I_{L1}^{S-I}(0^+)}{s}, \because I_{L1}^{S-I}(0^+) = I_{L1\min}^{S-I} \end{aligned} \quad (\text{A2.15b})$$

Now, after performing the inverse Laplace transform.

$$i_{L1}^{S-I}(t) = I_{L1\min}^{S-I} + \left(\frac{V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_6) = I_{L1\max}^{S-I}, \quad (A2.15c)$$

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \quad (A2.16a)$$

In (A2.16a), only the initial condition changes remaining are analogous to (A2.10b).

$$i_{Lb1}^{S-I}(t) = I_{b4}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_6) = I_{Lb1\min}^{S-I} \quad (A2.16b)$$

$$v_{Cr1}^{S-I}(t) = V_{01} \cos(\omega_{r1}t), \text{ from mode 5}$$

$$\text{at } t = t_5, v_{Cr1}^{S-I}(t_5) = 0$$

$$\Rightarrow \cos(\omega_{r1}t_5) = 0, \Rightarrow \omega_{r1}t_5 = \frac{\pi}{2}, \Rightarrow t_5 = \frac{\pi}{2\omega_{r1}} \quad (A2.17)$$

$$\therefore i_{Lr1}^{S-I}(t) = I_{Lr}^{S-I} + \frac{V_{01}}{Z_{r1}} \sin(\omega_{r1}t_5), \text{ from mode 5}$$

$$\Rightarrow i_{Lr1}^{S-I}(t) = I_{Lr}^{S-I} + \frac{V_{01}}{Z_{r1}} = I_{rp}^{S-I}$$

7) For mode 7

$$i_{L1}^{S-I}(t) \approx i_{L1}^{S-I}(t_6) \approx i_{L1}^{S-I}(t_7) \approx I_{L1\max}^{S-I}, \quad (A2.18)$$

$$\Rightarrow i_{L1}^{S-I}(t) = i_{Cr1}^{S-I}(t) + i_{Lb1}^{S-I}(t)$$

$$\Rightarrow i_{Cr1}^{S-I}(t) = i_{L1}^{S-I}(t) - i_{Lb1}^{S-I}(t)$$

$$\Rightarrow i_{Cr1}^{S-I}(t) = I_{L1\max}^{S-I} - i_{Lb1}^{S-I}(t), \text{ from (A2.18)} \quad (A2.19a)$$

$$\Rightarrow \frac{dv_{Cr1}^{S-I}(t)}{dt} = \frac{I_{L1\max}^{S-I}}{C_{r1}} - \frac{di_{Lb1}^{S-I}(t)}{C_{r1}}$$

Now, taking the Laplace transform of (A2.19a) and considering the initial conditions.

$$\Rightarrow \left[sV_{Cr1}^{S-I}(s) - V_{Cr1}^{S-I}(0^+) \right] = \frac{I_{L1\max}^{S-I}}{sC_{r1}} - \frac{I_{Lb1}^{S-I}(s)}{C_{r1}} \quad (A2.19b)$$

$$\Rightarrow V_{Cr1}^{S-I}(s) = \frac{I_{L1\max}^{S-I}}{s^2C_{r1}} - \frac{I_{Lb1}^{S-I}(s)}{sC_{r1}}$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$\Rightarrow v_{Cr1}^{S-I}(t) = \frac{1}{C_{r1}} \left(I_{L1\max}^{S-I} \times t - \int_0^t i_{Lb1}^{S-I}(\tau) d\tau \right) \quad (\text{A2.19c})$$

Now, solving for inductor current $i_{Lb1}(t)$,

$$\begin{aligned} \Rightarrow v_{Cr1}^{S-I}(t) - v_{Lr1}^{S-I}(t) - V_{bat} &= L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} \\ \Rightarrow \frac{di_{Lb1}^{S-I}(t)}{dt} &= \frac{1}{L_{b1}} \left(v_{Cr1}^{S-I}(t) - V_{bat} - L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} \right) \end{aligned} \quad (\text{A2.20a})$$

Now, taking the Laplace transform of (A2.20a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow \left[sI_{Lb1}^{S-I}(s) - I_{Lb1}^{S-I}(0^+) \right] &= \frac{1}{L_{b1}} \left(V_{Cr1}^{S-I}(s) - \frac{V_{bat}}{s} - L_{r1} \left[sI_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] \right) \\ I_{Lb1}^{S-I}(s) &= \frac{I_{Lb1}^{S-I}(0^+)}{s} + \frac{1}{sL_{b1}} \left(V_{Cr1}^{S-I}(s) - \frac{V_{bat}}{s} - L_{r1} \left[sI_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] \right) \\ \therefore I_{Lb1}^{S-I}(0^+) &= I_{Lb1}^{S-I}(t_6) = I_{Lb1\min}^{S-I} \\ \therefore I_{Lr1}^{S-I}(0^+) &= I_{Lr1}^{S-I}(t_6) = I_{rp}^{S-I} \end{aligned} \quad (\text{A2.20b})$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$\begin{aligned} i_{Lb1}^{S-I}(t) &= I_{Lb1\min}^{S-I} - \frac{1}{L_{b1}} \left(V_{bat} \times t - L_{r1} I_{rp}^{S-I} - \int_0^t v_{Cr1}^{S-I}(\tau) d\tau + L_{r1} i_{Lr1}^{S-I}(t) \right), \\ i_{Lb1}^{S-I}(t_7) &= I_{b5}^{S-I} \end{aligned} \quad (\text{A2.20c})$$

Now, solving for inductor current $i_{Lr1}(t)$,

$$\begin{aligned} \Rightarrow i_{Lr1}^{S-I}(t) &= i_{Ca1}^{S-I}(t) + i_{Lb1}^{S-I}(t) \\ \Rightarrow \frac{dv_{Ca1}^{S-I}(t)}{dt} &= \frac{1}{C_{a1}} \left(i_{Lr1}^{S-I}(t) - i_{Lb1}^{S-I}(t) \right) \\ \Rightarrow v_{Lr1}^{S-I}(t) + v_{Ca1}^{S-I}(t) &= 0 \\ \text{differentiating above} \\ \Rightarrow \dot{v}_{Lr1}^{S-I}(t) + \dot{v}_{Ca1}^{S-I}(t) &= 0 \end{aligned}$$

$$\begin{aligned} \because \omega_{a1} &= \frac{1}{\sqrt{L_{r1}C_{a1}}}, Z_{a1} = \sqrt{L_{r1}/C_{a1}}, \\ \Rightarrow \frac{d^2 i_{Lr1}^{S-I}(t)}{dt^2} + \omega_{a1}^2 i_{Lr1}^{S-I}(t) &= \omega_{a1}^2 i_{Lb1}^{S-I}(t) \end{aligned} \quad (A2.21a)$$

Now, taking the Laplace transform of (A2.21a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow \left[s^2 I_{Lr1}^{S-I}(s) - s I_{Lr1}^{S-I}(0^+) - i_{Lr1}^{S-I}(0^+) \right] + \omega_{a1}^2 I_{Lr1}^{S-I}(s) &= \omega_{a1}^2 I_{Lb1}^{S-I}(s) \\ \Rightarrow \left(s^2 + \omega_{a1}^2 \right) I_{Lr1}^{S-I}(s) &= s I_{Lr1}^{S-I}(0^+) + i_{Lr1}^{S-I}(0^+) + \omega_{a1}^2 I_{Lb1}^{S-I}(s) \\ \Rightarrow I_{Lr1}^{S-I}(s) &= \frac{s I_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{a1}^2} + \frac{i_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{a1}^2} + \frac{\omega_{a1}^2 I_{Lb1}^{S-I}(s)}{s^2 + \omega_{a1}^2} \\ \because I_{Lr1}^{S-I}(0^+) &= I_{rp}^{S-I}, i_{Lr1}^{S-I}(0^+) = 0. \end{aligned} \quad (A2.21b)$$

$$\Rightarrow I_{Lr1}^{S-I}(s) = \frac{s I_{rp}^{S-I}}{s^2 + \omega_{a1}^2} + \left(\frac{\omega_{a1}^2}{s^2 + \omega_{a1}^2} \right) I_{Lb1}^{S-I}(s)$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$i_{Lr1}^{S-I}(t) = I_{rp}^{S-I} \cos(\omega_{a1}t) + \omega_{a1} \int_0^t i_{Lb1}^{S-I}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau \quad (A2.21c)$$

Solving for capacitor voltage $v_{Ca1}(t)$,

$$\begin{aligned} \Rightarrow v_{Ca1}^{S-I}(t) &= -v_{Lr1}^{S-I}(t) \\ \Rightarrow v_{Ca1}^{S-I}(t) &= -L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} \end{aligned} \quad (A2.22a)$$

Differentiating (A2.21c) and using the Leibniz rule,

$$v_{Ca1}^{S-I}(t) = I_{rp}^{S-I} Z_{a1} \sin(\omega_{a1}t) - \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-I}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau \quad (A2.22b)$$

8) For mode 8

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (A2.23a)$$

In (A2.23a), only the initial condition changes remaining are analogous to (A2.1c).

$$i_{L1}^{S-I}(t) = I_{L1\max}^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_8) = I_4^{S-I}, \quad (\text{A2.23b})$$

Now, solving for inductor current $i_{Lr1}(t)$,

$$\Rightarrow i_{Ca1}^{S-I}(t) = i_{Lr1}^{S-I}(t) + i_{Lb1}^{S-I}(t) \quad (\text{A2.24a})$$

In this mode, $V_{ca1}(t_7)$ is at maxima which is only possible when $\omega_{a1}t_7 = \frac{\pi}{2}$, putting this in (A2.22b) as given below,

$$v_{Ca1}^{S-I} \Big|_{t_7} = I_{rp}^{S-I} Z_{a1} - \frac{1}{C_{a1}} \int_0^{\pi/2\omega_{a1}} i_{Lb1}^{S-I}(\tau) \sin(\omega_{a1}\tau) d\tau, \quad (\text{A2.24b})$$

$$\Rightarrow v_{Lr1}^{S-I}(t) - v_{Ca1}^{S-I}(t) = -V_{01} \quad (\text{A2.24c})$$

$$\Rightarrow i_{Lr1}^{S-I}(t) = \frac{-V_{01}}{L_{r1}} + \frac{v_{Ca1}^{S-I}(t)}{L_{r1}}, \text{ putting } t=0, \quad (\text{A2.24d})$$

$$\Rightarrow i_{Lr1}^{S-I}(0) = \frac{-V_{01}}{L_{r1}} + \frac{v_{Ca1}^{S-I}(0)}{L_{r1}}$$

$$\because v_{Ca1}^{S-I}(0) = v_{Ca1}^{S-I}(t_7)$$

$$i_{Lr1}^{S-I}(0) = \frac{-V_{01}}{L_{r1}} + \frac{v_{Ca1}^{S-I}(t_7)}{L_{r1}} \quad (\text{A2.24e})$$

differentiating (A2.24c)

$$\Rightarrow \dot{v}_{Lr1}^{S-I}(t) - \dot{v}_{Ca1}^{S-I}(t) = 0 \quad (\text{A2.24f})$$

$$\Rightarrow \frac{d^2 i_{Lr1}^{S-I}(t)}{dt^2} + \omega_{a1}^2 i_{Lr1}^{S-I}(t) = -\omega_{a1}^2 i_{Lb1}^{S-I}(t)$$

Now, taking the Laplace transform of (A2.24f) and considering the initial conditions.

$$\Rightarrow \left[s^2 I_{Lr1}^{S-I}(s) - s I_{Lr1}^{S-I}(0^+) - i_{Lr1}^{S-I}(0^+) \right] + \omega_{a1}^2 I_{Lr1}^{S-I}(s) = -\omega_{a1}^2 I_{Lb1}^{S-I}(s)$$

$$\Rightarrow (s^2 + \omega_{a1}^2) I_{Lr1}^{S-I}(s) = s I_{Lr1}^{S-I}(0^+) + i_{Lr1}^{S-I}(0^+) - \omega_{a1}^2 I_{Lb1}^{S-I}(s)$$

$$\Rightarrow I_{Lr1}^{S-I}(s) = \frac{s I_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{a1}^2} + \frac{i_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{a1}^2} - \frac{\omega_{a1}^2 I_{Lb1}^{S-I}(s)}{s^2 + \omega_{a1}^2}$$

$$\begin{aligned} \because I_{Lr1}^{S-I}(0^+) &= 0. \\ \Rightarrow I_{Lr1}^{S-I}(s) &= \frac{i_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{a1}^2} - \frac{\omega_{a1}^2 I_{Lb1}^{S-I}(s)}{s^2 + \omega_{a1}^2} \end{aligned} \quad (\text{A2.24g})$$

Putting (A2.24e) in (A2.24g), and after performing the inverse Laplace transform and using the convolution theorem.

$$i_{Lr1}^{S-I}(t) = \frac{\left(V_{ca1}^{S-I} \Big|_{t_7} - V_{01} \right) \sin(\omega_{a1} t)}{Z_{a1}} - \omega_{a1} \int_0^t i_{Lb1}^{S-I}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau \quad (\text{A2.24h})$$

Solving for capacitor voltage $v_{Ca1}(t)$,

$$\begin{aligned} \Rightarrow v_{Ca1}^{S-I}(t) &= V_{01} + v_{Lr1}^{S-I}(t) \\ \Rightarrow v_{Ca1}^{S-I}(t) &= V_{01} + L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} \end{aligned} \quad (\text{A2.25a})$$

Differentiating (A2.24h) and using the Leibniz rule,

$$\begin{aligned} v_{Ca1}^{S-I}(t) &= V_{01} - \left(V_{01} - v_{Ca1}^{S-I} \Big|_{t_7} \right) \cos(\omega_{a1} t) \\ &\quad - \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-I}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau = V_{C1}^{S-I}, \end{aligned} \quad (\text{A2.25b})$$

Now, solving for inductor current $i_{Lb1}(t)$,

$$\begin{aligned} \Rightarrow V_{01} - v_{Lr1}^{S-I}(t) - V_{bat} &= L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} \\ \Rightarrow \frac{di_{Lb1}^{S-I}(t)}{dt} &= \frac{1}{L_{b1}} \left(V_{01} - V_{bat} - L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} \right) \end{aligned} \quad (\text{A2.26a})$$

Now, taking the Laplace transform of (A2.26a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow \left[s I_{Lb1}^{S-I}(s) - I_{Lb1}^{S-I}(0^+) \right] &= \frac{1}{L_{b1}} \left(\frac{V_{01}}{s} - \frac{V_{bat}}{s} - L_{r1} \left[s I_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] \right) \\ I_{Lb1}^{S-I}(s) &= \frac{I_{Lb1}^{S-I}(0^+)}{s} + \frac{1}{s L_{b1}} \left(\frac{V_{01}}{s} - \frac{V_{bat}}{s} - L_{r1} \left[s I_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] \right) \\ \because I_{Lb1}^{S-I}(0^+) &= I_{Lb1}^{S-I}(t_7) = I_{b5}^{S-I} \\ \because I_{Lr1}^{S-I}(0^+) &= I_{Lr1}^{S-I}(t_7) = 0 \end{aligned} \quad (\text{A2.26b})$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$i_{Lb1}^{S-I}(t) = I_{b5}^{S-I} + \frac{1}{L_{b1}} \left((V_{01} - V_{bat}) \times t - L_{r1} i_{Lr1}^{S-I}(t) \right), \quad (A2.26c)$$

$$i_{Lb1}^{S-I}(t_8) = I_{b6}^{S-I}, \quad i_{Lr1}^{S-I}(t_8) = I_{r1}^{S-I}$$

9) For mode 9

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (A2.27a)$$

In (A2.27a), only the initial condition changes remaining are analogous to (A2.1c).

$$i_{L1}^{S-I}(t) = I_4^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_9) = I_5^{S-I}, \quad (A2.27b)$$

Now, solving for inductor current $i_{Lr1}(t)$,

$$\Rightarrow V_{01} + v_{Lr1}^{S-I}(t) = 0$$

$$\Rightarrow V_{01} + L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} = 0 \quad (A2.28a)$$

Now, taking the Laplace transform of (A2.28a) and considering the initial conditions.

$$\Rightarrow \left[s I_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] = - \frac{V_{01}}{s L_{r1}}$$

$$\Rightarrow I_{Lr1}^{S-I}(s) = \frac{I_{Lr1}^{S-I}(0^+)}{s} - \frac{V_{01}}{s^2 L_{r1}} \quad (A2.28b)$$

$$\therefore I_{Lr1}^{S-I}(0^+) = i_{Lr1}^{S-I}(t_8) = I_{r1}^{S-I}.$$

$$\Rightarrow I_{Lr1}^{S-I}(s) = I_{r1}^{S-I} - \frac{V_{01}}{s^2 L_{r1}}$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$i_{Lr1}^{S-I}(t) = I_{r1}^{S-I} - \frac{V_{01}}{L_{r1}} t \quad (A2.28c)$$

Now, solving for inductor current $i_{Lb1}(t)$,

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \quad (\text{A2.29a})$$

In (A2.29a), only the initial condition changes remaining are analogous to (A2.10b).

$$i_{Lb1}^{S-I}(t) = I_{b6}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_9) = I_{b7}^{S-I}, \quad (\text{A2.29b})$$

10) For mode 10

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (\text{A2.30a})$$

In (A2.30a), only the initial condition changes remaining are analogous to (A2.1c).

$$i_{L1}^{S-I}(t) = I_3^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad i_{L1}^{S-I}(t_{12}) = I_6^{S-I}, \quad (\text{A2.30b})$$

Now, solving for inductor current $i_{Lr1}(t)$,

$$\begin{aligned} \Rightarrow i_{Lr1}^{S-I}(t) &= i_{Ca1}^{S-I}(t) \\ \Rightarrow v_{Lr1}^{S-I}(t) + v_{Ca1}^{S-I}(t) &= 0 \\ \Rightarrow L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} + \frac{1}{C_{a1}} \int i_{Lr1}^{S-I}(t).dt &= 0 \end{aligned} \quad (\text{A2.31a})$$

Now, taking the Laplace transform of (A2.31a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow \left[sI_{Lr1}^{S-I}(s) - I_{Lr1}^{S-I}(0^+) \right] + \frac{I_{Lr1}^{S-I}(s)}{sC_{a1}} &= 0 \\ \Rightarrow \left(sL_{r1} + \frac{1}{sC_{a1}} \right) I_{Lr1}^{S-I}(s) &= L_{r1} I_{Lr1}^{S-I}(0^+) \\ \because I_{Lr1}^{S-I}(0^+) &= I_{Lb1\max}^{S-I}, \text{ from mode 3} \\ \Rightarrow \left(s^2 + \omega_{a1}^2 \right) I_{Lr1}^{S-I}(s) &= sI_{Lb1\max}^{S-I} \\ \Rightarrow I_{Lr1}^{S-I}(s) &= I_{Lb1\max}^{S-I} \left(\frac{s}{s^2 + \omega_{a1}^2} \right) \end{aligned} \quad (\text{A2.31b})$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$i_{Lr1}^{S-I}(t) = i_{Lb1\max}^{S-I} \cos(\omega_{a1}t) \quad (\text{A2.31c})$$

Now, solving for inductor current $i_{Lb1}(t)$,

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \quad (\text{A2.32a})$$

In (A2.32a), only the initial condition changes remaining are analogous to (A2.10b).

$$i_{Lb1}^{S-I}(t) = I_{Lb1\max}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-I}(t_{12}) = I_{b8}^{S-I}, \quad (\text{A2.32b})$$

Solving for capacitor voltage $v_{Ca1}(t)$,

$$\begin{aligned} \Rightarrow v_{Ca1}^{S-I}(t) &= v_{Lr1}^{S-I}(t) \\ \Rightarrow v_{Ca1}^{S-I}(t) &= L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} \end{aligned} \quad (\text{A2.33a})$$

Differentiating (A2.31c),

$$v_{Ca1}^{S-I}(t) = I_{Lb1\max}^{S-I} Z_{a1} \sin(\omega_{a1}t) \quad (\text{A2.33b})$$

11) For mode 11

$$L_1 \frac{di_{L1}^{S-I}(t)}{dt} = V_{in} - V_{01} \quad (\text{A2.34a})$$

In (A2.34a), only the initial condition changes remaining are analogous to (A2.1c).

$$i_{L1}^{S-I}(t) = I_6^{S-I} - \left(\frac{V_{01} - V_{in}}{L_1} \right) \times t, \quad (\text{A2.34b})$$

Now, solving for inductor current $i_{Lr1}(t)$,

$$\begin{aligned} \Rightarrow i_{Lr1}^{S-I}(t) &= i_{Ca1}^{S-I}(t) \\ \because v_{Lr1}^{S-I}(t) - v_{Ca1}^{S-I}(t) &= -V_{01}, \end{aligned}$$

differentiating above

$$\begin{aligned}
 &\Rightarrow \dot{v}_{Lr1}^{S-I}(t) = \dot{v}_{Ca1}^{S-I}(t), \\
 &\Rightarrow i_{Lr1}^{S-I}(t) = C_{a1} \frac{dv_{Lr1}^{S-I}(t)}{dt}, \\
 &\Rightarrow i_{Lr1}^{S-I}(t) = C_{a1} L_{r1} \frac{d^2 i_{Lr1}^{S-I}(t)}{dt^2}, \\
 &\because \omega_{a1} = \frac{1}{\sqrt{L_{r1} C_{a1}}}, \\
 &\Rightarrow \frac{d^2 i_{Lr1}^{S-I}(t)}{dt^2} + \omega_{a1}^2 i_{Lr1}^{S-I}(t) = 0
 \end{aligned} \tag{A2.35a}$$

Now, taking the Laplace transform of (A2.35a) and considering the initial conditions.

$$\begin{aligned}
 &\Rightarrow \left[s^2 I_{Lr1}^{S-I}(s) - s I_{Lr1}^{S-I}(0^+) - i_{Lr1}^{S-I}(0^+) \right] + \omega_{a1}^2 I_{Lr1}^{S-I}(s) = 0 \\
 &\Rightarrow \left(s^2 + \omega_{a1}^2 \right) I_{Lr1}^{S-I}(s) = s I_{Lr1}^{S-I}(0^+) + i_{Lr1}^{S-I}(0^+) \\
 &\Rightarrow I_{Lr1}^{S-I}(s) = \frac{s I_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{a1}^2} + \frac{i_{Lr1}^{S-I}(0^+)}{s^2 + \omega_{a1}^2} \\
 &\because I_{Lr1}^{S-I}(0^+) = I_{Lr1}^{S-I}(t_{12}) = 0, \text{ by (A2.31c)}
 \end{aligned} \tag{A2.35b}$$

$$\text{and } i_{Lr1}^{S-I}(0^+) = -\frac{V_{01}}{L_{r1}} + \frac{V_{Ca1}(0)}{L_{r1}}, \text{ by (A2.35a) and putting } t=0.$$

$$V_{Ca1}(0) = I_{Lb1\max}^{S-I} Z_{a1}, \text{ maxima at } t=0, \text{ in (A2.33b)}$$

$$\Rightarrow I_{Lr1}^{S-I}(s) = -\frac{V_{01}}{L_{r1} \omega_{a1}} \left(\frac{\omega_{a1}}{s^2 + \omega_{a1}^2} \right) + I_{Lb1\max}^{S-I} \left(\frac{\omega_{a1}}{s^2 + \omega_{a1}^2} \right)$$

Now, after performing the inverse Laplace transform.

$$i_{Lr1}^{S-I}(t) = \left(I_{Lb1\max}^{S-I} - \frac{V_{01}}{Z_{a1}} \right) \sin(\omega_{a1} t), \tag{A2.35c}$$

Now, solving for inductor current $i_{Lb1}(t)$,

$$L_{b1} \frac{di_{Lb1}^{S-I}(t)}{dt} = -V_{bat} \tag{A2.36a}$$

In (A2.36a), only the initial condition changes remaining are analogous to (A2.10b).

$$i_{Lb1}^{S-I}(t) = I_{b8}^{S-I} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad (A2.36b)$$

Solving for capacitor voltage $v_{Ca1}(t)$,

$$\begin{aligned} \Rightarrow v_{Ca1}^{S-I}(t) &= V_{01} + v_{Lr1}^{S-I}(t) \\ \Rightarrow v_{Ca1}^{S-I}(t) &= V_{01} + L_{r1} \frac{di_{Lr1}^{S-I}(t)}{dt} \end{aligned} \quad (A2.37a)$$

Differentiating (A2.35c),

$$v_{Ca1}^{S-I}(t) = V_{01} - \left(V_{01} - i_{Lb1max}^{S-I} Z_{a1} \right) \cos(\omega_{a1}t) \quad (A2.37b)$$

A.2.2 Mode-wise Analysis for State II Operation

The switching characteristics and operating modes in this state are shown in Figure 4.4 and Figure 4.5, respectively. Based on the operating modes, the time-domain analysis has been performed.

1) For mode 1

$$i_{Lr1}^{S-II}(t) = i_{Lb1}^{S-II}(t) \quad (A2.38a)$$

Now, taking the Laplace transform of (A2.38a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow (V_{bat} - V_{01}) - v_{Lr1}^{S-II}(t) &= L_{b1} \frac{di_{Lb1}^{S-II}(t)}{dt} \\ \Rightarrow \frac{di_{Lb1}^{S-II}(t)}{dt} &= \left(\frac{V_{bat} - V_{01}}{L_{b1}} \right) - \frac{L_{r1}}{L_{b1}} \frac{di_{Lr1}^{S-II}(t)}{dt} \\ \Rightarrow \frac{di_{Lb1}^{S-II}(t)}{dt} &= \left(\frac{V_{bat} - V_{01}}{L_{b1}} \right) - \frac{L_{r1}}{L_{b1}} \frac{di_{Lb1}^{S-II}(t)}{dt}, \text{ by (A2.38a)} \\ \Rightarrow (L_{b1} + L_{r1}) \frac{di_{Lb1}^{S-II}(t)}{dt} &= (V_{bat} - V_{01}) \end{aligned} \quad (A2.38b)$$

Now, taking the Laplace transform and considering the initial conditions.

$$\begin{aligned} \Rightarrow (L_{b1} + L_{r1}) \left[s I_{Lb1}^{S-II}(s) - I_{Lb1}^{S-II}(0^+) \right] &= \frac{(V_{bat} - V_{01})}{s} \\ \Rightarrow I_{Lb1}^{S-II}(s) &= \frac{I_{Lb1}^{S-II}(0^+)}{s} + \left(\frac{V_{01} - V_{bat}}{L_{b1} + L_{r1}} \right) \times \frac{1}{s^2} \\ \therefore I_{Lb1}^{S-II}(0^+) &= I_{Lb1}^{S-II}(t_0) \end{aligned} \quad (A2.38c)$$

Now, after performing the inverse Laplace transform.

$$i_{Lb1}^{S-II}(t) = i_{Lb1}^{S-II}(t_0) + \left(\frac{V_{bat} - V_{01}}{L_{r1} + L_{b1}} \right) \times t, \quad i_{Lr1}^{S-II}(t) = i_{Lb1}^{S-II}(t) \quad (A2.38d)$$

$$i_{Lb1}^{S-II}(t_1) = i_{Lr1}^{S-II}(t_1) = -I_{Lb1min}^{S-II}. \quad (A2.39)$$

2) For mode 2

$$L_{b1} \frac{di_{Lb1}^{S-II}(t)}{dt} = -V_{bat} \quad (A2.40a)$$

In (A2.40a), only the initial condition changes remaining are analogous to (A2.10b).

$$i_{Lb1}^{S-II}(t) = -I_{Lb1min}^{S-II} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-II}(t_2) = I_{b1}^{S-II}, \quad (A2.40b)$$

$$L_{r1} \frac{di_{Lr1}^{S-II}(t)}{dt} = -V_{01} \quad (A2.41a)$$

Now, taking the Laplace transform of (A2.41a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow L_{r1} \left[s I_{Lr1}^{S-II}(s) - I_{Lr1}^{S-II}(0^+) \right] &= -\frac{V_{01}}{s} \\ \Rightarrow s L_{r1} I_{Lr1}^{S-II}(s) - L_{r1} I_{Lr1}^{S-II}(0^+) &= -\frac{V_{01}}{s} \\ \Rightarrow I_{Lr1}^{S-II}(s) &= \frac{I_{Lr1}^{S-II}(0^+)}{s} - \frac{V_{01}}{s^2 L_{r1}}, \\ I_{Lr1}^{S-II}(0^+) &= i_{Lr1}^{S-II}(t_1) = -I_{Lb1min}^{S-II}, \\ \Rightarrow I_{Lr1}^{S-II}(s) &= \frac{-I_{Lb1min}^{S-II}}{s} - \frac{V_{01}}{s^2 L_{r1}} \end{aligned} \quad (A2.41b)$$

Now, after performing the inverse Laplace transform.

$$i_{Lr1}^{S-II}(t) = -I_{Lb1min}^{S-II} - \left(\frac{V_{01}}{L_{r1}} \right) \times t, \quad i_{Lr1}^{S-II}(t_2) = 0. \quad (A2.41c)$$

3) For mode 3

$$L_{b1} \frac{di_{Lb1}^{S-II}(t)}{dt} = -V_{bat} \quad (A2.42a)$$

In (A2.42a), only the initial condition changes remaining are analogous to (A2.10b).

$$i_{Lb1}^{S-II}(t) = I_{b1}^{S-II} - \left(\frac{V_{bat}}{L_{b1}} \right) \times t, \quad i_{Lb1}^{S-II}(t_3) = -I_{Lb1\max}^{S-II}, \quad (\text{A2.42b})$$

$$i_{Lr1}^{S-II}(t) = 0, \quad v_{Ca1}^{S-II}(t) = 0. \quad (\text{A2.43})$$

4) For mode 4

$$\begin{aligned} \Rightarrow i_{Lb1}^{S-II}(t) &= i_{Lr1}^{S-II}(t) + i_{Ca1}^{S-II}(t) \\ \Rightarrow i_{Ca1}^{S-II}(t) &= -i_{Lr1}^{S-II}(t) + i_{Lb1}^{S-II}(t) \\ \dot{v}_{Ca1}^{S-II}(t) &= \frac{1}{C_{a1}} \left(-i_{Lr1}^{S-II}(t) + i_{Lb1}^{S-II}(t) \right) \\ \therefore v_{Lr1}^{S-II}(t) &= v_{Ca1}^{S-II}(t) \text{ or} \\ i_{Lr1}^{S-II}(t) &= \frac{v_{Ca1}^{S-II}(t)}{L_{r1}} \end{aligned} \quad (\text{A2.44a})$$

differentiating above

$$\begin{aligned} \Rightarrow \dot{v}_{Lr1}^{S-II}(t) - \dot{v}_{Ca1}^{S-II}(t) &= 0, \\ \Rightarrow \frac{d^2 i_{Lr1}^{S-II}(t)}{dt^2} + \omega_{a1}^2 i_{Lr1}^{S-II}(t) &= \omega_{a1}^2 i_{Lb1}^{S-II}(t) \end{aligned}$$

Now, taking the Laplace transform of (A2.44a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow \left[s^2 I_{Lr1}^{S-II}(s) - s I_{Lr1}^{S-II}(0^+) - i_{Lr1}^{S-II}(0^+) \right] + \omega_{a1}^2 I_{Lr1}^{S-II}(s) &= \omega_{a1}^2 I_{Lb1}^{S-II}(s) \\ \Rightarrow (s^2 + \omega_{a1}^2) I_{Lr1}^{S-II}(s) &= s I_{Lr1}^{S-II}(0^+) + i_{Lr1}^{S-II}(0^+) + \omega_{a1}^2 I_{Lb1}^{S-II}(s) \\ \Rightarrow I_{Lr1}^{S-II}(s) &= \frac{s I_{Lr1}^{S-II}(0^+)}{s^2 + \omega_{a1}^2} + \frac{i_{Lr1}^{S-II}(0^+)}{s^2 + \omega_{a1}^2} + \frac{\omega_{a1}^2 I_{Lb1}^{S-II}(s)}{s(s^2 + \omega_{a1}^2)} \\ \therefore I_{Lr1}^{S-II}(0^+) &= I_{Lr1}^{S-II}(t_3) = 0, \\ \therefore i_{Lr1}^{S-II}(0^+) &= \frac{V_{Ca1}(0)}{L_{r1}} = 0, \text{ from previous mode} \\ \Rightarrow I_{Lr1}^{S-II}(s) &= \frac{\omega_{a1}^2 I_{Lb1}^{S-II}(s)}{s(s^2 + \omega_{a1}^2)} \end{aligned} \quad (\text{A2.44b})$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$i_{Lr1}^{S-II}(t) = \omega_{a1} \int_0^t i_{Lb1}^{S-II}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau, \quad (A2.44c)$$

Now, solving for inductor current $i_{Lb1}(t)$,

$$\begin{aligned} \Rightarrow V_{01} - v_{Lr1}^{S-II}(t) - V_{bat} &= L_{b1} \frac{di_{Lb1}^{S-II}(t)}{dt} \\ \Rightarrow \frac{di_{Lb1}^{S-II}(t)}{dt} &= \frac{1}{L_{b1}} \left(V_{01} - V_{bat} - L_{r1} \frac{di_{Lr1}^{S-II}(t)}{dt} \right) \end{aligned} \quad (A2.45a)$$

Now, taking the Laplace transform of (A2.45a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow \left[sI_{Lb1}^{S-II}(s) - I_{Lb1}^{S-II}(0^+) \right] &= \frac{1}{L_{b1}} \left(\frac{V_{01}}{s} - \frac{V_{bat}}{s} - L_{r1} \left[sI_{Lr1}^{S-II}(s) - I_{Lr1}^{S-II}(0^+) \right] \right) \\ I_{Lb1}^{S-II}(s) &= \frac{I_{Lb1}^{S-II}(0^+)}{s} + \frac{1}{sL_{b1}} \left(\frac{V_{01}}{s} - \frac{V_{bat}}{s} - L_{r1} \left[sI_{Lr1}^{S-II}(s) - I_{Lr1}^{S-II}(0^+) \right] \right) \\ \because I_{Lb1}^{S-II}(0^+) &= I_{Lb1}^{S-II}(t_3) = -I_{Lb1\max}^{S-II}, \\ \because I_{Lr1}^{S-II}(0^+) &= I_{Lr1}^{S-II}(t_3) = 0. \\ I_{Lb1}^{S-II}(s) &= \frac{-I_{Lb1\max}^{S-II}}{s} + \frac{1}{sL_{b1}} \left(\frac{V_{01}}{s} - \frac{V_{bat}}{s} - L_{r1} \left(sI_{Lr1}^{S-II}(s) \right) \right) \end{aligned} \quad (A2.45b)$$

Now, after performing the inverse Laplace transform and using the convolution theorem.

$$i_{Lb1}^{S-II}(t) = -I_{Lb1\max}^{S-II} + \left(\frac{V_{01} - V_{bat}}{L_{b1}} \right) \times t - \frac{L_{r1}}{L_{b1}} i_{Lr1}^{S-II}(t), \quad (A2.45c)$$

Solving for capacitor voltage $v_{Ca1}(t)$,

$$\begin{aligned} \Rightarrow v_{Ca1}^{S-II}(t) &= v_{Lr1}^{S-II}(t) \\ \Rightarrow v_{Ca1}^{S-II}(t) &= L_{r1} \frac{di_{Lr1}^{S-II}(t)}{dt} \end{aligned} \quad (A2.46a)$$

Differentiating (A2.44c),

$$v_{Ca1}^{S-II}(t) = \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-II}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau, \quad (A2.46b)$$

$$v_{Ca1}^{S-II}(t_4) = \frac{1}{C_{a1}} \int_0^{\pi/2\omega_{a1}} i_{Lb1}^{S-II}(\tau) \sin(\omega_{a1}\tau) d\tau, \quad (A2.46c)$$

$$i_{Lr1}^{S-II}(t_4) = \omega_{a1} \int_0^{\pi/2\omega_{a1}} i_{Lb1}^{S-II}(\tau) \cos(\omega_{a1}\tau) d\tau, \quad i_{Lb1}^{S-II}(t_4) = I_{b2}^{S-II},$$

by putting $\omega_{a1}t = \frac{\pi}{2}$, at maxima.

5) For mode 5

In (A2.47) and (A2.48), only the initial condition changes remaining are analogous to (A2.44c) and (A2.45c).

$$i_{Lr1}^{S-II}(t) = i_{Lr1}^{S-II}(t_4) \cos(\omega_{a1}t) - \left(\frac{V_{01} - v_{Ca1}^{S-II}(t_4)}{Z_{a1}} \right) \sin(\omega_{a1}t) + \omega_{a1} \int_0^t i_{Lb1}^{S-II}(\tau) \sin(\omega_{a1}(t-\tau)) d\tau. \quad (A2.47)$$

$$i_{Lb1}^{S-II}(t) = i_{b2}^{S-II} + \frac{(V_{01} - V_{bat}) \times t}{L_{b1}} + \frac{L_{r1}}{L_{b1}} i_{Lr1}^{S-II}(t_4) - \frac{L_{r1}}{L_{b1}} i_{Lr1}^{S-II}(t), \quad (A2.48)$$

Solving for capacitor voltage $v_{Ca1}(t)$,

$$\Rightarrow v_{Ca1}^{S-II}(t) = V_{01} + v_{Lr1}^{S-II}(t) \quad (A2.49a)$$

$$\Rightarrow v_{Ca1}^{S-II}(t) = V_{01} + L_{r1} \frac{di_{Lr1}^{S-II}(t)}{dt}$$

Differentiating (A2.47),

$$v_{Ca1}^{S-II}(t) = V_{01} - (V_{01} - v_{Ca1}^{S-II}(t_4)) \cos(\omega_{a1}t) - Z_{a1} i_{Lr1}^{S-II}(t_4) \sin(\omega_{a1}t) + \frac{1}{C_{a1}} \int_0^t i_{Lb1}^{S-II}(\tau) \cos(\omega_{a1}(t-\tau)) d\tau, \quad (A2.49b)$$

$$i_{Lr1}^{S-II}(t_5) = I_{r1}^{S-II}. \quad (A2.50)$$

6) For mode 6

$$i_{Lb1}^{S-II}(t) = I_{b1}^{S-II}(t) \approx -I_{Lb1\max}^{S-II} \quad (A2.51)$$

$$L_{r1} \frac{di_{Lr1}^{S-II}(t)}{dt} = -V_{01} \quad (A2.52a)$$

Now, taking the Laplace transform of (A2.52a) and considering the initial conditions.

$$\begin{aligned} \Rightarrow L_{r1} \left[sI_{Lr1}^{S-II}(s) - I_{Lr1}^{S-II}(0^+) \right] &= -\frac{V_{01}}{s} \\ \Rightarrow sL_{r1}I_{Lr1}^{S-II}(s) - L_{r1}I_{Lr1}^{S-II}(0^+) &= -\frac{V_{01}}{s} \\ \Rightarrow I_{Lr1}^{S-II}(s) &= -\frac{V_{01}}{s^2 L_{r1}} + \frac{I_{Lr1}^{S-II}(0^+)}{s}, \\ \Rightarrow I_{Lr1}^{S-II}(0^+) &= I_{Lr1}^{S-II}(t_5) = I_{r1}^{S-II}, \\ \Rightarrow I_{Lr1}^{S-II}(s) &= \frac{I_{r1}^{S-II}}{s} - \frac{V_{01}}{s^2 L_{r1}} \end{aligned} \quad (A2.52b)$$

Now, after performing the inverse Laplace transform.

$$i_{Lr1}^{S-II}(t) = I_{r1}^{S-II} - \left(\frac{V_{01}}{L_{r1}} \right) \times t, \quad v_{Ca1}^{S-II}(t) = 0. \quad (A2.53)$$

A.3 State-space Modeling and Small-signal Analysis Under Different Operating States for FPFTDC Converter in Ideal Conditions

The state-space modelling and small-signal analysis of the proposed FPFTDC converter under ideal operating conditions are carried out in CCM to investigate the dynamic behaviour and stability characteristics of the system under different operating states. The operating mode circuits corresponding to states I, III, and IV are illustrated in Figure 5.6, Figure 5.9, and Figure 5.11, respectively, while the associated switching characteristics durations are summarized in Table 5.2, Table 5.4, and Table 5.5. Based on the switching sequence and energy transfer paths in each operating state, the converter dynamics are analyzed using the state-space averaging approach. For each state, the large-signal state equations are formulated by applying Kirchhoff's voltage and current laws considering the inductor currents and capacitor voltages as the state variables. Subsequently, the averaged state-space model is derived over one complete switching period to represent the overall converter dynamics in CCM operation.

Further, small-signal perturbation and linearization are performed around the steady-state operating point to obtain the SSM of the converter. The derived SSM is

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utilized for analyzing the dynamic response, transfer function characteristics, and stability behaviour of the proposed converter under different operating conditions. In *state* II, the MVDC load is disconnected, resulting in a decrease in the steady-state current. However, the remaining operating constraints and dynamic characteristics remain similar to those of *state* I. Therefore, the SSM for *state* II are derived following a similar modeling procedure with suitable.

For *state* I & II operation, the state equations (A3.1) to (A3.7) are common and equations (A3.8) and (A3.9) for *states* I & II, respectively, are given below:

$$V_{Ls1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv}, \text{ switch } S_{s1} \text{ is On} \quad (\text{A3.1a})$$

$$V_{Ls1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv} - v_{c01}, \text{ switch } S_{s1} \text{ is Off} \quad (\text{A3.1b})$$

$$V_{Ls2} = L_{S2} \frac{di_{S2}}{dt} = V_{pv}, \text{ switch } S_{s2} \text{ is On} \quad (\text{A3.2a})$$

$$V_{Ls2} = L_{S2} \frac{di_{S2}}{dt} = V_{pv} - v_{c01}, \text{ switch } S_{s2} \text{ is Off} \quad (\text{A3.2b})$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = v_{c01} - v_{c02}, \text{ switch } S_{b2} \text{ is On} \quad (\text{A3.3a})$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = -v_{c02}, \text{ switch } S_{b2} \text{ is Off} \quad (\text{A3.3b})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = v_{c01} - v_{cfb}, \text{ switch } S_{b1} \text{ is On} \quad (\text{A3.4a})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = -v_{cfb}, \text{ switch } S_{b1} \text{ is Off} \quad (\text{A3.4b})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = v_{c01} - v_{cfb}, \text{ switch } S_{bb1} \text{ is On} \quad (\text{A3.5a})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = -v_{cfb}, \text{ switch } S_{bb1} \text{ is Off} \quad (\text{A3.5b})$$

$$i_{c02} = i_{L02} - i_{02} \quad (\text{A3.6})$$

$$i_{cfb} = i_{b1} + i_{b2} - i_{bat} \quad (\text{A3.7})$$

$$\begin{aligned} i_{c01} &= i_{S2} - i_{b1} - i_{01}, \text{ mode } 1, \forall (D_1 - D_3) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b1} - i_{01}, \text{ mode } 2, \forall (D_2 - D_1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{01}, \text{ mode } 3, \forall (1 - 2D_2) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b2} - i_{01}, \text{ mode } 4, \forall (D_2 - D_1) \times T \\ i_{c01} &= i_{S1} - i_{b2} - i_{01}, \text{ mode } 5, \forall (D_1) \times T \\ i_{c01} &= i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 6, \forall (D_3) \times T \end{aligned} \quad \text{for state I} \quad (\text{A3.8})$$

$$\text{where, } i_{01} = \frac{v_{c01}}{R_{01}}, i_{02} = \frac{v_{c02}}{R_{02}}, i_{bat} = \frac{v_{cfb}}{R_{03}}, i_{c01} = C_{01} \frac{dv_{c01}}{dt}$$

$$\begin{aligned}
 i_{c01} &= i_{S2} - i_{b1}, \text{ mode } 1, \forall (D_1 - D_3) \times T \\
 i_{c01} &= i_{S1} + i_{S2} - i_{b1}, \text{ mode } 2, \forall (D_2 - D_1) \times T \\
 i_{c01} &= i_{S1} + i_{S2}, \text{ mode } 3, \forall (1 - 2D_2) \times T \quad \text{for state II} \\
 i_{c01} &= i_{S1} + i_{S2} - i_{b2}, \text{ mode } 4, \forall (D_2 - D_1) \times T \\
 i_{c01} &= i_{S1} - i_{b2}, \text{ mode } 5, \forall (D_1) \times T \\
 i_{c01} &= i_{S2} - i_{b1} - i_{L02}, \text{ mode } 6, \forall (D_3) \times T
 \end{aligned} \tag{A3.9}$$

The matrices A_1 - A_6 in (A3.10) represent the state matrices corresponding to *state I* of the converter, whereas A denotes the averaged large-signal state matrix obtained through state-space averaging.

$$\begin{aligned}
 A_1 &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ 0 & \frac{-1}{C_{01}} & 0 & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} & A_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & \frac{-1}{C_{01}} & 0 & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} \\
 A_3 &= \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & 0 & 0 & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} & A_4 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & 0 & 0 & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix}
 \end{aligned}$$

$$A_5 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & 0 & 0 & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} \quad A_6 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & \frac{1}{L_{02}} & \frac{-1}{L_{02}} & 0 \\ 0 & \frac{-1}{C_{01}} & \frac{-1}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_{seq}} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad (A3.10)$$

The state-space representation is as follows:

(i). State equation: $\dot{\hat{x}} = \mathbf{A}\hat{x} + \mathbf{B}\hat{u} + \mathbf{E}\hat{d}_1$

(ii). Output equation: $y(t) = \mathbf{C}\hat{x} + \mathbf{D}\hat{u}$

Where the matrices **A**, **B**, **C** and **D** represent the system, input, output, and direct transmission matrices, and **E** is the state variable at steady-state.

State Variables and Input Vectors for state-I:

(i). State vector: $\hat{x}_1(t) = [\hat{i}_{in} \ \hat{i}_b \ \hat{i}_{L02} \ \hat{v}_{c01} \ \hat{v}_{c02} \ \hat{v}_{bat}]^T$

(ii). Input vector: $\hat{u}_1(t) = \hat{v}_{pv}$

Small-signal models for this state.

$\hat{x}_1(t) = A\hat{x}_1(t) + B\hat{u}_1(t) + E_1\hat{d}_1$; and $y_1(t) = C\hat{x}_1(t) + D\hat{u}_1(t)$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_b \\ \hat{i}_{L02} \\ \hat{v}_{c01} \\ \hat{v}_{c02} \\ \hat{v}_{bat} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-D_1)}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & \frac{D_2}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & \frac{D_3}{L_{02}} & \frac{-1}{L_{02}} & 0 \\ \frac{(1-D_1)}{C_{01}} & \frac{-D_2}{C_{01}} & \frac{-D_3}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} \hat{x}_1(t)$$

$$\begin{aligned}
 & + \begin{bmatrix} \frac{1}{L_{seq}} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{pv} \end{bmatrix} + \begin{bmatrix} \frac{V_{01}}{L_{seq}} & 0 & 0 \\ 0 & \frac{V_{01}}{L_{beq}} & 0 \\ 0 & 0 & \frac{V_{01}}{L_{02}} \\ \frac{-I_{in}}{C_{01}} & \frac{-I_b}{C_{01}} & \frac{-I_{L02}}{C_{01}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{d}_1 \\ \hat{d}_2 \\ \hat{d}_3 \end{bmatrix} \\
 & v_{01} = [0 \ 0 \ 0 \ 1 \ 0 \ 0] \hat{x}_1(t); v_{02} = [0 \ 0 \ 0 \ 0 \ 1 \ 0] \hat{x}_1(t); \text{ and } v_{bat} = [0 \ 0 \ 0 \ 0 \ 0 \ 1] \hat{x}_1(t)
 \end{aligned}
 \tag{A3.11}$$

The matrices A_1 - A_6 in (A3.12) represent the state matrices corresponding to *state* II of the converter, whereas A denotes the averaged large-signal state matrix obtained through state-space averaging.

$$\begin{aligned}
 A_1 &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ 0 & \frac{-1}{C_{01}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} & A_2 &= \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & \frac{-1}{C_{01}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{cb}} \end{bmatrix} \\
 A_3 &= \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} & A_4 &= \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix}
 \end{aligned}$$

$$A_5 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} & 0 \\ \frac{1}{C_{01}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix}$$

$$A_6 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & \frac{1}{L_{02}} & \frac{-1}{L_{02}} & 0 \\ 0 & \frac{-1}{C_{01}} & \frac{-1}{C_{01}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{L_{seq}} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad (A3.12)$$

State Variables and Input Vectors for *state-II*:

(i). State vector: $\hat{x}_2(t) = [\hat{i}_{in} \ \hat{i}_b \ \hat{i}_{L02} \ \hat{v}_{c01} \ \hat{v}_{c02} \ \hat{v}_{bat}]^T$

(ii). Input vector: $\hat{u}_2(t) = \hat{v}_{pv}$

Small-signal models for this state.

$$\dot{\hat{x}}_2(t) = A\hat{x}_2(t) + B\hat{u}_2(t) + E_2\hat{d}; \text{ and } y_2(t) = C\hat{x}_2(t) + D\hat{u}_2(t)$$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_b \\ \hat{i}_{L02} \\ \hat{v}_{c01} \\ \hat{v}_{c02} \\ \hat{v}_{bat} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-D_1)}{L_{seq}} & 0 & 0 \\ 0 & 0 & 0 & \frac{D_2}{L_{beq}} & 0 & \frac{-1}{L_{beq}} \\ 0 & 0 & 0 & \frac{D_3}{L_{02}} & \frac{-1}{L_{02}} & 0 \\ \frac{(1-D_1)}{C_{01}} & \frac{-D_2}{C_{01}} & \frac{-D_3}{C_{01}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} & 0 \\ 0 & \frac{1}{C_{fb}} & 0 & 0 & 0 & \frac{-1}{R_{03}C_{fb}} \end{bmatrix} \hat{x}_2(t)$$

$$\begin{aligned}
 & + \begin{bmatrix} \frac{1}{L_{seq}} & \frac{V_{01}}{L_{seq}} & 0 & 0 \\ 0 & 0 & \frac{V_{01}}{L_{beq}} & 0 \\ 0 & 0 & 0 & \frac{V_{01}}{L_{02}} \\ 0 & \frac{-I_{in}}{C_{01}} & \frac{-I_b}{C_{01}} & \frac{-I_{L02}}{C_{01}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{pv} \\ \hat{d}_1 \\ \hat{d}_2 \\ \hat{d}_3 \end{bmatrix} \\
 & v_{01} = [0 \ 0 \ 0 \ 1 \ 0 \ 0] \hat{x}_2(t); v_{02} = [0 \ 0 \ 0 \ 0 \ 1 \ 0] \hat{x}_2(t); \text{ and } v_{bat} = [0 \ 0 \ 0 \ 0 \ 0 \ 1] \hat{x}_2(t)
 \end{aligned}
 \tag{A3.13}$$

For *state III* operation, the state equations are given below:

$$V_{Ls1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv}, \text{ switch } S_{s1} \text{ is On} \tag{A3.14a}$$

$$V_{Ls1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv} - v_{c01}, \text{ switch } S_{s1} \text{ is Off} \tag{A3.14b}$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = v_{c01} - v_{c02}, \text{ switch } S_{b2} \text{ is On} \tag{A3.15a}$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = -v_{c02}, \text{ switch } S_{b2} \text{ is Off} \tag{A3.15b}$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = v_{c01} - v_{bat}, \text{ switch } S_{b2}, S_{b3} \text{ is On} \tag{A3.16a}$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = -v_{bat}, \text{ switch } S_{b3} \text{ is Off} \tag{A3.16b}$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = -v_{bat}, \text{ switch } S_{bb2} \text{ is On} \tag{A3.17a}$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = v_{c01} - v_{bat}, \text{ switch } S_{bb2} \text{ is Off} \tag{A3.17b}$$

$$i_{c02} = i_{L02} - i_{02} \tag{A3.18}$$

$$i_{cfb} = i_{b1} + i_{b2} - i_{bat} \tag{A3.19}$$

$$\begin{aligned}
 i_{c01} &= i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 1, \forall (D_1 + D_3 - 1) \times T \\
 i_{c01} &= i_{S1} + i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 2, \forall (1 - D_2 - D_1) \times T \\
 i_{c01} &= i_{S1} + i_{S2} - i_{01}, \text{ mode } 3, \forall (2D_2 - 1) \times T \\
 i_{c01} &= i_{S1} + i_{S2} - i_{b2} - i_{01}, \text{ mode } 4, \forall (1 - D_2 - D_1) \times T \\
 i_{c01} &= i_{S1} - i_{b2} - i_{01}, \text{ mode } 5, \forall (D_1) \times T \\
 i_{c01} &= i_{S2} - i_{b1} - i_{01}, \text{ mode } 6, \forall (1 - D_3) \times T
 \end{aligned}
 \tag{A3.20}$$

The matrices A_1 - A_6 in (A3.21) represent the state matrices corresponding to *state* III of the converter, whereas A denotes the averaged large-signal state matrix obtained through state-space averaging.

$$\begin{aligned}
 A_1 &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 \\ 0 & 0 & 0 & \frac{1}{L_{02}} & \frac{-1}{L_{02}} \\ 0 & \frac{-1}{C_{01}} & \frac{-1}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} & A_2 &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 \\ 0 & 0 & 0 & \frac{1}{L_{02}} & \frac{-1}{L_{02}} \\ 0 & \frac{-1}{C_{01}} & \frac{-1}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} \\
 A_3 &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 \\ 0 & 0 & 0 & \frac{1}{L_{02}} & \frac{-1}{L_{02}} \\ 0 & \frac{-1}{C_{01}} & \frac{-1}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} & A_4 &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} \\ 0 & 0 & \frac{-1}{R_{01}C_{01}} & 0 & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} \\
 A_5 &= \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_{seq}} & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} \\ \frac{1}{C_{01}} & 0 & 0 & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} & A_6 &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_{beq}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{02}} \\ 0 & \frac{-1}{C_{01}} & 0 & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} \\
 B &= \begin{bmatrix} \frac{1}{L_{seq}} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_{beq}} & 0 & 0 & 0 \end{bmatrix}^T
 \end{aligned} \tag{A3.21}$$

State Variables and Input Vectors for *state*-III:

$$(i). \text{ State vector: } \hat{x}_3(t) = \begin{bmatrix} \hat{i}_{in} & \hat{i}_b & \hat{i}_{L02} & \hat{v}_{c01} & \hat{v}_{c02} \end{bmatrix}^T$$

(ii). Input vector: $\hat{u}_3(t) = \begin{bmatrix} \hat{v}_{pv} & \hat{v}_{bat} \end{bmatrix}$.

Small-signal models for this state.

$\hat{x}_3(t) = A\hat{x}_3(t) + B\hat{u}_3(t) + E_3\hat{d}$; and $y_3(t) = C\hat{x}_3(t) + D\hat{u}_3(t)$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_b \\ \hat{i}_{L02} \\ \hat{v}_{c01} \\ \hat{v}_{c02} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-D_1)}{L_{seq}} & 0 \\ 0 & 0 & 0 & \frac{(1-D_2)}{L_{beq}} & 0 \\ 0 & 0 & 0 & \frac{(D_3-D_2)}{L_{02}} & \frac{-1}{L_{02}} \\ \frac{(1-D_1)}{C_{01}} & \frac{-(1-D_2)}{C_{01}} & \frac{-(D_3-D_2)}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} \hat{x}_3(t) + \begin{bmatrix} \frac{1}{L_{seq}} & 0 & \frac{V_{01}}{L_{seq}} & 0 & 0 \\ 0 & \frac{-1}{L_{beq}} & 0 & \frac{-V_{01}}{L_{beq}} & 0 \\ 0 & 0 & 0 & \frac{-V_{01}}{L_{02}} & \frac{V_{01}}{L_{02}} \\ 0 & 0 & \frac{-I_{in}}{C_{01}} & \frac{(I_b + I_{L02})}{C_{01}} & \frac{-I_{L02}}{C_{01}} \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{pv} \\ \hat{v}_{bat} \\ \hat{d}_1 \\ \hat{d}_2 \\ \hat{d}_3 \end{bmatrix}$$

$v_{01} = [0 \ 0 \ 0 \ 1 \ 0] \hat{x}_3(t)$; and $v_{02} = [0 \ 0 \ 0 \ 0 \ 1] \hat{x}_3(t)$.

(A3.22)

For *state IV* operation, the state equations are given below:

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = v_{c01} - v_{c02}, \text{switch } S_{b2} \text{ is On} \quad (\text{A3.23a})$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = -v_{c02}, \text{switch } S_{b2} \text{ is Off} \quad (\text{A3.23b})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = v_{c01} - v_{bat}, \text{switch } S_{b2}, S_{b3} \text{ is On} \quad (\text{A3.24a})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = -v_{bat}, \text{switch } S_{b3} \text{ is Off} \quad (\text{A3.24b})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = -v_{bat}, \text{switch } S_{bb2} \text{ is On} \quad (\text{A3.25a})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = v_{c01} - v_{bat}, \text{ switch } S_{bb2} \text{ is Off} \quad (\text{A3.25b})$$

$$i_{c02} = i_{L02} - i_{02} \quad (\text{A3.26})$$

$$i_{cfb} = i_{b1} + i_{b2} - i_{bat} \quad (\text{A3.27})$$

$$\begin{aligned} i_{c01} &= i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 1, \forall (D_1 + D_3 - 1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 2, \forall (1 - D_2 - D_1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{01}, \text{ mode } 3, \forall (2D_2 - 1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b2} - i_{01}, \text{ mode } 4, \forall (1 - D_2 - D_1) \times T \\ i_{c01} &= i_{S1} - i_{b2} - i_{01}, \text{ mode } 5, \forall (D_1) \times T \\ i_{c01} &= i_{S2} - i_{b1} - i_{01}, \text{ mode } 6, \forall (1 - D_3) \times T \end{aligned} \quad (\text{A3.28})$$

The matrices A_1 - A_4 in (A3.29) represent the state matrices corresponding to *state IV* of the converter, whereas A denotes the averaged large-signal state matrix obtained through state-space averaging.

$$\begin{aligned} A_1 &= \begin{bmatrix} 0 & 0 & \frac{1}{L_{beq}} & 0 \\ 0 & 0 & \frac{1}{L_{02}} & \frac{-1}{L_{02}} \\ -\frac{1}{C_{01}} & -\frac{1}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} & A_2 &= \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_{02}} \\ 0 & 0 & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} \\ A_3 &= \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_{02}} \\ 0 & 0 & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} & A_4 &= \begin{bmatrix} 0 & 0 & \frac{1}{L_{beq}} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_{02}} \\ \frac{-1}{C_{01}} & 0 & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} \end{aligned}$$

$$B = \begin{bmatrix} \frac{-1}{L_{beq}} & 0 & 0 & 0 \end{bmatrix}^T \quad (\text{A3.29})$$

State Variables and Input Vectors for *state-IV*:

$$(i). \text{ State vector: } \hat{x}_4(t) = \begin{bmatrix} \hat{i}_b & \hat{i}_{L02} & \hat{v}_{c01} & \hat{v}_{c02} \end{bmatrix}^T$$

(ii). Input vector: $\hat{u}_4(t) = \begin{bmatrix} \hat{v}_{bat} \end{bmatrix}$.

Small-signal models for this state.

$$\hat{x}_4(t) = A\hat{x}_4(t) + B\hat{u}_4(t) + E_4\hat{d}; \text{ and } y_4(t) = C\hat{x}_4(t) + D\hat{u}_4(t)$$

$$\begin{bmatrix} \hat{i}_b \\ \hat{i}_{L02} \\ \hat{v}_{c01} \\ \hat{v}_{c02} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{(1-D_2)}{L_{beq}} & 0 \\ 0 & 0 & \frac{(D_3-D_2)}{L_{02}} & \frac{-1}{L_{02}} \\ \frac{-(1-D_2)}{C_{01}} & \frac{-(D_3-D_2)}{C_{01}} & \frac{-1}{R_{01}C_{01}} & 0 \\ 0 & \frac{1}{C_{02}} & 0 & \frac{-1}{R_{02}C_{02}} \end{bmatrix} \hat{x}_4(t) + \begin{bmatrix} \frac{-1}{L_{beq}} & \frac{-V_{01}}{L_{beq}} & 0 \\ 0 & \frac{-V_{01}}{L_{02}} & \frac{V_{01}}{L_{02}} \\ 0 & \frac{(I_b + I_{L02})}{C_{01}} & \frac{-I_{L02}}{C_{01}} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{bat} \\ \hat{d}_2 \\ \hat{d}_3 \end{bmatrix} \quad (A3.30)$$

$$v_{01} = [0 \ 0 \ 1 \ 0] \hat{x}_4(t); \text{ and } v_{02} = [0 \ 0 \ 0 \ 1] \hat{x}_4(t)$$

A.3.1 State-space Modeling and Small-signal Analysis for Input Capacitor Design (C_{pv})

The PWM to the switches S_{S1} and S_{S2} are 180° phase-shifted, which produces only three modes of operation as shown in Figure A.3.1. During *mode 1*, only switch S_{S1} is turned on and switch S_{S2} is turned off with a duty ratio D_1 . During *mode 2*, both the switches are turned off with a duty ratio of $(1-2D_1)$ and during *mode 3*, switch S_{S2} is turned on and switch S_{S1} is turned off with a duty ratio of D_1 . The state-space representation and SSM of single-diode PV modules have been carried out to design the input capacitor (C_{pv}).

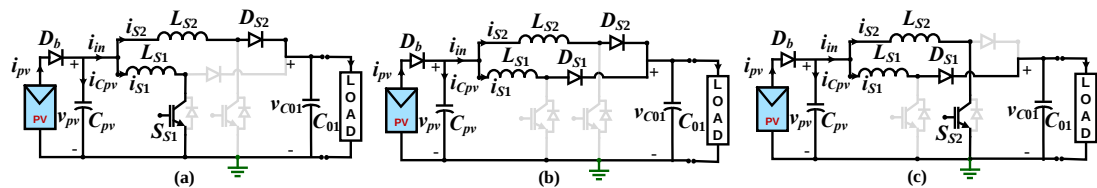


Figure A.3.1 Two-phase interleaved boost converter for (a) mode 1, (b) mode 2, and (c) mode 3 operation.

1

The generalized state-space equation can be written as follows:

$$\dot{\hat{\mathbf{x}}} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}} \quad (\text{A3.31})$$

where the state and input vector can be written as follows:

$$\hat{\mathbf{x}}(t) = [\hat{i}_{S1} \quad \hat{i}_{S2} \quad \hat{v}_{pv}]^T, \quad \hat{\mathbf{u}}(t) = \hat{v}_{c01} \quad (\text{A3.32})$$

The following mathematical relation can be written during mode 1 to mode 3:

$$\hat{i}_{in} = \hat{i}_{S1} + \hat{i}_{S2} = \hat{i}_{pv} - \hat{i}_{cpv} \quad (\text{A3.33})$$

$$\hat{i}_{S1}(t) = \left(\frac{\hat{v}_{pv}(t)}{L_{S1}} \right), \quad (\text{A3.34a})$$

$$\hat{i}_{S2}(t) = \left(\frac{\hat{v}_{pv}(t) - \hat{v}_{c01}}{L_{S2}} \right), \quad (\text{A3.34b})$$

$$\hat{v}_{pv}(t) = - \left(\frac{\hat{v}_{pv}(t)}{C_{pv}R_i} + \frac{(\hat{i}_{S1} + \hat{i}_{S2})}{C_{pv}} \right) \quad (\text{A3.34c})$$

where, negative sign of PV current denotes that load is source and R_i is input source resistance. The averaged large signal model of the system can be defined as follows:

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & \frac{1}{L_{s1}} \\ 0 & 0 & \frac{1}{L_{s2}} \\ \frac{-1}{C_{pv}} & \frac{-1}{C_{pv}} & \frac{-1}{C_{pv}R_i} \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \frac{-(1-D_1)}{L_{s1}} \\ \frac{-(1-D_1)}{L_{s2}} \\ 0 \end{bmatrix}, \quad \mathbf{E} = \begin{bmatrix} \frac{v_{C01}}{L_{s1}} \\ \frac{v_{C01}}{L_{s2}} \\ 0 \end{bmatrix} \quad (\text{A3.35})$$

Acquire the final state-space linearized equation for small signal modelling by applying perturbations to each variable.

$$\begin{aligned} \hat{\mathbf{x}}(t) &= \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}} + E\hat{d}_1 \\ \begin{bmatrix} \hat{i}_{S1} \\ \hat{i}_{S2} \\ \hat{v}_{pv} \end{bmatrix} &= \begin{bmatrix} 0 & 0 & \frac{1}{L_{s1}} \\ 0 & 0 & \frac{1}{L_{s2}} \\ \frac{-1}{C_{pv}} & \frac{-1}{C_{pv}} & \frac{-1}{C_{pv}R_i} \end{bmatrix} \begin{bmatrix} \hat{i}_{S1} \\ \hat{i}_{S2} \\ \hat{v}_{pv} \end{bmatrix} + \begin{bmatrix} \frac{-(1-D_1)}{L_{s1}} & \frac{v_{C01}}{L_{s1}} \\ \frac{-(1-D_1)}{L_{s2}} & \frac{v_{C01}}{L_{s2}} \end{bmatrix} \begin{bmatrix} \hat{v}_{C01} \\ \hat{d}_1 \end{bmatrix} \end{aligned} \quad (A3.36)$$

The transfer function can be written as follows:

$$\frac{\hat{v}_{pv}(s)}{\hat{d}_1(s)} = \frac{-\hat{v}_{c01}}{L_{seq}C_{pv}s^2 + \frac{L_{seq}}{R_i}s + 1} \quad (A3.37)$$

$$\text{where, } L_{seq} = \frac{L_{s1}L_{s2}}{L_{s1} + L_{s2}}$$

The above transfer function is second order system, now, after solving for C_{pv} , it can be written as follows:

$$C_{pv} = \frac{L_{seq}}{4(R_{mpp})^2 \zeta^2} \quad (A3.38)$$

where, $R_i = R_{mpp}$ at the maximum power point and ζ is the damping coefficient.

A.4 State-space Modeling and Small-signal Analysis Under Different Operating States for TMMFT Converter in Non-ideal Conditions

The SSMs analysis of the proposed TMMFT converter under non-ideal operating conditions is carried out in CCM to investigate the dynamic and stability characteristics of the system. Since the operating principles of the TMMFT converter are analogous to those of the FPFTDC converter discussed in Chapter 5, the detailed operating modes and switching characteristics are not repeated here. In this analysis, the effects of parasitic elements and non-idealities are incorporated into the modeling framework.

For *state* I & II operation, the state equations (A4.1) to (A4.10) are common and equations (A4.11) and (A4.12) for *states* I & II, respectively, are given below:

$$V_{Ls1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv} - r_{S1}i_{S1} - V_{SS1}, \text{switch } S_{s1} \text{ is On} \quad (\text{A4.1a})$$

$$V_{Ls1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv} - r_{S1}i_{S1} - V_{DS1} - v_{cp01}, \text{switch } S_{s1} \text{ is Off} \quad (\text{A4.1b})$$

$$V_{Ls2} = L_{S2} \frac{di_{S2}}{dt} = V_{pv} - r_{S2}i_{S2} - V_{SS2}, \text{switch } S_{s2} \text{ is On} \quad (\text{A4.2a})$$

$$V_{Ls2} = L_{S2} \frac{di_{S2}}{dt} = V_{pv} - r_{S2}i_{S2} - V_{DS2} - v_{cp01}, \text{switch } S_{s2} \text{ is Off} \quad (\text{A4.2b})$$

$$v_{cp01} = r_{c01}C_{01} \frac{dv_{c01}}{dt} + v_{c01} \quad (\text{A4.3})$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = v_{cp01} - v_{cp02} - r_{02}i_{L02} - V_{Sb1} - V_{Sb2}, \text{switch } S_{b2} \text{ is On} \quad (\text{A4.4a})$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = -v_{cp02} - r_{02}i_{L02} - V_{Db3}, \text{switch } S_{b2} \text{ is Off} \quad (\text{A4.4b})$$

$$v_{cp02} = r_{c02}C_{02} \frac{dv_{c02}}{dt} + v_{c02} \quad (\text{A4.5})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = v_{cp01} - r_{b1}i_{Lb1} - V_{Sb1} - v_{cfbp}, \text{switch } S_{b1} \text{ is On} \quad (\text{A4.6a})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = -r_{b1}i_{Lb1} - V_{Db2} - V_{Db3} - v_{cfbp}, \text{switch } S_{b1} \text{ is Off} \quad (\text{A4.6b})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = v_{cp01} - r_{b2}i_{Lb2} - V_{Sbb1} - v_{cfbp}, \text{switch } S_{bb1} \text{ is On} \quad (\text{A4.7a})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = -r_{b2}i_{Lb2} - V_{Dbb2} - v_{cfbp}, \text{switch } S_{bb1} \text{ is Off} \quad (\text{A4.7b})$$

$$v_{cfbp} = r_{cfb}C_{fb} \frac{dv_{cfb}}{dt} + v_{cfb} \quad (\text{A4.8})$$

$$i_{c02} = i_{L02} - i_{02} \quad (\text{A4.9})$$

$$i_{cfb} = i_{b1} + i_{b2} - i_{bat} \quad (\text{A4.10})$$

$$\begin{aligned} i_{c01} &= i_{S2} - i_{b1} - i_{01}, \text{ mode } 1, \forall (D_1 - D_3) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b1} - i_{01}, \text{ mode } 2, \forall (D_2 - D_1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{01}, \text{ mode } 3, \forall (1 - 2D_2) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b2} - i_{01}, \text{ mode } 4, \forall (D_2 - D_1) \times T \\ i_{c01} &= i_{S1} - i_{b2} - i_{01}, \text{ mode } 5, \forall (D_1) \times T \\ i_{c01} &= i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 6, \forall (D_3) \times T \end{aligned} \quad \text{For state I} \quad (\text{A4.11})$$

$$\text{where, } i_{01} = \frac{v_{cp01}}{R_{01}}, i_{02} = \frac{v_{cp02}}{R_{02}}, i_{bat} = \frac{v_{cfbp}}{R_{03}}, i_{c01} = C_{01} \frac{dv_{c01}}{dt}$$

$$\begin{aligned}
 i_{c01} &= i_{S2} - i_{b1}, \text{ mode } 1, \forall (D_1 - D_3) \times T \\
 i_{c01} &= i_{S1} + i_{S2} - i_{b1}, \text{ mode } 2, \forall (D_2 - D_1) \times T \\
 i_{c01} &= i_{S1} + i_{S2}, \text{ mode } 3, \forall (1 - 2D_2) \times T \\
 i_{c01} &= i_{S1} + i_{S2} - i_{b2}, \text{ mode } 4, \forall (D_2 - D_1) \times T \\
 i_{c01} &= i_{S1} - i_{b2}, \text{ mode } 5, \forall (D_1) \times T \\
 i_{c01} &= i_{S2} - i_{b1} - i_{L02}, \text{ mode } 6, \forall (D_3) \times T
 \end{aligned}
 \quad \text{For state II}$$

$$\text{where, } i_{01} = \frac{v_{cp01}}{R_{01}}, i_{02} = \frac{v_{cp02}}{R_{02}}, i_{bat} = \frac{v_{cfbp}}{R_{03}}, i_{c01} = C_{01} \frac{dv_{c01}}{dt}$$
(A4.12)

The matrices A_1 - A_6 in (A4.13) represent the state matrices corresponding to state I of the converter.

$$A_1 = \begin{bmatrix}
 \frac{-r_{S1}}{L_{S1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
 0 & \frac{-(r_{S2} + G_1)}{L_{S2}} & \frac{G_1}{L_{S2}} & 0 & 0 & \frac{-G_1}{L_{S2}r_{C01}} & 0 & 0 \\
 0 & \frac{G_1}{L_{b1}} & \frac{-(r_{b1} + G_1 + G_3)}{L_{b1}} & \frac{-G_3}{L_{b1}} & 0 & \frac{G_1}{L_{b1}r_{C01}} & 0 & \frac{-G_3}{L_{b1}r_{Cfb}} \\
 0 & 0 & \frac{-G_3}{L_{b2}} & \frac{-(r_{b2} + G_3)}{L_{b2}} & 0 & 0 & 0 & \frac{-G_3}{L_{b2}r_{Cfb}} \\
 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} & 0 \\
 0 & \frac{G_1}{r_{C01}C_{01}} & \frac{-G_1}{r_{C01}C_{01}} & 0 & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 & 0 \\
 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} & 0 \\
 0 & 0 & \frac{G_3}{r_{Cfb}C_{Cfb}} & \frac{G_3}{r_{Cfb}C_{Cfb}} & 0 & 0 & 0 & \frac{-G_3}{R_{03}r_{Cfb}C_{Cfb}}
 \end{bmatrix}$$

$$A_2 = \begin{bmatrix}
 \frac{-(r_{S1} + G_1)}{L_{S1}} & \frac{-G_1}{L_{S1}} & \frac{G_1}{L_{S1}} & 0 & 0 & \frac{-G_1}{L_{S1}r_{C01}} & 0 & 0 \\
 \frac{-G_1}{L_{S2}} & \frac{-(r_{S2} + G_1)}{L_{S2}} & \frac{G_1}{L_{S2}} & 0 & 0 & \frac{-G_1}{L_{S2}r_{C01}} & 0 & 0 \\
 \frac{G_1}{L_{b1}} & \frac{G_1}{L_{b1}} & \frac{-(r_{b1} + G_1 + G_3)}{L_{b1}} & \frac{-G_3}{L_{b1}} & 0 & \frac{G_1}{L_{b1}r_{C01}} & 0 & \frac{-G_3}{L_{b1}r_{Cfb}} \\
 0 & 0 & \frac{-G_3}{L_{b2}} & \frac{-(r_{b2} + G_3)}{L_{b2}} & 0 & 0 & 0 & \frac{-G_3}{L_{b2}r_{Cfb}} \\
 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} & 0 \\
 \frac{G_1}{r_{C01}C_{01}} & \frac{G_1}{r_{C01}C_{01}} & \frac{-G_1}{r_{C01}C_{01}} & 0 & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 & 0 \\
 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} & 0 \\
 0 & 0 & \frac{G_3}{r_{Cfb}C_{Cfb}} & \frac{G_3}{r_{Cfb}C_{Cfb}} & 0 & 0 & 0 & \frac{-G_3}{R_{03}r_{Cfb}C_{Cfb}}
 \end{bmatrix}$$

$$A_3 = \begin{bmatrix} \frac{-(r_{S1} + G_1)}{L_{S1}} & \frac{-G_1}{L_{S1}} & 0 & 0 & 0 & \frac{-G_1}{L_{S1}r_{C01}} & 0 & 0 \\ \frac{-G_1}{L_{S2}} & \frac{-(r_{S2} + G_1)}{L_{S2}} & 0 & 0 & 0 & \frac{-G_1}{L_{S2}r_{C01}} & 0 & 0 \\ 0 & 0 & \frac{-(r_{b1} + G_3)}{L_{b1}} & \frac{-G_3}{L_{b1}} & 0 & 0 & 0 & \frac{-G_3}{L_{b1}r_{Cfb}} \\ 0 & 0 & \frac{-G_3}{L_{b2}} & \frac{-(r_{b2} + G_3)}{L_{b2}} & 0 & 0 & 0 & \frac{-G_3}{L_{b2}r_{Cfb}} \\ 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} & 0 \\ \frac{G_1}{r_{C01}C_{01}} & \frac{G_1}{r_{C01}C_{01}} & 0 & 0 & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} & 0 \\ 0 & 0 & \frac{G_3}{r_{Cfb}C_{Cfb}} & \frac{G_3}{r_{Cfb}C_{Cfb}} & 0 & 0 & 0 & \frac{-G_3}{R_{03}r_{Cfb}C_{Cfb}} \end{bmatrix}$$

$$A_4 = \begin{bmatrix} \frac{-(r_{S1} + G_1)}{L_{S1}} & \frac{-G_1}{L_{S1}} & 0 & \frac{G_1}{L_{S1}} & 0 & \frac{-G_1}{L_{S1}r_{C01}} & 0 & 0 \\ \frac{-G_1}{L_{S2}} & \frac{-(r_{S2} + G_1)}{L_{S2}} & 0 & \frac{G_1}{L_{S2}} & 0 & \frac{-G_1}{L_{S2}r_{C01}} & 0 & 0 \\ 0 & 0 & \frac{-(r_{b1} + G_3)}{L_{b1}} & \frac{-G_3}{L_{b1}} & 0 & 0 & 0 & \frac{-G_3}{L_{b1}r_{Cfb}} \\ \frac{G_1}{L_{b2}} & \frac{G_1}{L_{b2}} & \frac{-G_3}{L_{b2}} & \frac{-(r_{b2} + G_1 + G_3)}{L_{b2}} & 0 & \frac{G_1}{L_{b2}r_{C01}} & 0 & \frac{-G_3}{L_{b2}r_{Cfb}} \\ 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} & 0 \\ \frac{G_1}{r_{C01}C_{01}} & \frac{G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} & 0 \\ 0 & 0 & \frac{G_3}{r_{Cfb}C_{Cfb}} & \frac{G_3}{r_{Cfb}C_{Cfb}} & 0 & 0 & 0 & \frac{-G_3}{R_{03}r_{Cfb}C_{Cfb}} \end{bmatrix}$$

$$A_5 = \begin{bmatrix} \frac{-(r_{S1} + G_1)}{L_{S1}} & 0 & 0 & \frac{G_1}{L_{S1}} & 0 & \frac{-G_1}{L_{S1}r_{C01}} & 0 & 0 \\ 0 & \frac{-r_{S2}}{L_{S2}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-(r_{b1} + G_3)}{L_{b1}} & \frac{-G_3}{L_{b1}} & 0 & 0 & 0 & \frac{-G_3}{L_{b1}r_{Cfb}} \\ \frac{G_1}{L_{b2}} & 0 & \frac{-G_3}{L_{b2}} & \frac{-(r_{b2} + G_1 + G_3)}{L_{b2}} & 0 & \frac{G_1}{L_{b2}r_{C01}} & 0 & \frac{-G_3}{L_{b2}r_{Cfb}} \\ 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} & 0 \\ \frac{G_1}{r_{C01}C_{01}} & 0 & 0 & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} & 0 \\ 0 & 0 & \frac{G_3}{r_{Cfb}C_{Cfb}} & \frac{G_3}{r_{Cfb}C_{Cfb}} & 0 & 0 & 0 & \frac{-G_3}{R_{03}r_{Cfb}C_{Cfb}} \end{bmatrix}$$

$$A_6 = \begin{bmatrix} \frac{-r_{S1}}{L_{S1}} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{(-r_{S2} + G_1)}{L_{S2}} & \frac{G_1}{L_{S2}} & 0 & \frac{G_1}{L_{S2}} & \frac{-G_1}{L_{S2}r_{C01}} & 0 & 0 \\ 0 & \frac{G_1}{L_{b1}} & \frac{-(r_{b1} + G_1 + G_3)}{L_{b1}} & \frac{-G_3}{L_{b1}} & \frac{-G_1}{L_{b1}} & \frac{G_1}{L_{b1}r_{C01}} & 0 & \frac{-G_3}{L_{b1}r_{Cfb}} \\ 0 & 0 & \frac{-G_3}{L_{b2}} & \frac{-(r_{b2} + G_3)}{L_{b2}} & 0 & 0 & 0 & \frac{-G_3}{L_{b2}r_{Cfb}} \\ 0 & \frac{G_1}{L_{02}} & \frac{-G_1}{L_{02}} & 0 & \frac{-(r_{02} + G_1 + G_2)}{L_{02}} & \frac{G_1}{L_{02}r_{C01}} & \frac{-G_2}{L_{02}r_{C02}} & 0 \\ 0 & \frac{G_1}{r_{C01}C_{01}} & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{r_{C01}C_{01}} & \frac{R_{01}r_{C01}C_{01}}{r_{C01}C_{01}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} & 0 \\ 0 & 0 & \frac{G_3}{r_{Cfb}C_{Cfb}} & \frac{G_3}{r_{Cfb}C_{Cfb}} & 0 & 0 & 0 & \frac{-G_3}{R_{03}r_{Cfb}C_{Cfb}} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ss1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{Sb1}) \\ \frac{1}{L_{b2}}(-V_{Dbb2}) \\ \frac{1}{L_{02}}(-V_{Sb1} - V_{Sb2}) \\ 0 \\ 0 \\ 0 \end{bmatrix}; B_2 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{Sb1}) \\ \frac{1}{L_{b2}}(-V_{Dbb2}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \\ 0 \end{bmatrix}; B_3 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{Db2} - V_{Db3}) \\ \frac{1}{L_{b2}}(-V_{Dbb2}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \\ 0 \end{bmatrix};$$

$$B_4 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{Db2} - V_{Db3}) \\ \frac{1}{L_{b2}}(-V_{Sbb1}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \\ 0 \end{bmatrix}; B_5 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{Db2} - V_{Db3}) \\ \frac{1}{L_{b2}}(-V_{Sbb1}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \\ 0 \end{bmatrix}; B_6 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ss1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{Sb1}) \\ \frac{1}{L_{b2}}(-V_{Dbb2}) \\ \frac{1}{L_{02}}(-V_{Sb1} - V_{Sb2}) \\ 0 \\ 0 \\ 0 \end{bmatrix};$$

$$\left\{ \begin{array}{l} C_1 = \begin{bmatrix} 0 & G_1 & -G_1 & 0 & 0 & \frac{G_1}{r_{C01}} & 0 & 0 \end{bmatrix}; C_2 = \begin{bmatrix} G_1 & G_1 & -G_1 & 0 & 0 & \frac{G_1}{r_{C01}} & 0 & 0 \end{bmatrix}; \\ C_3 = \begin{bmatrix} G_1 & G_1 & 0 & 0 & 0 & \frac{G_1}{r_{C01}} & 0 & 0 \end{bmatrix}; C_4 = \begin{bmatrix} G_1 & G_1 & 0 & -G_1 & 0 & \frac{G_1}{r_{C01}} & 0 & 0 \end{bmatrix}; \\ C_5 = \begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 & \frac{G_1}{r_{C01}} & 0 & 0 \end{bmatrix}; C_6 = \begin{bmatrix} 0 & G_1 & -G_1 & 0 & -G_1 & \frac{G_1}{r_{C01}} & 0 & 0 \end{bmatrix} \end{array} \right\}; \text{for 1}^{st} \text{output variable.}$$

$$\left\{ C_{1-6} = \begin{bmatrix} 0 & 0 & 0 & 0 & G_2 & 0 & \frac{G_2}{r_{c02}} & 0 \end{bmatrix} \right\}; \text{ for } 2^{\text{nd}} \text{ output variable, } \forall \text{ modes.}$$

$$\left\{ C_{1-6} = \begin{bmatrix} 0 & 0 & G_3 & G_3 & 0 & 0 & 0 & \frac{G_3}{r_{cjb}} \end{bmatrix} \right\}; \text{ for } 3^{\text{rd}} \text{ output variable, } \forall \text{ modes.}$$

$$D_{1-6} = [0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0 \ 0];$$

$$\text{where, } G_1 = \frac{R_{01}r_{c01}}{R_{01} + r_{c01}}, G_2 = \frac{R_{02}r_{c02}}{R_{02} + r_{c02}}, G_3 = \frac{R_{03}r_{cjb}}{R_{03} + r_{cjb}} \quad (\text{A4.13})$$

State Variables and Input Vectors for state-I:

(i). State vector: $\hat{x}_1(t) = [\hat{i}_{Ls1} \ \hat{i}_{Ls1} \ \hat{i}_{Lb1} \ \hat{i}_{Lb2} \ \hat{i}_{L02} \ \hat{v}_{c01} \ \hat{v}_{c02} \ \hat{v}_{bat}]^T$

(ii). Input vector: $\hat{u}_1(t) = \hat{v}_{pv}$

Small-signal models for this state.

$$A_{|S-I} = \begin{bmatrix} A_{11} & \frac{-(1-2D_1)G_1}{L_{S1}} & \frac{(D_2-D_1)G_1}{L_{S1}} & \frac{D_2G_1}{L_{S1}} & 0 & A_{16} & 0 & 0 \\ \frac{-(1-2D_1)G_1}{L_{S2}} & A_{22} & \frac{D_2G_1}{L_{S2}} & \frac{(D_2-D_1)G_1}{L_{S2}} & \frac{D_3G_1}{L_{S2}} & A_{26} & 0 & 0 \\ \frac{(D_2-D_1)G_1}{L_{b1}} & \frac{D_2G_1}{L_{b1}} & A_{33} & \frac{-G_3}{L_{b1}} & \frac{D_3G_1}{L_{b1}} & A_{36} & 0 & \frac{-G_3}{L_{b1}r_{cjb}} \\ \frac{D_2G_1}{L_{b2}} & \frac{(D_2-D_1)G_1}{L_{b2}} & \frac{-G_3}{L_{b2}} & A_{44} & 0 & A_{46} & 0 & \frac{-G_3}{L_{b2}r_{cjb}} \\ 0 & \frac{D_3G_1}{L_{02}} & \frac{-D_3G_1}{L_{02}} & 0 & A_{55} & A_{56} & A_{57} & 0 \\ A_{61} & A_{62} & A_{63} & A_{64} & A_{65} & A_{66} & 0 & 0 \\ 0 & 0 & 0 & 0 & A_{75} & 0 & A_{77} & 0 \\ 0 & 0 & \frac{G_3}{r_{cjb}C_{cjb}} & \frac{G_3}{r_{cjb}C_{cjb}} & 0 & 0 & 0 & A_{88} \end{bmatrix};$$

$$B_{|S-I} = \begin{bmatrix} \frac{1}{L_{S1}} \frac{-D_1}{L_{S1}} & 0 & 0 & 0 & 0 & \frac{-(1-D_1)}{L_{S1}} & 0 & 0 & 0 & 0 \\ \frac{1}{L_{S2}} & 0 & \frac{-D_1}{L_{S2}} & 0 & 0 & 0 & \frac{-(1-D_1)}{L_{S2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-D_2}{L_{b1}} & 0 & 0 & 0 & \frac{-(1-D_2)}{L_{b1}} & \frac{-(1-D_2)}{L_{b1}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-D_2}{L_{b2}} & 0 & 0 & 0 & 0 & \frac{-(1-D_2)}{L_{b2}} \\ 0 & 0 & 0 & \frac{-D_3}{L_{02}} & \frac{-D_3}{L_{02}} & 0 & 0 & 0 & \frac{-(1-D_3)}{L_{02}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$E_{1|S-I} = \begin{bmatrix} E_{11} \\ E_{21} \\ \frac{1}{L_{b1}}(-I_{LS1}G_1) \\ \frac{1}{L_{b2}}(-I_{LS2}G_1) \\ 0 \\ E_{61S} \\ 0 \\ 0 \end{bmatrix}; E_{2|S-I} = \begin{bmatrix} \frac{G_1}{L_{S1}}(I_{Lb1} + I_{Lb2}) \\ \frac{-G_1}{L_{S2}}(I_{Lb1} + I_{Lb2}) \\ E_{31} \\ E_{41} \\ 0 \\ E_{61b} \\ 0 \\ 0 \end{bmatrix}; E_{3|S-I} = \begin{bmatrix} 0 \\ \frac{1}{L_{S2}}(-I_{L02}G_1) \\ \frac{1}{L_{b1}}(-I_{L02}G_1) \\ 0 \\ E_{51} \\ E_{61a} \\ 0 \\ 0 \end{bmatrix};$$

$$C_{1-avg,|S-I} = [C_{11} \ C_{12} \ C_{13} \ C_{14} \ C_{15} \ C_{16} \ 0 \ 0]; C_{2-avg,|S-I} = \begin{bmatrix} 0 & 0 & 0 & 0 & G_2 & 0 & \frac{G_2}{r_{C02}} & 0 \end{bmatrix}; C_{15} = -D_3G_1;$$

$$C_{3-avg,|S-I} = \begin{bmatrix} 0 & 0 & G_3 & G_3 & 0 & 0 & 0 & \frac{G_3}{r_{C7b}} \end{bmatrix}; C_{11} = C_{12} = (1-D_1)G_1; C_{13} = C_{14} = -D_2G_1; C_{16} = \frac{G_1}{r_{C01}};$$

$$A_{11} = \frac{-(r_{S1} + (1-D_1)G_1)}{L_{S1}}; A_{22} = \frac{-(r_{S2} + (1-D_1)G_1)}{L_{S2}}; A_{33} = \frac{-(r_{b1} + D_2G_1 + G_3)}{L_{b1}}; A_{56} = \frac{D_3G_1}{L_{02}r_{C01}};$$

$$A_{44} = \frac{-(r_{b2} + D_2G_1 + G_3)}{L_{b2}}; A_{55} = \frac{-(r_{02} + D_3G_1 + G_2)}{L_{02}}; A_{66} = \frac{-G_1}{R_{01}r_{C01}C_{01}}; A_{77} = \frac{-G_2}{R_{02}r_{C02}C_{02}};$$

$$\begin{aligned}
\text{where, } A_{16} &= \frac{-(1-D_1)G_1}{L_{S1}r_{C01}}; A_{26} = \frac{-(1-D_1)G_1}{L_{S2}r_{C01}}; A_{36} = \frac{D_2G_1}{L_{b1}r_{C01}}; A_{46} = \frac{D_2G_1}{L_{b2}r_{C01}}; \\
A_{61} &= A_{62} = \frac{(1-D_1)G_1}{r_{C01}C_{01}}; A_{63} = A_{64} = \frac{-D_2G_1}{r_{C01}C_{01}}; A_{65} = \frac{-D_3G_1}{r_{C01}C_{01}}; A_{75} = \frac{G_2}{r_{C02}C_{02}}; A_{88} = \frac{-G_3}{R_{03}r_{Cfb}C_{fb}}; \\
A_{57} &= \frac{-G_2}{L_{02}r_{C02}}; E_{11} = \frac{1}{L_{S1}} \left(\left(I_{LS1}G_1 + 2I_{LS2}G_1 - I_{Lb1}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) + (V_{Ds1} - V_{Ss1}) \right); \\
E_{21} &= \frac{1}{L_{S2}} \left(\left(2I_{LS1}G_1 + I_{LS2}G_1 - I_{Lb2}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) + (V_{Ds2} - V_{Ss2}) \right); E_{61S} = \frac{-G_1}{r_{C01}C_{01}} (I_{LS1} + I_{LS2}); \\
E_{61b} &= \frac{-G_1}{r_{C01}C_{01}} (I_{Lb1} + I_{Lb2}); E_{31} = \frac{1}{L_{b1}} \left(\left(I_{LS1}G_1 + I_{LS2}G_1 - I_{Lb1}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) + (V_{Db2} + V_{Db3}) - V_{Sb1} \right); \\
E_{61a} &= \frac{-G_1}{r_{C01}C_{01}} (I_{L02}); E_{41} = \frac{1}{L_{b2}} \left(\left(I_{LS1}G_1 + I_{LS2}G_1 - I_{Lb1}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) + (V_{Dbb2} - V_{Sbb1}) \right); \\
E_{51} &= \frac{1}{L_{02}} \left(\left(I_{LS2}G_1 - I_{Lb1}G_1 - I_{L02}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Sb1} + V_{Sb2}) + V_{Db3} \right); \\
F_{1|S-I} &= [- (I_{LS1}G_1 + I_{LS2}G_1)]; F_{2|S-I} = [- (I_{Lb1}G_1 + I_{Lb2}G_1)]; F_{3|S-I} = [- (I_{L02}G_1)];
\end{aligned}
\tag{A4.14}$$

In matrices A_1 - A_6 in (A4.13) and (A4.14), putting R_{01} to infinity represents the state matrices corresponding to *state II* of the converter.

For *state III* operation, the state equations are given below:

$$V_{LS1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv} - r_{S1}i_{S1} - V_{SS1}, \text{ switch } S_{S1} \text{ is On} \tag{A4.15a}$$

$$V_{LS1} = L_{S1} \frac{di_{S1}}{dt} = V_{pv} - r_{S1}i_{S1} - V_{DS1} - v_{cp01}, \text{ switch } S_{S1} \text{ is Off} \tag{A4.15b}$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = v_{cp01} - v_{cp02} - r_{02}i_{L02} + V_{Db1} - V_{Sb2}, \text{ switch } S_{b2} \text{ is On} \tag{A4.16a}$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = -v_{c02}, \text{ switch } S_{b2} \text{ is Off} \tag{A4.16b}$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = v_{cp01} - v_{bat} - r_{b1}i_{Lb1} + V_{Db1}, \text{ switch } S_{b2}, S_{b3} \text{ is On} \tag{A4.17a}$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = -v_{bat} - r_{b1}i_{Lb1} + V_{Sb2} + V_{Sb3}, \text{ switch } S_{b3} \text{ is Off} \tag{A4.17b}$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = -v_{bat} - r_{b2}i_{Lb2} + V_{Sbb2}, \text{ switch } S_{bb2} \text{ is On} \tag{A4.18a}$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = v_{cp01} - v_{bat} - r_{b2}i_{Lb2} + V_{Dbb1}, \text{ switch } S_{bb2} \text{ is Off} \quad (\text{A4.18b})$$

$$\begin{aligned} i_{c01} &= i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 1, \forall (D_1 + D_3 - 1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b1} - i_{L02} - i_{01}, \text{ mode } 2, \forall (1 - D_2 - D_1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{01}, \text{ mode } 3, \forall (2D_2 - 1) \times T \\ i_{c01} &= i_{S1} + i_{S2} - i_{b2} - i_{01}, \text{ mode } 4, \forall (1 - D_2 - D_1) \times T \\ i_{c01} &= i_{S1} - i_{b2} - i_{01}, \text{ mode } 5, \forall (D_1) \times T \\ i_{c01} &= i_{S2} - i_{b1} - i_{01}, \text{ mode } 6, \forall (1 - D_3) \times T \end{aligned} \quad (\text{A4.19})$$

The matrices A_1 - A_6 in (A4.20) represent the state matrices corresponding to *state* III of the converter.

$$A_1 = \begin{bmatrix} \frac{-r_{S1}}{L_{S1}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-(r_{S2} + G_1)}{L_{S2}} & \frac{G_1}{L_{S2}} & 0 & \frac{G_1}{L_{S2}} & \frac{-G_1}{L_{S2}r_{C01}} & 0 \\ 0 & \frac{G_1}{L_{b1}} & \frac{-(r_{b1} + G_1)}{L_{b1}} & 0 & \frac{-G_1}{L_{b1}} & \frac{G_1}{L_{b1}r_{C01}} & 0 \\ 0 & 0 & 0 & \frac{-r_{b2}}{L_{b2}} & 0 & 0 & 0 \\ 0 & \frac{G_1}{L_{02}} & \frac{-G_1}{L_{02}} & 0 & \frac{-(r_{02} + G_2 + G_1)}{L_{02}} & \frac{G_1}{L_{02}r_{C01}} & \frac{-G_2}{L_{02}r_{C02}} \\ 0 & \frac{G_1}{r_{C01}C_{01}} & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{r_{C01}C_{01}} & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} \frac{-(r_{S1} + G_1)}{L_{S1}} & \frac{-G_1}{L_{S1}} & \frac{G_1}{L_{S1}} & 0 & \frac{G_1}{L_{S1}} & \frac{-G_1}{L_{S1}r_{C01}} & 0 \\ \frac{-G_1}{L_{S2}} & \frac{-(r_{S2} + G_1)}{L_{S2}} & \frac{G_1}{L_{S2}} & 0 & \frac{G_1}{L_{S1}} & \frac{-G_1}{L_{S2}r_{C01}} & 0 \\ \frac{G_1}{L_{b1}} & \frac{G_1}{L_{b1}} & \frac{-(r_{b1} + G_1)}{L_{b1}} & 0 & \frac{G_1}{L_{b1}} & \frac{G_1}{L_{b1}r_{C01}} & 0 \\ 0 & 0 & 0 & \frac{-r_{b2}}{L_{b2}} & 0 & 0 & 0 \\ \frac{G_1}{L_{02}} & \frac{G_1}{L_{02}} & \frac{-G_1}{L_{02}} & 0 & \frac{-(r_{02} + G_2 + G_1)}{L_{02}} & \frac{G_1}{L_{02}r_{C01}} & \frac{-G_2}{L_{02}r_{C02}} \\ \frac{G_1}{r_{C01}C_{01}} & \frac{G_1}{r_{C01}C_{01}} & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{r_{C01}C_{01}} & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} \frac{-(r_{S1} + G_1)}{L_{S1}} & \frac{-G_1}{L_{S1}} & 0 & 0 & 0 & \frac{-G_1}{L_{S1}r_{C01}} & 0 \\ \frac{-G_1}{L_{S2}} & \frac{-(r_{S2} + G_1)}{L_{S2}} & 0 & 0 & 0 & \frac{-G_1}{L_{S2}r_{C01}} & 0 \\ 0 & 0 & \frac{-r_{b1}}{L_{b1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-r_{b2}}{L_{b2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} \\ \frac{G_1}{r_{C01}C_{01}} & \frac{G_1}{r_{C01}C_{01}} & 0 & 0 & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$A_4 = \begin{bmatrix} \frac{-(r_{S1} + G_1)}{L_{S1}} & \frac{-G_1}{L_{S1}} & 0 & \frac{G_1}{L_{S1}} & 0 & \frac{-G_1}{L_{S1}r_{C01}} & 0 \\ \frac{-G_1}{L_{S2}} & \frac{-(r_{S2} + G_1)}{L_{S2}} & 0 & \frac{G_1}{L_{S2}} & 0 & \frac{-G_1}{L_{S2}r_{C01}} & 0 \\ 0 & 0 & \frac{-r_{b1}}{L_{b1}} & 0 & 0 & 0 & 0 \\ \frac{G_1}{L_{b2}} & \frac{G_1}{L_{b2}} & 0 & \frac{-(r_{b2} + G_1)}{L_{b2}} & 0 & \frac{G_1}{L_{b2}r_{C01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} \\ \frac{G_1}{r_{C01}C_{01}} & \frac{G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$A_5 = \begin{bmatrix} \frac{-(r_{S1} + G_1)}{L_{S1}} & 0 & 0 & \frac{G_1}{L_{S1}} & 0 & \frac{-G_1}{L_{S1}r_{C01}} & 0 \\ 0 & \frac{-r_{S2}}{L_{S2}} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-r_{b1}}{L_{b1}} & 0 & 0 & 0 & 0 \\ \frac{G_1}{L_{b2}} & 0 & 0 & \frac{-(r_{b2} + G_1)}{L_{b2}} & 0 & \frac{G_1}{L_{b2}r_{C01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} \\ \frac{G_1}{r_{C01}C_{01}} & 0 & 0 & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$\begin{aligned}
 A_6 = & \begin{bmatrix} \frac{-r_{S1}}{L_{S1}} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{(-r_{S2} + G_1)}{L_{S2}} & \frac{G_1}{L_{S2}} & 0 & 0 & \frac{-G_1}{L_{S2}r_{C01}} & 0 \\ 0 & \frac{G_1}{L_{b1}} & \frac{-(r_{b1} + G_1)}{L_{b1}} & 0 & 0 & \frac{G_1}{L_{b1}r_{C01}} & 0 \\ 0 & 0 & 0 & \frac{-r_{b2}}{L_{b2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} \\ 0 & \frac{G_1}{r_{C01}C_{01}} & \frac{-G_1}{r_{C01}C_{01}} & 0 & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix} \\
 B_1 = & \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{bat} + V_{Db1}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Sbb2}) \\ \frac{1}{L_{02}}(V_{Sb2} - V_{Db1}) \\ 0 \\ 0 \end{bmatrix}; B_2 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{bat} + V_{Db1}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Sbb2}) \\ \frac{1}{L_{02}}(V_{Sb2} - V_{Db1}) \\ 0 \\ 0 \end{bmatrix}; \\
 B_3 = & \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{bat} + V_{Sb2} + V_{Sb3}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Sbb2}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \end{bmatrix}; B_4 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{bat} + V_{Sb2} + V_{Sb3}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Dbb1}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \end{bmatrix}; \\
 B_5 = & \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{bat} + V_{Sb2} + V_{Sb3}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Dbb1}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \end{bmatrix}; B_6 = \begin{bmatrix} \frac{1}{L_{S1}}(V_{pv} - V_{Ds1}) \\ \frac{1}{L_{S2}}(V_{pv} - V_{Ds2}) \\ \frac{1}{L_{b1}}(-V_{bat} + V_{Db1}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Sbb2}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \end{bmatrix}; \\
 C_1 = & \begin{bmatrix} 0 & G_1 & -G_1 & 0 & -G_1 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; C_2 = \begin{bmatrix} G_1 & G_1 & -G_1 & 0 & -G_1 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; \\
 C_3 = & \begin{bmatrix} G_1 & G_1 & 0 & 0 & 0 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; C_4 = \begin{bmatrix} G_1 & G_1 & 0 & -G_1 & 0 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; \\
 C_5 = & \begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; C_6 = \begin{bmatrix} 0 & G_1 & -G_1 & 0 & 0 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix} \\
 & \text{for 1st output variable.} \\
 C_{1-6} = & \begin{bmatrix} 0 & 0 & 0 & 0 & G_2 & 0 & \frac{G_2}{r_{C02}} \end{bmatrix} \\
 & \text{for 2nd output variable, } \forall \text{ modes.} \\
 D_{1-6} = & \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix};
 \end{aligned}
 \tag{A4.20}$$

State Variables and Input Vectors for *state-III*:

(i). State vector: $\hat{x}_3(t) = [\hat{i}_{Ls1} \ \hat{i}_{Ls1} \ \hat{i}_{Lb1} \ \hat{i}_{Lb2} \ \hat{i}_{L02} \ \hat{v}_{c01} \ \hat{v}_{c02}]^T$

(ii). Input vector: $\hat{u}_3(t) = [\hat{v}_{pv} \ \hat{v}_{bat}]$.

Small-signal models for this state.

$$A_{|S-III} = \begin{bmatrix} A_{11} & \frac{-(1-2D_1)G_1}{L_{S1}} & A_{13|S-III} & \frac{(1-D_2)G_1}{L_{S1}} & A_{15|S-III} & A_{16} & 0 \\ \frac{-(1-2D_1)G_1}{L_{S2}} & A_{22} & \frac{(1-D_2)G_1}{L_{S2}} & A_{24|S-III} & \frac{(D_3-D_2)G_1}{L_{S2}} & A_{26} & 0 \\ A_{31|S-III} & \frac{(1-D_2)G_1}{L_{b1}} & A_{33|S-III} & 0 & \frac{-(D_3-D_2)G_1}{L_{b1}} & A_{36|S-III} & 0 \\ \frac{(1-D_2)G_1}{L_{b2}} & A_{42|S-III} & 0 & A_{44|S-III} & 0 & A_{46|S-III} & 0 \\ A_{51|S-III} & A_{52|S-III} & A_{53|S-III} & 0 & A_{55|S-III} & A_{56|S-III} & A_{57} \\ A_{61} & A_{62} & A_{63|S-III} & A_{64|S-III} & A_{65|S-III} & A_{66} & 0 \\ 0 & 0 & 0 & 0 & A_{75} & 0 & A_{77} \end{bmatrix};$$

$$B_{|S-III} = \begin{bmatrix} \frac{1}{L_{S1}} & 0 & \frac{-D_1}{L_{S1}} & 0 & 0 & 0 & 0 & \frac{-(1-D_1)}{L_{S1}} & 0 & 0 & 0 & 0 \\ \frac{1}{L_{S2}} & 0 & 0 & \frac{-D_1}{L_{S2}} & 0 & 0 & 0 & 0 & \frac{-(1-D_1)}{L_{S2}} & 0 & 0 & 0 \\ 0 & \frac{-1}{L_{b1}} & 0 & 0 & \frac{D_2}{L_{b1}} & \frac{D_2}{L_{b1}} & 0 & 0 & 0 & \frac{(1-D_2)}{L_{b1}} & 0 & 0 \\ 0 & \frac{-1}{L_{b2}} & 0 & 0 & 0 & 0 & \frac{D_2}{L_{b2}} & 0 & 0 & 0 & 0 & \frac{(1-D_2)}{L_{b2}} \\ 0 & 0 & 0 & 0 & \frac{-(D_3-D_2)}{L_{02}} & 0 & 0 & 0 & 0 & \frac{(D_3-D_2)}{L_{02}} & \frac{-(1-D_3-D_2)}{L_{02}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

where, $A_{33|S-III} = \frac{-(r_{b1} + (1-D_2)G_1)}{L_{b1}}$; $A_{44|S-III} = \frac{-(r_{b2} + (1-D_2)G_1)}{L_{b2}}$; $A_{36|S-III} = \frac{(1-D_2)G_1}{L_{b1}r_{C01}}$;

$A_{55|S-III} = \frac{-(r_{02} + (D_3-D_2)G_1 + G_2)}{L_{02}}$; $A_{46|S-III} = \frac{(1-D_2)G_1}{L_{b2}r_{C01}}$; $A_{56|S-III} = \frac{(D_3-D_2)G_1}{L_{02}r_{C01}}$;

$A_{63|S-III} = A_{64|S-III} = \frac{-(1-D_2)G_1}{r_{C01}C_{01}}$; $A_{65|S-III} = \frac{-(D_3-D_2)G_1}{r_{C01}C_{01}}$; $A_{13|S-III} = A_{15|S-III} = \frac{(1-D_2-D_1)G_1}{L_{S1}}$;

$A_{24|S-III} = \frac{(1-D_2-D_1)G_1}{L_{S2}}$; $A_{31|S-III} = \frac{(1-D_2-D_1)G_1}{L_{b1}}$; $A_{42|S-III} = \frac{(1-D_2-D_1)G_1}{L_{b2}}$;

$A_{51|S-III} = \frac{(1-D_2-D_1)G_1}{L_{02}}$; $A_{53|S-III} = -A_{52|S-III} = \frac{(D_3-D_2)G_1}{L_{02}}$; $F_{1|S-III} = F_{1|S-I}$;

$$\begin{aligned}
 E_{1|S-III} &= \begin{bmatrix} E_{11} \\ E_{21} \\ \frac{1}{L_{b1}}(-I_{LS1}G_1) \\ \frac{1}{L_{b2}}(-I_{LS2}G_1) \\ \frac{1}{L_{02}}(-I_{LS1}G_1) \\ E_{61S} \\ 0 \end{bmatrix}; E_{2|S-III} = \begin{bmatrix} \frac{-G_1}{L_{S1}}(I_{Lb1} + I_{Lb2} + I_{L02}) \\ \frac{-G_1}{L_{S2}}(I_{Lb1} + I_{Lb2} + I_{L02}) \\ E_{31|S-III} \\ E_{41|S-III} \\ E_{51a|S-III} \\ -(E_{61b} + E_{61a}) \\ 0 \end{bmatrix}; E_{3|S-III} = \begin{bmatrix} 0 \\ \frac{1}{L_{S2}}(I_{L02}G_1) \\ \frac{1}{L_{b1}}(-I_{L02}G_1) \\ 0 \\ E_{51b|S-III} \\ E_{61a} \\ 0 \end{bmatrix}; \\
 E_{31|S-III} &= \frac{1}{L_{b1}} \left(\left(-I_{LS1}G_1 - I_{LS2}G_1 + I_{Lb1}G_1 + I_{L02}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - V_{Db1} + (V_{Sb2} + V_{Sb3}) \right); \\
 E_{41|S-III} &= \frac{1}{L_{b2}} \left(\left(-I_{LS1}G_1 - I_{LS2}G_1 + I_{Lb2}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Dbb1} - V_{Sbb2}) \right); F_{2|S-III} = -(F_{2|S-I} + F_{3|S-I}); \\
 E_{51a|S-III} &= \frac{1}{L_{02}} \left(\left(-I_{LS1}G_1 - I_{LS2}G_1 + I_{Lb1}G_1 + I_{L02}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Db3} + (V_{Db1} - V_{Sb2})) \right); \\
 E_{51b|S-III} &= \frac{1}{L_{02}} \left(\left(I_{LS2}G_1 - I_{Lb1}G_1 - I_{L02}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) + (V_{Db3} + (V_{Db1} - V_{Sb2})) \right); F_{3|S-III} = F_{3|S-I}; \\
 E_{61b} &= \frac{-G_1}{r_{C01}C_{01}}(I_{Lb1} + I_{Lb2}); E_{31} = \frac{1}{L_{b1}} \left(\left(I_{LS1}G_1 + I_{LS2}G_1 - I_{Lb1}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) + (V_{Db2} + V_{Db3}) - V_{Sb1} \right); \\
 E_{61a} &= \frac{-G_1}{r_{C01}C_{01}}(I_{L02}); E_{41} = \frac{1}{L_{b2}} \left(\left(I_{LS1}G_1 + I_{LS2}G_1 - I_{Lb1}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) + (V_{Dbb2} - V_{Sbb1}) \right); \\
 E_{51} &= \frac{1}{L_{02}} \left(\left(I_{LS2}G_1 - I_{Lb1}G_1 - I_{L02}G_1 + \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Sb1} + V_{Sb2}) + V_{Db3} \right); \\
 F_{1|S-I} &= [- (I_{LS1}G_1 + I_{LS2}G_1)]; F_{2|S-I} = [- (I_{Lb1}G_1 + I_{Lb2}G_1)]; F_{3|S-I} = [- (I_{L02}G_1)]; \\
 C_{1-avg|S-III} &= [C_{11} \ C_{12} \ C_{13|S-III} \ C_{14|S-III} \ C_{15|S-III} \ C_{16} \ 0]; \\
 C_{2-avg|S-III} &= \begin{bmatrix} 0 & 0 & 0 & 0 & G_2 & 0 & \frac{G_2}{r_{C02}} \end{bmatrix}; \\
 C_{15|S-III} &= -(D_3 - D_2)G_1; C_{15|S-III} = -(D_3 - D_2)G_1; \\
 C_{13|S-III} &= C_{14|S-III} = -(1 - D_2)G_1;
 \end{aligned}$$

(A4.21)

For *state IV* operation, the state equations are given below:

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = v_{cp01} - v_{cp02} - r_{02}i_{L02} + V_{Db1} - V_{Sb2}, \text{ switch } S_{b2} \text{ is On} \quad (A4.22a)$$

$$V_{L02} = L_{02} \frac{di_{L02}}{dt} = -v_{c02}, \text{switch } S_{b2} \text{ is Off} \quad (\text{A4.22b})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = v_{cp01} - v_{bat} - r_{b1}i_{Lb1} + V_{Db1}, \text{switch } S_{b2}, S_{b3} \text{ is On} \quad (\text{A4.23a})$$

$$V_{Lb1} = L_{b1} \frac{di_{Lb1}}{dt} = -v_{bat} - r_{b1}i_{Lb1} + V_{Sb2} + V_{Sb3}, \text{switch } S_{b3} \text{ is Off} \quad (\text{A4.23b})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = -v_{bat} - r_{b2}i_{Lb2} + V_{Sbb2}, \text{switch } S_{bb2} \text{ is On} \quad (\text{A4.24a})$$

$$V_{Lb2} = L_{b2} \frac{di_{Lb2}}{dt} = v_{cp01} - v_{bat} - r_{b2}i_{Lb2} + V_{Dbb1}, \text{switch } S_{bb2} \text{ is Off} \quad (\text{A4.24b})$$

$$\begin{aligned} i_{c01} &= -i_{b1} - i_{L02} - i_{01}, \text{ mode } 1, \forall (D_3 - D_2) \times T \\ i_{c01} &= -i_{01}, \text{ mode } 2, \forall (2D_2 - 1) \times T \\ i_{c01} &= -i_{b2} - i_{01}, \text{ mode } 3, \forall (1 - D_2) \times T \\ i_{c01} &= -i_{b1} - i_{01}, \text{ mode } 4, \forall (1 - D_3) \times T \end{aligned} \quad (\text{A4.25})$$

The matrices A_1 - A_4 in (A4.26) represent the state matrices corresponding to *state IV* of the converter.

$$A_1 = \begin{bmatrix} \frac{-(r_{b1} + G_1)}{L_{b1}} & 0 & \frac{-G_1}{L_{b1}} & \frac{G_1}{L_{b1}r_{C01}} & 0 \\ 0 & \frac{-r_{b2}}{L_{b2}} & 0 & 0 & 0 \\ \frac{-G_1}{L_{02}} & 0 & \frac{-(r_{02} + G_2 + G_1)}{L_{02}} & \frac{G_1}{L_{02}r_{C01}} & \frac{-G_2}{L_{02}r_{C02}} \\ \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{r_{C01}C_{01}} & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$A_2 = \begin{bmatrix} \frac{-r_{b1}}{L_{b1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-r_{b2}}{L_{b2}} & 0 & 0 & 0 \\ 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} \\ 0 & 0 & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} \frac{-r_{b1}}{L_{b1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-(r_{b2} + G_2)}{L_{b2}} & 0 & \frac{G_1}{L_{b2}r_{C01}} & 0 \\ 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} \\ 0 & \frac{-G_1}{r_{C01}C_{01}} & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$A_4 = \begin{bmatrix} \frac{-(r_{b1} + G_1)}{L_{b1}} & 0 & 0 & \frac{G_1}{L_{b1}r_{C01}} & 0 \\ 0 & \frac{-r_{b2}}{L_{b2}} & 0 & 0 & 0 \\ 0 & 0 & \frac{-(r_{02} + G_2)}{L_{02}} & 0 & \frac{-G_2}{L_{02}r_{C02}} \\ \frac{-G_1}{r_{C01}C_{01}} & 0 & 0 & \frac{-G_1}{R_{01}r_{C01}C_{01}} & 0 \\ 0 & 0 & \frac{G_2}{r_{C02}C_{02}} & 0 & \frac{-G_2}{R_{02}r_{C02}C_{02}} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L_{b1}}(-V_{bat} + V_{Db1}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Sbb2}) \\ \frac{1}{L_{02}}(V_{Sb2} - V_{Db1}) \\ 0 \\ 0 \end{bmatrix}; B_2 = \begin{bmatrix} \frac{1}{L_{b1}}(-V_{bat} + V_{Sb2} + V_{Sb3}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Sbb2}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \end{bmatrix}; B_3 = \begin{bmatrix} \frac{1}{L_{b1}}(-V_{bat} + V_{Sb2} + V_{Sb3}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Dbb1}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \end{bmatrix}; B_4 = \begin{bmatrix} \frac{1}{L_{b1}}(-V_{bat} + V_{Db1}) \\ \frac{1}{L_{b2}}(-V_{bat} + V_{Sbb2}) \\ \frac{1}{L_{02}}(-V_{Db3}) \\ 0 \\ 0 \end{bmatrix};$$

$$E_2 = \begin{bmatrix} \frac{1}{L_{b1}} \left(\left(I_{Lb1}G_1 + I_{L02}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - V_{Db1} + (V_{Sb2} + V_{Sb3}) \right) \\ \frac{1}{L_{b2}} \left(\left(I_{Lb2}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Dbb1} - V_{Sbb2}) \right) \\ \frac{1}{L_{02}} \left(\left(I_{Lb1}G_1 + I_{L02}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Db3} + (V_{Db1} - V_{Sb2})) \right) \\ \frac{G_1}{r_{C01}C_{01}}(I_{Lb1} + I_{Lb2} + I_{L02}) \\ 0 \end{bmatrix} \quad E_2 = \begin{bmatrix} \frac{1}{L_{b1}} \left(\left(I_{Lb1}G_1 + I_{L02}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - V_{Db1} + (V_{Sb2} + V_{Sb3}) \right) \\ \frac{1}{L_{b2}} \left(\left(I_{Lb2}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Dbb1} - V_{Sbb2}) \right) \\ \frac{1}{L_{02}} \left(\left(I_{Lb1}G_1 + I_{L02}G_1 - \left(\frac{V_{01}G_1}{r_{C01}} \right) \right) - (V_{Db3} + (V_{Db1} - V_{Sb2})) \right) \\ \frac{G_1}{r_{C01}C_{01}}(I_{Lb1} + I_{Lb2} + I_{L02}) \\ 0 \end{bmatrix}$$

$$\begin{aligned}
 & \left\{ \begin{aligned} C_1 &= \begin{bmatrix} -G_1 & 0 & -G_1 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; C_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; \\ C_3 &= \begin{bmatrix} 0 & -G_1 & 0 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; C_4 = \begin{bmatrix} -G_1 & 0 & 0 & \frac{G_1}{r_{C01}} & 0 \end{bmatrix}; \\ & \text{for } 1^{\text{st}} \text{ output variable.} \end{aligned} \right\}; \\
 & \left\{ \begin{aligned} C_{1-4} &= \begin{bmatrix} 0 & 0 & G_2 & 0 & \frac{G_2}{r_{C02}} \end{bmatrix} \\ & \text{for } 2^{\text{nd}} \text{ output variable, } \forall \text{ modes.} \end{aligned} \right\}; \\
 & D_{1-4} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix};
 \end{aligned}
 \quad
 \begin{aligned}
 F_2 &= \begin{bmatrix} (I_{b1}G_1 + I_{b2}G_1 + I_{L02}G_1) \end{bmatrix}; F_3 = \begin{bmatrix} -(I_{L02}G_1) \end{bmatrix};
 \end{aligned}
 \tag{A4.26}$$

State Variables and Input Vectors for state-IV:

- (i). State vector: $\hat{x}_4(t) = \begin{bmatrix} \hat{i}_{Lb1} & \hat{i}_{Lb2} & \hat{i}_{L02} & \hat{v}_{c01} & \hat{v}_{c02} \end{bmatrix}^T$
- (ii). Input vector: $\hat{u}_4(t) = \begin{bmatrix} \hat{v}_{bat} \end{bmatrix}$.

Small-signal models for this state.

$$\begin{aligned}
 A_{|S-IV} &= \begin{bmatrix} A_{33|S-III} & 0 & \frac{-(D_3 - D_2)G_1}{L_{b1}} & A_{36|S-III} & 0 \\ 0 & A_{44|S-III} & 0 & A_{46|S-III} & 0 \\ -A_{53|S-III} & 0 & A_{55|S-III} & A_{56|S-III} & A_{57} \\ A_{63|S-III} & A_{64|S-III} & A_{65|S-III} & A_{66} & 0 \\ 0 & 0 & A_{75} & 0 & A_{77} \end{bmatrix}; \\
 B_{|S-IV} &= \begin{bmatrix} \frac{-1}{L_{b1}} & \frac{D_2}{L_{b1}} & \frac{D_2}{L_{b1}} & 0 & \frac{(1-D_2)}{L_{b1}} & 0 & 0 \\ \frac{-1}{L_{b2}} & 0 & 0 & \frac{D_2}{L_{b2}} & 0 & 0 & \frac{(1-D_2)}{L_{b2}} \\ 0 & \frac{-(D_3 - D_2)}{L_{02}} & 0 & 0 & \frac{(D_3 - D_2)}{L_{02}} & \frac{-(1-D_3 - D_2)}{L_{02}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \\
 C_{1-avg,|S-IV} &= \begin{bmatrix} C_{13|S-III} & C_{14|S-III} & C_{15|S-III} & C_{16} & 0 \end{bmatrix}; C_{2-avg,|S-III} = \begin{bmatrix} 0 & 0 & G_2 & 0 & \frac{G_2}{r_{C02}} \end{bmatrix};
 \end{aligned}$$

$$E_{2|S-IV} = \begin{bmatrix} \frac{F_{1|S-I}}{L_{b1}} + E_{31|S-III} \\ \frac{F_{1|S-I}}{L_{b2}} + E_{41|S-III} \\ \frac{F_{1|S-I}}{L_{02}} + E_{51a|S-III} \\ -(E_{61b} + E_{61a}) \\ 0 \end{bmatrix}; E_{3|S-IV} = \begin{bmatrix} \frac{1}{L_{b1}}(-I_{L02}G_1) \\ 0 \\ \frac{F_{1|S-I}}{L_{02}} + E_{51b|S-III} \\ E_{61a} \\ 0 \end{bmatrix};$$

where, $F_{3|S-IV} = F_{3|S-III}; F_{2|S-IV} = F_{2|S-III};$ (A4.27)

List of Publications

INTERNATIONAL JOURNALS

1. M. M. Masoom, M. Kumar, and N. Kumar, "Controllability Analysis and Controller Design of Time-Multiplexed Multiport Fault-Tolerant DC-DC Converter," *IEEE Transactions on Industrial Electronics*, (Accepted on 16 March 2026). **Impact factor: 7.2**
2. M. M. Masoom, M. Kumar, and N. Kumar, "Design and Characterization of Solar PV fed Fault Tolerant Multiport Converter with Reduced Current Ripple," *IEEE Transactions on Industry Applications*, vol. 61, no. 4, pp. 6644-6660, July-Aug. 2025, doi: 10.1109/TIA.2025.3544565. **Impact factor: 4.5**
3. M. M. Masoom, M. Kumar, and N. Kumar, "Robust Design and Controllability Analysis for Voltage Mode Controlled Multiport Converter with Structured Uncertainties," *International Journal of Circuit Theory and Applications* (2025): 1–16, <https://doi.org/10.1002/cta.70261>. **Impact factor: 1.6**

UNDER REVIEW

1. M. M. Masoom, M. Kumar, and N. Kumar, "Fault-Tolerant Soft-Switched Modular Bidirectional DC-DC Multiport Converter," *IEEE Transactions on Industry Applications*.

INTERNATIONAL CONFERENCES

1. M. M. Masoom, M. Kumar and N. Kumar, "Time-Multiplexed Fault-Tolerant Soft-Switched DC-DC Multiport Non-Isolated Converter," 2025 IEEE 5th *International Conference on Sustainable Energy and Future Electric Transportation (SEFET)*, Jaipur, India, 2025, pp. 1-6, doi: 10.1109/SEFET65155.2025.11255042.
2. M. M. Masoom, N. Kumar and M. Kumar, "Design and Power Flow Control in Standalone PV System with Reduced Battery Current Ripple," 2023 *International Conference on Power, Instrumentation, Control and Computing (PICC)*, Thrissur, India, 2023, pp. 1-6, doi: 10.1109/PICC57976.2023.10142520.

INDIAN PATENT

1. Fault-Tolerant Soft-Switched Modular Bidirectional DC-DC Multiport Converter. **(Published)**

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EDUCATION		
CLASS/DEGREE	INSTITUTE	YEAR
Ph.D.	Delhi Technological University, Delhi	2021-2026
M. Tech	Delhi Technological University, Delhi	2018-2020
B. Tech	Sir M. Visvesvaraya Institute of Technology, Bengaluru	2013-2017
Intermediate (C.B.S.E.)	A.R.S Public School, Bokaro Steel City	2010-2012
High School (I.C.S.E.)	Carmel School, Madhupur	2010

PROJECT

- “**Development of Fault Tolerant Power Converters for Solar PV-fed Hybrid Electric Vehicles (PVHEVs)**” under the guidance of Asst. Professor Dr Mayank Kumar, which is funded by the Science and Engineering Research Board (SERB), Department of Science & Technology, Government of India, under the SERB sanction order number **SRG/2021/001640** for a duration of 2 years from 30th December 2021 to 29th December 2023.

TECHNICAL SKILLS

Engineering Software	MATLAB/SIMULINK, PLECS, PS-CAD, EasyEDA, Altium
Programming Language	C/C++ and Python (Basics)
Other/s	Advanced MS Office

AWARDS AND ACHIEVEMENTS

- Graduate Aptitude Test in Engineering (GATE) Qualified 2018.
- Reviewed several peer-reviewed research articles for leading IEEE journals, including two for *IEEE Transactions on Power Electronics* and one for *IEEE Transactions on Industrial Electronics*.