

DESIGN AND ANALYSIS OF POSITIVE FEEDBACK SOURCE COUPLED LOGIC FOR PERFORMANCE ENHANCEMENT

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by

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CANDIDATE'S DECLARATION

I Shikha hereby certify that the work which is being presented in the thesis entitled **“Design and Analysis of Positive Feedback Source Coupled Logic for Performance Enhancement”** in partial fulfillment of the requirements for the award of the Degree of **Doctor of Philosophy**, submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from **January 2020 to June 2026** under the supervision of **Dr. Neeta Pandey and Dr. Kirti Gupta**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Candidate's Signature

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

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Certified that **Shikha** (Roll No. 2K19/PHDEC/505) has carried the research work presented in this thesis entitled “**Design and Analysis of Positive Feedback Source Coupled Logic for Performance Enhancement**” for the award of the Degree of **Doctor of Philosophy** from the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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*Dedicated with heartfelt gratitude to my Parents,
Husband, Son, and esteemed Supervisors for their
constant support, guidance, and encouragement
throughout this journey.*

ABSTRACT

With the rising demand for portable and low-power electronic systems such as consumer gadgets, biomedical implants, and sensor nodes, the design of mixed-signal systems that place both analog and digital circuits on a single chip have become increasingly important. Such integration benefits from fewer interfaces, lower power consumption and higher speed. In mixed-signal systems, the switching noise generated in digital blocks can adversely affect the performance of on-chip analog circuitry. In CMOS logic, this noise arises from current spikes and transient voltage fluctuations during switching. To mitigate these effects, several techniques at the various levels of abstractions have been developed. Among them, low switching-noise logic families have gained attention, as they maintain nearly constant supply current during transitions and operate with smaller voltage swings. Some notable logic styles are current steering logic (CSL) style, current balance logic (CBL) style, folded source coupled logic (FSCL) style and the source coupled logic (SCL) style.

Positive feedback is introduced in SCL wherein the reference voltage source is omitted for improving speed. The resulting logic family is called positive feedback source coupled logic (PFSCCL) which has emerged as a promising option due to its inherently low noise switching characteristics. The PFSCCL gates are primarily based on NOR/OR gates and hence infer cascading of gates of complex logic function realization. The existing PFSCCL fundamental cell-based gates enable single stage realization of complex logic functions by accommodating two or more minterms, however, they occupy larger area. This work investigates PFSCCL circuits and presents design enhancements aimed at improved overall efficiency. Here, the memristors are integrated into the PFSCCL realization to improve integration density and performance. Two designs are proposed, the first design incorporates memristors into the PFSCCL inverter whereas the second integrates memristors into the PFSCCL NOR/OR gate. The proposed designs have reduced gate count in comparison to PFSCCL NOR/OR gates, and reduced footprint than fundamental cell-based realization, thus leading to lower propagation delay and reduced power consumption.

Owing to positive feedback, low voltage swing and presence of constant current source, the PFSCCL style is known for high-speed operation. There is static power consumption in the circuit which limits its usage in battery-powered applications. The dynamic PFSCCL (D-PFSCCL) has been introduced to reduce power consumption wherein dynamic current source is employed in place of constant current source. The earlier work on D-PFSCCL gates focused primarily on improving dynamic current source and enhancing logic implementation using fundamental cells and transmission-gates. The logic implementation occupies larger area, therefore memristors are incorporated in D-PFSCCL design which not only reduce cascading for complex function realizations, but also improve footprint.

The registers are vital components used widely for data storage, data manipulation, and temporary data storage in high-performance computing used in SoC realizations.

The CMOS registers suffer from high switching noise and fail to provide an analog friendly environment in mixed-signal applications. Also, the significant power consumption at high operating frequency needs attention. To bridge this gap, PFSCl registers are designed. The available switch and sleep based tristate PFSCl buffers/inverters are used to realize static and dynamic PFSCl registers. These registers are based master slave approach wherein clock and its complement are used for proper operation. The issue of clock-skew is analyzed and a solution is also suggested to overcome this.

The operation of PFSCl gates developed using metal oxide semiconductor field-effect transistor (MOSFET) in deep submicron nodes deteriorate due to short-channel effects, leakage, and mobility degradation. The carbon nanotube FETs (CNTFETs) have emerged as a viable alternative owing to their near-ballistic transport, high mobility, and low leakage. The nonavailability of PFSCl circuit realizations in CNTFET is addressed next in this work. It is found that there is significant improvement in propagation delay.

All the proposed designs are functionally validated through extensive SPICE simulations using PTM 90 nm technology parameters. The proposals are also laid out using Microwind to assess area efficiency. The performance of the proposals is compared with existing counterparts in terms of propagation delay, power consumption, power delay product and area. Additionally, Stanford University 32 nm CNTFET model is used to validate the performance of CNTFET based gates.

LIST OF PUBLICATIONS

List of Journal Papers

1. Shikha, Neeta Pandey, and Kirti Gupta. "Memristor-based architectures for PFSCCL circuit realizations." *Circuits, Systems, and Signal Processing* 42, no. 8 (2023): 4985-5012.
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LIST OF ABBREVIATIONS

current steering logic	CSL
current balance logic	CBL
folded source coupled logic	FSCL
source coupled logic	SCL
Positive feedback source coupled logic	PFSCCL
fundamental cell	FC
dynamic PFSCCL	D-PFSCCL
carbon nanotube FETs	CNTFETs
System-on-Chip	SoC
analog-to-digital converters	ADCs
digital-to-analog converters	DACs
pull-down network	PDN
MOS current mode logic	MCML
quadtail cell	QC
linear feedback shift registers	LFSR
self-timed buffers	STB
transmission gates	TGs
dynamic current source	DCS
power delay product	PDP
parity generator	PG
carry skip adder	CSA
memristor based network	MBN
constant bias current	I_{ss}
voltage swing	V_{SWING}

small-signal voltage gain	A_v
noise margin	NM
propagation delay	τ_{PD}
drain-bulk junction capacitance	C_{db}
gate-source capacitance	C_{gs}
gate-drain capacitance	C_{gd}
two-input NOR gate	NOR2
two-input NAND gate	NAND2
two-input exclusive-OR gate	XOR2
bias voltage	V_{BIAS}
power supply	V_{DD}
platinum	Pt
low resistance state	LRS
high resistance state	HRS
low voltage level	V_{OL}
high voltage level	V_{OH}
carbon nanotube	CNT
multi-tube CNTFET width	W_g

CHAPTER 1

INTRODUCTION

1.1 Background

The rapid advancement in technology and the rising demand for portable and consumer electronic devices have led to a growing need of integrating multiple functions onto a single semiconductor chip. This has resulted in the widespread adoption of System-on-Chip (SoC) designs, where both analog and digital circuits are implemented on the same silicon die. Such integration improves the performance by reducing the propagation delay associated with inter-chip communication [1-7]. However, integrating analog and digital blocks together introduces certain challenges, particularly due to the noise generated by the digital logic components. Conventional CMOS logic, which is most used in SoC designs, produces significant switching noise during transitions. This switching noise severely degrades the performance of sensitive analog circuit, making it difficult to maintain high signal fidelity in mixed-signal environments [8-10]. To overcome this challenge, designers attempt to either reduce the noise or isolate the analog and digital blocks through appropriate design techniques. Various strategies have been proposed to reduce or manage this noise, such as optimizing the layout, controlling the placement of input/output pins, designing effective signal routing, using alternative substrate materials, and adopting noise-tolerant logic styles [11-34]. Among these, using alternative logic style with reduced switching noise for digital circuit design is one of the most effective approaches.

Alternative logic styles suited for mixed-signal applications typically maintain a nearly constant current during transitions and operate with reduced voltage swing. These features help in lowering the switching noise and making the design more robust. According to their mode of operation, four logic styles are identified: current balanced logic (CBL) [21-24], current steering logic (CSL) [25-27], folded source coupled logic (FSCL) [8, 28-30], and source coupled logic (SCL) [35-37]. Within these logic families, several enhanced variants have been proposed to improve performance of conventional topologies. Among all these, the SCL style is an amenable solution due to its simple structure and superior noise performance [35-37]. The SCL gate has a pair of NMOS transistors connected in a source coupled configuration and uses a current source. It works with reduced voltage swing and the presence of current source significantly reduces switching noise thereby making it well-suited for mixed-signal applications. It has been shown that SCL gates can reduce digital switching noise by nearly two orders of magnitude when compared to conventional CMOS logic gates [14-16]. The SCL gates are generally categorized as either differential or single-ended gates [35, 37]. Differential gates use series-gating approach for logic implementation, while single-ended gates have a structure where

input transistors share common source and are source coupled to a transistor whose gate is connected to reference voltage source [35-37]. Due to their excellent noise suppression capabilities and efficient power usage, SCL gates are widely used in a variety of high-speed digital applications. These include analog-to-digital converters (ADCs), digital-to-analog converters (DACs), front-end receivers, optical communication systems, and arithmetic units, among others [38-59]. A modified variant of the single-ended SCL approach, known as positive feedback source coupled logic (PFSCl), has been introduced in [37] to achieve enhanced high-speed performance. In this work, PFSCl style is thus, chosen for implementation of complex logic gates using improved realizations.

1.2 Positive feedback source coupled logic (PFSCl) style

A conventional SCL gate consists of a pull-down network (PDN), a constant current source and load transistor. A generic SCL gate consists of N-parallel input transistors source coupled to a single transistor in the PDN driven by an external voltage reference source [35]. Here, positive feedback is introduced in PDN of conventional SCL gate [37] to eliminate external voltage reference in source couple logic and the resulting variant of SCL is named as Positive Feedback SCL (PFSCl). It outperforms conventional SCL in terms of speed and power consumption.

PFSCl gates are single-ended and the conventional NOR/OR based realization scheme is followed which enables low voltage operation in comparison to differential SCL gates [37]. The potential and versatility of PFSCl style have been investigated [60-68] extensively in design of digital systems including arithmetic units, buffers, pipeline circuits, latches, as well as error detection and correction blocks [69-78].

The operation of PFSCl gates is explained along with the characterization of performance such as small-signal voltage gain, noise margin, and voltage swing and propagation delay in terms of bias current, transistor dimensions, and process parameters. Further enhancement of the propagation delay modeling for PFSCl gates is presented in [60], where an analytical expression of PFSCl gate for propagation delay is formulated based on the parasitic capacitances at the output node. The propagation delay derivation is performed by linearizing the circuit around the logic threshold, which enables simplified analytical evaluation through appropriate approximations.

The design aspects of PFSCl gates are examined in [61-62] with a focus on optimizing key performance metrics such as propagation delay, power consumption, and area usage. These parameters often involve trade-offs between the performance parameters depending on the applications specific requirements. In a separate study [63], PFSCl gates are compared with differential SCL also called as MOS current mode logic (MCML) gates by implementing and simulating basic logic functions like AND, OR, and NOR. The simulation results demonstrated that PFSCl gates are not only faster

but also require lesser chip area than their MCML counterparts under the same power supply and bias current conditions. Thus, making PFSCl a more effective choice for applications demanding both speed and compactness.

The concept of hysteresis is utilized in the design of PFSCl gates for improved performance [64]. The hysteresis improves the noise margin of the PFSCl gate. This implies that, for a given noise margin, a lower voltage swing is sufficient to maintain signal integrity, which reduces the propagation delay. For a given speed requirement, this reduction in propagation delay can be traded off with bias current to reduce the power consumption. Thus, PFSCl gates with hysteresis are more suitable for high-speed, low-power digital circuit designs.

Another improvement suggested in [65] is focused on enhancing the speed of PFSCl gates by replacing the conventional resistive/PMOS load with an active inductor load that comprise of NMOS and PMOS transistors. This load exhibits capacitive coupling which accelerates the charging and discharging of load capacitance. A mathematical model to establish relation between capacitive coupling and improvement in propagation delay is also discussed.

The conventional PFSCl gates follow NOR/OR based realization scheme. However, complex functions are generally expressed as sum-of-minterms that involves both AND and OR logic. Thus, in such cases, the implementation using conventional PFSCl realization scheme style becomes challenging. The functions require cascade of multiple PFSCl gates, which not only increase the propagation delay but also result in higher power consumption, since each gate maintains a separate constant current source. In an effort to address the issue, the use of multitail PFSCl gates are suggested in literature [66-69]. These gates introduce the capability of implementing AND-OR functionality in PFSCl style. Different multitail PFSCl gates namely fundamental cell (FC) [66-67], multithreshold FC [68] and quadtail cell (QC) [69] are suggested. Their use in logic function design reduces propagation delay and power consumption. The PFSCl FC proposed in [66] utilizes the triple-tail cells to implement a logic function expressed as sum of two minterms. This use of cell in PFSCl circuits reduce the number of stages and gate count. The same is illustrated through the design of FC based D-Latch achieves lower propagation delay and power consumption in comparison to conventional NOR/OR based D-Latch [66]. The configuration of PFSCl FC to implement different functions is also explained. The use of PFSCl FC has been extended for implementing a variety of digital circuits namely adders, serializers, demultiplexers, linear feedback shift registers (LFSRs), razor flip-flops and comparator [69-76]. The results consistently showed that PFSCl FC based designs outperform the conventional NOR/OR PFSCl based counterparts in terms of speed and power consumption. The study in [69-77] presents a modified CLB, an enhanced form of PFSCl FC, to better support complex logic functions for increases fan-in. The suggested cell design introduces an additional transistor in the outer branch, placed in parallel with the conventional FC. This change leads to a reduction in the total number

of gates needed for the comparator realization. The scheme is however restricted to certain type of logic function and thus cannot be generalized.

The use of PFSCCL logic in asynchronous pipeline design is illustrated in [78]. The pipeline designs in conventional NOR/OR, FC PFSCCL style are suggested. A hybrid realization pipeline design that optimizes the design by employing both conventional NOR/OR and FC based PFSCCL gates is also presented. The results show that the hybrid pipeline design reduces the gate count and the average power consumption, making it a more efficient option for asynchronous data processing systems.

In an effort to explore PFSCCL style in ultra-low power regime, the PFSCCL gates design for operation in subthreshold region is presented in [79]. The subthreshold PFSCCL gates significantly reduces static power consumption and maintains an acceptable switching behavior due to the reinforcing effect of positive feedback. The results demonstrate that subthreshold PFSCCL gates are highly suitable for ultra-low-power applications such as IoT nodes, wearable devices, and biomedical sensors.

A dynamic variant of PFSCCL style, referred to as dynamic positive feedback source coupled logic (D-PFSCCL) style that eliminates static power consumption and retains high-speed characteristics is presented in [80]. The conventional D-PFSCCL gates implements the functionality in the NOR/OR form only and works on precharge and evaluate logic. For complex functions, the cascaded D-PFSCCL gates malfunction and therefore the insertion of self-timed buffers (STB) is suggested [80]. Further, the AND-OR functionality and enhanced fan-in capability is imparted in the D-PFSCCL gates through the use of multithreshold transistors [81] and transmission gates (TGs) [82]. The other modification in D-PFSCCL gates is related to the dynamic current source (DCS). The modified DCS requires only true phase of clock signal and avoids the use of inverted clock signal as used in conventional D-PFSCCL gates.

The design of tristate buffer/inverter is also explored in PFSCCL style. Two different design methods named as switch and sleep transistor based are presented in [67, 83-84]. The conventional sleep transistor based PFSCCL tristate buffer/inverter design is found to be more power efficient, however it provides incomplete isolation of the output node during the high impedance state. Next in the paper, improved switch based and sleep transistor based tristate buffer/inverter topologies are put forward in [67,83-84]. Here, both the load section and current source are carefully modified to completely restrict the flow of bias current in the high impedance state. Further, the use of PFSCCL tristate buffer/inverter for the design of bus-based communication systems and D-latch design is illustrated in [83-84].

1.3 Motivation and scope of work

A conventional static PFSCCL gate implements the logic function based on NOR/OR realization scheme. This type of realization, in general, infers cascade of multiple PFSCCL NOR/OR gates with each gate employing a separate current source [37]. This

arrangement increases the overall propagation delay and power consumption. An alternate PFSCl multitail cell-based realization schemes that facilitates AND-OR functionality so as to provide the capability for implementing minterms of a logic function in a single PFSCl gate are suggested [66-69]. However, both the schemes infer multistage realization with high gate count and area that mitigate high speed advantage of PFSCl style. Thus, the realization of static PFSCl gates can further be enhanced by exploring design techniques that allow realization of logic functions with high fan-in in a single PFSCl gate [66,68-69]. These design techniques are aimed to further lower the gate count and improve the overall propagation delay and power consumption.

Another important challenge in modern VLSI design arises from the growing use of portable electronic devices, which demand extremely low power consumption circuits to minimize overheating and enhance portability. One effective approach to lower static power consumption is to further investigate D-PFSCl gates [80]. The existing work done in D-PFSCl gates is focus on the improvement of DCS [67,80] and PDN [81-82]. The D-PFSCl with modified PDN employs multithreshold transistors [81] or TGs [82], both of which results in significant area penalty. Thus, there is a scope to explore new methods to design D-PFSCl gates with reduced footprints.

Several techniques to realize PFSCl tristate buffer/inverter are suggested in literature [83-84]. The use of PFSCl tristate buffer/inverter has been demonstrated to design bus-based communication system and D-latch [83-84]. Their use can further be extended to the design of registers. The register design can further be analysed for clock skew sensitivity and subsequent clock insensitive PFSCl register design can be worked upon.

In literature, several studies emphasize that MOSFET scaling into the nanometer regime introduces critical challenges such as short-channel effects, increased leakage, and mobility degradation, all of which adversely impact circuit performance [85-88]. Thus, it becomes necessary to investigate PFSCl circuit design by employing alternate devices suited to nanometer regime. In literature, carbon nanotube field effect transistors (CNTFETs) is explored as an alternative as it offers near-ballistic transport, high carrier mobility, and reduced leakage currents [85-88]. Hence, incorporating CNTFET devices into the PFSCl gates can be worked upon.

In this work, various improved designs for PFSCl gates are explored with the aim of achieving the following objectives:

1. To design improved static PFSCl gates.
2. To explore methods for reducing the footprint of dynamic PFSCl gates.
3. To realize registers using PFSCl tristate buffer/inverter.
4. To investigate the use of advanced transistor technology in PFSCl style.

The following section highlights the key contributions made to achieve the defined objectives:

1. Two different realization schemes that incorporates memristors in static PFSCl gates are proposed. The realizations support higher fan-in by enabling the implementation of three-input logic functions with AND-OR functionality in a single stage. The proposed gates show improved propagation delay and power consumption in comparison to existing conventional static PFSCl counterparts.
2. Two memristor based designs are proposed for D-PFSCl gates. These realizations enhance the fan-in of D-PFSCl gates and subsequently reduces cascading of multiple stages. Thus, the proposed designs lead to improvements in overall propagation delay, power consumptions, and area.
3. The use of tristate PFSCl buffer/inverter is extended to the design of static and dynamic registers by following master slave configuration. The proposed PFSCl registers are further analyzed for clock skew sensitivity, and methods to design clock-insensitive PFSCl register design are worked upon.
4. The operation of CNTFET based PFSCl gates are investigated and a performance comparison is performed with MOSFET based counterparts. The study shows significant improvement in propagation delay and power delay product (PDP).

1.4 Organization of the thesis

In this work, novel PFSCl gate designs are developed through memristor integration, that enables the realization of complex logic functions with enhanced fan-in for AND-OR functionality. The proposed PFSCl gates offers improvement in propagation delay, power consumption and area. Additionally, the thesis presents PFSCl register designs with low power and clock skew insensitivity using PFSCl tristate buffer/inverter configurations. Finally, the potential of next generation device technologies is explored by employing CNTFET in PFSCl gates that resulted in notable improvements in propagation delay and PDP over MOSFET based PFSCl counterparts.

Chapter 2 presents an overview on the available static and dynamic PFSCl gates. Further, the operation of existing switch and sleep transistor based PFSCl tristate buffer/inverter is also elucidated.

Chapter 3 presents new design schemes for improving the performance of static PFSCl gates. The schemes are based on integrating memristor based network (MBN) with PFSCl inverter and PFSCl NOR/OR gates. Mathematical analysis to determine the voltage swing of the proposed gates is presented. The design scheme with memristor integration with PFSCl inverter is found to be area efficient while the scheme that integrated memristor with PFSCl NOR/OR gates provide reduced

propagation delay. The suitability of proposed gates in complex function realization is examined through implementation of 3-bit parity generator (PG), and 4-bit carry skip adder (CSA).

Chapter 4 focuses on reducing footprint of D-PFSCL gates. A memristor based network (MBN) is embedded within the D-PFSCL gate, forming a memristor aided dynamic PFSCL realization. Two new design schemes are put forward wherein MBN is integrated with D-PFSCL inverter and D-PFSCL NOR gate. Mathematical formulations to determine the voltage swing and propagation delay for proposed designs are put forward. The design scheme with memristor integration with D-PFSCL inverter is found to be area efficient while the D-PFSCL NOR based realization gives better propagation delay. The suitability of proposed gates in complex function realization is examined through implementation of 4:1 MUX.

Chapter 5 presents the design of PFSCL registers using switch and sleep transistor based PFSCL tristate buffers. Two register design approaches, namely static and dynamic registers, are presented. The working principle and structure of both approaches are discussed in detail. Through comparative analysis, it is observed that the sleep transistor based PFSCL register provides improved performance compared to the switch based design. Furthermore, the effect of clock skew on the performance of the proposed PFSCL registers is also investigated. Different methods are suggested to mitigate the impact of clock skew and ensure reliable register operation.

Chapter 6 presents the design of CNTFET PFSCL gates and compares their performance with MOSFET PFSCL counterpart. The gates implemented using CNTFET PFSCL styles shows advantages over conventional MOSFET PFSCL design in terms of propagation delay and PDP. A detailed analysis of these performance improvements is presented in this chapter.

Chapter 7 summarizes the work done throughout the thesis and brings forward potential avenues for future work.

CHAPTER 2

EXISTING PFSCCL GATES

2.1 Introduction

A comprehensive literature review on PFSCCL style highlighting the evolution of the logic style and identifying research gaps that form the basis for the current work was presented in the previous chapter. Building upon these insights, this chapter puts forward preliminaries of the existing PFSCCL designs. The available PFSCCL gates can be classified as static, dynamic and tristate buffer/inverter on the basis of their respective operating principles, design methodologies, and associated performance advantages.

2.2 Static PFSCCL gates

A conventional PFSCCL gate [37] is an improved form of SCL gates. These gates incorporate positive feedback by replacing the reference voltage source in the PDN of SCL gates. This arrangement improves the switching speed of the gate in comparison to the SCL gates. A discussion on the operating principle and performance parameter is presented further.

2.2.1 Conventional static PFSCCL gate

A generic N-input PFSCCL gate is shown in Fig. 2.1. The gate comprises of three basic sections, namely pull-down network (PDN), current source, and load transistors. The PDN consists of N-input transistors (M_1 - M_N) that are source coupled with a feedback transistor M_F to realize the given functionality in a NOR/OR form. The current source M_B maintains a constant bias current (I_{SS}) while the load transistors MP_1 and MP_2 perform the current-to-voltage conversion. It is pertinent to mention here that a generic N-input PFSCCL gate of Fig. 2.1 realizes NOR functionality. However, the same gate can be configured for OR functionality by obtaining the output from the drain terminal of load transistor (MP_2).

Operation and analysis

The static PFSCCL gates works on the current steering principle. Based on the logic level of the inputs A_1 - A_N , the bias current I_{SS} flows either through M_1 - M_N or M_F . If any of the inputs A_1 - A_N is/are high, I_{SS} flows through the corresponding ON transistors (left side branch) and a low voltage level is obtained at the output node, Q. Conversely, if all the inputs are low, a high voltage level is obtained at the output node, Q as I_{SS} gets steered through M_F (right side branch).

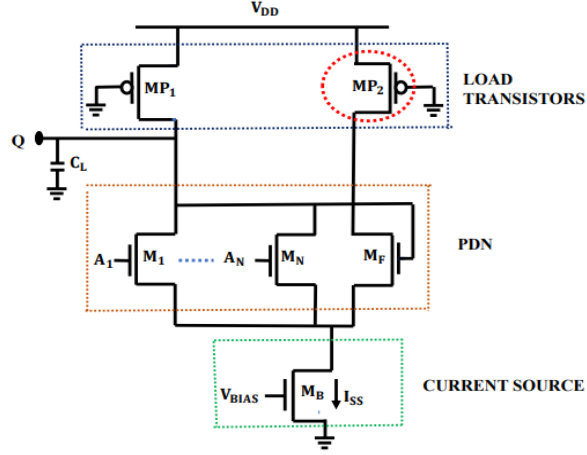


Fig. 2.1 Schematic of a generic N-input PFSCS gate [67]

A PFSCS inverter as drawn in Fig. 2.2 is considered to analyze the behavior. For a low voltage level at input A, M_1 is OFF and I_{SS} gets steered through M_F such that there exists no voltage drop across load transistor MP_1 . Thus, a high output voltage, V_{OH} is obtained at the output node, Q. Alternatively, for a high voltage level at input A, I_{SS} is steered through M_1 and a low output voltage, V_{OL} is obtained at the output node.

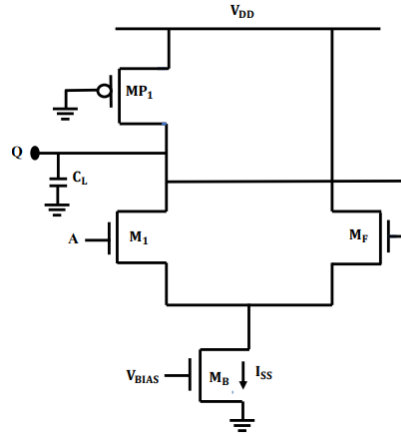


Fig. 2.2 PFSCS inverter [37]

The behaviour of a PFSCS inverter is analysed in terms voltage swing (V_{SWING}), small-signal voltage gain (A_v), and noise margin (NM). To calculate their values, it is necessary to determine the high and low output voltage levels. The output voltage for a PFSCS inverter, in general can be calculated as:

$$V(Q) = V_{DD} - I_{D,MP_1} R_P \quad (2.1)$$

Where I_{D,MP_1} and R_P are the drain current and equivalent linear resistance of load transistor MP_1 [37].

For a low voltage level at input A, transistor M_1 is OFF therefore no current flows through MP_1 ($I_{D,MP_1} = 0$). A high output voltage, V_{OH} is obtained and calculated as:

$$V(Q) = V_{OH} = V_{DD} \quad (2.2)$$

Similarly, for a high voltage level at input A, the current I_{SS} flow through transistor M_1 and load transistor MP_1 . The low output voltage, V_{OL} in this case is given as:

$$V(Q) = V_{OL} = V_{DD} - I_{SS} R_P \quad (2.3)$$

Voltage swing (V_{SWING}) [37]: The voltage swing is defined as difference of high and low output voltage levels and is computed as:

$$V_{SWING} = V_{OH} - V_{OL} = V_{DD} - (V_{DD} - I_{SS} R_P) \quad (2.4)$$

$$V_{SWING} = I_{SS} R_P \quad (2.5)$$

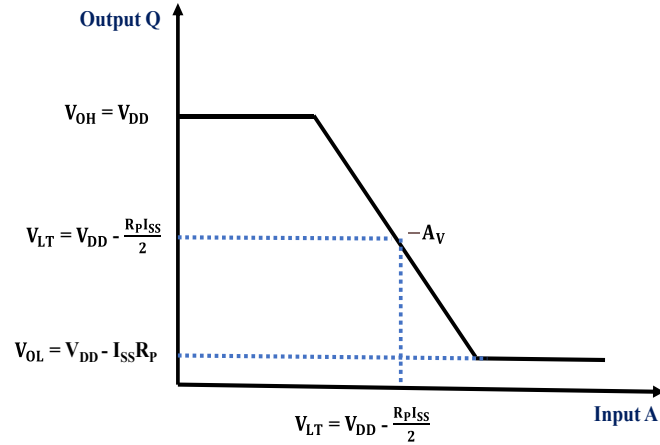


Fig. 2.3 Voltage transfer characteristics of a PFSCSCL inverter

The voltage transfer curve (VTC) of a PFSCSCL inverter is shown in Fig. 2.3. The curve is symmetric around the logic threshold voltage (V_{LT}) [37].

Small signal voltage gain (A_V) [37]: By applying superposition of the input signals applied to the gates of transistors M_1 and M_F , the A_V is calculated in the region near V_{LT} as:

$$A_V = \frac{g_{m,n} \frac{R_P}{2}}{1 - g_{m,n} \frac{R_P}{2}} \quad (2.6)$$

where $g_{m,n} = \sqrt{\mu_n C_{ox} \frac{W_N}{L_N} I_{SS}}$ is the transconductance of the transistors M_1 - M_F . The symbols μ_n , W_N and L_N represent effective electron mobility, effective channel width and channel length of the said transistors, respectively.

Noise margin (NM): The NM can also be computed by using the piecewise-linear approximation of the VTC [37] as:

$$NM = \frac{V_{SWING}}{2} \left(1 - \frac{1}{A_V} \right) \quad (2.7)$$

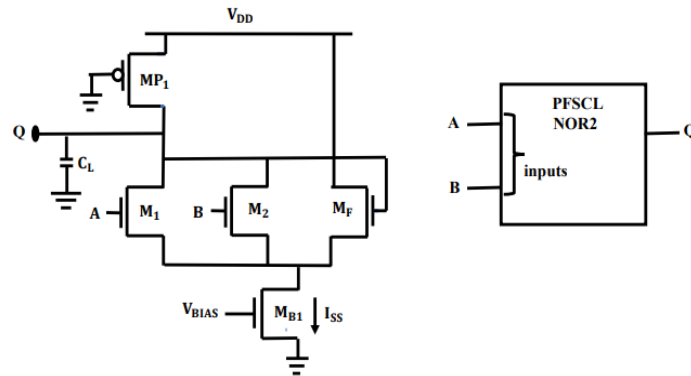
Propagation delay (τ_{PD}) [62]: The propagation delay of a PFSCSCL inverter is computed by analyzing linearized half circuit model. The propagation delay, τ_{PD} is evaluated as:

$$\begin{aligned} \tau_{PD} &= R_p C_{OUT} \\ &= R_p \left(C_{db,M1} + C_{gd,M1} + C_{db,MP1} + C_{gd,MP1} + C_{gd,MF} + \frac{1}{2} C_{gs,MF} + C_L \right) \end{aligned} \quad (2.8)$$

The total output capacitance C_{OUT} is evaluated by accounting for both intrinsic transistor capacitances and the external load capacitance C_L . For NMOS and PMOS devices, these intrinsic components include the drain–bulk junction capacitance (C_{db}), gate–source capacitance (C_{gs}), and gate–drain capacitance (C_{gd}). Owing to the Miller effect related to the gain between gate and source of transistor M_F , the effective contribution of C_{gs} is considered as half of its value [62].

Realisation of conventional static PFSCSCL gates

The conventional realization scheme of PFSCSCL gates is based on NOR/OR form of a function wherein the parallel input transistors are source coupled to a feedback transistor. The MOSFET based schematic and the symbolic representation of a two-input NOR gate (NOR2) gate is shown in Fig. 2.4(a). The same realization can be used as a two-input NAND (NAND2) gate by applying the inverted inputs through additional PFSCSCL inverters on the basis of De Morgan’s law as shown in Fig. 2.4(b). Thus, there exist cascading of PFSCSCL gates to implement NAND/AND functionality. The realization of two-input exclusive-OR (XOR2) gate is drawn in Fig. 2.5. The same NOR/OR realization scheme can be followed for the design of other complex functions having two or more inputs.



(a)

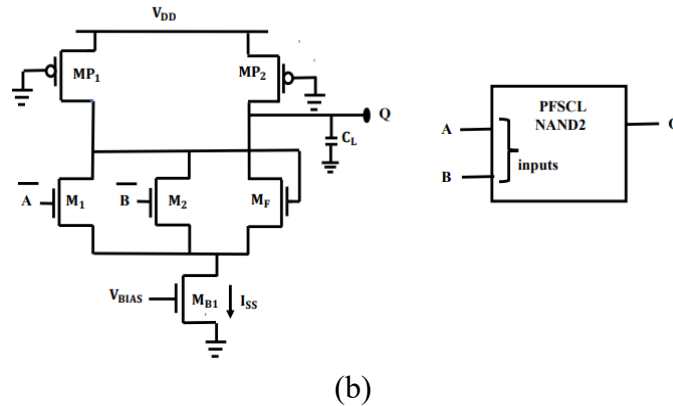


Fig. 2.4 Schematic and symbolic representation of conventional static PFSCS gates [66-67] (a) NOR2 (b) NAND2

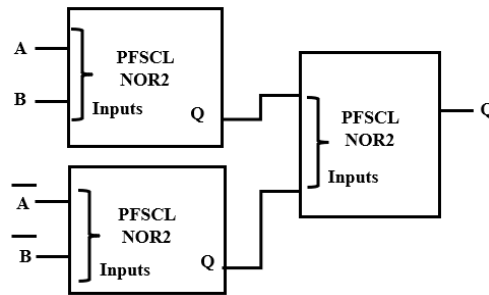


Fig. 2.5 Symbolic representation of conventional PFSCS XOR2 gate

2.2.2 PFSCS multitail cell

The conventional realization scheme in PFSCS style suggests the use of NOR/OR PFSCS gates only [37]. The basic capability of a PFSCS gate is further enhanced by introducing AND functionality along with the NOR/OR function. This is done by modifying the basic structure of PFSCS gate using multitail cell structure [66, 68-69]. A multitail cell is defined as the structure wherein multiple transistors are source coupled and their drain terminals are appropriately connected to either output or the power supply to implement AND functionality. In literature, different multitail cells named as fundamental cell (FC) [66], multithreshold fundamental cell [68] and quadtail cell (QC) [69] are suggested. A discussion on these multitail cells is presented further.

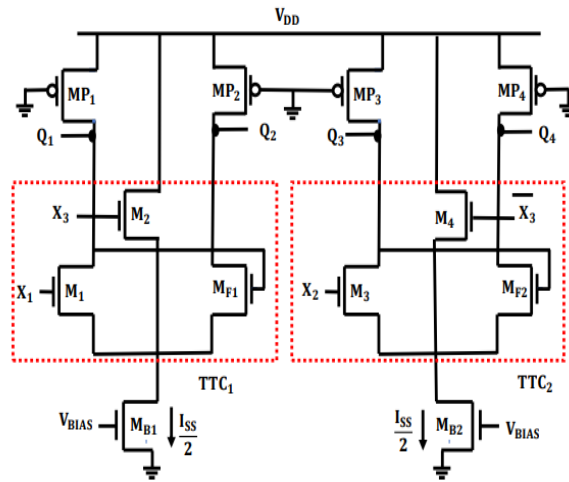
Conventional PFSCS FC

A conventional PFSCS FC suggested in [66] implements an arbitrary two input logic function expressed a sum of minterms in the single gate itself and thus, reduces cascading of stages. It consists of two triple-tail cells (TTCs) wherein each cell consists of three source coupled transistors. A FC comprising of two TTCs, namely TTC_1 (M_1, M_2, M_{F1}) and TTC_2 (M_3, M_4, M_{F2}), biased by two current sources is shown in Fig. 2.6(a). Each TTC has a current source of $I_{SS}/2$ value such that the PFSCS FC

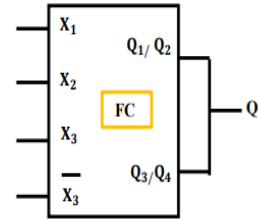
gate draws a total current of I_{SS} value from the power supply. It may be noted that a TTC connects middle transistors (M_2, M_4) in between the source coupled transistor pair (M_1, M_{F1}) and (M_3, M_{F2}) extending from the power supply to their respective common source node. The two TTCs, are driven by inputs X_1, X_2 , and X_3 and the output is obtained by performing wired-OR among any one of the outputs of the two TTCs $[(Q_1/Q_2), (Q_3/Q_4)]$. This feature enables FC to be configured for any arbitrary function [66-67]. At a particular instance, only one TTC is activated while the other TTC gets deactivated. An activated TTC has its middle transistor OFF such that the bias current ($I_{SS}/2$) flows in the outer transistors and generate the output accordingly. Conversely, a deactivated TTC has its middle transistor ON such that complete bias current ($I_{SS}/2$) flows through it and does not influence output. The proper activation/deactivation of a TTC requires the middle transistors M_2, M_4 to be made N times wider than M_1, M_3, M_{F1}, M_{F2} , so that maximum current flows through them. To illustrate this modification, consider the case when X_1, X_3 are at high logic level and X_2 is at low logic level. In this condition, TTC_2 is activated as M_4 is OFF. Alternatively, in TTC_1 , both M_1 and middle transistor M_2 are ON and in order to deactivate TTC_1 maximum current must flow through middle transistor M_2 . Thus, the width of middle transistor M_2 is made N times wider in comparison to the outer transistors M_1 and M_{F1} . The symbolic representation of FC is shown in Fig. 2.6(b) for simplification.

The output Q is given by

$$\begin{aligned}
 Q &= \overline{X_1} \overline{X_3} + \overline{X_2} X_3 \text{ if } Q_1 \text{ and } Q_3 \text{ are connected} \\
 &= \overline{X_1} \overline{X_3} + X_2 X_3 \text{ if } Q_1 \text{ and } Q_4 \text{ are connected} \\
 &= X_1 \overline{X_3} + \overline{X_2} X_3 \text{ if } Q_2 \text{ and } Q_3 \text{ are connected} \\
 &= X_1 \overline{X_3} + X_2 X_3 \text{ if } Q_2 \text{ and } Q_4 \text{ are connected}
 \end{aligned} \tag{2.9}$$



(a)



(b)

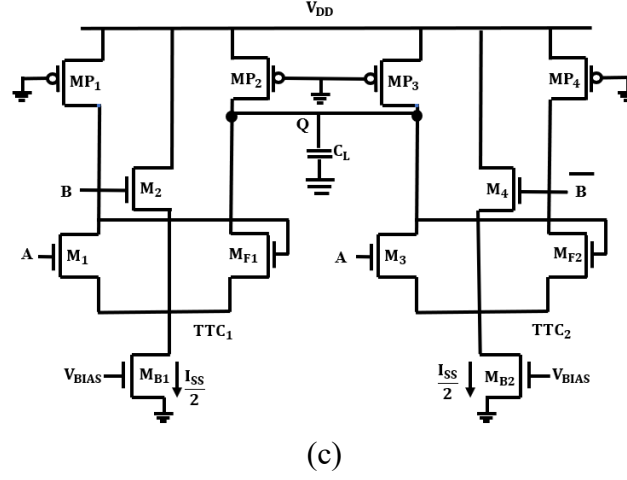


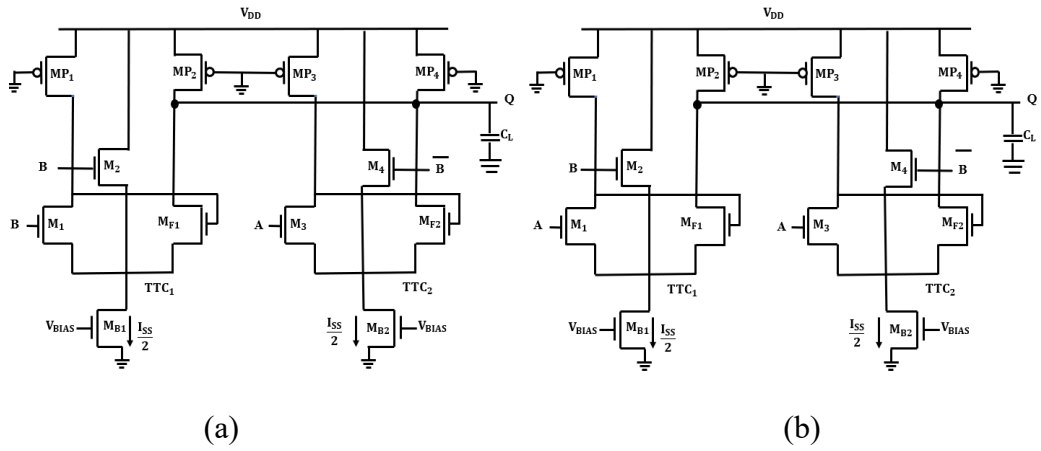
Fig. 2.6 Generic PFSCS FC [66-67] (a) Schematic (b) Symbolic representation (c) PFSCS FC XOR2 gate

Realization of FC based PFSCS gates

The concept of generic PFSCS FC is extended to implement a variety of two input logic functions. For example, the functionality of a XOR2 gate is obtained if input A is connected to X_1 and X_2 and input B is connected to X_3 in accordance to (2.9). By substituting the inputs, (2.9) represents the XOR2 functionality given as:

$$Q = A \cdot \bar{B} + \bar{A} \cdot B \quad (2.10)$$

The corresponding schematic of XOR2 gate is depicted in Fig. 2.6 I. The mapping of inputs X_1 , X_2 , and X_3 along with the interconnection of outputs Q_1 – Q_4 for implementing different two input logic functions is summarized in Table 2.1. The corresponding circuit representation of different logic functions is shown in Fig. 2.7. Furthermore, the FC based realization scheme has been applied to efficiently realize more complex circuits [71–76].



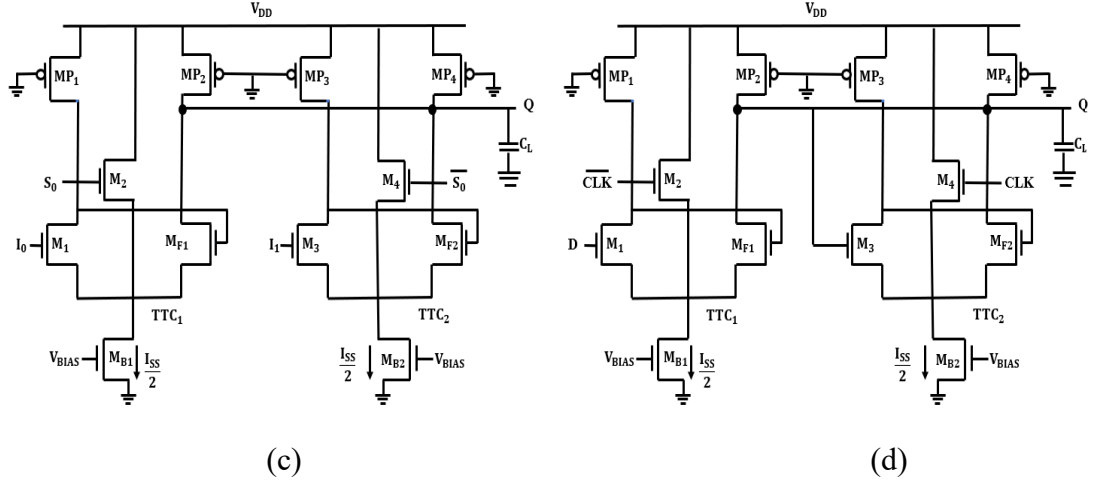


Fig. 2.7 Existing PFSCS FC based different logic functions [81] (a) AND2 (b) OR2 (c) 2:1 MUX (d) D-latch

Table 2.1 Mapping table of different logic functions

Logic function	Inputs	Mapping in PFSCS FC			Output
		X_3	X_1	X_2	
OR2	A, B	B	A	B	Q_2, Q_4
NOR2	A, B	B	A	B	Q_1, Q_3
NAND2	A, B	B	B	A	Q_1, Q_3
AND2	A, B	B	B	A	Q_2, Q_4
XOR2	A, B	B	A	A	Q_2, Q_3
XNOR2	A, B	B	A	A	Q_1, Q_4
2:1 MUX	S_0, I_0, I_1	S_0	I_0	I_1	Q_2, Q_4
D-latch	D, CLK	$\overline{\text{CLK}}$	D	D	Q_2, Q_4

Multithreshold PFSCS FC

In conventional PFSCS FC [66], the middle transistors are made wider than the outer transistors for proper operation. This requirement results in significant area overhead. An alternate FC topology suggests the use of low threshold voltage transistor as middle transistor for the proper operation of activation/deactivation. This FC topology is thus referred to as multithreshold PFSCS FC [68]. Fig. 2.8 shows the schematic of a general multithreshold PFSCS FC. The low threshold voltage NMOS transistors (M_2, M_4) are inserted between the source coupled transistor pair (M_1, M_{F1}) and (M_3, M_{F2}) extending from the power supply to their respective common source node and are represented using a bold symbol. The lower threshold voltage of the middle transistor M_2 and M_4 enables controlled conduction through the central branch. The generic multithreshold PFSCS FC can further be configured for different functionality by following the same mapping table as given for conventional FC in Table 2.1.

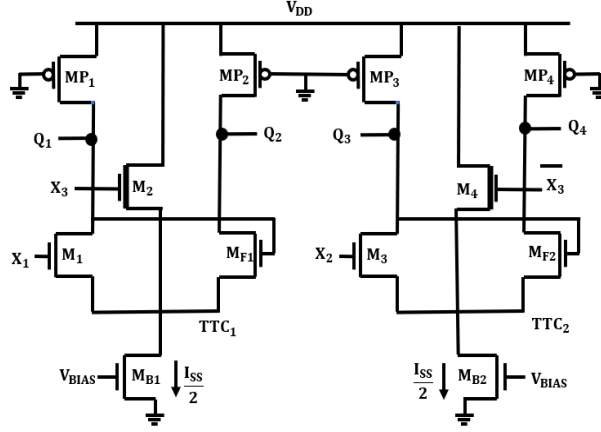


Fig. 2.8 Generic multithreshold PFSCS FC [68]

PFSCS quadtail cell (QC)

The concept of conventional PFSCS FC [66], approach is extended to realize logic function expressed as sum of minterms with 3-input variables in PFSCS circuits. The approach involves the use of a new circuit element named as PFSCS QC [69].

A PFSCS QC consists of four source coupled transistors (M_1 , M_2 , M_3 and M_F) connected to a constant current source (I_{ss}) as shown in Fig. 2.9. The transistors M_1 and M_F forms the outer transistor pair while the transistors M_2 , M_3 forms the inner transistor pair. The transistors in the inner pair are made N times wider in comparison to the outer transistor pair for proper activation/deactivation of the cell as done in conventional PFSCS FC. A suitable load can further be attached to the terminals Q_1 and Q_2 to obtain output from either Q_1 or Q_2 through current to voltage conversion by the connected load.

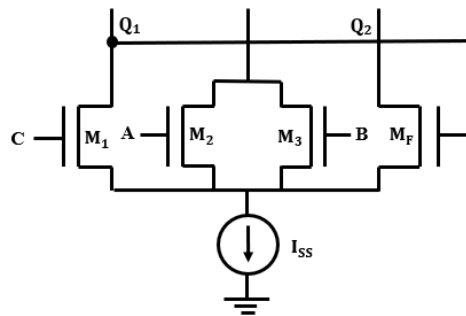


Fig. 2.9 Generic PFSCS QC [69]

The use of QC is extended to design a generic 3-input PFSCS gate with inputs X , Y , and Z . A generic PFSCS QC gate consisting of 4 QCs (QC_1 , QC_2 , QC_3 , QC_4) as shown in Fig. 2.10(a). The 4 QCs (QC_1 , QC_2 , QC_3 , QC_4) are attached to the load transistors (MP_1 , MP_2) as shown. The gate output is obtained by selecting one node from each QC and using it as either an inverter or a buffer depending on the required logic. Each QC is connected to current source of $I_{ss}/4$ value such that the PFSCS QC gate draws

a total current of I_{SS} value from the power supply. The generic PFSCS QC gate is configured as 3-input exclusive-OR (XOR3) gate as shown in Fig. 2.10(b).

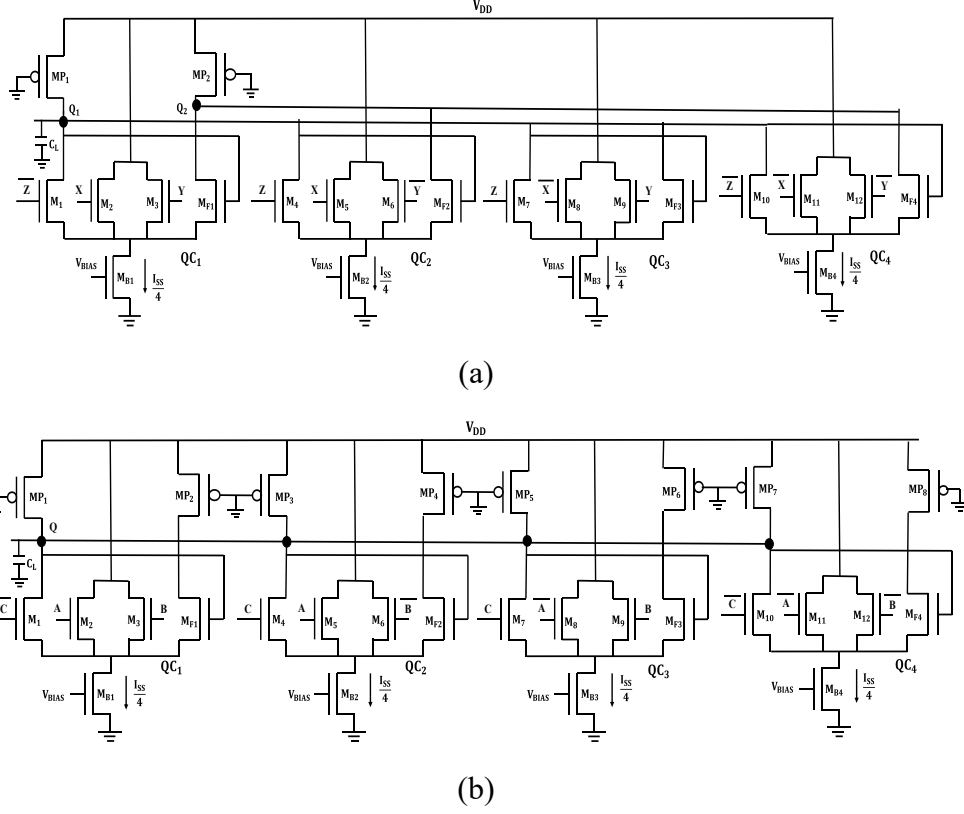


Fig. 2.10 (a) Generic 3-input PFSCS QC gate (b) PFSCS QC XOR3 gate [69]

2.2.3 Hybrid approach

The hybrid approach is based on the optimum design of PFSCS circuits through the use of available realization schemes. This approach involves the use of both NOR/OR and multitail cell realization schemes for the efficient design. Many hybrid realizations are suggested which show improved performance in comparison to the realizations based on using either NOR/OR or multitail cell realization schemes [71].

2.3 Dynamic PFSCS gates

This section describes the available dynamic PFSCS (D-PFSCS) gates [80]. Firstly, a brief on conventional D-PFSCS gate is presented which is followed by multithreshold transistor [81] and TG [82] based D-PFSCS designs.

2.3.1 Conventional D-PFSCS gate

The D-PFSCS gates offer enhanced speed and lower power consumption as compared to their static PFSCS counterparts [80]. A conventional D-PFSCS gate supports only

NOR/OR logic operations. The PDN is realized in the same manner as in static PFSCl gate, however the load transistor and the current source of conventional static PFSCl gate are replaced by precharge transistor and DCS respectively in a D-PFSCl gate. The circuit of a conventional D-PFSCl gate is depicted in Fig. 2.11. The PMOS transistor MP_1 serves as the precharge transistor, while the transistors M_{B1} , M_{B2} , and the capacitor C_{dyn} form the DCS. Both the precharge transistor and the DCS are controlled by a clock (CLK) signal.

Operation and analysis

A D-PFSCl gate works on precharge and evaluation logic depending upon the value of the CLK signal. When CLK is at low voltage level, the gate operates in the precharge phase. The precharge transistor MP_1 turns ON, and charges the output node, Q to V_{DD} . Simultaneously, the capacitor C_{dyn} is discharged to ground potential through the conducting M_{B2} transistor in DCS. During this phase, any changes in the inputs do not affect the output, as M_{B1} remains OFF. Conversely, when CLK is at high voltage level, the gate enters in the evaluation phase wherein M_{B1} conducts, while MP_1 and M_{B2} are turned OFF. In the evaluation phase, the output voltage at output node Q, either remains at high voltage level (V_{DD}) or discharges to low voltage level ($V_{DD} - V_{SWING}$), depending on the input conditions.

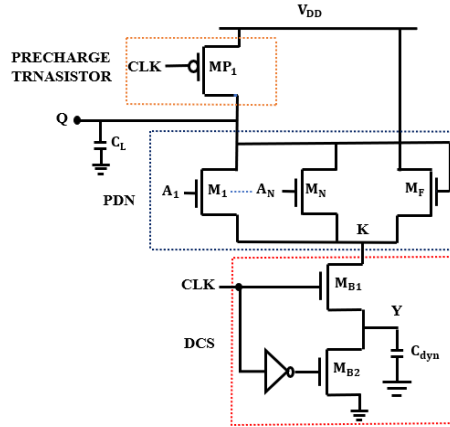


Fig. 2.11 Conventional D-PFSCl gate using NOR/OR scheme [80]

The necessary V_{SWING} in the evaluation phase is realized by choosing the capacitor C_{dyn} so that output capacitor discharges up to desired low voltage level, which is $V_{DD} - V_{SWING}$. It may be noted that output capacitance, C_{OUT} is sum of load capacitor C_L and parasitic capacitance associated with the transistors (M_1 - M_N , M_F , MP_1). Using the charge-conservation theorem, charge transfer between C_{OUT} and C_{dyn} is modelled as:

$$V_{DD}C_{OUT} = (C_{OUT} + C_{dyn})(V_{DD} - V_{SWING}) \quad (2.11)$$

$$C_{dyn} = \frac{V_{SWING} C_{OUT}}{V_{DD} - V_{SWING}} \quad (2.12)$$

In practical designs, a dummy transistor with a source and drain terminals shorted replaces the C_{dyn} capacitor. If the width and length of this dummy transistor are W_{Cdyn} and L_{Cdyn} , then its size can be calculated as:

$$W_{\text{Cdyn}} L_{\text{Cdyn}} = \frac{V_{\text{SWING}} C_{\text{OUT}}}{C_{\text{OX}}(V_{\text{DD}} - V_{\text{SWING}})} \quad (2.13)$$

C_{ox} denotes the oxide capacitance per unit gate area. D-PFSCL gates do not draw static power consumption since a continuous conductive path between the power supply and ground never forms. This behaviour is ensured by the switching mechanism of transistors M_{B1} and M_{B2} in DCS, where both transistors remain non-conducting at the same instant. Consequently, steady-state current flow is eliminated. However, power is still consumed during transitions due to charging and 19oolean19ingg effects, which is referred to as dynamic power and is given by:

$$P_{\text{dyn}} = C_{\text{OUT}} V_{\text{DD}} V_{\text{SWING}} f_{\text{CLK}} \quad (2.14)$$

where f_{CLK} is the clock signal frequency.

Realisation of conventional D-PFSCL gates

The complex logic function realization using conventional D-PFSCL gates requires cascading of gates. It is well known that direct cascading of D-PFSCL gates lead to erroneous output. To avoid this situation, it is suggested to use a static PFSCL inverter after D-PFSCL gate. Such a scheme introduces static power consumption, which contradicts the primary objective of reduced static power consumption. Alternatively, an intermittent STB is used that generates a delayed clock signal such that the evaluation phase in the next stage commences only after the completion of evaluation phase in the current stage [80]. The STB consists of two clocked cascaded inverters as illustrated in Fig. 2.12(a). The clock signal of the current stage (CLK_i) and the corresponding node Y voltage in the DCS of stage © forms the input to the STB. The output from the STB is then provided as the clock signal (CLK_{i+1}) to the subsequent stage (stage $i+1$). The symbolic representation of STB is drawn in Fig. 2.12(b). A complete realization of a 2:1 MUX using D-PFSCL NOR2 gates is illustrated in Fig. 2.13.

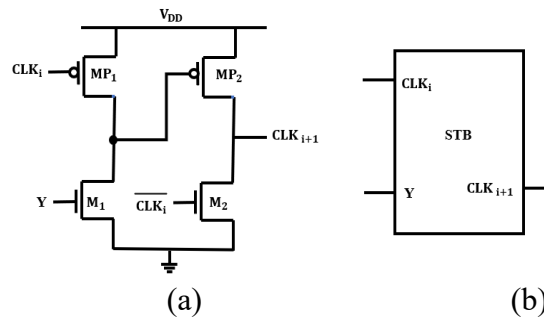


Fig. 2.12 STB [67, 80] (a) Schematic (b) Symbolic representation

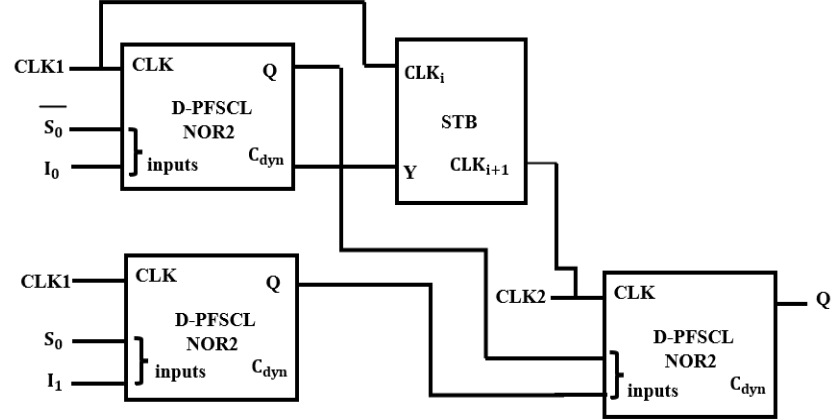


Fig. 2.13 Conventional D-PFSCL 2:1 MUX [67]

2.3.2 Multithreshold D-PFSCL FC realization

The conventional D-PFSCL gates has the limitation of implementing logic functions based on NOR/OR scheme which infers cascading of multiple D-PFSCL NOR/OR gates that degrades the overall performance. Thus, there is a need to introduce AND-OR functionality in D-PFSCL gates as most of the functions are expressed as sum of minterms. This issue is address by modifying the PDN of a D-PFSCL gate by employing multithreshold D-PFSCL gate. A generic multithreshold D-PFSCL FC gate consists of two triple-tail cells for realizing sum of two minterms as shown in Fig. 2.14. A low threshold voltage NMOS transistor, denoted as M_2 and M_4 is inserted between the source coupled transistor pair (M_1, M_{F1}), (M_3, M_{F2}) and power supply. For clear identification in the schematic, the transistors M_2, M_4 are represented using a bold symbol, while standard MOS symbols are used for the remaining transistors. The PMOS transistors $MP_1 - MP_4$ operate as precharge devices, and the output node, Q is wired-OR from the one of the output nodes Q_1/Q_2 and Q_3/Q_4 .

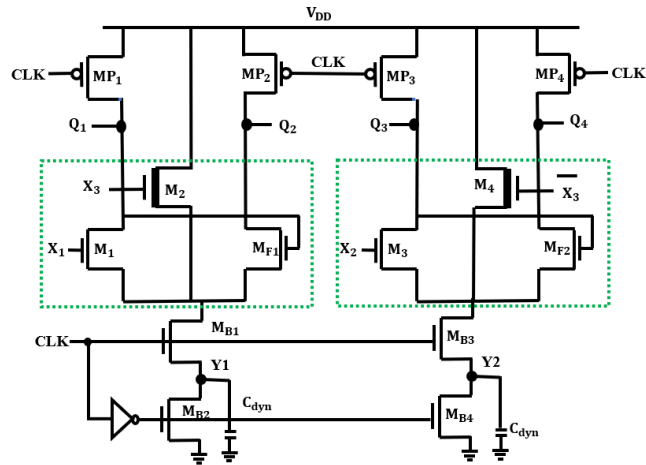


Fig. 2.14 Generic multithreshold D-PFSCL FC [81]

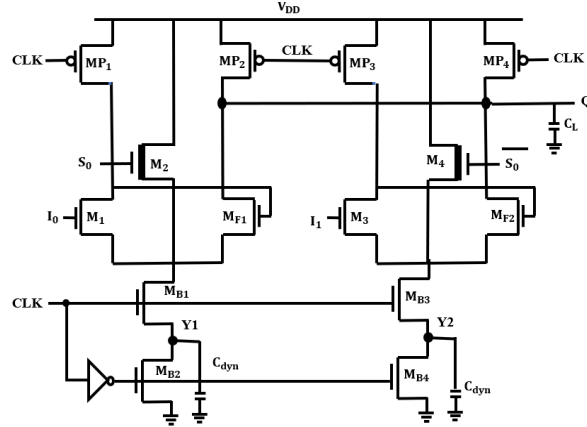


Fig. 2.15 Multithreshold D-PFSCL FC 2:1 MUX

The generic multithreshold D-PFSCL gate is configured to realize a 2:1 MUX with input lines I_0 , I_1 and select line S_0 as shown in Fig. 2.15. For the low value of the CLK signal, the output nodes are precharge to V_{DD} potential. Alternatively, for high value of CLK signal, the circuit enters the evaluation phase. When S_0 is at low logic level, the transistor M_4 turns ON and predominantly charges C_{dyn} as the threshold voltage of M_4 is lower than M_3 and M_{F2} . Consequently, I_1 is not reflected at the output. However, as M_2 is OFF, the voltage at input line I_0 gets reflected at the output node and the respective C_{dyn} is charged either through M_1 and M_{F1} . A similar behavior is observed when S_0 is at high logic level. The value of the C_{dyn} is calculated as done for conventional D-PFSCL gates. The multithreshold D-PFSCL scheme can be extended to design other logic functions. The mapping of inputs X_1 , X_2 , and the complemented input X_3 , along with the interconnection of outputs $Q_1 - Q_4$ for implementing different two input logic functions is summarized in Table 2.2.

Table 2.2 Realization of different logic functions

Logic function	Inputs	Mapping in D-PFSCL FC			Output
		X_3	X_1	X_2	
OR2	A, B	B	A	B	Q_2, Q_4
NOR2	A, B	B	A	B	Q_1, Q_3
NAND2	A, B	B	B	A	Q_1, Q_3
AND2	A, B	B	B	A	Q_2, Q_4
XOR2	A, B	B	A	A	Q_2, Q_3
XNOR2	A, B	B	A	A	Q_1, Q_4
2:1 MUX	S_0, I_0, I_1	S_0	I_0	I_1	Q_2, Q_4

TG based D-PFSCL gate

The multithreshold D-PFSCL gate offers the advantages of negligible static power consumption and allows any two-input logic function to be implemented within a

single stage. This approach reduces the need for intermediate STBs, and reduces both propagation delay and overall power consumption in comparison to conventional counterpart. However, for complex logic functions with more than two inputs, cascading multiple multithreshold D-PFSCL gates becomes necessary. Also, the use of low threshold voltage transistor adds an additional fabrication cost and makes its unattractive. Thus, to address these limitations and simultaneously supports higher fan-in, TGs are incorporated in the PDN of D-PFSCL gate [82]. A generalized structure of this realization is shown in Fig. 2.16. The required logic is realized using TGs, and the resulting output is fed to the D-PFSCL gate. The output of the TGs based 22oolean function, QT is connected to transistor M_1 of the conventional D-PFSCL inverter.

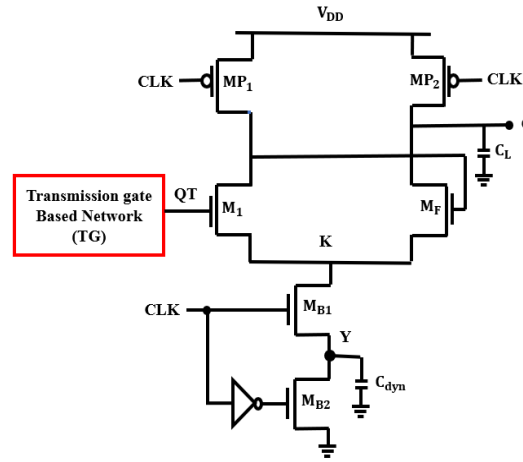


Fig. 2.16 Generic TG D-PFSCL gate [82]

The operation of TG based D-PFSCL gate is illustrated through a AND2 gate shown in Fig. 2.17. In the precharge interval, the output node Q is driven to the supply voltage V_{DD} via transistor MP_2 , while the dynamic capacitance C_{dyn} is simultaneously discharged to ground through M_{B2} . At the same time, the TG network processes the input logic, and the resulting signal QT is presented at the input of the D-PFSCL circuit.

During the evaluation phase, M_{B1} turns ON and based on the value of QT, either M_1 or M_F conducts. For the case when both the inputs A and B at low voltage level, TG1 is in high impedance state and TG2 conducts such that a low voltage level is obtained at QT. With low voltage as input, M_F conducts such that the output node is discharged from V_{DD} to $V_{DD} - V_{SWING}$. Similarly, for the case when both the input A and B are high, QT attains high voltage level. In this condition, M_1 conducts but the output node remains at high output voltage as no discharging path gets established. The value of the C_{dyn} is calculated as done for conventional D-PFSCL gates. The TG based D-PFSCL scheme can be extended to the other logic functions.

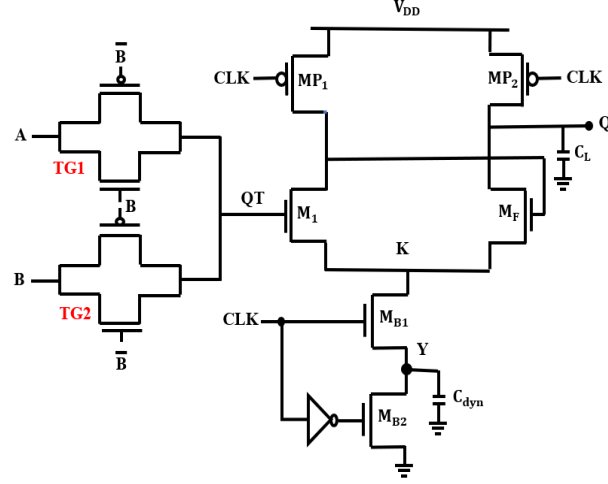


Fig. 2.17 TG D-PFSCL AND2 gate [82]

2.4 PFSCL tristate buffer/inverter

This section describes existing PFSCL tristate buffer/inverter and their use in design of D-latch. Available PFSCL tristate buffer/inverter designs can be broadly categorized into two configurations. In first configuration, a switch controlled by an Enable signal is added at the output of static PFSCL buffer/inverter to isolate the output node to exhibit high impedance state. The configuration is referred to as switch based PFSCL tristate buffer/inverter [83]. Alternatively, the second configuration utilizes the sleep transistor to realize the high impedance state, and is accordingly termed as sleep transistor based PFSCL tristate buffer/inverter [84]. Both categories, along with their respective variations, are discussed in the subsequent sections. All designs assume that the Enable signal has a full voltage swing.

2.4.1 Switch based PFSCL tristate buffer

A switch based PFSCL tristate buffer realization is illustrated in Fig. 2.18. In this realization, an additional PMOS transistor, M_6 is placed at the output of a conventional PFSCL buffer to enable tristate functionality. When the Enable signal is at low voltage level, M_6 remains ON, allowing the circuit to function as a regular buffer. However, when the Enable signal is high, M_6 turns OFF which effectively isolates the output node, Q to exhibit high impedance state.

Switch based PFSCL tristate buffer of Fig. 2.18 draws current when Enable signal assumes low or high logic voltage level and hence consumes power in both the states. Subsequently, several low-power variants of switch based tristate PFSCL buffer/inverter are proposed [83], all of which retain the output switch.

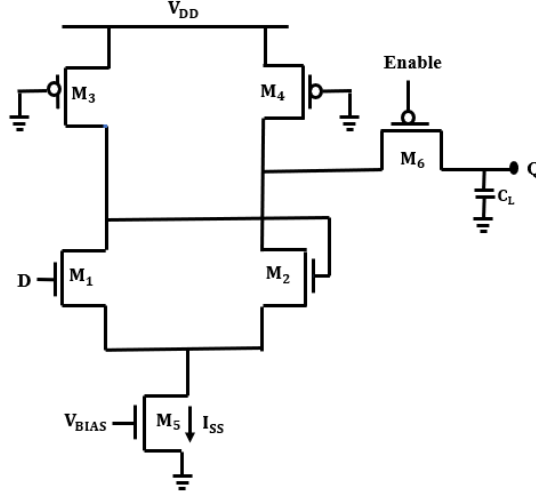


Fig. 2.18 Switch based PFSCCL tristate buffer [83]

The power consumption is minimized by inhibiting current flow during the high impedance state. This is achieved by altering either the load section or the current source section of the circuit. Based on these modifications, the resulting topologies are classified into two categories and are depicted in Fig. 2.20 [83]. The first category involves changes the load section (Topology 1), while the second focuses on modification in current source section (Topology 2-4).

The load section of PFSCCL tristate buffer is modified in Topology 1 (Fig. 2.19(a)) wherein the gates of load transistor M_3 and M_4 are controlled by Enable signal instead of permanently connecting these to ground terminal. Thus, offer Topology 1 operates as a conventional PFSCCL regular buffer and high impedance state for low and high values of Enable respectively.

In Topology 2, an additional PMOS transistor M_7 driven by Enable signal is inserted below the current source transistor in the conventional switch based PFSCCL tristate buffer as shown in Fig. 2.19(b). This adjustment allows the current to be controlled through the Enable signal. It is pertinent to mention that the inclusion of a PMOS transistor beneath the current source transistor in Topology 2 increases the required bias voltage (V_{BIAS}) so as to maintain the same current level (I_{SS}) as in a conventional PFSCCL buffer. To resolve this issue, Topology 3 repositions the two transistors M_5 and M_7 as shown in Fig. 2.19(c).

An alternative approach is to make the availability of bias voltage dependent on Enable signal. The suggested Topology 4 depicted in Fig. 2.19(d) uses a PMOS transistor M_8 and an NMOS transistor M_7 to manage the biasing of the current source transistor M_5 . A low Enable signal provides bias potential to the buffer while for high value of Enable, the buffer enters in high impedance by turning OFF the current source and ensure reduced power consumption.

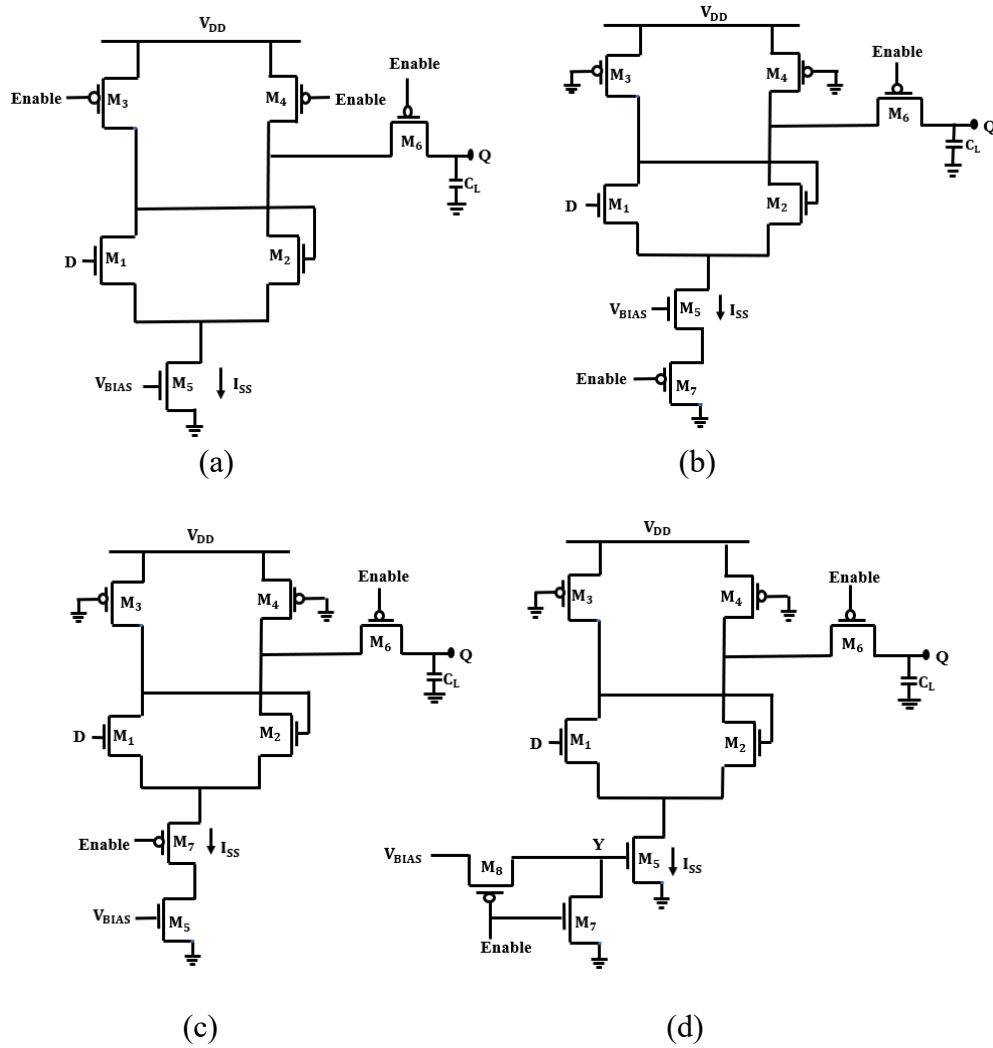


Fig. 2.19 Improved switch based PFSCSCL tristate buffer topologies [83] (a) Topology 1 (b) Topology 2 (c) Topology 3 (d) Topology 4

2.4.2 Sleep based PFSCSCL tristate buffer

This variant of PFSCSCL tristate buffer/inverter incorporates a sleep transistor connected in series with the power supply terminal of the conventional PFSCSCL tristate buffer/inverter. The corresponding schematic, depicted in Fig. 2.20 [84]. A low Enable signal allows the circuit to work as regular PFSCSCL buffer while the output node, Q transitions to a high impedance state for high value of the Enable signal. Unlike the conventional switch based configuration as shown in Fig. 2.18, the sleep transistor-based design is considered more power efficient, since no current is drawn through the circuit during the high impedance state [84].

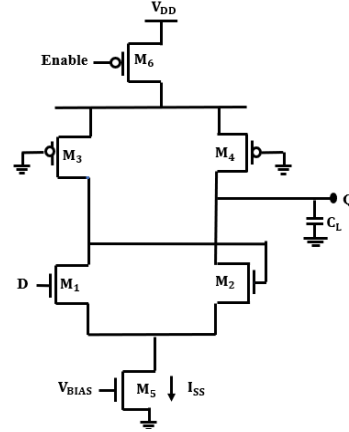
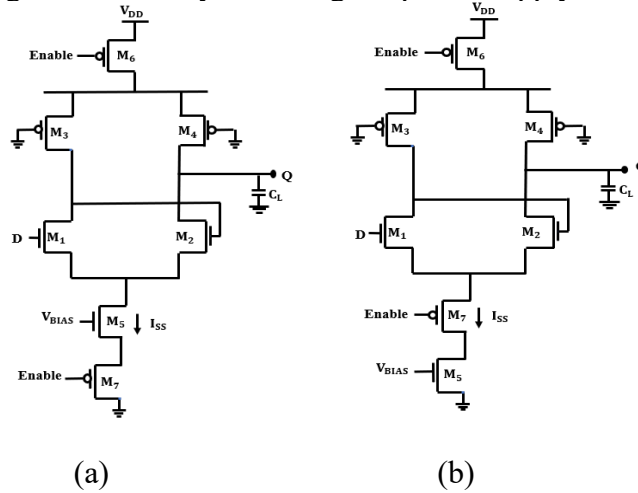


Fig. 2.20 Sleep transistor based PFSCSCL tristate buffer [84]

However, this topology fails to completely isolate output node, Q from the power supplies as the path from output node, Q to ground remain intact. The current source section is therefore modified to cutoff the path between output node, Q to ground when the circuit is disabled. The current source modification used in switch based tristate buffer Topologies 2-4 are used in sleep transistor based tristate buffer of Fig. 2.21 resulting in sleep transistor based tristate buffer Topologies 5-7. These topologies are depicted in Fig. 21(a)-(c). These topologies are power efficient as the current ceases to exist when the circuit is in high impedance state.

A closer analysis of Topologies 5-7 indicates that the primary role of transistor M_6 is to isolate the power supply from the output node in the high impedance state condition. This objective can alternatively be accomplished by directly controlling PMOS load transistors M_3 and M_4 through the Enable signal. This modification is applied to Topologies 5-7, resulting in three new Topologies 8, 9, and 10, as illustrated in Fig. 2.21 (d)-(f). In these derived Topologies, when the Enable signal is low, transistors M_3 and M_4 operate in the linear region, providing the necessary load to facilitate regular gate functionality. Conversely, when the Enable signal is high, these transistors enter the cutoff region, effectively removing the power supply connection.



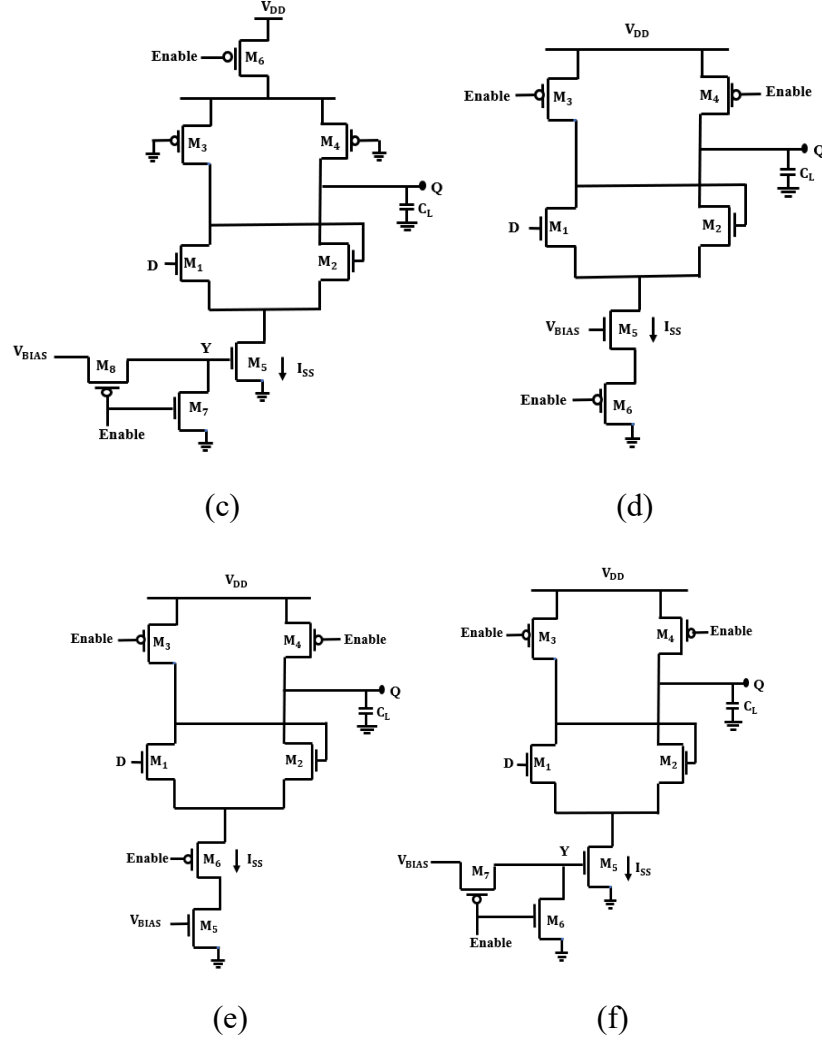


Fig. 2.21 Improved sleep transistor based PFSCSL tristate buffer topologies [84] (a) Topology 5 (b) Topology 6 (c) Topology 7 (d) Topology 8 (e) Topology 9 (f) Topology 10

2.4.3 D-latch design using sleep based PFSCSL tristate buffer

The D-latch design involves the cascade of two PFSCSL tristate buffers (PB1, PB2) controlled by CLK and $\overline{\text{CLK}}$ respectively as illustrated in Fig. 22(a) [84]. The output of PB2 is being fed back to retain the last output value. The schematic of the negative level D-latch using conventional sleep transistor based tristate buffer is shown in Fig. 22(b) wherein CLK and $\overline{\text{CLK}}$ signals are connected to Enable signal in the respective buffer. For a low value of CLK signal, PB1 operates as regular buffer such that the changes in input data, D are available at node, Q. The tristate buffer PB2 has no effect on output node, Q during this period as it operates in high impedance state. Conversely, for high value of CLK signal, PB1 enters into the high impedance state

while PB2 gets enabled and provides the last value of Q as the output.

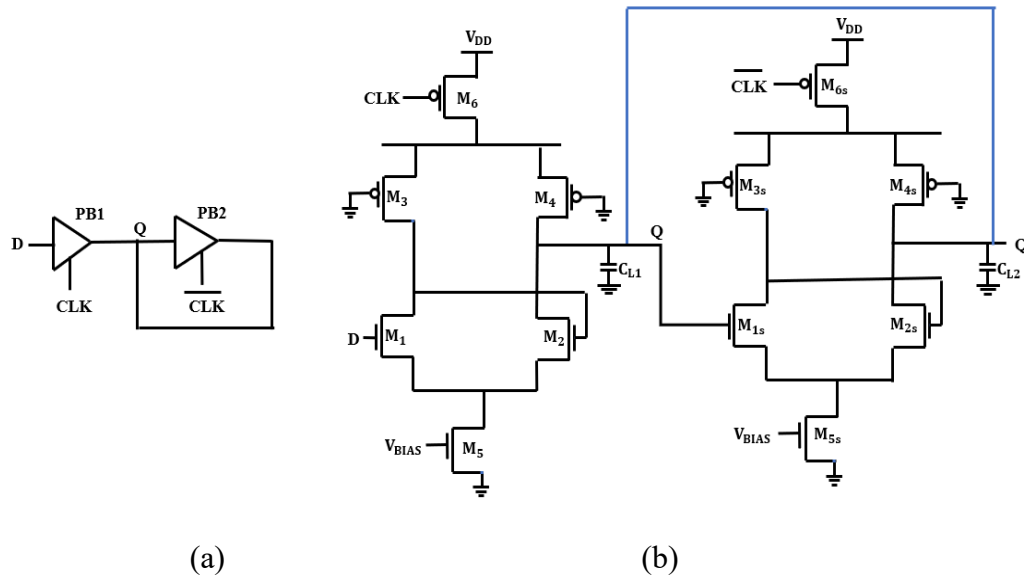


Fig. 2.22 Negative level D-latch based on sleep PFSCCL tristate buffer (a) Block diagram [84] (b) Schematic

2.5 Conclusion

This chapter presents basic concepts related PFSCCL gates. The operation and analysis of both static and dynamic PFSCCL gates are discussed. The improved form for both the categories of gates are presented. The approach to realize different logic function in static as well as dynamic gates is elaborated. Lastly, the PFSCCL tristate buffer/inverter is analyzed using various design approaches, including modifications in load and current source sections, with the objective of further improving power consumption and overall performance.

CHAPTER 3

IMPROVED STATIC PFSCCL GATES

3.1 Introduction

The existing PFSCCL realization schemes include either NOR/OR based realization or multistage cell-based realizations [37,66-69]. Both the schemes infer multistage realization with high gate count that mitigate high speed advantage of PFSCCL style. Thus, it is clear that improving the fan-in capability of PFSCCL gates is essential to fully utilize their advantages in mixed-signal applications. Recently, memristors are employed to provide AND-OR functionality in digital circuits due to the inherent features of smaller footprint and compatibility with CMOS technology [89-90]. The memristor are used in applications such as neural network [91-94], non-volatile static random-access memory [95-100], combinational circuits [101-105] analog signal processing and generation circuits etc. [106]. Therefore, in this chapter the use of memristors in realizing different logic functions in PFSCCL gates is explored and investigated. Two memristor based PFSCCL design schemes with the objective of enhancing the fan-in capability are worked upon.

The chapter describes memristor preliminaries, followed by two new static PFSCCL design schemes are presented, in which a memristor based network (MBN) is integrated with a PFSCCL inverter and a PFSCCL NOR/OR gate. These design schemes are referred to as proposed design scheme-1 and proposed design scheme-2, respectively. The operation of both proposed design schemes is elucidated and the corresponding voltage swing is calculated mathematically followed by simulations results for verifying functionality. The performance of the proposed gates is then compared with existing design schemes. Finally, the proposed design schemes are applied to different examples to illustrate their usefulness.

3.2 Memristor Preliminaries

Memristor is a two terminal passive element which stores the data in terms of resistance. It was postulated by Leon Chua in 1971 as a fourth circuit element, besides the other three elements namely, resistor, inductor and capacitor [107]. It remained a hypothetical component for substantial amount of time till William and his co-workers from HP labs introduced memristor physically in 2008 [108]. A memristor consists of an oxygen-deficient doped region, TiO_{2-x} , and a undoped TiO_2 region sandwiched between platinum (Pt) electrodes, as shown in Fig. 3.1(a). The doped region, with width W , behaves as a conductor, while the undoped region, with width $(D - W)$, acts as an insulator. The symbol of a memristor is illustrated in Fig. 3.1(b), where the shaded portion denotes the undoped region, and the unshaded portion represents the doped region.

When a high voltage level is applied at the doped side of the memristor, the oxygen deficiencies in the doped TiO_{2-x} layer repels toward the undoped TiO_2 layer. It increases width of TiO_{2-x} layer causing reduces the memristor resistance. In this condition, the memristor is in low resistance state (LRS) with corresponding resistance as R_{ON} . Conversely, if a low voltage level is applied across the memristor, oxygen gets attracted, resulting into the increased width of undoped TiO_2 layer. This condition is named as high resistance state (HRS) with resistance referred to as R_{OFF} . The behavior of memristor as per current flow is depicted in Fig 3.1I. Further, it is worth mentioning that if no voltage is placed across the memristor, the oxygen deficits region width remains unchanged and the memristor retains its former state. The relationship between the input voltage $V_m(t)$ applied across the memristor and the current ($i_m(t)$) passing through it is given by (3.1)

$$V_m(t) = M(t) i_m(t) \quad (3.1)$$

where $M(t)$ stands for memristance. The value of $M(t)$ [108] depends upon R_{ON} , R_{OFF} , W and D and is represented as, and is computed [108] as:

$$M(t) = R_{\text{ON}} \frac{W(t)}{D} + R_{\text{OFF}} \left(1 - \frac{W(t)}{D}\right) \quad (3.2)$$

In the above equation for the case when ($W = D$), the memristance is R_{ON} indicating that memristor is in LRS state. Similarly, if the undoped zone extends the entire length of the device (i.e., $W/D = 0$), the overall resistance is represented by R_{OFF} showing that memristor is in HRS state. This behavior of a memristor is gainfully used in basic digital gates design. In this work, their use is extended in the design of static PFSCCL gates with an aim to increase fan-in, as detailed in the next section.

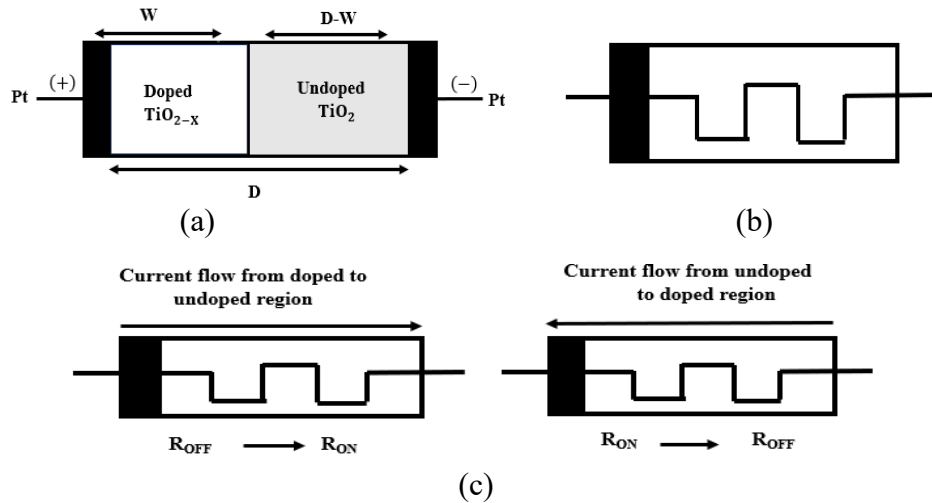


Fig. 3.1 Memristor (a) Physical structure (b) Symbolic representation (c) Switching behavior

3.3 Proposed memristor based static PFSCl designs

In this section, memristors are introduced in static PFSCl circuit design. Two design schemes are proposed, wherein the first scheme embeds MBN with a PFSCl inverter while the later uses with PFSCl NOR/ OR gate.

3.3.1 Proposed design scheme-1

The proposed design scheme-1 implements the logic function using MBN and feeds the corresponding intermediate output as an input to a PFSCl buffer/inverter. The design scheme is illustrated through a block diagram in Fig. 3.2. The schematic of proposed design scheme-1 PFSCl two-input NAND (NAND2) gate is shown in Fig. 3.3. Here, the MBN consist of two memristors T_1 and T_2 arranged in AND configuration. The inputs A and B are connected to T_1 and T_2 respectively and the intermediate output X_1 drives transistor M_1 of the PFSCl inverter. If the output is obtained from the other branch, then same circuit can behave as a 2-input AND (AND2) gate.

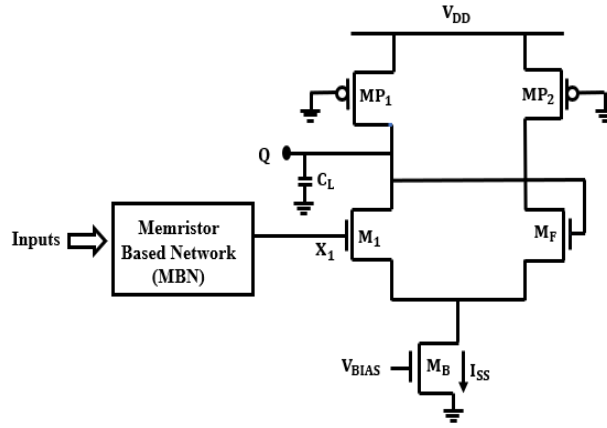


Fig. 3.2 Block diagram of Proposed design scheme-1 PFSCl gate

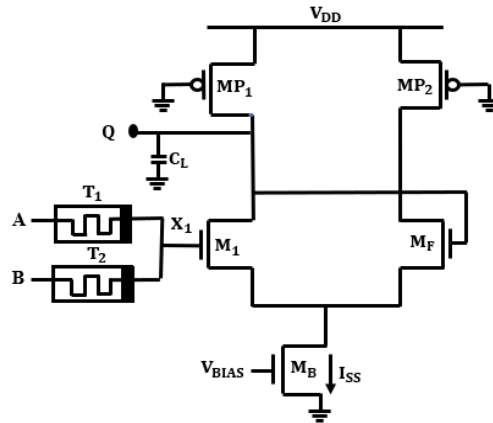


Fig. 3.3 Proposed design scheme-1 PFSCl NAND2 gate

Operation and analysis

The operation of PFSCCL gates realized using proposed design scheme-1 is illustrated through a NAND2 gate shown in Fig 3.3.

For the case when both the inputs A and B are at low voltage levels, no current flows through memristors T_1 and T_2 and the intermediate node X_1 attains a low voltage level. The low voltage at node, X_1 makes the bias current, I_{SS} to get steered through transistor M_F . Thus, no voltage drop occurs across MP_1 and a high output voltage level is obtained at output, Q. Alternatively, when input A is at low and B is at high voltage levels then there exists a current flow from T_2 to T_1 causing an increase in potential of X_1 . This high voltage at node X_1 causes steering of the bias current I_{SS} through M_1 such that there exists a potential drop across load transistor MP_1 and low voltage level is obtained at output, Q.

The analysis of the proposed design scheme-1 PFSCCL NAND2 gate is performed in terms V_{SWING} , A_V , and NM . The voltage swing is determined by first computing the voltage level at intermediate node X_1 for different input combinations and then determining the corresponding output of the gate. Further, the resistances of the memristor in HRS and LRS are assumed to be R_{OFF} and R_{ON} respectively. The high (V_{OH}) and low (V_{OL}) voltage levels for the inputs are assumed to be V_{DD} and $V_{DD} - V_{SWING}$ respectively. The voltages at different nodes are found by applying the voltage divider rule. Since, NAND2 gate has two inputs A and B, therefore a total of four combinations is possible and are analyzed below:

Case-1: Both the inputs A and B are at low (V_{OL}) voltage level.

Both the memristors T_1 and T_2 are driven by low input voltage so there is no current flow and the intermediate node X_1 is at V_{OL} . Further, for a low voltage level (V_{OL}) at the input of a PFSCCL inverter, the bias current I_{SS} is steered through M_F instead of M_1 and a high voltage level ($V_{OH} = V_{DD}$) is obtained at the output node, Q.

Case-2: Inputs A and B are low (V_{OL}) and high (V_{OH}) voltage level respectively.

In this condition, memristors T_1 and T_2 are in LRS and HRS respectively. This condition enables a current flow from T_2 to T_1 . The voltage at node X_1 is expressed as:

$$V(X_1) = \frac{(V_{DD} - V_{SWING}) R_{OFF} + V_{DD} R_{ON}}{R_{ON} + R_{OFF}} \quad (3.3)$$

As $R_{OFF} \gg R_{ON}$, (3.3) is reduced to

$$V(X_1) = V_{DD} - V_{SWING} \approx V_{OL} \quad (3.4)$$

Thus, a low voltage level is obtained at node X_1 , the bias current I_{SS} in the PFSCCL inverter is steered through M_F and a high output voltage ($V_{OH} = V_{DD}$) is obtained at the output, Q .

Case-3: Inputs A and B are high (V_{OH}) and low (V_{OL}) voltage level respectively.

The memristor T_1 and T_2 are in HRS and LRS state respectively. This condition enables a current flow from T_1 to T_2 . Thus, the voltage at node X_1 is expressed as:

$$V(X_1) = \frac{V_{DD} R_{OFF} + (V_{DD} - V_{SWING}) R_{ON}}{R_{ON} + R_{OFF}} \quad (3.5)$$

As $R_{OFF} \gg R_{ON}$, (3.5) reduced to

$$V(X_1) = V_{DD} - V_{SWING} \approx V_{OL} \quad (3.6)$$

Thus, a low voltage level is obtained at node X_1 , the bias current I_{SS} in the PFSCCL inverter is steered through M_F and a high output voltage ($V_{OH} = V_{DD}$) is obtained at the output, Q .

Case 4: Both the inputs A and B are at high (V_{OH}) voltage level.

Both the memristors T_1 and T_2 are driven by high input voltage so, there is no current flow and node X_1 is at V_{OH} . Thus, the bias current I_{SS} is steered through M_1 and a low voltage level ($V_{OL} = V_{DD} - V_{SWING}$) is obtained at the output node, Q of proposed design scheme-1 PFSCCL NAND2 gate. It is observed that the required functionality is achieved.

Further, the V_{SWING} , A_v and NM for the proposed design scheme-1 PFSCCL NAND2 gate is computed as:

$$V_{SWING} = V_{OH} - V_{OL} = V_{DD} - (V_{DD} - I_{SS} R_P) \quad (3.7)$$

$$V_{SWING} = I_{SS} R_P \quad (3.8)$$

$$A_v = \frac{g_{m,n} \frac{R_P}{2}}{1 - g_{m,n} \frac{R_P}{2}} \quad (3.9)$$

$$NM = \frac{V_{SWING}}{2} \left(1 - \frac{1}{A_v} \right) \quad (3.10)$$

where $g_{m,n} = \sqrt{\mu_n C_{ox} \frac{W_N I_{SS}}{L_N 2}}$, is the transconductance of the transistors M_1 - M_F , μ_n , W_N and L_N are the effective electron mobility, the effective channel width and length of the said transistors, respectively.

The proposed design scheme-1 is extended to the other basic functions realizations. The realization of a two-input OR (OR2) gate and exclusive-OR gate (XOR2) are

drawn in Fig. 3.4. The proposed design scheme-1 PFSCl OR2 gate is analysed to determine the voltage swing in a similar manner as done for the proposed design scheme-1 PFSCl NAND2 gate. The summary of node voltages for different input combinations for the proposed design scheme-1 PFSCl OR2 gate is listed in Table 3.1. Similarly, the concept is extended to the design of XOR2 gate as shown in Fig. 3.4(b). Table 3.2 summarize the logic levels at input intermediate node Y_1 , Y_2 , X_1 and the output node, Q .

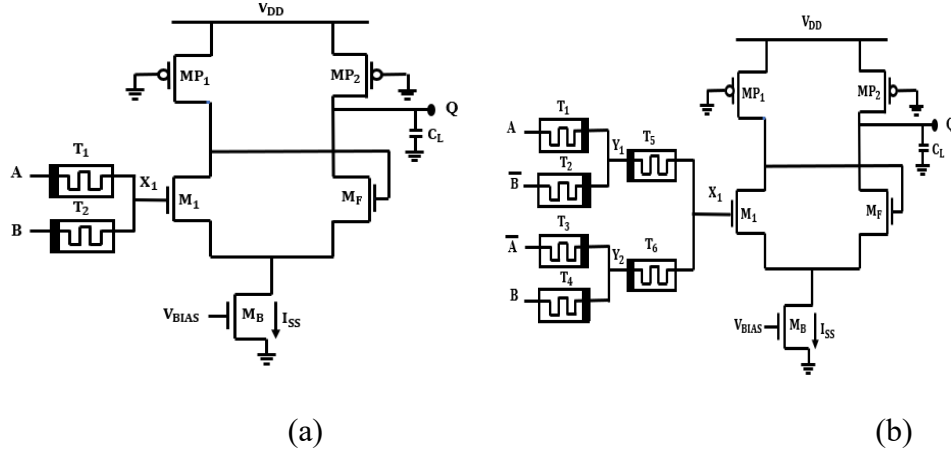


Fig. 3.4 Proposed design scheme-1 PFSCl gates (a) OR2 (b) XOR2

Table 3.1 Summary of node voltages in proposed design scheme-1 PFSCl OR2 gate

Inputs		Intermediate output	Output
A	B	X_1	Q
V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OH}	V_{OH}	V_{OH}
V_{OH}	V_{OL}	V_{OH}	V_{OH}
V_{OH}	V_{OH}	V_{OH}	V_{OH}

where $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - V_{SWING}$

Table 3.2 Summary of node voltages in proposed design scheme-1 PFSCl XOR2 gate

Inputs		Intermediate outputs			Output
A	B	Y_1	Y_2	X_1	Q
V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OH}	V_{OH}
V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OH}
V_{OH}	V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}

where $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - V_{SWING}$

3.3.2 Simulation section

The functionality of the gates namely NAND2 gate, OR2 gate, and XOR2 gate, based on proposed design scheme-1 is examined and their performance is compared with NOR/OR, FC, multithreshold FC based counterparts. All the simulations are carried out in LT spice by using PTM 90nm CMOS technology parameters with a power supply (V_{DD}), bias current (I_{SS}), voltage swing (V_{SWING}) and load capacitance (C_L) of 1.1V, 100 μ A, 400mV, 50fF respectively and memristor model suggested in [109]. The layouts are drawn in Microwind.

To elucidate the functionality of the proposed design scheme-1 PFSCS XOR2 gate, the timing waveform is shown in Fig. 3.5. It is observed that when both the inputs are at same logic level (either high or low) then a low output voltage level ($V_{OL} = V_{DD} - V_{SWING} = 1.1V - 0.4V = 0.7V$) is obtained. However, when both the inputs have different voltage levels, then a high voltage ($V_{OH} = V_{DD} = 1.1V$) is obtained at the output node, Q.

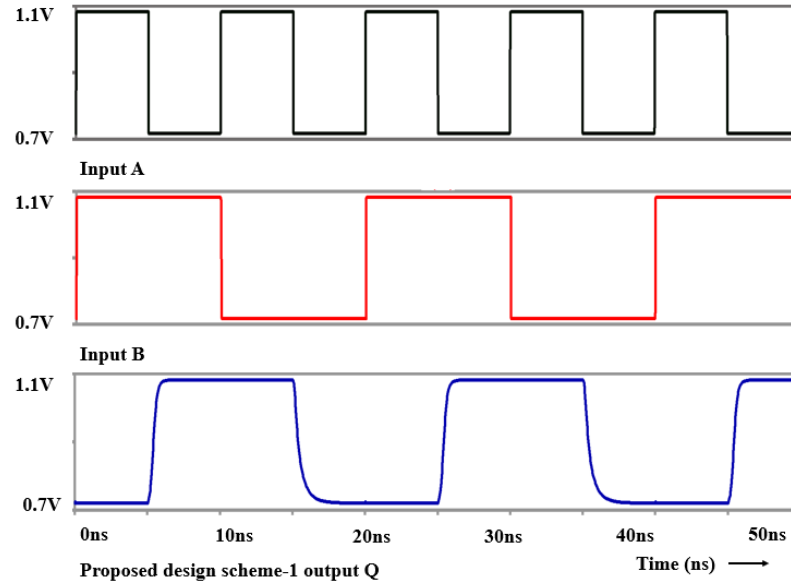


Fig. 3.5 Timing waveform of proposed design scheme-1 PFSCS XOR2 gate

The layout of proposed design scheme-1 based OR2, NAND2 and XOR2 are drawn using Microwind and are depicted in Fig. 3.6. The corresponding areas are calculated in Table 3.3. The performance of these gates are compared with the existing counterparts in terms of power consumption, propagation delay, power delay product (PDP), gate count, and area. The results are summarized in Table 3.3 The following observations are made:

1. The performance of proposed design scheme-1 NAND2 and OR2 gates is similar to NOR/OR based counterparts as the logic is implemented using a single PFSCS gate.

2. The proposed design scheme-1 XOR2 gate shows a maximum improvement of 66.66 %, 75.75 % in power consumption and PDP values respectively over existing counterparts. This improvement is due to the reduction in gate count to a single gate, compared to the three gates required in the conventional NOR/OR design scheme.
3. The proposed design scheme-1 XOR2 gate show a maximum improvement of 27.27 % improvement in propagation delay with respect to their existing counterparts, thus giving an edge for implementation large fan-in gates.
4. The area of gates based on proposed design scheme-1 is smaller in comparison to existing counterparts. A maximum area reduction of 94.85 % is observed in comparison to existing counterparts of PFSCSCL XOR2 gate design.

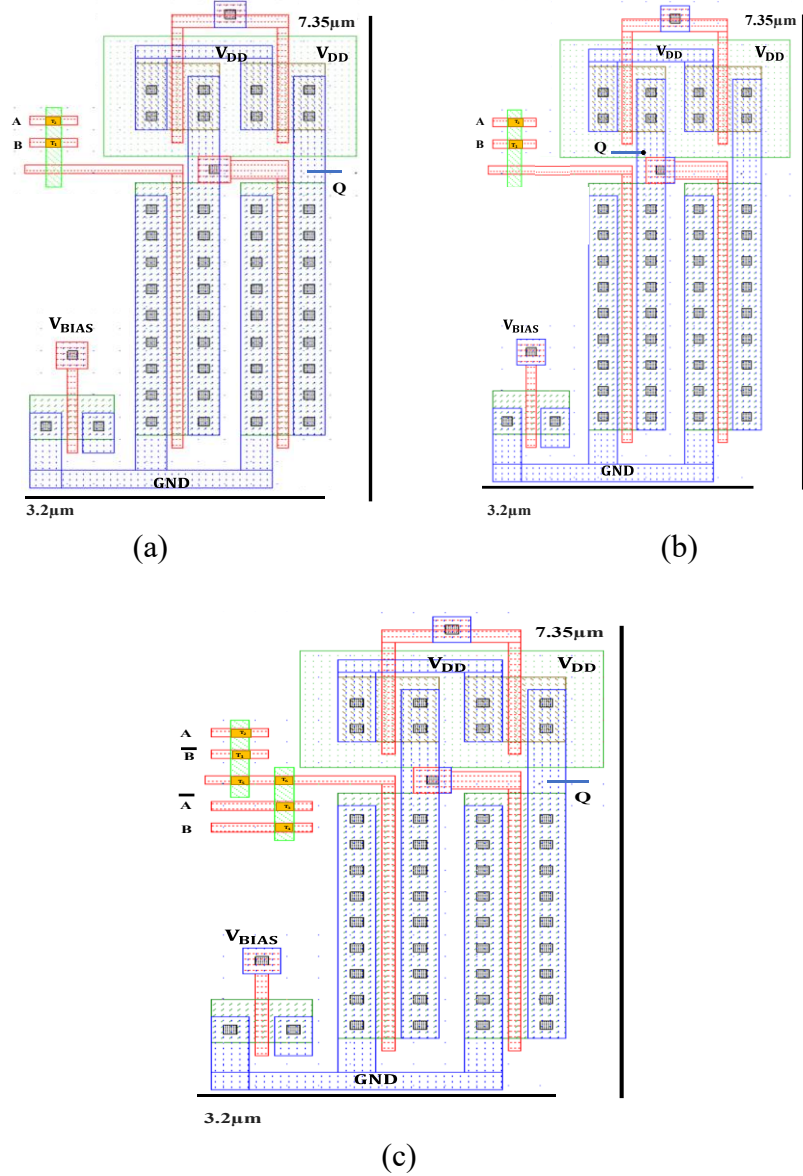


Fig. 3.6 Layout of proposed design scheme-1 PFSCSCL gates (a) OR2 (b) NAND2 (c) XOR2

Table 3.3 Performance comparison of different logic gates

Logic gate	Parameter Scheme	Power consumption (μW)	Propagation delay (ps)	PDP (fJ)	Gate count	Area (μm^2)
OR2	NOR/OR	110	388	42.62	1	40
	FC	110	420	46.20	1	457
	Multithreshold FC	110	420	46.20	1	86.8
	Proposed design scheme-1	110	396	43.56	1	23.52
NAND2	NOR/OR	110	392	43.10	1	40
	FC	110	420	46.20	1	457
	Multithreshold FC	110	420	46.20	1	86.8
	Proposed design scheme-1	110	396	43.56	1	23.52
XOR2	NOR/OR	330	550	181.50	3	114
	FC	110	420	46.20	1	457
	Multithreshold FC	110	420	46.20	1	86.8
	Proposed design scheme-1	110	400	44	1	23.52

3.3.3 Proposed design scheme-2

The proposed design scheme-2 is based on incorporating the advantages of PFSCCL NOR/OR gate with MBN. In this design, the minterms defined in a logic function are realized using MBN and the corresponding intermediate outputs are then fed to the input transistors of a PFSCCL NOR/OR gate as depicted in Fig. 3.7.

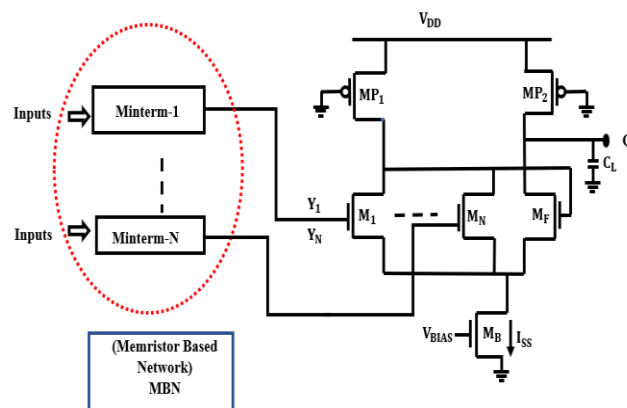


Fig. 3.7 Block diagram of proposed design scheme-2 PFSCCL gate

Operation and analysis

The operation of the proposed design scheme-2 PFSCCL gates is illustrated through a XOR2 gate shown in Fig. 3.8. The two minterms AB and $\bar{A}\bar{B}$ are realized by memristors (T_1, T_2) and (T_3, T_4) respectively. The corresponding outputs Y_1, Y_2 are further fed to the input transistors (M_1, M_2) of the PFSCCL OR2 gate.

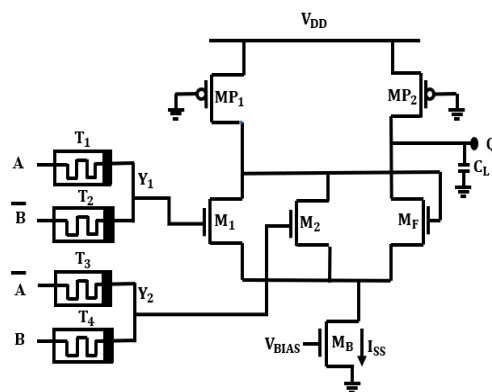


Fig. 3.8 Proposed design scheme-2 PFSCl XOR2 gate

The analysis of the proposed design scheme-2 PFSCl NAND2 gate is performed in terms V_{SWING} , A_v , and NM. A similar procedure as followed for the proposed design scheme-1 is performed to find voltage levels for XOR2 gate at different nodes for all possible input combinations. The procedure includes the computation of voltage levels at intermediate nodes Y_1 and Y_2 first and then determining the corresponding output of the gate for different input combinations. Further, the resistances of the memristor in high resistance state (HRS) and low resistance state (LRS) are assumed to be R_{OFF} and R_{ON} respectively. The voltages at different nodes is found by applying the voltage divider rule. The analysis for all the four input combinations is presented below:

Case-1: Both the inputs A and B are at low (V_{OL}) voltage level.

In this condition, the memristors T_1 and T_2 are driven by low and high voltage levels respectively therefore, there exists a current flow from T_2 to T_1 such that T_1 is in LRS state while T_2 attains HRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{(V_{DD} - V_{SWING}) R_{OFF} + V_{DD} R_{ON}}{R_{OFF} + R_{ON}} \quad (3.11)$$

As $R_{OFF} \gg R_{ON}$, (3.11) is reduced to

$$V(Y_1) = V_{DD} - V_{SWING} \approx V_{OL} \quad (3.12)$$

Since the memristors T_3 and T_4 are driven by high and low voltage levels respectively, therefore current flow through T_3 to T_4 . Thus, memristor T_3 is in HRS state while T_4 attain LRS state. The $V(Y_2)$ is expressed as:

$$V(Y_2) = \frac{V_{DD}R_{ON} + (V_{DD} - V_{SWING})R_{OFF}}{R_{ON} + R_{OFF}} \quad (3.13)$$

As $R_{OFF} \gg R_{ON}$, (3.13) is reduced to

$$V(Y_2) = V_{DD} - V_{SWING} \approx V_{OL} \quad (3.14)$$

The corresponding outputs Y_1, Y_2 are further fed to the input transistors (M_1, M_2) of the PFSCS OR2 gate. As both Y_1, Y_2 are at low voltage levels therefore, the bias current, I_{SS} is steered through M_F and a low voltage level ($V_{OL} = V_{DD} - V_{SWING}$) is obtained at the output node, Q.

Case-2: Inputs A and B are at low (V_{OL}) and high (V_{OH}) voltage levels respectively.

The memristors T_1 and T_2 are driven by low voltage level thus, there is no current flow across them and node, Y_1 attains a low voltage level (V_{OL}). Similarly, the memristors T_3 and T_4 are driven by high input voltage level so there is no current flow and a high voltage level (V_{OH}) is observed at node, Y_2 .

The corresponding intermediate outputs Y_1, Y_2 are further fed to the input transistors (M_1, M_2) of the PFSCS OR2 gate. The bias current I_{SS} is steered through M_2 in this condition. Thus, a high voltage level ($V_{OH} = V_{DD}$) is obtained at the output node, Q.

Case-3: Inputs A and B are at high (V_{OH}) and low (V_{OL}) voltage level respectively.

Both the memristors T_1 and T_2 are driven by high voltage level therefore, no current flow across them and the intermediate node Y_1 attains a high voltage level (V_{OH}). Similarly, the memristors T_3 and T_4 are driven by low voltage level so there is no current flow and node Y_2 is at low voltage level (V_{OL}).

The corresponding outputs Y_1, Y_2 are further fed to the input transistors (M_1, M_2) of the PFSCS OR2 gate, the bias current I_{SS} will steer through M_1 . Thus, a high voltage level ($V_{OH} = V_{DD}$) is obtained at the output node, Q.

Case-4: Inputs A and B are at high (V_{OH}) voltage level.

The memristors T_1 and T_2 are driven by high and low voltage levels respectively therefore there exists a current flow from T_1 to T_2 such that T_1 is in HRS state while T_2 attains LRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{V_{DD}R_{ON} + (V_{DD} - V_{SWING})R_{OFF}}{R_{OFF} + R_{ON}} \quad (3.15)$$

As $R_{OFF} \gg R_{ON}$, (3.15) is reduced to

$$V(Y_1) = V_{DD} - V_{SWING} = V_{OL} \quad (3.16)$$

Since the memristors T_3 and T_4 are driven by low and high voltage levels respectively, there exists a current flow through T_4 to T_3 . Thus, memristor T_3 is in LRS state while T_4 attain HRS state. Thus, $V(Y_2)$ is expressed as:

$$V(Y_2) = \frac{(V_{DD} - V_{SWING}) R_{OFF} + V_{DD} R_{ON}}{R_{ON} + R_{OFF}} \quad (3.17)$$

As $R_{OFF} \gg R_{ON}$, (3.17) is reduced to

$$V(Y_2) = V_{DD} - V_{SWING} = V_{OL} \quad (3.18)$$

The corresponding outputs Y_1, Y_2 are further fed to the input transistors (M_1, M_2) of the PFSCSCL OR2 gate. As low voltage level is obtained at Y_1, Y_2 therefore the bias current I_{SS} flows through M_F . Thus, a low voltage level ($V_{OL} = V_{DD} - V_{SWING}$) is obtained at the output node, Q . It is observed that the required functionality is achieved. The A_v and NM for the proposed design scheme-2 gates are computed as:

$$A_v = \frac{g_{m,n} \frac{R_p}{2}}{1 - g_{m,n} \frac{R_p}{2}} \quad (3.19)$$

$$NM = \frac{V_{SWING}}{2} \left(1 - \frac{1}{A_v} \right) \quad (3.20)$$

where $g_{m,n} = \sqrt{\mu_n C_{ox} \frac{W_N I_{SS}}{L_N \cdot 2}}$, is the transconductance of the transistors M_1 - M_F , μ_n , W_N and L_N are the effective electron mobility, the effective channel width and length of the said transistors, respectively.

Realization of logic gates

The proposed design scheme-2 is extended to realize 2:1 MUX. The realization of a 2:1 MUX with inputs lines I_0 and I_1 and select line S_0 , is drawn in Fig. 3.9. In the proposed design scheme-2 PFSCSCL 2:1 MUX, the memristors (T_1, T_2), (T_3, T_4) are arranged for AND functionality and the corresponding intermediate outputs for Y_1, Y_2 are fed to PFSCSCL OR gate.

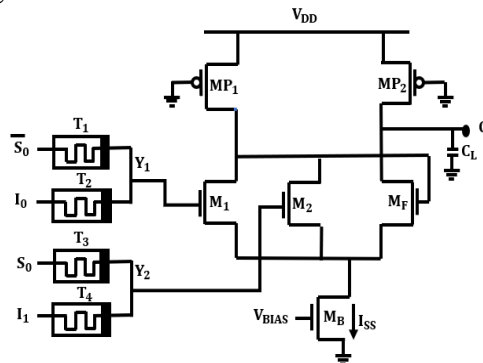


Fig. 3.9 Proposed design scheme-2 PFSCSCL 2:1 MUX

The same procedure as elaborated is followed to analyze the proposed design scheme-2 2:1 MUX. A summary of node voltage levels at different nodes is listed in Table 3.4.

Table 3. 4 Summary of node voltages in proposed design scheme-2 PFSCSCL 2:1 MUX

Inputs			Intermediate		Output
S_0	I_0	I_1	Y_1	Y_2	Q
V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OL}	V_{OH}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OH}
V_{OL}	V_{OH}	V_{OH}	V_{OH}	V_{OL}	V_{OH}
V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OH}
V_{OH}	V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OH}	V_{OH}	V_{OH}	V_{OL}	V_{OH}	V_{OH}

where $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - V_{SWING}$

3.3.4 Simulation section

The functionality of the proposed design scheme-2 PFSCSCL XOR2 gate is verified and the performance is compared with NOR/OR, FC, multithreshold FC design schemes. The same simulation environment as considered for proposed design scheme-1 is used for the proposed design scheme-2 PFSCSCL gates.

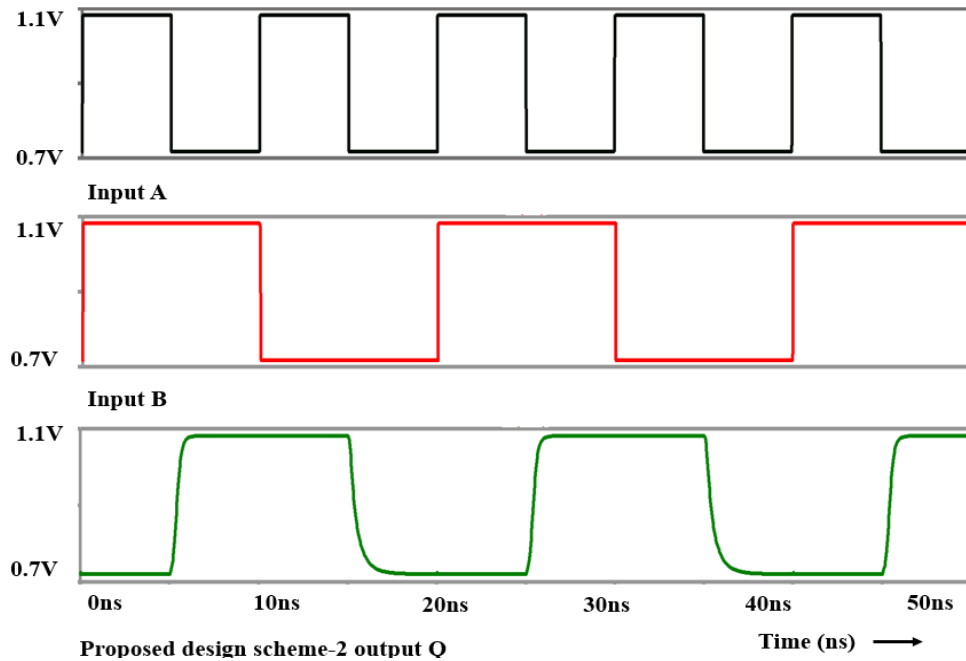


Fig. 3.10 Timing waveform of the proposed design scheme-2 PFSCSCL XOR2 gate

The timing waveform of proposed design scheme-2 XOR2 gate is shown in Fig. 3.10. It is observed that when both the inputs are at same logic level (either high or low) then the proposed design scheme-2 PFSCCL XOR2 gate produce a low output voltage ($V_{OL} = V_{DD} - V_{SWING} = 0.7V$). However, when the inputs have different voltage levels then a high voltage ($V_{OH} = V_{DD} = 1.1V$) is obtained at the output node, Q. Thus, the proposed design scheme-2 PFSCCL XOR2 gate conforms to the correct functionality.

The layout of proposed design scheme-2 based XOR2 is drawn using Microwind and are depicted in Fig. 3.11. The XOR2 performance is evaluated against existing designs by considering power consumption, propagation delay, PDP, gate count, and area. Table 3.5 presents the obtained results, based on which the following observations are noted:

1. The proposed design scheme-2 PFSCCL XOR2 gate shows maximum improvement of 66.66 %, 76 % in power and PDP values respectively over existing counterparts. This improvement is attributed to the low gate count that reduces the propagation delay and overall current that saves power consumption.
2. The proposed design scheme-2 PFSCCL XOR2 gate shows a maximum improvement of 28 % in propagation delay with respect to their existing counterparts, thus giving an edge for implementation large fan-in gates.
3. The proposed design scheme-2 XOR2 gate occupy the lowest area. A maximum area reduction of 92.76 % is observed in comparison to PFSCCL FC XOR2 gate.

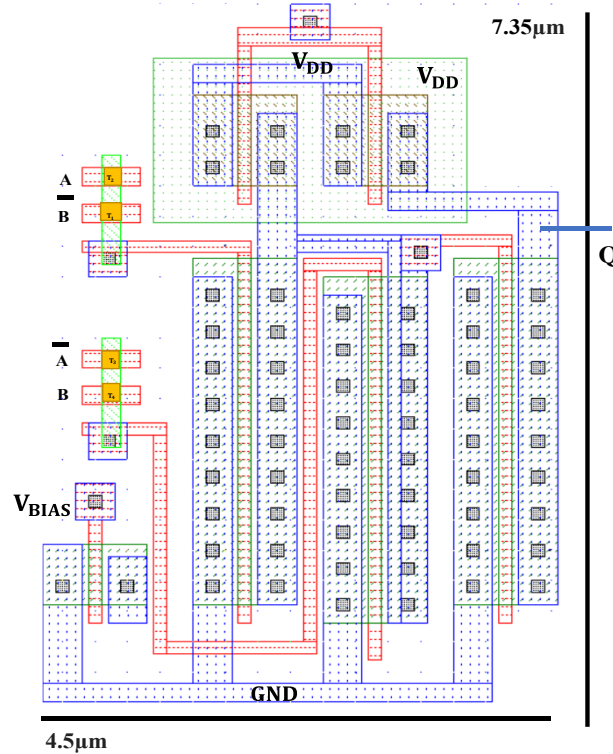


Fig. 3.11 Layout of proposed design scheme-2 PFSCCL XOR2 gate

Table 3.5 Performance comparison of XOR2 gate

Scheme Parameter	NOR /OR	FC	Multithreshold FC	Proposed design scheme- 2
Power consumption (μW)	330	110	110	110
Propagation delay (ps)	550	420	420	396
PDP (fJ)	181.5	46.20	46.20	43.56
Gate count	3	1	1	1
Area (μm^2)	114	457	86.8	33.07

3.4 Overall performance comparison

In this section, the performance of different gates designed using the proposed design schemes (1 and 2) and existing NOR/OR, FC, multithreshold FC based realizations compared. All the simulations are carried out in LT spice by using PTM 90 nm CMOS technology parameters and with a V_{DD} , I_{SS} , V_{SWING} and C_L of 1.1V, 100 μA , 400mV, 50fF respectively. Memristor model suggested in [109] is used and the layouts are drawn in Microwind. The impact of process variations is also studied. The performance is compared in terms of power consumption, propagation delay, PDP, gate count, and area. The overall results are summarized in Table 3.6 and the following observations are made:

1. The conventional NOR/OR realization is best suited to realize OR2 and NAND2 gates as they outperform in comparison to the existing FC, multithreshold FC realizations as well as proposed design scheme-1 realization. These gates cannot be realized using proposed design scheme-2 as there are no minterms.
2. For the functions expressed as sum-of-minterms, the results indicate that conventional NOR/OR realizations exhibit the largest propagation delay, power consumption and PDP values which is consequence of high gate count and multiple stages.
3. Out of the two proposed design schemes, it is observed that proposed design scheme-2 XOR2 gate has lower propagation delay than proposed design scheme-1 XOR2 gate for same value of power consumption.
4. The proposed design scheme-2 PFSCl XOR2 gate show maximum improvements of 28 %, 66.66 %, 76 % in propagation delay, power consumption and PDP values respectively over existing counterparts. This improvement is attributed to the low gate count that reduces the propagation delay and overall current that saves power consumption.
5. In terms of area, the proposed design schemes occupies the lesser area in comparison to existing counterparts due to the fabrication advantage wherein memristors are integrated on top of a CMOS substrate using postprocessing e.g. nanoimprint lithography (NIL), a process that does not disturb the CMOS circuitry underneath [110], wafer scale integration [111]. A maximum area reduction of 94.85 %, 92.76 % is observed with proposed design scheme-1 and proposed design scheme-

2 respectively in comparison to conventional PFSCS FC XOR2 gate.

Table 3.6 Performance comparison of different logic gates using different design schemes

Logic gate	Scheme Parameter	NOR /OR	FC	Multithresh old FC	Proposed design schemes	
					Scheme- 1	Scheme- 2
OR2	Power consumption (μW)	110	110	110	110	--
	Propagation delay (ps)	392	420	420	396	
	PDP (fJ)	43.12	46.20	46.20	43.56	
	Gate count	1	1	1	1	
	Area (μm^2)	40	457	86.8	23.52	
NAND2	Power consumption (μW)	110	110	110	110	--
	Propagation delay (ps)	388	420	420	396	
	PDP (fJ)	42.68	46.20	46.20	43.56	
	Gate count	1	1	1	1	
	Area (μm^2)	40	457	86.8	23.52	
XOR2	Power consumption (μW)	330	110	110	110	110
	Propagation delay (ps)	550	420	420	400	396
	PDP (fJ)	181.5	46.20	46.20	44	43.56
	Gate count	3	1	1	1	1
	Area (μm^2)	114	457	86.8	23.52	33.07

Further, the impact of process variations on all the existing and proposed design schemes for XOR2 gate is studied through Monte Carlo simulations and corner analysis. For Monte Carlo analysis, simulations are performed by varying the threshold voltage of MOS transistors with 5 % tolerance for 1000 runs. The timing waveforms of the proposed design scheme-2 XOR2 gate for 1000 runs shown in Fig.

3.12. The findings for mean (μ), standard deviation (SD) (σ) and variability (σ/μ) in propagation delay for proposed and existing design schemes for PFSCSCL XOR2 gate is placed in Table 3.7. The proposed design scheme-2 XOR2 gate exhibits least variation of 1.1 %.

The five standard process corners: Typical-Typical (TT), Fast-Fast (FF), Slow-Slow (SS), Slow-Fast (SF), and Fast-Slow (FS) for PTM 90 nm CMOS technology node are considered. Each corner represents different behaviour of NMOS and PMOS transistors, as well as supply voltage and temperature range [7]. The obtained results at each corner are summarized in Table 3.8. The process corner analysis confirms that all the existing and proposed design schemes for PFSCSCL XOR2 gate function correctly across all corners, indicating their robustness and reliability under diverse operating conditions. The best-case performance is obtained at FF design corner, and the worst-case performance is obtained at SS corner in all the proposed gates. It is found that the propagation delay, power consumption and PDP of the proposed design scheme-1 PFSCSCL XOR2 gate varies by a factor of 0.82, 0.81 and 1 respectively between the best and the worst cases whereas the corresponding variation for the proposed design scheme-2 PFSCSCL XOR2 gate is 0.79, 0.81 and 0.97 respectively. Overall proposed design scheme-2 can be chosen as an optimum design option due to low PDP, propagation delay and sensitivity to variations.

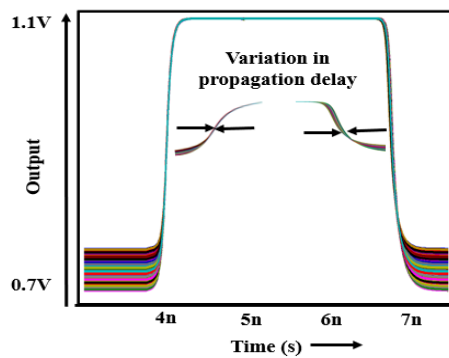


Fig. 3.12 Monte Carlo analysis of proposed design scheme-2 PFSCSCL XOR gate

Table 3.7 Monte Carlo results for PFSCSCLXOR2 gate

Scheme \ Parameter	Propagation delay (ps)		
	Mean (μ) (ps)	SD (σ) (ps)	Variability (%)
NOR/OR	555	17.5	3.2
FC	428	12.2	2.8
Multithreshold FC	428	12.2	2.8
Proposed design scheme-1	408	9.8	2.4
Proposed design scheme-2	402	4.4	1.1

Table 3.8 Process corner analysis for PFSCL XOR2 gate

Corner Scheme	TT	FF	SS	FS	SF
Power consumption (μW)					
NOR/OR	330	363	297	330	330
FC	110	121	99	110	110
Multithreshold FC	110	121	99	110	110
Proposed design scheme-1	110	121	99	110	110
Proposed design scheme-2	110	121	99	110	110
Propagation delay (ps)					
NOR/OR	550	498	612	558	588
FC	420	378	468	431	453
Multithreshold FC	420	378	468	431	453
Proposed design scheme-1	400	365	445	405	425
Proposed design scheme-2	396	361	454	401	426
PDP (fJ)					
NOR/OR	181.5	180.74	181.77	184.14	194.04
FC	46.2	45.74	46.33	47.41	49.83
Multithreshold FC	46.2	45.74	46.33	47.41	49.83
Proposed design scheme-1	44	44.17	44.06	44.55	46.75
Proposed design scheme-2	43.56	43.68	44.95	44.11	46.86

3.5 Design examples

To show the effectiveness of the proposed design schemes, a 3-bit parity generator (PG) and 4-bit carry skip adder (CSA) are considered.

Design example-1

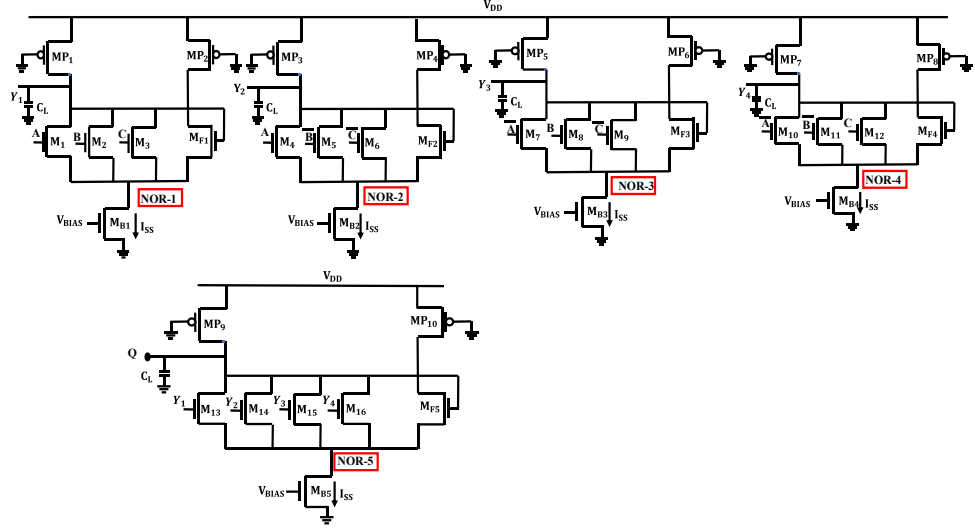
In a digital communication system, a PG is an important component for detecting errors during data transmission [112-113]. Parity bits are extra bits appended to binary data input in order to ensure that the total number of 1's in the binary data input is either even or odd. The functionality of a 3-bit parity generator is expressed as follows:

$$PG = A \oplus B \oplus C \quad (3.21)$$

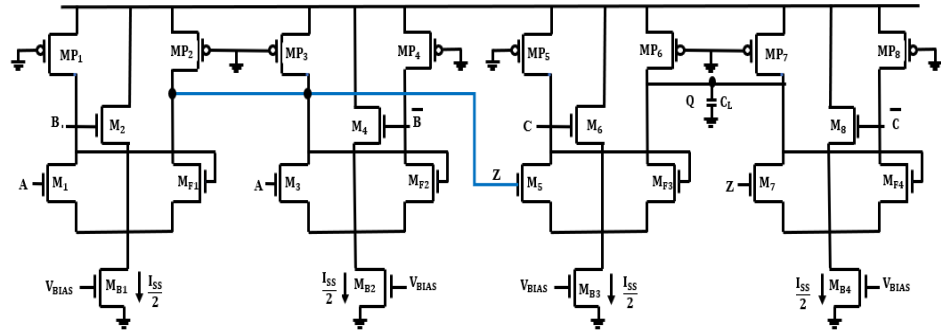
Based on the expression, it is clear that 3-bit PG requires 3-input XOR gate. The realization of the PG with inputs A, B, C in the existing NOR/OR, FC, multithreshold FC, QC and the proposed design schemes are drawn in Fig. 3.13. The NOR/OR PFSCL PG design is realized by following the Boolean expression given as:

$$Q = \overline{\overline{A + B + C}} + \overline{\overline{A + \overline{B} + \overline{C}}} + \overline{\overline{\overline{A} + B + \overline{C}}} + \overline{\overline{\overline{A} + \overline{B} + C}} \quad (3.22)$$

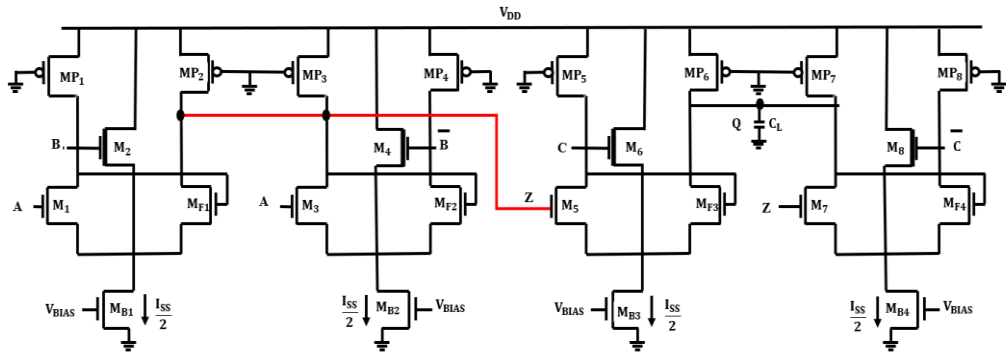
The individual maxterms are realized by 3-input PFSCSCL NOR gate (NOR-1, NOR-2, NOR-3, NOR-4) and their corresponding outputs ($Y_1 - Y_4$) are further fed to a 4-input NOR/OR PFSCSCL gate (NOR-5) as illustrated in Fig 3.13(a).



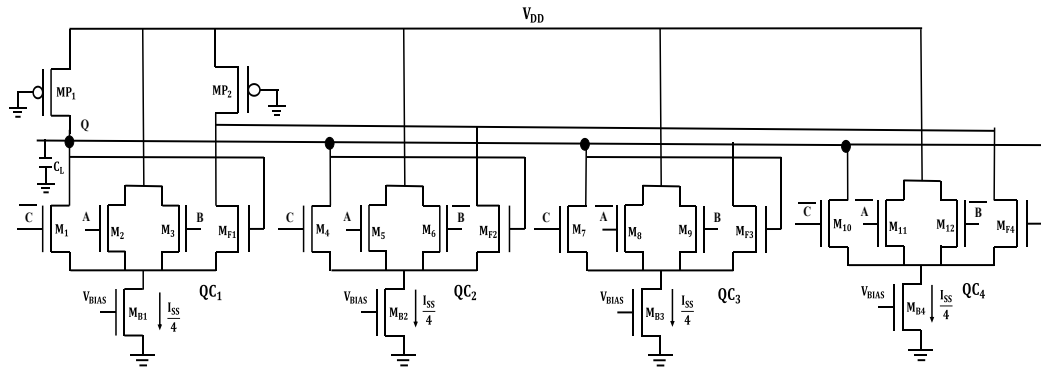
(a)



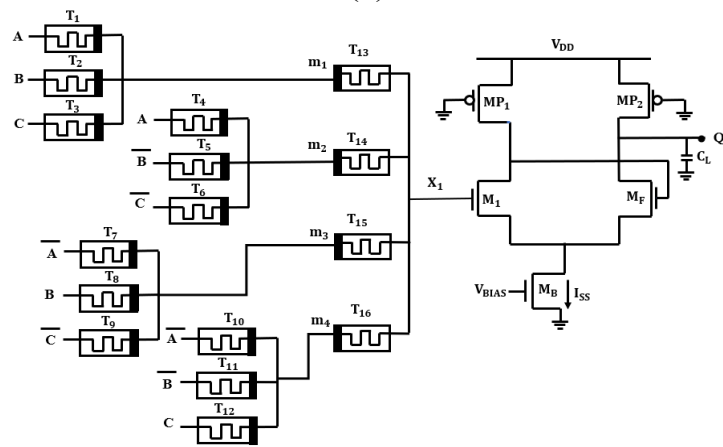
(b)



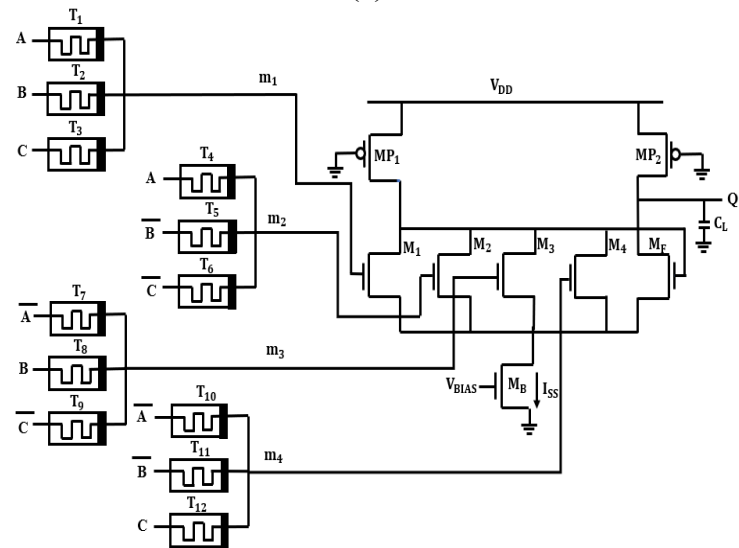
(c)



(d)



(e)



(f)

Fig. 3.13 PG using different PFSCS design schemes (a) NOR/OR [66-67] (b) FC [66-67] (c) Multithreshold FC [68] (d) QC [69] (e) Proposed design scheme-1 (f) Proposed design scheme-2

The conventional PFSCS FC and multithreshold FC PG are implemented using a cascade of two PFSCS FC XOR2 gates, as a single PFSCS FC can realize only up to two minterms. For PG realization, an XOR3 gate is required, which necessitates the cascading of XOR2 gates in conventional design schemes. The complete circuit diagrams of conventional PFSCS FC and multithreshold FC XOR3 gate are shown in Fig. 3.13 (b) and (c) respectively. Further, the PFSCS QC based realization however implements the PG in a single PFSCS gate as shown in Fig 3.13(d). The Boolean expression used in PFSCS QC for PG design is expressed as:

$$Q = A.B.C + A.\overline{B}.\overline{C} + \overline{A}.B.\overline{C} + \overline{A}.\overline{B}.C \quad (3.23)$$

The above Boolean function is followed for PG realization using the proposed design schemes. The circuit of PG using proposed design scheme-1 is drawn in Fig. 3.13(e). The minterms $A.B.C$, $A.\overline{B}.\overline{C}$, $\overline{A}.B.\overline{C}$ and $\overline{A}.\overline{B}.C$ are realized by the memristors ($T_1 - T_3$), ($T_4 - T_6$), ($T_7 - T_9$), ($T_{10} - T_{12}$) respectively and the corresponding outputs ($m_1 - m_4$) are further fed to the memristors ($T_{13} - T_{16}$) to realize OR functionality. The output of MBN drives a PFSCS buffer. Alternatively, the proposed design scheme-2 PG realize the four minterms and the directly feed the corresponding output to the input transistors $M_1 - M_4$ in a PFSCS OR gate as illustrated in Fig. 3.13(f).

Simulation section

The functionality of 3-bit PG based on proposed design schemes is examined and their performance is compared with existing NOR/OR, FC, multithreshold FC and QC based realizations. All the simulations are carried out in LT spice by using PTM 90nm CMOS technology parameters and memristor model suggested in [109] with a V_{DD} , I_{SS} , V_{SWING} and C_L of 1.1V, 100 μ A, 400mV, 50fF respectively. The layouts of PG based on existing schemes and proposed design schemes are drawn in Microwind. The results are summarized in Table 3.9 and the following observations are made:

Table 3.9 Performance comparison of 3-bit PG

Parameter Scheme	Power consumption (μ W)	Propagation delay (ps)	PDP (fJ)	Gate count	Area (μm^2)
NOR/OR	550	710	390.50	5	254
FC	220	609	133.98	2	914
Multithreshold FC	220	609	133.98	2	212
QC	110	513	56.43	1	1272
Proposed design scheme-1	110	416	45.76	1	23.52
Proposed design scheme-2	110	406	44.66	1	33.07

1. The PG design based on the proposed and the conventional QC schemes consume same power consumption and achieve a maximum reduction of 80 % in power consumption as compared to the conventional NOR/OR scheme.
2. The PG based on the proposed design scheme-2 shows a maximum propagation delay reduction of 42.81 % with respect to the NOR/OR scheme, mainly due to the reduced stages and gate count.
3. The proposed design scheme-2 achieves the maximum reduction in PDP vales of 88.54 % as compared to the existing counterparts and proposed design scheme-1.
4. The PG implemented using the proposed design scheme-1 occupies the minimum area. A maximum area reduction of 98 % is achieved in comparison to the PFSCS QC scheme due to the use of wider control transistor in the central branches.

Design example-2

Digital communication systems perform several operations such as data transmission, signal processing, and error control, all of which require high-speed arithmetic circuits. Among these, adders are fundamental since addition operations are repeatedly used in hardware processing. The CSA is a modified adder structure designed to reduce the effective carry propagation delay [114–115]. In a CSA, the adder bits are divided into blocks, and each block is examined to determine whether the incoming carry needs to propagate through it. If all bits within a block allow carry propagation, the carry is skipped and forwarded directly to the next block without waiting for internal carry computation. This technique reduces the carry propagation path, thereby lowering propagation delay and enhancing the overall adder performance, making CSAs suitable for high-speed digital and communication applications [7,116].

Fig. 3.14 illustrates the block diagram of a 4-bit CSA. Each 1-bit full adder in the block produces (S_i) and carry (C_i) outputs defined as:

$$S_i = A_i \oplus B_i \oplus C_i \quad (3.24)$$

$$C_{i+1} = (A_i \cdot B_i) + (C_i \cdot (A_i \oplus B_i)) \quad (3.25)$$

for $i=0$ to 3, where A_i are the adder inputs, C_i is the incoming carry, S_i is the sum, and C_{i+1} is the carry output. The propagate signals for each bit are defined as $P_i = A_i \oplus B_i$. These propagate signals are combined using a PFSCS 4-bit AND gate to generate an intermediate block propagate signal:

$$F = P_0 \cdot P_1 \cdot P_2 \cdot P_3 \quad (3.26)$$

A PFSCS 2:1 MUX is then used to select the appropriate output based on the control signal S_0 . The MUX output Q can be expressed as:

$$Q = \overline{S_0} F + S_0 \quad (3.27)$$

Here, the MUX forwards either the incoming carry or the generated carry to the next stage depending on the propagate condition. All these blocks full adders, AND gate, and MUX are implemented using PFSCl gate designs, following both existing and proposed schemes. The circuit-level implementation of individual gates has already been presented in the previous chapter and is therefore not repeated here.

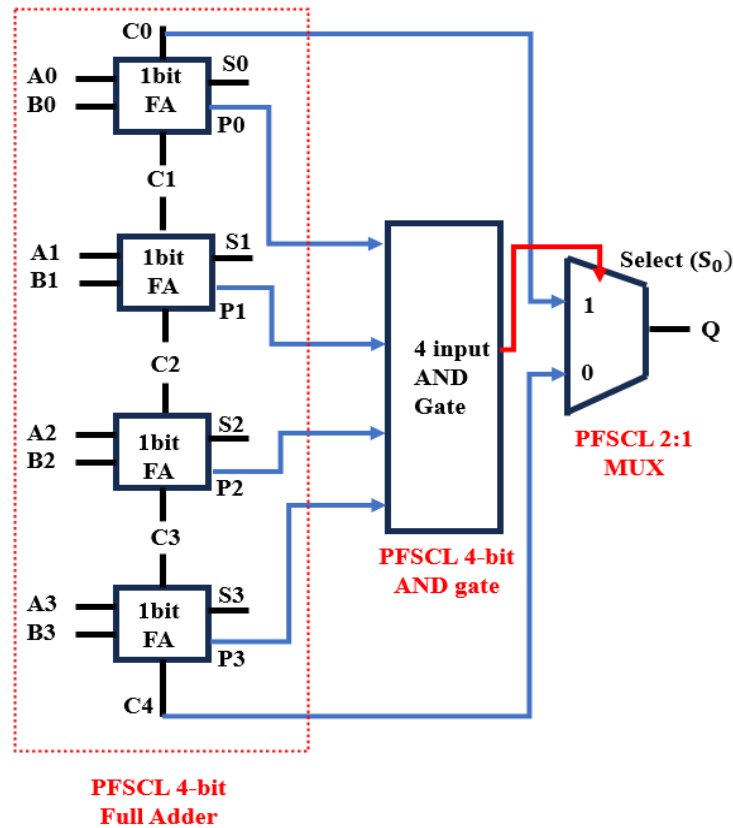


Fig. 3.14 Block diagram of 4-bit CSA

Simulation section

The functionality of the proposed CSA design schemes is evaluated and their performance is compared with PFSCl NOR/OR, FC, and multithreshold FC based realizations. The PFSCl QC realization is not considered in this analysis, as the CSA does not require an XOR3 gate, for which the QC scheme is primarily suited. The same simulation environment used for the proposed PG designs is also employed for the examined of the proposed CSA designs. The performance of the CSA is compared in terms of power consumption, propagation delay, PDP, gate count, and area. The results are summarized in Table 3.10. The following observations are made:

Table 3.10 Performance comparison of 4-bit CSA

Scheme Parameter	NOR/ OR	FC	Multithreshold FC'	Proposed design scheme-1	Proposed design scheme-2
Propagation delay (ps)	1245	1097	1097	801	769
Power consumption (μ W)	4400	3520	3520	1540	1540
PDP (fJ)	5478	3861	3861	1233	1184
Gate count	40	32	32	14	14
Area (μm^2)	3041	22560	2546	1324	1588

1. The CSA designs based on proposed design schemes consumes the same power consumption and achieve a maximum power reduction of about 65 % as compared to the conventional NOR/OR design scheme.
2. The CSA based on the proposed design scheme-2 shows a maximum propagation delay reduction of about 38.23 % with respect to the NOR/OR scheme, mainly due to the reduced stages and gate count.
3. The proposed design scheme-2 achieves the maximum reduction in PDP values of 78.38 % as compared to the existing counterparts and proposed design scheme-1.
4. The PG implemented using the proposed design scheme-1 occupies the minimum area, with a maximum area reduction of about 94 % compared to the PFSCS FC scheme due to the use of wider control transistor in the central branch.

3.6 Conclusion

In this chapter, memristors are introduced in PFSCS style to amalgamate their advantages in circuit design. Two new memristor based PFSCS design schemes are presented. The first proposed design scheme-1 employs memristors with a PFSCS inverter, while the second proposed design scheme-2 utilizes memristors integrated with PFSCS NOR/OR gates. The behavior of the proposed gates for the design schemes is analysed in terms of voltage swing, small-signal voltage gain and noise margin. The proposed gates eliminate the restriction of implementing NOR/OR or three input sum-of-minterms forms in existing architectures. The reduced gate count gives significant advantage in power consumption and propagation delay values. This premise is proven through the simulation of different gates using PTM 90 nm CMOS technology parameters and a TiO_2 memristor. The performance is compared with existing PFSCS counterparts. From the simulations results, it is clear that use of the

proposed design scheme-2 PFSCl gates show significant improvements in propagation delay, power consumption and PDP values respectively over existing counterparts. A maximum improvement of 28 %, 66.66 %, 75.75 % in propagation delay, power consumption and PDP values is obtained in proposed design scheme-2 PFSCl XOR2 gates over existing counterparts. In addition, a maximum area reduction of 94.85 % and 92.76 % is achieved using proposed design scheme-1 and scheme-2, respectively, compared to the conventional PFSCl FC XOR2 gate. Further, the robustness of proposed design scheme based PFSCl gates is evaluated under process variations using Monte Carlo simulations and corner analysis, which confirm correct functionality across all design schemes. Overall, this chapter establishes that memristor integration in static PFSCl style offers a promising approach for designing compact and efficient logic circuits suitable for mixed -signal applications.

CHAPTER 4

IMPROVED DYNAMIC PFSCS GATES

4.1 Introduction

D-PFSCS gates are considered a promising alternative to static PFSCS gates for portable and low power mixed-signal applications. In D-PFSCS gates, the constant current source used in static PFSCS gates is replaced with a dynamic current source (DCS), resulting in significant power savings [80]. Conventionally, the realization of logic functions in the D-PFSCS style relies on NOR/OR based D-PFSCS gates, which generally necessitates cascading multiple gates with intermittent self-timed buffers (STBs). This arrangement leads to increased propagation delay and power consumption, thereby degrading overall performance.

To address these issues, two alternative design schemes have been reported that modify the PDN using either low threshold voltage transistors [81] or transmission gates (TGs) [82]. D-PFSCS gates employing low threshold voltage transistors in the PDN are power efficient, however, they require an additional fabrication step in the form of threshold-adjust implant. TG based D-PFSCS gates can accommodate more than two minterms within a single gate, thereby reducing the number of logic stages. Despite this advantage, such design scheme incurs a larger footprint because both PMOS and NMOS transistors are used in the PDN, which necessitates well formation. Therefore, an alternative D-PFSCS realization scheme that mitigates the limitations of existing D-PFSCS styles is presented. This scheme is based on the use of memristors, motivated by their recent adoption in integrated circuit technology. The small footprint of memristors enables the design of D-PFSCS gates with a reduced overall area requirement.

The chapter describes the two new D-PFSCS styles wherein a memristor based network is incorporated with D-PFSCS inverter and D-PFSCS NOR/OR gates. The former is referred to as proposed design scheme-3 and latter is called proposed design scheme-4. The operation of both the proposed schemes are elucidated, the corresponding voltage swing is formulated mathematically followed by simulations results for verifying functionality and the performance of the proposed gates is compared with the existing counterparts.

4.2 Proposed memristor based D-PFSCS designs

In this section, memristors are introduced in D-PFSCS circuit design. Two design schemes are proposed, wherein the first scheme embeds MBN with a D-PFSCS inverter while the later uses with D-PFSCS NOR/ OR gate.

4.2.1 Proposed design scheme-3

A block diagram of D-PFSCL gate based on proposed design scheme-3 is depicted in Fig. 4.1. It uses precharge transistors (MP_1 , MP_2) and DCS (M_{B1} , M_{B2} , C_{dyn}) driven by a clock (CLK) signal. The PDN consist of a MBN that realizes the given functionality and the corresponding output further drives the D-PFSCL inverter/buffer.

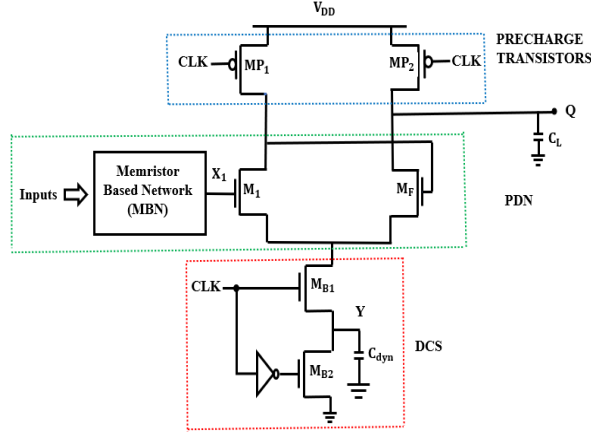


Fig. 4.1 Block diagram of proposed design scheme-3 D-PFSCL gate

Operation and analysis

To elucidate the concept further, a 2:1 MUX with input lines I_0 , I_1 , and select line S_0 is considered. Depending upon the select line S_0 , the value of either input I_0 or I_1 is transferred to the output node, Q and the functionality is expressed as:

$$Q = \overline{S_0}I_0 + S_0I_1 \quad (4.1)$$

The schematic of a 2:1 MUX based on proposed design scheme-3 is shown in Fig. 4.2. The minterms ($\overline{S_0}I_0$) and (S_0I_1) are realized by memristors (T_1 , T_2) and (T_3 , T_4) respectively. The corresponding intermediate outputs Y_1 and Y_2 are fed as inputs to the OR configured memristors (T_5 , T_6) whose output X_1 then drives the D-PFSCL buffer.

The circuit operates in two phases namely precharge and evaluation phase depending on the value of CLK signal. For a low value of CLK signal, the circuit operates in precharge phase. The output node, Q is precharged to V_{DD} and capacitor C_{dyn} discharged to ground. The output X_1 of MBN is changed according to the applied inputs (S_0 , I_0 , I_1). However, any change in voltage level at node X_1 does not affect the output node, Q as M_{B1} is OFF. Consequently, for a high value of CLK signal the circuit enters in evaluation phase, the transistors MP_1 , MP_2 , M_{B2} are turned OFF and PDN transistors M_1 and M_F evaluates according to the logic value obtained through MBN at node X_1 .

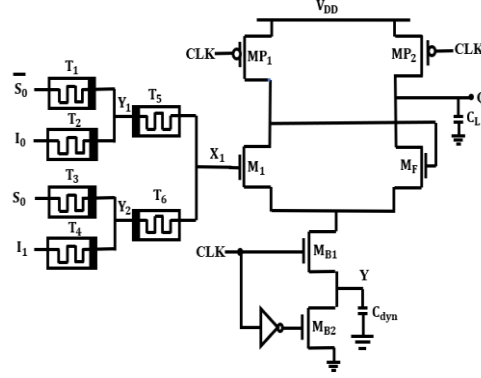


Fig. 4.2 Proposed design scheme-3 D-PFSCL 2:1 MUX

Considering the voltage levels of D-PFSCL style, the voltage level of MBN at node X_1 for different input combinations in the evaluation phase is analyzed here. Further, the resistances of the memristor in HRS and LRS states are assumed to be R_{OFF} and R_{ON} respectively. The high (V_{OH}) and low (V_{OL}) voltage levels for the inputs are assumed to be V_{DD} and $V_{DD} - V_{SWING}$ respectively. Since 2:1 MUX has three inputs S_0 , I_0 and I_1 , therefore there are eight possible input combinations. The voltage level at different nodes for different input cases are computed using voltage divider rule and the same is described below:

Case -1: All Inputs (S_0 , I_0 , I_1) are at low (V_{OL}) voltage level.

The memristors T_1 and T_2 are driven by high and low voltage levels respectively therefore, there exists a current flow from T_1 to T_2 such that T_1 is in HRS state while T_2 attains LRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{V_{DD}R_{ON} + (V_{DD} - V_{SWING})R_{OFF}}{R_{ON} + R_{OFF}} \quad (4.2)$$

As $R_{OFF} \gg R_{ON}$, (4.2) is reduced to

$$V(Y_1) \approx V_{DD} - V_{SWING} = V_{OL} \quad (4.3)$$

Similarly, both the memristors T_3 and T_4 are driven by low voltage levels, thus no current flow across them and $V(Y_2)$ attains a low voltage level (V_{OL}). Consequently, the memristors T_5 and T_6 are driven by low voltage level which leads to low voltage level (V_{OL}) at node X_1 expressed as:

$$V(X_1) = V_{DD} - V_{SWING} = V_{OL} \quad (4.4)$$

During the evaluation phase, a low voltage level at node X_1 turns OFF the transistor M_1 in the PDN. This results in a decrease in voltage at the output node, Q due to the charge transfer from C_L to C_{dyn} through M_F . Thus, a low voltage level ($V_{OL} = V_{DD} - V_{SWING}$) is obtained at the output node, Q . It is pertinent to mention here that appropriate value of C_{dyn} must be used to achieve required voltage swing. The

expression for C_{dyn} for a given voltage swing is found by using charge conservation theorem [80] and is given as:

$$C_{\text{dyn}} = \frac{V_{\text{SWING}} \times C_L}{V_{\text{DD}} - V_{\text{SWING}}} \quad (4.5)$$

Case-2: Inputs (S_0, I_0) are at low (V_{OL}) and I_1 is at high (V_{OH}) voltage levels.

The memristors T_1 and T_2 are driven by high and low voltage levels respectively therefore, there is a current flow from T_1 to T_2 such that T_1 is in HRS state while T_2 attains a LRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{V_{\text{DD}}R_{\text{ON}} + (V_{\text{DD}} - V_{\text{SWING}})R_{\text{OFF}}}{R_{\text{ON}} + R_{\text{OFF}}} \quad (4.6)$$

As $R_{\text{OFF}} \gg R_{\text{ON}}$, (4.6) is reduced to

$$V(Y_1) \approx V_{\text{DD}} - V_{\text{SWING}} = V_{\text{OL}} \quad (4.7)$$

The memristors T_3 and T_4 are driven by low and high voltage levels respectively such that current flow through T_4 to T_3 . Thus, memristor T_3 is in LRS state while T_4 attain HRS state. Thus, $V(Y_2)$ is expressed as:

$$V(Y_2) = \frac{(V_{\text{DD}} - V_{\text{SWING}})R_{\text{OFF}} + V_{\text{DD}}R_{\text{ON}}}{R_{\text{ON}} + R_{\text{OFF}}} \quad (4.8)$$

As $R_{\text{OFF}} \gg R_{\text{ON}}$, (4.8) is reduced to

$$V(Y_2) \approx V_{\text{DD}} - V_{\text{SWING}} = V_{\text{OL}} \quad (4.9)$$

Consequently, the memristor T_5 and T_6 are driven by low voltage levels leading to a low voltage level (V_{OL}) at node X_1 . In this case, M_F is ON and causes charge transfer from C_L to capacitor C_{dyn} during evaluation phase. Thus, a low voltage level ($V_{\text{OL}} = V_{\text{DD}} - V_{\text{SWING}}$) is obtained at the output node, Q .

Case-3: Inputs (S_0, I_1) are at high (V_{OH}) and I_0 is at low (V_{OL}) voltage levels.

As both the memristors T_1 and T_2 are driven by low voltage levels, there will not be any current flow and $V(Y_1)$ will be at low voltage level (V_{OL}). Like memristors T_1 and T_2 , both the memristors T_3 and T_4 are driven by high voltage level so, there will not be any current flow and $V(Y_2)$ will be at high voltage level (V_{OH}). Further, the memristors T_5 and T_6 are driven by low and high voltage levels respectively. There would be current flow through memristor T_6 to T_5 such that T_5 will be in HRS state while T_6 will attain LRS state. Thus, $V(X_1)$ is expressed as:

$$V(X_1) = \frac{(V_{\text{DD}} - V_{\text{SWING}})R_{\text{ON}} + V_{\text{DD}}R_{\text{OFF}}}{R_{\text{ON}} + R_{\text{OFF}}} \quad (4.10)$$

As $R_{OFF} \gg R_{ON}$, (4.10) is reduced to

$$V(X_1) \approx V_{DD} = V_{OH} \quad (4.11)$$

As high voltage level is obtained at node X_1 therefore M_1 is ON and M_F is OFF consequently there is no charge transfer from C_L and C_{dyn} in evaluation phase and a high voltage level ($V_{OH} = V_{DD}$) is obtained at the output node, Q.

Case-4: All inputs S_0 , I_0 and I_1 are at high (V_{OH}) voltage levels.

The memristors T_1 and T_2 are respectively driven by low and high voltage levels therefore, there is a current flow from T_2 to T_1 such that T_1 is in LRS state while T_2 attains HRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{(V_{DD} - V_{SWING})R_{OFF} + V_{DD} R_{ON}}{R_{ON} + R_{OFF}} \quad (4.12)$$

As $R_{OFF} \gg R_{ON}$, (4.12) is reduced to

$$V(Y_1) \approx V_{DD} - V_{SWING} = V_{OL} \quad (4.13)$$

Since both the memristors T_3 and T_4 are driven by high voltage levels, there is no current flow and $V(Y_2)$ is at high voltage level (V_{OH}). Further, the memristors T_5 and T_6 are driven by low and high voltage levels respectively. There would be current flow through T_6 to T_5 . Thus, $V(X_1)$ is expressed as:

$$V(X_1) = \frac{(V_{DD} - V_{SWING})R_{ON} + V_{DD} R_{OFF}}{R_{ON} + R_{OFF}} \quad (4.14)$$

As $R_{OFF} \gg R_{ON}$, (4.14) is reduced to

$$V(X_1) \approx V_{DD} = V_{OH} \quad (4.15)$$

As high voltage level is obtained at node X_1 therefore exist no charge transfer from C_L and C_{dyn} in evaluation phase and a high voltage level ($V_{OH} = V_{DD}$) is obtained at the output node, Q. Similar analysis is done for remaining input combinations. Table 4.1 enlists all intermediate node voltages and the output of 2:1 MUX based on proposed design scheme-3 for all possible input combinations.

Table 4.1 Node voltages in the proposed design scheme-3 D-PFSCL 2:1 MUX

Inputs			Intermediate node voltage			Output
S_0	I_0	I_1	Y_1	Y_2	X_1	Q
V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OL}	V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OH}
V_{OL}	V_{OH}	V_{OH}	V_{OH}	V_{OL}	V_{OH}	V_{OH}

V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OH}	V_{OH}
V_{OH}	V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OH}	V_{OH}	V_{OH}	V_{OL}	V_{OH}	V_{OH}	V_{OH}

where $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - V_{SWING}$

It is to be emphasized that the output makes only high to low transition so the high to low propagation delay (τ_{PHL}) is of significance. The propagation delay, τ_{PHL} is defined as the time elapsed between 50 % transition of the CLK signal to 50 % transition of the falling voltage at output node, Q of proposed design scheme-3 D-PFSCCL 2:1 MUX. The transistor is modelled as switch, S in series with resistor, R, C_L and C_{dyn} representing the output load capacitance and capacitance used in DCS respectively. The parasitic capacitance associated at node Y is ignored for first hand calculations as its value is insignificant in comparison to C_L and C_{dyn} . The equivalent circuit during evaluation phase which determines the propagation delay for charge transfer from C_L to C_{dyn} is shown in Fig. 4.3 (a) and the timing behavior is shown in Fig. 4.3(b).

Initially, the output node Q is precharged to V_{DD} and consequently upon changing the switch S from position 1 to position 2 at the reference time $t = 0$, charge redistribution takes place. After switching, the Kirchhoff voltage equation for the loop is written as:

$$i(t)R + \frac{1}{C_{dyn}} \int_{0^-}^t i(t)dt + \frac{1}{C_L} \int_{0^-}^t i(t)dt - V_{DD} = 0 \quad (4.16)$$

where $i(t)$ is current following in the circuit. Differentiation of (4.16) gives:

$$\frac{di(t)R}{dt} + \frac{1}{C_{dyn}} i(t) + \frac{1}{C_L} i(t) = 0 \quad (4.17)$$

Equation (4.17) can be solved for $i(t)$ by applying the initial condition in circuit just before switching action taken place ($t = 0^-$)

$$i(0) = k; \quad \text{where } k \text{ is a constant} \quad (4.18)$$

Also, in the circuit at time ($t = 0^-$), the voltage across load capacitor, $V_1 = V_{DD}$ and the capacitor C_{dyn} is discharged to ground i.e. $V_2 = 0$ such that

$$i(0) = k = \frac{V_{DD}}{R} \quad (4.19)$$

Using (4.19), the solution of (4.17) is given as:

$$i(t) = \frac{V_{DD}}{R} e^{-\left(\frac{C_L + C_{dyn}}{C_L C_{dyn} R}\right)t} \quad (4.20)$$

and the voltage at capacitor C_L is expressed as:

$$V_1(t) = -\frac{1}{C_L} \int_{-\infty}^t i(t)dt \quad (4.21)$$

Putting the value of $i(t)$ from (4.20) in (4.21) gives:

$$V_1(t) = -\frac{1}{C_L} \int_{-\infty}^t \frac{V_{DD}}{R} e^{-\left(\frac{C_L+C_{dyn}}{C_L C_{dyn} R}\right)t} dt \quad (4.22)$$

After, solving (4.22), the voltage $V_1(t)$ is computed as:

$$V_1(t) = \frac{V_{DD} C_{dyn}}{(C_L + C_{dyn})} e^{-\left(\frac{C_L+C_{dyn}}{C_L C_{dyn} R}\right)t} + K_1 \quad (4.23)$$

The value of constant K_1 is computed by applying the initial conditions and is found as:

$$K_1 = \frac{V_{DD} C_L}{(C_L + C_{dyn})} \quad (4.24)$$

By putting the value of K_1 , (4.23) modifies to (4.25).

$$V_1(t) = \frac{V_{DD} C_{dyn}}{(C_L + C_{dyn})} e^{-\left(\frac{C_L+C_{dyn}}{C_L C_{dyn} R}\right)t} + \frac{V_{DD} C_L}{(C_L + C_{dyn})} \quad (4.25)$$

Equation (4.25) can be used to calculate τ_{PHL} by putting $V_1(t) = V_{DD} - \frac{V_{Swing}}{2}$ where $t_{50\%}$ represents time at which output voltage falls to 50% of its value as shown in Fig. 4.3(b).

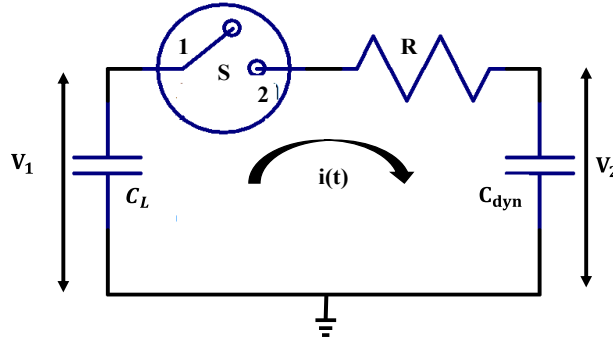
$$V_{DD} - \frac{V_{Swing}}{2} = \frac{V_{DD} C_{dyn}}{(C_L + C_{dyn})} e^{-\left(\frac{C_L+C_{dyn}}{C_L C_{dyn} R}\right)t_1} + \frac{V_{DD} C_L}{(C_L + C_{dyn})} \quad (4.26)$$

Taking logarithm of both sides and rearranging terms, (4.26) is written as:

$$\left[-\left(\frac{C_L+C_{dyn}}{C_L C_{dyn} R}\right) \tau_{PHL} \right] = \ln \left[1 - \frac{V_{Swing}(C_L+C_{dyn})}{2(V_{DD} C_{dyn})} \right] \quad (4.27)$$

Using (4.5) in (4.27), the high-to-low output delay, τ_{PHL} is found as:

$$\tau_{PHL} = \ln(2) R C_L \quad (4.28)$$



(a)

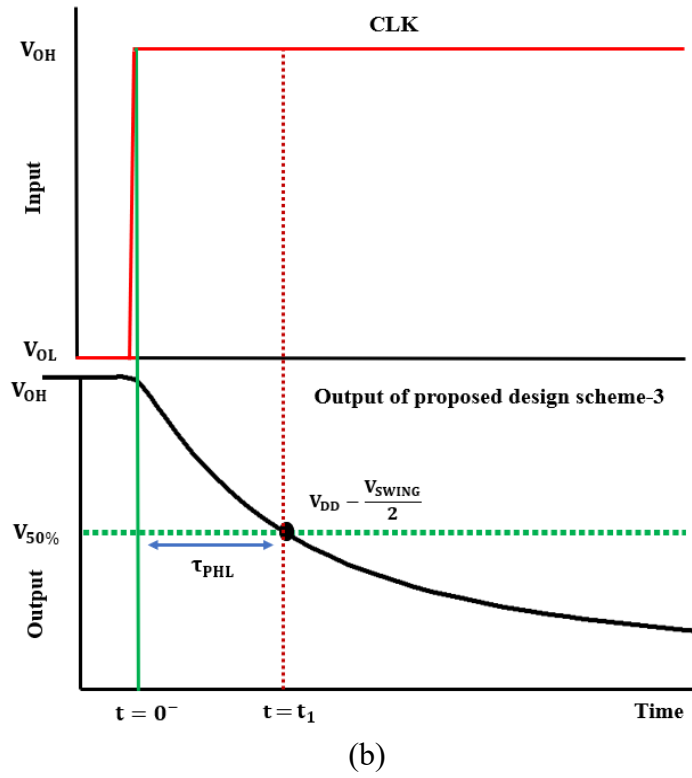
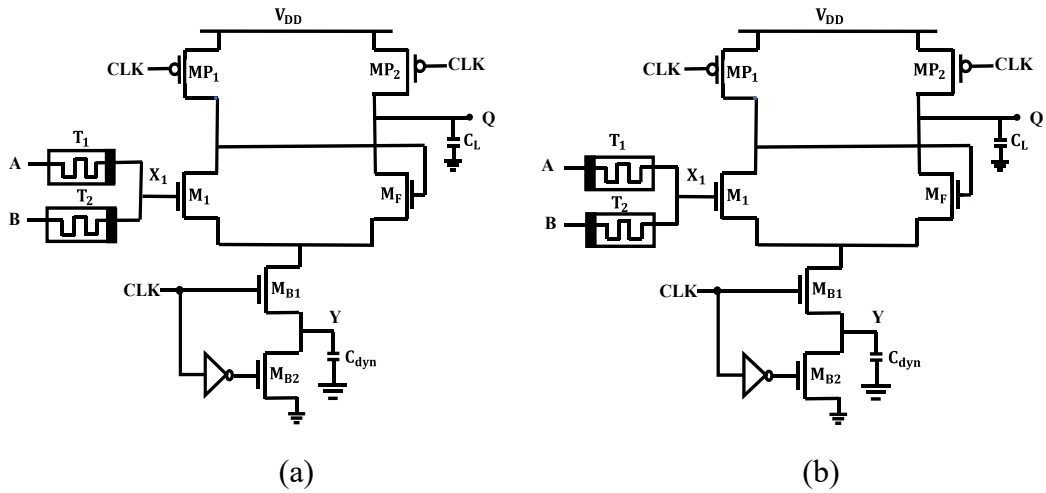


Fig. 4.3 Proposed design scheme-3 D-PFSCSCL 2:1 MUX (a) Equivalent circuit (b) Timing waveform

The proposed design scheme-3 is extended to realize other basic functions. The realization of AND2, OR2, and XOR2 gates are drawn in Fig 4.4.



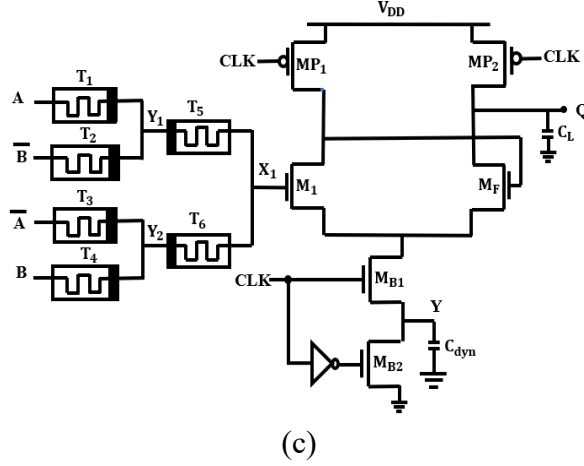


Fig. 4.4 Proposed design scheme-3 D-PFSCL gates (a) AND2 (b) OR2 (c) XOR2

4.2.2 Simulation section

The functionality of proposed design scheme-3 D-PFSCL 2:1 MUX is first verified and then its performance is compared with its existing D-PFSCL counterparts. All the simulations are carried out in LT spice by using PTM 90nm CMOS technology parameters and memristor model suggested in [109] with a V_{DD} , I_{SS} , V_{SWING} and C_L of 1.1V, 100 μ A, 400mV, 50fF respectively. The layout of all the 2:1 MUX realizations is drawn in Microwind. The timing waveforms of the proposed design scheme-3 D-PFSCL 2:1 MUX is shown in Fig. 4.5. It can be observed that for low value of CLK signal, the circuit is in precharge phase with output precharged to V_{DD} and the changes in inputs do not have any effect on the output node, Q. During the evaluation phase, input I_1 is reflected at the output node, Q for high value of S_0 while the input I_0 is available at the output node, Q for low value of S_0 . Thus, there is conformance between the timing waveform and the predicted behavior. The layout of D-PFSCL 2:1 MUX based on proposed scheme-3 drawn using Microwind is depicted in Fig. 4.6. and occupies area of 8.13 μm^2 .

Table 4.2 Performance comparison of different D-PFSCL 2:1 MUX

Parameter \ Scheme	NOR/ OR	Multithreshold FC	TG	Proposed design scheme-3
Gate count	3	1	1	1
STB count	1	0	0	0
Transistor count	29	16	12	8
Power consumption (μ W)	9.5	2.43	2.42	2.42
Propagation delay (ps)	683	315	311	311
PDP (fJ)	6.48	0.76	0.75	0.75
Memristor count	-	-	-	6
Area (μm^2)	80.99	28.8	11.8	8.13

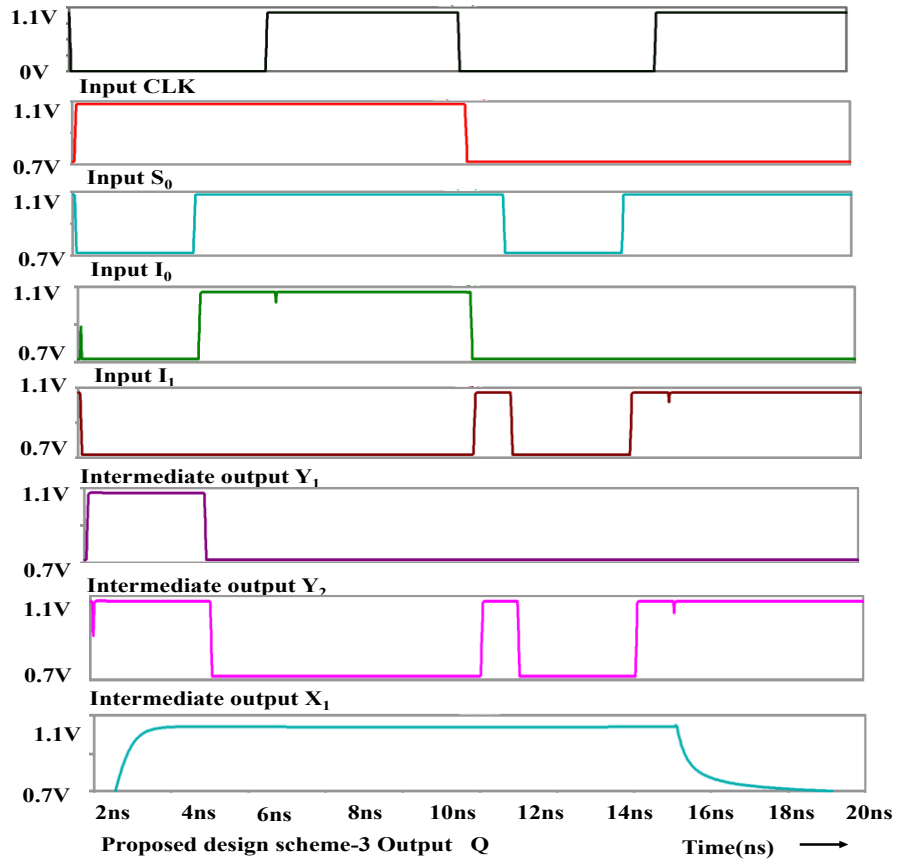


Fig. 4.5 Timing waveform of proposed design scheme-3 D-PFSCL 2:1 MUX

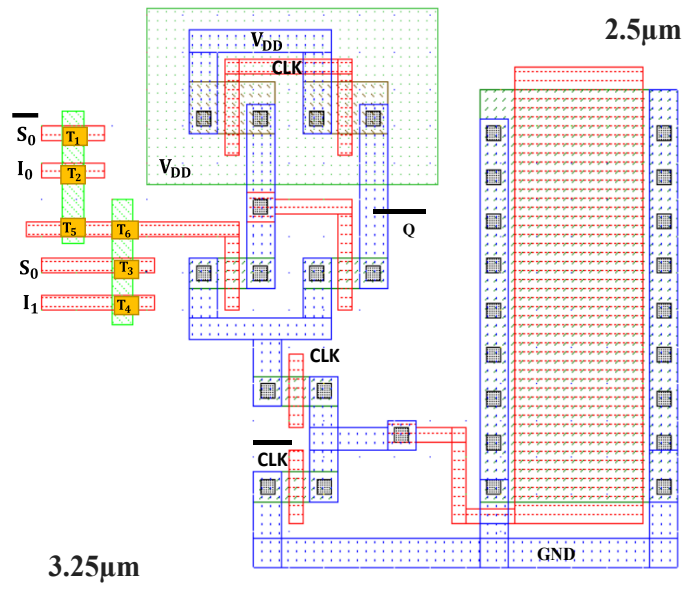


Fig. 4.6 Layout of proposed design scheme-3 D-PFSCL 2:1 MUX

The performance of D-PFSCL 2:1 MUX based on existing and proposed design scheme-3 is compared based on gate count, STB count, transistor count, power consumption, propagation delay, PDP, memristor count and area. The obtained values are listed in Table 4.2. The following observations are drawn.

1. The proposed design scheme-3 D-PFSCL 2:1 MUX achieves transistor count reductions of 72.4 %, 50 %, and 33.3 % compared to NOR/OR, FC, and TG based design schemes, respectively. This reduction is primarily because the 2:1 MUX realized using the NOR/OR scheme arranges the logic in two stages and requires intermittent STBs to ensure that the second stage begins evaluation only after the complete evaluation of the preceding stage. In contrast, the remaining schemes implement the 2:1 MUX within a single gate and therefore eliminate the need for STBs.
2. The proposed design scheme-3 D-PFSCL 2:1 MUX offers the same power saving of 75 % as offered by 2:1 MUX based on FC and TG schemes in comparison to NOR/OR based counterpart.
3. A maximum area reduction of 90 % is achieved through proposed design scheme-3 D-PFSCL 2:1 MUX. This is because memristors are integrated on top of CMOS substrate using postprocessing, e.g., nanoimprint lithography (NIL), a process that does not disturb the CMOS circuitry underneath [110-111].

4.2.3 Proposed design scheme-4

The proposed design scheme-4 employs MBN to implement minterms only and uses a D-PFSCL NOR/ OR gate to perform NOR/OR operation for sum of minterms. A realization for logic function with N-minterms using proposed design scheme-4 is depicted in Fig. 4.7. The respective outputs of N-minterms (Y_1 ----- Y_N) are fed to a N-input of OR D-PFSCL gate. The NOR output may also be taken from drain terminal of load transistor MP_1 .

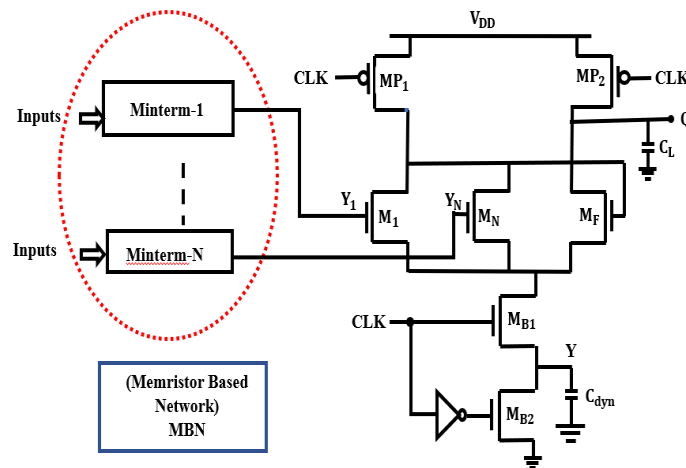


Fig. 4.7 Block diagram of proposed design scheme-4 D-PFSCL gate

Operation and analysis

The schematic of the proposed design scheme-4 D-PFSCCL 2:1 MUX is shown in Fig. 4.8. The memristors (T_1, T_2) and (T_3, T_4) implement the minterms $\overline{S_0}I_0$ and S_0I_1 respectively. The corresponding outputs Y_1 and Y_2 are fed to the input transistors M_1 and M_2 respectively in D-PFSCCL OR2 gate. For a low value of CLK signal, the circuit operates in precharge phase and the output node, Q is precharged to V_{DD} while capacitor C_{dyn} is discharged to ground. The changes in inputs update the output nodes Y_1 and Y_2 . However, these changes do not affect the output at node, Q as M_{B1} is OFF. Subsequently, the circuit enters in the evaluation phase when CLK assumes high value and the output gets evaluated accordingly. The analysis of the proposed design scheme-4 D-PFSCCL 2:1 MUX in the evaluation phase is performed by first computing the voltage levels at intermediate nodes Y_1 and Y_2 for different input combinations and then determining the corresponding output of the D-PFSCCL OR2 gate.

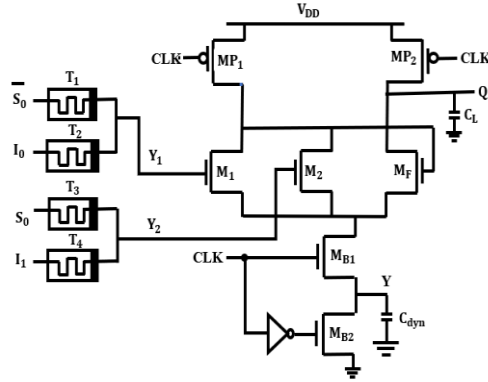


Fig. 4.8 Proposed design scheme-4 D-PFSCCL 2:1 MUX

For a 2:1 MUX, there are eight possible input combinations of (S_0, I_0, I_1). The voltage level at different nodes for all input combinations are computed using voltage divider rule and the same is described below:

Case-1: All Inputs S_0, I_0, I_1 are at low voltage level (V_{OL}).

The memristors T_1 and T_2 are driven by high and low voltage levels respectively therefore, current flows from T_1 to T_2 such that T_1 is in HRS state while T_2 attains LRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{V_{DD}R_{ON} + (V_{DD} - V_{SWING})R_{OFF}}{R_{ON} + R_{OFF}} \quad (4.29)$$

As $R_{OFF} \gg R_{ON}$, (4.29) reduces to

$$V(Y_1) \approx V_{DD} - V_{SWING} = V_{OL} \quad (4.30)$$

Since both T_3 and T_4 are driven by low voltage levels, therefore no current flow across them and $V(Y_2)$ attains a low voltage level (V_{OL}). During the evaluation phase, the low output voltage levels of Y_1 and Y_2 are fed to D-PFSCCL OR2 gate such that both the transistors M_1 and M_2 are OFF and M_F conducts. Subsequently, there exist a charge transfer from C_L and C_{dyn} in evaluation phase and a low voltage level ($V_{OL} = V_{DD} - V_{SWING}$) is obtained at the output node, Q.

Case-2: Inputs S_0, I_0 are at low voltage level (V_{OL}) and I_1 is at high voltage level (V_{OH}).

The memristors T_1 and T_2 are driven by high and low voltage levels respectively therefore, there is a current flow from T_1 to T_2 such that T_1 is in HRS state while T_2 attains LRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{V_{DD}R_{ON} + (V_{DD} - V_{SWING})R_{OFF}}{R_{ON} + R_{OFF}} \quad (4.31)$$

As $R_{OFF} \gg R_{ON}$, (4.31) reduces to:

$$V(Y_1) \approx V_{DD} - V_{SWING} = V_{OL} \quad (4.32)$$

The memristors T_3 and T_4 are driven by low and high voltage levels respectively such that current flow through T_4 to T_3 . Thus, memristor T_3 is in LRS state while T_4 attain HRS state. Thus, $V(Y_2)$ is expressed as:

$$V(Y_2) = \frac{(V_{DD} - V_{SWING})R_{OFF} + V_{DD}R_{ON}}{R_{ON} + R_{OFF}} \quad (4.33)$$

As $R_{OFF} \gg R_{ON}$, (4.33) reduces to:

$$V(Y_2) \approx V_{DD} - V_{SWING} = V_{OL} \quad (4.34)$$

During the evaluation phase, as both the outputs Y_1 and Y_2 are at low voltage level, transistor M_1 and M_2 are turned OFF. The transistor M_F causes charge transfer from C_L to C_{dyn} in evaluation phase and a low voltage level ($V_{OL} = V_{DD} - V_{SWING}$) is obtained at the output node, Q.

Case-3: Inputs S_0, I_1 are at high (V_{OH}) and I_0 is at low (V_{OL}) voltage level.

As both the memristors T_1 and T_2 are driven by low voltage levels, therefore there is no current flow and $V(Y_1)$ attains a low voltage level (V_{OL}). Like T_1 and T_2 , since both the memristors T_3 and T_4 are driven by high voltage level so no current flows and $V(Y_2)$ obtain a high voltage level (V_{OH}). In this case, M_1 is OFF while M_2 conducts such that no current flows from M_F . Thus, no charge transfer takes place from C_L to C_{dyn} and the output node, Q retains the high voltage level ($V_{OH} = V_{DD}$).

Case-4: All inputs S_0, I_0 and I_1 are at high (V_{OH}) voltage levels.

The memristors T_1 and T_2 are driven by low and high voltage level respectively therefore, there is a current flow from memristor T_2 to memristor T_1 such that T_1 is in LRS state while T_2 attains HRS state. Thus, voltage at node Y_1 , $V(Y_1)$ is expressed as:

$$V(Y_1) = \frac{(V_{DD} - V_{SWING}) R_{OFF} + V_{DD} R_{ON}}{R_{ON} + R_{OFF}} \quad (4.35)$$

As $R_{OFF} \gg R_{ON}$, (4.35) reduces to

$$V(Y_1) \approx V_{DD} - V_{SWING} = V_{OL} \quad (4.36)$$

Since both the memristors T_3 and T_4 are driven by high voltage levels, therefore no current flows through them and $V(Y_2)$ attains a high voltage level (V_{OH}).

During the evaluation phase, since Y_2 is at high voltage level, the transistor M_2 is turned ON causing M_F to be OFF. Thus, no charge transfer occurs from C_L to C_{dyn} and a high voltage level ($V_{OH} = V_{DD}$) is obtained at the output node, Q . Similar analysis is done for remaining input combinations and the Table 4.3 enlists voltage at different nodes of 2:1 MUX realized using proposed scheme-4.

Table 4.3 Summary of node voltages in proposed design scheme-4 D-PFSCL 2:1 MUX

Inputs			Intermediate outputs		Output
S_0	I_0	I_1	Y_1	Y_2	Q
V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OL}	V_{OH}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OH}
V_{OL}	V_{OH}	V_{OH}	V_{OH}	V_{OL}	V_{OH}
V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OH}
V_{OH}	V_{OH}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OH}	V_{OH}	V_{OH}	V_{OL}	V_{OH}	V_{OH}

where $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - V_{SWING}$

4.2.4 Simulation section

The functionality of the proposed design scheme-4 D-PFSCL 2:1 MUX is first verified and then the performance is compared with existing scheme counterparts. The same simulation environment considered for the proposed design scheme-3 D-PFSCL is used for the proposed design scheme-4 D-PFSCL gates.

The timing waveforms of proposed design scheme-4 D-PFSCL 2:1 MUX is shown in Fig. 4.9. It may be observed that output remains precharged to V_{DD} when the CLK signal attains a low voltage value. Further, during the evaluation phase, the selected input propagates to the output based on the select line S_0 . Thus, the observed

waveforms confirm the correct functionality of the proposed design scheme-4 D-PFSCL 2:1 MUX. The layout of the proposed design scheme-4 D-PFSCL 2:1 MUX is depicted in Fig. 4.10. It occupies an area of $9.62 \mu\text{m}^2$.

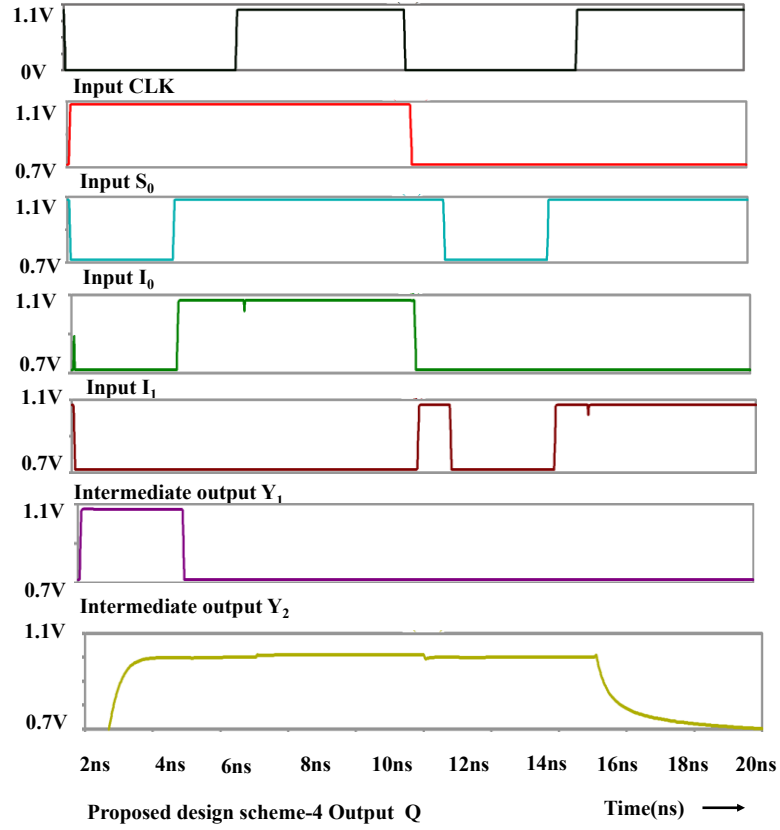


Fig. 4.9 Timing waveform of the proposed design scheme-4 D-PFSCL 2:1 MUX

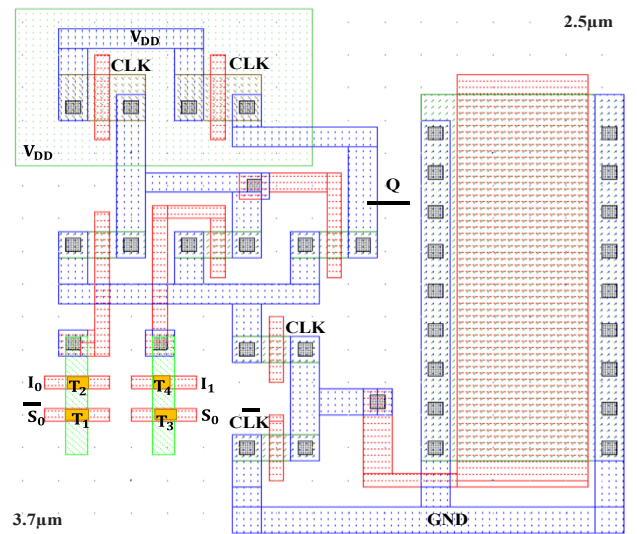


Fig. 4.10 Layout of proposed design scheme-4 D-PFSCL 2:1 MUX

Table 4.4 Performance comparisons of D-PFSCL 2:1 MUX

Parameter \ Scheme	NOR/ OR	Multithreshold FC	TG	Proposed design scheme - 4
Gate count	3	1	1	1
STB count	1	0	0	0
Transistor count	29	16	12	9
Power consumption (μ W)	9.5	2.43	2.42	2.4
Propagation delay (ps)	683	315	311	304
PDP (fJ)	6.48	0.77	0.75	0.72
Memristor count	-	-	-	4
Area (μm^2)	80.99	28.8	11.8	9.62

The performance of proposed design scheme-4 and existing schemes D-PFSCL 2:1 MUX is compared in terms of gate count, STB count, transistor count, power consumption, propagation delay, PDP, memristor count and area. The obtained values are listed in Table 4.4 and are discussed below:

1. The D-PFSCL 2:1 MUX implemented using the NOR/OR scheme consumes the highest power consumption, exhibiting approximately 75 % higher power compared to its counterparts based on other schemes. The propagation delay is minimum for proposed design scheme-4 D-PFSCL 2:1 MUX.
2. The D-PFSCL 2:1 MUX based on NOR/OR scheme has the highest PDP of 6.49 fJ, while proposed design scheme-4 D-PFSCL 2:1 MUX achieves the lowest PDP of 0.73 fJ, indicating a significant 88.75 % reduction. Thus, the proposed D-PFSCL design scheme-4 2:1 MUX has the minimum propagation delay and PDP values in comparison to existing ones.
3. The proposed design scheme-4 achieves a maximum area reduction of 88 %, primarily due to a substantial decrease in transistor count along with the added benefits of memristor integration.

4.3 Overall comparison

This section puts forward comparison of D-PFSCL 2:1 MUX based on NOR/OR, multithreshold FC, TG, and both the proposed design schemes. The parameters namely gate count, STB count, transistor count, power consumption, propagation delay, PDP, memristor count, and area are taken for comparison. All the designs are evaluated under the same simulation conditions to ensure a fair comparison. The findings are comprehended in Table 4.5 and the following observations are made:

Table 4.5 Overall comparison for D-PFSCL 2:1 MUX in different design schemes

Scheme Parameter	NOR/ OR	Multithreshold FC	TG	Proposed design scheme-3	Proposed design scheme-4
Gate count	3	1	1	1	1
STB count	1	0	0	0	0
Transistor count	29	16	12	8	9
Power consumption (μ W)	9.5	2.43	2.42	2.42	2.4
Propagation delay (ps)	683	315	311	311	304
PDP (fJ)	6.48	0.77	0.75	0.75	0.73
Memristor count	-	-	-	6	4
Area (μm^2)	80.99	28.8	11.8	8.13	9.62

1. The D-PFSCL 2:1 MUX realization using NOR/OR based scheme has the highest gate count.
2. Both proposed schemes require fewer transistors than the existing counterparts, with proposed design scheme-3 exhibiting the lowest transistor count among all designs.
3. The propagation delay and power consumption are minimized in the proposed design Scheme-4 D-PFSCL 2:1 MUX. The results show that the proposed design Scheme-4 outperforms existing counterparts by 55.4 % in propagation delay 74.7 % in power consumption, respectively.
4. The D-PFSCL 2:1 MUX implemented using the NOR/OR scheme exhibits the highest PDP of 6.49 fJ, whereas the proposed scheme-4 design achieves the lowest PDP of 0.73 fJ, corresponding to a significant reduction of 88.75 %
5. The proposed design scheme-3 MUX attains a maximum area reduction of 90 %, mainly due to a significant reduction in transistor count and the advantages offered by memristor integration.

Further, the impact of process variations on all the existing and proposed designs for 2:1 MUX is studied through both Monte Carlo simulations and corner analysis. For Monte Carlo analysis, simulations are performed by varying the threshold voltage of MOS transistors with 5 % tolerance for 1000 runs and the findings for the results are listed in Table 4.6. The results shows that the proposed design scheme-4 D-PFSCL 2:1 MUX shows a minimum variation of 0.9 % and 3.5 % in power consumption and propagation delay respectively as compared to considered designs.

The performance of all considered designs is examined at TT, FF, SS, FS and SF corners. The observations are placed in Table 4.7. The best-case performance is obtained at FF design corner, and the worst-case performance is obtained at SS corner

in all the designs. It is found that the propagation delay, power consumption and PDP of the proposed design scheme-3 D-PFSCL 2:1 MUX varies by a factor of 0.56, 0.725 and 0.69 respectively between the best and the worst cases whereas the corresponding variation for the proposed design scheme-4 D-PFSCL 2:1 MUX are 0.61, 0.68 and 0.72 respectively.

Table 4.6 Monte Carlo results for different D-PFSCL 2:1 MUX

Parameter Scheme	Power consumption (μ W)			Propagation delay (ps)		
	Mean (μ)	SD (σ)	Variability (%)	Mean (μ)	SD (σ)	Variability (%)
NOR/OR	9.8	0.1	1.02	690	26.3	3.8
Multithreshold FC	2.5	0.03	1.2	320	20	6.2
TG	2.4	0.022	0.9	310	11.8	3.8
Proposed design scheme-3	2.4	0.022	0.9	310	11.8	3.8
Proposed design scheme-4	2.45	0.022	0.9	305	10.8	3.5

Table 4.7 Process corner analysis for different D-PFSCL 2:1 MUX

Corner	TT	FF	SS	FS	SF
Power consumption (μW)					
NOR/OR	9.5	13	8.7	11.1	10.61
Multithreshold FC	2.43	3.81	2.4	3.31	3
TG	2.42	2.56	1.97	2.46	2.22
Proposed design scheme-3	2.42	2.7	1.96	2.45	2.23
Proposed design scheme-4	2.4	2.9	1.99	2.66	2.31
Propagation delay (ps)					
NOR/OR	683	495	1022	589	811
Multithreshold FC	315	140	359	173	304
TG	311	241	430	273	386
Proposed design scheme-3	311	237	428	244	389
Proposed design scheme-4	304	238	432	244	390
PDP (fJ)					
NOR/OR	6.48	6.44	8.89	6.54	8.61
Multithreshold FC	0.77	0.53	0.86	0.57	0.91
TG	0.75	0.62	0.85	0.67	0.86
Proposed design scheme-3	0.75	0.64	0.84	0.60	0.87
Proposed design scheme-4	0.73	0.69	0.86	0.65	0.90

4.4 Design example

The effectiveness of the proposed design schemes is demonstrated through the design of a 4:1 MUX. It has two select lines (S_0, S_1) and four input lines (I_0, I_1, I_2, I_3), with its output, Q defined as:

$$Q = \overline{S_0} \overline{S_1} I_0 + \overline{S_0} S_1 I_1 + S_0 \overline{S_1} I_2 + S_0 S_1 I_3 \quad (4.37)$$

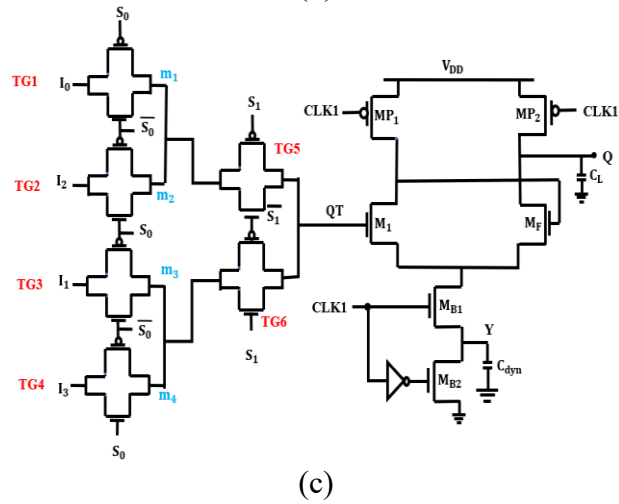
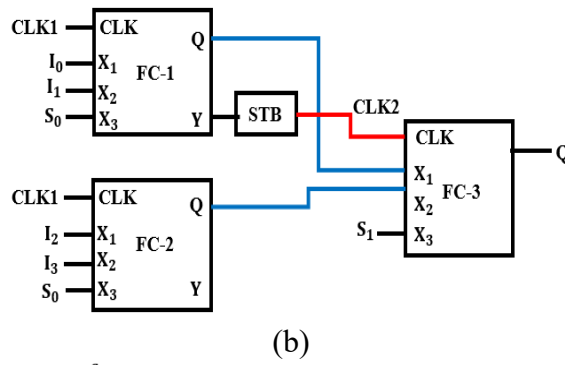
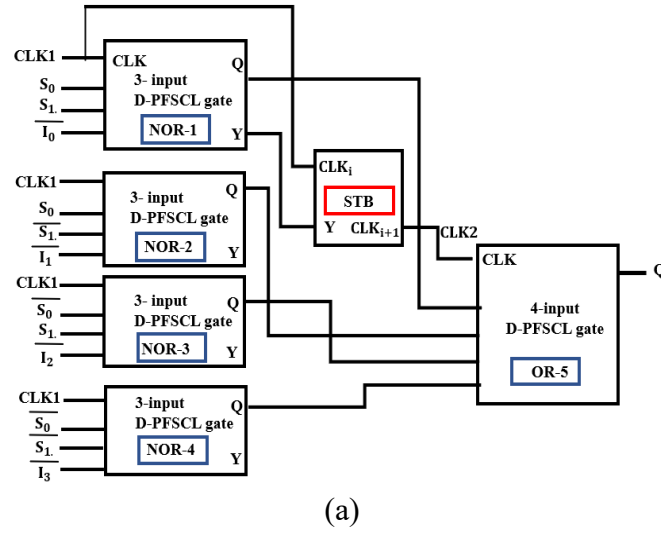
The realizations using existing NOR/OR, multithreshold FC and TG are shown in Fig. 4.11. The D-PFSCL 4:1 MUX based on NOR/OR scheme (Fig. 4.11(a)) uses two stages wherein the first stage uses four 3-input D-PFSCL NOR gates whose outputs are further fed to a 4-input D-PFSCL OR gate. It also employs an intermittent STB for proper operation. Similarly, the FC based realization of D-PFSCL 4:1 MUX as shown in Fig. 4.11(b) infers two stages due to the restriction of implementing only two minterms in a single gate. The TG based D-PFSCL 4:1 MUX employs single PFSCL gate as shown in Fig. 4.11(c). Here, TG1, TG2, TG3 and TG4 realize $\overline{S_0} I_0$, $S_0 I_2$, $\overline{S_0} I_1$ and $S_0 I_3$ respectively. These outputs are further provided to TG5 and TG6 controlled by S_1 . The output of TG5 and TG6 are further combined as QT to drive M_1 of the D-PFSCL buffer for 4:1 MUX functionality.

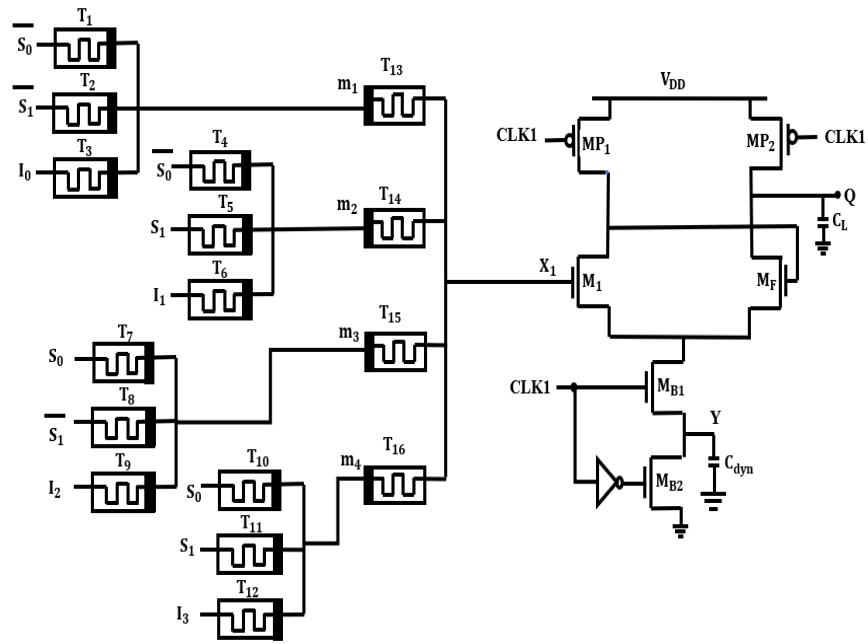
The D-PFSCL 4:1 MUX based on proposed design schemes 3 and 4 are shown in Fig. 4.11(d) and 4.11(e) respectively. In both the designs, the memristors ($T_1 - T_3$), ($T_4 - T_6$), ($T_7 - T_9$), ($T_{10} - T_{12}$) realize the minterms $\overline{S_0} \overline{S_1} I_0$, $\overline{S_0} S_1 I_1$, $S_0 \overline{S_1} I_2$ and $S_0 S_1 I_3$ respectively. These outputs are further combined by memristors ($T_{13} - T_{16}$), in accordance with design scheme-3 and the intermediate output is subsequently fed to the D-PFSCL buffer. In the proposed design scheme-4 D-PFSCL, the minterms output are directly fed as input to the 4-input D-PFSCL OR gate as shown.

The performance of considered D-PFSCL 4:1 MUX is compared on the basis various performance parameters and the findings are comprehended in Table 4.8. The following key observations can be drawn:

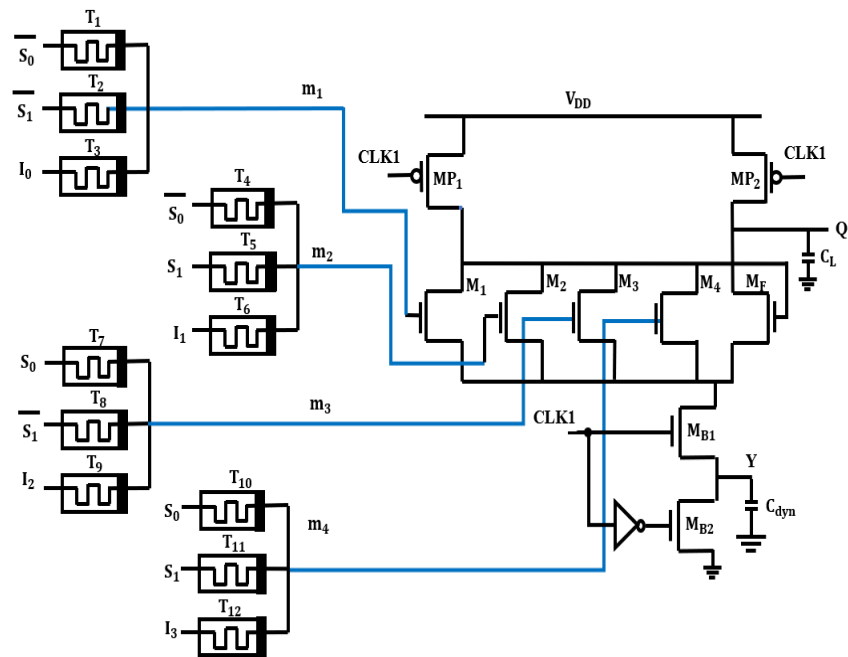
1. The transistor counts in 4:1 MUX realizations based on the proposed design schemes 3 and 4 is significantly lower as compared to existing counterparts.
2. The power consumption of TG based design and the proposed schemes is reduced by 75 % and 85 %, respectively, compared to their FC and NOR/OR based counterparts. This power advantage arises from single stage logic realization, in contrast to the multistage implementations used in FC and NOR/OR schemes.
3. Significant enhancements in propagation delay and PDP values are achieved as the proposed and TG based schemes implement the logic using a single gate. Reductions of 56 % in propagation delay and 93.4 % PDP are observed relative to the conventional NOR/ORbased scheme.
4. The D-PFSCL 4:1 MUX based on proposed scheme-3 occupies the smallest area while the one based on proposed scheme-4 offers the second best in this respect. An

overall area saving of at least 75 % with respect to TG based realization and maximum 94.4 % in comparison to the FC based counterparts is achieved.





(d)



(e)

Fig. 4.11 Realization of D-PFSCL 4:1 MUX using different scheme (a) NOR/OR (b) FC (c) TG (d) Proposed design scheme-3 (e) Proposed design scheme-4

Table 4.8 Performance comparison of different D-PFSCL 4:1 MUX

Scheme Parameter	NOR/ OR	Multithreshold FC	TG	Proposed design scheme	
				Scheme-3	Scheme-4
Gate count	5	3	1	1	1
STB count	1	1	0	0	0
Transistor count	48	50	20	8	11
Power consumption (μ W)	16.2	9.52	2.44	2.44	2.42
Propagation delay	705	568	317	317	311
PDP (fJ)	11.42	5.41	0.77	0.77	0.75
Memristor count	-	-	-	16	12
Area (μm^2)	131	147	32.9	8.13	15.08

4.5 Conclusion

This chapter presents two memristor aided design schemes for D-PFSCL style. The first proposed design scheme -3 uses a MBN in combination with a D-PFSCL inverter. The other design scheme-4 use the NOR/OR capability of D-PFSCL gate to further reduce the memristor count. The structure and the working of D-PFSCL 2:1 MUX realized using both the proposed schemes is presented which is followed by analysis of its voltage swing and delay. The functional verification of the two proposed D-PFSCL 2:1 MUX designs and their performance comparison with the existing designs is carried out using PTM 90 nm CMOS technology node parameters and TiO₂ memristor model. It is found that the proposed design scheme-3 D-PFSCL 2:1 MUX significantly reduces the area by 90 % in comparison with existing counterparts, however, the proposed design scheme-4 D-PFCSL 2:1 MUX outperforms existing counterparts by 55.4 %, 74.7 %, and 88.75 % in terms of propagation delay, power consumption, and PDP respectively. Simulations are also carried out for D-PFSCL 4:1 MUX and through comparison with existing D-PFSCL MUX, it is observed that proposed design scheme-4 MUX leads to maximum reduction of 56 %, 85 % and 94.46 % in propagation delay, power consumption and PDP respectively. Further, the robustness of proposed D-PFSCL gates using both existing and proposed design schemes is evaluated under process variations using Monte Carlo simulations and corner analysis, which confirm correct functionality across all design schemes. Overall, the proposed design schemes provide a simple and efficient approach for designing low-power and area-efficient D-PFSCL circuits.

CHAPTER 5

PFSCCL REGISTERS

5.1 Introduction

PFSCCL circuits have been widely employed in digital communication systems as well as in arithmetic and logic applications [60–78]. Registers play a crucial role in digital circuits by enabling functions such as data storage, data manipulation, and temporary data buffering in high-performance computing systems used for SoC realizations, as well as in digital signal processing applications including filtering, encoding, decoding, and arithmetic unit design [117-118]. Conventional CMOS registers suffer from high switching noise and do not provide an analog-friendly environment in mixed-signal applications. In addition, their significant power consumption at high operating frequencies remains a concern. However, comparatively little research has been directed toward the design of PFSCCL registers. Therefore, this chapter focus on the design of PFSCCL registers, that can be employed in digital circuit design in mixed signal application.

This chapter first explains the register design approach, followed by the proposed static and dynamic PFSCCL register designs. The design approach involves switch and sleep based PFSCCL tristate buffer approaches implemented in a master slave configuration. These register designs are referred to as static and dynamic register designs, respectively. The operation of both the proposed register designs is verified through simulation results to ensure proper functionality and the performance of the proposed register designs is compared. Additionally, the issue of clock overlap arising from unequal clock routing paths is addressed, and methods to achieve clock skew insensitive operation in PFSCCL registers are proposed. Finally, the implementation of a serial-in serial-out (SISO) shift register validates the feasibility of the proposed register designs at the system level.

5.1.1 Register design approach

The PFSCCL registers design approach employs two D-latch in a master slave configuration. The generic diagram of a positive edge triggered PFSCCL register is illustrated in Fig. 5.1. The master D-latch output reflects the respective changes in the input but are not transferred until the rising edge of a CLK signal. At the transition, the master D-latch transfers the data to the positive level sensitive slave D-latch, which retains the data until the next rising transition of the CLK signal.

The D-latch is designed by employing PFSCCL tristate buffer as explained in Chapter 2. As there are two categories namely switch and sleep based PFSCCL tristate buffer available in literature [83-84] therefore, so the register designs for both the categories

is presented. Further, the static and dynamic register designs in each category is discussed for the sake of completeness.

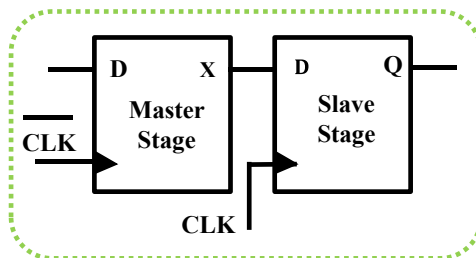


Fig. 5.1 Block diagram of master slave configuration for PFSCl register design

5.2 Proposed switch based PFSCl register designs

In this section, switch based tristate buffer is used to design registers based on the master slave configuration depicted in Fig. 5.1. The design of static registers is first explained, followed by the design of dynamic registers.

5.2.1 Static PFSCl registers

In this subsection, the design of static registers is elucidated. Three switch based tristate buffer topologies 2-4 presented in section 2.4.1 are used to design positive edge triggered switch based static PFSCl registers. The corresponding static register designs are referred to as SR-1 to SR-3. The MOS based schematic of SR-1 to SR-3 is depicted in Fig. 5.2. In all three designs, master stage comprises of tristate buffers PB1 and PB2 whereas PB3 and PB4 form the slave stage. The operation of the registers is explained by considering SR-1 register design as shown in Fig. 5.2(a). For a low value of CLK signal, transistors M_6 and M_7 are ON, while M_{13} and M_{14} are OFF, causing PB1 to operate as regular buffer and PB2 to remain in a high impedance state. In this condition, the changes in input data D are reflected at node X and are not transferred to the final output node, Q as PB3 operates in a high impedance state. The register, however, maintains its last state at final output node, Q due to the feedback connection of enabled PB4 tristate buffer. As the CLK signal makes a low to high transition, PB2 and PB3 gets enabled. The last output value of PB1 is thus maintained by PB2 which is further fed as input to PB3 and gets reflected at final output node, Q. It is worth mentioning that the proposed SR-1 register design necessitates a higher bias voltage to maintain the same current value I_{SS} due to the stacking of PMOS transistor below the current source. This voltage headroom is avoided in proposed SR-2 register design by placing PMOS transistors above corresponding current sources in each tristate buffer depicted in Fig. 5.2(b).

The proposed static register (SR-3) presents an alternate topology wherein the availability of bias voltage of the current source is made dependent on either CLK or $\overline{\text{CLK}}$ signal by using a PMOS transistor and a NMOS transistor of tristate buffers as

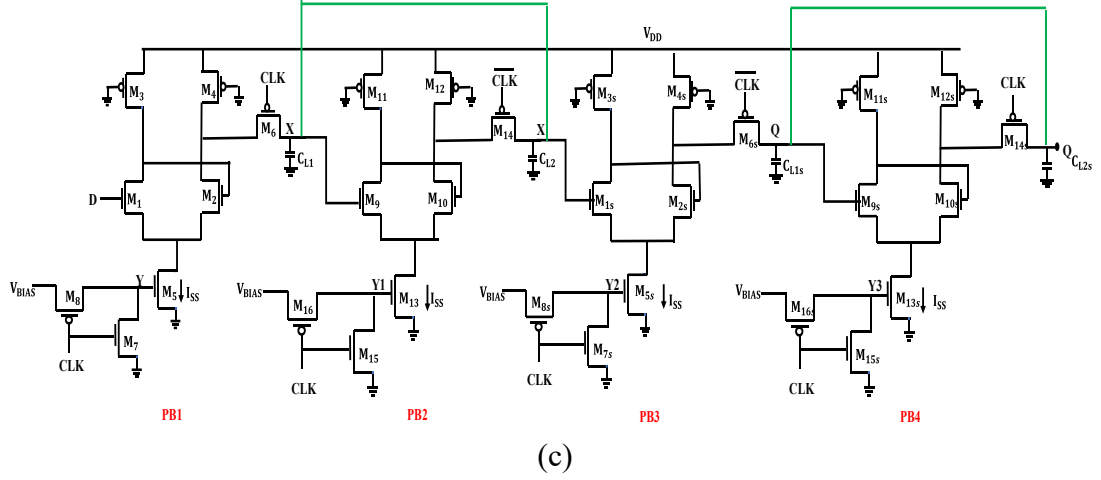


Fig. 5.2 Proposed switch based static PFSCCL registers (a) SR-1(b) SR-2 (c) SR-3

5.2.2 Dynamic PFSCCL registers

The design of dynamic PFSCCL registers works on temporary storage of charge and eliminates the presence of feedback mechanism to retain the data [117-118]. Thus, the dynamic PFSCCL register does not require the tristate buffers PB2 and PB4, which are used in the static PFSCCL registers (Fig. 5.2). The dynamic PFSCCL registers therefore require only two tristate buffers.

Three switch based positive edge triggered dynamic PFSCCL registers named as DR-1 to DR-3 are presented. The MOS based schematics of DR-1 to DR-3 are depicted in Fig. 5.3. In all three designs, master stage comprises of tristate buffers PBd1 while PBd2 forms slave stage. The PFSCCL DR-1 (Fig. 5.3(a)) use (Topology 2 [83]) that modifies the current source section of both the tristate buffers by inserting a PMOS transistor below the current source to control the flow of current for reduced power consumption. The topology suffers from high voltage headroom required to operate the current source. This drawback is eliminated in proposed DR-2 register (Fig. 5.3(b)) design by placing PMOS transistors above corresponding current sources in PBd1 and PBd2 in accordance with (Topology 3 [83]). The DR-3 register design is based on controlling the availability of bias voltage for a current source suggested as (Topology 4 [83]) as shown in Fig. 5.3(c). The operation of the proposed register can be explained for different values of CLK signal. For a low value of CLK signal, tristate buffer PBd1 is enabled and the corresponding changes at input D, are propagated to node X. As tristate buffer PBd2 is in high impedance, the voltage of node Q does not change. Subsequently, when the CLK signal becomes high, PBd1 enters into high impedance state and PBd2 gets enabled. The node voltage of X propagates to final output node Q, confirming the functionality of a positive edge triggered register.

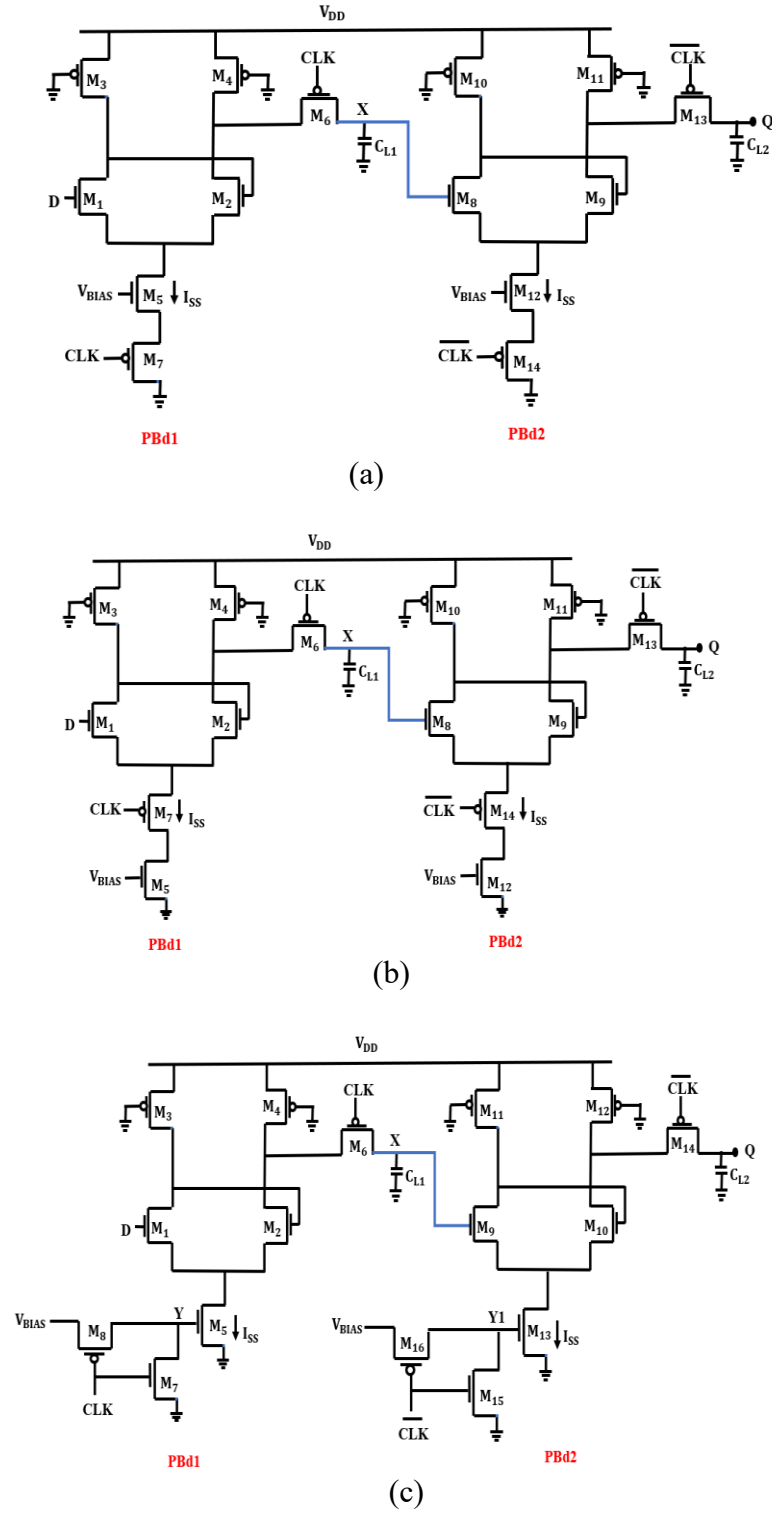
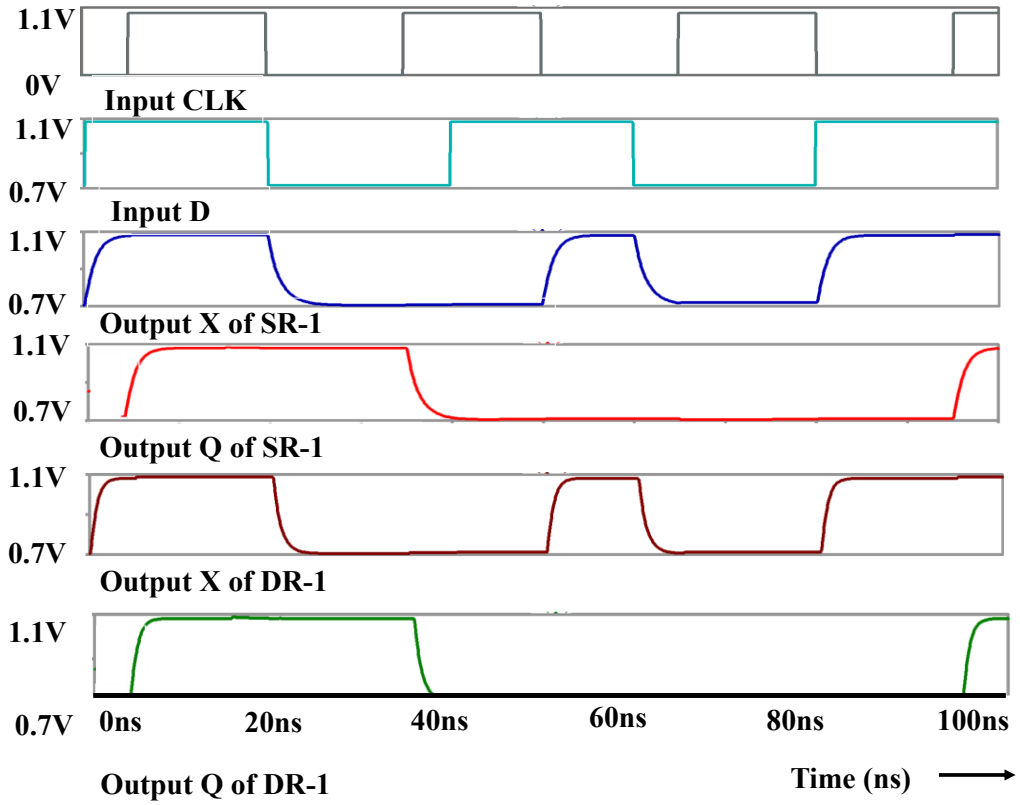


Fig. 5.3 Proposed switch based dynamic PFSCCL registers (a) DR-1 (b) DR-2 (c) DR-

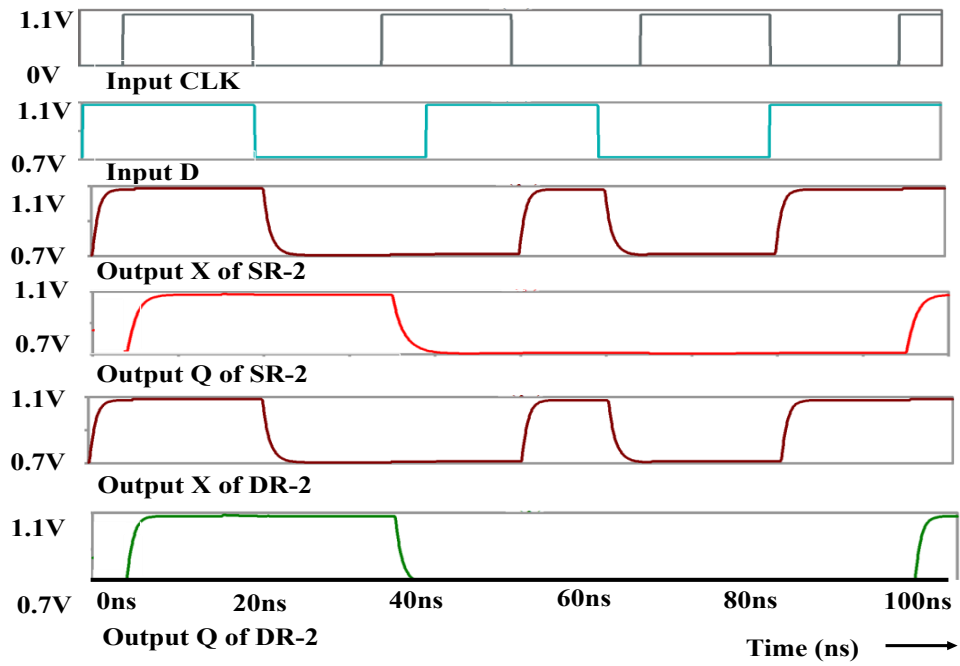
5.2.3 Simulation Section

In this section, the functionality of the proposed switch based static and dynamic PFSCl registers is verified through simulations in LTspice using PTM 90nm CMOS technology parameters. The V_{DD} , I_{SS} , V_{SWING} and C_L of 1.1 V, 400 μ A, 100 μ V and 50 fF, respectively, are taken. Furthermore, a comparative analysis between the proposed switch based static and dynamic PFSCl registers is carried out to evaluate their relative performance.

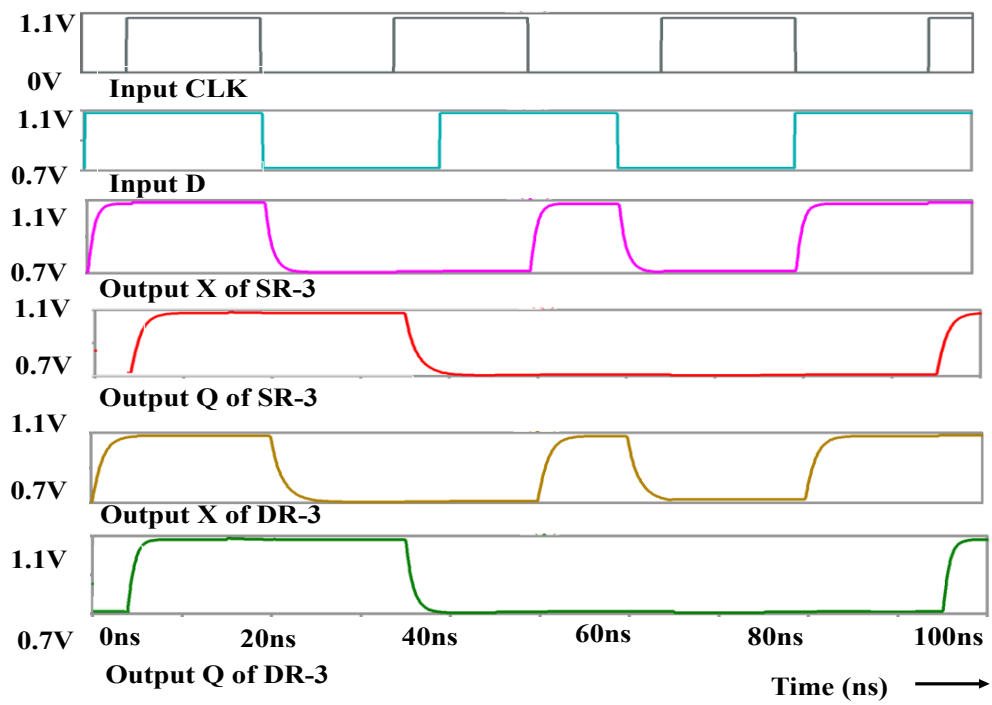
The timing waveforms with inputs D, CLK, node X and final output node, Q for proposed switch based static and dynamic PFSCl registers are shown in Fig. 5.4. It can be observed that for low voltage value of CLK signal, the changes in input D are reflected at node X, however the changes are not further transferred to final output node, Q. Further, during a low to high transition of CLK signal, the last value of node X is maintained and is available at final output node, Q. Thus, the timing waveforms conform to the functionality of a positive edge triggered register.



(a)



(b)



(c)

Fig. 5.4 Timing waveforms of proposed switch based positive edge triggered PFSCCL registers

Table 5.1 Performance comparison of proposed switch based 1-bit positive edge triggered PFSCCL registers

Parameter Register design	Propagation delay (ps)	Power consumption (μW)	PDP (fJ)	Transistor count
SR-1	911	220	200.42	28
SR-2	899	220	197.78	28
SR-3	928	220	204.16	32
DR-1	676	110	74.36	14
DR-2	655	110	72.05	14
DR-3	758	110	83.38	16

A performance comparison is drawn and the results are summarized in Table 5.1. The following observations are made from the results:

1. Among all proposed static register designs, SR-2 gives the best performance. It shows maximum reduction of 3.1 % in propagation delay and PDP and 12.5 % reduction in transistor count as compared to SR-3, while maintaining the same power consumption. This improvement is attributed to its optimized PFSCCL tristate buffer topology as suggested in [83], which reduces the internal node capacitances, enabling faster switching and shorter output enable time, thereby resulting in reduced propagation delay.
2. The dynamic register DR-2 demonstrates the best performance among all the proposed PFSCCL dynamic register designs, achieving a maximum reduction of 13.6 % in propagation delay and PDP, along with a 12.5 % reduction in transistor count as compared to DR-3, while maintaining the same power consumption. This improvement arises because static PFSCCL registers use four tristate buffers, whereas the dynamic design requires only two PFSCCL tristate buffers and also uses the optimized PFSCCL tristate buffer topology, as suggested in [83].
3. The proposed dynamic registers offer significantly better performance than proposed static register designs, observing 50 % lower power consumption due to the requirement of less no of PFSCCL tristate buffer for the implementation of PFSCCL dynamic registers. In addition, DR-2 achieves 27 % lower propagation delay and 63.5 % lower PDP compared to SR-2. This improvement is attributed to the operating principle of dynamic circuits, where current flows only during clocked operation, unlike static circuits where current continuously flows.

Overall, SR-2 and DR-2 exhibit the best performance among all the proposed static and dynamic register designs. Hence, these designs are chosen for area evaluation.

LAYOUTS of SR-2 and DR-2 are drawn in Microwind and are shown in Fig. 5.5. The area of SR-2 is found to be $2366 \mu\text{m}^2$, while that of DR-2 is $1050 \mu\text{m}^2$, indicating area efficiency of the latter.

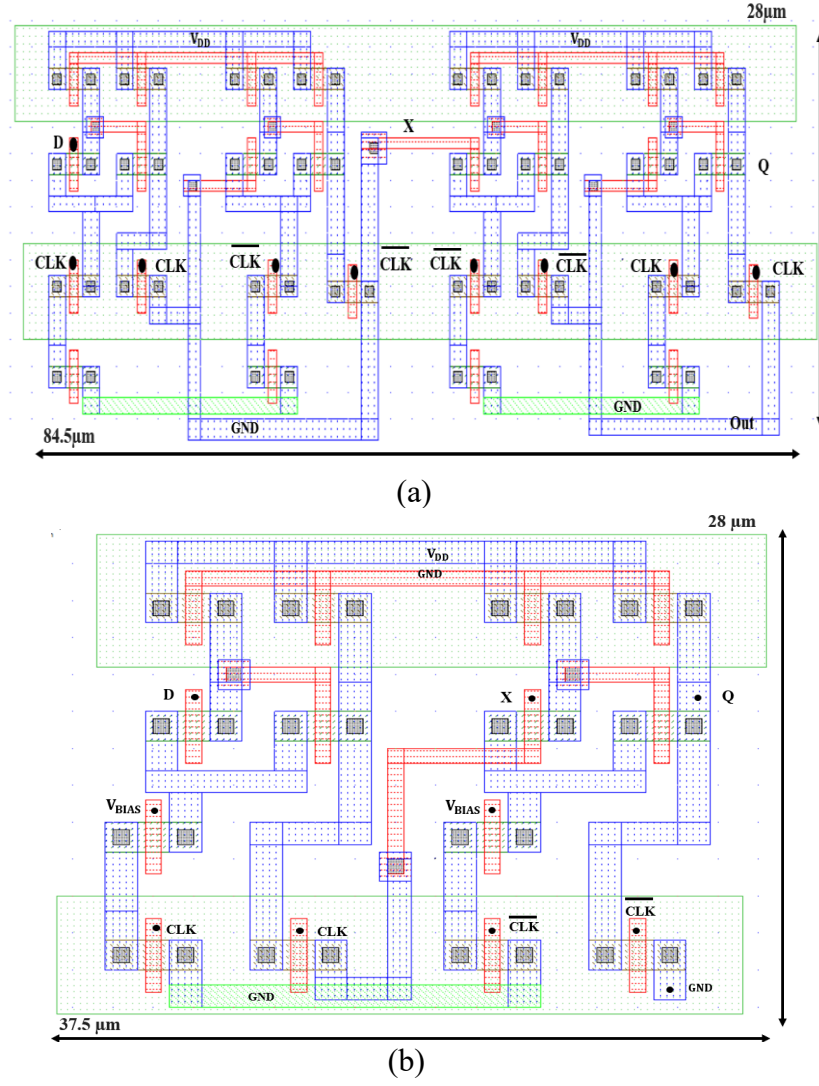


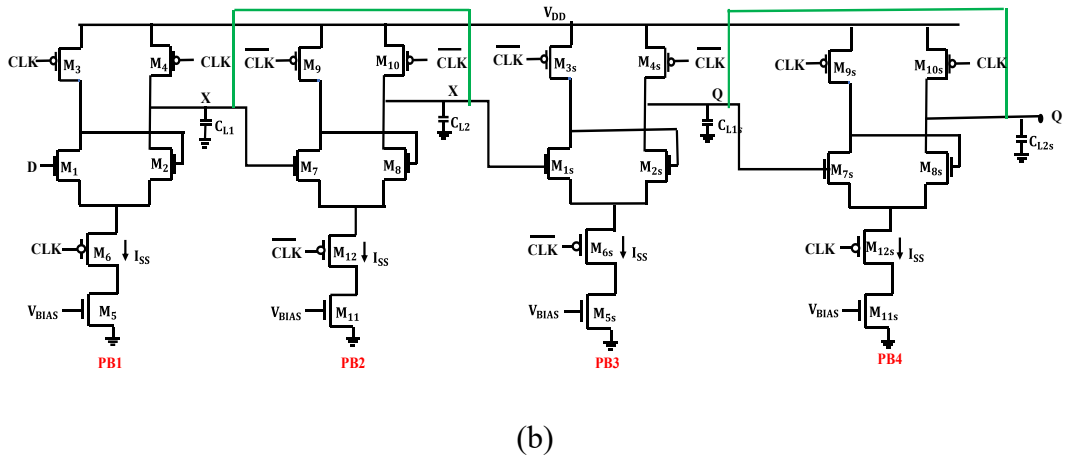
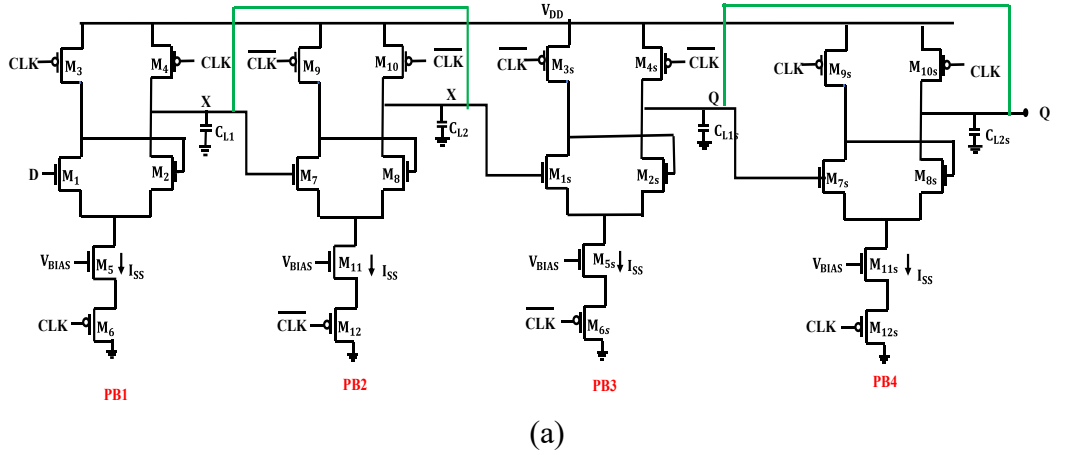
Fig. 5.5 Layout of proposed switch based positive edge triggered PFSCl registers
(a) SR-2 (b) DR-2

5.3 Proposed sleep based PFSCl register designs

This section presents sleep based PFSCl register design by employing sleep based tristate buffers in the master slave configuration depicted in Fig. 5.1. The design and operation of sleep based static registers is explained which is followed by dynamic registers.

5.3.1 Static PFSCl registers

In this subsection, the design of static registers is elucidated. Three sleep based tristate buffer Topologies 8-10 presented in section 2.4.2 are used to design sleep based positive edge triggered static PFSCl registers are named as SR-4 to SR-6. The MOS based schematic of SR-4 to SR-6 with master stage comprising of tristate buffers PB1, PB2 and the slave stage having PB3 and PB4 are depicted in Fig. 5.6. In the registers, a low value of CLK enables PB1 and disables PB2 that allows changes at input D to propagate to node X. The changes at node X are not further propagated to final output node, Q as PB3 is disabled. During this time, the previous output at node Q is maintained because PB4 remains enabled, which keeps the feedback path active. Subsequently, when CLK assumes high value, PB1, PB4 are disabled and PB2, PB3 are enabled. This prevents the changes at input D to propagate to node X, however, the last voltage level at node X is obtained at final output node, Q through PB2, PB3. It is worth mentioning that the above three sleep based static PFSCl register designs have feedback to store the last output. Therefore, another design that avoids feedback connection in sleep based static PFSCl registers is presented in the next subsection.



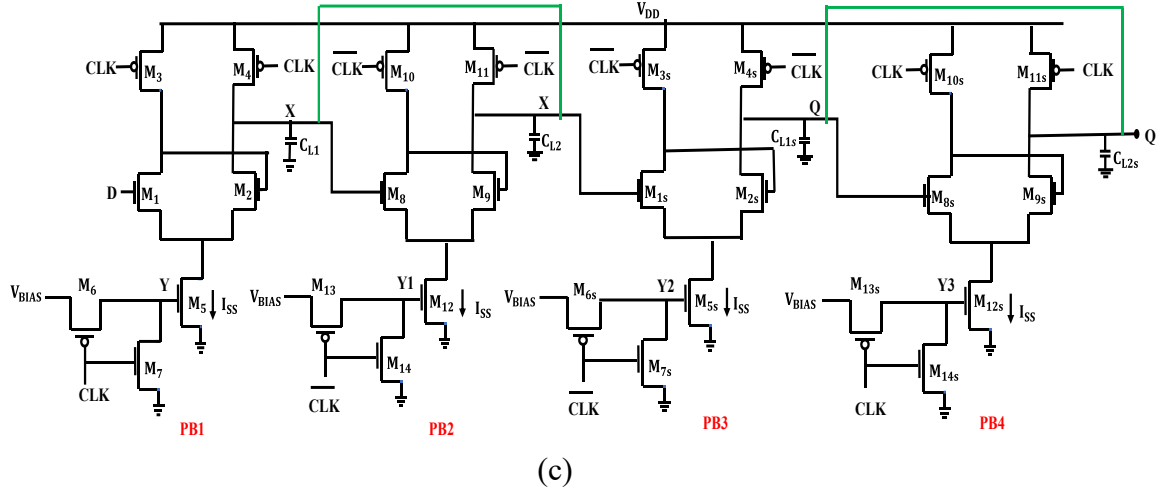


Fig. 5.6 Proposed sleep based static PFSCSCL registers (a) SR-4 (b) SR-5 (c) SR-6

5.3.2 Dynamic PFSCSCL registers

The design of dynamic PFSCSCL registers eliminates the presence of feedback mechanism to retain the data. It is based on temporary storage of charge and reduces the tristate buffers count in comparison to the static PFSCSCL registers (Fig. 5.6).

Three sleep based positive edge triggered dynamic PFSCSCL registers named as DR-4 to DR-6 are presented. The MOS based schematics of DR-4 to DR-6 are depicted in Fig. 5.7. In all three designs, master stage comprises of tristate buffers PBd1 while PBd2 forms slave stage. The PFSCSCL DR-4 use (Topology 8 [84]) that modifies the current source section of both the buffers by inserting a PMOS transistor below the current source to control the flow of current for reduced power consumption. The topology suffers from high voltage headroom required to operate the current source. This drawback is eliminated in proposed DR-5 register design by placing PMOS transistors above corresponding current sources in PBd1 and PBd2 in accordance with (Topology 9 [84]). The DR-3 register design is based on controlling the availability of bias voltage for a current source suggested as (Topology 10 [84]). The operation of the proposed register can be explained for different values of CLK signal. For a low value of CLK signal, tristate buffer PBd1 is enabled and the corresponding changes at input D are propagated to node X. As tristate buffer PBd2 is in high impedance, the voltage of node Q does not change. Subsequently, when the CLK signal becomes high, PBd1 enters into high impedance state and PBd2 gets enabled. The node voltage of X propagates to final output node, Q confirming the functionality of a positive edge triggered register.

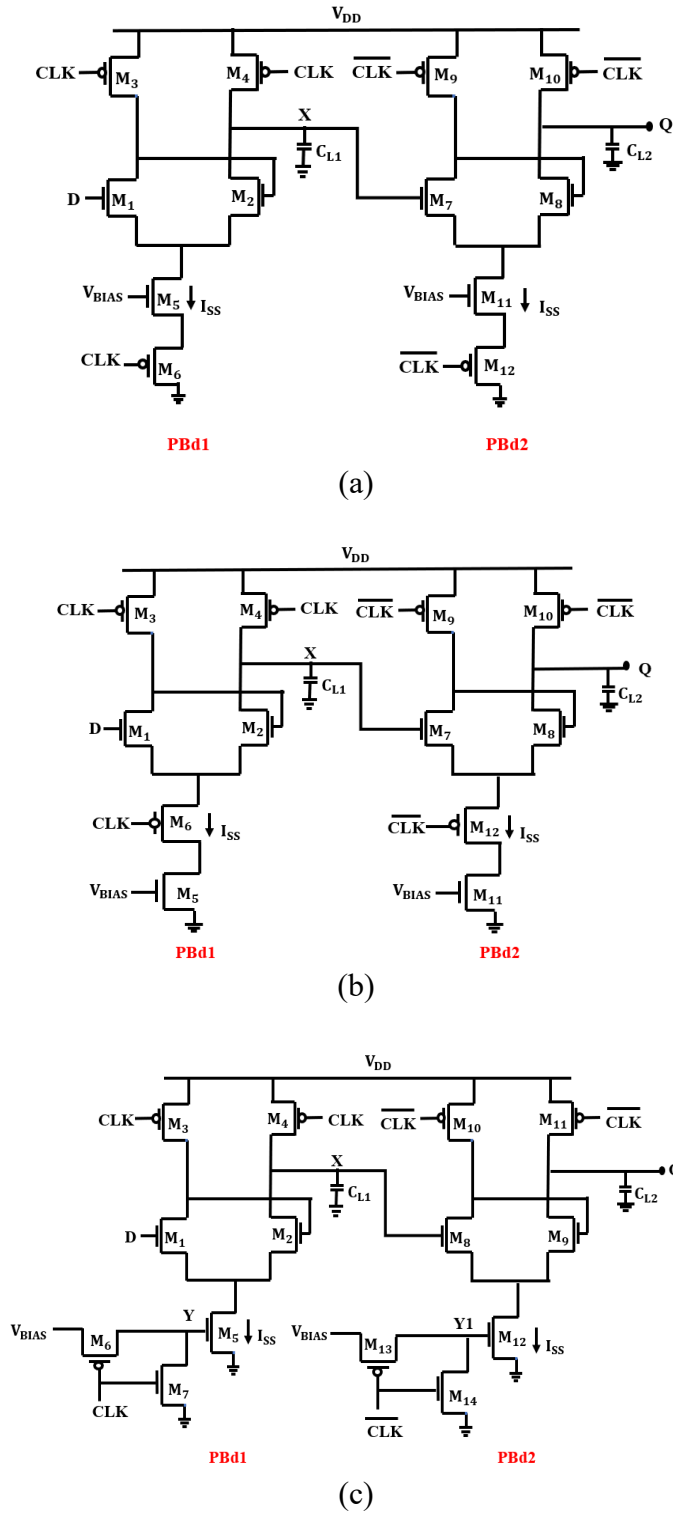
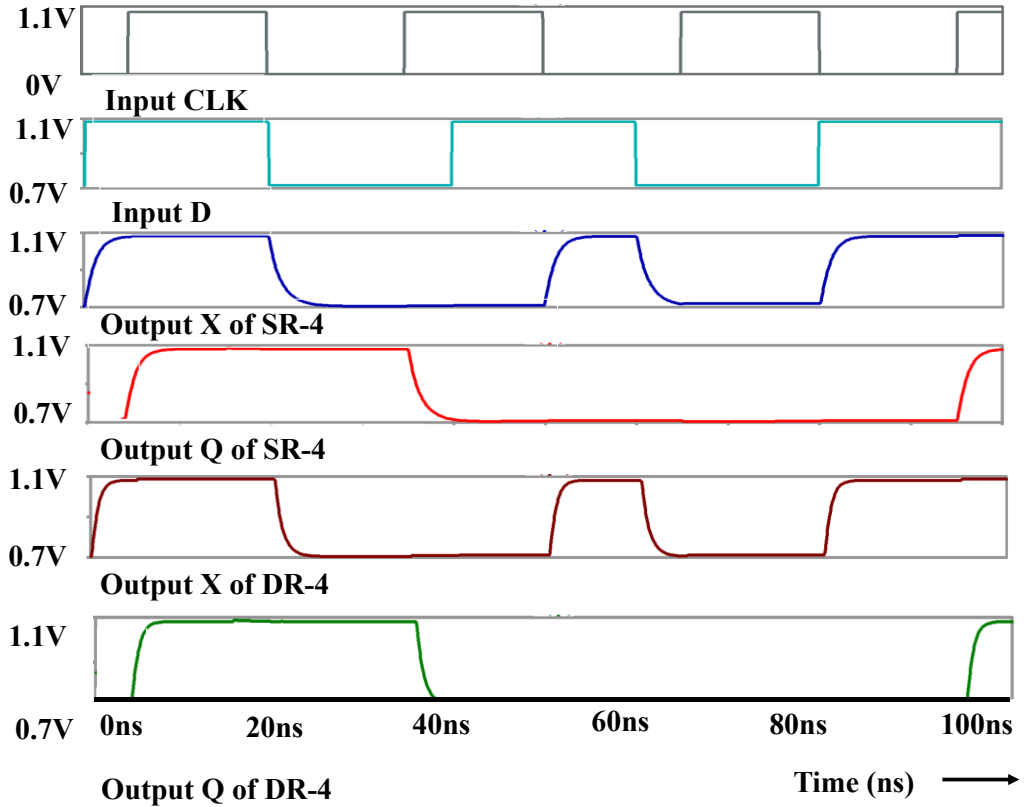


Fig. 5.7 Proposed sleep based dynamic PFSCCL registers (a) DR- 4 (b) DR-5 (c) DR-6

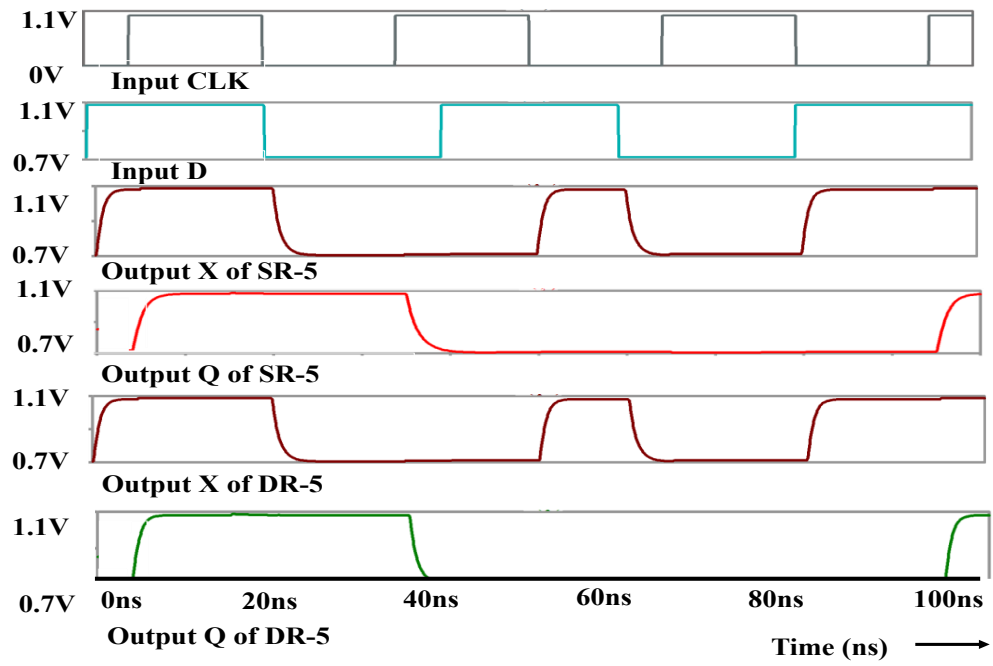
5.3.3 Simulation section

In this section, the functionality of the proposed sleep based PFSCCL registers is verified by implementing and simulating in LTspice using PTM 90nm CMOS technology parameters. The same simulation environment as considered for switch based proposed register designs is used for the sleep based proposed register designs. Furthermore, a comparative analysis between the proposed sleep based static and dynamic PFSCCL registers is carried out to evaluate their relative performance.

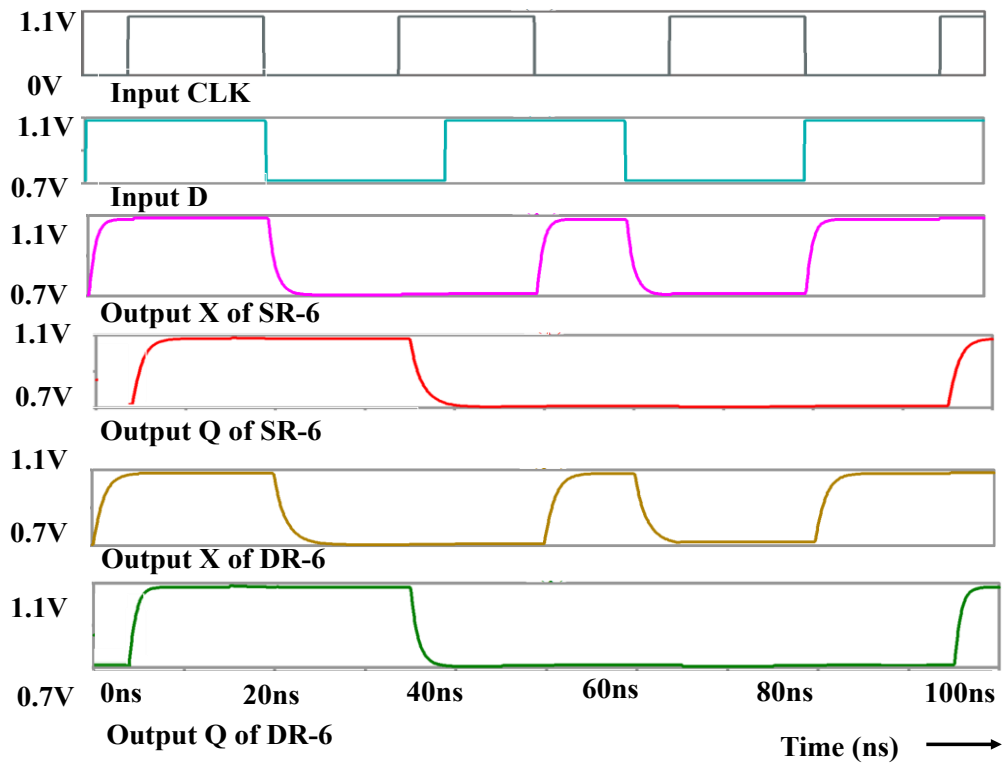
The timing waveforms showing input data D, CLK, intermediate master stage output X and final output node, Q for sleep based static and dynamic PFSCCL registers are shown in Fig. 5.8. It can be observed that for low value of CLK signal, the changes in input data, D are available at output, X and these changes are not further reflected at the final output node, Q in all the proposed registers. Further during a low to high transition of CLK signal, the last stored value at node X is made available at final output node, Q through the slave stage. Thus, all the proposed register designs exhibit the correct functionality.



(a)



(b)



(c)

Fig. 5.8 Timing waveforms of proposed sleep based positive edge triggered PFSCCL registers

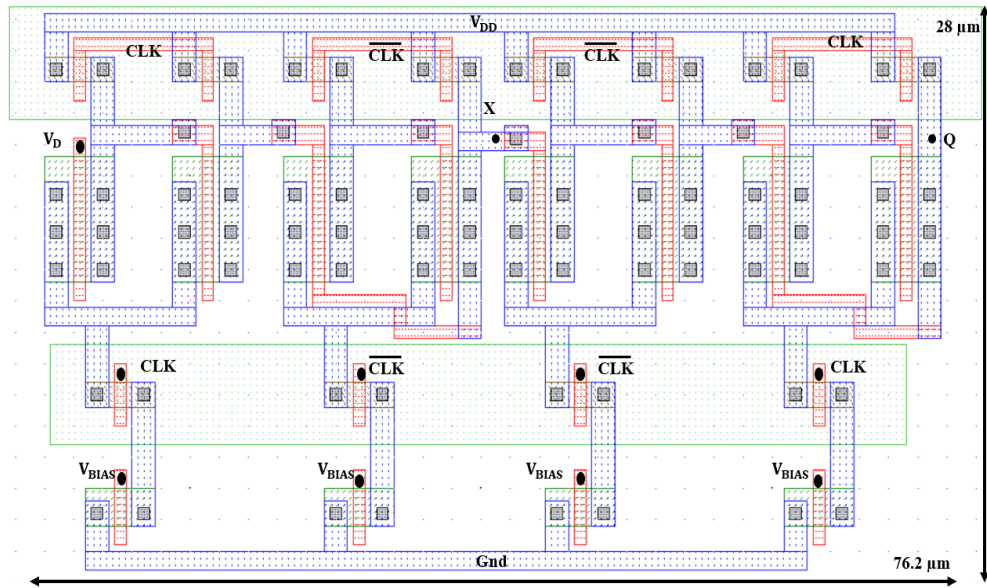
Table 5.2 Performance comparison of proposed sleep based 1-bit positive edge triggered PFSCCL registers

Register design \ Parameter	Propagation delay (ps)	Power consumption (μW)	PDP (fJ)	Transistor count
SR-4	807	220	177.54	24
SR-5	798	220	175.56	24
SR-6	829	220	182.38	28
DR-4	559	110	61.49	12
DR-5	542	110	59.62	12
DR-6	639	110	70.29	14

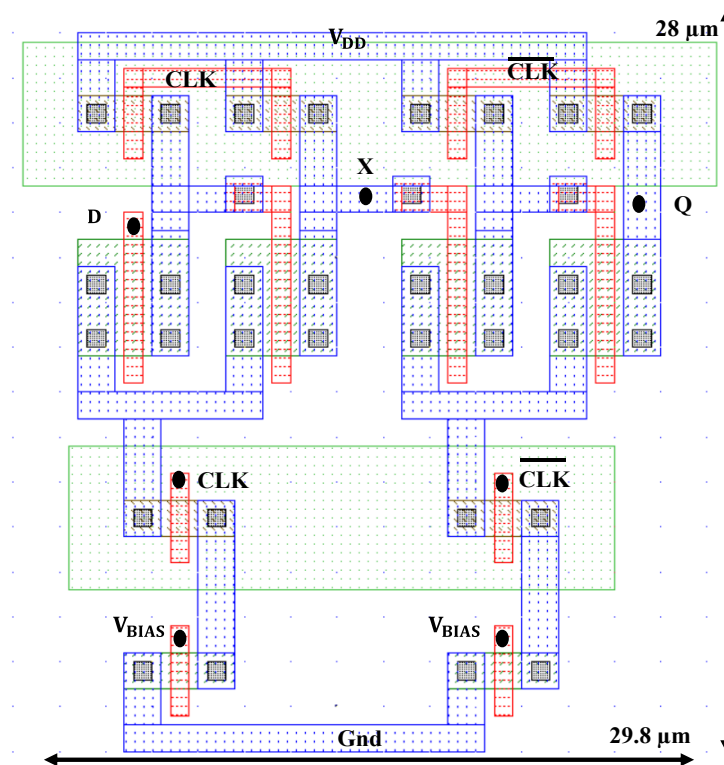
A performance comparison is performed and results are reported in Table 5.2 the following observations are made from the results

1. Among the sleep based static register designs, SR-5 gives the best performance. It shows about 3.73 % reduction in propagation delay and PDP and 14.28 % reduction in transistor count, while maintain the same value of power consumption as compared to SR-6.
2. The PFSCCL sleep based dynamic register, DR-5 performs the best among all proposed dynamic register designs. It observes maximum reduction of 15.17 % in propagation delay and PDP and 14.28 % reduction in transistor count while maintain the same value of power consumption as compared to DR-6.
3. The sleep based dynamic register DR-5 demonstrates the best performance among all proposed registers, outperforming the static register SR-5. It achieves 50 % lower power consumption due to the use of only two PFSCCL tristate buffers, compared to four in the static register design, along with a 50 % reduction in transistor count. Furthermore, DR-5 shows a 32.1 % reduction in propagation delay and a 66 % reduction in PDP compared to SR-5. This improvement is attributed to the dynamic operation, where current flows only during clocked evaluation, whereas static circuits maintain continuous current flow.

Overall, SR-5 and DR-5 show the best performance among all the proposed register designs. Further, area is calculated for the SR-5 and DR-5 register designs. Layouts of SR-5 and DR-5 are drawn in Microwind and are shown in Fig. 5.9. The area of SR-5 is found to be 2134 μm^2 , while DR-5 occupies 834 μm^2 , which shows about 60.9 % reduction in area for the dynamic register design compared to the static register design.



(a)



(b)

Fig. 5.9 Layout of proposed sleep based dynamic positive edge triggered PFSCSCL registers (a) SR-5 (b) DR-5

5.4 Overall performance

The overall performance comparison of all the proposed switch and sleep based static and dynamic PFSCl 1-bit registers is carried out using LTspice with PTM 90 nm CMOS technology parameters. The V_{DD} , I_{SS} , V_{SWING} and C_L of 1.1V, 400mV, 100 μ A and 50fF respectively are taken. Furthermore, a comparative analysis between the proposed switch and sleep based static and dynamic PFSCl registers is carried out to evaluate their relative performance. The results are reported in Table 5.3 and the following observations are made:

1. The performance of dynamic PFSCl registers is better than static registers. This superior performance is attributed to the dynamic circuit operation, where current flows only during clocked evaluation, avoiding continuous current paths present in static circuits, thereby reducing internal capacitances and improving overall speed and energy efficiency.
2. Among all proposed static PFSCl register designs, SR-5 exhibits the best performance. It enjoys maximum reduction of 14 % in propagation delay and PDP, and lower transistor count of 25 % compared to SR-3. This advantage stems from the fact that SR-5 uses an optimized PFSCl tristate buffer topology with reduced internal node capacitances and lower circuit complexity, which enables faster switching and reduced propagation delay.
3. The proposed dynamic PFSCl register design DR-5 demonstrates the best performance, achieving a maximum reduction of 13.6 % in both propagation delay and PDP, along with a 25 % reduction in transistor count compared to DR-3.
4. The performance of static register design SR-5 is best among static registers. As compared to SR-5, DR-5 exhibits 17.9 % reduction in propagation delay, 59 % lower PDP, 50 % lower power consumption, and a 50 % reduction in transistor count.

Overall, the dynamic register DR-5 outperforms all static and dynamic designs, offering the lowest propagation delay and PDP, along with significant reductions in power consumption and transistor count.

Table 5.3 Overall performance comparison of proposed switch and sleep based static and dynamic PFSCl registers

Parameter Register design	Propagation delay (ps)	Power consumption (μW)	PDP (fJ)	Transistor count
SR-1	911	220	200.42	28
SR-2	899	220	197.78	28
SR-3	928	220	204.16	32
SR-4	807	220	177.54	24
SR-5	798	220	175.56	24
SR-6	829	220	182.38	28

DR-1	676	110	74.36	14
DR-2	655	110	72.05	14
DR-3	758	110	83.38	16
DR-4	676	110	74.36	12
DR-5	655	110	72.05	12
DR-6	758	110	83.38	14

Further, the impact of process variations on propagation delay of proposed switch- and sleep based static and dynamic 1-bit PFSCl registers is studied through Monte Carlo simulation and corner analysis. The threshold voltage of MOS transistors with 5 % tolerance for 1000 runs. The obtained Monte Carlo simulation results are listed in Table 5.4. Overall, when comparing static and dynamic register designs, the proposed DR-5 register exhibits the lowest variations in propagation delay of 2.8 %

The process corner analysis results for performance parameters of proposed switch- and sleep based static and dynamic 1-bit PFSCl registers is performed and the statistical parameters are mentioned in Table 5.5 confirm that all the proposed register designs function correctly across all corners. In the proposed designs, the best and worst performances are observed at the FF and SS corners, respectively. It is found that the propagation delay, power consumption, and PDP of the proposed SR-5 vary by a factor of 0.58, 0.81 and 0.69 respectively between the best and the worst cases whereas the corresponding variation for the DR-5 is 0.37, 0.81 and 0.45 respectively. The results indicate the robustness and reliability under diverse operating conditions of the registers with DR as more tolerant to variations.

Table 5.4 Monte Carlo results for propagation delay of proposed switch and sleep based static and dynamic PFSCl registers

Parameter Register design	Mean (μ) (ps)	SD (σ) (ps)	Variability (%)
SR-1	920	40	4.35
SR-2	910	38	4.18
SR-3	935	42	4.49
SR-4	815	35	4.29
SR-5	800	32	4
SR-6	835	36	4.31
DR-1	688	22.1	3.21
DR-2	666	19.9	2.98
DR-3	754	33.3	4.41
DR-4	690	24.5	3.55
DR-5	650	18.2	2.8
DR-6	770	35.8	4.65

Table 5.5 Process corner analysis of proposed switch and sleep based static and dynamic PFSCCL registers

Corner Register design	TT	FF	SS	FS	SF
Power consumption (μW)					
SR-1	220	242	198	220	220
SR-2	220	242	198	220	220
SR-3	220	242	198	220	220
SR-4	220	242	198	220	220
SR-5	220	242	198	220	220
SR-6	220	242	198	220	220
DR-1	110	121	99	110	110
DR-2	110	121	99	110	110
DR-3	110	121	99	110	110
DR-4	110	121	99	110	110
DR-5	110	121	99	110	110
DR-6	110	121	99	110	110
Propagation delay (ps)					
SR-1	911	850	1480	1305	1360
SR-2	899	834	1423	1260	1314
SR-3	928	870	1505	1330	1388
SR-4	807	760	1302	1155	1208
SR-5	798	745	1275	1120	1180
SR-6	829	780	1350	1195	1255
DR-1	676	352	922	511	774
DR-2	655	325	867	478	733
DR-3	758	383	1155	523	778
DR-4	676	340	905	500	760
DR-5	655	315	850	470	720
DR-6	758	370	1100	515	770
PDP (fJ)					
SR-1	200.42	205.70	293.04	287.10	299.20
SR-2	197.78	201.83	281.75	277.20	289.08
SR-3	204.16	210.54	297.99	292.60	305.36
SR-4	177.54	183.92	257.80	254.10	265.76
SR-5	175.56	180.29	252.45	246.40	259.60
SR-6	182.38	188.76	267.30	262.90	276.10
DR-1	74.36	42.59	91.28	56.21	85.14
DR-2	72.05	39.33	85.83	52.58	80.63
DR-3	83.38	46.34	114.35	57.53	85.58

DR-4	74.36	41.14	89.60	55.00	83.60
DR-5	72.05	38.12	84.15	51.70	79.20
DR-6	83.38	44.77	108.90	56.65	84.70

5.5 Design example

The use of proposed PFSCl register is extended to the design of a 3-bit PFSCl serial in serial out shift register (SISO). The block diagram is drawn in Fig. 5.10(a) for illustration. The 3-bit SISO register design connects three positive edge triggered registers (K1, K2 and K3) in series with the output of the first register, K1 being fed as input to second register, K2 and so on. The circuit diagram of the 3-bit SISO register employing proposed PFSCl dynamic register design (DR-5) (Fig.5.7(b)) is shown in Fig. 5.10(b). For a low value of CLK signal, the tristate buffers PBd1, PBd3, PBd5 in K1, K2 and K3 are respectively enabled while PBd2, PBd4, PBd6 in K1, K2 and K3 remains in high impedance state. In this condition, the changes at the respective input nodes are available at the intermediate nodes but are not transferred to final output node, Q in each K1, K2 and K3 registers. Conversely, for a high value of CLK signal, the PB1, PB3, PB5 exhibits hold state while PB2, PB4, PB6 provides the last value at their intermediate nodes as the output of K1, K2 and K3 registers. Thus, the data stored in each register is transferred to the next register in chain as the next CLK arrives.

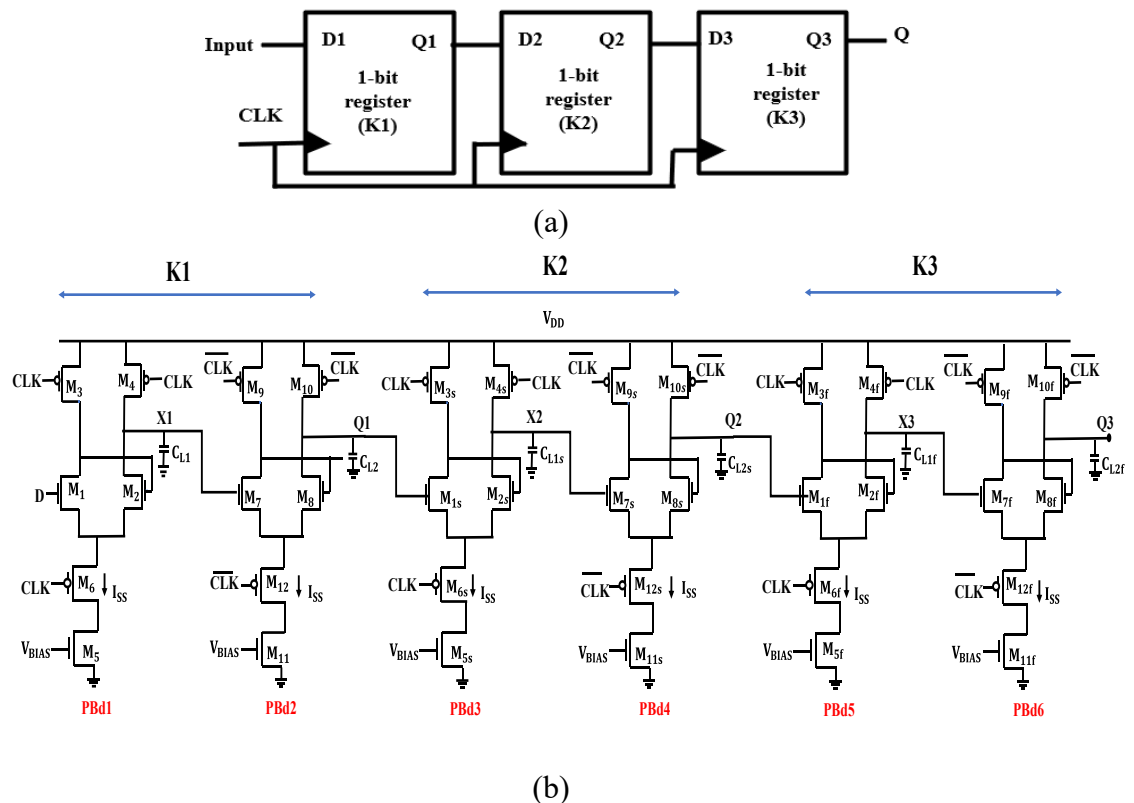


Fig. 5.10 (a) Block diagram of 3-bit SISO (b) Schematic 3-bit SISO based on DR-5 register

Table 5.6 Performance comparison of different 3-bit SISO register designs

Parmeter Register design	Propagation delay (ps)	Power consumption (μW)	PDP (fJ)	Transistor count
SR-1	2915	660	1923.90	84
SR-2	2777	660	1832.82	84
SR-3	3155	660	2082.30	96
SR-4	2824	660	1863.84	72
SR-5	2553	660	1684.98	72
SR-6	3067	660	2024.22	84
DR-1	2128	330	702.24	42
DR-2	2065	330	681.45	42
DR-3	2374	330	783.42	48
DR-4	1960	330	646.80	36
DR-5	1834	330	605.22	36
DR-6	2198	330	725.34	42

A performance comparison is performed and results are reported in Table 5.6 the following observations are made from the results.

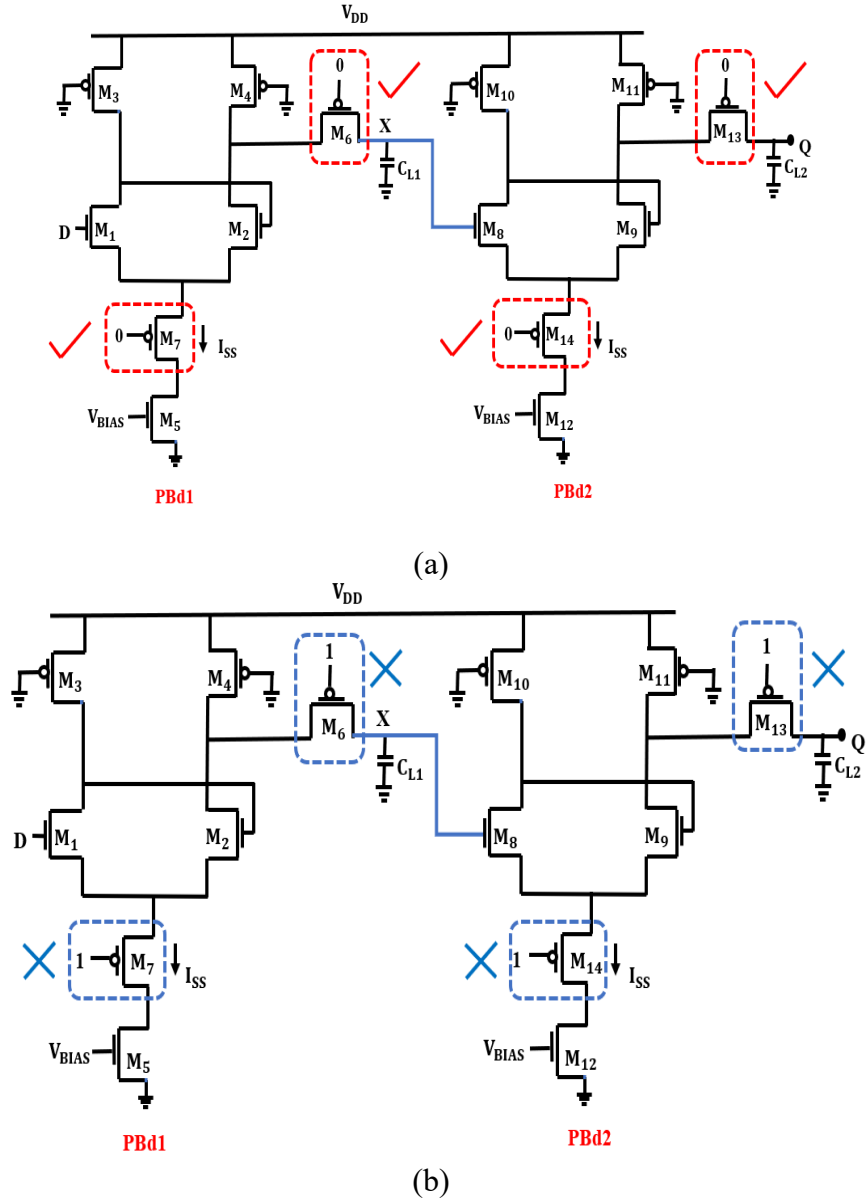
1. The proposed SR-5 register based 3-bit SISO register exhibits the best performance, achieving approximately 19.1 % reduction in propagation delay and PDP, along with 25 % lower transistor count compared to the SR-3 register design.
2. Among the dynamic registers, DR-5 based 3-bit SISO design demonstrates the best performance, with about 22.7 % reduction in propagation delay and PDP, and 25 % lower transistor count compared to the DR-3 based register design.
3. The DR-5 based 3-bit SISO register outperforms the SR-5 register with a maximum reduction of 28.1 % lower propagation delay, 64.1 % lower PDP, and 50 % reduction in both power consumption and transistor count.

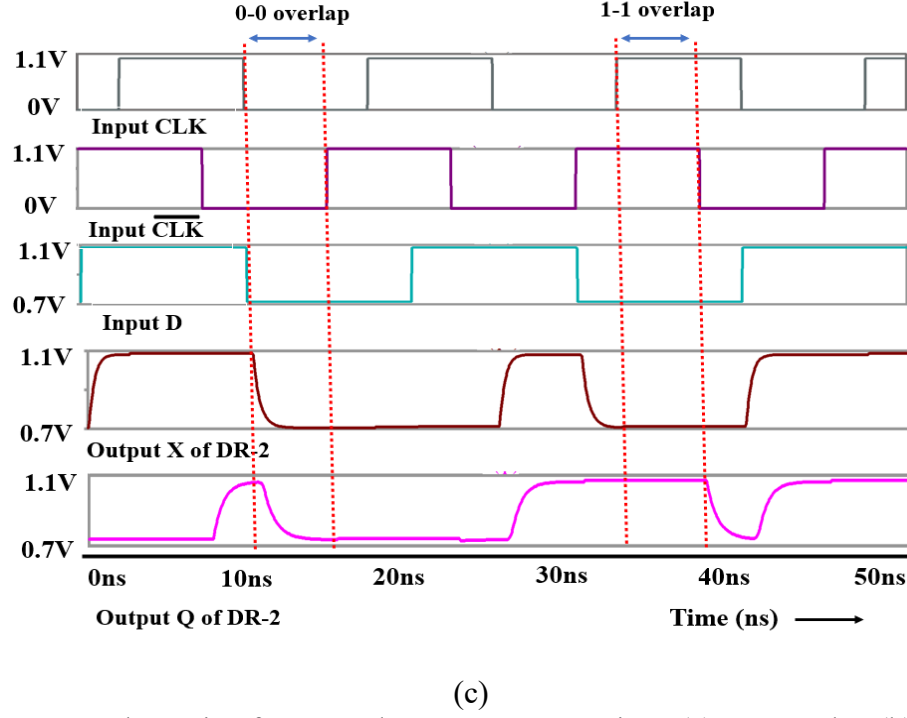
5.6 Clock overlap issue in PFSCS registers

A register design is usually based on employing perfect clock signal (CLK and $\overline{\text{CLK}}$) signals. However, in practical scenarios, achieving a perfect clock inversion signal is challenging due to different routing paths [118, 7]. This condition results in clock overlapping periods, termed as 0-0 and 1-1 overlaps, which leads to undesired behavior. In this section, the issue of clock overlap in the proposed PFSCS registers is studied, and thereafter, methods to address the clock overlap issue are suggested.

The proposed switch based PFSCS DR-2 is considered to illustrate the clock overlap issue. During the 0-0 overlap period, the CLK and $\overline{\text{CLK}}$ driven transistors M_6 , M_7 ,

M_{13} , and M_{14} , as indicated by the red tick mark in Fig. 5.11(a), conducts such that any change in input D gets reflected at the register final output node, Q. After the 0–0 overlap period when $\overline{\text{CLK}}$ becomes 1, the incorrect data appears at the output as the input data gets sampled during overlap period. Thus, the circuit malfunction as it fails to maintain the last value at its output node Q. Conversely, during the 1–1 overlap period, the transistors M_6 , M_7 , M_{13} , and M_{14} , as indicated in Fig. 5.11(b) by a blue tick mark, are turned OFF such that the output node Q maintains the last stored value. After the 1–1 overlap period when the $\overline{\text{CLK}}$ makes high to low transition, the master stage becomes transparent. The timing waveform of the proposed PFSCS DR-2 register, shown in Fig. 5.11(c), validates the theoretical propositions. Thus, it is evident that these overlap conditions must be addressed to ensure proper circuit operation.





(c)
Fig. 5.11 Schematic of proposed PFSCSCL DR-2 register (a) 0-0 overlap (b) 1-1 overlap (c) Timing waveform

The following methods are proposed for PFSCSCL registers to address the 0-0 overlap issue:

Method-1: This method suggests that the input data D should remain unchanged during the overlap period.

Method-2: In this method, the propagation delay of the master stage must be greater than the 0-0 overlap period. The 0-0 overlap period constraint is given as:

$$t_{0-0 \text{ overlap}} < t_{d_PB1} \quad (5.12)$$

Method-3: The last method suggests the use of a new additional circuit and is based on generating a local clock signal (PCLK) for the slave stage. The circuit adds two transistors PC_1 , and PC_2 for generating PCLK as shown in Fig. 5.12(a). During the 0-0 overlap period, the NMOS transistor PC_1 is OFF while PC_2 conducts that raises PCLK signal to a high voltage level. Consequently, the buffer PBd2 remains in high impedance state and maintains the last value at its output node, Q. During 1-1 overlap period, the NMOS transistor PC_1 conducts, while PC_2 is OFF, this results in low voltage for PCLK signal. This configuration allows the buffer PBd2 to maintain its original state without any changes. Fig. 5.12(b) shows the timing diagram of the proposed clock insensitive register design. It can be observed in Fig. 5.12 (b) that during the 0-0 overlap period the change in input D is not reflected at the output node Q. Hence, the operation of the proposed circuit is not affected by 0-0 and 1-1 overlap by following this method.

The proposed master-slave PFSCS register is designed such that it does not employ any dedicated non-overlapping clock generation block. In the proposed configuration, the input clock (CLK) is externally applied, while the signal (PCLK) is internally generated using the transistors PC₁ and PC₂, which are an integral part of the proposed register design. The generated PCLK provides the required phase separation between the master and slave stages, thereby preventing clock overlap without requiring any additional clock generation circuitry. From the SoC implementation perspective, no dedicated clock-skew mitigation network is added in the register design. Therefore, the proposed design does not introduce any area overhead at the system level. Similarly, since only two transistors are utilized for the internal generation of PCLK, the additional power consumption is negligible compared to the overall power budget of the SoC. Hence, the proposed architecture offers an efficient clock-overlap mitigation approach without imposing significant power or area penalties, making it well suited for SoC integration.

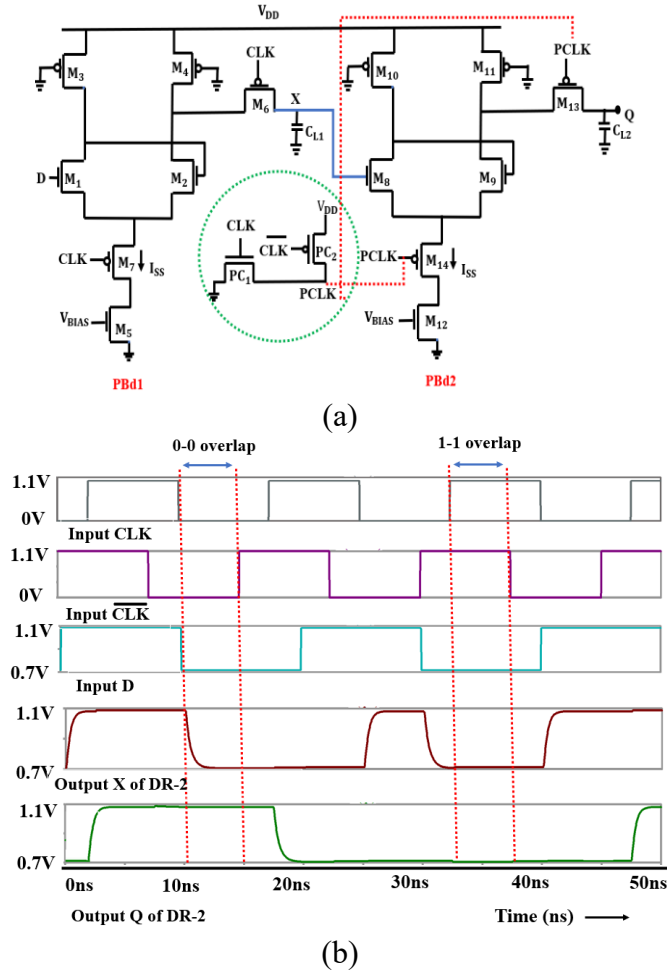


Fig. 5.12 Clock skew insensitive PFSCS dynamic register (a) Proposed method-3 using DR-2 (b) Timing waveform

5.7 Conclusion

This chapter presents the design and analysis of PFSCCL registers targeted for high-performance mixed-signal applications. The proposed design approach utilizes both switch based and sleep based PFSCCL tristate buffers. Two categories of registers static and dynamic are introduced. The static PFSCCL registers ensure continuous current flow during operation, whereas the dynamic register designs limit current flow and enable temporary charge storage. A total of six static register designs is proposed, categorized as SR-1 to SR-3 (switch based) and SR-4 to SR-6 (sleep based), and their performance is analyzed. Similarly, six dynamic register designs are developed, classified as DR-1 to DR-3 (switch based) and DR-4 to DR-6 (sleep based), and evaluated in detail. The proposed registers are validated using LTspice simulations with PTM 90 nm CMOS parameters. Simulation results indicate that among static registers, the sleep based SR-5 achieves superior overall performance, with reductions of 14 % in propagation delay, and PDP as compared other proposed register designs. In the case of dynamic registers, the sleep based DR-5 demonstrates the best performance, achieving improvements of 13.6 % in propagation delay, and PDP. A comparison between the best dynamic and static designs (DR-5 and SR-5) reveals that DR-5 achieves a reduction of 17.9 % in propagation delay, 59 % in PDP, 50 % in both power consumption and transistor count. Additionally, the issue of clock overlap arising from unequal clock routing paths is addressed, and techniques to achieve clock-skew insensitive operation in PFSCCL registers are proposed. The robustness of all register designs is verified through Monte Carlo simulations and corner analysis, confirming reliable operation under process variations. The feasibility of the proposed designs is validated through a 3-bit SISO register implementation.

CHAPTER 6

CNTFET BASED PFSCS GATES

6.1 Introduction

The conventional design of PFSCS circuits relies on planar silicon-based MOSFET technology. The continuous scaling of MOSFET dimensions has been pursued in line with Moore's Law to achieve higher integration density and enhanced circuit performance. However, as device dimensions approach the nanometer regime, several critical challenges arise. These include pronounced short-channel effects, increased leakage currents, and mobility degradation. Such non-ideal effects significantly deteriorate the overall performance and reliability of circuits, thereby posing limitations on further scaling of traditional MOSFET-based PFSCS designs. Therefore, there is a need to explore alternative device technologies suited for PFSCS style. CNTFETs have recently emerged as a promising substitute for MOSFETs due to superior carrier mobility, near-ballistic transport, and superior current driving capability [85-88]. CNTFETs have been employed in various application design in nanometer regime such as arithmetic circuits, full adder-subtractor architectures [120-121], and hybrid design [122-123]. Therefore, this chapter investigates the use of CNTFET technology in PFSCS style and put forwards a performance comparison between PFSCS circuits designed using MOSFET and CNTFET technologies.

6.2 CNTFET preliminaries

A CNTFET is a transistor that uses a carbon nanotube as its channel instead of silicon, enabling current flow between source and drain. Figures 6.1(a) and 6.1(b) show the cross sectional and top views of the CNTFET structure. The CNTFET consists of horizontally aligned cylindrical carbon nanotubes (CNTs) formed by rolling a thin sheet of graphene into a tube, with very small diameters [124]. In a typical CNTFET, the CNTs are placed on a substrate material, where the channel region is kept intrinsic, while doping is applied to the source and drain regions to allow efficient carrier injection. A high-k dielectric material is used to provide electrical insulation between the gate and the channel, which improves gate control and reduces leakage current. The intrinsic channel helps reduce scattering effects and enables near-ballistic transport, thereby enhancing the electrical performance of the CNTFET.

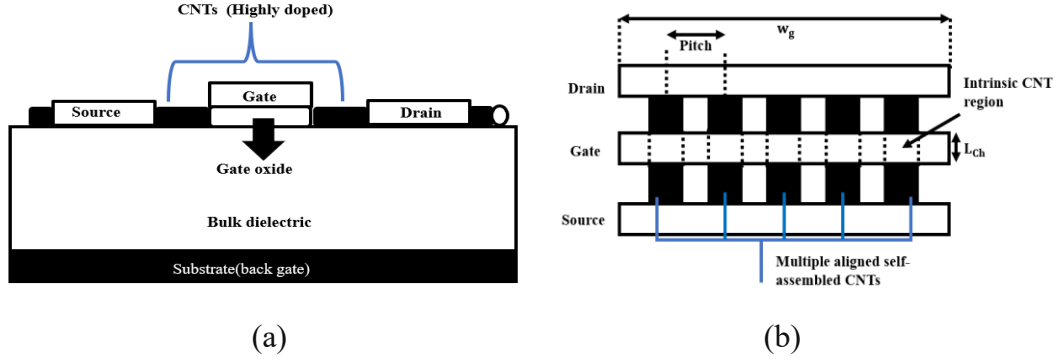


Fig. 6.1 CNTFET structure (a) Cross sectional view (b) Top view [88,124]

When multiple CNTs are used in parallel to form the channel, the overall gate width of the CNTFET depends on the number of nanotubes and their spacing. Therefore, the effective width (W_g) of a multi-tube CNTFET is defined to account for the combined contribution of all the nanotubes forming the channel. The W_g is determined using the expression given in [124] as:

$$W_g = \text{Pitch} \cdot (N_{\text{CNT}}) + D_{\text{CNT}} \quad (6.1)$$

Here, pitch denotes the center-to-center spacing between adjacent carbon nanotubes, N_{CNT} represents the number of tubes, and D_{CNT} indicates the tube diameter. Furthermore, D_{CNT} is calculated as:

$$D_{\text{CNT}} = Ch/\pi \quad (6.2)$$

where, chirality a key device level parameter in CNTFET design. The chirality determines the direction in which a graphene sheet is rolled to form a cylindrical carbon nanotube. The chirality of a carbon nanotube is given as:

$$Ch = a\sqrt{n_1^2 + n_2^2 + n_1n_2} \quad (6.3)$$

where $a = 0.249$ nm is lattice constant, n_1 and n_2 are integers. Depending on the values of (n_1, n_2) , a CNT can exhibit either metallic or semiconducting behavior. A CNT behaves as a metal when $n_1 = n_2$ or when $n_1 - n_2 = 3i$, where i is an integer and for all other values, it behaves as a semiconductor.

The CNT diameter directly influences the threshold voltage of a CNTFET [124].

$$V_{th} = 0.42/D_{\text{CNT}} \quad (6.4)$$

6.3 Proposed CNTFET based static PFSCl gates

This section presents the design of CNTFET based static PFSCl gates. These designs integrate CNTFET technology into the PFSCl style and study its effect on circuit performance.

6.3.1 Proposed design scheme-5

The proposed design scheme-5 is based on employing CNTFETs in PFSCl style. A Proposed design scheme-5 N-input CNTFET PFSCl gate is shown in Fig. 6.2. The proposed CNTFET PFSCl gate consists of three main components: a pull-down network (PDN), a current source, and load transistors. The PDN consist of N-input CNTFETs (CM_1 - CM_N) that are source coupled with a feedback CNTFET CM_F to realize the given functionality in a NOR/OR form. The current source CM_B maintains a constant bias current while the load transistors CP_1 and CP_2 perform the current-to-voltage conversion.

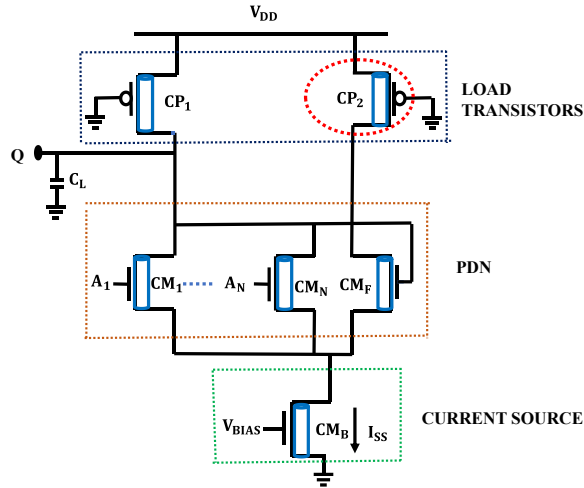


Fig. 6.2 Proposed design scheme-5 N-input CNTFET PFSCl gate

A CNTFET PFSCl gate works on the principle of current steering. A proposed CNTFET PFSCl inverter is drawn in Fig. 6.3 to illustrate the operation. The PDN comprises of source coupled transistor pair (CM_1 - CM_F), the current source uses an N-CNTFET transistor CM_B operating in saturation region whereas the P-CNTFET (CP_1) act as load for the inverter circuit. For a low voltage level at input A, I_{SS} gets steered to CM_F such that there exists no voltage drop across load transistor CP_1 and therefore a high voltage is obtained at the output node, Q ($V_{OH} = V_{DD}$). Alternatively, for high voltage level at input A, I_{SS} is steered through CM_1 and a low output voltage is obtained at the output node Q ($V_{OL} = V_{DD} - V_{SWING}$) where V_{SWING} corresponds to the voltage drop across load CP_1 .

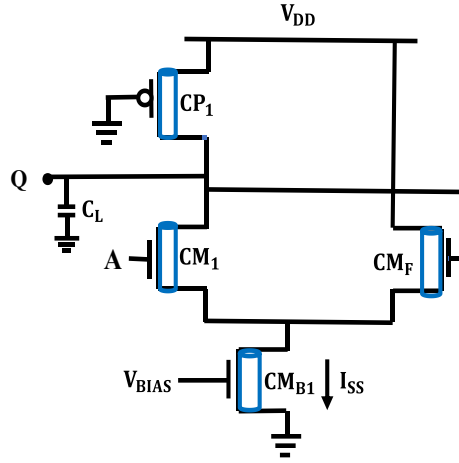


Fig. 6.3 Proposed design scheme-5 CNTFET PFSCl inverter

Realization of CNTFET PFSCl logic gates

The general N-input PFSCl gate shown in Fig. 6.2 implements an N-input NOR operation by arranging N CNTFETs in parallel, followed by an inversion stage at the input. Based on this, two input CNTFET PFSCl (NOR2) gate is realized by connecting two CNTFETs (CM_1 , CM_2) in parallel as shown in Fig. 6.4(a). When any one of the inputs is high, the corresponding CNTFET turns ON and a low voltage level is obtained at the output node. Alternatively, when all the inputs are low, the bias current flows through CNTFET CM_F such that no potential drop across the load transistor CP_1 and a high voltage V_{OH} is obtained. The node voltages corresponding to various input combinations of the proposed design-5 CNTFET PFSCl NOR2 gate is listed in Table 6.1.

The same circuit can be reconfigured to perform OR functionality by taking the output from the complementary load transistor, denoted as CP_2 as shown in Fig. 6.4(b). The same topology can be used for two-input CNTFET PFSCl NAND2 gate with help of De Morgan law as shown in Fig. 6.4(c). The functionality of a NAND2 gate is expressed as:

$$Q = \overline{A \cdot B} = \overline{A} + \overline{B} \quad (6.5)$$

The inputs are applied in the inverted form, and the output is taken from the other branch. Based on the same design principle, a CNTFET PFSCl XOR gate is shown in Fig. 6.4 (d). The XOR logic is represented as:

$$Q = A \oplus B = \overline{A} B + \overline{B} A \quad (6.6)$$

It consists of three identical 2-input CNTFET PFSCl NOR gates that are arranged in two levels. The first level is responsible for generating the minterms whereas the subsequent level implements the sum of minterms. The summary of node voltages for different logic functions such as OR2, NAND2, XOR2 gate are appended in Table 6.1.

Similarly, the realization of a CNTFET PFSCSCL 2:1 MUX with select line S_0 and data inputs I_0, I_1 is shown in Fig. 6.4(e). The summary of voltages at output node is summarized in Table 6.2.

Table 6.1 Summary of voltages in proposed design scheme-5 for different gates

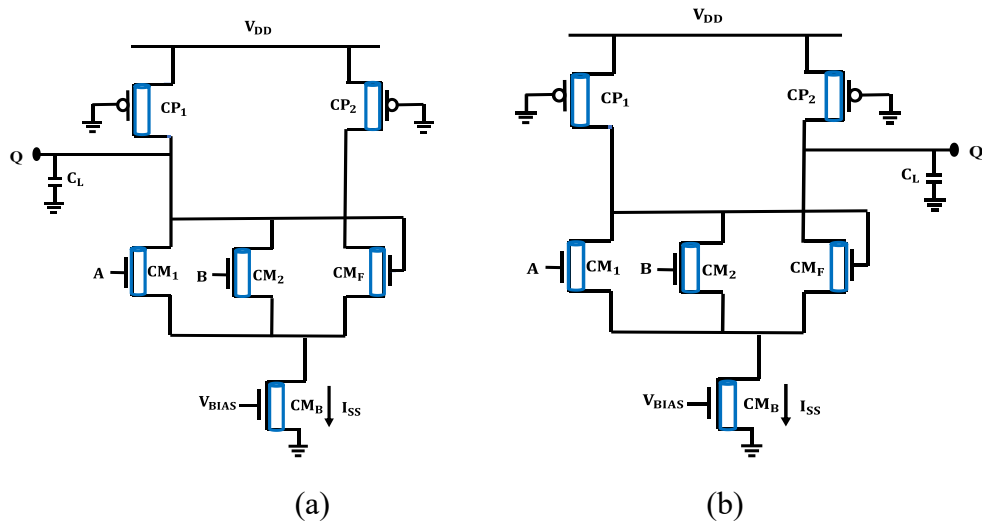
Inputs			Output Q		
A	B	NOR2	OR2	NAND2	XOR2
V_{OL}	V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OL}
V_{OL}	V_{OH}	V_{OL}	V_{OH}	V_{OH}	V_{OH}
V_{OH}	V_{OL}	V_{OL}	V_{OH}	V_{OH}	V_{OH}
V_{OH}	V_{OH}	V_{OL}	V_{OH}	V_{OL}	V_{OL}

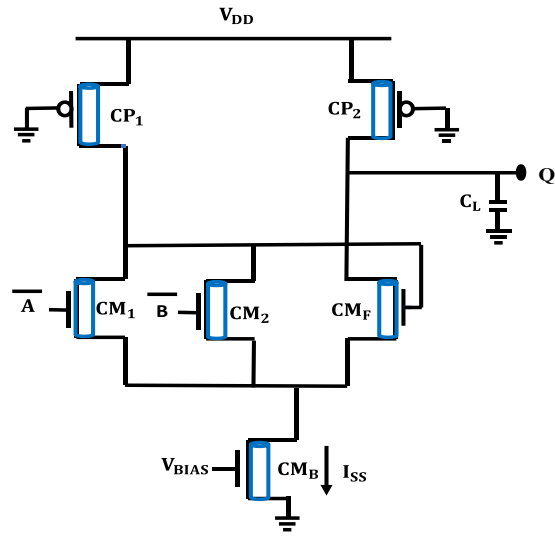
where $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - V_{SWING}$

Table 6.2 Summary of voltages in proposed design scheme-5 CNTFET PFSCSCL 2:1 MUX

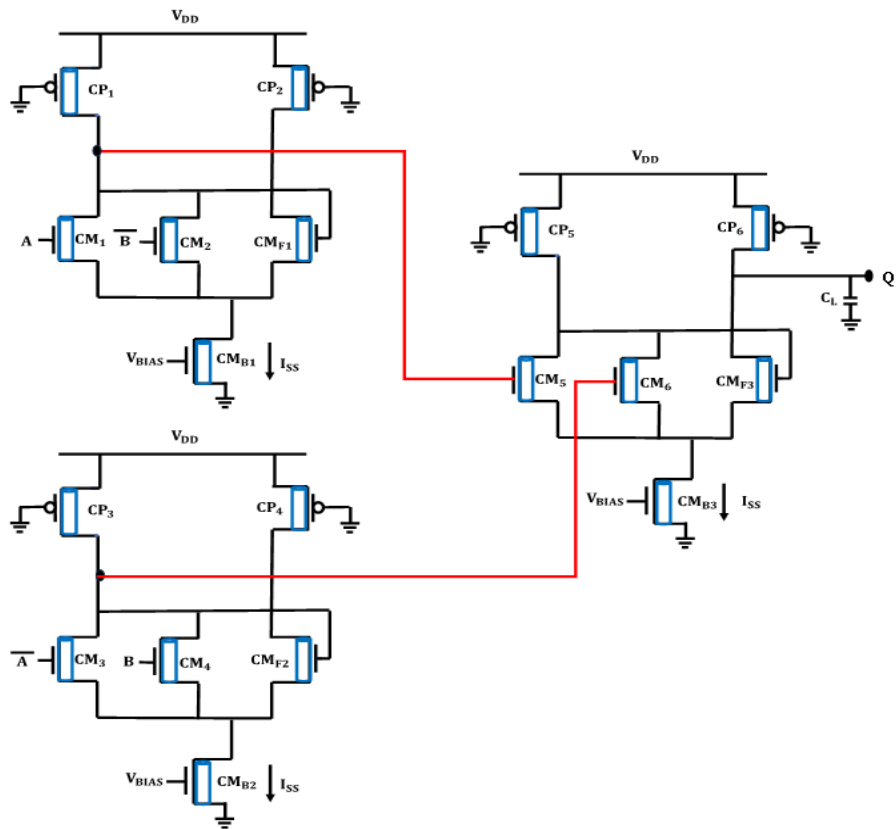
Inputs			Output
S_0	I_0	I_1	Q
V_{OL}	V_{OL}	V_{OL}	V_{OL}
V_{OL}	V_{OL}	V_{OH}	V_{OL}
V_{OL}	V_{OH}	V_{OL}	V_{OH}
V_{OL}	V_{OH}	V_{OH}	V_{OH}
V_{OH}	V_{OL}	V_{OL}	V_{OL}
V_{OH}	V_{OL}	V_{OH}	V_{OH}
V_{OH}	V_{OH}	V_{OL}	V_{OL}
V_{OH}	V_{OH}	V_{OH}	V_{OH}

where $V_{OH} = V_{DD}$ and $V_{OL} = V_{DD} - V_{SWING}$





(c)



(d)

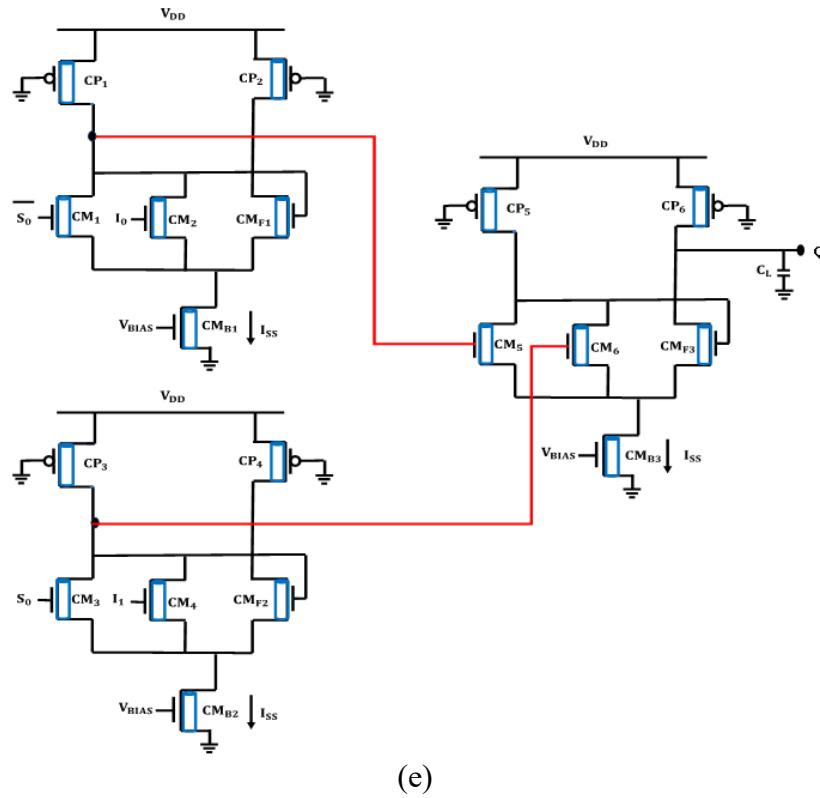


Fig. 6.4 Proposed design scheme-5 based two-input CNTFET PFSCl functions (a) NOR2 (b) OR2 (c) NAND2 (f) XOR2 (e) 2:1 MUX

6.4 Impact of CNTFET parameters on CNTFET PFSCl inverter

In this section, the impact of CNTFET device parameters such as CNT count, chirality, diameter, selection of pitch, dielectric material and oxide thickness on propagation delay. A CNTFET PFSCl inverter is simulated and analyzed by varying the device parameter and the optimized values are determined. Based on these optimized values, different CNTFET PFSCl gates are designed and simulated for performance comparison with MOSFET PFSCl gates.

(a) CNT count

The CNT count of a CNTFET determines the current driving capability which affects the propagation delay of CNTFET circuits. A graph showing the propagation delay of CNTFET PFSCl inverter relative to CNT count is drawn in Fig. 6.5 (a). It is evident that the propagation delay decreases rapidly when the number of CNTs increases from 2 to 8 due to higher current that results in faster switching. However, the reduction in propagation delay is not significant for further increase in CNT count while circuit complexity and area become more significant. Thus, the CNT count is selected as 8 to maintain low propagation delay with reasonable design complexity.

(b) Chirality

Chirality is a key parameter influencing the performance of CNTFETs, as it directly determines the threshold voltage. With an increase in chirality, the threshold voltage decreases. This reduction enhances carrier transport, resulting in higher drive current. Consequently, the channel resistance is reduced, which leads to lower propagation delay and improved switching speed. The variation of propagation delay with chirality for the CNTFET PFSCl inverter, as illustrated in Fig. 6.5(b), shows a consistent decrease in delay with increasing chirality. However, beyond chirality (19,0), the reduction in propagation delay becomes less significant. Moreover, higher chirality values are associated with a decline in the I_{on}/I_{off} ratio and increased leakage current due to reduced bandgap [124], which can adversely affect switching reliability. Therefore, chirality (19,0) is selected as the optimal value, as it offers a balanced trade-off between reduced delay, acceptable I_{on}/I_{off} ratio, and stable device operation.

(c) Selection of pitch

The pitch between the carbon nanotubes in a CNTFET influences both drive current and parasitic effects. The trend observed in the propagation delay of a CNTFET PFSCl inverter for various pitch values is shown in Fig. 6.5(c). It is observed that increasing pitch leads to reduced propagation delay. This is due to the fact that a larger pitch reduces the screening effect between adjacent CNTs, which improves the effective gate control and increases the drive current of the device that leads to a reduction in propagation delay. The propagation delay decreases rapidly at lower pitch values and then gradually saturates at higher pitch values. Beyond a pitch of 18 nm, there exists small reduction in propagation delay. Therefore, a pitch of 18 nm is selected as the optimum value, as it provides significant improvement in propagation delay while avoiding unnecessary increase in device area.

(d) Selection of dielectric material

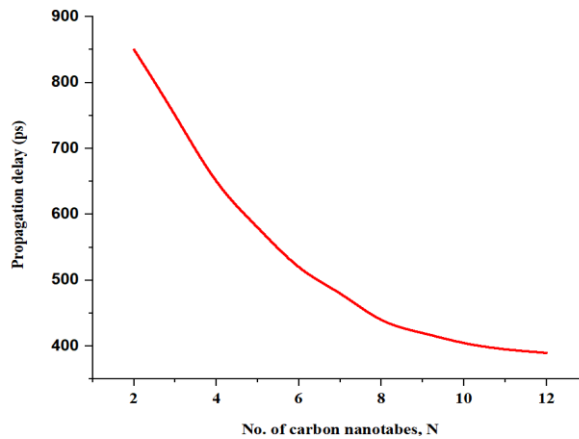
The dielectric material of a CNTFET controls the gate capacitance and electrostatic behavior of the device. High-k dielectric materials improve the gate control over the channel, which enhances the drive current. Since the propagation delay is inversely related to the drive current, an increase in dielectric constant leads to a reduction in propagation delay [124]. In this work, a dielectric constant of $K_{ox} = 25$ is considered, which corresponds to ZrO_2 . This material provides strong gate control and improved current driving capability, resulting in better switching performance. Although higher dielectric constant materials can be used, the improvement becomes marginal due to parasitic effects. Therefore, ZrO_2 ($K_{ox} = 25$) is selected as the dielectric material for the proposed CNTFET PFSCl gates.

After selecting the dielectric material (ZrO_2 with $K_{ox} = 25$), the oxide thickness is optimized to achieve improved device performance. The oxide thickness directly

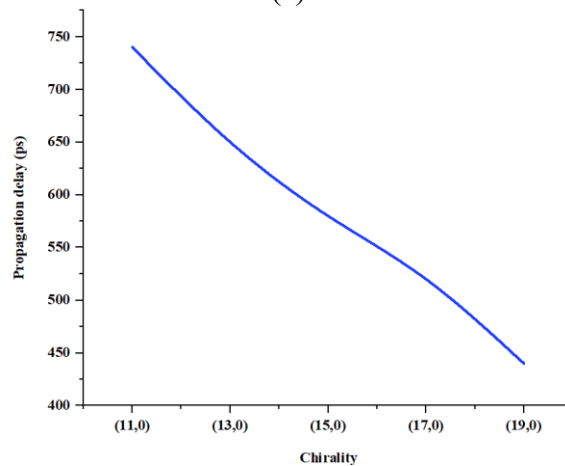
affects the gate-to-channel coupling and hence the drive current of the device. Since the propagation delay is inversely related to the drive current, any improvement in current results in faster switching and reduced propagation delay.

The graph between the propagation delay of CNTFET PFSCl inverter and oxide thickness reveals that the propagation delay initially decreases with an increase in oxide thickness and reaches a minimum at around 4 nm as shown in Fig. 6.5(d). This behaviour indicates an optimal balance between gate control and parasitic effects. However, beyond 4 nm, the delay starts to increase due to a reduction in gate capacitance, which results in weaker channel control and lower drive current, an oxide thickness of 4 nm is selected as the optimum value, as it provides minimum propagation delay while maintaining stable and efficient device operation.

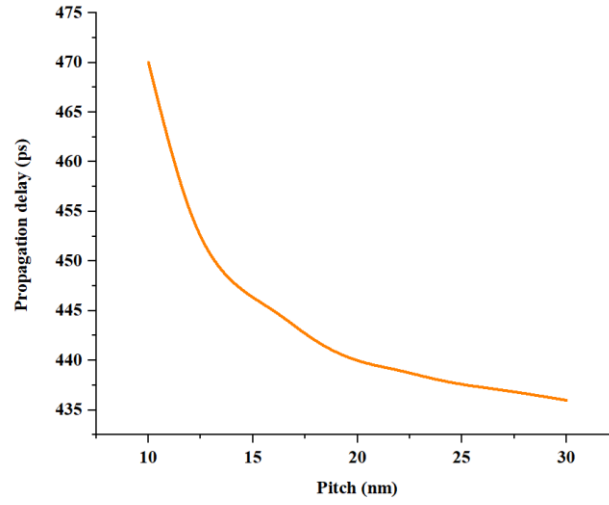
The optimized values of CNT count, chirality, pitch, dielectric material and oxide thickness on propagation are taken as 8, (19,0), 18 nm, ZrO_2 and 4 nm for further exploration.



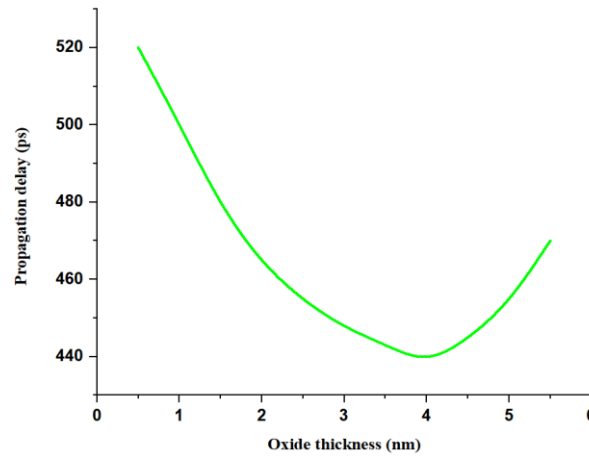
(a)



(b)



(c)



(d)

Fig. 6.5 Impact of CNTFET parameters on proposed design scheme-5 CNTFET PFSCl inverter (a) CNT count (b) Chirality (c) No. of pitch (d) Oxide thickness

6.5 Simulation section

The functionality of the proposed CNTFET PFSCl gates, namely inverter, two-input NAND2 gate, OR2 gate, XOR2, and 2:1 MUX, is verified, and their performance is compared with conventional MOSFET PFSCl counterpart. In addition, XOR3 gate is also implemented as a design example. All simulations are carried out in SPICE using the 32 nm Stanford CNTFET model [88] and 32 nm CMOS technology parameters. All simulations are performed with V_{DD} , I_{SS} , V_{SWING} and C_L of 1.1 V, 100 μA , 400 mV, and 50 fF respectively.

The simulation waveforms of the proposed CNTFET PFSCl inverter, NAND2, OR2, XOR2 gates, and 2:1 MUX are shown in Fig. 6.6. The inverter waveform in Fig. 6.6(a) confirms the availability of complementary logic level at the output node based on the applied input.

The waveform for the proposed CNTFET PFSCl OR2 gate, the output is observed to be at a high voltage level ($V_{OH} = 1.1$ V) whenever at least one of the inputs is high. The output switches to a low voltage level ($V_{OL} = 0.7$ V) only when both inputs are low, confirming the OR operation. Similarly, the waveform for the proposed CNTFET PFSCl NAND2 gate indicates that when both inputs A and B are at a high logic level, the output switches to a low voltage level ($V_{OL} = 0.7$ V). Alternatively, for all other input conditions, the output remains at a high voltage level ($V_{OH} = 1.1$ V), thereby validating the NAND operation.

The operation of the proposed CNTFET PFSCl XOR2 gate shown in Fig. 6.6(a) depends on whether the inputs are the same or different. When both inputs are at the same logic level, the output remains low ($V_{OL} = 0.7$ V), whereas for different input combinations, the output switches to a high voltage level ($V_{OH} = 1.1$ V), validating the XOR functionality.

For the 2:1 MUX, the output is controlled by the select line (S_0). When the S_0 is low, the output follows input A, whereas when the S_0 is high, the output follows input B. The timing waveforms in Fig. 6.6(b) clearly demonstrate correct 2:1 MUX behaviour.

Table 6.3 Performance comparison of different MOSFET and CNTFET logic functions

Parameter Function	MOSFET PFSCl logic functions		
	Propagation delay	Power consumption (μW)	PDP (fJ)
Inverter	743	110	81.73
OR2	1009	110	110.99
NAND2	837	110	92.07
XOR2	1700	330	561
2:1 MUX	1700	330	561
Proposed design scheme -5 CNTFET PFSCl functions			
Inverter	440	110	48.40
OR2	620	110	68.20
NAND2	491	110	54.01
XOR2	1128	330	372.24
2:1 MUX	1128	330	372.24

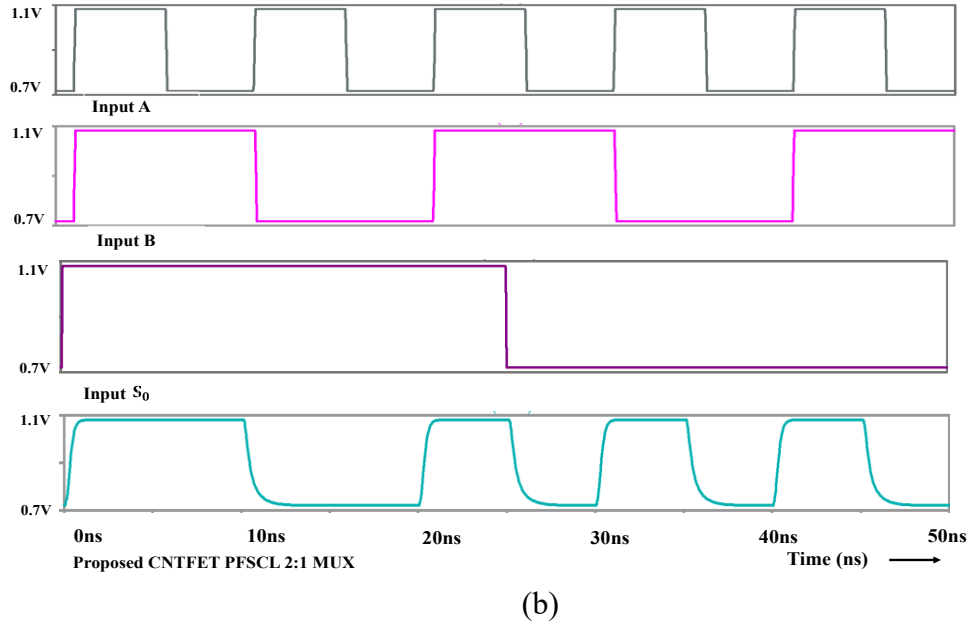
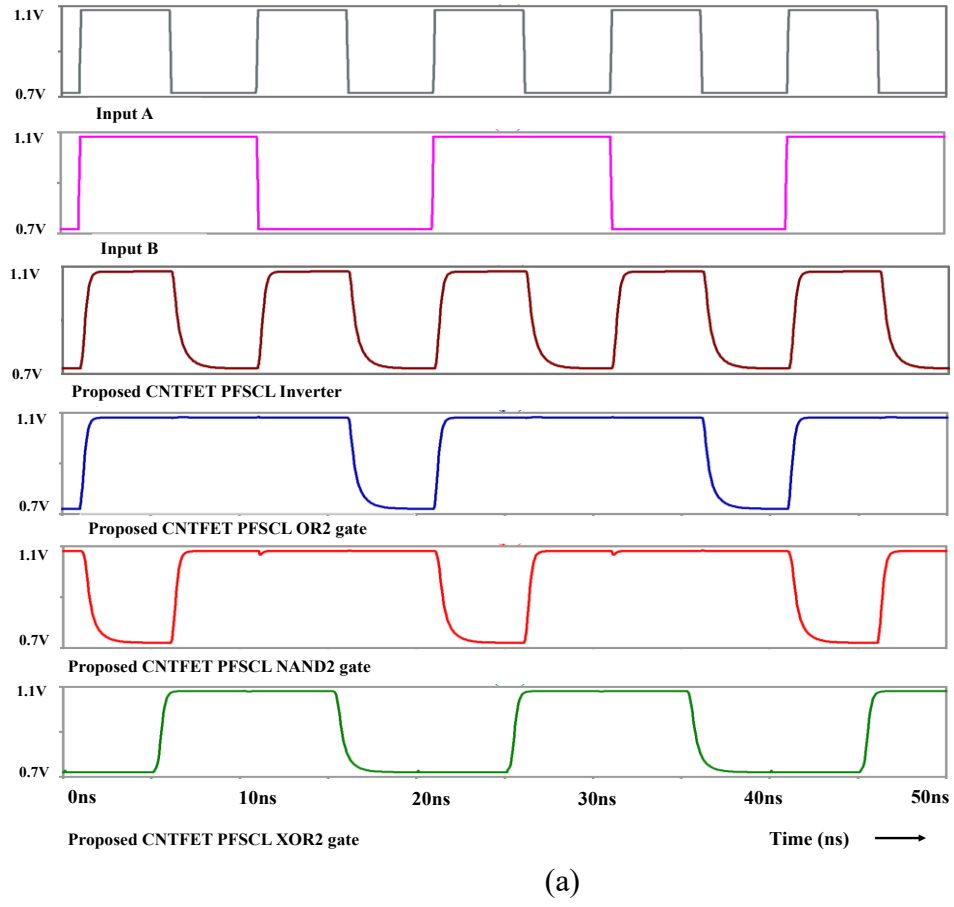


Fig. 6.6 Timing waveforms of different logic functions in proposed design scheme-5 CNTFET PFSCl style (a) Logic gates (b) 2:1 MUX

The performance of the proposed gates is compared with MOSFET PFSCl gates in terms of propagation delay, power consumption and PDP. The results are summarized in Table 6.3 and the following observations are made:

1. A significant improvement in propagation delay is observed for all proposed CNTFET PFSCl gates compared to conventional MOSFET PFSCl gates. Specifically, the proposed CNTFET inverter, OR2, and NAND2 gates achieve reductions in propagation delay of approximately 40.7 %, 38.6 %, and 41.4 %, respectively, relative to their MOSFET PFSCl counterparts. Notably, the XOR2 gate and 2:1 MUX shows a maximum reduction of 33.6 %, demonstrating the effectiveness of the CNTFET PFSCl design in improving switching speed.
2. The power consumption remains constant for both conventional MOSFET PFSCl gates and proposed CNTFET PFSCl gates as both designs utilize a constant current source.
3. A significant improvement in PDP is observed across all proposed CNTFET PFSCl gates as compared to conventional MOSFET PFSCl gates. The PDP reduction corresponds directly with the decrease in propagation delay while maintaining the same power consumption. For example, the XOR2 gate and 2:1 MUX achieves a maximum PDP reduction of 33.6 %, demonstrating improved energy efficiency.

Further process corner analysis is carried out for conventional MOSFET PFSCl and proposed CNTFET PFSCl inverter. The graph illustrated in Fig. 6.7 compares the propagation delay of MOSFET PFSCl and proposed CNTFET PFSCl inverters across five standard process corners: TT, FF, SS, FS, and SF. The proposed CNTFET PFSCl inverter consistently outperforms the conventional MOSFET PFSCl, achieving significantly lower propagation delays at all corners. For example, at the TT corner, the CNTFET PFSCl inverter has a delay of 440ps, compared to 743ps in the conventional MOSFET PFSCl. The best performance is observed at the FF while the worst case appears at the SS corner. Overall, the CNTFET PFSCl inverter not only improves speed but also maintains good stability under process variations, making it a superior choice for high-performance digital applications.

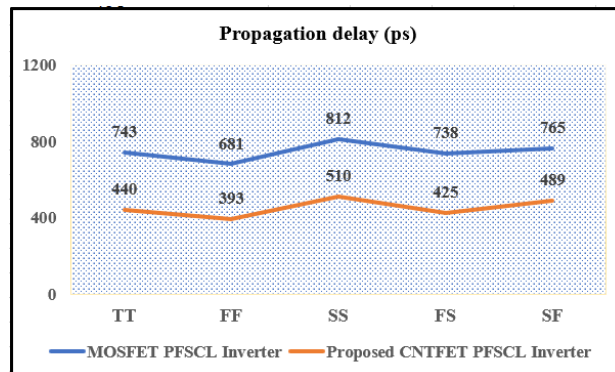


Fig. 6.7 Proposed design scheme-5 CNTFET PFSCl inverter across different corners

6.6 Design example

To demonstrate the efficiency of the proposed design scheme-5, a three input XOR3 gate is implemented. The operation of XOR3 for inputs A, B, and C can be written using NOR/OR representation as:

$$F = \overline{(A + B + C)} + \overline{(A + \bar{B} + \bar{C})} + \overline{(\bar{A} + B + \bar{C})} + \overline{(\bar{A} + \bar{B} + C)} \quad (6.7)$$

The above expression reveals that requirement of a 4-input PFSCS NOR/OR gate driven by the outputs the four 3-input PFSCS NOR/OR gates. The complete circuit is shown in Fig. 6.8 wherein the maxterms are realized by the 4 NOR/OR CNTFET PFSCS gates (NOR-1, NOR-2, NOR-3, NOR-4) and their corresponding outputs ($Y_1 - Y_4$) are further fed to the 4-input NOR/OR CNTFET PFSCS gate (NOR-5) to realize XOR3 gate functionality.

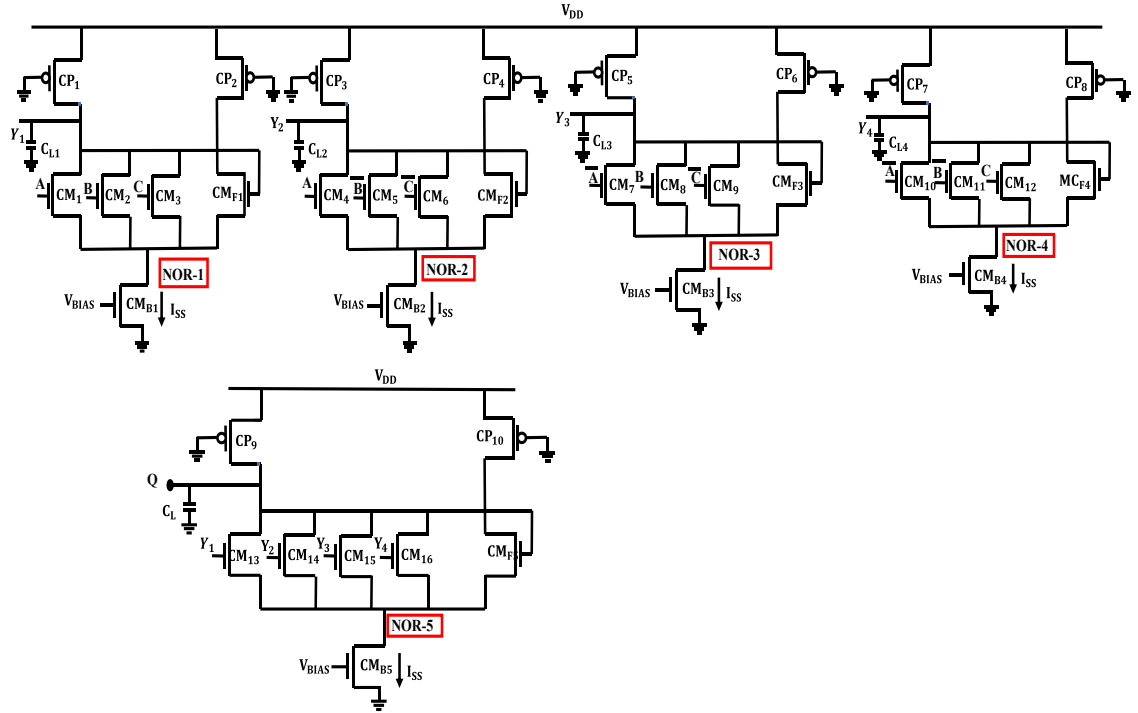


Fig. 6.8 Proposed design scheme-5 CNTFET PFSCS XOR3 gate

The functionality of the proposed design scheme-5 CNTFET PFSCS XOR3 gate is examined. The corresponding timing waveform is shown in Fig. 6.9. It is observed that when the number of inputs having the same logic level is even (either all low or two high), a low output voltage level is obtained. However, when an odd number of inputs have a high logic level, a high voltage is obtained at the output node, Q.

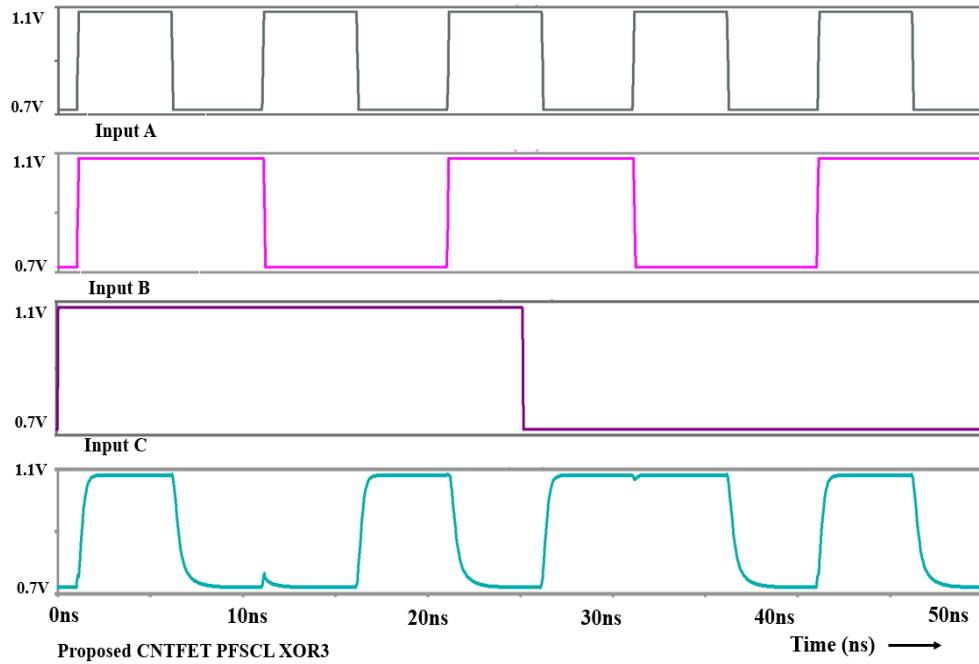


Fig. 6.9 Timing waveform of proposed design scheme-5 CNTFET PFSCl XOR3 gate

Table 6.4 Performance comparison of MOSFT and CNTFET XOR3 gate

Scheme	MOSFET PFSCl XOR3 gate	Proposed design scheme-5 CNTFET PFSCl XOR3 gate
Parameter		
Power consumption (μ W)	550	550
Propagation delay (ps)	2457	1656
PDP (fJ)	1351	911

The performance is further compared with MOSFET PFSCl XOR3 gate by using the same simulation conditions to ensure a fair comparison. The results are listed in Table 6.4. The proposed design scheme-5 CNTFET PFSCl XOR3 gate shows a maximum reduction of 32.6 % in both propagation delay and PDP as compared MOSFET PFSCl gate, while maintaining the same power consumption.

6.7 Conclusion

In this chapter, CNTFETs are introduced in the PFSCl style to enhance the performance at lower technology nodes. A novel CNTFET based PFSCl design scheme, referred to as proposed design scheme-5 is used for the realization different logic functions. An optimized design of CNTFET PFSCl inverter is determined

through the variations in CNTFET parameters that include variations in CNT count, chirality, pitch, and oxide thickness. The performance comparison of the proposed CNTFET PFSCl gates is compared through simulation using the 32 nm Stanford CNTFET model and PTM 32 nm CMOS model. The performance comparison indicates the proposed CNTFET PFSCl design scheme-5 CNTFET PFSCl gates significantly reduces both propagation delay and PDP values. A maximum improvement of 33.6 % in propagation delay and PDP while maintaining the same power consumption as the MOSFET PFSCl design. The robustness of the proposed and conventional PFSCl gates is further confirmed through corner analysis, which verifies correct functionality across all process corner. A three-input XOR3 gate is implemented to show the effectiveness of proposed design scheme-5. The overall results indicate that CNTFET PFSCl gates offer a highly promising and energy-efficient solution for high-speed mixed-signal applications at lower technology.

CHAPTER 7

CONCLUSION

This chapter gives a final overview of the work completed in this thesis and outlines possible future work that can be developed based on the basic ideas presented here.

7.1 Concluding remarks

This thesis presents novel designs of PFSCl gates for the implementation of complex logic functions with reduced propagation delay, power consumption, and area. Chapter 2 describes the fundamental concepts of PFSCl gates. It elaborates on the operation, analysis, and implementation of various logic functions using both static and dynamic PFSCl gates. A discussion on the PFSCl multitail cell used in these gates is also provided. Furthermore, improved design structures for both static and dynamic PFSCl gates are presented. Finally, the design of PFSCl tristate buffer/inverter is introduced, laying the groundwork for designing registers using the PFSCl approach.

In the chapter 3, memristors are employed in the realization the logic functions in static PFSCl gates. The use of memristor in function realization overcome the restriction of limited fan-in, high gate count and significant area requirement of the existing static PFSCl styles. Two new memristor based design schemes for static PFSCl gates are presented. The proposed design scheme-1 adds a memristor based network (MBN) with a PFSCl inverter, while the proposed design scheme-2 integrates the memristors with PFSCl NOR/OR gates. The behavior of the proposed gates based on both the design schemes is analysed in terms of V_{SWING} , A_V and NM . The simulation results of the proposed gates confirm the significant advantage in power consumption and propagation delay values. A maximum improvement of 28 % in propagation delay, 66.66 % in power consumption, 75.75 % in PDP values is obtained in proposed design scheme-2 PFSCl XOR2 gate over existing counterparts. In addition, a maximum area reduction of 94.85 % and 92.76 % is achieved using proposed design scheme-1 and scheme-2, respectively, compared to the conventional PFSCl FC XOR2 gate.

Chapter 4 focuses on the design of dynamic PFSCl gates with a reduced footprint. Memristors are incorporated in these designs due to their inherent advantage of low area requirements. They are utilized to realize the desired functionality, followed by implementation using PFSCl gates. Based on this approach, two memristor-based design schemes are proposed. The proposed design scheme -3, MBN is combined with a D-PFSCl inverter while in the proposed design scheme -4, D-PFSCl NOR/OR gates are employed to further reduce the number of memristors. The structure and operation of a D-PFSCl 2:1 multiplexer (MUX) using both proposed schemes are discussed in detail, along with an analysis of voltage swing and propagation delay. The theoretical propositions are validated through simulations of both D-PFSCl 2:1 MUX designs, and their performance is compared with existing designs. The results

indicate that design scheme-3 achieves a significant area reduction of 90 % compared to existing counterparts. Meanwhile, design scheme-4 demonstrates superior performance, achieving improvements of 55.4 %, 74.7 %, and 88.75 % in propagation delay, power consumption, and power-delay product (PDP), respectively. Further simulations are carried out for a D-PFSCL 4:1 MUX, which also shows substantial improvements, with maximum reductions of 56 % in propagation delay, 85 % in power consumption, and 94.4 % in PDP compared to existing D-PFSCL MUX designs.

Chapter-5 presents the design of PFSCL registers by using PFSCL tri-state buffers in master-slave configuration. The switch based and sleep based PFSCL tristate buffers are employed in register design. Register design in two categories namely static registers and dynamic registers are worked upon. The static PFSCL registers maintains continuous current flow during operation, whereas the dynamic PFSCL registers restricts the current flow and is based on temporary storage of charge. A total of six static PFSCL register designs, three in each category, SR-1 to SR-3 (switch based) and SR-4 to SR-6 (sleep-based) are proposed and analyzed. Similarly, six dynamic register designs, classified as DR-1 to DR-3 (switch based) and DR-4 to DR-6 (sleep-based), are developed and evaluated in detail. The registers designs are functionally verified through simulations and their performance is evaluated. The results demonstrate that the sleep based SR-5 register design achieves superior overall performance, with reductions of 14 % in propagation delay, and PDP as compared other proposed static PFSCL register designs. In the case of dynamic PFSCL registers, the sleep based DR-5 demonstrates the best performance, achieving improvements of 13.6 % in propagation delay, and PDP. A comparison between the best dynamic and static designs (DR-5 and SR-5) reveals that DR-5 achieves a 17.9 % reduction in propagation delay, 59 % reduction in PDP, 50 % power consumption, and a 50 % reduction in transistor count. Additionally, the issue of clock overlap arising from unequal clock routing paths is addressed, and techniques to achieve clock-skew-insensitive operation in PFSCL registers are proposed. Finally, the implementation of a serial-in serial-out shift register validates the feasibility of the proposed designs at the system level.

In chapter 6, CNTFETs replaces the planar MOSFETs used in PFSCL style to leverage their inherent advantages for efficient circuit design at lower technology node. A new design scheme-5 that employs CNTFET PFSCL gate design is proposed. The design of a CNTFET PFSCL inverter is optimized by varying CNTFET device parameters such as CNT count, chirality, pitch, and oxide thickness. The performance of the proposed CNTFET PFSCL gates is compared with MOSFET based PFSCL counterparts. The performance comparison indicates the proposed CNTFET PFSCL design scheme-5 gates significantly reduces both propagation delay and PDP values. A maximum improvement of 33.6 % in propagation delay and PDP while maintaining the same power consumption as the MOSFET PFSCL design. The proposed design scheme-5 is demonstrated through the implementation of a three-input XOR gate. Overall, the results indicate that CNTFET PFSCL gates offer a highly promising and

energy-efficient solution for high-speed mixed-signal applications at lower technology.

The robustness of the proposed and MOSFET PFSCl gates is further confirmed through corner analysis, which verifies correct functionality across all process corner.

7.2 Avenues for future work

The positive feedback source coupled logic style offers an efficient way to implement digital circuits used in mixed signal applications. It has advantage of eliminating switching noise generated in CMOS based counterparts. Here, the work is done to increase fan-in capabilities, reduce footprints and achieve better performance at lower technology nodes. The use of memristors and CNTFET in PFSCl style is explored. Also, the use of tristate PFSCl buffers is extended for the design of registers.

Some of the avenues for future work that can be taken up are

1. Static memristor-based PFSCl gates can be extended to realize multi-valued logic (MVL) gates, where signals have more than two logic levels. The advantage of multi-level resistive states of memristors can be integrated with PFSCl style such that the new MVL PFSCl gates can increase the information density in mixed signal application with reduced complexity.
2. Memristor-based dynamic PFSCl gates can be used to design high performance pipeline architectures.
3. The proposed PFSCl registers can be further improved to operate reliably in the subthreshold region, while maintaining low power consumption and better noise tolerance.
4. The work on CNTFET based PFSCl gates can be extended to develop complex digital blocks to be used in microprocessors and communication systems.

The practical aspects for the fabrication of hybrid Memristor-CNTFET-PFSCl circuits involves constraints related to the lithography, BEOL co-integration and manufacturing defects. The integration of nanoscale CNTFET structures with CMOS layers requires extremely high overlay accuracy during lithography and misalignment between different layers may degrade device performance and fabrication yield. Thus, advanced lithography techniques, such as E-beam lithography required to achieve the desired patterning accuracy, may increase the fabrication complexity and cost. Additionally, in hybrid Memristor-CNTFET-PFSCl circuits, CMOS devices are first fabricated in the Front-End-of-Line (FEOL), followed by the integration of Memristors and CNTFETs in the Back-End-of-Line (BEOL) layers with the requirement of maintain processing temperature below approximately 400°C. This excessive thermal budget may degrade the previously fabricated CMOS devices and metal interconnects, thereby affecting device reliability and overall circuit

performance. Thus, these fabrication challenges are important considerations for the practical realization of hybrid Memristor-CNTFET-PFSCL circuits. Advances in nanofabrication and low-temperature processing techniques are expected to support the future implementation of such hybrid architectures.

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LIST OF PUBLICATIONS

List of Journal Papers

1. Shikha, Neeta Pandey, and Kirti Gupta. "Memristor-based architectures for PFSCl circuit realizations." *Circuits, Systems, and Signal Processing* 42, no. 8 (2023): 4985-5012.
2. Shikha, Neeta Pandey, and Kirti Gupta. "Memristor-aided dynamic positive feedback source coupled logic." *Journal of Circuits, Systems and Computers* 35, no. 05 (2026): 2550439.
3. Shikha, Kirti Gupta, and Neeta Pandey. "Register design in positive feedback source coupled logic for mixed-signal applications." *Analog Integrated Circuits and Signal Processing* 124, no. 3 (2025): 57.
4. Shikha, Kirti Gupta, and Neeta Pandey. "High-performance PFSCl edge-triggered registers." *International Journal of Circuit Theory and Applications* (2025).

List of International Conference Papers

1. Shikha, Neeta Pandey, and Kirti Gupta. "Realization of positive feedback source coupled logic even parity generator/checker." In *2023 7th International Conference on Computing, Communication, Control and Automation (ICCUBEA)*, pp. 1-6. IEEE, 2023.
2. Shikha, Kirti Gupta, Neeta Pandey, "Energy-efficient carry skip adder realization in positive feedback source coupled logic style" in *16th International IEEE Conference on Computing, Communication and Networking Technologies*, IEEE 2025. (Presented)

List of Journal Paper Under Communication:

1. Shikha, Kirti Gupta and Neeta Pandey. "Optimized CNTFET based PFSCl circuits for improved delay and energy efficiency" *Analog Integrated Circuits and Signal processing*. Under Revision

CURRICULUM VITAE



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Core Competences

- Exceptionally brilliant and superb academic records.
- Crystal clear understanding of the underlying principles of the subject.
- In-depth knowledge of various techniques and approaches applied at a research project.

Higher Qualification

- Ph.D. in Digital VLSI from Delhi Technological University (DTU) in 2026.
- M.Tech. in Electronics and communication engineering. From UIET KUK in 2013 with
- 8.3 CGPA (2nd topper).
- B. Tech in Electronics and communication engineering. From UIET KUK in 2011 with 71.3% with honors
- 12th from Uma Bharti Senior secondary school Rewari in 2007 with 75 %.
- 10th with 80% (merit holder) in 2005.

Teaching Experience

- Worked as an Assistant professor in UIET (University institute and engineering and technology) KUK from 2nd September 2013 to 31st May 2014.
- Worked as an Assistant professor in DTU (Delhi Technological University) from 24th July 2014 to 31st May 2021.
- Currently working as an Assistant professor in Bharati Vidyapeeth's college of engineering Delhi from 1st August 2021 to till date.

Workshop and FDP Attended

1. Workshop on “Robotics” held at UIET, KUK on April 3rd to 5th, 2009.
2. Workshop on “high vacuum techniques, plasma characterization and thin film

- deposition” held on 30th November to 2nd December, 2009.
3. C language training for months 27 may to 27 July 2010.
 4. Workshop on “hands on practice on lab view” held at university institute of engineering & technology kurukshetra, 9th to 10th December 2011.
 5. Two-day induction training short term course for the teacher working on contract basis organized by UGC academic staff college, Kurukshetra University, Kurukshetra held on 8th to 9th October 2013.
 6. Two-week ISTE workshop on “signal & system” conducted by IIT Kharagpur under national mission of education through ICT (MHRD govt. of India) on Jan 2nd to Jan 12th 2014.
 7. FDP on recent and development in “Microwave & RF engineering” held at university institute of engineering & technology Kurukshetra on May 5th to may 10th 2014.
 8. One-week technical education quality improvement program (TEQUIP-11, SUB COM.11) of ministry of human resource development government. of India sponsored national course on “advanced in signal process & communication engineering held at university institute of engineering & technology Kurukshetra on May 26th to may 31th 2014.
 9. FDP on recent trends in “Pattern analysis and machine learning”, 11-15 July 2016, held at DTU, Delhi.
 10. One-week short term training program on “advance in image processing and computer vision” Organize by Department of Electronics and Communication Engineering, Delhi Technological University, Delhi April 2-6 2018.
 11. One-week short term training program on “Industry Oriented STC on VLSI Design Tools” Organize by Electronics and Communication Engineering Department NITTTR, Chandigarh, 21/03/2022 to 25/03/2022.
 12. One-week short term training program on “Industry Oriented STC on VLSI Design Tools” Organize by Electronics and Communication Engineering Department NITTTR, Chandigarh, 9/05/2022 to 13/05/2022.
 13. 5-Day online FDP on the theme “Inculcating Universal Human Values in Technical Education” All India Council for Technical Education (AICTE) from 9th to 13th May, 2022.
 14. One-week short term training program on “challenges and opportunities in VLSI design” Organize by Electronics and Communication Engineering Department NITTTR, Chandigarh, 25.07.2022 to 29.07.2022.
 15. 3-Day online FDP on the theme “Developing Research Skills” Sri Balaji College of Engineering, Jaipur from 23.02.2023-25.02.2023.
 16. 2-Day online FDP on the theme “Application of LabVIEW and Simulink in control system” School of Electronics Engineering at VIT-AP University, Amaravati, on 18.03.2023- 19.03.2023
 17. 3-Day online FDP on the theme “The Key enablers for Future communications” School of Electronics Engineering at VIT-AP University, Amaravati, on 26.03.2023- 28.03.2023.

18. 4-Day online FDP on the theme “Design and Fabrication of VLSI and Nanomaterial based sensors, VIT Chennai from 4.03.2023 to 7.03.2023.
19. 5-Day online FDP on the theme “Role of communication in IOT/IOMT VIT Chennai from 3.04.2023-7.04.2023.
20. 1-Day online FDP on the theme “Design and Fabrication Techniques of an Antenna: TV & Radio to sensors” School of Electronics Engineering at VIT-AP University, Amaravati, on 8th April 2023.
21. 3-Day online FDP on the theme “Deep learning and artificial intelligence based digital image processing” VIT Chennai from 24.04.2023-26.04.2023.
22. 1-Day webinar titled “Technological advances in communication of electronics for this decade” on “National Technological Day”, 11.05.2023 organized by the department of ECE in collaboration with institutions’ innovation council, DTU.
23. Two days capacity building workshop on OBE and Accreditation process (NEP-2020: Towards holistic education) during 02-03 June, 2023 organized by BVEC, New Delhi
24. 5-Day online FDP on the theme “Exploring the scope of engineering mathematics in control system and signal processing” VIT Chennai from 12.06.2023-16.06.2024.
25. 5-Day online FDP on the theme “Advanced semiconducting material and devices” VIT Chennai from 18.06.2023-20.06.2023.
26. Five days short term course in hybris mode on “Emerging trends in ECE, BVCOE, New Delhi.
27. One-week FDP on “Scilab programming for beginners” Organize by Electronics and Communication Engineering Department NITTTR, Chandigarh, 24.07.2023 to 28.07.2023.
28. One-week FDP on “Sustainable development goals: challenges and opportunities” Organize by Electronics and Communication Engineering Department NITTTR, Chandigarh, 21.08.2023 to 25.08.2023.
29. One-week FDP on “IoT and embedded systems” Organize by Electronics and Communication Engineering Department NITTTR, Chandigarh, 21.08.2023 to 25.08.2023.
30. FDP on “Semiconductor fusion nexus” Integrating academic insights and industry innovations: at Vivekananda institute of professional studies-technical campus from 08.01.24 to 13.01.24.
31. One-week Faculty Development Programmed on Emerging Trends in Electronics and Communication Engineering “Machine Learning and Data Science” from 11-15 March 2024, organized by the Department of Electronics and Communication Engineering, Bharati Vidyapeeth’s College of Engineering, New Delhi.
32. One-week short term course on “Hands on training on IOT & its application from 30th April to 4th May 2024 organized by the department of instrumentation and control engineering, BVCOE, New Delhi.
33. One week FDP on “importance of accreditation, OBE and NEP-2020 in higher education” organised by internal quality assurance cell (IQAC) in the

collaboration with department of applied science from 27th to 31st May 2024.

34. Two-week online faculty development program on frontiers in materials research, innovations and entrepreneurship (FRIME'24) organized by the department of humanities and sciences (physics), held from 25.07.24 to 08.08.24.
35. 3 Day FDP on "Navigating the Landscape of IPR" from 19th to 21st September 2024, organized by Research and development cell and Intellectual property Right cell, Bharati Vidyapeeth's college of Engineering, New Delhi.
36. One week of FDP on "Recent trends in electric vehicle held from 2nd to 6th Sep 2024 organized by the department of electrical engineering, Northern institute of engineering technical campus, Alwar Rajasthan in collaboration with the institution of engineering and technology (KLN) Kolkata.

Publications

List of Journal Papers

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circuits for improved delay and energy efficiency” Analog Integrated Circuits and Signal processing. Under Review

List of Book Chapters

1. J. Gupta, Shikha, P. Gupta “Demystifying the internet of things: A deep dive into protocols, architectures, technologies and beyond”, Wireless Communication networks and Applications, ISBN: 978-93-6252-398-3, IIP Series.
2. Priyanka Gupta, Shikha, Monica Bhutani, Jyoti Gupta, Monica Gupta, “Charging Ahead: Breakthroughs in Electric Vehicle Battery Enhancement” Solving Fundamental Challenges of Electric Vehicles, ISSN:2328-8205 EISSN:2328-823X, A volume in the Advances in Mechatronics and Mechanical Engineering (AMME) Book Series (Scopus Indexed).
3. Ms. Shikha, Mr. Ravi Sharma, Dr. Laxya, Mr. Sheersh Kumar Garg, Mr. Rahul Garg, “Materials of Tomorrow: Unveiling Novel Advances
4. Advancing Innovation in Smart Systems, Energy, Materials, and Manufacturing: Unleashing the Potential of IoT, AI, and Edge Intelligence, ISBN: 978-93-6252-733-2.
5. Dr. Monica Bhutani, Dr. Jyoti Gupta, Ms. Shikha, Dr. Priyanka Gupta, Ms. Neetu Settia, “AI-Driven Wound Assessment: Leveraging Wearable Sensors For Clinical Innovation” Advancing Innovation in Smart Systems, Energy, Materials, and Manufacturing: Unleashing the Potential of IoT, AI, and Edge Intelligence, ISBN: 978-93-6252-733-2.
6. Ms. Shikha, Dr. Priyanka Gupta, Dr. Monica Bhutani, Dr. Jyoti Gupta, “Innovations In Energy: IOT And AI Perspectives
7. Neetu Singh, Shikha, Avinash Gola, Sidharth, “Empowering Tomorrow's Mobility: Innovations In Electric Vehicle Technology With Iot And Ai Integration
8. Advancing Innovation in Smart Systems, Energy, Materials, and Manufacturing: Unleashing the Potential of IoT, AI, and Edge Intelligence, ISBN: 978-93-6252-733-2.
9. Ms. Disha Tuteja, Ms. Raman Dhand, Ms. Neetu Singh, “Innovative Materials Exploring Ai-Enhanced Applications” Advancing Innovation in Smart Systems, Energy, Materials, and Manufacturing: Unleashing the Potential of IoT, AI, and Edge Intelligence, ISBN: 978-93-6252-733-2.
10. Dr. Jyoti Gupta, Dr. Monica Bhutani, Dr. Priyanka Gupta, Ms. Shikha, “IOT And AI In Smart Systems: Creating Synergies For Tomorrow's Challenges” Advancing Innovation in Smart Systems, Energy, Materials, and Manufacturing: Unleashing the Potential of IoT, AI, and Edge Intelligence, ISBN: 978-93-6252-733-2.
11. Dr. Monica Bhutani, Ms. Neetu Singh, Ms. Shikha, Satyam Solanki, “Next-Generation Smart Grids: Integrating IOT And AI For Efficient Energy Management

12. Advancing Innovation in Smart Systems, Energy, Materials, and Manufacturing: Unleashing the Potential of IoT, AI, and Edge Intelligence, ISBN: 978-93-6252-733-2.

Declaration

I hereby acknowledge that all the details given above are true and complete to the best of my knowledge & belief.