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DESIGN AND PERFORMANCE OPTIMIZATION OF NANO SCALE VEDIC MULTIPLIER ARCHITECTURE

A Thesis Submitted
In Partial Fulfillment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY
by

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Acknowledgements

"Success is not final, failure is not fatal: It is the courage to continue that counts."
— Winston Churchill

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Candidate's Declaration

I, **Hemanshi Chugh**, hereby certify that the work which is being presented in the thesis titled **"Design and Performance Optimization of Nano Scale Vedic Multiplier Architecture"**, in partial fulfillment of the requirements for the award of the Degree of Doctor of Philosophy, submitted in the Department of **Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **January 2021** to **July 2025** under the supervision of **Dr. Sonal Singh**.

The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.



Candidate's Signature

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.



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Certificate by the Supervisor

Certified that **Hemanshi Chugh** (Enrollment No.: 2K20/PHDEC/508) has carried out their research work presented in this thesis titled **"Design and Performance Optimization of Nano Scale Vedic Multiplier Architecture"** for the award of **Doctor of Philosophy** in the Department of Electronics and Communication Engineering, Delhi Technological University, under my supervision. The thesis embodies results of original work and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or anybody else from this or any other University/Institution.



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With deep gratitude, I dedicate this thesis to my parents,
Mr. Krishan Baldev Chugh and Mrs. Sunita Chugh,
and to my dear husband, Mr. Chirag Malhotra,
for their boundless support, constant encouragement,
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Abstract

The persistent trend towards device miniaturization of electronic devices has made apparent the structural and operational limitations of the conventional CMOS technology such as increased leakage currents, excessive power dissipation, and challenges in further scaling. These issues have become critical bottlenecks to the sustained evolution of high-performance, energy-efficient computing systems. As CMOS technology approaches its physical limits, it is imperative to explore alternative paradigms that can sustain the trajectory of Moore's law while overcoming the inherent drawbacks of conventional transistor-based designs.

Quantum-Dot Cellular Automata (QCA) has emerged as a compelling post-CMOS technology, offering computation through the manipulation of electron positions rather than current flow. This unique mechanism enables ultra-low power operation, high device density, and fast switching speeds, positioning QCA as a promising candidate for next-generation nanoelectronic circuits.

This thesis aligns with this paradigm shift by addressing the critical challenge of efficient multiplier design through the integration of Vedic mathematics with QCA and reversible logic principles.

The primary objective of this research is to develop scalable, low-power Vedic multiplier architectures that are both computationally efficient and suitable for nanoelectronic implementation. To achieve this, the research begins with the development and evaluation of novel CMOS-based Vedic multiplier architectures, establishing a performance baseline and highlighting the constraints posed by CMOS technology in terms of energy and delay.

Building on this foundation, the research transitions into the QCA domain, where

optimized half and full adder layouts are designed which serve as building blocks for advanced adders such as Ripple Carry Adders (RCAs) and Carry Save Adders (CSAs). These designs incorporate coplanar and multilayer crossover strategies to address interconnect complexity while minimizing area and latency. A comprehensive evaluation of energy efficiency, quantum cost, and thermal behavior under varying cell sizes and temperatures is conducted using QCADesigner-E and QCAPro tools. Leveraging these optimized adder designs, the research further proposes a novel Vedic multiplier architecture implemented within the QCA framework, demonstrating significant improvements in computational efficiency and suitability for nanoelectronic applications.

In the final phase, the study introduces reversible logic into the QCA framework to further enhance energy efficiency. Two novel Vedic multiplier architectures, constructed using QCA-based Peres and BME reversible gates, are proposed. The results show a substantial reduction in power-delay product (PDP), with the reversible QCA-based multiplier achieving a PDP improvement of several orders of magnitude compared to its CMOS counterpart.

Collectively, these contributions reflect a systematic and innovative approach to arithmetic circuit design, combining ancient computational methods with emerging nanoelectronic technologies. The proposed architectures exhibit strong potential for use in high-performance, low-power applications such as signal processing, cryptography, biomedical electronics, and next-generation arithmetic processors.

List of Publications

SCI/SCIE Journals

1. **Hemanshi Chugh** and Sonal Singh (2024). Systematic exploration of N-Bit Vedic multipliers: A roadmap of technological approaches in pursuit of future trends. Nano Communication Networks, 100529. (Elsevier, Impact Factor 2.9)

2. **Hemanshi Chugh** and Sonal Singh (2024). Efficient co-planar adder designs in quantum dot cellular automata: Energy and cost optimization with crossover elimination, Integration, 94, p.102103. (Elsevier, Impact Factor 2.2)

3. **Hemanshi Chugh** and Sonal Singh (2024). Efficient quantum-dot adder optimization and analysis for future circuits, International Journal of Electronics, pp 1-21. (Taylor & Francis, Impact Factor 1.1)

4. **Hemanshi Chugh** and Sonal Singh (2025). An energy and cost-effective realization of high-performance single-layer vedic multiplier in quantum-dot cellular automata, Physica Scripta, 100, 065112. (IOP Publishing, Impact Factor 2.6)

IEEE International Conferences

1. **Hemanshi Chugh**, and Sonal Singh, "Design and implementation of a high-performance 4-bit Vedic multiplier using a novel 5-bit adder in 90 nm technology" in 2022 10th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions)(ICRITO), 2022, pp. 1-6, IEEE.

2. **Hemanshi Chugh**, and Sonal Singh, "Parametrical analysis and thermal sensitivity study of 8-bit Vedic multiplier", In 2023 14th International Conference on Computing Communication and Networking Technologies (ICCCNT), 2023, pp. 1-6, IEEE.

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List of Abbreviations

CMOS	Complementary Metal Oxide Semiconductor Field Effect Transistor rithmetic logic
VLSI	Very Large Scale Integration
DSP	Digital Signal Processing
ALU	Arithmetic and Logic Unit
VM	Vedic Multiplier
HA	Half Adder
FA	Full Adder
CSA	Carry Save Adder
RCA	Ripple Carry Adder
CLA	Carry Lookahead Adder
UT	Urdva Tiryakbhyam
PDP	Power Delay Product
EDP	Energy Delay Product
LUT	Lookup Table
MUX	Multiplexer
CC	Cell Count
GC	Gate Count
TC	Transistor Count
m-GDI	Modified-Gate Diffusion Input

Mc-CMOS	Multiple channel Complementary Metal Oxide Semiconductor Field Effect Transistor
HDL	Hardware Description Language
FPGA	Field Programmable Gate Array
QCA	Quantum-dot Cellular Automata
QCAD	Quantum-dot Cellular Automata Designer v2.0.3
MG	Majority Voter Gate
INV	Inverter Gate
CO	Crossover
CV	Coherence Vector Simulation Engine
TED	Total Energy Dissipation
AED	Average Energy Dissipation
Cost_{AD}	Area-to-Delay Cost
FoM	Figure of Merit
Cost_{ED}	Energy-to-Delay Cost
SF	Scaling Factor
AOP	Average Output Polarization
QCA-3x4B-CSA	QCA Based Three-input 4-bit Carry Save Adder
SCOD	Single Cell Omission Defect
DCOD	Double Cell Omission Defect
ECDD	Extra Cell Deposition Defect

List of Symbols

ϕ	Phase
ϵ_r	Relative Permittivity
U_T	Total Potential Energy
$\hbar$	Reduced Planck Constant
$\vec{\lambda}$	Coherence Vector
$\vec{\Gamma}$	Three-dimensional Energy Vector
E_k	Tunneling Energy

Chapter 1

Introduction

Binary addition and multiplication are essential operations for high-performance systems, particularly for microprocessors and DSP (Digital Signal Processing) applications. Multipliers are the primary and extensively used operations in various computer systems, and their VLSI implementation requires high speed, low power consumption, and design regularity in less area [1]. Multiplication involves three main stages, including partial product creation, reduction of partial products, and addition of carry propagation [2] as shown in Figure 1.1. Reducing partial products is crucial for power

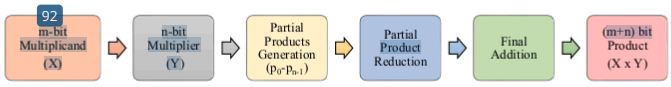


Figure 1.1: Basic multiplication process

and delay trade-offs. There are two categories of multiplier architecture: signed and unsigned. Different multiplier architectures, such as Array, Booth, Wallace Tree, Baugh Wooley, and Vedic, have been developed to simplify multiplication. Figure 1.2 shows a comparative illustration of the performance parameters of different multiplier architectures. It highlights the strengths and weaknesses of each architecture in terms of speed, power consumption, area utilization, regularity, and complexity. This comparison provides insights into the suitability of each architecture for various applications based on their performance requirements. Array multipliers are systematic and structured multipliers [3] that use the addition and shift algorithm, providing simple interconnections but significant delay [4, 5]. The Booth algorithm is used for multiplying signed numbers and uses the 2's complement form of binary numbers for multiplication. It checks three bits simultaneously, but its disadvantage is high power consumption [6]. The Wallace tree multiplier is faster than the array multiplier but has a complicated layout design [7, 8]. The Baugh-Wooley multiplier is effective for multiplying signed numbers and has a regular multiplication array, but requires a large routing area due to its hardware complexity[9]. Ancient Vedic mathematics has proven to be fast and highly efficient due to its regular and simple architecture,

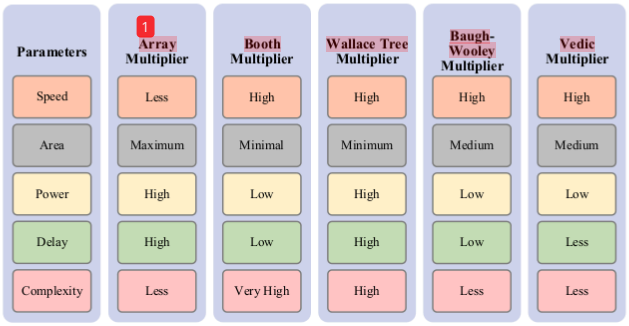


Figure 1.2: Comparison of multipliers

providing relatively fast, area, and power-efficient multiplier designs[10]. The thesis provides a detailed discussion of the Vedic multiplication process, specifically using the widely used Urdhva Tiryagbhyam (UT) sutra. This sutra is explained thoroughly, including its application in various scenarios and how it simplifies the multiplication process. The manuscript covers the steps involved in the Vedic multiplication algorithm, including the creation of partial products and their subsequent additions. The advantages of using the Vedic multiplication method are also highlighted, such as its simplicity, regularity, and speed, which make it a popular choice for many applications.

1.1 An Insight into Vedic Mathematics Sutras

Vedic mathematics is a system of prehistoric Indian mathematics that uses 16 principles that apply to different fields of mathematics, as indicated in Table 1.1. Further, Figure 1.3 present the classification of these Vedic sutras pertaining to various fields of mathematics. Multiplication stands out as a crucial operation despite the fact that there are many ways to improve the performance of DSP applications. Vedic multiplication, one of the most renowned methods for enhancing multiplication, generates both partial products and their sums concurrently. Therefore, the signal propagation time through the circuit is minimized, as a result of which the overall efficiency of the circuit is improved.

Table 1.1: Vedic mathematics technique

Vedic Sutra	**Meaning**
Urdhva Tiryagbyham	Vertically and crosswise
Yaavadunam	Whatever the extent to fits deficiency
Ekadhikina Purvena	By one more than the previous one
Ekanyunena Purvena	By one less than the previous one
Paraavartya Yojayet	Transpose and adjust
Puranapuranabyham	By the completion or non-completion
Sankalana-vyavakalanabhyam	By addition and by subtraction
Shesanyankena Charamena	The remainders by the last digit
Shunyam Saamyasamuccaye	When the sum is the same that sum is zero
Sopaantyadvayamantyam	The ultimate and twice the penultimate
Gunakasamuchyah	The factors of the sum is equal to the sum of the factors
Vyashtisamanstih	Part and Whole
Anurupye Shunyamanyat	If one is in ratio, the other is zero
Chalana-Kalanabyham	Differences and Similarities
Gunitasamuchyah	The product of the sum is equal to the sum of the product
Nikhilam Navatashcaramam Dashatah	All from 9 and the last from 10

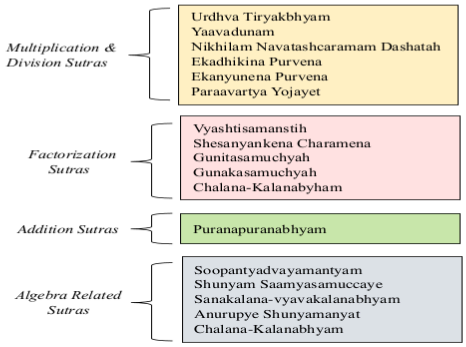


Figure 1.3: Categorisation of Vedic sutras

1.2 Urdhva Tiryagbhyam: A Path to Efficient Computation

Vedic mathematics offers a comprehensive approach to multiplication known as the Urdhva-Tiryagbhyam Sutra, which can be utilized in all instances of multiplication. The term Urdhva-Tiryagbhyam comes from the Sanskrit language, where, Urdhva means vertical and Tiryagbhyam means transverse. Vertical multiplication involves

multiplying the digits in the same position and vertically adding the results to produce the final answer. Transverse multiplication involves multiplying the digits diagonally and horizontally adding the results to generate the solution. By combining these two methods, the UT sutra can handle any multiplication scenario, making it a valuable tool in Vedic mathematics. Compared to other multipliers such as array, Booth, and Wallace tree, Vedic multiplication using the UT technique outperforms in terms of delay.

For an NN multiplication in general form, the procedure follows the "divide and conquer" approach by breaking down larger bit multiplication (NN, with N bits each) into smaller bits of size $(N/2 = n)$, which can be further decomposed into smaller bits of $n/2$ each up to the basic 2×2 multiplier block (shown in Figure 1.4). This regular and simplified algorithm results in a compact layout and reduction in overall runtime.

The architecture of an n-bit Vedic multiplier using the UT technique involves the

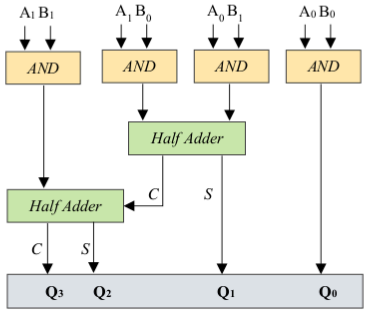


Figure 1.4: 2-bit VM basic module

following steps:

1. Partition the n-bit multiplicand and multiplier into two equal parts each: upper and lower parts.
2. Multiply the upper parts of the multiplicand and multiplier using conventional multiplication and obtain a partial product of size 2n bits.
3. Multiply the lower parts of the multiplicand and multiplier using conventional multiplication and obtain another partial product of size n bits.

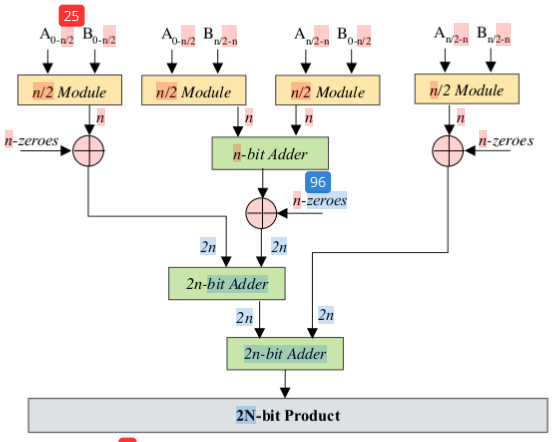


Figure 1.5: General Vedic module for n-bit multiplication

4. Add the partial products obtained in steps 2 and 3, which gives an intermediate product of size 3n bits.

5. Use the Urdhva Tiryagbhyam technique to obtain the n-bit product from the intermediate product obtained in step 4.

The Urdhva Tiryagbhyam technique involves the following steps:

1. Divide the intermediate product obtained in step 4 into two equal parts: upper and lower parts.

2. Add the upper and lower parts separately to obtain two intermediate results.

3. Shift the upper intermediate result to the left by n bits.

4. Add the shifted intermediate result and the lower intermediate result to obtain the final product.

An efficient architecture of an n-bit Vedic multiplier using the UT technique, shown in Figure 1.5, reduces the number of partial products and additions required as compared to the traditional multiplication methods.

1.3 Understanding Quantum-Dot Cellular Automata: A New Era in Computing

Over the past three decades, Moore's Law has accurately predicted the exponential growth in the number of transistors produced annually, with an astonishing increase by nearly eight orders of magnitude [11]. However, as with any exponential trend, this growth is now approaching its physical limits, particularly in CMOS technology, where further miniaturization is increasingly difficult and costly. These constraints have driven researchers to explore alternative technologies that can sustain progress in nanoelectronics. One such promising technology is Quantum-Dot Cellular Automata (QCA), which presents a novel design paradigm focused on minimizing area and power consumption while maintaining high-speed operation [12, 13].

Given the parallels between CMOS and QCA design, it is logical to adapt the well-established CMOS design process to QCA, with necessary adjustments. This new QCA design process enables the efficient layout of large-scale QCA devices, contributing significantly to the advancement of the technology. Throughout the history of CMOS design, the process has been continuously refined to optimize transistor-level system design, employing a top-down approach that emphasizes verification at each stage to minimize errors. In the context of QCA, the structural logic model is modified to incorporate the characteristics of quasi-adiabatically switched QCA cells instead of CMOS devices. Subsequent steps in the design process parallel those in CMOS design, but with QCA cells replacing CMOS transistors in logic models and component layouts.

QCA technology, thus opens up new avenues for exploring innovative design paradigms distinct from conventional CMOS, enabling the implementation and testing of circuits that prioritize minimizing area and power consumption while maintaining high-speed operation.

1.3.1 The Essentials of QCA: A Foundational Overview

A Quantum-dot Cellular Automata cell is a square device composed of four quantum dots connected by tunneling barriers, forming potential sites for two free electrons. These electrons can tunnel between the dots but cannot escape the cell [14]. Typically, these four-dot QCA cells are constructed from semiconductor materials like Si/SiO_2 or GaAs/AlGaAs, with each square-shaped quantum cell having a standard size of

18×18 nm and a spacing of 2 nm between neighboring cells as displayed in Figure 1.6. The electronic charge density at each corner of the square, denoted as ρ_i (where

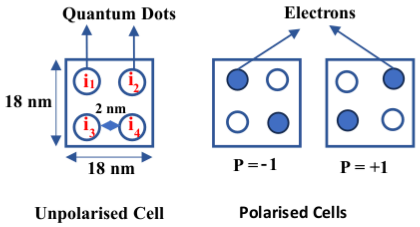


Figure 1.6: Polarization states of QCA cell

$i = 1, 2, 3, 4$), determines the cell's polarization (P) as defined by Eq. 1.1:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_2 + \rho_3 + \rho_4)} \tag{1.1}$$

As a result of electron–electron repulsion, electrons occupy diagonal positions within the cell, leading to two clearly defined polarization states, as shown in Figure 1.6. The polarization of a QCA cell is linearly influenced by neighboring quantum cells through electrostatic forces, with information propagation occurring via Coulombic interactions. These interactions cause the cell to switch bi-stably between the two polarization states. If the free electrons are positioned diagonally at i_1 and i_3, the cell polarization is +1, as given in Eq. 1.2.

$$P = \frac{(\rho_1 + \rho_3) - 0}{(\rho_1 + 0 + \rho_3 + 0)} = +1 \tag{1.2}$$

Conversely, if the electrons are positioned diagonally at i_2 and i_4, the cell polarization is -1, as described by Eq. 1.3.

$$P = \frac{0 - (\rho_2 + \rho_4)}{(0 + \rho_2 + 0 + \rho_4)} = -1 \tag{1.3}$$

The logic values 0 and 1 in binary have polarizations of -1 and +1 respectively in QCA cells [13].

In irreversible calculation, it has been proved that if the one-bit information is lost, the dissipated energy E_d can be given as:

$$E_d = K_b log_2 T \tag{1.4}$$

where K_b is the Boltzmann constant which approximately equals to $1.3806505 \times 10^{-23}$ JK^{-1} and T is the operating temperature. QCA cells perform computations by leveraging Coulombic interactions, where the polarization of each cell is influenced and determined by the polarization of its neighboring cells. Unlike CMOS technology, QCA cells do not exchange electrons during information processing; instead, they rely on the arrangement of electrons, known as polarisations, to interact directly with neighboring cells.

QCA wire: The information flow is enabled by arranging quantum cells in series, where cells are capacitively coupled to their neighbors through Coulombic interactions [14]. This coupling allows the cells to share the same polarization within the QCA array, facilitating the transmission of information. When an input is applied to the first standard 90° QCA cell at the left end of the line (denoted as X in Figure 1.7), it forces the cell into a specific polarization, breaking the degeneracy of the ground state, creating a higher energy state. To reach a new ground state, all subsequent

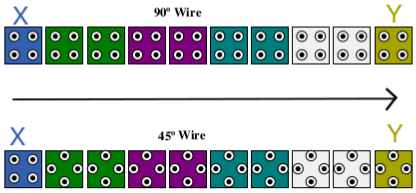


Figure 1.7: Information transfer using QCA wire

cells in the line must flip their polarization accordingly, ensuring that the polarization is propagated through the entire array of quantum cells. A significant advantage of QCA devices is the simplified interconnect, as the cells only communicate with their nearest neighbors, eliminating the need for long interconnect lines. The computation proceeds as inputs are applied to the cells at the edge of the system, and the output emerges at the opposite edge of the QCA array [13]. A QCA wire can also be comprised of cells oriented at 45°. With this orientation, as the binary value propagates down the length of the wire, it alternates between the polarization $P = +1$ and -1. The significant advantage of the 45-degree wire is that both a transmitted value and its complement can be obtained from a wire without the use of an explicit inverter [13].

QCA Clock: Unlike the traditional CMOS clock, which operates with just high and low phases, the clock mechanism in QCA is more complex and involves multiple phases. The primary function of the QCA clock is to stabilize the polarization of a set of cells, which in turn allows other cells to adjust their states accordingly. Unlike traditional systems, individual QCA cells are not timed independently. Instead, the cells are organized into sub-arrays as illustrated in Figure 1.7. The QCA clock controls the potential barriers that influence a group of QCA cells, known as a "clock zone". These barriers can be raised, lowered, or maintained in their current state, corresponding to the four distinct clock phases. All cells within a particular clock zone operate in the same phase, and a full clock cycle is completed when the clock zone progresses through all the four phases [13]. This clocking scheme is vital for

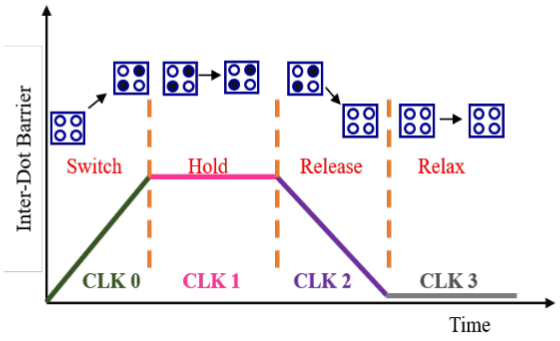


Figure 1.8: Clock zones in QCA

enabling efficient and synchronized data transfer within a QCA circuit. The four pipelined clock zones, designated as CLK0, CLK1, CLK2, and CLK3, operate with a phase difference of 90° relative to the preceding zone [13]. The phase for each clock zone is calculated using Eq. 1.5, where i represents the clock zone:

$$\phi_i = i \times \frac{\pi}{2} \tag{1.5}$$

Therefore, the clock 0 has $\phi = 0$, clock 1 has $\phi = \frac{\pi}{2}$, clock 2 has $\phi = \pi$ and clock 3 has $\phi = \frac{3\pi}{2}$. The QCA clocking mechanism consists of four phases: switch, hold, release, and relax, as shown in Figure 1.8. During the switch phase (the first clock

phase), QCA cells start in an unpolarized state with low inter-dot potential barriers. As the barriers are raised, the cells become polarized based on the state of their input cell, and the actual computation or switching occurs. By the end of this phase, the barriers are high enough to prevent electron tunneling, switch the cells into a fixed state [13].

In the hold phase (the second clock phase), the barriers remain high, allowing the outputs of one sub-array to serve as inputs for the next stage of the circuit. The release phase (the third clock phase) then lowers the barriers, permitting the cells to return to an un-polarized state. Finally, in the relax phase (the fourth clock phase), the barriers stay lowered, and the cells maintain their un-polarized state [13]. These four phases ensure the synchronized operation of the QCA circuit by carefully coordinating the movement of electrons within the cells. The precise timing and characteristics of each clock phase are essential for reliable information processing and the overall functionality of QCA circuits.

QCA Inverter and Majority Voter Gate basics: To implement complex logical functions in QCA, a set of basic logical gates is essential. For instance, constructing a multiplexer, decoder, or adder would be impossible without fundamental gates like the AND gate, OR gate, or inverter. One of the most crucial designs in QCA is the *NOT* gate. In this design, cells positioned diagonally to each other exhibit Coulombic

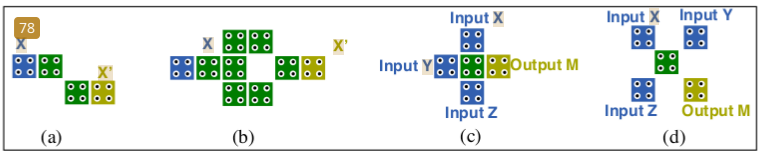


Figure 1.9: QCA configurations for the circuits (a) INV1 (b) INV2 (c)MG1 (d)MG2

repulsion, leading to reverse polarization. The two alternative layouts of the inverter gate are illustrated in Figure 1.9a and 1.9b, where the blue cells represent the input cell X, and the yellow cells indicate the output cell X'.

Another critical component in QCA circuits is the majority voter (MG) gate [15]. The gate typically features three inputs, one device cell, and one output as shown in Figure 1.9c and 1.9d. The output state of the MG gate is determined by the majority polarization of its inputs. The Boolean equation for the 3-input MG gate is provided

in Eq. 1.6:

$$M = XY + YZ + XZ \tag{1.6}$$

Logical function equation of QCA-AND-Logic and QCA-OR-Logic gate is represented in Eq. 1.7, and Eq. 1.8. Table 1.2 presents the verification of MG gate followed by the AND and OR logic gate of QCA by fixing one input.

$$Logical\ AND\ M(X, Y, 0) = X.Y \tag{1.7}$$

$$Logical\ OR\ M(X, Y, 1) = X + Y \tag{1.8}$$

Table 1.2: Truth table for MG gate, logical AND, and logical OR gate

Function	Inputs (X, Y, Z)			Output
	X	Y	Z	M
Majority Voter Gate (MG)	0	0	0	0
	0	0	1	0
	0	1	0	0
	0	1	1	1
	1	0	0	0
	1	0	1	1
	1	1	0	1
	1	1	1	1
Logical AND, Z (fixed input) = -1	0	0	0	0
	0	0	1	0
	0	1	0	0
	0	1	1	1
Logical OR, Z (fixed input) = +1	0	0	0	0
	0	0	1	1
	0	1	0	1
	0	1	1	1

The QCA implementation of two-bit logical AND and OR operations can also be easily achieved, as shown in Figure 1.10 [16]. The orange cell represents the cell with a fixed polarization of -1 or +1. It is important to note that because the MG gate allows for the generation of both AND and OR functions, and since the inversion of a signal value is also possible, the QCA logic set is functionally complete. This means that any logical circuit can be implemented using QCA devices. Consequently, with majority gates and inverters, all combinational and sequential circuits can be realized.

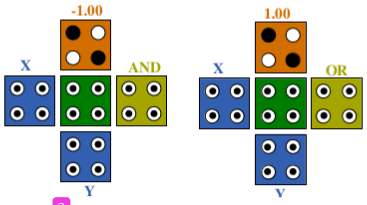


Figure 1.10: Logical AND and OR operation in QCA

QCA Crossovers: In the design of QCA circuits, two crossover processes are feasible: the coplanar crossover, which utilizes a single layer, and the multi-layer crossover, which involves more than one layer of quantum cells. The "QCA coplanar crossover" was proposed as a means of crossing signal wires on one plane so that completely planar circuits could be designed. The single-layer crossover is implemented using two distinct ways: one as the *rotated crossover* and the other as the *logical crossover*. To implement the rotated wire-crossing technique, the cells in the horizontal wire

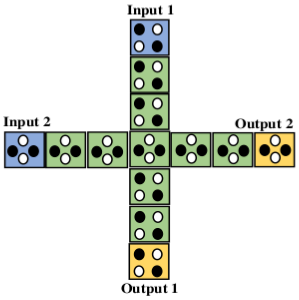


Figure 1.11: Rotated coplanar crossover

are rotated by 45 degrees, as depicted in Figure 1.11, while the vertical wire consists of standard 90 degree cells. This crossover is based on the fact that when placed adjacent to each other, a regular cell with dots arranged along the diagonals and a cell with the orientation of the dots rotated by 45 degrees (rotated cell) have very little mutual interaction. For effective signal transmission without interference from the crossing wire, the vertical wire must contain a sufficient number of cells (typically

three or more) beyond the intersection point. Additionally, the number of cells in the horizontal wire must be odd due to the characteristics of the rotated cells. The 45-degree rotation introduces additional spacing between the cells, which significantly decreases the energy separation between the ground state and the first excited state. This reduction in energy separation can negatively impact the device's performance in terms of maximum operating temperature, resistance to entropy, and minimum switching time [17].

Further, another wire-crossing technique was proposed by [18]. The principle of the relation between ground and excited states is as follows: The typical QCA clocking mechanism is divided into four stages as described earlier. During the switch and release stages, the tunneling barriers are either still rising or lowering, which can lead to duplicate states between the ground and excited states. In the hold and relax stages, the states are fixed as either the ground state or the excited state, respectively, because the tunneling barriers are fully raised or lowered. Data transmission between

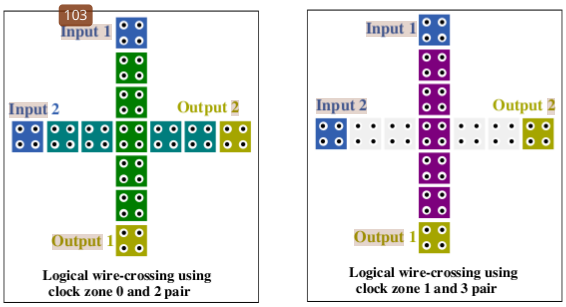


Figure 1.12: Logical coplanar crossover

adjacent cells is highly dependent on their respective clock zones. If two adjacent cells are in different clock zones where one cell is in the hold stage and the other is in the switch stage, data transmission occurs. The fixed polarization value in the hold-stage cell induces the same polarization in the switch-stage cell due to the Coulomb repulsion, causing a transformation from the excited state to the ground state.

Conversely, if the adjacent cells are in clock zones where one is in the hold stage and the other is in the release stage, or if both are in the switch or release stages, data transmission does not occur. This is because each clock zone is transitioning to

a different state. When one cell is in the hold stage and the other in the relaxed stage, they are in different states (ground and excited), and no Coulomb repulsion occurs between them, resulting in no data transmission without interference. Therefore, logical crossover can be successfully achieved between two adjacent cells when they are in clock zones 0 and 2 or in clock zones 1 and 3, as there is no interference at these stages as demonstrated in Figure 1.12.

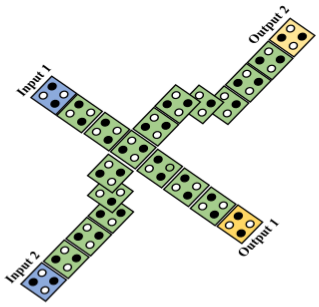


Figure 1.13: QCA multilayer crossover

The ability to cross QCA signals is crucial for even the simplest designs. The complex circuits using coplanar crossover are very likely to fail. Therefore, the use of multilayer QCA cells allows the signals to cross between different layers. Using a vertical interconnect, signals can be transmitted vertically from one layer to another, where they can then continue to propagate horizontally. In the "multilayer wire-crossing" technique as illustrated in Figure 1.13, a cross-bridge method is employed. This approach, while visually similar to the coplanar technique, is distinct in its three-dimensional structure. The horizontal chain of cells crosses over another layer using this bridge, which allows for further miniaturization and generalization of the design without the need to rotate the cells. They employ 90° wires to establish a bridge-type structure, with distinct functions assigned to the lower, middle, and upper layers. It can be seen that the polarization of the cells in a line alternates with that of each cell in every layer, but the magnitude of the polarization does not change. Therefore, multi-layer crossover requires a minimum of three layers, namely : the main layer, the vertical via layer, and the crossover layer. The cell size of the via and the crossover is the same as that of the main layer cells. The standard size is considered as $18 \times 18nm$

[19]. The vertical separation between these layers can be adjusted to align with the kink energy (E_{kink}) of the horizontally arranged cells. Unlike traditional CMOS integrated circuits, where metal layers are used solely to connect separate sections of a circuit without performing any computational functions, the additional layers in QCA circuits can serve as active components. This multilayer approach has the potential to significantly reduce the area required for QCA circuits compared to planar designs. However, despite its advantages, this technique can introduce noise problems between cells at intersection points within the crossover area and can involve higher costs and intricate designs [20].

1.4 Research Gaps

- While extensive studies have been conducted on Vedic multiplier architectures focusing on power, delay, and area, there is a notable gap in understanding how these architectures perform in terms of energy consumption under varying temperature conditions. The analysis of energy efficiency, particularly in relation to temperature fluctuations, remains unexplored in the context of CMOS technology. This research aims to investigate the impact of temperature variations on the energy consumption of Vedic multipliers, providing a comprehensive understanding of their thermal performance and potential design optimizations for energy-efficient computing.

- QCA technology is a recent and emerging field that offers promising alternatives to conventional CMOS technology, primarily due to its potential for lower power consumption and higher speed. While there has been progress in this field, the design and optimization of basic adder circuits using QCA across various wire schemes, still hold significant potential for exploration. This gap provides an opportunity to investigate the unique challenges and advantages of QCA-based adder circuits, including their structural configurations, efficiency, and scalability. By exploring these aspects, researchers can contribute to advancing low-power, high-speed computing applications and enhancing our understanding of how QCA technology can be optimized and applied effectively.

- The domain of Vedic multiplication within Quantum-dot Cellular Automata technology is still in its early exploration stages. Currently, there is a noticeable

absence of comprehensive performance analyses and implementations of Vedic multipliers in this technology. This nascent stage presents extensive possibilities for research and innovation, particularly in optimizing Vedic multipliers for improved efficiency, speed, and power consumption in QCA frameworks. Addressing these gaps, this thesis aims to conduct a detailed investigation into a novel 2-bit Vedic multiplier design, providing a foundational analysis that can guide future advancements in the field. By exploring this relatively untapped area, the research seeks to contribute significantly to the development of efficient multiplier circuits in QCA technology.

- Reversible logic can be synergistically combined with QCA technology to create innovative multiplier architectures. While both technologies individually offer distinct advantages, their integration for multiplier architectures remains underexplored. This research gap focuses on the potential benefits of combining reversible logic principles with QCA-based designs to develop novel Vedic multiplier architectures to achieve minimal power loss, increased computational efficiency, and reduced physical size, making them highly suitable for advanced computing applications.

1.5 Research Objectives

Based on a thorough review of the literature and identified research gaps, the following objectives have been established:

- Design of energy efficient n-bit Vedic multiplier architecture with improved electrical parameters in CMOS technology.
- To design and implement Majority gate-based adder circuits using different wire schemes in QCA technology.
- Design and implementation of Cellular Automata-based Vedic multiplier using designed adders to analyse performance in terms of complexity, area, delay, and cost functions.
- Design and implementation of a Novel Reversible Vedic multiplier architecture in quantum cellular automata.

1.6 Organization of Thesis

The primary focus of this research is on design and performance optimization of nano scale Vedic multiplier architecture. The organization of the research work is presented in a chapter-wise format in this thesis, as follows:

Chapter 1

This chapter aims to systematically explore N-bit Vedic multipliers and provide a road-map of technological approaches in line with current trends. By surveying existing research, key gaps are identified, which form the basis for establishing the objectives of this work. Following the identification of these research gaps and objectives, a brief overview of the thesis layout is provided.

Chapter 2

In this chapter, the working principles and performance parameters of CMOS and QCA-based Vedic multipliers are briefly explained. It also includes technological classification review of available Vedic multipliers in literature.

Chapter 3

This chapter focuses on implementing 4-bit and 8-bit Vedic multipliers using the Urdhva Tiryagbhyam algorithm, based on a 90 nm CMOS node technology file via Cadence Virtuoso. The proposed Vedic multiplier architectures are thoroughly compared with traditional CMOS multipliers across various performance parameters, including delay, area, power delay product (PDP), and energy-delay product (EDP). Additionally, the study investigates the thermal sensitivity of these multipliers by analyzing their energy consumption in response to temperature variations.

Chapter 4

This chapter presents the design and implementation of novel adder modules, including half adder, full adder, ripple carry adder (RCA), and carry save adder (CSA) in QCA technology using the majority voter gate with coplanar and multi-layer crossover techniques. The functionality of the proposed structures has been validated through simulations using QCADesigner Tool v2.0.3. Additionally, precise energy calculations were performed using both QCADesigner-E and QCAPro, providing accurate insights into energy dissipation. Further, these proposed adder circuits demonstrate improved circuit efficiency and streamlined layouts compared to previously reported research models.

Chapter 5

This chapter delves into the development of an optimized QCA-based 2-bit and 4-bit Vedic multiplier, a fundamental component in digital arithmetic operations. The proposed multiplier employs a cell-interaction-based coplanar architecture, leveraging the principles of Coulomb repulsion to propagate information among cells in QCA technology. This approach results in a highly efficient and compact design that significantly outperforms existing QCA-based multipliers.

Chapter 6

The primary focus of this chapter is on implementing Vedic multipliers using reversible logic gates within the QCA framework. It introduces novel single-layer QCA implementations of the reversible Peres and BME gates, optimized for minimal clock-cycle delay. These gates serve as building blocks for developing two distinct QCA designs of reversible Vedic multipliers (RVM1 and RVM2), which aim to reduce hardware complexity, enhance speed, and lower power dissipation. The results highlight the potential of combining reversible logic with QCA technology to advance digital circuit design. Additionally, comprehensive energy dissipation and performance analyses were conducted using the QCADesigner-E and QCAPro tools.

Chapter 7

This chapter provides a summary of the research presented in the thesis, along with suggestions for future work and its potential social impact.

Chapter 2

Literature Review and Design Strategies for Vedic Multipliers

2.1 Introduction

One of the most important parts of digital circuits is an ALU, or arithmetic logic unit. Various mathematical operations, including addition, subtraction, multiplication, division, and logical operations like AND, OR, NOT, XOR, etc. are performed on binary data [21]. For a variety of DSP (Digital Signal Processing) and DIP (Digital Image Processing) applications [22, 23], powerful microprocessor systems frequently use addition and multiplication operations extensively [24]. The published literature has documented numerous modified multiplier architecture implementations. This chapter mainly focuses on the following:

- Technology-centered classification of implementations of Vedic multipliers (VM). This manuscript focuses mainly on software simulation-based analysis of various modifications of the n-bit Vedic multiplier.
- A comprehensive comparative analysis is performed on the commonly used performance metrics for the design analysis to identify the best-performing technology for the Vedic multiplier.
- The bit-wise classification of the Vedic Multiplier gives a clear overview of the architectural significance of the technology used for different bit sizes.

The circuit's functional verification approaches have been comprehensively categorized from a holistic perspective, as depicted in Figure 2.1. By comprehensively analyzing and classifying VM implementations, it is observed that the digital implementation and functional verification of any circuit can be done with various front-end or back-end EDA tools as shown in Figure 2.2. However, this thesis further focuses on the designs and simulation of the Vedic N-bit multiplier [10] with back-end EDA tools, which provide a deep insight into the implementation of the most efficient "Urdhva-Tiryagbhyam" technique of Vedic multiplication by examining more than 100 research

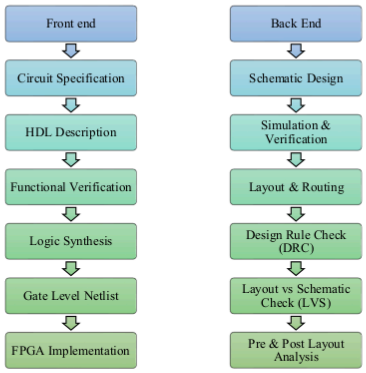


Figure 2.1: VLSI design and implementation

papers from IEEE, Springer Link, Elsevier, IET and Google Scholar. Architectural

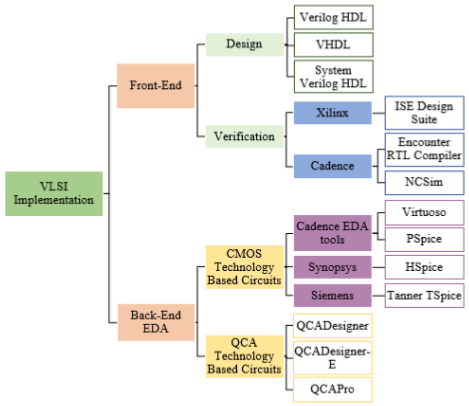


Figure 2.2: The taxonomy of functional verification of Digital circuits

design includes the development of the functional blocks and the communication protocol between these blocks, which are modeled using a Hardware Description Language (HDL) such as Verilog, VHDL, or System Verilog. The functional verification

phase is a method of proving the correctness of the design using synthesis, a process of converting the HDL design into a technology-specific gate-level netlist while taking into account all the constraints and optimization settings specified. This phase is referred to as the "front end" of the VLSI design. According to literature reports, synthesis is mainly performed using the Xilinx ISE design suite [25] or Cadence tools [26] such as the Encounter RTL compiler and NCSim.

2.2 HDL Based Implementation Approaches of n-bit Vedic Multiplier

To obtain a comprehensive understanding of the VM implementations several significant classification parameters are carefully analyzed, including delay, area, and power. These parameters are crucial performance metrics utilized to evaluate the efficiency of various VM implementations.

- *Delay:* Delay is typically measured as the time taken by the signal to propagate through the longest path in the circuit, known as the critical path. This is crucial as it determines the maximum operating frequency of the circuit. Some tools such as Xilinx perform a Static Timing Analysis. This analysis calculates the delays through different paths and identifies the critical path. The timing report generated by this analysis includes the minimum clock period, maximum frequency, setup and hold times, and slack, which all help in understanding the delay characteristics of the design.

- *Area:* In HDLs, area is often represented in terms of the number of resources used on the FPGA. These resources typically include Lookup Tables (LUTs), Flip-Flops (FFs), DSP blocks, and BRAM (Block RAM). The tool generates a report detailing the utilization of these resources after synthesizing and implementing the design. This report provides a summary of the number of LUTs, FFs, DSPs, BRAMs, and other resources are used, which collectively give an idea of the area occupied on the FPGA.

- *Power:* Power estimation tools are provided in Xilinx such as XPower Analyzer (in ISE) and Power Report (in Vivado) to estimate the power consumption. These tools analyze the design post-implementation and consider factors such as

switching activity, resource utilization, and signal frequencies. The power consumption of the circuit is broken down into dynamic power (caused by switching activity) and static power (caused by leakage currents). The tools estimate both types of power by analyzing the design's activity and the technology-specific power models.

Hereafter, the tables 2.1 to 2.4 present a comprehensive literature overview of hardware VM implementations utilizing various HDL languages. They cover bit lengths 2-64 and showcase various research studies, emphasizing their significant contributions in the field of VM implementation.
Simulation tools also play an important part in design optimization, allowing designers to experiment with different components and topologies before integrating circuit blocks into a physical layout. Simulation technology can also be used during functional testing of a chip to compare actual behavior with expected behavior. Following the front-end design methodologies utilizing HDL, it is crucial to explore the back-end design approaches for multiplier architectures, specifically focusing on CMOS technology and QCA technology. Unlike front-end design, which primarily deals with the architectural and functional aspects of the circuits through HDL, back-end design is concerned with the physical realization of these architectures, ensuring they meet the required performance metrics such as area, delay, and power.

2.3 CMOS Based Implementation Approaches of n-bit Vedic Multiplier

In the context of CMOS technology, tools like Cadence Virtuoso, Tanner TSpice, and Synopsys' HSpice, offer robust environments such as ADE, S-Edit, and PrimeSim respectively to carry out detailed schematic capture, layout design, and post-layout verification, providing an in-depth analysis of the circuit's physical characteristics. The design flow involves creating a transistor-level schematic, followed by layout generation, parasitic extraction, and final performance simulations to ensure the circuit adheres to the desired specifications. In addition, discrete analyses such as Monte Carlo analysis [48], parameter sweeping, DC analysis, AC/noise analysis, transient analysis, and static timing analysis [49] are performed to ensure that the gate-level design meets the timing requirements for the correct design operations and contributes to design optimization. The DRC (design rule check) and LVS (layout vs. schematic)[50]

Table 2.1: A summary of n-bit VM based on HDL Technology. (*Citations as recorded on 13/05/2024)

Year	Ref.	HDL	Bit	Tool	Version	Delay (ns)	Power (mW)	Area	Explanation	Citations
2022	[27]	Verilog	2	Xilinx	-	6.3	81.53	-	The delay and power of the modified VM using the modified sum product algorithm is lesser than the conventional VM.	2
2022	[27]	Verilog	4	Xilinx	-	7.824	195.43	-	The proposed multiplier has a 42.51% decrease in power and a 49.12% reduction in delay when compared to the conventional VM.	2
2021	[28]	Verilog	4	Xilinx	Vivado	3.75	0.0463	37 CC	The 4-bit Urdhva multiplier uses 5.0% less area, 35.9% less delay, and 4.35% less power.	1
2019	[29]	VHDL	4	Xilinx	v13.4	8.27	3.147	131.08 μm^2	The redundant data detector in VM lowers the number of active logic gates resulting in 58.9% reduction in gate count of the multiplier.	18
2022	[30]	Verilog	8	Cadence NCSIM	90 nm	3.6	0.049	-	The 8-bit design employs an iterative CSA and displays minimum PDP and EDP of 176.475 fJ, and 0.635 e^{-21} Js, respectively.	0
2021	[28]	Verilog	8	Xilinx	Vivado	6.69	0.0318	140 CC	The 8-bit Urdhva multiplier achieves 26.3% less area, 70% lower delay, and 19% power savings compared to the array multiplier.	1
2019	[29]	VHDL	8	Xilinx	v13.4	21.29	15.031	624.33 μm^2	The redundant data detector lowers the number of active logic gates of the multiplier by upto 75%.	18

CC: Cell Count, LUT: LookUp Table

Table 2.2: A summary of n-bit VM based on HDL Technology (*Citations as recorded on 13/5/2024) continued

Year	Ref.	HDL	Bit	Tool	Version	Delay (ns)	Power (mW)	Area	Explanation	Citations
2014	[31]	Verilog	8	Xilinx	v9.1i	15.752	-	192 LUT	An 8-bit VM with Kogge-Stone integration is implemented and compared with Array and Booth multipliers for delay.	32
2013	[32]	Verilog	8	Xilinx	v14.5	28.27	-	176 LUT	The 8-bit VM is implemented and displayed on Spartan 3E kit.	121
2013	[33]	Verilog	8	Xilinx	v10.1	23.079	99	-	UT and Nikhilam 8-bit VM are compared with an array multiplier to assess area, power, and delay.	38
2012	[34]	Verilog	8	Xilinx	v9.2i	11.886	-	139 LUT	A high-speed 8-bit ALU using CSA structure outperforms partitioned CSA, Modified Booth Wallace, Karatsuba, Array, and Wallace VMs.	12
2019	[29]	VHDL	8	Xilinx	v13.4	20.92	14.373	598.51 μm^2	The PDP is lowered to 23.78% for the 8-bit multiplier due to the use of 3-1-1-2 compressor.	18
2018	[35]	Verilog	8	Xilinx	v14.3	27.65	-	167 LUT	The VM achieves 20% lower delay and 16% less area than the Booth Multiplier.	3
2018	[36]	Verilog	8	Cadence NCSIM	-	-	0.051	1850 CC	The use of an 8-bit MUX-based adder shows 41% and 14% reduction in power as compared to carry-select adder and RCA.	1
2018	[37]	Verilog	8	Cadence RTL Compiler	180 nm	7.578	0.5267	0.025 mm^2	Significant reduction in speed and power dissipation is observed for the 8-bit VM.	4

Table 2.3: A summary of n-bit VM based on HDL Technology (*Citations as recorded on 13/05/2024) continued

Year	Ref.	HDL	Bit	Tool	Version	Delay (ns)	Power (mW)	Area	Explanation	Citations
2023	[38]	Verilog	16	Xilinx	Vivado	-	25490	361 LUTs	16-bit VM designed using suppression technique adders shows 10% and 24% improvement in area and power as compared to those with RCA.	1
2022	[30]	Verilog	16	Cadence NCSIM	90nm	4.547	0.2	-	The 16-bit architecture built using iterative CSA displays minimum PDP, and EDP of 932.93 fJ, and 4.24 e^{-21} Js, respectively.	0
2021	[39]	System Verilog	16	ALDEC-HDL	120 nm	6.9	0.27	13759 LUT	A 16-bit Vedic ALU, built with VM as a core component, shows improved performance over conventional ALUs.	0
2019	[29]	VHDL	16	Xilinx	v13.4	40.41	66.507	2753.65 μm^2	The VM using 3-1-1-2 compressor demonstrate 35% reduction in latency as compared to the modified Booth multiplier.	18
2016	[40]	VHDL	16	Xilinx	v13.1	32	-	-	Compressor adders in VM designs yield speed improvements of 27%, 30.5%, and 13.6% over Array, Wallace tree, and Booth multipliers, respectively.	41
2013	[41]	HDL	16	Xilinx	v13.2	6.216	0.027	203 LUT	VM outperformed Booth multipliers on Spartan 3 (3s50pq208-5) FPGA in speed and power efficiency.	16
2009	[42]	VHDL	16	Xilinx	-	23.064	-	-	VM architecture with UT sutra performs better than Modified Booth Wallace multiplier in terms of combinational latency.	73

Table 2.4: A summary of n-bit VM based on HDL Technology (**Citations as recorded on 13/05/2024) continued*

Year	Ref.	HDL	Bit	Tool	Version	Delay (ns)	Power (mW)	Area	Explanation	Citations
2013	[43]	VHDL	16	Xilinx	v12.1i	43.084	-	697 LUT	The path delays of VM using RCA are found efficient in contrast to VM with CSA.	7
2016	[44]	Verilog	16	Xilinx	-	25.825	-	600 LUT	The VM using RCA, KSA, and CLA has been implemented and compared on the basis of computational path delay.	4
2022	[30]	Verilog	32	Cadence NCSIM	90nm	9.0385	2.4963	-	The 32-bit VM using an iterative CSA, shows minimum PDP, and EDP of 22.56 pJ, and 203.935 e^{-21} Js, respectively.	0
2019	[45]	HDL	32	Xilinx	v12.3	24.457	-	2206 LUT	This paper implements 3:2 compressors in VM blocks on Virtex5-XC5VLX110T, achieving lower latency and area than array and Wallace multipliers.	2
2016	[46]	Verilog	32	Cadence Digital Compiler	45 nm	0.95	-	-	KSA is used to implement the VM. To perform RTL to GDSII code, the synthesized netlists were fed into Cadence SOC Encounter. The effects of the delay were contrasted with various multipliers.	10
2013	[33]	Verilog	32	Xilinx	v10.1	90.747	315	-	This paper compares UT and Nikhilam multipliers with array multiplier, evaluating area, power, and delay.	38
2016	[47]	VHDL	64	Xilinx	v14.1	29.967	-	2289 LUT	The Virtex4XC4VLX25 is used to construct VM and the results are compared with array and booth multipliers.	3

test phase is often referred to as the "back end" of the VLSI design. To evaluate the efficiency of the VM implementations crucial performance metrics are carefully analyzed.

- *Technology:* CMOS technology implementations encompass a wide variety of implementation techniques, including: MOSFET, FinFET, gate diffusion input (GDI), reversible gates, compressors, Multiple Channel CMOS, pass transistor logic (PTL), etc. Understanding these diverse techniques allows for a clearer and deeper understanding of the technology used, highlighting its advantages and disadvantages in terms of area, delay, and power.

- *Node:* The technology node, also known as the process node or process technology, refers to a particular semiconductor manufacturing process and its associated design rules. Different nodes typically correspond to different generations of circuits and architectures. The process node generally relates to the transistor's gate length (L_g), historically considered the "minimum feature size". In general, a smaller technology node indicates a smaller feature size, resulting in smaller, faster, and more power-efficient transistors.

- *Delay:* The multiplier needs a certain amount of time to produce the desired output, which is indicated by the delay parameter. Various techniques and design optimizations are explored to minimize the delay, enabling faster multiplication operations. In CMOS circuits, propagation delay is calculated as the time interval between 50% input and 50% output.

- *Power Consumption:* The power parameter assesses the energy consumption of the Vedic multiplier during its operation. Power efficiency is a crucial aspect of modern computing systems, as it directly impacts factors such as battery life, heat dissipation, and overall system performance. Different techniques, including low-power circuit designs and voltage scaling, are employed to minimize power consumption.

- *Area Occupied:* The area parameter focuses on the physical size or footprint occupied by the VM implementation. It quantifies the amount of circuitry required for the multiplier and plays a vital role in determining the overall chip size and integration density. In CMOS circuits, the area can be measured using

transistor count, gate count or calculated in μm^2 through layout designs. To minimize the area footprint, techniques such as circuit layout optimizations and innovative architectures are employed.

In addition to the narrative description, tables 2.5 to 2.8 provide a systematic overview of research studies focusing on VM implementations using CMOS technology. These tables highlight key details for bit sizes 2-32, where each row represents a different study.

2.4 QCA Based Implementation Approaches of n-bit Vedic Multiplier

In QCA technology, *QCADesigner* serves as a widely used foundational tool to design and simulate QCA circuits, offering a user-friendly interface for creating and testing layouts with a focus on basic functionality and speed analysis. Building on this, *QCADesigner-E* provides enhanced capabilities, particularly in energy estimation and advanced simulation models, making it more suitable for evaluating the practical viability and energy efficiency of QCA designs. Complementing these tools, *QCAPro* specializes in power dissipation analysis, offering detailed insights into leakage and switching energy consumption and thermal effects, which are critical for designing low-power nanoscale circuits. Together, these tools form a comprehensive suite for the design, simulation, and analysis of QCA circuits, from the basic layout creation to detailed power and energy efficiency evaluation.
To obtain a comprehensive understanding of the QCA based VM implementations several significant classification parameters are carefully analyzed.

- *Delay:* It is calculated by multiplying the clock period by the number of clocking zones along its critical path. In QCA circuits, delays are measured in units of 1/4 of a clock cycle.
- *Area:* A smaller circuit area generally means lower power consumption and faster signal propagation.
  Cell Area: This metric is calculated by multiplying the cell count of the circuit by the area of an individual cell ($18 \times 18\ nm^2$).
  Total Area: In assessing the architecture, the total area refers to the overall

Table 2.5: A summary of n-bit VM based on CMOS Technology (**Citations as recorded on 13/05/2024*)

Year	Ref.	Technology	Bit	Tool	Node	Delay(ns)	Power(μW)	Area	Explanation	Citations
2023	[51]	Reversible	2	Cadence EDA	180 nm	7.809	81000	24 GC	The proposed 2-bit VM performs consistently across all three models, with Model 3 achieving the lowest logic implementation cost.	2
2023	[52]	FinFeT	2	Cadence Virtuoso	180 nm	1450	0.59	-	At a supply voltage of 0.6 V, the FinFET-based VM designs demonstrate 54.4%, 38.6% and 65.3% lower delay, power, and energy respectively	2
2020	[53]	CMOS	2	Cadence Virtuoso	90 nm	0.0821	40.5	43.13 μm^2	The VM design reduces delay and power consumption by using NAND gates for carry generation .	5
2018	[54]	CMOS	2	Tanner	130 nm	0.88	5.742	64 TC	The GDI-based VM exhibits $\approx$ 60% lower power and requires 43.75% fewer transistors than CMOS logic.	25
2023	[52]	FinFeT	4	Cadence Virtuoso	180 nm	36800	1.8		At a supply of 0.6 V, the FinFET-based VM designs exhibits 31.2% and 53% lower power and energy consumption compared to the CMOS design	2
2023	[55]	CMOS	4	-	45 nm	0.04365	96.686	794 μm^2	The VM built using 4:2 compressor shows 0.995% reduction in area and 9.63% reduction in power as compared to conventional approach	1

Table 2.6: A summary of 4-bit VM based on CMOS Technology.(*Citations as recorded on 13/05/2024) continued

Year	Ref.	Technology	Bit	Tool	Node	Delay(ns)	Power(μW)	Area	Explanation	Citations
2023	[51]	Reversible	4	Cadence EDA	180 nm	16.415	113580	177 GC	The VM shows least implementation cost due to reduction in garbage outputs.	2
2023	[56]	m-GDI	4	Cadence Virtuoso	90 nm	0.532	0.00134	-	The m-GDI based VM shows 45% PDP improvement post-layout	1
2023	[57]	Compressors	4	Cadence Virtuoso	45 nm	0.1428	1.404	-	The VM using compressor chains achievs 97% reduction in PDP. Results are validated with 200-run Monte Carlo simulations.	6
2022	[58]	CMOS	4	Cadence Virtuoso	45 nm	0.168	-	-	The VM show 37% increase in speed as compared to array multiplier.	1
2022	[59]	CMOS	4	Cadence Virtuoso	90 nm	175.4	68.5	504 TC	A 75% reduction in the PDP of the proposed VM is observed as compared to the conventional VM.	0
2020	[53]	CMOS	4	Tanner	90 nm	-	290.2	421.92 μm^2	The 4-bit VM layout design involves strategic placement and routing for area optimization.	5
2018	[54]	CMOS-GDI	4	Tanner	130 nm	0.9297	88.21	242 TC	The 4-bit VM employs RCAs consisting of an 18T GDI-based FA. Monte Carlo simulations confirm the immunity to process variations.	25

m-GDI: Modified Gate Diffusion Input, GC: Gate Count

Table 2.7: A summary of n-bit VM based on CMOS Technology.(*Citations as recorded on 13/05/2024) continued

Year	Ref.	Technology	Bit	Tool	Node	Delay(ns)	Power(μW)	Area	Explanation	Citations
2017	[60]	CMOS	4	Cadence Virtuoso	$45nm$	90.29	2.911	-	The VM with modified adder blocks with some FAs replaced by HAs show reduced power and delay.	3
2014	[61]	CMOS	4	Cadence Virtuoso	$180nm$	-	17.45	-	The VM uses a 14T adder based on CPL logic for low power and high node voltage swings.	5
2012	[62]	CMOS	4	Tanner	$16nm$	1.71	180	618 TC	4-bit VM is implemented using fundamental 2-bit VMs, CLA, and HA in the design.	53
2012	[63]	CMOS	4	BSIM4	$0.25\mu m$	3.07	-	2.64 μm^2	DSCH2 VLSI CAD is used to design 4-bit multipliers (Braun, CSA, and VM). Simulated results indicate that the proposed VM circuit outperforms others.	4
2023	[51]	Reversible	8	Cadence EDA	180 nm	29.596	196110	915 GC	The VM shows least implementation cost due to reduction in garbage outputs.	2
2023	[52]	FinFeT	8	Cadence Virtuoso	180 nm	53400	3.68	-	At 0.6 V, the FinFET-based VM design showcase a 55.8% reduction in PDP compared to CMOS design.	2
2023	[57]	Compressors	8	Cadence Virtuoso	45 nm	0.4552	9.083	2204.9 μm^2	The 8-bit VM using 3:2 compressors (1976T) achieves 31% lower PDP, validated by Monte Carlo analysis.	6

Table 2.8: A summary of n-bit VM based on CMOS Technology. (*Citations as recorded on 13/05/2024) continued

Year	Ref.	Technology	Bit	Tool	Node	Delay(ns)	Power(μW)	Area	Explanation	Citations
2020	[64]	CMOS-GDI	8	Cadence Virtuoso	-	5.3	4.428	736 TC	The VM using GDI logic is proved superior in contrast to CMOS logic.	0
2017	[65]	CMOS	8	Cadence Virtuoso	180 nm	-	559.1	-	The VM consumes 14.22% and 18.86% less power than array and Wallace multiplier, respectively.	3
2017	[66]	CMOS-mGDI	8	Cadence Virtuoso	180 nm	0.2	30100	748 TC	Simulated at 1.8V, the m-GDI-based multiplier shows reduced metrics compared to alternatives.	14
2017	[60]	CMOS	8	Cadence Virtuoso	45 nm	90.63	25.23	-	The VM using FA and HA is shows lower power and delay in contrast to VM using RCA/CSA/Hybrid adders.	3
2014	[67]	Mc-CMOS	8	Cadence Spice	130 nm	0.244	780.4	-	The UT-based Mc-CMOS VM shows 72.61% improvement in PDP than traditional Mc-CMOS VM.	29
2013	[68]	CMOS/PTL	8	Tanner	90 nm	-	0.148	-	The VM exhibits power efficiency ranging from 19.88% to 34.29% at 100MHz and 15.17% to 29.90% at 50MHz compared to array multiplier.	15
2023	[51]	Reversible	32	Cadence EDA	180 nm	96.291	691920	17184 GC	VM using model-3 demonstrates least implementation cost due to decreased number of garbage outputs.	2

Mc-CMOS: Multiple channel CMOS, TC: Transistor Count, PTL: Pass Transistor Logic

rectangular space required for the design's implementation. An effective design minimizes the total area.

Area Utilization Factor: The area utilization factor of a circuit is a measure of how efficiently the available space is being utilized. It is calculated as the ratio of cell area to total area, multiplied by 100. A higher percentage indicates a favorable design approach.

- *Quantum Cost:* When assessing the effectiveness of QCA designs, the cost parameter is very important. Cost_{AD} is known to be the most general cost parameter, which is derived by the product of the area (in units of μm^2) and the square of the latency (number of clock cycles) (Eq. 2.1) [69].

$$Cost_{AD} = Area * Latency^2 \tag{2.1}$$

For instance, the 2-bit squarer circuits introduced by Angshuman Khan et al. [70] demonstrated area-delay costs of 0.61 and 0.04, respectively. The proposed 2-bit circuits showcase approximately 10 times lower area-delay cost when compared to the recent design by Safoev et al. [71]. Therefore, optimizing the area and minimizing the latency are crucial factors in reducing the quantum cost and enhancing the effectiveness of the QCA circuit designs.

The *Figure of Merit (FoM)* is another key metric specifically tailored to contribute to the complexity and performance of QCA circuits [69]. This QCA-specific cost parameter is determined by considering several factors: the number of majority voter (MG) gates utilized in the design, the number of inverters (INV) employed, the number of operated clocks (CK), and the number of crossovers (CV) used in the QCA layouts (Eq 2.2):

$$FoM = (MV^a + INV + CV^b) * CK^c \tag{2.2}$$

where a, b, and c are exponential weightings assigned to the MG count, CV count, and delay, respectively. The standard values are typically considered as a = b = c = 2 [69]. As an illustration, Angshuman Khan et al. [70] proposed 2-bit Vedic squarer circuits in his study. The initial proposed 2-bit squarer design utilized 4 majority gates, 0 inverters, and 2 crossovers, resulting in a latency of 1.75. Consequently, the FoM can be determined as:

$$FoM = (4^2 + 0 + 2^2) * 1.75^2 = 61.25 \tag{2.3}$$

In contrast, for the second 2-bit squarer design , only 1 majority gate, 0 inverters, and 1 crossover were employed, yielding a reduced delay of 0.75. Hence, the FoM is calculated as:

$$FoM = (1^2 + 0 + 1^2) * 1.75^2 = 1.125 \tag{2.4}$$

The tables 2.9 to 2.11 presents a literature overview specifically focused on VM implementations using QCA technology analyzing articles for bit lengths 2-8. These tables provide insights into parameters such as cell count, latency, number of inverters, majority voter gates used, number of crossovers in the design, and quantum cost of the circuit.

2.5 Discussion

By comprehensively analyzing and classifying VM implementations based on these parameters, researchers and designers can gain insight into the strengths and weaknesses of various techniques. This knowledge aids in the selection of appropriate implementation approaches based on specific requirements and constraints, leading to improved performance and efficiency in the design and implementation of VM. Furthermore, the evolution timeline presented in Figure 2.3 showcases significant breakthrough research in the technological approaches used to implement VM. The

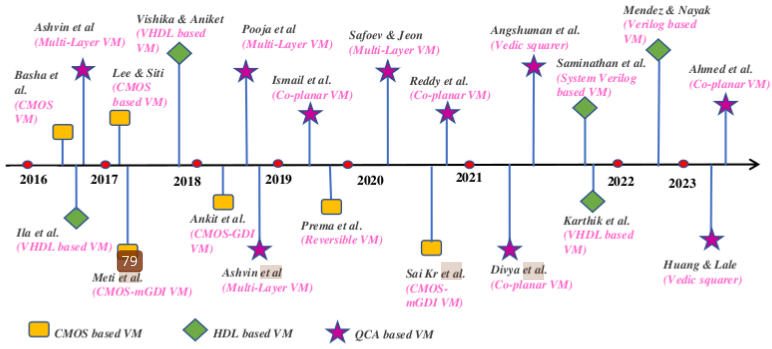


Figure 2.3: Timeline of the evolution of VM implementation approaches

Table 2.9: A summary of n-bit VM based on QCA Technology.(**Citations as recorded on 13/05/2024)*

Year	Ref.	Bit	Tool	Layer	Delay	CC	Area	MG	INV	CV	FoM	$Cost_{AD}$	Explanation	Citations
2023	[72]	2	QCAD, QCAD-E	Coplanar	0.5	107	0.12	-	-	-	-	0.03	Area enhancement of 48.45% is observed with TED of 3.62 $e-003$ eV.	0
2022	[73]	2	QCAD-E	Multilayer	1	115	0.13	8	0	5	89	0.13	An ultra-efficient VM with AED of 3.51 $e-003$ eV is presented.	3
2022	[70]	2	QCAD, QCAPro, QCAD-E	Coplanar	0.75	64	0.08	1	0	1	1.125	0.045	Area usage of design2 is $\approx$ 16% better than design1.	24
2021	[74]	2	QCAD	Coplanar	2	121	0.19	-	-	-	-	0.76	VM requires 2 QCA HAs(14 cells) and 4 AND gates.	7
2020	[71]	2	QCAD, QCAPro	Coplanar	2.25	194	0.17	7	0	7	496.12	0.86	The design uses a cell interaction-based HA, with detailed energy dissipation analyses.	44
2019	[75]	2	QCAD	Coplanar	4	77	0.17	2	1	0	80	2.72	Yavadunam-based Vedic squarer is designed with basic gates.	2

CC: Cell Count, TED: Total Energy Dissipation, AED: Average Energy Dissipation

Table 2.10: A summary of n-bit VM based on QCA Technology.(**Citations as recorded on 13/05/2024)*

Year	Ref.	Bit	Tool	Layer	Delay	CC	Area	MG	INV	CV	FoM	$Cost_{AD}$	Explanation	Citations
2019	[76]	2	QCAD	Coplanar	3.75	1683	8.42	6	3	2	604.6	118.4	VM is made using 4 MG and 2 HAs with considerable delay of 5 clock cycles.	2
2019	[77]	2	QCAD	Coplanar	8.25	726	2.66	13	9	7	15450.1	181.04	A rotated cell implementation of VM is done using the USE clocking scheme.	22
2018	[78]	2	QCAD	Multilayer	1	291	0.4	10	2	9	183	0.4	2-bit VM is implemented using HA.	13
2023	[72]	4	QCAD, QCAD-E	Coplanar	0.75	1108	1.72	-		-	-	0.9675	43.44% improvement in circuit size is observed with TED of 3.62 $e-003$ eV.	0
2022	[70]	4	QCAD, QCAPro, QCAD-E	Coplanar	1.5	545	0.6	11	16	23	1498.45	1.35	4-bit VM using E-shaped XOR and modified MG reduces cost.	36
2021	[74]	4	QCAD	Coplanar	1	1236	1.48	-	-	-	-	1.48	VM is implemented using a 49 cell RCA.	7
2020	[71]	4	QCAD	Multilayer	5.25	1726	1.74	33	0	26	48647.81	47.95	The 4-bit VM is built using multilayer RCA.	44

Table 2.11: A summary of n-bit VM based on QCA Technology.(**Citations as recorded on 13/05/2024)*

Year	Ref.	Bit	Tool	Layer	Delay	CC	Area	MG	INV	CV	FoM	$Cost_{AD}$	Explanation	Citations
2019	[75]	4	QCAD	Coplanar	8	211	0.43	-	-	-	-	-	The design requires a 2-bit squarer unit, a complement unit, and a left shifter.	2
2019	[77]	4	QCAD	Coplanar	4	15673	74.64	-	-	-	-	1194.24	A very bulky structure using USE scheme.	22
2018	[78]	4	QCAD	Multilayer	4	1959	2.39	-	-	-	-	38.24	4×4 VM is designed using 2×2 VM, HA and FAs.	13
2016	[79]	4	QCAD	Multilayer	4.25	1955	2.25	64	16	42	106135.25	40.64	The VM is built with HAs and FAs with each clock zone having 15 cells.	36
2023	[72]	8	QCAD, QCAD-E	Coplanar	1.75	7514	10.59	-	-	-	-	32.4625	60% area reductions are indicated with TED of 1.79 $e-001$ eV.	0
2020	[80]	8	QCAD	Coplanar	8.5	-	15.26	-	-	-	-	1102.535	Significant reductions in design metrics.	25
2018	[81]	8	QCAD	Multilayer	10.8	13533	18.4	313	83	517	42219719	2126.35	It has higher complexity but is faster due to fewer cells.	36

timeline demonstrates a paradigm shift from the conventional CMOS approach to the emerging and innovative QCA technology. Initially, early research efforts focused on VM implementations based on well-established and widely used CMOS technology, utilizing CMOS circuits and design methodologies to achieve VM functionality. However, as the timeline progresses, a notable shift towards the novel QCA technology becomes evident. QCA, being a promising alternative to CMOS, offers advantages such as higher speed, lower power consumption, and reduced area requirements. Researchers recognized the potential of QCA in enhancing VM performance and began exploring its application in this domain. Successful implementations of VM using QCA technology have demonstrated improved speed, reduced power consumption, and compact circuitry compared to CMOS-based counterparts. This paradigm shift towards QCA signifies the growing interest and recognition of its benefits over traditional CMOS approaches, indicating a pursuit of enhanced performance, efficiency, and the exploration of new technological frontiers in this field. Concerning Vedic multipliers, various studies have investigated different bit-lengths for multiplier implementations in CMOS technology, as evident from the tables 2.5 to 2.8. A design presented by Jie et al. [82] at 90 *nm* technology with a clock frequency of 1 MHz reported power dissipation of 2.29 x 10^{-2} mW. In comparison, Angshuman Khan et al. [70] developed a 2-bit Vedic multiplier using QCA technology, showcasing the effectiveness of this approach. Interestingly, they adopted a fixed frequency of 0.25 THz for their design, and power calculations were carried out using the QCADesigner-E tool. It's important to note that QCA Designer theoretically operates at a standard fixed frequency of 1 THz. Comparing the power dissipation between the CMOS-based Vedic multiplier [82] and the QCA-based implementations PD1 and PD2 by [70], an impressive reduction in power dissipation by 8545 and 16241 times approximately is showcased by the latter, highlighting the potential of QCA technology for energy-efficient digital circuitry. The appeal of QCA nanotechnology lies in its utilization of quantum dots, which possess unique properties that enable the construction of digital circuits with exceptional efficiency. As a result, implementing the Vedic multiplier using QCA technology facilitates high-speed execution of sub-multiplications and additions, accomplished with remarkable energy efficiency. These factors position QCA as a promising candidate for future digital circuit design, as it offers compelling advantages over traditional CMOS approaches. The bit-wise classification of research conducted in the field of Vedic multipliers is depicted in Figure 2.4. It is also evident

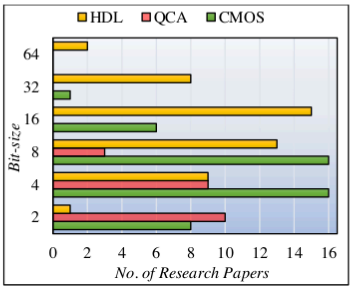


Figure 2.4: Bit-wise classification of the research in Vedic Multiplier

from the tables presented above that recent research has predominantly focused on investigating Vedic multiplier implementations using the innovative QCA technology. Particularly, the analysis has been concentrated on the lower-order bits to address verification and reliability aspects. As QCA technology continues to mature, it is anticipated that further research will be directed toward exploring QCA-based VM for higher-order bits, aiming to extend the application of this technology. In the context of the VM design process, behavioral modeling represents the initial step aimed at verifying the fundamental functionality of the VM. This modeling stage is technology-independent, facilitating a comprehensive spectrum of analysis and verification using HDL for Vedic multipliers with higher-order bits. Researchers leverage HDL languages to capitalize on the benefits of FPGA synthesis, which provides flexibility and thorough validation for VM designs encompassing larger bit lengths. This approach ensures a more accurate and efficient verification process, enabling researchers to explore complex VM designs with varying bit lengths, thus contributing to advancements in the field. In conclusion, the translation of the CMOS design process to QCA showcases the potential of QCA as a viable and efficient design method for nanoelectronics, ensuring continued progress in digital design and innovation.

2.6 Summary

This chapter presents a technology-centric categorization of Vedic multiplier implementations, primarily focusing on the software simulation analyses of various n-bit

Vedic multiplier architectures. A thorough comparison of commonly used performance key parameters, such as delay, power consumption, and area requirements, are used to identify the best technology for implementing a Vedic multiplier. The results show that using quantum-dot cellular automata (QCA) technology for the VM implementation speeds up sub-multiplication and addition and offers exceptional energy efficiency. These attributes position QCA as a promising candidate for future digital circuit design, offering compelling advantages over traditional CMOS approaches. Further, the detailed analysis has resulted in a bit-wise classification of the Vedic multiplier, offering a clear overview of the architectural relevance of the technology used for different bit sizes. It serves as a comprehensive resource for researchers and practitioners, paving the way for further research and development in this area.

Chapter 3

Design of energy efficient n-bit Vedic multiplier architecture with improved electrical-parameters

3.1 Introduction

The multiplication technique for two operands A and B, represented as $A = A_1A_0$ and $B = B_1B_0$, follows the Urdhva Tiryagbhyam (UT) sutra. Here, A_0 and B_0 are the least significant bits (LSBs), and A_1 and B_1 are the most significant bits (MSBs). The process begins with the vertical multiplication of the LSBs, which produces the

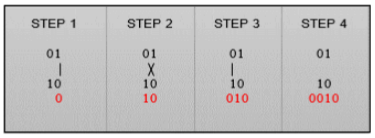


Figure 3.1: Illustrative depiction of 2-bit UT based Vedic multiplication

first bit of the product (Q_0). Next, crosswise multiplication of A_1B_0 and A_0B_1 is performed, and their sum generates the second bit of the product (Q_1). This is followed by the vertical multiplication of the MSBs ($A_1 \times B_1$) , with the resulting sum and carry combining to form the third and fourth bits of the final product (Q_2Q_3) [53], as depicted in Figure 3.1. Similarly, the multiplication process of a 4-bit

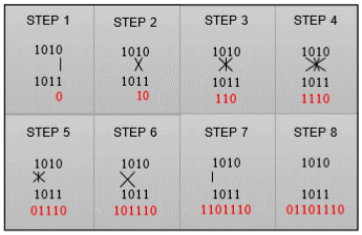


Figure 3.2: Illustrative depiction

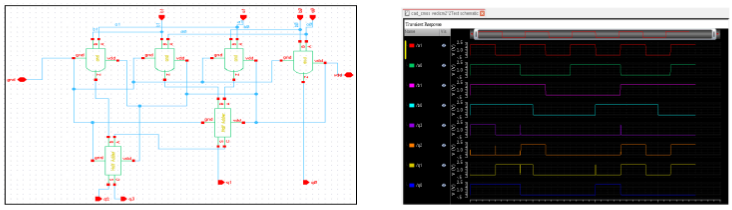
VM is illustrated in Figure 3.2 using binary operands 1010 (decimal 10) and 1011 (decimal 11). The algorithm involves generating partial products through vertical and crosswise multiplication steps, completing the process in seven steps to produce the final product 01101110 (decimal 110).

3.2 Schematic Representation and Simulation of n-bit Vedic Multipliers

This section proposes the schematic diagram of 2-bit, 4-bit and 8-bit Vedic multiplier architectures using the Urdhva Tiryagbhyam technique from Vedic mathematics in Cadence Virtuoso system design platform, version 6.1.5. The schematic designs are verified and simulated across all possible input combinations in the Analog Design Environment (ADEL) with a 90 nm CMOS technology library file at 1.8 V power supply using the Spectre simulation platform to ensure the reliability of the proposed multipliers.

3.2.1 2-bit VM employing UT Sutra

The schematic design of the 2-bit Vedic Multiplier (VM) is constructed using four AND gates and two half-adder modules, as illustrated in Figure 3.3(a). The corresponding simulation waveform is shown in Figure 3.3(b).

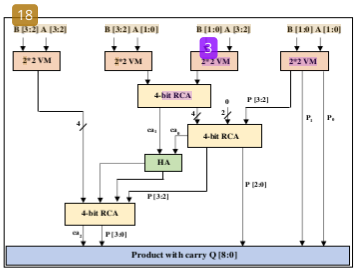


(a) Schematic design (b) Input-Output Waveform

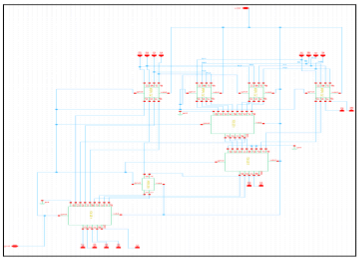
Figure 3.3: Standard CMOS Design of a 2-bit VM

3.2.2 4-bit VM employing UT Sutra

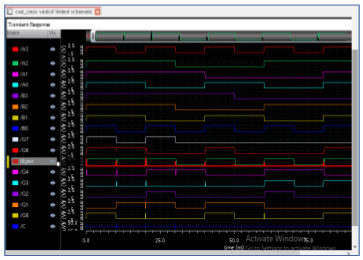
Conventional 4-bit Vedic Multiplier: The design employs four instances of the 2-bit Vedic Multiplier (VM) along with three 4-bit Ripple Carry Adders (RCAs) to compute the final carry and the 8-bit product output (Q_7 to Q_0), as illustrated in Figure 3.4(a). Figure 3.4(b) and 3.4(c) presents the schematic and the corresponding input-



(a) Block diagram



(b) Schematic design



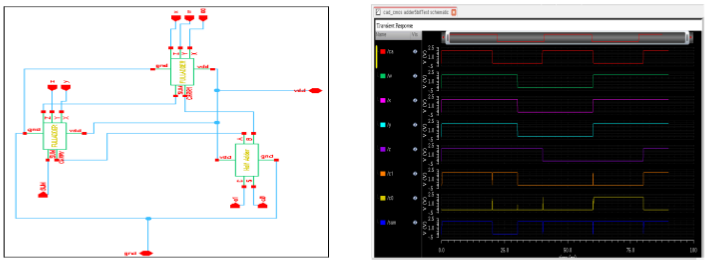
(c) Input output waveform of 4-bit VM

Figure 3.4: Standard CMOS 4-bit VM

output waveform of the conventional multiplier, where Q_7 to Q_0 represent the product bits, and C denotes the final carry output.

Proposed 4-bit Vedic Multiplier: In an effort to enhance the overall working of the multiplier, certain modifications are proposed in the initial building blocks of the architectural design. A special 5-bit adder is designed as shown in Figure 3.5(a) such that it takes 5 bits of binary data and generates a 3-bit output. The internal architecture consists of two full adders to generate the sum and a half adder to generate

the carry bits c_1 and c_0. Table 3.1 provides the truth table for the novel 5-bit special adder, listing all possible input-output combinations. It contains 32 unique 5-bit input combinations, each resulting in a corresponding three-bit output. However, Figure 3.5(b) illustrates the simulated waveforms for some of these combinations for validating the design.

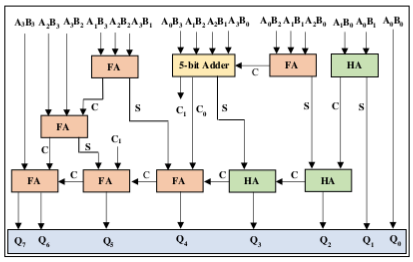


(a) Schematic design (b) Input output waveform

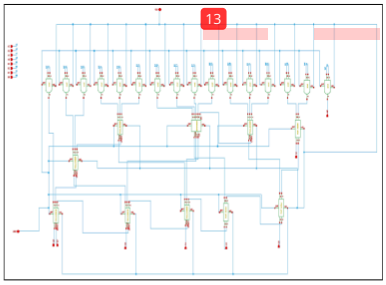
Figure 3.5: A novel 5-bit special adder

Table 3.1: Truth table of novel 5-Bit special adder

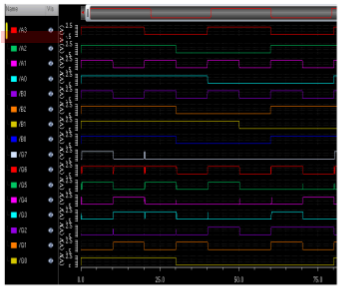
Inputs					Outputs			Inputs					Outputs		
ca	**w**	**x**	**y**	**z**	**c1**	**c0**	**sum**	**ca**	**w**	**x**	**y**	**z**	**c1**	**c0**	**sum**
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1	1	0	0	0	1	0	1	0
0	0	0	1	0	0	0	1	1	0	0	1	0	0	1	0
0	0	0	1	1	0	1	0	1	0	0	1	1	0	1	1
0	0	1	0	0	0	0	1	1	0	1	0	0	0	1	0
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
0	0	1	1	0	0	1	0	1	0	1	1	0	0	1	1
0	0	1	1	1	0	1	1	1	0	1	1	1	1	0	0
0	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0
0	1	0	0	1	0	1	0	1	1	0	0	1	0	1	1
0	1	0	1	0	0	1	0	1	1	0	1	0	0	1	1
0	1	0	1	1	0	1	1	1	1	0	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	1	0	0	0	1	1
0	1	1	0	1	0	1	1	1	1	1	0	1	1	0	0
0	1	1	1	0	0	1	1	1	1	1	1	0	1	0	0
0	1	1	1	1	1	0	0	1	1	1	1	1	1	0	1



(a) Block Diagram



(b) Schematic design



(c) Input output waveform

Figure 3.6: Proposed 4-bit VM using a special 5-bit adder

Table 3.2: Multiplication results of the 4×4 VM

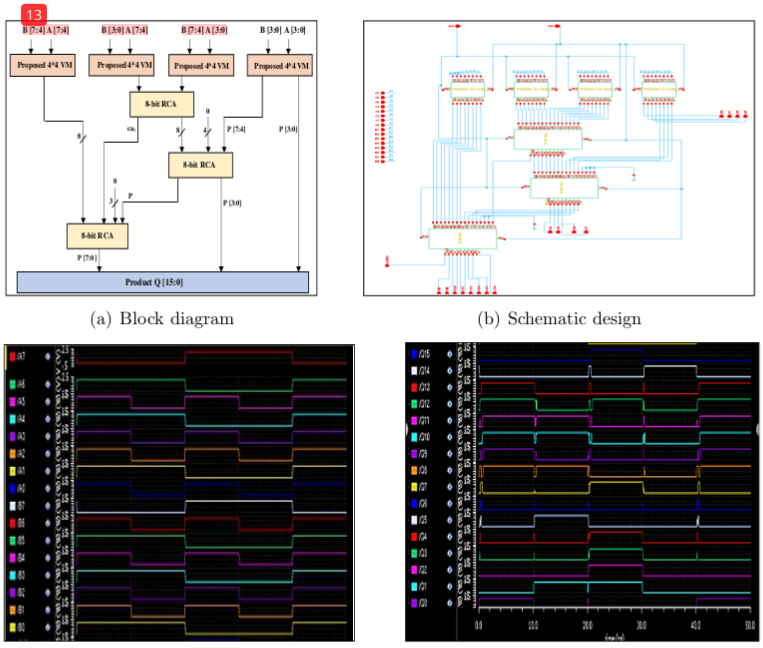
A		B		Q	
Decimal	**Binary**	**Decimal**	**Binary**	**Decimal**	**Binary**
15	1111	15	1111	225	11100001
13	1101	7	111	91	1011011
7	111	15	1111	105	1101001
1	1	2	10	2	10
10	1010	10	1010	100	1100100
8	1000	0	0	0	0
6	110	13	1101	78	1001110
4	100	5	101	20	10100

Building on this adder, an efficient multiplier architecture is developed, comprising sixteen AND gates, six full adders, and three half adders, as depicted in the block diagram in Figure 3.6(a). The CMOS schematic implementation of this architecture

is shown in Figure 3.6(b), while Figure 3.6(c) presents the simulated waveform of the novel design, with Q_7 to Q_0 representing the 8-bit product output. The proposed multiplier has been thoroughly tested for all possible input combinations while the waveform highlights only some results for validation as tabulated in Table 3.2.

3.2.3 8-bit VM employing UT Sutra

This section serves as an extension to the proposed 4-bit VM. An 8-bit VM is introduced using the modified 4-bit VM, supplemented by three 8-bit RCAs as shown in Figure 3.7(a). The schematic design of this 8-bit VM, illustrated in Figure 3.7(b) em-



(a) Block diagram

(b) Schematic design

(c) Input waveform

(d) Output waveform

Figure 3.7: The proposed 8× 8 Vedic multiplier

ploys the UT algorithm to ensure faster computation, making it ideal for low-power

and high-speed multiplication tasks. The simulated waveforms are illustrated in Figure 3.7(c) and 3.7(d), showing the 8-bit inputs, $A_7 - A_0$ and $B_7 - B_0$, and the resulting 16-bit output, $Q_{15} - Q_0$. In addition, these multiplication results for different input combinations have also been tabulated in Table 3.3.

Table 3.3: Multiplication results of proposed 8-bit Vedic Multiplier

Input A		**Input B**		**Output Q**	
Decimal	**Binary**	**Decimal**	**Binary**	**Decimal**	**Binary**
127	1111111	127	1111111	16129	0011111100000001
82	1010010	41	101001	3362	0000110100100010
173	10101101	214	11010110	37022	1001000010011110
128	10000000	128	10000000	16384	0100000000000000

3.3 Comprehensive Evaluation of N-bit Vedic Multipliers: Performance Metrics and Thermal Impact on Energy Consumption

In this section, detailed comparison is presented between the proposed multipliers and recent state-of-the-art. The thermal sensitivity of the multipliers is also investigated by analyzing the energy consumption in response to the temperature changes.
Power Delay Product (PDP) and Energy Delay Product (EDP) are key indicators of a design's energy efficiency (as indicated in Eq. 3.1).

$$PDP = Power \times Delay \quad EDP = PDP \times Delay \tag{3.1}$$

A lower PDP signifies better energy efficiency, as it reflects a circuit's ability to operate with minimal power consumption and delay. Similarly, a lower EDP demonstrates an optimal balance between energy efficiency and computational speed, highlighting a design's ability to manage the trade-off between power and delay. These attributes are particularly critical for energy-sensitive and high-speed applications, such as portable devices and energy-efficient processors. In this context, Table 3.4 and Table 3.5 provide valuable insights into the characteristics of the fundamental 2-bit VM module, along with quantitative data and metrics that enable a comprehensive comparison of the performance differences between the traditional and proposed VM modules. The overall improvement in design metrics for the proposed 4-bit and 8-bit VM circuit is

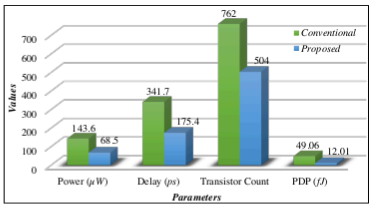
Table 3.4: Parametrical analysis of 2-bit VM

Parameters	**2-bit Vedic Multiplier**
Power	11.65 μW
Delay	0.11 ns
Energy	0.252 pJ
PDP	1.28 fJ
EDP	0.028 e^{-21} Js

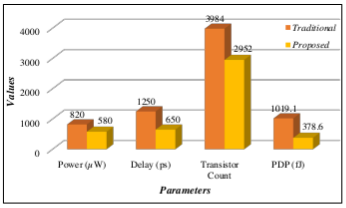
Table 3.5: Parametrical analysis of 4-bit and 8-bit VM

Parameters	**4-bit VM**		**8-bit VM**	
	Traditional	**Proposed**	**Traditional**	**Proposed**
No. of accepted trans steps	1568	1329	1799	1739
Total transient time (s)	24.32	13.95	39.521	27.41
Peak resident memory (MB)	57.5	50.5	135	110
Transistor Count	762	504	3984	2952
Delay (ns)	0.34	0.17	1.25	0.65
Power (mW)	0.143	0.0685	0.82	0.58
Energy (pJ)	13.10	9.30	33.49	27.38
PDP (fJ)	49.06	12.01	1019.1	378.6
EDP (e^{-21} Js)	0.016	0.002	1.27	0.25

also illustrated in Figure 3.8(a) and 3.8(b) respectively. Furthermore, the proposed multipliers have been bench-marked against several existing designs (Table 3.6) reported in the literature [53, 83, 60, 66], with respect to power consumption, delay, and PDP. The results clearly demonstrate that both the 4-bit and 8-bit VM implementations achieve superior performance across all evaluated metrics. The 4-bit and



(a) 4-bit VM



(b) 8-bit VM

Figure 3.8: Comparative analysis of traditional and proposed VM implementations

8-bit schematics are simulated for a transition time of 90 ns and 50 ns respectively.

Table 3.6: Comparative analysis of various multipliers with proposed implementation

Multiplier	**Technology**	**Power** (μW)	**Delay** (ns)	**PDP**
4-bit multipliers				
Wallace Tree using CMOS [83]	90 nm	2283	0.21	473.72 fJ
Wallace Tree using PTL [83]	90 nm	192	0.24	46.28 fJ
VM using Inverted gate [53]	90 nm	290.2	0.28	81.2 fJ
Proposed VM using 5-bit adder	90 nm	68.5	0.17	12.01 fJ
8-bit Vedic multipliers				
CMOS based VM [60]	45 nm	90.63	25.23	2.29 μJ
CMOS m-GDI based VM [66]	180 nm	30100	0.2	6.02 μJ
Proposed CMOS based VM	90 nm	582.46	0.65	377 fJ

The following inferences can be drawn:

1. There is significant reduction in propagation delay of the 4-bit and 8-bit proposed VM in comparison to the traditional designs. Specifically, the suggested 4-bit VM demonstrates a 39.29% improvement in delay when compared to the design reported by Patel et al. [53].
2. In contrast to the traditional design, the proposed 4-bit and 8-bit VM exhibit PDP improvements of 75.52% and 62.85% respectively.
3. The suggested 4- and 8-bit multipliers show remarkable reduction in EDP of 87.5% and 80.31% in contrast to the traditional approaches.
4. The 4- and 8- bit multipliers achieve substantial PDP reductions of 97.5% and 94% respectively when compared to the closest reported designs by Patel et al. [53] and Meti et al. [66].
5. The proposed 4-bit circuit consumes 29% less energy than the traditional multiplier over a 0-90 ns period, while the 8-bit Vedic multiplier achieves an 18% energy reduction over a 0-40 ns period.

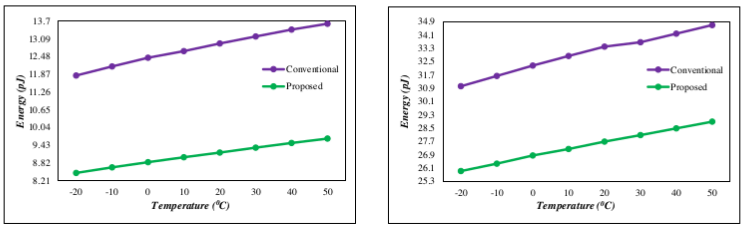
3.4 Impact of Temperature Variation on Energy Consumption

The thermal sensitivity of the proposed multipliers plays a critical role in evaluating how temperature variations influence the circuit's overall energy efficiency. Table

3.7 presents a detailed summary of the energy consumption analysis performed in this study. Additionally, Figure 3.9 illustrates the linear relationship between energy consumption and temperature for both 4-bit and 8-bit implementations. The analysis spans a temperature range from -20 to 50° *Celsius*, highlighting the impact of thermal fluctuations on energy performance.

Table 3.7: Impact of temperature variation on the energy consumption of 4-bit and 8-bit VM

Temperature (°C)	**Energy of 4-bit VM** (pJ)		**Energy of 8-bit VM** (pJ)	
	Traditional	**Proposed**	**Traditional**	**Proposed**
-20	11.83	8.48	31.01	25.91
-10	12.14	8.67	31.63	26.36
0	12.44	8.85	32.25	26.85
10	12.67	9.02	32.83	27.24
20	12.93	9.18	33.39	27.68
30	13.17	9.35	33.66	28.07
40	13.41	9.51	34.17	28.48
50	13.61	9.66	34.69	28.88
Average	12.78	9.09	32.95	27.43



(a) 4-bit VM (b) 8-bit VM

Figure 3.9: Temperature-dependent energy consumption of the conventional and proposed VM

The comparative analysis depicts a substantial decrease in energy consumption compared to the traditional design. Specifically, the average energy consumption of the proposed 4-bit VM is 28.8% lower than that of the traditional design, while the 8-bit VM architecture achieves a reduction of 16.7%. Moreover, the graph depicting the energy consumption of the traditional 8-bit VM shows fluctuations with increasing temperature, while the graph for the proposed 8-bit VM shows a linear and stable

trend. This remarkable reduction in energy consumption combined with the proposed designs' stability, highlights the proposed architecture's efficiency and effectiveness.

3.5 Summary

In this work, a comprehensive investigation into the design and performance optimization of Vedic multipliers based on the Urdhva Tiryagbhyam (UT) sutra, emphasizing their applicability in high-speed and low-power digital systems is presented. Two significant architectures were proposed: a 4-bit Vedic multiplier employing a novel 5-bit adder, and an 8-bit extended design constructed through modular reuse and efficient adder integration. The 4-bit and 8-bit designs achieved remarkable improvements in power consumption, delay, and power-delay product (PDP) when benchmarked against conventional multipliers, while also maintaining energy stability across a range of temperatures. These results affirm the architectural efficiency and thermal resilience of the proposed Vedic multiplier implementations. This work underscores the potential of Vedic arithmetic in reducing computational overhead and enabling parallelism, making it highly relevant for resource-constrained and performance-critical applications like digital signal processors, filtering units, and arithmetic logic components. Future research may focus on developing hybrid Vedic architectures for real-time embedded systems, investigating fault-tolerant implementations, and optimizing layout design for ASIC integration. Additionally, the integration of these multipliers into domain-specific architectures like AI accelerators and cryptographic units remains a promising direction.

Chapter 4

Realisation of Majority gate-based adder circuits using different wire schemes in Quantum Dot Cellular Automata technology

4.1 Introduction

Quantum-dot Cellular Automata (QCA) represents a highly promising nanotechnology with the potential to surpass traditional CMOS technology in terms of performance and scalability [84]. The QCA quantum dots are organized in a regular grid and are used to depict the binary digits 0 and 1. The state of a QCA circuit is ascertained by the alignment of the quantum dots, which can be manipulated using electrical or magnetic fields. QCA has several advantages over traditional silicon-based transistor technology. For example, QCA circuits can be much smaller and more energy efficient than their transistor counterparts. They have the potential to revolutionize computing and other fields by enabling the development of very small, more stable, and high-performance devices. Adder circuits are an integral part of digital circuits as they can be used to build devices that can perform complex mathematical calculations, process and analyze data, and perform a wide range of computational tasks. This chapter intends to present novel designs of adders and conduct a thorough evaluation of various attributes. QCADesigner 2.0.3 tool is utilized during the design stage and the two simulation engines: Bistable Approximation and Coherence Vector are used for the functional verification of the adders. The default parameters and initial conditions employed during simulation and performance analysis are summarized in Figure 4.1. A comprehensive performance evaluation is conducted based on these simulations with recent state-of-the-art adder architectures, encompassing various critical parameters such as complexity, total area requirement, quantum cost, and more to provide a well-rounded assessment of each proposed design. In addition, the proposed structures' energy dissipation is successfully evaluated through the QCADesigner-E [85] and QCAPro[86] tools.

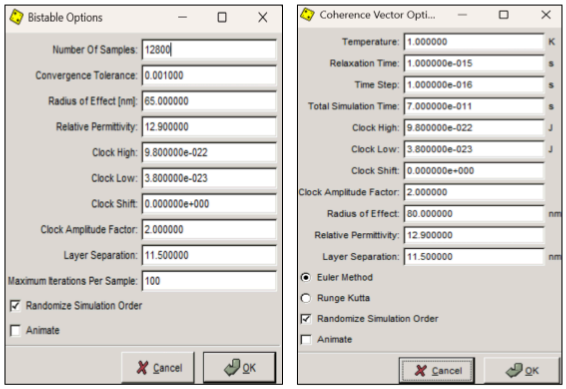


Figure 4.1: Types of simulation engines in QCA

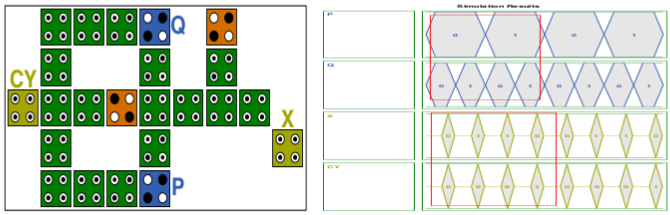
4.2 Efficient Co-Planar Adder Designs in Quantum Dot Cellular Automata

In this section, a novel layout for the Half Adder (HA) circuit is presented, followed by the implementation of a Full Adder (FA) circuit through strategic cell placement. Building on this, a 4-bit and 8-bit parallel adders are implemented using the proposed FA design. A key advantage of these designs is their implementation within a single layer, without relying on rotational (45°) cells or wire crossovers. These advancements offer improved circuit efficiency and streamlined layouts of the circuits.

Proposed Half Adder Circuit: Two binary variables, P and Q, can be added using a half adder circuit, generating two outputs: Sum (X) and Carry (CY), which can be computed as follows:

$$\text{Sum} = P \oplus Q \qquad \text{Carry} = P \cdot Q \tag{4.1}$$

A new QCA-based single-layer HA circuit is introduced, featuring several distinctive characteristics that set it apart. Notably, it eliminates the need for any crossovers by employing a single INV and an MG gate with a total of 23 cells in a single clock phase as demonstrated in Figure 4.2(a). The presented design achieves a latency



(a) QCA Implementation (b) Simulation waveform

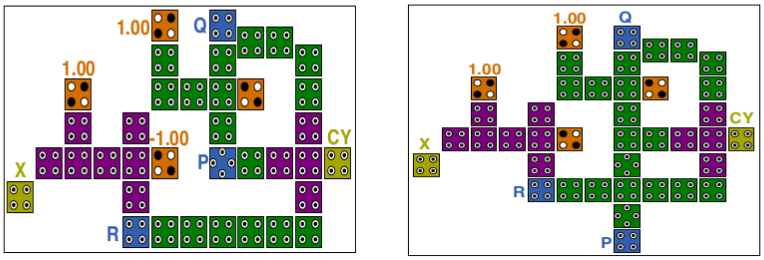
Figure 4.2: Proposed half adder cell design in QCA

of 0.25 clock zones, ensuring efficient operation. The architectural simplicity due to the absence of cross-wiring and low cell count of this design are the two significant benefits. The bi-stable approximation engine is used to display the truth table of HA as presented in Figure 4.2(b).

Full Adder: The arithmetic addition of three input bits is achieved through a combinational circuit called a 1-bit FA, which incorporates two significant bits, P and Q, along with a previous carry input, R. The FA produces two outputs: a sum X and a carry-out CY as:

$$Sum = P \oplus Q \oplus R \quad Carry - out = PQ + QR + PR \tag{4.2}$$

The schematic design, as illustrated in Figure 4.3(a), showcases a well-organized cell structure. Importantly, the proposed FA layout utilizes cell interaction and employs two XOR gates to generate X as well as a 3-input MG gate to produce CY. As depicted, this design avoids the usage of co-planar cross-wiring and solely relies on 90° cells arranged in a single layer. The effectiveness of the design is evident from its compactness, as it requires only 37 cells for the single-layer implementation. Additionally, the design has a latency of 0.5 clock cycles, indicating its efficiency in processing input signals. However, this arrangement lowers the transmission efficiency of the input signal P. Therefore, we also propose a scalable form of the full adder using rotated cell crossover as depicted in Figure 4.3(b). This design is composed of 40 cells with two clocking phases and an area of only 0.03 μm^2. The complete truth table has been thoroughly validated for accuracy using both bi-stable and coherence vector simulation engines, but the output results displayed in Figure 4.4 correspond to the results



(a) Proposed design (b) Scalable design

Figure 4.3: Proposed QCA-based full adder cell design

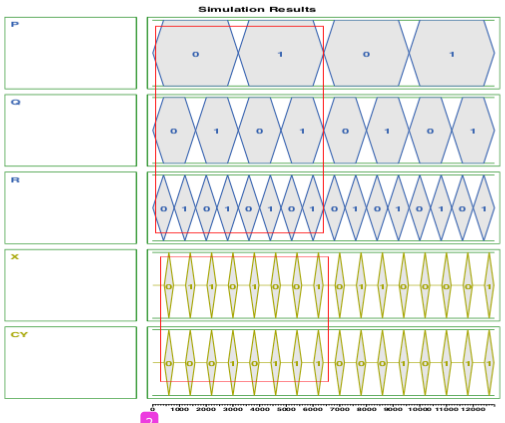


Figure 4.4: Verified truth table of proposed FA

obtained from the bi-stable approximation simulation engine.

n-bit Parallel Binary Adder: An n-bit parallel binary adder is used in digital circuits for n-bit addition where n FAs are cascaded in series. In this study, a 4-bit parallel binary adder is designed by utilizing 4 FAs, as illustrated in Figure 4.5. Consider the following representations of two 4-bit binary numbers, P and Q, represented as P = P3 P2 P1 P0 and Q = Q3 Q2 Q1 Q0, where R is the input carry to the first FA. The output denoted as X = CY X3 X2 X1 X0, consists of 5 bits. The

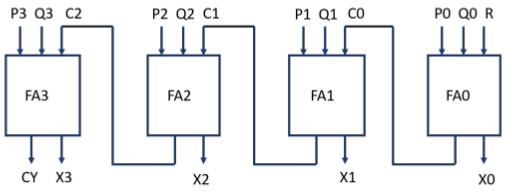


Figure 4.5: 4-bit parallel binary adder

adder in Figure 4.6 functions using a ripple carry, where the carry ripples from one stage to the next, commonly referred to as a ripple carry adder (RCA). The RCA

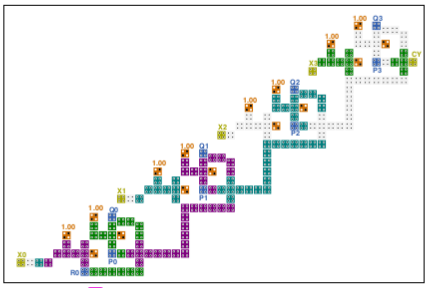
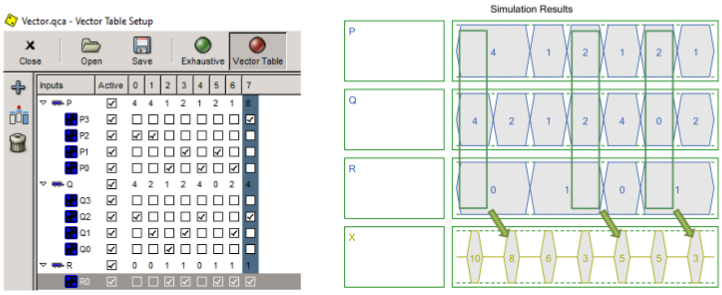


Figure 4.6: 4-bit parallel binary adder QCA layout

layout is implemented in a single layer to optimize the cost, as multi-layer designs tend to increase fabrication costs. This design achieves a minimum delay of 1 clock cycle while utilizing 174 cells over a 0.53 μm^2 area.

Because of the numerous entries in the test of the RCA, we evaluated some vector sets using the vector table as shown in Figure 4.7(a). The results can be verified from Figure 4.7(b) as the 4-bit parallel adder runs proficiently with a latency of 1 clock cycle. Furthermore, the study extends to 8-bit RCA, as depicted in Figure 4.8. The adder generates two outputs, X[7:0] and COUT, from three inputs, P[7:0], Q[7:0], and R0. The implementation employs 371 QCA cells and achieves a minimum latency of 2 clocks.



(a) Vector table setup (b) Simulation outputs

Figure 4.7: The simulation of the suggested 4-bit parallel adder

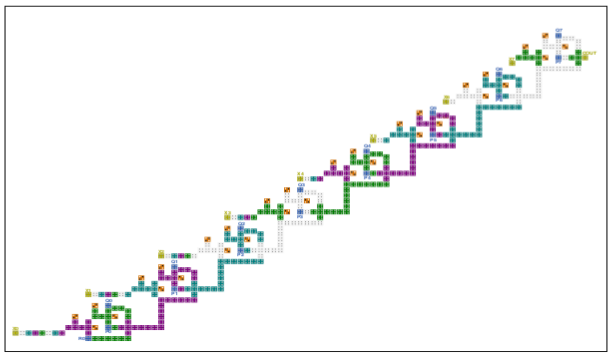


Figure 4.8: QCA layout of 8-bit parallel adder

4.2.1 Analyzing Metrics for Proposed QCA Adder Designs

To comprehensively assess the performance of QCA designs, various metrics are taken into consideration. This section analyses various performance attributes related to the proposed adder designs.

Complexity: The design complexity is quantified by the QCA cell count in the layout. Low complexity is desirable for an efficient QCA circuit. In the proposed layouts, HA, FA, and RCA have a complexity of 23, 37, and 174 respectively.

Area Optimization: To ensure a good design, it is desirable to minimize the cell area. The cell area is determined by multiplying the complexity of the circuit with the area of a single cell, assuming each small QCA cell has an area of 18×18 nm^2. The cell areas for the suggested HA, FA and RCA circuits are 0.007 μm^2, 0.011 μm^2, and 0.056 μm^2 respectively.
The rectangular space required to accommodate the circuit's architecture is referred to as the total area. For the proposed designs, the HA, FA, and RCA layouts need total areas of 0.014 μm^2, 0.027 μm^2, and 0.39 μm^2 respectively. The percentage of area used can be calculated by dividing the cell area by the total area and multiplying by 100. These estimates show that the proposed HA, FA, and RCA designs each occupy around 52.8%, 44.44%, and 14.44% of the total area, respectively.

Delay: A key parameter for evaluating a QCA circuit's performance is its delay. It is calculated by multiplying the clock period by the number of clocking zones along its critical path. In QCA circuits, delays are measured in units of 1/4 of a clock cycle. The delay of the suggested HA, FA, and 4-bit RCA layouts are 0.25,0.5 and 1.0 clock cycles respectively.

Cross Wiring: It is important to avoid wire crossing in QCA designs. The suggested layouts of the adder circuits successfully eliminate wire crossing, resulting in zero instances of any crossovers.

Layers: Multi-layer QCA layout designs are challenging and complex. Hence, single-layer designs are preferred. The proposed designs achieve significant advancements within a single layer, eliminating the requirement for rotational cells.

Cost Calculation: When assessing the effectiveness of QCA designs, the cost parameter is very important. Cost_{AD} is known to be the most general cost parameter, which is derived by the product of the area(in units of μm^2) and the square of the latency(number of clock cycles)(Eq. 4.3) [69].

$$Cost_{AD} = Area * Latency^2 \tag{4.3}$$

The equation demonstrates a direct relationship between the cost function, the area occupied, and the corresponding delay (in clock cycles) of the circuit. Therefore, optimizing the area and minimizing the latency are crucial factors in reducing the quantum cost and enhancing the effectiveness of the QCA circuit designs. The calculated Cost_{AD} of the suggested HA, FA, and 4-bit RCA is 0.001, 0.009, and 0.53 respectively.

The Figure of Merit (FoM) [69], is another key metric specifically tailored to contribute to the complexity and performance of QCA circuits. This QCA-specific cost parameter is determined by considering several factors: the number of MG utilized in the design, the number of INV employed, the number of operated clocks (CK), and the number of crossovers (CV) used in the QCA layouts (Eq. 4.4)

$$FoM = (MG^a + INV + CV^b) * CK^c \tag{4.4}$$

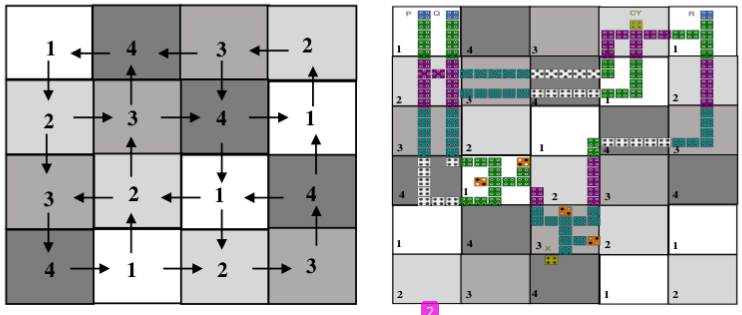
where a, b, and c are exponential weightings assigned to the MG count, CV count, and delay, respectively. The standard values are typically considered as a = b = c = 2 [69] [87]. It is important to note that the FoM of the proposed HA and FA circuits is 0.3125 and 2.75 respectively. Further, the energy-delay cost function is a different performance evaluation trade-off. It is calculated as (Eq.4.5),

$$Cost_{ED} = E^x * D^y \tag{4.5}$$

where D is the delay, E is the dissipated energy, x and y are experimental weights with standard values of 2 [69]. For instance, at 1.0 E_k tunneling level, the total energy dissipation of HA and FA is 34.7 meV and 64.1 meV, respectively. Hence, the present designs' energy-delay costs are 0.000075 and 0.001027 respectively.

4.2.2 Realistic Clocks

In order to ensure an efficient routing channel and a consistent structure, realistic clocking is crucial. While various clocking schemes have been suggested [88, 89], the USE clocking scheme [88] proves to be more efficient in terms of cell count, occupied area, and delay due to its regular and adaptable structure. According to the fundamental concept of the USE clocking scheme, clock zones with adjacent numbers are always placed close to one another, while clock zones with nonadjacent numbers are placed farther apart. Adhering to these constraints, a 4×4 matrix



(a) 4×4 USE matrix (b) proposed FA under USE clocking scheme

Figure 4.9: FA circuit using realistic USE clocking scheme

is depicted in Figure 4.9(a). Within this matrix, each numerical value represents a specific clock zone assigned to the corresponding square, and the arrows show the information flow between QCA cells situated in neighboring clock zones. Each clock zone, whether horizontal or vertical, in a given line of the system, follows a specific order that specifies the direction of information flow - to the right or left, up or down. As a result, each line has a predetermined direction, and adjacent lines are always oriented in the opposite direction [88]. Consequently, the USE clocking scheme is used to build the QCA layout of the proposed FA, as depicted in Figure 4.9(b). The layout consists of 137 cells, occupying an area of 0.18 μm^2, and yields an output after a delay of 1.75 clock cycles. The FA depicted using this technique is a more scalable and regular structure.

4.2.3 Performance Comparison and Discussions

Table 4.1 provides a comprehensive performance analysis, comparing the metrics of the suggested HA design with earlier research to highlight the advancements achieved by our design. Additionally, Figure 4.10 shows the percentage improvement made by the suggested HA design in contrast to the recent works. It is clear from the results presented in Figure 4.10, that the suggested design outperforms other designs in terms of area, latency, and thereby, area-delay cost. The previous designs have complexity in the range of 21–77, with cell area in the range of 0.02–0.08 μm^2 [90,

Table 4.1: Performance of proposed HA in comparison to existing designs

Circuits	Cell Count	Total Area(μm^2)	Crossover	Latency	Cost_{AD}
[90]	77	0.08	Multi-layer	1	0.08
[91]	65	-	Co-planar	1.25	-
[92]	62	0.08	NR	2	0.32
[93]	34	0.05	NR	0.75	0.028
[94]	44	0.05	NR	1	0.05
[95]	26	0.027	NR	0.5	0.0067
[96]	21	0.02	NR	0.5	0.005
Proposed	**23**	**0.014**	**NR**	**0.25**	**0.0008**

NR: Not Required

91, 92, 93, 94, 95, 96]. Although the design presented in [96] achieves a reduced cell count yet our design shows 50% and 84% improvement in terms of latency and area-delay cost. The FA design metrics are thoroughly compared in Table 4.2, and

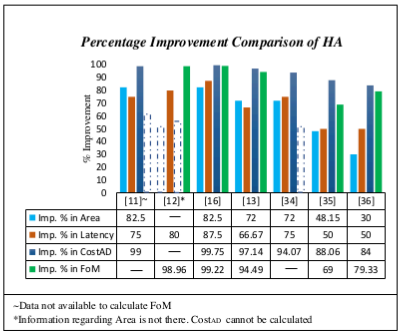


Figure 4.10: Proposed HA vs. previous works: percentage improvement in design Metrics

the FA design's percentage improvement over more recent works is graphically shown in Figure 4.11. Our proposed FA design saves 47% of cells while retaining a similar latency(0.5 clock cycles) as compared to the best-reported work [97]. The area-delay cost has also been significantly reduced by 64.3%. Moreover, the suggested adder performs better than the adder in [98], with improvements of 60% in area, 50% in latency, and consequently 90% in the area-delay cost. While having a similar number of cells to the design presented in [99], our concept achieves lower latency and a

79.6% reduction in area-delay cost, making it robust and cost-effective. Thus, the proposed design shows better performance on a number of critical parameters. The

Table 4.2: Performance of proposed FA in comparison to existing designs

Circuits	**Cell Count**	**Total Area**(μm^2)	**Crossover**	**Latency**	**Cost$_{AD}$**
[100]	228	0.28	NR	1.75	0.857
[101]	114	0.23	Co-planar	1.25	0.359
[102]	75	0.09	Co-planar	0.75	0.051
[103]	61	0.076	Co-planar	0.5	0.019
[84]	60	0.057	NR	1	0.057
[104]	56	0.047	Co-planar	1	0.047
[105]-a	52	0.038	NR	0.75	0.023
[105]-b	46	0.04	NR	0.75	0.023
[95]	47	0.04	Co-planar	0.75	0.023
[106]	44	0.043	NR	1.5	0.096
[107]-a	45	0.043	NR	0.75	0.024
[107]-b	43	0.037	NR	0.75	0.021
[108]	41	0.04	Co-planar	0.5	0.01
[109]	41	0.04	Co-planar	0.5	0.01
[99]	37	0.0245	Co-planar	1	0.0245
[110]	40	0.03	NR	1	0.03
[97]	70	0.056	Co-planar	0.5	0.014
[98]	46	0.05	Co-planar	1	0.05
[111]	35	0.02	Co-planar	2	0.08
[96]	37	0.04	NR	0.75	0.0225
Proposed	**37**	**0.02**	**NR**	**0.5**	**0.005**

NR: Not Required

performance of 4-bit RCA is comprehensively compared in Table 4.3, showcasing its strengths relative to recent designs. Furthermore, Figure 4.12 visually depicts the percentage improvement achieved by our suggested 4-bit RCA design when compared to the recent works. The RCA design put forth by [118] utilizes a minimum number of cells but suffers from a high latency of 5 clock cycles, resulting in a significantly high Cost$_{AD}$ of 4.5. Comparatively, our suggested adder design improves Cost$_{AD}$ by a remarkable 91.33%. In addition, the RCA design outperforms the latest reported RCA design [98] in terms of cell count, latency, and Cost$_{AD}$ by 32%, 33%, and 38.1% respectively. Improvements in design metrics are seen in the design suggested by [117]as it makes use of a multi-layer structure. posing challenges in fabrication. Since our design is built on a co-planar approach, the suggested RCA design is superior to recent designs.

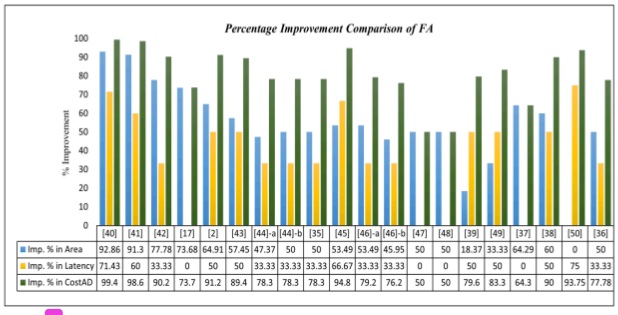


Figure 4.11: Proposed FA vs. previous works: percentage improvement in design Metrics

Table 4.3: Performance of proposed 4-bit RCA in comparison to existing designs

Circuits	Cell Count	Total Area(μm^2)	Crossover	Latency	Cost_{AD}
[112]	314	0.32	Multi-layer	1.5	0.72
[113]	295	0.3	Co-planar	1.5	0.675
[114]	269	0.37	Co-planar	3.5	4.53
[115]	237	0.24	Multi-layer	1.5	0.54
[108]	209	0.3	Co-planar	1.25	0.47
[116]	187	0.2	Co-planar	4	3.2
[117]	184	0.1	Multi-layer	2	0.4
[118]	70	0.18	Co-planar	5	4.5
[98]	256	0.42	Co-planar	1.5	0.63
Proposed	**174**	**0.39**	**NR**	**1**	**0.39**

NR: Not Required

4.2.4 Energy Dissipation Analysis: Assessing Power Consumption

One of the most crucial factors in determining the effectiveness and performance of the QCA circuit is energy dissipation. The analysis is performed using the QCADesigner-E [85] and QCAPro [86] softwares.

Energy calculation using QCADesigner-E: Each QCA cell is taken into account as an energy "bath" by the QCADesigner-E tool throughout each clock cycle. [85]. During each clock cycle, the QCA cells generate an energy "bath" as they sep-

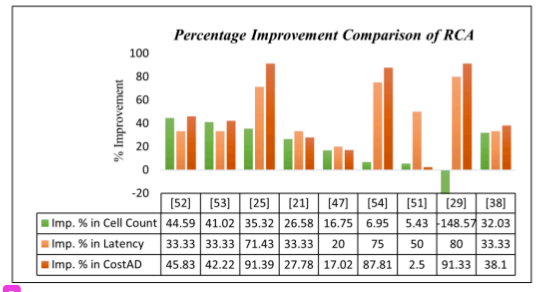


Figure 4.12: Proposed RCA vs. previous works: percentage improvement in design Metrics

arate, resulting in the total energy transferred to the QCA "bath" represented as E_{Bath}. Hence, the sum of all E_{Bath} energies represents the total energy dissipation. The energy calculation may have an error, denoted as E_{RR}, which can be negative, indicating energy transfer from environmental energy.

Table 4.4: Energy analysis of the proposed designs using QCADesigner-E

Energy Dissipation	**Proposed Adder Designs**		
	HA	**FA**	**4-bit RCA**
AED (eV)	8.88e-004	1.83e-003	5.27e-003
TED (eV)	9.77e-004	2.01e-002	5.8e-002

For the proposed circuits, 500,000 samples are used in the "coherence vector with energy" simulation engine to calculate the energy dissipation. The HA shows a 9.77e-004 eV total energy dissipation (TED), with a negligible error of -9.43e-004 eV. With a small error of -8.57e-005 eV, HA's average energy dissipation (AED) per cycle is 8.88e-004 eV. For the FA design, the TED amounts to 1.83e-003 eV, with a small error of -1.84e-004 eV. The AED per cycle for the FA is 2.01e-002 eV, with a small error of -2.02e-003 eV. Furthermore, the 4-bit RCA design showcases a TED of 5.27e-003 eV, with a negligible error of -4.76e-004 eV. The AED per cycle for the 4-bit RCA stands at 5.8e-002 eV, with a small error of -5.24e-003 eV. A summary of the energy dissipation results obtained using QCADesigner-E is also presented in Table 4.4.

Energy calculation using QCAPro: The QCA Pro tool [86] is a probabilistic model-

ing tool that utilizes fast approximation to estimate and analyze polarization error and non-adiabatic switching power loss. The power dissipation maps displaying the thermal hotspots for the suggested HA and FA layouts are shown in Figure 4.13 and Figure 4.14, respectively. These maps illustrate the power dissipation for different tunneling energies, specifically at $0.5E_k$, $1.0E_k$, and $1.5E_k$ at a fixed temperature of 2K presuming all QCA cells have constant power consumption. Comprehen-

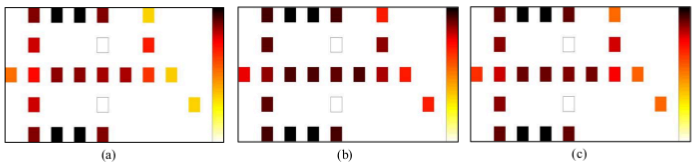


Figure 4.13: Thermal distribution of the FA circuit at $2K$ with tunneling energies: (a) $E_k = 0.5$, (b) $E_k = 1.0$ and (c) $E_k = 1.5$

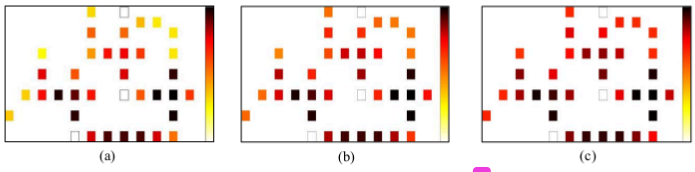


Figure 4.14: Thermal distribution of the FA circuit at $2K$ with tunneling energies: (a) $E_k = 0.5$, (b) $E_k = 1.0$, and (c) $E_k = 1.5$

Table 4.5: Evaluation of energy dissipation for HA designs under varying tunneling energy conditions

HA Circuit	**Leakage ED (meV)**			**Switching ED (meV)**		
	0.5 E_k	**1 E_k**	**1.5 E_k**	**0.5 E_k**	**1 E_k**	**1.5 E_k**
[119]	17.86	55.56	100.56	97.36	84.65	72.06
[91]	35.47	98.54	168.28	94.9	79.07	65.62
[120]	13.81	42.29	75.56	67.73	58.38	49.43
[121]	12.21	37.07	65.81	54.02	46.55	39.51
[95]	8.16	24.08	42.3	29.26	25.0	21.06
Proposed	**5.35**	**15.5**	**26.1**	**21.02**	**19.2**	**16.2**

sive energy dissipation data for the designed HA circuits, including a comparison of

Table 4.6: Evaluation of total energy dissipation and cost efficiency of the HA Designs across various tunneling energy levels

HA Circuit	**Total energy dissipation (meV)**			**Cost_{ED}**		
	0.5 E_k	**1 E_k**	**1.5 E_k**	**0.5 E_k**	**1 E_k**	**1.5 E_k**
[119]	115.22	140.21	172.62	NA	NA	NA
[91]	130.37	177.61	233.9	0.0265	0.0493	0.0854
[120]	81.54	100.67	124.99	0.0016	0.0025	0.0039
[121]	66.23	83.62	105.32	NA	NA	NA
[95]	37.42	49.08	63.36	0.00035	0.0006	0.001
Proposed	**26.37**	**34.7**	**42.3**	**0.00004**	**0.00007**	**0.0001**

NA: Data Not Available, Cost_{ED}: $(TED)^2 \times D^2$

Table 4.7: Evaluation of energy dissipation for FA designs under varying tunneling energy conditions

FA Circuit	**Leakage ED (meV)**			**Switching ED (meV)**		
	0.5 E_k	**1 E_k**	**1.5 E_k**	**0.5 E_k**	**1 E_k**	**1.5 E_k**
[91]	81.73	229.58	394.42	154.39	129.06	107.19
[122]	26.52	81.39	147.1	159.02	140.4	121.8
[119]	31.46	96.51	171.64	158.97	135.54	114.32
[123]	16.43	51.09	92.6	105.94	92.68	79.61
[95]	13.31	41.51	74.74	76.8	66	55.8
[124]	14.05	39.32	68.02	50.61	44.67	38.95
[125]	21.38	62.38	106.89	80.92	67.68	57.9
[103]	29.19	84.83	148.5	127.94	108.82	91.46
[126]	16.93	51.11	91.37	104.91	92.41	80.36
[106]	17.3	45.89	76.92	41.11	34.33	28.86
[84]	15.37	44.87	76.92	61.87	56.03	51.61
[104]	14.95	47.9	87.32	92.15	80.63	69.3
[127]	11.22	32.95	58.43	64.03	56.66	49.46
[96]	15.48	43.11	75.92	42.91	36.72	29.65
[128]	13.96	37.77	63.88	29.55	24.65	20.4
[107]-a	13.91	40.87	72.13	55.13	48.1	41.32
[107]-b	14.15	43.37	77.91	56.98	46.54	42.47
[129]	11.12	32.92	58.37	49.1	42.82	36.62
[110]	13.57	38.79	67.14	51.23	42.84	35.52
[130]	9.57	27.97	49.3	51.4	45.08	39.07
[97]	17.79	56.04	103.48	151.88	136.93	120.98
Proposed	**9.37**	**27.75**	**49.5**	**42.24**	**36.26**	**28.88**

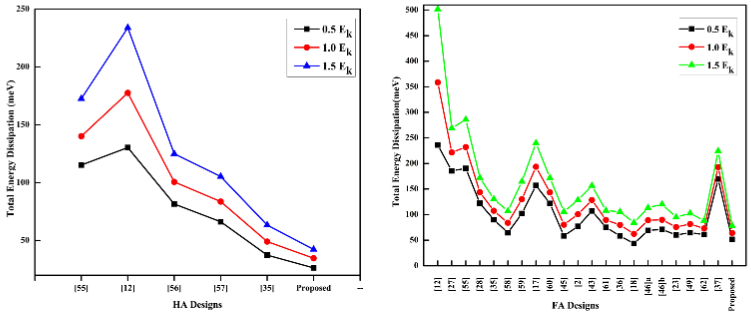
the energy-to-delay cost ($Cost_{ED}$) with previous designs, can be found in tables 4.5 and 4.6. Similarly, for the FA circuits, tables 4.7 and 4.8 are presented for the

Table 4.8: Total energy dissipation and cost analysis of proposed FA design versus previous designs at three tunneling energy levels

FA Circuit	Total energy dissipation (meV)			Cost_{ED}		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
[91]	236.12	358.64	501.61	0.2822	0.6511	0.1273
[122]	185.5	221.7	269	0.0537	0.0767	0.113
[119]	190.43	232.05	285.96	NA	NA	NA
[123]	122.37	143.77	172.21	0.0149	0.0206	0.0296
[95]	90.11	107.51	130.54	0.00456	0.0065	0.0095
[124]	64.66	83.99	106.97	0.00418	0.00705	0.0114
[125]	102.18	130.05	164.79	NA	NA	NA
[103]	157.13	193.65	239.97	0.0061	0.00937	0.0143
[126]	121.84	143.52	171.73	0.0148	0.0205	0.0294
[106]	58.41	80.22	105.78	0.00767	0.0144	0.0252
[84]	77.24	100.9	128.53	0.0059	0.0101	0.0165
[104]	107.1	128.53	156.62	0.0114	0.0165	0.0245
[127]	75.25	89.61	107.89	0.0056	0.008	0.0116
[96]	58.39	79.83	105.57	0.00191	0.00358	0.00629
[128]	43.51	62.42	84.28	0.00106	0.0021	0.00399
[107]-a	69.04	88.97	113.45	0.0026	0.00445	0.00723
[107]-b	71.13	89.91	120.38	0.00284	0.00454	0.00815
[129]	60.22	75.74	94.99	0.0009	0.00143	0.0022
[110]	64.8	81.6	102.66	0.0042	0.0066	0.011
[130]	61.04	73.05	88.37	0.0009	0.00133	0.00195
[97]	169.67	192.97	224.46	0.0072	0.0093	0.0125
Proposed	**51.61**	**64.1**	**78.38**	**0.0006**	**0.00102**	**0.00153**

NA: Data Not Available, Cost_{ED}: $(TED)^2 \times D^2$

corresponding data. The suggested HA design demonstrates much-improved energy efficiency when compared to various reported designs [119, 91, 120, 121, 95] at all three tunneling energy levels, as seen in Figure 4.15(a). Specifically, the suggested HA shows energy reductions of 29.5%, 29.3%, and 33.2% at 0.5 E_k, 1 E_k, and 1.5 E_k, respectively in comparison to the closest published design [95]. Furthermore, in the context of energy to delay cost $Cost_{ED}$, the proposed design outperforms all existing solutions, boasting substantial improvements compared to the recent design [95]. Specifically, it achieves an impressive 88.6% enhancement at 0.5 E_k, an 87.5% improvement at 1 E_k, and a remarkable 90% increase at 1.5 E_k. Further, in Figure 4.15(b), a comprehensive comparison of total energy dissipation in the proposed FA circuit with several existing designs ([84, 127, 96, 128, 129, 107, 130, 97]) is presented. Remarkably, the proposed FA design exhibits substantial energy reductions compared



(a) HA (b) FA

Figure 4.15: Comparison of total energy dissipation in proposed adder circuits and previous works at three tunneling energy levels

to the closest reported design [97], amounting to 69.5%, 66.7%, and 65% at 0.5 E_k, 1 E_k, and 1.5 E_k, respectively. The consistent improvement across varying tunneling energy levels further reinforces the potential of the proposed FA in achieving efficient and sustainable computational processes. Particularly, this improvement can be attributed to the integration of low complexity and optimized cell arrangements without the use of any crossover in our designs, making them highly viable for next-generation nanoelectronic applications.

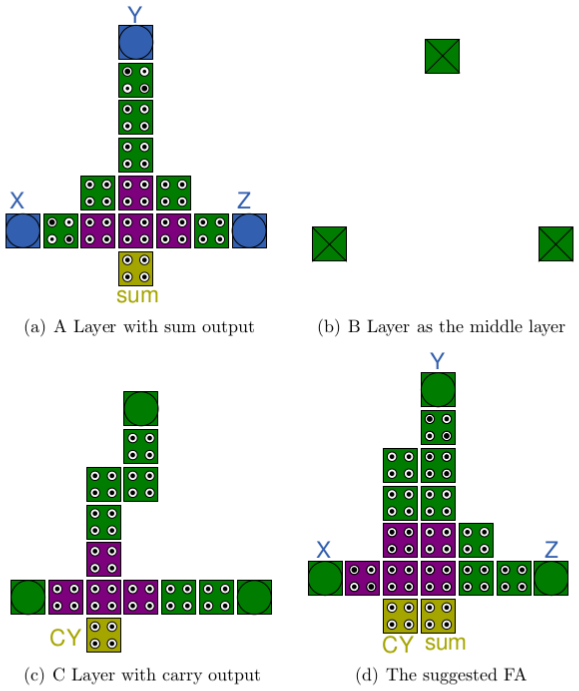
4.3 Efficient Multilayer Quantum-Dot Adder Optimization and Analysis for Future Circuits

The fundamental algebraic operation of addition is the foundation for many different algorithms, including elliptic-curve-cryptography, key-exchange algorithms, etc. However, due to the architectural simplicity of RCA, it is most suitable for use in general-purpose computers. This section presents the design of efficient multi-layer n-bit ripple carry adder (RCA) circuits, built using full adder (FA) units. The outputs are generated across distinct layers and verified using the QCADesigner-Ev2.2 tool, utilizing bi-stable and coherence vector energy setups with Euler and Runge-Kutta methods. The proposed designs are further evaluated for key performance metrics at three different scale factors (1, 0.8889, and 0.7778), corresponding to cell sizes of

$18 \times 18\ nm$, $16 \times 16\ nm$, and $14 \times 14\ nm$, respectively. Additionally, the impact of temperature on the average output polarization of the FA is analyzed. A detailed energy dissipation analysis for the proposed adder design is also provided.

4.3.1 Implementation of n-bit RCA

The proposed n-bit RCA design incorporates a basic module of a one-bit ML-FA, as suggested by [131]. The FA is noteworthy for its efficient use of only 32 standard QCA cells in a three-layered architecture (as illustrated in Figure 4.16(d)), without any use of rotational cells. Figure 4.17 displays the simulated results for the ML-FA in



(a) A Layer with sum output (b) B Layer as the middle layer

(c) C Layer with carry output (d) The suggested FA

Figure 4.16: The layout of the designed FA

the coherence vector (CV) simulation engine within QCADesigner-E. The latency of

the design is noted to be 0.5 CC. The primary cell layer A, incorporates three inputs

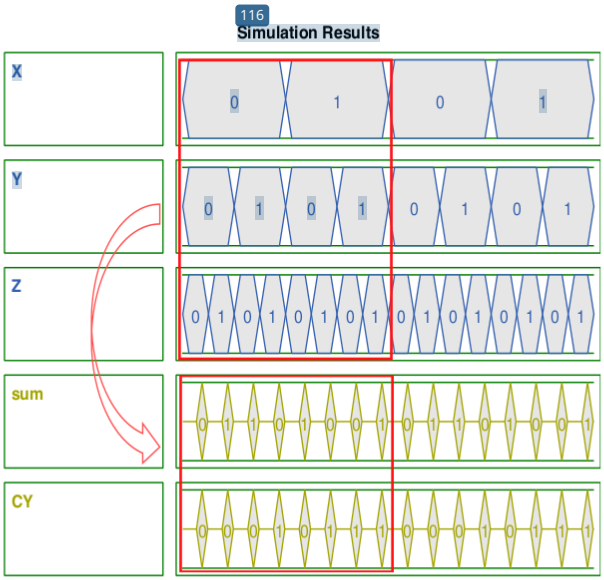
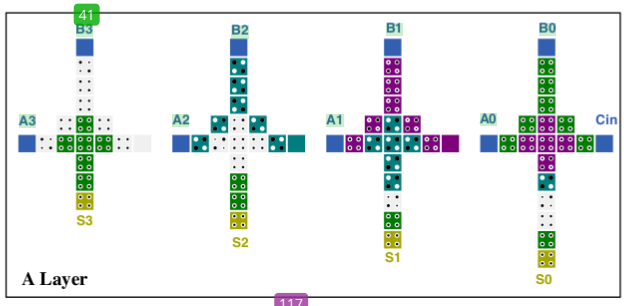


Figure 4.17: Simulated waveform of ML-FA design

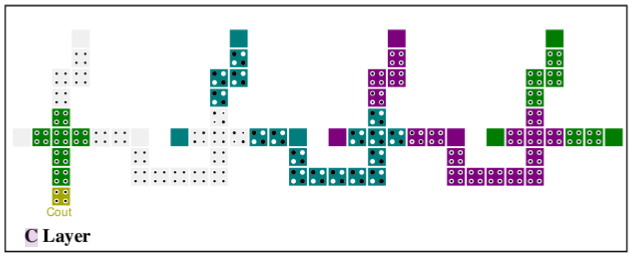
(X, Y, and Z) into a 3-input XOR gate, generating the output sum. The B layer, connecting the A and C layers, comprises three crossover cells. The C layer utilizes a 3-input majority voter (MG) gate for the carry output. Notably, the outputs (sum and CY) are generated in distinct layers and are not confined within a closed ring of cells. This architectural choice facilitates smooth scaling in larger circuit structures, contributing to the design's adaptability and scalability. The circuit occupies an area of 0.03 μm^2 and produces output with a latency of only 0.5 CC. Leveraging this scalability advantage, we present n-bit (n=4,8,16) RCA designs featuring n-cascaded-FAs, facilitating smooth carry transfer between stages. An n-bit RCA circuit includes inputs A[n-1 : 0], C_{in}, B[n-1 : 0], and outputs carry and sum [n-1 : 0]. Sum bits are generated in A layer, and the final carry is produced in C layer, as shown in Figure 4.18(a) and 4.18(c) respectively. Adhering to the design guidelines of maintaining a minimum of two cells in an individual clock [132], ensures efficient implementation



(a) A layer



(b) B layer



(c) C layer

Figure 4.18: The three-layered QCA implementation of the proposed 4-bit ML-RCA and superior performance in metrics like circuit area, number of cells, latency, and area-delay cost.

To ensure the functional correctness of the proposed 4-bit RCA design across a wide range of input scenarios, verification and testing for all possible input combinations have been performed. However, a well-defined vector table has been established

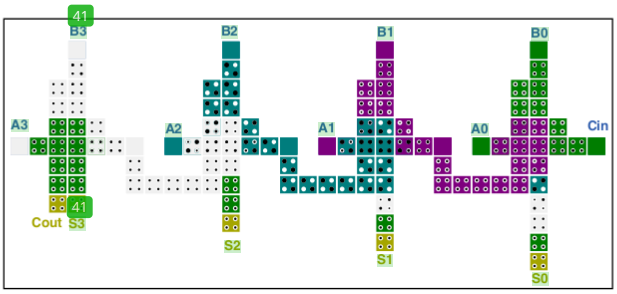


Figure 4.19: Cell Arrangement of suggested 4-bit-RCA design

Table 4.9: Vector table setup for 4-bit RCA

Bus	**Inputs**	**0**	**1**	**2**	**3**	**4**
A	A_3	1	0	1	0	1
	A_2	0	1	0	0	0
	A_1	0	0	0	1	0
	A_0	0	1	0	0	1
B	B_3	0	0	0	1	0
	B_2	1	1	0	0	0
	B_1	1	0	0	0	0
	B_0	0	1	0	1	1
C_{in}	C_{in}	0	1	1	0	1

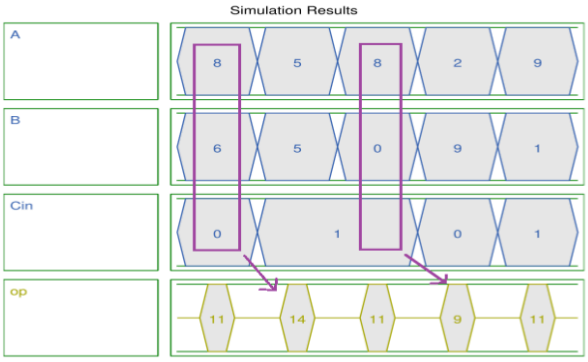
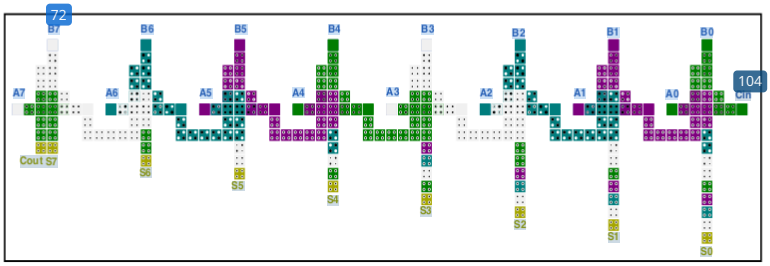
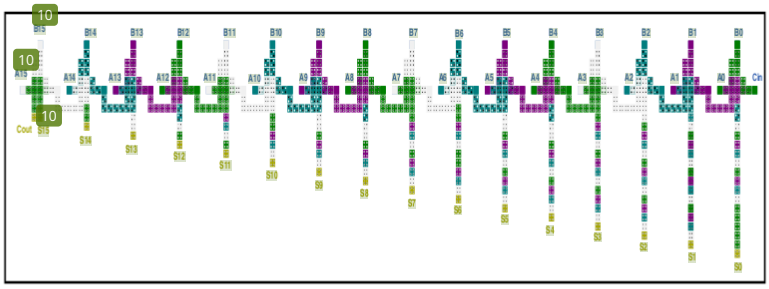


Figure 4.20: Simulation waveform of 4-bit-RCA



(a) 8-bit ML-RCA



(b) 16-bit ML-RCA

Figure 4.21: Cell arrangement of three layered n-bit QCA-RCA design

defining some of the input vectors, as depicted in Table 4.9. The outputs for the 4-bit RCA design simulated using the CV engine are presented in Figure 4.20. One notable advantage of the design is its low latency, with the sum of the adder being calculated after only 4 clock phases, resulting in a latency of one CC.

- *4-bit RCA Implementation:* This implementation as illustrated in Figure 4.19 utilizes 160 cells, occupying an area of 0.1 μm^2, and exhibiting a latency of 1 CC.
- *8-bit RCA Implementation:* As seen in Figure 4.21(a), a total of 342 cells are used for the implementation which occupies an effective area of 0.39 μm^2 and exhibits a latency of 2 CC.

- *16-bit RCA Implementation:* The implementation, shown in Figure 4.21(b), utilizes 768 cells in an area of 1.06 μm^2 with a latency of 4 CC.

4.3.2 QCA Cell-Size Scaling in QCADesigner-E

The size of the QCA cells can be scaled down using the QCADesigner-E tool. The scale factor (SF) for a QCA cell design can be calculated using the following mathematical formula [133] :

$$SF = \frac{New\ cell\ size\ (nm)}{Ideal\ cell\ size\ (nm)} \tag{4.6}$$

For instance, if the required circuit's cell-size is 14×14 nm, considering the ideal cell-size as 18×18 nm, then the SF is calculated as $SF = 14/18 = 0.7778$. The proposed adder designs have been evaluated for the following SFs:

$SF = 1$: QCA cell-size: 18×18 nm

$SF = 0.8889$: QCA cell-size: 16×16 nm

$SF = 0.7778$: QCA cell-size: 14×14 nm

The design structure for $SF = 0.8889$ and 0.7778 mirrors that of $SF = 1$ cells, as depicted in Figs. 4.16(d), 4.19, 4.21(a), and 4.21(b) for FA and n-bit-RCA designs, respectively. Table 4.10 evaluates the performance of the multi-layer adder designs presented in this section, considering various scaling factors. In the table, TA denotes the total area, while CA refers to the cell area, both measured in μm^2.

Table 4.10: Performance evaluation of ML adder designs across multiple SFs

Circuit	**Complexity**	**TA** (μm^2)	**CA** (μm^2)	**Latency**	**Cost$_{AD}$**	**Cell-size** (nm^2)	**SF**
1-bit	32	0.03	0.0103	0.5	0.0075	18×18	1
	32	0.02	0.0081	0.5	0.005	16×16	0.889
	32	0.01	0.0062	0.5	0.0025	14×14	0.7778
4-bit	160	0.17	0.0518	1	0.17	18×18	1
	160	0.13	0.0409	1	0.13	16×16	0.889
	160	0.098	0.0313	1	0.098	14×14	0.7778
8-bit	342	0.47	0.11	2	1.88	18×18	1
	342	0.38	0.0875	2	1.52	16×16	0.889
	342	0.24	0.067	2	0.96	14×14	0.7778
16-bit	768	1.36	0.248	4	21.76	18×18	1
	768	1.09	0.196	4	17.44	16×16	0.889
	768	0.79	0.1505	4	12.64	14×14	0.7778

Scaling Impact on Design Area: The influence of QCA scaling on the design area of the developed adder circuits is investigated. For the multi-layer FA QCA cells, the following results are observed:

- The 16×16 nm QCA cell design occupies an area of 0.02 μm^2, representing a 33.33% reduction in area compared to the 18×18 nm QCA cell.
- The 14×14 nm QCA cell design requires only 0.01 μm^2, yielding a 66.66% reduction in area relative to the 18×18 nm QCA cell.

Similarly, for the different bit configurations of the RCA circuit, the following percentage improvements are observed:

- The 4-bit RCA shows design area improvements of 23.5% for 16×16 nm cell size and 42.35% for v cell size, compared to the 18×18 nm QCA cell.
- The 8-bit RCA demonstrates advancements of 19.14% for 16×16 nm cell size and 48.9% for 14×14 nm cell size in the design area, respectively, as compared to the 18×18 nm QCA cell.
- The 16-bit RCA shows an improvement in design area of 19.85% for 16×16 nm cell size and 41.9% at 14×14 nm cell size, respectively, compared to the 18×18 nm QCA cell.

It can be noticed from Table 4.10 that decreasing the QCA cell size has a significant impact on the design area of adder circuits, resulting in greater efficiency and compactness for both FA and RCA designs.

Scaling Impact on Quantum Cost ($Cost_{AD}$): The effectiveness of QCA designs is majorly determined by the cost parameter. The most widely employed cost parameter (denoted as Cost_{AD}) [69], is derived by multiplying the total area (measured in μm^2) with the square of the latency (number of clock cycles). This equation establishes a clear and direct relationship between the cost function, the total area, and the corresponding delay in clock-cycles. Consequently, any optimization achieved in the total area through scaling-down will also lead to reduction in the quantum cost, enhancing the overall effectiveness of the QCA circuit designs. Specifically, for 1-bit-FA experiences Cost_{AD} is reduced by 33.3% and 66.66% for QCA cell sizes 16×16 nm and 14×14 nm respectively. Similarly, 23.5% and 42.35% reduction in Cost_{AD} is achieved for a 4-bit RCA circuit for cell sizes 16×16 nm and 14×14 nm respectively. Comparable reductions of 19.14% and 48.9% in Cost_{AD} are observed for 8-bit RCA for cell sizes of 16×16 nm and 14×14 nm respectively. In addition, Cost_{AD} is decreased for 16-bit RCA by 19.85% for a 16×16 nm cell and by 41.91% for a 14×14 nm

cell. These results highlight the significance of scaling down QCA cell sizes, leading to substantial improvements in area-delay costs and enhancing the overall efficiency of QCA circuit designs.

4.3.3 Energy Dissipation Analysis using QCADesigner-Ev2.2

The proposed 4-bit-RCA circuit's energy dissipation is determined using the coherence-vector with-energy engine in the QCADesigner-E v2.2 tool. As a result, the TED amounts to 4.8e-002 eV, with a small error of -4.88e003 eV. The AED per cycle is 4.36 e-003 eV, with a small error of -4.44e-004 eV. Table 4.11 provides an overview of energy dissipation results obtained through QCADesigner-E v2.2 comparing different 4-bit RCA designs. Notably, when contrasted with the latest state-of-the-art designs, the proposed 4-bit RCA stands out by demonstrating the least energy dissipation due to the compact, and systematic arrangement and placement of cells across three layers within the circuit.

Table 4.11: Energy dissipation of 4-bit-RCA circuits using QCADesigner-Ev2.2

4-bit RCA Designs	**AED per cycle** (eV)	**TED** (eV)
[115]	5.91e-003	6.32e-002
[129]-a	7.19e-003	7.91e-002
[129]-b	6.63e-003	7.29e-002
[134]-a	13.1e-003	14.4e-002
[134]-b	10.3e-003	11.4e-002
[135]	5.53e-003	6.09e-002
[136]	5.27e-003	5.80e-002
Proposed	**4.36e-003**	**4.80e-002**

4.3.4 Average Output Polarization Analysis

The Average Output Polarization (AOP) represents the average energy difference between the maximum(P_{max}) and minimum(P_{min}) polarization states of the output cells in the QCA circuit [137] calculated as:

$$AOP = \frac{P_{max} - P_{min}}{2} \tag{4.7}$$

For the output sum of the considered FA circuit with the scaling factor of 0.7778, the maximum polarization at $T = 2K$ is $9.72e-01$ and the minimum polarization is

$-9.72e-01$; hence, the AOP can be calculated as shown in Eq. 4.8:

$$\frac{[(9.72e-001)-(-9.72e-001)]}{2} = 3.57578 \tag{4.8}$$

Table 4.12: AOP calculation for ML-FA using Bi-stable approximation engine in QCADesigner-E tool for $T = 1K$

Cell Size (nm^2)	**Output**	P_{max}	P_{min}	**AOP**	**TST**
18×18	sum	9.54e-001	-9.54e-001	3.509	5 sec
	CY	9.55e-001	-9.55e-001	3.513	
16×16	sum	9.63e-001	-9.63e-001	3.542	5 sec
	CY	9.65e-001	-9.65e-001	3.55	
14×14	sum	9.72e-001	-9.72e-001	3.576	4 sec
	CY	9.74e-001	-9.74e-001	3.583	

Table 4.13: AOP calculation for ML-FA using CV engine in QCADesigner-E for $T = 1K$

Cell Size	**Output**	**Euler**				**Runge Kutta**			
(nm^2)		$P_{\max}$	$P_{\min}$	AOP	TST (s)	$P_{\max}$	$P_{\min}$	AOP	TST (s)
18×18	sum	0.955	-0.955	3.513	27	0.955	-0.955	3.513	62
	CY	0.955	-0.955	3.513		0.955	-0.955	3.513	
16×16	sum	0.964	-0.964	3.546	26	0.964	-0.964	3.546	60
	CY	0.965	-0.965	3.550		0.965	-0.965	3.550	
14×14	sum	0.972	-0.972	3.575	26	0.972	-0.972	3.575	60
	CY	0.974	-0.974	3.583		0.974	-0.974	3.583	

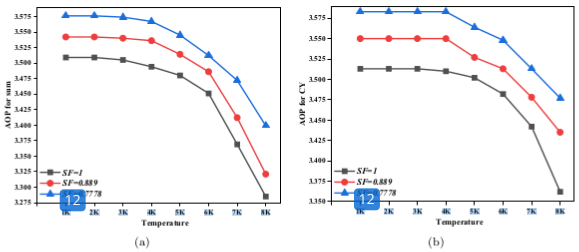


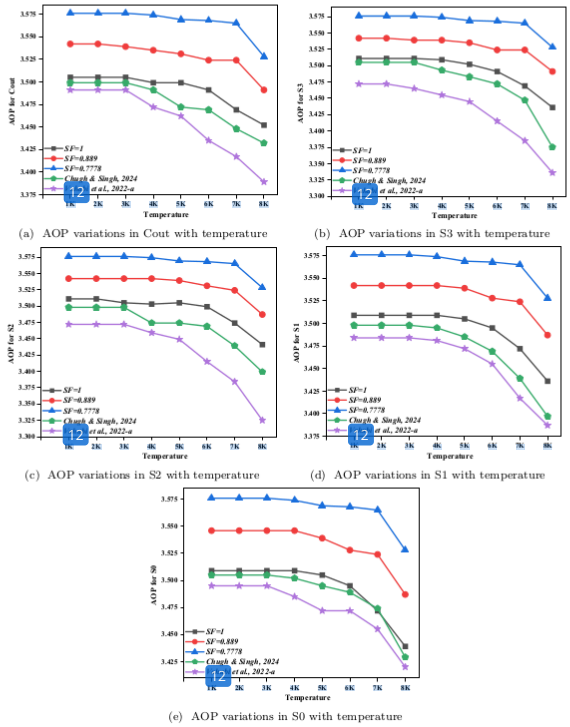
Figure 4.22: AOP versus temperature for ML-FA for three SFs

In Tables 4.12 and 4.13, P_{max}, P_{min}, AOP, and TST are the the maximum value of output polarization, the minimum value of polarization, average output polarization,

and total simulation time respectively for three different simulation engines across various SF for $T = 1K$. The average output polarisation for the 1-bit FA is assessed at varying temperatures through the application of the Euler method within the coherence vector simulation engine in QCADesigner-E tool. This analysis considered three distinct scaling factors ($SF = 1, 0.889, 0.7778$), and the compelling results are visually represented in Figure 4.22. Notably, the findings indicate the reliable functionality of the circuits, delivering precise outputs for both sum and carry functions within the temperature range of $1K$ to $8K$. However, as the temperature exceeds $8K$, the AOP experiences a significant and abrupt drop, resulting in inconsistent output for the FA. A discernible trend can be seen as the cell size is reduced, showcasing an enhanced resilience of the circuit and an increased AOP stability with temperature fluctuations. Furthermore, this analysis is also extended to the proposed 4-bit RCA, employing three distinct scaling factors. In comparison with circuits proposed by [136], as well as [129] with scaling factor of 1 (i.e. cell size of 18×18 nm), the results, illustrated in Figure 4.23, highlight intriguing insights. Significantly, the proposed RCA with $SF = 0.7778$, corresponding to cell-size of 14×14 nm, emerges as the most robust and consistent design across all five outputs[Cout S3 S2 S1 S0] within the temperature range up to $8K$. In contrast, the design by [129] exhibits significant polarisation drop for all outputs after reaching $6K$, indicating a potential performance limitation. Additionally, recent design by [136] reveals a sharp decline in polarisation for the output S3 after surpassing $6K$, resulting in an incorrect output. This comprehensive analysis underscores the importance of cell-size considerations in optimizing circuit performance across varying temperature conditions.

4.3.5 Quantitative Assessment of n-bit RCA Circuits: Key Design Metrics

The key metrics for the 4-bit RCA design, concerning previous designs at $SF = 1$, are presented in Table 4.14. The proposed 4-bit-RCA design excels in all parameters, achieving significant advancements across various multi-layer configurations. Notably, it demonstrates a substantial 81.4% reduction in Cost_{AD} compared to the approach by [115], an impressive 89.41% enhancement over [98], and a substantial 36% improvement compared to the design presented by[117] respectively.
Consequently, compared to the latest co-planar designs, our proposed approach outperforms existing models, achieving a cost reduction of 74.35% from [136], an im-



(a) AOP variations in Cout with temperature

(b) AOP variations in S3 with temperature

(c) AOP variations in S2 with temperature

(d) AOP variations in S1 with temperature

(e) AOP variations in S0 with temperature

Figure 4.23: AOP trends across temperature for proposed 4-bit-RCA across three SFs and reference designs

pressive 92.22% improvement over [135], an outstanding 98.14% reduction according to [134], and a notable 77.16% enhancement over [129] design. To further visualize these achievements, Figure 4.24 presents a graphical representation comparing the key parameters across various RCA circuit designs. The graph demonstrates that the proposed 4-bit RCA excels in all parameters by optimizing cell count, reducing the area, and minimizing latency. This optimization leads to a notable reduction in area-delay cost, highlighting the superior performance and cost-effectiveness of the proposed design across both multi-layer and co-planar architectures.

Table 4.14: Performance evaluation of 4-bit QCA-RCA

References	CC	TA (μm^2)	Delay	Crossover	Cost_{AD}
[138]	339	0.25	1.75	Co-planar	0.765
[112]	314	0.32	1.5	Multi-layer	0.72
[139]	308	0.29	2	Multi-layer	1.16
[140]	212	0.194	5	Co-planar	4.85
[115]	237	0.24	1.5	Multi-layer	0.54
[117]	184	0.1	1.25	Multi-layer	0.156
[108]	209	0.3	1.25	Co-planar	0.469
[113]	295	0.3	1.5	Co-planar	0.675
[98]	256	0.42	1.5	Co-planar	0.945
[135]	125	0.17	2.75	Co-planar	1.286
[129]-a	233	0.28	1.25	Co-planar	0.438
[129]-b	209	0.25	1.25	Co-planar	0.391
[141]	250	0.36	2.75	Co-planar	2.723
[134]-a	331	0.44	3.5	Co-planar	5.39
[134]-b	309	0.38	3.5	Co-planar	4.655
[136]	174	0.39	1	Not-Required	0.39
Proposed	**160**	**0.1**	**1**	**Multi-layer**	**0.1**

Also, it's worth noting that only certain papers provide data for all 4-bit, 8-bit, and 16-bit RCA implementations. Table 4.15 clearly shows the percentage improvements achieved by our proposed RCA designs, highlighting their superiority over existing counterparts. The following insights further explain these advancements:

- The proposed design introduces substantial improvements in various metrics compared to [146]. Notably, it achieves a remarkable remarkable 47.36%, 37.09%, and 58.91% reduction in the total area for 4-bit, 8-bit, and 16-bit RCA, respectively. Additionally, the latency improvements are significant, with reductions of 55.55%, 52.94%, and 51.51% for 4-bit, 8-bit, and 16-bit RCA, respectively, when compared to the work of [146]. Furthermore, the proposed design outperforms this most recent design by showcasing noteworthy cost advancements of 89.58%, 86.07%, and 90.34% in 4-bit, 8-bit, and 16-bit RCA, respectively.

- In comparison to [145], the proposed ML RCA design exhibits notable improvements across all design metrics. Specifically, the proposed designs offer substantial cost reductions of 63%, 37.6%, and 41% for 4-bit, 8-bit, and 16- bit RCA, respectively.

Table 4.15: Comparison of various Design Metrics of n-bit-RCA

Ref.	**Bit**	**CO**	**Cells**		**Total Area**		**Cell Area**		**Latency**		**Cost$_{AD}$**		**CS**	**SF**
			Count	% Imp.	μm^2	% Imp.	μm^2	% Imp.	CC	% Imp.	$A * L^2$	% Imp	(nm^2)	
[115]	4	ML	237	32.48%	0.24	58.33%	0.08	32.89%	1.5	33.33%	0.54	81.50%	18×18	1
	8	ML	517	33.80%	0.59	33.90%	0.17	34.13%	2.5	33.33%	3.69	57.70%	18×18	1
	16	ML	1224	37.25%	1.55	31.61%	0.40	37.37%	4.5	33.33%	31.39	46%	18×18	1
[142]	4	ML	178	10.11%	0.17	41.17%	0.06	11.45%	1.5	33.33%	0.38	73.70%	18×18	1
	8	ML	455	24.80%	0.71	45.10%	0.15	26.66%	2.5	33.33%	4.44	64.90%	18×18	1
	16	ML	1298	40.83%	1.97	46.20%	0.42	40.48%	4.5	33.33%	39.89	57.50%	18×18	1
[143]	4	ML	651	75.42%	1.2	91.70%	0.21	76.19%	4.25	76.50%	21.68	99.50%	18×18	1
	8	ML	1449	76.39%	3.56	89.00%	0.47	76.59%	8.25	75.80%	242.3	99.40%	18×18	1
	16	ML	3771	79.63%	11.77	90.90%	1.22	79.67%	16.25	75.40%	3108.02	99.50%	18×18	1
[139]	4	ML	308	48.05%	0.29	65.50%	0.10	50.00%	2	50%	1.16	91.40%	18×18	1
	8	ML	695	50.79%	0.79	50.60%	0.23	52.17%	3.75	46.70%	11.11	86%	18×18	1
	16	ML	1759	56.34%	2.51	57.80%	0.57	56.14%	5	20%	62.75	73%	18×18	1
[144]	4	CP	558	71.32%	0.85	88%	0.18	72%	5	80%	21.25	99.50%	18×18	1
	8	CP	1528	77.61%	2.93	86.70%	0.50	78.00%	9	77.80%	237.33	99.30%	18×18	1
	16	CP	4652	83.49%	10.85	90.20%	1.51	83.44%	17	76.50%	3135.65	99.50%	18×18	1
[145]	4	ML	166	3.61%	0.12	16.70%	0.05	0.00%	1.5	33.33%	0.27	63%	18×18	1
	8	ML	430	20.46%	0.4	2.50%	0.14	21.43%	2.5	33.33%	2.5	37.60%	18×18	1
	16	ML	1246	38.36%	1.42	25.40%	0.40	38.00%	4.5	33.33%	28.76	41%	18×18	1
[140]	4	CP	212	24.52%	0.194	48.50%	0.07	28.57%	1.25	20%	0.3	66.70%	18×18	1
	8	CP	513	33.33%	0.452	13.70%	0.17	35.29%	2.25	20%	2.29	31.90%	18×18	1
	16	CP	1401	45.18%	1.44	26.40%	0.45	44.44%	4.25	20%	26.01	34.80%	18×18	1
[146]	4	CP	156	-2.5%	0.19	47.36%	0.05	0.00%	2.25	55.55%	0.96	89.58%	18×18	1
	8	CP	501	31.70%	0.62	37.09%	0.16	31.25%	4.25	52.94%	11.2	86.07%	18×18	1
	16	CP	1205	36.26%	2.58	58.91%	0.39	35.89%	8.25	51.51%	175.6	90.34%	18×18	1
Proposed	**4**	**ML**	**160**	**-**	**0.1**	**-**	**0.05**	**-**	**1**	**-**	**0.1**	**-**	18×18	**1**
	4	**ML**	**160**	**-**	**0.09**	**-**	**0.04**	**-**	**1**	**-**	**0.1**	**-**	16×16	**0.889**
	4	**ML**	**160**	**-**	**0.08**	**-**	**0.03**	**-**	**1**	**-**	**0.09**	**-**	14×14	**0.7778**
Proposed	**8**	**ML**	**342**		**0.39**		**0.11**		**2**		**1.56**		18×18	**1**
	8	**ML**	**342**	**-**	**0.24**	**-**	**0.09**	**-**	**2**	**-**	**0.96**	**-**	16×16	**0.889**
	8	**ML**	**342**		**0.19**	**-**	**0.07**	**-**	**2**	**-**	**0.76**	**-**	14×14	**0.7778**
Proposed	**16**	**ML**	**768**	**-**	**1.06**	**-**	**0.25**	**-**	**4**	**-**	**16.96**	**-**	18×18	**1**
	16	**ML**	**768**	**-**	**0.79**	**-**	**0.20**	**-**	**4**	**-**	**12.64**		16×16	**0.8889**
	16	**ML**	**768**	**-**	**0.68**	**-**	**0.15**	**-**	**4**	**-**	**10.88**	**-**	14×14	**0.7778**

CO: Crossover, CS: cell-size

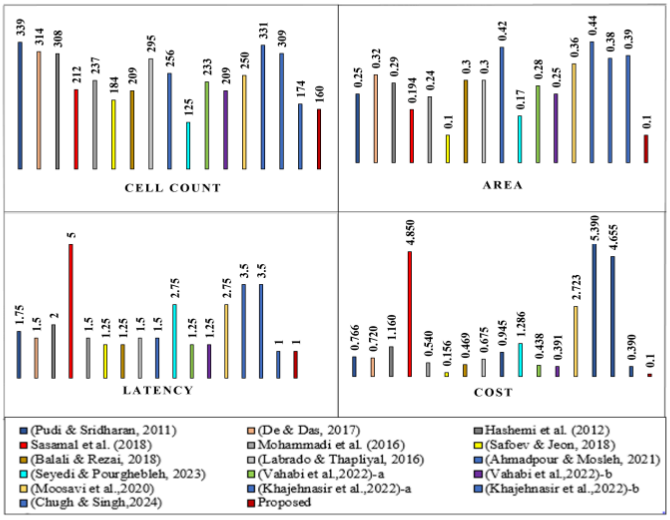


Figure 4.24: Comparison of performance metrics for 4-bit RCA

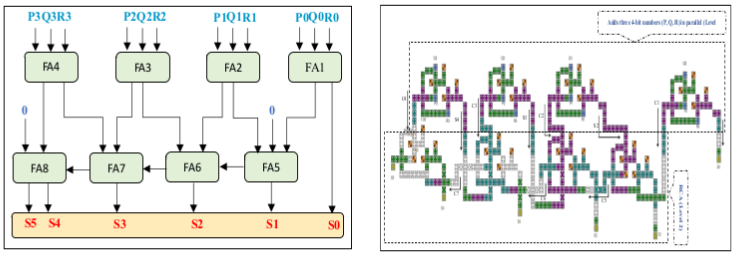
- Similarly, when contrasted with the designs presented by [140], the proposed 4-bit,8-bit and 16-bit-RCA designs demonstrate significant cost enhancements of 66.7%, 31.9%, and 34.8%, respectively. These findings underscore the superiority of the proposed ML-RCA over existing methodologies.

Ultimately it is observed that as the bit-size increases, the proposed RCA consistently outperforms across all important design metrics, indicating its superior performance and efficiency.

4.4 An Efficient Co-Planar Design of Carry-Save Adder Circuit (QCA-3x4B-CSA) using Quantum-Dot Cellular Automata with Optimized Energy Dissipation

4.4.1 Proposed QCA-3x4B-CSA Circuit Implementation

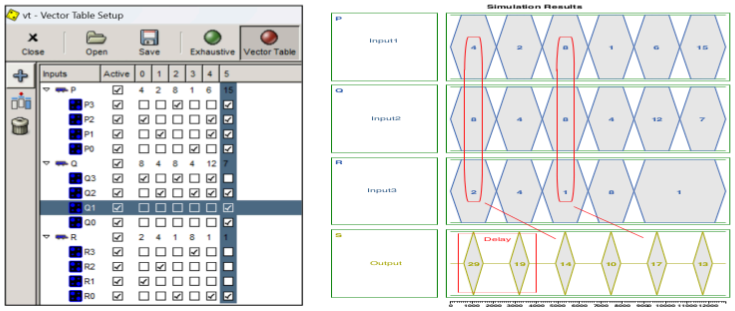
This section presents the design approach and implementation of the 4-bit three-input carry-save adder (QCA-3x4B-CSA) circuit. The full adder, shown in Fig. 4.3(a) [136], serves as the foundational building block for implementing the QCA-3x4B-CSA circuit. The structural diagram representation of the QCA-3x4B-CSA circuit is



(a) Structural diagram (b) QCA Implementation

Figure 4.25: The proposed three-input 4-bit carry save adder (QCA-3x4B-CSA)

demonstrated in Fig. 4.25(a). The implementation utilizes eight FA circuits which take three 4-bit inputs as P [P3P2P1P0] , Q [Q3Q2Q1Q0] and R [R3R2R1R0] to generate a 6-bit output S [S5S4S3S2S1S0]. The QCA-3x4B-CSA layout employs the co-planar cross-wiring technique to reduce costs since multi-layer crossover designs typically result in higher fabrication costs. The suggested QCA-based QCA-3x4B-CSA circuit design, illustrated in Fig. 4.25(b), ensures minimal delay of 1.25 clock cycles with total cell count of 431 cells in an area of 0.512 μm^2. Due to the extensive entries in the QCA-3x4B-CSA truth table, a few vector sets are examined, as shown in the vector table in Fig. 4.26(a). Based on this, the simulation outputs are verified in Fig. 4.26(b) to demonstrate the proficiency of the QCA-3x4B-CSA circuit.

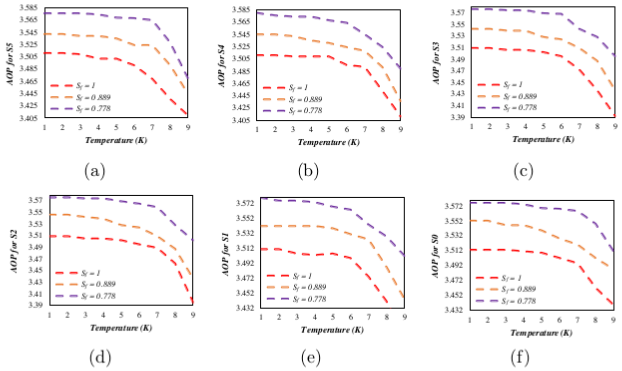


(a) Defined vector table (b) Verified simulated waveform

Figure 4.26: The proposed three-input 4-bit carry save adder (QCA-3x4B-CSA)

4.4.2 Average Output Polarization

The average output polarization for the proposed QCA-3x4B-CSA circuit is assessed for all outputs at varying temperatures through the application of the Euler method within the coherence vector simulation engine in QCADesigner-E tool. The com-



(a) (b) (c)

(d) (e) (f)

Figure 4.27: AOP trends across temperature for proposed QCA-3x4B-CSA circuit across three SF

pelling results for the outputs S5-S0 across three scaling factors are visually repre-

sented in Fig. 4.27. The graphs clearly indicate the stable functionality of the QCA-3x4B-CSA circuit, providing accurate outputs [S5-S0] across a temperature range of $1K$ to $8K$. However, beyond $8K$, the AOP experiences a sharp decline for all bits, resulting in inconsistent performance. It is worth noticing further that the proposed QCA-3x4B-CSA circuit with $S_f = 0.778$, corresponding to the QCA cell dimensions of 14x14 nm, emerges as the most resilient and uniform design across all six outputs [S5 S4 S3 S2 S1 S0] within $T \leq 8K$.

4.4.3 Energy Dissipation Analyses

Energy dissipation is a crucial factor that significantly influences the performance of QCA circuits. The analysis is performed using the QCADesigner-E v2.2 [85] and QCAPro [86] softwares.

Energy Dissipation Analyses using QCADesigner-E v2.2:
The adder circuits are evaluated for the energy dissipation using the QCADesigner-E v2.2 software. An overview of the obtained energy dissipation results for the adder circuits and the Cost_{ED} are presented in Table 4.16. It is evident from the Table that

Table 4.16: Analysis of energy dissipation of the proposed adder circuits using QCADesigner-E v2.2

Circuit	SF	Average ED (eV)		Total ED (eV)		Cost_{ED}
		E_{bath}	E_{rr}	E_{bath}	E_{rr}	
FA [136]	1	1.83e-003	-1.83e-004	2.01e-002	-2.02e-003	0.0001
	0.889	1.59e-003	-1.58e-004	1.75e-002	-1.76e-003	0.00007
	0.778	1.35e-003	-1.32e-004	1.49e-002	-1.45e-003	0.00005
QCA-3x4B-CSA	1	1.01e-002	-8.33e-004	1.11e-001	-8.33e-004	0.018
	0.889	9.72e-003	-8.12e-004	1.06e-001	-8.12e-004	0.017
	0.778	8.84e-003	-7.13e-004	9.68e-002	-7.84e-003	0.014

the QCA cell size scaling has a significant impact on the proposed circuits, leading to reductions in total energy dissipation and cost. Specifically, for the FA [136] circuit, 14x14 nm cell size corresponding to a $S_f = 0.778$ shows 25.9% reduction in TED as compared to the ideal size and a corresponding 50% reduction in the Cost_{ED}. Similarly, the scaling of 0.778 in the proposed QCA-3x4B-CSA circuit decreases the TED to 12.2% marking a 22.2% reduction in Cost_{ED}, making the circuits more energy-efficient and cost-effective at smaller cell sizes.

Energy Dissipation Analyses using QCAPro:

QCAPro software [86] serves as a probabilistic simulation platform that uses fast approximation to analyze both polarization inaccuracies and energy dissipation from non-adiabatic switching. The power dissipation maps displaying the thermal hotspots for the suggested QCA-3x4B-CSA layout is shown in Fig. 4.28. The Table 4.17 further presents the switching, leakage and total power dissipation for the suggested adder circuits along-with the Cost_{ED} parameter evaluated at different tunneling energies, specifically at $0.5E_k$, $1.0E_k$, and $1.5E_k$ at a fixed temperature of $2K$ presuming all QCA cells have constant power consumption.

Table 4.17: Evaluation of Energy Dissipation for Adder Designs under Varying Tunneling Energy Conditions

Circuit	0.5 E_k	1.0 E_k	1.5 E_k	Energy Dissipation
FA [136]	9.37	27.75	49.5	Leakage (meV)
FA [147]	22.14	67.37	120.49	
4-bit RCA [147]	116.69	531.01	912.43	
4-bit CLA [147]	356.84	1075.9	1612.2	
Proposed QCA-3x4B-CSA	150.32	410.1	631.18	
FA [136]	42.24	36.26	28.88	Switching (meV)
FA [147]	122	105.31	89.42	
4-bit RCA [147]	779.3	658.22	549.02	
4-bit CLA [147]	871.09	723.93	623.97	
Proposed QCA-3x4B-CSA	367.5	313.17	254.22	
FA [136]	51.61	64.1	78.38	Total (meV)
FA [147]	144.2	172.68	209.91	
4-bit RCA [147]	896.07	1189.23	1461.45	
4-bit CLA [147]	1227.93	1799.83	2236.15	
Proposed QCA-3x4B-CSA	517.82	723.25	885.4	
FA [136]	0.0006	0.00102	0.00153	Cost_{ED}
FA [147]	36.05	43.17	52.4775	
4-bit RCA [147]	10976.86	14568.07	17902.76	
4-bit CLA [147]	78587.52	115189.1	143113.6	
Proposed QCA-3x4B-CSA	0.417	0.816	1.223	

4.4.4 Comparative Insights on Performance Metrics

This section provides a comparative analysis of the proposed QCA implementation of the QCA-3x4B-CSA circuit against existing designs in the literature, focusing on

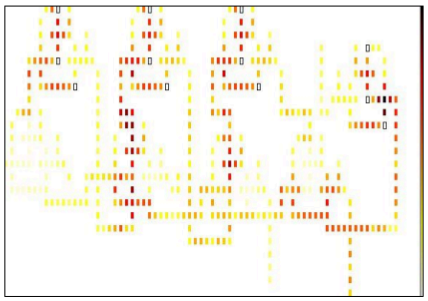


Figure 4.28: Thermal Distribution at $E_k = 0.5$ of the Three-Input QCA-3x4B-CSA Circuit Observed at $T = 2\,K$

key performance metrics such as number of cells, latency, design space, and area-to-delay cost (Cost_{AD}). Furthermore, the performance of the presented adder circuit is evaluated in relation to other complex adder architectures, offering a comprehensive view of its efficiency and competitive advantages. Table 4.18 compares the suggested

Table 4.18: Comparative Analysis of QCA-3x4B-CSA designs with recent state of art

Reference	**Cell Count**	**Latency**	**Area**	**Layer**	**Cost_{AD}**	**SF**
[148]	525	2.5	0.55	ML	3.44	1
[103]	696	2.25	0.66	CP	3.34	1
[131]	347	2.25	0.37	ML	1.87	1
[149]	521	1.75	0.62	CP	1.91	1
[150]	662	1.75	0.83	CP	2.54	1
Proposed	431	1.25	0.512	CP	0.8	1
Proposed	431	1.25	0.399	CP	0.62	0.889
Proposed	431	1.25	0.289	CP	0.45	0.778

QCA implementation of the QCA-3x4B-CSA circuit with the existing designs. The following observations highlight the improvements in various parameters:

- *Cell count:* The proposed QCA-3x4B-CSA circuit with $S_f = 1$ shows an impressive 38.07% and 34.89% reduction compared to [103] and [150] respectively. A notable 17.27% reduction is observed as compared to the most recent design [149]. However, there is a slight increase in cell count when compared to [131], as it uses multi-layer crossover technique to minimize the cell count but further increases fabrication cost.

- *Latency:* The suggested design achieves an impressive 50% and 44.44% reduction in latency as compared to the designs presented by [150] and [103]. A notable 28.57% improvement is seen in contrast to the recent reported design by [149].

- *$Cost_{AD}$:* The proposed QCA-3x4B-CSA design shows an impressive 77.03%, 76.35% and 68.9% reduction in Cost_{AD} compared to CSA designs in [148], [103] and [150] respectively. Additionally, a significant improvement of 58.64% is observed compared to the recent design by [149]. Further, as the SF is reduced, a significant decrease in the Cost_{AD} is observed. For the cell size of 14x14 nm, a total cost reduction of 43% is observed in the proposed design in contrast to the ideal cell size.

Table 4.19: Comparison of performance metrics of various adders

Circuits	**Cell Count**	**Latency**	**Area**	**Layer**	**Cost_{AD}**
Ladner-Fischer [138]	698	2	0.618	ML	2.47
Kogge-Stone [138]	815	2	0.738	ML	2.95
Han Carlson [138]	680	1.75	0.645	ML	1.97
Brent-Kung [138]	680	1.75	0.645	ML	1.97
CLA [103]	777	2.75	0.92	ML	6.96
CLA [151]	568	4.25	1.26	ML	22.75
CLA [147]	739	8	2.10	CP	134.4
CLA [152]	1575	3.5	1.89	CP	23.15
Proposed QCA-3x4B-CSA	431	1.25	0.512	CP	0.79

The proposed QCA-3x4B-CSA design demonstrates superior performance across all design metrics when compared to various existing adders, as illustrated in Table 4.19. Specifically, the proposed design achieves a significant 88.64% improvement in the Cost_{AD} as compared to the carry lookahead adder (CLA) by Cho et al. [152] and an impressive 77.48% improvement compared to the most recent CLA adder presented in [103]. Furthermore, substantial cost improvements are also observed relative to the various adders presented by Pudi et al. [138], with improvements of 68.02% over the LFA, 73.22% over the KSA, and 59.90% over both the HCA and BKA. Notably, the proposed CSA circuit significantly outperforms the most recent CLA adder [147]. These enhancements underscore the efficiency and effectiveness of the proposed design in optimizing key performance parameters.

4.5 Summary

This chapter presented a comprehensive investigation into QCA-based adder circuits, covering both co-planar and multilayer implementations, with the goal of achieving minimal area, delay, and energy consumption. Novel half and full adder layouts were proposed and extended into 4-bit, 8-bit, and 16-bit RCAs, along with a three-input CSA. The multilayer RCA architecture achieved up to 90.3% reduction in quantum cost and significant improvements in latency and area compared to recent state-of-the-art designs, while the co-planar RCA design, implemented without crossovers or rotational cells, achieved a 61.1% reduction in quantum cost and 58.4% improvement in latency. The proposed CSA design further enhanced efficiency, showing a 76.35% improvement in quantum cost over comparable existing circuits. Detailed simulations using QCADesigner-E and QCAPro validated the proposed designs' robustness in terms of energy dissipation, delay, and output polarization across varying temperatures and scaled cell sizes. Comparatively, the multilayer architectures offer greater compactness and performance, while the co-planar designs provide layout simplicity and fabrication feasibility. These results confirm the potential of QCA as a scalable, low-power alternative to CMOS for arithmetic logic design. The validated adder designs developed in this chapter form the foundational building blocks for the multiplier architectures discussed in the following chapter, where they are leveraged to construct efficient Vedic multipliers using QCA technology.

Chapter 5

Design and implementation of a cellular automata-based Vedic multiplier using designed adders to analyze performance in terms of complexity, area, delay, and cost functions

5.1 Introduction

Recent advancements in Quantum-dot Cellular Automata (QCA) have led to efficient implementations of arithmetic circuits, particularly adders and multipliers, with a strong focus on minimizing carry propagation delay [153, 154, 155]. In parallel, researchers have explored various sutra-based Vedic multiplier (VM) designs in QCA, such as Urdhva Tiryakbhyam, Nikhilam, and Anurupayana. Earlier works, including layered 2-bit and 4-bit architectures by Pooja et al. [156], and co-planar FIR filter-based VMs by Gassoumi et al. [76], demonstrated functional implementations but suffered from high cell counts, and significant latency. To address these limitations, Gassoumi et al. further proposed a low-power MAC design using the USE clocking scheme, though the design remained bulky and incurred high latency [77]. Efforts to reduce these constraints include Safoev and Jeon's compact 2×2 VM with a delay of 2.25 clock cycles [71], and Bahar et al.'s n-bit serial-parallel co-planar VM using a modified XOR gate, which showed notable reductions in area and cell usage along with detailed energy analysis [157]. Other contributions include squarer circuits by Khan et al. [70], achieving impressive gains in density and power, and recent works like Ahmadpour's reversible logic-based multiplier for IoT [158] and Daggula's 4-bit VM boasting 90% power efficiency over CMOS [159]. Despite these efforts, the field still lacks comprehensive performance analyses. Addressing this gap, this chapter begins with the physical verification and detailed fault analysis of the proposed half adder design, which is then integrated into a novel 2-bit VM implementation. The complete design is evaluated using QCADesigner-E and QCAPro; thus establishing a strong foundation for scalable, high-performance Vedic multiplication in QCA technology.

5.2 Physical Verification of HA Operation Using Kink Energy

In this section, the HA design presented in Figure 4.2(a) [136] serves as the foundation for implementing the 2-bit VM. The ongoing efforts involve conducting the physical verification and fault analysis to thoroughly explore the integration and performance of HA design in this context. When designing QCA circuits, it's crucial to understand that the polarization state of a cell isn't solely influenced by the input signal; rather, it intricately depends on the collective dynamics of its neighboring cells [160]. This principle tends to be overlooked in design processes, giving rise to sneaky noise paths. These unintended interactions between adjacent cells can lead to unwanted information flow within the QCA framework [160, 161]. While these spurious noise channels may seem negligible in smaller QCA designs, their impact grows exponentially as the design scales in size and complexity,resulting in functional failures. This phenomenon is related to the concept of kink energy, which represents the potential energy between electrons in QCA cells. The cumulative energy of a cell is derived from the kink energies of its neighboring cells, with the strength of each interaction diminishing as the distance increases. In accordance with this, the noise channels persist as long as multiple quantum cells coexist within each other's radius of influence. These paths can disrupt the intended operation of logically sound QCA building blocks, posing a challenge to the hierarchical composition of larger QCA designs.

To substantiate the physical validity of the proposed QCA-based HA design, our assumptions include uniform quantum cell dimensions (18×18 nm) and a 2 nm proximity between adjacent cells. Graphically, QCA cells are depicted as squares, with electron positions denoted by circles within each cell [162]. To ensure stability, the arrangement of electrons within each cell is meticulously optimized to minimize their potential energy. The energy (U) among two charges a and b is calculated in *Joules* using Eq.5.1

$$U_{ab} = \frac{1}{4\pi\pi_0\epsilon_r}\frac{q_a q_b}{|r_a - r_b|} \tag{5.1}$$

where ϵ_r is the relative permittivity, q_a and q_b are the charges of a and b cells separated by a distance of $|r_a - r_b|$. By replacing all standard values, U_{ab} can be written as

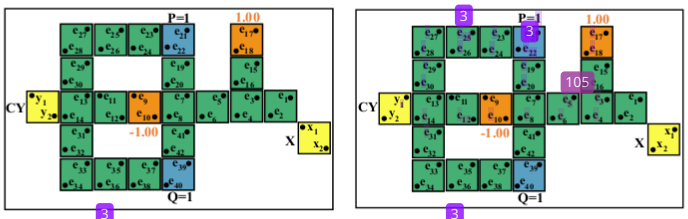
shown in Eq.5.2

$$U_{ab} = \frac{9 \times 10^9 \times (1.6)^2 \times 10^{-38}}{r_{ab}} = \frac{23.04 \times 10^{-29}}{r_{ab}} \tag{5.2}$$

The total potential energy (U_T) is determined by summing the potential energies calculated using Eq. 5.3 [160]:

$$U_T = \sum_{x=1}^{n} U_{ab} \tag{5.3}$$

The key principle of this approach is to determine the state with the minimum potential energy [161]. Since the HA has two inputs, it would have four different input combinations, resulting in a large number of calculations. To simplify the analysis, only the gate accuracy for the input mode (P, Q) = (1, 1) is considered in Fig. 5.1. The kink energy between electrons in the output cells X(x_1 and x_2) and CY(y_1,



(a) X=0 and CY=0 (b) X=1 and CY=1

Figure 5.1: The cellular network lattice of the proposed HA

Table 5.1: Computation of kink energy among all electrons of Figure 5.1(a)

For electron x_1	**For electron x_2**
$U_{x_1} = \sum_{i=1}^{42} U_{ix_1} = 9.86 \times 10^{-20} J$	$U_{x_2} = \sum_{i=1}^{42} U_{ix_2} = 10.75 \times 10^{-20} J$
$U_{x_1 x_2} = U_{x_1} + U_{x_2} = (9.86 + 10.75) \times 10^{-20} = 20.61 \times 10^{-20} J$	
For electron y_1	**For electron y_2**
$U_{y_1} = \sum_{i=1}^{42} U_{iy_1} = 14.74 \times 10^{-20} J$	$U_{y_2} = \sum_{i=1}^{42} U_{iy_2} = 30.15 \times 10^{-20} J$
$U_{y_1 y_2} = U_{y_1} + U_{y_2} = (14.74 + 30.15) \times 10^{-20} = 44.89 \times 10^{-20} J$	

y_2) with all other electrons is calculated and presented in Tables 5.1 and 5.2. These Tables analyze different scenarios based on the assumed values for the output sum and carry signals. However, Table 5.1 examines the situation where the output sum and carry are assumed to be zero. Similarly, Table 5.2 analyzes the scenarios with the

Table 5.2: Computation of kink energy among all electrons of Figure 5.1(b)

For electron x_1	**For electron x_2**
$U_{x_1} = \sum_{i=1}^{42} U_{ix_1} = 13.66 \times 10^{-20} J$	$U_{x_2} = \sum_{i=1}^{42} U_{ix_2} = 9.76 \times 10^{-20} J$
$U_{x_1x_2} = U_{x_1} + U_{x_2} = (13.66 + 9.76) \times 10^{-20} = 23.42 \times 10^{-20} J$	
For electron y_1	**For electron y_2**
$U_{y_1} = \sum_{i=1}^{42} U_{iy_1} = 26.25 \times 10^{-20} J$	$U_{y_2} = \sum_{i=1}^{42} U_{iy_2} = 15.14 \times 10^{-20} J$
$U_{y_1y_2} = U_{y_1} + U_{y_2} = (26.25 + 15.14) \times 10^{-20} = 41.4 \times 10^{-20} J$	

output sum and carry assumed to be one, respectively. The kink energy values in the corresponding tables can be compared to determine the correct values for the outputs X and CY, as a stable state has less energy. For the output CY, analyzing the values reveals that one is the correct value. Similarly, for the output X, the correct value is zero.

5.3 Reliability Assessment and Defect Analyses of the Proposed HA

- *Resilience to Single-Cell Omission Defect:*
  The suggested HA circuit is examined for its resilience against the omission of single-cell defect (SCOD) with the exception of the input, output, and fixed cells. To uniquely distinguish each cell within the circuit, a grid-based placement approach is utilized, as illustrated in Figure 5.2. The columns and rows of the matrix are labeled with natural numbers (1, 2, 3, etc.) and alphabet letters respectively. Table 5.3 shows that the X output demonstrates a fault tolerance ability of 58.8%, with 10 out of 17 instances producing fault-free outputs. However, the CY output achieves a fault tolerance ability of 70.58%, with only

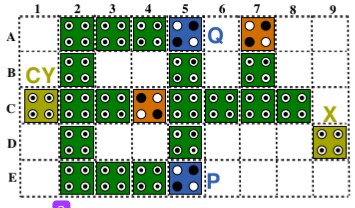


Figure 5.2: Layout of the fault-tolerant HA design

Table 5.3: Assessment of SCOD on proposed HA

Cell	Sum	Carry	Cell	Sum	Carry
A2	✓	×	A3	✓	✓
A4	✓	✓	B2	✓	×
B5	×	✓	B7	×	✓
C2	✓	×	C3	✓	✓
C5	×	✓	C6	×	✓
C7	×	✓	C8	×	✓
D2	✓	×	D5	×	✓
E2	✓	×	E3	✓	✓
E4	✓	✓			

12 out of 17 instances generating correct outputs. These results demonstrate the resilience of the HA circuit with a substantial majority of cases producing accurate outputs.

- *Resilience to Double-Cell Omission Defect:*
  Imperfect manufacturing processes can lead to the absence of multiple cells in a circuit. To assess the adder's resilience to this defect, the impact of double-cell omission (DCOD) is analysed on the circuit's sum and carry outputs. Table

Table 5.4: Assessment of DCOD on proposed HA

Cells	Sum	Carry	Cells	Sum	Carry
A2,A3	✓	×	A3,A4	✓	×
A2,B2	✓	×	B2,C2	✓	×
B5,C5	×	✓	B7,C7	×	✓
C2,D2	✓	×	C2,C3	✓	×
C5,C6	×	✓	C7,C8	×	✓
C5,D5	×	✓	D2,E2	✓	×
E2,E3	✓	×	E3,E4	✓	×

5.4 reveals that the X output exhibits a fault tolerance of 71.43%, while the CY output achieves a fault tolerance of 35.7%. These findings demonstrate the proposed adder's robustness against double-cell omission faults, with a significant majority of cases producing accurate outputs. Consequently, the proposed adder can be considered highly fault-tolerant in the presence of double-cell omission defect.

- *Resilience to Cell Displacement/Misalignment Defect:*
  This defect occurs when the displacement or misalignment of a cell exceeds a critical threshold (d_p), affecting the circuits functionality [163]. To ensure the robustness of HA circuit, the displacement of the device cells along four possible directions: North, South, East, and West is analyzed and presented in Table 5.5. Here, d_p represents the the maximum permissible displacement of a cell that does not affect the circuit's behavior. If a displacement or misalignment in a given direction is not possible, it is denoted by a '–'. Notably, a permissible displacement of $\geq 500nm$ suggests that the corresponding cell displacement has a negligible impact on the circuit's behavior. The results indicate that the HA circuit has a good tolerance against these defects.

Table 5.5: Assessment of cell displacement/misalignment defect for proposed HA circuit

	Displacement (d_p)		**Misalignment** (d_p)	
Cell	**North**	**South**	**East**	**West**
A2	$\leq 3nm$	-	-	$\leq 5nm$
A3	$> 500nm$	$\leq 16nm$	-	-
A4	$> 500nm$	$\leq 16nm$	-	-
Q	$\leq 3nm$	-	$\leq 7nm$	-
B2	-	-	$\leq 4nm$	$\leq 4nm$
B5	-	-	$\leq 1.2nm$	$\leq 5nm$
B7	-	-	$\leq 1.5nm$	$\leq 1.5nm$
CY	$\leq 3nm$	$\leq 3nm$	-	-
C3	$> 500nm$	$> 500nm$	-	-
C6	$< 1nm$	$< 1nm$	-	-
C7	-	$< 1nm$	-	-
C8	$\leq 1nm$	$\leq 7nm$	$< 10nm$	-
D2	-	-	$\leq 4nm$	$\leq 4nm$
D5	-	-	$\leq 1.2nm$	$\leq 5nm$
X	$\leq 10nm$	-	-	$\leq 10nm$
E2	-	$\leq 3nm$	-	$\leq 5\ nm$
E3	$> 500nm$	$\leq 16nm$	-	-
E4	$> 500nm$	$\leq 16nm$	-	-
P	-	$\leq 3nm$	$\leq 7nm$	-

- *Resilience to Extra Cell Deposition Defect:*
  The strength of the Coloumbic interaction between cells diminishes rapidly with increase in the distance. The radius of effect (RoE) is defined as the circular

area surrounding a cell's center within which it exerts influence on its neighbors. Therefore, cells placed in close proximity can affect each other's polarization

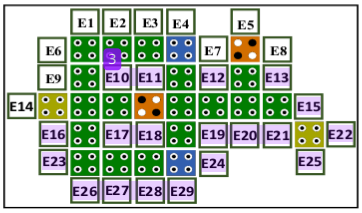


Figure 5.3: HA design with additional cell deposition

state. During the deposition process, extra cells may be introduced alongside those required for the circuit's proper operation. If these extra cells are positioned too close, they can degrade the circuit's performance. To assess the

Table 5.6: Assessment of ECDD on proposed HA

Cells	Sum	Carry	Cells	Sum	Carry
E1	✓	✓	E16	✓	✓
E2	✓	✓	E17	✓	✓
E3	✓	✓	E18	✓	✓
E4	✓	✓	E19	✓	✓
E5	✓	✓	E20	×	✓
E6	✓	✓	E21	×	✓
E7	✓	✓	E22	✓	✓
E8	✓	✓	E23	✓	✓
E9	✓	✓	E24	✓	✓
E10	✓	✓	E25	✓	✓
E11	✓	✓	E26	✓	✓
E12	×	✓	E27	✓	✓
E13	×	✓	E28	✓	✓
E14	✓	✓	E29	✓	✓
E15	×	✓			

proposed half-adder's resilience against such defects, additional cells labeled as E1-E29 are placed around the HA circuit, as displayed in Figure 5.3. The impact of each extra cell is individually analyzed (ECDD), and the observed outputs are summarized in Table 5.6. The sum output produced correct results for an impressive 24 of 29 possible scenarios, demonstrating an exceptional 82.75%

resilience against the deposition of the extra cells. Remarkably, carry exhibits unwavering fault tolerance, achieving 100% accuracy in all cases.

Table 5.7: Fault resilience assessment of QCA based Half Adder circuits

HA Designs	**SCOD**		**DCOD**		**ECDD**	
	Sum	**Carry**	**Sum**	**Carry**	**Sum**	**Carry**
[96]	57.14 %	28.57 %	66.66 %	33.33 %	68.18 %	63.63 %
[104]	23.53 %	76.47 %	25 %	75 %	76.47 %	88.24 %
Proposed	58.8%	70.6%	71.43%	35.7%	82.75%	100%

Further, Table 5.7 offers an extensive comparison of fault tolerance ratios among different HA circuits, including those designed by Majeed et al. [96] and Safoev et al. [104], which were examined for cell omission and cell addition defects. The table highlights the superior fault tolerance percentage of the proposed HA design compared to recent designs across all fault types for both outputs, as outlined below:

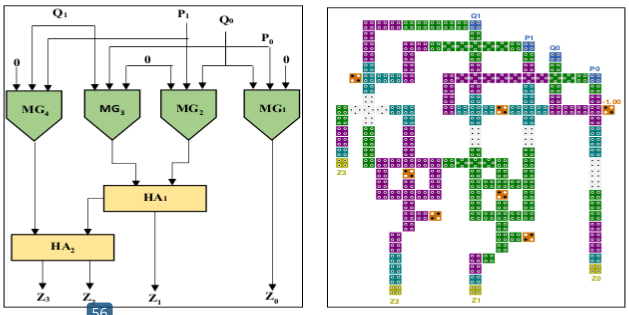
- For the sum output, it is evident that the proposed approach exhibits superior performance across all fault types compared to both references. Particularly, for SCOD, the proposed HA demonstrates a modest improvement of approximately 2.93% compared to [96], while achieving a remarkable 203.61% improvement compared to [104]. Similarly, for DCOD and ECDD, the proposed method showcases substantial enhancements of approximately 24.15% and 21.31%, respectively, compared to [96], and approximately 185.72% and 30.95%, respectively, compared to [104].

- Regarding the carry output, while the proposed method excels in improving carry output for SCOD compared to [96] (with a remarkable improvement of approximately 147.17%), it slightly lags behind [104], showing a decrease of approximately 53.26%. This lag can be attributed to the design of the underlying architecture of HA. However, for DCOD and ECDD, the suggested method outperforms both references significantly, achieving improvements of approximately 200% and 57.89%, respectively, compared to [96], and approximately 33.33% and 13.40%, respectively, compared to [104].

This comparison further underscores the robustness and potential efficacy of the proposed HA design in larger circuits.

5.4 Design and Implementation of the VM

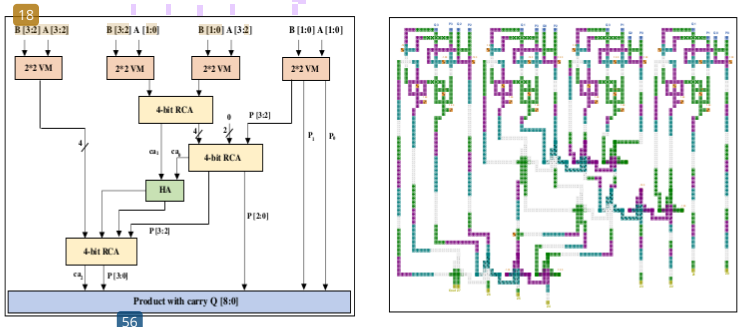
The QCA based VM design strategically utilizes co-planar wire-crossing for effective wire intersection, as illustrated in Figure 5.4. The proposed structure utilizes four



(a) Block diagram (b) QCA Implementation

Figure 5.4: The proposed 2-Bit VM

MGs and two half-adder circuits to implement the low-complexity 2-bit VM circuit. The number of cells in each clock zone are strategically used in order to ensure proper data propagation and transmission consistency. In particular, this design covers an area of 0.17 μm^2 utilizing only 179 QCA cells. The 4-bit VM can be constructed using



(a) Block diagram (b) QCA Implementation

Figure 5.5: The proposed 4-Bit VM

four modules of the proposed 2-bit VM, three ripple carry adders, and one OR gate, as illustrated in Figure 5.5(a) The corresponding QCA implementation, shown in Figure 5.5(b), achieves an efficient design with a minimum of 1762 cells, occupying an area of 1.76 μm^2 and operating with a latency of 4.25 clock cycles (17 clock zones). Figure 5.6

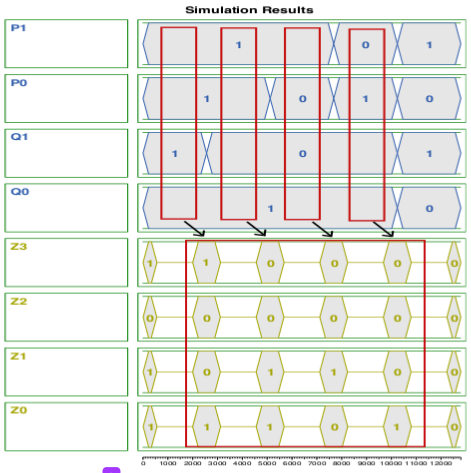


Figure 5.6: Simulated outputs of proposed 2-bit VM

illustrates the simulation waveform of the 2-bit VM, performed using QCADesigner-E (v2.2) with the coherence vector (energy-based) simulation engine under default parameters. The input waveforms of operands P (P_1P_0) and Q (Q_1Q_0), along with the resulting output waveforms of the product Z (Z_3, Z_2, Z_1, Z_0), are clearly depicted.

5.5 Holistic Examination and Comparative Assessment of the Proposed Circuit

Circuit Complexity Analysis: In the realm of QCA design, circuit complexity is typically assessed by evaluating the total number of majority gates (MG), inverters, and crossovers (CV) employed [69]. Among these metrics, the number of MGs holds particular significance, as it directly influences the circuit's irreversible power dissipation. Additionally, the number of crossovers in the design serves as an indicator

of fabrication difficulty, with multi-layer crossovers incurring a higher cost than co-planar crossovers. Therefore, minimizing these metrics becomes crucial to optimizing circuit performance.
In this regard, the proposed 2-bit VM design is a single-layer architecture, exclusively employing co-planar crossovers with a complexity of only 14, thereby minimizing both fabrication complexity and power dissipation.

Area Analysis: The overall area of a circuit is a prime consideration in assessing the efficiency and performance of the circuit. A smaller circuit area generally means lower power consumption and faster signal propagation.
Cell Area: This metric is computed by multiplying the cell count of the circuit by the default area of a cell ($18 \times 18\ nm^2$). In this context, the design efficiency of the presented VM circuit is established by cell area of 0.05 μm^2.
Total Area: In assessing the architecture, the overall rectangular region required for the implementation of the design is the total area of the circuit. An effective design minimizes the total area. The proposed VM circuit achieves a compact area of 0.176 μm^2.
Area Utilization Factor: The area utilization factor of a circuit is a measure of the efficiency with which available space is utilized. It is calculated as the ratio of cell area to total area, multiplied by 100. The proposed VM design demonstrates a commendable area utilization of 29.41%, indicating a favorable design approach, as a higher percentage is generally desirable.

Energy Calculation: Among various performance metrics, energy dissipation plays a crucial role in determining the overall efficiency of an electronic circuit. In the context of QCA circuits, two prominent methodologies are commonly employed to estimate power consumption. These methods involve using two well-established power estimation tools: QCAPro [86] and the QCADesigner-E tool [85] known for their effectiveness in estimating power consumption.
According to the upper bound energy dissipation model [164], the cumulative power dissipation within the circuit [165, 166] can be expressed as follows:

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{\mathrm{d}\vec{\Gamma}}{\mathrm{d}t}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{\mathrm{d}\vec{\lambda}}{\mathrm{d}t}\right] = P_1 + P_2 \tag{5.4}$$

In this context, $\hbar$ is the reduced Planck constant, $\vec{\lambda}$ signifies the coherence vector and $\vec{\Gamma}$ denotes the three-dimensional energy vectors that characterize the state of the QCA cell. P_1 represents the flow of power in and out of the clock as well as the intercell power flow, whereas P_2 denotes the dissipated power.

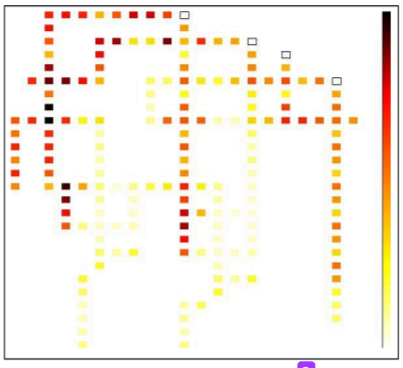


Figure 5.7: Thermal distribution for $E_k = 0.5$ of a 2-bit VM at $T = 2K$

The non-adiabatic upper bound power dissipation model presented in [164], derived from the quasi-adiabatic model by Timler et al. [166], is integrated into the QCAPro software. This model is utilized in our analysis to calculate the leakage, switching, and total energy dissipation of the proposed circuits at $T = 2K$ for different tunneling energies.

Table 5.8: Comparative Leakage Energy Dissipation using QCAPro

Circuits	**0.5**E_k		**1.0**E_k		**1.5**E_k	
	eV	**% per eV**	**eV**	**% per eV**	**eV**	**% per eV**
HA Designs						
[96]	0.0077	30.34	0.0206	24.83	0.0350	25.34
	0.0080	33.37	0.0226	31.51	0.0391	33.3
Proposed	0.0054	-	0.0155	-	0.0261	-
VM Designs						
[71]	0.0689	15.67	0.2008	37.65	0.3515	41.96
Proposed	0.0581	-	0.1251	-	0.204	-

Figure 5.7 illustrates the thermal layout depicting the average energy dissipated in each cell of a 2-bit VM. The darker spots indicate cells that, on average, dissipate

Table 5.9: Comparative Switching Energy Dissipation using QCAPro

Circuits	**0.5E_k**		**1.0E_k**		**1.5E_k**	
	eV	**% per eV**	**eV**	**% per eV**	**eV**	**% per eV**
HA Designs						
[96]	0.0214	1.68	0.0194	0.78	0.0167	2.82
[104]	0.0213	1.22	0.0193	0.62	0.0166	2.64
Proposed	0.0210	-	0.0192	-	0.0162	-
VM Designs						
[71]	0.1551	3.99	0.1332	5.33	0.1125	6.93
Proposed	0.149	-	0.1261	-	0.104	-

a larger amount of energy. The layout was obtained through simulations covering all possible input switching combinations for $E_k = 0.5$. The energy dissipation per cell scaled in units of 10^{-3} eV.

Table 5.10: Comparative Total Energy Dissipation using QCAPro

Circuits	**0.5E_k**		**1.0E_k**		**1.5E_k**	
	eV	**% per eV**	**eV**	**% per eV**	**eV**	**% per eV**
HA Designs						
[96]	0.0291	9.26	0.0400	13.18	0.0516	18.07
[104]	0.0293	10.03	0.0420	17.28	0.0558	24.15
Proposed	0.0264	-	0.0347	-	0.0423	-
VM Designs						
[71]	0.2241	7.54	0.334	24.79	0.464	33.47
Proposed	0.2071	-	0.2512	-	0.3086	-

Tables 5.8, 5.9, 5.10 provides the comparative average, switching, and leakage analyses of energy dissipation for the suggested designs with the recent reported designs, under the assumption that all QCA cells exhibit uniform power consumption. In these computations, three distinct tunneling energy values: 0.5 E_k, 1.0 E_k, and 1.5 E_k are utilized, while maintaining the standard QCA operational temperature at $2K$ for analysis. The percentage per eV unit (denoted as % per eV) in the table represents the corresponding decrease in energy dissipation of the suggested circuits when compared to the reference designs. The consistent improvement of the proposed designs across varying tunneling energy levels further reinforces the potential of the circuits in achieving efficient and sustainable computational processes.

The evaluation of the proposed design metrics is also done by using the QCADesigner-E (QDE) tool [167]. The percentage per eV unit (denoted as % per eV) in the table

Table 5.11: Comparative energy dissipation analysis using QCADesigner-E

Circuits	Avg_Ebath (AED)	% per eV	Sum_Ebath (TED)	% per eV
HA designs				
[96]	1.03e-003 eV (Error: -1.04e-004 eV)	14.56	1.14e-002 eV (Error:-1.15e-003 eV)	14.56
[104]	1.64 e-003 eV (Error: -1.77 e-004 eV)	46.3	1.80e-002 eV (Error:-1.95 e-003 eV)	46.3
Proposed	0.88 e-003 eV (Error: -0.85 e-004 eV)	-	9.77e-003 (Error: -9.43e-003 eV)	-
2-bit VM designs				
[71]	6.20e-003 eV (Error:-5.47e-004 eV)	11.77	6.83e-002 eV (Error:-6.02e-002 eV)	11.77
[159]	6.28e-003 eV (Error: -)	12.89	6.90e-002 eV (Error: -)	12.75
Proposed	5.47e-003 eV (Error: -4.68e-004 eV)	-	6.02e-002 eV (Error: -5.15e-003 eV)	-

represents the reduction in energy dissipation of the suggested circuits when compared to the reference design. Notably, both the proposed HA and VM designs exhibit significant reductions in total energy dissipation.

Assessment of Temperature on Average Output Polarization: A comprehensive investigation is conducted using the QDE tool to further assess the impact of temperature on the AOP [137] of the 2-bit VM. The output polarization is measured

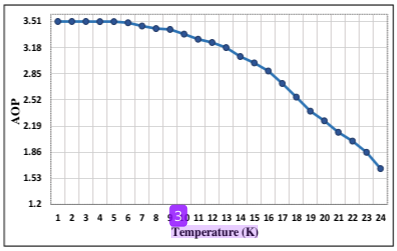


Figure 5.8: Variation in average output polarization (AOP) of 2-bit VM with temperature

at varying temperatures employing the Euler method of CV simulation engine. The results are visually depicted in Figure 5.8 and the following observations are drawn:

- The AOP of the circuits remains relatively stable until 6K. Beyond this point,

the output polarization gradually declines. Hence, as the temperature increases, the AOP decreases. This indicates that the computational fidelity of the circuit decreases with increasing temperature.

- The VM circuit exhibits stable and reliable computation over the low temperature range. This suggests that the circuits is robust to thermal fluctuations.

5.6 Comparative Analysis and Discussion

A comprehensive comparison of different QCA-based multiplier designs, including array [168, 169, 170], matrix[171], Baugh-Wooley [172], Booth [173] and proposed Vedic multiplier is presented. Table 5.12 provides a succinct summary of the performance metrics evaluated across these diverse multiplier architectures reinforcing the efficacy of the proposed VM in digital applications.

Table 5.12: Comparison of different 2-bit QCA multiplier architectures

Multipliers	CC	Latency	Area	Layer
Matrix [171]	7102	20	15.69	Multilayer
Serial [174]	306	8	0.48	Coplanar
Array [169]	1598	7	1.76	Coplanar
Array [168]	493	5	0.72	Coplanar
Array [170]	439	1.75	0.49	Coplanar
Baugh-Wooley [172]	688	3	0.91	Multilayer
Booth [173]	1257	7	-	Coplanar
Proposed VM	**179**	**1.75**	**0.17**	**Coplanar**

The comparative analysis in Table 5.13 highlights the significant advancements of the suggested design against previous approaches, including the most-recent VM by Daggula and Bevara [159], demonstrating careful consideration of trade-offs between speed, area, and complexity in QCA implementation.

Our design achieves a latency of 1.75 clock cycles, outperforming the recent design [159] (3.25 clocks) and matching the best performance of Khan et al. [70] and Premananda et al. [156], while maintaining a reduced cell count of 179 in a single layer. While multi-layer designs like Huang et al. [73] achieve lower cell counts, our single-layer approach offers a more cost-effective fabrication process [69]. This approach optimizes speed without excessive area consumption or fabrication complexity, as evidenced by the total area of 0.17 μm^2, which is considerably smaller than the 0.53

μm^2 reported in [159]. The design's complexity (14) is moderate and matches that of Safoev et al. [71], while being lower than the complexity of 17 in [159]. Notably, our implementation achieve significant improvements in $Cost_{AD}$, FoM, and $Cost_{ED}$ over all compared designs, indicating superior performance-to-resource ratios. These metrics demonstrate that our design effectively navigates the trade-offs inherent in QCA implementation, resulting in a cost and area-efficient multiplier. Additionally, Figure 5.9 shows the percentage improvement made by the suggested VM design in contrast to the recent single layer architectures in various design metrics. Furthermore,

Table 5.13: Comparative Study of Novel 2-Bit VM Design Against Previous Approaches

Parameters	**2-bit VM Designs**							
	[73]	[156]	[76]	[77]	[71]	[70]	[159]	**Proposed**
Layer	Multi	Multi	Single	Single	Single	Single	Single	**Single**
Cell Count	115	291	1683	726	194	135	266	**179**
Latency	1	1.75	15	8.25	2.25	1.75	3.25	**1.75**
Cell Area	0.037	0.0942	0.5452	0.2352	0.062	0.043	0.086	**0.05**
Total Area	0.13	0.4	8.42	2.66	0.17	0.2	0.53	**0.17**
No. of MGs	8	10	10	13	7	4	10	**8**
No. of INVs	0	2	3	9	0	0	3	**2**
No. of CVs	15	9	3	7	7	2	4	**4**
Complexity	23	21	16	29	14	6	17	**14**
$Cost_{AD}$	0.13	1.225	1894.5	181.046	0.8606	0.6125	5.59	**0.52**
FoM	289	560.43	25200	15450	496	61.25	1256.94	**251.1**
$Cost_{ED}$	-	0.255	12.42	11.19	0.059	0.0137	0.729	**0.0111**
Area Utilisation Factor	28.46%	23.55%	6.48%	8.84%	36.47%	21.50%	16.23%	**29.41%**

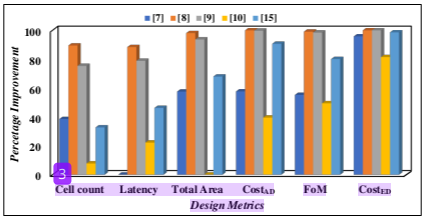


Figure 5.9: Proposed VM vs. Previous Works: Percentage Improvement in Design Metrics

Table 5.14 provides a comparative analysis of 4-bit VM designs against recent state-of-the-art implementations. The results indicate that the proposed design achieves

reductions of 40.07% in cell count, 76.12% in area, 77.63% in latency, and 98.81% in area-to-delay cost compared to the most recent design by [159]. In addition to these

Table 5.14: Comparative study of 4-bit VM against recent approaches

Circuit	**CC**	**Area**	**Latency**	**Cost$_{AD}$**	**Crossover**
[175]	1955	2.55	4.25	46.05938	Multilayer
[77]	15673	74.68	66	325306.1	Coplanar
[71]	1726	1.74	5.25	47.96	Multilayer
[159]	2940	7.33	19	2646.13	Coplanar
Proposed	**1762**	**1.76**	**4.25**	**31.61**	**Multilayer**

quantitative evaluations, it is important to consider practical challenges that arise when scaling QCA circuits. The traditional cost models ($Cost_{AD}$, FoM, and $Cost_{ED}$) as introduced by Liu et al. [69] and used for evaluating the proposed circuits, may not fully account for interconnect complexity, signal degradation, or long-term maintenance costs, particularly in larger circuits [176]. As designs scale, increased wire lengths and interference can reduce signal integrity, requiring repeaters or buffering mechanisms. Likewise, optimized partitioning, placement, and advanced routing become essential to minimize interconnect overhead. Additionally, maintenance costs such as those related to testing and fault diagnosis can be reduced through the implementation of fault-tolerant design architectures. While traditional models offer valuable insights, they could be extended to reflect real-world constraints, including material expenses and design tool limitations. We recognize the importance of these practical considerations and intend to explore them as part of our future research.

5.7 Summary

The realm of nanotechnology has witnessed remarkable advancements in nano-electronics circuits, and QCA technology has emerged as a promising alternative to traditional transistor-based technology. QCA offers significant advantages in terms of lower power consumption and higher speed, making it an attractive choice for future circuit design. In this chapter, an optimized QCA-based half-adder circuit is used for the subsequent creation of a cell-interaction-based co-planar 2-bit Vedic multiplier within the QCA framework, resulting in substantial improvements in circuit metrics such as cell area, quantum cost, and latency. The half adder is further assessed for cell omission and cell deposition defects. It is observed that the sum and carry outputs

show remarkable improvements against single- and double-cell omission and extra cell deposition defect. This comparison underscores the potential efficacy of the HA design in VM circuit. Comprehensive simulations and in-depth performance analysis for various design metrics is performed using the QCADesigner-E v2.2 and QCAPro tool for the suggested circuits. Notably, the proposed design achieves improvements of 22.22% and 81.35% in latency and cost, respectively, with a reduced number of crossovers as compared to the recent single-layer design. Further, the impact of temperature on the average output polarization is presented for the 2-bit VM design. In general, the proposed two-bit Vedic multiplier based on cell interaction demonstrates the potential of QCA technology for efficient and high-performance circuit design. Future research can explore integrating this high-performance, low-power multiplier unit into arithmetic and logic units (ALUs) and multiply-accumulate (MAC) units for signal and image processing systems in mobile devices, where energy efficiency and real-time processing are crucial.

Chapter 6

To develop a novel hybrid reversible Vedic multiplier in Quantum Cellular Automata technology

6.1 Introduction

Quantum-Dot Cellular Automata has emerged as a promising nanotechnology for designing high-performance digital circuits, offering ultra-compact layouts, low power dissipation, and fast switching speeds in the terahertz range. However, conventional irreversible circuits inherently dissipate energy due to information loss, as described by Landauer's principle, which quantifies heat dissipation at $K_bT \ln 2$ joules per bit [177]. Reversible logic overcomes this limitation by ensuring a one-to-one mapping between inputs and outputs, thereby enabling theoretically zero energy loss, as demonstrated in Bennett's foundational work [178]. Reversible logic circuits are particularly suitable for quantum computing and energy-efficient nano-electronics, as they prohibit fan-out and feedback while supporting bijective function mappings [179], as illustrated in Figure 6.1. This chapter focuses on the QCA-based implementation and optimization of two universal reversible logic gates: the 3×3 Peres gate and the 4×4 BME gate—the latter being implemented in QCA for the first time. Each design is evaluated for quantum cost, energy dissipation, and layout efficiency using QCADesigner-E. Furthermore, the application of these gates in Vedic multiplier designs is explored to highlight their practical utility in low-power arithmetic circuits.

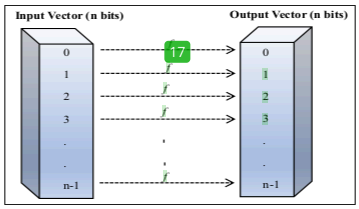


Figure 6.1: Bijective Function Mapping: Maintaining One-to-One Relationships

6.2 Reversible Logic Fundamentals

6.2.1 Quantum bits

In classical computing and information theory, a bit is the building block representing a 0 or a 1. Similarly, the realm of quantum computing and information is constructed upon an analogous concept known as the quantum bit or qubit (the quantum equivalent of a bit) as shown in Figure 6.2. The fundamental difference between a classical

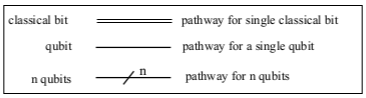


Figure 6.2: Wire illustrations of classical and quantum bits

bit and a qubit lies in their nature and capabilities. A classical bit assumes one of two possible states: either 0 or 1, representing off/on, false/true, or low/high. In contrast, a qubit also exists in its distinctive state. These states are symbolized by $0>$ and $1>$, representing the classical 0 and 1. This notation, such as '>', is known as Dirac notation. The quantum states $0>$ and $1>$ are called basis states, as they span a two-dimensional vector space used to describe qubits [180]. A qubit can hold not only 0 or 1 but also a linear combination of the fundamental states. This implies that a qubit can be in a combination of 0 and 1 states simultaneously until measured, offering a unique feature not present in classical bits. Additionally, qubits can exploit quantum phenomena like superposition and entanglement, allowing them to represent and manipulate more information than classical bits and perform parallel operations on multiple qubits at once. While classical bits operate based on logical gates like AND, OR, and NOT, qubits utilize quantum logic gates for computation. Quantum bits are faster than classical bits and can solve complex problems more efficiently due to their quantum nature and ability to explore multiple solutions simultaneously [178]. A single qubit can be characterized as follows:

$$\psi = \alpha 0> + \beta 1> \quad \alpha^2 + \beta^2 = 1 \tag{6.1}$$

where α and β are the probability amplitudes.

6.2.2 Reversible Design Primitives

- *Gate Count (NG):* The number of RLGs used to realize the function.
- *Ancillary Inputs (CI):* They are constant inputs added to provide supplementary control or state information in a circuit. Although useful, they tend to raise the gate count, complexity, and implementation cost [178]. Thus, designers must manage a trade-off between achieving reversibility and minimizing overhead from ancilla inputs.
- *Garbage Output (GO):* Reversible circuits, due to their bijective property, produce additional output bits termed garbage outputs (GO) that do not contribute to the final result and can be discarded [181]. Minimizing GO is crucial in design to optimize resource efficiency, reduce gate complexity, and limit circuit overhead. The relationship between the number of outputs and inputs is expressed by the following equation:

$$Input + CI = Output + GO \tag{6.2}$$

- *Quantum Cost (QC):* Quantum cost quantifies a circuit's complexity based on the cost of its primitive gates. A 1×1 gate has a quantum cost of zero, while any 2×2 gate is assigned a cost of one. The quantum cost for other reversible gates is determined by counting the number of V, V_+, and $CNOT$ gates within their implementation [87]. Here, V denotes the square root of the NOT gate, and V_+ is its Hermitian conjugate [182]. Furthermore, the relations $(V \times V) = (V_+) \times (V_+) = \text{NOT}$ and $V \times V_+ = V_+ \times V = I$ hold, where I represents the identity matrix.
- *Hardware Complexity (HC):* It is determined by the total number of logical operators used in the output expressions. The specific parameters α denotes the number of 2-input XOR gates; β signifies the number of 2-input AND gates; and γ denotes the number of NOT gates in the circuit. Therefore, HC of a circuit can be calculated as:

$$HC = N(\alpha)\alpha + N(\beta)\beta + N(\gamma)\gamma \tag{6.3}$$

where, $N(.)$ is the total number of operators in the circuit.

- *Total Reversible Logic Implementation Cost (TRLIC)*: TRLIC quantifies the efficiency of a reversible circuit design by combining the total number of gates, garbage outputs, constant inputs, and the quantum cost into a single metric.

$$TRLIC = \sum(NG, QC, CI, GO) \tag{6.4}$$

6.2.3 Quantum Computation

Similar to how classical computers utilize electrical circuits with wires and logic gates, quantum computers employ quantum circuits composed of wires and fundamental quantum gates to control and process quantum information. Quantum circuits employ

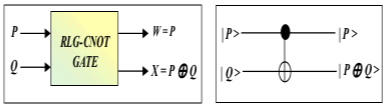


Figure 6.3: The prototypical multiple qubit controlled-NOT gate(RLG-CNOT gate)

quantum gates to implement reversible logic operations. These gates operate on qubits by applying unitary transformations, which are inherently reversible. Common examples include the Controlled-NOT (CNOT) and Toffoli gates, which serve as fundamental components in quantum computing. By combining and controlling such gates, complex reversible quantum circuits can be synthesized. The pivotal multi-qubit quantum CNOT gate features two input qubits: the control qubit and the target qubit [183]. The gate representation; illustrated in the right of Figure 6.3,

Table 6.1: Input–Output Mapping of the 2×2 RLG-CNOT Logic Gate

Inputs		**Outputs**	
P	**Q**	**W**	**X**
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

showcases the control qubit on the top line and the target qubit on the bottom line. The gate's functionality is as follows: when the control qubit is set to 0, the target qubit remains unchanged; however, if the control qubit is set to 1, the target qubit

undergoes a flip operation (Table 6.1). The CNOT gate's behavior can be described as:

$$00 > \longrightarrow 00 >;\ 01 > \longrightarrow 01 >;\ 10 > \longrightarrow 11 >;\ 11 > \longrightarrow 10 > \tag{6.5}$$

The quantum cost of the RLG-CNOT gate is 1 and the hardware complexity can be denoted as:

$$HC_{RLG-CNOT} = 1\alpha \tag{6.6}$$

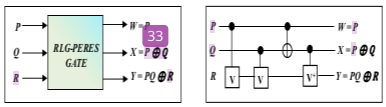


Figure 6.4: Block diagram and Quantum Realisation of RLG-Peres gate

Table 6.2: Input–Output Mapping of the 3 × 3 RLG-Peres Logic Gate

Inputs			Outputs		
P	**Q**	**R**	**W**	**X**	**Y**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Another well-known tripartite reversible gate is the Peres gate (RLG-Peres), also familiar as the new Toffoli gate. Functionally, it is equivalent to a Toffoli Gate followed by a Feynman/CNOT gate. The input vector, I_V = (P, Q, R) and output vector, O_V = ($W = P$, $X = P \oplus Q$, $Y = PQ \oplus R$) for RLG-Peres gate define the gate, with a quantum cost of 4. However, the hardware complexity is defined as :

$$HC_{RLG-Peres} = 2\alpha + 1\beta \tag{6.7}$$

Figure 6.4 illustrates both the block diagram and the quantum circuit model of the RLG-Peres gate. Table 6.2 lists the truth table that captures its logical behavior. In addition, the block diagram of the 4 × 4 reversible logic gate known as the BME gate [184] is presented in Figure 6.5, while Table 6.3 presents its corresponding truth

table. The gate uses an input vector $I_V = (P, Q, R, S)$ and produces an output vector $O_V = (W, X, Y, Z)$, with the outputs defined as $W = P$, $X = PQ \oplus R$, $Y = PS \oplus R$ and $Z = \overline{P}Q \oplus R \oplus S$ [184]. The quantum cost associated with the BME gate is determined to be 5 [185], and the hardware complexity can be calculated as:

$$HC_{BME} = 4\alpha + 3\beta + 1\gamma \tag{6.8}$$

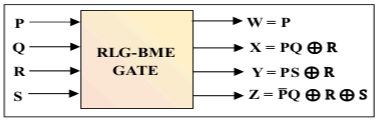


Figure 6.5: Block diagram of RLG-BME gate

Table 6.3: Input–Output Mapping of 4×4 RLG-BME gate

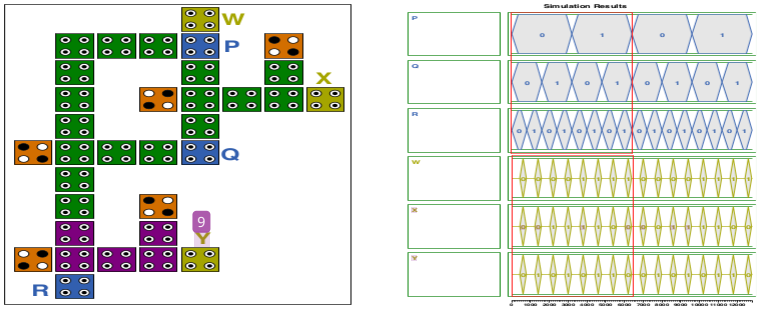
Inputs				Outputs			
P	**Q**	**R**	**S**	**W**	**X**	**Y**	**Z**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	0
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	0
1	1	0	1	1	1	1	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	0	0

6.3 Proposed Innovative Approaches to Vedic Multiplier Implementation

The subsequent section introduces novel architectures designed to implement Vedic multiplier circuits utilizing bijective algorithms within the RLG-based QCA framework. The simulation and verification of the truth tables of the suggested reversible gates is done using the CV simulation engine in the QCA Designer-E v2.2 software [85] initiated with 500000 samples and the cell size of 18*18 nm^2.

6.3.1 RLG-Peres Implementation

The proposed RLG-Peres gate implementation (Figure 6.6(a)) strategically utilizes 33 QCA normal cells to avoid closed input/output loops with 0.5 clock cycle delay. The verified simulation results of the RLG-Peres gate can be observed in Figure 6.6(b).

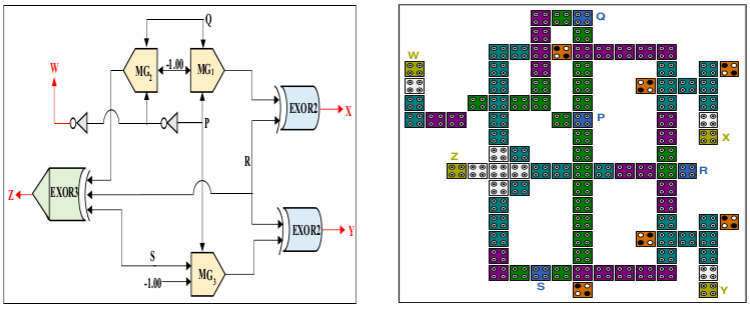


(a) QCA implementation (b) Simulation waveform

Figure 6.6: Proposed RLG-Peres gate

6.3.2 RLG-BME Implementation

The suggested implementation strategy for the RLG-BME gate is depicted in the block diagram provided in Figure 6.7(a). It features four inputs, P, Q, R, and S, and four outputs, W, X, Y, and Z, represented using red labels. The design incorporates three majority gates, two inverters, two 2-input EXOR gates represented as EXOR2 and one 3-input EXOR gate represented as EXOR3. Subsequently, Figure 6.7(b)



(a) QCA Architecture (b) QCA implementation

Figure 6.7: Proposed RLG-BME gate

showcases the proposed QCA architecture of the BME gate. This circuit, featuring 98 cell counts and an area of 0.12 μm^2, operates with just one clock cycle latency. The suggested RLG-BME circuit is implemented as a co-planar circuit, utilizing logical cross-wiring for crossovers. The results from the verified simulation of the RLG-BME gate are presented in Figure 6.8.

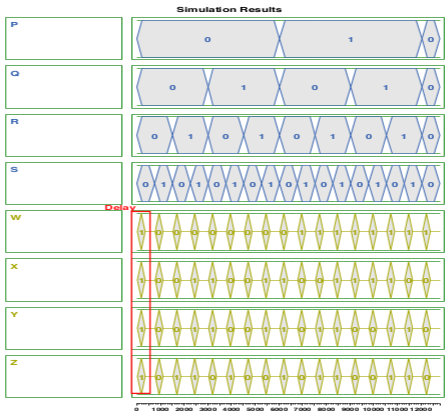
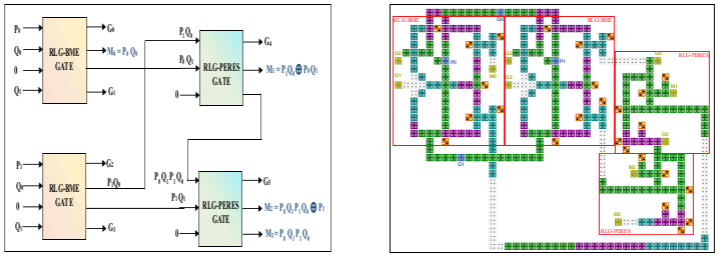


Figure 6.8: Verification of RLG-BME gate

6.3.3 Reversible 2-bits Vedic Multiplier (RVM1) Implementation

The reversible gates based approach for implementing 2×2 VM is presented in Figure 6.9(a). The suggested module takes two inputs, $PandQ : P_1P_0, Q_1Q_0$, and provide a 4-bit output $M[3:0]$ (as shown in blue) based on the UT sutra of VM.
The QCA based implementation of this RVM1 design (as presented in Figure 6.9(b))



(a) Block diagram (b) QCA Implementation

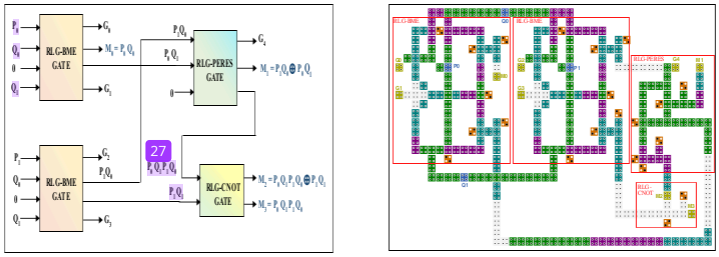
Figure 6.9: Proposed RVM module-1

incorporates four ancillary inputs and utilizes two RLG-BME and two RLG-Peres gates to obtain the final product of 2-bit VM. This suggested module generates six garbage outputs.

6.3.4 Optimized Reversible 2-bits Vedic Multiplier (RVM2) Implementation

The above-mentioned 2-bit Vedic reversible multiplier (RVM1) can be further optimized.

The QCA implementation of this optimized co-planar design (RVM2) utilizes two RLG-BME gates, one RLG-Peres gate, and one RLG-CNOT gate. This optimization reduces the number of ancillary inputs to 3 and garbage outputs to 5. The block diagram and circuit layout of RVM2 are depicted in Figure 6.10(a) and Figure 6.10(b) respectively. Figure 6.11 displays the validated simulation waveform corresponding to the novel Vedic modules RVM1 and RVM2.



(a) Block diagram (b) QCA Implementation

Figure 6.10: Proposed RVM module-1

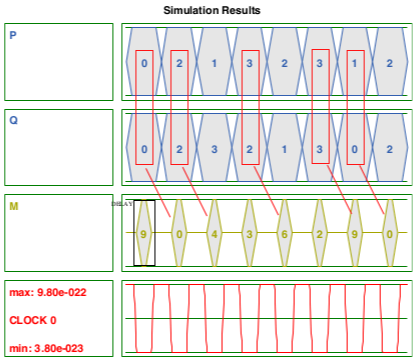


Figure 6.11: Verification of the proposed RVM1 and RVM2 module

6.4 Comparative Analysis

This section provides a holistic comparison of the structural analysis with the recent state of the art in various performance metrics. Additionally, the power dissipation maps and energy dissipation of the circuits are tabulated for a detailed analysis.

6.4.1 Performance and Structural Analysis

The proposed reversible gates are evaluated against recent QCA designs across various design metrics, as shown in Table 6.4.

Table 6.4: Comparative analysis of the reversible gates with recent state-of-the-art designs

Circuits	Cell Count	Area (μm^2)	Latency (ns)	Cost_{AD}	Crossover
RLG-Peres					
[186]	136	0.175	2.5	1.09375	Co-planar
[187]	51	0.049	0.75	0.027563	Co-planar
[188]	44	0.043	0.75	0.024188	Not Required
[189]	56	0.066	0.75	0.037125	Not Required
[190]	79	0.083	1.25	0.129688	Not Required
Proposed	**35**	**0.034**	**0.5**	**0.0085**	**Not Required**
RLG-BME					
Proposed	**98**	**0.12**	**1**	**0.12**	**Co-planar**
Proposed RVM					
RVM1	**371**	**0.44**	**2**	**1.76**	**Co-planar**
RVM2	**338**	**0.39**	**2**	**1.56**	**Co-planar**

The results clearly demonstrate that the proposed circuits excel in all metrics, including cell count, area, latency, and area-to-delay cost (Cost_{AD}) of QCA circuits.

Table 6.5: Comparison of the design primitives of 2-bit reversible multipliers

Module	NG	CI	GO	QC	HC	TRLIC
[191]	4	6	8	16	$6\alpha + 8\beta + 4\gamma$	34
[192]	6	6	6	20	NM	38
[193]	6	4	4	46	NM	60
[194]	6	5	5	22	$10\alpha + 5\beta + 0\gamma$	38
[195]	6	5	9	21	$11\alpha + 5\beta + 0\gamma$	41
Proposed RVM1	**4**	**5**	**6**	**18**	$12\alpha + 8\beta + 2\gamma$	**33**
Proposed RVM2	**4**	**3**	**5**	**15**	$11\alpha + 7\beta + 2\gamma$	**27**

NM: Not mentioned in the original source

The following observations can be concluded:

- The proposed RLG-Peres gate encompasses 35 QCA standard cells presenting a 68.75% improvement over 112 cells in the design by Das et al. [186], 31.37% improvement compared to the 51 cells in the design by Vahabi et al. [187], and a 20.45% improvement compared to the 44 cells in the most recent design by Patidar et al. [188].
- The area occupied by the proposed RLG-Peres gate is 0.034 μm^2, representing a significant 80.57% reduction compared to the 0.175 μm^2 area in the design

by Das et al. [186], 30.61% reduction from the 0.049 μm^2 reported by Vahabi et al. [187], and a 20.93% reduction from the 0.043 μm^2 reported by Patidar et al. [188].

- The latency of the proposed RLG-Peres gate is 0.5 clock cycles, which is a 33.33% improvement over the 0.75 latency in the designs reported in [187], [188] and [189].
- The Cost_{AD} of the proposed RLG-Peres gate is 0.0085, demonstrating a significant 99.22% improvement compared to [186], an impressive 69.16% improvement from [187], and a notable 64.84% improvement from [188].
- The suggested QCA design of the RLG-BME gate is built using co-planar crossover for efficient design integration, achieving minimal cell usage and latency with a Cost_{AD} of 0.12.
- The proposed RVM2 design shows substantial improvements over RVM1, with $\sim$ 9% reduction in cell count and $\sim$ 11.4% reduction in area usage, and $Cost_{AD}$ with the same latency of 2 clock cycle.

Further, Table 6.5 presents a comparative analysis of VM2 against previously reported designs [191, 192, 193, 194, 195] in terms of design primitives for 2-bit reversible multipliers. RVM2 demonstrates significant advantages over both RVM1 and the referenced designs. Specifically, RVM2 simplifies the design, requiring fewer resources for implementation and achieves reductions of 40%, 16.7%, and 18.2% in CI, QC, and TRLIC, respectively, compared to RVM1, indicating enhanced computational efficiency and optimization. Compared to [191], RVM2 requires 20% fewer CI and achieves a 16.7% reduction in QC. Additionally, RVM2 outperforms [191], [192], and [193] with improvements of 20.6%, 28.9%, and 55% in TRLIC, respectively, highlighting its superior efficiency and performance in 2-bit reversible multiplier designs.

6.4.2 Energy and Power Dissipation Analysis

The energy dissipation results for the utilized RLG gates were calculated using the 'coherence vector with energy' simulation engine in QCADesigner-E software version 2.2 [85].

Table 6.6: Energy and power dissipation analysis of the proposed reversible circuits using QCADesigner-E v2.2

Proposed Circuits	**TED(eV) (Sum_Ebath)**	**AED(eV) (Avg_Ebath)**	**P_d (W)**	**PDP (Ws)**
RLG-CNOT	6.97e-003 (Error: +/- -7.38e-004)	6.34e-004 (Error: +/- -6.71e-005)	1.12×10^{-9}	1.12×10^{-21}
RLG-Peres	3.10e-002 (Error: +/- -3.23e-003)	2.82e-003 (Error: +/- -2.94e-004)	2.49×10^{-9}	4.98×10^{-21}
RLG-BME	5.30e-002 (Error: +/- -5.27e-003)	4.81e-003 (Error: +/- -4.79e-004)	2.13×10^{-9}	8.52×10^{-21}
RVM1	1.19e-001 (Error: +/- -0.96e-002)	1.08e-002 (Error: +/- -1.01e-003)	2.39×10^{-9}	1.91×10^{-20}
RVM2	0.98e-001 (Error: +/- -0.89e-002)	0.87e-002 (Error: +/- -0.79e-003)	1.96×10^{-9}	1.57×10^{-20}

Table 6.7: Energy dissipation analysis of the proposed reversible circuits across three distinct tunneling energies at $T = 2K$ using QCAPro

RLG Circuits	**Leakage ED (meV)**			**Switching ED (meV)**			**Total ED (meV)**		
	0.5 E_k	**1.0 E_k**	**1.5 E_k**	**0.5 E_k**	**1.0 E_k**	**1.5 E_k**	**0.5 E_k**	**1.0 E_k**	**1.5 E_k**
CNOT [187]	3.16	8.71	14.79	8.90	7.45	6.26	12.06	16.16	21.05
Peres	10.92	27.15	45.33	39.55	21.42	18.83	50.47	48.57	64.16
BME	34.89	98.85	170.6	115.26	96.01	79.72	150.15	194.9	250.29
RVM1	106.3	212.3	342.7	485.6	398.8	319.01	591.9	611.1	661.71
RVM2	91.8	201.7	314.2	404.8	311.8	281.4	496.6	513.5	595.6

As it is evident from the table that the TED of the RLG-CNOT gate is $6.97 \times 10^{-3} eV$, with each electron charge being $1.607 \times 10^{-19} Joules$. Therefore,

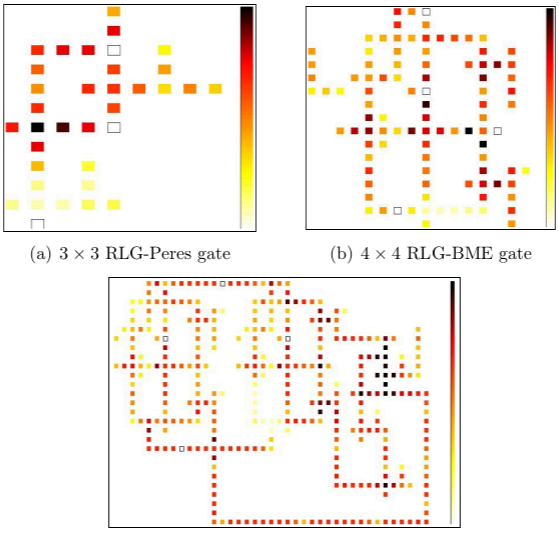
$$TED = 6.97 \times 10^{-3} \times 1.607 \times 10^{-19} = 11.20679 \times 10^{-22} Joules \tag{6.9}$$

Further, it is seen that the latency of RLG-CNOT is 0.25 clock cycles, and each clock cycle has a clock period of $4 \times 10^{-12} sec$. Hence, the total time delay can be represented as:

$$D = 0.25 \times 4 \times 10^{-12} = 1 \times 10^{-12} sec \tag{6.10}$$

Finally, the power dissipation (P_d) can be calculated as:

$$P_d = \frac{TED}{D} = \frac{11.20679 \times 10^{-22}}{1 \times 10^{-12}} = 1.120679 nW \tag{6.11}$$



(a) 3×3 RLG-Peres gate (b) 4×4 RLG-BME gate

(c) 2×2 RVM2

Figure 6.12: Power Dissipation Map of the proposed reversible gates for $0.5E_k$

Additionally, the power delay product evaluation criterion (PDP), based on [196] is illustrated in Table 6.6. The standard theoretical clock frequency of 1 THz is considered. The PDP can be represented in Ws as shown below:

$$PDP = Power(W) \times Delay(s) \tag{6.12}$$

Henceforth, Table 6.6 also showcases the power dissipation (P_d) and PDP values for the proposed reversible circuits. It reveals that RVM2 achieves a notable 17.9% reduction in P_d and PDP compared to RVM1. Based on the upper bound energy dissipation model [86], the QCAPro software is further utilized to assess the power consumption of QCA reversible gates by examining three distinct tunneling energies of $0.5E_k$, $1.0E_k$ and $1.5E_k$ between the dots with the standard operational temperature for QCA energy analysis set at $2K$. The thermal hotspots of the suggested QCA implementations for the RLG-Peres and RLG-BME gates at $0.5E_k$ are visualized in Figure 6.12(a) and Figure 6.12(b), respectively. Additionally, Figure 6.12(c)

illustrates the power dissipation map of RVM2 at $0.5E_k$. The power analysis, detailed in Table 6.7, measures the average, leakage, and switching energy dissipation for the proposed efficient reversible gates across all vector pairs. It highlights that RVM2 achieves reductions in energy dissipation compared to RVM1, with percentages of 16.1%, 16%, and 10% at tunneling energies of of $0.5E_k$, $1.0E_k$ and $1.5E_k$ respectively.

6.5 Summary

This chapter presents efficient designs of Vedic multipliers in QCA technology using reversible logic gates. The proposed reversible multipliers, RVM1 and RVM2, have been implemented based on the optimized QCA designs of reversible Peres and BME gates designed and simulated using the QCADesigner-E v2.2 tool. The simulation results reveal that RVM2, in particular, achieves significant reductions in ancillary inputs, quantum cost, and total reversible logic implementation cost compared to RVM1, demonstrating enhanced computational efficiency. Holistic energy and power dissipation analyses are conducted using QCADesigner-E and QCAPro tools, indicating that the proposed designs dissipate minimal energy. Notably, RVM2 shows substantial improvements in power dissipation and power-delay product compared to RVM1, highlighting its superior efficiency. The simplicity and effectiveness of the proposed co-planar designs make them highly reliable suitable for integration into various arithmetic logic units. These findings underscore the potential of integrating reversible logic with QCA technology to advance digital circuit design, enabling ultra-low power and high-speed computational circuits at the nano-scale.

Chapter 7

Conclusion, Future Scope and Social Impact

7.1 Conclusion

This thesis presents a comprehensive investigation into the design, implementation, and optimization of Vedic multipliers using Quantum-Dot Cellular Automata (QCA) technology. Based on a detailed review and analysis of various n-bit Vedic multiplier implementations across multiple technologies (ranging from 2 to 64 bits), the study highlights QCA as a promising alternative to the conventional CMOS technology, offering notable reductions in power consumption, propagation delay, and circuit area; positioning it as an ideal candidate for future nanoelectronic systems.

The initial phase of this research focused on implementing Vedic multipliers using CMOS technology. A novel 4-bit Vedic multiplier architecture was proposed, incorporating a customized 5-bit adder along with conventional full and half adders to optimize performance. This foundational design served as a baseline for evaluating computational efficiency and was subsequently scaled to an 8-bit implementation using modular 4-bit units and ripple carry adders. Simulation results for the extended design demonstrated significant improvements in terms of transistor count, energy-delay product (EDP), and power-delay product (PDP). Additionally, temperature-dependent analysis revealed average energy savings of 28.8% and 16.7% for the 4-bit and 8-bit designs, respectively, compared to traditional CMOS-based approaches.

Building on the insights gained from CMOS-based implementations, the research shifted focus toward exploring the potential of Quantum-Dot Cellular Automata technology for designing energy-efficient arithmetic circuits. In this phase, optimized layouts for half and full adder circuits were developed using coplanar QCA configurations, emphasizing simplicity, compactness, and reduced complexity. These designs formed the basis for constructing scalable Ripple Carry Adders (RCAs) and Carry Save Adders (CSAs), both of which demonstrated superior performance over existing designs in terms of layout cost, quantum cost, and energy efficiency. The effectiveness and reliability of these circuits were further validated through energy dissipation analysis using QCADesigner-E and QCAPro tools under various operating conditions.

To further enhance performance and address interconnect limitations, a multilayer crossover strategy was adopted for the implementation of high-performance RCA circuits. This approach significantly reduced area and routing complexity, while maintaining excellent functionality across different QCA cell sizes ranging from 14×14 nm to 18×18 nm. Moreover, thermal analysis based on average output polarization confirmed the robustness of these designs under varying temperature conditions, demonstrating their suitability for thermally constrained environments.

Leveraging the optimized coplanar half adder design, a fault-tolerant 2-bit Vedic multiplier was also developed. The proposed architecture exhibited strong resilience against fabrication-related faults such as single and double cell omission and deposition defects. Notably, the design achieved substantial reductions in quantum cost (81.35%) and latency (22.22%) compared to recent single-layer implementations, highlighting its practical viability.

In the final stage of this research, reversible logic was introduced into the QCA framework to further push the boundaries of low-power computation. Two Vedic multiplier architectures (RVM1 and RVM2) were constructed using newly proposed QCA layouts of reversible Peres and BME gates. Among these, RVM2 emerged as the more efficient design, offering reduced quantum cost, fewer ancillary inputs, and lower overall implementation complexity. Holistic simulation results confirmed RVM2's minimal energy dissipation and favorable power-delay product, underscoring the benefits of combining QCA with reversible logic for ultra-low power arithmetic design.

A particularly significant outcome of this study is the dramatic improvement in power-delay performance across technological transitions. The 2-bit Vedic multiplier implemented in CMOS exhibited a PDP of $1.28 \times 10^{-15} W$. When redesigned using QCA, the PDP was reduced to $9.674 \times 10^{-21} W$; an improvement of nearly six orders of magnitude. Taking this further, the introduction of reversible logic within the QCA framework lowered the PDP to $1.57 \times 10^{-20} W$. This progressive enhancement powerfully illustrates the transformative potential of combining Vedic mathematics with QCA and reversible logic, not only in terms of raw performance but also in achieving energy-efficient, sustainable circuit design.

The collective results and innovations from the individual chapters presented in this thesis affirm the viability of QCA-based Vedic multipliers as a next-generation solution for low-power, high-speed digital arithmetic. The integration of architectural,

physical, and fault-tolerant design techniques has produced a foundation that is not only theoretically compelling but also practically scalable for diverse nanoelectronic applications.

7.2 Future Work and Social Impact

Building on the foundations established in this thesis, several promising directions emerge for future exploration. Vedic multipliers, owing to their inherent efficiency and modular structure, hold strong potential in the development of advanced arithmetic processors such as ALUs, MACs, GPUs, and ASICs, where fast and power-efficient multiplication units are essential. Their integration into cryptographic systems could significantly accelerate core operations in encryption, hashing, and digital signature algorithms, thereby improving the speed and security of modern communication protocols. The biomedical domain also stands to benefit from Vedic multiplier implementations. Applications such as ECG, EEG, and medical image processing demand real-time or near-real-time performance, and VMs can deliver enhanced throughput and reduced latency for such computations. Additionally, low-power Vedic multipliers are particularly well-suited for Internet of Things (IoT) devices, where minimizing energy consumption is critical for extending device lifetime and enabling sustainable deployment. Future work can also explore the design of scalable and

Table 7.1: Versatile applications of Vedic multipliers in various fields

Domain	References	Explanation
Cryptography	[197, 198, 199, 200]	The computational efficiency of elliptic curve cryptography by accelerating key generation, scalar multiplication, and point operations. The execution speed of symmetric encryption algorithms like AES and DES is improved, and digital signature schemes such as RSA and DSA are optimized, strengthening the performance and security of modern cryptographic systems.
DSP	[201, 202, 203, 204, 205, 206, 207, 208, 209, 210]	VMs enhance image and signal processing by accelerating DWT-based decomposition for tasks like compression and feature extraction, optimizing convolution and FIR filter performance in DSP, and enabling faster FFT-based frequency analysis.
ALU	[39, 211, 212, 213, 214, 215, 216]	The performance is enhanced by VM in complex arithmetic and matrix operations due to improvement in speed and accuracy of floating-point computations.
MAC unit	[217, 218, 219, 220]	Vedic multipliers improve the efficiency of MAC units by accelerating multiplication and accumulation tasks in scientific simulations, numerical algorithms, and large-scale computations.
Biomedical	[201, 208, 221, 222, 223]	The processing of biomedical signals like ECG, EEG, and EMG is enhanced by efficiently performing tasks such as filtering and feature extraction, enabling real-time analysis and improvement in speed of complex simulations.

reconfigurable Vedic multiplier architectures that support large bit-width operations and adaptive functionality. This includes fault-tolerant designs, reversible computing implementations, and integration into AI accelerators and real-time signal processing pipelines. Such advancements would strengthen the applicability of QCA-based arithmetic units in both high-performance and energy-constrained environments. From a broader societal perspective, Vedic multiplier implementations contribute to technological domains with tangible real-world impact. They offer performance gains in digital signal processing, cryptography, high-speed computing, and biomedical electronics—domains critical to healthcare, communication, security, and scientific research. As highlighted in Table 7.1, the versatility of Vedic multipliers extends from image compression and data encryption to real-time signal analysis and large-scale simulations. By improving computational speed, reducing power consumption, and enabling compact and fault-resilient designs, this research supports the growing need for sustainable, efficient, and scalable hardware systems across multiple sectors.

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List of Publications

SCI/SCIE Journals (Accepted and published):

1. **Hemanshi Chugh** and Sonal Singh (2025). An energy and cost-effective realization of high-performance single-layer vedic multiplier in quantum-dot cellular automata, Physica Scripta, 100, 065112. (IOP Publishing, Impact Factor 2.6)

2. **Hemanshi Chugh** and Sonal Singh (2024). Systematic exploration of N-Bit Vedic multipliers: A roadmap of technological approaches in pursuit of future trends. Nano Communication Networks, 100529. (Elsevier, Impact Factor 2.9)

3. **Hemanshi Chugh** and Sonal Singh (2024). Efficient co-planar adder designs in quantum dot cellular automata: Energy and cost optimization with crossover elimination, Integration, 94, p.102103. (Elsevier, Impact Factor 2.2)

4. **Hemanshi Chugh** and Sonal Singh (2024). Efficient quantum-dot adder optimization and analysis for future circuits", International Journal of Electronics, pp 1-21. (Taylor & Francis, Impact Factor 1.2)

IEEE International Conferences

1. **Hemanshi Chugh**, and Sonal Singh, "Design and implementation of a high-performance 4-bit Vedic multiplier using a novel 5-bit adder in 90 nm technology" in 2022 10th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions)(ICRITO), 2022, pp. 1-6, IEEE.

2. **Hemanshi Chugh**, and Sonal Singh, "Parametrical analysis and thermal sensitivity study of 8-bit Vedic multiplier", In 2023 14th International Conference on Computing Communication and Networking Technologies (ICCCNT), 2023, pp. 1-6, IEEE.

Extended Work: SCI/SCIE Journals (Communicated/under review)

1. Robust Coplanar Designs of Reversible Peres and BME Gate in QCA Framework for Highly Efficient Vedic Multiplier Implementations, Physica Scripta, (2025). (Under Review) (IOP Publishing, SCI-E indexing, IF 2.6)

2. Thermally Stable and Cost-Efficient QCA-Based Co-Planar Design of a 4-Bit CSA with Optimized Cell Size Scaling, Analog Integrated Circuits and Signal Processing, (2025). (Under Review) (Springer, SCIE indexing, IF 1.4)

HEMANSHI CHUGH

SENIOR RESEARCH SCHOLAR
DELHI TECHNOLOGICAL UNIVERSITY (DTU)



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RESEARCH AREAS

- Low Power VLSI Design
- Quantum Dot Cellular Automata

SKILLS

- QCA Tools: QCAD, QCA Pro, QCAD-E
- Cadence Virtuoso
- Modelsim-Altera (Verilog)
- Tanner TSpice
- FPGA

TEACHING DOMAINS

- VLSI Design
- Digital Electronics

PROFILE

Redefining the paradigms of Quantum Computing and Low-Power VLSI, my research drives breakthroughs in nanoscale architectures that pave the way for energy-efficient and scalable computing systems.

Driven by a passion for cutting-edge technologies, I will deliver a research-focused teaching approach that accelerates academic growth and fosters innovation within the university.

EDUCATION

DELHI TECHNOLOGICAL UNIVERSITY 2021 - PRESENT

Ph.D. | Department of Electronics & Communication Engineering

Research Focus: VLSI Circuits, Quantum Dot Cellular Automata (QCA), Nanotechnology, Quantum Computing.

CENTRE FOR DEVELOPMENT OF ADVANCED COMPUTING (CDAC), NOIDA | GGSIPU 2014 - 2016

M.Tech (VLSI Design)| 83.8%

GURU TEGH BAHADUR INSTITUTE OF TECHNOLOGY, DELHI | GGSIPU 2010 - 2014

B.Tech (ECE) | 81.3%

ST. GEORGE'S SCHOOL, DELHI | CBSE

Grade 12 | 81.4% | 2010
Grade 10 | 91.6% | 2008

WORK EXPERIENCE

DR. AKHILESH DAS GUPTA INSTITUTE OF PROFESSIONAL STUDIES, DELHI | GGSIPU 2017-2021

Assistant Professor | ECE

PROJECTS UNDERTAKEN

M.TECH RESEARCH – HARDWARE-CENTRIC FPGA IMPLEMENTATIONS

FPGA-Based Multiplier Design: Design of Vedic, Booth Encoded Wallace Tree, Baugh Wooley, and Braun Multipliers with ripple carry, carry skip and carry select adders using Verilog HDL, and implemented using Xilinx Spartan 3E FPGA. Baugh Wooley excelled in signed operations, while Braun Multiplier with carry skip adder outperformed Vedic for unsigned operations.

FPGA-Based Sensor System for Biomedical Monitoring: Developed an FPGA-based real-time biomedical monitoring system using I2C and UART protocols, enhancing sensor data acquisition and real-time processing.

PH.D. RESEARCH – SOFTWARE-BASED CIRCUIT OPTIMIZATIONS

Technological Shifts in Multiplier Design and Optimization: Systematic analysis of N-bit Vedic multipliers, exploring front-end and back-end implementations highlighting the paradigm shift from CMOS to novel Quantum Dot Cellular Automata (QCA), while providing a classified framework for multiplier applications.

CMOS-Based Vedic Multiplier in Cadence Virtuoso: Design and implementation of high performance n-bit Vedic multiplier in 90nm node technology, with a comprehensive analysis of delay, power, and energy-delay product, followed by a thermal sensitivity study across temperature variations.

Quantum Dot Cellular Automata-based Adders: Energy and cost-efficient design of n-bit ripple carry adder using coplanar and multilayer wire schemes in QCADesigner, enhancing circuit efficiency and layout optimization, followed by the development of an efficient carry save adder in QCA, achieving significant improvements in area efficiency, quantum cost, and propagation delay.

Quantum Dot Cellular Automata-Based Multiplier: Design and evaluation of an N-bit Vedic Multiplier, leveraging optimized QCA-based adders to ensure cost and energy efficiency, followed by comprehensive performance assessment using QCADesigner-E and QCAPro softwares.

QCA-Based Reversible Multiplier: Development of an ultra-low-power reversible QCA multiplier with minimal clock cycle delay, focusing on energy dissipation and computational cost optimization for quantum computing architectures, complemented by extensive energy dissipation and performance analysis using QCADesigner-E and QCAPro.

RESEARCH PUBLICATIONS

JOURNAL ARTICLES

Chugh, Hemanshi, and Sonal Singh. "An Investigation with N-bit Vedic Multipliers: Systematic Literature Review, Classification, and Current Trends." **Nano Communication Networks** (2024): 100529. (Elsevier, Impact Factor 2.9, SCI)

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Chugh, Hemanshi, and Sonal Singh. "Efficient Quantum-Dot Adder Optimization and Analysis for Future Circuits." **International Journal of Electronics** (2024): 1-21. (Taylor & Francis, Impact Factor 1.3, SCIE)

Chugh, Hemanshi, and Sonal Singh. "An Energy and Cost-Effective Realization of High-performance Single-layer Vedic Multiplier in Quantum-Dot Cellular Automata." **Physica Scripta,** 100(6) (2025): 065112. (IOP Science, Impact Factor 2.6, SCIE)

Chugh, Hemanshi, and Sonal Singh. "Thermally Stable and Cost-Efficient QCA-Based Co-Planar Design of a 4-Bit CSA with Optimized Cell Size Scaling", Analog Integrated Circuits and Signal Processing, (2025). (Under Review) (Springer, Impact Factor 1.4, SCIE)

Chugh, Hemanshi, and Sonal Singh. "Robust Coplanar Designs of Reversible Peres and BME Gate in QCA Framework for Highly Efficient Vedic Multiplier Implementations", Physica Scripta, (2025). (Under Review) (IOP Science, Impact Factor 2.6, SCIE)

Payal, Ravi, Udit Kapoor, and Hemanshi Chugh. "Design and Implementation of Speed Efficient Vedic Multiplier using Verilog", **International Journal of Scientific Research and Education** (2015): 4752-4758. (Scopus Indexed)

Chugh, Hemanshi. "Designing various types of multipliers and their implementation on FPGA." **Journal of Emerging Technologies and Innovative Research (JETIR)** (2019): 1066-1070. (Scopus Indexed)

RESEARCH PUBLICATIONS

BOOK CHAPTER | SCI

Chugh, Hemanshi, and Sonal Singh. "Machine learning applications in rational drug discovery." **Drug Design Using Machine Learning** (2022): 97-116. (Wiley Online Library)

CONFERENCES

Chugh, Hemanshi, and Sonal Singh. "Parametrical Analysis and Thermal Sensitivity Study of 8-bit Vedic Multiplier." 2023 14th **International Conference on Computing Communication and Networking Technologies** (ICCCNT). IEEE, 2023.

Chugh, Hemanshi, and Sonal Singh. "Design and Implementation of a High-Performance 4-bit Vedic Multiplier Using a Novel 5-bit Adder in 90nm Technology." 2022 10th **International Conference on Reliability, Infocom Technologies and Optimization** (Trends and Future Directions) (ICRITO). IEEE, 2022

Chugh, Hemanshi. "FPGA Based Sensor System for Bio-Medical Monitoring using I2C and UART Protocol." **National Conference on Electronics, Communication and Computation**, 2020.

REFERENCES

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ORIGINALITY REPORT

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PRIMARY SOURCES

1	Hemanshi Chugh, Sonal Singh. "Systematic exploration of N-Bit Vedic multipliers: A roadmap of technological approaches in pursuit of future trends", Nano Communication Networks, 2024 Publication	10%
2	Hemanshi Chugh, Sonal Singh. "Efficient co-planar adder designs in quantum dot cellular automata: Energy and cost optimization with crossover elimination", Integration, 2024 Publication	8%
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60	Michael T. Niemier, Michael J. Kontz, Peter M. Kogge. "A design of and design tools for a novel quantum dot based microprocessor", Proceedings of the 37th conference on Design automation - DAC '00, 2000 Publication	<1%
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62	Sadulla Shaik, Satish Kanapala, Vallabhuni Vijay, Chandra Shaker Pittala. "Design and performance analysis of low power and energy-efficient vedic multipliers",	<1%

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