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# ML-ASSISTED DESIGN AND OPTIMIZATION OF ANALOG INTEGRATED CIRCUITS

A Thesis Submitted  
in Partial Fulfillment of the Requirements for the  
Degree of

## MASTER OF TECHNOLOGY

in

## VLSI DESIGN AND EMBEDDED SYSTEM

by

**Absar Alam**

24/VLS/27

Under the Supervision of

**Dr. Chhavi Dhiman**



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MAY, 2026

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I, **Absar Alam(24/VLS/27)** student of M.Tech (VLSI Design and Embedded System), hereby certify that the work which is being presented in the thesis entitled “**ML-ASSISTED DESIGN AND OPTIMIZATION OF ANALOG INTEGRATED CIRCUITS**” in partial fulfillment of the requirements for the degree of Master of Technology, submitted in Department of **Electronics and Communication Engineering.**, Delhi Technological University, New Delhi is an authentic record of my own work and not copied from any source without proper citation which is carried out under the supervision of **Dr. Chhavi Dhiman** .

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Dr. Chhavi Dhiman

Department of Electronics and Communication Engineering

Delhi Technological University

Date: May 2026

## ABSTARCT

This thesis proposes a machine-learning assisted framework for process-variation-aware transistor sizing of CMOS current mirrors, based on foundry-accurate Spectre simulations in a 45-nm technology node. The paper addresses a long-standing problem in analog integrated circuit design: the difficulty of systematically optimizing nonlinear circuit blocks, when device parameters, process variations, and design constraints are competing.

Current mirrors are one of the most basic building blocks in analog and mixed-signal systems. They are extensively used in bias generation, current replication, and signal conditioning and their performance directly affects current accuracy, power consumption, compliance voltage and robustness. The design of current mirrors has been based on manual iteration and SPICE simulation. It is a time consuming process and highly dependent on the expertise of the designer. At smaller technology nodes short channel effects, mobility degradation, oxide thickness variation and mismatch become more important and sizing becomes harder.

To tackle this issue, the present work proposes a data-driven approach based on 50,000 simulation points generated through foundry-accurate Spectre simulations with BSIM4.5 device models. The data set includes various transistor sizing parameters, operating conditions, and global process variation parameters such as mobility variation and oxide thickness variation. For prediction of current errors, power consumption, compliance voltage and process-variation sensitivity, supervised ensemble learning models such as Random Forest and Gradient Boosting regressors are used.

The proposed framework shows good prediction accuracy and reveals important dependencies between transistor dimensions and circuit behavior. In particular, the results indicate that features related to width-to-length ratios and output resistance have a significant impact on current accuracy and sensitivity to variations. The machine-learning-guided optimization step finds transistor widths that satisfy design constraints on error, power, and compliance voltage while greatly reducing the iteration time compared to manual SPICE-based exploration.

The thesis presents a reproducible and scalable methodology for analog design automation. It bridges physical circuit simulation and data-driven optimization and demonstrates that machine learning can be a promising aid for robust transistor sizing in advanced CMOS technologies. The results are relevant for research and industrial analog design flows, especially when speed, robustness and accuracy have to be balanced simultaneously..

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# CHAPTER 1

## 1. INTRODUCTION

### 1.1 INTRODUCTION TO ANALOG INTEGRATED CIRCUIT DESIGN

Analog integrated circuit design is one of the most important and technically difficult areas of electronics engineering. It is about circuits that operate on signals that continuously change, and not on discrete logic states. Real physical phenomena such as temperature, pressure, sound, light, chemical concentration and electromagnetic waves produce such signals. Since the physical world is inherently analog, analog circuits are the essential bridge between sensors, transducers, and digital processing systems.

In this age of large-scale digital integration, importance of analog design has not diminished, but increased. While digital computation seems to dominate the modern electronic systems, they still rely heavily on analog components for signal conditioning, data conversion, timing, biasing, power regulation and communication interfaces. Each sensor front-end, audio interface, wireless transceiver, biomedical acquisition system and power management unit contains critical analog blocks that determine the overall functionality and performance of the system.

In contrast, the abstraction and automation in digital circuit design are matured, but analog design is still mainly based on expert judgment, iterative simulation and trial-and-error sizing. This is mainly due to the highly nonlinear behavior of analog circuits and their sensitivity to many interacting variables. Performance can be affected by device dimensions, bias currents, temperature, supply voltage, parasitic capacitances, short-channel effects and manufacturing variations. This leads to a complicated design space that is difficult to explore manually.

Typically, the traditional analog design methodology starts with analytical approximations and then moves to circuit-level simulation. Analytical equations give useful intuition but often do not capture the full behavior of modern CMOS technologies. Second order effects become important due to deep-submicron and nanometer scale processes that are not captured well with simple long-channel models. Therefore, SPICE-class simulators are increasingly used by designers for this accurate evaluation.

However, simulation-based design has a high computational expense for large number of design variables. Many simulations may be needed for each design point candidate to characterize performance under process, voltage, and temperature variations. This is especially difficult when optimization has to take into account not only the nominal operation but also the robustness against process variation. In such cases the number of iterations required can be very large and the design turnaround time is greatly increased.

The increasing complexity of analog design has motivated the use of data driven methods. Machine learning offers a promising avenue for speeding up design exploration by learning the relationship between circuit parameters and performance metrics from simulation data. After training, a machine learning model can predict the behavior of a circuit at unseen design points in a fast manner thus relieving the need for repeated simulation. It changes the design process from a purely manual exploration to a hybrid workflow that combines simulation, prediction and optimization.

This thesis is on one of the most fundamental analog circuits: the CMOS current mirror. Current mirrors are widely used in bias networks and current steering applications, where transistor sizing has a significant impact on performance. Their behavior is sensitive to device parameters and process variation, and gives a meaningful and

practical case study for learning based analog design automation

### ML-Based Transistor Sizing Flow for CMOS Current Mirrors

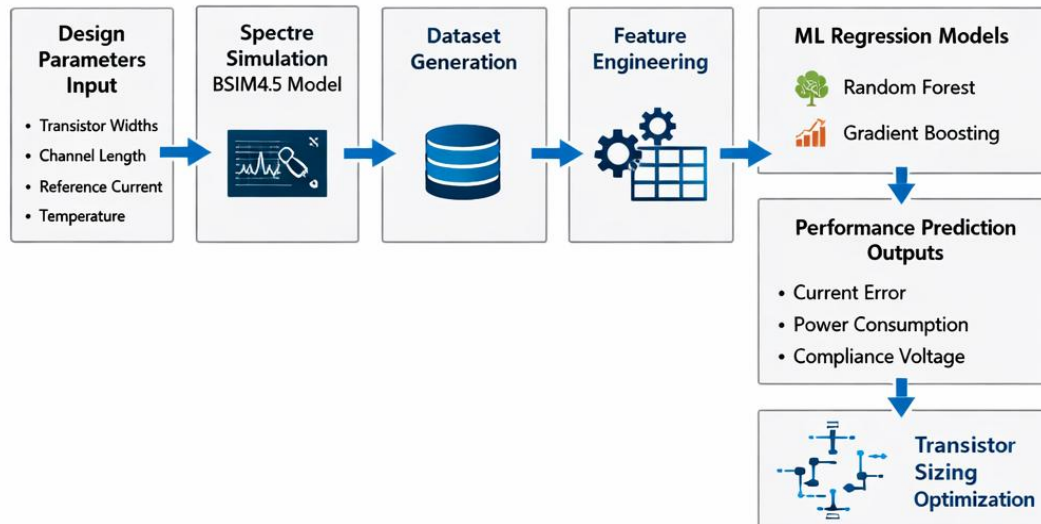


Fig. 1.1: ML-based transistor sizing flow

## 1.2 Background and Motivation

The motivation for this work is the continuing challenge of efficient and robust design of analog circuits in advanced CMOS technologies . When the technology is scaled up, the device behavior deviates more and more from the ideal assumptions. Small parameters that were once considered can become large sources of error. For example, channel length modulation, mobility degradation and oxide thickness variation can affect respectively the ideality of the current source, the transconductance and the electrical characteristics of the transistor. These effects make the analog performance very size sensitive.

Practically, engineers usually start from a nominal design point and then refine it iteratively by hand based on the results of simulation. This procedure may be useful for simple circuits, but quickly becomes inefficient when a number of design objectives must be satisfied at the same time. It is difficult for a designer to

simultaneously reduce the current mismatch, maintain the output compliance, minimize the power, and maintain robustness under variation. In most cases these optimization problems are nonlinear and multi-objective that makes them difficult to solve analytically.

Another important motivation is the increasing demand for design automation in the semiconductor industry. The complexity of modern integrated circuits is ever increasing but design cycles are to become shorter. To satisfy these demands, analog design needs tools that can reduce exploratory effort, with physical accuracy. This is where machine learning becomes interesting, as it can recognize patterns in the simulation data, allow predictions with many variables, and help find potentially good design areas.

This work is also driven by the increasing availability of high-quality simulation data. The modern EDA tools and foundry models enable the creation of huge data sets, which accurately represent the behavior of the real circuit. These datasets can then be used to train predictive models that, in combination with supervised learning techniques, can be used to accelerate design decision making. The main idea of the proposed method is the link between accurate simulation and intelligent learning.

Another motivation is robustness. Design for the nominal operation is not enough anymore in the advanced nodes. Circuits should be able to work reliably even under process variation, mismatch and uncertain operating conditions. A sizing solution that works well only under ideal conditions is of limited practical value. Hence, variation-aware design has been a necessity, particularly for biasing circuits such as current mirrors.

This thesis addresses these challenges by proposing a machine-learning-aided process-variation-aware transistor sizing methodology. The purpose of this method is to maintain the accuracy of the simulation-based analysis with a significant reduction of design time. In this way, it supports the larger goal of enabling intelligent automation in the design of analog ICs.

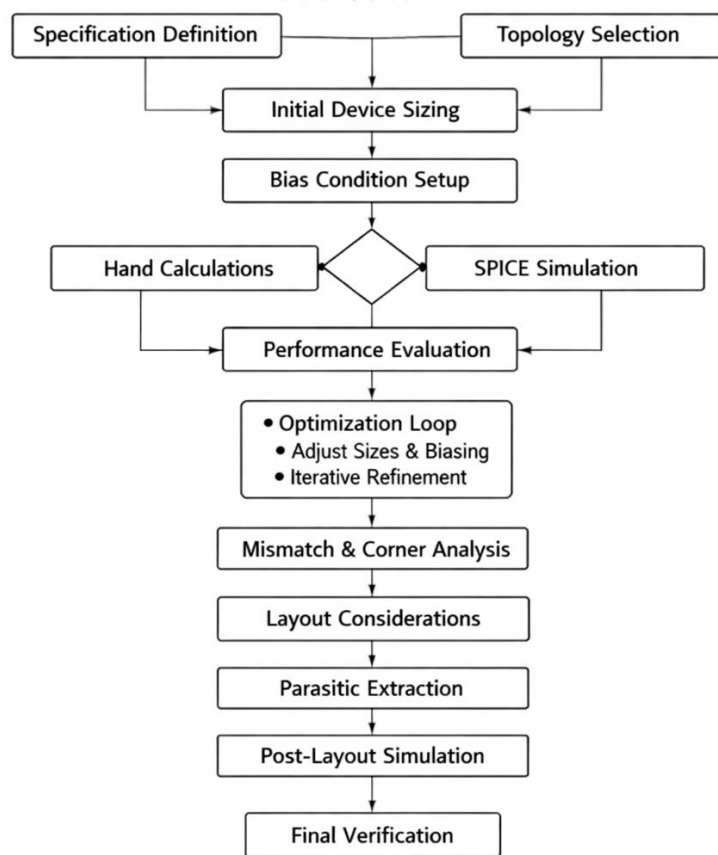


Fig. 1.2: Design and optimization workflow for CMOS current mirrors

### 1.3 CMOS Current Mirrors

A current mirror is a circuit that duplicates a reference current from one branch to another. It is one of the most used building blocks in analog integrated circuit design, as it provides a simple and effective way to bias and replicate the current. Current mirrors are used in operational amplifiers, bandgap references, data converters, differential amplifiers, current steering circuits and many other analog and mixed signal blocks.

The simplest current mirror consists of two matched transistors. One of the transistors is used to set up the reference current and the other transistor copies that current at the output. In an ideal case the output current equals to the reference current. In practice, however, the mirrored current is not equal to the reference because of finite output

resistance, channel-length modulation, transistor mismatch and limited compliance voltage.

The performance of a current mirror is heavily dependent on the transistor geometry. Width and length define current drive capability, output resistance, matching behavior and power consumption. Wider devices may improve current drive and reduce mismatch, but also parasitic capacitance and layout area. Increasing the channel length can increase output resistance and the current accuracy, but it can also decrease speed and affect compliance requirements. Thus, the sizing of transistors in current mirrors is a trade-off management exercise and not a mere maximization of a single parameter.

The short-channel effects change the behavior of the devices and require a more careful analysis of the current mirrors in modern CMOS technologies. With decreasing channel length, effects such as velocity saturation, drain induced barrier lowering, and degradation of mobility become more prominent. The classical equations are less predictable because of these effects. Hence, circuit designers have to rely on accurate simulation to capture the real operating behavior.

Current mirrors are particularly suitable for this research because they present a small but interesting analog design problem. Their performance metrics are explicit, quantifiable, and sensitive to transistor dimensions, making them suitable for machine-learning-based modeling. The study of current mirrors is a demonstration of the methodology that can be later extended to other analog blocks

## 1.4 Challenges in Analog IC Design

Analog integrated circuit design is fundamentally different from digital design in a number of aspects that lead to challenges. First, analog circuits are designed to operate over a continuous range of voltage and current, and small changes in parameters can lead to large changes in behavior. Second, the analog performance is often a function of the interaction of multiple design variables that results in a nonlinear and highly coupled design space. One big problem is that we rely on technology. With CMOS technology scaling down, device characteristics change significantly. The assumptions of older analytical models are no longer valid. Much more important are short channel effects, parasitic and nonlinearities. Hence, a design that works well in one technology node may not map directly to another.

The motivation for this work is the continuing challenge of efficient and robust design of analog circuits in advanced CMOS technologies. When the technology is scaled up, the device behavior deviates more and more from the ideal assumptions. Small parameters that were once considered can become large sources of error. For example, channel length modulation, mobility degradation and oxide thickness variation affect the ideality of the current source, the transconductance and the electrical characteristics of the transistor, respectively. These effects are very sensitive to the sizing of the analog performance.

In practice engineers often start from a nominal design point and then manually iteratively fine tune based on simulation results. This process can be useful for simple circuits but it becomes inefficient when several design objectives need to be satisfied at once. The second challenge is process variability. Transistor characteristics can vary from chip to chip, wafer to wafer due to fabrication variations and global parameter shifts. Due to manufacturing imperfections parameters such as mobility, threshold voltage and oxide thickness may differ. Matching is often a sensitivity in analog circuits and variation can degrade the accuracy of current and cause performance drift.

The third problem is multi-objective optimization. Often the goals of an analog circuit designer are conflicting. For example, lowering power consumption may require smaller device size or lower bias currents but this may reduce output compliance or increase sensitivity to variation. Alternatively, larger transistors or stronger biasing may be needed to improve accuracy at a cost of power and area. Such trade-offs are hard to balance without systematic exploration tools.

A fourth problem is that many practical circuits do not have closed form design equations. Simple equations can provide a first estimate, but are often not sufficient to model realistic foundry behavior. This forces designers to resort to expensive simulation when the design space is large. Another important limitation is the high cost of iterative simulation. Each candidate design may require to be simulated at several DC and variation-aware operating-points. Manual evaluation is not feasible for thousands of potential design points. This leads to a strong need for surrogate models and intelligent exploration methods.

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## CHAPTER 2

### LITERATURE REVIEW

#### 2.1 LITERATURE INTRODUCTION

Historically, analog integrated circuit design has been a process of expert knowledge, analytical calculation, and refinement based on simulation. Digital circuit design is highly synthesis and automation-driven, whereas analog design is still largely manual and iterative. This has led to the investigation of techniques that can reduce design time, improve prediction accuracy and provide robust decision making under realistic constraints. In recent years, machine learning has become one of the most promising approaches to support analog design and optimization. The literature related to this thesis covers a range of areas including current mirror design, analog circuit simulation, process variation modeling, and machine learning based design automation. This chapter summarizes the most relevant concepts and approaches in these areas. The aim is to set the stage for the current work, to highlight the limitations of prior approaches, and to motivate why a machine-learning-enabled, process-variation-aware transistor sizing framework is both timely and needed.

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## Conventional Analog IC Design Flow

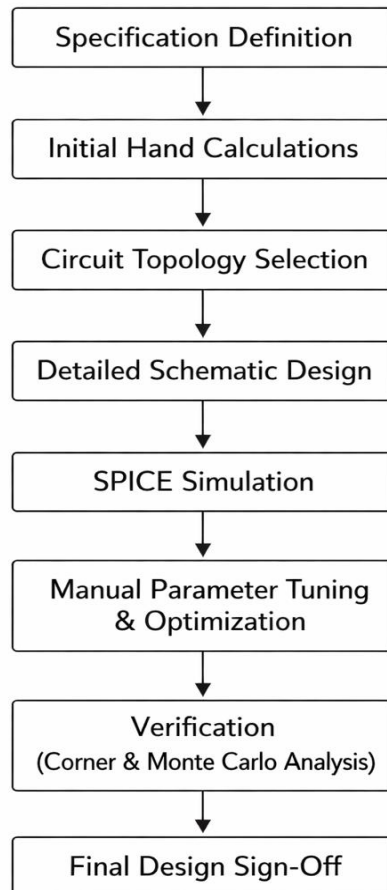


Fig. 2.1: Conventional analog IC design flow

## 2.2 Conventional Analog IC Design Flow

Historically, analog integrated circuit design has been a process of expert knowledge, analytical calculation, and refinement based on simulation. Digital circuit design is highly synthesis and automation-driven, whereas analog design is still largely manual and iterative. This has motivated researchers to investigate approaches that can reduce design time, improve prediction accuracy, and allow for robust decision making under practical constraints. In recent years, machine learning has emerged as one of the most promising approaches to assist analog design and optimization.

The literature used for this thesis is from several domains, including current mirror design, analog circuit simulation, process variation modeling and machine-learning based design automation. This chapter presents the most relevant concepts and approaches from these areas. The goal is to set the stage for the current work, highlight the shortcomings of previous approaches, and justify the need for a machine-learning aided, process-variation-aware transistor sizing framework.

The conventional analog IC design flow involves specification requirements, circuit topology selection, initial hand calculations, transistor level simulation, parameter tuning, and design verification. This method works fairly well for simple circuits but becomes increasingly inefficient as the number of constraints and design variables increases.

In the traditional flow the designer usually starts from a nominal point obtained from approximate equations. Then a set of candidate transistor dimensions is evaluated by SPICE or other circuit simulators. The designer then manually adjusts the values and re-runs the analysis based on the simulation results. This process can be repeated several times until the performance metrics meet the required thresholds.

This method, while widely used and understood, suffers from several disadvantages. First, there is a lot of reliance on the designer's intuition. Second, it might need a very large number of simulations. Third, it is hard to handle when the process variation is taken into consideration. Hence, conventional flow is often too slow for complex analog designs in advanced technologies.

The desire to automate or speed up this workflow has driven much of the research in analog design optimization and surrogate modeling. These efforts aim to reduce search time without sacrificing the ability to assess realistic device behavior.

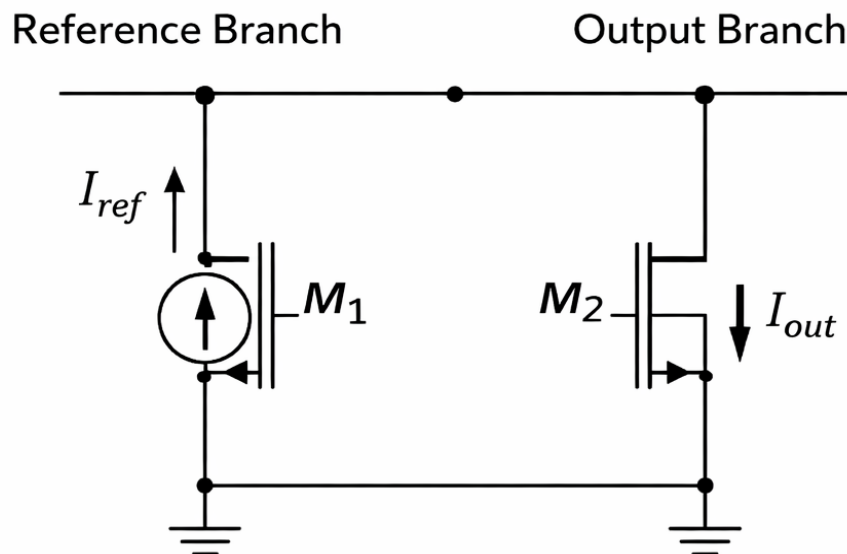


Fig. 2.2: Current mirror basic operation

## 2.3 Current Mirror Design and Performance Factors

Current mirrors are one of the most common analog reference circuits because they offer a compact means of generating and copying bias currents. The ideal current mirror copies the input current to the output branch without error. In practice, real current mirrors do contain a number of nonidealities, though.

Channel length modulation, which makes the output current dependent on the output voltage, is a major source of error. Another source is transistor mismatch due to geometry variations, random dopant fluctuations and layout-related effects. The compliance voltage is also important since the mirror can only accurately replicate current if the transistor output is in the proper operating region.

And that's why we have to carefully size the transistor in the current mirror. Width and length influence the mirror accuracy, output resistance and power dissipation. Thus the designer needs to make a trade-off between current accuracy and voltage headroom and energy efficiency. This trade-off makes the present mirror a suitable benchmark problem for studies in optimization and machine learning .

The literature on optimization of current mirrors shows that the improvement is obtained either by better device models or more systematic search strategies in the

design. Analytical methods alone are usually not enough, especially when deep-submicron effects are important. This necessitates simulation and learning based techniques.

## 2.4 Process Variation in 45-nm CMOS

With the CMOS technology scaling down to nanometer regimes, the process variations become more significant. The performance of analog circuits can be degraded by device-to-device mismatch and global parameter variations, particularly when they rely on accurate current replication. In a 45nm CMOS process, parameters like mobility, oxide thickness, threshold voltage and effective geometry can deviate from their nominal values.

These variations can cause changes in the electrical properties of the current mirror and can lead to current error, reduction in voltage compliance or unexpected power variations. Any sound methodology for analog design should take into account process variations at design exploration time, not only at the final implementation.

Traditional worst-case design methods and Monte Carlo analysis are useful but computationally expensive. Moreover, these methods often do not provide direct support for optimization. An attractive alternative is machine learning that learns the relationship between the design variables and the variation-sensitive performance metrics from simulation data.

## Sources of Process Variation in 45nm CMOS Technology

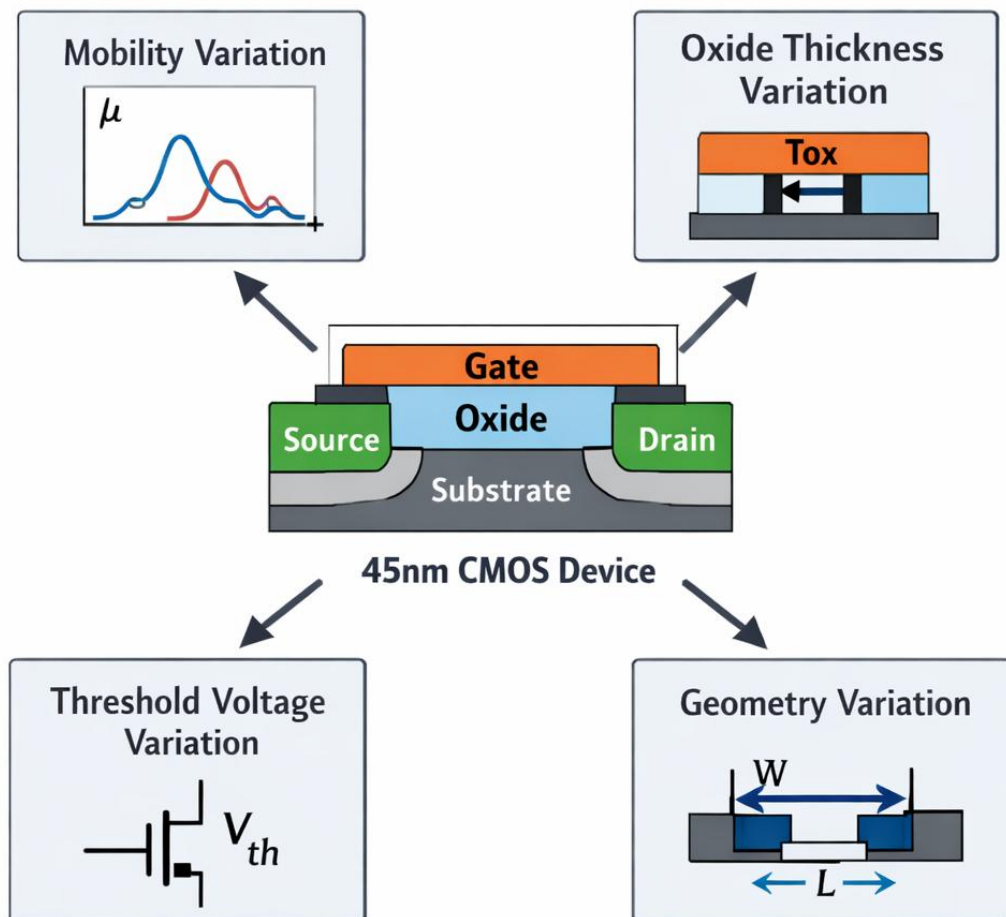


Fig. 2.3: Sources of process variation in 45-nm CMOS

## 2.5 Machine Learning for Analog Circuit Design

Machine learning has been increasingly applied to analog and mixed-signal design to accelerate prediction, optimization and robust analysis. The main idea is to develop a data-driven model that maps the inputs of a circuit (such as the transistor dimensions, bias currents and operating conditions) to its outputs (such as gain, bandwidth, power, error or sensitivity).

Previous studies have looked at various forms of machine learning. Neural networks have been used for circuit performance prediction. Decision trees and ensemble methods have been used for regression tasks with structured design data. Gaussian process models have also been considered in some contexts, due to their uncertainty quantification capabilities. In particular, ensemble-based methods are often particularly attractive for analog design, as they are well suited to nonlinear tabular data and tend to generalize well with moderate data sizes.

There are three main reasons why the use of machine learning in analog design is valuable. First, it decreases the number of expensive simulations needed at exploration time. Second, it can represent complex nonlinear relations between design variables. Third, it helps to identify the most influential parameters and thus increases interpretability. These benefits make ML especially suitable for transistor sizing problems in advanced CMOS technologies.

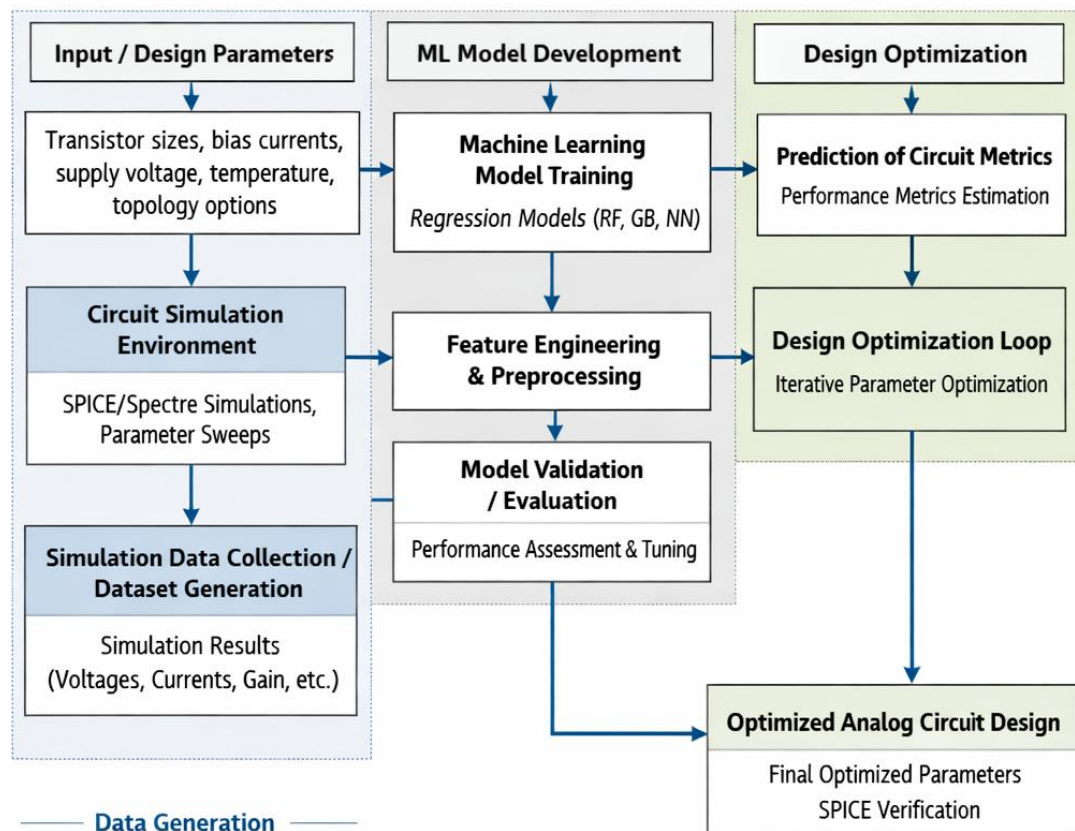


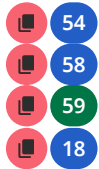
Fig. 2.4: Machine learning framework for analog circuit design

## 2.6 Ensemble Regression Models

Ensemble regression methods take the output from a number of decision trees or weak learners and combine them to produce more accurate and stable predictions. Two popular ensemble methods are Random Forests and Gradient Boosting. Random Forests build a large number of trees; each based on a random sample of the data and features and average their predictions. This reduces variance and increases robustness. Gradient Boosting builds trees sequentially, where each new tree attempts to correct errors of the prior trees. This often leads to improved predictive accuracy when the underlying relationships are complex.

These methods have some advantages in analog circuit modeling. They are very good for numeric tabular data, require little feature scaling and provide measures of feature importance. Also, relative to some of the deep learning alternatives, they are easy to train and interpret. Therefore, ensemble regression is very suitable for modeling performance at the circuit level and for design space exploration.

Ensemble models are especially useful in the context of this thesis because the simulation data contains nonlinear relationships between transistor sizing and performance metrics. The geometrical dependencies of the current error, power consumption, compliance voltage and variation sensitivity are highly non-trivial and are not independent. Ensemble methods handle such data well and provide a good compromise between speed, accuracy, and interpretability.



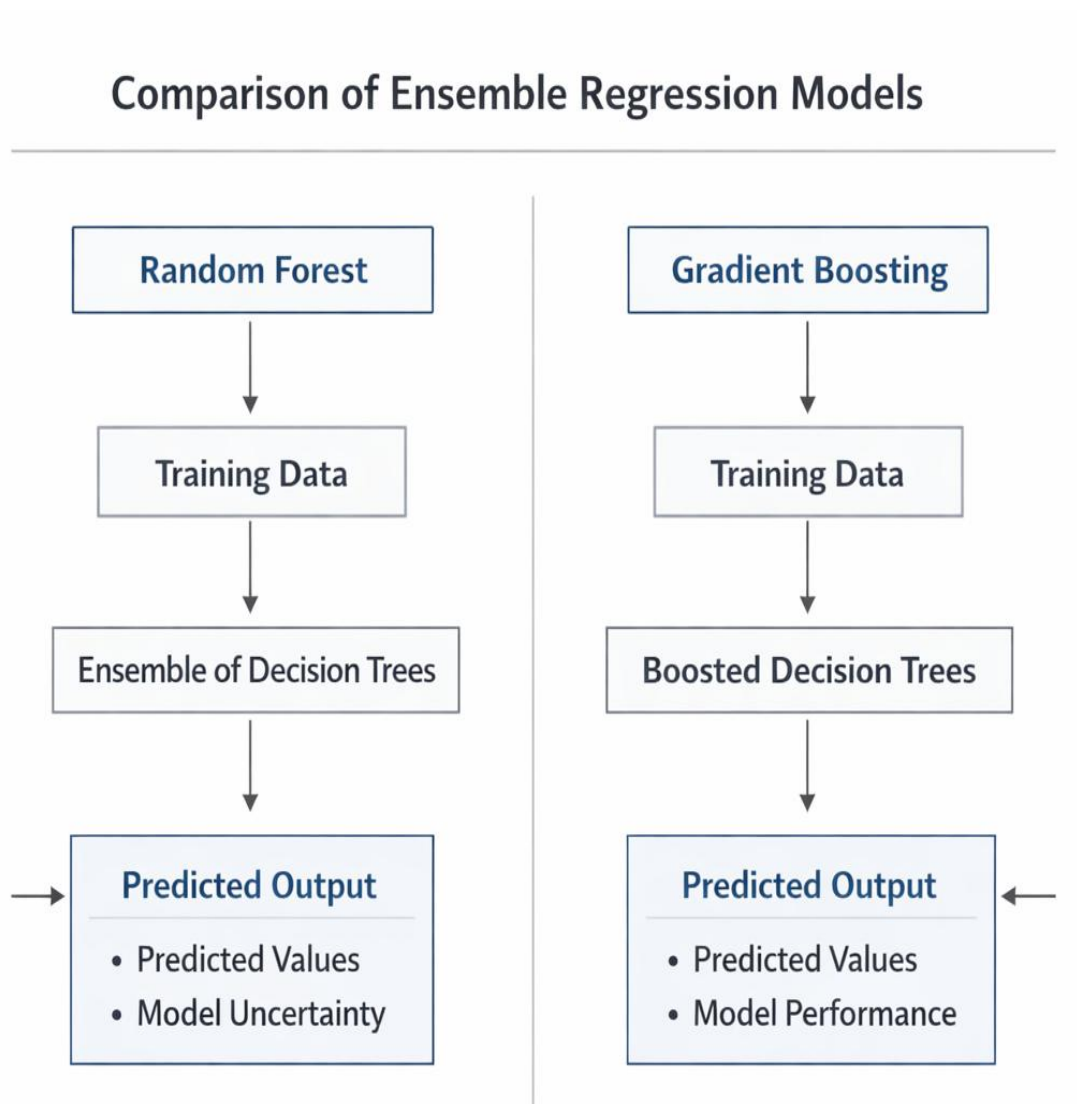


Fig. 2.5: Ensemble regression models used in this thesis

## 2.7 Research Gap

Prior work has made significant advances in the areas of analog design automation and machine learning based on optimization, but there still remain a few gaps. First of all, many studies are based on simplified device models instead of foundry-accurate simulations. That limits their practical relevance. Second, some approaches consider only nominal performance, without directly taking into account the process of variation sensitivity. Third, the size and realism of the dataset are often insufficient for strong generalization. Fourth, interpretability and feature analysis are sometimes missing, which makes it hard to understand why a model makes certain predictions.

Another important limitation is that many of the previous works treat prediction and optimization as separate from physical design constraints. In practical analog design, however, the solution must simultaneously satisfy this entire set of requirements. A model that predicts performance well but is unable to suggest feasible transistor sizes is of limited utility. A more complete framework is therefore needed.

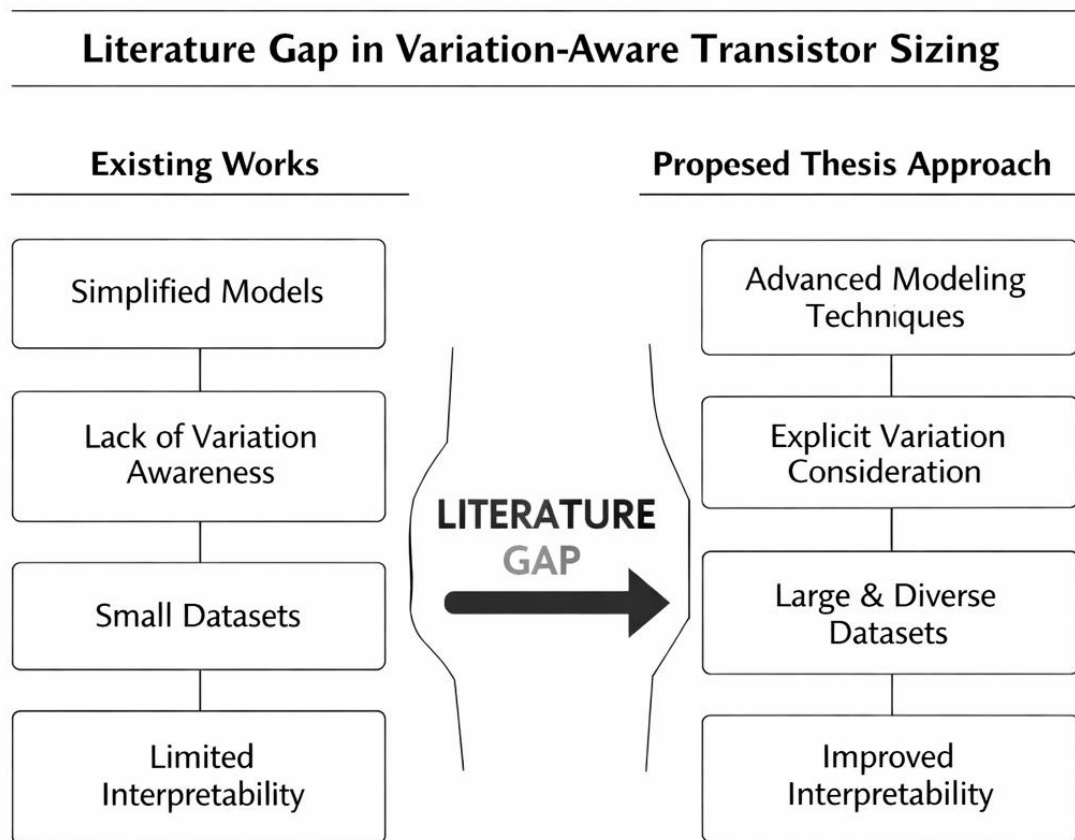


Fig. 2.6: Literature gap in variation-aware transistor sizing

This thesis aims at filling this gap, by combining foundry-accurate Spectre simulation, large-scale dataset generation, process-variation modeling, ensemble regression, feature importance analysis and ML-guided optimization. This integrated methodology is intended to offer a more practical and robust approach for current mirror sizing.

## CHAPTER 3

# CURRENT MIRROR DESIGN AND SIMULATION METHODOLOGY

### 3.1 Current Mirror Design Space

The main contribution of this thesis is the study of transistor sizing for CMOS current mirrors under realistic circuit conditions. The current mirror is a circuit that copies a reference current from one branch to another. Ideally, the currents are equal in magnitude. However, in a real CMOS implementation the output current depends on the transistor geometry, biasing, device mismatches and process variations. Thus, before any model training in machine learning, it is important to carefully define the design space.

In this work the design space is taken to be the transistor widths of the mirror devices, the channel length, the reference current and the operating temperature. The widths are varied systematically over a large range to include low-current, moderate-current and high-current operation regions. The channel length is fixed for the selected technology node and the reference current and temperature are varied to simulate real operating conditions. As a result, there is a rich and diverse set of simulation points to learn from.

Design space exploration aims not only at obtaining a working circuit, but also at understanding the effect of different sizing choices on performance metrics such as current error, power consumption, compliance voltage and process variation sensitivity. The dataset is then suitable for training regression models that generalize well across space by covering a sufficiently large range of values.



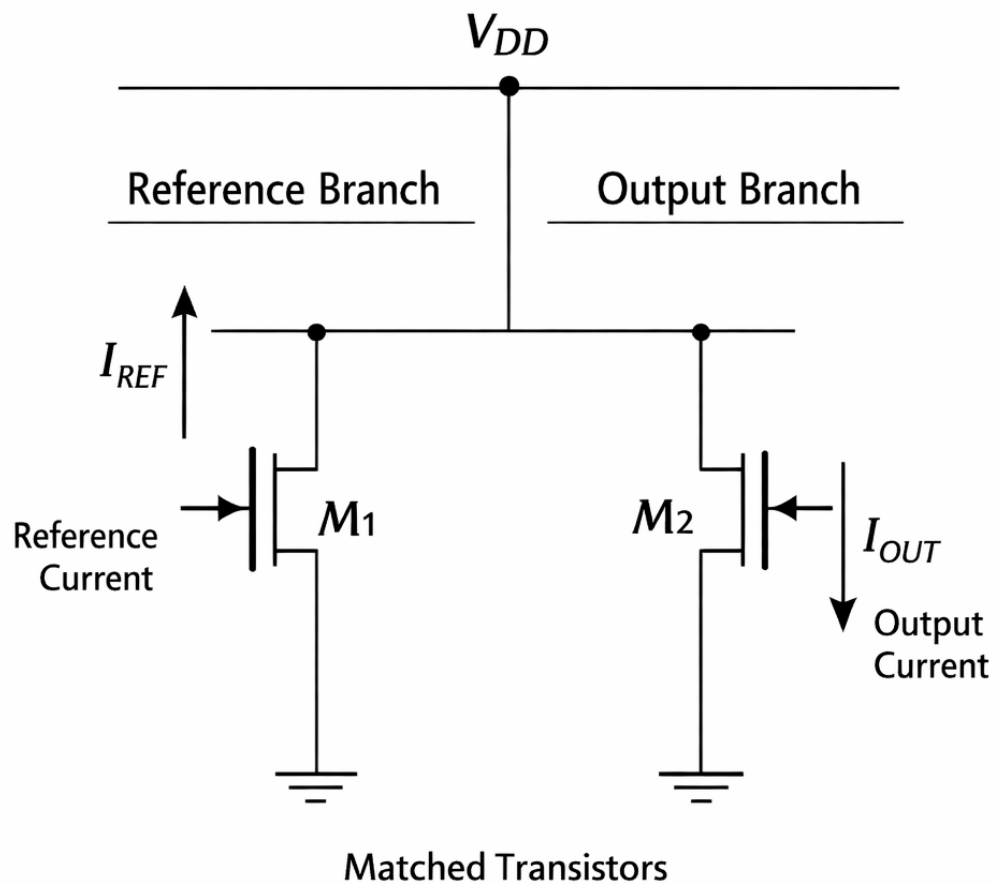


Fig. 3.1: CMOS current mirror schematic

### 3.2 Transistor Sizing Parameters

The most important design variable in current mirror optimization is the transistor size. In general, increasing transistor width improves current driving capability, and can reduce mismatches, but increases device capacitance, area and sometimes power. Channel length variation affects output resistance and saturation behaviour. Hence transistor sizing should be selected as a trade-off between accuracy, compliance, power and robustness.

The main sizing variables in the proposed framework are the widths of the transistors in the mirror topology. These widths are considered as an independent

input of the simulation and learning process. If you systematically change them, you can see how each individual size choice affects performance.

Further, the raw transistor dimensions are converted to derived quantities, e.g., width-to-length ratio and other normalized descriptors to aid machine learning. These transformed features allow the model to better capture the non-linear effects of sizing than the raw variables alone.

### 3.3 Foundry-Accurate Spectre Simulation Setup

Accurate simulation is the only way to produce meaningful training data. In this thesis the existing current mirror designs are studied with foundry-accurate BSIM4.5 models of a 45-nm technology node in Cadence Spectre. By employing a foundry-grade model, we ensure that short-channel effects, mobility degradation, channel-length modulation and other nonidealities are modeled as realistically as possible.

The flow of simulation starts with schematic capture of current mirror in design environment. Then, the parameters of the device are assigned according to the selected sweep conditions. Spectre does the DC analysis at each design point, and the output metrics are derived from the operating-point data obtained. Since the work is all about design-space exploration, the focus is on repeatable and systematic evaluation rather than a single circuit instance.

A significant strength of this work is the employment of a real simulation environment. This makes the corresponding data set more relevant to practical analog design and circumvents the limitations of simplified analytical approximations. Simulation is slower than direct evaluation by formula, but it provides ground truth data with sufficient fidelity for supervised learning.

**Table1.1— Parametric Sweep Ranges (45-nm CMOS)**

| Parameter         | Range                     | Step                  |
|-------------------|---------------------------|-----------------------|
| Transistor Widths | 0.12–10 $\mu\text{m}$     | 0.1 $\mu\text{m}$     |
| Channel Length    | 0.12 $\mu\text{m}$        | Fixed                 |
| Reference Current | 1–100 $\mu\text{A}$       | 1 $\mu\text{A}$       |
| Temperature       | 25–125 $^{\circ}\text{C}$ | 25 $^{\circ}\text{C}$ |

## Spectre Simulation Environment for CMOS Current Mirror Analysis

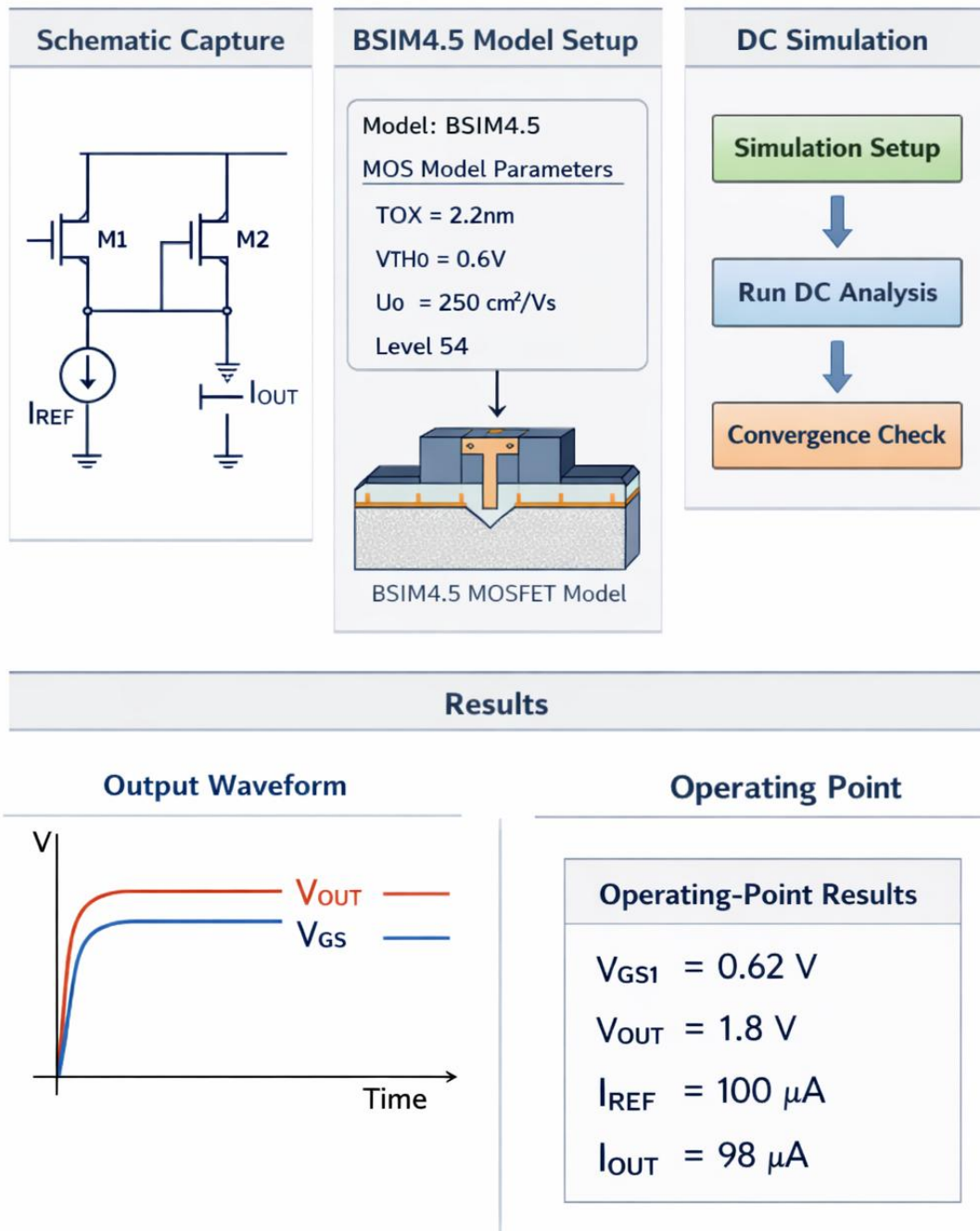


Fig. 3.2: Spectre simulation environment

### 3.4 Dataset Generation Using Parametric Sweeps

The data set used in this thesis was generated by systematic parametric sweeps of the desired transistor and operating parameters. The circuit behavior for each set of design parameters are summarized. This produces a large, structured table of input-output pairs for machine learning.

The usefulness of parametric sweeps is that they allow you to explore the design space in a predictable fashion. The sweep provides data with finely varying granularity and broad coverage, not random sampling without physical structure. This is particularly true in analog design, where small changes in the size of the transistor or in its biasing can dramatically change performance.

A large data set is needed because the relationship between input parameters and output metrics is non-linear. If only a few examples are used, the model might not learn important dependencies. On the other hand, a sweep-based data set that is large enough helps generalization and leads to more reliable predictions.

For each simulated design point, the key performance metrics relevant to the current mirror behavior are evaluated. This thesis studies the main parameters such as power consumption, current error and compliance voltage. These metrics reflect the key trade-offs in current mirror designs.

The present error is a measure of how close the output current is to the desired or reference current. This is a direct measure of the accuracy of the mirror. The smaller the current error the more accurate the current replication.

Power Consumption is the static power consumed by Circuit under selected operating conditions. Power efficiency is an important issue because the current mirrors are commonly used in bias networks. Such design with low error but high-power consumption may be unacceptable in the practice.

The compliance voltage is the minimum voltage that the mirror must output in order to function properly. In low voltage circuits, this metric is important because it determines the usable output range. Poor compliance of a design can lead to poor performance in system level applications.

Besides these primary measures, additional derived quantities can be calculated to support further analysis of the design space. These derived features can improve the quality of the machine learning features and help to unveil the trends of the circuits more clearly.

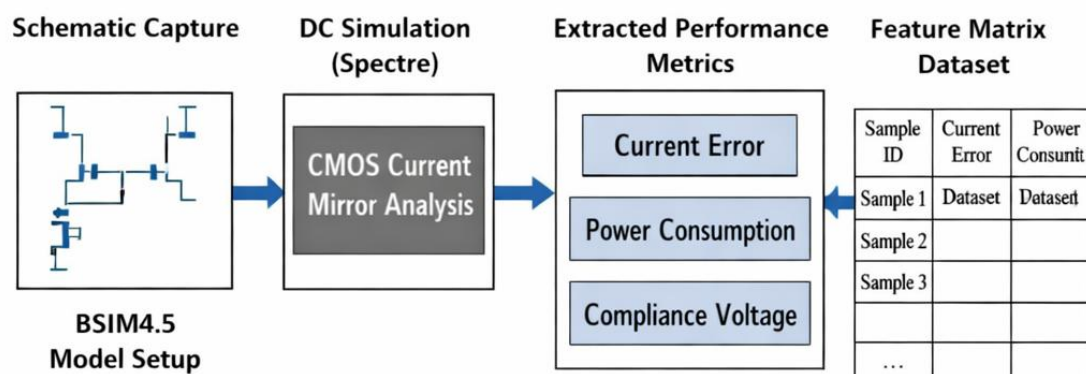


Fig. 3.3: Flow for dataset generation using parametric sweeps

### 3.5 Performance Metrics Extracted

The performance of each simulated design point is evaluated in terms of key performance metrics relevant to the current mirror behavior. The main metrics in this thesis are current error, power and compliance voltage. These metrics capture the major trade-offs in the present mirror design. Current error is the difference between the desired reference current and the output current. This is a direct metric of the mirror precision. The lower the current error, the more accurate the replication of current. Power consumption is the power needed by the circuit for the selected design point. Since current mirrors are widely used in bias networks, the power efficiency is an important issue. In practice, a design with low error but too much power might not be acceptable. Compliance voltage is the minimum output voltage needed for the mirror to operate correctly. This metric is particularly important for low voltage circuits, as it dictates the usable output range.

Compliance design that is poor may not function correctly in system level applications. In addition to these primary metrics, derived quantities may also be calculated to assist in further analysis of the design space. These derived features can improve the quality of the machine learning features and help to reveal the trends of the circuits more clearly.

### CMOS Current Mirror Performance Metrics Extraction

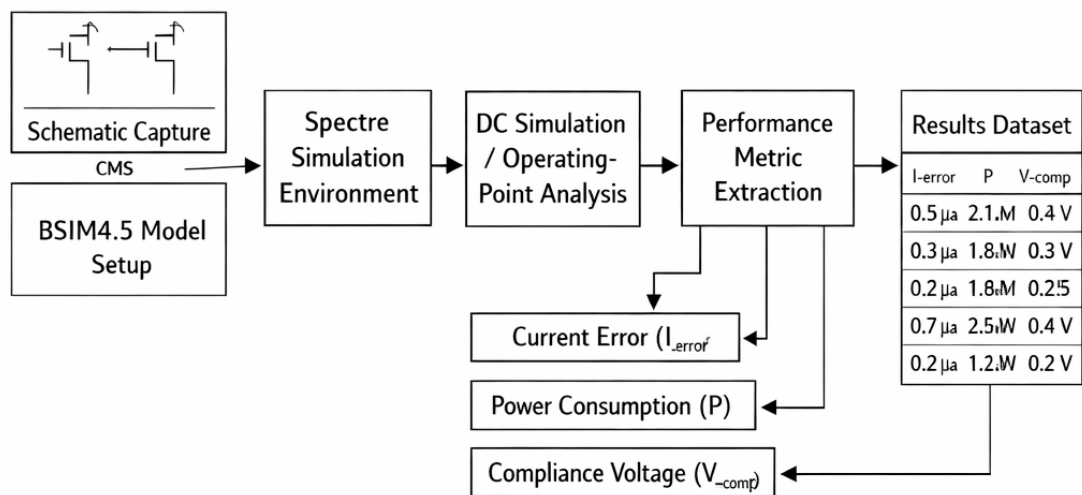


Fig. 3.4: Extraction of performance metrics from simulation data

### 3.6 Process Variation Modeling

One main objective of the thesis is to include process variations in the transistor sizing. Performance of current mirrors can be strongly affected by variations of fabrication parameters in advanced technologies. To account for this effect, the simulation framework incorporates global perturbations in parameters such as mobility variation and oxide thickness variation. In the paper, these are denoted by  $\mu_{0}$  and  $\text{ddtox}$ . These process parameters are introduced at the device-model level and enable the learning framework to observe the performance shifts under realistic manufacturing shifts. Rather than assuming idealized nominal conditions the study subjects the design points to controlled variation. This means the data produced is more representative of what happens in real silicon. Variation-aware modeling is critical, because today's mirrors need to be accurate not only at nominal conditions, but also across realistic

manufacturing spread. Thus the training dataset includes variation-related information such that the machine learning model can learn sensitivity patterns besides the nominal performance

### Process Variation Modeling in CMOS Current Mirror Simulations

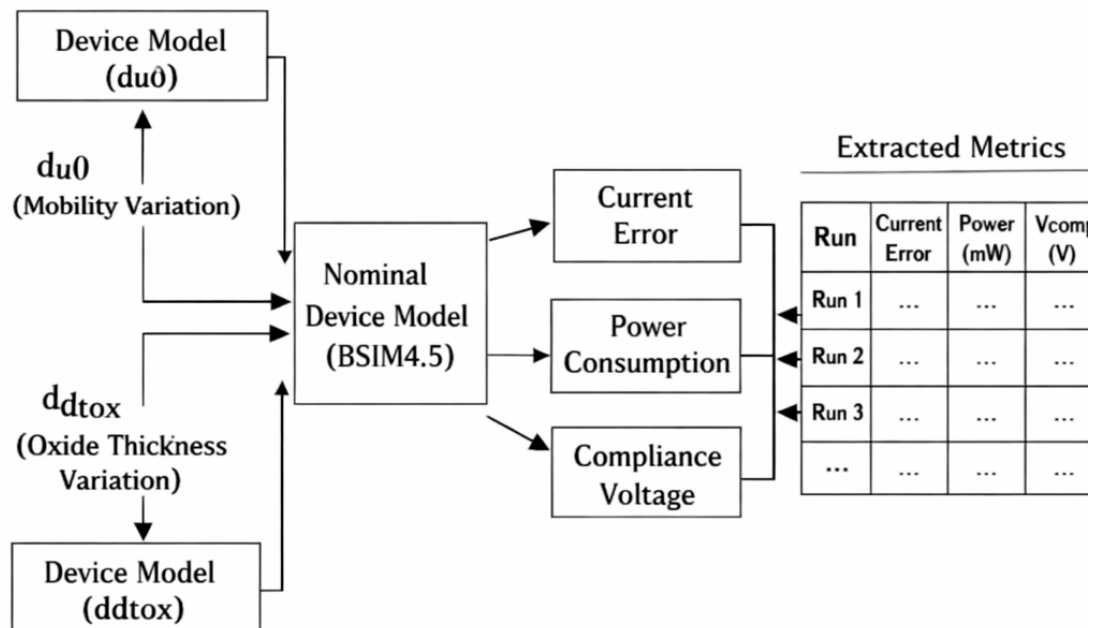


Fig. 3.5: Process variation modeling using du0 and ddt0x

### 3.7 Feature Engineering and Data Preparation

Often, raw simulation values are not enough for maximum predictive performance. To improve the learning process, features are extracted from the original transistor and operating parameters. These derived features include width to length ratios, normalized values and interaction terms that better capture non-linear relationships. Feature engineering is particularly relevant to analog circuit problems as many of the underlying dependencies are physical rather than purely statistical. The model can learn more efficiently and generalize better to unseen design points by designing features that capture known behavior of the circuits. After the feature creation, the data set is structured for machine learning. The inputs and the target labels are separated out and the data is cleaned to ensure consistency. The final prepared dataset is then fed to the regression models described in the next chapter.

### Feature Engineering Pipeline for CMOS Current Mirror Design Data

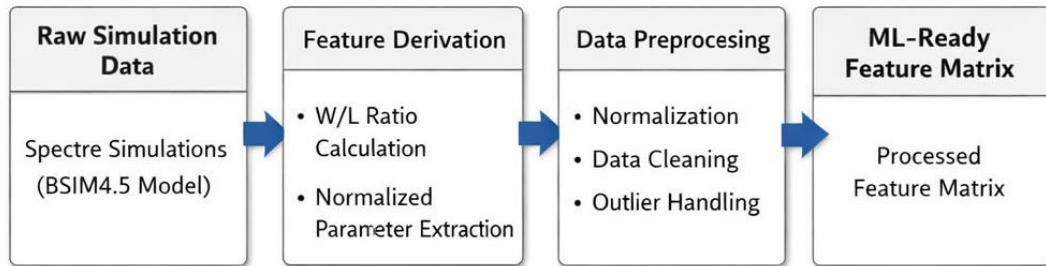


Fig. 3.6: Feature engineering pipeline

## CHAPTER 4

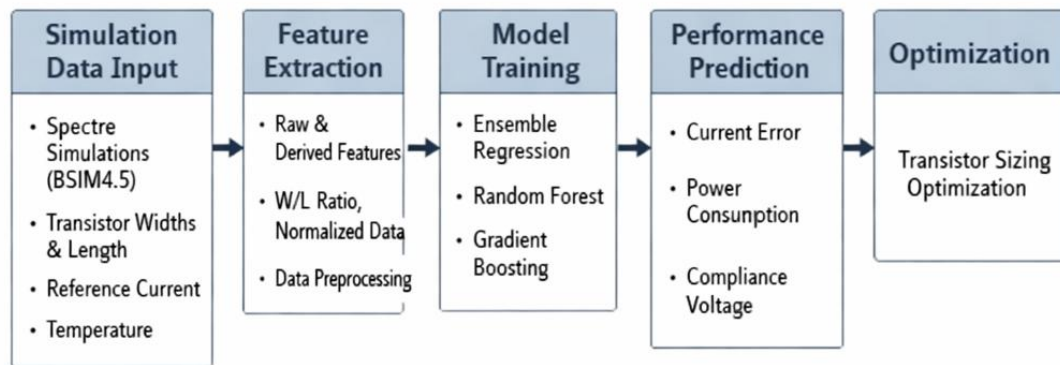
### MACHINE LEARNING FRAMEWORK FOR TRANSISTOR SIZING

#### 4.1 Overview of the Proposed ML Workflow

The proposed machine learning framework aims to learn the nonlinear relation between the transistor sizing parameters and the performance of CMOS current mirrors. Starting with simulation data from Spectre and ending with predictions of performance and optimized design recommendations, the workflow is: **The primary goal of the framework is to reduce the** design space exploration time and effort, while preserving the accuracy.

The workflow consists of four stages at a high level: dataset preparation, model training, model evaluation, and optimization. First, the simulation results are transformed into structured input-output pairs. Second, they train supervised learning models on the data. Third, the trained models are evaluated on the test data for their predictive performance. Finally, the best performing models are used to guide the decisions on transistor sizing.

Such a framework is of particular relevance for the design of analog circuits, where the relation between geometry and performance is highly non-linear and cannot be expressed with simple equations. Machine learning makes the design process drive much faster.



Proposed Machine Learning Framework for Transistor Sizing in CMOS Current Mirrors

Fig. 4.1 Proposed machine learning framework

## 4.2 Training and Testing Workflow

The data set is divided into training and testing sets to develop a reliable predictive model. The training set is used to train the model on the relationships between input features and output performance metrics, while the testing set is reserved for independent evaluation. This separation ensures that the model accuracy is measured on data not used for fitting and is not measured on examples already used for fitting.

The split is performed in a consistent and reproducible manner, usually with a fixed random seed. This allows the results to be compared across different experiments. A standard train-test split also helps to control the overfitting and makes it more meaningful to measure the model's generalization ability.

The model is trained with input features including transistor sizes, process variation conditions, and derived parameters after splitting. The trained model is then tested on unseen samples to evaluate prediction of current error, power consumption, compliance voltage and sensitivity. This gives you a quantitative picture of model performance with the metrics you get out of it.

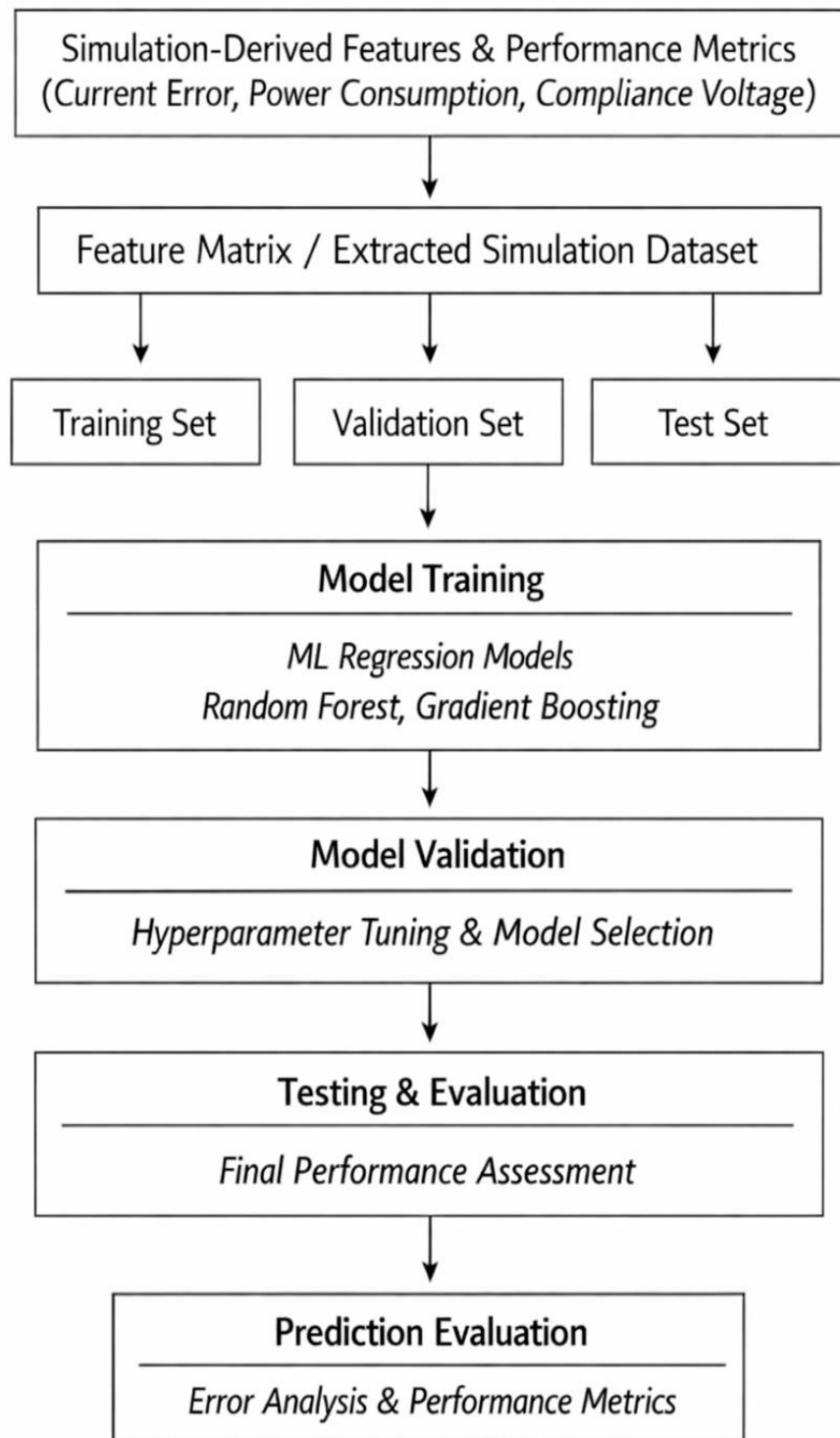


Fig. 4.2: Training and testing workflow

### 4.3 Random Forest Regression

Random Forest is one of the main regression models used in this thesis. It is an ensemble method that constructs multiple decision trees based on different bootstrap samples of data and averages their predictions. Each tree looks at a subset of the data and uses random subsets of features so the overall model is more stable and less prone to overfitting than a single decision tree.

In the field of data for analog circuit design, the Random Forest is especially useful since it can model the nonlinear relationships among multiple inputs without the explicit mathematical formulas. It works well on structured tabular data as well and gives useful feature importance scores. This is useful in the context of transistor sizing as it helps identify which variables are most important in determining the behavior of the current mirror.

The model is separately trained for each target metric. For example, a Random Forest regressor can be trained to predict the current error, another one to predict the power, and another one to predict the compliance voltage. This enables the framework to model multiple outputs with transparent evaluation.

## Random Forest Regression Architecture

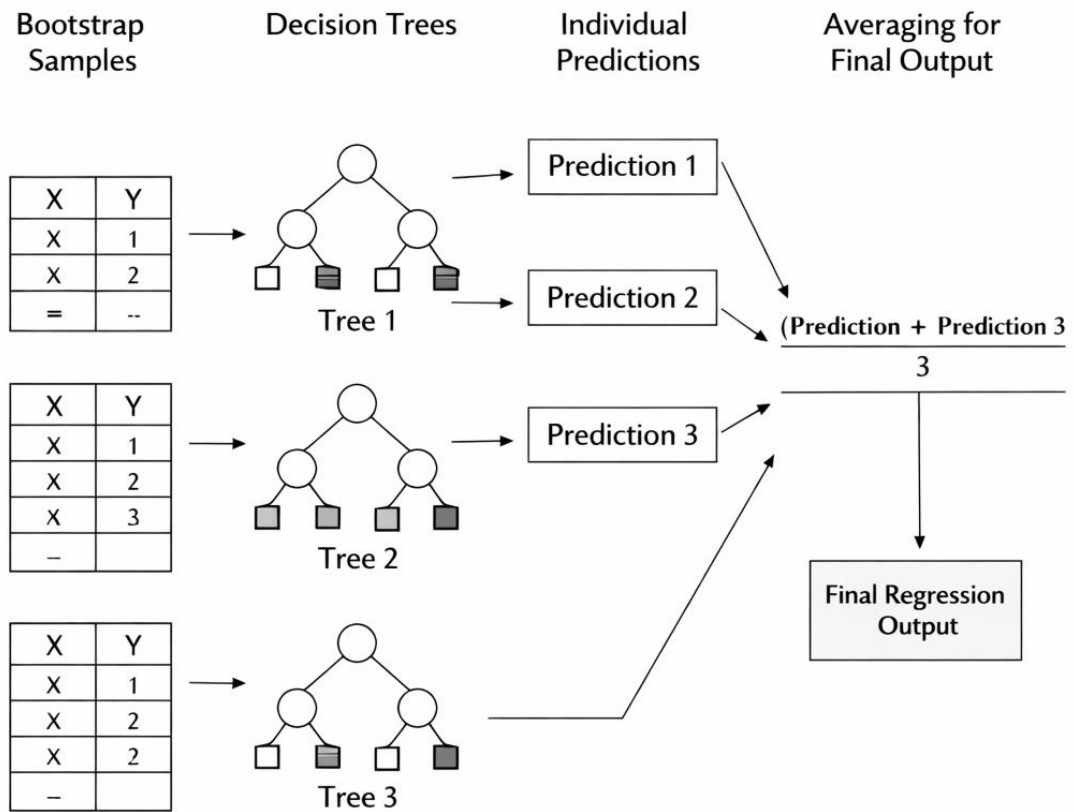


Fig. 4.3 : Random Forest regression architecture

## 4.4 Gradient Boosting Regression

In this work, we also use Gradient Boosting which is another ensemble learning method. Unlike Random Forest that averages many trees that are built independently, Gradient Boosting builds trees one after another. Each new tree tries to fix the prediction errors of the previous ensemble. This often leads to very accurate models when the underlying function is complex and non-linear.

Gradient Boosting is effective especially when the prediction needs higher accuracy. But analog circuits might behave a little differently depending on the size of the transistors and the process conditions. Hence, a boosting based regressor can capture the subtle differences in the data. This makes it a good complement to Random Forest in the proposed framework.

Also comparing Random Forest and Gradient Boosting helps to find the best model for different performance metrics. Sometimes one model is better for current errors, and another is better for compliance voltage. This multi-model approach leads to more robust models and better understanding of the learning.

### Gradient Boosting Regression Architecture

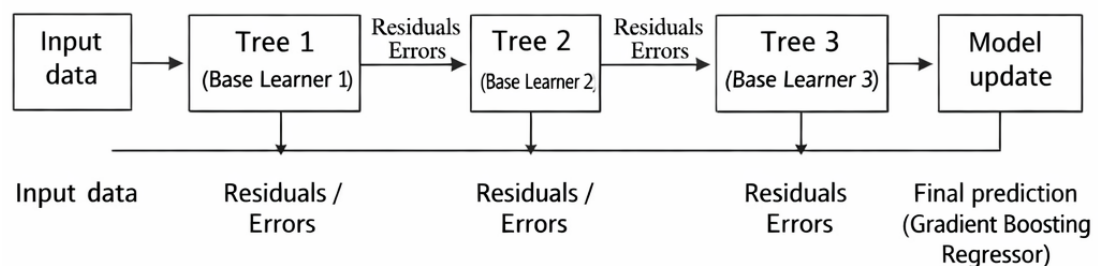


Fig. 4.4: Gradient Boosting regression architecture

## 4.5 Cross-Validation and Hyperparameter Tuning

The model parameters are tuned by cross-validation to improve the predictive performance. The accuracy and complexity of ensemble models are affected by hyperparameters such as depth of tree, number of estimators, learning rate, minimum split size etc. Therefore, proper tuning is needed to avoid underfitting or overfitting.

Cross-validation splits the training data into several folds and tests the model on different subsets of the data. This provides a more robust estimate of performance than a single split. It also helps in finding the hyperparameter settings that generalize well to unseen data.

The tuning is done systematically. Candidate parameter combinations are tried and the configuration with the best validation results is selected. This discipline improves the reliability of the final model and allows more robust conclusions to be drawn about predictive performance.

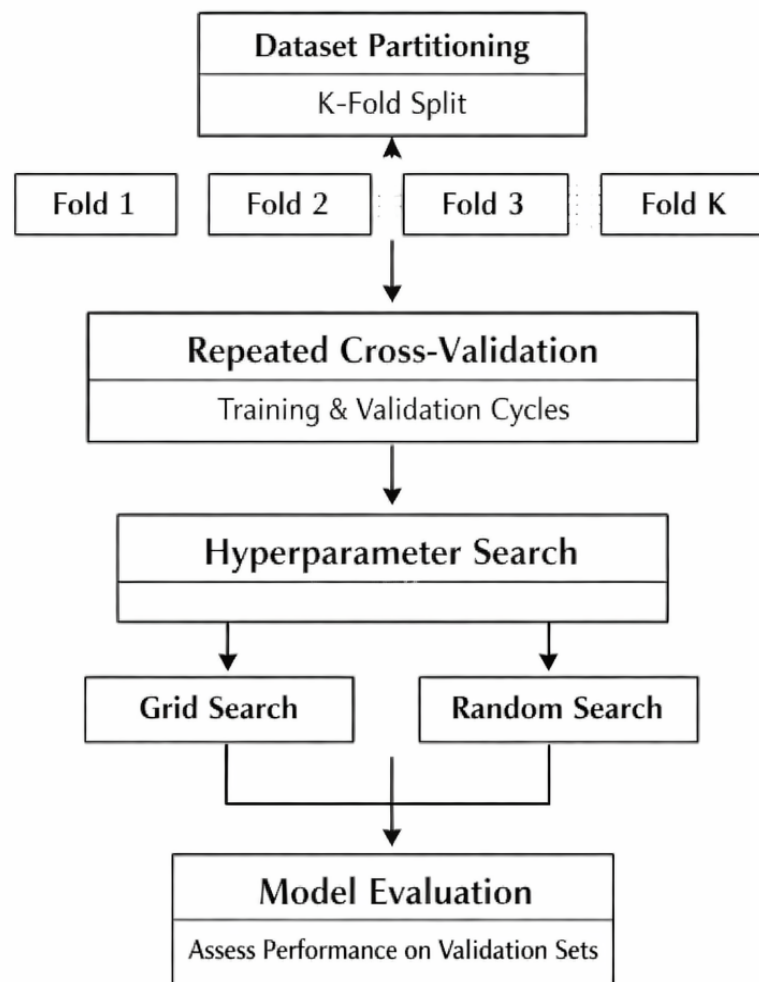


Fig. 4.5: Cross-validation and hyperparameter tuning process

## 4.6 Feature Importance Analysis

Importance analysis is a very useful interpretability tool for tree-based machine learning models. It measures the contribution of each input feature to the predictive power of the model. In this work, the effect of transistor and operation parameters on the current error, power, compliance voltage and variation sensitivity in CMOS current mirror sizing are analyzed.

The results of the feature importance analysis are useful for both model interpretation and engineering insight. For example, a high importance score for width-to-length ratio means that geometry is important to the behavior of the circuit. This conclusion is consistent with device physics and lends credibility to the machine learning model.

Feature importance can also be used to help simplify future design flows. If it turns out that some parameters have only a small influence, they can be fixed or given less priority in further optimization studies. This reduces the dimensionality and allows for more efficient search.

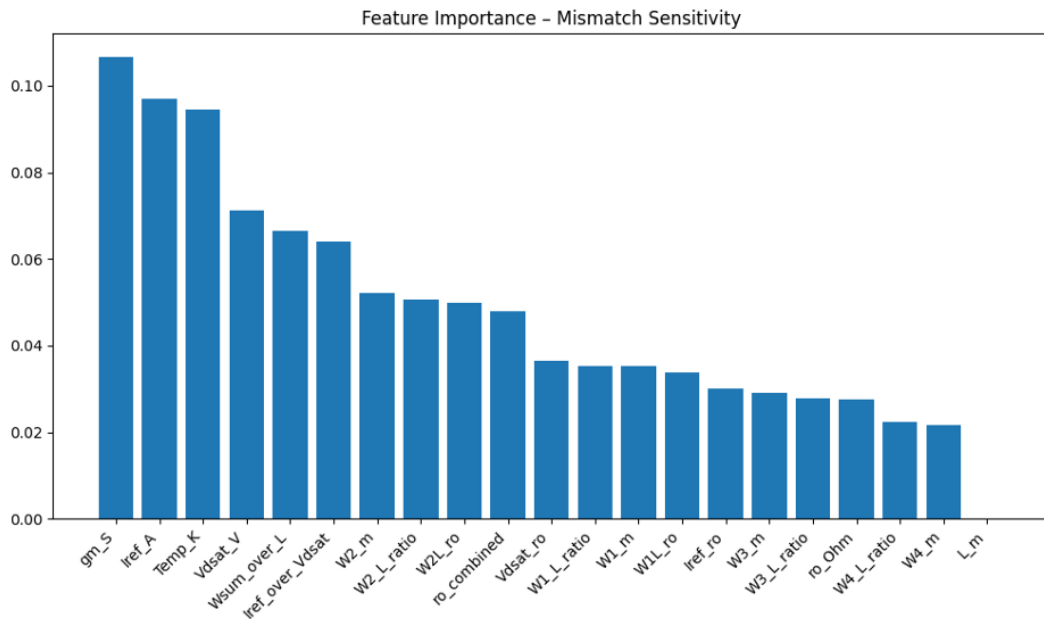


**Fig. 4.6 Feature importance analysis**

## 4.7 Feature Correlation Heatmap

The correlation analysis offers additional insights on the relationships between input features and output metrics. Correlation heatmap This helps in visualizing how strong the relationship between the variables is. This is particularly the case in analog design problems where multiple circuit parameters can be mathematically or physically coupled.

Looking at the correlation structure makes it easier to understand trade-offs and interdependencies in the design space. For example, making the transistor wider may improve one metric, but degrade another. Correlation analysis can identify such tendencies and help to develop better design intuition.

The heatmap also complements the importance of the features, as it shows if the two variables are redundant, or highly correlated. This can help you decide if

feature reduction or re-encoding is suitable.

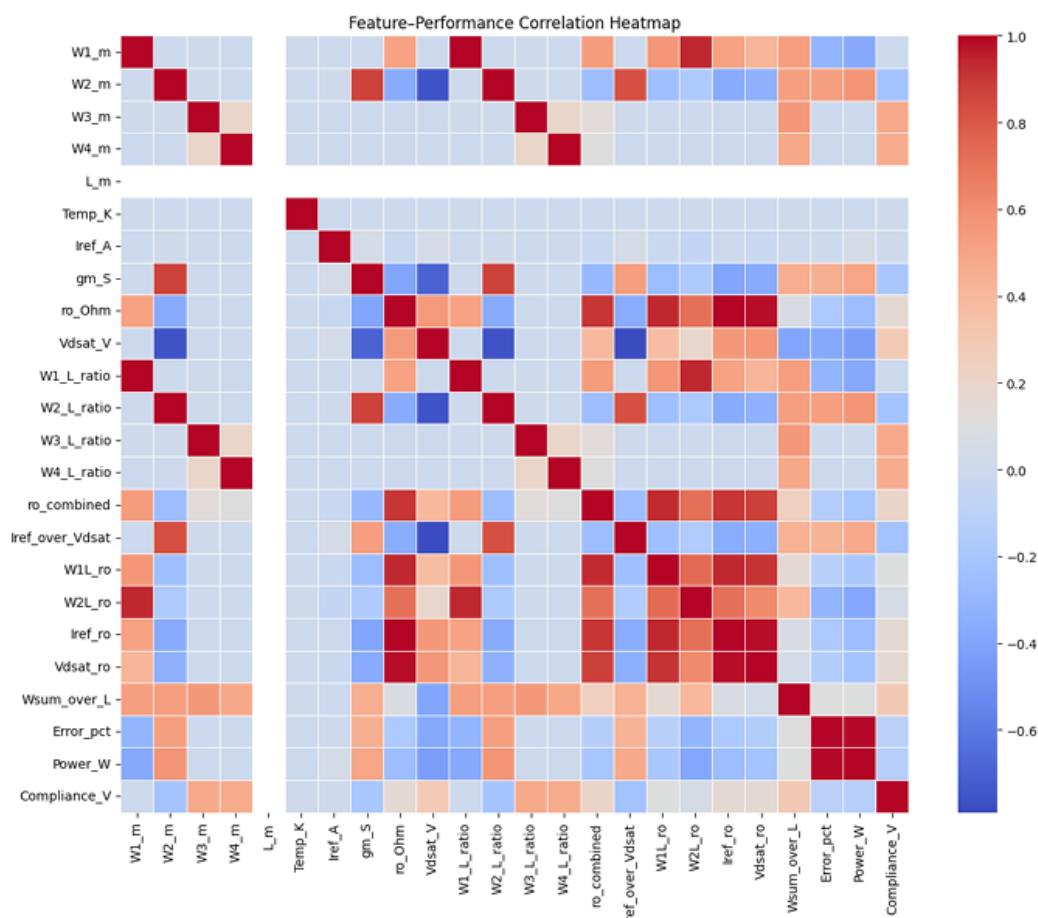


Fig. 4.7: Feature correlation heatmap

## CHAPTER 5

### RESULTS AND DISCUSSION

#### 5.1 Predicted Versus Simulated Current Error

The first major result of the proposed framework is the prediction of the current error for the unseen current mirror designs. Current error is an important parameter, as it directly reflects the accuracy of output branch in replication of reference current. In the proposed study, the machine learning models were trained to predict this metric from transistor sizing parameters, operating conditions and variation aware features.

The comparison between the predicted and simulated values shows good agreement, which proves that the models have successfully learned the nonlinear relationship in the simulation data. This is an important result, which demonstrates that a trained model can be a fast surrogate for SPICE-based evaluation. In practice, this means that designers can estimate mirror accuracy without running a full simulation for each candidate design.

The high prediction accuracy also indicates that the engineered features can capture the relevant physical behavior of the circuit. The error present is very dependent on the geometry of the transistor and the processing conditions. Any successful model would have to include these factors in some meaningful way. The results confirm that the proposed workflow fulfills that requirement.

**Table 5.1 — Performance Prediction Results**

| Metric       | MAE                  | R <sup>2</sup> |
|--------------|----------------------|----------------|
| Error (%)    | 9.05                 | 0.998          |
| Power (W)    | $4.1 \times 10^{-5}$ | 0.997          |
| Compliance V | 0.0164               | 0.981          |

## 5.2 Predicted Versus Simulated Power Consumption

Power consumption is another important metric in current mirror design, as the circuit is often employed as part of a biasing network or analog front-end where energy efficiency matters. However, a design with low current error can still be inappropriate, if it consumes too much power. Thus, power prediction was incorporated into the machine learning framework as one of its core tasks.

The results show that the ML models are able to predict accurately the power consumption over the design points tested. This demonstrates that the learned model can capture well the relationship between the transistor size, bias conditions and DC power behavior. Power is strongly correlated to current and device sizing, so the model needs to learn these dependencies well to predict accurately.

Accurate power prediction is useful from an engineering perspective, as it allows designers to quickly eliminate inefficient candidate solutions. It decreases the number of repeated circuit simulations and accelerates the overall design process.

## 5.3 Predicted Versus Simulated Compliance Voltage

A major practical constraint in design of current mirror is the compliance voltage. It states the minimum output voltage at which the mirror is still able to work correctly. This parameter is especially important for low voltage CMOS circuits as it defines the proper operation of the current mirror for the required output range.

The machine learning models also performed well in predicting the compliance voltage. The predicted values are very close to the simulation outputs, showing that the framework can learn the effect of sizing on voltage headroom and output operation range. This is an important result because, in advanced technologies, the compliance voltage is not always easy to estimate from simple analytical expressions.

The ability to accurately predict compliance can be used as a powerful screening tool for a designer prior to final verification. This is especially useful if there are many candidate points to be evaluated quickly.

## 5.4 Process-Variation Sensitivity Prediction

The contribution of this thesis is the inclusion of process-variation sensitivity into the prediction framework. The models were trained to predict not only nominal performance but also the response of designs to global variation effects such as mobility and oxide thickness shifts.

The results show that the prediction of process-variation sensitivity is harder than for nominal metrics. This is expected since variation-driven behavior can be partly stochastic and less deterministic. Nevertheless, the models are able to capture the main tendency with useful accuracy. This confirms the capability of the framework to model not only the ideal operation but also the variation-aware behavior.

The result is important as it assists in choosing robust design. A design that is good under nominal conditions, but very sensitive to process shifts would be a risky design in practice. ML model sensitivity prediction can be applied to find more robust transistor sizing options.

**Table 5.2 — Process-Variation Sensitivity Prediction**

| Metric                        | MAE    | R <sup>2</sup> |
|-------------------------------|--------|----------------|
| Process-Variation Sensitivity | 0.0103 | 0.003          |

## 5.5 ML-Guided Transistor Width Optimization

Then, the predictive models were used in an optimization flow to extract the transistor widths that meet the desired design constraints. The main requirement was to find solutions that keep the current error below an acceptable limit, the power below a specified threshold and the compliance voltage above a minimum value.

The optimization results show that the ML-assisted framework can effectively reduce the search space and find feasible transistor sizes in much shorter time than manual simulation. This is an important practical advantage of the proposed method. Then the designer can use the model to zoom in on only promising regions instead of spending hours exploring design candidates.

The optimization phase reveals the framework to be predictive and decision supportive. It actively suggests transistor dimensions that satisfy several constraints simultaneously and are thus well suited to analog design automation.

**Current Mirror Design Insights** One of the most important current mirror design insights is the trade-off between current accuracy and power consumption. One measure often influences the other. For example, increasing the size of the transistor may improve matching and reduce error, but may also increase the parasitic effects and the power usage. And as well as , lower power could mean smaller devices or lower currents , which can reduce accuracy .

The results of the proposed framework help to visualize such tradeoffs in a systematic way. By looking at predictions at many design points, the model shows how different choices of transistor sizing affect accuracy and power. That leads to balanced solutions, not extreme designs that optimize a single metric.

In practical analog design, a structured understanding of this trade-off is useful since most real applications require a balanced performance instead of a single optimization.

## 5.6 Trade-Off Between Current Accuracy and Power

One of the main insights in current mirror design is the tradeoff between current accuracy and power dissipation. Often one measure affects the other. For example, increasing the size of the transistor may improve matching and reduce error, but may also increase the parasitic effects and the power usage. And as well as , lower power could mean smaller devices or lower currents , which can reduce accuracy .

The results of the proposed framework help to visualize such tradeoffs in a systematic way. The model provides insight into the effects of various transistor sizing choices on accuracy and power by examining predictions at numerous design points. This helps to find balanced solutions rather than extreme designs optimized for a single metric.

This formal way of looking at this trade-off is useful in practical analog design because most real applications require balanced performance rather than isolated optimization.

## 5.7 Comparison of Manual Versus ML-Guided Design Iteration

The main advantage of suggested methodology is the shortening of the design iteration time. Manual analog design usually consists of repeated simulation cycles, parameter tuning and re-evaluation. This can take hours or longer depending on the complexity of the design space. In contrast, the trained ML model can quickly screen a large number of candidate designs and provides instant predictions.

The comparison between manual and ML-guided flows shows the significant improvement in efficiency by the proposed framework. Then the designer can use the model as a first pass decision tool and check only the most promising candidates with simulation. This hybrid approach is accurate and much less work.

This result shows the broader potential of machine learning for analog circuit design. The model is not a substitute for the designer, but an intelligent assistant to help explore and make better decisions faster.

## CHAPTER 6

### CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

#### 6.1 Summary of the Work

This thesis presented the process-variation-aware transistor sizing of CMOS current mirrors using machine-learning-assisted framework with foundry-accurate Spectre simulations. The main goal of the work was to reduce the manual effort involved in analog design while keeping realistic device behavior and robustness under process variation. To address this problem, a large dataset was built with systematic parametric sweeps over transistor dimensions, reference current, temperature and global process perturbations.

The proposed method combines supervised learning with circuit simulation. Gradient and Random Forest Boosting were trained for regression models for the key circuit metrics such as current error, power consumption, compliance voltage and process-variation sensitivity. The results showed that these models could capture the nonlinear mapping between transistor sizing and circuit behavior with high predictive capability.

One of the main benefits of the work is that the simulation data are obtained by using foundry-accurate BSIM4.5 models in a 45-nm CMOS technology node. This guaranteed that the learning framework was founded on physically realistic device behavior rather than simplified analytical assumptions. Therefore, the proposed approach can be employed in practical analog IC design flows.

This work has also shown that machine learning can be used to make robust transistor sizing decisions. The framework was used to extract the most influential sizing parameters from the feature importance and the correlations and to explain their effect on the performance. The learned relationships were then used in the optimization stage to find transistor widths satisfying practical constraints on accuracy, power and compliance voltage.

In summary, the thesis showed that machine learning can be successfully applied as a design-assist tool for analog current mirror optimization. It offers a fast surrogate to traditional simulation-based exploration and lays a foundation for more general analog design automation.

## 6.2 Main Contributions

The main contributions of this thesis are as follows:

### 1. Generation of large realistic datasets

We generated a large data set of ~50,000 design points using Spectre simulations with a 45nm BSIM4.5 model. The data set includes a wide range of transistor sizes and operating conditions.

### 2. Prediction of performance measures

The framework has been developed for prediction of current error, power consumption, compliance voltage and process variation sensitivity. With this multi-metric approach the model learnt several important features of the current mirrors performance.

### 3. Variation of size analysis process

In contrast to many other traditional design studies, the process variation parameters, e.g.  $\text{du0}$  and  $\text{ddtox}$ , were explicitly accounted for in this work. This increased the robustness of the framework and made it more generally applicable to realistic design scenarios.

### 4. Ensemble learning for analog forecasting

In this thesis, Random Forest and Gradient Boosting models were used to solve the analog circuit sizing problems. The ability of these methods to model nonlinear behavior and tabular simulation data was shown.

### 5. Feature engineering and interpretability

Features such as width to length ratios and normalized quantities were derived to improve the model performance. The analysis of feature importance also helped to discover the physical factors that influence the behavior of the circuit.

### 6. Machine Learning Based Transistor Sizing Optimization

The trained models were utilized to speed up the design-space exploration and find the transistor widths which meet the constraint-based design requirements. This was a big reduction in effort over tuning manually with simulation.

**These contributions jointly show that the proposed method is not only predictive but also practically useful for analog circuit design.**

### 6.3 Limitations

The proposed framework is effective but there are still some limitations that should be pointed out. First, we only consider the CMOS current mirrors in this study. This is an important and representative analog block, however the approach has not been validated yet on more complex circuits such as amplifiers, bias generators or data converters. More testing is needed to determine broader applicability.

Second, the process variation modeling in this thesis is based on selected global parameters, instead of full statistical Monte Carlo characterizations. The addition of  $\text{du0}$  and  $\text{ddtox}$  make the results more realistic, but a complete variation analysis would give a more complete robustness analysis.

Third, the model is trained on data generated in a specific technology node and simulation setup. Therefore, if the methodology is applied directly to another process node or PDK, the exact numerical behavior may change. Transferability across technologies would require retraining or adaptation.

Fourth, prediction with machine learning is fast but circuit verification cannot be replaced by it. Very unusual or extreme design corners may still need to be directly simulated in SPICE before finally being used. Hence, the ML model should be viewed as a surrogate and assistant rather than a full replacement of physical validation.

These limitations do not detract from the value of the framework but rather help to clarify the current scope of the framework, and the circumstances under which it should be applied.

## 6.4 Future Scope

The proposed work has many promising directions for future research.

### Extension to handle corners and Monte Carlo analysis

An obvious extension is to add full process corners and Monte Carlo simulations. This would offer a more complete characterization of robustness of design and statistical variation.

### Application to more complex analog blocks

The same machine assisted framework can be extended to other analog and mixed-signal circuits such as differential pairs, operational amplifiers, bias generators, current steering DACs and voltage references. These blocks would present additional optimization challenges and would further demonstrate the generality of the approach.

### Multi-objective optimization

Future work may consider more sophisticated multi-objective optimization techniques. Rather than treating current error, power and compliance voltage as separate considerations, a future framework could optimize all objectives together, under a Pareto-based approach.

### Integration with EDA tools

Another promising direction is integration with the electronic design automation tools. If the ML model can be embedded into the design environment, the workflow could become more seamless and accessible to circuit designers.

### Explainable and hybrid AI approaches

Future work may also focus on explainable machine learning, where the decision-making process of the model is made more transparent. Hybrid approaches combining analytical equations, simulation and machine learning may increase both accuracy and confidence.

### Expansion to new technology nodes

It would be interesting to understand the scalability of the framework by applying similar methodology to more recent CMOS processes. Intelligent design-assist

methods are likely to play a more important role as device dimensions are expected to further shrink.

The future directions suggest that the current thesis may provide a basis for further research in the area of analog design automation.

## 6.5 Social and Industrial Impact

This work is of industrial and social importance.

From the industry point, the framework can reduce the design time and increase the efficiency of the analog circuit development. This is especially important for applications with fast time-to-market and high design reliability requirements such as in communication systems, automotive electronics, consumer devices and sensor interfaces. It can reduce the number of manual simulation iterations and thus save engineering effort and speed up the development cycles.

Better analog design methodologies lead to better electronic systems in our daily life from a social point of view. Efficient current mirrors and other analog blocks are the basic building blocks for low power devices, portable instrumentation, medical electronics and connected sensors. Better design automation can lead to more energy efficient hardware, longer battery life, and more reliable operation in safety-critical applications.

The work also points to the growing importance of interdisciplinary engineering. It brings together circuit theory, semiconductor device modeling, machine learning and optimization. This is indicative of the path modern engineering is heading towards intelligent data assisted design methodologies that still retain physical understanding.

In this way, the thesis aims to contribute to both academic research and the long-term transformation of analog design practice.

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