

LOW POWER DYNAMIC TSPC D FLIP-FLOP FOR HIGH PERFORMANCE APPLICATIONS BASED ON CNTFET

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VLSI Design and Embedded Systems**

**by
Subodh Lakra
(Roll No. 2K24/VLS/23)**

**Under the Supervision of
Mr. Akshay Mann
Assistant Professor
Department of Electronics & Communication Engineering**



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daulatpur, Main Bawana Road, Delhi-110042, India

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Subodh Lakra



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-42

CANDIDATE'S DECLARATION

I, Subodh Lakra, hereby certify that the work which is being presented in the thesis entitled "LOW POWER DYNAMIC TSPC D FLIP-FLOP FOR HIGH PERFORMANCE APPLICATIONS BASED ON CNTFET" in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design and Embedded Systems submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from August 2025 to May 2026 under the supervision of Mr. Akshay Mann, Assistant Professor, Department of Electronics and Communication Engineering, Delhi Technological University.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute.

A handwritten signature in black ink, appearing to read "Subodh".

Subodh Lakra



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-42

CERTIFICATE BY THE SUPERVISOR

Certified that Subodh Lakra (Roll No. 2K24/VLS/23) has carried out the research work presented in this thesis entitled "LOW POWER DYNAMIC TSPC D FLIP-FLOP FOR HIGH PERFORMANCE APPLICATIONS BASED ON CNTFET" for the award of Master of Technology in VLSI Design and Embedded Systems from the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision.

The thesis embodies results of original work, and the studies are carried out by the student himself. The contents of this thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

Mr. Akshay Mann

Assistant Professor

Department of Electronics & Communication Engineering
Delhi Technological University

Date: 29/05/26

ABSTRACT

Low Power Dynamic TSPC D Flip-Flop for High Performance Applications Based on CNTFET

In today's Very Large Scale Integration (VLSI) systems, low power and high speed sequential circuits have become more and more important due to the demand for portable and high performance electronic systems. The digital circuits have different sequential elements which are important building blocks in digital circuits, which is the D flip-flops used in digital circuits are widely used in digital circuits which include registers, counters, memory elements and digital signal processing systems. But, there are significant problems with the conventional CMOS technology at nanoscale dimension like the leakage current, power dissipation and short channel effect. In this thesis, a comparative performance analysis of the two types of True Single Phase Clocked D Flip Flops (TSPCDFF): CMOS and CNTFET has been performed at 22nm technology. Four different TSPC D flip-flop architectures, conventional TSPC, modified TSPC, preset-enabled modified TSPC and redundant precharge-free TSPC D flip-flop architectures, have been investigated.

Evaluation of the performance is done on the basis of important parameters like Average power consumption, leakage current, propagation delay, Power Delay Product. The outcomes of the simulation confirm that the CNTFET based architectures offer high performance compared to CMOS based architectures. The redundant precharge-free CNTFET based TSPC D flip-flop was found to have the minimum PDP value among all the analysed architectures, which means that it has the lowest energy consumption and is best suited for the future low power high speed VLSI applications.

LIST OF PUBLICATIONS

1. Subodh Lakra and Akshay Mann, “Low Power Dynamic TSPC D Flip-Flop for High Performance Applications Based on CNTFET,” submitted to ”PICS-2026 2nd International Conference on Power and Intelligent Control System” Conference, 2026.

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NOMENCLATURE

CMOS	Complementary Metal Oxide Semiconductor
CNTFET	Carbon Nanotube Field Effect Transistor
TSPC	True Single Phase Clock
PDP	Power Delay Product
VLSI	Very Large Scale Integration
HSPICE	High Performance Simulation Program with Integrated Circuit Emphasis
CT	Conventional TSPC
MT	Modified TSPC
PMT	Preset Modified TSPC
PF	Precharge-Free TSPC

CHAPTER 1

INTRODUCTION

1.1 Introduction to VLSI Technology

In the last few decades or so, semiconductor technology has been advancing at a very fast pace and has turned electronic systems an entirely different world. The application of Very Large Scale Integration (VLSI) has led to the incorporation of millions of transistors on a single integrated circuit chip [29] circuit chip, which have made electronic devices compact, fast and efficient in terms of power consumption. VLSI systems are widely employed in various applications such as computers, communication systems, consumer electronics, medical systems, and industrial automation. With the ever improving fabrication technology, high density integrated circuits with performance and area improvements are becoming possible.

As the transistor dimensions have shrunk, the performance of circuits has increased in speed and decreased in power consumption. New integrated circuits are increasingly switching faster and are more functional as technology moves into the nano-scale region. But overscaling of the devices also poses several practical difficulties such as leakage current, short channel effects, reliability limited, and increased static power dissipation [22].

The constraints have spurred research and development into new device technologies that can perform as well at such low power consumption. Sequential circuits are basic building blocks of digital systems and are very common in digital communication systems, counters, memory units and processors. D flip-flops, being one of the most reliable data storage circuits and synchronization circuits, are one of the most commonly used sequential elements. Flip-flops are widely used in large digital systems, and their power consumption and switching speed have a significant impact on the overall performance of the system.

1.2 Scaling Trends in Nano-Scale CMOS Technology

A sequential circuit is one that has memory. Sequential circuits are digital circuits whose outputs are dependent on the current inputs as well as past states. These circuits are of fundamental importance in synchronous digital circuits for storing and processing information. Sequential circuits are used for various applications such as registers, counters, memory elements, and finite state machines [43]. The simple storage units of sequential logic systems are flip-flops [41], [42].

There are various types of flip-flops in digital circuits, based on the digital circuit application needs: SR flip-flop, JK flip-flop, T flip-flop and D flip-flop. Of these, D flip-flops are popular and widely used due to their simplicity of construction and efficient data storage capacity. In a high-speed digital system, the flip-flops can have a considerable portion of the propagation delay and power consumption [41, 42]. Thus, optimization of the architecture of the flip-flops has also a crucial role to assure low-power and high-performance operation of the circuit.

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1.4 Fundamentals of D Flip-Flops

A D flip-flop is a bistable sequential circuit which stores one bit of binary information. The output of the D flip-flop is changed based on the data input signal on the active clock edge. In SR flip-flops, the invalid state problem exists, which is resolved by the D

flip-flop. In addition, the D flip-flop allows reliable data transfer in synchronous digital systems. In registers, data buffers, shift registers, processors and memory circuits, d flip-flops are commonly used. If the size of the large digital system is large, it may include thousands of flip-flops, the switching activity of the flip-flops will be a significant part of the total switching activity of the system.

Therefore, designing low power flip-flops has become one of the major research fields in today's VLSI systems. The operating frequency [40] of digital circuits is directly related with the propagation delay of a flip-flop. Hence, in today's high performance application, high speed and low delay flip-flop architectures have become necessary.

1.5 True Single Phase Clock Technique

In the design of high speed sequential circuits, true Single Phase Clocking technique is used, since only one clock signal is required to operate the circuit. TSPC based circuits have a lower clock loading, simpler clock distribution, and faster switching speed than conventional master-slave circuits. The TSPC technique employs dynamic logic operation to decrease the number of transistors and enhance switching speed. TSPC architectures, which feature fewer clocked transistors, also lower the dynamic power consumption and offer better operating efficiency.

As a result of such benefits, TSPC D flip-flops are applicable to high speed VLSI applications. Due to the power reduction and propagation delay considerations, several architectures of TSPC D Flip-Flop have been proposed in recent years. In recent years, many architectures of TSPC D Flip-Flop have been proposed to reduce power consumption and improve propagation delay. The structures in [2] and [9] and [10] are modified TSPC structure that aim to reduce redundant switching activity and leakage current and have high speed operation.

1.6 Overview of CNTFET Technology

Carbon Nanotube Field Effect Transistor technology has been found to be a promising candidate for future nano scale integrated circuits, as an alternative to silicon based CMOS technology. CNTFET devices use carbon nanotubes in place of silicon as the channel material. Carbon nanotubes have excellent electrical properties such as high carrier mobility, near-ballistic transport and low leakage current. Compared with the conventional CMOS devices, CNTFET technology offers improved switching performance and electrostatic control [18]. Because of its low leakage current and

low power consumption, CNTFET based circuits are believed to be suitable for ultra-low-power VLSI applications. In the last few years, studies have investigated the implementation of CNTFET based imple- Logical circuits [14, 16, 18, 19], arithmetic units, memory cells and sequential circuits. It has been shown in several instances that CNTFET circuits can be designed to have a lower propagation delay and to have better Power Delay Product (PDP) than CMOS circuits. [24], [25]

1.7 Motivation of the Present Work

The increasing demand for portable electronic devices and high-performance computing systems has created a need for energy-efficient sequential circuits. Conventional CMOS technology suffers from increased leakage current and higher power dissipation at deep nano-scale dimensions. These limitations motivate the investigation of alternative device technologies capable of achieving low-power operation and high switching speed. TSPC D flip-flops are widely used in modern VLSI systems because of their compact structure and improved speed characteristics. However, limited comparative studies are available for evaluating CMOS and CNTFET based TSPC architectures under identical simulation conditions. Therefore, this work focuses on the comparative performance evaluation of different TSPC D flip-flop architectures implemented using CMOS and CNTFET technologies at 22 nm technology node.

1.8 Problem Statement

The propagation delay, leakage current and power consumption of CMOS-based sequential circuits increase when they are implemented at technology nodes of nanoscale. These challenges can constrain high-speed digital system efficiency, and drive the necessity for alternative low-power device technologies. While a number of low-power flipflop architectures are proposed, there is limited literature that compares and evaluates CMOS and CNTFET based TSPC D flip-flop architectures under the same simulation scenarios. Hence, the need for detailed performance analysis with important parameters like average power consumption, leakage current, propagation delay and Power Delay Product.

1.9 Research Objectives

The main goal of this research work is to simulate and compare the CMOS and CNTFET based TSPC D flip-flop designs at 22nm technology node using HSPICE simulation

environment. The particular objectives of this work are the following: 1. To learn various TSPC D flip flop circuits.

2. To implement the CMOS and CNTFET based TSPC D flip flop.

3. To test the average power consumption, leakage current, delay, and PDP.

4. Make a CMOS/ CNTFET technology comparison.

5. To find out the most energy efficient architecture in the TSPC D flip-flop.

1.10 Scope of the Thesis

The main theme of this thesis is the comparative study of 4 architectures of TSPC D flip-flops using 22 nm CMOS and CNTFET technology. It is limited to simulation based performance evaluation using HSPICE simulation environment. Average power consumption, leakage current, propagation delay and Power Delay Product are the major performance parameters considered in the study. No fabrication or physical implementation of circuits.

1.11 Organization of the Thesis

The thesis consists of six chapters. The introduction and background of the research work is presented in Chapter 1. The literature review on TSPC D flip-flops, CMOS technology and CNTFET based sequential circuits is discussed in Chapter 2. Chapter 3, the selected TSPC D flip flop architectures and their working are explained. The methodology and implementation of the simulation are described in Chapter 4. The results of the simulation and comparative analysis of the CMOS and CNTFET have been discussed in chapter 5. based architectures. At the end the conclusion, future scope and social impact of the research work is presented in Chapter 6.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

With the evolution of Very Large Scale Integration (VLSI) technology, need of digital systems with high-speed and low power has been rising. Sequential circuits are one of the most vital components of modern-day built-in systems because they are answerable for data storing, synchronizing, and timing operations. Flip-flops find wide application in processors, memory elements, communication systems, counters, registers and digital signal processing circuits. A large number of flip-flops are used in modern integrated systems and switching performance and power consumption of them directly affect the overall switching performance and power consumption efficiency of the digital circuits [1], [2].

As the CMOS technology has scaled towards deep nano-scale dimensions, several limitations have been observed such as the leakage current, threshold voltage variation, short-channel effects and increased static power dissipation in CMOS [3] and [4]. Such constraints lead to energy inefficiency in traditional CMOS sequential circuits and inspire the research of new technology and optimized circuit architecture for future VLSI applications. Since the introduction of the true single phase clocked (TSPC) D flip-flop, it has become very popular for high speed sequential circuit design because it only needs one phase of the clock to operate. Compared to conventional master/slave architecture, TSPC architectures offer lower clock loading, faster switching speed, easier clock distribution and smaller transistor count [5, 6].

In the literature, several variations of TSPC architecture have been suggested for further decrease of the dynamic switching activity and increase of overall energy efficiency. In recent years, Carbon Nanotube Field Effect Transistor (CNTFET) technology has been proposed as an alternative to the conventional CMOS technology that is being used for designing circuits for the future nanotechnology era. CNTFET devices have demonstrated better electrical characteristics including a high carrier mobility, near-ballistic transport, lower leakage current and lower switching losses [7, 8]. These characteristics make it possible to improve the speed and power consumption of circuits

based on CNTFETs over those based on CMOS. The review of the previous work has been presented in detail, covering CMOS flip-flops, TSPC architectures, low power sequential circuit design techniques, CNTFET technology, and comparison of CMOS and CNTFET based sequential circuits.

2.2 Conventional CMOS Sequential Circuits

The CMOS technology has been used as the dominant technology in digital IC design due to its low static power dissipation and high noise immunity. Because of their reliable switching characteristics and easy implementation, conventional CMOS based sequential circuits have been widely used in synchronous systems [9]. Some researchers have been working on power reduction and propagation delay in CMOS based flip-flop architectures. Wang and Yang [5] introduced an architecture of pulse triggered TSPC flip-flops for applications requiring high speed and low power in VLSI. Their work showed that by reducing the clock loading they can increase the speed of the circuit and reduce dynamic power consumption. In the 65 nm CMOS technology, Moreau et al. [10] designed a low power TSPC flip-flop architecture with low supply voltage. They managed to cut down energy usage, and enhance switching performance in low power applications. In the same way, Ajay Kumar et al. [11] suggested an 17 transistor static low power TSPC flip-flop architecture to reduce the number of transistors and the dynamic switching activity at the flip-flop.

The CMOS technology was successful, but with continued scaling down to the nano-scale, there are some limitations. CMOS-based sequential circuits suffer from leakage current and short channel effects which greatly affect the performance of such circuits [12]. The decrease in threshold voltage also results in higher static power dissipation and a lower noise margin for high density integrated systems. In order to optimize CMOS based flip-flops several different optimization techniques have been proposed such as clock gating, transistor sizing optimization, reduced switching activity and pulse triggered architectures [13] and [14]. These methods aim at decreasing the power consumption and enhance energy efficiency of synchronous digital systems.

2.3 Dynamic Logic and TSPC D Flip-Flop Architectures

The significant difference between dynamic logic circuits and static logic circuits is that dynamic circuits require less transistors and have faster switching speeds, which is an important factor in high-speed VLSI systems. Dynamic sequential circuits are

one of the most widely used circuits in high performance applications, such as TSPC D flip-flops [15]. This True Single Phase Clocking technique takes away the need for complementary clock signals and reduces the complexity of clock distribution networks. TSPC architectures are ones that only use one clock phase, which decreases clock power dissipation and increases switching performance [5]. Tang et al. [1] studied TSPC flip-flop architectures based on 3-independent-gate silicon nanowire FETs and showed high speed switching and low power consumption.

It was through their work that the significance of transistor level optimization for improving the performance of a sequential circuit was brought to light. Maheshwari and Sachdev [6] presented the architecture of low-energy static contention-free TSPC dual-edge triggered flip-flop which has reduced switching activity and low energy consumption. Their work is of minimizing contention current and energy efficiency in sequential circuits. There are also a few modified TSPC architectures proposed to minimize the redundant switching activity and enhance the energy efficiency. A modified TSPC D flip-flop architecture with a preset was suggested by Shaikh and Rahaman [16] with speed and power advantages over the conventional TSPC designs. Precharge-free architectures have gained lots of research interest due to the fact that the extra charging and discharging of internal dynamic nodes are avoided. Vishal et al. [17] proposed a low power and area precharge-free flip-flop architecture which resulted in significant power savings and superior Power Delay Product.

For reducing the clock frequency requirement and throughput, the research on Pulse triggered and Dual edge triggered TSPC architectures is taken [18] and [19]. These architectures minimize clock switching and increase the overall energy efficiency. Although there have been remarkable advances in TSPC architectures, dynamic circuits are still vulnerable to leakage current, charge sharing effect and process variations. Nano-Scale technology nodes [20] variations. Consequently, additional optimization and other device technologies are needed for future low power, high speed, sequential circuits.

2.4 Low-Power Sequential Circuit Design Techniques

With high operating frequencies and growing density of transistors in VLSI systems, power dissipation is becoming a serious issue of concern. The continuous switching of the clock makes sequential circuits a significant portion of the total chip power consumption [21]. Dynamic power dissipation in sequential circuits mainly occurs because of charging and discharging of load capacitances during switching transitions. Leakage current in nanoscale transistors [22] is the major cause of static power dissipation. A number of approaches have been suggested to minimize dynamic and static

power consumption. One of the most frequently used methods to reduce the unwanted clock transitions and to minimise the dynamic power consumption is clock gating [23].

The reduced transistor count architectures also contribute to reducing switching capacitance and energy efficiency. Recently, pulse-triggered flip-flops (PFFs) have become popular due to their high-speed operation at low clock loading [24]. Dual-edge triggered architectures additionally cut down on the clock frequency demands and enhance power efficiency [6]. Conditional precharge and conditional capture techniques have also been explored by several researchers that can help minimize redundant internal switching activity [25].

These techniques are designed to minimize unwanted power consumption when switching in idle situations. Other methods of power dissipation reduction in sequential circuits include voltage scaling and transistor sizing optimization [26]. But extreme voltage scaling can lead to higher propagation delay and lower reliability. The nano-scale technology nodes pose a severe leakage current problem because of the short channel effect and low threshold voltage [27]. As a result, the study of low leakage architecture and other transistor technologies have emerged as research directions in the field of modern VLSI design.

2.5 CNTFET Technology

The technology of Carbon Nanotube Field Effect Transistor (CNTFET) is a potential solution to the limitations of conventional CMOS technology for future nano-scale integrated circuits. CNTFET devices use carbon nanotubes as channel material that offers better electrical properties than silicon [7]. The characteristics of CNTFET devices are a high carrier mobility, low scattering effect, near-ballistic transport, and a low leakage current [28]. These properties allow the CMOS based circuits to be faster and consume less power than the CNTFET based circuits. The electrical properties and modelling of CNTFET devices in digital applications have been studied by several researchers. CNTFET technology offers better electrostatic channel control and less of short-channel effects, which leads to a better possibility of nano-scale circuit design [29].

Rupani et al. [8] introduced energy efficient CNTFET based arithmetic circuits and showed significant energy efficiency advantage over CMOS-based arithmetic circuits. Nagarajan et al. [6] has presented CNTFET based sequential elements for low power digital applications, with the results of propagation delay and leakage current reduction. Hybrid CMOS-CNTFET systems have also been considered for better integration with the current fabrication processes and better performance [32].

Such hybrid devices are those that use both CMOS and CNTFET technologies to

achieve the best performance in circuit operation. SRAM cells, multiplexers, latches, and arithmetic units with CNTFET have also been investigated for future low-power computing systems [33] and [34]. Most studies show that the Power Delay Product of CNTFET circuits is better than the Power Delay Product of the CMOS circuits and the leakage current is also lower than the leakage current in case of CMOS circuits. CNTFET technology has very good electrical properties, but there are some limitations to the practical applications, including fabrication complexity, alignment of the nanotubes and process variation [35]. However, CNTFET technology is still a very interesting one to consider in the future VLSI systems with small dimensions.

2.6 CNTFET Based Sequential Circuits

The sequential circuits using CNTFET have been explored by a few researchers to obtain better speed and reduce in power consumption. CNTFET based D flip-flops, latches and memory circuits have already been shown to exhibit better performance than their CMOS counterparts [31]. In the recent years, Vaithiyanathan et al. [4] studied the recent architectures of flip-flops for low power and high speed applications and concluded that the propagation delay and power consumption could be reduced significantly by implementing CNTFET. Nagaleela et al. [3] presented the high performance scan D flip-flop architecture with advanced transistor technologies and showed it to be faster and more energy efficient than existing architectures.

Binaei and Gholami [9] explored the architectures of D flip-flop using multiplexor technology in the nano-scale technologies with better switching performance and reduced energy consumption. It is shown in several comparative studies that sequential circuits built using CNTFETs are more power-efficient, have lower leakage currents, lower delays and lower Power Delay Products [39] and [40] than sequential circuits built using CMOS circuits. Based on CNTFET, ultra-low power sequential circuits for portable electronic systems and battery operated devices are also under research [41]. The lower power dissipation and lower operating voltage of the CNTFET devices.

Make them highly suitable for use in energy efficient applications. Recent studies have been dedicated to hybrid and optimized CNTFET architectures which can achieve improved reliability and better fabrication compatibility [42]. These studies also confirm the suitability of CNTFET technology for future generation VLSI systems.

2.7 Research Gap Identification

The literature shows that there are one or more architectures of low power TSPC D flip-flop proposed for high speed VLSI applications. Scientists also have shown the benefits of CNTFET for the design of low-power circuits at the nano scale. But most of the earlier works are concerned with CMOS or are only concerned with a single CNTFET implementation under various simulation parameters and technology nodes. Very few studies report comparative analysis of a number of TSPC D flip-flops implemented in both the CMOS and CNTFET technologies under similar simulation conditions [36, 39].

Moreover, most of the existing works consider only one of the performance metrics (either power reduction or delay reduction) and only few works consider multiple performance metrics, including average power consumption, leakage current, propagation delay, power dissipation, and Power Delay Product at once. Hence, there is a need to compare the different CMOS and CNTFET based TSPC D flip-flops architectures systematically. The circuits were simulated under identical 22 nm technology conditions and HSPICE simulation environment with accurate performance evaluation.

2.8 Summary

This chapter gave an in-depth review of the previous work done on CMOS sequential circuits, TSPC D flip-flops, low power design methods, CNTFET technology and CNTFET based sequential circuits. The literature revealed that CNTFET technology has many advantages over the conventional CMOS technology regarding the reduction of leakage current, power dissipation, faster switching speed, and higher energy efficiency. The review further shows how optimized TSPC architectures—including preset-enabled and redundant precharge-free designs—can further enhance the performance of sequential circuits.

However, in the existing literature the analysis of the CMOS and CNTFET based TSPC architectures is limited to the comprehensive comparative analysis under different simulation conditions. Hence, in this work, we are only concerned about the comparative performance analysis of four architectures of TSPC D flip-flop. The design has been done at 22 nm technology node using CMOS and CNTFET and simulated in HSPICE simulation environment.

CHAPTER 3

TSPC D FLIP-FLOP ARCHITECTURES

3.1 Introduction

Flip-flops are one of the most crucial sequential circuits employed in digital systems as they store and synchronize data. The speed, power dissipation and reliability of the VLSI system directly depend on the performance of flip-flops in high-speed VLSI systems. Because of their small clock loading, small structure and fast switching speed, true Single Phase Clocked (TSPC) D flip-flops are generally employed in the design of sequential circuits. This chapter introduces the various architectures of the TSPC D flip-flops, which are investigated in this research work. Four different architectures are explored and designed on both CMOS and CNTFET technologies at 22nm technology node. Conventional TSPC D flip-flop, modified TSPC D flip-flop, preset-enabled modified TSPC D flip-flop and redundant precharge-free TSPC D flip-flop have been chosen for analysis.

3.2 Conventional TSPC D Flip-Flop Architecture

One of the most common dynamic sequential circuits to be used in high speed applications is the conventional true single phase clocked D flip-flop. Architecture is clocked with only a single clock, making clock distribution easy and clock power consumption low.

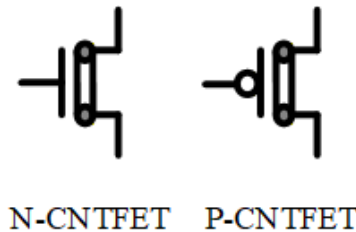


Figure 3.1: Symbol representation for N-CNTFET and P-CNTFET

The traditional TSPC was based on a single clock signal to control the dynamic

stages. On the active clock phase the input data is switched dynamically to the output. With fewer transistors and compact structure, switching performance and propagation delay have been enhanced. The conventional TSPC D flip-flop has better speed characteristics and is suitable to be used in high frequency applications. Switching activity in internal nodes, though, adds to power consumption and leakage current.

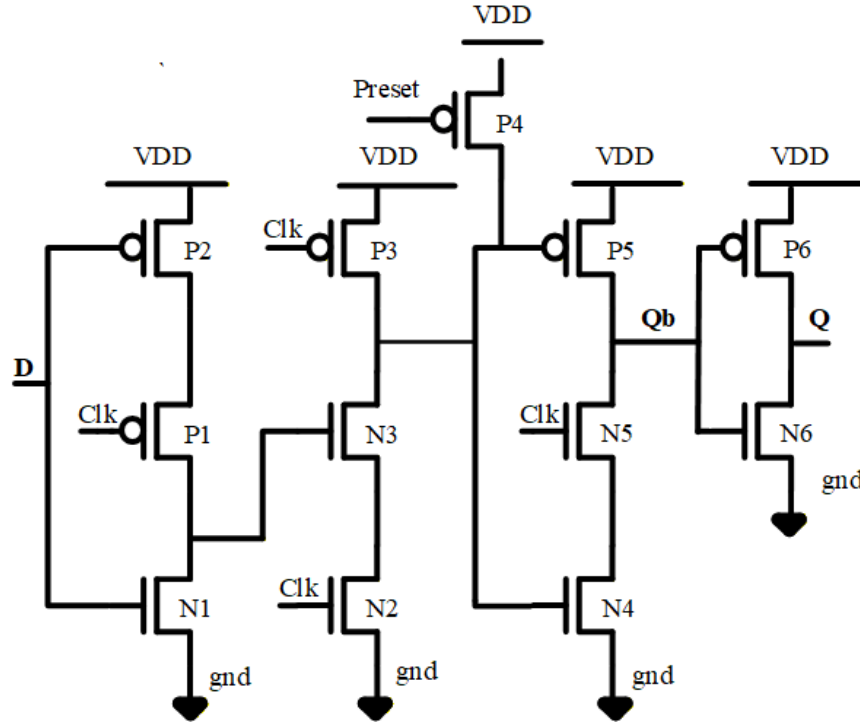


Figure 3.2: Conventional TSPC D Flip-Flop Architecture

CNTFET implementation of the conventional TSPC D flip-flop uses carbon nanotube field effect transistors (FETs) in place of MOS transistors. The CNTFET device's superior carrier mobility and lower leakage current allows the architecture to deliver better energy efficiency than CMOS implementation.

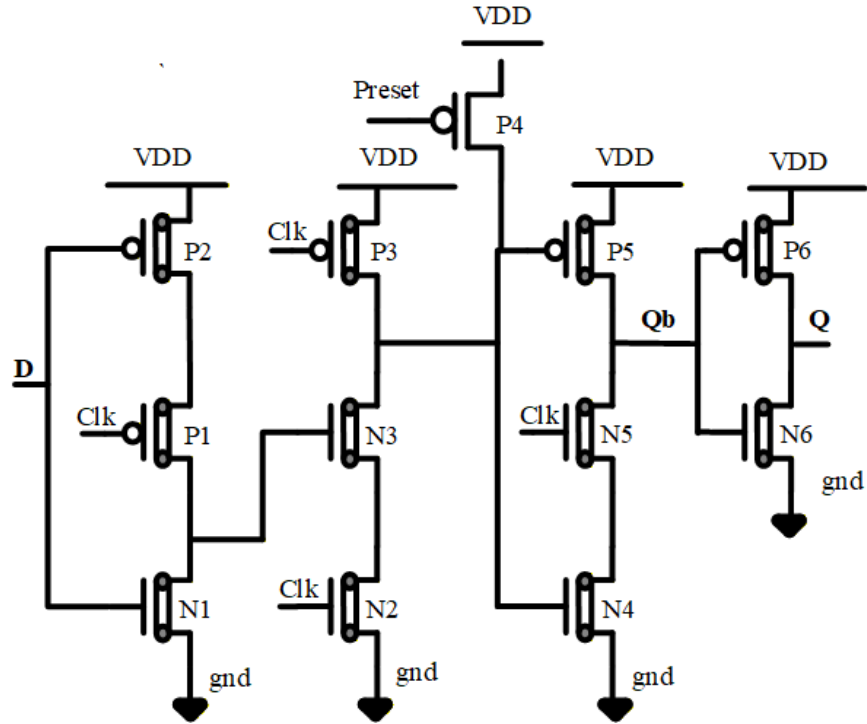


Figure 3.3: CNTFET Based Conventional TSPC D Flip-Flop Architecture

3.3 Modified TSPC D Flip-Flop Architecture

The modified TSPC D flip-flop design is designed for addressing the performance restrictions of traditional TSPC circuits. Some other transistor configurations are added to minimize the unnecessary switching of intermediate nodes. The modified architecture reduces unnecessary changeover between the different clocks while switching operation to reduce average power consumption. Also, the performance of Power Delay Product is improved by reducing number of dynamic node transitions. The modified structure shows better energy efficiency and propagation delay than the conventional TSPC structure. The architecture guarantees high speed operations, without any unnecessary internal switching activity.

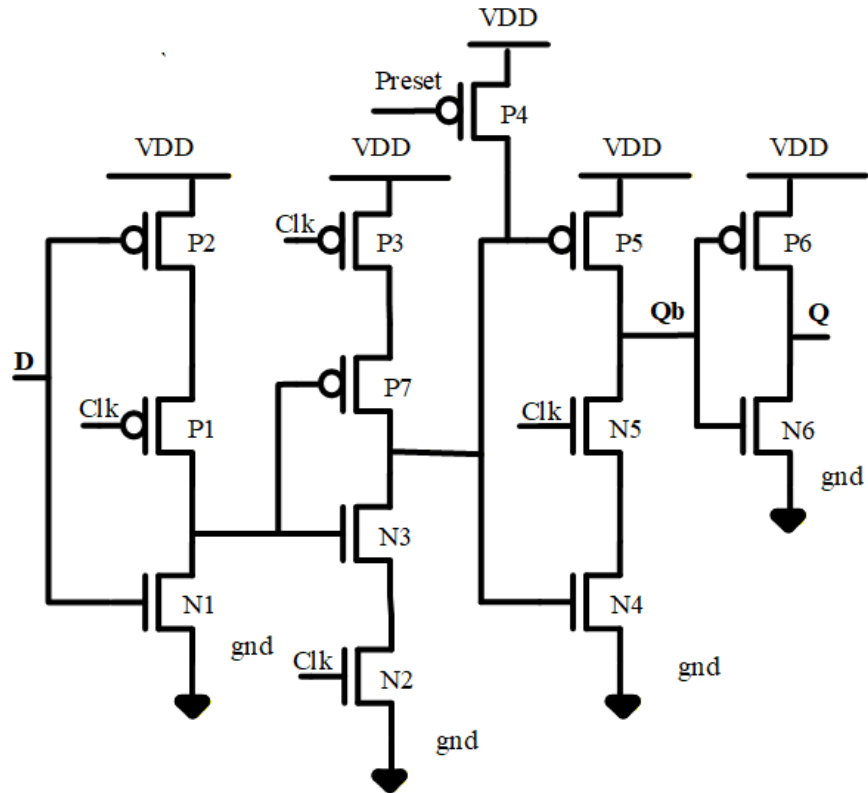


Figure 3.4: Modified TSPC D Flip-Flop Architecture

Further improvements in performance are achieved with the CNTFET implementation of the modified TSPC architecture, including the reduction of leakage current and the improvement of switching characteristics.

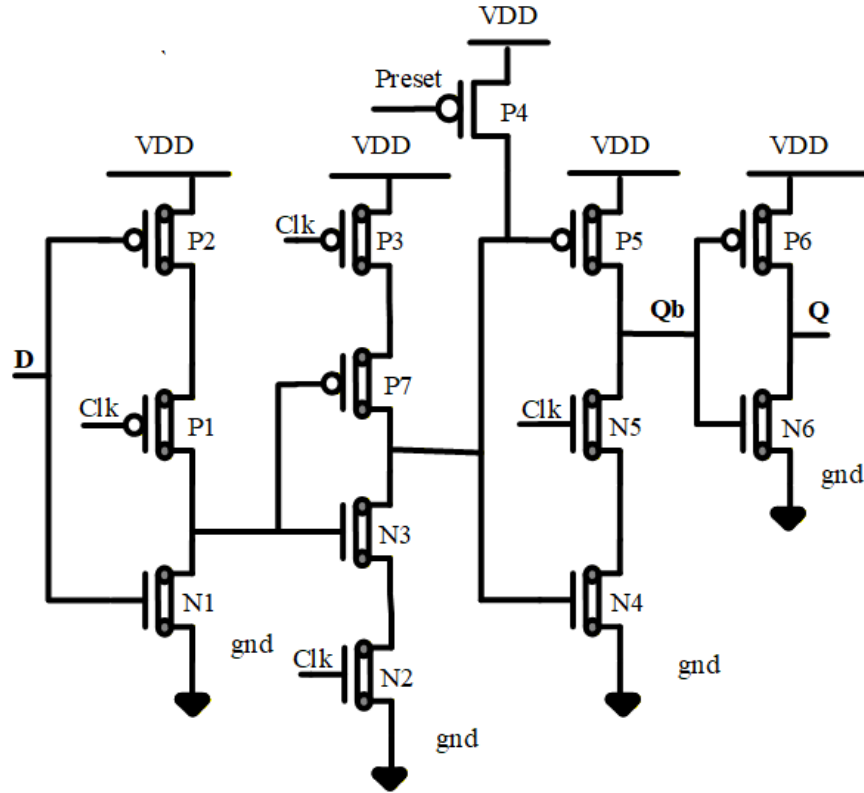


Figure 3.5: CNTFET Based Modified TSPC D Flip-Flop Architecture

3.4 Preset-Enabled Modified TSPC D Flip-Flop Architecture

Preset enabled modified TSPC D flip-flop architecture has been added, with preset functionality to be used for initialising the output state of the circuit. Preset control is used to increase operational flexibility in sequential systems and to control the system initialization when starting up. The design features low power switching characteristics and pre-programmed function. The added control logic enables the output logic to be forced to a desired value when needed. The addition of preset control adds to the complexity of the architecture, but it makes the architecture more reliable and initialization capabilities, thus making it appropriate for advanced sequential applications.

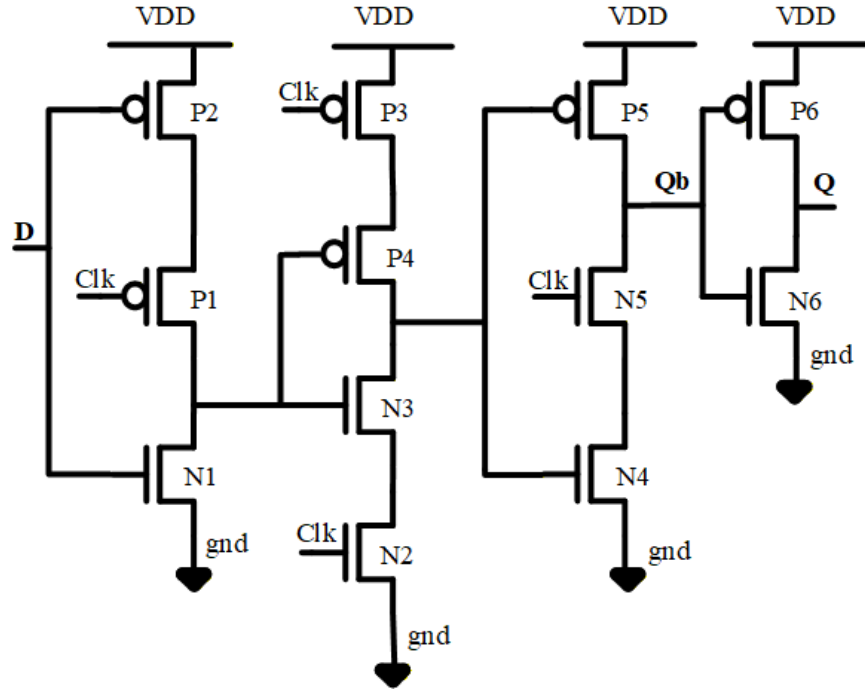


Figure 3.6: Preset-Enabled Modified TSPC D Flip-Flop Architecture

With the architecture designed in this way, the implementation of CNTFET significantly improves the leakage current and propagation delay performance compared to implementation using CMOS.

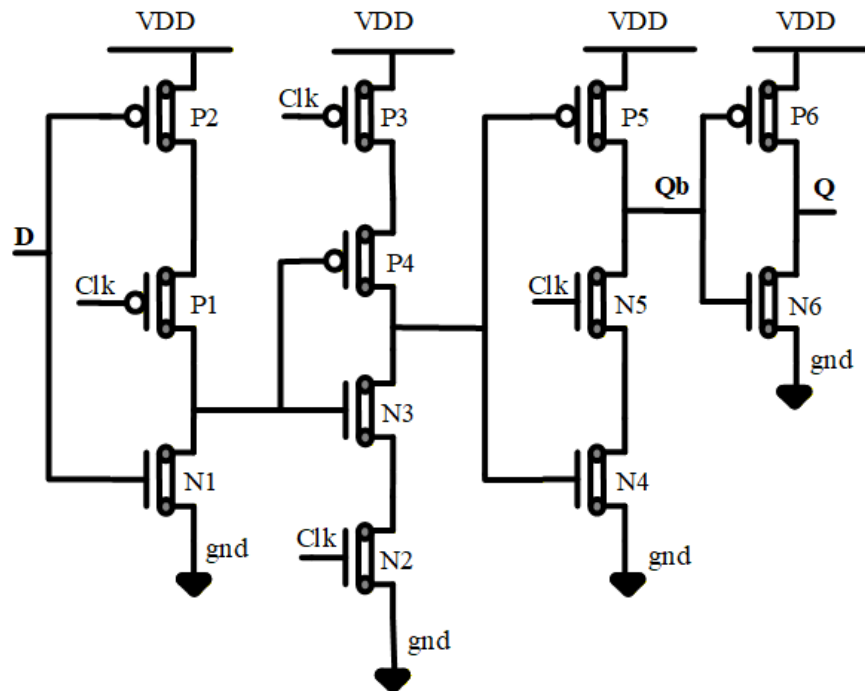


Figure 3.7: CNTFET Based Preset-Enabled Modified TSPC D Flip-Flop Architecture

3.5 Redundant Precharge-Free TSPC D Flip-Flop Architecture

Redundant precharge-free TSPC D flip-flop architecture reduces useless precharge during dynamic operation. Redundant charging and discharging of internal nodes are an important cause of dynamic power dissipation in a conventional dynamic circuit. The redundant precharge-free architecture cuts down on the precharging of unnecessary nodes and decreases dynamic switching activity. This results in lower average power consumption and improved energy efficiency. Its architectural structure has excellent Power Delay Product due to reduced propagation delay and power dissipation. The minimized switching activity makes the architecture very appropriate for low power nano-scale VLSI systems.

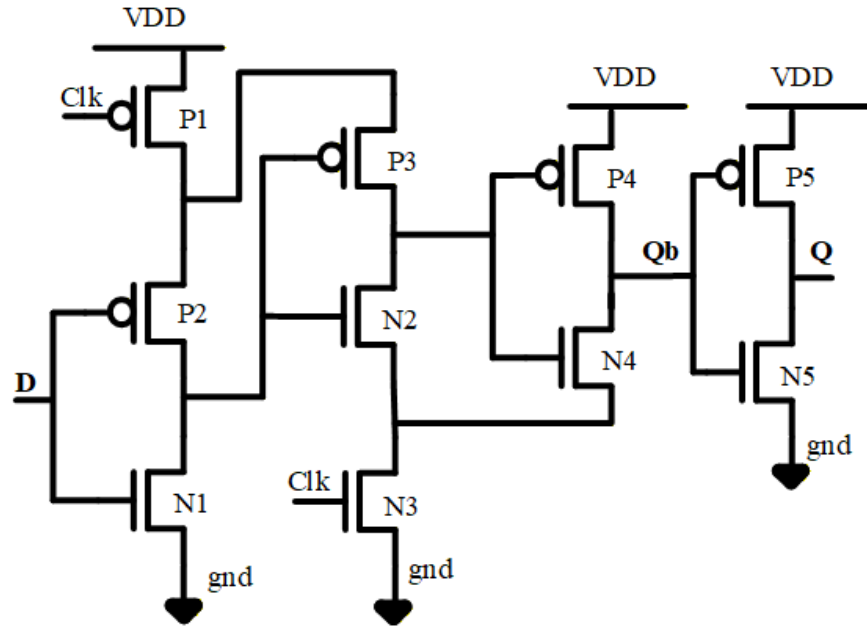


Figure 3.8: Redundant Precharge-Free TSPC D Flip-Flop Architecture

The CNTFET implementation of the redundant precharge-free architecture has enabled additional reductions in the leakage current and propagation delay of the architecture with the superior electrical properties of CNTFET devices.

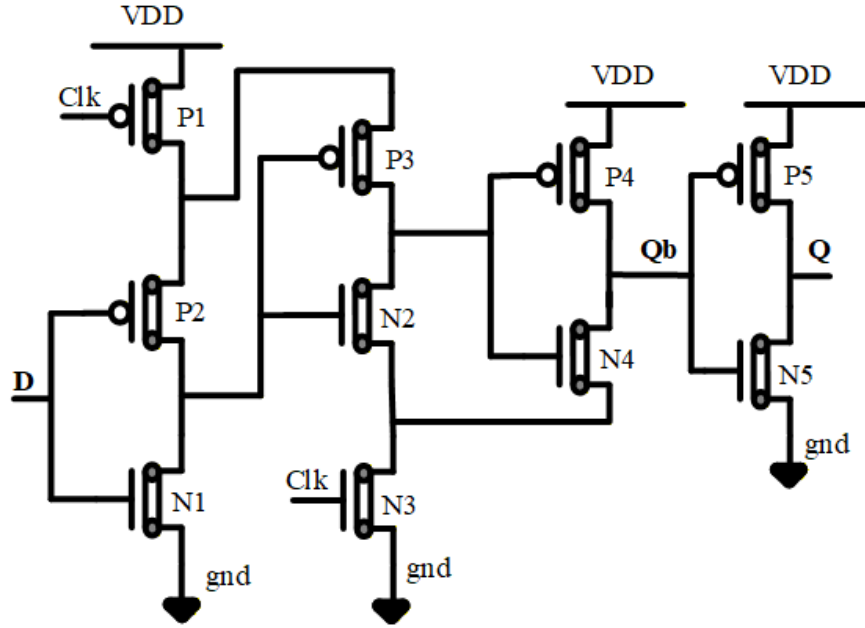


Figure 3.9: CNTFET Based Redundant Precharge-Free TSPC D Flip-Flop Architecture

3.6 CMOS Implementation of TSPC Architectures

The digital design of ICs widely uses CMOS technology due to its low static power consumption and high noise immunity. Here, four TSPC D flip-flops are designed with 22 nm CMOS technology. The CMOS implementations are based on PMOS and NMOS transistors to implement logic functionality. The dimensions and working of the transistors are chosen based on the 22 nm technology parameters. Despite CMOS technology's reliability, as it is scaled to smaller dimensions, leakage current and short channel effects rise. These constraints decrease the energy efficiency of sequential circuits fabricated using CMOS technology.

3.7 CNTFET Implementation of TSPC Architectures

CNTFET technology is regarded as a promising technology other than CMOS for future generation of nano scale integrated circuit. Carbon nanotubes are characterized by very good electrical properties like high carrier mobility, small leakage current, and near-ballistic carrier transport. The CMOS transistors of the TSPC D flip-flop architectures are replaced by CNTFET devices in this work. The implementations of the CNTFETs are done using compact SPICE models for simulation in the HSPICE environment. The switching performance and power consumption of CNTFET devices are improved

due to the electrostatic control and leakage current reduction in CNTFETs compared with CMOS devices. [24], [25]

3.8 Working Principle of TSPC D Flip-Flops

TSPC D flip-flops have just one clock phase to transfer data and to store the operation. The input data is sampled and sent to the output node during the ACTIVE clock transition. High-speed switching operation is made possible by dynamic logic stages. The clocked transistors are reduced in TSPC architectures, which reduces clock loading and hence the overall operational efficiency. Dynamic switching operation also helps to keep the number of transistors and implementation size to a minimum. Dynamic nodes are, however, prone to leakage currents and charge sharing effects and can impact circuit stability at nano-scale dimensions. [31] The key of TSPC architectures is to reduce the redundant switching activity and leakage current.

3.9 Comparative Structural Analysis

The four TSPC D flip-flop designs investigated in this work are different in transistor layout, switching activity (energy) and power minimization methods. The conventional TSPC architecture offers high speed operation in a small transistor arrangement. The TSPC architecture is modified to reduce redundant switches actions and be more energy efficient. The architecture with presets is enabled by introducing initialization functions, and the redundant, precharge-free architecture eliminates the need for unnecessary dynamic transitions. The redundant precharge-free TSPC D flip-flop is likely to deliver superior Power Delay Product performance across all architectures thanks to low switching activity and minimal dynamic power loss.

3.10 Summary

The different TSPC D flip-flops architectures which were taken for comparison in this study were presented in this chapter. All the architectures were discussed and their operational principles and expected performance were explained by both CMOS and CNTFET. The methodology and implementation of this simulation for performance evaluation is explained in the next chapter.

CHAPTER 4

SIMULATION AND RESULTS

4.1 SIMULATION

4.1.1 Introduction

In the field of VLSI circuits, simulation is an important component which is used for testing the performance of VLSI circuits prior to implementation. In this research work, two TSPC based CMOS and CNTFET architectures of D flip-flops are designed and simulated in HSPICE simulation environment. Operating conditions are assumed to be the same for all architectures, so that it is possible to make accurate comparisons between them. In this chapter, the simulation methodology, technology parameters, design environment and performance evaluation techniques employed in this work are presented.

4.1.2 HSPICE Simulation Environment

HSPICE is a widely-used circuit simulation software used to analyze analog and digital integrated circuits. The simulator offers accurate transient, DC and AC analysis for Nano-scale VLSI circuit design. In this work, HSPICE simulation environment is used to implement and evaluate the selected TSPC D flip-flop architectures. The transistor-level circuit designs are used for both CMOS and CNTFET circuits. implementation. The transient analysis is used with HSPICE to analyse the dynamic switching characteristics, propagation delay and power dissipation of the circuits.

4.1.3 22 nm CMOS Technology Parameters

The 22 nm CMOS technology is used to implement all CMOS based TSPC D flip-flop architectures. The transistor models are chosen based on the specifications in the CMOS technology level of the nanoscale.

Table 4.1: Technology Parameters Used for CMOS Simulation

Parameter	Value
Technology Node	22 nm
Supply Voltage	0.8 V
Temperature	25°C
Simulation Tool	HSPICE
Analysis Type	Transient
Simulation Time	20 ns

To ensure a fair comparison of the performance of the architectures, the supply voltage and operating conditions are kept constant. The 22 nm technology has smaller transistors to deliver high integration density and faster switching speed. In addition to leakage current and short-channel effects that impact overall energy efficiency, however, nano-scale CMOS technology presents other challenges.

4.1.4 CNTFET Device Model Parameters

Table 4.2: CNTFET Simulation Parameters

Parameter	Value
Technology Node	22 nm
Channel Material	Carbon Nanotube
Supply Voltage	0.8 V
Temperature	25°C
Simulation Tool	HSPICE
Analysis Type	Transient
Simulation Time	20 ns

Compact CNTFET SPICE models are used to implement the CNTFET based TSPC D flip- flop architectures. Carbon nanotube devices have high carrier mobility and near-ballistic transport, leading to higher switching performance. The CNTFET models used in the present work can be used with HSPICE simulation environment and are suitable for nano-scale circuit analysis. The device parameters are chosen based on the standard parameters of the CNTFET technology. The leakage current and power dissipation of the CNTFET devices are lower than that of the conventional CMOS transistors. The above features make CNTFET technology well suited for low power high speed VLSI systems.

4.1.5 Simulation Setup and Design Flow

The chosen TSPC D flip-flop architectures are implemented at the transistor level with HSPICE netlists. For CMOS implementation, both PMOS and NMOS transistors are used, whereas for CNTFET implementation, MOS devices are replaced by CNTFET transistors. All circuits are simulated under same operating conditions so that the performance of the circuits can be evaluated in a consistent manner. The input clock signals and data pulses are used to investigate the dynamic behaviour of the circuits. The design flow adopted in the present work consists of schematic implementation, set up of the transient analysis, checking of the waveforms, performance measurement and comparison.

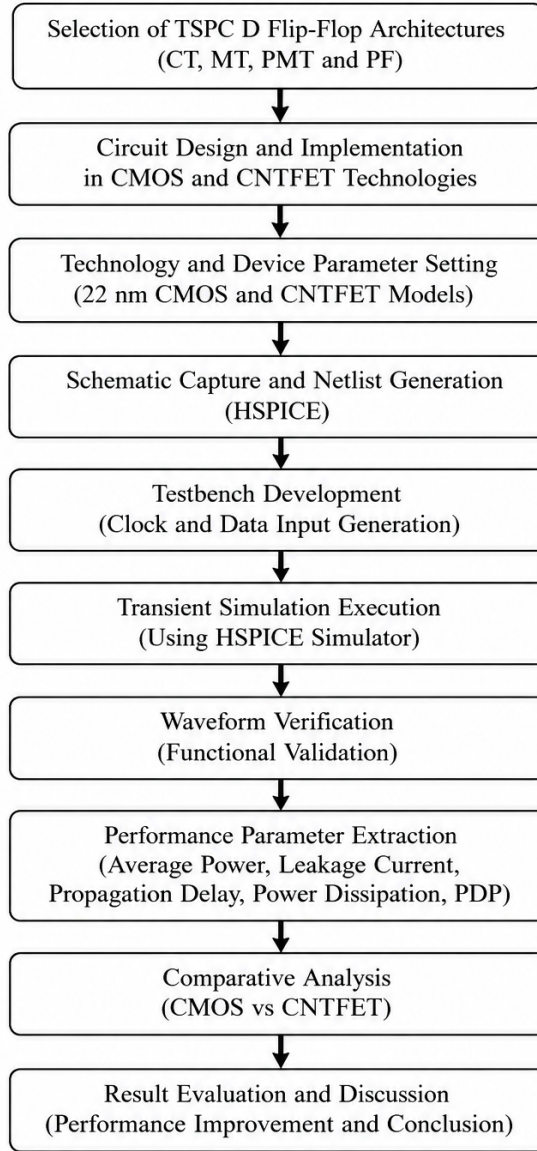


Figure 4.1: Simulation Flow for CMOS and CNTFET Based TSPC D Flip-Flop Architectures

4.1.6 Transient Analysis Methodology

Transient analysis is done to investigate the dynamic switching behavior of the TSPC D flip-flop architectures. The transient responses of the circuits are looked at with the clock and data input signals. Waveforms from the output are examined to ensure proper operation of the D flip-flops. Propagation delay and dynamic power consumption are obtained during switching operation. The transient analysis also enables the assessment of the stability and switching performance of the architectures based on CMOS and CNTFET.

4.1.7 Input Pulse and Clock Signal Configuration

The circuits are tested for functionality with clock signals and input data pulses to evaluate their performance characteristics. Data transfer operation of the TSPC D flip-flops is controlled by the clock signal. The pulse parameters are determined to guarantee the correct switching transitions and delay and the power consumption are measured correctly. All the CMOS and CNTFET architectures follow the same clock frequency and the same pulse width. The circuits were tested for functionality and transient responses to clock signals and input data pulses. For fair comparative evaluation both the CMOS based architecture and the CNTFET based architecture were operated with the same pulse configuration and operating conditions.

4.1.8 Measurement of Average Power Consumption

Average power consumption is one of the most crucial parameters in low power VLSI circuit design. Transient switching operation measurement of power consumption by using the supply current analysis. The average power is the product of the supply voltage and average current from the power supply during operation of the circuit. The equation used for average power calculation is given as:

$$P_{avg} = V_{DD} \times I_{avg} \quad (4.1)$$

Where: Where: P_{avg} is the average power consumption, V_{DD} is the supply voltage and I_{avg} is the average supply current. A lower average power consumption means that the circuit is more energy efficient.

4.1.9 Leakage Current Measurement Methodology

In nano-scale very large-scale integrated (VLSI) systems, leakage current is a significant component of power consumption. To assess static power characteristics of the TSPC D flip-flop architectures, the leakage current is measured. When the circuit is in inactive switching condition, the leakage current is observed. Small leakage current means a good static power performance. The devices based on CNTFET are expected to have a much lower leakage current than CMOS devices due to the electrostatic control.

4.1.10 Propagation Delay Measurement

Propagation delay represents the time required for the output signal to respond to changes in the input signal. In sequential circuits, propagation delay directly affects operating frequency and switching performance. Propagation delay is the time it takes

for the output signal to react to the change in the input signal. The propagation delay is significant in the operation frequency and switching speed of sequential circuits. Propagation delay is calculated from 50% level of the input and output pulses. A lower propagation delay means the switching speed is faster and high frequency performance is better. The propagation delay equation in this work is:

$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2} \quad (4.2)$$

Where: Where: t_{PLH} is the low to high transition delay and t_{PHL} is the high to low transition delay.

4.1.11 Power Dissipation Measurement Methodology

The energy dissipation is a critical parameter of sequential circuits for energy efficiency evaluations in nano-scale VLSI system. The power dissipation of CMOS and CNTFET based TSPC D flip-flop architectures were analyzed by transient analysis in HSPICE simulation environment. The same operating conditions and input pulses were used in all circuits to facilitate meaningful comparison. The power consumption was calculated by observing the current taken from the power supply when switching. The power dissipation of the circuits is the sum of the dynamic switching activity and the static leakage power. The lower the power dissipation, the more efficient the circuit, the less heat is generated, and the more efficient it will be for use in low-power high-speed digital circuits.

The power consumption was determined by analyzing the current drawn from the power supply during switching operation. Both dynamic switching activity and static leakage effects contribute to the overall power dissipation of the circuits. Lower power dissipation indicates improved circuit efficiency, reduced heat generation, and better suitability for low-power high-speed digital applications.

4.1.12 Power Delay Product Calculation

One of the key parameters for measuring the energy efficiency of digital circuits is Power Delay Product. The energy consumed in one switching operation is given by PDP. Generally, lower PDP means higher energy efficiency and better overall performance of circuits. [34] The Power Delay Product equation is given as:

$$PDP = P_{avg} \times t_{pd} \quad (4.3)$$

Where: Where: P_{avg} is the average power consumption, t_{pd} is propagation delay.

4.1.13 Performance Evaluation Parameters

Four important parameters are used to perform the analysis of the performance in this work: 1. Average Power Consumption

2. Leakage Current

3. Propagation Delay

4. Power Dissipation

5. Power Delay Product

These parameters are chosen because they have direct influence on the functionality of sequential circuits in terms of energy efficiency and switching.

4.1.14 Simulation Conditions and Assumptions

The simulation of all CMOS and CNTFET based TSPC D flip-flop architectures is performed under same operating conditions. Each supply voltage, temperature, simulation time and clock configuration are kept constant during the analysis. The performance evaluation is only for simulation-based analysis and conducted in the HSPICE environment. This work does not take into account process variation and fabrication-related effects.

4.1.15 Summary

The methodology and implementation details of the simulation of TSPC D flip-flop architectures using CMOS and CNTFET are introduced in this chapter. The HSPICE simulation environment, technology parameters, transient analysis methodology and performance evaluation techniques were discussed.

4.2 RESULTS

4.2.1 Introduction

The simulation results for CMOS and CNTFET based TSPC D flip-flop architectures at 22 nm technology node are presented in this chapter. The performance evaluation is done using the simulation environment of HSPICE with the same operating conditions. The important parameters like Average Power Consumption, Leakage current, Propagation Delay and Power Delay Product are used to perform the comparative analysis. The outcomes from the simulations prove the advantages of CNTFET technology for sequential circuits at low power consumption and high speed.

4.2.2 Functional Verification of TSPC D Flip-Flops

The transient response analysis of CMOS and CNTFET based TSPC D flip-flop architectures was carried out using HSPICE simulation environment in order to verify the functional correctness of the circuits. All the architectures were simulated under the same conditions by applying clock pulse and input data signals to all of them. The output waveforms show that the designed TSPC D flip-flops are working sequentially correctly. The plot of the waveform shows that the output signal tracks the input data only during the rising edge of the clock, thereby witnessing the proper functioning of the sequential circuits. The generated waveforms also show stable switching characteristics, with correct logic transitions and minimal distortion of the signals.

4.2.3 Conventional TSPC D Flip-Flop Waveforms

Transient response of the conventional TSPC D flip-flop architecture validates the data transfer operation with the active clock phase. The output transitions for the applied input signal are correct for both CMOS and CNTFET implementations.

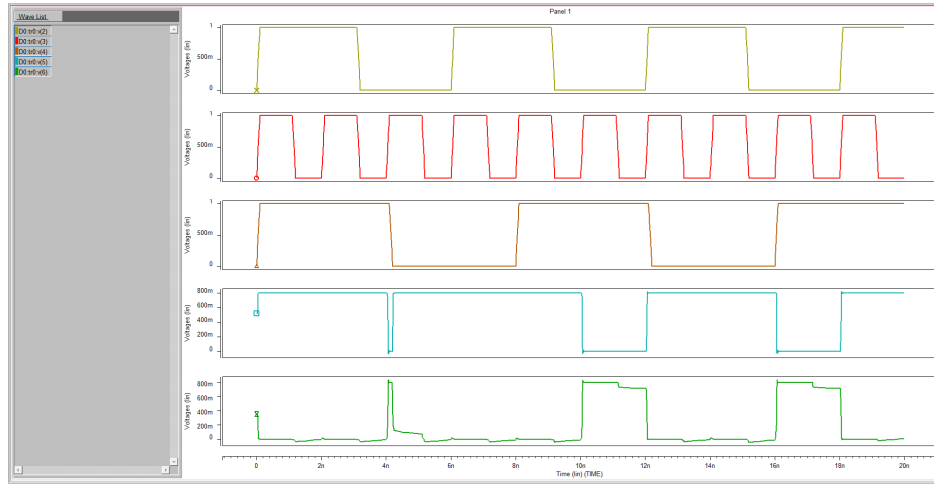


Figure 4.2: CMOS Based Conventional TSPC D Flip-Flop Waveform

The output response time of the conventional TSPC architecture based on CNTFETs is smaller than that of CMOS-based TSPC architecture, showing better carrier mobility and switching resistance of CNTFET devices.

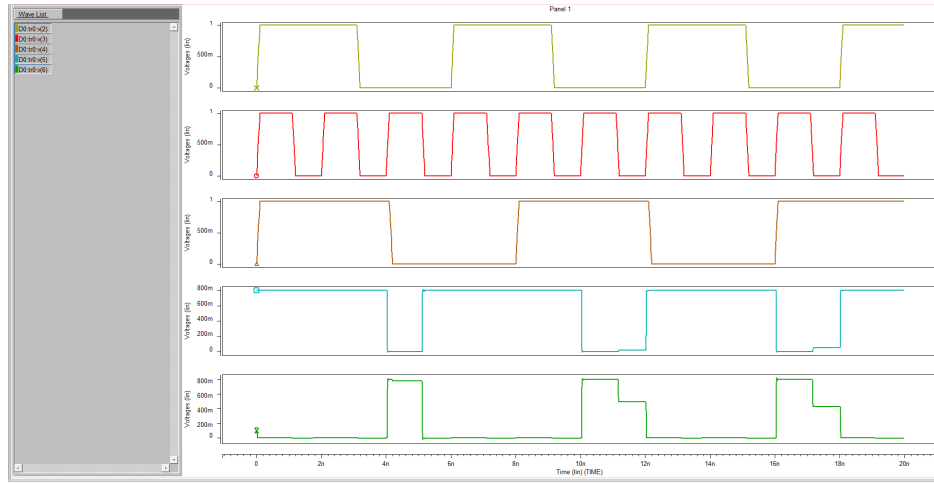


Figure 4.3: CNTFET Based Conventional TSPC D Flip-Flop Waveform

4.2.4 Modified TSPC D Flip-Flop Waveforms

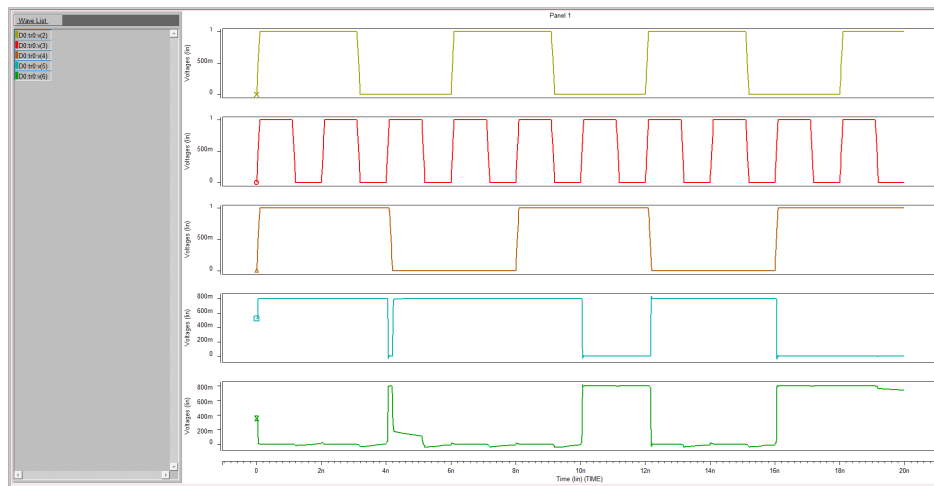


Figure 4.4: CMOS Based Modified TSPC D Flip-Flop Waveform

The modified TSPC D flip-flop architecture shows better switching behavior with minimum redundant node switching. The waveform analysis shows that the output transitions are stable with lower amount of dynamic switching activity.

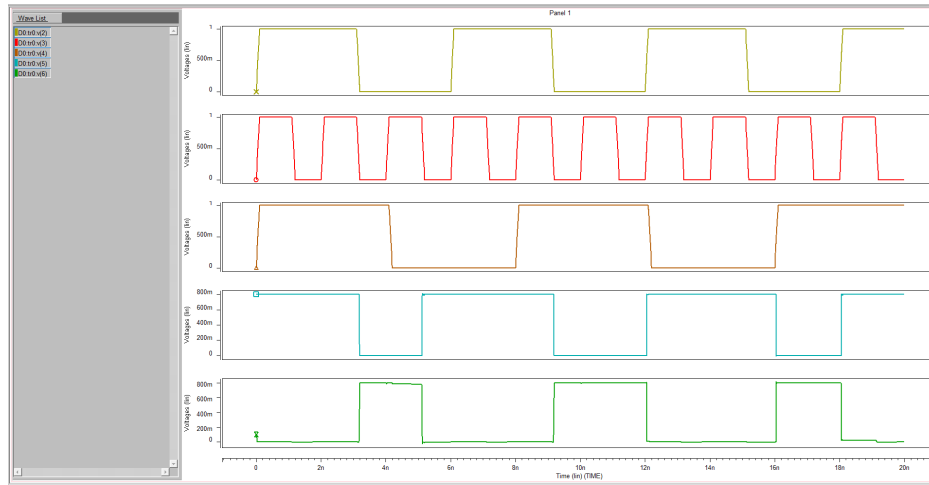


Figure 4.5: CNTFET Based Modified TSPC D Flip-Flop Waveform

The propagation delay and transition characteristics of the CNTFET implementation are improved over CMOS implementation. Less switching activity leads to lower power dissipation and better energy efficiency.

4.2.5 Preset-Enabled Modified TSPC D Flip-Flop Waveforms

The modified TSPC D flip-flop with preset confirms appropriate data transfer from preset and sequential operation when analyzed with the waveform analysis feature. The output state gets initialized to a value which is correct when simulated.

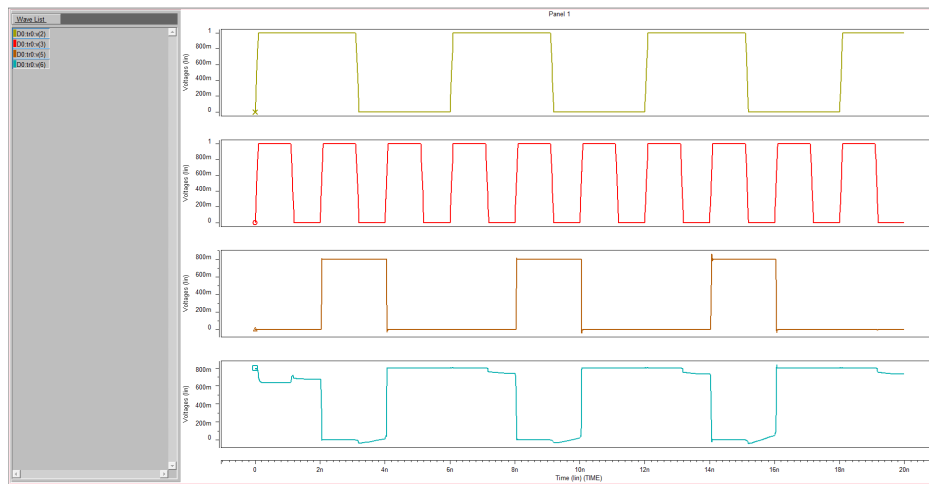


Figure 4.6: CMOS Based Preset-Enabled Modified TSPC D Flip-Flop Waveform

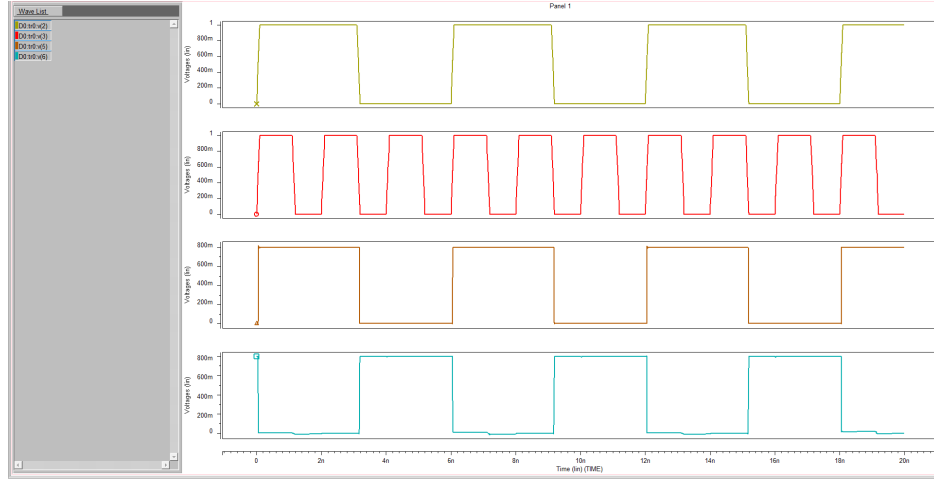


Figure 4.7: CNTFET-Based Preset-Enabled Modified TSPC D Flip-Flop Waveform

The CNTFET implementation demonstrates significantly improved switching speed and reduced propagation delay compared to CMOS implementation. Stable waveform transitions validate the reliability of the preset-enabled architecture.

4.2.6 Redundant Precharge-Free TSPC D Flip-Flop Waveforms

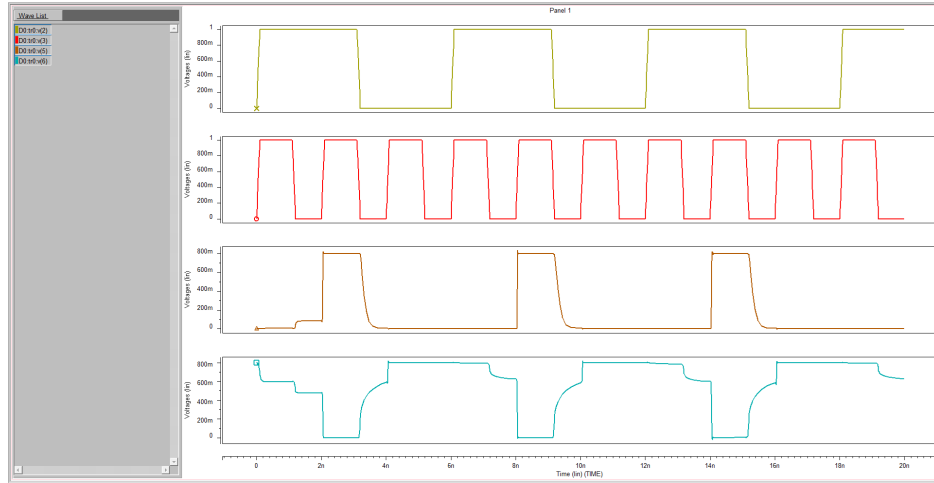


Figure 4.8: CMOS Based Redundant Precharge-Free TSPC D Flip-Flop Waveform

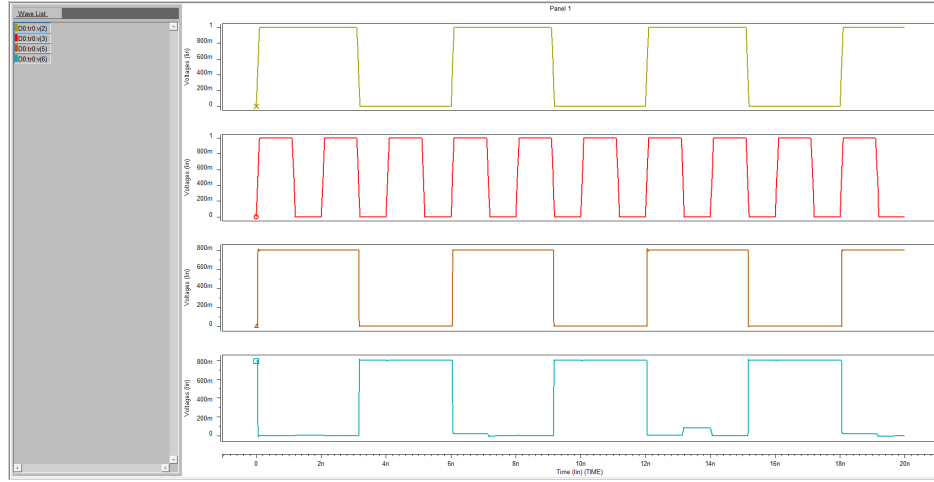


Figure 4.9: CNTFET Based Redundant Precharge-Free TSPC D Flip-Flop Waveform

The redundant precharge-free TSPC D flip-flop architecture has the characteristics of minimum unnecessary switching transitions during transients. The waveform analysis also shows enhanced dynamic behaviour and diminished redundant charging activity. The CNTFET based implementation has faster output transitions and a more stable output waveforms than the CMOS implementation. Less switching activity is a key factor in lower power consumption and better Power Delay Product.

4.2.7 Discussion of Waveform Analysis

All the architectures of CMOS and CNTFET based TSPC D flip-flop are verified to be functionally correct using the waveform analysis. In all the implementations of the CNTFET, the switching speed, propagation delay, and output transition characteristics have been found to be better than the CMOS circuits. The observed waveform behavior confirms the usefulness of CNTFET technology in high speed and low power sequential circuit applications. The transient response and switching characteristics of the TSPC D flip-flop with a redundant precharge free CNTFET is the most stable among all the designs.

4.2.8 Comparative Analysis of Average Power Consumption

According to the simulation results, the average power of CNTFET based TSPC D flip-flop architecture is significantly lower than the average power of CMOS based TSPC D flip-flop architecture. The reason for the decrease in the average power consumption is primarily attributed to the excellent electrical properties of the carbon nanotube transistors, such as high carrier mobility, low switching losses and near ballistic charge transport properties. Such properties allow CNTFET devices to use less switching

energy or have a better energy efficiency. The conventional TSPC architecture, the average power consumption of the CNTFET implementation is about 15% lower than that of the CMOS implementation.

In the same vein, the TSPC tweaked architecture shows almost a 20.98% reduction in the average power dissipation. The architectures with precharge enabled preset mode shows more significant improvement with average power reduction of 28.18% and 82.39% for the modified TSPC and redundant precharge-free architectures, respectively. The significant reduction in the precharge-free architecture is mainly attributed to the minimization of redundant switching activity along with reduction in the dynamic node transitions. The redundant precharge-free CNTFET based TSPC D flip-flop has the lowest average power consumption among all investigated architectures and is thus quite appropriate for ultra-low power VLSI applications.

Table 4.3: Comparative Analysis of Average Power Consumption

Architecture	CMOS Power (W)	CNTFET Power (W)
Conventional TSPC	1.00E-06	8.50E-07
Modified TSPC	1.02E-06	8.06E-07
Preset Modified TSPC	9.90E-08	7.11E-08
Precharge-Free TSPC	4.06E-07	7.15E-08

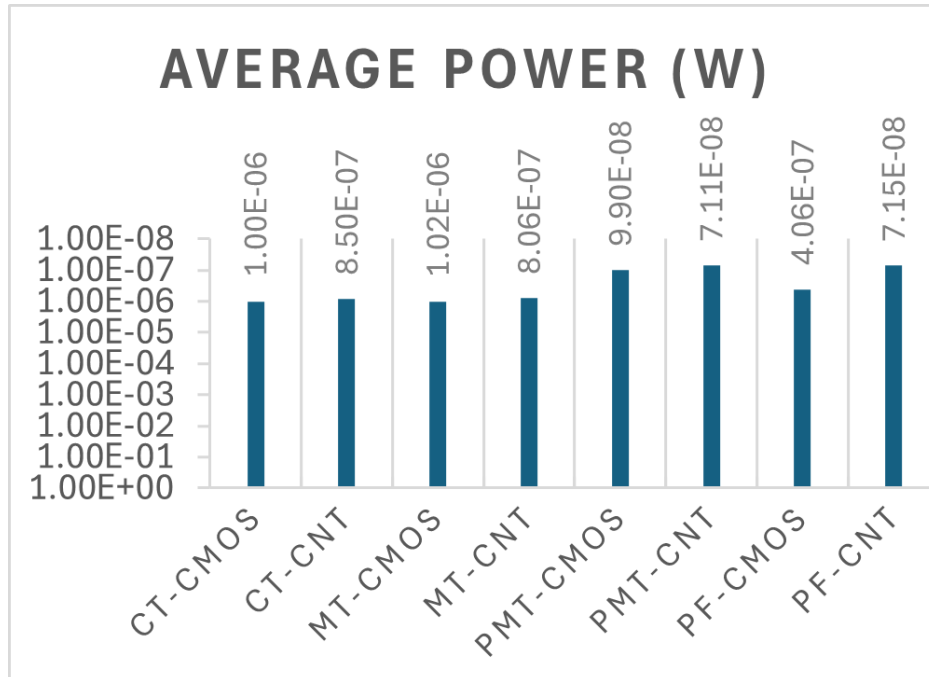


Figure 4.10: Comparative Average Power Analysis

4.2.9 Comparative Analysis of Leakage Current

Due to aggressive scaling of transistors and short channel effect, leakage current is one of the most important problems in the nano-scale CMOS technology. The simulation analysis clearly shows that the leakage current of an architecture based on the CNT-FET is significantly lower than the leakage current of the conventional CMOS based architecture.

Table 4.4: Comparative Analysis of Leakage Current

Architecture	CMOS Leakage (A)	CNTFET Leakage (A)
Conventional TSPC	2.01E-06	2.35E-09
Modified TSPC	2.01E-06	2.36E-09
Preset Modified TSPC	1.24E-08	2.58E-10
Precharge-Free TSPC	8.61E-09	2.52E-10

The leakage current of the conventional and modified CNTFET based TSPC architectures is about 99.88% less compared to CMOS circuits. Likewise, the leakage current reduction in the modified and redundant precharge-free CNTFET architectures are found to be nearly 97.92% and 97.07% respectively. The significant drop in leakage current can be explained by the enhanced electrostatic channel control, and short channel effect suppression in CNTFET devices. Lower leakage current directly helps to reduce energy dissipation due to static power. The results obtained indicate that the CNTFET technology is very promising for the design of low leakage sequential circuits in future nano-scale integrated systems.

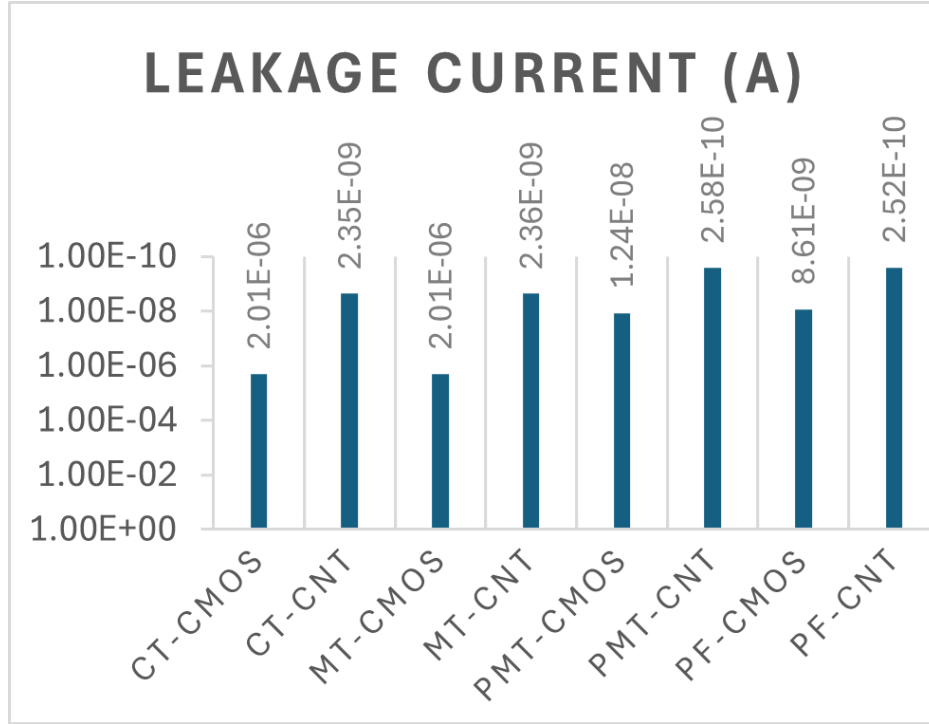


Figure 4.11: Comparative Leakage Current Analysis

4.2.10 Comparative Analysis of Power Dissipation

The power dissipation analysis also confirms the suitability of CNTFET technology in low power VLSI applications. The CNTFET based TSPC architectures exhibit extremely low power consumption when compared with the CMOS based ones under the same simulation conditions. The power dissipation of the two architectures (conventional and modified CNTFET) is reduced by nearly 99.88%. Likewise, the modified and redundant precharge-free CNTFET architectures with preset show around 97.91% and 97.07% reduction in power dissipation, respectively.

Table 4.5: Comparative Analysis of Power Dissipation

Architecture	CMOS Power Dissipation (W)	CNTFET Power Dissipation (W)
Conventional TSPC	1.60E-06	1.88E-09
Modified TSPC	1.60E-06	1.89E-09
Preset Modified TSPC	9.91E-09	2.07E-10
Precharge-Free TSPC	6.89E-09	2.02E-10

This diminution in power dissipation can be attributed primarily to the significant decrease in switching energy, leakage current and the enhancement in the transport

efficiency of the carbon nanotube devices.

Low power consumption prevents the problem of thermal effects and increases the reliability of the operation of integrated circuits.

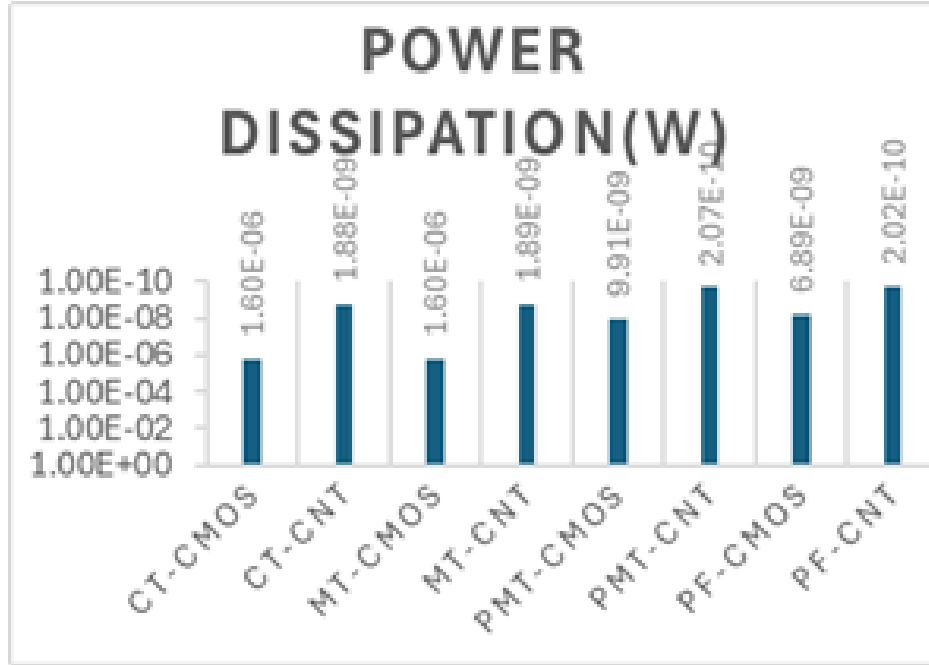


Figure 4.12: Comparative Power Dissipation Analysis

The above properties render the CNTFET based TSPC D flip-flops highly desirable in battery-powered portable electronic systems and as a component in high-density low-power integrated circuits.

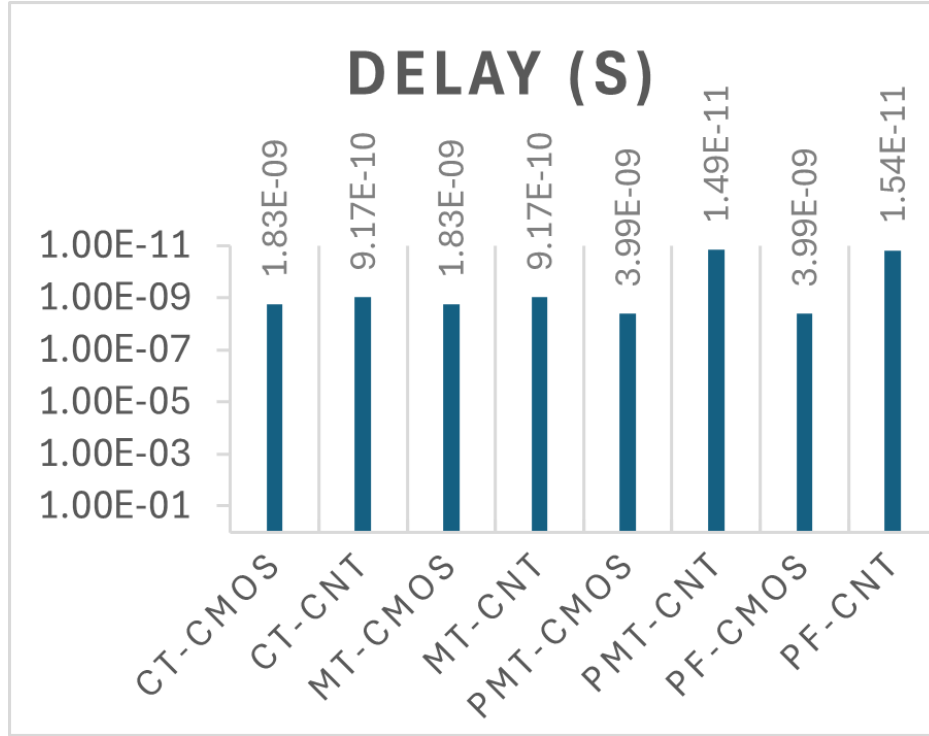
4.2.11 Comparative Analysis of Propagation Delay

Propagation delay is an important parameter for evaluating the switching speed of sequential circuits. A smaller propagation delay means the circuit can operate faster and perform better. The simulation results show that the proposed CNTFET based architectures run much faster than the CMOS based architectures. The propagation delay of the conventional and modified CNTFET is reduced by nearly 49.89% when compared with the CMOS circuits. In the case of precharge-free architectures with precharge-sets, significant delay reduction is seen: up to 99.63% in precharge-set enabled modified and up to 99.61% in precharge-set enabled redundant.

Table 4.6: Comparative Analysis of Propagation Delay

Architecture	CMOS Delay (s)	CNTFET Delay (s)
Conventional TSPC	1.83E-09	9.17E-10
Modified TSPC	1.83E-09	9.17E-10
Preset Modified TSPC	3.99E-09	1.49E-11
Precharge-Free TSPC	3.99E-09	1.54E-11

High carrier mobility and near-ballistic transport mechanism in CNTFET devices are the key factors responsible for superior delay performance, as it allows charge transport to happen quickly and switching time to be reduced.

**Figure 4.13:** Comparative Propagation Delay Analysis

The propagation delay of the preset-enabled modified CNTFET based TSPC D flip-flop is the minimum among all the architectures which can be used for high-speed digital applications.

4.2.12 Comparative Analysis of Power Delay Product

Power Delay Product is the overall efficiency of digital circuits, combining the power consumed and propagation delay. Smaller values of PDP means more efficient circuits and less energy consumed during switching operation. The simulation results show

that the PDP improvement is significant in the CNTFET based architectures than the CMOS based architectures. The conventional CNTFET architecture shows good improvement with PDP of around 57.43%, and the modified CNTFET architecture shows an improvement of almost 60.48%.

Table 4.7: Comparative Analysis of Power Delay Product

Architecture	CMOS PDP (J)	CNTFET PDP (J)
Conventional TSPC	1.83E-15	7.79E-16
Modified TSPC	1.87E-15	7.39E-16
Preset Modified TSPC	3.95E-16	1.06E-18
Precharge-Free TSPC	1.62E-15	1.10E-18

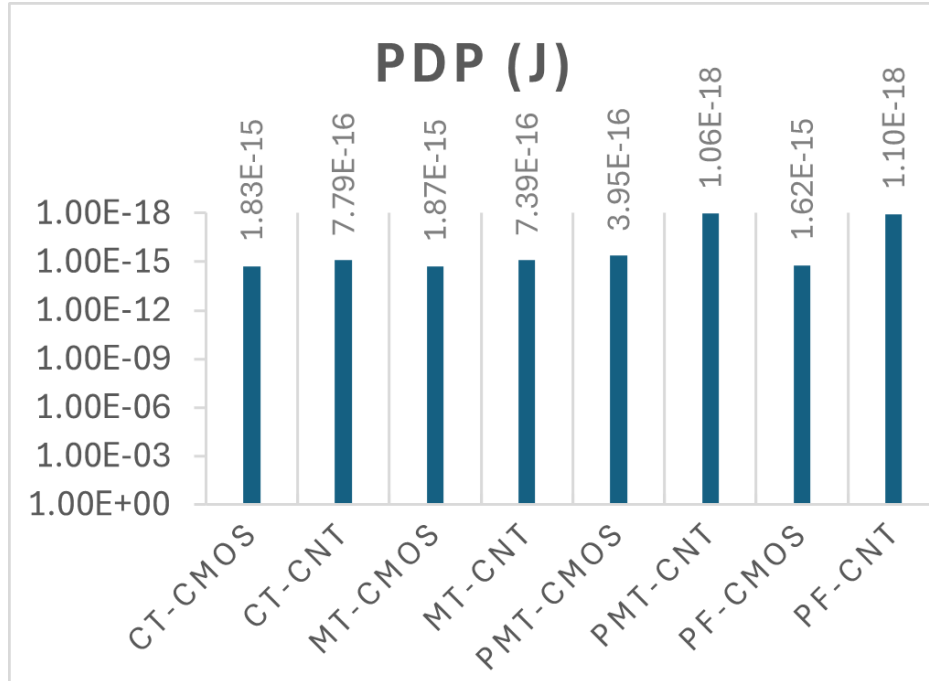


Figure 4.14: Comparative PDP Analysis

The modified architecture and redundant architecture with precharge feature are presented and modified by introducing the redundant architecture and precharge feature into the CNTFET, respectively. They show the remarkable PDP improvements of about 99.73% and 99.93%, respectively. The findings demonstrate that CNTFET technology can enable the high-speed performance with ultra-low power consumption. The TSPC D flip-flop designed using the redundant precharge-free CNTFET circuit has a minimum value of PDP among all the analyzed circuits, so it is the best overall energy efficient circuit.

4.2.13 Percentage Improvement Analysis

The percentage improvement gained by CNTFET implementations is done by comparing the architecture of CMOS and CNTFET.

Table 4.8: Percentage Improvement of CNTFET Based Architectures over CMOS

Parameter	CT Improvement	MT Improvement	PMT Improvement	PF Improvement
Average Power	15.00%	20.98%	28.18%	82.39%
Leakage Current	99.88%	99.88%	97.92%	97.07%
Power Dissipation	99.88%	99.88%	97.91%	97.07%
Delay	49.89%	49.89%	99.63%	99.61%
PDP	57.43%	60.48%	99.73%	99.93%

The results indicate that the switching performance and energy efficiency of CNTFET technology is significantly better than conventional CMOS technology.

4.2.14 Discussion on Energy Efficiency

The decreased average power consumption and less leakage current of CNTFET based architectures play significant role in increasing energy efficiency. Lower power dissipation is achieved in the precharge-free architecture due to the low switching activity. The overall switching characteristic of the sequential circuits is enhanced by the superior electrical properties of CNTFET devices like near ballistic transport and high carrier mobility. The redundant precharge-free CNTFET based TSPC D flip-flop has the most balanced performance among all the analyzed architectures, owing to its least switching activity and optimal propagation characteristics.

4.2.15 Comparative Summary of All Architectures

The comparison clearly indicates that the technology of CNTFET is superior to the CMOS technology in the architectures of TSPC nano-scale flip-flops. Power Delay Product characteristics are consistently better, switching speeds are faster, leakage current is significantly reduced, power dissipation is lower and average power consumption is lower with CNTFET based designs. The CNTFET is designed with redundant architecture which has no need for precharge, and it shows the best overall performance due to its very low power consumption and minimum PDP value. Likewise, the delay performance and high speed operation of the modified CNTFET architecture with preset

are excellent. Obtained simulation results confirm the potential application of CNTFET technology in future low power and high speed VLSI system. CNTFET based sequential circuits are able to offer an effective solution to design powerful energy efficient nano-scale integrated circuits as CMOS scaling hits its physical restrictions.

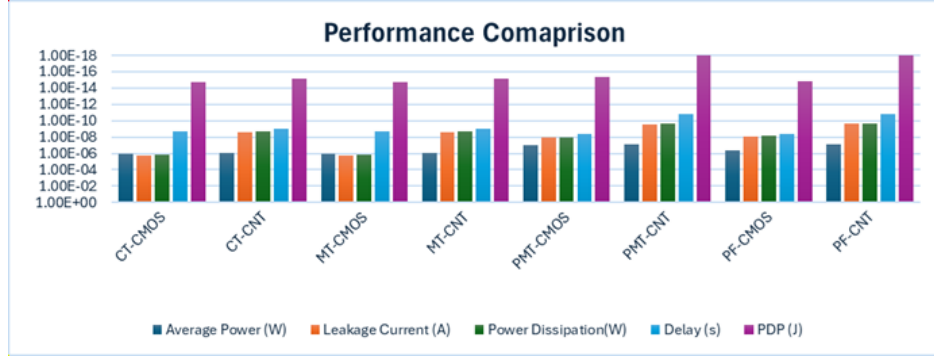


Figure 4.15: Performance comparison of all parameters

4.2.16 Limitations of the Present Work

The present work deals with the simulation based evaluation of the performance and the simulation is carried out using HSPICE environment. The present work does not take into account the process variations, fabrication difficulties and manufacturing limitations of CNTFET technology. The analysis is restricted to four architectures of TSPC D flip-flop at 22 nm technology node. In this research, the temperature variation analysis and process reliability analysis are not considered.

4.2.17 Summary

In this chapter, comparative performance analysis of the CMOS and CNTFET based TSPC D flip flop architectures was presented. According to the simulation results, the implementations of CNTFET can be used to reduce power consumption, leakage current, propagation delay and also to enhance the characteristics of propagation delay and power dissipation in comparison with the CMOS implementations. The conclusion and future scope of the research work is discussed in the next chapter.

CHAPTER 5

CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

5.1 Conclusion

This thesis compared the performance of CMOS and CNTFET based TSPC D flip-flops (DFFs) at 22nm technology level. Four different TSPC D flip-flop architectures are implemented and analyzed in HSPICE simulation environment: conventional TSPC, modified TSPC, preset-enabled modified TSPC and redundant precharge-free TSPC D flip-flop architectures. This comparative analysis is carried out for crucial performance parameters like Average power consumption, Leakage current, Propagation delay and Power Delay Product. From the simulation results, it is clearly seen that the performance of the CNTFET based architectures is far better than that of the CMOS based architectures.

The CNTFET implementations were able to reduce the average power consumption of the products, thanks to the reduced switching losses and to the improvement of the characteristics of the carrier transport. In addition, the leakage current was found to be reduced in all of the CNTFET based architectures, due to the superior electrostatic control and reduced short channel effects. The propagation delay analysis result showed Faster switching performance of CNTFET based TSPC D flip-flops as compared to CMOS circuits. The sequential circuits have better speed characteristics because of the lower channel resistance and high carrier mobility of CNTFETs.

The redundant precharge-free CNTFET based TSPC D flip-flop gave the best overall performance with minimum Power Delay Product when analyzed architectures. The unnecessary switching activity and dynamic node transitions were reduced to greatly enhance energy efficiency of the circuit. From the results obtained from this work, it is concluded that CNTFET technology is a potential future alternative to the conventional CMOS technology for future VLSI devices for low power and high speed applications.

5.2 Major Contributions of the Thesis

The significant contribution of this research work is summarized as follows:

1. Four different architectures for TSPC D flip-flop with CMOS and CNTFET technologies.
2. 22nm performance evaluation with the same simulation conditions in the HSPICE environment.
3. Analysis based on average power consumption, leakage current, propagation delay and Power Delay Product.
4. Redundant precharge-free CNTFET based TSPC D flip-flop (DFF) identified as the most energy efficient architecture.
5. Illustrating the benefits of the CNTFET over the future and the sequential circuits.

5.3 Future Scope

While the CNTFET based TSPC D flip-flop architectures showed better performance for this work, there are still some opportunities for future research. Future research could be regarding hybrid architectures of CMOS-CNTFET to get the most optimized trade-off between fabrication compatibility and performance improvement. Using CNTFET technology, some advanced sequential circuits like dual-edge triggered flip-flops and pulse triggered circuits can be studied as well. Process variation analysis, temperature variation analysis, noise analysis and reliability evaluation of CNTFET based circuits are some of the other areas for further studies. Practical VLSI applications to the physical implementation and fabrication issues of CNTFET technology can be further discussed. Also, ultra-low-power integrated systems using low-power CNTFET circuits, memory systems and processor architectures can also be explored.

5.4 Applications in Nano-Scale VLSI Systems

The sequential circuits based on CNTFET can be used efficiently in a modern nanoscale VLSI system to achieve low power consumption and high speed operation. Architectures discussed in this paper can be used in microprocessors, memories, portable electronics, communication and digital signal processing circuits. With low leakage current and energy dissipation, the circuits based on CNTFET are also power-budget sensitive, and hence suitable for battery-operated applications and energy-efficient computer systems.

5.5 Social and Technological Impact

With the growing demand for portable and energy-efficient electronic devices, new low-power technologies are needed. Power consumptions of modern electronic circuits can be reduced significantly by using CNTFET based sequential circuits. Improved energy efficiency helps in reducing heat generation and increasing battery life of portable electronic devices. By cutting down on energy usage, reduced power usage also helps keep computing systems environmentally friendly. Advanced nano-scale technologies like CNTFET can facilitate the research for future generations of AI hardware, high performance computing systems, and future communication technologies.

5.6 Final Remarks

This work successfully illustrated the benefits of CNTFET technology to the TSPC D flip flop architectures for low power high speed applications. From the simulation results, it is seen that the performance of CNTFET based sequential circuits are better than the conventional CMOS sequential circuits. The results of this study suggest that CNTFET technology has significant promise of future application in high speed, energy-efficient, nano-scale VLSI systems.

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APPENDIX-I

CT - CMOS HSPICE NETLISTS

This appendix presents the CMOS HSPICE netlists used for the simulation of conventional TSPC D flip-flop architectures. Similarly you can get the other CMOS netlist just the node coding should be kept in mind for circuit representation.

I.1 CMOS based Conventional TSPC D Flip-Flop HSPICE Netlist

```
.option post
.option ingold=2
.probe

VDD 1 0 DC 0.8
M1 8 3 9 9 PMOS W=44n L=22n
M2 9 2 1 1 PMOS W=44n L=22n
M3 7 3 1 1 PMOS W=44n L=22n
M4 7 4 1 1 PMOS W=44n L=22n
M5 6 7 1 1 PMOS W=44n L=22n
M6 5 6 1 1 PMOS W=44n L=22n

M7 8 2 0 0 NMOS W=44n L=22n
M8 10 3 0 0 NMOS W=44n L=22n
M9 7 8 10 10 NMOS W=44n L=22n
M10 11 7 0 0 NMOS W=44n L=22n
M11 6 3 11 11 NMOS W=44n L=22n
M12 5 6 0 0 NMOS W=44n L=22n

vd 2 0 PULSE(0 1 0 0.1n 0.1n 3n 6n)
vr 4 0 PULSE(0 1 0 0.1n 0.1n 4n 8n)
vc 3 0 PULSE(0 1 0 0.1n 0.1n 1n 2n)

.include "22nm.md"
* --- Transient Analysis ---
```

```
.tran 1n 20n
.print tran v(5) v(6)
.meas avg_power AVG p(vdd) FROM=1n TO=20n
.MEASURE TRAN tdlay TRIG V(2) VAL=0.4 TD=0.1n
+ RISE=1 TARG V(5) VAL=0.4 RISE=1
.MEASURE TRAN PDP PARAM='avg_power*tdlay'
.op
.end
```

APPENDIX-II

CT - CNTFET HSPICE NETLISTS

This appendix presents the CNTFET HSPICE netlists used for simulation of Conventional TSPC D flip-flop architectures. Similarly you can get the other CMOS netlist just the node coding should be kept in mind for circuit representation.

I.2 CNTFET based Conventional TSPC D Flip-Flop HSPICE Netlist

```
.options POST
.options AUTOSTOP
.options INGOLD=2      DCON=1
.options GSHUNT=1e-12  RMIN=1e-15
.options ABSTOL=1e-5   ABSVDC=1e-4
.options RELTOL=1e-2   RELVDC=1e-2
.options NUMDGT=4      PIVOT=13
.param    TEMP=25
.lib 'CNFET.lib' CNFET
.param Ccsd=0          CoupleRatio=0
.param m_cnt=1         Efo=0.6
.param Wg=0            Cb=5e-12
.param Lg=22e-9        Lgef=100e-9
.param Vfn=0           Vfp=0
.param m=19            n=0
.param Hox=10e-9       Kox=12

VDD 1 0 DC 0.8
XM1 8 3 9 9 PCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1

XM2 9 2 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1

XM3 7 3 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
```

```

+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1

XM4 7 4 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1

XM5 6 7 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1

XM6 5 6 1 1 PCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbp='Vfp' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1

XM7 8 2 0 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1
XM8 10 3 0 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1
XM9 7 8 10 10 NCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1
XM10 11 7 0 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1
XM11 6 3 11 11 NCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1
XM12 5 6 0 0 NCNFET Lch=Lg Lgeff='Lgef' Lss=16e-9 Ldd=16e-9
+ Kgate='Kox' Tox='Hox' Csub='Cb' Vfbn='Vfn' Dout=1 Sout=0
+ Pitch=10e-9 n1=m n2=n tubes=1

vd 2 0 PULSE(0 1 0 0.1n 0.1n 3n 6n)
vr 4 0 PULSE(0 1 0 0.1n 0.1n 4n 8n)
vc 3 0 PULSE(0 1 0 0.1n 0.1n 1n 2n)
.tran 1n 20n
.print tran v(5) v(6)
.meas avg_power AVG p(vdd) FROM=1n TO=20n
.MEASURE TRAN tdlay TRIG V(2) VAL=0.4 TD=0.1n
+ RISE=1 TARG V(5) VAL=0.4 RISE=1
.MEASURE TRAN PDP PARAM='avg_power*tdlay'
.op
.end

```

LIST OF PUBLICATIONS AND THEIR PROOFS

1. Subodh Lakra and Akshay Mann, “Low Power Dynamic TSPC D Flip-Flop for High Performance Applications Based on CNTFET,” submitted to ”PICS-2026 2nd International Conference on Power and Intelligent Control System” Conference, 2026.

Proof Attached: Conference paper submission acknowledgement mail.



24/VLS/23 SUBODH LAKRA <subodhlakra_24vls23@dtu.ac.in>

2nd International Conference on Power and Intelligent Control Systems (PICS-2026) : Submission (574) has been created.

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Track Name: PICS2026

Paper ID: 574

Paper Title: Performance Evaluation of CMOS and CNTFET Based TSPC D Flip-Flop Architectures at 22 nm Technology

Abstract:

Modern VLSI systems require sequential circuits that operate with reduced power consumption and improved speed at deep nanoscale technologies. Among various sequential elements, D flip-flops are widely utilized in registers, counters, memory units, processors, and digital signal processing applications. However, conventional CMOS-based flip-flops experience increased leakage current, short-channel effects, and higher power dissipation at lower technology nodes. Due to the inherent limitations associated with conventional devices, Carbon Nanotube Field Effect Transistor (CNTFET) technology has been established as an ideal alternative, offering advantages such as superior electrical property performance, near-ballistic carrier transportation, low leakage currents, and higher switching speeds.

This paper provides a comparative performance assessment of the TSPC D flip-flop architectures developed according to CMOS and CNTFET technologies at the 22 nm node of technology. Four variations of TSPC architectures have been designed and simulated under the HSPICE simulation environment, including conventional TSPC, modified TSPC, preset enabled modified TSPC, and redundant precharge-free TSPC D flip-flops. The comparative analysis is performed on average power consumption, leakage current, propagation delay, and Power Delay Product (PDP) as performance metrics. The simulation results demonstrate that CNTFET-based architectures provide significantly lower leakage current, reduced power consumption, improved propagation delay, and superior PDP performance compared to conventional CMOS implementations. Among all the considered architectures, the redundant precharge-free CNTFET based TSPC D flip-flop achieved the minimum PDP value, indicating enhanced energy efficiency for future low-power and highperformance VLSI applications.

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Primary Subject Area: Control and Automation - Modeling and Simulation

Secondary Subject Areas: Not Entered

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APPLICATIONS BASED ON CNFET

Total Pages 51.

Name of the Scholar SUBODH LAKRA.

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Name: Subodh Lakra

Educational Qualification:

- Master of Technology (Pursuing) in VLSI Design and Embedded Systems, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi.
- Bachelor of Technology in Electronics and Communication Engineering from Bhagwam Mahavir College Of Engineering and Technology from Gujarat technological University.

Research Interests:

VLSI Design, Low Power Digital Circuits, CNTFET-Based Circuit Design, Sequential Circuit Design, and High-Speed Integrated Circuits.

Technical Skills: HSPICE, Synopsys Custom Compiler, Verilog HDL, MATLAB, LaTeX, Linux, Verilog, Ltspice, Cadence Virtuoso and Xilinx Vivado

Research Work:

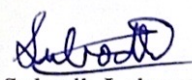
Worked on the design and analysis of low-power dynamic TSPC D Flip-Flops using CMOS and CNTFET technologies for high-performance VLSI applications.

Publications:

1. Subodh Lakra and Akshay Mann, "Low Power Dynamic TSPC D Flip-Flop for High Performance Applications Based on CNTFET," submitted to "PICS-2026 2nd International Conference on Power and Intelligent Control System" Conference, 2026.

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