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DESIGN OF MEMELEMENTS AND ITS APPLICATION IN MIXED SIGNAL PROCESSING CIRCUITS

34

A Thesis Submitted
in Partial Fulfilment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

by

RAHUL KUMAR GUPTA
(Roll No. 2K21/PHD/EC/08)

Under the Supervision of
Prof. Mahipal Singh Choudhry
&
Dr. Varun Saxena



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CANDIDATE'S DECLARATION

I, **Rahul Kumar Gupta**, hereby declare that the research work presented in this thesis titled **“Design of Memelements and its Application in Mixed Signal Processing Circuits,”** submitted in partial fulfilment of the requirements for the award of the **Doctor of Philosophy** degree in the **Department of Electronics and Communication Engineering, Delhi Technological University**, is a genuine and original contribution conducted by me between **August 2021 and July 2025**, under the supervision of **Prof. Mahipal Singh Choudhry** and **Dr. Varun Saxena**.

I further confirm that I have not submitted this thesis, in whole or in part, for the award of any degree at this or any other school.

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ABSTRACT

Memristor technology is gaining popularity for its potential uses in nanoelectronic memory, neuromorphic computer architectures, digital and analog modulation systems, and oscillator circuits. Memristor research has becoming increasingly popular. However, there is currently no single device on the market that can display true memristive behavior over a specific frequency range. Researchers rely on emulator circuits to study the features and possible uses of physical memristor prototypes, which are presently restricted. Memristor emulator circuits simulate the behavior and attributes of memristors. Memristors are a newly recognized passive element with potential uses in digital, analog, and mixed signal domains. Emulator circuits are crucial for understanding the underlying concepts and potential uses of memristors, especially in the absence of a physical memristor. They can be made in the lab using inexpensive off-the-shelf components.

Prof. L Chua profound a new circuit component in 1971 which behaves differently in comparison to three known passive components (resistor, capacitor, and inductor). After three decades, in 2008, D. B. Strukov and his team presented the first fabricated memristor and after a long gap (four decades), the concept of memelements extended to memcapacitor and meminductor. The researchers are keenly interested in exploring the characterization and application in different fields of memelements because of their non-linear and non-volatile properties. Further, the lack of fabrication-level implementation, researchers is trying to develop their circuit emulators and rely on this practical approach. Mostly existing circuit emulators are thoroughly analyzed, simulated, and summarized in detail with the different approaches. Hence, This thesis presents a comprehensive study and novel design methodologies for compact, low-power emulator circuits of emerging memory-based elements—namely memristors, memcapacitors, and meminductors—using CMOS-compatible technologies. Multiple emulator topologies have been proposed, each targeting specific performance metrics such as high-frequency operation, low power consumption, and hardware simplification. These circuits are realized through innovative configurations of MOSFETs, MOS capacitors (MOSCAPs), operational transconductance amplifiers (OTAs), differential mode floating gate (DMFG), gyrator circuit, and dynamic threshold techniques.

A compact memristor emulator design is presented, demonstrating different circuit approaches. The first design is a FMRE- floating memristor emulator and GMRE-grounded memristor emulator that uses a single MOSFET with a RC filter which is first

order, achieving operating frequencies up to 80 MHz within a compact $1.586 \mu\text{m}^2$ layout. The second design is a MOSCAP-based grounded passive memristor emulator, implemented with only MOSFETs (three numbers) and MOSCAP (one number), requiring no external biasing and emphasizing simplicity and power efficiency, with reliable operation up to 30 MHz. The third approach introduces a floating, fully passive memristor emulator that consists of MOSFETs (six numbers) and capacitor (one number), employing the DTMOS-dynamic threshold MOSFET technique. These circuits are analyzed through their hysteresis loops and current–voltage characteristics, confirming the expected memristor figures of merit. Furthermore, the proposed emulators are demonstrated in mixed-signal processing applications, including filters, Schmitt triggers, Colpitts oscillators, Chua’s oscillators, and XOR logic circuits.

For memcapacitor emulation, a design using a single multi-output OTA is proposed and validated through both 45nm CMOS simulation and hardware testing using the LM13700 IC. This circuit supports operations up to 4 MHz, consuming $272.5 \mu\text{W}$, and proves suitable for integration, differentiation, and neuromorphic learning tasks. Robustness is confirmed via Monte Carlo and PVT variation analyses.

Meminductor emulator circuits have also been investigated using different design strategies. In one grounded topology, six MOSFETs and two capacitors are employed to generate pinched hysteresis loops (PHL) at an operating frequency of 100 kHz, with performance validated through comprehensive PVT (process, voltage, and temperature) analysis and non-volatility testing. Another advanced design is based on an active gyrator configuration that utilizes five MOSFETs, including a MOS-based capacitor. This design achieves a high operating frequency of 200 MHz, with static and dynamic power consumptions of 2.52 mW and 3.23 mW, respectively, while occupying an area of $80.5 \mu\text{m}^2$. The practicality of these emulators is further demonstrated by their application in adaptive learning systems and chaotic oscillator circuits.

All emulator circuits are designed and simulated using Cadence Virtuoso Spectre tool with GPDK 180nm, 90nm, and 45nm CMOS technologies. Extensive analyses including transient response, hysteresis behavior, non-volatility, tunability, temperature stability, and process corner variation confirm the reliability and scalability of the proposed designs. Comparative studies show significant improvements in circuit simplicity, frequency performance, and power efficiency over existing emulator models.

These contributions collectively advance the practical realization of memory-based analog components in neuromorphic computing, nonlinear systems, and programmable analog signal processing, thereby supporting the next generation of intelligent hardware platforms.

Finally, in this thesis, we summarize the conclusions inferred from our research work and highlight the potential future scope in the field of next generation of intelligent hardware platforms.

Publications Related to the Thesis

Journal Papers Published

1. **R. K. Gupta**, M. S. Choudhry, V. Saxena, and others, “A single MOS-memristor emulator circuit,” *Circuits, Systems, and Signal Processing*, vol. 43, pp. 54–73, 2024. Available: <https://doi.org/10.1007/s00034-023-02500-5>
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4. **R. K. Gupta**, V. Saxena, and M. S. Choudhry, “Exploring Mem-Element Emulators: A Review. [Under Review].

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Thank you all for making this journey possible.

(Rahul Kumar Gupta)

Dedication

***This thesis is dedicated to my
family mother, father, brother, and
sisters.***

*For their endless love, support, and
encouragement*

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List of Symbols and Abbreviations

Symbols and Abbreviations	Description
π	pi (phase)
τ	Time constant
Ω	Ohm
ω	Angular frequency
f	frequency
k	Boltzmann constant
ϕ	Flux
g_m	Transconductance
C_{ox}	Oxide capacitance per unit area
A_m or V_m	signal amplitude
V_t or V_T	Threshold voltage of MOSFET
V_b or V_{BB}	Bias voltage
V_{BE}	Base emitter junction voltage of BJT
V_{FD}	Forward diode voltage
V_{To}	Thermal voltage
V_{DD}/V_{DD}	Positive power supply
V_{SS}	Negative power supply
vs	Versus
W/L	Channel width/Channel Length
k_p or K_p	Process transconductance parameter of PMOS
k_n	Process transconductance parameter of NMOS
q	Elementary charge
I_C	Collector current of BJT
I_s	Saturation current of BJT
J	Emitter junction current density of BJT
IC	Integrated circuit
HP	Hewlett Packard
ASIC	Application-specific Integrated Circuit

TSMC	Taiwan Semiconductor Manufacturing Company
UMC	United Microelectronics Corporation
SCL	Semi-Conductor Laboratory
RCA	Radio Corporation of America
EDA	Electronic Design Automation
VLSI	Very Large Scale Integration
PDKs	Process Design Kits
AI	Artificial Intelligence
ANN	Artificial Neural Network
SNN	Spiking Neural Network
STDP	Spike-timing-dependent plasticity
MNIST	Modified National Institute of Standards and Technology
MAC	Multiply and Accumulate
EEG	Electro-encephalogram
PCB	Printed circuit board
R	Resistor
C	Capacitor
L	Inductor
ADE	Analog Design Environment
MIM	Metal-insulator-metal
MCS	Monte Carlo Simulation
PVT	Process, Voltage and Temperature
TT	Typical-typical
SS	slow NMOS slow PMOS
HRS	High resistance state
LRS	Low resistance state
V-I or v-i	Voltage-current
PHL	Pinched hysteresis loop
ABB	Analog building block
FF	fast NMOS fast PMOS
SF	slow NMOS fast PMOS
FS	fast NMOS slow PMOS
TL	Translinear

CW	Clock-wise
CCW	Counter Clock-wise
CM	Current mode
CMC	Current mode circuit
VMC	Voltage mode circuit
NiO	Nickel oxide
HfO	Hafnium oxide
ZnO	Zinc oxide
wo	Tungsten oxide
TaO	Tantalum oxide
TiO ₂	Titanium dioxide
PCM	Phase change memory
RRAM	Resistive random access memory
MRAM	Magnetic random access memory
MRE	Memristor Emulator
CMOS	Complementary metal oxide semiconductor
BJT	Bipolar junction transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
DT-MOS	Dynamic threshold MOS
VDCC	Voltage differencing current conveyor
VDIBA	Voltage differencing inverting buffered amplifier
DVCCTA	Differential voltage current conveyor trans conductance amplifier
CDTA	Current differencing transconductance amplifier
VDBA	Voltage differencing buffered amplifier
DZ-VDTA	Dual Z output voltage dependent transconductance amplifier
CFTA	Current follower transconductance amplifier
CCII	Second generation current conveyor
OTA	Operational transconductance amplifier
CCTA	Current conveyor transconductance amplifier
VDTA	Voltage differencing transconductance amplifier

Chapter 1

Introduction of Memristor, Memcapacitor, and Meminductor

This chapter introduced the background of memristor, memcapacitor, and meminductor emulators and the challenges of the physical implementation of memelements. Furthermore, motivation and problem statement, research gaps, research objectives, and thesis organization are discussed.

1.1 Background

This thesis is a detailed report and collection of research findings on the concept of memristor, memcapacitor, and meminductor emulators and their application in mixed signal processing circuits. W. A. Dummer established the concept of integrated circuits (ICs) in 1952. All circuit components, including their interconnections, are built on a single semiconductor substrate in an integrated circuit (IC). Today, ICs are found in practically all electronic products, ranging from simple to very complicated systems, including digital cameras, microwave ovens, washing machines, cellphones, laptop computers, televisions, and even medical devices like pacemakers. This innovation has substantially transformed the electronics sector.

The majority of naturally occurring signals, including temperature, light, sound, seismic waves, humidity, and biological motions, are essentially analog. Furthermore, many electrical sensors generate analog signals as an output in reaction to external stimuli. Even digital systems frequently use analog circuits to communicate with the physical world. Advances in integrated circuit technology have permitted the integration of analog and digital functionalities onto a single chip, resulting in smaller, more efficient, and cost-effective hardware solutions for complicated jobs.

IC design has become increasingly dependent on the semiconductor technology utilized, such as bipolar junction transistors (BJTs), metal-oxide-semiconductor field-effect transistors (MOSFETs) [1], and complementary metal-oxide-semiconductor (CMOS). Over the last 30 years, CMOS has become the preferred technology due to its good fabrication compatibility, intrinsic capacitive behavior, and ease of integration [2]. Furthermore, CMOS analog circuits

provide advantages such as smaller chip size, faster operation, and lower power consumption, making them perfect for precision applications [3].

In 1971, Chua envisioned the missing fourth circuit element, the memristor, in addition to resistor, capacitor, and inductor [4]. More detailed discussions on a broad generalization of memristors as memristive systems were published in 1976 [5]. The memristor is a two-terminal nonlinear electric element. In 2008, after 37 years, Chua's missing memristor was finally discovered and fabricated by a team of researchers at Hewlett-Packard [6], and it was based on a thin film of titanium dioxide.

The memristor was conceptualized by analyzing the relationships among current i , charge q , voltage v , and flux ϕ . There are six different mathematical relations of connecting pairs of these four variables. Charge q and flux ϕ are the time integral of the current i and the voltage v , respectively, and the remaining four relationships define the four fundamental circuit elements such as the resistor, the capacitor, the inductor, and the missing fourth element, i.e., the memristor. The memristor was the missing link between flux ϕ and charge q . It is shown in Figure 1.1. Memristance is a non-linear, time-invariant property that directly relates electric charge to magnetic flux.

$$v(t) = M(q(t)) * i(t) \quad (1.1)$$

where $M(q(t))$ is the charge-controlled memristance.

$$M(q) = \frac{d\phi(q)}{dq} \quad (1.2)$$

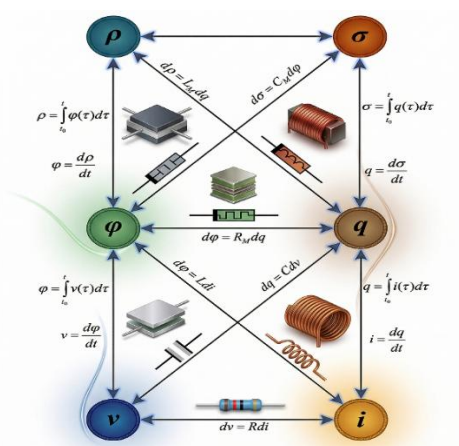


Figure 1.1 Relationship between voltage (v), current (i), charge (q), flux (ϕ), time-integral of flux (ρ) and time integral of charge (σ)[7], [8]

The figure 1.1 also illustrates the relationships among fundamental circuit variables—voltage v , current i , charge (q), and flux (ϕ) along with their time-integrated counterparts (σ) and (ρ). Classical elements such as the resistor, capacitor, and inductor define the relations between (v), (i), (q), and (ϕ), while the memristor establishes the missing link between charge and flux. The variables (σ) and (ρ) represent the time integrals of charge and flux, respectively, and are included as auxiliary variables for generalized modeling of memory elements.

Out of these four fundamental elements, Memristor has unique V-I characteristics which is shown in Figure 1.2. This unique behavior makes it suitable for the design of all sorts of Non-linear chaotic circuits.

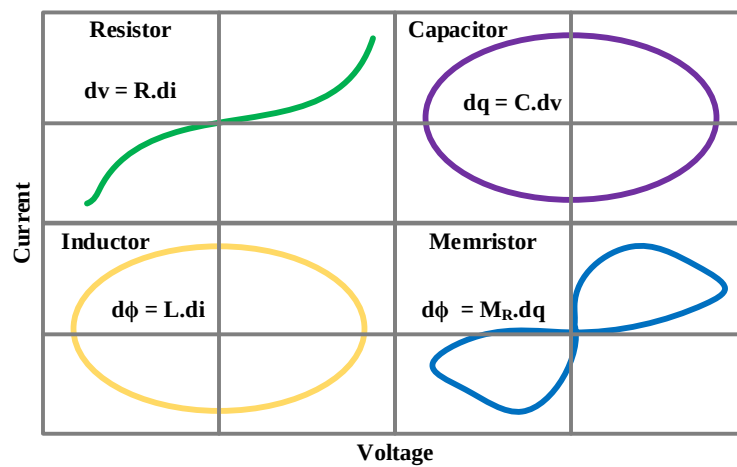


Figure 1.2 V-I characteristics of resistor, capacitor, inductor and memristor

Until 2008 the field of memristor design suffered from a lack of attention from the research community on account of a lack of solid-state implementation [9]–[12]. In 2008, Hewlett Packard and their research team announced the first fabricated memristor using titanium oxide which is fulfilling the definition of a memristor [6] and this is a new path for researchers in the field of memristor and its applications. The nonvolatility and non-linear behavior play a profound role in different fields such as digital logic design [13], analog programmable devices and computation circuits[14]–[17], adaptive filters[18], crossbar classifiers[19]–[21], neuromorphic circuits, neural networks [22]–[26], chaotic circuits [27], [28] and non-volatile memories[29]–[31]. Further, material-based memristors such as polymers [32], 2D materials[33] or graphene oxide[34]–[36], transition metal oxides (e.g., NiO and TaOx)[37], [38] have been studied and simulated but due to fabrication complexity and high cost, their validation in real-time applications is still not possible.

After the success of memristor Ventra, Pershin and Chua explore the concept of memcapacitor and meminductor [39],[40]. They defined the electrical relation between the time-integral of charge (σ) and the flux (ϕ) with the memcapacitor; and between the time-integral of the flux (ρ) and the charge (q) with the meminductor.

$$C(\phi) = \frac{d\sigma(\phi)}{d\phi} \quad (1.3)$$

$$L(q) = \frac{d\rho(q)}{dq} \quad (1.4)$$

All three memdevices also present a memory ability with the closed pinched hysteresis loop and with the capability of storing energy in capacitive and inductive forms respectively [41]. These devices are becoming the key of emergence of a new way of computation which known as neuromorphic computing and their characteristics are allowed to mimic biological computing. The ability of storing and process the information simultaneously would offer capabilities and power consumption, comparable to the human brain system [42], [43]. Since due to lack of solid state implementation, the memcapacitor and meminductor obstruct the prominent feature of these devices into real time applications. So, reasearchers are concentrated on development of emulators of these devices. The emulators are the circuits that satisfy the inherent equations of the memdevices emulators.

1.1.1 Classification of memelements

Mem-elements are classified based on the relationship between fundamental electrical variables: voltage (v), current (i), charge (q), and magnetic flux (ϕ). There are three primary types of mem-elements:

- ✓ Memristor (Memory Resistor)
 - Relation: Flux (ϕ) $\leftrightarrow$ Charge (q)
 - Characteristic Equation: $v(t)=M(q)i(t)$
 - Memory of: Charge
 - Function: Nonlinear resistor with memory
- ✓ Memcapacitor (Memory Capacitor)
 - Relation: Charge (q) $\leftrightarrow$ Voltage (v)
 - Characteristic Equation: $q(t)=C_m(\phi)v(t)$
 - Memory of: Voltage/Flux
 - Function: Capacitor with memory-dependent capacitance

- ✓ Meminductor (Memory Inductor)
 - Relation: Flux (ϕ) $\leftrightarrow$ Current (i)
 - Characteristic Equation: $\phi(t) = L_m(q)i(t)$
 - Memory of: Current/Charge
 - Function: Inductor with memory-dependent inductance

1.1.2 Application of memelements

Memristors have found widespread application in both analog and digital fields. They are mostly employed in two forms: discrete and crossbar configuration. In addition, memcapacitors and meminductors are popular applications in analog and digital circuits.

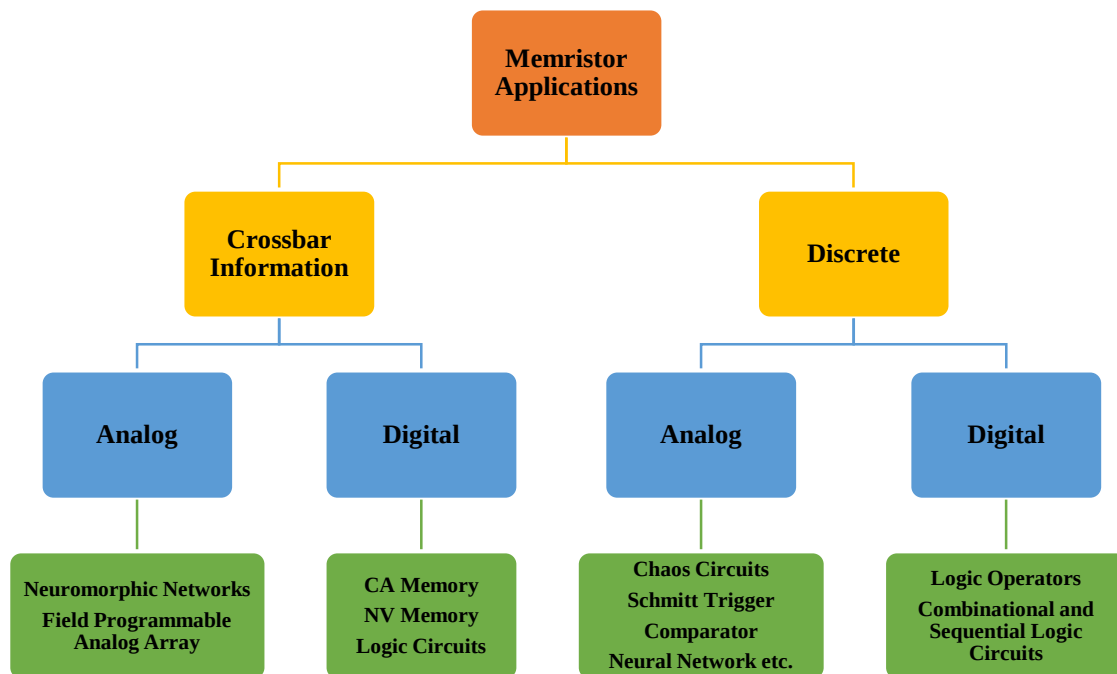


Figure 1.3 Application of memristors in different fields

1.2 Motivation and Problem Statement

1.2.1 Motivation

Contemporary computing devices suffer from limitations such as memory wall, instruction level parallelism and power wall. Further, in CMOS circuits, as the CPU frequency increases, the power dissipation increases. This limits the CPU maximum clock speed. Furthermore, problems with the current CMOS technology [9] such as leakage current, cost per piece and

scaling wall have resulted in the saturation of the Moore's law. There is an immediate need of certain alternative technologies that can keep up with the demands of advancing human computational needs. Few promising technologies, which are likely to be in the market within a span of a decade are 3-D CMOS circuitry and memristor based circuits. Other evolving technologies like Quantum dots, spin-wave devices still need a lot of development. Notably, major semiconductor foundries like as TSMC, UMC, and SCL have yet to include memristive components in their Process Design Kits (PDKs).

The conceptual foundation of mem-elements, has created transformative opportunities in memory storage, neuromorphic computing, and nonlinear circuit theory. The practical deployment and experimentation with physical memelements are hampered by limited commercial availability, high fabrication costs, fabrication process complexity, material non-idealities, and device parameter tunability limitations.

Nonetheless, memristor's distinguishing properties, including as non-volatile memory behavior and nonlinear resistance, have created potential for their usage in modern electronics for computing, data storage, and signal processing [44]. My personal interest in memristor emulators prompted me to look into more efficient emulator designs that offer faster speeds and smaller silicon space. This incentive led me to improve existing emulator architectures by focusing on crucial performance criteria like as energy efficiency and compactness.

This endeavor has widened my research into analog signal processing and computational architectures, in which memristor emulators may outperform physical solid-state prototypes. The rising quantity of literature and research on memristors piqued my interest in their possibilities for memory systems and neuromorphic computing. Professor Leon Chua's important 1971 paper "Memristor-The Missing Circuit Element" [4] introduced key ideas that remain extremely relevant and motivate improvements in the area today. However, many recent memristor versions still use a significant number of transistors and passive components. Recognizing these inefficiencies, I noticed an obvious need for optimization in memristor design. Furthermore, biologically inspired analog systems, particularly neuromorphic architectures with memristor crossbars, have emerged as strong edge computing solutions, providing substantial energy and area efficiency gains [45].

This, in turn, results in high power consumption and limited chip area. A detailed review of these problems has guided the development of memelement emulator designs, with the goal of

bridging existing technological gaps and enriching the present body of knowledge. Beyond adding to the literature on memelement emulators, this study improves understanding of their fundamental principles and prospective applications, opening up new avenues for researchers in the expanding field of arithmetic and neuromorphic computing.

My developing interest in memelements have motivated me to promote innovation and experimentation in this discipline. This work aimed to investigate the feasibility of designing high-speed memelement emulators with fewer transistors, explore the applications of memelement emulators in the field of analog and digital. The primary objective for this work is a desire to provide superior designs for memelement emulators that provide faster performance, greater stability, optimal frequency behavior, lower energy consumption, and a smaller silicon footprint. These goals sparked continued research into memelement applications in chaotic systems, neuromorphic computing, and data storage.

Overall, this thesis shows a concerted attempt to considerably develop silicon-based memelement emulator technologies by addressing current constraints, offering efficient alternatives, and increasing their reach in modern electronics and computing systems.

The purpose for building these emulators is:

- Circuit-level research to test and validate real-world applications.
- Mem-element emulators help to develop brain-inspired computer systems.
- Educate and train students in next-generation circuit design.
- Model testing and validation

Finally, the design of memristor, memcapacitor, and meminductor emulators closes the gap between theoretical promise and actual experimentation, driving innovation in developing computing paradigms, analog memory systems, and programmable analog circuits.

1.2.2 Problem Statement

The current challenges in the field of mem-device emulator synthesis are as follows:

1. Analyzing the proposed designs, possible solutions, associated with scaling the memelement based systems for practical applications.

2. Developing optimized mem-devices emulators using MOSFETs and undertaking their performance analysis
3. Evaluating the state of the art in memristor-based electronics and exploring where the future of the field.

1.3 Contribution of Thesis

Contributions of this thesis are as follows:

A Single MOS-Memristor Emulator Circuit: Proposed a high-frequency memristor emulator that may be used in both grounded and floating setups. This concept uses a single MOSFET to connect to a first-order RC filter and functions passively. It consumes no static power and only a few picowatts of dynamic power when an input signal is applied. The suggested circuit was simulated using the Cadence Virtuoso Spectre platform, and its mathematical formulation validates the emulator's memristive and incremental features. The emulator has a tiny layout area of $1.586 \mu\text{m}^2$ and can operate at frequencies up to 80 MHz. The suggested design was experimentally validated utilizing discrete components, including the ALD1117 dual P-channel enhancement-mode MOSFET array and an external RC network. The emulator's performance has been evaluated and confirmed for both analog and digital applications in floating and grounded modes.

A Passive Grounded MOSCAP- Memristor Emulator: A grounded passive memristor emulator based on a MOSCAP design that uses only three MOSFETs and a single MOS capacitor and does not require any external biasing. Previous research in this area has often used memristor emulators constructed from ordinary circuit blocks and other passive components. In comparison, the proposed architecture provides a much simpler framework. The circuit was simulated in Cadence Virtuoso using the GPDK 180nm CMOS technology node and tested using sinusoidal and pulse input signals. It can operate at frequencies as high as 30 MHz. The simulation findings show a distinct hysteresis loop and the current-voltage relationship that defines memristive behavior. The memristor's key performance criteria were successfully accomplished, and its practical applicability was demonstrated through filter design.

A Passive Floating C-MOS Memristor with Analog Applications: A totally passive floating memristor emulator is suggested, which employs six MOSFETs and a capacitor using the Dynamic Threshold MOSFET (DTMOS) approach. The circuit was simulated using GPDK

180nm CMOS technology in Cadence Virtuoso Spectre and studied for transient response, hysteresis behavior, and nonvolatile properties, including variations across process corners and temperatures. The design operates at frequencies up to 10 MHz with low power consumption, a small layout ($56.725 \times 57.15 \mu\text{m}^2$), and high-frequency performance. Its usefulness is illustrated in analog circuits such as Colpitt's chaotic oscillators, Chua's oscillator, and Schmitt trigger arrangements.

A Memcapacitor Emulator Circuit using a Single MO-OTA with Experimental Results and its Application in Neuromorphic and Mathematical Operations: A memcapacitor emulator was created utilizing a single multi-output operational transconductance amplifier (MO-OTA) and simulated in Cadence Virtuoso with 45nm GPDK technology. The experimental validation was carried out with the LM13700 OTA IC. The circuit may operate at up to 4 MHz with a power consumption of 272.5 μW . Its performance was assessed using transient analysis, hysteresis plots at different frequencies, and Monte Carlo simulations. The robustness was further proved by PVT variation testing. The suggested emulator is versatile, allowing applications ranging from mathematical functions such as integration and differentiation to neuromorphic adaptive learning systems.

A Minimalist MOS-based Meminductor Emulator Circuit: A grounded meminductor emulator (MIE) that employs a MOSFET-based design with six transistors and two capacitors. The circuit may generate pinched hysteresis loops (PHL) at frequency of up to 100 kHz. Extensive simulations, including PVT analysis and non-volatility testing, employing 180nm CMOS technology in Cadence Spectre, verify its reliability. The emulator consumes very little power, only a few microwatts. The comparative study demonstrates the benefits of the proposed MIE over existing designs.

MOSFET-Meminductor Emulator Circuit with Experimental Validation and Application in Adaptive Learning and Chua's oscillator circuit: A grounded meminductor emulator (MIE) that uses only five MOSFETs—three NMOS and two PMOS—is proposed. The concept employs an active gyrator structure, with one NMOS acting as a MOS capacitor, displaying both memory and inductive properties, avoiding the requirement for passive components. The circuit, which was simulated using 90nm GPDK CMOS technology in Cadence Virtuoso Spectre, has a steady frequency response up to 200 MHz. Non-volatility, thermal stability, tunability, Monte Carlo analysis, and process corners testing have all proven its reliability. The emulator consumes 2.52 mW static and 3.23 mW dynamic power, with an $80.5 \mu\text{m}^2$ layout

area. Its usefulness has also been proved in applications like as adaptive learning and chaotic oscillators, where it outperforms conventional solutions in terms of efficiency and compactness.

1.4 Thesis Organization

This thesis is divided into six chapters, starting with Chapter 1, which is the current introductory portion. Chapter 2 is a comprehensive overview of the literature on current-mode circuits and memelement models that are important to this study. Chapters 3, 4, and 5 each begin with an introduction before moving on to describe circuit implementation, simulation results, non-ideal analysis, performance comparisons with current designs, realistic hardware realizations, and their applications. Finally, Chapter 6 summarizes the study's findings and suggests potential future research topics.

Chapter 1 provides the research background of memelements and evolution, research flow, memelement description, research objectives, and an outline of the entire thesis based on a comprehensive literature review concerning memelement emulators.

Chapter 2 reviews the detail history and previous works on this research in past few years. Fundamental concepts of memristor, memcapacitor, and meminductor as well as the operation of a memelements. This review of the literature provides an overview of the modern memristor alternatives and their in-depth investigation, modeling along with potential future applications.

Chapter 3 discusses about the proposed memristor emulators circuits. floating/grounded memristor emulator having a single MOSFET connected to a first-order RC filter with high operating frequency up to 80 MHz within a compact $1.586 \mu\text{m}^2$ layout is presented, a grounded Passive MOSCAP-memristor emulator is presented consisting of only three MOSFETs and one MOSCAP without biasing emphasizing design simplicity and power efficiency up to 30 MHz frequency, and A floating fully passive memristor emulator, characterized by six MOSFETs and a capacitor, has been introduced, employing the dynamic threshold MOSFET technique (DTMOS). The proposed circuits analyzed the hysteresis loop and variation of current according to the voltage direction. The expected figure of merits of the memristor is successfully obtained and presented the memristor application in mixed signal processing circuits such as filters, Schmitt trigger, colpitt oscillator circuit, Chua's oscillator circuit and XOR logic circuit.

Chapter 4 discusses a memcapacitor emulator model has been proposed using a single multi-output operational transconductance amplifier (MO-OTA). The model has been simulated using Cadence Virtuoso 45nm GPDK technology. The experimental verification of the model

has been carried out using the existing operational transconductance IC LM13700. The circuit exhibits desired characteristics up to a frequency of 4 MHz and has a power consumption of 272.5 μ W. Using the proposed model, transient analysis and hysteresis curves have been plotted at different frequencies. The reliability of the proposed structure has been tested through Monte Carlo simulations. Process-voltage-temperature (PVT) variation testing has been performed to check the robustness of the proposed circuit. The proposed memcapacitor emulator model has been shown to have a diverse range of applications ranging from mathematical operations such as integration and differentiation to neuromorphic adaptive learning.

Chapter 5 discusses a compact grounded meminductor emulator (MIE) using only five MOSFETs (three NMOS, two PMOS) is proposed. It employs an active gyrator topology with one NMOS acting as a MOS capacitor to provide memory and inductive behavior, eliminating passive components. The design maintains a stable response up to 200 MHz and is validated through various analyses including non-volatility, thermal stability, tunability, Monte Carlo, and process corners. Implemented in 90 nm GPDK CMOS using Cadence Virtuoso, it consumes 2.52 mW static and 3.23 mW dynamic power, with an area of 80.5 μ m². Its use in adaptive learning and chaotic circuits shows practical potential, outperforming existing MIEs in efficiency and compactness.

Chapter 6 summarize the key finding of the research presented in this thesis and conclude the work. In this chapter also explores the future direction in the field of developing efficient memelement emulators or physical memelement, such as memristor, memcapacitor, meminductor with their application in mixed signal processing circuits. The discussion focuses on advancements in memristor, memcapacitor and meminductor emulators in the field of neuromorphic circuits, CMOS compatible optimization, hardware security, mixed signal IC integration, experimental fabrication and testing, adaptive and chaotic systems, and standard cell libraries for memelement emulators.

Chapter 2

Literature Review

This chapter explained the merits and demerits of existing state-of-the-art methods. We reviewed several methods of memristor, memcapacitor, and meminductor emulators. This helped us discover the research gaps in existing solutions in the area of memelement efficient designs and applications in mixed signal processing circuits. We also discussed the existing memelements emulators. Later, the research objective has been formulated based on these research gaps, which are addressed in this thesis.

Research on mem-element emulators such as memristors, memcapacitors and meminductor with its performance and applications at different aspects are have been reported in the literature since 1997. At first, we discuss the presently available memristor emulators and the their applications in the Section 2.1. It is followed by discussion of the literature review existing memcapacitor emulator in Section 2.2, meminductor emulators in Section 2.3 and application of these devices in the field of electronics in Section 2.4. The identified research gaps and research objectives have been discussed through Section 2.5 and 2.6 respectively.

2.1. Literature on Memristor Emulators

The general memristor (M_R) is elucidated as the n^{th} -order system that plants a nonlinear relation between the voltage (v) and current (i) [5]. It can be voltage controlled or current controlled depending on the intrinsic part of the input variable. Therefore, the n^{th} -order voltage-controlled is defined by the equation (2.1), and the current-controlled memristor is defined by the equation (2.3-2.4).

$$\dot{x} = f(x, i, t) \quad 2.1$$

$$v(t) = R(x, i, t). i(t) \quad 1.2$$

$$\dot{x} = f(x, v, t) \quad 2.2$$

$$i(t) = G(x, v, t). v(t) \quad 2.3$$

Where v and i are port voltage and current respectively;

$x = n$ internal state variable;

$R =$ Memristance; and

$G =$ Memductance.

The equation for a charge-controlled and flux-controlled memristor is a particular case of equations (2.1-2.2) and (2.3-2.4) respectively. Since R and G depend only on charge and flux respectively, so the charge-controlled and flux-controlled is defined by the equation (2.5) and (2.6) respectively.

Hence, memristor behavior is the same as linear resistance in the limit of infinite frequency and non-linear resistor in the limit of zero frequency.

$$v(t) = M_R \left(q(t) = \int_{t_0}^t i(\tau) d\tau \right) i(t) \quad 2.4$$

$$i(t) = M_R^{-1} \left(\phi(t) = \int_{t_0}^t v(\tau) d\tau \right) v(t) \quad 2.5$$

In the above equations, the initial instant of time, t_0 , may be selected to clinch that $\int_{-\infty}^{t_0} i(\tau) d\tau = 0$ and $\int_{-\infty}^{t_0} v(\tau) d\tau = 0$, respectively.

There are three main characteristics of memristor called fingerprints of memristor [46]. The first trace of the memristor is pinched hysteresis loop in which $i = 0$ whenever $v = 0$ for sinusoidal signal. The second trace of memristor is that the hysteresis lobe area should decrease as frequency increases which depicts the linearity at high frequency of memristor. At infinity frequency it becomes a single valued function and this property is called the third fingerprint of memristor.

Since, after the first literature presented by Chua [4] the memristor was fabricated by HP lab and their researchers using titanium oxide. The semiconductor forms two different resistive regions as low resistance (R_{on}) higher resistance (R_{off}) respectively [6]. Moreover, the memristor design by HP laboratories is not still commercialized due to its fabrication complexity and high

cost. It delays the commercialization of the real-time applications of the memristors. Therefore, researchers are attracted to memristor emulators using digital and analog methods.

An example of memristor emulator is the one proposed by Vista and Ranjan in Ref. [47] which is shown in Figure 2.1. This circuit is based on the mathematical model of flux-controlled memristors introduced by Daniel and Horst [48], which is represented in equation (2.7):

$$i(t) = \frac{1}{R_{off}} \exp\left(\frac{w(t)}{D} \ln \frac{R_{off}}{R_{on}}\right) t \quad 2.6$$

Where, $w(t) = w_0 + \frac{\mu_D}{D} \phi(t)$ and flux is the time integral of input voltage.

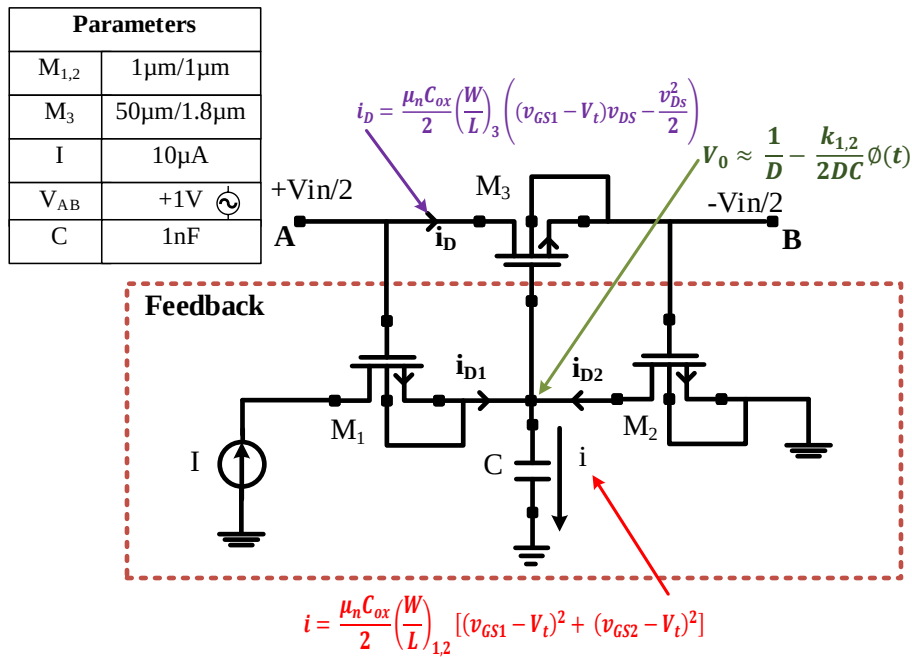


Figure 2.1 Memristor emulator circuit proposed by Vista and Ranjan [47]

Note that, above proposed structure uses only three NMOS transistors and a single capacitor but a constant current source is required. This circuit is simulated using 180nm TSMC CMOS technology. This circuit is achieving a variable resistance using a proper feedback of the voltage across the memristor (M_R). Since this circuit is floating and a current source is required for biasing of M1 transistor and the transistor M3 contributes variable resistance (r_{ds3}) can be formulated as shown in equation (2.8) and it varies accordance to V_{ds3} which consummate by the feedback circuit. The mathematical validation of the this circuit is explained in equations (2.9-2.13)

$$r_{ds3} = \frac{1}{k(V_{gs3} + V_{t3} + V_{ds3})} \quad 2.7$$

$$i = i_{D1} - i_{D2} \quad 2.8$$

$$i = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right)_{1,2} [(v_{GS1} - V_t)^2 + (v_{GS2} - V_t)^2] \quad 2.9$$

After solving the equation (10) we get the value of V_0 :

$$V_0 \approx \frac{1}{D} - \frac{k_{1,2}}{2DC} \phi(t) \quad 2.10$$

The drain current drawn through M_3 transistor:

$$i_D = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right)_3 \left((v_{GS1} - V_t)v_{DS} - \frac{v_{DS}^2}{2} \right) \quad 2.11$$

Hence the inverse memristance is shown in equation (13):

$$M^{-1}(\phi(t)) \approx \mu_n C_{ox} \left(\frac{W}{L} \right)_3 \left[\frac{1}{D} - V_t - \frac{k_{1,2}}{2DC} \phi(t) \right] \quad 2.12$$

This circuit closed pinched hysteresis loop exist till 13MHz frequency and it verifies all the three fingerprints. They have also done the experiment using IRF840 and a capacitor. The current source I is chosen in which the transistor should remain in saturated region. The author has shown the different application with their proposed memristor model such as Schmitt trigger, associative learning process and AM modulation and demodulation which shows the workability of the model. Hence Vista and Ranjan model is versatile and very simple, very less component is used, high operation frequency (upto 13MHz), layout area $2803\mu\text{m}^2$, less power consumption $6.725\mu\text{W}$ and suitable for IC fabrication.

A similar approach was proposed by Babacan, Yesil and Gul in Ref [49] and it is shown in Figure 2.2. This emulator circuit is designed using only four MOS transistor in which one transistor M_4 is used as an MOSCAP because capacitor is very important element to provide memory effect. This MOSCAP voltage drives M_3 transistor in saturation region. The DC power supply is used for biasing of transistors M_1 and M_2 . In this paper circuit equivalent ZnO thin film-based semiconductor memristor is fabricated by direct-current reactive magnetron sputter and it can also be used for emulating semiconductor device that demonstrate bipolar,

homogeneous and memristive characteristics fabricated using drift material (TiO₂, TaO_x, ZnO, HfO₂ and VO₂) and techniques such as sputter, atomic layer deposition and pulsed laser deposition. This circuit is operated upto 100MHz, layout area 366 μm². The pre and post layout simulation has been done using cadence spectre tool with 180nm TSMC CMOS technology.

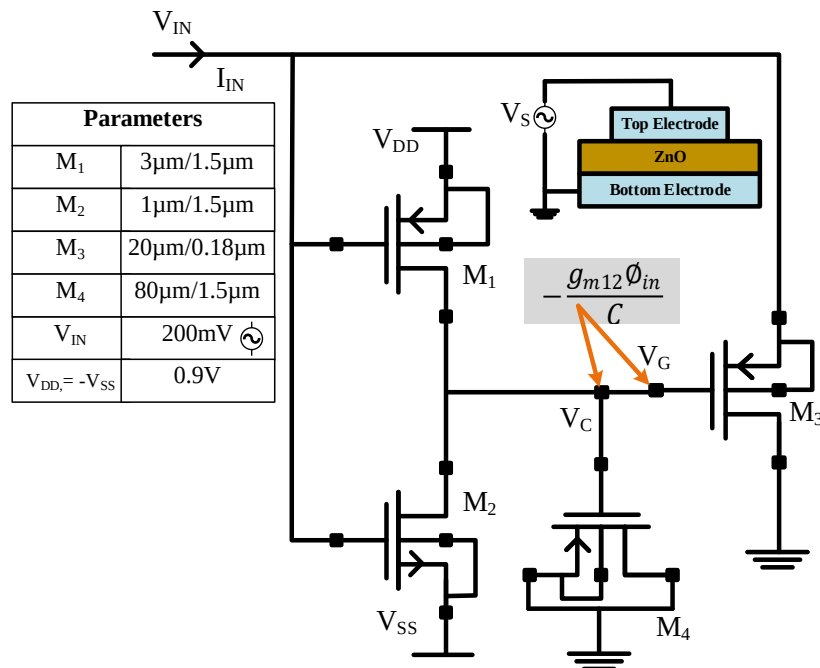


Figure 2.2 Memristor emulator circuit proposed by Yesil and Gul [49]

This memristor is purely grounded memristor. The memductance is represented mathematically in equation (2.14).

$$W((\phi_{in})) = -\mu_p C_{OX} \left(\frac{W}{L}\right)_3 V_{TP} - \mu_p C_{OX} \left(\frac{W}{L}\right)_3 \frac{g_{m12} \phi_{in}}{C} \quad 2.13$$

The experimental has been shown using ALD1116 and ALD1117 for transistors and power supplies are $\pm 6V$. The voltage current relationship for emulator circuit and fabricated ZnO memristor with variable sweep (-0.7V to 0.7V) has been shown and validate the both approaches.

Another example of this kind of design is proposed by Abdullah yesil in Ref [50] for grounded memristor emulator. The emulator circuit is shown in Figure 2.3. In this manuscript the emulator circuit consists of only seven MOS transistors and one grounded capacitor. The complete structure of this memristor circuit is laid by cadence spectre tool 180nm TSMC CMOS technology. This circuit occupies $456 \mu\text{m}^2$ area excluding the area of the capacitor. The

post layout and experimental results are validating the emulator circuit. The mathematical equation for memristance of this grounded memristor is shown in equation (2.15).

$$W(\phi_{in}) = K(-V_{SS} - V_{TH-5}) - K \frac{(g_6 + g_7)\phi_{in}}{C} \quad 2.14$$

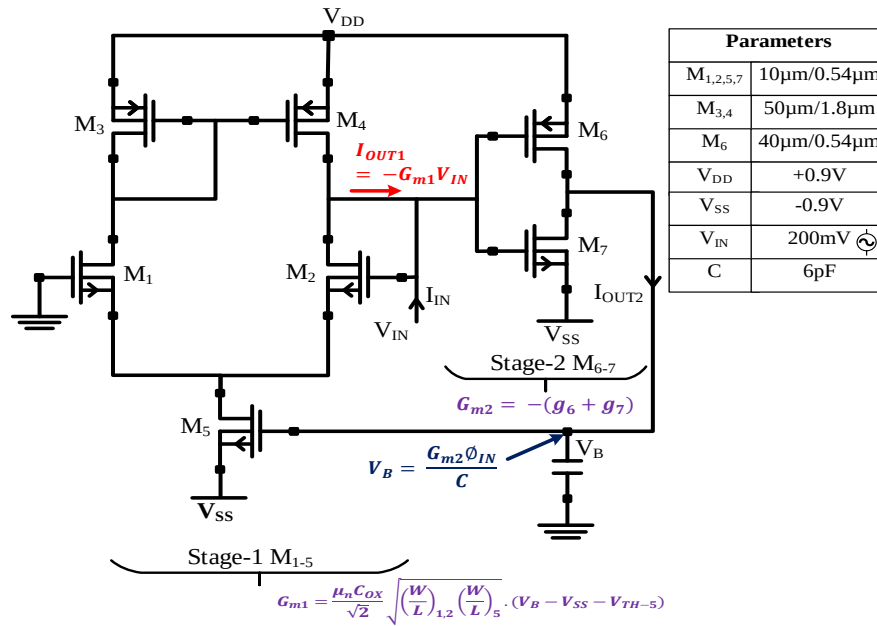


Figure 2.3 Memristor emulator proposed by Abdullah Yesil[50]

The author has also done the monte carlo analysis for the proposed memristor emulator for hundred different points observed that the emulator still operates in spite of mismatch of transistors and different process corners. This memristor emulator has been built on the breadboard using existing ALD1116 and ALD1117 transistors with DC supply $V_{DD} = -V_{SS} = 10V$ and the external capacitor with $10nF$ value. The simulation workability frequency and practical frequency upto 50MHz and 4MHz respectively.

The DT MOS [51] approach for memristor emulator was proposed by Pushkar, Rahul, Rajeev and Ravindra in Ref [52]. The proposed circuit has illustrated in Figure 2.4. Note that this is a novel approach and this circuit consists only three transistors (floating) and two transistors (grounded). This is remarkable point because it is the minimum transistor emulator circuit without using of any capacitor and DC biasing. Hence, it is fully passive memristor emulator.

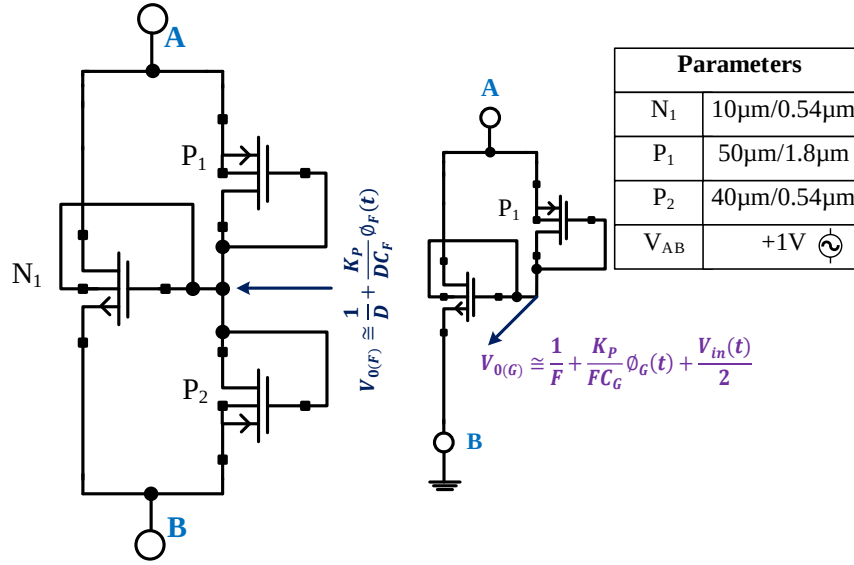


Figure 2.4 MOS-only memristor emulator circuit proposed by Pushkar, Rahul, Rajeev, and Ravindra[52]

The justification of the proposition has simulated using the cadence spectre tool 180nm GPDK parameters and experimentally verified by existing transistors ALD1116 and ALD1117. Authors has used DT MOS approach for varying the threshold voltage of N₁ transistor and fed back to the gate as a driving voltage for N₁ transistor. As input is varying threshold voltage also varies (shown in equation (2.16)) such that N₁ transistor operates in saturation region.

$$V_{THN1} = V_{THN1(0)} + \gamma \left(\sqrt{|2\psi_s + V_{SBN1}|} - \sqrt{2\psi_s} \right) \quad 2.15$$

$$\cong V_{THN1(0)} + K_B V_{SBN1}$$

The internal capacitance for floating and grounded composition of memristor emulator shown in equation (2.17).

$$C_F \cong C_G \cong W_{N1} L_{N1} C_{ox(N1)} + \frac{C_{sb0(P1)}}{1 + \frac{V_{in}}{2V_{THP1}}} \quad 2.16$$

The mendentance for both compositions are as follows:

$$W(\phi_F(t)) \cong \frac{K_N}{2} (K_B + 1) \left(\frac{1}{D} + \frac{K_P}{DC_F} \phi_F(t) \right) \quad 2.17$$

$$W(\phi_G(t)) \cong \frac{K_N}{2} (K_B + 1) \left(\frac{1}{F} + \frac{K_P}{FC_G} \phi_G(t) + \frac{V_{in}(t)}{2} \right) \quad 2.18$$

The main and important thing to notice about this emulator is power consumption and layout area. The static power consumption is zero and layout area is very less because only three or two transistors is used.

A different approach is presented by Babacan and Kacar in Ref [53]. They have used floating current source for memristor emulator circuit and the floating current source has been implemented by DTMOS. The DTMOS transistor are responsible for ultralow energy consumption. This FCS based memristor emulator circuit is represented in Figure 2.5. This emulator circuit is fully floating using only one FCS, one capacitor and two PMOS transistors. This circuit works in incremental and decremental when $V_P > V_N$ and $V_P < V_N$ respectively.

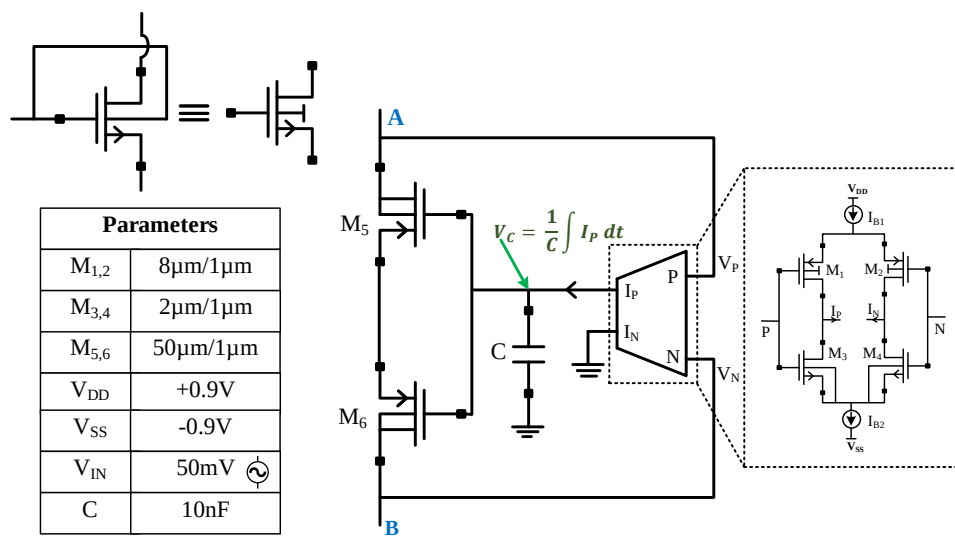


Figure 2.5 DTMOS approach memristor emulator proposed by Babacan and Kacar[53]

The bulk terminal of the PMOS transistors are connected to the drain of the transistor for operating in subthreshold region to obtain nonlinear characteristics. If the capacitor has lower value then the transistor can operated under the subthreshold region. The three important things of this circuit is high input resistor, efficient voltage control current source and ultra-low energy consumption. This emulator circuit can operated at very low frequency up-to 5Hz and behaves as a linear resistor at high frequencies. Hence this circuit is suitable for neuromorphic circuits. Author has presented associated learning circuit and analysed its learning activities.

The similar concept but different approach has been presented in the Ref. [54]. The authors has proposed OTA based memristor emulator circuit. This circuit consists of one OTA, one capacitor and two p-MOSs which shown in Figure 2.6. This circuit is fully floating and it operates in subthreshold region. The subthreshold region provide the high memristance value

and non-linear characteristics, which is the most important characteristics of memristor. The internal structure of OTA has shown in Figure 2.6.

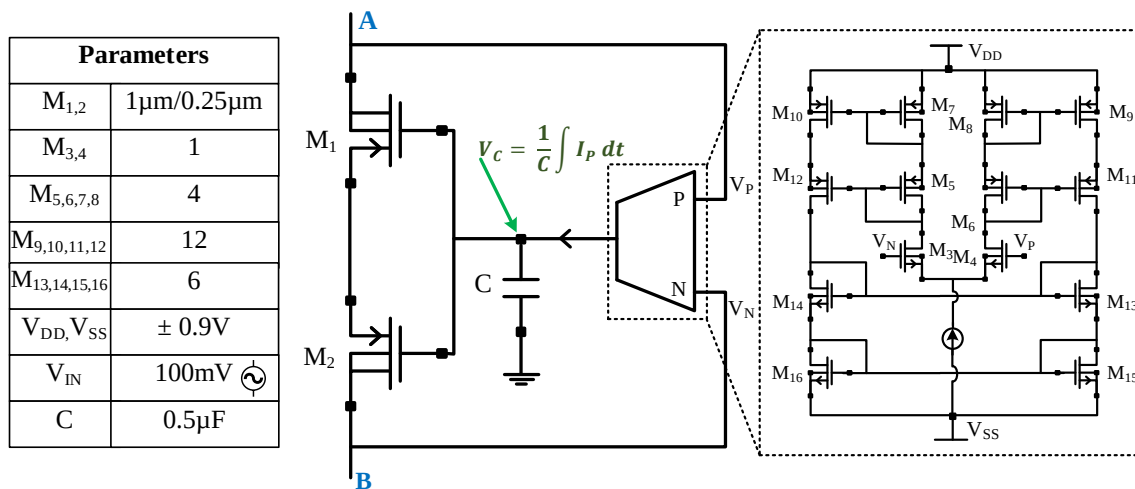


Figure 2.6 Memristor emulator circuit with subthreshold region proposed by Babacan and Kacar[54]

OTA is working as a voltage control current source and charged capacitor does not discharge when input signal does not exists. If the current of OTA flows through the capacitor, the capacitor start charging and voltage starts increasing and the charging time is $\tau = r_{gd} \cdot C$. The discharging time of capacitor is very long because of transistor high resistance then the negative terminal voltage becomes greater than the positive terminal voltage. Hence the current direction changes and flows from capacitor to OTA. The capacitor voltage drives the gate of the transistors and operates in subthreshold region. The advantage of fully floating memristor are the characteristics similar to real device and grounded device limit using the new devices.

Galin, Oscar, Stavros and Rodrigo [55] has presented a unique approach Switched capacitor for memristor emulator. This emulator circuit block diagram is shown in Figure 2.7. In this circuit author has utilized the switched capacitor technique for controlling the resistivity caused memristance. The control of this circuit is performed using pulse width modulation, which can be adapted very fast to changes in the values which simpler than a controlled pure resistance.

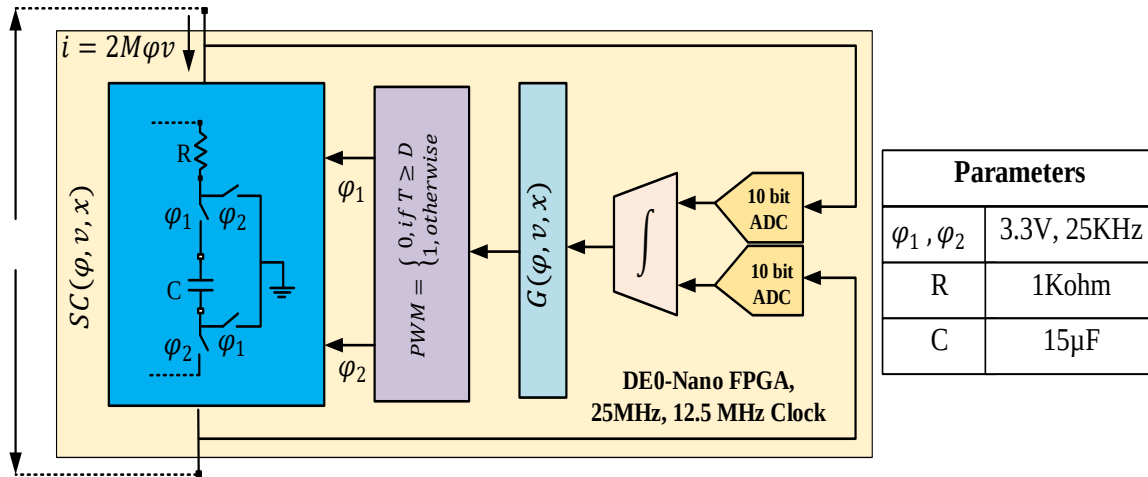


Figure 2.7 Switched capacitor approach for memristor emulator circuit proposed by Galin, Oscar, Stavros and Rodrigo[55]

This novel emulator circuit provides better linearity than that of a CMOS circuit, and a fine control that depends only on clock cycle not any analog value. This circuit is described mathematically in a general way by the equations (2.20-2.22):

$$i = G(\phi, v, x) \cdot v \quad 2.19$$

$$\dot{x} = g_\phi(\phi, v, x) \quad 2.20$$

$$\dot{\phi} = v \quad 2.21$$

Since the two controls signals ϕ_1 and ϕ_2 are equal in magnitude but 180° in phase difference. Hence the equivalent resistance of this circuit is

$$R_{eq} = R_0 + \frac{1}{f_s C} \frac{1 + \exp(\frac{DT}{\tau})}{1 - \exp(\frac{DT}{\tau})} \quad 2.22$$

This approach for memristor emulator is suitable for some hundred hertz of frequency even at 1 KHz frequency it shows a lot of noise. The main problem this presented memristor emulator was to design the control resistor stage but this novelty serves as a middle way in the transition from pure CMOS technology and implementing actual memristor devices.

Similar as above circuit design but a different approach has been presented in the Ref. [56]. In this approach presents an electronically adjustable memristor emulator circuit. It consists of only two MOS transistors and one current source which is shown in Figure 2.8.

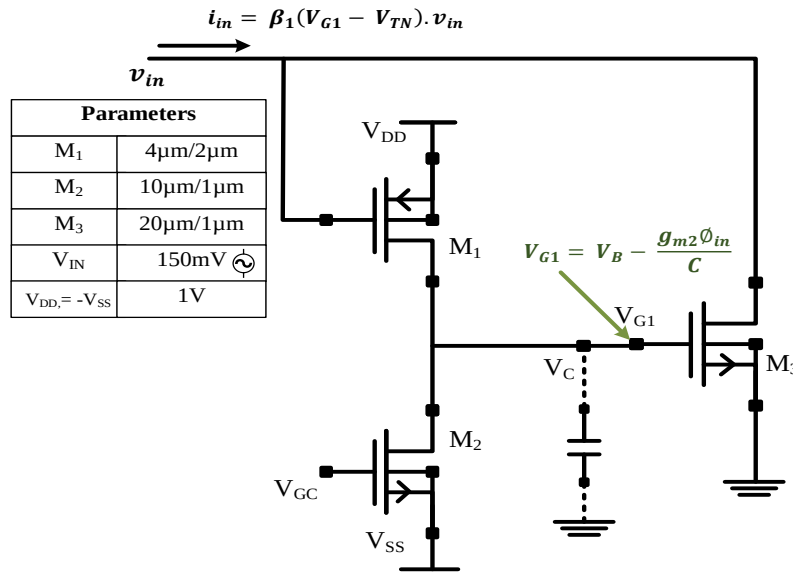


Figure 2.8 Electronically adjustable memristor emulator circuit proposed by Yildiz and Ozoguz[56]

In this approach the transistor internal capacitor is used as a memory element. Hence, this circuit takes a little space 122.4 μm². A modification technique also presented by the authors using NIC (negative impedance converter) for operating the memristor in active region which is shown in Figure 2.5. The simulation also done on the cadence spectre tool using UMC 180nm CMOS technology. This memristor works upto 40MHz frequency which is very good bandwidth as per high frequency application such as chaotic oscillator.

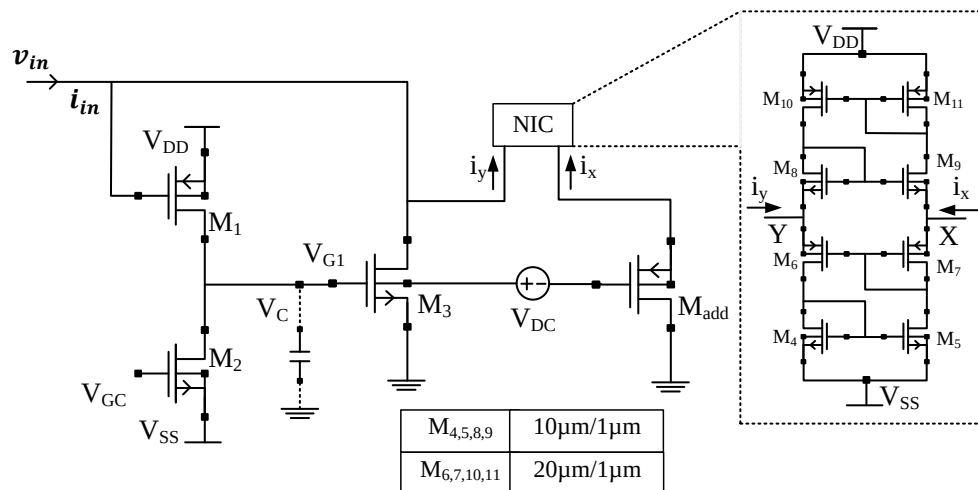


Figure 2.9 Modified emulator circuit using NIC (Negative Impedance Converter) proposed by Yildiz and Ozoguz[56]

In the presented MEC for the operating of M₃ transistor into linear region or triode region V_{DS} should be sufficiently small V_{DS} << V_{GS} - V_{TH}. V_{GC} acts as the control parameter of the memristor

and the intrinsic gate capacitor has been shown in dotted lines to show the memristive behaviour. VGC should be set appropriately. Hence the memristance of the above presented circuit is illustrated in the equation (2.24).

$$M_{eq}(\phi_{in}) = \left[\beta_1(V_{G1} - V_{TN}) - \beta_1 \frac{g_{m2}\phi_{in}}{C} \right] \quad 2.23$$

A generalized memristor with first order RC filter has been presented in Ref [57]. In this paper the memristor emulator circuit consists of diode bridge circuit and a first order parallel RC filter. This circuit is a voltage-controlled generalised memristor and it is shown in Figure 2.10. It means this circuit is fully passive element memristor emulator with six passive elements.

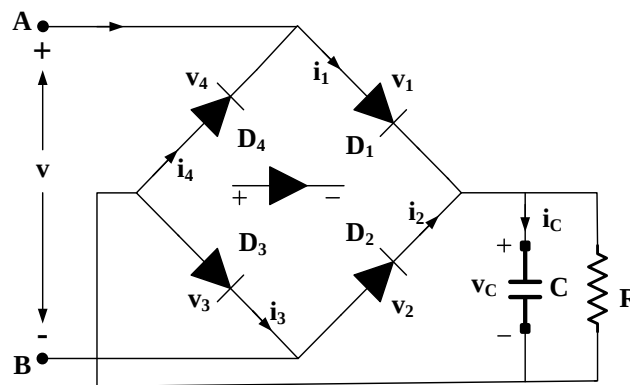


Figure 2.10 Generalized memristor using diode bridge circuit along with first order RC filter proposed by Bao, Yu, Hu and Liu[57]

The presented memristive circuit mathematical model is accord with the defined equations for the class of generalised memristor [58] and it is shown in equations (2.25-2.26) as follows:

$$i = g(v_c, v)v = 2I_S e^{-\rho v_c} \sinh(\rho v) \quad 2.24$$

$$\frac{dv_c}{dt} = f(v_c, v) = \frac{2I_S(e^{-\rho v_c} \cosh(\rho v) - 1)}{C} - \frac{v_c}{RC} \quad 2.25$$

This circuit has a satisfactory performance upto 10 KHz and there were variations in the pinched hysteresis loop for various amplitudes and it is noted that we can use different kinds of first order passive filters such as series RC, parallel RL and a series RL except parallel RC filter with the memristive diode bridge circuit. The circuit can generate the memristive behaviour for certain element parameters infact it can further have reduced to a diode bridge with an inductor. This approach is simpler and more intuitive and it is helpful to study memristor fundamentals and their applications such as colpitts chaotic oscillator [59], induced asymmetric attractor [60], and the XOR logic circuit [61].

Another application based approach of memristor emulator circuit is presented in Ref. [62]. Authors have presented a floating memristor emulator circuit, which supports STDP (Spike-Timing-Dependent Plasticity) characteristics. The proposed emulator circuit does not only emulates memristive and plasticity function but also fully floating characteristics. The circuit is illustrated in Figure 10. STDP as a family of learning mechanism in which neurons accumulate the input signals and when the input signal reaches the threshold of neurons and neuron starts fire. This fired signal is called spike. In the STDP two terms are important LTP (long term potentiation) and LTD(long term depression) which is pre-spike precedes the post-spike (neurons connection stronger) and post spike precedes the pre-spike (neurons connection weaker) respectively and demonstrated experimentally in [63]–[65]. STDP is described based on PSTDP (pair-based STDP) and this ruled is shown below:

$$\Delta w = \begin{cases} \Delta w^+ = A^+ e^{\left(\frac{-\Delta t}{\tau_+}\right)}, & \text{if } \Delta t > 0 \\ \Delta w^- = A^- e^{\left(\frac{-\Delta t}{\tau_-}\right)}, & \text{if } \Delta t \leq 0 \end{cases} \quad 2.26$$

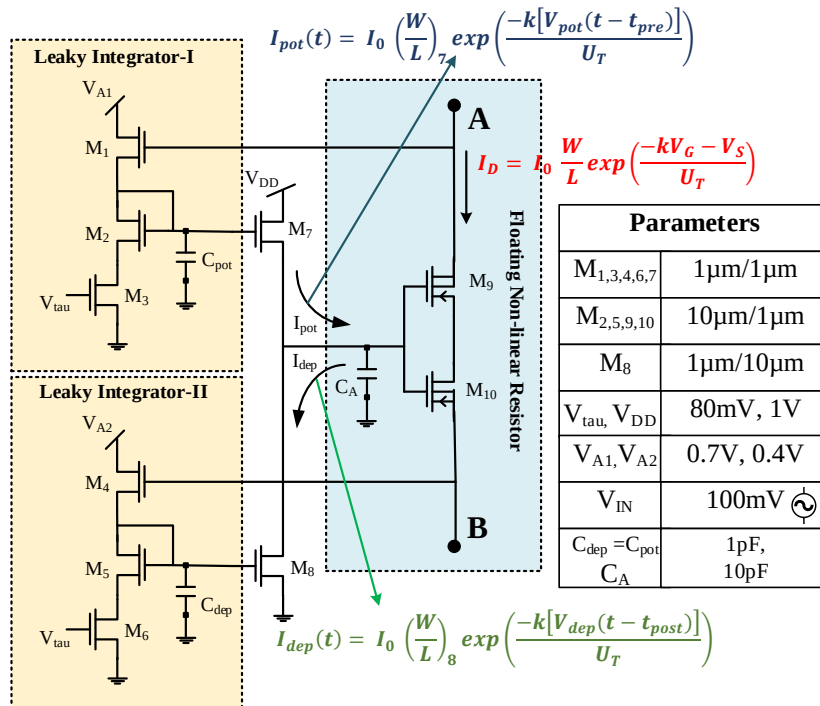


Figure 2.11 Memristor emulator with spike-timing-dependent-plasticity proposed by Babacan and Kacar[62]

This circuit consists of two parts as floating non-linear resistor and leaky integrator circuit. Floating non-linear resistor based on subthreshold region operated MOS transistors. For these

two symmetric connected p-MOS is used. Leaky integrator circuit is very important to provide synaptic rules LTP and LTD. Designed memristor emulator circuit consists of twelve MOS transistors and one capacitor. Since, this emulator, circuit resistance is very high so, very low current flows through the designed memristor emulator. Hence, this circuit consumes very less power. The memristive characteristics has been simulated using TSMC 180nm CMOS process model parameters and applied 100mV sinusoidal signal to proposed memristor emulator. The higher operating frequency of the designed memristor emulator is 5Hz, which is suitable for neuromorphic applications. Authors has presented the synaptic characteristics (LTP and LTD) in the manuscript, which is similar to biological synapse.

Table 2.1 highlights a concise comparison of the various memristor emulators.

Table 2. 1 Comparison of Different Memristor Emulators

Ref	MOSFET Count	Active/ Passive Components Used	Floating/ Grounded	Operating Frequency	Power Consumption	Technology Used
[47]	3	C-1	Floating	13MHz	6.725nW	0.18 μ m TSMC
[49]	4	-	Grounded	100MHz	Few nW	0.18 μ m TSMC
[50]	7	C-1	Grounded	50MHz	Few nW	0.18 μ m TSMC
[52]	2, 3	-	Grounded/ Floating	30MHz	Zero	0.18 μ m GPDK
[53]	6	C-1	Floating	10Hz	Few nW	0.18 μ m TSMC
[54]	16	OTA-1, C-1	Floating	30Hz	Few mW	0.18 μ m TSMC
[55]	»60	Nano FPGA, ADC-2, R-1, C-1	Floating	1KHz	in mW	-
[56]	3	C-1	Grounded	40MHz	in nW	0.18 μ m UMC
[57]	-	D-4, R-1, C-1	Grounded/ Floating	10KHz	—	—
[62]	10	C-3	Floating	5Hz	in nW	0.18 μ m TSMC

2.2. Literature on Memcapacitor Emulators

Memcapacitance C_M arises as a result of the non-linear relationship between the charge flowing through the device (q) and applied input signal (v) to the device. A n^{th} order VCMS (voltage-controlled memcapacitive system) is defined by the equation

$$q(t) = C_M(x_n, v, t)v(t) \quad 2.28$$

$$\dot{x} = f(x_n, v, t) \quad 2.29$$

whereas a n^{th} order CCMS (charge-controlled memcapacitive systems) is given by the equation

$$v(t) = C_M^{-1}(x_n, q, t)q(t) \quad 2.30$$

$$\dot{x} = f(x_n, q, t) \quad 2.31$$

where, x_n is the vector with n internal state variables and C_M^{-1} is the inverse memcapacitance.

A memcapacitor is a capacitor whose capacitance changes according to the previous states of the input variable acting on it. The memcapacitance is represented through a q - v closed pinched hysteresis loop. The main characteristic of this pinched hysteresis loop is a zero crossing behaviour wherein if $v = 0$ then $q = 0$ for any type of a sinusoidal input signal.

The memcapacitor is the category of a memcapacitive system with one state variable. In such a scenario, for a voltage controlled memcapacitor, Equations 2.28 and 2.29 reduce to

$$q(t) = C_M \left[\int_{t_0}^t v(\tau) d\tau \right] \cdot v(\tau) \quad 2.32$$

and for a current controlled memcapacitor, Equations 2.30 and 2.31 reduce to

$$v(t) = C_M^{-1} \left[\int_{t_0}^t q(\tau) d\tau \right] \cdot q(\tau) \quad 2.33$$

Where, t_0 = initial state of time, t_0 should be satisfy the condition that $\int_{-\infty}^{t_0} v(\tau) d\tau = 0$ and $\int_{-\infty}^{t_0} q(\tau) d\tau = 0$.

A memcapacitor emulator is presented by Hosbas and Kacar in Ref. [66]. In this paper, the authors have transformed memristor into a memcapacitor with the help of a mutator circuit. The memristor emulator and mutator circuit were both implemented using voltage difference transconductance amplifier (VDTA) and one capacitor each. This proposed circuit has two parts, a mutator circuit, and a memristor circuit, both of which are shown in Figure 2.12. The memcapacitance value for this emulator can be electronically controlled.

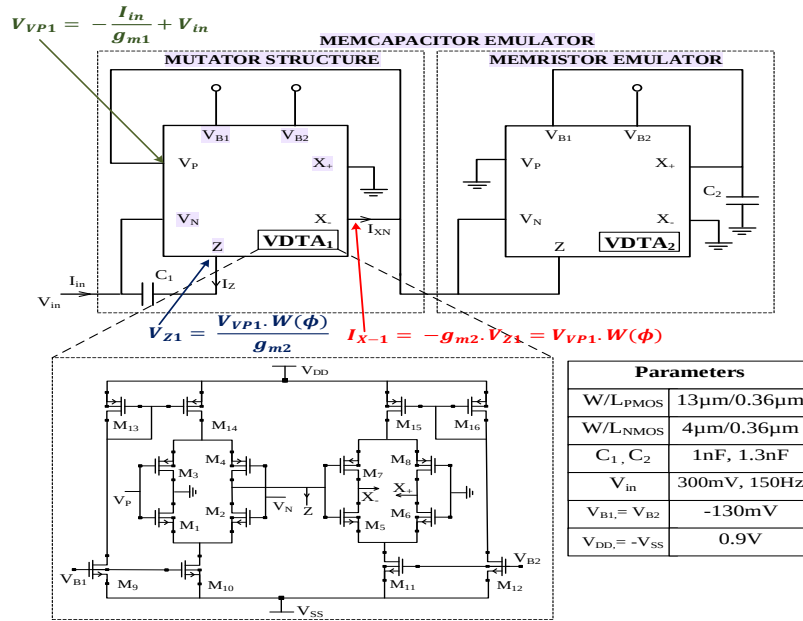


Figure 2.12 Memcapacitor emulator circuit using memristor and mutator circuit presented by Hosbas and Kacar [66]

According to the proposed circuit the current-voltage relationship of the VDTA is given by a matrix transformation

$$\begin{bmatrix} I_Z \\ I_{X+} \\ I_{X-} \end{bmatrix} = \begin{bmatrix} g_{m1} & -g_{m1} & 0 \\ 0 & 0 & g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_{VP} \\ V_{VN} \\ V_Z \end{bmatrix} \quad (2.34)$$

When the capacitor is replaced by a MOSFET behaving as a capacitor, commonly referred to as a MOSCAP, a better high-frequency performance is witnessed.

The inverse memcapacitance of this configuration has been calculated, shown in below equation

$$D_M = \frac{V_{IN}}{q(t)} = \frac{g_{m2}}{C_1(g_{m2} + W(\varphi))} + \frac{W(\varphi)I_{IN}}{g_{m1}(g_{m2} + W(\varphi)) \int I_{IN} dt} \quad (35)$$

where $W(\varphi) = K_1(-V_{SS} - V_{TH}) \pm \frac{g_{m2}K_1\varphi_{IN}}{C_2}$ is defined as the memductance of the memristor.

This circuit is simulated using LT-spice simulation software with TSMC 0.18μm process parameters. Instead of attempting to construct a new memcapacitor, this study successfully converts an existing memristor into a memcapacitor using a mutator circuit. The performance of the memcapacitor emulator circuit was examined at various frequencies up to 500Hz. In addition to the simulation results, the circuit characteristics have also been verified

experimentally using an existing active element (*LM13700*) and six passive elements. The authors have used and varied the capacitance of an external capacitor to evaluate the performance of the circuit at different frequencies.

A memcapacitor emulator circuit has been presented by Fouda and Radwan in Ref. [67]. In this script, the authors have proposed a design to emulate the memcapacitance using the rate of change of an applied voltage difference between the input terminals of the operational amplifier as shown in Figure 2.13. In this configuration, authors have used four OP-AMPs, one multiplier, some resistors and capacitors along with a current controlled source. This circuit follows the mathematical equation of a CCMC (charge-controlled memcapacitor) proposed by Biolek et al. [68] and it is given as Equation 2.36.

$$\frac{1}{C_M(t)} = \frac{1}{C_0} + k' \int_0^t q(\tau) d\tau \quad 2.36$$

To derive an equation similar to the Equation 2.36 for the model given in Figure 2.12, the authors begin by expressing current across the input capacitor, C_{in} as:

$$i_{in}(t) = C_{in} \frac{d(v_{in} - v_{FB})}{dt} \quad 2.37$$

A series of mathematical calculations involving integration and substitution of V_{FB} as given in Figure 2.13 yields the Equation 36:

$$v_{in}(t) = \frac{q(t)}{C_{in}} + \frac{q(t)}{RC_2C_1^2} \int_0^t q(\tau) d\tau \quad 2.38$$

2.39 which is similar to the form given an Equation 2.36.

$$C_M^{-1} = \frac{1}{C_{in}} + \frac{1}{RC_2C_1^2} \int_0^t q(\tau) d\tau \quad 2.39$$

This circuit is simulated using PSPICE and has been demonstrated as a charge-controlled memcapacitor operating at frequencies up to 10Hz. This work is entirely mathematical, and simulation has been performed to verify memcapacitor characteristics. No experimental verification of the proposed topology has been undertaken.

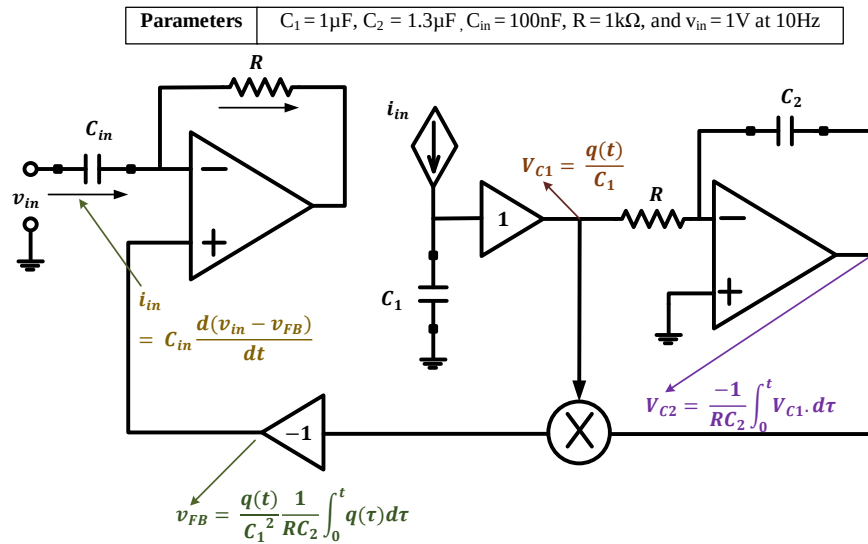


Figure 2.13 Memcapacitor emulator circuit proposed by Fauda and Radwan [67]

dividing Equation 38 throughout by $q(t)$, inverse memcapacitance C_M^{-1} is given by Equation Sah et al. in Ref [69] suggested a similar strategy without the requirement of a copy of the input current as a current controlled source (see Figure 2.13 for information about the current controlled source). The diode IN4148 ensures that the voltage at the output of the integrator remains negative in order to ensure that the circuit given in Figure 2.14 emulates a memcapacitor. The mathematical model of the proposed memcapacitor model is described by Equation 40 by adhering to the same idea as propounded by Fouda and Radwan in ref. [67]. The input voltage for this model therefore can be written as

$$v_{in}(t) = \frac{q(t)}{C_1} + \frac{q(t)}{RC_2 C_1^2} \int_0^t q(\tau) d\tau \quad (40)$$

Parameters	$C_2 = 1\mu\text{F}$, $C_1 = 100\mu\text{F}$, $R = 50\text{k}\Omega$, and $v_{in} = 1\text{V}$ at 0.1Hz to 25Hz , D1N4148
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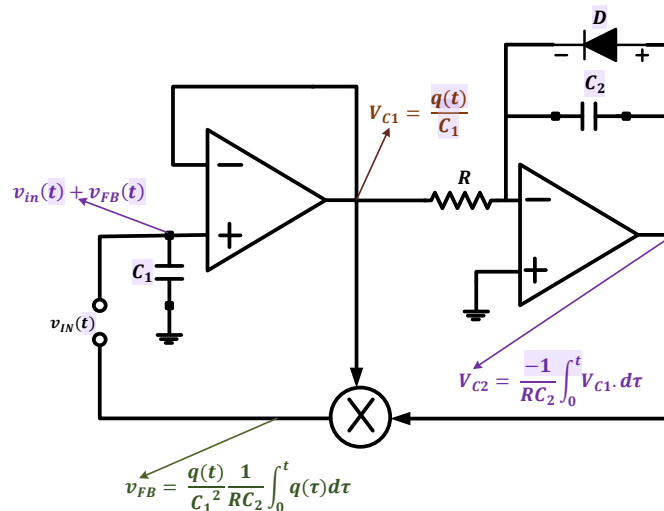


Figure 2.14 Memcapacitor emulator circuit presented by Sah et al. [69]

The authors have demonstrated that this model can accurately simulate a charge-controlled memcapacitor, operating frequencies ranging from 1 Hz to 25 Hz by using PSPICE simulations. The experimental verification has been done using existing elements such as two OP-AMPs, capacitors, resistors, a diode, and one multiplier block. The circuit has a simpler design and delivers a behavior similar to the one given in Figure 2.13.

A grounded memcapacitor was presented by Romero et al. in Ref. [70] using Miller effect. This memcapacitor emulator is a voltage-controlled memcapacitor which is shown in Figure 2.15. The input impedance of the circuit is as follows:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{IN}}{j\omega C_1(V_{IN} - V_{OUT})} = \frac{1}{j\omega C_1(1+A)} \quad 2.41$$

where A is the flux-dependent gain and the input impedance of the memcapacitor is $\frac{1}{1+A}$ times the feedback capacitor reactance. The authors have used a voltage-controlled resistor to change the amplifier circuit gain as per flux. In the emulator, a memristor can replace a voltage-controlled resistor for controlling the gain. The voltage-controlled memcapacitance of the proposed memcapacitor is derived in Equations 2.42, 2.43 and 2.44, given below:

$$\frac{d\sigma_{IN}}{dt} = \int C_1 \frac{dv_{C1}(t)}{dt} dt = C_1(v_{IN}(t) - v_{OUT}(t)) = C_M(\phi)v_{IN}(t) \quad 2.42$$

from the above the resulting memcapacitance is as:

$$C_M(\phi) = C_1 \left(2 + \frac{R_1}{R_V(\phi)} \right) \quad 2.43$$

$$C_M(\phi) = C_1 \left(2 + \frac{R_1}{R_M(\phi)} \right) \quad 2.44$$

The Equation 2.43 represents the memcapacitance as a function voltage-controlled resistor, and Equation 2.44 represents the memcapacitance as a function the memristance in place of a controlled resistor. It is evident from Equation 43 that a memristor can simulate a memcapacitor through a mutator circuit. It shall be seen in some later examples that even a meminductor emulator can be realized by using memristors along with a mutator circuit.

The simulation of the proposed memcapacitor emulator was done using PSPICE software. The operating frequency of this emulator circuit was up to 50Hz. The authors have also done the experimental verification with field programable analog array (FPAA) using a controlled-gain amplifier.

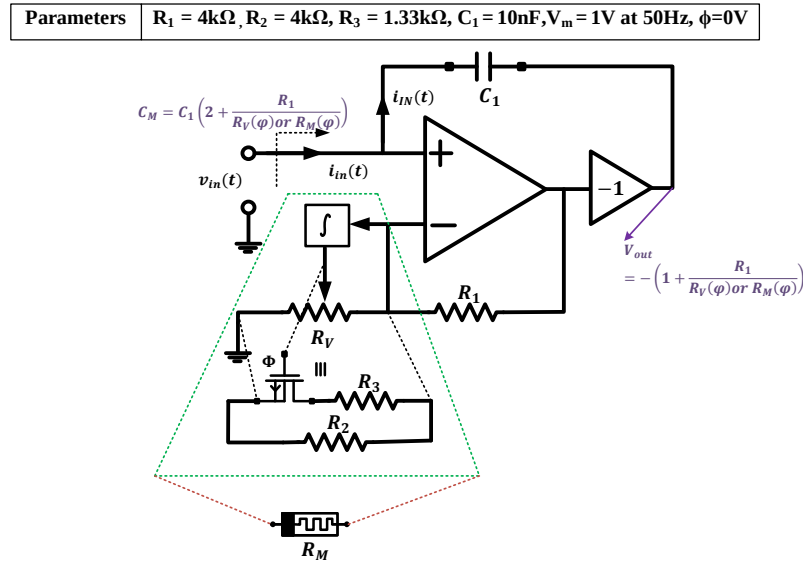


Figure 2.15 Memcapacitor emulator based on miller effect and replacement of voltage-controlled resistor with a voltage-controlled memristor, proposed by Romero et al. [70]

Pershin and Ventra in Ref. [71] introduce the theory of current conveyor circuits in mutator-based emulator models. The main benefit of using current conveyor circuit is the possibility of implementing floating memcapacitor emulators. The memcapacitor emulator based on this concept is shown in Figure 2.16. The memristor current and inductor L_1 current. Since in the current conveyor circuit, the voltage at the terminal of X and Y are equal, hence,

$$V_X = V_Y \quad 2.45$$

$$-i_{IN}(t) \cdot R_1 = \frac{-L_1}{R_M(\phi)} \cdot \frac{d(v_{IN}(t))}{dt} \quad 2.46$$

The Equation 2.46 present the memcapacitance of voltage-controlled memcapacitor and Iit is given by

$$C_M(\phi) = \frac{L_1}{R_1 R_M(\phi)} \quad 2.47$$

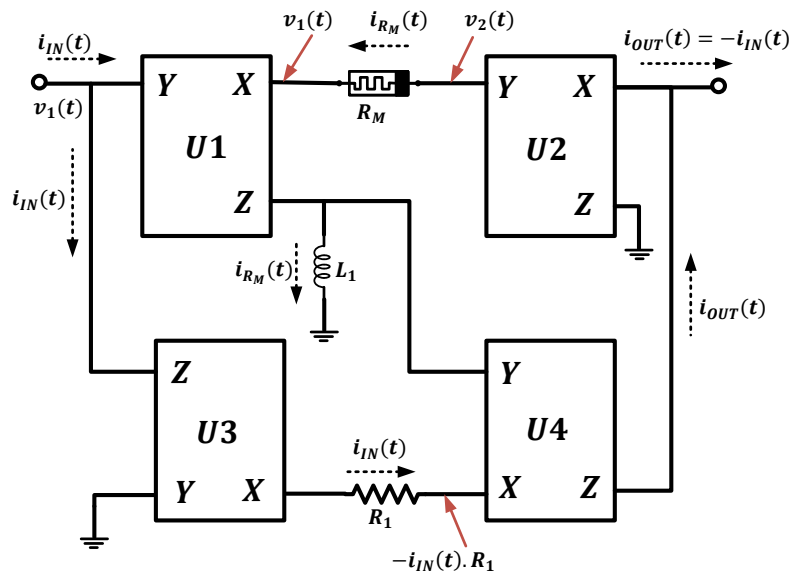
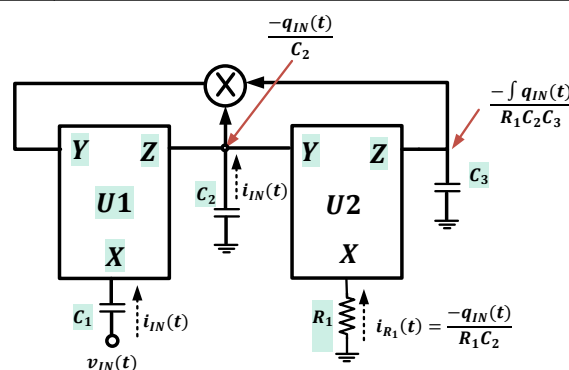


Figure 2.16 Mutator based memcapacitor emulator presented by Pershin and Di Ventra [71]

The proposed memcapacitor emulator circuit is analyzed using only a mathematical model. No simulation and experimental verification has been undertaken to verify the mathematical model of memcapacitor.

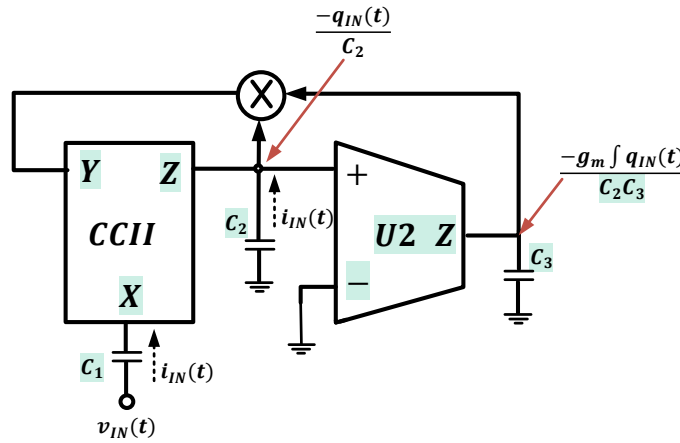
Yesil and Babacan [72] have presented two memcapacitor emulator circuits, the first circuit has been developed using two second-generation current conveyor (CC-II) circuits whereas the second circuit has been conceptualized using a combination of a single CC-II and an OTA. The two circuits are shown in Figure 2.17(a) and Figure 2.17(b). This approach avoids the implementation using a memristor emulator circuit and therefore the circuit design is not mutator-based. This reduces the complexity of the circuits.

Parameters	$R_1 = 500\Omega$, $C_1 = 2\mu\text{F}$, $C_2 = 1\mu\text{F}$, $g_m = 2\text{mA/V}$, $V_m = 3\text{V}$
------------	--



(a)

15



(b)

Figure 2.17 Memcapacitor emulator circuit based on CC-II and OTA proposed by Abdulla and Yesil [72]. a) based purely on CC-II, b) based on a combination of a CC-II and an OTA.

In the CC-II based memcapacitor emulator shown in Figure 2.17(a), the input current and memcapacitance have been derived using Equations 2.48 and 2.49.

$$i_{IN}(t) = C_1 \frac{d(v_{IN}(t) - \frac{q(t)}{R_1 C_2^2 C_3})}{dt} \quad 2.48$$

$$\frac{1}{C_M(q)} = \frac{1}{C_1} + \frac{1}{R_1 C_2^2 C_3} \int_{t_0}^t q(t) dt \quad 2.49$$

The memcapacitance of the second configuration (using CC-II and OTA based) shown in Figure 2.17 (b) has been derived and shown below

$$\frac{1}{C_M(q)} = \frac{1}{C_1} + \frac{g_m}{C_2^2 C_3} \int_{t_0}^t q(t) dt \quad 2.50$$

where, g_m is the transconductance of OTA.

The simulation results have been corroborated by experimental results using existing integrated circuits such as AD844s and AD633s. The proposed memcapacitor emulator is a charge-controlled circuit operated in the grounded mode. Both approaches are electronically controlled by changing the value of the equivalent resistor, which is implemented using two PMOS transistors. The operating frequency of the proposed circuit is up to 2KHz.

A grounded memcapacitor emulator has been discussed by Madsar et al. in Ref. [73], and is

9

3

shown in Figure 2.18. The authors have used a DTMOS floating current source (FCS) for this approach to the design of memcapacitor emulator. The floating current source consumes very little power. The relationship between currents flowing in the floating current source is given by Equation 2.51 and 2.52.

$$I_{B1} - I_{B2} + (I_P + I_N) = 0 \quad 2.51$$

$$I_{B1} = I_{B2} \text{ and } I_P = -I_N \quad 2.52$$

where I_{B1} and I_{B2} are the bias currents and I_P and I_N are FCS output currents. At node A, the voltage is given by

$$V_A = \frac{q(t)}{(C_1)^2} \int q(t) d(t) \quad 2.53$$

The voltage V_A shows a nonlinear change with respect to the charge $q(t)$. Here $q(t)$ is a controlled parameter, which provides memcapacitor characteristics to the emulator. Hence the circuit is a charge-controlled grounded memcapacitor emulator. The circuit is useful for low-frequency applications since the working frequency of the proposed memcapacitor is up to 7Hz.

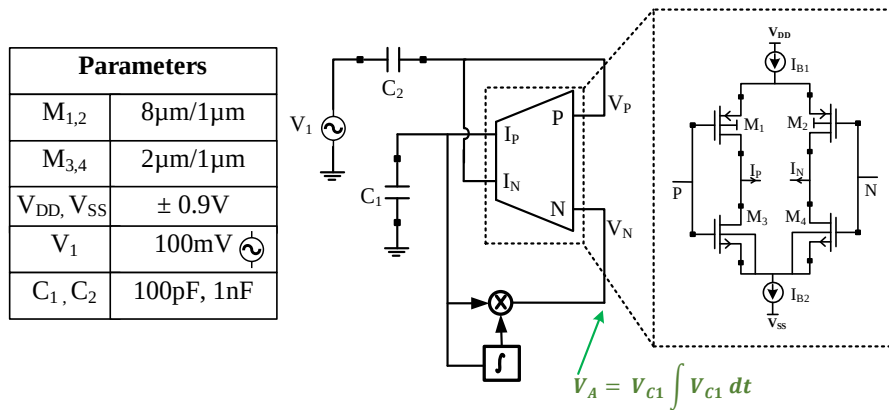
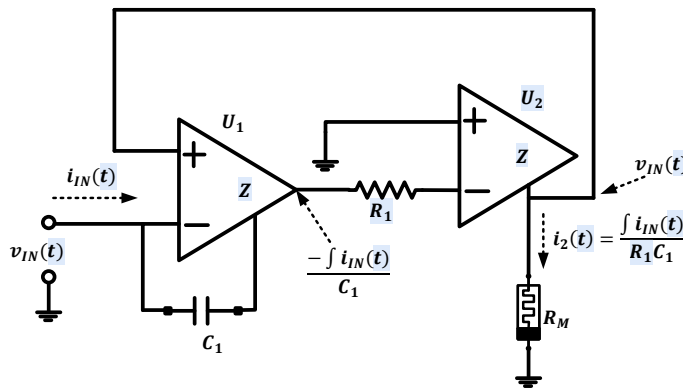


Figure 2. 18 FCS-based memcapacitor emulator presented by Madsar et al. [73]

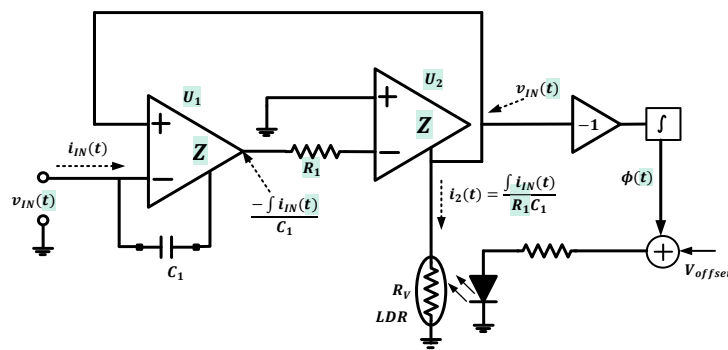
A voltage-controlled, mutator-based memcapacitor emulator was proposed by Wang et al. [8] shown in Figure 2.19(a) and 2.19(b). The authors have presented two approaches for implementing the memcapacitor emulator circuit. In the first approach, the authors have utilized two commercially available second-generation current conveyors (CC-II) and a

memristor (see Figure 2.19(a)). In the second approach, the authors have used a combination of light emitting diode and light-dependent resistor commonly known as a photocoupler, in place of a memristor to provide variable resistance as depicted in Fig. 2.19(b). In the circuit shown in Figure 2.19(b), the first CC-II circuit integrates the input current to produce a voltage proportional to the charge and the second CC-II circuit converts the voltage into a current which is then fed back to first CC-II integrator circuit using the relationship $I_Z = -I_-$ and $V_- = V_+$. The current flowing through the memristor becomes

$$i_2(t) = I_{Z2} = \frac{-v_{out1}}{R_1} = \frac{1}{R_1 C_1} \int_{t_0}^t i_{IN}(\tau) d\tau = \frac{q(t)}{R_1 C_1} \quad 2.54$$



(a)



(b)

Figure 2. 19(a) Memcapaitor emulator circuit proposed by Wang et al. [8] using voltage-current memristor (b) LED-LDR-based memcapacitor emulator schematic

The memristance of the proposed circuit is given by

$$R_M(\phi) = \frac{v_{IN}(t)}{i_2} = \frac{v_{IN}(t)R_1C_1}{q(t)} \quad 2.55$$

The equivalent memcapacitance of a memristor circuit can then be derived from its constitutive equation

$$C_M(\phi) = \frac{R_1C_1}{R_M(\phi)} \quad 2.56$$

In the second approach, the authors have introduced a new technique for handling VDRs (voltage-dependent resistors) and/or voltage-controlled memristors. This approach involves using a LED (light-emitted diode) that is optically coupled with an LDR (light-dependent resistor) as shown in Figure 2.19(b). It is important to note that the use of LDRs may limit the maximum frequency of the memcapacitor emulator because they typically have a slow response time. The operating frequency range of this circuit is 0.1Hz to 280 Hz.

Vista and Ranjan [74] have proposed a dual X current conveyor differential input transconductance amplifier (DXCCDITA) based memcapacitor emulator, which consists of two capacitors and one resistor as shown in Figure 2.20. The memcapacitance can be determined from the voltages ($v_{C_1}(t)$, $v_{C_2}(t)$, $V_Y(t)$) across the passive components C_1 , C_2 , and R_1 . The voltages $v_{C_1}(t)$, $v_{C_2}(t)$, and $V_Y(t)$ are given in Equations 2.57, 2.58 and 2.59 respectively.

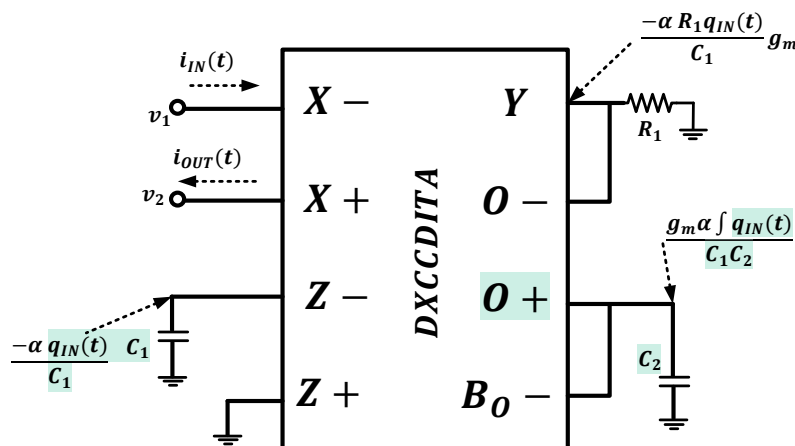


Figure 2. 20 DXCCDITA based memcapacitor emulator proposed by Vista and Ranjan [74]

$$v_{C_1} = v_{Z-} = \frac{1}{C_1} \int_{t_0}^t i_{C_1}(t) dt = \frac{1}{C_1} \int_{t_0}^t i_{Z-}(t) dt = \frac{\alpha}{C_1} \int_{t_0}^t i_{X-}(t) dt = \frac{\alpha q_{IN}(t)}{C_1} \quad 2.57$$

$$v_{c_2}(t) = V_{O_+}(t) = V_{B_{O_-}}(t) = \frac{1}{c_2} \int_{t_0}^t i_{O_+}(t) dt = \frac{g_m}{c_1} \int_{t_0}^t V_{Z_-}(t) dt = \frac{\alpha g_m}{c_2 c_1} \int_{t_0}^t q_{IN}(t) dt \quad 2.58$$

$$V_Y(t) = \frac{V_{X_+}(t)}{\beta} = \frac{-V_{X_-}(t)}{\beta} = V_{O_-}(t) = I_{O_-}(t) R_1 = -g_m V_{Z_-}(t) R_1 = \frac{-g_m \alpha q_{IN}(t) R_1}{c_1} \quad 2.59$$

The DXCCDITA input-output voltage current matrix is shown in the Equation 2.60.

$$\begin{bmatrix} I_Y \\ V_{X_+} \\ V_{X_-} \\ I_{Z_+} \\ I_{Z_-} \\ I_{O_{\pm}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ \beta & 0 & 0 & 0 & 0 & 0 \\ -\beta & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha & 0 & 0 & 0 & 0 \\ 0 & 0 & \alpha & 0 & 0 & 0 \\ 0 & 0 & 0 & \mp g_m & \pm g_m & 0 \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_{X_+} \\ I_{X_-} \\ V_{Z_+} \\ V_{Z_-} \\ V_{O_{\pm}} \end{bmatrix} \quad 2.60$$

Consequently, Equation 2,61 defines the behavior of the charge-controlled memcapacitor emulator circuit.

$$v_{IN}(t) = V_{X_-}(t) - V_{X_+}(t) = -2\beta V_Y = \frac{2\alpha\beta K R_1}{c_1} \cdot q(t) \quad 2.61$$

Hence the memcapacitance of CCMC (charge-controlled memcapacitor) is given by

$$\frac{1}{C_M(q)} = \frac{2\alpha\beta K R_1}{c_1} \cdot (V_{DD} - V_T + \frac{\alpha g_m}{c_1 c_2} \int_{t_0}^t q_{IN}(t) dt) \quad 2.62$$

The simulation has been performed using PSPICE. The proposed model has been tested in an adaptive neuromorphic structure [74] to validate its functioning. The emulator circuit can operate upto 1 MHz.

Table 2. 2 Comparison of memcapacitor emulators

Ref	Transistor Count	Components Used	Mutator	Grounded/ Floating	Control Variable	Operating Frequency
[66]	16	VDTA-1, C-1	Yes	Grounded	Charge	500Hz
[67]	»30	OPAMP-2, Multiplier-1, Copy of Input Current	No	Grounded	Charge	10Hz
[69]	»30	OPAMP-2, Multiplier-1, D-1, C-2, R-1	No	Floating	Charge	25Hz
[70]	»12	OPAMP-1, Memristor-1, C-1, R-1	Yes	Grounded	Voltage	50Hz
[71]	»50	CC-II+-4, C-1, R-1	Yes	Floating	Voltage	NA
[72]	»50	CC-II-2, Multiplier-1, C-3, R-1	No	Grounded	Charge	2KHz
[73]	4	C-2, Multiplier-1, Integrator-1	No	Grounded	Charge	7Hz
[8]	»30	CC-II, Memristor-1, R-	Yes	Grounded	Voltage	10Hz

		1, C-1, LDR-1				
[74]	30	DXCCDITA-1, C-2, R-1	No	Floating	Charge	1MHz

2.3. Literature on Meminductor Emulators

The meminductance (L_M) is a n^{th} order system that establishes a nonlinear relation between the current (i) across the terminal of the device and its input flux (ϕ) [39]. Depending on its constitutive input variables, the meminductor can either be current-controlled or flux-controlled. The n^{th} order CCMS (current-controlled meminductive systems) are defined by the equation

$$\phi(t) = L_M(x_n, i, t)i(t) \quad 2.63$$

$$\dot{x} = f(x_n, i, t) \quad 2.64$$

whereas a n^{th} order FCMS (flux-controlled meminductive system) is given by the equation

$$i(t) = L_M^{-1}(x_n, \phi, t)\phi(t) \quad 2.65$$

$$\dot{x} = f(x_n, \phi, t) \quad 2.66$$

where, x_n is the vector with state variables and L_M^{-1} is the inverse meminductance.

The meminductor is a type of inductor whose inductance depends on the history of successive variables that act as the input. The meminductance is represented through a $(i - \phi)$ closed pinched hysteresis loop. The main characteristic of this pinched hysteresis loop is a zero crossing behaviour wherein if $i = 0$ then $\phi = 0$ and vice versa for any sinusoidal input signal.

The meminductor is the category of a meminductive system with one state variable. In such a scenario, for a flux-controlled meminductor, Equations 2.63 and 2.64 reduce to

$$i(t) = L_M^{-1} \left[\int_{t_0}^t \phi(\tau) d\tau \right] \phi(\tau) \quad 2.67$$

and for a current-controlled meminductor, Equations 2.65 and 2.66 reduce to

$$\phi(t) = L_M \left[\int_{t_0}^t i(\tau) d\tau \right] i(\tau) \quad 2.68$$

Where, t_0 is the initial state of time and t_0 should be satisfy the condition that $\int_{t_0}^t i(\tau) d\tau = 0$ and $\int_{t_0}^t \phi(\tau) d\tau = 0$.

Wang [75] proposed a grounded meminductor emulator circuit that consists of a gyrator (similar to a mutator circuit) for transforming a memristor into a meminductor. The emulator circuit is shown in Figure 2.21. A gyrator circuit is an electronic circuit that simulates the behavior of an inductor using active components (such as transistors or operational transconductance amplifiers) and passive components (resistors).

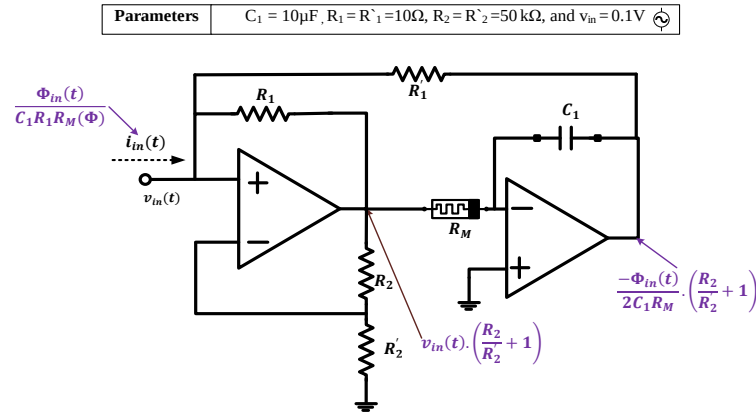


Figure 2. 21 Meminductor emulator circuit proposed by Wang [75]

The input current in the proposed circuit is expressed as given in the equation

$$i_{in}(t) = i_{R_1} + i_{R'_1} = v_{in}(t) \cdot \left(\frac{1}{R'_1} - \frac{R_2}{R_1 R'_2} \right) + \frac{\phi_{in}(t)}{2 R_2 R_M(\phi) C_1} \cdot \left(\frac{R_2}{R'_2} + 1 \right) \quad 2.69$$

If $R'_1 = R_1$ and $R'_2 = R_2$, Equation 2.69 can be reduces to much simpler equation given by Equation 2.70. Hence, the flux control meminductance is given by Equation 2.71.

$$i_{in}(t) = \frac{\phi_{in}(t)}{R_1 R_M(\phi) C_1} \quad 2.70$$

$$L_M(\phi) = R_1 R_M(\phi) C_1 \quad 2.71$$

Although this basic model was validated through simulations, it has not been analyzed experimentally using discrete components or existing blocks.

Romero et al. [76] presented an alternative mutator based meminductor emulator design using a Reordan gyrator circuit, as shown in Figure 2.22.

In the floating type meminductor, the input and output current are equal in magnitude but opposite in direction. The input current can be expressed as

$$i_{in} = v_{in} \cdot \frac{R_2 C_1}{R_4 R_M R_1} = -v_{in} \cdot \left(\frac{R_6}{R_7 R_5} + \frac{R_2 C_1 R_6}{R_M R_4 R_5 R_7} - \frac{1}{R_4} \right) \quad 2.72$$

For the circuit in Figure 2.22, the below mentioned relationship must hold

$$\frac{1}{R_4} = \frac{1}{R_1} = \frac{R_6}{R_5 R_7} \quad 2.73$$

Parameters	$R_1 - R_7 = 1 \text{ k}\Omega$, $C_1 = 47 \mu\text{F}$, $V_{in} = 1\text{V}$ at 13Hz , and $V_{offset} = 1.8\text{V}$
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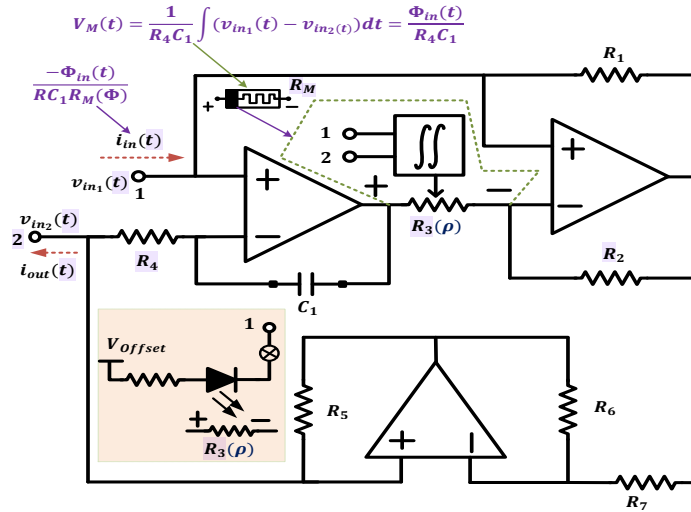


Figure 2. 22 Floating meminductor emulator using Reordan Gyrator presented by Romero et al. [76]

Considering R_3 as a flux-controlled impedance, and $R_1 = R_2 = R_5 = R_6 = R_7 = R_8 = R$, and applying Laplace transformation to Equation 2.72

$$I_{in}(s) = \frac{V_{in}(s)}{s} \cdot \frac{1}{RC_1 R_M(\phi(s))} \quad 2.74$$

The meminductance can be derived by the taking the inverse Laplace transform of Equation 2.74

$$L_M(\phi) = RC_1 R_M(\phi) \quad 2.75$$

The simulation for this emulator circuit has been done using PSPICE software and the experimental verification has been done using the existing blocks. The emulator circuit has an operating frequency upto 10KHz and finds application in the design of an adaptive low-pass filter.

Romero et al. [77] introduced a mutator-based grounded meminductor circuit utilizing Antoniou's gyrator circuit [78], shown in Figure 2.23.

As $i_{R_3} = i_{C_1}$, the value of meminductance can be obtained by calculating the current passing through resistor R_3 which can be expressed as the ratio of $v_{in}(t)$ and R_3

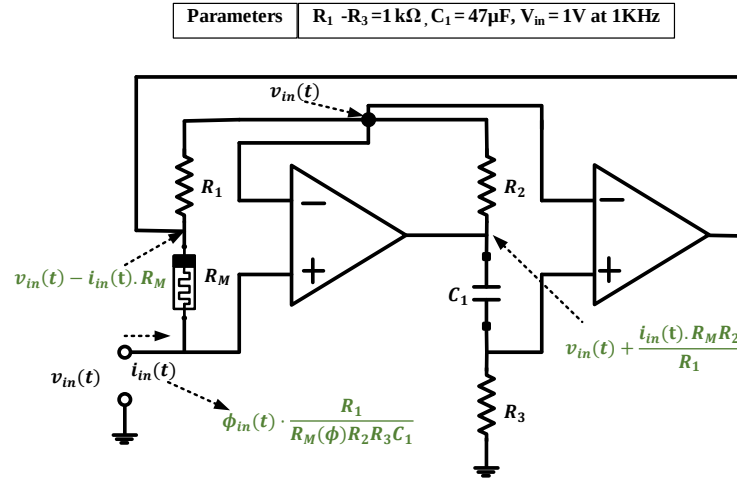


Figure 2. 23 Grounded meminductor emulator circuit based on gyrator designed upon Antoniou's circuit proposed by Romero et al. [77]

$$\frac{v_{in}(t)}{R_3} = \frac{C_1 R_M R_2}{R_1} \frac{d(i_{in}(t))}{dt} \rightarrow i_{in}(t) = \phi_{in}(t) \frac{R_1}{R_M(\phi) R_2 R_3 C_1} \quad 2.76$$

The aforementioned Equation 2.76 indicates that the circuit functions as a FCMI (flux controlled meminductor), whose meminductance is as

$$L_M(\phi) = \frac{R_M(\phi) R_2 R_3 C_1}{R_1} \quad 2.77$$

The proposed meminductor emulator circuit was simulated using a PSPICE simulator for frequencies up to 10KHz. This meminductor model was applied in an example of LTP- Long-Term Potentiation and LTD- Long-Term Depression [77] which replicates the long-term memory in biological circuits. However, this circuit can operate only in the grounded mode configuration.

Another meminductor emulator based on OTA is presented by Mustafa and Firat in Ref. [79]. The proposed meminductor emulator is electronically tunable. This meminductor emulator consists of two OTAs, an analog multiplier, two resistors, and two capacitors and is shown in Figure 2.24. The input current of the presented meminductor emulator circuit is given by

$$i_{in} = I_{C_1} + I_{R_1}, \quad V_{P1} = V_{P2} = V_p \quad 2.78$$

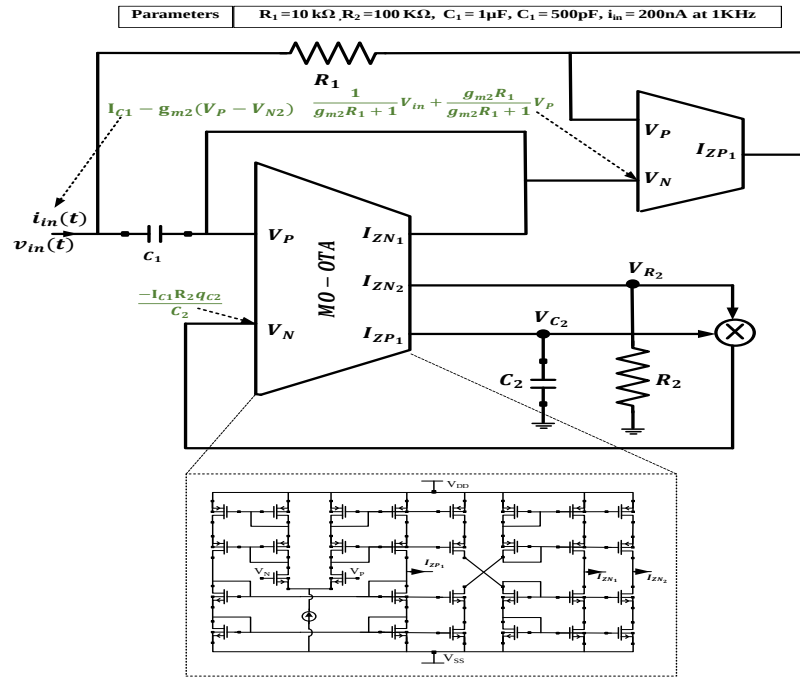


Figure 2. 24 Electronically tunable meminductor emulator presented by Mustafa and Firat [79]

The current flows in resistance R_1 is given by

$$I_{R1} = -I_{ZP1} = -g_{m2}(V_P - V_{N2}) = \frac{v_{in} - V_{N2}}{R_1} \quad 2.79$$

The voltage at the inverting terminal of second OTA, V_{N2} , is given by

$$V_{N2} = \frac{1}{g_{m2}R_1 + 1}v_{in} + \frac{g_{m2}R_1}{g_{m2}R_1 + 1}V_P \quad 2.80$$

The input voltage, V_{in} , of the emulator circuit becomes

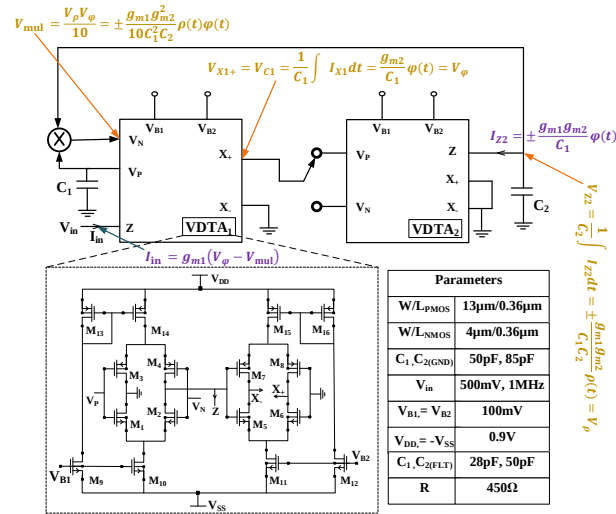
$$v_{in} = i_{in}(R_1 + \frac{1}{g_{m2}}) + I_{C1}(\frac{1}{g_{m1}} - \frac{1}{g_{m2}} - R_1 - R_2 \frac{q_{C2}}{C_2}) \quad 2.81$$

Integrating Equation 81, the flux in the circuit is given by

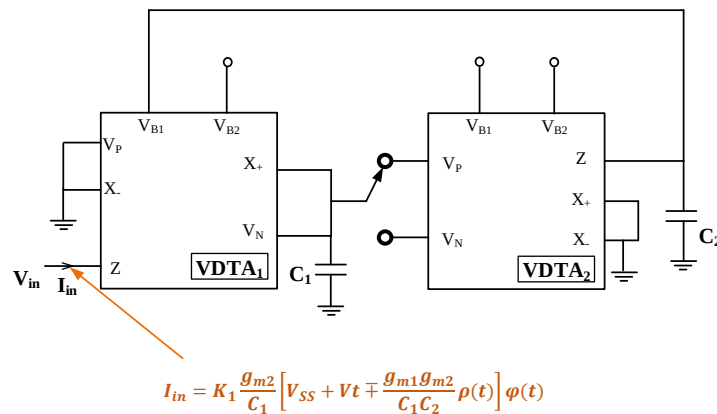
$$\phi(t) = \int v_{in} dt = (R_1 + \frac{1}{g_{m2}}) \int i_{in} dt + (\frac{1}{g_{m1}} - \frac{1}{g_{m2}} - R_1 - R_2 \frac{q_{C2}}{C_2}) \int I_{C1} dt \quad 2.82$$

The authors have verified the circuit by simulating it using LTSPICE tool with TSMC 0.18 μ m CMOS process parameter. The experimental verification of the emulator circuit has been done using the existing OTA IC OPA860. Since this emulator circuit is electronically tunable, the

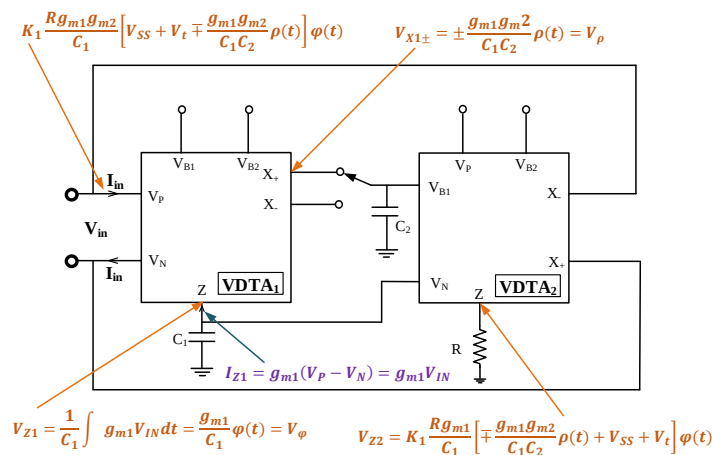
flux which is dependent on the transconductance of the OTAs can be adjusted by varying the biasing currents.



(a)



(b)



(c)

Figure 2. 25 (a) VDTA-based grounded meminductor emulator circuit (b) modified grounded Mode (c) floating mode [80]

Vista and Ranjan [80] have proposed a floating/grounded meminductor emulator using a voltage difference transconductance amplifier (VDTA) and a capacitor. The circuit of proposed meminductor emulator is presented in Figure 2.25. For the grounded configuration of the meminductor emulator, the voltage across the capacitor C_1 , V_{X1+} , and the corresponding current, I_{X1+} , are given by

$$V_{X1+} = V_{C1} = \frac{1}{C_1} \int I_{X1} dt = \frac{g_{m2}}{C_1} \varphi(t) = V_{\varphi} \quad 2.83$$

$$I_{X1+} = g_{m2} V_{in} \quad 2.84$$

The inverse meminductance of the grounded meminductor emulator is as

$$L_M^{-1} = \frac{g_{m1} g_{m2}}{C_1} \left[1 \mp \frac{g_{m1} g_{m2}}{10 C_1 C_2} \rho(t) \right] \quad 2.85$$

A multiplier block is used in the configuration of meminductor emulator. Authors have proposed another modified circuit to eliminate the multiplier block, and the modified grounded meminductor emulator circuit is shown in Figure 2.24. For the multiplication operation, the authors have used port characteristics of a VDTA. The meminductance of the modified approach of the grounded meminductor is given by

$$L_M^{-1} = K_1 \frac{g_{m2}}{C_1} \left[V_{SS} + V_t \mp \frac{g_{m1} g_{m2}}{C_1 C_2} \rho(t) \right] \quad 2.86$$

The floating meminductor circuit without using a multiplier block is also presented in this paper, and the equivalent inverse meminductance for floating meminductor is given by

$$L_M^{-1} = K_1 \frac{R g_{m1} g_{m2}}{C_1} \left[V_{SS} + V_t \mp \frac{g_{m1} g_{m2}}{C_1 C_2} \rho(t) \right] \quad 2.87$$

The authors have done the simulation using PSPICE software, and experimental verification has been done using the existing blocks. The authors have also used this proposed emulator circuit in neuromorphic circuits and verified the results through simulations. The operating frequency of the this circuit is up to 600KHz.

Aneet Singh and Rai [81] have presented an OP-AMP based meminductor emulator circuit, which consists of only a single OP-AMP, three resistors, one memristor, and two capacitors.

The proposed circuit is shown in Figure 2.26. The flux $\phi(t)$ in the proposed meminductor emulator circuit is given by

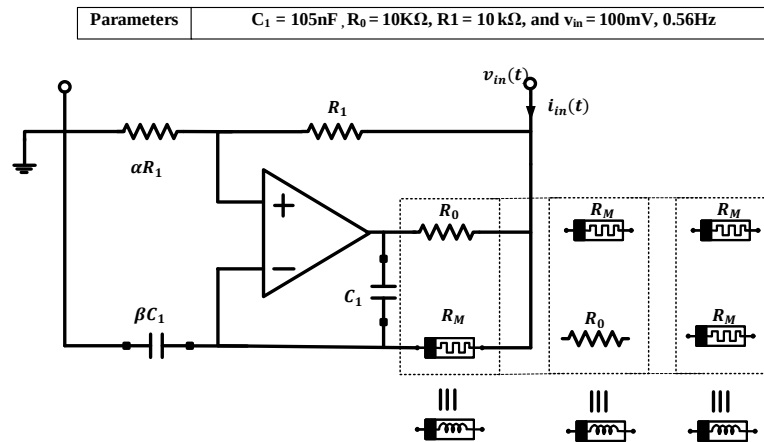


Figure 2. 26 Single OPAMP based meminductor emulator presented by Singh and Rai [81]

$$\phi(t) = \left[\frac{1}{(\alpha+1)} \left(\frac{1}{R} + \frac{(1-\alpha\beta)}{M_R} + \frac{1}{M_R} \right) + \frac{1}{sC(\alpha+1)M_R^2} \right]^{-1} \int I_{in} dt \quad 2.88$$

The nonlinear dopant drift model of the memristor is used for the implementation of the proposed meminductor emulator circuit. An application of a chaotic oscillator circuit has been presented in this work using the meminductor circuit, which verifies the various two-dimensional projection plots. The authors have simulated the proposed circuit using the LTspice tool and found satisfactory results over various frequencies up to 122 KHz.

Liang et al. [41] proposed a mutator based circuit utilizing CC-II blocks to emulate a floating flux-controlled meminductor emulator circuit. This emulator circuit is shown in Figure 2.27.

The current passing through the memristor is given by

$$i_{R_M}(t) = i_{R_2}(t) \quad 2.89$$

$$\frac{\phi_{in}(t)}{R_1 C_1 R_M} = \frac{i_{in}(t) R_3}{R_2} \quad 2.90$$

The equivalent meminductance of the circuit is given by

$$L_M(\phi) = \frac{R_2}{R_1 C_1 R_3 R_M(\phi)} \quad 2.91$$

The simulation of this circuit was done using the PSIPCE software and the circuit was experimentally validated using a sinusoidal input voltage at two different frequencies: 28.3 Hz and 36.9 Hz.

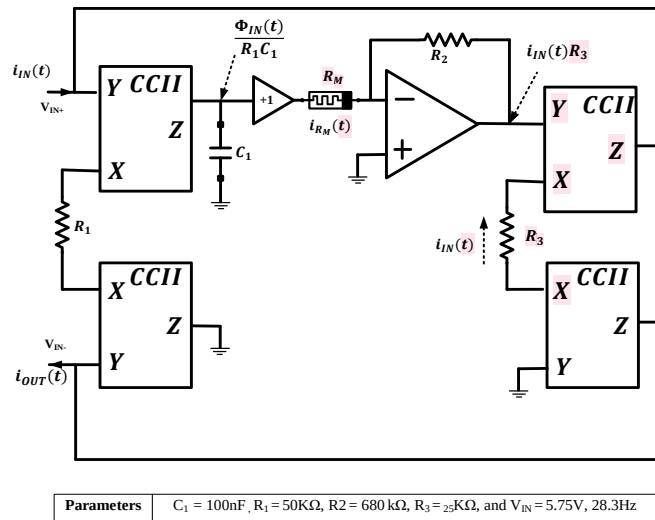


Figure 2. 27 CC-II based meminductor emulator circuit proposed by Liang et al. [41]

Most of the meminductor emulators relied on the use of either a memristor emulator or a memristor model for practical implementation. However, Fouda and Radwan [82] have presented a memristorless approach for meminductor emulator circuit. This emulator circuit is a purely grounded current-controlled meminductor. The circuit is shown in Figure 2.28.

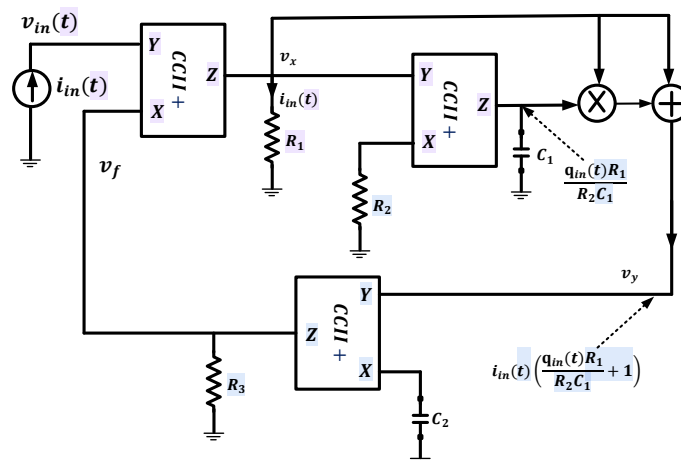


Figure 2. 28 Alternate approach of CC-II for meminductor emulator presented by Fouda and Radwan [82]

The design of this circuit is intended to satisfy the equation for CCMI (current-controlled meminductors), which is given by Equation 2.92.

$$\phi(t) = (L_0 + kq(t))i(t) \quad 2.92$$

Where k the mobility factor and L_0 is the initial inductance. Therefore, when considering $i_{R_3} = i_{C_2}$, the input flux is given by

$$\phi_{in}(t) = \left(R_1 R_3 C_2 + \frac{R_1^2 R_3 C_2}{C_1 R_2} q_{in}(t) \right) i_{in}(t) \quad 2.93$$

Through the comparison of the two equations 2.92 and 2.93, the current-controlled meminductance is expressed as shown in Equation 2.94.

$$L_M(q) = L_0 + kq_{in}(t) = R_1 R_3 C_2 + \frac{R_1^2 R_3 C_2}{C_1 R_2} q_{in}(t) \quad 2.94$$

The simulation of the presented circuit has been done through PSPICE software, and the operating frequency is up to 10 Hz. The experimental verification has been done using the existing integrated circuits.

Sah et al. [83] have also presented a CC-II-based meminductor emulator circuit which is shown in Figure 2.29. This mutator-based emulator circuit comprises five OP-AMPs, one CC-II, two current-controlled sources, ten resistors, two capacitors, and one multiplier block.

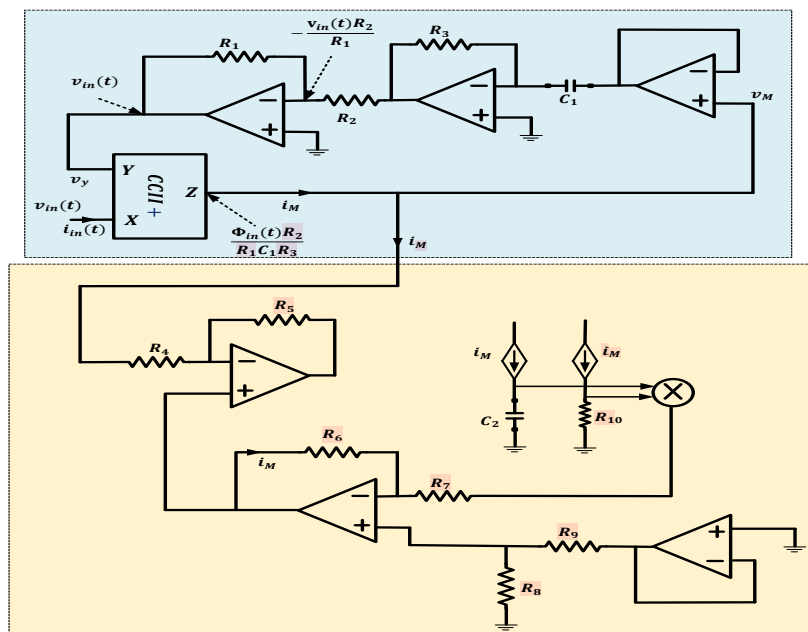


Figure 2. 29 Mutator based meminductor emulator circuit presented by Sah et al. [83]

Considering the current relationships $i_{C1} = i_{R1}$ and $i_{R2} = i_{R3}$ within this circuit facilitates the extraction of the constitutive equation for the equivalent flux-controlled meminductor.

The input current entering in the terminal X of CC-II is given by

$$i_{in}(t) = \phi_{in}(t) \frac{R_2}{C_1 R_1 R_3 R_M(\phi)} \quad 2.95$$

The resulting meminductance of the circuit is given by

$$L_M(\phi) = \frac{C_1 R_1 R_3 R_M(\phi)}{R_2} \quad 2.96$$

The simulations of the proposed circuit have been performed using PSPICE software and the experimental validation of the the simulated results has been done using the existing passive components and integrated circuits. The operating frequency of the circuit is up to 400Hz.

Finally, Table 2.3 comprises a brief comparison of the different meminductor emulators.

Table 2. 3 Comparison of existing meminductor emulators

Ref	Components Used	Mutator	Grounded/ Floating	Control Variable	Operating Frequency	Experimental
[75]	OPAMP-2, R-4, C-1	Yes	Grounded	Flux	Few Hz	No
[76]	OPAMP-3, Memristor-1	Yes	Grounded	Flux	10KHz	No
[77]	OPAMP-2, R-5, C-1	Yes	Floating	Flux	10KHz	Yes
[79]	OTA-2, Multiplier-1, R-2, C-2	No	Grounded	Flux	10KHz	Yes
[80]	VDTA-2, C-1	No	Grounded/ Floating	Flux	1MHz	Yes
[81]	OPAMP-1, R-3, C-2	Yes	Grounded	Flux	126KHz	Yes
[41]	CC-II-4, C-1, R_M -1, R-1	Yes	Floating	Flux	36.9Hz	No
[84]	CC-II+ - 1, OPAMP- 3, R-3, C-1	Yes	Grounded	Flux	400Hz	Yes
[82]	CC-II+ -3, R-3, C-2, Multiplier-1, Adder-1	No	Grounded	Current	10Hz	No

2.4. Literature on Universal Mem-Emulators

This section highlights noteworthy circuits found in the literature that have the capability to mimic any memelement with only minor adjustments to their structure or through the appropriate arrangement of their passive components. These circuit configurations are called the universal emulator interfaces.

Zhao, Wang, and Zhang [85] have proposed a universal emulator circuit shown in Figure 2.30. The memelement behavior depends on the configuration of the three ports Y_1 , Y_2 , and Y_3 as tabulated in Table 2.3. For the grounded mode of operation the switches S_1 and S_2 should be connected to the ground. The floating mode of operation is achieved when the switches S_1 and S_2 are connected to the Z and X terminal of the CC-II (U_5), respectively.

Before analyzing the mathematical model of different memelements, one must note the port characteristics of the CC-II which is given by

$$v_X = v_Y, i_Y = 0, i_Z = i_X \quad 2.97$$

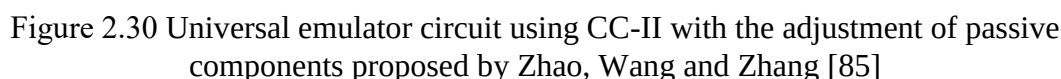
The mathematical representations of all the six memelement configurations are given as follows

Grounded Memristor:

$$v_{in}(t) = -\frac{R_0 R_2}{R_3} i_{in}(t) + \frac{R_0^2 R_2}{10 R_1 R_3 C_1} q(t) i_{in}(t) \quad 2.98$$

Table 2. 4 Passive component configuration for memelement emulator proposed by Zhao et al. [85]

Memelement	Configuration	Y_1	Y_2	Y_3
Memristor	Grounded	R_0	R_3	
Memristor	Floating	R_0	R_3	R_5
Memcapacitor	Grounded	C_0	R_3	
Memcapacitor	Floating	C_0	R_3	R_5
Meminductor	Grounded	R_0	C_0	
Meminductor	Floating	R_0	C_0	C_2


$$v_{\text{in}}(t) = V_+ - V_- = \left(\frac{R_0 R_4}{R_5} - \frac{R_0 R_2}{R_3} \right) i_{\text{in}}(t) + \frac{R_0^2 R_2}{10 R_1 R_3 C_1} q(t) i_{\text{in}}(t) \quad 2.99$$
$$v_{\text{in}}(t) = -\frac{R_2}{R_3 C_0} q(t) + \frac{R_2}{10 R_1 R_3 C_1 C_0} \sigma(t) q(t) \quad 2.100$$
$$v_{\text{in}}(t) = \left(\frac{R_4}{R_5 C_0} - \frac{R_2}{R_3 C_0} \right) q(t) + \frac{R_2}{10 R_1 R_3 C_1 C_0} \sigma(t) q(t) \quad 2.101$$
$$\varphi(t) = -R_0 R_2 C_0 i_{\text{in}}(t) + \frac{R_0^2 R_2 C_0}{10 R_1 C_1} q(t) i_{\text{in}}(t) \quad 2.102$$
$$\varphi(t) = (R_0 R_4 C_2 - R_0 R_2 C_0) i_{\text{in}}(t) + \frac{R_0^2 R_2 C_0}{10 R_1 C_1} q(t) i_{\text{in}}(t) \quad 2.103$$

75

A universal interface for constructing memelements was proposed by Ciyan et al. [86]. This paper focuses on a universal interface with some additional peripheral circuits for the implementation of memelements emulator as shown in Figure 2.31. The universal interface circuit consists of four CFOA, two resistors, and one capacitor. The peripheral circuits consist of some passive and active components. A varactor diode was used in peripheral circuits to obtain a variable capacitance. Authors have connected the terminals $T_1 - T_4$ of the peripheral circuits (shown in Green color boxes) with the universal interface circuit (shown in Blue color box) to obtain respective memelement operations.

The memristor operation is defined by $q - \phi$ relationship as shown in Equation 2.104

$$q(\phi) = \frac{1}{3}\alpha_1\phi^3 + \frac{1}{2}\beta_1\phi^2 + \gamma_1\phi \quad 2.104$$

and the memductance (inverse of memristance) $W(\phi)$ is given by Equation 2.105

$$W(\phi) = \frac{dq(\phi)}{d\phi} = \alpha_1\phi^2 + \beta_1\phi + \gamma_1 \quad 2.105$$

The memcapacitor operation is defined by the $\sigma - \phi$ relationship as shown in Equation 2.106

$$\sigma(\phi) = \alpha_2\phi^3 + \beta_2\phi^2 + \gamma_2\phi \quad 2.106$$

and the memcapacitance is given by Equation 2.107

$$C_m(\phi) = \frac{d\sigma(\phi)}{d\phi} = \alpha_2\phi^2 + \beta_2\phi + \gamma_2 \quad 2.107$$

Similarly, the meminductor operation is defined by the $q - \rho$ relationship as shown in Equation 2.108

$$q(\rho) = \frac{1}{3}\alpha_3\rho^3 + \frac{1}{2}\beta_3\rho^2 + \gamma_3\rho \quad 2.108$$

and the inverse value of the meminductance L_m^{-1} is given by Equation 2.109

$$L_{AB}^{-1}(\rho) = \frac{dq(\rho)}{d\rho} = \alpha_3\rho^2 + \beta_3\rho + \gamma_3 \quad 2.109$$

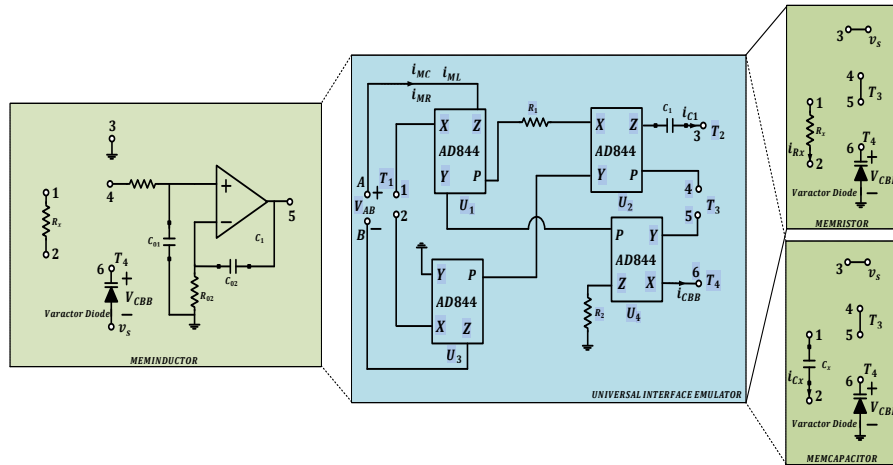


Figure 2.31 Universal emulator interface for building memelements using varactor diode proposed by Cian et. al. [86]

The coefficients $\alpha_1, \beta_1, \gamma_1, \alpha_2, \beta_2, \gamma_2, \alpha_3, \beta_3$, and γ_3 are defined as shown in Equations (2.110-2.112)

$$\alpha_1 = \frac{a_2 R_2}{R_x R_1^3 C_1^3}, \quad \beta_1 = -\frac{R_2(a_1 + 2a_2 v_s)}{R_x R_1^2 C_1^2}, \quad \gamma_1 = \frac{R_2(a_0 + a_1 v_s + a_2 v_s^2)}{R_x R_1 C_1} \quad 2.110$$

$$\alpha_2 = \frac{a_2 R_2 C_x}{R_1^3 C_1^3}, \quad \beta_2 = -\frac{R_2 C_x(a_1 + 2a_2 v_s)}{R_1^2 C_1^2}, \quad \gamma_2 = \frac{R_2 C_x(a_0 + a_1 v_s + a_2 v_s^2)}{R_1 C_1} \quad 2.111$$

$$\alpha_3 = \frac{a_2 R_2}{R_x R_{01}^3 R_1^3 C_{01}^3 C_1^3}, \quad \beta_3 = \frac{R_2(-a_1 + 2a_2 v_s)}{R_x R_{01}^2 R_1^2 C_{01}^2 C_1^2}, \quad \gamma_3 = \frac{R_2(a_0 - a_1 v_s + a_2 v_s^2)}{R_x R_{01} R_1 C_{01} C_1} \quad 2.112$$

All the configurations are operating in the floating mode upto 180KHz frequency. This universal emulator circuit offers advantages such as floating terminals, the ability to reconfigure among these three types of mem-elements, a simple circuit design, less area and power consumption, and the ability to operate at high frequencies.

Dongsheng et al. [87] proposed a universal emulator circuit using a varactor diode, shown in Figure 2.32. A floating mutator circuit is transformed into all three memelements by making use of a varactor diode, a resistor, and a capacitor.

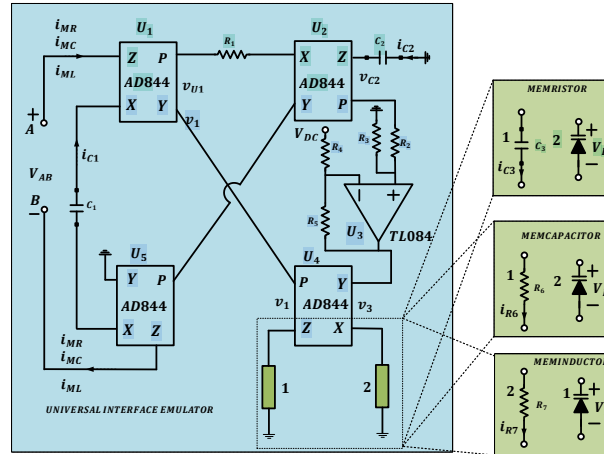


Figure 2. 32 The mutator schematic and additional circuitry to construct memristor, memcapacitor and meminductor with minor addition using varactor diode proposed by Dongsheng Yu et al. [87]

Since the varactor diode has a significant role in constructing memelement emulator circuits because of its tunable characteristics.

The capacitance (C_{vd}) of the varactor diode depends on applied reverse voltage (v) as shown in Equation 2.113

$$C_{vd} = C_{vd0} \left(1 + \frac{v}{V_d}\right)^{-\gamma} \quad 2.113$$

The elements given in the green-colored blocks as shown in Figure 2.32, should be configured properly as tabulated in Table 5 for the implementation of the memristor, memcapacitor, and meminductor. The guiding equations for the respective memelement emulators are given by

Memristor:

$$W(\phi) = \frac{\alpha C_1}{R_1 C_2 C_3} (a_0 + a_1 v_3 + a_2 v_3^2), v_3 = \alpha \frac{\phi_{AB}}{R_1 C_2} - \beta V_{DC} \quad 2.114$$

Memcapactor:

$$C(\phi) = \frac{\alpha R_6 C_1}{R_1 C_2} (a_0 + a_1 v_2 + a_2 v_2^2), v_2 = \alpha \frac{\phi_{AB}}{R_1 C_2} - \beta V_{DC} \quad 2.115$$

Meminductor:

$$L(q) = \frac{R_1 R_7 C_2}{\alpha C_1} (a_0 + a_1 v_1 + a_2 v_1^2), v_1 = \alpha \frac{q_{AB}}{C_1}, V_{DC} = 0 \quad 2.116$$

Table 2. 5 Connecting configuration for MR, MC, and MI proposed by Dongsheng et al. [87]

Mem-Element	Component in Block 1	Component in Block 2
Memristor	Capacitor (C_3)	Varactor Diode (v_d)
Memcapacitor	Resistance (R_6)	Varactor Diode (v_d)
Meminductor	Varactor Diode (v_d)	Resistance (R_7)

The simulation of the proposed emulator circuit has been done using PSPICE software, and the results have been verified by hardware implementation using the existing devices and discrete components. The operating frequency of the this circuit is up to 22 KHz.

Yue et al. [88] proposed charge-controlled grounded and floating memelement emulators with the connection combination of three switches ($S_1 - S_3$) and preserved positions ($P_1 - P_3$). The proposed emulator circuit is configured by several existing components such as seven resistors, a capacitor, three CC-II, a multiplier block, three preserved ports, and three switches as shown in Figure 2.33. The combinations of persevered ports and switches decide the behavior of the circuit, and are tabulated in Table 2.6.

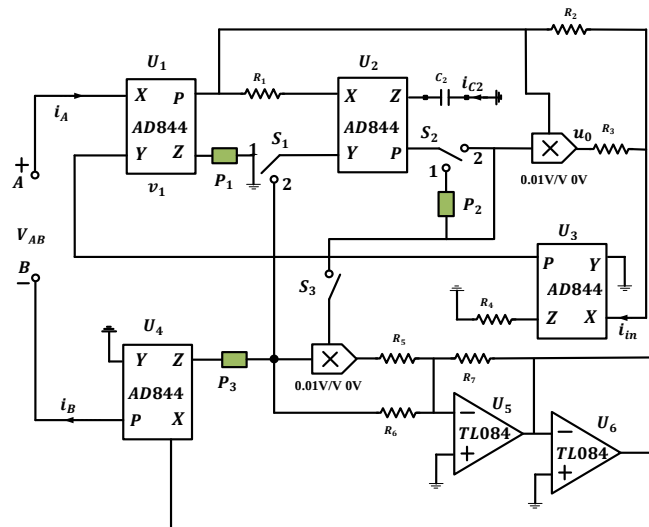


Figure 2.33 Schematic diagram for memory emulator with the adjustment of passive components proposed by Yue Liu et al. [88]

Table 2. 6 The memelement configurations with the combination of preserved ports and switches proposed by Yeu et al. [88]

Type	Grounded			Floating		
	MR	MC	MI	MR	MC	MI
S_1	1	1	1	2	2	2
S_2	2	2	P_2	2	2	P_2
S_3	Off	Off	Off	On	On	On
P_1	R_x	C_x	R_x	R	C	R
P_2	-	-	Integrator	-	-	Integrator
P_3	-	-	-	R_x	C_x	R_x

The mathematical model for the proposed memelements as per the combination tabulated in Table 2.5 as follows:

The grounded memristor:

$$R_M = \frac{v_A}{i_A} = -\frac{R_x^2 R_4}{10R_1 C_1 R_3} q_A + \frac{R_x R_4}{R_2} \quad 2.117$$

The grounded memcapacitor:

$$C_M^{-1} = \frac{v_A}{q_A} = \frac{R_4}{10R_1 C_1 C_x^2 R_3} \sigma_A + \frac{R_4}{C_x R_2} \quad 2.118$$

The grounded meminductance:

$$L_M = \frac{\varphi_A}{i_A} = \frac{R_x^2 C_2 R_4 R_8}{10R_1 C_1 R_3} q_{AB} + \frac{R_x R_4}{R_2} \quad 2.119$$

The floating memristor:

$$R_M = \frac{v_{AB}}{i_{AB}} = -\frac{R_x^2}{10R_1 C_1} \left(\frac{R_4}{R_3} + \frac{R_7}{R_5} \right) q_{AB} + R_x \left(\frac{R_4}{R_2} - \frac{R_7}{R_6} \right) \quad 2.120$$

The floating memcapacitor:

$$C_M^{-1} = \frac{v_{AB}}{q_{AB}} = \frac{1}{10R_1 C_1 C_x^2} \left(\frac{R_4}{R_3} - \frac{R_7}{R_5} \right) \sigma_{AB} + \frac{1}{C_x} \left(\frac{R_4}{R_2} - \frac{R_7}{R_6} \right) \quad 2.121$$

The floating memrinductor:

$$L_M = \frac{\varphi_{AB}}{i_{AB}} = \frac{R_x^2 C_2}{10R_1 C_1} \left(\frac{R_4 R_8}{R_3} - \frac{R_7}{R_5} \right) q_{AB} + R_x \left(\frac{R_4}{R_2} - \frac{R_7}{R_6} \right) \quad 2.122$$

The authors have verified the simulated results by performing experiments using the existing devices and discrete components for both floating and grounded memelement emulator

configurations. An interesting aspect of this proposed circuit is the widest bandwidth and the highest operating frequency upto 1.5MHz.

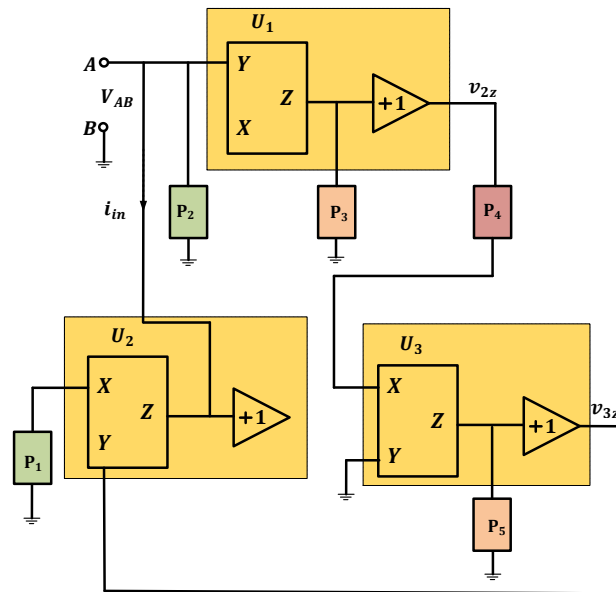


Figure 2. 34 Universal mutator circuit for all three memelement configurations proposed by Dongsheng et al. [89]

A universal mutator circuit was proposed by Dongsheng et al. [89], consisting of three CCII, three OPAMPs, and five preserved ports for passive components. The circuit is shown in Figure 2.34. The highlight of the work lies in the fact that one memelement can be transformed into another memelement as specified in Table 2.7 and 2.8.

Table 2. 7 Combination Case-1 for transforming memconductance proposed by Dongsheng et al. [89]

Uni-directional Transformation	Connection Combinations					Memconductance
	P_1	P_2	P_3	P_4	P_5	
MR $\rightarrow$ MC	C_1	R_2	R_3	G_m	R_5	$C_m = \frac{G_m C_1 R_3 R_5}{R_2}$
MC $\rightarrow$ MR	R_1	R_2	R_3	C_m	C_5	$G_m = \frac{C_m R_3}{R_1 R_2 C_5}$
MC $\rightarrow$ MI	R_1	R_2	C_3	C_m	C_5	$F_m = \frac{C_m}{R_1 R_2 C_3 C_5}$
MI $\rightarrow$ MC	C_1	C_2	R_3	F_m	R_5	$C_m = F_m C_1 C_2 R_3 R_5$
MR $\rightarrow$ MI	R_1	R_2	C_3	G_m	R_5	$F_m = \frac{G_m R_5}{R_1 R_2 C_3}$
MI $\rightarrow$ MR	R_1	C_2	R_3	F_m	R_5	$G_m = \frac{F_m C_2 R_3 R_5}{R_1}$

Table 2. 8 Combination Case-2 for transforming memconductance proposed by Dongsheng et al. [89]

Bi-directional Transformation	Connection Combinations					Memconductance
	P_1	P_2	P_3	P_4	P_5	
MR $\leftrightarrow$ MC	C_1	R_2	G_m	R_4	R_5	$C_m = \frac{C_1 R_5}{R_2 R_4 G_m}$
MC $\leftrightarrow$ MR	R_1	C_2	C_m	R_4	R_5	$G_m = \frac{C_2 R_5}{R_1 R_4 C_m}$
MC $\leftrightarrow$ MI	R_1	R_2	C_m	C_4	C_5	$F_m = \frac{C_4}{R_1 R_2 C_m C_5}$
MI $\leftrightarrow$ MC	R_1	R_2	F_m	C_4	C_5	$C_m = \frac{C_4}{R_1 R_2 F_m C_5}$
MR $\leftrightarrow$ MI	R_1	R_2	G_m	R_4	C_5	$F_m = \frac{1}{R_1 R_2 R_4 C_5 G_m}$
MI $\leftrightarrow$ MR	R_1	R_2	F_m	R_3	R_5	$G_m = \frac{1}{R_1 R_2 R_4 C_5 F_m}$

By connecting memory elements to positions P_1 , P_2 , and P_4 , it is possible to achieve eighteen transformations among memristor (MR), memcapacitor (MC) and meminductor (MI), and by connecting memory elements to position P_3 and P_5 , it is possible to achieve twelve bidirectional transformations among MR, MC, and MI.

The universal emulator circuit has the advantage that all six types of transformation can be achieved using only three OTAs, at most three resistors, and two capacitors. The operating frequency is up to a few Hz, which is suitable for low-frequency applications.

The Table 9 presents a constructive description of the prime features of the universal emulator circuits.

Table 2.9 Comparison of different universal memelement emulators

Ref.	Emulator	Mutator	Configuration	Control Variable	Components Used	Experimental	Operating Frequency
[85]	Memristor	No	Grounded/	Charge	AD844 - 05	Yes	5KHz
	Memcapacitor		Floating	Charge	OPAMP-01,		
	Meminductor			Charge	Passive Components		
[86]	Memristor	No	Floating	Flix	AD844 - 04,	Yes	180KHz
	Memcapacitor			Flux	OPAMP-01, Varactor Diode,		
	Meminductor			Charge	Passive		

					Components		
[87]	Memristor	No	Floating	Flux	AD844 - 04,	Yes	22KHz
	Memcapacitor			Flux	OPAMP-01, Varactor Diode,		
	Meminductor			Charge	Passive Components		
[88]	Memristor	No	Grounded/ Floating	Charge	AD844 - 04,	Yes	550KHz, 360KHz,
	Memcapacitor			Charge	OPAMP-02, Multipliers-02,		960KHz (Ground), 560KHz,
	Meminductor			Charge	Passive Components		240KHz, 1.5MHz (Floating)
[89]	Memristor	Yes	Grounded	Flux	AD844 - 03,	Yes	Few Hz
	Memcapacitor			Flux	Memristor-01, Multipliers-01,		
	Meminductor			Flux	Passive Components		

2.5. Literature Summary

This Literature provides an in-depth review of techniques proposed in the literature for emulating memristors, memcapacitors, meminductors, and universal emulators. The selected circuits used for emulation have been analyzed theoretically to determine their equivalent memristance, memcapacitance, and meminductance with their constitutive equations. The memristor emulators are based on only MOSFETs whereas most of the memcapacitor and meminductor emulators presented in the literature are based on mutator circuits, however, there are some emulator models that are not based on mutator circuits. For example, work in [84, 83] in centred around using a resistor, a capacitor and a varactor diode. Table 0, Table 1, Table 2, and Table 8 have been compiled to summarize the main features of the reviewed memelement emulators, offering a comprehensive overview of technological options. Even though the options for memelement design are quite extensive, this review paper has selected only a few specific examples. The memristor emulators are only MOSFET based since this technology offers less area and power consumption, higher operating frequency, and lower complexity. The memcapacitor and meminductor emulators are mostly mutator based since they are easy to implement, and have a simple mathematical modeling and analysis. Such examples also

exemplify the fact that the research in the direction of implementing memcapacitors and meminductors using only MOSFETs is still in its infancy. The work attempts to spur research in that direction.

2.6. Research Gaps

Based on the exhaustive evaluation of the literature presented in this thesis, many significant research gaps have been discovered that serve as the foundation for the issue statements addressed in this work:

- 1. Performance parameters of memristor emulators such as complexity, operating frequency range, and power consumption need improvement-** Despite considerable advancements in memristor emulator design, their performance parameters still require significant improvement. Many existing circuits suffer from high design complexity, involving a large number of active and passive components that increase chip area and reduce integration feasibility with modern CMOS processes. Moreover, their operating frequency range often remains limited to the kHz or low MHz domain, whereas practical applications in high-speed communication and RF systems demand operation in the tens or hundreds of MHz. Power consumption also poses a challenge, as continuous biasing and multiple transistor arrangements result in higher static and dynamic power usage, restricting their adoption in low-power and energy-efficient systems. Addressing these limitations is essential to enhance the scalability, simplicity, and efficiency of future memristor emulator designs..
- 2. Only MOSFET based designs for memcapacitor and meminductor emulators are yet to be reported-** While MOSFET-based memristor emulators are extensively reported in literature, similar efforts for memcapacitor and meminductor emulators remain limited. Most memcapacitor and meminductor emulators rely on passive RLC networks or active op-amp/gyrator structures, which, although functional, are not always compatible with nanoscale CMOS technologies. A pure MOSFET-based implementation of these devices could enable compact, fully integrable, and tunable designs with reduced area and power consumption, thereby making them more suitable for system-on-chip (SoC) applications. However, such designs have not yet been widely explored or optimized, leaving a clear research gap in developing efficient MOSFET-only memcapacitor and meminductor emulator circuits.

3. There exists limited applications of mem-devices emulators in nonlinear circuits-

Although memristor, memcapacitor, and meminductor emulators have been successfully designed and validated through I–V hysteresis loops and basic testing, their applications in nonlinear circuits remain unexplored. A few studies have demonstrated their utility in oscillators, such as Chua’s circuit, and in chaos-based systems, but broader applications in adaptive learning, neuromorphic architectures, and nonlinear analog circuits are still underexplored. Expanding their integration into nonlinear systems such as frequency multipliers, nonlinear controllers, secure communication circuits, and large-scale neuromorphic processors could unlock their full potential. Exploring these areas would not only validate emulator models further but also pave the way for practical real-world implementations of mem-devices.

2.7. Research Objectives

Based on the preceding discussion and detailed analysis undertaken throughout this thesis, the following important research objectives were successfully achieved:

Research Objective 1: To design efficient memristor, memcapacitor, and meminductor Emulator.

One of the key objectives of this study was to create small, high-performance emulator circuits that mimicked the behavior of memristors, memcapacitors, and meminductors. This goal entailed developing hardware-efficient designs with few active and passive components, with a special emphasis on MOSFET-only implementations to improve CMOS compatibility. The suggested emulator circuits were designed to precisely simulate the dynamic features of their solid-state equivalents while being simple, cheap in power consumption, and adaptable to modern analog and digital systems.

Research Objective 2: To examine the performance of memelements in analog circuits.

Another important goal was to evaluate the usefulness and effectiveness of the developed memelements in analog electronic systems. This entailed incorporating the designed memristor, memcapacitor, and meminductor emulators into a variety of analog circuit designs including filters, oscillators, and nonlinear dynamic systems. Detailed simulations and studies were conducted to determine their impact on signal behavior, frequency responsiveness, and overall circuit performance. The findings proved the practical benefits of these emulators in

improving the functionality of analog circuits, particularly in terms of tunability, nonlinearity, and memory-based dynamics.

Research Objective 3: To design and evaluate the performance of memelements in digital circuits.

The third goal was the introduction of memristive behavior into digital circuits. This study investigated the integration of memelements into combinational and sequential logic circuits in order to evaluate their performance in digital computing settings. The purpose was to investigate how memory-enabled components could affect logic operations, reduce circuit complexity, and increase energy efficiency. This study shows through simulation and design verification that memelements hold great promise for developing digital circuit architectures, particularly for next-generation low-power computing and memory systems.

In conclusion, this thesis has achieved its primary goals by introducing unique memelement designs and demonstrating their applicability and effectiveness in both analog and digital domains, thereby making significant contributions to the field of mem-device-based circuit design.

Chapter 3

Design of Efficient Memristor Emulators

This chapter explained the design of efficient memristor emulators which having few number of MOSFETs and its application in different analog and digital applications. In this chapter three memristor design are discussed in which one memristor emulator circuit having only single MOSFET, second memristor having only three MOSFETs with a MOSCAP, and third memristor having only six MOSFETs with one capacitor. The fingerprints of all the memristors have been verified using Cadence Virtuoso Spectre tool under 45nm, 90nm, and 180nm GPDK technology. The applicability of the memristor emulators also discussed in this chapter.

3.1 A Compact Memristor Emulator Circuit

2 A high-frequency, single-MOSFET-based memristor emulator architecture is presented, which includes a first-order RC filter and can operate in both floating and grounded modes. This emulator is fundamentally passive, consuming no static power and producing only a few picowatts of dynamic power under signal excitation. The emulator was designed and simulated in the Cadence Virtuoso Spectre environment, and mathematical modeling supports its incremental behavior and memristive properties. The layout requires only $1.586 \mu\text{m}^2$ and can operate at frequencies up to 80 MHz. A crucial feature of this study is the emulator's practical validation with discrete components, specifically the ALD1117 dual P-channel enhancement-mode MOSFET and an external RC network. The circuit performs admirably in both the analog and digital domains, and it stands out from other emulator designs due to its compact structure and extremely low power consumption.

3.1.1 Introduction

The memristor, invented by Leon Chua in the early 1970s [4], [5], is currently regarded as a fundamental circuit element alongside the resistor, capacitor, and inductor. Because of its simple structure, compact size, energy efficiency, and intrinsic data retention capability, the memristor has sparked widespread interest in its usage in current electronic circuit design. Its non-volatile nature makes it very useful in analog and digital applications. As the fourth basic passive element [6], memristors have been successfully used in a variety of applications,

including programmable analog systems [16], neuromorphic circuits [90], [91], chaotic oscillators [27], non-volatile storage [29], asymmetric attractors [60], XOR logic implementations [61], and the classic Chua's circuit [92], [93], [94].

Despite its potential, the complexity and high cost of manufacturing memristors have limited their practical use in real-time applications. To address this, researchers created memristor emulators—circuits that mimic the behavior of physical memristors. Adhikari et al. [46] developed emulators with important memristive properties, such as frequency-dependent hysteresis loops. Various implementations have leveraged active components like operational transconductance amplifiers (OTAs) [95][54][96], operational amplifiers (OPAMPs) [97][98] [99], current feedback op-amps (CFOAs) [100][101], second-generation current conveyors (CCII) [102][103], differential-difference current conveyors (DDCC) [104], current conveyor transconductance amplifiers (CCTA) [105], differential voltage current conveyor transconductance amplifiers (DVCCTA) [106], voltage differencing. While these techniques successfully simulate memristive features, they frequently result in increased circuit complexity and power consumption.

To address these restrictions, another line of research focuses on building memristor emulators with only MOSFETs and few passive components. This design concept supports high-frequency operation, simpler circuitry, and reduced power consumption. Vista and Ranjan's floating memristor emulator [47] is notable for its ability to function at up to 13 MHz using three NMOS transistors, a capacitor, and a DC current source. Similarly, John et al. [107] suggested a fully passive emulator employing BJTs, diodes, resistors, and capacitors that did not require external biasing, although it had non-ideal hysteresis characteristics. E. Gale [108] advanced memristor theory by developing new models and investigating a variety of non-ideal behaviors, including filament-based mechanisms.

Other notable works include Koymenn and Emmanuel's weak inversion CMOS design with log-domain transconductors and a grounded capacitor [109], Babacan et al.'s compact four-MOS memristor emulator with 100 MHz operation and a ZnO thin-film device [49], and a bias-free three-MOS transistor design operating at 100 kHz [110]. Additional designs by Abdulla [50] and Vishal [111] introduced modifications employing 7-transistor topologies, some with zero-threshold devices and DC sources for memcomputing. SPICE-based behavioral models have also been described in publications such as [48][112][113].

Pushkar et al. [114][52] demonstrated dynamic threshold-based MOSFET emulators that did not require passive components or external biasing, whereas recent designs using four-MOS architectures [115][116][117][118] investigated the balance between power efficiency and operating bandwidth. Minimalist MOSFET-based emulators, such as those described in [119][120][121], have also appeared, while hurdles remain in terms of layout efficiency and overall performance.

Researchers have also investigated passive memristor emulators that do not use MOSFETs at all, instead relying on rectifier circuits and first-order filters such as RC [57], RL [122], LCR [123], and three-phase bridges [124].

In this paper, we provide a new voltage-controlled grounded memristor emulator with floating-mode operation. The design uses a single MOSFET coupled to a simple RC network, which eliminates the requirement for external DC biasing. It has zero static power dissipation and low dynamic power usage (~ 7.75 pW), supporting frequencies up to 80 MHz. Analytical modeling, circuit simulations using Cadence Virtuoso with Generic Process Design Kit, and hardware realization with ALD1117 PMOS transistors are used to verify the emulator's operation. The experimental results show memristive hysteresis behavior over a wide frequency range.

The proposed design has several major benefits:

- A minimalist architecture using a single MOSFET and an RC network.
- In comparison to prior emulator designs, the layout area has been reduced.
- The structure is simple and suited for integration into bigger systems.
- Bias-free operation in power-constrained applications.

Table 3.2 provides a full comparison of other cutting-edge emulators. The remainder of this chapter is organized as follows:

Section 3.1.2 describes the theoretical modeling of the presented emulator. Section 3.1.3 discusses the experimental and simulation results. Section 3.1.4 shows applications such as a Schmitt trigger, chaotic oscillator, and XOR logic. Section 3.1.5 summarizes the benefits and potential implications of the proposed memristor architecture.

3.1.2 Design and Theory of Proposed Memristor Emulator

The suggested memristor emulator is based on a basic but effective circuit arrangement that contains a diode-connected transistor (serving as a voltage-controlled resistor) linked in series with a parallel RC filter which is first-order, as shown in Figure 3.1.

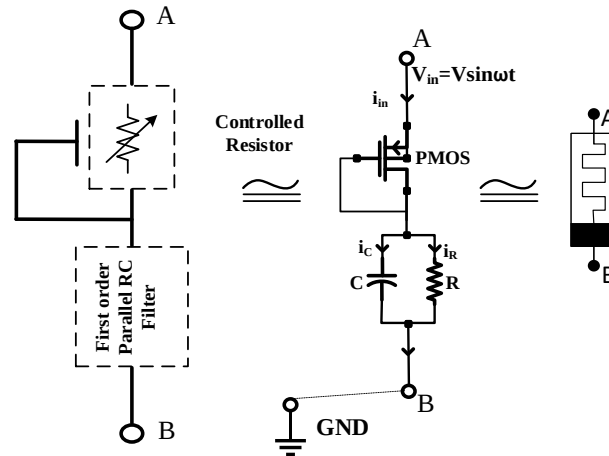


Figure 3. 1 Topology of memristor emulator consists of single MOSFET with RC filter

In small-signal operation, the diode-connected transistor acts similarly to a two-terminal resistive element, especially when the gate and drain are linked together. The impedance of this setup is about $1/g_m || r_o$, where g_m is the transconductance and r_o is the output resistance. The overall impedance might be approximated as $1/g_m$ when r_o is generally high [1].

In this design, a PMOS transistor is used to implement the diode-connected load. Shortening the gate and drain terminals equalizes the gate-to-source and drain-to-source voltages, resulting in $v_{gs} = v_{ds} = v_c - v_{in}$. This ensures that the PMOS runs consistently in the saturation area by satisfying the criteria $v_{ds} > v_{gs} - v_{tp}$. As a result, the drain current I_D can be calculated accordingly.

$$I_D = -\mu_p C_{ox} \left(\frac{W}{2L} \right) (v_{gs} - v_{tp})^2 \quad 3.1$$

The expression incorporates parameters such as hole mobility (μ_p), oxide capacitance (C_{ox}), the device aspect ratio (W/L), the gate–source voltage (v_{gs}), and the threshold voltage (v_{tp}). In this circuit, the input current (i_{in}) corresponds to the drain current and can be written as the product of the transconductance (g_m) and the input voltage (v_{in}).

$$i_{in} = I_D = g_m(v_c, v_{in}) \times v_{in} \quad 3.2$$

The conductance (g_m) depends on the capacitor voltage (v_C) and the input voltage (v_{in}). Kirchhoff's current law states that $I_D = i_C + I_R$, where I_R and i_C represent currents flowing across resistors and capacitors, respectively. One can write,

$$i_C = I_D - I_R \quad 3.3$$

$$C \frac{dv_C}{dt} = f(v_C, v_{in}) = k \times (v_{gs} - v_{tp})^2 - \frac{v_C}{R} \quad 3.4$$

where $k = -\mu_p C_{ox} W/2L$ and f is a function which depends on capacitor and input voltages. Now,

$$\frac{dv_C}{dt} = \frac{k(v_{gs} - v_{tp})^2}{C} - \frac{v_C}{RC} \quad 3.5$$

$$\frac{dv_C}{dt} = \frac{k(v_C - v_{in} - v_{tp})^2}{C} - \frac{v_C}{RC} \quad 3.6$$

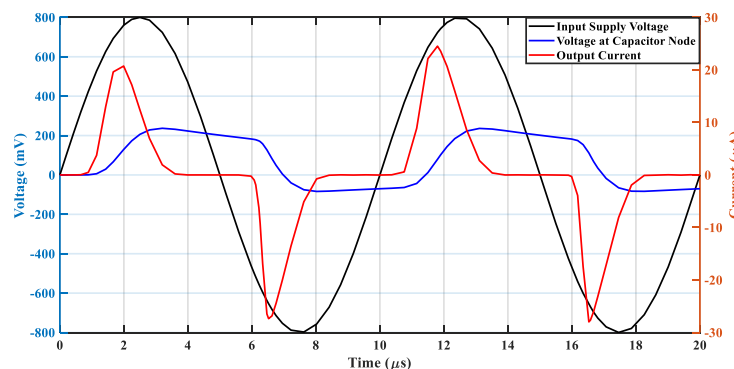
Our mathematical model of the memristor emulator is based on Equations (3.2) and (3.6). These equations are similar to those in [57][58], which consider diodes instead of MOSFETs in the circuit. The overall impedance of the circuit is determined in Equations (3.7-3.9).

$$M_R = \frac{V_{in}}{I_{in}} = \frac{1}{g_m} + \frac{1}{\frac{1}{X_C} + \frac{1}{R}} \quad 3.7$$

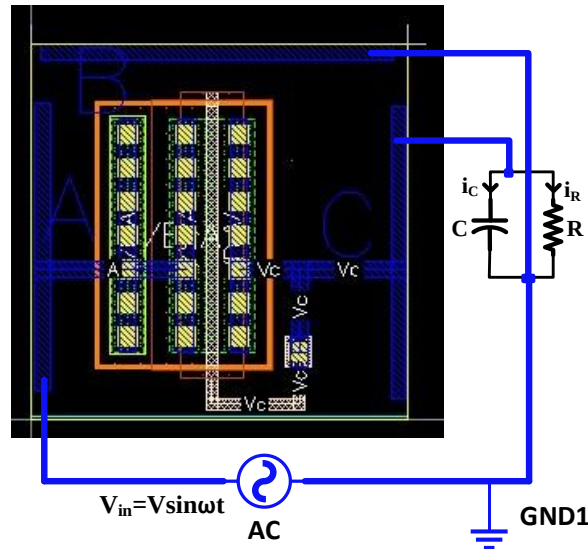
where $g_m = k.(v_{gs} - v_{tp})$, $X_C = 1/sC$ and $s = j\omega$.

$$M_R = \frac{1}{g_m} + \frac{R}{1+sRC} \quad 3.8$$

$$M_R = \frac{1}{k(v_C - v_{in} - v_{tp})} + \frac{R}{1+sRC} \quad 3.9$$



(a)



(b)

Figure 3. 2 (a) Transient behaviour (current, voltage, and capacitor voltage waveform) of the single MOS memristor emulator (b) CMOS layout circuit for single MOS memristor emulator circuit

Figure 3.2 (a) shows how the suggested circuit works for one time period, which is $T = 10\mu s$. Think about a capacitor with capacitance C that is fully discharged at $t = 0$. As long as the source to gate voltage, $v_{sg} \approx (v_{in} - v_c) < v_{tp}$, the capacitor will stay entirely discharged. The PMOS will also stay OFF until $|v_{sg}| < v_{tp}$. Because of this, the current I_D will be 0. Now, when the voltage v_{sg} is greater than the threshold voltage v_{tp} for the time interval $0 \leq t < 2.5\mu s$. The PMOS will start to conduct and act like a diode-connected load with a drain current $I_D = g_m(v_{in} - v_c)$. When there is a nonzero I_D in the circuit, the capacitor starts to charge. since of this, the current starts to drop since the difference $v_{in} - v_c$ drops. Now, between $2.5\mu s \leq t < 5\mu s$, the applied voltage drops, the capacitor starts to discharge, and when $|v_{in} - v_c| < v_{tp}$, the current in the circuit stops flowing again. PMOS turns OFF again. In the negative half cycle, from $5\mu s \leq t < 7.5\mu s$, the current gets stronger, but the direction changes because the capacitor starts to discharge. Finally, when $|v_{in} - v_c| < v_{tp}$, the current drops back to zero in the time range $7.5\mu s \leq t < 10\mu s$.

3.1.3 Model Simulation and Experimental Validation

The suggested memristor emulator circuit was simulated in the Cadence Virtuoso Spectre environment. The experimental validation setup contained a $1\text{ k}\Omega$ resistor, capacitors with values of 1 nF , 47 nF , 100 nF , and the ALD1117 dual P-channel enhancement-mode MOSFET

array. The circuit's physical arrangement (Figure 3.2 (b)) matches the schematic in Figure 3.1 and covers area roughly $1.586 \mu\text{m}^2$. Because the design does not use any external biasing sources, static power dissipation is nil, however dynamic power consumption varies according on the applied input voltage and resulting current.

To conduct simulations, we used an RC tank circuit with a $R = 100\text{k}\Omega$ resistor, $C = 100\text{pF}$ capacitor, and a $0.9\mu\text{m}/0.045\mu\text{m}$ PMOS transistor. Figure 3.3 shows that applying a sinusoidal input voltage with $0.8V_{p-p}$ amplitude and 100 kHz frequency validates memristive behavior in the emulator's transient current waveform.

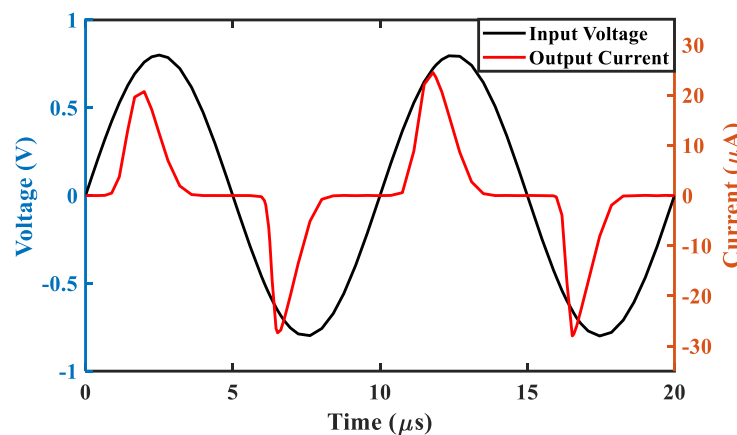


Figure 3. 3 The transient current response to the applied sinusoidal input of $0.8 V_{p-p}$ and frequency of 100 kHz

Pinched hysteresis loops, a trademark of memristive systems, were plotted for input frequencies ranging from 50 kHz to 1 MHz and 5 MHz to 80 MHz , as demonstrated in Figures 3.4 (a) and 3.4(b), respectively. The symmetry or asymmetry of these hysteresis loops is determined by the resistor value (R) in the emulator circuit. As seen in Figure 3.5(a), decreasing resistance causes increased asymmetry in the hysteresis curves, underscoring the importance of resistance in determining the emulator's dynamic response.

Figure 3.5(b) shows how altering capacitance (C) affects the current responsiveness of the memristor emulator. The results clearly reveal that the hysteresis loops have well-defined symmetry, which confirms consistent memristive activity across capacitance values.

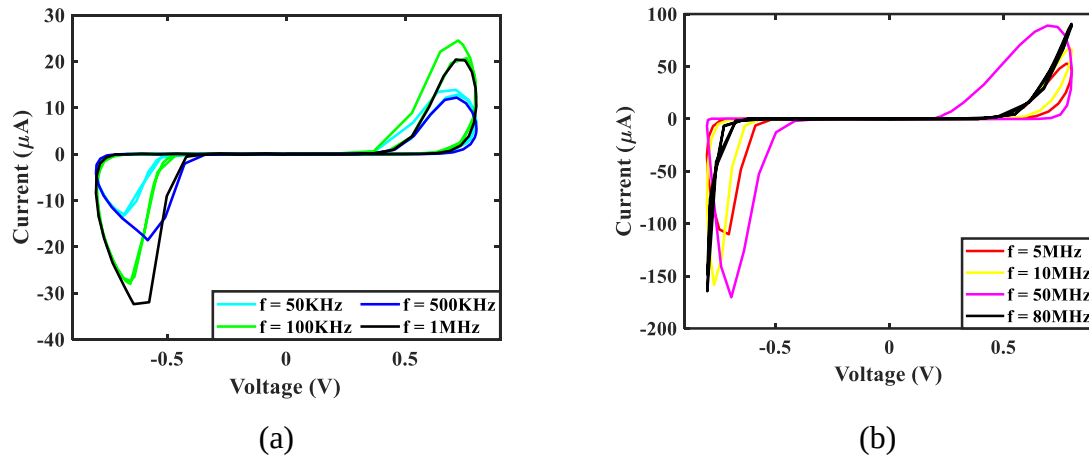


Figure 3.4 The pinched hysteresis curve for frequencies ranging from (a) 50 kHz to 1 MHz and (b) 5 MHz to 80 MHz

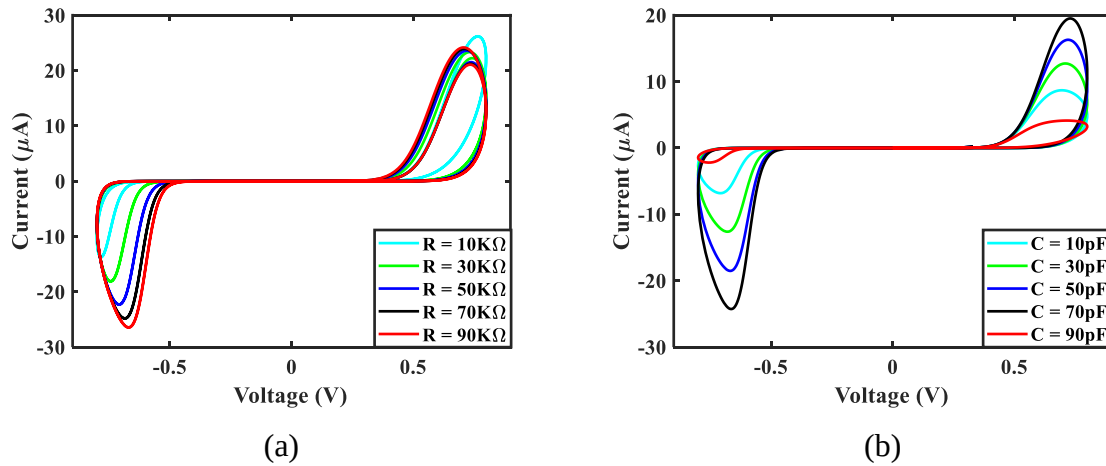


Figure 3.5 (a) Hysteresis curve of memristor emulator at different values of resistances (asymmetric). (b) Hysteresis curve at different values of capacitances

Figure 3.6 (a) shows that the voltage-current characteristics of the memristor remain consistent when the product of the input frequency and the capacitor value is remained constant. This happens because the capacitive reactance remains constant under these conditions, retaining the circuit's dynamic response.

In Fig. 3.6 (b), the suggested emulator's memductance decreases with a pulse input of $V_P = 0.8\text{ V}$ with a total period $T = 10\mu\text{ s}$, ($T = T_{\text{on}} (500\text{ ns}) + T_{\text{off}}$). The RC tank circuit consists of a $C = 1\text{ nF}$ capacitor and a $R = 50\text{ k}\Omega$ resistor. The ensuing staircase-shaped voltage at the capacitor terminal shows that the memductance holds its value even when the input pulse is withdrawn, demonstrating the emulator's non-volatile functionality.

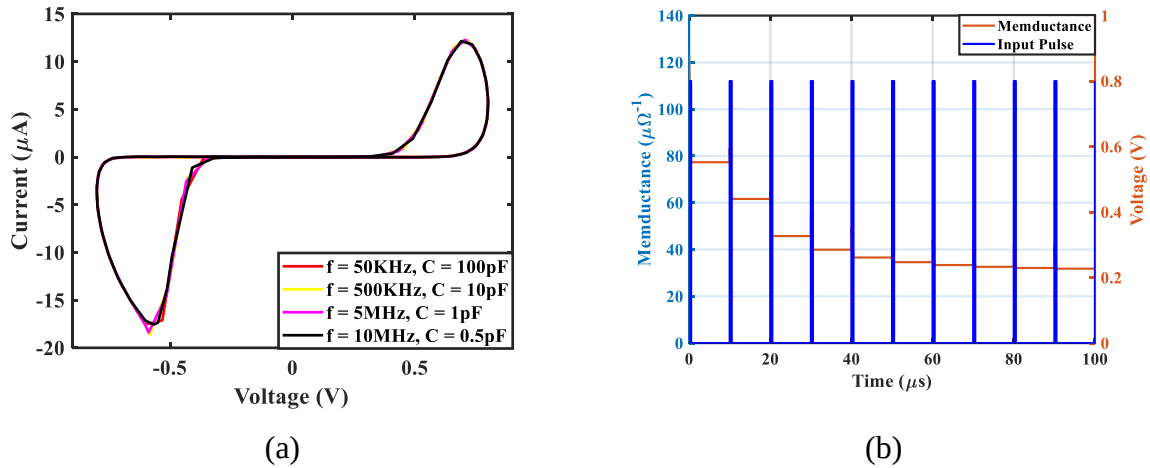
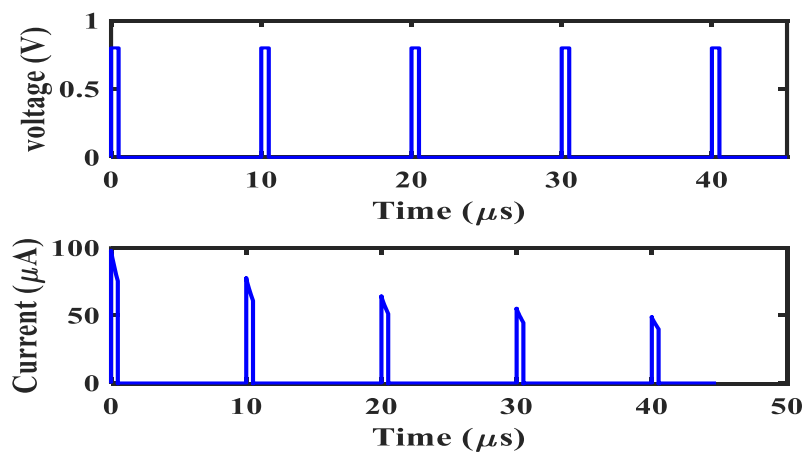


Figure 3. 6 (a) V–I curves for memristor emulator ($f \times C = \text{constant}$ behavior). (b) The incremental behavior of the presented memristor emulator.

Figure 3.7 (a) shows another illustration of the nonvolatile characteristic. Applying the same pulse train reduces the circuit's current from roughly 98 μA to 80 μA during the first ON cycle (500 ns). Surprisingly, this lower current level is maintained throughout the OFF cycle, demonstrating the suggested memristor emulator's ability to preserve memory.

Figure 3.7 (b) shows that the suggested memristor emulator performs consistently at temperatures ranging from $-40^\circ\text{C} - 80^\circ\text{C}$. Figure 3.7 (c) shows that the proposed memristor emulator performs well with different process such as slow-slow (SS), fast-slow (FS), slow-fast (SF), fast-fast (FF), and normal (NN).



(a)

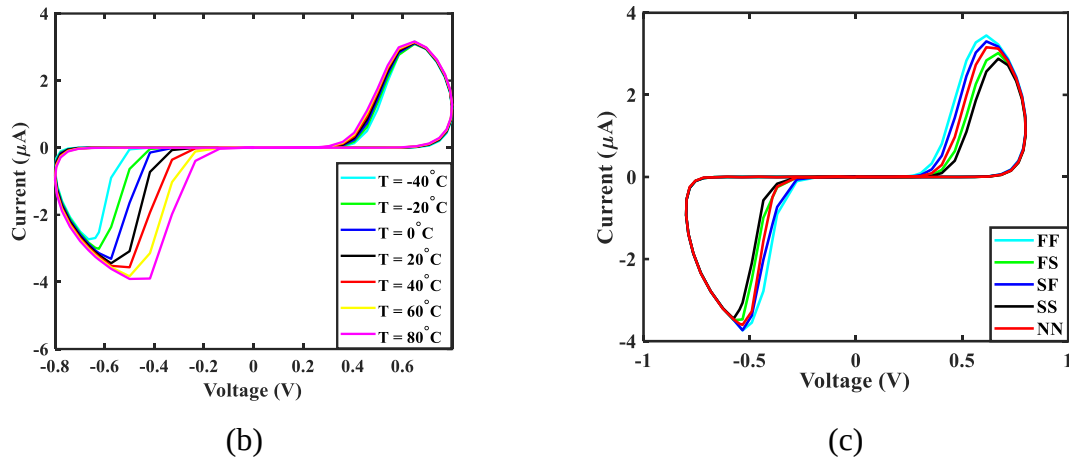


Figure 3.7 (a) Non-volatility behaviour of proposed memristor emulator. (b) The pinched hysteresis for different temperatures in $^\circ C$

Figure 3.8 (a) depicts the impact of altering the MOSFET's W/L ratio. The data clearly show that the aspect ratio has a direct influence on the emulator's drain current, with larger W/L ratios resulting in more current. Figure 3.8(b) depicts the behavior of the memristor emulator in both serial and parallel setups. In the series configuration, the current drops as the memristance value increases. In contrast, in the parallel design, the current increases due to the effective reduction in memristance.

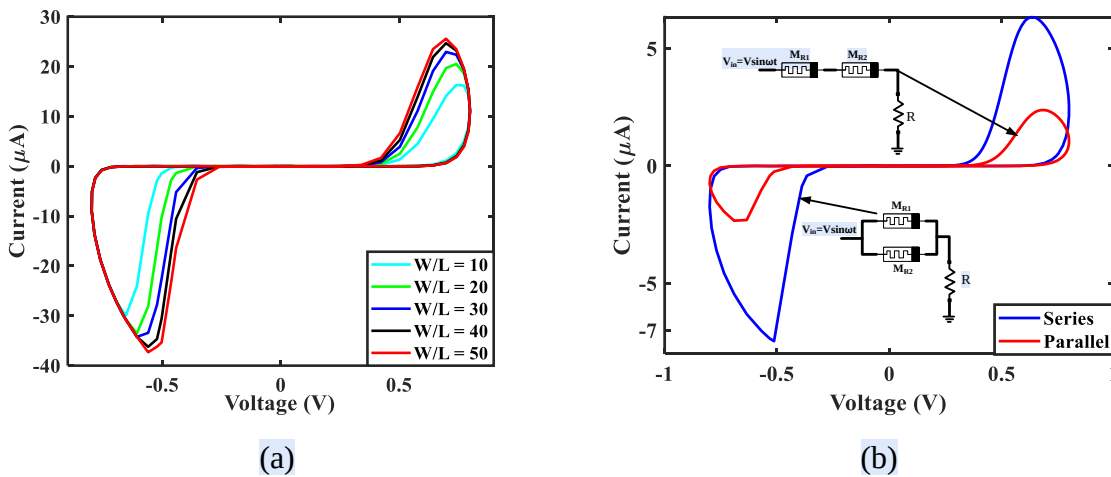


Figure 3.8 (a) The PH curves for varied W/L ratios. (b) The PH curve for different combinations (series and parallel) of memristor at 100 kHz

A Monte Carlo analysis of 200 simulation runs was performed to assess the emulator design's resilience and statistical reliability. The main parameters examined were drain current, threshold voltage, power consumption, and output resistance. The performance parameters were consistent throughout all trials, demonstrating the design's reliability. Figures 3.9 (a-d) illustrate the frequency distributions for various parameters. Figure 3.9 (a) shows the current

distribution in μA , figure 3.9(b) shows threshold voltage (in V), figure 3.9 (c) shows power consumption (in pW), and figure 3.9(d) shows output resistance (in $\text{G}\Omega$).

Each distribution is within the $\pm 3\sigma$ range around the mean (μ), where σ represents the standard deviation, indicating minimal volatility and strong parameter stability.

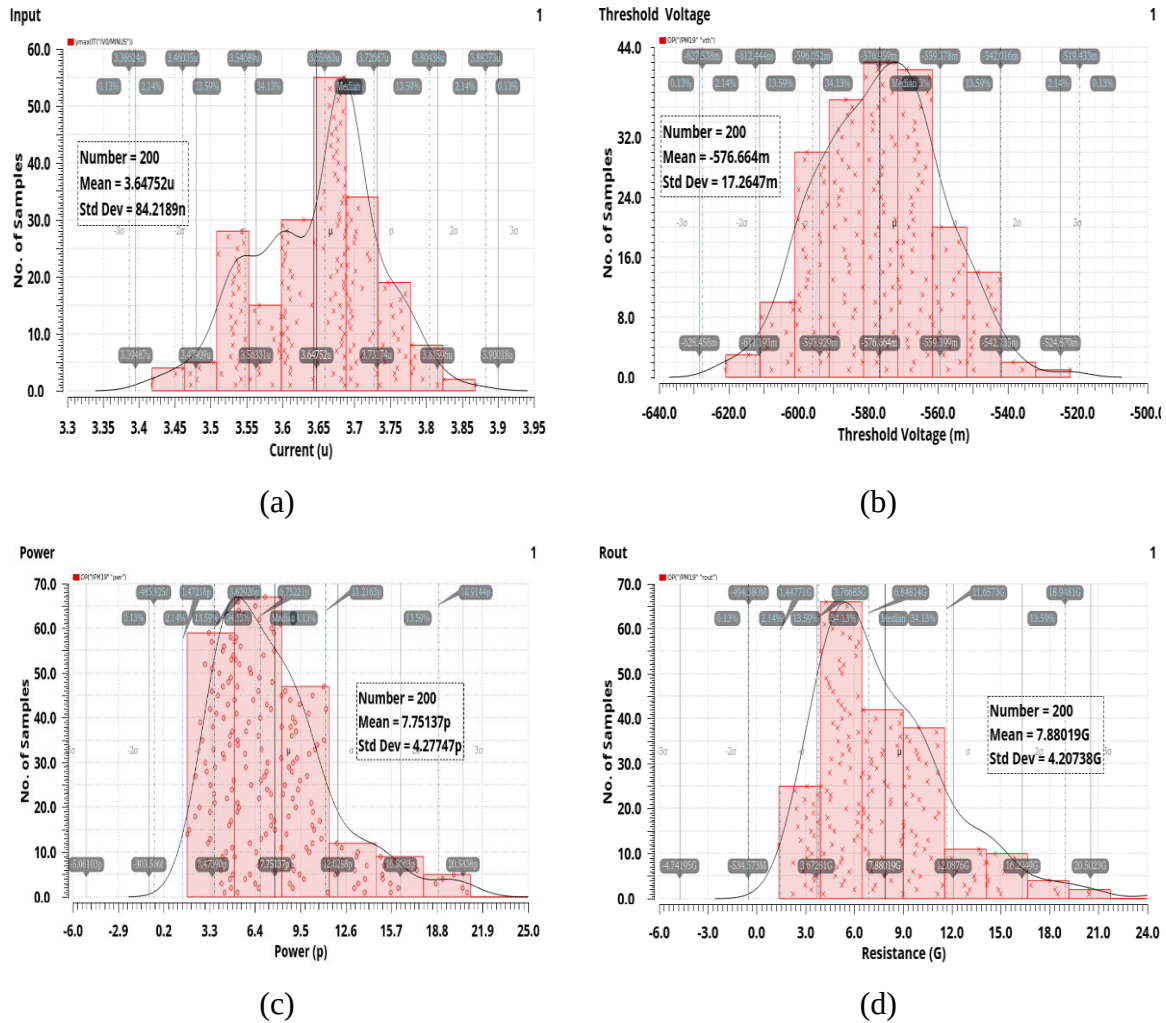
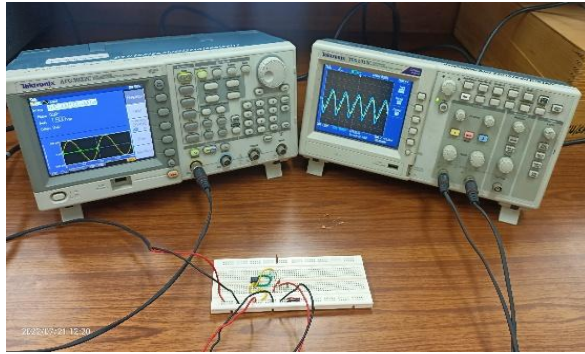
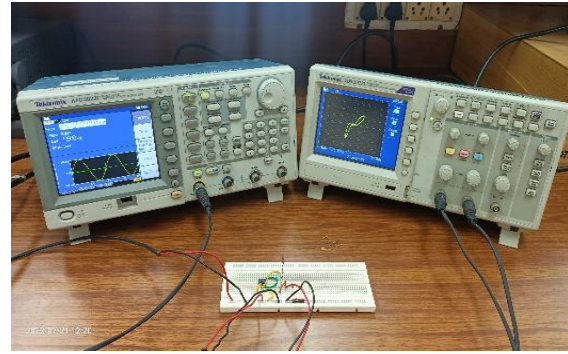


Figure 3. 9 Monte Carlo simulation results for different parameters (I_{max} , V_{th} , P , and M_{R}) of memristor emulator. (a) Monte Carlo for current in μA , (b) Monte Carlo for threshold voltage in V , (c) Monte Carlo power in pW, (d) Monte Carlo for memristance in $\text{G}\Omega$

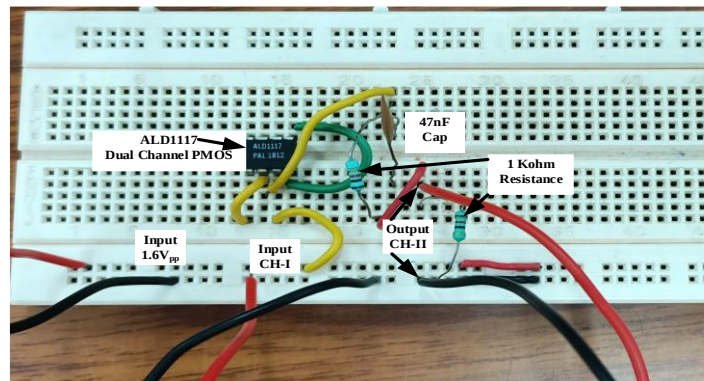
Figure 3.10 depicts the experimental setup for validation, which included a Tektronix TDS 2012C dual-channel digital storage oscilloscope (DSO) with 100 MHz bandwidth and 2 GS/s sampling rate. The experimental results (Figure 3.11) show hysteresis curves at various frequencies, proving the functional accuracy and operational reliability of the proposed memristor emulator topology.



(a)

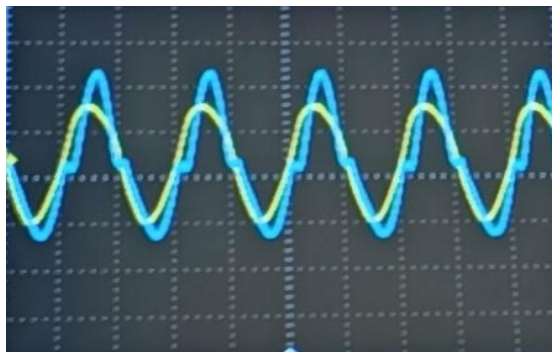


(b)

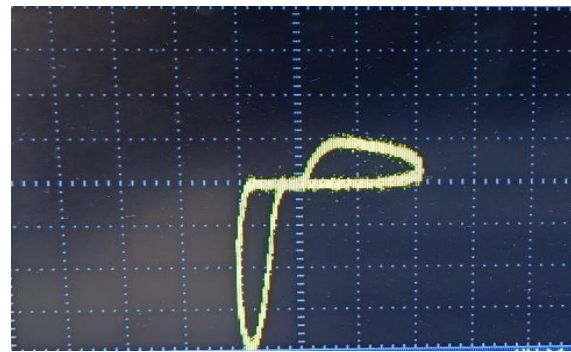


(c)

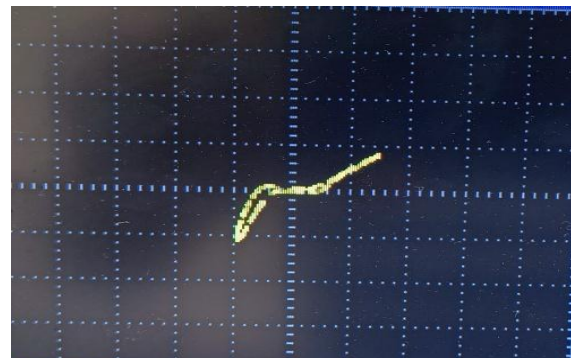
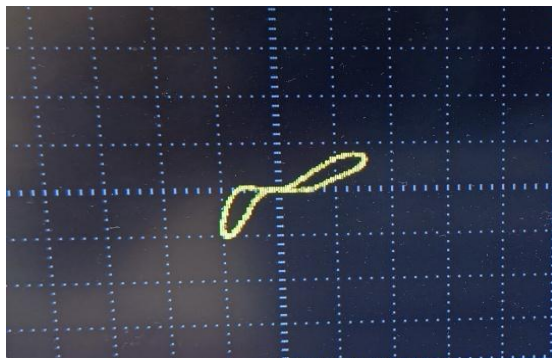
Figure 3. 10 (a) Complete hardware setup using breadboard circuit implementation (b) complete hardware setup at operating frequency of 100 kHz, and (c) breadboard circuit connections



(a)



(b)



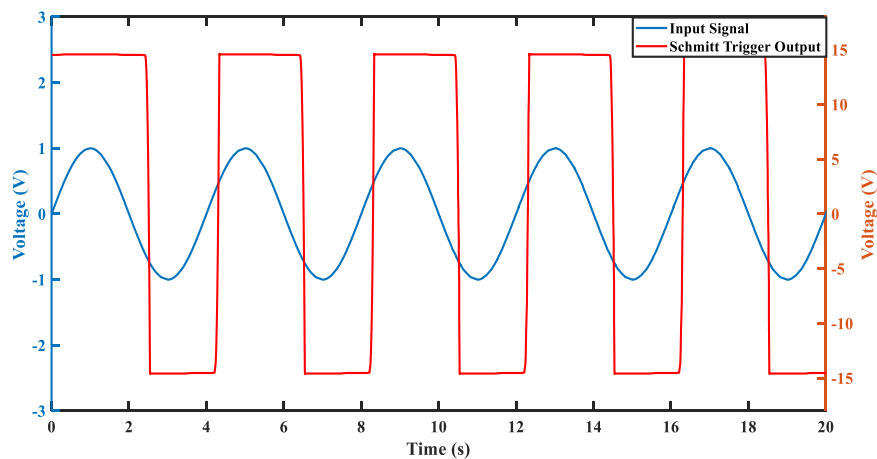
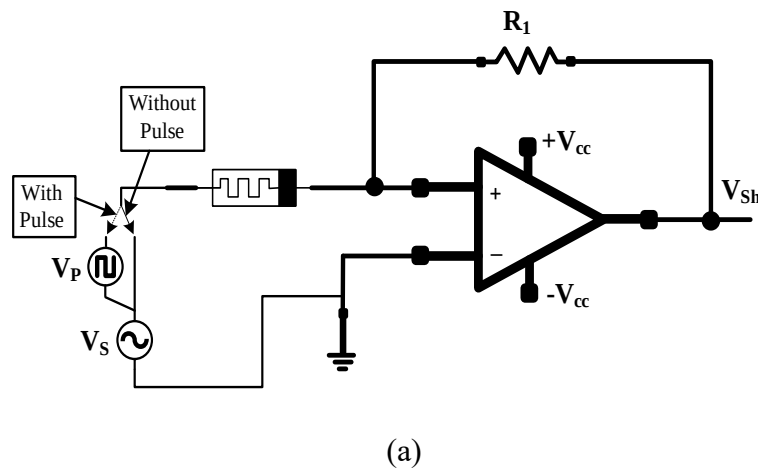
(c)

(d)

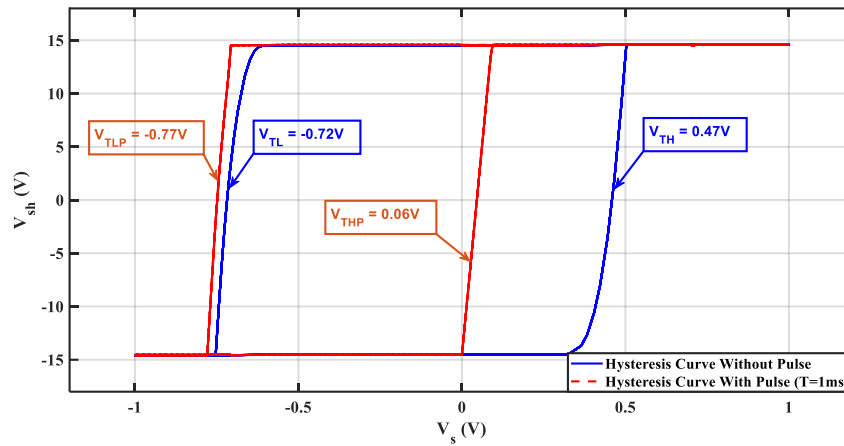
Figure 3. 11 Experimental PH curve for the proposed memristor emulator. (a) Input and output waveform. (b) PH curve at 50 kHz. (c) PH curve at 100 kHz. (d) PH curve at 500 kHz

3.1.4 Proposed Memristor Emulator Applications

Schmitt Trigger: In this section, we demonstrate some applications of the proposed memristor emulator, highlighting the emulator's usability and practical usefulness. The suggested emulator circuit is utilized to create a Schmitt trigger, a chaotic Colpitts oscillator, and an XOR function. The Schmitt trigger circuit depicted in Figure 3.12(a) is built around a single operational amplifier (TL082CD).



(b)



(c)

Figure 3. 12 Implementation of Schmitt trigger using proposed memristor emulator. (a) circuit diagram of Schmitt trigger. (b) Input (sinusoidal) and output (square) voltages for the Schmitt trigger circuit. (c) threshold voltage variation with external pulse

The upper and lower thresholds of the Schmitt trigger are given by

$$V_{TH} = V_{sat} \left(\frac{M_R}{R_1} \right), V_{TL} = -V_{sat} \left(\frac{M_R}{R_1} \right) \quad 3.10$$

V_{sat} indicates the saturation voltage of the OP-AMP (in volts), M_R specifies the memristance of the memristor emulator, and R_1 refers to the resistor value in the circuit. The operational amplifier is powered by a ± 15 V DC source. A resistor value of $R_1 = 50M\Omega$ powered by a sinusoidal input signal with a frequency of 250 Hz and a peak-to-peak voltage of 0.8 V (V_{p-p}). Figure 3.12 (b) illustrates the Schmitt trigger's input and output waveforms. Adding a 1 V programming pulse at 250 Hz to the input signal alters the circuit's hysteresis properties, as illustrated in Figure 3.12 (c). The emulator's memristance can be changed using a sequence of programming pulses, which alters the threshold voltage (V_{th}) of the Schmitt trigger circuit.

Memristive Colpitts Chaotic Oscillator: It has been reported earlier works that a fourth-order Colpitts oscillator is capable of exhibiting chaotic behavior. By incorporating a generalized memristor into the Colpitts configuration, a memristor-based chaotic oscillator is realized in reference [59]. In this proposed design, we have replaced the generalised memristor with the proposed single MOS memristor circuit. Considering the internal state variable v_0 associated with the memristor, the overall system becomes a fifth-order dynamical circuit.

As shown in Figure 3.13 (a) an NPN bipolar junction transistor is employed as the nonlinear active element in the oscillator. Neglecting parasitic effects, the transistor nonlinearity is

modelled using its exponential current–voltage characteristic, assuming a common-base forward current gain of unity. The transistor behavior is described using two parameters: the transport saturation current I_S and the thermal voltage V_T . Accordingly, the emitter current is expressed as

$$i_e = I_S \left(e^{\frac{v_{be}}{V_T}} - 1 \right) = I_S (e^{2\rho v_1} - 1) \quad 3.11$$

where $\rho = \frac{1}{V_T}$ and i_e denotes the emitter current. For the 2N2222 transistor used in this work, the parameters are $I_S = 3.0484 \text{ nA}$ and $V_T = 25 \text{ mV}$.

The system consists of four state variables corresponding to the voltages across capacitors C_1 , C_2 , and C_3 , denoted by v_1 , v_2 , and v_3 , respectively, along with the inductor current i_L . Additionally, the memristor introduces an extra state variable v_0 , representing the voltage across capacitor C_0 as shown in equation 3.6. By applying Kirchhoff's circuit laws and the constitutive relations of the circuit elements, the governing state equations can be derived as follows:

$$\begin{aligned} C_1 \frac{dv_1}{dt} &= i_M - i_R - \frac{V_{EE} + v_1}{R_1}, \\ C_2 \frac{dv_2}{dt} &= i_R - i_M - i_e, \\ C_3 \frac{dv_3}{dt} &= i_R - i_M - i_L, \\ L \frac{di_L}{dt} &= v_3, \\ C_0 \frac{dv_0}{dt} &= k(v_M - v_{tp})^2 - \frac{v_0}{R} \end{aligned} \quad 3.12$$

The analysis is carried out under the assumptions $i_b = 0$ and $i_c = i_e$. The memristor voltage is given by

$$v_M = -v_1 + v_2 + v_3,$$

while the memristor current and resistor current are expressed as

$$\begin{aligned} i_M &= k(v_M - v_{tp})^2, \\ i_R &= \frac{V_{CC} - v_M}{R_0} \end{aligned} \quad 3.13$$

By substituting equations (4) and (6) into (5), the resulting state equations are obtained as

$$\frac{dv_1}{dt} = \frac{k(v_M - v_{tp})^2}{C_1} - \frac{V_{CC} - v_M}{R_0 C_1} - \frac{V_{EE} + v_1}{R_1 C_1},$$

$$\begin{aligned}
 \frac{dv_2}{dt} &= \frac{V_{CC} - v_M}{R_0 C_2} - \frac{k(v_M - v_{tp})^2}{C_2} - \frac{I_S(e^{2\rho v_1} - 1)}{C_2}, \\
 \frac{dv_3}{dt} &= \frac{V_{CC} - v_M}{R_0 C_3} - \frac{k(v_M - v_{tp})^2}{C_3} - \frac{i_L}{C_3}, \\
 \frac{di_L}{dt} &= \frac{v_3}{L}, \\
 \frac{dv_0}{dt} &= \frac{k(v_M - v_{tp})^2}{C_0} - \frac{v_0}{RC_0}
 \end{aligned} \tag{3.14}$$

Finally, the above set of equations forms a five-dimensional nonlinear dynamical system, which serves as the basis for numerical analysis of the memristive Colpitts oscillator. The Jacobian matrix of (3.14), evaluated at the equilibrium point

$$\bar{S} = (\bar{v}_1, \bar{v}_2, \bar{v}_3, \bar{i}_L, \bar{v}_0),$$

is given by

$$J = \begin{bmatrix} -\frac{a_1}{C_1} - \frac{1}{R_1 C_1} & \frac{a_1}{C_1} & \frac{a_1}{C_1} & 0 & -\frac{a_2}{C_1} \\ \frac{a_1}{C_2} - \frac{a_3}{C_2} & -\frac{a_1}{C_2} & -\frac{a_1}{C_2} & 0 & \frac{a_2}{C_2} \\ \frac{a_1}{C_3} & -\frac{a_1}{C_3} & -\frac{a_1}{C_3} - \frac{1}{C_3} & -\frac{1}{C_3} & \frac{a_2}{C_3} \\ 0 & 0 & \frac{1}{L} & 0 & 0 \\ -\frac{a_2}{C_0} & \frac{a_2}{C_0} & \frac{a_2}{C_0} & 0 & \frac{1}{C_0} \left(\frac{1}{R_0} - \frac{1}{R_1} - a_1 \right) \end{bmatrix} \tag{3.15}$$

where

$$\begin{aligned}
 a_1 &= k(-\bar{v}_1 + \bar{v}_2 + \bar{v}_3 - v_{tp})^2 + \frac{1}{R_0} \\
 a_2 &= (-\bar{v}_1 + \bar{v}_2 + \bar{v}_3 - v_{tp})^2, \\
 a_3 &= \rho I_S e^{2\rho \bar{v}_1}
 \end{aligned} \tag{3.16}$$

Thus, the corresponding characteristic equation can be written as

$$\det(\lambda I - J) = 0 \tag{3.17}$$

For the circuit parameters illustrated above, the eigenvalues evaluated at the equilibrium point are given by

$$\lambda_{1,2} = \alpha_1 \pm j\beta_1 (\alpha_1 > 0)$$

$$\lambda_{3,4} = -\alpha_2 \pm j\beta_2 (\alpha_2 < 0)$$

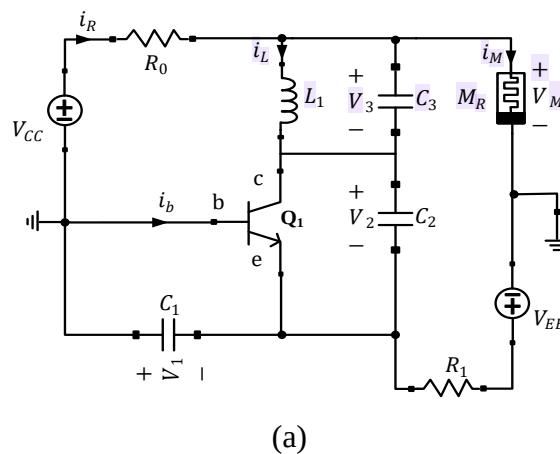
$$\lambda_5 = -\gamma (\gamma < 0)$$

From these results, it is observed that the system possesses:

- One pair of complex conjugate eigenvalues with positive real parts,
- One pair of complex conjugate eigenvalues with negative real parts, and
- One negative real eigenvalue.

This combination indicates that the equilibrium point is an unstable saddle-focus. Consequently, the system exhibits divergent yet bounded trajectories, leading to the formation of a spiral chaotic attractor.

Figure 3.13 (a) depicts further investigation of a memristor-based Colpitts oscillator. This oscillator has a BJT as a nonlinear component, capacitors ($C_0 = 100\text{pF}$, $C_1 = C_2 = 2\text{ }\mu\text{F}$, $C_3 = 33\text{ }\mu\text{F}$), an inductor ($L = 10\text{ mH}$), and resistors ($R = 100\text{k}\Omega$, $R_0 = 35\text{ }\Omega$, $R_1 = 1.5\text{ k}\Omega$) with dual power supply $V_{CC} = 5\text{ V}$ and $V_{EE} = -5\text{ V}$. Figures 3.13 (b) and 3.13 (c) exhibit spiral chaotic attractors with initial values $V_1(0) = 0.01\text{ V}$, $V_2(0) = 0.01\text{ V}$, $V_3(0) = 0\text{ V}$, $i_L(0) = 0\text{ A}$, and $V_0(0) = 0\text{ V}$.



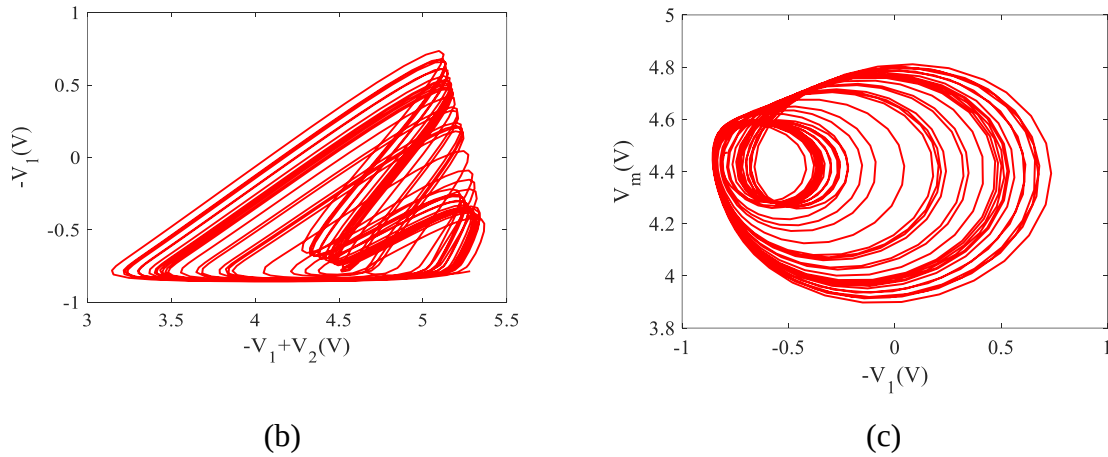


Figure 3.13 (a) Colpitts Chaotic Oscillator Circuit using memristor (b) Colpitts chaotic oscillator circuit performance for $(-V_1 + V_2)$ Vs $-V_1$ (c) Colpitts chaotic oscillator circuit performance for $-V_1$ Vs V_m

XOR Logic: Following that, an XOR logic gate is implemented with a differential amplifier arrangement and the proposed memristor emulator. The entire circuit is depicted in Figure 3.14(a). It has two main modules: an input and logic module, which includes the memristor, and an output test module. The differential amplifier utilizes the TL082 operational amplifier, which has dual channels and a gain-bandwidth product of 3MHz.

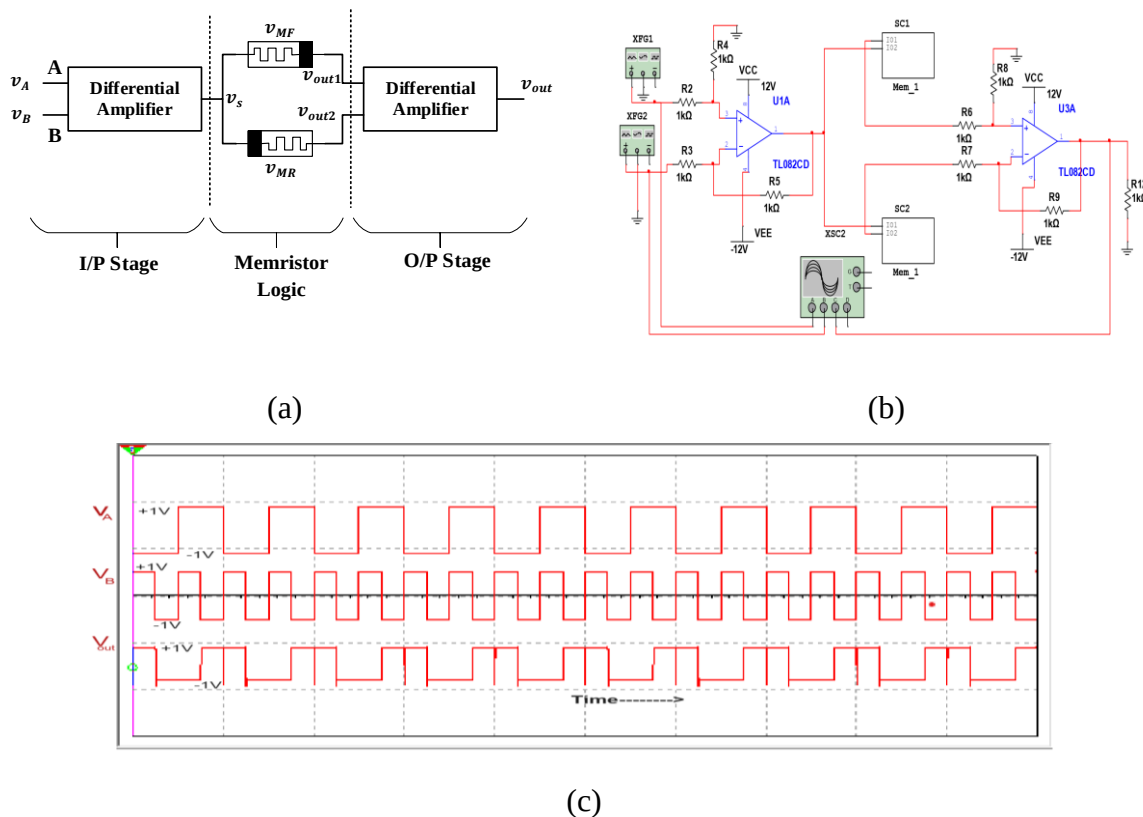


Figure 3.14 XOR logic implementation using Multisim. (a) XOR logic diagram. (b) circuit realization using Multisim. (c) transient analysis of the XOR logic circuit

Table 3. 1 Truth Table of Memristor XOR Logic Circuit

$A(v_A)$	$B(v_B)$	$v_A - v_B$	$v_{out} = v_{out 1} - v_{out 2}$	logic
V_1	V_1	0	0	0
V_1	0	V_1	> 0	1
0	V_1	$-V_1$	> 0	1
0	0	0	0	0

The functional behavior of the XOR logic gate is validated using the truth table shown in Table 3.1. Figure 3.14 (b) shows the implementation of the XOR logic gate using Multisim software, whereas Figure 3.14 (c) shows the transient behavior of the XOR logic gate implemented using the proposed memristor emulator.

$$v_{out 1} = |v_S| - v_{MF}, v_{out 2} = |v_S| - v_{MR}, v_{out} = v_{out 1} - v_{out 2} \quad 3.18$$

Tables 3.2 and 3.3 provide a comparative overview of previously reported memristor emulators [47], [49], [50], [53], [57], [60], [61], [95], [96], [98], [105], [106], [115]–[117], [119]–[121], [125]–[128], evaluating them on criteria such as active or passive component use, circuit topology, simulation and experimental validation, fabrication technology, operating frequency, and power consumption. A large number of these designs, including those in [95], [96], [98], [105], [106], [125]–[128], use a larger MOSFET count. In contrast, designs in [49], [50], [53], [108], [115]–[117], [119]–[121], use fewer MOSFETs, but at the expense of lower frequency operation and higher power dissipation when compared with the suggested design. Some general-purpose memristor implementations, such as those described in [57], [60], [61], mix passive and active components but have low operating frequencies. This work presents a unique memristor emulator that uses a single MOSFET and an R-C filter to achieve an operating frequency of up to 80 MHz with a low dynamic power consumption of 7.751 pW. Importantly, the absence of any external biasing source results in zero static power consumption, making the suggested device entirely passive and highly efficient in both performance and power.

Table 3. 2 Comparison of the Proposed Model with Existing Memristor Emulators on the basis of Design

Ref No.	Publication Year	MOSFET Count	Existing Blocks Used	Passive/ Active Component Count
[95]	2017	38	OTA-1	R - 1, C - 1
[96]	2023	17	OTA-1	C - 1
[98]	2023	> 20	OPAMP-1	R - 1, C - 1
[105]	2017	30	CCTA - 1	R - 3, C - 1
[106]	2017	29	DVCCTA - 1	R - 3, C - 1
[127]	2021	16	VDTA-1	C-1, R-1
[126]	2022	18	VDIBA-2	C-1
[125]	2023	22	CFDITA-1	C-1
[128]	2019	26	VDCC-1 MOSFET-2	C-1
[47]	2019	3	-	C - 1
[49]	2018	4	-	-
[50]	2018	7	-	C - 1
[116]	2022	4	-	-
[117]	2019	4	-	-
[115]	2022	4	-	C - 1
[120]	2023	4	-	C - 1
[119]	2023	3	-	C - 1
[121]	2023	2	-	-
[53]	2017	6	-	C - 1
[57]	2014	-	-	D - 4, R - 1, C - 1
[60]	2020	-	-	D - 6, R - 1, C - 1
[61]	2022	-	-	D - 4, R - 1, C - 1
Proposed Work	-	1	-	R - 1, C -1

Table 3. 3 Comparison of the Proposed Model with Existing Memristor Emulators on the basis of performance

Ref No.	Experiment/ Simulation	Floating /Grounded	Technology	Frequency	Power Consumption	Layout Area
[95]	Both	Grounded	0.18 μ m CMOS	1 kHz	Few nW	NA
[96]	Simulation	Floating	0.18 μ m GPDK	1 MHz	411 μ W	2596 μ m ²

[98]	Both	Floating	-	30MHz	Few mW	NA
[105]	Both	Both	0.18 μ m TSMC	10 MHz	5.22 mW	NA
[106]	Both	Grounded	0.25 μ m TSMC	1 MHz	4.88mW	NA
[127]	Both	Floating	0.18 μ m CMOS	50MHz	8 μ W	1065 μ m ²
[126]	Both	Grounded	0.18 μ m TSMC	12.7MHz	1.34mW	NA
[125]	Both	Both	0.18 μ m GPDK	10MHz	4.8 μ W	112 μ m ²
[128]	Both	Grounded	0.18 μ m TSMC	2MHz	NA	NA
[47]	Both	Floating	0.18 μ m TSMC	13 MHz	6.725nW	2803 μ m ²
[49]	Both	Grounded	0.18 μ m TSMC	100MHz	NA	366 μ m ²
[50]	Both	Grounded	0.18 μ m TSMC	50 MHz	-	456 μ m ²
[116]	Both	Floating	0.09 μ m GPDK	50MHz	2.6 μ W	59.41 μ m ²
[117]	Simulation	Grounded	0.18 μ m TSMC	100 kHz	400 μ W	196 μ m ²
[115]	Both	Floating	0.18 μ m TSMC	3MHz	8.24 μ W	158 μ m ²
[120]	both	Grounded	0.18 μ m GPDK	10MHz	20 μ W	NA
[119]	both	Grounded	0.09 μ m GPDK	5KHz	175nW	1154 μ m ²
[121]	both	Floating	0.065 μ m GPDK	300MHz	Zero	4.62 μ m ²
[53]	Simulation	Floating	0.18 μ m TSMC	10 Hz	-	NA
[57]	Both	Both	-	10 kHz	-	NA
[60]	Both	Both	-	20 kHz	-	NA
[61]	Both	Both	-	10 kHz	-	NA
Proposed Work	Both	Both	0.045 μ m GPDK	80 MHz	Zero	1.96 μ m ²

3.2 A passive grounded MOSCAP- memristor emulator

This section describes a grounded passive MOSCAP-based memristor emulator that uses only three MOSFETs and a single MOS capacitor and operates without external biasing. Unlike previous designs, which relied on complex arrangements with several active blocks and passive components, the suggested architecture has a much simplified structure. The circuit is developed and simulated in Cadence Virtuoso using GPDK 180 nm CMOS technology, with sinusoidal and pulse input inputs. The device can operate at frequencies up to 30 MHz and is

studied using pinched hysteresis loops and current-voltage characteristics that vary based on voltage polarity. The simulation results confirm the main behavioral fingerprints of an ideal memristor, and the proposed design is proven by its use in filter circuits, proving its promise in analog signal processing applications.

3.2.1 Proposed MOSCAP-memristor emulator circuit

This study offers a circuit configuration, represented in Figure 3.15, that consists of three NMOS transistors labeled N_1 , N_2 , and N_3 , as well as a single PMOS-based MOS capacitor (P_1). The circuit behaves like a memristor, with a nonlinear response and a constricted hysteresis loop under sinusoidal excitation. The circuit is designed as a passive grounded memristor emulator and does not require external biasing. In this system, the MOSCAP (P_1) modulates N_1 and N_2 , while N_3 controls the capacitor's charging and discharging dynamics. The MOSCAP acts as a passive storage element, enhancing the circuit's non-volatile nature. Table 3.4 shows the width-to-length (W/L) ratios of the circuit's constituent transistors.

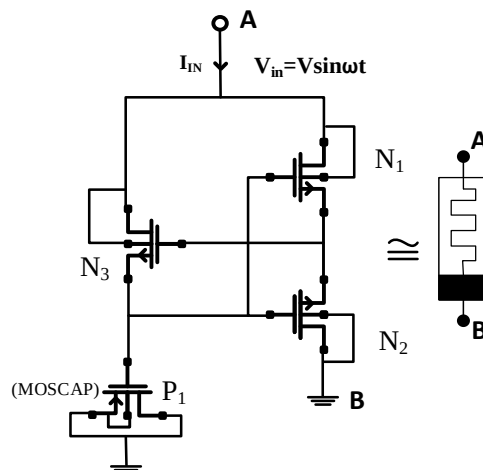


Figure 3. 15 Circuit diagram of MOSCAP-memristor emulator

Table 3. 4 W/L Ratios of NMOS and PMOS for MOSCAP-Memristor Emulator

Transistor	W/L Ratio (in $\mu\text{m}/\mu\text{m}$)
N_1	4/2
N_2	10/1
N_3	1/1
P_1	10/10

3.2.2 Simulation results of MOSCAP-memristor emulator circuit

In this work, all three distinctive fingerprints of a memristor were thoroughly examined and simulated utilizing Cadence Spectre tool and 180nm GPDK CMOS technology. The first fingerprint, the voltage-current (V-I) relationship, was investigated by monitoring signals at the input terminal, with the other terminal grounded due to the grounded memristor design. Figure 3.16 (a) shows a pinched hysteresis loop throughout a frequency range of 100 kHz to 30 MHz, with a sinusoidal input signal of 1.5 Vpp.

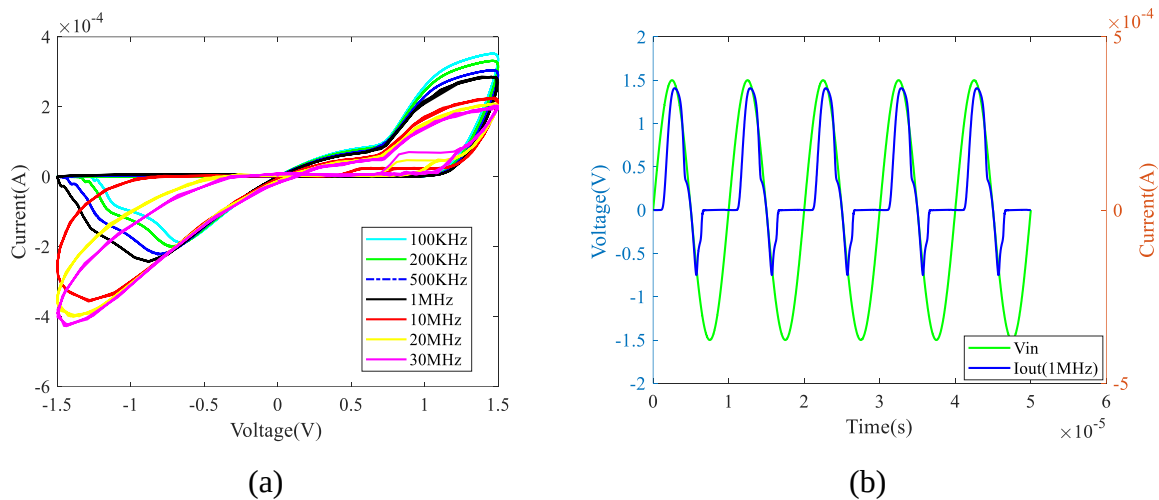


Figure 3. 16 (a) PHL curved for MOSCAP-memristor emulator at different frequencies (100 KHz – 30 MHz) (b) Transient waveforms of MOSCAP-memristor emulator at $f = 1$ MHz

Figure 3.16 (b) shows the voltage and current waveforms at 1MHz. The phase difference is virtually zero, indicating the memristor's resistive nature at that frequency. Figure 3.17 (a) depicts the second fingerprint, in which the memristor's performance is studied for various MOSCAP W/L ratios, revealing capacitance change as a function of frequency. This effect is further elaborated in Figure 3.17 (b), which shows the impact of MOS capacitance on different transistor shapes.

Figure 3.18 (a) depicts the third fingerprint, which proves the memristor's nonvolatile memory feature. A pulse signal (1 V amplitude, 500 ns pulse width, 10 μ s period, and 200 μ s total simulation duration) was applied, resulting in a gradual increase in voltage across the MOSCAP, indicating memory retention.

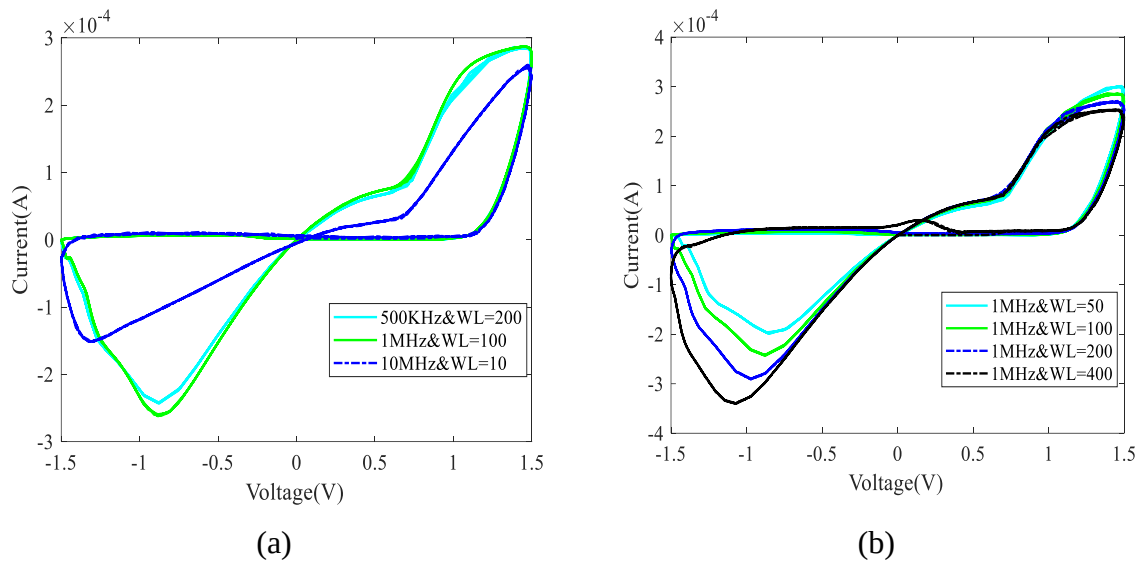
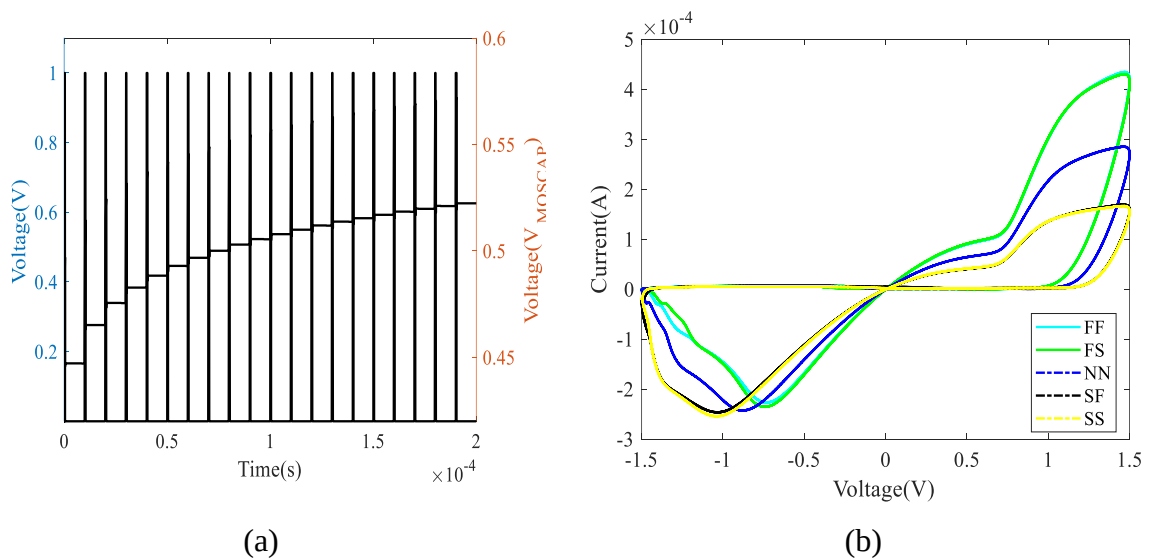
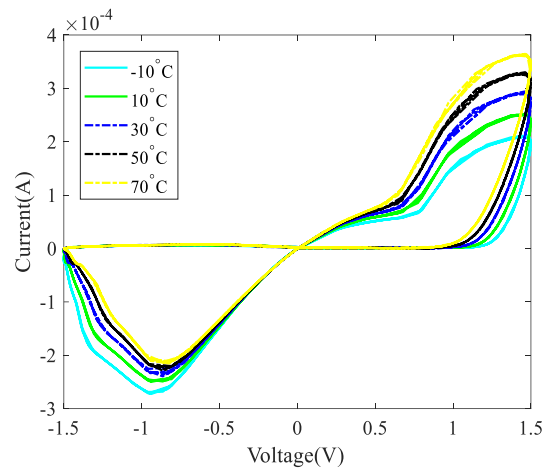


Figure 3. 17 (a) PHL curve (at different frequencies with different MOSCAP W/L Ratio) (b) PHL curve (at different MOSCAP W/L Ratio)

To ensure robustness under manufacturing differences, process corner simulations were performed for the FF, SS, NN, SF, and FS corners—where F represents Fast, S denotes Slow, and N denotes Nominal processes—as shown in Figure 3.18 (b). Temperature performance was also investigated between -10°C and 70°C , as shown in Figure 3.18 (c).

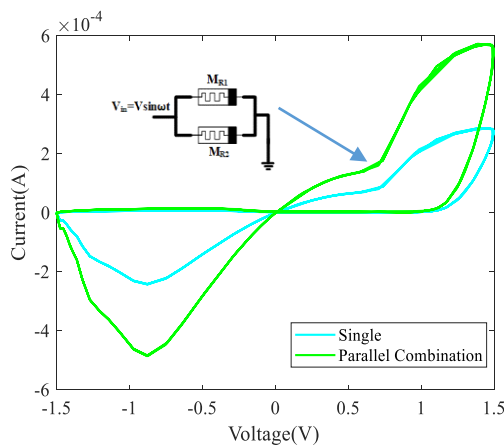
In addition, the behavior of two memristors operating in parallel was investigated (Figure 3.19 (a)). As expected, the combined memristance is less than that of a single memristor. Only the parallel design is considered because the proposed memristor is grounded.



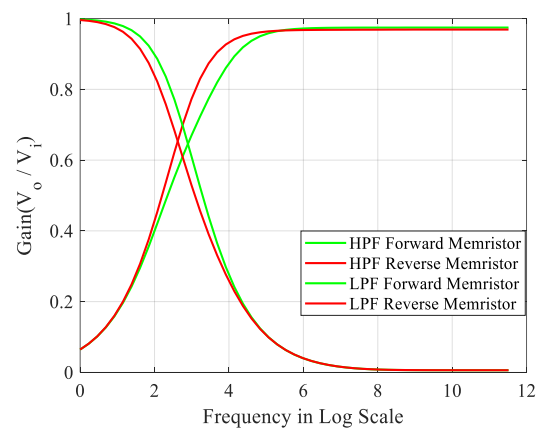


(c)

Figure 3. 18 (a) Non-volatility nature of MOSCAP-memristor emulator (b) Process Corner Analysis (for FF, FS, NN, SF, and SS) (c) Temperature variation analysis MOSCAP-memristor Circuit (-10°C to 70°C)



(a)



(b)

Figure 3. 19 (a) Effect on current of parallel combination of memristors (b) Response of passive high pass and low pass filters using memristor

The proposed emulator was also shown to work in passive filter circuits in practice. Figure 3.19 (b) shows simulated responses for low-pass (LPF) and high-pass filters (HPF), which corroborate the expected filtering behavior.

Cadence OrCAD-Capture was used to validate the memristor emulator, which included a discrete IRF840 MOSFET and a 22 nF capacitor operating at 100 kHz. The results, shown in Figure 3.20 (a-b) with MATLAB plots and OrCAD-Capture waveforms, validate the emulator's functionality.

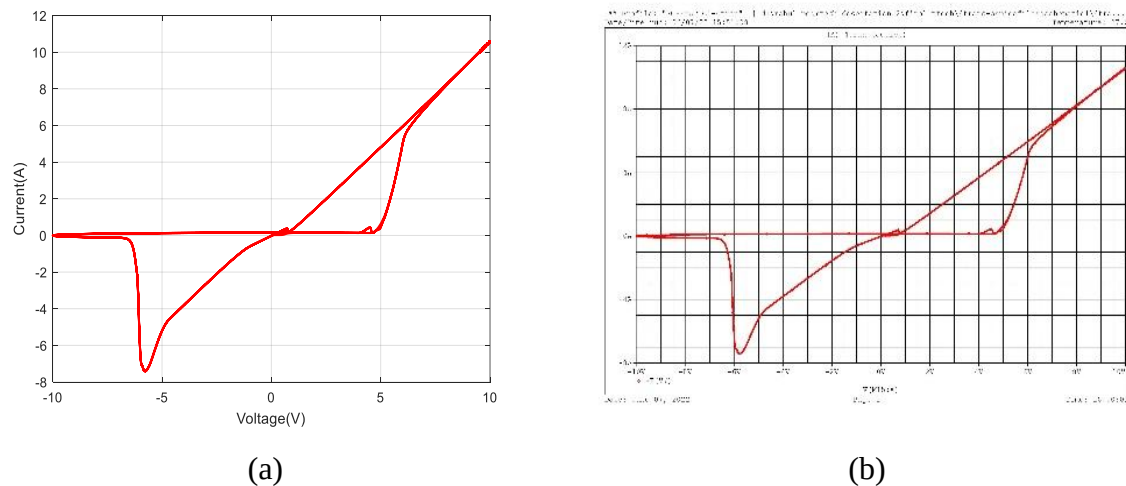


Figure 3. 20 (a) Experimental Result Plotted in MATLAB (b) Orcad-Capture Result using IRF840

Table 3.5. Comparison of MOSCAP-memristor emulator circuit with existing emulator circuit

Ref.	Existing Active Devices	Total Transistors	Passive Elements	Type of Memristor	Technology File	Power Dissipation	Working Frequency
[102]	DDCC	Forty	$R \rightarrow 2, C \rightarrow 1$	Grounded	35nm TSMC	-NA-	1MHz
[129]	-	Three	$C \rightarrow 1$	Grounded	180nm TSMC	0	100KHz
[53]	-	Three	$C \rightarrow 1$	Floating	180nm TSMC	6.725nW	13MHz
[47]	-	Three	0	Floating/ Grounded	180nm GPDK	0	20MHz/ 30MHz
[52]	OTA	Seventeen	$C \rightarrow 1$	Floating	180nm TSMC	-NA-	1 MHz
[130]	VDTA	Sixteen	$R \rightarrow 2, C \rightarrow 1$	Floating	180nm TSMC	-NA-	50 MHz
[131]		Sixteen	$C \rightarrow 1$	Floating	180nm TSMC	8.05 μ W	Few Hz
[54]	-	Seven	$C \rightarrow 1$	Grounded	180nm TSMC	-NA-	50MHz
Presented Circuit	-	Four	0	Grounded	180nm GPDK	0	30MHz

Finally, Table 3.5 summarizes the comparison with previous memristor emulator designs (completely floating, partially floating, and grounded). This comparison focuses on factors such as transistor count, grounding method, passive components, validation type (simulation/experimental), and operating frequency. Previous studies [47], [52]–[54], [102], [129]–[131] found larger transistor counts in [54], [102], [130], [131], but lower frequency operation was recorded in [53], [102], [129]–[131]. The proposed device, which employs four

MOSFETs and a MOSCAP, operates at high frequencies with no static power consumption, providing an efficient and compact memristor emulator solution.

3.3 A Passive Floating C-MOS Memristor with Analog Applications

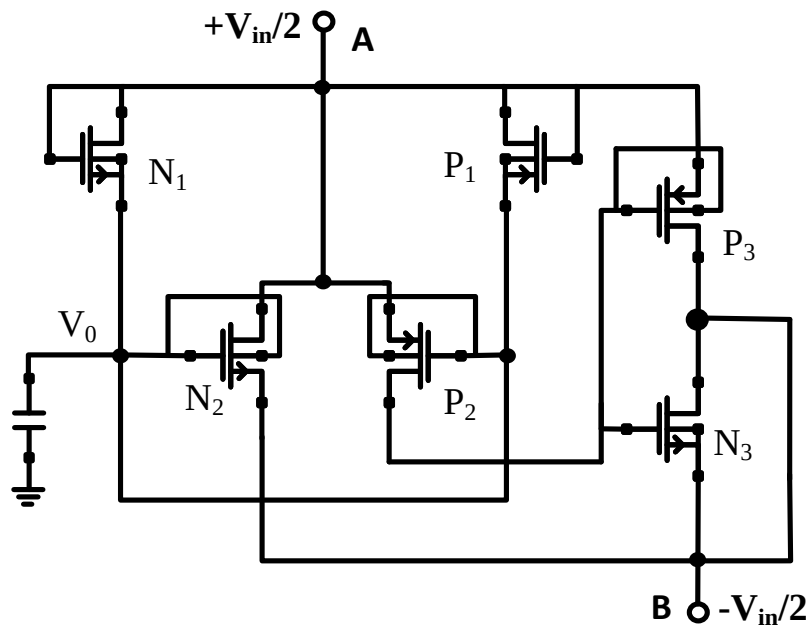
A floating, totally passive memristor emulator has been developed that uses MOSFETs (six numbers) and a capacitor and is based on the DTMOS- dynamic threshold MOSFET technique. The circuit was simulated using Cadence Virtuoso Spectre and GPDK 180nm CMOS technology. A thorough examination was conducted, encompassing its transient response, hysteresis behavior, and non-volatile memory features. The design was further tested against process corner fluctuations and at a wide temperature range to ensure its robustness. The emulator can operate at up to 10 MHz, making it ideal for high-frequency applications. Among its key features are its small size, low power consumption, and dynamic threshold capability, which improves switching performance. The physical configuration measures $56.725 \mu\text{m} \times 57.15 \mu\text{m}$. The proposed memristor emulator's practical relevance is proved by its use in analog circuit designs such as Colpitts chaotic oscillators, Chua's oscillator, and a Schmitt trigger. These examples demonstrate the emulator's flexibility and potential in sophisticated signal processing and neuromorphic devices.

3.3.1 Circuit diagram a passive floating C-MOS memristor

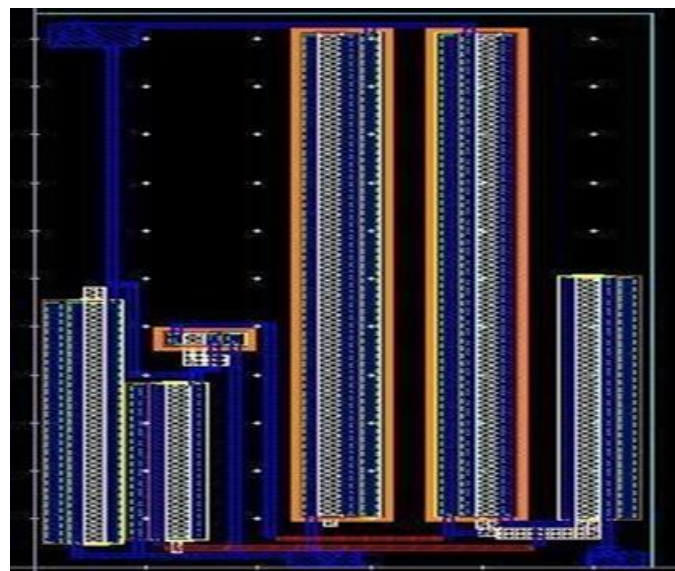
This study shows a memristor emulator circuit (Figure 3.21 (a)) that includes six MOSFETs and a single capacitor ($C = 5 \text{ pF}$). In the design, transistors P_1 and N_1 are designed as diode-connected elements, whereas P_2 and N_2 work together to simulate resistive behavior. Transistors P_3 and N_3 form an inverter, and their output supplies the bias voltage needed by transistor P_2 . This arrangement operates in a totally passive mode, which eliminates the requirement for an external bias voltage.

P_1 and N_1 function as diodes in the circuit because their gate and drain terminals are shorted. When the sinusoidal input signal voltage rises in a positive half cycle, the NMOS transistor N_1 becomes forward-biased, while P_1 remains reverse biased. These transistors are non-conductive until the input voltage surpasses about 0.7 V. Once this threshold voltage crosses, N_1 begins to conduct, allowing the capacitor to progressively charge. As current travels through the transistors and resistor (N_1 , N_2 , N_3 , and the resistor R), the total current through the resistor increases dramatically.

When the voltage peaks during the input's positive half-cycle, N_1 enters the saturation area. As the voltage falls from its peak, the capacitor begins to discharge via the N_3 source. When the voltage goes below 0.7 V, N_1 turns off and the discharge accelerates due to the high resistance channel. This discharge reproduces the waveform of the input signal.



(a)



(b)

Figure 3. 21 Circuit diagram of floating C-MOS memristor emulator (b) Layout of floating C-MOS memristor emulator circuit

In the input waveform's negative half-cycle, P_1 becomes forward biased and conducts. As a result, the capacitor is reverse charged along the path formed by P_1 , N_3 , and resistor R . When the negative voltage drops, the capacitor begins to discharge again. This constant charge-discharge cycle, which is coordinated with the input signal, generates the memristor's distinctive voltage-current (V-I) characteristics.

N_1 and P_1 's diode-like action is allowed by their diode-connected designs, which maintain them in the saturation area and allow them to function as small-signal resistors. The circuit's nonlinearity and the appearance of a pinched hysteresis loop demonstrate its memristive functionality. The W/L ratios of all MOSFETs used in this design are shown in Table 3.6.

The suggested emulator circuit, shown in Figure 3.21(b), has a silicon area of $56.725 \mu\text{m} \times 57.15 \mu\text{m}$, making it ideal for tiny integrated circuit implementations.

Table 3. 5 W/L Ratio of Transistor used in C-MOS memristor emulator circuit

MOSFETs	Type	W/L Ratio
N_1, N_3	NMOS	$25\mu\text{m}/1\mu\text{m}$
N_2	NMOS	$16\mu\text{m}/1\mu\text{m}$
P_1, P_3	PMOS	$50\mu\text{m}/1\mu\text{m}$
$P_2,$	PMOS	$1\mu\text{m}/1\mu\text{m}$

3.3.2 Simulation results of a passive floating C-MOS memristor

The performance of the proposed memristor emulator circuit was evaluated using the Cadence Virtuoso Spectre simulator and 180nm GPDK CMOS technology. Figure 3.22 (a) depicts the transient analysis of the output current in response to a sinusoidal input signal with a peak-to-peak value of 1.5V. The data clearly show classic zero-crossings at the sites where $V_{in} = 0$ and $I_{out} = 0$. Figure 3.22 (b) shows the hysteresis behavior at various input frequencies, including 10 kHz, 100 kHz, 500 kHz, 1 MHz, and 10 MHz, confirming the circuit's memristive nature as described in [46].

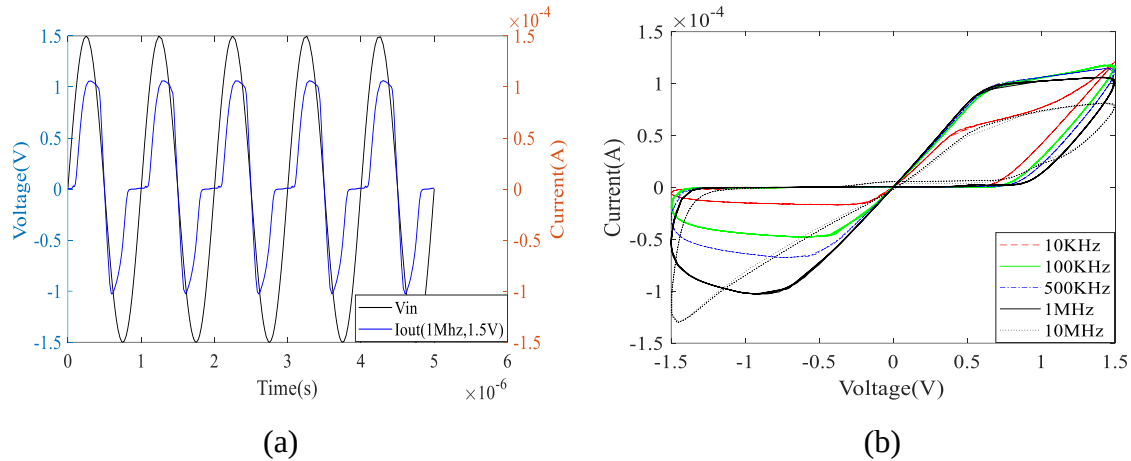


Figure 3. 22 (a) Transient analysis C-MOS memristor emulator circuit for the input signal with amplitude 1.5 V_{p-p} and 1 MHz frequency (b) PHL curve for C-MOS memristor emulator circuit for frequencies up to 10 MHz

Figure 3.23 (a) shows how the emulator's hysteresis loops change with different capacitance values ($C = 1\text{ pF}$, 2 pF , and 5 pF), illustrating that the output current is sensitive to capacitor values. The second key memristive characteristic, as described in [46], is seen in Figure 3.23 (b), where the memristive behavior is preserved while the product of frequency and capacitance remains constant, emphasizing the frequency-capacitance relationship.

Figure 3.32 illustrates the emulator's nonvolatile nature. Figures 3.33 and 3.34 analyze process variation and temperature effects, respectively, showing the circuit's robustness and reliability under a variety of operating situations

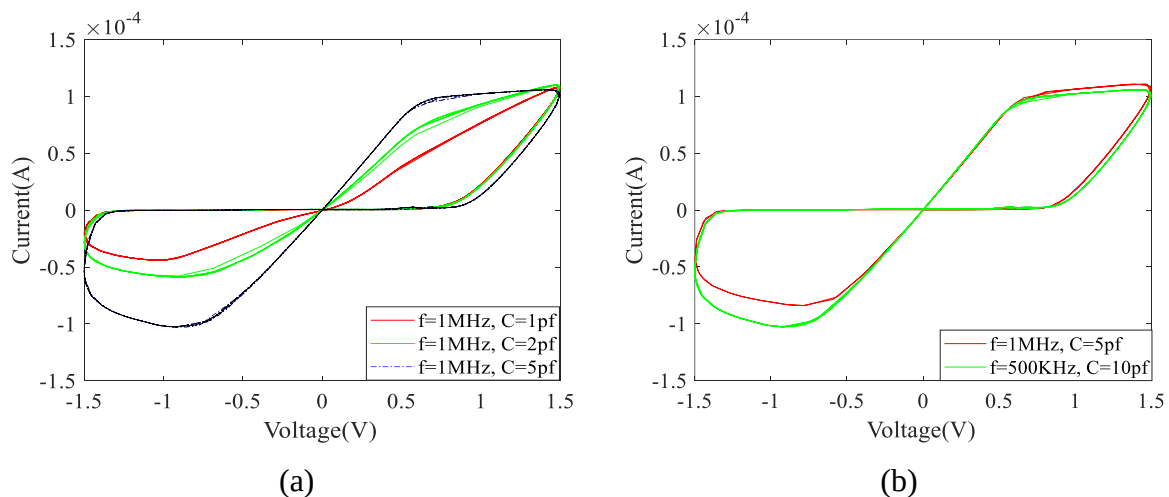


Figure 3. 23 (a) PH curve for C-MOS memristor emulator circuit for different capacitance value to show scalability (b) PH curve at various frequency and capacitances to observe ($f * C = \text{Constant}$) performance

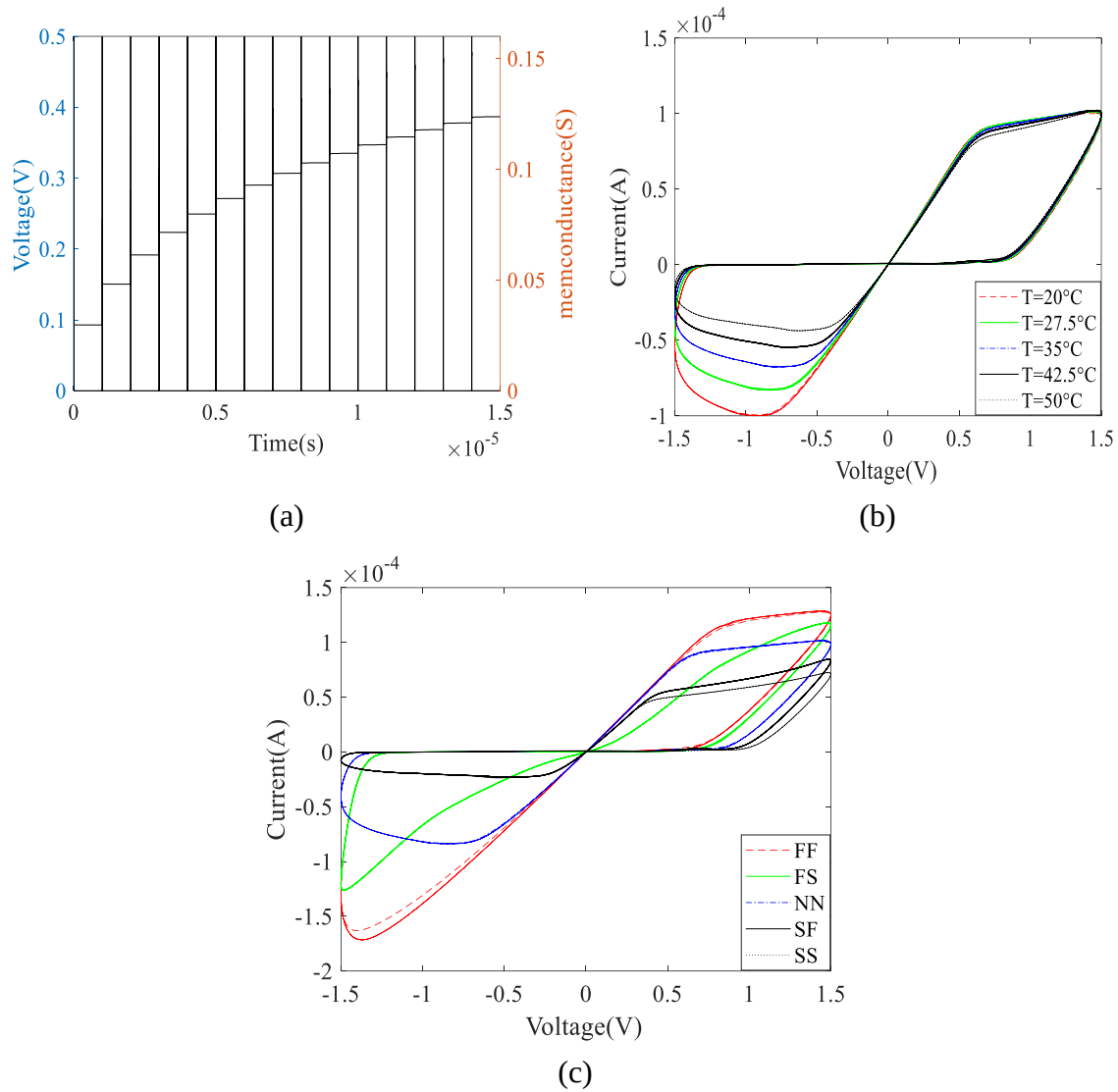


Figure 3. 24 (a) Non-volatile nature of C-MOS memristor emulator circuit (b) performance of C-MOS memristor emulator circuit at different temperature (20°C to 50°C) (c) Process corner analysis of C-MOS memristor emulator circuit

3.3.3 Application of a passive floating C-MOS memristor

To demonstrate the suggested memristor's practical utility, it was integrated into various resistor-based circuits, including a Schmitt trigger, a Colpitts chaotic oscillator, and Chua's oscillator. The proposed emulator effectively substituted the resistor in each application while retaining adequate functionality.

Figure 3.12 (a) illustrates the Schmitt trigger implementation, which employs an operational amplifier biased at ± 15 V DC and operated by a 250 Hz sinusoidal input signal with a 1 V peak-to-peak amplitude. A resistor of $R_1 = 20$ M Ω is incorporated. To assess threshold fluctuation, 1 V programming pulses at 1 kHz frequency were used. Figures 3.25 (a) and 3.25 (b) show the

transient response and the related hysteresis behavior. Schmitt triggers are widely employed in comparator circuits to generate clean digital outputs from analog inputs.

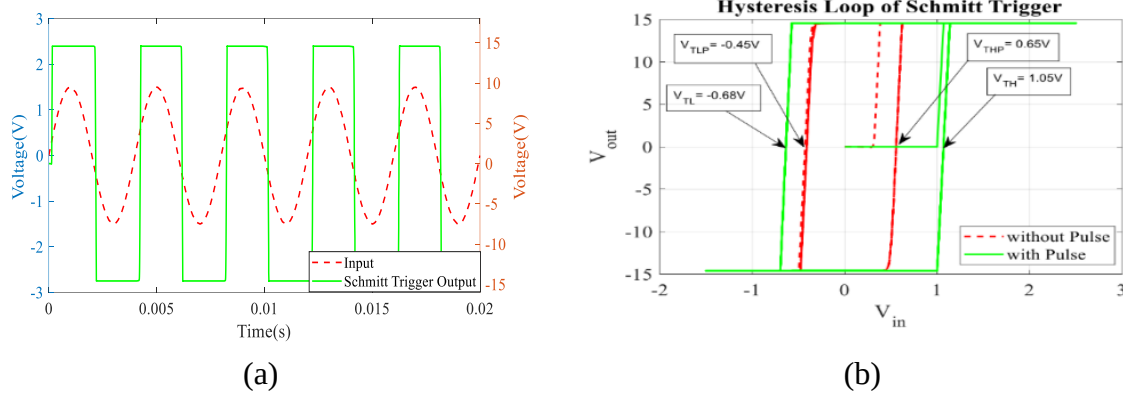


Figure 3. 25 (a) Square wave generation using Schmitt trigger circuit using memristor (b) hysteresis curve for Schmitt trigger circuit

The study contains an implementation of Chua's oscillator (Figure 3.26 (a)), which comprises inductors ($L_0 = 70$ mH, $L_1 = 7$ mH), capacitors ($C_0 = 1$ nF, $C_1 = 20$ nF), and a resistor $R_0 = 1$ M Ω . Figures 3.26 (b) and 3.26 (c) show details of the ensuing responses.

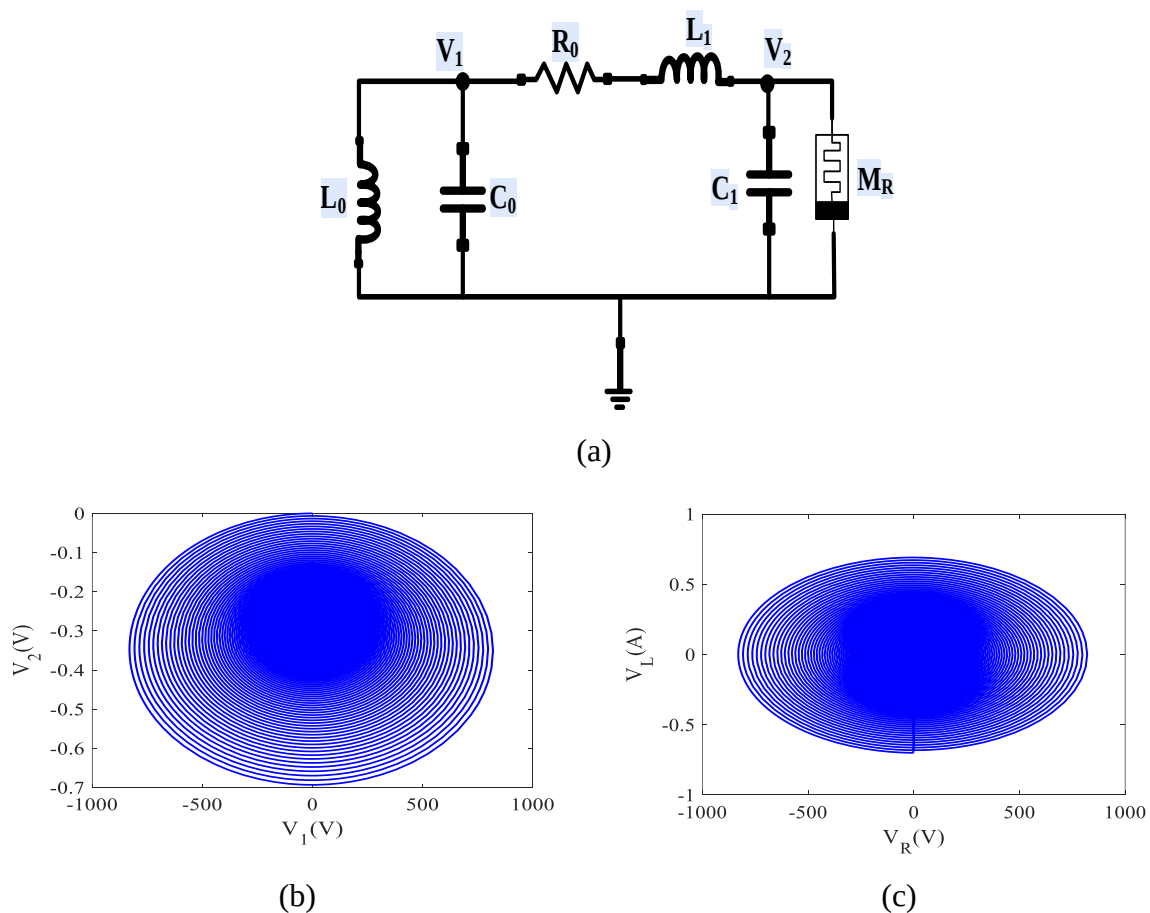


Figure 3. 26(a) Chua's Oscillator Circuit using memristor (b) Chua's oscillator circuit output for V_1 Vs V_2 (c) Chua's oscillator circuit for V_R Vs V_L

Finally, a detailed comparison was performed with previously published memristor emulator circuits [131][104][96][53][115][54][52][47][132], which included totally floating, partially floating, and grounded designs. The proposed emulator distinguishes itself by consuming no static power due to the lack of external bias. In the absence of input signals, power consumption is effectively zero. Table 3.7 presents a consolidated comparison.

Table 3.7 Comparison of C-MOS memristor emulator circuit with existing emulator circuit

Ref	Active Devices	Transistor Count	Passive Components Count	Memristor Type	Technology	Operating Frequency	Power Dissipation
[104]	DDCC-1	40	$R \rightarrow 2, C \rightarrow 1$	Grounded	35nm TSMC	1MHz	-NA-
[47]	-	3	$C \rightarrow 1$	Floating	180nm TSMC	13MHz	6.725nW
[52]	-	3	-	Both	180nm GPDK	20MHz 30MHz	zero
[96]	OTA-1	17	$C \rightarrow 1$	Grounded	180nm GPDK	1MHz	411.2 μ W
[131]	VDTA	16	$R \rightarrow 2, C \rightarrow 1$	Floating	180nm T SMC	50MHz	NA
[54]	-	16	$C \rightarrow 1$	Floating	180nm T SMC	Few Hz	8.015 μ W
[53]	FCS	6	$C \rightarrow 1$	Floating	180nm T SMC	10Hz	-NA-
[115]	-	4	$C \rightarrow 1$	Floating	180nm GPDK	3MHz	8.24 μ W
[132]	-	5	0	both	180nm GPDK	500MHz	zero
Proposed Work	-	6	$C \rightarrow 1$	Floating	180nm GPDK	10MHz	zero

3.4 Summary

This first describes a simple grounded memristor emulator that can operate in both grounded and floating versions. The circuit consists of a single MOSFET coupled with an R-C tank. Simulations are run in the Cadence Virtuoso Spectre environment, but the experimental prototype employs discrete components, especially the ALD1117 Dual P-channel enhancement-mode MOSFET and external resistor-capacitor elements. The proposed architecture can be implemented with either discrete components or nanometer-scale integrated circuit technology. The simulation and hardware results are consistent with the three key features of memristors, verifying the emulator's behavior across a wide range of frequencies and temperatures. This memristor emulator has several advantages over previous designs, including a streamlined and flexible structure, fewer active and passive components, operation at high frequencies up to 80 MHz, ultra-low dynamic power consumption of 7.751 pW, zero

static power, and a compact layout size of $1.586 \mu\text{m}^2$, making it suitable for integrated circuit fabrication. Its adaptability enables it to operate in both analog and digital systems. To demonstrate its practical utility, the emulator has been used to create a Schmitt trigger, a chaotic Colpitts oscillator, and an XOR logic gate. This design's key elements includes minimum circuit complexity, consistent and solid performance, capable of operating at high frequencies, extremely low power requirements, small silicon area. All of which make it an excellent choice for applications that require high-speed, low-power operation. However, the design has some limitations. It specifically requires external resistor and capacitor components, with the resistor being relatively large in value, typically on the order of several hundred kilo-ohms, which may not be optimal for all integration scenarios.

The second paper, an alternative approach memristor emulator circuit consists of only four transistors (N_1 , N_2 , N_3 , and P_1) with no external biasing. Because there is no external biasing, it is just passive. In comparison to other structures provided in the literature, this one is relatively simple. Some of them use existing blocks, such as multipliers, to achieve nonlinear behavior. The simulated beneficial results of the suggested circuit have been provided. This report also includes evaluations of process corners and temperature variations. This paper concludes with a demonstration of a simple memristor use as a low pass and high filter. In conclusion, all simulated results are acceptable and consistent with previous investigations. Because of its simple design, the proposed circuit will be quite useful in the future.

In the third study, an alternative technique of simulating a memristor circuit is discussed which is consisting of six MOSFETs and one capacitor with no external biasing. This memristor circuit is fully passive memristor and has a simpler design than existing published circuits. Simulations on the suggested circuit produced positive results. Furthermore, this study evaluates process corner and temperature variations, with detailed data. The practicality of this memristor emulator circuit is verified with a demonstration of a Colpitts chaotic oscillator and Chua's oscillator circuit. Additionally, an analysis and demonstration of a Schmitt trigger circuit as a regenerative comparator circuit are provided. To summarize, the simulated results are not only satisfactory, but also compatible with previous studies. The suggested circuit's simple construction shows great potential for future applications.

Chapter 4

A Memcapacitor Emulator Circuit and its Applications

This chapter explained the design of a memcapacitor emulator model which consists of only single multioutput transconductance amplifier (MO-OTA) under 45nm GPDK technology using Cadence Virtuoso Spectre (CVS) tool. The experimental verification is also explained using discrete components and existing MOOTA IC LM13700. The different analysis such as transient, PHL, process voltage temperature (PVT), and monte carlo analysis are also discussed. The applicability of this emulator circuit ranging from mathematical operation to neuromorphic adaptive learning are also presented in this chapter.

A memcapacitor emulator has been created using a single multi-output operational transconductance amplifier (MO-OTA). This design was simulated with Cadence Virtuoso and 45 nm GPDK technology. For experimental validation, the LM13700 operational transconductance IC was used. The circuit performs well up to 4 MHz and consumes only 272.5 μ W of power. The proposed model was used to study transient response and hysteresis behavior at various frequencies. Monte Carlo simulations proved its reliability, and the design's robustness was tested against process-voltage-temperature (PVT) changes. The emulator is versatile in a variety of applications, including basic mathematical operations such as integration and differentiation, as well as neuromorphic adaptive learning systems.

4.1 Introduction

Nonvolatile memory elements can be implemented using common nanoscale memory devices called as mem-elements, which include memristors, memcapacitors, and meminductors.

Leon Chua devised the memristor as the fourth circuit element [4], [5]. He proposed a mathematical theory for memristors, creating a link between flux and charge, which are key circuit variables.

Since its theoretical inception in 1971, mem-elements have undergone substantial research. Interestingly, Hewlett Packard (HP) was the first company to physically realize a memristor in 2008 [6]. In 2009, M. Di Ventra suggested an enlarged memristor theory, including memcapacitors and meminductors [39]. Memristors are defined by the charge-flux relationship, while memcapacitors are defined by the charge-voltage relationship. A meminductor's mathematical description focuses on the flux-current coupling. Pinched hysteresis and zero crossing behavior are crucial to the functionality of all three memelements [133]. Mem-elements offer high speed, low-energy dissipation and adaptable circuit designs.

Pershin and Di Ventra described the key attributes of memory elements in Figure 4.1 [134]. They classified mem-element qualities as specialized or general.

The mem-element domain saw a surge in memristor emulator design [49], [52]–[54], [95], [102], [114], [132], [135]–[139]. This was followed by applications in various electronic circuits [23], [91], [99], [100], [140]–[146], and eventually fabricated memristor models [6], [49], [147]–[149]. Several research groups developed higher-order elements, including meminductors [81], [150]–[154] and memcapacitors [8], [66], [67], [69], [70], [74], [86]–[88], [141], [155]–[177]. There are mathematical and PSPICE models for memcapacitor emulators [68], [178], as well as potential applications in memory devices, chaotic circuits, and oscillators [85], [179], [180].

Although a memristor can be physically implemented as a separate component, the manufacture of a memcapacitor is typically limited due to its complexity. Designing a memcapacitor emulator is a necessary first step towards realizing a memcapacitor. Developing an emulator makes sense for multiple reasons. Emulators are reliable, energy-efficient, and compatible with modern circuit designs. Active circuit-based memcapacitor emulators meet the parameters described above. Several studies [8], [66], [67], [69], [70], [72], [74], [86]–[88], [141], [155]–[158], [160]–[177], [181] have documented several types of memcapacitor emulators based on active circuit elements. There are two types of memcapacitor emulators: mutator-based (with a memristor) [8], [66], [70], [85], [141], [155], [157], [158] and non-mutator-based (without a memristor) [67], [69], [74], [86], [156], [159]–[161], [165], [170], [172], [173], [175]. Reference [85] depicts a universal charge-controlled memristor emulator. It contains three CCII, one analog multiplier, and five passive elements. This emulator can use the same topology to implement all three memory elements. In addition, Y.V. Persin [155] suggests using a microcontroller to command a digital potentiometer to emulate memcapacitors

and meminductors. Wang et al. [8] proposed a memcapacitor emulator with a mutator structure. The circuit has twelve resistors, two capacitors, an LDR, LED, diode, and five OPAMPs. The circuit has multiple active and passive components and lacked electronic flexibility. B. Biolek [157] modified the concept from [8] to convert the memristor to a memcapacitor, taking into account parasitic effects. Yu et al. [141] and Shah et al. [158] published designs for floating memcapacitor emulators using mutators. However, the emulators included both passive and active circuitry.

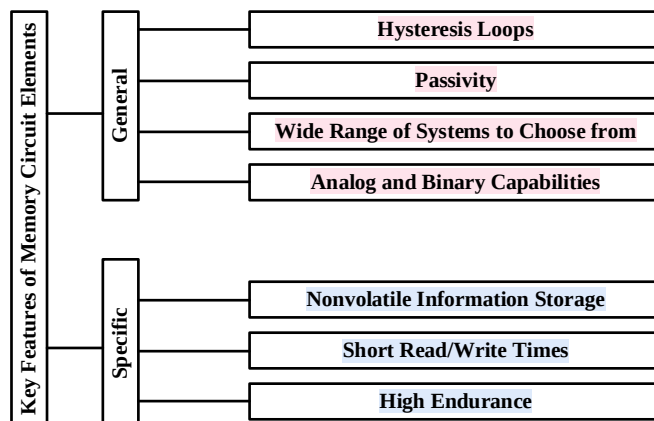


Figure 4. 1 Key features of memelements [134]

Konal et al. [156] suggested a voltage differential current conveyor (VDCC)-based memcapacitor emulator with electrically controllable characteristics. Yesil and Babacan [72] developed a CCII- second-generation current conveyor and OTA- operational transconductance amplifier based memcapacitor emulator circuit. This circuit may be regulated using discrete circuit elements and has tight hysteresis in the charge-voltage relationship, resulting in a powerful memory effect. However, the suggested structure has restricted uses due to its grounded nature. Vista and Ranjan [162] proposed a memcapacitor emulator using a DVCCTA. The emulator circuit is grounded and simple in design. Hosbas et al. proposed a voltage differencing transconductance amplifier (VDTA)-based memcapacitor emulator [66].

The memcapacitor emulator circuit includes a restricted hysteresis loop that may be adjusted electronically. However, its structure limits its potential applications. Fouda and Radwan designed a grounded memcapacitor emulator circuit with four OPAMPs, a multiplier, and a single current-controlled source [67]. Romero et al. [70] presented a memcapacitor emulator circuit based on the Miller effect. Petrovi C [170] presented a memcapacitor emulator circuit using a VDTA device and two grounded capacitors. The circuit was tested in a simulated

environment using commercially available components. The circuit was grounded and electronically controllable. Vista and Ranjan suggested a floating capacitor-emulating circuit [74]. The suggested circuit is electronically tunable. The memcapacitor emulator circuit was used to demonstrate an adaptive learning circuit. However, no experimental validation for the work was provided in [74]. Singh and Rai introduced a VDCC-based floating memcapacitor emulator circuit [173]. The circuit was replicated using a single VDCC, capacitor, and memristor. Sah et al. [69] designed a floating memcapacitor emulator with readily available components. There was one multiplier circuit and two OPAMPs used. Experimental findings were obtained by building the circuit on a breadboard. The circuit was not electronically tunable. Sharma et al. [172] developed a memcapacitor emulator circuit that can operate in both grounded and floating modes. The circuit consists of two second-generation current conveyors (CCII)s and a multiplier circuit that functions as a memristor and memcapacitor. This circuit lacks electronic tunability, despite having both incremental and decremental actions. Bhardwaj et al. [168] presented a universal memelement emulator using a single CCII, OTA, resistor, and two capacitors. Although the circuit is simple and extensible, there is no experimental validation provided in this study. Bhardwaj and Srivastava proposed a grounded charge-controlled memcapacitor emulator consisting of one VDCC, one OTA, two capacitors, and a resistor [169]. The circuit proposed in the paper lacks a multiplier circuit. The circuit can be electronically adjustable. The memcapacitor circuit has four AD844s, one OPAMP, a varactor diode, six resistors, and two capacitors [87]. This circuit is quite complex and consumes a significant amount of energy due to the vast number of passive components. Zheng et al. [86] proposed a universal interface for memristors, memcapacitors, and meminductors. The universal construction contains four AD844s, a varactor diode, two capacitors, and two resistors, which constitute a memcapacitor emulator circuit. The circuits employed multiple components due to the work's universal structure [87][86]. Wang et al. used a real memristor to create a floating memcapacitor emulator circuit [175]. The circuit comprised three AD844s, three passive components, and a memristor. The circuit design has been successfully simulated and experimentally validated.

Biolek et al. [165] presented a floating memcapacitor emulator with various active and passive components. Gur et al. proposed an easy MO-OTA-based floating memcapacitor emulator circuit in [163]. It has two MO-OTAs, four transistors, a capacitor, and a resistor. This circuit simulates a memcapacitor and may be adjusted electronically. However, no experimental verification has been done. Tatovi C. and Petrovi C. [174] proposed a floating memcapacitor

emulator circuit using one VDCC, two MOSFETs, and two capacitors. Although the circuit is adjustable, it was only tested in simulation mode.

This work presents and validates a memcapacitor emulator model based on a single MOOTA. The presented model effectiveness is verified by modeling in Cadence Virtuoso utilizing 45 nm GPDK technology and experimental verification with the LM13700 operational transconductance amplifier integrated circuit. The analysis covers key performance features such as frequency response, power consumption, transient behavior, hysteresis, and robustness to Monte Carlo and PVT fluctuations. The emulator's adaptability is highlighted, with possible applications in mathematical operations and neuromorphic adaptive learning. The suggested memristor emulator circuit simulates frequencies up to 4 MHz using GPDK technology and consumes around 272.5 μW of power. This work is supported by mathematical analysis, simulations, hardware implementation, and validation. The key features of the presented memcapacitor emulator circuit are;

- The proposed memcapacitor emulator contains a single MO-OTA with two capacitors and one resistor.
- In comparison to existing circuits, it boasts a more area-efficient design.
- The proposed emulator is simple to integrate with other circuits and devices, making it ideal for building potential applications.
- The suggested emulator does not require a multiplier or integrator circuit.

Table 4.2 presents a comparative examination of the important features. The work presents many studies, including transient, PVT, Monte-Carlo, and non-volatility analysis. Experimental validation was carried out with the existing components (LM13700, a resistor, and capacitors). The memcapacitor emulator circuit has been used to accomplish several applications, including adaptive learning and mathematical operations like differentiation and integration.

Section 4.2 introduces the mathematical model and notion of the proposed memcapacitor emulator. Section 4.3 describes the simulation and hardware validation of the memcapacitor emulator. Section 4.4 demonstrates many applications of the proposed memcapacitor emulator, including adaptive learning circuits, differentiators, and integrators. Section 4.5 summarizes the benefits of the proposed memcapacitor emulator design.

4.2 Design and Theory of Proposed Memcapacitor Emulator

4.2.1 Memcapacitor Theory

The four basic passive circuit elements—resistor, capacitor, inductor, and memristor—are fundamentally characterized by the relationships among the core electrical quantities: voltage, current, charge, and flux. Here, flux is obtained by integrating the applied voltage, while charge results from integrating the current passing through a component. Alongside these, memcapacitors and meminductors are also categorized as passive elements. By incorporating these extended passive devices, it becomes possible to define new derived quantities, such as resistivity (ρ), which is the integral of flux, and conductance (σ), which is the integral of charge. Specifically, a memcapacitor establishes a relationship between flux and the integrated charge (conductance), whereas a meminductor links charge to the integrated flux (resistivity) [182]. The respective integral expressions for current, voltage, charge, and flux are defined accordingly.

$$q(t) = \int I(t)dt, \varphi = \int V(t)dt, \sigma = \int q(t)dt, \rho = \int \varphi(t)dt \quad 4.1$$

Taking (4.1) into account, Equation (4.2) can be written as:

$$\frac{d\varphi}{dt} = \frac{d\varphi}{d\sigma} \frac{d\sigma}{dt} \quad 4.2$$

Here, $\frac{d\varphi}{dt} = V(t)$ and $\frac{d\sigma}{dt} = q(t)$. Considering these definitions, inverse memcapacitance can be defined by rewriting (4.2) as:

$$C_M^{-1} = D_M = \frac{V(t)}{q(t)} = \frac{d\varphi}{d\sigma} \quad 4.3$$

According to [182], [69], the inverse of the memcapacitance is given by:

$$C_M^{-1}(t) = D_M = \frac{d\varphi}{d\sigma} = \frac{V_{IN}(t)}{q(t)} = D_{M,\min} + K \int q(t)dt \quad 4.4$$

4.2.2 Building blocks and their characteristics

Specialized devices, such as operational transconductance amplifiers (OTAs) and its extended variation, multi-output OTAs, are frequently used in electronic circuits. These components have a wider bandwidth and a higher dynamic range than standard operational amplifiers. In both OTA and MO-OTA setups, the non-inverting $V_P(+)$ and inverting $V_N(-)$ terminals accept

voltage signals and produce a current output, effectively making them voltage-controlled current sources or voltage-to-current converters.

Because of their input-output nature, these amplifiers often have high input and output impedance, allowing them to handle greater voltages while drawing minimum current. Figure 4.2 (a) illustrates the circuit symbol for a MO-OTA, and Equation 4.5 expresses the mathematical link between its terminals.

$$I_P = I_N = 0, I_{p1} = -I_{n1} = -I_{n2} = g_m(V_P - V_N) = g_m \cdot V_{IN} \quad 4.5$$

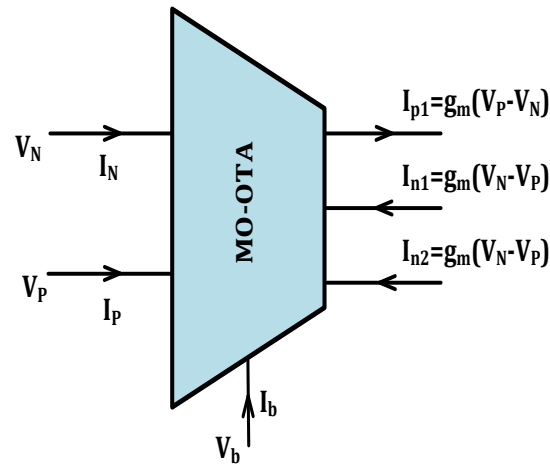
The characteristic equation and transconductance gain of MO-OTA are given in equations 4.6 and 4.7, respectively.

$$\begin{bmatrix} I_{p1} \\ I_{n1} \\ I_{n2} \end{bmatrix} = \begin{bmatrix} g_m & -g_m \\ -g_m & g_m \\ -g_m & g_m \end{bmatrix} \begin{bmatrix} V_P \\ V_N \end{bmatrix} \quad 4.6$$

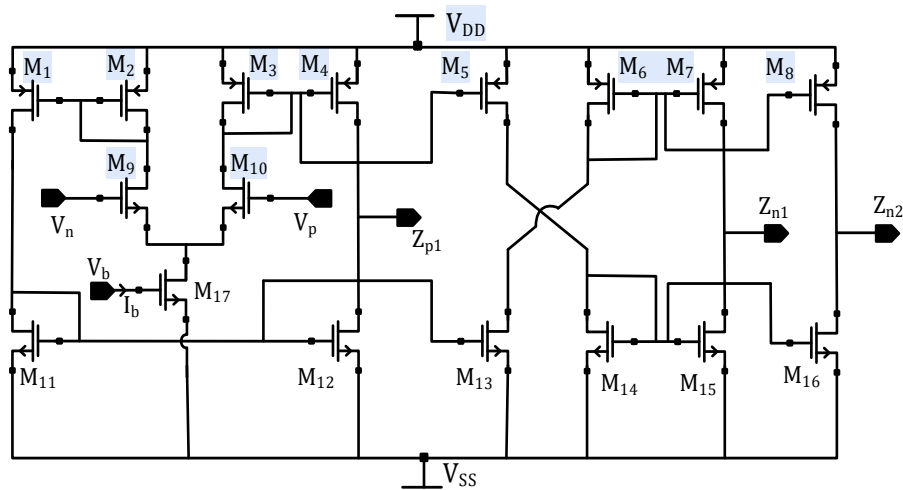
$$g_m = K(V_b - V_{SS} - V_{TH}) \quad 4.7$$

The constant K is illustrated as $K = B\mu_n C_{OX} \sqrt{\frac{1}{2} \left(\frac{W}{L}\right)_{M17} \left(\frac{W}{L}\right)_{M9}}$. The parameters are defined as, B is the current mirror ratio between transistors $M_{2,3}$ and $M_{1,4}$. μ_n is the carrier mobility (in $\text{m}^2/\text{V}\cdot\text{s}$), C_{OX} is the gate-oxide capacitance per unit area, and V_{TH} is the threshold voltage. The bias current I_b electronically adjusts the transconductance g_m , which is further regulated by the biasing voltage V_b .

Figure 4.2 (b) shows the internal design of the MO-OTA, consisting of seventeen transistors identified from ($M_1 - M_{17}$). The transistor M_{17} serves as a current source, providing the bias current I_b required for electronic circuit tuning. The W/L (width-to-length) ratios of these transistors are shown in Table 4.1.



(a)



(b)

Figure 4. 2 (a) Circuit symbol of MO-OTA (b) Internal structure of MO-OTA

Table 4. 1 W/L ratio of used Transistors

Transistors	Type	W/L Ratio
M_1, M_{4-8}	PMOS	360 nm/45 nm
M_{17}	NMOS	180 nm/90 nm
M_{11-16}	NMOS	120 nm/45 nm
M_{9-10}	NMOS	180 nm/45 nm
M_{2-3}	PMOS	200nm/45 nm

4.2.3 Building blocks and their characteristics

The proposed floating memcapacitor emulator is given in Figure 4.3. The proposed circuit comprises only a single MO-OTA (multiple output OTA), a single resistor, and two grounded capacitors.

For the proposed design, the inverse memcapacitance equation of memcapacitor emulator can be obtained using the characteristic equation 5 of MO-OTA, and taking $g_{m1} = g_m$. The voltage at the non-inverting terminal of MO-OTA which is equal to the voltage across the capacitor (C_1), can be written as

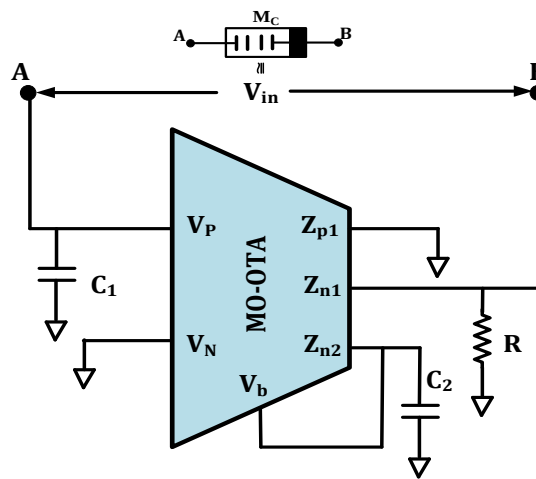


Figure 4. 3 Proposed memcapacitor emulator using a single MO-OTA

$$V_A = V_{C1} = \frac{1}{C_1} \int I_{IN}(t) dt = \frac{q(t)}{C_1} \quad 4.8$$

The voltage at the terminal B is equal to the potential across the resistor R. It can be written as equation 4.9

$$V_B = I_{n1}R = g_m(V_N - V_P)R = -g_m V_P R = -g_m \frac{q(t)}{C_1} R \quad 4.9$$

The biasing voltage of the MO-OTA is equal to the voltage across the capacitor C_2 , which can be adjusted by the varying W/L of the transistor M_{17} . The bias voltage can be written as equation 4.10

$$V_b = \frac{1}{C_2} \int I_{n2}(t) dt \quad 4.10$$

Using the equation 4.5 and equation 4.8, biasing voltage can be written as equation 4.11.

$$V_b = -\frac{g_m}{C_1 C_2} \int q(t) dt \quad 4.11$$

Substituting the value of biasing voltage V_{bias} from 4.11 into equation 4.7, the transconductance g_m can be written as equation 4.12

$$g_m = K \left(\frac{-g_m}{C_1 C_2} \int q(t) dt - V_{SS} - V_{TH} \right) \quad 4.12$$

$$g_m \left(1 + K \frac{1}{C_1 C_2} \int q(t) dt \right) = -(V_{SS} + V_{TH}) \quad 4.13$$

$$g_m = \frac{-(V_{SS} + V_{TH})}{\left(1 + K \frac{1}{C_1 C_2} \int q(t) dt \right)} \quad 4.14$$

$$g_m = \frac{K^2 (V_{SS} + V_{TH})}{C_1 C_2} \int q(t) dt - K (V_{SS} + V_{TH}) \quad 4.15$$

The applied input voltage to the memcapacitor emulator will be equal to the potential difference between terminals A and B. Hence, the input voltage V_{IN} can be written as equation 4.16

$$V_{IN} = V_A - V_B = \frac{q(t)}{C_1} + g_m \frac{q(t)}{C_1} R \quad 4.16$$

Substituting the equation 4.12 in equation 4.16, the inverse memcapacitance can be written as equation 4.17

$$C_M^{-1} = \frac{V_{IN}}{q(t)} = \frac{K^2 (V_{SS} + V_{TH}) R}{C_1^2 \cdot C_2} \int q(t) dt + \left(\frac{1 - K (V_{SS} + V_{TH}) R}{C_1} \right) \quad 4.17$$

The above-mentioned equation 4.17 consists of two terms, the first term being dynamic (time-dependent) and the second term being static (time-independent).

4.3 Simulation an Experimental Results

The proposed memcapacitor emulator circuit, shown in Figure 4.3, was simulated with the Cadence Virtuoso Spectre simulator and 45 nm GPDK technology. NI-Multisim was used to simulate the design utilizing discrete components, such as three LM13700 OTA ICs, one 200Ω resistor, six 10KΩ resistors (used for biasing various OTA IC pins), and two capacitors ($C_1 = 300\text{pF}$ and $C_2 = 47\text{nF}$). The same arrangement was created and tested on a breadboard in the lab. A digital storage oscilloscope was used to observe the hysteresis loop, and the circuit reached a maximum working frequency of 5.2 MHz under experimental conditions.

To simulate, a simple setup was utilized using a single MO-OTA, a resistor $R = 20K\Omega$, and two capacitors $C_1 = 1pF$ and $C_2 = 20pF$. Table 4.1 shows the width-to-length (W/L) ratios of the transistors employed in this design. Figure 4.4 depicts the memcapacitor emulator's transient response to a sinusoidal input signal of $0.7V_{p-p}$ peak-to-peak at a frequency of 100 kHz. Furthermore, Figure 4.5 shows the circuit's pinched hysteresis characteristics over a frequency range of 20KHz to 4MHz.

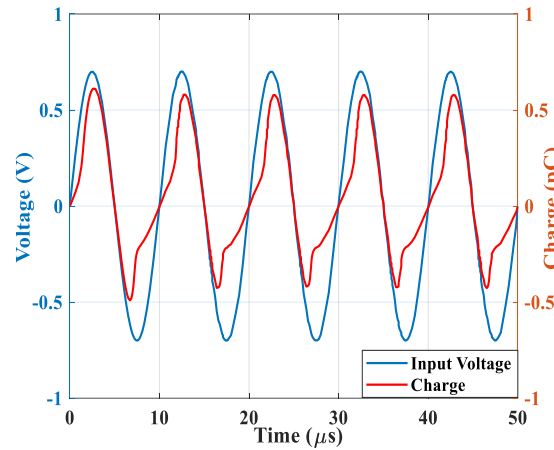


Figure 4. 4 Transient waveform of applied input sinusoidal signal (V_{IN}) and Charge $q(t)$ with the amplitude of $0.7 V_{p-p}$ and frequency of 100 KHz

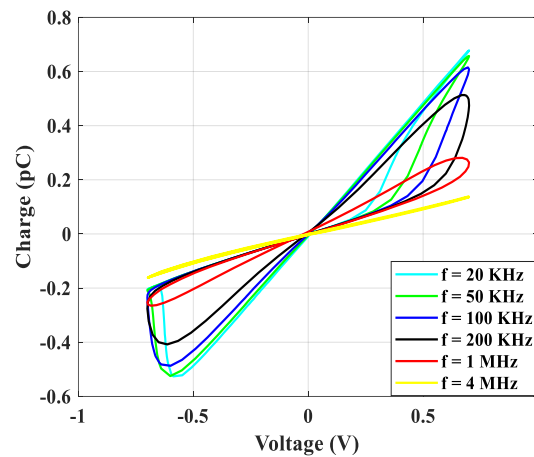


Figure 4. 5 Pinched hysteresis curve for the different frequencies 20 KHz - 4 MHz

Figures 4.6, 4.7, and 4.8 show the pinched hysteresis behavior and transient responses of the proposed memcapacitor emulator, emphasizing the effect of various passive devices on circuit performance. Figure 4.6 shows the effect of changing the capacitance C_1 between 1 pF and 9 pF. Increasing C_1 leads to a higher stored charge. A small shift in the pinching point is detected, revealing imperfections in the emulator behavior.

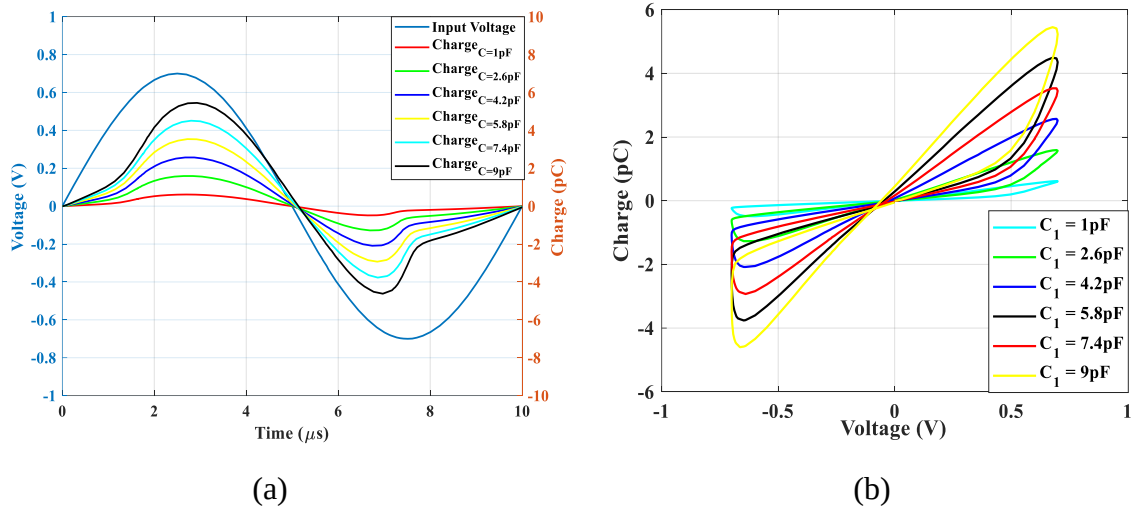


Figure 4. 6 (a) Transient and (b) hysteresis curve for capacitance C_1 (1 pF-9 pF)

Figure 4.7 illustrates how changing the capacitance C_2 from 10 pF to 90 pF impacts the output. Unlike C_1 , altering C_2 has negligible impact on the charge and keeps the pinching properties consistent. Figure 4.8 shows how resistance R , ranging from 10 k Ω to 90 k Ω , affects the circuit. The simulation demonstrates that the charge held by the memcapacitor is sensitive to the resistance value.

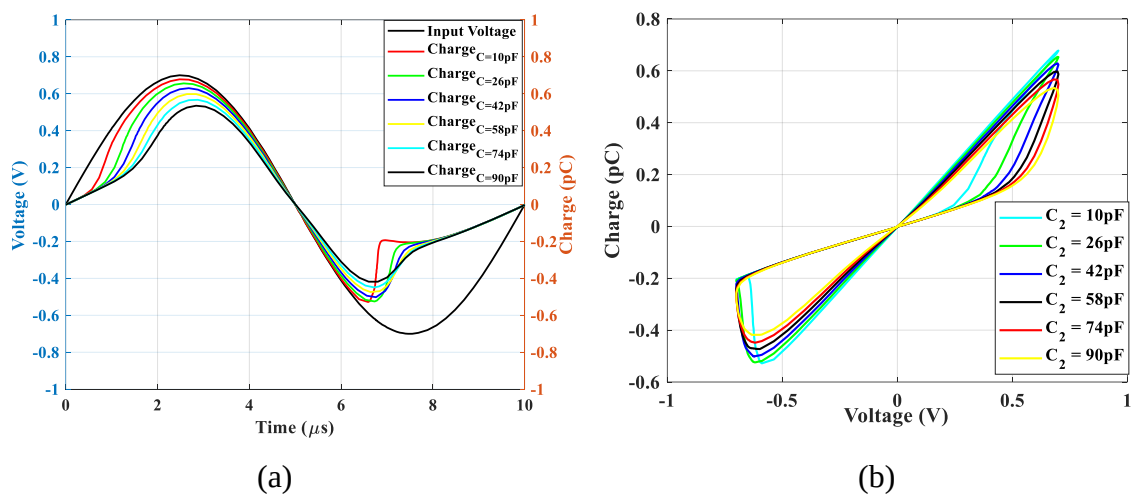


Figure 4. 7 (a) Transient and (b) hysteresis curve for capacitance C_2 (10 pF-90 pF)

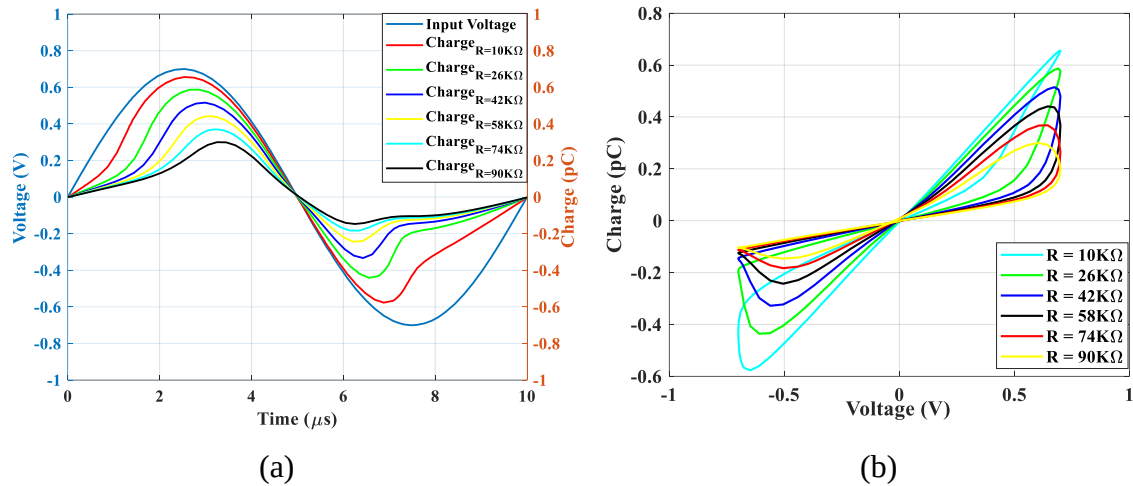


Figure 4. 8 (a)Transient and (b) hysteresis curve for Resistance R (10 k Ω -90 k Ω)

Figures 4.9 (a) and 4.9(b) show that the circuit operates stable over a temperature range of -100 $^{\circ}\text{C}$ to +110 $^{\circ}\text{C}$ and across multiple process corners, including Fast-Fast (FF), Slow-Fast (SF), Fast-Slow (FS), Slow-Slow (SS), and Typical (TT).

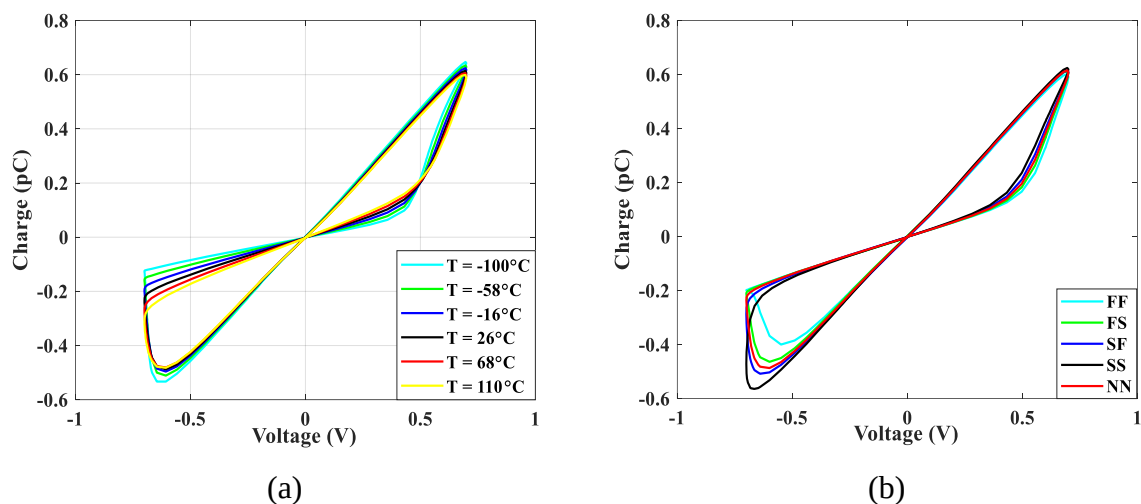


Figure 4. 9 (a) Hysteresis curve at different temperatures (-100 $^{\circ}\text{C}$ -100 $^{\circ}\text{C}$) (b) Hysteresis curve at different corners (FF, FS, SF, SS and NN)

Figure 4.10 illustrates the suggested design's nonvolatile characteristics. To evaluate this feature, a square wave input with two voltage levels (0 V and 200 mV), 1 μ s period, and 50% duty cycle was used. The output showed a gradual charge increment, demonstrating the memcapacitor's memory retention capabilities. Figures 4.11(a) and 4.11(b) confirm the non-volatile response. Unlike typical capacitors, this emulator maintains charge after pulse application. The charge steadily builds at the start of each pulse and eventually reaches saturation (see Figure 4.11), indicating good charge-holding performance.

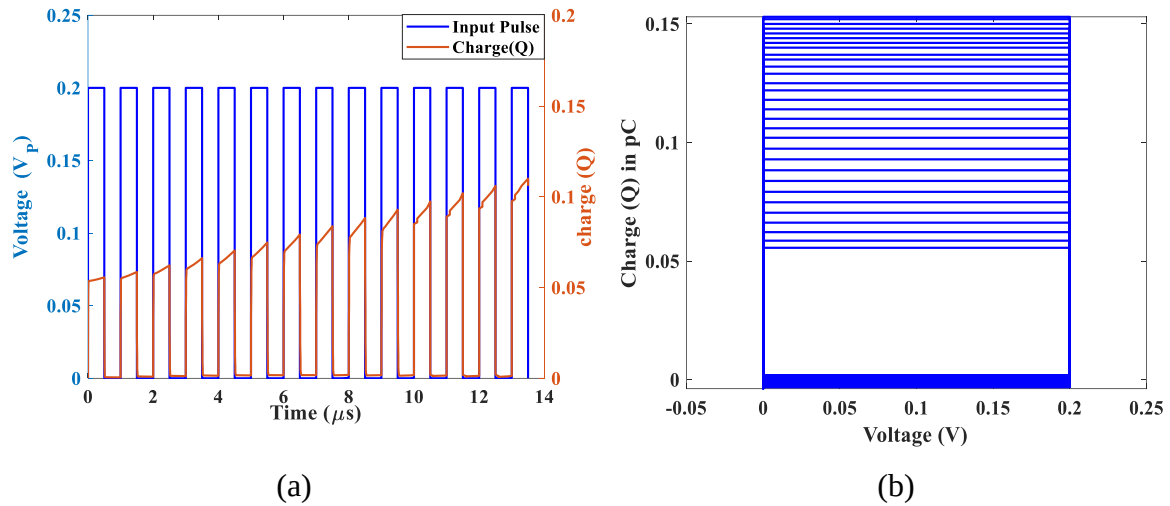


Figure 4. 10 (a) Non-volatile nature of proposed memcapacitor emulator circuit (b) Charge $q(t)$ levels at a different time of pulse

The suggested memcapacitor's energy density (E_d) was determined using the formula:

$$E_d = \frac{1}{2} \times C_M \times V^2 = q_{max} \times V \quad 4.18$$

where C_M is the memcapacitance, q_{max} is the peak stored charge, and V is the applied voltage.

For a 0.2 V input pulse and maximum charge of 0.175 pC, the energy density is:

$$E_d = 0.2 \times 0.175 \text{ pC} = 0.0175 \text{ pJ/cm}^3$$

The power density (P_d) calculated during a 1 μ s period is:

$$P_d = \frac{E_d}{T} = 0.0175 \text{ } \mu\text{W/cm}^3$$

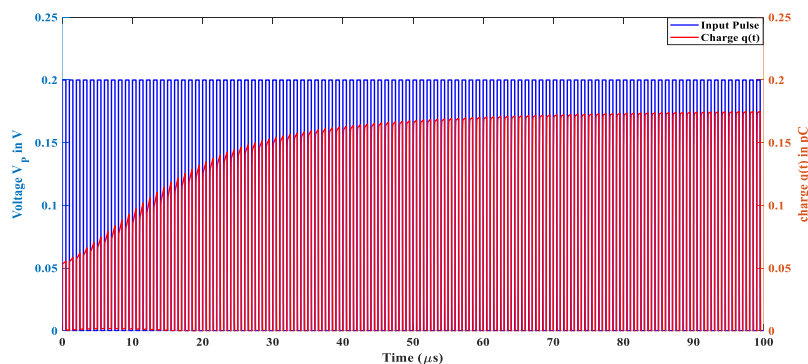
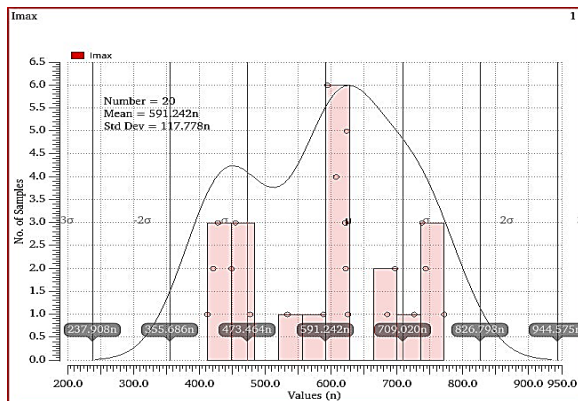


Figure 4. 11 The charging capacity of the proposed memcapacitor emulator for 100 μ s

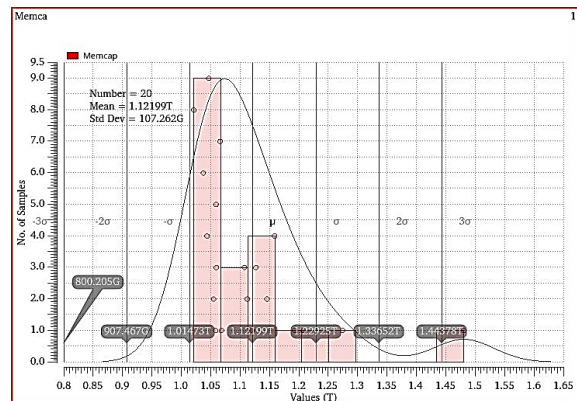
Figure 4.12 depicts the results of a 200-run Monte Carlo analysis to assess the circuit's robustness. This simulation evaluated key performance indicators such as maximum charge

($Q_{\max}$), power consumption, peak output current ($I_{\max}$), maximum input voltage ($V_{\max}$), and memory capacitance.

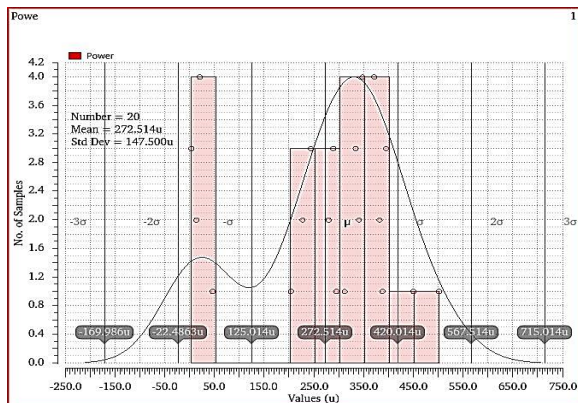
Figure 4.12(a) shows the distribution of output current (in nA), figure 4.12(b) shows variations in memcapacitance, figure 4.12 (c) shows power distribution (in μW), figure 4.12(d) shows distribution of Charge (in fC), figure 4.12 (e) shows variation of input voltage (in mV). The study reveals that all important parameters are within a 3σ range of their respective means, demonstrating consistent circuit functioning.



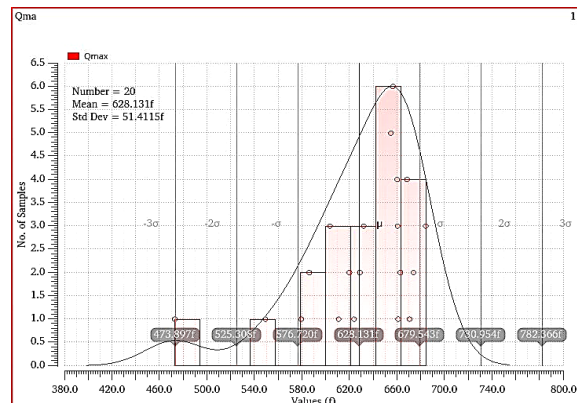
(a)



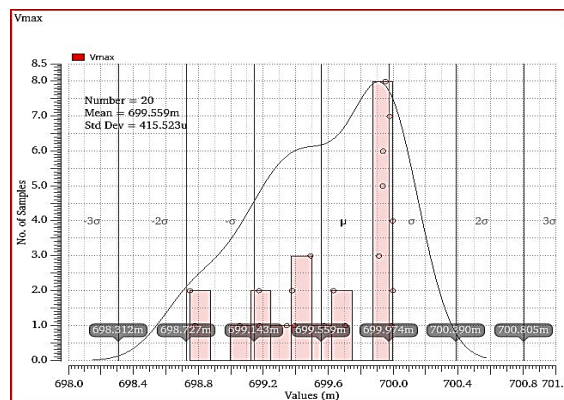
(b)



(c)



(d)



(e)

Figure 4. 12 Monte Carlo simulation results for various parameters ($I_{\max}$, M_C , P , Q , and $V_{\max}$) for memcapacitor emulator parameters (a) Monte Carlo simulation for current in nA (b) Monte Carlo simulation for memcapacitance (M_C) (c) Monte Carlo simulation for power (P) consumption in μW (d) Monte Carlo simulation for maximum Charge (Q) in fC (e) Monte Carlo simulation for maximum input voltage in mV

Figure 4.13 includes a long-term reliability evaluation that simulates 200 years of operational aging using parameters like $V_{\max}$, $I_{\max}$, $Q_{\max}$, and memcapacitance. The findings indicate fairly little performance decline over time.

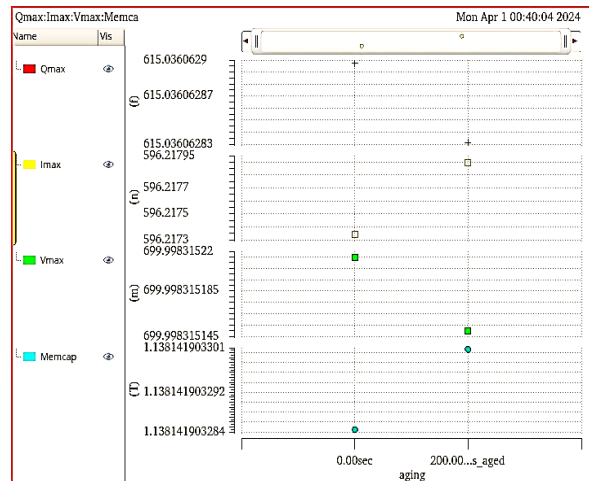
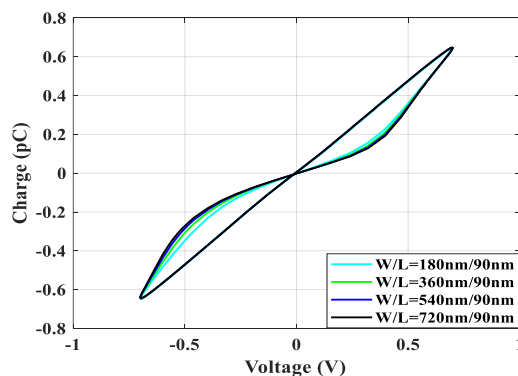
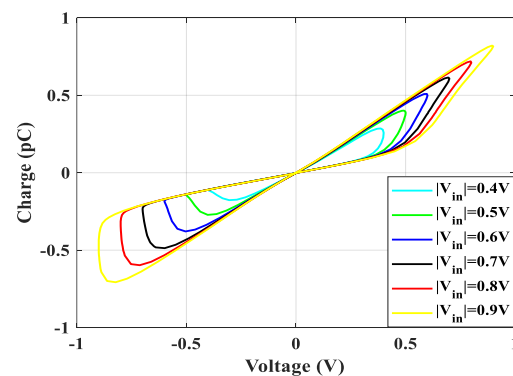


Figure 4. 13 Reliability Analysis of the proposed memcapacitor emulator with 200 years of aging

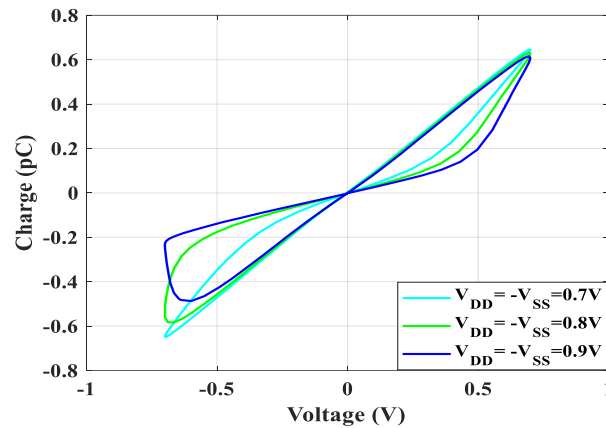
Figure 4.14 shows how input signal amplitude, bias voltages, and electrical tunability affect circuit behavior. Figure 4.14(a) shows the influence of transistor width (W) modification and tuning characteristics. Figure 4.14 (b) depicts hysteresis curves for input amplitudes of 0.4 V to 0.9 V. Figure 4.14c shows hysteresis fluctuations with biasing voltages ranging from ± 0.7 to ± 0.9 V.



(a)



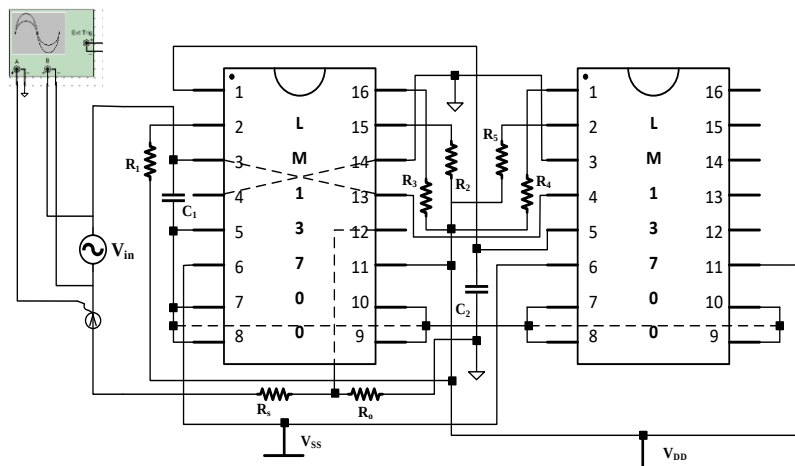
(b)



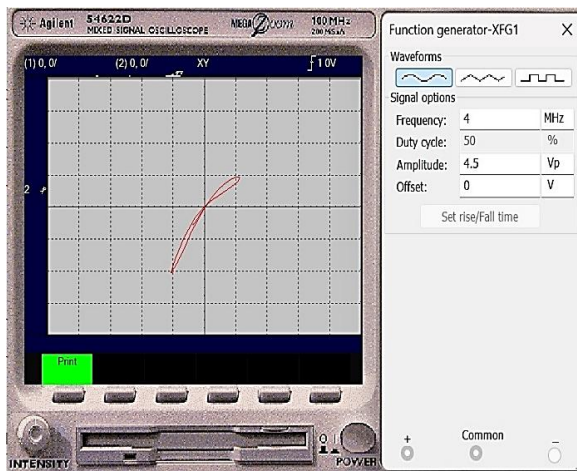
(c)

Figure 4. 14(a) Hysteresis curve for different W/L ratio of the transistor (b) Hysteresis curve for different input voltage amplitudes (c) Hysteresis curve for different biasing voltages

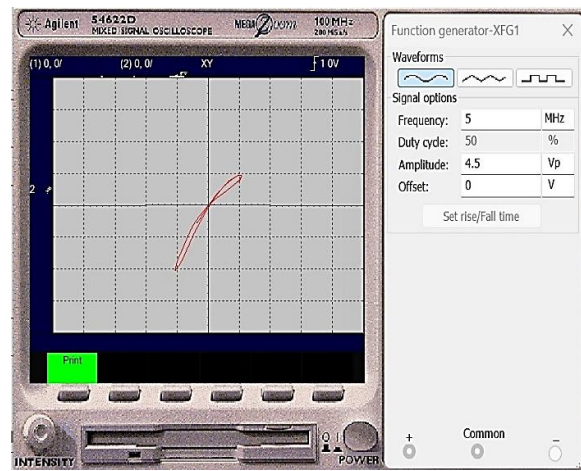
The practical implementation of the circuit was further tested with NI-Multisim. The system consisted of an LM13700 OTA IC, five 10 k Ω resistors (R_1 - R_5), one 1 k Ω resistor (R_0), a series resistor $R_S = 1.5$ k Ω , and two capacitors ($C_1 = 300$ pF and $C_2 = 47$ nF). The MO-OTA structure was created using three OTAs, and the circuit configuration is shown in Figure 4.15(a). Figures 4.15(b) and 4.15(c) demonstrate the simulation results for sinusoidal inputs at 4 and 5 MHz, respectively.



(a)



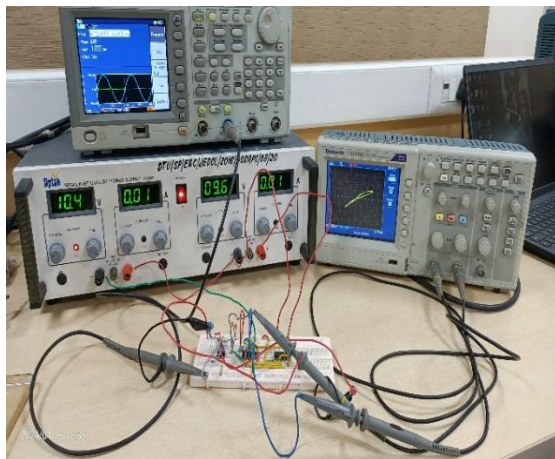
(b)



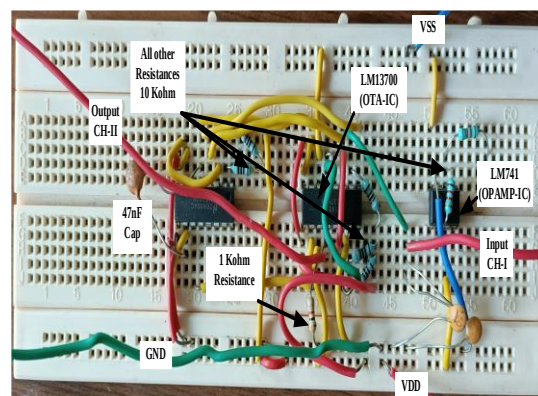
(c)

Figure 4. 15 (a) Wiring diagram of proposed memcapacitor for Multisim simulation (b) Hysteresis curve at 4 MHz (c) Hysteresis curve at 5 MHz

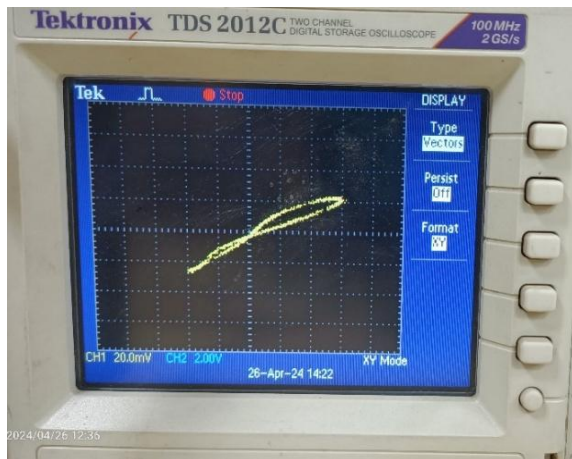
Experimental validation using the identical arrangement on a breadboard confirmed the simulation results. Figures 4.16 (a-d) illustrate the measured hysteresis curves, which closely matched those in the simulation. The arrangement demonstrated functioning up to 5.2 MHz, which confirmed the performance indicated in NI-Multisim simulations.



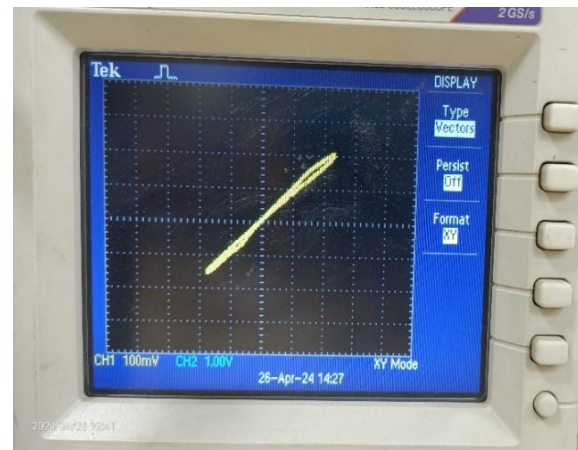
(a)



(b)



(c)

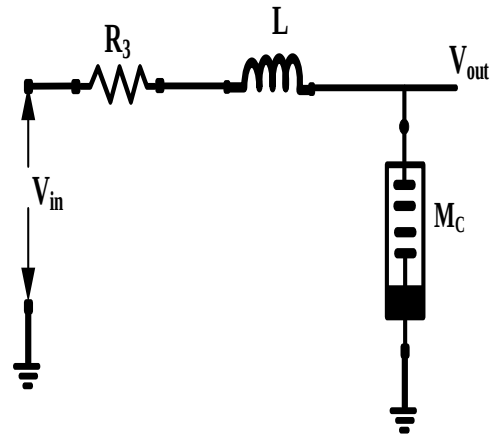


(d)

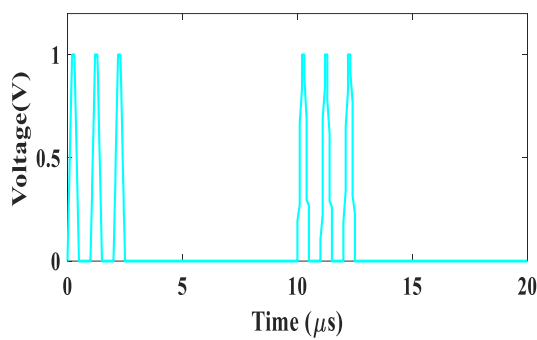
Figure 4. 16 (a) Complete experimental setup (b) Breadboard circuit (c) Hysteresis curve at 4.75 MHz (d) Hysteresis curve at 5.2 MHz

4.4 Application of the Proposed Memcapacitor Emulator

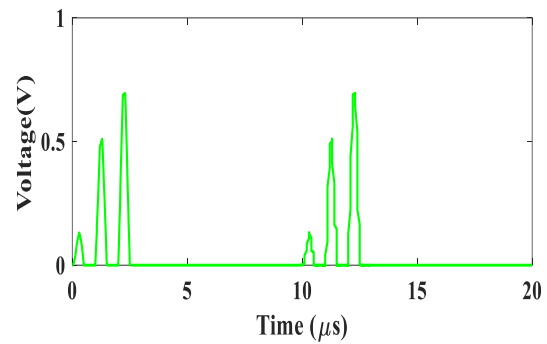
The proposed memcapacitor emulator has been used to construct adaptive neuromorphic architectures, such as the amoeba-inspired circuit [23], [53], [138], [142], [183]–[185]. Figure 4.17 (a) shows the adaptive response of the system using a circuit with a resistor ($R = 1 \text{ k}\Omega$), an inductor ($L = 1 \text{ }\mu\text{H}$), and the proposed memcapacitor. Figure 4.17 illustrates the adaptive learning circuit incorporating the proposed memcapacitor and its corresponding response to repeated input stimuli. The applied voltage pulses, representing temperature variations, are shown in Fig. 4.17 (b), while the output response, interpreted as locomotive speed, is depicted in Fig. 4.17 (c). It can be observed that the response amplitude increases with successive input pulses, indicating a cumulative effect due to the memory property of the memcapacitor. This behavior is consistent with previously reported studies[74], [186], [169], where repeated stimulation leads to enhanced system response. It is important to note that this phenomenon reflects history-dependent adaptive behavior rather than anticipatory action, as the system response is governed by the internal state evolution of the memcapacitive element.



(a)



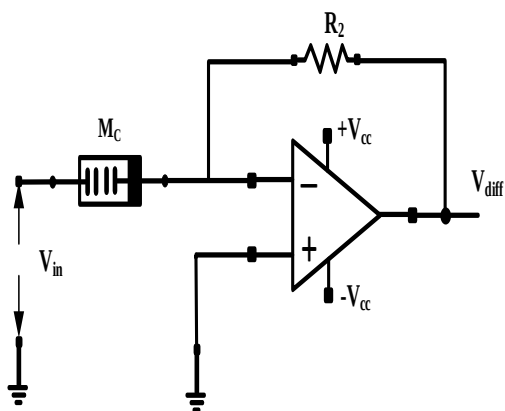
(b)



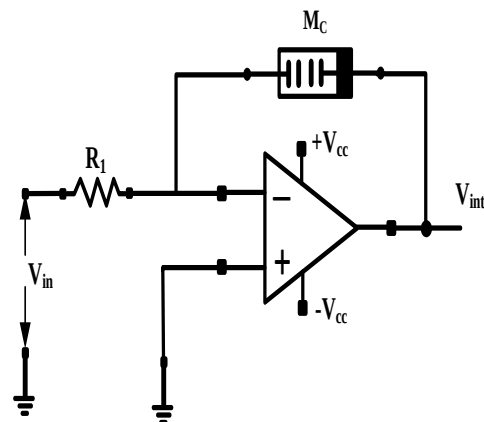
(c)

Figure 4. 17 (a) Adaptive learning circuit with proposed memcapacitor (b) Temperature variation in terms of voltage (c) locomotive speed response

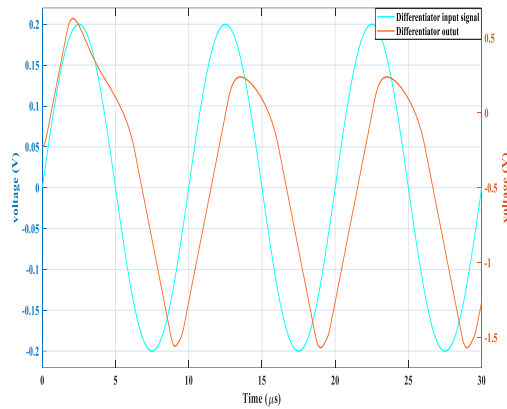
To demonstrate the emulator's adaptability, it has also been integrated into differentiator and integrator circuits, substituting the standard capacitor with the suggested memcapacitor, as illustrated in Figures 4.18 (a) and 4.18 (b). These circuits use an operational amplifier (Op-Amp) with resistors: $R = 1 \text{ k}\Omega$ for the integrator and $R = 80 \text{ k}\Omega$ for the differentiator.



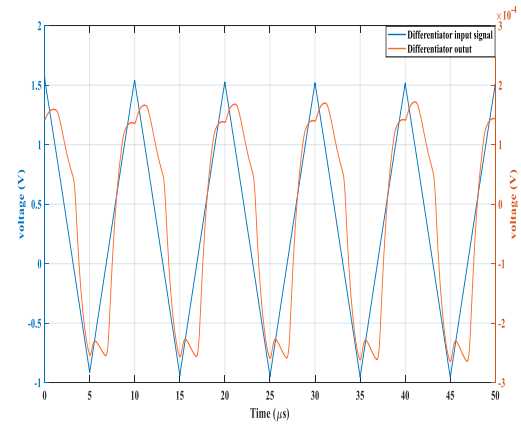
(a)



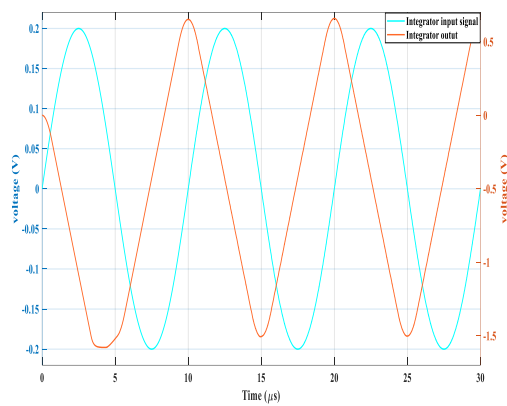
(b)



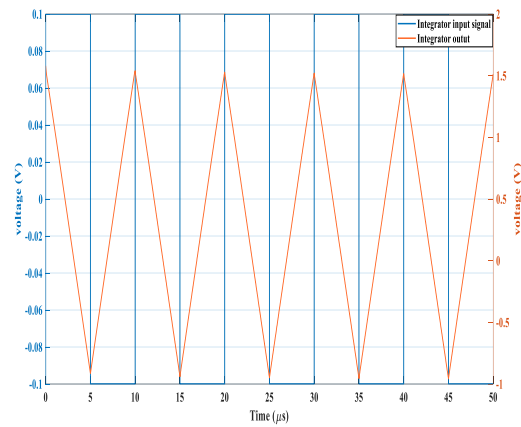
(c)



(d)



(e)



(f)

Figure 4. 18 (a) Op-AMP differentiator circuit using memcapacitor (b) Op-AMP intergrator circuit using memcapacitor (c-d) Response of differentiator circuit with input sinusoidal and ramp signal respectively (e-f) Response of integrator circuit with input sinusoidal and ramp signal respectively

Figures 4.18 (c-f) show the matching outputs from the differentiator and integrator. Both circuits were tested with a 200 mV sinusoidal input signal at a frequency of 100 kHz. The differentiator circuit generates an output that lags the input by 90°, whereas the integrator produces an output that leads the input by 90°, demonstrating proper phase behavior.

When a square wave signal with peak-to-peak voltage of 200 mV ($V_o = -100$ mV, $V_i = +100$ mV), period $T = 10$ μ s, and 50% duty cycle is applied to the integrator, it produces a ramp output. Applying this ramp signal to the differentiator results in a reconstructed square wave at the output. These findings demonstrate that the proposed memcapacitor emulator is well-suited for real-time implementations, such as adaptive learning circuits and analog computing applications that employ operational amplifiers.

The effect of parallel combination of the memcapacitors have been shown in Figure 4.19 and it is observed that charge value is increasing as the number of memcapacitors in parallel.

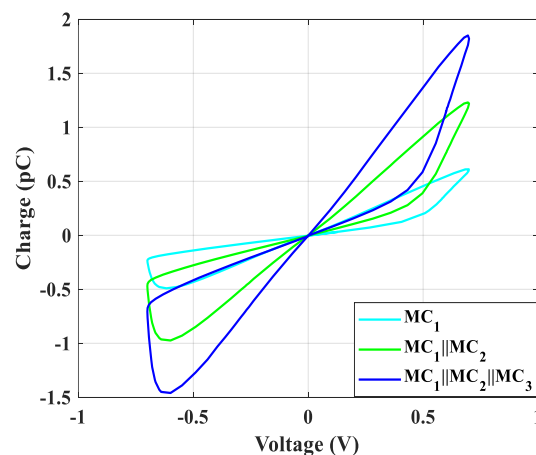


Figure 4. 19 Effect on charge with the parallel combination of memcapacitors

4.5 Comparison and Discussion

Tables 4.2 and 4.3 present a comparative analysis of many previously reported memcapacitor emulator designs [69], [85], [155]–[158], [163]. Factors considered in the comparison include the types of active and passive components, circuit configuration, technology employed, operating frequency, mutator-based design, and electrical tunability.

Many of the earlier implementations [85], [87], [157], [158], [160], [163] used multipliers in their designs, whereas the proposed emulator does not require one. Furthermore, several of the referenced systems [85], [155], [157], [158] use mutator structures to produce memcapacitive behavior, which the current design completely avoids in favor of a more streamlined and efficient approach.

While most previous works are limited to kilohertz-range operating frequencies, the suggested floating memcapacitor emulator can operate up to 4 MHz. It is built with two grounded capacitors, a single resistor, and a multi-output operational transconductance amplifier (MO-OTA) as the active component, resulting in low power consumption in the microwatt range and simplicity of construction.

Table 4. 2 Comparison of the Proposed Model with Existing Memcapacitor Emulators based on Design

Ref No.	Publication Year	Multiplier Used	Existing Blocks Used	Passive/ Active Component Count	Mutator Based
---------	------------------	-----------------	----------------------	---------------------------------	---------------

[85]	2019	Yes	CCII - 5, OPAMP - 1	R - 5, C -2	Yes
[157]	2010	Yes	CCII - 2	R - 1, C -1	Yes
[158]	2013	Yes	CCII - 2, OPAMP - 3	R - 4, C -2	Yes
[87]	2020	Yes	CCII - 4, OPAMP - 1	R - 6, C - 2, VD-1	No
[69]	2014	No	OP-AMP - 2	R - 1, C - 2, VD-1	No
[155]	2010	No	OTA - 1	R - 2, C -1	Yes
[156]	2021	Yes	MO-OTA - 2	R - 2, C -2	No
[163]	2023	Yes	MO-OTA - 2	R - 1, C - 1, T-4	No
Proposed Work	2024	No	MO-OTA - 1	R - 1, C -2	No

Table 4.3 Comparison of the Proposed Model with Existing Memcapacitor Emulators based on Performance

Ref No.	Experiment/ Simulation	Floating /Grounded	Technology	Frequency	Electronic Tunable
[85]	both	both	-	5 kHz	No
[157]	simulation	Floating	-	1 Hz	No
[158]	Simulation	Floating	-	900 Hz	No
[87]	Simulation	Floating	-	8 KHz	No
[69]	Both	Floating	-	25 Hz	No
[155]	simulation	Floating	-	5 Hz	No
[156]	simulation	Floating	-	10 Hz	Yes
[163]	simulation	Floating	-	20 KHz	Yes
Proposed Work	both	Floating	45 nm GPDK	4 MHz	Yes

4.6 Summary

This chapter introduces a novel model for designing charge-controlled memcapacitors. We propose a floating memcapacitor consisting of two grounded capacitors, one resistor, and one active MO-OTA block. The proposed memcapacitor model has several advantages, including a simple construction with few active and passive parts, freedom from mutator circuit constraints, higher operating frequency range (in the megahertz range), floating nature for easier integration, electrical tunability via MO-OTA bias voltage, and freedom from multiplier

or integrator constraints. The practicality of the proposed memcapacitor design was proven by simulations using Cadence Virtuoso and 45nm GPDK technology.

The proposed design is viable, as evidenced by strong agreement between the mathematical model, simulation, and experimental data. The proposed memcapacitor paradigm is suitable for real-time applications, as demonstrated by a simple design of an adaptive learning circuit using memcapacitors and Op-Amps. The circuit's simplicity enables compatibility with other circuits, potentially increasing the adoption of mem-system-based applications in the near future. In conclusion, the developed memcapacitor emulator has promising features such as configurable capacitance, low power consumption, and stable performance during PVT changes. Nonlinear charge storage and hysteresis make this capacitor ideal for advanced applications like neuromorphic computing, artificial synapses, and adaptive learning circuits.

Chapter 5

Meminductor Emulators using only MOSFETs and its Applications

This chapter explain a compact grounded meminductor emulator (MIE) using only five MOSFETs (three NMOS, two PMOS). It employs an active gyrator topology with one NMOS acting as a MOS capacitor to provide memory and inductive behavior, eliminating passive components. The design maintains a stable response up to 200 MHz and is validated through various analyses including non-volatility, thermal stability, tunability, Monte Carlo, and process corners. Implemented in 90 nm GPDK CMOS using Cadence Virtuoso with 2.52 mW static and 3.23 mW dynamic power, an area of 80.5 μm^2 . Its use in adaptive learning and chaotic circuits shows practical potential. A simple grounded meminductor emulator (MIE) based on a MOSFET configuration is also discussed in this chapter which consist of six MOSFETs and two capacitors. The proposed circuit may efficiently create pinched hysteresis loops (PHL) at frequencies up to 100 KHz.

5.1. MOSFET-Meminductor Emulator Circuit with Experimental Validation and Application in Adaptive Learning and Chua's oscillator circuit

A grounded meminductor emulator (MIE) with only five metal-oxide-semiconductor field-effect transistor (MOSFET) is proposed. Out of the five MOSFETs, three NMOS transistors and two PMOS transistors is proposed. The architecture uses an active gyrator topology in which one MOSFET (NMOS), which serves as a MOS capacitor, displays memory behavior and inductive properties as well. The MOS capacitor in the circuit eliminates the need for passive components. The proposed emulator maintains a stable frequency response up to 200 MHz. Its performance robustness has been validated through extensive analysis such as non-volatility test, thermal stability, tunability, Monte Carlo simulations, and process corner evaluations. Simulations are conducted using 90 nm GPDK CMOS technology on the Cadence Virtuoso Spectre (CVS) tool. The design achieves a static power consumption of 2.52 mW, a dynamic power of 3.23 mW, and occupies a silicon area of 80.5 μm^2 . Practical implementations

in adaptive learning systems and chaotic oscillator circuit further demonstrate its applicability in well-known nonlinear circuits. A comparative assessment with existing meminductor emulators highlight the proposed meminductor emulator's superior efficiency and compactness.

5.1.1. Introduction

The idea of memelements — memristors, memcapacitors, and meminductors —represents a paradigm shift in circuit theory. These elements have their theoretical basis in Chua's pioneering work on the memristor (hypothesized as the fourth fundamental circuit element) [4]. Though proposed in 1971, the physical realization of a memristor was carried out in Hewlett-Packard laboratory by Strukov et al. [6] in 2008. HRL Laboratories [187] presented the first working memristor array built on a CMOS chip. Even though memristors have been commercialized by KNOWM, their operational parameters are quite demanding [188].

Researchers have worked on several memristor models and emulators in order to postulate and examine a range of practical uses [52], [103], [132], [137], [189]. Once the memristor was conceptualized, efforts were made to realise memcapacitors [181], [190] and meminductors in an attempt to complete the trinity of memory-based elements propounded by Pershin and Di Ventra [190] and formalize the meminductor by its dependence on the time integral of current with its hysteretic flux-current relationship. These three memory elements have characteristics of non-volatility [191] and a constricted hysteresis loop. In spite of having immense theoretical potential, the practical implementation of a physical meminductor is still considered a difficult task. Hence, research articles describe a variety of meminductor emulator circuits that are used to physically investigate the dynamics of meminductive devices in the electronic world. The MIE circuits are broadly divided into two categories such as mutator-based MIEs [76], [77], [83], [87], [152], [153], [155], [173], [192]–[196] and MIEs without a mutator [41], [79]–[82], [150], [166], [197]–[204]. Early emulator designs used mutator circuits to convert memristive dynamics into meminductive properties. MIEs are further categorized as (including mutator or mutator less) MIEs with analog multiplier block [152], [153], [173], [192], [196], [204]–[207], MIEs with active building blocks such as operational transconductance amplifiers (OTAs) [79], [154], [195], [203], [208], field programmable analog arrays (FPAA) [204], voltage differential current conveyor (VDCC) [173], [195], current conveyor transconductance amplifiers (CCTAs) [200], operational amplifiers (OA) [81], [201], current difference buffered amplifier (CDBA) [154], [209], [210], voltage differencing transconductance amplifiers (VDTAs) [152],

[211], current difference transconductance amplifiers [208] voltage differential gain amplifier (VDGA) [210], and current conveyors (CCII)s [196], floating [41], [80], [87], [152], [153], [173], [192], [193], [195], [207] or grounded [77], [152], [155], [196], [203]–[206] MIEs, and universal emulators [85], [164], [166], [212]. Memelements have diversified applications such as, memristors in neuromorphic circuits [186], [213]–[215], programmable analog circuits [16], adaptive filters [18], and chaotic circuits [85]. Similarly, meminductor emulators find applications in many fields of applied sciences, such as, analog circuits [83], chaotic circuits [205], [206], [216]–[220], biological synaptic plasticity [193]–[195], [213], data encryption [202], [207], meminductor crossbars [214], [215], adaptive learning circuits [18], [209], and analog computing architectures [83], [186]. In chaos engineering [11], [216]–[223], meminductors have found applications in double-scroll attractors [224] and neuronal firing models [212], [225]. The previously designed meminductor circuits have high complexity since they have been conceptualized either by using analog multiplier blocks or active building blocks (ABBs) to achieve nonlinearity. The frequency performance of most of these emulators is restricted to kHz or low MHz range. Further, most of the designs that use active building blocks rely heavily on either active or passive components. The purpose of this work is to provide a meminductor emulator that has only five MOSFETs and presents a very simple architecture based on the concept of a gyrator circuit. The proposed emulator offers electronic tunability and excellent high-frequency performance (up to 200 MHz) with applications in chaos circuits and adaptive learning circuits. The key features of the proposed MIE are:

1. It has only five MOSFETs (three NMOS and two PMOS).
2. It is an area-efficient circuit with a circuit layout area of 80.5 μm^2 .
3. Its straightforward architecture reduces complexity, enabling easier implementation in practical systems.
4. The power consumption of the proposed MIE is 2.52 mW - static power and 3.23 mW - dynamic power.
5. The operating frequency of the proposed MIE is up to 200 MHz.

A comparative analysis of key characteristics is given Tables 2 and 3. To highlight the robustness of the emulator design, transient analysis, Process-Voltage-Temperature (PVT) analysis, Monte-Carlo analysis, thermal stability analysis, and nonvolatility analysis have been presented in this work. Experimental validation has also been performed using existing ICs of NMOS and PMOS arrays (ALD1116 and ALD1117).

2

Section 5.1.2 and 5.1.3 describes the mathematical theory and concept of the proposed meminductor emulator. Section 5.1.4 presents the simulation and hardware validation of the meminductor emulator. Section 5.1.5 showcases different applications, namely, adaptive learning circuits, chaos (Chua's oscillator) circuit. A comparative study of existing meminductor emulators also discussed in Section 5.1.6. The work is concluded by highlighting the advantages of the proposed meminductor emulator design in Section 6.

5.1.2 Design and Theory of Proposed Meminductor Emulator

5.1.2.1. Theory of Meminductor

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A meminductor emulator is a nonlinear inductor whose inductance depends on the history of the current passing through it, making it a memory element similar to the memristor. The voltage-current relationship governing the dynamics of a meminductor is

$$V(t) = L(x, I) \frac{dI(t)}{dt} \quad 5.1$$

33

where, $V(t)$ is the voltage across the meminductor, $I(t)$ is the current through it, and $L(x, I)$ is the state-dependent inductance. The internal state x evolves according to the equation

$$\frac{dx}{dt} = f(x, I) \quad 5.2$$

The above mentioned equation indicates that the inductance depends on both the instantaneous current and the historical state of the system. A meminductor would exhibit hysteresis in the flux-current relationship, where the magnetic flux given by the equation is

$$\varphi(t) = \int_0^t V(\tau) d\tau \quad 5.3$$

depends not only on the current but also on the path taken through the state space, giving rise to memory effects.

5.1.2.1. Circuit Diagram of Meminductor Emulator

The proposed meminductor emulator, which consists of only five MOSFET transistors, is shown in Figure 5.1. The transistors M_1, M_2, M_3 , and M_4 are used to create the meminductor. The transistor M_5 controls the charge on the floating gate (gate terminal of transistor M_5), which introduces the memory effect. The floating gate allows charge to accumulate over time,

leading to a memory based inductance. Input voltage (V_{in}) applied to the gate of M_2 , modulates the current through the circuit.

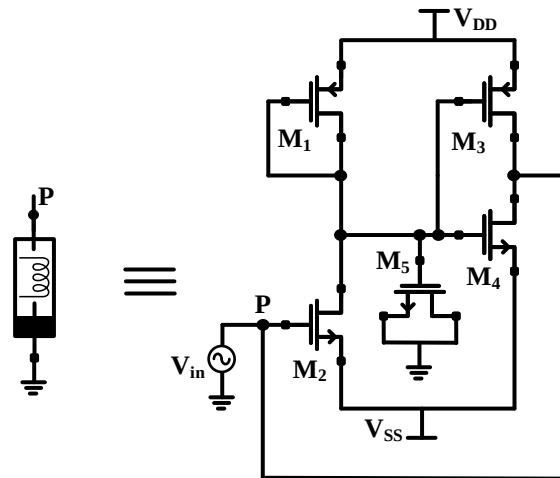


Figure 5. 1 Proposed meminductor emulator circuit.

Power supply voltages (V_{DD} and V_{SS}) provide the biasing and operating points. The stored charge influences the threshold voltage of the MOSFETs, altering the effective conductance and hence the current through the circuit. M_1 and M_2 form a differential pair, amplifying the input signal and feeding it to the floating gate. M_3 and M_4 act as current mirrors, creating a mirrored output that is fed back to the input gate. The combination of feedback and charge accumulation creates a nonlinear relationship between flux and current. When subjected to an AC input, the circuit exhibits a pinched hysteresis loop in the flux-current plane, which is the hallmark of meminductive behavior. The shape of the loop changes based on the history of the input signal due to the floating-gate memory effect. The aspect ratios of the used transistors are tabulated in Table 5.1.

Table 5. 1 W/L ratio of the transistors

Transistors	Type	W/L Ratio
M_1, M_3	PMOS	$10\mu m/0.18\mu m$
M_2, M_4	NMOS	$10\mu m/0.18\mu m$
M_5	NMOS	$0.40\mu m/0.18\mu m$

5.1.3 Mathematical Analysis of Proposed Meminductor Emulator

In this section, the meminductive nature of the circuit in Figure 5.1 has been mathematically analyzed using the differential mirror floating gate approach and the gyrator circuit approach. The emulator circuit is probed using the differential mirror floating gate approach because transistors M_1 and M_2 form a differential pair, transistors M_3 and M_4 form a current mirror, and transistor M_5 acts as a floating gate transistor. The same emulator circuit is probed using a gyrator circuit approach because a gyrator circuit typically uses two voltage-controlled current sources (transistors M_1 and M_2) to convert a capacitor (transistor M_5) into an inductor. Transistors M_3 and M_4 are part of the bias network and the feedback loop.

5.1.3.1. Differential Mirror Floating Gate (DMFG) Approach

Meminductance is defined as the flux-dependent inductance as

$$L_m(\phi) = \frac{\partial \phi}{\partial i} \quad 5.4$$

where ϕ is the flux linkage given by

$$\phi(t) = \int_0^t v(\tau) d\tau \quad 5.5$$

To derive the expression for the meminductance, the flux linkage $\phi(t)$ needs to be expressed in terms of transistor voltages and currents. Since the transistors operate in the saturation mode, the drain current i_D in the saturation region is given by

$$i_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad 5.6$$

where μ is the mobility of charge carriers, C_{ox} is the gate oxide capacitance per unit area, (W, L) are the width and length of the transistor, (V_{GS}, V_{DS}) are the gate-source and drain-source voltages, V_{th} is the threshold voltage and λ is the channel-length modulation parameter.

The relationship between the current and flux depends on the transistor saturation behavior and the feedback network. In the feedback network the current mirror and differential pair introduce a nonlinear relationship between the current and flux.

The current through M_1 is given by

$$i_{D1} = \frac{\mu C_{ox}}{2} \frac{W_1}{L_1} (V_{in} - V_{th})^2 (1 + \lambda V_{DS1}) \quad 5.7$$

Similarly, the current through M_2 is given by

$$i_{D2} = \frac{\mu C_{ox}}{2} \frac{W_2}{L_2} (0 - V_{th})^2 (1 + \lambda V_{DS2}) = 0 \text{ (cut-off for small } V_{in}) \quad 5.8$$

Since i_{D1} and i_{D2} flow in opposite directions, the current difference I_{tail} is given by

$$I_{tail} = i_{D1} - (-i_{D2}) \quad 5.9$$

The current i_{D3} flowing through the transistors M_3 is the same as i_{D1} whereas the current i_{D4} flowing through the transistor M_4 is proportional to i_{D3} , i.e.,

$$i_{D3} = i_{D1}, i_{D4} = \frac{W_4}{W_3} i_{D3} \quad 5.10$$

The mirrored currents, i_{D3} and i_{D4} provide feedback to the floating-gate transistor and therefore introduce a nonlinear dependency. The transistor M_5 acts as a memory element. The gate voltage of M_5 will be modulated by charge trapping leading to a dynamic threshold voltage given by

$$V_{th,5}(t) = V_{th,0} + \frac{Q_{fg}(t)}{C_{fg}} \quad 5.11$$

where $Q_{fg}(t)$ is charge on the floating gate, C_{fg} is the floating gate capacitance and the charge $Q_{fg}(t)$ evolves according to the equation given by

$$\frac{dQ_{fg}}{dt} = i_{D4} \quad 5.12$$

after substituting $Q_{fg}(t)$ from equation 5.12 into equation 5.11 $V_{th,5}(t)$ is given by

$$V_{th,5}(t) = V_{th,0} + \frac{1}{C_{fg}} \int_0^t i_{D4}(\tau) d\tau \quad 5.13$$

Thus, it is evident from equation 5.13 that the floating-gate transistor introduces memory into the threshold voltage. $V_{in}(t)$ drives the differential pair current, which gets mirrored and feeds the floating gate, dynamically influencing the flux linkage. The floating gate threshold is influenced by the flux as

$$V_{th,5}(t) = V_{th,0} + \frac{1}{C_{fg}} \phi(t) \quad 5.14$$

The current through M_5 is given by

$$i_{D5} = \frac{\mu C_{ox}}{2} \frac{W_5}{L_5} (V_{GS5} - V_{th,5}(t))^2 \quad 5.15$$

Substituting the flux dependence from equation 5.14, i_{D5} becomes

$$i_{D5} = \frac{\mu C_{ox}}{2} \frac{W_5}{L_5} \left(V_{GS5} - V_{th,0} - \frac{\phi(t)}{C_{fg}} \right)^2 \quad 5.16$$

The meminductance $L_m(\phi)$ is given as

$$L_m(\phi) = \frac{\partial \phi}{\partial i_{D5}} \quad 5.17$$

Taking the derivative, the meminductance is given by

$$L_m(\phi) = \left[\frac{\mu C_{ox}}{2} \frac{W_5}{L_5} \cdot 2 \left(V_{GS5} - V_{th,0} - \frac{\phi(t)}{C_{fg}} \right) \cdot \frac{-1}{C_{fg}} \right]^{-1} \quad 5.18$$

$$L_m(\phi) = - \frac{1}{\mu C_{ox} \frac{W_5}{L_5} \left(V_{GS5} - V_{th,0} - \frac{\phi(t)}{C_{fg}} \right) / C_{fg}} \quad 5.19$$

Therefore, the meminductance of the proposed circuit becomes

$$L_m(\phi) = - \frac{C_{fg}}{\mu C_{ox} \frac{W_5}{L_5} \left(V_{GS5} - V_{th,0} - \frac{\phi(t)}{C_{fg}} \right)} \quad 5.20$$

Clearly the meminductance is nonlinear and depends explicitly on the flux. The negative sign reflects the phase inversion caused by the feedback loop. The floating gate dynamically shifts the threshold voltage, creating memory-based inductance. The meminductance is tunable through both the gate-source voltage and the charge on the floating gate.

Parasitic capacitance and resistance in a MOS transistor occur on account of the separation of mobile charges in the regions within the structure of MOSFET and the interconnect resistances due to the metallic structure, respectively. Non-desirable in nature, the parasitic resistance is not affected by the frequency of operation, however, the parasitic capacitance, though, negligible at low frequencies, becomes a serious issue at higher frequencies, especially in RF circuits. Hence, it becomes prudent to analyze the emulator circuit in the presence of parasitic capacitance and resistance.

For each transistor, the gate-source capacitance, including the gate overlap capacitance (C_{ov}) and gate oxide capacitance (C_{ox}), is given by

$$C_{gs} \approx C_{ox}WL + C_{ov} \quad 5.21$$

The drain-to-source capacitance includes the junction capacitance, and it is given by

$$C_{ds} \approx C_{j0} \frac{1}{\sqrt{1+V_{DS}/V_{bi}}} \quad 5.22$$

where, C_{j0} is the zero-bias junction capacitance and V_{bi} is the built-in junction potential. The floating gate introduces additional coupling capacitances C_{fgs} (floating gate to source capacitance), C_{fgd} (floating gate to drain capacitance), and C_{fgt} (floating gate to substrate capacitance). Parasitic resistances due to channel, contact, and interconnect resistance are R_s , R_d , and R_g , respectively. The drain current with channel-length modulation and gate capacitance effects is given by

$$i_D = \frac{\mu C_{ox} W}{2 L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) + \frac{V_{GS} - V_{th}}{R_s} \quad 5.23$$

The current through the gate capacitance is given by

$$i_{Cgs} = C_{gs} \frac{dV_{GS}}{dt} \quad 5.24$$

The current through the drain capacitance is given by

$$i_{Cds} = C_{ds} \frac{dV_{DS}}{dt} \quad 5.25$$

The current through the coupling capacitances from the floating gate is given by

$$i_{fg} = C_{fgs} \frac{dV_{GS}}{dt} + C_{fgd} \frac{dV_{DS}}{dt} + C_{fgt} \frac{dV_{sub}}{dt} \quad 5.26$$

In the presence of parasitic capacitance and resistance, the drain current flowing through M_1 is given by

$$i_{D1} = \frac{\mu C_{ox} W_1}{2 L_1} (V_{in} - V_{th})^2 (1 + \lambda V_{DS1}) + C_{gs1} \frac{dV_{GS1}}{dt} + \frac{V_{in} - V_{th}}{R_{s1}} \quad 5.27$$

The drain current flowing through M_2 is given by

$$i_{D2} = \frac{\mu C_{ox} W_2}{2 L_2} (0 - V_{th})^2 (1 + \lambda V_{DS2}) + C_{gs2} \frac{dV_{GS2}}{dt} + \frac{0 - V_{th}}{R_{s2}} \quad 5.28$$

The current i_{D2} can still be considered zero due to the transistor cut-off for small input voltage (v_{in}).

Thus, the tail current (as described in equation 5.9) is given by

$$I_{tail} = i_{D1} - (-i_{D2}) \quad 5.29$$

For the current mirror, the current through the transistor M_3 , including the gate and drain capacitance charging current, is given by

$$i_{D3} = \frac{\mu C_{ox}}{2} \frac{W_3}{L_3} (V_{GS3} - V_{th})^2 (1 + \lambda V_{DS3}) + C_{gs3} \frac{dV_{GS3}}{dt} + C_{ds3} \frac{dV_{DS3}}{dt} \quad 5.30$$

Current through M_4 is given by

$$i_{D4} = \frac{W_4}{W_3} i_{D3} + \frac{V_{GS4} - V_{th}}{R_{S4}} \quad 5.31$$

The floating-gate charge is given as the difference of the current through the transistor M_4 and gate leakage current i_{leak} due to subthreshold conduction and gate tunneling.

$$\frac{dQ_{fg}}{dt} = i_{D4} - i_{leak} \quad 5.32$$

Hence, the threshold voltage of transistor M_5 gets modified and is given by

$$V_{th,5}(t) = V_{th,0} + \frac{1}{C_{fg}} \left[\left(\int_0^t (i_{D4} - i_{leak}) dt' \right) + C_{fgs} V_{GS5} + C_{fgd} V_{DS5} + C_{fgt} V_{sub} \right] \quad 5.33$$

The flux linkage with parasitic capacitance is given by

$$\phi(t) = \int_0^t (v_{in}(t') + R_s i_{D5} + i_{Cgs} + i_{Cds} + i_{fg}) dt' \quad 5.34$$

Using equation 5.24, 5.25 and 5.26 in the equation 5.34, the flux linkage becomes

$$\phi(t) = \int_0^t v_{in}(t') dt' + R_s \int_0^t i_{D5}(t') dt' + C_{gs} V_{GS}(t) + C_{ds} V_{DS}(t) + C_{fgs} V_{GS5} + C_{fgd} V_{DS5} + C_{fgt} V_{sub} \quad 5.35$$

In order to evaluate the current through transistor M_5 , the floating-gate model yields

$$i_{D5} = \frac{\mu C_{ox}}{2} \frac{W_5}{L_5} \left(V_{GS5} - V_{th,0} - \frac{\phi(t)}{C_{fg}} \right)^2 \quad 5.36$$

Taking into consideration the effects of gate and drain parasitics, the drain current flowing through M_5 is given by

$$i_{D5} = \frac{\mu C_{ox}}{2} \frac{W_5}{L_5} \left(V_{GS5} - V_{th,0} - \frac{\phi(t)}{C_{fg}} - \frac{V_{GS5} C_{gs5}}{C_{fg}} - \frac{V_{DS5} C_{ds5}}{C_{fg}} \right)^2 \quad 5.37$$

The meminductance is given by

$$L_m(\phi) = \frac{\partial \phi}{\partial i_{D5}} \quad 5.38$$

Upon taking the derivative, the expression for the meminductance is given by

$$L_m(\phi) = - \frac{C_{fg}}{\mu C_{ox} \frac{W_5}{L_5} \left(V_{GS5} - V_{th,0} - \frac{\phi(t)}{C_{fg}} - \frac{V_{GS5} C_{gs5}}{C_{fg}} - \frac{V_{DS5} C_{dn5}}{C_{fg}} \right)} \quad 5.39$$

Hence, the effects of parasitic capacitances and resistances are summarized below:

- C_{gs5}, C_{ds5} reduce meminductance by adding extra flux terms.
- R_s introduces a resistive loss, affecting dynamic behavior.
- Coupling capacitances distort the flux-current relationship.

5.1.3.2. Gyrator Circuit Approach

A gyrator is a special two-port electrical network that transforms one impedance into another, for instance, a capacitor into an inductor, or vice versa, depending on how the gyrator is connected to the circuit. A pure gyrator itself does not store energy like inductors or capacitors, it only emulates their behavior. A gyrator typically uses two voltage-controlled current sources (VCCS) to convert a capacitor into an inductor. The inductance value of the inductor is given by $L = C/(G_1 G_2)$, where G_1 and G_2 are the transconductances of the VCCSs. If the transconductances are controlled by memristive elements or by charge stored in MOSFET gates, then the inductance would have memory, i.e., meminductance.

The proposed emulator configuration follows a gyrator circuit approach. In the proposed circuit, the transistors $M_1 - M_5$ form a gyrator structure in which the transistors M_1 and M_2 are the VCCSs, and the transistors ($M_3 - M_5$) are the part of a bias network or part of a feedback loop. The transconductance (g_m) of a MOSFET, which depends on the gate-source voltage, is influenced by the previous values of currents.

The inductance L , of the active inductor based on the gyrator, is given by:

$$L = \frac{C}{g_{m1} g_{m2}} \quad 5.40$$

where g_{m1} , and g_{m2} are the transconductances of MOSFETs M_1 and M_2 . These transconductances depend on the gate voltage of the transistor (M_5), which is controlled by the charge $q(t) = \int i(t) dt$.

Assuming that the gate voltage V_g is proportional to $q(t)$ (via a capacitor integrating current):

$$g_{m1}, g_{m2} \propto q(t) \Rightarrow g_{m1} = k_1 q(t), g_{m2} = k_2 q(t) \quad 5.41$$

Thus, the effective inductance is given by

$$L(q) = \frac{C}{k_1 k_2 q^2(t)} = \frac{K}{q^2(t)}, K = \frac{C}{k_1 k_2} \quad 5.42$$

For a time-varying inductor, the voltage-current relationship is given by

$$v(t) = \frac{d}{dt} [L(q)i(t)] = L(q) \frac{di}{dt} + i(t) \frac{dL}{dq} \frac{dq}{dt} \quad 5.43$$

Substituting $L(q) = K/q^2$ and $\frac{dL}{dq} = -\frac{2K}{q^3}$ in the equation 5.43, $v(t)$ is given by

$$v(t) = \frac{K}{q^2} \frac{di}{dt} - \frac{2Ki^2(t)}{q^3} \quad 5.44$$

A meminductor is defined by $\phi(t) = L_M(q)q(t)$. Since $\phi(t) = \int v(t)dt$, substituting ??, $\phi(t)$ is given by

$$\phi(t) = \int \left(\frac{K}{q^2} \frac{di}{dt} - \frac{2Ki^2}{q^3} \right) dt \quad 5.45$$

By performing simple calculations using integration by parts, substituting $\left(i = \frac{dq}{dt}\right)$, in equation 5.45 and re-arranging, the meminductance $L_M(q)$ is given by

$$L_M(q) = \frac{K}{q^3} \frac{dq}{dt} \quad 5.46$$

This reveals a dependence on $\frac{dq}{dt}$, indicating meminductive behavior where inductance varies dynamically with both charge and current.

Hence, the meminductance L_M is nonlinear and state-dependent and it is given by

$$L_M(q, i) = \frac{K}{q^3} i(t) \quad 5.47$$

In order to perform a parasitic meminductance analysis of the MOSFET-based gyrator circuit which is shown in Figure 5.2, key parasitics such as transistor output resistances (r_o), gate source / drain capacitances (C_{gs}, C_{gd}, C_{ds}) and modulation of body effects have been considered. Each MOSFET is modeled with transconductance g_m , output resistance r_o , and capacitances C_{gs}, C_{gd} , and C_{ds} .

The effective capacitance C_{eff} at the gyrator node with parasitics is given by

$$C_{\text{eff}} = C + C_{gs1} + C_{gd1} + C_{ds1} + C_{gs2} + C_{gd2} + C_{ds2} \quad 5.48$$

Where C is the capacitance of MOSCAP M_5 . This modifies the inductance expression which is now given by

$$L_{\text{eff}} = \frac{C_{\text{eff}}}{g_{m1}g_{m2}} \quad 5.49$$

The body effect and output resistance r_o reduce the effective transconductance. Hence, for a MOSFET in saturation, the effective transconductance $g_{m,\text{eff}}$ is given by

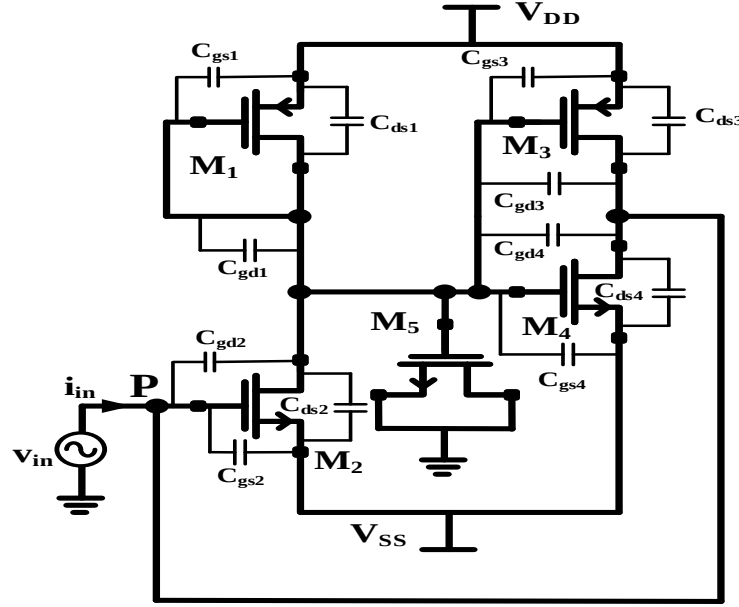


Figure 5. 2 Proposed meminductor emulator circuit with parasitics

$$g_{m,\text{eff}} = \frac{g_m}{1 + \frac{g_m}{r_o^{-1} + j\omega C_{gs}}} \approx \frac{g_m}{1 + g_m X_\omega} \quad 5.50$$

where ω is the operating frequency. Since $g_{m1}, g_{m2} \propto q(t)$ (gate charge), and $X_\omega = \frac{1}{r_o^{-1} + j\omega C_{gs}}$, the inductance is given by

$$L(q, \omega) = \frac{C_{\text{eff}}}{g_{m1,\text{eff}}g_{m2,\text{eff}}} \approx \frac{C_{\text{eff}}(1 + g_{m1}X_{\omega1})(1 + g_{m2}X_{\omega2})}{k_1 k_2 q^2(t)} \quad 5.51$$

This introduces frequency dependence and nonlinear resistive losses. The voltage equation now includes resistive and capacitive parasitics and is given by

$$v(t) = \underbrace{\frac{K}{q^2} \frac{di}{dt}}_{\text{Inductive term}} - \underbrace{\frac{2Ki^2}{q^3}}_{\text{Memristive term}} + \underbrace{\frac{i(t)}{g_{m,\text{eff}} X_\omega}}_{\text{Loss term}} + \underbrace{\frac{d}{dt} (C_{\text{eff}} v_{\text{node}}(t))}_{\text{Capacitive transient}} \quad 5.52$$

Here $v_{\text{node}}(t)$ represents voltage swings at internal nodes due to C_{gd} and C_{ds} . The modified flux $\phi(t)$ is given by

$$\phi(t) = \int \left[\frac{K}{q^2} \frac{di}{dt} - \frac{2Ki^2}{q^3} + \frac{i}{g_{m,\text{eff}} X_\omega} + C_{\text{eff}} \frac{dv_{\text{node}}}{dt} \right] dt \quad 5.53$$

Using integration by parts and substituting $i = dq/dt$ in the equation 53, the meminductance is given by

$$L_M(q, i, \omega) = \frac{K}{q^3} i(t) + \frac{C_{\text{eff}}}{g_m X_{\omega} q} + \frac{C_{\text{eff}} \omega}{q^2} \quad 5.54$$

Clearly, the meminductance given by equation 5.54 has an explicit dependence on charge, current, and frequency, with added losses from r_o

Combining all effects, the final meminductance is given by

$$L_M(q, i, \omega) = \frac{K}{q^3} i(t) \cdot \underbrace{\left[\frac{1}{1 + \frac{1}{g_m X_{\omega}} + j\omega C_{\text{eff}} X_{\omega}} \right]}_{\text{Parasitic attenuation factor}} \quad 5.55$$

Incorporating parasitics reveals that the meminductive behavior is non-ideal, with frequency-dependent inductance, losses from r_o , capacitive coupling, reduced effective Q -factor, enhanced nonlinearity from body effects and charge-modulated C_{eff} .

5.1.4 Simulation and Experimental Results

The proposed meminductor emulator circuit as depicted in Figure 5.1, is simulated using the CVS tool with 90 nm GPDK technology. Further, the same circuit has also been experimentally implemented on a breadboard in a laboratory with the help of N-type MOSFET array ALD1117 and P-type MOSFET array ALD1116. The hysteresis curve is observed on a digital storage oscilloscope. The operating frequency obtained in the laboratory is up to 850 KHz. The layout of the presented meminductor emulator, is depicted in Figure 5.3. The chip area of the proposed meminductor emulator circuit is $80.5 \mu\text{m}^2$.

For the simulation of the proposed meminductor emulator circuit, five transistors (M_{1-5}) have been used. The aspect ratio (W/L) of the transistors is shown in Table 5.1. Figure 5.4 shows the transient behavior of different parameters (e.g., voltage, current, and flux) for the proposed meminductor emulator circuit with the applied sinusoidal input signal ($V_{\text{in}} = 0.2 V_{p-p}$ and $f_{\text{in}} = 100 \text{ KHz}$).

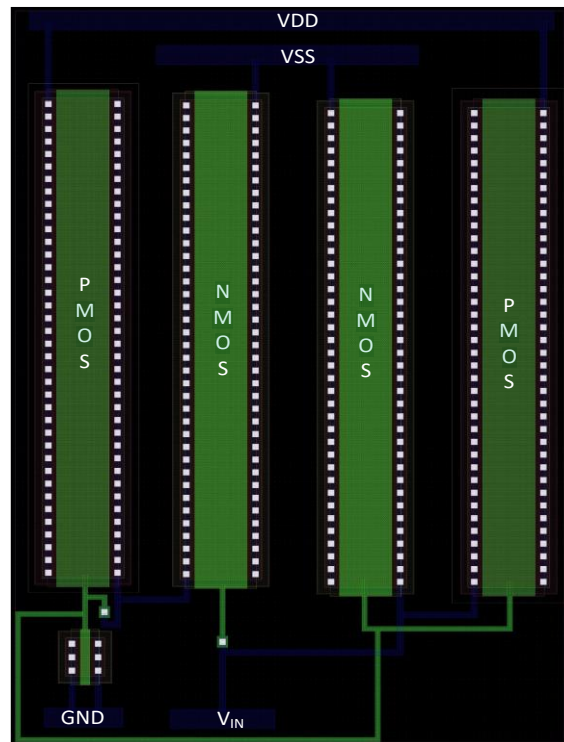
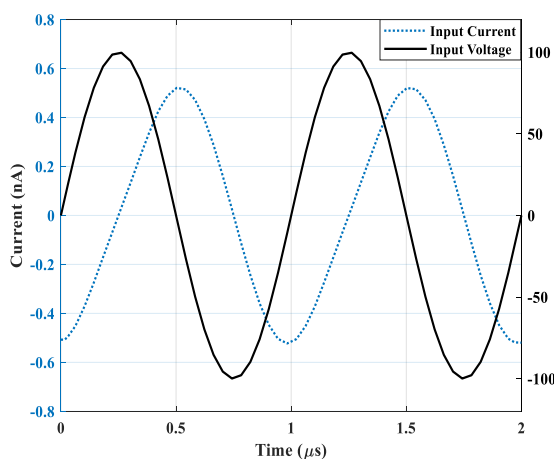
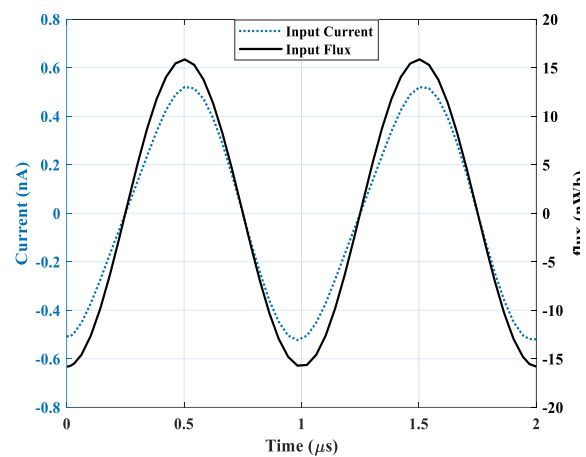


Figure 5. 3 Layout of proposed MIE circuit

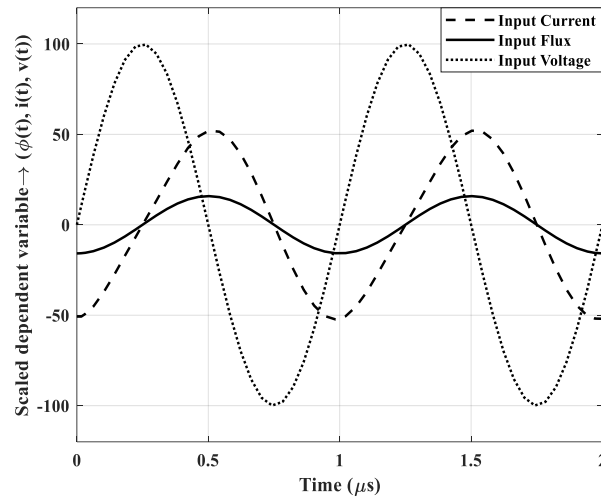
The 90° out of phase between the applied input voltage and the current flowing through the circuit, which shows the inductive behavior of the circuit, is shown in Figure 5.4(a). The current and flux waveforms are in the same phase as shown in Figure 5.4(b), which also indicates the inductive behavior of the proposed meminductor circuit.



(a)



(b)

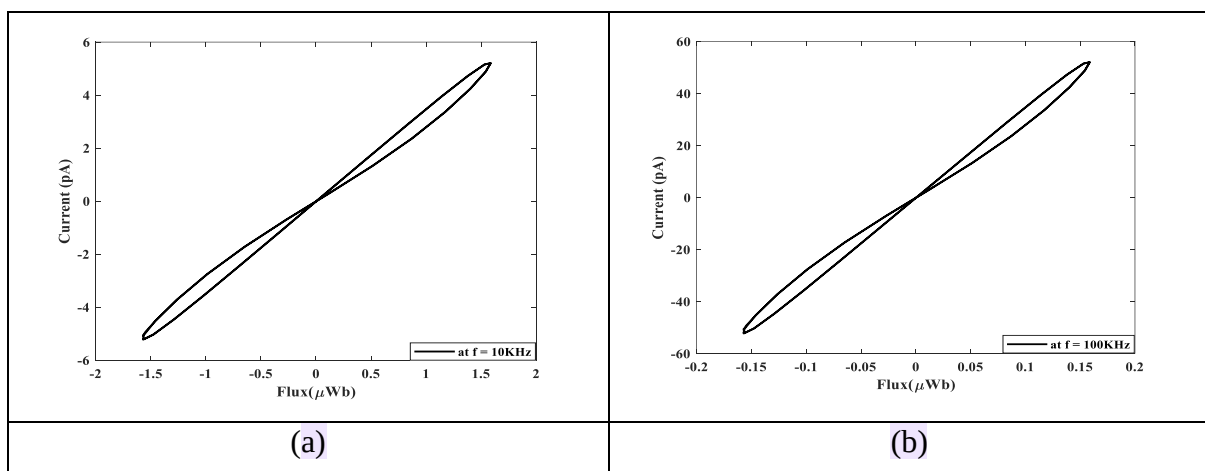


(c)

Figure 5. 4 (a) Transient waveform of input voltage and input current (b) Transient waveform of input flux and input voltage (c) Representation of signal waveforms (flux, current, and voltage) current

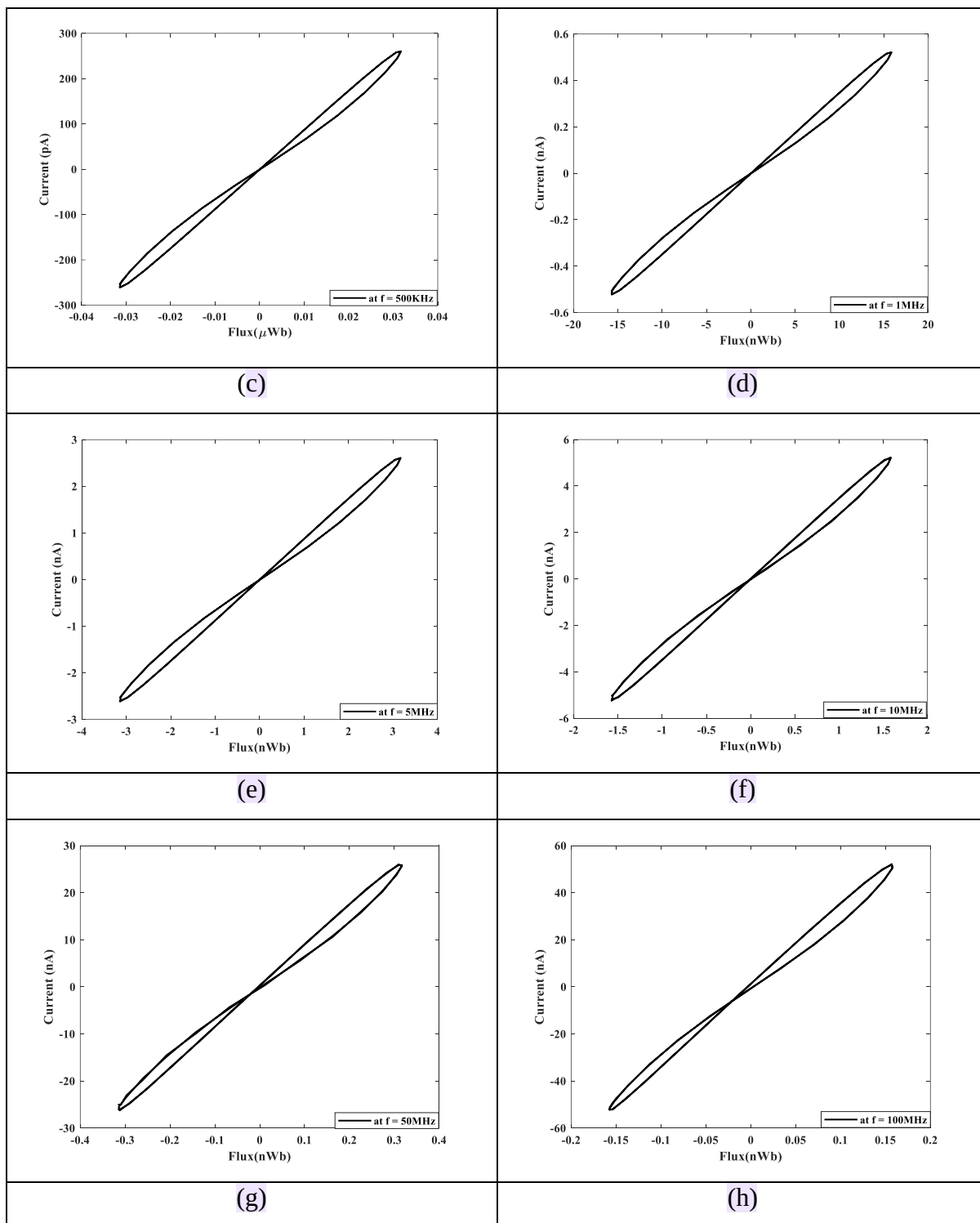
The PH curve of the proposed meminductor emulator have been simulated for a dynamic range of frequencies (10 KHz to 500 MHz). All the PHLs are shown in Figure 5.5, and it is observed that the proposed meminductor emulator works satisfactorily for the range of frequencies up to 200 MHz as shown in Figure 5.5 (a-h).

The PH curve deforms at high frequencies (200 MHz and 500MHz) (see Figure 5.5 (i-j). Hence it can be safely concluded that the working frequency of the proposed meminductor emulator is approximately up to 200 MHz , which is higher in comparison to other pre-existing meminductor emulators.



(a)

(b)



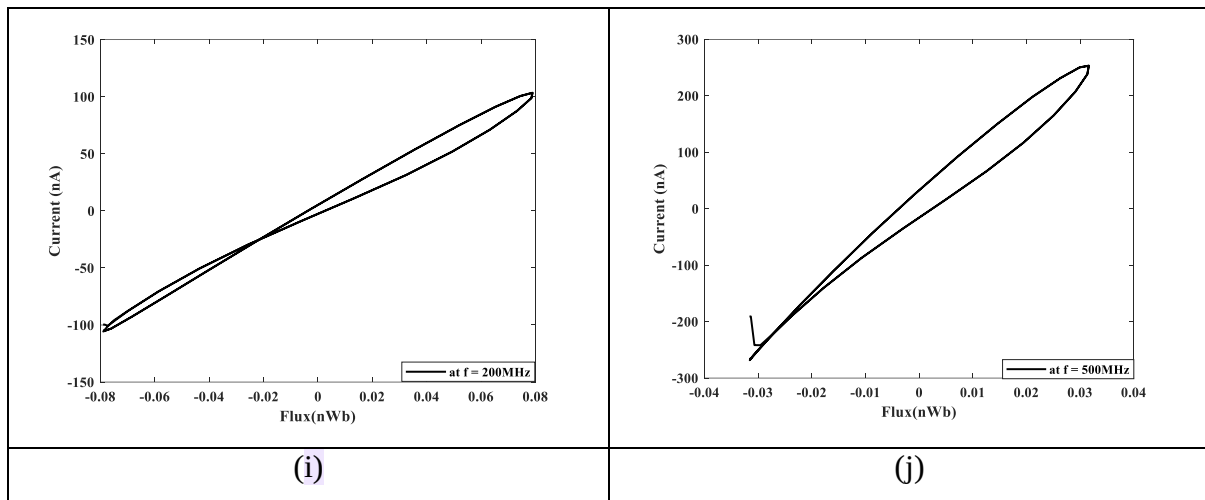


Figure 5.5 (a-j) The PH curves of the proposed meminductor emulator for the range of frequencies (10 KHz to 500 MHz)

Figure 5.6 shows the non-volatile characteristics of the proposed meminductor emulator circuit's. A square pulse with the two level voltages (low level = 0 V and high level 100mV), time period of $10 \mu\text{s}$, and 50% percent of duty cycle is applied to exhibit the non-volatile characteristics. A staircase behavior of the meminductance indicates the memory characteristics of the proposed meminductor emulator circuit.

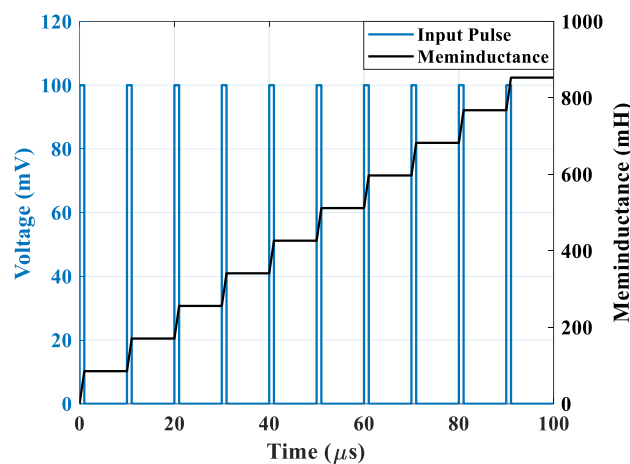


Figure 5.6 Non-volatile nature of proposed meminductor emulator circuit

A 200-run monte carlo simulation, illustrated in Figure 5.7, has been carried out to assess the reliability of the proposed meminductor emulator. The analysis considers key parameters such as maximum flux (ϕ_{max}), power consumption, peak output current (I_{max}), peak input voltage (V_{max}). Specifically, Figure 5.7(a) shows the frequency distribution of the maximum output current (in nA), Figure 5.7 (b) presents the power distribution (in mW), Figure 5.7 (c) shows the flux distribution (in nWb), and Figure 5.7(d) shows the distribution of input voltage (in mV).

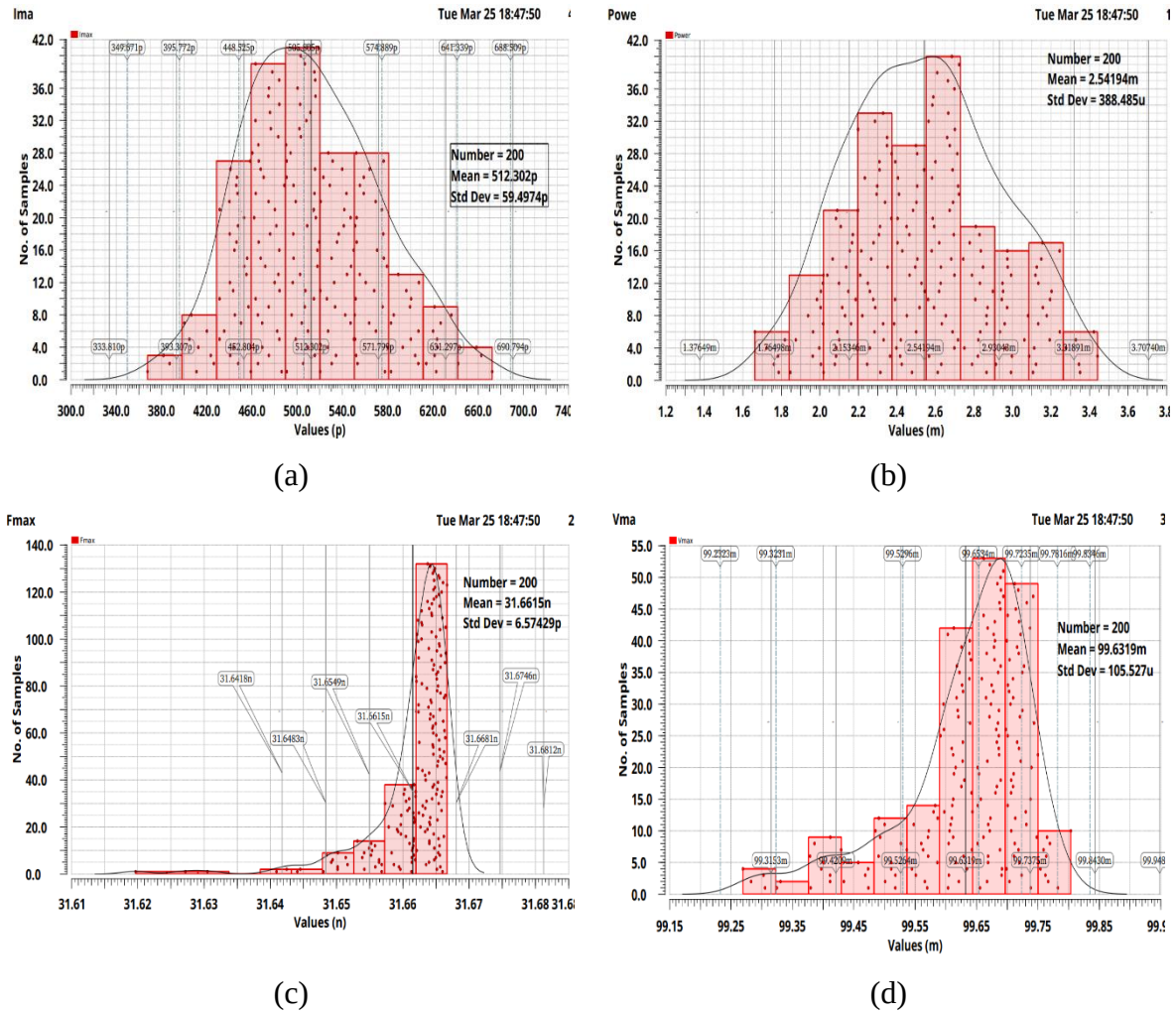


Figure 5. 7 Monte Carlo simulation results for different parameters (I_{max} , P, ϕ , and V_{max}) of proposed meminductor emulator parameters (a) Frequency distribution for current (I_{max}) in nA (b) Frequency distribution for power (P) consumption in mW (c) Frequency distribution for maximum flux (ϕ) in nWb (d) Frequency distribution for maximum input voltage (V_{max}) in mV

The results confirm that the variations in all observed parameters remain within the 3σ range of their respective mean (μ), indicating the robustness of the design. Figure 5.8 shows the PHL for simulation of 200 runs of the proposed meminductor emulator at a particular frequency (1 MHz).

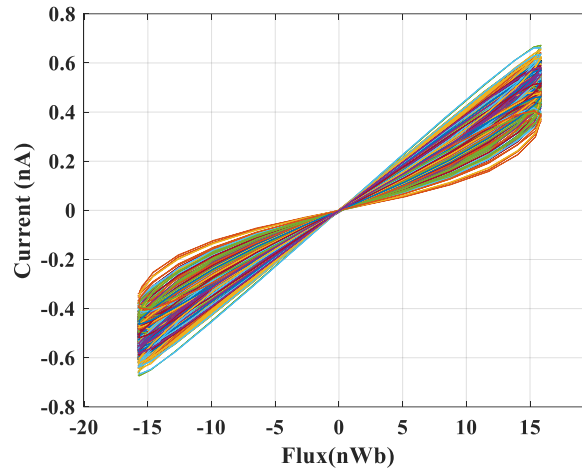
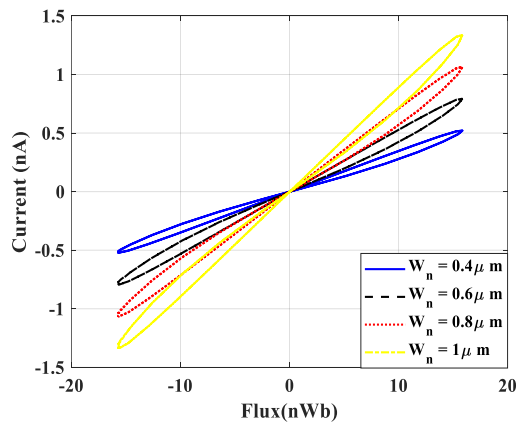
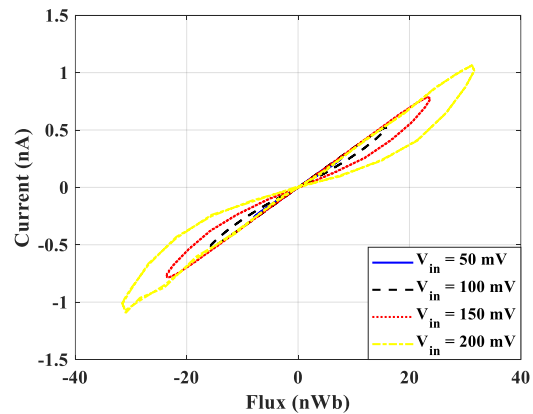


Figure 5. 8 Monte-carlo (200 run) PHL for proposed meminductor emulator circuit

Figure 5.9 illustrates the influence of input voltage amplitude, various biasing voltages, and electronic tunability on the behavior of the proposed meminductor emulator. In Figure 5.9(a), the impact of changes in transistor width is depicted, highlighting the tunable nature of the proposed meminductor emulator circuit. Figure 5.9(b) presents the PHL corresponding to different input voltage amplitudes ranging from 0.05 V to 0.2 V . Meanwhile, Figure 5.9(c) displays the PHL under different biasing conditions, with ($V_{dd} = -V_{ss} = 0.4$ V to 1.2 V).



(a)



(b)

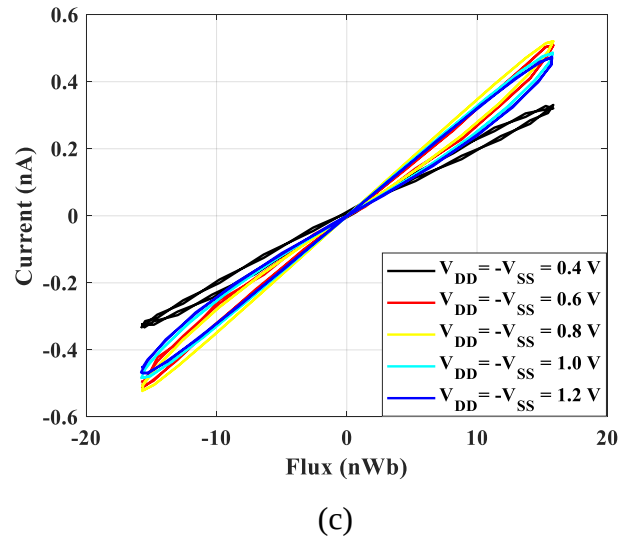
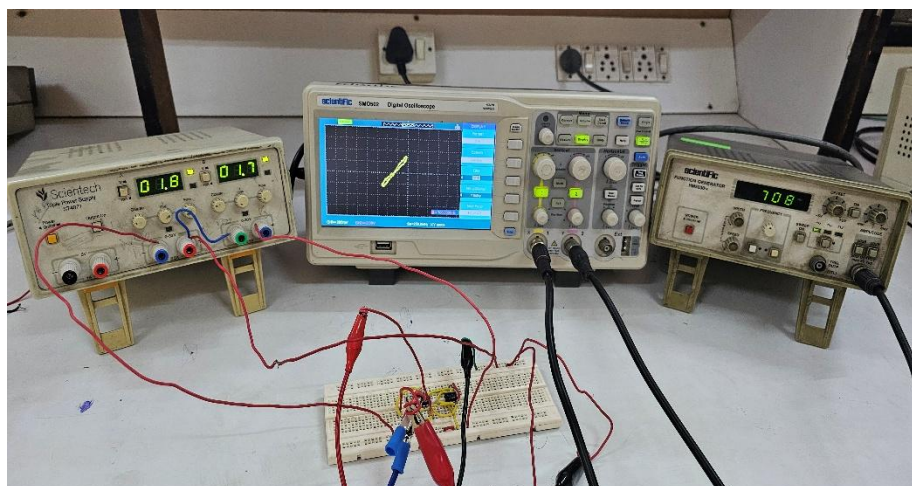
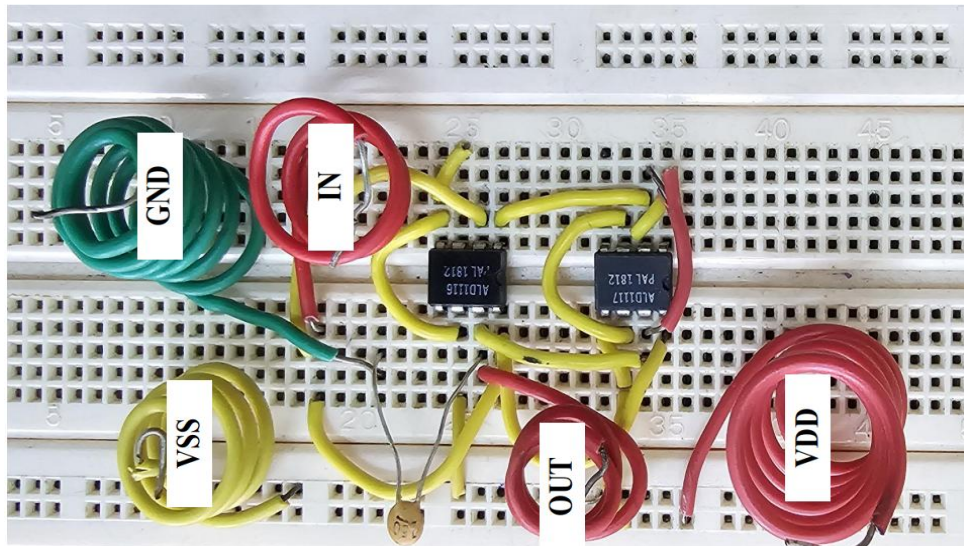


Figure 5. 9 (a) PHL for different W/L ratio of the transistor (b) PHL for different input voltage amplitudes (c) PHL for different biasing voltages

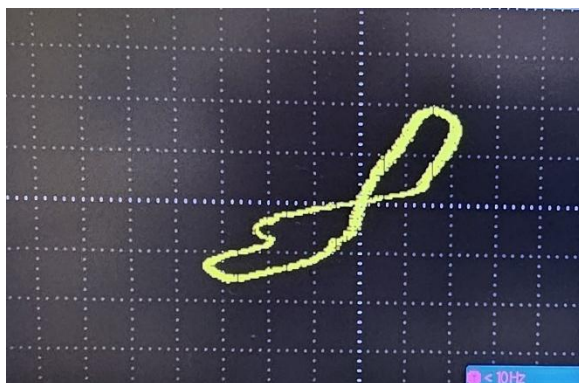
The experimental validation of the simulation results has been observed in the laboratory using ALD1116 NMOS array, ALD1117 PMOS array, and one capacitor with a capacitance value of 150 pF. The complete setup of experiment with Digital Storage Oscilloscope (DSO SMO502), 3 MHz Function Generator (Scientific HM5030-4), and a triple power supply (Scientech ST4071), is shown in Figure 5.10 (a). The breadboard diagram is illustrated in Figure 5.10(b). The PHLs of the proposed configuration are shown in Figures 5.11 (a-d) for different frequencies (256KHz, 556KHz, 779 KHz, 850KHz).



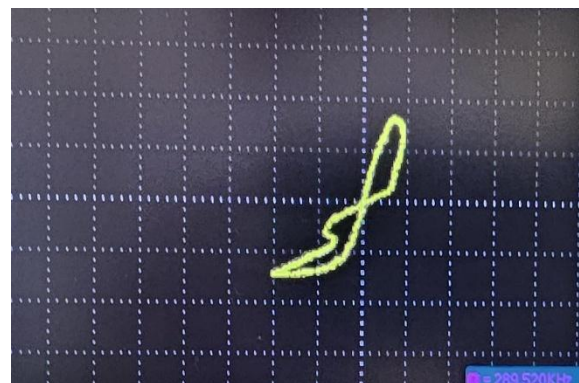


(b)

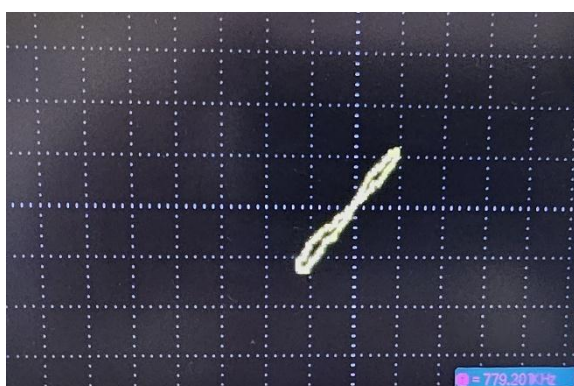
Figure 5. 10 (a) The complete setup of the experiment for the proposed meminductor emulator configuration (b) Breadboard diagram



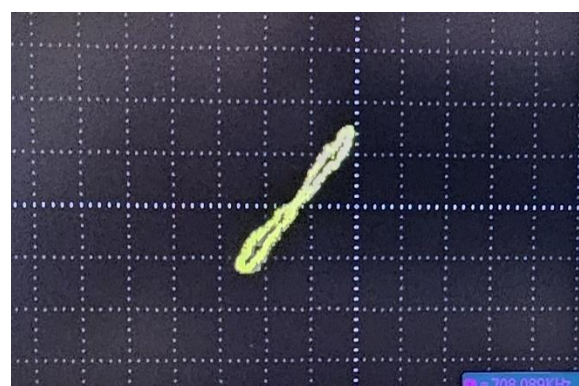
(a)



(b)



(c)



(d)

Figure 5. 11 (a) PHL at 256 KHz (b) PHL at 556 KHz (c) PHL at 779 KHz (d) PHL at 850 KHz

The operating frequency of the laboratory setup is up to 850 KHz . The experimental results are validating the simulation results. The power analysis is also shown in Figure 5.12.

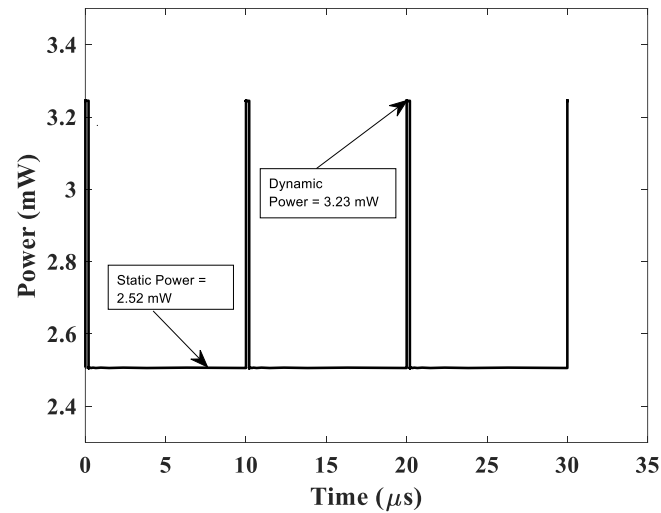


Figure 5. 12 Power analysis of meminductor emulator circuit.

The pre-layout and post-layout simulations have also done at the input frequency of 5 MHz . It is shown in Figure 5.13 and observed that there is slight variation in the pinched hysteresis loop (PHL) of the proposed meminductor emulator which is satisfactory for the fabrication of the proposed meminductor emulator.

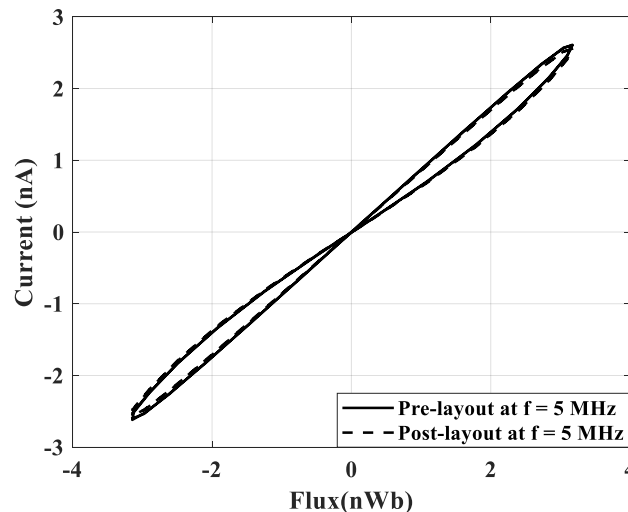


Figure 5. 13 Pre and Post-layout simulation of proposed meminductor emulator at 5 MHz frequency

The PVT (Process-Voltage-Temperature) variation analysis is presented in Figure 5.15 (a) and Figure 5.14(b). The results indicate that the proposed meminductor emulator circuit demonstrates strong resilience across a wide range of temperature (-100°C to $+100^{\circ}\text{C}$) and

under various process corners, such as Fast-Fast (FF), Slow-Fast (SF), Fast-Slow (FS), Slow-Slow (SS), and Typical (or Normal) conditions.

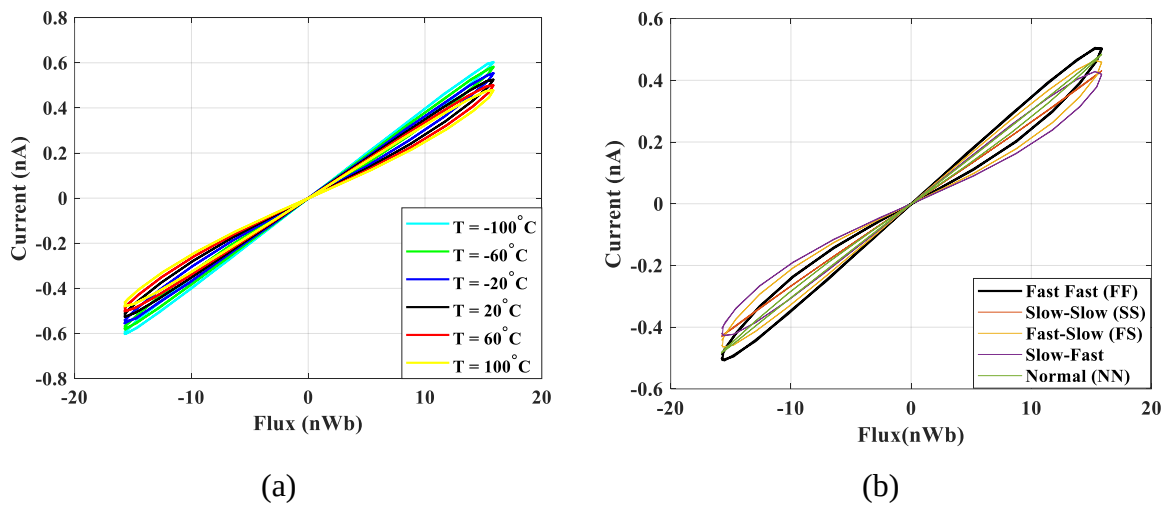
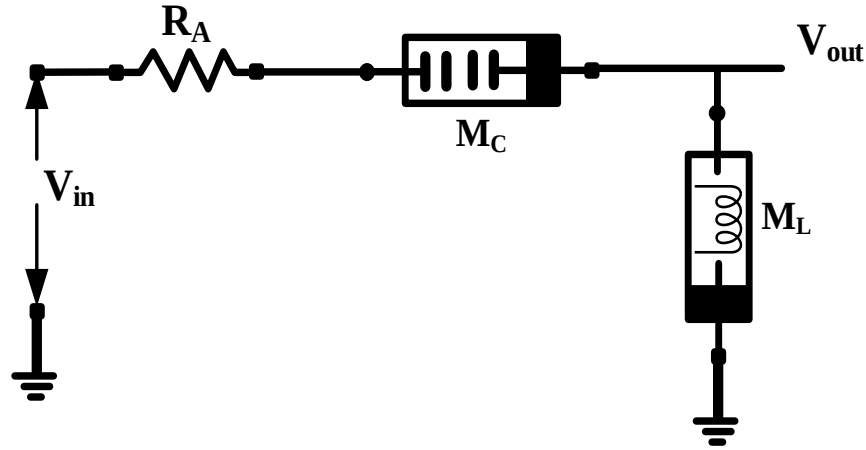


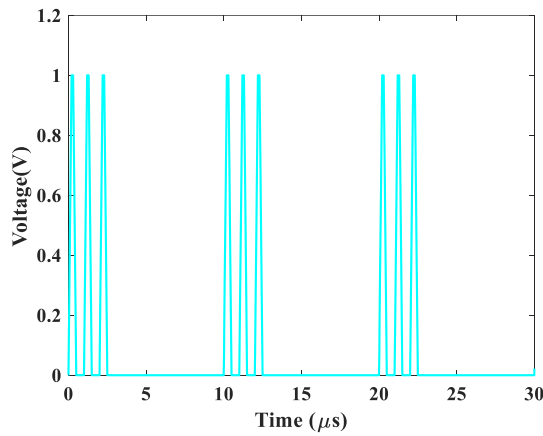
Figure 5. 14 (a) Pinched hysteresis loops (PHLs) at different temperatures (-100°C – 100°C)
(b) Pinched hysteresis loops at different corners (FF, FS, SF, SS and NN)

5.1.5 Application of MOS-based Meminductor Emulator

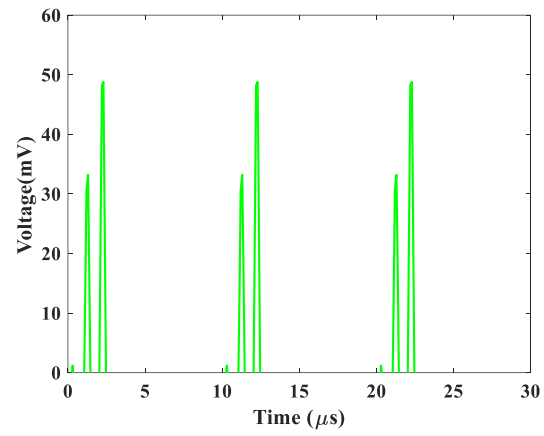
An adaptive neuromorphic system, an amoeba-inspired circuit [173], [209], [210], has been realized using the proposed meminductor emulator. The adaptive behavior circuit, illustrated in Figure 5.15(a), consists of a resistor ($R = 1\text{ K}\Omega$), a memcapacitor, and the proposed meminductor emulator. Figure 5.15 illustrates the adaptive learning circuit incorporating the proposed memcapacitor and meminductor with its corresponding response to repeated input stimuli. The applied voltage pulses, representing temperature variations, are shown in Figure 5.15 (b), while the output response, interpreted as locomotive speed, is depicted in Figure 5.15(c). It can be observed that the response amplitude increases with successive input pulses, indicating a cumulative effect due to the memory property of the memelements. This behavior is consistent with previously reported studies [74], [186], [169], where repeated stimulation leads to enhanced system response. It is important to note that this phenomenon reflects history-dependent adaptive behavior rather than anticipatory action, as the system response is governed by the internal state evolution of the memcapacitive element.



(a)



(b)



(c)

Figure 5. 15 (a) Adaptive learning circuit with proposed meminductor emulator (b) Voltage corresponding to temperature variation (c) Locomotive speed response

This section reports a simple electronically tunable meminductor emulator-controlled Chua's circuit. It is implemented by using two capacitors, an inductor, a resistance, a nonlinear resistance, and a tunable meminductor, as shown in Figure 5.16(a). The mathematical representation of the meminductor emulator based on Chua's circuit is given by the below mentioned set of equations 5.56 to 5.59.

$$C_1 \cdot \frac{dV_{C1}}{dt} = \frac{V_{C2} - V_{C1}}{Z_{RL}} - I_{MI} \quad 5.56$$

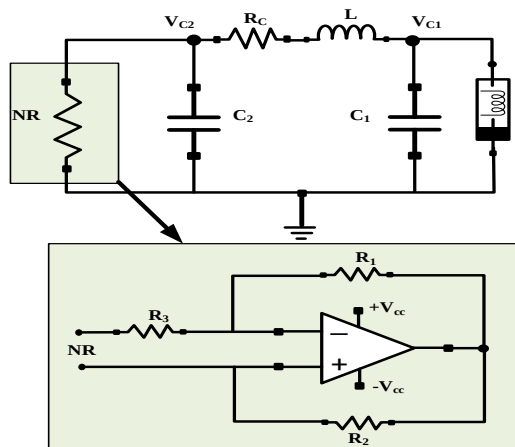
$$C_2 \cdot \frac{dV_{C2}}{dt} = -\frac{V_{C2} - V_{C1}}{Z_{RL}} - I_{NR} \quad 5.57$$

$$L \cdot \frac{dI_L}{dt} + I_{RL} \cdot R = V_{C2} - V_{C1} \quad 5.58$$

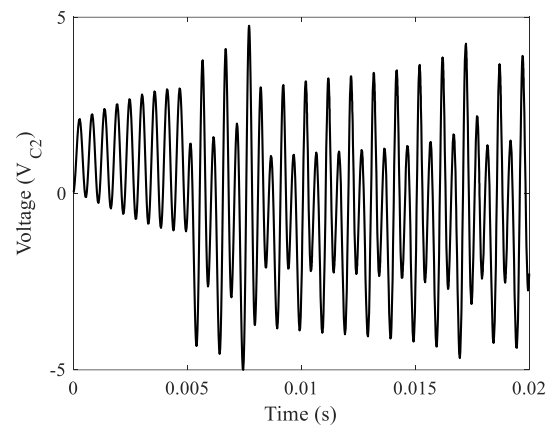
$$L_m \cdot \frac{dI_{M1}}{dt} + I_{RL} \cdot R = V_{C2} - V_{C1} \quad 5.59$$

Where the meminductance (L_m) of the proposed circuit is written as equations 5.20, 5.39, 5.47, and 5.55.

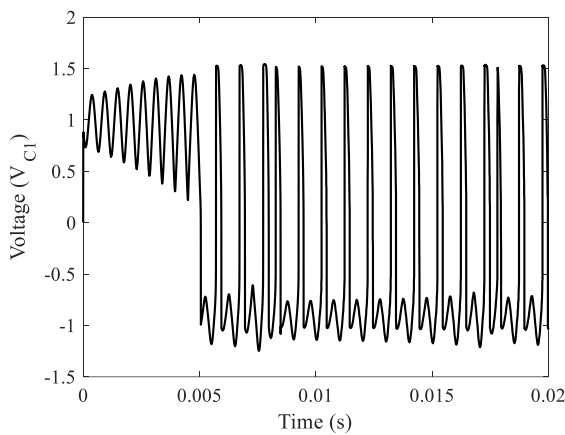
The represented chua's circuit consists of the specific parameter values of C_1, C_2, L , and R chosen as $8nF, 93nF, 89mH$, respectively, and a negative resistance (NR) as shown in Figure 5.16(a). The time domain behaviour of the different parameters of Chua's circuit is shown in Figure 5.16.



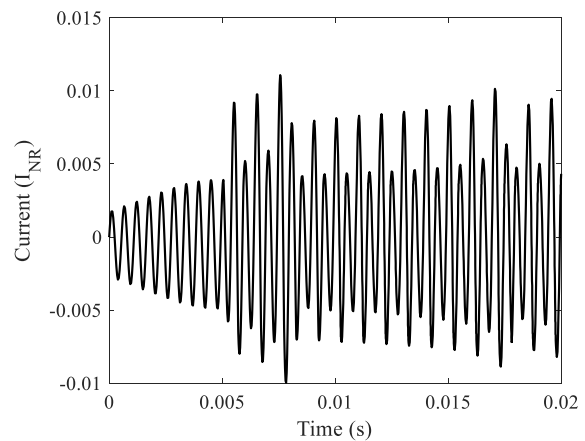
(a)



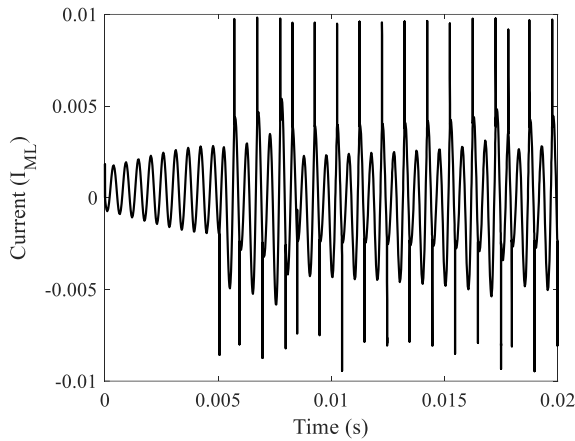
(b)



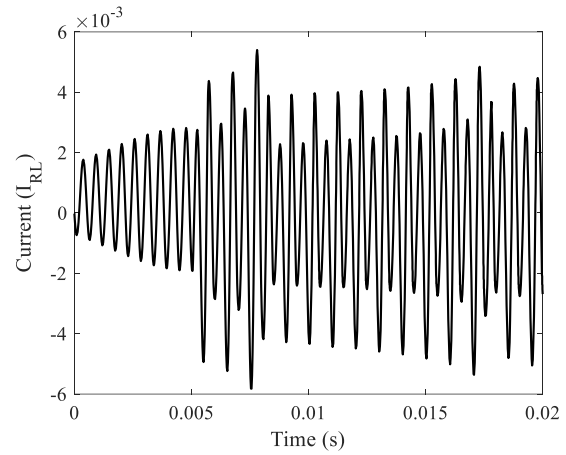
(c)



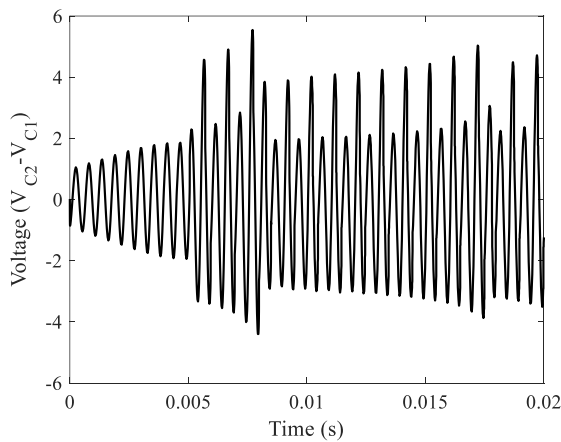
(d)



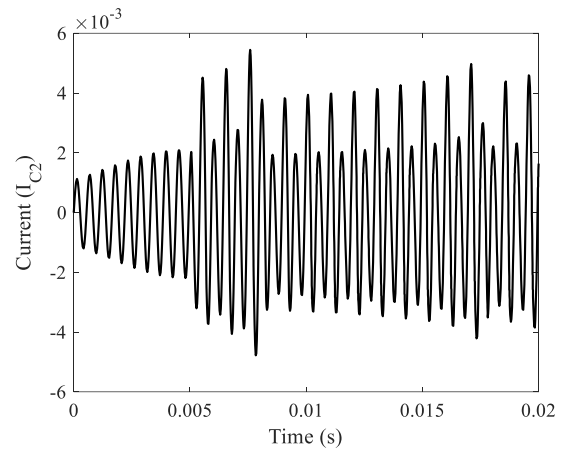
(e)



(f)



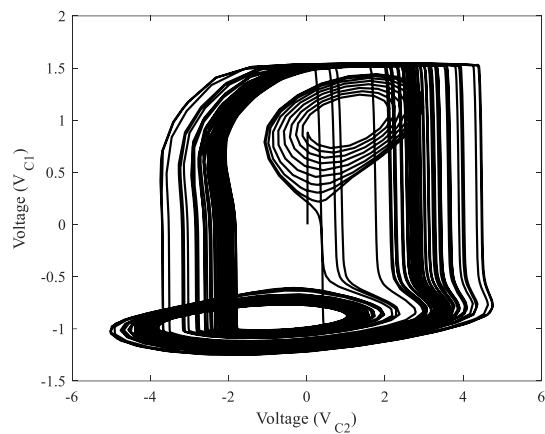
(g)



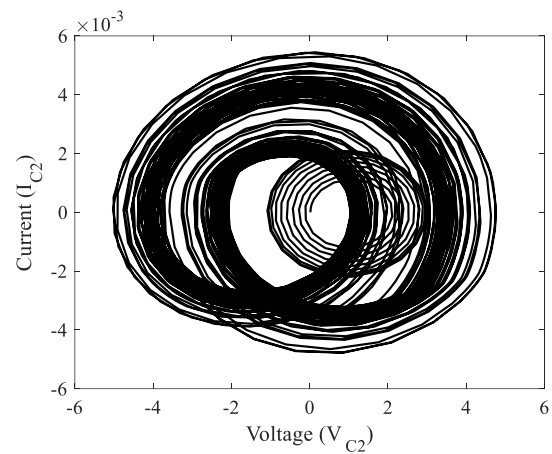
(h)

Figure 5. 16 (a) Chaos circuit diagram using proposed meminductor emulator (b-h) Chua's circuit time domain response using proposed meminductor emulator

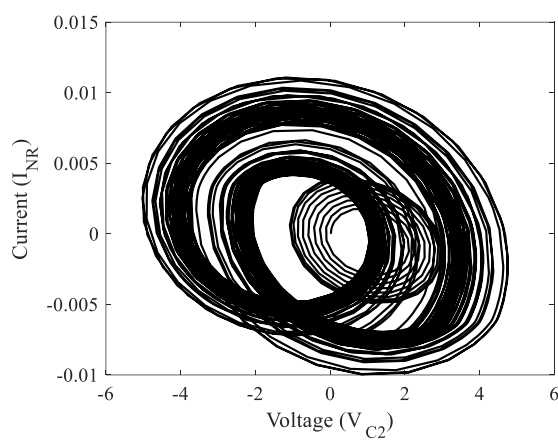
The response of voltages (V_{C1} , V_{C2}) across capacitors, currents through the inductor (L), capacitors (C_1 and C_2 , negative resistance (NR), and meminductor (M_L) are shown in Figure 17. The graphs of Chua's circuit between V_{C2} Vs V_{C1} , V_{C2} Vs I_{C2} , V_{C2} Vs I_{NR} , V_{C2} Vs I_{ML} , V_{C2} Vs I_{RL} , $V_{C2} - V_{C1}$ Vs I_{ML} , $V_{C2} - V_{C1}$ Vs I_{NR} , and $V_{C2} - V_{C1}$ Vs V_{C1} are shown in Figure 5.17 (a-h).



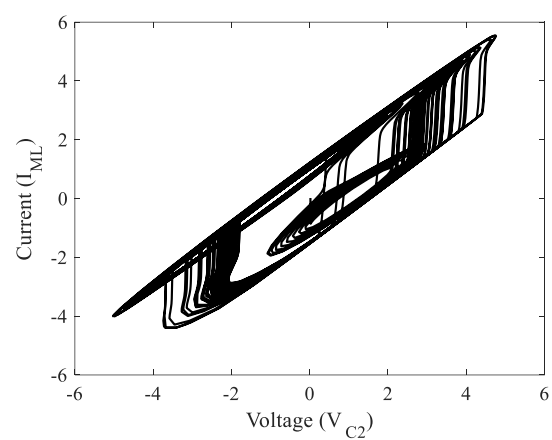
(a)



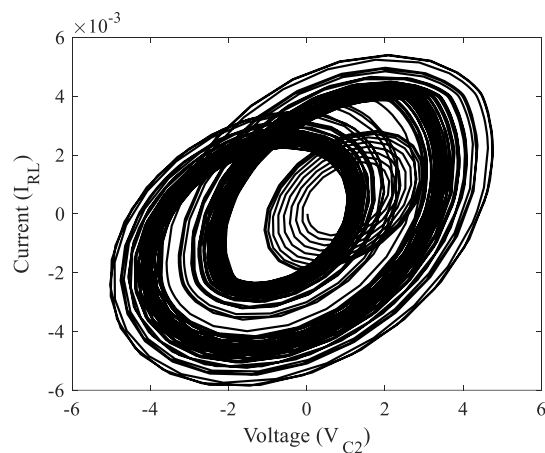
(b)



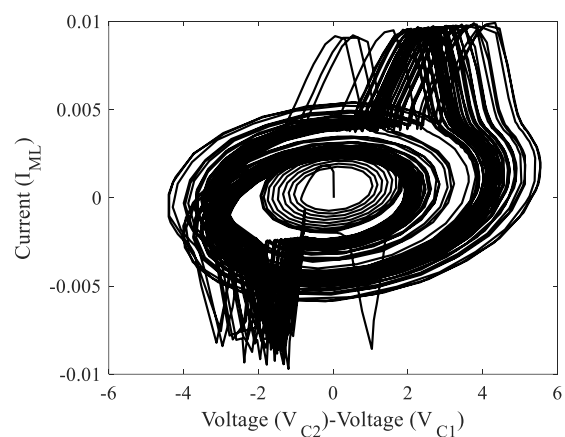
(c)



(d)



(e)



(f)

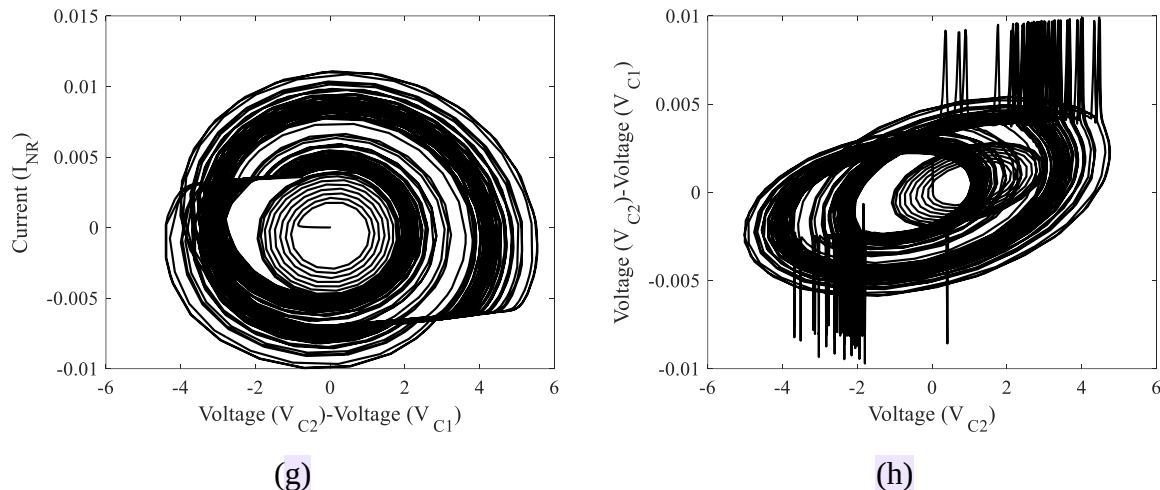


Figure 5. 17 (a-h) Chua's circuit response using proposed meminductor emulator

5.1.6 Comparison and Discussion

A comparison of existing meminductor emulators [6], [41], [77], [80], [87], [152], [153], [155], [173], [192]–[196], [204]–[207] is presented in Tables 5.2 and 5.3. The comparison is based on active/passive elements, circuit structure, technology, operating frequency, mutator-based, and electronic tunability. A multiplier is used in several prior existing meminductor emulator circuits [79], [152], [153], [173], [192], [196], [204]–[206], whereas the proposed meminductor emulator circuit does not require any multiplier circuit. In contrast to the proposed circuit, several emulators [41], [77], [152], [155], [173], [192], [195], [196] have mutator circuits for implementing the meminductor emulator making the overall design rather complex. The operating frequency of the tabulated existing memcapacitor emulators is up to some MHz. This work presents an only MOSFET based meminductor emulator with no passive components, with an operating frequency up to 200 MHz and 2.35 mW of power consumption.

Table 5. 2 Comparison of the Proposed Model with Existing Meminductor Emulators based on Design

Ref No.	Year	Multiplier Used	Existing Blocks Used	Passive/ Active Component Count	Mutator Based
[41]	2014	NO	CCII+ - 2, OPAMP - 1	R - 1, C - 1, L - 0	Yes
[205]	2016	Yes	OP-AMP - 4	R - 1, C - 2, L - 0	No
[80]	2019	No	VDTA - 2	R - 1, C - 2, L - 0	No
[87]	2019	No	AD844-4, OPAMP - 1	R - 5, C - 2, L - 0	No
[206]	2019	Yes	OP-AMP - 7	R - 13, C - 2, L - 0	No

[153]	2020	Yes	OTA - 1, OPAMP - 1	R - 8, C - 2, L - 0	No
[207]	2022	Yes	OP-AMP - 5	R - 11, C - 2, L - 0	No
[155]	2010	No	OP-AMP - 1	R - 1, C - 1, L - 0	Yes
[203]	2018	No	OTA - 1	R - 1, C - 1, L - 1	No
[77]	2020	No	OP-AMP - 3	R - 6, C - 1, L - 0	Yes
[204]	2020	Yes	Integ-2, IA - 2, Adder - 1	R - 0, C - 2, L - 0	No
[173]	2021	Yes	VDCC - 2	R - 1, C - 1, L - 0	Yes
[152]	2022	Yes	OP-AMP - 2	R - 3, C - 1, L - 0	yes
[195]	2022	No	MVDCC - 1, OTA - 1	R - 0, C - 2, L - 0	yes
[196]	2023	Yes	DOCCII - 1, CCII - 1, OPAMP - 5	R - 2, C - 2, L - 1	Yes
[192]	2023	yes	OTA - 1, MOOTA - 1	R - 1, C - 2, L - 0	yes
[193]	2024	No	CCII - 2, OTA 1	R - 1, C - 2, L - 0	yes
[194]	2024	No	OTA - 3	R - 0, C - 2, L - 0	No
Proposed Work	2025	No	MOSFET - 5	R - 0, C - 0, L - 0	No

Table 5. 3 Comparison of the Proposed Model with Existing Meminductor Emulators based on Performance

Ref No.	Experiment (yes/no)	Floating /Grounded	Power Consumption	Frequency	Electronic Tunable	Technology used
[41]	Yes	Floating	NA	37 Hz	No	NA
[205]	Yes	Grounded	NA	180 Hz	No	NA
[80]	Yes	Floating	NA	1 MHz	Yes	180 nm
[87]	Yes	Floating	NA	22 KHz	No	NA
[206]	No	Grounded	NA	200 Hz	No	NA
[153]	Yes	Floating	NA	5 KHz	Yes	NA
[207]	Yes	Floating	NA	200 Hz	No	NA
[155]	No	Grounded	NA	8 Hz	No	NA
[203]	No	Grounded	NA	500 Hz	No	NA
[77]	No	Floating	NA	10 KHz	No	NA
[204]	No	Grounded	NA	20 KHz	No	NA
[173]	Yes	Floating	NA	700 KHz	No	TSMC

[152]	No	Grounded	NA	5 KHz	No	180nm GPDK
[195]	Yes	Floating	NA	300 KHz	Yes	180 nm
[196]	No	Grounded	NA	700 Hz	Yes	NA
[192]	Yes	Floating	3.87 mW	1 MHz	Yes	
[193]	Yes	Grounded	NA	300 KHz	Yes	NA
[194]	No	Grounded	NA	10 MHz	Yes	
Proposed Work	Yes	Grounded	2.35 mW	200 MHz	Yes	90 nm GPDK

5.2. A Minimalist MOS-based Meminductor Emulator Circuit

A simple grounded meminductor emulator (MIE) based on a MOSFET configuration is presented in this paper. With six MOSFETs and two capacitors, the proposed circuit may efficiently create pinched hysteresis loops (PHL) at frequencies up to 100 KHz. The dependability of the design is confirmed by thorough analyses that include PVT assessments, which refer to modeling chips at various process, voltage, and temperature corners and non-volatility testing. Simulations were performed with 180 nm CMOS technology characteristics in CST (Cadence Spectre Tool). The consumption of power is a few microwatts in the proposed MIE. A comparative analysis of existing designs illustrates the benefits of the proposed MIE circuit.

5.2.1. Circuit Diagram and Working of Minimalist MOS-based Emulator

This research introduces a new and simple meminductor emulator circuit, as illustrated in Figure 5.18, comprising six MOSFETs and two capacitors. Among these components, the transistors M1 and M2 function as common source (CS) amplifier in which M2 drives the transistor, and M1 functions as a current source load controlled by VC1. M3 and M4 also act as a CS amplifier in which VC2 is applied as an input to transistor (M4) and transistor (M3) is the current source load controlled by an external biasing voltage VB. Similarly, M5 and M6 also represent the CS stage. In the third stage of the common source amplifier, VC1 is applied to the M6 transistor as input, and M5 is the current source load that VC2 controls. The aspect ratio (W/L) is illustrated in Table 5.4.

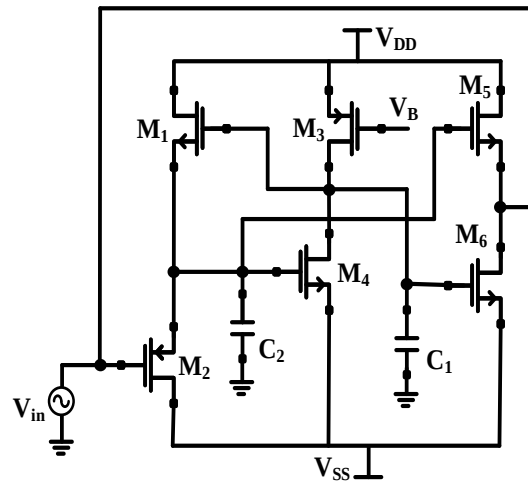


Figure 5. 18 Circuit Diagram of Minimalist MOS based Meminductor Emulator

Table 5. 4 W/L Ratio of used MOSFETs

MOSFETs	Type	W/L Ratio (μm)
M ₁ , M ₃	N-type MOS, P-type MOS	4 $\mu\text{m}/0.18 \mu\text{m}$
M ₂₋₄	N-type MOS	2 $\mu\text{m}/0.18 \mu\text{m}$
M ₅₋₆	N-type MOS	6 $\mu\text{m}/0.18 \mu\text{m}$

5.2.2. Simulation Results of Minimalist MOS-based Meminductor

This section provides a simulation examination of the proposed MIE. All evaluations were carried out utilizing the CVS tool and 180 nm GPDK technology. The MIE's characteristics were derived using a bias voltage of $V_B = -0.8 \text{ V}$ and supply voltages of $V_{DD} = 0.9 \text{ V}$ and $V_{SS} = -0.9 \text{ V}$, as well as capacitor values $C_1 = 500 \text{ pF}$ and $C_2 = 100 \text{ pF}$.

The major objective is to investigate the transient behavior of the suggested MIE. A sinusoidal input signal ($V_{in} = 400 \text{ mV}$, $f_{in} = 10 \text{ kHz}$) was used to investigate the meminductive response. Figure 5.19 shows the phase difference between flux (ϕ) and input current, proving the inductive nature of the MIE. Figures 5.19 and 5.20 show the time-domain waveforms of input current (i), flux (ϕ), and voltage (V) for the proposed emulator.

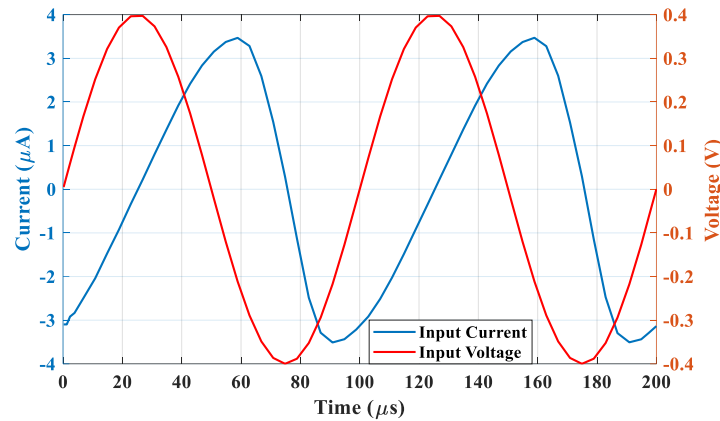


Figure 5. 19 Transient behavior of Minimalist MOS-based Meminductor Emulator

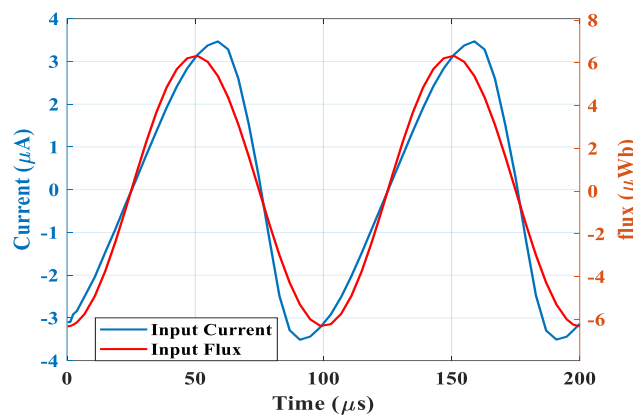


Figure 5. 20 Transient behaviour of MIE (Integration of input voltage as an input flux and input current).

One of the most important aspects of semiconductor devices is their non-volatile behavior. The suggested MIE's meminductance is predicted to change throughout the ON phase of the applied pulse signal but remain constant during the OFF period. To test this functionality, a pulse input with $V_1 = 100$ mV, $V_2 = 0$ mV, $T_{ON} = 5$ μs, and $T_{OFF} = 5$ μs is used. Figure 5.20 shows the meminductance, which is calculated as the ratio of flux (ϕ) to input current (i). As demonstrated in Figure 5.21, the meminductance increases linearly throughout the ON interval and remains constant during the OFF interval, verifying the suggested MIE's non-volatile nature.

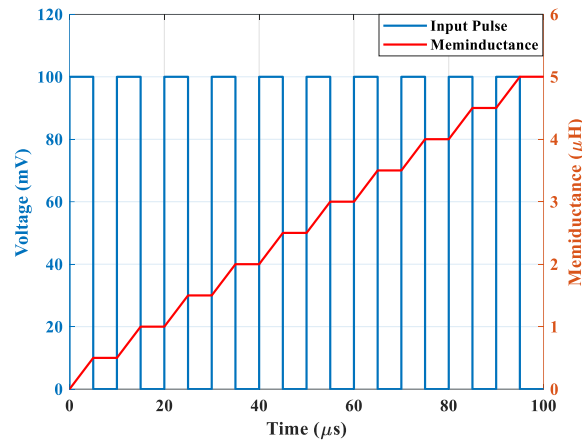


Figure 5. 21 Non-volatile characteristics of proposed MIE circuit

When excited with a sinusoidal input, the proposed MIE demonstrates a fundamental feature of meminductive devices: the **pinched hysteresis loop (PHL)** plotted between flux (ϕ) and **current (i)**. Figures 5.22 - 5.27 show the PHL curves obtained for various input frequencies with a constant amplitude of 400 mV. The unique dumbbell-shaped loop intersecting at the origin verifies the emulator's meminductive nature. PHLs are detected at frequencies ranging from 100 Hz to 100 kHz, as illustrated in Figures 5.22 to 5.27. At higher frequencies (10 kHz to 100 kHz), as shown in Figures 5.24 to 5.27, aberrations from optimum behavior arise, including a considerable shift in the pinching point. These consequences represent the non-ideal properties of the proposed MIE circuit.

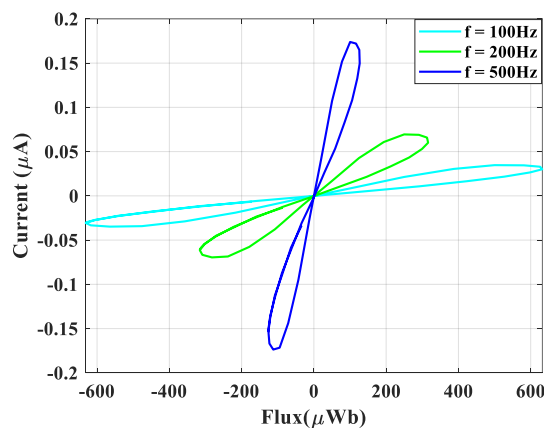


Figure 5. 22 PHL curve (f_{in} : 100 Hz to 500 Hz, V_{in} =400mV)

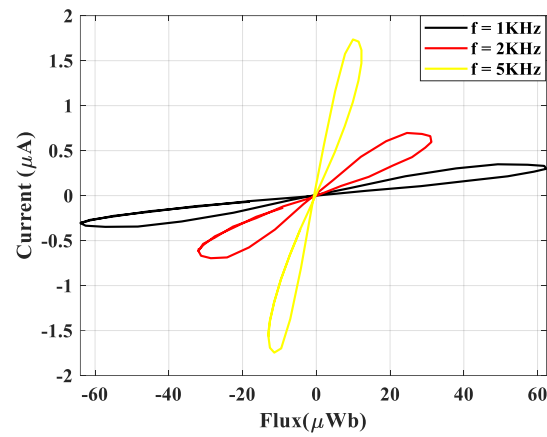


Figure 5. 23 PHL curve (f_{in} : 1 KHz to 5 KHz, $V_{in} = 400\text{mV}$)

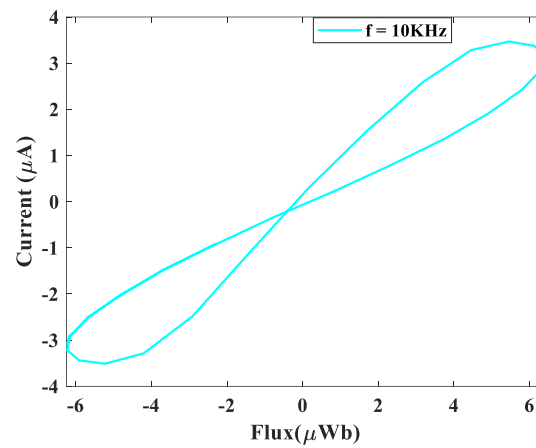


Figure 5. 24 PHL curve ($f_{in} = 10\text{ KHz}$, $V_{in} = 400\text{ mV}$)

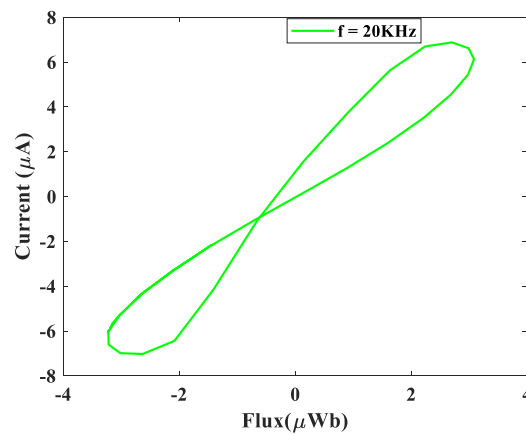


Figure 5. 25 PHL curve ($f_{in} = 20\text{ KHz}$, $V_{in} = 400\text{ mV}$)

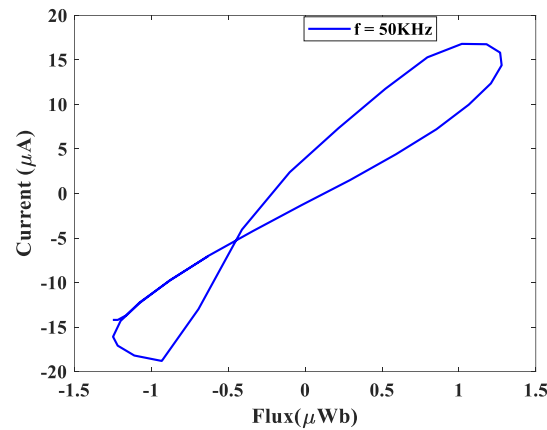


Figure 5. 26 PHL curve ($f_{in}=50$ KHz, $V_{in}=400$ mV)

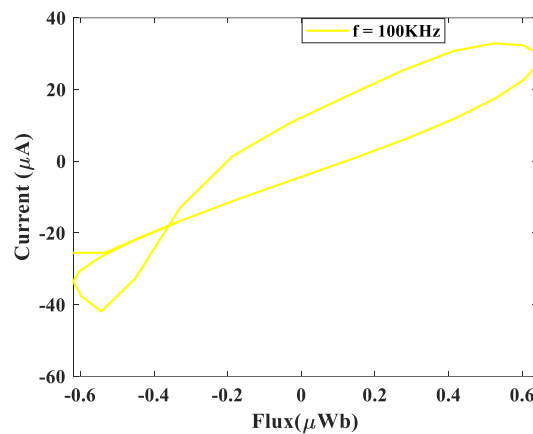


Figure 5. 27 PHL curve ($f_{in}=100$ KHz, $V_{in}=400$ mV)

Because many applications require changeable capacitance, it is critical to assess the tunability of the circuit's capacitive parts. Changes in capacitance alter the shape of the PHL curve, exhibiting the emulator's tweaking capability. The PHL properties of the proposed MIE were investigated using an input signal of $f_{in}=20$ kHz and $V_{in}=400$ mV, with C_2 and C_1 values varied. Figure 5.29 shows zero-crossing PHL curves for C_2 values ranging from 50 pF to 200 pF, demonstrating robust capacitance-tuning capability. Similarly, Figure 5.28 shows the zero-crossing PHL curves generated by varying C_1 from 100 pF to 1 nF.

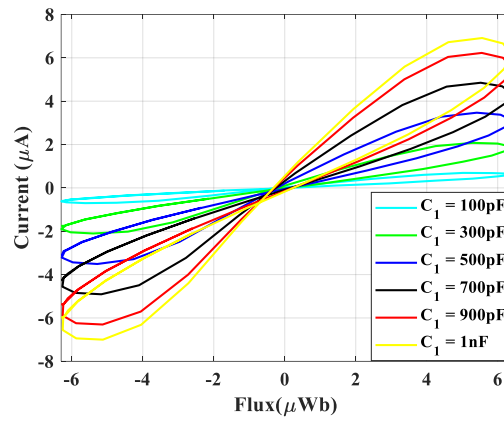


Figure 5. 28 PHL curve (C_1 : 100pF to 1nF)

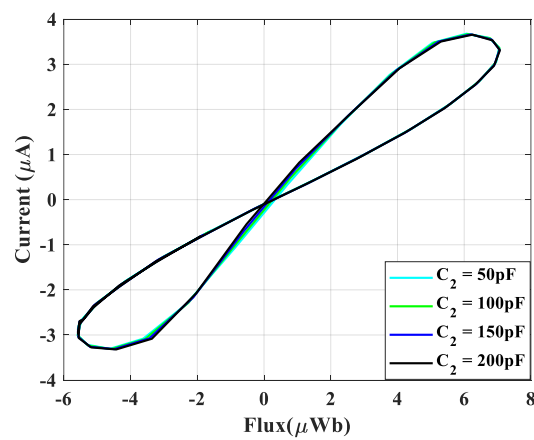


Figure 5. 29 PHL curve (C_2 : 50pF to 200pF)

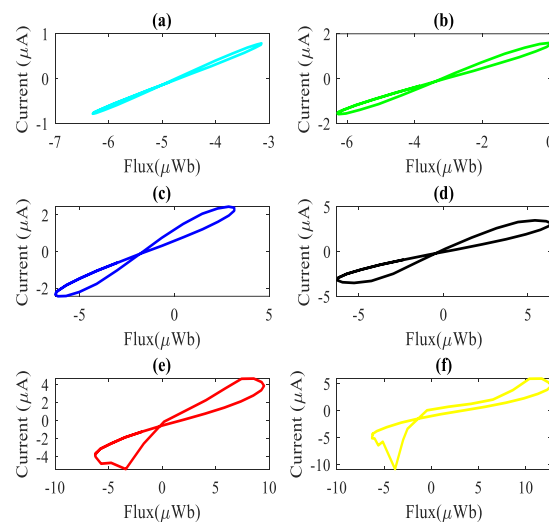


Figure 5. 30 PHL curve (V_{in} : 300 mV to 800 mV)

Electronic tunability is another important feature of the proposed MIE, as it reflects its sensitivity to changes in the applied bias voltage or current. Figure 31 depicts the PHL curves obtained for bias voltages ranging from -300 mV to -1 V, which demonstrate this adjustable characteristic. Similarly, Figure 30 shows the PHL curves of the MIE for various input supply voltages ranging from 300 mV to 800 mV at a frequency of 10 kHz.

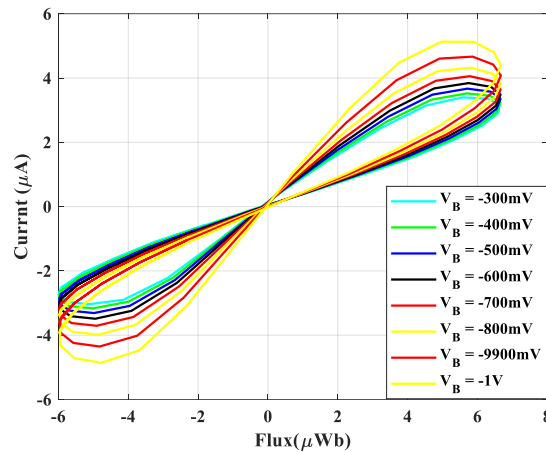


Figure 5. 31 PHL curve (V_B : -300 mV to -1 V)

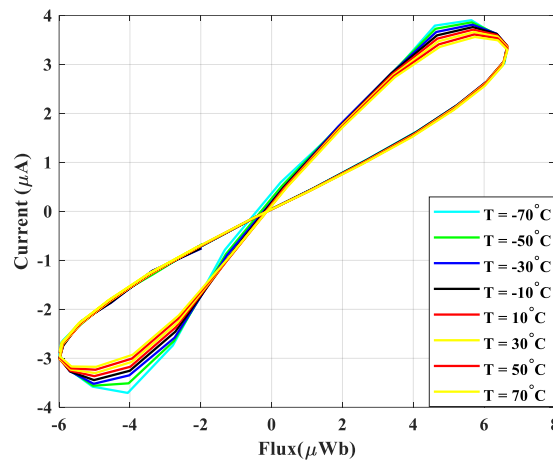


Figure 5. 32 PHL curve (-70°C to 70°C)

The performance of the suggested MIE was further evaluated at temperatures ranging from -70°C to $+70^{\circ}\text{C}$. Figure 5.32 shows the relevant PHL curves, which reveal that the device maintains its expected meminductive properties throughout the temperature range. The regular loop forms confirm the emulator's stable operation in the face of heat changes. Table 5.5 presents a comparison of the MOS-based meminductor emulator to existing designs.

Table 5. 5 Comparison of Existing Memristors with Proposed Memrinductor Emulators taking Different Parameters

Ref	Active Building Blocks	MOSFETs	RLCs	Multiplier less	M _R	Frequency	Electronic Tunable	Consumed Power	Floating (F) /Grounded (G)
[206]	CCII = 2, OTA = 1	33	R-1, C-2, L-0	Yes	0	300 KHz	Yes	NA	Grounded
[203]	CCII = 1, OPAMP = 8	31	R-9, C-2, L-0	No	0	400 Hz	No	NA	Floating
[198]	OPAMP = 7	-	R-13, C-2, L-0	No	0	300 Hz	No	NA	Grounded
[209]	VDTA = 2	64	R-0, C-2, L-0	Yes	0	1.5 MHz	Yes	NA	Floating
[152]	DVCC = 1, OTA = 2	34	R-1, C-2, L-0	No	0	10 MHz	Yes	120uW	Grounded
[192]	VDBA = 1, CDBA = 1	36	R-1, C-2, L-0	Yes	0	2 MHz	Yes	NA	Floating
[145]	OPAMP = 2	-	R-3, C-1, L-0	No	1	5 KHz	No	NA	Grounded
Proposed Work	-	6	R-0, C-2, L-0	Yes	0	100 KHz	Yes	1.19uW	Grounded

5.3 Summary

In this chapter, a compact and efficient grounded MOS-based meminductor emulator (meminductor emulator) utilizing only five MOSFET transistors has been proposed and validated. By employing a novel gyrator-based architecture and leveraging a MOSCAP to emulate a floating-gate behavior, the design eliminates the need for passive components, achieving high integration and tunability. The proposed meminductor emulator exhibits a flat frequency response up to 200 MHz and demonstrates non-volatility, thermal stability, and robustness against process variations through Monte Carlo and corner analyses. Implemented in 90nm GPDK CMOS technology and validated using the Cadence Virtuoso Spectre tool, the meminductor emulator shows superior performance compared to existing emulators. The power consumption and chip area are 2.35 mW and $80.5\mu\text{ m}^2$. Its practical applicability has been confirmed in adaptive learning and chaotic oscillator circuits, underscoring its potential for future use in neuromorphic and nonlinear dynamic systems. Another work also aims to replicate a MIE circuit in an alternative manner using six MOSFETs and two capacitors with external biasing. The proposed circuit provides a more simple and efficient design than previously proposed circuits. The simulation results show that the proposed circuit works effectively. Furthermore, research of its behavior under different temperature settings demonstrates its robustness in a variety of contexts. The key advantages of this design include fewer components, a simpler architecture, and consistent performance across diverse operating circumstances. These characteristics make the suggested MIE a strong contender for future

applications in signal processing, neuromorphic systems, and programmable analog circuits.

However, additional experimental validation will be required to determine its practical practicality. Further improvements in real electrical systems could boost power efficiency and extend the frequency range, thereby making it even more beneficial.

Chapter 6

Conclusion and Future Scope

This chapter summarize the key finding of the research presented in this thesis and conclude the work. In this chapter also explores the future direction in the field of developing efficient memelement emulators or physical memelement, such as memristor, memcapacitor, meminductor with their application in mixed singnal processing circuits. The discussion focuses on advancements in memristor, memcapacitor and meminductor emulators in the field of neuromorphic circuits, CMOS compatible optimization, hardware security, mixed signal IC integration, experimental fabrication and testing, adaptive and chaotic systems, and standard cell librarieres for memelement emulators.

6.1 Conclusion

This thesis describes the design, development, and validation of tiny, CMOS-compatible emulators for three essential memory elements: memristors, memcapacitors, and meminductors. Each emulator was meticulously constructed, simulated, and analyzed utilizing common CMOS technologies, including 45nm, 90nm and 180nm GPDk nodes, and validated with Cadence Virtuoso Spectre simulations. The designs exhibit key characteristics of their theoretical counterparts, including non-volatility, history-dependent behavior, frequency adaptability, and robust performance under process, voltage, and temperature (PVT) fluctuations. The suggested memristor emulators, available in both grounded and floating versions, offer high-frequency response (up to 80 MHz), low power consumption, and small silicon area, making them suitable for integration in analog and digital systems. They have been used successfully in chaotic oscillators, XOR gates, and neuron circuits. The memcapacitor emulator, built with MO-OTA and basic components, introduces a floating charge-controlled model with extensive tunability, low power operation, and interoperability with analog learning circuits. Its hysteresis nature and nonlinear storage dynamics make it an excellent choice for neuromorphic devices and artificial synapses. The meminductor emulator uses a unique MOS-gyrator-based topology that eliminates passive parts, resulting in flat frequency response up to 200 MHz, tunability, small layout, and low power consumption. Applications in adaptive learning systems and chaotic circuits demonstrate its practical value.

Together, these emulator circuits provide reduced architectures, increased tunability, low power operation, and ease of integration, solving various limitations of real mem-devices. Their proven use in mixed-signal processing applications demonstrates their potential as key components in next-generation intelligent and adaptive electronic systems. Despite their effectiveness in replicating key characteristics of memristive behavior, memristor emulators implemented using CMOS or discrete components exhibit several inherent limitations. Unlike physical memristors, emulator circuits rely on active elements and external power sources, resulting in increased complexity, power consumption, and reduced scalability. In the proposed memelement emulator circuits, the memory state is stored in internal capacitive nodes, and therefore the retention is inherently governed by leakage currents and parasitic effects. Due to the complexity of accurately modeling all leakage mechanisms in nanoscale CMOS, an exact analytical estimation of retention time is not straightforward. However, the retention behavior has been qualitatively verified through transient simulations, which show that the stored state persists for a finite duration after the removal of the input signal. This confirms that the proposed circuits exhibit memory characteristics with finite (quasi-nonvolatile) retention, consistent with emulator-based implementations reported in the literature. Additionally, the accuracy of emulation depends on device matching and operating conditions, making the system sensitive to noise, temperature variations, and process variations. These factors restrict the practical deployment of memristor emulators in large-scale integration, although they remain highly useful for prototyping, analysis, and validation of memristive systems.

6.2 Future Scope

The design of memelement emulators—specifically memristors, memcapacitors, and meminductors—offers a promising foundation for the development of next-generation mixed-signal processing circuits. Looking ahead, several key directions can be explored to extend the work presented in this thesis:

- **Integration in Neuromorphic Computing Systems:** Future research can focus on integrating memelement emulators into neuromorphic architectures to enhance learning capabilities, synaptic plasticity modeling, and energy-efficient signal processing.
- **CMOS-Compatible Optimization:** As CMOS technology continues to scale, optimizing memelement emulator designs for ultra-low power and high-frequency performance in advanced technology nodes (e.g., 7 nm, FinFET) can further improve their suitability for embedded systems and IoT applications.

- **Hardware Security Applications:** The non-linearity and memory features of memelements can be exploited for developing secure cryptographic primitives and physically unclonable functions (PUFs), opening avenues in hardware security.
- **Mixed-Signal IC Integration:** Extending the emulator designs for seamless integration in complex mixed-signal ICs—such as analog front-ends, ADCs/DACs, and RF circuits—can lead to more compact, tunable, and reconfigurable systems.
- **Experimental Fabrication and Testing:** Moving from simulation-based validation to physical prototyping and silicon implementation would allow practical evaluation of noise immunity, process variations, and long-term reliability.
- **Adaptive and Chaotic Systems:** Further exploration of memelement-based adaptive filters and chaotic oscillators can contribute to advanced applications in communication systems, random number generation, and secure signal modulation schemes.
- **Standard Cell Libraries for Mememulators:** Developing standard cell libraries and design automation tools for memelement emulators can accelerate their adoption in commercial EDA workflows and ASIC design.

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