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FAULT-TOLERANT AND PHASE CURRENT BALANCE CONTROL OF THREE-PHASE INTERLEAVED BOOST- CONVERTER UNDER NON-IDEAL CIRCUIT CONDITIONS

A DISSERTATION

**SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS FOR THE AWARD OF THE DEGREE OF**

MASTER OF TECHNOLOGY

IN

POWER ELECTRONICS & SYSTEMS

Submitted by:

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I hereby certify that the project Dissertation titled “**Fault-Tolerant and Phase Current Balance Control of Three-Phase Interleaved Boost Converter under Non-Ideal Circuit Conditions**” which is submitted by Undresh, Roll No. 2K24/PES/15, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This thesis presents a three-phase interleaved boost (TPIB) converter with fault tolerant capability that focuses on balancing the inductor current in three legs under non-ideal circuit conditions. PI controllers are used to maintain a stable output voltage by utilizing a voltage control loop alongside a current control loop, which also help eliminate overshoots and undershoots, as well as disturbances in the circuit. By keeping the current evenly distributed across three legs of inductors with parasitic, the system reduces ripple, enhance reliability and lifespan of the converter, which leads to easy and smoother operation of the circuit. The open circuit fault is introduced in the circuit, so if the fault is present in any leg at a particular switching cycle, then the load is distributed to the remaining healthy legs to get a constant current. The modelling of TPIB converter is performed by getting the transfer function of the system. The proposed method has been analysed and simulated in MATLAB SIMULINK. The simulation shows the results of balanced currents in healthy conditions as well as after fault conditions in the circuit.

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LIST OF ABBREVIATIONS

DC	Direct Current
IBC	Interleaved Boost Converter
TPIB	Three Phase Interleaved Boost
ACS	Average Current Sharing
ESR	Equivalent Series Resistance
CCM	Continuous Conduction Mode
LHP	Left Half Plane
RHP	Right Half Plane
TF	Transfer Function
PI	Proportional Integral

CHAPTER 1

INTRODUCTION

The rapid development of renewable energy systems, electric vehicles and portable electronic devices has generated a growing demand for efficient and reliable power conversion systems. The core of these systems are the DC-DC converters that convert electrical energy from one voltage to another with high efficiency and accurate regulation. The boost converter is widely used in the various topologies of the DC-DC converter in applications where the output voltage is higher than the input voltage such as photovoltaic applications, fuel cell applications and battery powered applications.

For conventional single-phase boost converters, the high-power level can be severely restricted by large input and output current ripple, high thermal stress on the individual components, and limited power density. These limitations have resulted in the development of the Three-Phase Interleaved Boost Converter which has three parallel boost phases whose gate signals are mutually phase shifted by 120° . The interleaved operation provides significant ripple cancellation, component stress reduction and overall converter efficiency improvement which is attractive for electric vehicle charging, photovoltaic systems and fuel cell interfaces.

The TPIB converter has some practical implementation issues, such as phase current unbalance due to mismatch of component parameters, deterioration in performance due to parasitic elements, and sensitivity to open switch failure that can result in severe current unbalance and potentially lead to converter failure.

To tackle these problems, this thesis presents modelling, control and fault tolerant operation of the TPIB converter under non-ideal circuit conditions. A PI voltage controller and Average Current Sharing technique are projected for controlled output voltage and stable phase current sharing, with a fault-tolerant strategy for open-switch faults. The whole project is confirmed through MATLAB/Simulink simulations.

1.1 DC-DC Converter

A DC-DC converter is a power electronic circuit that converts a DC voltage from one level to another by either stepping it up, stepping it down, or both. The controlled switching of semiconductor devices like MOSFETs or IGBTs, combined with energy storage elements such as inductors and capacitors are used to efficiently transfer and adjust energy from source to load.

The basic operating principle depends on the switching action of semiconductor devices at high frequencies, classically ranging from a few kilohertz to several megahertz. By governing the ON and OFF duration of the switch which is expressed as the duty cycle D . The average output voltage can be exactly regulated irrespective of dissimilarities in input voltage or load current.

DC-DC converters are classified into two main categories:

Non-isolated converters: These converters do not have galvanic isolation which makes them simple and efficient for many applications. Buck, Boost and Buck-Boost converters come under these converters. These converters give good efficiency and simple configuration of circuit which makes them appropriate for applications where galvanic isolation is not required.

Isolated converters: These converters have galvanic isolation such as Flyback, Forward, Push-Pull, and Full-Bridge converters. A high-frequency transformer provides electrical isolation between input and output, making them vital in safety-critical and high-voltage applications.

The DC-DC converter is evaluated in terms of voltage conversion ratio, efficiency, output voltage ripple, transient response, and power density. With the advancement of wide bandgap semiconductor devices such as Silicon Carbide (SiC) and Gallium Nitride (GaN), modern DC-DC converters attain efficiencies exceeding 95% even at high power levels. DC-DC converters have wide application in battery-powered portable electronics, electric vehicle drivetrains and photovoltaic energy systems, charging systems, fuel cell interfaces, and industrial automation. Their ability to regulate voltage precisely and efficiently under varying conditions makes them an important building block in every modern power electronic system.

1.2 Topologies of DC-DC Converters

The direction of voltage change, degree of electrical isolation, and amount of energy storage elements are three characteristics that are used to define topologies of DC-DC converters; applications determine which advantages specific topologies can offer.

Non-Isolated Topologies

The Buck, Boost, and Buck-Boost converters are the fundamental non-isolated topologies.

Buck converter: It is a step-down topology that generates an output voltage lower than the input. It consists of a switch, a freewheeling diode, an inductor, and an output capacitor. The voltage conversion ratio in Continuous Conduction Mode (CCM) is equal to the duty cycle D , i.e., $V_o = D.V_{in}$. It is broadly used in voltage regulator modules and battery charging applications.

Boost converter: It is a step-up topology that generates an output voltage higher than the input. Energy is stored in the inductor during the switch ON period and released to the output during the OFF period. The conversion ratio in CCM is $V_o = \frac{V_{in}}{(1-D)}$. It is commonly used

in power factor correction circuits, renewable energy interfaces and electric vehicle systems.

Buck-Boost converter: It can produce an output voltage either higher or lower than the input, but with reversed polarity. It is used in portable devices where the battery voltage varies above and below the required output. The conversion ratio is $V_o = -\frac{D.V_{in}}{(1-D)}$.

There are other advanced non-isolated topologies which include:

Cuk Converter: It provides non-inverted output with low input and output current ripple.

SEPIC Converter: Single-Ended Primary Inductance Converter, is capable of step up or step down with non-inverted output.

Interleaved Converters: These are parallel combination of multiple converter phases with phase-shifted switching and offers the considerably reduced current ripple and improved power handling.

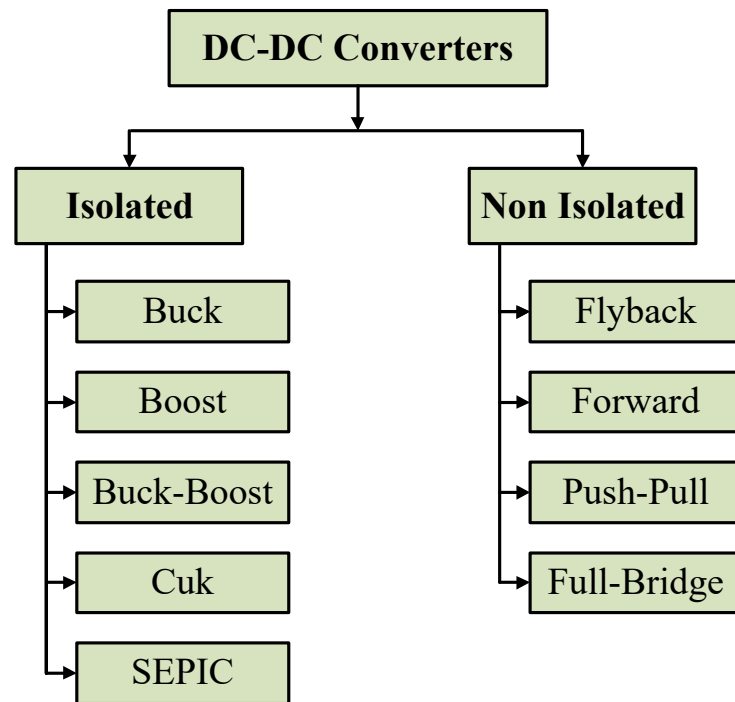


Figure 1.1 Different topologies of DC-DC Converter

Isolated Topologies

Isolated converters use a high-frequency transformer to deliver galvanic isolation between input and output, which is essential in telecommunication power supplies and off-board EV chargers.

Flyback Converter: It is derived from the Buck-Boost topology. It is simple and cost-effective for low-to-medium power applications.

Forward Converter: More efficient than Flyback at medium power levels.

Push-Pull Converter: Uses two switches with a center-tapped transformer for better power capability.

Full-Bridge Converter: Uses two switches with a center-tapped transformer for better power capability.

Among all the listed topologies the Interleaved Boost Converter is high current and high-power application the most efficient and reliable.

1.3 Three Phase Interleaved Boost (TPIB) Converter

The Three-Phase Interleaved Boost (TPIB) Converter is an advanced power conversion topology that consists of three distinct boost converter stages connected in parallel

between a common input source and a common output load. The duty cycles for all phases are the same, but the gate signals are 120° out of phase with each other, which gives a significant performance improvement over a conventional single phase boost converter. Each phase of the TPIB converter consists of an inductor, a MOSFET switch and a free-wheeling diode. The three phases share a common input voltage source V_{in} and a common output capacitor C_o across load resistance R . The interleaved PWM signals of the three switches are generated with a phase displacement of 120° from each other, so that the switching transitions of the three phases are evenly distributed within the switching period. Each individual phase operates on the same principle as a single-phase boost converter. When the switch is ON, the corresponding inductor stores energy from the input source. In the OFF time the inductor releases its stored energy to the output through the freewheeling diode. The current ripples of the three inductors are time-staggered due to the 120° phase displacement, and are therefore partially cancelled at the input and output terminals. Hence the ripple frequency of the total input current is three times the individual switching frequency and the peak-to-peak ripple magnitude is reduced significantly as compared to a single-phase converter.

The interleaved switching distributes the power handling over three phases, which alleviates the current stress on individual components and enables a more compact and thermally balanced converter design. The lower rms currents in each phase lead to lower conduction losses in the switches, diodes, and inductor windings, which in turn improves the overall efficiency. In addition, the effective inductance seen at the input and output is reduced because of the parallel connection of three inductors, resulting in faster dynamic response to load changes. However, the TPIB converter is subject to the phase current imbalance in non-ideal circuit conditions. The presence of multiple phases leads to higher control complexity. The open-switch fault can result in the loss of balanced operation. These challenges are the major motivation for the present research work.

1.4 Need of Current Balancing

In an ideal TPIB converter, the total input current is divided equally among the three phases, thus providing equal power sharing and uniform thermal distribution among the three phases. However, in practice several factors cause the current distribution among the

interleaved phases to be non-uniform and active current balancing becomes a necessary requirement for reliable converter operation. The current imbalance is often caused by component tolerances. Even within the same tolerance band, inductors, capacitors and switching devices can vary slightly in their electrical characteristics. Even a small difference in the inductance value between the three phases means that one phase is charging and discharging at a different rate than the others, thus resulting in unbalanced steady state currents.

The consequences of an imbalance in the phase currents are serious. Unequal current sharing causes hotspots in the phase with the highest current, which accelerates component degradation and can lead to premature converter failure. In addition, the present imbalance degrades the ripple cancellation property which is one of the major advantages of the interleaved topology, increasing the effective input and output current ripple and stressing the filter components.

Therefore, the balanced phase currents are not only desirable but also critical from reliability and efficiency point of view. To maximize the performance advantages of the three-phase interleaved topology under practical operating conditions, an active current balancing mechanism that continuously monitors and corrects phase current deviations is required.

1.5 Non-Ideal Circuit Condition

Theoretically, DC-DC converters are usually modelled under ideal assumptions, where the switching devices are assumed to be ideal, the passive components have no parasitic elements and all the connections of the circuit are lossless. However, real-world converters deviate significantly from these ideal conditions due to parasitic elements which are inherently associated with physical components. Performance, efficiency and control behaviour of the converter are greatly influenced by these non-ideal circuit conditions.

The most common parasitic in practical converters is the Equivalent Series Resistance (ESR) of inductors and capacitors. The ESR of an inductor is the resistance losses in the winding wire and core material. This resistance causes an additional voltage drop, which reduces the effective voltage available to energy storage, changes the slope of the inductor current and decreases the steady-state output voltage below its ideal value. In a similar way, the output capacitor ESR adds a voltage ripple component at the output which is directly

proportional to the output current ripple, thereby degrading the quality of the output voltage waveform.

To design control algorithms that take these non-ideal effects into account, and to understand the behaviour of the converters under practical operating conditions, it is crucial to develop a mathematical model that includes parasitic elements.

1.6 Problem statement

The Three-Phase Interleaved Boost Converter has significant performance advantages over conventional single-phase topologies. However, its practical application is limited by phase current imbalance due to mismatches in component parameters, performance degradation due to parasitic elements such as inductor equivalent series resistance (ESR), capacitor ESR, and MOSFET on-state resistance, and vulnerability to open-switch faults that may result in overcurrent, thermal runaway, and converter failure. However, the challenges are not simultaneously realizable by the traditional control strategies based on the ideal converter model. Thus, a clear need exists for a unified control scheme that is able to achieve phase current balancing under non-ideal circuit conditions and also to provide a fault-tolerant operation capability without compromising the output voltage regulation.

1.7 Research objective

The main objective of this project is to design and model a fault-tolerant (TPIB) converter that can preserve stable and balanced operation under practical parasitic values. This includes accurately as well as parasitic resistances of inductors and capacitors, which effect the current distribution and dynamic characteristics of the converter. A main goal is to make sure the proper current balancing between the three inductor legs using a synchronized control strategy that associates with PI-based voltage control loop with a current control loop. This method aims to get uniform current sharing, minimize overall current ripple, recover converter efficiency, and reduce stress on individual components. Maintaining a stable and controlled output voltage during unlike operating conditions while minimizing transient issues as overshoot, undershoot, and fast variations caused by load or input fluctuations is another important objective.

1.8 Organization of Thesis

The thesis is organized into 6 chapters

Chapter 1 includes detailed introduction of TPIB converter with its research objective and problem statement. Chapter 2 includes detailed literature review including current sharing, fault tolerant topology and application of TPIB converter. Chapter 3 includes modelling of TPIB converter with parasitic. Chapter 4 explains controller design, time and frequency response of TPIB converter. Chapter 5 includes fault tolerant operation with open switch technique. Chapter 6 includes result and discussion of system. Chapter 7 includes conclusion and future scope introduced topology.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

As technology is developing, the demand for efficient and consistent power conversion is getting more important than past. Power converters play an important role in every modern electronic system, acting as the bridge between different voltage levels, energy sources, and loads. Whether it's in small consumer equipment or large-scale industrial equipment, these converters make certain that energy is delivered with less distortions and with maximum efficiency. Interleaved boost converter is better than classic boost because of its ability to reduce current ripple, share the load across multiple phases, and improve efficiency. Interleaved converters are commonly used to enhance power handling capabilities and minimize output voltage ripple, it is important to keep proper phase balance to completely operate these benefits[1]. Fig. 1, represents three-phase interleaved boost (TPIB) converter in renewable energy-based DC grid. The PV panels supply power through DC-DC MPPT converter. The power generated by converter then stepped down using DC-DC converter and feeds different loads, such as DC appliances and electrolyzer. A bidirectional DC-DC converter is linked with battery energy storage system (BES) with DC bus letting charging and discharging for energy management[2]. This architecture allows efficient energy utilization, storage, and hydrogen production under varying solar conditions[3].

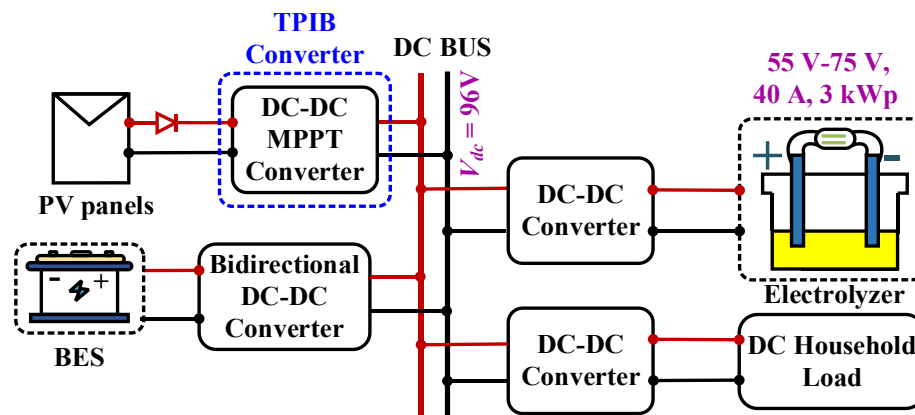


Figure 2.1 TPIB converter with fault tolerance in renewable energy-based system.

A three-phase interleaved boost (TPIB) converter is a step-up DC-DC converter. In this converter, the flow of current is through three inductors connecting in parallel with each other. With this it can handle increase in power and helps to eliminate overloading on individual element. But one of the challenges in this converter is to keep the current balanced in all three phases[4]. Heating, reduced efficiency, and even damage can be caused to the components if the currents aren't evenly shared in the circuit[5], [6]. To make the system work properly and to run for long time, we need to achieve proper current balancing[7], [8]. Different control strategies are used for this purpose current balancing i.e. hysteresis current control and average current balancing. Hysteresis current control method is used to maintain the inductor current within a defined upper and lower band around the reference[9]. When current reaches the upper limit, the switch is turned off, and when it reaches the lower limit, the switch is turned on. This gives very fast dynamic response and intrinsic current limiting. However, average current balancing compares the average values of the three phase currents and adjusts the control signals such that all currents intersect to a common reference over each switching cycle. This method guarantees long-term constant current distribution. The interleaved nature of the circuit reduces battery current ripple and the size of the solar PV side capacitor with increased current capability. It also provides fault-tolerant capability against open circuit switch faults (OCSFs)[10].

Research has been going on different types of fault techniques as well. There are various types of switching device faults that occurs in the power converters. The most common faults in switching devices are open circuit fault (OCF) and short circuit fault (SCF)[11], [12]. OCF has less damage risk because of low detection speed whereas SCF has high risk of causing component damage as it occurs because of overcurrent in the circuit and has fast detection process. Fault detection is achieved through real-time monitoring of inductor current slopes or voltage/current imbalances, enabling rapid identification of issues like open-circuit or short-circuit faults[13]. Though fault detection delays or uneven current sharing can temporarily affect efficiency, these adaptive mechanisms ensure graceful degradation, allowing the converter to power critical loads reliably. This fault resilience makes interleaved boost converters ideal for high-stakes applications like electric vehicles, renewable energy systems, and aerospace power supplies, where uninterrupted operation is paramount.

This chapter presents an organized analysis of the present literature in each of these

areas, recognizing the key contributions made by former researchers and highlighting the openings that inspire the present work.

2.2 DC-DC Converter

DC-DC converters are widely used in many industrial applications, including electric vehicles, aerospace, ships and renewable energy systems. The rapid growth of electric vehicles and renewable energy technologies has increased the need for reliable and efficient power conversion. Reliable power electronics systems are a widely discussed subject in the literature, and component failure, especially in semiconductor switches, is a major concern for converter design [14]. A survey of the reliability of power electronic converters in the industry showed that power semiconductor switch failures account for a significant percentage of the total number of converter failures, emphasizing the importance of effective fault management strategies in actual converter systems [15].

The circuit parasitic elements have a significant influence on the performance of the DC-DC converters. A comprehensive stability and sensitivity analysis showed that uniformly sampled DC-DC converters with parasitic elements such as inductor ESR, capacitor ESR, source resistance, diode forward voltage drop and MOSFET on-state voltage have a lower voltage conversion ratio but a more stable converter system due to the shifting of poles of the forward path transfer function away from the imaginary axis [16].

Digital controllers for DC-DC converters have had an increasing importance due to their flexibility, immunity to aging effects and easy implementation [17]. It has been proved that the stepped variation of the voltage gain due to the digital controller sampling frequency affects the stability of the converter, especially at higher duty ratios, for which the sensitivity of the voltage gain to the multisampling factor is much higher [18]. These results are directly applicable to the Three-Phase Interleaved Boost Converter which, in general, operates at relatively high duty cycles to realize the desired voltage step-up ratio.

2.3 Multiphase Interleaved Boost Converter

For high current and high-power density applications, multiphase interleaved DC-DC converters provide an efficient solution. An n-phase converter splits its input current into n phases. This feature allows the converter to manage higher currents with improved efficiency

and lower stress on the components. Additionally, interleaving the phase current ripples results in a reduced overall current ripple, and an increased ripple frequency. As a result, this may eliminate the need for additional filtering.

Interleaved converter topologies improve battery charging applications that implement power factor correction. The interleaved structure results in a significant increase in both charging efficiency and current quality, compared to traditional single-phase systems [19].

A four-port fault-tolerant DC-DC converter utilizing a two-phase interleaved boost topology, coupled with maximum power point tracking, was presented to reduce input current ripple. Detailed mathematical expressions for the input current ripple, considering different duty cycle regions, were developed. It was shown that employing phase interleaving results in the input current ripple becoming zero, at a duty cycle of 0.5, thus confirming the theoretical advantage of the interleaved topology [20].

The modeling and characterization of multiphase interleaved converters has been an area of keen research. The development of an open-circuit switch fault diagnosis and fault tolerant control of output-series interleaved boost DC-DC converters has shown that an accurate model of the behavior of the interleaved converter is a major contributor in developing effective fault detection and reconfiguration strategies [20]. A novel real time rapid fault tolerant diagnosis and compensation strategy for m-phase interleaved boost converters has demonstrated that the inherent redundancy of multiphase converters allows the converter to function, even with one or more phases failing, but with increased current stress and misaligned ripple in the remaining phases [21].

2.4 Current Sharing Technique

A new method for current sharing for low-voltage high-current voltage regulator modules shows that current balance can be accomplished with duty cycle modulation by the adjustment of phase current [22]. An adjustment method that involves no sensors analyses balance-control for multi-phase converters, while using the converter's own switching signals to measure phase currents [23].

Using one-current sensor current sharing and sensing for n-paralleled converters was analysed and a technique was established that regulates current while balancing the overhead

required for the multi-phase system [24]. Achieving current balance with the circuit in a state of interleaved DC-DC conversion with the use of a single DC-Link sensor was accomplished and compared to the reduction of sensor system requirements [25]. A balance and reconstruction system of the DC-Link currents for multi-phase coupled-inductor converters expanded the sensor techniques to interleaved Magnetically Coupled systems [26]. The use of a single current measuring sensor to reconstruct the phase currents for interleaved three-phase bidirectional converters was shown to be a feasible option for electric vehicles [27].

2.5 Fault-Tolerant Converter Topologies

With the demand for constant energy delivery for safety-critical applications, the need for fault tolerance on Power Electronics Converters has gained momentum. The detection of open-circuit faults on switching devices to ensure timely management is a necessity in the prevention of a catastrophic failure on the Converter. The unit magnitude of PWM phase-to-phase output voltages and the control effort gating signals are utilized in a recent study to detect, identify and locate faults in an interleaved, n-phase, buck converter. The faults studied include open-circuit switch faults and open-circuit diode faults [28]. The study showed that the developed algorithm is capable of the detection and localization of several open-circuit switch faults in one switching cycle. The detection and localization of open-circuit diode faults can also be achieved in one and a half switching cycles.

A rapid detection and localization algorithm was also developed to locate faults and open-circuit switch faults in interleaved three-phase buck converters [29]. This method was based on the analysis of the output PWM voltages and gating signals. It was shown that the switch fault causes the input current and phase inductor currents of the faulty phase to shrink to zero, while the healthy phases conduct in a dominating manner, and thus a fault signature is carried, which can be detected in a couple of switching intervals.

Using an observer-based method, an open-circuit switch fault diagnosis and fault-tolerant control method was developed for output-series interleaved boost DC-DC converters. This method controlled the inductor currents to detect faults, and then redistributed the load current among the healthy phases [19]. This method of open-circuit fault diagnosis for multi-phase floating DC-DC boost converters showed a rapid and an accurate fault detection method that is robust to parameter uncertainties and measurement noise, based on a sliding

mode observer [30].

Using residual state observer time-domain analysis coupled with an observer-based switch open-circuit diagnostic method for interleaved boost converters, fault detection has been achieved without the need for additional circuit hardware, other than that used for normal control of the converter [31],[32]. Several research studies focused on open-circuit fault diagnosis within interleaved DC-DC converters, as well as reconfiguration strategies to ensure sequential operational continuity after the failure of a converter phase. These studies have been extended to residential and commercial buildings, as well as DC microgrid systems, and have demonstrated the high practical applicability of interleaved converter fault tolerance designs [33], [34], [35]. The enhanced fault tolerance of converters, particularly in renewable energy systems where the source of energy may become completely depleted as a result of converter hardware failure, is extremely important. The systems of fault tolerance were demonstrated for photovoltaic and fuel cell stand-alone power supply systems through the development of rapid and effective power switch open-circuit fault detection systems for interleaved boost converters [36], [37]. Phase shifting control for three-phase interleaved boost converters [20], [38] was proposed to mitigate the effects of lost converter phases on the converter output voltage using fault-tolerance systems. Moreover, it has been shown that the interleaved boost converters have fault tolerance to keep the regulated output power after a fault in one of the converter phases. A fault-tolerant, solar photovoltaic supply system demonstrated that controlled output voltage at all ports can be upheld, even in fault conditions, through the inherent severance of the interleaved topology combined with the use of fault tolerant components [39], [18].

2.6 Parasitic Effect in Converter

Understanding how parasitic circuit elements affect the function of DC-DC converters is essential to the precise modelling and regulation of real-life converters. Numerous analyses of parasitic effects in DC-DC converters have helped show that including inductor ESR, capacitor ESR, source resistance, diode forward voltage, and the voltage drop across an active switch, create notable deviations in predicted characteristics such as the voltage conversion ratio, stability, and sensitivity [16]. The analysis indicated that parasitic ESR elements in boost converters affect the converter's voltage gain the most at higher duty cycles. This is

especially pertinent to the operation of the TPIB converter when employed in renewable energy applications.

A fault-tolerant single-switch DC-DC converter is designed to endure open and short-circuit switch catastrophes, the implanted parasitic effects into the converter design to set an appropriate fault detection threshold. A fault diagnosis approach for interleaved DC-DC converters was proposed on the basis of output voltage analysis, and showed that parasitic-induced deviations of output voltage waveforms can be used for the fault diagnosis of DC-DC converters in a reliable and simple manner [41].

2.7 Applications

The range of applications of the Three-Phase Interleaved Boost Converter that spans across almost all areas of power electronics can be best demonstrated in electric vehicle systems. Interleaved converter topologies have been extensively used within electric vehicles due to their high efficiency, low current ripple, and fault tolerant properties. The use of interleaved converters within the battery charging of electric vehicles with an improvement of the charging current quality and the overall system efficiency is an example [17].

In fault-tolerant interleaved converters, even when some switches are faulty, the objective of photovoltaic systems remains achievable, including the delivery of regulated output voltage and the maintenance of maximum power point tracking, particularly in applications involving solar energy, where reliability and continuous operation are especially important [18]. The deployment of fault tolerant interleaved converters in solar energy applications was validated by the development of a fault diagnosis and post-fault reconfiguration scheme for interleaved boost converters in photovoltaic systems [39].

Research in reference [36] demonstrates that in fuel cell power generation systems, efficient and fast fault detection algorithms can improve the reliability and availability of interleaved DC-DC boost converters. Their fault-tolerance capability is the key to protecting fuel cell stacks from damage caused by abnormal operating conditions. This research later extended this type of fault-tolerant design to standalone photovoltaic and fuel cell power systems equipped with floating interleaved topologies, and verified that the design is applicable across multiple types of renewable energy scenarios [37].

For DC microgrid applications, it has been shown that fault tolerant DC-DC

converters are critical in achieving continuous and reliable power delivery and that open-circuit fault diagnosis and reconfiguration strategies allow the microgrid to keep operating without interruption after failures of converter components [35]. Fault-tolerant interleaved boost converters have been shown to be practically implemented to provide reliable DC power conversion with minimal disruption during fault events for homes and offices applications [34].

CHAPTER 3

TPIB CONVERTER WITH PARASITIC

3.1 Introduction

With the widespread use of renewable energy systems, electric vehicles, fuel cell power systems and data centre power supplies, the demand for high efficiency, high power density DC-DC power conversion has increased rapidly. Conventional single phase boost converter is simple in design, but suffers from serious limitations in high current applications. Such limitations include high input and output current ripple, high thermal stress on a single set of components and limited power handling capability. These limitations have motivated the development of multiphase interleaved converter topologies as a better alternative for demanding power conversion applications.

Interleaving is the operation of multiple identical converter phases in parallel with the switching signals of the individual phases shifted in time by the same amount with respect to each other. In an N-phase interleaved converter the phase shift between adjacent phases is $360/N$ degrees, such that switching events are evenly spread over the switching period. This uniform distribution of switching events causes the current ripples of the individual phases to be distributed in time, thus causing a significant cancellation of ripple at the common input and output terminals of the converter. The ripple cancellation level improves with the number of phases and for the three-phase configuration the actual ripple frequency at input and output is three times the single-phase switching frequency.

The TPIB Converter is the most popular multiphase interleaved topology in power electronics practice, providing the best trade between circuit complexity and performance improvement. It is composed of three parallel boost converter stages with a common input source and common output capacitor and load. The three gate signals are mutually phase shifted by 120° . The TPIB converter is thoroughly discussed in this chapter, including the circuit description, operating principle, complete mathematical derivation of voltage gain and inductor current waveforms, ripple analysis, effects of parasitic elements, state space modelling, PI controller design, Average Current Sharing technique and fault-tolerant strategy.

3.2 Circuit Description of TPIB Converter

The Three-Phase Interleaved Boost Converter is formed with three separate boost converter phases in parallel, between a common DC input voltage source V_{pv} and a common output stage consisting of a filter capacitor C and load resistance R . Each phase $i = 1, 2, 3$ has an inductor L_i , a MOSFET switch S_i , and a free-wheeling diode D_i . These three phases are connected such that one terminal of each inductor is connected to the positive terminal of the input source while the other terminal is connected to the drain of the corresponding switch. The MOSFETs have their source connected to the negative ground and the freewheeling diodes have their anode connected to the junction between the inductor and the MOSFET drain. Each freewheeling diodes cathodes are connected together to the positive terminal of the output capacitor C , as well as in parallel with the load resistance R .

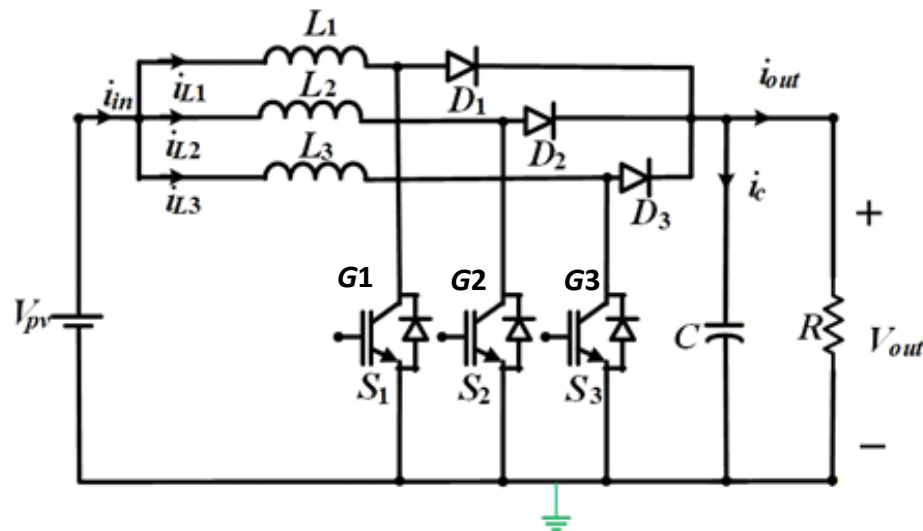


Figure 3.1: Circuit diagram of TPIB converter

The three switches S_1 , S_2 , and S_3 are driven by PWM signals G_1 , G_2 , and G_3 respectively, each switch is operating at the same switching frequency f_s with equal duty cycles D , but with a mutual phase displacement of 120° ($T/3$, where $T = 1/f_s$ is the switching period). This phase displacement is the main feature of the interleaved topology and it causes the ripple cancellation effect that makes the TPIB converter different from a simple parallel combination of three boost converters.

The circuit has three inductor currents i_{L1} , i_{L2} and i_{L3} , the output capacitor voltage V_C it is same as output voltage V_{out} under ideal conditions, and the total input current $i_m = i_{L1} + i_{L2} + i_{L3}$. In all the analyses presented in this chapter, the converter operates in Continuous Conduction Mode (CCM), i.e. none of the three inductor currents go to zero during normal steady-state operation.

3.3 Operating Principle and Modes of Operation

The fundamental working mechanism of each phase of the TPIB circuit is similar to that of a one-phase boost converter. In each phase, the phase switches alternatively from the ON position, where the respective phase's MOSFET is conducting, to the OFF position, where the MOSFET is not conducting. The three phases are operated using an equal duty cycle D but at evenly spaced switching instances, each spaced apart by $T/3$ in time.

Switch ON State (Charging Mode)

When the switch is ON, then diode will be reverse biased because of the high output voltage. The input voltage supply gets directly connected to the inductor, and hence, the current through it begins to rise linearly. The rate of change of the inductor current during its ON condition can be explained using Faraday's law of induction:

$$L \cdot \frac{di_{Li}}{dt} = V_{pv} \quad (3.1)$$

Here L is the inductance of each phase ($L_1 = L_2 = L_3 = L$ for the ideal case)

Integrating over the ON interval of duration $D \cdot T_s$:

$$\Delta i_{Li(rise)} = \left(\frac{V_{pv}}{L} \right) \cdot D \cdot T_s = \frac{V_{pv} \cdot D}{L \cdot f_s} \quad (3.2)$$

Here D is the duty cycle, T_s is the switching period, and f_s is the switching frequency

During the ON state, no current flows from phases to the output through diodes. The output capacitor alone supplies the load current during this interval for that particular phase.

Switch OFF State (Discharging Mode)

When switch is turned OFF, the inductor attempts to maintain its current, forcing diode into forward conduction. Both the input source and the inductor now supply energy to the output. The voltage across the inductor during the OFF state is:

$$L \cdot \frac{di_{Li}}{dt} = V_{pv} - V_{out} \quad (3.3)$$

Integrating over the OFF interval of duration $(1-D)T_s$:

$$\Delta i_{Li(fall)} = \left(\frac{V_{pv} - V_{out}}{L} \right) \cdot (1-D)T_s \quad (3.4)$$

Volt-Second Balance and Voltage Gain

In steady-state operation, the net change in inductor current over one complete switching period must be zero (volt-second balance principle). Setting the sum of the rising and falling current increments to zero:

$$\Delta i_{Li(rise)} + \Delta i_{Li(fall)} = 0 \quad (3.5)$$

$$\left(\frac{V_{pv}}{L} \right) \cdot DT_s + \left(\frac{V_{pv} - V_{out}}{L} \right) \cdot (1-D)T_s = 0 \quad (3.6)$$

Expanding and simplifying:

$$V_{pv} - V_{out}(1-D) = 0 \quad (3.7)$$

Solving for the voltage conversion ratio (voltage gain) of the ideal TPIB converter:

$$\frac{V_{out}}{V_{pv}} = \frac{1}{(1-D)} \quad (3.8)$$

This is the ideal boost converter essential voltage gain expression, in force for each phase of the TPIB converter

The duty cycle D required to achieve a desired output voltage V_{out} from a given input voltage V_{pv} is therefore:

$$D = 1 - \left(\frac{V_{pv}}{V_{out}} \right) \quad (3.9)$$

Steady-State Inductor Current

The average inductor current of steady state condition in each phase is determined by the power balance condition. By assuming ideal operation and identical current sharing among the three phases, the average inductor current per phase is:

$$I_{L_{avg}} = \frac{I_{out}}{3(1-D)} \quad (3.10)$$

Here, $I_{out} = \frac{V_{out}}{R}$ is the output current and R is the load resistance

Then again, from the input side, the total input current equals three times the per-phase inductor current, and from power balance $P_{pv} = P_{out}$:

$$V_{pv} \cdot I_{pv} = V_{out} \cdot I_{out} \quad (3.11)$$

$$I_{L_{avg}} = \frac{I_{pv}}{3} = \frac{V_{out} \cdot I_{out}}{3 \cdot V_{pv}} = \frac{V_{out}^2}{3 \cdot R \cdot V_{pv}} \quad (3.12)$$

Modes of Operation for Three-Phase Interleaved Configuration

The duty cycle D of three-phase interleaved configuration, the converter can operate in two different modes reliant on the value of D comparative to $\frac{1}{3}$ add $\frac{2}{3}$.

For $0 < D < \frac{1}{3}$: At this duty, at most one switch is ON and the other two are OFF. The overlapping of three switches never happens in their ON periods.

For $\frac{1}{3} < D < \frac{2}{3}$: At this duty, exactly one or two switches are concurrently ON. The two switches conduct concurrently during this time intervals.

For $\frac{2}{3} < D < 1$: At this duty, two or three switches may be at the same time ON.

For presented work, the converter operates at $D = 0.7$ which simultaneously falls in the range $\frac{2}{3} < D < 1$, meaning that two switches ON at the same time during a section of the switching

period. The specific switching sequence for the three phases with 120° phase shift is: G_1 leads G_2 , G_2 leads G_3 , and G_3 leads G_1 by $T/3$ simultaneously.

Since the converter contains the 3 active switches, so the converter operates are 8 switching modes.

Table 3.1 Switching Modes of TPIB converter

Mode	S_1	S_2	S_3
1	ON	ON	ON
2	ON	ON	OFF
3	ON	OFF	ON
4	OFF	ON	ON
5	ON	OFF	OFF
6	OFF	ON	OFF
7	OFF	OFF	ON
8	OFF	OFF	OFF

3.4 Mathematical Analysis and Voltage Gain

Inductor Current Waveform Derivation

Consider switch S_1 turned ON at time $t = 0$ and turned OFF at time $t = D.T_s$. The inductor current i_{L1} rises linearly from its minimum value $i_{L\min}$ to its maximum value $i_{L\max}$ during the ON period, and falls linearly back during the OFF period.

During ON period ($0 \leq t \leq D.T_s$):

$$i_{L1}(t) = i_{L\min} + \left(\frac{V_{pv}}{L} \right) t \quad (3.13)$$

During OFF period ($D.T_s \leq t \leq T_s$):

$$i_{L1}(t) = i_{L\max} + \left(\frac{V_{pv} - V_{out}}{L} \right) (t - D.T_s) \quad (3.14)$$

The inductor peak-to-peak current ripple for each phase is:

$$\Delta i_L = i_{L\max} - i_{L\min} = \frac{V_{pv} D}{L f_s} \quad (3.15)$$

Here Δi_L is the peak-to-peak ripple in each phase inductor current.

Total Input Current Ripple

The total input current i_{in} is the sum of the three phase currents:

$$i_{in} = i_{L1}(t) + i_{L2}(t) + i_{L3}(t) \quad (3.16)$$

As the three phase currents are same in wave form but shifted by $T/3$ from one another, the sum of those currents has cancellation in ripple effect. Ripple frequency of the total current that enters the system is $3f_s$. The peak-to-peak ripple of the total input current is dependent

upon the duty cycle. For $0 < D < \frac{1}{3}$:

$$\Delta i_{in} = \left(\frac{V_{pv}}{L} \right) \cdot D \cdot (1 - 3D) \cdot T_s \quad (3.17)$$

For $\frac{1}{3} < D < \frac{2}{3}$:

$$\Delta i_{in} = \left(\frac{V_{pv}}{L} \right) \cdot (2D - 1) \cdot (1 - D) \cdot \frac{T_s}{(1 - D)} \quad (3.18)$$

For $\frac{2}{3} < D < 1$:

$$\Delta i_{in} = \left(\frac{V_{pv}}{L} \right) \cdot (1 - D) \cdot (3D - 2) \cdot T_s \quad (3.19)$$

It can be seen that the maximum input current ripple of the interleaved topology decreases three times as compared to the single-phase boost configuration working at the same switching frequency, inductance value, and duty ratio. In other words, the ripple elimination occurs at the particular duty ratio value $D=1/3, 2/3$ in the three-phase case.

Output Voltage Ripple

The output voltage ripple of the TPIB converter depends on the ripple current into the output capacitor. The output capacitor current is the difference between the total diode current and the load current. Since the diode currents have an effective frequency of $3f_s$, the ripple of the output voltage is significantly reduced compared to a single-phase converter. The output voltage ripple peak-to-peak is roughly.

$$\Delta V_{out} \approx \frac{V_{out} \cdot D}{3RC \cdot f_s} \quad (3.20)$$

Here C is output capacitance, R is load resistance and f_s is switching frequency

It can be observed that the output voltage ripple of the TPIB converter is reduced by about a factor of 3 compared to the single-phase boost converter with the same component values, which verifies the advantage of the interleaved topology in reducing the output voltage ripple.

Inductor Design

The inductance value of each phase of the TPIB converter is chosen so that the inductor current ripple of each phase is limited to an acceptable portion of the average inductor current. The minimum inductance to obtain a specified maximum ripple $\Delta i_{L_{\max}}$ at the worst-case duty cycle is:

$$L_{\min} = \frac{V_{pv} \cdot D}{\Delta i_{L_{\max}} \cdot f_s} \quad (3.21)$$

The selected inductance of 330 μH per phase is selected on the practical basis of inductance size, current ripple, and transient speed.

Output Capacitor Design

The output capacitance is selected to limit the output voltage ripple to an acceptable percentage of the output voltage.

$$C_{\min} = \frac{V_{out} D}{3R \Delta V_{out_{\max}} \cdot f_s} \quad (3.22)$$

The selected capacitance of 220 μF provides a comfortable margin above the minimum required value, ensuring low output voltage ripple under all operating conditions.

3.5 Ripple Analysis and Cancellation

The ripple cancellation property of the Three-Phase Interleaved Boost Converter is one of its most important and distinctive characteristics. To understand this property quantitatively, consider the three inductor current waveforms i_{L1} , i_{L2} , i_{L3} , each having the same triangular waveform shape with the same amplitude and period, but mutually phase-shifted by $T/3$. Each current can be expressed as a Fourier series consisting of a DC component plus harmonics at frequencies $f_s, 2f_s, 3f_s$, etc.

For Phase 1, the inductor current can be written as:

$$i_{L1}(t) = i_{L_{avg}} + \sum \left[a_n \cos(2n \pi f_s t) + b_n \sin(2n \pi f_s t) \right] \quad (3.23)$$

For Phase 2 i.e. phase-shifted by $T/3$:

$$i_{L2}(t) = i_{Lavg} + \sum \left[an * \cos \left(2n * n * f_s * t - \frac{2\pi n}{3} \right) + an * \sin \left(2n * n * f_s * t - \frac{2\pi n}{3} \right) \right] \quad (3.24)$$

For Phase 3 i.e. phase-shifted by $2T/3$:

$$i_{L3}(t) = i_{Lavg} + \sum \left[an * \cos \left(2n * n * f_s * t - \frac{4\pi n}{3} \right) + an * \sin \left(2n * n * f_s * t - \frac{4\pi n}{3} \right) \right] \quad (3.25)$$

The total input current is the sum of the three phase currents:

$$i_{in}(t) = i_{L1}(t) + i_{L2}(t) + i_{L3}(t) \quad (3.26)$$

For any harmonic of order n , the sum of three sinusoids with equal amplitude and mutual phase shifts of $\frac{2\pi n}{3}$ is:

$$\cos \theta + \cos \left(\theta - \frac{2\pi n}{3} \right) + \cos \left(\theta - \frac{4\pi n}{3} \right) = 0 \text{ for } n \neq 3k \quad (3.27)$$

$$\cos \theta + \cos \left(\theta - \frac{2\pi n}{3} \right) + \cos \left(\theta - \frac{4\pi n}{3} \right) = 3 \cos \theta \text{ for } n = 3k \quad (3.28)$$

Here k is any positive integer ($k = 1, 2, 3, \dots$)

This mathematical result shows that all harmonics of the individual phase currents are completely cancelled in the total input current except those whose order is a multiple of 3 (i.e., harmonics at frequencies $3f_s, 6f_s, 9f_s, \dots$). The fundamental switching frequency component (f_s) and its non-triple harmonics ($2f_s, 4f_s, 5f_s, \dots$) are totally cancelled. Thus, the minimum harmonic frequency contained in the total input current is $3f_s$, which is three times the individual phase switching frequency. This effectively triplicates the ripple frequency, which greatly reduces the required filter component size. At $3f_s$, the capacitor impedance is 3 times less than at f_s .

To systematically investigate the ripple cancellation property of TPIB converter, the phase currents are characterized using Fourier series expansion. Due to the phase displacement between phases are 120° , harmonic cancellation happens according to the trigonometric identities given in (3.27) and (3.28) [42].

The degree of ripple cancellation is quantified by the ripple reduction factor, defined as the ratio of the peak-to-peak input current ripple of the three-phase interleaved converter to that of a single-phase converter with the same parameters,

$$\text{Ripple Reduction Factor} = \frac{\Delta i_{in3\phi}}{\Delta i_{in1\phi}} \quad (3.29)$$

The ripple cancellation is most effective when the duty cycle is close to 2/3 or 1/3, at which points the ripple in the total input current approaches zero. For $D = 0.7$ (near by 2/3), important ripple reduction is attained compared to the single-phase case.

3.6 Effect of Parasitic Elements

The ideal analysis given in the previous sections assumes that all circuit components are ideal and lossless. The parasitic elements of each physical part cause the converter behavior to deviate from the ideal one. The parasitic elements of the TPIB converter that are most important are the equivalent series resistance (ESR) of the inductors (r_{L1}, r_{L2}, r_{L3}), the ESR of the output capacitor (r_C), and the on-state resistance of the MOSFET switches. Understanding the effects of these parasitic is important for accurate converter design and control.

Effect of Inductor ESR

Each real inductor has a resistance in the winding due to the finite conductivity of the wire used to make it. This winding resistance, called r_{Li} for phase i , is a series resistance in the inductor branch.

During the ON state with switch S_i closed, the voltage across inductor L_i is reduced by the voltage drop across r_{Li} is

$$L_i \frac{di_{Li}}{dt} = V_{pv} - r_{Li} \cdot i_{Li} \quad (3.30)$$

During the OFF state with switch S_i open, both the input source and the output voltage appear across the inductor-resistance series combination:

$$L_i \frac{di_{Li}}{dt} = V_{pv} - V_{out} - r_{Li} \cdot i_{Li} \quad (3.31)$$

By applying volt-second balance to the averaged inductor, we get,

$$D * (V_{in} - D(V_{pv} - r_{Li} \cdot i_{Li})) + (1 - D)(V_{pv} - V_{out} - r_{Li} \cdot i_{Li}) = 0 \quad (3.32)$$

The per-phase DC inductor current for the winding resistance is get by solving the power balance equation:

$$i_{Li} = \frac{(V_{pv} - (1-D)V_{out})}{r_{Li}} \quad (3.33)$$

In a three-phase interleaved converter with unequal winding resistances ($r_{L1} \neq r_{L2} \neq r_{L3}$), the per-phase currents will be unequal even when the same duty cycle D is applied to all phases. The highest current is carried by phase with the lowest winding, and vice versa. In practical TPIB converter the fundamental cause of current imbalance inspires the need for control of active current sharing.

Effect of Capacitor ESR

The equivalent series resistance r_C of the output capacitor contains an extra component of output voltage ripple that is proportional to the flow of ripple current through the capacitor. The total output voltage ripple with capacitor ESR is the sum of the ripple due to capacitor charge/discharge and the ripple due to the resistive voltage drop across r_C :

$$\Delta V_{out(total)} = \Delta V_{out(capacitive)} + \Delta V_{out(ESR)} \quad (3.34)$$

$$\Delta V_{out(ESR)} = r_C \cdot \Delta i_C \quad (3.35)$$

Here Δi_C is the peak-to-peak ripple current through the output capacitor C .

Modified Voltage Gain with All Parasitic

In the case of balancing the modified voltage gain of the TPIB converter is derived using the complete averaged model by taking the inductor ESR, capacitor ESR and assuming equal parasitic parameters for all three phases. The analysis is based on a full volt-second balance and charge balance.

$$V_{out} \approx \frac{V_{pv}}{(1-D)} \cdot \left[1 - \frac{r_L}{R \cdot (1-D)^2} \right] \quad (3.36)$$

This expression clearly demonstrates that the voltage gain of the practical converter is always lower than the ideal value $1/(1-D)$, and the deviation increases with the increase in the inductor ESR r_L or decrease in the load resistance R i.e., at higher load currents. The voltage gain also decreases as D tends towards 1. This is because the denominator term $\frac{r_L}{R \cdot (1-D)^2}$ becomes very large at high duty cycles.

Efficiency with Parasitic

The overall conversion efficiency of the TPIB converter accounting for inductor copper losses is derived from the ratio of output power to input power:

$$\eta = \frac{P_{out}}{P_{pv}} = \frac{V_{out} \cdot I_{out}}{V_{pv} \cdot I_{pv}} \quad (3.37)$$

The total power loss due to inductor ESR in all three phases is:

$$Pr_L = r_{L1} \cdot i_{L1}^2 + r_{L2} \cdot i_{L2}^2 + r_{L3} \cdot i_{L3}^2 \quad (3.38)$$

For the case of balanced currents ($i_{L1} = i_{L2} = i_{L3} = i_L$):

$$Pr_L = 3 * r_{Lavg} \cdot i_L^2 \quad (3.39)$$

where $r_{Lavg} = \frac{r_{L1} + r_{L2} + r_{L3}}{3}$ is the average winding resistance

Therefore, efficiency is,

$$\eta = \frac{P_{out}}{P_{out} + Pr_L} = \frac{1}{1 + \frac{3r_{Lavg} \cdot i_L^2}{P_{out}}} \quad (3.40)$$

This expression confirms that when the winding resistance decreases the efficiency improves and as the output power increases.

3.7 TPIB converter with parasitic

An IBC without parasitic elements works under ideal state, where components like inductors, capacitors, switches and diodes are assumed to be lossless and ideal. In this ideal case, the converter attains high voltage gain controlled by the duty cycle, reduced input current ripple, and balancing of current in the phases due to perfect synchronization and uniformity. The interleaving technique maximize the ripple frequency by three times in a 3-phase configuration, significantly minimizing the magnitude of ripple currents and voltages, so that smaller filter components and better power quality can be attained. As there will be no resistive losses so, the overall system efficiency remains high and voltage drops across the switches and diodes are almost negligible. However, in practical converters, parasitic elements such as inductor winding resistance and capacitor equivalent series resistance (ESR) introduce extra resistive and conduction losses. These parasitic resistances decrease the effective voltage gain by causing voltage drops during switching and conduction periods. Subsequently, the output voltage is lesser than the ideal estimate for the similar duty cycle. The

effectiveness of the converter reduces because power losses as heat in the parasitic resistances. The parasitic can affect the ripple by increasing input current and output voltage ripples, and can create unbalanced current distribution between the three phases, exposing unequal thermal loading.

The schematic diagram of the IBC converter with parasitic is illustrated in Fig. 3.1, showcasing a three-phase interleaved boost converter. The three-phase IBC include three parallel boost converter legs connected at input and output in the circuit. Each leg consists inductor (L_1, L_2, L_3) with parasitic resistances (r_{L1}, r_{L2}, r_{L3}), power switches (S_1, S_2, S_3) and diodes (D_1, D_2, D_3). The output is connected to common capacitance C with equivalent series resistance (ESR) r_c across load R . The three switches are controlled by PWM signals shifted 120° w.r.t. each other. The current passes through three parallel inductor legs are i_{L1} , i_{L2} and i_{L3} , capacitor is i_c and load is i_{out} .

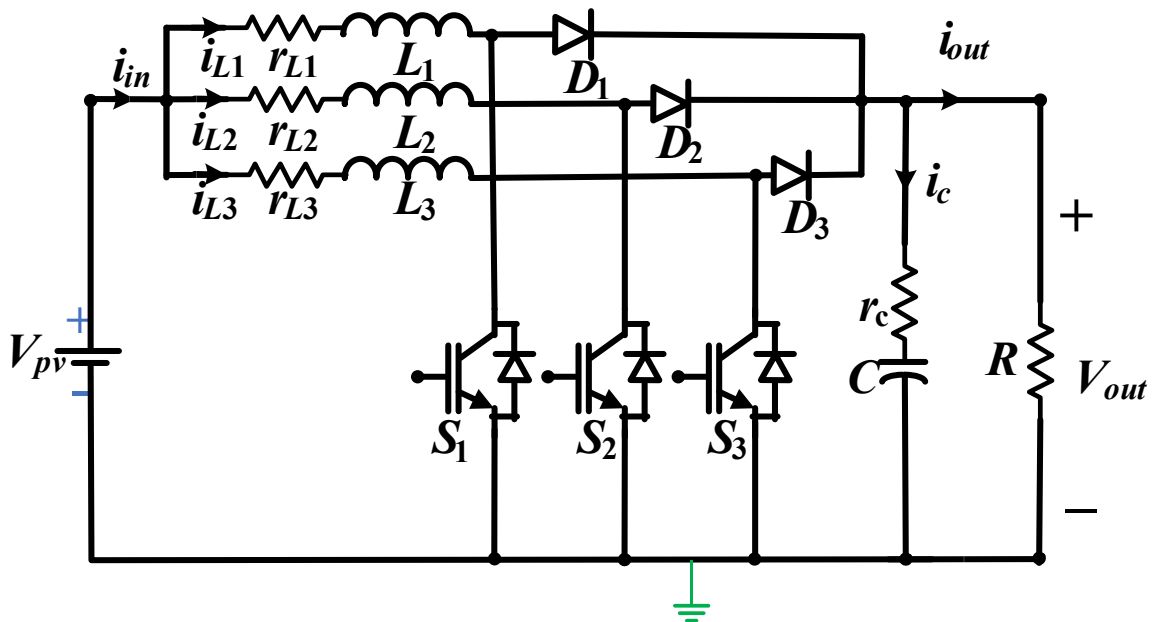


Figure 3.2 Circuit diagram of TPIB converter with circuit parasitic.

Here, Input voltage is V_{pv} i.e. DC source. D is duty cycle. T_s is switching period. To define the different legs of inductor in the equation value n is defined where $n=1,2,3$. TPIB converter is assumed to be in Continuous conduction mode (CCM) for all inductors. The output voltage is given by.

$$V_{out} = \frac{V_{pv}}{1-D} \quad (3.41)$$

3.8 Mathematical Modelling of TPIB Converter

The TPIB Converter includes Inductor parasitic resistances i.e. r_{L1}, r_{L2}, r_{L3} , Capacitor ESR r_c , Output capacitance C , Load resistance R .

The duty ratios of the three phases are defined as:

$$d_1 = D + \hat{d}_1 \quad (3.42)$$

$$d_2 = D + \hat{d}_2 \quad (3.43)$$

$$d_3 = D + \hat{d}_3 \quad (3.44)$$

Where D is steady-state duty cycle, $\hat{d}_i$ is small perturbation in duty cycle

The state variables are,

$$x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_{out} \end{bmatrix} \quad (3.45)$$

Switch ON-State Equations

In IBC each leg operates in two states i.e. switch on state and switch off state. In switch on state also called charging mode of inductor. When switch of a particular phase is ON, the corresponding diode becomes reversed biased and the inductor stores energy.

Applying KVL for phase 1:

$$V_{pv} = V_{L1} + V_{rL1} \quad (3.46)$$

Since,

$$V_{L1} = L_1 \frac{di_{L1}}{dt} \quad (3.47)$$

$$V_{rL1} = r_{L1} i_{L1} \quad (3.48)$$

Therefore,

$$L_1 \frac{di_{L1}}{dt} = \frac{V_{pv} - r_{L1} i_{L1}}{L_1} \quad (3.49)$$

Similarly,

$$L_2 \frac{di_{L2}}{dt} = \frac{V_{pv} - r_{L2}i_{L2}}{L_2} \quad (3.50)$$

$$L_3 \frac{di_{L3}}{dt} = \frac{V_{pv} - r_{L3}i_{L3}}{L_3} \quad (3.51)$$

Capacitor equation during ON-state

During ON-state, the load is supplied only by the capacitor

By applying KCL, we can get capacitor current,

$$i_C = -i_{out} \quad (3.52)$$

Output current as,

$$i_{out} = \frac{V_{out}}{R} \quad (3.53)$$

$$i_C = -\frac{V_{out}}{R} \quad (3.54)$$

Considering capacitor ESR,

$$V_{out} = V_C + r_C i_C \quad (3.55)$$

$$V_{out} = V_C - r_C \frac{V_{out}}{R} \quad (3.56)$$

Hence,

$$V_{out} = \frac{V_C}{1 + \frac{r_C}{R}} \quad (3.57)$$

Now,

$$i_C = C \frac{dV_C}{dt} \quad (3.58)$$

By substituting V_{out} , we get,

$$C \frac{dV_C}{dt} = -\frac{V_{out}}{R} \quad (3.59)$$

$$\frac{dV_C}{dt} = -\frac{V_C}{RC \left(1 + \frac{r_C}{R}\right)} \quad (3.60)$$

During this interval, no current flows from particular leg to the output. The output capacitor alone supplies the current to the load.

Switch off state equations

In switch off state also called discharging mode of inductor, the energy in the inductor is dissipate through the diode into output stage.

Applying KVL for phase-1,

$$V_{pv} = V_{L1} + V_{rL1} + V_{out} \quad (3.61)$$

$$L_1 \frac{di_{L1}}{dt} = V_{pv} - V_{out} - r_{L1} i_{L1} \quad (3.62)$$

$$\frac{di_{L1}}{dt} = \frac{V_{pv} - V_{out} - r_{L1} i_{L1}}{L_1} \quad (3.63)$$

Similarly,

$$\frac{di_{L2}}{dt} = \frac{V_{pv} - V_{out} - r_{L2} i_{L2}}{L_2} \quad (3.64)$$

$$\frac{di_{L3}}{dt} = \frac{V_{pv} - V_{out} - r_{L3} i_{L3}}{L_3} \quad (3.65)$$

In this mode, both the input source and inductor supply energy to load, giving boosted output voltage. As three switched are operating in 120° phase shifts, at any period of time at least one phase will be delivering energy to load. This gives smoother current waveform and reduced ripple.

Capacitor equation during OFF-state

Applying KVL for phase-1

$$i_C = i_{L1} - i_{out} \quad (3.66)$$

$$i_{out} = \frac{V_{out}}{R} \quad (3.67)$$

$$i_C = i_{L1} - \frac{V_{out}}{R} \quad (3.68)$$

Using ESR relation,

$$V_{out} = V_C + r_C i_C \quad (3.69)$$

$$V_{out} = V_C + r_C \left(i_{L1} - \frac{V_{out}}{R} \right) \quad (3.70)$$

$$V_{out} = \frac{V_C + r_C i_{L1}}{1 + \frac{r_C}{R}} \quad (3.71)$$

$$i_C = C \frac{dV_C}{dt} \quad (3.72)$$

$$C \frac{dV_C}{dt} = i_{L1} - \frac{V_{out}}{R} \quad (3.73)$$

Substituting V_{out} , we get,

$$C \frac{dV_C}{dt} = i_{L1} - \frac{1}{R} \left(\frac{V_C + r_C i_{L1}}{1 + \frac{r_C}{R}} \right) \quad (3.74)$$

State Space Averaging equation

Using state-space averaging equation,

$$\dot{x} = d(x_{ON}) + (1-d)(x_{OFF}) \quad (3.75)$$

For phase-1,

$$\frac{di_{L1}}{dt} = d_1 \left(\frac{V_{pv} - r_{L1} i_{L1}}{L_1} \right) + (1-d_1) \left(\frac{V_{in} - V_{out} - r_{L1} i_{L1}}{L_1} \right) \quad (3.76)$$

$$\frac{di_{L1}}{dt} = \left(\frac{V_{in} - (1-d_1)V_{out} - r_{L1} i_{L1}}{L_1} \right) \quad (3.77)$$

Similarly,

$$\frac{di_{L2}}{dt} = \left(\frac{V_{in} - (1-d_2)V_{out} - r_{L2} i_{L2}}{L_2} \right) \quad (3.78)$$

$$\frac{di_{L3}}{dt} = \left(\frac{V_{in} - (1-d_3)V_{out} - r_{L3} i_{L3}}{L_3} \right) \quad (3.79)$$

The averaged capacitor equations,

$$\frac{dV_C}{dt} = k_C (1-D)(i_{L1} + i_{L2} + i_{L3}) - \frac{k_C}{R} V_C \quad (3.80)$$

$$\text{Here, } k_C = \frac{R}{R + r_C}$$

Small-Signal Modelling

The perturbation variables are defined as

$$i_{L1} = I_{L1} + \hat{i}_{L1} \quad (3.81)$$

$$i_{L2} = I_{L2} + \hat{i}_{L2} \quad (3.82)$$

$$i_{L3} = I_{L3} + \hat{i}_{L3} \quad (3.83)$$

$$V_{out} = V_O + \hat{v}_O \quad (3.84)$$

$$V_C = V_C + \hat{v}_c \quad (3.85)$$

From equation (3.42), (3.43), (3.44) we can write different duty.

By substituting these equations into averaged equations and neglecting second-order perturbation terms yields the linearized small-signal equations.

For phase-1,

$$L_1 \frac{d\hat{i}_{L1}}{dt} = \hat{v}_{pv} - (1 - D_1) \hat{v}_O + V_O \hat{d}_1 - r_{L1} \hat{i}_{L1} \quad (3.86)$$

Similarly, for phase-2 and phase-3

$$L_2 \frac{d\hat{i}_{L2}}{dt} = \hat{v}_{pv} - (1 - D_2) \hat{v}_O + V_O \hat{d}_2 - r_{L2} \hat{i}_{L2} \quad (3.87)$$

$$L_3 \frac{d\hat{i}_{L3}}{dt} = \hat{v}_{pv} - (1 - D_3) \hat{v}_O + V_O \hat{d}_3 - r_{L3} \hat{i}_{L3} \quad (3.88)$$

Capacitor Equation

$$i_C = (1 - D)(i_{L1} + i_{L2} + i_{L3}) - \frac{V_{out}}{R} \quad (3.89)$$

$$C \frac{dV_C}{dt} = (1 - d_1) i_{L1} + (1 - d_2) i_{L2} + (1 - d_3) i_{L3} - \frac{V_{out}}{R} \quad (3.90)$$

$$C \frac{d(V_C + \hat{v}_c)}{dt} = (1 - D_1 - \hat{d}_1)(I_{L1} + \hat{i}_{L1}) + (1 - D_2 - \hat{d}_2)(I_{L2} + \hat{i}_{L2}) + (1 - D_3 - \hat{d}_3)(I_{L3} + \hat{i}_{L3}) - \frac{V_{out} + \hat{v}_{out}}{R} \quad (3.91)$$

For steady state equation all DC terms will cancel and becomes equal to zero.

$$C \frac{dV_C}{dt} = (1 - D_1)(I_{L1}) + (1 - D_2)(I_{L2}) + (1 - D_3)(I_{L3}) - \frac{V_{out}}{R} = 0 \quad (3.92)$$

$$C \frac{d\hat{v}_c}{dt} = (1 - D_1)(\hat{i}_{L1}) - I_{L1} \hat{d}_1 + (1 - D_2)(\hat{i}_{L2}) - I_{L2} \hat{d}_2 + (1 - D_3)(\hat{i}_{L3}) - I_{L3} \hat{d}_3 - \frac{\hat{v}_{out}}{R} \quad (3.93)$$

By putting ESR with capacitor we get,

$$C \frac{d\hat{v}_c}{dt} = \sum_{k=1}^3 \left[(1-D_k) \hat{i}_{Lk} - I_{Lk} \hat{d}_k \right] - \frac{\hat{v}_{out}}{R} \quad (3.94)$$

The state space equations are,

$$\dot{x} = Ax + Bu \quad (3.95)$$

$$\hat{v}_o = \hat{v}_c + \hat{r}_c \hat{i}_c \quad (3.96)$$

By assuming $D_1 = D_2 = D_3 = D$

$$L_1 \frac{d\hat{i}_{L1}}{dt} = -(1-D) \hat{v}_o + V_o \hat{d}_1 - r_{L1} \hat{i}_{L1} \quad (3.97)$$

$$L_1 \frac{d\hat{i}_{L1}}{dt} = -(1-D) \hat{v}_c - r_c (1-D) \hat{i}_c + V_o \hat{d}_1 - r_{L1} \hat{i}_{L1} \quad (3.98)$$

By solving we get,

$$L_1 \frac{di_{L1}}{dt} = V_{pv} - r_{L1} i_{L1} - (1-D) k_c v_c - r_c k_c (1-D) (i_{L1} + i_{L2} + i_{L3}) \quad (3.99)$$

Similarly,

$$L_2 \frac{di_{L2}}{dt} = V_{pv} - r_{L2} i_{L2} - (1-D) k_c v_c - r_c k_c (1-D) (i_{L1} + i_{L2} + i_{L3}) \quad (3.100)$$

$$L_3 \frac{di_{L3}}{dt} = V_{pv} - r_{L3} i_{L3} - (1-D) k_c v_c - r_c k_c (1-D) (i_{L1} + i_{L2} + i_{L3}) \quad (3.101)$$

$$C \frac{dv_c}{dt} = (1-D) k_c (i_{L1}) + (1-D) k_c (i_{L2}) + (1-D) k_c (i_{L3}) - \frac{k_c}{RC} \quad (3.102)$$

Space state matrix from above equations is

$$A = \begin{bmatrix} -\frac{r_{L1} + r_c k_c (1-D)}{L_1} & -\frac{r_c k_c (1-D)}{L_1} & -\frac{r_c k_c (1-D)}{L_1} & -\frac{(1-D) k_c}{L_1} \\ -\frac{r_c k_c (1-D)}{L_2} & -\frac{r_{L2} + r_c k_c (1-D)}{L_2} & -\frac{r_c k_c (1-D)}{L_2} & -\frac{(1-D) k_c}{L_2} \\ -\frac{r_c k_c (1-D)}{L_3} & -\frac{r_c k_c (1-D)}{L_3} & -\frac{r_{L3} + r_c k_c (1-D)}{L_3} & -\frac{(1-D) k_c}{L_3} \\ \frac{(1-D) k_c}{C} & \frac{(1-D) k_c}{C} & \frac{(1-D) k_c}{C} & -\frac{k_c}{RC} \end{bmatrix} \quad (3.103)$$

$$B = \begin{bmatrix} \frac{1}{L_1}(V_o - r_c k_c (I_{L1} + I_{L2} + I_{L3})) \\ \frac{1}{L_2}(V_o - r_c k_c (I_{L1} + I_{L2} + I_{L3})) \\ \frac{1}{L_3}(V_o - r_c k_c (I_{L1} + I_{L2} + I_{L3})) \\ -\frac{(I_{L1} + I_{L2} + I_{L3})}{C} \end{bmatrix} \quad (3.104)$$

Output equation,

$$y = Cx + Du \quad (3.105)$$

$$C = [r_c k_c (1 - D_1) \quad r_c k_c (1 - D_2) \quad r_c k_c (1 - D_3) \quad k_c] \quad (3.106)$$

The transfer function is derived from

$$G(s) = C(sI - A)^{-1} B + D \quad (3.107)$$

By applying formula to the matrix and putting the values, we get fourth-order control-to-output transfer function.

$$G(s) = \frac{\Delta V_{out}(s)}{\Delta D(s)} = \frac{-2.466 \times 10^4 s^3 + 8.915 \times 10^8 s^2 + 1.882 \times 10^{12} s + 8.963 \times 10^{14}}{s^4 + 3120 \times 10^3 s^3 + 6.661 \times 10^6 s^2 + 8.234 \times 10^9 s + 3.428 \times 10^{12}} \quad (3.108)$$

This transfer function is the fourth order system which contains the four variables i.e. three inductor currents and one capacitor voltage. The numerator of TF is third order which introduces three finite zeros.

3.9 Conclusion

This chapter concludes about TPIB converter synthesis with and without ESR values. It also presents the modelling of TPIB with parasitic. This chapter elaborates the modelling with average values, small signal values and transfer Function of TPIB converter with ESR.

CHAPTER 4

CONTROLLER DESIGN OF TPIB CONVERTER

4.1 Introduction

The control of the Three-Phase Interleaved Boost (TPIB) converter requires a systematic approach that links the mathematical model of the physical plant and the practical needs of stable voltage regulation, phase current sharing and robustness to load and parameter variations. In chapter 3, we derived the state-space model of the TPIB converter including parasitic elements. In this chapter we will use the derived model to make a complete controller design study. The procedure begins from the identification of the steady-state operating point and then linearization of the converter model to a small signal state space representation. The derived linear model is then analyzed using its poles, zeros, natural frequencies and damping ratios to obtain an insight into the open loop dynamic behavior of the converter.

Based on this open-loop analysis, a Proportional-Integral (PI) controller is designed to achieve the desired closed-loop performance specifications. The simulation of the design is verified in the frequency domain analysis with bode plots, Nyquist plots, gain and phase margin calculations and in the time domain analysis of the closed loop step response. Sensitivity to load variation is also studied to verify the robustness of the designed controller at various operating conditions. All analyses and results presented in this chapter are obtained from the derived state-space model using the MATLAB-based linear systems toolbox.

4.2 Controller Design for Balancing of Current In IBC

The closed-loop output voltage control algorithm for the TPIB converter is presented in Fig. 3.2, The output voltage V_{out} is feedback to sum block and equated to the reference voltage V_{ref} to generate an error signal, and then it is fed to the PI controller to generate the duty ratio D . The two duty ratios are compared with 120° phase-shifted triangular carrier waves having system frequency to generate the gating pulses G_1 , G_2 , G_3 , respectively.

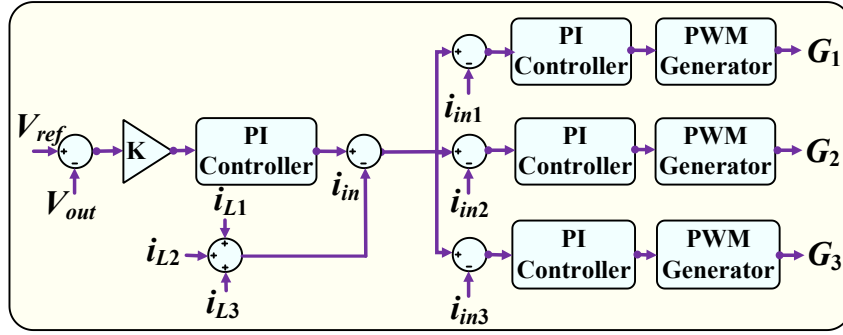


Figure 4.1 Closed-loop control of TPIB converter with phase current balance in voltage control mode.

A dual-loop control scheme is used to maintain both output voltage regulation and current balancing. For voltage control, the output voltage V_{out} is compared against the reference V_{ref} . The error signal passes through a PI controller

$$i_{ref} = K_p (V_{ref} - V_{out}) + K_i \int (V_{ref} - V_{out}) dt \quad (4.1)$$

Here K_p is the proportional gain and K_i is integral gain of PI controller. The total reference current is generated using eq. which maintains the desired output voltage. For current balancing control, the average current is calculated as

$$i_{avg} = \frac{i_{L1} + i_{L2} + i_{L3}}{3} \quad (4.2)$$

The current error for each leg is,

$$e_n = \frac{i_{ref}}{3} - i_n \quad (4.3)$$

The error is processed by a PI controller to adjust duty cycle of respective phase. This makes sure that current in all three inductors are equal and eliminates the mismatches due to parasitic.

The PI controller is designed by using small-signal transfer function which is obtained from the state-space averaged model of the converter. The transfer function is represented by dynamic relationship between duty cycle variation and output voltage variation. The TF of TPIB converter is expressed from equation (3.108).

This transfer function is the fourth order system which contains the four variables i.e. three inductor currents and one capacitor voltage. The numerator of TF is third order which

introduces three finite zeros. The existence of right-half plane (RHP) zero at approximately 38,186 rad/s is characteristic property of boost converter which shows the non-minimum phase behavior causing from sudden withdrawal of inductor current from output when the switch is on.

Table 4.1 Poles and Zeros of Open-Loop Transfer Function

Type	Location (rad/s)	Remarks
Pole 1	$-531.2 + j1790.3$	Complex conjugate pair
Pole 2	$-531.2 + j1790.3$	Complex conjugate pair
Pole 3	-1312.4	Real pole
Pole 4	-749.0	Real pole
Zero 1	$+38178$	RHP zero (non-minimum phase)
Zero 2	-1280	LHP zero
Zero 3	-744	LHP zero

All four poles lie in the left-half-plane (LHP), that confirms that the open-loop plant is stable. The complex conjugate pole pair $-531.2 + j1790.3$ rad/s is the dominant pole pair that shows the oscillatory transient behavior, whereas the real poles at -749 and -1312.4 rad/s shows the lag.

The PI controller transfer function is $C_{PI(s)} = K_p + \frac{K_i}{s}$. The initial controller begins with pure integrator design to show the integral gain that achieves the required low-frequency loop gain. The root locus and frequency-domain synthesis shows as initial integral gain i.e. 1.8878. This integral controller provides infinite gain at DC, confirming zero steady-state error, but also offers limited phase margin and bandwidth. A proportional term is used to improve the phase margin and the transient response speed.

After frequency-domain optimization the PI parameters are used to achieve the target bandwidth and stability margins.

Table 4.2 Final PI Controller Parameters

Controller Parameters	Symbol	Values
Proportional Gain	K_p	0.0020
Integral Gain	K_i	1.8878
Closed-Loop Bandwidth	BW	739.25 rad/s

The relatively small K_p shows the high open-loop gain of the converter plant at low frequencies, whereas the K_i provides the loop gain. The K_i is chosen to get the desired closed-loop bandwidth while maintaining the required stability margins. Fig. 4.2 shows the closed loop Bode plot of TPIB converter.

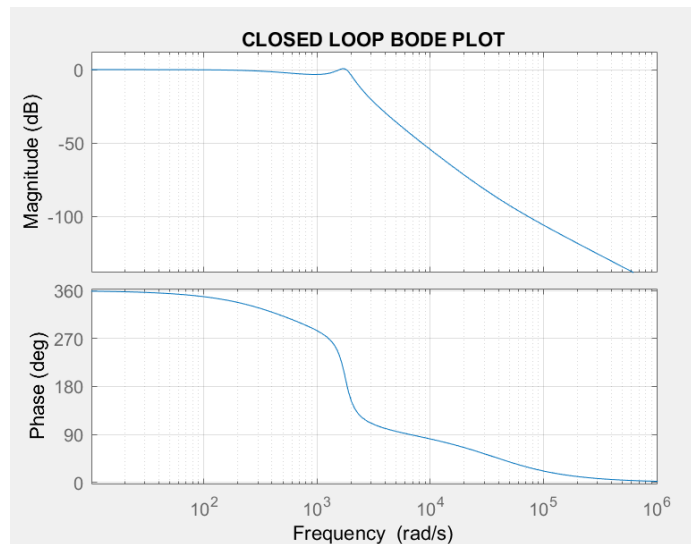


Figure 4.2 Closed-Loop Bode Plot of TPIB

4.3 Average Current Sharing (ACS) Technique

The Average Current Sharing scheme is carried out by using an additional control loop which works together with the outer voltage controller to achieve even current sharing between all three interleaved channels. The basic concept behind the ACS scheme is that the average of the three phase currents acts as the reference current for each channel such that if

the current of any phase exceeds the average current, its duty cycle gets reduced and if it falls below the average current, its duty cycle gets increased until the current of each phase converges to the same average current level.

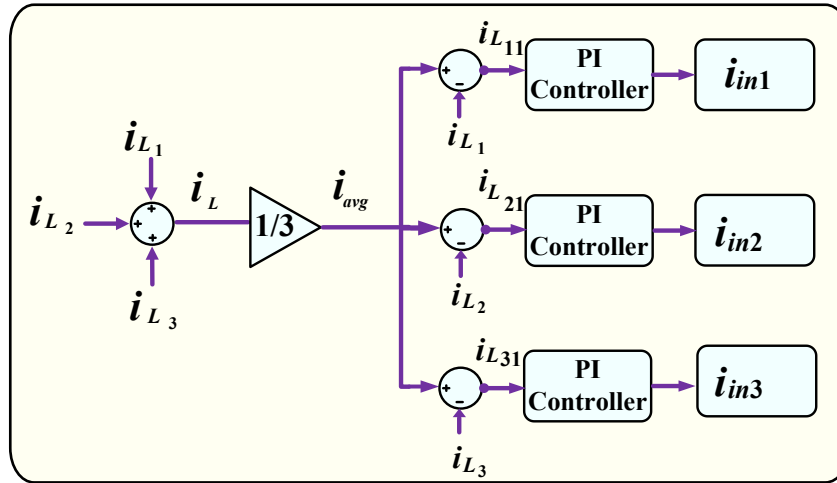


Figure 4.3 Close loop control of ACS for TPIB converter.

The input current of three inductors is i_{L1} , i_{L2} , i_{L3} respectively. They are sensed by current sensors. To compute the average current value

$$i_{avg} = \frac{i_{L1} + i_{L2} + i_{L3}}{3} \quad (4.4)$$

This is the ideal reference for each leg. Computing the current errors for each phase

$$i_{L11} = i_{avg} - i_{L1} \quad (4.5)$$

$$i_{L21} = i_{avg} - i_{L2} \quad (4.6)$$

$$i_{L31} = i_{avg} - i_{L3} \quad (4.7)$$

Each error goes into its own PI controller and each PI fine-tunes the PWM duty cycle of each phase. If a phase has less current, PI increases its duty then current will increase and if a phase has more current, PI decreases its duty then current will decrease. The output of ACS is computed as i_{in1} , i_{in2} , i_{in3} . These signals later modify the PWM duty to enforce current balancing.

The average current is obtained by calculating the summation of the three phase currents and dividing by three at each instant. In order to obtain the average value, each phase is provided with a separate current error compensator that provides the error between the average current and individual phase current to give the output as a duty cycle modification signal. This

modification signal is then added to the common duty cycle signal provided from the outer voltage control loop through PI controller. The current error compensator used is of PI type in order to have zero current sharing error in the steady state.

The entire hierarchical control scheme can be viewed as three levels operating together to accomplish the required converter function. On the first level of the scheme, the PI voltage controller regulates the output voltage by producing a common duty cycle instruction in response to the error of the output voltage. On the second level, the ACS controller produces an individual duty cycle instruction for each leg based on the difference between each leg's current and the average value of the leg currents. Finally, on the third level, the PWM modulator generates pulse width modulation signals for the three MOSFET switch gates with different duty cycles and 120° phase angles.

This method works especially well when trying to overcome the current imbalance due to mismatches in ESRs of inductors. If one phase happens to have a larger ESR compared to the other phases, then in its normal state, without any kind of compensation, such a phase will naturally carry a smaller current due to the higher voltage drop occurring because of the larger resistance. The current imbalance detection part of the ACS algorithm detects such an event, and accordingly, the controller raises the duty cycle of the phase having the problem. By increasing the duty cycle, the ACS controller compensates for the mismatched inductor ESRs, and therefore provides proper current balancing.

4.4 Open-Loop Stability, Controllability and Observability

A complete characterization of the system requires the verification of three basic properties: stability, controllability and observability. The properties are studied by eigenvalue analysis of the A matrix and rank tests of the controllability and observability matrices.

Eigenvalue Analysis

The eigenvalues of the system matrix A are equal to the open-loop poles of the transfer function since they both describe the free response of the system. The eigenvalues calculated are

$$\text{Eigenvalues} = [-5312 + j1.7903, -5312 - j1.7903, -749.0, -1312.4] \text{ rad/s}$$

As all the eigenvalues have strictly negative real parts, the open-loop system is asymptotically stable. There are no pole-zero cancellation problems and the system is well

conditioned for the design of the controller.

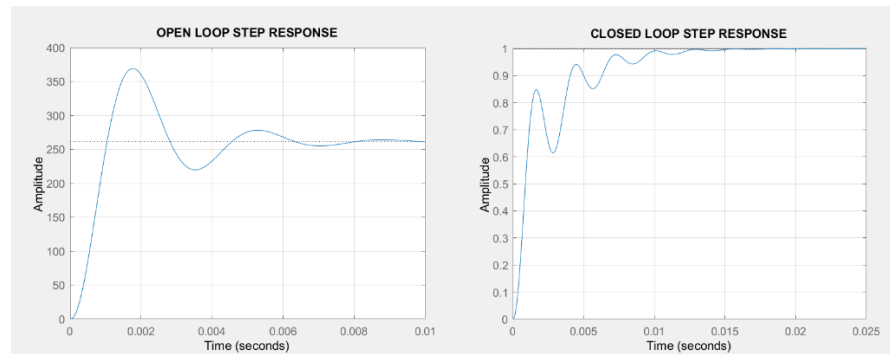


Figure 4.4 Open-Loop and Closed-Loop Step response.

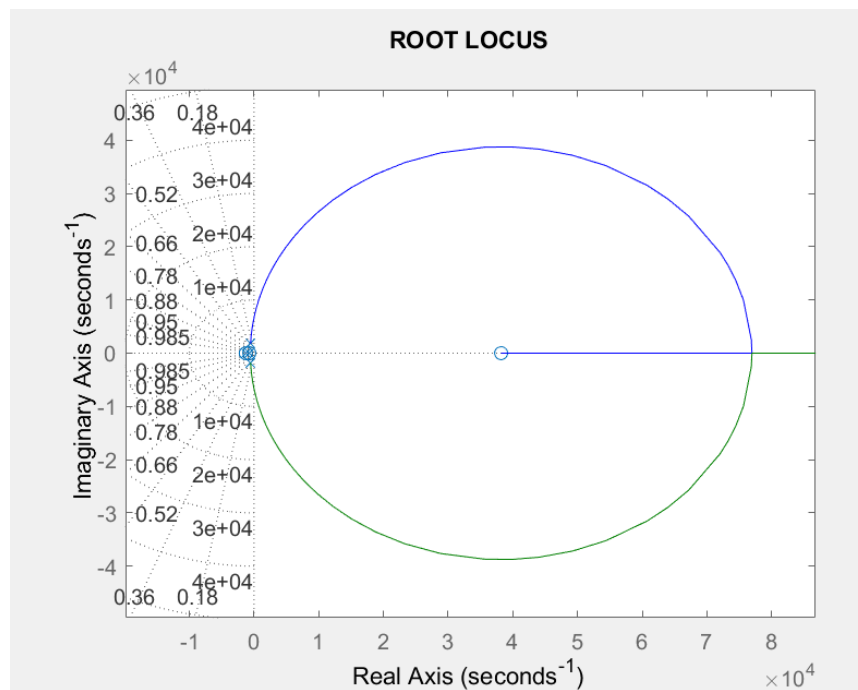


Figure 4.5 Root Locus Plot of TP1B converter

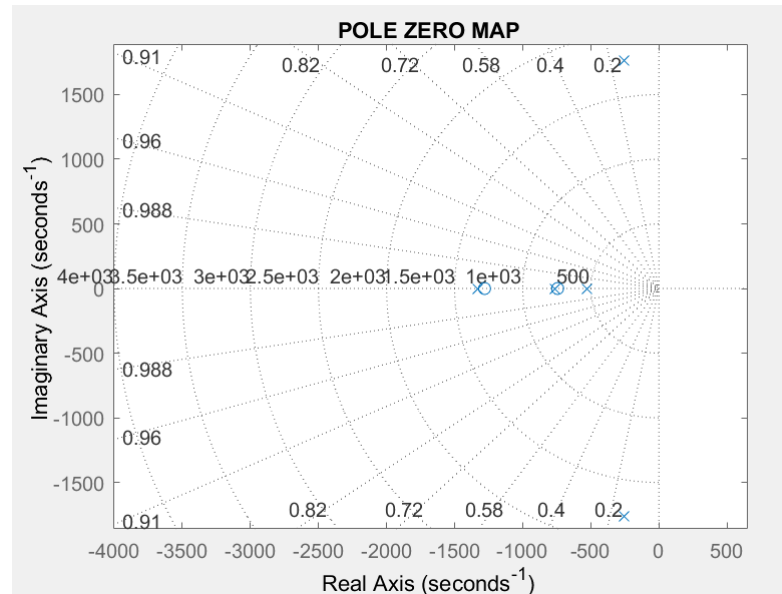


Figure 4.6 Open-Loop and Closed-Loop Step response.

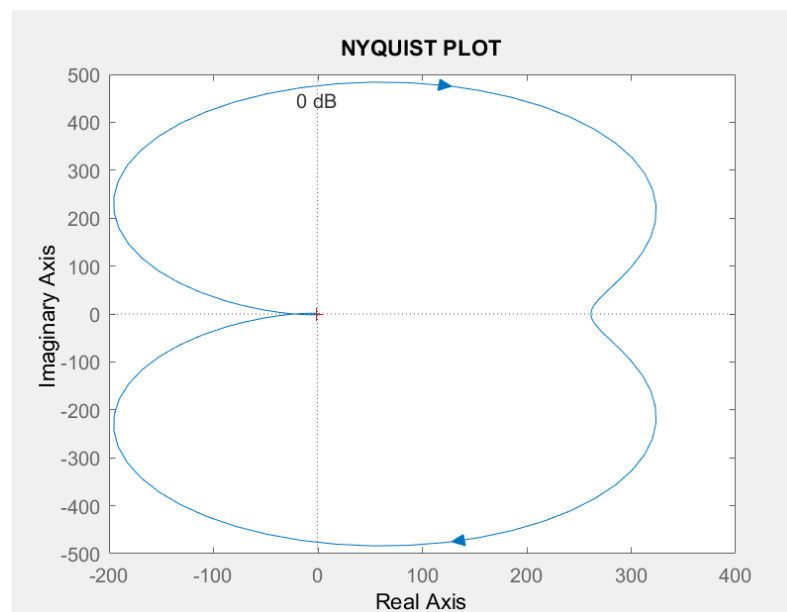


Figure 4.7 Nyquist Stability Plot

Controllability and Observability

For the four state, single input, single output system, the controllability matrix $\sum C$ and the observability matrix $\sum O$ are formed.

Rank $\sum C = 4 = n$, System is Controllable

Rank $\sum O = 4 = n$, System is Observable

Full controllability means the system can be driven from any initial state to any desired final state in a finite time via the duty cycle input. Full observability implies that the entire internal state of the converter can be reconstructed from the output voltage measurement alone. These properties jointly verify the suitability of the state-space model for control design and state estimation.

The system characterizes the oscillatory and decay behaviour of each mode using natural frequencies and damping ratios.

Table 4.3 Natural Frequencies and Damping Ratios of Open-Loop System

Mode	Natural Frequency ω_n (rad/s)	Damping Ratio ξ
Mode 1 (Real pole)	749	1.0000 (critically damped)
Mode 2 (Real pole)	1312.4	1.0000 (critically damped)
Mode 3 (Complex pair)	1867.4	0.2835 (underdamped)
Mode 4 (Complex pair)	1867.4	0.2835 (underdamped)

The two real poles Modes 1 and 2 have damping ratio of 1.0 which means that they are critically damped and decay exponentially without oscillation. The complex conjugate pair Modes 3 and 4 has a natural frequency of 1867.4 rad/sec (roughly 297 Hz) and a damping ratio of 0.2835, which is within the underdamped regime. This complex pole pair is the dominant mode that determines the oscillatory step response of the open-loop converter and gives rise to the characteristic overshoot and ringing in the open-loop step response. The damping ratio is relatively low i.e. 0.2835, which motivates the need of a well-designed feedback controller to improve the closed-loop damping and mitigate oscillatory transients .

4.5 Frequency-Domain Analysis of Closed-Loop System

The closed-loop system is characterized by its frequency-domain stability margins and frequency response. The loop gain transfer function for it is given by,

$$L(s) = C_{PI}(s).G(s)$$

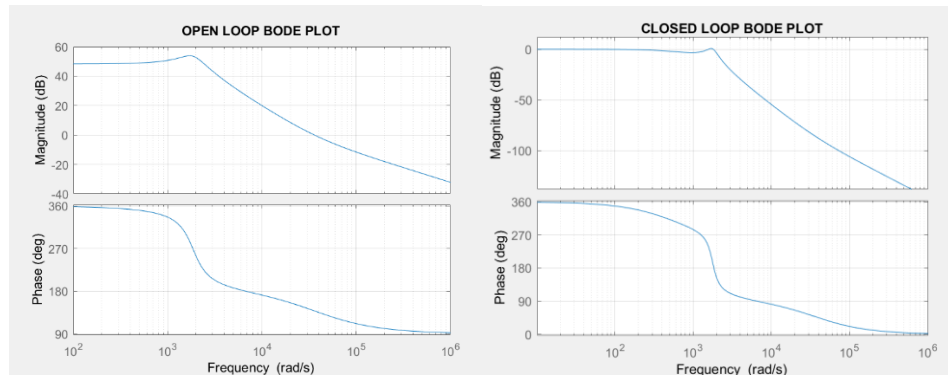


Figure 4.8 Open-loop and Closed-Loop Bode plot of TP1B converter

Gain and Phase Margins

The closed-loop stability robustness can be measured by the gain and phase margin. They tell about the additional gain or phase lag the loop can tolerate before becoming marginally unstable.

Table 4.4 Closed-Loop Frequency Domain Stability Parameters

Stability Parameter	Value
Gain Margin	6.284 dB
Phase Margin	79.89°
Gain Crossover Frequency	1849.1 rad/s
Phase Crossover Frequency	532.24 rad/s
Resonant Peak	0.6354 dB

A gain margin of 6.284 dB means that the loop gain can be increased by a factor of 2.06 before it would become unstable. A phase margin of 79.89° is well within the generally accepted design guideline of 45°–80° for power converter voltage control loops, indicating that the closed-loop system has adequate damping with good robustness against plant parameter variations. These margins give confidence that the controller will be stable for the parasitic mismatches and load variations that occur in practice.

The gain crossover frequency is 1849.1 rad/s. This is the frequency where the magnitude of the loop gain is unity (0 dB). This is about 68 times lower than the switching frequency of 20 kHz which confirms the adequate separation between the control bandwidth and the switching frequency. The phase crossover frequency also lies below the gain

crossover frequency which tells about the conditionally stable system with positive gain margin. Fig 4.9 shows the Gain and Phase Margin plots for Open and Closed loop system and Fig 4.10 shows the Frequency response under different Duty ratios.

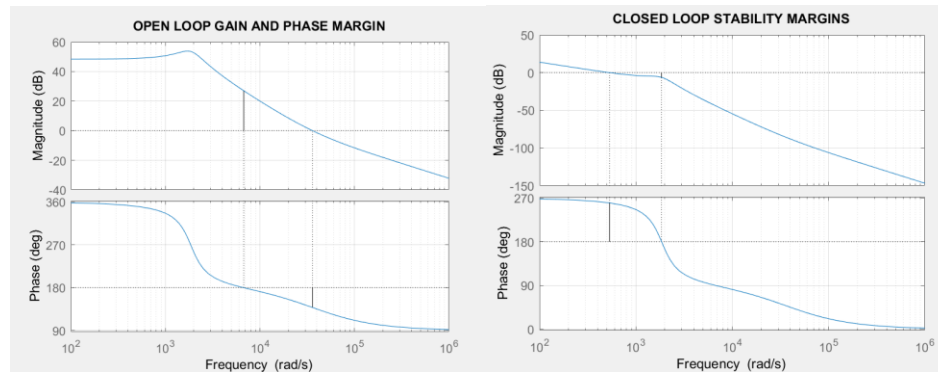


Figure 4.9 Gain and Phase Margin plots for Open and Closed loop system

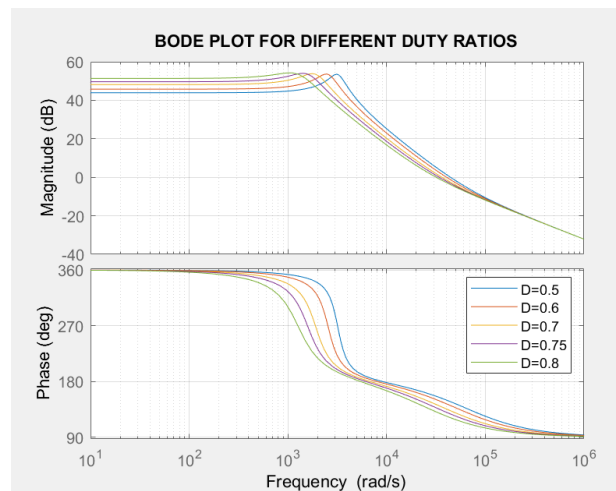


Figure 4.10 Frequency response under different Duty ratios

Closed-Loop Poles and Zeros

The closed-loop poles determine the stability and transient performance of the feedback system. The PI controller add one zero and one pole at origin to make the closed-loop system fifth order.

Table 4.5 Closed-Loop Poles and Zeros

Type	Location (rad/s)	Remarks
Closed-loop pole 1	$-253.0 + j1764.1$	Dominant complex pair
Closed-loop pole 2	$-253.0 + j1764.1$	Dominant complex pair
Closed-loop pole 3	-1330.8	Real pole
Closed-loop pole 4	-526.1	Real pole
Closed-loop pole 5	-760.8	Real pole
Closed-loop zero 1	$+38178$	RHP zero (inherited)
Closed-loop zero 2	-1280	LHP zero
Closed-loop zero 3	-943	LHP zero (PI zero)
Closed-loop zero 4	-744	LHP zero

All five closed loop poles are in the LHP, confirming closed loop stability. The dominant pole pair at $-253.0 + j1764.1$ rad/sec has a natural frequency of about 1782.1 rad/sec and a damping ratio of ζ 0.142. This is underdamped but the oscillatory transient is well suppressed by the integral action. The real poles at -526.1 , -760.8 and -1330.8 rad/s introduce additional but non-dominant decay modes.

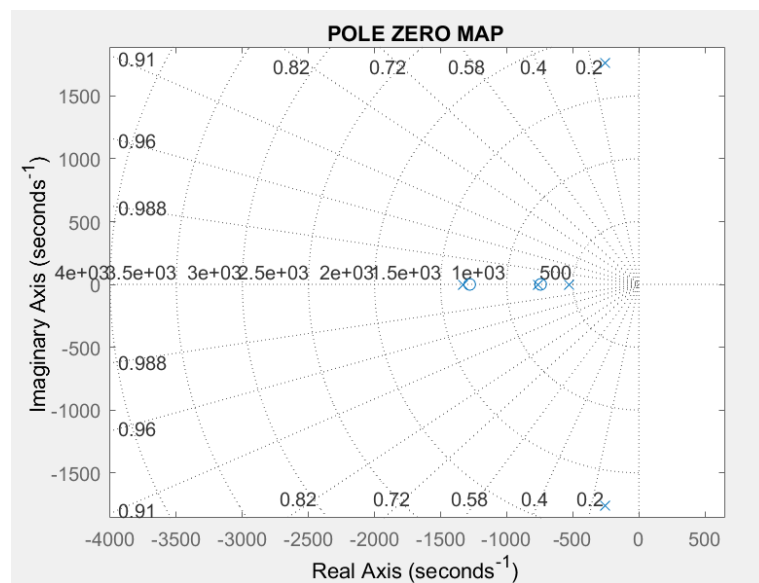


Figure 4.11 Closed-Loop Pole Zero map

4.6 Time-Domain Analysis of Closed-Loop System

The time-domain step response of closed-loop system gives the measurement of controller performance. The response is attained by applying the unit step to the closed-loop TF and measuring the performance metrics.

Closed-Loop Step Response Metrics

Table 4.6 Closed-Loop Step Response Performance

Performance Metric	Symbol	Value
Rise Time (10%-90%)	t_r	1.70 ms
Settling Time (2% criterion)	t_s	9.9 ms
Peak Time	t_p	6.3 ms

The closed loop response is achieved with zero percent overshoot and zero steady state error which are the main design criteria for a regulated power supply. The response is moderately fast with a rise time of 1.70 ms, which is adequate for the 20 kHz switching converter where the control bandwidth is limited to 428 rad/s. The settling time of 9.9 ms is also within the range of application.

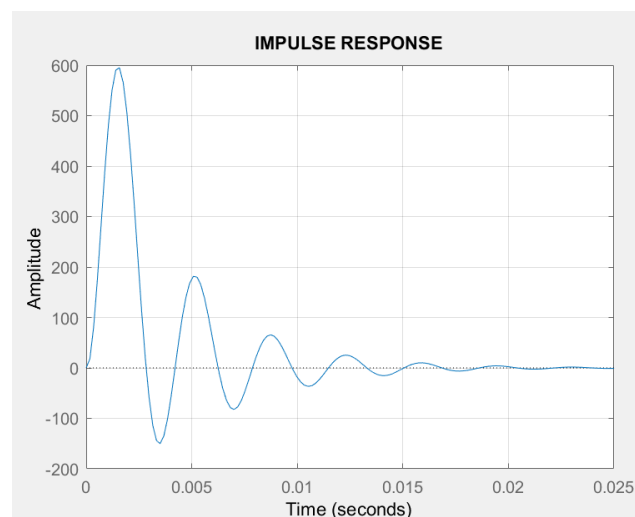


Figure 4.12 Impulse response of Closed-Loop system

Effect of Load Variation on Step Response

The sensitivity of the closed-loop response to changes in the load resistance is a critical test of controller robustness. In practical applications, such as electric vehicle charging systems and photovoltaic interfaces, the output load can vary greatly. The step response of the TPIB converter with five different load resistances ($R = 20, 30, 40, 50, 60 \Omega$) is shown in Fig. 4.13.

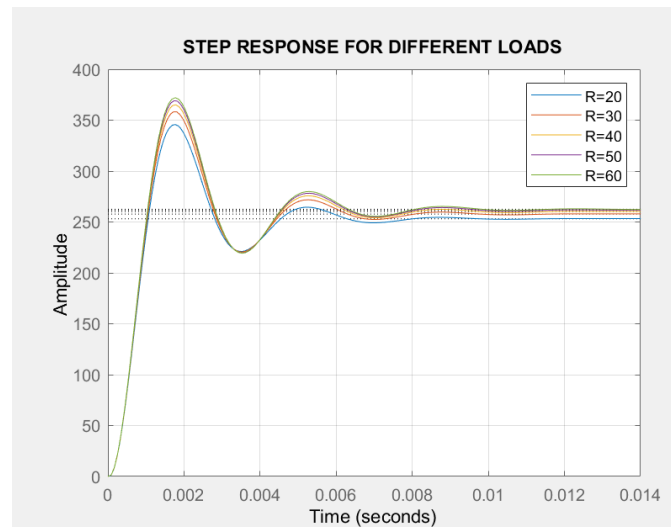


Figure 4.13 Step response for different loads

The step responses for all five load conditions converge to the same steady state value of approximately 260 V (the scaled output), confirming that the integral action successfully rejects DC load disturbances. The transient responses exhibit a common peak overshoot of about 35-40% at 2 ms, followed by a damped oscillation settling within about 10-14 ms. The variation in peak amplitude over different load values is small indicating that the PI controller provides good robustness over the tested load range.

The small increase of the peak overshoot for lighter loads (larger R) is expected, as the open-loop converter gain increases with the load resistance, effectively increasing the loop gain and decreasing the phase margin a bit. However, all the five responses are stable and converge to the regulated reference, which confirms the robustness of the designed PI controller.

4.7 Conclusion

This chapter concludes about the control technique of TPIB converter. It elaborates about the PI characteristics, ACS, frequency and time domain of the TPIB converter.

CHAPTER 5

FAULT TOLERANT OPERATION

5.1 Introduction

Reliable, continuous operation of power electronic converters is an important requirement for applications such as electric vehicle drivetrains, renewable energy systems and aerospace power supplies. Converter failure can have serious consequences, ranging from loss of system functionality to safety hazards. There are different failure modes in the Three-Phase Interleaved Boost Converter, and the open-switch faults of the MOSFET switching devices are very common and require a suitable fault-tolerant control strategy. This chapter introduces the fault detection algorithm, the converter reconfiguration strategy for continued operation after an open switch fault, and a detailed analysis of power losses and efficiency in the healthy and fault-tolerant states.

5.2 Fault Tolerant Strategy

The fault tolerant strategy developed in this work aims at assessing the capabilities of the TPIB converter to maintain the output voltage stable and the inductor currents balanced in the event of an open-circuit switch fault in one of the phases of the converter. The strategy is deliberately practical and simulation-based. The fault is manually introduced by turning off the gate signal of the affected switch and the converter response is observed to verify the success of the ACS controller, as well as, the PWM interleaving logic to adapt to the reduced-phase operation.

The fault considered in this study is an OCF in the MOSFET switch. An open-circuit fault occurs when a switching device permanently fails to conduct during its intended-ON state, effectively removing that phase from active power processing. This is the most common fault type in boost converter topologies and results in the loss of one interleaved phase. Under healthy three-phase operation, the three gate signals (G1, G2, G3) are created by comparing distinct PI controller outputs against three carrier waveforms that are phase-shifted by 120° with respect to each other. This standard interleaving confirms that the switching events of the three phases are uniformly distributed across the switching period which minimise the

input current ripple and distributing the thermal stress equally among the switches.

The adjacent phases of interleaving angle in healthy operation are:

$$\theta_{healthy} = \frac{360^\circ}{N} = \frac{360^\circ}{3} = 120^\circ \quad (5.1)$$

Switch 1, 2 and 3 each fire in consecutively with a uniform 120° phase offset within every switching cycle. All three inductor currents (I_{L1} , I_{L2} , I_{L3}) are active and display the characteristic triangular ripple waveform, oscillating between approximately 1 A and 3.5 A in steady state.

After the fault, only Switch 2 and 3 remain active.

$$\theta_{fault} = \frac{360^\circ}{N-1} = \frac{360^\circ}{2} = 180^\circ \quad (5.2)$$

This 180° interleave is the best arrangement for two-phase operation, as it maximizes the cancellation of input ripple between the remaining phases.

The ACS controller updates the current reference of each remaining active phase in order to share the total load current equally:

$$I.L_{active} = I_{out} \frac{(V_{out} / V_{pv})}{(N-1)} \quad (5.3)$$

The individual PI controllers of Phase 2 and Phase 3 set the inductor currents to this updated reference, thus enforcing current balance under the two-phase post-fault condition.

5.3 Operation of TPIB Converter

The TPIB converter works by combining three identical boost converter phases. These phases are connected in parallel at both the input and output terminals. Each one has its own inductor, a power switch, and a diode. The switches get PWM gating signals that are shifted by 120° from each other. This interleaved switching spreads the input current across all three phases, which cuts down on ripple, boosts efficiency, and helps the components stay cooler.

Healthy operating condition

By looking at the healthy operating condition, we conclude that all three legs carry their share of the power. The gating signals are spaced 120° apart so the switches don't turn on at the same time and take turns. This phase shift increases the ripple frequency on both

the input and output sides, which keeps the actual ripple much lower.

When a switch is ON, its inductor grabs energy from the input and builds current, following the basic boost converter principle. When the switch flips OFF, the inductor's energy goes to the output capacitor and load through the diode. Since the three phases take turns delivering power, there is always at least one feeding the load. That leads to a smoother output current and less voltage ripple. The interleaving also makes sure the input current gets split between the inductors ideally, each phase takes a third of the total input current.

In real-world components are not ideal. Inductor losses and capacitor ESR lead to small mismatches and some extra heating. A PI-based current balancing controller steps in here. It keeps an eye on the phase currents and tweaks the duty cycles so that all phases pull their weight. The controller keeps each current close to the average, smoothing things out. Because the phases interleave, ripple currents partially cancel each other out it have many advantages such as much lower input current ripple, minimized output voltage ripple, less electromagnetic interference (EMI), shared thermal stress and better converter efficiency.

Open Switch Fault Condition

For fault-tolerant operation the TPIB converter has built-in control strategies so it keeps running even if one Phase suffers an open-circuit fault, this kind of thing is common in power electronics, because of thermal stress, over current, or gate driver issues. Open-circuit faults aren't usually destructive, but if ignored, it can destruct the current balance.

If a leg fails and its current drops to zero, the controller spots this immediately with real-time monitoring. It isolates the faulty phase and shifts the load to the remaining healthy phases. If the phase 1 goes has fault, the controller cuts it out, and phases 2 and 3 pick up the slack. The system keeps powering the load and keeps the voltage steady.

When this happens, the phase shift between the two working legs changes to 180° . It still cancel-out ripple, so the output stays smooth. The converter doesn't shut down and keeps going. After the fault introduction in circuit the faulty phase gets isolated, the healthy phases carry extra current, output voltage regulation stays intact, converter doesn't stop operating and system reliability improves.

This fault-tolerant feature really matters in places like renewable energy setups, electric vehicles, aerospace, and DC microgrids, where power just cannot be removed. Keeping the converter running during faults boosts reliability and avoids total system failure.

5.4 Conclusion

This chapter concludes about the fault tolerant capability of the TPIB converter. It explains about the open fault occurrence in the system and gives idea about healthy and faulty condition in the circuit. It also explains about the changes of duty cycle when in natural and faulty state.

CHAPTER- 6

RESULTS AND DISCUSSION

6.1 Introduction

This chapter exhibits the simulation results from the MATLAB/Simulink model of the Three-Phase Interleaved Boost (TPIB) Converter under non-ideal circuit conditions with parasitic elements, PI voltage controller, Average Current Sharing (ACS) controller, and fault-tolerant operation strategy. The parameters of the converter are listed in Table 6.1. The parasitic resistances of the inductors are deliberately mismatched among the three phases to emulate realistic non-ideal conditions and to verify the effectiveness of the proposed current balancing method.

The simulation results are presented in a structured way including healthy condition analysis, current balancing performance under parasitic mismatch, effect of the ACS controller, open-switch fault analysis, current redistribution after fault occurrence, efficiency analysis and a comprehensive discussion summarizing all findings. The waveforms are obtained from MATLAB/Simulink simulations to guarantee precise representation of high-frequency switching transients.

Table 6.1 System Parameters

Parameter name	Values
Per phase Inductance (L)	330 μ H
Switching Frequency (f_s)	20 kHz
Output Capacitance (C_{out})	220 μ F
Input Voltage (V_{pv})	24 V
Output Load Voltage (V_{out})	80 V
Proportional Gain of Controller (K_p)	0.1
Integral Gain of Controller (K_i)	150

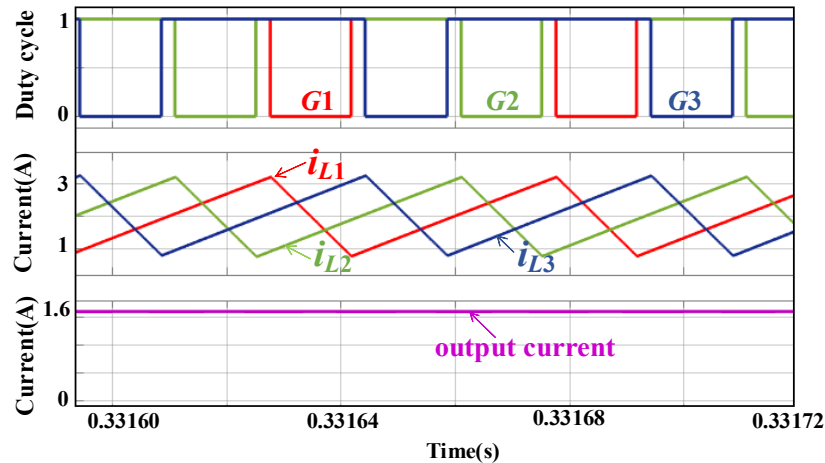


Figure 6.1 TPIB converter with phase gating pulse, inductor currents and output current.

6.2 Healthy Condition Analysis

Under normal working conditions, an interleaved boost converter works by maintaining three identical phases of a boost converter, each phase has its inductor and switch, which work in parallel with each other in even-spaced switching cycles. This technique introduced that each phase switches turned on and off at the same frequency, at the fixed time, it ensures that the current pulses are distributed evenly in each phase throughout the switching period. As a result, smoother and reduced ripples can be seen in the input current drawn from the source from compared to a single-phase boost converter. It also helps to minimize electromagnetic interference and stress on input components. The output voltage is managed through a control circuit, typically using pulse-width modulation (PWM), which adjusts the duty cycle of each phase's switch to maintain a stable output voltage in any case of changes in input voltage or load state. By dividing the load current across three phases, the converter minimizes conduction losses in each inductor and switch, which improves overall efficiency and disperse heat more evenly in the circuit. It improves reliability and thermal management in the system. This synchronized and balanced operation assures that the interleaved boost converter gives high performance, lower noise, and greater durability, which in turn makes it suitable for applications essential for high power and efficiency. Fig. 6.2. represents the TPIB converter with balance current under normal condition.

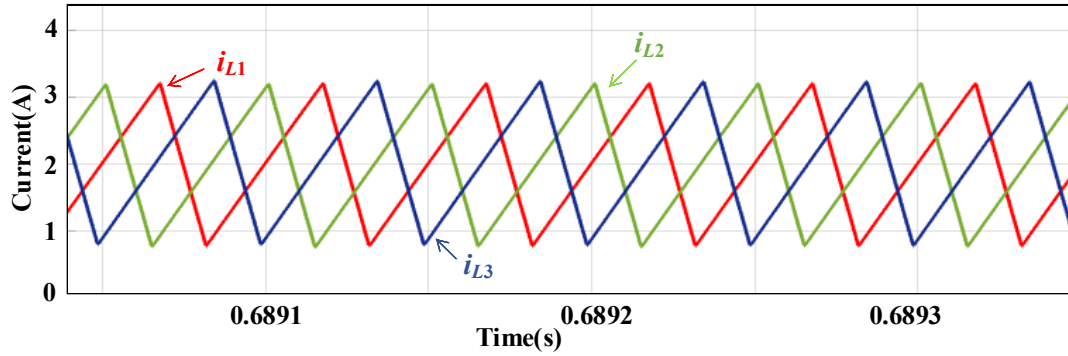


Figure 6.2 TPIB converter with balance current under normal (healthy) condition.

6.3 Current Balancing Performance

The current balancing performance of the TPIB converter is estimated under intentionally introduced parasitic resistance mismatches among the three phases. The three inductor parasitic resistances are set to $r_{L1} = 0.3 \, \Omega$, $r_{L2} = 0.5 \, \Omega$, and $r_{L3} = 0.2 \, \Omega$, representing a realistic non-ideal condition where manufacturing tolerances result in different winding resistances among the three inductors. Without active current balancing control, the phase with the lowest parasitic resistance, i.e. r_{L3} carries the highest current, while the phase with the highest resistance i.e. r_{L2} carries the lowest current.

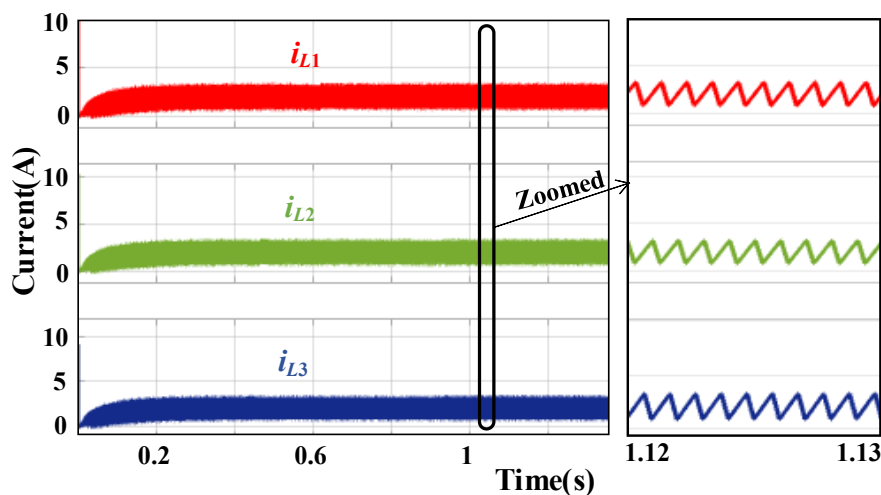


Figure 6.3 TPIB converter with balance current in each leg under healthy condition.

The zoomed result of balanced current in each leg is represented in Fig 6.3. It shows the individual phase currents over a longer time window, confirming that under the proposed ACS control scheme all three phases maintain equal average currents despite the intentional parasitic mismatch. The ACS controller continuously monitors I_{L1} , I_{L2} , and I_{L3} , computes their average, and adjusts the individual duty cycle corrections to drive each phase current toward the common average, restoring balanced current distribution and maintaining the ripple cancellation advantage of the interleaved topology.

6.4 Effect of ACS Controller

Balancing the phase currents under non-ideal circuit conditions requires the Average Current Sharing (ACS) controller. This controller is a secondary control loop that produces separate duty cycle correction signals for each phase. The control action depends on the difference between the phase current and the computed average of the three phase currents. The outer PI voltage controller provides a common duty cycle command which is added to these correction signals to obtain the final duty cycle of each phase. In phase 2, the phase with the maximum parasitic resistance i.e. r_{L2} a positive duty cycle correction is performed to compensate the lower current inherently present and increase the energization time such that the current can be restored to the average value. Phase 3 has the lowest parasitic resistance i.e. r_{L3} so a negative correction is applied to slightly reduce its duty cycle, so that it doesn't carry too much current. The simulation results indicate that the ACS controller can achieve balanced current distribution under non-ideal parasitic mismatch conditions. In the steady state, the three phase currents settle at approximately equal average values. The ACS controller bandwidth is chosen to be about one decade lower than the voltage control loop bandwidth, thus avoiding interference of the current sharing corrections with the faster voltage regulation dynamics.

6.5 Open Switch Fault Analysis

Under fault conditions, such as switch failures or phase malfunctions, an TPIB converter employs fault-tolerant strategies to support operation with minimum performance deterioration. The aim is to achieve constant current when fault is introduced in the converter.

Fault can be detected by using real-time monitoring of inductor current and current imbalances, which helps to identify the fault. Once a fault is detected, the system reconfigures by disconnecting the faulty phase and distributing the load to healthy phases. In three-phase converter, if one phase fails, the other two phase's duty cycle is dynamically increased to maintain the output voltage. The phases are phase shifted by 180° which helps to get minimum ripple in the output current. The pre-fault and post-fault inductor current waveform in TPIB converter are represented at fig. 5.4. Before fault all three inductors share load evenly. After fault occurrence in leg 1, the current i_{L1} drops to zero, while other two legs increase their current i_{L2} and i_{L3} to balance the current sharing.

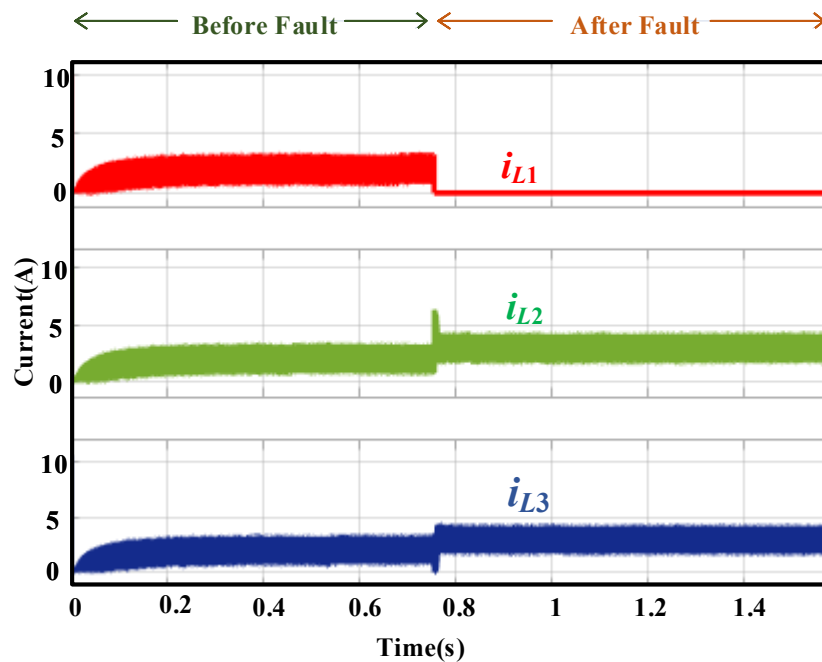


Figure 6.4 . TPIB converter with balance converter with open circuit switch fault.

6.6 Current Redistribution after Fault

The fault-tolerant reconfiguration is carried out by turning off gate signal G_1 , changing the current sharing reference from one third to one half of the total current, and modifying the phase displacement between G_2 and G_3 from 120° to 180° for optimal ripple cancellation with two active phases.

The occurrence of fault and steady state of inductor current after the fault is

represented in fig. 6.5. (a). When the fault appears, the current i_{L1} instantly drops to zero, confirming OCF. Consequently, currents i_{L2} and i_{L3} increases and dynamically adjust to share the load to maintain stable operation. In pre-fault, the average inductor current is about 1.78 A. Whereas in post-fault only two legs are conducting, so average current increases to 2.67 A per leg. This represents nearly 50% increment in average current.

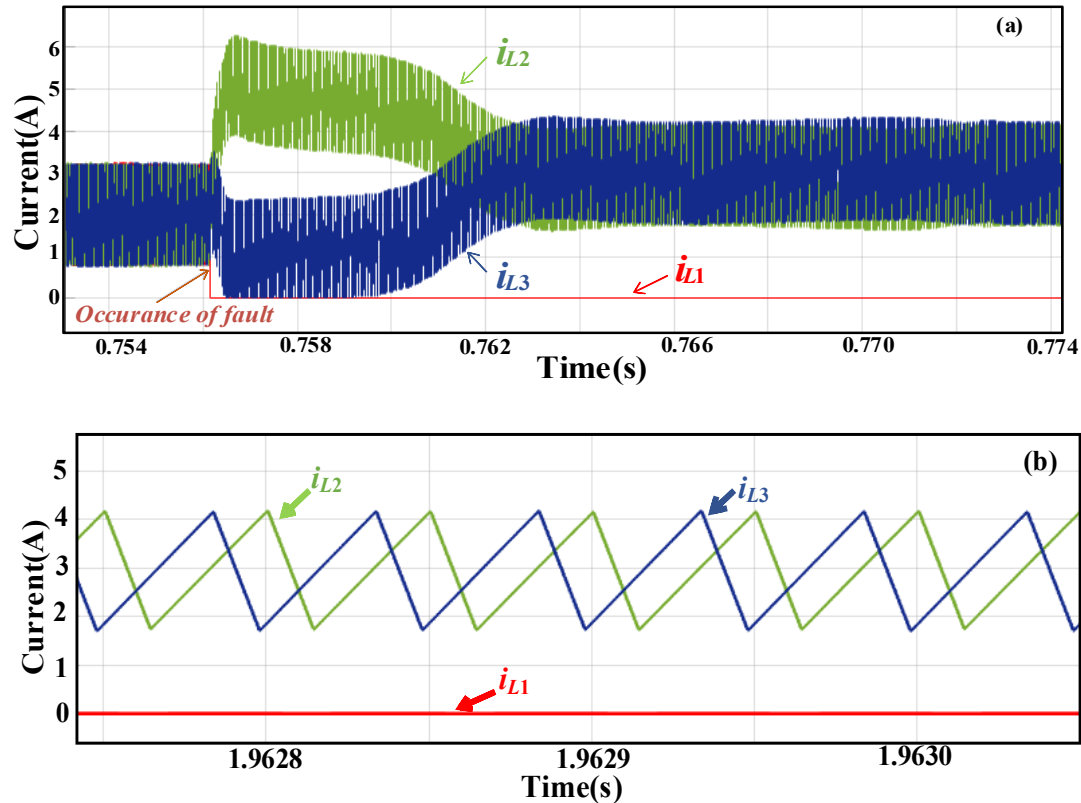


Figure 6.5 TPFB converter (a) occurrence of fault (b) After fault steady state condition.

Fig. 6.5 (b) shows post-fault steady-state waveforms when the converter is fully switched to two-phase fault tolerant operation. The i_{L1} still remains 0 verifying the permanent disconnection of the faulty phase. The i_{L2} and i_{L3} are balanced triangular waveforms with 180° phase displacement and with an average value of about 2.67 A each. The output voltage and current are maintained at their regulated values, showing a successful continuous fault tolerant operation.

Table 6.2 pre-fault and post-fault comparison of Operating Conditions

Parameter	Pre-Fault (3-Phase)	Post-Fault (2-Phase)
Active Phases	3	2
Average Current per Phase	1.78 A	2.67 A
Phase Displacement	120°	180°
Output Voltage	80 V	80 V (regulated)
Output Current	1.6 A	1.6 A (maintained)
Ripple Frequency	$3 \times f_{sw} = 60 \text{ kHz}$	$2 \times f_{sw} = 40 \text{ kHz}$

6.7 Efficiency Analysis

The efficiency of the TPIB converter is calculated for the healthy three-phase operation and the fault-tolerant two-phase operation. The efficiency is defined as the ratio of the output to the input power and is obtained by averaging the instantaneous power waveforms over a number of switching cycles in MATLAB/Simulink in order to eliminate the effect of the switching ripple from the power measurements. In the case of healthy three-phase operation for the given parasitic resistances, the converter shows good efficiency at the nominal operating point. Output voltage is 80 V Load resistance is 50 Ω Output power is 128 W. The total power loss is calculated from the inductor copper losses of the parasitic winding resistances r_{L1} , r_{L2} and r_{L3} , capacitor ESR losses and switching losses of MOSFET devices and freewheeling diodes. Phase 2 has higher losses of copper in comparison with other two phases because of its higher parasitic resistance. Thus, parasitic resistance matching needs to be considered in order to improve design in practice.

The per-phase current for fault-tolerant operation with two phases increases by about 50% from 1.78 A to 2.67 A. As inductor copper losses are directly proportional to the square of the current, copper losses in two healthy phases will become much higher. Therefore, the efficiency of the converter in terms of power losses will be reduced in comparison with a normal three-phase system delivering the same amount of power. Nevertheless, a fault-tolerant system operates efficiently and delivers a regulated output power during fault-tolerant

mode.

6.8 Conclusion

The simulation outcomes shown in this chapter provide comprehensive validation of the control approach proposed in this research work for the TPIB DC-DC converter in non-ideal operating environments. The study of healthy operation proves successful implementation of the three-phase interleaving approach with all required parasitic effects, which can be seen from the output voltages, phase currents, and duty cycles obtained in simulations and compared to their theoretical expectations.

The current balancing study showed that without an active current-sharing technique, parasitic resistance imbalances in $L_1 = 0.3 \Omega$, $L_2 = 0.5 \Omega$, and $L_3 = 0.2 \Omega$ would lead to substantial imbalance between currents flowing through the phases. The active current sharing approach proved successful at correcting these imbalance issues by providing adequate correction in individual phase duty cycles and therefore bringing back the advantages of the interleaved structure, namely the ripple cancellation effect. Thus, the initial hypothesis was proven valid for practical applications of TPIB converters.

Based on the above discussion on the fault analysis and fault tolerant reconfiguration results, it is concluded that the proposed current monitoring method together with the fault tolerant switching technique can effectively monitor any open switch condition and subsequently enable fault tolerant operation of the two-phase TPIB with only a minor perturbation of the output voltage. The increase in the average per phase current value from 1.78A to 2.67A after the fault occurrence supports the expected theoretical prediction.

From the above results, it is clear that the proposed hierarchical controller structure using PI voltage controller along with ACS controllers for current sharing and fault tolerant reconfiguration is capable of handling the non-ideal situation and hence a viable approach for realizing a highly reliable two phase TPIB converter suitable for applications such as electric vehicle charging system and photovoltaic energy converter.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion

This article examines a three-phase interleaved boost (TPIB) converter that effectively maintains balanced inductor currents across all three legs, in the presence of parasitic elements and open-circuit faults. The system uses PI controllers in both the voltage and current control loops, permitting stable output voltage regulation while capably minimizing dynamic disturbances such as overshoots, undershoots, and transient ripple. The synchronized control strategy makes sure the uniform current distribution among the three inductors, which reduces input current ripple, improves converter efficiency and lifespan of the system.

Furthermore, the addition of a fault-tolerant mechanism allows the converter to logically redistribute current through the remaining healthy phases during an open-circuit fault. This capability ensures continuous operation, prevents overloading of components, and maintains constant output current without requiring full system shutdown. By putting non-idealises such as parasitic resistances in inductors and capacitors, the proposed method mirrors realistic operating conditions and improves the robustness of the overall design.

The presentation of the anticipated control and fault-tolerant strategy has been carefully analysed and validated through MATLAB/Simulink simulations. The results confirm that the converter attains stable voltage regulation, balanced phase currents, and smooth fault handling under both ideal and faulty operating circumstances. These outcomes validate that the presented TPIB converter is highly suitable for practical applications where high efficiency, reliability, and resilience to faults are essential.

7.2 Future Scope

The presentation of the current balancing method in the three-phase interleaved boost converter can be further enhanced in several ways. Although the current design effectively maintains equal current in all three legs and achieves open-circuit faults, future work can emphasis on constructing the system even more stable under different operating conditions.

Improved Current Control: The PI-based current controller works fine, but future systems

can consist of adaptive or auto-tuning PI controllers that adjust their gains automatically based on load changes or variations in parasitic resistances. This will help sustain better current balance under all operating conditions.

Parasitic Tracking: Since inductor parasitic resistances change with temperature and ageing, future designs can evaluate these changes in real time. Updating the controller with these values will improve accuracy in current sharing.

Handling Multiple Faults: The present model mainly focuses on single open-circuit faults. In future work, the system can be extended to manage multiple faults or partial faults such as increased ESR or inductor deprivation. This will make the converter more robust in real-life applications.

Sensor Optimization: The balancing of current works on accurate current sensing. In future work we can sightsee methods to minimize the number of sensors to make the system more cost-effective.

Hardware Implementation: The planned controller has been verified in MATLAB SIMULINK. A future step is to make the design on hardware to verify the controller's performance under practical switching losses, and parasitic effect.

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