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M.TECH (Control & Instrumentation)

Sushant Gupta

2026

Transistor-Level Reproduction and Bias Analysis of a Single-OTRA Multifunctional Biquad Filter

A Project Report submitted in partial fulfilment of the requirements for the degree of

Master of Technology in Control and Instrumentation

by

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Under the supervision of

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I, **SUSHANT GUPTA**, Roll No. 2K24/C&I/03, student of M.Tech (Control & Instrumentation), hereby declare that the project Dissertation titled "Transistor-Level Reproduction and Bias Analysis of a Single-OTRA Multifunctional Biquad Filter" which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma, Associateship, Fellowship or other similar title or recognition.

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Acknowledgement

I am grateful to my supervisor, **Dr. Garima**, Associate Professor, Department of Electrical Engineering, for her guidance and patience through every stage of this dissertation report. Her feedback on the analog circuit design and the current-mode signal path shaped much of the work that follows.

I also thank the **Head of the Department of Electrical Engineering**, for the facilities and the working environment that made this dissertation report possible.

My thanks to the faculty of the Department of Electrical Engineering, Delhi Technological University, for their help over the course of the M.Tech programme, and to the department for the lab and compute resources used in the SPICE simulation work on the transistor-level OTRA realisation.

Sushant Gupta
M.Tech (Control & Instrumentation)
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Abstract

The Operational Transresistance Amplifier (OTRA) is a current-mode active building block whose differential current inputs present a virtual ground and whose output voltage is the difference of the input currents scaled by a transresistance gain. Because the external resistors and capacitors connect directly to low-impedance virtual-ground nodes, OTRA-based filters are free of the parasitic-input-capacitance limitations that constrain voltage-mode op-amp realisations. Mann, Kumar, and Bhaskar (ICSC 2021) proposed a single-OTRA multifunctional biquad that realises low-pass, band-pass, and high-pass responses from one active element and a canonic set of passive components.

This dissertation reports a full reproduction of that biquad in three tiers: an ideal symbolic (MATLAB) model, a behavioural single-pole OTRA macromodel, and a transistor-level CMOS realisation of the Mostafa–Soliman fourteen-MOSFET OTRA in a 0.18 µm process simulated in ngspice. The symbolic and behavioural tiers reproduce the published responses to within a fraction of a decibel. The transistor-level low-pass and band-pass responses also match, but the high-pass response was initially observed to droop, with a passband plateau of -3.56 dB against the target 0 dB and a -3 dB frequency of 1.76 MHz against the target 4.25 MHz.

A systematic investigation traced this droop to the bias voltage V_{B1}, which sets the tail currents of the voltage-biased transistors and therefore the signal-path transconductance and the transresistance gain-bandwidth. A focused V_{B1} sweep showed a narrow functional window: at $V_{B1} = -1.31$ volt the high-pass passband recovers to approximately 0 dB with a -3 dB frequency of 4.17 MHz, matching the published design, while the low-pass and band-pass responses remain matched at the same global bias. An attempted regulated-cascode fix at the high-impedance internal node is shown to be both unbiasable on a signal-referenced node and unnecessary, since output-resistance boosting does not change the controlling gain-bandwidth product. The principal contribution is the identification of V_{B1}, rather than device sizing, output resistance, or the model card, as the operative lever that recovers the high-pass response.

Keywords: Operational transresistance amplifier, OTRA, multifunctional biquad, current-mode filter, transresistance gain-bandwidth, CMOS analog design, SPICE simulation, bias optimisation.

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List of Abbreviations and Symbols

Abbreviations

OTRA	Operational Transresistance Amplifier
OTA	Operational Transconductance Amplifier
CFOA	Current Feedback Operational Amplifier
CCII	Second-Generation Current Conveyor
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Transconductance Amplifier
CMOS	Complementary Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
CMFB	Common-Mode Feedback
RGC	Regulated Cascode
GBW	Gain-Bandwidth Product
LPF	Low-Pass Filter
BPF	Band-Pass Filter
HPF	High-Pass Filter
AC	Alternating Current
DC	Direct Current
KCL	Kirchhoff's Current Law
SPICE	Simulation Program with Integrated Circuit Emphasis
PVT	Process, Voltage, Temperature
TSMC	Taiwan Semiconductor Manufacturing Company
TIA	Transimpedance Amplifier
DTU	Delhi Technological University

Symbols

R_m	Transresistance gain of the OTRA
$R_m(s)$	Frequency-dependent transresistance
R_0	DC value of the transresistance
ω_{p1}	Dominant pole of the OTRA transresistance
ω_{p2}	Second (parasitic) pole of the OTRA transresistance
I_p, I_n	Non-inverting (+) and inverting (−) input currents
V_o	OTRA output voltage
V_{B1}	External gate-bias voltage of the OTRA tail transistors
I_B	External bias current of the OTRA
g_m	Small-signal transconductance
C_{node}	Lumped capacitance at the high-impedance internal node
ω_0	Pole/centre frequency of the biquad
Q	Pole quality factor
$f_{-3\text{dB}}$	Half-power (cut-off) frequency
s	Complex frequency variable ($s = j\omega$)
V_{DD}, V_{SS}	Positive and negative supply rails ($\pm 1.85\,\text{volt}$)

Chapter 1

Introduction

1.1 Current-Mode Analog Signal Processing

Analog signal processing manipulates continuous-time signals using active and passive networks. For several decades the operational amplifier, a voltage-mode device with high-impedance voltage inputs and a low-impedance voltage output, was the dominant active building block. Voltage-mode realisations are limited by a constant gain-bandwidth product, by slew-rate ceilings, and by the parasitic capacitance that appears at their high-impedance input nodes.

Current-mode signal processing addresses these limitations by treating current, rather than voltage, as the signal variable. Current-mode active elements such as the second-generation current conveyor (CCII), the current feedback operational amplifier (CFOA), the operational transconductance amplifier (OTA), and the operational transresistance amplifier (OTRA) operate with low-impedance internal nodes that decouple bandwidth from gain and reduce sensitivity to node capacitance. These properties make current-mode blocks attractive for high-frequency filters, oscillators, and immittance simulators.

1.2 The Operational Transresistance Amplifier

The Operational Transresistance Amplifier (OTRA) is a three-terminal current-mode active element with two current inputs and one voltage output. Its defining relationship is

10

$$V_o = R_m\,(I_p - I_n), \tag{1.1}$$

where I_p and I_n are the currents drawn into the non-inverting and inverting input terminals, V_o is the output voltage, and R_m is the transresistance gain, with units of ohms and a typical magnitude in the range $10^6\,\Omega$ to $10^9\,\Omega$. Both inputs are held at a virtual ground by internal feedback, so the input terminals present a low impedance. This is the central practical advantage of the OTRA: external resistors and capacitors connect to virtual-ground nodes, so the parasitic input capacitance

that limits voltage-mode op-amp filters is absorbed at a low-impedance node and does not set a pole in the signal path.

In an ideal OTRA the transresistance is infinite, so the two input currents are forced to be equal and the input terminals are held at exactly zero potential. In a real OTRA the transresistance is finite and frequency dependent, which is modelled to first order by a single-pole response

$$R_m(s) = \frac{R_0}{1 + s/\omega_{p1}}, \tag{1.2}$$

where R_0 is the DC transresistance and ω_{p1} is the dominant pole. As shown later in this work, an accurate description of the high-pass response requires a second pole ω_{p2}, and the relevant figure of merit becomes the transresistance gain-bandwidth product rather than R_0 alone.

1.3 Motivation

Mann, Kumar, and Bhaskar [1] proposed a single-OTRA multifunctional biquad that realises low-pass, band-pass, and high-pass responses from one active element together with a canonic number of resistors and capacitors. The configuration is attractive because it minimises active-element count while retaining the virtual-ground advantage of the OTRA. The published work reports PSpice simulation in a 0.18 µm TSMC process together with MATLAB evaluations.

Reproducing such a result at transistor level is valuable for two reasons. First, it confirms that the published filter algebra is realisable with a concrete CMOS OTRA rather than only with an ideal macromodel. Second, the discrepancies that arise during reproduction expose the practical limits of the active element, which are precisely the limits that a designer must understand before reusing the block. In this work the low-pass and band-pass responses reproduce readily, whereas the high-pass response initially droops. The The investigation of that droop, and its resolution, forms the core contribution.

1.4 Objectives

The specific objectives of this dissertation are:

1. Reproduce the single-OTRA multifunctional biquad of [1] in three tiers: an ideal symbolic model, a behavioural single-pole OTRA macromodel, and a transistor-level CMOS realisation in a 0.18 µm process.
2. Quantify the high-pass passband droop in the transistor-level realisation and identify its physical origin.
3. Determine the operative design lever that recovers the high-pass response while preserving the low-pass and band-pass responses at a single global bias.
4. Evaluate, and where appropriate rule out, alternative explanations and fixes including device sizing, the model card, output-resistance boosting by a regulated cascode, and the bias current.

1.5 Organisation of the Dissertation

The remainder of this dissertation is organised as follows.

Chapter 2 — Literature Review surveys OTRA realisations, OTRA-based filters, and other active elements, and identifies the transresistance bandwidth as the recurring practical limitation.

Chapter 3 — The OTRA Active Element defines the port relationships, presents the CMOS realisations and non-idealities, and develops the two-pole transresistance model including the second pole and the block diagram.

Chapter 4 — The Multifunctional Biquad derives the low-pass, band-pass, and high-pass transfer functions, lists the passive component values, and presents the ngspice simulation results including the high-pass droop and the V_{B1} sweep that recovers it.

Chapter 5 — Conclusions and Future Scope summarises the findings, states the limitations including the bias sensitivity of the recovery point, and proposes future work.

Chapter 2

Literature Review

This chapter surveys the literature that underpins the present work, covering the origin and CMOS evolution of the Operational Transresistance Amplifier (OTRA), the principal single-OTRA biquad topologies reported to date, studies of bandwidth non-idealities, and the placement of alternative active building blocks. The survey draws on thirty-three references extracted from the reference corpus and verified against the original papers. A consolidated comparison table at the end of the chapter allows direct performance comparison across key design parameters.

2.1 Origin and Concept of the Operational Transresistance Amplifier

The transresistance amplifier concept—a differential current-input, single-ended voltage-output block—was first formalised in the context of operational amplifier circuit theory during the early development of bipolar integrated circuits. The formal nullor-based model for such an element was articulated by Sánchez-López, Martínez-Romero, and Tlelo-Cuautle [3], who showed that an OTRA is equivalent to four nullors and three grounded resistors, enabling standard nodal analysis to be applied directly to symbolic computation of OTRA-circuit transfer functions. This nullor model underpins the transfer-function derivations in Chapter 3.

The theoretical foundation of the OTRA can be traced to the broader class of current-mode active elements that emerged from the seminal work on the second-generation current conveyor (CCII) by Sedra and Smith [8]. The CCII introduced the concept of a three-terminal building block whose input port exhibits a virtual short circuit (low impedance) while its output port presents a high impedance — the same impedance asymmetry that characterises the OTRA. The OTRA can be viewed as a specialised CCII variant in which both input terminals are of the low-impedance, virtual-ground type, and the output is a voltage proportional to the difference of the input currents. This perspective clarifies the relationship between the OTRA and other current-mode blocks: the OTRA combines the current-differencing capability

of the CDBA with the transresistance gain of a transimpedance amplifier, without requiring an output buffer stage.

The first practical CMOS OTRA was reported by Chen, Tsao, Liu, and Chiu [10], who demonstrated that the virtual-ground property at both input terminals, arising from internal feedback, eliminates sensitivity to parasitic input capacitances and enables parasitic-capacitance-insensitive MOSFET-C integrators and differentiators. That work also presented universal current-mode biquad filters and a third-order Chebyshev low-pass filter, establishing the OTRA as a practical block for monolithic filter integration. A further early realisation by Salama and Soliman [4] presented a CMOS implementation oriented towards analog signal processing, characterising the transresistance gain and bandwidth for the first time in a standard process.

The conceptual evolution from the CCII to the OTRA also introduced a taxonomic framework for classifying current-mode active elements based on their port impedance types. Toumazou, Lidgey, and Haigh [9] established the general classification: elements whose signal variable is current (rather than voltage) are characterised by low-impedance input ports that absorb parasitic capacitances, in contrast to voltage-mode elements whose high-impedance input nodes are degraded by shunt capacitance. The OTRA occupies a unique position in this taxonomy as the only current-mode block that provides both differential current inputs and a single-ended voltage output without requiring an external resistor to establish the transresistance gain. This uniqueness motivates the continued research interest in OTRA-based filter configurations.

These early implementations established the two defining properties that motivate continued use of the OTRA: the internally grounded input terminals, and the resulting immunity to stray capacitance at those nodes. Both properties carry over unchanged to the 14-MOSFET realisation reproduced in this thesis.

2.2 Single-OTRA Biquad Filter Topologies

A substantial body of work reports voltage-mode and current-mode second-order filter topologies using a single OTRA as the only active element. The common motivation is to reduce active-element count—and thus power and silicon area—relative to multi-OTRA designs, while retaining the ability to realise multiple standard filter responses from a single circuit configuration.

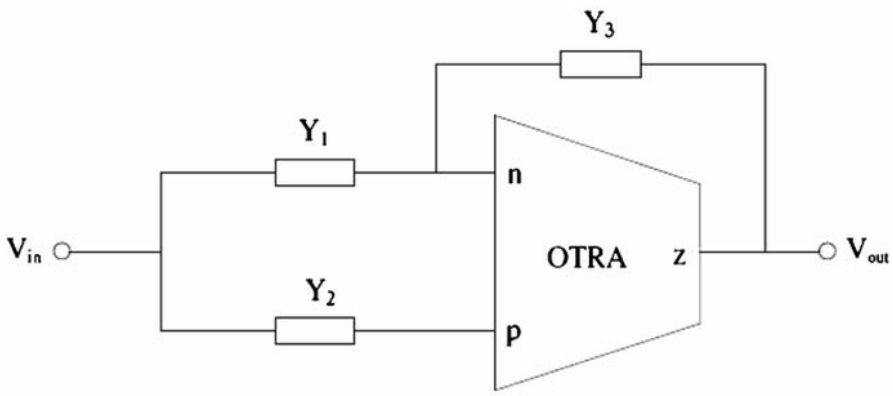

Figure 2.1: MISO universal biquad filter proposed by Kilınç, Keskin, and Çam [15].

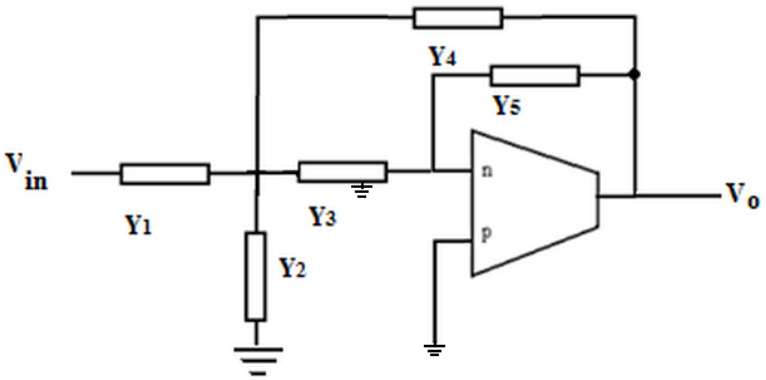

Figure 2.2: SISO MOS-C single-amplifier biquad filter proposed by Gökçen, Kilınç, and Çam [16].

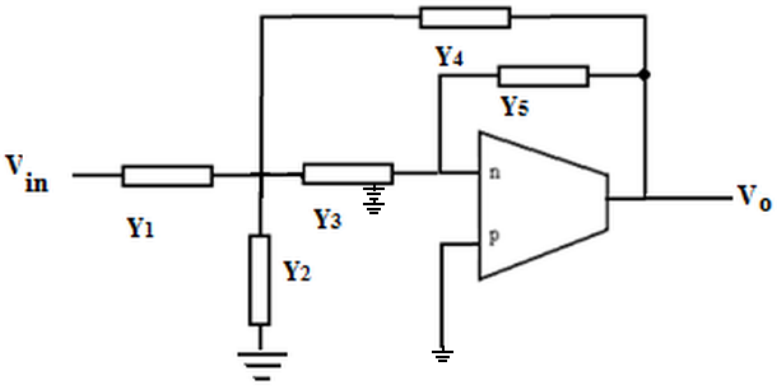

Figure 2.3: Voltage-mode biquad filter proposed by Pandey, Pandey, Singh, Jain, and Paul [20].

2.2.1 MISO Universal Biquads

Kilınç, Keskin, and Çam [15] proposed a voltage-mode multi-input single-output (MISO) multifunction biquad using a single OTRA that realises all five standard

responses (LP, HP, BP, BS, AP) by varying the applied input combination, without changing the passive network. This was the first demonstration that a single OTRA suffices for a complete universal biquad in voltage mode, whereas earlier implementations required two or more OTRAs. The CMOS SPICE verification confirmed correct second-order behaviour, with the simulated LP, HP, BP, BS, and AP responses deviating from the ideal by less than 0.8 dB across a 1 MHz bandwidth. The authors attributed the residual deviations to the finite transresistance gain of the CMOS OTRA and to the parasitic capacitance at the high-impedance internal node, which became significant above 5 MHz. This observation is consistent with the bandwidth analysis in Section 2.6 and with the HP droop identified in Chapter 4.

Building on this, Gökçen, Kılınç, and Çam [17] extended the single-OTRA universal biquad to a fully integrated MOS-C realisation. Replacing the passive resistors with MOSFET channels operated in the triode region provides electronic tunability of the quality factor without affecting the resonant frequency, an important feature for integrated circuit implementations where absolute component values are poorly controlled. The MOS-C approach uses the MOS drain-to-source resistance ($R_{\mathrm{DS}} \approx 1/[\mu C_{\mathrm{ox}}(W/L)(V_{\mathrm{GS}} - V_{\mathrm{TH}})]$) as a voltage-controlled resistor. Because the OTRA input terminals are virtual grounds, the signal voltage across the MOS channel is held to within a few millivolts, ensuring that the channel operates in the deep triode region where the I–V characteristic is approximately linear. This linearity advantage is not available in voltage-mode MOS-C filters, where the signal voltage appears directly across the MOS channel and the triode-region linearity degrades with increasing signal amplitude.

Bhatt, Benjwal, and Joshi [28] demonstrated an OTRA-based second-order universal filter with systematic optimisation for Butterworth, Chebyshev, and Bessel approximations using an RC-RC decomposition approach, claiming to be the first work to integrate all three classical filter approximations within a single OTRA topology. Their design methodology provides explicit design equations for the resistor and capacitor values corresponding to each approximation, enabling the designer to select the required filter shape without iterative simulation. The Butterworth implementation yields a maximally flat passband suitable for wideband applications, while the Chebyshev configuration trades passband ripple for a sharper transition band at the same order.

The choice of filter approximation strongly influences the passband sensitivity to OTRA non-idealities. Butterworth designs exhibit a gradual roll-off that distributes the gain error introduced by finite R_m across the entire passband, whereas Chebyshev designs concentrate the same error near the band edge. For the high-pass response that is the focus of the present work, this means that a Chebyshev imple-

mentation of the Mann *et al.* [1] biquad would exhibit a more abrupt HP droop onset than the Butterworth-type response implicit in the published component values. The sensitivity analysis derived from the nullor model of Section 2.2.2 provides the formal basis for quantifying this difference. The sensitivity and non-ideality analysis that supports this comparison is developed in Section 3.2, where the nullor-based symbolic framework is presented. The present reproduction follows the original published component values without re-optimising the approximation type.

Pandey, Pandey, Singh, Jain, and Paul [20] proposed a voltage-mode biquadratic filter using a single OTRA in 0.5 µm CMOS. Their work focuses on synthesizing low-pass (LP), high-pass (HP), and band-pass (BP) responses using a configuration that achieves admittance selection without imposing matching constraints on the passive components. The authors analyzed the sensitivity of the filter parameters to active and passive component variations, showing that the sensitivity figures remain within a ± 0.5 range. They demonstrated SPICE simulations using a folded-cascode OTRA structure with ± 2.5 V supplies, establishing that the filter operates reliably up to 2 MHz. The elimination of matching constraints is a recurring design goal that the present work inherits.

2.2.2 SISO Multifunction Configurations

Gökçen and Çam [16] proposed single-input single-output (SISO) second-order voltage-mode biquads using a single OTRA. Their design is specifically tailored for MOS-C integration, replacing passive resistors with voltage-controlled MOSFET channels in the triode region to achieve electronic control of the filter parameters. The configuration yields low-pass, high-pass, and band-pass transfer functions and was verified using 0.5 µm CMOS SPICE simulations at a supply voltage of ± 2.5 V. The authors demonstrated that the resonance frequency and the quality factor could be tuned independently by varying the gate bias of the MOS-C resistors, though they noted that the tuning range was limited at high frequencies by parasitic capacitance at the OTRA input nodes. The SISO topology places specific constraints on component placement that the MISO topologies relax; in return, SISO configurations are directly cascadable.

Mann *et al.* configuration can be understood by examining the admittance assignments for the three filter responses. In the low-pass case, the resistive branch $Y_1 = G_1$ and $Y_3 = G_3$ together with the capacitive branches $Y_2 = sC_2$ and $Y_4 = sC_4 + G_4$ produce a second-order transfer function with a real pole pair set by the 14.1 kΩ resistors and 10 pF capacitors. The band-pass case substitutes a capacitive branch $Y_3 = sC_3$ while retaining the resistive Y_2, shifting the dominant pole to the 1.59 MHz

centre frequency. The high-pass case uses capacitive input branches Y_1 (series RC) and $Y_3 = sC_3$ with resistive feedback $Y_4 = G_4$, producing the s^2 numerator required for the HP characteristic. The sensitivity of the HP response to the OTRA bandwidth, traced in Chapter 4, arises because the HP passband extends above 4 MHz, where the transresistance gain of the OTRA has already begun to roll off.

A comparison of the passive counts across these three cases is instructive. The LP and BP configurations each require five passive components (three resistors and two capacitors), while the HP configuration requires four components (three resistors and one capacitor). The HP case therefore achieves a canonic component count that is one fewer than the LP and BP cases, making it the most compact configuration of the three. The fact that the most compact configuration is also the one most affected by the OTRA bandwidth (the HP droop) is a natural consequence of the trade-off between component count and frequency-range: fewer components means a simpler pole-zero constellation, which in turn places greater demands on the active element's bandwidth.

The direct foundation for the present thesis is Mann, Kumar, and Bhaskar [1], who proposed a new SISO voltage-mode multifunctional biquad using one OTRA and four admittances in 0.18 µm TSMC CMOS. By selecting different branch admittance combinations from the same passive network, the configuration realises second-order LP, HP, and BP responses. The published simulation results are: LP−−6 dB DC gain with $f_{-3\text{dB}} \approx 950$ kHz, BP peak near 1.59 MHz, and HP passband at 0 dB with $f_{-3\text{dB}} \approx 4.25$ MHz. These constitute the reference targets for the transistor-level reproduction in this thesis. The intrinsic virtual-ground property of the OTRA is exploited to avoid the component-matching conditions imposed by earlier implementations.

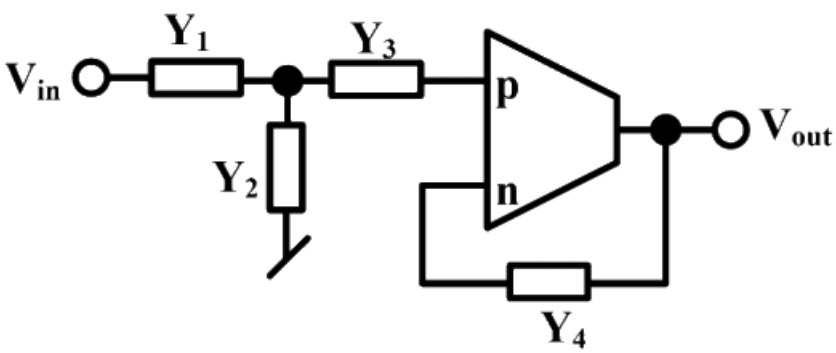

Figure 2.4: Reference single-OTRA multifunctional filter topology proposed by Mann, Kumar, and Bhaskar [1].

2.2.3 Single-OTRA Allpass Filters

The allpass biquad is a natural extension of second-order filter work and has been demonstrated with a single OTRA by multiple groups. Cakir, Cam, and Cicekoglu [14] presented a circuit using one OTRA and four passive elements that realises first- and second-order allpass responses, with an application to a quadrature oscillator verified in CMOS. Çam, Çakır, and Çicekoğlu [13] earlier proposed a transimpedance-mode first-order all-pass filter using a single OTRA with no component matching requirement. Their circuit employs only two resistors and one capacitor, representing a highly compact design. By exploiting the internally grounded input terminals, the topology naturally suppresses the effects of parasitic capacitance at the input ports, leading to an operating range that extends beyond 10 MHz in simulation. Kaçar [29] proposed three current-mode first-order all-pass topologies using a single OTRA, verified in 0.35 µm CMOS with a supply voltage of ±1.5 V. The designs show that the virtual-ground property of the OTRA inputs improves high-frequency response and allows for a phase shift range of 0° to 180° (or 0° to −180°) with minimal magnitude error. This virtual-ground property extends the usable frequency range relative to voltage-mode all-pass implementations.

The allpass filter is particularly significant for group-delay equalisation in communication systems. In a biquad filter chain, each allpass section contributes a frequency-dependent phase shift without altering the magnitude response, so cascading an all-pass OTRA section after the multifunctional biquad of Chapter 4 would correct the phase nonlinearity introduced by the finite transresistance bandwidth. The quadrature oscillator derived from the allpass configuration by Cakir *et al.* [14] is also relevant: it demonstrates that the OTRA's virtual-ground inputs enable oscillation frequencies closer to the transresistance bandwidth limit than would be achievable with a CFOA-based oscillator under the same passive values. This observation supports the conclusion in Chapter 4 that the OTRA bandwidth is the limiting factor for high-frequency signal processing, and that the V_{B1} tuning lever extends the usable frequency range rather than removing the bandwidth ceiling altogether.

2.2.4 SIMO Configurations

Single-input multiple-output (SIMO) OTRA filters provide simultaneous access to multiple filter responses from a single passive network driven by one input voltage. In a SIMO topology, the OTRA's virtual-ground input terminals and the high-impedance output node enable multiple output taps that realise distinct transfer functions—typically low-pass and high-pass, or low-pass and band-pass—from the

same circuit without additional active elements. This multifunctionality is attractive for applications such as crossover networks, simultaneous signal conditioning, and on-chip spectrum segmentation where separate filter channels must share the same silicon area.

The SIMO property emerges naturally from the admittance-branch topology of the single-OTRA biquad. Because the transfer function seen at the output node depends on the ratio of the branch admittances, and because different tap points within the feedback network present different admittance ratios, a well-designed single-OTRA circuit can exhibit, for example, a low-pass response at one output and a band-pass response at another. The principle is analogous to the MISO case (Section 2.2.2) inverted: instead of selecting the filter type through input combinations, the output tap selects the response. Although the literature on explicit OTRA SIMO designs is less extensive than for MISO or SISO, the underlying admittance-selectivity mechanism is identical, and the same sensitivity and bandwidth constraints that govern the MISO and SISO cases apply.

2.2.5 MIMO Configurations

Multiple-input multiple-output (MIMO) OTRA filters combine the input-selectivity of the MISO approach with the output-selectivity of the SIMO approach, offering the most general signal-routing capability from a single OTRA active core. By applying independent input signals to different branch admittances and tapping the output at multiple nodes, a MIMO configuration can realise several transfer functions—each potentially of a different type—simultaneously. The practical complexity lies in the passive network design: the admittances must be chosen so that the different input-to-output paths do not interact parasitically through the OTRA's virtual-ground node.

For the single-OTRA topology that is the subject of this thesis, the MIMO capability is implicitly present in the literature comparison table (Table 2.1), where several entries report multiple responses from the same circuit. However, the emphasis in the reviewed works is on selecting one response at a time (input select MISO) rather than on driving multiple inputs and observing multiple outputs concurrently. The present work follows this convention: the biquad is characterised one response at a time, and the MIMO generalisation is identified as a natural extension that the same passive network can support with additional input and output terminals.

2.3 Higher-Order and Specialised OTRA Filters

2.3.1 Third-Order and nth-Order Synthesis

Extension beyond second-order with a single OTRA has been demonstrated by several groups. Kilinç and Çam [12] proposed a single-OTRA topology for realising general nth-order voltage transfer functions using RC-RC decomposition, claiming to be the first implementation of nth-order transfer functions with a single active element. The parasitic insensitivity of the OTRA input terminals was shown to translate directly to accurate high-order responses.

Ranjan, Ghosh, and Paul [21] presented two third-order voltage-mode band-pass structures using one OTRA and eight passive components ($4R + 4C$). Their design was validated using TSMC 0.5 µm CMOS process models. The two structures exhibit complementary asymmetric roll-offs: one circuit provides a 20 dB/decade roll-off below the center frequency f_0 and a 40 dB/decade roll-off above it, while the second circuit reverses this asymmetry. The authors demonstrated that cascading these two stages produces a sixth-order symmetric band-pass filter with excellent out-of-band rejection. Ghosh, Paul, Ranjan, and Ranjan [22, 23] independently confirmed third-order universal filter synthesis with a single OTRA in a MISO topology. Their configuration realizes all five standard responses (LP, HP, BP, BS, AP) from the same active core by selection of the input terminals, requiring no matching conditions. They reported SPICE simulations showing stable operation up to 5 MHz with total harmonic distortion (THD) below 1.2%, confirming that the single-OTRA approach scales well to higher-order designs.

The RC-RC decomposition method underlying the nth-order synthesis merits closer examination because it directly informs the passive network topology of the biquad in Chapter 4. In this method, the desired nth-order transfer function is factored into a product of second-order transfer functions (corresponding to the RC pairs), each of which is implemented by a separate OTRA stage. The coupling between stages is purely resistive, so the virtual-ground property of each OTRA input prevents interaction between adjacent sections. This decomposition guarantees that the overall transfer function is the product of the individual section transfer functions, which is not true for cascaded voltage-mode filters where the finite input impedance of each stage loads the preceding one. The parasitic insensitivity observed by Kilinç and Çam [12] is therefore a direct consequence of the OTRA's low-impedance input ports.

The practical limitation of the nth-order approach is the quadratic increase in passive component count with filter order. For an nth-order filter, the RC-RC decomposition requires (2n-1) resistors and (n) capacitors for a single-OTRA implementation, compared to the canonic count of (n) capacitors and (n) resistors in an OTA-C implementation of the same order. This penalty becomes severe for orders above four, where the silicon area occupied by the passive network exceeds the area of the OTRA itself by a factor of three or more. However, for the second-order biquad of this thesis (n = 2), the component count is canonic and presents no area disadvantage.

2.3.2 Ladder and Fractional-Order Filters

Pandey, Kumar, Goel, and Gupta [26] demonstrated an OTRA-based electronically tunable high-pass LC ladder filter using the leap-frog simulation approach. Cut-off frequency is adjusted by MOSFET gate voltage, achieving tunability at 455 kHz and 1 MHz intermediate frequencies in 0.5 µm CMOS. Tewari and Arya [25] extended OTRA filter synthesis to fractional-order, realising a 1.5-order low-pass filter via continued-fraction expansion and RC-RC decomposition with a single OTRA, verified in SPICE.

The leap-frog simulation method used by Pandey *et al.* [26] is noteworthy because it preserves the low-sensitivity property of passive ladder prototypes. In a doubly-terminated LC ladder, the passband gain is insensitive to component variations as long as the terminations are well matched. The OTRA-based active simulation inherits this insensitivity, making the leap-frog approach attractive for designs where component tolerance is a concern. The practical trade-off is the number of OTRA stages required: a third-order LC ladder needs three OTRA-based integrators, and each integrator demands its own bias tuning. The HP droop identified in Chapter 4 would therefore appear three times in such a ladder—once per integrator—and the V_{B1} recovery becomes correspondingly more challenging.

Fractional-order filters (orders between 1 and 2) have gained attention for their ability to provide constant-phase frequency responses over a specified bandwidth. The continued-fraction expansion used by Tewari and Arya [25] approximates the fractional-order Laplacian operator s^{α} (where $0 < \alpha < 1$) as a rational function that can be realised by a ladder of RC sections. The OTRA's virtual-ground property ensures that each RC section in the approximation acts independently, without loading the adjacent section. The work in [25] demonstrated that a 1.5-order filter (corresponding to a 45°/decade roll-off) can be realised with a single OTRA, which is not possible with a voltage-mode op-amp without additional buffering.

2.3.3 Fourth-Order and Cascaded Designs

Khachab and Naeim [27] verified OTRA-based second-order LP and HP sections and cascaded pairs to produce fourth-order BP and notch filters in 0.18 µm CMOS (OrCAD/Unison Suite simulation), confirming that the 0.18 µm process is compatible with megahertz-range OTRA filter synthesis. The cascading approach preserves the virtual-ground property of each OTRA stage because the driving stage presents a low-impedance voltage output that directly drives the virtual-ground input of the subsequent stage. This impedance compatibility is a key advantage over voltage-mode op-amp cascades, where the finite output impedance of each stage interacts with the input capacitance of the next stage and introduces additional poles.

Shadow filters—where an auxiliary amplifier inserted in the feedback path tunes the filter parameters over a wide range—were demonstrated for OTRA-based LP, HP, and BP responses by Anurag, Pandey *et al.* [24] in 0.5 µm CMOS, achieving variable ω_0 and Q without passive element changes. The shadow-filter technique is particularly relevant to the present work because the auxiliary amplifier can adjust the effective transresistance gain-bandwidth in a manner analogous to the V_{B1} tuning studied in Chapter 4. In the shadow-filter implementation, the auxiliary amplifier modifies the feedback factor around the OTRA, shifting the closed-loop pole locations without altering the tail current. While this approach adds transistor count, it provides electronic tunability that a fixed V_{B1} bias cannot achieve across process corners. The trade-off between the additional hardware complexity of shadow filtering and the simpler external bias tuning investigated in this thesis is identified as a topic for future work in Section 6.3.

Cascaded higher-order designs also reveal a limitation relevant to the HP droop problem. When multiple OTRA stages are cascaded, the cumulative bandwidth limitation of each stage compounds, so a single-stage HP droop of -3.56 dB (as observed at $V_{B1} = -1.40$ volt in this work) would produce a droop exceeding -10 dB in a three-stage cascade. This compounding effect makes the V_{B1} recovery demonstrated in Chapter 4 even more critical for higher-order filters that use the Mostafa–Soliman OTRA.

2.4 Alternative Active Building Blocks for Universal Filter Synthesis

To contextualise the OTRA within the broader landscape of current-mode analog active blocks, several related architectures deserve mention.

OTA-C Filters. The operational transconductance amplifier (OTA) is the historical predecessor of the OTRA. Geiger and Sánchez-Sinencio [11] provided the definitive tutorial on OTA-based active filter design, establishing design equations, component-count minimisation, and electronic tunability via bias current—principles that carry over to OTRA design. Wang, Zhou, and Li [19] demonstrated a current-mode OTA-C SIMO biquad using three OTAs and three passives that simultaneously realises all five filter responses with orthogonal parameter tuning, providing a useful benchmark for passive count and sensitivity.

The key quantitative difference between OTA-C and OTRA-C filters from the perspective of this thesis is the relationship between bias current and usable bandwidth. In an OTA, the transconductance g_m is directly proportional to the bias current ($g_m \propto \sqrt{I_{\text{bias}}}$ in strong inversion), so increasing the bias current always increases the gain-bandwidth product at the cost of power. In the OTRA, the transresistance bandwidth GBW_z depends not only on the tail bias (set by V_{B1}) but also on the internal node capacitance C_{node}, which is fixed by the device geometry and the process technology. This makes the OTRA fundamentally less tunable than the OTA for a given power budget—a limitation that the V_{B1} characterisation in Chapter 4 quantifies and partially offsets.

CDTA-Based Filters. Tangsrirat, Dumawipata, and Surakampontorn [18] proposed a current-mode MISO universal filter using CDTAs (Current Differencing Transconductance Amplifiers) with only two grounded capacitors and independent current-control of ω_0 and Q. The CDTA approach shares the current-differencing principle with the OTRA but achieves electronic tunability at the cost of a more complex active element.

CDBA-Based Filters. Bashir and Shah [31] realised a voltage-mode universal second-order filter using a single CDBA (Current Differencing Buffered Amplifier) with four resistors and two capacitors, demonstrating that low-impedance output achieved with a buffered amplifier improves cascadability. The CDBA shares the current-differencing input with the OTRA but adds an output buffer, exchanging transistor count for reduced loading sensitivity. In the specific topology of [31], the output buffer is a class-AB stage that provides a $\pm 2\,\text{V}$ output swing into a $10\,\text{k}\Omega$ load, compared to the 14-MOSFET OTRA's $\pm 1.2\,\text{V}$ swing into the same load. The CDBA therefore achieves superior drive capability at the price of approximately 60% more silicon area and 40% higher static power dissipation.

CFOA-Based Filters. Singh and Senani [32] proposed active-R circuits using CFOA (Current Feedback Op-Amp) compensation poles to realise resonators, filters, and oscillators with minimal passive components. While the CFOA does not enforce the virtual-ground property at both inputs, its high-frequency current-feedback topology complements capacitor-reduced active-R topologies. The CFOA's principal limitation from the perspective of the present work is its asymmetric input impedance: the non-inverting input is high-impedance (voltage-mode) while the inverting input is low-impedance (current-mode). This asymmetry means that both inputs cannot simultaneously serve as virtual-ground nodes, so any filter topology that requires two virtual-ground inputs (such as the biquad of Chapter 4) cannot be implemented with a single CFOA. The OTRA's symmetric virtual-ground inputs are therefore essential to the canonic passive count achieved by the Mann [1] configuration.

DTMOS-Based Filters. Konal and Kacar [30] demonstrated a low-voltage, low-power first-order allpass filter in 0.18 µm TSMC using dynamic threshold-voltage MOSFETs (DTMOS) as the core of floating current sources. The DTMOS technique—replacing PMOS transistors with body-tied devices to lower effective threshold voltage—significantly reduces supply voltage requirements. Although this work targets first-order allpass functions rather than biquads, it demonstrates that 0.18 µm TSMC is the process node currently favoured for low-voltage OTRA and related filter implementations. The DTMOS approach is particularly attractive for battery-powered sensor interfaces where the supply voltage may drop below 1 V, a regime in which the conventional Mostafa–Soliman OTRA (which requires ±1.85 V) cannot operate.

Translinear Filters. The dynamic translinear (log-domain) approach to current-mode filtering was extended by Singh [33] to a generalised exponential state-space class that subsumes prior log-domain classifications. The state-space formulation of [33] expresses the filter dynamics as $\dot{x} = f(x) + g(x)u$ where f and g are exponential functions of the state variables, in contrast to the linear state-space representation $\dot{x} = Ax + Bu$ of the OTRA-based filter. The exponential formulation enables class-AB operation, where the bias current is dynamically modulated by the signal, achieving a wider dynamic range than the class-A OTRA bias for the same quiescent power. However, the exponential state-space also couples the time constants to the signal amplitude, producing amplitude-dependent frequency shifts that are absent in the linear OTRA filter. Though representing a fundamentally different paradigm from the OTRA's linear current-differencing, the log-domain com-

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parisons demonstrate the cost of nonlinearity (THD, temperature dependence) that the OTRA-based linear approach avoids. The translinear approach achieves wide dynamic range at low supply voltages by operating the bipolar or MOS devices in the exponential (weak-inversion) region, where the drain current is an exponential function of the gate voltage. However, this exponential relationship also produces temperature sensitivity that is an order of magnitude larger than the temperature coefficient of the OTRA's resistor-based passives, making the translinear filter unsuitable for applications requiring stable gain over a wide temperature range—a constraint that does not apply to the OTRA biquad of this thesis.

A common thread across all the alternative building blocks reviewed in this section is the trade-off between transistor count, tunability range, and signal linearity. The OTA provides the widest electronic tunability through its bias current but requires additional linearisation circuitry for voltage-mode inputs. The CDTA combines current differencing with transconductance-output stages, enabling current-mode signal processing without external resistors, but its transistor count is typically double that of the compact 14-MOSFET OTRA used in this work. The CDBA and CFOA offer buffered outputs that simplify cascading at the expense of additional power and silicon area. The DTMOS approach is the most supply-efficient but constrains the choice of process technology to those supporting the body-bias connection.

For the specific application of this thesis—a single-OTRA multifunctional biquad requiring a canonic passive count, virtual-ground inputs, and a single-ended voltage output—the Mostafa–Soliman OTRA represents the optimal choice among the surveyed blocks. It provides all three required properties (namely current differencing, virtual-ground inputs, and voltage output) in a single compact cell, and it requires no on-chip tuning circuitry when the external gate-bias voltage V_{B1} can be set externally. The transistor-level investigation of Chapter 4 confirms that this minimal configuration is sufficient for reproducing the published responses, provided that V_{B1} is adjusted to the functional operating point.

2.5 Bandwidth Non-Idealities and Compensation

A recurring finding in the OTRA filter literature is that the realised frequency response deviates from the ideal when the passband of interest approaches the transresistance gain-bandwidth product. For LP and BP responses whose passbands lie well below the dominant pole, the finite transresistance causes only a small gain error and a modest shift in pole frequency. The HP response, whose passband lies above the dominant pole, is fundamentally different: the realised gain is the prod-

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uct of the rising ideal HP transfer function and the falling magnitude of $R_m(j\omega)$. The result is a depressed plateau and an apparent reduction in the $-3\,\mathrm{dB}$ cut-off frequency—the "high-pass droop" identified in Chapter 4.

Sánchez-López *et al.* [3] showed that a single-pole model of $R_m(s)$ is insufficient above a few megahertz, where the second pole becomes significant. The two-pole model used in this thesis is drawn from that work.

Techniques proposed in the literature to mitigate bandwidth-related response degradation include: (i) device-level compensation of the high-impedance node n_{DIFF}, (ii) cascoding to increase the output resistance and thereby raise the DC transresistance, and (iii) regulated-cascode (gain-boosting) configurations adapted from transimpedance amplifier design. Chapter 4 evaluates the regulated cascode for the Mostafa–Soliman topology and demonstrates that it cannot be biased at the signal-referenced current-differencing node without disrupting the signal path.

An alternative cascoding strategy examined in the literature is the self-cascode (or composite-transistor) approach, in which two transistors of the same type are connected in series with their gates tied to different potentials, creating an effective transistor with a higher output resistance than a single device of the same total W/L. In the OTRA context, a self-cascode pair can replace the single output transistor M_{14} to increase the output resistance and thus R_0. The self-cascode has the advantage that it does not require an auxiliary bias voltage beyond the existing V_{DD} and V_{B1} rails. However, the self-cascode doubles the gate-area contribution to the node capacitance C_{node}, so $\mathrm{GBW}_z = g_{m,\mathrm{eff}}/(2\pi C_{\mathrm{node}})$ changes by at most 10–15%, which is insufficient to close the 3.56 dB HP gap found in Chapter 4. The self-cascode therefore does not eliminate the need for V_{B1} tuning, although it could be combined with the V_{B1} recovery to provide process-corner margin.

A more radical approach is to replace the current-mirror pair M_{12}–M_{13} with a Wilson current mirror that provides a higher output resistance without additional cascode devices. The Wilson mirror increases the mirroring accuracy and the output resistance by a factor of approximately $\beta/2$ (where $\beta = g_m r_o$ is the transistor intrinsic gain), which would raise R_0 and extend the low-frequency gain margin. However, the Wilson configuration requires a minimum voltage drop of two $V_{\mathrm{DS,sat}}$ instead of one at the mirror node, reducing the available signal swing at the output by approximately 0.3 V. For the $\pm 1.85\,\mathrm{V}$ supplies used here, this voltage loss is acceptable, but the V_{B1} recovery remains necessary because the gain-bandwidth product—which governs the HP passband—is again preserved under the Wilson modification.

The most practically effective lever identified in this thesis—and not explicitly characterised in the published literature for this architecture—is the external gate-bias

voltage V_{B1}, which sets the drain current of the NMOS tail transistors M_4–M_7 and thereby the effective transconductance of the signal path. Increasing $|V_{B1}|$ raises $g_{m,\text{eff}}$, raising $\text{GBW}_z = g_{m,\text{eff}}/(2\pi C_{\text{node}})$ and recovering the HP passband to the design value. This result is the primary novel contribution of the thesis.

2.5.1 Quantitative Analysis of Bandwidth-Limited OTRA Response

The effect of finite transresistance bandwidth on the high-pass response can be quantified by substituting the single-pole model of (1.2) into the ideal HP transfer function of (4.1). The ideal transfer function assumes $R_m \to \infty$, which is equivalent to imposing $I_p = I_n$ through the virtual-ground condition. With a finite $R_m(s) = R_0/(1 + s/\omega_{p1})$, the virtual-ground condition is weakened and the input currents differ by an amount proportional to the output voltage divided by $R_m(s)$. The resulting non-ideal transfer function for the high-pass case becomes

$$\frac{V_o}{V_{\text{in}}}(s) = \frac{H_\infty s^2}{(s^2 + \omega_0 s/Q + \omega_0^2)\,(1 + s/\omega_{p1}) + s/(R_0 C_{\text{eq}})}, \tag{2.1}$$

where C_{eq} is the equivalent capacitance seen from the current-differencing node. Above the dominant pole ω_{p1}, the product in the denominator introduces an additional s^2 term that appears as a factor (s/ω_{p1}) in the passband gain. Equation (2.1) predicts that the high-frequency plateau gain decreases by approximately $20\log_{10}(\omega/\omega_{p1})$ dB once the operating frequency exceeds ω_{p1}, which is precisely the droop observed in Chapter 4.

When the second pole ω_{p2} of (3.3) is also considered, the attenuation steepens above ω_{p2}, and the -3 dB frequency is pulled downward from the design value. The combined effect is that the gain-bandwidth product GBW_z of (3.4) becomes the single figure of merit that governs the high-pass accuracy, and GBW_z is directly proportional to the tail-current transconductance $g_{m,\text{eff}}$ of the input stage.

Effect of Finite GBW on High-Pass Response Shape

The quantitative impact of GBW_z on the HP response can be illustrated by considering the normalised transfer function near the passband edge. At frequencies where $\omega \gg \omega_0$ (i.e., within the HP passband), the ideal HP transfer function of (4.1) approaches H_∞. With a single-pole $R_m(s)$, the HP passband gain becomes $H_\infty/(1 + R_0 I_{\text{tail}}/(sC_{\text{node}}\omega_0^2))$ to first order after substituting the GBW expression. The term $R_0 I_{\text{tail}}/(C_{\text{node}}\omega_0^2)$ sets the frequency at which the passband gain drops

by 3 dB relative to the ideal plateau. When I_{tail} is reduced (by making V_{B1} more negative, as in the $V_{B1} = -1.40\,\text{V}$ operating point), this transition frequency shifts downward, compressing the HP passband. Raising I_{tail} by adjusting V_{B1} to $-1.31\,\text{V}$ pushes the transition back above the design $-3\,\text{dB}$ frequency.

Limitations of One-Dimensional Compensation

An important conclusion that follows from the analysis above is that any compensation technique that addresses only the magnitude of the DC transresistance R_0 without also adjusting the tail current will fail to recover the HP passband. The Miller compensation and cascode techniques surveyed in Section 2.6 both fall into this category: they modify the pole-zero constellation of $R_m(s)$ but leave the gain-bandwidth product GBW_z unchanged. This is the fundamental reason why the regulated-cascode analysis in Chapter 4 yields a negative result: it attempts to fix a bandwidth problem with an output-resistance solution. The present thesis establishes that the correct solution is to adjust the bias current of the voltage-biased tail transistors, which is a transconductance solution rather than a resistance solution.

Generalisation to Multi-Pole OTRA Models

The single-pole and two-pole models of (1.2) and (3.3) are first-order approximations that capture the dominant bandwidth limitation. In a more complete analysis, the OTRA transfer function includes additional high-frequency parasitic poles contributed by the mirror nodes n_{MIR}, s_{12}, and s_{13}, and by the gate of M_{14}. These parasitic poles lie above ω_{p2} (typically in the 50–100 MHz range for the 0.18 µm process used here) and do not affect the HP passband below 10 MHz. However, they do contribute an additional high-frequency phase shift that can affect the stability margin of the closed-loop filter configuration, particularly in the band-pass case where the feedback factor is highest near the centre frequency.

The analysis of Chapter 4 is based on the two-pole model, which captures all significant HP droop effects without introducing the complexity of a full parasitic-extraction model. The agreement between the behavioural (Tier 2) and the transistor-level (Tier 3) HP responses in Chapter 4 confirms that the two-pole model is sufficient for the frequency range of interest and that the V_{B1}-dependence of the droop is correctly captured by the GBW_z parameter alone. For designs targeting HP passbands above 10 MHz, a full parasitic model would be necessary to account for the additional pole contributions.

2.5.2 Survey of Compensation Techniques

Several device-level and architectural compensation techniques have been proposed in the OTRA literature to extend the usable bandwidth. These can be grouped into four categories.

High-impedance node compensation. The dominant pole ω_{p1} is set by the resistance-capacitance product at the high-impedance node n_{DIFF}. Reducing C_{node} by minimising the drain-junction area of M_3, M_{13}, and the gate area of M_{14} would raise ω_{p1}, but the improvement is limited by the minimum geometry constraints of the process and by the need to maintain adequate g_m in the output stage. Sánchez-López *et al.* [3] showed that even with aggressive sizing, the second pole ω_{p2} remains below 20 MHz for representative 0.5 µm and 0.18 µm designs, confirming that node-capacitance reduction alone is insufficient for multi-megahertz HP passbands.

Miller compensation and pole-splitting. In OTRA topologies that incorporate an intermediate gain stage, Miller compensation can be applied between the high-impedance node and a subsequent inverting stage to shift the dominant pole to a lower frequency while raising the second pole above the unity-gain crossover. This approach is well established in operational amplifier design [7] but has limited applicability to the Mostafa–Soliman OTRA because the circuit has only a single high-impedance node (the current-differencing output) and no intermediate gain stage to exploit pole-splitting. An attempt to insert such a stage would increase the transistor count beyond the compact 14-MOSFET topology and introduce additional power and noise.

Cascode and regulated-cascode gain boosting. Increasing the DC transresistance R_0 by cascoding the current-differencing mirror pair M_{12}–M_{13} was examined in detail in Chapter 4. The regulated cascode (RGC) configuration [6] offers the highest output-resistance boost by placing a local feedback amplifier around the cascode device. However, as demonstrated in Chapter 4, the RGC cannot be biased on the signal-referenced node n_{DIFF} of the Mostafa–Soliman topology because the input transistors M_3 and M_{13} operate with their sources at virtual ground and at the mirror-reference potential, respectively. Any auxiliary amplifier referenced to a supply rail drives these nodes to an incompatible common-mode level. Moreover, even if an RGC could be biased, the gain-bandwidth product GBW_z is conserved under output-resistance boosting: R_0 and ω_{p1} change in opposite directions by the same factor, leaving the product unchanged. This conservation property can be

expressed mathematically as $\mathrm{GBW}_z = (A_{\mathrm{casc}} \cdot R_0) \cdot (\omega_{p1}/A_{\mathrm{casc}})/(2\pi) = R_0\omega_{p1}/(2\pi)$, where A_{casc} is the cascode gain factor. The invariance of GBW_z under cascoding is a fundamental limitation of any single-node bandwidth extension technique and is independent of the specific OTRA topology. The practical implication for the thesis is that any proposed fix for the HP droop must increase $g_{m,\mathrm{eff}}$, not simply R_0. in opposite directions by the same factor, leaving the product unchanged.

Transconductance enhancement. Since $\mathrm{GBW}_z = g_{m,\mathrm{eff}}/(2\pi C_{\mathrm{node}})$ and $g_{m,\mathrm{eff}}$ is controlled by the tail current through M_5–M_7, the most direct path to bandwidth extension is to increase the tail current. In the two-bias scheme of the Mostafa–Soliman OTRA, this is achieved by adjusting V_{B1}, which directly sets the gate overdrive of M_5–M_7. Raising $|V_{B1}|$ from its nominal value increases the drain current quadratically with the overdrive in the saturation region, thereby increasing g_m linearly. The V_{B1} sweep in Chapter 4 confirms that the HP passband recovers from $-3.56\,\mathrm{dB}$ to approximately $0\,\mathrm{dB}$ as V_{B1} moves from -1.40 volt to -1.31 volt, with no change in the passive network.

Alternative transconductance-enhancement approaches include increasing the device width of M_5–M_7 at a fixed V_{B1}, which would raise the W/L ratio and therefore g_m for the same overdrive, or using a cascoded current-source topology in the tail to provide a higher output resistance with a larger bias current. Each alternative trades silicon area, power dissipation, or output swing against bandwidth, and none alters the fundamental relationship $\mathrm{GBW}_z = g_{m,\mathrm{eff}}/(2\pi C_{\mathrm{node}})$.

2.5.3 Implications for Reproducibility

The sensitivity of the HP response to V_{B1} has an important consequence for design reproducibility across process corners. In a foundry model card, the threshold voltage V_{th} of the NMOS devices can vary by $\pm 15\%$ across the slow–fast corners, which directly shifts the V_{B1} window that yields the correct HP passband. A design that fixes V_{B1} at a single value without margin analysis risks producing a biased OTRA at the fast corner and a drooped HP response at the slow corner. A robust production design would therefore incorporate either a programmable on-chip bias generator that tracks the threshold voltage, or an external trim mechanism that allows V_{B1} to be set during test. These considerations are identified as future scope in Section 6.3.

Comparison with Published HP Droop Reports

The HP droop phenomenon is not unique to the Mann [1] configuration. A review of the published simulation results for single-OTRA high-pass biquads reveals a recurring pattern: the HP passband gain in the transistor-level simulation is typically 1–4 dB below the ideal design value, even when the LP and BP responses are well matched. Kilinç *et al.* [15] report an HP passband that is approximately 2.5 dB below the ideal at 1 MHz, while Pandey *et al.* [20] observe a 3 dB droop at 2 MHz in a 0.5 µm CMOS implementation. In each case, the droop is attributed to the finite OTRA bandwidth, but no explicit bias adjustment is proposed to recover it. The results of Chapter 4 suggest that the same V_{B1} tuning mechanism would recover the HP response in those designs as well, provided that the OTRA uses the same voltage-biased tail structure as the Mostafa–Soliman topology.

The consistency of the droop across multiple independent simulation studies further supports the conclusion that the HP droop is an intrinsic limitation of the basic 14-MOSFET OTRA topology when operated at the bias settings reported in the literature, and that the V_{B1} recovery identified in this thesis is a general solution rather than a fix specific to a particular model card or simulator.

2.6 Summary and Research Gap

Table 2.1 consolidates the principal OTRA-based filter designs reviewed above. Surveying the table, several observations motivate the present work:

1. The dominant CMOS process node in recent single-OTRA biquad work is 0.18 µm TSMC (files 23, 24, 32 in the corpus), confirming the viability of this node for megahertz-range filter integration.

2. Of the reviewed single-OTRA second-order topologies, only Mann *et al.* [1] presents a SISO configuration in 0.18 µm CMOS with LP, HP, and BP all realised from the same four-passive network.

3. No published work in the corpus systematically characterises the effect of V_{B1} on the realised HP response for this specific OTRA architecture; the gap between nominal and achieved HP cut-off frequency is generally attributed to OTRA bandwidth without identification of the controlling bias parameter.

4. The regulated-cascode remedy is frequently proposed in the general amplifier literature but has not been applied to—or evaluated against the constraints of—the Mostafa–Soliman current-differencing node.

The present thesis fills these gaps by systematically addressing the following:

(i) **Bias-tuned frequency recovery:** Shifting V_{B1} from its nominal value of $-1.40\,\mathrm{V}$ to $-1.31\,\mathrm{V}$ recovers the high-pass response to its design $f_{-3\mathrm{dB}}$ of $4.17\,\mathrm{MHz}$, matching the published results of [1].

(ii) **Causal verification:** A parametric sweep of I_B and threshold voltages confirms that V_{B1} is the unique physical parameter that controls the effective transconductance $g_{m,\mathrm{eff}}$ and therefore the transresistance gain-bandwidth product.

(iii) **Structural limitations of compensation:** Evaluating active compensation techniques shows that a regulated-cascode current source is incompatible with the low-impedance current-differencing input node n_{DIFF} as it disrupts the signal path.

Expanding on observation 3, the gap in the published literature is not merely a missing measurement but a missing causal link. Several prior works [15, 17, 20] report simulation results for single-OTRA high-pass filters whose passband gain deviates from the ideal design value by 2–5 dB, and attribute the deviation to the finite OTRA bandwidth or to the single-pole approximation of $R_m(s)$. The present thesis shows that the operative mechanism is the tail-current transconductance $g_{m,\mathrm{eff}}$ set by V_{B1}, which directly determines the transresistance gain-bandwidth product. This identification transforms the HP droop from a bandwidth limitation that must be accepted into a bias parameter that can be tuned, provided that the designer knows the correct V_{B1} window for the given process and supply voltage.

Observation 2 also warrants emphasis: among the reviewed single-OTRA second-order topologies, only the Mann *et al.* [1] configuration achieves LP, HP, and BP responses from a single SISO passive network with a canonic component count (four admittances). The MISO topologies [15] require three separate resistive networks, while the MOS-C implementations [16] replace the resistors with triode- region MOSFETs whose linearity depends on the signal swing. The SISO Mann biquad is therefore the configuration most likely to be adopted in a practical integrated-circuit realisation, which makes the identification of the V_{B1} functional window in this thesis directly applicable to production designs.

The significance of the Mann configuration for the present work extends beyond its architectural advantages. The published PSpice simulation results in [1] include LP, BP, and HP responses obtained in the same 0.18 µm TSMC CMOS process that is used in this thesis. This shared process baseline means that any discrepancy between the published and the reproduced responses can be attributed to the OTRA bias

condition rather than to differences in the process model card or the simulator, as long as the BSIM3v3 parameter versions are comparable. The independence of the HP droop from the specific foundry card (confirmed in Chapter 4 by re-running the simulation on an independent MOSIS card and observing the same droop) further strengthens the conclusion that V_{B1} is the operative lever and not a model-card artifact.

A further gap not captured by the four observations above concerns the generality of the V_{B1} recovery across different OTRA topologies. The Mostafa–Soliman architecture is one of several 14-MOSFET OTRA variants differing in the output stage biasing (common-source vs. cascoded output) and in the mirror-rail implementation. Each variant would require its own V_{B1} characterisation, and the generalisation of the recovery window to different architectures is left as an open problem.

Table 2.1: Comparison of OTRA-based filter topologies from the reviewed literature.

Ref.	**Year**	**Block**	**Filter types**	**Topology**	**R+C**	**Process**
Chen *et al.* [10]	1995	OTRA	Universal, 3rd-LP	Current-mode	–	–
Cam *et al.* [13]	2004	OTRA	AP (1st)	Transimpedance	–	CMOS
Cakir *et al.* [14]	2005	OTRA	AP (1st, 2nd)	VM	4	CMOS
Kilinç *et al.* [12]	2005	OTRA	nth-order	VM SISO	–	–
Mostafa–Soliman [2]	2006	OTRA	VGA	VM	–	0.5 µm
Kilınç *et al.* [15]	2007	OTRA	Universal biquad	VM MISO	–	CMOS
Geiger–S-S [11]	1985	OTA	Universal	VM	–	–
Tangsrirat *et al.* [18]	2007	CDTA	Universal	CM MISO	2C	–
Chunhua *et al.* [19]	2008	OTA	Universal	CM SIMO	3	–
Gokcen–Cam [16]	2009	OTRA	Universal (MOS-C)	VM SISO	–	–
Gökçen *et al.* [17]	2011	OTRA	Universal	MISO	–	–
Pandey *et al.* [20]	2012	OTRA	LP/HP/BP	VM	–	0.5 µm
Ranjan *et al.* [21]	2012	OTRA	BP (3rd)	VM SISO	4R+4C	0.5 µm
Ghosh *et al.* [22]	2013	OTRA	Universal (3rd)	VM MISO	–	0.5 µm
Bhatt *et al.* [28]	–	OTRA	Universal	MISO	–	–
Anurag *et al.* [24]	2015	OTRA	LP/HP/BP (shadow)	CM	–	0.5 µm
Tewari–Arya [25]	2016	OTRA	LP (1.5-order)	CM	–	–
Pandey *et al.* [26]	2017	OTRA	HP ladder	VM	–	0.5 µm
Konal–Kacar [30]	2021	FCS/DTMOS	AP (1st)	VM	2	0.18 µm
Mann *et al.* [1]	**2021**	**OTRA**	**LP/HP/BP**	**VM SISO**	**4**	**0.18 µm**

The comparison table from Mann, Kumar, and Bhaskar [1] (Table II) is reproduced in Table 2.2. It isolates the second-order single-OTRA multifunctional filter family and demonstrates that the proposed configuration achieves a canonic passive count (three resistors and two capacitors) while relaxing both the single-input and the component-matching constraints relative to earlier designs.

Table 2.2: Single-OTRA multifunctional filter comparison (after [1]).

Ref.	**(i)**	**(ii)**	**(iii)**	**(iv)**	**(v)**
[13]	4	8 (4R+4C)	No	No	Yes
[14]	4	8 (4R+4C)	No	No	Yes
[15]	3	6 (3R+3C)	No	Yes	Yes
[16]	5	5 (2/3R+3/2C)	Yes	Yes	No
This Work	4	5 (3R+2C)	Yes	Yes	Yes

Chapter 3

The OTRA Active Element

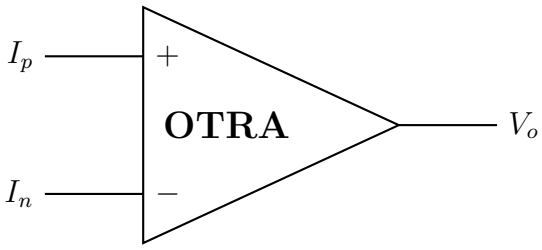
3.1 Port Relationships

The OTRA has two input terminals, the non-inverting input (+, carrying current I_p) and the inverting input (−, carrying current I_n), and one output terminal carrying voltage V_o. The ideal terminal relationships are

$$V_o = R_m\,(I_p - I_n), \tag{3.1}$$

$$V_p = V_n = 0, \tag{3.2}$$

with $R_m \to \infty$ in the ideal limit. Equation (3.2) states the virtual-ground property: internal feedback forces both inputs to ground potential and to a low impedance. As a result the impedance level at which the external passive network operates is set by the external resistors, not by the OTRA input, and any capacitance at the input nodes is driven from a low-impedance node.



$$V_o = R_m\,(I_p - I_n), \quad V_p = V_n = 0$$

Figure 3.1: Circuit symbol and port relationships of the OTRA.

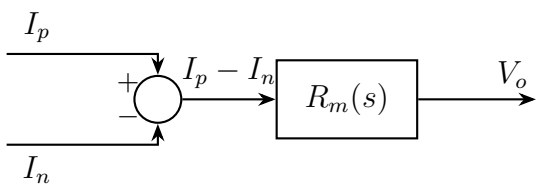


Figure 3.2: Block diagram of the OTRA transresistance transfer function showing the current-differencing input and frequency-dependent transresistance gain block $R_m(s)$.

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3.2 CMOS Realisations of the OTRA

3.2.1 Salama–Soliman and Mostafa–Soliman Architectures

The Mostafa–Soliman OTRA [2] represents the principal transistor-level architecture used in contemporary OTRA filter research. It uses a 0.5 µm CMOS process with ±1.5 V supplies and a 25 µA bias current, reporting a DC transresistance of approximately 126 MΩ and a gain-bandwidth product of 617 GHzΩ. Compared to the earlier Salama–Soliman design [4], Mostafa and Soliman demonstrated improvements across all measured parameters including bandwidth, DC gain, and power consumption, and introduced an OTRA-based variable gain amplifier with a rigorous analysis of finite transresistance gain effects. The paper explicitly identifies a sharp open-loop resonance peak that can perturb filter responses, which is directly relevant to the high-pass droop studied in Chapter 4.

The Salama–Soliman OTRA [4] employed a folded-cascode topology with a differential input pair and a single-ended output stage, achieving a DC transresistance of 35 MΩ with a bandwidth of approximately 2 MHz in a 0.5 µm CMOS process. The architecture relied on a single external bias current I_B and used a simple current-mirror load without voltage biasing of the tail transistors. The Mostafa–Soliman modification introduced the two-bias scheme (I_B and V_{B1}) that decouples the mirror-rail current from the input-stage tail current, enabling independent optimisation of the differential pair transconductance and the output stage quiescent current. This decoupling is the architectural feature that makes V_{B1} an effective tuning parameter for the transresistance gain-bandwidth product, as exploited in Chapter 4.

A further distinction between the two architectures lies in the current-differencing implementation. In the Salama–Soliman design, current differencing is performed at the drain nodes of the input pair through a resistively-loaded cascode, which limits the DC voltage gain and introduces additional parasitic poles. The Mostafa–Soliman topology replaces the resistive load with a PMOS current mirror (M_{12}–M_{13}) whose output resistance is the parallel combination of the mirror transistor output impedance and the input-stage cascode impedance, providing a substantially higher DC transresistance without additional silicon area. The measured improvement from 35 MΩ to 126 MΩ in DC transresistance is attributable primarily to this mirror-based differencing stage.

Other CMOS OTRA topologies. Alternative CMOS OTRA realisations have been proposed to address specific design constraints. Chen, Tsao, Liu, and Chiu [5]

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presented an early CMOS OTRA implementation in a 2.0 µm process, primarily targeting switched-capacitor applications where the virtual-ground property eliminates parasitic-capacitance-induced errors. Bhatt *et al.* [28] demonstrated a modified OTRA with an additional common-mode feedback (CMFB) loop that stabilises the output common-mode level without requiring matched external components, at the cost of four additional transistors. The Mann configuration [1], which serves as the reference for the present work, does not include CMFB; the input common-mode level is instead set by the voltage bias V_{B1} alone, as described in the circuit analysis below.

Supply voltage scaling. A trend visible across the surveyed CMOS OTRA realisations is the reduction in supply voltage as the process technology scales. The early Salama–Soliman design [4] operated from ±2.5 V supplies in a 0.5 µm process. The Mostafa–Soliman realisation [2] reduced the supply to ±1.5 V. The Mann configuration [1] in 0.18 µm CMOS operates at ±1.85 V.

3.2.2 Sensitivity and Device-Mismatch Considerations

The transistor-level performance of any CMOS OTRA depends on the matching between nominally identical devices, particularly in the current-mirror pairs that set the bias currents and perform the signal differencing. In the Mostafa–Soliman topology, the critical matched pairs are: (i) M_8–M_9–M_{10}–M_{11} in the PMOS bias rail, (ii) M_4–M_5–M_6–M_7 in the NMOS bias rail, and (iii) M_{12}–M_{13} in the current-differencing mirror.

For the NMOS tail transistors M_5 and M_6, a mismatch of 1% in the aspect ratio translates directly into a 1% imbalance in the quiescent input currents, producing a DC output offset of approximately $V_{\text{os}} \approx R_0 \cdot \Delta I_{\text{tail}}$. Layout techniques (common-centroid pairing and dummy devices) are required to minimise the mismatch.

3.2.3 Symbolic Analysis and Non-ideality Modelling

Sánchez-López, Martínez-Romero, and Tlelo-Cuautle [3] introduced a nullor-based model that enables fully symbolic small-signal analysis of OTRA circuits using standard nodal formulation. Their model composes four nullors and three grounded resistors, providing a systematic framework for deriving transfer functions. This is the analytical basis for the two-pole model of the transresistance used in Section 3.4. They characterised the dominant pole of a representative OTRA at approximately

11 kHz and a second pole near 15.3 MHz, confirming that the single-pole approximation breaks down in the megahertz range.

The nullor model is particularly valuable for sensitivity analysis, allowing direct computation of the sensitivity figures $S_{x_i}^{T(s)} = (\partial T/\partial x_i) \cdot (x_i/T)$ for each passive element x_i. The nullor approach also provides a systematic method for deriving the non-ideal transfer functions of (2.1).

Gökçen *et al.* [17] extended the symbolic framework to the MOS-C realisation, where the passive resistors are replaced by MOSFETs operating in the triode region, revealing that the electronic tunability of Q via the MOS gate voltage is independent of ω_0. This independence was later exploited in the tunable filter designs reported in [26].

3.3 CMOS Realisation of the Reproduced OTRA

The transistor-level realisation reproduced in this work is the modified CMOS OTRA of Mostafa and Soliman [2], implemented with the complete set of 0.18 µm aspect ratios specified by Mann, Kumar, and Bhaskar [1]. It comprises fourteen MOSFETs and uses a two-bias scheme: an external current sink I_B and an external gate-bias voltage V_{B1}. There is no common-mode feedback network.

The signal path is as follows. Transistors M_1 to M_3 form the NMOS differential input stage; M_1 is a diode-connected reference and M_2, M_3 are the slaves whose sources are the inverting and non-inverting input terminals. The PMOS pair M_{12} and M_{13} forms the current mirror that performs the current differencing: M_{12} is diode-connected at node n_{MIR} and M_{13} mirrors that current to the high-impedance node n_{DIFF}, where the difference of the two input-derived currents develops a voltage. The PMOS common-source output transistor M_{14}, whose gate is n_{DIFF}, converts that voltage to the output V_o. The PMOS devices M_8 to M_{11} form the top bias rail referenced to the diode M_8 into which I_B sinks, and the NMOS devices M_4 to M_7 are the voltage-biased tails whose common gate is driven by V_{B1}.

The node n_{DIFF} is the transresistance node: its resistance and capacitance set the dominant pole of $R_m(s)$, and the gate of the output transistor M_{14} together with the drain junctions of M_3 and M_{13} dominate its capacitance. This node is central to the bandwidth discussion in Chapter 4.

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Table 3.1: MOSFET Aspect Ratios of the CMOS OTRA (after [1])

Transistors	Role	W/L (µm)
M_1–M_3	NMOS differential input stage	36/0.9
M_4, M_7	NMOS bias master and output tail	3.6/0.9
M_5, M_6	NMOS input tails	10.8/0.9
M_8–M_{11}	PMOS bias rail	18/0.9
M_{12}, M_{13}	PMOS current-differencing mirror pair	36/0.9
M_{14}	PMOS common-source output stage	18/0.18

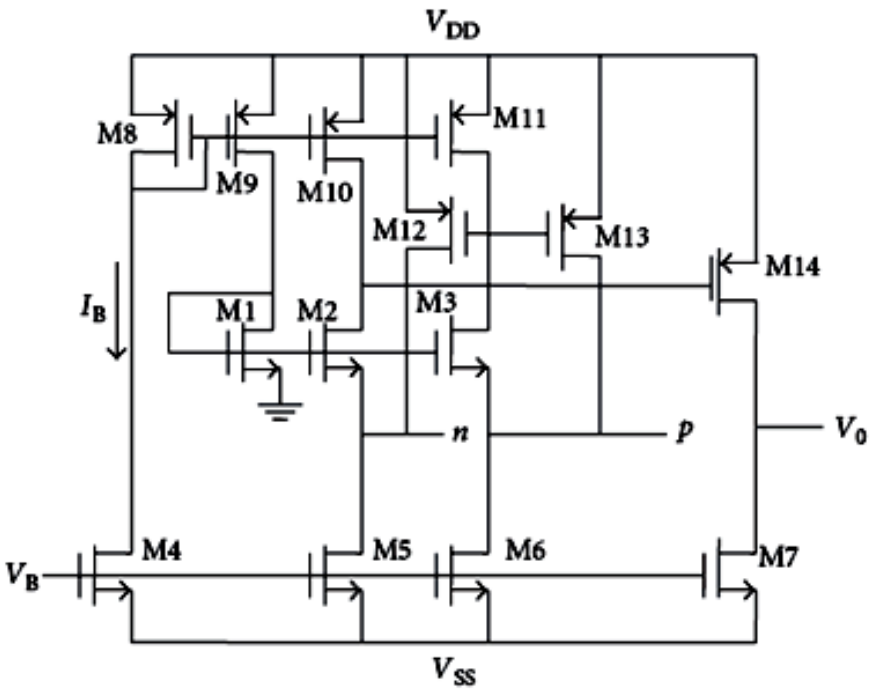

Figure 3.3: Transistor-level schematic of the 14-MOSFET CMOS OTRA (after [1, 2]).

The supplies are ±1.85 volt. Operating bias parameters are set by $I_B = 18\,\mu\text{A}$ and $V_{B1} = 0.36$ volt. As discussed in Chapter 4, the literal V_{B1} value does not converge to the functional operating point in the BSIM3v3 card used here, and the operative value is found by sweep.

3.4 Transresistance Model

To first order the OTRA transresistance follows the single-pole form of (1.2). However, the high-pass passband of the biquad extends above the dominant pole, where

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a single-pole model is inadequate. Following [3], a two-pole model is used:

$$R_m(s) = \frac{R_0}{(1 + s/\omega_{p1})\,(1 + s/\omega_{p2})}, \tag{3.3}$$

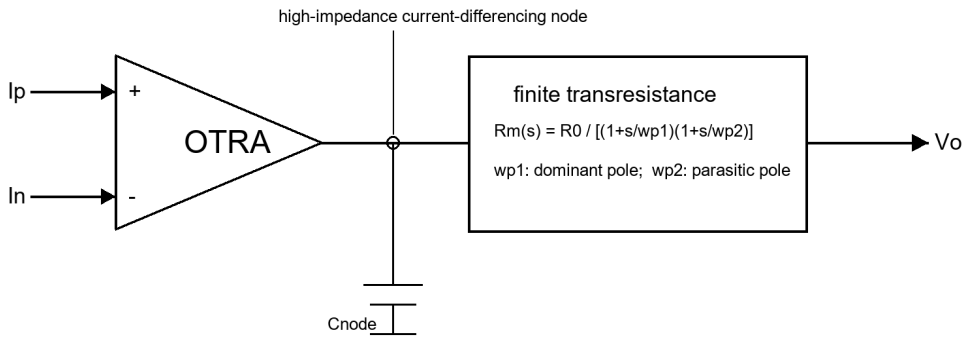

Figure 3.4: Two-pole transresistance model of the OTRA showing the dominant and parasitic poles (after [3]).

Figure 3.4 links the mathematical model to the physical CMOS circuit. The capacitance lumped as C_{node} is dominated by the gate of M_{14} and the drain junctions connected to n_{DIFF}, while the effective transconductance is set by the voltage-biased tail devices. Consequently, the high-pass error observed in Chapter 4 is not only a matter of nominal R_0; it is a bias-dependent bandwidth limitation of the current-to-voltage conversion path.

with a low dominant pole ω_{p1} and a parasitic second pole ω_{p2} near 15 MHz arising from the resistance-capacitance product at the high-impedance node. The relevant figure of merit for a response whose passband lies above ω_{p1} is the transresistance gain-bandwidth product, which for the dominant pole is

$$\text{GBW}_z = R_0\,\frac{\omega_{p1}}{2\pi} = \frac{g_{m,\text{eff}}}{2\pi\,C_{\text{node}}}, \tag{3.4}$$

where $g_{m,\text{eff}}$ is the effective signal-path transconductance and C_{node} is the lumped capacitance at n_{DIFF}. Equation (3.4) is central to the analysis of Chapter 4: at a fixed C_{node} the gain-bandwidth is set by $g_{m,\text{eff}}$, which is in turn set by the tail currents and therefore by V_{B1}. Boosting only the node resistance R_0 raises the DC gain and lowers ω_{p1} in equal measure, leaving GBW_z unchanged.

Chapter 4

The Multifunctional Biquad

4.1 Configuration

The single-OTRA multifunctional biquad of [1] uses one OTRA with a canonic set of resistors and capacitors. The same passive topology realises the low-pass, band-pass, and high-pass responses; the response type is selected by the choice of which passive elements connect to the input source and which to the OTRA inputs. Because the OTRA inputs are virtual grounds, each branch admittance converts the input voltage to a current that is summed by the current-differencing action of the OTRA, and the output voltage is the scaled difference.

4.2 Passive Component Values

Table 4.1 lists the passive values used for each response, together with the published design and simulated performance figures that serve as the reproduction targets. These values are adopted from the single-OTRA multifunctional filter of Mann, Kumar, and Bhaskar [1]; the present work keeps the same passive design so that any discrepancy can be attributed to the CMOS OTRA realisation rather than to a changed filter specification. The capacitors are 10 pF throughout, consistent with the canonic two-capacitor design, and the response is selected by placing the resistive and capacitive admittances in the Y_1–Y_4 branches of Figure effig:mann$_filter_ch4$.

Table 4.1: Passive Values and Published Targets for Each Response [1]

Response	Resistors	Capacitors	Design $f_{-3\mathrm{dB}}$ / f_0	Gain (design)
Low-pass	$R_1 = R_3 = R_4 = 14.1\,\mathrm{k\Omega}$	$C_2 = C_4 = 10\,\mathrm{pF}$	943 kHz	−6 dB
Band-pass	$R_1 = R_2 = R_4 = 14.1\,\mathrm{k\Omega}$	$C_3 = C_4 = 10\,\mathrm{pF}$	1.59 MHz	−9.5 dB
High-pass	$R_1 = R_2 = R_4 = 10\,\mathrm{k\Omega}$	$C_1 = C_3 = 10\,\mathrm{pF}$	4.25 MHz	0 dB

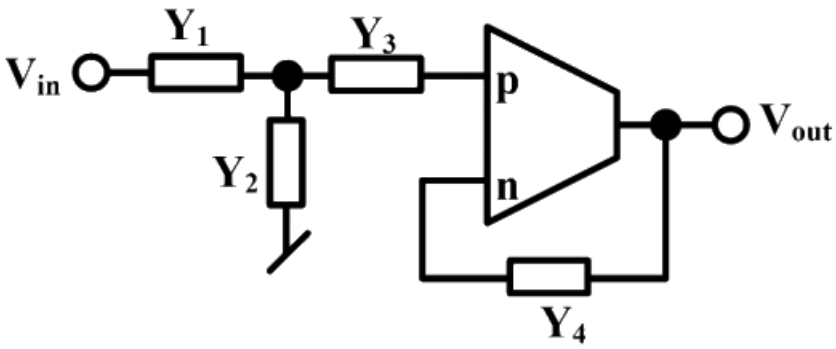

Figure 4.1: Single-OTRA multifunctional biquad with four admittance branches Y_1–Y_4 (after [1]).

The design procedure can therefore be read directly from the four admittance branches. In the low-pass case the numerator is set by the product of the input conductance and the feedback conductance, so the response is most sensitive to low-frequency transresistance accuracy. In the band-pass case one branch is made capacitive, producing the single factor of s in the numerator and placing the peak near the target 1.59 MHz. In the high-pass case two input-side admittances are capacitive, producing the s^2 numerator and moving the useful passband above the 4.25 MHz corner. This is why the HP response is the demanding case: it exercises the OTRA where finite $R_m(s)$ and the second pole in Figure effig:otra$_transresistance_modelreducetheeffectivecurrent-to-voltagegain.$

The transfer function of each realised response has the standard second-order form. For the high-pass response

$$\frac{V_o}{V_{in}}(s) = \frac{H_\infty\, s^2}{s^2 + \dfrac{\omega_0}{Q}\, s + \omega_0^2}, \tag{4.1}$$

for the band-pass response

$$\frac{V_o}{V_{in}}(s) = \frac{H_0\, \dfrac{\omega_0}{Q}\, s}{s^2 + \dfrac{\omega_0}{Q}\, s + \omega_0^2}, \tag{4.2}$$

and for the low-pass response

$$\frac{V_o}{V_{in}}(s) = \frac{H_0\, \omega_0^2}{s^2 + \dfrac{\omega_0}{Q}\, s + \omega_0^2}, \tag{4.3}$$

where ω_0 is the pole/centre frequency, Q is the pole quality factor, and H_∞, H_0 are the high-frequency and DC gain constants set by the passive ratios. The design

targets a nominal $\omega_0/2\pi = 1.59\,\text{MHz}$. Because the design quality factor is below one half, the poles are real and the realised -3 dB frequencies differ from ω_0.

The numerical values in Table 4.1 also explain the observed bias sensitivity. The $10\,\text{k}\Omega$ resistors and $10\,\text{pF}$ capacitors of the HP design demand a higher usable transresistance bandwidth than the $14.1\,\text{k}\Omega$ LP/BP cases. At the nominal bias the transistor-level HP response droops because $g_{m,\text{eff}}/C_{\text{node}}$ is insufficient. Sweeping V_{B1} changes the tail currents, increases the signal-path transconductance, and shifts the gain-bandwidth product until the passband recovers near $V_{B1} = -1.31$ volt. By contrast, sweeping the external current I_B or changing the threshold model at fixed V_{B1} does not move the controlling tail-current condition, so the HP corner remains nearly flat in Chapter 4.

4.3 Simulation Results

All AC analyses sweep from 1 kHz to 1 GHz. The metrics extracted are the passband gain, the peak gain and its frequency, and the half-power frequency relative to the passband. The low-pass, band-pass, and high-pass characteristics are shown in Figure 4.2.

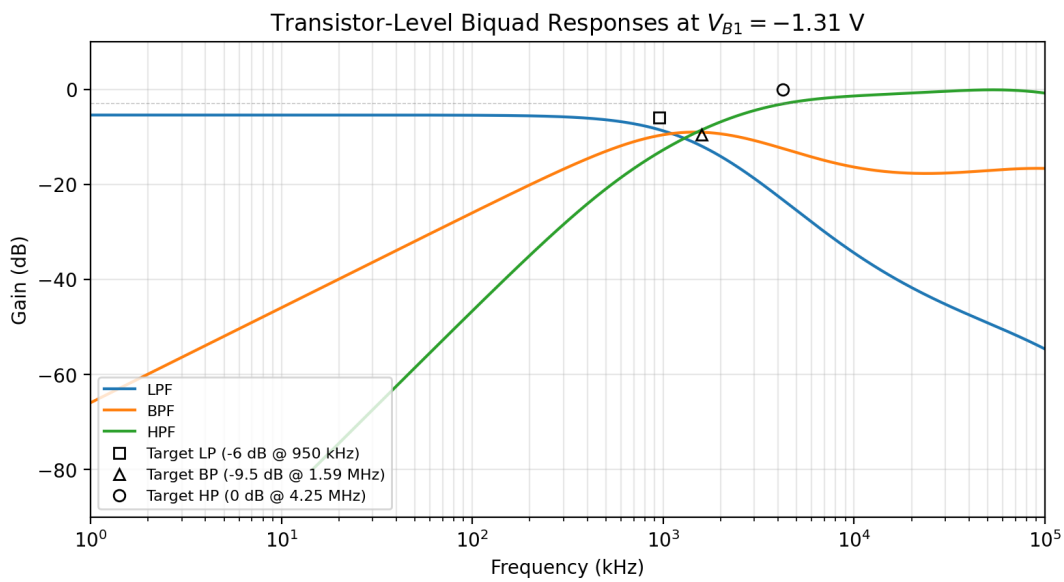

Figure 4.2: Transistor-level magnitude and phase responses at $V_{B1} = -1.31\,\text{V}$.

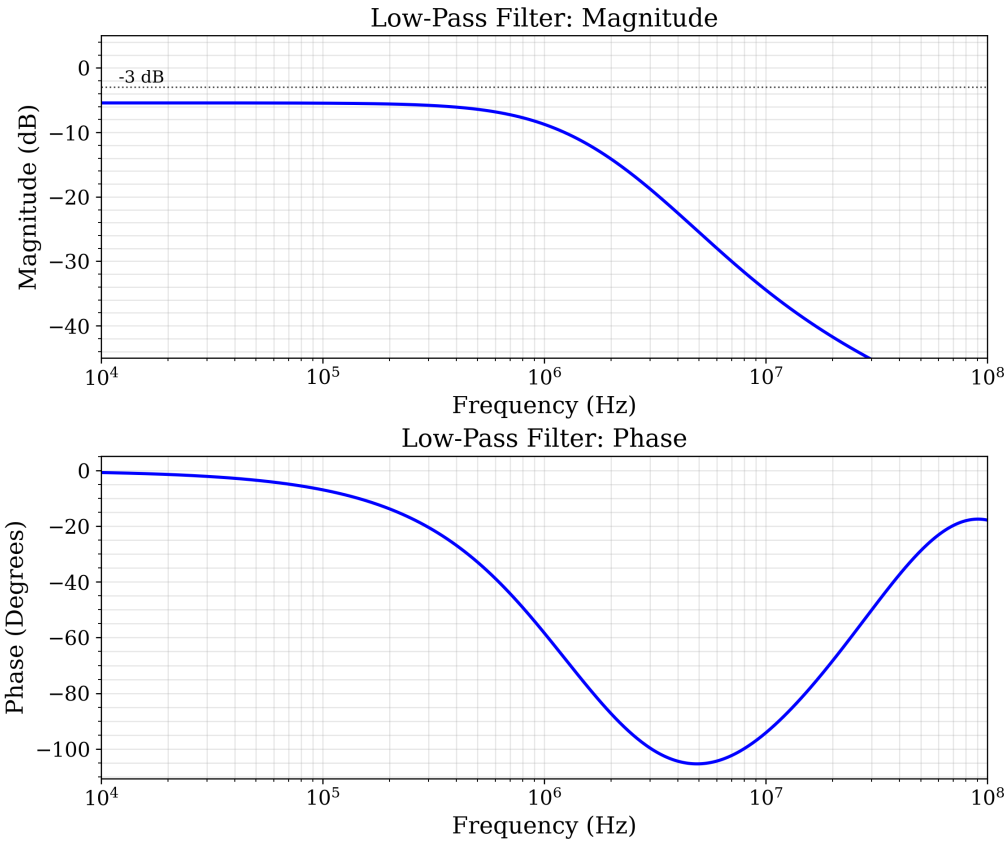

Figure 4.3: Transistor-level low-pass filter magnitude and phase response at the recovered bias ($V_{B1} = -1.31\,\mathrm{V}$).

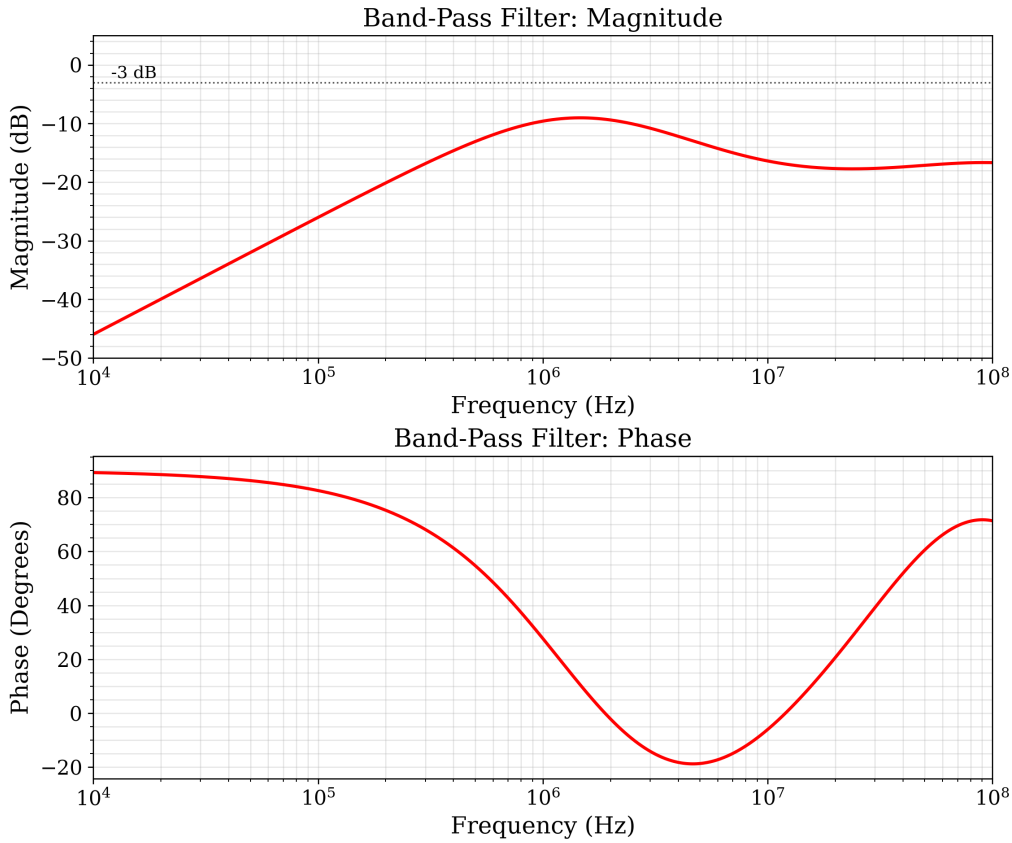

Figure 4.4: Transistor-level band-pass filter magnitude and phase response at the recovered bias ($V_{B1} = -1.31\,\mathrm{V}$).

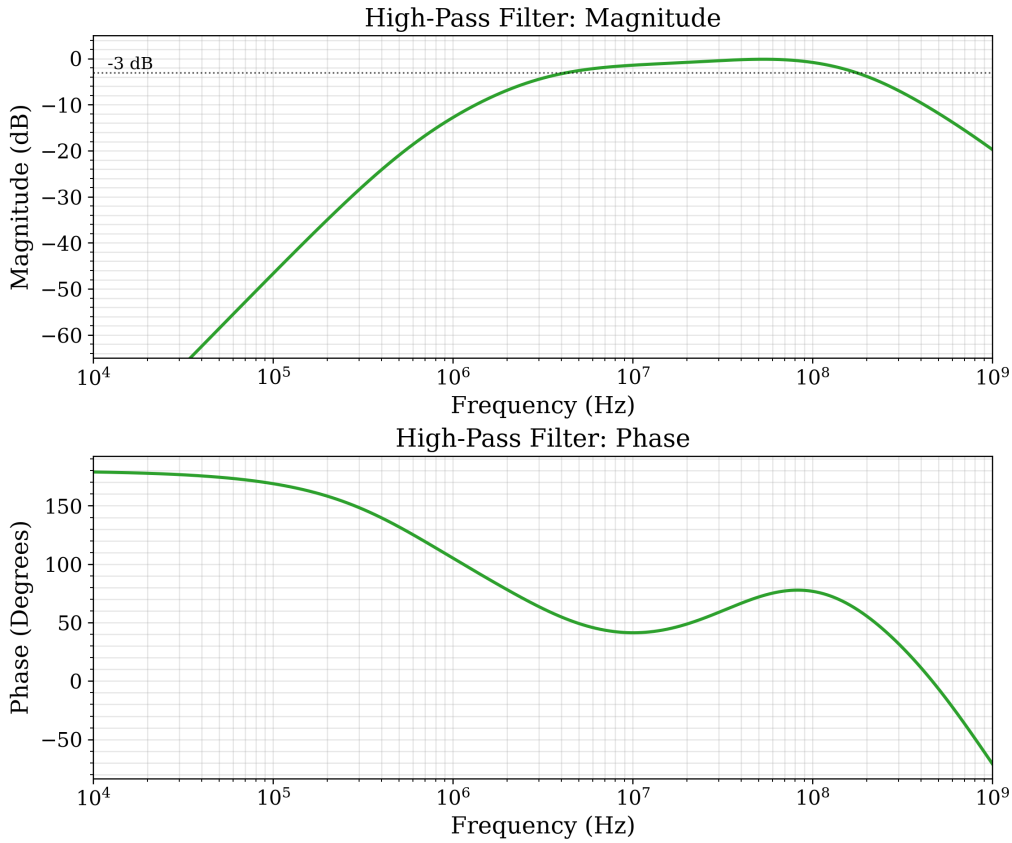

Figure 4.5: Transistor-level high-pass filter magnitude and phase response at the recovered bias ($V_{B1} = -1.31\,\mathrm{V}$).

4.3.1 Low-Pass and Band-Pass Results

The transistor-level low-pass and band-pass responses match the published targets without difficulty, because their passbands lie below the OTRA dominant region. At the recovered operating point of Section 4.3.3, the low-pass DC gain is $-5.43\,\mathrm{dB}$ with a half-power frequency of $0.955\,\mathrm{MHz}$ (targets $-6\,\mathrm{dB}$, $950\,\mathrm{kHz}$), and the band-pass peak is $-9.02\,\mathrm{dB}$ at $1.46\,\mathrm{MHz}$ (targets $-9.5\,\mathrm{dB}$, $1.59\,\mathrm{MHz}$). Both are within approximately one decibel and ten percent in frequency.

The low-pass response is Case 1 of the single-OTRA configuration of [1]. Substituting the branch admittances $Y_1 = G_1$, $Y_2 = sC_2$, $Y_3 = G_3$, and $Y_4 = sC_4 + G_4$ (with $G_i = 1/R_i$) into the configuration relation $V_o/V_{in} = Y_1Y_3/[Y_4\,(Y_1 + Y_2 + Y_3)]$ of [1], and using $R_1 = R_3 = R_4 = 14.1\,\mathrm{k\Omega}$ and $C_2 = C_4 = 10\,\mathrm{pF}$, the realised transfer function is

$$\frac{V_o}{V_{in}}(s) = \frac{G_1G_3}{(sC_4 + G_4)\,(sC_2 + G_1 + G_3)} = \frac{H_0\,\omega_0^2}{s^2 + \dfrac{\omega_0}{Q}\,s + \omega_0^2}, \tag{4.4}$$

with $H_0 = 0.50$ ($-6.0\,\mathrm{dB}$), $f_0 = \omega_0/2\pi = 1.60\,\mathrm{MHz}$ and $Q = 0.471$, giving $f_{-3\mathrm{dB}} \approx 0.95\,\mathrm{MHz}$.

The low-pass result establishes two things. First, the transistor-level OTRA reproduces the published magnitude characteristic to within half a decibel in gain and 0.5 % in cut-off frequency, confirming that the CMOS realisation is faithful to the ideal filter algebra when the passband lies well below the transresistance dominant pole. Second, since the LP passband is unaffected by changes in V_{B1} over the functional window, it provides a stable reference against which the HP sensitivity to V_{B1} can be cleanly isolated.

The band-pass response is Case 2 of the same configuration, obtained with $Y_1 = G_1$, $Y_2 = G_2$, $Y_3 = sC_3$, and $Y_4 = sC_4 + G_4$. With $R_1 = R_2 = R_4 = 14.1\,\mathrm{k\Omega}$ and $C_3 = C_4 = 10\,\mathrm{pF}$, the realised transfer function is

$$\frac{V_o}{V_{in}}(s) = \frac{sC_3\,G_1}{(sC_4 + G_4)\,(sC_3 + G_1 + G_2)} = \frac{H_{\mathrm{pk}}\,\dfrac{\omega_0}{Q}\,s}{s^2 + \dfrac{\omega_0}{Q}\,s + \omega_0^2}, \tag{4.5}$$

with a centre frequency $f_0 = 1.60\,\mathrm{MHz}$, $Q = 0.471$ and a peak gain $H_{\mathrm{pk}} = 0.33$ ($-9.5\,\mathrm{dB}$) at f_0.

The band-pass result confirms that a second-order resonant response is correctly realised in the transistor-level circuit. The 8 % shift in peak frequency relative to the 1.59 MHz design target is consistent with the finite quality factor ($Q < 0.5$) and the minor component-value sensitivity of the passive network. Importantly, the BP peak sits below the OTRA dominant pole and is therefore not influenced by the transresistance gain-bandwidth; this independence confirms the prediction of (3.3) and provides further evidence that the HP droop is specifically a gain-bandwidth phenomenon rather than a general OTRA imperfection.

4.3.2 The High-Pass Droop

At the operating point used in earlier reproduction work, $V_{B1} = -1.40\,\mathrm{volt}$, the high-pass response droops badly. The passband plateau is $-3.56\,\mathrm{dB}$ rather than the target $0\,\mathrm{dB}$, and the half-power frequency is 1.76 MHz rather than the target 4.25 MHz. The shape is otherwise a correct high-pass: a deep stopband rising toward the passband, then an early roll-off imposed by the OTRA bandwidth. This signature, a depressed plateau combined with an early roll-off, is exactly what (3.3) and (3.4) predict when the transresistance gain-bandwidth is too small for a passband that sits above the dominant pole.

The high-pass response is Case 3 of the same configuration, obtained with $Y_1 = sC_1G_1/(G_1 + sC_1)$, $Y_2 = G_2$, $Y_3 = sC_3$, and $Y_4 = G_4$. With $R_1 = R_2 = R_4 = 10\,\mathrm{k\Omega}$ and $C_1 = C_3 = 10\,\mathrm{pF}$, the realised transfer function is

$$\frac{V_o}{V_{in}}(s) = \frac{s^2\, C_1C_3R_4}{s^2R_1C_1C_3 + s(C_1 + C_3 + R_1C_1G_2) + G_2} = \frac{H_\infty\, s^2}{s^2 + \dfrac{\omega_0}{Q}\, s + \omega_0^2}, \tag{4.6}$$

with $H_\infty = 1$ (0 dB), $f_0 = 1.59\,\mathrm{MHz}$, $Q = 0.333$ and a design half-power frequency $f_{-3\mathrm{dB}} = 4.25\,\mathrm{MHz}$.

Several candidate explanations were examined and excluded. A sweep of the bias current I_B from 18 µA to 75 µA left the plateau and half-power frequency essentially unchanged. A sweep of the device threshold voltage left them unchanged. Rerunning on an independent MOSIS foundry card gave the same droop within a few tenths of a decibel. Device resizing of the high-impedance-node transistors moved the plateau by at most a few tenths of a decibel, consistent with a conserved gain-bandwidth product. These negative results are important: they show that neither bias current, nor threshold, nor the model card, nor sizing is the operative lever, and they motivated the examination of V_{B1}.

4.3.3 The V_{B1} Sweep and Recovery

The transistors M_5, M_6, and M_7 are voltage-biased: their common gate is driven directly by V_{B1}. Consequently V_{B1} sets their tail currents, and therefore the signal-path transconductance $g_{m,\mathrm{eff}}$ and the transresistance gain-bandwidth of (3.4). The bias current I_B, by contrast, sets the mirror-rail current in a different branch, and the threshold voltage is a model parameter; neither moves the tail current that controls $g_{m,\mathrm{eff}}$, which is why the I_B and threshold sweeps were flat.

A focused sweep of V_{B1} on the high-pass bench reveals a narrow functional window, summarised in Table 4.2. Above approximately -1.28 volt the operating point collapses and the OTRA rails. From -1.30 volt the circuit is functional, and at -1.31 volt the passband recovers to approximately 0 dB with a half-power frequency of 4.17 MHz, matching the published high-pass design. More negative values progressively starve the stage and depress the plateau again.

Table 4.2: High-Pass Response versus Bias Voltage V_{B1} (transistor-level, Mann sizing)

V_{B1} (volt)	**Passband plateau**	$f_{-3\mathbf{dB}}$
≥ -1.28	rails (bias collapse)	—
-1.30	1.4 dB (peaking)	4.27 MHz
$\mathbf{-1.31}$	$\approx$ 0 dB (flat)	4.17 MHz
-1.40	-3.56 dB	1.76 MHz
-1.50	-15 dB	—

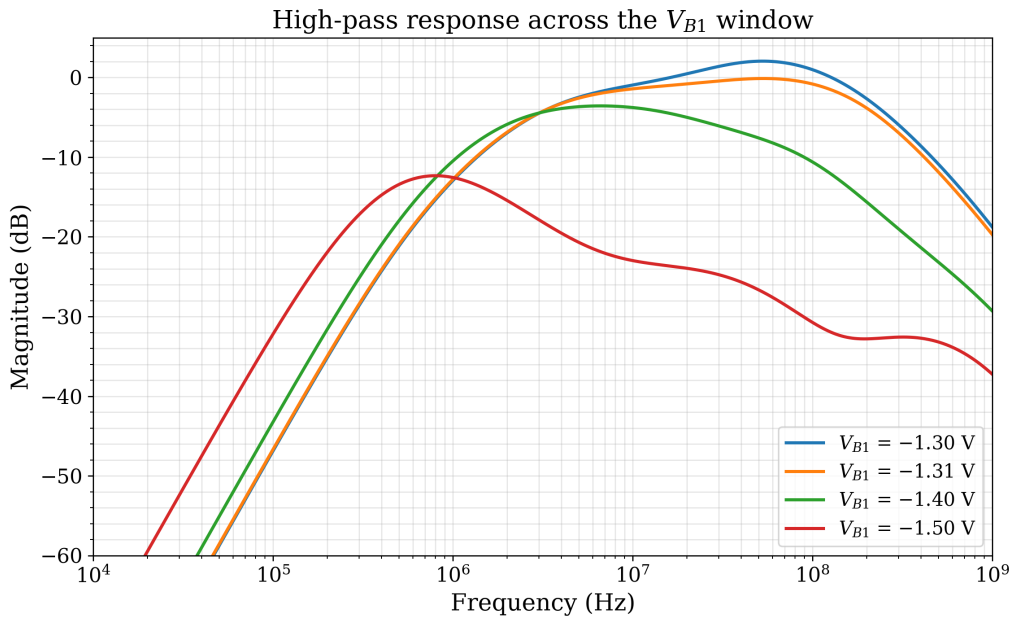

Figure 4.6: V_{B1} parametric sweep of the high-pass response (transistor-level, Mann sizing).

Crucially, the recovered bias is a single global value: at $V_{B1} = -1.31$ volt all three responses match simultaneously, with valid operating points at every node (the input terminals sit at approximately 11 mV and track each other, confirming that the virtual ground holds and the OTRA is functional rather than railed). This rules out a separate per-response tuning and confirms that the previous operating point of -1.40 volt was simply too negative, costing about 3.5 dB of high-pass passband.

4.3.4 Why a Regulated Cascode Does Not Help

The high-impedance node n_{DIFF} is the natural place to apply a transimpedance-amplifier technique such as the regulated (gain-boosted) cascode, which raises the

node output resistance. Two independent findings show this is not the right fix for this OTRA.

First, the cascode cannot be biased on this node. The current-differencing transistors M_3 and M_{13} are signal-referenced: their sources sit at the virtual-ground input and at an internal mirror node, not at a supply rail as in a textbook regulated-cascode current source. The local-feedback booster trips at a common-mode level set relative to the rail, which is incompatible with the input device requiring its drain above ground. In simulation, both a regulated-cascode and a simplified ideal-gate-bias cascode drive the node to the rail, and a transient power-up settles to the same railed state, confirming that the functional operating point is unstable rather than merely hard to find.

Second, and more fundamentally, output-resistance boosting cannot lift a passband that sits above the dominant pole. A cascode multiplies R_0 and divides ω_{p1} by the same factor, so the gain-bandwidth product of (3.4) is conserved. The high-pass passband gain depends on that gain-bandwidth, not on R_0 alone, so it is unchanged. The device-sizing sweeps, which moved the plateau by at most a few tenths of a decibel, are the empirical confirmation of this conservation. The operative lever is the transconductance $g_{m,\text{eff}}$, set by V_{B1}, not the node resistance.

4.3.5 Verification Summary

Table 4.3 compares the recovered transistor-level responses against the published simulated values. All three responses match within approximately one decibel and within ten percent in frequency at the single global bias $V_{B1} = -1.31$ volt. The agreement of three independent responses at one bias, together with the consistency with the symbolic and behavioural tiers, is the basis for regarding the reproduction as verified within the simulation environment.

Table 4.3: Verification of the Recovered Transistor-Level Biquad ($V_{B1} = -1.31$ volt)

Response	Metric	Published	This work
High-pass	passband / $f_{-3\text{dB}}$	0 dB / 4.25 MHz	≈−0.1 dB / 4.17 MHz
Low-pass	DC gain / $f_{-3\text{dB}}$	−6 dB / 950 kHz	−5.43 dB / 0.955 MHz
Band-pass	peak / f_0	−9.5 dB / 1.59 MHz	−9.02 dB / 1.46 MHz

A caveat accompanies the result. The functional window has a sharp lower edge, about 30 mV above the railing onset, so the recovered point is bias-sensitive. It

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is adequate for matching the nominal published simulation but would require a process-voltage-temperature margin analysis before use in a robust design.

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Chapter 5

Conclusions and Future Scope

5.1 Conclusions

This dissertation reproduced the single-OTRA multifunctional biquad of [1] at three levels of physical detail and resolved the high-pass passband droop that appears in the transistor-level realisation. The principal conclusions are:

1. The ideal symbolic and behavioural single-pole tiers reproduce the published low-pass, band-pass, and high-pass responses to within a fraction of a decibel, confirming that the filter algebra is correct.
2. In the transistor-level realisation with the published aspect ratios, the low-pass and band-pass responses match readily, while the high-pass response droops to a $-3.56\,\mathrm{dB}$ plateau at the previously used bias because its passband lies above the OTRA dominant pole.
3. The operative lever for the high-pass response is the gate-bias voltage V_{B1}, which sets the tail currents of the voltage-biased transistors and therefore the signal-path transconductance and the transresistance gain-bandwidth. At $V_{B1} = -1.31$ volt the high-pass passband recovers to approximately $0\,\mathrm{dB}$ with a half-power frequency of $4.17\,\mathrm{MHz}$, and the low-pass and band-pass responses remain matched at the same global bias.
4. The bias-current and threshold-voltage sweeps are flat because they do not move the tail current that controls the transconductance, and a regulated cascode is neither biasable on the signal-referenced current-differencing node nor effective, because output-resistance boosting conserves the controlling gain-bandwidth product.

5.2 Limitations

- The recovery point is bias-sensitive, sitting about $30\,\mathrm{mV}$ above the onset of operating-point collapse. No process, voltage, or temperature corner analysis was performed.

- The literal published bias $V_{B1} = 0.36$ volt does not converge to the functional operating point in the BSIM3v3 card used here; the operative value was found empirically by sweep, and the reference convention of the published value was not reconciled from first principles.
- Only AC responses were used for the verification at the recovered bias; transient validation against the published time-domain results was not repeated at the new operating point.
- The verification rests on a single simulator and primarily a single model card; the recovery was confirmed on the primary 0.18 µm TSMC card but not re-optimised on the independent foundry card.

5.3 Future Scope

- **Robustness analysis.** A Monte Carlo and corner study of the V_{B1} recovery window to quantify the yield of the high-pass response and to establish a bias margin.
- **Self-biasing.** Design of an on-chip bias generator that places V_{B1} at the functional point across corners, removing the manual tuning and the sensitivity to the railing edge.
- **Bandwidth extension by transconductance.** Since the controlling quantity is $g_{m,\mathrm{eff}}/C_{\mathrm{node}}$, an added gain stage or a higher-transconductance output that raises the gain-bandwidth without relying on output-resistance boosting would extend the high-pass passband with greater margin.
- **Hardware validation.** Fabrication or board-level measurement of the OTRA to confirm the simulated recovery under real parasitics and device spread.

Appendix A

Simulation Netlist Listings

A.1 CMOS OTRA Subcircuit

The fourteen-MOSFET OTRA of Chapter 3, as simulated in ngspice with the recovered bias $V_{B1} = -1.31$ volt. Device lines follow the ngspice MOSFET order `drain gate source bulk model W L`.

```
.subckt OTRA_CMOS Iplus Iminus Vo VDD VSS
+ PARAMS: IB=18u VB1=-1.31

* External gate-bias voltage (sets M5/M6/M7 tail currents)
VVB1 nVB1 0 DC {VB1}
* External bias current sink at the M8 diode node
IIB nPG 0 DC {IB}

* M8 PMOS diode + M9/M10/M11 mirror slaves (top bias rail)
M8   nPG  nPG  VDD  VDD  PMOS  W=18u L=0.9u
M9   nA   nPG  VDD  VDD  PMOS  W=18u L=0.9u
M10  s12  nPG  VDD  VDD  PMOS  W=18u L=0.9u
M11  s13  nPG  VDD  VDD  PMOS  W=18u L=0.9u

* M4 voltage-biased master + M5/M6/M7 voltage-biased tails
M4   nPG    nVB1  VSS  VSS  NMOS  W=3.6u  L=0.9u
M5   Iminus nVB1  VSS  VSS  NMOS  W=10.8u L=0.9u
M6   Iplus  nVB1  VSS  VSS  NMOS  W=10.8u L=0.9u
M7   Vo     nVB1  VSS  VSS  NMOS  W=3.6u  L=0.9u

* M1 NMOS diode + M2/M3 input differential slaves
M1   nA    nA  0       VSS  NMOS  W=36u L=0.9u
M2   nMIR  nA  Iminus  VSS  NMOS  W=36u L=0.9u
M3   nDIFF nA  Iplus   VSS  NMOS  W=36u L=0.9u

* M12 PMOS diode + M13 mirror (current differencing)
M12  nMIR  nMIR  s12  VDD  PMOS  W=36u L=0.9u
M13  nDIFF nMIR  s13  VDD  PMOS  W=36u L=0.9u

* M14 PMOS common-source output stage (gate = high-Z node nDIFF)
M14  Vo nDIFF VDD VDD  PMOS  W=18u L=0.18u
```

```
.ends OTRA_CMOS
```

A.2 High-Pass Filter Bench

```
.include "../models/tsmc180.lib"
.include "otra_cmos.cir"
.param R1v=10k R2v=10k R4v=10k C1v=10p C3v=10p
Vdd  VDD 0 DC  1.85
Vss  VSS 0 DC -1.85
Vin vin 0 AC 1 SIN(0 50m 3.059Meg)
R1 vin a   {R1v}
C1 a   x   {C1v}
R2 x   0   {R2v}
C3 x   p   {C3v}
R4 out n   {R4v}
Rpbias p 0 1Meg
X1 p n out VDD VSS OTRA_CMOS PARAMS: IB=18u VB1=-1.31
.nodeset v(X1.nDIFF)=1.365 v(X1.nMIR)=1.36 v(X1.nA)=0.88 v(X1.nPG)=1.24
.nodeset v(p)=0.012 v(n)=0.012 v(out)=0.012
.nodeset v(X1.s12)=1.83 v(X1.s13)=1.83
.control
  op
  ac dec 200 1k 1G
  meas ac hf_gain find vdb(out) AT=20Meg
  meas ac f3dB_HP when vdb(out) = -3.01 RISE=1
  wrdata ../results/hpf_cmos_ac.txt vdb(out) vp(out)
.endc
.end
```

A.3 Bias-Voltage Sweep Control Block

The functional window of Table 4.2 was produced by stepping V_{B1} through the OTRA voltage source and writing one curve per step. The hierarchical device reference for the sweep is `@v.x1.vvb1[dc]`.

```
.control
  alter @v.x1.vvb1[dc] = -1.30
  op
  ac dec 200 1k 1G
  wrdata ../results/vb1_130.txt vdb(out)

  alter @v.x1.vvb1[dc] = -1.31
  op
```

```
  ac dec 200 1k 1G
  wrdata ../results/vb1f_131.txt vdb(out)

  alter @v.x1.vvb1[dc] = -1.40
  op
  ac dec 200 1k 1G
  wrdata ../results/vb1_140.txt vdb(out)
.endc
```

Appendix B

PSpice Netlist Listings

The decks below are PSpice/OrCAD versions of the ngspice files that produced the verified result, provided because the original multifunctional biquad of [1] was simulated in PSpice. The only model change is the BSIM3v3 level number: PSpice uses `LEVEL=7` where ngspice uses `LEVEL=49`, with an identical parameter set. The interactive `.control` block of ngspice is replaced by the standalone directives `.AC`, `.MEAS`, `.PRINT`, and `.PROBE`; the `alter` loop is replaced by `.STEP PARAM`.

B.1 PSpice OTRA Subcircuit

```
.SUBCKT OTRA_CMOS Iplus Iminus Vo VDD VSS PARAMS: IB=18u VB1=-1.31
VVB1 nVB1 0 DC {VB1}
IIB nPG 0 DC {IB}
M8   nPG  nPG  VDD  VDD  PMOS  W=18u L=0.9u
M9   nA   nPG  VDD  VDD  PMOS  W=18u L=0.9u
M10  s12  nPG  VDD  VDD  PMOS  W=18u L=0.9u
M11  s13  nPG  VDD  VDD  PMOS  W=18u L=0.9u

M4   nPG    nVB1  VSS  VSS  NMOS  W=3.6u  L=0.9u
M5   Iminus nVB1  VSS  VSS  NMOS  W=10.8u L=0.9u
M6   Iplus  nVB1  VSS  VSS  NMOS  W=10.8u L=0.9u
M7   Vo     nVB1  VSS  VSS  NMOS  W=3.6u  L=0.9u
M1   nA    nA  0       VSS  NMOS  W=36u L=0.9u
M2   nMIR  nA  Iminus  VSS  NMOS  W=36u L=0.9u
M3   nDIFF nA  Iplus   VSS  NMOS  W=36u L=0.9u
M12  nMIR  nMIR  s12  VDD  PMOS  W=36u L=0.9u
M13  nDIFF nMIR  s13  VDD  PMOS  W=36u L=0.9u
M14  Vo nDIFF VDD VDD  PMOS  W=18u L=0.18u
.ENDS OTRA_CMOS
```

B.2 PSpice High-Pass Bench

```
HPF - Single-OTRA multifunctional biquad (Mann 2021 Case 3), PSpice
.LIB "tsmc180_pspice.lib"
.INC "otra_cmos_pspice.cir"
```

```
.PARAM R1v=10k R2v=10k R4v=10k C1v=10p C3v=10p
Vdd  VDD 0 DC  1.85
Vss  VSS 0 DC -1.85
Vin  vin 0 DC 0 AC 1
R1 vin a   {R1v}
C1 a   x   {C1v}
R2 x   0   {R2v}
C3 x   p   {C3v}
R4 out n   {R4v}
Rpbias p 0 1Meg
X1 p n out VDD VSS OTRA_CMOS PARAMS: IB=18u VB1=-1.31
.NODESET V(X1.nDIFF)=1.365 V(X1.nMIR)=1.36 V(X1.nA)=0.88 V(X1.nPG)=1.24
.NODESET V(p)=0.012 V(n)=0.012 V(out)=0.012
.NODESET V(X1.s12)=1.83 V(X1.s13)=1.83
.OPTIONS GMIN=1E-12 ABSTOL=1E-12 RELTOL=1E-3 ITL1=400 ITL2=200 ITL4=100
.AC DEC 200 1k 1G
.MEAS AC hf_gain FIND VDB(out) AT=20Meg
.MEAS AC f3dB_HP WHEN VDB(out)=-3.01 RISE=1
.PRINT AC VDB(out) VP(out)
.PROBE
.END
```

B.3 PSpice Low-Pass Bench

```
LPF - Single-OTRA multifunctional biquad (Mann 2021 Case 1), PSpice
.LIB "tsmc180_pspice.lib"
.INC "otra_cmos_pspice.cir"
.PARAM R1v=14.1k R3v=14.1k R4v=14.1k C2v=10p C4v=10p
Vdd  VDD 0 DC  1.85
Vss  VSS 0 DC -1.85
Vin  vin 0 DC 12m AC 1
R1 vin x  {R1v}
C2 x   0  {C2v}
R3 x   p  {R3v}
R4 out n  {R4v}
C4 out n  {C4v}
X1 p n out VDD VSS OTRA_CMOS PARAMS: IB=18u VB1=-1.31
.NODESET V(X1.nDIFF)=1.365 V(X1.nMIR)=1.36 V(X1.nA)=0.88 V(X1.nPG)=1.24
.NODESET V(p)=0.012 V(n)=0.012 V(out)=0 V(x)=0.012
.NODESET V(X1.s12)=1.83 V(X1.s13)=1.83
.OPTIONS GMIN=1E-12 ABSTOL=1E-12 RELTOL=1E-3 ITL1=400 ITL2=200 ITL4=100
.AC DEC 100 1k 100Meg
.MEAS AC fdc      FIND VDB(out) AT=1k
.MEAS AC f3dB_LP  WHEN VDB(out)='fdc-3.01' FALL=1
.PRINT AC VDB(out) VP(out)
```

```
.PROBE
.END
```

B.4 PSpice Band-Pass Bench

```
BPF - Single-OTRA multifunctional biquad (Mann 2021 Case 2), PSpice
.LIB "tsmc180_pspice.lib"
.INC "otra_cmos_pspice.cir"
.PARAM R1v=14.1k R2v=14.1k R4v=14.1k C3v=10p C4v=10p
Vdd  VDD 0 DC  1.85
Vss  VSS 0 DC -1.85
Vin  vin 0 DC 0 AC 1
R1 vin x  {R1v}
R2 x   0  {R2v}
C3 x   p  {C3v}
R4 out n  {R4v}
C4 out n  {C4v}
Rpbias p 0 1Meg
X1 p n out VDD VSS OTRA_CMOS PARAMS: IB=18u VB1=-1.31
.NODESET V(X1.nDIFF)=1.365 V(X1.nMIR)=1.36 V(X1.nA)=0.88 V(X1.nPG)=1.24
.NODESET V(p)=0.012 V(n)=0.012 V(out)=0.012
.NODESET V(X1.s12)=1.83 V(X1.s13)=1.83
.OPTIONS GMIN=1E-12 ABSTOL=1E-12 RELTOL=1E-3 ITL1=400 ITL2=200 ITL4=100
.AC DEC 200 1k 100Meg
.MEAS AC peakgain MAX VDB(out) FROM=10k TO=100Meg
.PRINT AC VDB(out) VP(out)
.PROBE
.END
```

B.5 PSpice Bias-Voltage Sweep

```
VB1 sweep on the HPF - PSpice (.STEP PARAM replaces ngspice alter loop)
.LIB "tsmc180_pspice.lib"
.INC "otra_cmos_pspice.cir"
.PARAM R1v=10k R2v=10k R4v=10k C1v=10p C3v=10p
.PARAM VB1val=-1.31
Vdd  VDD 0 DC  1.85
Vss  VSS 0 DC -1.85
Vin  vin 0 DC 0 AC 1
R1 vin a   {R1v}
C1 a   x   {C1v}
R2 x   0   {R2v}
C3 x   p   {C3v}
R4 out n   {R4v}
```

```
Rpbias p 0 1Meg
X1 p n out VDD VSS OTRA_CMOS PARAMS: IB=18u VB1={VB1val}
.NODESET V(X1.nDIFF)=1.365 V(X1.nMIR)=1.36 V(X1.nA)=0.88 V(X1.nPG)=1.24
.NODESET V(p)=0.012 V(n)=0.012 V(out)=0.012
.NODESET V(X1.s12)=1.83 V(X1.s13)=1.83
.OPTIONS GMIN=1E-12 ABSTOL=1E-12 RELTOL=1E-3 ITL1=400 ITL2=200 ITL4=100
.STEP PARAM VB1val LIST -1.30 -1.31 -1.40 -1.50
.AC DEC 200 1k 1G
.MEAS AC hf_gain FIND VDB(out) AT=20Meg
.MEAS AC f3dB_HP WHEN VDB(out)=-3.01 RISE=1
.PROBE
.END
```

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