TCAD-BASED MAGNETIC ANALYSIS OF 2D-MagFinFET IN ORTHOGONAL DIRECTIONS FOR MEDICAL MICRO-ROBOTS APPLICATION

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I, **Aman**, hereby certify that the work which is being presented in the thesis entitled **"TCAD-BASED MAGNETIC ANALYSIS OF 2D-MagFinFET IN ORTHOGONAL DIRECTIONS FOR MEDICAL MICRO-ROBOTS APPLICATION"** in partial fulfillment of the requirements for the award of the Degree of Master of Science, submitted in the Department of Applied Physics, Delhi Technological University is an authentic record of my own work carried out during the period from August 2025 to May 2026 under the supervision of **Prof. Rishu Chaujar**.

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Certified that **Aman (24/MSCPHY/03)** has carried out the research work presented in this thesis entitled **"TCAD-BASED MAGNETIC ANALYSIS OF 2D-MagFinFET IN ORTHOGONAL DIRECTIONS FOR MEDICAL MICRO-ROBOTS APPLICATION"** for the award of Master of Science from the Department of Applied Physics, Delhi Technological University, Delhi, under my supervision.

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ABSTRACT

The need for magnetic sensor is aggressively increasing in medical area to navigate the medical micro-robots through the blood vessels to target. This dissertation presents a detailed TCAD based investigation of novel Two Directional Magnetic Fin Field Effect Transistor (2D-MagFinFET) magnetic sensor based on the advanced 3D architecture of Field Effect Transistor. The proposed device is designed to overcome the limitation of traditional magnetic sensor to only sense the single direction magnetic field. The proposed device is designed to sense orthogonal magnetic field in Y and Z direction. It is operated on concept of Lorentz force act on charge carrier in channel when external magnetic field applied which deflect the carrier from their path which governs differential current (ΔI_D). Device uses two parallel fins to sense the magnetic field. One fin will detect the magnetic field of Y-direction and other one of Z-direction without any coupling of relative sensitivity. Two layers of SiO_2/HfO_2 as gate dielectric is used to enhance the overall performance of the proposed device. The performance of the proposed device is analyzed in terms of SS, V_{TH}, I_{ON}, I_{OFF}, *DIBL, SR,* magnetic sensitivity (S_A) and Relative magnetic sensitivity (S_R).

The proposed device demonstrates a SS of 59.96 mV/dec which is improved by 4.83% in contrast to existing devices. The V_{TH} of device is increased from 0.21 V to 0.48 V by 128.57% which help to protect the sensor to turn on accidently. I_{OFF} and I_{ON} currents of the proposed device is 5.24 fA and 12.9 μA having *SR* of 2.39×10^9. The proposed device has a DIBL of 8.24 mV/V at gate length of 50 nm show how efficiently device overcome the problem of short channel effect. These results demonstrate the better switching and performance of proposed device than the existing device. The magnetic response shows the linear dependency of differential current (ΔI_Y and ΔI_Z) with Magnetic field having a sensitivity of 159.27 nA/T in Y-direction and 147.13 nA/T in Z-direction at 100 μA biased current. The relative sensitivity is 0.00159 T^{-1} and 0.00147 T^{-1} in Y and Z direction respectively, improved from recently reported device. Owing the magnetic sensitivity in orthogonal direction the proposed device is suitable for the spatial tracking and navigation of medical micro-robots.

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ABBREVIATIONS

2D-MagFinFET	Two Directional Magnetic Fin Field Effect Transistor
AMR	Anisotropic Magnetoresistance
BEOL	Back-End-Of-Line
BJT	Bipolar Junction Transistor
BOX	Buried Oxide
CMOS	Complementary Metal-Oxide-Semiconductor
DIBL	Drain-Induced Barrier Lowering
FinFET	Fin Field-Effect Transistor
GMR	Giant Magnetoresistance
HKMG	High-k Metal Gate
JFET	Junction Field-Effect Transistor
MAGFET	Magnetic Field Effect Transistor
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS/ PMOS	n-channel/ p-channel MOSFET
SCE	Short Channel Effect
SDE	Sentaurus Structure Editor
SNR	Signal-to-Noise Ratio
SOI	Silicon-on-Insulator
SRH	Shockley-Read-Hall
SS	Subthreshold Swing
STI	Shallow Trench Isolation
SWB	Sentaurus Workbench
TCAD	Technology Computer Aided Design
UTB-SOI	Ultra-Thin Body Silicon-on-Insulator

NOMENCLATURE

B	External Magnetic Field
B_Y / B_Z	Magnetic Field in Y/Z-direction
C_{OX}	Gate Capacitance
D_1, D_2, D_3, D_4	Drain Contacts
g_d	Output Conductance
g_m	Transconductance
G_H	Geometrical Correction Factor
H_{fin}	Fin Height
I_D/ I_{DS}	Biased Drain current / Drain Current
I_{OFF} / I_{ON}	OFF-state Leakage Current / ON-state Drive Current
L_G	Lateral Gate Length
N_A, N_D	Doping Concentration
S_A	Absolute Magnetic Sensitivity
S_R	Relative Magnetic Sensitivity
SR	Switching Ratio
T_{OX}	Oxide Thickness
V_{DD}	Supply Voltage
V_{DS}	Drain-to-Source Voltage
V_{GS}	Gate-to-Source Voltage
V_{TH}	Threshold Voltage
W_{eff}	Effective Channel Width
W_{fin}	Fin Width
μ_{ch}	Carrier Mobility
ΔI_D	Differential Drain Current

CHAPTER 1

INTRODUCTION AND EVOLUTION OF SEMICONDUCTOR

1.1. Introduction

Over two thousand years ago, ancient civilizations specially the Greeks and the Chinese discovered naturally magnetized pieces of the mineral magnetite. They noticed that these stones could magically attract iron, but they didn't initially use them for direction. But the actual invention which help the ancient era was the invention of using magnets to find direction belongs to ancient China during the Han Dynasty (around 200 BCE to 200 CE). They crafted the first compass, known as the **"south-pointing spoon" (Sinan)**. It was made from a carved piece of lodestone shaped like a ladle, which was placed on a smooth bronze plate. When the spoon was allowed to settle, its handle would always mysteriously point south. Initially, this was used for geomancy and fortune-telling (Feng Shui) rather than oceanic navigation.

It took centuries for humanity to actually understand *why* the compass needle moved. In 1600, an English scientist named William Gilbert published a book called *De Magnete*, where he proposed a brilliant idea: **The Earth itself is a giant magnet.**

Here is the physics of how it works:

- **The Earth's Core:** Deep inside the Earth, a churning ocean of molten liquid iron generates massive electrical currents. These currents create a global magnetic field that wraps around the entire planet.
- **Magnetic Poles:** This global field has two main focal points: the Magnetic North Pole and the Magnetic South Pole.
- **Alignment:** A fundamental rule of magnetism is that opposite poles attract. A compass is simply a tiny, lightweight magnet balanced on a nearly frictionless pivot. Because it is free to rotate, the "North-seeking" end of the compass needle is pulled by the Earth's magnetic field until it aligns perfectly with the magnetic lines traveling between the Earth's poles.

So, when you hold a compass, you are essentially holding a tiny sensor that detects the invisible magnetic forces generated thousands of miles beneath your feet.

However, for macroscopic world navigation is quite simple because the forces of nature are predictable. But when we shrink down to micro-scale, the laws of classical physics collapse, rendering localized orientation tracking immensely difficult. But why? we are moving towards the micro-scale. Is this really so essential? The answer is yes. The human vascular system is of the size of microscale we have to go through the micro and nano-scale during the surgery in modern era. So, the navigation at that scale is quite important for us.

To get around such limitations, modern solid-state electronics needs to compress the old mechanics of the compass into a quantum confined silicon architecture, replacing the physical rotating needle with a dynamic stream of mobile electrons. This electronic deflection leads to an asymmetric current distribution which is essentially governed by the Hall effect and the formation of a localized Hall current. An orthogonal magnetic field laterally drives electrons in the silicon channel to the fin sidewalls, leading to the generation of an internal transverse electric field, the Hall field, to counteract the Lorentz force. Under some biasing conditions in current mode operation, this local

field causes a transverse drift current to flow in the channel. Thus, the charge density is dynamically modified by the Hall current

1.2. Evolution of Semiconductor Devices

The first invention of the vacuum diode by British physicist John Ambrose Fleming in 1904 marked the beginning of the semiconductor era. In 1906, American engineer Lee de Forest invented the vacuum transistor, enabling electronic tubes to perform amplification and oscillation. This groundbreaking development marked the beginning of the modern electronics industry.

On December 6, 1947, William Shockley, John Bardeen, and Walter Brattain developed the world's first germanium point-contact transistor at Bell Laboratories in Murray Hill. This breakthrough is considered one of the most significant inventions in modern history, as it enabled electronic devices such as radios, calculators, and computers to become smaller, more efficient, and cost-effective, while also laying the foundation for the development of integrated circuits.

In April 1950, Shockley introduced the first bipolar junction transistor (BJT), commonly known as the PN junction transistor. Even today, most transistors continue to operate based on the PN junction principle.

In 1952, the junction field-effect transistor (JFET) was successfully developed[1]. Later, in 1959, Mohamed Atalla and his team invented the Metal-Oxide-Semiconductor (MOS) structure.

In 1963, Frank Wanlass and Chih-Tang Sah proposed the first CMOS (Complementary Metal-Oxide-Semiconductor) technology, in which n-MOS and p-MOS devices were combined into a complementary configuration. This CMOS structure had almost no static power during operation and was suitable for logic circuits. CMOS technology provides several advantages such as low power consumption, high integration density and simple fabrication. It has become the dominant technology for the manufacture of integrated circuits since the 1970s and 1980s, and accounts for more than 95% of the global semiconductor integrated circuit industry today.

A comprehensive timeline illustrating this historical evolution, beginning from early vacuum tube technology and progressing toward modern nanoscale FinFET architectures, is presented in Figure 1.1[2].

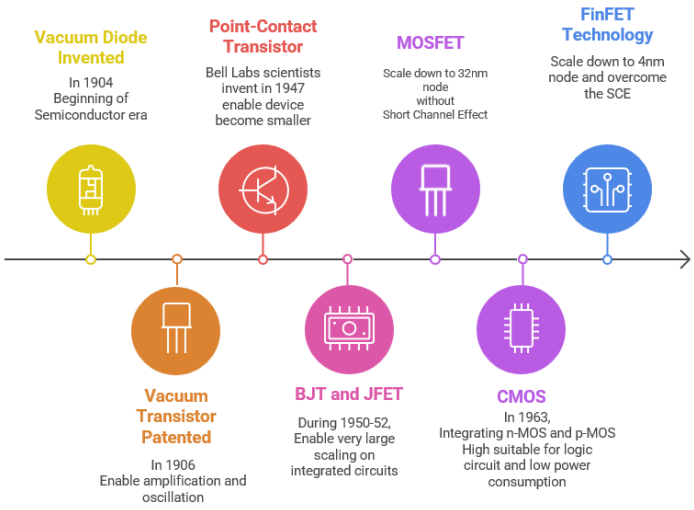


Figure 1.1. Evolution of Semiconductor Devices

1.3. Moore's law

When it comes to semiconductors, one of the first things most people think of is Moore's Law. This seminal engineering and economic forecast that guided the development of the digital era for more than half a century is intimately tied to the development of modern solid-state electronics. In 1965 Gordon Moore proposed what became known as Moore's Law: the number and complexity of components that could be integrated onto a single silicon chip would increase by about a factor of two every eighteen to twenty-four months, while the cost of manufacturing remained much the same, and computational performance would rise correspondingly[3]. For many decades, this prediction was confirmed by the steady improvement of complementary metal-oxide-semiconductor (CMOS) technology that steadily shrank planar transistor dimensions. This incredible progress was mainly driven by Dennard Scaling which indicated that when the lateral gate length of a planar transistor was scaled down, the operating voltage and the oxide thickness could be scaled down proportionally. This scaling allowed higher switching speeds, lower power

consumption and better device performance while keeping the power density across the silicon chip nearly constant. The prediction has been confirmed by the steady and predictable shrinkage of the physical dimensions of planar devices through the gradual evolution of complementary metal-oxide-semiconductor (CMOS) technology over the last few decades. All this rapid progress was based on the so-called Dennard scaling. The Dennard scaling was based on the assumption that the lateral gate length of a planar transistor can be scaled down, while the operating voltage and the oxide thickness can be scaled down proportionally. With the Dennard scaling, engineers can achieve faster switching speeds and lower power consumption while keeping the total power density of the silicon chip.

6.4.1. Limitations of Moore's law

But as lithographic features scaled down into the deep nanometer regime, the physical foundations of Moore's Law hit a fundamental barrier called the power wall. Conventional 2D planar CMOS architectures have approached the limit of downscaling below the 32 nm limit because the operating voltage could not be decreased further without degrading the device speed. This stagnation resulted in severe short channel effects, especially drain induced barrier lowering and severe subthreshold swing degradation, which allowed the horizontal drain field to dominate over the vertical gate field[4]. When turned off, transistors started leaking huge amounts of passive current, turning idle power dissipation into an impossible thermodynamic crisis threatening to bring to a halt the historical trajectory of Moore's Law. The physical scaling limits that ultimately resulted in the breakdown of the classical parameter matrix are caused directly by the severe short channel effects (SCEs) and DIBL. The structural geometry of a planar MOSFET varies drastically when the lateral gate length (L_G) is scaled beyond 32 nm.

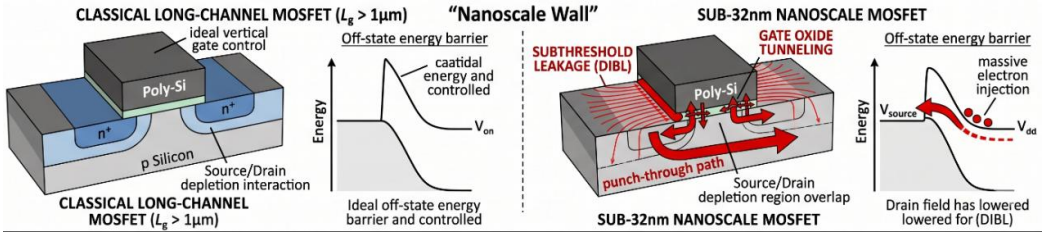
6.4.2. Short Channel Effect (SCE)

Short-Channel Effects (SCEs) are the fundamental physical limit where aggressive transistor downscaling starts to compromise normal electronic operation. In a conventional long-channel MOSFET, the gate electrode exerts a strong electrostatic

control on the channel, where the vertical electric field is the dominant driving force for carrier transport and the effect of the horizontal drain field is negligible[5]. However, as the dimensions of the device shrunk below the 32 nm regime in order to follow the trend of Moore's Law, the distance between the source and drain regions became very small. This reduction allowed the drain horizontal electric field to penetrate deep into the channel and directly compete with the gate field to control the channel potential. As a result, the gate control is degraded, with a degradation of the subthreshold swing, carrier velocity saturation and leakage through punch-through conduction paths, even when the transistor is in an OFF state.

The gate electrode can exert strong one-dimensional vertical control of the channel carriers in a conventional long-channel MOSFET (LG > 1μm) because the source and drain depletion regions are well separated. The long-channel energy band diagram shows that a high and sharply defined potential barrier at the source junction can effectively block electron flow, achieving a clean off-state with negligible leakage.

Whereas, aggressive scaling of the transistor below the 32nm regime leads to the overlap of the source and drain depletion regions significantly, with the reduced channel length. This structural encroachment provides a subsurface punch through leakage path that bypasses the electrostatic control of the gate. In addition, the extreme thinning of the gate oxide required to maintain surface modulation of the channel results in the formation of very high vertical electric fields which may induce quantum mechanical tunnelling of electrons through the dielectric. This tunnelling effect



(a) (b)

Figure 1.2. Comparison of Classical Long-Channel and Sub-32 nm Nanoscale MOSFETs Highlighting Short-Channel Effects (a) Long Channel MOSFET (L_G>1μm) and (b) Sub-32 nm Nanoscale MOSFET

produces a continuous leakage in the off-state with a significant impact on the device's standby power and overall reliability. Figure 1.2 presents a comparative energy band analysis highlighting the degradation of the off-state energy barrier and the emergence of subthreshold leakage pathways in sub-32 nm device architectures.

6.4.3. Drain-Induced Barrier Lowering (DIBL)

The main problem with this geometrical evolution is the DIBL, which changes the energy band profile of the device in a fundamental way. In a classical long-channel transistor in the off-state (V_{GS} = 0 V) a strong electrostatic barrier at the source–channel junction prevents electron flow. However, in a short-channel planar device with high drain bias (V_{DS}), the horizontal electric field spans the shortened channel length and effectively lowers the source injection barrier. Such a reduction enables the thermionic injection of majority carriers from the source into the channel even at V_{GS} = 0V. Thus, DIBL causes a large increase in the subthreshold leakage current (I_{OFF}) and makes the V_{TH} highly unstable, decreasing unpredictably as the drain voltage increases. This can lead to serious logic errors in high density integrated circuits and thus degrade the reliability and performance of the device.
The shrinkage of lateral dimensions of a sub 32 nm nanoscale MOSFET directly Favors DIBL since the lateral drain electric field can penetrate deep into the source side depletion region. In a conventional long channel device the electrostatic energy barrier at the source junction is still high, and is dominated almost entirely by the vertical gate bias with little influence from the drain voltage over the channel[4]. However, a high drain bias (V_{DD}), as shown in the nanoscale energy band profile, penetrates into the shortened channel and lowers the local conduction band edge, thus reducing the source injection barrier. This potential distortion causes an undesired electron injection from the source directly into the inversion region of the channel. As a consequence, the strong coupling between the drain field and the channel causes a

large increase of the I_{OFF} and an unstable V_{TH} which decreases continuously with the increasing drain bias, eventually leading to a degradation of the reliability of the transistor as a switching device.

6.4.4. Degradation of Subthreshold Swing (SS)

At the same time, the short-channel electrostatics impose a tight physical constraint on the SS of the transistor, which dictates the required V_{GS} to change the drain current by one order of magnitude during switching transitions. In a classical long-channel device the gate capacitance (C_{OX}) is perfectly coupled to the channel body and this allows the device to turn off sharply around the basic thermionic limit of 60 mV/dec at room temperature. In a scaled short-channel geometry, however, this capacitive coupling is severely compromised by the parasitic voltage divider formed by the depletion capacitance, which steals potential from the gate electrode. This capacitive degradation pushes the subthreshold swing way beyond its optimum threshold, leaving the device in a sluggish semi-conductive state. The SS degradation, subsurface punch-through where the source and drain depletion regions physically merge to form an uncontrolled conduction path, and direct gate-oxide quantum mechanical tunnelling combine to create an unmanageable power wall that prevents conventional 2D planar CMOS configurations from being scaled down any further[6].

The degradation of the SS is also further accelerated by the horizontal field mechanics of DIBL. With DIBL, the drain field in the horizontal direction can go deep into the channel and reduce the barrier for source injection, which means the gate electrode has no longer unique control over the off-state current profile. With the increase of V_{DS}, it behaves like a second gate terminal and injects a large part of drain-induced thermionic carriers into the channel inversion layer. This parasitic current injection reduces the subthreshold current-voltage (I_{DS}-V_{GS}) slope, driving the subthreshold swing well beyond the ideal 60 mV/dec limit. This illustrates the direct degradation of the subthreshold swing by DIBL and how the planar architecture is trapped into a high leakage, energy inefficient operating regime, and thus the transistor cannot switch sharply between on and off states at high drain biases.

1.4. Ultra-Thin Body Silicon-on-insulator

The Ultra-Thin Body Silicon-on-Insulator (UTB-SOI) architecture successfully extended the semiconductor scaling roadmap by inserting a thick insulating buried oxide (BOX) layer deep in the substrate that physically isolates an ultra-thin layer of top silicon to serve as the active channel[7]. This semiconductor body is fabricated to be ultra-thin so that it is fully depleted of mobile charge carriers at zero gate bias and there is no physical space below the gate for the development of subterranean punch-through leakage currents. This structural confinement requires all traveling electrons to be located directly at the interface of the gate dielectric, which dramatically reduces parasitic drain field penetration and maintains strong vertical electrostatic control without the need for heavy, mobility degrading channel doping.

By neutralizing the primary subsurface leakage pathways inherent to bulk silicon, UTB-SOI allowed the industry to scale planar devices down into the deep nanometer regime while maintaining an acceptable current switching ratio. The cross-sectional structure of the UTB-SOI architecture, emphasizing the ultra-thin active silicon body and the BOX) layer, is illustrated in Figure 1.3[8].

However, as feature sizes approached the sub-20 nanometer regime, this single-gate planar geometry reached severe physical, manufacturing, and thermodynamic

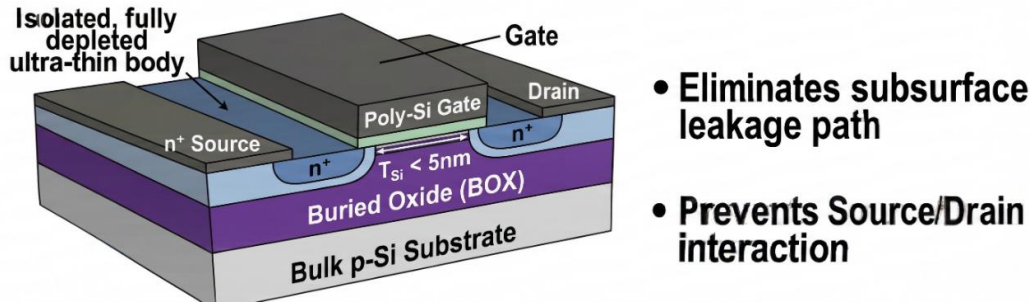


Figure 1.3. Ultra-Thin Body Silicon-On-Insulator Structure

limitations. To maintain electrostatic command at ultra-short gate lengths, the silicon body thickness had to be thinned down to a few atomic layers, introducing extreme

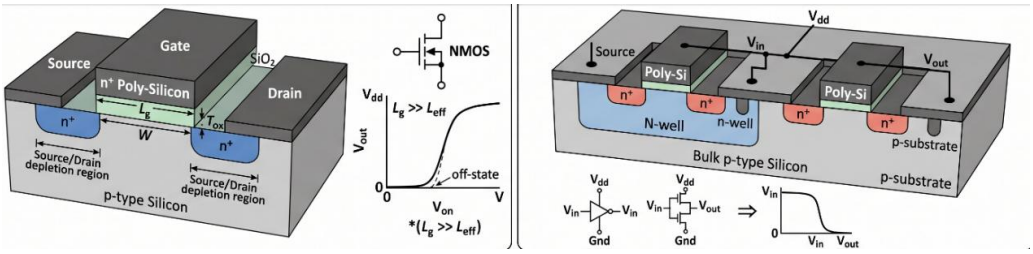
process variations where even a single-atom fluctuation caused massive shifts in the threshold voltage and triggered quantum- size effects that heavily degraded carrier mobility. Furthermore, because the underlying dioxide layer acts as a severe thermal bottleneck, the heat generated by carrier transport became trapped within the channel, causing localized self-heating that reduced the on-state drive current. Simultaneously, high electric field lines from the drain began to completely bypass the thin channel, penetrating deep through the underlying buried oxide to couple back into the source junction from beneath, completely compromising the off-state leakage control of the device and forcing the transition to three-dimensional multi-gate geometries like the FinFET.

1.5. Complementary metal-oxide-semiconductor (CMOS)

The fundamental building block of modern solid-state microelectronics is the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), a four-terminal voltage-controlled device that regulates carrier transport through a semiconductor channel using an applied electric field. Structurally, a conventional bulk MOSFET consists of a semiconductor substrate, heavily doped source and drain regions, and a heavily doped gate electrode that controls current flow. The gate is electrically isolated from the substrate by an ultra-thin dielectric layer, traditionally silicon dioxide (SiO_2). MOSFETs are mainly classified into two complementary categories based on the dominant carriers forming the inversion layer during conduction: n-channel MOSFETs (NMOS) and p-channel MOSFETs (PMOS). In NMOS devices, a positive V_{GS} attracts electrons and forms an n-type inversion layer within a p-type substrate, whereas PMOS devices use a negative V_{GS} to accumulate holes at the surface of an n-type substrate[9].

To improve computational efficiency and minimize static power dissipation, the semiconductor industry integrated these complementary device types into Complementary Metal-Oxide-Semiconductor (CMOS) technology. In a conventional planar CMOS structure, NMOS and PMOS transistors are fabricated side-by-side on a common silicon substrate using localized oppositely doped regions called wells. For example, in a standard p-type substrate, the NMOS device is directly formed in the

substrate, while the PMOS device is fabricated inside an engineered n-type well (N-well) to ensure electrical isolation. Additional isolation between neighbouring devices is achieved using Shallow Trench Isolation (STI) structures filled with SiO_2. *In a typical CMOS inverter configuration, the gate terminals of both NMOS and PMOS are connected to a common input voltage* V_{IN} while their drains are connected together to produce the output voltage (V_{OUT}). Since one transistor remains OFF while the other operates in the ON state, the CMOS structure effectively eliminates a direct current path between the supply voltage (V_{DD}) and ground (Gnd), thereby reducing power consumption mainly to switching operations. The structural configurations and basic circuit schematics of a conventional bulk MOSFET and a standard planar CMOS inverter are illustrated in Figure 1.4[10].



(a) (b)

Figure 1.4. (a) Bulk MOS Transistor (MOSFET) and Schematic and (b) Planar CMOS Structure

During the highly successful scaling era governed by Moore's Law and Dennard Scaling, the geometric dimensions of planar CMOS devices were continuously reduced to enhance performance. Before the limitations of planar scaling became significant, important device parameters were systematically scaled by a factor of approximately ($\kappa = 0.7$) with each new technology generation. The lateral gate length (LG) which is the length between the source and drain regions was reduced to shorten the carrier transit time and to increase the switching speed. To maintain strong electrostatic control over the shortened channel, the silicon dioxide gate oxide (T_{OX})

thickness was also scaled down proportionally. Meanwhile, the V_{DD} was also scaled down to maintain the internal electric fields stable[11]. The channel doping concentration (N_A or N_D) was increased to avoid merging of source and drain depletion

TABLE 1.1. Planar CMOS Scaling Parameter Matrix (Dennard Scaling Era)[12]

Scaling Parameter	Symbol	Classical Scaling Factor	Impact on Pre-Failure CMOS Performance
Gate Length	L_G	1/ κ	Reduced by 30% per generation, enabling a 40% increase in the intrinsic switching speed.
Channel Width	W	1/ κ	Reduced for optimum packing density and minimum total active gate area footprint.
Gate Oxide Thickness	T_{OX}	1/ κ	Proportionally thinned to keep high gate C_{OX} and strong vertical charge control.
Supply Voltage	V_{DD}	1/ κ	Scaled to exponentially reduce dynamic power consumption proportional to $(V_{DD})^{2.}$
Channel Doping Density	N_{SUB}	κ	Increased by 40% to avoid undesirable parasitic depletion layer growth into the short channel.
Parasitic Capacitance	C_G	1/ κ	Decreased per transistor, reducing the total charge required to switch states.
Power Density	P/A	1	Remained completely constant (invariant), preventing thermal runaway during historical scaling cycles.

regions. This method of coordinated scaling resulted in optimized SS, effective suppression of DIBL and improved high ON-state drive current (I_{ON}) with I_{OFF}. As a result, the present switching ratio (ION/IOFF) remained extremely efficient for

decades until the device dimensions approached the nanoscale regime, where planar structures began to suffer significant short-channel electrostatic limitations. Table 1.1 summarizes the rules of the game for the historical optimization era of the device performance as well as the corresponding impacts of parameter variations[12].

1.6. Fin Field-Effect Transistor (FinFET)

The invention of the Fin Field-Effect Transistor (FinFET) marked a significant shift from traditional two-dimensional planar technology to novel three-dimensional multi-gate architectures and enabled the semiconductor industry to circumvent the critical thermal and electrostatic limits of planar scaling. As the miniaturization of traditional devices progressed to the point where the gate electrode could no longer effectively control the inversion channel, researchers re-designed the geometry of the silicon channel itself. The FinFET structure is a device where the conducting channel is lifted vertically from the substrate to form an ultra-thin fin and the gate electrode surrounds the fin from multiple sides, thus restoring the strong electrostatic control over the carrier transport in the device. This major architectural breakthrough enabled technology scaling below the 22 nm node, delivering higher I_{ON}, significantly lower static power, and further performance improvements consistent with Moore's Law[13].

1.6.1. Architecture of 3D FinFETs

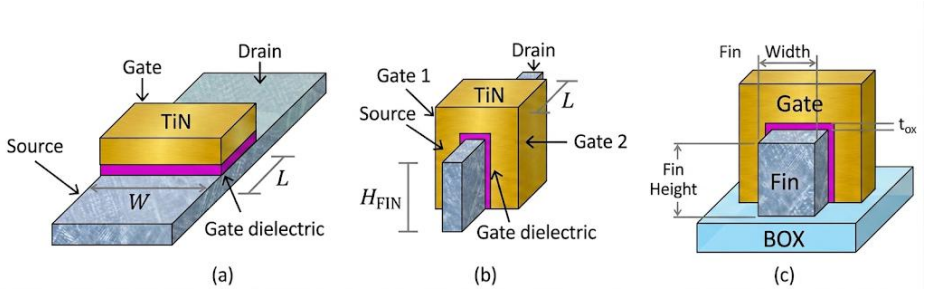


Figure 1.5. Structure Schematic (a) planar MOSFET and (b) FinFET and (c) Demonstrating H_{fin} as fin height and W_{fin} as fin width

The architectural advantage of the FinFET lies in the accurate geometry of its active area, turning the electrostatic landscape from a single-plane interface into a multi-axial control volume. Structurally, the core of the device is an ultra-thin monocrystalline silicon fin of height H_{fin} and physical width W_{fin}, etched perpendicularly from the underlying substrate. The gate electrode conformally wraps around this vertical pillar to create a tri-gate architecture where three different physical facets contribute to the carrier transport[14]. This 3-D structural configuration allows an intense performance boost for the complementary logic circuits, which allows deep device scaling without an increase of the horizontal layout footprint on the chip. Figure 1.5. The transition from conventional planar MOSFET to multi-gate FinFET architecture and the main geometric parameters such as H_{fin} and W_{fin}.

1.6.2. Electrostatic Quantization and Effective Channel Width Formulas

The multi-gate configuration mathematically modifies the basic equations for the effective channel width W_{eff} and capacitive coupling of the transistor. The channel width of a conventional planar device is a fixed layout dimension constrained to the horizontal plane. In a single-fin tri-gate FinFET, the gate simultaneously controls the charge carriers from the vertical sidewalls as well as the horizontal top surface, and hence the total conducting perimeter is given by the following geometrical relation[13]:

$$W_{eff} = 2.H_{fin} + W_{fin} \tag{1.1}$$

In advanced sub-14nm nodes, a dielectric hard mask is often deliberately left on top of the silicon fin prior to gate deposition. This additional isolation layer prevents the penetration of the vertical field from the top part of the electrode, resulting in a true double-gate FinFET device with conduction along the vertical sidewalls, and changing the effective width formula to:

$$W_{eff} = 2\,H_{fin} \tag{1.2}$$

This allows a larger I_{ON} for heavy capacitive loads, without increasing the lateral gate length. To scale the architecture horizontally, several parallel fins are placed under a single, continuous gate electrode. The total effective width for a multi-fin structure with N identical fins is given by[13]:

$$W_{eff} = N(2 H_{fin} + W_{fin}) \quad (1.3)$$

This discretized quantized scaling mechanism requires the use of complex Technology Computer Aided Design (TCAD) tools to optimize the fin pitch (the physical distance between the neighbouring fins) and to prevent local parasitic capacitance from impeding the high frequency performance of the integrated circuit.

1.6.3. Choice of Channel Material and Advanced Gate Stack Integration

The core channel material still remains predominantly monocrystalline silicon, because of its excellent mechanical stability, high quality native oxide interfaces and seamless compatibility with existing infrastructure. However, with the physical thickness of vertical fin shrinking down to sub-10 nm scales, the conventional silicon dioxide (SiO2) gate dielectrics become non-viable due to the severe quantum mechanical tunnelling. To overcome this material limitation, state-of-the-art FinFET architectures use an advanced high-k metal gate (HKMG) stack. The traditional oxide is replaced by a high-permittivity transition metal oxide, particularly hafnium dioxide (HfO2), which has a significantly higher dielectric constant (κ=25) than silicon dioxide (κ=3.9). The high-k dielectric material enables a physically thicker insulating layer to suppress quantum tunnelling leakage but maintain the same capacitive gate control quantified mathematically as a sub-nanometer Equivalent Oxide Thickness (EOT).

This is done by replacing the polysilicon gate electrode used in previous generations with engineered metal gate electrodes to remove the parasitic phenomenon called the polysilicon depletion effect. This metal gate stack is formed with an adjustable combination of work function metals, e.g., titanium nitride (TiN) for PMOS and tantalum nitride (TaN) for NMOS, conformally deposited over the hafnium oxide

layer. By fine tuning the work function of these atomic layers, the flat band voltage can be tuned and the V_{TH} of the FinFET can be tailored without the use of heavy channel ion implantation. This advanced material architecture suppresses the ionized impurity scattering in the ultra-thin silicon fin to preserve the high carrier mobility and achieve the maximum I_{ON} at low operating voltages.

1.6.4. Enabling Downscaling and Mitigating SCE and DIBL

The FinFET architecture provides multi-directional electrostatic control by wrapping the gate electrode around three sides of the vertical channel, thereby effectively eliminating SCE and DIBL. In a planar device, the lateral electric field from the drain can easily bypass the gate control by penetrating deep into the bulk substrate. In a FinFET, the vertical gate field penetrates the ultra-thin fin from both opposing sidewalls simultaneously, compressing the internal depletion regions and shielding the channel core from the drain field. The dominance of this multi-axis gate prevents the horizontal drain voltage from lowering the source injection barrier, which effectively suppresses DIBL and stabilizes the V_{TH} from drain-bias fluctuations. Additionally, the parasitic subsurface punch-through paths are fully suppressed due to the physical restriction of the channel body depth by the narrow W_{fin} which restores the SS near the ideal thermionic value of 60 mV/decade and limits the I_{OFF} to the femto-ampere level.

1.7. How and Why FinFET are good for Sensor

The structural and material triumphs that allowed the FinFET to rescue the semiconductor roadmap from the power wall also established an ideal physical framework for solid-state sensor design. When a standard planar MOSFET is utilized as a sensor, its active carrier transport is confined to a flat, two-dimensional sheet at the silicon surface, which severely limits the interaction volume between the moving charge carriers and external physical stimuli. The FinFET architecture, on the other hand, takes the channel out of the plane of the substrate and forms a 3D vertical fin, thereby significantly increasing the surface-area-to-volume ratio of the active conducting core [15]. This vertical geometry allows the internal inversion layer to be exposed to environmental fields from several directions at the same time. The W_{fin} is

selected to be very small to suppress the short channel effects and thus the entire volume of the channel is fully depleted and is under tight multi-axial electrostatic constraint, assuring that even a microscopic external perturbation will cause an immediate, highly measurable reorganization of the internal carrier density profile.

1.7.1. FinFET as Biosensors

The high-k metal gate (HKMG) stack and the physical topology of the FinFET provide an excellent platform for chemical and biological sensing applications often referred to as FinFET based Biosensors (BioFETs). The vertical sidewalls provide an unshielded three-dimensional sensing surface by removing the metal gate electrode and exposing the underlying high-permittivity HfO_2 passivation layer directly to a fluidic or gaseous environment. Target chemical ions or biomolecules bound to specific receptor molecules immobilized on these vertical oxide facets act as a direct, fluidic gate bias by virtue of their intrinsic electrical charge. The ultra-thin fin geometry provides exceptional electrostatic coupling and so this surface-bound charge instantaneously modulates the conductivity throughout the entire depth of the vertical silicon channel. This bulk volume modulation leads to a very sharp change of the device V_{TH} and an exponential change of the subthreshold current. This enables the FinFET sensor to achieve single molecule detection limits and response times that are orders of magnitude better than conventional flat-panel chemical sensors[15].

1.7.2. FinFET as magnetic sensor

This remarkable sensitivity is particularly useful when the multi-gate architecture is adapted for magnetic field sensing, a device modification known as the Magnetic FinFET (MAGFinFET). The moving charge carriers within a vertical silicon fin are instantaneously exposed to a localized Lorentz force when a current flows axially from the source to the drain in the presence of an external magnetic field vector[16]. The magnetic force accelerates the electrons transversely across the narrow width of the fin, driving them toward one of the vertical sidewalls depending on the direction of the magnetic vector. The channel is formed by two symmetric parallel vertical gates. This

leads to a transverse deflection of the carriers, resulting in an asymmetric carrier accumulation and thus a Hall voltage between the opposite sidewalls. This internal charge asymmetry is converted directly into a measurable current imbalance (ΔI_{DS}) between the two split drains by strategically modifying the contact layout at the drain terminal such as splitting a single drain into two parallel symmetric contacts, thus turning a standard computing architecture into an ultra-sensitive, nano-scale multi-axial magnetic sensor[16].

1.8. Transition to Multi-Axis Analysis and Future Scope

From the above discussion, it can be concluded that the FinFET architecture is highly suitable and particularly promising for advanced solid-state sensor applications due to its strong electrostatic control and high surface-to-volume ratio. Moreover, as discussed earlier in this chapter, external magnetic field sensing provides one of the most practical and efficient approaches for nanoscale navigation systems. To better understand how these three-dimensional device architectures can be optimized for complex operating conditions, a detailed review of existing research is necessary. Therefore, **Chapter 2** presents a comprehensive discussion on the structural design of previously reported magnetic sensors, their inherent single-axis sensing limitations, the existing research gaps related to multi-axis vector detection, and their potential application in the navigation of micro-medical robot.

CHAPTER 2

LITERATURE REVIEW AND RESEARCH OBJECTIVE

2.1. Introduction

In the previous chapter, the evolution of semiconductor technology from conventional planar MOSFETs to advanced 3D FinFET architectures was discussed. The study also highlighted how the unique geometry of FinFETs makes them highly promising for advanced sensor applications due to their strong electrostatic control and high surface-to-volume ratio. Furthermore, it was established that the Earth's magnetic field can serve as an effective and practical medium for direction sensing and nanoscale navigation.

In this chapter, several existing magnetic sensor designs based on advanced 3D FinFET architectures will be reviewed. The discussion will also address the inherent limitation of conventional MAGFinFET structures, which are primarily restricted to single-axis sensing and therefore cannot accurately detect orientation changes in multiple directions. As a result, multi-directional sensing architectures become essential for achieving precise and reliable spatial tracking. Additionally, this chapter

will explore how such magnetic sensing systems can be utilized for the navigation and spatial tracking of medical micro-robots.

2.2. Overview of Traditional Architecture

Before discussing the architectural necessity of the multi-gate FinFET for nanoscale magnetic sensing, it is essential to first evaluate the operational principles and physical limitations of classical solid-state magnetic sensors. In this section, we will briefly introduce three dominant technologies that have historically been used for magnetic sensing.

2.2.1. Bulk Silicon Hall Plates

Bulk silicon Hall plates are among the most commonly used magnetic sensors in conventional macroscopic systems. These devices are formed using a flat and continuous layer of doped bulk silicon integrated with four orthogonally positioned contact terminals. When a magnetic field is applied perpendicular to the sensor surface, the resulting Lorentz force deflects the moving charge carriers toward the device edges, producing a measurable Hall voltage. A schematic illustration of the Lorentz-force-induced carrier deflection occurring within a continuous n-type bulk silicon Hall plate is presented in Figure 2.1[17]. Conventional bulk silicon Hall sensors generally

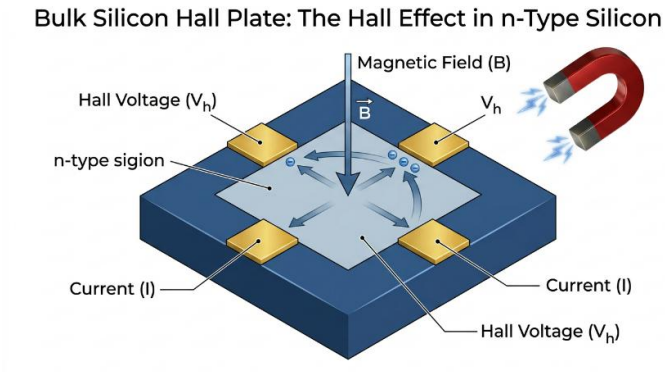
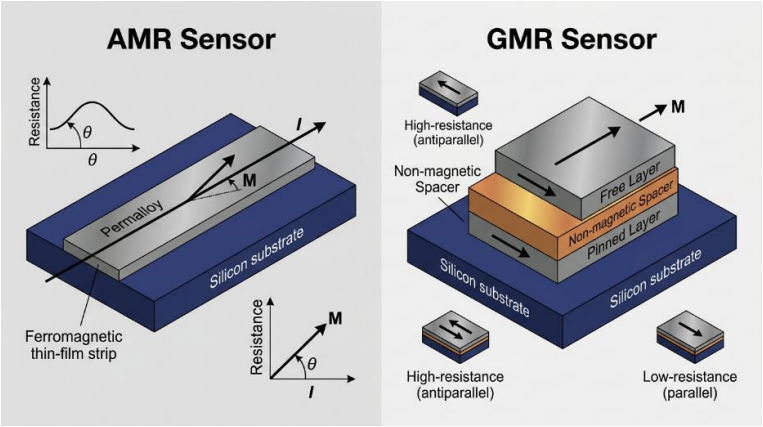


Figure 2.1. Mechanism of bulk silicon Hall sensor

demonstrate current-related sensitivities in the range of 100 to 200 V/AT. However, their overall performance is significantly limited by intrinsic offset voltages arising from lithographic imperfections and piezoresistive stress introduced during packaging. To reduce the zero-field offset errors, advanced dynamic offset cancellation techniques are typically used, including current spinning and chopping methods. While effective, these methods greatly increase the required silicon area and often contribute additional switching noise to the sensing circuitry.

2.2.2. Magnetoresistive Sensors (AMR/GMR)

Anisotropic Magnetoresistance (AMR) and Giant Magnetoresistance (GMR) sensors are based on quantum mechanical electron scattering effects. Such sensors are usually made by depositing alternating very thin layers of ferromagnetic and non-magnetic metallic materials. The basic structures and the corresponding mechanisms of resistance change of AMR and GMR sensors are shown in Fig. 2.2[18]. GMR and TMR sensors are characterized by a much higher magnetic sensitivity and faster response characteristics than conventional silicon Hall plates. However, their high non-linearity



(a) (b)

Figure 2.2. Structural configuration and resistance variation mechanism of (a) AMR and (b) GMR

and intrinsic magnetic hysteresis effects significantly restrict their application in continuous ultra-low-power integrated tracking systems. Moreover, these devices use special ferromagnetic materials, such as cobalt-iron alloys, which are hard to incorporate in standard silicon CMOS fabrication lines without contamination. Consequently, expensive and custom Back-End-Of-Line (BEOL) processing techniques are required, which further limits their scalability for high-density sensor array applications[19].

2.2.3. Planar Magneto-transistors (MAGFETs)

A traditional MAGFET is essentially a conventional planar MOSFET that is structurally modified commonly by splitting the drain terminal to enable magnetic field sensing. Its operation is based on the same galvanomagnetic Lorentz-force-induced carrier deflection observed in Hall sensors, while the intrinsic transistor gain mechanism amplifies the generated signal. The three-dimensional structure of the planar split-drain MAGFET, illustrating the transverse carrier deflection produced under an externally applied magnetic field, is shown in Figure 2.3[20]. Although planar MAGFETs provide better CMOS compatibility compared to GMR sensors, they face significant challenges during aggressive geometric scaling. As the lateral channel

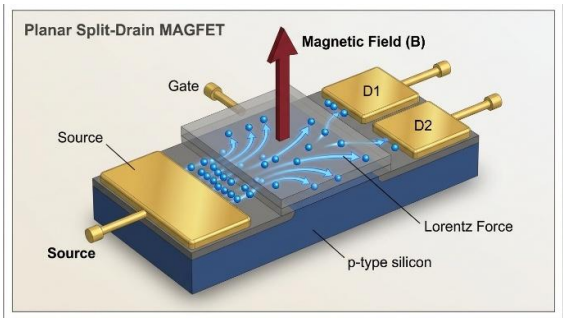


Figure 2.3. 3D structure of planar split drain MAGFET

length decreases, the carrier deflection path becomes extremely short, limiting the development of sufficient charge asymmetry and resulting in poor Signal-to-Noise

Ratios (SNR). Moreover, the large planar silicon–oxide interface introduces substantial 1/f (flicker) noise at low operating frequencies, which can easily overwhelm the weak magnetic response unless the device is operated under excessively high bias currents[21].

2.3. The Scaling and Biomedical Power Dilemma

Together, these limitations of conventional sensor architectures highlight the fundamental incompatibility of these sensors to modern deep-nanometer applications. The planar Hall plates and MAGFETs are aggressively scaled down and the effective interaction volume is reduced significantly, leading to a major loss of magnetic sensitivity. To overcome this degradation, conventional devices generally require the injection of large bias currents, often in the milliampere range. The limitations of these conventional sensor architectures collectively point to their fundamental incompatibility with modern deep-nanometer applications. The planar Hall plates and MAGFETs are aggressively scaled down and the effective interaction volume is reduced significantly, leading to a major loss of magnetic sensitivity. To mitigate this degradation conventional devices usually require injection of large bias currents often in the milliampere range. However, such a power-intensive approach is impractical for untethered biomedical micro-robots operating inside the human vascular system. The excessive self-heating generated by these high currents can easily exceed biologically safe thermal limits, potentially causing permanent damage to nearby tissues and cells. Therefore, achieving highly sensitive, low-noise, and cross-talk-free magnetic tracking at the nanoscale requires a fundamental shift from conventional planar structures toward advanced three-dimensional fully depleted multi-gate architectures.

2.4. Magnetic FinFET (MAGFinFET) Devices

To overcome the severe scaling limitations and power challenges associated with conventional planar sensors, recent research has increasingly shifted toward three-dimensional device architectures. The following section presents a detailed discussion of the advanced Magnetic FinFET (MAGFinFET), focusing on how its 3D multi-gate

structure and split-drain configuration help restore magnetic sensitivity at nanoscale dimensions. In addition, the performance characteristics and key metrics reported in existing literature will also be systematically reviewed and analysed.

2.5. Fundamental Concept of MAGFinFET

In this section we will discuss the main principle on which MAGFinFET are operated and how they help us to detect the magnetic field. Basically, there are two drain split method by which we use FinFET as a magnetic sensor. Let's discuss about that principle in following sections.

2.5.1. MAGFET: split drain configuration

The Magnetic Field Effect Transistor (MAGFET) is a solid-state magnetic sensor derived from the conventional planar MOSFET architecture. The key structural modification in a traditional MAGFET is the incorporation of a symmetrical split-drain configuration. Instead of a single drain terminal, the MAGFET channel terminates into two separate drain contacts, represented as D_1 and D_2, while sharing a common gate (G) and source (S). The top-view geometric layout of the split-drain configuration, highlighting the effective channel dimensions and the physical separation distance (d) between the drain contacts, is illustrated in Figure 2.4[22].

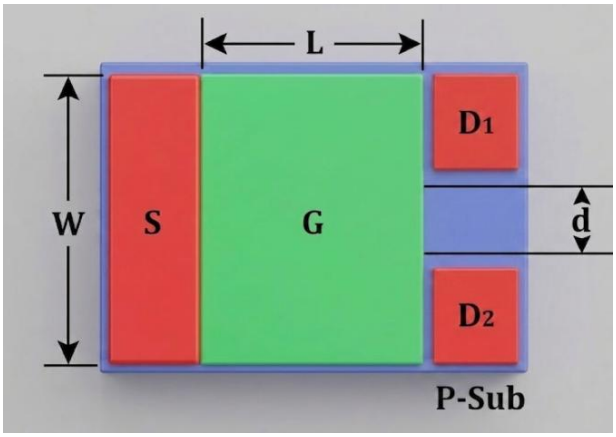


Figure 2.4. Split-drain configuration of MAGFET

The MAGFET sensing operation is based on galvanomagnetic current-mode Hall effect. In the absence of an external perpendicular magnetic field, the charge carriers move symmetrically along the channel and therefore the drain currents at both contacts (I_{D1} and I_{D2}) are almost similar. If, however, an external magnetic field is applied perpendicular to the sensor surface, the moving carriers in the semiconductor channel are subjected to a Lorentz force.

This force laterally deflects the carriers, disturbing the symmetrical current distribution and causing the total drain current to divide unevenly between the two drain terminals. The resulting ΔI_D acts as the primary sensing parameter for determining both the magnitude and direction of the applied magnetic field, and is expressed as:

$$\Delta I_D = I_{D1} - I_{D2} \tag{2.1}$$

The current imbalance between the split drains at present is directly related to the Hall current (I_H). The mathematical relationship governing this current difference is given by (2.2)[23].

$$\Delta I_D = \frac{I_H}{2} = \frac{1}{2}\,\mu_{ch}\,\frac{L}{W}\,G_H I_D B \tag{2.2}$$

where μ_{ch} is the carrier mobility in the channel, L is the channel length, W is the channel width, G_H is the geometrical correction factor, I_D is the total drain current (I_{D1} + I_{D2}) and B is the externally applied perpendicular magnetic field. The relative sensitivity (S_R) is defined to evaluate the performance of the MAGFET using the geometric and material properties of the device as:

$$S_R = \frac{1}{2}\,\mu_{ch}\,\frac{L}{W}\,G_H \tag{2.3}$$

In addition, the theoretical maximum relative sensitivity (S_{IMAX}) is limited by the carrier mobility and the device aspect ratio, expressed as:

$$S_{IMAX} = 0.37\mu_{ch} \quad for \quad \frac{L}{W} \to \infty \tag{2.4}$$

The theoretical analysis suggests that the sensitivity can be enhanced by increasing the aspect ratio L/W. However, in practice, the current deflecting mechanism takes place in a relatively short Hall region, where the Hall voltage cannot fully compensate the Lorentz force. Thus, for improving the operational sensitivity, the planar MAGFET geometry generally requires a small channel width (W) to effective channel length.

2.5.2. MAGFET: non-split drain (gapless contact)

Based on the basic operating principles of the conventional MAGFET, the geometrical correction factor (G_H) must be optimized to maximize the magnetic sensitivity. We demonstrate that for a normal symmetric split-drain architecture, a GH value close to 1 requires the physical isolation gap between the two drain halves to be fabricated as narrow as possible. However, aggressive scaling of this separation distance leads to significant fabrication limitations and possible structural discontinuities. Fig. 2.5. Structural configuration of the gapless non-split drain MAGFET, with the continuous drain topology for the extraction of the differential current signals without the introduction of geometric discontinuities[24].

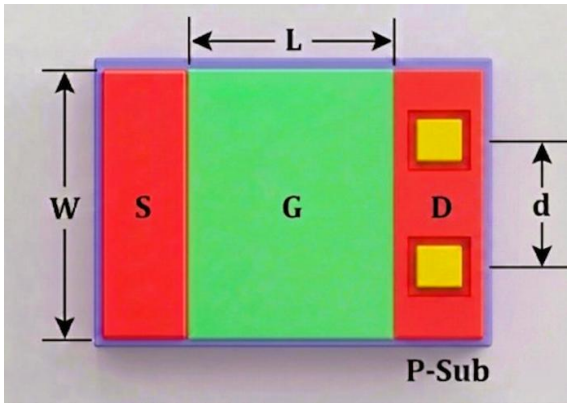


Figure 2.5. Non-split drain (Gapless contact)

To circumvent the fabrication constraints and electrical losses associated with a physical gap, researchers proposed an alternative architectural concept: the gapless, or non-split drain MAGFET. Rather than physically dividing the semiconductor drain into two isolated regions, this design utilizes a single, continuous drain structure. To

support and measure the ΔI_D arising from the magnetic induction force, two distinct electrical contacts are placed at the opposite lateral edges of this unified drain region[22].

The major advantage of the non-split drain configuration is the carrier dynamics transport. If there is no physical barrier or structural discontinuity partitioning the drain, the charge carriers continuously deflect from the channel deep into the drain region and eventually flow out through the nearest respective contact. This continuous monolithic structure suppresses the typical electrical losses and scattering due to the discontinuity of a physical gap. Hence, this design evolution showed that a physical separation of drain regions is not essentially necessary for detecting present differences caused by the Lorentz force, and is independent of the minimum-gap restrictions imposed by standard fabrication technologies.

2.5.3. 3D Multi-Gate Solution

Recent work has addressed the large area overhead and power constraints of traditional planar sensors by embedding galvanomagnetic sensing directly into advanced FinFET architectures. The MAGFINFET solves a lot of geometric scaling problems of planar devices by converting the conductive channel into a fully depleted 3D vertical silicon fin. The multi-gate structure provides a strong electrostatic control from multiple directions which allows for an efficient operation even in the subthreshold region. More importantly, the vertical fin geometry provides a high surface-to-volume ratio that enables a larger fraction of the mobile charge carriers to interact with the external magnetic field. This increased interaction results in a larger deflection of the carriers induced by the Lorentz force without the need of a large planar sensing area

2.5.4. Performance Metrics in Current Literature

Recent studies have shown that split-drain MAGFinFETs are capable of achieving exceptionally high relative current sensitivities, often surpassing conventional planar MAGFETs while utilizing a much smaller active silicon area. In addition, these devices preserve near-ideal subthreshold swing characteristics, allowing them to

operate with very low bias currents, typically within the microampere range. This low-power operation is particularly important for biomedical applications, as it satisfies the

TABLE 2.1. Summary of Existing Magnetic Sensor Technologies in Literature

Sensor Technology	Typical Power Consumption	Sensing Capability	Primary Limitation Identified in Literature
Bulk Silicon Hall Plates	High (mA range)	Single-Axis	High offset voltage and low SNR at nanoscale
AMR / GMR Sensors	Medium to High	Single-Axis	High non-linearity, hysteresis and poor CMOS compatibility.
Planar MAGFETs	High (mA range)	Single-Axis	Weak Lorentz deflection path of sub-32nm nodes
Conventional MAGFinFETs	High (~ 1 mA)	Single-Axis	Arrays cross talk and multi directional vectors tracking incapability.

strict thermal and energy requirements necessary for the safe and continuous tracking of medical micro-robots within biological environments.

2.6. Problem Statement

While MAGFinFETs are successful in overcoming many of the major challenges associated with conventional planar sensors, such as scaling limitations, high power consumption, and low sensitivity, they still suffer from a significant drawback. They are typically limited to single-axis magnetic field sensing. Therefore, these devices are not capable of accurately resolving the full orientation of an externally applied magnetic field. However, for practical navigation applications, particularly with advanced tracking systems, integration of multiple FinFET-based magnetic sensors on one platform is necessary to develop multi-directional sensing capability. However,

close integration of two or more MAGFinFETs brings another big challenge due to the electromagnetic and electrostatic cross-talk among neighbouring devices. This results in an interesting research question for simultaneous operation of multiple FinFET sensors on the same chip while maintaining independent and interference free magnetic sensing performance.

From the above discussion we can conclude that for architecture of micro scale magnetic sensor we have to face following problems:

a) Reduced Interaction Volume: The scaling of planar magnetic sensors down to micro- and nanoscale dimensions leads to a drastic decrease of the carrier deflection path, which in turn causes a weaker Lorentz-force interaction, and hence a reduced magnetic sensitivity.

b) Degradation of Signal-to-Noise Ratio (SNR): At very small dimensions, the generated magnetic signal becomes very weak and is easily dominated by thermal noise and interface related 1/f (flicker) noise.

c) Thermal Constraints in Biomedical Systems: The enhancement of the nanoscale sensitivity often requires large bias currents which can lead to excessive self-heating and exceed the safe thermal limits needed for in-vivo biomedical micro-robot applications.

d) Single-Axis Sensing Limitation: Conventional micro-scale sensor architectures including split-drain MAGFinFETs, are typically limited to single-axis magnetic field detection and thus cannot accurately sense complex three-dimensional orientation changes.

e) Cross-Talk in Multi-Sensor Arrays: The integration of multiple single axis sensors on the same platform for multi-directional tracking increases silicon area and introduces large electromagnetic and electrostatic cross-talk phenomena between adjacent devices.

2.7. Research gap and objective

The 3D multi-gate architecture has the advantage of geometrical scaling, though the present MAGFinFET designs do not offer a full-featured multi-directional sensing capability to avoid prohibitive cross-talk penalties. And also Keep take care of problem mention in previous section the main aim of this research is focused on solution of these problems.

The above mention problem can we solve by a proposed device having the following advancement in the 3D-architecture. The aim of this work is to develop multi direction sensing device without any cross disturbance for the navigation purpose.

2.7.1. Dimensional Scaling: Fin Width and Fin Length Optimization

The scaling down to the deep nanoscale is necessary for high-density integration and micro-robotic applications. However, aggressive miniaturization usually leads to serious electrostatic problems such as SCE and DIBL. A proper optimization of W_{fin} and overall fin length (L_{fin}) is a key factor in the proposed 2D-MagFinFET architecture to keep good electrostatic control while at the same time maximize the magnetic sensitivity.

The multi-gate structure with ultra-thin fin width can achieve excellent control of the fully depleted channel, which can effectively reduce SCEs and DIBL and maintain near-ideal subthreshold characteristics. More importantly, the strong nanoscale confinement results in a dramatic enhancement of the galvanomagnetic response. The fin width is very narrow so that the deflected charge carriers only travel a short transverse distance before reaching the dielectric boundary. So even a small change in magnetic field will quickly cause electrons to pile up next to the sidewall, and cause a rapid and very localized charge imbalance.

Furthermore, the global magnetic sensitivity is strongly dependent on the total physical length of the fin structure. The length of the fin defines the total distance that the electrons travel between the source and the asymmetric drain contacts. Increasing the fin length increases the carrier transit time inside the device, which allows the orthogonal Lorentz force to act on the moving electrons over a longer distance. The

longer fin therefore results in a much greater cumulative transverse deflection before the carriers reach the drain terminals, and thus significantly enhances the multi-axial sensing capability of the proposed device.

2.7.2. Substrate Engineering: The Silicon-on-Insulator (SOI) Advantage

To further enhance the performance of the proposed device for the high-sensitive nanoscale tracking applications, the device is intentionally designed on a SOI substrate rather than the traditional bulk silicon platform. The existence of a thick insulating BOX layer underneath the active fins offers a number of critical electrostatic and operational advantages that effectively compensate the drawbacks of traditional sensor structures.

From the device physics point of view, the SOI structure provides a complete dielectric isolation, which eliminates unwanted parasitic conduction paths under the channel. This greatly reduces the off-state leakage current and enhances the overall power efficiency of the device. In addition, the BOX layer effectively suppresses deep-substrate SCEs and DIBL, which are common in bulk FinFET devices at highly scaled dimensions.

More importantly, in galvanomagnetic sensing applications, the BOX layer acts as a strong physical barrier for the deflected charge carriers. The moving electrons are acted upon by a Lorentz force from an external magnetic field that drives the carriers transversely across the channel region. In conventional bulk structures, many of these deflected electrons can scatter into the substrate, reducing the effective sensing signal. However, in the SOI-based design, the buried oxide blocks any downward carrier penetration and the deflected charge is fully confined within the active fin region.

The strong carrier confinement results in the displaced electrons being accumulated more efficiently along the fin sidewalls, and thus a larger charge imbalance in the channel. Consequently, the induced galvanomagnetic response is greatly amplified, significantly improving the overall multi-axial sensitivity and sensing performance of the proposed 2D-MagFinFET architecture.

2.7.3. Ultra-Low Power Operation and Mitigation of Biomedical Thermal Constraints

The proposed dual-parallel fin 2D-MagFinFET is structurally optimized for high galvanomagnetic sensitivity under an ultra-low bias current regime of 1 μA -100 μA to meet the stringent power constraints of conventional magnetic sensors for biomedical applications.

As noted, before, conventional micro-scale sensors suffer from poor signal-to-noise ratios, and have to artificially compensate by injecting massive bias currents, often in the milliampere range. This power-hungry approach produces a lot of Joule heating. In the extremely sensitive context of in-vivo biomedical tracking, for example within the human vascular system, such a level of thermal dissipation directly violates biological safety limits and can cause immediate and irreversible cellular damage.

The proposed device, using the better electrostatic control and the tighter carrier confinement of the multi-gate SOI architecture, achieves a strong noise-free current imbalance without strong current injection. The sensor has been designed to operate in this very small window of 1 μA to 100 μA to drastically lessen the overall static and dynamic power consumption. More importantly, it completely removes localized self-heating. This architecture thus successfully addresses the thermal limitations of micro-medical systems, ensuring permanent, tissue-safe operation and making the device highly appropriate for untethered navigation of medical micro-robots.

2.7.4. Multi-Axis Sensing and Cross-Talk Elimination

Accurate spatial navigation of medical micro-robots in complex biological environments requires continuous and real-time sensing of their multi-axial orientation. However, the conventional split-drain MAGFinFET structures are limited to single axis magnetic field detection. Multi-directional sensing has been conventionally achieved by integrating several orthogonally placed sensors into dense arrays. This approach, based on arrays, works well at larger scales but is highly inefficient when it comes to nano-scale applications as it increases the active silicon area and leads to significant electromagnetic and electrostatic cross-talk between

neighbouring devices. Such unwanted interactions would distort the individual sensing signals and degrade the overall tracking accuracy.

To overcome these shortcomings, the proposed device uses a novel dual-parallel fin design. The proposed design includes two parallel vertical silicon fins in a single gate-controlled structure with asymmetrically designed non-split drain contacts, instead of several independent single-axis sensors.

This unique structural design allows the detection of magnetic fields in multiple axes without interference. In a complex magnetic environment, the orthogonal magnetic field components, especially in the B_Y and B_Z directions, generate different Lorentz forces on the moving charge carriers when the device is subjected to a magnetic environment. The dual-fin topology and asymmetric drain design result in spatially separated directional carrier deflections that are converted into independent electrical responses. Accordingly, the device is capable of internally decoupling multiple directional signals and can simultaneously detect orientation changes in different axes with a single compact structure.

The proposed device combines multi-directional sensing in a single architecture avoiding the use of large multi-device sensor arrays. This not only reduces the overall device footprint, but also removes inter-device cross-talk that normally impacts conventional array-based systems. Thus, the proposed architecture can provide highly accurate, interference-free multi-axial sensing while maintaining the ultra-compact dimensions required for deep-nanoscale biomedical navigation and micro-robotic applications.

2.8. Chapter Summary and Transition to Methodology

In this chapter, a detailed review of solid-state magnetic sensor technologies was presented, focusing on the major physical, electrical, and structural challenges associated with deep-nanoscale scaling. The discussion showed that although conventional three-dimensional MAGFinFET architectures effectively overcome many of the power consumption and sensitivity limitations of traditional planar

devices, their symmetrical split-drain configuration inherently limits them to single-axis magnetic field detection. Moreover, it was established that implementing multi-directional sensing through high-density arrays of single-axis sensors is not suitable for nanoscale biomedical applications, as it significantly increases the silicon footprint and introduces severe electromagnetic cross-talk between neighbouring devices.

To overcome these limitations, this chapter proposed the conceptual design of a novel multi-axis sensor known as the dual-parallel fin architecture. The proposed architecture combines customized asymmetric non-split drain contacts, aggressive fin scaling, and a SOI substrate to theoretically achieve fully decoupled and cross-talk-free spatial tracking while operating within an ultra-low power range of 1 μA to 100 μA, making it suitable for tissue-safe biomedical applications.

Based on this theoretical and structural foundation, the next chapter (**Chapter 3**) will focus on the detailed device architecture and computational methodology of the proposed sensor. It will present the complete TCAD simulation framework, including the optimized device dimensions, quantum mechanical carrier transport models, and numerical boundary conditions used to validate the multi-directional sensing performance of the proposed device architecture.

CHAPTER 3

2D-MagFinFET: ARCHITECTURE AND METHODOGOLOGY

3.1. Introduction

The previous chapter detailed the primary scaling and power concerns of traditional solid-state magnetic sensors. Specifically, the spatial sensing limitations and array-induced cross-talk of typical MAGFinFET structures. To meet the challenges at the nano-scale, this chapter presents the structural design and operation methodology of the proposed dual-parallel fin "Two Directional Magnetic Fin Field Effect Transistor (2D-MagFinFET). This nomenclature explicitly highlights the architecture's capability to detect and resolve magnetic field vectors in two independent orthogonal directions (B_Y and B_Z) simultaneously within a single device footprint. This chapter provides a detailed discussion on the device geometry and the galvanomagnetic transport mechanisms contributing towards multi-directional magnetic field sensing. Additionally, the validation methodology of the proposed sensor architecture is also discussed, showing its potentiality for accurate and low-power spatial tracking of medical micro-robots in complex biomedical environments. A systematic validation is

established with the Synopsys Sentaurus TCAD by a comprehensive three-dimensional computational framework.

3.2. Synopsys Sentaurus TCAD Simulation Overview

To properly simulate the complex nanoscale geometry and the galvanomagnetic transport behaviour of the proposed 2D-MagFinFET, the simulation methodology is divided into several operational stages, using specialized Synopsys Sentaurus TCAD tools. This modular simulation procedure allows detailed structural modelling, accurate physical analysis and reliable extraction of the electrical and multi-directional magnetic sensitivity characteristics of the device.

Synopsys Sentaurus is a leading TCAD software suite for the simulation, analysis and optimization of advanced microelectronic devices. It is a virtual semiconductor laboratory that enables researchers to numerically solve the fundamental equations of solid-state physics to model the fabrication processes, the electrical operation and the reliability characteristics of complex nano-scale structures such as FinFETs and SOI devices.

The complete modular workflow of the Synopsys Sentaurus TCAD framework is shown in Figure 3.1. The Sentaurus Workbench (SWB) Graphical User Interface

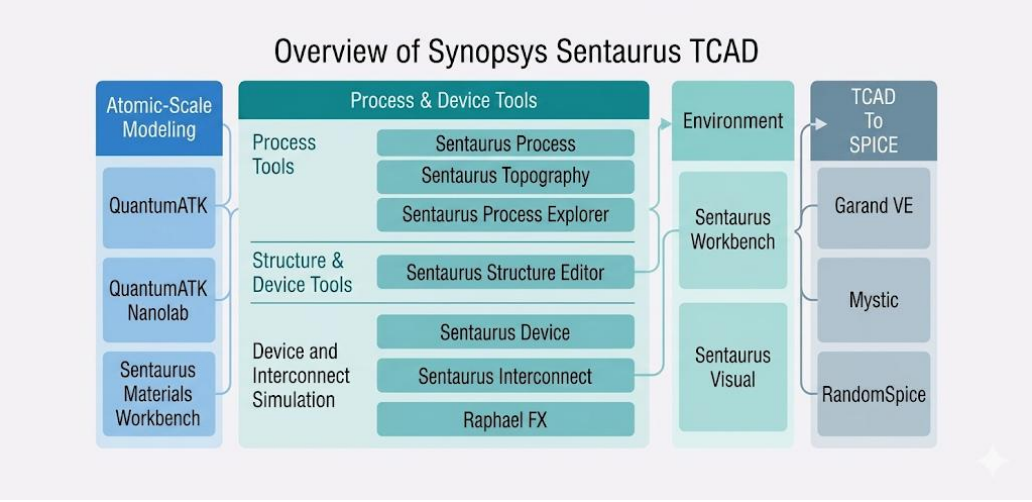


Figure 3.1. Overview of Synopsys Sentaurus TCAD

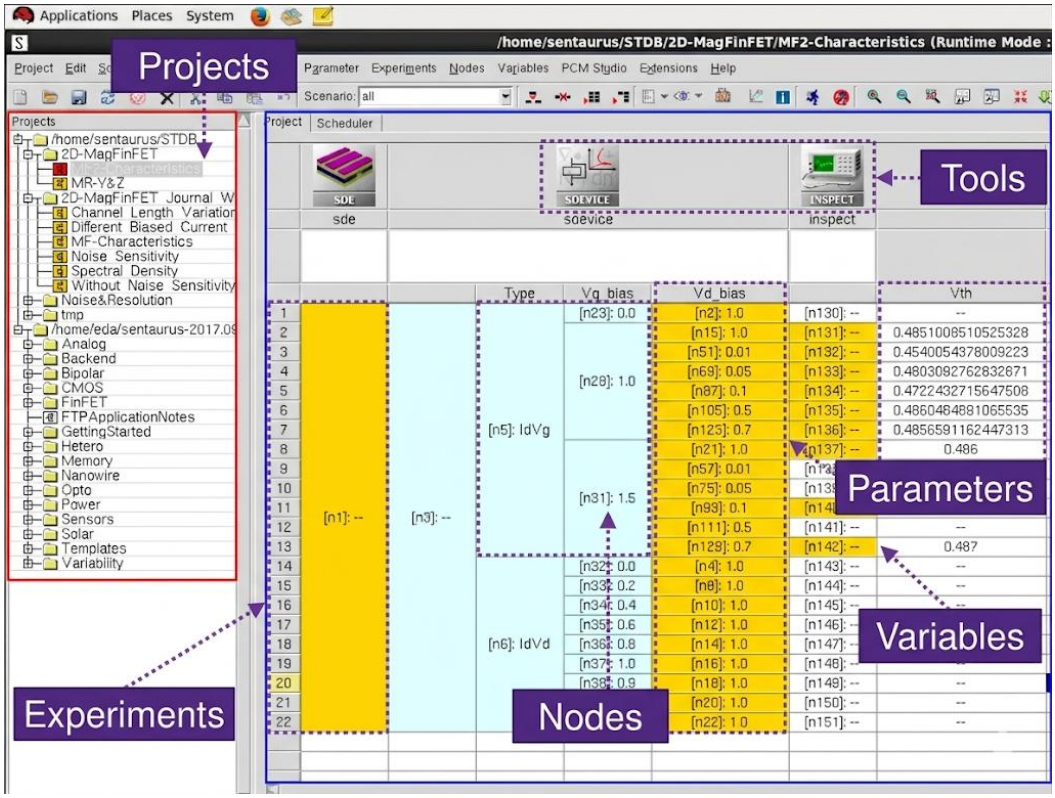


Figure 3.2. GUI of Sentaurus Workbench (SWB)

(GUI) that integrates the different simulation modules and manages the scheduling of parameter sweeps during the simulation process is shown in Figure 3.2. The complete simulation procedure and the customized Sentaurus tools used in this study are described in the following sections[25].

3.2.1. Sentaurus Process (sprocess)

The Synopsys Sentaurus TCAD framework's advanced simulation tool for modelling semiconductor fabrication procedures is called Sentaurus Process (sprocess). It is specifically designed to model realistic cleanroom manufacturing processes including anisotropic silicon fin etching, thermal oxidation and controlled dopant implantation. Although sprocess is very effective in evaluating the practical manufacturability of semiconductor devices, the main objective of this work is to theoretically investigate and optimize the geometric and galvanomagnetic transport behaviour of the proposed

multi-axis architecture[26]. Therefore, to achieve accurate and mathematically controlled dual-parallel fin geometries without the structural variations introduced by fabrication-based simulations, the device structure in this work is directly defined using the Sentaurus Structure Editor (SDE).

3.2.2. Sentaurus Structure Editor (SDE)

In this work the primary tool for the direct and highly controlled construction of the semiconductor device topology is SDE. The proposed 2D-MagFinFET is constructed with 3D geometric primitives such as cuboids, cylinders and planes. These structures are combined and modified using precise Boolean operations to define the exact geometry of the dual-parallel fins, SOI substrate and customized asymmetric drain regions. Within this geometry, SDE is also used to assign material properties to each device region and to define the initial doping concentrations needed[25].

In addition to the structural design, the SDE is also responsible for the creation of the computational mesh used in the numerical simulation. This mesh has discrete nodal points where the equations describing the physics are solved. An adaptive meshing method is applied to refine the mesh adaptively around the critical dielectric interfaces and along the fin sidewalls. The local refinement is that the numerical representation of the focused galvanomagnetic charge distribution is improved and the efficiency of the whole simulation time is preserved.

3.2.3. Sentaurus Device (sdevice)

Sentaurus Device (sdevice) is the physics core solver of the TCAD simulation framework. Its main function is to transform the static device structure generated in SDE into dynamic electrical and magnetic performance characteristics. We use Finite Element Method (FEM) for discretizing the computational mesh and for solving a strongly coupled system of Partial Differential Equations (PDEs) at each mesh node to simulate the steady-state behaviour of the proposed semiconductor device.

The simulation is fundamentally based on core semiconductor transport equations. In particular, sdevice solves Poisson’s equation to determine the electrostatic potential

(φ) throughout the multi-gate structure that relates the electrostatic potential to the local space charge density (ρ) and the material permittivity (ε) as follows:

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon} \tag{3.1}$$

Meanwhile, to model the carrier transport under the applied ultra-low 1V bias condition, sdevice solves the carrier continuity equations. For electrons, where (n) is the electron concentration, the continuity equation contains the divergence of the electron current density (Jn) and the processes of carrier generation (G) and recombination (R):

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla . \ J_n + G - R \tag{3.2}$$

sdevice solves these transport equations together with the necessary galvanomagnetic physical models to accurately evaluate the Lorentz force on the mobile electrons under the externally applied B_Y and B_Z. This allows an accurate analysis of the transverse electron deflection and the resulting current imbalance created at the asymmetric drain terminals[27].

3.2.4. Sentaurus Inspect

The physical transport simulations are performed with Sentaurus Device and the data is mainly analysed and visualized with Sentaurus Inspect as a post-processing tool in the TCAD workflow. sdevice calculates the underlying mathematical and physical behaviour of the device, while Inspect translates these numerical simulation outputs into measurable electrical and galvanomagnetic properties[27].

First, the tool is applied to extract important DC electrical parameters from the simulated transfer characteristics (I_D-V_{GS}). In particular, Inspect correctly evaluates the V_{TH} and SS to assess the electrostatic control and short-channel behaviour of the dual-parallel fin structure. The switching efficiency of the device is also studied by extracting I_{ON} and I_{OFF}. The resulting SR further validates the effectiveness of the SOI

architecture, and verifies the ultra-low, tissue-safe current range of 1 µA to 100 µA operation of the device.

$$Switching\ Ration\ (SR) = \frac{I_{ON}}{I_{OFF}} \tag{3.3}$$

In addition to the standard electrical characterization, Inspect is the main tool for evaluation of the multi-directional magnetic sensitivity of the proposed device. The software analyses the localized drain currents at the asymmetric contacts (I_{D1}, I_{D2}, I_{D3}, I_{D4} etc.) under different externally applied magnetic field conditions. Inspect calculates the drain current imbalance (ΔI_D) and plots it as a function of the orthogonal magnetic field components (B_Y and B_Z) to obtain the final sensitivity characteristics. The results finally confirm the primary aim of the proposed research, i.e., the independent and cross-talk free spatial magnetic tracking capability.

3.3. Proposed Architecture of the 2D-MagFinFET

Following the computational methodology, this section presents the detailed physical and geometric design of the proposed Two-Directional Magnetic Fin Field-Effect Transistor (2D-MagFinFET). The device architecture is tailored to overcome the spatial sensing limitations and the array-induced cross-talk encountered with conventional magnetic sensor structures. The proposed design provides compact, , and efficient magnetic field detection for advanced nano-scale applications by incorporating multi-axis magnetic sensing capability for both (B_Y *and* B_Z) directions on a single highly scaled silicon platform.

3.3.1. Dual-Parallel Fin and SOI Foundation

The proposed 2D-MagFinFET has a completely different basic structure from the conventional single fin MAGFET structure, by introducing a dual parallel fin configuration. In this design, two identical fully depleted vertical silicon fins are fabricated parallelly to each other along the longitudinal direction of the device. Both fins are controlled by a common gate stack, enabling synchronized electrostatic

modulation of the conductive channels, while operating within an ultra-low subthreshold current range of 1 uA to 100 uA.

Importantly, the entire multi-fin structure is fabricated on SOI substrate. The active silicon fins are separated by a thick BOX layer for electrical isolation. As explained in the theoretical framework, this BOX layer has two basic functions, namely: to inhibit subterranean leakage currents in order to mitigate SCE, and to act as a physical confinement barrier for charge carriers. The BOX layer avoids the leakage of electrons into the bulk substrate when they are deflected vertically by an external transverse magnetic field, thus forcing the accumulated charge to remain confined within the active device region and hence improving the overall magnetic sensitivity.

3.3.2. Geometric Structure

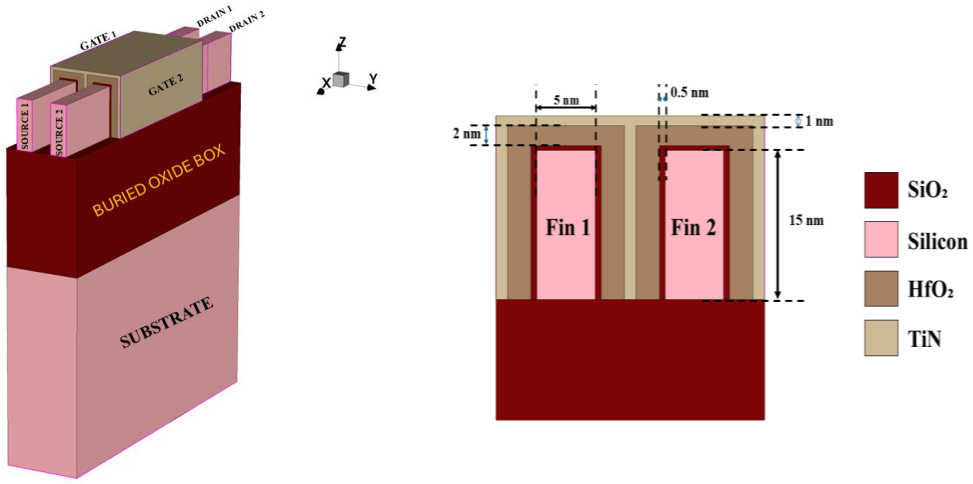
The device is made of two identical parallel silicon fins of 5 nm width and 15 nm height, which provide optimal multi-gate electrostatic control and maximize the transverse Lorentz deflection path. These fins are separated by a strict center-to-center distance of 11 nm. The total longitudinal distance from the source to the drain boundaries is 100 nm with a unified gate stack located exactly in the middle of the fins

TABLE 3.1. Geometric Dimension of Device

Parameter	Dimension
Fin Height, F_H	15 nm
Fin Width, F_W	5 nm
Interfacial Oxide thickness, t_{OX}	0.5 nm
Gate Dielectric thickness, D_{GD}	2 nm
Channel length, L_{CH}	50 nm
Gate Length, L_G	50 nm
Length from Source (S) to Drain (D) side	100 nm
Separation between Fins, D_F	11 nm
Source/Drain Doping Concentration, $N_{S,D}$	5×10^{20} cm^{-3}
Channel Doping Concentration, N_{CH}	5×10^{15} cm^{-3}

providing a well-defined effective channel length and a gate length of LG = 50 nm. Figure 3.3 shows the visual representation of the proposed device.

A HKMG stack is used to reduce the SCE and improve the gate-to-channel capacitive coupling. This multi-layer gate structure contains a 0.5 nm thin interfacial layer of SiO_2 directly adjacent to the silicon channel to minimize the interface trap density. Above this interface layer, HfO_2 is used as the primary high-κ gate dielectric and is covered by a TiN metal gate electrode. Furthermore, the whole active architecture is isolated from the bulk substrate by a 30 nm thick SiO2 BOX layer, preventing substrate leakage and confining the deflected electrons strictly within the active fin volume. The parameters of all the devices are shown in Table 3.1.



(a) (b)

Figure 3.3. (a) Geometrical structure of 2D-MagFinFET and (b) Cross-sectional view of structure

The essential semiconductor junctions are defined by the regional doping profiles. Arsenic is used for source and drain regions to make heavily doped n-type terminals with concentration of 5×10^{-20} cm^{-3}. On the other hand, boron is used in the channel region to maintain the p-type background concentration light at 5×10^{-15} cm^{-3} so that the channel remains fully depleted during operation.

3.4. Multi-Axis Contact Topology and Asymmetric Design

To enable multi-direction magnetic field sensing without the cross-talk problem of clustered sensor arrays, the proposed 2D-MagFinFET architecture uses a non-split drain approach and well-designed contact configurations. The novelty of this design lies in the possibility to independently detect the orthogonal components of the magnetic field (B_Y and B_Z). This is achieved by assigning a sensing direction to each parallel fin through customized contact orientation and structural asymmetry.

3.4.1. Fin 1: Horizontal (Y-Axis) Sensing Topology

Fin 1 is designed specifically for sensing the (B_Y) component for horizontal (Y-axis) magnetic field sensing. Two contacts D_1 and D_2 are symmetrically placed at opposite lateral sidewalls of the drain extension region to detect the change in differential current under the applied magnetic field.

Both contacts are designed with identical cross-sectional areas to ensure balanced current extraction under zero magnetic field conditions. In addition, the contacts are separated by a minimum distance of 5 nm, corresponding to the fin width (W_{fin}). As established in the operating principles of non-split MAGFET structures, maintaining this minimum spacing is important for maximizing sensitivity to lateral carrier

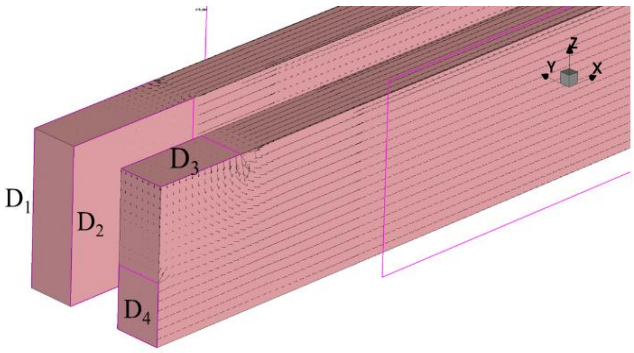


Figure 3.4. Drain contact Visualization

deflection. The precise geometric orientation and symmetrical placement of these horizontal sensing contacts on Fin 1 are visually detailed in Figure 3.4.

3.4.2. Fin 2: Vertical (Z-Axis) Sensing Topology

In contrast, Fin 2 is designed for vertical (Z-axis) magnetic field sensing, specifically targeting the (B_Z) component that induces carrier movement along the vertical direction. To detect this vertical deflection, the sensing contacts I_{D3} and I_{D4} are placed asymmetrically along the drain region. Contact D_3 is located on the upper surface of the drain, whereas contact D_4 is positioned near the bottom outer region adjacent to the BOX layer. The deliberate vertical asymmetry and unequal surface area scaling of these sensing contacts on Fin 2 are visually detailed in Figure 3.4.

Importantly, the contact areas are intentionally designed to be unequal. The lower contact (D_4) is made slightly smaller than the upper contact (D_3) to compensate for the naturally higher current density in the vicinity of the silicon-box interface, caused by accumulation effects. The deliberate geometric asymmetry is used to balance the current extraction behaviour of both contacts under normal operating conditions.

3.4.3. Zero-Field Calibration and Offset Considerations

The precise arrangement of these sensing contacts ensures accurate zero-field calibration of the proposed device. Under ideal operating conditions in the absence of an external magnetic field, the calibrated structure maintains the differential drain currents along both sensing directions at nearly zero, such that the horizontal-axis (Y) response ($\Delta I_Y = I_{D1} - I_{D2}$) and the vertical-axis(Z) response ($\Delta I_Z = I_{D3} - I_{D4}$) remain balanced. The simulation methodology further considers that any unintended structural misalignment or uncalibrated asymmetry in the contact dimensions can introduce inherent carrier deflection, leading to continuous offset errors even under zero-field conditions.

3.5. Operating Principle and Galvanomagnetic Mechanism

The operating principle of the proposed 2D-MagFinFET is based on the galvanomagnetic current-mode Hall effect occurring within the highly confined three-dimensional dual-parallel fin structure. The device operates by converting externally applied multi-directional magnetic fields into measurable differential drain current signals through the action of the Lorentz force on the mobile charge carriers flowing inside the conductive channels.

3.5.1. Zero-Field Baseline Operation

Under normal operating conditions, when a drain bias voltage (V_D) is applied and the V_{GS} exceeds the threshold voltage ($V_{GS} > V_{TH}$), conductive channels are formed within both fully depleted silicon fins. In the absence of an external magnetic field (B = 0 T), electrons move symmetrically from the source toward the drain along the longitudinal direction of the device, assumed to be the x-axis. Due to the carefully calibrated and symmetric device structure, this carrier transport results in an equal distribution of drain current across the sensing contacts. As a result, the differential drain current for both the horizontal and vertical sensing directions remains ideally zero, such that ($\Delta I_Y = 0$ and $\Delta I_Z = 0$).

3.5.2. Multi-Axis Resolution in the Dual-Fin Architecture

The dual-fin architecture is developed in order to independently decouple and quantify the orthogonal components of this Lorentz force in an effort to eliminate the cross-talk of conventional sensor arrays

- Deflection (Y-Axis Response) of Fin 1: The orthogonal horizontal magnetic field component (B_Y) propagates through the device and exerts a lateral Lorentz force on the electrons flowing through Fin 1. Instead of flowing directly to the drain contacts, the electron cloud is pushed to one of the lateral sidewalls. This leads to a localized high current density on one side of the fin and a carrier depletion zone on the other side. The symmetric contacts (D_1 and D_2) of the sides immediately

sense this asymmetry in space and generate a non-zero ΔI_Y proportional to the applied horizontal magnetic flux.

- Fin 2 Deflection (Z-Axis Response): In this case, the cross-product results in a vertical Lorentz force when the complementary vertical magnetic field component (B_Z) enters the device. This force either pushes the electrons up towards the top gate interface, or down towards the BOX layer. The vertically offset asymmetric contacts (D_3 and D_4) on Fin 2 effectively capture this vertical charge shift, resulting in the ΔI_Z.

The 2D-MagFinFET shows a successful distinguish multi-directional magnetic vectors by assigning one fin strictly for lateral deflection and the second fin strictly for vertical deflection. This allows the device to output independent sensing simultaneously for very accurate spatial tracking.

3.6. Device Simulation and Methodology Used

To validate the theoretical framework and operational behaviour of the proposed 2D-MagFinFET, a comprehensive three-dimensional computational analysis was performed using the Synopsys Sentaurus TCAD. The overall simulation methodology was systematically divided into multiple stages using three major software modules to ensure the accurate structural modelling and detailed physical analysis. The exact three-dimensional geometry, material regions, doping distributions and the highly refined computational mesh required for the dual-parallel fin architecture were initially defined by using the SDE.

The structural design was transferred to a dynamic electrical and galvanomagnetic properties, and was carried out with the sdevice as the main physics solver. The coupled differential equations describing the carrier transport were self-consistently solved. We also incorporated several special transport models in the simulation framework to accurately model nanoscale electrostatics and magnetic interactions inside the proposed 2D-MagFinFET. The operation of the device is based on the deflection of carriers by the Lorentz force in an ultra-scaled 5 nm silicon fin. Hence, the conventional drift-diffusion transport equations were extended with additional

models to account for magnetic transport behaviour, surface scattering effects and quantum confinement phenomena.

Finally, Sentaurus Inspect was used for post-processing and visualization of the simulation results. This enabled the accurate extraction of important electrical parameters such as subthreshold transfer characteristics and multi-directional magnetic sensitivity responses.

To correctly capture the underlying solid-state physics of the proposed 2D-MagFinFET architecture, a carefully chosen set of physical models needs to be activated in the Sentaurus TCAD simulation framework. These models self-consistently solve the fundamental governing equations of the nanoscale semiconductor devices like Poisson's equation, carrier continuity equations, and Fermi-Dirac carrier statistics. To correctly capture the unique electrostatics and magnetic transport behaviour of the proposed device the conventional simulation framework was further improved by using special transport and recombination models as discussed in the following sections:

3.6.1. Drift-Diffusion Model

The basic carrier transport model in Sentaurus Device is the drift-diffusion model, which is widely used to investigate the semiconductor device functioning under stable operating conditions. In this model, the transport of carriers is governed by two main mechanisms: the drift of carriers under the action of an electric field and the diffusion of carriers due to concentration gradients.

Accordingly, the electron and hole current densities are mathematically expressed as:

$$J_n = \mu_n(n\nabla E_C - 1.5nkT\nabla lnm_n) + D_n(\nabla n - n\nabla ln\gamma_n) + \mu_n nk\left\{ln\left(\frac{n}{N_C(T)}\right) - \frac{3}{2} - ln(\gamma_n)\right\}\nabla T \quad (3.5)$$

$$J_p = \mu_p(n\nabla E_V - 1.5pkT\nabla lnm_p) + D_p(\nabla p - p\nabla ln\gamma_p) + \mu_p pk\left\{ln\left(\frac{p}{N_V(T)}\right) - \frac{3}{2} - ln(\gamma_p)\right\}\nabla T \quad (3.6)$$

The first term represents the contribution arising from the spatial variations in the electrostatic potential, electron affinity, and bandgap energy. The remaining terms

account for the effects of carrier concentration gradients as well as the spatial variation of the effective masses of electrons and holes. For Boltzmann statistics, ($\gamma_n = \gamma_{p=1}$). Finally, the last term associated with the temperature gradient ensures that a temperature difference does not generate a voltage difference or an electrical current, since thermoelectric effects are not considered in the drift-diffusion model[28].

3.6.2. Carrier Mobility Models

In typical bulk silicon devices the carrier mobility is often assumed to be a constant material property. However, in the highly confined 5 nm FinFET geometry, electrons experience frequent and severe scattering events that dramatically reduce their transport velocity. In order to correctly estimate the I_{ON} and the corresponding Hall carrier deflection, the constant mobility parameter (μ) was substituted by a complete local mobility model based on the Matthiessen rule. This approach incorporates multiple dominant scattering mechanisms for a more realistic description of carrier transport in the nanoscale device.

- Doping-Dependent Mobility (Masetti Model): Carrier scattering is dominated by ionized impurity scattering in the highly doped source and drain extension regions (Arsenic concentration is up to 5×10^{-20} cm^{-3}). There are Coulombic forces between the mobile electrons and the fixed dopant ions which greatly reduces the carrier mobility. In Sentaurus the Masetti doping-dependence model is turned on to account for this. This model calculates the degraded low-field mobility (μ_{dop}) as a function of the total local impurity concentration ($N_A + N_D$):

$$\mu_{dop} = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^{\alpha}}$$

  where μ_{max} is the lattice mobility of intrinsic silicon, μ_{min} is the saturation mobility at massive doping levels, and N_{ref} and α are empirical fitting parameters[29].

- Transverse Field and Surface Roughness (Lombardi Model): The carrier transport is localized around the silicon-dielectric (Si/SiO_2) interfaces, due to the highly confined 5 nm fin geometry of 2D-MagFinFET. The applied gate bias leads to a strong transverse electric field that confines the electrons tightly against these physical boundaries, heavily increasing surface-induced scattering. The Lombardi model is applied to reproduce this phenomenon accurately. The effective surface mobility (μ_{surf}) in this formulation is obtained by incorporating the degradation effects of acoustic phonon scattering (μ_{ac}) and surface roughness scattering (μ_{sr}) to the intrinsic bulk mobility (μ_b) using Matthiessen's rule. To accurately simulate this phenomenon the Lombardi model is implemented. This formulation calculates the effective surface mobility (μ_{surf}) by considering the degradation effects of both acoustic phonon scattering (μ_{ac}) and surface roughness scattering (μ_{sr}) in the intrinsic bulk mobility (μ_b) via Matthiessen's rule:

$$\frac{1}{\mu_{surf}} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \tag{3.7}$$

  The addition of this model is important for the 2D-MagFinFET, since ignoring the surface roughness scattering within such a strictly scaling architecture would lead to an important overestimation of the carrier drift velocity and thus would fundamentally distort the calculated Lorentz force deflection.

- High-Field Saturation (Canali Model): Although the previous models calculate the low-field mobility, (μ_{low}), they do not account for the high lateral electric fields generated by the applied 1V drain bias across the short 50 nm channel. At these high fields carriers gain large kinetic energy and emit optical phonons[29]. This leads to a saturation of their drift velocity (v_{sat}), forbidding an infinite acceleration. The Canali high field saturation model is activated in order to properly bound the electron velocity and to evaluate the final effective mobility (μ_{eff}):

$$\mu_{eff} = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low} F_{||}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{3.8}$$

where $F_{||}$ where E is the driving electric field parallel to the direction of the current flow and β is a temperature dependent exponent. This model maintains the electrostatics within a physically realistic range for the 1V operating regime.

3.6.3. Carrier Recombination and Generation Models

In order to correctly estimate the standby power consumption, SS and I_{OFF} of the 2D-MagFinFET, the simulation should take into account the continuous generation and recombination of electron-hole pairs in the semiconductor lattice. The net recombination rate (RNET) directly controls the carrier continuity equations. Two main non-radiative recombination mechanisms were explicitly modelled for this multi-gate architecture:

- Shockley-Read-Hall (SRH) Recombination: Within the 5 nm active silicon channel and particularly along the extensive high-κ dielectric interfaces, crystalline defects and impurities introduce localized energy states deep within the forbidden bandgap. These trap states facilitate phonon-assisted recombination. The SRH model is employed to calculate this defect-driven recombination rate (R_{SRH}):

$$R_{SRH} = \frac{pn - n_i^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{3.9}$$

  where p and n represent the local hole and electron concentrations, n_i is the intrinsic carrier concentration, and τ_p and τ_n are the doping-dependent minority carrier lifetimes. The terms n_1 and p_1 account for the energy level of the trap state, typically assumed to be near the intrinsic Fermi level (mid-gap). Incorporating SRH recombination is essential for the 2D-MagFinFET to accurately model the

subthreshold leakage currents that flow when the device operates in the OFF-state regime.

- Auger Recombination: While SRH dominates in the lightly doped channel, it is insufficient for modelling the heavily doped regions of the device. The source and drain extensions of the 2D-MagFinFET are heavily doped with Arsenic at a concentration of 5×10^{-20} cm^{-3}. In such highly populated regimes, Auger recombination becomes the overwhelmingly dominant carrier loss mechanism. This is a three-particle physical process where an electron and a hole recombine, but rather than emitting a photon, the excess energy is transferred as kinetic energy to a third mobile carrier (either an electron or a hole), which subsequently thermalizes back to the band edge. The Auger recombination rate (R_{Auger}) is mathematically defined as:

$$R_{Auger} = \left(C_n n + C_p p\right)(pn - n_i^2) \tag{3.10}$$

where C_n and C_p are the empirical Auger capture coefficients for electrons and holes, respectively. The activation of this model in Sentaurus Device ensures that the minority carrier lifetimes in highly degenerate source and drain contacts are not unduly prolonged, ensuring the electrostatic integrity of the simulated junctions.[27].

3.6.4. Quantum Confinement

For ultra-scaled multi-gate architectures with structural dimensions below 10 nm (such as the 5 nm fin width of the proposed 2D-MagFinFET), the classical electrostatic models alone are not sufficient to properly describe the carrier behaviour. At these length scales quantum mechanical confinement effects become relevant and lead to the splitting of continuous energy bands into discrete sub-bands and to the shifting of the centroid of the carriers away from the silicon-dielectric interface, often referred to as volume inversion.

Quantum confinement effects are typically modeled in the Synopsys Sentaurus TCAD framework using methods like the Density Gradient (DG) method or the eQuantumPotential model. However, there is an important numerical limitation in the TCAD physics solver, i.e., quantum potential models and complex magnetic transport simulations cannot be implemented at the same time. In particular, the mathematical formulation of the eQuantumPotential model is not entirely compatible with the tensor-based cross-product calculations required by the Galvanic Transport model.[27]

The activation of the Galvanic Transport model is essential since the main operating principle of the proposed 2D-MagFinFET is based on the accurate extraction of the ΔI_D at the asymmetric contacts. Thus, explicit quantum potential models were not considered in the simulation framework.[27].

To compensate the lack of direct quantum confinement modelling but yet to keep the thermodynamic accuracy high, the simulations were based on Fermi-Dirac carrier statistics instead of conventional Boltzmann approximations. The Fermi–Dirac-based approach remains highly effective in accurately evaluating the overall electrostatic and galvanomagnetic transport behaviour, even though the exclusion of quantum potential effects might cause a slight underestimation of the V_{TH} due to the lack of quantum-induced band structure modifications. This methodology provides the reliable extraction of the transverse carrier deflection and current imbalance characteristics needed to validate the multi-axis magnetic sensing capability of the proposed device.

3.6.5. Galvanic Transport Model

For studying the influence of magnetic fields on semiconductor devices the transport equations for the motion of electrons and holes have to be formulated and solved correctly. In this work the standard drift-diffusion model of carrier current densities J_n and J_p is extended by including magnetic field–dependent terms, thereby accounting for the effect of the Lorentz force on carrier transport. The magnetic field in the needed direction is included and implemented in the Sentaurus TCAD using the Galvanic Transport model[27].

$$J_{\propto} = \mu_{\propto} g_{\propto} + \mu_{\propto} \frac{1}{1+(\mu_{\propto}^{*} B)^2} [\mu_{\propto}^{*} B \times g_{\propto} + \mu_{\propto}^{*} B \times (\mu_{\propto}^{*} B \times g_{\propto})] \quad (3.11)$$

Here, α represents the carrier type in the semiconductor (n and p), J_{α} denotes the carrier current density vector, and g_{α} corresponds to the current vector in the absence of mobility effects. The term μ_{α}^{*} indicates the Hall mobility, B represents the magnetic induction vector.

3.7. Summary

In this chapter, the detailed architectural design, operating principles and computational methodology of the proposed Two-Directional Magnetic Fin Field Effect Transistor (2D-MagFinFET) are presented. To overcome the limitations of spatial sensor and the array-induced cross-talk of the conventional magnetic sensor architecture, a novel dual-parallel fin structure on the SOI substrate was proposed. The main novelty of the proposed device, the tailored asymmetric non-split drain contact configuration, was elaborated in detail. The proposed architecture by using symmetric drain contacts (D_1, D_2) on Fin 1 and vertically asymmetric contacts (D_3, D_4) on Fin 2, effectively separates the orthogonal Lorentz-force-induced carrier deflections, and thus allows for simultaneous and independent sensing of horizontal (B_Y) and vertical *(B_Z)* magnetic field components.

Additionally, in this chapter the complete 3D simulation framework for the validation of the proposed device architecture was established. We have presented a systematic description of the Synopsys Sentaurus TCAD workflow, including the geometric construction by SDE and the advanced physical analysis by sdevice. Several specialized physical models, including the Galvanomagnetic Transport model, Matthiessen's rule-based mobility degradation models (Masetti, Lombardi and Canali) and carrier recombination mechanisms such as SRH and Auger recombination models were implemented and justified to accurately capture nanoscale electrostatic and magnetic transport behaviour.

After defining the physical device architecture and the computational simulation methodology, the next chapter (Chapter 4: Simulation Results and Discussion) will

present the extracted simulation data and performance evaluation of the proposed 2D-MagFinFET. First, the zero-field DC electrical characteristics of the device will be analysed to confirm its electrostatic integrity and ultra-low-power switching performance. Then, a detailed analysis of the multi-axis galvanomagnetic response will be performed by analysing ΔI_D under different orthogonal magnetic field conditions to quantify the absolute and relative magnetic sensitivities of the proposed sensor architecture.

CHAPTER 4

ELECTRICAL CHARACTERISTICS OF 2D-MagFinFET

4.1. Introduction

Following the establishment of the structural architecture and computational methodology in Chapter 3, this chapter presents the baseline simulation results and performance evaluation of the proposed 2D-MagFinFET. Although the primary objective of the device is multi-axis magnetic field sensing, the proposed architecture fundamentally operates as a highly scaled semiconductor device and must therefore demonstrate strong electrical performance characteristics. Accordingly, this chapter focuses on evaluating the zero-field electrostatic integrity of the dual-parallel fin structure to verify its operation as an efficient ultra-low-power semiconductor Important DC electrical parameters, including SS, V_{TH}, DIBL, and SR, are extracted from the transfer and output characteristics to examine the electrostatic stability and

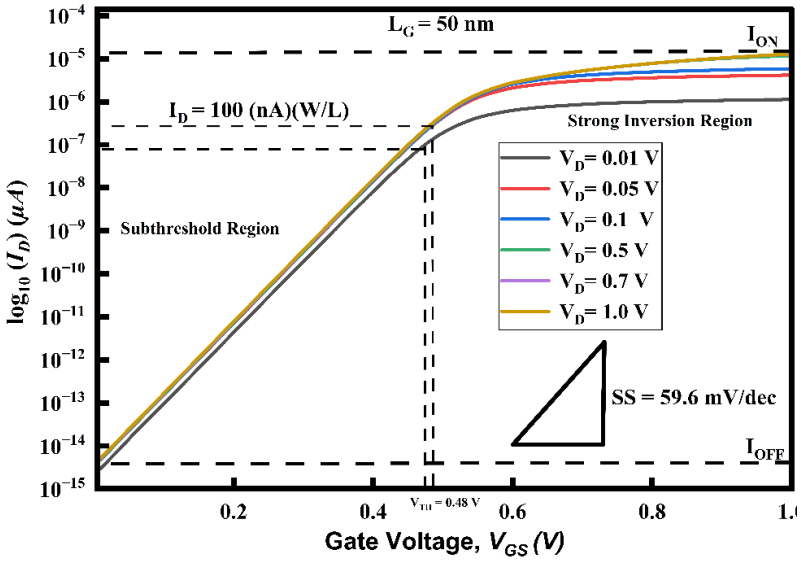
switching efficiency of the device. Furthermore, a systematic parametric analysis of gate-length variation is presented to evaluate the structural robustness of the proposed design and to investigate the fundamental trade-offs between aggressive dimensional scaling and electrostatic integrity. The detailed investigation of the multi-axis galvanomagnetic response of the proposed sensor particularly the analysis of ΔI_D under varying orthogonal magnetic field conditions to evaluate its spatial tracking capability be presented systematically in the following chapter.

4.2. Electrical Characteristics

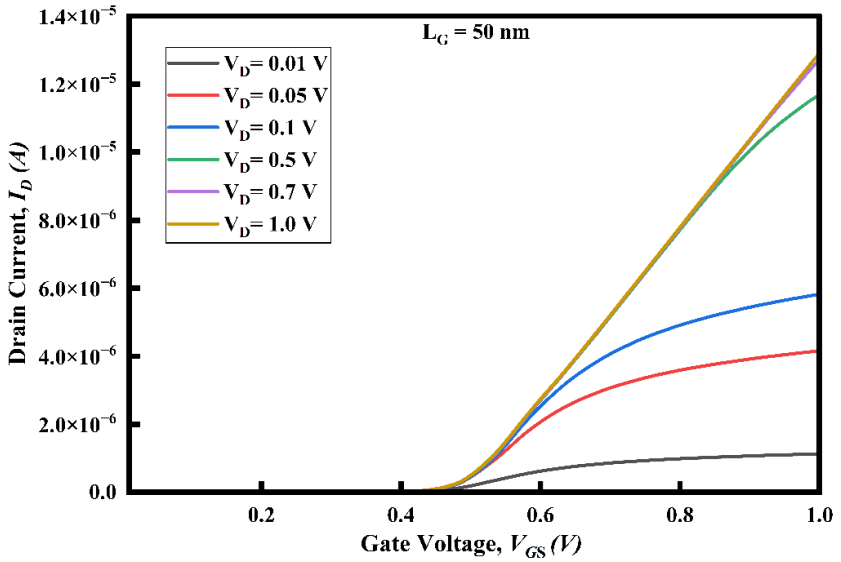
Before analysing the galvanomagnetic sensing performance of the proposed device, it is essential to first evaluate the baseline electrostatic characteristics of the 2D-MagFinFET. Since the operation of a magnetic sensor depends heavily on a stable and well-controlled baseline current, the presence of severe SCE or excessive subthreshold leakage can significantly degrade the Signal-to-Noise Ratio (SNR) of the magnetic response. Therefore, the device was initially simulated under zero magnetic field conditions (B = 0 T) to validate its functionality as a highly scaled and ultra-low-power FinFET device.

4.3. Transfer Characteristics and Gate-Length Scaling (I_D-V_{GS})

Figure 4.1 Transfer characteristics of the proposed 2D-MagFinFET obtained by using Quasistationary Sweep simulation technique. Instead of using one analytical equation, this approach uses a detailed numerical solving method. In the simulation, the drain vo) is kept constant at 1.0 V and the V_{GS} gradually sweeps from 0.0 V to the supply voltage of 1.0 V. The simulator solves the coupled semiconductor transport equations including Poisson's equation and the carrier continuity equations simultaneously at each incremental V_{GS} step until stable numerical convergence is achieved. This systematic process well describes the formation of the conductive channel and the corresponding change of the drain current under the control of the gate and thus the key electrostatic parameters such as V_{TH} and SS can be accurately extracted.



(a)



(b)

Figure 4.1. Transfer Characteristics (a) log scale of I_{DS}-V_{GS} and (b) I_{DS}-V_{GS} of 2D-MagFinFET

The obtained I_{DS}-V_{GS} characteristics are analysed under two important operating regions:

4.3.1. Subthreshold Region ($V_{GS} < V_{TH}$)

From the logarithmic scale, it is observed that the drain current increases exponentially with the increase in VGS. The sharp linear behaviour in this region confirms the strong electrostatic control of the ultra-thin fin channel by the HKMG stack, which suppresses the leakage currents at the subsurface.

4.3.2. Strong Inversion Region ($V_{GS} > V_{TH}$)

A strong volume inversion layer is formed in the dual-fin structure when VGS is larger than the threshold voltage. The characteristics on the linear scale show a smooth increase of the drive current with no sign of any series resistance effects indicating that the heavily doped source and drain extensions are able to inject charge carriers into the channel.

4.4. Short-Channel Effect (SCE) and Switching Analysis

To quantitatively evaluate the electrostatic robustness of the proposed 2D-MagFinFET at the 50 nm gate-length node, the important short-channel parameters were extracted from the simulated transfer characteristics shown in Figure 6. The importance of evaluating these parameters arises because any degradation in electrostatic control could result in baseline current instability, which would severely reduce the signal-to-noise ratio during magnetic field sensing operations.

4.4.1. Subthreshold Swing (SS):

The Subthreshold Swing is defined as the change in gate-to-source voltage required to increase the drain current by one decade (an order of magnitude) within the subthreshold operating region. It acts as a direct measure of the transistor's switching

efficiency and reveals how abruptly the device can transition from the OFF state to the ON state.

The proposed device exhibits an excellent SS value of 59.96 mV/dec. This is a very efficient value, close to the theoretical ideal room temperature thermionic emission limit of 60 mV/dec. The SS of this device is much better than that of conventional structures due to the use of a specialized HKMG stack with HfO_2. This gate stack combined with the ultra-thin 5 nm fin geometry provides superior electrostatic capacitive coupling. The channel is fully controlled by the gate, reducing leakage paths and enabling a near-perfect sharp transition between the OFF and the ON state.

4.4.2. Threshold Voltage (V_{TH}) and Roll-Off:

The Threshold Voltage is essentially the minimum voltage between the gate and source needed to invert the surface of the semiconductor and create a continuous channel of conduction between the source and drain. It actively determines the exact voltage level at which the device turns ON. The threshold voltage was extracted to be exactly 0.48 V by constant-current extraction method from the transfer characteristics of Figure 6. This is a very optimum value for a sensitive magnetic sensor. This threshold of 0.48 V is 128.57% higher when compared to the previously reported baseline FinFET devices with a low V_{TH} of 0.21 V. This higher value is very useful as it prevents the device from accidentally going ON due to thermal noise or small voltage fluctuations. In addition, the dual-fin structure and 30 nm BOX layer suppress the threshold voltage roll-off by providing strong control of the gate on the channel potential and avoiding premature barrier degradation.

4.4.3. Drain-Induced Barrier Lowering (DIBL):

DIBL is an important short-channel effect that occurs when the electric field from the drain region penetrates into the channel and reduces the source-to-channel potential barrier. It reflects how strongly the transistor can maintain stable channel control against variations in drain voltage. DIBL is determined from the change of V_{TH} with drain bias and can be mathematically expressed as [3]

$$\text{DIBL} = \frac{\Delta V_{TH}}{\Delta V_{DS}} = \frac{V_{TH}(V_{DS,low}) - V_{TH}(V_{DS,high})}{V_{DS,high} - V_{DS,low}} \quad (4.1)$$

The proposed 2D-MagFinFET exhibits a very low DIBL value of 8.23 mV/V. The very low DIBL confirms the strong electrostatic screening of the ultra-thin 5 nm fin structure. The narrow fin geometry gives excellent channel shielding and very little penetration of the drain field into the source-channel region in the multi-gate structure. Therefore, the operating current of the baseline is very stable even with the variation of the drain voltage. This stability is especially important for magnetic sensing applications where any stray electrical fluctuation could be mistaken for a magnetic sensing signal.

4.4.4. Switching Ratio (SR):

The Switching Ratio or ON/OFF current ratio is the ratio of the maximum drive current (I_{ON}) when the transistor is fully turned ON to the standby I_{OFF} when the transistor is turned OFF. It is the ultimate measure of the device's digital switching capability, power efficiency and overall electrostatic integrity.

The I_{ON} is measured at exactly 12.9 µA, while the I_{OFF} is strongly suppressed to an ultra-low level of 5.24 fA (femtoamperes). This results in an excellent digital switching ratio of about 2×10^9. This very high ratio is obtained because the multi-gate geometry aggressively depletes the entire 5 nm fin in the OFF state, and the 30 nm BOX layer provides a strict physical barrier that completely eliminates deep-substrate leakage paths. Importantly, the extracted ON-current of 12.9 µA is strictly within the ultra-low power operating range of 1 µA to 100 µA. This low power validation validates that the device meets the strict requirements of thermal dissipation and safety for continuous operation within biomedical micro-robot applications.

4.5. Output Characteristics (I_D-V_{DS})

The output characteristics describe the relationship between the I_{DS} and the V_D at different constant V_{GS} conditions. This analysis is important for evaluating carrier transport efficiency, velocity saturation effects, and channel-length modulation in the proposed 2D-MagFinFET. As shown in Figure 5, the I_D-V_{DS} characteristics were

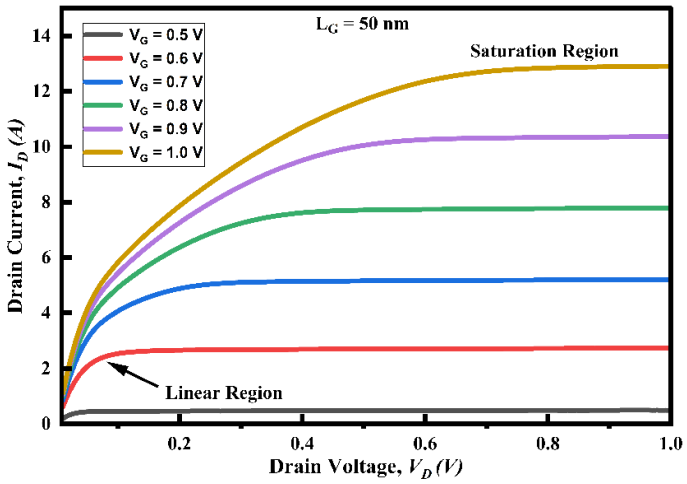


Figure 4.2. Output Characteristics of device

obtained by sweeping the drain voltage from 0.0 V to 1.0 V, while maintaining the V_{GS} at fixed values ranging from 0.5 V to 1.0 V with an increment of 0.1 V. The output characteristics can generally be divided into two major operating regions which are shown in the Figure 4.2.

4.5.1. Linear (Ohmic) Region:

At lower drain voltage conditions ($V_{DS} < V - V_{TH}$), the channel behaves like a voltage-controlled resistor. In this region, the drain current increases linearly with the applied drain voltage because the electric field remains nearly uniform throughout the channel and the carrier mobility is relatively unaffected.

In this operating region, the curves shown in Figure 5 display a strong linear increase in drain current. The steep slope confirms efficient carrier transport and indicates that

the heavily doped source and drain extensions (5×10^{-20} cm^{-3} Arsenic doping) introduce very low parasitic series resistance.

4.5.2. Saturation Region:

If the drain–source voltage VDS exceeds the pinch-off condition ($V_{DS} \geq V_{GS} - V_{TH}$), the lateral electric field inside the channel is very high. In this situation, the carriers reach their maximum drift velocity, causing velocity saturation, and the drain current becomes independent of further increase in V_{DS}.

The proposed device shows very stable and well-defined saturation regions for all VGS conditions. It is of particular importance that the saturation curves are flat. This is a sign that the channel-length modulation effects are effectively suppressed by the three-dimensional multi-gate architecture. This means that the depletion region near the drain does not substantially shorten the effective channel length during operation.

Importance for Magnetic Sensing: Achieving a stable and nearly flat saturation current is extremely important for the operation of the 2D-MagFinFET as a magnetic sensor. Since the sensing mechanism depends on detecting very small ΔI_D generated by Lorentz-force-induced carrier deflection, the baseline drain current must remain highly stable. Any noticeable slope in the saturation region would allow drain voltage fluctuations to introduce unwanted current variations, generating electrical noise that could interfere with or mask the actual magnetic sensing signal.

4.6. Analog Performance Metrics (Transconductance and Output Conductance)

While the previously extracted parameters confirm the device as an efficient ultra-low-power digital switch, a magnetic sensor fundamentally operates as an analog transducer. The ΔI_D generated by the Lorentz force must remain stable and easily detectable. Therefore, evaluating the analog amplification capability of the proposed

2D-MagFinFET is essential through the extraction of Transconductance (g_m) and Output Conductance (g_d).

4.6.1. Transconductance (g_m):

g_m is defined as the first derivative of the drain current with respect to the V_{GS} and is mathematically represented as $g_m = \partial I_D/\partial V_{GS}$ at a constant V_{DS}. voltage. It indicates how effectively the channel current responds to variations in the gate voltage and reflects the intrinsic amplification capability of the transistor.

As illustrated in Figure 4.3., the proposed 2D-MagFinFET demonstrates a peak transconductance of approximately 25.92 µS. This high g_m value is primarily attributed to the ultra-thin 0.5 nm interfacial oxide layer together with the 2 nm HfO2 high-κ gate dielectric, which collectively enhance the gate-to-channel capacitance (C_{OX}) and strengthen electrostatic gate control over the channel region. A high transconductance is particularly advantageous for magnetic sensing applications because it allows even small variations in channel potential, such as the transverse Hall voltage induced by an external magnetic field, to be efficiently amplified into measurable ΔI_D. As a result, the absolute magnetic sensitivity of the proposed sensor is significantly improved.

4.6.2. Output Conductance (g_d):

Output conductance is defined as the first derivative of the drain current with respect to the drain-to-source voltage and is mathematically represented as $g_d = \partial I_D/\partial V_{DS}$ while the device operates in the saturation region. It is the inverse of the output resistance (R_{OUT}) and serves as an important parameter for evaluating channel-length modulation effects. As shown in Figure 4.4., the extracted output conductance of the proposed device is extremely low, rapidly decreasing and stabilizing near 0 µS once the device enters the deep saturation region. In an ideal long-channel transistor, g_d ideally approaches zero under saturation conditions. For aggressively scaled nanoscale

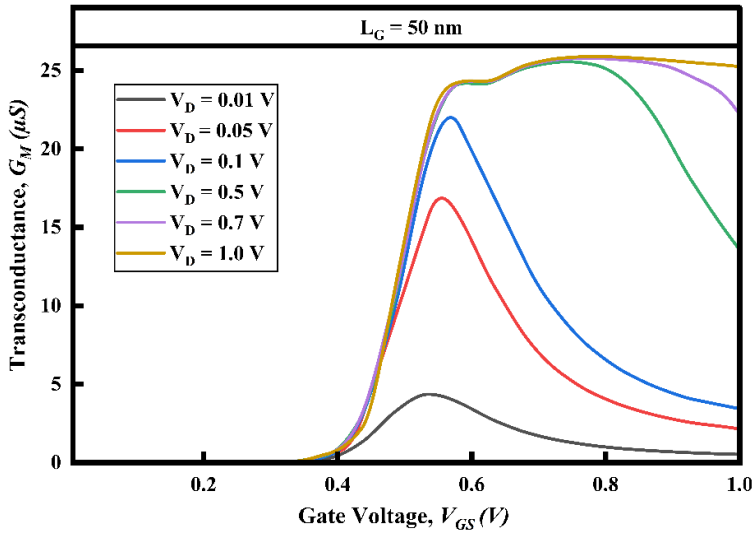


Figure 4.3. Transconductance g_m versus V_{GS} at gate length 50nm

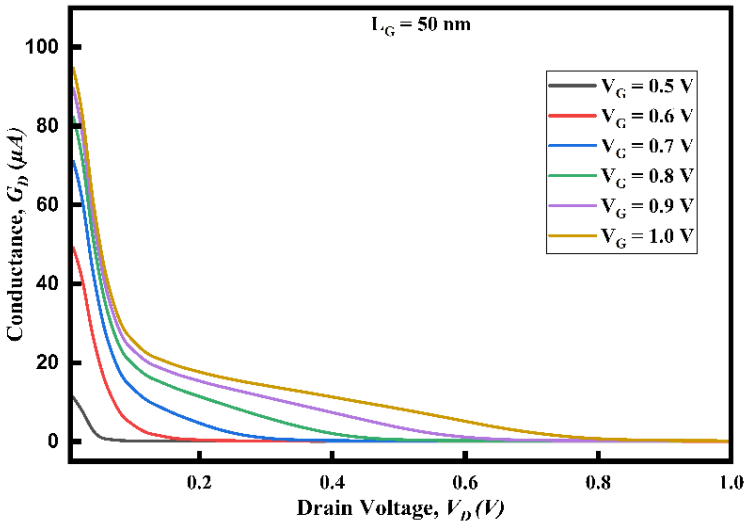


Figure 4.4. Conductance G_D versus V_{GS} at gate length 50nm

devices such as the proposed 50 nm FinFET, a low g_d value confirms that the multi-gate architecture effectively suppresses drain-induced channel shortening by limiting the excessive expansion of the drain depletion region into the channel.

Importance for Magnetic Sensing: Maintaining a very low output conductance is one of the most critical requirements for a current-mode magnetic sensor. A low g_d ensures that the saturation current remains highly stable and unaffected by small drain voltage fluctuations. This stable baseline operation guarantees that the extracted ΔI_D originates purely from Lorentz-force-induced carrier deflection, minimizing electrical noise and preserving the independent sensing capability of both the Y-axis and Z-axis detection channels.

4.7. Gate Length (L_G) impact on Device Performance

In order to comprehensively assess the robustness and scalability of the proposed 2D-MagFinFET architecture, a systematic parametric analysis was performed by varying the L_G. Modern semiconductor technology is moving aggressively scaled sub-20 nm nodes for higher integration density. The proposed device was simulated with multiple gate lengths from 50 nm down to 10 nm.

. The extracted zero-field electrostatic parameters, which highlight the fundamental trade-offs between aggressive dimensional scaling and electrostatic integrity, are summarized in Table 5.2, while the corresponding graphical trends of these parameters are illustrated in Figure 4.5, 4.6 and 4.7.

4.7.1. Subthreshold Swing (SS) Degradation

SS is an important parameter that reflects how efficiently a transistor switches between the OFF and ON states. As observed from the extracted results Figure 4.5., reducing the gate length from 50 nm toward the aggressively scaled 10 nm regime leads to a noticeable degradation in this parameter. The SS gradually increases from a near-ideal value of 59.97 mV/dec at 50 nm to 63.39 mV/dec at 10 nm. This increasing trend

clearly indicates a gradual weakening of electrostatic gate control over the channel carriers as the device dimensions continue to scale down.

TABLE 4.1. Variation of V_{TH}, SS, I_{OFF} and S_R along with variation of L_G

Gate Length (L_G) nm	**Threshold Voltage (V_{TH}) V**	**Subthreshold Swing (SS) mV/dec**	**OFF-Current (I_{OFF}) femtoAmpere (fA)**	**Switching Ratio (S_R)**
50	0.485	59.97	5.24	2.46×10^9
40	0.503	60.08	6.06	1.12×10^9
30	0.498	60.47	7.44	5.42×10^9
20	0.484	60.89	10.60	2.46×10^8
10	0.478	63.39	28.09	6.24×10^7

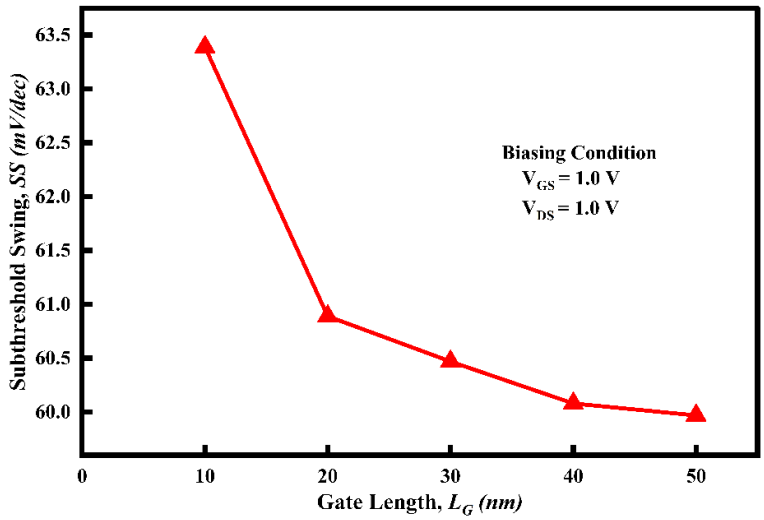


Figure 4.5. *SS* variation with variation in L_G

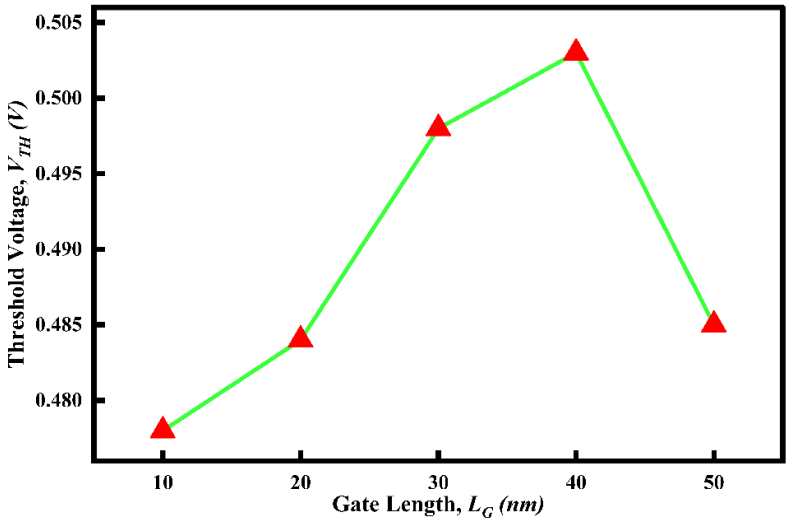


Figure 4.6. V_{TH} variation with variation in L_G

4.7.2. Threshold Voltage (V_{TH}) Roll-off

At the same time, gate-length scaling also produces a significant effect on the V_{TH}. The device maintains a relatively strong V_{TH} of 0.485 V at the 50 nm node, with a slight improvement observed at 40 nm. However, as the gate length is further reduced, a noticeable threshold voltage roll-off begins to appear, with V_{TH} decreasing to 0.478 V at the 10 nm node.

This behaviour is a well-known characteristic of DIBL, where the close proximity of the drain region begins to electrostatically influence the source-channel potential barrier, thereby increasing the likelihood of unintended device turn-on.

4.7.3. Switching Ratio (SR) Variation

Most importantly, the combined reduction in electrostatic gate control together with the increasing influence of DIBL results in a significant rise in static leakage current. The I_{OFF} increases from an extremely low 5.24 fA at the 50 nm node to 28.09 fA at the 10 nm node. As a consequence, the SR decreases by nearly two orders of magnitude, dropping from an exceptional value of approximately 2.46×10^9 to nearly 6.24×10^7. However, despite these expected short-channel limitations at aggressively scaled dim-

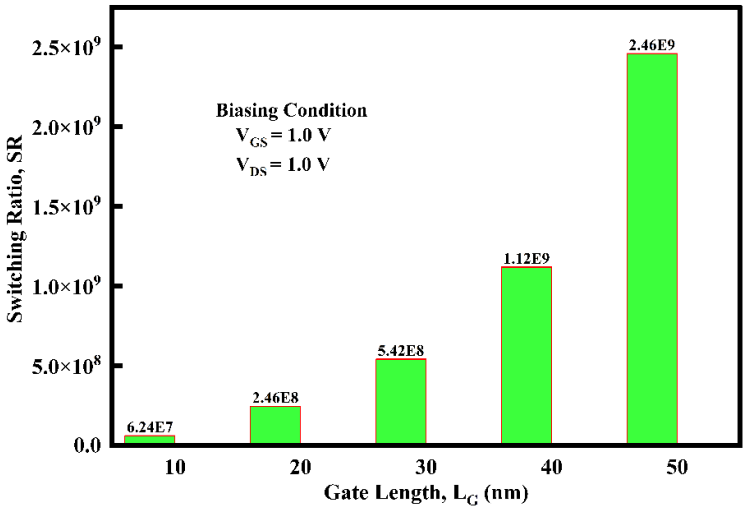


Figure 4.7. *Bar graph of increasing SR* with variation in L_G

ensions, the dual-parallel ultra-thin fin architecture continues to maintain a practically acceptable switching ratio even at the 10 nm node, highlighting the strong geometric robustness and scalability of the proposed device design.

4.7.4. Optical Gate Length Conclusion

While scaling the proposed 2D-MagFinFET toward sub-20 nm technology nodes enables extremely high integration density, the parametric analysis clearly highlights the associated physical trade-offs. The aggressively scaled shorter channel lengths (10 nm and 20 nm) noticeably degrade the zero-field electrostatic integrity of the device by worsening the SS and significantly reducing the S_R.

4.8. Summary

This chapter systematically evaluated the zero-field electrostatic behaviour and baseline analog performance of the proposed 2D-MagFinFET. Before operating as a highly sensitive magnetic sensor, the device must first demonstrate stable and low-noise semiconductor switching characteristics. Through detailed 3D TCAD simulations, it was confirmed that the dual-parallel fin architecture, supported by the

HKMG stack and the 30 nm BOX layer, effectively suppresses severe SCE even at aggressively scaled dimensions. To further validate the structural robustness of the device, a systematic parametric analysis of L_G scaling down to 10 nm from 50 nm was performed, confirming the 50 nm node as the optimum physical dimension for maintaining a balance between strong electrostatic control and sufficient active magnetic sensing volume.

The extracted transfer characteristics of optimized 50 nm structure showed a near ideal SS of 59.97 mV/dec and stable V_{TH} of 0.485 V. Moreover, the proposed architecture presents a very low DIBL (8.23 mV/V) and g_m (25.92 μS) value, which indicates strong resistance for the drain-field penetration and superior intrinsic signal amplification ability. Together with an excellent SR of 2.46×10^9, these results prove that the device successfully operates in the ultra-low-power range between 1 and 100 μA, which is required for biomedical micro-robot applications.

Establishing such a stable baseline current is extremely important for current-mode magnetic sensing applications. Since the sensing mechanism depends on detecting extremely small ΔI_D generated by external magnetic fields, any electrical instability in the baseline current would introduce unwanted noise and reduce sensing accuracy. Having validated the strong electrostatic integrity, optimized dimensional scaling, and stable electrical performance of the proposed 2D-MagFinFET, the next chapter focuses on the active galvanomagnetic behaviour of the device.

CHAPTER 5

MAGNETIC RESPONSE

5.1. Introduction

In the previous chapter, the zero-field electrical characteristics of the proposed 2D-MagFinFET have been analysed and discussed thoroughly. On this ground, the current chapter aims to investigate the active magnetic response of the device, with particular attention to its multi-axis sensing capability and comparative performance with existing magnetic sensor architectures. The proposed dual-parallel fin structure is specially designed for independent detection of orthogonal magnetic field components, which distinguishes from the conventional solid-state magnetic sensors (e.g., bulk Hall plates and single-fin MAGFETs) that are generally limited to single-axis magnetic field detection. In this chapter, therefore, the galvanomagnetic transport behaviour of the device is investigated under different magnetic field conditions, its absolute and relative magnetic sensitivities are estimated and its structural immunity against cross-axis interference and cross-talk effects is verified.

5.2. Measurement Methodology and Biasing Conditions

To evaluate the spatial sensing capability of the proposed 2D-MagFinFET, specific physical models and customized structural configurations were incorporated into the simulation framework. As discussed earlier in the simulation methodology of Chapter 2 (Section 2.5.2), the magnetic response of the device is governed by the Galvanomagnetic Transport model within the Sentaurus TCAD environment. This

model self-consistently integrates the Lorentz force into the conventional carrier continuity and drift-diffusion transport equations. In addition, accurate extraction of the resulting spatial charge imbalance requires the customized asymmetric split-drain architecture described in Chapter 3 (Section 3.5), where Fin 1 employs symmetric lateral drain contacts (D_1, D_2), while Fin 2 utilizes vertically positioned area-scaled contacts (D_3, D_4).

5.2.1. Biasing Strategy

At the very small 50 nm Lg of the proposed device, it is important to reduce the effect of electrostatic channel length modulation and thermal noise to get a pure magnetic sensing response. However, at nanoscale dimensions a conventional constant drain voltage application can induce strong drain-field penetration, giving rise to electrical fluctuations that may mask the very small carrier deflections induced by the magnetic field. This problem is overcome by deliberately operating the device in a constant current bias configuration. During the entire simulation the I_D is fixed to 100 µA. The ultra-low bias current is chosen to ensure stable electrostatic operation of the short 50 nm channel and to meet the stringent thermal and power constraints of the biomedical micro-robotic applications. Under this stable operating condition, the external magnetic field is swept in a gradual manner from -0.5 T to +0.5 T in discrete steps of 0.1 T.

5.2.2. The Lorentz Force Deflection Mechanism

The operating principle of the proposed 2D-MagFinFET is based on the Galvanomagnetic transport mechanism, which is governed by the Lorentz force equation:

$$F_L = -q(v \times B) \tag{5.1}$$

where -q represents the elementary charge of an electron, (v) denotes the carrier drift velocity vector, and (B) represents the externally applied magnetic field vector[30]. In the proposed device structure, the primary electron transport occurs along the longitudinal channel direction, defined as the X-axis (V_x). Since the Lorentz force acts

perpendicular to both the carrier velocity vector and the applied magnetic field vector, the introduction of a transverse magnetic field generates an orthogonal force that redistributes the moving charge carriers within the silicon fins. This carrier redistribution mechanism forms the basis of the dual-axis magnetic sensing capability of the proposed architecture.

(a) Y-Axis Deflection Mechanism:

Applying an external magnetic field in the vertical direction (B_Z) results in a Lorentz force on charge carriers in the Y-direction via the vector cross-product ($V_y \times B_Z$). The electrons are pushed horizontally across the narrow 5 nm fin width . This transverse carrier motion causes electrons to accumulate near one sidewall of the fin and a decrease in carrier concentration near the other sidewall. As a result, the symmetric lateral drain contacts (D_1 and D_2) experience a measurable current imbalance. The drain current increases at the carrier accumulation side and decreases at the opposite side, producing a horizontal differential current represented as ($\Delta I_Y = I_{D1} - I_{D2}$). =

(b) Z-Axis Deflection Mechanism:

Also, when an external magnetic field is applied along the horizontal direction (BY), the vector cross-product ($V_z \; x \; B_Y$) generates a Lorentz force along the vertical Z-direction. In Fin 2, electrons act as carriers, being deflected upwards to the top gate interface or downwards to the Buried Oxide (BOX) layer, depending on the polarity of the magnetic field applied. The vertical carrier imbalance leads to the current imbalance between the drain contacts in a vertical position (D_3 and D_4). This leads to a vertical differential current generation that is expressed as ($\Delta I_Z = I_{D3} - I_{D4}$).

(c) X-Axis no active deflection mechanism:

Importantly, the vector cross-product is zero under the application of a magnetic field along the direction of carrier transport (B_X) ($V_x \times B_X = 0$). Under this condition the electrons are not deflected by the Lorentz force and thus no charge imbalance is created in the space between the fins. This basic physical behaviour ensures that the proposed

device is only sensitive to the transverse magnetic field component, providing the basis for extracting independent orthogonal differential current signals. The following sections discuss quantitative evaluation of these magnetic sensitivities.

5.3. Evaluation of Multi-Axis Magnetic Sensitivity

For quantitative evaluation of the proposed 2D-MagFinFET's performance as a spatial tracking sensor, the differential currents resulting from the Lorentz-force-induced carrier deflection must be transformed into the standardized sensitivity parameters. The galvanomagnetic device performance in terms of sensing is characterized mainly by two parameters: Absolute Sensitivity and Relative Sensitivity.

For all subsequent sensitivity calculations, the device was operated under a constant steady-state bias current (I_D) of 100μA, whilst the applied magnetic field (B) was linearly swept across the defined measurement range.

5.3.1. Absolute Magnetic Sensitivity (S_A):

The absolute sensitivity is defined as the $\Delta \boldsymbol{I}$ generated for a unit variation of the applied external magnetic field (B). It is the direct electrical output response of sensor and is obtained from the slope of magnetic response characteristics. S_A is calculated using (5.2)[31].

$$\boldsymbol{S_A} = \left|\frac{\Delta \boldsymbol{I}}{\Delta \boldsymbol{B}}\right| \tag{5.2}$$

5.3.2. Relative Magnetic Sensitivity (S_R):

Relative sensitivity is defined as the absolute sensitivity normalized to the I_D flowing through the device. This parameter is particularly important when comparing the efficiency of different magnetic sensor designs. This measures the efficiency of the sensor to convert a low power electrical signal into a magnetic output that can be detected. The SR of the device is evaluated by (5.3)[32].

$$S_R = \frac{S_A}{I_D . B} \tag{5.3}$$

5.4. Y-Direction Magnetic Response and Sensitivity Analysis

The magnetic response of the proposed 2D-MagFinFET in the Y-direction is mainly dictated by the geometric structure of Fin 1. To evaluate this spatial sensing capability accurately without electrostatic noise or the effect of channel-length modulation, the device with a highly scaled 50 nm gate length is operated at a steady state of constant ID of 100 uA. The external magnetic field is applied only in the orthogonal Z-direction (B_Z) and is linearly swept from -0.5 T to 0.5 T in discrete steps of 0.1 T during the simulation. Under these controlled biasing conditions, the electrons flowing through the channel are subject to a lateral Lorentz force that physically deflects the electrons along the Y-direction towards the symmetrically positioned lateral drain contacts D_1 and D_2.

This localized carrier deflection gives arise to a measurable current imbalance, which is continuously extracted as the horizontal differential current represented by $\Delta I_Y = I_{D1} - I_{D2}$. From Figure 6 it is evident that the differential current is a linearly dependent on the applied magnetic field throughout the complete simulation.

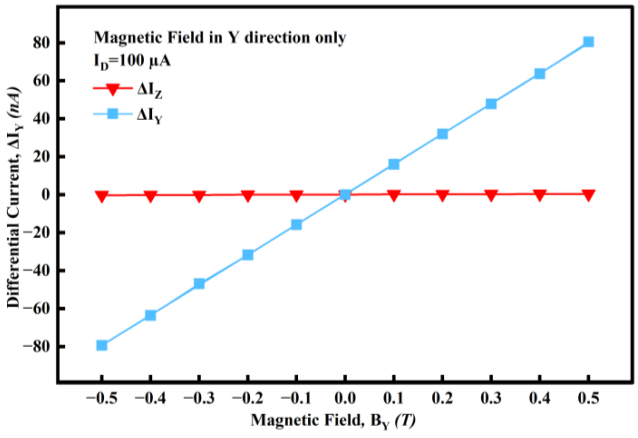


Figure 5.1. Magnetic Response for Y-direction only

By extracting the slope of this linear response curve, the absolute magnetic sensitivity of the device along the Y-direction is calculated to be 159.27 nA/T. Furthermore, to evaluate the overall efficiency of the sensor, this absolute sensitivity is normalized with respect to the operating bias current, resulting in a relative magnetic sensitivity (SR) of 0.0159 T^{-1}. These results confirm that the strong 5 nm carrier confinement of Fin 1, combined with the ultra-low constant current biasing condition, effectively captures the lateral carrier redistribution required for high-resolution spatial magnetic sensing and tracking applications.

5.5. Z-Direction Magnetic Response and Sensitivity Analysis

The Z-direction magnetic response, which enables the proposed 2D-MagFinFET to achieve true multi-axis spatial tracking capability, is governed exclusively by Fin 2 and its customized

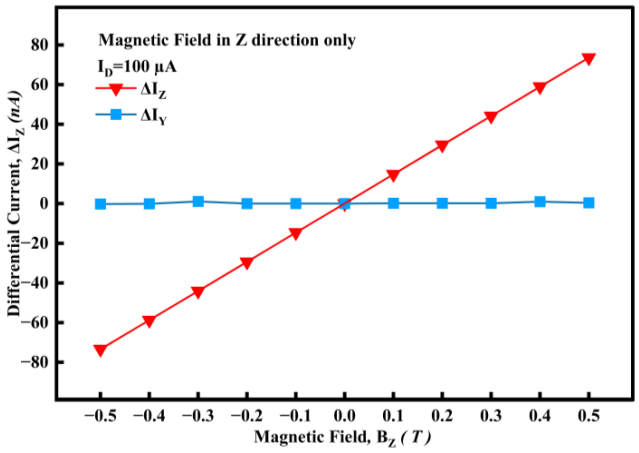


Figure 5.2. Magnetic Response for Z-direction only

asymmetric contact configuration. Consistent with the previous analysis, the device with a highly scaled 50 nm gate length is operated under the same steady-state constant bias current of 100 µA to maintain baseline stability and suppress electrostatic interference effects. During this evaluation, the external magnetic field is applied along

the orthogonal Y-direction (BY) and linearly swept from −0.5 T to 0.5 T in discrete increments of 0.1 T. Under these operating conditions, the Lorentz-force vector cross-product drives the moving electrons vertically along the Z-direction, forcing them either toward the top gate interface or downward toward the Buried Oxide (BOX) layer depending on the polarity of the applied magnetic field.

This vertical redistribution of carriers creates a measurable spatial charge imbalance that cannot be correctly captured with conventional symmetric drain contacts. Instead, the vertically offset D_3 and D_4 successfully detect the imbalance. This imbalance gives rise to a vertical $\Delta I_Z = I_{D3} - I_{D4}$. The measured ΔI_Z response shows a very linear relationship with the applied magnetic field in the whole range of tested values, as illustrated in Figure 7. The absolute magnetic sensitivity along the Z-direction is calculated to be 147.13 nA/T by taking the slope of this response curve. In addition, normalizing this to the constant bias current of 100 \mu A gives a S_R of 0.0147 T^{-1}.

These results strongly confirm the effectiveness of the proposed asymmetric drain-contact engineering. Importantly, the purposely scaled area of the bottom contact (D_4) compensates well the carrier scattering and charge accumulation effects around the silicon–BOX interface, thus allowing stable and high-resolution vertical magnetic sensing performance.

5.6. Multi-Axis Resolution and Orthogonal Independence

The most significant advantage of the proposed 2D-MagFinFET architecture is its capability to perform simultaneous multi-axis magnetic sensing without experiencing structural cross-talk. In practical biomedical environments, magnetic fields are rarely aligned along a single ideal axis. Therefore, an efficient spatial tracking sensor must be capable of resolving complex three-dimensional magnetic field vectors into their independent orthogonal components.

5.6.1. Simultaneous Multi-Vector Tracking

To test this capability, the device was subjected to magnetic fields applied in the Y and Z directions together. Both Fin 1 and Fin 2 are actively involved under these simultaneous external forces. The device is able to isolate complex magnetic vector, as illustrated in Figure 5.3, where each fin exhibits the same linear magnetic response and sensitivity (159.27 nA/T for Fin 1 and 147.13 nA/T for Fin 2) as found during individual, single-axis testing. The readout circuitry can easily discriminate the active fin by sensing the different absolute sensitivities of the two axes and thus successfully determine the specific orientation of the applied magnetic field.

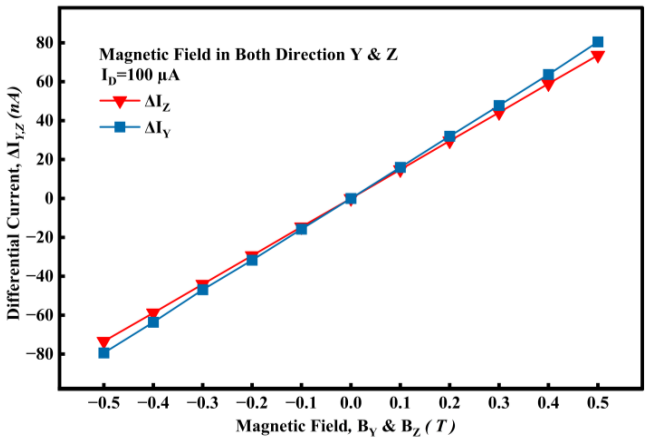


Figure 5.3. Magnetic Response for Both directions together

5.6.2. Structural Cross-Talk Suppression

The simultaneous operation of these individual sensitivities clearly shows the structural immunity of the dual-parallel fin architecture against cross-axis interference. The physical distance between the fins is only 11 nm, but the strong electrical isolation provided by the SOI substrate decouples the galvanomagnetic transport behaviour of the two sensing channels. For the magnetic field in the Y-direction, the lateral differential current in Fin 1 (ΔI_Y) is essentially zero and only the vertical charge distribution in Fin 2 is affected. Similarly, magnetic field applied along Z-direction modulates only the horizontal charge distribution in Fin 1, while the vertical differential current in Fin 2 (ΔI_Z) does not show any measurable deflection.

5.6.3. Longitudinal (X-Axis) Magnetic Immunity

Significantly, the proposed device also shows complete immunity to magnetic interference in the direction of carrier transport. When the magnetic field is applied parallel to the longitudinal channel axis (B_X), the carrier velocity vector aligns with the magnetic field vector and the Lorentz-force cross-product mathematically becomes zero. In this condition the moving electrons are not deflected by the Lorentz force and thus no spatial charge imbalance is created in either fin. This fundamental physical property guarantees the proposed 2D-MagFinFET responds solely to the transverse magnetic field components, which strongly validates its potential to be used as a highly precise and ultra-low-power magnetic sensing platform for biomedical micro-robotic navigation systems.

5.7. Performance Benchmarking and Comparative Analysis

To quantitatively evaluate the architectural and operational benefits of the proposed 2D-MagFinFET, we compared its zero-field electrical performance and active magnetic sensing characteristics with that of a state-of-the-art conventional MAGFinFET structure. The S_R was chosen as the key comparison metric to accurately evaluate their real electromagnetic sensing efficiency because the two architectures have fundamentally different structural configuration and biasing conditions. Furthermore, both devices were simulated under the same 50 nm gate length condition to allow a fair and rigorous comparison.

5.7.1. Baseline MAGFinFET Characteristics and Limitations

The baseline MAGFinFET as a conventional solid-state magnetic sensing architecture is designed with a single-channel configuration, which naturally limits its sensing capability to the magnetic fields applied only along the Z-direction. From the electro-static point of view, the baseline device shows a V_{TH} of 0.21 V and I_{OFF} of 50.53 pA. The device shows a relatively high S_A of 181.6 nA/T, but the response is strongly

dependent on a large driving current, requiring a constant bias current of 1 mA to generate a measurable differential output signal. This high biasing requirement is a major operational limitation for biomedical micro-robotic navigation systems that need strict thermal safety and ultra-low-power operation.

The real electromagnetic efficiency of magnetic sensors in different power operating conditions should be fairly evaluated by normalizing the absolute sensitivity with respect to the applied bias current. This normalized parameter, called relative S_R, enables a more reliable comparison between different sensor architectures. Due to its high 1 mA operating current requirement, the conventional MAGFinFET achieves a relatively low S_R value of only 0.001 T^{-1}, while still remaining limited to single-axis sensing functionality.

TABLE 5.1. Comparative performance analysis of the proposed 2D-MagFinFET

Parameter	MAGFinFET [33]	2D-MagFinFET [This work]	Improvement
V_{TH}	0.21V	0.48 V	128.57 % increses
***SS* (mV/dec) at L_G = 50 nm**	63	59.96	4.83 % reduction
I_{OFF}	50.53 pA	5.24 fA	99.99 % reduction
I_{ON}	62.13 µA	12.9 µA	79.24 % reduction
SR	1.22×10^6	2.39×10^9	1959 times increase
Magnetic Sensitivity S_A	181.6 nA/T in Z-direction (I_D = 1mA)	147.13 nA/T in Z-direction and 159.27 nA/T in Y-direction (I_D = 100 µA)	Orthogonal sensing capability
Magnetic Sensing	Only in Z-direction	In orthogonal directions (Y and Z)	Dual-axis Independent sensing

On the other hand, the proposed 2D-MagFinFET takes advantage of the improved carrier confinement from the dual-parallel ultra-thin fin structure for efficient operation at a much-reduced constant bias current of only 100 µA, leading to a 10× decrease in active power consumption. Additionally, the device geometry optimized

successfully suppresses the OFF-state leakage current to an extremely low value of 5.24 fA, minimizing static power dissipation. Consequently, the proposed architecture achieves an exceptional ON/OFF switching ratio of approximately 2.46×10^9, representing nearly a three-order-of-magnitude improvement over the baseline device (1.23×10^6) and demonstrating significantly enhanced electrostatic gate control.

Despite operating under such ultra-low-power conditions, the proposed device maintains strong signal integrity and achieves improved relative magnetic sensitivities of 0.00159 T^{-1} along the Y-direction and 0.00147 T^{-1} along the Z-direction. These results correspond to sensitivity improvements of approximately 59% and 47%, respectively, compared to the conventional baseline MAGFinFET architecture.

TABLE 5.2. Comparative study of Relative Sensitivity with MAG FinFET

Sensor Architecture	Sensing Axis	Operating Bias (ID)	Relative Sensitivity (SR) in T^{-1}
Conventional MAGFinFET	Single-Axis (Z-direction)	1 mA	0.001
Proposed 2D-MagFinFET	Multi-Axis (Y-direction)	100 µA	0.00159
Proposed 2D-MagFinFET	Multi-Axis (Z-direction)	100 µA	0.00147

The proposed 2D-MagFinFET successfully overcomes the structural, thermal, and operational limitations of conventional single-axis MAGFinFET devices while providing enhanced normalized sensitivity, independent multi-axis magnetic sensing, superior switching performance, and significant reduction of power consumption.

5.8. Comparative Analysis Based on Relative Sensitivity

To quantitatively evaluate the electromagnetic sensing efficiency of the proposed 2D-MagFinFET, its performance was compared to several leading solid-state magnetic sensor architectures. Because different sensor technologies work with very different structures and bias conditions, S_A is not sufficient for a completely fair comparison. Hence, the main comparison metric is the S_R which normalizes the magnetic response to the applied I_D. Such normalization is particularly important for biomedical micro-robotic applications that require ultra-low-power operation and strict thermal safety constraints.

The comparative relative sensitivity values of the proposed device and the conventional state-of-the-art MAGFinFET architecture are summarized in Table 5.1.

TABLE 5.3. Relative sensitivity comparison among different magnetic sensing device

MAGNETIC SENSING DEVICES	GATE LENGTH, L_G (CONFIGURATION)	RELATIVE SENSITIVITY, S_R (T^{-1})
MAGFINFET [33]	50 nm (non-split drain)	0.002
FIN RESISTOR [33]	30 nm (non-split drain)	0.001
MAGFET [34]	L/W=1 (non-split drain)	0.050
MAGFET [34]	200 nm (Split drain)	0.003
GAN MAGFET [35]	100 nm (Split drain)	0.120
NC-FINFET [32]	30 nm (non-split drain)	0.240
2D-MAGFINFET [THIS WORK]	50 nm (non-split drain) In orthogonal directions	0.00159 in Y 0.00147 in Z

As illustrated in Table 5.1, conventional single-channel MAGFinFET architectures are inherently limited to single-axis magnetic field detection along the Z-direction. In addition, these devices require a relatively high driving current of 1 mA to generate a

measurable differential output signal, which significantly reduces their overall electromagnetic efficiency and restricts their S_R to only 0.001 T^{-1}. Such high-power consumption remains a major limitation for their integration into modern power-constrained microelectronic and biomedical systems.

5.9. Summary

This chapter comprehensively evaluated the multi-axis magnetic sensing performance of the proposed 2D-MagFinFET under varying external magnetic field conditions. The extracted results confirmed that the proposed dual-parallel fin architecture successfully achieves independent orthogonal magnetic field detection with strong immunity against structural cross-talk. In addition, the device demonstrated enhanced relative magnetic sensitivity, ultra-low-power operation, and superior electromagnetic efficiency compared to conventional MAGFinFET architectures. These findings validate the suitability of the proposed sensor for advanced biomedical micro-robotic navigation and spatial tracking applications.

After investing the electrical and magnetic performance of the proposed architecture, the next chapter draws the overall conclusions of this research, together with possible future improvements and research directions for the 2D-MagFinFET technology.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1. Introduction

This last chapter summarizes the overall research, design methodology and simulation analysis carried out in this thesis. It provides a summary of the main results and performance characteristics of the zero-field electrostatics of the proposed device presented in Chapter 4, and of its multi-axis magnetic sensing capability and intrinsic noise behaviour presented in Chapter 5. The overall operational advantages of the proposed 2D-MagFinFET over conventional single-axis magnetic sensor architectures are demonstrated in this chapter by combining these results. Besides, the chapter includes the future scope of the proposed work to emphasize the advanced noise reduction techniques that are needed to take the proposed nanoscale architecture from theoretical simulation to the practical implementation in the field of biomedical.

6.2. Summary of 2D-MagFinFET

In this thesis, the design, simulation and comprehensive performance evaluation of a novel dual-channel magnetic sensor, namely 2D-MagFinFET, developed for accurate spatial tracking and navigation of biomedical micro-robots was presented. In the context of the continuous scaling of modern microelectronic systems towards compact and energy-constrained biomedical environments, the demand of highly sensitive, multi-axis and ultra-low-power magnetic sensors has significantly increased beyond the capabilities of the conventional single-channel MAGFinFET architectures.

The proposed device employs a Silicon-on-Insulator (SOI) dual-parallel fin structure with a highly scaled 50 nm gate length to realize independent orthogonal magnetic sensing successfully. Using Sentaurus TCAD simulations and implementation of the Galvanomagnetic Transport model, it was demonstrated that the specially engineered symmetric and asymmetric drain-contact configurations allow the device to independently detect the magnetic field components along both the Y-axis and Z-axis without structural cross-talk. Moreover, the proposed architecture was completely immune to magnetic interference in the longitudinal X-axis.

The proposed 2D-MagFinFET also demonstrated excellent electrostatic performance compared to the conventional magnetic sensing architectures. The device shows a stable V_{TH} of 0.485 V and an excellent SS of 59.97 mV/dec, indicating a good electrostatic gate control and efficient switching behaviour. The electrostatic robustness was further confirmed by minimized DIBL value of 8.23 mV/V and output g_d close to 0 µS which offers a highly stable baseline current with high resistance to short-channel modulations effects. In addition, the aggressive geometric confinement of the ultra-thin fin structure effectively decreased the I_{OFF} to only 5.24 fA, resulting in an excellent SR of about 2.46×10^9. Furthermore, the architecture achieved a high g_{max} of 25.92 µS, showing strong intrinsic signal amplification capability.

Most importantly, the proposed architecture successfully addressed the severe power and thermal limitations associated with biomedical micro-robotic systems. While

conventional state-of-the-art MAGFinFET devices generally require a large operating current of 1 mA, the proposed 2D-MagFinFET achieved highly linear galvanomagnetic sensing operation using an ultra-low constant bias current of only 100 μA. Despite this significant reduction in active power consumption, the device maintained strong magnetic sensing performance and achieved S_R of 0.00159 T^{-1} along the Y-direction and 0.00147 T^{-1} along the Z-direction.

By combining independent multi-axis magnetic sensing capability, enhanced normalized sensitivity, excellent electrostatic control, and ultra-low-power operation, the proposed 2D-MagFinFET demonstrates strong potential as a next-generation magnetic sensing platform for biomedical micro-robotic navigation and advanced nanoscale spatial tracking applications.

6.3. What next

The strong absolute and relative sensitivity reached in the development of high-performance solid-state magnetic sensors is only the first step in the performance evaluation. The next big challenge will be to understand the intrinsic noise behaviour and the real spatial resolution capability of the device. Noise and resolution are among the most important operational parameters for magnetic sensors, especially in biomedical micro-robotic applications where the target magnetic fields for navigation are very weak. The real-world applicability of any sensor is ultimately limited by its noise floor, regardless of the raw magnetic sensitivity. This noise floor is caused by unavoidable internal electrical fluctuations, arising from thermal agitation, bulk carrier generation-recombination processes and interface-related defects. Since the differential current induced by an external magnetic field is smaller than the intrinsic noise fluctuations, the sensing signal cannot be reliably detected or recovered. Therefore, it is necessary to consider the sensor resolution, usually defined as the Minimum Detectable Magnetic Field (B_{min}), which is the lowest magnetic field intensity that the sensor can physically detect. This relationship between signal strength and intrinsic noise provides a bridge between theoretical semiconductor device physics and practical sensor engineering.

6.4. Future Scope

The TCAD-based computational analysis of the proposed 2D-MagFinFET has yielded very promising performance, however, the practical implementation of this device architecture from the theoretical simulation needs to be further studied in terms of the fundamental limits of device scaling and magnetic sensing resolution. The results obtained in this work lay a strong foundation and give a clear direction for several important future research developments:

6.4.1. Fundamental Noise Analysis and Physical Validation

In nanoscale semiconductor devices, intrinsic electrical noise creates a fundamental noise floor that can obscure extremely small differential current signals. Using small-signal AC simulations, the intrinsic Noise Current Spectral Density (SI(f)) of the proposed 2D-MagFinFET was extracted by considering three major physical noise mechanisms: low-frequency Flicker (1/f) noise caused by interface trap states, mid-frequency Generation-Recombination (G-R) noise associated with bulk carrier fluctuations, and high-frequency Diffusion or thermal noise. By normalizing the combined noise floor with respect to the absolute magnetic sensitivity of the device, the B_{min} was theoretically estimated.

An important future direction of this work involves the physical fabrication of the proposed 2D-MagFinFET using CMOS-compatible SOI technology in order to experimentally validate these theoretical predictions. In practical fabricated devices, real interface trap densities and process-induced imperfections are expected to introduce additional low-frequency 1/f noise components. Therefore, comparing the experimentally extracted B_{min} values with the theoretical TCAD-based limits established in this study will be essential for optimizing the fabrication process and further improving the overall sensing performance of the device.

6.4.2. Design of Ultra-Low-Noise Readout Circuitry

The equivalent wide-band magnetic resolution (B_{eq}) calculated in this study serves as an important design foundation for the next stage of system-level development, namely on-chip signal processing integration. For the proposed 2D-MagFinFET to operate as a fully autonomous sensing platform, the extracted ΔI_Y and ΔI_Z must be accurately amplified and converted into digital signals. Since the calculated B_{min} defines the fundamental noise limit of the device, future research should focus on developing integrated CMOS-compatible readout circuits, such as ultra-low-noise Differential Transimpedance Amplifiers (DTAs), whose input-referred noise remains significantly lower than the intrinsic noise spectral density of the sensing fins themselves.

6.4.3. Implementation of Active Noise Mitigation Techniques

The low frequency, which is the typical operating environment for biomedical micro-robots, is dominated by the 1/f interface noise and greatly limits the magnetic resolution of the sensor. Thus, future work on the 2D-MagFinFET system will be primarily aimed at the integration of advanced dynamic offset-cancellation techniques. Low-frequency 1/f noise can be suppressed by shifting it away from the baseband region by using device biasing schemes, such as spinning-current operation and chopping-based modulation. By employing these active noise reduction techniques, the magnetic resolution should be greatly improved with the reduction of the B_{min} which will improve the overall detectivity and sensitivity of the proposed sensor architecture.

6.5. Conclusion

The development of biomedical micro-robotics is intrinsically limited by the miniaturization, power efficiency and spatial resolution of navigational sensors. In this thesis, these critical challenges are successfully tackled by proposing and evaluating extensively the 2D-MagFinFET. This work shows that ultra-low-power orthogonal magnetic vector tracking can be realized by the transition from conventional single-axis, high-power MAGFET designs to a nanoscale dual-channel FinFET architecture. The successful decoupling of the magnetic responses of the Y-axis and Z-axis and the

excellent zero-field electrostatic integrity of the device is a significant step forward in current-mode magnetic sensing.

Although further optimization is needed to transfer the TCAD computational modelling to a physical, in-vivo implementation, especially for intrinsic noise reduction and integrated readout circuitry, the fundamental architecture presented in this paper offers a solid basis for future advancements.

REFERENCES

[1] L. Ł. a. A. Jakubowski, "History of Semiconductors," *ournal of Telecommunications and Information Technology,* vol. 39, p. 1, 2010, doi: https://doi.org/10.26636/jtit.2010.1.1015.

[2] C. A. Mack, "Fifty years of Moore's law," *IEEE Transactions on Semiconductor Manufacturing,* vol. 24, no. 2, pp. 202-20, 2011.

[3] R. Chaujar, "Towards Extended Hückel model-based reliability performance enhancement of gate stack graphene nanoribbon field effect transistor," *Microelectronics Reliability,* vol. 173, p. 115869, 2025.

[4] T. Skotnicki, "Materials and device structures for sub-32 nm CMOS nodes," *Microelectronic Engineering,* vol. 84, no. 9-10, pp. 1845-1852, 2007.

[5] J. N. Haddock, X. Zhang, S. Zheng, Q. Zhang, S. R. Marder, and B. Kippelen, "A comprehensive study of short channel effects in organic field-effect transistors," *Organic electronics,* vol. 7, no. 1, pp. 45-54, 2006.

[6] J. Lee, C. Medina-Bailon, O. Badami, and V. P. Georgiev, "Subthreshold swing (SS) degradation as the origin of SS saturation in nanoscale cryogenic gate-all-around MOSFETs," *Semiconductor Science and Technology,* vol. 40, no. 9, p. 095002, 2025.

[7] N. Maity, R. Maity, and S. Baishya, "Ultra thin body partial silicon-on-insulator MOSFET with suppressed floating body effect: A simulation study," *Journal of Nanoelectronics and Optoelectronics,* vol. 12, no. 5, pp. 472-479, 2017.

[8] Y. C. Yee *et al.*, "Nanoscale ultra-thin-body silicon-on-insulator P-MOSFET with a SiGe/Si heterostructure channel," *IEEE Electron device letters,* vol. 21, no. 4, pp. 161-163, 2000.

[9] R. J. Baker, *CMOS: circuit design, layout, and simulation*. John Wiley & Sons, 2019.

[10] H. H. Radamson *et al.*, "State of the art and future perspectives in advanced CMOS technology," *Nanomaterials,* vol. 10, no. 8, p. 1555, 2020.

[11] H. Iwai, "CMOS technology-year 2010 and beyond," *IEEE Journal of Solid-State Circuits,* vol. 34, no. 3, pp. 357-366, 1999.

[12] F. H. G. Robert H. Dennard, Hwa-Nien Yu, V. Leo Rideout, Ernest Bassous, Andre R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," *IEEE Journal of Solid-State Circuits,* vol. SC-9, Issue 5, pp. 256–268, October 1974, doi: 10.1109/JSSC.1974.1050511.

[13] B. Yu *et al.*, "FinFET scaling to 10 nm gate length," in *Digest. International Electron Devices Meeting*, 2002: IEEE, pp. 251-254.

[14] R. S. Pal, S. Sharma, and S. Dasgupta, "Recent trend of FinFET devices and its challenges: A review," in *2017 Conference on Emerging Devices and Smart Systems (ICEDSS)*, 2017: IEEE, pp. 150-154.

[15] T. Sahoo, N. Kumar, P. K. Sahoo, and S. R. Panda, "Process-induced variability in a three-channel FinFET hydrogen sensor: design, statistical

assessment and sensitivity evaluation," *Physica Scripta,* vol. 100, no. 12, p. 125024, 2025.
[16] N. Jankovic, O. Kryvchenkova, S. Batcup, and P. Igic, "High sensitivity dual-gate four-terminal magnetic sensor compatible with SOI FinFET technology," *IEEE Electron Device Letters,* vol. 38, no. 6, pp. 810-813, 2017.
[17] S. In't Hout and S. Middelhoek, "High temperature silicon Hall sensor," *Sensors and Actuators A: Physical,* vol. 37, pp. 26-32, 1993.
[18] A. G. Ravlik, "AMR and GMR Layers and multilayers for magnetic field sensors," in *Nanostructured Magnetic Materials and Their Applications*: Springer, 2002, pp. 22-42.
[19] P. Ripka, M. Tondra, J. Stokes, and R. Beech, "AC-driven AMR and GMR magnetoresistors," *Sensors and Actuators A: Physical,* vol. 76, no. 1-3, pp. 225-230, 1999.
[20] J. Lau, P. K. Ko, and P. C. Chan, "Modelling of split-drain magnetic field-effect transistor (MAGFET)," *Sensors and Actuators A: Physical,* vol. 49, no. 3, pp. 155-162, 1995.
[21] G. F. Santillan-Quinonez, V. Champac, and R. S. Murphy, "Exploiting magnetic sensing capabilities of short split-drain MAGFETs," *Solid-State Electronics,* vol. 54, no. 11, pp. 1239-1245, 2010.
[22] R. Rodríguez-Torres, E. A. Gutiérrez-Domínguez, R. Klima, and S. Selberherr, "Analysis of split-drain MAGFETs," *IEEE Transactions on Electron Devices,* vol. 51, no. 12, pp. 2237-2245, 2004.
[23] T. Phetchakul, C. Pamonchom, and A. Poyai, "MAGFinFET: The Channel Length Effect," in *2020 6th International Conference on Engineering, Applied Sciences and Technology (ICEAST)*, 2020: IEEE, pp. 1-4.
[24] R. Nakachai, A. Poyai, and T. Phetchakul, "Non-split drain MAGFET," in *2019 5th International Conference on Engineering, Applied Sciences and Technology (ICEAST)*, 2019: IEEE, pp. 1-4.
[25] Y.-C. Wu and Y.-R. Jhan, "Introduction of synopsys sentaurus TCAD simulation," in *3D TCAD Simulation for CMOS Nanoeletronic Devices*: Springer, 2017, pp. 1-17.
[26] I. Avci *et al.*, "Three-dimensional TCAD process and device simulations," in *2006 16th Biennial University/Government/Industry Microelectronics Symposium*, 2006: IEEE, pp. 41-46.
[27] S. D. U. Manual, "Sentaurus device user manual," *CA, USA: Synopsys, Synopsys,* 2022.
[28] R. Stratton's, "Diffusion of Hot and Cold Electron in Semiconductor Barriers," Physical Review vol. 126, p. 6, doi: https://doi.org/10.1103/PhysRev.126.2002.
[29] A. O. W. Bludau, W. Heinke, "Temperature dependence of the band gap in silicon," *Journal of Applied Physics* vol. 45, no. 4.
[30] P. Bechthold, "B 7 Galvanomagnetic Transport: from Hall Effect to AMR," 2009.
[31] K. T. N. Swe, A. Poyai, and T. Phetchakul, "Investigation of Noise and Resolution of Magnetic FinFET (MAG-FinFET)," *IEEE Sensors Journal,* vol. 25, no. 2, pp. 2479-2486, 2024.

[32] R. K. Maurya, R. G. Debnath, R. Saha, and B. Bhowmick, "Enhanced magnetic field sensing with MAGNC-FinFET: A current mode Hall effect approach," *IEEE Transactions on Nanotechnology,* vol. 23, pp. 250-256, 2024.
[33] K. T. N. Swe, C. Pamonchom, A. Poyai, and T. Phetchakul, "Novel MAGFinFET: Operation, design and geometry effect for modern sensors," *Journal of Mobile Multimedia,* vol. 18, no. 4, pp. 1301-1332, 2022.
[34] R. Nakachai, A. Poyai, and T. Phetchakul, "High sensitivity non-split drain MAGFET for wireless sensor networks," *Journal of Mobile Multimedia,* vol. 16, no. 1-2, pp. 45-64, 2020.
[35] S. Faramehr, B. Thomas, N. Janković, J. Evans, M. P. Elwin, and P. Igić, "Analysis of GaN MagFETs compatible with RF power technology," in *2018 41st International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, 2018: IEEE, pp. 0050-0053.

TCAD-Based magnetic analysis of 2D-MagFinFET in Orthogonal directions for Medical Micro-Robots application

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Abstract*—In this work, a new magnetic sensor Two Directional Magnetic Fin Field Effect Transistor (2D-MagFinFET) is analyzed for magnetic sensing. The proposed device is designed to sense orthogonal magnetic field in two directions. It is operated on the concept of Lorentz force acting on the carrier in channel due to magnetic field applied. Device uses two parallel fins to sense the magnetic field. One fin will detect the magnetic field of Y-direction and the other one of Z-direction. The performance of the proposed device is analyzed in terms of Threshold Voltage (V_{TH}), Subthreshold Swing (SS), On-Current (I_{ON}), Off-Current (I_{OFF}), Magnetic Sensitivity and Relative magnetic sensitivity (S_R) compared to existing device. The author analyzed the V_{TH} increase from 0.21 V to 0.48 V by 128.57 % and SS decrease from 63 mV/dec to 59.96 mV/dec by 4.83 %. I_{OFF} and I_{ON} currents of the proposed device is 5.24 fA and 12.9 µA having a switching ratio (I_{ON}/I_{OFF}) of 2.39 × 10^9. These results demonstrate the better switching and performance of proposed device than the existing device. The magnetic response shows the linear dependency of differential current (ΔI_Y and ΔI_Z) with Magnetic field having a sensitivity of 159.27 nA/T in Y-direction and 147.13 nA/T in Z-direction at 100 µA biased current. The relative sensitivity is 0.00159 T^{-1} and 0.00147 T^{-1} in Y and Z direction respectively, improved from recently reported device. Owing the magnetic sensitivity in orthogonal direction the proposed device is suitable for the spatial tracking and navigation of medical micro-robots.

Keywords*—2D-MagFinFET, Magnetic sensor, SOI FinFET, Lorentz Force, Galvanic Transport model, TCAD

INTRODUCTION

The FinFET was first proposed in 1998 to solve the short channel effect and drain-induced barrier lowering effect (DIBL). Moore's law states that the number of transistors integrated on the semiconductor chip approximately doubles every two years. This scaling trend has driven the evolution of planar metal–oxide–semiconductor field-effect transistors (MOSFETs). This technology enables very large-scale integration (VLSI). However, when MOSFET dimensions approach the nanometer scale Moore's law faced physical limitation due to short channel effect (SCE), leakage current, and reduced gate control[1].

To sustain scaling beyond planar structure, advanced device 3D architecture such as Fin Field Effect Transistors (FinFETs) were introduced. In FinFETs, the channel is formed as a vertical fin surrounded by gate from multiple sides, providing superior electrostatic control. This structure sustains continuously continues Moore's law by enabling further scaling while reducing leakage current and improving performance of the device[2].

FinFETs not only improve the performance but are highly suitable for sensor applications due to excellent electrostatic integrity and high surface to volume ratio. The vertical fin geometry offers a high surface to volume ratio allowing external physical parameters such as magnetic field etc. These external parameters strongly influence carrier transport in channel. Their low power consumption and nanoscale dimensions further make FinFETs ideal for highly sensitive and energy efficient sensing devices[3].

The MAGFinFET was first proposed in 2019 by the authors as a novel magnetic sensing device based on the FinFET architecture. This device is designed to detect the vertical magnetic field applied along the Z-direction. It operates on the principle of a non-split drain MAGFET structure, where a gapless drain contact model is used, adopted from Nakachai *et al.* [4], is employed. Conventional MAGFinFET architectures are inherently limited to single-axis sensing, making them unsuitable for detecting orientation changes across multiple directions. Therefore, multi-directional sensing systems are essential for achieving highly accurate and reliable spatial

tracking. This 2D-MagFinFET is the first proposed device that uses dual channel FinFET design to detect the two-direction magnetic field. This device is operated according to the motion of the carrier due to Lorentz force under external magnetic field. Due to Lorentz force, the carrier shifted toward one drain which cause the increase in drain current in one side and decrease in other side and an imbalance is create which give differential currents (ΔI_Y and ΔI_Z) for Y and Z direction respectively [5].

In this present work, the author has studied the structural geometry, electrical characteristics and magnetic sensing of the proposed device using the Sentaurus TCAD. Also, the effect of two orthogonal magnetic field on the orthogonality independency of device is analyzed. Author also demonstrates this device is highly recommended and suitable for the spatial tracking and navigation of medical micro-robots which can be done precisely.

DEVICE STRUCTURE AND SIMULATION

Structure Geometry

The proposed Dual-Fin 2D-MagFinFET simulated structure is illustrated in Fig. 1. In this configuration, the device represents a conventional multi-fin FinFET architecture consisting of two fins aligned parallel to each other with a center-to-center spacing of 11 nm. The width and height of the fins are 5 nm and 15 nm, respectively. The gate length is maintained at 50 nm. The gate structure is composed of multiple layers, including Silicon dioxide (SiO_2), Hafnium oxide (HfO_2), and Titanium nitride (TiN) metal gate. The channel length is kept equal to the gate length ($L_G = L_{CH} = 50\,\text{nm}$). The distance between the source and drain regions is 100 nm, with the gate positioned at the center of the fins. A thin SiO_2 (high-κ dielectric of 3.9) interfacial layer with a thickness of 0.5 nm is incorporated between the channel and the gate dielectric[6]. Additionally, HfO_2 (high-κ dielectric of 22) material is utilized as the gate dielectric to improve the electrostatic control of the gate over the fins. The cross-sectional view of device structure is shown in Fig. 2. Arsenic is employed for source/drain doping to create n-type regions with a concentration of $5 \times 10^{20}\ \text{cm}^{-3}$, whereas boron is used for channel doping to obtain p-type behavior with a concentration of $5 \times 10^{15}\ \text{cm}^{-3}$. Since the device is based on a Silicon-on-Insulator (SOI) FinFET structure, 30 nm thick buried oxide (BOX) layer of SiO_2 is incorporated into the structure. All device parameters are tabulated in TABLE I.

To enable magnetic field sensing, the authors adopted a non-split drain concept. The drain contacts are arranged symmetrically to ensure equal current extraction from each

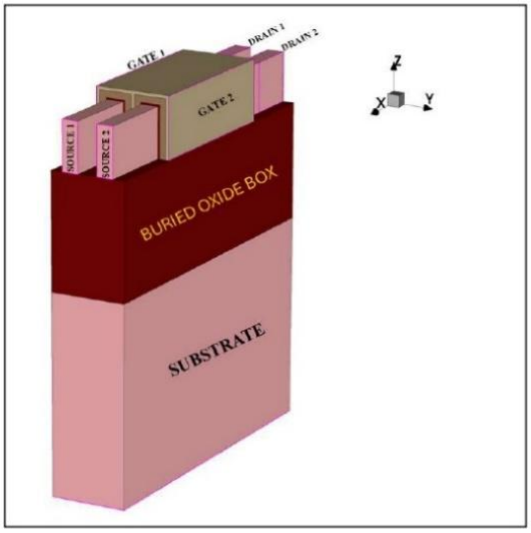

Fig. 1 Geometrical structure of 2D-MagFinFET

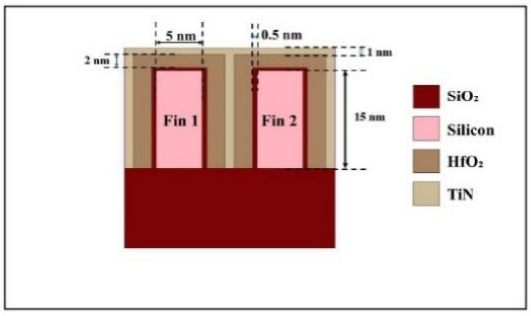

Fig. 2 Cross-sectional view of structure

TABLE I
GEOMETRIC DIMENSION OF DEVICE

Parameter	Dimension
Fin Height, F_H	15 nm
Fin Width, F_W	5 nm
Interfacial Oxide thickness, t_{OX}	0.5 nm
Gate Dielectric thickness, D_{GD}	2 nm
Channel length, L_{CH}	50 nm
Gate Length, L_G	50 nm
Length from Source (S) to Drain (D) side	100 nm
Separation between Fins, D_F	11 nm
Source/Drain Doping Concentration, $N_{S,D}$	$5 \times 10^{20}\ \text{cm}^{-3}$
Channel Doping Concentration, N_{CH}	$5 \times 10^{15}\ \text{cm}^{-3}$

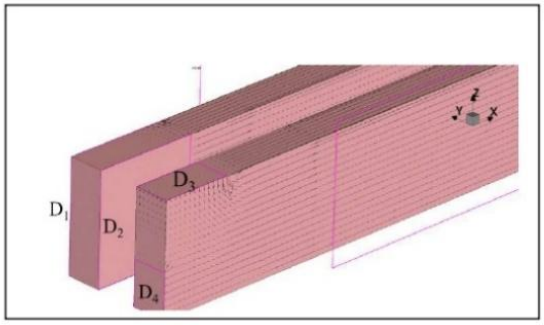

Fig. 3 Drain contacts visualization

contact. This device is designed to sense magnetic fields in 2 directions (Y and Z), so the orientation of the contacts on both fins is different. The Fin 1 is designed to sense the Y-direction magnetic field, and Fin 2 is designed to sense the Z-direction magnetic field. The contact on Fin 1 is placed on the side of drain having the same cross section area and separation of 5 nm same as fin width named as D_1 and D_2. The distance between drain contacts should be minimum to get better sensitivity[7]. The contact of Fin 2 placed one on the top of the drain side and the other is on the bottom side of the outer face of the drain named as D_3 and D_4. The area of the Fin 2 contacts is different. Bottom outer face contact (D_4) cross-section area is slightly less than the upper side drain contact (D_3) because the current density in bottom contact is high due to interface interaction with the Buried Box as shown in Fig. 3. Without any magnetic field, the difference in the drain currents (ΔI_Y and ΔI_Z) is zero but can have a deflection if the orientation and length of contact are not symmetrical and different[8]. The visual representation of drain contacts is shown in Fig. 3.

TCAD Simulation

The study of the performance analysis and evaluation of different electrical properties and magnetic sensing of the device is carried out using the Synopsys Sentaurus TCAD. This TCAD framework incorporate physical model to accurately represent the underlying device Physics for the proposed design. For nano electronic devices, standard governing equations are available within the simulation environment. Most used equations are drift diffusion currents, current continuity equation, Poisson equation, Fermi-Dirac probability are calculated accurately and simultaneously. The Quantum effect can be considered here for better results, but eQuantumpotential model cannot be applied with the Galvanic Transport model[9]. As the Off-state leakage current which is an important aspect for the FinFET, Shockley-Read-Hall model is used for accuracy. For high doping concentration in S/D region Bandgap Narrowing model is used. Other models such as Auger and Enormal for surface scattering are used.

To analyze the impact of magnetic fields on semiconductor devices, the transport equations governing the motion of electrons and holes must be accurately formulated and solved. In this work, the conventional drift–diffusion model for carrier current densities J_n and J_p is extended by including magnetic field–dependent terms, thereby accounting for the effect of the Lorentz force on carrier transport. Within Sentaurus TCAD, the Galvanic Transport model is employed to incorporate and apply the magnetic field along the required direction as follows [9].

$$J_\alpha = \mu_\alpha g_\alpha + \mu_\alpha \frac{1}{1+(\mu_\alpha^* B)^2}[\mu_\alpha^* B \times g_\alpha + \mu_\alpha^* B \times (\mu_\alpha^* B \times g_\alpha)] \quad (1)$$

Here, α represents the carrier type in the semiconductor (n and p), J_α denotes the carrier current density vector, and g_α corresponds to the current vector in the absence of mobility effects. The term μ_α^* indicates the Hall mobility, B represents the magnetic induction vector.

RESULT AND DISCUSSION

This section is split into three sections. The first section investigates the electrical characteristics of proposed device and discusses the Transfer characteristics, Output Characteristics, V_{TH}, SS and switching performance of the proposed 2D-MagFinFET. In second section, the author analyzes the magnetic sensing of the device and also studies about the orthogonality independency of the magnetic sensing when magnetic field is applied. In the final section, a comparative analysis is presented between the proposed 2D-MagFinFET and other recently reported devices.

Electrical Characteristics

The Transfer characteristic of the proposed device is depicted in Fig. 4.

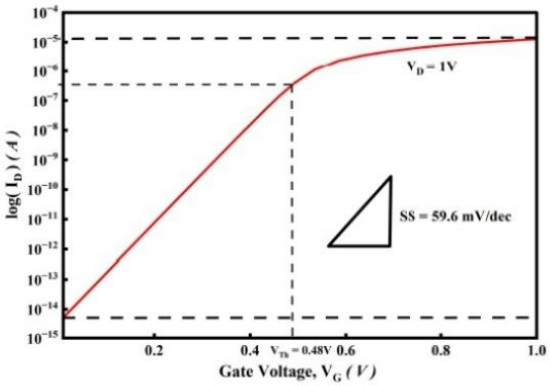

Fig. 4 Transfer Characteristics of 2D-MagFinFET

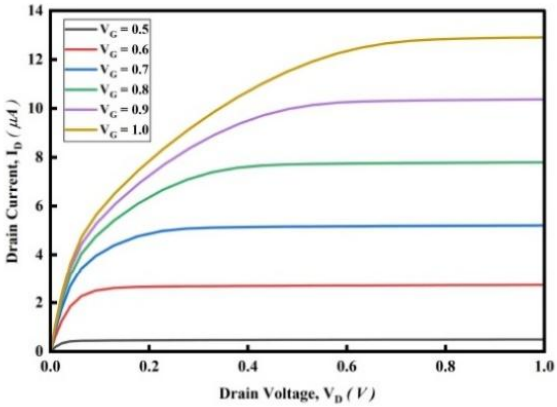

Fig. 5 Output Characteristics of device

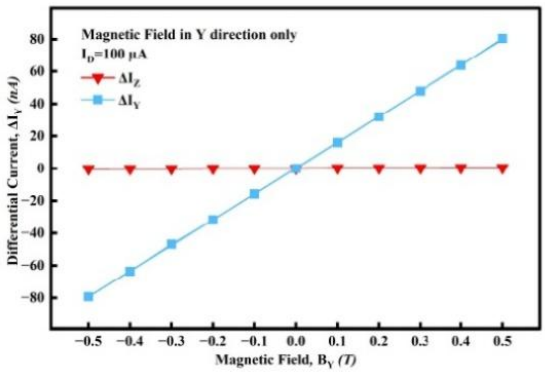

Fig. 6 Magnetic Response for Y-direction only

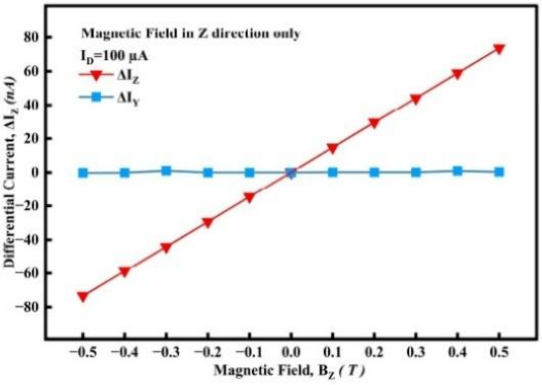

Fig. 7 Magnetic Response for Z-direction only

The gate voltage (V_G) is varied from 0 to 1 V at constant drain voltage (V_D) equals to 1 V. The figure demonstrates Subthreshold Swing (*SS*) has a value of 59.96 mV/dec which measure how efficiently device switches from completely OFF to ON state. The *SS* of the proposed device is improved by 4.83 % quite good as compared to the reported device demonstrate better switching performance[10]. The Threshold voltage (V_{TH}) measured as 0.48 V increases by 128.57 % which is higher than the existing device due to Gate stack which will protect device from accidently turning ON [10]. The proposed magnetic sensor demonstrates superior switching performance, as extracted from Fig. 4 at V_D = 1 V. The device achieved a high on-current (I_{ON}) of 12.9 μA and low off-current (I_{OFF}) 0f 5.24 femto Ampere (fA). This measures I_{ON}/I_{OFF} *ratio* of approximately 2.39×10^9, indicating excellent gate control and low power sensing application. The incorporation of a high-κ dielectric layer in the gate stack enhances the electric fields, thereby reducing the potential barrier in the OFF state. Consequently, this results in an increase in I_{ON} and a decrease in I_{OFF} [11].

The Output characteristic of 2D-MagfinFET were analyzed for V_G ranging from 0.5 *V* to 1.0 *V* with a step size of 0.1 *V* (Fig. 5). The curve depicts well defined linear and saturation regions. It indicates a strong transportation of the carrier in the 3D fin at different V_G.

Magnetic Response

Fig. 6 and Fig. 7 show the magnetic response of the 2D-MagFinFET when only 1 direction (either Y or Z) magnetic field is applied. The current difference ΔI_Y /ΔI_Z vs Magnetic field is plotted. The device is biased using a constant current (I_D) source of 100 μA. The magnetic field varies from -0.5 T to 0.5 T with a step of 0.1 T in vertical direction Y and Z separately. D_1, D_2, D_3 and D_4 are connected to V_D = *1V*. The current difference is taken as the difference in the drain current I_{D1} and I_{D2} and represented by $\Delta I_Y = I_{D1} - I_{D2}$ for Y direction magnetic field. Similarly, for Z direction $\Delta I_Z = I_{D3} - I_{D4}$ is the differential current. At zero magnetic field there is no deflection in differential currents.

1. Magnetic field in 1-Direction only

The Y direction magnetic response of the device can be shown in Fig. 6. The most important thing which should be noticed is that when a magnetic field is applied in Y direction, only Fin 1 is an active one. Here it is clearly showing the linear dependence of the differential current when magnetic field is varied from 0 to 0.5 T. The zero deflection in ΔI_Z shows device is orthogonal independent according to magnetic field applied which is difficult to achieve. The sensitivity can be measured

and defined as ΔI_Y *Vs* ΔB. For the gate length 50 nm sensitivity is 159.27 nA/T for Y direction.

The Z direction magnetic response is shown in Fig. 7. This time Fin 2 is active, and Fin 1 doesn't show any response to magnetic fields. Magnetic field is again varied from -0.5 T to 0.5 T. The plot of differential current ΔI_Z also show the linear dependency with respect to magnetic field. The sensitivity measured for 50 nm gate is 147.13 nA/T for Z direction. The relative sensitivity of the device, calculated using (2), is calculated 0.00159 T^{-1} in Y direction and 0.00147 T^{-1} in Z direction[12].

$$\text{Relative Sensitivity, } S_R = \frac{\Delta I_{Y,Z}}{I_D B} \quad (2)$$

2. *Magnetic field in 2-Direction*

When the magnetic field is applied simultaneously in both Y and Z direction, then Fin 1 and Fin 2 both are active and exhibit the same magnetic response which was observed individually in each direction. The magnetic response under application of magnetic fields in both directions is illustrated in Fig. 8. The different sensitivity of Y and Z direction helps us to determine which Fin is active and direction of applied magnetic field. When the X direction magnetic field is applied, both fins show no deflection. That is why this device is named "2D-MagFinFET" demonstrate this is 2 directional magnetic sensors.

Comparative analysis of proposed device

To evaluate the performance advancement of the proposed device, TABLE II benchmarks the electrical and magnetic characteristics and improvement in different parameters of 2D-MagFinFET against the MAGFinFET proposed by Swe *et al.* [10]. As shown in Table II, the proposed device achieves better switching characteristics and stronger gate control, while also providing higher magnetic sensitivity a low bias current of 100 µA compared to the MAGFinFET biased at 1 mA reported by Swe *et al.* [18].

Table III presents a comparative overview of the relative sensitivity (S_R) across various reported magnetic sensing devices. The data clearly demonstrates that the proposed 2D-MagFinFET achieves highly competitive sensitivity, specifically noting its ability to sense in orthogonal directions (0.00159 T^{-1} in the Y-direction and 0.00147 T^{-1} in the Z-direction). This represents an improvement over several conventional models, such as standard MAGFinFET and Fin Resistors at similar gate lengths. It should be noted, however, that a direct comparison is complex due to significant variations in the underlying structures and doping profiles of the benchmarked devices.

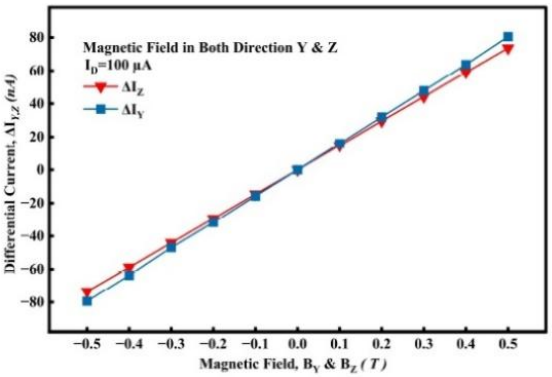

Fig. 8 Magnetic Response for Both directions together

TABLE II. PERFORMANCE COMPARISON OF THE PROPOSED 2D-MAGFINFET

Parameter	MAGFinFET [10]	2D-MagFinFET [This work]	Improvement
V_{TH}	0.21V	0.48 V	128.57 % increses
SS (mV/dec) at L_G = 50 nm	63	59.96	4.83 % reduction
I_{OFF}	50.53 pA	5.24 fA	99.99 % reduction
I_{ON}	62.13 µA	12.9 µA	79.24 % reduction
Switching Ratio	1.22×10^6	2.39×10^9	1959 times increase
Magnetic Sensitivity	181.6 nA/T in Z-direction (I_D = 1mA)	147.13 nA/T in Z-direction and 159.27 nA/T in Y-direction (I_D = 100 µA)	Orthogonal sensing capability
Magnetic Sensing	Only in Z-direction	In orthogonal directions (Y and Z)	Dual-axis Independent sensing

TABLE III
RELATIVE SENSITIVITY COMPARISON AMONG DIFFERENT MAGNETIC SENSING DEVICE

MAGNETIC SENSING DEVICES	GATE LENGTH, L_G (CONFIGURATION)	RELATIVE SENSITIVITY, S_R (T^{-1})
MAGFINFET [10]	50 nm (non-split drain)	0.002
FIN RESISTOR [10]	30 nm (non-split drain)	0.001
MAGFET [7]	L/W=1 (non-split drain)	0.050
MAGFET [7]	200 nm (Split drain)	0.003
GAN MAGFET [13]	100 nm (Split drain)	0.120
NC-FINFET [12]	30 nm (non-split drain)	0.240
2D-MAGFINFET [THIS WORK]	50 nm (non-split drain) In orthogonal directions	0.00159 in Y 0.00147 in Z

CONCLUSION

The proposed 2D-MagFinFET enables the detection of vertical magnetic fields in orthogonal directions, while achieving a 4.83 % improvement in subthreshold swing (*SS*) and 128.57 % increase in threshold voltage (V_{TH}) relative to the previously reported device. The switching ratio (I_{ON}/I_{OFF}) is achieved 2.39 × 10^9 demonstrate better performance. The sensing of the magnetic field in one direction operates independently of the sensing in the other direction. No disturbance is observed in the magnetic response of the direction in which the magnetic field is not applied. The device structure is based on a conventional multi-channel SOI FinFET with different positions and orientations of the drain contacts, denoted as D_1, D_2, D_3 and D_4. The sensing mechanism is based on the Lorentz force, where the charge carriers experience deflection when a magnetic field is applied. When magnetic fields are applied in the Y and Z directions, the sensitivities of the device are 159.27 nA/T and 147.13 nA/T, respectively. The device achieves relative sensitivity of 0.00159 T^{-1} in Y direction and 0.00147 T^{-1} in Z direction in contrast to the other baseline magnetic sensor which can sense in Z direction only. In 2D-MagFinFET the difference in sensitivity in Y and Z direction enables the determination of the direction of the applied magnetic field. The overall comparison is also done with recently reported devices demonstrates proposed device can sense in orthogonal direction with improvement in the sensitivity over several reported devices. Therefore, the proposed 2D-MagFinFET can be suitable for low power, high performance and navigation application like spatial tracking and navigation of medical micro-robots due to its capability of sensing two vertical magnetic field.

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REFERENCES

[1] C. N. Yalung, W. Yamwong, and D. Tantraviwat, "Optimization of multi-fins FinFET implemented on SOI wafer based on SiGe and Gaussian process regression," *IEEE Access,* vol. 12, pp. 163444-163451, 2024.

[2] S. Virumandi and P. Kumar, "Performance and Reliability Assessment of Schottky Complementary Multi-FinFET Inverter for Advanced Scaling Nodes," *IEEE Access,* 2025.

[3] T. Sahoo, N. Kumar, P. K. Sahoo, and S. R. Panda, "Process-induced variability in a three-channel FinFET hydrogen sensor: design, statistical assessment and sensitivity evaluation," *Physica Scripta,* vol. 100, no. 12, p. 125024, 2025.

[4] R. Nakachai, A. Poyai, and T. Phetchakul, "Non-split drain MAGFET," in *2019 5th International Conference on Engineering, Applied Sciences and Technology (ICEAST)*, 2019: IEEE, pp. 1-4.

[5] K. T. N. Swe, A. Poyai, and T. Phetchakul, "Investigation of Noise and Resolution of Magnetic FinFET (MAG-FinFET)," *IEEE Sensors Journal,* vol. 25, no. 2, pp. 2479-2486, 2024.

[6] R. Chaujar, "Performance Assessment of Gate-Stacked Junctionless Trigate FinFET With Multi-Material Work Function Engineering," in *2025 13th International Conference on Intelligent Embedded, MicroElectronics, Communication and Optical Networks (IEMECON)*, 2025: IEEE, pp. 1-5.

[7] R. Nakachai, A. Poyai, and T. Phetchakul, "High sensitivity non-split drain MAGFET for wireless sensor networks," *Journal of Mobile Multimedia,* vol. 16, no. 1-2, pp. 45-64, 2020.

[8] R. Rodríguez-Torres, E. A. Gutiérrez-Domínguez, R. Klima, and S. Selberherr, "Analysis of split-drain MAGFETs," *IEEE Transactions on Electron Devices,* vol. 51, no. 12, pp. 2237-2245, 2004.

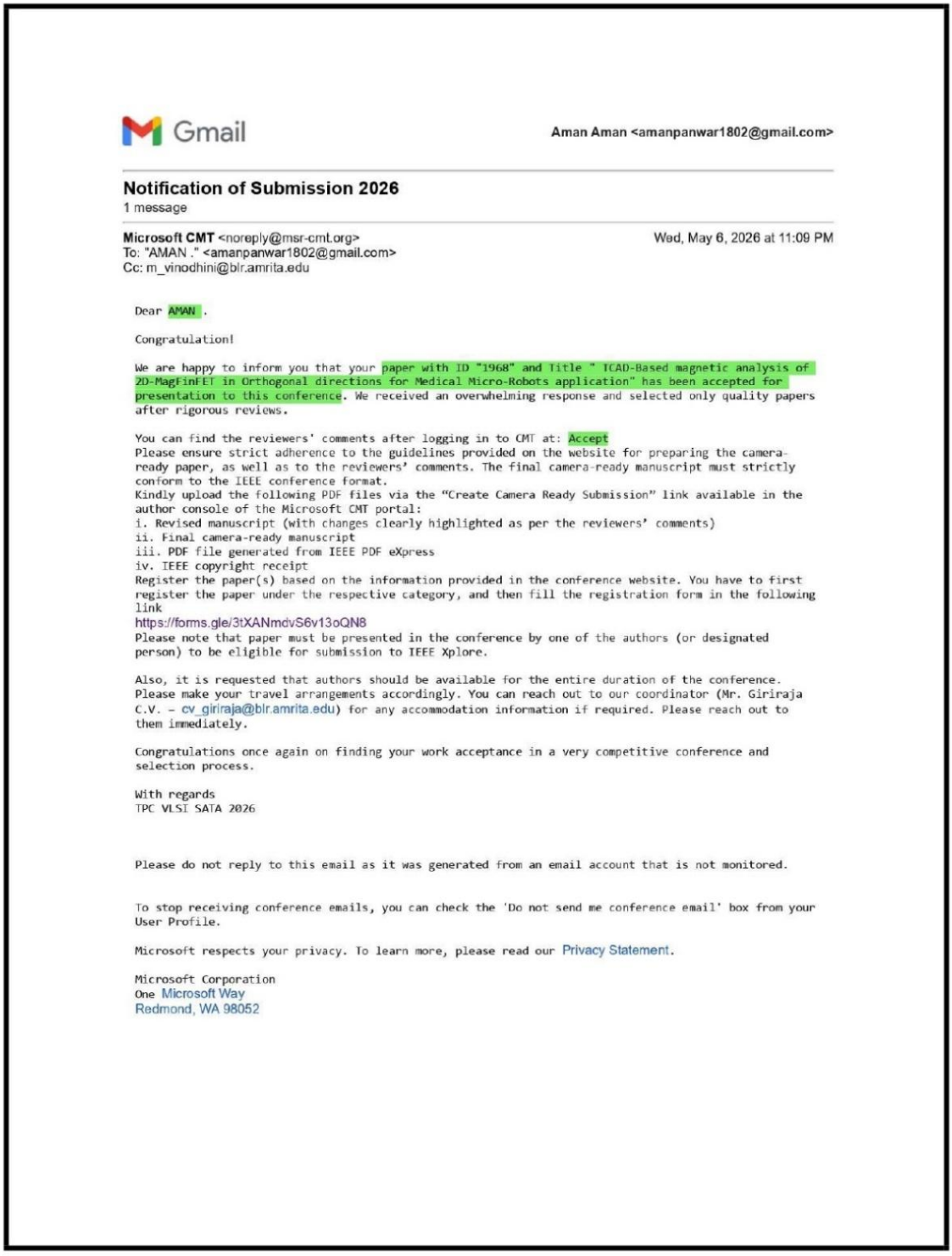
[9] S. D. U. Manual, "Sentaurus device user manual," *CA, USA: Synopsys, Synopsys,* 2022.

[10] K. T. N. Swe, C. Pamonchom, A. Poyai, and T. Phetchakul, "Novel MAGFinFET: Operation, design and geometry effect for modern sensors," *Journal of Mobile Multimedia,* vol. 18, no. 4, pp. 1301-1332, 2022.

[11] R. Chaujar, "Towards Extended Hückel model-based reliability performance enhancement of gate stack graphene nanoribbon field effect transistor," *Microelectronics Reliability,* vol. 173, p. 115869, 2025.

[12] R. K. Maurya, R. G. Debnath, R. Saha, and B. Bhowmick, "Enhanced magnetic field sensing with MAGNC-FinFET: A current mode Hall effect approach," *IEEE Transactions on Nanotechnology,* vol. 23, pp. 250-256, 2024.

[13] S. Faramehr, B. Thomas, N. Janković, J. Evans, M. P. Elwin, and P. Igić, "Analysis of GaN MagFETs compatible with RF power technology," in *2018 41st International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, 2018: IEEE, pp. 0050-0053.



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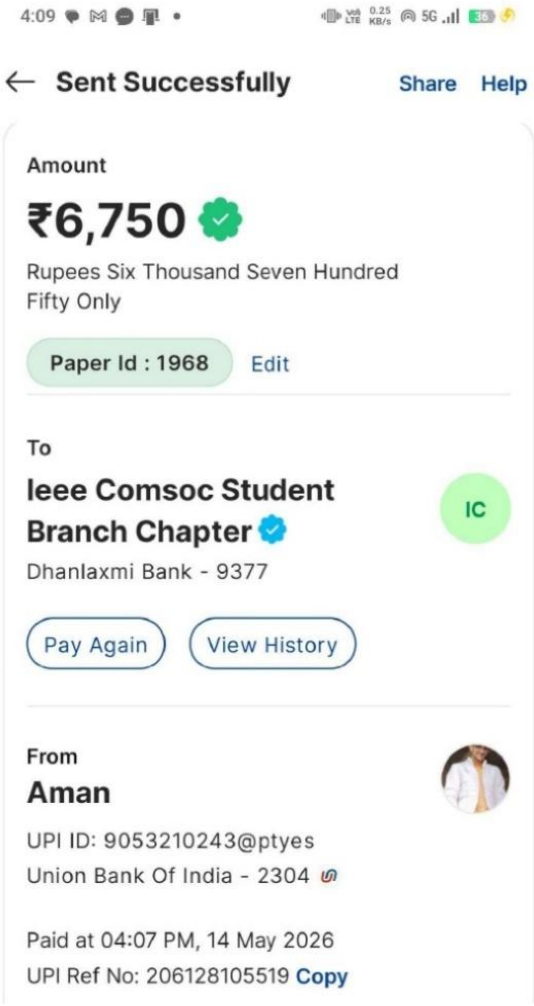
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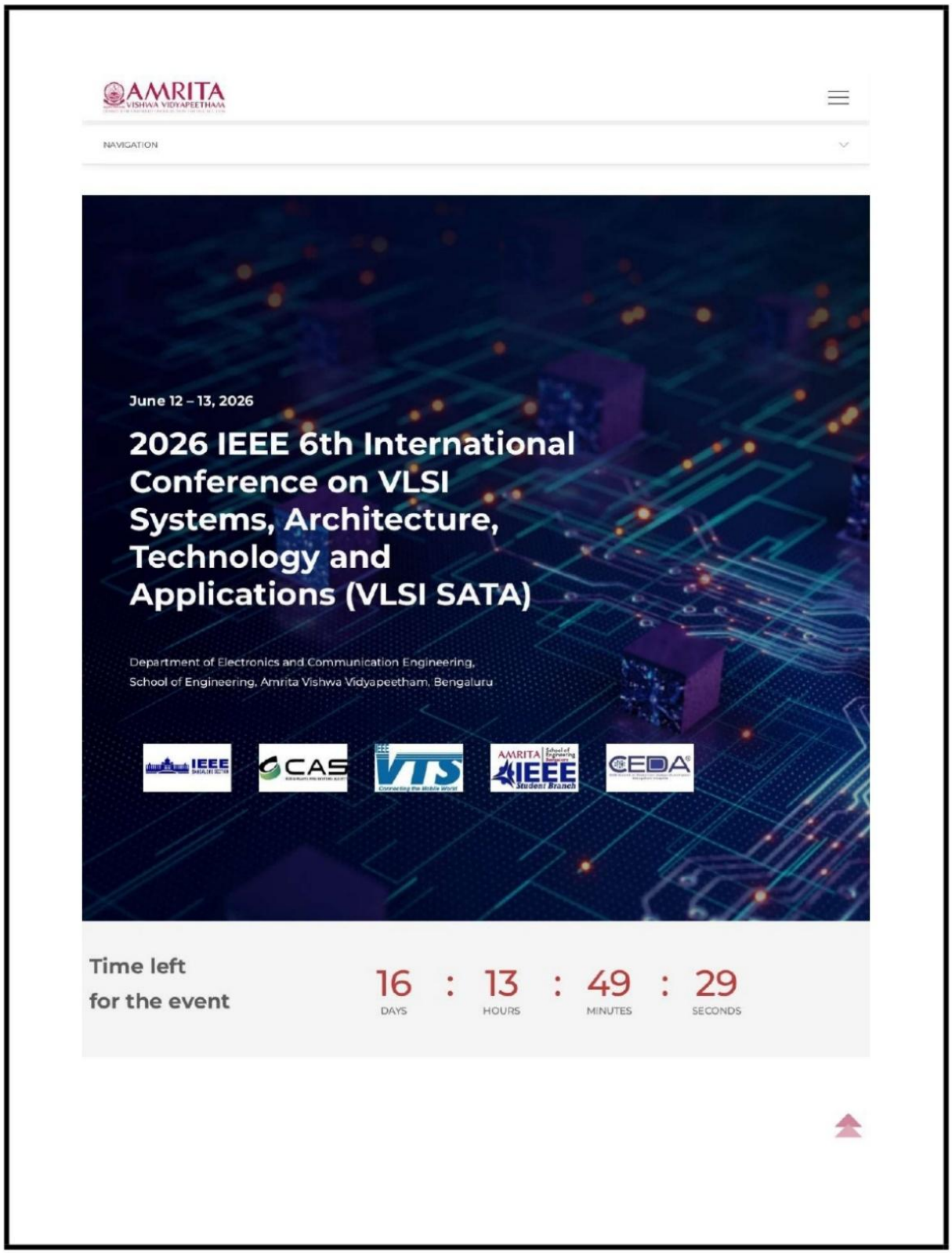
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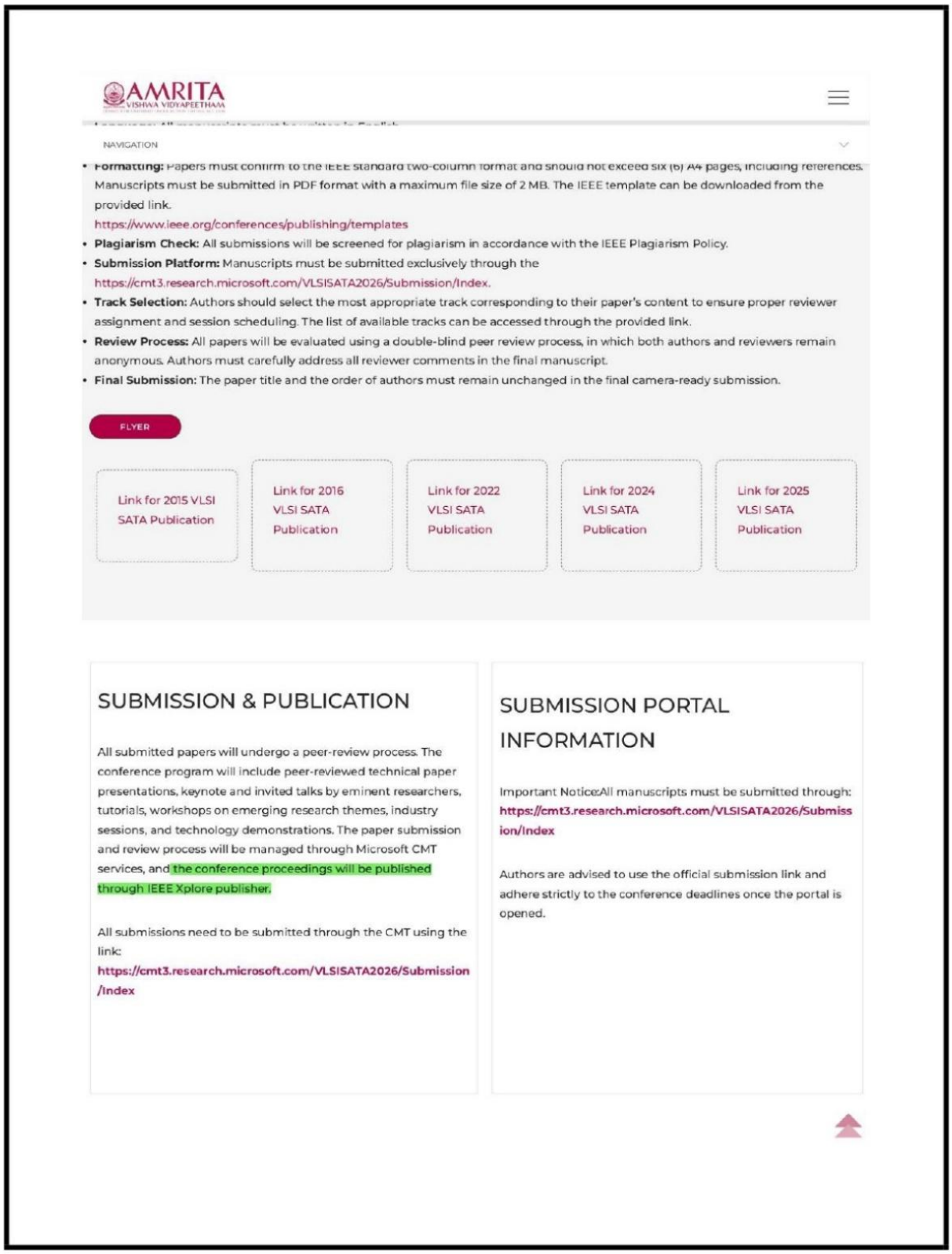
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