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MODELLING, ANALYSIS AND CONTROL OF NON-IDEAL SEPIC DC-DC CONVERTER

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I, Saurabh Batham, Roll No. 2K24/PES/08, student of M.Tech (Power Electronics & Systems), hereby declare that the project Dissertation titled "Modelling, Analysis and Control of Non-Ideal SEPIC DC-DC Converter" which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "Modelling, Analysis and Control of Non-Ideal SEPIC DC-DC Converter" which is submitted by Saurabh Batham, Roll No. 2K24/PES/08, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This thesis presents the design and comparative analysis of PI and PID controllers for a non-ideal SEPIC DC-DC converter intended for electric vehicle charging applications. The converter is configured to step up a 24V input to a regulated 48V output under Voltage Mode Control. A complete non-ideal small-signal model is derived by the State-Space Averaging technique, taking into account inductors, capacitors, switching devices and input source parasitic resistances, leading to a fourth-order control-to-output transfer function. Two systematic tuning methods, the classical Cohen-coon method and the model based Internal Model Control (IMC) approach, are investigated and compared. Both the controllers are implemented and evaluated with the help of circuit level simulation in MATLAB/Simulink. The performance is evaluated in terms of transient response characteristics such as rise time, settling time and overshoot and disturbance rejection capability under input voltage and load variations. The comparison reveals the relative merits of each tuning method and gives a systematic basis for controller choice in non-ideal DC-DC converter applications.

Keywords: *Battery Charging, Cohen-coon, Internal Model Control, PI Controller, SEPIC Converter, State Space Matrix.*

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LIST OF SYMBOLS

Parameters	Definitions
V_o	Output Voltage (V)
V_g	Input Voltage (V)
D	Duty ratio
T	Switching Period (s)
f_{sw}	Switching Frequency (Hz)
I_o	Output Current (A)
R	Load Resistance (Ω)
L_1, L_2	Converter inductors (H)
C_1, C_2	Converter capacitors (F)
r_{L_1}, r_{L_2}	Inductor ESR (Ω)
r_{C_1}, r_{C_2}	Capacitor ESR (Ω)
r_{sw}	MOSFET switch on resistance (Ω)
r_{sw}	Diode forward resistance (Ω)
V_d	Diode forward voltage drop
r_g	Source internal resistance (Ω)
I_{L_1}, I_{L_2}	Steady-state inductor currents
V_{C_1}, V_{C_2}	Steady-state capacitor voltages
K_p	Proportional Gain
K_I	Integral gain
K_d	Derivative gain
λ	Internal Model Control tuning parameter
ξ	Damping ratio of reduced plant
β	RHP zero coefficient

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

The world's energy landscape is changing at an accelerated rate with the imminent need to decarbonize transport and decrease reliance on fossil fuels. Among the various viable and promising alternatives, the use of Electric Vehicles (EVs) is leading the way for green urban transport and cutting down on carbon emission. EV adoption has witnessed an unprecedented and rapid growth worldwide as evidenced by the IEA-million's of electric vehicles have been deployed annually on roads of North America, Europe and Asia, with governments and public bodies setting strict policy and legislative targets on the phase out of internal combustion engines within the next two to three decades, boosting EV technology adoption for both passengers and commercial fleets.

Central to this EV-based paradigm is the need to develop smart and resilient power electronics systems. At a fundamental level, the process of charging an electric vehicle, be it at home, public charging points or fast charge stations, involves the transfer of electrical energy from available power source to electric vehicle battery pack in a controlled manner. This process is achieved using DC-DC converters, which are responsible for interfacing energy sources to battery packs, controlling the output voltage and current to meet battery's precise charging profile, thereby impacting the overall charging process efficiency, battery health, lifetime and the reliability of the charging infrastructure.[1]

The increased penetration of renewable energy sources, in particular solar photovoltaic (PV) systems, in EV charging, has made this power conversion chain more complex. The inherent variability of the input voltage, caused by variations in solar irradiance levels throughout the day, is a challenge faced by solar-powered EV charging stations which are increasingly being utilized as part of green energy initiatives. In such situations, the DC-DC converter should be capable of stepping up and stepping down the input voltage as necessary and still provide a stable output voltage that is suitable for charging the battery. The flexibility in this operation, coupled with the need for a non-inverted output polarity, implies that a converter topology choice is crucial for the design.

The Single-Ended Primary Inductance Converter, commonly referred to as SEPIC converter, is one of the most powerful and versatile topologies for the above application. The SEPIC topology is an extension of basic boost converter with two inductors, two capacitors, a single active switch and a diode to provide the non-inverting buck-boost feature. This type of topology is very useful in that it can adjust

the output voltage higher or lower than the input voltage, but still maintain the correct polarity as opposed to the more traditional buck-boost topology which generates a negative output voltage. The ability to convert voltage bidirectionally and maintain the battery's polarity is a practical feature for EV charging applications with widely varying source voltage and a desired battery voltage range.[2]

Beside its flexibility for voltage conversion, the SEPIC converter also provides a continuous input current waveform, which reduces the electromagnetic interference (EMI) generated at the input port and also reduces the filtering requirements. This is a very useful feature when interfacing with renewable energy sources where the current draw is smooth and uninterrupted, which is good for the source, be it a PV panel or a battery bank. Moreover, the dual active bridge and the CŪK converter variant with active switches are more complex in terms of gate drive circuitry and control implementation than the SEPIC single switch configuration.

However, to realise these theoretical advantages in a practical hardware implementation, a careful and rigorous approach to modelling and control design is necessary. One of the most common limitations observed throughout most of the existing literature on SEPIC converters is the assumption of idealised component models in the analysis and controller design. In the ideal model, inductors are assumed to be pure reactances with no series resistance, capacitors are assumed to be lossless, and switching devices are assumed to have zero voltage drop in the on-state and no switching losses. These simplifications are pedagogically convenient and analytically tractable, but they introduce a fundamental break between the theoretical model and the real-world hardware that any practical engineer must eventually confront.

In fact, all inductors wound on a ferrite or powder core will have a measurable DC resistance, also known as the winding resistance or DCR. Each electrolytic or ceramic capacitor employed as a part of the power stage has an Equivalent Series Resistance (ESR) that can lead to conduction losses and changes in the converter frequency response. The MOSFET switch has a fixed ON state resistance $R_{DS_{(on)}}$. The freewheeling diode has a current dependent voltage drop. These parasitic elements together significantly change the small-signal transfer function of the converter. The pole and zero locations are moving, the DC gain is changing and in some cases the damping characteristic of complex conjugate pole pairs is greatly affected, all of which have direct implications with respect to the stability and performance of any feedback controller designed with the ideal model.

It should not be mistaken that the deviation of ideal and non-ideal converter model is just an academic problem. If the controller is designed using an ideal model of the plant and it is applied to a practical converter with parasitics, the transient response might get degraded or stability margins decreased, or in worst-case scenario the closed loop system may become unstable. This mismatch between model and reality has serious practical implications in an application as critical as EV battery charging, where controller instability can lead to battery over voltage, thermal

runaway, or damage to the power electronics. Therefore, it is important that the small-signal model used for the controller design accurately portrays the non-ideal behaviour of the converter including the effect of all significant parasitic resistances.

1.2 Motivation

This thesis is motivated by precisely the need for a more realistic and practically grounded approach to the design of SEPIC converter control. The controllers designed in this work are inherently more representative of what would be expected to perform correctly on actual hardware, by including the non-ideal elements of the converter in the small-signal model from the start. This enhances the validity of the simulation results, but also provides a more reliable and honest basis for the comparison between the two tuning methodologies investigated. The converter is designed to step up a 24V input of a low-voltage DC bus or a partially discharged battery to a regulated 48V output, a specification directly aligned with the requirements of 48V EV systems and DC microgrid charging nodes.

Two different control techniques are compared in this thesis: the Cohen-coon PI tuning method and the internal model control (IMC) based PID approach; chosen to represent distinctly different design philosophies. Cohen-coon, representing an empirical process control-based approach, provides a simple closed-form expression for tuning the controller gain and integral time in relation to the characteristics of the plant's step response. On the other hand, the IMC-PID approach is a model-based design approach that uses the plant transfer function to provide an explicit analysis and design method that allows a more precise control of the closed-loop bandwidth and robustness. The use of both methods on the same non-ideal SEPIC plant and the assessment of their performance under identical conditions presents a rigorous and fair basis for comparative analysis – one that has direct impact on practical converter design decisions in the EV charging domain.

1.3 Literature Review

The control of DC-DC converters has been an active research area for several decades in the field of power electronics. This is motivated by the ever increasing demand for more efficient, compact and reliable power conversion systems in a broad spectrum of applications. The literature surrounding SEPIC converters, small-signal modelling, and PI/PID controller tuning is abundant and changing, and a thorough knowledge of prior work is crucial to interpreting the contributions of this thesis.

The SEPIC converter was first formally examined in early literature on non-inverting buck-boost configurations, and has since attracted significant academic and industrial attention due to its unique combination of voltage step-up and step-down functionality with a non-inverting output polarity. The early works established the basic operating principles of the SEPIC in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), drawing steady state voltage conversion ratios and identifying the main design trade-offs concerning component selection [1].

In further studies, this basic analysis was extended to take into account the effect of non-ideal components on the converter functionality, since the parasitic resistances, especially the ESR of capacitors and the winding resistance of inductors, affect the performance and the dynamic behaviour of the converter in a significant way [3].

Extensive literature exists regarding the use of SEPIC converter in battery charging and renewable energy interface. Many papers demonstrate that SEPIC converter topology can be beneficial for solar MPPT application, in which voltage of panel can be step-up and step-down according to the irradiation without limitations unlike those boost only topologies [3]. Lately, the application of SEPIC converter for auxiliary systems of EVs and low voltage DC microgrids is reported as it has a single switch topology, and continuous input current feature is attractive for regulated power supply [4].

Precise small-signal models for DC-DC converters are fundamental to any formal control design methodology. The most commonly used approach to obtain switching converter small-signal transfer functions is the State-Space Averaging (SSA) technique, proposed by Middlebrook and uK [5]. This method averages converter state equations over a full switching cycle and then linearizes the averaged model about a selected operating point to extract the control to output transfer function-describing the dynamic behavior of the system. This technique has been widely applied to the SEPIC converter with small-signal models varying depending on the number of non-ideal components to consider [6].

One particular characteristic that is common among all of the different SEPIC small-signal models described in the literature is the presence of a right half Plane (RHP) zero in the control to output transfer function. The RHP zero is inherent to the energy storing mechanism within the SEPIC and severely limits the achievable closed loop bandwidth. In fact, in practice the loop crossover frequency should be kept well below the RHP zero frequency to avoid degradation of phase which will push the system towards instability [3]. This is an well known characteristic limitation that has been researched and documented extensively within the power electronics control literature. The fourth order small signal transfer function for a non-ideal SEPIC converter with parasitic series resistances within the two inductors and two capacitors is also considered here and yields complex conjugate poles with a RHP zero, as documented in [4].

1.3.1 Classical Controller Tuning Methods

The Cohen-coon tuning was established by G. H. Cohen and G. A. Coon in 1953 [9] and was considered one of the earliest organized methods of tuning controller parameters for process control. The method is based on fitting the open loop step response of the plant and then deriving closed-form expressions to calculate P and I gains directly from the derived parameters. It was initially designed to work in process industries (reactors, loops for flow control and temperature), but it also attracted interest from outside of this field due to the fact that one does not require a detailed

plant model and only a good open loop step response which is also of interest to power electronics.[5]

However, applying Cohen-coon tuning to a converter, such as SEPIC in this case has significant drawbacks. The primary reason is that a high order non minimum phase plant is approximated as a system

, and this introduces a modelling error, which in particular at the high frequency end (where the higher order dynamics and RHP zero are most influential) can cause significant deviation of the P and I gain. Still Cohen-coon tuned controllers showed adequate transient response in some converter applications and served as a basis for comparison with more analytical tuning methods.[7][9]

The Ziegler-Nichols tuning also follows a similar theme of obtaining controller gains from little plant information (the ultimate gain and ultimate period determined using a relay test or the parameters at the inflection point of the step response). Compared to Cohen-coon it leads to more aggressive controllers with significant overshoot. Both methods have in common the lack of sophistication that they do not use the full information in frequency domain of a known plant transfer function [19].

In contrast, a very different framework for controller design based on the system's transfer function has been proposed by Garcia and Morari. In this Internal Model Control (IMC) approach, rather than estimating parameters from step response information, an internal model of the plant is built within the feedback loop, and the controller is obtained from the inverse of this model. The controller is often filtered by a low-pass filter that consists of a single tuning parameter, the closed loop time constant, which can be transformed in to the standard PID controller format as shown below [20].

IMC-PID has been used widely in process control, and more recently in power electronics. Its advantages over classic empirical methods (e.g., Ziegler-Nichols, Cohen-coon) are that there is a clear handle on the bandwidth, that for stable plants it inherently gives an internally stable controller, and that its transient performance often exhibits less overshoot than the classic controllers [20]. For applications such as converters, for which a small-signal model of the system may be available, IMC control naturally leverages the known system dynamics without having to make any approximations [12][16].

Improved phase margins and more predictable closed-loop behaviour compared to classical tuning have been reported in research on IMC-based DC-DC converter control, especially for plants with complex pole structures or non-minimum phase characteristics [16]. The key design issue remains the choice of λ, a smaller value yielding faster response at the expense of robustness, while a larger value trading off bandwidth in favour of stability margin. This explicit single-parameter tradeoff makes the IMC-PID framework practically appealing to the converter control design.

1.4 DC-DC Power Converters: Overview

Efficient conversion and control of electric power is an essential requirement in almost all fields of modern electronics and energy systems. It is essential to transfer power from the input source to the load at controllable voltage and current levels to ensure the performance, efficiency and reliability of consumer electronics, industrial motor drives, clean energy systems, electric vehicle charging stations and many other applications in direct current power system. In DC power system, the circuit element to achieve this function is called DC-DC converters, which is able to transfer an unregulated or a variable input voltage to a desired and regulated output voltage with high efficiency and low power consumption.

The operation principle of DC-DC converters is based on switched-mode power conversion. Compared to the linear regulators which dissipate the unwanted power in the form of heat to achieve voltage regulation, switched-mode converters employ high-frequency switching of the semiconductor switches, which are commonly MOSFETs, with storage elements, such as inductors and capacitors, to regulate the output voltage. The voltage conversion ratio of the converter is primarily determined by the duty cycle of the switching signal, which is defined as the ratio of the switching period when the switch is in the on-state. Closed-loop converter can maintain a stable regulated output under varying input and load conditions by modulating duty cycle in response of output voltage feedback.[1]

Power converter electronics can be broadly categorized into three types depending upon how the voltage conversion is achieved. The first type concerns the very common step-down or buck converter, which gives an output voltage less than the input, and is commonly used in point of load regulation. The second type involves the step-up or boost converter which is often used in battery management and renewables. The third type of power converter involves what are known as topologies such as the buck-boost, Ćuk, SEPIC and Zeta which either step up or step down, but employ differences such as output polarity, the continuity of the input current, the number of devices employed, and the ease of control. These types of non-isolated power conversion topologies are separated from the type of flyback, forward, push-pull and phase shifted full-bridge converters which include a high frequency transformer in the design, resulting in link galvanic isolation. From the standpoint of safe design, this link isolation is sometimes desirable, sometimes undesirable, but in safety critical applications, it is essential, and an important consideration.[5]

Several important parameters are used to evaluate the performances of a DC-DC converter. Among them perhaps the most significant one is the conversion efficiency which represents the ratio of the output power to the input power. The power dissipated in the converter leads directly to heat production, limited battery life in portable applications and the cost associated with running a large system [5]. Voltage regulation where the output voltage is kept constant across varying load currents and input voltages is equally crucial and the quality of the control system that regulates the output voltage depends on the quality of the feedback loop. Transient response

indicates how rapidly and how smoothly the converter can react to instantaneous changes in load or input. This is vital in applications where constant conditions are unusual such as EV charging. Additional performance characteristics such as output voltage ripple, EMI, power density and stress across individual components contribute to determining whether a particular topology and control scheme will be appropriate for a given application.

Electric Vehicles (EV) are progressively taking up more space in the transportation market, and the current converter technology is face with new and difficult challenges. For EV charging systems, it is essential that these DC-DC converters maintain a wide range of input voltage variations, especially in the case where the system is supplied by a solar or a battery bank. Furthermore, they are required to produce precisely regulated voltages and currents in compliance with the EV battery management system. The desire for converters capable of operating at wide-input ranges, having robust closed-loop controls under load or source variations and achieving high efficiencies throughout a wide operating range have generated a renewed focus on many converter topologies. It turns out that the SEPIC converter (which is elaborated in the next section) has become an appealing solution to this issue; it possesses some advantageous and flexible features that outperform existing boost or buck converters.

1.5 The SEPIC Topology: Significance and Challenges

The Single-Ended Primary Inductance Converter (SEPIC) topology enjoys a special niche among the many non-isolated DC-DC converter topologies available to the power electronics designer, since it can do both voltage step-up and step-down functions while maintaining a non-inverted output polarity [3]. SEPIC, first proposed by Slobodan Ćuk and Robert Middlebrook at the California Institute of Technology, has grown into a practically relevant converter architecture, studied extensively in academic literature and increasingly deployed in applications from batteries and battery management systems to green energy interfaces and EV charging front-ends.

The SEPIC converter in its standard configuration comprises of two inductors, two capacitors, a single switch typically a MOSFET and a diode. In Continuous Conduction Mode (CCM) the steady state voltage conversion ratio is V_{out}/V_{in}=D/(1-D) where D is the duty cycle of the main switch. This relation confirms that the SEPIC can generate an output voltage greater than or less than the input voltage depending on whether the duty cycle is above or below 0.5 and makes it suitable to be used in applications where the source voltage is variable.

An important advantage for practical purposes in SEPIC over buck-boost is the fact that the output voltage polarity is the same as the input. Conventionally the buck-boost results in a negative output voltage compared to input ground and thus the design may become complicated requiring additional level shifting circuit. SEPIC results in positive output voltage to the same input ground. This fact makes it useful for battery charging application where the voltage polarities are supposed to be the same. Another

advantageous feature is the input current is continuous in SEPIC due to the series inductor present at input side which further reduces EMI and hence the filtering requirement at source side. This is a useful feature when interacting with the energy sources like PV, etc. For EV charging.

But, SEPIC has some non-trivial challenges of control design despite these advantages. The small-signal control-to-output transfer function is of fourth order, due to the two inductors and two capacitors in the power stage. This introduces several poles in the open loop frequency response including a couple of complex conjugate poles which can be of quite low damping causing resonant peaking and associated phase degradation which has to be carefully handled in the feedback loop.

More importantly, the SEPIC small signal transfer function exhibits a right half Plane (RHP) zero behavior common to other boost-derived topologies. The RHP zero appears as a non-minimum phase behaviour when the duty cycle is increased to increase the output voltage, the output first dips before eventually rising; this behaviour produces a counter-intuitive transient response. In the frequency domain the RHP zero adds an additional phase lag which limits the achievable closed loop bandwidth. Controller design for such systems should limit the crossover frequency to well below RHP zero frequency to maintain adequate phase margin.

Non ideal SEPIC converters add another layer of complexity that ideal models simply don't capture. The parasitic ESR of both inductors and both capacitors shifts pole-zero locations away from where the ideal model predicts, introducing discrepancies that can affect stability margins and transient behaviour [7]. Thus, a controller designed for an ideal plant can behave very differently on a real converter. This is exactly the reason why we are using a non-ideal model for the controller synthesis.

1.6 Role of Controller Tuning in Converter Performance

The converter design process involves more than just selecting the right topology and sizing the passive parts. The other part which is also equally critical is the design of a feedback control system to accurately and stably maintain the desired output voltage over all the expected operating conditions.

The controller is the decision-making element in the closed-loop system. It constantly senses the output voltage, compares it to a reference and continuously adjusts the duty cycle to force the error to zero. Its effectiveness in this respect depends not only on its structure but more importantly on values of its tuning parameters making controller tuning a paramount concern in practical converter design.

The control strategy employed in this work is Voltage Mode Control in which the output voltage is sensed directly and fed back to compensator whose output modulates the duty cycle of the PWM signal driving the main switch. The compensator is usually a PI or PID controller. Its parameters, proportional gain K_p, integral gain K_i, and derivative gain K_d if any, determine the open loop frequency response of the

compensated plant. These parameters define the gain crossover frequency, phase margin, gain margin and ultimately the transient and steady-state behaviour of the closed-loop system.

Controller tuning affects converter performance across several dimensions. In the time domain, the proportional gain $K_p$primarily governs the speed of the initial response to a disturbance or setpoint change. A higher K_p generally produces a faster rise time, but risks increased overshoot and potential oscillation if set too aggressively. The integral gain K_i determines how quickly accumulated steady-state error is corrected, ensuring the output voltage settles at the reference value regardless of load or input variations [17]. Poorly tuned integral action, however, can lead to integrator windup, sluggish settling, or sustained oscillation. Where a derivative term is included, K_d provides anticipatory action by responding to the rate of change of the error, improving transient damping at the cost of increased sensitivity to high-frequency noise.

The loop compensation parameters have a direct impact on the closed-loop system's stability margins in the frequency domain. The phase margin, defined as the extra phase lag to reach the instability point at the gain crossover frequency, is the key performance index in power converter control loops. The widely recommended value in industry practice and academia for a stable system is 45° (minimum), while optimal values are typically between 45° and 60°. The system dynamic shows too much overshoot and ringing at low phase margin, while the response is too slow if the phase margin is chosen too conservatively and the converter cannot respond fast enough to load variations, which is of particular importance in EV charging where the demand may rise rapidly.

In addition to nominal performance, tuning parameters also provide an indication of the closed-loop system's robustness with respect to plant uncertainty and to changes in operating point. The controller tuned correctly should present adequate performance not only to the nominal operating point for which it was designed, but for the operating envelope of input voltage, load current, and component variations normally encountered. This robustness is especially important for a non-ideal SEPIC converter in which parasite parameters cause parameter dependencies, resulting in shifts in the small signal transfer function with operating point.

In this thesis two tuning methods are studied within this framework – the Cohen-coon method and the IMC-PID methodology are applied and discussed. The methods differ in terms of parameter selection from a methodical and calculative point of view. Their relative merits in the various forms of transient performance, frequency-domain stability and disturbance rejection are the main question addressed in this work through systematic simulation based analysis [7][8].

1.7 Research Gap

A major consistent shortcoming within the literature covered in the previous sections is the fact that the overwhelming majority of work regarding the tuning of PI and PID controllers for switched converters assumes a plant model which is largely idealised. Within the reviewed works components in the converter are ideal and parasitic resistances ignored, leading to reduced-order, simpler structure transfer functions of the plant. An uncertainty therefore exists with regard to controller tuning based on an ideal model which is also valid in real-world implementation - especially within safety conscious applications such as that of EV battery charging [3][5].

Moreover, most of the prior comparative works on controller tuning approaches for DC-DC converter have focused only under the nominal, steady-state operational condition. The tuned controllers behavior on practical disturbance such as sudden input voltage change and step change load has received less systematic study for SEPIC based EV charger [7][21]. In an real EV charger system, the input voltage will change as the grid quality change or the renewable source changes its output and also load will suddenly change during charging status transition [7][21].

This thesis directly deals with both the problems. A more practical and representative description of the plant is used for controller design by considering the non-ideal parasitic parts of the SEPIC converter from the start while designing the controllers. Moreover, input voltage and load disturbance tests are performed in addition to the nominal tests for both the Cohen-coon PI and IMC-PID controller to evaluate the controllers.

1.8 Objectives of the Thesis

The main goal of this thesis is to develop, implement, and compare PI and PID controllers for a non-ideal SEPIC DC-DC converter under Voltage Mode Control, which is specifically useful for electric vehicles charging applications. The particular objectives that are followed in this work are:

1. To obtain the non-ideal small-signal model of the SEPIC converter by including the parasitic resistances of the inductors and the equivalent series resistances of the capacitors into the State-Space Averaging framework, resulting in a fourth-order control-to-output transfer function that accurately represents the dynamics of a physically realisable converter and then design a Proportional-Integral (PI) controller for the non-ideal SEPIC plant, using the Cohen-coon tuning method. The system approximation is used to find the desired plant parameters, and the standard Cohen-coon closed form expressions are used to find the controller gains.
2. The Internal Model Control (IMC) based tuning approach is used for designing a Proportional-Integral-Derivative (PID) controller for the same plant, and the controller parameters are systematically derived from the plant transfer function and the closed loop tuning parameter λ is chosen such that the stability

margins are adequate then next to implement the two closed-loop control systems in MATLAB/Simulink. To validate the performance of the two closed-loop control systems by time-domain simulation of the entire non-ideal SEPIC converter under nominal operating conditions.

3. To evaluate and compare the performance of both the controllers in terms of key time domain metrics like rise time, settling time, percentage overshoot and steady state error and frequency domain stability indicators like gain margin and phase margin and then assess robustness and disturbance rejection capability of both the controllers by subjecting their closed-loop systems to step variations in source voltage and sudden changes in load resistance, and then comparing the resulting deviation and recovery characteristics.

CHAPTER 2

SEPIC CONVERTER: CIRCUIT AND MODELLING

2.1 Circuit Topology

The SEPIC converter considered in this work is composed of two inductors, $L_1$and L_2, two capacitors C_1 and C_2, a MOSFET switch, and a diode arranged in the conventional SEPIC topology. The input voltage source V_g supplies energy through the first inductor L_1, which is connected in series with the source side of the converter. The coupling capacitor C_1 links the junction between $L_1$and the MOSFET switch to one terminal of the second inductor L_2. The opposite terminal of L_2 is connected to the anode of the output diode. On the output side, the capacitor C_2 is placed in parallel with the load resistance R, while the cathode of the diode is tied to the output node to deliver power to the load [1][3].

The MOSFET switch connects the common junction of $L_1$and C_1 to ground. Its switching operation, controlled through the PWM duty ratio D, regulates the transfer of energy from the input stage to the output. In practical operation, the converter is capable of providing either step-up or step-down voltage conversion depending on the selected duty cycle, which makes the SEPIC topology quite flexible for wide input voltage applications.

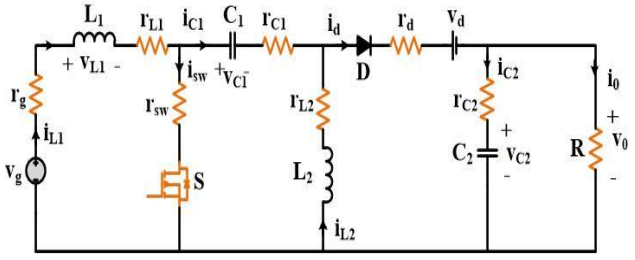

Fig. 2.1: Circuit Diagram of Non-Ideal SEPIC

Under steady-state CCM operation, the duty cycle and voltage conversion relationship of the SEPIC is given by:

$$\frac{V_o}{V_g} = \frac{D}{(1-D)} \tag{2.1}$$

For the converter specifications considered in this thesis an input voltage of 24 V and a desired output voltage of 48 V the required steady-state duty cycle is calculated as $D = 0.667$. This is reasonably close to the value of $D = 0.679$obtained from the complete non-ideal analysis, where the parasitic voltage drops across the resistive elements are also considered.

In an ideal SEPIC converter model, all passive elements are assumed to be lossless, while the switching devices are treated as ideal components. In practice however, actual converter components deviate from these assumptions and introduce several parasitic effects. Therefore, a detailed non-ideal converter model is considered in this thesis, incorporating the major loss and parasitic elements that are present in a practical implementation. The following non-idealities are included in the developed model:

Each inductor, L_1 and L_2, possesses ESR represented by r_{L_1} and r_{L_2}, respectively, corresponding to the DC resistance of the copper windings. In this design, both inductors are assumed to have the same ESR value of $r_L = 0.2\ \Omega$. Similarly, capacitors C_1 and C_2 include Equivalent Series Resistance (ESR), represented by r_{C_1} and r_{C_2}, which accounts for resistive losses associated with the dielectric material and terminal connections. Both capacitors have an ESR value of $r_C = 0.1\ \Omega$.

The MOSFET switch is modelled as having a finite on state resistance of $r_{sw} = 0.04\ \Omega$ and thus conduction losses are incurred during the ON interval of the switching cycle. The diode model includes forward resistance of $r_d = 0.1\ \Omega$ and forward voltage drop of $V_d = 0.7$ V, so that the model can represent the practical conduction behaviour of the rectifier diode. In addition, the input source is modelled with an internal resistance of $r_g = 0.08\ \Omega$ to take into account the finite source impedance of supply [2].

These non-ideal elements are included and the resulting small-signal model is much more accurate in a practical sense than the ideal case. The parasitic resistances contribute to additional damping of the resonant pole pairs, shift the locations of the zeros of the control-to-output transfer function and affect the overall DC gain of the converter. As a result, stability margins and transient response characteristics of the closed-loop system are changed. Because of this, the non-ideal model forms an important basis for realistic and practically relevant controller design.

The complete set of converter parameters used throughout this thesis is summarized in Table 2.1.

TABLE 2.1: SEPIC CONVERTER PARAMETERS

Parameters	***Value***
Input Voltage, V_g	24 V
Output Voltage, V_o	48 V
Load Current, I_o	2.53 A
Duty Cycle, D	0.679
Load Resistance, R	19.2 Ω
Capacitance, C = $C_1 = C_2$	35.36 μF

Parameters	***Value***
Capacitor Resistance, $r_c = r_{c_1} = r_{c_2}$	0.1 Ω
Inductance, $L = L_1 = L_2$	0.125 mH
Inductor Resistance, $r_L = r_{L_1} = r_{L_2}$	0.2 Ω
Switch- on Resistance, r_{sw}	0.04 Ω
Diode forward resistance, r_d	0.1 Ω
Source internal Resistance, r_g	0.08 Ω
Diode forward voltage drop, V_d	0.7 V
Switching Frequency, f	100 KHz
Current through Inductor L_1, I_{L_1}	6.087 A
Current through Inductor L_2, I_{L_2}	2.56 A
Voltage across Capacitor C_1, V_{C_1}	24 V
Voltage across Capacitor C_2, V_{C_2}	48 V

2.2 Operating Principle

The SEPIC converter operates through two distinct circuit states within each switching cycle, determined by the ON and OFF states of the MOSFET switch. Understanding the converter behaviour during these intervals is important for explaining how energy is transferred from the input source to the output load, as well as how the voltage conversion ratio is established through the switching duty cycle.

The converter operates in continuous conduction mode (CCM) at switching frequency f_s and duty cycle d, exhibiting two distinct states: switch-ON interval (dT_s) and switch-OFF interval ($(1-d)T_s$).

2.2.1 Switch On-Interval ($0 \leq t \leq dT_s$)

During Switch on mode, MOSFET is in ON state while the diode is reverse-biased. When the MOSFET switch is turned on, it presents a low-impedance path to ground. During this interval, the input voltage V_g is applied directly across inductor L_1, causing the current through L_1 to rise linearly at a rate determined by the inductor value and the applied voltage. Simultaneously, the coupling capacitor C_1 which has been charged to approximately the input voltage V_g during steady-state operation applies its stored voltage across inductor L_2, causing the current through L_2 to also rise linearly. The diode is reverse biased during this interval, isolating the output capacitor C_2 and the load from the input-side circuitry. The load current during this interval is therefore

supplied entirely by the charge stored in the output capacitor C_2, which discharges gradually into the load resistance R [1][2].

2.2.2 Switch Off-Interval ($dT_s \leq t \leq T_s$)

When the MOSFET switch is turned off, the energy stored in both inductors L_1 and L_2 must be released. Since inductor currents cannot change instantaneously, both inductors now forward bias the output diode and drive current into the output node. During this interval, the combined energy from L_1, L_2, and the coupling capacitor C_1 is transferred to the output capacitor C_2 and the load. The diode current is equal to the sum of the inductor currents in $L_1$and L_2, and both inductor currents decrease approximately linearly as stored energy is delivered to the output stage. During this interval, the coupling capacitor C_1also gets recharged, restoring its voltage to nearly $V_g$before the beginning of the next switching cycle [2][3].

2.2.3 Continuous Conduction Mode Operation

The converter implemented within this thesis is fully CCM, meaning the currents through inductors L_1 and L_2 do not reach zero prior to the next switching event within any complete switching cycle. There are several practical benefits to employing a fully CCM converter in this application. Since both inductor currents are continuous, both the switch and diode have a reduced peak current to handle and therefore have reduced conduction losses. This also helps alleviate the current handling requirements on the components. Also, the input current from the source is a smoother signal with reduced ripple, improving the source compatibility and EMI performance. The calculated parameters at this rated point were I_{L_1} = 6.087 A and I_{L_2} = 2.56 A, well above zero for CCM operation based on the rated converter parameters given in Table 2.1.

$$\frac{V_o}{V_g} = \frac{D}{(1-D)} \tag{2.2}$$

This yields an ideal duty cycle of 0.667 for the 24 V input and 48 V output, matching D=0.679 as calculated from the full non-ideal solution that takes the resistive drops through the parasitic elements into consideration.

2.3 State-Space Averaging and Transfer Function Derivation

The development of a controller for switching converters requires a mathematical model to describe the relationship between the input that affects the controller, i.e. The duty cycle d, and the output that is to be regulated, i.e. VOUT. Switch-mode converters are time-varying systems by nature of their switching operation, which means that linear control theory is not directly applicable. The State-Space Averaging technique, developed by Middlebrook and Ćuk, addresses this by replacing the time-varying switched circuit with a continuous averaged model that preserves the low-frequency dynamics of the converter while eliminating the switching ripple. This averaged model is then linearized around the nominal operating point to yield a linear time-invariant small-signal representation suitable for transfer function extraction and frequency-domain controller design.

2.3.1 State Variable Identification

The state variables of the SEPIC converter are chosen as the quantities associated with the energy storage elements the currents through the two inductors and the voltages across the two capacitors. Accordingly, the state vector is defined as:

$$x = [i_{L_1} \quad i_{L_2} \quad i_{C_1} \quad i_{C_2}]^T$$

These four state variables fully describe the dynamic state of the converter at any instant, and their evolution over time under each switching interval is governed by the KVL and KCL equations derived from the non-ideal circuit model.

2.3.2 MODE 1: During ON State

Applying KVL and KCL to the non-ideal SEPIC circuit during the switch on-interval, with all parasitic resistances included, yields the following set of first-order differential equations governing the evolution of the state variables:

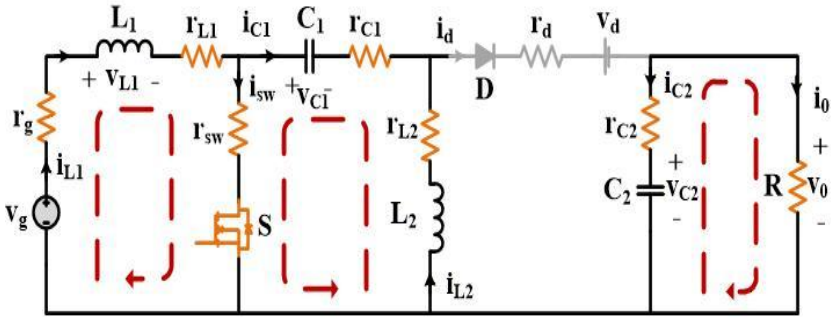

Fig. 2.2: Circuit Diagram of Non-Ideal SEPIC in *dT* mode

$$L_1 \frac{di_{L_1}}{dt} = v_g - i_{L_1} r_g - i_{L_1} r_{L_1} - i_{L_1} r_{sw} - i_{L_2} r_{sw} \tag{2.3}$$

$$L_2 \frac{di_{L_2}}{dt} = v_{C_1} - i_{L_2} r_{L_2} - i_{L_2} r_{C_1} - i_{L_2} r_{sw} - i_{L_1} r_{sw} \tag{2.4}$$

$$C_1 \frac{dv_{C_1}}{dt} = - i_{L2} \tag{2.5}$$

$$C_2 \frac{dv_{C_2}}{dt} = - \frac{v_{C_2}}{R + r_{C_2}} \tag{2.6}$$

$$v_o = v_{C_2} + i_{C_2} r_{C_2} \tag{2.7}$$

substituting the value of i_{C_2} ,we get

$$v_o = v_{C_2} \frac{R}{(R + r_{C_2})} \tag{2.8}$$

These equations constitute the on-state model, capturing the effect of inductor ESR r_{L_1} and r_{L_2}, switch on-resistance r_{sw}, capacitor ESR r_{C_1} and r_{C_2}, and source resistance rg on the circuit dynamics [3].

State and output equation thus obtained for dT mode from these equation's respectively are,

$$\begin{bmatrix} \dot{\imath}_{L_1} \\ \dot{\imath}_{L_2} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} -\frac{r_g + r_{L_1} + r_{sw}}{L_1} & -\frac{r_{sw}}{L_1} & 0 & 0 \\ -\frac{r_{sw}}{L_2} & -\frac{r_{L_2} + r_{C_1} + r_{sw}}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2(R + r_{C_2})} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_g \\ v_d \end{bmatrix} \quad (2.9)$$

$$[v_o] = \begin{bmatrix} 0 & 0 & 0 & \frac{R}{(R + r_{C_2})} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} \quad (2.10)$$

During dT mode,

$$A_1 = \begin{bmatrix} -\frac{r_g + r_{L_1} + r_{sw}}{L_1} & -\frac{r_{sw}}{L_1} & 0 & 0 \\ -\frac{r_{sw}}{L_2} & -\frac{r_{L_2} + r_{C_1} + r_{sw}}{L_2} & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2(R + r_{C_2})} \end{bmatrix} \quad (2.11)$$

$$B_1 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad \boldsymbol{E_1} = \begin{bmatrix} 0 & 0 & 0 & \frac{R}{(R + r_{C_2})} \end{bmatrix} \text{ and } F_1 = [0] \quad (2.12)$$

2.3.3 MODE 2: During OFF State

During the off-interval, the diode conducts and the switch is open. Applying KVL and KCL to this circuit configuration yields:

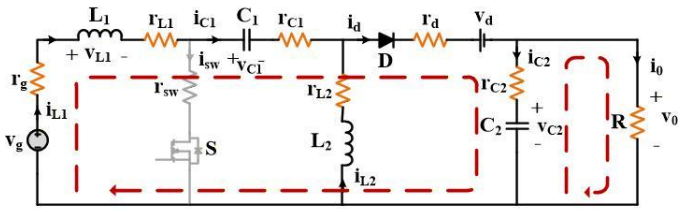

Fig. 2.3: Circuit Diagram of Non-Ideal SEPIC in (1-*d*)*T* mode

$$L_1 \frac{di_{L_1}}{dt} = v_g - i_{L_1}(r_g + r_{C_1} + r_{L_1} + r_D) - v_{C_1} - v_D - i_{L_2} r_D - v_{C_2} \frac{R}{R + r_{C_2}} \quad (2.13)$$

$$L_2 \frac{di_{L_2}}{dt} = -i_{L_1}(r_D + r_{L_2}) - v_D - i_{L_1} r_D - v_{C_2} \left(\frac{R}{R + r_{C_2}}\right) \quad (2.14)$$

$$C_1 \frac{dv_{C_1}}{dt} = - i_{L_1} \quad (2.15)$$

$$C_2 \frac{dv_{C_2}}{dt} = - \frac{v_{C_2}}{R + r_{C_2}} + - \frac{R\, i_{L_2}}{R + r_{C_2}} - \frac{R\, i_{L_1}}{R + r_{C_2}} \quad (2.16)$$

$$v_o = v_{C_2} + i_{C_2} r_{C_2} \quad (2.17)$$

$$v_o = v_{C_2} \frac{R}{(R + r_{C_2})} + \frac{R r_{C_2} i_{L_1}}{(R + r_{C_2})} + \frac{r_{C_2} i_{L_2} R}{(R + r_{C_2})} \quad (2.18)$$

Substituting value of i_{C_2} we get,

These equations capture the diode forward resistance r_D, forward voltage drop V_D, and the interaction of the output capacitor ESR with the load resistance during the freewheeling interval.

State and output equation obtained for (1-d) T mode respectively are,

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{C_1} \\ \dot{v}_{C_2} \end{bmatrix} = \begin{bmatrix} -\frac{r_g + r_{L_1} + r_{C_1} + r_d}{L_1} & -\frac{r_d}{L_1} & -\frac{1}{L_1} & -\frac{1}{L_1(R + r_{C_2})} \\ -\frac{r_d}{L_2} & -\frac{r_{L_2} + r_d}{L_2} & 0 & -\frac{1}{L_2(R + r_{C_2})} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{R}{C_2(R + r_{C_2})} & \frac{R}{C_2(R + r_{C_2})} & 0 & -\frac{1}{C_2(R + r_{C_2})} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & -\frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_g \\ v_d \end{bmatrix} \quad (2.19)$$

$$[v_o] = \begin{bmatrix} \frac{Rr_{C_2}}{(R + r_{C_2})} & \frac{Rr_{C_2}}{(R + r_{C_2})} & 0 & \frac{R}{(R + r_{C_2})} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{C_1} \\ v_{C_2} \end{bmatrix} \tag{2.20}$$

During (1-d) T mode,

$$A_2 = \begin{bmatrix} -\frac{r_g + r_{L_1} + r_{C_1} + r_d}{L_1} & -\frac{r_d}{L_1} & -\frac{1}{L_1} & -\frac{1}{L_1(R + r_{C_2})} \\ -\frac{r_d}{L_2} & -\frac{r_{L_2} + r_d}{L_2} & 0 & -\frac{1}{L_2(R + r_{C_2})} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{R}{C_2(R + r_{C_2})} & \frac{R}{C_2(R + r_{C_2})} & 0 & -\frac{1}{C_2(R + r_{C_2})} \end{bmatrix} \tag{2.21}$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & -\frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, E_2 = \begin{bmatrix} \frac{Rr_{C_2}}{(R + r_{C_2})} & \frac{Rr_{C_2}}{(R + r_{C_2})} & 0 & \frac{R}{(R + r_{C_2})} \end{bmatrix} \text{ and } F_2 = [0] \tag{2.22}$$

2.3.4 Linearization and Small-Signal Extraction

The averaged model is nonlinear due to the products of state variables and the duty cycle. To obtain a linear time-invariant model suitable for controller design, the averaged equations are perturbed around the DC operating point [1][2]. Each variable is expressed as the sum of its DC steady-state value and a small AC perturbation:

$$\bar{\imath}_{L1} = I_{L1} + \hat{\imath}_{L1} \tag{2.23}$$

$$\bar{\imath}_{L2} = I_{L2} + \hat{\imath}_{L2} \tag{2.24}$$

$$\bar{v}_{C1} = V_{C1} + \hat{v}_{C1} \tag{2.25}$$

$$\bar{v}_{C2} = V_{C2} + \hat{v}_{C2} \tag{2.26}$$

$$\bar{d} = D + \hat{d} \tag{2.27}$$

2.3.5 State Space Matrix

The two sets of state equations are combined by weighting the on-state model by the duty cycle D and the off-state model by (1−D), yielding the averaged state-space representation:

$$\hat{\dot{x}} = A\hat{x} + B\hat{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d} \tag{2.28}$$

With A_1, B_1 corresponding to the on-state and A_2, B_2 to the off-state coefficient matrices respectively [3].

Where,

$$A = A_1 D + A_2(1-D) = (A_1 - A_2)D + A_2 \tag{2.29}$$

$$B = B_1 D + B_2(1-D) = (B_1 - B_2)D + B_2 \tag{2.30}$$

Solving and substituting these values, state equation is written as,

$$\begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{C_1} \\ \hat{v}_{C_2} \end{bmatrix} =$$

$$\begin{bmatrix} -\frac{r_g + r_{C_1} + r_{L_1} + r_D - Dr_{C_1} - Dr_D + Dr_{sw}}{L_1} & -\frac{r_D - Dr_D + Dr_{sw}}{L_1} & \frac{D-1}{L_1} & \frac{R(D-1)}{L_1(R+r_{C_2})} \\ -\frac{r_D - Dr_D + Dr_{sw}}{L_2} & -\frac{r_D - Dr_D + Dr_{sw} + r_{L_2} + Dr_{C_1}}{L_2} & \frac{D}{L_2} & \frac{R(D-1)}{L_2(R+r_{C_2})} \\ -\frac{D-1}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ -\frac{R(D-1)}{C_2(R+r_{C_2})} & -\frac{R(D-1)}{c_2(R+r_{C_2})} & 0 & -\frac{1}{C_2(R+r_{C_2})} \end{bmatrix} \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{C_1} \\ \hat{v}_{C_2} \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{V_{C_1} + V_D + I_{L_1} r_{C_1} + I_{L_1} r_D + I_{L_2} r_D - I_{L_1} r_{sw} - I_{L_2} r_{sw}}{L_1} + \frac{RV_{C_2}}{L_1(R+r_{C_2})} \\ \frac{V_{C_1} + V_D - I_{L_2}(r_{C_1} - r_D + r_{sw}) + I_{L_1}(r_D - r_{sw})}{L_1} + \frac{RV_{C_2}}{L_2(R+r_{C_2})} \\ -\frac{I_{L_1} + I_{L_2}}{C_1} \\ -\frac{R(I_{L_1} + I_{L_2})}{C_2(R+r_{C_2})} \end{bmatrix} \hat{d} \tag{2.31}$$

Similarly, small signal model's output equation is given by,

$$\hat{y} = E\hat{x} + F\hat{u} + [(E_1 - E_2)X + (F_1 - F_2)U]\hat{d} \tag{2.32}$$

Where,

$$E = E_1 D + E_2(1-D) = (E_1 - E_2)D + E_2 \tag{2.33}$$

$$F = F_1 D + F_2(1-D) = (F_1 - F_2)D + F_2 \tag{2.29}$$

Then,

$$[\widehat{v_o}] = \begin{bmatrix} -\frac{Rr_{C_2}(D-1)}{(R + r_{C_2})} & -\frac{Rr_{C_2}(D-1)}{(R + r_{C_2})} & 0 & \frac{R}{(R + r_{C_2})} \end{bmatrix} \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{C_1} \\ \hat{v}_{C_2} \end{bmatrix} \tag{2.34}$$

CHAPTER 3
CONTROLLER DESIGN FOR CONVERTER

This section covers the designing of controller using the two above mentioned control techniques, their models and their implementation for the non-ideal SEPIC Converter, the calculation's.

3.1 Theoretical Background of Cohen-coon Method

The Cohen-coon tuning method was one of the first widely cited systematic approaches to PI and PID controller parameter selection. Developed by G. H. Cohen and G. A. Coon in 1953. The method, initially developed for process control applications in the chemical and manufacturing industries, provides closed-form analytical formulas for the proportional gain, integral time and derivative time of a controller, obtained from a limited set of parameters extracted from the open loop step response of the plant. It's simplicity is the reason for its lasting popularity since the method does not require a detailed mathematical model of the plant other than what can be deduced from a single open loop step test [9].

The Cohen-coon method uses various parameters where K is the static process gain, τ is the first order time constant and L is apparent dead time or the transport delay. These parameters jointly describe the plant steady-state gain, the speed of its dynamic response, and the time lag between the application of a control input and the beginning of a measurable output response. The Cohen-coon method although a simplification for higher order systems, reflects the essential input-output dynamics that control the tuning of a PI or PID controller and provides a sufficient basis for the Cohen-coon tuning formulas [7][9].

Two standard graphical techniques are used to identify the parameters from the open loop step response. The process gain K is determined directly as the ratio of the steady-state change in the output to the magnitude of the applied step variation in the control input. The dead time L is identified as the interval between the application of the step input and the instant at which the output response begins to show a noticeable deviation from its initial value. In practice, this is commonly approximated as the point where the response reaches nearly 10% of its total change.

The time constant τ is then evaluated using the 63.2% criterion, which states that for a first-order system, the output reaches 63.2% of its final steady-state value at a time equal to $L + \tau$ after the step input is applied. By determining these two points of time from the curve of the step response and determining values for the parameters, the whole description of the plant can be derived [19][20].

The controller parameters can be calculated directly once the parameters are identified using the tuning relations of Cohen-coon. In case of the PI controller the equations for K_p and T_i read:

$$K_p = (\frac{1}{K})(\frac{\tau}{L})(0.9 + \frac{L}{12\tau}) \quad (3.1)$$

$$T_i = L[\frac{\left(30+3\left(\frac{L}{\tau}\right)\right)}{\left(9+20\left(\frac{L}{\tau}\right)\right)}] \quad (3.2)$$

The integral gain K_i for the parallel controller configuration can then be expressed as

$$K_i = \frac{K_p}{T_i} \quad (3.3)$$

These equations all adhere to the general concept behind the Cohen-coon method, which is a closed-loop response with a quarter decay ratio of one. In other words the amplitude of successive oscillations decays by a factor of four per cycle during the step response. Cohen and Coon chose this value as a balance between fast and damped responses but it typically produces reasonably aggressive controllers with moderate amounts of overshoot in some applications [7].

A specific characteristic of the Cohen-coon method is its reliance on the ratio L/τ which represents the relative significance of the dead time to the lag in the plant dynamics. When L/τ is small, i.e. the plant lag dominates the dead time, the method tends to give controllers with larger proportional gains and smaller integral times leading to a faster and more responsive closed-loop response. Naturally as the value of L/τ increases the tuning relations become more conservative. This is to accommodate the increased difficulty associated with controlling systems with significant dead time. This inherent adaptation to the dead-time-to-lag ratio is one of the main features that differentiate the Cohen–Coon approach from simpler tuning techniques such as Ziegler–Nichols, and results in the broader application of the method across various plant characteristics.

3.2 Cohen-coon Method

The application of the Cohen–Coon tuning procedure to the non-ideal SEPIC converter begins with an open-loop step test performed in the MATLAB/Simulink environment. The converter is initially operated in open loop at the nominal operating condition, with an input voltage of $V_g = 24$ V and a duty cycle of $D_1 = 0.679$, corresponding to a steady-state output voltage of $V_{o1} = 44.83$ V. At $t_s = 0.05$ s, a small step increase is introduced in the duty cycle, increasing it to $D_2 = 0.699$, giving a step magnitude of $\Delta D = 0.02$. Following the applied step, the output voltage settles to a new steady-state value of $V_{o2} = 48.45$ V, resulting in a total output variation of $\Delta V_o = 3.62$ V.

3.2.1 Parameters for Cohen-coon

Process Gain (K) - The static process gain of the plant is evaluated as the ratio of the change in output voltage to the applied step change in the duty cycle:

$$K = \Delta V_o / \Delta D = 3.62 / 0.02 = 181 \text{ V/unit}$$

This value represents the DC sensitivity of the converter output with respect to variations in the duty cycle around the nominal operating point, and it acts as the primary scaling parameter in the Cohen–Coon tuning relations.

Dead Time (L) - The dead time is identified from the open-loop step response as the time elapsed between the application of the duty cycle step at ts = 0.05s and the point at which the output voltage first begins to rise measurably. From the step response, this delay is measured as:

$$L = 0.002505 \text{ s}$$

Time Constant (τ) - The time constant is determined using the 63.2% criterion. The output voltage value corresponding to 63.2% of the total step change is computed as:

$$y_{63.2} = V_{o1} + 0.632 \times \Delta V_o = 44.83 + 0.632 \times 3.62 = 47.12 \text{ V}$$

The time at which the output reaches this value is identified from the step response curve, and the time constant is extracted as:

$$\tau = t_{63.2} - t_s - L = 0.0012613 \text{ s}$$

Cohen-coon PI Gain Calculation-

Substituting the identified system parameters into the Cohen-coon PI tuning expressions, with $L/\tau = 0.002505 / 0.0012613 \approx 1.9868$:

Proportional Gain:

$$K_p = (1/181) \times (0.0012613/0.002505) \times (0.9 + 1.9868/12) \approx 0.00296$$

Integral Time:

$$T_i = 0.002505 \times [(30 + 3 \times 1.9868) / (9 + 20 \times 1.9868)] \approx 0.0018488 \text{ s}$$

Integral Gain:

$$K_i = \frac{K_p}{T_i} = 0.00296 / 0.0018488 \approx 1.60$$

The practically implemented controller gains, after minor adjustment to account for simulation convergence, are:

$$K_p = 0.002988, K_i = 1.594$$

These gains define the Cohen-coon PI controller applied to the non-ideal SEPIC converter in the closed-loop simulation, the configuration and results of which are presented in the subsequent sections.

3.3 Internal Model Control: Principle and Structure

The Internal Model Control framework, first formalised by Garcia and Morari in 1982, represents a significantly distinct philosophy in feedback controller design as compared to classical tuning methods. Instead of identifying controller parameters from a limited characterisation of the plant step response, the IMC approach explicitly incorporates a theoretical framework of the plant in the structure of the control loop and analytically derives the controller from this model. This direct use of plant knowledge gives the IMC framework a systematic and transparent character the designer has a clear and intuitive handle on how the controller parameters are associated with the plant dynamics and the intended closed-loop behaviour [16].

3.3.1 IMC Control Structure

In the basic IMC control structure, the actual plant G(s) and an internal model GM(s) are in parallel in the feedback loop. The controller Q(s) is applied to the difference between the reference signal and the output of the internal model instead of the direct plant output error. If the internal model is exactly the same as the actual plant, i.e., GM(s) = G(s), the feedback signal from the internal model cancels exactly the plant output, and the loop effectively opens. Ideally, the closed-loop response is completely specified by the controller Q(s) and the plant, with no feedback correction. In practice, model mismatch and disturbances provide a non-zero feedback signal to trigger corrective action, thus providing robustness to uncertainty [18][21].

The IMC controller $Q(s)$ is designed as the inverse of the invertible portion of the plant model, combined with a low-pass filter $F(s)$ to ensure both realizability and robustness of the controller:

$$Q(s) = [GM^{-}(s)]^{-1}.F(s) \tag{3.4}$$

Where $G_M^{-}(s)$ represents the minimum-phase invertible part of the plant model, while $F(s)$ denotes the IMC filter used to shape the closed-loop response characteristics [18]. The equivalent feedback controller $C(s)$, which can be implemented within a standard unity feedback structure, is then obtained from $Q(s)$ using the transformation:

$$C(s) = \frac{Q(s)}{[1 - Q(s).GM(s)]} \tag{3.5}$$

This formulation allows the IMC-based controller to be directly implemented in a conventional feedback loop without requiring any structural changes to the overall control architecture.

3.3.2 Plant Factorization for Non-Minimum Phase Systems

The non-ideal SEPIC converter as derived in Chapter 2, has a right-half plane zero in its transfer function – it is a Non-Minimum Phase Structure System (NMPSS). Due to the existence of the RHP zero, the complete plant model cannot be inverted directly. The inversion of a RHP zero would result in an unstable pole in the controller,

and hence an internally unstable closed-loop system [21]. This is elegantly handled in IMC framework by factorising the plant. The plant model is factorised in two parts:

$$GM(s) = GM^{-}(s) \cdot GM^{+}(s) \tag{3.6}$$

Here, $G_M^+(s)$ contains the non-invertible right-half-plane (RHP) zero component, while $G_M^-(s)$ represents the minimum-phase invertible part of the plant. During the controller design process, only $G_M^-(s)$ is inverted, whereas $G_M^+(s)$ remains within the loop and its influence on the closed-loop response is handled through appropriate filter design. For the SEPIC converter plant, the factorization can be expressed as:

$$GM^{+}(s) = (-\beta s + 1)$$

$$GM^{-}(s) = \frac{K_p}{(\tau^2 s^2 + 2\xi\tau s + 1)} \tag{3.7}$$

Where the RHP zero is represented by the coefficient $\beta > 0$.

3.3.3 Filter Selection for NMPSS

The selection of the IMC filter $F(s)$ plays an important role in the control of non-minimum phase stable systems (NMPSS). A conventional first-order filter of the form $1/(1 + \lambda s)$ is generally inadequate for second-order plants containing RHP zeros, since it does not provide sufficient roll-off characteristics or adequate phase compensation. Therefore, for the SEPIC converter considered in this work, the proposed second-order filter $F_3(s)$ is adopted:

$$F_3(s) = \lambda^2 [\frac{(\beta + 2\lambda)}{(1 + \lambda s)}] \tag{3.8}$$

This filter introduces a single tuning parameter, λ, referred to as the closed-loop time constant, which determines the basic trade-off between response speed and robustness of the closed-loop system. A smaller value of λ results in a faster response but reduced robustness, whereas a larger value leads to a more conservative controller with improved stability margins. The complete IMC-PID parameter set is obtained from λ and the extracted plant parameters using closed-form relations, making λ the primary tuning variable in the overall design procedure.

3.4 PID Derivation for the SEPIC Plant

The IMC-PID controller design for the non-ideal SEPIC converter follows a systematic sequence of steps, namely: plant order reduction, parameter extraction, selection of λ, IMC gain computation, and finally conversion into the standard PID structure. Each of these steps is discussed below using the numerical values obtained for the SEPIC converter parameters listed in Table 2.1.

3.4.1 Model Order Reduction

The fourth-order SEPIC converter transfer function derived in Section 2.3 is first reduced to a second-order approximation using the truncation method. In this approach, only the lower-order terms up to s^2 are retained in both the numerator and denominator polynomials, while the $s^4$and s^3 terms are neglected. This reduction is justified by the fact that the higher-order terms contribute minimally to the low-frequency dynamics that govern the controller design. The validity of the reduction was verified in MATLAB by comparing the step responses of both the original fourth-order and reduced second-order models, confirming closely matching transient behaviour and identical DC gains [13][14][15]. The resulting second-order reduced model is:

$$G_r(s) = \frac{1.369 \times 10^{-6}s^2 - 0.001853s + 161.6}{2.748 \times 10^{-6}s^2 + 0.003407s + 204} \tag{3.9}$$

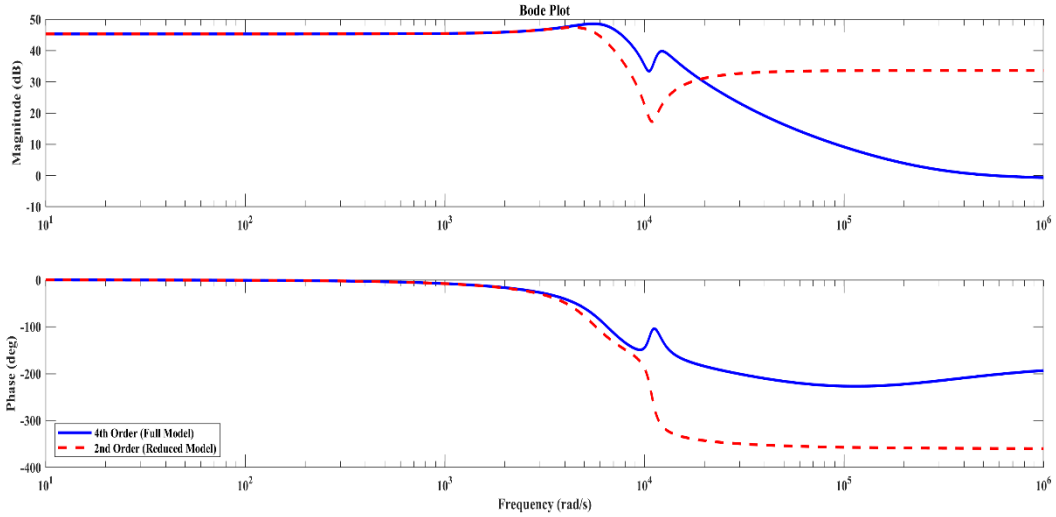

Fig. 3.1: Bode Plot comparison between 4th order and 2nd order reduced transfer function

The Bode plots of both models match closely in the low frequency region where the controller operates below 2000 rad/s. Since the designed controller have crossover frequencies well below this, the 2nd order reduction is valid for controller design purposes.

3.4.2 Extraction of Plant Parameters

The reduced model is expressed in the standard NMPSS second-order form:

$$G_p(s) = K_p \frac{(-\beta s+1)}{(\tau^2 s^2+2\xi\tau s+1)} \tag{3.10}$$

The four plant parameters are extracted by normalizing the numerator and denominator by their respective constant terms. Dividing the denominator by 204 and comparing with $\tau^2 s^2 + 2\xi\tau s + 1$:

$$\tau^2 = 2.748\times10^{-6}/204 = 1.347\times10^{-8} \Longrightarrow \tau = 1.161\times10^{-4}\ \text{s} \tag{3.11}$$

$$2\xi\tau = 0.003407/204 = 1.670\times10^{-5} \Longrightarrow \xi = 0.0719 \quad (3.12)$$

Dividing the numerator by 161.6 and comparing with $K_p(-\beta s + 1)$:

$$K_p = 161.6/204 = 0.7922 \quad (3.13)$$

$$\beta = 1.147\times10^{-5}/0.7922 = 1.447\times10^{-5}\ \text{s} \quad (3.14)$$

Since $\beta > 0$, the presence of the RHP zero at $s = +1/\beta = +69{,}143$ rad/s is confirmed, consistent with the open-loop analysis of Section 2.4.

3.4.3 IMC-PID Parameter Calculation

Substituting $\lambda = 0.08$ s and the extracted plant parameters into the F_3 filter IMC-PID formulas:

Proportional gain of IMC controller:

$$K_c = \frac{2\xi\tau}{[K_p(\beta + 2\lambda)]} = \frac{(2 \times 0.0719 \times 1.161\times10^{-4})}{[0.7922 \times (1.447\times10^{-5} + 0.16)]} = 1.317\times10^{-4} \quad (3.15)$$

Integral time constant:

$$\tau_I = 2\xi\tau = 2 \times 0.0719 \times 1.161\times10^{-4} = 1.670\times10^{-4} \quad (3.16)$$

Derivative time constant:

$$\tau_D = \tau/(2\xi) = \frac{1.161\times10^{-4}}{(2\times0.0719)} = 8.071\times10^{-4} \quad (3.17)$$

Derivative filter time constant:

$$\tau_f = \frac{\lambda^2}{(\beta+2\lambda)} \quad (3.18)$$

Conversion to Standard PID Gains,

The IMC controller takes the standard form:

$$C(s) = K_c \times \frac{(\tau_I.\tau_D.s^2+\tau_I.s+1)}{[\tau_I.s.(1+\tau_f.s)]} \quad (3.19)$$

Expanding into parallel PID form $C(s) = K_p + \frac{K_i}{s} + \frac{K_d.s}{(1+\tau_f.s)}$, the standard PID gains are obtained as:

$$K_p = K_c = 3.521\times10^{-3} \quad (3.20)$$

$$K_i = \frac{K_c}{\tau_I} = 3.521\times10^{-3} / 1.240\times10^{-3} = 2.8 \quad (3.21)$$

$$K_d = K_c \times \tau_D = 3.521\times 10^{-3} \times 2.621\times\times 10^{-4} = 9.229\times 10^{-7} \quad (3.22)$$

The complete controller transfer function with all numerical values substituted is:

$$C(s) = \frac{1.144\times10^{-10}s^2+4.367\times10^{-7}s+3.521\times10^{-5}}{5.256\times10^{-9}s^2+1.240\times10^{-4}s} \quad (3.23)$$

The stability margins of the compensated loop L(s) = C(s)·G(s) were evaluated using the Bode plot of the loop gain with the fourth-order plant. The results confirm that the IMC-PID controller meets all design requirements [22].

3.5 CLOSED LOOP SYSTEM CONFIGURATION

The closed-loop simulation environment for both controllers is implemented in MATLAB/Simulink using a switched-mode circuit-level model of the non-ideal SEPIC converter. Rather than using the linearized small-signal transfer function for simulation, the complete non-linear switching circuit is modelled in Simulink, capturing the full switching behaviour of the converter including the effects of all parasitic resistances identified in Section 2.1. This method ensures that the simulation results are representative of the actual behaviour of the converter under realistic operating conditions rather than only the simplified dynamics of the linearized model.

3.5.1 Power Stage Model

The SEPIC power stage is modeled with ideal switching devices and the parasitic effects are modeled with series resistance elements of the respective components. The inductors L_1 and L_2 are modelled by the series connection of the winding resistances r_{L_1} and r_{L_2} . Similarly, both the capacitors C_1 and C_2 have their individual ESRs r_{C_1} and r_{C_2}. The MOSFET switch is modeled by a finite on-state resistance r_{sw} and the diode model includes the forward resistance r_d and the forward voltage drop V_d. The source resistance r_g is also connected in series with the input voltage source. All component parameters are chosen according to the values in table 2.1 in order to guarantee a direct consistency between the theoretical model and the simulation implementation.

3.5.2 Feedback Control Loop

The closed loop control framework is based on the common Voltage Mode Control scheme. The converter output voltage is sensed and compared to the reference voltage of 48V at an error summing junction. The resulting error signal is fed to the controller block (either the Cohen-coon conventional PI controller or the IMC-PID controller) according to the simulation case. The duty cycle command is the output of the controller. This duty cycle signal is passed through a saturation block that saturates the duty cycle to the physically meaningful range of 0 to 1. This prevents integrator windup and ensures that a valid input is always fed to the PWM modulator. The PWM

block receives the duty cycle command and creates the gate drive signal to the MOSFET switch. The feedback loop is now closed [6].

For the Cohen–Coon implementation, the controller block uses a parallel-form PI controller with $K_p = 0.002988$and $K_i = 1.594$. In the IMC-PID configuration, the same position of the controller is substituted by a parallel form PID controller with a derivative filter, with parameters $K_p = 3.521 \times 10^{-3}$, $K_i = 2.8$, $K_d = 9.229 \times 10^{-7}$, and filter time constant $\tau_f = 3.999 \times 10^{-2}$ s. In both cases, the power stage model and all other simulation parameters are kept the same, and therefore any differences in performance that are observed between the two controllers can be purely attributed to the controller tuning method, rather than any differences in the plant or simulation setup.

3.5.3 Disturbance Testing Configuration

For robustness evaluation, the Simulink model incorporates two additional signal injection points that are activated independently for disturbance testing. Input voltage variation is introduced using a Signal Builder block connected to the input source, which imposes a step change in V_{in} at a specified simulation time while the controller attempts to maintain the output at 48V. Load variation is tested by switching the load resistance R between two values at a specified time using an ideal switch, simulating a sudden throw-on or throw-off of load. In both cases the core power stage and controller configuration remain unchanged, with only the disturbance signal being activated. For nominal step response evaluation, both disturbance inputs are disabled and the converter operates with a fixed 24V input and constant 19.2Ω load throughout the simulation [17].

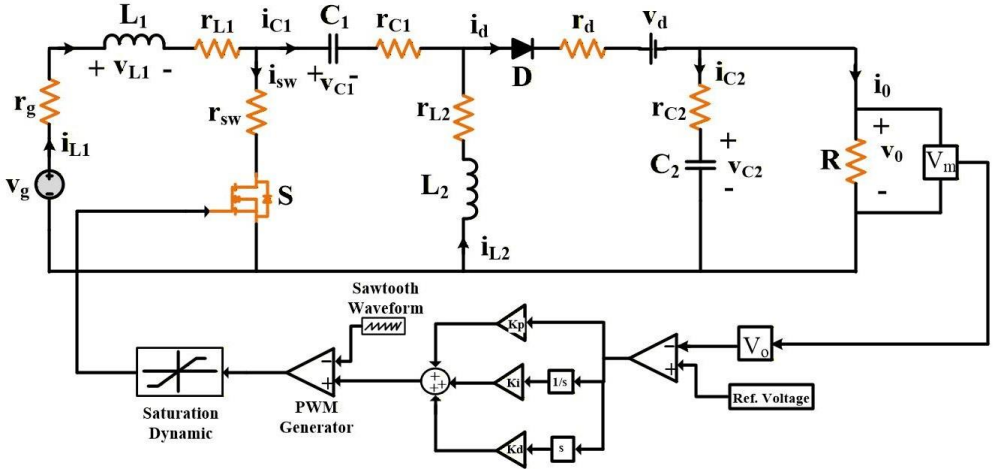

Fig. 3.2: Closed Loop Non-Ideal SEPIC Converter

CHAPTER 4
RESULTS AND DISCUSSION

4.1 Simulation Results

The closed-loop simulation of both the Cohen-coon PI and IMC-PID controllers is carried out in MATLAB/Simulink using the non-ideal SEPIC converter model described in Chapter 2. Three categories of tests are performed for each controller: nominal step response, source voltage disturbance, and load disturbance. The results obtained from the developed models are presented in this section through the output voltage waveforms along with extracted performance indices. A more detailed comparative discussion and interpretation of the results is provided later in this Chapter.

4.1.1 Basis of Comparison

The comparative assessment presented in this chapter is done in a strictly controlled and consistent manner, such that any differences in performance between the two controllers are due only to the tuning methodology and not to differences in the plant, operating conditions or simulation setup. The Cohen-coon PI and IMC-PID controllers are both implemented on the same non-ideal SEPIC converter model as described in Chapter 2. All component parameters are the same as those described in Table 2.1 and are not changed between simulation runs. The nominal input voltage, load resistance, switching frequency, and reference output voltage are used for the baseline comparison. The same disturbance profiles are applied to both controllers for robustness evaluation.

The performance of the two controllers is tested in three main test cases. The first is the nominal step response test, which measures how well each controller can drive the converter output from zero initial conditions to the regulated 48V reference under normal operating conditions. This test characterizes the transient response quality of each controller in terms of the speed and smoothness in reaching the desired output voltage. The second scenario is the source voltage disturbance test. Here a sudden drop of the input voltage is introduced in the middle of the simulation, in order to assess how well each controller rejects disturbances on the input side and brings back the regulated output. The third scenario is the load disturbance test that applies step changes in the connected load resistance to evaluate the controller's ability to maintain regulation under varying output power demand a condition directly representative of the dynamic load profile experienced in EV battery charging applications.

In addition to these dynamic tests, the diode and MOSFET current waveforms seen under closed-loop operation are used to qualitatively investigate the switching device stress behaviour of both controllers. The results of all three test scenarios are discussed and presented in the subsequent sections, ending in a comprehensive comparative summary in Section 4.5.

At the beginning, it is important to note that both controllers generate the same steady state error of 0.7131V under nominal operating conditions. As shown in Section 3.6, this offset is the sum of the resistive voltage drops of the non-ideal parasitic elements of the converter. It is therefore a limitation at the plant level and not a deficiency of either controller. Therefore the steady-state error is not regarded as a discriminating factor in the comparative study. The performance evaluation is focused on the dynamic performance features that are differentiating between the two tuning strategies.

4.2 Nominal Step Response

The nominal step response test is carried out to evaluate the closed-loop performance of each controller under standard operating conditions, with a fixed input voltage of $V_g = 24$ Vand a constant load resistance of $R = 19.2\ \Omega$. The converter begins from zero initial conditions, after which the controller regulates the output voltage from 0 V toward the reference value of 48 V. The corresponding output voltage responses for the Cohen–Coon PI and IMC-PID controllers are presented in Fig. 4.1 and Fig. 4.2, respectively.

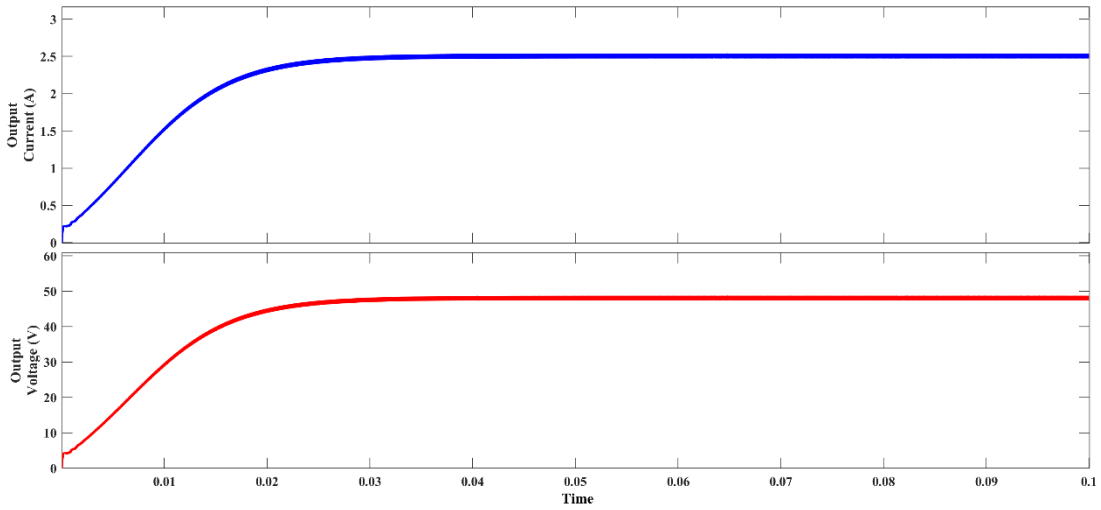

Fig 4.1 Cohen-coon nominal step response plot

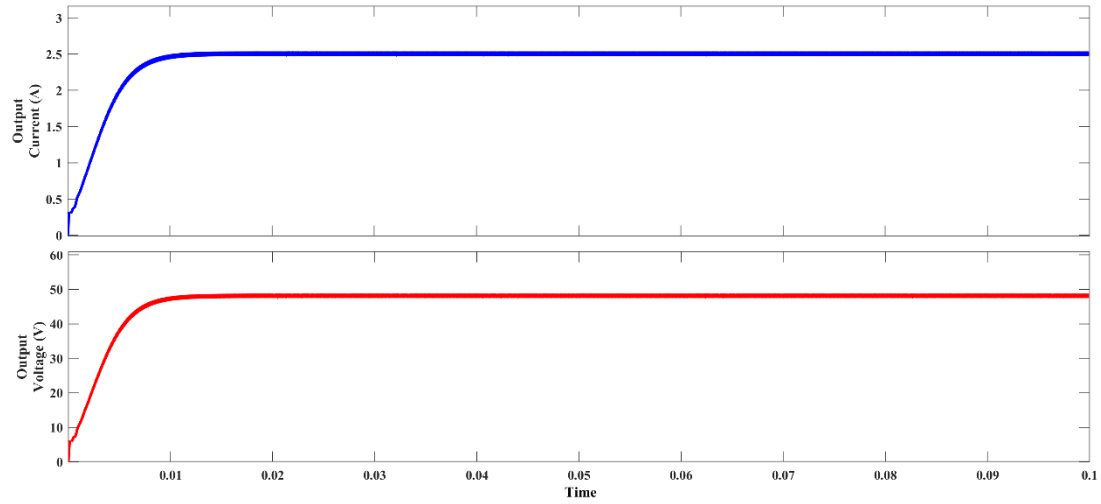

Fig 4.2 IMC-PID nominal step response plot

The rise time of the Cohen-coon PI controller is 0.016858 s and the settling time is 0.030687 s. The percentage overshoot is 1.5000% and the peak output voltage is 48.47V. The IMC-PID controller had a rise time of 0.010856 s, a settling time of 0.019287 s, a percentage overshoot of 1.4972%, and a peak output voltage of 48.53V. The overshoot levels of both controllers are very close, which indicates similar damping in the closed-loop transient response.

Both controllers reach a final output voltage of approximately 48.71V with a steady state error of 0.7131V in both cases. This similar steady-state offset is not a deficiency in the integral action of either controller, but rather is an indication of the cumulative effect of non-ideal parasitic voltage drops across the inductor winding resistances, capacitor ESR values, switch on-resistance, and diode forward voltage drop present in the model of the converter. These resistive losses give rise to a common inherent steady-state drift of both controllers, since this is a property of the plant and not a controller specific phenomenon.

The performance indices of both controllers under normal operating conditions are shown in Table 4.1.

Table 4.1: Nominal Step Response Performance Metrics

Metric	***Cohen-coon***	***IMC-PID***
Rise Time	0.016858 s	0.010856 s
Settling Time	0.030687 s	0.019287 s
Peak V_{out}	48.47 V	48.53 V
Steady State Error	0.7131 V	0.7131 V

The transient performance of both controllers under nominal step response conditions reveals meaningful differences in dynamic behavior, despite similar overshoot levels observed in both cases. The IMC-PID controller gives a rise time of 0.010856 s and the Cohen-coon PI controller gives a rise time of 0.016858 s. This is an improvement in the rise time of about 35.6%. Similarly, the IMC-PID controller settles in the ±2% regulation band in 0.020287 s, whereas the Cohen-coon PI controller takes 0.030687 s about 51.3% longer to settle. Both controllers show nearly the same percentage overshoot values of 1.4972% and 1.5000% respectively, which shows that neither controller introduces excess oscillatory behaviour during the startup transient despite the difference in their tuning philosophies.

This is a direct consequence of the model based design approach of the IMC-PID controller, which provides a faster transient response. The IMC framework determines the controller parameters analytically from the plant transfer function, with the tuning process directly targeting a desired closed-loop time constant through the parameter λ. By making explicit use of the plant model, the IMC-PID controller is able to achieve a more deliberately shaped closed-loop response than the Cohen–Coon approach. In contrast, the Cohen–coon method derives its controller gains from an approximation of the plant and is based on the empirical quarter-decay-ratio criterion. As a result, the approximation does not fully capture the higher-order dynamics and

complex pole characteristics of the non-ideal SEPIC converter, leading to more conservative controller gains and, consequently, a slower transient response.

A significant observation is the similar overshoot of the two controllers. There is a big difference in rise time and settling time but both controllers keep the overshoot below 1.5% which is well within the acceptable range for voltage regulation in battery charging applications where the excessive overvoltage must be avoided. This demonstrates that the slower response of the Cohen-coon controller is not caused by poorer stability or more oscillatory behaviour. Instead, the conservative tuning appears primarily as a slower transient response, which is a less critical shortcoming from the point of view of practical implementation.

For EV charging applications, the faster transient performance achieved by the IMC-PID controller has clear practical benefits. When the charger is first connected to the vehicle battery, the converter must establish the required output voltage as quickly as possible to initiate the charging process. Reduced rise and settling times therefore translate into shorter startup delays and a faster transition to normal charging operation. In high-utilization environments, such as public fast-charging stations, improvements in dynamic response can contribute to a more efficient overall charging cycle.

4.3 Disturbance Rejection and Robustness

4.3.1 Source Voltage Disturbance Response

The source voltage disturbance test is used to evaluate each of the controllers ability to hold the regulated output voltage against a sudden reduction of input supply voltage. A step reduction in input voltage is applied at t = 0.04s while the controller remains active in closed loop. The output voltage responses of both controllers to this disturbance are shown in Fig. 4.3 and Fig. 4.4 respectively.

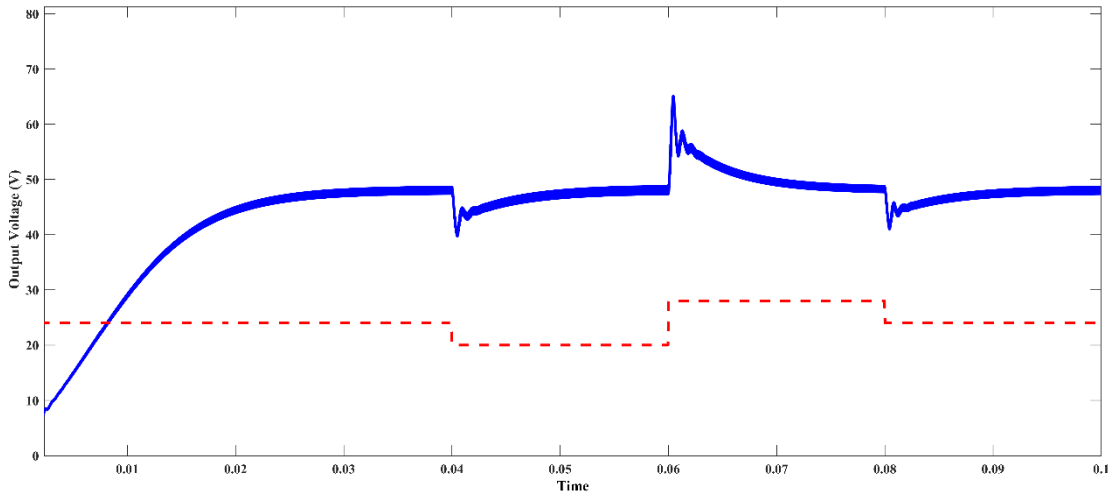

Fig 4.3 Source voltage disturbance response of Cohen-coon PI controller

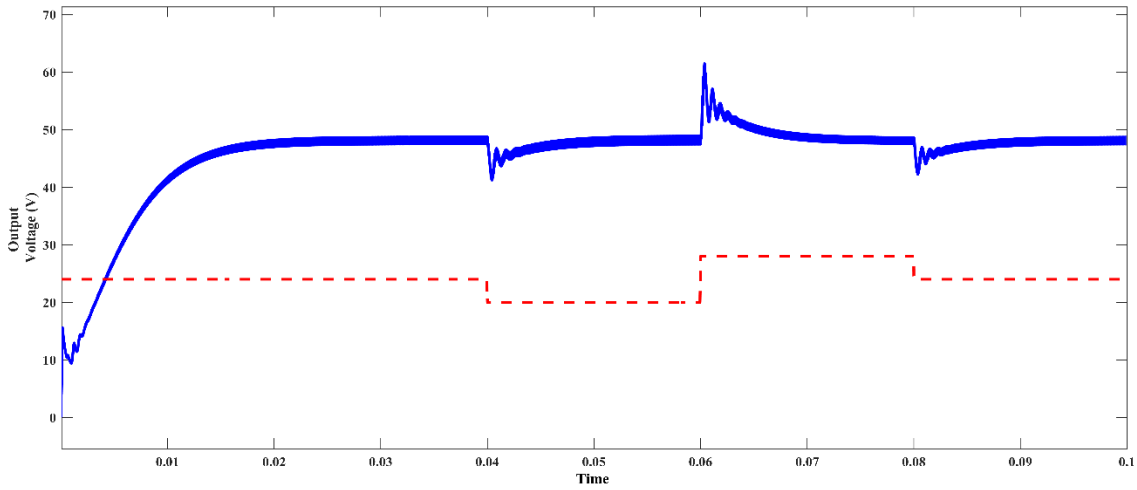

Fig 4.4 Source voltage disturbance response of IMC-PID controller

Following the input voltage step at t = 0.04s, the IMC-PID controller experiences a momentary voltage dip of 6.7901V, with the output voltage reaching a minimum of approximately 41.21V before recovering to the regulated value. The recovery time defined as the time elapsed from the disturbance until the output voltage re-enters and remains within the ±2% regulation band around 48V is measured as 0.008717 s. A voltage spike of 0.9055V above the reference is observed during the recovery transient.

The Cohen-coon PI controller experiences a larger voltage dip of 8.2057V under the same disturbance conditions, with the output reaching a minimum of approximately 39.79V. The recovery time is measured as 0.013327 s approximately 53% longer than that of the IMC-PID controller. A comparable voltage spike of 0.9054V is observed during recovery.

The first dip is higher and the recovery period is more prolonged, but both controllers return the output voltage to the stabilised band after the disturbance. The source disruption response metrics are summarised in Table 4.2.

Table 4.2: Source Voltage Disturbance Metrics

Metric	***Cohen-coon***	***IMC-PID***
Voltage Dip	8.2057 V	6.7901 V
Voltage Spike	15.99 V	13.45 V
Recovery Time	0.013327 s	0.8717 s

The source voltage disturbance test also shows the superior disturbance rejection capability of the IMC-PID controller. In the case of a sudden drop of the input voltage at $t = 0.04$ s, the IMC-PID controller limits the dip of the output voltage to 6.7901 V and recovers the regulation in 0.008717 s. The voltage dip experienced by Cohen-coon PI controller is 8.2057 V, which is about 20.8% more than that of IMC-PID controller under the same disturbance condition. In addition, its recovery time is 0.013327 s, making it approximately 52.9% slower to regain regulation following the disturbance.

The larger dip and slower recovery of the Cohen-coon controller can be attributed to its lower control bandwidth resulting from the conservative gain values derived through the tuning procedure. A controller with lower bandwidth responds more slowly to changes in plant operating conditions, allowing the output voltage to deviate further from the reference before the corrective action takes effect. The IMC-PID controller, with its higher proportional gain Kc and analytically derived integral action, is able to respond more aggressively to the disturbance-induced error and drive the output back to regulation more quickly.

The recovery transient of both controllers results in voltage spikes of about 15.99 V for Cohen-coon and about 13.45 V for IMC indicating overshoot behaviour in the disturbance response. The symmetry of spike magnitude indicates that the difference between the two controllers is in the initial response speed rather than overshoot in the recovery. Neither controller violates the output voltage spec during the recovery.

Source voltage disturbances are a realistic and often encountered operating condition in the context of EV charging especially in solar-powered charging stations where irradiance variations result in fast fluctuations of the PV panel output voltage, or in grid-connected chargers where voltage sags and swells occur due to grid instability. The test findings indicate that the IMC-PID controller has better disturbance reject ability. This means that the IMC-PID controller is more able to deal with real-world variabilities of the input while continuing to offer the stable and controlled charging voltage to the battery.

4.3.2 Load Disturbance Response

The load disturbance test is conducted to determine the ability of each controller to ensure regulation of the output voltage under the condition of sudden load variation. Two load switching events are applied sequentially during the same simulation run. First, a 76 Ω resistor is connected in parallel with the nominal 19.2 Ω load at $t = 0.04$ s. Later, at $t = 0.08$ s, the 76 Ω resistor is replaced with a 38 Ω resistor. The resulting output voltage responses for both controllers under these sequential load disturbances are presented in Fig. 4.5 and Fig. 4.6, respectively.

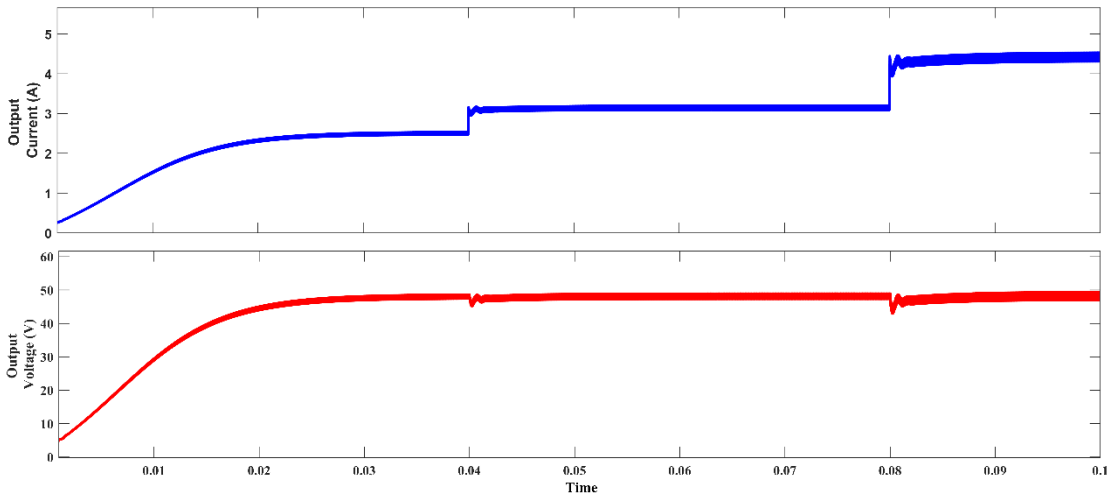

Fig. 4.5 Load disturbance response of Cohen-coon PI controller

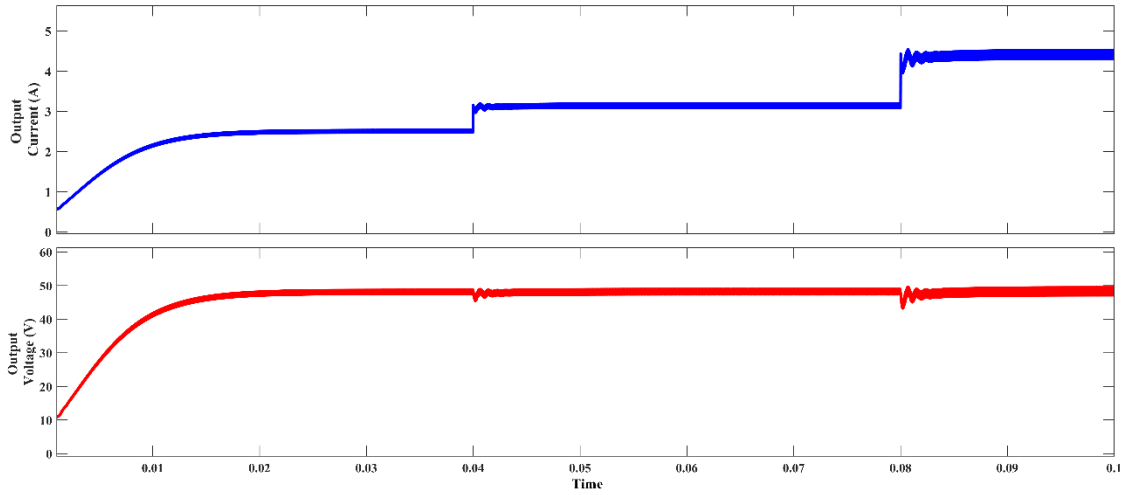

Fig. 4.6 Load disturbance response of IMC-PID controller

The output voltage deviations for both controllers due to both load switching events remain within the ±2% regulation band of ±0.96V from the 48V reference for the entire simulation. Neither of the controllers loses regulation at any time in the load disturbance test. The maximum dip in voltage observed in all the load events is 4.25V and 4.16V for Cohen-coon PI and IMC-PID respectively which are well within the permissible band. The maximum voltage spike does not exceed 1.71V for Cohen-coon PI and 1.09V for IMC-PID.

This result demonstrates that both controllers provide robust load disturbance rejection for the non-ideal SEPIC converter under the tested conditions, with neither controller requiring a measurable recovery period as the output voltage never exits the regulated band. The load disturbance metrics are summarized in Table 4.3.

Table 4.3: Load Disturbance Metrics

Metric	***Cohen-coon***	***IMC-PID***
Max Voltage Dip (Load 1)	2.5111 V	2.37 V
Max Voltage Spike (Load 1)	1.71 V	0.71 V
Recovery Time (Load 1)	Within Band	Within Band
Max Voltage Dip (Load 2)	4.25 V	4.16 V
Max Voltage Spike (Load 2)	1.71 V	1.09 V
Recovery Time (Load 2)	Within Band	Within Band

The result of load disturbance test is significant different with the result of source disturbance test. For both load switching events (76Ω load is connected at t = 0.04s and load is switched to 38Ω at t = 0.08s), output voltage variation of both controllers fall within the ±2% regulation band of ±0.96V. The maximum voltage dip for all load events is 4.25V for Cohen-coon PI and 4.16V for IMC-PID, whereas the maximum spike is not larger than 1.71V and 1.09V respectively.

The performance of the two controllers is almost identical during load disturbance testing which indicates that the response to load transients is dominated mainly by the inherent output impedance characteristics of the SEPIC converter and not by the specific controller tuning. The voltage deviations caused by the load are relatively small and within the regulation range. No obvious recovery time is required. This implies that the output capacitor C_2 can provide the transient energy requirement and buffer the load change efficiently before the controller has to take a significant corrective action. Such behaviour is consistent with the comparatively large output capacitance of 35.36 μF employed in the converter design.

Although the two controllers exhibit almost identical performance under load disturbance conditions, this observation is important in its own right. It demonstrates that neither tuning approach introduces instability or excessive sensitivity to load variations.

4.4 Switching Device Stress Analysis

The switching device stress analysis examines the current waveforms of the MOSFET switch and the output diode under closed-loop operation for both controllers. The scope waveforms of the diode and MOSFET currents under Cohen-coon PI and IMC-PID control are presented in Fig. 4.7 and Fig. 4.8 respectively.

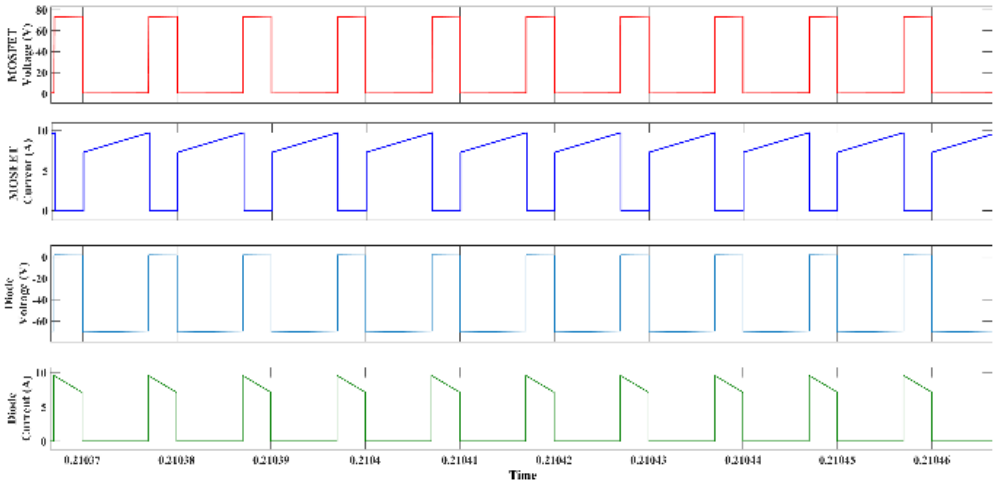

Fig. 4.7 MOSFET and diode current waveforms under Cohen-coon PI control

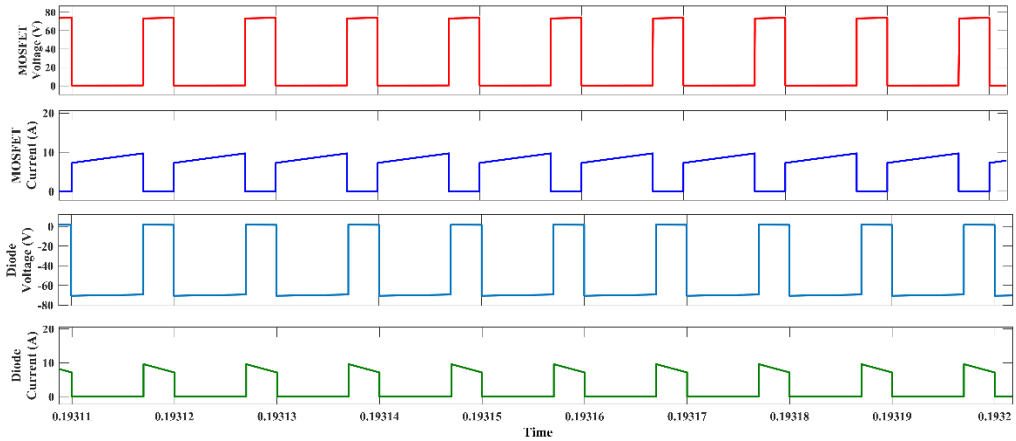

Fig. 4.8 MOSFET and diode current waveforms under IMC-PID control

The current waveforms confirm that both controllers maintain comparable switching device stress levels under nominal operating conditions. The pulsed nature of the switch and diode currents is consistent with CCM operation of the SEPIC converter at the 100 kHz switching frequency established in Table 2.1.

The stress analysis of the switching device deals with the current waveforms of MOSFET switch and output diode with closed-loop operation for both controllers. At present the waveforms shown in Fig. 4.7 and Fig. 4.8 show that the stress on the switching devices for both controllers are qualitatively similar under nominal operating conditions.

The pulsed behaviour of the current waveforms of diode and MOSFET agrees with the CCM operation at 100 kHz switching frequency, as it is expected from the converter design. The peak current values of both waveforms are similar for both controllers. This implies that the difference in tuning methodology does not result in significantly different current stress on the switching devices during steady state operation.

Note that during the startup transient, there is a short time of high current through the switching devices in both controllers as the inductor currents ramp up from zero to their steady state values. The faster startup response of the IMC-PID controller reduces the duration of this elevated stress period compared to the Cohen–Coon controller. Nevertheless, in both cases the device stresses remain within the safe operating limits of the components specified in Table 2.1.

4.5 Frequency Response

4.5.1 Open Loop Frequency Response

Before designing a feedback controller for the non-ideal SEPIC converter, it is important to describe the open-loop frequency response of the plant transfer function G(s) derived in Section 2.3. This analysis gives a clear understanding of the dynamic performance of the uncompensated system, identifies stability challenges that the controller has to solve, and specifies the frequency-domain restrictions within which the controller design must operate.

The open-loop Bode plot of the non-ideal SEPIC transfer function is obtained by evaluating G(s) across a wide range of frequencies using MATLAB, with the numerical transfer function coefficients corresponding to the converter parameters listed in Table 2.1. The resulting magnitude and phase plots are presented in Fig. 4.9.

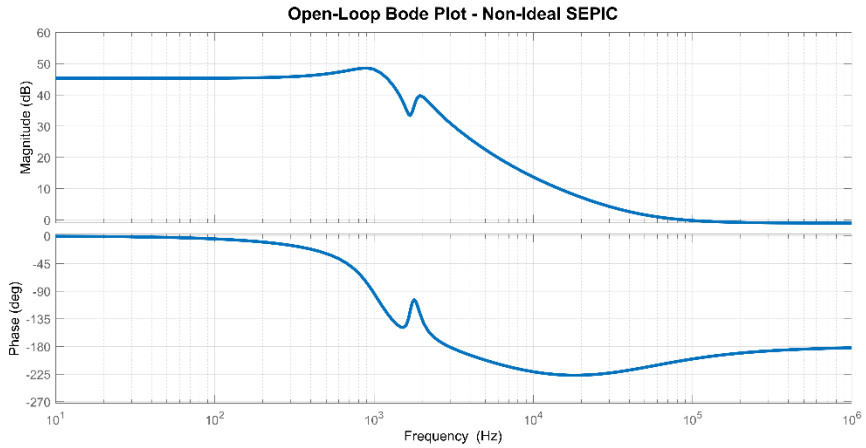

Fig. 4.9: Frequency response of Non-Ideal Uncompensated Open Loop SEPIC Converter

The open-loop transfer function exhibits a DC gain of 184.26 V/V, corresponding to 45.31 dB. This high DC gain is a direct consequence of the large voltage conversion ratio of the converter stepping up from 24V to 48V combined with the influence of the non-ideal parasitic resistances on the low-frequency gain of the plant. While a high DC gain is generally desirable from a steady-state regulation standpoint, it also means that the open-loop gain remains elevated across a wide frequency range, contributing to the stability challenges discussed below.

The plant transfer function exhibits two pairs of complex conjugate poles, which is consistent with the fourth-order behaviour of the non-ideal SEPIC small-signal model. The first pole pair is located at $-1247 \pm j11547$ rad/s, corresponding to a natural frequency of nearly 11614 rad/s and a damping ratio of approximately $\zeta \approx 0.107$. A second pole pair located at $-2279 \pm j6168$ rad/s, having a natural frequency approximately 6578 rad/s and an already more significant damping ratio value. As both pole pairs are on the left-half Plane, from the point of view of the poles locations, the open loop plant is stable.

Although, the damping ratio value for the dominant poles pair is small, resulting in a resonant peak for the magnitude response and a quick phase shift about the related natural frequency area. It is the presence of such a resonance feature that leads to significant phase lags in the mid-range of frequencies, which becomes a key aspect responsible of the closed-loop system instability.

The transfer function contains four zeros. Three of these are located in the left-half Plane and contribute beneficially or neutrally to the phase response. The fourth zero, however, is a right-half Plane zero located at +37,643.5 rad/s, corresponding to a frequency of approximately 5991 Hz. As discussed in Section 2.3, the RHP zero imposes a hard constraint on the achievable closed-loop bandwidth. Standard control design practice requires that the gain crossover frequency of the compensated loop be limited to no more than one-fifth of the RHP zero frequency, placing an upper bound of approximately 7,529 rad/s on the crossover frequency for this converter. Exceeding

this limit would result in the phase contribution of the RHP zero eroding the phase margin of the closed-loop system to an unacceptable level.

The open-loop frequency response reveals that the uncompensated plant is conditionally unstable. The gain crossover frequency of the uncompensated system occurs at 563,368 rad/s a value that is more than fifteen times the RHP zero frequency and far beyond any practically meaningful control bandwidth for this converter. At this crossover frequency, the uncompensated plant exhibits a phase margin of $-22.25°$, indicating that the system would become unstable if operated in a unity feedback configuration without any form of compensation. The gain margin, which is approximately 1 dB, further highlights the very limited stability reserve available in the uncompensated loop.

This analysis clearly demonstrates the need for a well designed feedback controller that reduces the gain crossover frequency to a value well below the RHP zero constraint, recovers enough phase margin at the new crossover frequency and at the same time provides satisfactory rejection of the input and load disturbances. The ability of each of the two controller tuning methodologies investigated in this thesis, the Cohen-coon PI method and the IMC-PID approach, to meet these constraints, is a central part of the comparative evaluation and the results are presented in this Thesis.

4.5.2 Loop Gain Bode Analysis

To further characterize the closed-loop behaviour of both controllers, the loop gain L(s) = C(s)·G(s) is evaluated across the frequency domain for each compensated system. The loop gain Bode plots for the Cohen-coon PI and IMC-PID controllers are presented in Fig. 4.10 and Fig. 4.11 respectively.

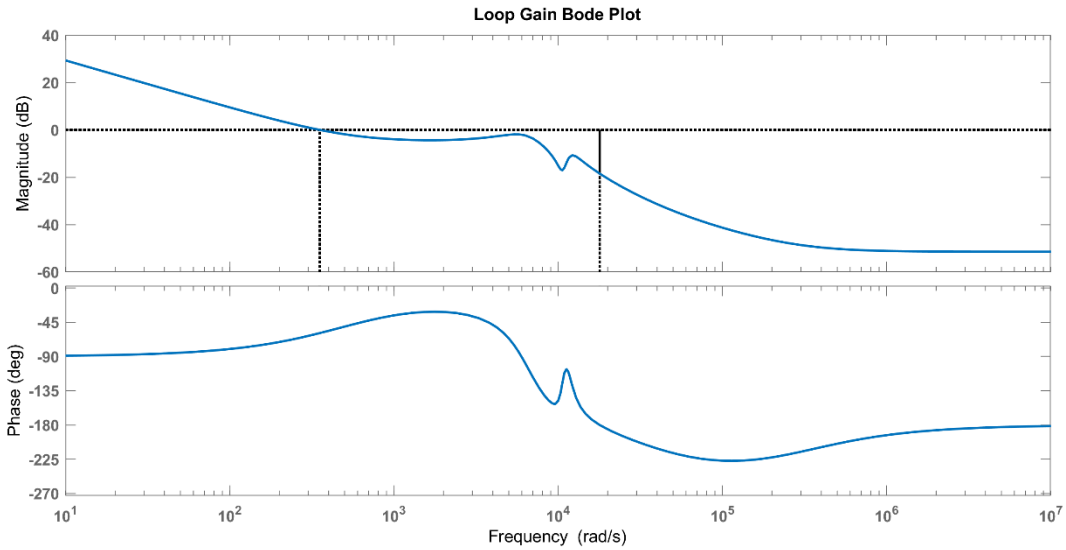

Fig. 4.10 Loop gain Bode plot of Cohen-coon PI

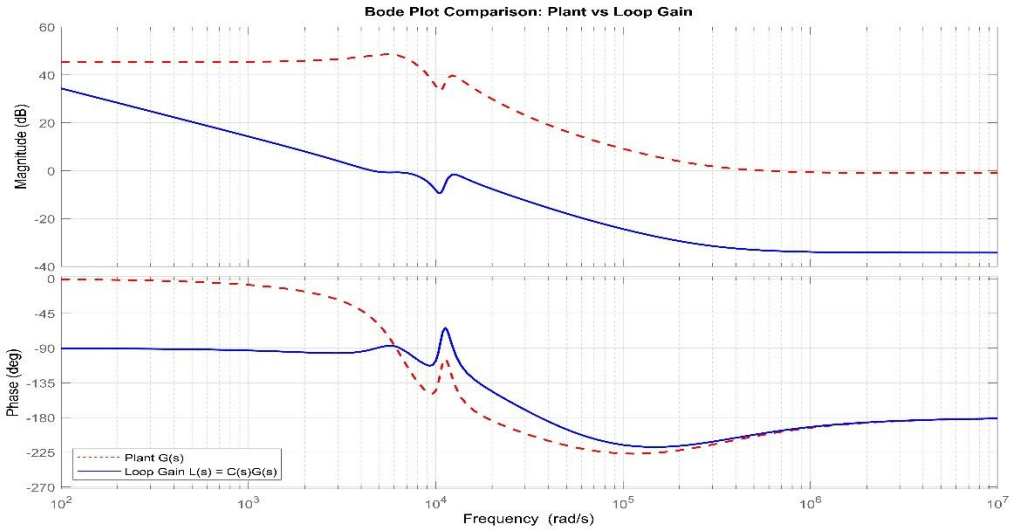

Fig. 4.11 Loop gain Bode plot of compensated IMC-PID

The Bode plots confirm the stability of the closed loop system for both the compensated loops, as the gain and phase are consistent with the transient behavior from the step response and disturbance rejection simulations. Both controllers are designed to have gain crossover frequencies sufficiently lower than the RHP zero frequency of 37,643.5 rad/s defined in Section 2.4. This confirms that both designs respect the fundamental bandwidth constraint of the non-minimum phase nature of the SEPIC plant.

4.6 Comparative Summary

The results obtained from all simulation studies are summarized in Table 4.4, which presents a comprehensive side-by-side comparison of the two controllers across all considered performance metrics. This table provides the primary basis for conclusions presented in Chapter 5.

Table 4.4: Comprehensive Performance Comparison Cohen-coon PI vs IMC-PID

Performance Criterion	***Cohen-coon PI***	***IMC-PID***
Rise Time	0.016858 s	0.010856 s
Settling Time	0.030687 s	0.020287 s
Overshoot	66.02 V	63.29 V
Peak V_{out}	48.47 V	48.53 V
Steady State Error	0.7131 V	0.7131 V
Source Disturbance Dip	8.2057 V	6.7901 V
Source Disturbance Spike	15.99 V	13.45 V

Performance Criterion	***Cohen-coon PI***	***IMC-PID***
Source Recovery Time	0.013327 s	0.008717 s
Load Disturbance Dip	2.511 V	2.37 V
Load Disturbance Spike	1.71 V	0.71 V
Load Recovery	Within band	Within band
Device Stress	Comparable	Comparable
Design Complexity	Low	Moderate
Plant Model Required	No	Yes

By comparing the results, it can be observed that the IMC-PID controller has a better performance for most of the evaluated criteria, especially regarding transient response and source disturbance rejection. The Cohen–Coon PI controller is comparable only in terms of steady-state error, which is mostly limited by the plant parameters, load disturbance rejection and device stress. The main advantage of this method is the simplicity of tuning procedure. Unlike the IMC-PID approach, it does not need a detailed plant transfer function and can be tuned using a simple open-loop step test. It makes it an attractive option when a complete small-signal model of the system is not available.

The overall comparative study demonstrates the suitability of IMC-PID controller for the non-ideal SEPIC converter for EV charging applications where the major design requirements are fast dynamic response and effective disturbance rejection. The PI controller presented is easier to tune and implement, but is less suitable for applications where simplicity and ease of deployment are more important than the best possible dynamic performance. These observations are examined further in Chapter 5.

CHAPTER 5
CONCLUSION AND FUTURE WORK

5.1 Conclusion Drawn

This thesis presents a simulation-based comparative analysis and the following conclusions are drawn:

1. **IMC-PID delivers superior transient response:** The rise time and settling time of the IMC-PID controller are 0.010856 and 0.020287 s, respectively, which are about 35.6% and 33.9% better than those of the Cohen-coon PI controller. The overshoot of both controllers is kept below 1.5% indicating that the performance advantage of the IMC-PID is demonstrated in a faster response speed rather than an increased oscillation tendency. Such a superior dynamic performance, compared to the empirical approximation based Cohen-coon approach, is the result of the analytical model-based design of the IMC framework that explicitly exploits the plant transfer function in the controller synthesis.

2. **IMC-PID provides better source disturbance rejection:** The IMC-PID controller limits the output voltage dip to 6.7901 V and the recovery time to 0.008717 s when the input supply voltage is suddenly reduced, while the same values for the Cohen-coon PI controller are 8.2057 V and 0.013327 s. This is a 17.3% reduction in voltage dip and a 34.6% faster recovery – a meaningful advantage in EV charging scenarios that often see input voltage fluctuations due to renewable energy variability or grid instability.

3. **Non-ideal modelling is essential for realistic controller evaluation:** The inclusion of parasitic resistances in the converter model produces a fourth-order transfer function with complex pole structure and a RHP zero that significantly differs from the ideal second-order model commonly used in literature. The steady-state error resulting from the parasitic voltage drops, the bandwidth constraint imposed by the RHP zero, and the damping characteristics of the complex poles all have direct consequences for controller design and performance. This thesis demonstrates that controllers designed and evaluated on the non-ideal plant model produce results that are more representative of what would be expected in physical hardware implementation.

5.2 Future Scope

The work in this thesis forms the basis for several avenues of future research and development that can extend and build on the results reported herein.

Hardware Implementation and Validation: The simplest and most direct way to extend this work is to physically implement the two controllers on a real SEPIC converter prototype. While MATLAB/Simulink results provide a reliable basis for comparison under the developed non-ideal model, experimental hardware validation

would be valuable in confirming the practical applicability of the conclusions presented in this work. Hardware implementation would also reveal additional non-ideal effects that are not fully captured in simulation, including gate-driver delays, switching dead-time effects, and temperature-dependent variations in component parameters. Furthermore, implementation on a digital control platform such as a DSP or FPGA would provide insight into the practical challenges associated with discretizing the continuous-time IMC-PID controller for operation at a switching frequency of 100 kHz.

Advanced Control Strategies: Model predictive control (MPC), sliding mode control (SMC), and fractional order PID control are among the promising alternatives that can be compared to the Cohen–Coon PI and IMC-PID controllers studied here. Such an investigation would provide a broader understanding of the control design trade-offs for non-minimum phase power converters, and may also identify control approaches that can better address the bandwidth limitations imposed by the RHP zero as compared to conventional PI/PID-based methods.

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Saurabh Batham

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