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COMPARATIVE THD ANALYSIS OF 31-LEVEL AND 63-LEVEL REDUCED SWITCH MULTILEVEL INVERTER WITH PASSIVE FILTER

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CANDIDATE DECLARATION

I, LAYBA , Roll No. 2K24/PES/23 student of M. Tech. (POWER ELECTRONICS AND SYSTEM), hereby declare that the project titled **"Comparative THD Analysis of 31-Level and 63-Level Reduced Switch Multilevel Inverter with Passive filter"** under the supervision of PROF. MADHUSUDAN SINGH and PROF. MINI SREEJETH, Department of Electrical Engineering, Delhi Technological University, in partial fulfilment of the requirements of the degree of Master of Technology, has not been submitted elsewhere.

Place: Delhi
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CERTIFICATE

This is to certify that the Project entitled **"Comparative THD Analysis of 31-Level and 63-Level Reduced Switch Multilevel Inverter with Passive filter"** being submitted by **Layba(24/PES/23)** in partial fulfilment of the requirement for the degree of Master of Technology in Power Electronics and System at DTU is an authentic record of the work carried out by her under our supervision and guidance.

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ABSTRACT

The Multilevel inverter have gained recognition in last few decades. They are being utilized to convert the DC voltage into AC voltage in the form of steps or levels, with increasing the steps the output voltage start achieving the shape similar to the sine wave which results in reducing the harmonic distortion. However, increasing the levels in output voltage of multilevel inverter leads to increase in the power electronic components and devices which makes the design massive. The Multilevel inverters are widely being used in various applications like renewable energy systems, high power motor drives, HVDC transmission, FACT devices, electric vehicles and many more. A wide range of controlling methods and modulation techniques are being introduced to enhance the efficiency and operation.

In our work, we have designed the 31-level and 63-level reduced switch multilevel inverter. Simulation has been carried out using MATLAB Simulink. The load used in the simulation of MLI are taken as R-L load. The Total Harmonic Distortion for each system has also been analyzed and studied from simulation results. The design of the 31-level reduced switch multilevel topology consists of twelve switches and four DC sources and the 63-level topology consists of fourteen switches and five DC sources, aiming to reduce the THD obtained and enhancing its efficiency. In order to further reduce the THD, an LC and LCL filter has been designed, and a comparative THD analysis has been performed by considering the two cases, that is, one without a filter and another with LC and LCL filter. The THD's observed are falling under IEEE 519 standards, which is below 5%.

We have also implemented the design of lower-level reduced switch topologies, which is 5-level and 7-level Reduced Switch MLI and then observed the THD's. Then, we have designed the LC filter for both topologies and observed the THD's and compared the results.

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
THD	Total Harmonic Distortion
MLI	Multilevel Inverter
LC	Inductor–Capacitor

CHAPTER 1
INTRODUCTION

1.1. Background and Motivation

Power electronics plays a vital role in the conversion of power from one form to another using converters and power electronic devices such as IGBT, MOSFET, SCR and many others. Multilevel inverters are also utilized widely for this purpose of converting DC into AC as the output voltage provided is much closer to a sinusoidal waveform and has higher power handling capability, higher efficiency, etc.[1]-[2].The conventional inverters provide the square wave output voltage with larger harmonic distortion, whereas MLI provide the output voltage in the form of multiple steps resembling the sinusoid, thus reducing the harmonic distortion. They are extensively being used in incorporating renewables to the grid, such as solar, wind, etc, hence acting as an interface between them [3]-[4].

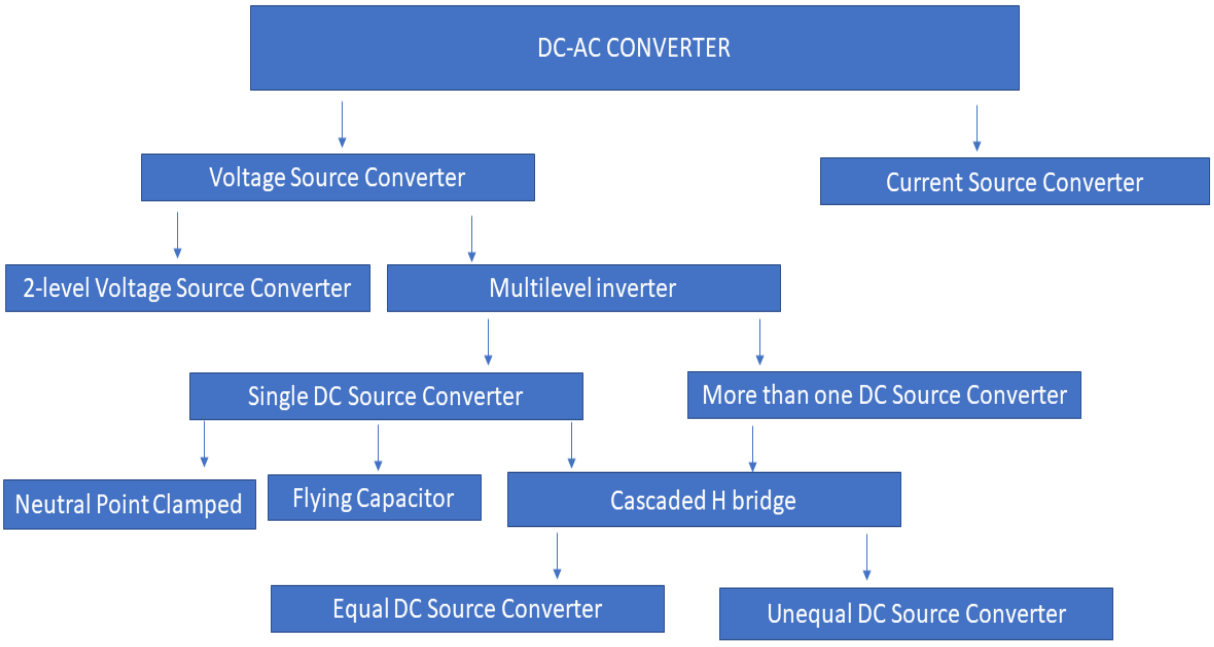


Fig. 1.1: Flowchart classifying DC-AC Converter [23]

A multilevel inverter generates an output sinusoid approximated using a staircase method by integrating several direct current (DC) voltage sources with semiconductor switches. It is important to note that the above process eliminates harmonics in the output voltage waveform

and minimizes THD. Moreover, since voltage stress is shared between several components, multilevel inverters can handle higher voltages and power compared to two-level inverters [2]. The quality of the output voltage waveform is expected to improve with an increase in the number of output voltage levels.

Thus contributing towards affordable and clean energy which falls under SDG 7 and SDG 9. The conventional topologies of multilevel inverter include the diode clamped, neutral point clamped, cascaded bridge and flying capacitor [5]. These traditional topologies require more number of power electronic components, as neutral point clamped topologies require clamping diodes, the flying capacitor topology of a multilevel inverter requires capacitors, thus making the circuit bulky in size and complex[6].

1.2. Significance of Reduced Switch MLI Topologies

Technical and economical importance of RS-MLI investigations is highlighted by the increasing popularity of power electronics converters in different applications. In the sphere of renewable energy sources, the worldwide installation volume of grid-tied photovoltaics already exceeds 1.2 terawatt by the end of 2023, and multilevel inverters have become the primary power interface for utility-scale systems. Economical benefits provided by the RS-MLI technology result in a decrease in the cost per kilowatt of electricity generated by solar panels, where the cost reduction in inverter hardware of 15–20% provides for the same amount of reduction in system capital expenditure (approximately 2–3%) [14].

In the case of industrial motor drives, MLI drives are becoming more popular for use in medium voltage applications such as compressors, pumps, fans, and conveyors. This is due to their better output waveforms that reduce stresses in the motor insulation system and the consequent avoidance of the need for an output filter. The use of RS-MLI drives in industrial applications provides two advantages: lower converter costs and increased efficiency because of the reduced switching losses, as seen in literature [15] where efficiencies have been improved by 0.5 – 1.2 percent.

From the point of view of basic research in power electronics, RS-MLI offers a fertile field of research with much remaining to be discovered regarding novel circuit topologies, new theories of modulation, digital control methods, and reliability considerations. Systematic approaches to the design of new circuit topologies, switching states, and model-based predictive control methods based on the particular structure of RS-MLI circuits represent a highly fruitful area of

investigation with important industrial applications [16].

The reduced switch multilevel topologies have a lower number of switches compared to traditional topologies of multilevel inverter thus overcoming the major disadvantage of the three basic topologies, which include complex control and cost, as with the increase in switches, the control becomes complex.[7]-[11].

1.3. Contribution of Thesis

In our work, we have designed the 31-level and 63-level reduced switch multilevel inverter. Simulation has been carried out using MATLAB Simulink. The load used in the simulation of MLI are taken as R-L load. The Total Harmonic Distortion for each system has also been analyzed and studied from simulation results. The design of the 31-level reduced switch multilevel topology consists of twelve switches and four DC sources and the 63-level topology consists of fourteen switches and five DC sources, aiming to reduce the THD obtained and enhancing its efficiency. In order to further reduce the THD, an LC and LCL filter has been designed, and a comparative THD analysis has been performed by considering the two cases, that is, one without a filter and another with LC and LCL filter[12]-[13]. The THD's observed are falling under IEEE 519 standards, which is below 5%.

1.4. Organization of Thesis

The thesis is organized into 6 chapters:

Chapter 1 includes the motivation and background of reduced switch MLI, the significance of reduced switch topologies and the summary of research.

Chapter 2 provides a detailed literature survey including various reduced switch topologies, switching techniques and various applications.

Chapter 3 elaborates the 5-level and 7-level reduced switch MLI including their THD analysis with LC filter.

Chapter 4 presents the detailed comparative THD analysis of 31-level and 63-level MLI with LC and LCL filter in consideration.

Chapter 5 presents the results obtained which includes THD graphs and voltage waveforms of 31-level and 63-level reduced switch topology.

Chapter 6 presents the conclusion and future scope.

CHAPTER 2

LITERATURE REVIEW

2.1. Introduction

This chapter presents a systematic overview of the latest literature available about multilevel inverter (MLI) technology. It discusses the evolution and basic working principle of the three classical MLI configurations – NPC, FC, and CHB inverters[18],[19],[20]. It also presents the information regarding the symmetric and asymmetric CHB configurations as well as their impact[3]. The field of the emerging RSC MLI topologies is analyzed and discussed briefly. Furthermore, it also briefly discusses modulation and control techniques applied to multilevel inverters[3]. Afterwards, it deals with the analysis of harmonic distortion assessment, passive and active filtering methods that have been employed for achieving better power quality. Lastly, it addresses the practical implementation issues of MLIs in photovoltaic interfaces as well as adjustable speed drive applications.

2.2. Introduction to Multilevel Inverter Topologies

The concept of multilevel power conversion originated from Baker and Bannister's pioneering work from 1975, where the fundamentals were laid down for synthesizing AC voltages from multiple DC voltage levels [17]. The subsequent landmark contributions, including the neutral point clamped (NPC) inverter introduced by Nabae, Takahashi, and Akagi in 1981, the flying capacitor (FC) inverter created by Meynard and Foch in 1992, and the cascaded H-bridge (CHB) converter designed by Hammond in 1997, collectively formed the three classic types of multilevel converters still used extensively today in medium voltage drives and power quality equipment [18], [19], [20]. An important review paper published by Rodriguez et al. in 2002, summarizing this field, became the highly cited source for many researchers in power electronics community [21]. Another important review work published by Malinowski et al. in 2010 focused on cascaded multilevel inverters [3].

The NPC inverter brought in the idea of using clamping diodes for connecting the phase leg mid-points to a common neutral bus for generating three levels of output voltages from a single DC bus. Although proven and extensively used in industry, the NPC configuration experiences unbalanced losses across its switching elements, thereby making it less efficient in terms of its maximum power capability and switching frequency [20], [3]. In contrast, the FC topology

employed floating capacitors instead of clamping diodes, which provided increased modularity and redundancy in switching modes, but created serious voltage balance issues, particularly in traction applications, where the use of many pre-charge circuits is necessary [19]. As compared to the other two configurations, the CHB inverter, with its switching units consisting of a full bridge power cell fed from a separate DC source, provides highest modularity and robustness against failures. The modular nature of the inverter makes it easy to scale-up, and even when one cell fails, its operation may be avoided without halting the load, resulting in very high system availability [3].

2.3 Cascaded H-Bridge Inverters: Symmetric and Asymmetric Configurations

The research on CHB inverters has been further classified based on symmetry and asymmetry. In the case of symmetry, each of the H-bridge cells has a DC source of the same value. In the case of a series of N inverter cells, the highest possible phase voltage levels will be 2N + 1. For applications involving a higher number of levels, the relation is linear, which means that there is a direct proportionality between the number of cells and the number of voltage levels. Asymmetry, or hybrid design, involves assigning different DC voltages for successive cells in a certain ratio, usually a binary or trinary one. For the binary ratio arrangement, the possible number of voltage levels will be 2^(N+1) – 1, whereas, in the trinary ratio arrangement, the number of levels will be 3^N [3].

Asymmetric and hybrid cascaded topology systems were discussed systematically by Malinowski et al. [3], who pointed out that in trinary-asymmetric topology the high-voltage cell holds about 89% of the total output power, leading to a compelling case in using different devices – IGCTs for the high voltage cells and relatively low rated IGBTs for other cells – and this combination of devices is referred to as hybrid cascaded topology system. Further research was conducted by Bana et al. [22], who classified the newly designed MLIs according to their switch-reduction features and named them RSS MLI, RSA MLI, and RSM MLI. In other words, RSS MLI and RSA MLI have H-bridges, while RSM MLI does not. They concluded that asymmetric MLIs provide the most efficient conversion of the DC source number to output voltage level number and emphasized the problems in MLIs, including voltage balancing problem, redundant switching issue, and fault tolerance.

With respect to practical implementations involving high-level counts, Hayat et al. [23] showed how a five-sourced asymmetric binary combination having source levels with magnitude ratios

of 1:2:4:8:16 can achieve sixty-three levels of both positive and negative voltages on the load using only nine semiconducting switches, including five Power MOSFETs used for the generation of the levels and four others for reversing the polarity of the output voltages by employing an H-bridge circuitry. Clearly, this is quite efficient when compared to the 124 switches that are needed for generating the same sixty-three output levels using the symmetric CHB configuration, making the RS-ASCHBMLI one of the most efficient architectures to-date.

2.4 Reduced Switch Count Multilevel Inverter Topologies

The rationale for investigating the RSC MLI design has been succinctly described by Vemuganti et al. [7], stating that adding any new switch to the MLI will necessitate the addition of an independent gate driver, power isolation, cooling arrangement, and protection scheme, which adds to the cost, board space requirement, and failure chances. Moreover, a higher number of switches will pose challenges for the modulation controller from the computational point of view. In the same study, RSC-MLI designs have been categorised into six broad classes such as generalised topologies, stacked topologies, unit-based topologies, switched capacitor topologies, transformer-based topologies, and three-phase topologies [7].

From among the generalised topology, the MLDCL, SSPS, RV, SCSS, and MLM topologies employ a distinct polarity generator (normally an H-bridge) and level generators made up of half-bridge chopper modules [7]. The T-type RSC-MLI, which was introduced in 2006, connects the midpoint of one phase leg of the H-bridge to the DC link using bi-directional switches, enabling a significant reduction in the number of switches, as it operates with only two devices conducting simultaneously, thus reducing conduction losses [7]. The HSC-based topology is an extension of the T-type topology, where unidirectional switches are used in a hexagonal configuration, providing more switching flexibility for asymmetric DC source ratios [7].

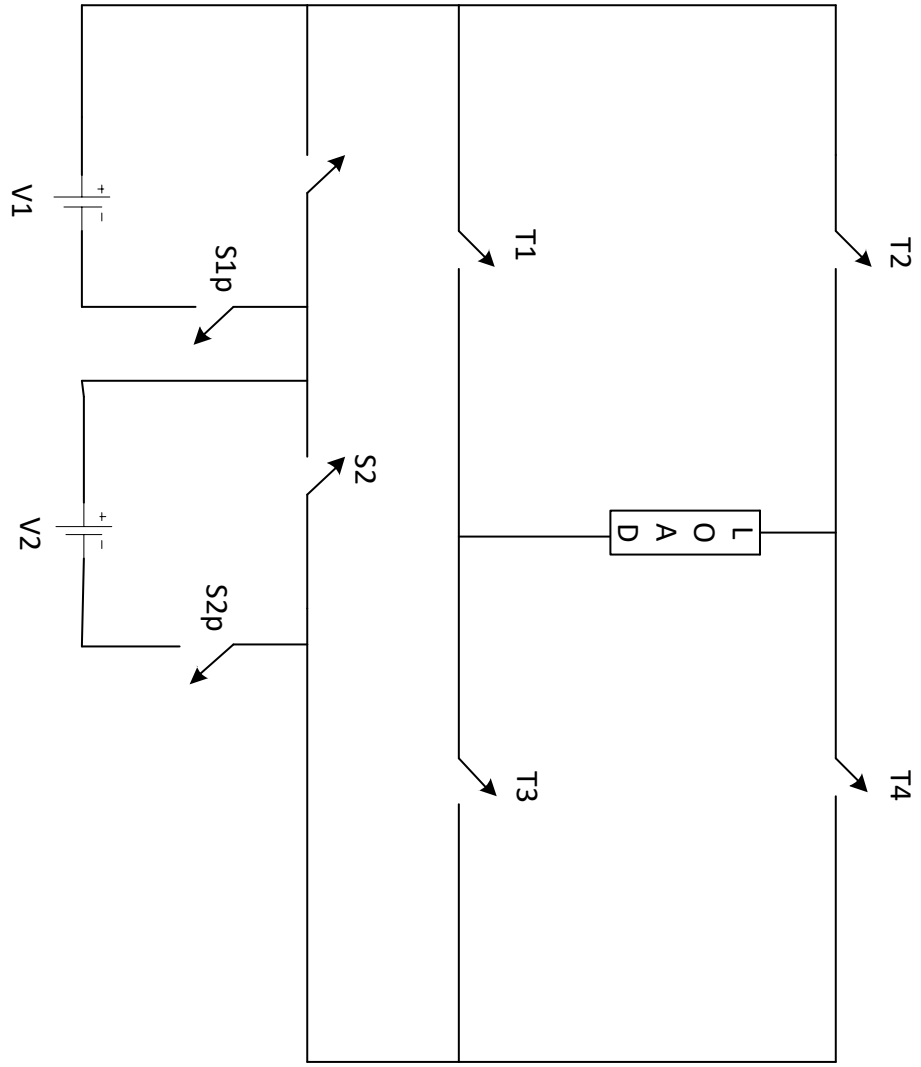


Fig. 2.1: MLDCL:Reduced Switch Topology [7]

The switched-capacitor MLI topologies have been gaining huge momentum recently owing to their ability to use one less or more than one DC sources for each output level through switching sequences and also operate in an inherently boost mode, thus allowing peak output voltage to be higher than the total sum of the stiff DC source voltages [7]. In particular, the seven-level SC tripler topology by Peng et al. is capable of boosting the voltage three times with only one DC source and eight switches with self-balanced capacitor voltages [7]. Additionally, the thirteen-level SC tripler-plus-doubler topology by Ye et al. uses tripler and doubler units to multiply the number of output levels but does not compromise on self-balancing feature of its capacitor voltages [7]. Moreover, Lee's single-stage switched-capacitor module topology offers nine output levels by doubling the DC source voltage with only ten switches and two self-balanced capacitors irrespective of the load power factor and modulation index [7].

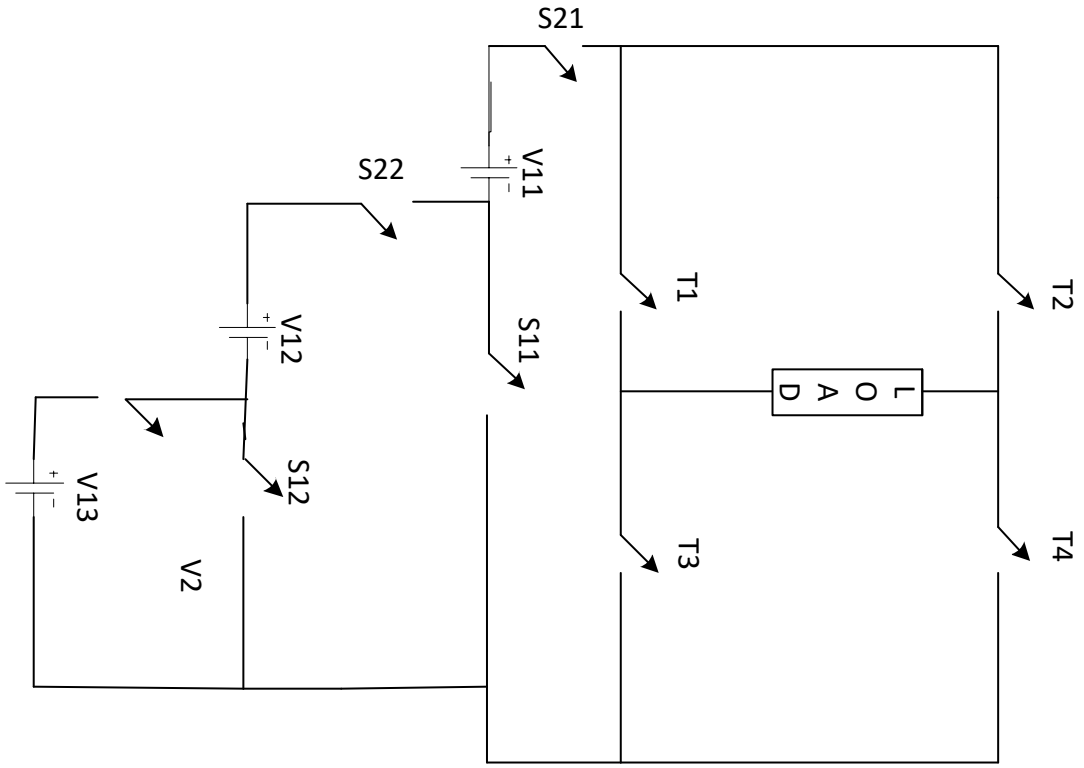


Fig. 2.2:SCSS:Reduced Switch Topology[7]

Stacking topology involving the serial connection of several inverters with different voltage ratings is symbolized by the idea of the level doubling network (LDN). In an LDN configuration, the floating capacitor two-switch module is added to the existing MLI in order to double the level of output along with providing inherent self-balance feature whereby if there is any imbalance between LDN capacitor voltage and its target value which should be one-half of the voltage of primary bus, the DC component of the output current automatically recharges the capacitor [7].

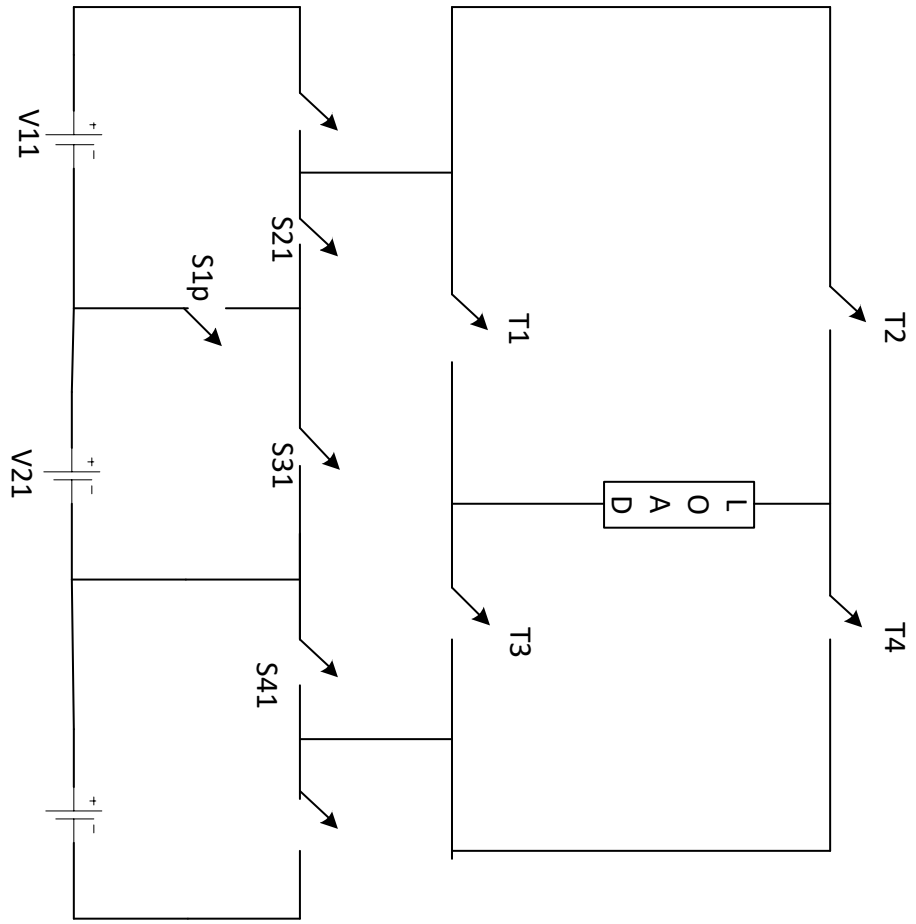


Fig. 2.3: RV:A Reduced Switch Topology[7]

2.5 Modulation and Control Strategies for Multilevel Inverters

The modulation techniques for MLIs can be generally classified as high frequency modulation techniques like multilevel carrier based pulse width modulation (PWM) and space vector modulation (SVM), or fundamental frequency modulation techniques, predominantly the selective harmonic elimination (SHE) and nearest level control (NLC) [3]. The most popular technique used in cascaded MLIs was found to be phase shifted PWM by Malinowski et al. [3], because it ensures even switching operations within cells, balanced power distribution between different H-bridges, and implementation simplicity irrespective of the number of cascaded cells. Although the level shifted PWM is extensively used in NPC inverters, it may lead to unbalanced power distribution between CHB cells and needs a rotational carrier approach to solve this problem [3].

To solve the problem of realizing low THD using fewer switches at the fundamental frequency,

the voltage-reference technique used in RS-ASCHBMLI by Hayat et al. [23] presents an efficient method that eliminates the use of iterative solutions to the SHE equations. In this solution method, the comparator of the switching control module compares the absolute value of a reference signal with a set of equidistant DC offsets, creating a binary output signal whose positive edges indicate the switching angles. In a 63-level inverter, with thirty-one DC offsets, thirty-one switching angles will be formed based on arcsine of the normalized magnitude of the DC offset. Consequently, THD of approximately 1.02% for the first twenty-seven harmonics will be obtained, which is extremely low compared to the 5% threshold in the IEEE 519 harmonic standards [23].

For cases where lower order dominant harmonics need to be eliminated especially the 3rd, 5th, and 7th harmonics which cannot be eliminated effectively in single phase inverters, SHE-PWM technique is the most efficient harmonic elimination method. Dahidah et al.[24] gave an extensive survey of multilevel SHE-PWM equations and their corresponding solution algorithms including Newton-Raphson technique, resultant method, and evolutionary algorithms such as PSO and GA. According to Bana et al.[22], a PSO based-SHE controller on RSS-MLI proved to be capable of eliminating 3rd harmonic in a five-level output, 3rd and 5th in a seven-level output and 3rd, 5th, and 7th in a nine-level output. Predictive control scheme discussed by Malinowski et al.[3] was further extended to include cascaded asymmetric MLIs where the inverter was considered a finite state machine and each switching state was selected to minimise cost function comprising output current error and switching frequency penalty terms.

2.6 Total Harmonic Distortion and Filtering Approaches

Total Harmonic Distortion (THD) is the main measure used in determining the quality of the output wave shape of MLI, referring to the ratio of the root mean square value of all harmonics voltage amplitudes to the root mean square value of the fundamental voltage amplitude. Expressions for amplitude calculation of individual harmonics of an MLI generating stepped output at fundamental frequency of switching operations are mathematically obtained using the Fourier analysis method. Closed form equations for obtaining amplitudes of individual odd harmonics were developed for 63-level RS-ASCHBMLI by Hayat et al. [23]. According to this study, fundamental amplitude = 184.74V (for Vdc1=6V), and the amplitude of the third harmonic = -1.43V. Therefore, the voltage THD is 1.004%, based on calculations of the first twenty-seven harmonics. The presence of half-wave symmetry ensures that all even harmonics

and DC components do not appear in the output waveforms [23].

However, for inverters with lower-level counts where the inherent THD is relatively higher, the application of passive filtering and active filtering assumes a very important role. In an empirical comparison of THD reduction in a five-level cascaded H-bridge MLI system, Praween & Kumar [12] compared the effects on THD when there was no filter at all, a passive LC low-pass filter, and the presence of a dynamic voltage restorer (DVR). Their findings show the initial value of THD of the five-level unfiltered MLI in the experiment as 23.06%, which was brought down to 15.76% with the use of a passive LC filter (with L = 0.125 H, C = 20.28 μF) and further brought down to 11.50% when using a DVR with a 0.074 H inductor filter and 100V DC energy source. Clearly, the results support the overall theory that DVR compensation offers better performance than passive LC filtering when it comes to harmonic cancellation within cascaded H-bridges due to the compensating voltage injection technique in DVR filtering, even though passive LC filtering has the benefit of simplicity and cost-efficiency [12]. LC filter design for multilevel inverters is based on low-pass filtering concepts, where the cut-off frequency is chosen as one-tenth of the switching frequency in order to provide sufficient attenuation of the major harmonics associated with the switching frequency group. Minimum value of inductance depends on the permissible current ripple of the inductor under the specified DC bus voltage; on the other hand, the capacitor value is determined using the cut-off frequency criterion. For a switching frequency of ten kilohertz and ripple percentage of twenty percent, in accordance with Praween and Kumar [12], inductance is equal to 0.125 H, and capacitance amounts to about 20.28 μF, implying that the values of components are considerable, which is a drawback in comparison to the active DVR configuration.

2.7 Applications in Renewable Energy and Drive Systems

Cascaded multi-level inverters play a very important role in renewable energy interfacing topologies. The modular nature of their DC bus configuration ensures their compatibility with the distributed DC source from a series connection of PV strings, with each string being able to deliver an isolated DC voltage to an H-bridge cell of the converter. This allows the use of maximum power point tracking (MPPT) technique separately for each PV sub-string, thus overcoming the problem of energy loss caused by shading effects on the PV modules. As discussed in Bana et al. [22], several cascaded multilevel inverter topologies that have been used in conjunction with PV systems recently are PUC inverter, switched capacitor SSPS converter, and Quasi-Z-source.

The cascade MLI structure has seen widespread use in ASD systems to control medium-voltage induction motors for various purposes such as pumping, fans, compressors, and conveyors. The commercial availability of CHB-based ASDs with voltages varying between 2.3kV to 13.8kV and output power capacities ranging between 0.3MVA to 30MVA has been reported by Malinowski et al. [3] among various other authors; this demonstrates the practical realization of this structure. The minimization of the voltage swing per switch cycle in CHB ASD system eliminates the risk of electrical breakdown of the motor insulation and shaft currents in bearings, as well as allowing long motor cables without having to use du/dt filters [3].

According to Vemuganti et al. [7], although numerous RSC-MLI topologies have emerged in the scientific literature, their actual industrial adoption has faced certain limitations caused by decreased switch redundancy, inadequate fault tolerance, and increased controller complexity compared to traditional modular CHBs. It was predicted that topologies featuring attractive levels of modularity, a low level of TSV, and the property of self-balancing, e.g., MLDCL, half-leg T-type, and LDN, were more likely to experience industrial implementation in the near future. The use of wide bandgap semiconductor switches, namely SiC MOSFETs and GaN HEMTs, in RSC-MLIs can be considered a highly influential approach toward further advancements due to its contribution to an increased switching frequency, reduced conduction losses, higher temperature operation, and higher power density [22], [7].

2.8. Conclusion

This literature review has highlighted the development of the multilevel inverter topologies from basic to the advanced and reduced switch structures including their drawbacks. It has presented the development of reduced switch multilevel topologies and the structures including their applications in the field of renewables and electric drives, yet it requires more development in structures and design by reducing the switches which contributes in getting lower THD's economically. These limitations define the motivation for the present study and will be addressed in the chapters that follow.

CHAPTER – 3

REDUCED SWITCH MULTILEVEL INVERTER

3.1. Introduction

This chapter consists of lower level topologies of reduced switch MLI which acted as foundation in building the desired topology and achieving the desired result. The 5-level reduced multilevel inverter switch topology consists of 8 power electronic switches, which is lesser as compared to other topologies of multilevel inverter and 2 DC sources which are chosen as V1=Vdc and V2=2Vdc and the value of Vdc=20V.The design of the proposed 5-level and 7-level reduced switch multilevel inverter is demonstrated in the Fig. 1. Similarly, the arrangement of the 7-level reduced switch multilevel inverter also includes 8 power electronic switches and 2 DC sources, which is lower as compared to the cascaded H-bridge multilevel inverter. The arrangement of the circuit is shown in Fig. 1. A part of the demonstrated circuit consisting of switches S1, S1p, S2 and S2p generates the level or steps in the output waveform and the other part consisting of switches T1, T2, T3 and T4 are responsible for polarity generation as it reverses the level which are produced by level generator [13]. The switches employed for the design and simulation of 5-level and 7-level multilevel inverter are insulated gate bipolar transistors, and the load that has been utilized is an RL load.

The switching scheme utilised for the 5-level reduced switch multilevel inverter is depicted in Table 3.1, and the switching scheme employed for the 7-level reduced switch MLI has been tabulated in Table 3.2, which depicts the magnitude and switching involved in all seven levels. In case of 5-level, the magnitude of voltage levels are V1, V2, 0, -V1 and -V2 and for 7-level are V1, V2, V1+V2, 0, -V1, -V2 and -(V1+V2).

3.2. Five-Level Reduced Switch MLI Topology

The design of 5-level reduced switch multilevel inverter consists of two DC voltage sources, where V1=Vdc and V2=2Vdc and eight switches. The output voltage consists the following levels which are:

0, V1, V2, -V1, -V2

The switching scheme of 5-level reduced switch multilevel inverter topology is represented in the Table3.1. and the circuit diagram of 5-level reduced switch multilevel inverter is

represented in Fig. 3.1 below:

A part of the demonstrated circuit consisting of switches S1, S1p, S2 and S2p generates the level or steps in the output waveform and the other part consisting of switches T1, T2, T3 and T4 are responsible for polarity generation as it reverses the level which are produced by level generator[13]. The switches employed for the design and simulation of 5-level and 7-level multilevel inverter are insulated gate bipolar transistors, and the load that has been utilized is an RL load.

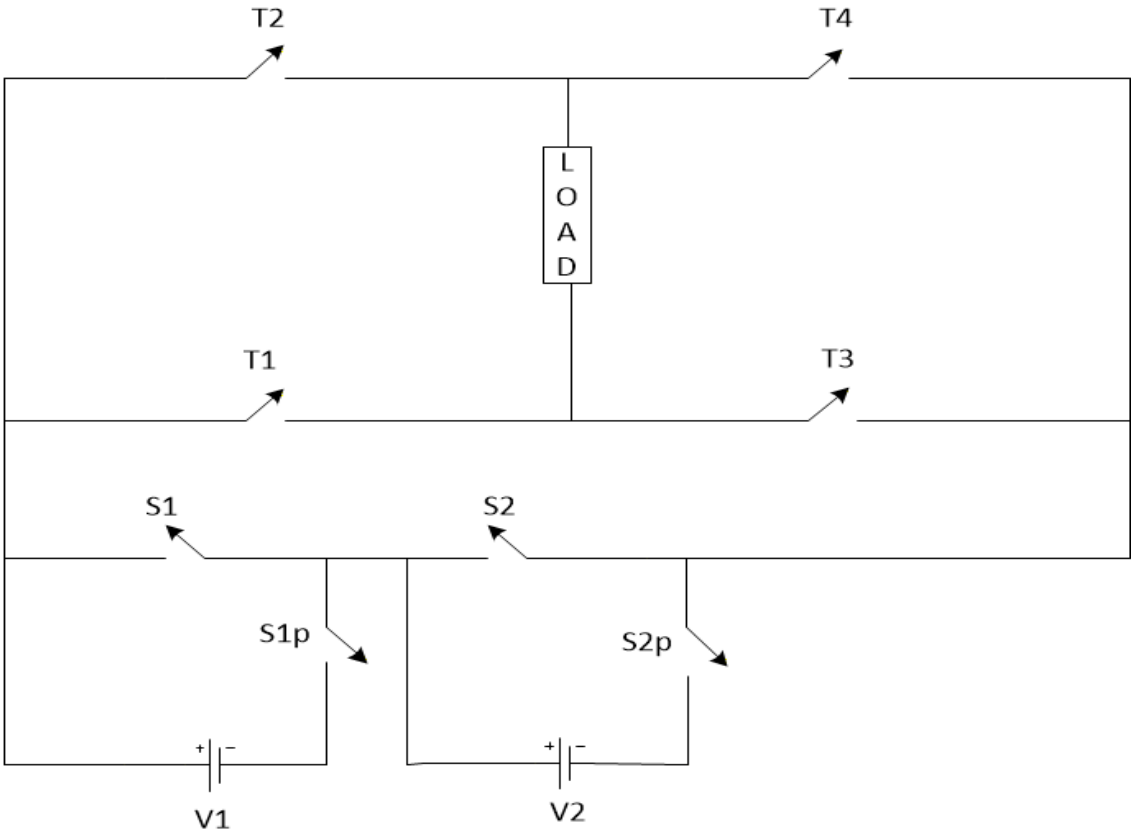


Fig. 3.1: Circuit diagram of a 5-level reduced switch multilevel inverter

Table 3.1: Switching scheme for 5-level reduced switch topology

SWITCHING STATES(0=OFF,1=ON)								OUTPUT VOLTAGE
T1	T2	T3	T4	S1	S1p	S2	S2p	V0
0	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	V1
0	1	1	0	1	0	0	1	V2
1	0	0	1	0	1	1	0	-V1
1	0	0	1	1	0	0	1	-V2

3.3. Seven-Level Reduced Switch Topology

The design of a 7-level reduced switch multilevel inverter consists of two voltage sources, where V1=Vdc and V2=2Vdc and eight switches. The output voltage consist of the following levels, which are:

0, V1, V2, V1+V2, -V1, -V2, -(V1+V2)

The switching scheme of the 7-level reduced switch multilevel inverter topology is represented and has been tabulated in the Table 3.2 below and the circuit diagram of 7-level reduced switch multilevel inverter is represented in Fig. 3.2 below.

A part of the demonstrated circuit consisting of switches S1, S1p, S2 and S2p generates the level or steps in the output waveform and the other part consisting of switches T1, T2, T3 and T4 are responsible for polarity generation as it reverses the level which are produced by level generator [13]. The switches employed for the design and simulation of 5-level and 7-level multilevel inverter are insulated gate bipolar transistors, and the load that has been utilized is an RL load.

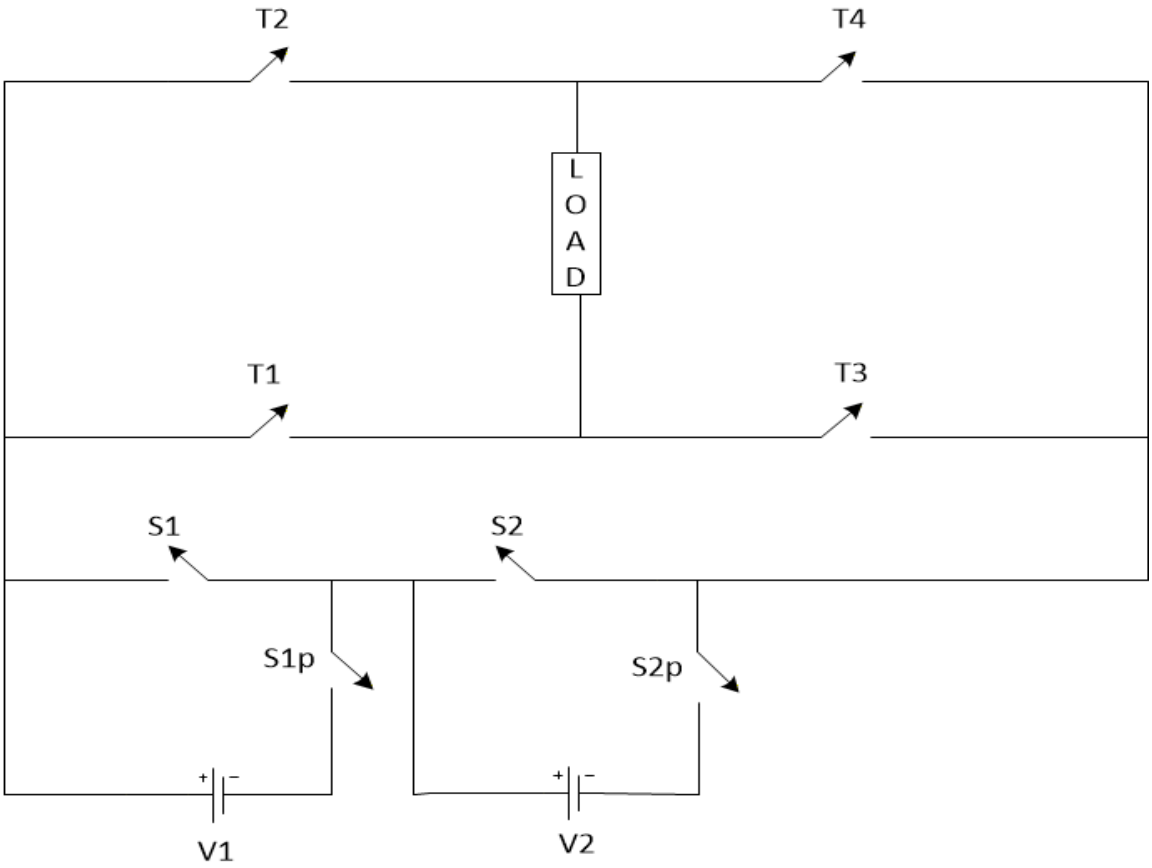


Fig. 3.2 Circuit diagram of 7-level reduced switch multilevel inverter

Table 3.2. Switching scheme for 7-level reduced switch topology

SWITCHING STATES(0=OFF,1=ON)								**OUTPUT VOLTAGE**
T1	T2	T3	T4	S1	S1p	S2	S2p	V0
0	1	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	V1
0	1	1	0	1	0	0	1	V2
0	1	1	0	0	1	0	1	V1+V2

1	0	0	1	0	1	1	0	-V1
1	0	0	1	1	0	0	1	-V2
1	0	0	1	0	1	0	1	-(V1+V2)

3.4 Five-Level and Seven-Level Reduced Switch Multilevel Inverter with filter

LC filter in which L stands for inductor and C for capacitor is being designed for the 5-level and 7-level reduced switch count multilevel inverter to enhance the efficiency of the MLI and reduce the total harmonic distortion. They are used to block or allow specific frequencies, depending on the purpose, it is termed as a band pass and band stop filter. The damping resistance has also been considered while designing the filter which is implemented on a 5-level and 7-level reduced switch multilevel inverter. The damping resistance is placed in series with the capacitor of the LC filter, which plays a significant role in damping out the oscillations, as there is a trade of energy between the capacitor and inductor which leads to voltage and current oscillations; thus, the damping resistor suppresses it. For design consideration, the ripple in inductor current is taken as 20 percent of the load current. The equations utilized for designing the LC filter for both the topologies are as follows;

$$\Delta I_L = \frac{Vdc}{4 * L * f_s} \qquad (3.1)$$

$$C = \frac{100}{4 * L * {f_s}^2 * \pi^2} \qquad (3.2)$$

The damping resistance has also been considered while designing the filter which is implemented on a 5-level and 7-level reduced switch multilevel inverter. The damping resistance is placed in series with the capacitor of the LC filter, which plays a significant role in damping out the oscillations, as there is a trade of energy between the capacitor and inductor which leads to voltage and current oscillations; thus, the damping resistor suppresses

it. The design of filter has been shown in Fig. 2 and the block diagram in Fig. 3 illustrates the construction and operation of the reduced switch multilevel inverter. The evaluation of damping resistance is done by using the formula described in the equation below, in which Є represents the damping ratio, which is taken as 0.7 for calculating the damping resistance of the designed filter to enhance the performance.

$$R = 2\epsilon * \sqrt{\frac{L}{C}} \qquad (3.3)$$

Where,

Vdc= Input Voltage

L= value of inductor in LC filter

C = value of the capacitor in the LC filter

f_s = switching frequency

ΔI_L = change in inductor current

R = value of damping resistance

Є = damping ratio

The values of the parameters selected for simulation are given in Table2.3

Table 3.3. Values of parameter selected for designing filter

Parameter	**Considered values**
Input Voltage	Vdc=20V 2Vdc=40V
RL Load	45 ohm and 55 mH
Filter Inductor	28.8 mH
Filter Capacitor	22 µF
Damping Resistance	50.6 ohm

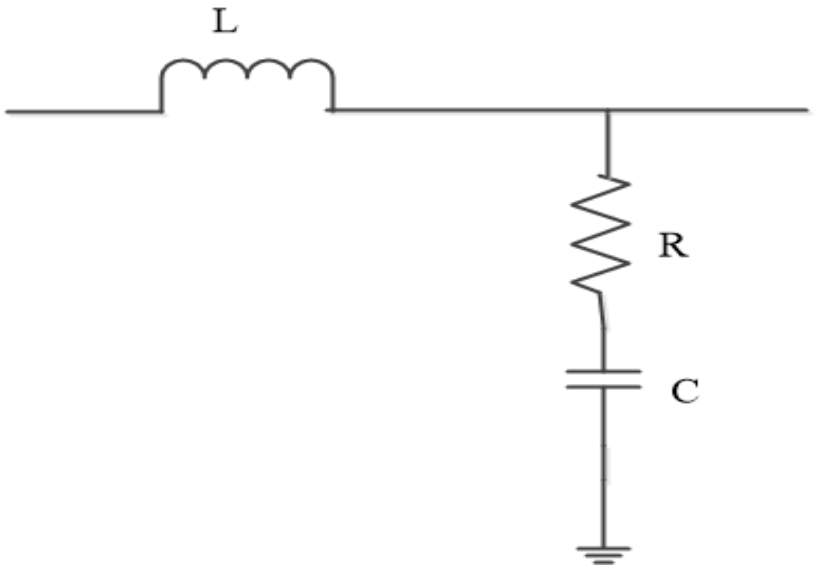


Fig. 3.3 LC filter with damping resistance

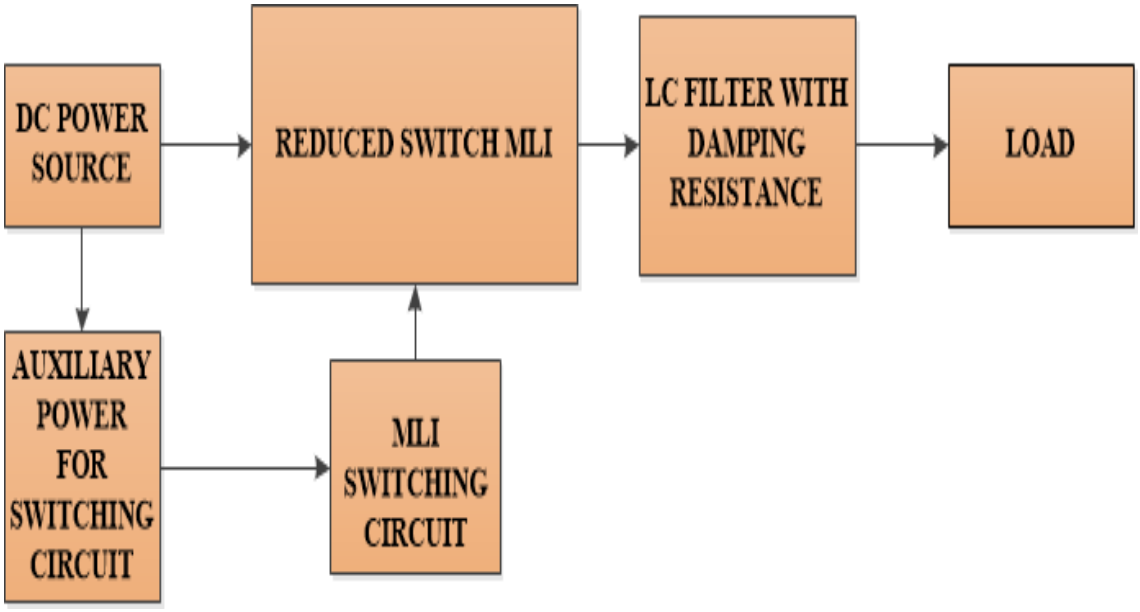


Fig.3.4: Block diagram of 5-level and 7-level reduced switch multilevel inverter with filter

3.5. Simulation Results

This chapter consists of the simulation model and results obtained for the 5-level, 7-level reduced switch MLI and also with the designed filter multilevel inverter. The THDs have been compared for the 5-level and 7-level reduced switch MLI with and without taking the filter into consideration.

3.5.1 Five-level Reduced Switch MLI

The simulation model for 5-level reduced switch MLI is shown in the Fig. 3.1 below in which T1, T2, T3 and T4 are the IGBT switches which are responsible for polarity generation and S1, S1p, S2 and S2p generate the level or steps;

The Fig. 3.7 illustrates the results procured on simulating the design of 5-level reduced switch MLI, which is, the voltage waveform and the THD obtained.

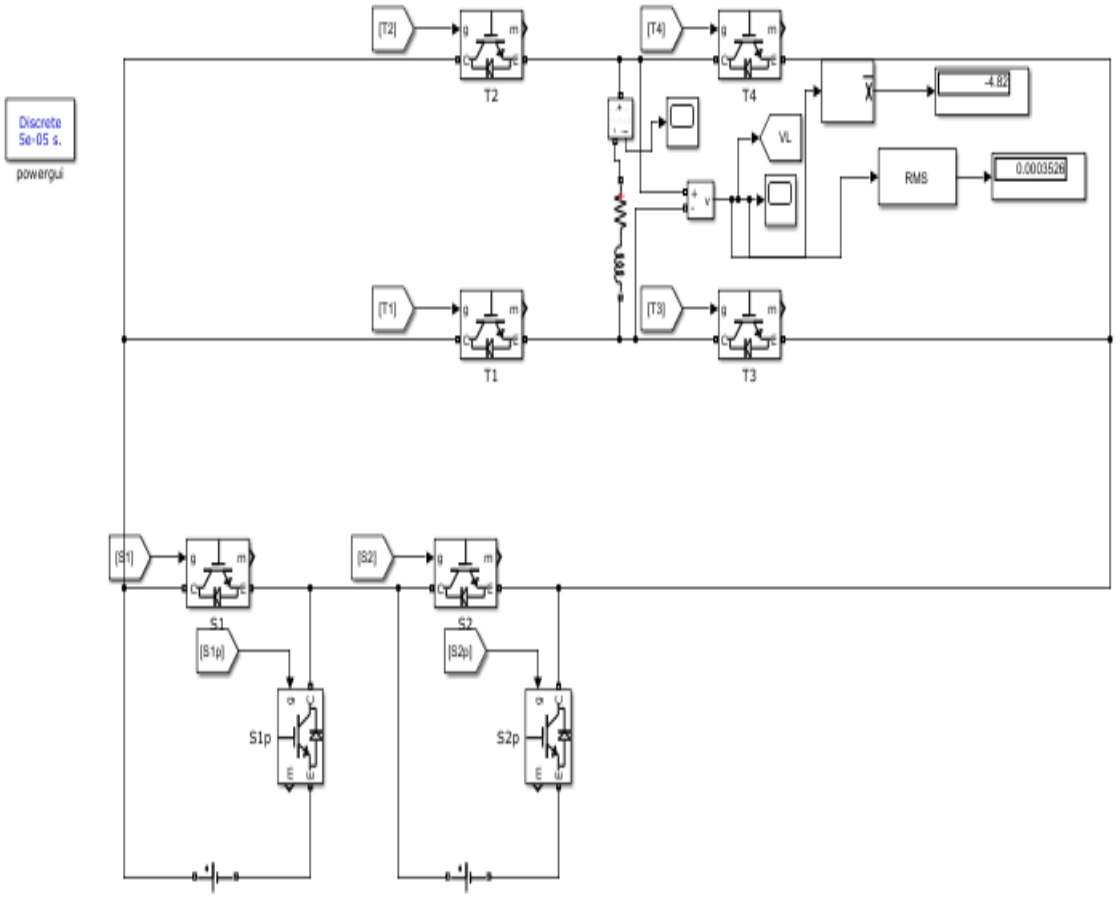


Fig.3.5: Simulation of 5-level Reduced switch multilevel inverter topology

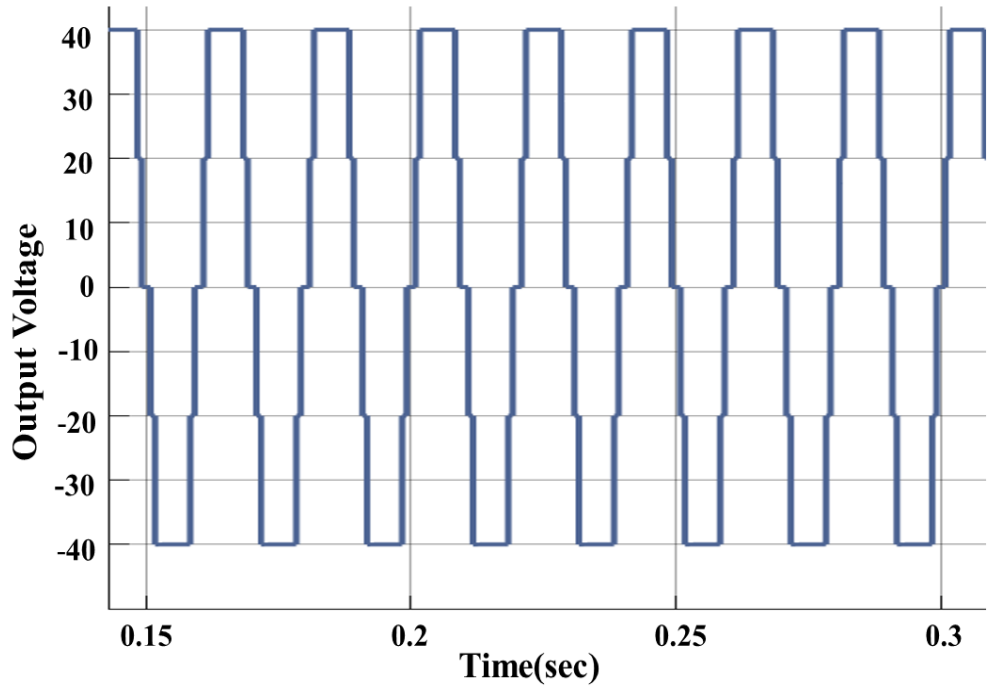


Fig. 3.6: Voltage waveform of 5-level Reduced switch multilevel inverter topology

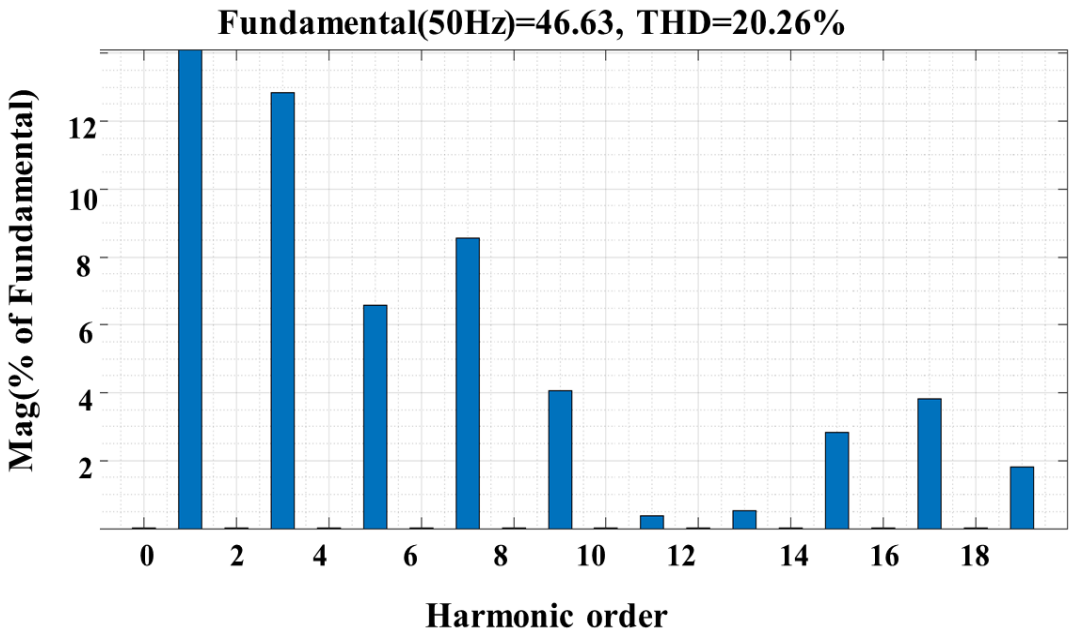


Fig3.7. THD for 5-level Reduced switch MLI

3.5.2 Seven-level Reduced Switch Multilevel Inverter

The results obtained for 7-level topology for voltage waveform and THD analysis are represented below in Fig. 3.3. In Fig. 3.2, T1, T2, T3 and T4 are the IGBT switches that are responsible for polarity generation, and S1, S1p, S2 and S2p generate the levels.

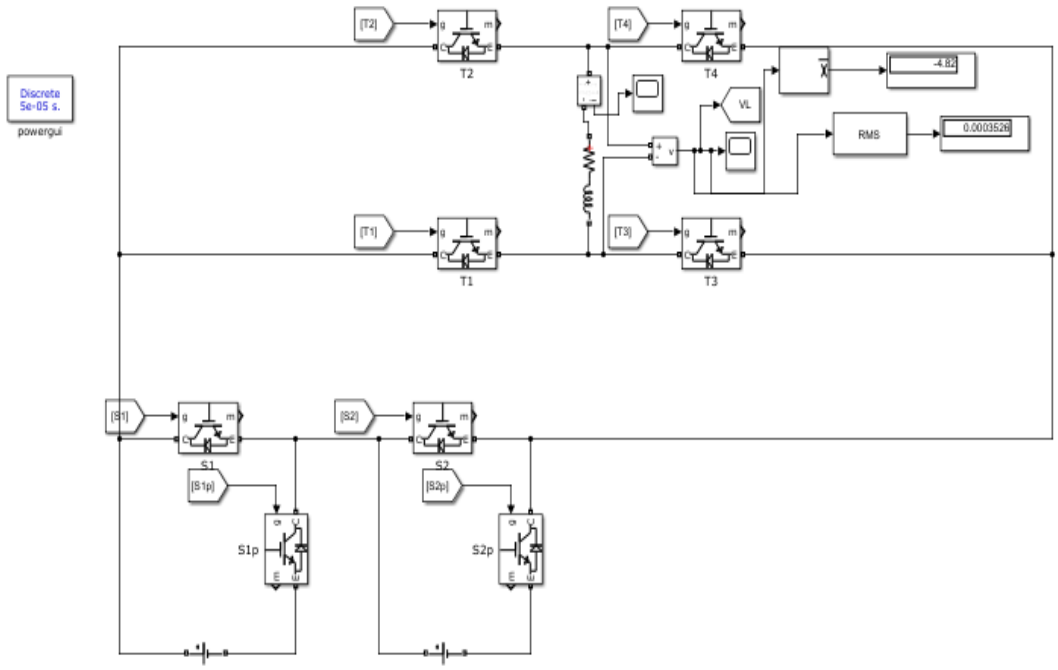


Fig3.8: Simulation of a 7-level reduced switch multilevel inverter topology

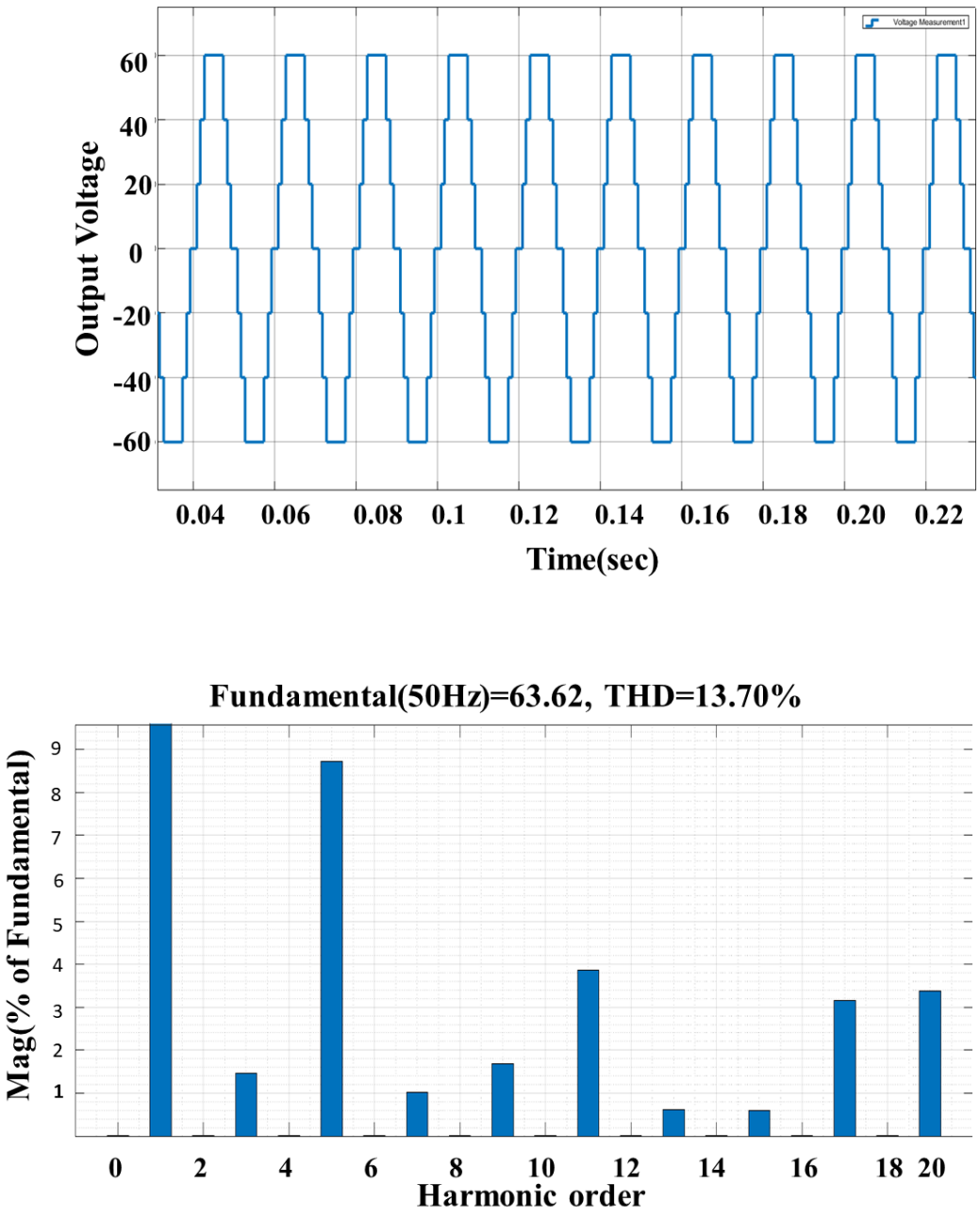


Fig. 3.9: Voltage waveform and THD analysis for 7-level Reduced Switch MLI

3.5.3 Five-Level Reduced Switch Multilevel Inverter with filter

The simulation design of 5-level reduced switch MLI is represented in Fig. 3.4 in which T1, T2, T3 and T4 are the IGBT switches that are responsible for polarity generation, and S1, S1p, S2 and S2p generate the levels, along with it LC filter is added before the RL load.

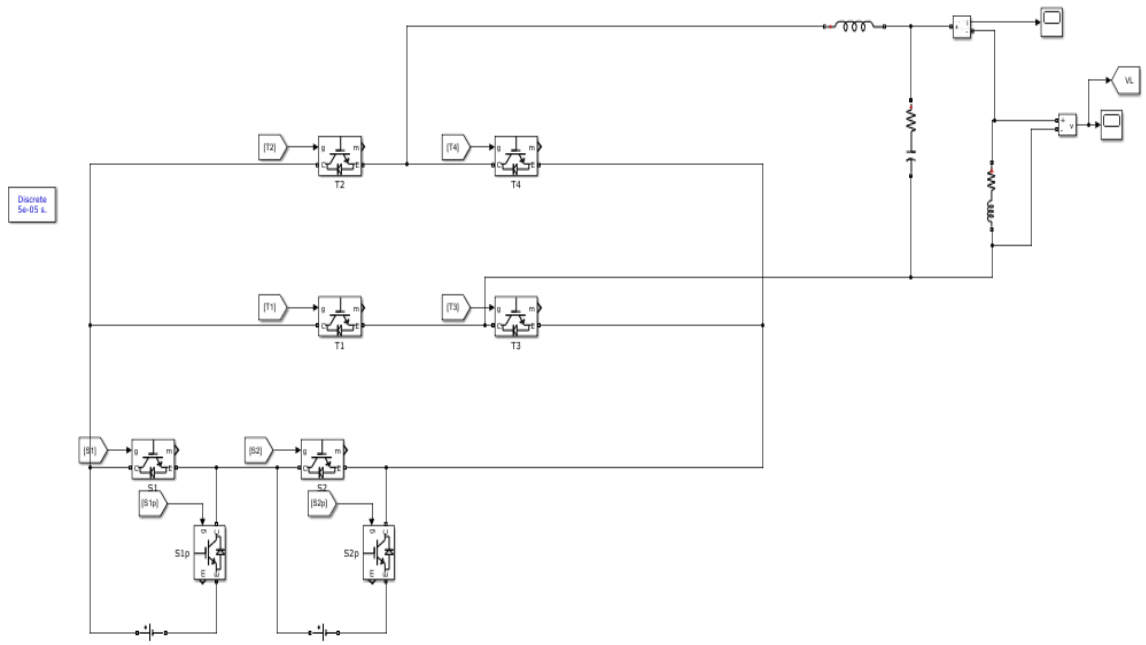
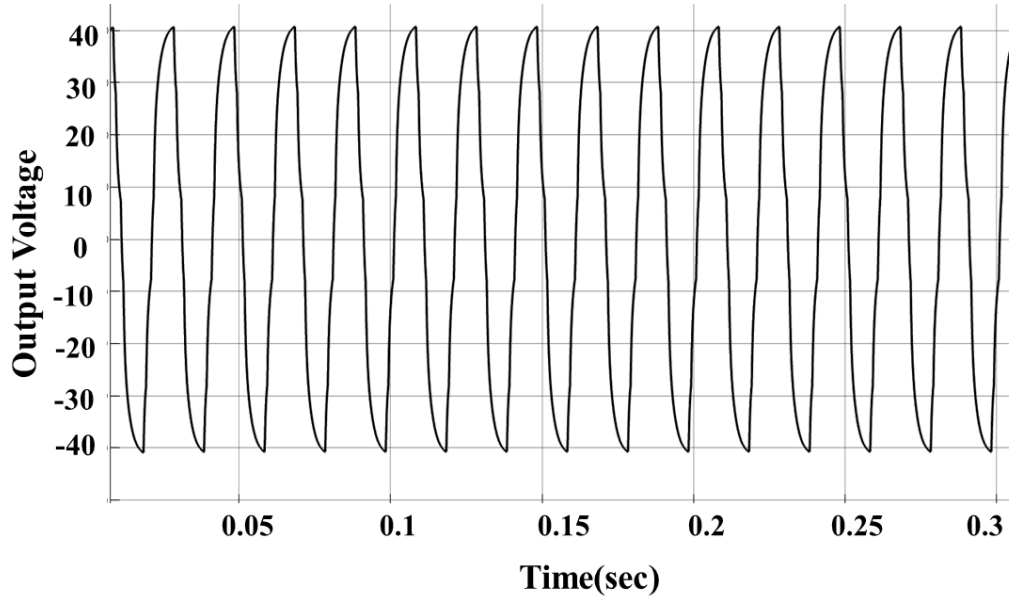


Fig. 3.10: Simulation diagram of 5-Level Reduced Switch MLI with filter

The results procured on adding a filter to the 5-level reduced switch MLI on voltage waveform is represented in Fig. 3.5 and Fig. 3.6 represents the THD obtained on simulating the designed MLI with the filter.



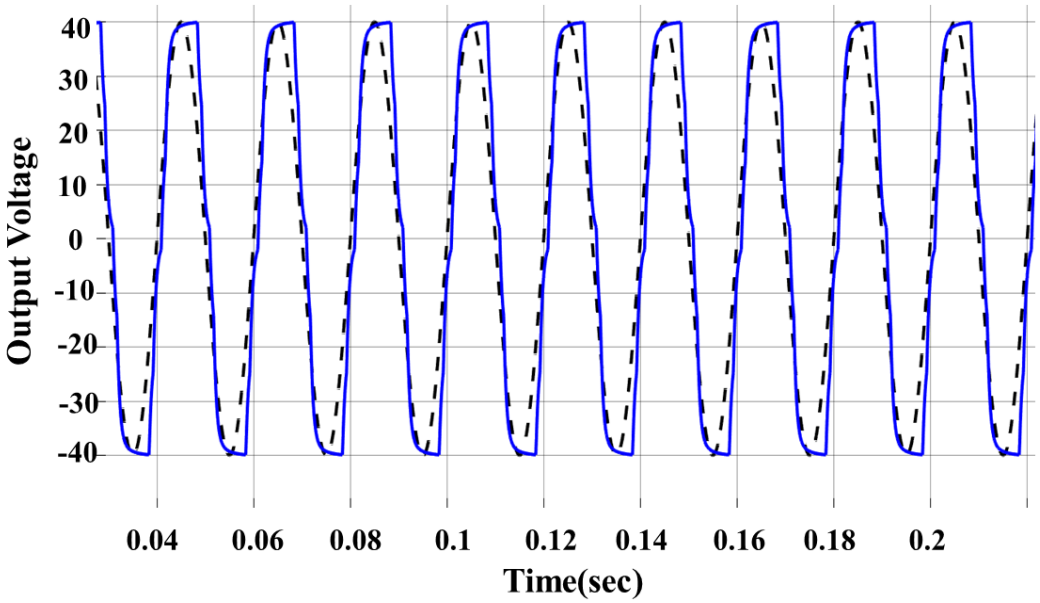


Fig. 3.11: Voltage waveform of 5-level with filter and Voltage waveform of 5-level with sine reference

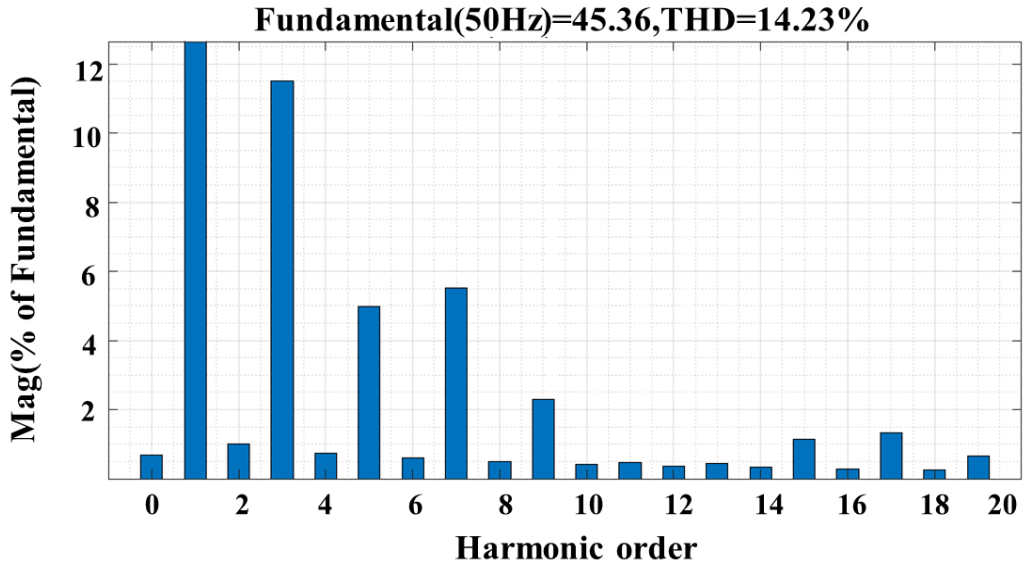


Fig. 3.12: THD of 5-level reduced switch MLI with filter

3.5.4 Seven-Level Reduced Switch Multilevel Inverter with filter

The simulation design of 7-level reduced switch MLI is represented in Fig. 3.7 in which T1, T2, T3 and T4 are the IGBT switches that are responsible for polarity generation, and S1, S1p, S2 and S2p generate the levels, with it LC filter is added along with damping resistance

before the RL load to damp out the oscillations caused by inductor and capacitor and get smoother and ripple free waveforms.The results procured on adding a filter to the 7-level reduced switch MLI on voltage waveform is represented in Fig. 3.8 and represents the THD obtained on simulating the designed MLI with the filter.

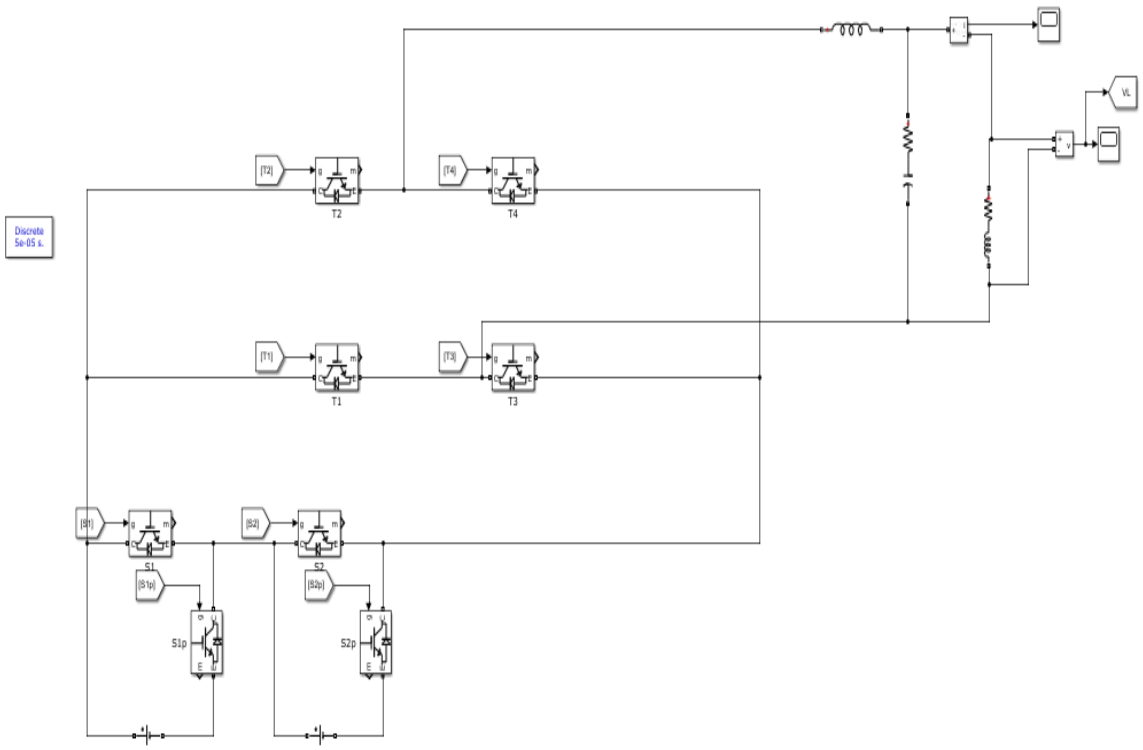
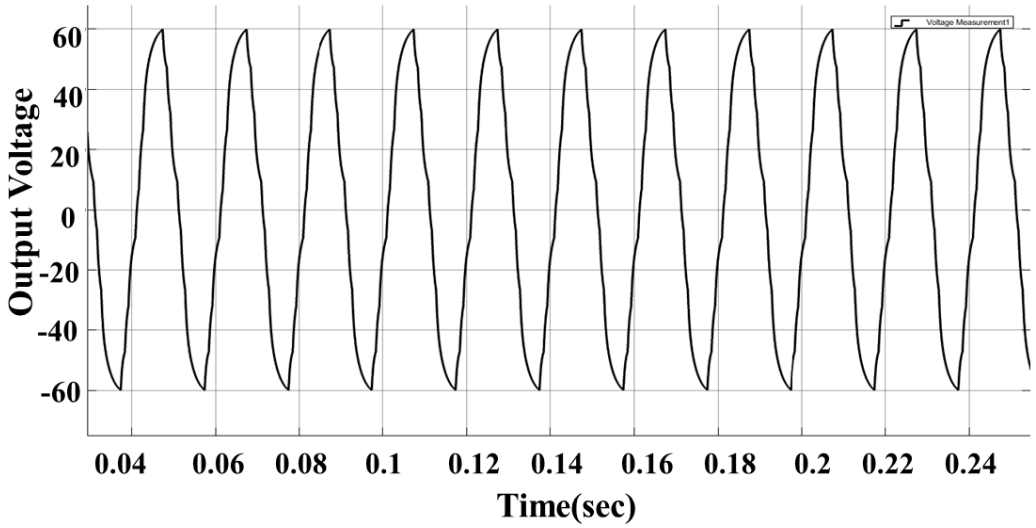


Fig. 3.13: Simulation of 7-level reduced switch MLI with filter



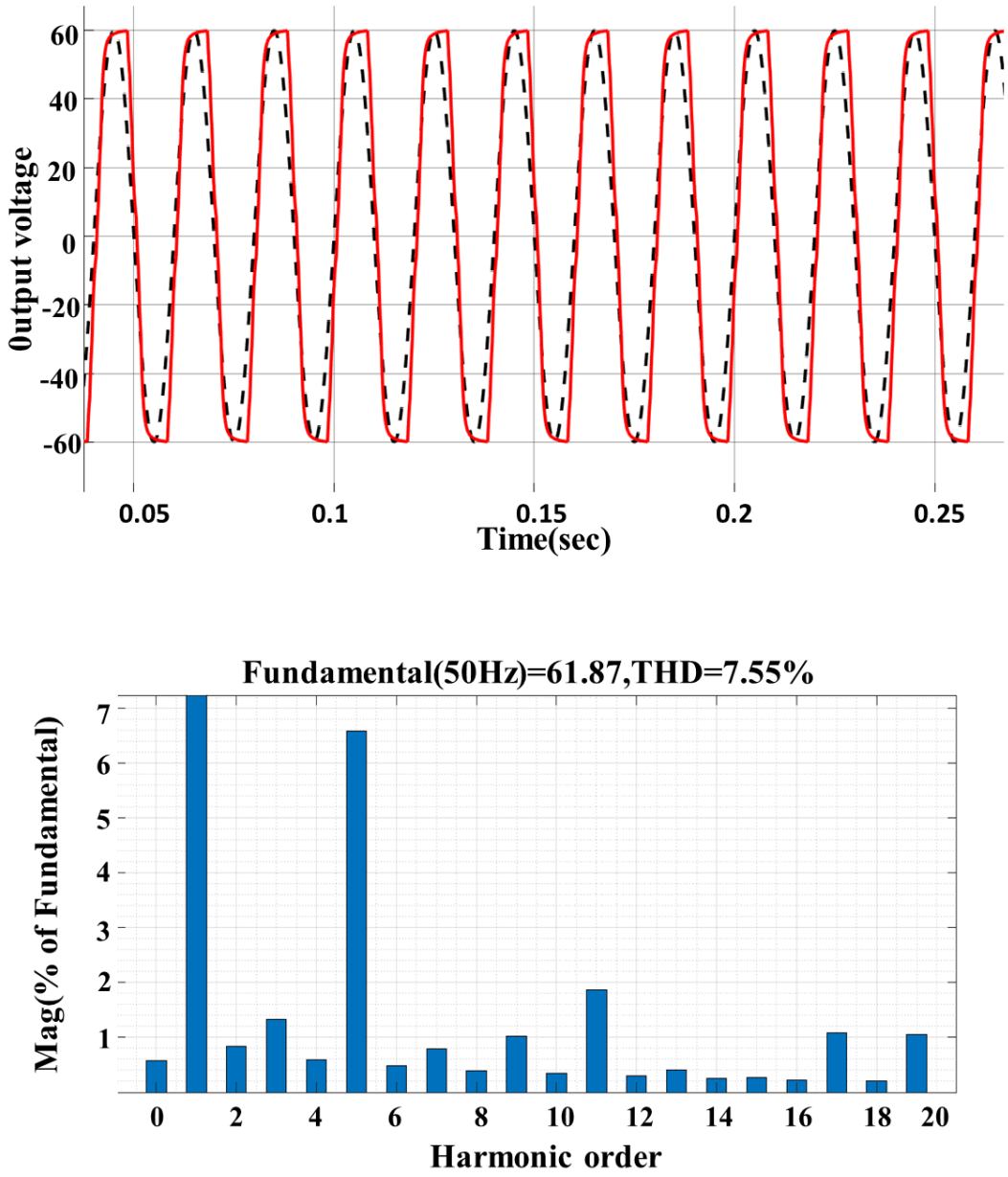


Fig. 3.14: Voltage waveform and THD of 7-level reduced switch MLI

3.6. Discussion

The THD exhibited by the 5 and 7-level reduced switch multilevel inverter without filter and with LC filter along with damping resistance has been discussed and compared in Table 3.4. below:

Table 3.4: Comparison of THD's for 5 and 7-level reduced switch Multilevel inverter

Reduced Switch Multilevel inverter	THD without filter	THD with LC filter
5- level	20.26%	14.23%
7-Level	13.70%	7.55%

3.7. Conclusion

Simulating the design of a five-level and seven-level reduced switch multilevel inverter yielded THDs of 20.26% and 13.70%, respectively. Furthermore, the THD that has been recorded when the LC filter and damping resistance are applied is 14.23% and 7.55%, respectively, which is almost half for 7-level. Applying the specified filter, that is, LC filter with damping resistance to the reduced switch topology of 5 and 7 level MLI has therefore significantly improved the THD, as can be seen by comparing the results in both the cases.

CHAPTER-4

31 and 63 LEVEL REDUCED SWITCH MLI WITH PASSIVE FILTER

4.1. INTRODUCTION

This chapter presents the advanced and more economic design of a 31-level reduced switch MLI consisting of 12 switches and 4 DC voltage sources along with a passive filter to further reduce the THD and 63-level reduced switch MLI with 14 power electronic switches and 5 DC sources with passive filter thus making it more compatible for many advanced applications. The passive filters implemented with the converter include the designed LCL and LC filter, and the effect on THD has also been evaluated.

4.2. Thirtyone(31)-level and Sixtythree(63)-level Reduced switch MLI

The 31 level reduced switch topology of MLI consists of 4 DC sources 12 power electronic switches, which are distributed as 4 switches which are T1, T2, T3, T4 for generating polarity in the output waveform ,that is, positive and negative half in the output and the other 10 switches which are S1,S2,S3,S4,S1P,S2P,S3P,S4P are responsible for generating the steps in the output voltage waveform depending on the switching of these switches and similarly 63-level reduced switch MLI requires 5 DC sources and 14 power electronic switches for polarity and step generation[13]. The switches employed for the design and simulation of multilevel inverter are insulated gate bipolar transistors, and the load that has been utilized is an RL load.

For both the topologies of reduced switch MLI, during the positive half cycle T1 and T2 conducts from polarity generator circuit and current flows from positive to negative and during the other half cycle which is negative half cycle T3 and T4 conducts and the current flows from negative to positive, thus creating the positive and negative polarity in the output and meanwhile the level generating switches generates the steps in the voltage output waveform based on the switching provided using the switching circuit[25]-[26].Logic based switching is involved which is depicted in Table4.1 and Table4.2 for 31 level and 63 level respectively, and the circuit diagram consisting of level and polarity generation parts of circuit is depicted in Fig4.1 and 4.2 .

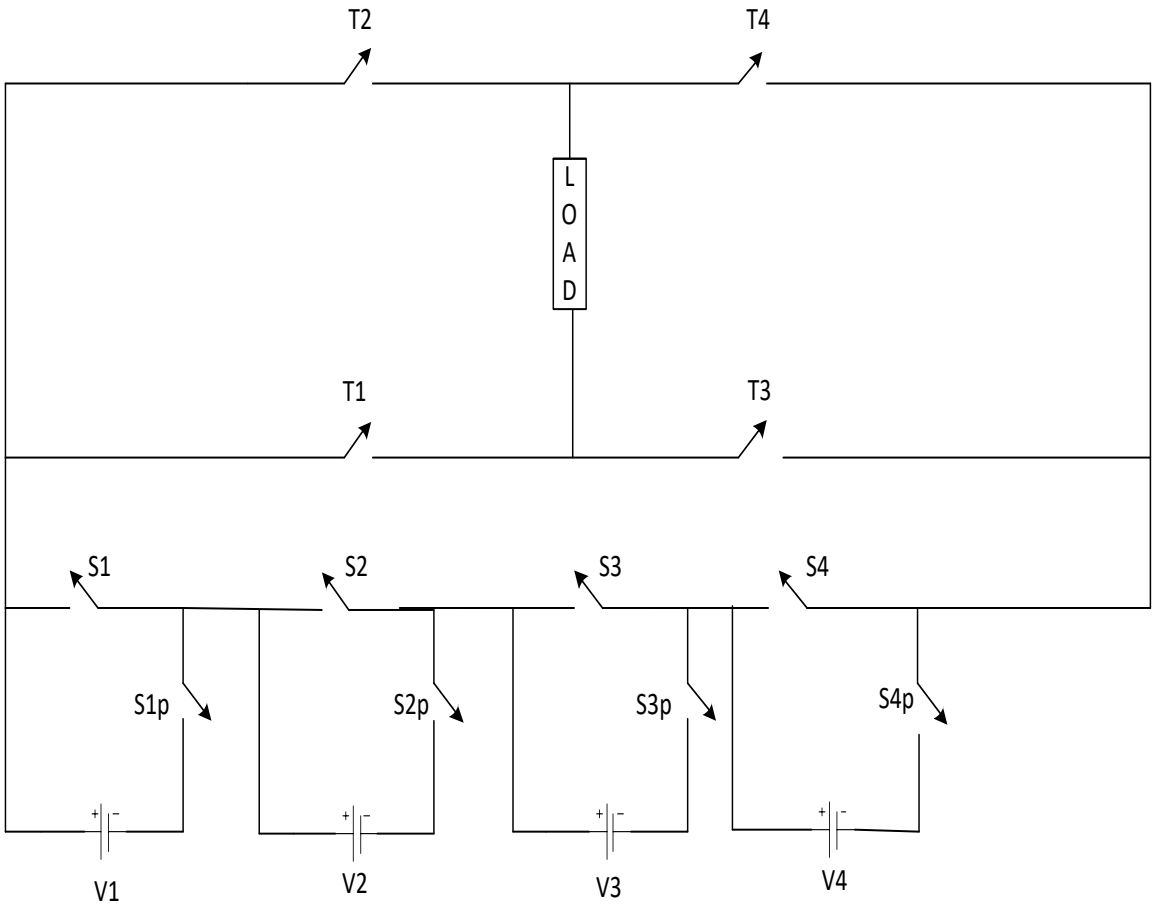


Fig. 4.1: 31 level Reduced Switch MLI circuit diagram

Table4.1: Switching of 31 level reduced switch MLI for positive half cycle

SWITCHING STATES												**OUTPUT VOLTAGE**
T1	T2	T3	T4	S1	S1p	S2	S2p	S3	S3P	S4	S4P	V0
0	1	1	0	1	0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	1	0	1	0	V1
0	1	1	0	1	0	0	1	1	0	1	0	V2
0	1	1	0	0	1	0	1	1	0	1	0	V1+V2

0	1	1	0	1	0	1	0	0	1	1	0	V3
0	1	1	0	0	1	1	0	0	1	1	0	V1+V3
0	1	1	0	1	0	0	1	0	1	1	0	V2+V3
0	1	1	0	0	1	0	1	0	1	1	0	V1+V2+V3
0	1	1	0	1	0	1	0	1	0	0	1	V4
0	1	1	0	0	1	1	0	1	0	0	1	V1+V4
0	1	1	0	1	0	0	1	1	0	0	1	V2+V4
0	1	1	0	0	1	0	1	1	0	0	1	V1+V2+V4
0	1	1	0	1	0	1	0	0	1	0	1	V3+V4
0	1	1	0	0	1	1	0	0	1	0	1	V1+V3+V4
0	1	1	0	1	0	0	1	0	1	0	1	V2+V3+V4
0	1	1	0	0	1	0	1	0	1	0	1	V1+V2+V3+ V4

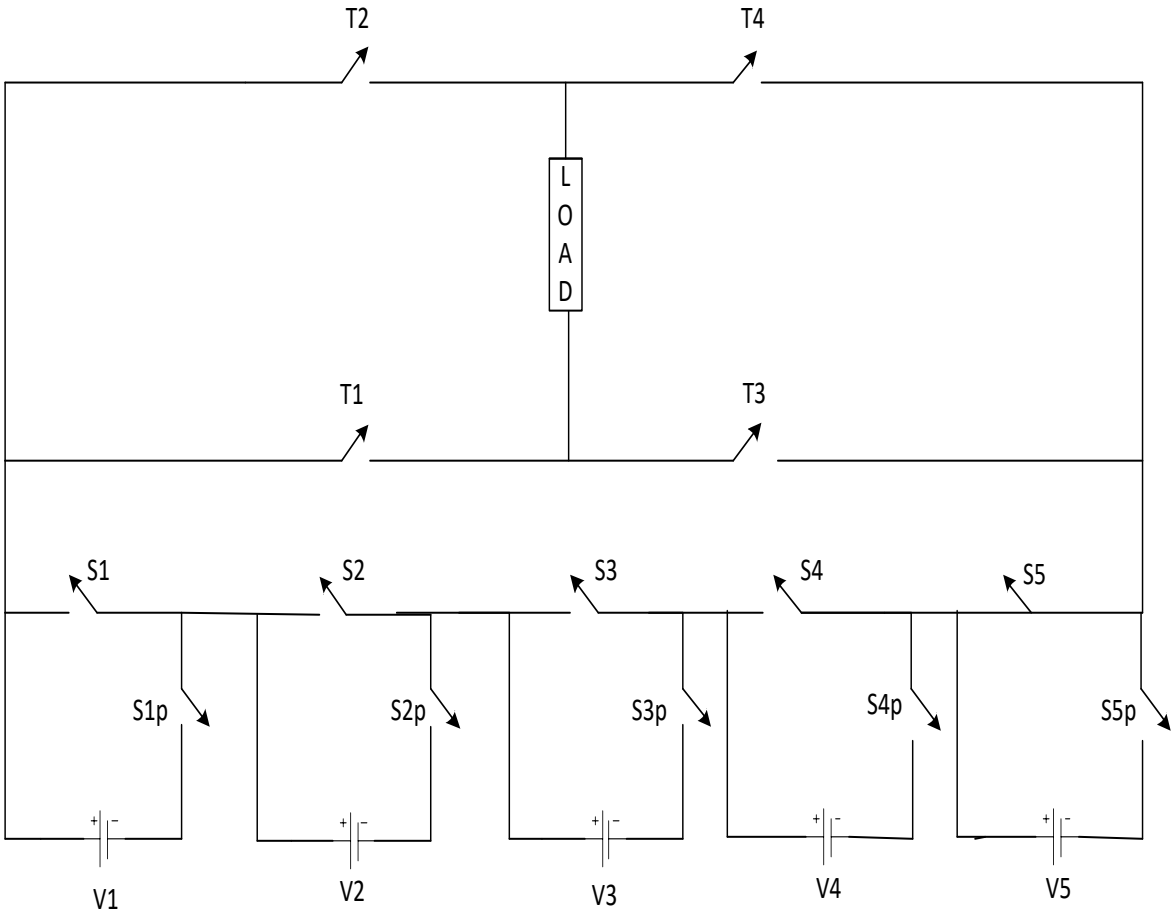


Fig. 4.2: 63 LEVEL Reduced switch MLI Circuit Diagram

Table 4.2: Switching of 63 level reduced switch MLI for positive half cycle

SWITCHING STATES														**OUTPUT VOLTAGE**
T1	T2	T3	T4	S1	S1p	S2	S2p	S3	S3P	S4	S4P	S5	S5P	V0
0	1	1	0	1	0	1	0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	0	1	0	1	0	1	0	V1
0	1	1	0	1	0	0	1	1	0	1	0	1	0	V2
0	1	1	0	0	1	0	1	1	0	1	0	1	0	V1+V2

0	1	1	0	1	0	1	0	0	1	1	0	1	0	V3
0	1	1	0	0	1	1	0	0	1	1	0	1	0	V1+V3
0	1	1	0	1	0	0	1	0	1	1	0	1	0	V2+V3
0	1	1	0	0	1	0	1	0	1	1	0	1	0	V1+V2+V3
0	1	1	0	1	0	1	0	1	0	0	1	1	0	V4
0	1	1	0	0	1	1	0	1	0	0	1	1	0	V1+V4
0	1	1	0	1	0	0	1	1	0	0	1	1	0	V2+V4
0	1	1	0	0	1	0	1	1	0	0	1	1	0	V1+V2+V4
0	1	1	0	1	0	1	0	0	1	0	1	1	0	V3+V4
0	1	1	0	0	1	1	0	0	1	0	1	1	0	V1+V3+V4
0	1	1	0	1	0	0	1	0	1	0	1	1	0	V2+V3+V4
0	1	1	0	0	1	0	1	0	1	0	1	1	0	V1+V2+V3 +V4
0	1	1	0	1	0	1	0	1	0	1	0	0	1	V5
0	1	1	0	0	1	1	0	1	0	1	0	0	1	V1+V5
0	1	1	0	1	0	0	1	1	0	1	0	0	1	V2+V5
0	1	1	0	0	1	0	1	1	0	1	0	0	1	V1+V2+V5
0	1	1	0	1	0	1	0	0	1	1	0	0	1	V3+V5
0	1	1	0	0	1	1	0	0	1	1	0	0	1	V1+V3+V5
0	1	1	0	1	0	0	1	0	1	1	0	0	1	V2+V3+V5
0	1	1	0	0	1	0	1	0	1	1	0	0	1	V1+V2+V3 +V5
0	1	1	0	1	0	1	0	1	0	0	1	0	1	V4+V5

0	1	1	0	0	1	1	0	1	0	0	1	0	1	V1+V4+V5
0	1	1	0	1	0	0	1	1	0	0	1	0	1	V2+V4+V5
0	1	1	0	0	1	0	1	1	0	0	1	0	1	V1+V2+V4 +V5
0	1	1	0	1	0	1	0	0	1	0	1	0	1	V3+V4+V5
0	1	1	0	0	1	1	0	0	1	0	1	0	1	V1+V3+V4 +V5
0	1	1	0	1	0	0	1	0	1	0	1	0	1	V2+V3+V4 +V5
0	1	1	0	0	1	0	1	0	1	0	1	0	1	V1+V2+V3 +V4+V5

4.3. Passive filter Design applied to 31 and 63-level MLI

Passive filter which are used for attenuating certain frequencies. LC and LCL are applied before the RL load in the 31 and 63 level reduced switch MLI to smoothen out the levels generated in the output voltage waveform to produce less distorted voltage waveform with lower THD and therefore much more similar to sinusoidal waveform. The THD have been evaluated and compared first by applying the designed LC filter and then by applying the designed LCL filter before load. The equations involved in designing LC and LCL filters are demonstrated in (1),(2),(3) and(4), (5), (6)respectively. The filer design has been shown in Fig. 4.3 and 4.4.

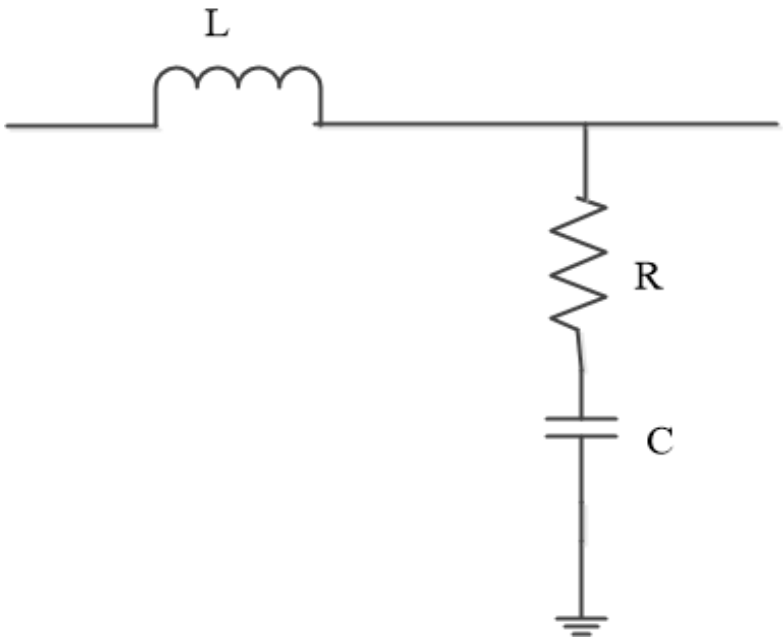


Fig. 4.3: LC Filter design implemented for Reduced switch MLI

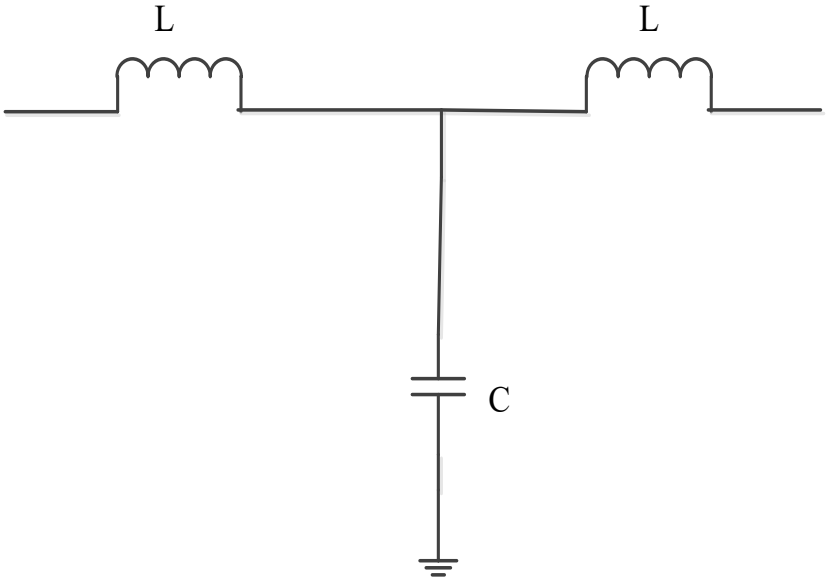


Fig. 4.4: LCL Filter design for Reduced Switch MLI

$$\Delta I_L = \frac{Vdc}{4 * L * f_s} \qquad (4.1)$$

$$C = \frac{100}{4 * L * {f_s}^2 * \pi^2} \qquad (4.2)$$

$$R = 2\epsilon * \sqrt{\frac{L}{C}} \quad (4.3)$$

$$L_1 = \frac{Vdc}{6 * \Delta I_L * f_s} \quad (4.4)$$

$$L_2 = 0.5L_1 \quad (4.5)$$

$$C = \frac{0.05 * S}{V^2 * 2 * \pi * f} \quad (4.6)$$

Where,

Vdc= Input Voltage

L= value of inductor in LC filter

C = value of the capacitor in the LC filter

f_s = switching frequency

ΔI_L = change in inductor current

R = value of damping resistance

ϵ = damping ratio

L_1 =value of inductor in LCL filter

L_2=value of inductor before load in LCL filter

The values of parameters selected for simulation are provided in the Table4.3 for 31 level and Table 4.4 for 63 level

Table 4.3: Values of parameters selected for designing the 31-level Reduced Switch MLI

Parameter	**Considered values**
Input Voltage	V1=15V, V2=30V, V3=60V, V4=120V
RL Load	45 ohm and 55 mH
LC Filter Inductor	11.25 mH
Filter Capacitor	9.2 μF

Damping Resistance	50 ohm
LCL Filter Inductor(L1)	7.5 mH
LCL Filter Inductor(L2)	4 mH
LCL Filter Capacitor	3.6 μF

Table 4.4: Values of parameters selected for designing the 63-level Reduced Switch MLI

Parameter	**Considered values**
Input Voltage	V1=15V, V2=30V, V3=60V, V4=120V, V5=240V
RL Load	45 ohm and 55 mH
Filter Inductor	5.63 mH
Filter Capacitor	4.49 μF
Damping Resistance	50 ohm
LCL Filter Inductor(L1)	3.75 mH
LCL Filter Inductor(L2)	1.8 mH
LCL Filter Capacitor	3.6 μF

CHAPTER 5

RESULT AND DISCUSSION

5.1. INTRODUCTION

This chapter presents the results obtained for 31-level and 63-level Reduced Switch MLI . It includes the Total Harmonic Distortion graphs for 31-level and 63-level reduced switch MLI without applying any filteration technique and also the THD graph obtained with designed LC and LCL filter. The voltage waveforms obtained are also presented for each 31-level and 63-level with and without filter. The voltage waveforms also include reference sine wave and enlarged steps view.

5.2. Thirtyone(31) and Sixtythree(63)-level MLI

The output voltage waveform produced on simulating the design of a 31 and 63-level reduced switch MLI with 4 dc sources for 31 level and 5 dc sources for 63 level, where V1=Vdc, V2=2Vdc, V3=4Vdc and so on and 12 and 14 power electronic switches for 31 level and 63 level respectively, 4 of which are involved in polarity generation part of the circuit and the rest in step generation, has been demonstrated in Fig. 5.3 and 5.8. The simulation circuits are depicted in Fig. 5.1 and 5.6.

The THD in the output voltage waveform of a 31-level and 63-level reduced switch MLI without applying any kind of filter has been demonstrated in Fig. 5.2 and 5.7. Fig. 5.4 presents the clear and enlarged view of 31-levels obtained on simulating the design of 31-level reduced switch topology and Fig. 5.9 presents the enlarged view of all 63-level obtained.

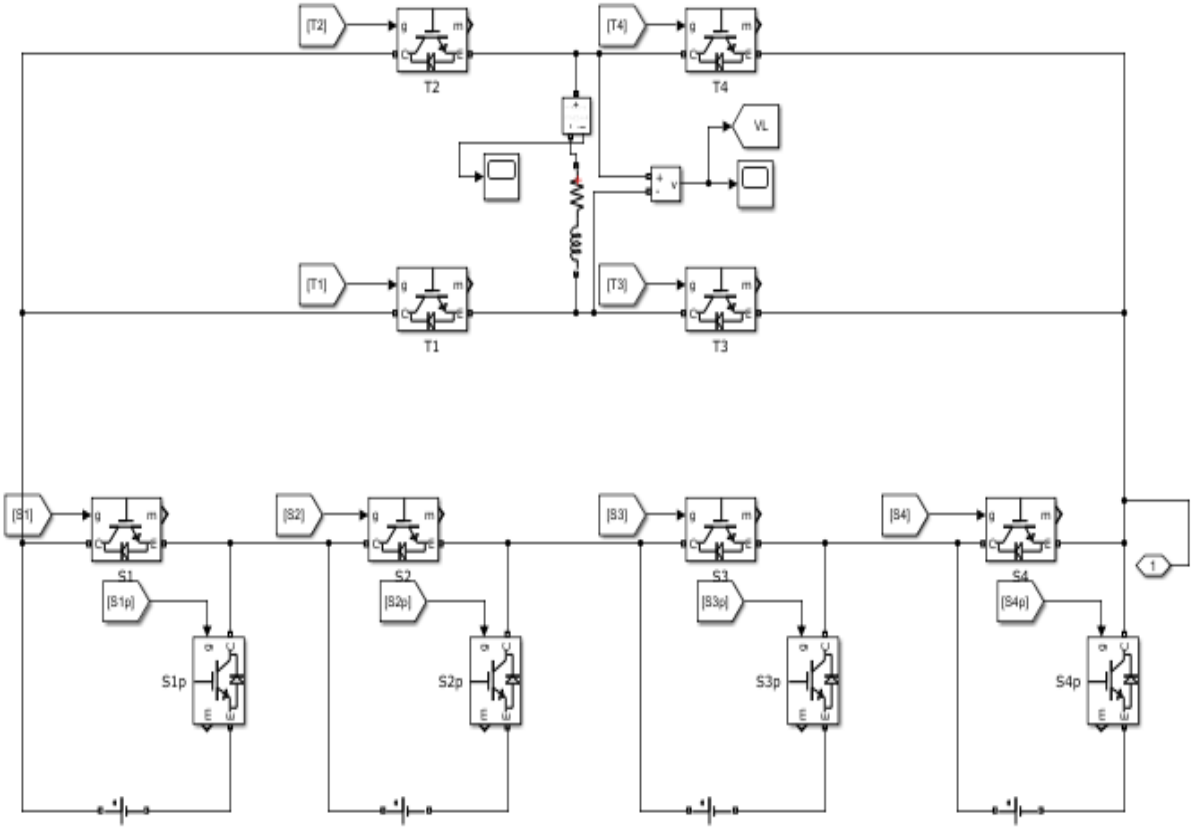


Fig. 5.1: Simulation Circuit of 31-level Reduced Switch MLI

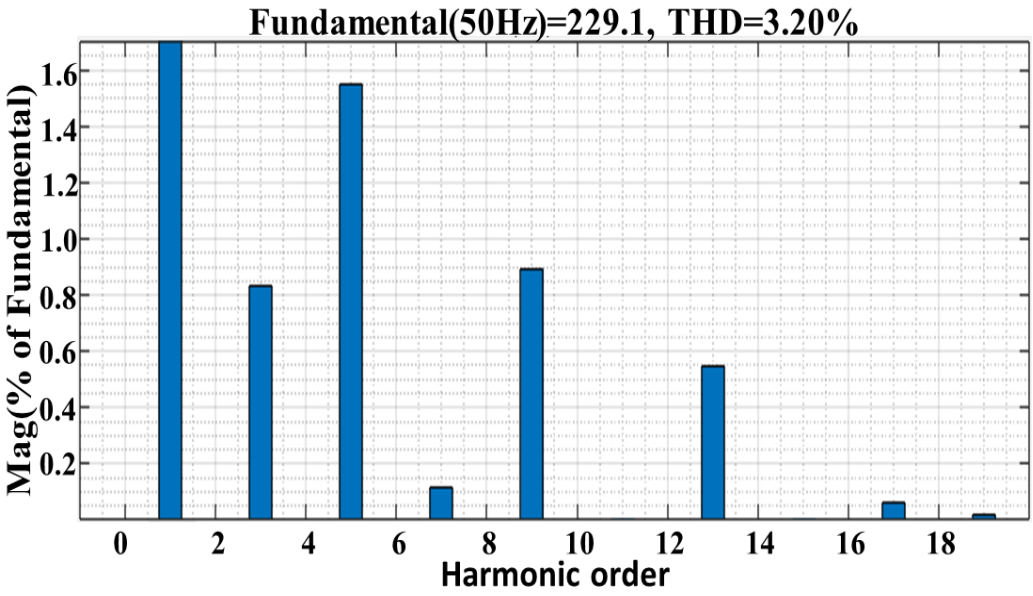


Fig. 5.2: THD of 31 level Reduced Switch MLI without filter

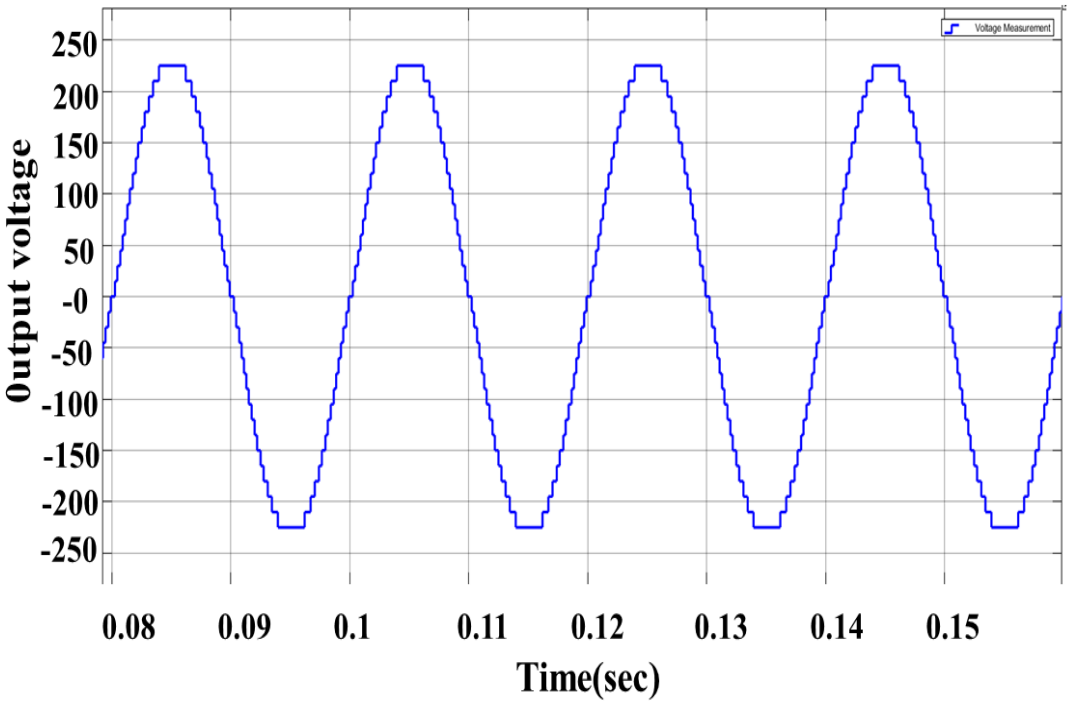


Fig. 5.3: Voltage waveform of 31 level Reduced Switch MLI without filter

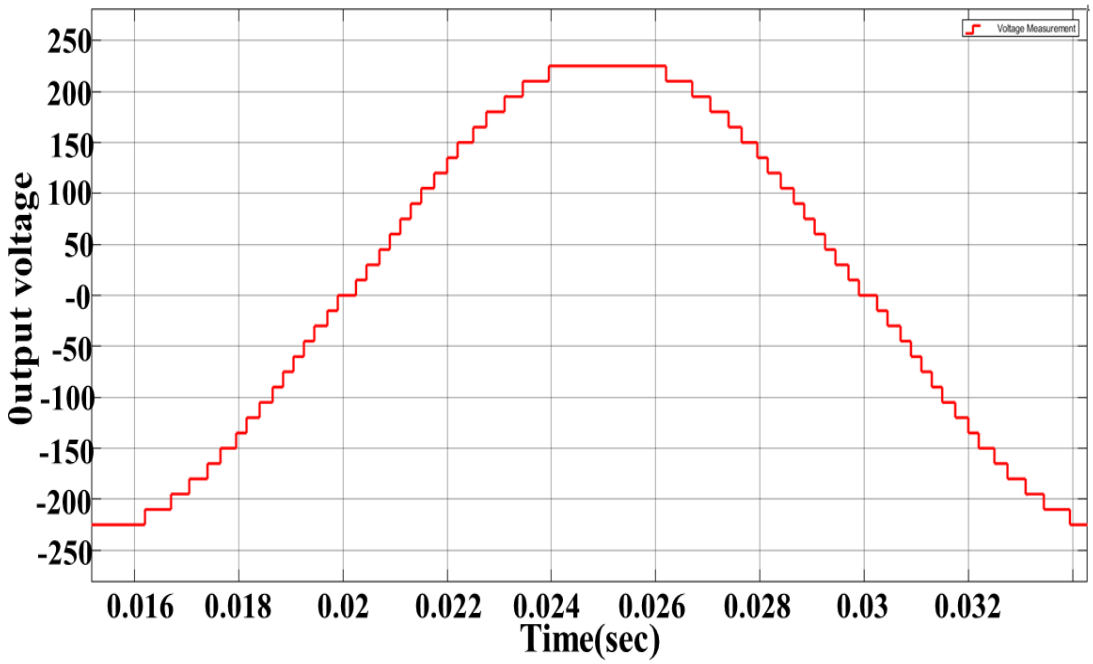


Fig. 5.4: Enlarged view of 31 levels of output voltage

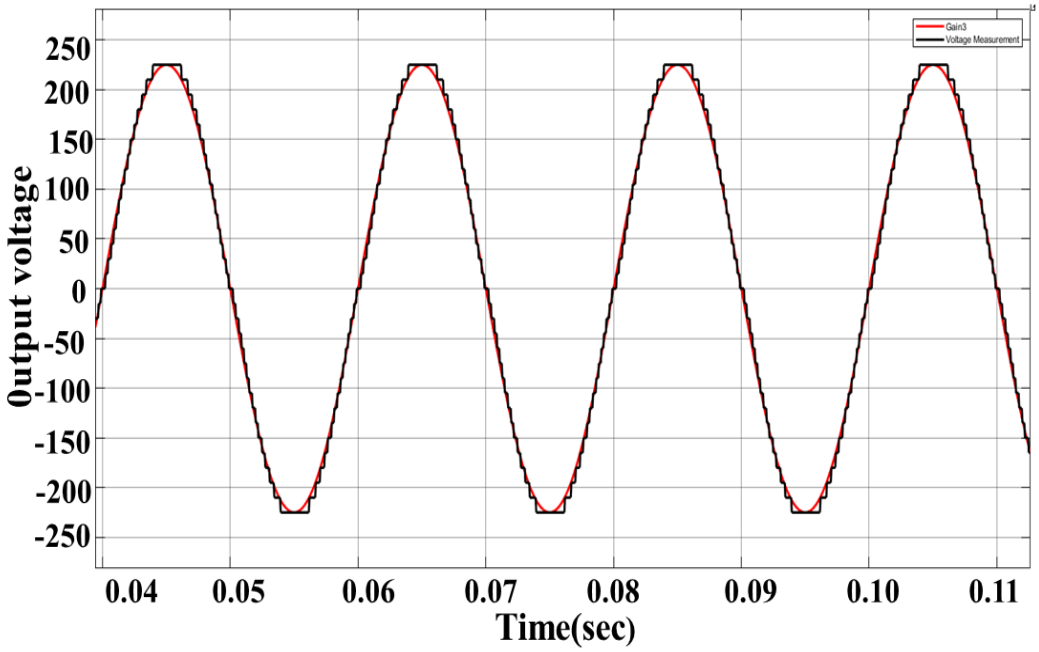


Fig. 5.5: Voltage waveform of 31 level reduced switch MLI with sine reference

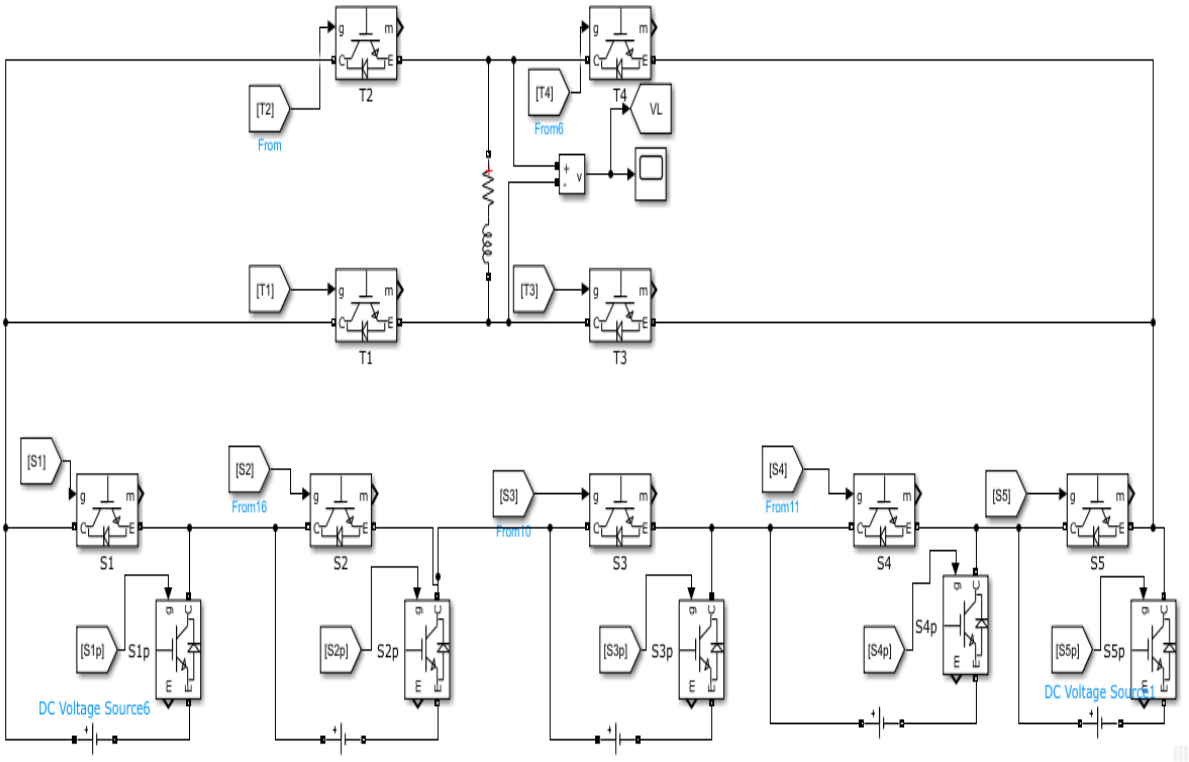


Fig. 5.6: 63-level Reduced Switch MLI

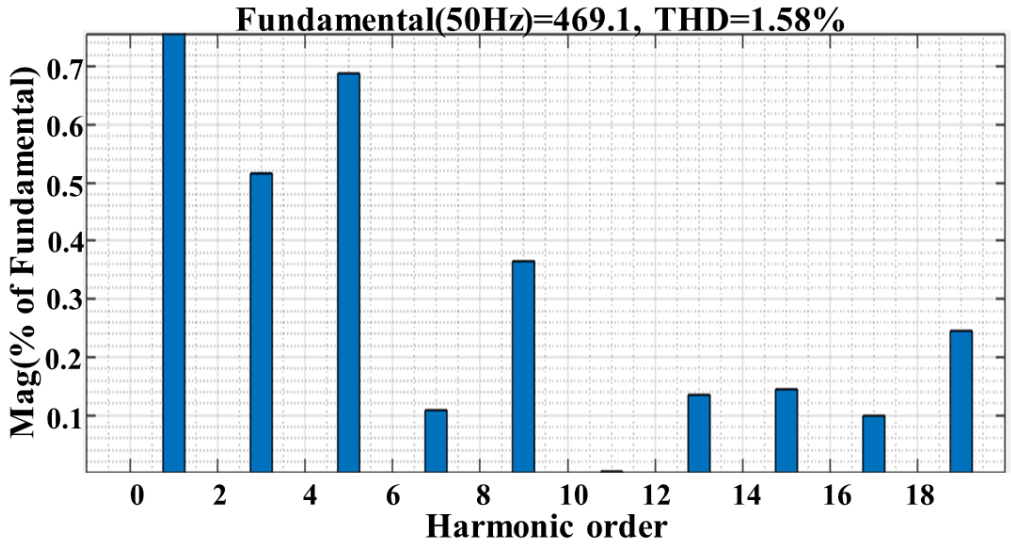


Fig. 5.7: THD of 63 level Reduced Switch MLI without filter

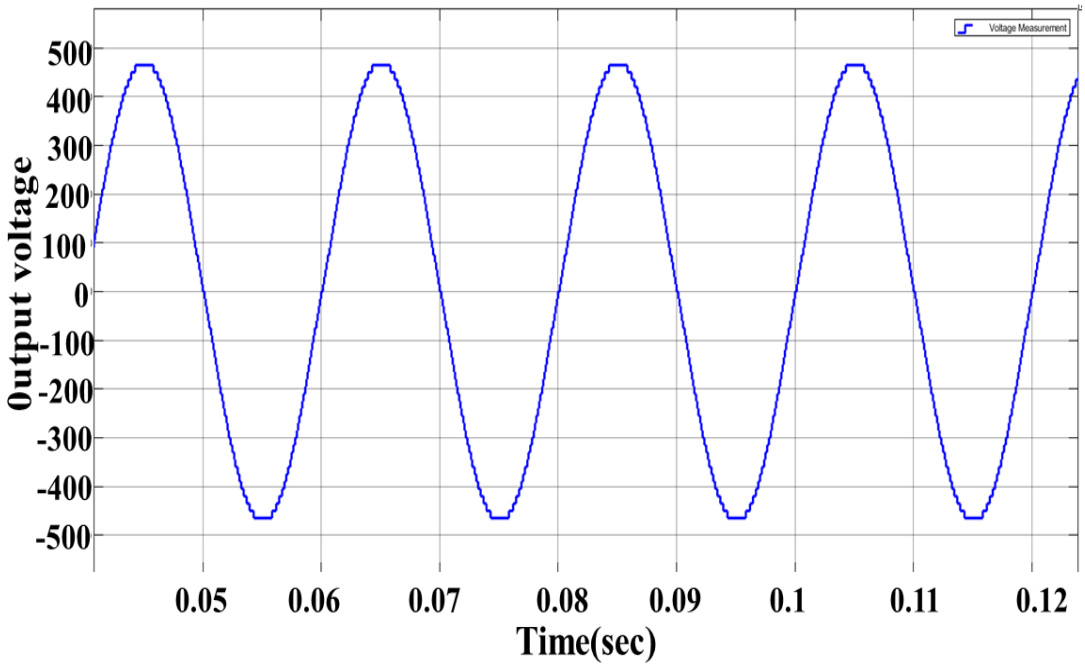


Fig. 5.8: Voltage waveform of 63 level reduced switch MLI without filter

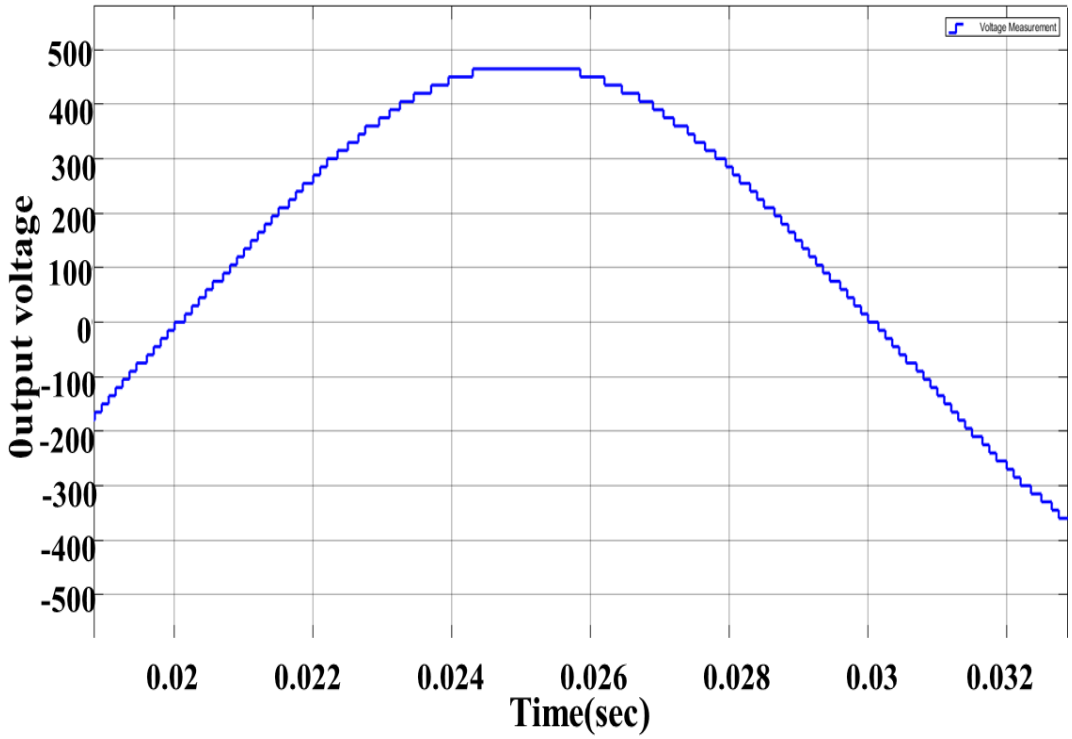


Fig. 5.9: Enlarged view of 63 levels generated in output voltage

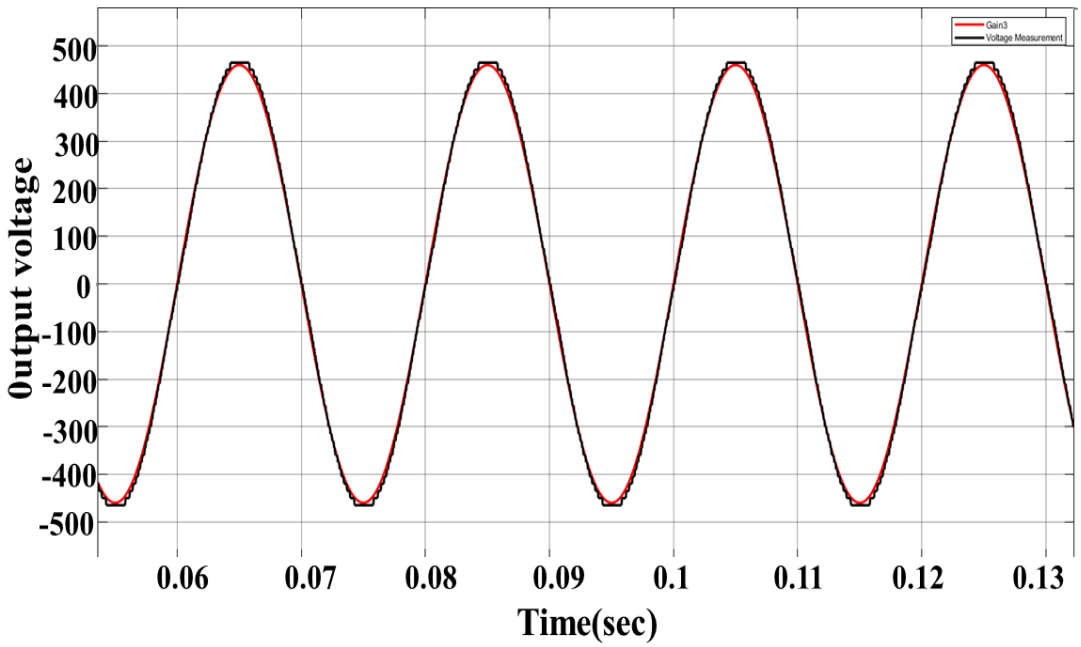


Fig. 5.10: Voltage waveform of 63 level reduced switch MLI with sine reference

5.3. Thirtyone(31) and Sixtythree(63)-level with passive filter

The output voltage waveform on applying the designed passive filters on 31 level and 63 level, which is, on applying the LC filter before the load, has been shown in Fig. 5.13 and 5.17 respectively for 31 level and 63 level. The voltage waveform for 31 and 63 level on applying LCL filter are shown in Fig. 5.21 and Fig. 5.25 respectively.

The THD procured on applying the filter, that is, on applying the LC filter design on 31 and 63 level, it has been found to be 2.04% and 1.02% as shown in Fig. 5.12 and 5.16 and on applying the LCL filter, it came out to be 2.05% and 1.07% as shown in Fig. 5.20 and 5.24 respectively.

The simulation circuit for 31-level and 63-level with LC filter is depicted in Fig. 5.11 and 5.15 respectively and simulation circuit including LCL filter is depicted in Fig. 5.19 and 5.23.

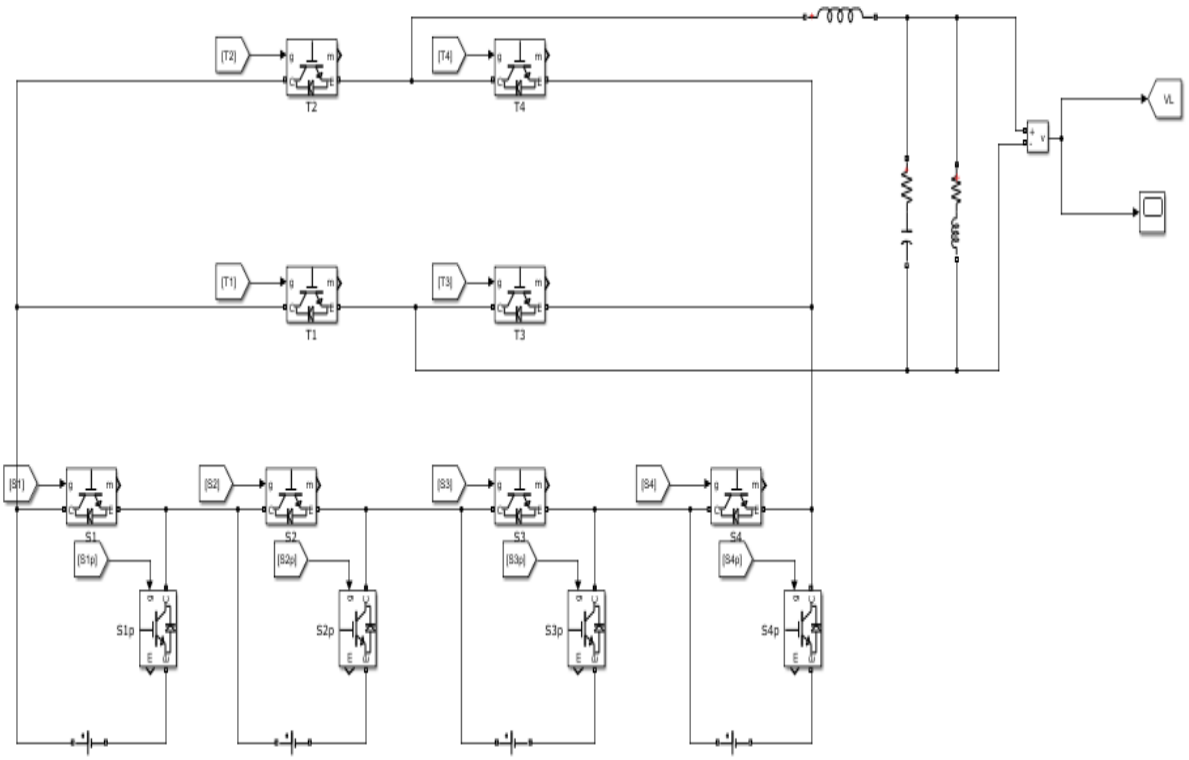


Fig. 5.11: Simulation Circuit of 31-level with LC filter

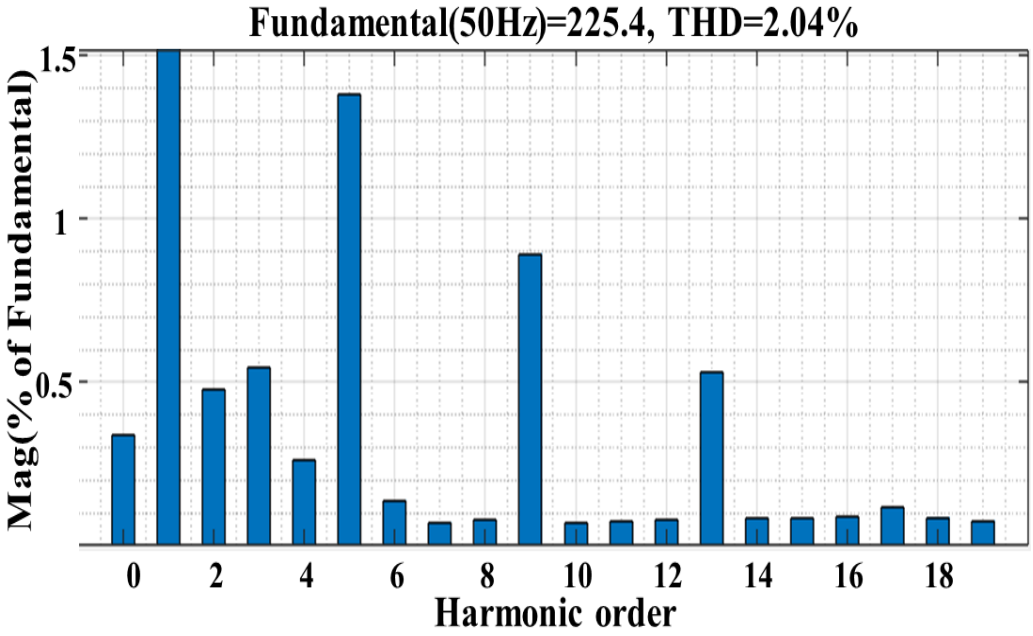


Fig. 5.12: THD of 31 level Reduced Switch MLI with LC filter

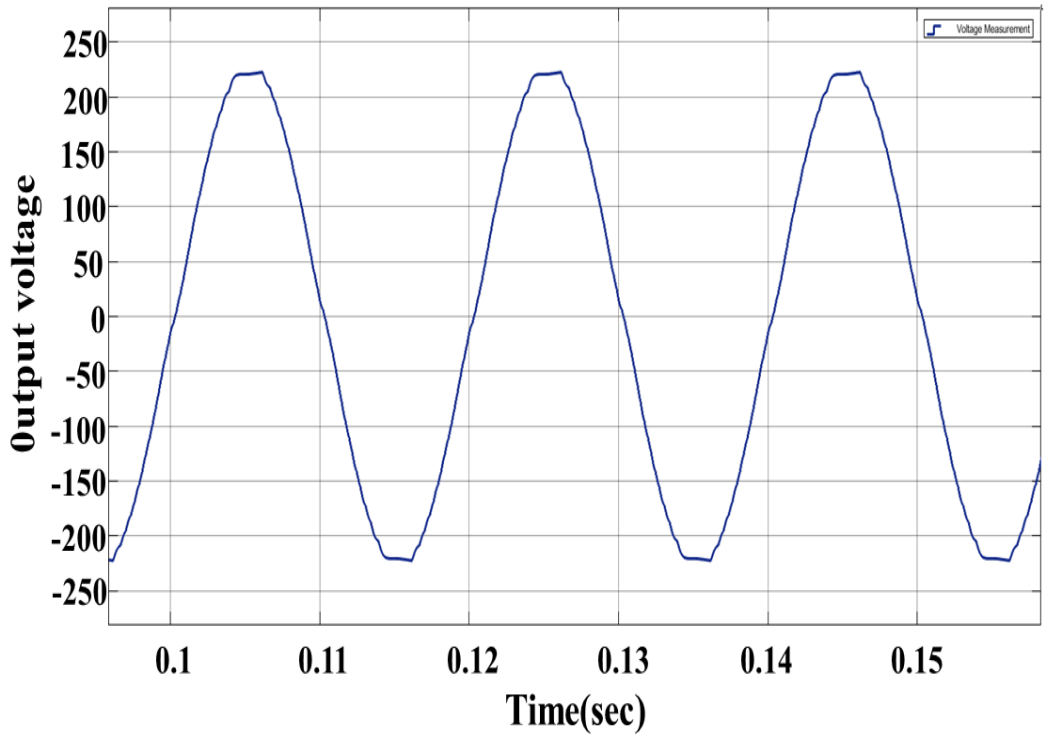


Fig. 5.13: Voltage waveform of 31 level Reduced Switch MLI with LC filter

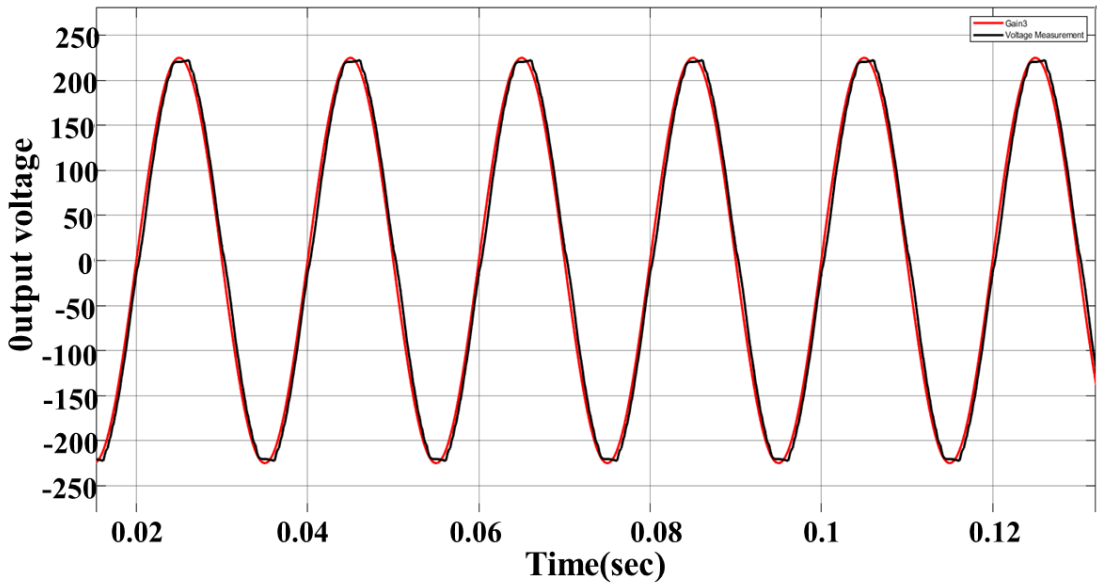


Fig. 5.14: Voltage waveform of 31 level Reduced Switch MLI with LC filter with sine reference

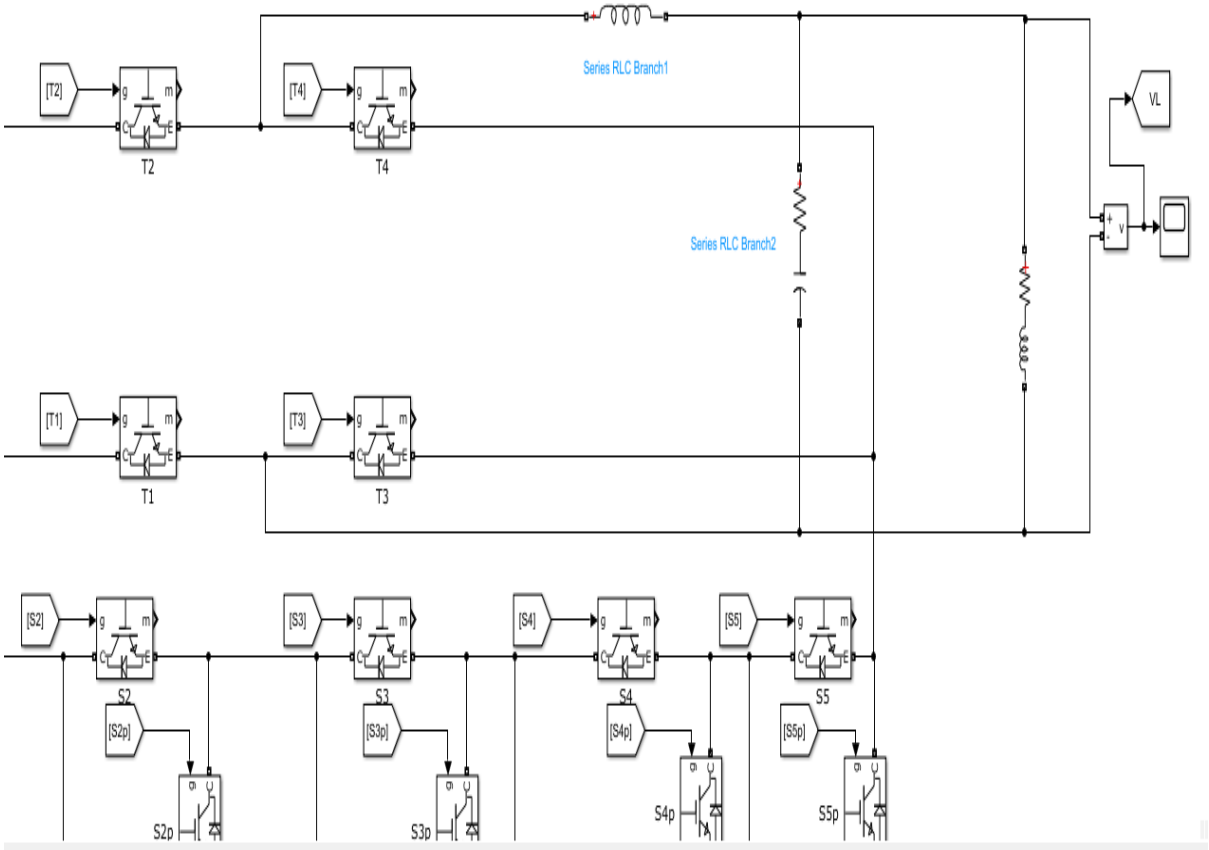


Fig. 5.15: Simulation Circuit of 63-level with LC filter

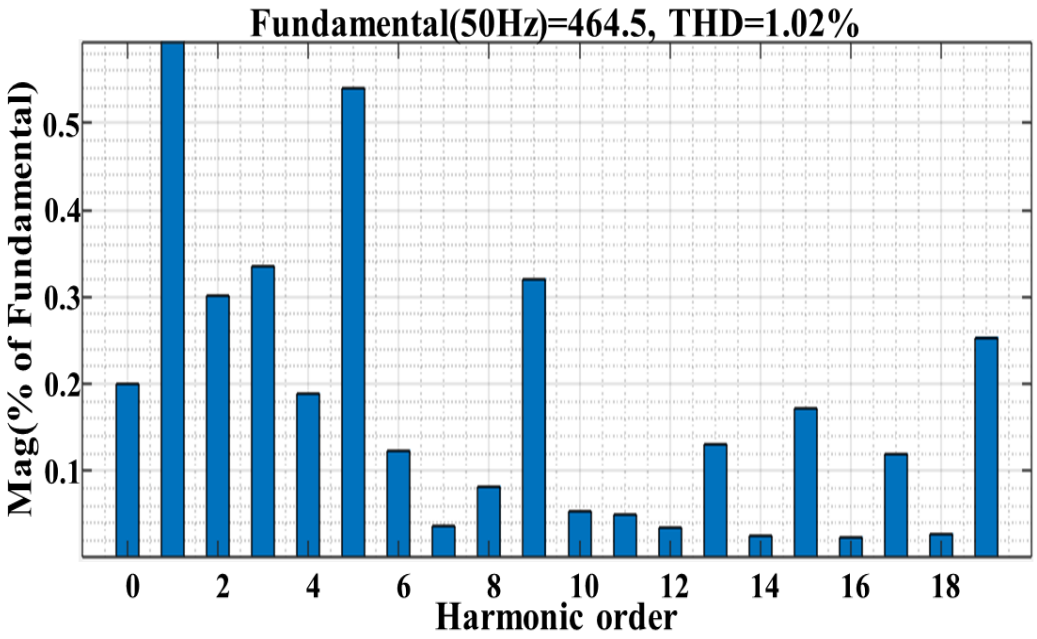


Fig. 5.16: THD of 63 level Reduced Switch MLI with LC filter

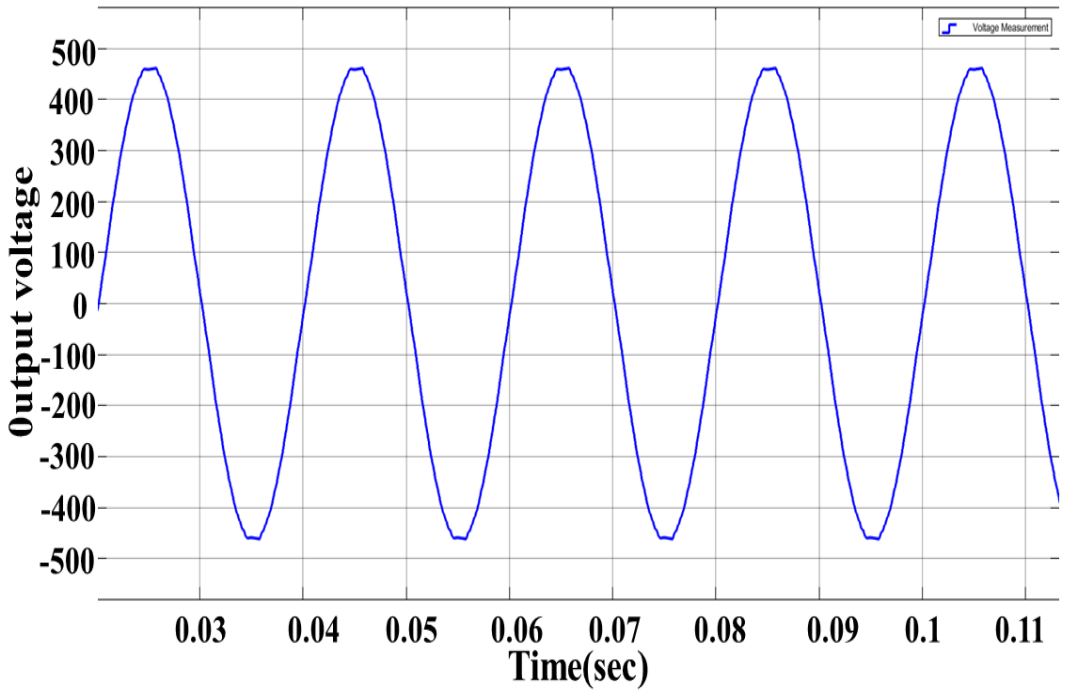


Fig. 5.17: Voltage waveform of 63 level reduced switch MLI with LC filter

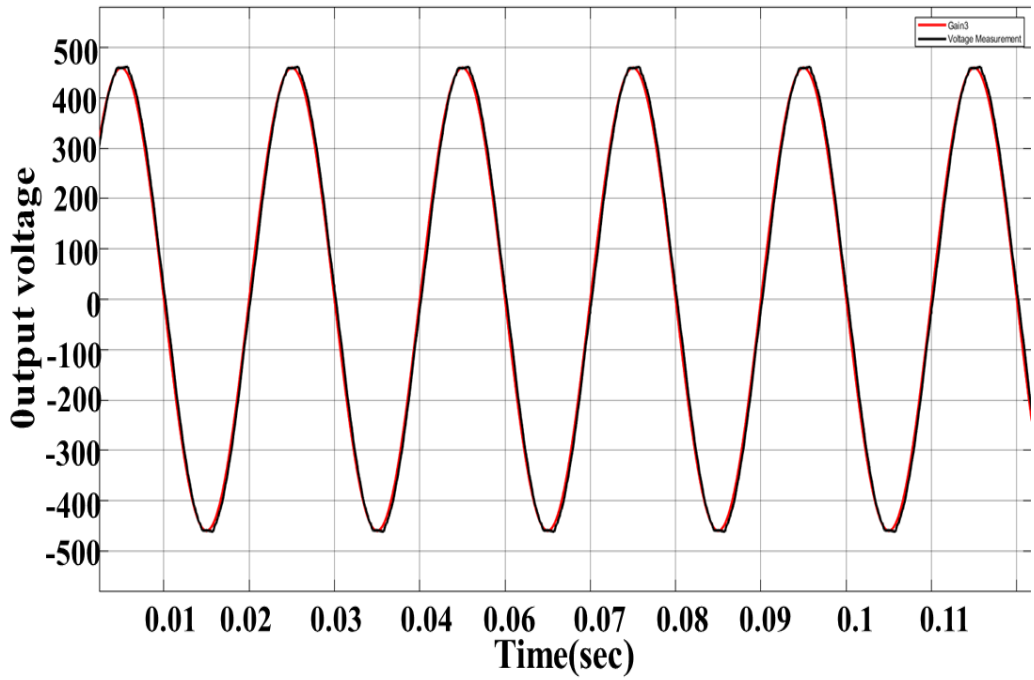


Fig. 5.18: Voltage waveform of 63 level reduced switch MLI with LC filter with sine reference

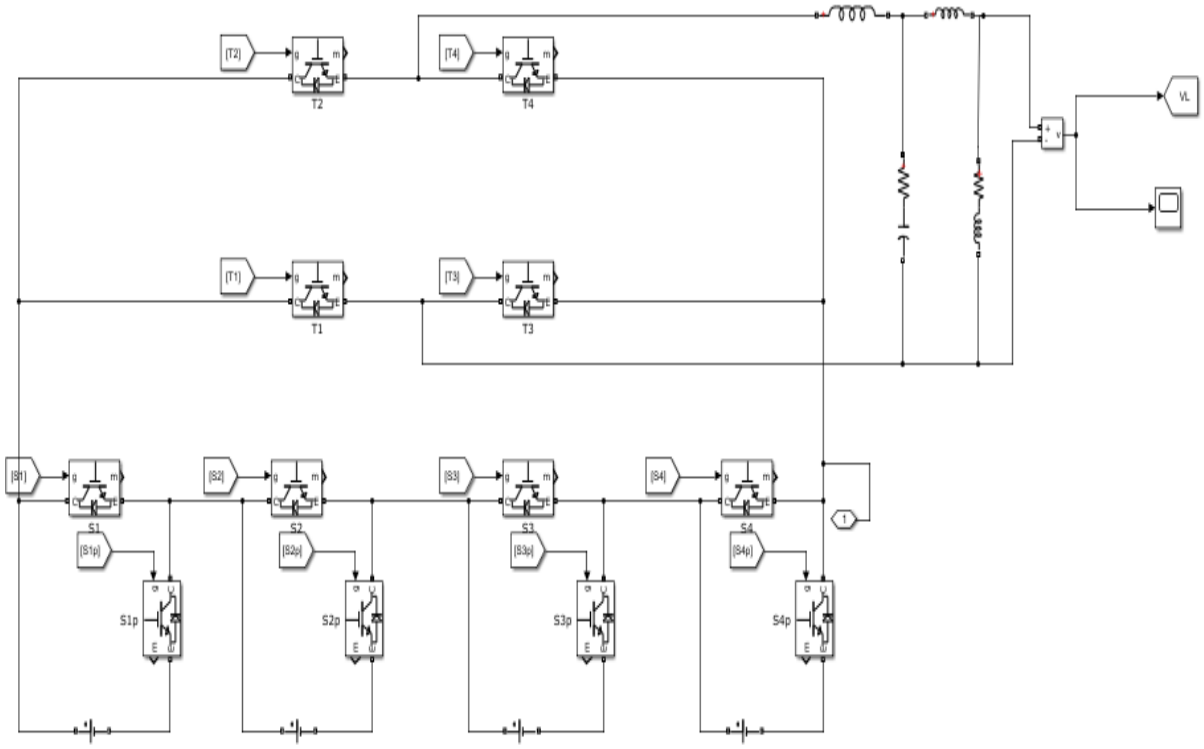


Fig. 5.19: Simulation Circuit of 31-level with LCL filter

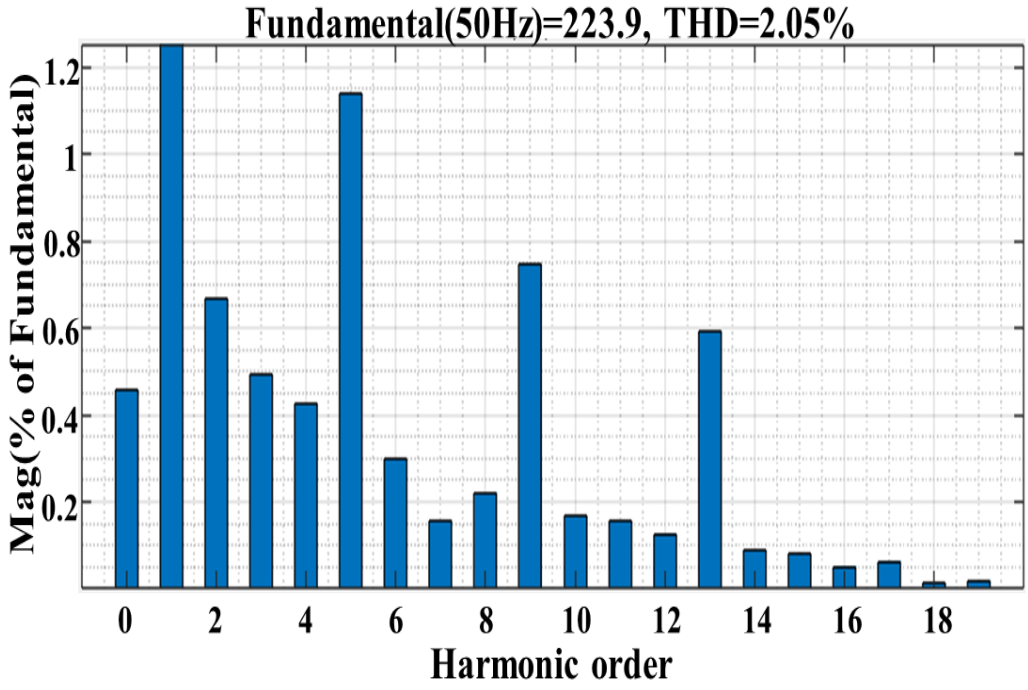


Fig. 5.20: THD of 31 level reduced switch MLI with LCL filter

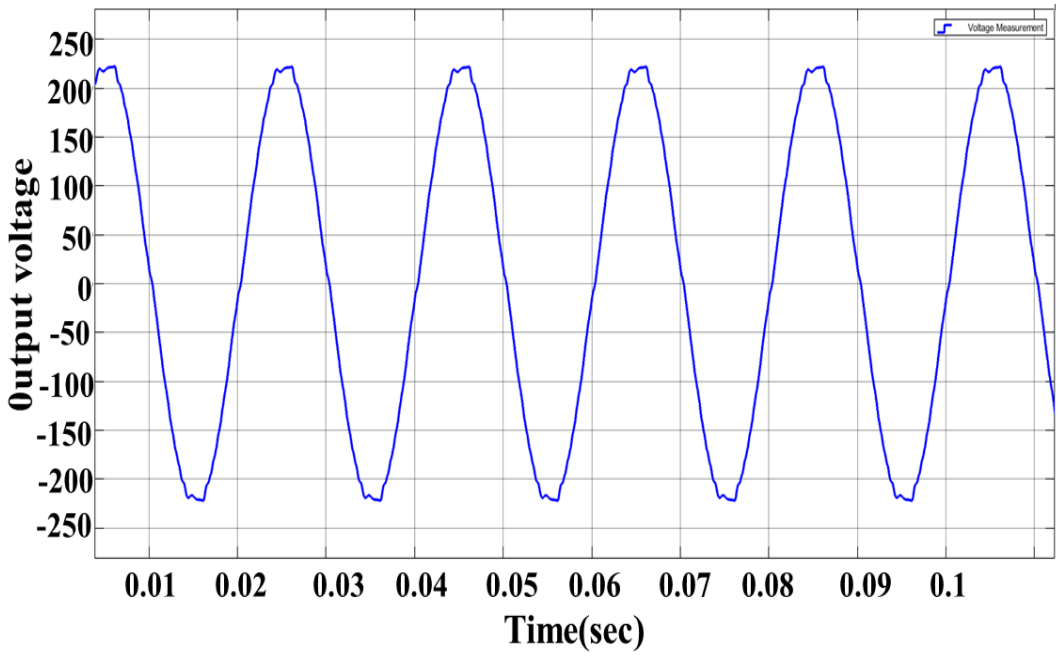


Fig. 5.21: Voltage waveform of 31 level reduced switch MLI with LCL filter

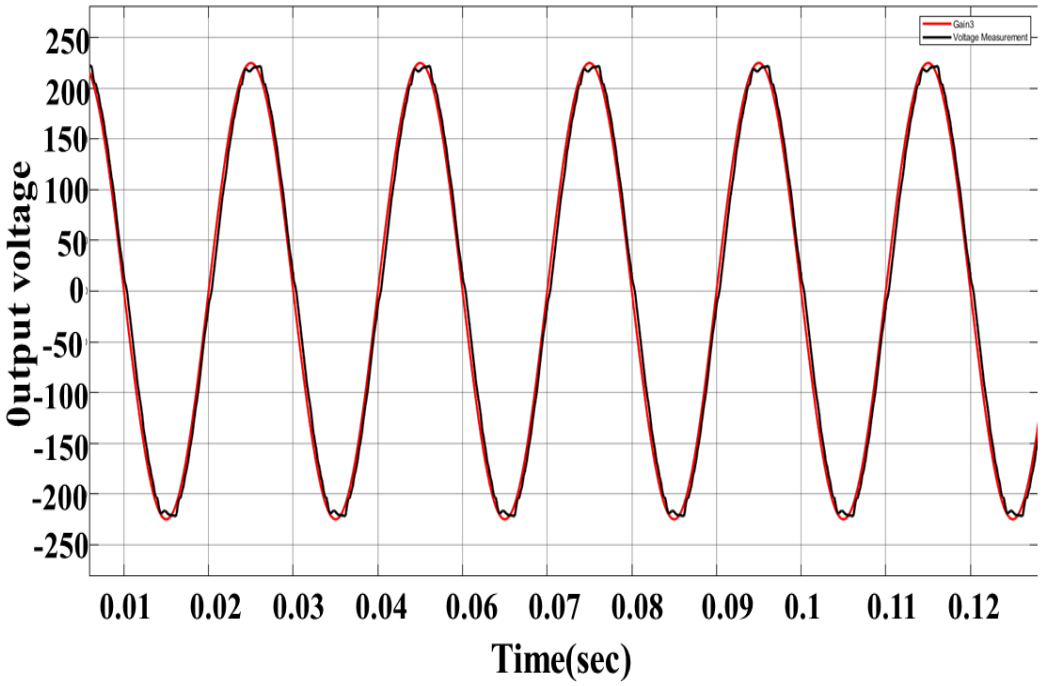


Fig. 5.22: Voltage waveform of 31 level reduced switch MLI with LCL filter with sine reference

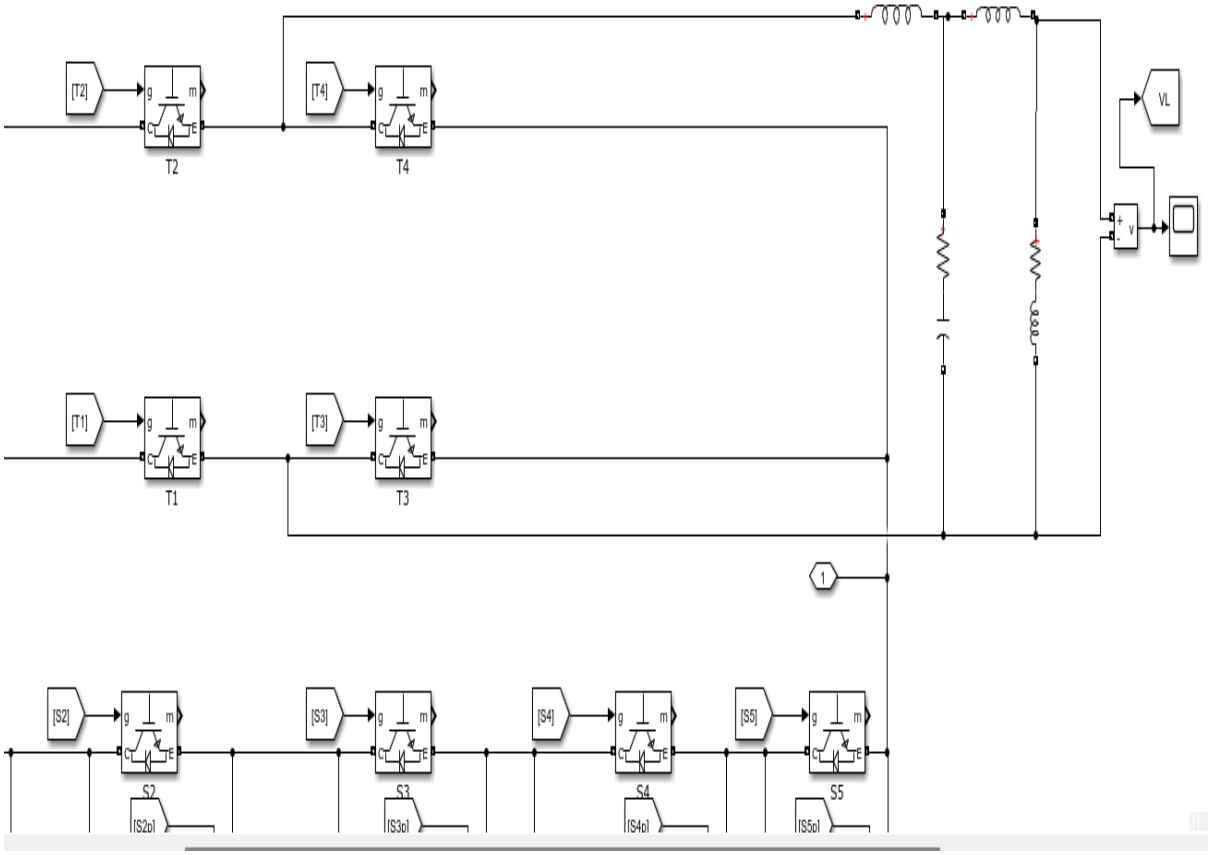


Fig. 5.23: Simulation Circuit of 63-level with LCL filter

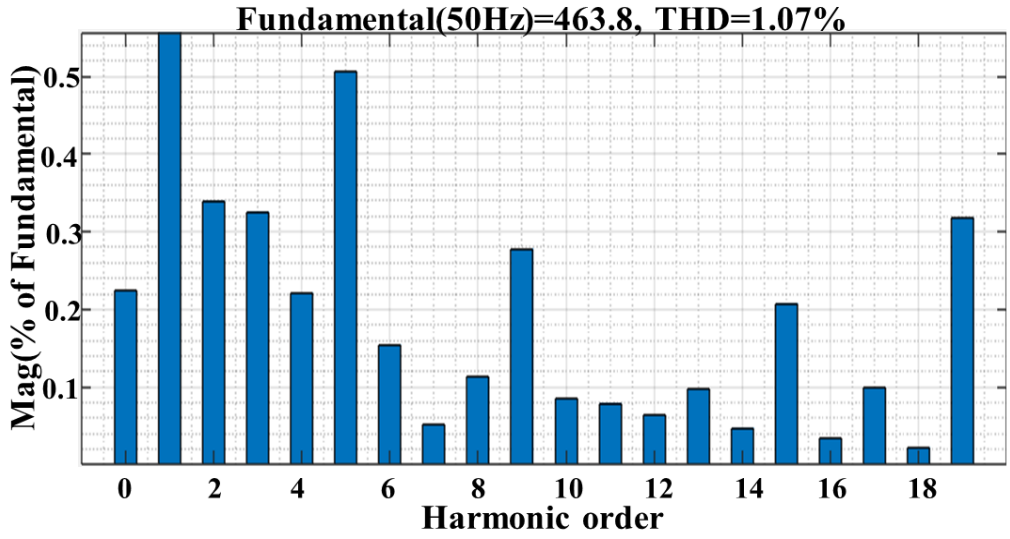


Fig. 5.24: THD of 63 level reduced switch MLI with LCL filter

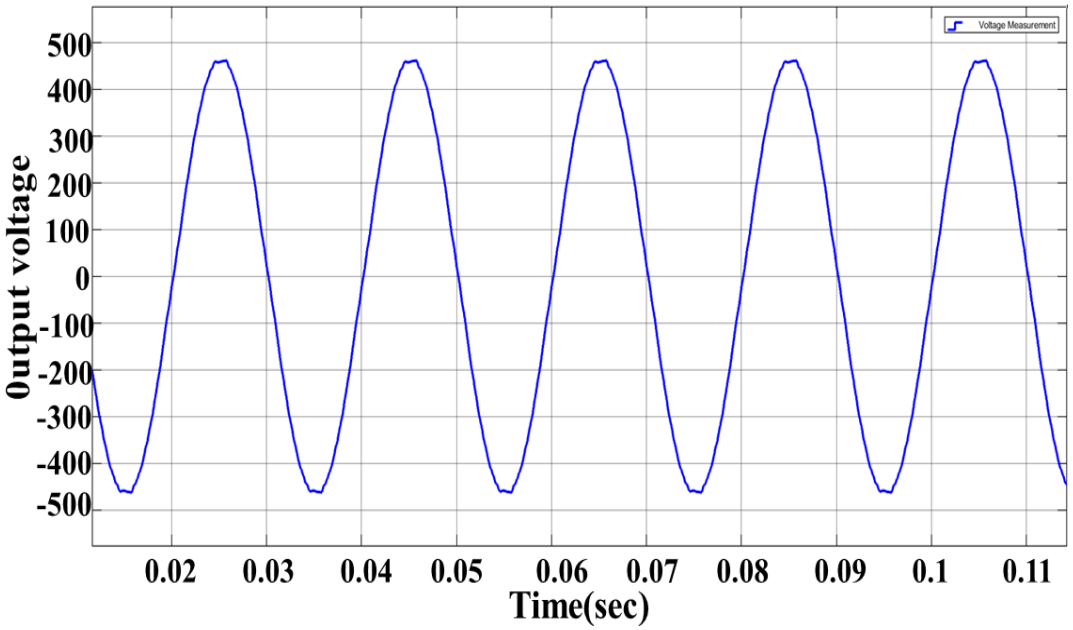


Fig. 5.25: Voltage waveform of 63 level reduced switch MLI with LCL filter

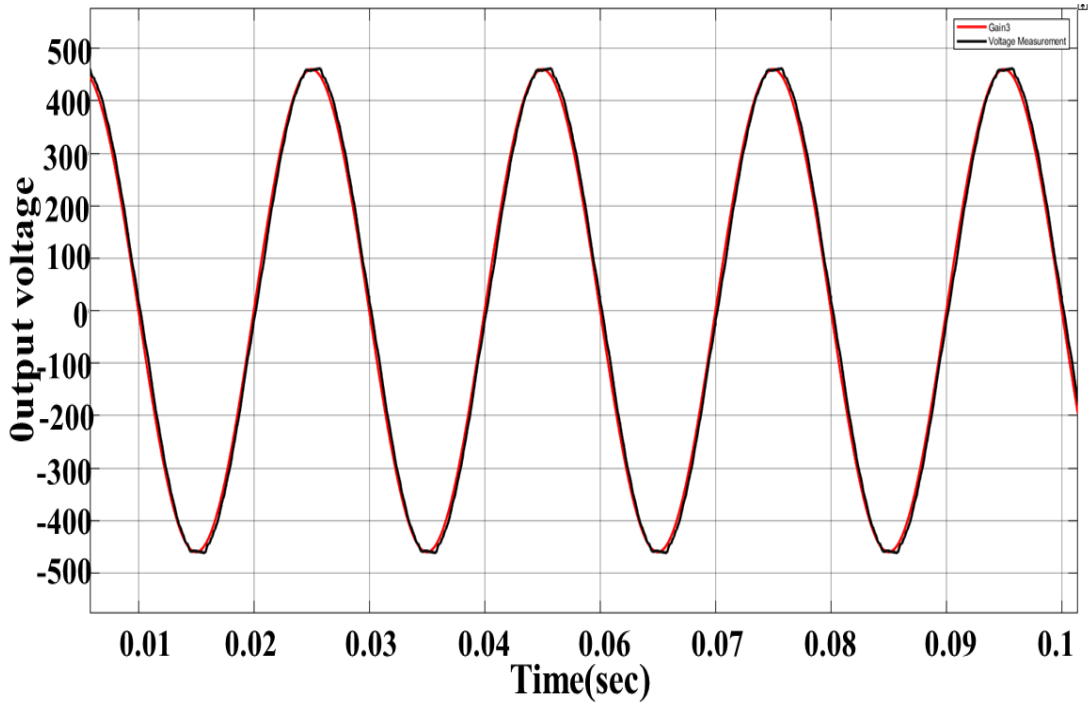


Fig. 5.26: Voltage waveform of 31 level reduced switch MLI with LCL filter with sine reference

5.4 Discussion

Table5.1: Comparative analysis of THD's of reduced switch MLI with passive filter

REDUCED SWITCH MLI	THD WITHOUT FILTER	THD WITH LC FILTER	THD WITH LCL FILTER
31 level MLI	3.2%	2.04%	2.05%
63 LEVEL MLI	1.58%	1.02%	1.07%

5.5 Conclusion

On simulating 31-level reduced switch MLI model, it yielded THD of 3.2% without taking filter in consideration, whereas on applying the designed LC filter, the THD reduced to 2.04% and on applying the designed LCL filter, it is recorded as 2.05% which is nearly equal and under IEEE 519 standard. In case of 63-level reduced switch MLI, the THD recorded without applying the designed passive filter is 1.58%, whereas on applying LC filter it reduced to 1.02% and on applying LCL filter it came out to be 1.07% which is also nearly equal and also under IEEE 519 standard.

CHAPTER – 6

CONCLUSION AND FUURE SCOPE

6.1. Summary of Contribution

In this work 31-level and 63-level reduced switch MLI has been proposed which aims on reducing the power electronic switches and components and reduction of total harmonic distortion which makes it more efficient[7].Conventional topologies of multilevel inverter requires numerous power electronic components[5]-[6].

Taking this in consideration, we have designed reduced switch MLI. The design resulted in the reduction of switches as well as DC voltage sources The 31-level and 63-level topologies consists of 4 polarity generating switches and 8 level generation switches, which makes a total of 12 switches for 31-level and 14 switches for 63-level as it involves 10 switches as polarity generators. In the process of achieving the desired higher level topology, we have also developed lower level reduced switch MLI, which is, 5-level and 7-level.

On simulating 31-level reduced switch MLI model, it yielded THD of 3.2% without taking filter in consideration, whereas on applying the designed LC filter, the THD reduced to 2.04% and on applying the designed LCL filter, it is recorded as 2.05% which is nearly equal and under IEEE 519 standard.

In case of 63-level reduced switch MLI, the THD recorded without applying the designed passive filter is 1.58%, whereas on applying LC filter it reduced to 1.02% and on applying LCL filter it came out to be 1.07% which is also nearly equal and also under IEEE 519 standard, which was earlier 20.26% and 13.70%, respectively for 5-level and 7-level. Furthermore, the THD that has been recorded when the LC filter and damping resistance are applied is 14.23% and 7.55%, respectively, which is almost half of the 7-level.

6.2. Future Scope

The future potential of Reduced Switch Multi-Level Inverters (MLI) is highly attractive, and demanding particularly in the sector of evolving energy systems all across the globe. As these inverters utilize lesser or reduced numbers of switching devices such as IGBT and MOSFET and power sources, they providing advantages like cost savings, smaller physical dimensions,

minimal heat loss, and higher efficiency when compared with conventional topologies of MLIs. Within the application domain of electric vehicles (EVs), reduced switch MLIs enhance battery performance and reduce the overall weight of the vehicle, thereby enabling a suitable choice for motors and chargers and therefore leading to a more efficient system economically. They find extensive application in solar and renewable energy systems for the efficient coupling of energy sources with the electricity grid economically as in the sector of PV power conversion is essential. With the advancement of smart grids globally, the utility of these inverters increases owing to their small size and fewer fault possibilities.

Moreover, with respect to control application, intelligent switching methods which involves the utilisation of AI and IOT would be vital for tapping into the true capabilities of RSMLIs. Techniques like PWM tuning using artificial intelligence (AI), MPC, and SHE will make it possible to achieve optimal switching with simultaneous reduction in harmonics and switching losses. As far as applications are concerned, RSMLIs have the potential to revolutionise renewable energy technologies such as solar energy and wind energy conversion, energy storage in batteries, EV drives, and microgrids, among others. Reliability, fault tolerance would be the future foundations of RSML inverter research and development. The new inverter structures will provide self-repairing switching circuits, artificial intelligence for fault detection, and prognostics and health management for continuous operation in critical applications, hence it would make the system more reliable and efficient.

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PUBLICATION

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