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Phase Current Balance Control of Fault-Tolerant Three-Phase Interleaved Buck Converter under Non-Ideal Circuit Conditions

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Phase Current Balance Control of Fault-Tolerant Three-Phase Interleaved Buck Converter under Non-Ideal Circuit Conditions

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY
IN
POWER ELECTRONICS & SYSTEMS

Submitted by:

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M. Tech (Power Electronics and Systems) Saurabh Gupta 2026

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CANDIDATE'S DECLARATION

I, **SAURABH GUPTA**, Roll No. 2K24/PES/25 student of M. Tech (Power Electronics & Systems), hereby declare that the project Dissertation titled **"Phase Current Balance Control of Fault-Tolerant Three-Phase Interleaved Buck (FTTPIB) Converter under Non-Ideal Circuit Conditions"** which is submitted by me to the Department of Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously submitted for the award of any Degree, Diploma.

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CERTIFICATE

I hereby certify that the project Dissertation titled **"Phase Current Balance Control of Fault-Tolerant Three-Phase Interleaved Buck (FTTPIB) Converter under Non-Ideal Circuit Conditions"** which is submitted by Saurabh Gupta, Roll No. 2K24/PES/25, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Date: 31/05/2026

DR. MAYANK KUMAR

(SUPERVISOR)

4

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2

Finally, I must express my very profound gratitude to my parents, seniors and to my friends for providing me with unfailing support and continuous encouragement throughout the research work.

Date: 31/05/2026

Saurabh Gupta

M. Tech (Power Electronics & Systems)

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ABSTRACT

This thesis introduces phase current balance control of fault-tolerant three-phase interleaved buck (FTTPIB) converter. The interleaving structure of the converter provides the fault-tolerant characteristics, which helps to improve reliability and makes it operational under fault conditions. The controller design ensures that the phase / inductor current in all three branches of the converter is balanced under circuit parasitic and open circuit switch fault conditions. Using interleaving structure of the FTTPIB converter i.e., equal phase shifting of the gate pulse, the converter reduces the output current ripple, which helps to provide better power quality under high current low voltage load applications such as electrolyzers. The structure also reduces stress on individual semiconductor devices. The phase current balance enables the equal current stress across each phase. The simulation results are captured using MATLAB/Simulink software to show the current balance characteristics of the converter under circuit parasitic and open circuit switch fault conditions.

TABLE OF CONTENT

turnitin Page 11 of 85 - Integrity Submission Submission ID trn:oid:::27535:142302638

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

FTTPIB	Fault-Tolerant Three-Phase Interleaved Buck
TPIBC	Three-Phase Interleaved Buck Converter
IBC	Interleaved Buck Converter
SCIBC	Series-Capacitor Interleaved Buck Converter
DC–DC	Direct Current to Direct Current
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
PWM	Pulse-Width Modulation
ACS	Average Current Sharing
HCC	Hysteresis Current Control
SMC	Sliding Mode Control
MPC	Model Predictive Control
ESR	Equivalent Series Resistance
R_L	Inductor Parasitic Resistance
i_{L1}, i_{L2}, i_{L3}	Inductor Currents of Phase 1, 2, 3
EV	Electric Vehicle
VRM	Voltage Regulator Module
RES	Renewable Energy System

LIST OF SYMBOLS

Symbol	Description
S_1, S_2, S_3	High-/low-side semiconductor switches of the 3-phase converter
D_1, D_2, D_3	Freewheeling diodes of each phase
L_1, L_2, L_3	Phase inductors
R_{L1}, R_{L2}, R_{L3}	Series parasitic resistance of each phase inductor
C	Output capacitor
ro	ESR (equivalent series resistance) of capacitor
i_{L1}, i_{L2}, i_{L3}	Per-phase inductor currents
i_L	Generic instantaneous inductor current
I_L	Total output/load current
$iavg$	Average of three phase currents
i_{L11}, i_{L21}, i_{L31}	ACS residual current errors: iavg − phase current
i_{in}	Input current
i_{out1}, i_{out2}, i_{out3}	Per-phase output currents used in control diagram
V_{in}	Input DC source voltage
V_{out}	Output voltage
V_{ref}	Reference output voltage
D	Duty cycle (base duty)
d_1, d_2, d_3, d_4	Duty components associated with operating modes
ΔD_k	Duty-cycle correction for the k-th phase in ACS balancing
D_{base}	Base duty command before ACS correction
G_1, G_2, G_3	PWM gate pulses for 3 phases
T	Switching period
t_1 … t_6	Switching instants defining converter operating modes
d_1T, d_2T, d_3T	Numerical on-times shown in waveform plots
K_p, K_i	PI controller gains
f_s / f_{switch}	Switching frequency

CHAPTER 1
INTRODUCTION

1.1. DC-DC Converters:

Power electronics is a rapidly growing field of electrical engineering that deals with the conversion, control, and conditioning of electric power using semiconductor devices such as MOSFETs, IGBTs, and diodes [1]. Due to the growing need for efficient energy consumption, DC-DC converters have become important elements in modern electronic and electrical systems [2]. These converters are used for converting one level of DC voltage to other with high efficiency and reliable performance. They are of great importance in applications such as renewable energy system, electric vehicles (EVs), battery energy storage systems, telecommunication and industrial automation [3–5].

For the purpose to improve power density and overall system reliability and to reduce switching and conduction losses, high efficiency DC-DC converters are needed. Converters are frequently used in the integration of renewable energy in solar photovoltaic and wind energy systems for voltage regulation and maximum power transfer [6].. Efficient power conversion is also required for EV charging infrastructure to achieve fast charging and protect the battery [7]. Hydrogen electrolyzer systems use conventional DC-DC converters to provide the controlled and stable DC power required for electrolysis to produce hydrogen [8]. Therefore, the development of advanced converter topologies with improved efficiency, fault tolerance and current balancing capability has become an important research area in modern power electronics. [9, 10].

1.2. Interleaved Converter Topologies:

Conventional DC–DC converter topologies such as buck, boost, and buck–boost converters are widely used in power electronic applications for voltage regulation and power conversion [11]. However, as power and current requirements increase, conventional converters face several limitations, including high current ripple, increased switching stress, large filter size, poor thermal management, and reduced efficiency. To overcome these drawbacks, interleaved converter topologies are introduced in modern power electronic systems [13, 14].

An interleaved converter consists of multiple converter phases connected in parallel and operated with a phase shift between switching signals. The phase-shifted operation distributes the input and output current to different phases, which reduces the stress on the individual switches and passive components [15]. Interleaving is mainly required in high power applications such as electric vehicles, renewable energy systems, battery charging systems and aerospace power supplies where efficiency and reliability are of extreme significance [16, 17].

The conventional buck converter is a DC-DC power electronic converter that successfully steps down the input DC voltage to a lower output voltage. It usually contains a power switch, diode, inductor and capacitor [18]. The conventional buck converter is simple and widely used, but it has limitations for high power applications due to large current ripple, increased thermal stress and reduced efficiency [19]. The interleaved buck converter topology has been proposed [20] to overcome these drawbacks.

An interleaved buck converter is made up of multiple parallel connected buck converter phases, which are operated with phase shifted switching signals. The need for interleaving is due to the increasing demand for high current and high-power density applications such as electric vehicles, renewable energy systems, and hydrogen electrolyzers [21]. The converter divides the load current over multiple phases [22], this reduces the stress on the components and improves overall performance.

A key advantage of interleaving is ripple reduction. Due to the phase cancellation of the inductor currents of different phases, the total output current ripple is much less than that of a conventional single-phase converter. This reduces the requirement of bulky filters and enhances the quality of the output voltage [23]. Another important advantage is the better thermal distribution, where the heat generation is distributed over several semiconductor devices, resulting in better temperature management and improved converter lifetime [24]. Therefore, interleaved converter topologies provide higher efficiency, better dynamic response, reduced electromagnetic interference, and improved reliability for modern high-performance power electronic applications [25].

1.3 Three-Phase Interleaved Buck Converter (TPIBC):

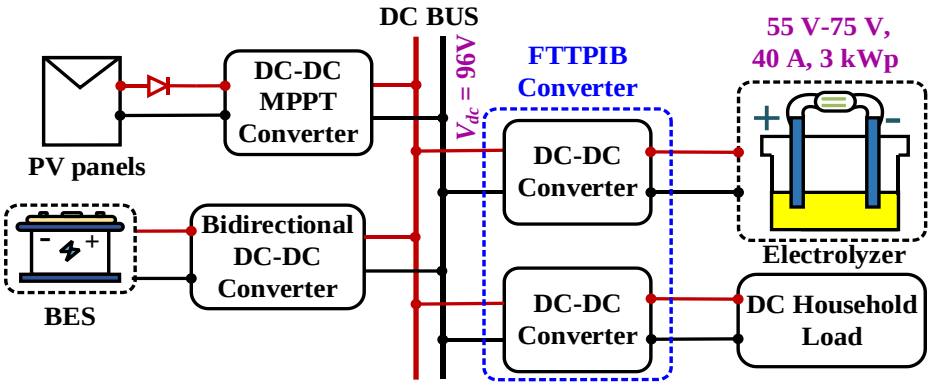

Figure 1.1. FTTPIB converter in a renewable energy-based system.

For high-power and high-current applications, the TPIBC is a sophisticated DC-DC converter topology. It is made up of three identical buck converter phases that are connected in parallel. Each phase has an inductor, a capacitor, a power switch, and a diode or synchronous switch. The converter may distribute power among several pathways because all three phases share a common input and output [26]. When compared to a traditional single-phase buck converter, this topology increases reliability, minimizes component stress, and improves efficiency [27].

The proposed TPIBC is designed for hydrogen electrolyzer and DC household load applications powered through a photovoltaic (PV) system and battery energy storage (BES). The converter operates from a DC bus voltage of 96 V and provides a regulated output voltage in the range of 55 V to 75 V with a rated output power of 3 kW and output current of 40 A [28]. The interleaved converter consists of three parallel buck converter phases operating with a phase shift of 120° to achieve ripple reduction and equal current sharing [29].

For the designed TPIBC, the nominal operating parameters are considered as follows: input voltage $V_{in} = 96\ \text{V}$, output voltage $V_{out} = 75\ \text{V}$, output current $I_{out} = 40\ \text{A}$, switching frequency $f_s = 25\ \text{kHz}$, and load power $P_{out} = 3\ \text{kW}$. Under healthy operating conditions, the load current is equally shared among the three phases. Therefore, each phase carries approximately $13.3\ \text{A}$. The output voltage remains stable around $75\ \text{V}$ with reduced ripple due to interleaving operation. The output power obtained is approximately $3000\ \text{W}$ with converter efficiency around 94–96%.

During the pre-fault condition, small parasitic resistances create a slight current imbalance among the phases. The phase currents may vary as $14\ \text{A}$, $13\ \text{A}$, and $13\ \text{A}$

, while the output voltage slightly drops to nearly $73\,V$. The ripple content also increases because of unequal current sharing.

After an open-switch fault in one converter phase, the fault-tolerant operation redistributes current among the remaining healthy phases using the Average Current Sharing (ACS) control technique [30]. In this condition, the healthy phases carry approximately $20\,A$ each, while the faulty phase current becomes zero. The output voltage is maintained around $68-70\,V$, and the output power remains close to $2.7-2.9\,kW$. Thus, the proposed TPIBC ensures continuous operation, improved reliability, and stable power delivery even under fault conditions [31].

The working principle of the TPIBC is based on an interleaving operation, where each converter phase operates with the same switching frequency but with a phase shift between the gate pulses. The switching signals in a three-phase system are 120° apart. The output current ripple decreases significantly, and the output voltage is smoother as a result of this phase-shifting principle, which causes the inductor current ripples of various phases to partially cancel one other Moreover, the power density and performance levels can be increased by employing filters that are smaller in size. Another important criterion that determines the performance of TPIBCs is the sharing of current across three phases. Current supplied is equally distributed among all three converters, and this implies reduced thermal stress on the converter's components as well as increased efficiency of the converter. For applications, where high power is required, such as in electrolyzer for hydrogen, EV chargers and renewables, the proper distribution of currents increases the life span of the converter and enhances its reliability. Among the key strengths associated with the use of interleaving in the construction of converters include reduction in output ripple currents. Compared to the single phase converters, output ripple currents are significantly reduced in the case of interleaving due to the cancellation of the inductor currents of different phases. Another key strength of using interleaving includes thermal balance that arises as a result of generation of heat by several semiconductor devices. This allows for efficient cooling of the system due to effective heat dissipation. In recent years, interleaving converters have proved to be efficient, reliable, and dynamic.

1.4 Fault-Tolerant Converter Topologies:

When reliable and continuous functioning is needed in today's power electronic systems, fault-tolerant converters are essential. Converter failure can result in

significant performance degradation, system shutdown, and economic loss in high-power applications including hydrogen electrolyzers, renewable energy systems, electric cars, aerospace systems, and data centers. As a result, increasing DC-DC converter reliability has emerged as a key topic of power electronics research [32].

Switching device issues are one of the main problems with power converter reliability. When a semiconductor device fails in the open state, it disrupts the current flow, resulting in phase current imbalance, output voltage oscillations, and an open-switch fault [33]. A short-circuit defect, on the other hand, is more dangerous since it causes an excessive amount of current to flow through the converter, which could overheat and harm semiconductor devices and passive components. If these problems are not sorted out, then converter efficiency will be reduced and might even result in the complete failure of the entire system.

Some of the factors which contribute towards parasitic effects that affect the converter are switching transients, stray inductances, and parasitic capacitances. The voltage spike, electromagnetic interference, and switching losses can all be attributed to these unwanted parasitic effects. Converter fault tolerance is a technique wherein the converter continues to function normally even when faults arise due to the sharing of currents across the good phases of the converter.

1.5 Problem Statement:

1.5.1 Current imbalance due to parasitic resistance:

For multi-phase interleaved buck converters to achieve high efficiency, low ripple, and dependable operation, all phases must share current equally. But in real-world applications, parasitic resistances in semiconductor switches, inductors, PCB tracks, and connecting wires cause current imbalance [34]. Unequal current distribution among the converter phases results from small changes in component characteristics, which lowers system reliability and degrades performance [35].

1.5.2 Uneven Current stress on semiconductor devices:

In certain semiconductor devices, uneven current sharing results in one converter phase carrying more current than the others, increasing conduction and switching losses. Switches and inductors experience thermal stress as a result of this high current, which may decrease component life and raise the risk of device failure. Furthermore, increased input and output current ripple results from the imbalance in

phase currents, which reduces the effectiveness of ripple elimination methods in interleaved convertersIncreased ripple imposes greater stress on filtering components and decreases output voltage quality.

In applications that require reliability and uninterrupted service, such as hydrogen electrolyzers, renewables interfacing, and electric vehicle chargers, the problem takes on greater significance. Consequently, for providing current balance between the three phases, minimizing ripple, and improving thermal management within the fault tolerant three-phase interleaved buck converter system, an effective current balancing scheme must be implemented.

1.6 Research Objectives:

The primary objective of the current study is the design and implementation of a Fault-Tolerant TPIBC and its optimal current balancing control system for high power DC applications. Idea is to divide a circuit in which the three phases of the converter can balance themselves despite any imbalance in their resistances or ESR ratings. Idea is to design a fault tolerant TPIBC in which a balance between the three phases is achieved with maximum efficiency despite any imperfections present within the circuit. To achieve the desired objectives, the first step would be the mathematical modelling of the converter.

Three-loop controller system employed in the project has been designed as per this model, wherein there is an outer loop based on voltage control, inner loops for controlling the current in each phase, and finally the Average Current Sharing (ACS) loop [36]. The average current controller continuously calculates the average current and makes fine adjustments in the duty cycle to ensure balanced phase current, thus minimizing the difference caused due to any mismatch in the components. This particular design of the controller employs hierarchical bandwidths wherein the current control is faster, followed by ACS, while the voltage loop control is slower. Moreover, the proposed method will also consider analysing the operation of the converter system in case of an open-switch fault condition. Such fault tolerance analysis is conducted to determine whether the converter system can continue its operation in the event of having a defective switching element. Besides, other issues that should be considered are the reduction of the output current ripple and improving the thermal performance and reliability of semiconductor elements.

Simulations are conducted to validate efficiency of the mentioned methodologies. These simulations will involve the study of fault tolerance, steady-state behavior, and the minimization of output current ripple. The end goal of this project is to demonstrate that the proposed ACS fault tolerant system has greatly enhanced the operation of the converter system.

Generally speaking, this work is aimed at developing an effective fault-tolerant converter system that can be applied in applications such as renewable energy systems, EV charging stations, and hydrogen electrolyzer systems.

1.7 Scope of thesis:

As it was mentioned previously, this thesis deals with the study of analysis and control of the Three-Phase Interleaved Buck Converter. In particular, the analysis will be carried out for the healthy system as well as the failed system in its work process. The main attention will be paid to the creation of the converter topology and using different control techniques with Matlab/Simulink.

As one of the methods, current mode control will be used to achieve high performance and better dynamic characteristics. Moreover, the Proportional-Integral (PI) Average Current Sharing (ACS) method will be implemented in this study. According to the literature sources, the ACS controller can decrease the negative impact of the parasitic resistance influence on uneven current sharing between the three converter phases [37].

The following important aspect of this study is the examination of the fault tolerant properties of the converter concerning open switch faults. Comparisons of the healthy system and the faulty one will be performed to examine their reliability, stability, and performance parameters. This research will help to optimize the converter parameters to provide higher efficiency and reliability.

1.8 Contribution of thesis:

In the present thesis, fault-tolerant topology of TPIBC and an effective method of current balancing within the converter stages are considered. One of the most distinctive features of this work that contributes to its novelty is an analysis of current balancing under less-than-ideal conditions that take into account such factors as parasitic resistances and components' asymmetry. A considerable attention has been

paid to the effects of parasitic causing current imbalance and their performance impacts.

Another contribution to existing knowledge that has been brought about by the present thesis is the implementation of Average Current Sharing control strategy based on PI-controller. Proposed current-sharing scheme allows keeping currents balanced within all three stages of the converter, which reduces circulation currents, decreases thermal stresses and improves efficiency of the converter [38]. The methods of reducing ripples have been implemented in this thesis, which provides low output current ripples thanks to phase shifting operations.

Additionally, this study will examine the TPIBC's capacity to manage open switch faults. Through dynamic current distribution and other working phases, the converter can continue to operate even after the fault. In such a scenario, this improves the power electronic converter's reliability. In summary, the thesis improves the design of a reliable, effective, and fault-tolerant power electronics converter for use in hydrogen electrolyzers, EV chargers, and renewable energy applications.

1.9 Organization of Thesis:

The research or thesis on the fault-tolerant Three-Phase Interleaved Buck Converter (TPIBC) with current balancing control is methodically presented in this thesis, which is divided into multiple chapters.

Chapter 1 Introduction: DC-DC Converters, Interleaved Converter Topologies, Three-Phase Interleaved Buck Converter (TPIBC), Fault-Tolerant Converter Topologies, Problem Statement , Current unbalance due to parasitic resistance, Uneven Current stress on semiconductor device , Research Objectives , Scope of thesis, Contribution of thesis, Organization of Thesis

Chapter 2 Literature Review: Introduction: DC-DC Converter Multiphase Interleaved Converter: Current Sharing Techniques in Interleaved Converters Fault-Tolerant Converter Techniques Application of TPIBC Converter: Research Gap Identification: Summary of Literature Review:

Chapter 3 TPIBC under healthy and faulty conditions, introduction of TPIBC, circuit diagram of TPIBC, operation of TPIBC, TPIBC under healthy condition, pulse width modulation (PWM), technique of TPIBC under healthy condition, TPIBC under faulty

condition, pulse width modulation (PWM) technique of TPIBC under faulty condition, modes of operation of TPIBC, mode 1, mode 2, mode 3, mode 4, mathematical equations and switching states of TPIBC

Chapter 4 modelling of TPIBC with circuit parasitic, mathematical modelling, state-space averaging, control design (small-signal model), state space model, control to output transfer functions, line to output transfer function, inductor current transfer functions, current ripple analysis, effect of parasitic resistance, output voltage ripple analysis, advantages and limitations of TPIBC

Chapter 5 controller design for the proposed TPIBC, introduction, need for current balancing, control strategies, average current sharing (ACS) technique, outer voltage loop, inner current loop, ACS balancing loop:, duty analysis of using ACS balancing, control design and comparative analysis of TPIBC

Chapter 6 Results and Discussion, System parameters, operation under normal condition, operation under open-circuit switch faulty condition

Chapter 7 Conclusion and future scope, References, Publication

20

CHAPTER 2
LITRATURE REVIEW

2.1 Introduction:

In this literature review chapter, a detailed study and discussion of literature related to the following topics will take place – DC-DC converters, interleaved converters, current balancing strategies, and fault-tolerant control methods. In connection with the increasing demand for renewable energy systems, electric vehicles, energy storages, and hydrogen electrolysis devices, the significance of using effective and reliable DC-DC converters has become more and more pronounced. The research was aimed at creating new designs of such converters, which have high efficiency, low ripple factor, improved thermal characteristics, and fault-tolerance.

Among various kinds of converters, the widely known type of converters is a conventional buck converter that functions as a step-down converter due to its simplicity and easy control algorithm. Nevertheless, applying the buck converter in the case of high-power and currents results in specific drawbacks of this design, including high current ripple, high requirements to thermal performance, inefficient operation, and bulky filters. Consequently, the proposed solution to these issues is an interleaved buck converter. Various investigations were carried out to investigate the current balancing technique because of the presence of non-uniform currents owing to parasitic resistance and device mismatch in the interleaved buck converters. Current balancing control approaches including droop control, master-slave control, average current sharing (ACS) control, and current mode control have been widely investigated in existing literature. Of all the stated control techniques, ACS control technique is considered superior with respect to current balancing and dynamic response than others.

Furthermore, fault tolerance studies have become significant owing to the demand for reliable power conversion system. Literature is focused on fault detection, fault diagnosis, and fault tolerance in power conversion systems. This chapter includes the brief description of related literature that addresses researches performed in the fields of the interleaved buck converters and fault tolerance. The selected literature is the basis of the proposed research study on the fault tolerant TPIBC using current balancing control technique.

2.2 DC-DC Converter:

One of the most common DC-DC converters that are applied in converting high-level DC voltage into low-level DC voltage is the conventional buck converter. This converter employs the use of simple components, such as a power switch, diode, inductor, capacitor and load. The buck converter works based on high frequency operation of switching and a control of the output voltage via the duty cycle of the power switch. Efficiency, easy design, and simple construction make this converter suitable for various applications such as battery charger systems, renewable energy sources, telecommunication systems, computer power systems, and electric vehicles.

In instance where CCM is considered, the inductor current remains the same during the entire switching operation. This results in an improvement in efficiency and a reduction in ripple voltage. Using mathematics, the output voltage is directly proportional to the duty cycle and expressed by : $V_{out} = D.V_{in}$

Where D is the duty cycle of the switching signal. While the conventional buck converter is useful for low and medium power levels, there are certain limitations with regard to the high power level of such a circuit configuration. The limitations include the fact that high currents passing through a single switch and the inductor cause increased conduction loss. Another limitation includes input/output current ripple, which necessitates large filters. To mitigate the shortcomings, scientists have come up with various remedies like the use of synchronous buck converters and soft switches. But the single-phase converter still suffers from inefficiency and inadequate heat control due to increased load. Moreover, in practical situations, the switching losses and parasitic resistance affect the performance of the converters.

However, to overcome the limitations, interleaved buck converter configurations were proposed. In such converters, load current is shared among different phases, which improves efficiency and distributes heat properly. Hence, the basic buck converter can be used as the main component of more advanced configurations, which will be presented in further chapters of the dissertation.

2.3 Multiphase Interleaved Converter:

Interleaved multiphase converters have been used widely in many applications for high power DC to DC conversions due to higher efficiencies, less ripple, and thermal benefits. In this technique, different converter blocks operate in parallel through signals that are shifted in phase. Interleaving refers to dividing the total load current into various stages, leading to less burden on active components like semiconductors and passives. Multiphase converters result in higher efficiencies and greater reliability.

The greatest advantage that multiphase converters offer is ripple cancellation. As a result of shifting phases of signals for different converter stages, there is cancellation of input and output ripples, resulting in more stable output voltages without much use of filters. These converters have been employed in many areas such as renewable energy sources, electric cars, battery charging systems, and hydrogen electrolysis applications.

There are many problems associated with current sharing in multiphase converters owing to resistive effects in semiconductors and imbalance in converters. For this reason, many current sharing techniques have been proposed.

2.4 Current Sharing Techniques in Interleaved Converters:

Current equal distribution is one of the most important requirements in multiphase interleaved converters in order that the current can be equally distributed among all the phases of the converter. But due to the presence of parasitic resistance, component tolerance, delay in switching, and unbalanced inductors, it becomes very difficult for the current to be equally shared among all the phases of the converter, leading to heating and power loss as well as poor current regulation, resulting in poor performance of the power converter system. Various methods have been suggested for overcoming such issues.

Average Current Sharing method (ACS) is considered as one of the best approaches for achieving current sharing equally in an interleaved power converter. Here in ACS method, average value of the current flowing in all the phases of the converter is determined and then compared with the current flow in each phase to produce a compensating signal for equal current sharing. There are several benefits of using this current sharing method and also it is commonly used along with current mode control.

Another popular control technique used is the Master-Slave Control, wherein one of the converter phases will be considered as the master phase with reference while others will follow it. Though a very easy technique to implement, the malfunction of the master phase may influence the reliability of the whole system. The technique of Droop Control changes the reference output voltage based on the load current. It can easily be implemented with no communication link required, but it has an error in current sharing. Hysteresis Control can provide a fast response along with easy implementation through current regulation within a set band; however, it gives variable switching frequency. Predictive Control and Sliding Mode Control are some advanced techniques that ensure fast response time, robustness, and enhanced stability when parameters vary. Digital Control Techniques utilizing DSPs and microcontrollers have become popular due to their advantages including programmability, flexibility, fault detection, and control accuracy in today's fault-tolerant interleaved converters.

2.5 Fault-Tolerant Converter Techniques:

Fault-tolerant converters are designed to ensure that power electronic devices continue to operate reliably even in the presence of faults. In high-power systems such as renewable energy devices, electric vehicles, aerospace systems, and hydrogen electrolysis cells, converter faults can cause significant issues, including system outages and degraded performance. As a result, various fault-tolerance strategies have been proposed to enhance the performance and safety of these devices.

An effective approach in this regard is redundancy schemes in which additional converters or components are added to the device. This helps continue functioning despite failure of the main converter phase. However, this process increases system complexity and cost. Fault detection methods are used to identify abnormal operating conditions such as open-switch faults, short-circuit faults, overcurrent, and voltage imbalance. Researchers commonly use current sensors, voltage monitoring, observer-based methods, and signal processing techniques for fast and accurate fault detection.

After fault detection, fault isolation methods are applied to separate the faulty component from the healthy converter system. Isolation prevents fault propagation and protects semiconductor devices from further damage. Protective switches and control algorithms are generally used for this purpose.

Therefore, modern fault-tolerant interleaved converters mainly employ PI-based ACS

control techniques to achieve equal current distribution and reliable converter performance under healthy as well as faulty operating conditions.

Finally, reconfiguration methods are implemented to redistribute current among the remaining healthy phases and continue converter operation. In interleaved converters, current balancing controllers such as Average Current Sharing (ACS) help achieve dynamic current redistribution during fault conditions. These techniques improve converter reliability, reduce downtime, and ensure uninterrupted power delivery in critical applications.

2.6 Application of TPIBC Converter:

22

Hydrogen energy systems have gained significant attention in recent years because of the increasing demand for clean and sustainable energy technologies. Among different hydrogen production methods, water electrolysis is widely used due to its environmentally friendly operation and compatibility with renewable energy sources such as solar photovoltaic and wind energy systems. In an electrolyzer system, electrical energy is converted into chemical energy by splitting water molecules into hydrogen and oxygen gases. The performance and efficiency of the electrolyzer mainly depend on the quality of the DC power supplied to the electrolyzer stack.

Electrolyzer systems typically require a low voltage and high current DC power source for successful production of hydrogen. In real life applications, any ripples or fluctuations within the output current of the DC power source may result in poor performance of the electrochemical reaction process. Ripple within the current results in overheating, degradation of the electrodes, inefficient hydrogen production, and reduction of the life expectancy of the electrolysis stack.

In order to meet such specifications, the Three Phase Interleaved Buck Converter (TPIBC) becomes a suitable method for high current DC systems. In the TPIBC design, many buck converters run with phase-shifted signals that lead to reduced ripple and better output current quality. Due to the interleaving process, there is a considerable reduction in input and output current ripple, with the load current being shared equally by each converter stage.

As a result, TPIBC is highly compatible with hydrogen electrolyzer, battery charger, fuel cell system, and electric vehicle applications, which require stable low-voltage high current DC. In addition, the application of current balancing and fault-tolerance

schemes makes the converter work reliably both in normal operations and faulty operations.

2.7 Research Gap Identification:

There have been several studies conducted on multiphase interleaved buck converters, current sharing methodologies, and fault-tolerant approaches for high power DC applications. While current methods enhance the converter performance during ideal operations, there exist various practical problems that need to be addressed. One of the most significant disadvantages that has been found in conventional current sharing approaches is their inefficiency during non-ideal scenarios including parasitic resistances, component tolerances, switching times, and temperature variations. Practical issues tend to cause unequal distribution of currents among different phases of the converters leading to current imbalance and loss in conversion efficiency.

The current imbalance problem exists in most conventional converters when the system is subjected to dynamic modes and faults. The inability to balance currents causes unnecessary thermal stresses on semiconductor components and inductors, and hence decreases the efficiency of the entire system. In addition, the capability of ripple elimination of the converter is compromised when current sharing is not adequately addressed.

Fault tolerance handling techniques have also been highlighted as another problem in earlier studies. Most fault-tolerance techniques involve increased use of hardware components, complex sensing mechanisms, and complex algorithms that add to the cost of implementation and make the system more complicated. In some instances, the performance of the converters suffers greatly following the faults.

Consequently, the need for an enhanced ACS scheme that ensures accurate current sharing when the system is healthy and faulty arises. The objective of this study will be to develop a fault-tolerant three-phase interleaved buck converter utilizing PI-based ACS technique [39].

2.8 Summary of Literature Review:

In this chapter, an extensive review has been conducted regarding the state of the art in the area of conventional buck converters, multiphase interleaved converters, various current sharing techniques, fault-tolerant converter technology, and electrolyzer application. The results from the study revealed that conventional buck converters are ideal for use in applications where low to medium power level is required; but due to some of their drawbacks such as high ripple current, higher thermal stress, and low efficiency at high power levels, they are limited to only low and medium power levels.

Some of the commonly used techniques for current balancing include Average Current Sharing (ACS), droop control, master-slave control, current mode control, and digital control. Among the aforementioned current balancing techniques, ACS techniques have proven to be more accurate and efficient. In addition, the role of fault-tolerant converter system has been explained along with its significance in critical applications such as renewable energy, electric vehicles, and electrolyzers.

In addition to this, the impact of parasitics, ESR, switching delays, and imperfect semiconductor devices was also examined since these factors considerably influence the sharing of currents. From a review of the existing literature, it can be seen that there are significant problems in terms of current imbalance and fault tolerance in imperfect operating conditions. With this consideration in mind, a modified PI-based ACS-controlled fault tolerant TPIBC system has been suggested in this research study.

CHAPTER 3
TPIBC UNDER HEALTHY AND FAULTY CONDITIONS

3.1 Introduction of TPIBC

Three-Phase Interleaved Buck Converter (TPIBC) is one of the most recent DC-DC converter topologies developed to cater to the rising requirement for high current, high-power applications. Single-phase buck converters are very popular for use in voltage step-down applications due to their simple and easy construction. However, as the power levels grow higher, there are various drawbacks associated with single-phase converters. These include the generation of high current ripples, switching losses, poor thermal distribution, and the application of excessive stress on semiconductor elements. All these factors limit the performance of the converters and lower their reliability in terms of operation and power density.

In order to counteract the limitations faced by the single-phase buck converters, the technique of interleaving is introduced. Multiple converter phases are connected in parallel to form a bank of converters and switching signals that operate at different phases are used. As far as the Three-Phase Interleaved Buck Converter is concerned, three identical buck converter sections are operated in parallel mode while being subjected to switching signals with 120° phase difference. The load current is shared by the three phases.

One of the key advantages of TPIBC is the decrease in input/output current ripples owing to the ripple cancellation effect that results from phase shifting. Low ripples mean there will be little need for huge filter capacitors and high-quality output voltages. Moreover, the multiphase feature means that the heat produced is shared across multiple semiconductors instead of focusing on one phase alone.

TPIBC converters are widely used in renewable energy systems, electric vehicle charging systems, fuel cells, battery energy storage systems, and hydrogen electrolyzer applications where stable low-voltage and high-current DC output is required. Furthermore, implementation of current balancing and fault-tolerant control strategies improves converter reliability and enables continuous operation under abnormal operating conditions. Therefore, TPIBC has emerged as an effective solution for modern high-power DC conversion applications.

3.2 Circuit Diagram of TPIBC:

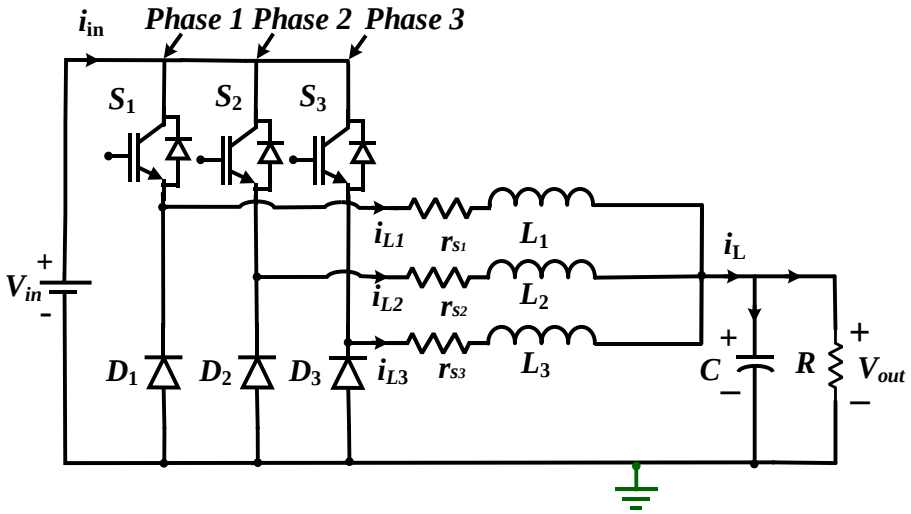

Figure 3.1 Circuit diagram of TPIBC with circuit parasitic.

The circuit configuration of the Three-Phase Interleaved Buck Converter (TPIBC) shown in Figure 2 consists of three identical buck converter phases connected in parallel and supplied from a common DC source (V_{in}). Each converter phase contains power semiconductor switches (MOSFETs or IGBTs) (S_1, S_2, S_3), diodes (D_1, D_2, D_3), inductors (L_1, L_2, L_3) and each inductor has parasitic resistance (r_{L1}, r_{L2}, r_{L3}) and shares a common output capacitor and load. The converter phases are operated using gate pulses shifted by 120° to achieve ripple reduction and improved current distribution. Also producing near-constant output current through ripple cancellation. The use of interleaving ensures that both i_{in} and i_L are spread over three phases, i.e., *Phase*-1, *Phase*-2, *Phase*-3. It is important to note that the correct choice of components plays an important role in sustaining the converter's performance and reliability.

Interleaving provides certain benefits in terms of reduced voltage and current ripples, effective heat dissipation, enhanced transient behavior, and high power density. At the same time, the disadvantages of interleaving include current imbalance due to mismatching of device parameters, increased circuit complexity, and susceptibility to component faults and tolerances. In real-world applications, there can be various faults occurring in the form of open switch, short circuit fault, or open inductor. An open switch will cause interruption in current in one phase, thus forcing other phases to compensate for it. Short circuit faults create high current in the inductor and might result in failure of the whole circuit. Power switches which use either MOSFETs or

IGBTs are the major switching components of the circuit. They run at high frequencies and regulate the amount of energy that is to be transferred between the input source and the output. The duty cycle of the switch signal is what controls the level of the output voltage of the converter.

The diodes are used as freewheeling diodes whose purpose is to create a path for the flow of current when the switching action of the switches is at its OFF stage. They enable smooth flow of current through the inductor, thus ensuring continuity in energy supply to the load.

Inductor is applied in every phase of the converter for storing energy and reducing the ripple effect in the current. Inductor serves in shaping the current wave shape and ensuring that there is continuous conduction mode operation. Due to the fact that current is shared by all the three phases, the stress experienced by the inductors becomes very minimal. Output Capacitor is connected across the load in order to reduce the effect of voltage ripples and ensure that there is a consistent output voltage.

Effects of Parasitics in Converters In practical power electronic converters, the effect of parasitic resistances plays an essential role in the operation of the converters. Parasitics can occur in semiconductor devices, inductors, capacitors, and PC board wiring. Resistances are inevitable in practical systems, and inductor parasitic resistance will increase the conduction losses and decrease converter efficiency. The switching delay in semiconductor devices influences synchronization between converter phases and may cause current imbalance in interleaved converters. One critical parasitic component is the Equivalent Series Resistance (ESR) of capacitors, which leads to energy dissipation, ripple in the output voltage, and generation of heat. Thus, it becomes imperative to consider the parasitic effect during the design and analysis of converters for an effective assessment of their performance. In addition, non-ideal components like the MOSFET and IGBT experience finite switching losses, on-state resistances, and leakage currents.

3.3 Operation of TPIBC

3.3.1 TPIBC under Healthy Condition

Under healthy operating conditions, the Three-Phase Interleaved Buck Converter (TPIBC) operates with all three converter phases functioning normally and contributing equally to power transfer. The converter consists of three identical buck

converter legs connected in parallel and controlled by gate pulses shifted by 120°. The phase-shifted operation ensures equal distribution of current among the three phases and significantly reduces input and output current ripple. During converter operation, each semiconductor switch alternates between ON and OFF states according to pulse-width modulation (PWM) signals. When a switch in a particular phase is turned ON, electrical energy from the DC input source is transferred to the corresponding inductor, causing the inductor current to increase gradually. During the OFF period, the stored energy in the inductor is released through the freewheeling diode and supplied to the output load. Since all three phases operate with identical switching frequency and duty cycle but with phase displacement, energy transfer occurs continuously throughout the switching cycle.

The total load current is equally shared among the three phases by implementing an Average Current Sharing (ACS) technique. For the proposed converter having an output current requirement of 40 A, each phase carries approximately 13.3 A under ideal operating conditions. Equal current distribution reduces current stress on semiconductor devices and improves thermal management. Moreover, the interleaving effect causes cancellation of ripple components generated by individual phase currents, thereby improving output current quality and reducing the requirement for large filter components.

Under normal circumstances, the TPIBC offers consistent output voltage, reduced ripple, minimized conduction losses, and improved efficiency. Consequently, the converter exhibits increased reliability and superior performance than traditional single-phase converters used for applications involving higher currents, such as the electrolysis of hydrogen and charging of electric vehicles.

3.3.2 Pulse Width Modulation (PWM) Technique of TPIBC under Healthy Condition

The PWM control method is one of the commonly used control strategies in interleaved converters for controlling output voltage and power transfer process. In case of TPIBC, equal frequency PWM signals are applied to the three switches (S_1, S_2, S_3) with a phase angle of 120°. The duty cycle of PWM determines the ON time of the switches and has a direct impact on the output characteristics of the converter. The three modes of operation of the converter can be distinguished based on the duty cycle value.

The PWM interleaving control method is a popular strategy in the multi-phase conversion system due to improved converter performance and lower ripple value. The PWM interleaving method is applied in TPIBC in the way that three phases of the converter are controlled with identical duty cycles and frequencies while keeping a certain phase displacement. The main purpose of applying PWM interleaving control method is an even distribution of load current across converter phases and improved output characteristics. Phase shift is modified according to the number of active phases and can be represented as:

$$\theta = \frac{360^{\circ}}{N} \tag{3.1}$$

Where N denotes the number of active phases, For N=3, phase shift becomes 120°.

In healthy conditions, the phase angle of the three pulses is 120° apart from each other. As one switching cycle makes an angle of 360°, the phase difference between two consecutive converters is calculated using 360°/3=120°. This helps to make sure that the output current ripple formed by the inductors partially gets canceled out because of each other. This results in increasing the ripple frequency at the output three times the switching frequency. If the switching frequency of each leg is 20 kHz, then the effective ripple frequency at the output will become 60 kHz.

One of the primary benefits associated with PWM interleaving technology is the process of ripple cancellation. The inductor current ripples of each of the converters' phases occur due to the switching process. However, since the ripples are phase-shifted from each other, their effects cancel each other out when they interact on the output stage. Consequently, the total ripples occurring at the output stage become considerably smaller compared to a traditional single-phase buck converter.

The timing diagram of the TPIBC includes three switching signals which are the phase-A, phase-B, and phase-C gate pulses, which are 120° apart from each other. It should be noted that thanks to this sequence of events, energy transfer occurs constantly. Thus, in addition to improving the ripple behavior, PWM interleaving provides increased efficiency and improved heat dissipation as well as reduced stress for high current applications, such as hydrogen electrolyzer.

Case 1: D < 1/3

With a duty ratio below one-third of the switching period, each phase has an on-time which is fairly small. At this point, there is practically no overlapping time between switching pulses from different phases. During their ON-time, each phase independently transmits energy. There is no effective ripple compensation since only one phase is active at a given time. Hence, input and output current ripple levels are high, and the utilization efficiency of the converter is low. However, the current balancing across phases stays well-maintained since it involves phase-shifted operation.

Case 2: D = 1/3

At the stage when the duty cycle equals one-third, the on-time periods of adjacent phases are evenly spread without any over-lap. It can be termed as the best condition when the ripple level is minimum. In such a case, the ripple current caused by one phase gets cancelled out by the others because of the 120° phase difference. Thus, the output ripple current level drops to its lowest possible value.

Case 3: D > 1/3

If the duty ratio is greater than one-third, overlap during switching of consecutive phases increases significantly. Multiple phases operate at the same time for some period of time. In this case, efficiency for power conversion improves along with the capacity for handling higher loads. Overlap can also cause circulating currents among the phases and increased switching losses. Even if current balancing takes place with ACS, high duty ratio can still cause extra thermal stresses and care must be taken while designing such control. Therefore, appropriate duty ratio selection becomes crucial in achieving the desired results from the TPIBC.

3.3.3 TPIBC under Faulty Condition

Under faulty operation, the TPIBC operates quite differently than in the case of healthy operation owing to the presence of the fault condition existing within one of the phases of the converter. Within practical electronic systems, semiconductor device faults may be caused due to several reasons such as gate driver faults, excessive heat, faulty switching, aging and others. One of the most common types of faults that are seen within interleaved converters is an open switch fault.

In the case where an open circuit switch fault occurs in one of the converter's phases, only two other phases will be operational. The controller system will then change its switching control process to ensure that the output performance of the system is maintained. In such a case, since there are only two working phases, their phase difference becomes 180° from 120°. Phase shift is modified accordingly to the number of active phases and can be represented as:

$$\theta = \frac{360^{\circ}}{N} \tag{3.2}$$

Where N denotes the number of active phases. For N=2, Phase shift becomes 180°.

An open-switch fault in any of the legs of the TPIBC causes it to become non-operational and be unable to share the power supply burden. Therefore, the faulty leg does not contribute any current. To meet the load requirements, however, the other two legs have to carry the current load of the non-operating leg. Without a proper control method in place, the above problem will lead to an imbalance of current sharing among the three phases.

In case of faults, the ripple cancellation ability is affected since only two phases are involved in the conversion process. This means that the ripple frequency will be reduced from $\mathbf{3}fs$ in the normal situation to $\mathbf{2}fs$ when the system is faulty. If the switching frequency is assumed to be 20 kHz, then the ripple frequency changes from 60 kHz to 40 kHz.

In order to provide stable converter performance, an ACS control approach is employed. This controller keeps track of the currents flowing in each phase and automatically reallocates the load current among the phases that are performing satisfactorily. In the case of the control algorithm designed using this approach, having a total output current of 40 A, in the event of a fault in one phase, the other two phases handle approximately 20 A each.

Healthy timing diagram includes three pulses of gates (*Phase*-1, *Phase*-2, and *Phase*-3), having an interval of 120°. In case of one-phase failure, the phase pulse is not there anymore, leaving behind only two gate pulses with a phase angle difference of 180°. The new timing sequence helps provide uninterrupted power, along with ensuring that the currents of the healthy phases are shared evenly. Hence, Adaptive PWM interleaving helps achieve fault tolerance in TPIBC.

Though the operation of the converters remains unaffected in case of fault, there is bound to be some compromise on performance. Due to decreased active phases, the ripple cancellation capability is reduced, leading to higher current and voltage ripple at the output. In addition, due to increased current loading in healthy semiconductors, there is greater heat loss too. But with the use of fault-tolerant techniques for control, continuous power delivery can still be ensured, which will make the system more reliable.

3.3.4 Pulse Width Modulation (PWM) Technique of TPIBC Under Faulty Condition

Under faulty operating conditions, the PWM control strategy of the TPIBC requires modification to maintain stable converter operation after one phase becomes inactive. Since one converter phase is avoid at fault, only two healthy phases deliver in power transfer. The switching pulses of the healthy phases are adjusted to compensate for the loss of the faulty converter leg and maintain the required output voltage and current.

Case 1: D < 1/3

When the duty cycle is less than one-third of the switching period, the ON interval of each healthy switch is relatively small. Since only two active phases remain available after fault occurrence, the overlap between switching signals is limited. During this operating condition, the converter transfers relatively low power to the load and current ripple becomes higher because the ripple cancellation effect decreases compared to healthy operation. The converter can continue operating, but ripple content and current stress increase.

Case 2: D = 1/3

When the duty cycle reaches one-third, better switching coordination is realized among the other two functional phases. PWM pulses are allocated uniformly in order to minimize the effect of ripple cancellation using fewer functional phases. Under this condition, current balancing is much easier and therefore results in good converter performance compared to when using duty cycles below one-third.

Case 3: D > 1/3

For duty cycles larger than one-third, there will be longer ON times for the switches and considerable overlap of the switching periods for the healthy switches. Such a situation makes it possible for the converter to fulfill higher requirements by providing larger conduction periods for healthy switches. Nevertheless, the larger current through the healthy switches means more conduction losses in addition to thermal stress on the switches.Thus, proper control of PWM becomes crucial under such fault scenarios for sustaining stability and low ripple levels.

3.4 Modes of Operation of TPIBC

The operation of the Three-Phase Interleaved Buck Converter (TPIBC) can be analyzed in terms of four operating modes according to the switch states of the semiconductors and the associated current paths. In each switching period, various combinations of switches and diodes operate in order to produce a current flow resulting in energy transmission from the input to the output. The impact of the parasitic resistance (r_{L1}, r_{L2}, r_{L3}) of the inductor affects the distribution of currents and adds extra conduction losses in real-world applications.

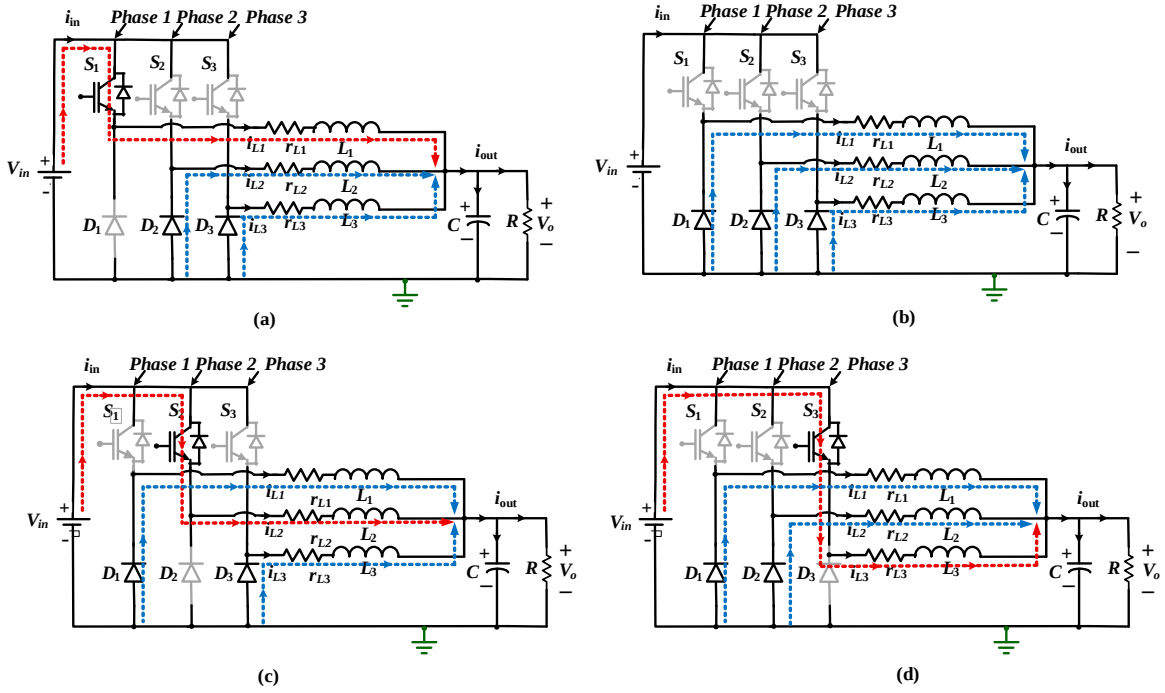

Figure 3.2. Circuit diagram of TPIBC with inductor parasitic resistance during (a) *mode*-1 (b) *mode*-2 (c) *mode*-3 (d) *mode*-4

3.4.1 Mode 1

In the first operational mode, illustrated in diagram (a), the active semiconductor switch S_1 is turned ON, while the parallel switches S_2 and S_3 remain in their OFF state. The input DC voltage V_{in} is applied directly across the first phase of the interleaved structure. Consequently, the primary current flows from the input source through S_1, the parasitic resistance r_{L1}, and the primary inductor L_1, before reaching the output filter capacitor C and the load resistor R. Throughout this duration, L_1 accumulates magnetic energy, resulting in a linear increase in its phase current. Simultaneously, the second and third phases operate in a freewheeling capacity. Because S_2 and S_3 are open, the energy previously stored in inductors L_2 and L_3 sustains the current flow to the load. These discharging currents circulate from the ground plane, forward-biasing the freewheeling diodes D_2 and D_3. The currents pass through r_{Z2} and r_{Z3} paralleling their corresponding inductors, decaying linearly with respect to time. The total current i_{out} that goes into the load, is derived by summing up the charging current in phase one and discharging current in phase two and three.

$$\frac{di_{L_1}}{dt} = \frac{V_{in}}{L_1} - \frac{r_{L_1} i_{L_1}}{L_1} - \frac{V_O}{L_1} \tag{3.3}$$

$$\frac{di_{L_2}}{dt} = -\left(\frac{r_{L_2} i_{L_2}}{L_2} + \frac{V_O}{L_2} \right) \tag{3.4}$$

$$\frac{di_{L_3}}{dt} = -\left(\frac{r_{L_3} i_{L_3}}{L_3} + \frac{V_O}{L_3} \right) \tag{3.5}$$

$$\frac{dV_C}{dt} = \frac{i_{L_1}}{C} + \frac{i_{L_2}}{C} + \frac{i_{L_3}}{C} - \frac{V_O}{RC} \tag{3.6}$$

3.4.2 Mode 2

Mode 2 shown in Fig. (b) Represents a midway operation mode where all three switches S_1, S_2, and S_3 are turned OFF completely. This is due to the reason that the duty cycle of the system remains below one-third (D < 1/3). During this sub-interval, the primary input voltage source V_{in} is isolated from the main power stage, meaning no direct energy is drawn from the supply. However, the whole operation relies on the stored magnetic energy in the three phase inductors (L_1, L_2 and L_3). In the absence of the input voltage, the freewheeling diodes (D_1, D_2 and D_3) become active, allowing the current to pass through the inductors. In every phase, the current passes from the

ground terminal to the conducting diode and then to the series resistance (r_{Z1}, r_{Z2}, r_{Z3}), and then to the inductors, to make it to the output side.. Because the inductors are discharging against the output voltage, the current in all three branches experiences a linear decay. The output capacitor *C* absorbs these combined decaying currents to filter the output and maintain a regulated voltage across the load resistor.

$$\frac{di_{L_1}}{dt} = -\left(\frac{r_{L_1} i_{L_1}}{L_1} + \frac{V_O}{L_1}\right) \tag{3.7}$$

$$\frac{di_{L_2}}{dt} = -\left(\frac{r_{L_2} i_{L_2}}{L_2} + \frac{V_O}{L_2}\right) \tag{3.8}$$

$$\frac{di_{L_3}}{dt} = -\left(\frac{r_{L_3} i_{L_3}}{L_3} + \frac{V_O}{L_3}\right) \tag{3.9}$$

$$\frac{dV_C}{dt} = \frac{i_{L_1}}{C} + \frac{i_{L_2}}{C} + \frac{i_{L_3}}{C} - \frac{V_O}{RC} \tag{3.10}$$

3.4.3 Mode 3

The third mode of operation, shown in diagram (c), initiates the active energy accumulation phase for the second interleaved branch. In this specific configuration, switch S_2 is commanded to the ON position, while switches S_1 and S_3 are actively held in the OFF state. With S_2 conducting, the primary DC input voltage V_{in} is coupled directly to the phase two circuitry. Current propagates from the source, through the semiconductor switch S_2 the associated parasitic resistance r_{L2}, and the inductor L_2, subsequently delivering power to the common output node. During this specific interval, the magnetic core of L_2 stores energy, which is characterized by a linear ramp-up of the phase two current i_{L2}. Concurrently, the first and third parallel branches function in their freewheeling states. The inductors L_1 and L_3 act as secondary power sources, discharging their previously stored energy to support the ongoing load demand. The current through each respective completes the cycle by causing a forward bias on the freewheeling diode D_1 and D_3, demonstrating a smooth linear descent. The combined superposition of the increasing current in phase two with

decreasing currents in phase one and three sustains the ripple-free qualities vital to interleaved systems.

$$\frac{di_{L_1}}{dt} = -\left(\frac{r_{L_1} i_{L_1}}{L_1} + \frac{V_O}{L_1}\right) \tag{3.11}$$

$$\frac{di_{L_2}}{dt} = \frac{V_{in}}{L_2} - \frac{r_{L_2} i_{L_2}}{L_2} - \frac{V_O}{L_2} \tag{3.12}$$

$$\frac{di_{L_3}}{dt} = -\left(\frac{r_{L_3} i_{L_3}}{L_3} + \frac{V_O}{L_3}\right) \tag{3.13}$$

$$\frac{dV_C}{dt} = \frac{i_{L_1}}{C} + \frac{i_{L_2}}{C} + \frac{i_{L_3}}{C} - \frac{V_O}{RC} \tag{3.14}$$

3.4.4 Mode 4

Mode 4, represented by figure (d), is the final active sub-interval in the basic switching cycle, where attention is paid to the third parallel path. In this case, the controller activates the switch S_3 ON, while the main switches, S_1 and S_2 , continue in the OFF state. Activation of the S_3 ensures that there is a direct electrical path from the power source Vin to the inductor. The power flows via S_3 , the parasitic resistance present in r_{L3} and L_3 , charging the output filter and powering the load. During this entire time, L_3 is able to absorb energy, hence making the current i_{L3} increase linearly. Similarly, the diode D_3 is reversed biased and does not conduct. On the other hand, phases 1 and 2 operate in the mode of discharging energy. Since the switches are in the open state, inductors L_1 and L_2 discharge their magnetic energy to prevent any interruption in the load. The circuit in this instance operates through the free-wheeling paths formed by the forward-biased diodes D_1 and D_2 . Here, current flows from the source through the diodes i_{L1} and i_{L2} to the load with linearly decreasing value. This, according to previous discussion, guarantees the minimization of the ripple component in the output current.

$$\frac{di_{L_3}}{dt} = \frac{V_{in}}{L_3} - \frac{r_{L_3} i_{L_3}}{L_3} - \frac{V_O}{L_3} \tag{3.15}$$

$$\frac{di_{L_1}}{dt} = -\left(\frac{r_{L_1} i_{L_1}}{L_1} + \frac{V_O}{L_1}\right) \tag{3.16}$$

$$\frac{di_{L_2}}{dt} = -\left(\frac{r_{L_2} i_{L_2}}{L_2} + \frac{V_O}{L_2}\right) \tag{3.17}$$

$$\frac{dV_C}{dt} = \frac{i_{L_1}}{C} + \frac{i_{L_2}}{C} + \frac{i_{L_3}}{C} - \frac{V_O}{RC} \tag{3.18}$$

3.4.5 Mathematical Equations and Switching States of TPIBC

The equivalent circuit diagram of TPIBC can be defined as a combination of three power stages connected in parallel, having one DC input source (V_{in}) and a common output filter consisting of a capacitor (C) and a load resistor (R). In each of the parallel phases, there is a switch element (S_k, where k = 1, 2, 3), freewheeling diode (D_k), and energy storage inductor (L_k). In order to model real-world behavior of the circuit, the parasitic resistance (r_{Lk}) of each inductor has been included into the equivalent circuit diagram.

The current paths within the converter shift strictly based on the operational phase. In the active state (when a switch is ON), current flows directly from V_{in}, through the conducting active switch S_k, the associated parasitic resistance r_{Lk}, and the inductor L_k, delivering power to the output network while the corresponding diode D_k remains reverse-biased. During the freewheeling state (when a switch is OFF), the stored magnetic energy forces the current to maintain circulation from the ground plane, forward-biasing the diode D_k, passing through r_{Lk} and L_k, and finally dissipating into the load.

The present flow pattern in the converter changes strictly depending on its mode of operation. In active mode (switch ON), current is supplied directly from the source V_{in}, flowing through the active switch S_k, its parasitic resistance r_{Lk} , and the inductor L_k, providing energy for the output circuit when the respective diode D_k is in reverse bias. When in freewheeling mode (switch OFF), the stored magnetic energy pushes current to continue circulating from the ground plane, forward biasing the diode D_k , flowing through r_{Lk} and L_k .

The dynamic continuous inductor currents are given by mathematical equations. If S_k is ON, the inductor voltage determines a linear increase in current as defined by the differential equation:

$$L_k \frac{di_{Lk}}{dt} = V_{in} - i_{Lk}.r_{Lk} - V_o \tag{3.19}$$

S_k is OFF, the accumulated energy is discharged and the current decay is governed

by:

$$L_k \frac{di_{Lk}}{dt} = V_{in} - i_{Lk}.r_{Lk} - V_o \quad (3.20)$$

The total instantaneous output current supplied to the filter network is the aggregate sum of all individual phase currents:

$$i_{out} = i_{L1} + i_{L2} + i_{L3} \quad (3.21)$$

The switching states are in a 120° phase-shift pattern so that properly interleaved operations are ensured. In the duty cycle configuration of $d < 1/3$, the states change in a systematic way. *Mode* 1 is defined by the Boolean state $(S_1 = 1, S_2 = 0, S_3 = 0)$. Mode 2 is a transitional discharging state with all switches OFF $(S_1 = 0, S_2 = 0, S_3 = 0)$. *Mode* 3 activates the second phase $(S_1 = 0, S_2 = 1, S_3 = 0)$, and *Mode* 4 activates the final phase $(S_1 = 0, S_2 = 0, S_3 = 1)$. This well coordinated sequence reduces greatly the output voltage ripple and distributes evenly the thermal stress among all the semiconductor devices.

12

Table I 3.1 Different Modes of Operation of TPIBC

Modes of operation	Time Interval	Load Current Characteristics	Active Switches
Mode 1	$t_0 - t_1$	i_{L1} ↑ i_{L2} ↓ i_{L3} ↓	S_1, D_2, D_3
Mode 2	$t_1 - t_2$, $t_3 - t_4$, $t_5 - t_6$	i_{L1} ↓ i_{L2} ↓ i_{L3} ↓	D_1, D_2, D_3
Mode 3	$t_2 - t_3$	i_{L1} ↓ i_{L2} ↑ i_{L3} ↓	D_1, S_2, D_3
Mode 4	$t_4 - t_5$	i_{L1} ↓ i_{L2} ↓ i_{L3} ↑	D_1, D_2, S_3

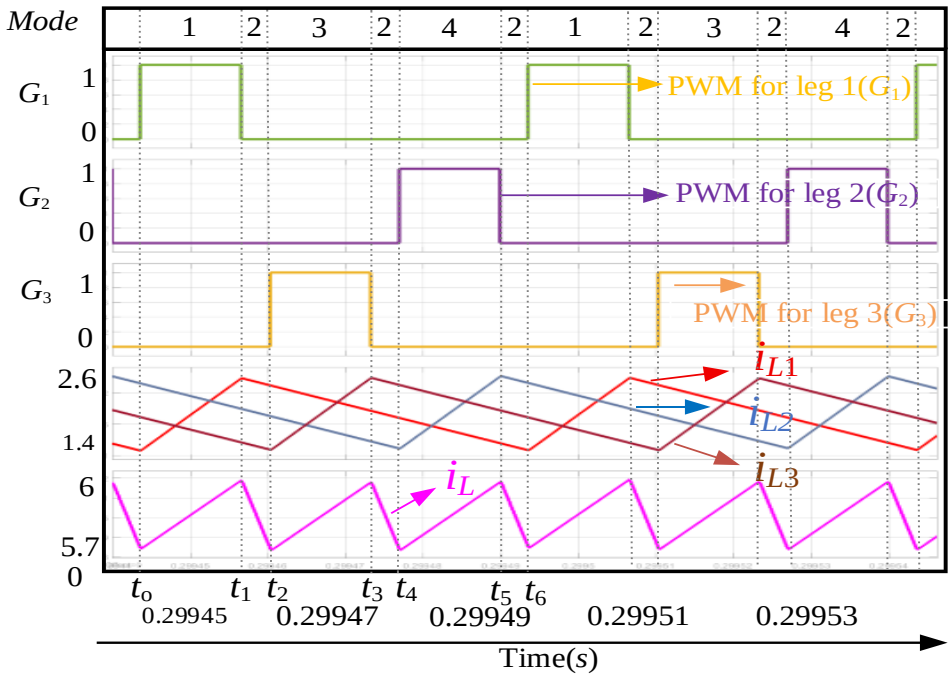

Figure 3.3 FTTPIB converter with phase gating pulse, inductor currents and output current.

CHAPTER 4
MODELLING OF TPIBC WITH CIRCUIT PARASITICS

4.1 Mathematical Modeling

Step 1: To model this TPIBC in state-space matrix form, we will use the **State-Space Averaging Method**. We will assume the converter operates in Continuous Conduction Mode (CCM), which is standard for interleaved high-power applications.

First, we identify our state variables (energy-storing elements), input, and switching functions.

- **State Vector (*x*):** The currents through the three inductors and the voltage across the output capacitor

$$x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_o \end{bmatrix} \tag{4.1}$$

- **Input (*u*):** The input DC voltage source

$$u = V_{in} \tag{4.2}$$

- **Switching Functions (s_k):** Let $s_1, s_2, s_3 \in \{0,1\}$ represent the states of the active switches S_1, S_2, S_3.
- s_k = 1: Switch is ON, diode is reverse-biased. Node voltage is V_{in}.
- s_k = 0: Switch is OFF, freewheeling diode conducts. Node voltage is 0.

Step 2: Instantaneous Differential Equations

We apply Kirchhoff's laws to the circuit for each phase to get the large-signal differential equations.

1. Inductor Equations (KVL): For any given phase *k* (where *k* = 1, 2, 3), the voltage across the inductor L_k is the node voltage minus the voltage drop across its series resistance r_{Lk} minus the output voltage V_o

$$\frac{di_{L1}}{dt} = -\frac{r_{L1}}{L_1} i_{L1} - \frac{1}{L_1} V_o + \frac{s_1}{L_1} V_{in} \tag{4.3}$$

$$\frac{di_{L2}}{dt} = -\frac{r_{L2}}{L_2} i_{L2} - \frac{1}{L_2} V_o + \frac{s_2}{L_2} V_{in} \tag{4.4}$$

$$\frac{di_{L3}}{dt} = -\frac{r_{L3}}{L_3} i_{L3} - \frac{1}{L_3} V_o + \frac{s_3}{L_3} V_{in} \tag{4.5}$$

2. Capacitor Equation (KCL): Applying KCL at the output node, the sum of the currents from the three inductors equals the current through the capacitor plus the current through the load resistor (R).

$$i_{L1} + i_{L2} + i_{L3} = C\frac{dV_o}{dt} + \frac{V_o}{R} \tag{4.6}$$

Rearranging for the voltage derivative:

$$\frac{dV_o}{dt} = \frac{1}{C} i_{L1} + \frac{1}{C} i_{L2} + \frac{1}{C} i_{L3} - \frac{1}{RC} V_o \tag{4.7}$$

4.2 State-Space Averaging:

To make the model useful for linear control design, we average the equations over a single switching period T_s The discrete switching states s_1, s_2, s_3 are replaced by their continuous duty cycles d_1, d_2, d_3 where $d \in [0,1]$.

$$\frac{di_{L1}}{dt} = -\frac{r_{L1}}{L_1} i_{L1} - \frac{1}{L_1} V_o + \frac{d_1}{L_1} V_{in} \tag{4.8}$$

$$\frac{di_{L2}}{dt} = -\frac{r_{L2}}{L_2} i_{L2} - \frac{1}{L_2} V_o + \frac{d_2}{L_2} V_{in} \tag{4.9}$$

$$\frac{di_{L3}}{dt} = -\frac{r_{L3}}{L_3} i_{L3} - \frac{1}{L_3} V_o + \frac{d_3}{L_3} V_{in} \tag{4.10}$$

$$\frac{dV_o}{dt} = \frac{1}{C} i_{L1} + \frac{1}{C} i_{L2} + \frac{1}{C} i_{L3} - \frac{1}{RC} V_o \tag{4.11}$$

Final Matrix Formulation: Now, we can format these averaged differential equations into the standard state-space form:

$$\dot{x} = Ax + Bu \tag{4.12}$$

The System Matrix (A):

$$A=\begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & -\frac{1}{L_1} \\ 0 & -\frac{r_{L2}}{L_2} & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{r_{L3}}{L_3} & -\frac{1}{L_3} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{4.13}$$

The Input Matrix (B):

$$B=\begin{bmatrix} \frac{d_1}{L_1} \\ \frac{d_2}{L_2} \\ \frac{d_3}{L_3} \\ 0 \end{bmatrix} \tag{4.14}$$

Therefore, the complete Large-Signal Averaged State-Space Model is:

$$\begin{bmatrix} \frac{di_{L1}}{dt} \\ \frac{di_{L2}}{dt} \\ \frac{di_{L3}}{dt} \\ \frac{dV_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & -\frac{1}{L_1} \\ 0 & -\frac{r_{L2}}{L_2} & 0 & -\frac{1}{L_2} \\ 0 & 0 & -\frac{r_{L3}}{L_3} & -\frac{1}{L_3} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_o \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L_1} \\ \frac{d_2}{L_2} \\ \frac{d_3}{L_3} \\ 0 \end{bmatrix} V_{in} \tag{4.15}$$

4.3 Small-Signal Modelling of TPIBC

If you intend to use this matrix to extract transfer functions (like control-to-output $\frac{\hat{v}_o}{\hat{d}}$) for tuning PI/PID compensators, you will need to perturb and linearize this model.

By substituting $x = X + \hat{x}$, $d = D + \hat{d}$ and $v_{in} = V_{in} + \hat{v}_{in}$ into the equations above and removing the steady-state DC terms and non-linear AC cross-products, your control matrix B_d relating the state derivatives specifically to variations in the duty cycles $\hat{d}_1, \hat{d}_2, \hat{d}_3$ becomes:

$$B_d = \begin{bmatrix} \frac{V_{in}}{L_1} & 0 & 0 \\ 0 & \frac{V_{in}}{L_2} & 0 \\ 0 & 0 & \frac{V_{in}}{L_3} \\ 0 & 0 & 0 \end{bmatrix} \tag{4.16}$$

This B_d matrix is highly relevant when simulating specific switch faults (e.g., forcing $d_1 = 0$) to observe dynamic system recovery.

To design your closed-loop controllers (like a PI controller for voltage regulation), you need the small-signal AC model. By applying the perturbation and linearization method mentioned previously, we isolate the dynamic responses.

The standard small-signal state-space equation is:

$$\dot{\hat{x}} = A\hat{x} + B_v\hat{v}_{in} + B_d\hat{d} \tag{4.17}$$

$$\hat{y} = C\hat{x} + D\hat{u} \tag{4.18}$$

Where the " $\hat{}$ " denotes small AC variations around the steady-state operating point.

Assuming you are controlling the duty cycles identically during normal operation (d_1=d_2=d_3=d), the matrices are:

- **System Matrix (*A*):** Remains the same as the large-signal model.
- **Input-to-State Matrix (B_v):** Corresponds to line variations $\hat{v}_{in}$.

$$B_v = \begin{bmatrix} \frac{d}{L_1} \\ \frac{d}{L_2} \\ \frac{d}{L_3} \\ 0 \end{bmatrix} \tag{4.19}$$

- **Control-to-State Matrix (B_d):** Corresponds to duty cycle variations $\hat{d}_1, \hat{d}_2, \hat{d}_3$.

$$B_d = \begin{bmatrix} \frac{V_{in}}{L_1} & 0 & 0 \\ 0 & \frac{V_{in}}{L_2} & 0 \\ 0 & 0 & \frac{V_{in}}{L_3} \\ 0 & 0 & 0 \end{bmatrix} \tag{4.20}$$

- **Output Matrix (C):** If we are regulating the output voltage $\hat{v}_o$, we isolate the 4th state.

$$C = \begin{matrix} 0 & 0 & 0 & 1 \end{matrix} \tag{4.21}$$

- **Feedforward Matrix (D):** Is zero, as duty cycle does not instantly appear at the output voltage.

$$D = \begin{matrix} 0 & 0 & 0 \end{matrix} \tag{4.21}$$

4.4 Transfer Functions of TPIBC:

With the matrices defined, you can extract the transfer functions using the standard formula:

$$G(s) = C(sI - A)^{-1}B + D \tag{4.22}$$

To find the Control-to-Output Transfer Function $G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}$, you would use B_d

Because you have three independent control inputs $\hat{d}_1, \hat{d}_2, \hat{d}_3$, $G_{vd}(s)$ will actually yield a 1×3 matrix of transfer functions, one for each phase's contribution to the output voltage. In a perfectly balanced, symmetrical system ($L_1 = L_2 = L_3 = L$ and $r_{L1} = r_{L2} = r_{L3} = r_L$), these three transfer functions will be identical.

4.4.1 Control to Output Transfer Functions:

$$G_{vd1}(s) = \frac{V_o(s)}{d_1(s)} = \frac{1.021\times10^9 s^2 + 1.021\times10^{12} s + 2.553\times10^{14}}{s^4 + 2978s^3 + 6.68\times10^7 s^2 + 6.506\times10^{10} s + 1.614\times10^{13}} \tag{4.23}$$

Continuous-time transfer function.

$$G_{vd2}(s) = \frac{V_o(s)}{d_2(s)} = \frac{1.021\times10^9 s^2 + 1.021\times10^{12} s + 2.553\times10^{14}}{s^4 + 2978s^3 + 6.68\times10^7 s^2 + 6.506\times10^{10} s + 1.614\times10^{13}} \tag{4.24}$$

Continuous-time transfer function.

$$G_{vd3}(s) = \frac{V_o(s)}{d_3(s)} = \frac{1.021\times10^9 s^2 + 1.021\times10^{12} s + 2.553\times10^{14}}{s^4 + 2978s^3 + 6.68\times10^7 s^2 + 6.506\times10^{10} s + 1.614\times10^{13}} \tag{4.25}$$

Continuous-time transfer function.

4.4.2 Line to Output Transfer Function:

$$G_{vg}(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{1.596\times10^7 s^2 + 1.596\times10^{10} s + 3.989\times10^{12}}{s^4 + 2978s^3 + 6.68\times10^7 s^2 + 6.506\times10^{10} s + 1.614\times10^{13}} \tag{4.26}$$

Continuous-time transfer function.

4.4.3 Inductor Current Transfer Functions:

$$G_{id1}(s) = \frac{i_{L1}(s)}{d_1(s)} = \frac{480000s^3 + 1.189\times10^9 s^2 + 2.125\times10^{13} s + 1.039\times10^{16}}{s^4 + 2978s^3 + 6.68\times10^7 s^2 + 6.506\times10^{10} s + 1.614\times10^{13}} \tag{4.27}$$

Continuous-time transfer function.

$$G_{id2}(s) = \frac{i_{L2}(s)}{d_2(s)} = \frac{480000s^3 + 1.189\times10^9 s^2 + 2.125\times10^{13} s + 1.039\times10^{16}}{s^4 + 2978s^3 + 6.68\times10^7 s^2 + 6.506\times10^{10} s + 1.614\times10^{13}} \tag{4.28}$$

Continuous-time transfer function.

$$G_{id3}(s)=\frac{i_{L3}(s)}{d_3(s)}=\frac{480000s^3+1.189\times10^9 s^2+2.125\times10^{13}s+1.039\times10^{16}}{s^4+2978s^3+6.68\times10^7 s^2+6.506\times10^{10}s+1.614\times10^{13}} \quad (4.29)$$

Continuous-time transfer function.

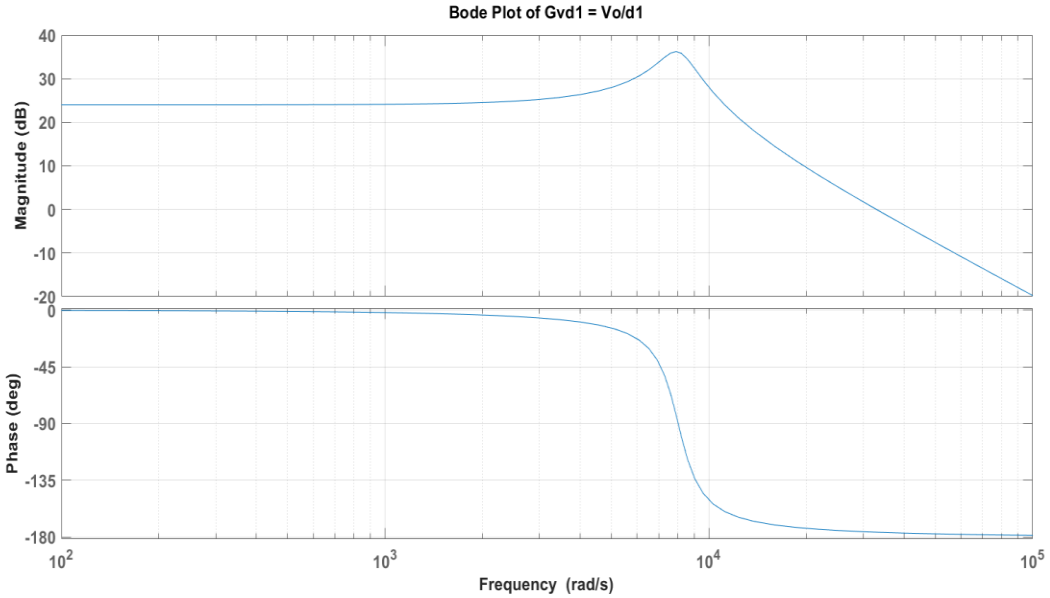

Figure 4.1 Bode Plot of Control-to-Output Transfer Function $G_{vd1}(s)=\frac{V_o(s)}{d_1(s)}$

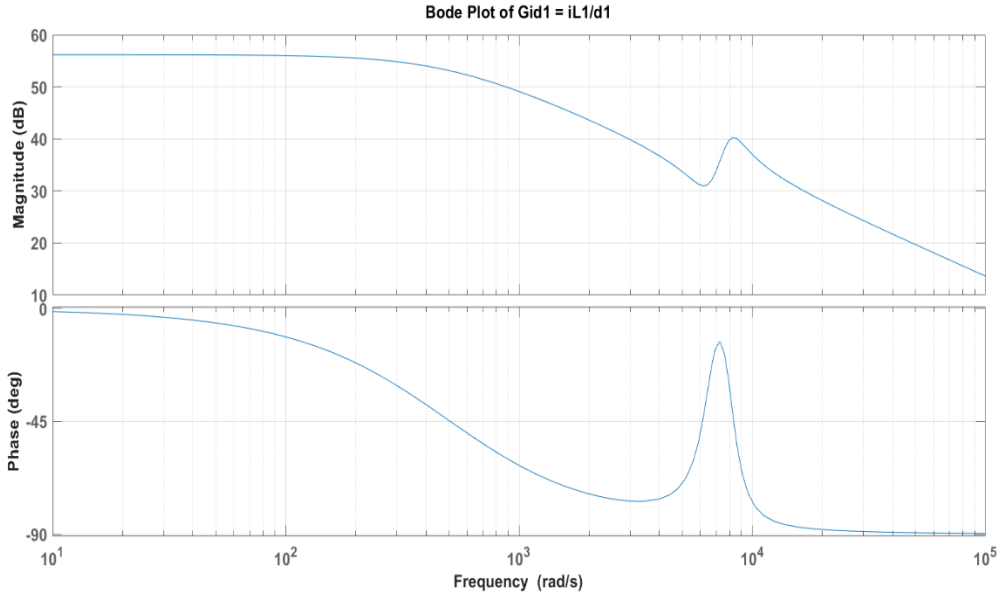

Figure 4.2: Bode Plot of Current Loop Transfer Function $G_{id1}(s)=\frac{i_{L1}(s)}{d_1(s)}$

4.5 Current Ripple Analysis

Current ripple analysis is an important aspect in the performance evaluation of the TPIBC. In high-current DC-DC converter applications, excessive ripple current affects output voltage quality, increases switching losses, produces additional thermal stress, and reduces overall system efficiency. Therefore, reduction of ripple current is one of the major objectives in interleaved converter design. The TPIBC topology achieves significant ripple reduction through phase-shifted operation of multiple converter phases.

In a conventional single-phase buck converter, the entire load current flows through a single inductor, resulting in relatively high inductor current ripple and output voltage ripple. However, in the proposed TPIBC, the total load current is divided among three parallel converter phases operating with a phase shift of 120°. Due to this interleaving operation, the ripple components generated by individual phase inductors partially cancel each other at the output side. Consequently, the net output current ripple becomes significantly smaller compared to a single-phase converter.

Symbol	Description
(Δi_L)	Inductor ripple current
(V_{in})	Input voltage
(V_o)	Output voltage
(D)	Duty cycle
(T_s)	Switching period
(L)	Inductance

The inductor current ripple equation is: $i_L = \frac{(V_{in} - V_o)DT_s}{L}$ Because of interleaving, the effective ripple frequency at the output becomes three times the switching frequency under healthy operating conditions. For example, if each converter phase operates at 20 kHz, the effective ripple frequency observed at the output becomes approximately 60 kHz. Higher ripple frequency reduces the requirement for large filter components and improves dynamic response.

Under one-phase fault conditions, only two active phases participate in power transfer. In this situation, the ripple cancellation capability decreases because the phase shift changes from 120° to 180°. As a result, output current ripple increases and additional stress is imposed on the remaining healthy phases. As a result, current ripple analysis

is crucial for evaluating converter performance in both abnormal and healthy operating situations.

4.6 Effect of Parasitic Resistance

In real power electronic converter there are no ideal conditions of the circuit, as the internal characteristics and non-ideal resistance of every electrical component exist. These undesirable parasitic elements are called Parasitic Resistances. The Three-Phase Interleaved Buck Converter (TPIBC) has a predominant parasitic resistance in the windings of the inductor, semiconductor switches, interconnecting conductors and PCB tracks, plus parasitic resistance of the capacitors, specifically their ESR. These resistances are typically small but play significant roles in converter performance, especially for high current applications like hydrogen electrolyzers, renewable energy systems, and electric vehicle charging systems.

Among different parasitic elements, the inductor parasitic resistance plays a major role in current sharing and power loss. Due to the presence of winding resistance (r_L), voltage drop occurs across the inductor during converter operation. This additional voltage drop reduces the effective output voltage and increases conduction losses. The inductor voltage equation considering parasitic resistance is expressed as: $L\frac{di_L}{dt} = DV_{in} - V_o - r_L i_L$ The term r_L represents the voltage drop caused by the parasitic resistance. As the load current increases, the power loss associated with parasitic resistance also increases according to: $P_{loss} = i_L^2 r_L$

Also, the current balancing between interleaved phases is compromised by parasitic resistance. Due to small differences in the resistance value between the different inductors, unequal currents are shared, resulting in one phase having a greater current in it than the others. Two of the disadvantages of this imbalance are increased thermal stress to the semiconductor device and decreased converter reliability.

If the operating conditions are not ideal, the effect of parasitic resistance is more significant, due to the rise of current in the remaining healthy phases following fault. Therefore, the conduction loss and temperature rise at the point rise considerably higher. Further, parasite response lowers converter efficiency, changes transient response and influences the transient response of the system.

To obtain reliable operation under healthy and faulty conditions, therefore, parasitic resistance must be properly considered at mathematical modelling, controller design and performance analysis of the designed proposed TPIBC system should be carried out.

4.7 Output Voltage Ripple Analysis

One of the key performance parameters in Three-Phase Interleaved Buck Converter (TPIBC) mainly used in the field of high current DC-output systems including hydrogen electrolyzers, fuel cell systems and battery charging systems is the output voltage ripple. High voltage spike might cause inefficiency in the system, impact the load function and add load on output components. As a result, it is crucial to have minimum output voltage ripple to ensure stable operation of the converter.

The interleaving operation of three converter phases results in a greatly reduced output voltage ripple for the proposed TPIBC. The ripples have a 120° phase shift and almost cancel each other out for the ripple components of individual inductors. This means that the output current from this combination is smoother and the voltage drop across the output capacitor is less. The output voltage ripple can be expressed as: $V_o = \frac{\Delta i_L}{8Cf_s}$

Where Δi_L inductor ripple current, in which C represents the value of the output capacitor and fs refers to the switching frequency. During normal operating condition, the ripple frequency becomes three times the switching frequency; hence voltage ripple will be lower. However, under the case of one-phase fault, ripple cancellation becomes difficult, making the voltage ripple higher.

4.8 Advantages and Limitations of TPIBC

In addition to several benefits offered by multi-phase converters compared to other converters, there are more specific advantages possessed by TPIBC compared to traditional single-phase buck converters. One of the advantages of TPIBC is associated with the ability of the converter to produce much lower current ripple due to 120°. phase shift of its operation. The decrease in ripple not only improves the output voltage quality but also allows designing less bulky filter devices. Besides, better current balancing among the phases results in lower heat dissipation of semiconductors and inductors. Load currents become evenly distributed and the efficiency and power

capability of the power converter become higher. In addition, the multi-phase configuration ensures the reliability of the power converter, which is capable of working fault-tolerant in case of failure of one phase.

Even with these benefits and some drawbacks to TPIBC still exists: Multiple gate driver circuits, current sensors, switching devices are necessary for the converter system, which raises the system complexity and implementation cost. It is essential to have an accurate current control at the present time to prevent any imbalance in current distribution between phases. Converter performance can also be impacted by mismatches and parasitic resistances. Furthermore, under faulty operating conditions, the ripple gets worse and extra pressure are added to the still healthy phases.

CHAPTER 5

CONTROLLER DESIGN FOR THE PROPOSED TPIBC

5.1 Introduction

The design of the controller is an important parameter in enhancing the performance and stability of the Three Phase Interleaved Buck Converter (TPIBC). For high current direct currents (DC) applications like hydrogen electrolyzers, renewable energy systems, battery charging systems and electric vehicles, correct control of output voltage and current sharing among phases of a converter is vital for reliable operation. Considering the multiphase structure of TPIBC, it is necessary to take into account the differences in the current distribution, which can be caused by mismatches in the components, parasitic resistances, switching delays, and faulty conditions. Thus, a desirable approach towards a control strategy is to plan for balancing the system in both health and fault situations.

This chapter introduces Modeling and implementation of the designed controller for the proposed TPIBC system. The controller features a design aimed at maintaining stable output voltage, enhancing dynamic performance, minimizing ripple, and providing equal-current sharing between converter stages. A PI based Average Current Sharing (ACS) control technique is used to reduce the current imbalance to the converter and improve its reliability. The chapter also discusses PWM generation, the feedback control loop, current-balancing methodology, and fault-tolerant control operation. Furthermore, the performance of the proposed controller under one-phase fault of the power supply is analyzed to check the efficacy of the proposed controller in keeping the converter stable and deliver continuous power while various faults have been occurred.

5.2 Need for Current Balancing

Controller Designing is one of the major parameters that play an important role in improving the performance of the TPIBC. In DC applications such as Hydrogen Electrolyzers, Renewable Energy Systems, Battery Charging Systems, and Electric Vehicles where the current level is higher, the control of the output voltage and current sharing among various phases in a converter becomes important for proper functioning of the circuitry. Since TPIBC is a multistage converter, it is mandatory to consider the variations in the current sharing due to component mismatch, parasitic resistance,

switching delays, and faults. Hence, a better idea would be to adopt a strategy where balance can be maintained in healthy as well as fault cases.

Consequences of Uneven Current Sharing, It can be seen that uneven current sharing will negatively affect the efficiency to compensate for ripple which is one of the main advantages of using interleaved converters. With the increase in the current density in each phase, there comes an increase in power loss due to power dissipation and aging of the components utilized. It is crucial that a suitable approach to current balancing in each phase is implemented. For example, ACS is a good approach for achieving reliable system operation.

5.3 Control Strategies

5.3.1 Average Current Sharing (ACS) Technique

Average Current Sharing (ACS) is one of the widely adopted control techniques for achieving equal current distribution in multiphase DC-DC converters. In a TPIBC, current balancing becomes essential because practical systems contain parasitic resistances, component mismatches, switching delays, and thermal variations that produce unequal current distribution among converter phases. The ACS technique minimizes these current mismatches by continuously monitoring individual phase currents and generating correction signals for balancing the converter operation.

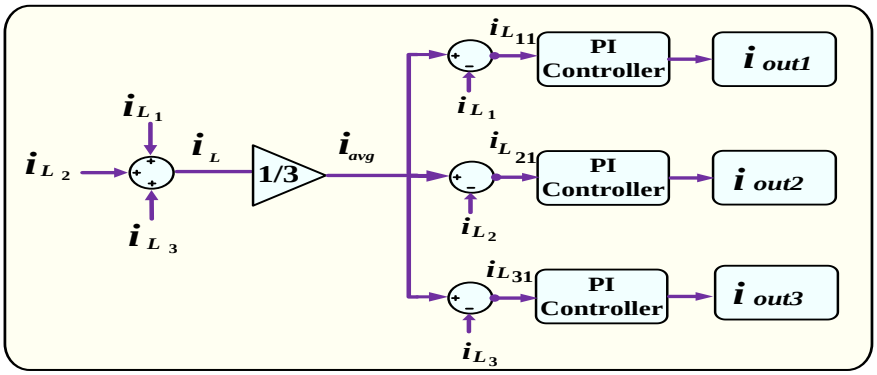

Fig.5.1. Current control of TPIBC for phase current balance in current control mode

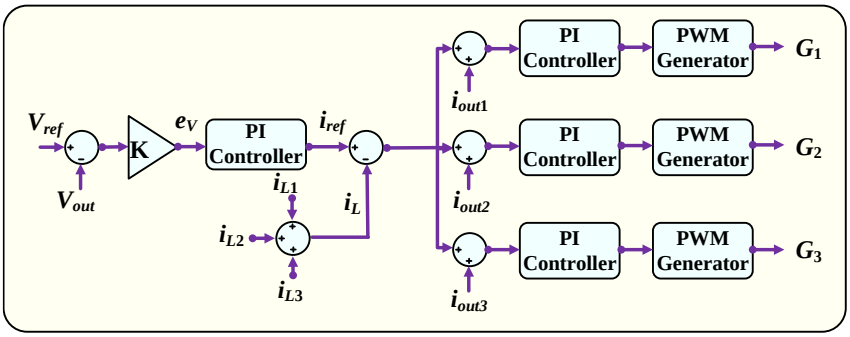

Fig. 5.2. Closed-loop control of TPIBC with phase current balance in voltage control mode.

In the ACS technique, the currents of all converter phases are measured and used to calculate an average reference current. For the proposed three-phase converter, the average current is obtained as:

$$i_{avg} = \left(i_{L1} + i_{L2} + i_{L3}\right)/3 \tag{5.1}$$

$$e_k = i_{avg} - i_{Lk} \tag{5.2}$$

The difference between the average current and each phase current generates current error signals:

Phase-1 current error: $e_{i1} = i_{avg} - i_{L1}$, Phase-2 current error: $e_{i2} = i_{avg} - i_{L2}$, Phase-3 current error: $e_{i3} = i_{avg} - i_{L3}$,Where e_k represents the current-sharing error of phase *k*. A proportional–integral (PI) compensator acting on e_k produces a small duty-cycle correction ΔD_k which is superimposed on the nominal duty command from the per-phase current controller. This adjustment drives each phase current to follow the common average, ensuring balanced current distribution under non-ideal and dynamic conditions. [14]

The overall control structure employs a three-loop structure.

1. *Outer voltage loop:* regulates the output voltage V_o by comparing it with a reference V_{ref}; the resulting error $e_V = V_{ref} - V_o$ is processed by a voltage-loop PI to generate the total reference current I_{ref}.
2. *Inner current loops:* each phase employs a fast PI current controller that tracks its reference $i_{ref,k} = I_{ref}/3$.
3. *Intermediate ACS balancing loop:* operates at a mid-speed bandwidth to equalize phase currents. Its PI compensator injects duty-cycle

corrections ΔD_k to minimize e_k that ΔD_k is defined at [6] and k is a phase inductor current in TPIBC (where k=1, 2, 3) also, D_{base} is an initial value of duty ratio for K^{th} phase in that duty applied ΔD_k to get ACS technique.

Hence, the final duty ratio is:

$$D_k = D_{\text{base},k} + \Delta D_k \tag{5.3}$$

For stable operation, loop bandwidths follow structure

$$f_{current} >> f_{balancer} >> f_{voltage} \tag{5.4}$$

Current loop bandwidth is one-tenth of the switching frequency, the balancing loop one-fifth of that and the voltage loop one-fifth of the balancer's bandwidth. Bandwidth shows how quickly the control loops implement adjust with your TPIBC to power supply. Clamp final duty cycle: (Typical limits: $D_{min} = 0.05$, $D_{max} = 0.95$).

Implementations of all phase currents are sampled synchronously within each PWM cycle to avoid ripple. The algorithm computes i_{avg}, updates both current-loop and balancing-loop PI regulators with Implement saturation limits on ΔD_k to avoid over modulation (loss of control, excessive ripple or thermal stress) or shoot-through (simultaneous conduction of high-side and low-side switches) and limits the resultant duty within the permissible modulation range [21]. Fig. 4. Shows the overview of the system and how the Current control of TPIBC for phase current balance in current control mod of system helps in changing and adjusting the phase of the legs in ideal conditions.

Compared to basic voltage and current loop control, ACS introduces an additional balancing loop that ensures uniform current sharing, ACS detects these mismatches directly (measures per-phase currents), forms e_k, and corrects duties to remove steady-state imbalance [15]. Tune PI by Modeling output filter and adjusting gains. Parasitic effects, such as ESR, may require modifications to the tuning parameters. It actively compensates parasitic-caused steady errors that simple fixed loops cannot eliminate reliably and ACS method measures per-phase currents, computes arithmetic average, and forces each phase to track the average, which is direct and accurate. Its primary benefits are robustness, accuracy, and simplicity; its drawbacks include the requirement for accurate per-phase current sensing and appropriate bandwidth separation to prevent interconnected loop interaction [7] [14].

In addition to the existing voltage and current control, the ACS approach incorporates

a feedback loop in the voltage/current control scheme. While simple control allows for an adequate current-sharing mechanism when the components are identical, ACS is capable of achieving accurate current balancing regardless of whether the converters match. It relies on phase current sensing and PI-based duty correction, yet makes a system more complex and expensive in comparison with simple control; however, it guarantees better stability and better fault tolerance, transient response, and steady-state performance provided that the control loop bandwidth is carefully selected to avoid interference between loops.

Each of the error signals is processed using the PI controllers in order to produce a signal that would affect duty cycle adjustment. As a result, converters operating with lower currents will have a larger duty ratio, whereas those running with excess current will have their duty ratios decreased.

A number of advantages can be pointed out with regard to ACS. First, it allows for more efficient current distribution within the converter. Moreover, ACS reduces thermal stress of each of the phases due to ripple current reduction, and also enables redistributing current in case of a phase failure.

Control structure for the designed TPIBC is hierarchical and comprises multiple feedback loops to ensure that the desired output voltage is achieved while also achieving equal sharing of currents in different phases of the converter. The control loop basically includes the following three main loops:

5.3.2 Outer Voltage Loop

The outer voltage loop is responsible for regulating the converter output voltage to the desired reference value. The measured output voltage is continuously compared with the reference voltage to generate voltage error.

Voltage error: $e_v = V_{ref} - V_o$,The generated error signal is processed through a PI controller to produce the reference current signal: $i_{ref} = PI(e_v)$

The outer voltage loop operates comparatively slower than current loops because output voltage dynamics change slowly. The primary objective of this loop is to maintain stable output voltage despite load variations and fault conditions.

5.3.3 Inner Current Loop

The inner current loop provides fast dynamic control of converter phase

currents. The reference current obtained from the outer voltage loop is distributed among converter phases and compared with measured phase currents.

Reference current for each phase: $i_{avg} = \frac{i_{ref}}{3}$

Each current loop generates error signals: $e_{c1} = i_{avg} - i_{L1}$, $e_{c2} = i_{avg} - i_{L2}$, $e_{c3} = i_{avg} - i_{L3}$

These errors are processed using PI controllers to generate duty cycle commands for PWM generation. Since current dynamics are faster than voltage dynamics, the inner current loop ensures rapid response during transient conditions.

5.3.4 ACS Balancing Loop:

The ACS balancing loop continuously monitors phase currents and compensates for current mismatch caused by non-ideal effects. The average current is computed from all converter phases and compared with individual phase currents.

Average current: $i_{avg} = \frac{i_{L1} + i_{L2} + i_{L3}}{3}$ (5.5)

Balancing error: $\Delta i_k = i_{avg} - i_{Lk}$ (5.6)

Where: k=1,2,3

The feedback signals produced by the balance controller will make sure that there is proper modulation of the PWM duty cycle and proper distribution of the currents. If there are any fault conditions, then the ACS control algorithm will help share the current between healthy phase legs.

5.4 Duty analysis of using ACS balancing

A TPIBC with realistic inductor parasitic resistance exhibits distinct behaviors depending on the commanded duty ratio relative to the phase shift (T/3): non-overlap (D<1/3) (D=0.25), boundary (D=1/3) (D=0.33) and overlap (D>1/3) (D=0.41). Notation used herein: per-phase inductor currents i_{L1}, i_{L2}, i_{L3}; total load current I_L = i_{L1}+i_{L2}+i_{L3}; instantaneous average i_{avg} = (i_{L1}+i_{L2}+i_{L3})/3; and ACS residuals i_{L11} = i_{avg} − i_{L1}, i_{L21} = i_{avg} − i_{L2}, i_{L31} = i_{avg} − i_{L3}. Under ideal (zero- inductor parasitic resistance) conditions, identical duty commands produce equal phase currents (≈I_L/3) and phase-shifted ripple that cancels in sum. With non-zero and mismatched (R_{L1}, R_{L2}, R_{L3}), however, the relation between duty and phase current is biased by series resistance and steady current imbalance appears phases with lower inductor parasitic resistance carry higher share.

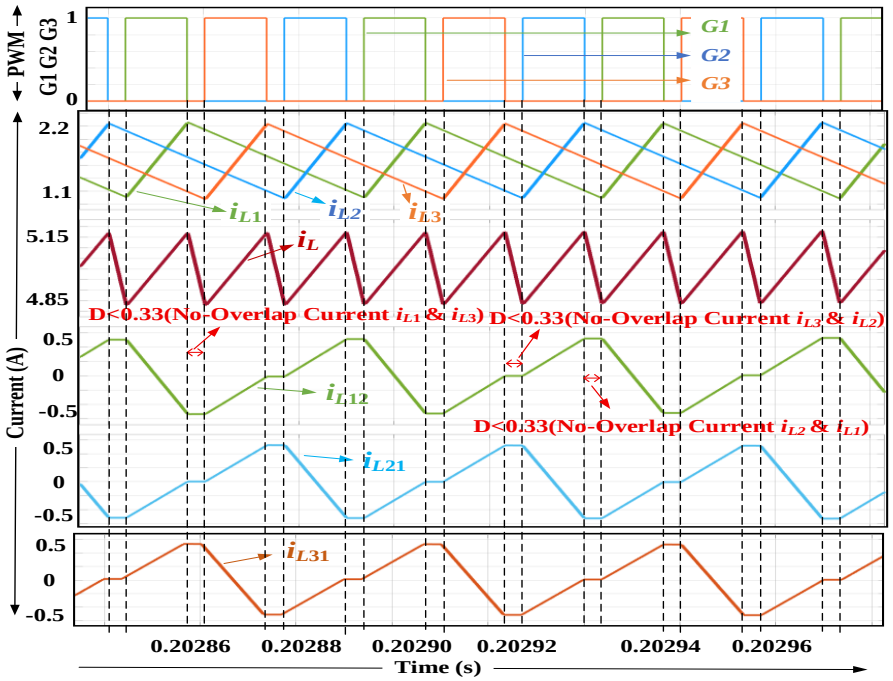

Figure 5.3. FTTPIB converter with balance current under normal (healthy) at condition D=0.25 (D<1/3).

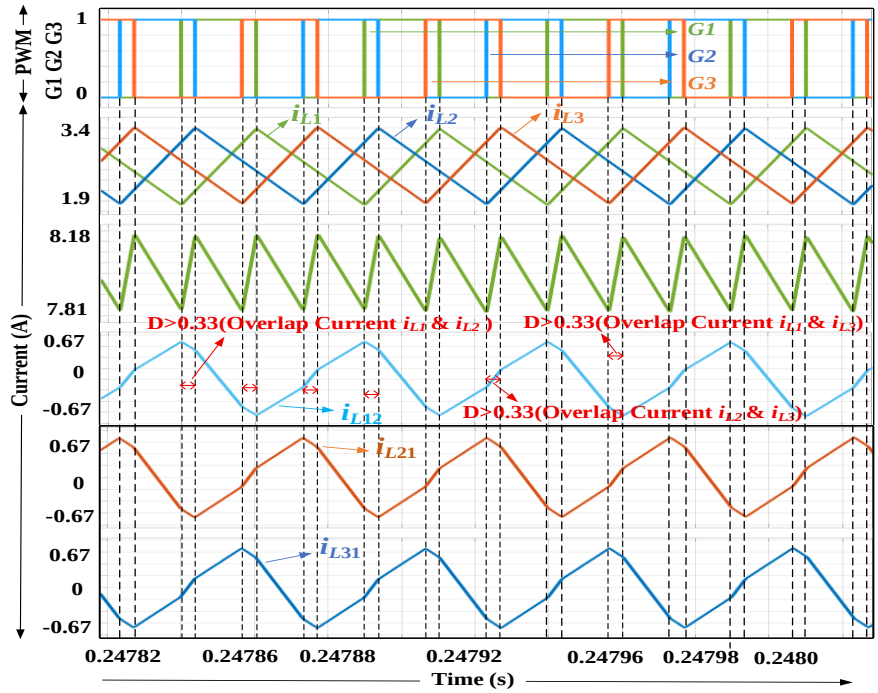

Figure 5.4 FTTPIB converter with balance current under normal (healthy) at condition D=0.415 (D>1/3).

In non-overlap (*D<1/3)*, on-PWM does not coincide, so it is measured using synchronous sampling and corrected by an Average current sharing (ACS) balancer that computes i_{avg}, forms per-phase errors, and applies small duty ΔD_k shown in Fig.

4, and the impact is shown in Fig. 6. Automatically it senses the required need and adjusts duty accordingly for the controller to maintain phase current balance, and we get some flat current i_{L12}, i_{L21}, and i_{L31} at some points like edges where PWM signals do not overlap; that condition is shown in Fig. 6. At the boundary (D=1/3) the system is sensitive to dead-time and timing edges: tiny overlaps or gaps can produce sampling bias, so precise timing and end-of-on sampling are required. In this condition we get proper balance current in current control mode with ACS. In the overlap regime (D>1/3), phase can lead to increased RMS currents; switching losses due to transient phase-to-phase circulating currents are shown in Fig. 7. As is shown in Fig. 7, we see that there is an irregular waveform current i_{L12}, i_{L21}, and i_{L31} generated at certain points, especially at overlapping points of the PWM signal generation.

The major problems encountered include existing imbalance, circulation currents, which may lead to additional faults. The measures to be taken for fault prevention include nesting the control system, sampling simultaneously, controlling the duty cycle change (ΔDk), and ensuring that ACS bandwidth is much less than the current-loop bandwidth [15]. Open-circuit (OC) fault occurs due to increasing phase and balancer saturation.

5.5 Control Design and Comparative Analysis of TPIBC

The design process of the controller for TPIBC was conducted based on the small-signal transfer functions which were derived from the state-space average model of the circuit. The controller was designed using two loops, which were referred to as voltage control loop and current control loop. In other words, the former controls the output voltage while the latter controls the inductor currents.

The small-signal control-to-output transfer function was used to represent the relationship between duty cycle perturbations and output voltage variations. Similarly, the current-loop transfer function was utilized to describe the relationship between duty-cycle variation and inductor current response. These transfer functions were obtained from the averaged state-space model using Laplace transformation techniques.

For controller implementation, proportional-integral (PI) controllers were selected due to their simple implementation, ease of tuning, and ability to eliminate steady-state

error. The PI controller can be expressed as: $[G_c(s) = K_p + \frac{K_i}{s}]$; Where: Kp represents proportional gain and Ki represents integral gain.

Initially, manually tuned controller gains were selected using an iterative tuning procedure. The voltage loop employed manually selected gains: $Kp = 0.1$, $Ki = 1000$

Similarly, for current-loop control: $Kp = 0.1$, $Ki = 2000$ .These manually selected gains were used as reference values for evaluating controller performance.

Subsequently, automatic controller tuning was performed using transfer-function-based tuning techniques. The transfer function of the converter was used to determine controller parameters that satisfy stability and dynamic performance requirements. Automatic tuning provides controller gains by considering system bandwidth, crossover frequency, and phase margin constraints.

The obtained controllers were incorporated into a closed-loop configuration using unity feedback architecture. The closed-loop transfer function can be expressed as: $[T(s) = \frac{G_c(s)G(s)}{1 + G_c(s)G(s)}]$; Where: [$G(s)$] represents the plant transfer function and [$Gc(s)$] represents the controller transfer function.

To evaluate controller performance, both manually tuned controllers and transfer-function-based controllers were analyzed using transient and frequency-domain performance indices.

Transient analysis included:

- Rise time
- Settling time
- Percentage overshoot
- Steady-state behavior

Frequency-domain analysis included:

- Gain margin
- Phase margin

- Bandwidth
- Stability margins

The closed-loop step response was used to evaluate transient characteristics, while Bode analysis was performed to examine frequency response characteristics and system robustness. Pole-zero analysis was used in addition to test the stability of the system as well as analyze the effect of moving poles because of controller design.

Comparison of the manually tuned control gains to the gains calculated based on transfer functions will help evaluate the efficiency of the controller and understand how the parameters affect the system dynamics. Such comparison is particularly important for higher-order converters such as the three-phase interleaved buck converter because multiple energy storage elements significantly influence system dynamics.

Overall, the controller design methodology provides systematic evaluation of converter stability, transient performance, and robustness while ensuring adequate regulation of output voltage and current sharing among converter phases.

(Kpv_{auto} = 0, Kiv_{auto} =55.9661, Kpi_{auto} = 0.0019, Kii_{auto}=2.9683)

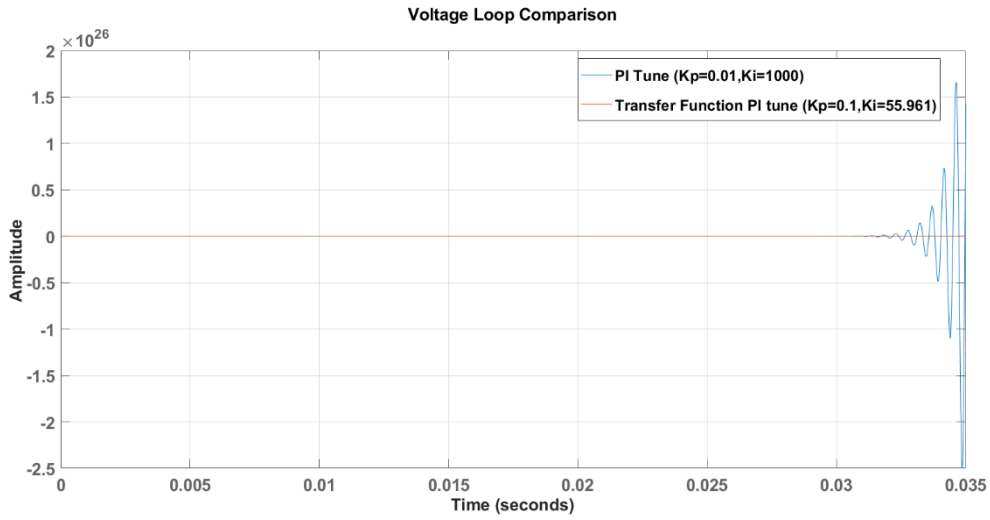

Figure 5.5 Closed-Loop Performance Comparison of Voltage Loop Controllers for TPIBC

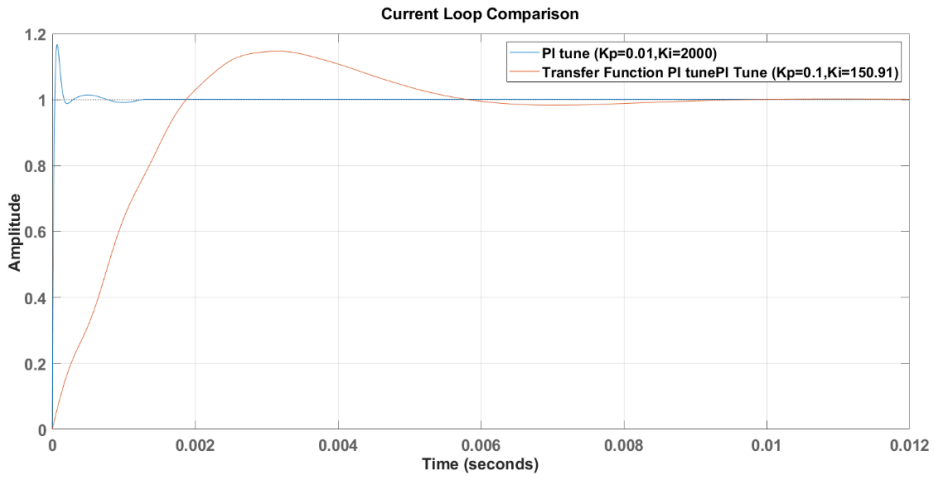

Figure 5.6 Closed-Loop Performance Comparison of Current Loop Controllers for TPIBC

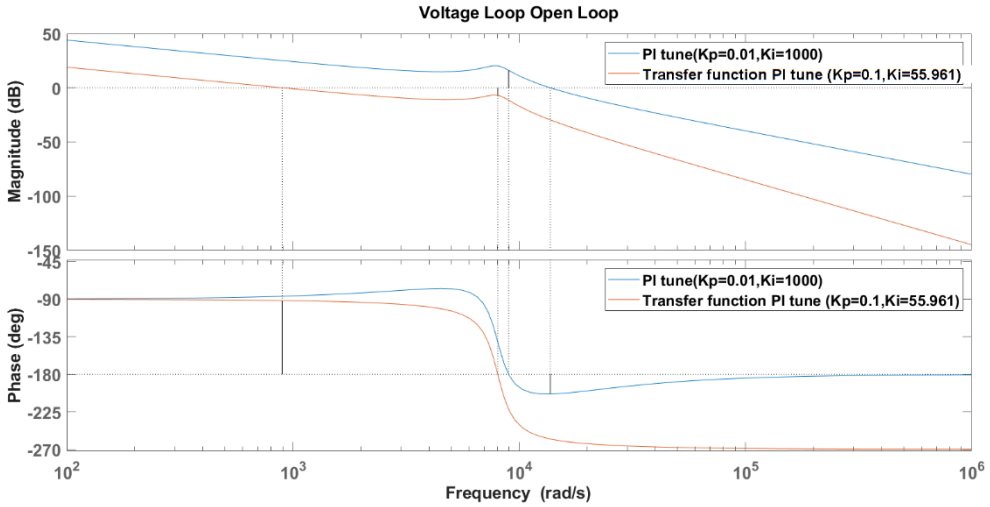

Figure 5.7 Open-Loop Frequency Response Analysis of Voltage Loop Controllers

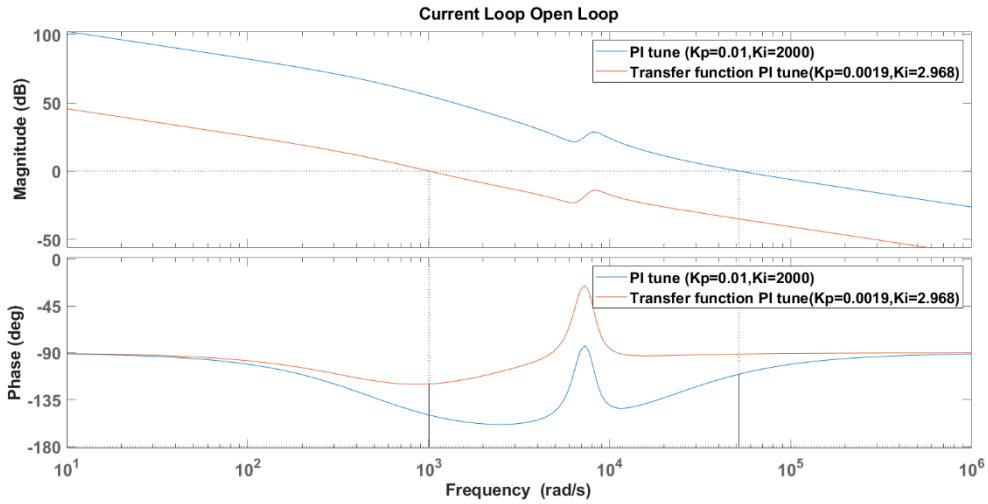

Figure 5.8 Open-Loop Frequency Response Analysis of Current Loop Controllers

How K_p and K_i were obtained

Tuning methodology as:

Step 1: Obtain transfer function:

$$G(s)$$

Step 2: Select crossover frequency:

Voltage loop:

$$f_c \approx \frac{f_s}{10}$$

Current loop:

$$fc > Voltage\,Loop\,Bandwidth$$

Step 3: Compute plant gain at crossover:

$$K_p = \frac{1}{|G(j\omega_c)|}$$

Step 4: Place controller zero:

$$\omega_z = \frac{K_i}{K_p}$$

Step 5: Calculate:

$$K_i = K_p \omega_z$$

Thus, controller gains are selected based on converter dynamics rather than trial-and-error tuning.

This explanation matches the behaviour visible in your graphs:

- Voltage trial tuning → unstable oscillatory response

- Transfer-function voltage tuning → stable response
- Current trial tuning → higher bandwidth but lower robustness
- Transfer-function current tuning → improved damping and stability

Table II 5.1 Comparison of PI Controller Tuning Methods for TPIBC

PERFORMANCE PARAMETER	TRIAL METHOD	FREQUENCY RESPONSE METHOD	PIDTUNE METHOD
(K_p)	0.1000	0.0946	0.0000
(K_i)	1000	118.8878	55.9661
Rise Time (s)	NaN	0.000124	0.002465
Settling Time (s)	NaN	0.005962	0.004348
Overshoot ($\%$)	NaN	18.7327	0.0785
Phase Margin (deg)	-23.7113	9.1577	88.4014
Gain Margin (dB)	-16.1389	∞	6.9868
Bandwidth (rad/s)	18167.1400	1548.0055	920.2853
Closed Loop Stability	Unstable	Marginally Stable	Stable
Steady-State Error	Cannot Converge	Small	Very Small
Controller Nature	Aggressive Tuning	Moderate Tuning	Integral Dominant

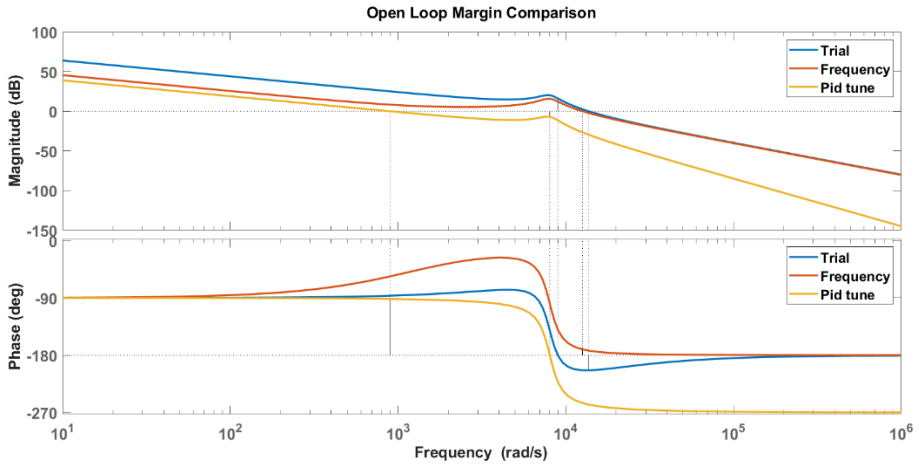

Figure 5.9 Open-Loop Margin Comparison of PI Controller Tuning Methods

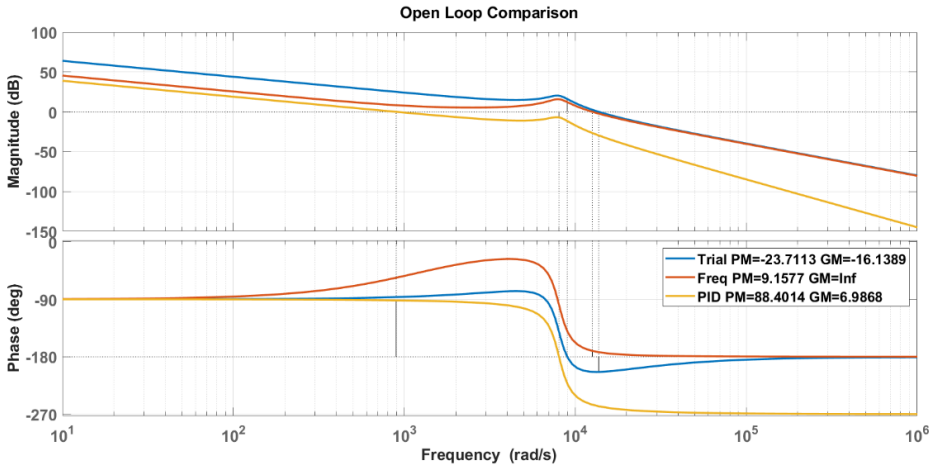

Figure 5.10 Open-Loop Frequency Response Comparison Using Different PI Tuning Techniques

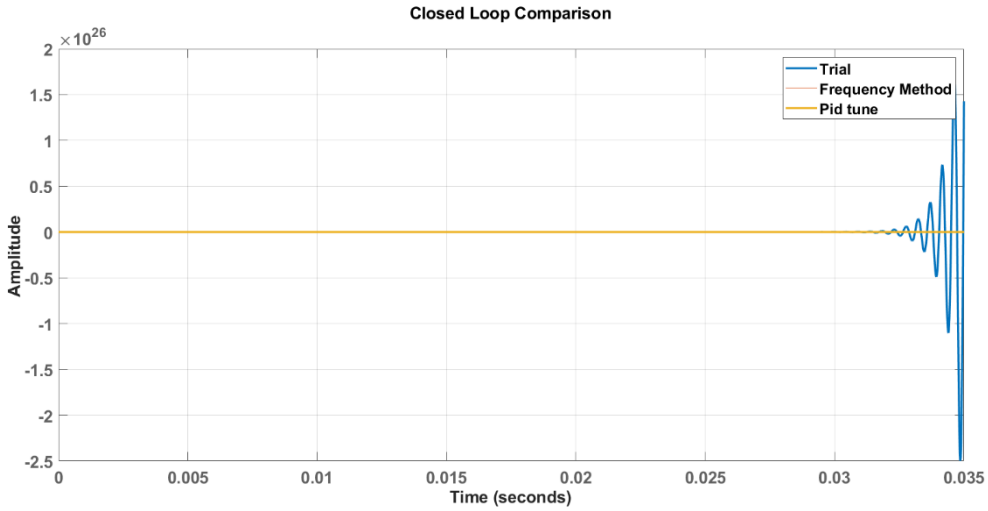

Figure 5.11 Closed-Loop Dynamic Response Comparison of Controller Tuning Methods

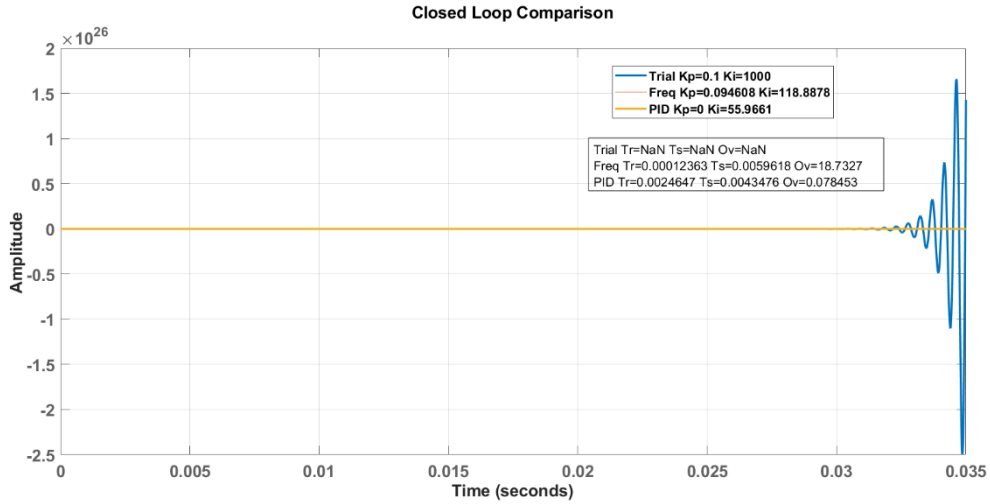

Figure 5.12 Closed-Loop Performance Comparison Using Different PI Tuning Techniques

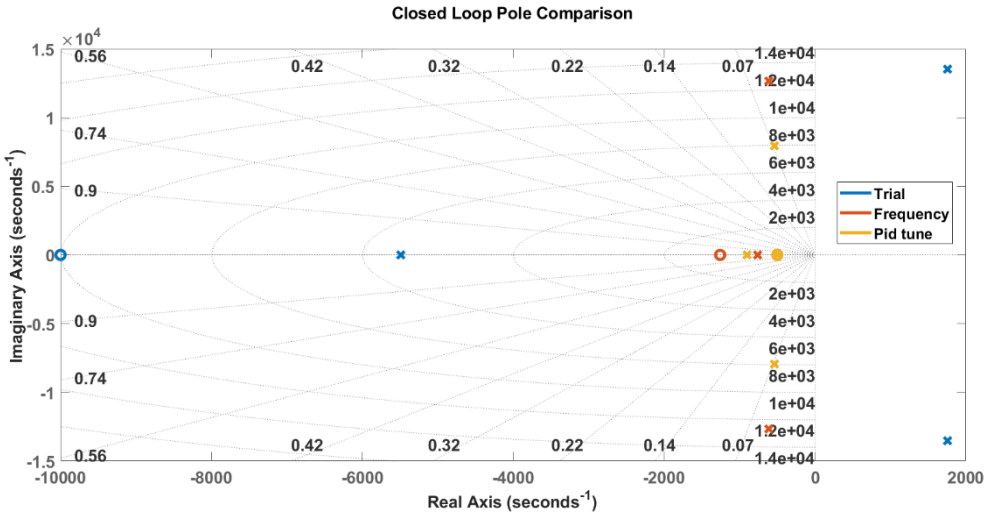

Figure 5.13 Closed-Loop Pole Distribution Comparison for Controller Stability Analysis

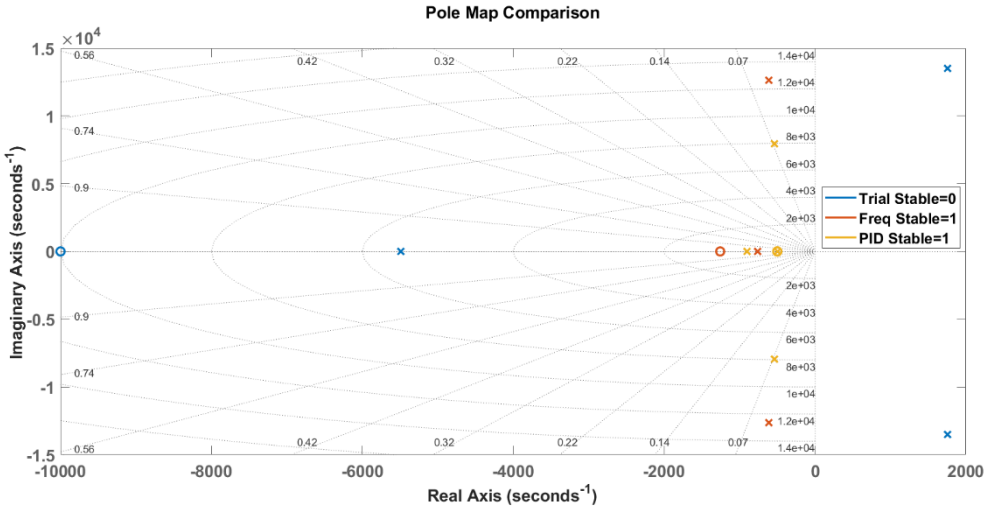

Figure 5.14 Pole Map Comparison of Different PI Controller Tuning Methods

CHAPTER 6
RESULTS AND DISCUSSION

6.1 System Parameters

The recommended fault-tolerant control mechanism has been modelled using MATLAB/SIMULINK. Table I lists the parameters that were utilized to simulate the system. The inductor current waveform for each of the legs for D< 0.33 (non-overlapping) is shown in Fig. 6.1. Moreover, the PI control is used to achieve equitable current distribution across legs. Fig. 6.1. Manifests an open-circuit switch fault, which is simulated in the converter's first phase at time t = 0.3s. The gains of the PI controller are changed in less than one switching cycle, or less than 20 µs, upon the occurrence of the fault, while the current through the faulty leg becomes zero. It also shows the effectiveness of the digitally implemented PI control.

Table III 6.1 System Parameters

Parameter Name	Value
Power Ratings	3 kW
Per Phase Inductance (L_1, L_2, L_3)	1 mH
Switching Frequency	20 kHz
Output Capacitance	100 µF
Input Voltage	100-120 V
Nominal Voltage of Battery	55-75V

6.2 Operation under Normal Condition

A TPIBC comprises three buck legs with a 120° phase shift between their outputs, designed to balance inductor currents with parasitic resistance and cancel high-frequency components in Fig. 6.1 A TPIBC in a normal operation features balanced current sharing, with each phase carrying roughly one-third of the total output current, mitigated by control systems against minor imbalances. The 120° phase shift of switching ripples across the three phase results in cancellation at the output, TPIBC have lower output voltage ripple than single-phase systems. This interleaving effect reduces output ripple and allows for smaller filtering components. Interleaved multi-phase buck converters, particularly three-phase designs, surpass single-phase systems by reducing conduction losses leading to lower per-phase current and diminished i^2R loss. Moreover, such an interlacing technique improves dynamic response and stability

through the increase in effective dynamics due to damping, resulting in superior filtering and reduction in ripple, thus improving the control loop. In this way, normal three-phase operation gives a smooth output with less ripple, equal current sharing, higher efficiency, and stability

6.3 Operation under Open-Circuit Switch Faulty Condition

In this case, a method is being presented for the detection of faults in real-time and reconfiguration for keeping the DC source feed uninterrupted by identifying the type of fault in a TPIBC, which acts as a supply for electrolyzer. There are basically two types of faults; one is open-circuit fault, where the MOSFET, diodes, or inductor windings fail due to opening, and the other is the short-circuit fault, where the switch or diode fails due to shorting.

Comparative logic and per-phase current sensing are used to implement fault detection. Every phase current is continuously compared to the predetermined thresholds and the predicted average by the scheme; persistent deviations from these limits (lasting longer than a brief persistence timer to few switching cycles) result in a fault declaration.

A fault in one leg of a three-phase system, such as an open-circuit or short-circuit failure of a switch or diode, breaks system symmetry. In such scenarios, one leg is rendered inoperable, forcing two legs to bear the entire load in Fig 8. So current sharing in open-switch fault and short-circuit fault: If a high-side or low-side switch in leg 1 is stuck open, phase 1 ceases current supply, causing its inductor current to zero. A control loop will compensate by increasing the duty cycle in the remaining phases (2 and 3) to maintain constant output current. Consequently, phases 2 and 3 will each need to handle approximately half the load instead of one-third, resulting in a roughly 50% increase in their inductor currents in Fig 6.1. i_{L1} falls to zero, while i_{L2} and i_{L3} rise. In TPIBC this makes the phase shift between the two active phases effectively 180° in Fig. 8 under post fault steady state condition.

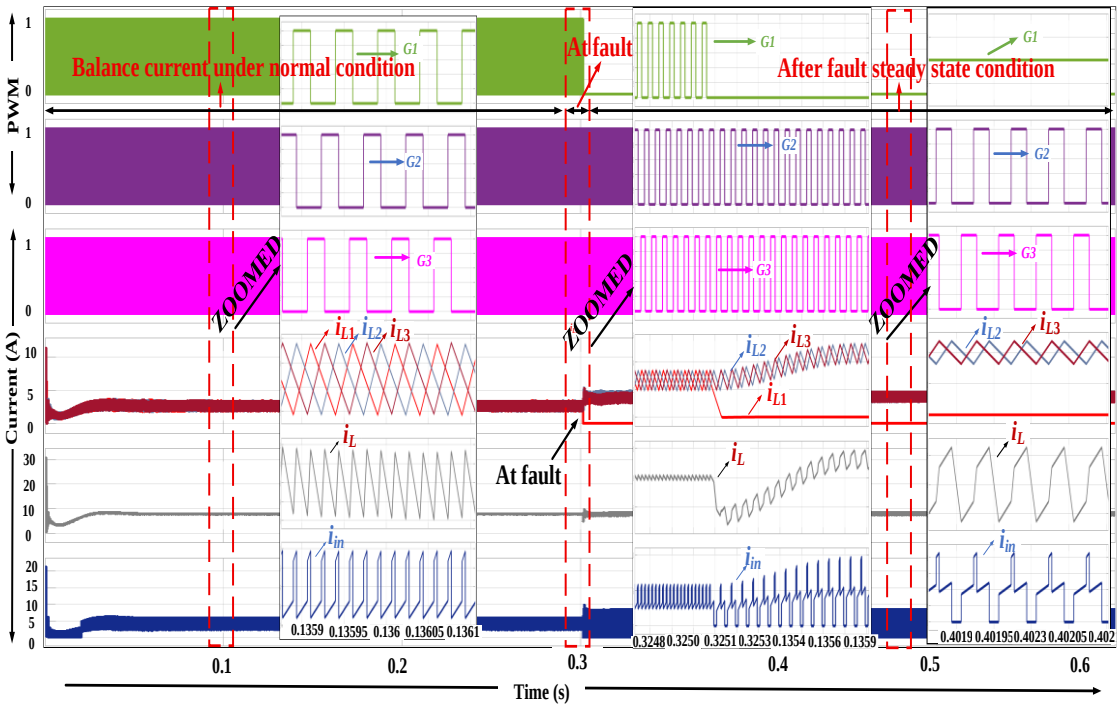

Figure 6.1 FTTPIB converter with balance current under normal (healthy) condition, occurrence of fault, Post fault steady state condition

A shorted switch, such as a MOSFET failing ON, in one leg of a TPIBC is considered a severe fault that can cause input/output shorts and trigger protective shutdowns. The analysis will examine the system status after fault detection. One result of having only one active phase is that ripple cancellation does not occur anymore because the two out-of-phase currents do not cancel the fundamental switching waveform anymore.

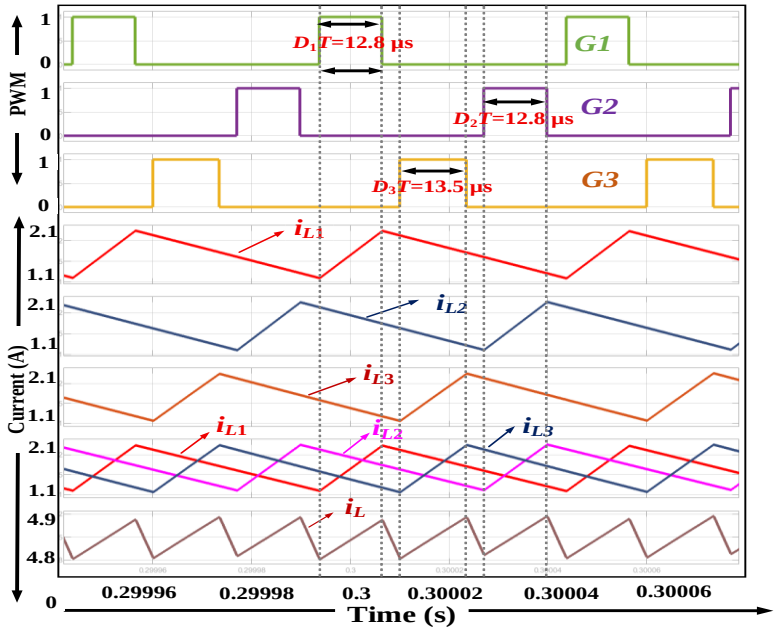

Figure 6.2 FTTPIB converter with balance current at condition one leg higher parasitic resistance.

In fig. 6.2. FTTPIB has a tolerance of one leg resistance so that one leg is considered as having higher parasitic resistance, like R_{L3}=1 ohm in i_{L3} phase so in that condition i_{L1} and i_{L2} have the same switching period time (D_1T *and* D_2T=12.8μs) but i_{L3} shows a greater switching time duration (D_3T=13.5μs) to get balanced 3-phase inductor current in FTTPIB. This results in a substantial increase in output current and voltage ripple, with the dominant ripple frequency potentially shifting from f_s to $2f_s$, significantly amplifying ripple amplitude. The output voltage and current consequently become more distorted, exhibiting higher-frequency ripple components and possible shifts in the DC baseline in Fig 6.2.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

TPIBC works well in high-power DC-DC conversions, minimizing ripple currents in the output and boosting the apparent switching frequency via carrier interleaving. Accurate simulations of both dynamic and steady-state operation were realized through extensive Modeling and Analysis of the switching states. PWM controllers proposed for voltage and current mode control guarantee regulated voltage operation and fast transient response. In particular, a dual-loop control in a voltage mode yields similar performance as that of single-loop control in a current mode. This circuit is appropriate for use in EV chargers, renewable energy converters, and batteries. High-efficiency and balanced currents characterize the converter. The fault tolerance aspect enables sustained supply at lower output power on occurrence of single leg failure, which is essential in ensuring reliability.

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