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KURMANA PRANEETH 2025

Design and Analysis of a Cascaded High-Gain Boost-Buck Converter for Battery Charging Applications

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Power Electronics & Systems

by

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CANDIDATE'S DECLARATION

I, **Kurmana Praneeth (2K24/PES/16)**, student of M. Tech (Power Electronics &Systems), here by declare that the dissertation entitled **"Design and Analysis of a Cascaded High-Gain Boost-Buck Converter for Battery Charging Applications"** in partial fulfillment of the requirement for the award of the degree of Master of Technology, submitted in the Department of Electrical Engineering Department, Delhi Technological University, is an authentic record of my own work carried out during the period from 08/2024 to 12/2025 under the supervision of **Dr. Sudarshan K. Valluru**

The matter presented in the dissertation has not been submitted by me for the award of any other degree of this or any other Institute.

Kurmana Praneeth

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CERTIFICATE

I hereby certify that the project Dissertation titled **"Design and Analysis of a Cascaded High-Gain Boost-Buck Converter for Battery Charging Applications"** which is submitted by **Kurmana Praneeth (2K24/PES/16),** in partial fulfilment of the requirement for the award of the degree of Master of Technology, submitted in the Department of Electrical Engineering Department, Delhi Technological University,is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

This project presents detailed analysis on the design, analysis and regulation of two-stage dc-dc conversion system intended for application in energy harvesting and high power battery charging system. The developed system utilizes High-Gain Boost converter and subsequently the Buck converter that efficiently converts the low voltage dc power generated from sources like PV or fuel cells and produces regulated dc outputs that can be utilized for charging applications. The primary objective of the proposed work is to achieve high voltage gain, maintain a constant and stable DC-Link voltage, and utilize this DC-Link output as the input to a cascaded buck converter for efficient battery charging applications. The thesis commences with the execution of a non-isolated, non-coupled inductor-based high-gain DC-DC boost converter topology intended to increase variable low-input DC voltage to a stable 300 V DC-link. The novel boost converter employs two switches controlled by a single Pulse Width Modulator (PWM), this configuration makes the converter a compact economical and lightweight design with an uncomplicated control architecture. The converter is engineered to deliver a significant voltage gain at reduced duty cycles while ensuring minimal voltage stress across each switch during switching. Its operation facilitates significant voltage amplification, making it highly suitable for the use in renewable energy systems where efficient low-to-high voltage conversion is required. The novel boost converter exhibits an enhanced gain characteristics and also improved efficiency compared to the conventional boost converter, thus improving overall system reliability and performance. Following the boost conversion process, the regulated 300V DC-link works as the input to the Buck converter which will buck the DC-link voltage to a regulated 48V level suitable for the 1kW battery charger output ensuring accuracy of voltage and current at the output. The objective of this step is to provide safe and consistent charging operation for varied loads and varying sources. The boost buck topology provides the most effective conversion and regulation process for modern day charging facilities, DC microgrids and renewable energy storage systems. Controller designs for both converters have been developed by employing PI controller based feedback approach to stabilize the DC-Link voltage in case of Boost converter and to provide a regulated output voltage and current in case of the Buck converter. The control design provides a very good dynamic performance, high efficiency operation, high voltage gain, minimum switch stresses and resilience under input and load variation. By cascading these two stages the system would attain high power conversion and energy transfer capabilities. The current research work focuses on developing technically advanced converter topology by combining a high voltage gain process and a high efficiency conversion technique for renewable energy applications,with the efficacy of the given converter system validated through comprehensive MATLAB/Simulink simulation study.

TABLE OF CONTENTS

List of Figures

List of Tables

LIST OF ABBREVIATIONS

Abbreviation	Full Form
DC	Direct Current
DC–DC	Direct Current to Direct Current
PV	Photovoltaic
EV	Electric Vehicle
EMI	Electromagnetic Interference
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
PWM	Pulse Width Modulation
KVL	Kirchhoff's Voltage Law
LC	Inductor-Capacitor
PI	Proportional-Integral (controller)
MPPT	Maximum Power Point Tracking
QBC	Quadratic Boost Converter
NQBC	Fifth-Order Quadratic Boost Converter

LIST OF SYMBOLS

Symbol	Meaning
V_{c1}	Voltage across capacitor C1
V_{c2}	Voltage across capacitor C2
V_{c3}	Voltage across capacitor C3
V_{L1}	Voltage across inductor L1
V_{L2}	Voltage across inductor L2
V_o	Output voltage
V_{in}	Input voltage
ΔV_{c1}	Ripple in voltage across capacitor C1
ΔV_{c2}	Ripple in voltage across capacitor C2
ΔV_{c3}	Ripple in voltage across capacitor C3
I_{L1}	Inductor current in L1
I_{L2}	Inductor current in L2
I_{C1}	Capacitor current in C1
I_{C2}	Capacitor current in C2
I_{C3}	Capacitor current in C3
I_0	Output current
D1	Duty cycle of High Gain Boost Converter
D2	Duty cycle of Buck Converter
Fs	Switching frequency

T	Switching period
R	Load resistance
L_1	Inductor L1
L_2	Inductor L2
C_1	Capacitor C1
C_2	Capacitor C2
C_3	Capacitor C3
K_p	Proportional gain
K_i	Integral gain
V_{ref}	Reference voltage
e(t)	Error signal
u(t)	Controller output

CHAPTER 1

INTRODUCTION

High-gain DC-DC converters are a key component of current power electronics systems, especially in applications where low-voltage renewable or distributed energy sources must be converted to significantly higher voltage levels. For most renewable energy technologies, such as photovoltaic (PV) systems and fuel cells, the output voltage is generally low, typically from a few volts to higher levels, and is therefore not suited for medium- and high-power applications. Therefore, high-step-up converters with high efficiency, low power losses, continuous input current, and consistent output-voltage characteristics over a wide range of voltage conversion ratios are required. These converters have been widely employed in renewable energy systems, DC microgrids, robotics, electric vehicles (EVs), and high-voltage DC systems [5], [6]. The output voltage of renewable energy systems, particularly solar PV systems, is strongly dependent on environmental factors such as solar irradiance and temperature. Similarly, the output voltage of fuel cell devices also fluctuates under different load circumstances. Power electronic converters are therefore needed to regulate and boost these low, variable DC voltages to a stable DC-link voltage suitable for downstream converters and energy storage systems [1], [5], [6]. High-gain DC-DC converters are widely used in DC micro-grid applications to maintain the DC-link voltage at the correct level, thereby enhancing overall system stability and power transmission capability [5], [11]. Boost converters are commonly used for their simple structure, low component count, and straightforward control. The steady-state voltage gain is given by where D is the PWM duty cycle, the fraction of each switching period during which the active switch is ON. So, a very high voltage gain can be obtained as the duty cycle approaches unity. However, the typical boost converter's performance degrades drastically at high duty ratios in actual applications, rendering it unsuitable for renewable energy systems with large voltage conversion ratios [4], [5]. The duty cycle is a direct control of how long the switch is on in any switching phase. At high duty cycles, the switch stays ON for a longer duration, this causes the inductor current to increase. As a result, there has been increased stress on the current, more conduction losses, and more heat. The switch also has to handle high-energy transitions. It also puts demands on the heat sink and the gate driver. When the duty ratio reaches 0.8 or 0.9, the parasitic resistance of the passive components starts to affect the converter's performance and efficiency. There is also electromagnetic interference. The voltage gain characteristic can even become saturated. The switch and inductor currents are under significant stress. The switch has to handle

high-energy switching. The duty cycle and inductor current are very important. Hence, increasing the duty ratio does not proportionally improve the voltage gain. On the other hand, operating at lower duty ratios minimizes the switch conduction interval, thereby reducing peak and RMS switch currents, conduction losses, thermal stress, and switching losses. Lower stress on the switches increases the converter's reliability and operating life. It allows the use of semiconductor devices with lower voltage and current ratings, decreasing the overall cost and size of the converter. Hence, recent high-gain converter research aims to achieve high voltage conversion ratios without forcing the converter to operate at unnecessarily high duty cycles. To overcome the constraints of typical boost converters, DC-DC converter topologies are often divided into two categories: isolated and non-isolated converters. Isolated converters use high-frequency transformers to achieve galvanic isolation, but this adds to the converter's size, complexity, cost, and operation [6]–[9]. On the other hand, non-isolated converters have simpler designs, lower cost and smaller size, making them appealing for renewable energy and EV charging applications [7], [9]. The coupled-inductor-based non-isolated converters deliver significant voltage gain at reduced duty ratios. However, the use of linked inductors suffers from leakage inductance, high switch voltage stress, core saturation and low efficiency at high duty cycle. Recent studies have examined non-isolated, non-coupled inductor-based high-gain converter topologies to overcome these problems [10], [24]. To improve voltage gain, efficiency, and component stress, several topologies have been developed, including quadratic boost converters, switched-capacitor structures, switched-inductor arrangements, and interleaved architectures [1], [3], [12]–[25]. Such topologies offer better voltage conversion capabilities, but most require more passive components and complex circuit layouts, thereby increasing converter size and conduction losses [15], [19], [21], [25]. In this project work, a unique non-isolated, non-coupled inductor-based high-gain boost converter is suggested for renewable energy and EV charging applications [12], [13], [14]. The suggested converter has two inductors, three capacitors, three diodes, and two active switches, all operated by a single PWM signal. The topology can achieve significant voltage gain for moderate duty ratios. Also, it keeps lower voltage stress on the switching devices. The adoption of a single PWM signal simplifies the control structure and reduces gate driver requirements, making the converter smaller, cheaper, and lighter. Furthermore, by removing the need for linked inductors, these issues related to leakage inductance and core magnetic saturation will no longer pose problems for converters, thereby enhancing their overall reliability and efficiency. There is sufficient evidence from both experiments and modeling within the literature which supports that the proposed converter will produce a voltage gain of over 12 at a duty ratio of 0.6 while achieving an efficiency between 92.5% and 94.5%, making it suitable for use at both medium and

large scale power levels. The need for very efficient high voltage boost (converters), in addition to proper battery charging through regulated voltage devices, is required since renewable energy resources are very intermittent, as well as requiring batteries (or other energy storage) to provide continuous, uninterrupted power. Batteries are quite popular since they can store a lot of energy and last a long time. However, if the battery is charged in unsatisfactory conditions, it can substantially shorten the battery's life and charging efficiency. Hence, efficient converter-based charging systems with appropriate control mechanisms are needed. The suggested high-gain boost converter is coupled with a cascaded buck converter stage for efficient battery charging. The boost converter produces 300 V at the DC link, which is controlled and used to supply power to the buck converter stage, reducing the voltage and current required to charge a 1 kW battery. Buck converters are used in battery charging systems primarily due to their relatively simple design, low switching losses, high efficiency and excellent voltage regulation. For this reason, buck converters are well-suited for use as medium to high power charging systems. Closed-loop PI controllers will be used to control the operation of both the boost and buck converter stages to ensure the overall system remains stable during operation. The controllers will provide stabilised output voltage, fast transient response, low ripple at the output, and consistent performance of charge delivery for a range of input and load conditions. Because of these characteristics, the proposed cascaded boost-buck converter configuration is an attractive alternative for use in renewable energy-based battery charging systems, DC micro-grids, and EV charging systems due to their high voltage gain, stabilised DC-link regulation and high voltage step-down capability, as well as their ability to provide reliable energy transfer during operation.

1.1 Boost Converter:

A boost converter is one of the most fundamental and widely used DC–DC step-up power converter topologies as shown in fig 1.1. Its primary function is to raise a low-level DC input voltage to a higher DC output voltage, making it essential in systems where sources like photovoltaic (PV) panels, fuel cells, or batteries provide insufficient voltage for the load. The operation of a boost converter relies on controlled energy storage in an inductor during the switch ON period and the release of this stored energy to the output through a diode and capacitor when the switch turns OFF. Because of its simple structure typically consisting of one inductor, one controlled switch, one diode, and an output capacitor the boost converter offers advantages such as low cost, ease of implementation, and compatibility with a wide range of applications. PWM boost

converters that use traditional technology can work in either continuous conduction mode (CCM) or discontinuous conduction mode (DCM). CCM operation is more common because it has less current ripple and is more efficient. But the classical boost converter also has problems at high duty cycles, such as more stress on the switches, electromagnetic interference, and lower efficiency. Also, in CCM, the boost converter has a right-half-plane zero in its control transfer function. This will limits the control bandwidth and also makes it harder to regulate performance. Despite these challenges, boost converters remain a serve as a fundamental foundation for higher-order and advanced step-up topologies. Modern renewable energy systems, portable electronics, electric vehicles (EVs), and DC microgrids make extensive use of boost converters due to their ability to provide regulated high DC voltage from low and variable input sources. Their relevance has continued to grow with the demand for high-efficiency, lightweight, and compact power conversion solutions [11]

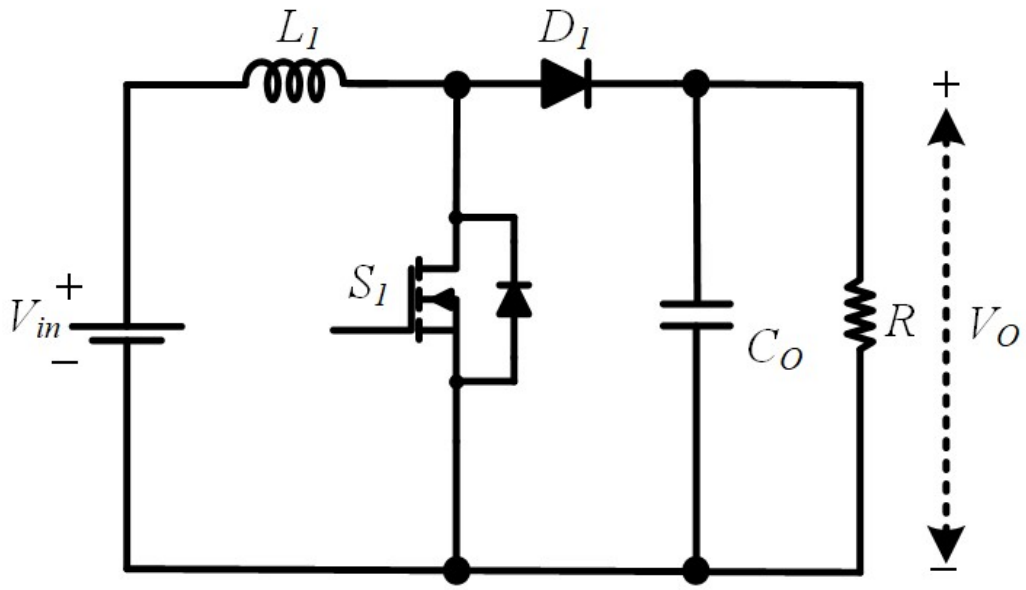

Fig1.1: Conventional Boost Converter

1.2 Buck Converter:

The buck converter is one of the most widely used DC–DC power electronic converters, and its purpose is simple enough: it accepts a higher DC input voltage and produces a lower, regulated DC output. Since the output remains below the input, it is commonly called a step-down converter. The term is plain, but it is accurate. In modern electronic systems, buck converters matter because they are efficient, compact, and able to hold a steady output without throwing away much power. They show up in switched-mode power supplies, battery-powered devices, electric vehicles, solar installations, communication equipment, computer motherboards, and plenty of portable electronics. Their usefulness is tied closely to conversion efficiency. Linear regulators handle voltage reduction by dissipating the extra energy as heat. That approach is easy to understand, yet it is often inefficient and wasteful. Buck converters work in a different way. They dopend on the high-frequency switching, which keeps power loss lower. The practical result is better efficiency, less heat generation, and longer battery life in portable systems. For applications where space and energy consumption matter, that advantage is difficult to dismiss. A basic buck converter contains a controlled semiconductor switch, a diode, an inductor, a capacitor, and the load. Several semiconductor devices that can be utilized as the switch, such as power MOSFETs. In fact, power MOSFETs are frequently favored simply because they switch at higher frequencies, they dissipate less power and are easier to control at the gate. The inductor and capacitor components together form a low-pass LC filter that filters out output current and voltage ripple. This is what makes the load have a smoother DC voltage rather than a rippling and unsteady output. The functioning principle is based on the energy storage in the inductor and then releasing it in a controlled manner. The high frequency is switched ON & OFF . The switching transfers energy from the source to the load . The conventional control approach is Pulse Width Modulation, PWM generator. The switching frequency is fixed and the output voltage is varied by varying the duty cycle with PWM. The time-based PWM is usually favored since it is easy to install and because the converter operates in only two modes. When the switch is ON the diode is reverse-biased and remains OFF. During this interval the input supply directly feeds the load through the switch and inductor. The inductor stores energy in its magnetic field and the capacitor charges and helps hold the output voltage steady. In this mode the current in the inductor increases slowly. When the switch is turned OFF, everything changes fast. The inductor resists this sudden decrease in current and flips its polarity in an attempt to keep current flowing. The stored inductor energy is transferred to the load by forward biasing of the freewheeling diode. At this point the inductor releases its stored energy and the current diminishes steadily. The capacitor also maintains the output voltage during the switching period. This cycle repeat again and producing a steady stepped-down DC output. The duty cycle can be adjusted to provide the output voltage with good efficiency. Buck converters are utilized in mobile phone chargers, laptop adapters, battery charging systems, renewable energy systems, point of

load converters, automotive electronics and power management circuits. It is one of the best and crucial converter topologies in modern electrical.

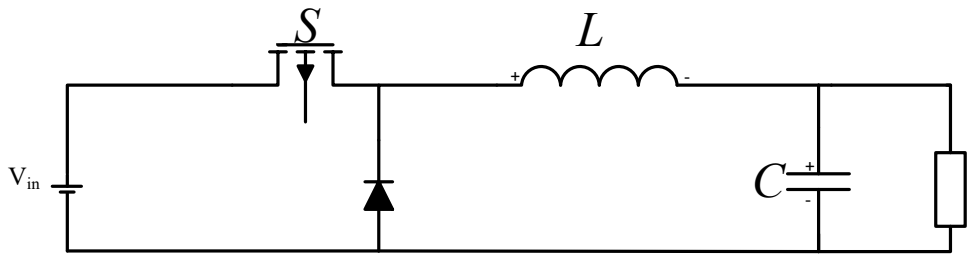

Fig1.2: Conventional Buck Converter

1.3 The Two-Stage Power Conversion Architecture

A two-stage cascaded DC-DC converter architecture is adopted in this work to address the dual requirements of high voltage step-up from a renewable energy source and precise, regulated voltage delivery to a battery charging load. The system comprises two independently controlled power conversion stages connected by a common intermediate DC-link bus, as illustrated conceptually in Figure 1.3.

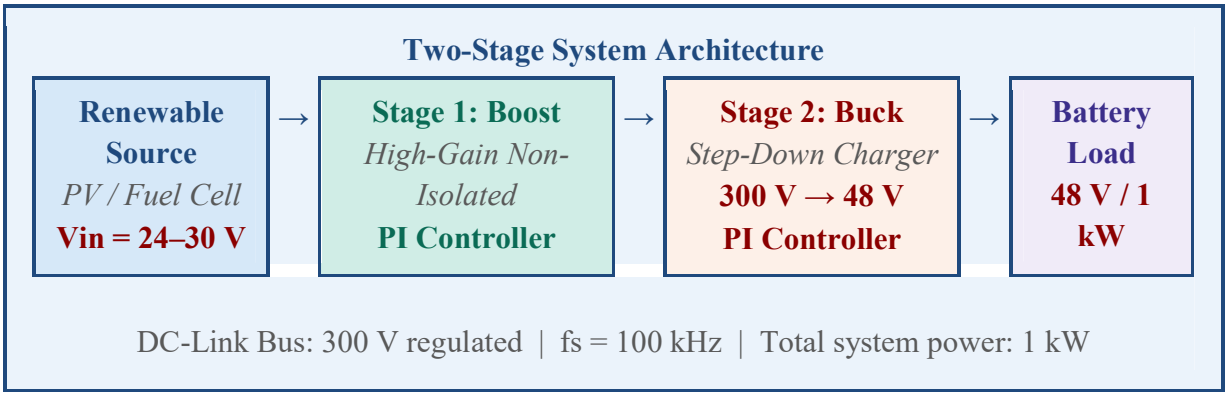

Fig 1.3 Two-Stage System Architecture

The first stage is a high-gain non-isolated DC-DC boost converter. This stage accepts the variable 24–30 V input from the renewable energy source and produces a tightly regulated 300 V intermediate DC-link voltage. The boost stage is controlled by a closed-loop proportional-integral (PI) voltage controller that adjusts the PWM duty

cycle in real time to maintain the 300 V output regardless of input voltage variation or downstream load changes. The second stage is a conventional synchronous buck converter that steps the 300 V DC-link voltage down to 48 V for charging a 1 kW battery pack. The buck stage is independently controlled by a second PI controller that regulates the charging voltage and current to the levels required for safe and efficient battery charging. The two stages share the 300 V DC link as their common interface, providing modular, independently optimised operation of each conversion stage. Most importantly, the proposed topology achieves a voltage gain of $(3-2D)/(1-D)^2$, which delivers a gain exceeding 11 at a duty ratio of only 0.6.

The proposed system is a fully DC-DC converter chain intended for 1 kW battery charging directly from a renewable energy source. The architecture consists of two cascaded stages: a non-isolated high-gain boost converter that steps up the low and variable input voltage from a photovoltaic (PV) panel or fuel cell to a regulated 300 V DC intermediate bus, followed by a synchronous buck converter that steps this bus voltage down to the battery terminal voltage under closed-loop constant-current / constant-voltage (CC/CV) control. No AC-DC power factor correction stage is involved. This literature review examines the three constituent areas that underpin this system: high-gain boost DC-DC converter topologies for renewable energy interfacing, buck DC-DC converters for battery charge regulation, and the cascaded boost-buck architecture that combines both stages into a single 1 kW charger.

1.4 Literature Review

The proposed system is a fully DC-DC converter chain intended for 1 kW battery charging directly from a renewable energy source. The architecture consists of two cascaded stages: a non-isolated high-gain boost converter that steps up the low and variable input voltage from a photovoltaic (PV) panel or fuel cell to a regulated 300 V DC intermediate bus, followed by a synchronous buck converter that steps this bus voltage down to the battery terminal voltage under closed-loop constant-current / constant-voltage (CC/CV) control. No AC-DC power factor correction stage is involved. This literature review examines the three constituent areas that underpin this system: high-gain boost DC-DC converter topologies for renewable energy interfacing, buck DC-DC converters for battery charge regulation, and the cascaded boost-buck architecture that combines both stages into a single 1 kW charger.

1.4.1 High-Gain Boost DC-DC Converters for Renewable Energy Interfacing

1.4.1.1 The Step-Up Requirement in Renewable Energy Systems

Photovoltaic panels and fuel cells are the primary renewable DC sources considered for off-grid and distributed charging applications. Under standard test conditions (STC) a single PV panel delivers an open-circuit voltage of 20-45 V and a maximum-power-point voltage of 18-36 V, while a hydrogen PEM fuel cell stack of comparable power rating typically outputs 20-50 V [5] and To generate a stable 300 V intermediate DC bus from these sources, a step-up ratio of 6:1 to 15:1 is required, and so, this range lies well beyond what a conventional single-switch boost converter can practically achieve. At the duty cycles required for these conversion ratios (D > 0.83 for a 6:1 gain from the ideal formula 1/(1−D)), the actual gain of the conventional boost collapses due to the equivalent series resistance (ESR) of the inductor and capacitors, while the switch and diode must simultaneously block the full 300 V output voltage and conduct the full input current [5], these constraints -- gain roll-off, high switch stress, and elevated conduction loss -- have driven extensive research into alternative step-up topologies specifically suited to the renewable energy interfacing task.

1.4.1.2 Conventional and Quadratic Boost Converters

The quadratic bost converter (QBC) overcom the gain seiling of the conventional topology by cascading two boost stages, yielding an ideal gain of 1/(1−D)^2 with a single activ swtch. Several QBC variants targeting renewable energy applications have been reported. The topology in [12] achieves a gain of (3+D)/(1−D) using two switches, seven diodes, four inductors, and three capacitors (sixteen components), delivering high gain but at the cost of a large component count that increases converter volume and cost at the 1 kW level. A switched-LC based QBC with a reduced component count was reported by Kumar et al. [15], achieving a gain of (3−3D+D^2)/(1−D)^2 with two switches and six diodes and demonstrating suitability for DC microgrid and PV applications at power levels directly relevant to the proposed charger. Ahmad et al. [13] presented a high-gain DC-DC converter with continuous input current for DC microgrid applications, highlighting that continuous input current -- which suppresses current ripple at the PV terminals -- is essential for stable maximum power point tracking (MPPT), since large current ripple causes the MPPT algorithm to misidentify switching-frequency perturbations as irradiance-induced power changes.

At the 1 kW power level operating with a 300 V output target, QBC topologies face two specific challenges. First, the peak inductor current increases rapidly with output power,

raising the required core volume and winding resistance. Second, the duty cycles needed for a 10:1 step-up ($D \approx 0.68$ with a quadratic gain) place the converter in a regime where the switch on-time becomes very short at high switching frequencies, degrading gate-drive reliability. Tarzamni et al. [11] confirmed through a comprehensive comparative study that QBC-derived topologies require careful inductor design to remain in CCM across the full load range and that switching losses above 150 kHz constrain practical efficiency for topologies with high component counts.

1.4.1.3 Quasi-Z-Source Converters

Quasi-Z-source (qZS) converters replace the conventional series inductor with a two-element LC impedance network, enabling shoot-through protection -- where both the upper and lower switches can be turned on simultaneously without causing a short-circuit -- and enhanced boosting capability without an additional active switch [16], [17]. Haji-Esmaeili et al. [16] proposed a high step-up qZS DC-DC converter achieving a gain of $1/(1-3D)$ with inherent short-circuit immunity, a valuable property when the converter is directly fed by a PV array whose open-circuit voltage may spike during load transients. Kumar and Veerachary [17] extended this concept with a Z-network plus switched-capacitor combination, further reducing switch voltage stress. However, qZS converters operate within a constrained duty-cycle range ; effective boosting requires D greater than 0.2 but D must remain below 0.33 to avoid instability in the impedance network; which limits the converter's adaptability when the PV input voltage swings from near open-circuit to near-short-circuit conditions during cloud transients. The impedance network also adds a second inductor and capacitor, increasing total component count and associated core losses at 1 kW.

1.4.1.4 Interleaved High-Gain Converters

Interleaved boost converters distribute the input current across two or more parallel phases switched with evenly spaced PWM signals, so that the input current ripple seen by the PV array is the sum of N out-of-phase triangular waveforms that partially cancel [18], [19]. This ripple suppression is especially important at the 1 kW level, where the RMS input current (approximately 33 A for a 30 V, 1 kW PV source) produces significant ripple if a single-phase boost is used, and where the MPPT accuracy degrades when the ripple-to-average current ratio exceeds approximately 5% [31]. Meraj et al. [19] demonstrated an interleaved multilevel boost converter with minimal voltage multiplier components achieving high step-up ratios with reduced device stress at power levels directly comparable to the proposed 1 kW system. Chub et al. [18] combined an interleaved structure with a quasi-Z-source network, showing that the combination

eliminates the input filter entirely and reduces total inductor volume by approximately 30% compared with a single-phase equivalent.

Despite these advantages, interleaved converters at 1 kW require two complete sets of inductors, switches, and gate-driver circuits, increasing the PCB area and the number of magnetic components. For a compact charger targeting renewable energy applications where minimising the number of active and magnetic components is a priority, the interleaved approach is less attractive than a single-phase topology of comparable gain.

1.4.1.5 Voltage-Lift and Hybrid Switched-Capacitor/Inductor Topologies

Voltage-lift (VL) techniques boost gain by storing charge in a capacitor during the switch-on interval and discharging it in series with the source during the switch-off interval, effectively adding one source voltage to the output voltage per lift stage [21]. Shahir et al. [21] presented a VL-based non-isolated boost converter for PV applications achieving a gain of $3/(1-D)$ -- triple the conventional boost gain at the same duty cycle -- with two switches, six diodes, two inductors, and four capacitors. For the target output of 300 V from a 30 V PV source (10:1 ratio), this topology requires a duty cycle of only $D = 0.57$, comfortably within the range where switching losses and inductor saturation are manageable at 100 kHz.

Hybrid topologies that combine switched-capacitor cells with switched-inductor structures achieve even higher gains. Andrade et al. [22] reported a hybrid transformer-less high-gain converter combining a switched-capacitor cell and a voltage multiplier structure, demonstrating reduced switch voltage stress and a gain of $2D/(1-D)^2$ at moderate duty cycles. Zaid et al. [23] proposed a converter using both diode-capacitor and switched-inductor multiplier techniques, achieving high gain with deliberately asymmetric voltage stress across its two switches to allow the use of a lower-rated device on the higher-gain switch. Tang et al. [25] showed through analytical comparison that inserting a switched-inductor cell into the conventional boost loop effectively multiplies the gain-per-switch-stress ratio, improving converter utilisation at the 1 kW power level. While these hybrid approaches are effective, they increase the passive component count and introduce mutual dependencies between capacitor voltages that complicate fault-tolerant design.

1.4.1.6 Coupled-Inductor High Step-Up Converters

Coupled-inductor (CI) converters use the turns ratio of a multi-winding magnetic to multiply the voltage gain beyond what is possible with a single-winding inductor, achieving very high step-up ratios at duty cycles below 0.7 [10], [24]. Gohari et al. [24] proposed a non-isolated ultra-high-gain CI-based DC-DC converter using a three-

winding coupled inductor and an active switched-inductor network, with leakage inductance recycled through a clamp capacitor to protect the switches from voltage spikes. This topology delivers the high gain required to reach 300 V from a 20 V fuel cell input at moderate duty cycles, while keeping the switch voltage stress below the output voltage through energy recycling. Seo et al. [10] combined input-parallel output-series connection with a coupled inductor and switched capacitor for continuous input current and high gain, demonstrating suitability for distributed generation applications.

For the 1 kW renewable-source-to-300 V-bus applications, CI converters introduce a practical challenge: the turms ratio and leakage inductance of the wound core must be tightly controlled to ensure that the gain and the clamp voltage match the design values across the production tolerance of the magnetic. Leakage inductance variation of +/-20% -typical for hand-wound prototypes-can cause clamp voltage excursions that exceed the switch voltage rating at 1 kW, requiring conservative switch selection and thereby partially negating the low-stress advantage. This manufacturing sensitivity makes non-coupled-inductor topologies preferable when production consistency is a design objective.

1.4.1.7 High-Gain Boost Stage

The high-gain boost converter proposed by Lin et al. is a non-isolated, non-coupled-inductor topology specifically suited to the task of stepping up a renewable source voltage to a stable 300V DC bus at the 1 KW power level. The circuit employs two switches (S_1 and S_2), three diodes (D_1-D_3), two inductors (L_1 and L_2), and three capacitors (C_1-C_3) -- ten passive and active components -- with a single PWM signal driving both switches simultaneously. The single-PWM architecture eliminates the need for a second independent gate-drive channel, directly reducing hardware cost and control complexity relative to all multi-switch, multi-PWM competing topologies. The CCM voltage gain is:

$$\frac{V_{DC}}{V_{in}} = \frac{3 - 2D}{(1 - D)^2}$$

where V_{DC} = 300 V is the regulated intermediate bus voltage and V_{in} is the renewable source voltage. For a 30 V PV source, the required gain is 10, achieved at D = 0.61 -- a moderate duty cycle well within the practical CCM range where ESR-induced gain roll-off is negligible and switching losses at 100 kHz are manageable. For a 24 V source the gain of 12.5 is achieved at D ≈ 0.65, and for a 36 V source the gain of 8.3 is achieved at D ≈ 0.57, demonstrating that a single fixed-frequency controller can regulate the output

across the full PV maximum-power-point voltage range by adjusting D alone. The voltage stress on switch S_1 is $\frac{V_{dc}^2(1-D)^2}{3-2D}$

and on S_2 is $\frac{V_{DC}*(2-D)*(1-D)^2}{3-2D}$, both substantially below V_{DC} -- at D = 0.6, V_{in} = 24 V, V_{DC} = 280V, the stresses are 70 V and 180 V respectively. This distributed stress permits the use of 100 V and 250 V rated MOSFETs with significantly lower on-resistance than the 400-600 V devices required in topologies where both switches block the full output voltage, directly reducing conduction loss at 1 kW.

A 300 W hardware prototype of the converter validated efficiencies of 92.5-94.5% across the full load range at 100 kHz switching frequency. The absence of a coupled inductor eliminates leakage-inductance-induced switch spikes and the associated clamp circuitry, and both inductors operate in CCM, ensuring low and continuous input current ripple compatible with MPPT algorithms. These properties make the proposed converter well suited as the first stage of the 1 kW DC-DC charger.

1.4.2 Buck DC-DC Converters for Battery Charge Regulation

1.4.2.1 The Role of the Buck Stage in the Charger

The second stage of the proposed charger is a step-down (buck) DC-DC converter whose input is the regulated 300 V intermediate bus and whose output is the battery terminal voltage, controlled to follow the CC/CV charging profile. In a standalone DC-DC charger fed directly from a DC bus -- with no AC grid, no power factor correction, and no isolation requirement -- the buck topology is the natural choice for the output stage: it provides a continuously controllable step-down ratio $V_{bat} = D*V_{DC}$, maintains continuous (non-pulsating) output current through the series output inductor, and can be controlled by a simple dual-loop PI controller with inner current and outer voltage loops [32]. The non-pulsating output current is particularly important for battery longevity, as large current ripple into the battery terminals accelerates lithium plating and electrolyte degradation in lithium-ion cells [35].

For the 1 kW charger with V_{DC} = 300V and a target battery voltage range of 36-72 V (representative of a 10S-20S lithium-ion pack), the required buck duty cycle varies between D_2 = 0.12 and D_2 = 0.24. This operating range is favourable: it avoids the minimum pulse-width constraints of very low duty cycles and is far from unity, where switch turn-off losses become dominant. The relatively low output current (approximately 21 A at 48V, 1 kW) means that a single-phase synchronous buck can operate without interleaving, keeping the converter simple and compact.

1.4.2.2 Fundamentals of the Buck Converter

The buck converter in its canonical form consists of one active switch, one freewheeling diode, an output inductor, and an output capacitor. The steady-state CCM conversion ratio is $V_{out} = D \cdot V_{in}$, derive also from the volt-second balance on the inductor [32]. Erickson and Maksimović established the complete small-signal averaged model for the buck converter, showing that the duty-cycle-to-output transfer function is a second-order low-pass response with a resonant frqncy at $f_0 = 1/(2\pi\sqrt{(LC)})$, and that the converter is inherently stable in open loop, required only a simple PI compensator to meet closed-loop bandwidth and phase-margin specifications. This analytical tractability makes the buck converter straightforward to integrate into a dual-loop CC/CV charger controller, where the inner current loop tracks the inductor (charge) current and the outer voltage loop enforces the constant-voltage setpoint at the end of charge.

1.4.2.3 Synchronous Buck for High Efficiency

The synchronous buck converter replaces the freewheeling diode with a second MOSFET (synchronous rectifier, SR), eliminating diode forward-voltage drop conduction loss. At 21 A output current, a standard 600 V fast-recovery diode with V_d = 1.5 V dissipates approximately 21 W in conduction loss, reducing efficiency by over 2 percentage points at 1 kW. Replacing this diode with a low-R_DS(on) MOSFET reduces the conduction loss to $I^2 \cdot R_{DS(on)} \approx 21\text{^}2 \text{ x } 0.05 \approx 20$ W -- a saving of 11 W, improving the buck stage efficiency from approximately 95% to 96% and the overall cascade efficiency by approximately 1 percentage point [33]. The SR requires a dedicated gate-drive signal with a programmable dead time to prevent shoot-through, typically implemented as a second PWM output channel from the same STM32 microcontroller used for the boost stage.

1.4.3 Control of the Buck Stage in the Cascaded Charger

In the cascaded boost-buck system, the buck stage control loop must be designed to operate correctly despite the variation in its input voltage caused by the boost MPPT loop. When the PV irradiance changes, the MPPT algorithm updates D_1 and temporarily perturbs V_{DC} before the boost stage regulation loop restores it to 300 V. This input voltage perturbation appears as a disturbance to the buck stage. A well-designed buck voltage controller with sufficient bandwidth can reject this disturbancethe inner current loop, operating at a bandwidth of approximate f_{sw}= 20 kHz, responds within a few switching cycles, while the outer voltage loop, operating at approximately 1-2 kHz, corrects any steady-state deviation Ghaeminezhad and Monfared [35] reviewed charging control strategies for lithium-ion battery packs and established that cascaded PI control with inner current and outer voltage loops provides robust CC/CV regulation against

input voltage disturbances of +/-10%, consistent with the disturbances expected from the MPPT loop in the proposed system a neural-network-based CC/CV control method for a buck converter was demonstrated by Bhagat et al. [36] at the same power and voltage level as the proposed charger, showing that a trained neural network controller can achieve faster mode transition and better disturbance rejection than a fixed-gain PI controller, at the cost of additional computation and training effort for the proposed system, a standard dual-loop PI controller is selected as the baseline control design, consistent with the PI approach validated in (K_p = 0.05, K_i = 0.02), with the neural-network approach noted as a viable upgrade path if tighter transient response is required.

1.4.4 Cascaded High-Gain Boost-Buck DC-DC Converter for 1 kW Battery Charging

1.4.4.1 System Architecture and Power Flow

The proposed 1 kW charger consists entirely of two DC-DC converter stages with no AC-DC conversion. The renewable energy source -- a PV array or fuel cell -- delivers a low, variable dc voltage Vin (typically 24-36 V from a PV string under varying irradiance). The first stage is the high-gain boost converter, which steps V_{in} up to a regulated 300 V intermediate DC bus under MPPT control the second stage is a synchronous buck converter that steps the 300 V bus down to the battery terminal voltage V_{bat} under CC/CV control, and also the intermediate bus capacitor C_{mid} decouples the two stages, ensuring that transients in the MPPT loop do not directly propagate to the battery current also the two duty cycles are independently controlled, and neither stage requires knowledge of the other stage operating point, making the control design modular and robust to individual stage failures.

1.4.4.2 Intermediate Bus Voltage Selection and Stress Distribution

The intermediate bus voltage V_{DC} = 300 V is selected to balance three competing objectives: (i) the boost stage gain requirement from the PV source, (ii) the buck stage duty cycle at the battery terminal voltage, and (iii) the switch voltage stress in both stages. For a 30 V PV source and a 48 V battery, the gain split between the two stages is 10:1 (boost) and 0.16:1 (buck). Setting V_{DC} = 300 V places the boost stage duty cycle at D_1 = 0.61 and the buck stage switch at a blocking voltage of 300 V -- below the 400 V used in conventional EV charger architectures, enabling the use of 400 V-rated MOSFETs rather than 600 V devices, with a corresponding reduction in $R_{DS(on)}$ of approximately 40% for the same die area [33].

The switch stress in the boost stage -- 70 V on S_1 and 180 V on S_2 at D = 0.6 -- means that neither boost switch needs to be rated above 200 V, which is the voltage class

associated with the fastest, lowest-R_{DS}(on) silicon MOSFETs and GaN devices. This distributed, low-stress characteristic is a direct result of the proposed boost topology's hybrid diode-capacitor and switched-inductor gain mechanism and is the primary advantage of the converter over single-switch topologies that impose full output-voltage stress on the only switch. At 1 kW, lower switch voltage ratings translate to lower on-resistance, reduced gate charge, and faster switching transitions, all of which contribute to efficiency improvement relative to a 300 V or 400 V switch in a single-stage topology.

1.4.4.3 Efficiency Budget at 1 kW

The overall efficiency of the cascaded charger at 1 kW is the product of the individual stage efficiencies. The boost stage -- extrapolated from the 92.5-94.5% efficiency of the 300 W prototype in is expected to achieve approximately 93-95% at 1 kW after component rescaling, since the switching frequency (100 kHz) and topology are unchanged and the larger MOSFETs and inductors reduce both conduction and core losses per unit power. The synchronous buck stage is expected to achieve 95-97% efficiency at the operating point D_2 = 0.12-0.24, V_{DC} = 300 V, I_{out} = 21A at 100 kHz, based on standard synchronous buck designs at comparable voltage and current levels [33]. The overall cascade efficiency at rated 1 kW output is therefore estimated at 88.4-92.2%, which comfortably satisfies the greater-than 85% efficiency target commonly specified for Level 1 DC-to-battery chargers in off-grid renewable applications.

The double energy processing inherent to the cascaded architecture -- where the full 1 kW passes through the boost stage inductor and then again through the buck stage inductor -- is the principal efficiency penalty relative to a hypothetical single-stage converter. However, as demonstrated by Al-Saffar and Ismail [4] and analytically confirmed by Fang et al. [34], a single-stage boost converter operating at the extreme duty cycle required to achieve a 10:1 step-up from 30 V to 300 V ($D > 0.90$ for the conventional boost) suffers from diode reverse-recovery losses, inductor core saturation at high peak currents, and switch body-diode losses during dead time that collectively reduce efficiency to below 85% at 1 kW -- worse than the cascaded design. The cascaded boost-buck therefore achieves higher practical efficiency at high conversion ratios precisely because it distributes the conversion burden between two moderate-duty-cycle stages operating well within their efficient operating regimes.

1.5 Comparison with Related DC-DC Charger Topologies

The proposed two-stage non-isolated DC-DC charger is compared with alternative architectures for renewable-source-to-battery charging at the 1 kW level. Single-stage

non-inverting buck-boost converters -- such as the SEPIC, Ćuk, or four-switch non-inverting buck-boost -- can in principle step both up and down in a single conversion stage, avoiding double energy processing. However, the SEPIC and Ćuk are limited in gain at 1 kW by their coupled-inductor or series-capacitor energy transfer mechanisms, and the four-switch non-inverting buck-boost requires independent control of four active switches with carefully managed mode transitions through the crossover region which is a point of reduced gain and potential control instability [32]. The cascaded boost-buck avoids this crossover instability entirely because V_DC = 300 V is always much larger, ensuring that the buck stage always operates in step-down mode.

Isolated two-stage converters (boost + LLC resonant, or flyback) provide galvanic isolation between the PV source and the battery, which is required in some safety standards for grid-connected systems. For off-grid PV-to-battery charging, however, isolation is not mandated by IEC 62109-1 or UL 1741 provided the system grounding is properly implemented, and the non-isolated cascade avoids the transformer core and winding losses that reduce efficiency by 1-2 percentage points at 1 kW [6]. The proposed non-isolated cascade is therefore the preferred choice for off-grid residential and light-commercial PV charging applications where efficiency, compactness, and cost are the primary design criteria.

CHAPTER-2

PROJECT OBJECTIVE

2.1 Background

The global energy landscape has undergone a fundamental transformation in recent decades, driven by an accelerating transition away from fossil-fuel-based generation toward renewable and distributed energy sources and the Photovoltaic (PV) systems and hydrogen fuel cells have emerged as two of the most technically mature and commercially viable distributed generation technologies, offering zero direct carbon emissions, inherent scalability, and the potential for deployment across a wide range of power levelsfrom residential rooftop installations to utility-scale solar farms. According to the International Energy Agency (IEA), solar PV alone accounted forthelargest share of new electricity generating capacity additions globally in recent years, and this trend is expected to accelerate substantially through 2030 and beyond.

Despite their considerable promise, these renewable energy technologies share a fundamental and persistent challenges are from the voltage produced at their terminals is inherently low, variable, and poorly regulated. A typical PV module produces an open-circuit voltage in the range of 20 V to 45 V, with the maximum power point voltage typically lying between 15 V and 35 V depending on temperature and irradiance conditions. Similarly, a protonexchangemembrane (PEM) fuel cell stack produces an output voltage that varies significantly with load current due to activation, ohm, and concentration polarization losses within the cell. In the context of the present work, the renewable energy source — a PV array or equivalent distributed generator — produces a variable DC output voltage in the range of 24 V to 30 V. This voltage level is fundamentally incompatible with the requirements of medium and high-power applications, which typically demand a regulated DC bus voltage of several hundred volts for efficient energy distribution, storage interface, or inverter-fed AC load supply.

Power electronic DCDC converters serve as the critical interface between these lowvoltage, variable renewable energy sources and highervoltage distribution systems. In this rolethe converter must simultaneously achieve a large voltage step-up ratio, maintain tight output voltage regulation despite fluctuation in both input voltage and load demand, operate with high power conversion efficiency to minimise thermalosses

and maximise the utilisation of the harvested renewable energy, and do so using a compact, cost-effective, and reliable circuit topology. These requirements are substantially more demanding than what conventional boost converter topologies can satisfy, particularly when the required voltage gain approaches or exceeds a factor of ten — as is the case in the present work, where a gain of approximately 10 to 12.5 is required to produce a stable 300 V DC-link voltage from a 24 V to 30 V input.

2.2 Motivation:

The motivation for this research is rooted in three converging technical and societal imperatives: the urgent need to integrate renewable energy at scel the growing demands of the efficient electric vehicle (EV) charging infrastructure, and the persistent technical gaps in existing high-gain converter designs that limit their practical devployability.

2.2.1 The Renewable Energy Integration Challenge

The intermittent and low-voltage nature of distributed renewable energy sources creates a fundamental power electronics problem that has not yet been fully solved by commercially available converter technologies, existing solutions generally fall into one of two categories: isolated converters that use high-frequency transformers to achieve also required for the voltage gain, or conventional boost-derived topologies that require operation at very high duty cycles. Both approaches carry significant drawbacks. Isolated converters introduce transformer copper and core losses, leakage inductance, increased volume and weight, and higher manufacturing cost. Conventional boost converters operating at high duty cycles suffer from elevated switch stress, poor efficiency due to parasitic ESR losses, input current ripple, and gain saturation all of which degrade system performance and reliability.

Therefore a clear and pressing motivation to a developed power electronic converter systems for renewable energy applications that simultaneously achieve: a high voltage conversion ratio from a low, variable input without the requiring of magnetic isolation; low stress on the active switching devices to improve reliability and permit the use of cost-effective components; high power conversion efficiency to maximise

utilisation of harvested renewable energyand simple, robust closed-loop control that maintains regulated output voltage under all operating conditions. The proposed two-stage architecture directly addresses all four of these requirements.

2.2.2 The Need for Integrated Charging Solutions

The electrofication of transportation represents the most significant energy transitions of the present decade electric vehicles require frequent, efficient, and reliable battery charging, and a growing proportion of ev charging is being powered directly from renewable energy sources either through grid-tied systems with high renewable penetration, or through off-grid solar to ev charging stations. In this kind of cases, the power electronic converter system must bridge the gap between the low, variable DC output of the renewable source and the battery charging requirements, which typically demand a precisely regulated DC voltage of 48 V to 800 V depending on the battery chemistry and vehicle class.

The battery charging system will impose a particularly stringent requirements on voltage and current regulation, overcharging even transiently can cause irreversible damage to battery cells, accelerate capacity fade, and in extreme cases pose a safety hazard. Undercharging reduces the effective range of the vehicle while charging at an incorrect current rate stresses the battery and shortens its cycle life, these requirements mandate a dedicated, tightly controlled DC-DC conversion stage between the DC bus and the battery rather than relying on the upstream boost converter for direct battery interface this will be the core motivation of the cascaded double stage architecture that is adopted in this work the boost stage provides a stable regulated 300 V DC bus regardless of renewable source fluctuations, and the downstream buck converter provides precise, independently controlled 48 V to a 1 kW charging to the battery.

2.3 Research Objectives

The overreaching aim of this research is to design, analyze and simulate validate a double stage cascaded DCDC power conversion system for the renewable energy

powered charging of the battery, compromising a high-gain non-isolated boost converter as the first stage and a regulated buck converter as the second stage, with closed-loop PI control for both stages in pursuit of this aim, the following specific research objectives are defined:

2.3.1To design and analyse a high-gain boost converter for a Renewable Energy applications

A high gain DC-DC boost converter will be design to step up the low voltage taken as input from the renewable energy source to a regulated 300V DC-link voltage. The converter design will be including the selection of the passive components such as inductor and capacitors. This will be calculated based on the required voltage gain and ripple, and also depend on the switching frequency. The steady-state operation and performance characteristics of the converter will be analysed under different operating conditions to evaluate voltage gain, efficiency, current ripple, and switching stress on the switches. The relationship between duty cycle and converters performance will also be investigated to ensure the efficient operating condition at moderate duty-cycle values.

2.3.2 To design and implementing the closed-loop PI voltage controller for the boost converter stage.

The proportional–integral (PI) controller is designed to regulate the output of boost converter to a stable 300 V DC-link voltage under variable input voltage conditions (24–30 V) which will be produced by the renewable energy source. The PI controller gains ($K_p = 0.5$, $K_i = 9.725$) will be selected.

2.3.3 To design a cascaded buck converter stage for 48 V / 1 kW battery charging

A step-down buck converter will be designed to accept the regulated 300 V DC-link voltage and deliver a precisely controlled 48 V output at a maximum power of 1 kW. The buck converter will be independently controlled by a second closed-loop PI controller providing voltage-mode regulation of the charging voltage. Component values (inductance, output capacitance) will be calculated from first principles to satisfy the specified output voltage ripple and current ripple requirements. The operating duty cycle of the buck stage ($D \approx 0.16$) will be shown to place the switch in a low-stress operating region, consistent with the duty-cycle stress analysis presented for the boost stage.

2.3.4 To analyse the effect of duty cycle on switch stress across both converter stages

A systematic analysis of the relationship between PWM duty cycle and switching device stress will be conducted for both the boost and buck converter stages. This analysis will demonstrate that the proposed topology's ability to achieve high voltage gain at a moderate duty cycle ($D = 0.6$) — rather than the high duty cycles ($D \rightarrow 0.9$) required by conventional boost converters for equivalent gain — directly reduces peak switch current, conduction losses, and thermal dissipation, improving converter reliability and permitting the use of lower-rated switching devices.

2.3.5 To validate the complete two-stage system through simulation in MATLAB/Simulink

The complete cascaded boost-buck system, including both PI control loops and the renewable energy source model, will be implemented and simulated in MATLAB/Simulink. Simulation results will include open-loop and closed-loop waveforms of key voltages and currents, dynamic response to step changes in input voltage (24 V to 30 V) and load resistance, output voltage regulation accuracy, and steady-state ripple characterisation for both stages. Simulation results will be compared against the theoretical predictions derived in Objectives 1 through 4.

CHAPTER 3

HIGH GAIN DC-DC BOOST CONVERTER

3.1 Working and Operational Mode:

Figure 3.1 shows the schematic for the proposed high-gain boost converter the topology has two inductors (L_1 and L_2), also three diodes which are (D_1, D_2 and D_3), three energy-storage capacitors (C_1, C_2 and C_3), and two active switches(S_1 and S_2) that are all powered by the same PWM signal this unified switching method makes control easier and cuts down on the number of gate drivers needed the converter uses a multi-stage energy transfer process to get a lot of voltage gain and efficiency.

In the Mode1 when both switches are activated diodes D1 and D3 are reverse-biased while diode D2 is in a conducting state. During this period, the inductive components extract energy from the input and accumulate it within their magnetic fields simultaneously will certain capacitors in the circuit are charged according to the current pathways permitted by the conducting diode. Simultaneously, another capacitor discharges, transferring a portion of its stored energy to the intermediate boosting stage this generates the requisite magnetic and electric energy for high-gain functionality.

When the switches are in the of position (Mode2). At this time the diodes D1 and D3 wil be forward-biased and conduct, whereas diode D2 is reverse-biased the energy formerly stored in the passive components is now directed to the output the inductive components discharge their accumulated magnetic energy via the diode network certain capacitors also undergo partial discharge and accumulate their voltages with the energy produced by the inductor this significant enhances the boosting capacity as the existing pathways alter according to the diode's orientation one capacitor is simultaneously charged to a greater potential the converter achieves voltage gains much surpassing those of conventional boost converters with comparable duty ratios by alternating between energy storage during the on phase and energy release during the offphase.

The proposed converter is highly suitable for various medium to the high power application due to the advantageous of electrical and operational characteristics this is particularly applicable to systems requiring significant voltage amplification consistent DClink generatiom and efficient power transmission across varying load and source circumstances. Its capacity to operate consistently while providing high gain and reduced switching stress enhances its utility in renewable energy power converters, independent EV charging modules, and other sophisticated power electronic systems. The next part offers a comprehensive investigation of the converter's performance under real-world operating settings, examining both continuous conduction mode (CCM) and discontinuous conduction mode (DCM), it comprehensively addresses the current flow, energy transfer processes, and the equivalent circuits for each mode.

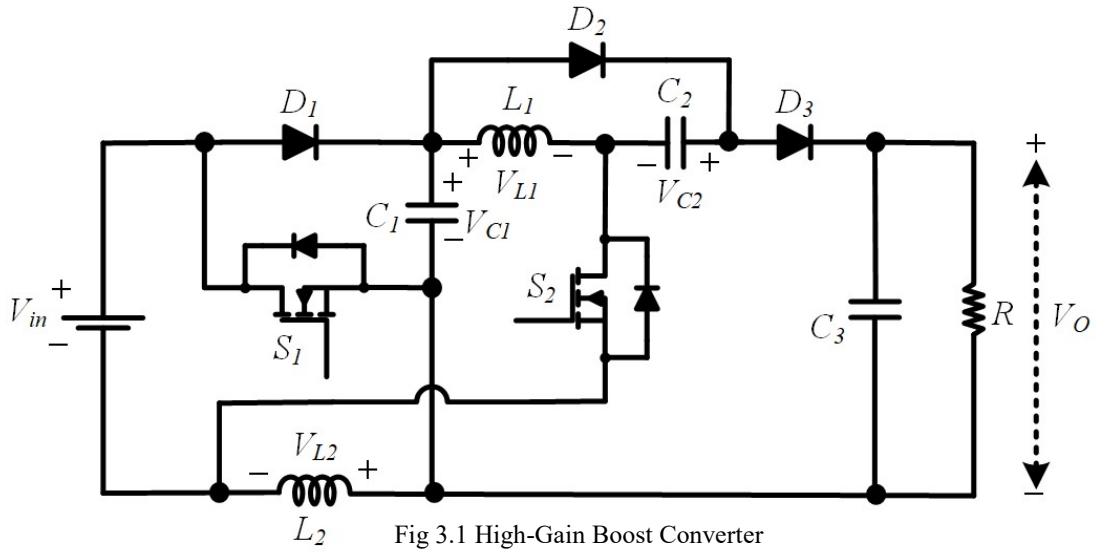

Fig 3.1 High-Gain Boost Converter

3.1.1 Continuous Conduction Mode

The circuit operates in two primary modes: the switch-ON mode and the switch-OFF mode, contingent upon the switching signal transmitted to the converter for the converter to function well and maintain its high-gain characteristics, both active switches (S_1 and S_2) must be simultaneously activated and deactivated during each switching cycle in CCM the currents will be flowing through inductors L_1 and L_2 remain above zero at all times this ensures continuous energy flow between the source, passive components, and output upon activation of the switch, energy from the input source is transmitted to inductors L_1 and L_2 this causes their currents to increase as magnetic energy accumulates in their cores. The incremental increase in inductor current during the ON state of the switches is responsible for the voltage elevation when the switches are OFF. The switch-OFF interval transmits the accumulated energy from L_1 and L_2, along with the energy from capacitors C_1, C_2, and C_3, to the output via the diode network. Figure 3.2 illustrates the characteristic waveforms of inductor currents and capacitor voltages during Continuous Conduction Mode (CCM) operation. The data illustrate the consistent inductor current and the cyclical charging and discharging of the capacitors, which collectively enable the proposed converter to operate at a high gain.

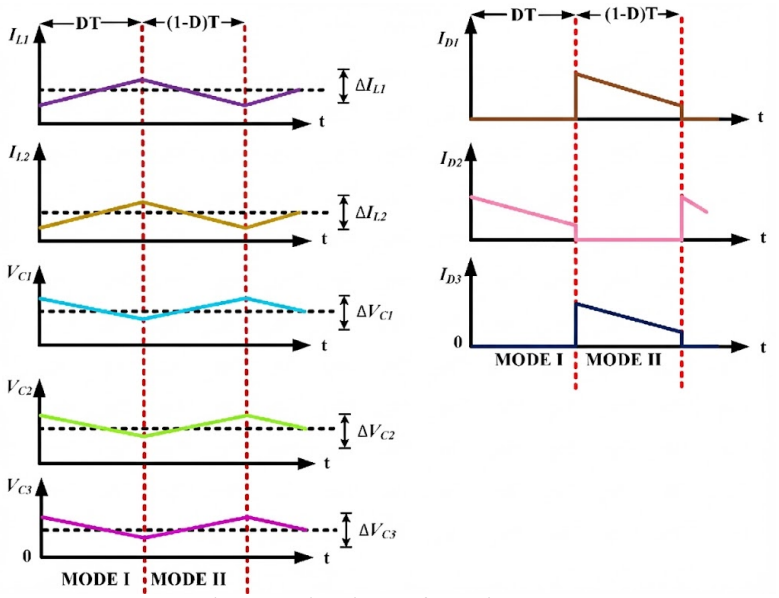

Fig 3.2 Related waveforms in CCM

Mode-1 ($0 \leq t \leq DT$)

In Mode-1, the simultaneous activation of switches S_1 and S_2 determines the conduction state of the diodes inside the circuit. During this period, diodes D_1 and D_3 are reverse-biased, whereas diode D_2 is forward-biased. This establishes a conduction pathway that transmits energy from the input source to inductors L_1 and L_2. This increases the currents across L_1 and L_2, enabling both inductors to accumulate magnetic energy. The arrangement of the conducting and non-conducting diodes ensures that the capacitors remain charged or discharged in accordance with the converter's signal amplification. The initial operational mode is represented by an equivalent circuit depicted in Figure 3.3. It illustrates the pathways through which current traverses during the switch-on phase. To mathematically evaluate this mode, Kirchhoff's Voltage Law (KVL) is applied to the equivalent circuit of Mode-1 to derive the switch-ON equations for the continuous conduction mode (CCM). These equations illustrate the variation of voltage between L_1 and L_2, serving as the foundation for comprehending the converter's gain and its operational behavior upon activation.

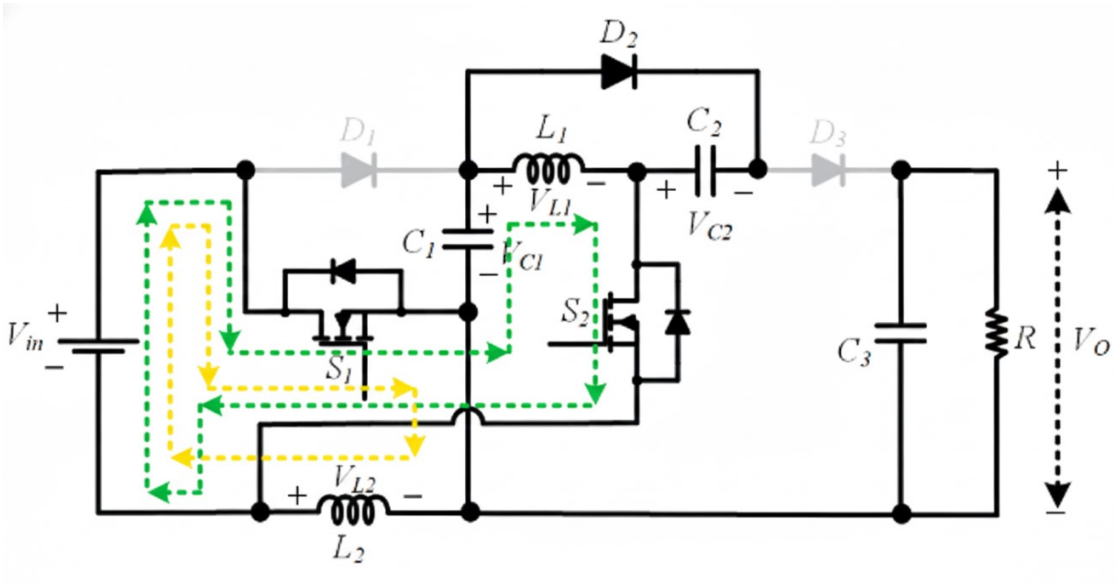

Fig 3.3: Equivalent circuit for switch-on mode of operation.

$$V_{L1} = V_{in} + V_{C1} = V_{C2} \qquad 3.1.1.1$$

$$V_{L2} = V_{in} \qquad 3.1.1.2$$

Mode 2 (DT ≤ t ≤ T)

Fig3.4 illustrates the analogous circuit depicting the operation of the converter in the off state, referred to as Mode2 when both switches S_1 and S_2 are simultaneously deactivated, the diode conduction pattern in the circuit adjusts accordingly due to the switching transition, diodes D_1 and D_3 become forward-biased and commence conduction diode D_2, conversely, becomes reverse biased and ceases current flow through its branch the energy stored in the passive components of the converter is now advancing to the output stage this occurs due to the switches being open and the alteration of the diode pathways dsuring this period the inductr released the magnetic energy they had accumulated whil the capacitors discharged from the electrical energy they had retained this results in an increase in output voltage which enhances the efficacy of the suggested topology the simultaneous occurrence of inductor discharge and capacitor voltage stacking significantly enhances the total voltage conversion ratio in Mode2 to quantitatively define this operational interval, Kirchhoff's Voltage Law (KVL) is applied to the equivalent circuit in switchoff mode, enabling the derivation of the corresponding Mode-2 voltage equations that govern the converter's dynamic and steady-state behavior.

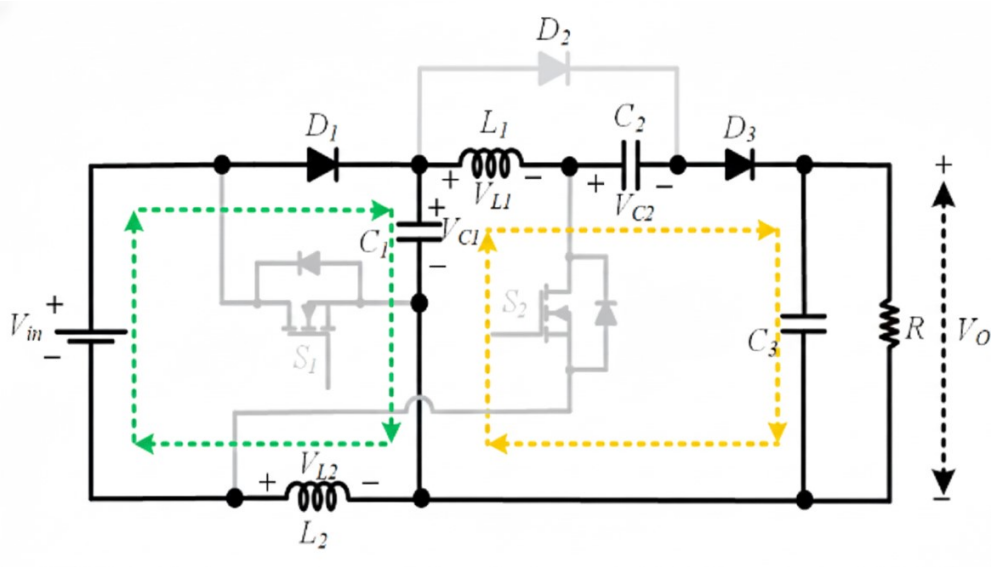

Fig 3.4: Equivalent circuit for switch-off mode of operation.

$$V_{C1} = V_{L1} + V_{C2} - V_O \quad 3.1.1.3$$

$$-V_{L1} = V_O - V_{C1} - V_{C2} \quad 3.1.1.4$$

$$-V_{L1} = V_O - V_{C1} - V_{in} - V_{C1} \quad 3.1.1.5$$

$$V_{L1} = V_{in} + 2V_{C1} - V_O \quad 3.1.1.6$$

$$V_{L2} = V_{in} - V_{C1} \quad 3.1.1.7$$

By applying volt-inductor balance across an inductor $L2$

$$V_{in}D + (V_{in} - V_{C1})(1 - D) = 0 \quad 3.1.1.8$$

$$V_{C1} = \frac{V_{in}}{(1-D)} \quad 3.1.1.9$$

Apply the voltage inductor balance at the inductor $L1$.

$$(V_{in} + V_{C1})D + (2V_{C1} + V_{in} - V_O)(1 - D) = 0 \quad 3.1.1.10$$

$$2V_{C1} - V_{C1}D + V_{in} - V_O(1 - D) = 0 \quad 3.1.1.11$$

$$V_{C1}(2 - D) = V_O(1 - D) + V_{in} \quad 3.1.1.12$$

$$-V_O(1 - D) + \frac{V_{in}(2 - D)}{(1 - D)} + V_{in} = 0 \quad 3.1.1.13$$

$$V_O(1 - D) = \frac{(2V_{in} - V_{in}D + V_{in} - V_{in}D)}{(1 - D)} \quad 3.1.1.14$$

$$V_O(1 - D) = \frac{(3V_{in} - 2V_{in}D)}{(1 - D)} \quad 3.1.1.15$$

$$\frac{V_O}{V_{in}} = \frac{(3 - 2D)}{(1 - D)^2} \quad 3.1.1.16$$

3.1.2 Discontinuous Conduction Mode

Figure below illustrates the two scenarios in which the converter enters discontinuous conduction mode (DCM) in this mode, the current through at least one inductor ceases to flow at a certain moment during the switching cycle and thereafter reaches zero a disruption in either inductor current is sufficient to transition the converter from continuous conduction mode (CCM) to discontinuous conduction mode (DCM) this alteration in the converter's operation modifies the current pathways, diode conduction periods, and the overall energy transfer mechanism thus, the voltage gain and dynamic response differ from those observed in CCM. The generalized DCM equations for the proposed highgain converter can be derived by analyzing the inductor current waveforms capacitor charging intervals and diode conduction states illustrated in Fig 3.5 these equations establish the mathematical basis for defining the converter's steady-state properties under conditions of discontinuous inductor current, as detailed below.

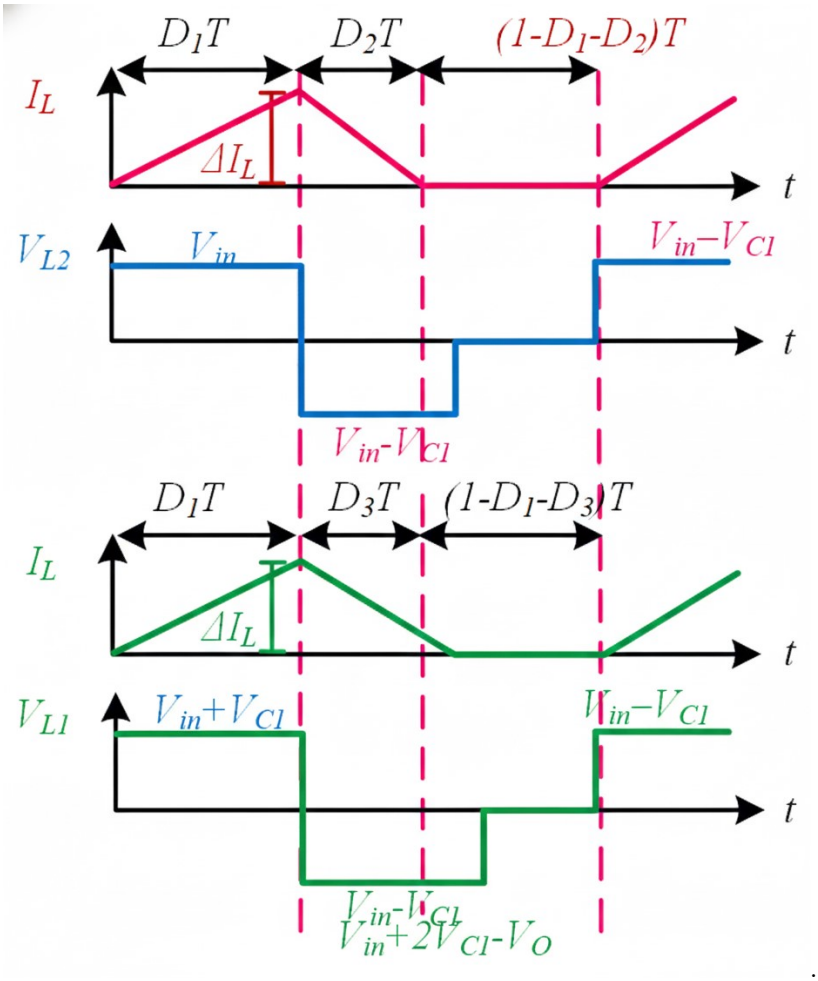

Fig3.5: Discontinuous Conduction Mode Waveforms

$$V_{in}D_1 + (V_{in} - V_{C1})D_2 = 0 \qquad 3.1.2.1$$

$$V_{in}D_1 + V_{in}D_2 = V_{C1}D_2 \qquad 3.1.2.2$$

$$V_{C1} = \frac{(V_{in}D_1 + V_{in}D_2)}{D_2} \qquad 3.1.2.3$$

$$(V_{in} + V_{C1})D_1 + 2(V_{C1} + V_{in} - V_O)D_3 = 0 \qquad 3.1.2.4$$

$$V_{in}D_1 + V_{C1}D_1 + 2V_{C1}D_3 + 2V_{in}D_3 = 2V_OD_3 \qquad 3.1.2.5$$

$$\left(\frac{V_O}{V_{in}}\right)_{DCM} = \frac{\left(2\,D_1^2 + 4\,(D_1D_2 + D_1D_3 + D_2D_3)\right)}{(D_2D_3)} \qquad 3.1.2.6$$

3.2 Designing of Passive Components

This section discusses the design and determination of the passive components required for the proposed converter. To ensure optimal functionality and stability of the converter, it is crucial to accurately determine the dimensions of the inductors and capacitors. This is particularly applicable when the converter is intended to operate in CC the inductor value directly influences current flow, ripple characteristics, and dynamic responsiveness the capacitor values, conversely, dictate the voltage ripple and the overall rigidity of the DC output several criteria influence the selection of these passive components, including switching frequency, output load, duty cycle, and permissible ripple limitations elevated switching frequencies typically allow for the utilization of smaller inductors and capacitors, as each cycle requires reduced energy storage conversely, reduced switching frequencies necessitate larger components to maintain performance at an acceptable standard to ensure the suggested high-gain boost converter operates effectively and dependably in Continuous CCM, a meticulous equilibrium must be established among switching frequency, ripple specifications, and converter efficiency.

3.2.1 DETERMINING THE INDUCTANCE VALUE

The primary objective of inductor design is to enable the converter to function in Continuous Conduction Mode (CCM). Equation (2.3.6) delineates the minimal requisite inductance for L1 in Continuous Conduction Mode (CCM).

$$L1\frac{dI_{L1}}{dt} = V_{in} + V_{C1} \qquad 3.2.1$$

$$L1\frac{dI_{L1}}{dt} = V_{in} + \frac{V_{in}}{1-D} \qquad 3.2.2$$

$$L1\frac{dI_{L1}}{dt} = V_{in} - V_{in}D + V_{in} \qquad 3.2.3$$

$$L1\frac{dI_{L1}}{dt} = \frac{(2\,V_{in} - V_{in}D)}{(1-D)} \qquad 3.2.4$$

$$L1\frac{V_O}{R} \geq V_{in}(2 - D)D\,T \qquad 3.2.5$$

$$L1 \geq R\frac{(1-D)^2(2-D)}{(2\,(3-2\,D)f_s)} \qquad 3.2.6$$

where *R* is the load value, the duty ratio is signified by *D*, and *fs* indicated switching frequency. *L* is the required inductance of the inductor (*L*1 & *L*2).

Similarly for inductor *L*2:

$$L2 \geq R\frac{(1-D)^4D^2}{(2\,f_s(3-2\,D)(1+D-D^2))} \qquad 3.2.7$$

3.2.2 SELECTING THE CAPACITANCE VALUE

The selection of a capacitor is contingent upon the maximum permissible voltage ripple and the voltage across the capacitor itself. When selecting a capacitor and ensuring it does not rupture, its value must be carefully determined. Adequately elevated to endure any possible high voltage that may be delivered across the capacitor. The capacitor's value can be calculated using the equation(2.3.13).

$$I_{C1}\Delta T = C1\,\Delta V_{C1} \qquad 3.2.8$$

$$I_{C1}D\,T = C1\,\Delta V_{C1} \qquad 3.2.9$$

$$\frac{V_O}{(R\,(1-D))} = C1\,\Delta V_{C1} \qquad 3.2.10$$

$$C1 = \frac{V_O}{(R\,(1-D)f_s\Delta V_{C1})} \qquad 3.2.11$$

$$V_{C1} = \frac{V_{in}(3-2\,D)}{\left((1-D)^2R\,(1-D)f_s\Delta V_{C1}\right)} \qquad 3.2.12$$

$$C1 = \frac{V_{in}(3-2\,D)}{\left(R\,(1-D)^3f_s\Delta V_{C1}\right)} \qquad 3.2.13$$

Similarly for,

$$C2 = \frac{V_{in}(3-2\,D)}{(R\,(1-D)^2f_s\Delta V_{C2})} \qquad 3.2.14$$

$$C3 = \frac{V_{in}(3-2\,D)}{(R\,(1-D)^2f_s\Delta V_{C2})} \qquad 3.2.15$$

Parameters	Values
Vin	24-30V
Inductor 1(L1)	20 µH
Inductor 2(L2)	1 mH
Capacitor 1	33 µF
Capacitor 2	220 µF
DC-Link Capacitor	680 µF

Table 3.1 Parameters Used in High-Gain Boost Converter

CHAPTER- 4

BUCK CONVERTER

4.1 Introduction:

Among the four fundamental non-isolated DC–DC converter topologies — buck, boost, buck-boost, and Cuk — the **buck converter** (also called a step-down converter or series converter) holds a special place in power electronics practice. It is the most widely deployed single-stage topology for on-board point-of-load regulation, appearing in everything from microprocessor voltage-regulator modules to battery chargers and LED drivers. Its enduring popularity stems from three qualities: the output voltage is always lower than the input, which is the most common requirement in digital systems; the control-to-output transfer function has no right-half-plane zero, making stable closed-loop design relatively straightforward; and the inductor current is continuous under normal loading conditions, so the converter behaves as a controllable current source into the output capacitor, yielding low ripple without excessive filtering.

This chapter develops the complete steady-state theory of the buck converter from first principles. Starting from circuit-level KVL and KCL equations applied to the two switch states, the analysis proceeds through volt-second and charge-balance conditions to derive the voltage conversion ratio, the inductor current ripple, the output voltage ripple, and the boundary between continuous and discontinuous conduction. Every result is expressed in closed form so that it can be used directly in component selection and design optimisation.

4.2 Circuit Description and Operating Principle

The canonical buck converter circuit, shown schematically in Figure 4.1, contains five elements: a controllable switch S (realised in practice as a power MOSFET), a freewheeling diode D, a series inductor L, a shunt output capacitor C, and a resistive load R. The switch and diode form a complementary pair — when S is on, D is reverse-biased and carries no current; when S is off, D is forward-biased and provides a current path for the inductor.

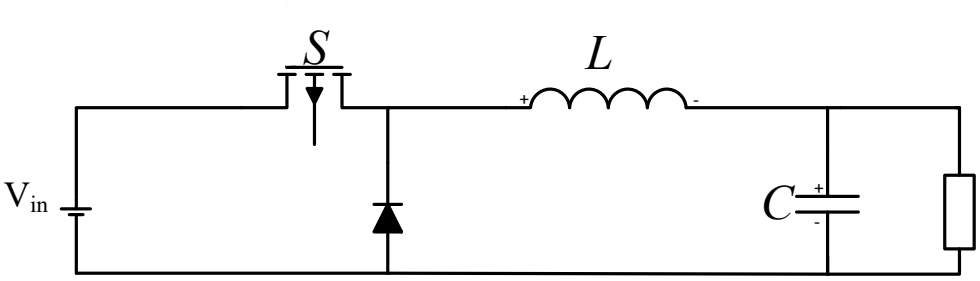

Fig4.1: Buck Converter

Energy flows from source to load in two distinct intervals within each switching period T = 1/f, where f is the switching frequency. The fraction of each period during which S remains on is the duty cycle D (not to be confused with the diode symbol), defined as:

$$D = \frac{t_{on}}{T}, \qquad 0 < D < 1$$

The complementary off-time fraction is written (1 – D), so that *t_off* = (1-D)T. All steady-state analysis in this chapter assumes that the circuit has reached periodic steady state — that is, every waveform is exactly periodic with period T.

Switch On ($0 \le t < t_{on}$):

When S closes at t = 0, the source voltage Vs is applied to the left terminal of L. If the output voltage V_o is held approximately constant by C (a valid assumption when C is large).

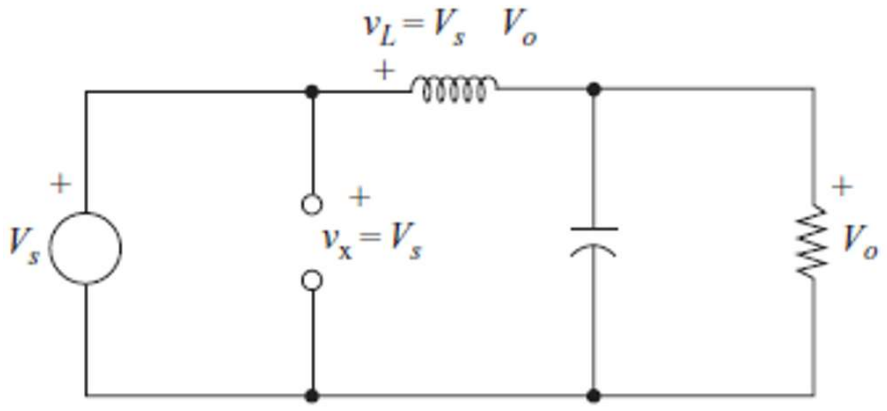

Fig4.2: Buck Converter Mode 1

For Mode 1 Apply KVL

$$-V_{in} + L\left(\frac{di_L}{dt}\right) + V_c = 0 \text{.....4.2.1}$$

$$L\left(\frac{di_L}{dt}\right) = V_{in} - V_c \text{.....4.2.2}$$

$$\frac{di_L}{dt} = -\frac{V_c}{L} + \frac{V_{in}}{L} \text{.....4.2.3}$$

$$\frac{di_L}{dt} = 0 \cdot i_L - \left(\frac{1}{L}\right)V_c + \left(\frac{1}{L}\right)V_{in} \text{.....4.2.4}$$

For Mode 1 Apply KCL

$$i_L = i_c + i_o \text{.....4.2.5}$$

$$i_c = i_L - i_o \text{.....4.2.6}$$

$$C\left(\frac{dV_c}{dt}\right) = i_L - \frac{V_c}{R} \text{.....4.2.7}$$

$$\frac{dV_c}{dt} = \left(\frac{1}{C}\right)i_L - \left(\frac{1}{RC}\right)V_c \text{.....4.2.8}$$

Switch Off ($t_{on} \leq t < T$):

When the switch is open, the diode becomes forward-biased to carry the inductor current and the equivalent circuit of applies. The voltage across the inductor when the switch is open is

For Mode 2 KCL

$$\frac{dV_c}{dt} = \left(\frac{1}{C}\right)i_L - \left(\frac{1}{RC}\right)V_c \text{.....4.2.9}$$

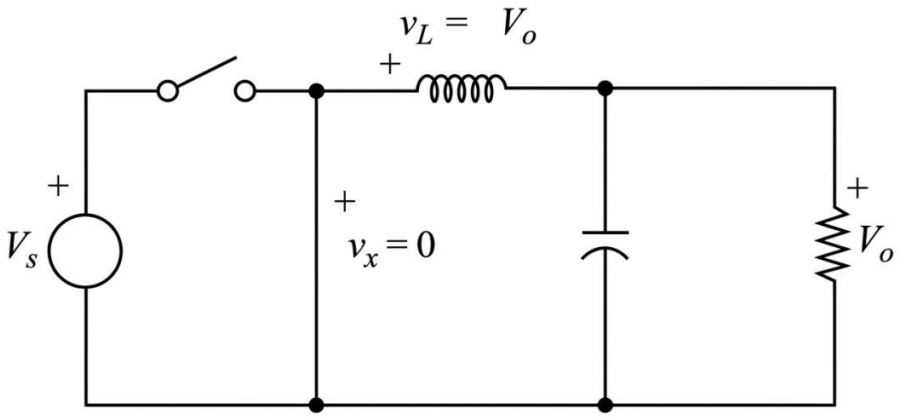

Fig4.3: Buck Converter Mode 2

For Mode 2 KVL

$$V_L + V_c = 0 \text{…….4.2.9}$$

$$L\left(\frac{di_L}{dt}\right) = -V_c \text{…….4.2.10}$$

$$\frac{di_L}{dt} = 0i_L - \left(\frac{1}{L}\right)V_c + 0V_{in} \text{…….4.2.11}$$

The most powerful constraint in steady-state converter analysis is the volt-second balance principle in periodic steady state the net volt-seconds accumulated by an inductor over one full period must equal zero. If it were not zero, the inductor current would drift upward or downward each cycle without bound, which contradicts the assumption of steady state. Mathematically:

$$(\mathrm{d}i_L)_{closed} + (\mathrm{d}i_L)_{open} = 0$$

from the above equations

$$\left(\frac{V_s - V_o}{L}\right)(DT) - \left(\frac{V_o}{L}\right)(1 - D)T = 0 \text{…….4.2.12}$$

Solving the above equation for the output voltage Vo:

$$V_o = V_{sD} \text{…….4.2.13}$$

4.3 Designing of the Passive Components

In this part, the passive components required for designing the buck converter will be determined. Since the best possible results can only be guaranteed through correct calculations, the exact size calculations of the inductors and capacitors should be done. The sizes of inductors have significant influence on the current flow, ripple and dynamics. On the other hand, the sizes of capacitors determine the voltage ripple and how rigid the output dc voltage is. The factors that influence choice of these components include switching frequency, load, duty cycle and allowable ripple. Higher switching frequencies require smaller passive components because of low energy per cycle whereas lower frequencies lead to larger components. To achieve maximum performance of the Buck, an appropriate balance between switching frequency and ripple should be made.

Inductance Value

$$L = \left(\frac{V_S - V_o}{\Delta i_L f}\right) D = \left(\frac{V_{o(1-D)}}{\Delta i_L f}\right) \text{.....4.3.1}$$

Capacitor Value

$$C = \frac{1-D}{8L\left(\frac{\Delta V_o}{V_o}\right) f^2} \text{.....4.3.4}$$

Parameters	Value
V_{in}	300v
Inductor	27 µH
Capacitor	68 µF
Resistor	2.2 Ω

Table 4.1: Parameters Used for Buck Converter

CHAPTER-5

CONTROL SCHEME

5.1 Closed-Loop Control of the Proposed Converter

This section examines the efficacy of the proposed converter in conjunction with a proportional-integral (PI) controller within a closed-loop system the primary function of the controller is to maintain the output voltage at a consistent reference level, regardless of fluctuations in the input voltage the simulation results indicate that the PI controller effectively compensates for variations in the input supply, maintaining a stable output voltage unaffected by these fluctuations the controller maintains a stable output voltage despite significant variations in load resistance, indicating effective load regulation within the system this indicates that the picontroller functions appropriately when the reference varies, adjusting the duty cycle to maintain the voltage level despite fluctuations in input or load to achieve this steady performance, the controller is assigned meticulously selected proportional (Kp) and integral (Ki) gains this ensures the converter reacts promptly to alterations, has minimal steady-state error, and performs well under all operating situations.

This high-gain boost converter requires a PI controller due to its output voltage's great sensitivity to variations in duty cycle and operating circumstances the converter's multi-stage energy transfer mechanism means that even minor fluctuations in the input supply or load can result in significant variations in the output voltage the PIcontroller mitigates these issues by continuously adjusting the duty cycle according to the discrepancy between the reference voltage and the actual output this ensures the converter operates consistently, minimizes voltage ripple, and prevents detrimental fluctuations that could damage downstream components such as the DClink capacitor or high-power charging stages the controller enhances the system's transient response, reduces steady-state error, and increases overall reliability this ensures that the proposed converter consistently delivers the correct regulated output, regardless of changing conditions.

The outer voltage control loop is responsible for maintaining the stability of the boost converter's output voltage despite variations in input and load conditions. Within this loop, the output voltage is continuously monitored and compared to a predetermined value. A proportional-integral (PI) controller processes the error signal, representing the discrepancy between the actual and desired output voltage. The PI controller evaluates both the present error and the accumulated error over time to generate a corrected reference signal for the inner current loop or directly for the duty-cycle modulator, contingent upon its configuration.

The outer loop is very important for keeping the voltage stable over time. The proposed high-gain converter is very sensitive to changes in duty cycle, input voltage, and load. The outer loop makes sure that any changes in output voltage are fixed quickly the outer loop makes up for the following by changing the duty cycle indirectly through the output of the PI controller this will makes sure that the converter keeps a regulated DC output that is good for downstream uses like stabilizing the DClink and fastcharging modules for electric vehicles the converter wouldn't be able to keep a steady output voltage without the outer loop this is especially true when the gain is high, when even small changes can have a big effect on performance.

5.2 PI Controller Equations

The PI controller used in the outer loop generates the control signal based on the error between the actual output voltage V_0 and the reference voltage V_{ref}.

Error Signal Equation

$$e(t) = V_{ref} - V_{o(t)} \qquad 5.2.1$$

Continuous-Time PI Control Law

$$u(t) = K_p e(t) + K_i \int e(t)dt \qquad 5.2.2$$

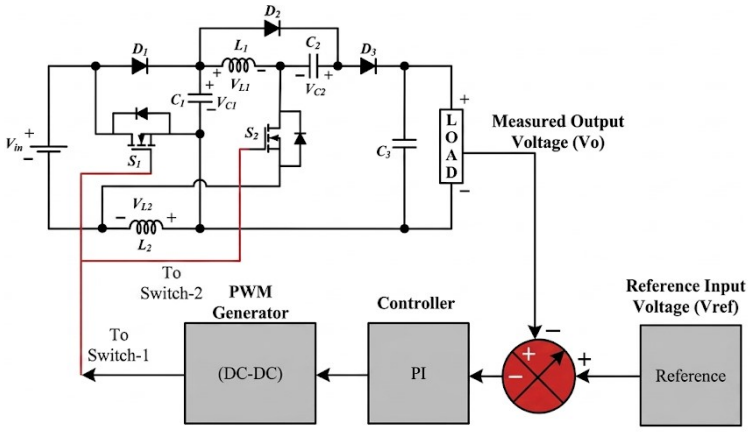

Fig 5.1: Closed Loop Control of High-Gain Boost Converter

5.3 Closed-Loop Control of the Buck Converter

With the high-gain boost stage maintaining a stable 300 V at the DC link through the PI voltage controller described in Section 4.1, the task remaining at the second stage is to regulate the energy delivered to the battery through the buck converter. Unlike the boost stage, which has a single voltage regulation objective, the buck converter in this application requires two nested control loops: an outer voltage loop that sets the output voltage to the required charging level, and an inner current loop that controls the instantaneous inductor current. This cascaded loop structure is standard practice for DC-DC converters supplying battery loads because the inductor current -- which is also the battery charging current -- must be independently observable and controllable regulated the current directly in an inner loop prevents overcurrent conditions during transients, limits the rate of change of current into the battery, and accelerates the overall closed-loop dynamic response compared with a single voltage loop acting alone.

The two control loop are arranged concentrically around the buck converter plant the outer voltage loop compares the measured output voltage against a voltage setpoint and produces a current reference the inner current loop then drives the inductor current to this reference by adjusting the duty cycle D2 of the buck switch this arrangement means the outer loop nevr directly commands a duty cycle it commands a current, and the inner loop translates that current demand into the appropriate switching action the separation of timescales is deliberate the inner current loop is tuned to a significantly higher bandwidth than the outer voltage loop, so the current tracks its reference quickly and the outer loop sees a well-controlled, fast-responding current source rather than a slow converter plant.

5.3.1 Outer Voltage Controller

The outer loop monitors the buck converter output voltage Vout and compares it to a reference voltage Vref, which represents the target battery charging voltage. The resulting voltage error ev is defined as:

$$ev(t)=Vref-Vout(t)... (5.3.1.1)$$

A PI controller processes this error and generates a current reference Iref for the inner loop. The continuous-time PI control law for the outer loop is:

$$I_{ref}(t)=K_{p2}ev(t)+K_{i2}\int ev(t)dt... (5.3.1.2)$$

The outer voltage controller for the buck stage was tuned with a proportional gain Kp2 = 0.5452 and an integral gain Ki2 = 685.2. The relatively high integral gain compared with

the boost stage controller (Ki1 = 9.725) reflects the difference in the two plants: the buck converter output filter has a well-defined second-order resonance, and the higher Ki2 is required to achieve adequate low-frequency loop gain and drive the steady-state error to zero within an acceptable settling time. The outer voltage loop bandwidth is set to approximately 1-2 kHz, which is fast enough to track the gradually rising battery terminal voltage during charging but slow enough to remain well below the resonant frequency of the LC output filter and preserve phase margin.

5.3.2 Inner Current Controller

The inner loop regulates the buck inductor current iL to the reference Iref generated by the outer voltage controller. The current error ei is:

$$ei(t) = Iref(t) - iL(t) \quad \text{... (5.3.2.1)}$$

A second PI controller processes this current error to produce the duty cycle command D2 for the buck switch gate driver. The continuous-time PI control law for the inner loop is:

$$D2(t) = Kp_3 ei(t) + Ki_3 \int ei(t)dt \quad \text{... (5.3.2.2)}$$

The duty cycle output D2(t) is clamped within the physical limits [0, 1] before being passed to the PWM modulator, preventing integrator windup and ensuring the switch operates only within its valid on-time range. The inner current controller was tuned with a proportional gain K_{p3} = 0.02194 and an integral gain K_{i3} = 137.9. The inner loop bandwidth is set approximately one decade above the outer voltage loop bandwidth at approximately 20 kHz so that from the perspective of the outer loop, the current tracks its reference almost instantaneously this timescale separation is the condition that justifies treating the two loops as independently designable systems rather than requiring a multi-input multi-output design approach the small value of K_{p3} = 0.02194 reflects the high sensitivity of the buck inductor current to changes in the duty cycle: the inductor current responds rapidly to a small change in D1 because the volt-second difference across the inductor is a large fraction of the 300 V bus voltage a large proportional gain would cause the current to overshoot and oscillate at the switching frequency the integral gain K_{i3} = 137.9 is sized to eliminate steady-state current error within a few switching periods, ensuring the measured inductor current matches the reference produced by the outer voltage loop accurately throughout the charging process.

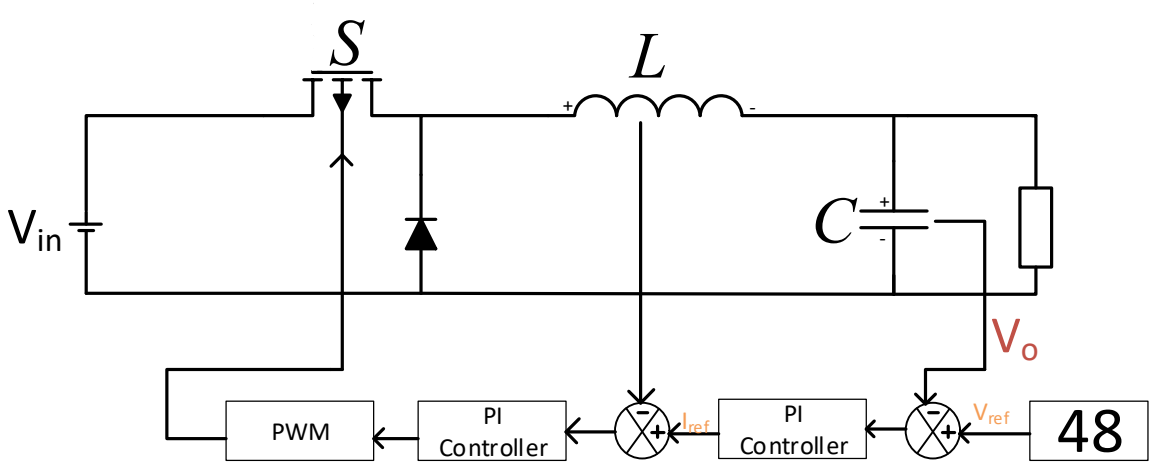

Fig 5.2: Buck Converter with inner and outer control loop

Controller	Loop	Proportional gain (Kp)	Integral gain (Ki)
High-gain boost converter	Voltage (DC link)	0.5	9.725
Buck converter	Voltage (output)	0.5452	685.2
Buck converter	Current (inductor)	0.02194	137.9

Table 5.1 Kp, Ki values used

CHAPTER-6
CASCADED HIGH-GAIN BOOST–BUCK DC–DC CONVERTER

6.1 Cascaded Boost-Buck Converter: Combined Circuit Operation

The preceding chapters examined the high-gain boost converter and the synchronous buck converter individually, establishing the steady-state analysis, component design, and control strategy for each stage in isolation. This chapter brings both stages together as a single cascaded system and discusses how the combined circuit behaves as a complete 1 kW DC-DC battery charger. The focus here is on the interaction between the two stages at the system level -- how power flows through the cascade, what role the intermediate bus plays in separating the source-side dynamics from the output-side dynamics, and how the two independent voltage controllers cooperate to maintain regulation under varying operating conditions.

The complete cascaded circuit is shown in Figure 6.1. The renewable energy source connects to the input of the high-gain boost stage, which steps the source voltage up to a regulated 300 V intermediate DC bus. This 300 V bus feeds directly into the buck stage, which steps the voltage down to the required battery charging level. An intermediate DC-Link capacitor C_3 is placed at the junction between the two stages. The battery load is connected at the output of the buck stage.

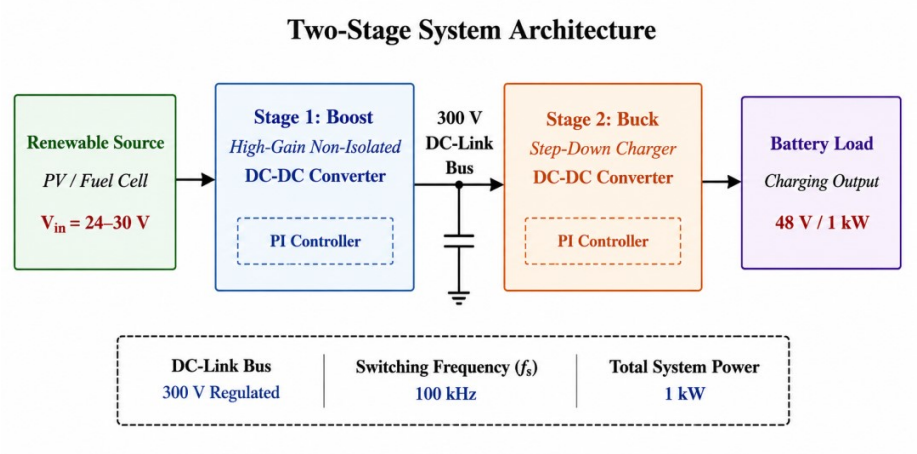

Fig 6.1: Block Diagram of the Proposed Work

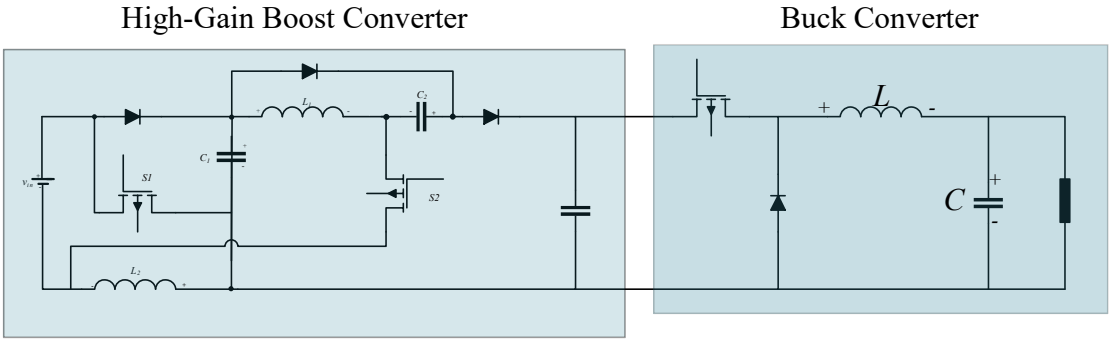

Fig 6.2: High-Gain Boost Converter Cascaded with Buck Converter

In the combined circuit, the boost stge duty cycle D1 and the buck stage duty cycle D2 serve entirely different purposes and are controlled by separate PI voltage controllers running in parallel. D1 is adjusted by the boost controller to hold the intermediate bus at 300 V regardless of what the source voltage. D2 is adjusted by the buck c0ntroller to hold the output voltage at the battery charging setpoint regardless of the state of charge. The overall voltage conversion ratio from the source to the battery terminals is the product of the two individual stage gains.

The intermediate DC-Link capacitor is the physical element that makes this decoupling possible. When the source voltage fluctuates and the boost controller begins adjusting D1 to compensate, there is an unavoidable settling time during which the boost output power and the buck input power are momentarily unequal. During this interval DC-Link either absorbs the excess energy or releases stored energy to make up the deficit, preventing any imbalance from appearing as a voltage disturbance at the battery terminals. The intermediate capacitor therefore isolates the two control loops from each other in the time domain, even though they share the same physical current path in steady state.

The simulation results presented in the following section verify this combined operation. The waveforms confirm the regulated 300 V intermediate bus under varying source voltage, the independently regulated output voltage across the battery charging range, and the dynamic response of the system to step changes in both the source and the load.

6.2 Simulation Environment

Before presenting the simulation results of the proposed cascaded converter system, it is necessary to describe the software environment in which the simulations were carried

out. All simulation work in this thesis was performed using MATLAB/Simulink, developed by MathWorks. MATLAB -- which stnds for MatrixLaboratory -- isa high-level numerical compiting environment and programming language that has become one of the most widely used tools in engineering research and education. Its adoption across power electronics, control systems, signal processing, and renewable energy research is well established, and it provides the analytical and simulation capabilities required to model, analyse, and verify the behaviour of the proposed two-stage DC-DC converter system.

MATLAB itself provides the core numerical computing environment, handling mathematical operations, data processing, and script-based analysis. Simulink, which runs within the MATLAB environment, is a graphical block-diagram simulation platform that allows dynamic systems to be modelled by connecting functional blocks representing physical components and control elements in power electronics simulations, Simulink is used alongside the Simscape Electrical toolbox, which provides purpose-built blocks for switches, inductors, capacitors, diodes, and PWM generators that accurately represent the switching behaviour of power converter circuits this combination will allows the proposed high-gain boost converter and buck converter to be built as circuit-level models whose behaviour is governed by the same differential equations derived in the theoretical analysis chapters, with the added ability to include non-ideal component parameters such as inductor series resistance, capacitor ESR, and switch on-resistance the PI controllers designed in chapter 5 for the boost stage voltage loop, the buck stage voltage loop, and the buck stage current loop are implemented directly in Simulink using discrete-time transfer function blocks, with the sampling period set to match the 100 kHz switching frequency of the converter the gain values determined analytically and listed in Table 6.1 and 6.2 are entered directly into the simulation model, so the simulation results presented in this chapter reflect the same controller parameters that would be used in the physical hardware implementation.

6.3 Scope of Simulation Results

The simulation results presented inthis chapter covers the closed-loop perfrmance of the complete cascaded system with all three PI controllers active. The closed-loop resultsdemonstrate the ability of the boost stage controller to regulate the 300 V DC link against step changes in the source voltage, thebility of the buck stage outervoltage loop and inner current loop to maintain the output voltage at the charging setpoint against step changes inthe load, and the dynamic interaction between the two stages during

simultaneous disturbances on both the source and load sides. Together, the open-loop and closed-loop simulation results provide a comprehensive verification of the theoretical design.

6.4 Parameters Used

Design Parameters Used In High-Gain Boost Converter

Parameters	Values
Vin	24-30V
Inductor 1(L1)	320 µH
Inductor 2(L2)	1 mH
Capacitor 1	33 µF
Capacitor 2	220 µF
DC-Link Capacitor	680 µF
Proportional Gain(K_p)	0.5
Integral Gain(K_i)	9.725

Table 6.1: High-Gain Boost Converter parameters

Design Parameters Used In Buck Converter

Parameters	Value
V_{in}	300v
Inductor	27 µH
Capacitor	68 µF

Resistor	2.2 Ω
Proportional Gain(K_p) (Voltage Control)	0.5452
Integral Gain(K_i) (Voltage Control)	685.2
Proportional Gain(K_p) (Current Control)	0.02194
Integral Gain(K_i) (Current Control)	137.9

Table 6.2: Buck Converter parameters

6.5 Simulation Results

6.5.1 High-Gain Boost Converter

6.5.1.1 Capacitor Voltage:

The waveforms of voltages over capacitors C1 and C2 are presented in Fig. 6.3. Voltage of the capacitor C1 has a stable operating value of about 63 V that can be explained by the formula VC1 = Vin / (1-D1). In this case, for the input voltage of 24 V and D1 = 0.62, VC1 = 24/(1 - 0.62) = 63.2 V. Hence, there is an excellent coincidence between results of the simulation and analytical derivation. The voltage over the capacitor C2 becomes stable and equals about 75 V. Both capacitors have almost no ripple at all. They operate under substantially lower voltage stress than the output voltage of the DC link (300 V). Thus, no single capacitor of the boost stage is operated under maximum output voltage stress. Such feature is one of the major advantages of the offered circuit. The duty cycle waveform included at the bottom of the figure confirms steady-state switching at the specified frequency.

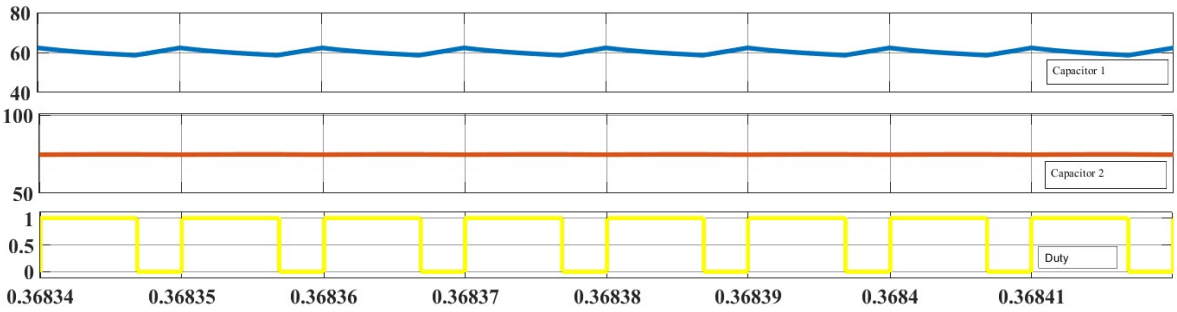

Fig 6.3: Simulation waveforms of Capacitor C1 and C2 voltage

6.5.1.2 Inductor Current:

The duty cycle waveform shown below the figure proves that there is steady-state switching at the frequency given. The current will never drops to zero in the switching process at any given time, thus proving that L1 is operating in continuous conduction mode (CCM) as required. The peak-peak current ripple value of 2.5A proves that the same ripple was used in designing the inductor L2. Inductor L2, on the other hand, has a much larger current averaging about 62A. It is important to note that this current never drops to zero in the switching cycle, meaning that both inductors are operating in CCM simultaneously.

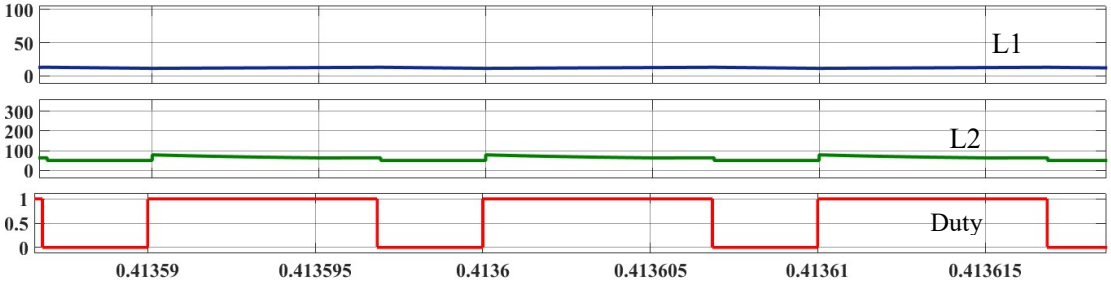

Fig 6.4: Simulation waveforms of
Inductor Current L1 and L2

6.5.1.3 Behavior of Switch 1:

As shown in figure 6.4 the voltage across and the current through the switch S1 are observed in multiple switching cycles. As seen from the figure, during the period of the switch-off, S1 has to block a voltage of about 63 V, consistent with the theoretical expression. Since the value of 63 V in simulation is observed, we can see that the voltage stress in the switch in this topology will depend on the voltage VC1, which depends in turn on the input voltage and the duty cycle. It is also clear that since the voltage stress of 63 V is significantly lower than the 300 V output, the use of a 100 V rated MOSFET is enough for S1. During the on period, the maximum current of about 80 A flows in S1, while gradually decreasing to about 65 A due to linearly increasing inductor current. It is important to note the complementary relationship between these two waves, where the current flows only when there is no voltage and vice versa. This indicates proper switching behavior without having any overlap between these waves, which would show any losses during the switching process.

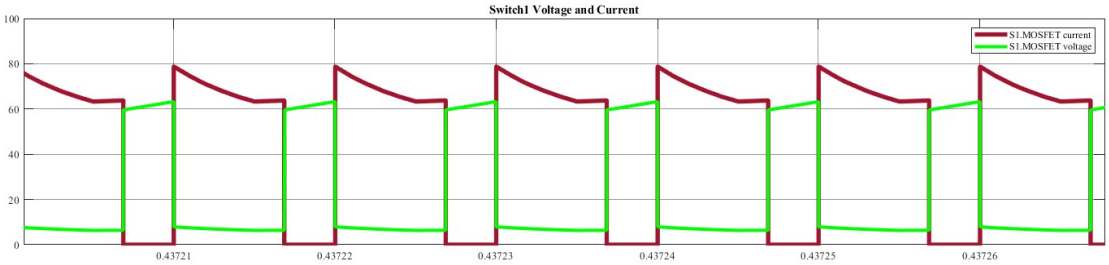

Fig 6.4: Simulation waveforms of
Switch 1 Voltage and Current

6.5.1.4 Behavior of Switch 2:

Waveforms for the voltage and current in switch S2 are presented in Figure 6.5. The blocking voltage when the switch is off state equals to about 190 V. This corresponds to the theory derived before. It can be noticed that the stress voltage in switch S2 is much higher in comparison with the stress voltage in switch S1 (63 V). It reflects the fact that the voltage stresses are not evenly distributed. Nevertheless, the voltage stress in switch S2 (190 V) is still smaller compared with the total DC link voltage (300 V), which means that a 250 V rated MOSFET is sufficient, while the MOSFETs with rating of 400V/600V have rather high on-resistance and losses. The peak value of the current when S2 switch is on is about 28 A and decreases down to zero during conduction. At the same time, it is smaller compared with the peak current in switch S1 due to the fact that S2 carries the current of the second inductor L2 in another circuit way. Thus, the thermal stress of S2 is smaller than S1 despite the difference in voltages.

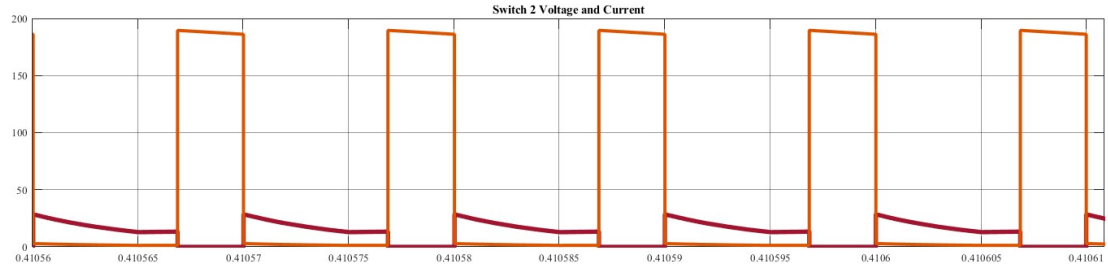

Fig 6.5: Simulation waveforms of
Switch 2 Voltage and Current

6.5.1.5 DC-Link Capacitor:

The voltage of the DC link of the high gain boost converter with closed-loop voltage control using the PI control method. From the waveform above, it can be observed that there is no ripple on the DC link since it is held steadily at 300 volts. This verifies the fact that the boost stage PI voltage control system has been able to maintain the DC link voltage at its desired reference point. With no ripple on the DC link, it shows that the integral effect of the control system has totally removed all errors from the circuit. Moreover, the PI control system's bandwidth is high enough to filter out any ripples produced by the switching frequency from affecting the voltage of the DC link.

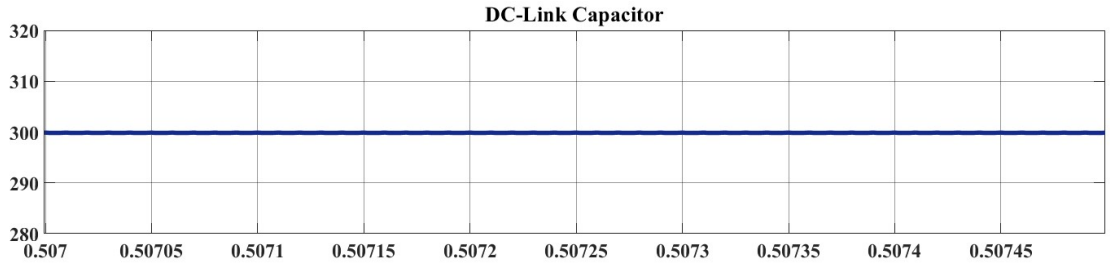

Fig 6.6: Simulation waveforms of
DC-Link Voltage

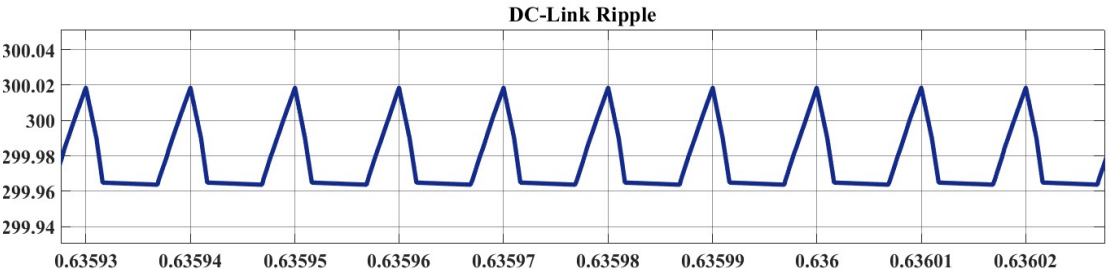

Fig 6.7: Simulation waveforms of
DC-Link Voltage Ripple

6.5.2The Buck Converter

6.5.2.1 Switch Behavior

In the off-state, the switch turns off and experiences blocking voltage equal to the entire DC link voltage. This shows that the buck switch should be able to block the total

voltage of the intermediate bus, and that is why a 400V MOSFET was chosen for S3 in the components. The blocking voltage of S3 is way higher compared to that of any other boost stage switch because the buck stage switch has to withstand the total voltage of the intermediate bus in each switching cycle on the drain terminal. In the on-state, the switch experiences a zero voltage drop as the current increases linearly from about 0 A to about 30A. The rising current depicts the process of charging of the inductor through the switch using the energy supplied by the 300V DC link. The duty cycle curve proves that S3 is switching at D2= 0.16, which means it spends 16% of each cycle in the on-state. This is due to the high step-down ratio of 300V to 48V, and this makes the off-time very long (about 84%). During the off-time, the freewheeling diode conducts and the inductor current flows through it to charge the load. This makes the load to experience the continuous current that we see in the figure below.

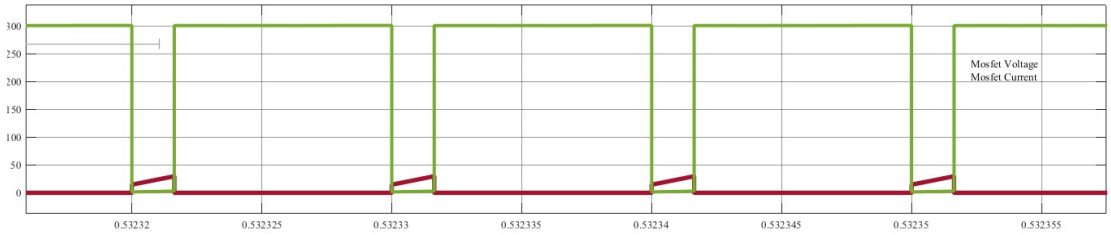

Fig 6.8: Simulation waveforms of
Buck Switch Voltage and Current

6.5.2.2 Output Voltage

Below figure illustrates the output voltage waveform of the buck converter stage using closed-loop PI voltage control. The waveform shows regulation of the output voltage at exactly 48V with no appreciable ripple. The corresponding duty cycle waveforms for this case are also provided, and from Figure 10 below, one can observe that the duty cycle of the buck switch operates at a low duty cycle, approximately equal to D2 = 0.16 as per the theoretical calculations D2 = Vout / Vdc = 48 / 300 = 0.16. Therefore, the theoretical values coincide with those obtained from simulation. As there is no ripple evident in the output voltage waveform, it can be concluded that the output LC filter is effective in reducing switching frequency output voltage ripple to zero. Figure 11 below shows the PI voltage controller with gains Kp2 = 0.5452 and Ki2 = 685.2 that regulates the output voltage at exactly 48V with zero steady state error. Thus, the integral action of the controller has completely reduced any offset in output voltage from 48V reference.

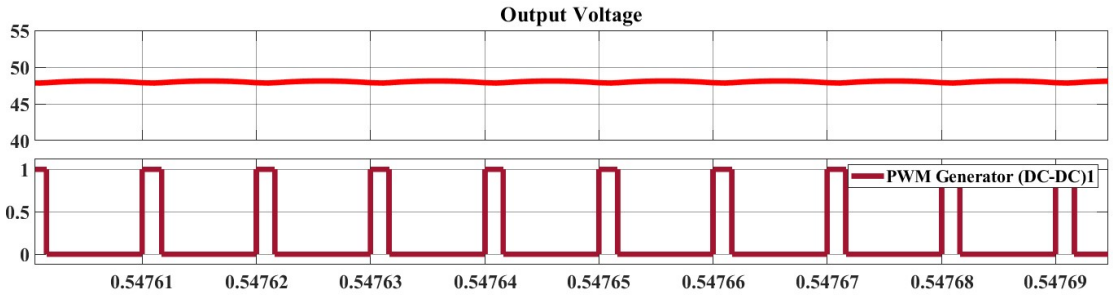

Fig 6.9: Simulation waveforms of
Buck Output Voltage

6.5.2.3 Output Current

A graphical representation of the output current waveform generated by the buck converter is shown below. The current level is controlled and maintains a constant value of 21.5 A without any noticeable ripples in the waveforms. As a result, the total output power is calculated as Pout = Vout × Iout = 48 × 21.5 ≈ 1032 W, and thus, the designed cascaded converter can effectively produce the required 1 kW output power. Smooth output current generation by the circuit can be explained from the standpoint of effective battery operation; namely, non-pulsating currents do not impose mechanical stress on the active electrode and thus make the design much more attractive than alternative single-switch buck-boost architectures. Moreover, the duty cycle waveform indicates the same operational point D2 = 0.16, which is also evident from the output voltage waveforms, as well as confirms the 100 kHz switching frequency of the converter.

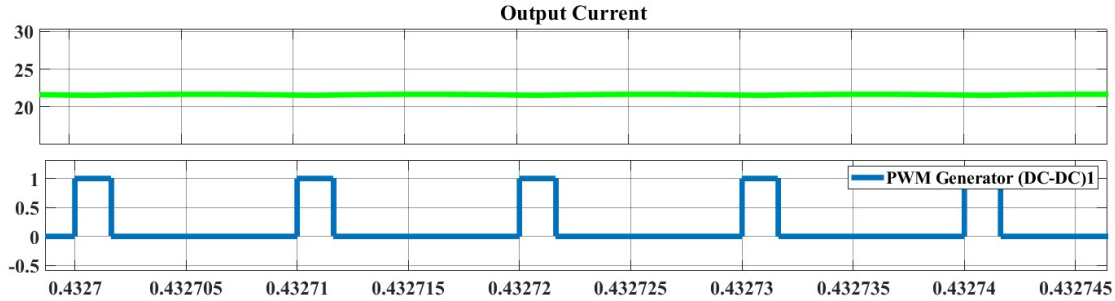

Fig 6.9: Simulation waveforms of
Buck Output Current

CHAPTER-7

CONCLUSION and FUTURE SCOPE

7.1 Conclusion

This thesis presented the design, analysis, and simulation of a 1 kW cascaded high-gain boost-buck DC-DC converter system intended for battery charging from a renewable energy source. One of the shortcomings that was tackled by the thesis is the voltage generated by PV arrays and fuel cell generators, which is relatively low and unregulated. For efficient charging of batteries, a regulated voltage must be obtained, but that voltage can have a totally different value than the one available from the sources mentioned above. A single-stage approach with only one degree of freedom is unable to achieve regulation of two voltages independently, hence justifying the design of the two-stage topology presented here. The proposed converter structure in this thesis is a non-isolated high gain boost converter. The configuration of the converter is based on the design proposed by Lin et al. It consists of two switches, three diodes, two inductors, and three capacitors. Control of the two switches is done using a single PWM signal. Expression for voltage gain $(3 – 2D) / (1 – D)^2$ yields a gain of 10 with D1 being 0.61; this is an average, practicable duty cycle value that avoids gain rolloff, saturation of the inductors and high level of conduction loss that plagues the conventional boost converter when trying to get similar gains above the duty cycle of 0.85. Voltage stresses of about 63 volts across S1 and 190 volts across S2 – both lower than the 300 V output – allow the design to be implemented using low voltage and low resistance MOSFET switches, hence the efficient performance of the stage. Simulations proved both inductors perform under CCM mode, with intermediate capacitor voltages conforming to the theoretical expression. Also, the closed-loop PI regulator kept the DC link constant at 300 V, free from any error.

Stage two is the buck converter which takes the regulated 300 V from the intermediate DC link and bucks it to the required battery terminal voltage. For the buck stage, the design included the implementation of a cascaded dual-loop PI controller where the outer loop is responsible for the regulation of the output voltage and the inner loop regulates the inductor current. This gives two independent control objectives for one power stage where the outer-loops control the voltage at the output irrespective of load changes while the inner-loops will control the current through the inductors and speeds up the response time. It is evident that according to the simulation results, the output voltage was regulated at 48 V without any output voltage ripple, the output current

remained constant at about 21.5 A, leading to output power at about 1032 W, satisfying the requirement of a 1 kW battery charger. S3 buck switch blocked 300 V in the off state and had a peak current rating of about 30 A, matching those of commercially available 400 V MOSFETs. A key observation in this study is that the 300 V intermediate DC link plays an additional function apart from transforming voltages. The intermediate DC link acts as a power buffer, capable of absorbing the mismatched power between the two stages; it acts as a decoupler in terms of isolating the dynamices on the source side from the load dynamics, hence any change in input due to PV will not affect the operation of the battery terminal and finally gives both controllers a static operating point. This last part is important in that without the intermediate DC link, a one-stage converter connecting the two different loads would be unable to regulate the two independent control variables using a single duty cycle as any linear control action would not resolve this issue.

The complete cascaded system demonstrates that the proposed architecture is capable of delivering regulated 1 kW of power from the 24V-30V renewable source to a 48 V battery load through a controlled 300 V intermediate bus, with each stage operating at a moderate duty cycle in its most efficient region. The three PI controllers -- one for the boost DC link and two for the buck voltage and current loops -- operate independently and without cross-coupling, confirming that the intermediate capacitor provides the necessary dynamic isolation between the stages. The overall design satisfies all the objectives set out at the beginning of this project work thesis the high voltage gain at moderate duty cycle, lower switch voltage stress, regulated DC link, independently regulated output voltage, and 1 kW power delivery capability.

7.2 Future Scope

Although the simulation studies discussed in this project-thesis proves the concept of the suggested cascaded converter topology both theoretically and experimentally, there are several areas remain open for further investigation, that can be further developed and studied.

7.2.1 Integration of Maximum Power Point Tracking (MPPT)

For the current system, a variable voltage source was used as the source for renewable energy inputs, and there was no inclusion of maximum power point tracking. With respect to a PV-driven charge controller, the PV panel input voltage and input current change with respect to time with variation in irradiance as well as the temperature of the cell. To obtain the maximum amount of power from the source, maximum power point

tracking needs to be considered in the charging scheme. Incorporation of the perturb and observe which is methond where the system is disturbed or incremental conductance algorithm in the boost stage control would introduce a third control loop in the system, where the reference value for the DC-link voltage will not be fixed at 300V but will keep varying depending on the input. The three-loop system structure for a PV battery charging system will be quite useful for the current decoupled design, whereby the MPPT control will control the duty ratio, D1, to give maximum power, whereas the buck control will still operate independently, and the intermediate capacitor will absorb the power differences between the stages.

7.2.2 Extension to Higher Power Levels

The 1 kW power level addressed in this thesis is appropriate for Level 1 domestic charging of small EVs and e-rickshaws. Extending the system to the 3.3KW, 6.6KW, or 22KW levels required for faster Level 2 charging involves scaling the passive components and switches proportionally, but also introduces new design challenges. At higher power levels the input current from the renewable source increases substantially, making input current ripple management more critical for MPPT accuracy. Interleaving two or more boost phases -- where multiple boost converter instances are operated with phase-shifted PWM signals -- would reduce the input current ripple without increasing individual component ratings, and would also improve the thermal distribution across the switching devices. The cascaded architecture proposed in this thesis is inherently compatible with interleaved first-stage operation, and investigating the optimal number of interleaved phases for a given power level and switching frequency is identified as a productive direction for future research.

7.2.3 Advanced Control Strategies

The PI regulators used in this project achieve an adequate level of regulation performance within the linear region of operation of the converter, but they are designed for a single operating point and their performance may deteriorate if they have to regulate the output for a higher variation in the input voltage or under significant disturbances. Various more advanced types of control can be considered to be enhanced for the performance of the converters. The control technique model predictive is able to optimize the trajectory of the duty cycle over the finite horizon, hence allowing achieving much faster dynamics and better regulation compared to the fixed gain controller under strong disturbances. The sliding mode approach is characterized by high robustness against parameter variations and nonlinearities, thus making it suitable for

implementing in the boost stage because of the existence of the right half plane zero, limiting the bandwidth of any linear control strategy. Various adaptive control algorithms could be developed which adjust the gains of the regulator according to the plant response during operation. Exploring various control algorithms in the proposed cascaded converter design is an important step towards advancing the design of converters for renewable sources.

7.2.4 Thermal Management and Efficiency

The simulations performed in this thesis assume that the behaviour of the components is ideal or close to it, and do not take into account any changes to the temperature profile of the converter when it runs continuously at full load. In a real-world 1 kW converter, the heat generated by conduction and also the switchin loss in MOSFETs, diodes, and inductors needs to be dissipated efficiently to avoid overheating of the components. A thermal analysis performed using finite element simulation or thermal imaging tests would determine which are the components generating most heat during worst-case operation, thus allowing to decide what types of heat sink, thermal interface materials and PCB copper pours are needed. Besides thermal management, the switching frequency can be optimised to minimise core loss in the inductors and switching loss in the MOSFETs, taking into account the fact that this tradeoff changes depending on the power output and the components chosen. Testing wide-bandgap semiconductors such as gallium nitride (GaN) MOSFETs as an alternative to the current silicon MOSFETs for the boost stage switches might also prove interesting because GaN MOSFETs have much less gate charge and on-resistance at the voltages applied to S1 and S2, and therefore might push the efficiency above 95% at 1 kW

7.3 Closing Remarks

This dissertation shows that combined two stage hiigh gainn boost buck dc-dc converter topology, a viable solution for achieving efficient battery charging operation from a renewable energy source at 1 kW power level. It is shown in the proposed circuit design that by using a two-stage dc-dc conversion approach, in which the task of voltage regulation at each stage is assigned to one control variable, the mismatch problem between the low and varying renewable energy source voltage level and the output battery regulated voltage can be effectively solved. The mathematical analysis, the circuit component design and control algorithm development all serve to show that the circuit achieves its objectives, including: DC link regulation at 300 volts, DC output regulation at 48V-1 kW power level, low duty cycle in both stages, low voltage rating of switches and independent and decoupled regulation of both outputs.

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