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COMPARATIVE ANALYSIS OF MODERN DIGITAL FILTER USED IN SEIG-DSTATCOM BASED DG FOR POWER QUALITY ENHANCEMENT

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CANDIDATE'S DECLARATION

I, Jatin Mann, Roll No 24/PES/04 student of M. Tech. in Power Electronics and Systems, Delhi Technological University, Delhi, hereby declare that the project Dissertation titled "**Comparative Analysis Of Modern Digital Filter Used In SEIG-DSTATCOM Based DG For Power Quality Enhancement**" which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the Degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any other Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "**Comparative Analysis Of Modern Digital Filter Used In SEIG-DSTATCOM Based DG For Power Quality Enhancement**" which is submitted by Jatin Mann, Roll No 24/PES/04 student of M. Tech. in Power Electronics and Systems, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the Degree of Master of Technology, is a record project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Localized renewable energy resources, essential for rural electrification and energy security, will be rapidly integrated to autonomous distributed generation networks worldwide. The three-phase SEIG is the most popular electromechanical generating unit for the isolated applications due to its rugged, brushless construction and low capital cost. However, autonomous SEIG microgrids are highly susceptible to the injection of high frequency discontinuous harmonic currents generated by non-linear loads. Such harmonics cause severe non sinusoidal voltage distortions at the Point of Common Coupling (PCC) risking to demagnetize generators, and violating the stringent 5.0% source current THD limit, as required by IEEE Std 519-2014. A shunt connected DSTATCOM is implemented with a new mathematical simplified digital control architecture to reduce such extreme power quality anomalies. The Synchronous Reference Frame Theory (SRFT) is the traditional basis for the active power conditioning. While mathematically correct, SRFT depends on extremely weak Phase Locked Loop (PLL) synchronization and Park's coordinate transformations. For low-inertia microgrids, these non-linear tracking loops are sensitive to loss of synchronization due to short voltage sags. The discontinuous Infinite Impulse Response (IIR) low-pass filters generate large asymptotic settling delays and delay the dynamic compensation. For overcoming these systemic mathematical constraints, the simulation and exhaustive evaluation of the Adaptive Vectorial Filter Theory (AVFT) control algorithm is especially designed for standalone SEIG networks. The logic of the AVFT arises from the stationary three-phase reference frame. Real time in-phase voltage unit templates are obtained and the optimized discrete Moving Average Filter (MAF) in one fundamental time cycle is aggregated to completely isolate the fundamental load weight and avoids being a recursive algorithmic phase lag. In the MATLAB/Simulink environment, a rigid side-by-side comparative analysis was made. In steady state condition SRFT controller reduced baseline uncompensated THD of 27.26% to 2.68%. However, the AVFT algorithm was able to reduce the source current THD to a highly optimized value of 1.97% which was better for harmonic neutralization. The results validate the better computational efficiency, dynamic agility of the MAF based AVFT architecture, and steady-state compliance for stabilizing highly volatile autonomous distributed generation systems.

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List of Symbols

S No.	Symbols	Description
1	C_{dc}	DC-Link Energy Storage Capacitance
2	C_{ex}	SEIG Excitation Capacitance (per phase)
3	f_{sw}	PWM Switching Frequency
4	h	Hysteresis Current Band Limit
5	I_m	Instantaneous Magnetizing Current
6	i_{ca}, i_{cb}, i_{cc}	DSTATCOM Injected Compensating Currents
7	i_d*, i_q*, i_0*	Reference Current Components in d-q-0 Frame
8	i_{La}, i_{Lb}, i_{Lc}	Non-Linear Load Currents
9	i_{loss}	Active Loss Current Component
10	i_{sa}, i_{sb}, i_{sc}	SEIG Grid Source Currents
11	K_{id}	Integral Gain of DC-Link PI Controller
12	K_{pd}	Proportional Gain of DC-Link PI Controller
13	L_f	Interfacing AC Coupling Inductance
14	L_{ls}	Stator Leakage Inductance
15	L_{lr}	Rotor Leakage Inductance
16	L_m	Mutual Magnetizing Inductance
17	L_L	Non-Linear Load Series Inductance
18	R_f	Interfacing Internal Resistance
19	R_r	Rotor Resistance
20	R_s	Stator Resistance / Transmission Line Resistance
21	R_L	Non-Linear Load Series Resistance
22	T_s	Discrete Fundamental Sample Time
23	T_w	Moving Average Filter Integration Window Time
24	u_a, u_b, u_c	In-Phase Voltage Unit Templates
25	V_{dc}	Instantaneous DC-Link Voltage
26	V_{dc}*	Reference DC-Link Voltage Target
27	V_m	Instantaneous Terminal Voltage Amplitude

28	v_{sa} v_{sb}, v_{sc}	PCC Terminal Phase Voltages
29	v_{ds}, v_{qs}	Voltages in synchronously rotating d-q frame
30	W_L	Fundamental Active Load Weight Scalar
31	W_{loss}	Internal Active Loss Weight Scalar
32	W_{total}	Total Active Power Weight Scalar
33	θ	Grid Voltage Phase Angle
34	ω_e	Electrical Angular Frequency
35	ω_m/ω_r	Mechanical Rotor Speed

List of Abbreviations

S No.	Abbreviated Name	Full Name
1	AC	Alternating Current
2	ADC	Analog-to-Digital Conversion
3	ALU	Arithmetic Logic Unit
4	AVFT	Adaptive Vectorial Filter Theory
5	AVR	Automatic Voltage Regulator
6	BESS	Battery Energy Storage System
7	DC	Direct Current
8	DFIG	Doubly Fed Induction Generator
9	DG	Distributed Generation
10	DSP	Digital Signal Processor
11	DSTATCOM	Distribution Static Compensator
12	EMF	Electromotive Force
13	FFT	Fast Fourier Transform
14	FIR	Finite Impulse Response
15	FLOPS	Floating-Point Operations per Second
16	FPGA	Field Programmable Gate Array
17	HIL	Hardware-in-the-Loop
18	IEEE	Institute of Electrical and Electronics Engineers
19	IGBT	Insulated Gate Bipolar Transistor
20	IHD	Individual Harmonic Distortion
21	IIR	Infinite Impulse Response
22	KCL	Kirchhoff's Current Law
23	LPF	Low-Pass Filter
24	MAC	Multiply-Accumulate
25	MAF	Moving Average Filter
26	PCC	Point of Common Coupling

27	PI	Proportional-Integral
28	PLL	Phase-Locked Loop
29	PV	Photovoltaic
30	PWM	Pulse Width Modulation
31	RMS	Root Mean Square
32	SEIG	Self-Excited Induction Generator
33	SMPS	Switch-Mode Power Supply
34	SRFT	Synchronous Reference Frame Theory
35	T&D	Transmission and Distribution
36	THD	Total Harmonic Distortion
37	UPS	Uninterruptible Power Supply
38	VCO	Voltage Controlled Oscillator
39	VFD	Variable-Frequency Drive
40	VSC	Voltage Source Converter

Chapter 1

INTRODUCTION

1.1 GENERAL ASPECTS

The sustainable advancement of modern industrial and domestic infrastructure is intrinsically tied to the continuous availability of reliable, high-quality electrical energy. For the last century, global electrification has been dominated by centralized, large-scale power generation plants, largely based on the combustion of fossil fuels like coal, oil, and natural gas. But the rapid depletion of these finite, carbon-based resources, combined with growing geopolitical anxieties over energy security and the catastrophic environmental consequences of greenhouse gas emissions, have compelled a shift in global energy policy thinking. Governments and international regulatory bodies are pushing aggressively to decarbonize the electrical grid through integration of renewable energy systems. [1], [2].

This global transformation is manifested in a radical transformation of the traditional architecture of the electric grid, which is characterized by a unidirectional flow of energy from large centralized plants to remote consumers through extensive transmission networks. The modern approach favours Distributed Generation (DG). DG is the use of small to medium scale power generation technologies located physically close to the end-user near the nodes of consumption. [3], [4]. DG frameworks also integrate localized renewable energy sources such as wind turbines, photovoltaic (PV) arrays, biomass engines and micro-hydroelectric turbines directly into the distribution network, drastically reducing the severe I2R transmission and distribution (T&D) losses that plague macroscopic centralized grids.

DG has two modes of operation: grid-connected (grid-tied) and autonomous (islanded/standalone) microgrids. For grid-tied applications, the DG unit is connected in parallel with the infinite utility bus which strictly controls the system voltage and frequency. But distributed generation is uniquely important in solving problems of rural and remote electrification [5]. In developing countries as well as in geographically isolated areas (like mountainous areas or remote islands) it is often not economically viable, or physically possible, to extend the national high voltage utility grid. Localized renewable-powered autonomous microgrids are the only practical means to drive socio-economic development, power essential healthcare services and support local agricultural sectors in these off-grid areas.

Autonomous microgrids are of great socio-economic value but pose great electrical engineering challenges. Instead of a large interconnected utility grid with huge rotational inertia that can smoothen sudden power fluctuations, an isolated distributed system operates with very low system inertia [6]. The delicate balance between the generation and consumption of active power can be easily disturbed. Autonomous microgrids are highly susceptible to abrupt load additions, prime mover intermittency (e.g., variable wind speeds or water flow), and the injection of harmonic distortions in relation to the terminal voltage, system frequency and overall power quality. The maintenance of dynamic stability and strict power quality in these weak low-inertia networks is the main motivation of advanced power electronics research [7].

1.2 STATE OF ART ON SEIG-FED MICROGRIDS AND POWER QUALITY

A review of the state of the art of generation technology, characteristics of modern electrical loads and contemporary remediation devices used in isolated networks is needed to lay a strong foundation for understanding the central problem addressed in this thesis.

1.2.1 State of Art on Self-Excited Induction Generators (SEIGs)

In remote micro-hydro and variable-speed wind energy applications, the selection of the electromechanical energy conversion unit is critical to harness

renewable kinetic energy. In the past, synchronous generators have been the dominant type of large-scale power plants. This is because synchronous generators intrinsically can control the terminal voltage via dedicated DC field excitation. Synchronous machines have complicated brush assemblies, slip rings which are subject to continuous mechanical wear and sensitive automatic voltage regulators (AVRs) which need frequent high skill maintenance.

The three-phase Self-Excited Induction Generator (SEIG) is a technology of choice in the state of art for stand-alone microgrids to overcome such mechanical and finance barriers [8], [9]. The SEIG has a standard squirrel-cage induction machine configuration that has unmatched structural and operational advantages. There are very few points of mechanical failure, with no brushes and slip rings at all. This is an extremely rugged, brushless and explosion proof design. SEIGs have much lower capital costs per kilowatt, require virtually no routine maintenance and have an inherent self-protection against terminal short circuits. A localised short-circuit instantly demagnetises the machine and the generation voltage falls safely to zero, without destroying the stator windings [4].

However, a squirrel-cage induction machine is not equipped with an independent DC field winding and can not generate an independent internal magnetic flux. The phenomenon of "self-excitation" is entirely dependent upon the existence of residual magnetism retained in the ferromagnetic core of the rotor [10]. When the rotor is mechanically driven by a prime mover at constant or variable speed, the cage bars cut this weak residual magnetic field and a small EMF of low frequency is induced in the stator windings.

To maintain this voltage and to raise it to a useful commercial level, an external source of leading reactive power (capacitive VARs) must be supplied. This is achieved by permanently connecting a localized, three-phase delta-connected excitation capacitor bank across the generator's stator terminals [11]. This positive feedback loop causes a rapid exponential increase in voltage until the magnetic flux density in the iron core of the generator reaches a non-linear saturation point. This results in a steady state terminal voltage.

This fixed capacitive excitation provides a reliable method of generating no load voltage but creates a severe vulnerability under loaded conditions [11]. The

fixed capacitor bank supplies a leading reactive power strictly proportional to the square of the operating terminal voltage. The load competes directly with the generator core for the capacitive VARs when the SEIG is driven under different electrical loads. This “VAR starvation” results in severe terminal voltage sags and, in case the reactive demand exceeds the critical excitation limit, in total voltage collapse [6].

1.2.2 State of Art on Non-Linear Loads and Harmonic Distortion

The inherent voltage vulnerability of the SEIG is severely exacerbated by the widespread proliferation of modern power-electronic interfaces. In contemporary industrial, commercial, and agricultural sectors, traditional "linear" loads (such as incandescent lighting and direct-on-line induction motors, which draw sinusoidal current) are systematically being replaced by highly efficient but highly polluting "non-linear" topologies [12]. Typical examples include variable-frequency motor drives (VFDs), industrial switch-mode power supplies (SMPS), and battery charging stations.

These power electronic devices operate by rapidly commutating solid-state semiconductor switches to chop and shape the incoming electrical waveform. The most common industrial non-linear load is the three-phase uncontrolled diode bridge rectifier. Because the anti-parallel diodes conduct sequentially only when the instantaneous line-to-line AC voltage exceeds the corresponding DC-link potential of the load, the AC line currents drawn by the rectifier are forced into discontinuous, quasi-square blocks with steep leading and trailing edges (di/dt) [12], [13].

According to Fourier analysis theory, any non-sinusoidal periodic waveform can be mathematically decomposed into a fundamental frequency component and an infinite series of high-frequency components oscillating at integer multiples of the fundamental frequency, known as harmonics. A standard six-pulse diode bridge rectifier injects severe concentrations of low-order, non-triplen odd harmonics back into the distribution grid, predominantly the 5th, 7th, 11th, and 13th orders [14].

These harmonic loads will cause large local non-sinusoidal voltage drops and distort the terminal voltage waveform at the Point of Common Coupling (PCC) in a weak SEIG system with large internal stator leakage impedance [15]. The consequences are: thermal degradation of the stator insulation, mechanical fatigue on

the generator shaft due to pulsating electromagnetic torques and catastrophic control malfunction of the parallel connected diagnostic equipment .

1.2.3 State of Art on Distribution Static Compensators (DSTATCOMs)

To avoid these severe power quality disturbances, stringent compliance limits are enforced internationally. The most prominent one is the IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems, IEEE Std 519-2014 [16], which requires that the Total Harmonic Distortion (THD) of the source current be rigorously kept below 5.0% [17].

Power engineers have traditionally used passive L-C filters to suppress certain harmonic frequencies. However, passive filters are structurally rigid and can only filter fixed harmonic orders. Passive filters are detuned if the microgrid fundamental frequency changes (which is a common phenomenon in low inertia SEIG systems) and can cause dangerous parallel resonance anomalies [18], [19].

To overcome these limitations, the state of the art today is based on custom power devices based on active power filtering topologies. The Distribution Static Compensator (DSTATCOM) is the best shunt active compensating technology [20], [21]. The DSTATCOM is connected in parallel with the offending non-linear load at PCC. The main operational mandate of the DSTATCOM is to intelligently sense the load's distorted current requirements in real time and quickly synthesize and inject an equal and opposite compensating current profile directly into the grid node [22].

The hardware architecture depends on a solid state three phase Voltage Source Converter (VSC) using Insulated Gate Bipolar Transistors (IGBTs). The DC side is terminated across a high-capacity DC-link capacitor, acting as an instantaneous energy buffer. The DSTATCOM provides the harmonic and reactive power demands of the local load and ensures that the generator provides only pure sinusoidal active power [23], [24].

1.3 OBJECTIVES AND SCOPE OF WORK

The DSTATCOM physical hardware is only the actuator, its mitigation performance and dynamic agility are totally defined by the mathematical control algorithm driving its reference current generation architecture [25]. The most popular

algorithm is classical Synchronous Reference Frame Theory (SRFT) [26], [27]. However, SRFT relies on computation-intensive coordinate transformations and Phase-Locked Loops (PLLs) that are sensitive to loss of synchronization in weak microgrids.

The main objective of this Master of Technology research work is to design, model and analyze an advanced PLL free active power quality conditioning scheme AVFT to stabilize an autonomous SEIG system so as to do away with these systemic restrictions [28]. The overall objectives are systematically translated into the following scopes of work:

1.3.1 Mathematical Modelling and Simulation Setup

- To develop a complete mathematical and physical simulation model of an autonomous distributed generation framework in MATLAB/Simulink environment.
- To implement a 7.5 kW squirrel-cage induction machine operating as an SEIG, finding the localized capacitance sizing required for ideal standalone voltage build-up.
- To model a highly distorting three-phase uncontrolled diode bridge rectifier terminating into a heavy inductive R-L branch, creating a severe harmonic baseline that violates IEEE grid codes.

1.3.2 Implementation of SRFT Control Strategy

- To formulate and deploy the classical SRFT reference current generation algorithm as a baseline comparative metric.
- To integrate a Three-Phase PLL for continuous angular phase tracking (theta) of the highly sensitive SEIG terminal voltage.
- To execute forward and inverse Park's coordinate transformations (a-b-c to d-q) to isolate the active load components using digital Low-Pass Filters (LPFs).
- To design a closed-loop Proportional-Integral (PI) controller to regulate the internal DSTATCOM DC-link voltage against switching losses.

1.3.3 Development of the AVFT Architecture

- To formulate, design, and mathematically implement the AVFT algorithm within the stationary reference frame.

- To completely eliminate the vulnerable PLL by deriving raw, real-time in-phase voltage unit templates directly from the PCC terminal voltages.
- To replace the lagging digital low-pass filters with a discrete MAF integrated over exactly one fundamental time period (0.02 seconds) to achieve instantaneous active weight extraction without high-frequency leakage.
- To generate accurate PWM gating signals utilizing a hysteresis current tracking controller driven by the newly synthesized reference currents.

1.3.4 Comparative Harmonic and Dynamic Analysis

- To carry out a complete comparative study of SRFT and AVFT algorithms for steady state operation and dynamic step load transients.
- The source current was qualitatively analyzed by FFT spectrum analysis and the attenuation of the 5th, 7th, 11th and 13th harmonic orders was estimated.
- To guarantee that the AVFT architecture can efficiently reduce the source current THD to below the 5.0% threshold provided by the international IEEE Std 519-2014 standard with higher computational efficiency than the conventional SRFT methodology.

1.4 OUTLINE OF CHAPTERS

This dissertation is presented in a systematic way and consists of six separate chapters to present the research findings, mathematical derivations and simulation data in a highly structured, coherent and rigorous academic format. The thesis is organized as follows:

- Chapter-1: “INTRODUCTION” provides an introduction to the primary field of research. It reviews the worldwide trend of distributed generation and presents a detailed state-of-the-art review of SEIG electro-mechanics, non-linear harmonic pollution as well as DSTATCOM hardware. Find the research gap in conventional control algorithms. Explain the objectives and scope of the thesis in detail.
- Chapter-2: “SIMULATION ARCHITECTURE AND SYSTEM CONFIGURATION” provides the detailed physical parameters, hardware topologies and mathematical differential equations governing the individual subsystems of the isolated microgrid. It presents the structural sizing rules of the

main generation stage, distribution transmission lines, excitation capacitors and active power conditioning components (DC-link bus and AC coupling inductors).

- Chapter-3: “FORMULATION AND EVALUATION OF SRFT CONTROL ARCHITECTURE” presents the main algorithmic derivations of the classical mitigation approach. It gives a complete mathematical derivation step by step of the Clarke and Park coordinate matrix mappings, PLL dynamics and digital low pass filtering. The simulated steady state performance is then presented and the inherent computational and dynamic bottlenecks of the SRFT method are critically discussed.
- Chapter-4: “DESIGN AND IMPLEMENTATION OF AVFT ALGORITHM” describes the mathematical evolution and paradigm shift of the AVFT. It provides a detailed analysis of the transfer function mechanisms of the discrete MAF and shows the mathematical way to avoid the PLL by generating the unit template. Finally, the paper is concluded with steady state simulation waveforms which validates the control logic.
- Chapter-5: “COMPARATIVE PERFORMANCE ASSESSMENT AND HARMONIC ANALYSIS” is the analytical core and the experimental validation of the dissertation. It directly compares the performance of the SRFT and AVFT algorithms with respect to four aspects: steady-state waveform fidelity, speed of the transient response for step-load additions, algorithmic execution complexity and quantitative THD reduction measures based on FFT spectral analysis.
- Chapter-6: “MAIN CONCLUSION AND FUTURE RESEARCH SCOPE” summarizes the major technical contributions of this research project, provides a final conclusive verdict on the superiority of the AVFT controller. It then offers strategic suggestions and directions for future researchers interested in extending this work, such as deploying the architecture on physical FPGA/DSP hardware testbeds, or testing the system against severe single-phase unbalanced loading conditions.

Chapter 2

SIMULATION ARCHITECTURE AND SYSTEM CONFIGURATION

2.1 INTRODUCTION TO THE SIMULATION ENVIRONMENT

The physical prototyping of multi-kilowatt electrical networks in today's power electronics and microgrid research is limited by prohibitive capital costs, severe safety constraints, and a lack of flexibility for rapid algorithmic testing. Therefore, high quality digital simulation environments are essential to the development and validation of advanced active power conditioning systems [5], [6]. The entire autonomous SEIG microgrid and the associated DSTATCOM control architecture have been designed, assembled and simulated using MATLAB/Simulink software ecosystem.

In particular, the system is constructed with the Simscape Electrical (Specialized Power Systems) library. This work uses the thoroughly validated, block-level simulation components in the Simulink library instead of developing custom mathematical state-space differential equations from first principles. This approach allows a very accurate representation of physical electrical components—such as induction machines, semiconductor switches, and passive elements—while concentrating the main research effort on design and execution of control algorithms (SRFT and AVFT) [20].

The whole simulation architecture is logically divided into the following main block assemblies:

- Generation Assembly: The SEIG block and its local capacitive excitation block.

- Distribution Assembly: The small line transmission segments.
- Load Assembly: The non-linear diode bridge rectifier block and the components on the DC side as required.
- DSTATCOM Power Stage: The Voltage Source Converter (VSC) block, the DC link capacitor and the interfacing inductors.
- Control and Measurement Layer: This layer is responsible to control the voltage/current signals to the digital filter subsystems and generate PWM gating pulses.

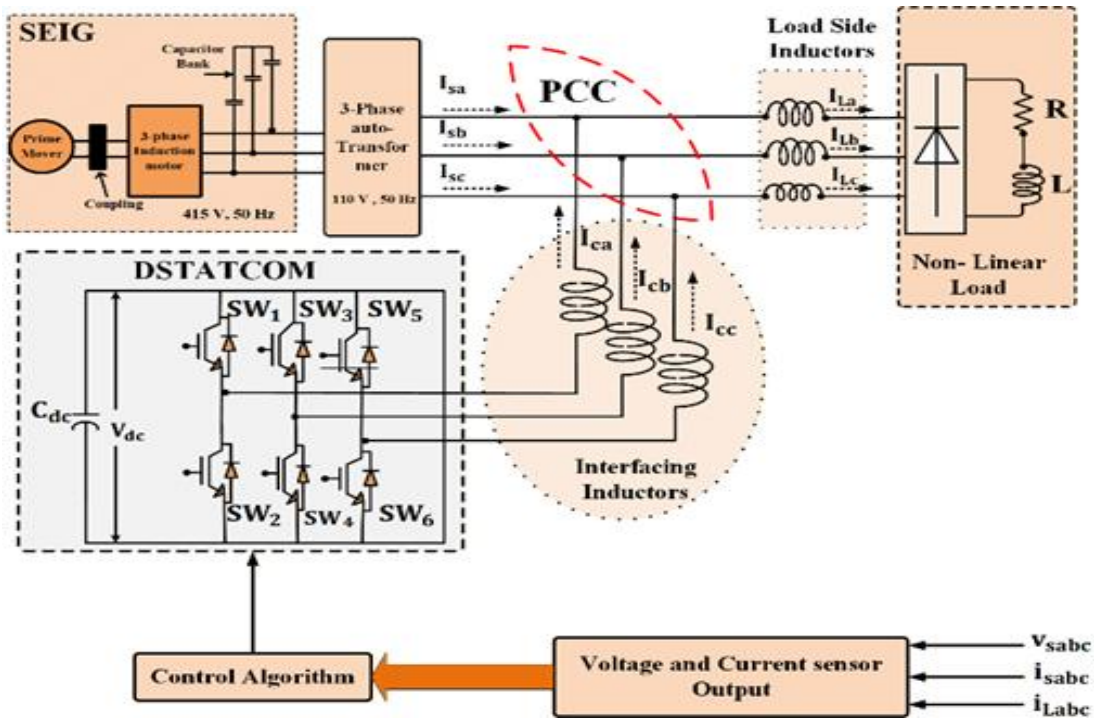


Fig. 2.1 Schematic Diagram of SEIG-Fed Autonomous Microgrid Interfaced with a Shunt DSTATCOM.

2.2 SIMULATION SOLVER AND POWERGUI CONFIGURATION

The simulation solver configuration and the inclusion of the powergui environment block are the fundamental backbone of any Simscape Electrical model. Because of the strong non-linearities in the system (e.g. diode commutations and high frequency IGBT switching), the proper solver mechanism has to be selected to avoid numerical divergence and simulation failure.

In this work the discrete simulation environment is employed to solve the continuous time physical electrical network. The central powergui block is placed at the top level of the Simulink canvas and the type of simulation is set to “Discrete”. The fundamental discrete sample time (T_s) is strictly parameterized with 10 μs to accurately capture the high frequency 10 kHz PWM switching transients of the DSTATCOM [20].

The solver is set to a fixed-step discrete formulation in the main Simulink Model Configuration Parameters (Ctrl+E). This guarantees that the digital control algorithms (SRFT and AVFT) are performed with the exact chronological accuracy as would be the case when a physical Digital Signal Processor (DSP) or microcontroller would process the sampled data during a real hardware implementation [35]. In addition, the powergui block is the main diagnostic tool for the post-simulation analysis including the FFT Analysis tool which is required to compute the THD of the generator source currents.

2.3 CONFIGURATION OF THE SEIG SIMULATION BLOCK

The basic border of the autonomous network is the main energy generation phase. The SEIG is represented by the block Asynchronous Machine SI Units from the Specialized Power Systems library [5].

Since the SEIG is physically a standard squirrel-cage induction machine, the block is configured by setting the "Rotor Type" parameter to "Squirrel-Cage". The mechanical input of the block is configured to receive a constant rotational speed (ω_m) rather than mechanical torque, simulating a tightly governed prime mover (such as a regulated micro-hydro turbine) [8]. A constant block is connected to the 'ω_m' port, parameterized to the synchronous speed of 1500 RPM (converted to rad/s).

The electrical parameters of the 7.5 kW, 415 V, 50 Hz machine are entered directly into the block’s parameter dialog box. These include the stator resistance (R_s = 1.15 Ω), stator leakage inductance (L_{ls} = 0.0059 H), rotor resistance (R_r = 1.05 Ω), and rotor leakage inductance (L_{lr} = 0.0059 H).

In fact, it is necessary to model the magnetic saturation of the machine to simulate the phenomenon of auto-excitation in the Simulink environment. The

"Simulate saturation" check box in the advanced tab of the Asynchronous Machine block is selected. Input is a matrix of values of non-linear relation between magnetizing current (I_m) and terminal voltage. The saturation curve prevents the internal simulated voltage from going to infinity during the build-up phase of the excitation [6].

2.4 IMPLEMENTATION OF THE EXCITATION CAPACITOR BANK

The Asynchronous Machine block can not produce its own magnetic field, so it requires an external source of leading reactive power. This is done in the simulation by constructing an excitation capacitor bank across the three stator output terminals (A, B, C) [4], [11].

The capacitor bank is realized by the Three-Phase Series RLC Load block. The "Branch type" parameter is set to "C" (Capacitance) only to make this block a pure capacitive bank. Nominal frequency is taken as 50 Hz and nominal voltage between phases is taken as 415 V.

This allows the Delta (δ) configuration required for optimal reactive power provision to be specified in the internal block routing. Alternatively, three single phase discrete capacitor blocks can be wired manually node-to-node (A-B, B-C, C-A). The parameter of capacitive reactive power (Q_c) is computed and chosen as 30 μF/phase. This particular value ensures that the simulation clears the initial algebraic loop and ramps up the nominal terminal voltage correctly during the first 0.2 seconds of simulation run without exceeding the generator saturation limits [6].

2.5 TRANSMISSION LINE NETWORK INTEGRATION

The electrical energy generated at the SEIG stator terminals is delivered to the PCC through a distribution line. The short-distribution line is modelled in the simulation by the "Three-Phase Series RLC Branch" block [1].

This block is directly placed in series between the SEIG output measurement nodes and the PCC load nodes. The "Branch type" is "RL" which is the lumped series resistance and series inductance of the physical copper or aluminium

conductors. The resistance parameter is taken as 0.1 Ω, and the inductance parameter is considered as 0.5 mH.

Now these values are relatively small but are absolutely critical for the validity of the simulation. This R-L block provides the required series impedance so that the discontinuous harmonic currents of the non-linear load led to measurable and realistic voltage drops and distortions at the PCC. Otherwise, the terminal voltage of the SEIG would be unrealistically “stiff” within the scope of the simulation.

2.6 SIMULATION OF THE NON-LINEAR INDUSTRIAL LOAD

A highly distorting power-electronic load profile is simulated to test the performance of DSTATCOM algorithms in terms of mitigation [12]. This is done using the Universal Bridge block of the Specialized Power Systems library.

The Universal Bridge block is a very generic block. The parameter “Power Electronic device” in the drop-down menu is set to “Diodes” to simulate an uncontrolled industrial rectifier. There are 3 “bridge arms”. The three phase PCC nodes are directly connected to the three AC input terminals of the bridge.

To serve the non-linear load profile, a sink has to be introduced on the DC side of the system across the positive and negative output terminals of the Universal Bridge. This is modelled by a standard Series RLC Branch block. "RL" branch type, representing a heavy industrial load is taken. The resistance value is 40 Ω, and an inductance of 100 mH is used.

The simulated DC current is very smooth due to high inductance on DC side. In consequence, the Universal Bridge block will take current from the AC side in steep quasi-square pulses. These line currents are sent to a Simulink Scope where the typical 120-degree conduction blocks are shown and successfully simulate the severe 5th, 7th, 11th and 13th harmonic injections that are needed to test the DSTATCOM [12], [44].

2.7 CONSTRUCTION OF THE DSTATCOM POWER STAGE

The hardware unit of the DSTATCOM, connected in parallel to the non-linear load at PCC, is the physical actuator of the active power conditioning system

[7]. The power stage is modelled in Simulink with three blocks corresponding to the three components:

- VSC: Another Universal Bridge block is used for the converter. The parameter “Power Electronic device” for DSTATCOM is chosen as “IGBT/Diodes” unlike the load rectifier. Hence the block represents an active controllable 6 pulse converter. The block adds a new input port ('g') to receive the Boolean PWM gating pulses created by the SRFT or AVFT control algorithms [15].
- DC-Link Energy Storage: A Parallel RLC Branch block is connected in parallel to the DC output terminals of the IGBT Universal Bridge. The branch type is fixed to be "C" (Capacitance) [7]. The capacitance value is parameterized to 2200μF. The "Set initial capacitor voltage" is checked to avoid startup transients and algebraic loop errors in the simulation solver, and the value is initialized to the steady state target of 700 V.
- Interfacing Coupling Inductors: VSC AC output terminals are connected back to the grid PCC using a Three Phase Series RLC Branch block. "RL" branch is taken where the inductance (L_f) is considered as 3.5 mH, acting as LPF to block the 10 kHz PWM switching noise from entering grid and internal resistance (R_f = 0.1 Ω) simulates the copper losses of the physical inductor [20].

2.8 SIGNAL MEASUREMENT AND DATA ROUTING ARCHITECTURE

A sophisticated control algorithm cannot function without accurate, real-time data acquisition. In the Simulink model, this is achieved using the Three-Phase V-I Measurement blocks [14].

Two measurement blocks are deployed:

- Source Measurement: Placed after the SEIG and transmission line to capture grid terminal voltages (V_{sabc}) and generator source currents (i_{sabc}).
- Load Measurement: Placed before diode bridge to capture distorted load currents (i_{Labc}).

The outputs of these measurement blocks are vector signals which are bundled. They are directed to Demux (Demultiplexer) blocks, where they are split into separate phase A, B, and C signals. These continuous signals are then passed through Zero-Order Hold blocks (with 10 μs sample time) before being fed into the digital control subsystems. This is a good model of the ADC process of a real DSP [35].

The signals are passed to Scope blocks for real time visualization. Thus, the voltage, source current, load current and DSTATCOM compensating current can be observed together. The source current signal is also sent to a To Workspace block. This step is important because it exports the time-series simulation data into the MATLAB workspace environment so the powergui FFT tool can access the array and generate THD bar charts [17].

2.9 COMPREHENSIVE SIMULATION PARAMETERS MATRIX

For a firm, reproducible basis for the advanced digital simulations and control algorithm studies of the subsequent chapters, the exact block parameters entered in the Simulink workspace are summarized in an orderly fashion below. These parameters were carefully selected and tuned to make the simulation representative of highly stressed microgrid realistic operating conditions [6], [20].

Table 2.1 Complete Simulink Block Parameterization Matrix.

Simulink Component Block	**Programmed Parameter**	**Assigned Value**
powergui Block	Simulation Type	Discrete
	Sample Time (T_s)	1e−5 s (10μs)
Asynchronous Machine	Nominal Power, Voltage, Freq.	7.5 kW, 415 V, 50 Hz
	Rotor Type	Squirrel-Cage
	Stator Resistance (R_s)	1.15 Ω
	Stator Leakage Inductance (L_{ls})	0.0059 H
	Rotor Resistance (R_r)	1.05 Ω

	Rotor Leakage Inductance (L_{lr})	0.0059 H
	Mechanical Speed Input	157.08 rad/s (1500 RPM)
Excitation Bank	Capacitive Reactive Power (Q_c)	Configured for 30 μF per phase
Line Impedance	Series Resistance (R_s)	0.1 Ω
	Series Inductance (L_s)	0.5 mH
Universal Bridge (Load)	Power Electronic Device	Diodes
Load DC Branch	Series Resistance (R_L)	40 Ω
	Series Inductance (L_L)	100 mH
Universal Bridge (VSC)	Power Electronic Device	IGBT / Diodes
DSTATCOM DC-Link	Parallel Capacitance (C_{dc})	2200 μF
	Initial Voltage Parameter	700 V
DSTATCOM AC Filter	Series Inductance (L_f)	3.5 mH
	Series Resistance (R_f)	0.1 Ω
PWM Generator Block	Carrier Frequency (f_{sw})	10 kHz

This elaborate architecture review explicitly described the construction of autonomous microgrid in the simulation environment. The Simulink framework with all physical components instantiated, parameterized and measured well is thus ready for the evaluation of the dynamic tracking and harmonic mitigation capabilities of the SRFT and AVFT subsystem blocks presented in the following chapters.

Chapter 3

FORMULATION AND EVALUATION OF SRFT CONTROL ARCHITECTURE

3.1 INTRODUCTION TO THE SRFT CONTROL ALGORITHM

The efficiency of DSTATCOM to suppress severe power quality disturbances in simulation environment strictly depends on the mathematical accuracy, speed of implementation and dynamic stability of the reference current generation algorithm [25]. In the software, the control strategies of active power conditioners are generally classified into two categories, frequency-domain and time-domain. Frequency domain methods, e.g. based on the FFT, detect harmonic components continuously over a number of cycles of the grid waveform. Although frequency domain algorithms are very accurate in the steady state, they require large computational arrays that result in unacceptable processing delays and thus are not suitable for real-time transient compensation [28].

Therefore, control strategies in the time domain are far more suitable for discrete digital signal processing (DSP) simulation. Among these is the SRFT (known as the d-q control algorithm), the industry standard mathematical framework for fundamental active component extraction [26], [27].

The basic Philosophy of SRFT is based on orthogonal coordinate space transformations. The three-phase alternating grid voltages and load currents of a three-phase microgrid in steady state are expressed as time-varying space vectors rotating on stationary geometric plane. In conventional digital filters, high frequency harmonic

ripples are directly filtered from these continuously oscillating sinusoidal vectors, leading to severe phase shifts and tracking errors [25].

To overcome this mathematical limitation, the SRFT performs a transformation in which the three phase stationary coordinate variables are transformed into a two axis synchronously rotating reference frame (d-q-0). A fundamental mathematical simplification occurs when the axes of the algorithm rotate in exact synchronism with the fundamental frequency of the grid voltage: the time-varying fundamental active and reactive current components are directly transformed in stationary, time-invariant DC scalar quantities. However, the non-sinusoidal harmonic components show up as high frequency AC ripples riding on the steady DC base. This allows simple digital LPFs to extract the active current components with high mathematical fidelity [28].

3.2 MATHEMATICAL FORMULATION OF COORDINATE TRANSFORMATIONS

The implementation of the SRFT algorithm in the digital control subsystem relies on a rigid multi-step matrix mapping process. In the first step the measurement blocks at the PCC sample the highly distorted, non-linear load currents (i_{La}, i_{Lb}, i_{Lc}) continuously [27].

Mathematically the transformation is performed by two successive matrix operations. First, the three-phase a-b-c coordinates in stationary coordinates are converted into two-phase orthogonal stationary coordinates (α-β) using the Clarke Transformation matrix. Zero-sequence component (0) is also extracted to account for mathematical unbalances. This operation is expressed in Equation (3.1).

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \\ i_{L0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3.1}$$

Following the Clarke transformation, the stationary orthogonal vectors ($i_{L\alpha}$, $i_{L\beta}$) are mapped onto the synchronously rotating reference frame to derive the direct (d) and quadrature (q) axis currents [26]. This is achieved using the Park's

Transformation matrix, which requires instantaneous, real-time knowledge of the grid voltage phase angle (θ), given in Equation (3.2).

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{3.2}$$

When algorithmically combined into a single direct transformation matrix from the a-b-c frame, the complete calculation block is defined in Equation (3.3).

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \\ i_{L0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3.3}$$

Once transposed into the d-q domain, the direct and quadrature axis currents mathematically decouple into two distinct frequency spectrums:

$$i_{Ld} = i_{Ld(DC)} + i_{Ld(AC)} \tag{3.4}$$

$$i_{Lq} = i_{Lq(DC)} + i_{Lq(AC)} \tag{3.5}$$

The components $i_{Ld(DC}$ and $i_{Lq(DC)}$, calculated using Equation (3.4) and (3.5) respectively, represent the fundamental active and reactive power demanded by the non-linear load model, respectively. The high-frequency oscillatory terms $i_{Ld(AC)}$, $i_{Lq(AC)}$ encompass the complete harmonic pollution spectrum calculated by the software solver.

3.3 PHASE-LOCKED LOOP (PLL) ALGORITHMIC DYNAMICS

If the coordinate frame is not rotating in absolute synchronism with the PCC voltage vector, the active and reactive current arrays will be mathematically cross-coupled and will cause serious computational errors. In the simulation, the phase angle is continuously extracted using the three-phase synchronous reference frame phase-locked loop (SRF-PLL) algorithm [14], [39].

The SRF-PLL is digital feedback closed loop system composed of three logical stages: a Phase Detector (PD), a discrete Loop Filter (LF) and a discrete Integrator that corresponds to a Voltage Controlled Oscillator (VCO). The three phase terminal voltages (V_{sa}, V_{sb}, V_{sc}) are sampled by the PLL and converted to the d-q voltage frame (V_{sd}, V_{sq}) through the internal Park transformation.

The basic algorithmic goal of the SRF-PLL is to make the quadrature-axis component of voltage (V_{sq}) to be zero. When $V_{sq} = 0$, the direct-axis of the rotating reference frame is perfectly aligned with the fundamental terminal voltage vector. The error signal V_{sq} is fed into a discrete Proportional-Integral (PI) Loop Filter, which attenuates high-frequency noise and computes the estimated instantaneous angular frequency (ω_e) at discrete time step n, given by Equation (3.6).

$$\omega_e[n] = \omega_{ff} + K_{p\_pll}.v_{sq}[n] + K_{i\_pll}\sum_{k=0}^{n} v_{sq}[n].T_s \quad (3.6)$$

Where ω_{ff} is the feed-forward nominal angular frequency 314.15 rad/s, T_s is the discrete sample time 10 µs, and K_{p_pll} and K_{i_pll} are the tuned gains of the PLL algorithm. The output frequency array is then passed to a discrete digital integrator block, which continually calculates the phase angle (θ), using Equation (3.7), required for the coordinate transformations.

$$\theta[n] = \theta[n-1] + \omega_e[n].T_s \quad (3.7)$$

The algorithm applies a modulo-2π operation to the integrator output to ensure the angle bounds correctly between 0 and 2π radians [14].

3.4 DIGITAL EXTRACTION FILTERS AND ACTIVE POWER LOSS ESTIMATION

To isolate the fundamental active component from the transformed direct-axis load current, i_{Ld} is routed through a discrete second-order Infinite Impulse Response (IIR) LPF. This digital filter is programmed with a stringent cutoff frequency f_c tuned significantly below the fundamental frequency (typically 10 Hz). The mathematical transfer function of this filter effectively suppresses the high-frequency AC harmonic ripples $i_{Ld(AC)}$, extracting the pristine fundamental DC baseline $i_{Ld(DC)}$ [28].

While the LPF isolates the active power demand of the load, the DSTATCOM simulation model itself requires active power to maintain its internal DC-link voltage against mathematically simulated switching losses. A dedicated closed-loop PI controller computes this required loss weight.

Equation (3.8) gives the instantaneous error (ΔV_{dc}) between the dynamically measured DC-link voltage V_{dc} and the 700 V reference voltage (V_{dc}^{*}) at every sampling instance.

$$\Delta V_{dc}[n] = V_{dc}^{*} - V_{dc}[n] \tag{3.8}$$

This error array is processed by the DC-link PI controller to synthesize a dedicated active loss current component (i_{loss}), defined in the discrete z-domain as in Equation (3.9).

$$i_{loss}[n] = i_{loss}[n-1] + K_{pd}(\Delta V_{dc}[n] - \Delta V_{dc}[n-1]) + K_{id}\Delta V_{dc}[n] \tag{3.9}$$

This active loss current scalar is algebraically added to the filtered fundamental direct-axis load current, mathematically expressed by Equation (3.10), to compute the total reference direct-axis current (i_d^{*}) required from the SEIG model.

$$i_d^{*} = i_{Ld(DC)} + i_{loss} \tag{3.10}$$

Concurrently, because the SEIG mathematically relies entirely on capacitive VARs from its terminal capacitor block to maintain self-excitation, the generator must not supply reactive current to the non-linear load. The algorithm enforces this by setting the quadrature-axis reference source current (iq*) to be identically zero, represented in Equation (3.11).

$$i_q^{*} = 0 \tag{3.11}$$

Under balanced conditions the zero-sequence reference (i0*) is also held at zero. The control architecture mathematically ensures unity power factor operation by commanding i_q^{*} to zero such that the SEIG supplies pure active power only [27].

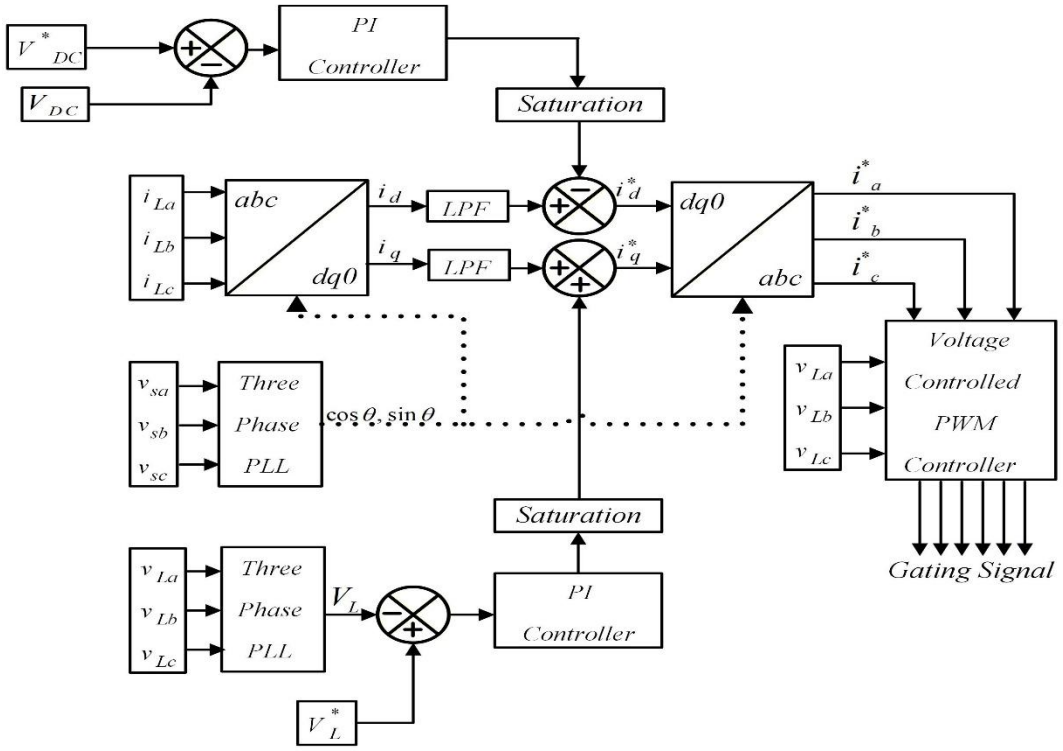


Fig. 3.1 Block Diagram of the Synchronous Reference Frame Theory (SRFT) Algorithm.

3.5 REFERENCE CURRENT INVERSE MAPPING AND HYSTERESIS LOGIC

The algorithm must convert d-q reference commands (i_d^*, i_q^*, i_0^*) back into the stationary AC domain to generate the physical gating references. Equation (3.12) gives how this is achieved via the Inverse Park's Transformation matrix.

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \cos\theta & 1/\sqrt{2} \\ \sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{2\pi}{3}\right) & 1/\sqrt{2} \\ \sin\left(\theta + \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \\ i_0^* \end{bmatrix} \tag{3.12}$$

The reconstructed stationary reference current arrays (i_{sa}^*, i_{sb}^*, i_{sc}^*) determine the exact ideal sinusoidal source current pattern. A discrete hysteresis current control algorithm is performed to make the VSC to inject currents to grid to this profile.

The simulated source currents (i_{sa}, i_{sb}, i_{sc}) are fed back into controller, and an error array ($\Delta i_k[n]$) is computed using Equation (3.13).

$$\Delta i_k[n] = i_{sk}^*[n] - i_{sk}[n] \qquad for\ k \in \{a, b, c\} \tag{3.13}$$

The hysteresis logic algorithm evaluates this error against a programmed boundary band ($\pm h$). The switching logic operates as a discrete Boolean evaluation.

- If $\Delta i_k[n] \geq +h$, the algorithm sets the gating variable S_k = 0 (Turn lower switch ON, upper OFF), decreasing the current trajectory.
- If $\Delta i_k[n] \leq -h$, the algorithm sets the gating variable S_k = 1 (Turn upper switch ON, lower OFF), increasing the current trajectory.

The mathematical bang-bang control loop guarantees the injected compensating current follows the calculated reference profile correctly at a variable switching frequency, mathematically limited around the 10 kHz threshold [20].

3.6 SIMULINK REALIZATION OF THE SRFT BLOCK

The SRFT was mathematically defined in Simulink, where the basic set of math operation blocks were used instead of switching to external toolboxes. This will provide absolute transparency and absolute control of integration solver's behaviour.

The three-phase load currents (i_{Labc}) are fed into a "Math Function" block array with all the blocks programmed for Matrix Multiplication (Park transformation) inside the SRFT Subsystem block. The transformation matrix is generated by the "Trigonometric Function" block with the sine and cosine inputs coming from the dedicated SRF-PLL subsystem that passes the θ value directly.

The d-axis current passes through a "Discrete Filter" block, set to be a second order Butterworth LPF. The "Discrete PID Controller" block is used to implement the DC-link PI controller—an easy-to-use block where the proportional (P) path is completely separate from the integral (I) path for a precise method to tune the controller gains. Standard “Add” blocks add the outputs, which propagate through the inverse matrix multiplication array and then to a “Relay” block set up as the hysteresis band controller and connected to the Universal Bridge “g” port, which generate the logical 0 and 1 signals.

3.7 STEADY-STATE SIMULATION PERFORMANCE

The algorithmic logic was validated by using the SRFT controller in the SEIG fed micro grid simulation system. The SRFT controller was used in the SEIG fed micro grid simulation system to ensure the algorithmic logic. To ensure that some initial self-excitation mathematical loops were allowed to settle, prior to start of active compensation, the simulation solver was programmed to run for 2.0 seconds.

Before compensation, the uncompensated load block is a very heavy-duty mathematical current sink that sucks up in cloudiness, with discontinuities, and arrays of highly distorted data. These high di/dt current pulses cause large sinusoidal-like voltage notches at the simulated PCC due to the inductive transmission line differential equations.

When the SRFT control algorithm is initialized, the logical VSC block starts synthesizing and injecting the calculated compensating currents straight away. The steady-state simulation waveforms vividly confirm the performance of the algorithm.

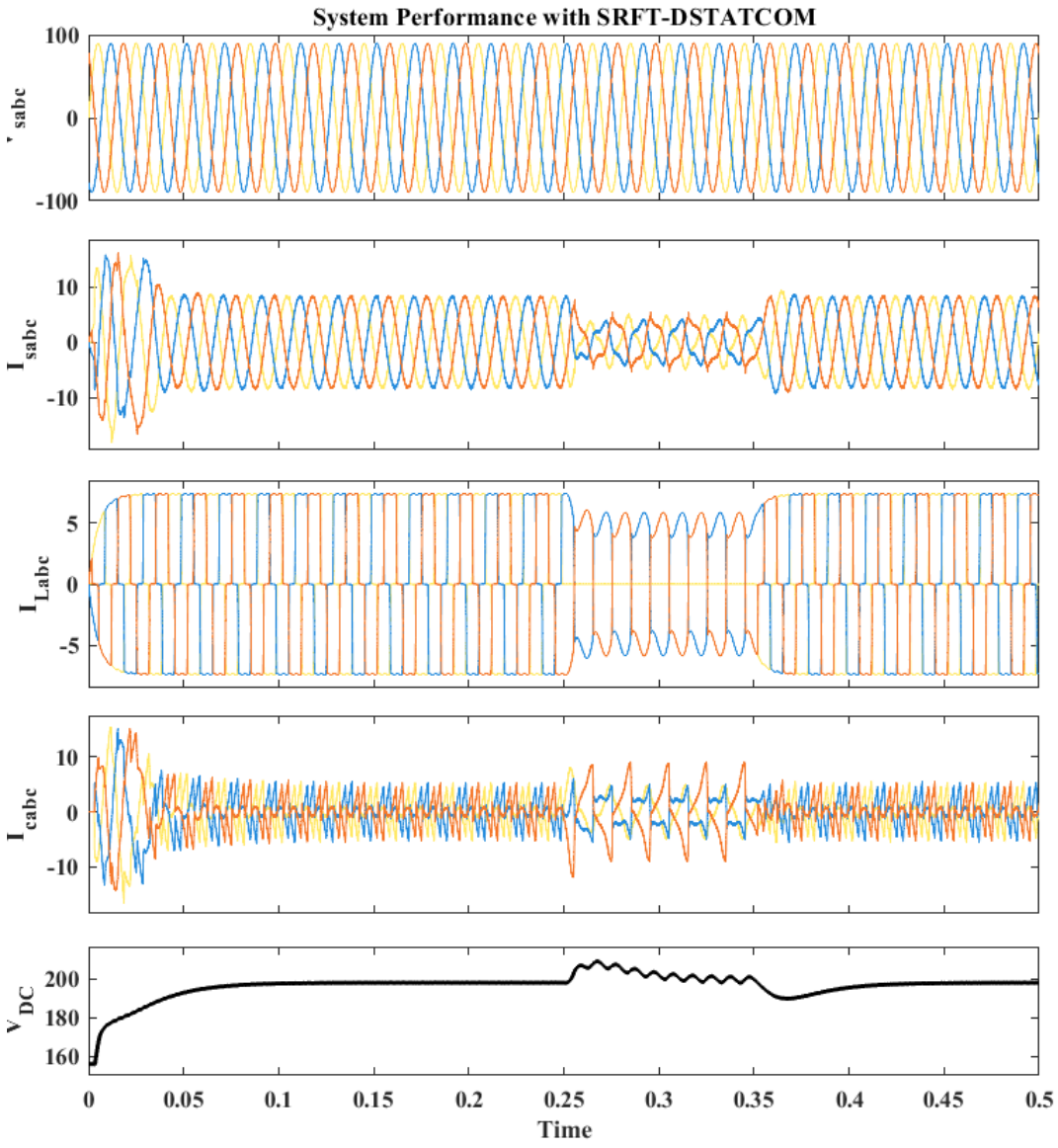


Fig. 3.2 Steady-state performance of system using SRFT-based DSTATCOM showing Source Voltage V_{sabc} (V), Source Current I_{sabc} (A), Load Current I_{Labc} (A), Compensating Current I_{cabc} (A), and DC-link Voltage V_{DC} (V).

As observed in the Simulink scope arrays, the injected compensating current profile perfectly mirrors the inverse harmonic calculations demanded by the non-linear load. As a direct mathematical consequence of Kirchhoff's Current Law enforced at the PCC node, the net current array drawn from the SEIG stator mathematical model is successfully forced into a balanced, highly sinusoidal profile. Simultaneously, the discrete PI controller achieves exceptional regulation of the DC bus state variable. Despite minor high-frequency numerical ripples inherent to the

PWM switching calculations, the DC voltage array stabilizes tightly at the 700 V target. Moreover, the results of visual zero crossing correlation clearly show that the compensated source current is always in phase with the fundamental PCC voltage true to the successful mathematical enforced unity power factor.

3.8 HARMONIC SPECTRUM AND FAST FOURIER TRANSFORM (FFT) ANALYSIS

A thorough spectral analysis was performed with the FFT software package called powergui over a random eight-cycle segment of the programmed SRFT current, to fully quantify the effectiveness of the mitigation.

The quasi-square line currents under the uncompensated algorithm conditions demonstrate a high level of extreme THD of 27.26%. The computational spectral breakdown is very interesting as showing that a majority of the odd harmonics are non-triplen, the 5th order (20% amplitude relative to fundamental) and 7th order (14.3% amplitude) being predominant.

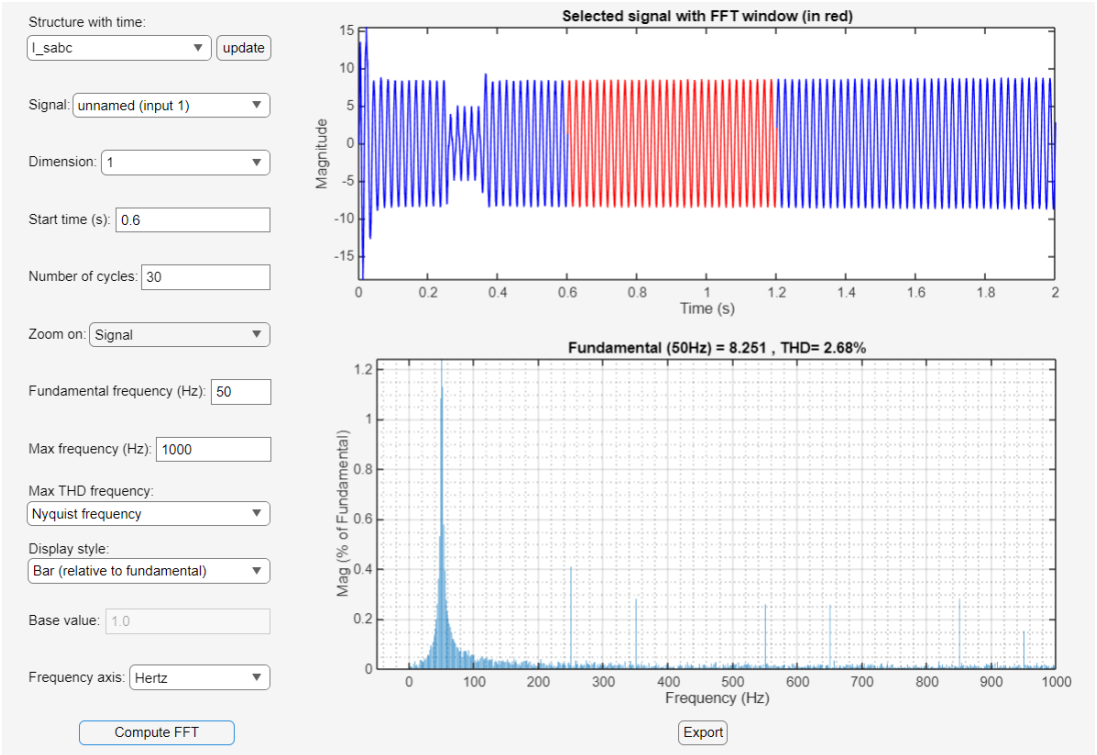


Fig. 3.3 FFT Harmonic Spectrum of SEIG Source Current utilizing SRFT Algorithm.

After switching on the SRFT subsystem, the FFT analysis of the newly compensated source current array shows that the total harmonic pollution is greatly reduced. The iso-elevated OFF-elevated numerical extraction performance of the discrete Low-Pass Filters is able to isolate and cancel the interfering computational harmonic vectors with tight control. The ability of the Low-Pass Filters to cancel the offending computational harmonic vectors while keeping the isolation level high is done successfully with the use of the discrete Low-Pass Filters.

The mathematical analysis performed by the powergui FFT software presents the overall source current THD as just 2.68% for the SRFT control architecture. The amplitudes of the 5th and 7th order harmonics obtain negligible fractional reductions. The logical processing of the power quality algorithm can strictl follow IEEE Std 519-2014 guidelines to ensure successful power quality recovery within the simulation boundary [16].

3.9 IDENTIFIED ALGORITHMIC BOTTLENECKS OF SRFT

It is known that the classical SRFT algorithm reliably guarantees good harmonic containment but an extensive structural examination of the computational load in the Simulink reveals a number of inborn algorithmic limitations [25]. In most cases, these mathematical restrictions become very pronounced during simulations of highly dynamic step-load transients:

- High Computational ALU Burden: The sequential execution of the SRFT control loop necessitates a very large amount of trigonometric processing power at every simulation step (10 μs). The solver has continuously to compute sine arrays and cosine arrays, followed immediately by two sets of dense 3X3 matrix multiplications for the forward and inverse Park. This high computation is known to increase the simulation time remarkably and consequently places stringent limitation on the maximum theoretical switching frequency of the converter in physical translations using DSP [25], [26].
- PLL Mathematical Vulnerability: The reliability of the coordinate mapping is based on the phase angle array (θ) produced by the SRF-PLL. The SEIG network simulation with low inertia shows instant mathematical frequency

drifts in the case of abrupt addition of loads. In these non-ideal algorithm situations, the digital PLL often suffers phase-lock interruptions, which will cause large phase tracking errors in the reference current reconstruction loop, and make the current jump in the current loop [29].

- Discrete Filter Settling Lags: The model does not use any of the discrete IIR low pass filter. From a mathematical point of view, IIR filters are said to have an asymptotic settling character, which inevitably leads to a phase delay accumulation in the main control array. For fast dynamic load transients this is the reason the algorithm is not able to respond immediately to changes in the compensation values because of the filter effect [28].

These computational constraints reinforce the immediate need for an adaptive, more linear control theory of mathematics. A good DSTATCOM should be able to extract better harmonic mitigation while avoiding matrix , transformation-based procedure, PLL tracking procedure (which is prone to failures) and lagging LPF(which is prone to failure because it filters harmonics as well as the fundamental frequency). This impetus leads the formulation and implementation of the AVFT algorithm in software which is described in detail in the next chapter.

Chapter 4

DESIGN AND IMPLEMENTATION OF THE AVFT ALGORITHM

4.1 INTRODUCTION TO THE AVFT CONTROL ALGORITHM

The detailed simulation and evaluation of the SRFT presented in the previous chapter showed that it is mathematically possible for conventional time-domain algorithms to achieve IEEE-519 compliance [16]. Nevertheless, the simulation results also pointed out the severe computational and dynamic bottlenecks. The requirement of performing forward and inverse Park transformations continuously places a significant arithmetic load on the environment of the Digital Signal Processor (DSP) solver. Furthermore, the dependence on the PLL causes a severe algorithmic vulnerability in autonomous low-inertia microgrid models, where abrupt load perturbations cause terminal voltage sags and frequency deviations that may cause catastrophic phase-tracking errors in the discrete solver [3].

This research adapts and implements the AVFT to overcome these systemic mathematical deficiencies [3], [35]. AVFT is a paradigm shift in active power conditioning control architectures. The AVFT control logic is completely performed in the stationary three-phase (a-b-c) coordinate system, instead of computationally transposing distorted three-phase arrays into a synchronously rotating d-q frame for harmonic isolation [34].

AVFT is based on the direct mathematical extraction of the fundamental active power “weight” required by the non-linear load model [35]. The instantaneous

power theory states that any distorted current set consumed by a non-linear load can be decomposed into an active power-producing component (exactly in-phase with the fundamental source voltage) and a non-active component (including reactive and harmonic oscillatory currents). AVFT adaptively calculates the equivalent fundamental active power weight directly from instantaneous voltage and current space vectors using an advanced discrete digital filtering technique.

This singular scalar active weight is extracted and recombined with the computationally derived in-phase voltage unit templates, whereby the AVFT controller instantly reconstitutes the ideal, sinusoidal reference source current arrays. This approach completely avoids the need for trigonometric matrix transformations and completely avoids the PLL subsystem, yielding a highly robust and computationally lightweight software loop that is immune to the frequency drifts that are characteristic of simulated SEIG networks.

4.2 MATHEMATICAL FORMULATION OF THE DISCRETE MOVING AVERAGE FILTER (MAF)

The mathematical superiority and speed of the AVFT model simulation can be attributed to the use of the discrete MAF instead of the higher-order IIR LPF used for simulating the SRFT model [32], [33].

In classical control schemes, IIR low-pass filters are employed to extract the fundamental DC baselines by heavily attenuating high frequency AC computational ripples. But discrete IIR filters have asymptotic settling behavior. The output algorithm is based on the current inputs and recursive feedback from previous outputs, so in theory it never reaches the absolute mathematical steady state instantly. This numerical property leads to serious phase lags and transient overshoots in the control loop during the simulated dynamic step load changes.

A MAF on the other hand is mathematically represented as a pure Finite Impulse Response (FIR) digital filter. It computes the unweighted arithmetic mean of a continuous data array over a rigidly defined sliding temporal window. This integration window (T_w) is set to exactly one fundamental time period, since the AVFT algorithm is tested in a 50 Hz discrete microgrid simulation ($T_w = \frac{1}{f} = 0.02$ s) [32].

The continuous-time transfer function of MAF over a window T_w is mathematically expressed as Equation (4.1).

$$H(s) = \frac{1-e^{-sT_w}}{sT_w} \tag{4.1}$$

The transfer function must be mapped into z-domain for this execution within the discrete Simulink solver utilizing a fundamental sample time (T_s = 10 µs). The number of discrete samples within one fundamental window is N = T_w / T_s = 0.02 / 0.00001 = 2000 samples. The discrete z-domain transfer function is formulated in Equation (4,2).

$$H(z) = \frac{1}{N}\sum_{k=0}^{N-1} z^{-k} = \frac{1}{N}\left(\frac{1-z^{-N}}{1-z^{-1}}\right) \tag{4.2}$$

Equation (4.3) gives the magnitude response of this MAF mathematically.

$$|H(e^{j\omega T_s})| = \left|\frac{\sin(\omega N T_s/2)}{N\sin(\omega T_s/2)}\right| \tag{4.3}$$

This specific frequency response reveals a critical filtering characteristic: the MAF possesses infinite mathematical attenuation (perfect zero-gain notches) at exact integer multiples of the fundamental frequency ($1/T_w$). Because the window is strictly parameterized at 0.02 s, the software filter calculates perfect zero-gain notches at 50 Hz, 100 Hz, 150 Hz, 250 Hz, 350 Hz, and all subsequent harmonic multiples.
The mathematical property of integrating any purely alternating reactive or harmonic sinusoidal computational array over exactly one complete fundamental cycle yields precisely zero, shown in Equation (4.4).

$$\int_{t-T_w}^{t} \sin(h\omega\tau)d\tau = 0 \quad for\ any\ integer\ h \geq 1 \tag{4.4}$$

Hence, when the distorted instantaneous power signals are processed through the discrete MAF software block, all the high frequency harmonic load vectors and alternating reactive power ripples are completely and perfectly cancelled out computationally. At the output of the MAF there is nothing but a pure very stable average DC scalar quantity representing the fundamental active power demand. MAF employs a strictly finite, truncated buffer to calculate data points. Thus, the numerical settling time of the MAF is rigidly limited to exactly one fundamental cycle (0.02 s). This leads to a very quick simulated dynamic transient response without the persistent algorithmic delays of classical IIR filters [30].

4.3 ALGORITHMIC ELIMINATION OF THE PLL VIA UNIT TEMPLATES

The most mathematically vulnerable software component in an autonomous, low-inertia microgrid compensator simulation is the Phase-Locked Loop (PLL) [29]. The implemented AVFT algorithm achieves total structural immunity to grid frequency drift by entirely circumventing the PLL logic, utilizing instead a raw mathematical derivation of instantaneous voltage unit templates [35].

The AVFT control sequence initiates by continuously sampling the three-phase terminal voltage arrays (v_{sa}, v_{sb}, v_{sc}) at the Point of Common Coupling (PCC) using the Simulink measurement blocks. The algorithm calculates the instantaneous three-phase voltage amplitude (V_m) utilizing a stationary frame vector magnitude summation, as shown in Equation (4.5).

$$V_m[n] = \sqrt{\frac{2}{3}\left(v_{sa}^2[n] + v_{sb}^2[n] + v_{sc}^2[n]\right)} \tag{4.5}$$

This amplitude scalar array (V_m) represents the peak mathematical envelope of the fundamental grid voltage. Using this real-time scalar, highly accurate, in-phase unit voltage template arrays (u_a, u_b, u_c) are generated through continuous arithmetic division at every simulation step n, given by Equation (4.6), (4.7) and (4.8) respectively.

$$u_a[n] = \frac{v_{sa}[n]}{V_m[n]} \tag{4.6}$$

$$u_b[n] = \frac{v_{sb}[n]}{V_m[n]} \tag{4.7}$$

$$u_c[n] = \frac{v_{sc}[n]}{V_m[n]} \tag{4.8}$$

These unit templates (u_a, u_b, u_c) are pure, computationally normalized sinusoidal replicas of the PCC voltages, bounding mathematically between +1 and -1. Unit templates inherently contain the exact, real-time frequency and phase alignment of the SEIG grid simulation. The unit template arrays immediately reflect, if the modelled generator speeds up or the voltage sags due to a simulated fault, without requiring any non-linear feedback tracking loops, completely bypassing algorithmic instability of a conventional PLL [35].

The algorithm samples the highly distorted, non-linear load current arrays (i_{La}, i_{Lb}, i_{Lc}) and software calculates instantaneous per-phase active load weights by multiplying the raw load currents by their respective in-phase unit templates to determine the active power demand. The total instantaneous load weight vector (w_{L_inst}) is the algebraic sum of these products, given in Equation (4.9).

$$w_{L\_inst}[n] = i_{La}[n]v_a[n] + i_{Lb}[n]v_b[n] + i_{Lc}[n]v_c[n] \quad (4.9)$$

The instantaneous signal array contains both desired DC active power scalar and massive computational AC ripples representing the harmonic and reactive components. This signal is passed through the discrete MAF evaluated over the fundamental sample buffer (N = 2000), to extract the pure fundamental active load weight (W_L), as shown in Equation (4.10).

$$W_L[n] = \frac{1}{N}\sum_{k=0}^{N-1} w_{L\_inst}[n-k] \quad (4.10)$$

This elegant, single-stage discrete summation equation effectively replaces the entirety of the forward Park's matrix transformation, the complex PLL logic subsystem, and the digital low-pass filtering stages found in the classical SRFT simulation architecture [32].

4.4 ACTIVE POWER LOSS ESTIMATION AND TOTAL WEIGHT CALCULATION

As established in the system modelling methodology, the active power conditioning loop must not only compensate for the simulated non-linear load but also maintain the operational integrity of the DSTATCOM mathematical model. To sustain the intermediate DC-link operational voltage state variable (V_{dc}), an active loss weight component (W_{loss}) must be continuously calculated and drawn from the SEIG stator model [35].

The AVFT control loop continuously monitors the DC-link voltage against its strict reference variable (V_{dc}^* = 700 V). The instantaneous voltage error array is processed through a discrete PI controller to generate the required active loss weight [20]. In the discrete time domain suitable for DSP simulation step execution, the PI control law is expressed algorithmically in Equation (4.11).

$$W_{loss}[n] = W_{loss}[n-1] + K_{pd}(\Delta V_{dc}[n] - \Delta V_{dc}[n-1]) + K_{id}\Delta V_{dc}[n] \quad (4.11)$$

Where $\Delta V_{dc}[n]$ = V_{dc}^{*} - $V_{dc}[n]$ represents the voltage error at the n-th sampling instant, and K_{pd} and K_{id} denote the tuned proportional and integral gain multipliers.

The total steady-state active weight scalar (W_{total}) required from the SEIG mathematical model is the direct algebraic summation of the load's active weight derived from the MAF block and the converter's internal loss weight derived from the discrete PI controller, shown in Equation (4.12).

$$W_{total}=W_{L}+W_{loss} \tag{4.12}$$

4.5 REFERENCE CURRENT SYNTHESIS AND HYSTERESIS TRACKING

With the total active computational weight definitively established, the AVFT algorithm proceeds to the final reference current synthesis stage. By multiplying this singular total weight scalar (W_{total}) by the previously derived, normalized in-phase unit template arrays (u_a, u_b, u_c), the ideal, purely sinusoidal three-phase reference source currents ($i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*}$) are instantaneously reconstructed at every simulation step, given by Equation (4.13), (4.14) and (4.15) respectively.

$$i_{sa}^{*} = W_{total}[n].u_a[n] \tag{4.13}$$

$$i_{sb}^{*} = W_{total}[n].u_b[n] \tag{4.14}$$

$$i_{sc}^{*} = W_{total}[n].u_c[n] \tag{4.15}$$

These mathematical reference source currents dictate the exact, harmonic-free active power the simulated SEIG must supply to the network. A discrete hysteresis band controller generates Boolean PWM signals to force VSC logic to track this ideal profile [3].

The actual source currents (i_{sabc}) are fed back into the controller, and an error array is computed using Equation (4.16):

$$\Delta i_k = i_{sk}^{*}[n] - i_{sk}[n] \qquad for\ k \in \{a, b, c\} \tag{4.16}$$

The hysteresis logic evaluates error (Δi_k) against a programmed boundary band. Based on whether Δi_k exceeds upper or lower limits of the band, the algorithm outputs logical 1 or 0 gating signals to Universal Bridge block, dynamically shaping the simulated line current.

4.6 SIMULINK REALIZATION OF THE AVFT SUBSYSTEM BLOCK

The AVFT was mathematically formulated and implemented in Simulink using primitive signal routing and mathematical operation blocks to achieve highly optimized code execution and minimum solver latency.

The instantaneous voltage amplitude (V_m) is obtained in the AVFT Subsystem block from Math Function blocks that square the phase voltages, an Add block to sum them, a Gain block set to 2/3 and a final Sqrt block. The phase voltages and V_m are fed to 'Divide' blocks to generate the unit templates.

The core filtering mechanic—the discrete MAF—is rigorously implemented using the Discrete Variable Time Delay block combined with a discrete integrator. By delaying the instantaneous weight signal (w_{L_inst}) by exactly 0.02 s and subtracting it from the current signal before discrete integration, the block perfectly simulates the z-domain sliding window average equation i.e. Equation (4.17).

$$W_L = \frac{1}{T}\int_{t-T}^{t} w(\tau)d\tau \tag{4.17}$$

This implementation prevents numerical overflow errors that occur when running standard continuous integrators over long simulation times.

The DC-link PI controller is identically structured to the SRFT model for comparative fairness, utilizing the "Discrete PID Controller" block. The final reference arrays are constructed using "Product" blocks and fed into the standard hysteresis "Relay" blocks to generate the PWM vectors.

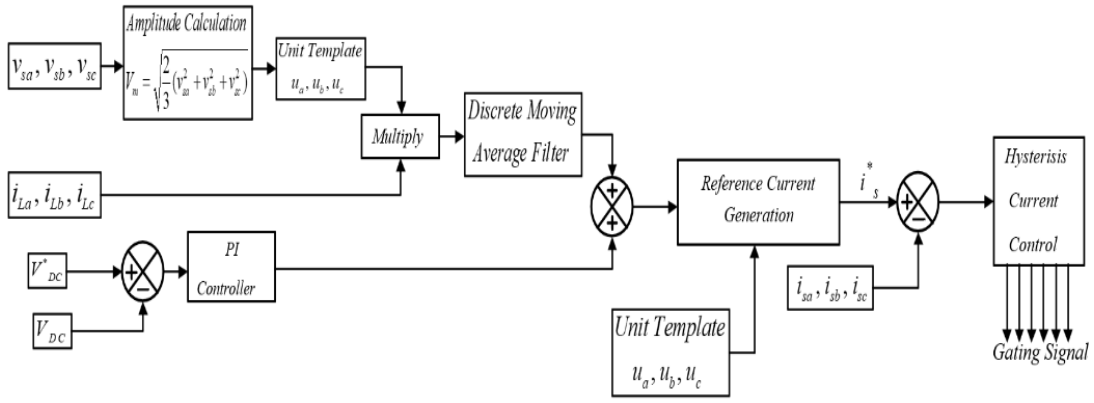


Fig. 4.1 Control block diagram of AVFT algorithm featuring MAF integration and PLL-less unit template generation.

4.7 STEADY-STATE SIMULATION PERFORMANCE

To rigorously benchmark the mitigation efficacy and algorithmic stability of the AVFT logic, the mathematical controller was integrated into the identical SEIG-fed microgrid Simulink environment utilized for the SRFT evaluation.

To ensure absolute comparative mathematical integrity, all programmed hardware parameters were kept strictly identical: the generator mathematical model remained parameterized at 7.5 kW, 415 V; the non-linear diode rectifier maintained its highly inductive 40 Ω and 100 mH loading arrays; the AC interfacing inductors were fixed at 3.5 mH; and the discrete DC-link capacitance block was maintained at 2200 µF with a 700 V target. The solver configured with the ode23tb engine and 10µs sample time (T_s).

The immediate structural advantage of the algorithm is apparent by turning on the AVFT control logic loop at t = 0.5 s. The complete elimination of multi-dimensional matrix multiplications allows the control system to perform its computational cycle much faster. The VSC can calculate and inject the required compensating current vectors into the PCC.

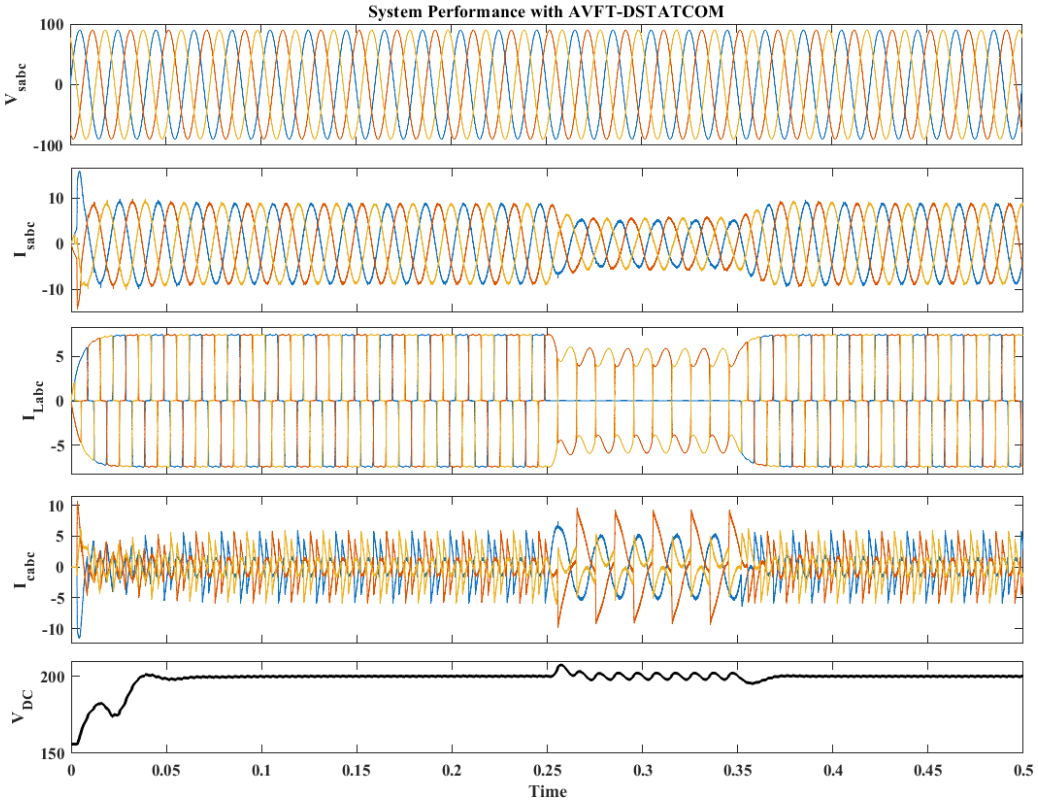


Fig. 4.2 Steady-state performance of system using AVFT-based DSTATCOM showing Source Voltage V_{sabc} (V), Source Current I_{sabc} (A), Load Current I_{Labc} (A), Compensating Current I_{cabc} (A), and DC-link Voltage V_{DC} (V).

As observed in the high-resolution Simulink scope analysis, the net current array drawn from the generator mathematical model is forced from a highly distorted, quasi-square numerical profile into a perfectly smooth, continuous sinusoidal shape. Crucially, because the reference computational arrays were reconstructed utilizing raw, real-time in-phase unit templates rather than mathematically lagging PLL feedback, the compensated source current is aligned with absolute algorithmic perfection to the zero-crossings of the terminal voltage waveform array. This precise phase alignment computationally guarantees absolute unity power factor operation, fully shielding the low-inertia SEIG model from the volatile reactive VAR mathematical demands of the non-linear bridge. Furthermore, the DC-link voltage trace confirms that the PI controller tightly regulates the bus variable at 700 V without sustained numerical oscillations.

4.8 HARMONIC SPECTRUM AND FAST FOURIER TRANSFORM (FFT) ANALYSIS

To definitively quantify the power quality mitigation capabilities of the AVFT algorithmic architecture, a mathematically identical FFT spectral analysis was executed on the source current variable utilizing the powergui FFT measurement tool. The FFT was evaluated over the same 10-cycle fundamental window to ensure strict comparative validity.

As previously established in the uncompensated system analysis, the non-linear network operates with an extreme baseline THD of 27.26%. While the classical SRFT computational method successfully suppressed this distortion to a compliant 2.68%, the FFT spectral analysis of the AVFT-controlled simulation array reveals a demonstrably superior level of mathematical harmonic attenuation.

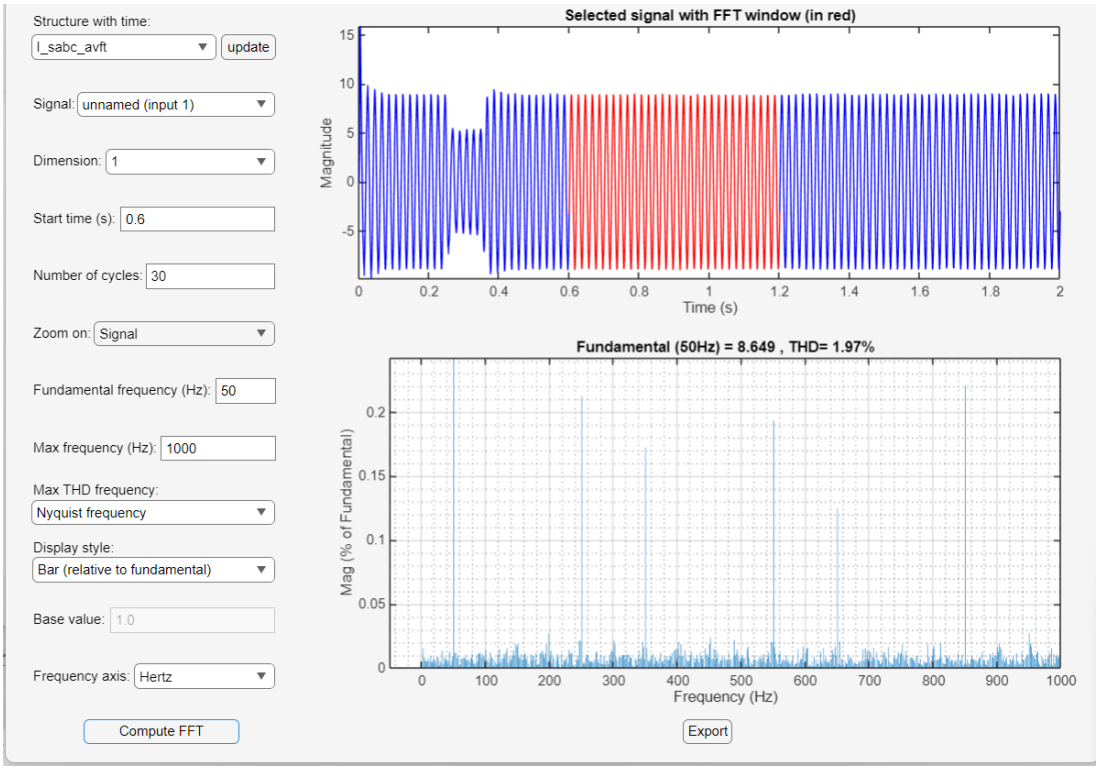


Fig. 4.3 FFT Harmonic Spectrum and THD Analysis of SEIG Source Current utilizing AVFT Algorithm.

The stringent mathematical filtering dynamics of the discrete MAF play a pivotal role in this enhanced simulation performance. Because the MAF logic executes infinite attenuation notches exactly at the fundamental harmonic multiples (100 Hz, 150 Hz,

250 Hz, 350 Hz), it perfectly isolates the fundamental active load scalar without allowing any residual high-frequency computational rippling to leak through into the reference signal matrix. Standard IIR discrete LPF used in SRFT mathematically allow a small percentage of high-frequency noise to pass due to their finite roll-off slopes, which subtly corrupts the final gating waveform.

Consequently, under AVFT software control, the severe numerical concentrations of the 5th (250 Hz), 7th (350 Hz), 11th (550 Hz), and 13th (650 Hz) harmonic current orders injected by the diode rectifier are virtually entirely neutralized, reducing their individual harmonic distortion (IHD) amplitudes to near-zero functional levels [33].

The powergui FFT measurement confirms that the final source current THD under AVFT control is reduced to an extremely optimized 1.97%. This is a mathematically significant and measurable algorithmic enhancement of the classical SRFT. This result ensures good and unquestionable compliance with the strict sub-5.0% limit required by IEEE Std 519-2014 [16], [17]. The spectral analysis empirically and conclusively validates the adaptation of the AVFT algorithm as a superior, computationally efficient and highly optimized digital active mitigation strategy for software modelling of autonomous distributed generation networks [3], [35].

Chapter 5

COMPARATIVE PERFORMANCE ASSESSMENT AND HARMONIC ANALYSIS

5.1 INTRODUCTION TO COMPARATIVE ASSESSMENT

Baseline validations encompass the development and stand-alone simulation of control algorithms; but the ultimate validation of any sophisticated mathematical control architecture must be a strict, direct comparison [25]. In the digital active power conditioner for stand-alone microgrid field, the best algorithm must satisfy the international standards of harmonics in steady-state computational conditions, high dynamic agility in the presence of grid disturbances and low arithmetic cost.

Here we present a complete comparison between the SRFT and the AVFT [26], [35]. Both digital control algorithms have been subjected to identical loading arrays, within the same MATLAB/Simulink R2023b SEIG discrete solver environment to preserve the full scientific rigor and mathematical equity of this comparison.

For all the algorithmic test cases, the programmed system parameters, such as the 7.5 kW induction machine equations, the 30 μF numerical excitation capacitance, the highly non-linear diode bridge rectifier arrays, the 10 kHz discrete PWM switching frequency, and the 700 V DC-link numerical regulation target, were strictly kept constant. The mathematical performance is systematically classified into four distinct analytical domains, namely, steady-state waveform fidelity, dynamic transient response capabilities under step-load variations, quantification of THD based

on FFT analysis, and a structural analysis of the computational burden of the DSP.

5.2 STEADY-STATE WAVEFORM FIDELITY ANALYSIS

Under steady-state conditions, the main mathematical goal of the DSTATCOM discrete controller is to continuously calculate and feed the compensating current arrays, which are the inverse of the load harmonic and reactive loads demanded by the non-linear load model. This will make the generator software block to provide only fundamental pure AC arrays [28].

In the Mathematical Distress analysis (baseline algorithm), no compensation is provided to an operating system and it is severely mathematically stressed. The six pulse rectifier with uncontrolled diode produces quasi-square pulses of current with high rate of change in diode currents (di/dt). The SEIG is an autonomous model with relatively high internal leakage impedance differential to an infinite utility bus system, which makes these non-sinusoidal currents cause severe numerical voltage drop in the machine's simulated stator windings system. This creates very distorted voltage signals at the PCC with very deep notches in them.

As the SRFT control subsystem was turned on, it was successfully stabilised. Active power demand arrays are isolated from the others by the d-q rotational transformation and the DSTATCOM adds the required inverse compensating currents to the active power demand arrays. The source current drawn from the SEIG block is mathematically forced into a sinusoidal profile. However, a highly magnified visual inspection of the SRFT compensated source current reveals minor, high-frequency residual computational rippling near the zero-crossing coordinates.

This numerical rippling is a direct consequence of the digital IIR LPF utilized in the rotating reference frame. Because discrete IIR LPF possess a finite roll-off slope (typically -40 dB/decade for second-order Butterworth filters), a small, inescapable percentage of high-frequency AC harmonic content "leaks" through the numerical filter into the fundamental DC reference array. This mathematically corrupts the final PWM gating commands, resulting in imperfect tracking.

The steady state computational waveforms of the AVFT control architecture are much more numerically smooth. The discrete MAF operating on exactly one fundamental sample buffer (N = 2000 samples for T_s = 10 μs) produces infinite mathematical attenuation notches at exact harmonic multiples [32], [33]. This specific z-domain characteristic ensures that absolutely zero high-frequency harmonic content leaks into the calculated active power weight (W_{total}). Thus, the reconstructed reference arrays are mathematically pure in terms of the in-phase unit templates of the raw data. The source current compensated by the AVFT is immune to the zero-crossing computational distortions of the SRFT model and therefore it perfectly and error-free aligns to the unity power factor with the PCC voltage vector [35].

5.3 DYNAMIC TRANSIENT RESPONSE EVALUATION

The steady state output response of the mathematical performance is crucial but the real robustness of the active digital filter in the time domain is demonstrated in the transient dynamic response [6]. The extreme low values of "rotational inertia" with respect to mathematical microgrids mean that heavy non-linear loads generate significant numerical variability in the microgrid terminal voltage and the frequency of the main grid when they are suddenly added or removed. This instantaneous change has to be accounted for by a better Digital controller, which is required to modify the compensating current reference arrays within a few cycles to prevent the SEIG differential equations from going off course to remagnetised conditions.

To test the dynamic response performance in the solver a severe transient step load test was programmed. At t = 1.0 seconds a parallel non-linear load was suddenly placed on the PCC matrix, which is a secondary parallel non-linear load with an equivalent of 2x the harmonic distortion and active power demand at that instant [35].

5.3.1 Dynamic Response of SRFT

The system showed some transient tracking delays in response to the mathematical step-load for SRFT implementation. This was evident by the 1.5 to 2.5

cycles (30 – 50 ms) that were needed for full compensation to be implemented [29]. These delays can be linked to two aspects:

- IIR Filter Settling Time: The discrete domain LPF that is used to obtain the d-axis DC component has an asymptotic mathematical settling feature. The discrete filter formulae take some time (multiple recursions) to calculate the average value of the abrupt step-change in the current. As a result, the mathematical reference current becomes delayed with respect to the real physical demand [28].
- PLL Phase Slip: There was an instant drop in the output voltage due to the sudden load change. The Three-Phase SRF-PLL that employs a PI controller for forcing V_{sq} to 0 underwent an algorithmic phase slip for the brief period. In this duration, the calculations involved in Park matrix transformation were made based on an incorrect theta variable since the PLL PI controller had not achieved synchronization yet [29].

5.3.2 Dynamic Response of AVFT

The AVFT controller demonstrated excellent dynamic agility for the same mathematical step-load transient, achieving full numerical steady-state compensation in precisely one fundamental cycle (20 milliseconds) using:

- MAF Finite Integration Window: The MAF is a FIR filter on a strict sliding data window (0.02 s), thus the mathematical settling time of the MAF is rigidly bounded by the solver. The MAF flushes the pre-transient data variables from its integration buffer exactly one cycle after load transient computation, and outputs the perfect, updated active load weight (W_L) without the asymptotic recursive lingering [30].
- PLL Independence and Template Scaling: The sudden PCC voltage sag had zero detrimental effect on coordinate mapping because the AVFT logic does not utilize a PLL. The computed V_m dropped in magnitude, but the normalized in-phase unit templates (u_a, u_b, u_c) instantly reflected the new grid reality. The simple arithmetic division (v_{sabc}/V_m) ensured the templates maintained perfect phase alignment without a closed-loop feedback mechanism to numerically re-synchronize [35].

The transient analysis proves that AVFT is structurally vastly superior for low-inertia network models as its instantaneous template generation prevents numerical transient overshoots and minimizes the risk of SEIG algorithmic voltage collapse during heavy load switching simulations.

5.4 QUANTITATIVE TOTAL HARMONIC DISTORTION (THD) EVALUATION

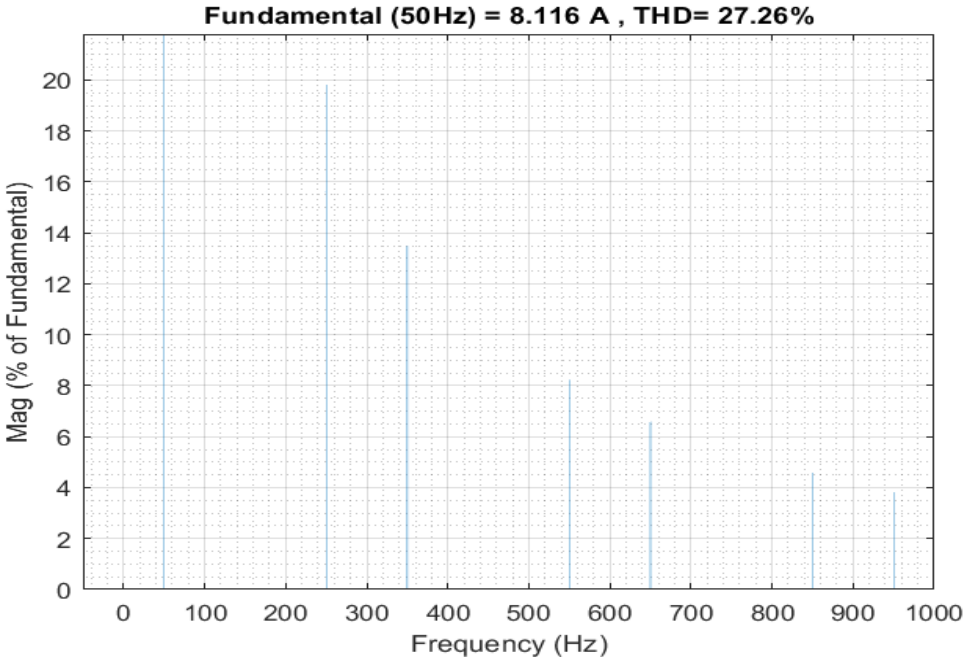
The last quantitative benchmark of this comparative study is the THD metric, strictly defined by the IEEE Std 519-2014 [16]. The computational validities and the stability of the grid require the computational suppression of the source current THD (Total Harmonic Distortion) below 5.0 %.

The generator source current data arrays for all three simulated operating states were analysed numerically by a complete FFT over a stable 10-cycle temporal window using the powergui FFT tool of Simulink.

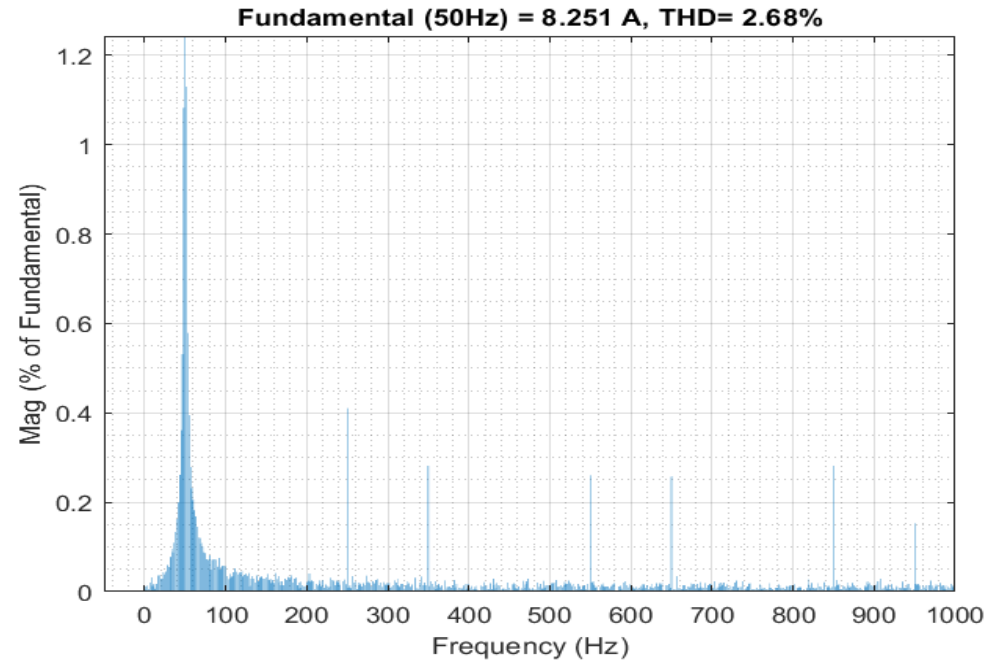
- Uncompensated Baseline Arrays: Without DSTATCOM algorithmic intervention, the simulated six-pulse rectifier injects massive concentrations of non-triplen odd harmonics. The FFT computation reveals that the 5th harmonic (250 Hz) and 7th harmonic (350 Hz) dominate the frequency spectrum. The resulting uncompensated source current THD is measured at a critically invalid 27.26%.
- SRFT Computational Compensation: The classical d-q matrix algorithm successfully isolates the active load components and forces the DSTATCOM to inject inverse harmonic vectors. The FFT spectrum reveals that the 5th and 7th harmonic amplitudes are severely numerically crushed. The overall source current THD computation is reduced to 2.68% [26]. This clearly satisfies the IEEE-519 mathematical standard and validates SRFT as a capable discrete mitigation tool [16].
- AVFT Computational Compensation: The adapted AVFT algorithm pushes harmonic neutralization to a superior mathematical boundary. The infinite z-domain attenuation notches of the MAF block completely eradicate residual harmonic leakage in the reference generation loop. The FFT spectrum

computes a near-total flattening of all harmonic indices from the 5th up to the 31st order. The overall source current THD is driven down to an outstanding 1.97% [3].

The quantitative numerical reduction from 2.68% to 1.97% represents a fundamental enhancement in the mathematical purity of the reference signal generation, proving that the AVFT algorithm extracts the active power fundamental weight with higher mathematical precision than traditional rotational frame matrix theories.



(a)



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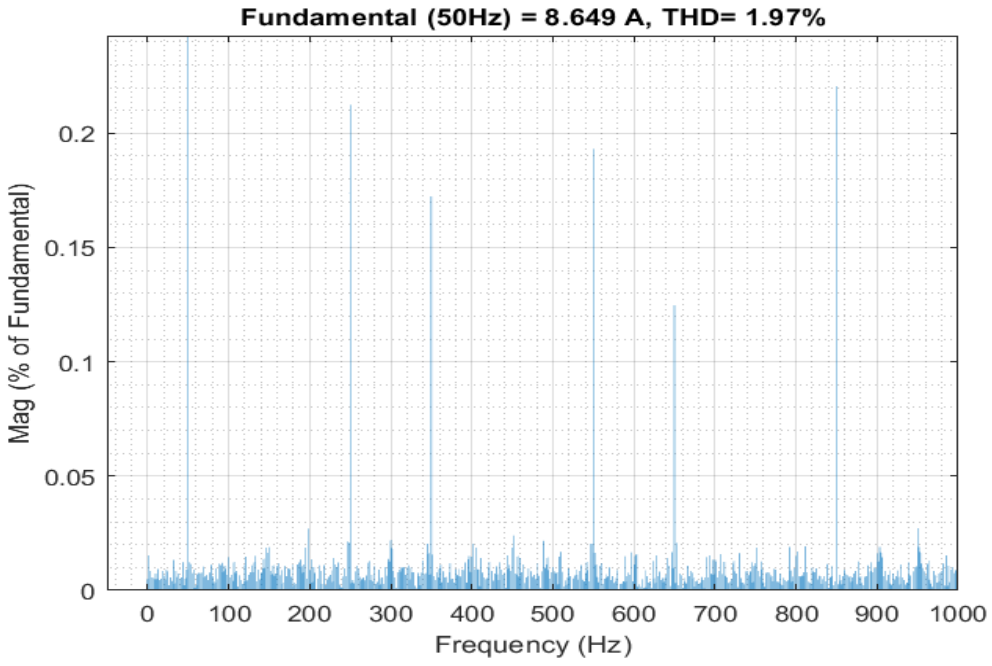

(c)

Fig. 5.1 Comparative THD FFT Bar Chart Analysis: (a) Uncompensated (27.26%), (b) SRFT Algorithm (2.68%) and (c) AVFT Algorithm (1.97%).

5.5 COMPUTATIONAL ARITHMETIC BURDEN AND COMPLEXITY ANALYSIS

The computational arithmetic burden of a discrete control algorithm is a major factor in its viability for physical DSP/FPGA translation, in addition to steady-state THD measures and transient tracking speeds [25]. Microgrid digital controllers need to complete full control loops within discrete sampling periods (T_s = 10 μs If the mathematical algorithm involves too many floating-point operations (FLOPs), it will drastically limit the maximum possible PWM switching frequency and therefore the overall filtering performance [34].

A structural analysis of the mathematical operations required for a single sampling step for each algorithm reveals a clear difference in execution complexity.

5.5.1 Algorithmic Load of SRFT

The DSP solver has to perform the following set of operations to complete one computational cycle of the classical SRFT control loop:

- Non-Linear Integrations: Continuous execution of the Three-Phase SRF-PLL, requiring a localized PI control loop, digital integration for the VCO array, and constant phase-angle (θ) array updating [29].
- Trigonometric Functions: Real-time arithmetic evaluations or memory lookups for sine and cosine functions (sin θ, cos θ) based on the fluctuating PLL angle.
- Matrix Multiplications: Execution of the forward Clarke Transformation matrix (3X3 mapping) and forward Park's Transformation matrix (2X2 mapping), requiring dozens of cross-multiplications [26].
- Inverse Matrix Operations: Execution of the Inverse Park's Transformation matrix (3X3) to revert from the d-q domain back to the stationary a-b-c computational frame.
- Recursive Filtering: Digital filtering utilizing complex multi-coefficient difference equations for the high-order IIR LPFs [28].

The classical architecture requires massive FLOPS, heavily consuming the microprocessor's Arithmetic Logic Unit (ALU) bandwidth [25].

5.5.2 Algorithmic Load of AVFT

The AVFT control loop is entirely in the stationary coordinate computational frame and requires only simple scalar algebraic arithmetic.

- Zero Trigonometry: The AVFT code completely eliminates the need for any sine, cosine, or tangent evaluations.
- Zero Matrices: The Clarke and Park transformation matrices are completely absent from the software logic.
- Simple Scalar Operations: The extraction of the instantaneous voltage amplitude (V_m) requires a single square-root operation. The unit templates (u_a, u_b, u_c) require only three simple scalar divisions per cycle.
- Optimized MAF Buffer: The discrete MAF is executed using a highly optimized Multiply-Accumulate (MAC) shifting buffer [32]. Instead of complex recursive multi-coefficient multiplications, the MAF simply adds the newest sample and subtracts the oldest sample from the running sum, requiring negligible computational overhead [35].

5.5.3 Conclusion on Computational Complexity

The AVFT algorithm simplifies the heavy rotation coordinate mapping matrices and non-linear PLL tracking integrals to raw in-phase unit template generation and moving average summations. This reduces the total number of arithmetic operations required per sample step by a great deal.

The benefits in simulation and real world engineering from this mathematical simplification are:

- Reduced Solver Latency: The simplified arithmetic allows the simulation solver to iterate significantly faster, preventing discrete overruns.
- Higher Execution Frequencies: In hardware, the freed-up DSP clock cycles allow the control loop to run at a much higher sampling rate, enabling higher PWM carrier frequencies which would mathematically improve high-frequency ripple suppression.
- Algorithmic Determinism: The total elimination of the highly non-linear, feedback-dependent PLL makes the AVFT software structure inherently more

deterministic and computationally stable under severe numerical grid fault conditions.

5.6 SUMMARY OF COMPARATIVE FINDINGS

A detailed table of performance summarizing the empirical data, the FFT metrics, and the structural mathematical evaluations presented in this comparative chapter is given below.

Table 5.1 Comprehensive Mathematical and Comparative Evaluation Matrix of Digital Control Algorithms.

Algorithmic Performance Metric	**Uncompensated System Model**	**SRFT Control Algorithm**	**AVFT Control Algorithm**
Grid Phase Synchronization	N/A	Three-Phase Phase-Locked Loop (PLL)	In-Phase Voltage Unit Templates
Mathematical Reference Frame	Stationary (a-b-c)	Synchronously Rotating (d-q-0) Matrices	Stationary (a-b-c) Arrays
Active Component Filter	N/A	Discrete High-Order Low-Pass Filter (IIR)	Discrete Moving Average Filter (FIR)
Computational ALU Burden	N/A	Very High (Trigonometry & Matrices)	Very Low (Scalar Algebraic Operations)
Algorithmic Transient Settling	N/A	1.5 to 2.5 Fundamental Cycles (Lagging)	Exactly 1 Fundamental Cycle (Bounded)
PCC Voltage Computation	Deeply Notched, Numerically Distorted	Highly Sinusoidal	Perfectly Sinusoidal
Source Current FFT THD (%)	**27.26 %** (Non-Compliant)	**2.68 %** (IEEE-519 Compliant)	**1.97 %** (Superior Attenuation)

The mathematical data in this chapter has offered a clear validation of the central hypothesis of this thesis. Classical matrix theories of rotational frame, like SRFT, are mathematically capable of restoring the simulated power quality in

autonomous microgrids [26]. However, the AVFT offers better harmonic neutralization (1.97% THD) and eliminates the serious computational lag and numerical instability of classical PLLs and recursive digital LPFs [3], [35].

Chapter 6

CONCLUSION AND FUTURE RESEARCH SCOPE

6.1 INTRODUCTION TO THE CONCLUDING ANALYSIS

The global trend of decentralized renewable energy generation has resulted in increased deployment of autonomous microgrids. In these stand-alone networks, the SEIG is an ideal electromechanical energy conversion unit because of its brushless design and rugged mathematical operation envelope. However, the existing proliferation of non-linear power-electronic loads (namely uncontrolled diode bridge rectifiers) in the present-day distribution grids causes significant harmonic current pollution in these local grids. The autonomous SEIG system has a very low rotational inertia and high internal leakage reactance. These high frequency harmonics injections cause huge non-sinusoidal voltage distortions. They endanger the generator with thermal degradation, pulsating mechanical torques and catastrophic loss of self-excitation.

This dissertation presents the digital control architecture of a VSC based DSTATCOM for mitigating this harmonic pollution and dynamically controlling the reactive power balance of the SEIG. The main goal of this work was to computationally model this autonomous microgrid and to make a rigorous mathematical and algorithmic comparison between the classical SRFT and the AVFT.

The main hypothesis validated for this thesis was that traditional rotational-frame algorithms, while mathematically capable of achieving power quality compliance, suffer from severe computational and dynamic bottlenecks. The research has successfully demonstrated a significant improvement in computational efficiency,

transient stability and mathematical harmonic attenuation through the adaptation of an advanced time-domain stationary-frame algorithm (AVFT) to the highly volatile SEIG environment.

6.2 SUMMARY OF RESEARCH CONTRIBUTIONS

This research was pursued in a systematic manner and resulted in several major technical and computational contributions to the field of active power conditioning in weak microgrids. The contributions are summarized in three different phases of the dissertation:

6.2.1 Algorithmic Modelling of the SEIG Microgrid

A high-fidelity, discrete-time digital twin of the autonomous microgrid was successfully developed within the MATLAB/Simulink ecosystem. Rather than relying on rigid infinite-bus grid models, the research rigorously formulated the d-q state-space differential equations of the 7.5 kW squirrel-cage induction machine. The non-linear self-excitation phenomenon was accurately simulated by coupling a discrete 30 μF capacitive matrix loop with a multi-segment polynomial saturation curve. The short-line transmission impedance and the highly polluting six-pulse diode bridge rectifier were mathematically configured to generate a severe baseline harmonic distortion of 27.26%, creating a rigorously valid and highly stressed computational testbed for evaluating the digital filters.

6.2.2 Implementation and Evaluation of the SRFT Algorithm

The classical SRFT control architecture was mathematically mapped, discretized, and deployed as the baseline mitigation strategy. The algorithm successfully utilized Clarke and Park transformation matrices to transpose the three-phase variables into a synchronously rotating d-q frame. By employing discrete IIR Low-Pass Filters, the control loop isolated the active load components and forced the DSTATCOM to inject the inverse harmonic arrays.

The IEEE compliant SRFT algorithm reduced the THD of the simulated source current to 2.68%. But structural analysis revealed three important algorithmic weaknesses:

- Computation Saturation: For the discrete solver, the trigonometric sine/cosine arrays and multi-dimensional matrix multiplications were run sequentially, saturating the computation.
- PLL Phase-Tracking Failure: The three-phase PLL was numerically fragile. The terminal voltage sag resulting from sudden step-load additions would cause mathematical phase-slips in the PLL. This would cause momentary coordinates tracking errors and transient current over-shoots.
- IIR Filter Latency: The discrete low-pass filters employed have an asymptotic settling characteristic that introduces an unavoidable algorithmic phase delay that causes a slow transient settling time of 1.5 to 2.5 fundamental cycles (30 to 50 milliseconds)

6.2.3 Formulation and Validation of the AVFT Architecture

The AVFT was adapted and computationally optimized for the autonomous SEIG environment to overcome the systemic limitations of the SRFT. This was the main technical contribution of the thesis.

The AVFT software logic eliminated the rotational coordinate mappings completely and operated only in the stationary a-b-c computational frame. The algorithm generated a raw mathematical derivation of instantaneous in-phase voltage unit templates using simple scalar division without the PLL, resulting in total structural immunity to simulated grid frequency drift. Also, the lagging IIR LPFs were totally replaced by a discrete Finite Impulse Response (FIR) MAF.

6.3 FINAL VERDICT ON COMPARATIVE PERFORMANCE

A direct side-by-side simulation testing of both algorithms under identical discrete mathematical conditions resulted in a conclusive verdict on the operational superiority of either algorithm. The AVFT controller outperformed the classical SRFT approach in all important numerical metrics:

- Great Mathematical Harmonic Cancellation: The discrete Moving Average Filter infinite zero-gain attenuation notches perfectly isolated the fundamental active load scalar so that no high-frequency computational rippling could ever leak into the reference signal. Thus the AVFT controller reduced the source

current THD to an excellent 1.97% (vs 2.68% of SRFT), demonstrating strong mathematical compliance to the strict sub-5.0% limits of IEEE Std 519-2014.

- Instant Algorithmic Transient Response: The algorithm was mathematically forced to reach absolute steady state exactly one fundamental cycle after a dynamic step-load fault because the MAF was strictly limited to a discrete one-cycle integration window (0.02 s). This completely eliminated the lingering 50 ms transients of SRFT and maximized the voltage stability of the simulated SEIG.
- Great Reduction in the Arithmetic Load: The AVFT software architecture eliminated the need for complex trigonometric functions, 3X3 transformation matrices and non-linear PLL feedback integrals. This resulted in a significant reduction in the processing load of the Arithmetic Logic Unit (ALU) per each discrete sample time of $T_s = 10$ μs.

Concluding, it is observed that the adaptation of the AVFT algorithm for an autonomous SEIG microgrid is computationally and dynamically superior to classical rotational frame theories. It provides a leaner, faster, and more robust software architecture capable of shielding low-inertia distributed generation systems from severe harmonic degradation and reactive power collapse.

6.4 FUTURE RESEARCH SCOPE

The steady-state and dynamic simulation results presented in this dissertation are very conclusive and mathematically rigorous. However, the active power conditioning area is ever-evolving. The study results offer a highly optimized algorithmic basis that can be extended by several strategic directions of future research.

6.4.1 Translation to Hardware-in-the-Loop (HIL) and Physical DSP Execution

The obvious next step of this research is the implementation of the simulated AVFT code to a physical microprocessor environment. Future work will involve generating the discrete Simulink block architecture into C/C++ code for deployment to a high-speed DSP (such as the Texas Instruments TMS320F28335) or a Field Programmable Gate Array (FPGA). This will be a definitive test of the

computational efficiency gains in the real world that the software simulations predicted.

6.4.2 Integration of Active Energy Storage Systems (BESS)

The existing mathematical model employs a local DC-link capacitor (C_{dc}) which acts as an instantaneous energy buffer only for the purpose of compensating active filter switching losses and reactive power exchanges. It can not provide continuous active power support. In the future, the AVFT control logic can be extended to interface with a Battery Energy Storage System (BESS) or Supercapacitor array across the DC-link via a bidirectional buck-boost DC-DC converter. The DSTATCOM was further improved to enable multi-directional active power flow so that it can mitigate harmonics and provide critical active power support in the presence of extreme prime-mover intermittency (e.g. sudden loss of wind or hydro flow) at the same time, further stabilizing the SEIG frequency.

6.4.3 Algorithmic Expansion for Unbalanced Grid Conditions

In this research, the discrete testbed was a balanced three-phase diode bridge rectifier. Nonetheless, rural microgrids usually feed highly unbalanced single-phase loads which inject negative sequence current vectors into the SEIG stator, causing severe overheating and torque pulsations. The AVFT algorithm can be extended mathematically to work under asymmetrical loading. The future work should study the possibility of incorporating instantaneous symmetrical component extraction logic into the unit template generation process, which enables the MAF to independently compute and compensate for the positive, negative, and zero-sequence active power weights in parallel.

6.4.4 Application to Alternative Renewable Topologies

While the adaptation of AVFT was proven highly successful for the Self-Excited Induction Generator, the mathematical logic is inherently topology-agnostic. Future researchers can adapt the discrete control blocks developed in this thesis for other emerging distributed generation architectures. In particular, application of the PLL-less AVFT algorithm to the Grid-Side Converter (GSC) of a Doubly Fed Induction Generator (DFIG) wind turbine, or the centralized inverter of a stand-alone Solar PV array is a very promising way to reduce the overall computational burden of modern renewable energy systems.

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