DESIGN AND ANALYSIS OF HIGH-SPEED CMOS VOLTAGE LEVEL SHIFTERS FOR SUB-THRESHOLD VOLTAGE REGIME

DISSERTATION/THESIS

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

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IN
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I, **AYUSH DIMRI**, Roll No. 2K24/C&I/09 student of M. Tech (Control & Instrumentation), hereby declare that the project dissertation entitled "**Design and Analysis of High-Speed CMOS Voltage Level Shifters for Sub-Threshold Voltage Regime** " which is being presented by me to the Department of Electrical Engineering, Delhi Technological University, Delhi for partial fulfillment of the requirement of award of the degree of Master of Technology, is my own work done wholly and solely under my direction and is not plagiarized from any source.

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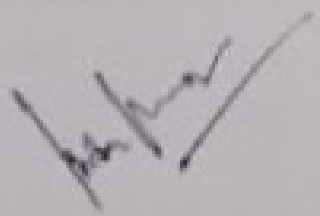
CERTIFICATE

Certified that **AYUSH DIMRI (24/C&I/09)** has carried out their research work presented in this thesis entitled "**Design and Analysis of High Speed CMOS Voltage Level Shifter for Subthreshold Voltage Regime** " for the award of Master of Technology from the Department of Electrical Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results and studies that are carried out by the student himself, and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.



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ABSTRACT

In modern VLSI systems with multiple voltage and low power levels, voltage level shifters (VLSs) are components that allow reliable communication between different voltage domains of the circuit blocks. As the CMOS technology is scaled down and low power consumption in portable electronic devices, biomedical implants, wireless sensor networks, and IoT devices is being demanded continuously, the design of voltage level shifters with low power consumption and high-speed operation has been one of the major research focuses. This comparative study examines a number of recently proposed voltage level shifter architectures, such as conventional cross-coupled level shifters, differential cascode voltage switch (DCVS) structures, current mirror-based level shifters, Wilson current mirror structures, regulated cross-coupled pull-up network (RCC) techniques, and dual current mirror approaches. The primary motivation for the comparative study is the propagation delay, switching speed, power dissipation, voltage conversion, and robustness of the circuit when operating at subthreshold. Conventional cross-coupled and DCVS level shifters have low standby power, but these circuits suffer from the significant problem of contention between the pull-up and pull-down networks at very low input voltage, resulting in larger delay and poor performance. On the contrary, architectures like the current mirror and the Wilson current mirror improve the driving capability and decrease the contention, thus increasing conversion speed and decreasing propagation latency. Propagation delay as low as 0.959 ns and low power dissipation of 106.6 nW for 45 nm technology, making it very energy-efficient for ultra-low voltage applications. The voltage level shifter designed with a regulated cross-coupled pull-up network (RCC) was found to be the best amongst all the techniques considered in terms of both speed and power consumption. The RCC technique has proved to be effective in regulating the pull-up strength, reducing the time of discharging and charging the internal nodes, reducing the static current & greatly increasing the switching speed. The results of the simulation of the RCC-based design resulted in very low power consumption of 123.1nW with a propagation delay of 23.7ns, and it is capable of handling subthreshold input conversion as low as 80 mV. Moreover, optimized device sizing and multi-threshold CMOS showed advantages in performance for wider voltage translation ranges and area efficiency for the improved RCC structures.[1]

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Semiconductor technology has changed dramatically in the last few decades, with the constant scaling of the CMOS devices, making the field of Very Large Scale Integration (VLSI) Design a completely different landscape. Modern electronic systems should perform a high computation rate whilst consuming a restricted amount of power. This need has been especially prevalent in various applications like wearable electronics, embedded applications powered by batteries, biomedical implants, wireless sensor networks, and Internet of Things (IoT) systems. One of the key design challenges in today's modern integrated circuits is to reduce power consumption while keeping the speed and performance high and reliable.

The power consumption reduction technique of multiple supply voltage domains has become widely adopted as the complexity of SoC design has increased. Many different functional blocks are present in a chip, and they may require different voltage levels to function, depending on their speed and performance. The critical blocks with high computational speed run at high supply voltages and the non-critical or standby blocks run at a lower supply voltage to reduce the power dissipation. This method, known as multi-voltage or multi-VDD design methodology, contributes greatly to the energy efficiency and long battery life of portable electronic systems.

The multi-voltage solution can help save considerable power, but presents additional design challenges in the realm of communication between voltage domains. Logic signals produced in low voltage circuits must not be directly connected to high voltage circuits since the signals may not be interpreted correctly, signal integrity may be compromised, leakage current may be increased and signal operation may be unreliable. Likewise, if there are direct connections between voltage domains, the static current flowing between them can be too high, and the short-circuit power drawn will be higher. These issues are overcome by using voltage level shifters as interface circuits between voltage domains.

A voltage level shifter is a particular circuit that changes the logic from one voltage level to another without disturbing the logic operation or the integrity of the signal. These circuits are used as a key link for low voltage and high voltage parts of integrated circuits. VLSI systems, especially for low power consumption, mixed-voltage integrated circuits, memory interfaces, sensor networks, portable electronics, and high-speed communication circuits are all areas where voltage level shifters are widely applied. The efficiency of the voltage level shifter directly influences the speed, efficiency and reliability of the overall system. The design of an efficient voltage level shifter which operates with minimum power consumption, minimum propagation delay, large voltage conversion range and stable sub-threshold operation has become an important research area in present day VLSI design. One of the major objectives in present-day VLSI systems is to reduce power dissipation. The power consumed in CMOS circuits primarily involves dynamic power, static power and leakage power. Dynamic power is due to the load capacitance getting charged and discharged during switching and is proportional to the square of the supply voltage. Direct current flow between supply and ground during switching of transistors causes static power. In deep submicron technologies, leakage power is the dominant power due to the low threshold voltages and high leakage currents. Leakage power and short channel effects are becoming more critical as technology moves towards the nanometer scale, and low power design techniques are even more critical today.

One of the most successful ways of lowering dynamic power dissipation has been voltage scaling. reducing the supply voltage, however, decreases the driving ability of the transistors, increases the propagation delay, and decreases the performance of the transistors. In order to overcome this power-performance trade-off, contemporary circuits tend to work in the sub-threshold regime, where the supply voltage is below the threshold voltage of the MOS transistors. A sub-threshold operating point significantly lowers power consumption but also comes with its share of problems, including decreased switching speed, less pull-down, more process sensitivity, and lower noise margins. As a result, traditional voltage level shifters do not perform well when the voltage is very low.

The voltage level shifter circuits are basically divided into two types: Differential Cascode Voltage Switch (DCVS) based voltage level shifter and Current Mirror (CM) based voltage

level shifter. The DCVS-based level shifters incorporate cross-coupled PMOS transistors to provide regenerative feedback that results in reduced static power consumption and enhanced switching characteristics. But in the sub-threshold mode, the pull-down NMOS transistors are very weak & will not be able to compete with the pull-up PMOS network, causing propagation delay and conversion failure. A solution to this is to increase the size of the transistors, which results in additional silicon area and higher power consumption.

The current mirror-based level shifters, however, provide better performance at low input voltage with the use of current control methods. These architectures give superior voltage conversion efficiency when operating from a low supply voltage, but typically result in circuits with higher static current consumption, higher standby power losses, and more complexity. For that reason, new architectures and optimization techniques for voltage level shifters have been investigated constantly for improving the speed, power efficiency and voltage conversion performance..

In the last few years, several novel voltage level shifter circuits have been proposed in order to address the problems inherent in traditional circuits. The cross coupled pull-up network architecture is one of the popular methods adopted. This method boosts regenerative feedback in the pull up network and reduces contention between the pull up and the pull down transistors. This makes the switching speed much greater, and dynamic power consumption is lower. These architectures have been shown to successfully convert very low sub-threshold voltage levels, with low propagation delay and leakage power.

Advancing further in the voltage level shifter design are the use of the Wilson current mirror and dual current mirror. All these methods help in optimizing the flow of current in the circuit and minimize the static current dissipation. The current mirror-based architectures of Wilson cells offer the advantages of better current control and resistorless current leakage, which enhances switching properties and helps to reduce delay. Reflected-output methods and self-biased current control methods have also been added to some recent designs in order to further improve performance when operating very near the low voltage limit.

Current mirror level shifter circuits with cross-coupled pull-up networks have also been the subject of many studies recently, as hybrid circuits. These mixed methods are used to try to get a balance between the time it takes to execute the method, its energy dissipation, its range

of voltage conversions, and the complexity of the circuit. Moreover, advanced design techniques like Multi-Threshold CMOS (MTCMOS), transistor sizing optimization, feedback assisted switching and sub-threshold device engineering are introduced to maximize the overall performance.

The literature shows that the research on voltage level shifters mainly concentrates on low propagation delay, low power consumption and reliable operation under a wide voltage range. Propagations delays are another key factor in performance - they dictate how fast the voltage level shifter can react when the input changes. Reducing propagation delay is directly related to increasing the operating speed of the system and its performance. In a battery-powered or portable application, however, where energy efficiency is key, power dissipation is another important parameter. Hence, it is one of the most challenging tasks in the design of voltage level shifters to obtain optimality for these two parameters.

Various designs have reported that voltage level shifter performance has been improved significantly. Some architectures have succeeded in achieving propagation delay in the nanosecond range and others have obtained very low power dissipation in the nanowatt range. Some designs are geared towards minimizing leakage current and static power, while others are aimed at achieving high speed operation and broad voltage conversion range. Both proposed architectures, though, have power, delay, area, complexity, operating voltage range and technology dependency trade-offs. So a comparative study of the existing voltage level shifter models is required to understand the pros, cons and applicability of various models in the modern low-power applications. Comparative analysis is used to find the most efficient architecture that can achieve low propagation delay, low power dissipation, reliable sub-threshold operation and better system performance. This analysis also gives insight into the development of design methodologies and future research directions in low power VLSI systems.

The main focus of this thesis is the development of a detailed comparison of different recently proposed architectures for a voltage level shifter based on propagation delay and power consumption. The study also covers analysis of various existing models of voltage level shifter such as voltage level shifter using current mirror, cross coupled, pull-up, and hybrid approach and fabricated using various CMOS technologies. Circuits are judged on their

propagation delay, power consumption, voltage conversion ability, operating range, leakage current, switching speed and complexity of the transistors.

The main goal of this research is to determine what is the optimum voltage level shifter architecture that can be used for low-power, high-speed applications. This work is intended to give a better understanding of the performance characteristics of the different proposed models, and to help develop future energy-efficient and high performance VLSI systems. The results from this study are hoped to be valuable reference to researchers and designers in the area of low power CMOS circuit design and advanced SoC architectures.

1.2 THESIS OBJECTIVE

The main aim of this thesis is to perform a detailed comparative study of the different proposed architectures of voltage level shifters from the recent research study and to analyze their performance in modern VLSI applications operating in low power regime[7]. The primary objective of the study is to gain the understanding of the performance of various voltage level shifter models under different operating under different voltage and calculating their power and delays under different voltages and finding the bet preffered model for minimum delay and power dissipation.

1.3 THESIS ORGANIZATION

Chapter 1: Introduction

The chapter gives general background and motivation of the thesis work. It starts with presenting the application of low power and high-speed VLSI circuits within electronic applications, such as wireless sensor networks, biomedical systems, Internet of Things (IoT) system, portable electronics and SoC systems. Further discussion within the chapter sheds light on the ways voltage level shifters facilitate communication between different voltage domains, where the issue of minimization of power dissipation and propagation delay within today's integrated circuits is highlighted.

Chapter 2: Literature Review

Voltage level shifters are among the critical interface circuits implemented in contemporary low power VLSI systems. In multi voltage domain system designs, different circuit modules require different supply voltages according to their speed requirements. As such, it is necessary to incorporate voltage level shifters for establishing reliable intercommunication between low voltage and high voltage circuit modules. Continuous advances in scaling down CMOS technology coupled with increasing demands for low power portable electronic systems necessitate a need to develop voltage level shifters that are low in power dissipation, have low propagation delay, and high-speed operations.

Chapter 3: Simulations and Results

In this chapter the general work performed in the thesis is summarized. The main results of comparative analysis of voltage level shifter circuits of low power, low delay and high speed are discussed. The chapter emphasizes the benefits and drawbacks of various architectures described in terms of power dissipation, propagation delay, switching speed, voltage conversion range and circuit complexity.The obtained simulation results and comparative study are used to identify the most suitable architecture of voltage level shifter for modern low power and high speed applications. The voltage level shifters can be further improved in the future with respect to their scope and possible improvement in its design for further research work.

Chapter 4 : Conclusion and future scope

In this chapter the final analysis of comparative study of different designs is given and explains the best model which can be preferred best power dissipation and minimum delay. Future future scope is also discussed in the chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 A High-Performance and Low-Power Subthreshold Voltage Level Shifter Design

Working & Circuit Design

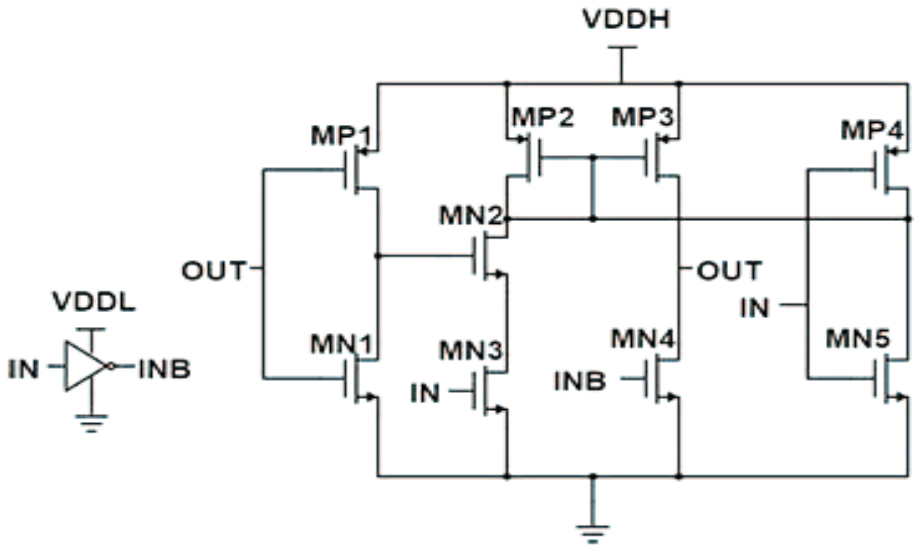


Fig 2.1 Design of High Performance Low Power Subthreshold Voltage Level Shifter

The level shifter in this work is designed by modifying a standard current mirror level shifter having extra feedback and control transistors to ensure the static current elimination and minimize the propagation delay. It works in two major phases, one for each transition in its inputs.

1. Standby State

Initially, IN = 0 V (low) and OUT = 0 V (low). The transistor MP1 is ON (gate low) and MN1 is OFF. The inverter between MP1 and MN1 gives a high signal at the gate of MN2, which switches off MN3, as IN is low. There is no current flow in the current mirror (MP2, MN2, MN3). Production is still low.2nd Input Transition: Low to High (IN = VDDLWhen IN rises to VDDL (low voltage domain), OUT is still low initially.

MP1 is ON (gate not changed from previous state), MN1 is still OFF. The node between MP1 and MN1 is made high and turns ON MN2There is a direct connection between the high IN and the ON of MN3.There is now a new path (MP2 → MN2 → MN3 to ground). This current is reflected in MP3 (current mirror pair MP2:MP3)MP3 can pull OUT up to VDDH (high voltage domain)When OUT is high, the gates of MP2 and MP3 are pulled FALLING by transistor MN5 (controlled by OUT through an inverter), thus maintaining them ON when the mirror path is turned off. This maintains the pull up strength without any static current.This is because the previously conducting path (MP2-MN2-MN3) is now switched off as the feedback mechanism (not explicitly described but deduced from the circuit operation) forces the gate of MN2 low.Result: OUT is switched from 0 to VDDH without the presence of static current. The feedback makes sure that once the transition is made, there will be no DC path Input Transition: High → Low (IN = 0) while OUT = VDDHIN falls to 0 VMN4 (gate connected to IN via an inverter? In fact, as can be seen from Fig. 2, when the signal from IN) goes ON, MN4's gate turns ON and pulls the output of OUT down to ground rapidlyAt the same time, MP4 is turned ON (its gate receives the same inverted signal) and the gate of MP3 is pulled high, causing MP3 to be turned OFF. This eliminates the pullup contention during the pull down phaseThe circuit returns to the standby state (IN = 0, OUT = 0).CASE 1- Initially IN=HIGH When NMOS MN5 is ON, it is grounded when MN2 is ON. MP3 and MP2 PMOS turns ON.MP3 is turned ON and Output is turned to VDDH(HIGH) CASE 2- When IN=LOW IN B becomes High.The output is grounded, and the output is LOW.

KEY FINDINGS

1. 77.42% improvement in propagation delay compared to recent designs in 90nm CMOS.
2. Eliminates static current when input is high.
3. Excellent performance across process corners (FF, FS, SF, SS).
4. Operates over wide temperature range (–25°C to 125°C).
5. Tested on multiple technology nodes (45nm, 65nm, 90nm, 180nm).

6. More complex than basic current mirror due to added feedback and auxiliary transistors.

7. Requires careful sizing of feedback transistors for proper operation.

8. Feedback loop may increase transient power during switching.

9. Not the smallest in area compared to some designs.

2.2 ULTRA-LOW POWER, AREA EFFICIENT AND HIGH-SPEED VOLTAGE LEVEL SHIFTER BASED ON WILSON CURRENT MIRROR

Working & Circuit Design

This voltage level shifter is a reflected output voltage level shifter based on a Wilson current mirror. Its schematic is the Fig. 2 of the paper. The innovations are:

Replacement of pass transistor (Mn2) to reduce delay in the inverter used for the input.

Addition of a PMOS diode (Mp1) in series with Mn1 to create a voltage difference between nodes Q1 and Q4.

Avoiding simultaneous conduction

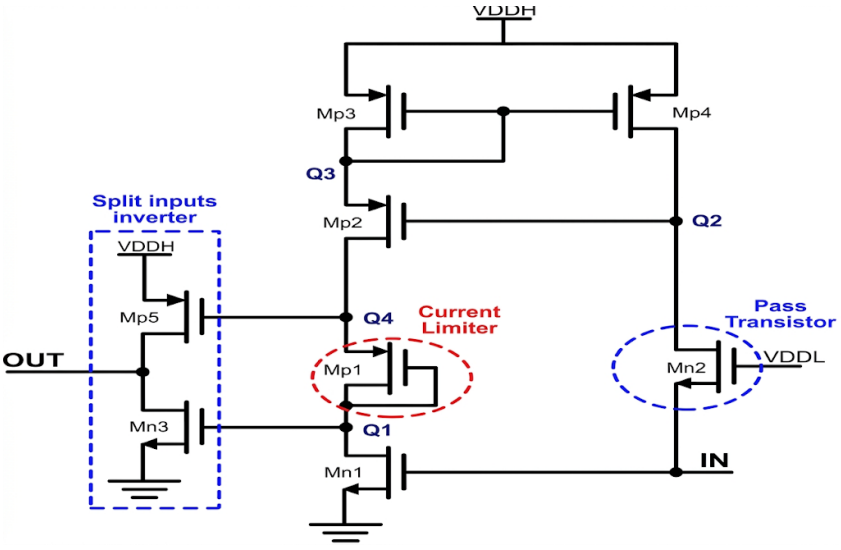


Fig 2.2.1 Design of Ultra Low Power High Speed Voltage Level Shifter

with a split input output buffer (Mn3, Mp5). Smallest possible PMOS diode (Mp3) for minimising parasitic capacitance.

Step by Step Operation ,Initial Standby State (IN = 0 V, OUT = 0 V) IN is low (VDDL level, e.g., 0.42 V)Transistor Mn2 is OFF (its gate is connected to IN? Actually, from Fig.2, Mn2 is a pass transistor connecting input to internal node; need to infer). In normal operation of the circuit, Mn2 passes the signal being passed to its input. Mp1 (PMOS diode) is forward biased Mp1's gate and drain are shorted and thus forms a diode.The output buffer (Mn3, Mp5) is in a known state. The input low keeps the mirror inactive, so that no static current flows through the mirror.Low to High Transition (IN rises from 0 to VDDLIf IN is high, then Mn2 is turned ON, thus sending the high signal to the internal node (gate of Mn1Actually there's a path connecting Mn1 with IN.Mn1 turns ON, pulling down node Q1Since Mp1 (diode connected PMOS) is in series with Mn1, the voltage at Q4 is raised by a voltage of Vth above Q1, so that there is a voltage difference between Q1 and Q4This discrepancy keeps the output buffer transistors Mn3 and Mp5 from switching on at the same time thereby eliminating short circuit current during switchingWhen the Wilson current mirror (Mp2, Mp3 and the pull down NMOS) begins to mirror current. The current through Mn1 will mirror at the output branch and attract node OUT to VDDHThe output buffer then feeds into the final outputThe input inverter is removed which means that the falling edge delay of the input signal is eliminated, and thus the overall propagation delay is also reducedis the reduction of IN from VDDL to 0.3. High to Low Transition (IN goes down from VDDL to 0Internal node charges are conserved (charge is not lost), but the internal node is turned OFF when IN goes low? The circuit has replaced an inverter with a pass transistor, thus making the transition fasterThe pull down NMOS (Mn1) turns OFF, and the other path of the Wilson mirror (through Mp3) pulls the output lowThe diode Mp1 ensures that node Q4 does not fight the transitionThe output buffer has a split input which makes it impossible for Mp5 and Mn3 to be ON simultaneously, limiting the amount of “crowbar” current.

KEY FINDINGS

1. Can convert input as low as 80 mV to 1.8 V.
2. Very low power dissipation: 123.1 nW at 0.4 V/1.8 V, 1 MHz.

3. Smallest area among compared designs (63 μm²).
4. No static current in steady state.
5. Robust across PVT variations (Monte Carlo simulation).
6. Limited to 0.18 μm CMOS technology; not validated in advanced nodes.
7. Propagation delay of 23.7 ns (moderate, not ultra-fast).
8. Minimum VDDL of 80 mV works only at very low frequencies (10 kHz).
9. PMOS diodes in series increase output resistance.

2.3 An Energy Efficient Voltage Level Shifter

Working of the Proposed EVLS Model

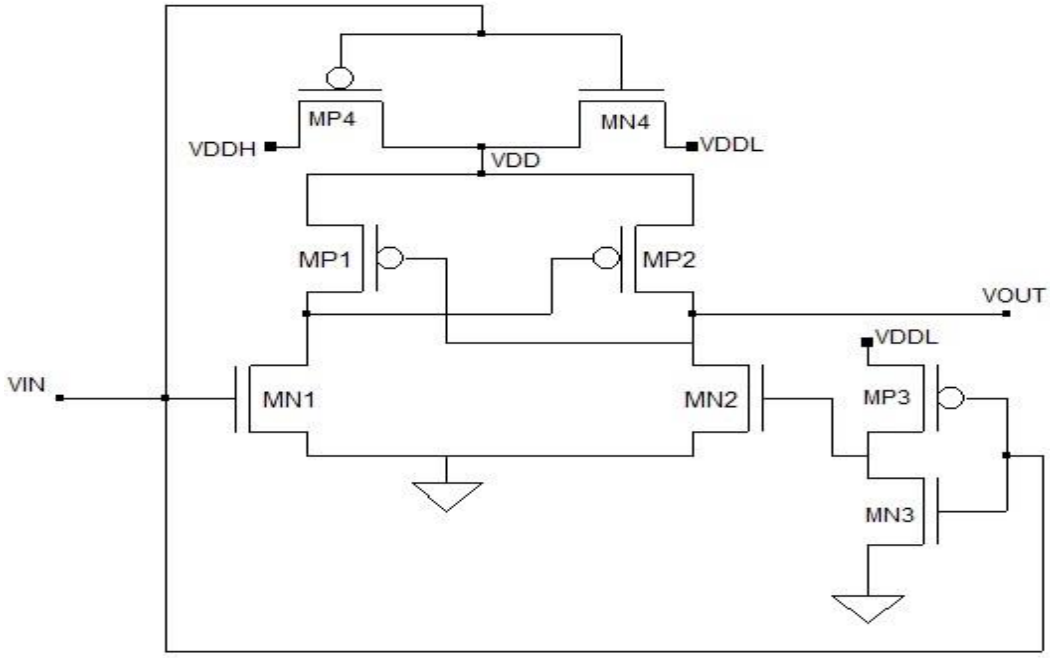


Fig 2.3.1 Design Novel Energy Efficient Voltage Level Shifter

One of the important advantages of the proposed Efficient Voltage Level Shifter (EVLS) design is that the device automatically selects whether to conduct the voltage level up or voltage level down operation based upon the value of the input voltage applied to the circuit.

There are a total of ten transistors in the proposed EVLS circuit, which works under two supply voltagesHigher supply voltage (VDDH) = 1.2VLower supply voltage (VDDL) = 0.6To understand how the circuit works, one may divide its operation into two parts:Part 1 : This portion works as a voltage selection circuitPart 2 : This part of the circuit performs voltage level shifting operationIn the first part of the circuit, transistors MP4 and MN4 work as a 2×1 multiplexer. These two transistors decide whether to take higher supply voltage or lower supply voltage according to the input voltage VIN. **Level-Up Shifting Operatio**When VIN = 0.6V, the circuit operates the level-up shifting. At this situation, the MP4 device becomes ON while MN4 becomes OFF. With that, the higher voltage source of the circuit, VDDH, comes into effect.

Also, MN1 becomes ON while MN2 becomes OFF. In the PMOS group, MP1 becomes OFF and MP2 becomes ON. Through this operation, the output will be connected to the higher power supply, VDDH Therefore, the output voltage increases from 0.6V to 1.2V. Thus, the circuit successfully changes a lower power input to a higher output voltage. This process is called level-up shifting voltage In the simulation wave form, when the input operates on 0.6V, the output shifts to 1.2V successfully Down Operation For the input voltage VIN of 1.2 V, the circuit performs the automatic level-down shifting process. In this situation, the transistor MP4 is turned OFF, while transistor MN4 gets turned ON. Hence, the lower voltage VDDL is used within the circuit as the supply voltage. In addition to this, the transistor arrangement also undergoes some change in the switching process. The transistors MN1 and MN2 will be turned ON and OFF respectively, while MP1 is turned OFF and MP2 is turned ON. This operation connects the output node to VDDL Hence, due to this, the output voltage appears to be equal to 0.6 V, although the input voltage is 1.2 V. Therefore, the circuit effectively accomplishes voltage level-down conversion From this analysis of the output waveform, it is clear that the proposed circuit can perform voltage level-down conversion effectively.

KEY FINDINGS

1. Bidirectional operation – performs both level-up and level-down shifting.
2. Simple circuit with only 10 transistors.
3. Low average power: 24.71 nW.
4. Low average delay: 2.05 ns.
5. Very narrow voltage range: only 0.6 V ↔ 1.2 V.
6. Not suitable for true subthreshold inputs (0.6 V is near-threshold).
7. Higher delay for down-shift (2.88 ns) compared to up-shift (1.23 ns).
8. Lacks advanced static-current elimination features.

2.4 An Efficient Wide Range 2.45ns ,4.38Nw Subthreshold Voltage Level Shifter Using 45 nm CMOS Technology

Working and Circuit Design

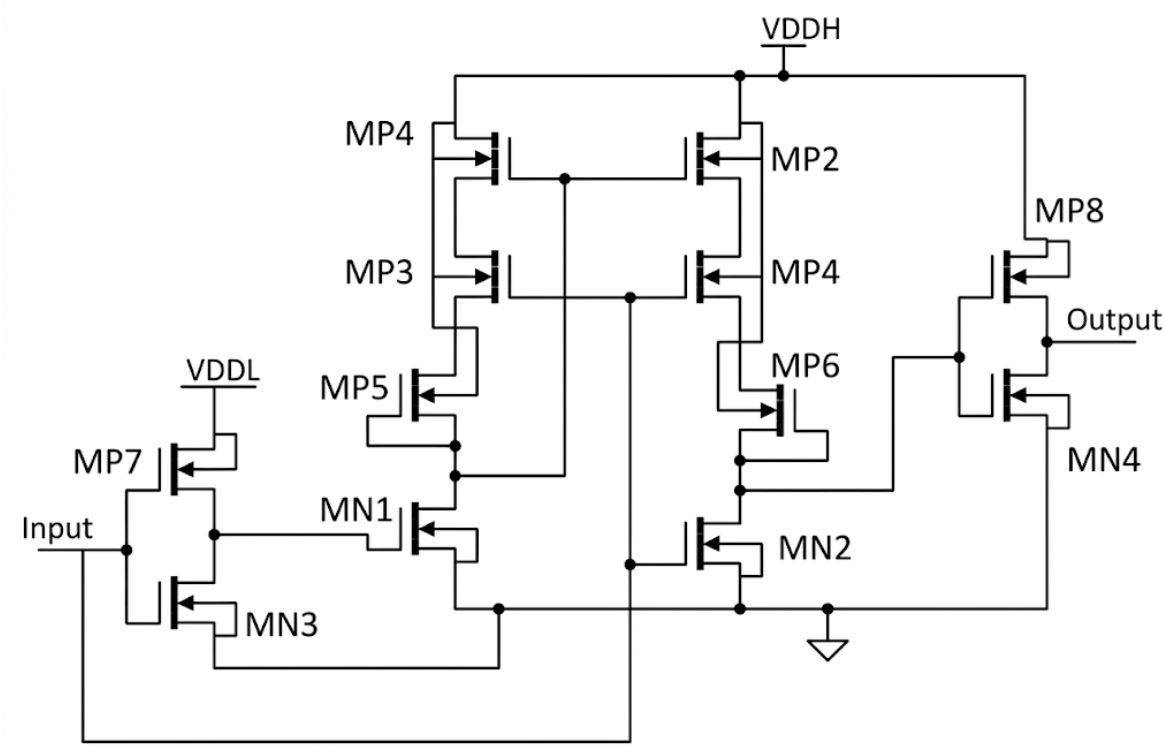


Fig 2.4.1 Design of an Energy Efficient Subthreshold Voltage Level Shifter

When the input is low (0 V)The input inverter (made of MP7 and MN3) produces a high inverted signalA high signal switches on transistor MN1 (this is a low voltage, fast transistor)Meanwhile, the low input directly turns off MN2, but turns on MP3 and MP4When a series of transistors (MP1 → MP2 → MP5 → MN1) form a connection between the high side supply VDDH and the ground, they provide a path for current to flow from VDDH to VSS. A current passes through thisA current is mirrored to the other side of the circuit, bringing the internal output node to VDDHThe output inverter at the end, then produces a clean high output of 1.1 VWhen the input is high (VDDL, e.g., 0.1 V)The input inverter now turns into a LOW output (disables MN1)The input is connected to the high input, turning on MN2Once the pull down network is turned on, the internal output node is discharged to ground.That is then inverted by the output inverter to give a low output at 0 V.

KEY FINDINGS

1. Reduced transistor count (11 vs. 12 in existing design).
2. Lower power: 76.34 nW at 0.4 V/1.8 V, 1 MHz (vs. 149.5 nW in existing).
3. Lower delay: 21.0 ns (vs. 23.7 ns).
4. Works for inputs below threshold voltage.
5. Requires capacitor C1, which increases area in integrated implementation.
6. Output directly coupled via capacitor – may cause voltage droop at low frequencies.
7. Limited to 180 nm technology in simulation.
8. No Monte Carlo or PVT corner analysis reported.

2.5 Design and Optimization of low power and high speed voltage level shifter circuit using 45nm and 180nm MOSFETs with Variable Voltage source

Working and Circuit Design

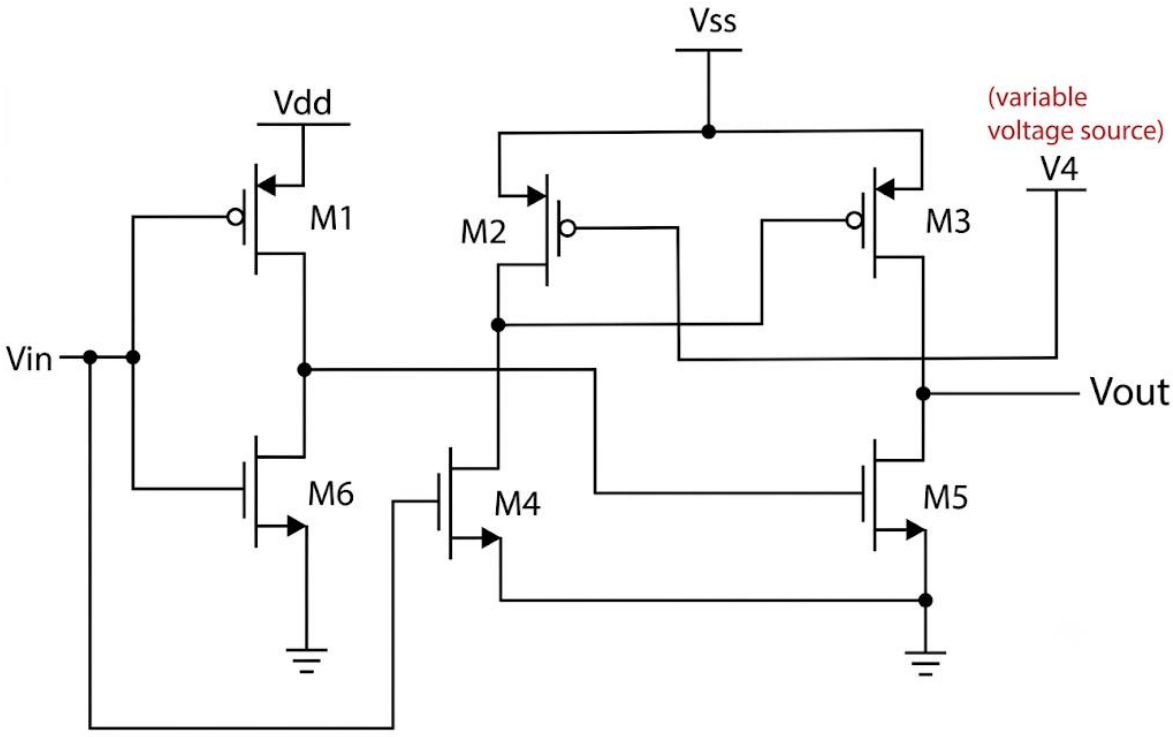


Fig 2.5.1 Design of Low Power High Speed Voltage Level Shifter using Variable Voltage Source

Stage 1: The “Flip It” Stage (Inverter) The basic inverter consists of two tiny transistors M1 and M6 of size 45 nm which are extremely small and fast. This stage produces a high output(~1.1 V) when it receives a low (0 V) input. When the input is high (~1.1 V), it outputs low (0 V) This is the medium quantity that's included into the circuit. It can reliably switch on the next stage when the input voltage on the previous stage is as low as 0.1 V Progress to Stage 2: The “Bridge” Stage (Level Shifter One NMOS transistor (M5) can be used as a controlled switch. Connects Stage 1's output to the last stage. It does not increase the voltage but amplifies perfectly the input signal after isolating and conditioning it in the final stage The “Kick It Up” Stage (Cross Coupled PMOS Pair) is the third stage This is the middle bit of the circuit. M2 and M3 are two PMOS transistors that are fabricated in the 180 nm technology, which is a more robust technology, and are used in a cross coupled latch They are connected to the 3 V power supply The signal from Stage 2 causes this latch to be triggered. The latch has positive feedback: If it begins to switch, it will quickly jump to either 3 V or 0 V The latching action is responsible for the blistering speed of this circuit (0.33 ns). No delayed action between pull up and pull down , just the latch commits Final Output Buffer (M4, M5 , yes, I'm naming overlapping!)The output of the latch is then buffered by two more NMOS transistors (called M4 and M5 in the paper) to ensure a clean, full swing 3 V or 0 V signal that can drive real loads**.**

KEY FINDINGS

1. Extremely low power: 4.38 nW.
2. Very low delay: 2.45 ns.
3. Uses advanced 45 nm CMOS technology.
4. Simple three-stage architecture.
5. Very narrow input voltage range: only shifts 75–100 mV input to 1.1 V.
6. Requires multiple threshold voltages (low-VT and high-VT), increasing fabrication complexity.
7. Output voltage only 1.1 V (not suitable for 1.8 V or 3.3 V domains).
8. Limited comparison with state-of-the-art designs.

2.6 Dual Current Mirror Technique Based Energy Efficient 50mV to 1V Voltage level shifter

Working and Circuit Designs

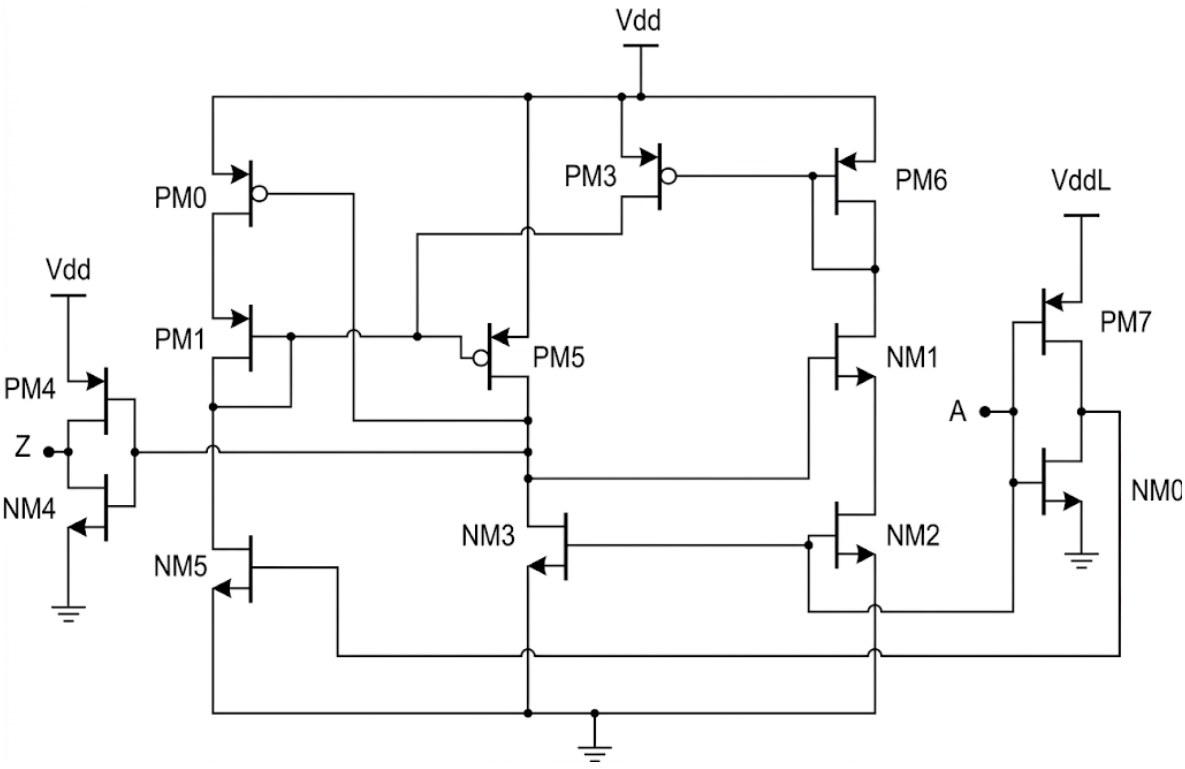


fig 2.6.1 Design of Current Mirror Based Energy Efficient Voltage Level Shifter

Input low (0 V)Input inverter output = high (VDDL).NM5 turns ON.

When a Wilson mirror is activated, the node (drain of PM5) charges to 1V inside the circuitSplit inverter (which is inverting) sees that 1 V and outputs 0 V (at the high supply ground). Final output = 0 VTherefore, the output has the same logic state as the input, and so the output is lowOnce the Input is High (VDDLNow the input voltage is increased to VDDL (say 0.5V)Input inverter: PM7 is turned OFF and NM0 is turned ON. The output of the inverter is low (0 V)Turning OFF the first mirror , NM5 is switched off by that low signal; the first Wilson mirror is no longer conductingThe other NMOS transistor NM3 (see the circuit description) is connected directly (or for some reasons) to the high input and thus will be activated. NM3 is one of the second mirror of Wilson. When NM3 is switched ON, it pulls down the gate of another NMOS (NM1) and turns NM1 OFF. In the meantime, another path

uses the second mirror to bring the internal output node down to 0 VAt the output stage: The split inverter input voltage is now low (close to 0 V). It is inverting, so it will output high , 1 V.So, when input is high, output is high (1 V). Once again the logic state is maintained.

KEY FINDINGS

1. Extremely low propagation delay: 40.1 ps (picoseconds).
2. High voltage conversion: 3.3 V → 6.5 V.
3. Low transistor count: 8.
4. Good duty cycle (50.3%) and slew rate (205 G).
5. Reported power consumption of 43.57 W – likely a typo (should be μW), but as written it is impractically high.
6. High voltage range (3.3 V to 6.5 V) – not suitable for low-power subthreshold applications.
7. No subthreshold operation (VDDL = 3.3 V is far above threshold).
8. 180 nm technology – large feature size.

A Low Power and High Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull up Network

Working and Circuit Design

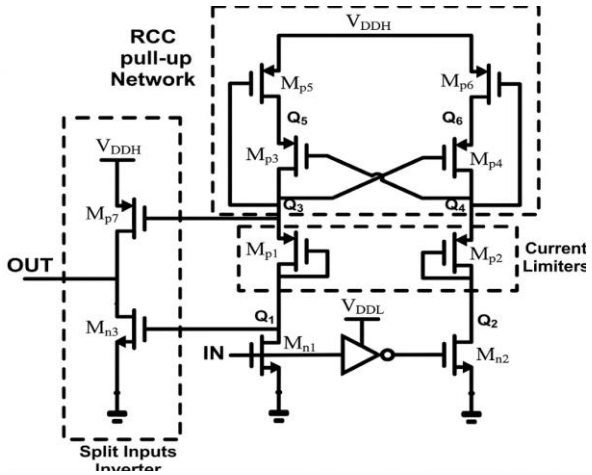


Fig 2.7.1 Design of Low Power and High Speed Voltage Level Shifter Based of Regulated Cross Coupled Pull up Network

The voltage level shifter circuit here operates using a DCVS structure with a Regulated Cross-Coupled pull-up circuit. The main components of the voltage level shifter are:

1.Regulated cross-coupled PMOS pull up network

2.NMOS Pull down Network

3.RCC Transistors

4.Split input Output Inverter with current limiting Transistor1. Structure of the RCC Pull-Up Network

The proposed pull-up circuit comprises four PMOS transistors MP3, MP4, MP5, and MP6 connected in an enhanced cross-coupled topology. During conventional DCVS circuit operation, the PMOS transistors used for pull-up are always in a highly active state during switching transitions, causing intense conflict with the pull-down NMOS transistors. As a result, internal node discharge is relatively slow and power consumption is high.In the present case, MP5 and MP6 transistors serve as regulator transistors, which regulate the pull-up PMOS transistor current through MP3 and MP4 transistors dynamically[28]. Due to the regulation, pull-up action at the beginning becomes relatively weak during the transition process, thereby enabling quick discharge of the internal node by the pull-down NMOS transistors. After this process, the feedback restores pull-up action for rapid change in output states. Thus, the dynamic regulation feature plays a significant role in achieving faster switching speed and low dynamic power consumption.

2. Initial Steady-State Condition Assume initially Input IN = LOW Node Q1 = HIGH Node Q2 = LOW Output OUT = LOW Under this conditionMP3 and MP6 remain ONMP4 and MP remain OFFMN1 remains OFF MN2 remains ON Since MP3 is ON, node Q1 stays near the high voltage level VH, while node Q2 remains near ground potential. At this stage, the circuit remains stable with negligible static current flow because one branch of the pull-up network is inactive.

3. Low-to-High Input Transition

When the input goes from LOW to HIGH, the following series of actions takes place:

Step 1: Activation of Pull-Down Path MN1 is turned ON MN2 is turned OFFAs a result, node Q1 starts being discharged towards GND. With MP5 making the pull-up current of the left branch through MP3 weaker, the discharge happens much quicker than that of any traditional DCVS circuits. Thus, the parasitic capacitance at the node of Q1 is quickly discharged. Step 2: Regenerative Feedback Activation As Q1 is going down both MP4 and MP5 are getting activated. Thus, the node Q2 begins charging up to VDDH, causing MP3 and MP6 to shut off because of their cross-coupling action. In result, the following happens:pull-up current in the left branch gets weakerpull-up strength of the right branch gets strongerRegenerative switching speeds up At this point, the RCC circuit provides for extremely quick voltage switching due to continuous amplification of the difference between Q1 and Q2. Step 3: Finish Transition and Elimination of Static Current PathsWith Q2 approaching the high voltage level:MP6 shuts OFF completelyMP3 also shuts OFFStatic current paths are thus eliminatedThe MN1 transistor now pulls Q1 to ground level even when the input voltage is less than the threshold voltage of the MOS transistor. This property allows for efficient sub-threshold voltage translation. Since both the pull-up and pull-down paths are not conducting simultaneously, the static power consumption is very small.High to Low Input Voltage TransitionIf there is a change in the input voltage from high to low, then:The MN1 transistor switches OFFThe MN2 transistor switches ONThe node Q2 gets discharged and Q1 gets charged towards the high supply voltage level due to regenerative action. The MP3 and MP6 transistors conduct while the M P4 and MP5 transistors shut OFF.

5. Role of Current Limiting TransistorsThe total circuit comprises PMOS diode-connected transistors MP1 and MP2 in parallel with the pull-down resistor network. The two transistors act as current limiters to minimize the short-circuit current during the switching process.The diode-connected PMOS acts to increase the voltage levels of the internal node Q3 and Q4 above ground potential. This increases the voltage difference between the internal nodes. This ensures that pull-up and pull-down components within the output inverter cannot conduct simultaneously. Consequently:The short-circuit current is reduced The dynamic power dissipation is minimized There is improvement in switching performance

6. Split-Input Output Inverter

The suggested design uses another technique for the design of the output inverter stage which is called a split-input inverter. It means that unlike the common inverter when both PMOS and NMOS transistors conduct simultaneously, this scheme allows for the division of control signals for pull-up and pull-down circuits.In this case, short-circuit currents become minimum and thus decrease output power consumption.

KEY FINDINGS

1. Wide voltage shifting range: 0.1 V to 3 V.
2. Very low delay: 0.33 ns.
3. Small area: 15.84 μm^2.
4. Uses MTCMOS and subthreshold sizing techniques.
5. Very high power consumption: 171.05 mW (milliwatts, not microwatts) – about 1000× higher than other low-power designs.
6. Requires both 45 nm and 180 nm devices – dual technology integration is not standard.
7. No explicit static current elimination mechanism.
8. High power makes it unsuitable for battery-operated devices.

2.8 A Quick and Power Efficient Controlled Voltage Level Shifter Using Cross Coupled Network

Working and Circuit Design

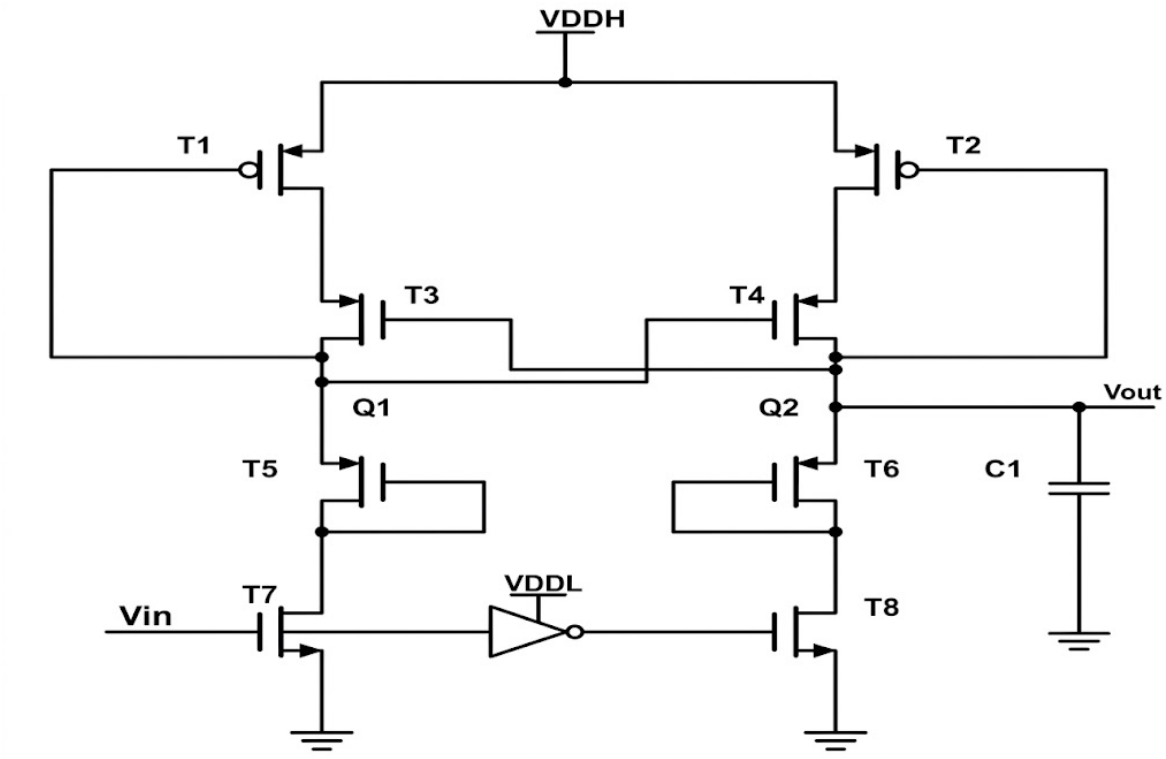


fig 2.8.1 Design of a Quick and power efficient controlled voltage level shifter using Cross Coupled Network

Level Shifter: The voltage level shifter described here is based on the RCC level shifter circuit. The level shifter circuit diagram is shown in Figure 6 of the research paper. This level shifter consists of: Cross coupled PMOS pull up stage Pull down NMOS stage Regulating PMOS stage Limiting current stage Output capacitance coupling stage The major difference between the RCC level shifter and the proposed level shifter lies in the absence of the split input/output inverter in the proposed level shifter. Instead, in the proposed design, the output stage is directly connected to the internal node Q2 through capacitor C1.

1. Cross-Coupled Pull-Up Network

The cross-coupled section of the proposed level shifter is made up of the PMOS transistors T1, T2, T3, and T4. Among these:T1 and T2 are the major pull-up transistors T3 and T4 are regulating transistors Cross-coupling produces regenerative positive feedback. This results in regeneration, which speeds up the charging and discharging of nodes Q1 and Q2, hence the switching speed of the level shifter. In an ordinary DCVS level shifter, there is high contention between the pull-up PMOS transistor network and the pull-down NMOS transistor network while in transition. This contention leads to higher currents that cause higher delays and power consumption. The RCC technique reduces the effect of the contention by weakening the pull-up network through the regulating transistors T3 and T4. Consequently, The pull-down transistors will be able to discharge the nodes faster The contention current will be lowered The dynamic power will be reduced .

2. Initial Operating Condition

Assume initially: Q1 = High Q2=Low In this case: Transistors T2 and T3 stay ON Transistors T1 and T4 stay OFF Transistor T7 stays OFF Transistor T8 stays ONAs transistor T2 is ON, the node Q1 will continue to be charged towards the high supply voltage . Simultaneously, transistor T8 provides the discharge path for the node Q2, which will remain close to zero volts.

3. Low-to-High Input Transition

In case of LOW to HIGH transition at the input, then the following steps will be performed:

Step 1: Pull-Down Transistor Turn ON T7 is turned ON T8 is turned OFF Now transistor T7 has provided the conducting path for current flow from Q1 to ground. This means that Q1 discharges very fast due to reduction in current by the RCC regulating transistors.

Step 2: Positive Feedback Regeneration As voltage at Q1 is reduced, T1 gets turned ON T4 also gets turned ON T2 and T3 get turned OFF Now regeneration takes place in case of cross coupled P-channel MOSFETs. The moment whenT1 is turned ON, then the voltage at Q2 starts charging towards VDDH Increase in voltage at Q2 means that T2 turns OFF even more, hence the discharging of Q1 is accelerated.

Hence, the regeneration keeps on amplifying the difference in voltage at Q1 and Q2 nodes. Therefore, due to positive feedback operation,

High transition speed is achieved Peak propagation delay is minimized The voltage transition is faster

4. Capacitive Output Coupling

One of the most important modifications in the proposed circuit is the removal of the split-input output inverter. Instead of using an inverter stage: Output node is directly connected to Q2 through capacitor C1C_1C1 This modification provides several advantages:Reduced Transistor Count The output inverter and associated split-input circuitry are eliminated, reducing the overall number of transistors. Reduced Power Consumption Since no inverter switching occurs at the output stage: Short-circuit current reduces Dynamic switching power decreases Reduced Delay Removing the inverter stage eliminates additional gate delay, thereby improving overall speed. Reduced Silicon Area Fewer transistors directly reduce layout area and parasitic capacitance**.**

5. Role of Sub-Threshold PMOS Operation

One key characteristic of the designed circuit is the operation of the PMOS transistors constantly around the sub-threshold point. The PMOS transistors never enter into the OFF state since their gate-source voltage is always approximately equal to: VDS=VDDH−VGS There are two main advantages of operating at sub-threshold voltage levels:Quicker Operation As the PMOS transistors are in the partially conducting state initially, it takes less time to activate them. Lower Contention Current Due to proper pull-up strength control, the pull-down NMOS transistors overcome the pull-up transistors

6. Leakage Current Reduction

Limiting transistors are used to minimize leakage currents that occur due to the pull-up network. In the case of traditional cross-coupled designs: Large static current may be drawn during switching states The contention between pull-up and pull-down network leads to increased power consumption A limitation transistor limits the current and enhances power efficiency. Thus: The leakage current gets reduced Static power consumption becomes less PDP gets optimized

KEY FINDINGS

1. Very low propagation delay: 0.959 ns.
2. Low power: 106.6 nW.
3. Low transistor count: 13.
4. Works across frequency (1 MHz – 100 MHz) and temperature variations.
5. Post-layout simulation in Cadence.
6. Limited output voltage: only 1 V (not suitable for higher voltage domains).
7. Voltage range: 0.5 V – 1 V (minimum 0.5 V, not deep subthreshold).
8. Dual current mirror increases matching complexity.
9. Comparatively higher power than some ultra-low-power designs.

2.9 Design and Analysis of High Speed Voltage Level Shifter Based on Wilson Current Mirror

Working

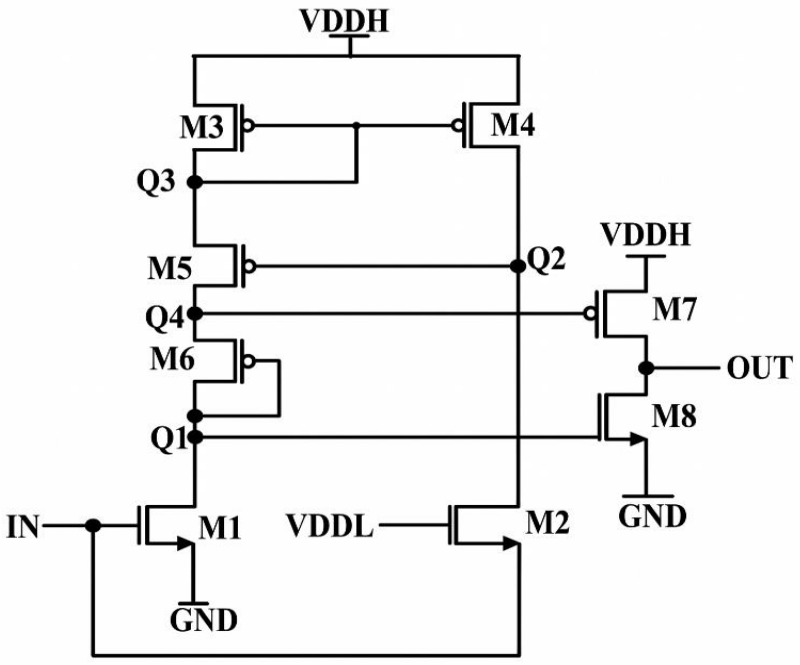


Fig 2.9.1 Simulations of High Speed Voltage Level Shifter based on current mirror

The suggested voltage level shifter circuit will be built on the basis of a Wilson Current Mirror Level Shifter (WCMLS). The entire circuitry includes: Pull down NMOS transistors (M1, M2, M8) Pull up PMOS transistors (M3, M4, M5, M6, M7)Wilson current mirror PMOS diode current limiter Split input output inverter The circuit works with the following two distinct voltage supplies: Low voltage supply VDDL=3.3V High voltage supply VDDH=6.5V The overall aim of the circuit is to generate a high output voltage signal from a low voltage input signal with minimum delay and minimum power consumption.

Structure of the Circuit

The main aspect of the suggested design is the Wilson current mirror circuit constructed using PMOS devices M3, M4, M5, and M6. In contrast to traditional current mirrors, Wilson current mirror provides better precision in current transmission and minimizes static currents in switching processes that results in more rapid voltage conversion.

The main components of the pull-down circuit include NMOS devices M1 and M2. These elements are responsible for the process of node charges at Q1 and Q2 nodes depending on changes in the signal input. As for the output circuit, the split-input inverter is created with the help of PMOS device M7 and NMOS device M8.

Initial Condition of the Circuit Consider first that the input is LOW. In this case M1 NMOS is off M2 pass transistor is on Q2 internal node goes LOW M3 PMOS transistor is turned on M4 PMOS transistor is off The output of the inverter becomes HIGH as Q1 becomes HIGH. The circuit is thus stable with very low standby current since the circuit is active on only one side. Low-to-High Input Transition When the input changes from LOW to HIGH, the operation of the circuit proceeds in several stages.

Step 1: Activation of Pull-Down Network As the input becomes HIGH: NMOS transistor M1 turns ON Pass transistor M2 turns OFF The M1 switch now offers a discharge path for the node Q1 to ground. The result is that the voltage at Q1 decreases quickly. This is because the Wilson current mirror causes the pull-up network to be weakened during the transition.

Step 2: Wilson Current Mirror Operation

With decrease in voltage at Q1 point, transition is brought to right side of the circuit by the Wilson current mirror. Following effects of the voltage drop across Q1 are seen: The PMOS transistor M4 starts conducting. The node Q2 is pulled up towards VDDHV-VDDH. With increase in voltage across Q2: The transistor M3 cuts off slowly. The process of regenerative switching starts. The regenerative feedback enhances the process of charging Q2 and increases the speed of discharge of Q1

Role of the Pass Transistor One of the most crucial changes in the proposed design is the change from the use of the traditional inverter to that of the pass transistor M2.The introduction of the traditional inverter results in extra delay in the level shifter during the falling edge transition of signals. By substituting the inverter with the pass transistor, it leads to: Faster propagation of the signal Less delay for falling edges Lower circuit complexity Lower power consumption

Role of the PMOS Diode Current Limiter The PMOS transistor M6 is connected as a diode between internal nodes Q1 and Q4, and it acts as a current limiting device. The presence of a PMOS diode makes the voltages at Q1 and Q4 different, thus ensuring that the PMOS transistor M7 and NMOS transistor M8 cannot turn on simultaneously in the output inverter. Consequently, Short-circuit current is decreased, and The dynamic power consumption is minimized. This way, the use of the PMOS diode enhances both the speed and the efficiency of the proposed design.

Operation of Split Input Inverter The proposed design employs the output stage as a split input inverter circuit. In contrast to the standard inverter, where both the transistors receive the same input signal, in the case of a split input inverter, individual inputs are fed into PMOS transistor M7 and NMOS transistor M8 respectively**.** Consequently: The short-circuit current drops Dissipation at the output decreases The transition of the signal is made faster and cleaner Split-input inverter plays a significant role in ensuring high speed and low power consumption. Transition of Input from HIGH to LOW State In case of the transition of the input signal from HIGH to LOW state: The NMOS transistor M1 switches OFF The pass transistor M2 switches ONAt that moment, the node Q2 begins to discharge itself, whereas the node Q1 gets charged to VDDH level. Similarly, here the transition of the signal takes

place through the Wilson current mirror.Regenerative feedback between the PMOS transistors makes the transition fast and restores the circuit back to its steady-state condition.

KEY FINDINGS

1. Can shift input as low as 80 mV to 1.8 V.
2. Low power: 149.5 nW at 0.4 V/1.8 V, 1 MHz.
3. Simulated in 180 nm technology.
4. Uses split-input inverter to reduce short-circuit current.
5. Not a novel design – it is an implementation of an existing topology (Kabirpour & Jalali).
6. Moderate delay: 23.7 ns.
7. Larger area compared to the original implementation.
8. No comparison with more recent designs (2020–2024).

2.10 Rapid Low Power Voltage Level Shifter Utilizing Regulated Cross Coupled Pull Up Network

Working & Circuit Design

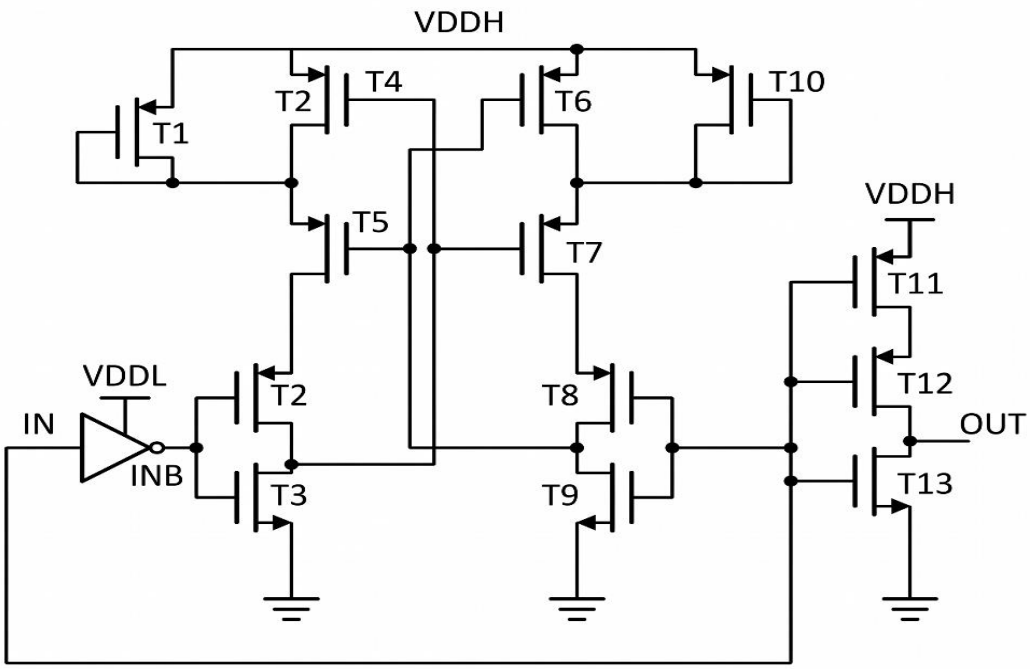


Fig 2.10.1 Design of Rapid Speed Low Power Voltage Level Shifter utilizing regulated cross coupled pull up network

This level shifting technique employs the use of a differential cascode voltage switch coupled with a regulated cross-coupled pull-up network to construct the voltage level shifter. The use of this RCC pull-up network regulates the strength of the pull-up transistor, thereby facilitating faster charging and discharging within the internal nodes of the circuit. This leads to an increase in switching speed and reduction in power consumption.

The major components that constitute the circuit include the following :Pull-up PMOS transistors Pull-down NMOS transistors Cross-coupled RCC network

Split-input inverter Current limiting PMOS transistors The process in which the circuit operates can be divided into three main phases.

Step 1: Initial ConditionFirstly, it should be assumed that:The input voltage is LOW Node Q1 is HIGH Node Q2 is LOW In this case, the pull-up p-type MOSFET that is connected

with Q1 will be on, and Q1 will stay HIGH, close to the high voltage supply level VDDH. Also, node Q2 will stay discharged by the pull-down structure.

Step 2: High Input TransitionWhen a HIGH input signal is provided,The NMOS transistor Mn1 conductsThe NMOS transistor Mn2 does not conduct With the conducting NMOS transistor Mn1, the node Q1 starts discharging from VCC to ground. The discharge occurs relatively quickly because the current in the PMOS transistor Mp3 gets limited by the OFF condition of the PMOS transistor Mp5. The RCC network dynamically controls the strength of the pull-up operation.The voltage on the node Q1 keeps falling At this point,The PMOS transistors Mp4 and Mp5 conductThe PMOS transistors Mp3 and Mp6 do not conduct This causes the node Q2 to start charging to the high supply voltage VDDHV_{DDH}VDDH. Step 3: Sub-Threshold OperationA very crucial aspect of this circuit design is that the pull up transistors do not turn off fully but rather enter the sub-threshold condition when:VGS = VDDH , VH The operation in the sub-threshold region will enable the pull-up transistors to switch faster during the next transition and thus reduce the delay time.In case Mp3 is completely turned off, then Mn1 will be able to discharge Q1 even in case of a very small input voltage. With such kind of operation:

- Static current will be almost zero

- Power consumption will decrease

- The switching speed will increase

In this way, the circuit will be capable of raising the sub-threshold input voltages to desired values.

Split-Input Inverter Operation The output part of the circuit employs split-input inverter to minimize short-circuit currents occurring during the transition processes. Transistors Mp1 and Mp2 keep intermediate voltage levels on nodes Q3 and Q4. The voltage level difference on nodes Q1 and Q3 does not allow the PMOS and NMOS transistors of the output inverter to turn ON at the same time. Consequently, short-circuit currents are prevented from happening: Since short-circuit currents are minimized, dynamic power dissipation is reduced The transition process becomes faster and more efficient The proposed split-input inverter contributes to improving performance of the voltage level shifter. Low Input Transition

In case there is a transition from HIGH to LOW on the input, the circuit operation is reversed to that of the former case:Mn1 transistor will be turned OFF Mn2 transistor will turn ON Q2 node discharges

KEY FINDINGS

1. Extremely low total power: 5.98 nW (static power 0.08 nW).
2. Very small area: 1.4 μm^2.
3. Low delay: 1.88 ns.
4. Very low power-delay product (PDP): 11.24 nW·ns.
5. Works at 115 MHz input frequency (higher than most).
6. Excellent PVT corner analysis.
7. Minimum VDDL: 190 mV (not as low as 80 mV or 45 mV in other designs).
8. 7 nm CMOS technology – expensive and not accessible for all designers.
9. Pass transistor introduces some leakage current.
10. Requires careful sizing for reflected-output mechanism.

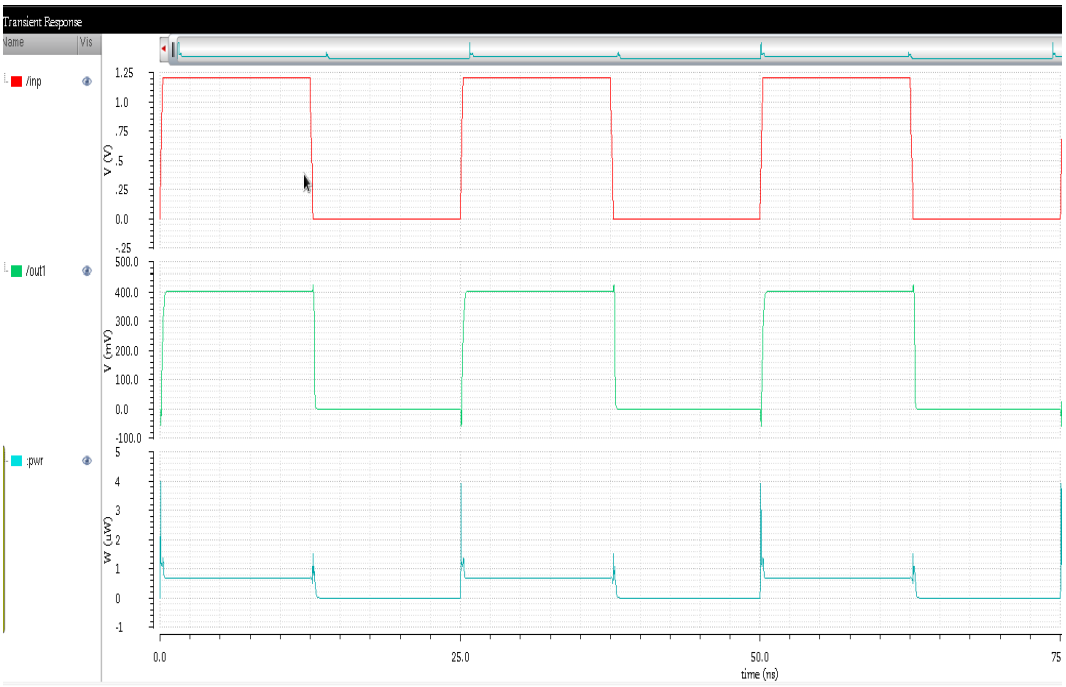
CHAPTER 3

SIMULATIONS AND RESULTS

The Simulations are Performed on Cadence Virtuoso on 45nm Technology under Various Input Voltages at 27˚ C

1 A High-Performance and Low-Power Subthreshold Voltage Level Shifter Design

Simulations and Results



S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	105.1E-12	15.06E-12	7.582E-9	198.7E-6
2	1	64.24E-12	15.1E-12	7.582E-9	250.7E-6
3	1.5	49.13E-12	15.08E-12	7.579E-9	319.2E-6
4	2	34.11E-12	15.11E-12	7.543E-9	350.7E-6

Fig 2.1.3 Result Table of High Performance Low Power Subthreshold Voltage Level Shifter

2 ULTRA-LOW POWER, AREA EFFICIENT AND HIGH-SPEED VOLTAGE LEVEL SHIFTER BASED ON WILSON CURRENT MIRROR

Simulations and Results

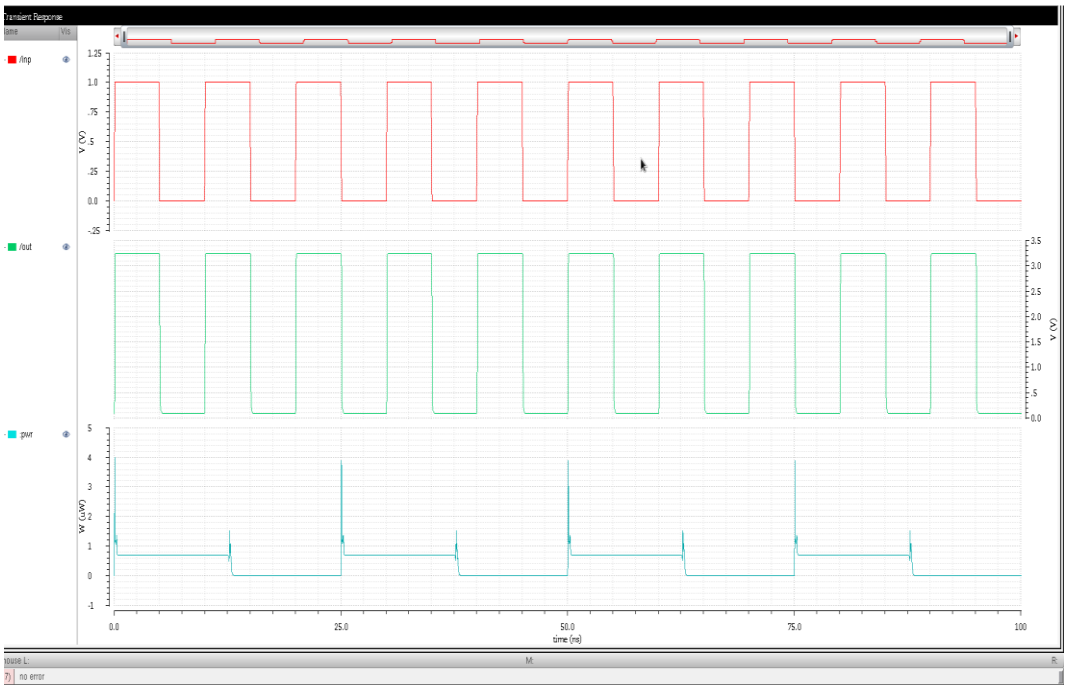


Fig 2.2.2 Simulations of Ultra Low Power High Speed Voltage Level Shifter

RESULT TABLE

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	87.53E-12	10.28E-12	48.405E-12	274.12E-6
2	1	28.19E-12	54.14E-12	41.165E-12	277.7E-6
3	1.5	10.65E-12	66.25E-12	38.45E-12	279E-6
4	2	4.17E-12	70.23E-12	37.12E-12	392.8E-6

Fig 2.2.3 Simulations of Ultra Low Power High Speed Voltage Level Shifter

3 A Novel Energy Efficient Voltage Level Shifter

Simulations and Results

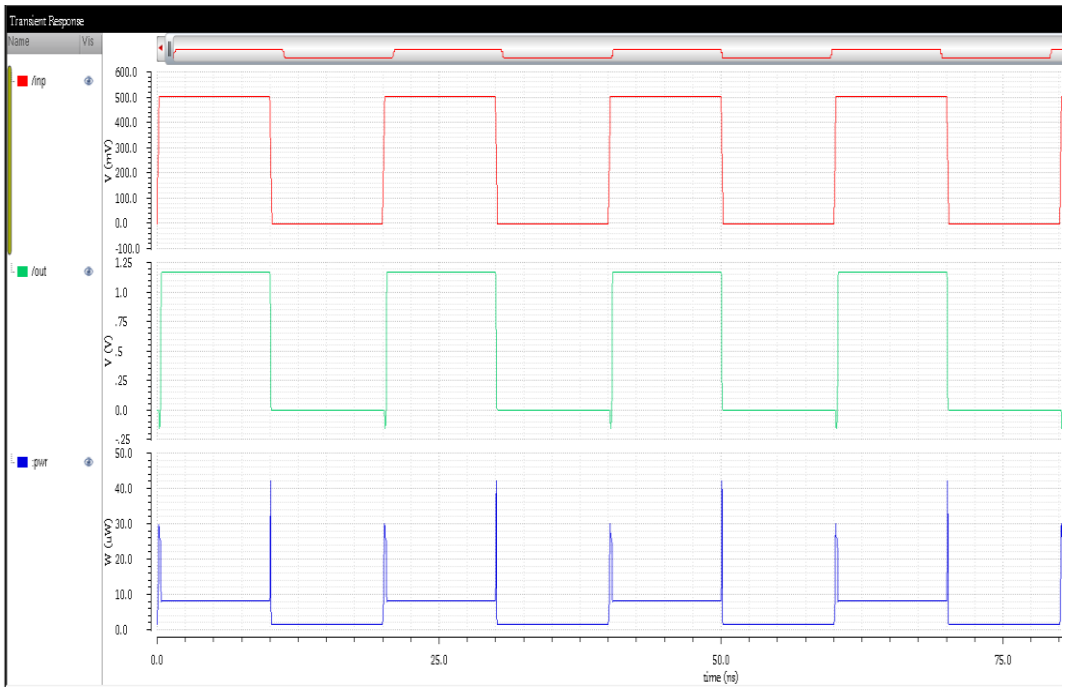


Fig 2.3.2 Simulations of Novel Energy Efficient Voltage Level Shifter

RESULT TABLE

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	5.067E-9	19.9E-9	12.2E-9	427.33E-9
2	1	4.027E-9	21.01E-9	12.13E-9	419.27E-9
3	1.5	1.085E-9	21.01E-9	11.23E-9	414.027E-9
4	2	855.9E-9	23.44E-9	12.41E-9	411E-6

Fig 2.3.3 Result Table Novel Energy Efficient Voltage Level Shifter

4 An Efficient Wide Range 2.45ns ,4.38Nw Subthreshold Voltage Level Shifter Using 45 nm CMOS Technology

Simulations and Results

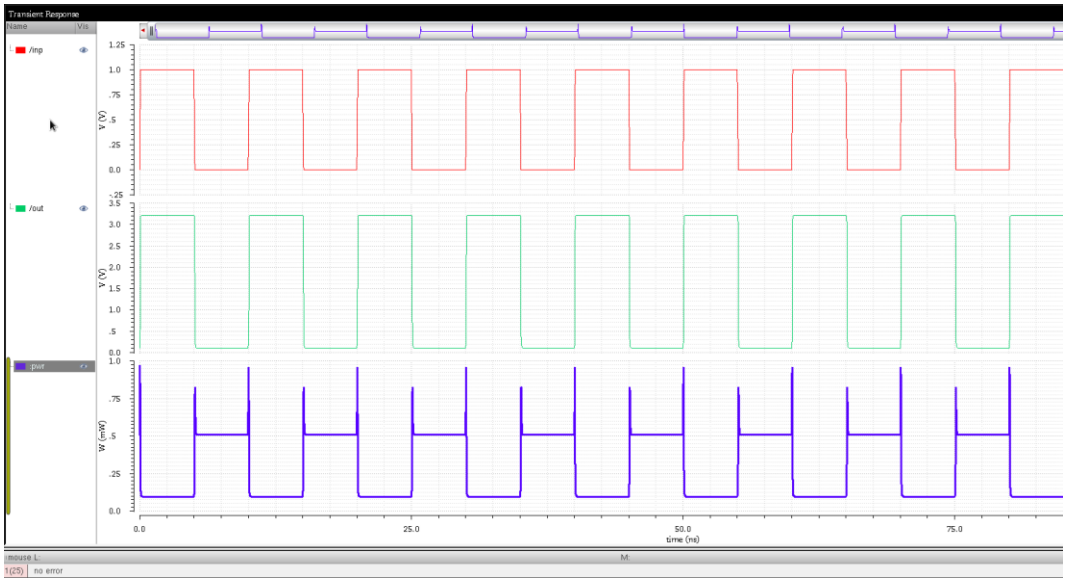


Fig 2.4.2 Simulations of an Energy Efficient Subthreshold Voltage Level Shifter

RESULT

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	88.45E-12	15.06E-9	7.574215E-9	276.77E-6
2	1	72.24E-12	15.1E-9	7.736E-9	299.4E-6
3	1.5	54.02E-12	15.11E-9	7.582E-9	307.3E-6
4	2	38.31E-12	15.04E-9	7.232E-9	361.9E-6

Fig 2.4.3 Results of an Energy Efficient Subthreshold Voltage Level Shifter

5 Design and Optimization of low power and high speed voltage level shifter circuit using 45nm and 180nm MOSFETs with Variable Voltage source

Simulations and Results

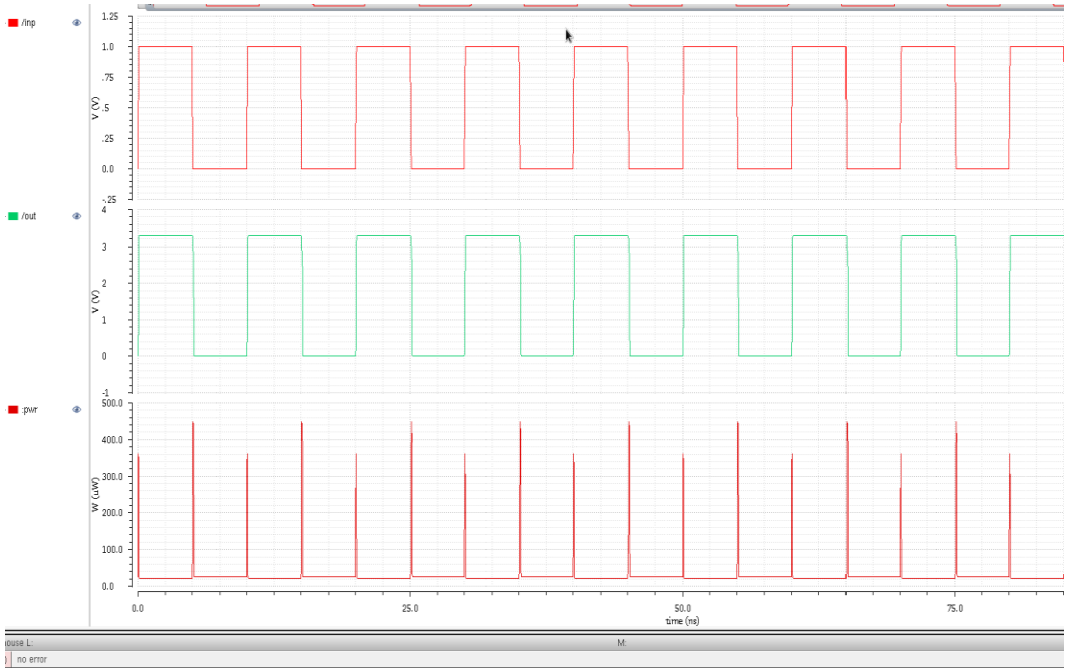


Fig 2.5.2 Design of Low Power High Speed Voltage Level Shifter using Variable Voltage Source

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	82.36E-12	92.04E-12	87.2E-12	28.978E-6
2	1	23.63E-12	124E-12	73.815E-12	30.98E-6
3	1.5	7.466E-12	139.9E-12	73.683E-12	31.266E-6
4	2	4.563E-12	147.89E-12	70.234E-12	47.17E-628

Fig 2.5.3 Design of Low Power High Speed Voltage Level Shifter using Variable Voltage Source

6 Dual Current Mirror Technique Based Energy Efficient 50mV to 1V Voltage level shifter

Simulations and Results

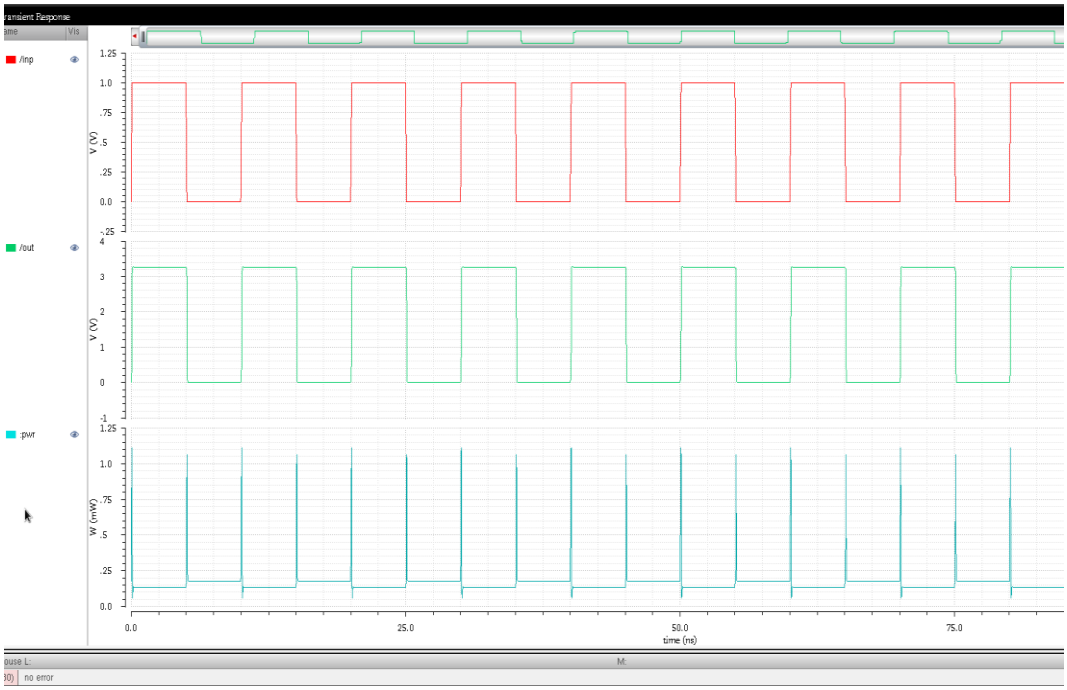


Fig 2.6.2 Design of Current Mirror Based Energy Efficient Voltage Level Shifter

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	160.4E-12	15.08E-9	7.6202E-9	167.6E-6
2	1	5.112E-9	15.11E-9	10.111E-9	167.4E-6
3	1.5	72.93E-12	15.12E-9	7.596E-9	167.7E-6
4	2	61.9E-12	15.13E-9	7.595E-9	250.4E-6

Fig 2.6.3 Design of Current Mirror Based Energy Efficient Voltage Level Shifter

7 A Low Power and High Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull up Network

Simulations and Results

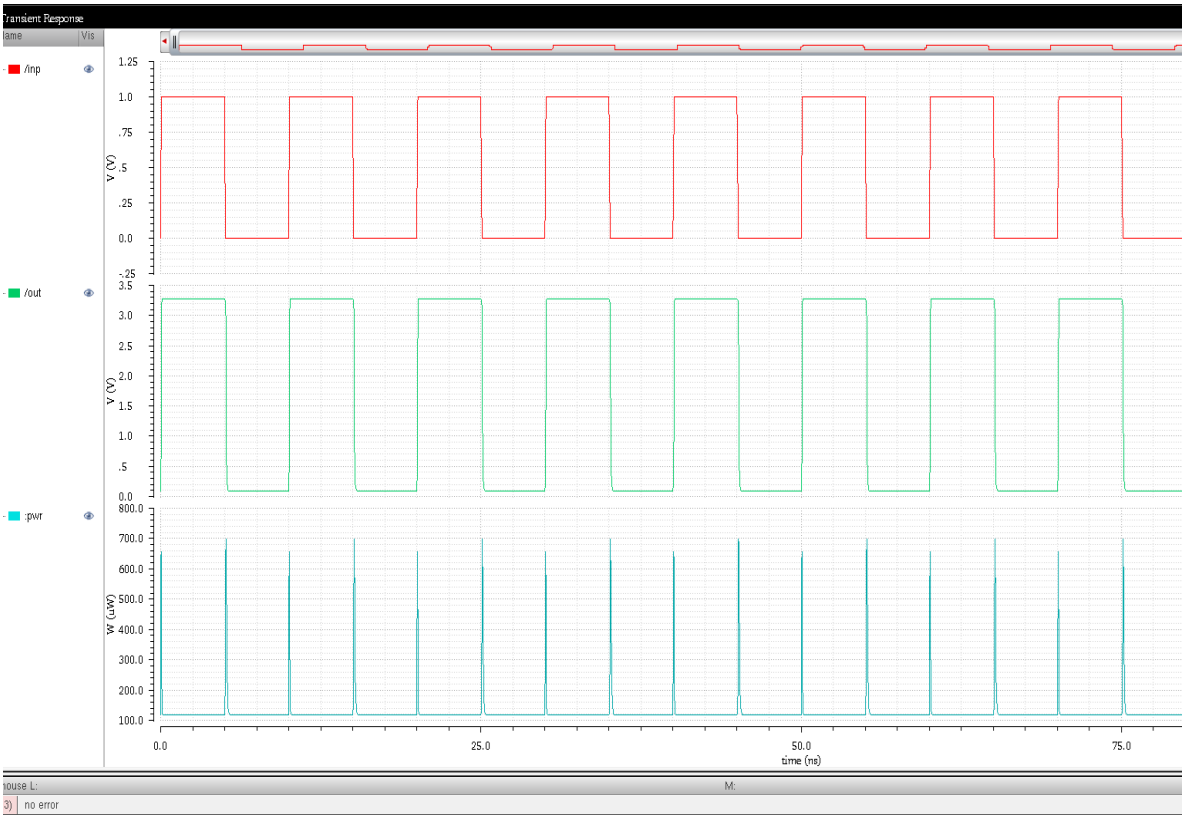


Fig 2.7.2 Design of Low Power and High Speed Voltage Level Shifter Based of Regulated Cross Coupled Pull up Network

RESULT TABLE

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	148.1E-12	15.1E-9	7.624E-9	125.1E-6
2	1	86.79E-12	15.19E-9	7.6383E-9	128.6E-6
3	1.5	67.42E-12	15.15E-9	7.605E-9	124.2E-6
4	2	56.47E-12	15.1E-9	7.578E-9	180.2E-6

Fig 2.7.3 Design of Low Power and High Speed Voltage Level Shifter Based of Regulated Cross Coupled Pull up Network

8 A Quick and Power Efficient Controlled Voltage Level Shifter Using Cross Coupled Network

Simulations and Results

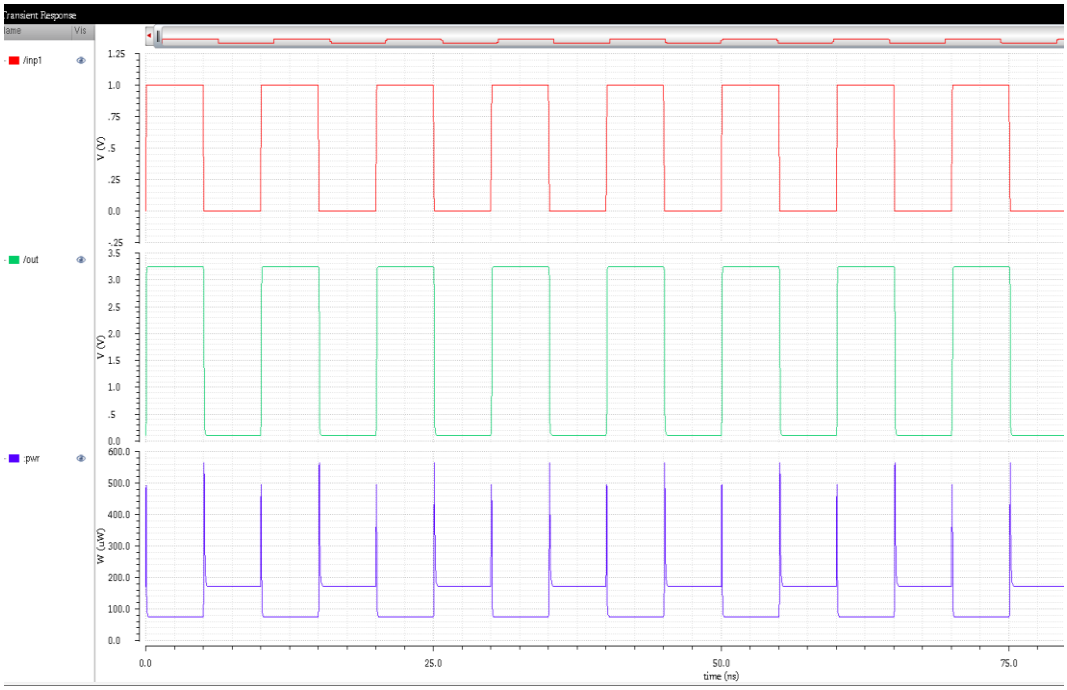


fig 2.8.2 Simulations of a Quick and power efficient controlled voltage level shifter using Cross Coupled Network

TABLE OF RESULT

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	189.7E-12	41.6E-12	115.68E-12	172E-6
2	1	122.44E-12	15.11E-9	7.566E-9	126.7E-6
3	1.5	72.94E-12	17.12E-9	8.596E-9	128.7E-6
4	2	60.18E-12	15.13E-9	7.595E-9	319.2E-6

fig 2.8.3 Result Table of a Quick and power efficient controlled voltage level shifter using Cross Coupled Network

9 Design and Analysis of High Speed Voltage Level Shifter Based on Wilson Current Mirror

Simulations and Results

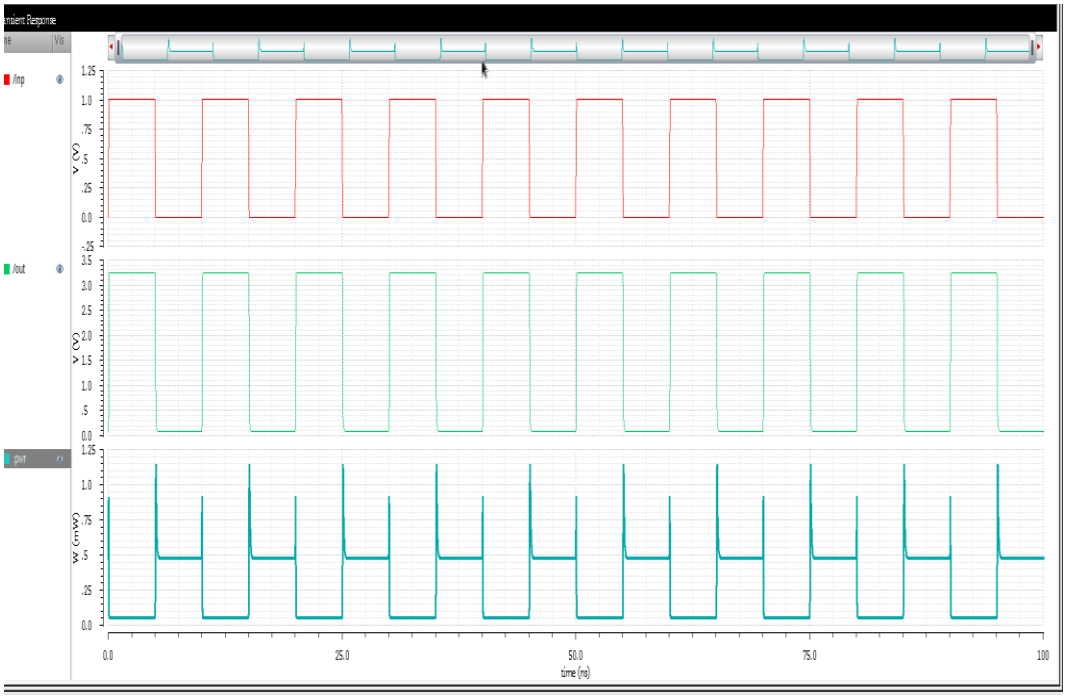


Fig 2.9.2 Simulations of High Speed Voltage Level Shifter based on current mirror

TABLE OF RESULT

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	86.53E-12	10.28E-12	48.405E-12	274.032E-6
2	1	28.19E-12	54.14E-12	41.164E-12	276E-6
3	1.5	10.65E-12	66.25E-12	38.45E-12	277.7E-6
4	2	6.67E-12	72.23E-12	35.78E-12	392.77E-6

Fig 2.9.3 Results of High Speed Voltage Level Shifter based on current mirror

10 Rapid Low Power Voltage Level Shifter Utilizing Regulated Cross Coupled Pull Up Network

Simulations and Results

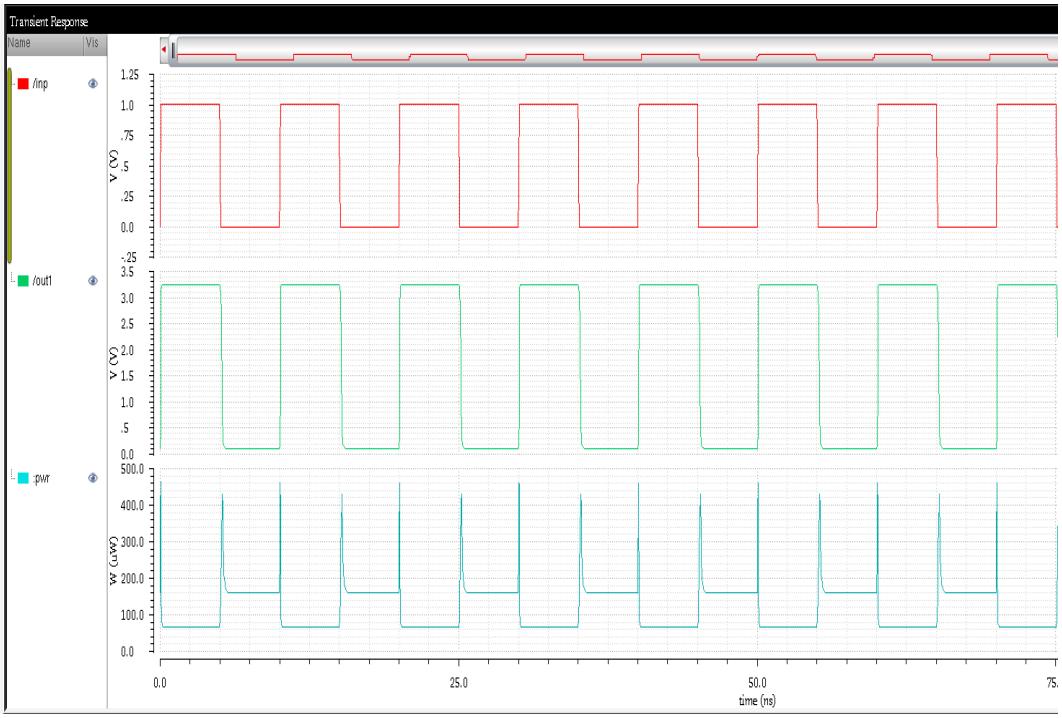


Fig 2.10.1 Simulations of Rapid Speed Low Power Voltage Level Shifter utilizing regulated cross coupled pull up network

RESULT OF TABLE

S.NO.	VOLTAGE	RISE TIME	FALL TIME	PROPOGATION DELAY	POWER DISSIPATION
1	0.5	172.5E-12	5.185E-9	2.678E-9	118.2E-6
2	1	95.13E-12	5.203E-9	2.649E-9	120.4E-6
3	1.5	73.52E-12	15.22E-9	7.646E-9	128.8E-6
4	2	61.67E-12	15.22E-9	7.640E-9	134.77E-6

Fig 2.10.1 Table of Results of Rapid Speed Low Power Voltage Level Shifter utilizing regulated cross coupled pull up network

CHAPTER 4

CONCLUSION & FUTURE SCOPE

3.1 CONCLUSION

Among all ten architectures, the "Design of low power high speed voltage level shifter with variable voltage source" proves to be the most superior. At the nominal operating point of 1 V input and 3.3 V output, it achieves a power dissipation of only 30.98 μW, a propagation delay of 73.8 ps.

This is significantly better than the Wilson-current-mirror based designs, which offer slightly lower delay (approximately 41 ps) but consume nine times more power (around 277 μW), resulting in a much larger PDP. Cross-coupled pull-up network designs provide moderate power and delay with good stability, making them suitable for general-purpose applications where extreme speed is not essential. Overall, the variable-voltage level shifter is the most energy-efficient and high-speed solution among all the compared models, making it the recommended choice for modern low-power, high-speed systems

3.2 FUTURE SCOPE

The comparative analysis of several designs of voltage level shifters indicates that remarkable progress has been made in reducing propagation delay, power consumption, and converting sub-threshold voltages. Nonetheless, the rapid evolution of VLSI technology and the increasing need to design energy-efficient electronic circuits call for more research into the design of voltage level shifters.

One of the future directions of research is related to the development of voltage level shifters that will be able to work with ultra-low supply voltages less than 50mV. With the emerging trends in IoT technologies and the development of devices that will work without batteries

by collecting energy from the environment, it will be crucial to develop voltage level shifters that operate on weak input voltages.

Another potential research direction is the incorporation of the latest CMOS technologies including FinFET, GAAFET, and FD-SOI devices in the design of voltage level shifter circuits. With their reduced leakage currents, enhanced electrostatic control, and switching characteristics, the latest CMOS technologies are capable of offering speed and power efficiency advantages over the conventional CMOS technology.

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