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Abstract

The design of compact high voltage pulser circuits capable of operating at high frequencies of MHz range remains as a big challenge in modern electronic and biomedical engineering fields. Existing pulser circuit design operate at single digit MHz pulse frequency ranges with low repetition rates. Conventional switching and transformer based designs suffer from various switching losses, distorted waveforms and reduced efficiency at high frequencies. This thesis is focused to address this gap of research by presenting the design and simulation results of a voltage pulser circuit design that is capable of generating 300V pulses with pulse frequencies ranging from 39kHz to 20MHz with a variable repetition frequency. The design includes a frequency divider circuit, a pulse transformer for transmitting the voltage pulse and analog-digital converters and a microcontroller for further processing the received signal.

The proposed design makes use of flip flop based frequency divider circuit to get pulses at various frequencies and a frequency selector topology implemented using AND logic. A pulse transformer topology is used to amplify the selected pulse voltage upto 300V. Simulation results show a voltage pulses that has peak voltage above 300V for the required pulse width duration and voltage droop of 20V to 40V. It is also observed that all the pulse have a 50% duty cycle with rise times of less than 8% of pulse width and fall times of less than 8% of pulse width. Simulation results show an output current in milliamperes with a power from a 5V DC source. The proposed design serves as a foundation for further study of high voltage high frequency voltage pulser circuit that have uses in dental devices as well as in applications that necessitate such a pulser circuit.

CHAPTER 1

INTRODUCTION

1.1 Background

In this chapter we have discussed Voltage Pulser circuit architectures have progressed in recent years, these advancements had been driven to satisfy the need for a efficient and high voltage pulser circuit system. In high voltage systems, particularly compact systems that work with microcontrollers the pulse frequency plays a pivotal role in deciding the entire circuit design. The higher the pulse frequency is, the complex it becomes to design a voltage pulser circuit that preserves the waveform as well to increase the amplitude of the pulse.

Among the commercially available voltage pulser circuit systems, they either make use of a high DC source to achieve output pulses at kilo-volts range with less current from source or output peak to peak voltage of not more than 200V when using a moderate voltage DC source. This makes them not compact nor efficient to work with a 5V DC source. Moreover those designs have output currents high than the limit an human body can safely take.

This thesis focuses on the design and analysis of a voltage pulser circuit using simple topologies to keep it compact and simple. The simulation is conducted using PROTEUS 9 PROFESSIONAL EDA tool. Keep parameters such as pulse width, rise time, fall time, output current are analyzed to evaluate the implemented design.

1.2 Motivation

With increased need for non invasive medical devices growing day by day and increased need for those devices to be as small as possible, there exists a need for designs that is not complex nor inefficient. Recent research works done in this field has indicated trends toward a compact system design with higher pulse frequencies but does not tick all the boxes this works intends to achieve.

The motivation behind this work stems from the need for such a system that makes use of simpler design that produces high voltage high frequency pulse efficiently while achieving operating parameters that is safe for non invasive medical uses.

1.3 Problem Statement

While existing designs and devices achieve the needed voltage and max out at frequency requirements, they are all invasive in nature. Three key challenges are observed in voltage pulser design:

1. Pulse Width: Maintaining the pulse width at high frequencies without waveform distortion.
2. Rise/Fall Time: At frequencies in tens of MHz range the rise time and fall time cannot be more than 5ns to preserve pulse shape
3. Output Current: To be non invasive in nature the output current cannot be more than 10mA

This thesis addresses these challenges by designing an efficient high voltage high frequency voltage pulser circuit that is compact as well as non invasive in nature while making use of simpler circuit topology and analyzing its pulse width, rise/fall times and output current through simulation.

1.4 Objectives

To ensure a structured approach the following objectives are defined in thesis:

- Design and implement a simple frequency divider and selector circuit.
- Design a simple pulse transformer that will amplify the pulse amplitude upto 300V
- For the receiver side, make use of analog-to-digital converters and a microcontroller that are readily available.
- Simulate pulse generation to verify the functionality and measure the output voltage.
- Analyze the output waveform and measure pulse width, rise/fall times, and output current.

1.5 Novelty of proposed circuit design

The major contributions of this paper are summarized below:

- A simple and inexpensive architecture for high voltage pulse generation that solves the difficulties of conventional resonant converters, Marx generator, Blumlein networks and others in generating high voltage pulses in multiple stage manner is proposed.

- D-flip-flop based frequency divider is implemented for generating various operating frequencies from the reference clock of 20 MHz with the minimum usage of the hardware and desired accuracy of frequency division.
- Frequency selecting and isolation circuit is implemented based on logic gates that gives the freedom of selecting the frequency and repetition rate of the pulses as needed with the digital architecture.
- A pulse transformer has been employed as the element for increasing the voltage in single stage that provides the galvanic isolation along with amplification of approximately 60 times voltage without resonant power converter or cascaded high voltage stage.
- A large frequency range from 39.0625 kHz to 20 MHz is achieved making the circuit capable of performing under various operating frequencies and adjustable repetition rate.
- Control structure based on microcontroller has been designed which permits selection of frequency, repetition rate in programmable manner and could be further integrated with data acquisition system and signal processing modules.
- A reduction in the number of components, size, cost and complexity have been achieved from the proposed architecture.

1.6 Literature Review

The non invasive application of for variety of uses cases in medical field has gained preference over other methods, due to the advantages it provides. The method of using high voltage low current pulses in such cases where the data has to be recorded and processed without causing any perturbation to the human body is one such technique. While the design and systems for pulse generators were around for a considerable time, the advancements made over the years are noteworthy. The field of high voltage pulse generation has undergone phenomenal evolution over the past two decades owing to developments in semiconductor technology, desire for miniaturization of the systems and need for power efficient operation at high frequencies in a vast number of applications. While early designs were dependent on bulk transformers, spark-gap switches, gas-discharge tubes etc., the modern designs are moving towards fully solid-state configurations capable of producing rapid high-voltage pulses from low-voltage supply. This development is possible due to advancements in MOSFET technology (especially WBG like GaN, SiC), modular circuit topologies, resonant techniques, capacitive pulse forming and integrated level shifting. A very fundamental idea the evolvement of the pulse generators has followed is moving away from the high-voltage, monolithic devices to low-voltage, modular building blocks that can be cascaded, stacked or resonated to obtain high voltages. Similar approach has been shown by the authors [2], where the classical Marx generator is redefined. Instead of using energy-dissipating, non-scalable resistive isolation networks used traditionally in Marx generators, this design uses inductive isolation between the stages. While the Marx-type generators may

generate pulses of scale microseconds at moderate repetition rate, but newer applications such as high-speed imaging, excitation of EMAT, nano-scale systems, require sub-nanosecond or nanosecond pulses with mega hertz repetition rate. This becomes problematic at such frequencies due to existence of parasitic capacitances, switching delays and recharge constraints in the standard Marx generators. The authors in [3] proposes an architecture by using a combination of LC resonance boosting with Blumlein pulse forming techniques to combat the problem. Another such direction, where the sub 10ns pulses have been successfully generated, is the capacitive chopping technique used by the authors [4]. Contrary to the resonant or Marx based topologies, where the energy is stored in some element and discharged in a precisely timed manner, CCC technique essentially translates an energy stored in capacitors into well-defined time-varying voltage differentials.

While focusing on nanosecond range pulse, there has also been efforts towards the design of megahertz repetition rate high voltage pulsers, for industrial applications like electro-optic modulators and high speed lasers. The work [5] demonstrates an example of using modern pulse generator topology exploiting wide-bandgap devices, which is a key to the design for stringent specification. The authors, in their paper, designed and built a stacked configuration of Silicon Carbide MOSFETs, biased at relatively low voltage to produce pulsers with voltage up to 5 kV, operating at megahertz repetition rate. The author proposed a separated heatsink topology, where the thermal and electrical path is isolated from each other, which reduces the stray capacitance between MOSFETs. Biomedical imaging applications require pulsers which can be easily miniaturized without compromising waveform quality, efficiency and transducer driving strength. The authors [6] designed a system for a miniaturized high voltage pulser that solves the challenge of having small local bypass capacitance for supply rail stability. Their solution is a balance capacitive high voltage level shifting circuit that operates under highly unstable supply rail conditions. Another direction was presented by [7] where they demonstrated an architecture for ultrasound imaging that provides improved acoustic excitation, in order to avoid the biasing issue in the mechanical structure of ultrasound transducer, that is found in unipolar pulses. Bipolar pulse excitation is preferred because it is linear to mechanical excitation for both piezoceramic and CMUT type ultrasound transducers. Their 3-level pulser generates RZ multilevel waveform which include positive and negative polarity plus zero level to control movement of the transducer membrane, minimize the non-linear echo artifacts. Electroporation protocol require pulsed with very high voltage (hundreds-thousands volts), but very short pulse width, which are necessary to temporarily open pore of cell membrane. Piezoelectric transformers (PTs) can amplify low voltage to high voltage very compactly, and are of high interest for electroporation applications. The authors of [8] explored an architecture that combines PTs with wide-bandgap semiconductor to build a compact, efficient, magnetic-free high voltage pulse generator. Outside of the medical scope, high current pulse systems provide some hints regarding energy recycling, staging of energy transfer and the practices in magnetic switching which are relevant for high voltage pulsers. The proposed system [9] use multistage pulse transformers coupled with XRAM inductive current multiplication, to achieve very high current pulse, though the design focuses on current rather than frequency, principles of staging the energy trans-

fer, controlling leakage inductance and recovering the energy stored in the inductance is still useful at low voltage, high frequency pulsed as a way to enhance efficiency by using energy recovery. Magnetic isolation for solid state MARX generators was reported by the authors [10]. A challenging part for high voltage stack topology is synchronization of all floating switches. Using magnetic isolation this problem was overcome, the designer used stacked magnetic core and windings to synchronize all the switching stages.

Another study by the authors of [11] outlines a novel high voltage pulsed generator intended to improve on existing diode opening switch (DOS) generators in the context of nanosecond pulsed electric field applications for tumor ablation via electroporation. Specifically, the semi-controlled nature of diodes limits their pulse width and imposes an upper repetition rate based on the resonant period; the novel modulator described is built from multistage linear resonant loops allowing adjustment of the pulse width within diode based LR discharging circuits. Another work by the authors of [12] attempts to address the problem of requiring a high-amplitude and high-frequency power supply for electromagnetic acoustic transducer non-contact metal thickness measurement in an industrial environment. They develop a LCC filter designed for a non-resistive inductive load by optimizing the Q-factor, incorporate techniques for minimizing transient startups and endings by precharging and damping, and develop a specialized receiving circuit with depletion MOSFETs to achieve both high-voltage transmission and microvolt echo reception. Authors in [13] also developed an novel high voltage multiply pulser in a BCD CMOS process which allows for a high power efficiency for a capacitive load like piezoelectric micromachined ultrasound transducers. Their design makes use of a modular architecture wherein supply adder modules are connected in series, and supply addition is done on one phase, and the supply is delivered on the other, allowing charge to be shared on a capacitive load, thus greatly reducing power loss.

Focusing on the field of biomedical imaging, [14] describes another effort toward the development of low-power ultra high-frequency pulsers. For example, driving ultrasound transducers at extremely high frequencies of 15 MHz involves very fast charge and discharge of the transducer's capacitance, and thus CVf switching losses can become very high; their approach recycles the residual energy on the transducer after each pulse in a two-stage manner. The development of pulse transformers is a continuing and developing field, aimed at reducing physical size, power loss, and improving pulse fidelity, voltage capability, and operating frequency. Earlier developments focused on applications such as radar and microwave imaging where there was a need for low-rise time rectangular pulses with minimal pulse droop and waveform distortion. This type of pulse transformer design, as well as the trade-offs between parameters such as magnetizing inductance, leakage inductance, stray capacitance, and the source and load impedances is explored by the authors in [1]. They also discuss the importance of using a magnetic core material with a high pulse permeability and low eddy current losses. The drive for smaller and lighter pulsed power systems has been fueling research into higher-frequency and higher-power-density transformers. The authors of [15] explore some techniques to meet these demands, by designing a pulse transformer with a ferrite EE core and a sectioned secondary winding made of Litz wire in an attempt to reduce

leakage inductance and stray capacitance.

An alternative research topic that is well-investigated is that on novel magnetic materials and modular transformer design for high voltage pulsed power applications (as discussed in [16]). In this work, a multi-core pulse transformer incorporating nanocrystalline toroidal cores design was proposed. A new magnetic materials design has yielded better performances of higher permeability, lower core loss and high temperature stability than traditional ferrite cores used, providing improved applicability for high frequency design. It has successfully minimized the number of cores and windings to decrease losses on secondary winding and improve performance reliability during high voltage operations. Following this, integration of pulse transformers into multistage pulsed power systems to attain a higher voltage gain and minimize stresses on the semiconductor switches has been further studied. The architecture presented was a two-stage pulse generator, consisted of a full-bridge DC-DC converter followed by a pulse transformer based pulse generator, as demonstrated in [17].

As high voltage pulsed systems designs become more complex, and required in the applications of biomedical imaging or industrial sensing where precision is a significant factor, the interactions of characteristics between the semiconductor switch device, the circuit topology, and the circuit parasitic parameters are also of crucial importance. While early HV pulser designs did not take much concern about the magnetic component's non-linearities and parasitics, the development of the required ever-narrower pulses in nano-second domain, together with higher repetition frequencies in mega Hertz regime, makes a knowledge about limitation in switching devices, package inductance, layout capacitance and transmission line characteristic increasingly necessary. It is very evident that these factors are inseparable with required good drive circuits and topologies that enable high voltage, high repetition frequency and high volumetric density simultaneously, from the literature review conducted.

The novelty of the proposed work is a compact high-voltage, high-frequency pulser architecture capable of producing output voltage pulses greater than 300 V with an input of a 5 V DC supply over a wide frequency range of 39.0625 kHz to 20 MHz. This new architecture is distinctly different from a number of available pulse generation systems which are based on complicated resonant converters, Marx generator, multistage voltage multiplier, or external high-voltage power supplies. It utilizes a simple D-flip-flop-based frequency divider and logic-gate-based pulse selection approach to generate multiple operating frequencies from a single clock. It relies solely on pulse transformers as the primary voltage amplification components thereby avoiding bulky high-voltage conversion stages, which in turn result in a compact, less complicated circuit with minimal components and at reduced costs. It provides programmable frequency selection and controllable repetition rate through digital logic, which is suitable for various biomedical and dental applications. Simulation results prove its ability to retain pulse shape, with minimal voltage droop, rapid rise and fall times and output currents in the mA range, appropriate for non-invasive applications. Also, a receiver architecture which incorporates commercial amplifiers, ADCs, and microcontroller interfaces are introduced to further complement a full sensing/signal-processing system. The wide frequency operation range, use of a low-voltage supply, compact implementation, and generation of a high voltage pulse make the proposed work stand out among

many published designs.

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CHAPTER 2

METHODOLOGY

2.1 Overview

2.1.1 Frequency Division

While there are many ways to perform frequency division or even frequency multiplication, selected a simple method to not make the circuit complex while also preserving the overall rise time and fall time. Frequency division using D-flip flops is the easiest method to achieve this. A D-flip flop configured in toggle mode performs an accurate divide by 2 operation by feeding the inverted output back to the input. There by generating a stable output frequency that is exactly half of the input clock frequency. Compared to other flipflops such as JK and SR flipflops D flip flops offers a simpler

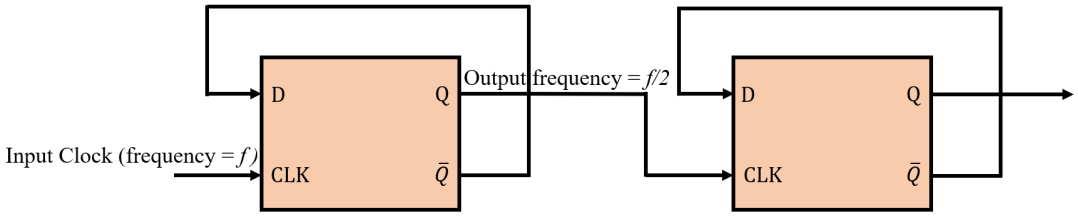

Figure 2.1: D-flipflop based frequency division operation

implementation, fewer connections and reduced chances of invalid states or switching errors. Compared to T flipflops, D flipflops are easily available in wider area and easily configurable. These make the circuit more reliable at high operating frequencies while maintaining signal integrity and timing accuracy. Also, D flipflops generally exhibit low propagation delay which help in preserving the rise time and fall time requirements for high frequency pulse generation applications.

2.1.2 Frequency Selection Logic

An AND logic gate used for frequency selection and pulse control due to its simple implementation, fast switching capability and reliable operation at high frequencies. AND gate allows the required frequency signal to pass only when the control signal is enabled, so thereby it provides an efficient method for pulse gating without causing any

significant delay or distortion to the waveform. Although high speed switching devices such as GaN FETs can also be used for signal selection, but they require additional gate driving circuits and more complex biasing arrangements. These increase the overall circuit complexity and cost. Furthermore, the use of GaN FETs for simple frequency selection is unnecessary because logic gates perfrom the same operation with lower power consumption and simpler integration.

2.1.3 Pulse transformer

A Pulse Transformer is used to generate high voltage pulse through electrical amplification. It also serves the purpose of achieving isolation between the low voltage control circuitry and the high voltage output circuitry. Unlike power transformers that are primarily dealing with the transfer of sinusoidal waveforms, pulse transformers are specifically designed for efficient and high speed transfer of pulses with short duration and with a minimal loss in pulse shape. It operates based on the principle of electromagnetic induction whereby rapidly varying current in the primary winding induces a pulse of high voltage proportional to the ratio of teh number of turns in the secondary and primary winding, in the secondary winding. The voltage can thus be stepped up to the required value without the requirement of multi stage converter circuits thus simplifying the complexity and space requirements. This technique helps retain the faster rise and fall times required for high frequency pulse generation applications. Of the avail-

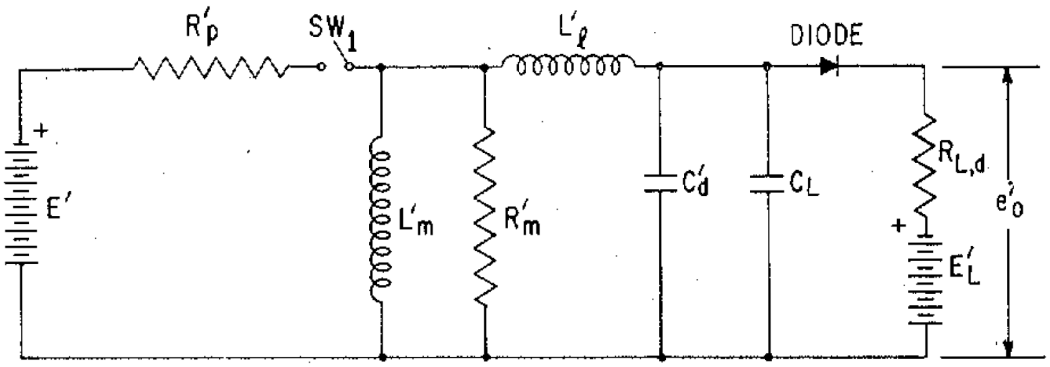

Figure 2.2: Equivalent Pulse Transformer [1]

able methods of generating high voltages like cascaded boost converters, Cockcroft-Walton multiplier circuits, resonant RF amplification stages, the pulse transformer was chosen for its simplicity and increased circuit efficiency. Other high voltage amplification techniques was studied and posed limitations such as increased circuit complexity in design, switching losses, requirement of complex filtering circuitry. In addition, the duty cycle control for high frequency boost converter stages can be a problem due to the need of additional complex compensation network designs. Thus, the pulse transformer offers a simpler solution. It also improves isolation between circuitry and lowers the count of circuit components.

2.2 Proposed Method

After analyzing and studying various methods for pulse generation and control circuit designs, implemented a simple method to do frequency division, pulse selection and pulse amplification.

The pulse generation system takes a 20 MHz, 5V input pulse signal and produces output pulses with up to 300 V. The output of the 20 MHz input signal is divided by a D-flip-flop based frequency divider to produce a variety of different output frequencies including 1.25MHz, 625 kHz, 312.5 kHz and 39 kHz. The output of each frequency divider is fed to the AND-logic-based pulse isolation stage, to enable the output at the selected operating frequency, and input by frequency and repetition rate signals from the STM32F429ZI controller, into each corresponding frequency's amplification channel. Each amplifier channel has pulse transformers incorporated, to increase the amplitude of the pulses, while also giving each channel electrical isolation. These separate, tuned, pulse amplifiers drive the high voltage pulses into the output transmitter section for transmission. This entire system can be driven by a single 5V DC supply.

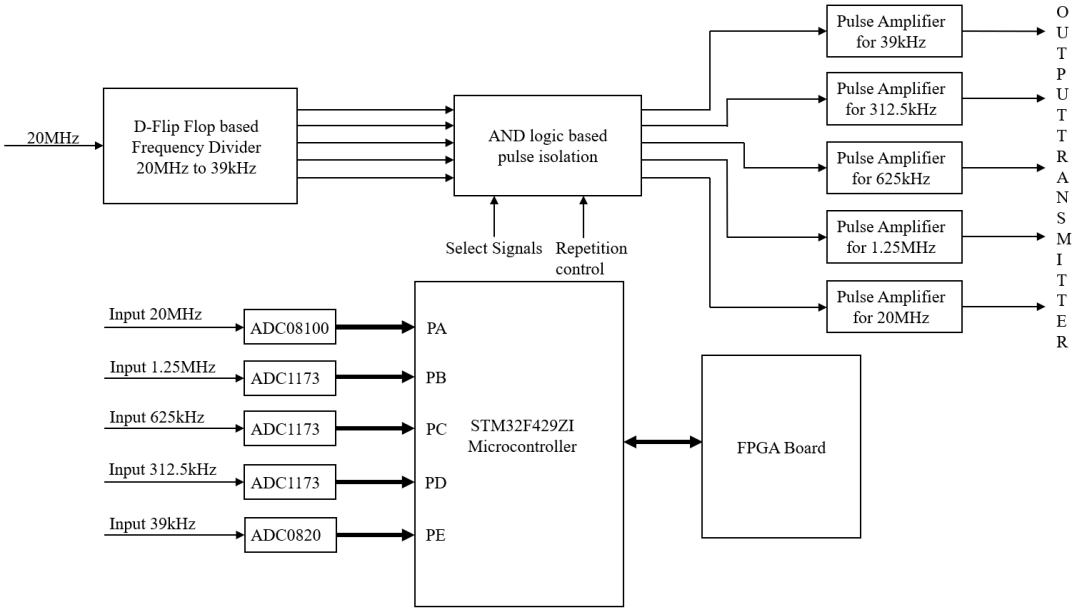

Figure 2.3: Implemented Block Diagram

2.2.1 Frequency Divider

Implemented D-flip flop based frequency division mechanism using flip flop IC 74HCT74 As shown in the figure 2.4 the initial input is 20MHz pulse that can be generated either from the microcontroller or from the FPGA board or using any type of oscillator circuit. For a cascaded *n* D-flip flops, the general equation for frequency of clock signal is,

$$f_{out} = \frac{f_{in}}{2^n} \tag{2.1}$$

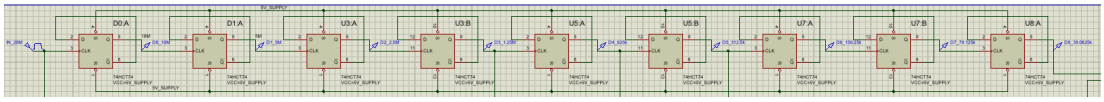

Figure 2.4: Implemented D-flip flop based frequency divider

All the flip flops are powered by a 5V DC supply source. With input at 20MHz, nine D-flipflops are used to get frequencies of 10MHz, 5MHz, 2.5MHz, 1.25MHz, 625kHz, 312.5kHz, 156.25kHz, 78.125kHz and 39.0625kHz. Off these frequencies the desired frequencies are 20MHZ, 1.25MHz, 625kHz, 312.5kHz and 39.0625kHz.

2.2.2 Pulse Isolation

The obtained frequencies are controlled through AND logic gates for desired frequency selection and pulse isolation and repetion control. As shown in the figure 2.5 the obtain

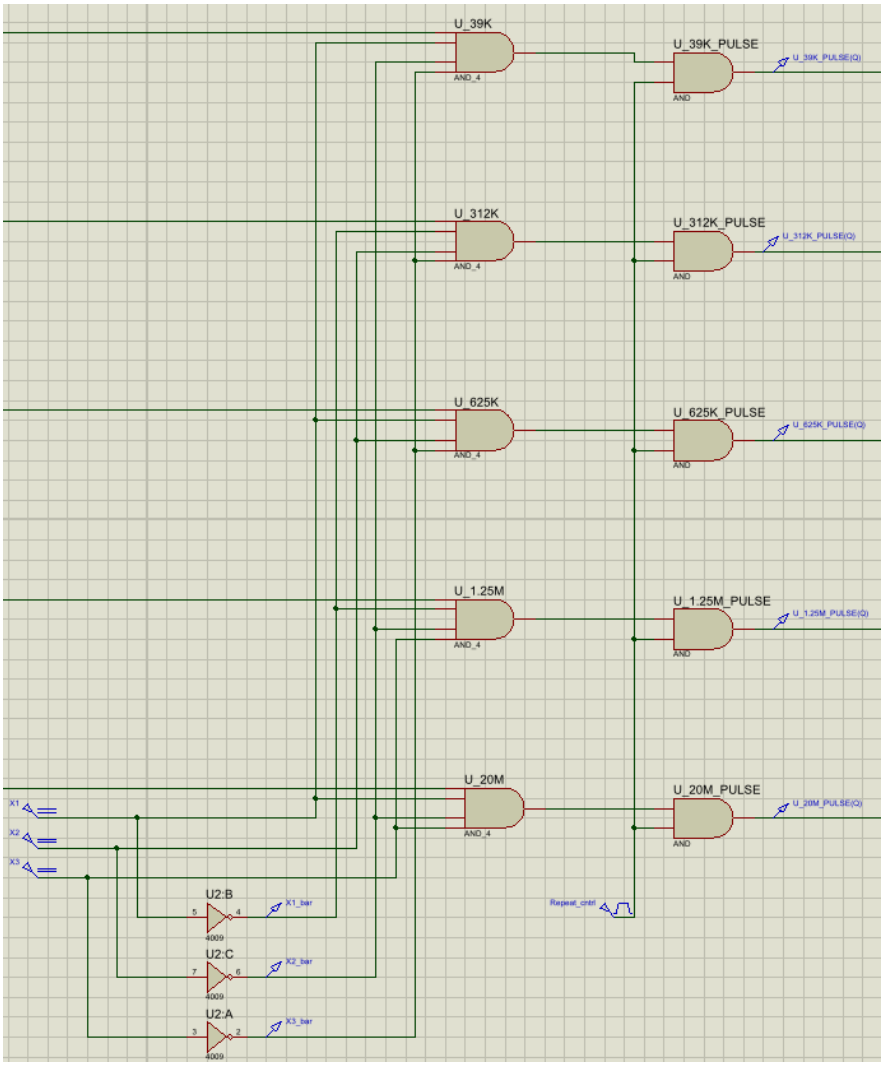

Figure 2.5: Implemented frequency selection mechanism

frequencies are selected using select signals that will be generated from the microcon-

troller. Based on the select signal value the desired frequency is passed through and sent for the pulse isolation. Here another AND logic is used where one input is the desired frequency while the other input would be the repetition control signal from the microcontroller.

The pulse is isolated by controlling the duty cycle of the repetition control signal. The pulse is repetition frequency is controlled by the frequency of the repetition control signal.

2.2.3 Pulse Amplification

The isolated pulse is then received at the input of pulse transformer block. Since PROTEUS EDA software does not have native pulse transformer, the symbol of a generic transformer is used while the spice model of pulse transformer is inserted in place of the transformer spice model.

As shown in the figure 2.6 a two winding pulse transformer is implemented where the load is modeled as transducer block. The output of pulse isolation logic is connected to one terminal of the primary winding through a capacitor-inductor path while the other terminal of the primary winding is connected to the ground. The capacitor and inductor is used to keep the primary inductor energized while constant voltage is applied when the input pulse reaches its maximum voltage.

The magentizing inductance value of primary winding is obtained using the equation

$$L_{mag} = \frac{\mu_o \cdot \mu_{max} \cdot {N_p}^2 \cdot A_e}{l_e} \tag{2.2}$$

where L_{mag} is the magnetizing inductance of the primary winding, while

- μ_{max} is the maximum permeability of core material
- N_p is the number of turns of the primary winding
- A_e is the effective cross-sectional area of coil
- l_e is the effective length of the coil

respectively.

The pulse transformer are modeled to have Nickel-Zinc ferrite core and Manganese-Zinc ferrite core due to their high frequency operating properties. Each pulse transformer's secondary winding is modeled to have an impedance of 50Ω. The coupling coefficient of each transformer is set to mirror the real world value of high frequency pulse transformers. The load is modeled as a transducer with capacitance of 10pF, and resistance of 1M Ohm.

2.2.4 Receiver Circuitry

The receiver circuitry that can be used to process the received response to the pulse signal transmitted is also proposed. The circuitry consists of five amplifiers and five analog to digital converters that are readily available, each for a single frequency and

has sampling rates at five times the pulse frequency there by being higher than the standard Nyquist rate. As shown in the figure 2.7, each of the amplifiers and ADCs are carefully chosen to have sampling rate atleast five times of the input signal frequency. These converters outputs digital data in 8-bits and is connected to the microcontroller STM32F429ZI. Each of the channel banks of the microcontroller is dedicated to individual ADCs while one bank is used to interface with a FPGA board, in this case a Raspberry Pi 4 board.

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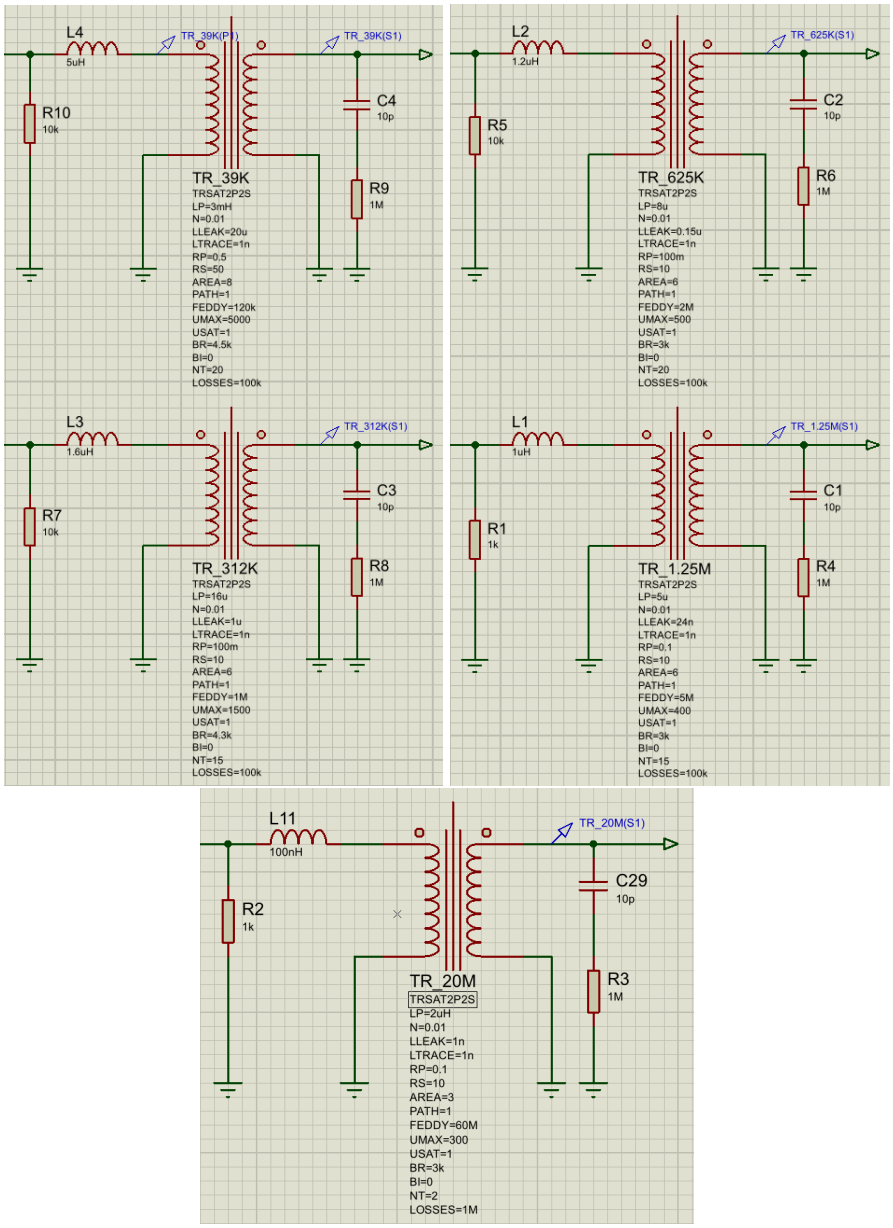

Figure 2.6: Implemented Pulse Transformers

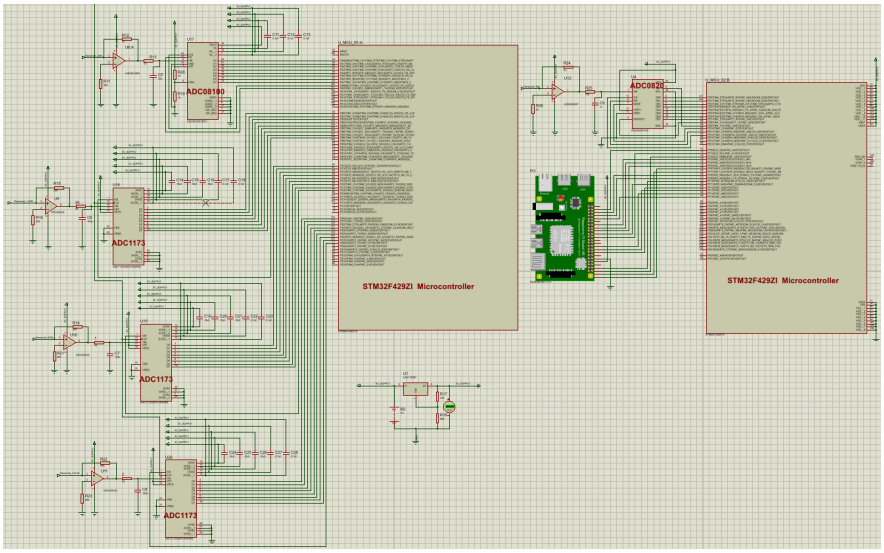

Figure 2.7: Receiver Circuitry

CHAPTER 3

RESULTS AND DISCUSSION

3.1 Simulation Setup

The circuit design is implemented using PROTEUS EDA software. All the blocks in the circuit are connected to a 5V DC supply while the converters and microcontroller is connected to a 3V supply achieved using LM317 voltage regulator block. The input 20MHz signal is modeled with 1ns rise time and fall time delay. The repetition control signal duty cycle is carefully choose to capture the pulse accurately, which is done by taking into account the propagation delay caused by the D-flip flops and the inverters in the select signals' path. So the control signals are modeled to work after a full cycle of the lowest frequency is completed to maintain uniformity across the pulse isolation logic for all the desired frequencies. The duty cycle of the repetition control is set to be at 80% of the time period of desired pulse frequency.

The pulse width, rise time, and fall time were calculated using Equations 3.1, 3.2 and 3.3.

$$T_{\text{pulsewidth}} = t_{50\%}^{\text{fall}} - t_{50\%}^{\text{rise}} \tag{3.1}$$

$$T_{\text{rise}} = t_{90\%} - t_{20\%} \tag{3.2}$$

$$T_{\text{fall}} = t_{20\%} - t_{90\%} \tag{3.3}$$

The inductor connected to the terminal of the primary winding is air-core inductor. The capacitor connected in series with the inductor is ceramic material capacitors, which are chosen because of their rapid charge discharge characteristics. The values of inductor and capacitor connected to the primary windings of the pulse transformer is chosen in such a way that when the input pulse reaches its maximum voltage, to keep the voltage droop at the output minimum and to prevent de-energizing the primary inductor coil, the values are chosen after experimental verification. While the receiver circuitry is also placed for processing the recieved signal after transmitting the pulse, it is not simulated due to the complexities arising with the need computing hardware and software instability caused by it.

3.2 Results

3.2.1 Frequency division

The input 20MHz pulse is given to the first D - flip flop. The observed frequency at the output of that first flipflop is 10MHz. Similarly the frequency observed at the output of third flipflop is 5MHz. This is observed from the figure 3.1.

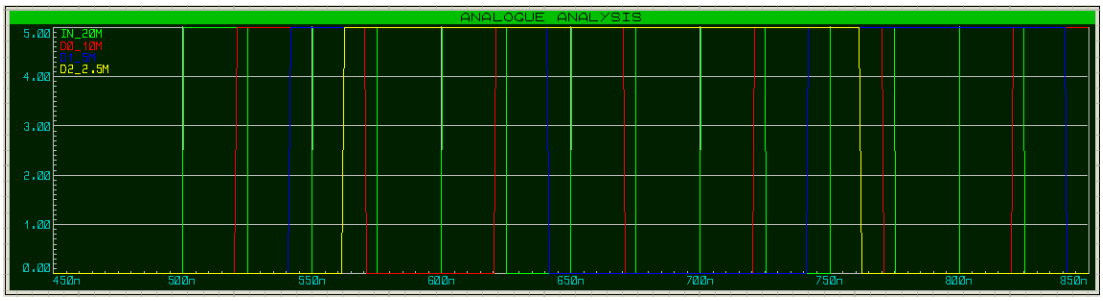

Figure 3.1: Output of first three D-flipflops: a)20MHz(Green) b)10MHz(Red) c)5MHz(Violet) d)2.5MHz(Yellow)

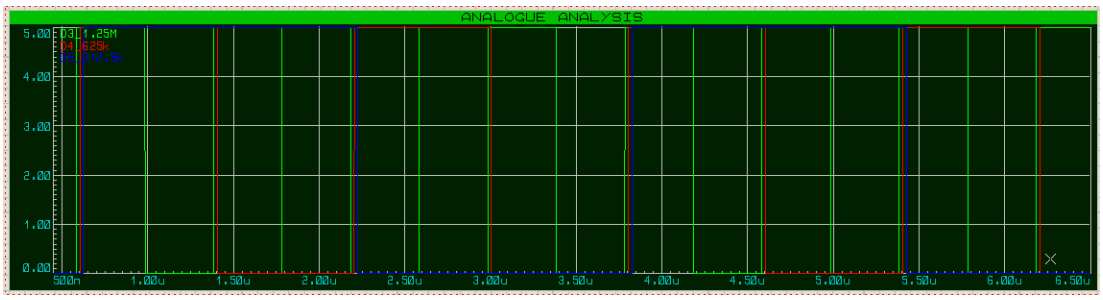

Figure 3.2: Output of middle three D-flipflops: a)1.25MHz(Green) b)625kHz(Red) c)312.5kHz(Violet)

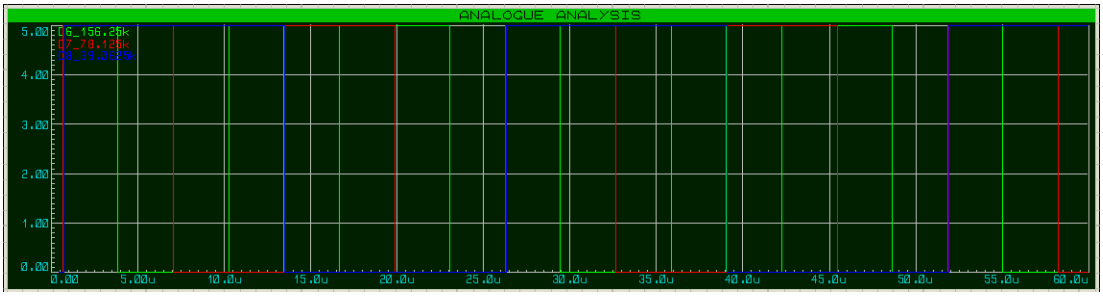

Figure 3.3: Output of last three D-flipflops: a)156.25kHz(Green) b)78.125kHz(Red) c)39.0625kHz(Violet)

From the figures 3.1, 3.2 and 3.3 it is observed that all required frequency signals are obtained without any significant change in rise time and fall time when compared with the input signal using the equations 3.2 and 3.3

3.2.2 20MHz Pulse

The input 20MHz signal is directly fed to the frequency selector logic whose output is fed to the pulse isolator logic using the select signals and repetition control signal. The isolated pulse is then fed to the pulse transformer for pulse amplification purpose. The 20MHz frequency is selected by setting the select signals values to 101. The duty cycle of repetition control signal is set at 40ns as per the simulation requirement. From the figure 3.4 it can be observed that the required pulse is isolated.

Figure 3.4: 20MHz pulse logic a) 20MHz input pulse(Green) b)Repetition control signal(Red) c) Isolated 20 MHz pulse(Violet)

From the figure 3.5, it is observed that the input 5V 20MHz pulse is amplified to a peak of 325V. The observed voltage droop is less than 20V as the signal hold above 300V for the required pulse width duration. From the figure 3.5 it is can be observed

Figure 3.5: 20MHz 300V Output Pulse)

that the pulse width of the amplified pulse is 25ns when measured at the mid-point of the pulse and the rise time and fall time is 1.7ns as per the equations 3.1, 3.2 and 3.3

From the figure 3.6, we can see the response to the generated pulse that was given as input, using the response that was modeled using first order transfer function to model the human tooth. The obtained waveform have the observed rising and decaying characteristics due to the lossy dielectric nature of human tooth due to its enamel, dentin and pulp resistive and capacitive nature.

3.2.3 1.25MHz Pulse

The 1.25MHz signal obtained from the frequency divider block is fed to the frequency selector logic whose output is fed to the pulse isolator logic using the select

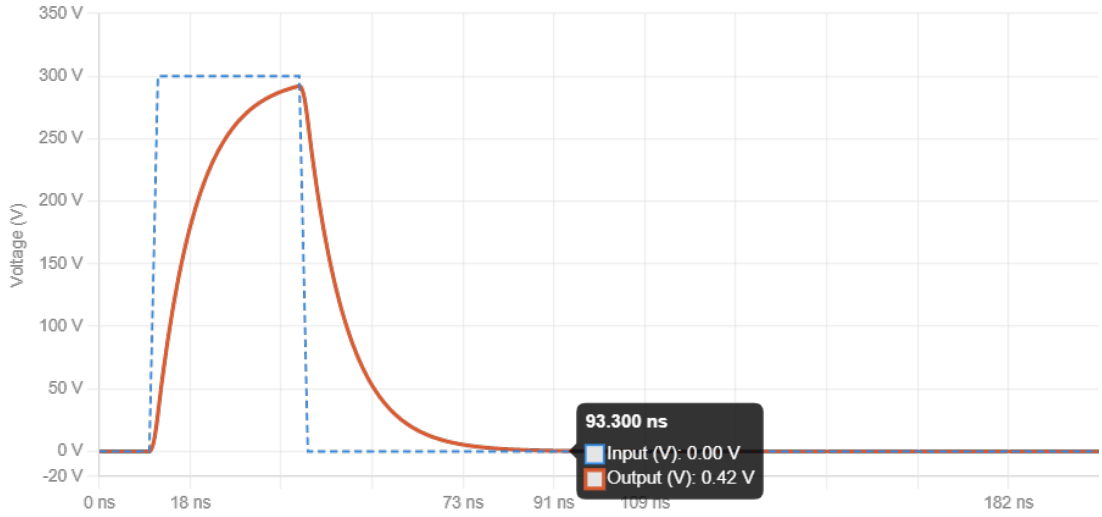

Figure 3.6: 20MHz response

signals and repetition control signal. The isolated pulse is then fed to the pulse transformer for pulse amplification purpose. The 1.25MHz frequency is selected by setting the select signals values to 100. The duty cycle of repetition control signal is set at 640ns as per the simulation requirement. From the figure 3.7 it can be observed that the required pulse is isolated.

Figure 3.7: 1.25MHz pulse logic a) 1.25MHz input pulse(Green) b)Repetition control signal(Red) c) Isolated 1.25 MHz pulse(Yellow)

From the figure 3.8, it is observed that the input 5V 1.25MHz pulse is amplified to a peak of 340V. The observed voltage droop is less than 30V as the signal hold above 300V for the required pulse width duration. From the figure 3.8 it is can be observed that the pulse width of the amplified pulse is 400ns when measured at the mid-point of the pulse and the rise time and fall time is 16ns as per the equations 3.1, 3.2 and 3.3 From the figure 3.9, we can see the response to the generated pulse that was given as input, using the response that was modeled using first order transfer function to model the human tooth. The obtained waveform have the observed rising and decaying characteristics due to the lossy dielectric nature of human tooth due to its enamel, dentin and pulp resistive and capacitive nature.

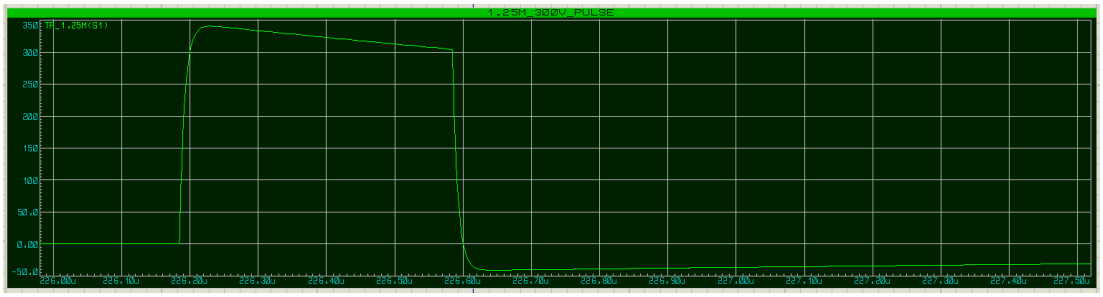

Figure 3.8: 1.25MHz 300V Output Pulse)

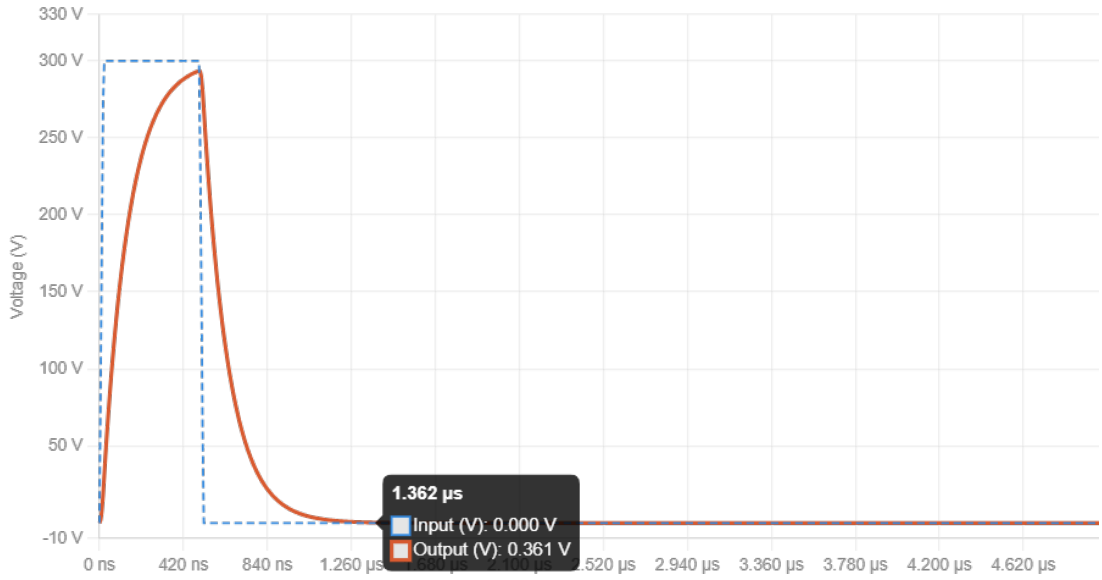

Figure 3.9: 1.25MHz response

3.2.4 625kHz Pulse

The 625kHz signal obtained from the frequency divider block is fed to the frequency selector logic whose output is fed to the pulse isolator logic using the select signals and repetition control signal. The isolated pulse is then fed to the pulse transformer for pulse amplification purpose. The 625kHz frequency is selected by setting the select signals values to 011. The duty cycle of repetition control signal is set at 1.28us as per the simulation requirement. From the figure 3.10 it can be observed that the required pulse is isolated.

From the figure 3.11, it is observed that the input 5V 625kHz pulse is amplified to a peak of 355V. The observed voltage droop is less than 40V as the signal hold above 300V for the required pulse width duration. From the figure 3.11 it is can be observed that the pulse width of the amplified pulse is 800ns when measured at the mid-point of the pulse and the rise time and fall time is 30ns as per the equations 3.1, 3.2 and 3.3

From the figure 3.12, we can see the response to the generated pulse that was given as input, using the response that was modeled using first order transfer function to model the human tooth. The obtained waveform have the observed rising and decaying characteristics due to the lossy dielectric nature of human tooth due to its enamel, dentin

Figure 3.10: 625kHz pulse logic a) 625kHz input pulse(Green) b)Repetition control signal(Red) c) Isolated 625kHz pulse(Yellow)

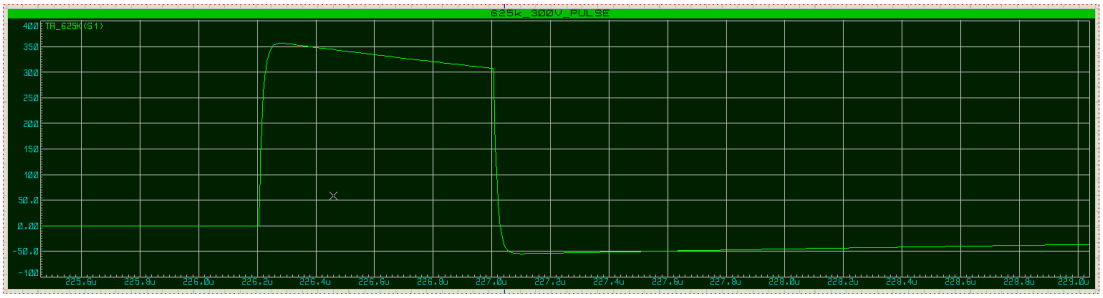

Figure 3.11: 625kHz 300V Output Pulse)

and pulp resistive and capacitive nature.

3.2.5 312.5kHz Pulse

The 312.5kHz signal obtained from the frequency divider block is fed to the frequency selector logic whose output is fed to the pulse isolator logic using the select signals and repetition control signal. The isolated pulse is then fed to the pulse transformer for pulse amplification purpose. The 312.5kHz frequency is selected by setting the select signals values to 010. The duty cycle of repetition control signal is set at 2.56us as per the simulation requirement. From the figure 3.13 it can be observed that the required pulse is isolated.

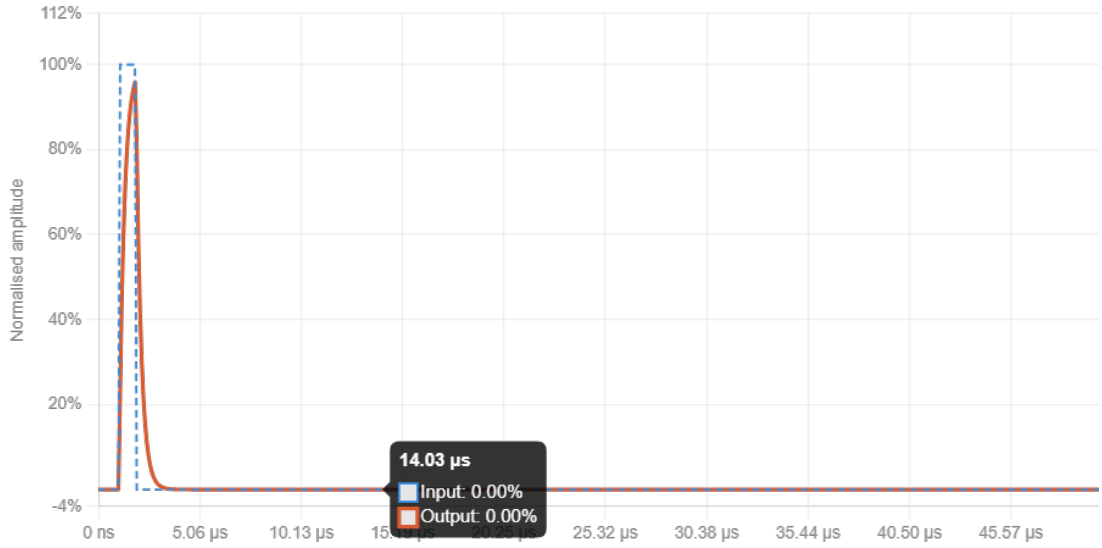

Figure 3.12: 625kHz response

Figure 3.13: 312.5kHz pulse logic a) 312.5kHz input pulse(Green) b)Repetition control signal(Red) c) Isolated 312.5kHz pulse(Yellow)

From the figure 3.14, it is observed that the input 5V 312.5kHz pulse is amplified to a peak of 345V. The observed voltage droop is less than 40V as the signal hold above 300V for the required pulse width duration. From the figure 3.14 it is can be observed that the pulse width of the amplified pulse is 1.6us when measured at the mid-point of the pulse, repeated at 5kHz repetition frequency and the rise time and fall time is 50ns as per the equations 3.1, 3.2 and 3.3

From the figure 3.15, it can be observed that the pulse width of the amplified pulse is 1.6us, repeated at a frequency of 20kHz and the rise time and fall time is 50ns as per the equations 3.1, 3.2 and 3.3. From the figure 3.16, we can see the response to the generated pulse that was given as input, using the response that was modeled using first order transfer function to model the human tooth. The obtained waveform have the observed rising and decaying characteristics due to the lossy dielectric nature of human tooth due to its enamel, dentin and pulp resistive and capacitive nature.

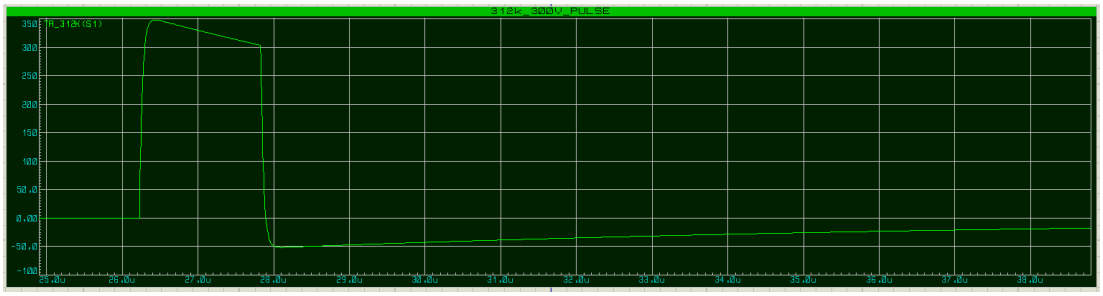

Figure 3.14: 312.5kHz 300V 5kHz (Output Pulse)

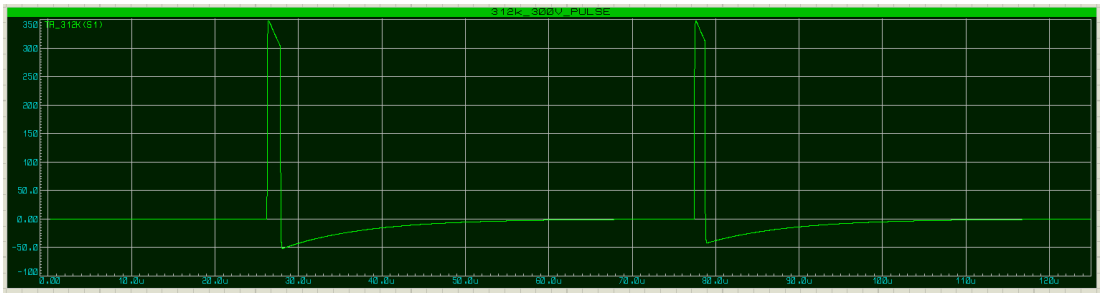

Figure 3.15: 312.5kHz 300V 20kHz (Output Pulse)

3.2.6 39.0625kHz Pulse

The 39.0625kHz signal obtained from the frequency divider block is fed to the frequency selector logic whose output is fed to the pulse isolator logic using the select signals and repetition control signal. The isolated pulse is then fed to the pulse transformer for pulse amplification purpose. The 39.0625kHz frequency is selected by setting the select signals values to 001. The duty cycle of repetition control signal is set at 20.48us as per the simulation requirement. From the figure 3.17 it can be observed that the required pulse is isolated.

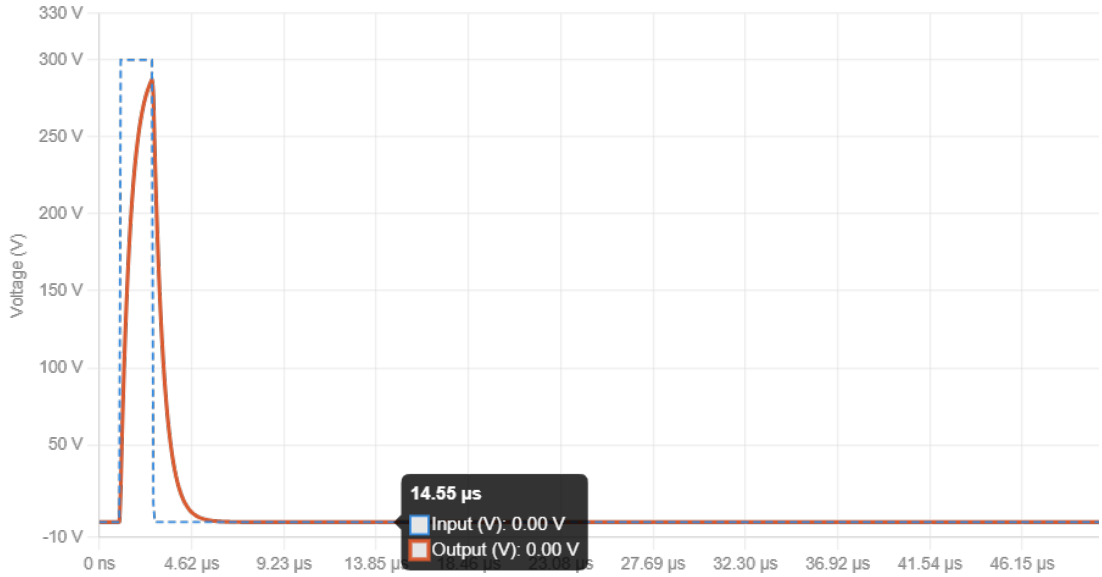

Figure 3.16: 312.5kHz response

Figure 3.17: 625kHz pulse logic a) 39.0625kHz input pulse(Green) b)Repetition control signal(Red) c) Isolated 39.0625kHz pulse(Yellow)

From the figure 3.18, it is observed that the input 5V 3.0625kHz pulse is amplified to a peak of 370V and the signal holds above 300V for the required pulse width duration. From the figure 3.18 it is can be observed that the pulse width of the amplified pulse is 12.8us when measured at the mid-point of the pulse, repeated at 5kHz repetition frequency and the rise time and fall time is 1us as per the equations 3.1, 3.2 and 3.3

From the figure 3.19, it can be observed that the pulse width of the amplified pulse is 12.8us, repeated at a frequency of 20kHz and the rise time and fall time is 1us as per the equations 3.1, 3.2 and 3.3.

From the figure 3.20, we can see the response to the generated pulse that was given as input, using the response that was modeled using first order transfer function to model the human tooth. The obtained waveform have the observed rising and decaying characteristics due to the lossy dielectric nature of human tooth due to its enamel, dentin and pulp resistive and capacitive nature.

In Table 3.1 a comparison of the proposed pulser to several other high voltage pulse generators described in the literature is presented. As can be seen from the table most existing pulse generators are implemented using complex architectures like resonant

Figure 3.18: 39.0625kHz 400V Output Pulse)

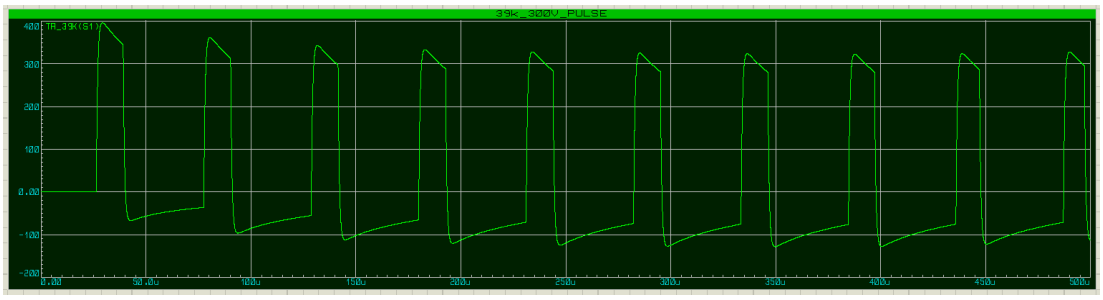

Figure 3.19: 39.0625kHz 300V 20kHz (Output Pulse)

converter, Marx generator, Blumlein pulse-forming network, capacitive chopping circuit, modular pulse modulators or wide bandgap semiconductor-based architectures to generate high voltage pulses. The output voltages are typically from several hundred volts to tens of kilovolts with some architectures achieving nanosecond pulse width. The main drawback of those complex architectures is that they typically require either high voltage DC supply or multiple power stages, complex control strategies, specialized semiconductor switches or a huge number of passive and active components increasing complexity and size.

On the other hand, the work presented here uses a relatively simple architecture involving a D-flip-flop-based frequency divider, logic-gate based frequency selection and pulse isolation circuitry and a pulse transformer for voltage boosting. The proposed pulse generator is capable to generate an output voltage between 300V-400V from only a 5V DC supply and over a wide frequency range between 39.0625kHz and 20MHz. Unlike resonant or Marx pulse generators, the proposed system does not require high energy storage networks, cascaded power stages or high voltage input power source. In addition, frequency selection is easily achievable with digital frequency dividers by changing only one value and the architecture is scalable without significant modifications.

Even though the proposed pulse generator is lower in output voltage than some of the high power pulsed power generators reported in literature, the implementation has the main advantages of being low cost, compact and having a very simple circuit, low voltage source, fewer components and easy control and makes the proposed pulser an excellent candidate for compact biomedical, dental, ultrasound and sensing applications requiring moderate high voltage pulse and wide frequency programmability.

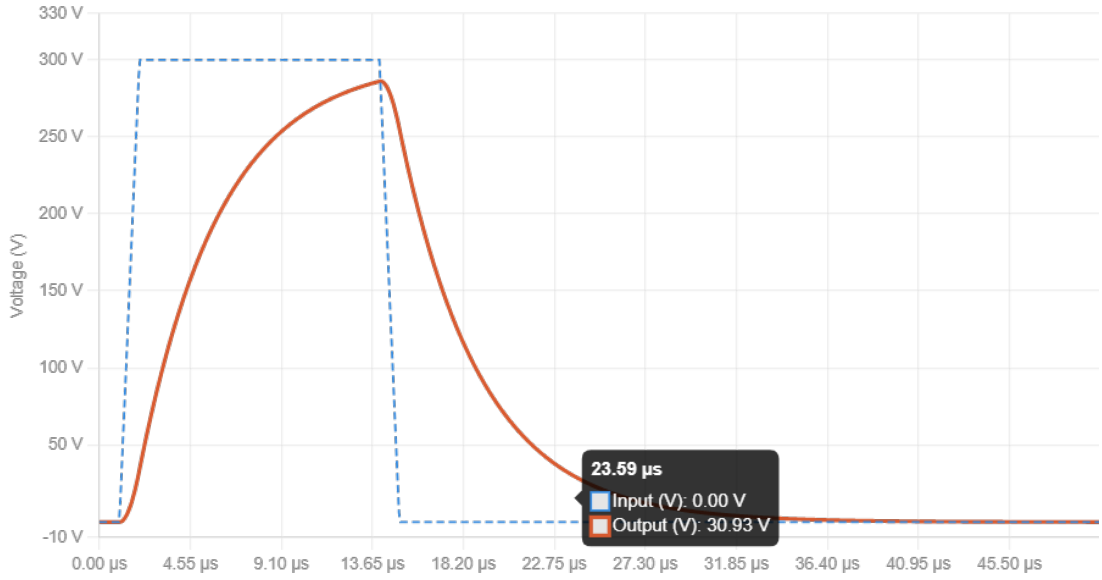

Figure 3.20: 39.0625kHz response

Table 3.1: Comparison of the Proposed Pulser with Existing High-Voltage Pulse Generators

Reference	Topology	Input	Output Voltage	Frequency	Complexity
[11]	Multilevel LC Resonant Network	HV DC	2.8 kV	3 MHz	High
[4]	Capacitive Chopping Circuit	HV Capacitors	6.5 kV	Nanosecond Range	Very High
[12]	LCC Resonant Inverter with SiC MOSFETs	HV DC	±1000 V	1.5 MHz	High
[8]	Piezoelectric Transformer Based Generator	LV DC	Several kV	High Frequency	High
[10]	Solid-State Marx Generator	HV DC	30 kV	0–1 kHz	Very High
[2]	Boost-Marx Generator	235 V	10 kV	Pulse Mode	High
[3]	Blumlein Stack with LC Boost	HV DC	kV Range	MHz Range	High
[5]	Modular Pulsed Power Modulator	HV DC	5 kV	1 MHz	High
[17]	Two-Stage Pulse Transformer System	120 V	1.08 kV	20 kHz	Medium
[6]	Integrated CMOS Pulser	65 V	65 V_{pp}	6 MHz	Medium
Proposed Work	**D-Flip-Flop Frequency Divider + Pulse Transformer**	**5 V**	**300–400 V**	**39.0625 kHz–20 MHz**	**Low**

CHAPTER 4

CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

4.1 Conclusion

In this work, designed and analyzed an efficient voltage pulser circuit that is suitable for high frequency operation with a large output voltage swing. The operation of the pulser was based on a circuit that uses D flip-flops for frequency division. With this, it can achieve many frequencies with a simple implementation and stable timing. AND gate logic was used for selecting the desired pulse frequency, then AND gates were for pulse selection, which isolated the pulse required for generation, avoiding the distortion to pulse frequency or pulse shape and kept the pulse at the required amplitude. A pulse transformer is used for high-voltage amplification and is also able to isolate the power and logic circuit from the output stage.

Simulation result shows the circuit designed can generate a 300V peak to peak pulse with rise time and fall time less than 5ns and 50% duty cycle which lead to very stable operation and symmetrical pulse generation. In conclusion, the design is simple, compact, small in size and can produce high frequency pulse generation for applications which require rapid high voltage pulse signals.

4.2 Future Scope

While the work has been carried out to achieve all the listed objectives, there are some ways in which few additional works that can be made upon this work. The additional works can be done to make changes in the following areas:

1. While the number of frequency channels chosen in this work is five, it is not limited to 5 but can be increased to desired number by making changes in the frequency divider block.
2. Further work on pulse transformer can be carried out to achieve higher output voltage swings.
3. While the proposed work uses D flip flop based frequency divider to obtain various frequencies, other methods could also be explored.

While the above listed areas are just some of the areas where future work can be carried out, but it is not limited to those areas as future work could be carried out in terms of other aspects as well to further enhance this work.