MODELING, ANALYSIS AND CONTROL OF POWER CONVERTER TOPOLOGIES FOR EV CHARGING APPLICATIONS

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I, SIVANANTH G, Roll No – 2K24/PES/20 student of M.Tech in Power Electronics and Systems, Department of Electrical Engineering,hereby declare that the thesis Dissertation titled "MODELING, ANALYSIS AND CONTROL OF POWER CONVERTER TOPOLOGIES FOR EV CHARGING APPLICATIONS" which is submitted by us to the Electrical Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "MODELING, ANALYSIS AND CONTROL OF POWER CONVERTER TOPOLOGIES FOR EV CHARGING APPLICATIONS" which is submitted by SIVANANTH G, Roll No –2k24/PES/20, Power Electronics and Systems, Department of Electrical Engineering ,Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Abstract

With the recent rise of EVs, demand for better, reliable performing chargers with more efficiency is increasing. Role of converters is crucial in Electric Vehicle chargers to efficiently convert power, improve power quality, and safely operate the battery charging. In this thesis, a modelling, analysis, control and comparison of some power factor correction coverters (PFC) and two isolated dc-dc converters that can be used for EV chargers are carried out.

For the first rectification stage in front end, three different PFC converters;Boost PFC, Interleaved Boost PFC and Flyback PFC, are modeled and simulated in MATLAB/Simulink. Power Factor improvement, THD, output voltage ripple, regulation and conversion efficiency are observed for each topology and a comparative study between these three converters is carried out. From the studies that the Interleaved Boost PFC offers an advantage for reducing source current ripple & improves sharing of the current in switches, with less harmonics. Flyback PFC converter is used with galvanically isolated stage for low to medium power chargers.

For the second stage, FBC and PSFB topologies are studied. Performance evaluation, like voltage regulation, switching features, and power capacity were compared along with power transfer capability and efficiency. The FBC offers efficient power transfer with isolated stages, and is effective for mid to high level power chargers. PSFB provides improved efficiency and reduces the switching stresses using soft-switching.

Finally, comparison is done between all mentioned topologies in order to select appropriate converter configuration.Keywords: Electric Vehicle Charging, Power Factor Correction, Boost PFC, Interleaved Boost PFC, Flyback PFC, Full Bridge converter, PSFB , Power Quality, MATLAB/Simulink.

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CHAPTER 1

INTRODUCTION

1.1 Overview

This work deals with investigating various converters and their control techniques to achieve better power quality, lesser harmonic distortions in the suitable range to meet the need of the modern EV charging. The accelerated growth of EV applications has greatly accelerated the development of state-of-art power electronic conversion systems. Increasing consciousness towards the environment, depletion of fossil fuels and stringent rules and regulations have provided a passage from conventional internal combustion engine vehicles to EVs. EVs are more efficient, environment friendly, economical to run, utilize the power efficiently and are considered as one of the most viable options for future energy generation.[1] [2]

Many power conversion stages are required for modern electric vehicle application i.e., Battery charging, auxiliary power supply, energy management. Many power conversion stages are involved in modern electric vehicles such as: rectification stage, PFC, dc-dc & load regulation. All these stages greatly influence the charging efficiency and reliability of electric vehicles, and ultimately the charging performance [3].

In conventional rectifier stage, diode bridge rectifier is used along with a large filter capacitor to build simple and low-cost circuit. Such circuits have input current that appears as a highly distorted form of current. The current from the grid appears as a pulse having narrow and high magnitude at the peak value of the voltage. Such circuits have very poor power factor and suffer from high harmonics[4].

The generation of harmonics by nonlinear devices affects power system in various manners: Overheating of transformers and cables, Generation of noise at power frequency, voltage distortion and decreased reliability of electrical devices used in associated circuit. The low power factor demand for a large value of apparent power from the grid, therefore decreasing overall system efficiency. So for all these issues there is a need to comply with standard limits such as IEC 61000-3-2 [2, 5].

There are numerous PFC techniques available. The boost converter topology is preferred and frequently used because of its simplicity in structure, higher efficiency and better control over input current waveform. For control of conventional boost PFC circuits, PI controller is extensively used, due to its simplicity. However, the PI controller cannot accurately compensate for the harmonics under dynamic conditions. Advanced control techniques are often implemented for enhanced performance like Proportional Resonant (PR) control, Lyapunov-based nonlinear control.

Higher power applications of boost PFC converter necessitates an interleaved topology, because of reduced current ripple, more even thermal distribution of losses and increased efficiency. An interleaved boost PFC converter utilizes multiple converter phase units displaced in time, reducing current ripple at the input.[6, 7]

Isolated second stage are used for chargers in addition to PFC stage for isolation purpose and to provide regulated output. The FBC is best for mid to high power isolation purpose as it is appropriate for higher power application and efficient utilization of transformer. PSFB[8] is an advanced topology and gives advantage of soft switching and high frequency applications.Flyback PFC with Single stage is a viable alternative for small applications with low power. It operates in DCM with naturally sinusoidal shape.[9][3] [4].

In this thesis various converters and their control techniques appropriate for EV charging applications are studied and compared against one another. The performances comparison involves the implementation and comparison of the PI based, PR based and Lyapunov based controlled Boost PFC & Interleaved Boost PFC, single stage Flyback PF, isolated dc-dc converters like FBC and PSFB, compared based on power factor, THD, efficiency, voltage regulation.

1.2 Need for EV Charging Converters

The recent rapid penetration of electric vehicle (EV) markets leads to the high demands for efficient and economical EV charging systems. Unlike ordinary electric loads, EV charging systems are characterized by various input voltages, high power operation and strict requirements of power quality, and the control stages must accommodate different input voltages and high power levels. Due to it acting as the link between the electrical grid and the EV battery, performance characteristics such as efficiency and system reliability are vital for the system.[10]

An efficient ac-dc converter is an indispensable part of any EV charging system as it provides a constant voltage to charge a battery while source provides AC. Given the need for a voltage regulation mechanism, a galvanic isolation scheme, a battery management system, and an auxiliary power supply capability, a multi-stage conversion system is needed.

The traditional EV charger based on uncontrolled diode rectifier results in insufficient efficiency and a high degree of current harmonic distortion, which arises from the fact that due to its non-linear behavior, diode rectifiers exhibit high input current distortion, which in turn has an adverse impact on power quality in the grid. Since a huge no. of EVs needs to be charged from grid, severe harmonic pollution due to charging system operation accumulates rapidly, causing strain on electrical distribution systems and degradation of integrated electrical devices.

A highly efficient power conversion capability is also a necessary criterion for EV charging system design, as EVs are typically driven for long periods and require large amounts of energy. A high efficiency power converter is therefore most suitable for efficient energy delivery and switching loss reduction. High switching frequency offers an efficient method for improving power converter efficiency. It allows for high switching frequencies, while meeting specified energy delivery and output voltage within a

certain timeframe.

The galvanic isolation is very important for safety. The dc-dc isolated converters provide this. FBC & PSFB designs are often chosen for medium to high power applications for their relatively high efficiency and appropriate transformer performance. Simple and economical topologies like the flyback converter can be considered for lower power systems[9].

Another important criterion to meet for modern EV charging system is power quality. International standards for electric vehicle charging, such as IEC 61000-3-2, define limitations on harmonics into the grid. An EV charging system should have high power factor and low THD.

Advanced control strategies such as PI, PR, and non-linear controller based on Lyapunov method must be employed to achieve good voltage regulation and fast dynamic response under grid voltage and load variations. It is apparent that power electronic converters with high efficiency play an increasing role in modern EV charging systems, the demands for which continue to grow for faster, more efficient, compact, and safe charging systems. Therefore, comprehensive analysis and effective control of these converters are of paramount importance.

1.3 Issues in Power Quality

Growth in the no, of power electronic converters employed in electric vehicle charging stations leads to degradation of power quality. The converters used in most of these chargers consist of high frequency switching converters and nonlinear rectification stages, which tend to consume non sinusoidal currents from grid. The resulting distortion leads to harmonic pollution, coupled with low power factor and poor efficiency of the entire system.

Typically, a rectifier is formed by a dbr with a huge dc link capacitor. The capacitor can only be charged when the instantaneous voltage provided by grid exceeds the voltage level in dc link capacitor. This causes short pulses being generated as input current, with each pulse being emitted when the AC source voltage reaches its peak. The input current can therefore be described as highly distorted and non sinusoidal[6, 7].

A multitude of problems can result from harmonic currents being generated. The increased harmonic content causes a higher rate of power loss, both in transmission lines and transformers, and in electrical machines; the additional heating due to these harmonics. The voltage waveform across the distribution network becomes distorted as a result of these harmonics and the effects may be undesirable for certain sensitive devices powered by the same bus. Excessive harmonic components in the current lead to increases in interference, and also a decline in overall lifespan and reliability of electronic components.

Poor power factor is another significant problem encountered in these types of systems. While the real power can be said to remain the same, it has to be understood that the harmonics will increase the apparent power being supplied by the mains. This consequently means that larger quantities of power are consumed from mains and this leads to wastage of resources.

The THD of input current is most widely used means of assessing the quality of

power. A high THD is synonymous with low quality and poor performance of the converter. This kind of THD leads to instability of the grid, malfunctioning of other components coupled to the same bus and thermal overload of certain electrical devices. Such negative consequences indicate that high quality is of utmost importance, and have lead to the implementation of very strict regulations for harmonics, both in modern power systems and in power electronics.[2, 5]

1.4 PFC Techniques

PFC is a key function needed these days in power electronic system. The key reason for use of PFC is to make the source current closely matches with the input voltage waveform, hence the converter can achieve better power factor & very low THD [11]. PFC methods have been broadly classified into two main categories; namely,

1.4.1 Passive PFC

In this, inductor, capacitor and L/C filter elements are utilized to decrease the harmonics. The main benefits are the simplicity of control and low component cost, however, there are some shortcomings; they are bulky and heavy, dynamic response is bad, harmonics compensation is not efficient and their efficiencies are poor at large power levels. Usually the Power factor of these types of PFC is around 0.7 to 0.8, so it is not suitable for the high performance and modern EV chargers[9].

1.4.2 Active PFC

This uses a switching converter and some closed loop controllers to make source current follow the source voltage. They provides low THD & high efficiency . They are compact, lightweight, and fast responding. Because of these advantageous features, Active PFC methods are more favorable in application for EV chargers and industrial power supplies.

Several types of active PFC converters are discussed below.[3, 9].The performance of PFC converter is greatly depends on the chosen topology as well as control methods. While PI controllers are commonly utilized and simple, their use in PFC will lead to static state error and low harmonic reduction capacity. Control methods like PR controller and Lyapunov-based non-linear control approaches significantly improves current tracking ability and reduce the THD of a PFC converter. Hence research for novel control strategies of Active PFC converter for modern EV charger becomes important[3].

1.4.3 Types of converters used for PFC

Several topologies have been explored for single-phase PFC front ends:

1. **Boost Converter (Most Common):**
   (a) Simple structure, high efficiency, near-unity power factor.

(b) Operates only in step-up mode hence limiting its use in low input voltage conditions.

(c) Widely used in commercial EV chargers [6, 7]

2. **Buck–Boost Converter:**

   (a) Has increasing or decreasing capability.

   (b) Useful for wide-range input voltages: 90 V–265 V AC.

   (c) Primary disadvantage: higher component stresses and lower efficiency compared to Boost

3. **SEPIC Converter:**

   (a) Allows both to increase and decrease voltage with non-inversion.

   (b) More flexible but requires more components.

   (c) Suitable for universal input EV chargers.

4. **Cuk Converter:**

   (a) Provides increase or decrease in voltage capability with low current ripple at input.

   (b) More complicated, less effective since there is a multitude of elements for energy storage.

5. **Bridgeless Topologies:**

   (a) Input diode bridge elimination, reducing conduction losses.

   (b) Improved efficiency, especially at higher power levels.

   (c) Complex control and EMI challenges.

Several other converters and variations are also used depending on advances in semiconductor devices and system requirements.

1.4.4 Control Strategies used in PFC converters

Control plays an essential role in shaping the input current and maintaining constant dc bus voltage. Some commonly adopted strategies include -ACMC, [12] PCMC, [12] & Hysteresis control.

1.5 Isolated DC-DC converters

Needed mainly due to two reasons, isolation for safety & minimize noise and EMI.For low power applications (below 500 W) Flyback converter is the best choice due to its minimum number of components and less cost. For medium - high power applications (above 500 W) FBC is used.[13, 14]

Other isolated converters like PSFB converters, Resonant converters, are implemented to obtain high efficiency & large frequency purposes. These can implement the ZVS and ZCS(Resonant).[15, 16]

Control techniques are used to get a stable, undistorted o/p voltage. The techniques used are, PI or PID controllers (Linear control) & others like Lyapunov[9].

1.6 Objectives of the Thesis

In accordance with these above objectives the present thesis will endeavour to address each of them as below:

1. To model and analyze performance characteristics of different power converter topologies used in EV applications.
2. To design and implement a basic Boost PFC converter to optimize power factor at input, reducing input harmonics.
3. To implement and analyze performances of different controllers i.e PI, PR and Lyapunov based techniques used for Boost PFC.
4. To analyze and develop a multi-phase or interleaved Boost PFC converter for reducing the ripple, increasing overall power density.
5. To model & analyze a Flyback PFC converter operated in D.C.M mode.
6. To design and analyze isolated dc-dc converter topologies, (FBC and PSFB).
7. To implement effective closed loop control strategies for precise output control & improving transient performance.
8. To compare efficiency, power factor, THD, voltage regulation and transient performance of all the developed power converter topologies.
9. To analyze all the developed power converter topologies in MATLAB/ Simulink.

1.7 Scope

The scope of work is to do modeling, analysis & control of power converters for EV charging.This thesis covers the below mentioned topics;

1. Boost PFC with PI, PR & Lyapunov control.
2. Interleaved Boost PFC with PI and PR control.
3. Single stage Fly back PFC converter in DCM operation.
4. Full Bridge and PSFB converter.

The performance is measured on the basis of power factor, THD, & voltage regulation, dynamics etc. All the graphs are the results of simulations. No hardware was available for experimental verification.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Recently, EV chargers utilize converters in one form or another. In the present day with ever increasing numbers of EV, many different forms of power electronic converters are being researched for high efficiency and for potentially achieving better power quality and reduced total harmonic distortion. Different number of power conversion stages are implemented in an EV charging system namely, ac to dc, pfc, Isolated dc - dc power stages. In order to achieve this we have to use good control strategies.

Numerous research has been done in various control schemes such as proportional-integral (PI) controller, which is commonly implemented as it's the easiest, or other advanced controllers like proportional-resonant (PR) controller and Lyapunov control are being explored in recent times.

2.2 Boost PFC Converter

It has growing interest among researchers and is discussed extensively in the literature because it is simple, low THD, high efficiency. It is able to give a higher output than rectified input, and offers good power factor correction capability.[7] [6] [17]

Several modes of operations have been studied on boost PFC converter, namely CCM, CRM and DCM. The current ripple and peak current is lower in CCM than in DCM, but it has complicated control. The DCM control is simpler and natural shaping of current, but at higher power levels, it has a greater stress and conduction loss than the CCM.[7] [6] [17]

Numerous control strategies are applicable for boost PFC. PI controller is commonly used due to its simplicity in control. However, the PI control cannot perfectly compensate the harmonics under transients. Advanced control schemes like proportional resonant (PR) control and nonlinear Lyapunov based control were later developed to eliminate this limitation.

The PR control is found to obtain a well sinusoidal current and low steady state error. This control gives better power factor as it achieves low THD and also exhibits satisfactory dynamic performance. Lyapunov based nonlinear control aims to improve the system stability during parameter and load disturbances.[7] [6] [17]

Though the boost PFC converter has several merits, it has some demerits also. It has only boost mode of operation. Fast switching leads to more losses & EMI which

might require specialized control design and circuit optimization.[18]

In general, the boost PFC converter remains to be a highly efficient converter with a simple control scheme to make its way through as a preferred choice in EV charging and advanced power electronics applications.[7] [6] [17]

2.3 Interleaved Boost PFC Converter

Due to growing demand of high power EV charging systems, limitations of single phase Boost PFC converter such as high input current ripple, heavy thermal stress, large conduction loss and so on, become more evident. Therefore multi- phase interleaved Boost PFC is investigated for mid to high rating applications.

Formed with interconnecting multiple conventional Boost converter leg with their respective inductors and switches in parallel. Input switch of each leg is turned on and off in out-of-phase, the phase difference between any two legs switching signal is controlled through varying different delay angle. Interleaving different legs switching signal phase can result in partial cancelation of ripple component and significant reduction of total input current ripple. As the effect of current ripple cancelation, a interleaved converter system has lower input current ripple and consequently less EMI emission compared with the conventional single phase converter.[19] [20] [21]

There are also numerous papers have reported interleaved Boost PFC converter has better efficiency and thermal distribution than conventional single phase Boost converter. Due to the shared load current distribution among the number of parallel Boost converter legs (i.e. Switches, inductor and diodes) the components' current stress will be smaller so that the reliability of the converter is enhanced so as to achieve higher power rating.

As the researchers found, by effectively reducing input current ripple, the interleaved converter require smaller input filter. Small input current ripple means smaller pass components will be applied so as to reduce the size and improve power density.

Depending on desired power value and stage numbers, different interleaving methods can be used. 2 phase interleaved boost converter can significantly reduce ripple in current & controller can be easily designed, this topology has been applied widely in EV charging application. If further ripple cancellation is desired then high stage interleaving can be used but complexity is increased.[19] [20] [21]

Various control strategies have been developed by [22] for interleaved boost PFC converter, the standard PI controller was mainly used method due to its simplicity, but it can not compensate well for dynamics harmonic components under transient condition.

Thus PR (proportional resonant) controller was proposed for interleaved converter. PR controller can make AC signal tracking have very small tracking error with unity power factor, it have been demonstrated that THD and power factor is significantly improved in interleaved converter with PR controller than PI controller.

Besides many advantages of interleaved Boost converter, there still exist few disadvantages such as complex driving circuits, need balance the current of each leg, and synchronization of switching signals between stages are required, thus effective controller must be used to maintain steady converter system operation.[19] [20] [21]

2.4 Flyback PFC Converter

In case of small power range uses, this topology can be useful, because of combining power factor correction and isolation in a single stage. Since a Flyback topology is the simple, with low component count, small size it is a candidate to be used for EV auxiliary charger and low power battery charging application.

This works in DCM was reported by Choi et al. In [13]. The paper show simplified control structure with input current shaping improvement. Since at DCM operation, magnetizing current is start from zero and return to zero it allows shaping the input current without complicate control scheme [13, 14]. Wang et al. In [14] analyzed control scheme and mode of operation for isolated PFC and claimed better voltage regulation by the controller design. According to the authors Flyback converter is the preferred for compact charging application which demands for isolation and low component number. At [23] Flyback based EV charging application is demonstrated to have smaller size and simpler configuration in the context of one stage with both PFC & isolation. This topology has been found as a alternative for small range charger & auxiliary supply.

For PFC purpose Flyback converters often work at DCM, when magnetizing current starts from zero during each cycle and is return to zero. By using this working operation we can shape the input current, and achieve power factor correction without using complicated current feedback loop [13, 14].

The disadvantage of the Flyback PFC converter topologies in compared to other is that, the higher current stress, the relatively higher switching loss of the switch, the higher output voltage ripple and also more critical design for the transformer due to storage of energy and galvanic isolation for all type of Flyback converter topologies [13, 14]. Various control schemes, for example PI control, dual loop voltage-current control have been proposed to improve the regulation of the Flyback PFC converter [24]. It is concluded that for low power application like in EV charger the Flyback PFC converter shows a simple and low cost solution due to its simple configuration, however the high current stress limitations prevent its use in high power application.

2.5 FBC

FBC most common at mid and high power purposes as it has efficiency of transformer utilization, higher power transfer and galvanic isolation. It is used as a power conditioning stage in EV charging systems after the PFC to regulate low voltage DC output for battery charging [25, 4, 3].

Various researches have proved that FBC can be efficiently used in high power applications. Jain and Joos [25] claims that FBC could achieve better power transfer and less device stresses when compared with low power isolated converters. The circuit design could work effectively at applications with requests for high power transfer and high efficiency usage of transformer.

In the original researches of Mohan et al [3] and Hart [4], FBC can be seen as a bridge composed of four switches which are all controllable. The input given is then rectified and filtered into a required low voltage DC output. Since the power is transferred in both half-periods of the AC signal, this means that it will result in higher

efficiency usage of magnetic component and higher power density.

Within the scope of EV charging applications, studies indicate that FBC has a favorable operating condition to use as an isolated battery charger [1]. Such results indicate that the circuit is able to manage its output voltage properly and provide electrical isolation. Therefore, it is widely applied as a medium and high power converter.

PI controllers have traditionally been employed due to its simplicity and good voltage regulation feature; however some modern controls, like soft-switching & smart modulation, were proposed and developed to reduce switching losses and device stresses so that converter efficiency can be increased [25, 4, 1].

Four switches are used in FBC converter. As the control circuit for four switches becomes complex, and synchronization is essential to prevent shoot-through condition. Designing a suitable high frequency transformer also plays a vital role in power density and performance.

2.6 PSFB

PSFB is a common converter topology used in large rated purposes as it has capabilities like better efficiency & low loss switching. It is found to be very attractive for EV charger, telecom power, server power and industrial power applications that are associated with the requirement of high efficiency and power density [26, 15].

Several researches were found investigating the application of PSFB converters in high power chargers. According to one recent work, PSFB converter achieves significantly improved performance over the conventional hard-switched Full Bridge converters through utilizing phase shift control strategy [26]. Instead of changing duty ratio, the PSFB uses the phase difference in gate drive signals for the bridge legs while keeping switching frequency constant. Thus, it achieves appropriate voltage regulation and also makes soft switching possible.

One of the most prominent features of PSFB converter is its ability of achieving zero voltage switching (ZVS). As demonstrated in literature, ZVS is crucial for greatly reducing switching losses as power switches[15, 16]. This reduces stress on the power devices, increases converter efficiency and reduces EMI. These properties make it more suitable for EV chargers that requires high efficiency and effective thermal management.

There have been several comparison studies showing that PSFB converter shows better performance than conventional Full Bridge converter under medium and high power range application. This improvement is achieved because the PSFB converter offers lower switching losses and better thermal characteristics [27, 26]. A high frequency transformer provides the necessary isolation & used for provide voltage gain through adequate turns ratio. Moreover, higher frequency reduces the magnetic component size to yield high power density.

Various control schemes have been researched and proposed ofr better operating PSFB converters. PI controller based closed loop control remains popular due to its simple implementation and good steady state characteristics. Additionally, soft-start schemes are frequently implemented to limit the in-rush transient dynamics[16].

PSFB converter offers several advantages, there are also certain design challenges

to be considered. The optimal ZVS can be heavily affected by parameters such as leakage inductance, load current, switching dead time and transformer design. When operated in minimum loads, efficiency may decrease significantly [15, 16]. Therefore, proper design for magnetic components and switches needed.

With literature reviewed, it can be concluded that the PSFB converter is an efficient choice for high power application such as EV charging system that can greatly provide high efficiency and minimize switching stress through achieving soft switching operation.

2.7 Control Techniques Used in Power Converters

In the operation of EV charging converter, the control technique mainly determined the performance and the power quality of the converters as well as stability. In general, the control has assure the output to be constant, provide stable operation while under load variations, and decrease the harmonic on source in order to achieve better input power quality. Based on these considerations, researchers have been focused on several different control techniques for improved transient response

PI controller is one of the most commonly utilized technique that is easy to implement and provides good steady state performance. The researchers had adopted this technique for Boost PFC, Flyback PFC, FBC & PSFB in order maintain output voltage and provide stability [17, 18]. Integral of PI controller is responsible in eliminating the steady state errors while proportional term helps to get faster dynamic responses.

However, PI controller was found to be poor in AC current control applications since they have a finite gain at fundamental frequency, can never perfectly track sinusoidal references and are incapable of efficient harmonic rejection [3]. The efficiency degrades under the changing input condition or nonlinear load.

To resolve this drawback, the proportional-resonant (PR) controller was proposed. The infinite gain achieved at resonance frequency which would enable very accurate tracking of the reference sine current with negligible steady-state error [17]. Experiments also showed that the PR-controlled PFC converter had better power factor & lower THD compared with PI-controlled converters. PR control is hence often utilized for boost PFC and interleaved boost PFC converters under sinusoidal AC current control conditions.

Advanced control methods such as Lyapunov-based controller has recently obtained significant interest for modern power electronic converters. This type of control offers robustness and stability properties of the converter system. Based on nonlinear control theory, it can guarantee the stability by fulfilling the Lyapunov stability criteria [28]. This controller was shown to have fast dynamic, small overshoot, and improved robustness against input voltage variations, load variations, and parameter variations.

Apart from the aforementioned controllers, SMC, MPC, and hysteresis control fall under advanced control techniques. Although these methods can perform better than classical linear controllers with good robustness, they are very complex and computationally intensive [28].

In comparing these works, it is clear that the control technique is important to the EV charging converter's performance. Although the PI is simple, PR controller of-

fers better harmonic rejection with the regulation of the AC current. For an extreme nonlinear operating conditions, the Lyapunov-based controller can even provide more effective controllability. Further research on control methods is definitely required in order to find out which one could provide the optimal control performance and efficiency for the EV charging converters.

2.8 Research Gap

From the above literature survey it has been observed that there is a considerable number of works on each individual PFC converter topologies and isolated DC-DC converters for the EV charging application. The majority of these works are focused towards enhancing the power factor and THD reduction along with efficient operation of the converter structure, varying with control techniques.

Many of the conventional studies on the Boost PFC converters with the PI-based control technique shows that results are acceptable, but the performance in harmonic compensation and the transient response under load variations are poor. Studies have been carried out separately for advanced control techniques such as PR and non-linear Lyapunov based control. Though there is less investigation of comparing the control schemes for the same conditions.

Similarly for higher power application interleaved Boost PFC converters are used since current ripple is less and heat distribution is better. Detailed analysis between the conventional and interleaved converter with different control strategies are not explored to its potential in many literatures. For low power isolated application Single stage Flyback PFC has also been studied with less components and simpler structure. But in most of the literatures only two stage PFC structure or an isolated DC-DC converter alone are explored not combined for EV charging.

In high power isolation system FBC & PSFB are mainly studied for high power, high efficiency applications with the provision for isolation. PSFB converter offers soft switching, but limited investigation are available in literature concerning both converters together under EV charging operation.

Hence it has been observed that some literatures are focused on analyzing AC-DC stage alone and others have worked on individual DC-DC stage separately. There is an immediate need to work on a combination of these different converter topologies and control methods in an integrated manner for the EV charging application.

Therefore the present work is to investigate the following aspects:

1. Comparative analysis between the conventional and interleaved Boost PFC converter.
2. Comparative analysis between the PI, PR and Lyapunov based control techniques.
3. Investigation on single stage Flyback PFC converter.
4. Comparison of FBC & PSFB.
5. Comparison of overall system performance under various EV charging application conditions.

2.9 Conclusion

In this chapter, a extensive literature review for different converters topologies & control strategies adopted for EV chargers were carried out. Boost & interleaved boost PFCs, Flyback PFC, FBC & PSFB with their operating principles, advantages and disadvantages have been discussed. Also, the significance of using advanced control strategies like PI, PR and Lyapunov based control to improve the converter performance and its power quality as well as dynamic response were identified in the literature review. Some of the existing studies on harmonic reduction and power factor improvement and isolated DC-DC converters were surveyed.

From the literature review conducted, research gap was identified to be on the comparative study of multiple converters and control strategies for EV chargers, which is addressed in the present work by performing modelling, analyzis & control of different PFC & isolated conerter topologies using MATLAB/Simulink. The system architecture and basic concepts required to study the converter topology and its control in the next chapter are presented in the following.

CHAPTER 3

BOOST PFC CONVERTER

3.1 Introduction

It has growing interest among researchers and is discussed extensively in the literature because it is simple, low THD, high efficiency. It is able to give a higher output than rectified input, and offers good power factor correction capability.[7] [6] [17]

Several modes of operations have been studied on boost PFC converter, namely CCM, CRM and DCM. The current ripple and peak current is lower in CCM than in DCM, but it has complicated control. The DCM control is simpler and natural shaping of current, but at higher power levels, it has a greater stress and conduction loss than the CCM.[7] [6] [17]

Numerous control strategies are applicable for boost PFC. PI controller is commonly used due to its simplicity in control. However, the PI control cannot perfectly compensate the harmonics under transients. Advanced control schemes like proportional resonant (PR) control and nonlinear Lyapunov based control were later developed to eliminate this limitation.

The PR control is found to obtain a well sinusoidal current and low steady state error. This control gives better power factor as it achieves low THD and also exhibits satisfactory dynamic performance. Lyapunov based nonlinear control aims to improve the system stability during parameter and load disturbances.[7] [6] [17]

Though the boost PFC converter has several merits, it has some demerits also. It has only boost mode of operation. Fast switching leads to more losses & EMI which might require specialized control design and circuit optimization.[18]

In general, the boost PFC converter remains to be a highly efficient converter with a simple control scheme to make its way through as a preferred choice in EV charging and advanced power electronics applications.[7] [6] [17]

This chapter describes the modelling, analysis, & control of boost PFC. The topology, mode of operation, mathematical models, controller design and simulation results using PI, PR and Lyapunov based controller are presented.

3.2 Converter Topology and Operation

This circuit is made up of a few things: a DBR , a diode, a power switch, a inductor, an capacitor & output.

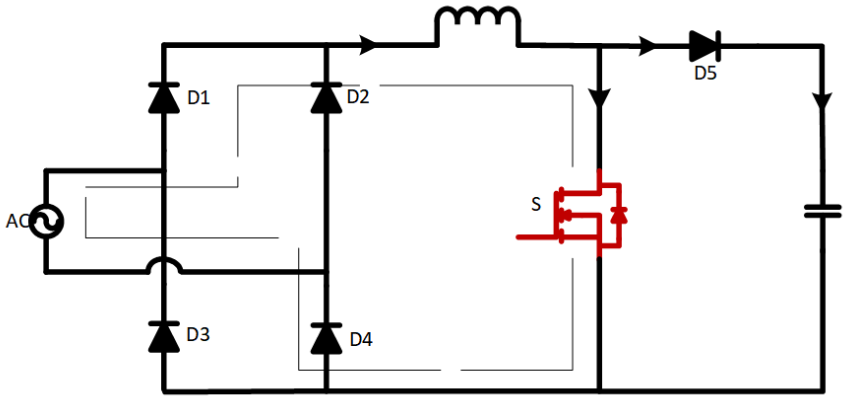

Fig. 3.1: Circuit diagram of Boost PFC

This stage does one thing: it takes rectified voltage & boosts into a regulated DC output actually more than the input.[6, 7].

Tbl. 3.1: Parameters of circuit

Parameters	**Symbol**	**Value**
Source	V_{in} (ac)	230 V_{rms}
Output Voltage	V_o	400 V
Load	R	80 Ω
Inductor	L	1 mH
Capacitor	C	5 mF
Switching Frequency	F_{sw}	25 kHz

The table 3.1 contains all the parameter values for the circuit.

- Switch ON Condition:

Inductor is connected directly to supply and stores energy. Inductor current rises linearly with time. During this interval Diode is OFF, load energized from capacitor[11].

- Switch OFF Condition:

Here, diode is ON, the output gets it power through diode. Voltage in the inductor changes polarity, so output is boosted. [11]

3.3 Mathematical Modeling and Design

The mathematical modeling of the boost PFC is done from its two modes of operation. This model is used to get necessary parameter values & to design control logic. The moathematical modelling as follow: [6, 7]

3.3.1 Mode 1: (0 to t_{on}) (Switch – Closed & Diode – Open)

The current in inductor increases linearly simultaneously, capacitor discharges slightly to maintain load voltage.[6, 7]

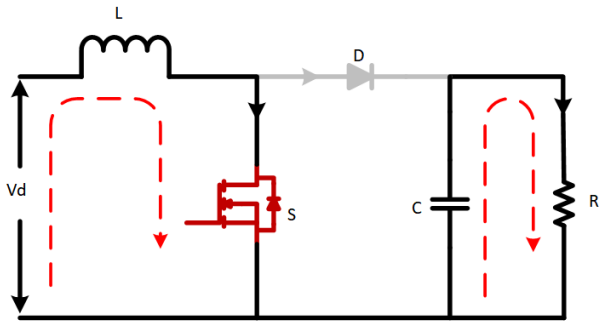

Fig. 3.2: Boost PFC Circuit Mode 1

from [6, 7] By KVL [4],

$$-V_{in} + L * \frac{di_L}{dt} = 0 \tag{3.1}$$

$$\frac{di_L}{dt} = \frac{V_{in}}{L} \tag{3.2}$$

from [6, 7] By KCL [4],

$$i_D = i_c + i_o \tag{3.3}$$

$$i_c = i_D - i_o \tag{3.4}$$

$$C \cdot \frac{dV_c}{dt} = -\frac{V_o}{R} \tag{3.5}$$

$$\frac{dV_c}{dt} = -\frac{V_c}{R \cdot C} \tag{3.6}$$

3.3.2 Mode 2: (t_{on} to T) (Switch – Open & Diode – Closed)

By KVL [4],

$$-V_{in} + L * \frac{di_L}{dt} + V_c = 0 \tag{3.7}$$

$$\frac{di_L}{dt} = \frac{-V_c}{L} + \frac{V_{in}}{L} \tag{3.8}$$

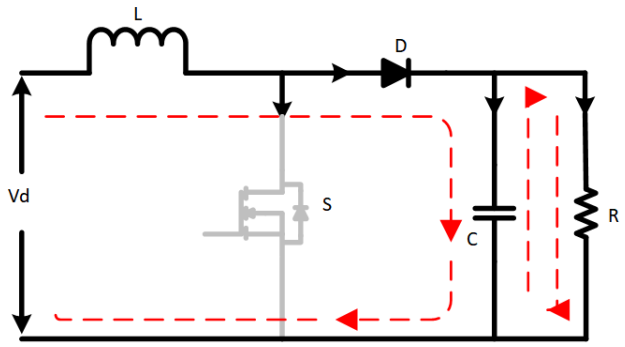

Fig. 3.3: Boost PFC Circuit Mode 2

By KCL [4],

$$i_D = i_c + i_o \& i_D = i_L \tag{3.9}$$

$$i_c = i_L + i_o \tag{3.10}$$

$$C * \frac{dv_c}{dt} = i_L + \frac{V_o}{R} \tag{3.11}$$

$$\frac{dV_c}{dt} = \frac{i_L}{C} - \frac{V_o}{R * C} \tag{3.12}$$

3.3.3 Averaged State-Space Model

From equations obtained from KVL,

$$\frac{d\bar{i}_L}{dt} = -\frac{(1-\bar{d}) * \bar{V}_c}{L} + \frac{V_{in}}{L} \tag{3.13}$$

From equations obtained from KCL,

$$\frac{d\bar{V}_c}{dt} = \frac{(1-\bar{d}) * \bar{i}_L}{C} - \frac{\bar{V}_c}{R * C} \tag{3.14}$$

3.3.4 Small Signal Analysis

$$\frac{d\widehat{i}_L}{dt} = -\frac{(1-D) * (\widehat{V}_c)}{L} + \frac{(\hat{d}) * (V_c)}{L} + \frac{\widehat{v}_{in}}{L} \tag{3.15}$$

$$\frac{d\widehat{v}_c}{dt} = \frac{(1-D) * (\widehat{i}_L)}{C} - \frac{(\hat{d}) * (I_L)}{C} - \frac{\widehat{V}_c}{R * C} \tag{3.16}$$

Now, the transfer function will be,

$$\frac{\widehat{i}_L(s)}{\widehat{d}(s)} = \frac{(1-D) * R * I_L + V_C * (1 + sRC)}{s^2 RLC + sL + (1-D)^2 * R} \tag{3.17}$$

$$\frac{\widehat{v_c}(s)}{\widehat{i_L}(s)} = \frac{(1-D)*V_C - (sI_L L)}{(sRC+1)*V_C + (1-D)*R} \tag{3.18}$$

3.3.5 Design Calculations

Duty Cycle(D):
Peak of input AC voltage:

$$V_{in}(pk) = \sqrt{2} * V_{rms} = 325 \text{ V} \tag{3.19}$$

Now, Duty ratio is[6, 7],

$$D = 1 - \frac{2 * V_m}{\pi * V_o} = 0.4827 \tag{3.20}$$

So the nominal duty ratio is 48.3 %. The power rating is found using:

$$P_o = \frac{V_o^2}{R} = \frac{400^2}{80} = 2000 \text{ W} \tag{3.21}$$

Calculation of Boost Inductance(L):
Inductor formula is:.[6, 7]

$$L = \frac{V_{in} * D}{\Delta I_L * f_s} \tag{3.22}$$

The Boost inductor is designed according to allowable inductor ripple current percentage. Ripple is generally selected from 20% to 40% average input current[7]. In this work, 40% is considered [4]:

$$I_{in} = Po/V_{in} = 2000/325 = 6.15 \text{ A} \tag{3.23}$$

The allowable ripple current is selected as:

$$\Delta I_L = 0.4 I_{in} = 2.46 \text{ A} \tag{3.24}$$

Substituting the design values: L = 0.99 mH
Therefore, L = 1 mH
Output Capacitor Design Calculation(C):
The capacitor value is calculated using [11]:

$$C = \frac{I_o * D}{\Delta V_o * f_s} \tag{3.25}$$

Assuming the allowable ripple be 1%,
$\Delta V_o = 0.01 \times 400 = 4$ V
Substituting the converter parameters: C = 25 μF
The theoretically obtained capacitor value represents the minimum capacitance required for ripple reduction. However, in practical PFC applications, a much larger

capacitor is selected to minimize low-frequency ripple and improve DC bus stability.

Therefore, C = 2 mF

3.4 PI Controller Design

For getting stable output & making input current good we use a double loop structure also known as a loop PI structure. This structure is comprised of the two following loops [17].

Outer loop makes dc output voltage stable, and it generates a signal which defines how much current is desired.

Inner loop makes sure input current to follow the input voltage, enable maximum power transfer with minimum harmonic generation [17][3]

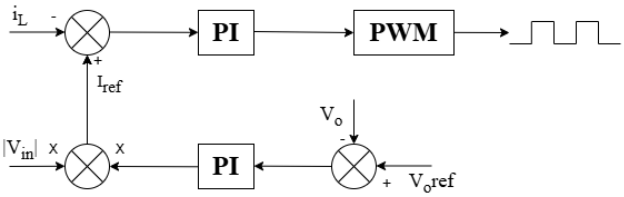

Fig. 3.4: PI control block diagram

Transfer function of PI is written [18] as follows:

$$G_{PI}(s) = K_p + K_i/s \tag{3.26}$$

This means we have, K_p proportional gain and K_i integral gain.

We pick gains so that converter works stablly & it respond quickly & have a small error when it is running steadily.

Ziegler Nichols Method:

This method involves the Routh-Hurwitz (RH) criteria [3] , from which we will obtain the ultimate gain, K_u. By utilizing the auxiliary (even) equation obtained from the RH criteria and substituting $s = j\omega_{cr}$, we can determine the critical crossover frequency, ω_{cr}. From ω_{cr}, we can find the ultimate time period:

$$T_u = \frac{2\pi}{\omega_{cr}} \tag{3.27}$$

Now, for the outer loop, several techniques are utilized determining corresponding K_p and K_i values from the system transfer function.

3.4.1 Voltage loop design

The output voltage is monitored constantly and error calculated in ref. of 400 Volts. Voltage error is fed into PI, that gives current reference [12]:

$$e_v(t) = V_{ref} - V_o \tag{3.28}$$

The reference for current shaping is,

$$I_{ref} = K_{pv} e_v + K_{iv} \int e_v \, dt \tag{3.29}$$

After several tuning iterations, controller gains selected as shown,

Tbl. 3.2: Voltage Loop PI Gains

Gains	Val
K_p	41.48
K_i	214.28

Gain values chosen offer:

- Steady output voltage regulation
- Less overshoot
- Better settling time
- Steady DC bus voltage at 400 V

3.4.2 Current Loop design

This loop is to make the input current to follow input voltage. Error calculated from inductor current & reference current [17]:

$$e_i(t) = I_{ref} - I_L \tag{3.30}$$

Required duty is given by,

$$d(t) = K_{pc} e_i + K_{ic} \int e_i \, dt \tag{3.31}$$

where $d(t)$ represents duty control signal.

The PWM pulses are synthesized, compring controller signal with a high-freq. waveform.[3]

The current loop gains were tuned so as to produce good current tracking, low harmonic distortion, and stable working. Selected gains after tuning,

Tbl. 3.3: Current Loop PI Parameters

Parameter	Val
K_p	0.005
K_i	2

To limit duty ratio into the maximum allowed working region, and to prevent the wind-up of the controller in transients, a saturation block is used and positioned after the current controller.

The applied two-loop PI control structure provides:

- Smooth regulation of 400 V output voltage
- Well-shaped current sine wave
- Lower THD
- Nearly unity power factor

3.5 PR controller design

To enhance the sinusoidal current tracking ability and attenuate the harmonic distortion, PR controller used in current loop. Comparing PI, PR achieves much better tracking for AC sinusoidal signals and reduces the error at the fundamental freq. [17].

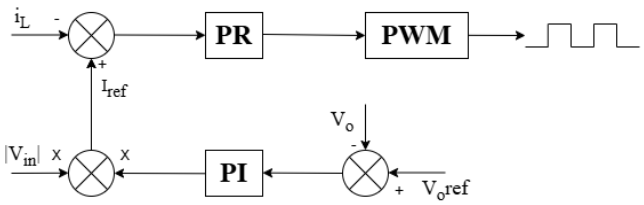

Fig. 3.5: PR block diagram

In the present control scheme, voltage loop uses PI control to get stable output voltage, & inner current loop uses PR controller to shape current.[17].

The actual TF for PR,

$$G_{PR}(s) = K_p + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{3.32}$$

where:

$$K_p = \text{proportional gain} \tag{3.33}$$
$$K_i = \text{resonant gain} \tag{3.34}$$
$$\omega_c = \text{cutoff frequency} \tag{3.35}$$
$$\omega_0 = \text{resonant angular frequency} \tag{3.36}$$

The resonant angular frequency is selected based on the AC supply fundamental frequency [17]and is calculated as:

$$\omega_0 = 2\pi f \tag{3.37}$$

For a 50 Hz supply frequency:

$$\omega_0 = 2\pi \times 50 = 314 \text{ rad/s} \tag{3.38}$$

Thus:

$$\omega_0^2 = (314)^2 = 98696.04 \tag{3.39}$$

The PR controller is implemented in MATLAB/Simulink using the transfer function block. The numerator and denominator coefficients used for implementation are:

$$\text{Numerator Coefficients:} \quad [10 \quad 1 \quad 10 \times 98696.04] \tag{3.40}$$

$$\text{Denominator Coefficients:} \quad [10 \quad 98696.04] \tag{3.41}$$

The implemented PR controller transfer function therefore becomes:

$$G_{PR}(s) = 10 + \frac{10s}{s^2 + 98696.04} \tag{3.42}$$

The controller gains are chosen through a series of tuning attempts in MATLAB/Simulink. The tuning parameters were adjusted to provide:

- Better sinusoidal current tracking
- Less Total Harmonic Distortion (THD)
- Stable converter operation
- Quick dynamic response
- Higher power factor

Tbl. 3.4: PR Controller Parameters

Parameter	**Val**
K_p	10
K_i	10
ω_0	314 rad/s
ω_0^2	98696.04

3.6 Lyapunov-Based Controller Design

Lyapunov stability theory is adopted for the controller design where right Lyapunov function E(t) is proposed such that it decreases all the time. So, the system energy decreases as time goes on. If dE(t)<0 then the system will remain to be stable.

For getting, error of current, $e = i_{ref} - i_L$

If $E(x)$ is the candidate Lyapunov [28] energy function, then for asymptotic stability,

$$E(x) > 0 \quad \text{and} \quad \dot{E}(x) < 0 \quad \forall x \neq 0 \tag{3.43}$$

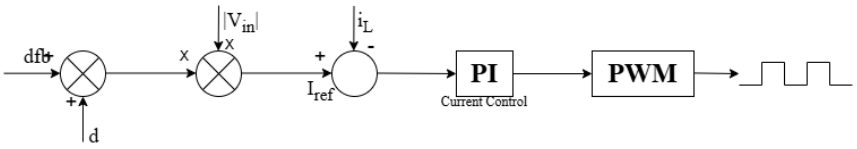

Fig. 3.6: Lyapunov control block diagram

Energy stored in boost can be given as

$$E = \frac{1}{2}Li_l^2 + \frac{1}{2}Cv_c^2 \tag{3.44}$$

$$[E] = \frac{1}{2}\begin{bmatrix} i_L & v_C \end{bmatrix}\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}\begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{3.45}$$

$$[E] = \frac{1}{2}[x]^T P[x] \qquad \text{here } [x] = \begin{bmatrix} i_L & v_C \end{bmatrix}^T \tag{3.46}$$

If

$$e_{i_L} = \bar{i}_L - I_L; \qquad e_{v_c} = \bar{v}_C - v_C; \qquad e_d = \bar{d} - d_{ff} \text{ (or) } \bar{d} - D \tag{3.47}$$

$$\Rightarrow \bar{i}_L = e_{i_L} + I_L; \qquad \bar{v}_c = e_{v_c} + v_c; \qquad d_{fb} = \bar{d} - d_{ff} \Rightarrow \bar{d} = d_{fb} + d_{ff} \tag{3.48}$$

$$\Rightarrow E = \frac{1}{2}Le_{i_L}^2 + \frac{1}{2}Ce_{v_c}^2 \Rightarrow \frac{1}{2}e^T Pe \tag{3.49}$$

For boost converter,

$$v_0 = \frac{v_{in}}{1-d} \tag{3.50}$$

$$\Rightarrow v_0 = \frac{v_{in}}{1-d_{ff}} \tag{3.51}$$

$$\Rightarrow 1 - d_{ff} = \frac{v_{in}}{v_0} \Rightarrow 1 - \frac{v_{in}}{v_0} \tag{3.52}$$

The average model is:

$$L\frac{d\bar{i}_L}{dt} = -(1-\bar{d})\bar{v}_c + v_{in} \tag{3.53}$$

$$C\frac{d\bar{v}_c}{dt} = (1-\bar{d})\bar{i}_L - \frac{\bar{v}_c}{R} \tag{3.54}$$

and

$$v_c = v_0 \tag{3.55}$$

Put LHS $= 0 \quad [\dot{x} = 0]$ steady state or dc value

$$\Rightarrow 0 = -(1 - \bar{d}_{ff})\bar{v}_c + v_{in} \tag{3.56}$$

$$\Rightarrow d_{ff} = 1 - \frac{v_{in}}{v_c} \tag{3.57}$$

$$v_c = \frac{v_{in}}{1 - d_{ff}} \tag{3.58}$$

$$\& \; 0 = (1 - d_{ff})I_L - \frac{v_c}{R} \tag{3.59}$$

$$\Rightarrow \frac{v_c}{R} = I_L(1 - d_{ff}) \tag{3.60}$$

$$\Rightarrow I_L = \frac{v_c}{R(1 - d_{ff})} \tag{3.61}$$

$$\frac{d}{dt}(e_{i_L} + I_L) - \frac{v_{in}}{L} - \left(\frac{1 - d_{ff} - d_{fb}}{L}\right)(e_{v_c} + v_c) \tag{3.62}$$

$$\Rightarrow \quad \frac{de_{i_L}}{dt} + \frac{dI_L}{dt} = \frac{v_{in}}{L} - \frac{1}{L}\left[e_{v_c} - d_{ff}e_{v_c} - d_{fb}e_{v_c} + v_c - d_{ff}v_c - d_{fb}v_c\right] \tag{3.63}$$

$$\Rightarrow \quad \frac{de_{i_L}}{dt} = \frac{v_{in}}{L} - \frac{v_c}{L}(1 - d_{ff} - d_{fb}) - \frac{e_{v_c}}{L}(1 - d_{ff} - d_{fb}) \tag{3.64}$$

During steady state $\frac{dI_L}{dt} = 0$

$$\Rightarrow \frac{de_{i_L}}{dt} = \frac{v_{in}}{L} - \frac{v_c}{L}(1 - d_{ff} - d_{fb}) - \frac{e_{v_c}}{L}(1 - d_{ff} - d_{fb}) \tag{3.65}$$

$$\Rightarrow \frac{de_{i_L}}{dt} = \frac{v_c}{L}d_{fb} - \left(\frac{1 - d_{ff}}{L}\right)e_{v_c} + \frac{d_{fb}}{L}e_{v_c} \tag{3.66}$$

Represent it in standard form,

$$\dot{e} = Ge + (He + h)d_{fb} \tag{3.67}$$

From equation (3.58),

$$1 - d_{ff} = \frac{v_{in}}{v_c} \tag{3.68}$$

$$\Rightarrow \frac{v_{in}}{L} - \frac{v_{in}}{v_c} \cdot \frac{v_c}{L} = \frac{v_{in}}{L} - \frac{v_{in}}{L} \tag{3.69}$$

$$\frac{de_{i_L}}{dt} = -\left(\frac{1 - d_{ff}}{L}\right)e_{v_c} + \frac{d_{fb}}{L}e_{v_c} + \frac{v_c}{L}d_{fb} \tag{3.70}$$

$$G = -\frac{1 - d_{ff}}{L}; \qquad H = \frac{1}{L}; \qquad h = \frac{v_c}{L}$$

Also,

$$\frac{d\bar{v_c}}{dt} = \frac{(1-\bar{d})}{C}\bar{i}_L - \frac{\bar{v}_c}{RC} \tag{3.71}$$

$$\Rightarrow \frac{d}{dt}(e_{v_c} + v_c) = \left(\frac{1 - d_{fb} - d_{ff}}{C}\right)(e_{i_L} + I_L) - \frac{1}{RC}(e_{v_c} + v_c) \tag{3.72}$$

$$\Rightarrow \frac{de_{v_c}}{dt} = \frac{1}{C}\left[e_{i_L} - d_{fb}e_{i_L} + I_L - d_{fb}I_L - d_{ff}I_L\right] - \frac{1}{RC}(e_{v_c}) - \frac{v_c}{RC} \tag{3.73}$$

$$\Rightarrow \frac{de_{v_c}}{dt} = -\frac{1}{RC}e_{v_c} - \frac{v_c}{RC} + \frac{e_{i_L}}{C}\left[1 - d_{fb} - d_{ff}\right] + \frac{I_L}{C}\left[1 - d_{fb} - d_{ff}\right] \tag{3.74}$$

$$\Rightarrow \frac{d}{dt}e_{v_c} = -\frac{1}{RC}e_{v_c} + \left(\frac{1 - d_{ff}}{C}e_{i_L}\right) - \frac{d_{fb}}{C}e_{i_L} - \frac{I_L}{C}d_{fb} \tag{3.75}$$

$$\left\{-\frac{v_c}{RC} + \frac{I_L}{C}(1 - d_{ff}) = -\frac{v_c}{RC} + \frac{V_c}{R(1-d_{ff})}\frac{(1-d_{ff})}{C}\right. \tag{3.76}$$

Using equation,

$$= -\frac{v_c}{RC} + \frac{v_c}{RC} = 0 \tag{3.77}$$

$$\Rightarrow \frac{de_{v_c}}{dt} = -\frac{1}{RC}e_{v_c} + \frac{(1 + d_{ff})}{C}e_{i_L} - \frac{d_{fb}}{C}e_{i_L} - \frac{I_c}{C}d_{fb} \tag{3.78}$$

Here,

$$G = -\frac{1}{RC}e_{v_c} + \left(\frac{1 - d_{ff}}{C}\right)e_{i_L} \tag{3.79}$$

$$H = -\frac{d_{fb}}{C}e_{i_L} \tag{3.80}$$

$$h = -\frac{I_L}{C}d_{fb} = -\frac{1}{C} \times \frac{v_c}{R(1 - d_{ff})} \tag{3.81}$$

The state-space error in matrix form as:

$$\begin{bmatrix} \frac{de_{i_L}}{dt} \\ \frac{de_{v_c}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1+d_{ff})}{L} \\ \frac{1-d_{ff}}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} e_{i_L} \\ e_{v_c} \end{bmatrix} + \begin{bmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} e_{i_L} \\ e_{v_c} \end{bmatrix} d_{fb} + \begin{bmatrix} \frac{v_c}{L} \\ -\frac{v_c}{(1-d_{ff})RC} \end{bmatrix} d_{fb} \tag{3.82}$$

Representing equation in terms of matrix:

$$E = \frac{1}{2}\begin{bmatrix} e_{i_L} & e_{v_c} \end{bmatrix} \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{3.83}$$

$$E = \frac{1}{2}[e]^T[P][e] \tag{3.84}$$

Now find K and d_{fb} by $\dot{E} < 0$:

$$K = \frac{1}{2}\left[[H]^T[P] + [P][H]\right] \tag{3.85}$$

$$\text{\&}\ d_{fb} = -\alpha\left[[e]^T[K][e] + [h]^T[P][e]\right]\ \text{\&}\ \alpha > 0 \tag{3.86}$$

Find K and d_{fb} and implement Lyapunov based controller:

$$K = \frac{1}{2}\left[[H]^T[P] + [P][H]\right] \tag{3.87}$$

$$K = \frac{1}{2}\left\{\begin{bmatrix} 0 & -\frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix}\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} + \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}\begin{bmatrix} 0 & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{bmatrix}\right\} \tag{3.88}$$

$$K = \frac{1}{2}\left\{\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} + \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}\right\} = \frac{1}{2}\begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{3.89}$$

The resulting feedback control law becomes:

$$\boldsymbol{d_{fb} = -\alpha\left[V_C * e_{i_L} - \frac{V_c * e_{v_c}}{(1 - d_{ff})R}\right]} \tag{3.90}$$

In this controller strategy, at any time the controller determines the duty cycle ratio dependent on the states of the converters and the error at that time. The reference for the input current is thus followed, while maintaining the output voltage steady. Lyapunov controlled Boost PFC converter offers:

- Enhanced nonlinear stability
- Fast dynamic performance
- Less overshoot
- Better disturbance rejection
- Enhanced current tracking capability
- Lower harmonic distortion

Compared to the typical PI and PR controllers, the Lyapunov controller possesses better stability under nonlinear dynamics of the converter and different operating conditions[28].

3.7 Simulation Results

3.7.1 Boost PFC with PI control

Input voltage & current

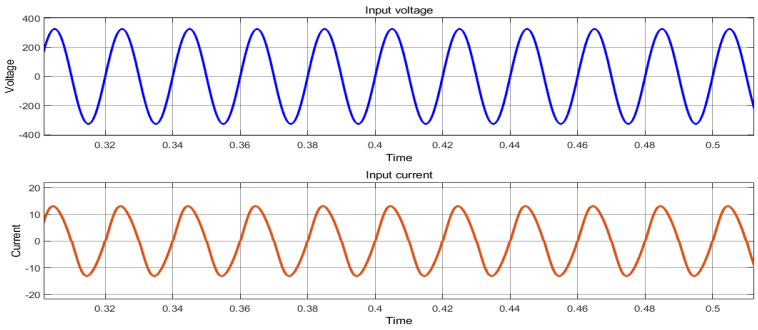

Fig. 3.7: Input voltage & current of Boost PFC

Output voltage

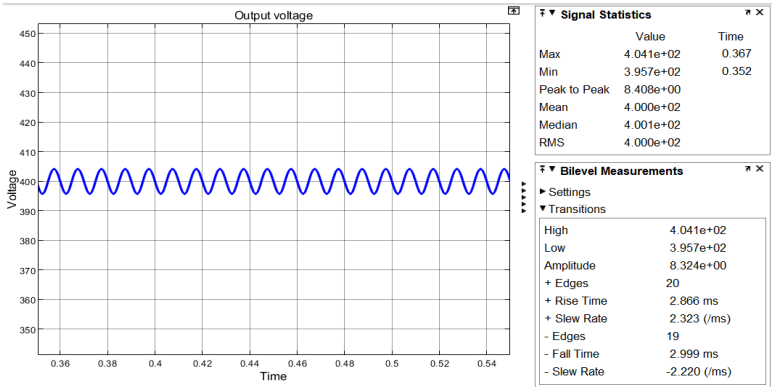

Fig. 3.8: Output voltage of Boost PFC

Load Current

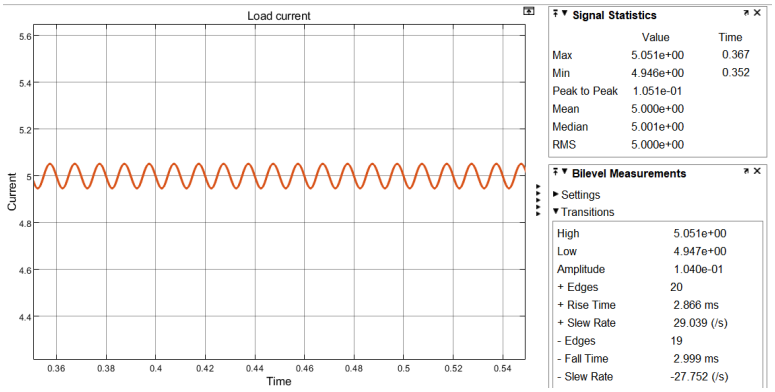

Fig. 3.9: Load current of Boost PFC

Total Harmonic Distortion

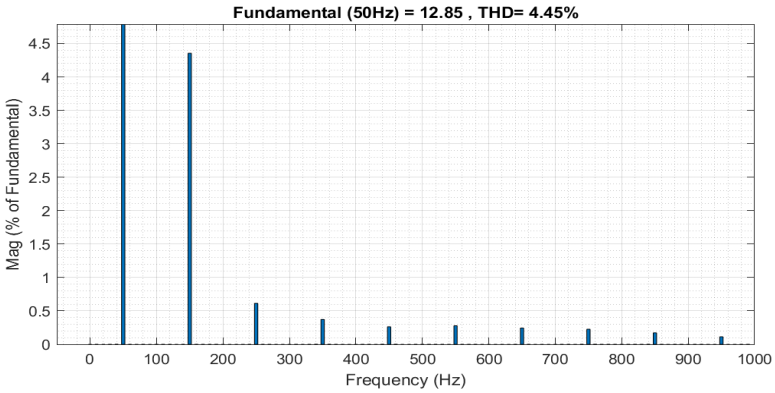

Fig. 3.10: THD analysis

THD = 4.45% and Power factor = 0.99

3.7.2 Boost PFC with PR control

Input voltage & current

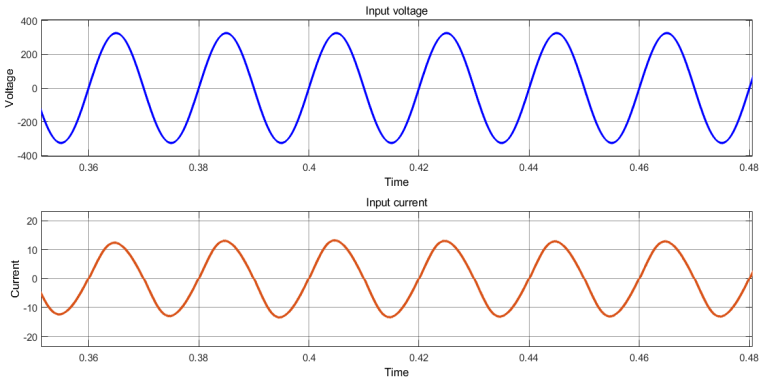

Fig. 3.11: Input voltage & Input current of Boost PFC

Output voltage

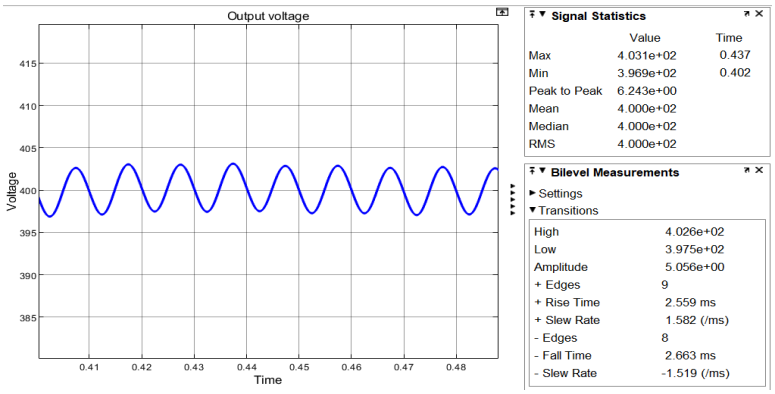

Fig. 3.12: Output voltage of Boost PFC

Load Current

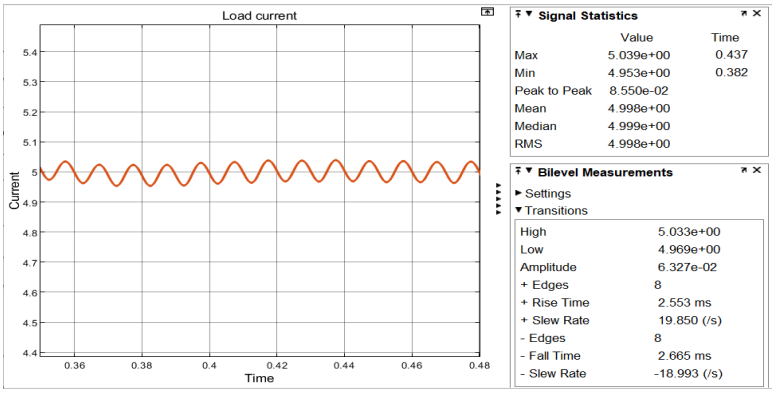

Fig. 3.13: Load current of Boost PFC

Total Harmonic Distortion

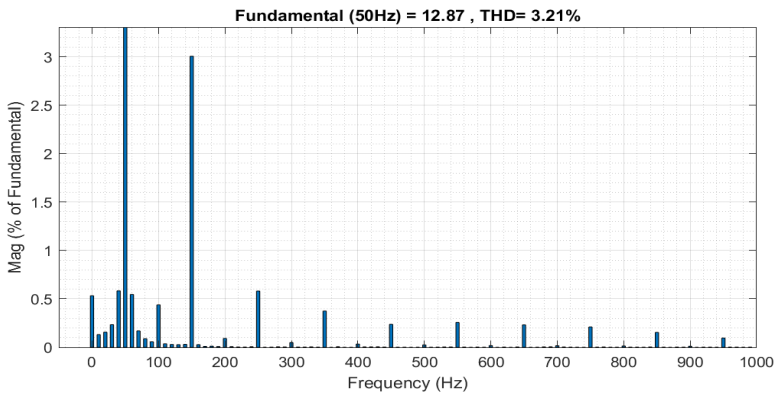

Fig. 3.14: THD analysis, THD = 3.21% and Power factor = 0.99

3.7.3 Boost PFC with Lyapunov control

Input voltage & current

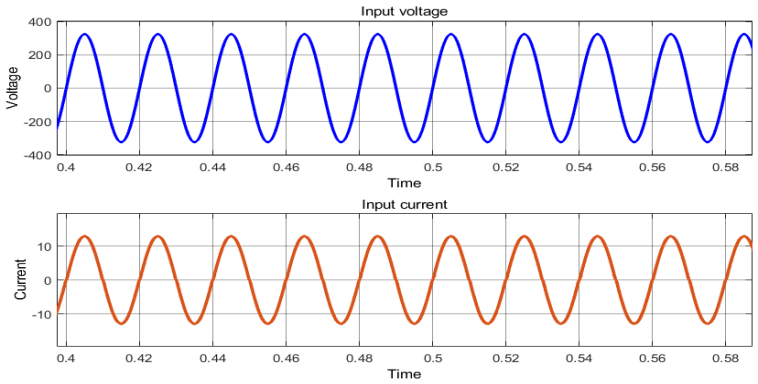

Fig. 3.15: Input voltage and current of Boost PFC

Output voltage

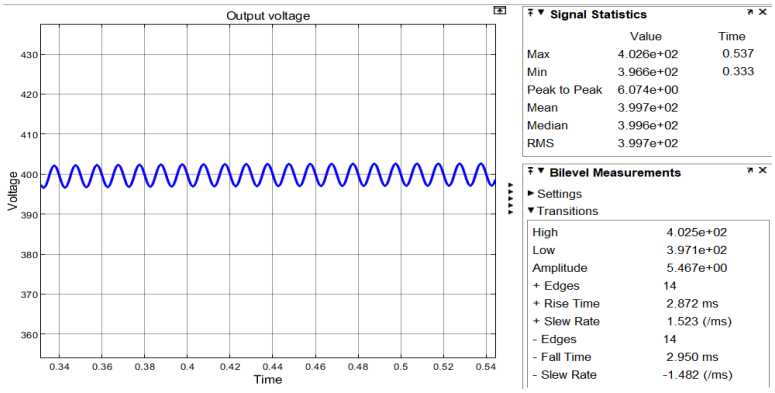

Fig. 3.16: Output voltage of Boost PFC

Load Current

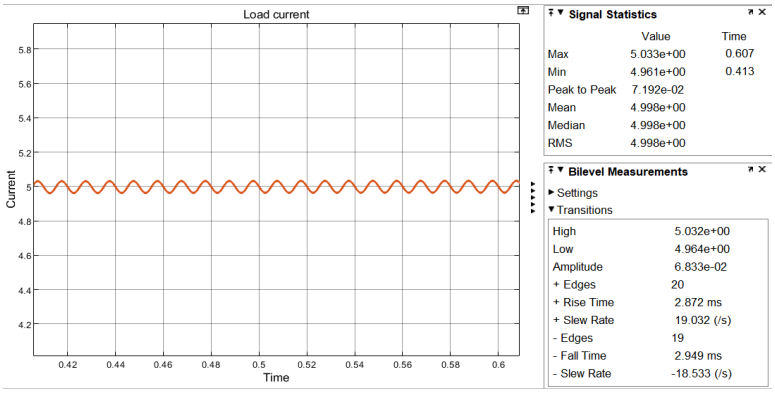

Fig. 3.17: Load current of Boost PFC

Total Harmonic Distortion

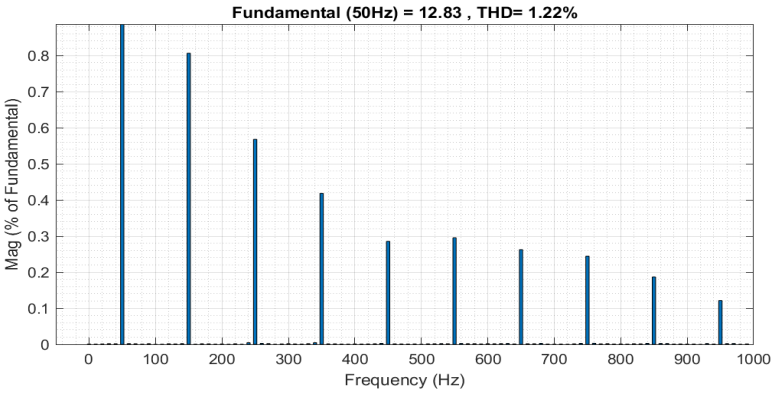

Fig. 3.18: THD analysis

THD = 1.22% and Power factor = 0.999

3.8 Conclusion

From the observation of the simulations and the results it is clearly visible that Lyapaunov control provides better transient response and also less THD, therefore the power factor is better with lyapunov control.

CHAPTER 4

INTERLEAVED BOOST PFC CONVERTER

4.1 Introduction

Regarding the increasing demand of high power of the modern EV charging systems, the traditional single phase Boost PFC converter is becoming restricted because of its high input current ripple, which caused a higher stress on the individual components (thermal and conduction loss).

This has multiple converter legs with different phase shifted control signals. Due to the fact that different legs are operating at out of phase with each other, the input current ripple is cancelled among them which gives better input current quality and also the EMI could be reduced to some extent. Besides that, the current sharing among each converter leg could also greatly reduce the stress on individual components.

Here, 2 phase operating PFC for EV charging system is proposed. Phase difference between legs is 180°. A regulation of DC output voltage, lower harmonics for this PFC is analyzed[19] [20].

The advantage using interleaved Boost PFC converter:

- Reduced current ripple
- Better thermal distribution
- High power capability
- Smaller filter size
- Higher efficiency

In this thesis, the two kinds of control methods- PI and PR control methods are utilized for this PFC.

4.2 Converter Topology and Operation

2 legs are connected in parallel & switched based on time shifted signals to realize the operation. This paper, simulates a 2-phase PFC to achieve the improved input current quality, reduce ripple current and increase converter performance for EV charging application.

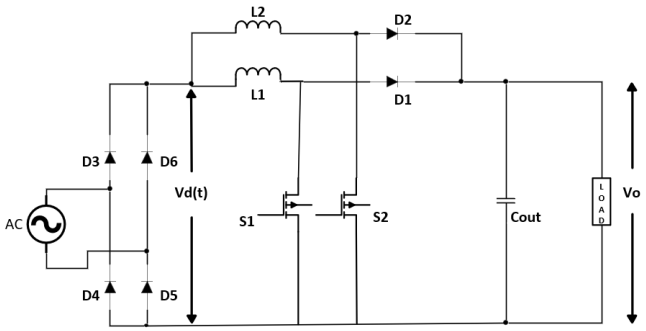

Fig. 4.1: Interleaved Boost PFC Circuit Diagram

The system has a DBR, two boost inductors, two power semiconductor switches, two diodes, output capacitor & a load. Voltage input rectified with DBR, then fed to the converter as input.[19]

The performance indices for PFC is below 4.1

Tbl. 4.1: Specs of Interleaved Boost PFC

Configuration	**Symbol**	**Val**
Input Voltage	V_{in}	230 V (rms)
Output Voltage	V_o	400 V
Power	P_o	2 kW
Load Resistance	R	80 Ω
Inductor per Phase	L_1, L_2	1 mH
Output Capacitance	C	5 mF
Switching Frequency	f_s	25 kHz
Phase Shift	Φ	180°

Both phases of converter were switched with 180 phase shift between gate pulses in the topology described. This phased shifted operation cancels a portion of the input inductor current ripple which greatly reduces it in i/p side.

This operation helps input current share equally in each half of two converter phases which reduces individual stress to semiconductor devices and passive components, decreasing power devices thermal effect. As a result, the efficiency of the converter has been largely increased.

At switch ON phase, inductor draws energy. When the switch turns OFF,inductor delivers energy to load through diode[19]

The converter has lower input current ripple, higher pf & lower harmonics as a result of ripple cancellation from interleaving.

4.3 Mathematical modelling and Design

Two boost converters are switched in 180 phase shift in this topology. Ripple current is partly cancelled by using 180 phase shifted switching. Operation of converter is explained.

4.3.1 Mode 1: Both Switches ON

Switches simultaneously ON. Inductors stores energy this phase. Current rises linearly. As no current is diverted to diodes in this instant load is fed from output capacitor.

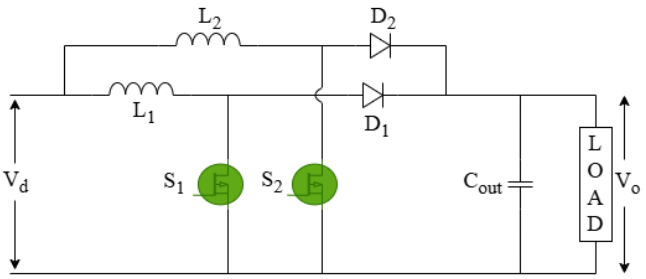

Fig. 4.2: Interleaved Boost PFC Circuit for Mode 1

Voltage in inductors is:

$$V_{L_1} = V_{L_2} = V_{in}$$

Applying Kirchhoff's Voltage Law (KVL):

$$L\frac{di_{L_1}}{dt} = L\frac{di_{L_2}}{dt} = V_{in} \tag{4.1}$$

Thus:

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{in}}{L} \tag{4.2}$$

The capacitor current equation during this interval becomes:

$$\frac{dV_o}{dt} = -\frac{V_o}{RC} \tag{4.3}$$

4.3.2 Mode 2 & 3: One Switch ON and One Switch OFF

During this interval, one converter phase stores while another transfers energy to output. The phases is operated alternatively.

Inductor voltages are expressed as:

$$V_{L1} = V_{in} \tag{4.4}$$

$$V_{L2} = V_{in} - V_o \tag{4.5}$$

Applying KVL:

$$L\frac{di_{L_1}}{dt} = V_{in} \tag{4.6}$$

$$L\frac{di_{L_2}}{dt} = V_{in} - V_o \tag{4.7}$$

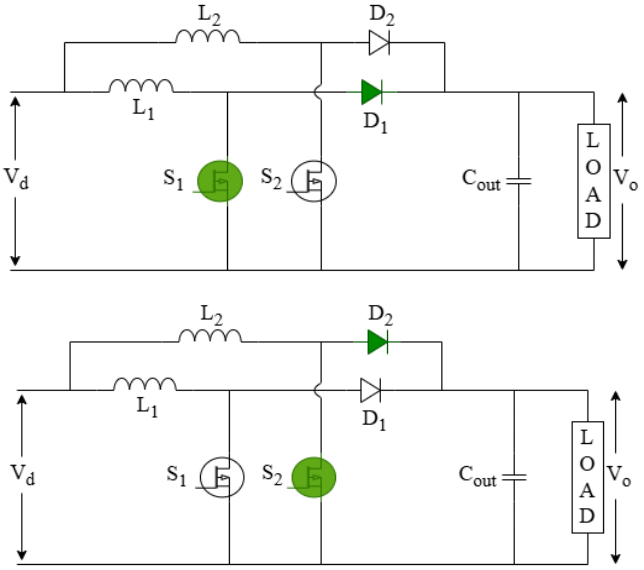

Fig. 4.3: Circuit for Mode 2 & 3

The capacitor current equation becomes:

$$C\frac{dV_o}{dt} = i_{L_2} - \frac{V_o}{R} \tag{4.8}$$

At next half cycle,switching states are reversed because of 180°phase.

This mode is responsible for the ripple cancellation effect in the interleaved converter and significantly reduces the overall input current ripple.

4.3.3 Mode 4: Both Switches OFF

During this interval, both switches are turned OFF and inductors delivers energy to output through diode. The inductor currents decrease while supplying.

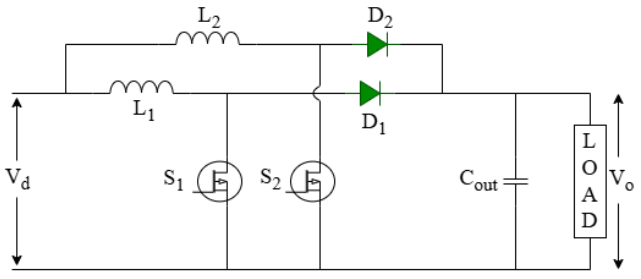

Fig. 4.4: Interleaved Boost PFC Circuit for Mode 4

Inductors voltage:

$$V_{L_1} = V_{L_2} = V_{in} - V_o \tag{4.9}$$

Applying KVL:

$$L\frac{di_{L1}}{dt} = L\frac{di_{L2}}{dt} = V_{in} - V_o \tag{4.10}$$

Thus:

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{V_{in} - V_o}{L} \tag{4.11}$$

The capacitor current equation becomes:

$$C\frac{dv_o}{dt} = i_{L1} + i_{L2} - \frac{v_o}{R} \tag{4.12}$$

Duty cycle is given by[19, 22]:

$$V_o = \frac{V_{in}}{1 - D} \tag{4.13}$$

D is duty ratio.

4.3.4 Avg State-Space Model

This model of interleaved Boost converter as follows,
Averaged inductor current equation is expressed as:

$$L\frac{di_L}{dt} = V_{in} - (1 - D) \tag{4.14}$$

Similarly, the averaged capacitor voltage equation becomes[19]:

$$C\frac{dv_o}{dt} = (1 - D)(i_{L1} + i_{L2}) - \frac{V_o}{R} \tag{4.15}$$

The corresponding averaged state-space representation is therefore given by:

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{2(1-D)}{C} & -\frac{1}{RC} \end{bmatrix}\begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} \tag{4.16}$$

The averaged model represents the large-signal dynamics & is useful to design controller for stability.

4.3.5 Small Signal Analysis

For controller design and transient analysis, using perturbations & linearisation, converter variables are represented as[19]:

$$i_L = I_L + \hat{i}_L \tag{4.17}$$

$$v_o = V_o + \hat{v}_o \tag{4.18}$$

$$d = D + \hat{d} \tag{4.19}$$

where:

- I_L, V_o and D represent steady-state quantities
- $\hat{i}_L$, $\hat{v}_o$ and $\hat{d}$ represent small perturbations.

Inductor current equation becomes:

$$\frac{d\hat{i}_L}{dt} = -(1-D)\hat{v}_o + V_o\hat{d}L \tag{4.20}$$

Similarly, the capacitor voltage equation becomes:

$$C\frac{d\hat{v}_o}{dt} = 2(1-D)\hat{i}_L - 2I_L\hat{d} - \frac{\hat{v}_o}{R} \tag{4.21}$$

4.3.6 Design Calculations

Duty Cycle(D):
Peak of input AC voltage:

$$V_{in}(pk) = \sqrt{2} * V_{rms} = 325 \text{ V} \tag{4.22}$$

Now, Duty ratio is[6, 7],

$$D = 1 - \frac{2 * V_m}{\pi * V_o} = 0.4827 \tag{4.23}$$

So the nominal duty ratio is 48.3 %. The power rating is found using:

$$P_o = \frac{V_o^2}{R} = \frac{400^2}{80} = 2000 \text{ W} \tag{4.24}$$

Calculation of Boost Inductance(L):
The output power of the converter is:

$$P_o = \frac{400^2}{80} = 2000 \text{ W}$$

The average input current is:

$$I_{in} = \frac{2000}{325} = 6.15 \text{ A}$$

Since two phases share the current equally:

$$I_{L1} = I_{L2} = \frac{6.15}{2} = 3.075 \text{ A}$$

Assuming ripple current of 40%:

$$\Delta I_L = 0.4 \times 3.075 = 1.23 \text{ A}$$

The switching period is:

$$T_s = \frac{1}{25 \times 10^3} = 40 \ \mu s$$

The inductance value is calculated using:

$$L = \frac{V_{in} D T_s}{\Delta I_L} \tag{4.25}$$

Substituting the values:

$$L = \frac{325 \times 0.1875 \times 40 \times 10^{-6}}{1.23}$$

Thus: L≈ 1.98 mH

For practical implementation: L_1=L_2=1 mH

Output Capacitor Design Calculation(C):

The capacitor value is calculated using:

$$C = \frac{I_o * D}{\Delta V_o * f_s} \tag{4.26}$$

Assuming the allowable ripple is 1% . $\Delta V_o = 0.01 \times 400 = 4$ V

Substituting the converter parameters: C = 25 μF

The theoretically obtained capacitor value represents the minimum capacitance required for ripple reduction. However, in practical PFC applications, a much larger capacitor is selected to minimize low-frequency ripple and improve DC bus stability[19].

Therefore, the output capacitor value is selected as, C = 2 mF

4.4 PI Controller Design

For getting stable output & making input current good we use a double loop structure also known as a loop PI structure. This structure is comprised of the two following loops [17].

Outer loop makes dc output voltage stable, and it generates a signal which defines how much current is desired.

Inner loop makes sure input current to follow the input voltage, enable maximum power transfer with minimum harmonic generation [17][3]

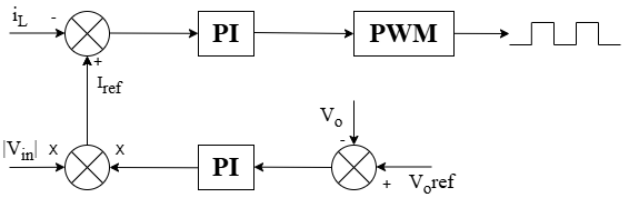

Fig. 4.5: PI control block diagram

Transfer function of PI is written [18] as follows:

$$G_{PI}(s) = K_p + K_i/s \tag{4.27}$$

This means we have, K_p proportional gain and K_i integral gain.

We pick gains so that converter works stablly & it respond quickly & have a small error when it is running steadily.

Ziegler Nichols Method:

This method involves the Routh-Hurwitz (RH) criteria [3] , from which we will obtain the ultimate gain, K_u. By utilizing the auxiliary (even) equation obtained from the RH criteria and substituting $s = j\omega_{cr}$, we can determine the critical crossover frequency, ω_{cr}. From ω_{cr}, we can find the ultimate time period:

$$T_u = \frac{2\pi}{\omega_{cr}} \tag{4.28}$$

Now, for the outer loop, several techniques are utilized determining corresponding K_p and K_i values from the system transfer function.

4.4.1 Voltage loop design

The output voltage is monitored constantly and error calculated in ref. of 400 Volts. Voltage error is fed into PI, that gives current reference [12]:

$$e_v(t) = V_{ref} - V_o \tag{4.29}$$

The reference for current shaping is,

$$I_{ref} = K_{pv}e_v + K_{iv}\int e_v\, dt \tag{4.30}$$

After several tuning iterations, controller gains selected as shown,

Tbl. 4.2: Voltage Loop PI Gains

Gains	**Val**
K_p	0.05
K_i	0.2

Gain values chosen offer:

- Steady output voltage regulation
- Less overshoot
- Better settling time
- Steady DC bus voltage at 400 V

4.4.2 Current Loop design

This loop is to make the input current to follow input voltage. Error calculated from inductor current & reference current [17]:

$$e_i(t) = I_{ref} - I_L \tag{4.31}$$

Required duty is given by,

$$d(t) = K_{pc} e_i + K_{ic} \int e_i \, dt \tag{4.32}$$

where $d(t)$ represents duty control signal.

The PWM pulses are synthesized, comparing controller signal with a high-freq. waveform.[3]

The current loop gains were tuned so as to produce good current tracking, low harmonic distortion, and stable working. Selected gains after tuning,

Tbl. 4.3: Current Loop PI Parameters

Gain	**Val**
K_p	1.3
K_i	85

To limit duty ratio into the maximum allowed working region, and to prevent the wind-up of the controller in transients, a saturation block is used and positioned after the current controller.

The applied two-loop PI control structure provides:

- Smooth regulation of 400 V output voltage
- Well-shaped current sine wave
- Lower THD
- Nearly unity power factor

4.5 PR controller design

To enhance the sinusoidal current tracking ability and attenuate the harmonic distortion, PR controller used in current loop. Comparing PI, PR achieves much better tracking for AC sinusoidal signals and reduces the error at the fundamental freq. [17].

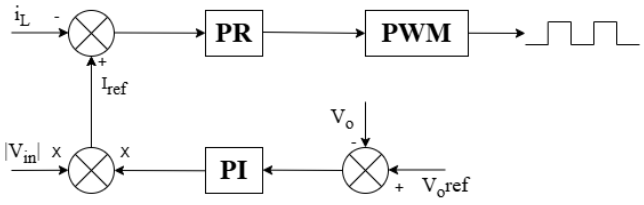

Fig. 4.6: PR block diagram

In the present control scheme, voltage loop uses PI control to get stable output voltage, & inner current loop uses PR controller to shape current.[17].

The actual TF for PR,

$$G_{PR}(s) = K_p + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{4.33}$$

where:

$$K_p = \text{proportional gain} \tag{4.34}$$
$$K_i = \text{resonant gain} \tag{4.35}$$
$$\omega_c = \text{cutoff frequency} \tag{4.36}$$
$$\omega_0 = \text{resonant angular frequency} \tag{4.37}$$

The resonant angular frequency is selected based on the AC supply fundamental frequency [17]and is calculated as:

$$\omega_0 = 2\pi f \tag{4.38}$$

For a 50 Hz supply frequency:

$$\omega_0 = 2\pi \times 50 = 314 \text{ rad/s} \tag{4.39}$$

Thus:

$$\omega_0^2 = (314)^2 = 98696.04 \tag{4.40}$$

The PR controller is implemented in MATLAB/Simulink using the transfer function block. The numerator and denominator coefficients used for implementation are:

$$\text{Numerator Coefficients:} \quad [10 \quad 1 \quad 10 \times 98696.04] \tag{4.41}$$
$$\text{Denominator Coefficients:} \quad [10 \quad 98696.04] \tag{4.42}$$

The implemented PR controller transfer function therefore becomes:

$$G_{PR}(s) = 10 + \frac{10s}{s^2 + 98696.04} \tag{4.43}$$

Tbl. 4.4: PR Controller Parameters

Parameters	**Val**
K_p	10
K_i	10
ω_0	314 rad/s
ω_0^2	98696.04

The controller gains are chosen through a series of tuning attempts in MATLAB/Simulink. The tuning parameters were adjusted to provide:

- Better sinusoidal current tracking
- Less Total Harmonic Distortion (THD)

- Stable converter operation
- Quick dynamic response
- Higher power factor

4.6 Simulation Results

4.6.1 Interleaved Boost PFC with PI control

Input voltage & current

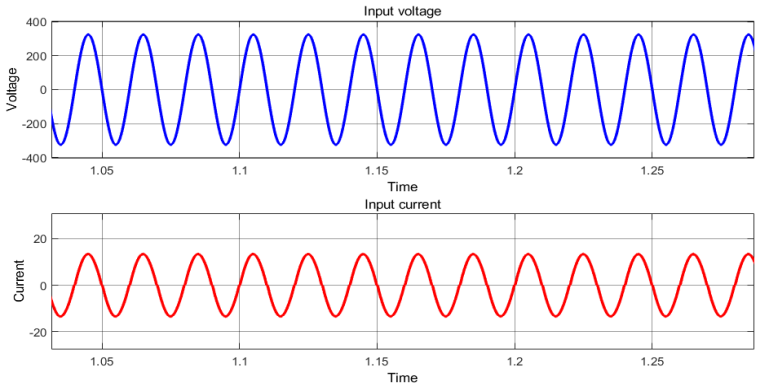

Fig. 4.7: Input voltage & current waveform

Inductor Current

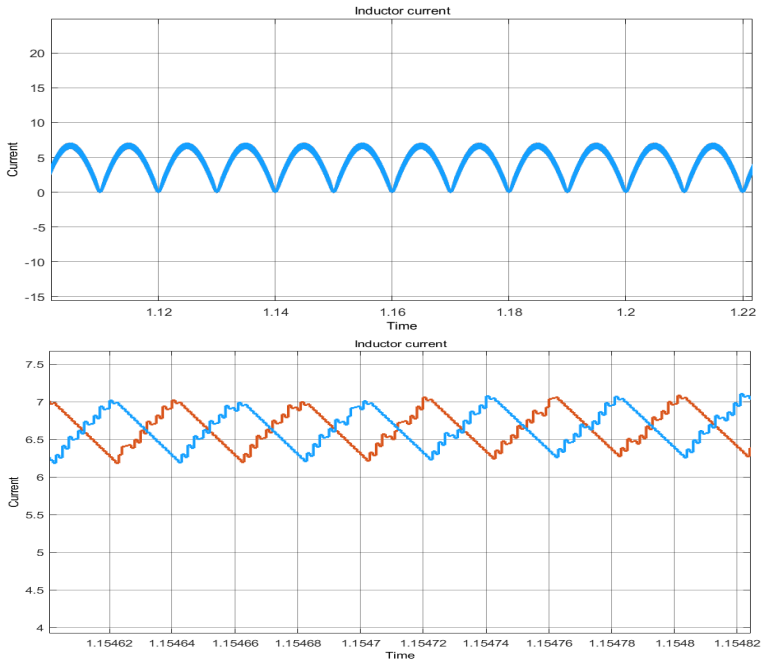

Fig. 4.8: Inductor current waveform

Output voltage

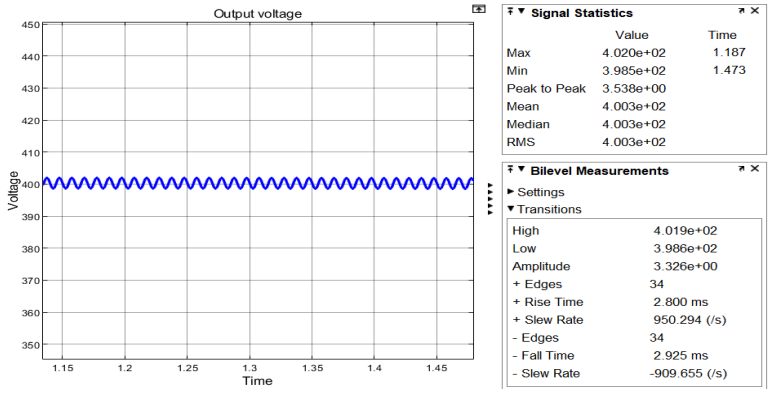

Fig. 4.9: Output voltage waveform

Load Current

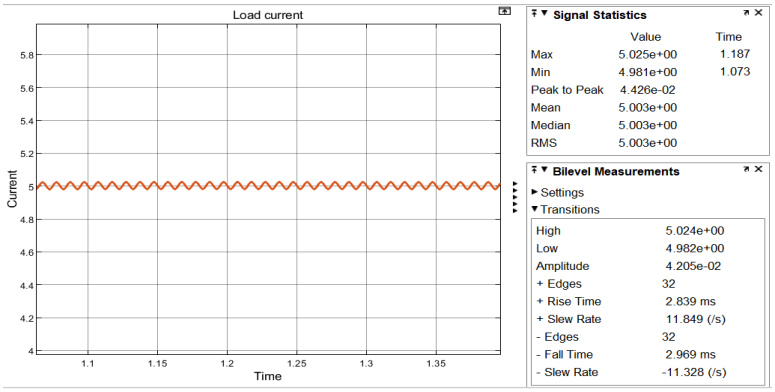

Fig. 4.10: Load current waveform

Total Harmonic Distortion

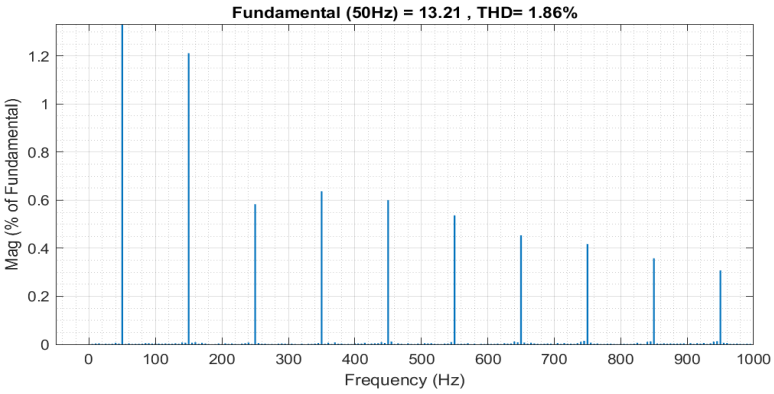

Fig. 4.11: THD analysis

THD = 1.8% and Power factor = 0.999

4.6.2 Interleaved Boost PFC with PR control

Input voltage & current

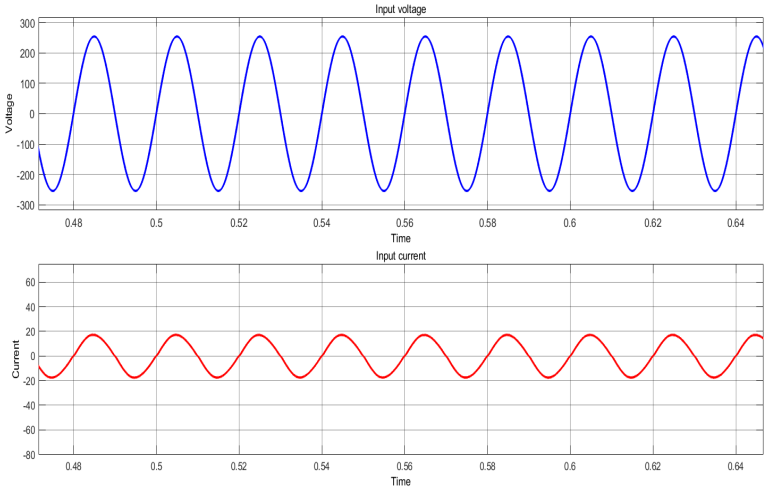

Fig. 4.12: Input voltage & current waveform

Inductor Current

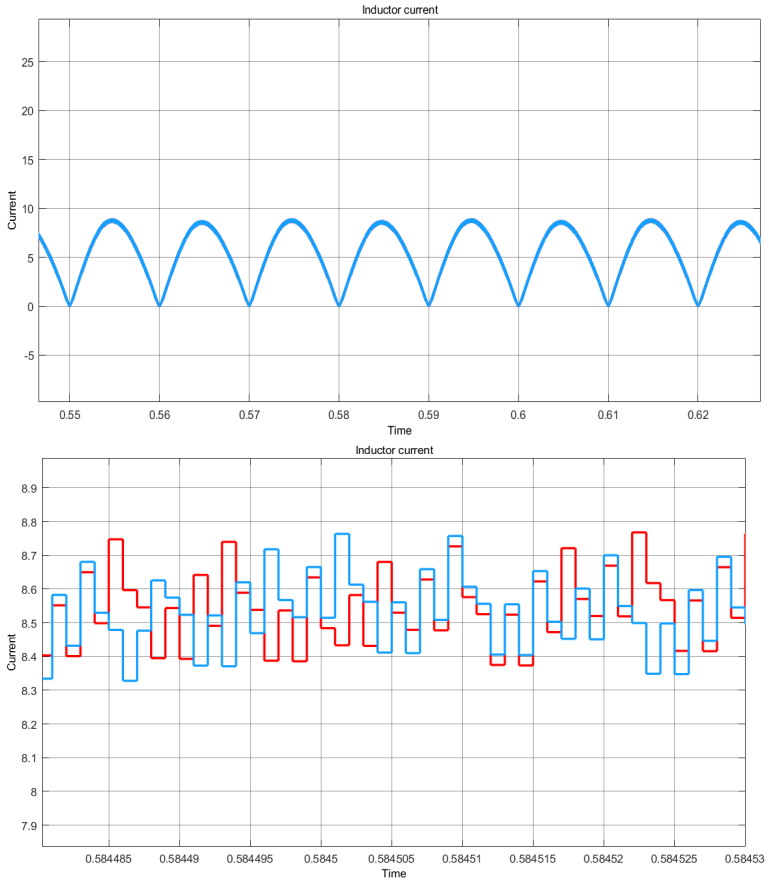

Fig. 4.13: Inductor current waveform

Output voltage

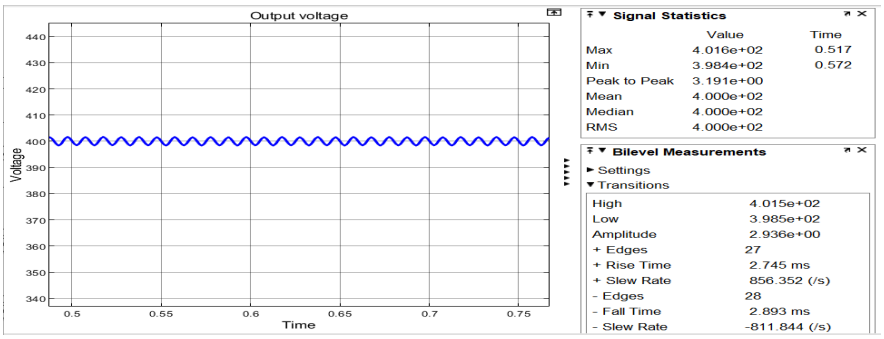

Fig. 4.14: Output voltage waveform

Load Current

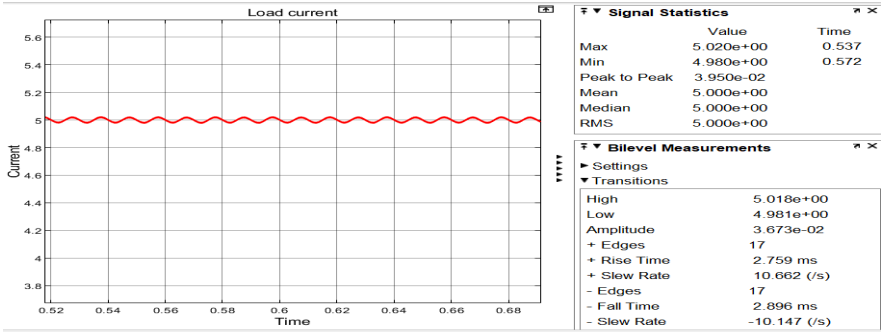

Fig. 4.15: Load current waveform

Total Harmonic Distortion

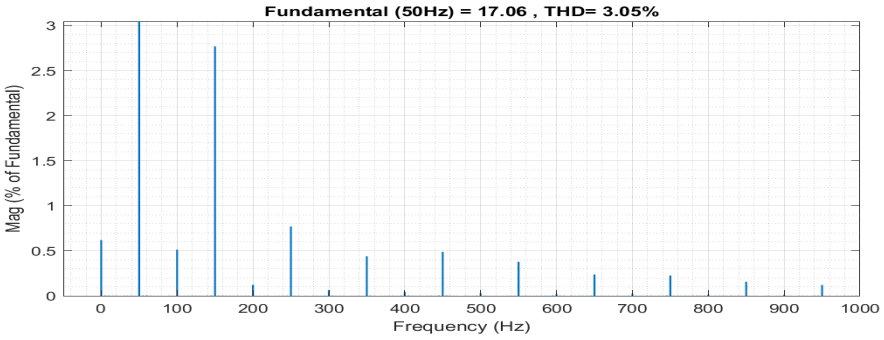

Fig. 4.16: THD analysis

THD = 3% and Power factor = 0.99

4.7 Conclusion

As result shows this PFC has low ripple in current and achieves a better power than the conventional boost PFC as it has very low THD

CHAPTER 5

SINGLE-STAGE FLYBACK PFC CONVERTER

5.1 Introduction

Thic PFC is considered as good for the low and mid rated EV chargers because they have a smaller structure, low component count and more power conversion capability compared to two-stage structures. Instead of separating into two stages, a single stage converter is considered where both functions are combined in a single power conversion stage, and thus reduced the size, cost and the control complexity of the overall converter.[13] [14]

There are many topologies of the single stage converters, among them Flyback converter is highly preferred as its circuit is simple and it also provides the necessary transformer isolation, and better for low rated application. In Flyback converter, [23, 24] stores energy in Transformer magnetizing inductance while charging period, & the stored energy delivered for output when discharging period.[13] [14]

Some advantages of the Flyback converter are as below:

- Electrical Isolation
- Low Component Count
- Compact Structure
- Simple Control
- Low cost of converter design

However the Flyback converter has a problem in its input current as it is discontinuous and higher ripple of current at higher power is also a problem. Thus the controller should be designed properly and the converter parameters are also important to have a better output of converter and also power quality.

5.2 Converter Topology and Operation

This is the only step Flyback PFC converter which performs two actions, namely, to improve power factor and to convert DC-DC power all in one stage.

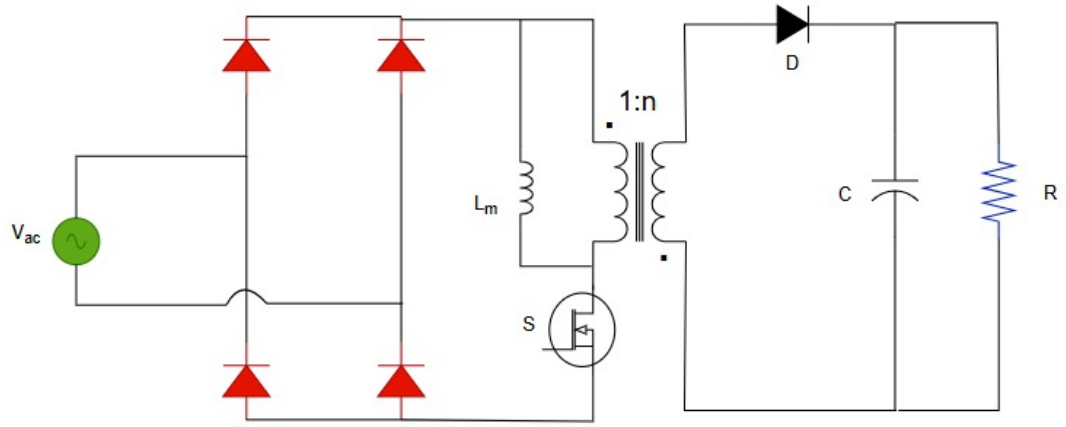

Fig. 5.1: Flyback Converter Circuit

The components present in the circuit are diode bridge rectifier, Flyback transformer, power semiconductor switch, output diode, output capacitor and output load resistor.

Initially, AC voltage is applied to DBR. Flyback transformer serves the purpose of isolation and storing the energy and then converting it.The specification for designed single stage Flyback PFC converter are as in 5.1 Flyback converter stage is coupled with output voltage.

The components present in single stage Flyback PFC converter are diode bridge rectifier, Flyback transformer, power semiconductor switch, output diode, output capacitor and output load resistor.

Tbl. 5.1: Design Specifications of Single-Stage Flyback PFC

Configuration	**Symbol**	**Val**
Input voltage	V_{in}	230 V (rms)
Output voltage	V_o	48 V
Power	P_o	100 W
Load Resistance	R	23 Ω
Magnetizing Inductance	L_m	900 μH
Output Capacitor	C_o	4000 μF
Switching Frequency	f_s	50 kHz

- Switch ON Condition

When you close the power switch at the time which the power switch should be closed the power switch is closed. Then the rectifier produces a voltage to section of Flyback Transformer. A section of Flyback Transformer stores energy and while this section stores energy the current flowing in it grows and grows linearly.

The secondary diode of the Flyback Transformer blocks any current during this period of time. Therefore no energy is produced on the output side. Now stored energy in the output storage capacitor now drives power to load.

The voltage across a section of the Flyback transformer which stores energy during this period of time is given by:

$$V_{Lm} = V_{in} \tag{5.1}$$

Applying Kirchhoff's Voltage Law (KVL):

$$L_m \frac{di_p}{dt} = V_{in} \tag{5.2}$$

Thus:

$$\frac{di_p}{dt} = \frac{V_{in}}{L_m} \tag{5.3}$$

- Switch OFF Condition

During the OFF interval, Transformer winding polarity reverses. Stored energy in L_{mag}, transferred to other side through output diode. Secondary current flows through o/p capacitor & load resistance.Voltage across magnetizing inductance during this interval is expressed as:

$$V_{Lm} = -\frac{N_p}{N_s} V_o \tag{5.4}$$

Applying KVL:

$$L_m \frac{di_p}{dt} = -\frac{N_p}{N_s} V_o \tag{5.5}$$

Thus:

$$\frac{di_p}{dt} = -\frac{N_p V_o}{N_s L_m} \tag{5.6}$$

where:

- N_p = primary turns
- N_s = secondary turns

voltage conversion ratio for Flyback,

$$V_o = \frac{N_s}{N_p} \frac{D}{1-D} V_{in} \tag{5.7}$$

D = duty ratio

So Flyback converter carries out two tasks at the same time: regulated output voltage; at the same time, one great advantage of this converter is that it can isolate and this capability is not possessed by other converters. Thus, in order to achieve the two tasks, this component can become very small and it comprises only several components.

Now, let's make a comparison between Flyback converter and Boost PFC converter. Some disadvantages exist for Flyback converter, like its input current is discontinuous, higher ripple and so on; it is very sensitive for controller design. The controller design

in Flyback converter is quite critical in order to ensure a well power quality and hence to make this system to be a useful and working system.

5.3 Mathematical Modeling and Design Calculations

For us to know how the converter operates we should make a model of it. It will enable us to select parameters for the converter as well as designing the control circuit. [23].

5.3.1 Mode 1: Switch ON Condition

During this period, rectified voltage is input for primary winding of Flyback Transformer. Energy gets stored in the Transformer L_{mag} while output diode remains reverse biased.

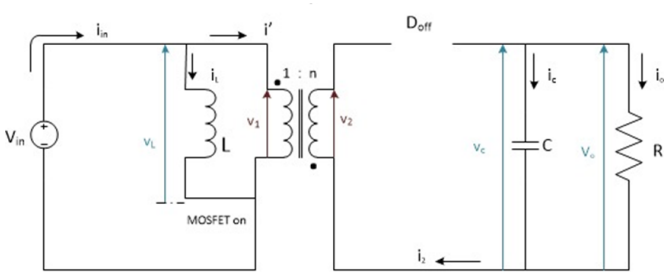

Fig. 5.2: Flyback PFC mode 1 Circuit diagram

Applying Kirchhoff's Voltage Law (KVL):

$$L_m \frac{di_p}{dt} = V_{in} \tag{5.8}$$

Thus:

$$\frac{di_p}{dt} = \frac{V_{in}}{L_m} \tag{5.9}$$

5.3.2 Mode 2: Switch OFF Condition

During the OFF interval, the transformer winding polarity reverses. The energy from L_{mag} is transferred into secondary side through output diode.

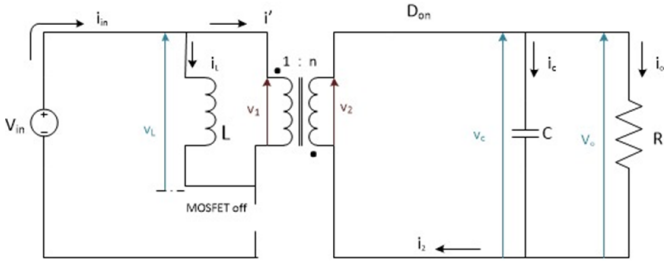

Fig. 5.3: Flyback PFC mode 2 Circuit diagram

Applying KVL:

$$L_m \frac{di_p}{dt} = -\frac{N_p}{N_s} V_o \tag{5.10}$$

Thus:

$$\frac{di_p}{dt} = -\frac{N_p V_o}{N_s L_m} \tag{5.11}$$

5.3.3 Avg State-Space Model

The averaged inductor current equation becomes:

$$L_m \frac{di_p}{dt} = DV_{in} - (1-D)\frac{N_p}{N_s} V_o \tag{5.12}$$

Similarly, the averaged capacitor voltage equation is expressed as:

$$C_o \frac{dv_o}{dt} = (1-D)\frac{N_s}{N_p} i_p - \frac{V_o}{R} \tag{5.13}$$

The corresponding averaged state-space representation is therefore given by:

$$\frac{d}{dt}\begin{bmatrix} i_p \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)N_p}{L_m N_s} \\ \frac{(1-D)N_s}{C_o N_p} & -\frac{1}{RC_o} \end{bmatrix} \begin{bmatrix} i_p \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{D}{L_m} \\ 0 \end{bmatrix} V_{in} \tag{5.14}$$

The averaged model represents behavior & forms basis of controller design and stability analysis.

5.3.4 Small-Signal Modelling

For transient analysis, perturbations & linearisation are performed.
Converter variables are represented as:

$$i_p = I_P + \hat{i}_p v_o = V_o + \hat{v}_o d = D + \hat{d} \tag{5.15}$$

where

- I_P,V_O and D represent steady-state quantities.
- $\hat{i}_p$, $\hat{v}_o$ and $\hat{d}$ represent small perturbations.

Inductor current equation becomes:

$$L_m \frac{d\hat{i}_p}{dt} = -(1-D)\frac{N_p}{N_s}\hat{v}_o + \frac{N_p V_o}{N_s}\hat{d} \tag{5.16}$$

Similarly, the capacitor voltage equation becomes[23]:

$$C_o \frac{d\hat{v}_o}{dt} = (1-D)\frac{N_s}{N_p}\hat{i}_p - \frac{N_s I_P}{N_p}\hat{d} - \frac{\hat{v}_o}{R} \tag{5.17}$$

5.3.5 Design calculations

Duty Ratio Calculation

Maximum inpt AC voltage is calculated using:

$$V_{in(pk)} = \sqrt{2} V_{in(rms)} \tag{5.18}$$

Substituting the input voltage:

$$V_{in(pk)} = \sqrt{2} \times 230 = 325 \text{ V} \tag{5.19}$$

From the transformer specifications used in the MATLAB/Simulink model:

$$\frac{N_s}{N_p} = \frac{72}{325} = 0.221 \tag{5.20}$$

The duty ratio is calculated using:

$$D = \frac{V_o}{V_o + \frac{N_s}{N_p} V_{in}} \tag{5.21}$$

Substituting the converter specifications:

$$D = \frac{48}{48 + 0.221 \times 325} = 0.401 \tag{5.22}$$

Thus: $D = 40.1\%$

Transformer Design Calculation

Flyback relies on specific turns ratio to operate, the turns ratio is derived based on the voltage swing requirements for the Flyback converter, to ensure that they are fulfilled. The Flyback transformer contributes to satisfying these requirements.

The entire Flyback depends on its transformer. It is evident that Transformer is vital for working of converter.

Turns ratio used in the simulation model is:

$$\frac{N_s}{N_p} = 0.221 \tag{5.23}$$

Thus, the approximate transformer turns ratio becomes:

$$N_p : N_s \approx 4.5 : 1 \tag{5.24}$$

The transformer apparent power rating is selected as: $P_{rating} = 100\ VA$

The primary current is calculated as:

$$I_p = \frac{P_o}{V_{in}} = \frac{100}{325} = 0.307 \text{ A} \tag{5.25}$$

Similarly, the secondary current is calculated as:

$$I_s = \frac{P_o}{V_o} = \frac{100}{48} = 2.08 \text{ A} \tag{5.26}$$

Tbl. 5.2: Flyback Transformer Parameters

Specifications	**Val**
Transformer Rating	100 VA
Primary voltage	325 V
Secondary voltage	72 V
Primary Resistance	0.1 Ω
Secondary Resistance	0.02 Ω
Magnetizing Inductance	900 μH
Switching Frequency	50 kHz

Magnetizing Inductance Design
The average input current is calculated as:

$$I_{in} = \frac{100}{325} = 0.307 \text{ A} \tag{5.27}$$

Assuming ripple current of 40%:

$$\Delta I_p = 0.4 \times 0.307 = 0.123 \text{ A} \tag{5.28}$$

The switching period corresponding to 50 kHz is:

$$T_s = \frac{1}{50 \times 10^3} = 20\mu s \tag{5.29}$$

The magnetizing inductance is calculated using:

$$L_m = \frac{V_{in} D T_s}{\Delta I_p} \tag{5.30}$$

Substituting the design values:

$$L_m = \frac{325 \times 0.401 \times 20 \times 10^{-6}}{0.123} \tag{5.31}$$

Thus: $L_m \approx$ 0.85 mH
For practical implementation, the magnetizing inductance is selected as: L_m =900 μH
Output Capacitor Design
The output current is calculated as:

$$I_o = \frac{100}{48} = 2.08 \text{ A} \tag{5.32}$$

Assuming allowable output voltage ripple of 2%:

$$\Delta V_o = 0.02 \times 48 = 0.96 \text{ V} \tag{5.33}$$

The output capacitor is calculated using:

$$C_o = \frac{I_o D}{f_s \Delta V_o} \tag{5.34}$$

Substituting the converter parameters:

$$C_o = \frac{2.08 \times 0.401}{50 \times 10^3 \times 0.96} \tag{5.35}$$

Thus: $C_o \approx 17.4\ \mu F$ However, for improved output voltage stability and reduced low-frequency ripple, the value choose is C_o=4000 μF

5.4 PI Controller Design

For getting stable output & making input current good we use a double loop structure also known as a loop PI structure. This structure is comprised of the two following loops [17].

Outer loop makes dc output voltage stable, and it generates a signal which defines how much current is desired.

Inner loop makes sure input current to follow the input voltage, enable maximum power transfer with minimum harmonic generation [17][3]

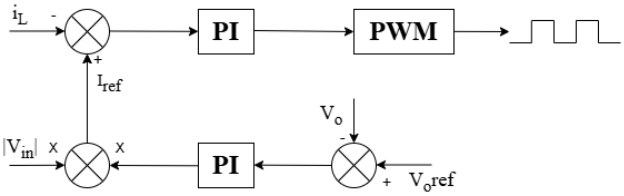

Fig. 5.4: PI control block diagram

Transfer function of PIis written [18] as follows:

$$G_{PI}(s) = K_p + K_i/s \tag{5.36}$$

This means we have, K_p proportional gain and K_i integral gain.

We pick gains so that converter works stablly & it respond quickly & have a small error when it is running steadily.

Ziegler Nichols Method:

This method involves the Routh-Hurwitz (RH) criteria [3] , from which we will obtain the ultimate gain, K_u. By utilizing the auxiliary (even) equation obtained from the RH criteria and substituting $s = j\omega_{cr}$, we can determine the critical crossover frequency, ω_{cr}. From ω_{cr}, we can find the ultimate time period:

$$T_u = \frac{2\pi}{\omega_{cr}} \tag{5.37}$$

Now, for the outer loop, several techniques are utilized determining corresponding K_p and K_i values from the system transfer function.

5.4.1 Voltage loop design

The output voltage is monitored constantly and error calculated in ref. of 400 Volts. Voltage err is fed into PI, that gives current reference [12]:

$$e_v(t) = V_{ref} - V_o \tag{5.38}$$

The ref for current shaping is,

$$I_{ref} = K_{pv} e_v + K_{iv} \int e_v \, dt \tag{5.39}$$

After several tuning iterations, controller gains selected as shown,

Tbl. 5.3: Voltage Loop PI Gains

Gains	**Val**
K_p	0.08
K_i	0.05

Gain values chosen offer:

- Steady output voltage regulation
- Less overshoot
- Better settling time
- Steady DC bus voltage at 400 V

5.4.2 Current Loop design

This loop is to make the input current to follow input voltage. Error calculated from inductor current & ref current [17]:

$$e_i(t) = I_{ref} - I_L \tag{5.40}$$

Required duty is give ny,

$$d(t) = K_{pc} e_i + K_{ic} \int e_i \, dt \tag{5.41}$$

where $d(t)$ represents duty control signal.

The PWM pulses are synthesized, compring controller signal with a high-freq. waveform.[3]

The current loop gains were tuned so as to produce good current tracking, low harmonic distortion, and stable working. Selected gains after tuning,

Tbl. 5.4: Current Loop PI Parameters

Gain	Val
K_p	0.125
K_i	4.5

To limit duty ratio into the maximum allowed working region, and to prevent the wind-up of the controller in transients, a saturation block is used and positioned after the current controller.

The applied two-loop PI control structure provides:

- Smooth regulation of 400 V output voltage
- Well-shaped current sine wave
- Lower THD
- Nearly unity power factor

5.5 Simulation Results

Input voltage & current

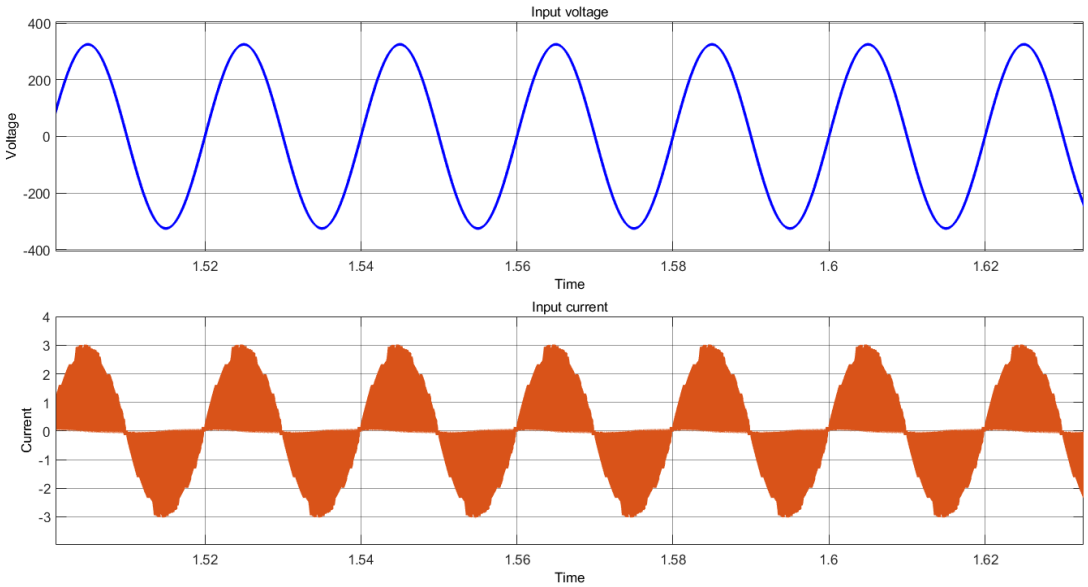

Fig. 5.5: Input voltage & current waveform of Flyback PFC

Transformer input voltage

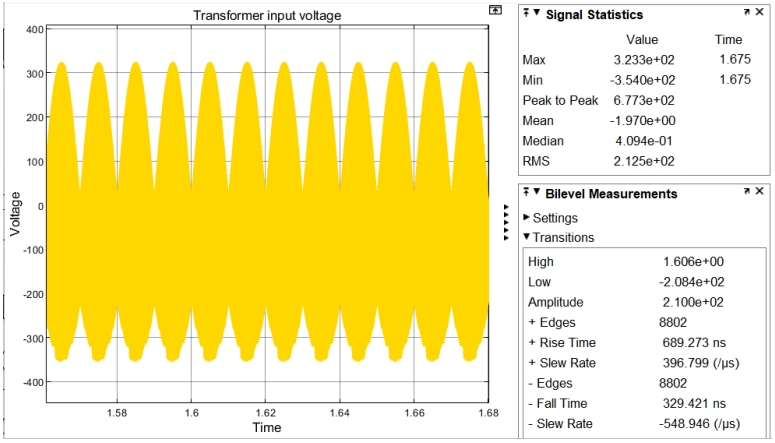

Fig. 5.6: Transformer Input voltage waveform of Flyback PFC

Transformer Input Current

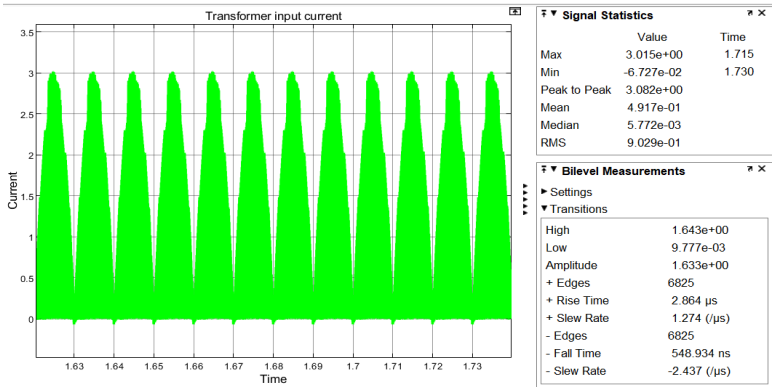

Fig. 5.7: Transformer input current of Flyback PFC

Output Voltage

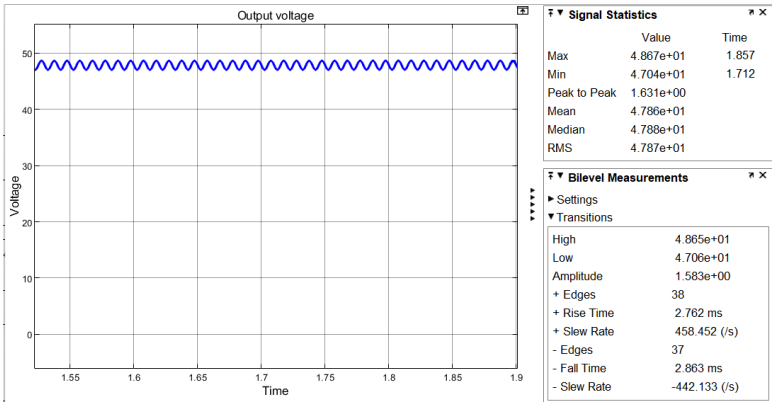

Fig. 5.8: Output voltage of Flyback PFC

Load Current

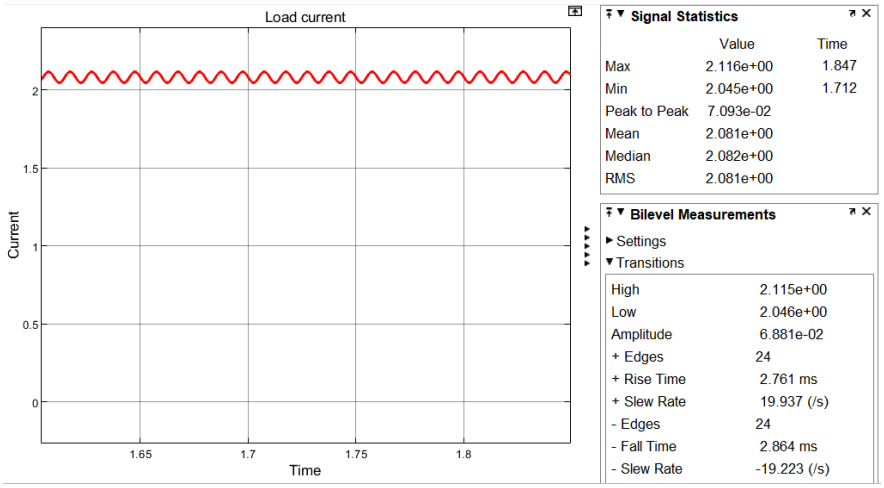

Fig. 5.9: Output current of Flyback PFC

Total Harmonic Distortion

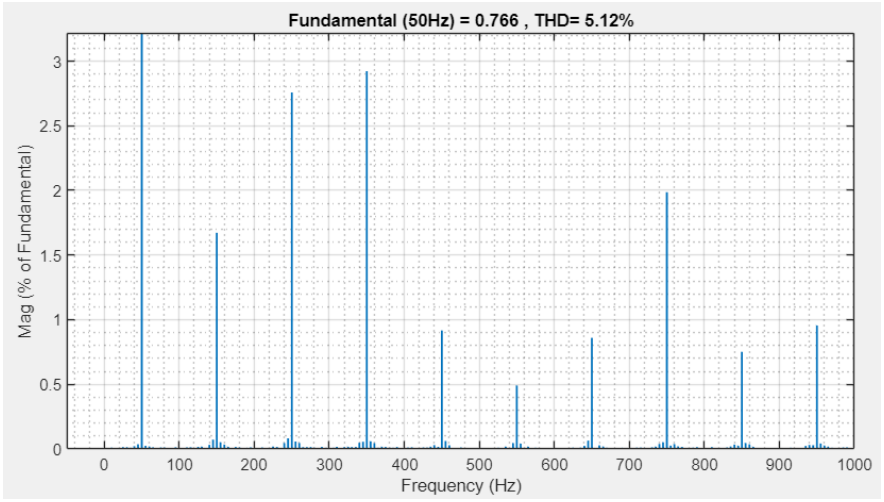

Fig. 5.10: Total Harmonic Distortion analysis of Flyback PFC

THD = 5.12% and Power factor = 0.99

5.6 Conclusion

Thus it is observed that Flyback PFC attains better power factor as it has low THD in DCM mode. It can be only used for low power rated applications

CHAPTER 6

FULL BRIDGE CONVERTER

6.1 Introduction

To achieve power delivery for the rapidly growing demands of high-power EV charging, it is necessary to design highly efficient isolated DC-DC converters capable of changing high to low voltage, regulated dc with acceptable efficiency & reliability. Out of several topologies of isolated converters, FBC is better for mid to high rated range because it has higher power handling, better transformer utilization, suitable for high frequency switching[1].

FBC comprises four power semiconductor switches configured in a bridge, a high-freq isolation Transformer, rectification stages, & output filter components. FBC transforms input dc to high-freq ac using bridge inverter stage which is transferred through transformer and is rectified to the desired regulated DC voltage. [25] The Full bridge offers superior transformer utilization and reduced semiconductor device voltage stresses over the half-bridge and push-pull configurations. Because entire input voltage present in Transformer Primary, Fuller bridge is appropriate for high rated applications.[3] [4]

Full Bridge has following advantages:

- High power handling capability
- Transformer isolation
- Higher transformer utilization
- Lower voltage stress on switches
- High frequency switching capability

But design requires correct controller tuning and parameter setting for stable operation and best transient performance. The analysis for operating principles, mathematical model is done here.

6.2 Converter Topology and Operation

Once the first stage boost PFC generates a regulated 400 V DC bus from the low voltage AC input, the full bridge converter takes the 400 V and down-converts it to 48 V to feed the load, and also provides isolation btw output & input. In this project,

FBC must produce a regulated 1000 W DC output from a high voltage bus supplied by 1^{st}stage. A switching frequency of 50 kHz is used to allow for small transformer sizes and small passive component sizes, which would be of importance when implementing a real power supply.[3] [4]

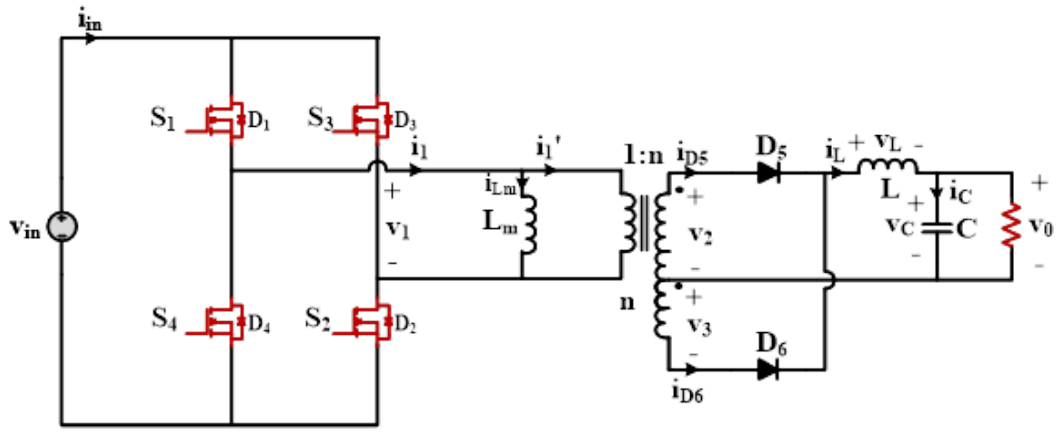

Fig. 6.1: FBC circuit Diagram

FBC basically contains power electronic circuit with 4 switches in "H" config. FBC process the input & gives an output with controlled magnitude & polarity using pulse-width modulation. Whether output voltage is increased or decreased depends upon toplogy & other factors.

FBC usually in practice used with Transformers & filtering components to form isolation FBC topology's merits: can accept high input voltage, high output current, and low power stress on the switches. Since it is isolated,grounds of input & output independent, thus eliminating ground loops and increasing safety[1].

Tbl. 6.1: Specs of FBC

Specs	Symbol	Val
Input voltage	V_{in}	400 V (rms)
Output voltage	V_o	48 V
Power	P_o	1 kW
Load Resistance	R	2.3 Ω
Inductor	L_o	200 μH
Capacitor	C_o	2200 μF
Switching Frequency	f_s	50 kHz

The Full Bridge converter works like this. The switches are turned on in pairs together. Pairs are diagonally opposing switches.

When S_1 and S_4 are ON for 1^{st} half of switching cycle then we have positive input voltage across primary winding

Other half switching cycle turn on switches S_2 and S_3 which will reverse the primary voltage and we have the negative input voltage across primary. The output of the

secondary winding is then inverted into a DC voltage by the output diodes which are filtered out for output voltage from FBC using an output LC filter.

6.3 Mathematical Modeling and Design Calculations

6.3.1 Mode 1

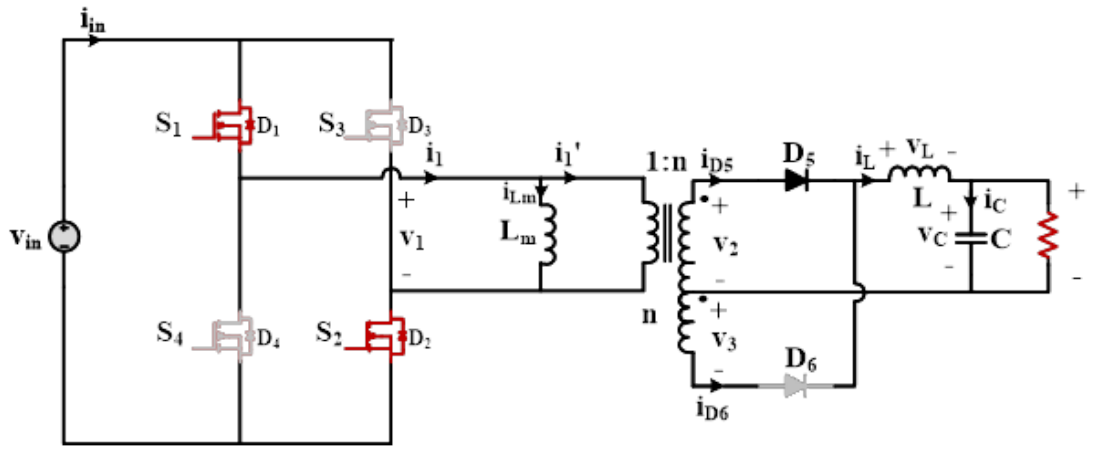

Fig. 6.2: Circuit Diagram of FBC in 1st Mode

$$\frac{v_{in}}{1} = \frac{v_2}{n} \tag{6.1}$$

Apply KVL,

$$v_{Lm} = v_{in} \tag{6.2}$$

$$\frac{di_{Lm}}{dt} = \frac{v_{in}}{L_m} \tag{6.3}$$

And,

$$v_L = v_2 - v_C \tag{6.4}$$

From 6.1,

$$\frac{di_L}{dt} = \frac{n}{L}v_{in} - \frac{v_C}{L} \tag{6.5}$$

Apply KCL,

$$i_L = i_C + i_0 \tag{6.6}$$

$$\frac{dv_C}{dt} = \frac{i_L}{C} - \frac{v_C}{RC} \tag{6.7}$$

6.3.2 Mode 2

Apply KVL,

$$-v_{Lm} + v_{in} = 0 \tag{6.8}$$

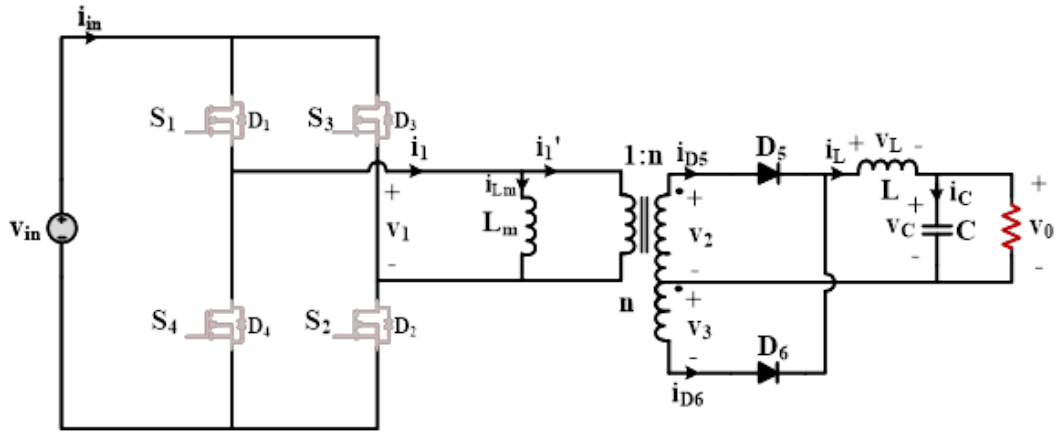

Fig. 6.3: Circuit Diagram of FBC 2nd Mode

$$\frac{di_{Lm}}{dt} = 0 \tag{6.9}$$

$$\frac{di_L}{dt} = \frac{-V_c}{L} \tag{6.10}$$

$$\frac{dv_C}{dt} = \frac{i_L}{C} - \frac{v_C}{RC} \tag{6.11}$$

6.3.3 Mode 3

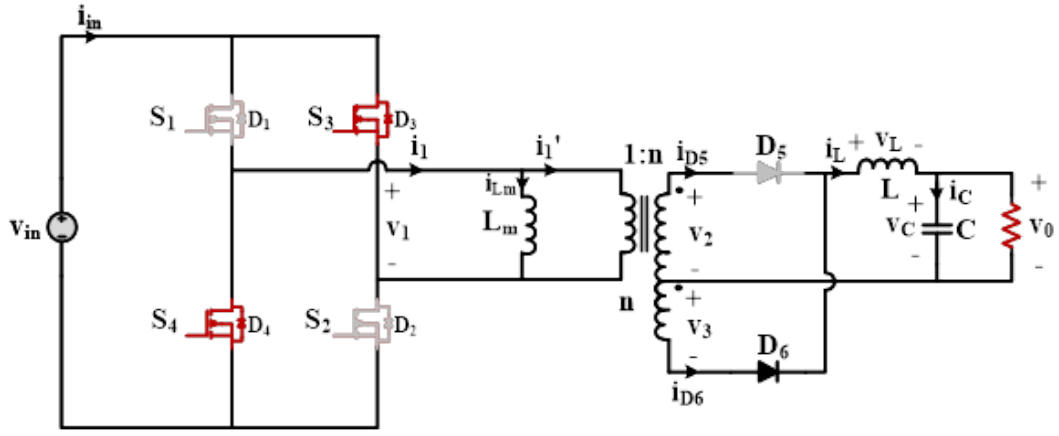

Fig. 6.4: Circuit Diagram of FBC 3rd Mode

$$\frac{v_{in}}{1} = \frac{v_3}{n} \tag{6.12}$$

Apply KVL,

$$-v_{Lm} = v_{in} \tag{6.13}$$

$$\frac{di_{Lm}}{dt} = -\frac{v_{in}}{L_m} \tag{6.14}$$

And,

$$v_L = -v_3 - v_C \tag{6.15}$$

From equation 6.12,

$$\frac{di_L}{dt} = \frac{n}{L}v_{in} - \frac{v_C}{L} \tag{6.16}$$

Applying KCL,

$$i_L = i_C + i_0 \tag{6.17}$$

$$\frac{dv_C}{dt} = \frac{i_L}{C} - \frac{v_C}{RC} \tag{6.18}$$

6.3.4 Mode 4

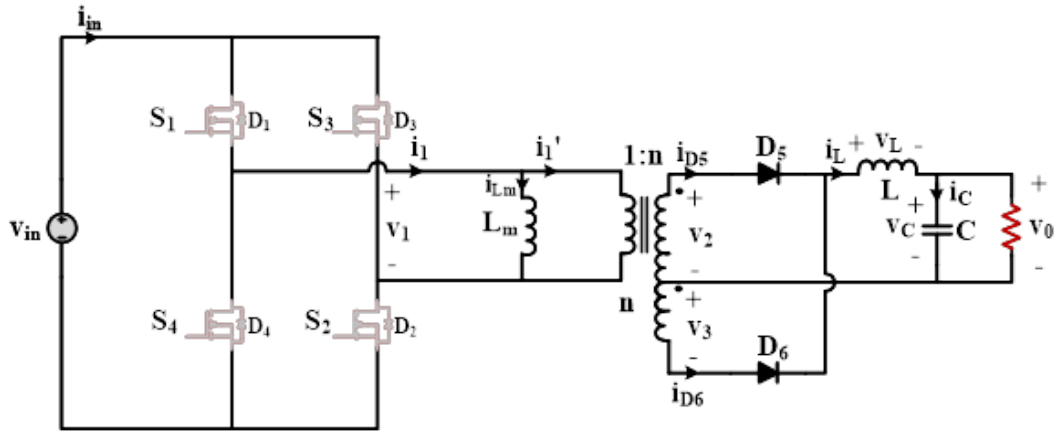

Fig. 6.5: Circuit Diagram of FBC 4th Mode

Apply KVL,

$$\frac{di_{Lm}}{dt} = 0 \tag{6.19}$$

And,

$$\frac{di_L}{dt} = -\frac{v_C}{L} \tag{6.20}$$

On applying KCL,

$$\frac{dv_C}{dt} = \frac{i_L}{C} - \frac{v_C}{RC} \tag{6.21}$$

6.3.5 State Space Average Model

Averaging of equations 6.3, 6.9, 6.14 and 6.19

$$2\bar{d}\frac{d\bar{i}_{Lm}}{dt} + 2\left(1-\bar{d}\right)\frac{d\bar{i}_{Lm}}{dt} = \bar{d}\frac{v_{in}}{L_m} - \bar{d}\frac{v_{in}}{L_m} \tag{6.22}$$

$$\frac{d\bar{i_{Lm}}}{dt} = 0 \tag{6.23}$$

Averaging of equations 6.5, 6.10, 6.16 and 6.20 [25]

$$2\bar{d}\frac{d\bar{i_L}}{dt} + 2\left(1-\bar{d}\right)\frac{d\bar{i_L}}{dt} = \bar{d}\left(\frac{n}{L}v_{in} - \frac{v_C}{L}\right) + \left(1-\bar{d}\right)\left(-\frac{v_C}{L}\right) + \bar{d}\left(\frac{n}{L}v_{in} - \frac{v_C}{L}\right) + \left(1-\bar{d}\right)\left(-\frac{v_C}{L}\right) \tag{6.24}$$

$$d\frac{\bar{i_L}}{dt} = \frac{\bar{d}n\bar{v}_{in}}{L} - \frac{\bar{v}_C}{L} \tag{6.25}$$

Averaging of equations 6.7, 6.11, 6.18 and 6.21[25]

$$2\bar{d}\frac{d\bar{v}_C}{dt} + 2\left(1-\bar{d}\right)\frac{d\bar{v}_C}{dt} = \bar{d}\left(\frac{\bar{i}_L}{C} - \frac{\bar{v}_C}{RC}\right) + \left(1-\bar{d}\right)\left(\frac{\bar{i}_L}{C} - \frac{\bar{v}_C}{RC}\right) + \bar{d}\left(\frac{\bar{i}_L}{C} - \frac{\bar{v}_C}{RC}\right) + \left(1-\bar{d}\right)\left(\frac{\bar{i}_L}{C} - \frac{\bar{v}_C}{RC}\right) \tag{6.26}$$

$$\frac{d\bar{v}_C}{dt} = \frac{\bar{i}_L}{C} - \frac{\bar{v}_C}{RC} \tag{6.27}$$

6.3.6 Small Signal Analysis

Adding perturbations in equation 6.25 [25],

$$\frac{dI_L}{dt} + \frac{d\hat{i}_L}{dt} = \frac{V_{in}n}{L}D - \frac{V_C}{L} + \frac{V_{in}n}{L}\hat{d} - \frac{\hat{v}_C}{L} \tag{6.28}$$

Adding perturbations in equation 6.27,

$$\frac{dV_C}{dt} + \frac{d\hat{v}_C}{dt} = \frac{I_L}{C} - \frac{V_C}{RC} + \frac{\hat{i}_L}{C} - \frac{\hat{v}_C}{RC} \tag{6.29}$$

Comparing DC terms in LHS and RHS in equation 6.28,

$$\frac{dI_L}{dt} = \frac{V_{in}n}{L}D - \frac{V_C}{L} \tag{6.30}$$

$$\frac{dI_L}{dt} = 0 \text{ since, } I_L = 0 \tag{6.31}$$

$$V_{in} = \frac{V_C}{nD} \tag{6.32}$$

Comparing DC terms in LHS and RHS in equation 6.29

$$\frac{dV_C}{dt} = \frac{I_L}{C} - \frac{V_C}{RC} \tag{6.33}$$

$$I_L = \frac{V_C}{R} \tag{6.34}$$

Comparing small signal terms in equation 6.28,

$$\frac{d\hat{i}_L}{dt} = -\frac{\hat{v}_C}{L} + \frac{V_{in}n}{L}\hat{d}(40) \tag{6.35}$$

Comparing small signal terms in equation 6.29

$$\frac{d\hat{v}_C}{dt} = \frac{\hat{i}_L}{C} - \frac{\hat{v}_C}{RC}(41) \tag{6.36}$$

6.3.7 Design Calculations

Duty Cycle(D):

Transformer turns ratio obtained is:

$$n = \frac{N_s}{N_p} = \frac{57}{400} = 0.1425$$

Voltage ratio is:

$$V_o = 2nDV_{in}$$

Duty ratio is therefore calculated as:

$$D = \frac{V_o}{2nV_{in}}$$

Substituting the converter specifications:

$$D = \frac{48}{2 \times 0.1425 \times 400} = 0.42$$

Thus: D=42.1%

Transformer Design Calculation

Transformer turns ratio selected from the MATLAB/Simulink model is:

$$n = \frac{57}{400} = 0.1425n = 40057 = 0.1425$$

Thus, the approximate transformer turns ratio becomes:

$$N_p : N_s \approx 7 : 1$$

The transformer apparent power rating selected for the converter is:

$$P_{rating} = 1200 \text{ VA}$$

Primary current is :

$$I_p = \frac{1000}{400} = 2.5 \text{ A}$$

Secondary current is :

$$I_s = \frac{1000}{48} = 20.83 \text{ A}$$

The choice of magnetising inductance is actually very important as this is the value of the quantity that provides the transformer with its flux when the transformer is operating. From the analysis of passing through the magnetising inductance one can state that with increasing of the value of magnetising inductance there would be the increasing of magnetising current which results in decreasing of core losses in the transformer.[1]

From the analysis of transformer, it can be concluded that the choice of magnetising inductance affects the following factors: Magnetising current magnitude, Transformer efficiency, Saturation & Stability of full bridge converter.

Speaking about magnetising inductance it is necessary to say that the latter performs some function in the transformer and that magnetising inductance is the factor that provides the transformer with flux. As mentioned above, the choice of magnetising inductance is very important as without it the transformer could not operate properly.

The transformer parameters used in the simulation are summarized in table 6.2

Tbl. 6.2: Transformer Parameters

Parameters	**Val**
Transformer rating	1200 VA
Primary voltage	400 V
Secondary voltage	57 V
Primary Resistance	25 $m\Omega$
Secondary Resistance	10 $m\Omega$
Magnetizing Inductance	5 mH
Switching Frequency	50 kHz

Output Inductor Design

The output current is calculated as:

$$I_o = \frac{1000}{48} = 20.83 \text{ A}$$

Assuming ripple current of 20%:

$$\Delta I_L = 0.2 \times 20.83 = 4.16 \text{ A}$$

The switching period corresponding to 50 kHz is:

$$T_s = \frac{1}{50 \times 10^3} = 20 \ \mu s$$

The output inductance is calculated using:

$$L_o = \frac{(nV_{in} - V_o)DT_s}{\Delta I_L}$$

Substituting the values:

$$L_o = \frac{(0.1425 \times 400 - 48) \times 0.421 \times 20 \times 10^{-6}}{4.16}$$

Thus: $L_o \approx 91\mu H$ For practical implementation: L_o=200 μH
Output Capacitor Design
The allowable ripple is 1%.

$$\Delta V_o = 0.01 \times 48 = 0.48 \text{ V}$$

The output capacitor is calculated using:

$$C_o = \frac{I_o DT_s}{\Delta V_o}$$

Substituting the converter parameters:

$$C_o = \frac{20.83 \times 0.421 \times 20 \times 10^{-6}}{0.48}$$

Thus: C_o ≈366 μF For improved output voltage stability and reduced ripple, the capacitor value is selected as: $C_o = 2200\ \mu F$

6.4 PI Controller Design for FBC

It is responsible to keep Output voltage stable.This control makes Output voltage waveform be good..

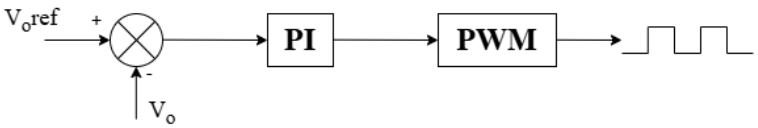

Fig. 6.6: PI control block Diagram

Transfer function of PIis written [18] as follows:

$$G_{PI}(s) = K_p + K_i/s \tag{6.37}$$

This means we have, K_p proportional gain and K_i integral gain.

We pick gains so that converter works fine & respond quickly & have a small error when it is running steadily. The PI controller gains are very important, for the PI controller.

6.4.1 Voltage loop design

The output voltage is monitored constantly and error calculated in reference of 400 Volts. Voltage error is fed into PI, that gives needed duty [12]:

$$e_v(t) = V_{ref} - V_o \tag{6.38}$$

After several tuning iterations, the voltage loop PI controller gains are selected as

Tbl. 6.3: Voltage Loop PI Parameters

Gain	Val
Kp	0.1
Ki	1

6.5 Simulation Results

PWM Pulse

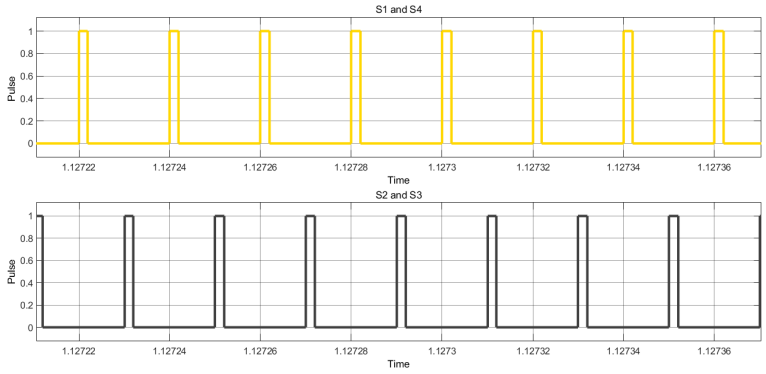

Fig. 6.7: PWM Pulse of FBC

Transformer Input voltage

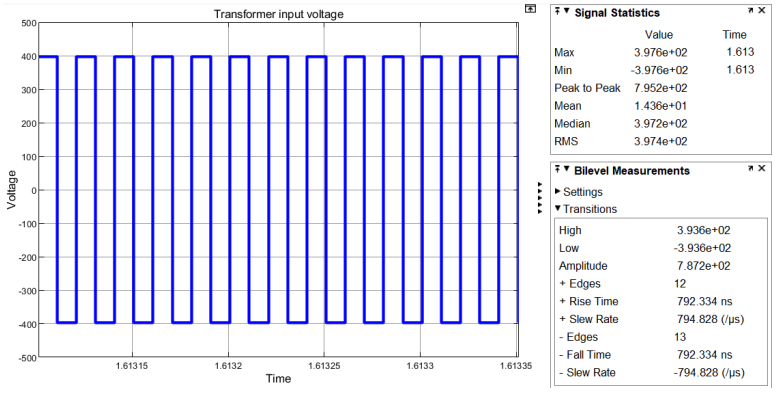

Fig. 6.8: Transformer input voltage of FBC

Transformer Input current

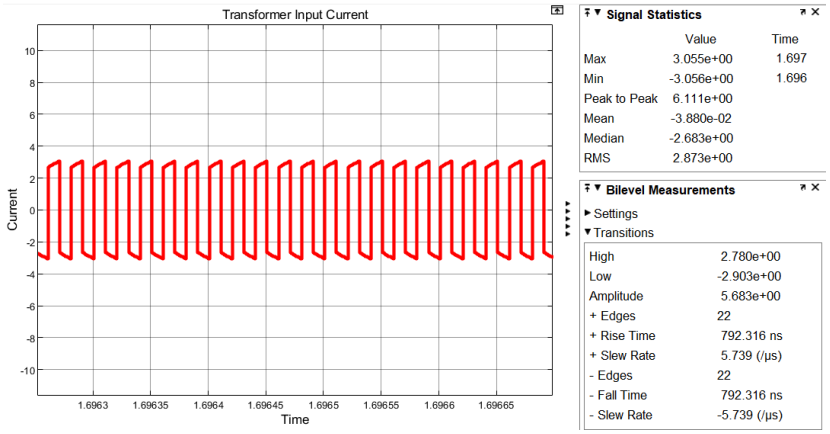

Fig. 6.9: Transformer input current of FBC

Output voltage

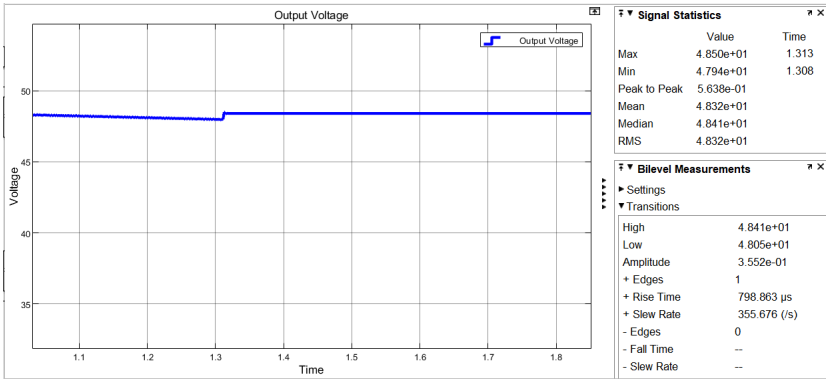

Fig. 6.10: Output voltage FBC

Output current

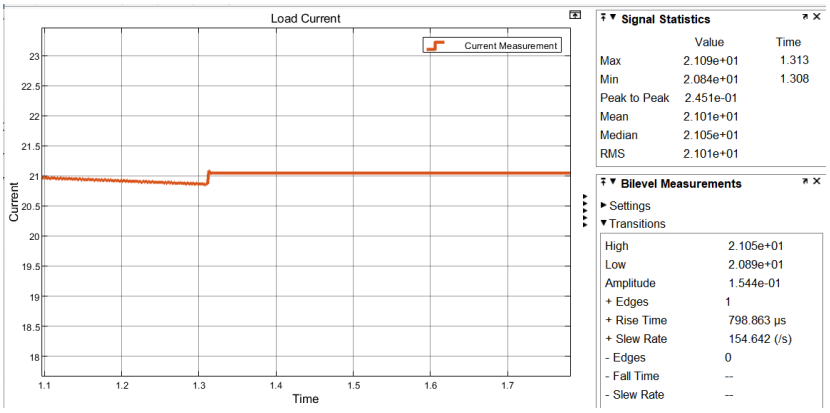

Fig. 6.11: Output current FBC

6.6 Conclusion

Thus FBC, suited in medium rated uses. It provides isolation also. The simulation results showed a correct operation of bridge, transformer excitation, and voltage regulator stability. On the other hand, due to hard-switching, increased device stresses, switching losses of converter, and hence a relative lower efficiency compared to some more advanced soft switching topologies.

CHAPTER 7

PSFB

7.1 Introduction

The switching losses in traditional Hard switched Full Bridge converter are higher especially for higher power level with an increased EMI as the power level grows higher. Hence soft-switching converter topology is more popularly used for modern EV charging application.[15] [16]

Among different types of soft-switching topology PSFB is preferred among others to handle power from medium to high level isolated DC-DC conversion with a better efficiency with low switching stress and Zero Voltage Switching (ZVS) ability.[15]

PSFB has 4 semiconductor swtches that are operated in full bridge config, a high freq isolation Transformer, rectification, filter circuit & control circuitry. In PSFB, voltage regulation is done by phase shifting angle of 2 bridges & also ZVS can be achieved.

In PSFB swtches are switched ON under zero voltage, therfore losses while switching is reduced & thus efficiency is increased. A reduction in switching stress also results in good thermal characteristics with operation in higher frequency.

Here PSFB is designed & analysed for dc-dc conversion of 400 V into 48 V DC regulated for the purpose of EV charging at 50 kHz switching frequency.PI control implemented for this PFC to control output voltage.[16]

PSFB merits are listed below:

- ZVS
- Low switching losses
- Higher converter efficiency
- Lower electromagnetic interference
- Isolation with Transformer
- High power density

However careful selection of phase shift angle and transformer parameter is crucial for soft switching of the devices and operation of converter under variable loads.

In this chapter the operating principle, modeling, design calculations and controller design for PSFB converter have been carried out.

7.2 Converter Topology and Operation

It is a more complex topology in the PSFB converter. It has wide range of application in high rated uses because it has soft-switching capability & better efficiency of conversion. The secondary voltage of high frequency transformer is then filtered by the output LC filter.[15] [16]

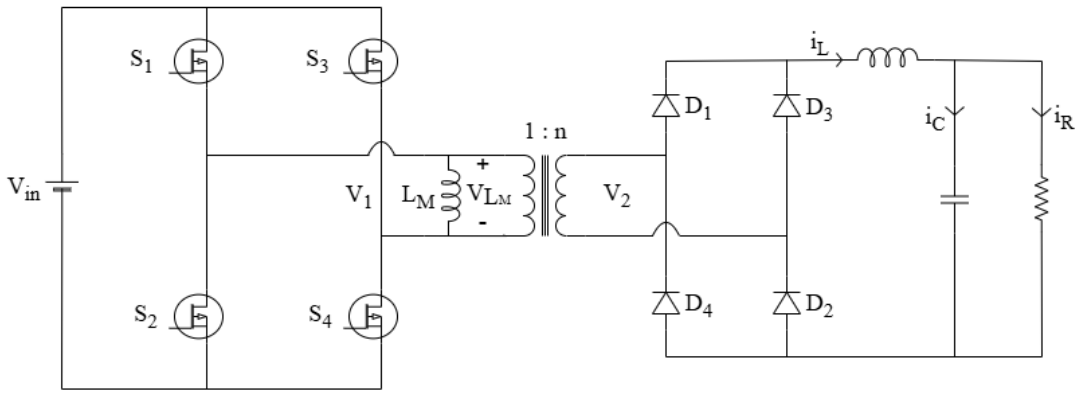

Fig. 7.1: Phase Shift Full Bridge Converter Circuit Diagram

The specifications of PSFB are given in tbl 7.1.

Tbl. 7.1: Specs of PSFB

Specs	Symbol	Val
Input voltage	V_{in}	400 V (rms)
Output voltage	V_o	48 V
Power	P_o	2 kW
Load Resistance	R	1.152 Ω
Inductor	L_o	1 mH
Capacitor	C_o	3300 μF
Switching Frequency	f_s	50 kHz

PSFB has 4 semiconductor swtches that are operated in full bridge config, a high freq isolation Transformer, rectification, filter circuit & control circuitry. In PSFB, voltage regulation is done by phase shifting angle of 2 bridges & also ZVS can be achieved.

- Mode 1: This is the positive power transfer interval.

Swtches S1 and S4, ON-ed at a time. The input voltage given across primary of the Transformer. It is applied positively. Source transfers energy via Transformer & rectification to load.

- Mode 2: this is the freewheeling interval.

Here, swtches that make up a bridge leg ON-ed at a time. As no voltage given to primary of the Transformer, stored energy allows current through load to remain constant. This Mode 2 is useful in obtaining zero voltage switching as the switch capacitances are discharged before the switching edge is reached. Thus the load still receives energy from mode 2 of the power transfer.

- Mode 3: This is the negative power transfer interval.

Swtches S2 and S3, ON-ed at a time. The input voltage given across primary of the Transformer. It is applied negatively. Source transfers energy via Transformer & rectification to load.

- Mode 4: this is the freewheeling interval.

At this point the transformer gets a break. Its main voltage becomes zero. NOw already stored energy in coils takes over & helps to keep current going to load. This energy also makes sure that the converter switches on and off smoothly.

The converter works better when it switches on and off smoothly and loses energy. This makes the whole system work efficiently reduces interference with other devices and keeps the temperature under control. The switching and lower losses, in the converter really improve how well it works overall including its efficiency and how well it works with other devices and its temperature.

7.3 Mathematical Modeling and Design

The mathematical model for the PSFB converter helps in understanding converter dynamics, choosing suitable converter parameters and design of the controller. The PSFB converter uses phase-shift between the bridge legs for realization of soft switching and hence reducing the switching losses.[27]

7.3.1 Mode 1 Positive Power Transfer Interval

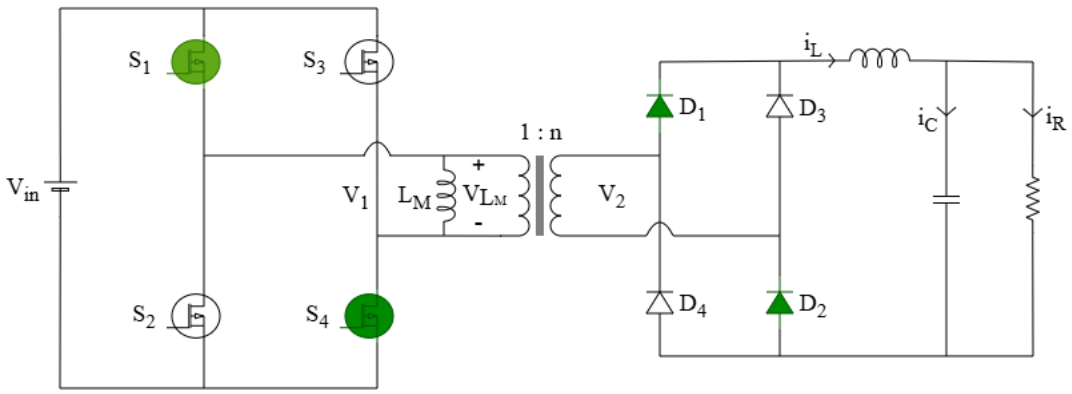

Fig. 7.2: Phase Shift Full Bridge Converter Mode 1

$$\frac{di_{L_M}}{dt} = \frac{1}{L_M} * v_{in} \tag{7.1}$$

$$\frac{di_L}{dt} = \frac{1}{L}(nV_{in}) - \frac{1}{L}V_C \tag{7.2}$$

$n = \frac{N_s}{N_p}$, Transformer turns ratio.[16, 26]

$$i_L = i_C + i_o \tag{7.3}$$

$$\Rightarrow i_C = i_L - i_o \tag{7.4}$$

$$\Rightarrow \frac{dV_C}{dt} = \frac{1}{C}i_L - \frac{1}{C} * \frac{V_o}{R} \tag{7.5}$$

$$\frac{dV_C}{dt} = \frac{i_L}{C} - \frac{V_c}{RC} \tag{7.6}$$

7.3.2 Mode 2 Freewheeling Interval

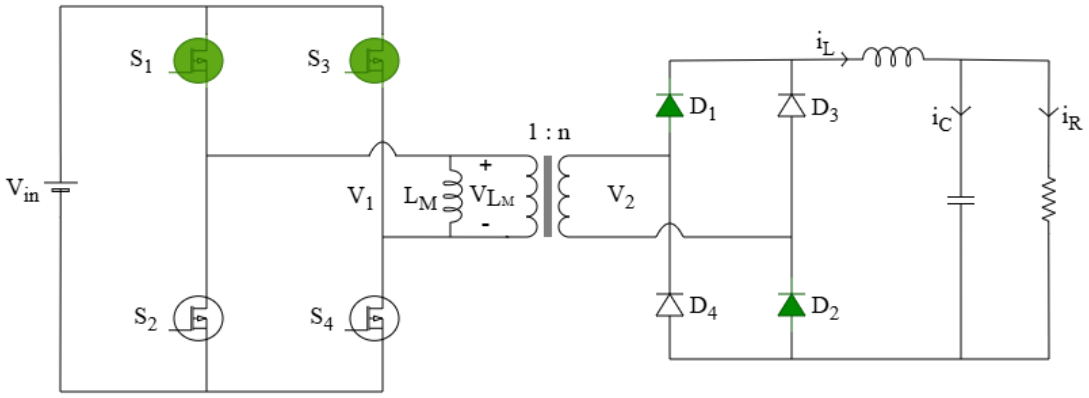

Fig. 7.3: PSFB 2nd Mode

$$V_1 = 0 \Rightarrow V_{L_M} = 0$$
$$V_2 = nV_1 = 0$$

$$\frac{di_{L_M}}{dt} = 0 \tag{7.7}$$

From [16, 26]

$$-V_2 + V_L + V_C = 0 \Rightarrow V_L = -V_C \Rightarrow \frac{di_L}{dt} = \frac{-V_C}{L} \tag{7.8}$$

$$i_L = i_C + i_o \Rightarrow \frac{dV_C}{dt} = \frac{i_L}{C} - \frac{V_C}{RC} \tag{7.9}$$

7.3.3 Mode 3 Negative Power Transfer Interval

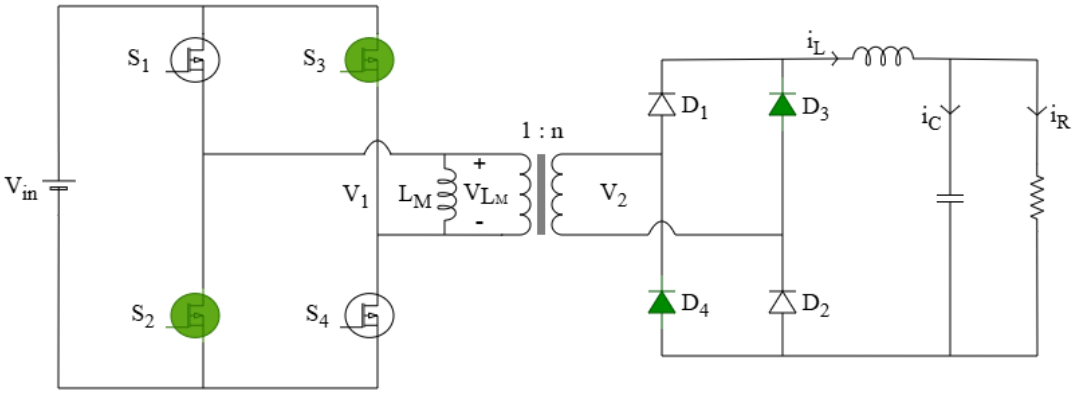

Fig. 7.4: Phase Shift Full Bridge Converter Mode 3

$$V_1 = -V_{in} \Rightarrow V_{L_M} = -V_{in} \tag{7.10}$$

$$V_2 = -nV_{in} \tag{7.11}$$

$$\frac{di_{L_M}}{dt} = \frac{1}{L_M}(-V_{in}) \tag{7.12}$$

$$+V_2 - V_L - V_C = 0 \tag{7.13}$$

$$V_L = V_2 - V_C \Rightarrow \frac{di_L}{dt} = \frac{-nV_{in}}{L} - \frac{V_C}{L} \tag{7.14}$$

$$i_C + i_o = i_L \Rightarrow i_C = i_L - i_o \Rightarrow \frac{dv_C}{dt} = \frac{i_L}{C} - \frac{V_C}{RC} \tag{7.15}$$

7.3.4 Mode 4 Freewheeling Interval

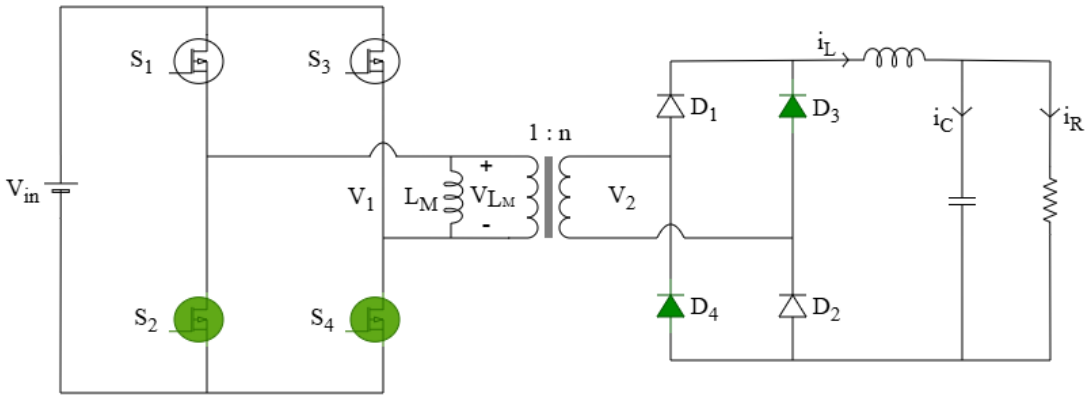

Fig. 7.5: Phase Shift Full Bridge Converter Mode 4

$$V_1 = 0 \Rightarrow V_{L_M} = 0 \Rightarrow \frac{di_{L_M}}{dt} = 0 \tag{7.16}$$

$$V_2 = 0 \qquad (V_2 = nV_1) \tag{7.17}$$

$$\text{From [16, 26]} + V_2 - V_L - V_C = 0 \Rightarrow V_L = -V_C \tag{7.18}$$

$$\frac{di_L}{dt} = \frac{-V_C}{L} \tag{7.19}$$

$$i_C + i_o = i_L \Rightarrow i_C = i_L - i_o \tag{7.20}$$

$$\Rightarrow \frac{dV_C}{dt} = \frac{i_L}{C} - \frac{V_C}{RC} \tag{7.21}$$

7.3.5 Averaged State-Space Model

PSFB avg model got by combining operating intervals over one switching period.

From the equations 7.1, 7.2, 7.6, 7.7, 7.8, 7.9, 7.12, 7.14, 7.15, 7.16, 7.19 and 7.21,
equations 7.1, 7.2, 7.6, & 7.12, 7.14, 7.15, X by dT
equations 7.7, 7.8, 7.9, & 7.16, 7.19, 7.21, X by (1 - d)T
$\Rightarrow$ from equations 7.1 , 7.7 & 7.12 , 7.16 ;

$$2T\frac{d\bar{i}_{L_M}}{dt} = 0 \Rightarrow \frac{d\bar{i}_{L_M}}{dt} = 0 \tag{7.22}$$

$\Rightarrow$ from equations 7.2 , 7.8 & 7.14 , 7.19 ;

$$\Rightarrow \frac{d\bar{i}_L}{dt} = \frac{-\overline{V_C}}{L} + \frac{2n\bar{d}V_{in}}{L} \tag{7.23}$$

$\Rightarrow$ from equations 7.6., 7.9 & 7.15, 7.21 referred from [26]

$$\frac{d\overline{V_C}}{dt} = \frac{\bar{i}_L}{C} - \frac{\overline{V_C}}{RC} \tag{7.24}$$

Averaged model representation is therefore given by:

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_o} \\ \frac{1}{C_o} & -\frac{1}{RC_o} \end{bmatrix}\begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{2Dn}{L_o} \\ 0 \end{bmatrix} V_{in} \tag{7.25}$$

The averaged model represents the large-signal dynamics& is useful for designing controller & stability.[27]

7.3.6 Small-Signal Modeling

For transient analysis, perturbations & lineraisation is performed[27].Converter variables are represented as:

$$i_L = I_L + \hat{i}_L v_o = V_O + \hat{v}_o d = D + \hat{d} \tag{7.26}$$

where:

- I_L, V_o and D represent steady-state quantities.
- $\hat{i}_L$, $\hat{v}_o$ and $\hat{d}$ represent small perturbations.

Inductor current equation becomes[27]:

$$L_o \frac{d\hat{i}_L}{dt} = 2nV_{in}\hat{d} - \hat{v}_o \tag{7.27}$$

Similarly, the capacitor voltage equation becomes[27]:

$$C_o \frac{d\hat{v}_o}{dt} = \hat{i}_L - \frac{\hat{v}_o}{R} \tag{7.28}$$

7.3.7 Design Calculations

Duty Ratio(D):
Transformer turns ratio is:

$$n = \frac{N_s}{N_p} = \frac{100}{400} = 0.25$$

voltage ratio of PSFB is:

$$V_o = 2nDV_{in}$$

Duty ratio is :

$$D = \frac{V_o}{2nV_{in}}$$

Substituting the converter specifications:

$$D = \frac{48}{2 \times 0.25 \times 400} = 0.24$$

Thus: $D = 24\%$
Transformer Design Calculation
Transformer turns ratio is:

$$n = \frac{100}{400} = 0.25$$

Thus, the approximate transformer turns ratio becomes:

$$N_p : N_s = 4 : 1$$

The transformer apparent power rating selected for the converter is:

$$P_{rating} = 2000 \text{ VA}$$

Primary current is:

$$I_p = \frac{2000}{400} = 5 \text{ A}$$

Secondary current is:

$$I_s = \frac{2000}{48} = 41.67 \text{ A}$$

Transformer parameters used are in tbl 7.2

Tbl. 7.2: Transformer Parameters

Parameters	**Val**
Transformer Rating	2000 VA
Primary voltage	400 V
Secondary voltage	100 V
Switching Frequency	50 kHz

Output Inductor Design
The output current is calculated as:

$$I_o = \frac{2000}{48} = 41.67 \text{ A}$$

Assuming ripple current of 20%:

$$\Delta I_L = 0.2 \times 41.67 = 8.33 \text{ A}$$

The switching period corresponding to 50 kHz is:

$$T_s = \frac{1}{50 \times 10^3} = 20 \, \mu s$$

The output inductance is calculated using:

$$L_o = \frac{(nV_{in} - V_o)DT_s}{\Delta I_L}$$

Substituting the values:

$$L_o = \frac{(0.25 \times 400 - 48) \times 0.24 \times 20 \times 10^{-6}}{8.33}$$

Thus: $L_o \approx 300 \, \mu H$

For practical implementation and improved ripple reduction, the inductance value is selected as:

$$L_o = 1000 \, \mu H$$

Output Capacitor Design
Allowable output ripple is 1% .

$$\Delta V_o = 0.01 \times 48 = 0.48 \text{ V}$$

The output capacitor is calculated using:

$$C_o = \frac{I_o D T_s}{\Delta V_o}$$

Substituting the converter parameters:

$$C_o = \frac{41.67 \times 0.24 \times 20 \times 10^{-6}}{0.48}$$

Thus: $C_o \approx 417\ \mu F$
For improved output voltage stability and reduced ripple, the capacitor value is selected as: $C_o = 3300\ \mu F$

7.4 PI Controller

PSFB is going to use a PI controller for getting stable output voltage of the PSFB converter. PI controller will make sure PSFB works correctly so the output voltage stays at 48 V.

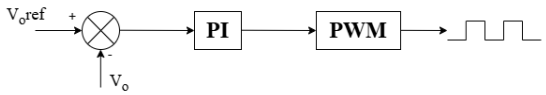

Fig. 7.6: PI control block Diagram

It does this by changing & using phase shift, btw bridge legs of PSFB. PI controller has two parts: the integral and the proportional.These two parts help the PSFB converter work well when things change.

When the PSFB converter is working steadily there will be no error.The PI controller does a good job of controlling the PSFB converter.The PSFB converter and the PI controller are a team.The PSFB converter will work properly because of the PI controller.

PI controller tf is[12]:

$$G_P I(s) = Kp.Ki/s$$

This means we have:

- K p is the proportional gain
- K i is the integral gain

The phase shift signal that is generated drives the generator that produces the pulses. This generator operates at a frequency of 50 kHz. The pulses generated by the phase

shift turn the on and off the pieces of the PSFB converter. Those are in advanced and in delay.[16]

For generation of the phase-shifted PWM signals, a MATLAB Function block is implemented in the Simulink model. The function generates required PWM signals.[16]

This phase shift controls required duty ratio applied across Transformer primary winding, thereby regulating the converter output voltage.

The PI-controlled PSFB converter presented here has the following advantages:ZVS , Less losses while switching , Better converter efficiency , Good regulation of the output voltage , Less electromagnetic interference , Good transient characteristics. The overall PSFB converter is modeled and simulated under MATLAB/Simulink, which is analyzed.

7.5 Simulation Results

PWM Pulse

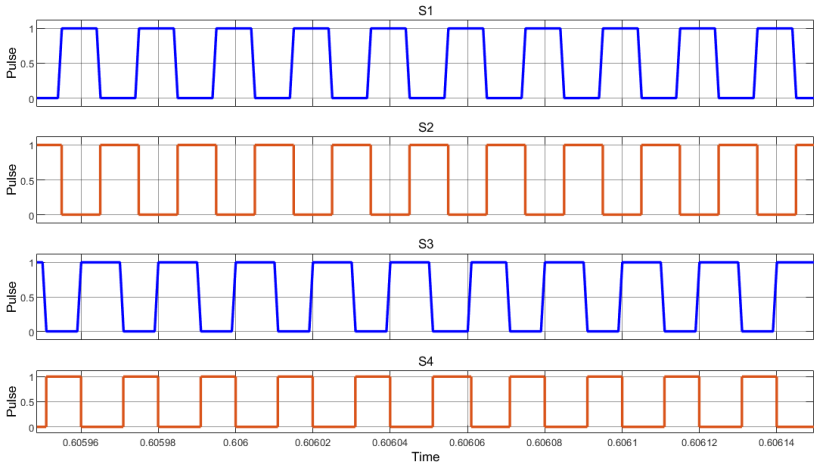

Fig. 7.7: PWM Pulse waveform of PSFB

Transformer Input voltage

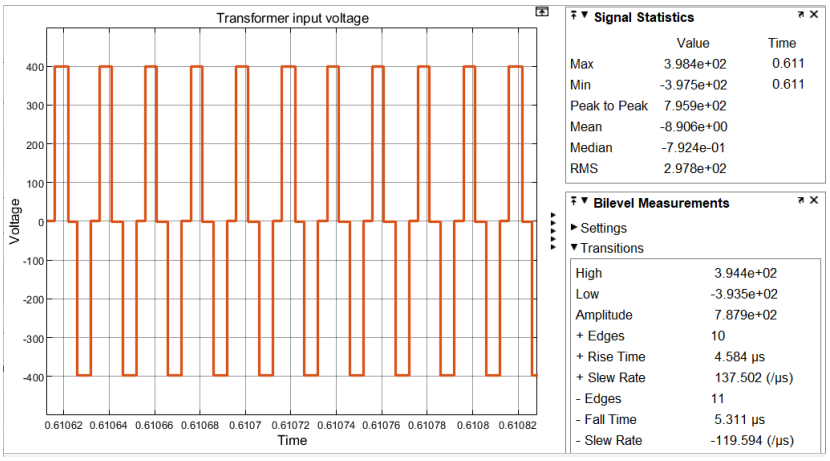

Fig. 7.8: Transformer Input voltage of PSFB

Transformer Input current

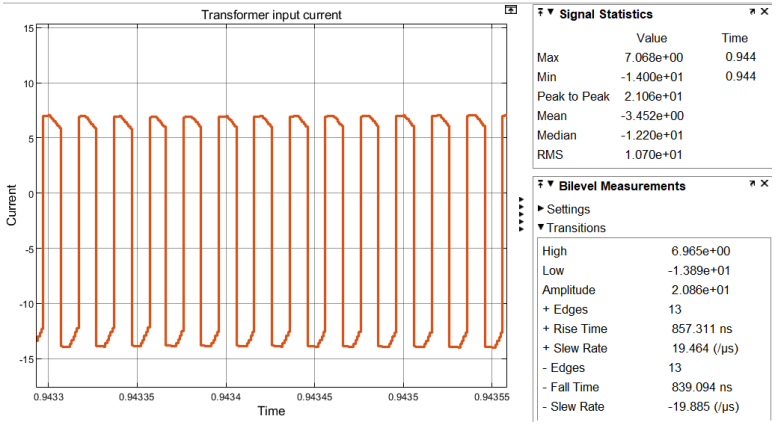

Fig. 7.9: Transformer Input current of PSFB

Output voltage

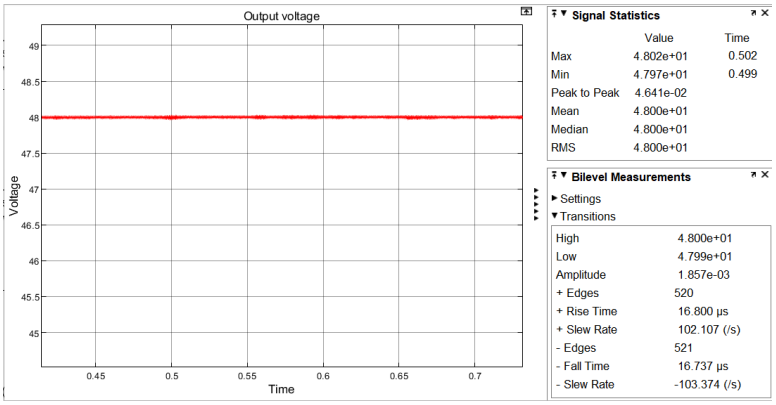

Fig. 7.10: Output voltage of PSFB

Load Current

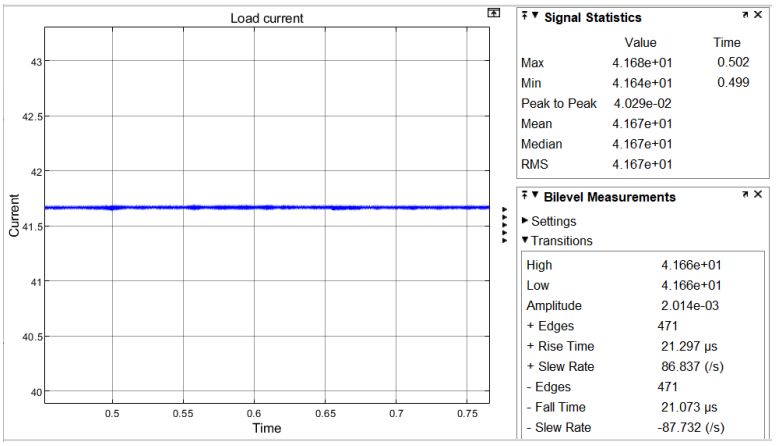

Fig. 7.11: Output current of PSFB

7.6 Conclusion

The PSFB was modelled & analyzed. Using phase shift & soft-switching in PSFB converter reduced the switching losses, smoother current transitions and higher efficiency was observed. Results from simulation shows it provides excellent load voltage regulation, stable power transfer & higher efficiency compared with ordinary FBC. Thus it is better suitable for high rated isolated DC-DC conversion applications of EV charging system.[26]

CHAPTER 8

COMPARATIVE ANALYSIS AND OVERALL PERFORMANCE OF THE SYSTEM

8.1 Introduction

The efficiency of a given electric vehicle charger highly depends on the characteristics of both front-end PFC and isolated DC-DC converters. Hence the analysis of various converter topologies are being performed to establish best suitable topologies in chargers. Comprehensive comparative analysis between the simulated PFC converters & isolated dc-dc converters are performed & results are in this chapter. The analysis is being performed based on several performance parameters like efficiency, power factor(PF), THD, voltage regulation, ripple values, switching characteristic, practicality of implementation in the EV chargers etc [10, 8].

Three types of PFC topologies that were investigated were Boost, Interleaved boost & Flyback. Likewise two isolated DC-DC converters that were implemented and analyzed were FBC & PSFB converter.[21, 2].

Simulations were performed systematically and compared on various parameter like efficiency etc of each converter topologies. Along with that the performance evaluation of total EV charging system is being compared so as to find the most efficient, with better power quality and good voltage regulation and practicability in EV charger applications.

8.2 Overall EV Charging System configuration

The EV charging system which has been designed and developed has two power conversion stages: front end power factor correction stage & dc dc stage. PFC was designed & developed with aim of shaping input ac source & delivering high stable output with low THD & good power factor. The regulated DC stage provided power to the second stage of power conversion which was an isolated d.c-d.c converter. This converter received d.c-link voltage as input and delivered the required low-voltage dc for charging the battery of the EV. Apart from regulating the output dc-dc converter also provide the safety and isolation for the charger, to separate the battery from source. DC link cap was utilized to maintain voltage regulated btw the two power stages. With the usage of the above mentioned two power stages the charger provides good power quality and efficient and regulated delivery, power from source to the battery. [10, 8, 21]

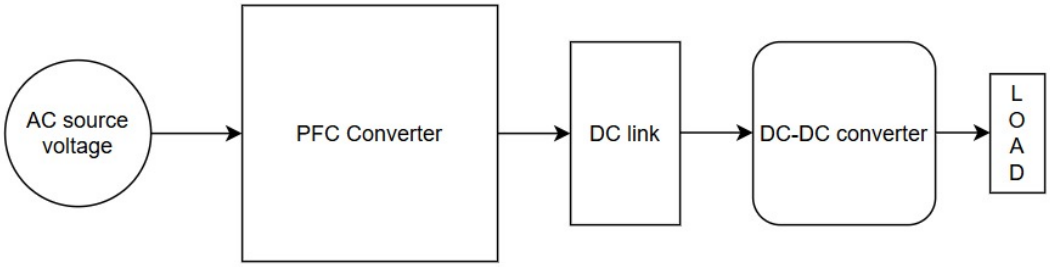

Fig. 8.1: System Block Diagram

Figure 8.1 illustrates the overall configuration of the proposed two-stage EV charging system considered in this work.

8.3 Overall System Performance Analysis

The operation of combined PFC & isolated DC-DC converter for different operating conditions was simulated.A proper input current shape, and the regulated output voltage of battery charging process, THD analysis stable DC link voltage were performed.

The AC input current waveform was almost sinusoidal & follows input. Ripple content was found to be within acceptable range at desired level 400 V. The 2nd stage would enable regulation of required voltage level.Total efficiency of the charging system is limited by efficiency of both stages.

8.3.1 Boost PFC with Full Bridge Converter

Using PI Controller

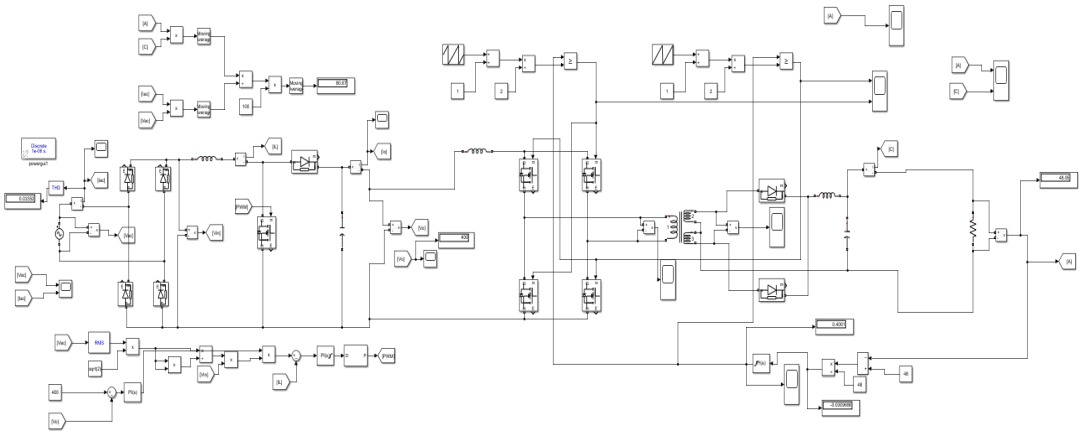

Fig. 8.2: Simulation circuit

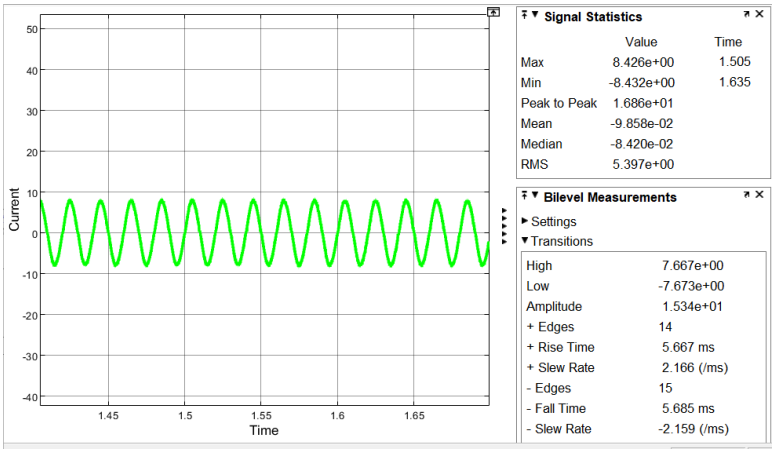

Fig. 8.3: Input current

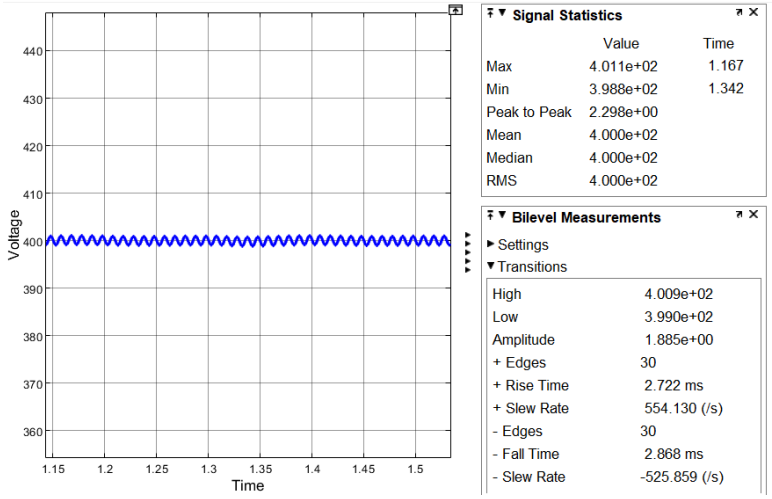

Fig. 8.4: DC Link voltage

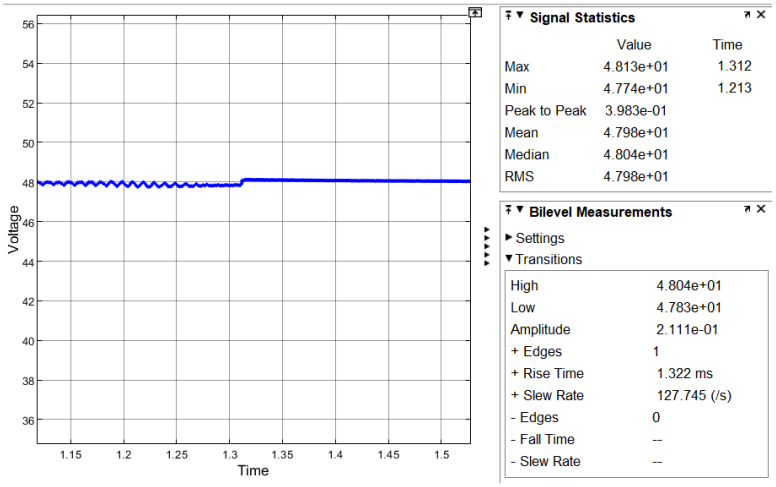

Fig. 8.5: Output voltage

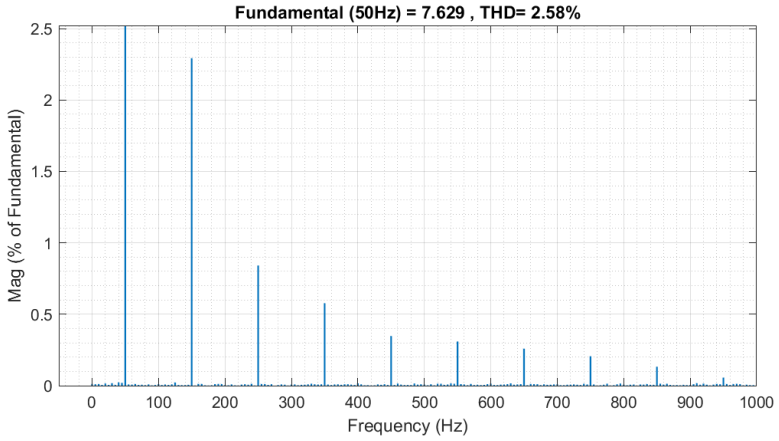

Fig. 8.6: Harmonic Analysis

T.H.D = 2.58% & pf = 0.999

Using PR Controller

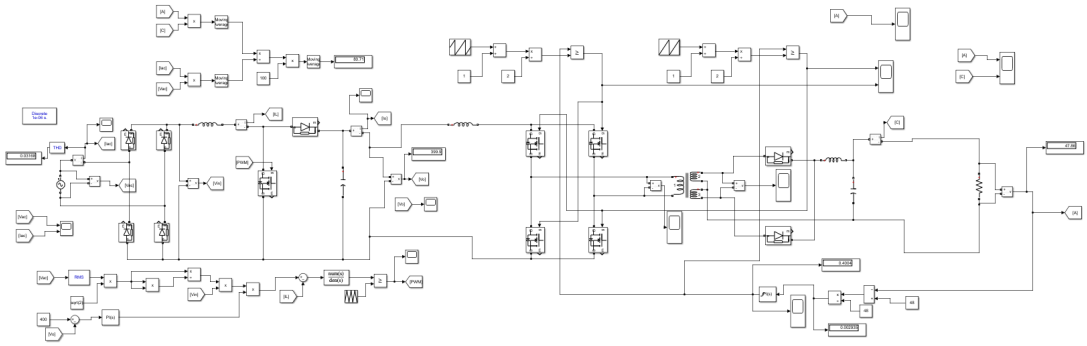

Fig. 8.7: Simulation circuit

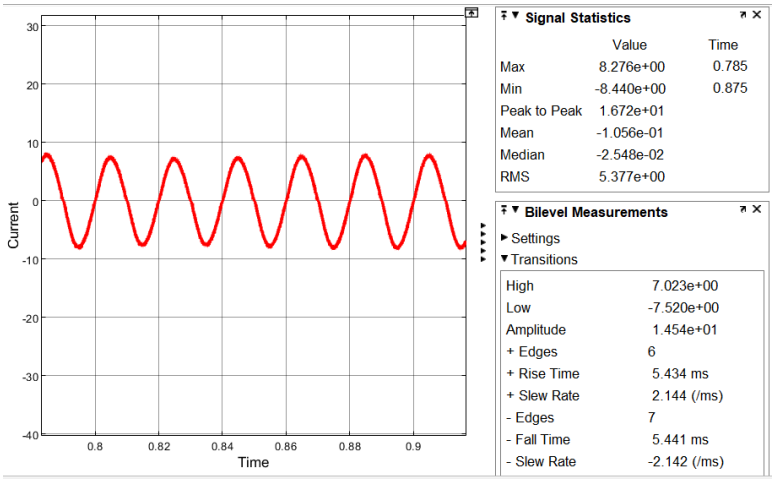

Fig. 8.8: Input current

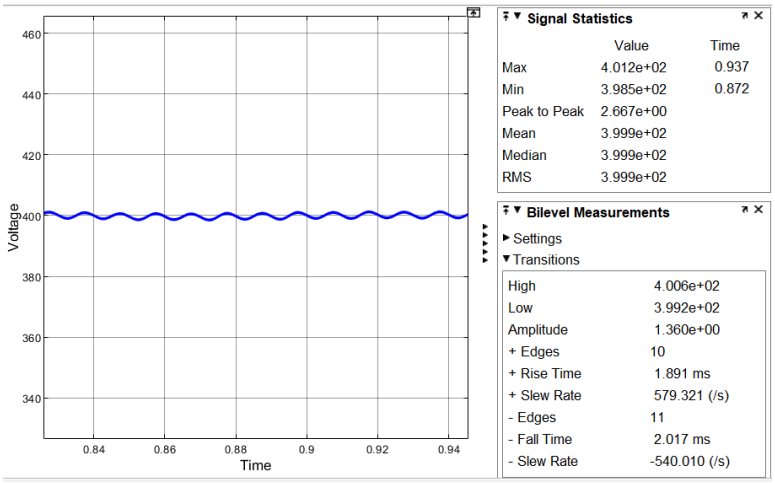

Fig. 8.9: DC Link voltage

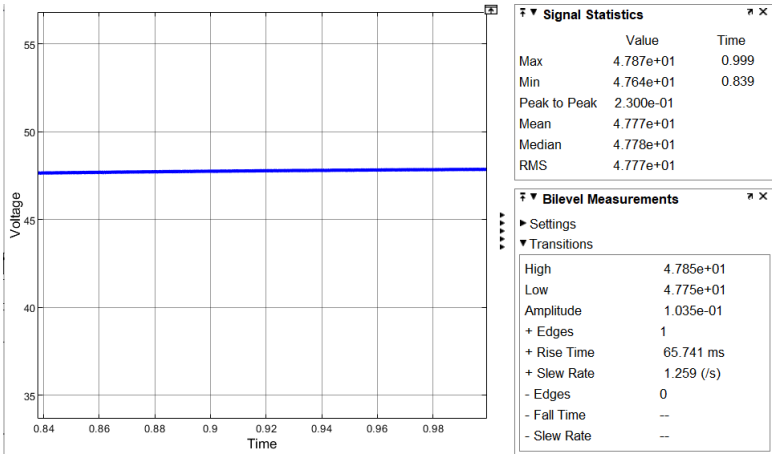

Fig. 8.10: Output voltage

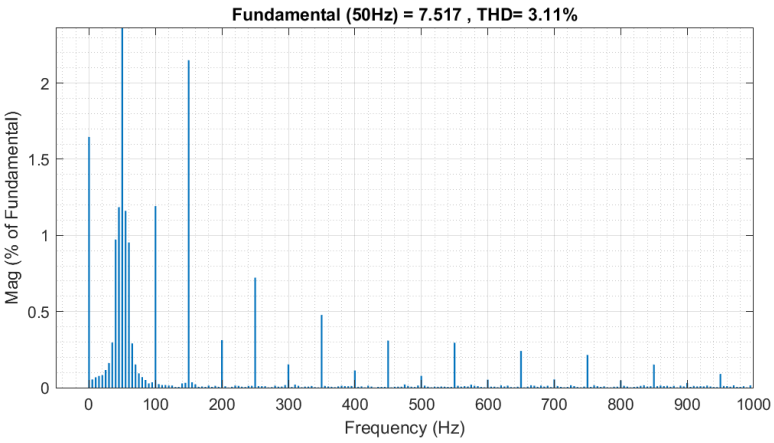

Fig. 8.11: Harmonic Analysis

T H D = 3.11% & pf = 0.99

Using Lyapunov Controller

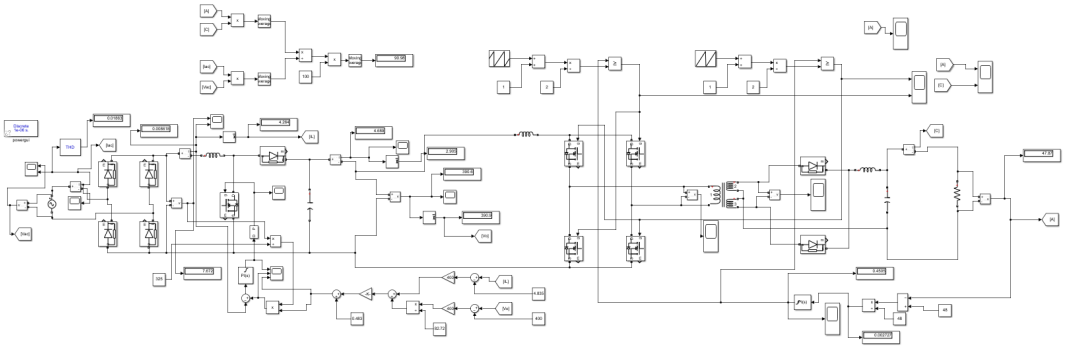

Fig. 8.12: Simulation circuit

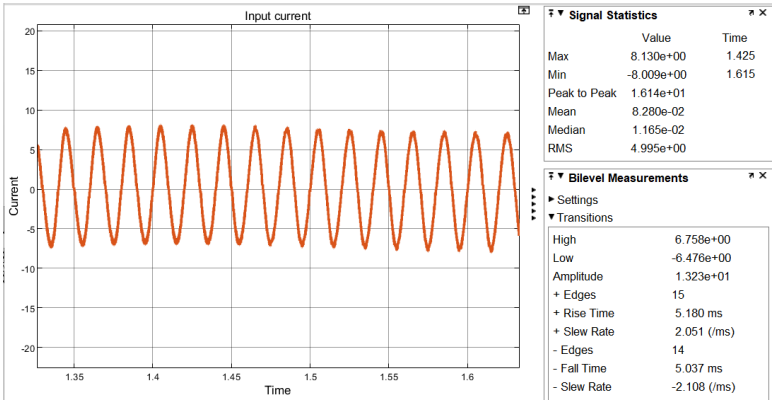

Fig. 8.13: Input current

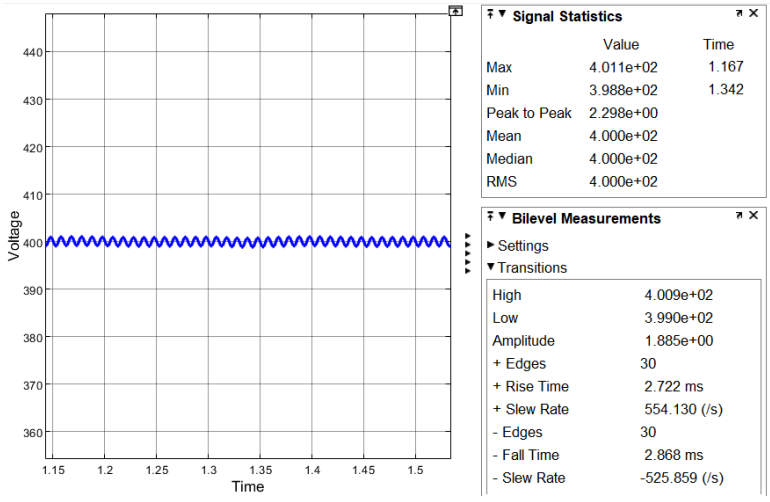

Fig. 8.14: DC Link voltage

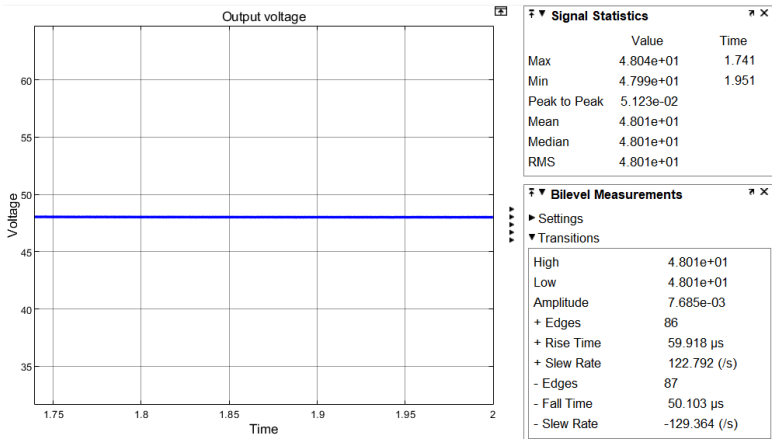

Fig. 8.15: Output voltage

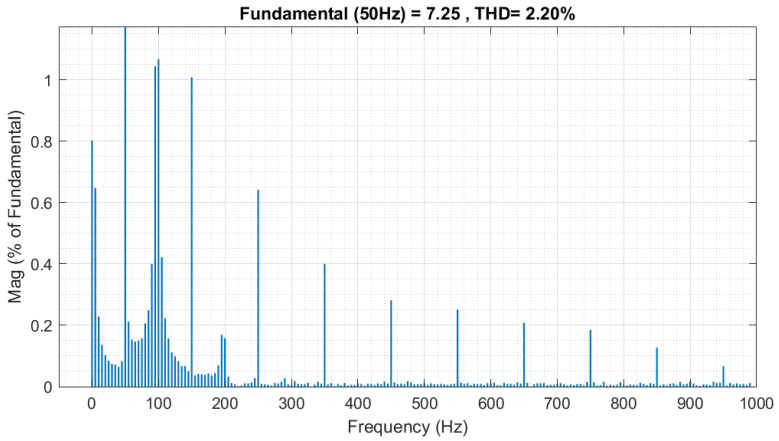

Fig. 8.16: Harmonic Analysis

T.H.D = 2.2% & pf = 0.99

8.3.2 Interleaved Boost PFC + PSFB

Using PI Controller

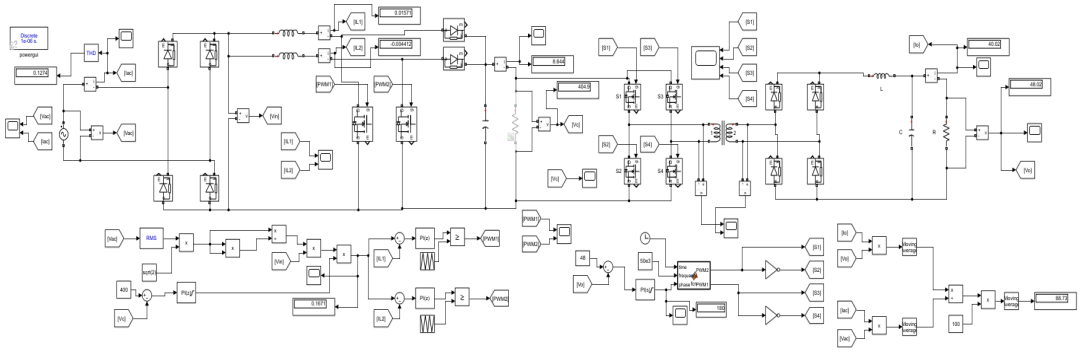

Fig. 8.17: Simulation circuit

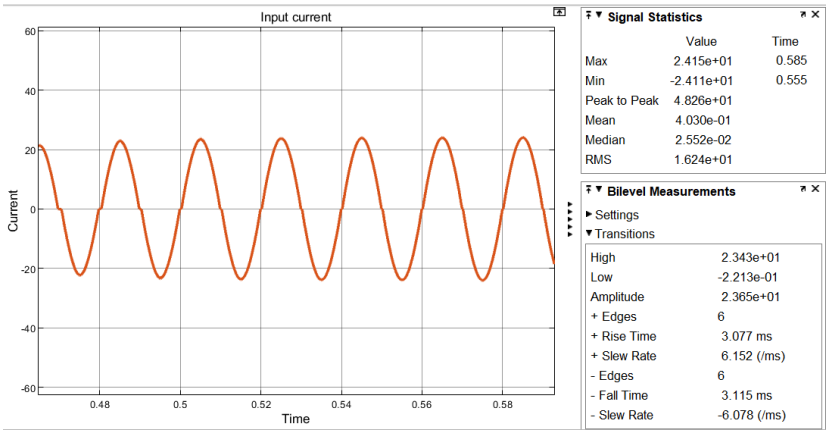

Fig. 8.18: Input current

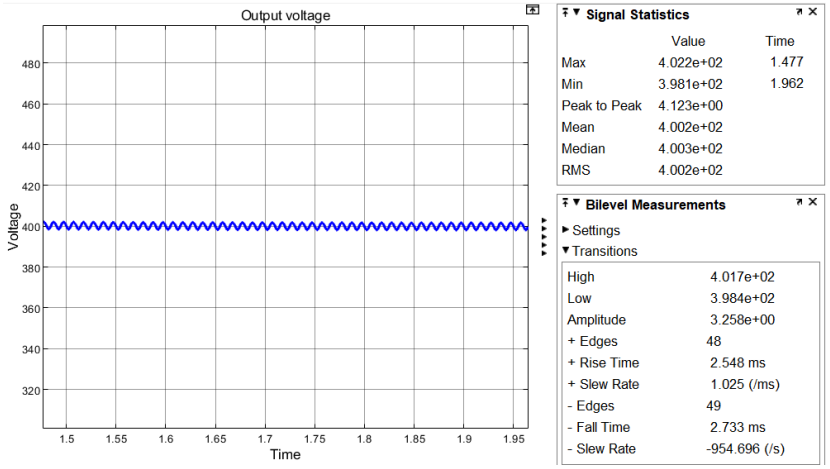

Fig. 8.19: DC Link voltage

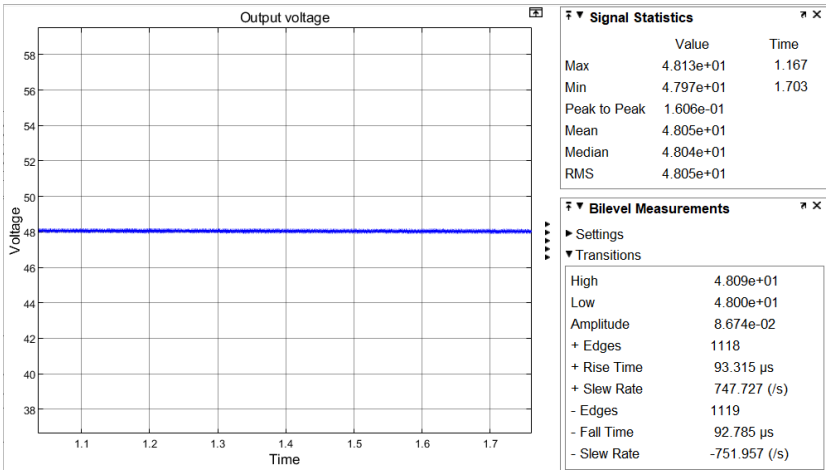

Fig. 8.20: Output voltage

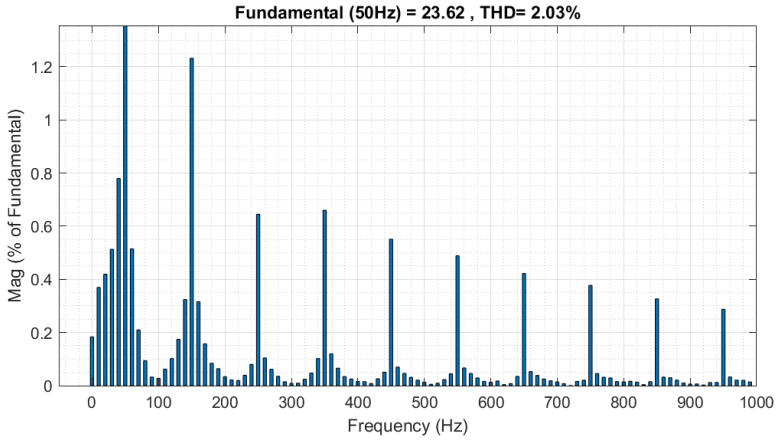

Fig. 8.21: Harmonic Analysis

T.H.D = 2% & pf = 0.999

Using PR Controller

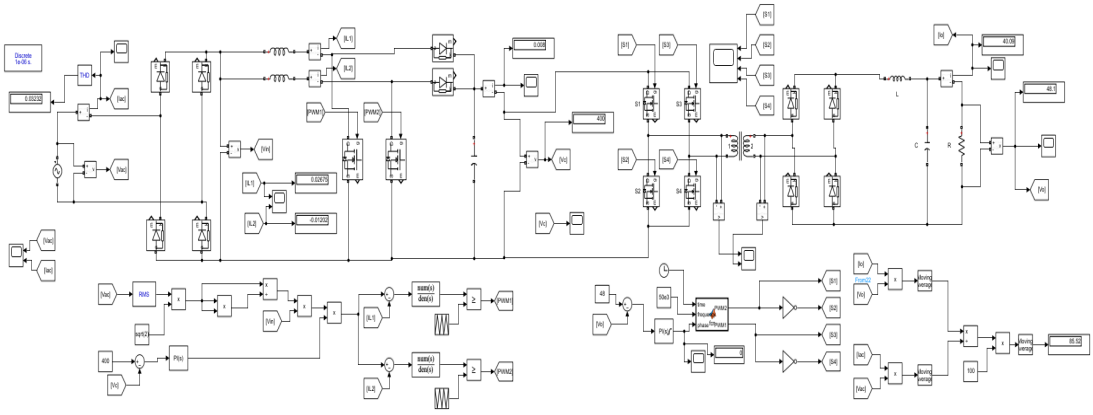

Fig. 8.22: Simulation circuit

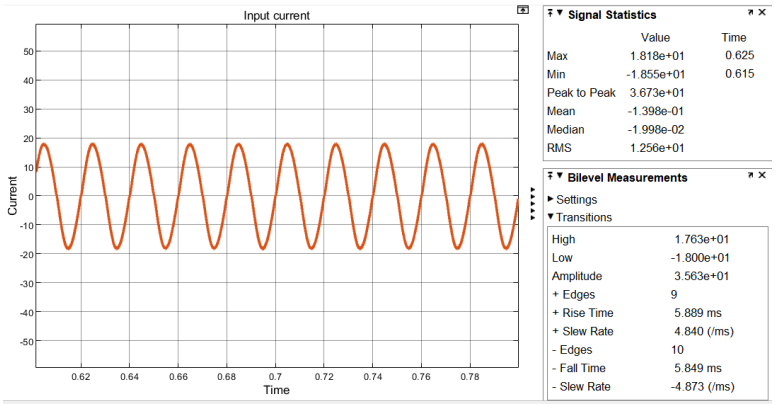

Fig. 8.23: Input current

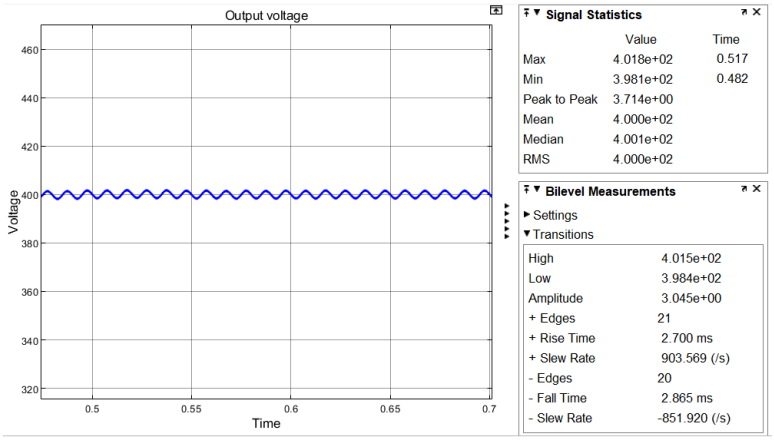

Fig. 8.24: DC Link voltage

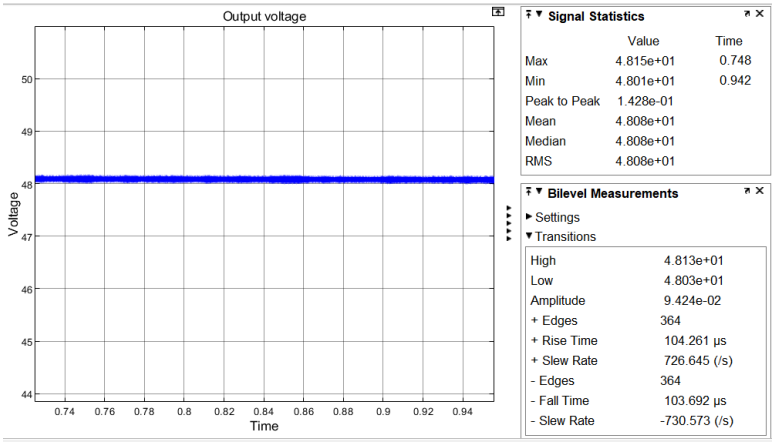

Fig. 8.25: Output voltage

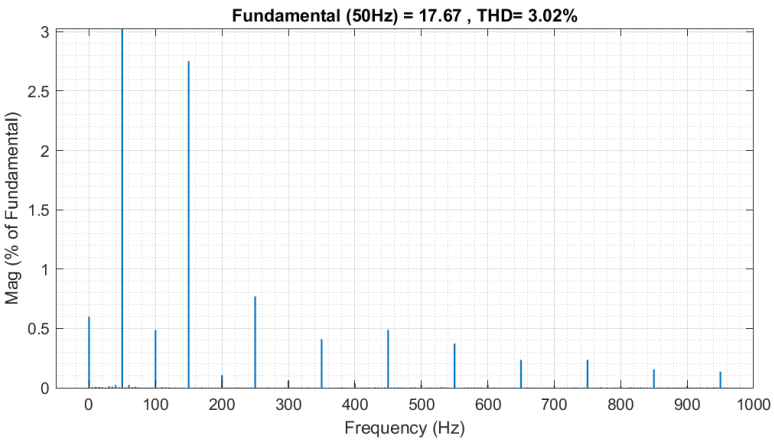

Fig. 8.26: Harmonic Analysis

T.H.D = 3% pf = 0.99

Tbl. 8.1: Overall Performance Comparison of Converter Topologies

Parameter	**Boost PFC with PI + FBC**	**Boost PFC with PR + FBC**	**Boost PFC with Lyapunov + FBC**	**IBC with PI + PSFB**	**IBC with PR + PSFB**
Power Factor	0.99	0.99	0.999	0.999	0.99
THD	2.58	3.1	2.2	2	3
Isolation	Yes	Yes	Yes	Yes	Yes
Efficiency	85%	83%	91%	87%	91%
EV Charger Suitability	Good	Good	Excellent	Good	Excellent

8.4 Comparison of PFC Converters

Boost PFC showed good voltage regulation, reasonably efficiency & unity power factor. However, ripple in current & voltage is more at high power operating conditions. [15] [21]

Tbl. 8.2: Comparison of PFC Converter Topologies

Parameter	**Boost PFC**	**Interleaved Boost PFC**	**Flyback PFC**
Input voltage	230 rms	230 rms	230 rms
Output voltage	400 V	400 V	400 V
Power Factor	0.99	0.998	0.98
THD	2.2	1.8	5.1
Efficiency (%)	95%	94%	85%
Output Voltage Ripple	Moderate	Low	Moderate
Input Current Ripple	Moderate	Very Low	High

The IBC was better than boost. As there is multiple number of phases operate in interleaved mode, ripple in current & voltage is low & good current sharing happened as well as the temperature of devices are distributed much better. Therefore IBC is best suited with high power EV charging.

The flyback PFC converter gives the benefit of galvanic isolation and circuit configuration is relatively simple. However, due to operate in the DCM, the current ripple and the harmonics distortion is more than boost based PFC converter, it is suitable for the low & medium rated charger.

8.5 Comparison of DC-DC Converters

Isolated DC-DC conversion was successfully achieved by the FBC with output voltage regulation at medium level applications.system was found to work effectively with good power handling capacity. However, hard-switching operation results in more switching losses and device stresses than the soft-switching systems.[19] [15]

Tbl. 8.3: Comparison of Isolated DC-DC Converters

Parameter	**FBC**	**PSFB**
Input voltage	400 V	400 V
Output Voltage	48 V	48 V
Power Rating	1 kW	2 kW
Transformer Isolation	Yes	Yes
Efficiency (%)	86%	91%
Voltage Regulation	Good	Excellent
High Power Suitability	Good	Excellent

Compared to FBC, PSFB was superior. Phase shift control mechanism in PSFB enables smooth transitions and soft switching. This significantly reduced the switching loss in the switching elements and improved efficiency compared to hard-switching systems. It was also shown to exhibit much less switching stresses and enhanced high power performance.

PSFB converter exhibits better efficiency and dynamic performance based on simulation which leads it as an excellent application in high power isolated EV charging system.

8.6 Conclusion

This Chapter presented the comparative study and total efficiency analysis of above mentioned converters. Presented simulation results, all designed converters were performing their operation as designed with the operating condition. Among all the studied PFC topology, Interleaved Boost PFC showed better overall characteristics with lower ripple, harmonic characteristics and power capability. For the studied isolated DC-DC converter, PSFB converter showed better efficiency, less switching loss and achieved soft switching. For combined EV charging system with IBC and PSFB converter, system showed steady state condition, high power quality, high efficiency for application in advanced EV charging system.

CHAPTER 9

CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

9.1 Conclusion

In this thesis, the designs, models, control and comparison of three types of PFC converters and two types of isolated DC-DC converters for EV charger application has been analyzed and the goal is to provide with good power quality and power transfer with efficiency and reliable power transmission via appropriate selection of converters and appropriate control of converters.

First three types of PFC converters such as Boost, IBC & Flyback topologies are modelled & simulatred. From results it is shows that the Boost PFC give adequate regulation in voltage as well as less harmonics, so power factor is improved, hence it is useful for medium rated applications. But IBC has very less ripple in current & voltage, which means it is suitable for higher power applications, & it gives with smooth input current also. Flyback PFC provides galvanic isolation and its power factor correction ability and performance were less in comparison with boost PFC as it works on DCM and harmonic is relatively more.

Next converters such as FBC & PSFB have been modelled, simulated and analyzed. FBC could be suits for medium and slightly high power levels with proper selection of converter topology, and good voltage regulation is achieved by this topology.Major drawbacks of FBC were the large switching loss occurring during the hard switching operations. For PSFB converter with phase shifted control, soft switching is achieved which considerably reduces the switching loss than FBC, thus good voltage regulation is provided at high power level. Results shows that PSFB gives a better performance than FBC.

Overall, all the converters are compared on the basis of efficiency, power factor, ripple content and voltage regulation. Among the input PFC stage, boost PFC with Lyapunov controller shows better results & also interleaved boost converter gives the best performance since the input current is practically without ripple and harmonic free. PSFB shows a better efficiency compared to FBC. Hence, entire system comprising of boost PFC with Lyapunov + FBC & IBC + PSFB showed better overall performance with good voltage regulation and higher power quality.

9.2 Future Scope

Despite the acceptable simulation performance of the presented EV charging system, a number of future research and extension issues have been identified.

The proposed converter topologies should be implemented on the hardware platform so that practical results can be obtained & compared with results from simulation. Based on implemented system, extensive experiment could be conducted on the switching losses, thermal performance, EMC interference, components tolerances, etc.

The presented charging system could also be extended for bidirectional power flow for V2G and V2H purpose. So that EV battery could be used for the smart energy management or grid support services.

Further studies may be made to employ [8]WBG semiconductor devices such as SiC or GaN [8] switch to realize high frequency and smaller size power converter as well as high efficiency system performance.

Also, a comprehensive design can be developed on a renewable energy assisted system. For example a photovoltaic or battery energy storage system coupled with the developed EV charger, to build a sustainable and energy-efficient charging infrastructure.

Based on the above studies and results of this thesis, it is reasonable to draw conclusion that a high performance EV charging system based on the proposed circuit topology and control scheme has been designed and successfully simulated, which also has great potential on further research and implementation on the hardware platform.

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