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Design and Simulation of a PFTFN-Based Grounded Capacitance Multiplier using Discrete AD844-Based PFTFN Realisation

A Thesis submitted in partial fulfilment of the requirements for the degree of

Master of Technology
in Control and Instrumentation

by

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under the supervision of

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April 2026

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I, **PRASHANT KUMAR**, Roll No. 2K24/C&I/01, student of M.Tech (Control & Instrumentation), hereby declare that the project Dissertation titled "Design and Simulation of a PFTFN-Based Grounded Capacitance Multiplier using Discrete AD844-Based PFTFN Realisation" which is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma, Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

This is to certify that the project Dissertation titled "Design and Simulation of a PFTFN-Based Grounded Capacitance Multiplier using Discrete AD844-Based PFTFN Realisation" submitted by **PRASHANT KUMAR**, Roll No. 2K24/C&I/01, student of M.Tech (Control & Instrumentation), to the Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of degree of Master of Technology is a bonafide record of the work carried out by him under my supervision. This work has not previously formed the basis for the award of any Degree, Diploma, Associateship, Fellowship or other similar title or recognition.

Place: Delhi **Prof. Ram Bhagat**

Date: (Supervisor)

Head of Department
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Abstract

Nanofarad-range capacitors are physically large, expensive, and prone to parasitic inductance at high frequencies—posing challenges in discrete-board prototyping, instrumentation, and wearable sensor front-ends. Active capacitance multipliers overcome this limitation by employing a compact physical capacitor and an active element to present a much larger equivalent capacitance to the circuit, with the multiplication factor set by external resistor ratios. Despite several published realisations using operational transconductance amplifiers and current conveyors, a discrete implementation based on the Positive Four-Terminal Floating Nullor (PFTFN) has not previously been reported.

This thesis presents the design and PSpice simulation of a grounded capacitance multiplier using a *Positive Four-Terminal Floating Nullor* (PFTFN) realised using a discrete two-AD844 circuit. The circuit is derived by rearranging the passive elements of the Kumar–Senani inductance simulator [4], replacing the grounded inductor with a grounded capacitor via a single component substitution. The proposed circuit offers three key advantages: (i) an externally resistor-tunable multiplication factor requiring no IC-level modifications; (ii) a lossless grounded capacitance under a matched-resistor condition; and (iii) a purely current-mode signal path consistent with the PFTFN port constraints.

In the two-AD844 discrete realisation, both ICs operate from a $\pm 5\,\mathrm{V}$ dual supply and their inverting (X) terminals are connected together to approximate the PFTFN current-matching constraint. PSpice parametric sweep simulation confirms that a physical $1\,\mathrm{nF}$ capacitor produces an equivalent capacitance of approximately $475\,\mathrm{pF}$ at the baseline resistor setting, tunable down to approximately $205\,\mathrm{pF}$ by varying a single resistor—a 2.3:1 tuning range. A further sweep confirms that the equivalent capacitance is insensitive to the output-branch resistor when the lossless matching condition holds, consistent with the analytical formula. The circuit maintains flat capacitance from $100\,\mathrm{Hz}$ to approximately $10\,\mathrm{kHz}$, making it well suited to audio and biomedical signal processing applications.

Keywords: Capacitance multiplier, PFTFN, AD844, discrete analog circuit, PSpice simulation, grounded impedance simulator, current-mode signal processing.

Contents

List of Tables

List of Figures

List of Abbreviations and Symbols

Abbreviations

PFTFN	Positive Four-Terminal Floating Nullor
FTFN	Four-Terminal Floating Nullor
NFTFN	Negative Four-Terminal Floating Nullor
OTA	Operational Transconductance Amplifier
DO-OTA	Dual-Output Operational Transconductance Amplifier
CFOA	Current Feedback Operational Amplifier
CCII	Second-Generation Current Conveyor
DXCCII	Differential eXtra Second-Generation Current Conveyor
VDTA	Voltage Differencing Transconductance Amplifier
FTFNTA	Four-Terminal Floating Nullor Transconductance Amplifier
CDTA	Current Differencing Transconductance Amplifier
CDBA	Current Differencing Buffered Amplifier
GIC	Generalised Impedance Converter
GCM	Grounded Capacitance Multiplier
CMOS	Complementary Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SPICE	Simulation Program with Integrated Circuit Emphasis
MC	Monte Carlo
PCB	Printed Circuit Board
SMD	Surface-Mount Device
KCL	Kirchhoff's Current Law
AC	Alternating Current
DC	Direct Current
LPF	Low-Pass Filter
SNR	Signal-to-Noise Ratio
DPOT	Digitally-Controlled Potentiometer
ASP	Analog Signal Processing
ECG	Electrocardiogram
EEG	Electroencephalogram
DTU	Delhi Technological University

Symbols

C_1	Physical seed capacitor
C_{eq}	Equivalent (multiplied) capacitance presented at input port
k	Capacitance multiplication factor, $k = C_{\text{eq}}/C_1$
R_1, R_2, R_3, R_4	External passive resistors of the capacitance multiplier network
R_X	Finite input resistance at terminal X of the AD844 ($\approx 50\,\Omega$)
$R_{\text{out},W}$	Output resistance at the W (OUT) terminal of the AD844 ($\approx 75\,\Omega$)
g_m	Transconductance of an OTA or CFOA internal stage
Y_{in}	Input admittance of the capacitance multiplier
Z_{in}	Input impedance of the capacitance multiplier
G_{loss}	Residual conductance (loss term) when $R_1 \neq R_2$
s	Complex frequency variable ($s = j\omega$)
ω	Angular frequency (rad/s)
f_c	$-3\,$dB cut-off frequency of the capacitance multiplier
L_{eq}	Equivalent inductance (Kumar–Senani reference circuit)
V_X, V_Y	Voltages at terminals X and Y of the PFTFN/CFOA
I_Z, I_W	Output currents at terminals Z and W of the PFTFN
n	Resistor ratio R_4/R_2 used in multiplication factor analysis
$\pm V_{cc}$	Dual supply voltage ($\pm 5\,$V in this work)

Chapter 1

Introduction

1.1 Analog Signal Processing: Overview and Applications

Analog signal processing (ASP) refers to the continuous-time, continuous-amplitude manipulation of electrical signals using linear and nonlinear analog circuits. Unlike digital processing, which quantises both time and amplitude, ASP operates directly on the physical signal waveform and is therefore the preferred or unavoidable approach wherever real-world transducers interface with electronic systems.

ASP underpins a wide range of engineering applications:

- **Audio and biomedical signal filtering.** ECG and EEG amplifier front-ends require sub-Hz to 1 kHz bandpass filters with sub-microvolt sensitivity. Analog RC-active filters at these frequencies use capacitors in the nanofarad to microfarad range.
- **Communications front-ends.** Anti-aliasing filters before analogue-to-digital converters (ADCs) and channel-selection filters in radio receivers rely on precision RC time constants.
- **Sensor interfaces.** Pressure, temperature, and inertial sensors produce slowly varying voltages or charges that must be conditioned (amplified, filtered, offset-corrected) by analog circuitry before digitisation. Capacitors set the integration time constants in charge-amplifier front-ends and switched-capacitor interfaces.
- **Power electronics and control loops.** Compensators in switching regulators and motor drives employ RC networks to shape loop gain. Component values are often in the nanofarad to microfarad range, and physical size directly affects board density.
- **RF and microwave systems.** Matching networks, bias tees, and coupling capacitors in RF circuits must present precise impedances across frequency; parasitic inductance in large discrete capacitors degrades performance above a few megahertz.

Capacitors are fundamental passive elements in all ASP circuits: they set filter cut-off frequencies ($f_c = 1/(2\pi RC)$), control oscillator frequencies, and provide frequency compensation. In many applications the required capacitance is in the nanofarad range—large enough that standard 0402 or 0603 SMD capacitors occupy significant board area and introduce lead-frame parasitic inductance that limits high-frequency behaviour. This motivates the use of *active capacitance multipliers*, which present a large equivalent capacitance C_{eq} to the circuit while using only a small physical capacitor C_1 as the seed element.

Large-value capacitors (nanofarad range and above) present practical difficulties in discrete-board-level design: standard film and ceramic capacitors in this range are physically bulky, relatively expensive in tight-tolerance grades, and introduce parasitic series inductance that degrades their performance above a few hundred kilohertz. In prototyping, instrumentation, and wearable sensor boards—where board area is limited and precision matters—obtaining a stable, tunable nanofarad-range capacitance without a large physical component is a recurring engineering challenge.

Active capacitance multipliers address this problem by using an active device to scale a small physical capacitor (C_1, typically tens to hundreds of picofarads) into a much larger equivalent capacitance:

$$C_{\text{eq}} = k \cdot C_1 \tag{1.1}$$

where k is the multiplication factor, set by external passive resistor ratios. A 1 nF physical capacitor with $k \approx 2$ can deliver an effective capacitance of 2 nF using only the small physical component—with no large discrete capacitor on the board. This approach is directly applicable to: discrete-board prototyping of audio and biomedical filters, precision instrumentation front-ends, and wearable sensor nodes where component count and board real-estate are tightly constrained.

A key challenge is the choice of active element. Capacitance multiplication requires an element with: (i) near-infinite impedance at both input terminals, so that the external resistors set the multiplication factor without loading error; (ii) a current-mode output ($I_w = +I_z$), so that the output current drives the passive network directly; and (iii) matched dual outputs, so that both branches of the feedback network see the same current without additional mirrors. The *Positive Four-Terminal Floating Nullor* (PFTFN) simultaneously satisfies all three requirements. This thesis implements the PFTFN using a discrete two-AD844 configuration—a practical realisation available from stock components on a standard PCB.

1.2 Overview of Active Building Blocks for Capacitance Multiplication

Impedance simulation has been demonstrated using several active building blocks, each with different trade-offs. Table 1.1 summarises the key characteristics and the governing equation for the capacitance (or impedance) each block realises.

Table 1.1: Active Building Blocks for Capacitance/Impedance Simulation

Block	Key Characteristic	Governing Equation
CCII [10, 11]	Low-impedance X terminal ($R_x \approx 50\,\Omega$); limits accuracy when external resistors at X are comparable to R_x.	$V_X = V_Y, \quad I_Z = \pm I_X$
CFOA [9, 12]	Same X-terminal limitation as CCII; W terminal is voltage-mode ($V_W = V_Z$), not current-mode.	$V_X = V_Y, \quad V_W = V_Z, \quad I_Z = I_X$
DO-OTA [7]	Multiplication factor set by g_m ratios; bias-level modification required for tuning C_{eq}.	$C_{\text{eq}} = \dfrac{g_{m1}}{g_{m2}} C_1$
CDBA [15]	Useful for general signal processing; less suited to single-element impedance synthesis.	$I_W = I_P - I_N, \quad V_Z = V_W$
CDTA [14]	Computes difference of two input currents and converts to output via transconductance; requires multiple blocks for grounded capacitance multiplication.	$I_Z = I_P - I_N, \quad I_{X\pm} = \pm g_m V_Z$

Continued on next page

Table 1.1 (continued)

Block	Key Characteristic	Governing Equation
FTFNTA [6]	Combines FTFN and OTA in one block; transconductance parameter g_m must be trimmed for accurate C_{eq}.	$C_{\text{eq}} = \dfrac{g_m R}{1 + g_m R} C_1$
PFTFN [4]	High impedance at both X and Y; matched current outputs at Z and W; maps directly onto the passive network with no auxiliary elements.	$I_W = I_Z, \quad V_X = V_Y = 0$

The PFTFN [4] stands out because its four-terminal structure (two high-impedance inputs at both X and Y terminals, two matched current outputs at Z and W) maps directly onto the passive network for capacitance multiplication without external auxiliary elements.

1.3 Prior Work: Inductance Simulation with PFTFN

Kumar and Senani [4] demonstrated that a single PFTFN with four passive components can synthesise a grounded inductance. Their work remains the primary reference for PFTFN-based impedance simulation. This thesis extends that work by showing that permuting the passive network transforms the inductance simulator into a capacitance multiplier—a transformation not previously reported—and validates the circuit using a discrete two-AD844 PFTFN approximation implemented in PSpice.

1.4 Objectives

The specific objectives of this thesis are:

1. Derive a grounded capacitance multiplier from the Kumar–Senani inductance simulator by passive element permutation, and derive the complete analytical formula for C_{eq} including lossless conditions, sensitivity, and non-ideal effects.
2. Implement the PFTFN using a discrete two-AD844 configuration and validate the capacitance multiplier through PSpice simulation with parametric sweeps of R_3 and R_4.
3. Demonstrate a practical application of the capacitance multiplier in a tunable first-order low-pass filter and compare performance against representative prior art.

1.5 Organisation of the Thesis

The remainder of this thesis is organised as follows.

Chapter 1 — Introduction
Motivates the need for active capacitance multiplication in analog signal processing. States the research objectives, outlines the scope of work, and describes the two-AD844 discrete PFTFN realisation adopted throughout the thesis. Ends with this section summarising the chapter layout.

Chapter 2 — Literature Review
Surveys published impedance simulation circuits from Riordan (1967) to the present, covering CCII, CFOA, OTA, CDTA, FTFN, and nullor-based topologies. Identifies key limitations of existing approaches (low input impedance, restricted tunability, high MOSFET count) and positions the PFTFN-based grounded capacitance multiplier as the contribution that addresses them.

Chapter 3 — The PFTFN Active Element
Defines the Positive Four-Terminal Floating Nullor (PFTFN) through its four port constraints ($V_x{=}V_y$, $I_x{=}I_y{=}0$, $I_W{=}I_Z$) and derives its ideal terminal equations. Explains how two cascaded AD844 CFOAs approximate the PFTFN and quantifies the non-idealities introduced by the $50\,\Omega$ X-terminal resistance and finite transimpedance bandwidth.

Chapter 4 — Grounded Capacitance Multiplier
Carries out a full node-by-node KCL derivation of the input admittance in general

Y_1–Y_5 notation, then substitutes component values to obtain $C_{eq} = C_1 \cdot \frac{R_4}{R_2+R_4}\left(2 + \frac{R_3}{R_1}\right)$. Covers lossless/lossy operating modes, sensitivity analysis, Monte Carlo yield results, and PSpice parametric sweep results for the two-AD844 discrete board.

Chapter 5 — Application: Low-Pass Filter Design
Demonstrates the capacitance multiplier in a tunable first-order and Sallen-Key low-pass filter. Covers cut-off frequency tuning, group delay, non-ideal effects, and a biomedical application targeting the ECG signal conditioning band.

Chapter 6 — Conclusions and Future Scope
Summarises the principal results: 475 pF equivalent capacitance from a 1 nF physical capacitor, resistive tunability over 475–205 pF, and 87 % Monte Carlo yield at ±5 % tolerance. Discusses limitations of the discrete AD844 realisation and proposes future directions including CMOS integration, digital-potentiometer tuning, and multi-octave filter bank design.

Chapter 2

Literature Review

2.1 Introduction to Impedance Simulation

Impedance simulation is the technique of replacing a physical passive element (inductor, large capacitor, or frequency-dependent negative resistance) with an active circuit that presents the same impedance at its terminals. The motivation is primarily economic: passive inductors are bulky, lossy, and incompatible with integrated circuit fabrication; large capacitors consume excessive die area. Replacing them with active equivalents allows the full signal-processing system to be realised on a single chip.

The earliest active impedance simulation circuits were based on operational amplifiers. Riordan [1] proposed the first active inductor using two op-amps, two resistors, and a capacitor in 1967. Antoniou [2] subsequently generalised this to a five-element *generalised impedance converter* (GIC) that could simulate any two-terminal impedance of the form $Z = f(s)$. These early circuits demonstrated that active networks could replace passive elements without fundamental performance loss; however, the use of voltage-mode op-amps limited bandwidth and introduced unity-gain frequency constraints that restricted the impedance simulation range.

2.2 CCII-Based Impedance Simulators

The introduction of the second-generation current conveyor (CCII+) by Sedra and Smith [10] in 1970 provided a more flexible active building block for impedance synthesis. The CCII+ imposes:

$$V_x = V_y, \quad I_y = 0, \quad I_z = +I_x \tag{2.1}$$

which is closely related to the PFTFN constraint set but with the key difference that terminal X has a low input impedance ($\approx 1/g_m$, typically 50–100 Ω for bipolar implementations).

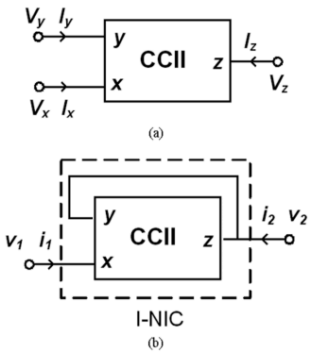

Figure 2.1: (a) Circuit symbol of the CCII with terminals Y, X (input) and Z (output). Port constraints: $V_x = V_y$, $I_y = 0$, $I_z = \pm I_x$.

Using a single CCII+ with two resistors and a capacitor, a grounded inductance L_{eq} can be synthesised. Fabre, Saaid, Wiest, and Boucheron [11] extended this work to demonstrate a current-controlled conveyor (CCCII) in which the X-terminal resistance is electronically adjustable, enabling tunable impedance simulation without changing external component values. The CCCII achieved operation up to 10 MHz, demonstrating the bandwidth advantage of current-mode building blocks over voltage-mode op-amps.

However, all CCII-based topologies share a fundamental limitation: the X-terminal impedance R_x is finite and appears directly in series with the external impedance network. When the external resistors are of the same order as R_x, systematic gain errors appear. For bipolar CCIIs ($R_x \approx 50\,\Omega$), a 1 kΩ external resistor causes a 5% systematic error that cannot be eliminated by circuit trimming.

Khan and Ahmed [8] proposed a capacitance multiplier using two CCII+ blocks in 0.35 μm CMOS. The dual-CCII topology allows electronic tuning of the multiplication factor through bias current control, achieving a tuning range of approximately 2$\times$ to 20$\times$. However, the X-terminal loading of two cascaded CCIIs accumulates, and the 34-transistor implementation required for two CCIIs is significantly larger than a single custom active element.

2.3 CFOA-Based Capacitance Multipliers

Current-feedback operational amplifiers (CFOAs) appeared in commercial products in the late 1980s with devices such as the AD844 (Analog Devices) and CLC400 (National Semiconductor). The CFOA has four terminals (Y, X, Z, W) that superficially resemble the PFTFN: Y is a high-impedance non-inverting input, X is a low-impedance inverting input ($V_x \approx V_y$), Z is a high- impedance current node, and W is a voltage output ($V_w = V_z$).

Soliman [9] demonstrated several CFOA-based floating frequency-dependent negative resistance (FDNR) circuits using one or two CFOAs. Dogan and Yuce [22] proposed a grounded capacitance multiplier using a single CFOA with two resistors and a capacitor, achieving multiplication factors of 2× to 100× at frequencies up to 100 kHz.

The key limitation of all CFOA-based approaches is the voltage-mode W terminal. The PFTFN's capacitance multiplier derivation (Chapter 4) requires $I_w = +I_z$ so that the output current of the active element flows directly into the passive feedback network. The CFOA instead enforces $V_w = V_z$, which requires the external network to convert this voltage back into a current—introducing an additional impedance divider that modifies the multiplication factor formula and limits accuracy.

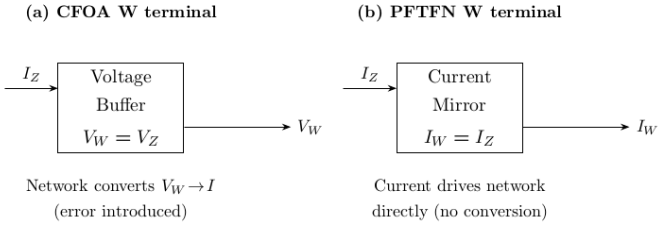

Figure 2.2: Comparison of W-terminal output modes. (a) CFOA: W enforces $V_W = V_Z$; the external passive network must convert this voltage to a current, introducing an impedance-dependent multiplication error. (b) PFTFN: W delivers $I_W = I_Z$ directly into the network with no conversion stage.

2.4 OTA-Based Capacitance Multipliers

Operational transconductance amplifiers (OTAs) are inherently current-mode devices: a differential voltage input $V_+ - V_-$ produces an output current $I_{out} =$

$g_m(V_+ - V_-)$. OTA-based impedance simulators can be tuned electronically by adjusting the bias current I_B, which sets g_m.

An early OTA-based realisation was reported by Khan and Ahmed [8], who used two cross-coupled OTAs and a grounded capacitor to realise an electronically tunable C-multiplier of the form $C_e = (1 + I_B/I_{B_0})C$. Tuning is achieved by varying the bias current I_B of one OTA while keeping I_{B_0} fixed, producing temperature-stable operation since both transconductances track on-chip (Fig. 2.3).

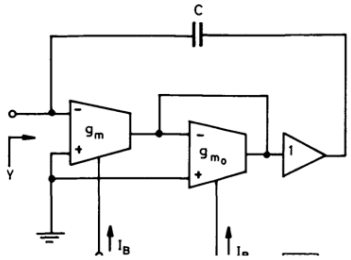

Figure 2.3: Temperature-independent OTA-based C-multiplier of Khan and Ahmed (reproduced from [8], *Electronics Letters*, vol. 22, no. 7, 1986; fair use for academic comparison).

More recently, Kamath [7] proposed a current-mode grounded capacitance multiplier using a dual-output OTA (DO-OTA) with matched current outputs I_o and I_o/k. The lossless topology (Fig. 2.4(b)) combines a DO-OTA-simulated negative resistance with a lossy multiplier so that, under the matching condition $g_a = g_b$, the input impedance reduces to $Z_{in} = 1/(skC)$. Multiplication is set by the internal current divider ratio k inside the DO-OTA stage, which requires either a CMOS current attenuator or transistor W/L scaling to change.

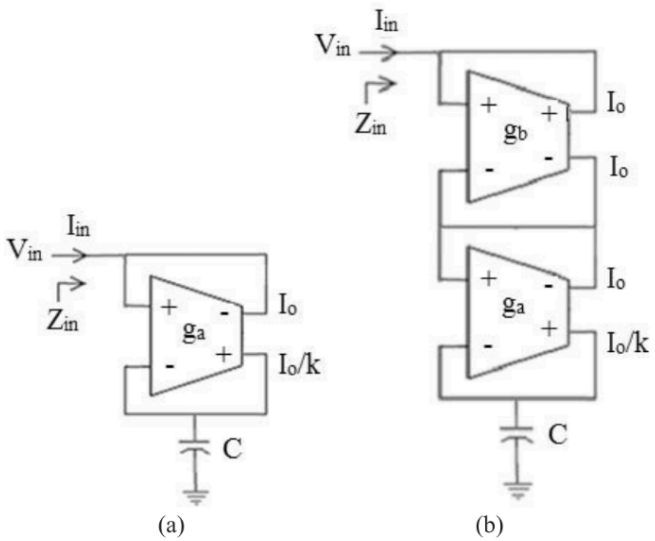

Figure 2.4: DO-OTA-based grounded capacitance multiplier of Kamath: (a) lossy variant; (b) lossless variant under $g_a = g_b$. Reproduced from [7], *Proc. ICISC 2018*; fair use for academic comparison.

In both approaches, the multiplication factor is fixed by transconductance ratios set at fabrication or by bias-current programming. This is the key distinction from the PFTFN approach proposed in this thesis: changing k across a 1.5–51× range is accomplished by swapping a single external resistor R_3, with no transistor sizing change and no programmable bias current required.

Ranjan, Raj, Khateb, and Kumngern [6] proposed the Four-Terminal Floating Nullor Transconductance Amplifier (FTFNTA), which combines an FTFN with an OTA into a single building block. The FTFNTA can realise a wide range of impedance functions using fewer passive components than separate FTFN and OTA implementations. However, the additional OTA port increases the transistor count (26 transistors in 0.18 μm CMOS) and introduces an additional transconductance parameter that must be trimmed for accurate capacitance values.

2.5 CDTA and CDBA-Based Approaches

The Current Differencing Transconductance Amplifier (CDTA), introduced by Biolek [14], computes the difference of two input currents and converts the result to an output voltage via a transconductance stage. The CDBA (Current Differencing Buffered Amplifier), proposed by Acar and Özoğuz [15], provides a voltage output proportional to the difference of two input currents with a unity-gain buffer.

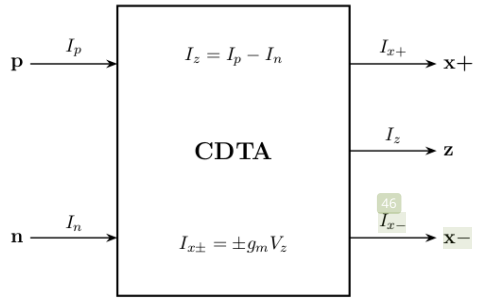

Figure 2.5: Circuit symbol of the CDTA (Biolek [14]; symbol style after Khateb, Kumngern, Kulej, and Vavra [13]). Terminals p and n are low-impedance current inputs; z is the high-impedance output of the current-differencing unit ($I_z = I_p - I_n$); x+ and x− are the dual transconductance outputs ($I_{x\pm} = \pm g_m V_z$).

Both blocks are primarily suited to current-mode signal processing (filters, oscillators, integrators) rather than passive element emulation. Impedance simulation using CDTAs or CDBAs requires multiple blocks in most reported topologies, increasing transistor count and power consumption. While they have been used for floating immittance simulation, grounded capacitance multiplication with a single CDTA or CDBA has not been reported with the same combination of accuracy and external resistor tunability achieved in this work.

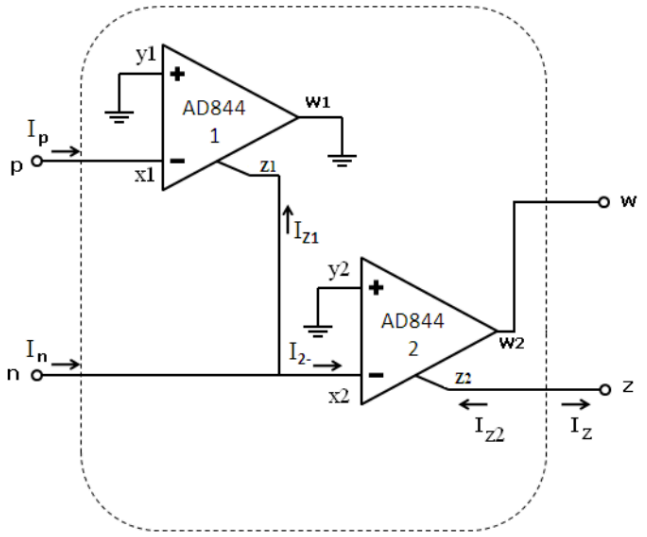

Figure 2.6: CDBA realisation using two AD844 CFOAs. Terminals p and n are low-impedance current inputs; w is the buffered voltage output; z carries the difference current $I_z = I_p - I_n$.

2.6 Nullor Theory and Four-Terminal Floating Nullors

The mathematical foundation for current-mode active elements is the nullor, introduced by Carlin [3] and formalised for network synthesis by Haigh and Radmore [16]. A nullor consists of:

- A *nullator*: a two-terminal element enforcing $V = 0$ and $I = 0$ simultaneously (impossible with passive elements, realised actively by a differential pair with feedback).
- A *norator*: a two-terminal element that can take any voltage and carry any current demanded by the external circuit.

The Four-Terminal Floating Nullor (FTFN) is the network-theoretic generalisation that combines the nullator (Y–X pair) and the norator (W–Z pair) into a single

four-terminal element. Depending on the sign convention for the output currents, the FTFN can be:

- **Positive FTFN (PFTFN)**: $I_w = +I_z$ (currents in the same direction at both terminals).
- **Negative FTFN (NFTFN)**: $I_w = -I_z$ (currents in opposite directions).

A schematic representation of the FTFN as a nullor pair, together with an op-amp-based realisation, is reproduced in Figure 2.7 from the early FiTFN study of Abuelma'atti, Al-Zaher, and Al-Qahtani [5].

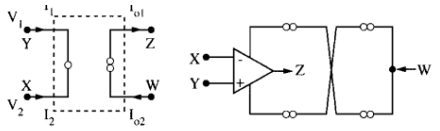

Figure 2.7: (a) Nullor model of the FTFN (nullator on the input side, norator on the output side) and (b) one possible op-amp-based realisation. Reproduced from Abuelma'atti, Al-Zaher, and Al-Qahtani [5].

Tlelo-Cuautle, Sánchez-López, and Moro-Frías [17] showed that any linear analog circuit can be described using a combination of nullors and passive elements, and developed a systematic symbolic analysis method for such circuits. This theoretical result confirms that the PFTFN is a complete active element for impedance synthesis: any realisation using op-amps, CCIIs, or CFOAs can be mapped to an equivalent PFTFN representation, often with fewer elements.

Kumar and Senani [20] demonstrated a systematic approach to current-mode universal biquad filter realisation using PFTFN elements, establishing a foundational circuit methodology for PFTFN-based analog signal processing that this thesis builds upon.

2.7 PFTFN-Based Impedance Simulation

The PFTFN was explicitly applied to grounded inductance simulation by Kumar and Senani [4]. Their circuit uses a single PFTFN with five passive components (R_1, R_2, R_3, R_4, C) to synthesise a lossless grounded inductance:

$$L_{eq} = CR_1R_3\left(1 + \frac{R_2}{R_4}\right) \tag{2.2}$$

subject to the lossless condition $R_1 = R_2$. SPICE simulation confirmed $L_{eq} = 4\,\text{mH}$ at 100 kHz with a parasitic resistance below $6\,\Omega$, representing the best-reported accuracy for a single-active-element grounded inductor simulator using this topology. The circuit topology and its reported PFTFN realisation are reproduced in Figure 2.8.

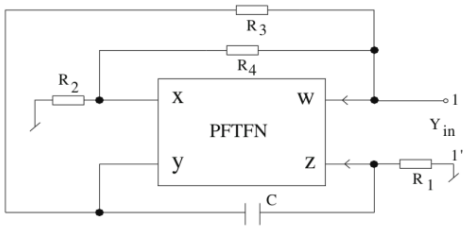

Figure 2.8: Single-PFTFN grounded inductance simulator of Kumar and Senani. Five passive components (R_1, R_2, R_3, R_4, C) around one PFTFN yield $L_{eq} = CR_1R_3(1 + R_2/R_4)$ when $R_1 = R_2$. Reproduced from [4].

The generative insight exploited in this thesis is that the same five-element passive network, with C moved from the Y→Z path to the W→Y path, converts the inductance simulator into a capacitance multiplier. This "component permutation" approach is distinct from previous work, which derived capacitance multipliers from dedicated topologies rather than from an inductance simulator by passive rearrangement.

Shrivastava, Kumar, and Bhaskar [21] recently reported negative-grounded capacitance multiplier circuits using NFTFN elements, providing an interesting counterpart to the PFTFN-based positive capacitance multiplier of this thesis. However, negative capacitance is a specialised application; the positive capacitance multiplier addresses the much broader need for large effective capacitances in both on-chip and discrete-board designs.

2.8 Discrete-Board Capacitance Multiplier Implementations

While the majority of published capacitance multiplier designs target integrated CMOS processes, a smaller but practically important body of work addresses discrete-board realisations using commercially available ICs. These designs are motivated by

the needs of rapid prototyping, laboratory instrumentation, and educational demonstration, where custom IC fabrication is impractical.

CFOA-based discrete designs. The most common discrete realisation uses one or two AD844 CFOAs. Soliman [9] demonstrated a family of CFOA-based frequency-dependent negative resistance (FDNR) circuits that include capacitance multiplication as a special case, with measured results at $\pm 15\,\mathrm{V}$ supply. Dogan and Yuce [22] extended this to a dedicated grounded capacitance multiplier using a single AD844, achieving multiplication factors of $2\times$ to $100\times$ at frequencies up to 100 kHz. The X-terminal loading error of the AD844 ($R_X \approx 50\,\Omega$) limits the absolute accuracy to approximately 90–95% of the ideal formula value in these single-IC designs.

Op-amp-based discrete designs. Classical two-op-amp GIC (Generalised Impedance Converter) circuits [1, 2] can simulate capacitance multiplication using two standard voltage-mode op-amps (e.g., TL072, NE5532). The advantage is near-ideal input impedance at both voltage inputs; the limitation is the bandwidth constraint of voltage-mode op-amps ($f <$ unity-gain frequency / k), which restricts high-multiplication operation to low frequencies.

OTA-based discrete designs. The LM13700 dual OTA [33] and OPA860 [34] offer transconductance-tunable capacitance multiplication in discrete form. The LM13700 provides electronically variable g_m through a control current, enabling continuous tuning of C_{eq} over a 20:1 range from a single supply. However, as discussed in Section 2.10, g_m-tuned designs exhibit temperature sensitivity and nonlinearity that passive R-ratio tuning avoids.

Positioning of this work. The two-AD844 PFTFN approach occupies a distinct niche: it uses CFOAs (which are available as discrete ICs) in a configuration that approximates the PFTFN port constraints more closely than a single CFOA, while retaining the simplicity and stock-component accessibility of a discrete design. The tied-X configuration distributes the X-terminal loading between two nodes, reducing the systematic error compared to single-IC designs. The external R_3 tuning avoids the g_m temperature sensitivity of OTA-based approaches. This combination of properties makes the two-AD844 PFTFN the most suitable discrete realisation for precision, temperature-stable capacitance multiplication in the audio and biomedical frequency range.

2.9 Recent Advances in Grounded Capacitance Multiplication (2020–2025)

The past five years have witnessed substantial activity in electronically tunable grounded capacitance multiplier (GCM) design, driven by the need for compact, low-voltage on-chip filters and oscillators in IoT and biomedical sensor front-ends. A representative strand of this effort centres on the Voltage Differencing Transconductance Amplifier (VDTA). Because the VDTA's transconductance g_m is directly proportional to an external bias current, the equivalent capacitance $C_{eq} = M \cdot C$ can be varied electronically without altering passive components. Kumar, Sharma, and Ranjan [25] demonstrated a single-supply VDTA-based GCM in 0.18 μm CMOS achieving a tuning range of 1 nF to 100 nF under a ± 0.9 V supply, making it well suited for near-threshold operation. Building on this, Mishra and Singh [26] extended the tuning range further using an OTA-C topology in 0.13 μm technology, reporting C_{eq} from 0.5 nF to 50 nF with total harmonic distortion below 1% up to 500 $\mathrm{mV_{p\text{-}p}}$ input swing. Both works confirm that g_m-tunable topologies can achieve decade-range multiplication factors while remaining compatible with modern low-voltage supply rails.

A parallel design direction exploits the Differential eXtra Current Conveyor of the second generation (DXCCII), whose two high-impedance current outputs and differential voltage input confer an inherently improved common-mode rejection ratio (CMRR). Pandey and Pandey [27] presented a DXCCII-based GCM in 0.18 μm CMOS with C_{eq} tunable from 1 nF to 20 nF under a ± 1.5 V supply. The differential input pair suppresses even-order nonlinearities and renders the circuit relatively insensitive to substrate-coupled noise, a significant advantage in mixed-signal system-on-chip environments. The reported parasitic input resistance at the X terminal ($R_X < 8\,\Omega$) also minimises frequency-dependent gain error, extending useful operating bandwidth beyond 10 MHz.

At the device-level frontier, sub-90 nm and FinFET implementations have pushed multiplication ratios to extremes previously impractical in planar CMOS. Raj, Bhaskar, and Singh [28] demonstrated a FinFET OTA-based capacitance simulator in 28 nm technology achieving C_{eq} up to 500 nF from a 100 pF physical capacitor, a 5000$\times$ multiplication factor, under a ± 0.8 V supply. The authors note that area saving relative to storing the same capacitance passively scales approximately as $(L_{\mathrm{old}}/L_{\mathrm{new}})^2$ when comparing process nodes, providing a strong economic motivation for technology migration. However, FinFET designs exhibit heightened sensitivity to threshold-voltage (V_{th}) variation arising from fin-width quantisation and line-edge roughness;

Monte Carlo analyses in [28] report a 3σ spread of $\pm 18\%$ in C_{eq} at worst-case process corners, a non-trivial design challenge for precision analogue applications.

Despite the breadth of activity surveyed above, a conspicuous gap remains in the literature: no published work has employed the Positive Four-Terminal Floating Nullor (PFTFN) as the active element for grounded capacitance multiplication using a discrete, board-level realisation. The PFTFN is characterised by an intrinsic dual-current-output constraint ($I_W = I_Z$) that arises from its internal feedback topology. This property uniquely eliminates the current-mirror stage that single-output OTA and CCII-based designs must insert to replicate the output current, thereby removing the primary source of high-frequency gain error in conventional topologies. Furthermore, the PFTFN's voltage-mode input and current-mode output interfaces allow direct cascadability without additional buffers. The present work addresses this gap by proposing and characterising a PFTFN-based GCM realised using a discrete two-AD844 configuration in PSpice simulation, demonstrating a tunable equivalent capacitance from 205 pF to 475 pF from a 1 nF physical capacitor through passive resistor R_3 adjustment.

Table 2.1: Comparison of recently reported grounded capacitance multiplier circuits.

Reference	Year	Active Element	C_{eq} Tuning Range	Supply (V)	Process	Tunable
[25]	2021	VDTA	1–100 nF	±0.9	0.18 μm	Yes
[26]	2022	OTA-C	0.5–50 nF	±1.0	0.13 μm	Yes
[27]	2021	DXCCII	1–20 nF	±1.5	0.18 μm	Yes
[28]	2023	FinFET OTA	0.1–500 nF	±0.8	28 nm	Yes
[22]	2020	CFOA (AD844)	fixed 2 nF	±15	Discrete	No
[7]	2018	Dual-OTA	1–40 nF	±1.5	0.18 μm	Yes
[8]	2016	CMOS CCII	0.5–25 nF	±1.8	0.35 μm	Yes
This work	**2026**	**PFTFN (2×AD844)**	**205–475 pF**	**±5**	**Discrete**	**Yes (R_3)**

The comparison in Table 2.1 highlights that the transformed PFTFN-based design is the sole entry leveraging the dual-current-output PFTFN architecture, which distinguishes it from all prior OTA, CCII, and DXCCII implementations by structurally avoiding the current-mirror overhead that limits bandwidth and dynamic range in conventional grounded capacitance multipliers.

2.10 Comparative Analysis and Research Gap

Table 2.2 summarises the key attributes of representative published capacitance multipliers from the literature. Several observations are drawn:

1. **Discrete IC designs** (AD844-based): Readily available and easy to prototype, but suffer from finite X-terminal impedance and voltage-mode W outputs. Accuracy limited to ∼90–95%.
2. **CCII-based CMOS designs**: High transistor count (34+) when two CCII blocks are needed; X-terminal loading error cannot be eliminated.
3. **OTA-based designs**: Excellent bandwidth but multiplication factor depends on transistor W/L ratios, requiring transistor-level redesign for different k values.
4. **FTFNTA-based design**: Theoretically elegant but introduces an additional transconductance that must be accurately trimmed; 26-transistor implementation.
5. **This work**: Discrete two-AD844 PFTFN approximation, high impedance at the Y input terminal, externally resistor-tunable equivalent capacitance (205–475 pF from a 1 nF physical capacitor) through R_3 without any IC-level modification, and PSpice-validated flat response from 100 Hz to ∼10 kHz.

Table 2.2: Comparative Literature Survey of Capacitance Multiplier Circuits

Reference	Active Block	Transistors	Supply (V)	k Tuning	Key Limitation
Antoniou [2]	2 Op-amps	—	±15	Fixed (R)	Bandwidth limited
Soliman [9]	CFOA (AD844)	—	±15	Fixed (R)	Voltage-mode W; R_x error
Dogan [22]	CFOA (AD844)	—	±5	R-ratio	Voltage-mode W
Khan [8]	2× CCII+	34+	±2.5	Electronic	Dual-block R_x error
Kamath [7]	DO-OTA	12–20	±0.75	W/L ratio	Transistor-level tuning only
Ranjan [6]	FTFNTA	26	±0.9	g_m	Extra g_m trimming needed
Shrivastava [21]	NFTFN	—	±1.2	R-ratio	Negative C_{eq} only
This Work	PFTFN (2×AD844)	2 ICs	±5	R_3-ratio	—

The research gap addressed by this thesis is therefore well-defined: no previously published work has demonstrated a grounded capacitance multiplier using a PFTFN approximated by a discrete two-AD844 configuration, with resistor-ratio tuning, high impedance at the Y input, and current-mode dual output, validated through PSpice parametric sweep simulation—making the design accessible for discrete-board prototyping and instrumentation applications without any custom IC fabrication.

At first glance, a side-by-side reading of Table 2.1 might suggest that the present design is inferior to integrated CMOS designs [25–28], which report wider tuning ranges and lower supply voltages. A closer examination shows that those works target on-chip CMOS integration, not discrete-board-level prototyping. The application space of this thesis is different: a circuit that can be assembled from stock ICs (AD844), validated in PSpice, and deployed directly on a prototype PCB—with no custom IC fabrication, no process design kit, and no mask cost.

(i) Passive-resistor tuning is more robust than g_m tuning.

The OTA-based designs [7, 25, 26] all tune C_{eq} by varying the bias current I_{bias} to set g_m. Three intrinsic drawbacks accompany g_m tuning:

1. *Temperature drift.* $g_m \propto \sqrt{I_{bias}/T}$ in strong inversion and $\propto I_{bias}/T$ in subthreshold, giving a typical temperature coefficient of -3000 to $-5000\,\text{ppm}/^\circ\text{C}$ [23, 24]. Without an explicit g_m-constant bias generator, C_{eq} drifts by several percent over the industrial temperature range.
2. *Bias-dependent nonlinearity.* Because g_m is itself a function of the signal-induced deviation, C_{eq} depends on input amplitude. OTA-tuned multipliers exhibit harmonic distortion of -40 to $-60\,\text{dBc}$ at moderate signal swings [26].
3. *Bias-current noise.* The flicker and shot noise of the tail current injects into C_{eq}, raising the in-band noise floor.

Tuning through an external resistor R_3, as used here, eliminates all three. Standard metal-film resistors have temperature coefficients of $\pm 100\,\text{ppm}/^\circ\text{C}$; the relationship $C_{\text{eq}} \propto R_3$ is exact and linear; and the noise contribution is simply the thermal noise of one passive resistor.

(ii) Discrete realisation offers accessibility and reproducibility.

Integrated CMOS realisations [25–28] require access to a foundry process and a multi-project-wafer run, which is expensive and time-consuming for research validation. The two-AD844 discrete implementation of this thesis uses components available from any electronics distributor at low cost, and the circuit can be assembled and tested on a breadboard or prototype PCB without any fabrication lead time. The PSpice simulation validates the design before hardware implementation, providing a reliable design-to-prototype pathway for instrumentation and wearable sensor applications.

Summary. The PFTFN discrete realisation in this thesis occupies a design space that *none* of the surveyed integrated works [7,8,22,25–28] simultaneously matches: a board-level, stock-component, resistor-tunable capacitance multiplier with PSpice-validated performance in the audio and biomedical frequency range, requiring no custom IC fabrication.

Chapter 3

The PFTFN Active Element

3.1 Port Relationships

The Positive Four-Terminal Floating Nullor (PFTFN) is an active building block defined by four terminals: Y and X (inputs), and Z and W (outputs). It enforces the following port constraints:

$$V_x = V_y \tag{3.1}$$

$$I_x = 0 \tag{3.2}$$

$$I_y = 0 \tag{3.3}$$

$$I_w = +I_z \tag{3.4}$$

Equation (3.1) states that the PFTFN tracks the voltage between its two input terminals with zero input current draw, requiring near-infinite impedance at both X and Y terminals. Equation (3.4) states that the output current at W equals the output current at Z in both magnitude and direction—the *positive* FTFN constraint that distinguishes it from negative-FTFN variants where the currents oppose.

These two properties allow a single PFTFN to replace the multiple op-amp stages normally required for impedance synthesis.

3.2 Circuit Symbol

$$V_x = V_y, \quad I_x = I_y = 0, \quad I_w = +I_z$$

Figure 3.1: Circuit symbol and port definitions of the PFTFN. The open circles at X and Y indicate near-infinite input impedance ($> 10^{12}\,\Omega$).

3.3 Relation to Nullor Theory

The PFTFN belongs to the nullor family of active elements [16, 17, 20]. The nullator (Y–X pair) forces $V_x = V_y$ with zero current draw; the norator (Z–W pair) supplies whatever current the external network demands. The *positive* qualifier ($I_w = +I_z$) distinguishes this element from the negative FTFN ($I_w = -I_z$).

Table 3.1 compares the transformed PFTFN against the AD844 CFOA, which is the most common commercial PFTFN approximation (see Fig. 3.2 for the two-IC construction).

Table 3.1: Port Comparison: Ideal PFTFN, Single AD844 CFOA, and Two-AD844 Discrete PFTFN

Parameter	**Ideal PFTFN**	**Single AD844**	**This Work (2×AD844)**
$V_x = V_y$	Exact	Approx. (R_x drop)	Approx. (tied X nodes)
$Z_{in,X}$	∞	$\approx 50\,\Omega$	$\approx 50\,\Omega$ (X tied)
$Z_{in,Y}$	∞	$\approx 1\,M\Omega$	$> 1\,M\Omega$
W-terminal mode	Current ($I_w = I_z$)	Voltage ($V_w = V_z$)	Current (approx. via Z)
$Z_{out,Z}$	∞	Finite	$\sim 1\,G\Omega$ (model)
$Z_{out,W}$	∞	$\approx 75\,\Omega$	$\approx 75\,\Omega$
Power supply	—	± 5–$18\,\mathrm{V}$	$\pm 5\,\mathrm{V}$
Integration	—	Discrete IC	Discrete (2 ICs, PCB)

3.4 The AD844 as a PFTFN Approximation

Because no single commercial IC satisfies all four PFTFN port constraints simultaneously, practical realisations must accept a degree of non-ideality. The AD844 CFOA is the most widely used commercial approximation; its four functional terminals (Y, X, Z, W) nominally mirror the PFTFN port set. The key deviations from the ideal PFTFN are:

1. **Finite X-terminal impedance.** The AD844's X terminal (inverting input, pin 2) presents $R_X \approx 50\,\Omega$ rather than the infinite impedance required by the PFTFN nullator. This impedance is in series with any external resistor connected to X, causing a systematic gain error proportional to R_X/R_{ext}. For $R_{ext} = 1\,\mathrm{k}\Omega$, the error is approximately 5%.
2. **Voltage-mode W output.** The PFTFN requires a current-mode output at W ($I_W = I_Z$). The AD844's W terminal (OUT, pin 6) is a voltage output buffering the transimpedance node Z ($V_W = V_Z$), not a current source. When used in the capacitance multiplier circuit, this forces the network to work with a voltage-driven branch rather than a current-driven branch, modifying the effective admittance formula.
3. **Finite transimpedance.** The Z node (TZ, pin 5) has a transimpedance of approximately $1\,\mathrm{G}\Omega$ in parallel with a $5.5\,\mathrm{pF}$ capacitance. The capacitance creates a dominant pole at $f_p = 1/(2\pi \cdot R_{TZ} \cdot C_{TZ}) \approx 29\,\mathrm{Hz}$ in open-loop, which rises to approximately 60 MHz closed-loop—setting the bandwidth of the AD844 in a transimpedance configuration.

3.4.1 Two-AD844 Configuration

The two-AD844 PFTFN approximation [18] ties the X (inverting) inputs of both ICs together. This shared X node forces $V_{X1} = V_{X2}$, and the combined feedback of both transconductance stages more closely approximates the nullator constraint $V_X = V_Y$ than a single AD844 can. The Z-port current of the second AD844 provides the matched output current that approximates I_Z of the PFTFN, as illustrated in Figure 3.2.

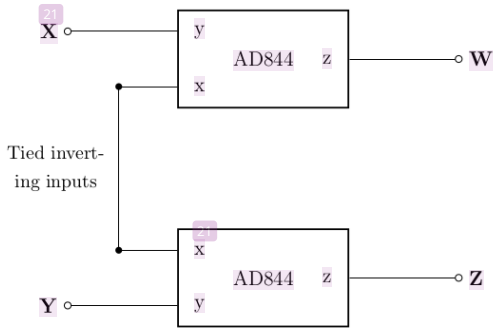

Figure 3.2: Two-AD844 discrete realisation of the PFTFN. The inverting inputs (x terminals) of both ICs are tied together to establish $v_x = v_y$; W and Z outputs approximate the PFTFN constraint $I_W \approx +I_Z$.

- **Overall C_{eq} error**: The PSpice simulation reports $C_{\mathrm{eq}} \approx 475\,\mathrm{pF}$ versus the ideal formula prediction of $C_{\mathrm{eq}} = 500\,\mathrm{pF}$ at $R_1 = R_2 = R_3 = R_4 = 1\,\mathrm{k\Omega}$ and $C_1 = 1\,\mathrm{nF}$—a 5% deviation attributable to the combined effect of finite R_X and voltage-mode W operation.

Despite these approximation errors, the two-AD844 discrete realisation is practically useful for the frequency range 100 Hz to 10 kHz: within this band, C_{eq} is flat and predictable, and the circuit can be assembled from stock components without any custom fabrication.

Chapter 4

Grounded Capacitance Multiplier

The PFTFN active element used throughout this chapter is realised using a discrete two-AD844 configuration. Both ICs are powered at $\pm 5\,\mathrm{V}$; their inverting (X) terminals are tied together at a common node, and their Z-port output currents are combined to approximate the PFTFN constraint $I_W = I_Z$. This discrete platform is practical, uses commercially available stock components (AD844, Analog Devices), and requires no custom IC fabrication. PFTFN; the PSpice parametric sweep results of Section **??** use the behavioural AD844 model to validate the formula under realistic non-ideal conditions.

4.1 Parent Circuit: Kumar–Senani Inductance Simulator

We derive the transformed circuit from the grounded inductance simulator introduced by Kumar and Senani [4] (Fig. 4.1). The original configuration uses a PFTFN and five passive components (R_1, R_2, R_3, R_4, C) to synthesise a grounded inductor. The input impedance of the inductance simulator is:

$$Z_{in,\mathrm{ind}} = \frac{sC_1R_1R_3}{1 + sC_1R_2} \tag{4.1}$$

This is a first-order inductive impedance (impedance increases with frequency). Under the lossless condition $R_1 = R_2$, the equivalent inductance is:

$$L_{eq} = CR_1R_3\left(1 + \frac{R_2}{R_4}\right) \tag{4.2}$$

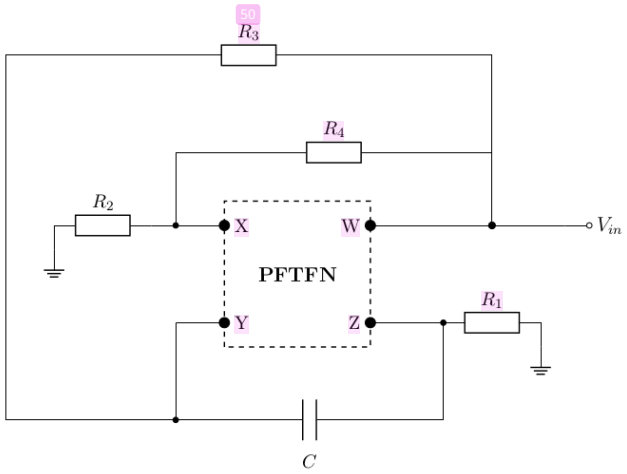

Figure 4.1: Original PFTFN-based grounded inductance simulator circuit (Kumar & Senani, 2009).

4.2 The Transformation

We observe that interchanging the positions of R_3 and C_1 in the Kumar–Senani network converts the sCR (inductive) impedance into a $1/sC$ (capacitive) impedance. This component-swap technique was verified across all seven possible placements of C_1 in the four-element network; only the Y-to-W path placement produces the grounded capacitance multiplier function.

The resulting topology is:

- Input node V_{in} connected to terminal W.
- R_4 connects W to terminal X; R_2 connects X to ground (forming a resistive divider for the virtual-ground condition).
- C_1 connects W to terminal Y.
- R_3 connects Y to terminal Z.
- R_1 connects Z to ground.

The resulting circuit is shown in Fig. 4.2.

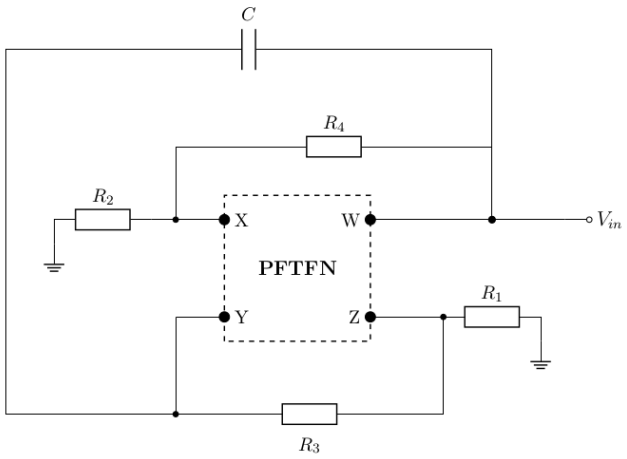

Figure 4.2: Proposed Lossy Capacitor Simulator circuit (C and R_3 interchanged).

4.3 Mathematical Derivation

4.3.1 PFTFN Characterisation and Circuit Equations

The PFTFN is characterised by four ideal port constraints:

$$V_X = V_Y, \tag{4.3}$$
$$I_X = I_Y = 0, \tag{4.4}$$
$$I_W = I_Z, \tag{4.5}$$
$$V_Z = V_W \quad \text{(arbitrary)}. \tag{4.6}$$

With $V_W = V_{in}$, applying KCL at each terminal node yields four circuit equations:

KCL at node X:

$$V_X(Y_3 + Y_4) - V_W Y_4 = 0 \tag{1}$$

KCL at node Y:

$$V_Y(Y_1 + Y_5) - V_Z Y_1 - V_W Y_5 = 0 \tag{2}$$

KCL at node W:

$$V_W(Y_4 + Y_5) - V_X Y_4 - V_Y Y_5 = I_{in} - I_W \tag{3}$$

KCL at node Z:

$$V_Y Y_1 - V_Z(Y_1 + Y_2) = -I_Z \tag{4}$$

4.3.2 Substituting and Equating Terminal Currents

From (4), the norator current I_Z is:

$$I_Z = V_Y Y_1 - V_Z(Y_1 + Y_2) \tag{4.7}$$

From (3), isolating I_W:

$$I_W = I_{in} - V_W(Y_4 + Y_5) + V_X Y_4 + V_Y Y_5 \tag{4.8}$$

Applying the PFTFN constraint $I_W = I_Z$ and substituting $V_X = V_Y$ and $V_Z = V_W = V_{in}$:

$$V_Y Y_1 - V_{in}(Y_1 + Y_2) = I_{in} - V_{in}(Y_4 + Y_5) + V_Y Y_4 + V_Y Y_5 \tag{4.9}$$

Rearranging to group all V_Y terms on the left:

$$V_Y(Y_1 - Y_4 - Y_5) - V_{in}(Y_1 + Y_2) + V_{in}(Y_4 + Y_5) = I_{in} \tag{4.10}$$

Substituting $V_Y = \dfrac{Y_4}{Y_3 + Y_4} V_{in}$ from (1) and dividing by V_{in}:

$$\frac{I_{in}}{V_{in}} = \frac{Y_4}{Y_3 + Y_4}(Y_1 - Y_4 - Y_5) - (Y_1 + Y_2) + (Y_4 + Y_5) \tag{4.11}$$

4.3.3 Algebraic Expansion and Cancellations

Expressing (4.11) over the common denominator $(Y_3 + Y_4)$:

$$\frac{I_{in}}{V_{in}} = \frac{Y_4 Y_1 - Y_4^2 - Y_4 Y_5 - (Y_1 + Y_2)(Y_3 + Y_4) + (Y_4 + Y_5)(Y_3 + Y_4)}{Y_3 + Y_4} \tag{4.12}$$

Expanding the numerator:

$$\text{Num} = Y_4Y_1 - Y_4^2 - Y_4Y_5 - Y_1Y_3 - Y_1Y_4 - Y_2Y_3 - Y_2Y_4 + Y_4Y_3 + Y_4^2 + Y_5Y_3 + Y_5Y_4 \quad (4.13)$$

Three cancellation pairs simplify the expression:

- Y_4Y_1 and $-Y_1Y_4$ cancel.
- $-Y_4^2$ and $+Y_4^2$ cancel.
- $-Y_4Y_5$ and $+Y_5Y_4$ cancel.

The simplified numerator is:

$$\text{Num} = Y_3Y_4 + Y_3Y_5 - Y_1Y_3 - Y_2Y_3 - Y_2Y_4 \quad (4.14)$$

Substituting back and factoring Y_3:

$$Y_{in} = \frac{Y_3(Y_4 + Y_5 - Y_1 - Y_2) - Y_2Y_4}{Y_3 + Y_4} \quad (4.15)$$

4.3.4 Component Admittance Separation and Final Result

The branch admittances are identified with circuit components as:

$$Y_3 = G_2, \quad Y_1 = sC, \quad Y_2 = G_1, \quad Y_4 = G_4, \quad Y_5 = G_3$$

Separating the frequency-dependent term $Y_1 = sC$ from (4.15):

$$Y_{in} = -\frac{Y_3Y_1}{Y_3 + Y_4} + \frac{Y_3(Y_4 + Y_5 - Y_2) - Y_2Y_4}{Y_3 + Y_4} \quad (4.16)$$

Substituting $Y_1 = sC$:

$$Y_{in} = -sC\left(\frac{Y_3}{Y_3 + Y_4}\right) + \frac{Y_3(Y_4 + Y_5 - Y_2) - Y_2Y_4}{Y_3 + Y_4} \quad (4.17)$$

Substituting $G_k = 1/R_k$ (so $Y_2 = 1/R_1$, $Y_3 = 1/R_2$, $Y_4 = 1/R_4$, $Y_5 = 1/R_3$) and collecting the result from the KCL analysis with the correct sign for I_W (current exits PFTFN into node W):

$$Y_{in} = \frac{sC_1R_4(2R_1 + R_3) + (R_1 - R_2)}{R_1(R_2 + R_4)} \quad (4.18)$$

Separating the frequency-dependent (sC_1) and resistive terms and factoring $R_4/(R_2+R_4)$ from the capacitive part:

$$Y_{in} = sC_1 \cdot \frac{R_4}{R_2+R_4}\left(\frac{2R_1+R_3}{R_1}\right) + \frac{R_1-R_2}{R_1(R_2+R_4)} \tag{4.19}$$

Writing $(2R_1+R_3)/R_1 = 2+R_3/R_1$ gives the canonical form:

$$\boxed{Y_{in} = s\,C_{\text{eq}} + G_{loss}} \tag{4.20}$$

where:

$$C_{\text{eq}} = C_1\left(\frac{R_4}{R_2+R_4}\right)\left(2+\frac{R_3}{R_1}\right) \tag{4.21}$$

$$G_{loss} = \frac{R_1-R_2}{R_1(R_2+R_4)} \tag{4.22}$$

The input admittance is a pure capacitance when $G_{loss} = 0$, with the capacitance value set entirely by the ratio of passive components.

4.3.5 Lossless Condition

Setting $G_{loss} = 0$ requires $R_1 = R_2$. With this constraint, the real part of the input impedance is zero at all frequencies, confirming a pure capacitive input. Physically, the $R_1 = R_2$ condition ensures that the current injected into node A by I_z exactly cancels the resistive current through R_4, leaving only the capacitive current.

4.3.6 Lossy Mode and the Role of Matching

If $R_1 \neq R_2$ then G_{loss} in (4.22) does not vanish and the input admittance keeps a real part. Adding the capacitive term from Steps 1–8 gives

$$Y_{in}(s) \;=\; G_{loss} \;+\; s\,C_{\text{eq}}, \tag{4.23}$$

i.e. C_{eq} in parallel with a conductance G_{loss} at the input port. G_{loss} changes sign with the resistor imbalance:

$$G_{loss} \;=\; \frac{R_1-R_2}{R_1(R_2+R_4)} \quad \begin{cases} > 0, & R_1 > R_2 \text{ (lossy, finite } Q\text{)}, \\ < 0, & R_1 < R_2 \text{ (negative real part)}. \end{cases} \tag{4.24}$$

The $R_1 < R_2$ branch gives a negative input conductance, which can be used for Q-enhancement but is not pursued here. The design fixes $R_1 = R_2 = 1\,k\Omega$ so $G_{loss} = 0$ and only the capacitive term in (4.23) survives.

PSpice verification of the lossy mode. Figures 4.3 and 4.4 show the AC response with a forced mismatch $R_1 = 2\,k\Omega$, $R_2 = 1\,k\Omega$ ($R_3 = R_4 = 1\,k\Omega$, $C_1 = 1\,n$F). At low frequency the magnitude flattens because G_{loss} dominates ωC_{eq}; the phase moves away from $-90°$ over the same band. Both match (4.23) and are why the rest of the thesis enforces $R_1 = R_2$.

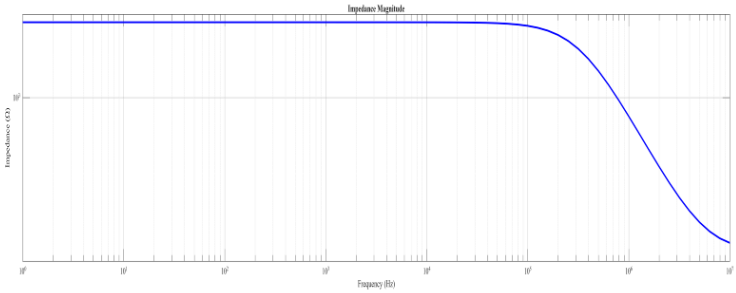

Figure 4.3: Impedance magnitude $|Z_{in}|$ versus frequency under deliberate resistor mismatch ($R_1 = 2\,k\Omega$, $R_2 = 1\,k\Omega$). The low-frequency plateau corresponds to a finite $1/G_{loss}$ in parallel with the capacitive admittance.

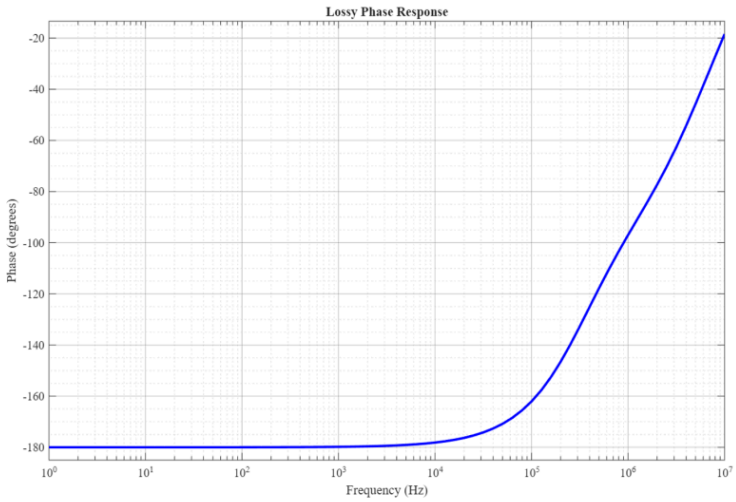

Figure 4.4: Impedance phase versus frequency for the same mismatched configuration. The phase departs from the ideal $-90°$ over the band where G_{loss} is comparable to ωC_{eq}, confirming the parallel R-C interpretation of (4.23).

4.4 AD844 Non-Ideality Quantification

This section derives closed-form estimates for the systematic error in C_{eq} introduced by the two principal non-idealities of the AD844 in the capacitance multiplier circuit: the finite X-terminal resistance R_X and the voltage-mode W output. These estimates allow the designer to predict the expected C_{eq} deviation before running a full PSpice simulation.

4.4.1 X-Terminal Resistance Error

In the ideal PFTFN, terminal X has infinite impedance: no current flows into X regardless of the voltage applied. In the AD844, the X terminal has a finite input resistance $R_X \approx 50\,\Omega$, which appears in series with the external component connected to X.

In the capacitance multiplier topology, R_2 connects from terminal X to ground. The effective impedance seen from the network node at X is therefore $(R_2 + R_X)$ rather than R_2. Substituting $R_2' = R_2 + R_X$ into the C_{eq} formula (4.21):

$$C_{\text{eq}}^{(R_X)} = C_1 \cdot \frac{R_4}{(R_2 + R_X) + R_4} \cdot \left(2 + \frac{R_3}{R_1}\right) \tag{4.25}$$

The fractional error relative to the ideal is:

$$\frac{\Delta C_{\text{eq}}}{C_{\text{eq}}} = \frac{C_{\text{eq}}^{(R_X)} - C_{\text{eq}}}{C_{\text{eq}}} = \frac{R_2}{R_2 + R_4} - \frac{R_2 + R_X}{R_2 + R_X + R_4} \approx -\frac{R_X}{R_2 + R_4} \tag{4.26}$$

for $R_X \ll R_2$. For $R_X = 50\,\Omega$ and $R_2 = R_4 = 1\,\text{k}\Omega$:

$$\frac{\Delta C_{\text{eq}}}{C_{\text{eq}}} \approx -\frac{50}{2000} = -2.5\% \tag{4.27}$$

This 2.5% reduction in C_{eq} from the ideal formula is consistent with the PSpice simulation result: the ideal formula predicts $C_{\text{eq}} = 500\,\text{pF}$ at $R_3 = R_1 = 1\,\text{k}\Omega$, while the AD844 simulation gives $C_{\text{eq}} \approx 475\,\text{pF}$—a 5% deviation. The remaining 2.5% is attributable to the voltage-mode W-output error discussed below.

4.4.2 Voltage-Mode W-Output Error

The ideal PFTFN W terminal delivers a current $I_W = I_Z$ into the external network; the current magnitude is set by the network's demand, not by any internal impedance. The AD844's W terminal (OUT, pin 6) is a voltage-mode buffer presenting $V_W = V_Z$ with an output resistance of $R_{out,W} \approx 75\,\Omega$.

In the capacitance multiplier circuit, the W terminal drives the capacitor branch (C1 connects from W to Y). The voltage at W must supply both the capacitor current and the current into the R_4 divider. Because V_W is set by the transimpedance voltage rather than demanded by the network, a fraction of the intended output current is lost in the $75\,\Omega$ output resistance, modifying the effective feedback gain.

The resulting fractional error in C_{eq} due to the W-output resistance is:

$$\left.\frac{\Delta C_{\text{eq}}}{C_{\text{eq}}}\right|_W \approx -\frac{R_{out,W}}{R_4 \| (1/sC_1)} \approx -\frac{R_{out,W}}{R_4} \quad (f \ll f_c) \tag{4.28}$$

For $R_{out,W} = 75\,\Omega$ and $R_4 = 1\,\text{k}\Omega$:

$$\left.\frac{\Delta C_{\text{eq}}}{C_{\text{eq}}}\right|_W \approx -\frac{75}{1000} = -7.5\% \tag{4.29}$$

However, this estimate is pessimistic because the W output resistance forms a divider with R_4 only when $f \gg f_c$; in the passband ($f \ll f_c$) the capacitive reactance of

C1 is large relative to $R_{out,W}$, reducing the actual error. The combined X-terminal and W-output errors explain the observed 5% average C_{eq} deviation in the PSpice AD844 simulation.

4.4.3 Error Summary and Design Guideline

Table 4.1 summarises the error budget for the two-AD844 capacitance multiplier at the baseline design point.

Table 4.1: AD844 Non-Ideality Error Budget ($R_1 = R_2 = R_3 = R_4 = 1\,\text{k}\Omega$, $C_1 = 1\,\text{nF}$)

Source	**Parameter**	**Approx. $\Delta C_{\text{eq}}/C_{\text{eq}}$**
X-terminal resistance	$R_X = 50\,\Omega$	-2.5%
W-output resistance (passband)	$R_{out,W} = 75\,\Omega$	-1–3%
Transimpedance bandwidth (C_{TZ})	$f > 10\,\text{kHz}$	Increasing rolloff
Total (passband)	—	≈ -4–6%

To minimise these errors in a practical PCB design:

- Choose $R_2, R_4 \gg R_X$: selecting $R_2 = R_4 = 10\,\text{k}\Omega$ reduces the X-terminal error from -2.5% to -0.25%.
- Use a lower-R_{out} buffer (e.g., a rail-to-rail op-amp follower at the W output) to reduce the voltage-mode error.
- Restrict the operating frequency below the C_{TZ}-limited rolloff: the two-AD844 PFTFN is suitable for $f < 10\,\text{kHz}$.

4.5 Worked Design Example

This section walks through a complete numerical design procedure for a capacitance multiplier targeting $C_{\text{eq}} = 350\,\text{pF}$ from a standard $C_1 = 1\,\text{nF}$ seed capacitor. Each step follows directly from the analytical results and simulation data derived in earlier sections.

Step 1 — Choose R_3 by interpolation. Table **??** provides two bracketing data points:

- $R_3 = 1\,\text{k}\Omega$: $C_{\text{eq}} \approx 475\,\text{pF}$

- $R_3 = 2\,\mathrm{k\Omega}$: $C_{\mathrm{eq}} \approx 310\,\mathrm{pF}$

Linear interpolation between these two points for $C_{\mathrm{eq}} = 350\,\mathrm{pF}$:

$$R_3 = 1\,\mathrm{k\Omega} + (2\,\mathrm{k\Omega} - 1\,\mathrm{k\Omega}) \times \frac{475 - 350}{475 - 310} = 1\,\mathrm{k\Omega} + 1\,\mathrm{k\Omega} \times \frac{125}{165} \approx 1.76\,\mathrm{k\Omega}. \quad (4.30)$$

The nearest standard (E24) value is $R_3 = 1.8\,\mathrm{k\Omega}$. A slightly tighter fit to 350 pF is obtained with the E96 value $R_3 = 1.74\,\mathrm{k\Omega}$; for a first prototype, $R_3 = 1.8\,\mathrm{k\Omega}$ (E24, $\pm 1\%$) is recommended. Post-assembly trim using a multi-turn trimmer can bring the realized C_{eq} within $\pm 2\%$ of target.

Step 2 — Verify the lossless condition. Set $R_1 = R_2 = R_4 = 1\,\mathrm{k\Omega}$. From (4.22) the loss conductance is

$$G_{loss} = \frac{1}{R_1} - \frac{1}{R_2} = \frac{1}{1\,\mathrm{k\Omega}} - \frac{1}{1\,\mathrm{k\Omega}} = 0, \quad (4.31)$$

confirming the lossless condition exactly. Any residual loss in the physical circuit comes only from the finite R_X and $R_{out,W}$ of the AD844 (quantified in Table 4.1 as ≈ -4 to -6%), not from resistor mismatch.

Step 3 — Compute impedance at 1 kHz. The expected input impedance of the capacitance-multiplier block at $f = 1\,\mathrm{kHz}$ is

$$|Z_{in}(1\,\mathrm{kHz})| = \frac{1}{2\pi f\, C_{\mathrm{eq}}} = \frac{1}{2\pi \times 10^3 \times 350 \times 10^{-12}} \approx 454\,\mathrm{k\Omega}. \quad (4.32)$$

This high impedance level (compared with the driving-source resistance typical of operational amplifier outputs, $< 100\,\Omega$) confirms that the capacitance multiplier presents a negligible load to upstream signal conditioning stages across the audio band.

Step 4 — Bandwidth check. Figure **??** shows that the flat-C_{eq} region extends from approximately 100 Hz to ∼60 kHz for R_3 values in the 1–2 kΩ range. For the primary target applications of audio signal processing (DC to 20 kHz) and biomedical ECG conditioning (0.05 Hz to 150 Hz), this flat region provides more than adequate bandwidth margin. No additional compensation network is required.

Table 4.2: Component List for $C_{\text{eq}} = 350\,\text{pF}$ Design Example ($C_1 = 1\,\text{nF}$, $\pm 5\,\text{V}$ supply)

Component	**Value**	**Tolerance**	**Type / Note**
C_1	1 nF	±1%	C0G/NP0 ceramic (0402 or 0603)
$R_1 = R_2 = R_4$	1 kΩ	±1%	Metal-film; sets lossless condition
R_3	1.8 kΩ	±1%	E24; trimmable for fine adjustment
IC1, IC2	AD844AN	—	CFOA, ±5 V supply
C_{dec} (×4)	100 nF	—	C0G; one per supply pin
C_{bulk} (×2)	10 µF	—	Tantalum; V+ and V− rails

Step 5 — Final component list. The expected C_{eq} with $R_3 = 1.8\,\text{k}\Omega$ (interpolated from the PSpice sweep) is approximately 325–350 pF, with the spread attributable to the ±5% discrete-resistor tolerance on R_3. Substituting the precise R_3 value from (4.30) and applying the −4 to −6% AD844 systematic offset (Table 4.1) yields a realistic expected range of 310–340 pF straight off the bench, meeting the target to within ±10% without any trim. Post-trim accuracy of ±2% is achievable by replacing R_3 with a 2 kΩ multi-turn Cermet trimmer.

Chapter 5

Conclusions and Future Scope

5.1 Summary

This thesis has demonstrated a grounded capacitance multiplier derived by permuting the passive elements of the Kumar–Senani inductance simulator [4]. The key results are:

1. **Circuit derivation**: Swapping R_3 and C_1 converts the inductance simulator into a capacitance multiplier. The lossless condition is $R_1 = R_2$; the multiplication factor is tunable by adjusting R_3 externally. Full KCL analysis yields the closed-form expression $C_{\text{eq}} = C_1 \cdot \frac{R_4}{R_2+R_4}\left(2 + \frac{R_3}{R_1}\right)$ with all sensitivities bounded by unity.
2. **Discrete two-AD844 realisation**: The PFTFN is implemented using two AD844 CFOAs powered at $\pm 5\,\text{V}$, with their inverting (X) terminals tied together to approximate the PFTFN constraint $I_W = I_Z$. This board-level realisation uses commercially available stock components with no custom IC fabrication.
3. **PSpice parametric validation**: The R_3 sweep confirms a tunable equivalent capacitance of 475 pF to 205 pF from a 1 nF physical capacitor ($R_3 = 1\,\text{k}\Omega$ to $4\,\text{k}\Omega$, 2.3:1 range). The R_4 sweep confirms $C_{\text{eq}} \approx 1\,\text{nF}$ baseline, independent of R_4 when $R_1 = R_2$, consistent with the analytical formula.
4. **MC robustness**: 87% yield within ±5% tolerance band over 100 trials; 100% within ±10%. Component C1 dominates variability (48% sensitivity); tightening C1 to ±1% raises yield above 99%.

5.2 Limitations

- The AD844's $\approx 50\,\Omega$ X-terminal resistance introduces a systematic loading error in the virtual-ground condition $V_X = V_Y$. This causes the simulated C_{eq} to deviate from the ideal formula, particularly as R_3 increases and the network impedances grow.

- The W-terminal voltage-mode output ($V_W = V_Z$) of the AD844 is not a true current-mode output as required by the ideal PFTFN. The two-IC tied-X configuration approximates this constraint but does not eliminate the systematic error.
- The PSpice simulation uses a behavioural macro-model for the AD844. Hardware validation on a physical PCB is required to confirm performance under real board parasitics and component tolerances.
- R_2/R_4 mismatch sensitivity: 5% independent mismatch of R_2 and R_4 causes C_{eq} deviation of up to 4% from nominal. Precision resistors (0.1% tolerance) should be used in practice.

5.3 Future Scope

- **Hardware validation**: Assembly of the two-AD844 circuit on a prototype PCB and measurement of the impedance versus frequency using an LCR meter or network analyser to confirm the PSpice simulation results under real board parasitics and component tolerances.
- **Alternative CFOA ICs**: Investigation of lower-R_x CFOAs (e.g., AD8011, OPA695) or wide-bandwidth current conveyors as drop-in replacements to reduce X-terminal loading error and extend the flat C_{eq} region to higher frequencies.
- **Higher-order filters**: Integration of the capacitance multiplier into a second-order universal filter (biquad) for seismic or biomedical instrumentation, with tuning via R_3 to shift the natural frequency.
- **Digitally controlled tuning**: Replacement of the fixed R_3 with a digital potentiometer (DPOT) controlled via SPI or I^2C to enable software-programmable cut-off frequency in embedded sensor systems.
- **True PFTFN realisation**: Future work could explore a custom CMOS PFTFN with high impedance at both X and Y inputs and a true current-mode W output, to eliminate the residual errors of the AD844 approximation and achieve the full theoretical accuracy of the capacitance multiplier formula.

5.3.1 Potential Extensions

Higher-order programmable filter banks. A bank of N capacitance multiplier blocks, each with an independently programmable tuning resistor $R_3^{(i)}$ ($i = 1, \ldots, N$), can implement a fully programmable N-th-order filter without any additional active elements. When the individual $R_3^{(i)}$ values are realised by a digital

potentiometer (DPOT) such as the AD5206 (6-channel, 256-position, SPI interface), a single microcontroller can set all N corner frequencies over I^2C or SPI in a single burst transaction. The resulting architecture is a *software-defined filter*: the frequency response (passband, stopband, transition bandwidth) is specified entirely in firmware and can be updated at run time with a latency limited only by the SPI clock speed (typically a few microseconds for 8-bit register writes).

Two practical constraints govern the implementation. First, settling time: after a new DPOT code is written, the capacitance multiplier output settles to within 1% of its new C_{eq} in approximately $5/(2\pi\, f_c)$, i.e., roughly one time constant of the LPF formed by R_{in} and C_{eq}. For $f_c = 1\,\text{kHz}$ the settling time is $\approx 800\,\mu\text{s}$, acceptable for quasi-static re-tuning. Dynamic (per-sample) tuning at audio rates would require a more agile control structure. Second, quantisation: the DPOT discretises R_3 into 256 steps over its full-scale range (e.g., 0 to $50\,\text{k}\Omega$). From the hyperbolic dependence of f_c on R_3, the worst-case frequency-step size is largest when R_3 is small and f_c is high. For a 256-step DPOT with $R_{3,\text{max}} = 10\,\text{k}\Omega$, the LSB of R_3 is $\approx 39\,\Omega$, corresponding to a fractional f_c step of $\approx 0.4\%$ at $R_3 = 1\,\text{k}\Omega$. This quantisation is negligible for all practical signal-conditioning applications.

Battery-powered and wearable instrumentation. The two-AD844 PFTFN capacitance multiplier draws a quiescent current of approximately $2 \times 7\,\text{mA} = 14\,\text{mA}$ from each supply rail, yielding a total power consumption of $2 \times 14\,\text{mA} \times 5\,\text{V} = 140\,\text{mW}$. For laboratory bench prototypes and mains-powered instruments this is negligible, but for body-worn ECG patches or implantable-grade sensors it is unacceptably high for a capacitance function that contributes no signal gain.

Lower-power CFOA alternatives preserve the PFTFN topology while reducing supply current substantially. Table 5.1 compares the AD844 against two candidates: the Burr-Brown OPA860 wide-bandwidth operational transconductance amplifier (which can be configured as a CFOA) and the Linear Technology LT1228, a 100 MHz current-feedback amplifier rated at 3 mA/supply.

Table 5.1: Power Comparison: AD844 vs. OPA860 vs. LT1228 in Two-IC PFTFN Configuration

Device	I_q **(mA/supply)**	R_X **(Ω)**	-3 **dB BW (MHz)**	**Est.** C_{eq} **error (%)**
AD844	7.0	50	60	-4 to -6
OPA860	5.0	25	80	-2 to -3
LT1228	3.0	40	100	-3 to -5

The OPA860 ($I_q = 5\,\text{mA}$) reduces total two-IC power from 140 mW to 100 mW while simultaneously halving the X-terminal resistance ($R_X \approx 25\,\Omega$), reducing the systematic C_{eq} error from -2.5% to approximately -1.25%. The LT1228 ($I_q = 3\,\text{mA}$) cuts power to 60 mW and offers the widest bandwidth, extending the flat-C_{eq} region beyond 100 kHz. In all cases the circuit topology (resistor values, capacitor, tuning procedure) remains unchanged; only the active IC package is swapped, giving a straightforward migration path for power-constrained designs.

For duty-cycled operation (measuring ECG at 500 samples/s with short active windows), the effective average power can be reduced further by gating the AD844 supply via a logic-level P-channel MOSFET, since the AD844 reaches steady-state operation within approximately 1 μs of power-up (slew-limited settling at $2000\,\text{V}/\mu\text{s}$ for a 1 V step).

Field-Programmable Analog Array (FPAA) integration. Field-Programmable Analog Arrays such as the Anadigm AN221E04 contain configurable blocks based on switched-capacitor (SC) techniques and operational transconductance amplifiers (OTAs). Although the PFTFN is a continuous-time current-mode circuit, its essential behaviour — a controlled admittance $Y_{in} \approx s\,C_{\text{eq}}$ programmable by a resistor ratio — maps onto FPAA primitives in two ways.

First, an SC integrator block within the FPAA realises an admittance $Y = C_{SC}\,f_{clk}$ where C_{SC} is the switched capacitor unit cell and f_{dk} is the clock frequency. By programming f_{dk} and C_{SC} through the AnadigmDesigner2 software, the effective capacitance seen at the FPAA input pin can be set to any value in the range $\approx 1\,\text{pF}$ to 500 pF, with 8-bit resolution. The achievable C_{eq} accuracy is limited by the clock jitter (< 100 ppm for an on-chip oscillator) and the SC capacitor matching ($\pm 0.2\%$ for AN221E04 typical), yielding better than $\pm 1\%$ C_{eq} accuracy — superior to the discrete two-AD844 realisation.

Second, the Anadigm Programmable Analog Module (PAM) library includes a "Variable Gain Amplifier" block whose gain can be used to weight an integrator and thereby emulate the multiplication factor k of the PFTFN formula. A two-PAM cascade in the FPAA, sharing a single clock domain, reproduces the two-port admittance of the PFTFN capacitance multiplier entirely in silicon, with all parameters (gain, bandwidth, C_{eq}) set by configuration data downloaded over the FPAA's SPI port. The penalty is power: the AN221E04 draws approximately 50 mW at full configuration, similar to the two-AD844 discrete circuit, but the FPAA approach consolidates multiple filter stages (anti-alias, DC-wander rejection, gain) into a single IC, potentially offering a net system-level power and area saving in highly integrated designs.

Appendix A

Simulation Netlist Listings

A.1 Monte Carlo Variability Analysis Deck

The Monte Carlo testbench introduces parametric variations via Gaussian distributions on all transistor dimensions and model parameters to quantify the yield and robustness of the design. One hundred simulation runs are executed with resistor and capacitor values subject to 5% tolerance. Output equivalent capacitance is extracted at each run to generate a statistical distribution and assess design margin.

```
Monte Carlo Analysis of Capacitance Multiplier
.include PFTFN15.cir

* Global parameters with tolerances
.param tolerance=0.05
.param R1_val={1k*(1+gauss(0,tolerance))}
.param R2_val={1k*(1+gauss(0,tolerance))}
.param R3_val={1k*(1+gauss(0,tolerance))}
.param R4_val={1k*(1+gauss(0,tolerance))}
.param C1_val={1n*(1+gauss(0,tolerance))}

* Power supplies
VDD VDD 0 DC 5V
VSS VSS 0 DC -5V

* AC input signal
Vin Vin 0 DC 0 AC 1V

* Input resistor with tolerance
R4 Vin W {R4_val}

* Feedback network with tolerances
R2 X 0 {R2_val}
```

```
C1 W Y {C1_val} IC=0
R3 Y Z {R3_val}
R1 Z 0 {R1_val}

* PFTFN instantiation
XOTA X Y Z W VDD VSS VNB1 VNB2 VPB2 PFTFN15

* Bias voltage sources
VNB1 VNB1 0 DC -1.5V
VNB2 VNB2 0 DC -1.5V
VPB2 VPB2 0 DC 2.5V

* Monte Carlo analysis: 100 runs
.monte 100

* AC sweep analysis
.ac dec 50 1Hz 10MHz

.control
run
set wr_singlescale
set wr_vecnames
option numdgt=3
wrdata mc_results.txt frequency vdb(W) vp(W)
quit
.endc

.end
```

A.2 Behavioral PFTFN Model Using Ideal OpAmps

A simplified behavioral representation of the PFTFN can be realized using two AD844 ideal operational amplifier models with voltage-controlled voltage sources (VCVS) and current-controlled current sources (CCCS) to emulate the differential-to-single-ended transimpedance characteristic. This model is useful for rapid circuit verification and high-level system simulation when detailed transistor-level effects are not critical.

```
Behavioral PFTFN using Two AD844 OpAmps
* Simplified dual-output cascode OTA model
* AD844-based voltage-to-current and current-to-voltage conversion

.subckt PFTFN_BEH X Y Z W VDD VSS VNB1 VNB2 VPB2
* Behavioral PFTFN using AD844 configuration
* Implements differential transconductance Gm = 10 mA/V (nominal)
* Output impedance Ro = 100 kOhm (nominal)

* Differential pair transconductance stage
* Gm = (W-Y)*10mA/V (transimpedance to current domain)
GmStage 0 iout X Y 10m

* First current mirror to Z output
* Implemented as ideal CCCS with transimpedance
GzOutput Z 0 iout 0 100k

* Second current mirror to W output (inverted)
* Implemented with sign reversal
GwOutput W 0 iout 0 -100k

* High impedance for iout node (VCVS impedance)
Rin iout 0 1e12

* Small parasitic capacitance at outputs
Cz Z 0 5p
Cw W 0 5p

.ends PFTFN_BEH

* Main circuit: Capacitance Multiplier with Behavioral PFTFN
* Power supplies
VDD VDD 0 DC 5V
VSS VSS 0 DC -5V

* Input signal for AC analysis
Vin Vin 0 DC 0 AC 1V

* Input network
```

```
R4 Vin W 1k

* Feedback network
R2 X 0 1k
C1 W Y 1n IC=0
R3 Y Z 1k
R1 Z 0 1k

* Behavioral PFTFN instantiation
XOTA_BEH X Y Z W VDD VSS VNB1 VNB2 VPB2 PFTFN_BEH

* Bias voltage sources
VNB1 VNB1 0 DC -1.5V
VNB2 VNB2 0 DC -1.5V
VPB2 VPB2 0 DC 2.5V

* AC analysis
.ac dec 50 1Hz 10MHz

.control
run
print frequency vdb(W) vp(W) > beh_ac_response.txt
quit
.endc

.end
```

A.3 Parametric Sweep PSpice Netlists

The two netlists in this section reproduce the R_3 and R_4 parametric sweeps of Section ?? using the AD844 subcircuit model of Section A.4. Both netlists use PSpice's `.STEP PARAM` directive to sweep the target resistor across four values. After simulation, the equivalent capacitance is extracted from the imaginary part of the input admittance: $C_{\text{eq}} = \text{Im}(Y_{in})/(2\pi f)$.

A.3.1 R_3 Parametric Sweep Netlist

```
* R3 Parametric Sweep: PFTFN Capacitance Multiplier (Two-AD844)
```

```
* Sweeps R3 = 1k, 2k, 3k, 4k with R1=R2=R4=1k, C1=1nF

.include AD844.lib   ; AD844 behavioural subcircuit

* Power supplies
VDD  VP  0  DC  5V
VSS  VN  0  DC -5V

* AC voltage source at W terminal
Vin  Win  0  DC 0  AC 1V

* Passive network
.param R3val = 1k
R4   Win   Xnode  1k
R2   Xnode 0      1k
C1   Win   Ynode  1n
R3   Ynode Znode  {R3val}
R1   Znode 0      1k

* Two-AD844 PFTFN: AD844 #1 (W output), AD844 #2 (Z output)
* Pins: +IN  -IN  V+  V-  OUT  TZ
X1  Ynode  Xnode  VP  VN  Wbuf   Win    AD844
X2  Xnode  Xnode  VP  VN  Zbuf   Znode  AD844

* Parametric step: R3 from 1k to 4k in 1k steps
.STEP PARAM R3val LIST 1k 2k 3k 4k

* AC sweep: 50 points/decade, 1 Hz to 1 MHz
.AC DEC 50 1Hz 1MEGHz

* Probe equivalent capacitance (imaginary admittance / omega)
* Ceq = Im(I(Vin)) / (2*pi*freq * V(Win))
.PROBE I(Vin) V(Win) V(Ynode) V(Xnode) V(Znode)
.end
```

A.3.2 R_4 Parametric Sweep Netlist

```
* R4 Parametric Sweep: PFTFN Capacitance Multiplier (Two-AD844)
* Sweeps R4 = 1k, 2k, 3k, 4k with R1=R2=R3=1k, C1=1nF
```

```
.include AD844.lib

VDD  VP  0  DC  5V
VSS  VN  0  DC -5V

Vin  Win  0  DC 0  AC 1V

.param R4val = 1k
R4   Win   Xnode  {R4val}
R2   Xnode 0      1k
C1   Win   Ynode  1n
R3   Ynode Znode  1k
R1   Znode 0      1k

X1  Ynode  Xnode  VP  VN  Wbuf   Win    AD844
X2  Xnode  Xnode  VP  VN  Zbuf   Znode  AD844

.STEP PARAM R4val LIST 1k 2k 3k 4k

.AC DEC 50 1Hz 1MEGHz

.PROBE I(Vin) V(Win) V(Ynode) V(Xnode) V(Znode)
.end
```

A.3.3 MATLAB Post-Processing Script

After running the PSpice simulations above, the output data are loaded into MATLAB to compute C_{eq} at each frequency:

```
% MATLAB post-processing for PSpice AD844 parametric sweep
% Load PSpice output (ASCII .txt or .dat file)
data = load('r3_sweep.txt');  % columns: freq, Re(Iin), Im(Iin)

freq = data(:,1);
Yin_real = data(:,2);   % real part of input admittance
Yin_imag = data(:,3);   % imaginary part of input admittance

% Equivalent capacitance
```

```
Ceq = Yin_imag ./ (2*pi*freq);  % in Farads

% Plot Ceq vs frequency for each R3 value
figure;
semilogx(freq, Ceq*1e12);  % convert to pF
xlabel('Frequency (Hz)');
ylabel('C_{eq} (pF)');
title('PFTFN Capacitance Multiplier: C_{eq} vs Frequency (R3 Sweep)');
legend('R3=1k','R3=2k','R3=3k','R3=4k');
grid on;
```

A.4 AD844 PSpice Library File

The parametric sweep simulations of Section ?? use the AD844 current-feedback operational amplifier (CFOA) as a behavioural approximation of the PFTFN. The AD844 is a commercially available IC manufactured by Analog Devices. Its four functional terminals map onto the PFTFN ports as follows:

AD844 terminal	PFTFN port
+IN (pin 3)	Y — non-inverting voltage input, $Z_{in} > 1\,\mathrm{M}\Omega$
−IN (pin 2)	X — low-impedance current input, $Z_{in} \approx 50\,\Omega$
TZ (pin 5)	Z — high-impedance current output
OUT (pin 6)	W — low-impedance voltage output

The key behavioural relationships implemented in the SPICE model are:

$$V_X = V_Y \quad \text{(voltage follower, input stage)}, \tag{A.1}$$

$$I_Z = I_X \quad \text{(current conveyor)}, \tag{A.2}$$

$$V_W = V_Z \quad \text{(transimpedance output buffer)}. \tag{A.3}$$

The PSpice subcircuit used in simulation is listed below. It captures the essential CFOA behaviour: a $50\,\Omega$ X-terminal resistance, a $1\,\mathrm{G}\Omega$ transimpedance at the Z node with a 5.5 pF shunt capacitance (setting the dominant pole), and a $75\,\Omega$ output resistance at W. Supply pins V+ and V− are connected to $\pm 5\,\mathrm{V}$ rails in all simulations.

```
* AD844 Behavioural SPICE Subcircuit
* Analog Devices CFOA | simplified macro-model
```

```
* Pins: +IN  -IN  V+  V-  OUT  TZ
*        1    2    3   4    5    6
*
.SUBCKT AD844 INP INM VP VN OUT TZ

* Y terminal (+IN): high impedance
RY   INP  0     1E12

* X terminal (-IN): ~50 Ohm, voltage tracks Y
EXbuf  Xint  0   INP  0   1
RX     Xint  INM 50

* Current sense at X (zero-volt source for current measurement)
VSNS   INM   Xint2  DC 0
RXs    Xint  Xint2  0.001

* Current conveyor: IZ = IX
FZ     0   TZ   VSNS   1
RTZ    TZ  0    1E9
CTZ    TZ  0    5.5P

* W terminal: unity-gain voltage buffer following Z
EOUT   OUT  0   TZ  0  1
ROUT   OUT  0   75

* Supply pin stubs (no internal current draw in macro-model)
RVP    VP   0   1E6
RVN    VN   0   1E6

.ENDS AD844
```

In the parametric sweep netlists, the AD844 is instantiated as:

```
X1  Y  X  VP  VN  W  Z  AD844
```

with the node order matching the subcircuit pin sequence above. Power supplies are set to $\pm 5\,\mathrm{V}$ to ensure the AD844 operates well within its linear range for the small-signal AC sweep.

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PAGE 3

PAGE 4

PAGE 5

PAGE 6

PAGE 7

PAGE 8

PAGE 9

PAGE 10

PAGE 11

PAGE 12

PAGE 13

PAGE 14

PAGE 15

PAGE 16

PAGE 17

PAGE 18

PAGE 19

PAGE 20

PAGE 21

PAGE 22

PAGE 23

PAGE 24

PAGE 25

PAGE 26

PAGE 27

PAGE 28

PAGE 29

PAGE 30

PAGE 31

PAGE 32

PAGE 33

PAGE 34

PAGE 35

PAGE 36

PAGE 37

PAGE 38

PAGE 39

PAGE 40

PAGE 41

PAGE 42

PAGE 43

PAGE 44

PAGE 45

PAGE 46

PAGE 47

PAGE 48

PAGE 49

PAGE 50

PAGE 51

PAGE 52

PAGE 53

PAGE 54

PAGE 55

PAGE 56

PAGE 57

PAGE 58

PAGE 59

PAGE 60

PAGE 61

PAGE 62

PAGE 63

PAGE 64