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FGMOS based VDTA realizations with enhanced performance

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI and Embedded Systems

Submitted by:

Arushi Saxena

24/VLS/007

Under the supervision of

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MAY, 2026

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I, hereby certify that the Project Dissertation titled "FGMOS based VDTA designs with enhanced performance" which is submitted by Arushi Saxena, Roll No. 24/VLS/007 to Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi
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Dr. Rajeshwari Pandey
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CONTENTS

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Arushi Saxena

ABSTRACT

This thesis presents a comparative study of floating-gate MOSFET-based voltage differencing transconductance amplifier realizations with the objective of improving low-voltage operation and transconductance performance for analog signal-processing applications. This work consolidates two research studies carried out during the M. Tech. program, both using the CMOS VDTA as the reference architecture and then explore circuit modifications at the input transconductance stage. In the first study, FGMOS devices are introduced to exploit the capacitive gate coupling and threshold voltage modulation. Then, partial positive feedback is subsequently employed to enhance the effective transconductance. In the second study, a series-parallel current mirror is incorporated to further boost transconductance while preserving the low-voltage benefits of the FGMOS-based structure. All circuits are simulated in 180 nm CMOS technology using LTspice under identical supply and biasing conditions to ensure a fair comparison.

The simulation results show that the conventional CMOS VDTA provides a transconductance of 1.27 mS with a bandwidth of 405.7 MHz, whereas the FGMOS-based realization supports low-voltage operation and exhibits modified frequency behaviour with a bandwidth improvement. The PPF-enhanced design increases transconductance to 1.84 mS with a bandwidth reduction to 148 MHz, while the SPCM-enhanced implementation achieves the highest transconductance of 4.23 mS, with bandwidth of 126.3 MHz.

Overall, the findings demonstrate that FGMOS-based VDTA architectures are effective for low-voltage analog design, while PPF and SPCM techniques offer significant transconductance boost with the expected gain-bandwidth trade-off.

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CHAPTER 1

INTRODUCTION

1.1. Voltage Differencing Transconductance Amplifier

The VDTA is a versatile current-mode active building block that has gained considerable attention in modern analog circuit design. It is a dual-input, dual-output transconductance-based device in which the differential voltage is applied at the input terminals is converted into currents at the internal and output terminals. Owing to its high input impedance, high output impedance and electronically adjustable transconductance, the VDTA is well suited for low-voltage, low-power and high frequency analog signal-processing applications. The block is especially useful in the realization of filters and oscillators, where precise control of transconductance and frequency response is needed.

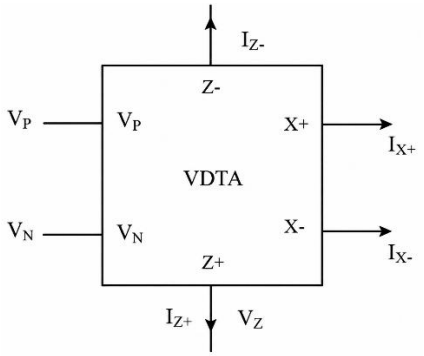

Figure 1: Symbolic representation of the VDTA [3]

Figure 1 illustrates the symbolic representation of the VDTA, showing the differential input terminals $V_P$and V_N, the Z-terminal current outputs, and the X-terminal current outputs. In its ideal form, the VDTA consists of two differential input terminals, commonly denoted as $V_P$and V_N, and a pair of high-impedance output terminals, typically represented as Z^+, Z^-, X^+, and X^-. The differential voltage $V_P - V_N$ is first converted into a current at the Z terminals through the input transconductance stage. This current is then further processed by the second transconductance stage to generate the corresponding output currents at the X terminals. The terminal relations can be expressed in simplified form as a proportional relationship between the input differential voltage and output currents. This two-stage conversion mechanism provides flexibility in circuit design and allows the VDTA to function as an important transconductance -controlled element.

The principal advantage of the VDTA lies in its ability to provide tuneable transconductance without requiring a proportional increase in the bias current. This makes it particularly attractive for low-power analog designs. Furthermore, the use of VDTA enables the compact implementation of high-order analog functions with improved robustness to voltage swings. However, the performance of a conventional CMOS VDTA is often constraint by supply-voltage limitations, finite bandwidth and the trade-off between transconductance enhancement and frequency response. Consequently, several modified implementations have been proposed in the literature to improve its low-voltage operation and overall performance. In the present works, the VDTA serves as the baseline architecture and its modified realizations are investigates using floating-gate MOSFET devices and transconductance-boosting techniques to achieve improves low-voltage analog performance.

The operation of the VDTA may also be understood from its small-signal terminal behavior. In an ideal implementation, the differential voltage applied between $V_P$and $V_N$is converted into equal and opposite currents at the $Z^+$and Z^-terminals by the first transconductance stage. These currents are subsequently processed by the second transconductance stage to generate the corresponding output currents at the $X^+$and X^-terminals. Since the input terminals exhibit high impedance, the preceding stage is not significantly loaded, while the high output impedance at the current terminals facilitates straightforward cascading in analog integrated circuits. Such current-mode operation is advantageous because it supports small-signal processing with improved bandwidth and reduced voltage headroom, compared with conventional voltage-mode amplifiers.

14 A further important feature of the VDTA is the independent control of its transconductance parameters. In practical CMOS realizations, the two transconductance stages are biased separately, allowing the designer to tune the circuit response through adjustment of the bias currents. This enables a wide range of transfer characteristics to be obtained without altering passive component values, making the VDTA particularly attractive for electronically tuneable filters, oscillators and impedance conversion circuits. The independent tuneablity of the two stages also provides greater flexibility in shaping the gain and frequency response of the overall system.

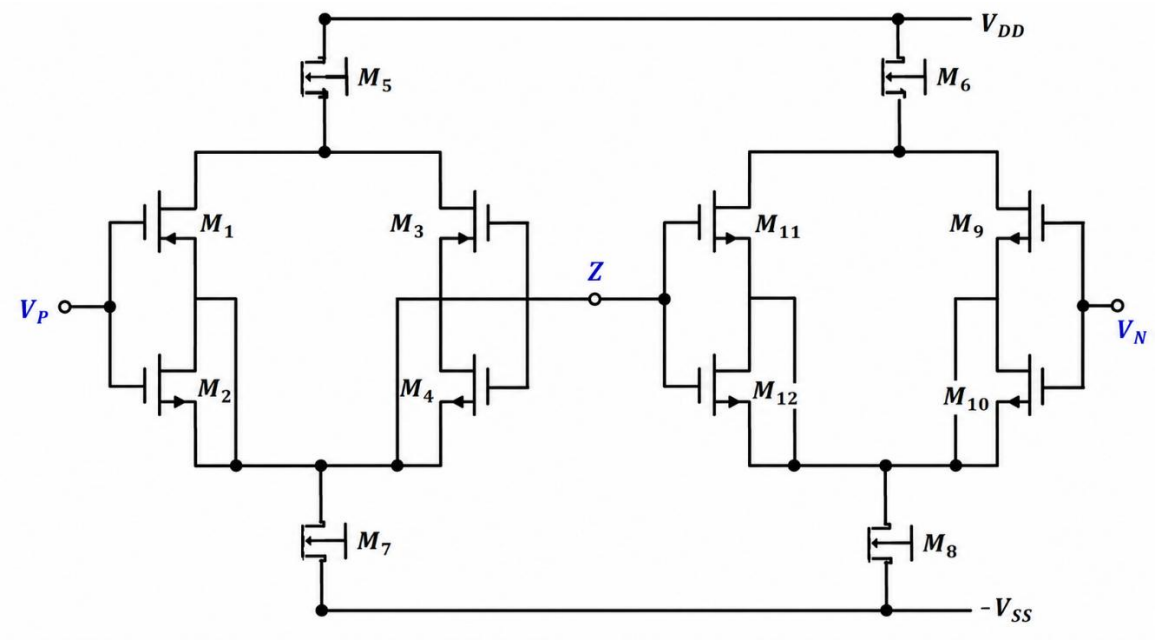

Figure 2: Transistor level schematic of the conventional CMOS VDTA architecture [10]

The CMOS implementation of the VDTA shown in Figure 2 illustrates the transistor level realization of the ideal block using a differential transconductance stage, current-mirror loading, and biasing networks to establish the required small-signal operation. In this topology, the input differential voltage applied between $V_P$and $V_N$is sensed by the first transconductance stage and translated into currents at the internal Znode. The Z-terminal voltage is then further processed by the second transconductance stage to generate the corresponding output currents at the $X^+$and X^-terminals. The circuit operates in current mode, and therefore the input terminals exhibit high impedance, while the output terminals provide high output impedance, which is desirable for cascading in integrated analog signal-processing systems. The use of bias currents $I_{b1}$and I_{b2}sets the operating point of the two transconductance stages and determines the effective transconductance values of the VDTA.

From a small-signal perspective, the ideal terminal relations of the VDTA may be written as

$$I_{Z+} = g_{m1}(V_P - V_N), I_{Z-} = -g_{m1}(V_P - V_N) \quad (1.1)$$

$$I_{X+} = g_{m2}V_Z, I_{X-} = -g_{m2}V_Z \quad (1.2)$$

where g_{m1} and g_{m2} denote the transconductances of the first and second stages, respectively. For a MOS-based realization operating in saturation, the transconductance is approximately given by

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \quad (1.3)$$

which shows that the transconductance can be controlled electronically through the bias current and device dimensions. This tunability is one of the main advantages of the VDTA, since the same core can be adapted for a wide range of current-mode applications simply by adjusting the biasing conditions.

The structure shown in the figure is therefore well suited for low-voltage analog design, because the differential input stage enables signal transfer without requiring large voltage swings. Nevertheless, the performance of a conventional CMOS VDTA remains limited by finite output resistance, parasitic capacitances and the trade-off between transconductance and bandwidth. For this reason, modified versions based on floating-gate MOSFETs and transconductance enhancement techniques are considered in this thesis to improve low-voltage operation and overall circuit performance.

1.2. Floating gate MOSFETs

The floating-gate MOSFETs are specialized MOS transistors in which the gate terminal is electrically isolated and receives input signals through capacitive coupling rather than direct ohmic connection. Figure 3 illustrates the floating gate, that is surrounded by multiple control gates, and the applied voltages are capacitively summed at the isolated gate node. This unique structure enables the effective gate voltage to be influenced by more than one input, thereby offering a flexible means of controlling the device operating point. This capacitive charge-sharing mechanism allows the threshold voltage of the transistor to be effectively shifted, making the FGMOS devices highly suitable for low-voltage analog circuit design.

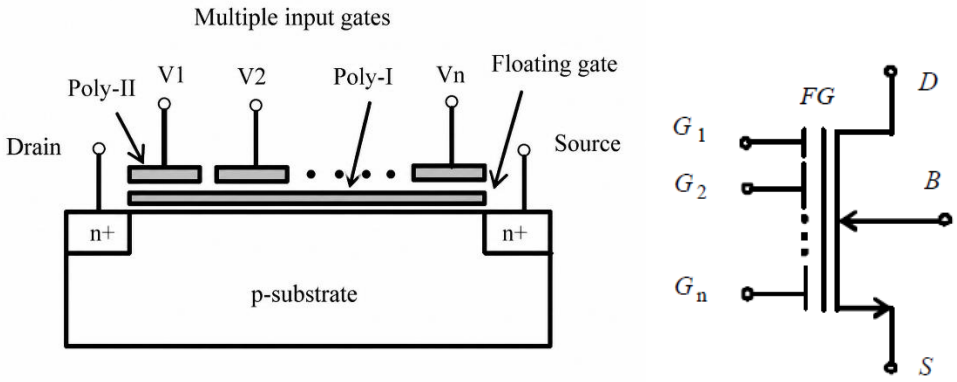

Figure 3: (a) Structure of MIFG transistor **(b)** Symbol of MIFG transistor [1]

One of the principal advantages of the FGMOS devices is their ability to reduce the voltage headroom required for proper transistor operation. The device can remain functional even when the supply voltage is significantly constraint due to the lowered

effective threshold voltage achieved as a result of capacitive division. This feature makes the device particularly useful in the modern CMOS technologies, where scaling of supply voltages often limits the performance of conventional analog circuits.

The practical use of the FGMOS devices is associated with certain non-idealities, such as charge leakage, parasitic capacitances and the need for an appropriate DC bias path to establish a stable operating point. In the present works, FGMOS devices are employed in the input transconductance stage of the VDTA to facilitate low-voltage operation and to investigate their impact in circuit performance. The structure shown in figure 3 highlights the basic floating-gate configuration and the manner in which multiple control inputs are capacitively coupled to the isolated gate terminal.

The operation of an FGMOS device is governed by the potential developed at the floating gate, which is determined by capacitive charge sharing among the input gates and the parasitic capacitances associated with the structure. Since the gate node is electrically isolated, the effective gate voltage is a weighted combination of the applied input voltages, stored charge, and bias potentials. For an n-input floating-gate transistor, the floating-gate voltage may be expressed as

$$V_{FG} = \frac{\sum_{i=1}^{n} C_i V_i + C_B V_B + C_D V_D + C_S V_S + Q_{FG}}{C_T} \quad (1.4)$$

where C_i is the coupling capacitance associated with the i^{th} input, V_i is the corresponding input voltage, C_B, C_D, and C_S represent the parasitic capacitances associated with the body, drain, and source nodes, Q_{FG} is the charge stored on the floating gate, and C_T is the total capacitance seen at the floating node. The total capacitance can be written as

$$C_T = \sum_{i=1}^{n} C_i + C_B + C_D + C_S + C_{par} \quad (1.5)$$

where C_{par} denotes the remaining parasitic capacitance of the floating-gate node. The capacitive coupling factor for the i^{th} input is defined as

$$\alpha_i = \frac{C_i}{C_T} \quad (1.6)$$

so that the floating-gate voltage may also be expressed in the compact form

$$V_{FG} = \sum_{i=1}^{n} \alpha_i V_i + \frac{Q_{FG}}{C_T} \quad (1.7)$$

with $\sum_{i=1}^{n} \alpha_i < 1$ due to the presence of parasitic capacitances.

For a MOS transistor operating in the saturation region, the drain current is given by

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \quad (1.8)$$

where $\mu$is the carrier mobility, $C_{ox}$is the oxide capacitance per unit area, $W/L$is the aspect ratio, V_{TH} is the threshold voltage, λ is the channel-length modulation coefficient, and V_{DS} is the drain-to-source voltage. In an FGMOS device, the gate-to-source voltage is replaced by the floating-gate potential, i.e., $V_{GS} \rightarrow V_{FG} - V_S$. Hence, the effective threshold requirement is reduced, allowing the transistor to conduct at lower supply voltages. This property is especially beneficial in low-voltage VDTA realizations, where the available voltage headroom is limited.

The small-signal transconductance of the device is obtained as

$$g_m = \frac{\partial I_D}{\partial V_{FG}} = \mu C_{ox} \frac{W}{L}(V_{FG} - V_{TH})(1 + \lambda V_{DS}) \quad (1.9)$$

and, under the square-law approximation, it may also be written as

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \quad (1.10)$$

This relation shows that the transconductance can be controlled by the bias current and effective gate coupling, enabling tuneable analog operation without requiring a proportional increase in power consumption. In the VDTA, the devices FGMOS devices in the input transconductance stage therefore provides two important advantages, first, it reduces the effective threshold voltage and supports operation at reduced supply voltage, second, it improves the flexibility of transconductance control through capacitive weighting of input signal, as a result, the FGMOS-based VDTA is better suited for low-voltage, low-power current-mode analog signal-processing applications.

1.3. Transconductance enhancement techniques for VDTA realization

The conventional CMOS and FGMOS-based VDTA structures, although suitable for low-voltage operation, are still constrained by the trade-off between transconductance, bandwidth and bias current. In a practical analog integrated circuit, the effective transconductance of a VDTA directly influences key performance metrics such as current transfer efficiency, frequency response and gain in current-mode filter and oscillator applications. Consequently, transconductance enhancement techniques are introduced to improve the effective small-signal performance of the circuit without a proportional increase in static power dissipation. Among the commonly used approaches, partial positive feedback and series-parallel techniques are particularly attractive because they operate at the circuit level and can be integrated with the existing VDTA topology without fundamentally altering its basic differential structure,

The motivation for using partial positive feedback lies in its ability to introduce controlled regenerative action in the transconductance stage, but feeding a fraction of the output signal back in phase to the input, the effective loop gain if the stage is increased, resulting in a higher equivalent transconductance, this technique is especiallyuseful when stronger current conversion is required by reduction in bandwidth, since the added regenerative feedback shifts the dominant pole toward lower frequencies. Therefore, PPF provides a means of boosting transconductance while maintaining low-voltage operation.

The SPCM technique, in contrast, improves transconductance by modifying the current-mirror load structure so that the output current is effectively replicated and amplified through series and parallel current paths. This approach increases the current-driving capability of the transconductance stage without requiring an increase in bias current. From a design perspective, SPCM is attractive because it achieves significant transconductance enhancement through improved current transfer efficiency rather than strong regenerative feedback. As a result, it is particularly suitable for applications in which high transconductance is required within a fixed power budget. Nevertheless, the additional mirror devices introduce parasitic capacitances and internal node loading, which may reduce bandwidth and must be considered during device sizing and bias optimization.

In the present work, both PPF and SPCM are employed as complementary transconductance boosting strategies for the FGMOS-based VDTA. The use of these techniques allows a systematic comparison of circuit-level enhancement methods in terms of transconductance improvement, bandwidth degradation, and overall suitability for low-voltage analog signal-processing applications. Together, they provide two distinct but effective routes for optimizing the performance of the proposed VDTA architectures under constrained supply conditions.

CHAPTER 2
LITERATURE REVIEW

The continuous scaling down of the CMOS technology node has led to an increase in the demand for analog devices that can reliably operate at low supply voltages and also maintain the performance parameters like transconductance, bandwidth and power efficiency. Current mode signal processing is thus a sought-out approach because it offers improved dynamic range and better suitability for low-voltage operations than many conventional voltage mode counterparts. The voltage differencing transconductance amplifier (VDTA) has gained attention due to its flexible use in realizing filters, oscillators and other signal processing blocks. In this work, the conventional VDTA serves as the baseline circuit, providing the reference AC and DC behaviours. The recent research has focused mostly on improving the VDTA performance using circuit level transconductance boosting. The transconductance-boosted VDTA architectures reported in [1] show that partial positive feedback can be used effectively to increase the effective transconductance of a VDTA. That work demonstrates substantial enhancement in g_m, but also confirms the associated reduction in bandwidth, revealing the well-known trade-off between gain boosting and frequency response. At the same time, there have been multiple researches investigating device level techniques for low-voltage analog designs. The broader performance-improvement strategies summarized in [2] show that low-power analog design requires a careful balance among device choice, biasing method, and circuit performance. The DTMOS- and FD-FVF-based VDTA reported in [3] further confirms that low-voltage operation is achievable, although typically with increased implementation complexity and design constraints. Likewise, the CMOS realization of voltage-differencing structures in [4] demonstrates that practical analog blocks can be implemented in standard CMOS processes, but their performance remains strongly influenced by supply-voltage and biasing limitations. Enhanced low-voltage analog design can be obtained by using floating gate techniques. The captive coupling mechanism in the device allows threshold voltage programmability in floating-gate MOSFETs making them suitable for analog circuits that require post fabrication tuning and reduced voltage headroom [5]. The work in [6] extends the same concept to QFGMOS-based circuit by using quasi floating gate operations approach, which improved the low-voltage behaviour, bandwidth and power performance issues of the conventional FGMOS device by reducing the charge accumulation. Similarly, for

FGMOS/QFGMOS-based MI-OTA, it has been established that floating-gate based structures function efficiently at low voltage supply and offer flexible analog circuit design. The study supports that to improve performance parameters of VDTA realizations, FGMOS-based transconductance stages should be used [7]. In order to enhance the transconductance without proportionally increasing power consumption various circuit-level enhancement techniques have been employed. It has also been observed that in an adaptive-biased VDBA, positive response in combination with adaptive basing can improve transconductance gain and dynamic response while retaining the circuit's power efficiency [8]. The study proves, that partial positive feedback is a practical approach to enhance transconductance gain in analog blocks with bandwidth penalty in acceptable range [1 and 8]. In [9] a low-voltage low-power FGMOS transistor based cascode current mirror is used to design a current-mode full wave rectifier. It has been simulated in various conditions and shows improved performance in terms of output impedance, current accuracy and power consumption.

Gupta et al. [11] presented a high performance VDBA with adaptive biasing and partial positive feedback for improving the transconductance of the circuit while maintaining low standby power. In other works, Gupta et al. [12] proposed an adaptive biased VDIBA and established that partial positive feedback combined with adaptive biasing can significantly improve transconductance with only a moderate bandwidth penalty. More recently, Rani et al. [13] presented two transconductance-boosted VDTA structures, one focusing on partial positive feedback and the other based on gate-to-source voltage enhancement and concluded that transconductance can be increased substantially with acceptable reduction in bandwidth. Gupta et al. [14] further demonstrated that a series-parallel current mirror (SPCM) can also be used to boost transconductance in VDIBA structures by increasing the effective current gain at constant bias current.

These prior studies, motivated the present work to investigate the comparison of various VDTA implementations. The conventional CMOS VDTA is used as the baseline reference, further the input stage devices are replaced with floating-gate devices for improved low-voltage operation and for the final enhancement SPCM-based architecture in added to the circuit for boosting the transconductance. The aim of this study is to show that the combination of FGMOS and SPCM can be used for producing higher transconductance while preserving low-voltage operation.

Despite these advancements, in most of the studies the VDTA realization focuses either on device-level low-voltage operation or circuit-level transconductance boosting lacking the combination of both the concepts in a unified framework. The proposed work addresses this gap by considering a conventional VDTA, FGMOS-based VDTA, PPF-enhanced VDTA and

the SPCM-enhanced under identical simulation conditions in 180 nm CMOS technology using LTspice. A comparative analysis has been presented considering low-voltage operation and transconductance boosting for analog signal processing in practical applications. The study aims to provide the criteria to select the suitable topology based on the application whether the priority is tunability, bandwidth enhancement or transconductance efficiency. The simulation results showed that the conventional CMOS VDTA attains g_m = 1.27 mS with a bandwidth of 405.7MHz, the FGMOS-based VDTA attains g_m = 0.88 mS with a bandwidth of 443.3 MHz, the PPF-enhanced VDTA achieves g_m= 1.84 mS with a bandwidth of 148 MHz, and the SPCM-enhanced VDTA achieves the highest transconductance of 4.23 mS, with bandwidth of 126.3 MHz, clearly showing the trade-off between transconductance boosting and bandwidth reduction.

CHAPTER 3

CMOS BASED AND FLOATING GATE MOSFET BASED VDTA

This chapter presents the design and implementation of the conventional CMOS-based VDTA and the FGMOS-based VDTA architectures considered in the present work. The conventional CMOS realization is first discussed to establish the fundamental operating principles and baseline performance characteristics of the VDTA under low-voltage operating conditions. Subsequently, the FGMOS-based implementation is introduced by incorporating floating-gate MOSFET devices into the input transconductance stage in order to improve low-voltage operation and transconductance behavior.

1. Conventional CMOS based VDTA

The CMOS-based VDTA is used as the reference topology in this work. The architecture is typically realized using two cascaded transconductance stages. The first stage senses the differential input voltages $V_P - V_N$ and converts it into a differential current that is directly proportional to the voltage difference at the internal high impedance Z terminals. The second stage processes the current of the first stage and produces the corresponding output current at X terminal. Owing to the high input impedance of the P and N terminals and the high output impedance of the Z and X terminals, the VDTA is well suited for analog signal-processing applications.

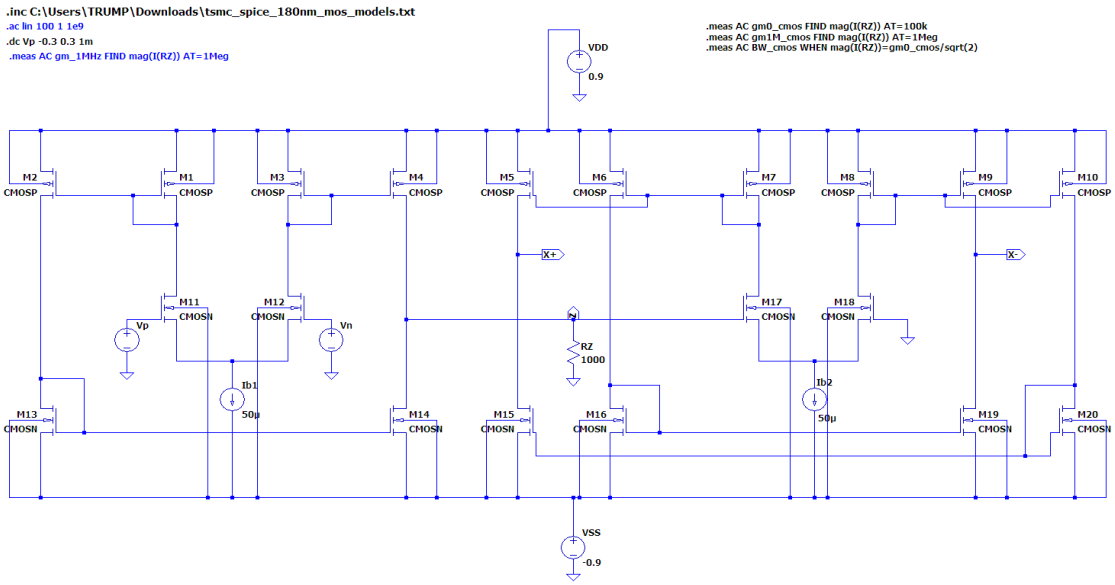

Figure. 4: Conventional CMOS-based VDTA circuit implementation

In the small-signal domain, the terminal relations of the conventional VDTA can be written as:

$$I_{Z+} = g_{m1}(V_P - V_N) \quad (3.1)$$
$$I_{Z-} = -g_{m1}(V_P - V_N) \quad (3.2)$$
$$I_{X+} = g_{m2}V_{Z+} \quad (3.3)$$
$$I_{X-} = -g_{m2}V_{Z+} \quad (3.4)$$

where, g_{m1} and g_{m2} denote the transconductances of the first and second stages, respectively. In an ideal VDTA, the differential input voltage is therefore translated into a pair of equal and opposite currents at the Z terminals, which are subsequently mirrored and converted at the X terminal. This two-stage current conversion provides flexible transconductance control and facilitates cascading with other current-mode blocks. For the MOS-based implementation, the input differential pair is operated in saturation so that the drain current can be approximated by

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (3.5)$$

and the corresponding transconductance is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \frac{2I_D}{V_{OV}} = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \quad (3.6)$$

where $V_{OV} = V_{GS} - V_{TH}$ is the overdrive voltage, μC_{ox} is the process transconductance parameter. The small-signal resistance of the circuit directly influences the finite output impedance and the high-frequency response of the conventional VDTA. The reference CMOS VDTA therefore establishes the baseline transconductance and bandwidth against which the FGMOS-based and SPCM-enhanced versions are compared.

To validate the performance of the conventional CMOS VDTA realization, extensive simulations have been performed using LTspice in 180 nm CMOS technology. The circuit characteristics have been investigated through DC, AC, noise, and voltage-temperature variation analyses. The DC analysis establishes the operating point and verifies the proper biasing conditions of the transconductance stages, whereas the AC analysis evaluates the frequency response, transconductance characteristics, and bandwidth performance of the conventional architecture. Noise analysis is included to assess the spectral noise behavior and signal integrity of the circuit under small-signal

operation. Furthermore, voltage and temperature variation analyses are carried out to investigate the robustness and stability of the conventional CMOS VDTA under varying supply and environmental conditions. The corresponding simulation results are presented and discussed in the following plots

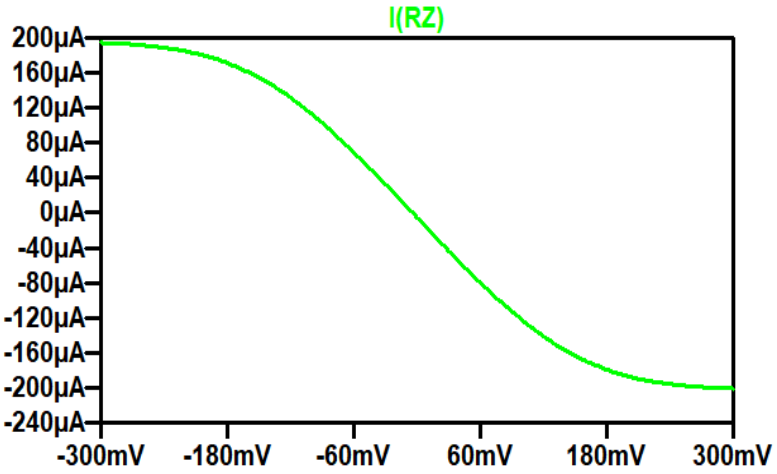

Figure 5: DC response of conventional CMOS-based VDTA configurations

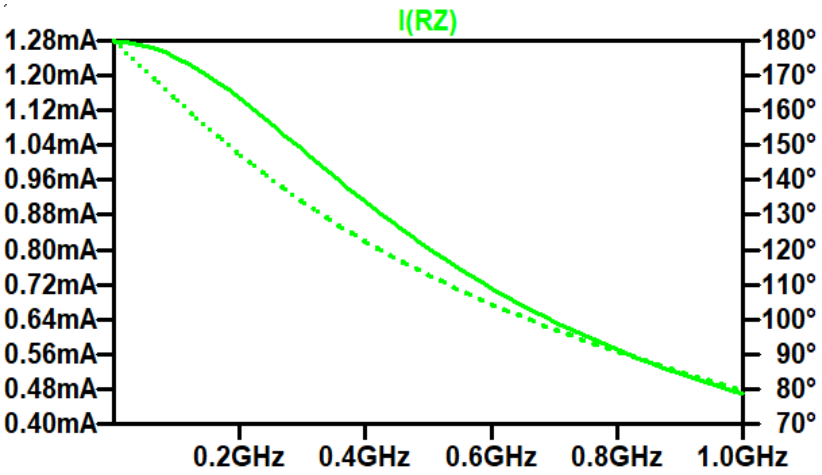

Figure 6: AC response of conventional CMOS-based VDTA configurations

Overall, the simulation results validate the proper operation of the conventional CMOS VDTA and establish it as a suitable reference architecture for evaluating the performance improvements achieved through the proposed enhancement techniques.

3.2. Floating gate MOSFET based VDTA

The input CMOS transconductance stage is replaced by a floating-gate MOSFET based realization to investigate the effect of capacitive charge sharing on the VDTA behaviour. In an FGMOS device, the control gate is established through capacitive coupling from multiple input terminals. This feature enables threshold-voltage modulation. In the present topology, the floating-gate is biased through a very large resistance connected to a reference node, while one or more capacitors C_i couple the input signals to the floating-gate node. The resistor provides a DC discharge path for leakage and charge accumulation, whereas the capacitors determine the AC coupling strength.

The floating-gate voltage is given by the capacitive division relation

$$V_{FG} = \frac{\sum_{i=1}^{n} C_i V_i + C_B V_B + C_{par} V_{par}}{\sum_{i=1}^{n} C_i + C_B + C_{par}} \qquad (3.7)$$

where C_i represents the input coupling capacitors, V_i are the applied input voltages, C_B is the bias coupling capacitance, V_B is the bias voltage, and C_{par} denotes the parasitic capacitance associated with the floating-gate node. For a simplified single-input case, the relation can be written as

$$V_{FG} = \frac{C_{in} V_{in} + C_B V_B}{C_{in} + C_B + C_{par}} \qquad (3.8)$$

The corresponding floating-gate transconductance stage generates a drain current that can be approximated, in saturation, by

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{FG} - V_{TH})^2 (1 + \lambda V_{DS}) \qquad (3.9)$$

and the small-signal transconductance becomes

$$g_{m,FG} \approx g_m \cdot \alpha_{in} \qquad (3.10)$$

where α_{in} is the capacitive coupling coefficient defined as

$$\alpha_{in} = \frac{C_{in}}{C_{in} + C_B + C_{par}} \qquad (3.11)$$

Equation (12) shows that the effective transconductance of the FGMOS stage is not only determined by the intrinsic MOS transconductance g_m, but also by the coupling factor α_{in}.

Hence, the overall gain is strongly influenced by the selected capacitor values and parasitic floating at the floating node.

The large resistor $R$and the total floating-node capacitance C_{FG} define the low-frequency pole of the floating-gate network as

$$f_{FG} = \frac{1}{2\pi R C_{FG}} \tag{3.12}$$

$$C_{FG} = C_{in} + C_B + C_{par} \tag{3.13}$$

The pole determines the frequency range over which the floating-gate node behaves as a quasi-static charge-sharing node. The FGMOS-based VDTA provides a modified transconductance response and slightly reduced bandwidth.

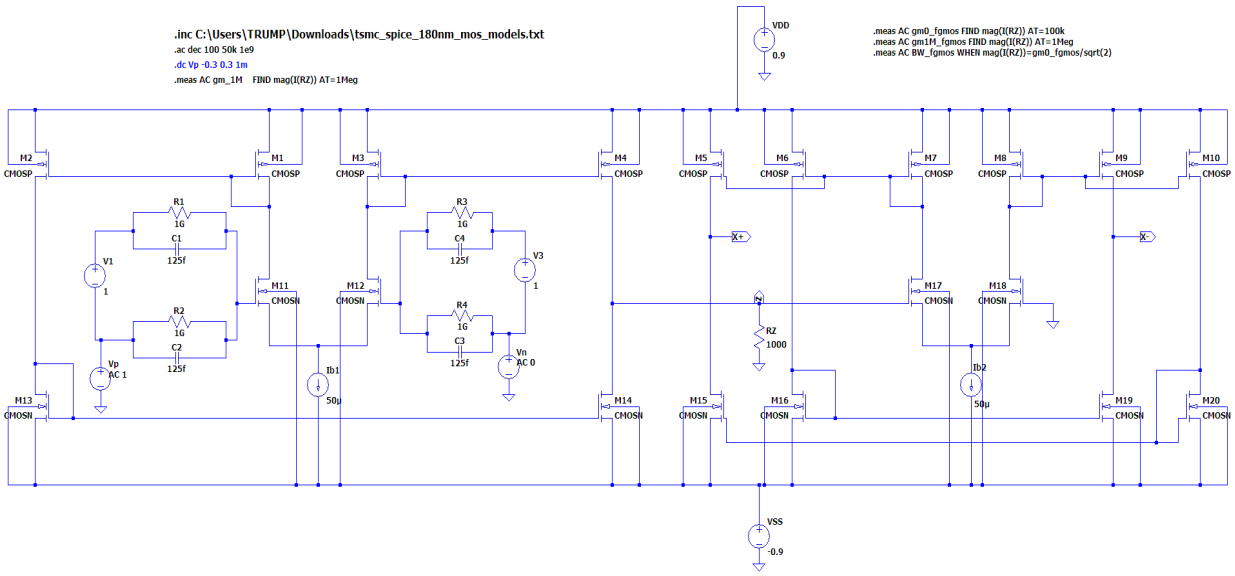

Figure. 7: FGMOS-based VDTA implementation

To examine the effectiveness of the floating-gate implementation, the FGMOS-based VDTA has been extensively simulated using LTspice in 180 nm CMOS technology. The proposed architecture has been evaluated through DC, AC, noise, and voltage-temperature variation analyses in order to investigate its low-voltage operating characteristics and overall analog performance. The DC analysis verifies the proper establishment of the floating-gate bias conditions and the operating point of the transconductance stages, while the AC analysis is used to study the frequency response, effective transconductance, and bandwidth behavior of the FGMOS-based realization. Noise analysis has been performed to evaluate the influence of floating-gate operation on the spectral noise characteristics of the circuit. In addition, voltage and temperature variation analyses are included to assess

the sensitivity and stability of the proposed architecture under changing operating conditions. The obtained results are presented in the subsequent sections for performance evaluation and comparison with the conventional CMOS implementation.

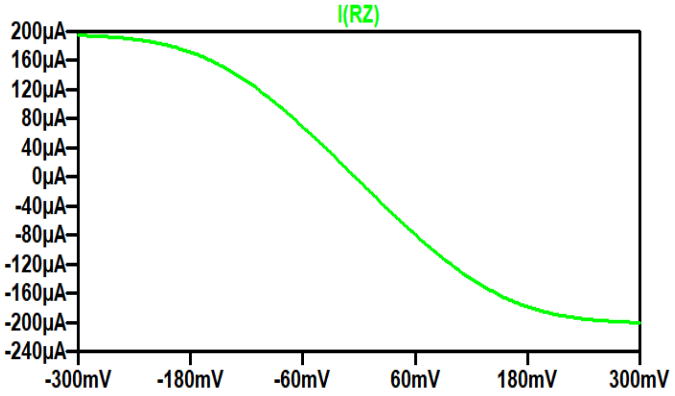

Figure 8: DC response FGMOS-based VDTA configurations

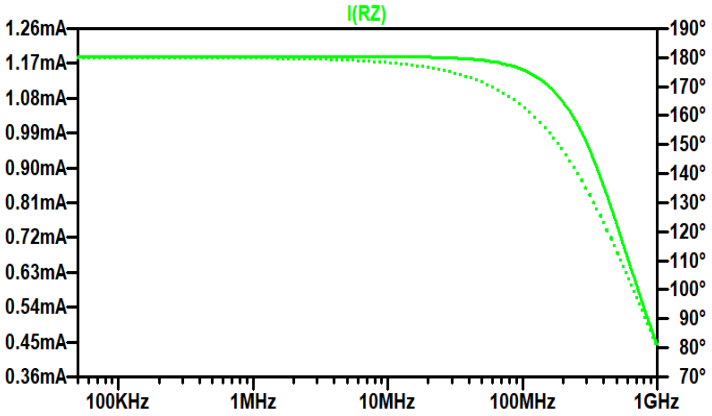

Figure 9: AC response FGMOS-based VDTA configurations

The obtained results confirm that the incorporation of FGMOS devices enables effective low-voltage operation while maintaining satisfactory transconductance and frequency response characteristics suitable for analog signal-processing applications.

CHAPTER 4

PARTIAL POSITIVE FEEDBACK ENHANCED VDTA

Partial positive feedback is an effective transconductance boosting technique widely employed in low-voltage analog circuits to enhance the small-signal gain and effective transconductance of differential stages without significantly increasing the bias current. The technique operates by introducing a controlled regenerative feedback mechanism through cross-coupled MOS transistors, which partially compensate the output conductance of the active load and strengthen the differential current transfer of the input stage.

In a conventional differential transconductance stage, the effective transconductance is limited by the intrinsic transconductance parameter g_m of the MOS devices and the available bias current. The incorporation of the cross-coupled transistor pair int the load section, a fraction of the output signal is positively fed back to the input nodes in phase with the differential signal. The regenerative action reduces the effective output conductance and introduces a negative incremental resistance at the output nodes. Consequently, the differential voltage developed across the active load increases, resulting in an amplified small-signal current response and an enhancement in the effective transconductance of the overall circuit.

The operation of the PPF structure can be studies through the small-signal analysis. g_{mp} represents the transconductance of the cross-coupled feedback transistors and g_{mn} represents the transconductance of the main differential pair, the effective transconductance may be approximated as:

$$g_{m,eff} = \frac{g_{mn}}{1-k} \tag{4.1}$$

where k denotes the positive feedback factor associated with the regenerative network. As the value of k approaches unity, the effective transconductance increases significantly due to the reduction in the equivalent output resistance of the load network. However, the excessive positive feedback may drive the circuit toward instability or latch-up conditions, therefore the feedback factor must remain below the critical limit required for stable operation.

The addition of PPF also modifies the pole structure of the amplifier. Since the regenerative action effectively increases the low-frequency gain, the dominant pole shifts towards the lower frequencies, resulting in a reduction in bandwidth. Thus, PPF inherently introduces a gain-bandwidth trade-off, where transconductance enhancement is achieved at the expense of the frequency response. Therefore, proper sizing and appropriate biasing conditions are therefore

necessary to obtain an optimum compromise among transconductance improvement, linearity, bandwidth, power dissipation and stability.

In the present works, the PPF technique is incorporated into the FGMOS-based VDTA architecture to enhance the effective transconductance of the input stage under low-voltage operating conditions. The regenerative feedback provided by the cross-coupled structure increases the current-driving capacity of the VDTA and improves its transconductance performance while maintaining low-power operation.

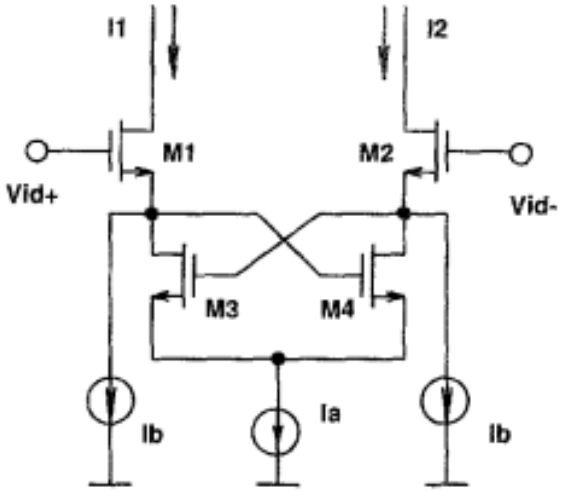

Figure 10: Cross-coupled partial positive feedback (PPF) structure used for transconductance enhancement in the proposed VDTA architecture [15]

The origin of transconductance enhancement in a PPF network may be understood from the reduction in effective output impedance produced by the regenerative path. In a conventional differential transconductance stage, the incremental output current is determined primarily by the intrinsic transconductance of the input pair and the finite output resistance of the active load. When a cross-coupled pair is introduced, a portion of the output voltage is coupled back in phase to reinforce the input differential signal. This action increases the incremental current response for a given input excitation and therefore increases the effective transconductance of the stage.

The corresponding effective gain of the stage may also be represented in a similar form as

$$A_{v,\text{eff}} = \frac{A_v}{1-\beta} \qquad (4.2)$$

where A_v is the small-signal gain of the uncompensated stage. Likewise, the effective output resistance is increased by the regenerative action of the feedback network and may be approximated as

$$R_{out,\text{eff}} = \frac{R_{out}}{1-\beta} \quad (4.3)$$

where R_{out} is the output resistance without feedback. These relations indicate that the PPF technique strengthens the current transfer capability of the circuit by effectively increasing the small-signal gain seen at the output nodes. In VDTA-based implementations, this translates into a larger output current for the same input differential voltage, thereby improving the effective transconductance of the Z-stage or X-stage depending on the point of feedback insertion.

From a frequency-domain perspective, the regenerative network modifies the pole locations of the amplifier. Since the low-frequency gain is increased, the dominant pole is shifted toward lower frequencies, and the bandwidth is reduced accordingly. A simplified first-order representation of this effect can be written as

$$\omega_{p,\text{eff}} \approx \omega_p(1-\beta) \quad (4.4)$$

$$f_{-3\text{dB,eff}} \approx f_{-3\text{dB}}(1-\beta) \quad (4.5)$$

where $\omega_p$and $f_{-3\text{dB}}$are the dominant pole frequency and 3-dB bandwidth of the uncompensated stage, respectively. This expression clearly reflects the gain-bandwidth trade-off associated with positive feedback. Although the transconductance enhancement is significant, the designer must ensure that βremains below unity so that the circuit remains stable and does not enter a latch-up or bistable condition. In practice, the feedback strength is selected such that the enhancement in transconductance is obtained while preserving an acceptable phase margin and linear operating range.

For the VDTA realization considered in this thesis, the PPF network is introduced in the input transconductance stage to increase the current conversion efficiency under fixed bias conditions.

The PPF technique is therefore particularly useful in applications where a higher transconductance is required without increasing the bias current, such as low-voltage filters, tuneable analog blocks, and current-mode signal-processing circuits. However, because the technique introduces a deliberate regenerative path, careful transistor sizing and bias optimization are necessary to achieve a practical compromise among transconductance enhancement, bandwidth, power dissipation, and circuit stability.

In the present work, the PPF technique is employed as a circuit-level enhancement strategy for the FGMOS-based VDTA. The objective is to exploit the low-voltage capability of the floating-gate input stage while using positive feedback to recover and improve the effective transconductance. This combination provides a useful design framework for analog building

blocks that must operate under limited supply voltage yet still require strong small-signal performance.

In the proposed architecture, the cross-coupled PMOS transistor pair provides a regenerative effect that behaves as a negative impedance, thereby strengthening the effective current conversion of the input stage. This increases the apparent transconductance without requiring a proportional increase in bias current. The PPF-enhancement in VDTA structures results in g_m improvement at the cost of reduced bandwidth.

For the proposed architecture, the effective transconductance may be expressed in the simplified firm as:

The gain enhancement factor due to partial positive feedback can be observed to be:

$$A_{PPF} = \frac{g_{m,eff}}{g_m} = \frac{1}{1-\eta} \tag{4.6}$$

which shows that the effective transconductance increases as the feedback factor approaches unity. For the differential input pair, the output current at Z-terminal can be written as:

$$I_Z = g_{m,eff}(V_P - V_N) \tag{4.7}$$

Now, substituting the value of $g_{m,eff}$,

$$I_Z = \frac{g_m}{1-\eta}(V_P - V_N) \tag{4.8}$$

In this work, PPF is therefore used as the final enhancement stage, allowing the VDTA to achieve a g_m higher while retaining the low-voltage benefits. To further increase the effective transconductance of the proposed FGMOS-based VDTA, a series-parallel current mirror is introduced in the load path of the input transconductance stage. The purpose of this addition is to reinforce the differential current generated by the FGMOS input stage without increasing the bias current of the circuit. In contrast to the conventional current mirror, the SPCM structure employs a series connection in one branch and a parallel connection in the complementary branch, thereby providing current amplification through stacking and current replication.

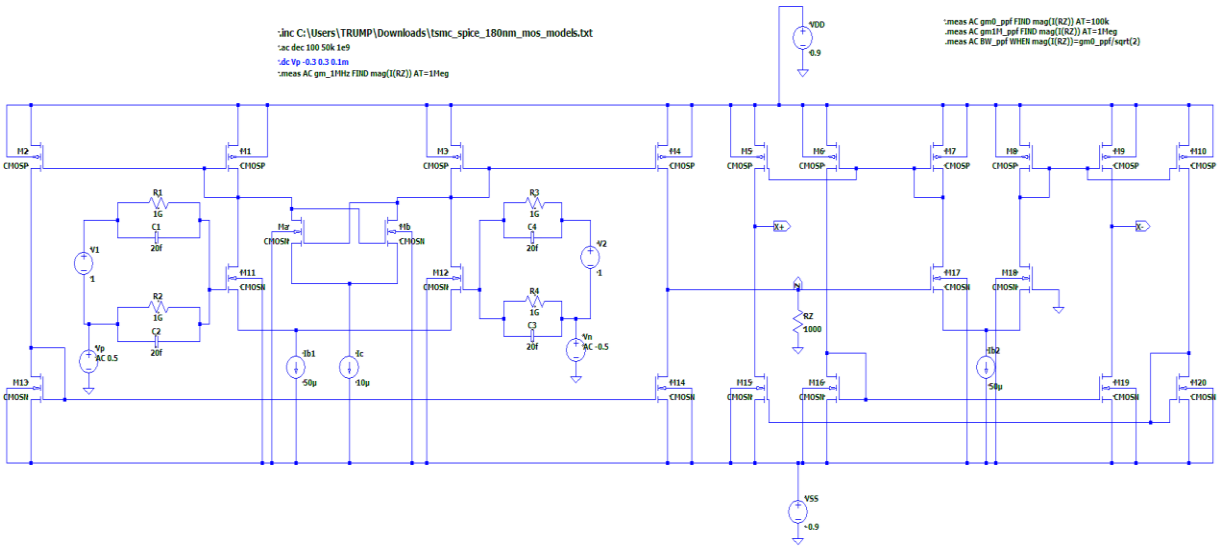

Figure 11: Proposed PPF-enhanced VDTA implementation

To validate the effectiveness of the partial positive feedback enhancement technique, the PPF-based VDTA architecture has been simulated in LTspice using 180nm CMOS technology. The performance of the proposed circuit has been investigated through DC, AC, noise analyses. The DC analysis is used to confirm the proper biasing of the regenerative feedback network and stable operation of the transconductance stage. The AC analysis evaluates the enhancement in effective transconductance, gain characteristics and the corresponding variation in bandwidth resulting from the introduction of the PPF technique. Noise analysis has also been carried out to study the influence of the regenerative feedback mechanism on the spectral noise performance of the circuit. Furthermore, voltage and temperature variation analyses are performed to examine the robustness and operational stability of the PPF-enhanced architecture under varying environmental and supply conditions. The obtained simulation results are discussed in the following sections to analyse the trade-offs between transconductance enhancement, bandwidth and stability.

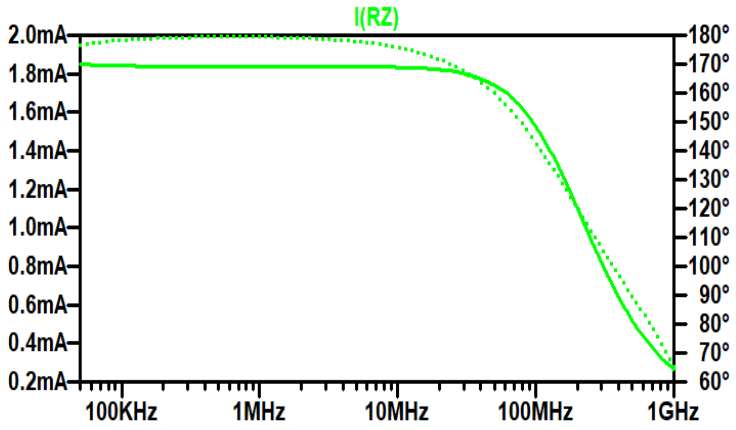

Figure 12: DC response of PPF-enhanced VDTA implementation

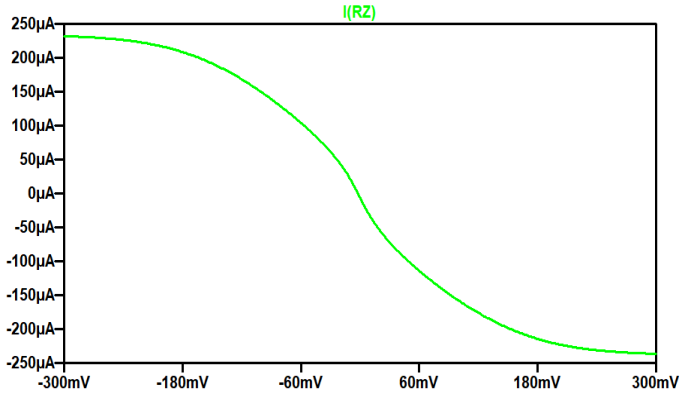

Figure 13: AC response of PPF-enhanced VDTA implementation

The simulated noise response exhibits a near constant behaviour across the central portion of the frequency band and exhibits a mild downward trend at higher frequencies, indicating that the circuit preserves stable small-signal behaviour with the useful operating range. This gradual variation is physically consistent with the finite bandwidth of the transconductance stage and the frequency-dependent attenuation of noise at the output node. Overall, the obtained response confirms that the proposed realization provides transconductance boosting without introducing any abnormal noise peaking or instability in the operating range.

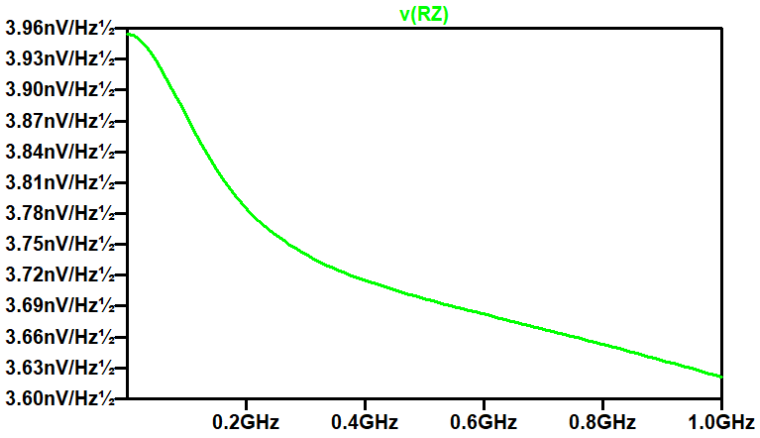

Figure 14: Noise characterisation of the PPF-enhanced VDTA

Overall, the simulation results demonstrate that the incorporation of partial positive feedback effectively enhances the transconductance performance of the FGMOS-based VDTA under low-voltage operating conditions, while exhibiting the expected trade-off between gain enhancement and bandwidth reduction.

In the temperature variations analysis, the circuit was simulated at $-20°C$, $27°C$, and $80°C$. The obtained responses indicate that the effective transconductance decreases progressively with increasing temperature. The highest transconductance decreases progressively with increasing temperature. The highest transconductance is observed at $-20°C$, while the lowest

5

response occurs at $80°C$. This behaviour is attributed to the reduction in carrier mobility at elevated temperatures, which lowers the current driving capability of the MOS transistors. A corresponding reduction in the high-frequency response is also observed with increasing temperature. However, the overall frequency characteristics remain stable without any abnormal gain peaking., thereby confirming reliable thermal stability of the proposed architecture.

The supply voltage variation analysis was further carried out for supply voltages of $\pm 0.8V$, $\pm 0.9V$, and $\pm 1.0V$. The obtained AC characteristics demonstrate that the effective transconductance increases gradually with increasing supply voltage due to improved transistor overdrive conditions and enhanced current transfer efficiency. The circuit exhibits only minor variation in bandwidth over the considered supply voltage range while maintaining stable overall frequency response characteristics. The absence of instability or excessive gain variation confirms the robustness of the proposed PPF-enhanced FGMOS-based VDTA under supply voltage fluctuations.

The obtained voltage and temperature variations results validate the operational stability of the proposed architecture and demonstrate its suitability for low-voltage applications operating under varying environmental conditions.

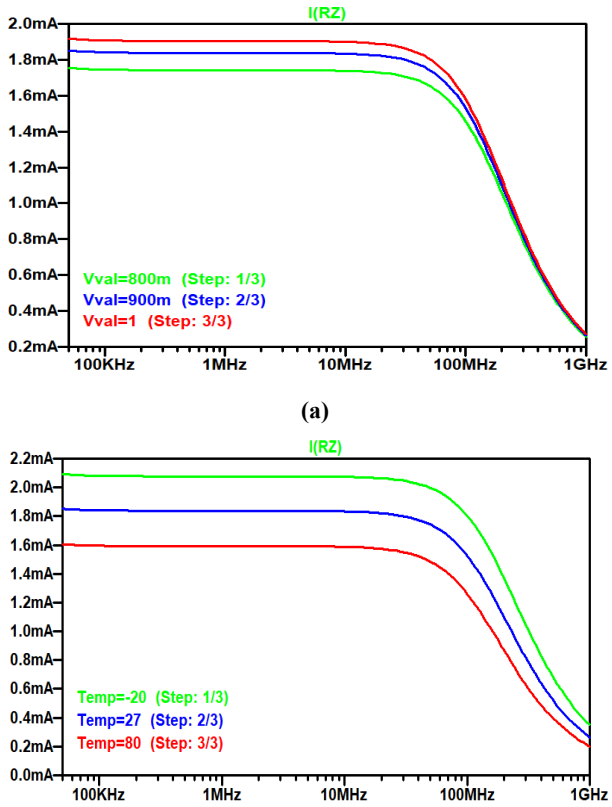

Figure 15: Voltage and temperature variation characteristics of the proposed PPF-enhanced FGMOS-based VDTA

9 Overall, the simulation results demonstrate that the incorporation of partial positive feedback effectively enhances the transconductance performance of the FGMOS-based VDTA under low-voltage operating conditions, while exhibiting the expected trade-off between gain enhancement and bandwidth reduction.

CHAPTER 5

SERIES-PARALLEL CURRENT MIRROR ENHANCED VDTA

The series-parallel current mirror technique is a transconductance enhancement approach employed in analog integrated circuits to improve current-driving capability, effective transconductance and gain characteristics while operation under low-voltage and low-power conditions. The technique utilizes a combination of series-connected and parallel-connected current mirror branches to achieve controlled current amplification and improved current distribution within the transconductance stage. In comparison with conventional current mirror configurations, the SPCM structure provides higher current transfer efficiency and better utilization of the available bias current, thereby enhancing the overall performance of the circuit.

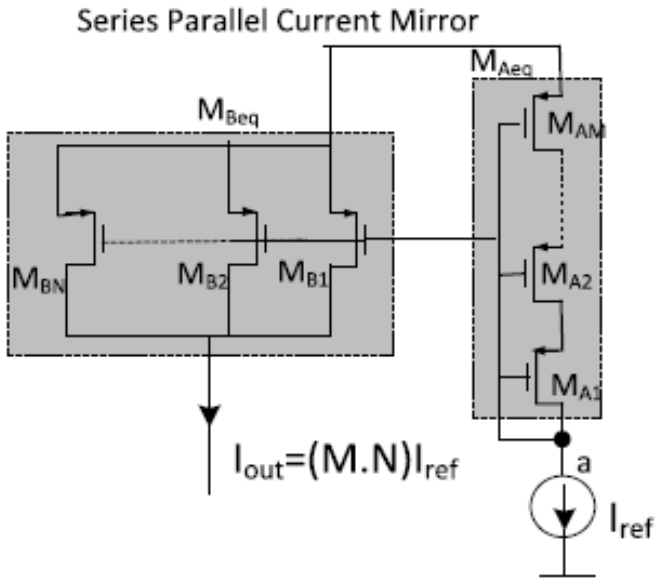

Figure 16: Series-parallel current mirror configuration for effective current multiplication and transconductance boosting [14]

In conventional differential transconductance stage, the output current is directly limited by the bias current and intrinsic device transconductance, the SPCM architecture overcomes this limitation by employing multiple current-mirroring paths that replicate and scale the differential signal currents. The parallel mirror branches increase the effective transconductance of the circuit without requiring a proportional increase in the effective output current capability, whereas the series-connected arrangement improves current transfer

accuracy and output resistance. As a result, the effective transconductance of the circuit increases without requiring a proportional increase in the static power dissipation.

The SPCM network effectively multiplies the signal current generated by the input differential pair. The enhancement in effective transconductance results in larger output currents for a given differential input voltage, thereby improving the gain and signal-processing capability of the active block.

An important advantage of the SPCM technique is that the transconductance enhancement is achieved through current replication rather than aggressive regenerative feedback. Consequently, the stability issues commonly associated with strong positive feedback structures are significantly reduced. Furthermore, the increase output resistance provided by cascaded current-mirroring paths contributes to improved gain characteristics and better current matching. However, the introduction of additional mirror stages increases parasitic capacitance at internal nides, which may shift the dominant poles of the circuit and reduce the overall bandwidth.

The working principle of the SPCM technique may be further interpreted in terms of current replication and effective gain multiplication in the transconductance stage. In a practical MOS current mirror, the mirrored output current is determined by the aspect-ratio ratio of the mirror devices and by the finite output resistance of the transistors. For an ideal current mirror, the output current can be expressed as

$$I_{out} = I_{ref}\left(\frac{(W/L)_{out}}{(W/L)_{ref}}\right) \qquad (5.1)$$

where $I_{ref}$is the reference current and $I_{out}$is the mirrored current. In the presence of channel-length modulation, the current becomes slightly dependent on the drain-to-source voltage and may be written as

$$I_{out} = I_{ref}(1 + \lambda V_{DS}) \qquad (5.2)$$

where $\lambda$is the channel-length modulation parameter. The SPCM configuration improves upon this conventional relation by using a composite mirror structure that provides a larger effective current transfer ratio through the combined action of series and parallel branches. This leads to a higher output current for the same input excitation, thereby increasing the effective transconductance of the VDTA stage.

For the input differential pair, the signal current may be written as

$$I_{id} = g_m V_{id} \qquad (5.3)$$

where $V_{id} = V_P - V_N$ is the differential input voltage. When the SPCM network multiplies this current by a factor n, the effective output current becomes

$$I_{out,eff} = nI_{id} = ng_m V_{id} \quad (5.4)$$

and hence the effective transconductance of the stage is given by

$$g_{m,eff} = ng_m \quad (5.5)$$

This expression shows that the SPCM technique enhances transconductance by increasing the current delivered to the output node without requiring a proportional increase in bias current. Since the enhancement is obtained through current-mirror reconfiguration rather than regenerative positive feedback, the circuit generally preserves stable small-signal operation and avoids the latch-up conditions that may arise in strongly feedback-biased structures.

Another important aspect of the SPCM topology is its effect on the small-signal output resistance. Since the series-connected branch increases the incremental resistance seen at the output node, the effective output resistance can be approximated as

$$R_{out,eff} \approx nR_{out} \quad (5.6)$$

where $R_{out}$is the output resistance of a conventional mirror branch. The increase in output resistance improves the current-source behavior of the stage and enhances the signal transfer capability of the VDTA. However, the additional devices required by the SPCM network introduce parasitic capacitances at internal nodes, and these parasitics influence the frequency response of the circuit. The dominant pole may be approximated by

$$\omega_p \approx \frac{1}{R_{out,eff} C_{par}} \quad (5.7)$$

where C_{par} represents the effective parasitic capacitance at the internal node. As $R_{out,eff}$ increases, the pole may shift to a lower frequency, which explains the observed reduction in bandwidth in SPCM-enhanced realizations. Thus, the technique introduces a gain-bandwidth trade-off, although the transconductance improvement is often substantial.

In the present works, the SPCM technique is incorporated into the FGMOS-based VDTA architecture to achieve substantial transconductance enhancement under low-voltage operating conditions. The current-mirroring network improves the effective current transfer capability of the transconductance stage and enables the VDTA to deliver significantly higher output currents compared to the conventional and the PPF-enhanced structures. This makes SPCM-based VDTA suitable for high-gain current-mode analog signal processing applications.

In the proposed VDTA architecture, the SPCM network is used as a local gain-enhancement element for the FGMOS input stage. If the series branch is formed using N identical MOSFETs and the parallel branch using M identical MOSFETs, the mirror output current can be ideally expressed as:

$$I_{out,SPCM} = (M \cdot N) I_{ref} \tag{5.8}$$

where I_{ref} is the reference current of the mirror. Under the assumption of matched devices and equal bias conditions, the effective differential current generated at the transconductor output is increased by approximately the same factor. Consequently, the effective small-signal transconductance of the proposed stage can be written as:

$$g_{m,\text{eff}} \approx (M \cdot N)\, g_{m,\text{FGMOS}} \tag{5.9}$$

where $g_{m,\text{FGMOS}}$ denotes the transconductance of the standalone FGMOS-based input stage. For the low-frequency region, this relation shows that the SPCM network provides a direct g_m multiplication effect, while the overall bias current remains essentially fixed. This is the key advantage of this approach, since g_m enhancement is achieved through current-mirror reconfiguration rather than through an increase in static power dissipation.

From a small-signal perspective, the transconductance boost arises because the SPCM reduces the effective loading seen by the floating-gate input node and increases the incremental current delivered to the next stage. A first-order representation of the boosted transconductance may be expressed as

$$g_{m,\text{SPCM}} \approx \alpha_{FG} \frac{(M \cdot N)\, g_{m,\text{MOS}}}{1 - \beta} \tag{5.10}$$

where α_{FG} is the capacitive coupling factor of the floating-gate node, $g_{m,\text{MOS}}$ is the intrinsic MOS transconductance, and β is the effective positive-feedback coefficient introduced by the mirror arrangement. Equation (18) indicates that the final transconductance is governed jointly by the floating-gate coupling and the mirror multiplication factor. Therefore, the proposed stage can be tuned to obtain a substantially larger g_m than the conventional CMOS and FGMOS realizations.

The enhancement, however is accompanied by a reduction in bandwidth because the current multiplication provided by the positive feedback increases the effective gain of the input stage and shifts the dominant pole to a lower frequency. This gain-bandwidth trade-off is consistent with the behaviour of SPCM-enhanced circuit variation. The SPCM-enhanced VDTA presents a structure with a significantly larger effective output current and a correspondingly higher transconductance while preserving the same bias current range, this results in a reduction in bandwidth.

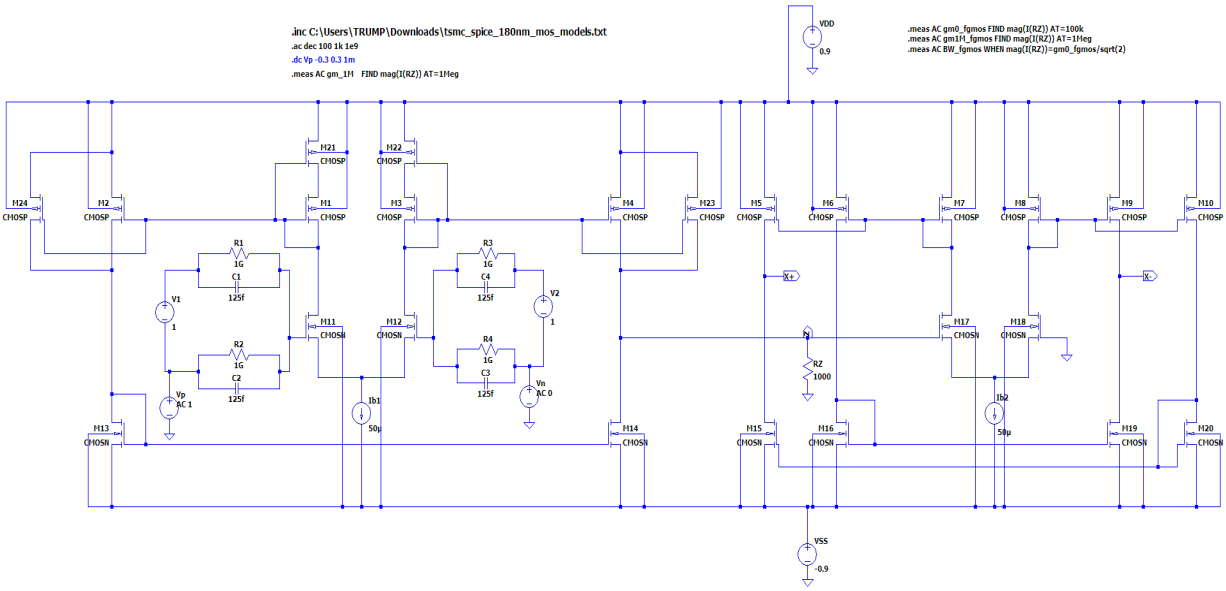

Figure. 17: Proposed SPCM-enhanced VDTA implementation

The performance of the SPCM-enhanced VDTA has been investigated throigh extensive simulations performed in LTspice using 180nm CMOS technology. To evaluate the effectiveness of the series-parallel current mirror technique, the proposed architecture has been subjected to DC, AC and voltage temperature variation analyses. The DC analysis verifies the correct operation of the modified current mirror network and establishes theoperating point of the transconductance stages. The AC analysis is employed to evaluate the enhancement in the effective transconductance, gain behaviour and bandwidth characteristics achieved through the SPCM configuration. The voltage and temperature varuiation analyses are carried out to investigate the robustness and stability of the proposed architecture under varying operating conditions.The corresponding simulation results are presented in the following plots.

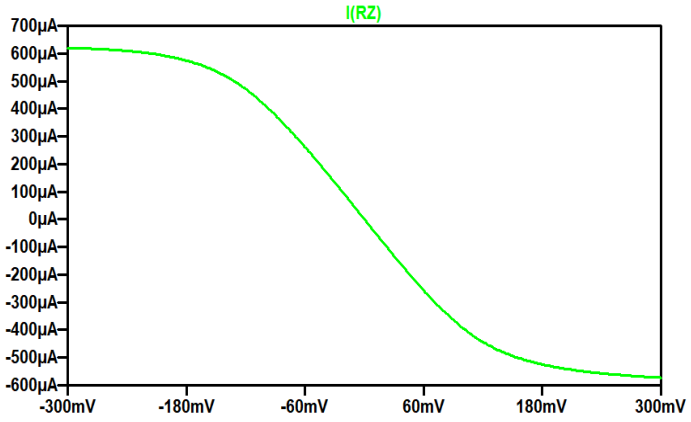

Figure 18: DC response of SPCM-enhanced VDTA

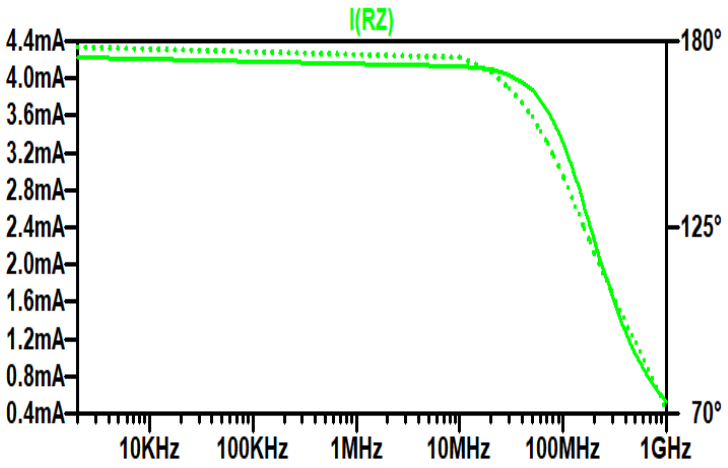

Figure 19: AC response of SPCM-enhanced VDTA

The simulation results indicate that the SPCM technique provides substantial transconductance enhancement through improved current transfer efficiency, thereby making the proposed architecture suitable for high-gain current-mode analog applications operating under low-voltage conditions.

CHAPTER 6

COMPARATIVE RESULTS AND DISCUSSION

The performance of the proposed VDTA is evaluated for the four implementations. The principal performance metrics considered in this study are the effective transconductance and the -3dB bandwidth, extracted from small-signal AC analysis. DC analysis is also performed to verify proper biasing and stable circuit operation across all three configurations. The conventional CMOS VDTA serves as the reference and exhibits a transconductance of approximately 1.27 mS with a bandwidth of about 405.7 MHz. This result represents a balanced trade-off between transconductance and frequency response and provides a suitable benchmark for evaluating the impact of the subsequent modifications. When the input stage is replaced by an FGMOS-based realization, the transconductance is observed to be approximately 1.19 mS, while the bandwidth increases slightly to around 414 MHz. This behavior is attributed to the capacitive coupling at the floating-gate node, which modifies the effective gate control and shifts the operating point. A significant enhancement is obtained when the PPF-enhanced technique is used, an effective transconductance of 1.84 mS is obtained with bandwidth of 148MHz. then with the SPCM technique is incorporated into the FGMOS-based VDTA. In this case, the effective transconductance increases to approximately 4.23 mS, corresponding to more than a threefold improvement over the conventional CMOS design. The transconductance boost is achieved without increasing the bias current. The enhancement in transconductance is accompanied by a reduction in bandwidth to approximately 126.3 MHz.

VDTA Scheme	$I_b(\mu A)$	g_m(mS)	BW (MHz)
Conventional CMOS VDTA	50	1.27	405.7
FGMOS-based VDTA	50	1.19	414
PPF-enhanced VDTA	50	1.84	148
SPCM-enhanced VDTA	50	4.23	126.3

Table 2: Performance Comparison of VDTA Implementations

The proposed results are compared with the performance of existing VDTA-based structures. Since, the published works use different circuit parameters used for simulation, thus this comparison can be interpreted as a trend-based benchmark. Narang and Aggarwal reported DTMOS/FD-FVF-based VDTAs in 180 nm CMOS, obtaining transconductance values of

22 415.62 µS and 422.89 µS with bandwidths of 225.9 MHz and 296.21 MHz, respectively, at a bias current of 10 µA. Rani et al. later proposed transconductance-boosted VDTA structures using partial positive feedback and gate-to-source voltage enhancement, reporting gm enhancement of 140% and 53% with -3 dB frequencies of 160 MHz and 630 MHz, respectively. These results confirm that feedback-assisted techniques can significantly improve transconductance, although at the cost of a bandwidth penalty in certain cases. Table 3 presents a comparison between the proposed VDTA and selected existing structures.

Ref.	VDTA Topology	Supply Voltage (V)	Bias Current (μA)	g_m (S)	BW (MHz)	Key Observation
Proposed	CMOS	±0.9	50	1.27 m	405.7	Baseline reference
Proposed	FGMOS	±0.9	50	1.19 m	414	Floating-gate input stage
Proposed	PPF-Enhanced	0.9	50	1.84 m	148	Enhanced transconductance using PPF
Proposed	SPCM-enhanced	±0.9	50	4.23 m	126.3	Highest g_m in this study
[3]	FD-FVF/DTMOS (proposed-I)	±0.7	10	415.62 μ	225.9	Low-voltage operation
[3]	FD-FVF/DTMOS (proposed-II)	±0.5	10	422.89 μ	296.21	Lower supply, improved BW
[13]	PPF-based boosted	±0.6	50	140% improvement	160	Strong gm enhancement
[13]	Inverting-amplifier boosted	±0.6	50	53% above conventional	630	Moderate gm boost, higher BW

Table 3: Comparison between the proposed VDTA and existing structures having technology 180nm

The comparison indicates that the proposed circuit with the combination of FGMOS and SPCM technique achieves a higher transconductance than the reference CMOS VDTA and also exceeds the reported boosted transconductance VDTA trends. Overall, the results demonstrate that the FGMOS devices introduce flexibility in biasing and input coupling and the addition of the SPCM technique increases the effective transconductance. Thus, making the proposed architecture is suitable for low voltage operation with boosted transconductance.

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CHAPTER 7

CONCLUSIONS

This thesis has presented the design, implementation, and comparative evaluation of several VDTA realizations based on a conventional CMOS architecture, an FGMOS-based input stage, and two transconductance enhancement techniques, namely partial positive feedback (PPF) and series-parallel current mirror (SPCM). The conventional CMOS VDTA was employed as the benchmark structure to establish a reference point for transconductance, bandwidth, linearity, and overall small-signal performance. The modified architectures were then investigated to assess the extent to which device-level and circuit-level enhancement techniques can improve the suitability of VDTA structures for low-voltage current-mode analog signal-processing applications.

The incorporation of FGMOS devices at the input stage demonstrated that capacitive coupling and threshold-voltage modulation can be effectively exploited to reduce the voltage headroom required for circuit operation. This enables the VDTA to function reliably under low-supply-voltage conditions, which is a critical requirement in deep-submicron analog design. The floating-gate configuration also provides flexibility in controlling the effective gate potential through capacitive division, thereby allowing the input stage to be biased more efficiently than in a conventional gate-driven CMOS implementation. The simulation results confirm that the FGMOS-based realization preserves the fundamental functionality of the VDTA while improving low-voltage operability.

The first enhancement approach investigated in this thesis, namely PPF, was introduced to increase the effective transconductance of the FGMOS-based VDTA through regenerative feedback. By incorporating a controlled positive feedback path in the active load section, the input differential signal is reinforced, resulting in an increase in the effective current conversion capability of the transconductance stage. This mechanism significantly improves the transconductance compared to the conventional CMOS realization. However, the enhancement is accompanied by a reduction in bandwidth, which is consistent with the well-known gain-bandwidth trade-off inherent to positive-feedback-based circuits. The results therefore indicate that PPF is particularly suitable when higher transconductance is required and a moderate reduction in frequency response is acceptable.

The second enhancement approach, based on SPCM, was used to further increase the current-driving capability of the FGMOS-based VDTA. In this structure, the current mirror network is reconfigured using series and parallel branches to improve current replication and transfer efficiency without increasing the bias current. The SPCM technique strengthens the effective output current delivered by the transconductance stage and produces a marked increase in overall transconductance. Among the investigated realizations, the SPCM-enhanced architecture exhibited the highest transconductance, demonstrating that mirror-based current amplification can be an effective means of boosting VDTA performance within a fixed power budget. As in the case of PPF, this improvement is achieved with a bandwidth penalty, thereby confirming that transconductance enhancement and frequency response must be traded off against one another in practical analog design.

15 The simulation results obtained in 180 nm CMOS technology using LTspice validate the effectiveness of the proposed approaches under identical operating conditions. The conventional CMOS VDTA yielded a transconductance of 1.27 mS with a bandwidth of 405.7 MHz. The PPF-enhanced version increased the transconductance to 1.84 mS, while reducing the bandwidth to 148 MHz. The SPCM-enhanced realization achieved a transconductance of 4.23 mS with a bandwidth of 126.3 MHz. These results clearly establish that both enhancement techniques are capable of substantially improving transconductance, though each does so through a different mechanism and with a distinct impact on bandwidth and circuit response. The DC transfer characteristics confirmed proper biasing and linear operation in the intended signal range, while the AC analysis demonstrated the frequency-domain trade-offs introduced by the enhancement networks. Additional noise and variation analyses further indicated that the proposed structures maintain acceptable robustness under operating changes.

Overall, the thesis shows that FGMOS, PPF, and SPCM constitute practical and effective design strategies for improving VDTA performance in low-voltage current-mode analog systems. The FGMOS device provides the basic low-voltage operating advantage, PPF offers regenerative transconductance enhancement, and SPCM yields strong current-mirror-based gain boosting. Taken together, these results demonstrate that the proposed VDTA architectures can serve as suitable active building blocks for analog filters, tuneable transconductor, and other current-mode signal-processing circuits where design objectives such as transconductance, bandwidth, supply voltage, and power dissipation must be carefully balanced.

APPENDICES

LIST OF PUBLICATIONS

17

1. "FGMOS based VDTA with transconductance boosting techniques", 2nd IEEE Uttar Pradesh Section Women in Engineering International Conference on Electrical Electronics and Computer Engineering (UPWIECON-2026), NIELIT India – ***Accepted,*** **Scopus indexed**.

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2. "FGMOS-based VDTA realizations with enhanced performance", 6th International Conference on Emerging Trends and Technologies on Intelligent Systems (ETTIS 2026) – ***Accepted***

   Conference proceedings in Springer Book Series "*Lecture Notes in Networks and Systems" (LNNS*), **Scopus indexed**.

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14. P. Gupta, S. Bansal, L. Singla, and J. Gupta, “Realization of a New CMOS Transconductance Boosted Voltage Differencing Inverting Buffered Amplifier (TB-VDIBA) using Series Parallel Current Mirror (SPCM),” Journal of Circuits, Systems, and Computers, vol. 34, no. 10, 2025.

15. R. Wang and R. Harjani, "Partial positive feedback for gain enhancement of low-power CMOS OTAs," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 21–35.