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SMART ECO FILL FOR FASTER DESIGN CYCLE AND DFM AT DEEP SUB-MICRON TECHNOLOGY

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SMART ECO FILL FOR FASTER DESIGN CYCLE AND DFM AT DEEP SUB-MICRON TECHNOLOGY

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by

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CANDIDATE'S DECLARATION

I, MUSKAN SINGH (Roll No. 2K24/VLS/20), hereby declare that the thesis titled **'Smart ECO Fill for Faster Design Cycle and DFM at Deep Sub-Micron Technology'**, submitted in partial fulfilment of the requirements for the award of the degree of Master of Technology in the Department of Electronics and Communication Engineering at Delhi Technological University, is based on my original work carried out during the period from June 2025 to May 2026 under the guidance of **Prof. Alok Kumar Singh**.

I further confirm that this thesis has not been submitted, either fully or partially, for the award of any other degree or academic qualification at any other institute or university.

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CERTIFICATE BY THE SUPERVISOR(s)

This is to certify that MUSKAN SINGH (Roll No. 2K24/VLS/20) has successfully completed the research work presented in the thesis titled **"Smart ECO Fill for Faster Design Cycle and DFM at Deep Sub-Micron Technology"** in partial fulfilment of the requirements for the award of the degree of Master of Technology in the Department of Electronics and Communication Engineering, Delhi Technological University, under my guidance and supervision.

The work presented in this thesis is original and has been carried out independently by the candidate. To the best of my knowledge, the thesis or any part of it has not been submitted previously for the award of any degree or diploma at this or any other university/institution.

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ABSTRACT

One of the driving factors in the semiconductor industry is technology scaling, while technology scaling is enabling the higher number of devices in smaller area by shrinking devices.

The continuous growth in transistor integration has significantly improved chip capability and functionality within compact silicon area. However, scaling down metal interconnect dimensions introduces several manufacturing and reliability challenges, requiring additional process optimization and layout-aware fabrication techniques, leading to increasing complexity in the processes being used and also posing the challenges in increased design rules (Design rules check - DRC) and design for manufacturability (DFM) requirements for better yield. [5]

The DFM process/data includes two major steps, first is with adding special cells to the design to meet the density of diffusion and poly and secondly with dummy metal insertion in the design to meet the metal density. [5]

The DRC and DFM complexity are growing exponentially as we are moving towards deep submicron technologies. Hence, design convergence time for DRC and DFM is also going higher. This is resulting in larger time taken for DRC and DFM convergence compared to earlier technology nodes, which means the above process needs to start much earlier in the design cycle than previous process generation. Taking more time for LV convergence reduces the time available for late ECOs which are due to bug-fixes, timing, noise, power and other design fixes. The current ECO implementation tools cannot handle design with DFM. Designers need to remove the DFM data to implement late ECOs and then re-insert the DFM data and then post – DFM DRC cleaning is required. This adds to the overall schedule and large effort for each ECO cycle. Hence there is a need for tool/flow/methodology which can help in implementing ECOs post DFM, thereby reducing schedule impact due to late ECOs. The aim of the project is to provide the design/tool/methodology solution to the problem described above and enable taking in late ECOs in design without affecting schedule. [5]

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CHAPTER 1

INTRODUCTION

In 1965, Gordon Moore observed that the number of transistors integrated onto a semiconductor chip was increasing at a rapid rate over successive years [1]. The observation that later became known as Moore's Law suggested that transistor count on semiconductor chips would continue increasing with each generation of technology development [1]. This trend contributed significantly to device miniaturization and improvements in fabrication processes over time. Progress in semiconductor manufacturing also enabled a greater number of transistors to be integrated within a limited chip area while reducing defects and improving the processing capability of modern computing systems.

As VLSI technologies move toward smaller feature sizes, integrated circuits become more vulnerable to process and manufacturing variations [2]. For semiconductor industries, reducing design and development time while maintaining manufacturing reliability remains an important objective. Present-day chip development is affected by multiple factors such as fabrication constraints, verification challenges, and continuously changing market expectations. Because of these factors, achieving efficient design convergence and reducing product development time have become important considerations during modern chip implementation processes [2]. Therefore, efficient manufacturing convergence and faster time-to-market strategies have become important factors for improving product competitiveness and large-scale deployment efficiency [8]

1.1 ASIC DESIGN FLOW

It is essential to have an idea of exactly what type of chip one wants to design beforehand. The design process begins with an initial concept, which gradually evolves into different stages before reaching the final implementation. The first step involves defining design specifications based on the required functionality of the chip [2]. These specifications generally include performance targets, power consumption limits, area constraints, selected fabrication technology, and operational requirements. As the implementation progresses through synthesis, placement, routing, and verification stages, the design is transformed into optimized physical representations [2][7].

To manage the increasing complexity of large designs, the system is commonly divided into smaller functional blocks that interact through predefined interfaces. The architectural structure, such as RISC/CISC organization, ALU design, and pipelining techniques, is also finalized during this stage. Timing verification is performed

throughout the design flow to ensure reliable circuit operation. Static Timing Analysis (STA) is widely used to detect setup, hold, and propagation delay violations and verify that the implemented design satisfies performance requirements after physical implementation [10].

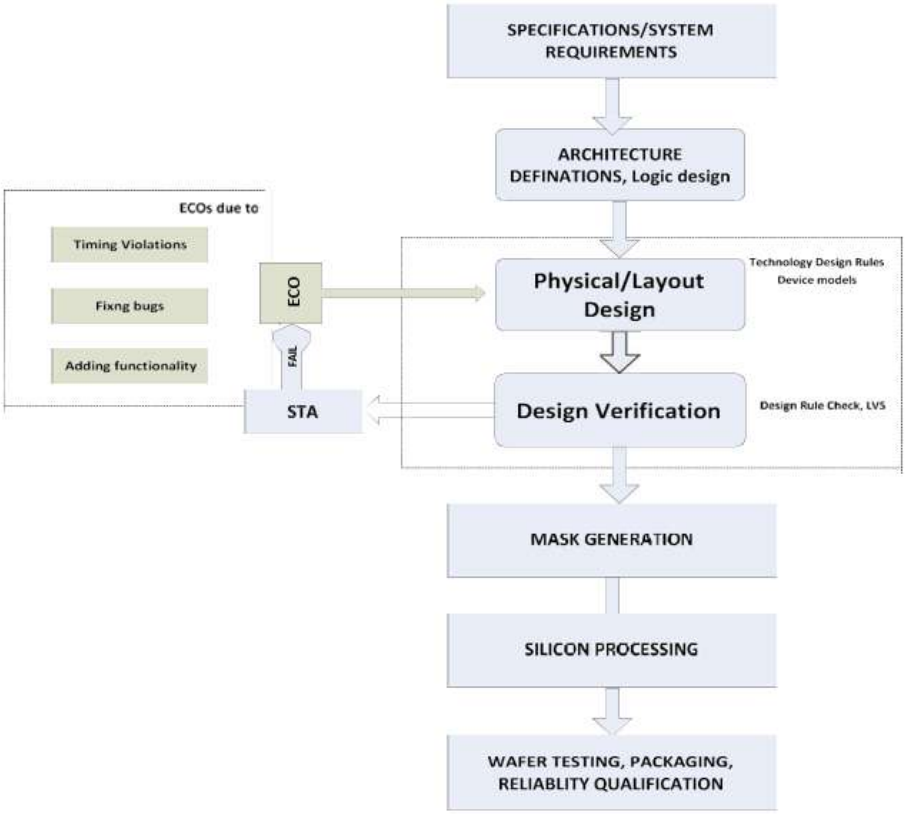

Fig. 1.1 ASIC Design Flow

1.2 Physical Verification

After completion of the backend design stages, the generated implementation must be verified carefully to ensure that it performs as intended from both electrical and logical perspectives. During this stage, certain issues identified during verification may be considered acceptable if they do not significantly affect circuit functionality, performance, or reliability. However, when errors have the potential to impact the behavior of the design, appropriate modifications become necessary. Such changes are generally kept minimal because extensive alterations can introduce additional design complications and increase verification effort. In practice, engineers prefer localized modifications so that the impact on already validated sections of the design remains limited. Therefore, layout updates at this stage are commonly performed by

experienced design engineers using careful analysis and optimization techniques before final implementation.

PV checks are:

Design rule checking (DRC) ensures that the layout satisfies manufacturing constraints defined for a particular technology [6]. These rules include parameters such as minimum line width, spacing between adjacent structures, and via-related requirements. Additional conditions may vary depending on process technology and interacting layers. Violating these rules can introduce manufacturing defects and functional issues, making DRC an essential step for ensuring reliable chip implementation [6].

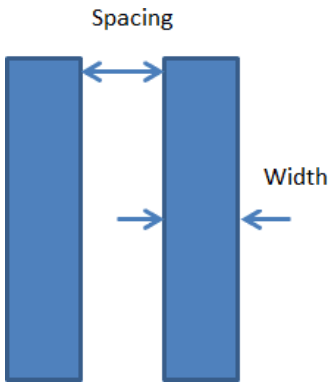

Fig. 1.2 DRC rule for Spacing

Layout versus schematic (LVS) is carried out to compare the connectivity information obtained from the physical layout with the intended circuit netlist generated during synthesis stages [6] [7]. The main purpose of this verification process is to confirm that the implemented layout preserves the intended logical behavior and accurately reflects the original circuit design.

Antenna verification is used to detect charge accumulation effects that may develop on floating interconnect structures during fabrication processes such as plasma etching [6]. Excessive charge generation during these stages can create reliability issues by affecting sensitive transistor gate structures. Therefore, appropriate routing techniques and protection mechanisms are incorporated to minimize such effects and maintain reliable circuit operation.

Electrical rule checking (ERC) is performed to verify the correctness of power distribution and signal behavior within an implemented design. During this process, several electrical parameters such as ground connectivity, transition characteristics, capacitive loading, and fan-out limitations are analyzed to identify potential electrical

issues [6] [10]. These verification checks contribute to maintaining reliable and stable circuit operation during practical implementation.

After completion of physical verification stages, the finalized layout database is prepared for semiconductor fabrication through photolithographic mask generation. The manufactured wafer is subsequently divided into individual dies, followed by chip packaging and functional testing procedures prior to deployment.

1.3 DFM

As VLSI technology continues to advance into smaller production nodes, designers and manufacturing companies have encountered a previously overlooked set of yield-related issues. To address these yield problems, the semiconductor industry has adopted new tools and techniques known as design for manufacturing (DFM) [5].

DFM has become a key area of research within the semiconductor industry. While deep-submicron processes allow for the creation of compact, high-performance chips, working within the nanometer scale introduces significant challenges in terms of manufacturability. Basically, nanometer technologies lead to lower yields, reduced reliability, and poorer test results, which have a major impact on the time it takes to generate profit. These factors are driving design teams to modify traditional design processes. At the same time, the pressure to bring products to market quickly is pushing companies to start mass production before defect levels are considered acceptable. Due to these trends, a company's success in producing functional silicon at advanced manufacturing nodes depends on how quickly it can develop working designs, ensuring high yield [2]. The design for manufacturing (DFM) methodology focuses on reducing defects that may arise during semiconductor production processes. By addressing manufacturability-related issues at earlier design stages, the need for repeated design modifications can be minimized, leading to shorter development cycles and reduced overall production cost [5].

As VLSI technology advances toward process nodes beyond 22 nm, the complexity associated with interconnect layouts satisfying Place and Route (PNR) and Static Timing Analysis (STA) constraints continues to increase [12]. Consequently, Design for Manufacturing (DFM) verification has become increasingly important for maintaining manufacturing reliability and improving yield performance [5] [12].

1.4 Importance of DFM

Chemical Mechanical Polishing (CMP) plays an important role in semiconductor fabrication as it is used to obtain a uniform and planar surface during manufacturing processes. The performance of CMP is strongly influenced by how evenly the layout density is distributed across different regions of the chip. Variations in metal density may lead to surface-related defects such as metal dishing and dielectric erosion. These imperfections can negatively influence lithography accuracy, affect interconnect performance, and reduce the overall manufacturing yield of the fabricated device [5] [11].

In advanced deep sub-micron technologies, maintaining balanced routing density has become increasingly important due to higher device integration and reduced process margins [13]. To overcome density imbalance issues, additional dummy metal structures are inserted into sparse layout regions to improve planarization quality and enhance manufacturing consistency after CMP processing [12] [15].

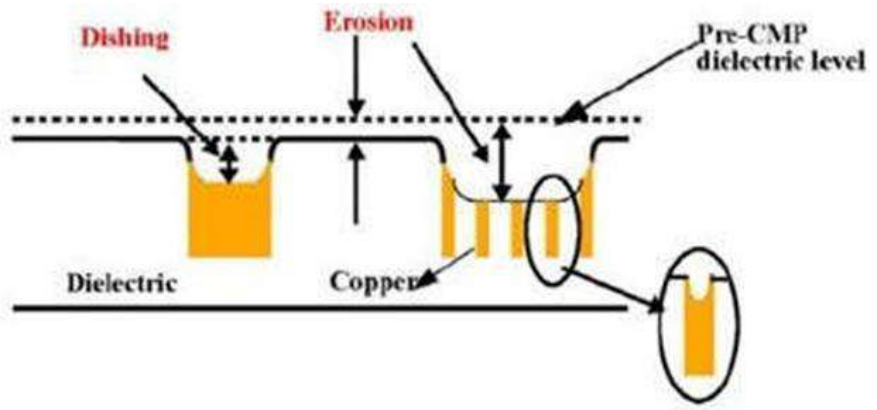

Fig. 1.3 Metal dishing and dielectric erosion

In modern technology, designs have a high number of devices packed into a small area, typically less than 1 cm^2. To support this high device density, fabrication processes often use multiple metal layers.

There are two main methods for inserting dummy metal, one of them is rule-based and the other is model-based. Layout must meet certain density requirements to ensure good post-CMP results. The density criteria dictate how much dummy material should be added so that the layout density stays within a range of acceptable minimum and maximum values. Rule-based methods focus on filling empty areas in the layout to meet density rules for both overlapping and non-overlapping sections of the design. [11]

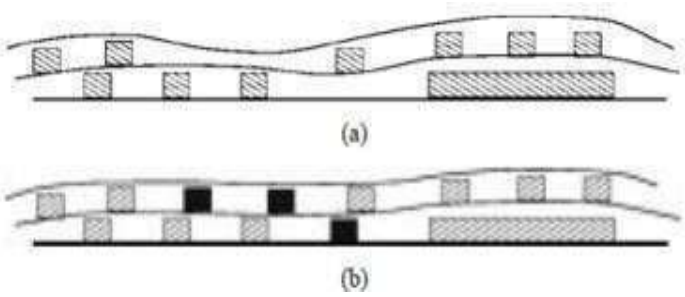

Fig. 1.4 ILD planarization due to non-uniform layout density

(a) before dummy metal fill insertion

(b) after dummy metal fill insertion (black tiles)

Design for Manufacturability (DFM) and Design for Yield (DFY) methodologies have become increasingly important in advanced semiconductor technologies, where fabrication reliability depends on close interaction between circuit implementation, physical layout optimization, and manufacturing-aware verification processes [5][15]. Modern integrated circuit designs such as System-on-Chip (SoC), mixed-signal architectures, and deep sub-micron implementations require coordination across multiple stages of the physical design flow to achieve acceptable yield and reliable post-fabrication performance. [12]

The design for manufacturing (DFM) philosophy aims to reduce defects that happen during the manufacturing process, which in turn reduces the need for design revisions and shortens production time, ultimately lowering the total cost of the product. As VLSI technology continues advancing toward smaller process nodes beyond 22 nm, the complexity associated with physical layout design increases significantly. Satisfying conventional design constraints alone is no longer sufficient to ensure reliable circuit operation after fabrication. The reduction in feature dimensions and the growing complexity of layouts make manufacturing processes more sensitive to variations during stages such as critical dimension (CD) control, chemical-mechanical polishing (CMP), and lithography. Because of these challenges, Design for Manufacturing (DFM) verification has become an important requirement for achieving reliable fabrication and improved manufacturing yield [5].

CHAPTER 2

ECO

Engineering Change Orders (ECOs) are widely applied during the later stages of VLSI implementation for introducing functional corrections, timing improvements, and localized routing modifications without repeating the complete physical design flow [4] [8]. Re-implementing an entire design after identifying errors at advanced stages can significantly increase both development effort and overall design time.

For advanced semiconductor technologies, regenerating photomasks for all fabrication layers after detecting design issues can increase manufacturing cost as well as turnaround time. To reduce this overhead, metal-only ECO methodologies modify only selected interconnect layers while preserving already validated portions of the layout database [17] [18]. This methodology supports efficient implementation of post-layout modifications and helps reduce fabrication cost while maintaining previously verified design information and improving tape-out schedule efficiency [4] [20].

During the initial stages of IC implementation, designers often reserve unused logic resources known as spare cells at different locations within the layout to support future design changes [8] [17]. When post-layout bugs or functional updates are identified, these spare cells can be utilized for introducing localized netlist modifications without affecting major portions of the existing physical design.

Typically, spare cells remain connected to predefined logic states until they are required during ECO implementation. The necessary design changes are introduced by selectively reconnecting the inputs and outputs of these cells while maintaining functional equivalence with the intended circuit behavior [18]. After modification, formal verification and timing analysis procedures are carried out to validate the correctness of the updated design [6] [10].

ECO methodologies are generally classified according to the nature of modifications introduced within the design flow. Functional ECOs mainly address logic corrections and specification changes, whereas timing ECOs focus on improving signal delays, transition behavior, and load balancing across critical paths [8] [18].

Compared with repeating the complete implementation flow, ECO-based approaches considerably reduce redesign effort, implementation cost, and turnaround time. However, performing ECO modifications during the final tape-out stages may become more challenging because the available routing flexibility and optimization resources are limited [4] [20].

2.1 Types of ECOs

Non-Freeze Silicon ECO

Before the base implementation layers are finalized, ECO modifications can be introduced at stages such as RTL, gate-level netlist, or placement with greater design flexibility [8] [18]. During these phases, additional logic elements and routing resources can still be inserted or optimized with relatively fewer implementation constraints. Once the lower fabrication layers become fixed, modifications are generally restricted to upper metal layers. Such approaches are commonly referred to as metal-only ECO techniques because they preserve previously validated base-layer structures while allowing required design updates [4] [20].

Freeze Silicon ECO

Once the base silicon layers are frozen, introducing additional standard cells into the design becomes highly restricted. Under such conditions, ECO implementation primarily relies on pre-inserted spare cells and localized routing modifications to achieve the required functionality updates [17] [18].

Since the lower fabrication layers remain unchanged, routing updates can be performed in parallel with manufacturing preparation stages, thereby reducing redesign overhead and shortening implementation turnaround time. Reusing previously validated base-layer masks also helps minimize photomask cost during subsequent tape-out iterations [4] [8].

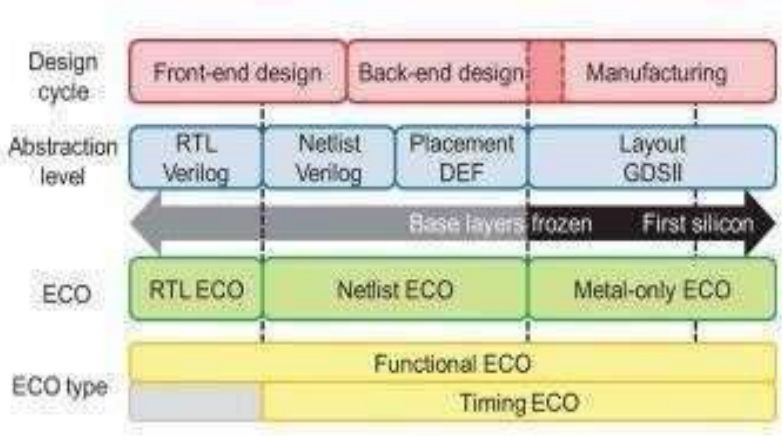

Fig. 2.1 ECO Type and ECO Stages

2.2 ECO Design Flow

Typical ECO Design Flow

A typical manual ECO design process involves IC designers making changes at the register transfer level and verifying that the updated code matches the new specifications. Initially, the old net-list is scanned to identify potential areas for modification. Once these areas are identified, the net-list is revised, and the functional equivalence between the latest netlist and register transfer level is checked. ECO is typically used for major fixes originating from RTL, and such fixes can be time-consuming if the designer has to manually correct the bug by adding new logic. [8]

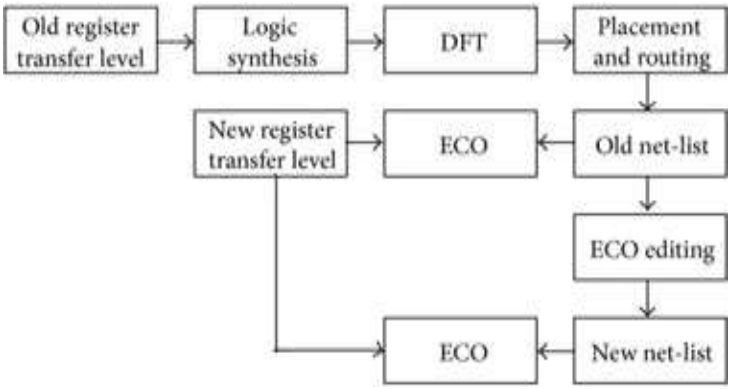

Fig. 2.2 Typical ECO Design Flow

Two Phase ECO Design Flow

In a two-phase ECO implementation methodology, the modified logic behavior is first analyzed to determine the required functional corrections within the existing design database [18] [24]. A list of available spare cells is then utilized to map the updated logic into appropriate physical locations without disturbing major portions of the validated layout.

After completion of logic mapping and patch insertion, verification procedures such as functional equivalence analysis and timing validation are performed to confirm that the revised implementation satisfies updated design specifications [6] [10].

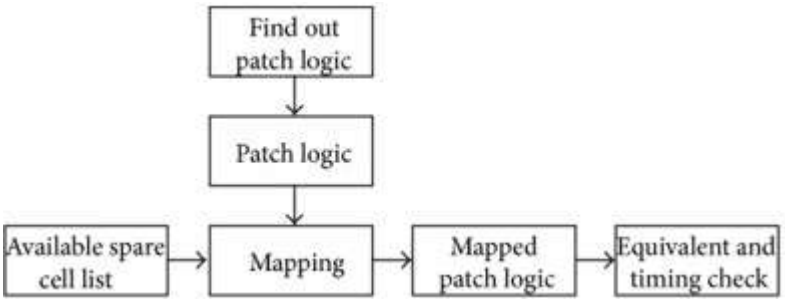

Fig. 2.3: Two-phase ECO design flow

Reliable metal-only ECO implementation depends on efficient utilization of spare-cell resources distributed across different regions of the physical layout [17] [24]. Proper distribution of spare cells improves flexibility for implementing localized functional modifications during later design stages.

Additionally, the incremental routing updates must be supported by ECO routing techniques along with minimizing the disturbance in the existing signal path and preservation of the previously optimized interconnect structures [18]. Efficient management of ECO modification data further simplifies implementation complexity and improves convergence during post-layout verification stages [25].

A powerful ECO synthesizer: This tool must utilize the physical information of spare cells, such as their location and type, to guide the technology remapping effectively. Due to limited spare cell resources, especially in later ECO runs, there may be a shortage of cells. Additionally, selected spare cells might not be at their ideal locations, leading to timing issues and routing congestion. [8]

An all-layer ECO is typically carried out before mask generation. There are no restrictions on the layout changes allowed during this process. A robust ECO flow must be in place as the design approaches tape-out. ECOs can be performed at any stage in the design flow, including post-placement, post-CTS, and post-routing. [8]

ECOs are used for following purpose:

Fix timing violations – Certain constraints might be overlooked, and an ECO can add inverter and buffer depending on the behavior of the design. [8]

Bugs - They often appear in the final stages. As the tape-out deadline approaches, simulations may reveal bugs that were previously unnoticed. If an ECO can fix these bugs without requiring a full redesign, engineers prefer it, especially when the complexity and runtime of the design are high, making it beneficial to preserve existing results and databases.

Adding functionality – While post-signoff ECOs are less common for major new features, smaller addons can be done rather than redoing the entire design. [8]

2.3 ECO scripts for ICC

ECO modifications in ICC can be implemented either through direct database editing commands or by applying changes using an updated ECO netlist description [7] [8]. Since these modifications alter the existing physical design database, backup copies of the original implementation data are generally preserved before executing ECO operations.

Metal-layer ECO implementation commonly involves incremental placement adjustments, buffer insertion, routing updates, and localized connectivity modifications within the existing layout environment [7].

CHAPTER 3

LIMITATIONS ON CURRENT ECO TOOL AND PROCESS

Before the manufacturing process begins, a semiconductor chip goes through multiple implementation steps such as synthesis, placement, clock-tree optimization, and routing. Each of these steps takes time, which is why it usually takes between nine months to one year to complete the development of a standard-sized chip before it can be sent for fabrication. All Companies in the semiconductor industry target to reducing their cycle time to get ahead of their competitors because of the fierce competition.[8]

As per the design functionality and physical layout limitations logic cels might get inserted, modified or removed during the ECO implementation stages. For these newly added logic elements the connectivity must be updated meticulously to ensure routing consistency and appropriate circuit behavior.

In general, these modified instances are automatically positioned inside the available layout region during the ECO placement procedure, along with incremental routing methodologies the impacted signal paths are pinpointed and only the required interconnect structures get updated [7] [8].

3.1 Existing ECO Cycle and Limitations

As stated earlier in previous chapters, ECOs can be at different stages of Physical verification, if the ECO is to be implemented at final stages, the db will be with below stage and conditions [8]
Db is done with DFM flow (Dummy base fill and Metal fill) [5]
Db is clean from DRC, LVS and Density
And Db is ready for tape-out.

Considering there is a major RTL bug fixes with minor/major changes, the db must go through following steps as highlighted in figure 3.1

(i) Dummy fills must be removed from tape-out ready db

(ii) ECO will be implemented on this db

(iii) Run DFM flow to insert dummy fills for both base and Metal layers [5]

(iv) Complete verification process (DRC, DEN, LVS)

(v) Provide the db for designer to check if the logic is implemented and no new timing issues seen [10]

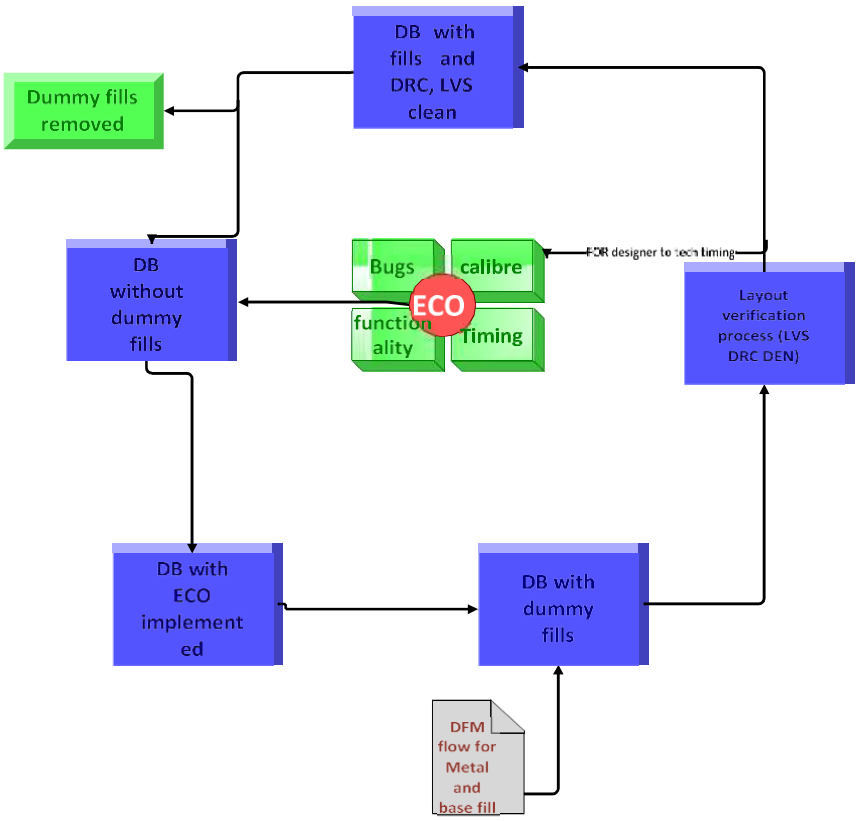

Fig. 3.1 One complete ECO cycle

Hence to complete the above stages the below listed issues seen

(i) Run time for DFM flow to add fills over ECO done design is huge. [5]

(ii) And the most significant of an ECO fill flow is the timing impact by completely new fill added into the design [8]

In case of post-DFM stages, ECO implementation will lead to more time to converge, due to following issues [5]

(i) Dummy base cells to be removed to implement ECO (adding logic cells) [8]

(ii) Dummy Metal fills must be removed since the logic cells added have pins which short will these fills.

(iii) Redo DFM flow for both base and metal fills post ECO fixes, which has huge run time and increased timing violations. [5]

Hence re-running all the steps from the process cycle for every bug becomes very costly both monetary and time wise.

CHAPTER 4

PROPOSED SOLUTION

This dissertation proposes a new method for ECO flow cycle and a tool development to reduce the runtime and impact on timing violations in ECO process [8]

4.1 Smart ECO Tool

The Smart ECO fill methodology utilizes localized fill analysis techniques to identify layout regions affected by ECO-related routing modifications [4] [20]. Instead of regenerating fill structures across the complete chip database, the methodology selectively updates only those regions influenced by design changes while preserving previously validated fill geometries in unaffected areas.

By limiting refill operations to ECO-sensitive regions, the proposed approach reduces runtime overhead and minimizes timing disturbances introduced during post-layout modification stages [8] [10]. This selective refill strategy also improves timing convergence efficiency and supports faster tape-out schedules in advanced deep sub-micron implementations [5] [20].

The methodology is particularly effective when ECO modifications impact only a small portion of the overall layout, since localized refill processing significantly reduces verification complexity compared to conventional full-chip DFM refill approaches [4].

4.2 Proposed ECO Fill Flow

When relatively minor changes are made to the design via ECOs, design teams would always prefer not to refill the entire design database from scratch, but instead, to make changes to the fill database only in those regions where the design changes occurred. Hence the concept is explained from the below figure 4.1, to start with the process the Db which need to go through ECO process is removed with dummy fills which were placed using DFM flow, Once the Db is without dummy fills, the ECO is implemented on the Db by the designer or layout owner, when the ECO implementation is completed, the dummy fills removed will be stored in a container and will be overlaid back on Db with ECO done. This process of retaining fills will give a greater advantage as discussed before with timing, run time etc. [5]

Proceeding with fills over Db, the nets which are edited during ECO flow will be provided by Designer and same nets are used to check if any dummy fills are shorting

with these nets, and these shorting fills will be removed from the design, this process will be carried with separate flow called Fill Short Finder, Hence the Db will have an empty areas where the fills are removed, and these empty areas must be filled with dummy fills. [8]

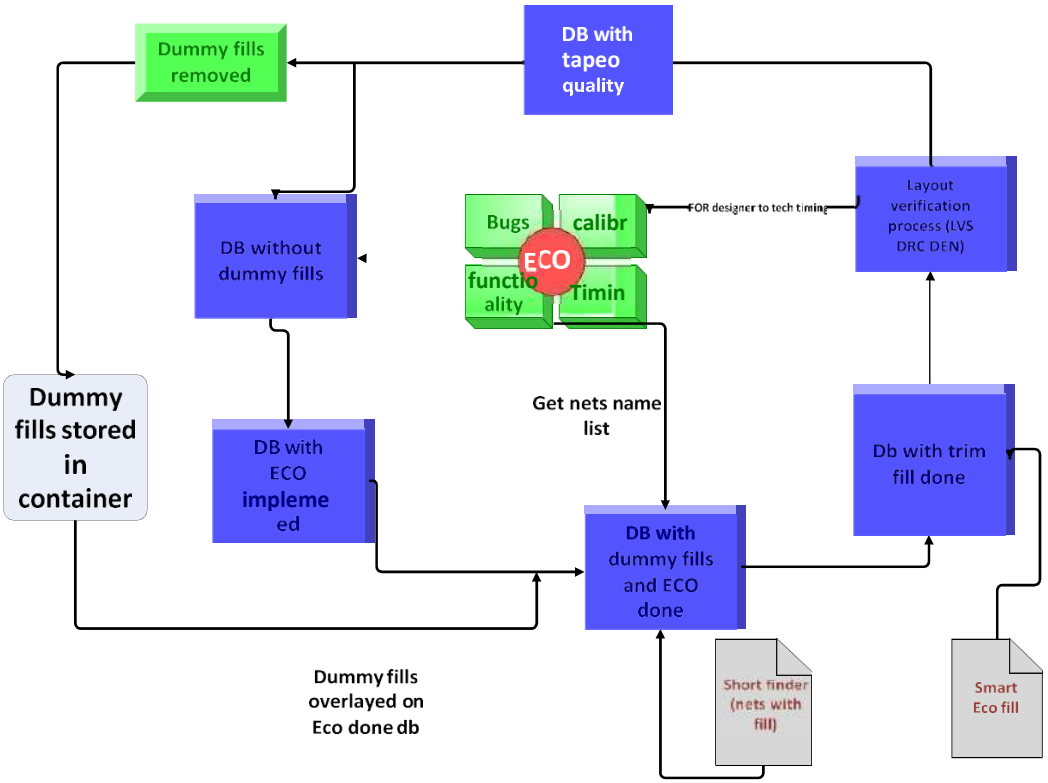

Fig. 4.1 Smart ECO fill process

Smart Eco fill flow helps us in filling these bounding areas where the fills are removed and does a smart way of filling in these areas considering all the DRC rules making sure there are minimal errors seen once the fill is done. And the fill done db is taken through the LV process and provided back to the designer for other timing checks. [8]

Hence, Smart Eco fill flow overcomes from filling the entire chip from scratch which incurs the penalty of long runtimes, while making changes to the fill only in the regions surrounding the ECO changes, minimizes the impact on timing. [8]

The Smart Eco fill approach saves the time penalty of a full fill run, reduces the file size penalty of flattening the fill database, and minimizes the timing impact. [8]

An example of a good candidate for an ECO fill run might be an ECO involving changes in some gate functionality or drive strengths, and a localized rerouting of those changes in a limited area. Multiple small areas like this are well-handled by a Smart ECO fill process. [8]

Smart ECO fill technology can solve both of those problems simultaneously, by [8]

(i) Getting the fills retained back into the Db and to remove those existing fill shapes that conflict with the new ECO design shapes, [8]

(ii) Refilling only in the areas where ECO changes occurred, either due to design metal removed by the user, or fill shape removal during the ECO fill flow, rather than refilling the entire chip. [8]

4.3 Timing Impact

One of the major advantages of the Smart ECO fill methodology is the reduction of timing disturbances caused during post-ECO refill operations [8] [10]. By restricting fill modifications only to localized routing regions affected by ECO implementation, the methodology minimizes parasitic variation and avoids unnecessary changes across stable portions of the layout database.

Since most of the previously verified fill structures remain preserved, post-ECO timing convergence becomes more efficient and requires fewer verification and optimization iterations [13]. In addition, maintaining controlled spacing between critical signal nets and regenerated fill structures helps improve routing reliability and timing consistency during late-stage physical design closure [4] [20].

4.4 Summary

A smart ECO fill approach effectively reduces run time and minimizes timing impact, all of which are critical factors to design teams, especially since fill comes at the end of the design flow, [20] when the tape-out pressure is the highest. Smart ECO fill flows provide forward-thinking design teams with another option to help them control and manage their tape-out schedule when designing at advanced nodes. [8]

CHAPTER 5

IMPLEMENTATION ON PROPOSED APPROACH

Before to start on proposed new ECO flow implementation, let's see about few tools used which are essential for the proposed approach. [8]

5.1 Fill_Short_finder

The Fill Short Finder module is designed to detect dummy fill geometries that overlap with routing paths modified during ECO implementation [3] [14]. The developed TCL-based flow analyzes edited signal nets individually across different metal layers and generates temporary geometric representations for identifying intersecting fill regions.

Fill structures creating overlap or short conditions with ECO-modified nets are selectively identified and removed, while unaffected density regions remain preserved within the layout database [11]. The localized processing methodology helps reduce unnecessary design modifications and improves runtime efficiency during post-ECO verification stages [8].

Fill short finder is a TCL based tool and the algorithm consists of following steps to be processed to find fill shorts with ECO implemented nets. [8]

(i) Get the list of nets edited during ECO implementation. [8]

(ii) Read each shape from the list of nets and build a container and array of each layer metal shapes

(iii) Get all intersecting vias and create a virtual-shapes, append into the array.

(iv) Check for dummy fill shapes intersecting each net shape and virtual shapes. [11]

(v) Resulting dummy fill shapes are loaded into a single container and processed as per the requirement. [11]

The below Figure 5.1 details the fill short finder with a flow chart diagram,

The code starts with reading the list of nets that are edited during ECO implementation, this list can be an input from Designer or Physical layout owner, these list of nets are processed to get each net shape of a different metal layers and stored in a variable X, and the same nets are processed in parallel to get the list of vias, these vias dimensions

are used to create a virtual shape and same are restored in the variable X, hence the X variable has both individual net shapes and virtual shapes created. The shapes with respect to its individual metal layer are processed to get its respective bounding boxes and are stored in the form of an array which helps for easy processing. [8]

Let us consider the with the list of nets N = {net1 net2 net3 net4 net5}
Layers to be processed is for metal3 and metal4
Signal net – net1 has four metal3 and two metal4 shapes.
Therefore, the resulting metal shapes are stored in array format AXB
Hence, X (metal3 {x11, y11 x21, y21}) # bbox of shape1 correspond to net1 (metal3 {x11, y11 x21, y21}) # bbox of shape1 correspond to net2 (metal3 {x11, y11 x21, y21})
(metal4 {x11, y11 x21, y21}) # and so on…

Once this array of X is created, this array is used to get the intersecting dummy fills, the list of resulting dummy fills are stored in variable Z and can be removed from the design for further processing. [11]

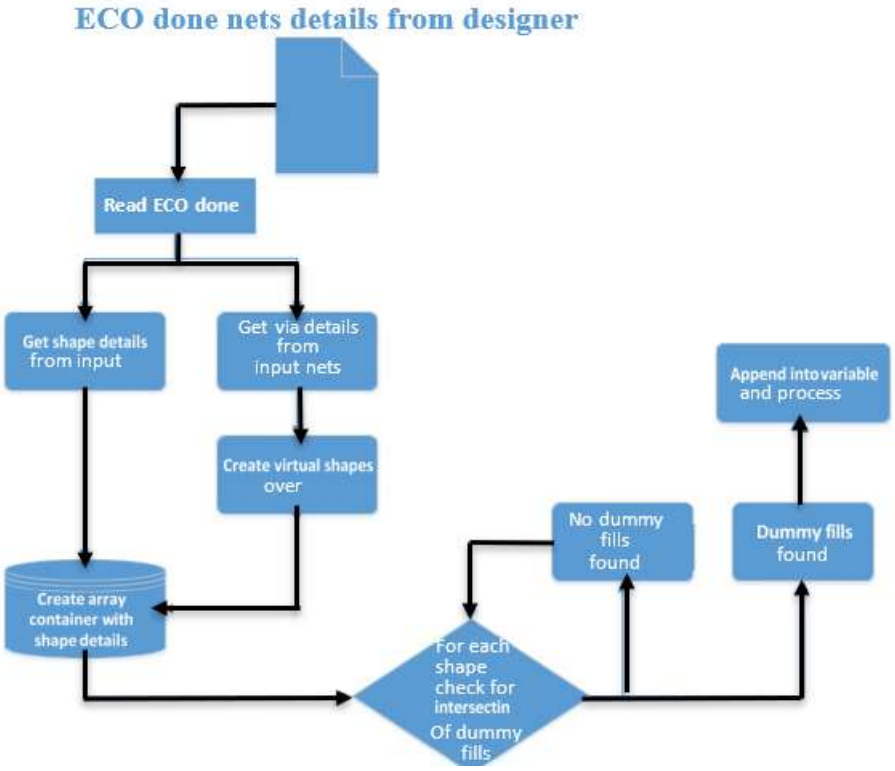

Fig. 5.1 Fill_Short_Finder tool flow

To develop this tool, TCL scripting language has been used, which is a powerful language to work on an IC compiler which helps us to handle, process, manipulate the

metal shapes in the design.
Figure 5.2 shows the representation of nets shorting with fills and how nets are processed to remove dummy fills from the design. [11]

In Figure 5.2a the NETX, NETY and NETZ are the nets which are edited during ECO implementation, once the retained fill container is overlapped on ECO done db, the dummy fills retained from the container are seemed to be shorted with these three nets, [8]
Hence as discussed from previous Figure 5.1, the nets edited are processed and intersecting fills are listed and removed from the design as shown in Figure 5.2b,
Once the Fill trim process is done using "Fill_Short_Finder" flow, the database can be processed for further stages.

Fig. 5.2 Dummy fills and signal nets
(a) signal nets overlapping on dummy fills.
(b) Intersecting dummy fills are removed leaving only signal nets. [11]

From previous section we studied on the tool developed to remove the intersecting dummy fills over signal nets edited during ECO implementation, in this section let us understand about an important tool "smart ECO fill" which is essential to implement the new ECO flow methodology, [8]
Smart ECO fill tool uses multiple files to get the details of metal dimensions and also write into different file format to complete the filling of dummy shapes in the design, hence before we start on the tool let us understand few of these important file formats [8]

5.2 Physical Design Technology Parameters

The technology file contains process specific parameters such as layer thicknesses and the sheet resistance of the various layers. These technology files describe a generic CMOS process.
For better understanding let's take an example of the generic CMOS process. Below is the technology file used in a similar CMOS process. In figure 5.3 the cross-section for various substrate layers is illustrated. This technology file is divided further into sub-sections. The <chip> statement is at the start of the first sub-section. Then comes the chips x and y dimensions in the first two lines. For optimal results the area should be approximately four times the size of the layout. For example, in a 400x400 sized chip a spiral inductor of 200x200 dimension would give the best results.

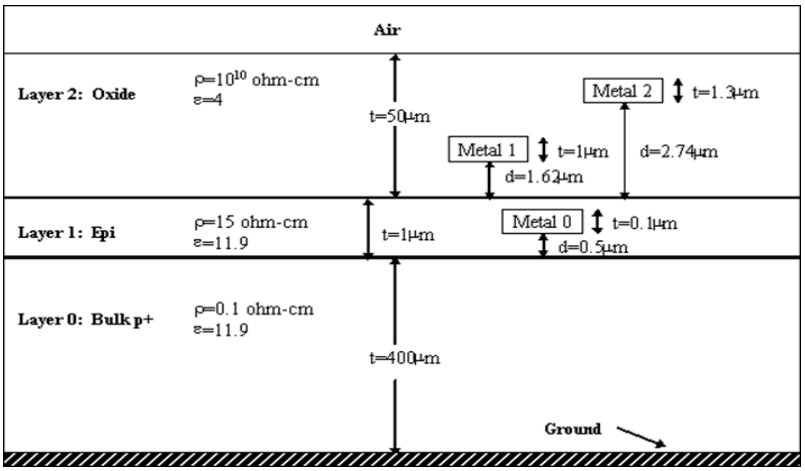

Fig. 5.3: CMOS cross-section view

Next, various dielectric and substrate layers are defined in the <layer> statements. A conducting substrate layer is specified by stating its resistivity in ohm-cm. A dielectric layer can be modeled as an equivalent resistivity according to the dielectric loss tangent. The thickness is specified in microns. The relative permittivity is unitless. Notice that the substrate layers are defined from bottom up. In other words, the order is important. Thus, the bulk layer is listed first, followed by the epi, and finally followed by the oxide, metal, via layer. The below Figure 5.4 shows the sample technology file format.

<chip>
chipx = 512; dimensions of the chip in x direction in microns
chipy = 512; dimensions of the chip in y direction in microns
TechFile = sample.tek; the name of this file
TechPath = /home/unknown/tekf;
the pathname of the data files freq = 0.1
eddy = 0; Layer 0 defined below is conductive
eddy = 1; Layer 1 defined below is also conductive;

Layer 2 is not conductive (oxide)
<layer> 0; Bulk Substrate
rho = 0.1; Resistivity: ohm-cm
t = 400; Thickness: microns
eps = 11.9; Permitivity: relative
<layer> 1; Epi Layer
<same as bulk substrate format>
<layer> 2; Oxide Layer
<same as bulk substrate format>
<metal>; Substrate Contact Layer = 1; Epi Layer
rsh = 30; Sheet Resistance Milli-Ohms/Square
t = 0.1; Metal Thickness (microns)
d = 0.5; Distance from bottom of layer (microns)
name = msub; name used in ASITIC
color = yellow; color in ASITIC
<via> 0; metal 1 to substrate
top = 1; via connects up to this metal layer
bottom = 0; via connects down to this metal layer
r = 5; resistance per via
width = 0.4; width of via
space = 1.3; minimum spacing between vias
overplot1 = 0.3; minimum distance to substrate metal
overplot2 = 0.3; minimum distance to metal 1
name = via0; name in ASITIC
color = purple; color in ASITIC
<metal> 1; metal layer 1
layer = 2
rsh = 50
t = 1
d = 1.62
name = m1 color = red
<via> 1; metal 1 to metal 2
top = 2
bottom = 1
r = 4
width = .5
space = 1.5
overplot1 = 0.4; to substrate metal
overplot2 = 0.4; to metal 1
name = via1
color = white

Fig. 5.4 Technology File format

5.3 DEF

The Design Exchange Format (DEF) file is primarily used to represent the physical implementation details of an integrated circuit layout. It stores information related to chip dimensions, component placement, routing data, and layout constraints required during the back-end design process.

A DEF file generally includes:

- Overall die area information
- Interconnection details between modules
- Placement locations of standard cells and macros
- Floorplanning data such as rows and regions
- Routing and placement blockage definitions
- Placement-related constraints
- Power domain specifications

The beginning section of the DEF file contains statements that define the syntax and parsing rules used for interpreting the file contents.

==========

```
01. VERSION 5.7 ;
02. DIVIDERCHAR "/" ;
03. BUSBITCHARS "[]" ;
04. DESIGN c17 ;
05. UNITS DISTANCE MICRONS 1000 ; 06. DIEAREA ( 0 0 ) ( 8000 8000 );
99. END DESIGN
```

==========

Line 01 indicates the DEF version used in the design file.

Line 02 defines the hierarchy separator symbol used for module representation.

Line 03 represents the notation used for bus signals and grouped connections.

Line 04 identifies the name of the circuit design.

Line 05 defines the relationship between DEF database units and physical dimensions in microns.

Using the coordinate values the overall chip layout boundary is specified as per DIEAREA statement.

Lastly, the DEF description ends with the END DESIGN statement.

5.4 Smart ECO Fill

The Smart ECO Fill Methodology is shown in the Figure 5.5. By reading the user-defined bounding box regions where ECO modifications are applied the user-defined bounding box regions this process is initiated. Details about the metal geometries within those regions is extracted into a stream file.

Track-related details are also extracted simultaneously from the technology file (.tf).

Through logical comparison the vacant routing tracks are identified after processing both datasets together with the tool. The metal fill structures can be generated to maximize the use of these empty bounding box regions yield from this process. Due to the expensive computation of directly creating large fill geometries, to do fill generation efficiently a DEF-based method is used.

To restore the missing metal fills in these ECO-modified regions, the DEF file generated is imported back into the design database later. Using Intel standard rule-check files, also known as runsets, the design rule check is verified during this procedure.

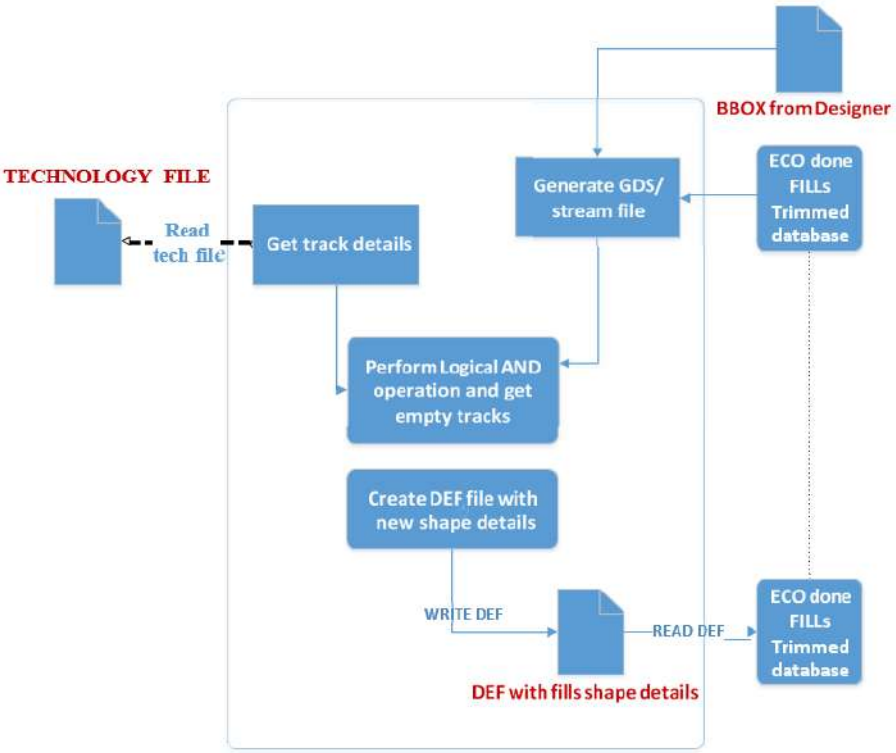

Fig. 5.5: Smart ECO tool flow

A sample tape-out layout database is shown in Figure 5.6 where after the ECO process the Metal 4 fill structures are removed from shorted nets. The highlighted red regions

represent the locations where ECO modifications were carried out. These regions are provided to the smart fill tool in the form of bounding box coordinates represented as {x1 y1}{x2 y2}. The tool uses these coordinate boundaries to identify the affected regions and regenerate the required metal fill structures.

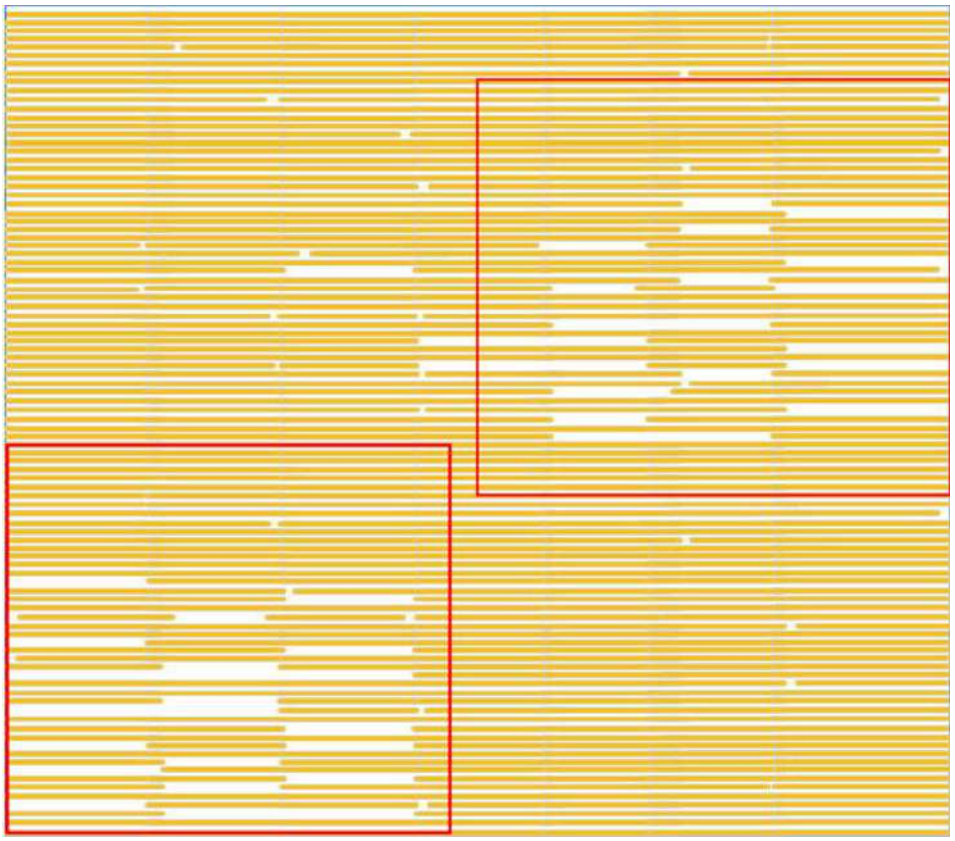

Fig. 5.6: ECO implemented area with dummy fills removed shorting signal net

After receiving the designer-defined bounding box regions, the smart ECO tool executes several processing stages discussed earlier, including technology file extraction, stream file generation, logical comparison operations, and DEF file creation and loading.

Based on these operations, the affected ECO regions are automatically populated with dummy metal fills while ensuring that all required design rule checks (DRCs) are satisfied, as illustrated in Figure 5.7.

Fig. 5.7: ECO implemented design with smart ECO fill done

After execution of the Smart ECO Fill flow on the ECO-modified database, only a small number of DRC violations generally remain, which can be resolved manually by the layout engineer. Once these remaining issues are corrected, the design becomes ready for timing verification and final validation.

Since the flow updates only the ECO-affected regions for dummy fill removal and regeneration, both processing runtime and timing impact are significantly minimized.

CHAPTER 6

TEST RESULTS AND DISCUSSION

Following chapter, outputs from the various flow methodology and tools developed in chapter 4 are recorded at different stages and analyzed to see if and how the proposed new ECO flow methodology gives improved results [8]
The following topics details on different steps followed in new proposed ECO flow methodology and the real test case results [8]

6.1 Tape-out Database

As discussed over previous chapters, considering due to some bug fixes, silicon feedback, timing fixes, multiple ECOs are received and to be implemented over the tape-out ready database. [8]
Figure 6.1 shows the real case database which is clean from LVS, DRC with dummy fill done for DFM and ready for tape-out. The database receives an ECO to add a few buffers and to improve the net (to route in a higher metal layer, above M3). [5]

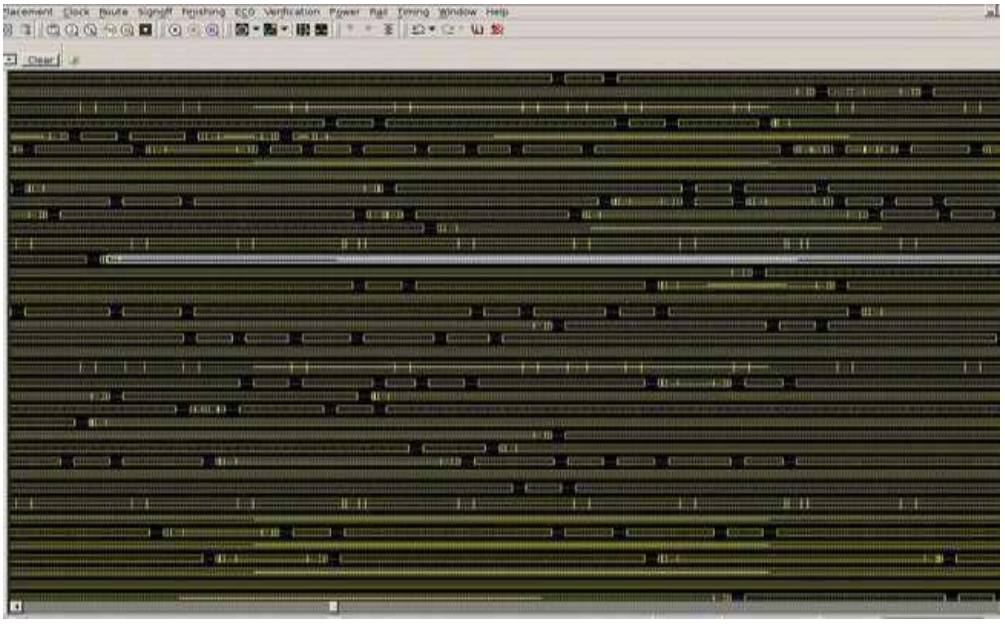

Fig. 6.1: ECO implemented design with smart ECO fill done [8]

6.2 Dummy fill separation

Figure 6.2 shows the design where the dummy fills are separated from the database, hence only the signal/power/clock nets are present in the design, Figure 6.3 shows the container that has only dummy fills which are separated from the design and these fills are preserved which will be overlayed in later stages once the ECO is implemented on the design. [8]

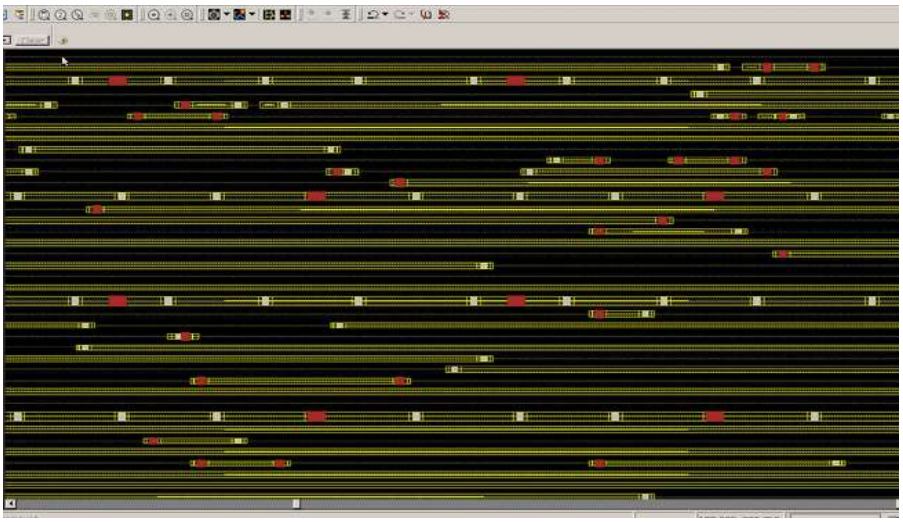

Fig. 6.2: Tape-out database without dummy fills

Hence the design with no dummy fills is been taken over by layout owner to implement the given ECO, during ECO implementation multiple nets will be edited and cells will be added and moved depending on the area congestion. [8]

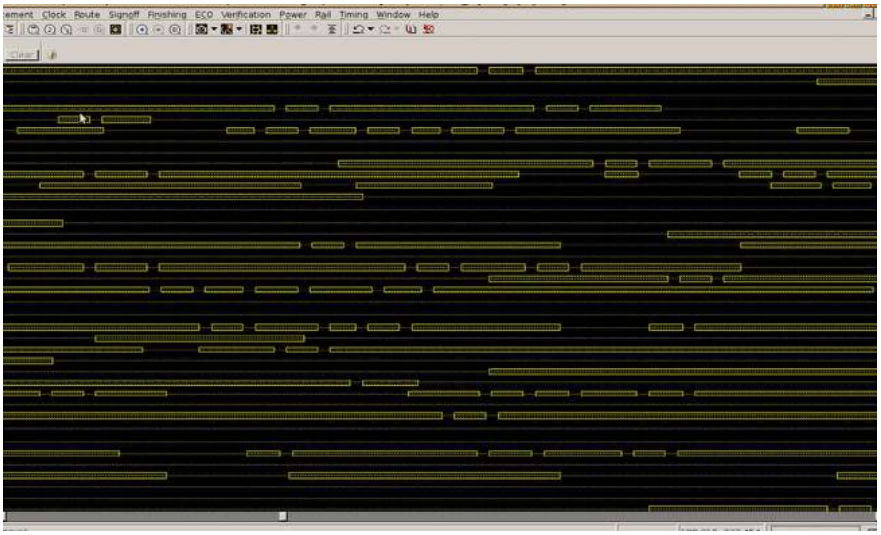

Fig. 6.3: Dummy fill container (contains removed dummy fills from the design) [11]

6.3 ECO Implementation

As discussed in earlier chapters, ECOs from the designer can be for various reasons, these could be, Pre silicon feedback, post silicon feedback, bug fixes, timing fixes, Metal only fixes, etc. [8]
Below Figure 6.4 shows a few sample ECO commands that are used to test new ECO flow methodology and smart ECO flow tools. [8]

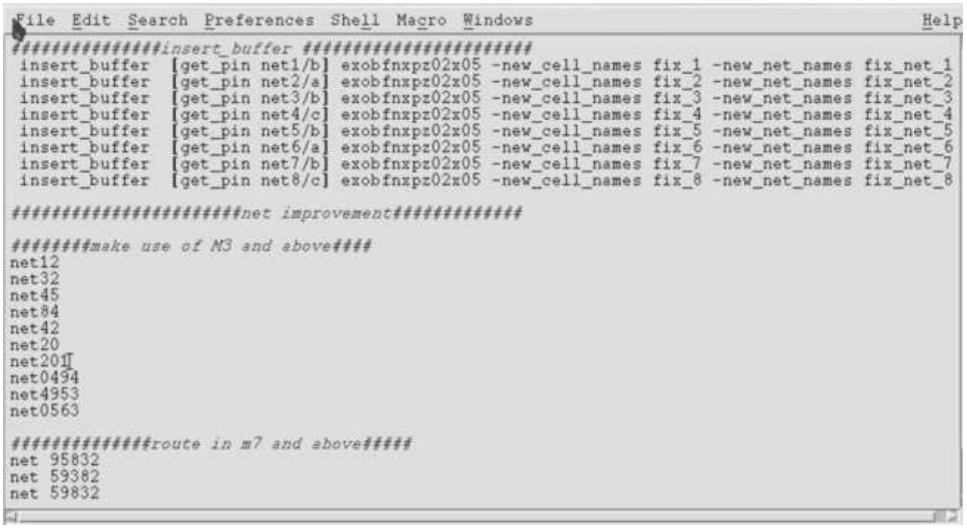

Fig. 6.4: Sample ECO commands

Post ECO implementation, listed nets from Figure 6.4 are edited and modified, resulting change in the track usage for these particular net shapes, which will be causing multiple net movement due to metal area congestion, Figure 6.5 shows the entire path of three sample nets (colored in green, orange, pink) which were modified as a part of ECO implementation for net improvements [8]

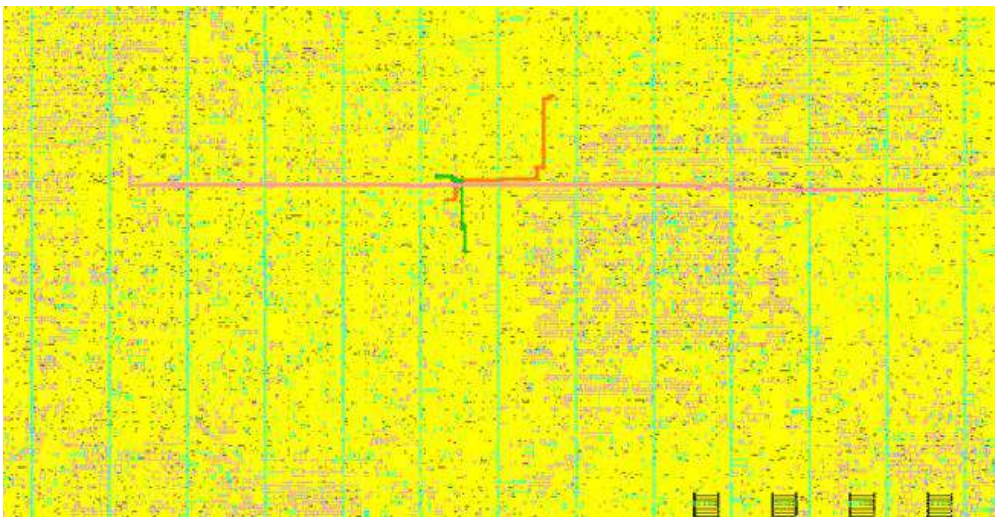
Fig. 6.5: ECO implemented database, edited nets highlighted [8]

Once the ECO is implemented, the dummy fills container is retained back over ECO implemented database, Figure 6.6 represents the view of metal fills overlayed back on the database post ECO, as we seen in the below Figure, fills retained and overlaid over the database are shorting with metal nets which were edited during ECO. [8]

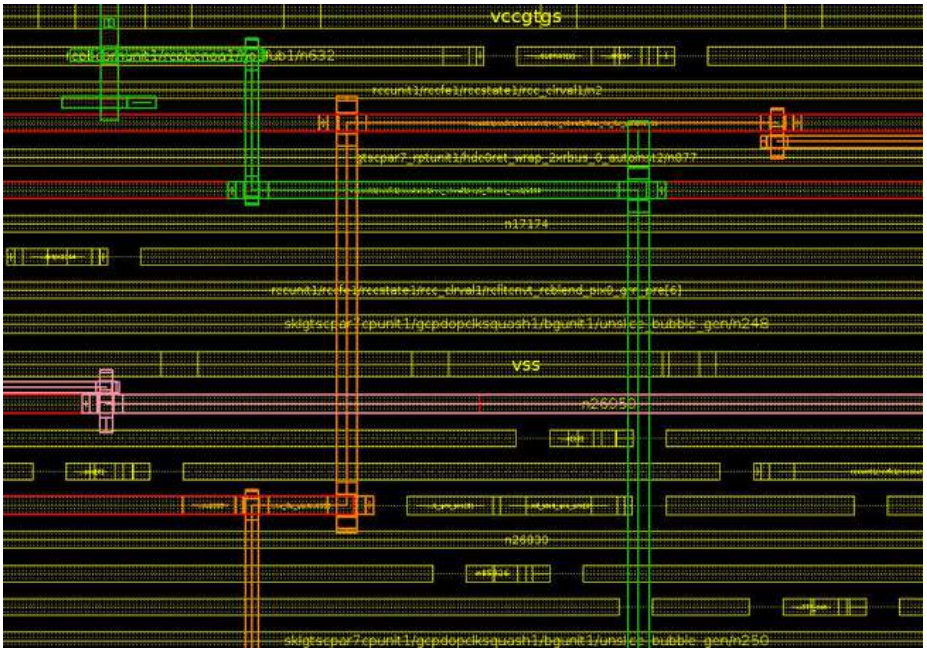

Fig. 6.6: Dummy fills overlapping on signal nets

6.4 Fill Short finder Results

Post retaining the dummy fills from fill container, and overlayed on ECO database, we see huge shorts due to edited nets shorting with fills and these fills in turn shorting with other nets as shown in Figure 6.7 [8]

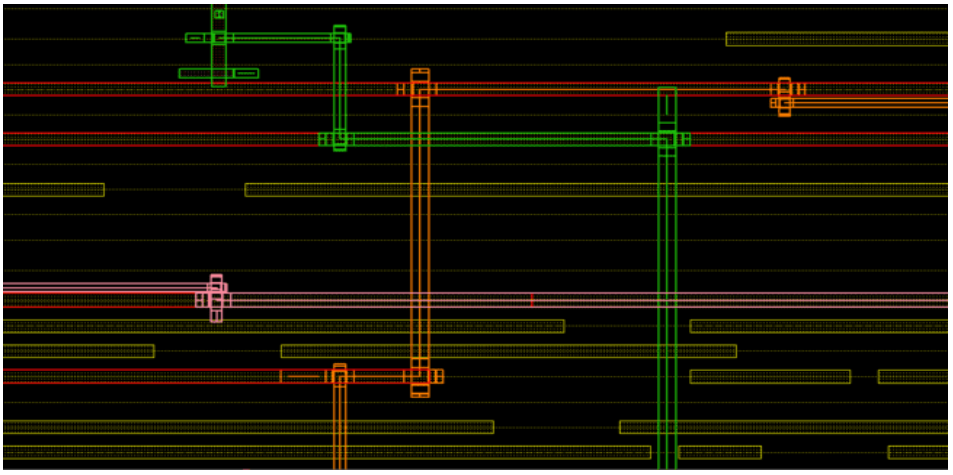

Fig. 6.7: Dummy fills view shorting over signal nets edited [11]

Hence, we make use of tool called Fill short finder, the tcl based Fill short finder read net details from layout owner input file, check for all intersecting dummy fill shapes and removed from the design, leaving empty area around these edited nets and making sure no shorts seen due to these overlapping dummy fills on these nets. Figure 6.8 shows the snapshot from the database post dummy fills removed which are overlapping ECO edited signal nets from the database, resulting in retaining all other dummy fills and removing only shorting dummy fills. With which result gives a great advantage in less timing impact. [8]

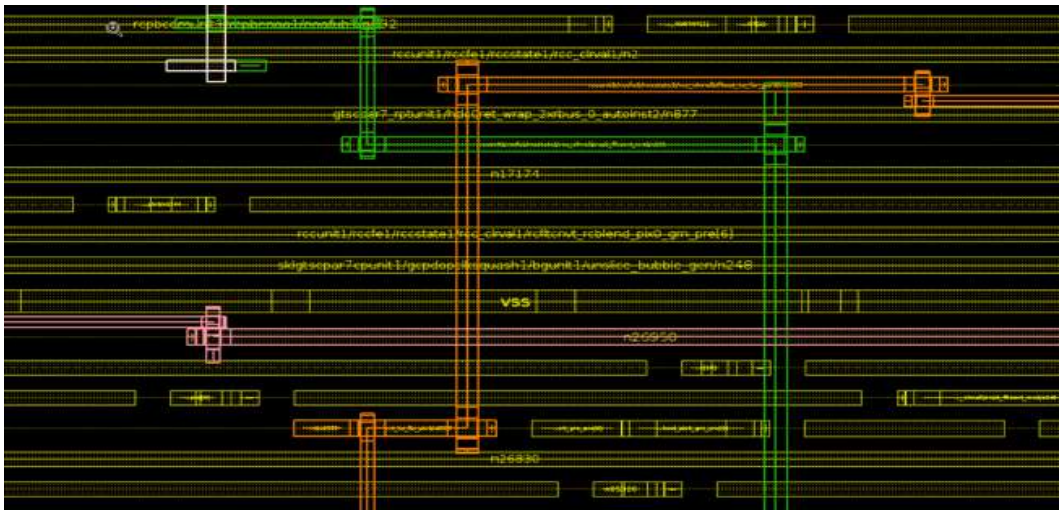

Fig. 6.8: Dummy fills shorting signal nets removed using fill short finder tool [11]

6.5 Smart ECO fill flow

With shorting dummy fills removed from the design, the database is carried through smart ECO fill flow, Smart ECO fill flow is a tcl based tool which does multiple operations to fill the empty spaces in the ECO done database. [8]

By reading designer provided bboxs, getting track details, reading shape details within provided bboxs and performing logical operations shown in Figure 6.8, the ECO implemented areas at three locations are filled with dummy fills using smart ECO fill flow. [8]

Figure 6.9 illustrates the three bounding box areas where the ECO implementation was carried out. At these three areas, the shorting dummy fills along with their associated signals were removed from the design. [8]

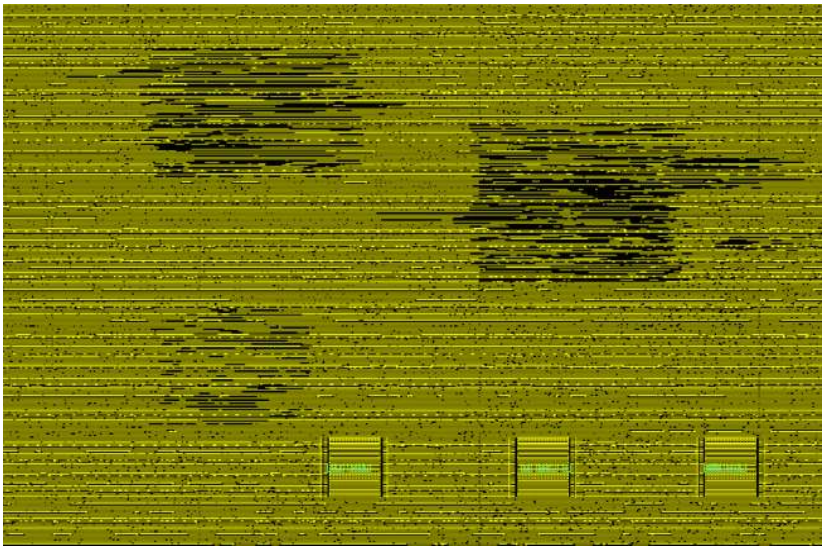

Fig. 6.9: ECO implemented areas with dummy fills removed [8]

Figure 6.10 shows Metal4 dummy fills created back at the missing locations using smart ECO fill flow. To create these Metal4 dummy fills, as discussed, a DEF file was generated. This method is a faster way to create metals at these locations compared to using the create_user_shapes ICC command for creating these dummy shapes, DEF creation method gives greater advantage in terms of runtime for shape creation in the database. [8]

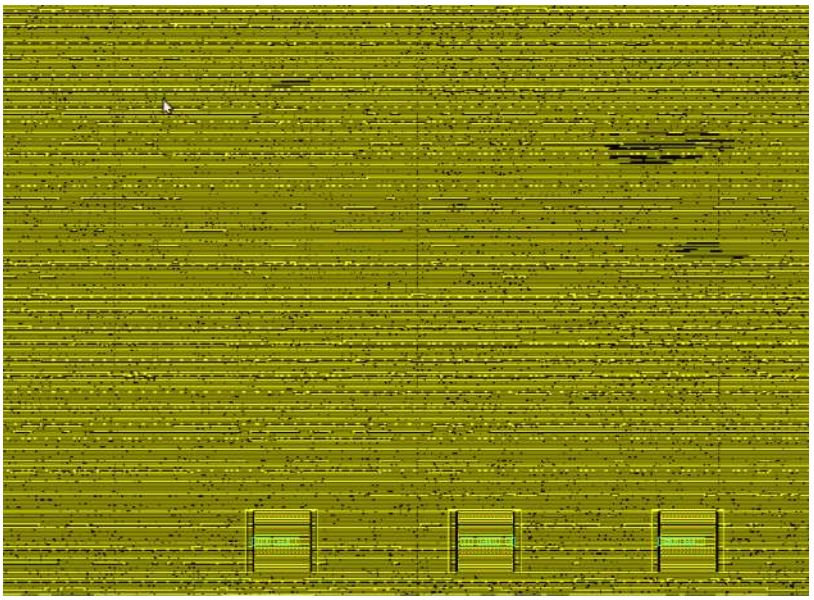

Fig. 6.10: Dummy fills created using smart ECO fill flow [8]

6.6 Drawback in Smart ECO fill flow approach

Smart ECO fill flow approach discussed in previous section gives greater advantage in filling the empty areas in the design, post ECO implementation and also greater impact by reducing timing errors and runtime. [8]

The approached ECO fill flow read the bounding box as an input from the designer and to fill the area with dummy fills, but few of the areas are not filled by dummy fills, this is due to designer input bounding box not covering the areas where the fills were removed which are shorting the signal nets using Fill Short finder. This results in more empty areas post ECO fill flow as shown in Figure 5.11 (red circled with missing dummy fills) and causing layout owners with more manual efforts to add these dummy fill shapes and fix all the DRC errors resulted. [8]

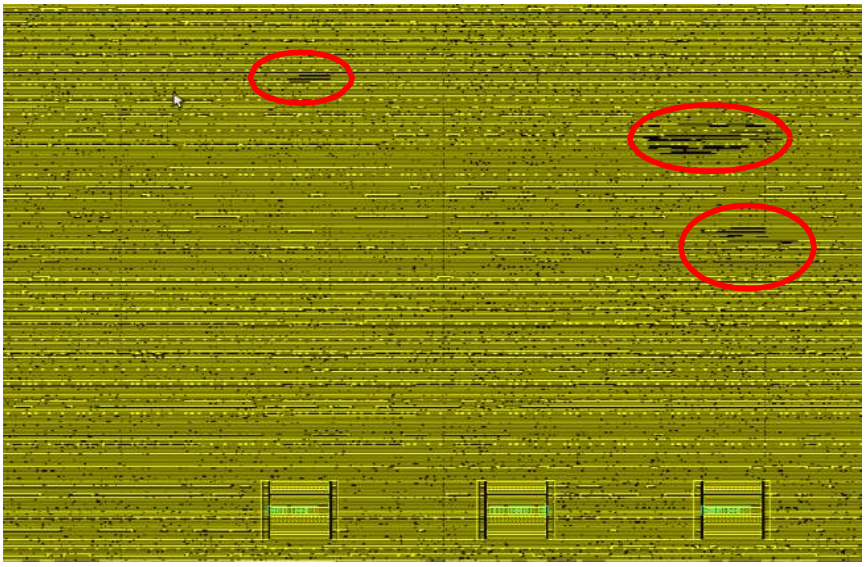

Fig. 6.11: Missing Dummy fills at ECO implemented areas [8]

6.7 New Approach for Smart ECO fill flow

To overcome the drawback of missing dummy fills, new approach was used in Smart ECO fill flow, and the new approach is, instead of generating stream file for the area based Metal4 shapes, generate stream file for entire design, and doing a logical AND operation with track details extracted from technology file, [8]

Hence with the above approach, we will be getting all the empty areas where dummy fills are missing and no area will be skipped since the missing details depend on the entire database stream file rather than the bounding box area stream file. [11]

And this new approach code was modified in existing Smart ECO tool flow and tested on the same test case database. [8]

Figure 6.12 shows the ECO done area with dummy fills were removed which are shorting edited signal nets. [8]

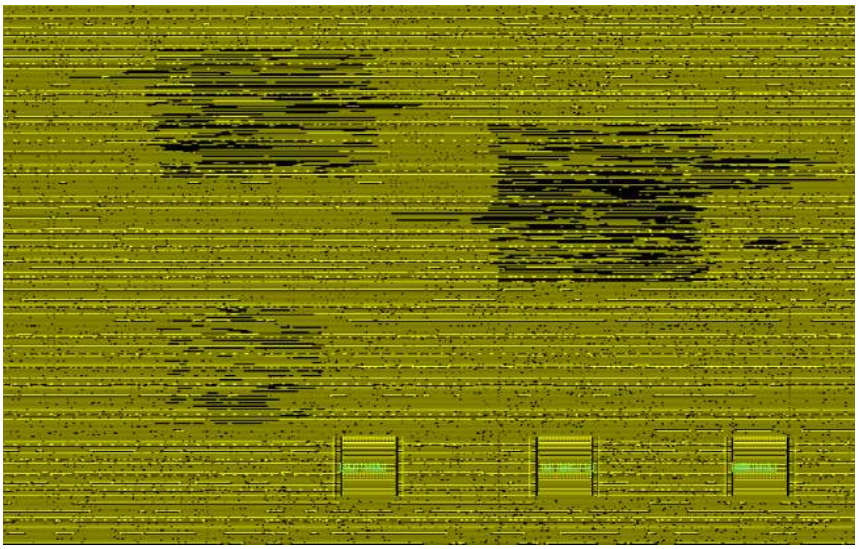

Fig. 6.12: ECO implemented areas with dummy fills removed, for new approach [8]

Figure 6.13 shows the usage of new ECO Fill flow on the fills removed design, resulting in proper filling of dummy fills in the entire design and not missing any areas without fills. [8]

Hence the entire new design flow methodology gave a greater reduction in ECO implementation runtime. And also reduced timing impact by retaining existing fills from the tape-out database. [8]

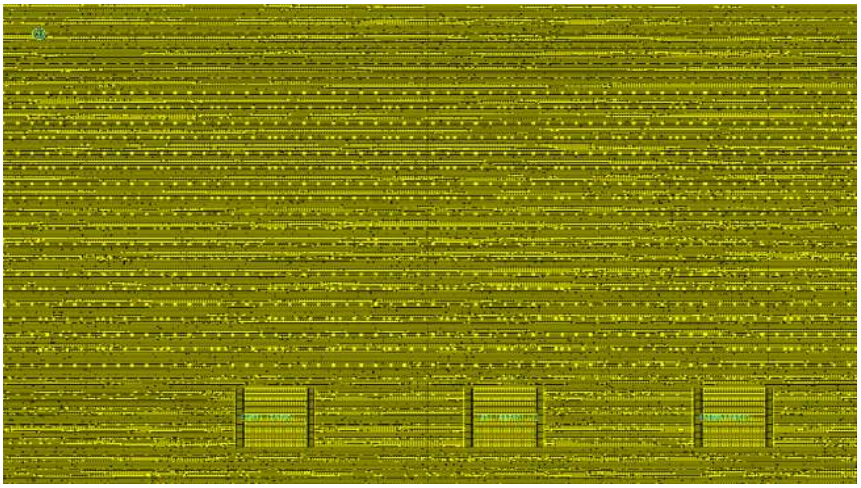

Fig. 6.13: Design with Dummy fills created with new Smart Fill flow [11]

Table 1 show the comparison of Existing ECO flow and proposed new ECO flow, [8]

Design area	Existing ECO flow			New ECO flow		
	DFM flow			Smart ECO flow		
	Metal2	Metal4	All metal layers	Metal2	Metal4	All metal layers
65738.2953	3 hr	2 hr 10min	10hr 55min	2 hr	1hr 35min	6hr 15min
97191.4854	3hr 15min	1hr 50min	12hr 20min	3hr 15min	1hr 50min	7hr
371400.1805	5 hr	4hr 40min	18hr 55min	5 hr	4hr 40min	9hr 35min
850032.1943	6 hr 15min	5hr 45min	26hr 30min	6 hr 15min	5hr 45min	12hr 10min

Table 1: Run time comparison of Existing and new approach ECO flow [8]

Hence one cycle time for ECO flow process from designer to layout owner for ECO implementation, and with DFM done and DRC clean post ECO implementation back to designer was 4 days with existing ECO flow, with new ECO flow approach we are able to complete within 2 days. Hence there is 50% of ECO cycle time reduction and timing fixes iteration. [5]

CHAPTER 7

CONCLUSION

The project was of great interest to the ECO flow methodology, as it saves the entire ECO cycle time by 50%. The new approach was carried out by identifying the problems and overhead in the ECO cycle stages and providing solutions with new tools was also to make the Designer and layout owner job simple and timing closure easier. [8]

The tools were developed so that they are in generic form and could be used independent of technology, and design. Contribution towards the project involved in developing the idea behind the project, and also developing the tools required and implementing new ECO flow for the idea. The new ECO flow and tools were tested extensively on many designs and enhancement features added to help the user. [8]

CHAPTER 8

FUTURE WORK

With new ECO flow methodology, ECO cycle time is greatly reduced, but during this ECO implementation, the buffers, net improvements are carried out manually by the Layout owner, hence new different tools can be developed which automates the cell placement, physical connectivity between two cells. The other approaches are, during minor ECO implementation, very few cells are inserted or very few nets are improved, in such cases layout owner must have an option to place these cells manually and also fill these cells with dummy fills for such small areas and get design rule check clean, hence still further ECO cycle time can be reduced. [8]

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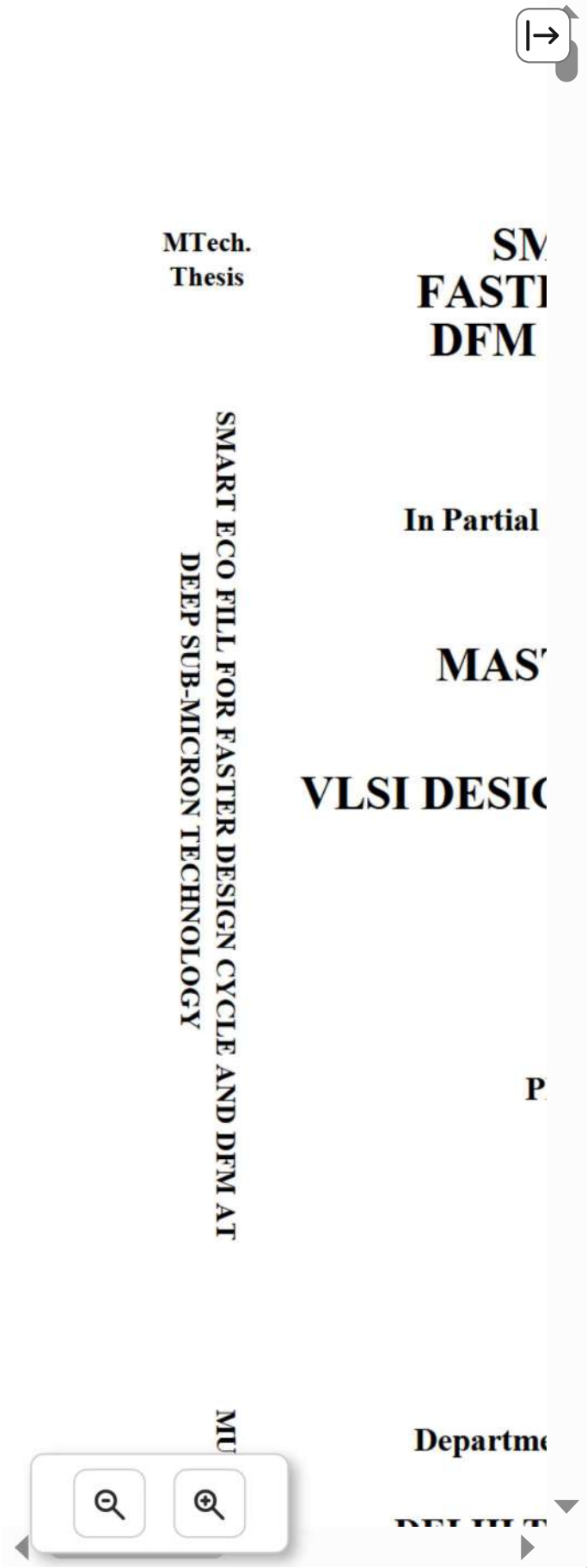

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MUSKAN SINGH
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Professional Summary:

Aspiring Physical Design Intern at STMicroelectronics with hands-on experience in RTL-to-GDSII flow on advanced technology nodes. Skilled in block and top-level implementation including floorplanning, placement, CTS, routing, and timing closure, ECO using Cadence Innovus. Strong understanding of STA, physical verification, and PPA optimization. Responsible for PNR (floorplan to signoff) and design closure, with hands-on expertise in Innovus, Calibre.

Projects:

Client Projects

PROJECT- 3 (**STMicroelectronics)** *July 2025- Present*

Responsibilities and Challenges:

- Working on full RTL-to-GDSII physical design flow on **12nm** technology node using Cadence Innovus.
- Performed floorplanning, placement, CTS, routing, and timing closure.
- Worked on congestion analysis and fixing strategies during placement and routing stages.
- Supported physical verification (DRC/LVS) to ensure design rule compliance.
- Contributed to PPA (Power, Performance, Area) optimization.
- Worked on ECO implementation and improving timing violations.
- Solved max transition, SI, Noise related issues.
- Collaborated with cross-functional teams for design convergence.

PROJECT- 2 (**Infosys Limited**) *Nov 2021 - July 2024*

Responsibilities and Challenges:

- Developed Power BI dashboards using DAX, KPIs, and drill-down analysis.
- Worked with Oracle SQL for data extraction, transformation, and validation.
- Handled complete lifecycle: requirement gathering → development → testing → support.
- Supported enterprise client (Daimler – Mercedes-Benz) for business insights.
- Enabled data-driven decision-making through visualization and reporting.

PROJECT- 1 (**DRDO: CFEES)** *May 2019 - July 2019*

Responsibilities and Challenges:

- Designed and implemented a data acquisition system for collecting real-time sensor data.
- Interfaced multiple sensors with Arduino Uno for data capture and processing.
- Established communication between two Arduino boards using ISI protocol.
- Developed embedded logic in C++ (Arduino IDE) for synchronized data transfer.
- Implemented automated system to collect, process, and transmit sensor data via email.
- Handled challenges related to data synchronization, communication reliability, and signal interfacing.
- Ensured efficient data flow between modules with minimal delay.

Certifications:

NPTEL – VLSI Physical Design:

- Certified in VLSI Physical Design through NPTEL, covering concepts of backend flow and physical implementation.
- https://drive.google.com/file/d/1SqfuJwAHoeXqhgWzOLxnMRBCTnva7Xhx/view?usp=sharing

NPTEL – RTL TO GDS FLOW:

- Certified in RTL to GDSII, NPTEL.
- https://drive.google.com/file/d/1LJi_4Cw-o7vn4xWOXIf2-PlK1VVUFJUI/view?usp=sharing

Education:

- Master of Technology [2024-2026] in VLSI Design and Embedded Systems from Delhi Technological University (DTU): 8.37 CGPA
- Bachelor of Technology [2017-2021] in Electronics and Communication Engineering from NSUT East Campus, Formerly AIACTR, Delhi: 8.56 CGPA
- Senior Secondary from Mayur Public School, Delhi: 87%
- High School from Mayur Public School, Delhi: 8.8 CGPA

Personal Details:

DOB: Jan 14,2000

Languages known: English, Hindi

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