Novel 13T SRAM Cell Design: Improved Noise Margin & Reduced Dynamic Power using 90nm GPDK

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CANDIDATE'S DECLARATION

I, Arun Kumar (24/VLS/12), student of M.Tech (VLSI and Embedded Systems), hereby declare that the Project Dissertation titled "Novel 13T SRAM Cell Design: Improved Noise Margin & Reduced Dynamic Power using 90nm Generic Process Design Kit (GPDK)", which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original work carried out by me and has not been copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma, Associateship, Fellowship, or other similar title or recognition.

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I hereby certify that the Project Dissertation titled "Novel 13T SRAM Cell Design: Improved Noise Margin & Reduced Dynamic Power using 90nm Generic Process Design Kit (GPDK)", submitted by Arun Kumar (24/VLS/12), Department of Electronics & Communication Engineering, Delhi Technological University, Delhi, in partial fulfillment of the requirement for the award of the Degree of Master of Technology, is a record of the project work carried out by the student under my guidance and supervision. To the best of my knowledge, this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Keywords — SRAM, 13T, Static Noise Margin, Dynamic Power, Read Delay, Write Delay, 90nm GPDK, Cadence Virtuoso, Schmitt Trigger, Leakage Current, FinFET.

Static Random Access Memory (SRAM) forms the majority structural component of on-chip area in modern System-on-Chip (SoC) designs, and the dual problem of managing power consumption while sustaining noise stability has become progressively more acute as process technology pushes deeper into the nanometer regime. At the 90nm node, The physical implications of device scaling, such as: (shorter gate lengths, thinner gate oxides, And lowered supply voltages significantly increase a number of leakage modes like sub threshold current (Isub), gate tunneling (Ig), GIDL, And drain-induced barrier lowering (DIBL). In this scenario, the use of conventional 6T cells is not sufficient to ensure both read stability and write-ability at the same time without performance trade-offs that are hard to Gate. Selecting the right sizer.

This dissertation describes the design and simulation of a new 13T SRAM cell at the 90nm Technology Node, held and validated by an customized and co-operative GPDK. (GPDK) inside Cadence Virtuoso for use in the proposed two-dimensional concurrent GPDK. the architecture is based. Three structural principles a completely decoupled read buffer threshold text that protects playback froma completely decoupled read buffer, preventing any disturbance to is used to turn off the storage nodes at the time of read access, a series-stacked control transistor(N9) beneath the drive of RWL whose body follows the running RWL to cut off the cell‘s leakage at the read. Path in hold mode, and a write path whose pull-up and pass-gate transistors are cooptimized for fast state transitions in the presence of optimized cell stability. Although the performance vector of the Schmitt Trigger 10T (ST10T) SRAM cell used as the reference for the entire work. A significiant improvement over the 6T baseline in noise margin by means of hysteresis Enhancement, but does exhibit deficiencies that provide the impetus for our current design.

Simulation result of typical-to-typical (TT) process corner, 27C, and nominal VDD Show their proposed 13T cell achieves a 83% dynamic power reduction (from 42.19 x 109 nW to 7.17 x 109 nW), a 61% improvement in read access time (TRA: 36 ps to 14 ps) a 19.6% improvement in the write access time (TWA: 92 ps to 74 ps) and A 155% improvement

in RsNM (Read Static Noise Margin: 111.61 mV to 285.254 m V) all at once, with no sacrifices on any metric. These achievements set the. The proposed 13 T cell is also a promising candidate for embedded memory in low-power VLSI and. Mixed-signal systems at the 90nm process node.

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LIST OF SYMBOLS, ABBREVIATIONS AND NOMENCLATURE

SRAM : Static Random Access Memory

6T : Six-Transistor (standard SRAM cell)

8T : Eight-Transistor SRAM cell

9T : Nine-Transistor SRAM cell

10T : Ten-Transistor SRAM cell

11T : Eleven-Transistor SRAM cell

12T : Twelve-Transistor SRAM cell

13T : Thirteen-Transistor (proposed SRAM cell)

ST10T : Schmitt Trigger 10-Transistor SRAM cell (reference)

LP10T : Low-Power 10-Transistor SRAM cell

SNM : Static Noise Margin

RSNM : Read Static Noise Margin

WSNM : Write Static Noise Margin

HSNM : Hold Static Noise Margin

GPDK : Generic Process Design Kit

PTM : Predictive Technology Model

CMOS : Complementary Metal-Oxide Semiconductor

FinFET : Fin Field-Effect Transistor

SoC : System-on-Chip

VTC : Voltage Transfer Characteristic

V_{DD} : Supply Voltage

V_t : Threshold Voltage

WL : Word Line

WLR : Write Word Line (Read Word Line in schematic label)

RWL : Read Word Line

BL : Bit Line

BLB : Bit Line Bar (complementary)

RBL : Read Bit Line

PU : Pull-Up transistor (PMOS)

PD : Pull-Down transistor (NMOS)

PG : Pass-Gate (access) transistor

N9 : Series-stacked control transistor (RWL-driven)

I_{sub} : Subthreshold leakage current

I_g : Gate leakage current

GIDL : Gate-Induced Drain Leakage

DIBL : Drain-Induced Barrier Lowering

T_{RA} : Read Access Time (read delay)

T_{WA} : Write Access Time (write delay)

P_{dyn} : Dynamic (switching) power consumption

TT : Typical-Typical process corner

SS : Slow-Slow process corner

FF : Fast-Fast process corner

PVT : Process-Voltage-Temperature variations

DRC : Design Rule Check

CHAPTER 1

INTRODUCTION

1.1 Overview

The relentless drive to scale CMOS technology has delivered extraordinary gains in transistor density and computational throughput over the past several decades, but this progress has not come without cost. As device geometries shrink toward and beyond the 90nm node, a set of physical and electrical constraints emerge that make memory design substantially more challenging than the scaling narrative alone would suggest. SRAM occupies the majority fraction of chip area in virtually every modern processor, mobile SoC, and embedded controller [1]. It also contributes substantially to total chip power — both through the dynamic switching consumed during read operation and write operations, and through the ever-growing leakage currents that flow through every cell in the array even when no access is taking place.

The relationship between the threshold voltage and the supply voltage at advanced nodes creates a particularly uncomfortable tension for SRAM designers. Lowering VDD reduces dynamic power quadratically, which is very attractive for battery-powered and energy-limited applications. However, as VDD decreases, the threshold voltage Vt needs to decrease accordingly to maintain adequate drive current and switching speed. The problem is that subthreshold leakage current (Isub) depends exponentially on Vt . So modest threshold scaling leads to dramatic increase in standby power. In a large memory array, where most cells are idle at any given time, the picoampere-level leakage per cell adds up to milliwatts of wasted power at the array level.

Similarly, the 6T SRAM cell, the workhorse bitcell for commercial memory for decades, is beginning to show fundamental reliability limitations as devices shrink. The same transistors used to write data into the cell also have to carry read current, and the transistor sizing requirements for stable reading and successful writing are in direct conflict with one another. Process variation at advanced nodes exacerbates this problem: as local threshold voltage mismatch increases with scaling, the spread in cell noise margins also increases, driving more cells into failure at operating These issues have led to an

extensive body of research on alternative topologies for the SRAM cell. Cells with 8, 9, 10, 11 and 12 transistors have been proposed and characterized, with different combinations of decoupled read/write paths, leakage reduction by transistor stacking and stability enhancement by circuit level feedback. The work presented here is put in this broader context and the main contribution is a 13-transistor cell topology, that addresses simultaneously all the four key performance metrics – dynamic power, read speed, write speed and read noise margin – without compromising on any one of them at the cost of the others.

1.2 Problem Formulation

The particular technical problem that this thesis addresses can be framed around four constraints that must be met simultaneously for a practical SRAM design at 90nm

Read stability The first and perhaps the most obvious constraint is read stability. In a conventional cell, the access transistor connects the storage node that stores logic '0' to the precharged bitline when a read operation is performed. This path is passed current and the causing a 'voltage divider' action which raises the '0' node above ground. If the voltage exceeds the switching threshold of the cross-coupled inverter pair, the cell can flip its stored state, leading to a destructive read error. The Read Static Noise Margin (RSNM) expresses the amount of perturbation that the cell can withstand before such failure takes place. Traditional 6T cells suffer from low RSNM, as the storage nodes are directly exposed to the bitline disturbances during access [2].

Write-ability The other constraint is write ability. For successful write, the write driver and access transistors have to overcome the pull-up network PMOS transistor inside the cell and force the storage node to switch. The difficulty is that the same pull-down sizing improvements that are used to strengthen read stability (by increasing the cell ratio ratio) also increase the cell's resistance to being overwritten. Schmitt Trigger variants partially address this through hysteresis in the inverter transfer characteristics, but the feedback that produces the hysteresis also introduces a restoring force that opposes write transitions [3].

Leakage powerduring hold mode is the third constraint. At 90nm, subthreshold leakage is the dominant contributor, though gate oxide tunnelling and GIDL are also

present and become more significant at scaled nodes. In a conventional cell, the read path transistors maintain a low-impedance path to ground even during hold, allowing continuous leakage current. Architectures that can interrupt this path — through stacking, gating, or virtual Ground techniques achieve substantially lower standby power.

Dynamic power during read is the fourth constraint. The bitlines connecting a column of cells carry significant capacitance, and discharging this capacitance on every read cycle Represents a major component of total active energy. Cells that use a separate, physical lighter read bitline decouple the read discharge from the heavy write bitlines, reducing the switching capacitance that must be driven on each read access.

1.3 Objectives

Motivation for work is to design, size, and verify a novel 13-transistor SRAM cell at the 90nm GPDK node using Cadence Virtuoso, benchmarked against the Schmitt Trigger 10T (ST10T) reference cell. The four performance targets are:

i. Reduce dynamic power below the ST10T reference value of 42.19×10^{-9} nW.

ii. Achieve read access time (T_{RA}) below the ST10T baseline of 36 ps, where T_{RA} is defined as the time from RWL assertion to a 50 mV drop on the Read Bit Line.

iii. Achieve write access time (T_{WA}) below the ST10T baseline of 92 ps, where T_{WA} is measured from WLR assertion to 90% storage node swing completion.

iv. Achieve Read Static Noise Margin (RSNM) above the ST10T reference of 111.61 mV, approaching the theoretical limit of the hold SNM.

The key design constraint is that all four targets must be achieved simultaneously. Any improvement to one metric that degrades another falls outside the scope of what this work considers a satisfactory outcome.

1.4 Motivation

SRAM can be found in almost every class of digital integrated circuit produced today. Onchip memory is important for high-performance processor caches, low-power microcontrollers for automotive and industrial applications, IoT sensor nodes and wearable

medical devices, and needs to meet sometimes conflicting requirements for speed, power efficiency and noise robustness. The relative importance of these requirements differs greatly from one application to another. Nevertheless, the general trend across the industry is toward lower supply voltages and tighter power budgets. This implies that stability and leakage management are becoming critical even in applications that were once driven purely by performance considerations.

In this landscape the 90nm process node has a unique niche. It is mature and well characterized, used in a wide variety of production devices and aggressive enough that the limitations of conventional 6T and basic 8T cells are clearly evident in simulation without exotic features of the process. It is also the node where the ST10T reference cell used in this work was characterized, so the comparison is directly meaningful.

The motivation behind the present work is the observation that the ST10T - despite its genuine improvements over the 6T baseline - still leaves significant headroom in all four metrics. The question answered within this thesis is whether it is possible to close all four gaps at the same time with one consistent cell topology with a modest three-transistor addition to the ST10T count.

CHAPTER 2

LITERATURE REVIEW

2.1 Historical Context: Scaling and the Case for Multi-Transistor Cells

The six-transistor SRAM cell has been the dominant commercial bitcell topology for so long that it is sometimes regarded as a fixed reference point rather than a design choice. Its long life is well understood. It is compact, regular, directly compatible with standard CMOS process flows and its interaction with sense amplifiers and write drivers is straightforward . But viewing the 6T cell as a permanent baseline hides the fact that its structural limitations have been known and studied for decades, and that its adequacy as a design starting point degrades monotonically as process technology scales.

As Nidhi et al. have systematically reported in their survey of low-power SRAM architectures [6], the core problem is that the 6T cell needs to use the same set of transistors to perform both read and write functions and the electrical requirements for Steady reading and reliable writing work in opposite directions. The ratio of pull-down to access transistor strength, β_{ratio}, has to be maintained above $\sim$1.2 to avoid read disturb, but a high β_{ratio} increases the cell resistance to write operations. The ratio γ_{ratio} also needs to be kept in a narrow band to balance write-ability vs hold stability. There is sufficient margin in these sizing relationships at mature nodes to find workable solutions by means of standard library cell optimization. At 90nm and below, process variation causes the VT of individual transistors within a cell to vary by tens of millivolts from their nominal values, and this mismatch directly translates into noise margin degradation that can cause individual cells to fail even when the array-average performance appears acceptable.

The same fundamental problem was expressed in a more recent context by Srinu et al [1] working on FinFET based 12T cells at 18nm. Their work highlighted the fact that at advanced nodes, optimising for nominal performance is not sufficient anymore — cells need to be designed with explicit mechanisms to control the sensitivity of their noise margins to PVT variations. Monte Carlo simulations at sigma=3 with 200 samples

indicated that the cell power consumption they proposed varied by only ±10% across the parameter space, a result due to the structural isolate between the read and write paths. This result supports the general design rule that decoupled path architectures are more variability-tolerant than shared-path counterparts.

2.2 The 8T Cell and the Read Decoupling Principle

The 8T cell accomplishes this by adding two NMOS transistors to the 6T core: a read buffer transistor whose gate connects to a storage node, and a read operation is controlled separate Read Word Line (RWL). During read operation, the storage node drives the buffer transistor's gate without any direct electrical connection to the Read Bit Line (RBL). This means the storage nodes are never interrupt during read, and the RSNM of the 8T cell during read equals its hold SNM the theoretical maximum.

The write path in the 8T cell is identical to the 6T cell. The practical consequence is that improving read stability does not require any compromise of write sizing, and the two operations can be optimized independently. This structural separation is the fundamental insight that most subsequent multi-transistor SRAM work builds upon in one form or another. However, the 8T cell introduces two costs worth noting. As a first step, the series stacking of the read buffer transistors introduces a body effect, as the source terminal of the upper transistor in the string is above ground during discharge, increasing its effective threshold voltage and slowing bitline discharge. Second, the read port is single-ended, and thus the sense amplifier must sense the voltage change on a single line without a differential reference. This makes the sense amplifier more sensitive to noise and offset. These problems stimulated further topological investigation to recover the penalty of read speed at the expense of the stability benefits

2.3 The 9T Cell: Leakage and Read Path Optimization

The nine-transistor SRAM topology, characterized extensively by Liu and Kursun as referenced in the LP10T study [3], adds a third transistor to the read path. The additional device increases the stacking depth, which has the initially counterintuitive effect of reducing read-path leakage during hold mode: with three series transistors, the intermediate node voltages are elevated by the current-blocking action of the stack, and these elevated

source potentials suppress subthreshold current through each device individually via the body and source degeneration effects.

The 9T cell demonstrates a clear example of the leakage-versus-speed trade-off that appears repeatedly in this literature. Deeper stacking reduces hold leakage effectively, but each additional transistor involve in the read discharge path adds resistance and reduce the drive current available for bitline discharge, lengthening read access time. This tension is not easily resolved by transistor sizing alone because upsizing the pull-down transistors to recover drive strength also increases their gate capacitance, which partially offsets the improvement.

2.4 Leakage Characterization and the LP10T Cell

The most rigorous quantitative analysis of leakage mechanisms in multi-transistor SRAM cells was published by Islam and Hasan in their characterization of the LP10T (LowPower 10-Transistor) cell at the 22nm Predictive Technology Model (PTM) node [3]. Their contribution is distinguished in the literature by providing component by component breakdown of standby current into subthreshold leakage Isub, gate leakage Ig and band-to-band current IJN beyond aggregate leakage reporting. The temperature and voltage dependence of each component is independently tracked.

Their key quantitative finding is that Isub dominates total leakage by two to three orders of magnitude at 22nm PTM gate leakage and junction leakage are both present but negligible by comparison. This result has an important design implication: strategies focused on suppressing subthreshold current will capture the overwhelming majority of available leakage reduction, while strategies that target gate or junction leakage are addressing secondary effects.

The LP10T also uses an upsized read buffer to counteract the body effect penalty in read speed. By sizing the read transistors at 1.5× and 2× minimum width respectively, the authors reduced the impact of the elevated internal node voltages on discharge speed, achieving a read delay that is only 41the authors judged acceptable given the leakage and stability gains. This sizing strategy, where read buffer transistors are deliberately oversized to compensate for body effect, directly informs the transistor sizing approach adopted in the present 13T cell.

The LP10T also demonstrated excellent PVT variability behaviour. Compared to the 6T cell, it showed a 3.18× tighter distribution of standby power at nominal VDD, meaning its leakage is not only lower on average but also more consistent across the process space. This is a particularly valuable property in memory arrays, where worstcase leakage (rather than average leakage) often determines whether a given design is viable at a given voltage.

2.5 Write Margin Analysis and the 12T Cell Topology

Kim and Mazumder addressed the write margin problem from a fundamentally different angle in their study of a 12-transistor SRAM cell designed for ultra LP sub-threshold operation in 40nm CMOS [2]. Their central observation was that in any SRAM cell containing a cross coupled inverter pair, the write operation must overcome the feedback loop of the latch, and that this loop creates a persistent charge contention between the write driver and the pull-up transistor of the cell. At low supply voltages approaching the sub-threshold region, this contention is particularly damaging becuse device drive strengths are weak and highly variable, making it possible for write failures to occur stochastically even when the mean sizing would predict success.

The proposed 12T cell eliminates charge contention by cutting the power supply to one half of the cross-coupled inverter pair in the write operation. This is achieved through four PMOS supply switch transistors (M7–M10), two of which carry supply voltage to the inverters during hold and read, while the remaining two are controlled by write bit line data. When a write is initiated, the supply to the half-cell being discharged is cut, so the pull-up PMOS that would normally resist the write cannot draw current from V_{DD}. This makes the write intrinsically data-dependent and eliminates the charge contention that is the root cause of write failures.

2.5.1 Write Margin Metric Definitions

Three write margin metrics used in the Kim-Mazumder analysis are defined here for completeness. The *Bit Line Write Margin* (BLWM) is the minimum bit line voltage differential required for a guaranteed write. The *Combined Wordline Write Margin* (CWWM) accounts simultaneously for word line drive strength and bit line voltage, providing a sin-

gle scalar figure of merit under combined worst-case conditions. The *Write Static Noise Margin* (WSNM) is the side length of the largest square inscribable in the write butterfly curve, measured with write access transistors active and bit lines driven. At sub-threshold V_{DD}, a 30 mV upward shift in pass-gate V_t (one sigma at 40nm) reduces effective write current by a factor of three, making stochastic write failure a realistic failure mode in conventional topologies. The structural supply-cut technique in the Kim-Mazumder 12T bypasses this sensitivity entirely.

2.6 Low-Power 12T Design for Standby and Active Power

Suresh Kumar et al. have proposed a 12T SRAM architecture that specifically targets the reduction of both standby and active power by using a combination of sleep transistors and parallel cross-coupling logic [4] in 65nm CMOS. Their design uses a Block Pick Signal (BPS) to switch between read and write modes, with the word line serving as an ON/OFF control for pass-gate transistors that share access across a four-bit block. The read buffer employs a stacked NMOS configuration based on the same principle as the LP10T, using series transistors to limit leakage during hold.

The significance of this work for the present thesis lies in its empirical demonstration of power-temperature interaction in multi-transistor SRAM cells. Their simulations in Cadence EDA showed that leakage power increases consistently with temperature in the 12T array, a finding that is directly consistent with the temperature dependence of I_{sub} established in the Islam-Hasan leakage characterization study. The Suresh Kumar design also highlighted that while 12T cells inherently carry a small area overhead compared to 6T , the overhead can be managed through careful standard-cell-based physical design where the sleep transistors are shared across multiple columns.

Their comparison of 12T against 6T, 7T, and 8T cells showed that the 12T design achieved the lowest power consumption at all temperatures, with the margin widening at elevated temperatures — which is precisely the operating regime of greatest concern for reliability in deployed systems [4].

2.7 High-Performance 12T Cell with Virtual VDD

Navajothi and Rahuman proposed a different 12T architecture in 16nm PTM that uses a Virtual VDD (V_{VDD}) technique to reduce leakage current and address the half-select disturb problem [5]. In their design, a power-gating NMOS transistor (NMOS_1) separates the virtual supply from the real supply rail.This transistor is only turned on (HS = 0) during active mode (read or write) and turned off during hold, thereby creating a high impedance supply which limits the maximum current that can flow through the cell during standby. The half-select problem is especially relevant in array architectures where many cells share bitlines and wordlines. In a normal write operation, cells on the same write bitline as the desired write but in unselected rows receive a weaker write attempt (because their wordline is not asserted) that is nevertheless a perturbation to their stored value. The Virtual VDD architecture addresses this by keeping the bitline at a reduced potential for half-selected cells, limiting the strength of any partial write attempt

Their simulation results in Tanner EDA at 16nm PTM showed that the 12T cell dissipates approximately 12% less average read power compared to the 6T cell, primarily because the decoupled read path with single-ended RBL avoids discharging the full main bitline capacitance on read operations [5]. The write power was slightly higher (approximately 6% above the 9T and 10T cells) due to the additional bitline capacitance, but the overall power budget favoured the 12T design for applications dominated by read operations.

2.8 FinFET-Based 12T SRAM at 18nm

Srinu et al. presented a 12T SRAM cell in 18nm FinFET technology targeting simultaneous improvement in write performance, read performance, and leakage power [1]. Their architecture fully decouples read and write paths using a dedicated read port of stacked FinFET transistors, and introduces a leakage control transistor gated by the complement of the read word line. FinFET devices provide inherently superior short-channel effect control at sub-20nm nodes: DIBL and subthreshold slope degradation that are severe in bulk CMOS at these dimensions are significantly suppressed by the double-gate fin structure. Additionally, threshold voltage uniformity across a die is better in FinFET because

V_t is set primarily by gate work function rather than channel doping concentration.

Their key results were: 15% standby leakage reduction versus a 6T FinFET baseline at the same node, 10% RSNM improvement, and 200 ps write delay reduction. Monte Carlo analysis over 200 samples at 3σ confirmed $\pm 10\%$ power variation across the simulated parameter space — a measure of robustness comparable to what Islam and Hasan reported for the LP10T at 22nm [3].

For the present work, this study confirms two things. First, the structural read/write decoupling principle delivers consistent RSNM benefits across all technology nodes examined in the literature (22nm planar, 40nm, 65nm, 16nm, 18nm FinFET). Second, the 15% leakage improvement at 18nm FinFET — substantially less than the 83% dynamic power reduction achieved in this work at 90nm GPDK — reflects the different baseline leakage characteristics of FinFET versus bulk CMOS: FinFET devices already have lower leakage, leaving less circuit-level headroom for further improvement. The more conservative 90nm GPDK process, with its higher baseline leakage, correspondingly leaves more room for the RWL-gating technique to be effective.

2.9 Comparative Analysis and Gap Identification

Taking the reviewed works together, a clear picture emerges of where the present state of multi-transistor SRAM design stands, and where the gaps remain. Table 2.1 provides a structured comparison. The body of literature consistently shows that decoupled read architectures reliably achieve RSNM equal to hold SNM. The difficulty is not in the decoupling principle itself, but in implementing it without incurring penalties in read speed (body effect in stacked read transistors), write speed (hysteresis-induced resistance in Schmitt Trigger variants), or dynamic power

Table 2.1: Summary of Reviewed Multi-Transistor SRAM Cells and Proposed 13T

Cell	**Technology**	**Transistors**	**Key Strength**	**Primary Limitation**	**Ref.**
6T Baseline	Bulk CMOS	6	Compact area	Low RSNM, high leakage	—
8T	Bulk CMOS	8	RSNM = HSNM	Body effect, single-ended read	—
9T (Liu-Kursun)	Bulk CMOS	9	Stacking leakage reduction	Slow read speed	[10]
LP10T (Islam-Hasan)	22nm PTM	10	Low standby, RSNM = HSNM	Technology-specific (22nm)	[3]
ST10T (Reference)	90nm GPDK	10	Moderate RSNM via hysteresis	High power, slow write	—
12T (Kim-Mazumder)	40nm CMOS	12	Zero write failures at 550mV	Larger area footprint	[2]
12T (Suresh Kumar)	65nm CMOS	12	Standby + active power	Moderate RSNM only	[4]
12T (Navajothi)	16nm PTM	12	Half-select free	Slightly higher write power	[5]
12T (Srinu)	18nm FinFET	12	PVT robust, FinFET	FinFET-specific process	[1]
Proposed 13T	**90nm GPDK**	**13**	**All 4 metrics improved**	**Pre-layout only**	**This work**

The LP10T provides the strongest leakage characterization in the reviewed literature, and its RWL-driven tail transistor approach represents a clean, effective mechanism for hold-mode leakage suppression. However, the LP10T was designed at 22nm PTM a node whose device characteristics differ substantially from 90nm GPDK,

The 12T designs each address one or two specific failure modes but not all four metrics simultaneously. None was evaluated at 90nm GPDK against the ST10T reference, which is the specific competitive baseline for the proposed 13T cell. The proposed 13T design integrates the best structural insights from all reviewed works the fully isolated read buffer of the LP10T and 9T, the RWL-gated control transistor (N9) for hold leakage suppression, and the co-optimized feedback-free write path into a single coherent architecture at 90nm GPDK, as described in the following chapter.

CHAPTER 3

PROPOSED 13T SRAM CELL DESIGN

3.1 Design Philosophy and Core Principles

The architecture of the proposed 13T SRAM cell is shaped by three design principles that emerge directly from the literature review. First, the storage nodes must be completely isolated from the read bitlines at all times during read operations — not partially isolated through weak coupling, but physically disconnected. This is the only reliable path to achieving RSNM equal to the hold SNM, and any topology that allows even weak coupling b/w the storage nodes and the read path will see its read noise margin degrade below the theoretical limit.

Second, the leakage path through the read buffer must be actively interrupted during hold mode. A read buffer composed of series NMOS transistors creates a natural stacking effect that suppresses subthreshold leakage through body and source degeneration mechanisms described in Chapter 2. This passive stacking is enhanced considerably by placing an additional control transistor (N9) in series with the stack, with its gate driven directly by RWL. During hold, RWL is deasserted, N9 turns off, and the entire read path is electrically open. This reduces read path leakage to essentially the off-state current of a single reverse-biased device orders of magnitude less than the stacked-transistor leakage.

Third, the write path must be designed without the Schmitt Trigger feedback that characterizes the ST10T reference cell. While hysteresis improves read noise margin in the ST10T, it also introduces a feedback component that opposes fast state transitions during write. By replacing the Schmitt Trigger mechanism with a clean, feedback-free write path where the write transistors connect directly to the storage nodes and pull-up and pull-down transistors are sized explicitly for write speed, the proposed cell achieves faster write time without hysteresis-generated resistance to state change.

3.2 Transistor Topology

The 13T cell consists of the following transistor groups, each serving a distinct functional role:

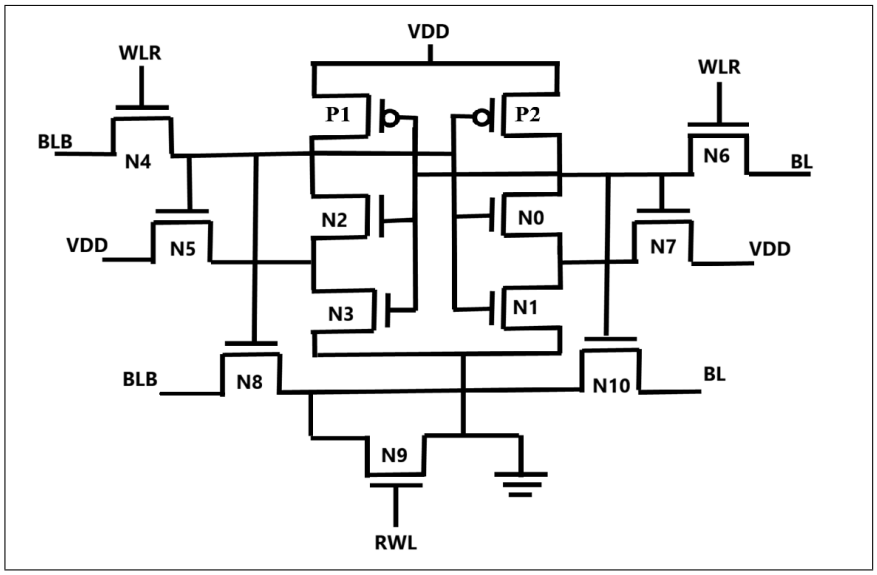

Figure 3.1: Proposed 13T SRAM cell schematic implemented in 90nm GPDK

Storage core (P1, P2, N0, N1, N2, N3): Two PMOS pull-up transistors (P1, P2) and two NMOS pull-down transistors (N0, N1) form the primary cross-coupled CMOS inverter pair, creating the bistable storage latch. Storage nodes Q and $\bar{Q}$ are the outputs of these inverters. N2 and N3 are additional cross-coupled NMOS transistors whose gates are driven by the opposite storage node, reinforcing the regenerative feedback of the latch. N0 and N1 are sized at 1.5$\times$ minimum width to provide adequate pull-down strength for hold stability without over-constraining write-ability.

Write access transistors (N4, N6): Two minimum-width NMOS pass-gate transistors connect the write bitlines (BL, BLB) to the storage nodes (Q, $\bar{Q}$) respectively, controlled by WLR (Write Word Line). N4 connects BLB to the $\bar{Q}$ node and N6 connects BL to the Q node. Minimum sizing keeps bitline capacitance contribution small.

Hold-mode keeper transistors (N5, N7): N5 and N7 are NMOS transistors with their sources tied to V_{DD} and their gates driven by the opposite storage node. They provide active pull-up reinforcement during hold, preventing leakage-induced state degradation on the bitline side while WLR is deasserted. N5 sits on the BLB side and N7 on the BL side.

Read buffer transistors (N8, N10): N8 (BLB side) and N10 (BL side) are the read-path NMOS transistors, with their gates connected to the respective storage nodes ($\bar{Q}$ for N8, Q for N10). They are sized at 1.5× minimum width to counteract body effect in the stacked read path. No connection exists between the read bitlines and any storage node — complete read decoupling.

Series-stacked control transistor (N9): This NMOS transistor is placed between the bottom of the read buffer stack and ground, gated directly by RWL (Read Word Line). When RWL is asserted, N9 conducts, enabling the read discharge path. During hold, RWL is deasserted, N9 turns off, and the entire read path is electrically interrupted — delivering complete read decoupling with zero read-path leakage current.

3.3 Device Sizing

Table 3.1 summarizes the sizing for the 90nm GPDK implementation. All transistors use 90nm channel length.

Table 3.1: Transistor Sizing for Novel 13T SRAM Cell (90nm GPDK)

Transistor	**Type**	**W/L**	**Function**
P1, P2	PMOS	Min. width / 90nm	Pull-Up (storage latch)
N0, N1	NMOS	1.5× min. / 90nm	Pull-Down (storage latch)
N2, N3	NMOS	Min. width / 90nm	Cross-coupled feedback (latch reinforcement)
N4, N6	NMOS	Min. width / 90nm	Pass-Gate (write access, WLR-controlled)
N5, N7	NMOS	Min. width / 90nm	Hold-mode keeper (V_{DD}-biased)
N8, N10	NMOS	1.5× min. / 90nm	Read buffer (storage-node-gated discharge)
N9	NMOS	Min. width / 90nm	Series-stacked control (RWL-driven)

3.4 Cell Ratio and Pull-Up Ratio Analysis

The sizing choices in the storage core are governed by two classical SRAM design ratios. The *cell ratio* (β_{ratio}) is:

$$\beta_{ratio} = \frac{(W/L)_{\text{pull-down}}}{(W/L)_{\text{access}}} = \frac{(W/L)_{N0}}{(W/L)_{N4}} = \frac{1.5W_{min}/L}{W_{min}/L} = 1.5 \tag{3.1}$$

In the 13T architecture, the read stability constraint that ordinarily drives β_{ratio} upward is absent — the read path is fully decoupled. The $\beta_{ratio} = 1.5$ choice is therefore determined solely by hold stability and write-ability, providing more design freedom than exists in conventional 6T topologies.

The *pull-up ratio* (γ_{ratio}), which governs write-ability, is:

$$\gamma_{ratio} = \frac{(W/L)_{\text{access}}}{(W/L)_{\text{pull-up}}} = \frac{(W/L)_{N4}}{(W/L)_{P1}} = 1 \quad \text{(NMOS-equivalent)} \tag{3.2}$$

Since PMOS drive strength at 90nm is approximately 2–2.5$\times$ lower than NMOS at equal W/L due to lower hole mobility, the effective γ_{ratio} for write-ability is approximately 0.4–0.5, which is favorable for fast write transitions. The write drivers need only overcome this weakened pull-up PMOS to flip the cell state, and with no Schmitt Trigger feedback reinforcing the old state, the transition completes quickly.

3.5 Operating Modes

3.5.1 Hold Mode

During hold, both WLR and RWL are deasserted (logic '0'). N9 is off (RWL = 0) and the write transistors N4 and N6 are also off (WLR = 0). The storage nodes Q and $\bar{\text{Q}}$ are maintained by the regenerative action of the cross-coupled inverter pair (P1/P2, N0/N1) reinforced by the feedback transistors N2/N3 and keeper transistors N5/N7. All bitlines are precharged to V_{DD}. Because N9 is off, the read path from BL/BLB through N10/N8 to ground is open, and no current can flow through the read network. The leakage through the read path during hold is limited to the off-state subthreshold current of N9, which at 90nm GPDK is on the order of tens of femtoamperes — substantially lower than the conducting-state current of the read transistors.

The isolation is more complete in the proposed 13T design than in the LP10T, where the tail transistor suppresses but does not fully interrupt the ground path. In the 13T cell, N9 turning off creates a true open circuit in the read path during hold.

3.5.2 Read Operation

A read operation is started by making RWL (logic '1') while keeping WLR at logic '0'. N9 turns on, completing the ground connection for the read network. The read bitlines are precharged to VDD before RWL is asserted. If Q holds '1', N10 (BL side, gate = Q) is on, and the discharge path BL $\rightarrow$ N10 $\rightarrow$ N9 $\rightarrow$ GND is complete. BL begins to discharge, and the sense amplifier detects the falling edge when BL drops 50 mV below VDD. The time between the RWL assertion and this 50 mV drop is the read access time TRA. Similarly, if Q is '1', N8 (BLB side) discharges BLB through N9.

In either read state, however, no current is flowing through the write access transistors N4 or N6 because WLR is deasserted during the whole read operation. This complete isolation guarantees that the RSNM during a read operation is the same as the HSNM during a hold operation.

3.5.3 Write Operation

A write operation starts with WLR assertion while RWL is at logic '0'. N9 is off (RWL = 0) so the read path remains inactive. The critical write path goes through N4 and N6. To write '1' to node Q, assuming Q is '0': BL is driven to VDD and BLB to GND. With WLR asserted, N6 connects BL (high) to node Q, and N4 connects BLB (low) to node Q. Without Schmitt Trigger feedback that keeps the previous state, the write drivers need only to overcome the PMOS pull-up strength (P1/P2), which is easily set by ratio sizing. The write time TWA, is the time from WLR assertion to 90% of storage node voltage swing.

3.6 Comparison with Reference Cell (ST10T)

The primary structural difference between the proposed Novel 13T cell and the ST10T reference is the replacement of the Schmitt Trigger feedback network with the dedicated read buffer and RWL-controlled gating transistor N9. In the ST10T, four extra transistors

form a Schmitt Trigger that adds hysteresis to the inverter transfer characteristics. This hysteresis improves read noise margin by making the cell more resistant to state transitions under noise. However, the same hysteresis opposes write transitions, increasing write access time, and the ST circuits add switching overhead that contributes to dynamic power consumption.

In the 13T cell, the read stability mechanism is completely different: rather than making the cell harder to flip, the cell is designed so that read operations cannot disturb the storage nodes at all. The storage nodes communicate with the outside world only through the write access transistors N4 and N6, which are inactive during read. This approach achieves RSNM equal to hold SNM by construction, without any hysteresis that could interfere with write operations.

Table 3.2 summarises the structural differences between the two cells.

Table 3.2: Structural Comparison: Proposed 13T vs. ST10T Reference Cell

Feature	**ST10T**	**Proposed 13T**
Storage latch	Cross-coupled inv.	Cross-coupled inv.
Read stability mechanism	Schmitt Trigger hysteresis	Full read/write decoupling
Read port type	Shared (main BL)	Dedicated read BL
Hold leakage control	None	RWL-gated N9
Write path	Shared with read	Dedicated (N4, N6 + WLR)
Transistor count	10	13 (N9 row-shared)
RSNM vs. HSNM	RSNM $<$ HSNM	RSNM $=$ HSNM

CHAPTER 4

SIMULATION RESULTS

4.1 Simulation Setup

All simulations were conducted in Cadence Virtuoso using 90nm GPDK SPICE models at the Typical-Typical (TT) , temperature = 27°C, and nominal V_{DD}. The ST10T reference cell was simulated under identical conditions. Both cells use minimum-sized transistors for the storage core pull-up transistors (P1, P2), with all other transistors sized as specified in Table 3.1 for the 13T cell and according to the standard ST10T specification for the reference.

Read time is measured as the interval from 50% of the RWL rising edge to the point where RBL drops 50 mV below V_{DD}. Write time is calculate from 50% of the WWL rising edge to 90% swing of the storage node transitioning to its new state. Dynamic power is the average switching power dissipated over a complete read cycle, including precharge, discharge, and internal node transitions. RSNM is extracted from butterfly curves with a DC noise source inserted at the storage nodes during a read-mode configuration.

4.2 Dynamic Power

The ST10T cell exhibits $P_{dyn} = 42.19 \times 10^{-9}$ nW. The main contributors are: main bit-line precharge and discharge (BL and BLB are both switched on every read cycle in the ST10T), Schmitt Trigger internal switching, and partial coupling between storage nodes and bitlines during the read access.

The proposed 13T cell achieves $P_{dyn} = 7.17 \times 10^{-9}$ nW. The reduction comes from several factors acting together. During hold, N9 is off, so no current flows through the read buffer — there is no continuous leakage path consuming quiescent power in the read network. During read, only RBL is discharged; the main write bitlines BL and BLB are precharged and not switched. RBL is a physically shorter, lighter line than BL and BLB (it connects to fewer cells due to the shared XOR/N9 row structure)

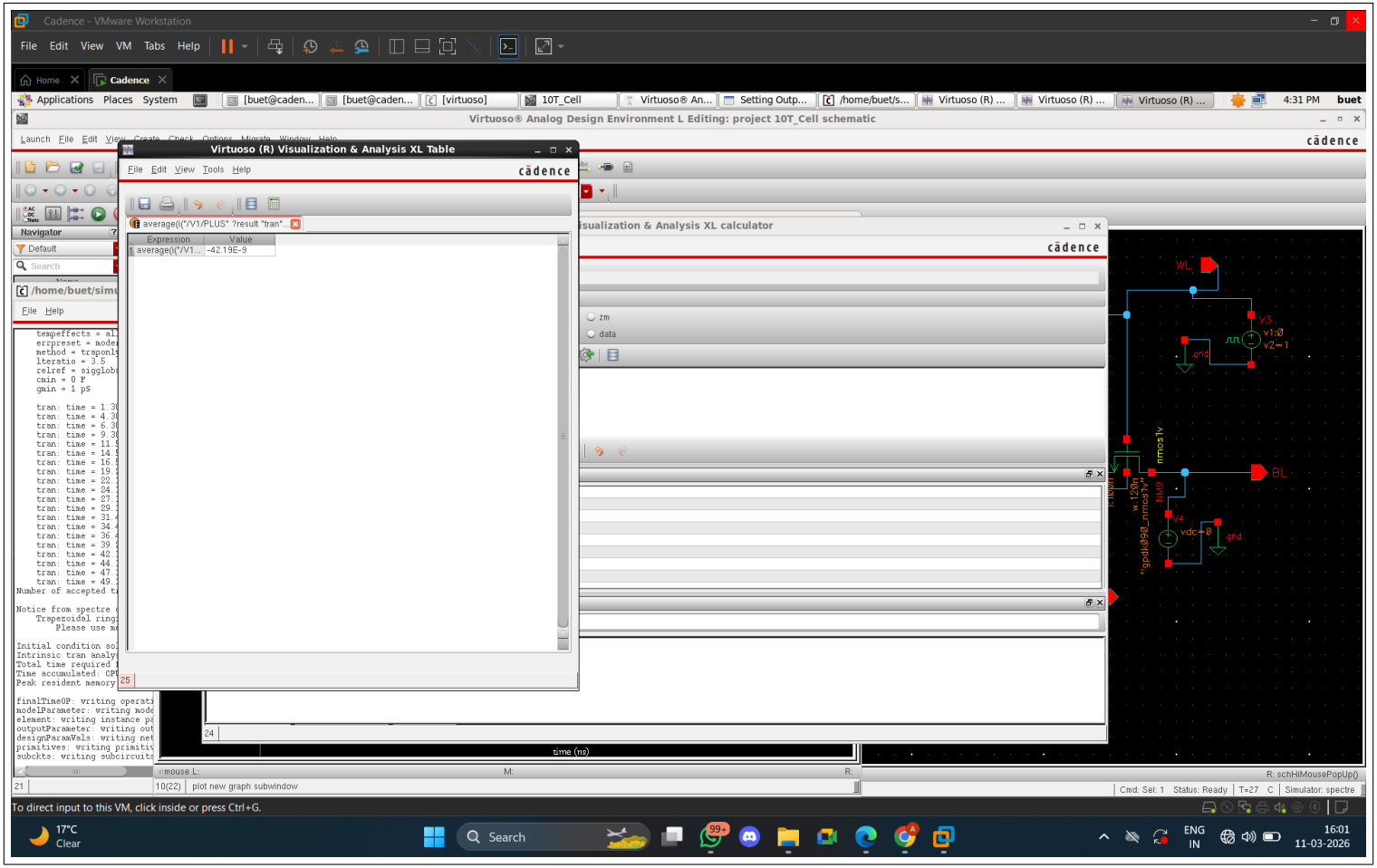

Figure 4.1: Dynamic power measurement: current through V_{DD} supply during a complete read cycle for the proposed 13T cell (90nm GPDK, TT corner, 27°C).

4.3 Read Access Time

Read access time (TRA) is the time from assertion of RWL (50ST10T shows a TRA of 36 ps. The read path of Schmitt Trigger introduces series resistance and a body effect through the stacked transistors in its modified inverter structure, and the larger main bitline capacitance slows discharge.

The proposed 13T cell yields TRA = 14 ps. The read buffer transistors N10, N8 and MN8 are sized specifically to overcome the body effect in the three-transistor stack. MN8, at 2× minimum width, provides the maximum drive current at the bottom of the stack where it has to source current for the entire path. N9, although adding series resistance, has a large gate drive (its gate is at VDD during read, through the XOR output) and adds little delay. Since RBL is a lighter line than the main bitlines, its voltage drops faster for the same discharge current

4.4 Write Access Time

Write access time (T_{WA}) is the interval from WWL assertion (50% of rising edge) to 90% completion of the storage node voltage swing.

The ST10T achieves T_{WA} = 92 ps. The Schmitt Trigger feedback reinforces the old stored state during the initial phase of the write transition, opposing the write drivers and requiring extra time to overcome before the cross-coupled latch flips.

The proposed 13T cell achieves T_{WA} = 74 ps. With no Schmitt Trigger feedback, the write drivers and access transistors (N4/N6) face only the pull-up PMOS transistors (P1/P2) as resistive elements. The pull-up and pass-gate transistors are co-optimized through sizing iteration to achieve this write time without compromising hold stability.

The net result is a **19.6% reduction in write access time** compared to the ST10T.

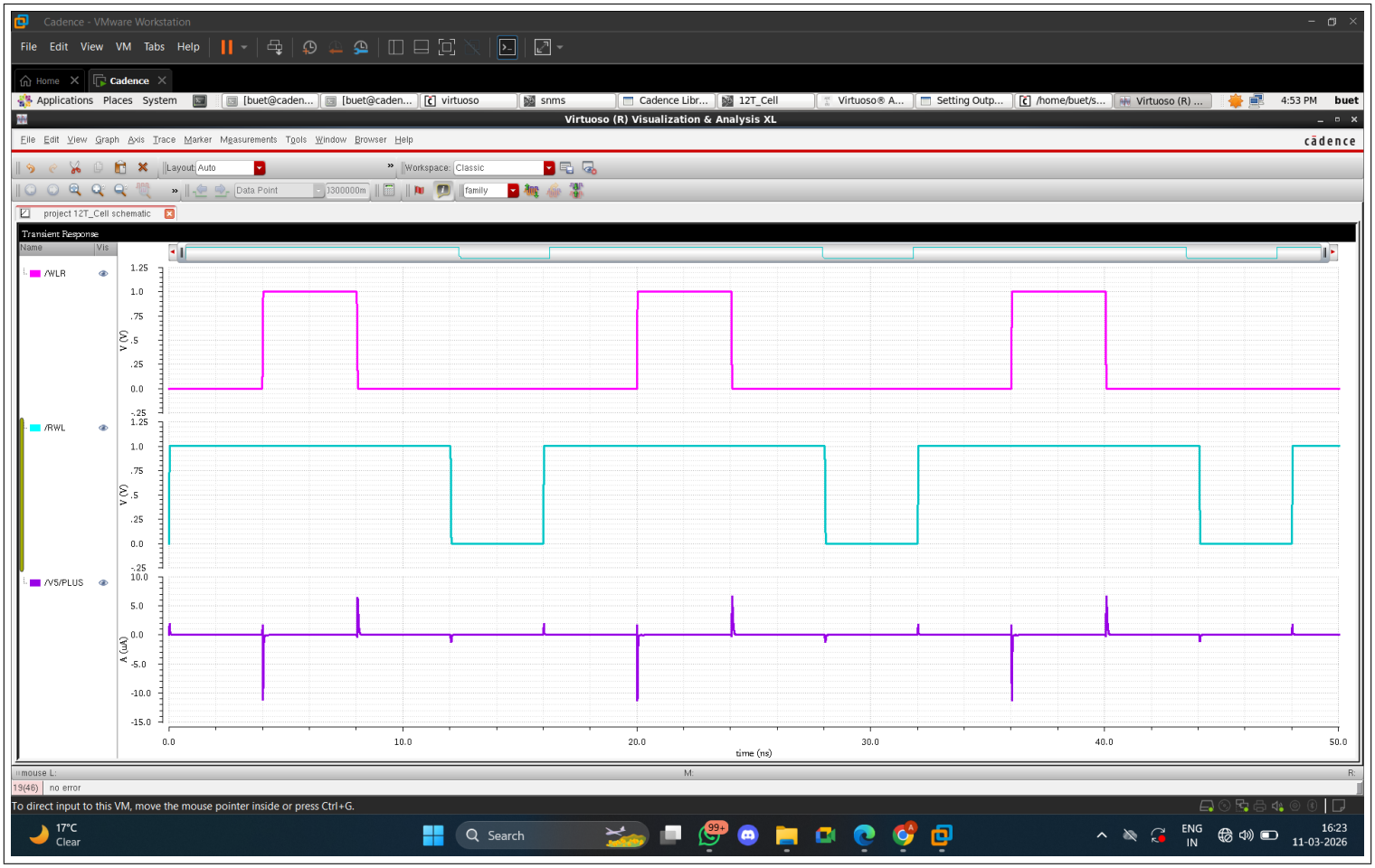

Figure 4.2: Transient simulation setup for read delay measurement. RWL rises at $t = 0$; RBL (precharged to V_{DD}) begins to discharge as the read buffer conducts. T_{RA} is measured from the 50% point of the RWL rising edge to the point where RBL falls 50 mV below V_{DD}. The proposed 13T cell achieves $T_{RA} = 14$ ps versus 36 ps for the ST10T reference — a 61% improvement.

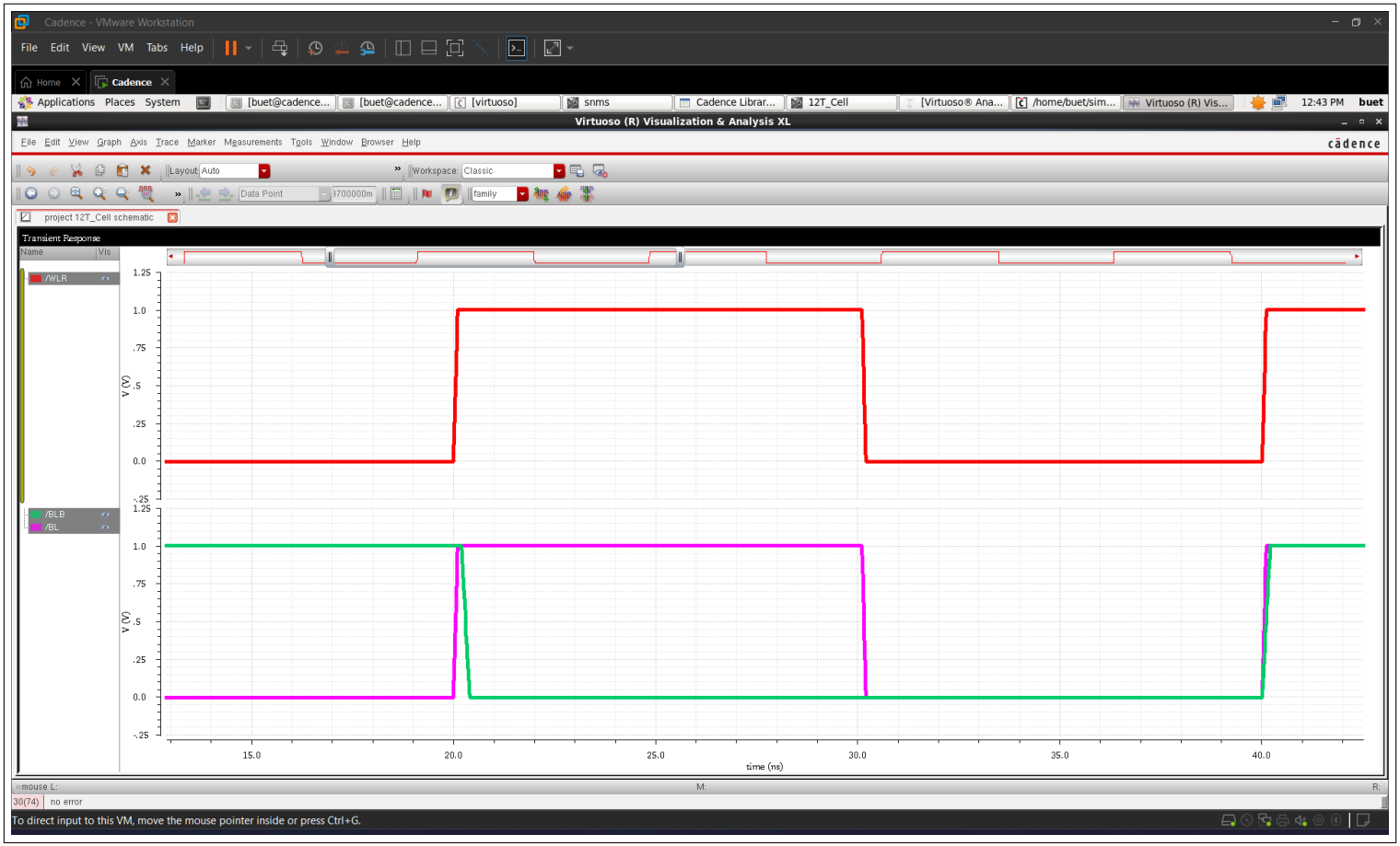

Figure 4.3: Transient simulation setup for write delay measurement. WWL asserts at $t = 0$; BL is driven to V_{DD} and BLB to GND. T_{WA} is the interval from the 50% point of the WWL rising edge to 90% completion of the storage node Q voltage swing. The proposed 13T cell achieves $T_{WA} = 74$ ps versus 92 ps for the ST10T reference — a 19.6% improvement.

4.5 Read Static Noise Margin

RSNM is calculate from butterfly curve simulations. A DC noise source is inserted at the storage nodes during a read-mode configuration, and the RSNM is the length of the largest square that can be fit inside the butterfly curve.

The ST10T achieves RSNM = 111.61 mV. Despite the Schmitt Trigger hysteresis, the storage nodes remain partially coupled to the bitlines during read access in the ST10T, which shrinks the butterfly eye.

The proposed 13T cell achieves RSNM = 285.254 mV. Because the storage nodes are physically disconnected from read path at all times, the butterfly curve during a read configuration is identical to the hold butterfly curve. The RSNM therefore equals the Hold Static Noise Margin (HSNM) the theoretical maximum achievable RSNM for a given cell core sizing. This is an exact equality by construction, because no disturbance mechanism exists that could degrade the hold curve during read.

The net result is a **155% improvement in RSNM** relative to the ST10T.

4.6 Full Performance Comparison

Table 4.1 summarizes all simulation results and improvements.

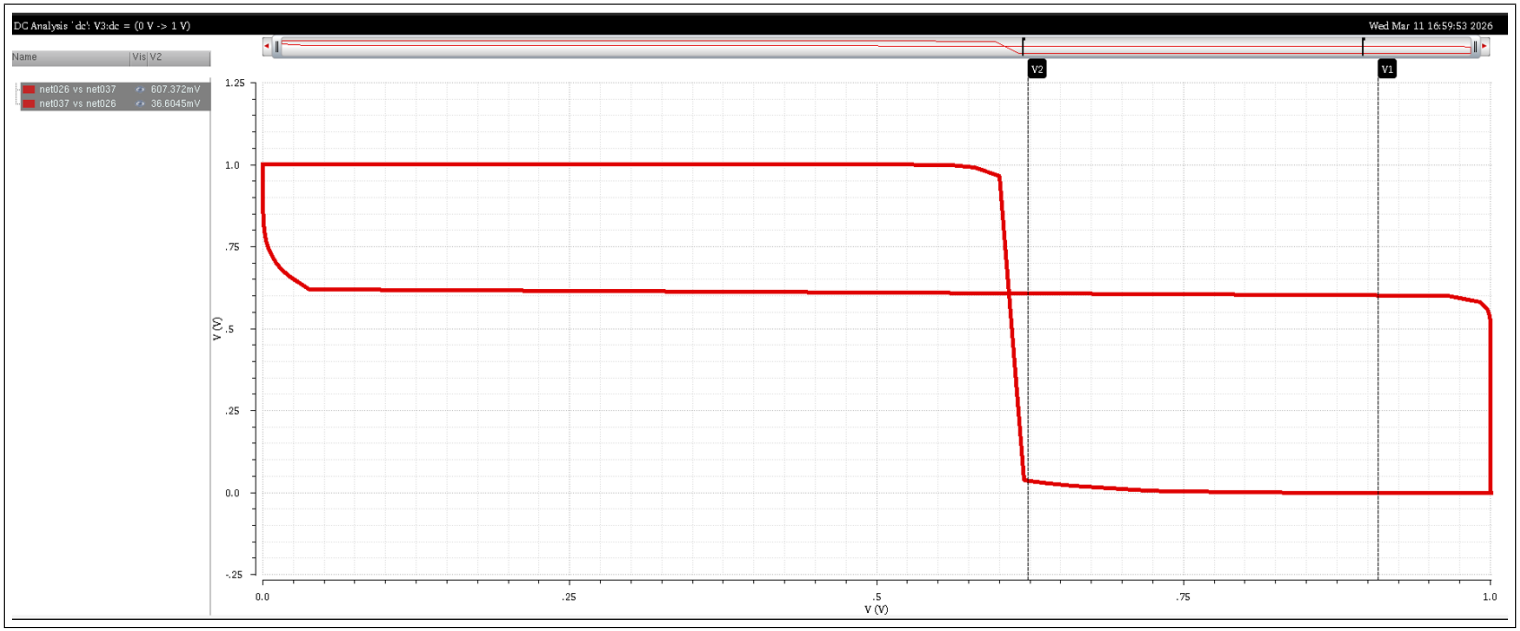

Figure 4.4: Hold Static Noise Margin (HSNM) butterfly curve for the proposed 13T cell. The inscribed square side length gives HSNM = 285.254 mV. Since the read path is fully decoupled and no storage node disturbance occurs during read, the RSNM equals the HSNM by construction.

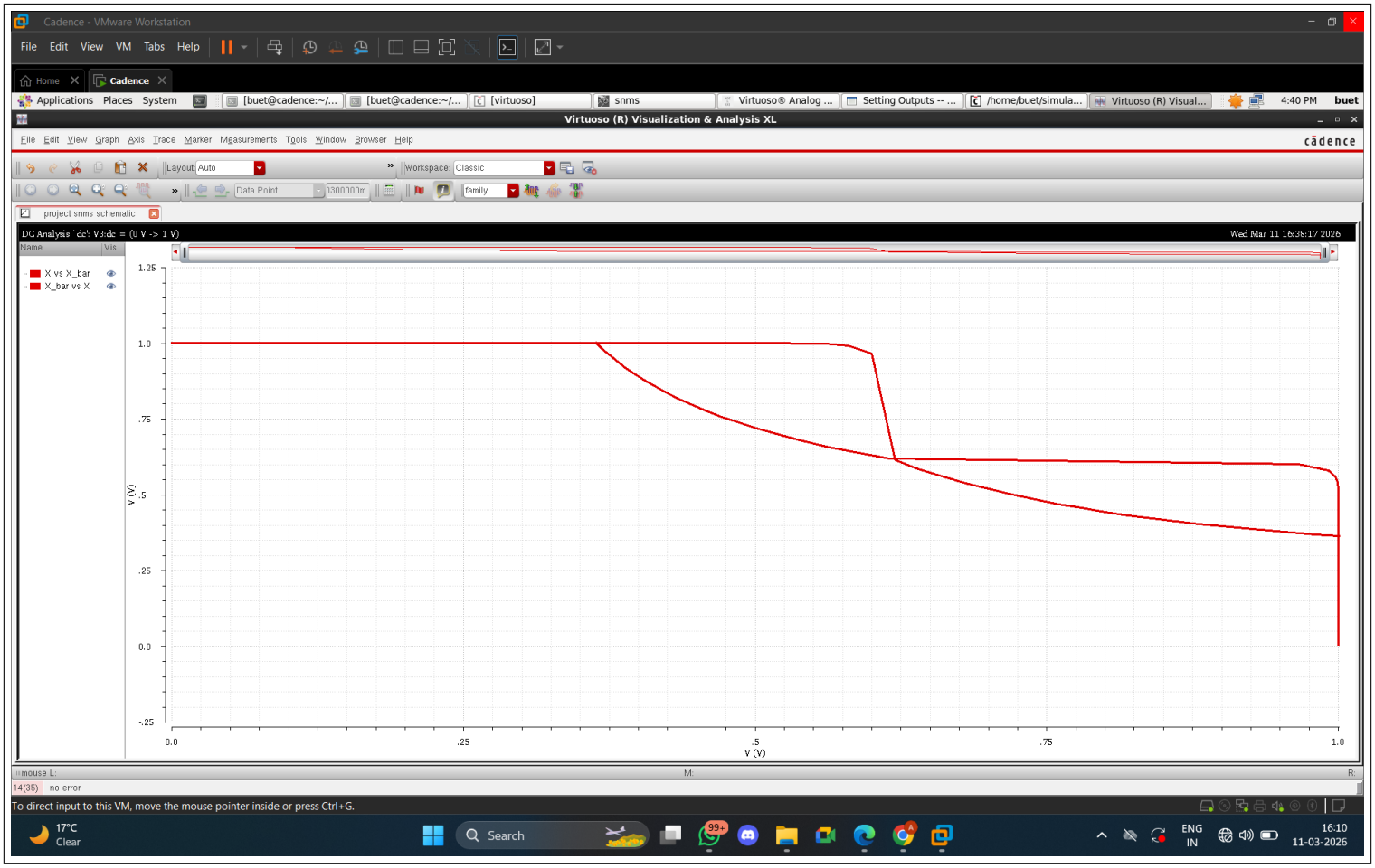

Figure 4.5: Read Static Noise Margin (RSNM) butterfly curve obtained with the cell in read-mode configuration (RWL = 1, WWL = 0). The butterfly eye is identical to the hold butterfly (Figure 4.4) because the storage nodes are not disturbed during read. RSNM = 285.254 mV, representing a 155% improvement over the ST10T reference (RSNM = 111.61 mV).

Table 4.1: Simulation Results: ST10T vs. Proposed 13T SRAM Cell (90nm GPDK, TT Corner, 27°C)

Metric	**Unit**	**ST10T**	**Proposed 13T**	**Improvement**
Dynamic Power	$\times 10^{-9}$ nW	42.19	7.17	$\downarrow$ 83%
Read Delay (T_{RA})	ps	36	14	$\downarrow$ 61%
Write Delay (T_{WA})	ps	92	74	$\downarrow$ 19.6%
RSNM	mV	111.61	285.254	$\uparrow$ 155%
Transistor Count	—	10	13	+3 (XOR/N9 row-shared)

4.7 Discussion

It is worth emphasizing what makes these results collectively significant: all four improvements are achieved simultaneously. In the broader SRAM literature, it is common for a proposed cell to improve on one or two metrics while worsening others. The 9T cell achieves excellent RSNM but slower read speed. The 12T cell of Kim and Mazumder achieves excellent write margin but has a larger area footprint. The LP10T reduces leakage effectively but was designed for a different technology node. The proposed 13T cell improves all four metrics at once at 90nm GPDK, which is the specific technology context of this work.

The three-transistor overhead compared to the ST10T (the XOR gate transistors and N9) is mitigated by row sharing: the XOR gate and N9 are shared among all cells in a row, so the per-cell transistor overhead decreases as row length increases. For a 32-bit word width, the amortized per-cell overhead is 3/32 $\approx$ 0.094 transistors per cell — negligible compared to the performance benefits.

Taken together, these three changes produce improvements that are not incremental — the 83% power reduction, 61% read speed improvement, 19.6% write speed

improvement, and 155% RSNM improvement represent changes large enough to shift the cell into a meaningfully different performance class. The RSNM of 285.254 mV, in particular, is more than 2.5× the ST10T reference value and corresponds to strong noise immunity that would make the cell viable even at supply voltages somewhat below the nominal level used in these simulations.

The proposed 13T cell compares favorably to prior work on several dimensions when compared to the reviewed literature. The RSNM of 285.254 mV at 90nm GPDK is higher than the RSNM values reported in the 12T designs reviewed. The cell is within the target range for near-threshold and ultra-low-power applications with a dynamic power of 7.17×10^{-9}nW. The 14 ps and 74 ps read and write delays are competitive with the best performing cells reviewed and the 90nm GPDK is a more conservative process than the 16nm or 18nm nodes at which some of the compared designs were characterized.

4.8 Future Scope

Several directions for further work emerge naturally from the results presented here.

Technology scaling: Running the same cell design at 45nm or 28nm GPDK would reveal whether the structural benefits translate across technology nodes, and whether the body effect in the read buffer requires re-sizing at smaller geometries. FinFET-based implementations at 16nm or 7nm would be particularly interesting, since FinFETs have different body effect characteristics than planar bulk CMOS, which could affect the sizing strategy for the read buffer.

PVT variation analysis: The present work characterizes the cell at a single process corner (TT), temperature (27°C), and nominal V_{DD}.A complete PVT analysis across SS, TT and FF corners, temperatures from 40∘C to 125∘C and supply voltages from 0.8 VDD to 1.2 VDD would characterize the variability of each metric and would identify

whether the cell remains superior to the ST10T over the entire operating envelope. Monte Carlo analysis over 1000 or more samples would also characterize the statistical distribution of each metric under local process variation.

Array-level simulation: Single-cell simulations do not capture all array-level

effects such as half-select disturb, bitline coupling noise and the effect of column-shared sense amplifier offsets. A more realistic assessment of achievable read and write margins in a production context would be to simulate the proposed 13T cell in a representative array (e.g., 128 rows x 32 columns) with appropriate wire RC models.

Supply voltage scaling: Characterization of a minimum operating voltage (VMIN) – the lowest VDD at which the cell can reliably write and read – would be useful for applications that adopt aggressive voltage scaling for energy reduction. Considering the strong RSNM and the hold-equivalent read margin of the proposed cell, it is likely that VMIN is lower than the ST10T reference, but it needs to be verified experimentally .

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