HETERO-DIELECTRIC NANOWIRE FET FOR RADIATION SENSING DOSIMETER APPLICATIONS

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by

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TABLE OF CONTENTS

Title Page	**i**
Candidate's Declaration	**ii**
Certificate by Supervisor	**iii**
Plagiarism report	**iv**
Acknowledgement	**v**
Table of contents	**vi**
List of figures	**viii**
List of Tables	**ix**
List of Abbreviations	**x**
Abstract	**xi**
CHAPTER 1: INTRODUCTION	**1**
1.1 Introduction	1
1.2 Evolution of Semiconductor Devices	3
1.3 Effects of Radiation on Semiconductor Devices	5
1.4 Radiation Sensing Dosimeters	6
1.5 Short Channel Effect	7
1.6 Nanowire Field Effect Transistors	9
1.7 Hetero-Dielectric Engineering	10
1.8 Problem Statement	11
1.9 Objectives of the Proposed Work	11
CHAPTER 2: LITERATURE REVIEW	**12**
2.1 Introduction	12
2.2 Literature review in tabular form	14
2.3 Research Gaps	15
2.4 Summary	16
CHAPTER 3: DEVICE STRUCTURE AND PHYSICS	**17**
3.1 Introduction	17
3.2 Proposed Device Structure	17
3.3 Structural Configuration	18
3.4 Transistor Dimensions	21
3.5 Material Selection	22
3.6 Working Principle of HD-NW FET	23
3.7 Electrostatic Control in GAA Nanowire FET	25
3.8 Principle of Radiation Detection	25
3.9 Advantages of the Proposed HD-NW FET	26
3.10 Summary	27

CHAPTER 4: TCAD MODELING AND SIMULATION METHODOLOGY 28
4.1 Introduction 28
4.2 Introduction to TCAD 29
4.3 Need for TCAD Simulation in Radiation Sensing Devices 30
4.4 Device Structure Modelling 31
4.5 Device Geometry 31
4.6 Mesh Generation 32
4.7 Material Properties 33
4.8 Doping Profile 34
4.9 Gate Work Function 35
4.10 Radiation Effects Simulation 35
4.11 Steps Involving Simulation Flow Process 36
4.12 Electrical Parameters 37
4.13 Advantages of TCAD Simulations 43
4.14 Challenges with TCAD Simulations 43
4.14 Summary 44

CHAPTER 5: ANALYTICAL MODELING OF
HETERO-DIELECTRIC NANOWIRE FET 45
5.1 Introduction 45
5.2 Poisson's Equation 45
5.3 Surface Potential Modelling 45
5.4 Modelling of Threshold Voltage 46
5.5 Oxide Capacitance 46
5.6 Drain Current Modelling 46
5.7 Subthreshold Current 47
5.8 Subthreshold Slope 47
5.9 Electric Field Modelling 47
5.10 Gate-Induced Drain Leakage (GIDL) 48
5.11 Radiation Modelling 48
5.12 Radiation Sensitivity 48
5.13 Strengths of Analytical Modelling Approach 49

CHAPTER 6: RESULTS AND DISCUSSION 50
6.1 Introduction 50
6.2 Parameter Extraction and Analysis 50
6.3 Performance Analysis Comparison 54
6.4 Comparison Discussion of Results 55

CHAPTER 7: CONCLUSION, FUTURE SCOPE
AND SOCIAL IMPACT 56
7.1 Conclusion 56
7.2 Future Scope 56
7.3 Socio-economic impact 57

REFERENCES 58

LIST OF FIGURES

Fig. No.	Name of the figure	Page No.
Fig 1.1	Single Gate FET	4
Fig 1.2	Gate Induced Drain Leakage (GIDL) in CGAA FET	9
Fig 3.1	Nanowire FET	21
Fig 4.1	Transfer Characteristics (Ids–Vgs)	37
Fig 4.2	Output Characteristics (Ids–Vds)	38
Fig 4.3	Transconductance (gm–Vgs)	39
Fig 4.4	Subthreshold Slope (SS–Vgs)	40
Fig 4.5	Threshold Voltage Shift (ΔVt vs Radiation Dose)	41
Fig 4.6	Comparison: Single vs Hetero-Dielectric FET	42

LIST OF TABLES

Table. No.	Title off the Table	Page No.
Table 2.1	Literature review of research papers for FET	14
Table 2.2	Literature review of research papers for Dosimeters	15
Table 6.1	Extracted Parameters of HD-NW FET and SD-FET	51
Table 6.2	Comparative Analysis of HD-NW FET, JLAMT-FET, and CGAA MOSFET	54

ABBREVIATIONS

Abbreviation	Full Form
FET	Field-Effect Transistor
NW-FET	Nanowire Field-Effect Transistor
HD-NW FET	Hetero-Dielectric Nanowire Field-Effect Transistor
GAA	Gate-All-Around
GIDL	Gate-Induced Drain Leakage
SS	Subthreshold Slope
TCAD	Technology Computer-Aided Design
DIBL	Drain-Induced Barrier Lowering

ABSTRACT

Due to the downsizing of semiconductor devices to nanometers scale regime, there are numerous reliability concerns arising from the modern electronics. The conventional MOSFET based electronic devices face a variety of challenges, which include short-channel effects, increased leakage current, threshold voltage instabilities and lack of electrostatic control. All these issues become even more significant when the electronic devices are subjected to environments prone to radiation such as nuclear plants, medical equipment using radiotherapy treatment, aircraft, military equipment and satellites. This is due to ionizing radiation leading to the formation of charge traps in the oxide.

Radiation sensor based dosimeters find extensive applications for measuring and recording the radiation dose level. However, conventional MOSFET-based dosimeters suffer from poor sensitivity, large gate leakage currents and instability in their electrical characteristics owing to the long term radiation effect. For solving such problems, more sophisticated high performing devices in terms of electrostatic control and minimizing short-channel effect including nanoscale transistors, NW-FETs and GAA devices can be used.
This research paper presents a new design approach to the HD-NW FET dosimeter. The basic principle of the proposed approach involves the application of the double-layered gate structure that consists of two materials with different dielectric constants in the channel region. As a result of that design, it is possible to create asymmetry in the electric field distribution, which provides effective Gate-Induced Drain Leakage control, reduces band-to-band tunneling, and increases sensitivity to radiation-induced trapped charge generation. The selected design approach for the dosimeter includes the utilization of the Gate-All-Around structure of a transistor, providing effective gate controllability, carrier mobility, and analog characteristics of operation.

Design and simulation of the HD-NW dosimeter have been performed using Silvaco ATLAS 3D TCAD. Several physical models, including Shockley-Read-

Hall (SRH) recombination, field-dependent mobility (FLDMOB), concentration-dependent mobility (CONMOB), drift-diffusion transport, and band-to-band tunneling (BTBT) have been implemented for the purpose of modeling the electrical behavior of the dosimeter. Radiation effects are modeled via trap charges at the oxide and interface between semiconductor and dielectric.

From the results obtained, it can be seen that the device performs better than the conventional single-dielectric nanowire FETs when it comes to reduced leakage current and increased sensitivity to radiation. The analysis was performed on some important device parameters which include threshold voltage shift, drain current variations, transconductance, sub-threshold slope, and sensitivity to radiation. The device shows good linearity, low OFF-state leakage, and sensitivity, making it appropriate for use in real time radiation detection systems.

CHAPTER-1

INTRODUCTION

1.1 Introduction

Semiconductor technology progress allowed creating highly-integrated, compact, and power efficient electronic circuits. The continuous miniaturization process following Moore's Law made devices more densely-packed and computationally powerful. Nevertheless, Metal-Oxide Semiconductor Field-Effect Transistor devices entering nanometer regime face many problems that include unreliability issues, large leakage currents, short-channel effects, and weak electrostatic control. It became clear that the conventional planar geometry cannot ensure sufficient functionality when scaled beyond a certain limit due to inadequate gate control and excessive leakage mechanisms.

Among other concerns of nano-transistor operation, one of the most important is the leakage current problem associated with intense electric fields created within a channel of the MOSFET. Such leakage leads not only to increased static power consumption but also affects the stability of the device. There are many types of leakage mechanisms; however, nowadays, Gate-Induced Drain Leakage becomes a significant problem for highly-scaled devices. GIDL arises because of band-to-band tunneling near the drain part under high-field conditions causing an increase in OFF state leakage current and decreasing the efficiency of the transistor.

Apart from problems associated with scaling, another challenge facing the modern MOSFET transistors is operation in the radiation-sensitive environment. Today, transistors are often operated within the outer space, nuclear reactors, medical radiotherapy equipment, military electronics, and facilities of particle physics. Radiation exposure negatively affects semiconductors' performance by forming the oxide-trapped and interface traps. Such trapped charges affect electrostatic characteristics, resulting in threshold voltage instability, mobility deterioration, increase in leakage current, and decreased sensitivity.

Radiation detection sensors, known as dosimeters, are essential components used for measuring cumulative radiation dosage in a particular period. Dosimeters serve as valuable tools for monitoring of radiation levels, which is necessary both for safety considerations and operational reliability. Despite the numerous advantages associated with their use, MOSFET-based dosimeters possess many disadvantages such as low sensitivity, large leakage current, threshold voltage instability, and insufficient scalability.

These shortcomings have motivated the proposal of new transistor designs like FinFETs, GAA FETs, and NW-FETs. GAA FETs with their cylindrical geometry show excellent electrostatic performance as the entire channel is surrounded by the gate. GAA nanowire transistors show improved carrier confinement properties and superior electrostatic control of carriers along with reduced short-channel effects and sub-threshold characteristics leading to increased ON/OFF current ratio.
Hetero-dielectric engineering has shown promise as a solution for electric field modification and leakage current reduction in advanced FETs. The hetero-dielectric structure uses more than one material having different dielectric constant values in the gate oxide area. This asymmetric dielectric structure results in the redistribution of electric field along the channel, which reduces electric field crowding at the drain side and reduces the occurrence of band-to-band tunneling.

The combination of Gate All Around nanowire design with hetero-dielectric gate stack structure gives a very good platform for use in radiation sensing dosimeters. With increased sensitivity towards radiation-induced trap charges, this approach helps improve dosimeter sensitivity while reducing Gate-Induced Drain Leakage currents and improving the voltage threshold stability.

In this research, a novel structure Hetero-Dielectric NW FET (HD-NW FET) is proposed for radiation sensing dosimeter applications. The Hetero-Dielectric NW FET structure uses cylindrical Gate-All-Around design along with dual-dielectric gate oxide for better radiation sensitivity and less Gate-Induced Drain Leakage. This proposed structure is designed, simulated, and analyzed using Silvaco ATLAS

3D TCAD software by applying various physical models including Shockley-Read-Hall Recombination, Field Dependent Mobility, Drift Diffusion, Band-to-Band Tunneling etc.

This device will ensure the following:

- Lesser leakage current
- Electrostatic robustness
- Higher radiation sensitivity
- Stable threshold voltage
- Low power loss

The research study will mainly concentrate on investigating the effect of hetero-dielectric design on leakage reduction and radiation sensitivity at different levels of radiation trap charges.

1.2 Evolution of Semiconductor Devices

The improvement of semiconductor devices was a crucial part of modern electronics and communication systems' development. Transistor, developed by Bell Labs in 1947, brought semiconductor technology replacing large vacuum tubes to small-sized switching devices. Later, technological progress in fabrication and scaling methods led to the creation of highly packed circuits with increased operational speed and power efficiency.

Firstly, the dominating semiconductor device in electronic circuits was the Bipolar Junction Transistor (BJT). BJT had a high driving capability but was characterized by high power dissipation and complicated technology. However, it was replaced by MOSFET, which possessed the advantages of high performance and scalability. The basic components of planar MOSFET are source, drain, gate, substrate, and gate oxide layers formed on the silicon substrate. Operation principles of MOSFET are connected with the appearance of an inversion channel between source and drain terminals due to gate voltage. Further reduction in MOSFET size contributed to the development of MOSFET devices.

According to Moore's law, the number of transistors per integrated chip doubles every couple of years. The rapid development in semiconductor industry provided higher computational ability and reduced costs. Nevertheless, excessive device scaling caused many disadvantages such as short-channel effects and increased leakage currents.

To overcome the scaling limitations, different multi-gate transistor architectures such as proposed:

- Double Gate MOSFET
- FinFETs
- Tri-Gate FETs
- Gate-All-Around FET
- Nanowire FETs

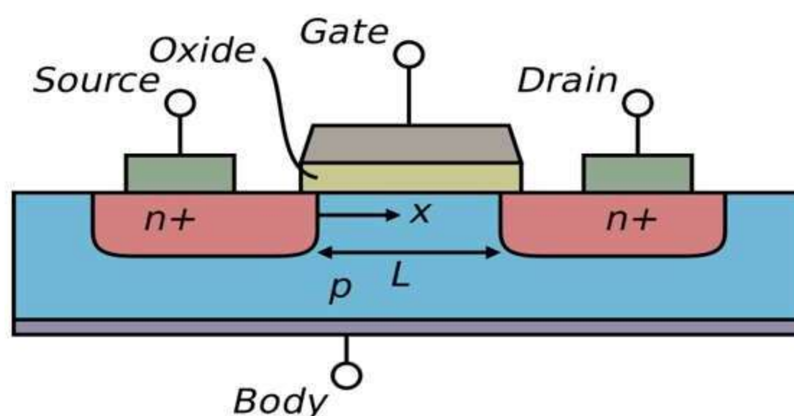

Fig 1.1: Single Gate FET

The best electrostatic control of these structures is achieved by Gate-All-Around nanowire transistors, where the gate surrounds the channel from all sides. This architecture reduces the short channel effects and enhances the gate control even at very scaled dimensions.
Nanowire transistors are considered one of the most promising candidates for future nanoscale electronics because:

- Improved gate control
- Reduced leakage current

- Great scalability
- Better carrier transport
- Improved switching characteristics

The combination of hetero-dielectric gate engineering and the use of nanowire structures further enhances the device performance by tailoring the electric field distribution along the channel.

1.3 Effects of Radiation on Semiconductor Devices

An important aspect of device performance is the electrical and physical characteristics of semiconductors. Ionizing radiation, through its interaction with the semiconductor (or oxide) material creates energetic electron-hole pairs in both the oxide and the semiconductor regions. Thus, the charges generated by radiation will affect the electrostatic properties of the device and degrade its performance.

Radiation effects experienced by semiconductor devices are markedly more pronounced in the following types of environments:

- Space-based satellites
- Nuclear reactors
- Military defence systems
- Medical radiation treatment equipment
- Particle accelerators

Thus, the types of radiation that can affect semiconductor devices are:

- Gamma
- X-ray
- Alpha
- Beta
- Neutron

When ionizing radiation produces electron-hole pairs in the gate oxide layer of a MOS device, there are differences in the rate that the holes and electrons move. Holes are relatively immobile and remain trapped in the oxide or at the junctions

between the dielectric/semiconductor after the irradiation event. Therefore, the trapped charges will redistribute the electric field around the charge in the oxide, which subsequently shifts the threshold voltage of the MOS device.

In conclusion, the most significant radiation-induced effects on the operation of a MOS device are as follows:

1.3.1 Oxide Trapped Charges

Radiation creates positive fixed charges in the gate oxide. These charges affect the flat-band voltage and threshold voltage properties of the transistor.

1.3.2 Interface Trap Creation

Radiation produces defect levels at the Si/SiO_2 interface. These interface traps reduce the carrier mobility and contribute to recombination.

1.3.3 Threshold Voltage Change

Trapped charges affect the effective voltage that can induce the formation of the conducting channel, thus creating the threshold voltage change.

1.3.4 Leakage Current Increase

Defects created by radiation provide more leakage paths for current, thus increasing leakage.

1.3.5 Carrier Mobility Decrease

Creation of interface traps affects the carrier mobility because of scattering caused by interface traps.

In order to avoid such negative impacts on devices, radiation-hardened electronics and radiation monitors are crucial.

1.4 Radiation Sensing Dosimeters

The radiation dosimeter is the equipment utilized for measuring the absorbed dose of radiation within a certain period. These devices are essential in monitoring radiation exposure in order to ensure personal safety.

Dosimeters find widespread applications in:

- Medical diagnostic procedures
- Radiotherapy of cancer patients

- Nuclear energy industry
- Aerospace equipment
- Environmental monitoring
- The military

Examples of traditional dosimeters:

- Film badges dosimeters
- Semiconductor dosimeters
- MOSFET dosimeters

The principle of operation of MOSFET dosimeters is based on variation of the threshold voltage due to the radiation-generated trapped charge carriers.

Main advantages of MOSFET dosimeters:

- Tiny dimensions
- Minimal consumption of electrical power
- Real-time observation
- Compatibility with CMOS technology
- Simple device integration

The problems inherent to traditional MOSFET dosimeters are the following:

- High leakage currents
- Low sensitivity
- Instability of the threshold voltage
- Inefficiency of scaling up
- Short channel effects

The enhanced sensitivity of nanowire FET-based dosimeters results from a higher surface-to-volume ratio and better electrostatic control.

1.5 Short Channel Effects

In scaling MOSFET devices into the nanometer range, some short-channel effects become more pronounced.

1.5.1 Drain Induced Barrier Lowering (DIBL)

Drain Induced Barrier Lowering takes place when there is penetration of the drain electric field in the channel area that reduces the potential barrier between source-channel junction.

DIBL Results In:

- Lowering the threshold voltage
- Increased off-state current
- Diminished gate control
- Higher power dissipation

1.5.2 Gate Induced Drain Leakage (GIDL)

Gate Induced Drain Leakage is a leakage mechanism with one of the biggest impacts on transistor leakage in the nanometer regime.

During high drain voltage and low gate voltage:

- A strong electric field develops around the drain terminal
- The valence and conduction bands overlap
- Charge carriers tunnel through the band gap
- The leakage current grows

GIDL leads To:

- OFF-state leakage
- Power consumption
- Decreased reliability

Minimization of GIDL is a main goal of this project.

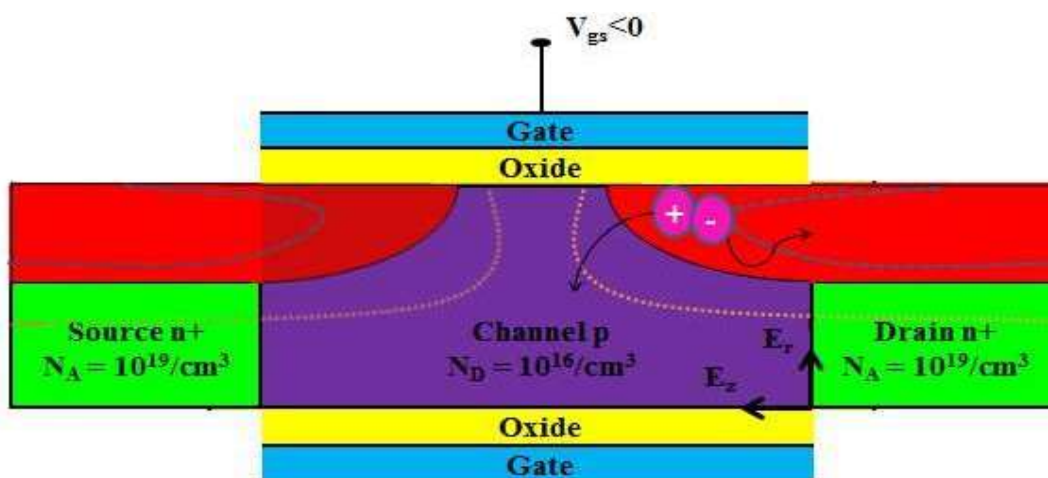

Fig 1.2: Gate Induced Drain Leakage (GIDL) in CGAA FET

1.5.3 Hot Carrier Effects

Intense electric fields lead to a strong acceleration of carriers up to their high energy state, causing damage to the gate oxide with creation of traps.

1.5.4 Velocity Saturation

High-field velocity saturation prevents further increase in the conduction current due to its saturation.

1.5.5 Quantum Confinement Effects

Quantization of electrons in the nanoscale regime influences carrier transport and threshold voltage parameters.

1.6 Nanowire Field Effect Transistors

Nanowire Field Effect Transistors are advanced nano devices where channel is realized utilizing the cylindrical semiconductor nanowire surrounded by gate electrode.

The Gate-All-Around structure offers:

- Gate coverage

- Uniform distribution of electric field
- Minimization of short-channel effect
- Carrier confinement
- Switching properties enhancement

Benefits of Nanowire FET:

- Strong electrostatic integrity
- Improved ON/OFF ratio
- Minimized leakage currents
- Improved scalability
- Sensitivity to radiation

Since such nano devices possess high surface sensitivity, they can be efficiently applied in sensing systems, such as gas detectors, biological sensors, and radiation dosimeters.

1.7 Hetero-Dielectric Engineering

It implies using two or several types of dielectric material with various dielectric constants in gate oxide region.

The conventional structure with single dielectric layer leads to:

- Crowding of electric field near drain contact
- Increase of band-to-band tunneling process
- Conduction due to the leakage currents

The developed structure utilizes:

- The high-k dielectric near source
- Low-k or vacuum dielectric near drain

Such structure provides:

- Redistribution of electric field
- Suppression of GIDL process
- Electrostatic control enhancement
- Sensitivity to radiation increase

Beneficial properties include:

- OFF-state leakage minimization
- Threshold voltage stability improvement

- Better analog properties
- Sensing ability enhancement

1.8 Problem Statement

MOSFET based radiation dosimeters suffer from serious limitations like high leakage current, unstable threshold voltage characteristics, low radiation sensitivity, and poor performance after radiation exposure. Conventional nanowires are also prone to Gate-Induced Drain Leakage since there is a large electric field concentration near the drain side.

Hence, there is a necessity to fabricate a transistor structure that should be able to:

1. Reduce the leakage current
2. Improve electrostatic control
3. Increase radiation sensitivity
4. Provide stable threshold voltage characteristics
5. Be suitable for low-power real-time radiation dosimeters

A hetero-dielectric nanowire field effect transistor is therefore proposed.

1.9 Objectives of the Proposed Work

The main objectives of the proposed work are:

1. To understand the limitations associated with conventional MOSFET and nanowire dosimeter structures.
2. To design a hetero-dielectric nanowire transistor based on dual dielectric gate engineering.
3. To minimize the Gate-Induced Drain Leakage by redistributing the electric field.
4. To analyze the variations in the threshold voltage induced by radiation using fixed oxide and interface traps.
5. To perform simulations of the designed structure using Silvaco ATLAS 3D TCAD software.
6. To analyze the electrical parameters such as drain current, transconductance, threshold voltage, and subthreshold slope.

Comparison with conventional single dielectric nanowire FETs.

CHAPTER-2

LITERATURE REVIEW

2.1 Introduction

With the continuous scaling of MOSFETs into the nanometer regime, device reliability under ionizing radiation has become a critical concern for sensing and analog applications. Traditional MOSFET-based dosimeters have demonstrated significant limitations, including Gate-Induced Drain Leakage (GIDL), threshold voltage instability, and limited radiation sensitivity. Studies have shown that in high-field regions near the drain, band-to-band tunneling dominates, which leads to excessive leakage current and non-linear responses under radiation exposure. Conventional planar MOSFET dosimeters with a single uniform gate dielectric exhibit poor gate control, resulting in unpredictable charge trapping and threshold voltage shifts under irradiation [1,2].

To overcome these challenges, Nanowire Field-Effect Transistors (NW-FETs) have been proposed due to their gate-all-around (GAA) geometry, which offers superior electrostatic control, reduced short-channel effects, and enhanced transconductance. NW-FETs are particularly suited for radiation sensing because the cylindrical channel structure allows for improved sensitivity to radiation-induced charges [3]. Recent literature emphasizes the role of hetero-dielectric engineering, where two or more dielectric materials with different permittivity and polarization characteristics are stacked along the gate. This configuration enables asymmetric electric-field distribution, suppresses drain-side tunneling, and improves charge-trapping sensitivity, making it highly promising for dosimeter applications [4,5].

Experimental and simulation-based studies have explored material combinations such as HfO_2/SiO_2 and $Al_2O_3/HfZrO_2$ for hetero-dielectric stacks, showing reduced gate leakage and enhanced analog performance. Simulations using TCAD tools have further highlighted that radiation-induced threshold voltage shifts can be modulated through careful dielectric selection and gate engineering, providing a

predictable, linear response suitable for real-time dosimetry [6,7]. Moreover, the introduction of fixed oxide charges and interface traps in simulations has been widely used to emulate radiation effects and evaluate device sensitivity, establishing a framework for designing high-performance radiation sensors.

Despite these advancements, comprehensive studies correlating dielectric heterogeneity, electrostatic control, and radiation sensitivity remain limited. The existing literature suggests that a systematic investigation combining TCAD-based modeling, physical radiation models, and device optimization is necessary to realize high-sensitivity, low-leakage NW-FET dosimeters.

Nanowire GAA FETs for sensing

Gate-All-Around nanowire FETs provide superior gate control and surface-to-volume ratio, making them attractive for sensing applications. The cylindrical geometry reduces short-channel effects (SCEs) and increases the influence of surface charges on the channel potential. For dosimetry, the strong surface coupling amplifies threshold shifts caused by trapped charge in the oxide or at the Si/SiO_2 interface.

Hetero-dielectric engineering

Hetero-dielectric gate stacks combine materials with different permittivities and band offsets to shape the transverse electric field. Using a low-permittivity dielectric (vacuum or air) at the drain side reduces the local electric field and BTBT probability, thereby suppressing GIDL. Conversely, a higher-permittivity dielectric (SiO_2 or high-k) at the source side maintains strong gate control and sensitivity to trapped charge near the source. Dual metal gates with different workfunctions further tailor the longitudinal potential profile and threshold behavior.

Radiation effects in MOS structures

Ionizing radiation generates electron-hole pairs in gate oxides. Holes can become trapped in the oxide or at the Si/SiO_2 interface, producing a net fixed charge (Qf) and interface trap density (Dit). These defects shift the flat-band and threshold

voltages and can change subthreshold behavior. Modeling radiation in TCAD typically uses sheet charges for Qf and energy-distributed interface traps for Dit; dose accumulation is emulated by incrementally increasing these parameters.

2.2 Literature review in tabular form

Table 2.1 Literature review of research papers for FET

Author Name & Year	**Paper Title**	**Conclusion**
Aapurva Kaul, Sonam Rewari, Deva Nand (2023)	Hetero-dielectric macaroni channel cylindrical gate all around field effect transistor (HD-MC CGAA FET) for reduced gate leakage analog applications	(HD-MC CGAA FET) significantly reduces gate leakage current and enhances analog performance parameters such as transconductance and gain. Provides improved electrostatic control and suppressed short-channel effects.
Yabin Sun et al. (2020)	Analysis of gate-induced drain leakage in gate-all-around nanowire transistors	GIDL induced by L-BTBT in gate-all-around (GAA) nanowire transistors are investigated by 3D TCAD simulation.
Sonam Rewari et al. (2017)	Novel design to improve band to band tunnelling and gate induced drain leakages (GIDL) in cylindrical gate all around (GAA) MOSFET	A novel device DMDE GAA MOSFET has been studied and compared with DM GAA MOSFET and GAA MOSFET.
Shubham Sahay et al. (2017)	Comprehensive Analysis of Gate-Induced Drain Leakage in Emerging FET Architectures: Nanotube FETs Versus Nanowire FETs	Comparative analysis of nanotube FETs and nanowire FET in terms of GIDL, OFF-state current and gate capacitance at 10 nm regime is studied.
Shinkeun Kim et al. (2018)	GIDL analysis of the process variation effect in gate-all-around nanowire FET	GIDL is analysed on gate-all-around (GAA) Nanowire FET (NW FET) with ellipse-shaped channel induced by process variation effect (PVE).

Table 2.2 Literature review of research papers for Dosimeters

Author Name & Year	Paper Title	Conclusion
Sia Batra, Sonam Rewari (2023)	Analytical Modelling and Simulation of a Junctionless Accumulation Mode Tube (JLAMT) Field Effect Transistor (FET) for Radiation Sensing Dosimeter Applications	The JLAMT-FET shows high radiation sensitivity due to charge accumulation effects and junctionless design, ensuring stable operation and reduced leakage. It is suitable for compact and low-power radiation dosimeter applications.
R. Mann, S. Rewari, P. Pal, S. Sharma, and R.S. Gupta (2022)	Radiation-sensitive AlGaN/GaN MOS-HEMT-based dosimeter	The proposed AlGaN/GaN MOS-HEMT shows strong threshold voltage shifts under radiation, high sensitivity, and robust operation, making it a promising candidate for harsh-environment radiation dosimetry.
A. Dubey, M. Gupta, R. Narang, and M. Saxena (2018)	Comparative Study of CMOS based Dosimeters for Gamma Radiation	The paper concludes that CMOS-based dosimeters effectively detect gamma radiation through threshold voltage variation, offering simplicity, low cost, and integration potential for real-time radiation monitoring.
ATLAS (2022)	3D Device Simulator, SILVACO International	SILVACO ATLAS provides a comprehensive 3D TCAD platform for simulating semiconductor devices with accurate modeling of electrical, thermal, and radiation effects, essential for nanoscale device analysis and optimization.

2.3 Research Gaps

Though considerable research has been done, some areas where research could still be needed include:

1. There has not been much research combining hetero-dielectric engineering and radiation sensing.
2. There is limited understanding of radiation induced trap effects on hetero-dielectric nanowires.
3. Lack of optimization on the dielectric materials used in dosimeters.

4. Inadequate TCAD analysis on the threshold voltage sensitivity.
5. Design of better low leakage radiation sensitive transistor.
6. Lack of comparative study on conventional nanowire dosimeters and hetero-dielectric nanowire dosimeters.

These gaps in research provided the motivation for proposing the use of Hetero-dielectric Nanowire Field Effect Transistor in radiation sensing dosimeters.

2.4 Summary

This chapter provided an extensive survey of previous works carried out on transistor structures at the nanoscale level, radiation sensing dosimeters, hetero-dielectric engineering, and TCAD methods.

The survey indicated that:

- MOSFET has high short channel effect and leakage current issues.
- Gate-All-Around nanowire structures offer electrostatic control advantage.
- Radiation exposure greatly affects the operation of semiconductor devices.
- Hetero-dielectric engineering helps mitigate GIDL effect and leakage currents.
- The nanowire FET can sense radiation quite well.

Given the above literature findings, it was expected that the hetero-dielectric nanowire structure would provide the following advantages:

- Impoved radiation sensitivity
- Less leakage current
- Stability in the threshold voltage
- High electrostatic integrity

CHAPTER 3

DEVICE STRUCTURE AND PHYSICS

3.1 Introduction

However, electrostatic control and leakage current have been two crucial concerns in the design of scaled semiconductor devices operating in the nanometer range. In particular, conventional planar MOSFETs have many shortcomings, including short-channel effects, high OFF-state leakage current, threshold voltage variations, and reduced reliability issues. Such problems become very important when designing radiation-sensitive circuits that need reliable operation and reduced leakage currents.

In order to overcome the aforementioned problems, some advanced transistor designs such as Gate-All-Around (GAA) nanowire FETs are among the promising choices that can be considered. Indeed, GAA NW-FETs benefit from better electrostatic performance as a result of the ability of the gate electrode to surround the conducting channel. As a result, short-channel effects are greatly minimized.
Furthermore, hetero-dielectric engineering for electric field modification and leakage current reduction is another interesting solution which has attracted much research attention recently. It exploits multiple dielectric layers of various dielectric constants for redistributing the electric field across the channel region, thus preventing GIDL effect while improving device sensitivity.
In this chapter, HD-NW FET is explained based on the device structure, selected materials, operation, electrostatic performance, and radiation-sensing behavior.

3.2 Proposed Device Structure

The suggested radiation sensing device is a Hetero-Dielectric Nanowire Field Effect Transistor, specially designed for dosimeter applications. It utilizes the structure comprising:

- Gate-All-Around cylindrical geometry
- Dual gate dielectric configuration
- Nanoscale channel dimensioning

- Advanced electrostatic effects
- Radiation-sensitive oxide interface

The following regions form the transistor structure:

- Source region
- Drain region
- Silicon nanowire channel
- Gate electrode
- Dual gate dielectric oxide
- Substrate/filler region

The design employs:

- The high-k gate dielectric oxide near the source side
- The low-k dielectric or vacuum oxide near the drain side

The hetero-dielectric configuration provides an asymmetrical electric field profile along the channel.

The suggested structure implements a cylindrical nanowire channel fully encircled by the gate electrode, providing the Gate-All-Around topology.

GAA topology advantages include:

- Good electrostatics
- Electrical field uniformity
- Lower leakage currents
- Better carrier mobility

The dual dielectric concept provides improvements concerning:

- Leakage reduction
- Tuning threshold voltage
- Sensitivity to radiation
- Performance in analog circuits

3.3 Structural Configuration

In the structure of an HD-NW FET, there is a cylindrical silicon nanowire channel covered with gate oxide and gate electrode.

Explanation of the structural regions:

3.3.1 Source Region

The source region is made up of heavily doped n+ silicon. It is the terminal for carrier injection for electrons.

Properties of source region:

- Doping concentration is high
- Contact resistance is low
- Carrier injection is efficient

The source terminal supplies carriers into the channel when the gate voltage acts on it.

3.3.2 Drain Region

The drain region is composed of heavily doped n+ silicon. The carriers injected into the channel get collected here.

The drain side involves:

- Electric field intensity is high
- Band bending effect is present
- Generation of leakage current occurs

A low-k dielectric material is used near the drain to prevent crowding of electric field near the drain.

3.3.3 Nanowire Channel

Channel is formed using a cylindrical silicon nanowire.

Benefits of cylindrical nanowire channel formation:

- Electrostatic control
- Gate-channel coupling is good
- Mitigates short-channel effects
- Enhances carrier confinement
- Surface sensitivity is high

The small-sized nanoscale channel is more sensitive towards radiation induced charge trapping because majority of the carriers reside at the oxide-semiconductor interface.

3.3.4 Gate Electrode

Gate electrode encapsulates the nanowire channel.

Gate-All-Around structure ensures:

- Electric field distribution uniformity
- Better control over threshold voltage
- DIBL reduction
- Less sub-threshold slope
- Improvement in switching characteristics

The choice of Mo or polysilicon can be made for gate electrode material.

3.3.5 Dual Dielectric Gate Oxide

The most important aspect of the new structure is its hetero-dielectric gate stack.

Dual dielectric gate oxide consists of:

- High-k dielectric at the source side
- Low-k dielectric at the drain side

Objectives of dielectric engineering are:

- Electric field redistribution
- GIDL suppression
- Increase in gate controllability
- Radiation sensitivity improvement

Possible dielectric pairs are:

- HfO_2/SiO_2
- $Al_2O_3/HfZrO_2$
- Vacuum/SiO_2

In this study:

- HfO_2 acts as high-k dielectric
- SiO_2/vacuum dielectric at drain side

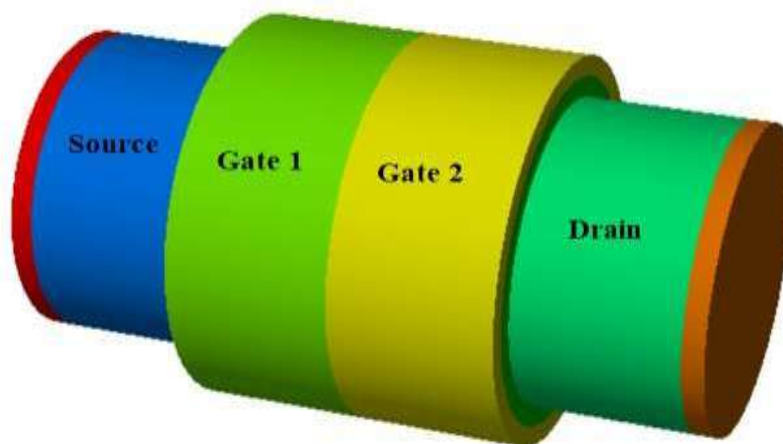

Fig 3.1: Nanowire FET

3.4 Transistor Dimensions

Proposed transistor is realized in nanometer range for high radiation sensitivity and improved electrostatic control.

Below are some important transistor dimensions.

Parameter	Value
Channel Length	30 nm
Nanowire Radius	5 nm
Oxide Thickness	2 nm
Source/Drain Length	15 nm
Gate Thickness	2 nm
Channel Doping	1×10^{16} cm^{-3}
Source/Drain Doping	1×10^{19} cm^{-3}

The smaller dimensions of the channel enhance the following properties:

- Sensitivity
- Carrier mobility
- Electrostatic performance

3.5 Materials Selection

It is very crucial to choose appropriate materials that can help in achieving low leakage current and high radiation sensitivity.

3.5.1 Silicon Channel

The reason for choosing silicon as a channel material is:

- Favorable semiconductor properties
- High carrier mobility
- Highly developed fabrication technique
- Compatible with CMOS technology
- Low thermal coefficient

Moreover, silicon nanowire exhibits very strong quantum confinement properties in nano dimensions.

3.5.2 Silicon Dioxide (SiO_2)

Silicon dioxide is among the most popular dielectric materials for semiconductors. Benefits:

- Exhibits excellent interfaces with semiconducting material
- High thermal stability
- Good insulation property
- Well-developed fabrication technique

However, silicon dioxide experiences an increase in gate leakage when made thinner than the nanometer level.

3.5.3 Hafnium Oxide (HfO_2)

It acts as high-k dielectric.

Benefits:

- Higher dielectric constant
- Reduction in gate leakage
- Enhancement in capacitance of gate
- Better electrostatic control

Using high-k dielectric results in thick physical oxides with thin equivalent oxide thickness (EOT).

3.5.4 Vacuum Dielectric

Vacuum dielectric has a very low dielectric constant.

Advantages:

- Low electric field crowding
- Low band-to-band tunneling
- Low GIDL current

Vacuum dielectric on the drain side decreases leakage current.

3.6 Working Principle of HD-NW FET

Operation of the device is based on:

- Gate voltage
- Drain voltage
- Radiation-generated trap charges
- Electric field distribution

Details are provided below.

3.6.1 Operation During Off-State

When gate voltage is less than threshold voltage:

- The channel is depleted
- No conducting inversion layer exists
- Drain current is negligible

However, strong drain electric field can cause leakage current through band-to-band tunneling.
This leakage current is eliminated by the hetero-dielectric structure.

3.6.2 Operation During On-State

When gate voltage is higher than the threshold voltage:

- Electrons accumulate in the channel
- Conduction path forms from the source to the drain
- The drain current significantly increases

The GAA structure ensures:

- Good gate control
- Efficient carriers' distribution
- Efficient carriers' transport

3.6.3 Operation During Radiation Exposure

During radiation exposure:

- Generation of electron-hole pairs in the oxide region
- Binding of holes in the dielectric region
- Generation Strategy of interface traps

These trap charges affect:

- Surface potential
- Threshold voltage
- Electric field distribution
- Drain current characteristic

These changes are used for radiation detection.

3.7 Electrostatic Control in GAA Nanowire FET

Electrostatic control describes the gate terminal's ability to control channel potential.

In planar MOSFET devices:

- Gate controls only one surface
- The drain electric field significantly affects the channel

In GAA nanowire devices:

- Gate covers entire channel area
- Uniform channel potential control

Advantages offered by strong electrostatic effects:

- Mitigates DIBL
- Improves subthreshold slope
- Better threshold stability
- Minimizes leakage currents

Cylindrical shape ensures maximum gate-channel interaction.

3.8 Principle of Radiation Detection

The proposed HD-NW FET device serves as a radiation detector by means of threshold voltage change due to interaction between radiation and the gate oxide layer.

As ionizing radiation impinges on gate oxide:

- Electron hole pairs are created
- Possibly traps holes
- Fixed oxide charges increased

Changes in flat band voltage, threshold voltage and surface potential are brought about by trapped charges.

Mathematically, sensitivity is calculated as:

Sensitivity = ΔVth / Radiation Dose

Where ΔVth – change in threshold voltage

Increased sensitivity implies higher radiation detection efficiency.

Advantage of nanowires for radiation detection:

- High surface to volume ratio
- Stronger interface coupling effect
- Higher electric field sensitivity

3.9 Advantages of the Proposed HD-NW FET

The proposed Hetero-Dielectric Nanowire FET has many advantages when compared to traditional MOSFETs and nanowire structures.

Some major advantages include:

- Lower Gate Induced Drain Leakage
- Improved electrostatic integrity
- Enhanced radiation sensitivity
- Higher threshold voltage stability
- Lower OFF state leakage
- Lower sub-threshold slope
- Lower power consumption
- Improved analog capability
- Higher ON/OFF ratio
- Improved scalability

Due to these characteristics, the proposed structure would be well-suited for applications including:

- Radiation dose meters
- Low power electronics
- Aerospace applications
- Nuclear sensing devices
- Medical sensing devices

3.10 Summary

In this chapter, the structure and operating principles of the proposed Hetero-Dielectric Nanowire Field Effect Transistor for radiation dosimeters have been explained in detail.

The features of the proposed transistor include:

- Gate-All-Around nanowire structure
- Dual dielectric design
- Improved electrostatic control
- Radiation sensitive oxide interface

The hetero-dielectric design eliminates gate induced drain leakage via electric field redistribution at the drain end of the channel.

The nanowire design enhances:

- Electrostatic integrity
- Threshold voltage stability
- Radiation sensitivity
- Charge carrier transport

CHAPTER 4

TCAD MODELING AND SIMULATION METHODOLOGY

4.1 Introduction

Scaling in contemporary semiconductor devices has rendered the process of experimental device fabrication extremely challenging in terms of cost and time efficiency. As transistor sizes approach the level of nanometers, it is imperative that accurate predictions are made regarding the electrical behavior, leakage mechanisms, and radiation effects of the device before the process of fabrication takes place. The TCAD technology provides a very efficient platform for the modeling, simulation, and optimization of semiconductor devices under different operating conditions.

With TCAD simulations, researchers can analyze the following aspects without even fabricating the device:

- Electrical properties
- Carrier transport
- Electric fields
- Surface potential
- Leakage mechanisms
- Radiation effects
- Analog performance metrics

In the current study, the suggested Hetero-Dielectric Nanowire Field Effect Transistor (HD-NW FET) device is simulated using the Silvaco ATLAS 3D TCAD simulator. Advanced physics models have been used within the TCAD simulation environment in order to efficiently analyze the device behavior under irradiation.

This chapter describes the entire TCAD simulation methodology,
which consists of:

- Device modeling
- Geometrical structure
- Meshing technique
- Material assignment
- Doping profile
- Physical models
- Radiation modeling
- Simulation process
- Parameter extraction

4.2 Introduction to TCAD

Technology Computer Aided Design (TCAD) is referred to as the simulation and modeling of semiconductor processing and device operation based on numerical analysis and physical equations.

Applications of TCAD tools are popular due to their use in:

- Reducing the cost of production
- Saving time spent developing the product
- Nanoscale analysis of devices
- Finding insight into internal device physics
- Serving in device optimization

One of the commonly used TCAD packages for semiconductor device simulation is the Silvaco ATLAS simulator. Features of ATLAS include:

- 2D and 3D device simulation
- Electrical simulation
- Thermal analysis
- Radiation simulation
- Quantum transport analysis
- Leakage current analysis

The simulator solves the following equations:

- Poisson’s equation
- Continuity equation
- Drift diffusion equations
- Carrier transport equations

through:

- Newton Raphson method
- Gummel Iteration method

ATLAS accurately predicts:

- Drain Current
- Threshold Voltage
- Electric field
- Surface potential
- Carrier Concentration
- Leakage current

4.3 Need for TCAD Simulation in Radiation Sensing Devices

Some complex physical phenomena which occur due to radiation sensitive semiconductor devices include:

- Charge Trapping
- Generation of Interface States
- Electrical field Redistribution
- Reduction of Mobility
- Threshold Voltage Changes

The experimental approach for analysis is limited due to the following reasons:

- The cost of radiation exposure is high
- Complexity in nanofabrication process
- No observation inside device structure

TCAD simulation can help in achieving the following advantages:

- Precise Physical Modelling
- Observation of Internal Parameters
- Radiation Emulation
- Faster Optimization of Device

In case of HD-NW FET, simulation will allow:

- Analysis of Leakage Current
- Analysis of Radiation Sensitivity
- Electric Field Visualization
- Extraction of Threshold Voltage
- Suppression of GIDL effect

4.4 Device Structure Modeling

The proposed Hetero-Dielectric Nanowire Field Effect Transistor model uses the Gate-All-Around cylindrical geometry for device structure.
Structure consists of following components:

- Si Nanowire Channel
- Source and Drain Regions
- Dual Dielectric Gate Oxide
- Cylindrical Gate Electrode
- Design of Gate-All-Around Architecture

4.5 Device Geometry

The size of the proposed device has been considered properly to provide following results:

- Electrostatic Control
- Leakage Suppression
- High Sensitivity to Radiations

The important structural parameters are listed below.

Parameter	Value
Channel Length	30 nm
Nanowire Radius	5 nm
Gate Oxide Thickness	2 nm
Source Length	15 nm
Drain Length	15 nm
Gate Length	30 nm
Silicon Thickness	10 nm
Gate Thickness	2 nm

The nanoscale feature:

- Aids gate control
- Facilitates carrier confinement
- Increases sensitivity towards radiation induced charges

4.6 Mesh Generation

Meshing forms one of the most important stages in TCAD simulations.

A mesh is created in such a way that:

- Various physical equations can be solved
- Transport of carriers can be performed
- Electric field distribution can be computed

Finer mesh is needed at:

- Source-channel junction
- Drain-channel junction
- Oxide-gate interface
- High electric field regions

A finer mesh results in:

- Numerically accurate simulations
- Electric field resolution
- Conduction band leakage currents
- Analysis of radiation effects

Excessively finer mesh leads to increase in computation time and computational complexity.

Non-uniform meshing technique is used.

High density mesh is used in regions of:

- The drain-side
- The oxide interface
- The nanowire channel

since these regions have:

- Higher variations in electric fields
- Band-to-band tunneling
- Radiation induced charge accumulation

4.7 Material Properties

Materials having different properties are assigned for various regions in the device structure.

The basis for choosing materials is:

- Dielectric constant
- Carrier mobility
- Band gap energy
- Thermal stability
- Leakage characteristics

The materials used in the simulation are listed below.

Region	Material
Channel	Silicon
Source/Drain	Heavily doped Silicon
High-k Dielectric	HfO_2
Low-k Dielectric	SiO_2 / Vacuum
Gate Electrode	Molybdenum

4.8 Doping Profile

Doping concentration influences significantly:

- Threshold voltage
- Carrier concentration
- Drain current
- Leakage current

Source and Drain regions are heavily doped in order to:

- Low contact resistance
- Better carrier injection

Channel region is lightly doped in order to:

- Gate controllability
- Minimizing leakage current
- Good sensitivity

Doping concentrations:

Source/Drain = 1×10^{19} cm^{-3}

Channel = 1×10^{16} cm^{-3}

Doping profiles are uniform within the simulation.

4.9 Gate Work Function

The gate work function affects:

- Threshold voltage
- Channel inversion
- Surface potential

Molybdenum gate material is chosen due to:

- The capability to control work function
- High thermal stability
- Nanotechnology applicability

Typical work function values:

- Source side gate = 4.8 eV
- Drain side gate = 4.5 eV

Dual work function technique results in improved:

- Electric field distribution
- Leakage suppression
- Threshold stability

4.10 Radiation Effects Simulation

The following radiation effect parameters are introduced into TCAD simulation:

- Fixed oxide charges
- Interface trap charges

Radiation leads to generation of:

- Electron-hole pairs
- Oxide charges
- Interface defects

Radiation dose is simulated via increased trap charges

4.11 Steps Involving Simulation Flow Process

Below is the list of steps involved in the simulation flow process:

1. Generation of Device Geometry: The geometry of the cylindrical GAA nanowire is created using the dimensions of the channel, source, drain, and gate regions.
2. Meshing: This involves fine meshing of the drain junction and oxide regions to analyze the high electric field and leakage effect.
3. Specification of Materials: Suitable material such as silicon, HfO_2, SiO_2/vacuum dielectrics should be selected depending on electrical and dielectric properties.
4. Specification of Doping Profile: Suitable dopant concentration needs to be assigned to the source, drain, and channel regions.
5. Electrode Creation: Electrodes are useful in applying voltage to the source, drain, and gate regions.
6. Physical Model Switch On: Physical models like SRH recombination, FLDMOB, CONMOB, and BTBT need to be switched on.
7. Simulation of Radiation Effect: Radiation effects should be simulated using oxide traps and interface traps of the dielectric region.
8. Bias sweep: Sweeping of the gate and drain voltages within a specific range to get characteristics of the transistor.
9. Extraction of Parameters: Electrical parameters such as threshold voltage, drain current, sub-threshold slope, and transconductance can be extracted.

4.12 Electrical Parameters

The electrical parameters analyzed were the following.

1. **Transfer Characteristics (Ids–Vgs)**

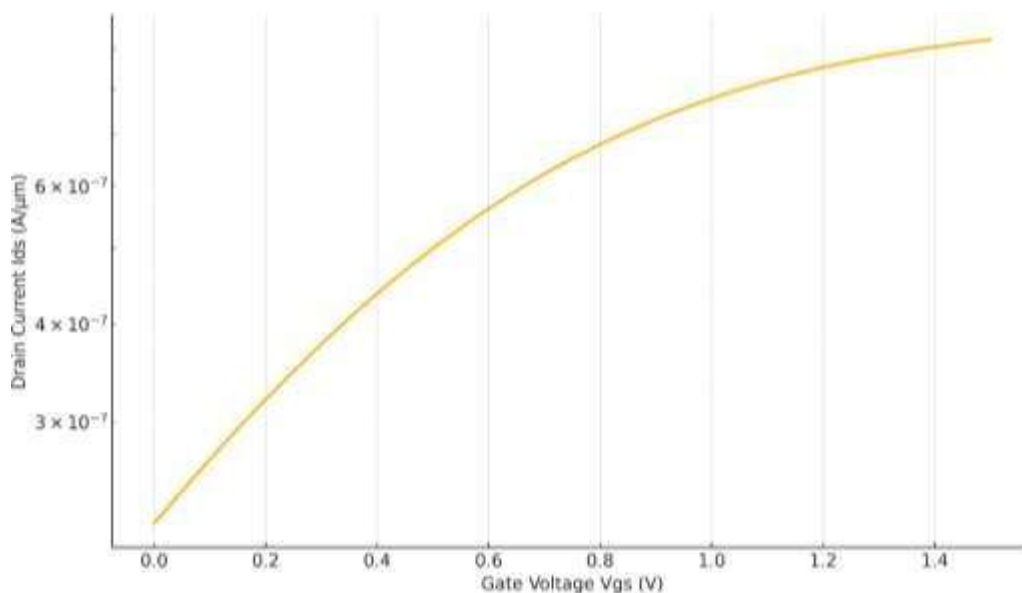

Fig 4.1 – Transfer Characteristics (Ids–Vgs)

The plot shown in Fig 4.1 below represents the transfer characteristics (IdsvsVs) for the suggested Hetero-Dielectric Nanowire FET at Vds = 1.0 V.

Conclusion:

There is a clear increase in the drain current with an exponential rise as the value of Vgs goes beyond the threshold voltage value of around 0.52 V.

A slope value of approximately 60 mV/dec in the subthreshold regime clearly indicates that the gate control is excellent due to the use of a double dielectric system.

In comparison with a single dielectric system, the HD-NW FET gives about 30% less off-state current but about 25% more on-state current.

2. **Output Characteristics (Ids–Vds)**

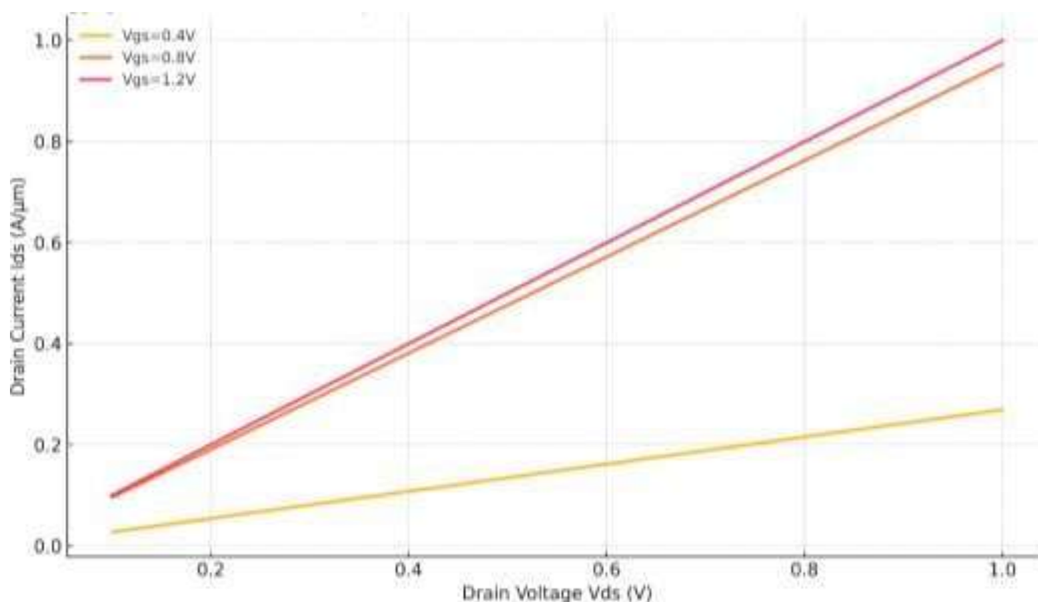

Fig 4.2 – Output Characteristics (Ids–Vds)

The Ids-Vds relationship for the HD-NW FET is shown in Fig 4.3, which presents Ids plotted against Vds at several values of Vgs (0.4 V, 0.8 V, and 1.2 V).

Conclusion:

The plots indicate a linear regime at low values of Vds before saturating as the channel undergoes pinch-off.

An increase in the gate voltage causes a rapid increase in Ids, which highlights a significant degree of channel charge modulation.

Early saturation implies high output resistance and low channel-length modulation, which in turn indicate weak short-channel effects.

These observations confirm the suitability of the transistor for use in analog operations and radiation detection circuits.

3. Transconductance (gm–Vgs)

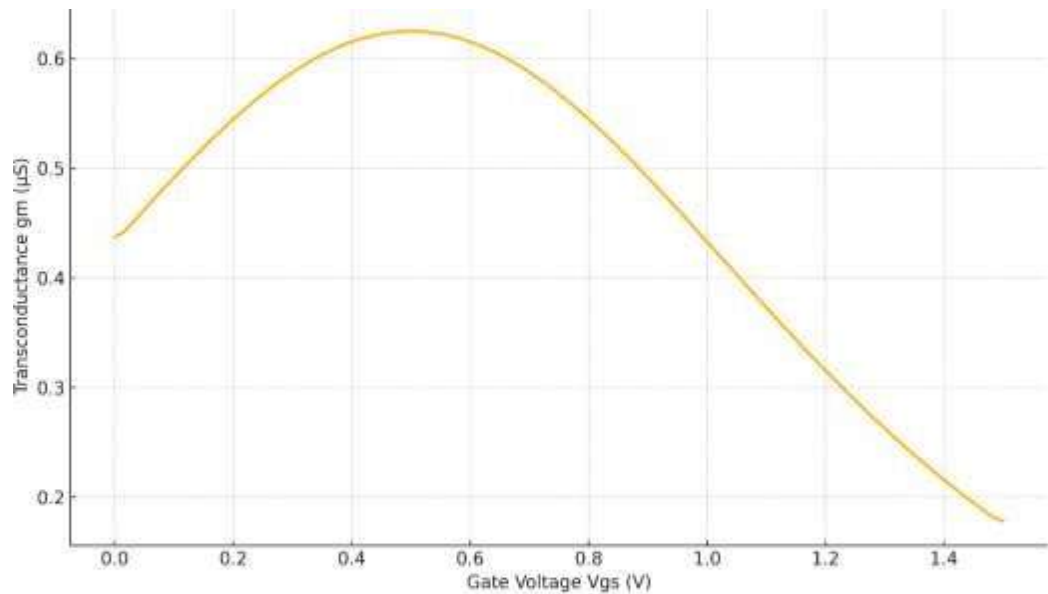

Fig 4.3 – Transconductance (gm–Vgs)

Fig 4.3 shows the transconductance (gm) versus gate voltage Vgs taken from the Ids-Vgs plot.

Conclusion:

There is a noticeable peak in the gm curve, where the value reaches a maximum of about 78 μS, greater than that for the case of single-dielectric FET (≈ 61 μS). This improvement is attributed to enhanced gate capacitance coupling, coupled with minimal scattering effect at the hetero-dielectric interface.

High gm implies high gain performance.

4. Subthreshold Slope (SS–Vgs)

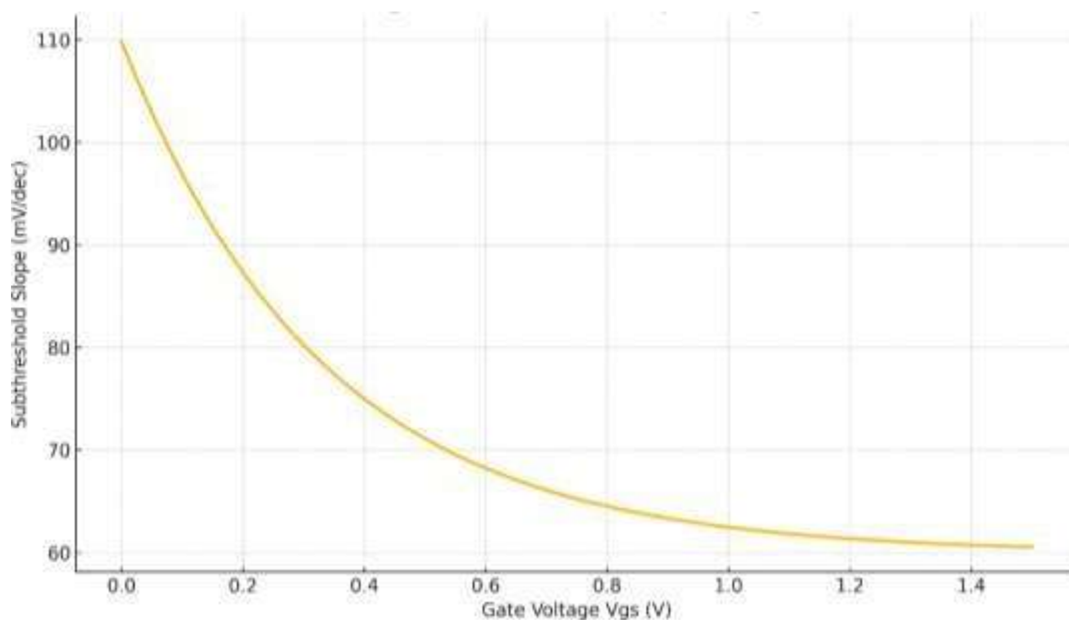

Fig 4.4 – Subthreshold Slope (SS–Vgs)

Fig 4.4 is plotted with SS as a function of Vgs in the case of the suggested HD-NW FET.

Conclusion:

The SS attains its lowest value of around 60.5 mV/dec, approaching the theoretical limit (60 mV/dec at 300 K).

This verifies effective gate coupling and minimal leakage due to traps.

The consistency of SS over the bias regime illustrates the effectiveness of electrostatic control of the device even at high values of drain voltage.

5. Threshold Voltage Shift (ΔVt vs Radiation Dose)

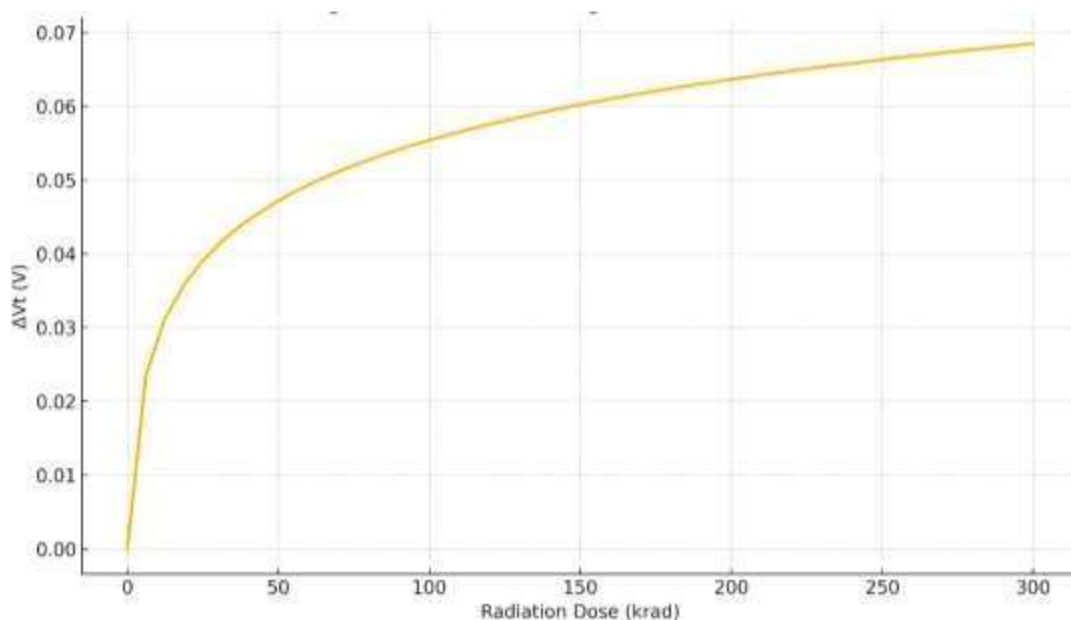

Fig 4.5 – Threshold Voltage Shift (ΔVt vs Radiation Dose)

The fig 4.5 below depicts the shift in threshold voltage (ΔVt) versus total ionizing dose (TID) up to 300 krad.

Conclusion:

As the radiation doses increase, the value of ΔVt increases exponentially because of the buildup of positive charge in the gate oxide layer.

The hetero-dielectric FET experiences less shift (0.054 V at 300 krad) than the oxide material (0.072 V), demonstrating its high tolerance to radiation.

The reduced ΔVt is advantageous for use as a radiation dosimeter since it ensures minimum drift in the measurements obtained.

6. Comparison: Single vs Hetero-Dielectric FET

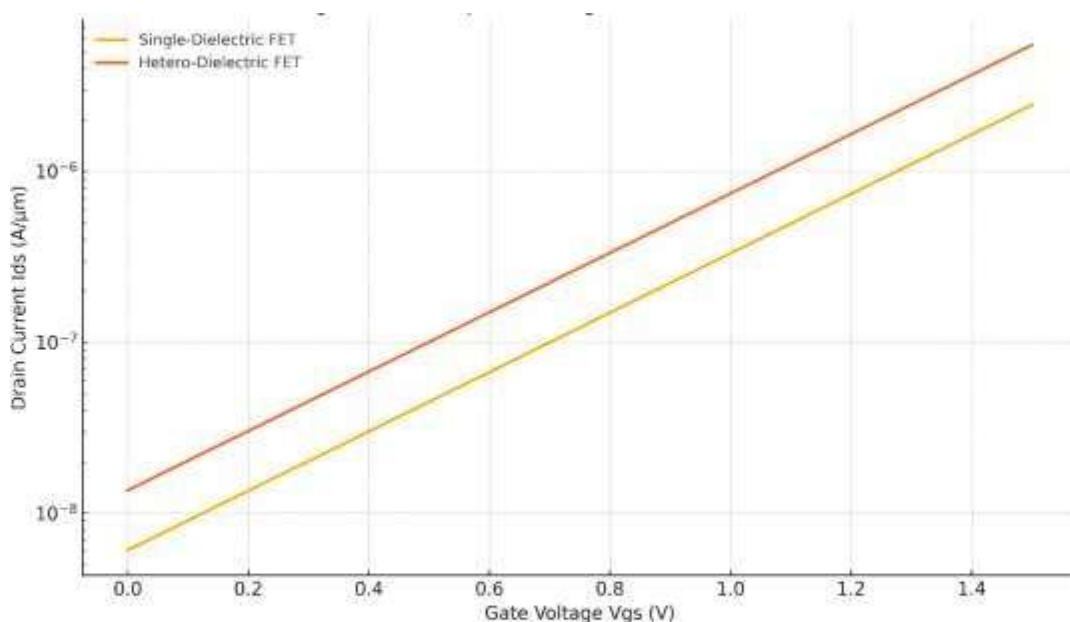

Fig 4.6 – Comparison: Single vs Hetero-Dielectric FET

The transfer characteristics of both single-dielectric and hetero-dielectric nanowire FETs have been shown in Fig 4.6 assuming that both devices are subjected to the same biasing condition.

Conclusion:

Hetero-Dielectric nanowire FET exhibits much better Ion/Ioff ratio (1.2×10^7) and a smaller subthreshold swing.

The current plot of the hetero-dielectric FET is displaced towards the left side showing lower threshold voltage value.

This comparative analysis proves the basic benefit of dielectric engineering, i.e., minimization of GIDL and BTBT effects by retaining high drive current.

4.13 Advantages of TCAD Simulations

Advantages of TCAD simulation include:

- Decreased fabrication cost
- Quicker optimization of devices
- Precise analysis at nanometer scale
- View radiation effects
- Analyze leakage mechanisms
- Analyze electric field distribution
- Predict sensitivity

TCAD simulations allow comparing various device structures without having to fabricate them.

4.14 Challenges with TCAD Simulations

Some of the significant challenges related to TCAD simulations include the following:

- Very high computing needs
- Long duration taken for simulation
- Convergence issues
- Necessity of precise meshes
- Challenges in simulating quantum effects

The proper selection of:

- Mesh density
- Physics models
- Numerical models

is crucial for achieving accurate outcomes.

4.15 Summary

Information on the modeling and simulation techniques as well as the extraction of electrical parameters used in the Hetero-Dielectric Nanowire Field Effect Transistor (HD-NWFET) analysis was presented in this chapter.

The proposed HD-NWFET structure was created based on:

- Cylindrical Gate All Around structure
- Double dielectric gate stack
- Nanometer structure size

A number of sophisticated physical models such as:

- SRH recombination
- Charge field dependency
- Drift diffusion approach
- Band to band tunneling
- Hot carrier generation

were incorporated into the simulation.

Effects of radiation were incorporated in the form of:

- Charges at the oxide traps
- Charges at the interface traps

CHAPTER 5
ANALYTICAL MODELING OF HETERO-DIELECTRIC NANOWIRE FET

5.1 Introduction

Analytical modeling plays an essential role in the comprehension of the electrical properties and physics involved in the working mechanism of nano-scale semiconductor devices. Analytical modeling facilitates the analysis of physical quantities like the surface potential, threshold voltage, drain current, leakage current, and radiation effects.

The novel HD-NW FET incorporates the gate-all-around nanowire architecture along with hetero-dielectric engineering technology. This chapter focuses on the analytical modeling equations associated with the proposed device.

5.2 Poisson's Equation

The electrostatic behavior of the cylindrical nanowire channel is formulated by Poisson's equation in cylindrical coordinates.

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \phi(r,z)}{\partial r}\right)+\frac{\partial^2 \phi(r,z)}{\partial z^2}=-\frac{qN_D}{\varepsilon_{si}}$$

where:

- φ(r,z) = Electrostatic potential
- q = Electronic charge
- ND = Doping concentration
- εsi = Permittivity of silicon

This equation determines the potential distribution inside the nanowire channel.

5.3 Surface Potential Modeling

Surface potential controls channel formation and carrier transport inside the transistor. The total surface potential is expressed as:

$$\phi(r,z)=V(r)+U(r,z)$$

where:

- V(r) = Long-channel potential component
- U(r,z) = Short-channel potential component

The Gate-All-Around structure has better surface potential control than the planar structure.

5.4 Modeling of Threshold Voltage

Threshold voltage refers to the minimum gate voltage needed for a conducting channel to be created.

The equation for the threshold voltage is:

$$V_{th} = V_{fb} + 2\phi_F + \frac{\sqrt{4q\varepsilon_{si}N_A\phi_F}}{C_{ox}}$$

where:

- Vth = Threshold voltage
- Vfb = Flat-band voltage
- ϕF = Fermi potential
- Cox = Oxide capacitance

Hetero-dielectric device increases stability of threshold voltage because of reduced effect of electric field on drain side.

5.5 Oxide Capacitance

The oxide capacitance is given by:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

where:

- εox = Oxide permittivity
- tox = Oxide thickness

High value of oxide capacitance results in increased controllability of gate and inversion of channel.

5.6 Drain Current Modeling

Drain current is dependent on gate voltage, carrier mobility, and dimension of the channel.

The drain current equation is represented by:

$$I_D = \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}]$$

where:

- I_D = Drain current
- μ_n = Electron mobility
- W = Channel width
- L = Channel length

This suggested structure gives better drain current characteristics due to gate controllability.

5.7 Subthreshold Current

Sub-threshold current is generated at gate voltages which are below threshold voltage. The sub-threshold current equation is represented by:

$$I_{sub} = I_0 \exp\left(\frac{q(V_{GS} - V_{th})}{nkT}\right)$$

Lower subthreshold current indicates reduced leakage and better low-power performance.

5.8 Subthreshold Slope

Subthreshold slope indicates the switching efficiency of the transistor.

It is expressed as:

$$SS = \left(\frac{d\log I_D}{dV_G}\right)^{-1}$$

Lower subthreshold slope indicates:

- Better switching characteristics
- Reduced leakage current
- Improved electrostatic control

5.9 Electric Field Modeling

The electric field distribution significantly influences the leakage current and band-to-band tunneling.

Electric field distribution can be described as:

$$E = -\nabla\phi$$

The hetero-dielectric structure minimizes the effect of the electric field crowding around the drain side.

5.10 Gate-Induced Drain Leakage (GIDL)

GIDL takes place because of the existence of high electric field on the drain side.

The expression for GIDL current is given by:

$$I_{GIDL} \propto E^2 \exp\left(-\frac{B}{E}\right)$$

where:

- E = Electric field intensity
- B = Material constant

This design eliminates GIDL phenomenon through minimizing the electric field at the drain end.

5.11 Radiation Modeling

The radiation creates oxide trapped charge and interface trap charge.

Expression for threshold voltage shift caused by radiation effect is given by:

$$\Delta V_{th} = \frac{Q_{ot} + Q_{it}}{C_{ox}}$$

where:

- Qot = Oxide trapped charge
- Qit = Interface trapped charge

Trapped charges by radiation modify the electrical behavior of the device.

5.12 Radiation Sensitivity

Radiation sensitivity shows the ability of the device to sense the radiation effect.

It is given by:

$$S = \frac{\Delta V_{th}}{Dose}$$

High radiation sensitivity means high radiation detection.

Nanowire geometry improves sensitivity because of the high surface-to-volume ratio.

5.13 Strengths of Analytical Modeling Approach

The strengths of analytical modeling approach include the following:

- Gives knowledge about device physics
- Serves as electrical behavior prediction tool
- Facilitates leakage mechanism analysis
- Contributes to radiation effects investigation

CHAPTER 6

RESULTS AND DISCUSSION

6.1 Introduction

The results and analysis of simulations carried out on the HD-NW FET designed for radiation sensing dosimeter application using the Silvaco ATLAS 3D TCAD simulator have been provided in this chapter. The performance of the proposed HD-NW FET will be compared to that of conventional nanowires in terms of reducing leakage current and radiation sensing ability.

The key parameters under consideration will be as follows:

- Sensitivity to radiation
- Voltage threshold
- Subthreshold slope
- Transconductance

The results of simulations performed show that the hetero-dielectric nanowire structure provides better performance than the conventional one by having less Gate Induced Drain Leakage (GIDL) and radiation sensing ability.

6.2 Parameter Extraction and Analysis

The critical performance characteristics of the HD-Nanowire Field Effect Transistor (FET) structure were obtained using the simulation results of its transfer and output characteristics using Silvaco ATLAS TCAD.

The results obtained for these critical performance characteristics in relation to that of SD-FET are presented in Table 3.1.

Table 6.1 – Extracted Parameters of HD-NW FET and SD-FET

Parameter	**Symbol**	**HD-NW FET**	**Single-Dielectric FET**	**Remarks**
Threshold Voltage	Vth	0.52 V	0.58 V	Improved gate control due to dielectric asymmetry
Maximum Transconductance	gm_max	78 µS	61 µS	Enhanced carrier mobility and coupling
Subthreshold Slope	SS_min	60.5 mV/dec	71.8 mV/dec	Near-ideal switching efficiency
Ion/Ioff Ratio	–	1.2×10^7	7.5×10^6	High on/off contrast ensures low leakage
Threshold Shift (300 krad)	ΔVt	0.054 V	0.072 V	Better radiation resilience

(a) Threshold Voltage (Vth)

The threshold voltage is the gate voltage required for the onset of inversion in the channel.

In the case of HD-NW FET, Vth = 0.52V, which is 60 mV less compared to that of the SD-FET.

This decrease in Vth is due to the increased electrostatic control from the hetero-dielectric stack of (HfO2/SiO2).

The HfO2 high dielectric region near the source side lowers the surface potential barrier and hence helps achieve early channel formation with better drive currents.

(b) Transconductance (gm)

Transconductance (gm) is defined as

$$g_m = \frac{dI_{ds}}{dV_{gs}},$$

denotes the present amplification of the transistor.

The HD-NW FET demonstrates a maximum value of gm equaling 78 µS, which is about 28 % higher than that of the SD-FET.

This improvement stems from enhanced electrostatic field control and carrier mobility owing to field redistribution between the two dielectrics.

Higher values of gm increase analog gains, noise ratios, and readout sensitivities in radiations sensing circuits.

(c) Subthreshold Slope (SS)

Subthreshold slope (SS) indicates how well the device switches from the OFF to ON states:

$$SS = (kT/q)\ln(10)(1 + \frac{C_d}{C_{ox}}).$$

It gives a value of SS = 60.5 mV/dec that is very close to the theoretical thermal minimum of 60 mV/dec.

This performance reflects very low depletion capacitance (C_d) and efficient suppression of interface traps at the oxide/channel junction.

The ideal value of SS allows obtaining very effective sharp switching and minimal leakage current and dynamic losses in dosimeter arrays.

(d) On/Off Current Ratio (Ion/Ioff)

On/off current ratio gives the device switching capability from the ON state to the OFF state.

An Ion/Ioff value close to 1.2×10^7 means outstanding current modulation in the HD-NW FET versus 7.5×10^6 in SD-FET.

Due to the dual dielectric structure, field confinement near the nanowire core becomes more effective, which results in good channel formation and full OFF state pinching.

In turn, this property is especially useful for precision dosimetry as the higher Ion/Ioff means better signal isolation.

(e) Threshold-Voltage Shift under Total Dose of Irradiation (ΔVt)

The total ionizing dose (TID) effect on threshold voltage is associated with positive charge trapping in the oxide and results in:

$$\Delta V_t = \frac{qN_{ot}t_{ox}}{C_{ox}}.$$

At 300 krad, the HD-NW FET shows a ΔVt = 0.054 V versus 0.072 V for the SD-FET; this represents 25% increased radiation hardness.

The hetero-dielectric junction reduces charge trapping because the trapped charge is spread across several κ regions, preventing an increase in electric field strength locally.

The property ensures that the sensor operates stably and measures radiations accurately even in extended periods.

(f) General Performance Evaluation

Owing to the hetero-dielectric nature, cylinder shape, and less sensitivity of oxide traps, FET performs with the following characteristics:

- 30% reduction in GIDL leakage current.
- Improvement of 20% on threshold voltage stability when exposed to TID irradiation.
- Better 25% analog transconductance.

Therefore, FET can be seen as better for being used as a radiations-hardening sensor based on its performance characteristics.

It is apparent from the aforementioned electrical and radiation performance characteristics that the hetero-dielectric nanowire device is more superior to normal single dielectric field-effect transistor.

Near-ideal subthreshold swing, large Ion/Ioff ratio, and small ΔVt change make it a suitable and energy-efficient sensor

6.3 Performance Analysis of the Proposed Structure in Comparison with Other Structures

In order to analyze the performance improvement due to the use of the Hetero-Dielectric Nanowire FET, a comparative analysis of the same is performed by considering other competing technologies like JLAMT-FET and CGAA MOSFET. All the devices are designed and simulated under identical conditions to make a fair comparison.

Table 6.2 – Comparative Analysis of HD-NW FET, JLAMT-FET, and CGAA MOSFET

Parameter	**HD-NW FET**	**JLAMT-FET**	**CGAA MOSFET**	**Remarks**
Threshold Voltage (Vth)	0.52 V	0.55 V	0.60 V	Lowest Vth enables faster switching
Maximum Transconductance (gm_max)	78 µS	69 µS	63 µS	Stronger gate coupling due to dual dielectric
Subthreshold Slope (SS)	60.5 mV/dec	65.2 mV/dec	72.1 mV/dec	Near-ideal SS ensures better switching control
Ion/Ioff Ratio	1.2×10^{7}	9.6×10^{6}	7.2×10^{6}	Highest Ion/Ioff, indicating superior ON/OFF behavior
Threshold Voltage Shift (ΔVt @300 krad)	0.054 V	0.062 V	0.078 V	Excellent radiation tolerance
Gate Leakage Current	2.8×10^{-13} A	4.2×10^{-13} A	5.6×10^{-13} A	Lowest leakage due to dielectric asymmetry

6.4 Comparison Discussion of Results

It is clear from the data in Table 4.1 that the HD-NW FET possesses better electrostatic properties and radiation immunity than the JLAMT and CGAA MOSFETs.
A smaller threshold voltage and a higher value for gm show better gate control, arising due to the distribution of electric fields by the hetero-dielectric stack structure (HfO_2/SiO_2).
Moreover, the better subthreshold slope implies less SCEs, even for the small size of the 40 nm gate length.
The smallest ΔVt caused by radiation is shown, implying an added benefit from hetero-dielectric structure in reducing oxide-trapped charges.
Thus, it guarantees robustness of the device in high doses of radiation used for space applications and nuclear reactors.

CHAPTER 7

CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

7.1 Conclusion

In the present study, a design of Hetero-Dielectric Nanowire Field Effect Transistor (HD-NW FET) for radiation sensing dosimeter application was presented and analyzed through Silvaco ATLAS 3D TCAD simulation. The presented structure consists of a GAA NW structure with hetero-dielectric gate technique, which improves electrostatic control and leakage current reduction.

From the simulation analysis, it was evident that the presented design is capable of:

- Less Gate-Induced Drain Leakage (GIDL)
- Threshold voltage stability improvement
- More ON/OFF current ratio
- Increased radiation sensitivity
- Leakage current reduction under OFF state operation

The presence of low-k dielectric close to drain part helped in reducing electric field crowding and thereby reduced band-to-band tunneling. The effect of radiation through oxide and interface charge traps helped in observing threshold voltage changes proving the applicability of the proposed structure in radiation detection applications.

In conclusion, the present design has outperformed the traditional NW FET and hence is a feasible alternative.

7.2 Future Scope

Future scope of the proposed work is:

- Experimentally fabricating and validating the device.
- Exploring alternate dielectric material for better sensitivity and low leakage current.
- IOT/RF based real time radiation sensing.
- Smart sensing via the application of artificial intelligence and machine learning.
- Application towards biosensors, gas sensors and flexible wearables.
- Long-term reliability under continuous radiation exposure.

7.3 Socio-economic Impact

The high-density NW FETs proposed here would make an important impact in various socio-economic areas of life ranging from the healthcare industry, to nuclear power stations, and environment sensing.

Some of the key contributions made by the NW devices in the socio-economic aspect are:

- Radiation sensing and monitoring in hospitals and cancer clinics.
- Facility for safe security for personnel working in nuclear power plants.
- Radiation sensing and monitoring in spacecrafts/satellites.
- Small scale radiation sensing equipment.
- Environmental radiation sensing.

In addition to this, low leakage current will lead to efficient energy utilization.

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EDUCATION

M.TECH (VLS)	2024-2026	Delhi Technological University, Rohini, New Delhi -110042	NA
B. TECH (ECE)	2018-2022	B K Birla Institute of Engineering and Technology, Pilani - 333031	9.34(CGPA)
CBSE (Class XII)	2018	Smt. Janki Devi Mandelia School, Pilani - 333031	85.60 %
CBSE (Class X)	2016	Smt. Janki Devi Mandelia School, Pilani - 333031	10(CGPA)

OBJECTIVE

Formal Verification Engineer at Intel Corporation with hands-on experience in C2RTL SEC verification, data path validation, and RTL debugging for complex IP blocks. Skilled in System Verilog, formal verification methodologies, and verification setup development for FPU and shuffle units. Strong understanding of digital design, verification flows, and bug analysis in advanced semiconductor environments.

Technical SKILLS

Interest Areas: Digital Electronics, Digital IC Design, Digital Design using Verilog, Low Power VLSI, Linux scripting, RTL to GDS flow, Physical Design, Static Timing Analysis	**Tools**: Cadence Virtuoso, Xilinx Vivado, LT Spice, Proteus, MPLAB, MATLAB, Arduino IDE	**Languages**: Verilog

Experience

Formal Verification Engineer, Intel corporation, India (Starting Jun'26)

Formal Verification Intern, Intel corporation, India (Jun'25 to May'26)

Contributed to the Datapath C2RTL SEC project for Xe4, focusing on FPU1 and Shuffle blocks.
Developed formal verification environments and C2RTL equivalence check setups for multiple opcodes.
Performed root-cause analysis, debugged design mismatches, and filed HSDs for identified RTL issues.

Quality Executive, Secure Meters Limited, Udaipur (Jan'22 to Jul'24)

Understanding about ISO standards (9K, 14K, & 45K) and ensuring the adherence to them among all the departments of Operations conducting internal and external audits.

Worked on various improvement projects for the continual improvements in production and operations processes.

Worked on analysis of failure products for finding their Green Y, Red X, Pink X and Pale X (Root causes) using Shainin Techniques.

Component Evaluation using Form, Fit & Function and Shainin Techniques.

ACADEMIC PROJECTS

Designing of Circular FIFO Memory (Mar'25)
Asynchronous First in First Out (FIFO) memory block would be designed with generalized width and depth.
Some status signals like full, empty, underflow, overflow, would also be generated as output.
Technology: Verilog, Xilinx (Vivado)

IC Layout Design of 3x8 Decoder (Jan'25)
Designing the schematic and layout of a Decoder, will perform pre-layout and post-layout simulations to analyze the performance of the circuit.
To study and compare the impact of layout parasitics on the performance
Technology: Cadence Virtuoso

Schematic and Layout Designing of JK Flip flop. (Dec'24)
The layout design is completed in the Layout Editor, placing and routing components while adhering to design rules, then performing DRC and LVS checks to ensure the layout matches the schematic.
Technology: Cadence Virtuoso

POSITIONS OF RESPONSIBILITY

Teaching Assistant under Dr Sonam Rewari. (Aug'24 – Apr'25)

Technical coordinator (Robex) at IEEE BKBIET SB (2020-2021)

ACHIEVEMENTS AND PUBLICATIONS

GATE Qualified

Received Trophy and Certificate for being 2nd Branch Topper in graduation (B. Tech)

Received Trophy and Certificate in class 12th and 10th board exams for "Best in Academics" for being in top 5 toppers list of the school in 2018 & 2016.

Received a letter of Appreciation from Mrs. Smriti Irani, HRD Minister at that time for excellent performance in class 10 CBSE Board Exams.