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Chapter 1 :Introduction

1.1 The Growing Challenge of Power Integrity in Advanced ICs

The evolution of integrated circuit (IC) technology has been marked by relentless scaling, enabling the integration of billions of transistors onto a single chip. This progress has driven remarkable improvements in computational power, energy efficiency, and device miniaturization. However, as technology nodes shrink and operating frequencies increase, new challenges have emerged—chief among them is the issue

of power integrity. Ensuring a stable and reliable power supply across the entire chip has become a critical concern for designers of modern VLSI and embedded systems. One of the most significant threats to power integrity is supply noise, which refers to unwanted fluctuations in the power supply voltage delivered to the various components of an IC. These fluctuations can arise from a combination of factors, including rapid switching of transistors, parasitic resistance and inductance in the power grid, and dynamic current demands from different circuit blocks. As supply voltages decrease with each technology generation, the noise margin—the difference between the actual supply voltage and the minimum required for correct operation—also shrinks, making circuits more susceptible to even minor voltage variations.

13 2 33

1.2 Understanding the Power Grid and Supply Noise

To appreciate the complexity of power delivery in modern ICs, it is helpful to visualize the on-chip power grid as a network of resistive, capacitive, and inductive elements, as illustrated in Figure 1 below.

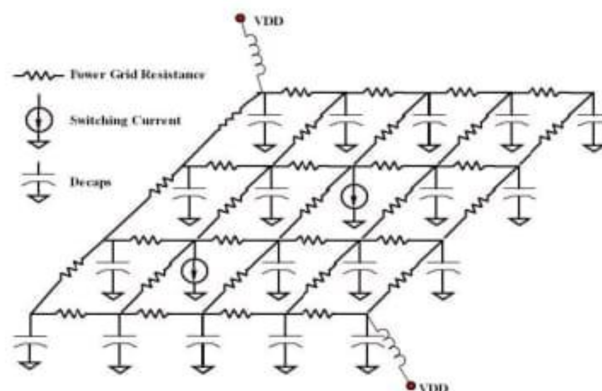

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Figure 1.1: Simplified Model of an On-Chip Power Grid with Decoupling Capacitors and Switching Currents

The diagram represents a typical power grid structure in an advanced IC. The grid consists of resistive interconnects (modeling the resistance of metal lines), decoupling capacitors (decaps) distributed throughout the grid, and current sources representing the dynamic switching activity of logic cells. The VDD nodes indicate the points where the external power supply is connected to the grid.

In this model:

- **Power Grid Resistance**: The resistive elements represent the inherent resistance of the metal layers
  used to distribute power across the chip. As the grid extends to reach all parts of the IC, the cumulative resistance can become significant, especially in large or densely packed designs.
- **Switching Current**: The current sources symbolize the time-varying current demands of logic cells as they switch states. These rapid changes in current can induce voltage fluctuations (supply noise) across the grid.
- **Decoupling Capacitors (Decaps)**: The capacitors are strategically placed to act as local energy
  reservoirs, supplying instantaneous current to nearby cells during switching events and thereby stabilizing the supply voltage.

1.3 The Impact of IR Drop

A key phenomenon that arises in the power grid is the **IR drop**—the voltage drop that occurs across the resistive elements of the grid as current flows from the VDD supply to the load. The IR drop can be expressed as:

$$V(drop)=I\times R$$

where I is the current drawn by the circuit and R is the resistance of the power grid path. As shown in Figure 1, the distributed nature of the grid means that different parts of the chip may experience different voltage drops, potentially leading to insufficient supply voltage at critical nodes. This can result in timing errors, logic failures, and degraded performance, particularly in high-speed and low-voltage designs.

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1.3.1 Static IR Drop versus Dynamic IR Drop

IR drop manifests in two fundamentally distinct forms, each with different causes, characteristics, and mitigation strategies:

Static IR Drop occurs under DC or steady-state conditions. It is caused by the continuous leakage currents and static power consumption of cells in a quiescent state. While static IR drop is generally smaller in magnitude than its dynamic counterpart, it establishes a baseline voltage offset that every cell experiences regardless of switching activity. In modern low-power designs that employ power gating and multiple voltage domains, static IR drop analysis is critical for verifying that always-on logic receives adequate voltage even when large portions of the chip are powered down.

Static IR drop is computed as:

$$V(\text{static}) = I(\text{leakage}) \times R(\text{grid})$$

where I(leakage) represents the aggregate leakage current flowing through a given section of the power grid, and R(grid) is the effective DC resistance of that path. In advanced FinFET nodes, where leakage currents are substantial even at low temperatures, static IR drop can contribute 10–20% of the total observed voltage drop budget.

Dynamic IR Drop is the more severe and complex form. It arises from the simultaneous switching of large numbers of transistors during active operation. When a clock edge triggers millions of logic cells to switch within a few picoseconds, the instantaneous current demand spikes sharply. This rapid di/dt (rate of change of current with time) interacts not only with the resistive elements of the PDN but also with its parasitic inductance L, producing an additional inductive voltage drop component:

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$$V(\text{dynamic}) = I \times R + L \times (dI/dt)$$

The inductive component $L \times (dI/dt)$ is responsible for the most severe transient voltage droops seen in high-frequency designs. At operating frequencies above 1 GHz, the rate of current change can be so rapid that the inductive drop dominates over the resistive component, causing supply voltage to dip by 10–15% of VDD within a single clock cycle. Such droops, if not properly managed, can cause setup time violations in flip-flops, corrupted logic states, and in extreme cases, complete functional failure of the affected circuit block.

1.3.2 Consequences of IR Drop on Circuit Performance

The effects of IR drop on circuit performance are pervasive and multifaceted. Understanding these consequences is essential for appreciating why power integrity has become a first-order design constraint in advanced semiconductor design.

Timing Degradation is the most immediate and quantifiable consequence of IR drop. The propagation delay of a CMOS logic gate is inversely related to its supply voltage — lower voltage means slower switching. The relationship is approximately described by the alpha-power law model:

t(pd) ∝ V(DD) / [V(DD) - V(th)]^α

where V(th) is the transistor threshold voltage and α is a fitting parameter (typically 1.0–1.3 for modern FinFET devices). When IR drop reduces the effective VDD seen by a cell, its propagation delay increases. For a cell operating at 0.9V nominal with a 100 mV IR drop (effective VDD = 0.8V), the delay increase can be 15–25% depending on the logic style and transistor sizing. In a critical timing path already operating close to the clock period, this additional delay directly causes setup time violations — the flip-flop at the end of the path captures incorrect data, resulting in functional errors.

Dynamic IR drop is particularly insidious because it is temporally correlated with clock edges. The worst-case voltage droop typically occurs 100–500 ps after a rising clock edge, precisely when data is propagating through combinational logic toward the capturing flip-flop. This temporal alignment between maximum IR drop and critical data propagation makes dynamic IR drop violations difficult to guard against with simple timing margin additions.

Signal Integrity Degradation is a secondary but significant consequence. In mixed-signal designs, supply noise couples capacitively and inductively into sensitive analog circuits, degrading signal-to-noise ratio (SNR), increasing jitter in phase-locked loops (PLLs), and introducing offset errors in analog-to-digital converters (ADCs). Even in purely digital designs, supply noise can couple into high-impedance nodes through substrate and well connections, causing spurious switching in near-threshold logic cells.

Electromigration Acceleration is a long-term reliability concern directly linked to IR drop conditions. In regions of the power grid experiencing high IR drop, the current density in metal segments is by definition elevated — since V = IR,

high drop with fixed resistance implies high current. Metal segments carrying current densities above the electromigration limit experience accelerated metal atom migration, leading to void formation and eventual open-circuit failure over the operational lifetime of the device. IR drop analysis and electromigration analysis are therefore intimately linked and are typically performed together in sign-off tools like RedHawk-SC.

Power Efficiency Reduction represents a systemic consequence of poor IR drop management. Voltage regulators and power management ICs compensate for anticipated IR drop by supplying a voltage slightly above the nominal VDD — a practice called voltage guardband. If IR drop analysis indicates a worst-case drop of 150 mV, the system may be designed to supply 0.9V + 0.15V = 1.05V to ensure all cells receive at least 0.9V. Since dynamic power scales as V^2, operating at 1.05V instead of 0.9V increases dynamic power consumption by approximately 36% — a severe efficiency penalty paid entirely to compensate for a suboptimal power grid.

1.3.3 IR Drop in Advanced Technology Nodes — Scaling Challenges

The challenge of managing IR drop has intensified dramatically with each successive technology generation, driven by several compounding scaling trends that simultaneously increase current demand and decrease the ability of the power grid to supply it.

Voltage Scaling has reduced nominal supply voltages from 1.8V in 180nm processes to 0.7–0.9V in current 5nm and 3nm nodes. While lower voltages reduce dynamic power ($P = CV^2f$), they critically reduce the noise margin available to absorb IR drop. A 100 mV drop on a 1.8V supply represents only 5.6% of VDD — manageable with reasonable design margins. The same 100 mV drop on a 0.75V supply represents 13.3% of VDD — a potentially catastrophic loss that can cause widespread timing failures. As voltage scaling continues toward near-threshold computing, where VDD approaches V(th), even 50 mV of IR drop can render the design non-functional.

Current Density Increase has accompanied voltage scaling as designers pack more transistors into the same area while maintaining or increasing performance. Despite individual transistor power reduction, the aggregate current demand per unit area (current density in A/mm^2) has increased consistently across technology generations. Modern high-performance processor cores can draw current densities exceeding 1 A/mm^2, placing extreme demands on the power delivery infrastructure.

1.4 The Role of Decoupling Capacitors

Decoupling capacitors play a vital role in mitigating supply noise and IR drop. By providing a local source of charge, decaps can quickly respond to transient current demands, reducing the magnitude of voltage fluctuations seen by sensitive circuit elements. The effectiveness of decaps depends on their value, placement, and the frequency characteristics of the noise they are intended to suppress. In the illustrated power grid, decaps are distributed throughout the network, close to the points of highest

switching activity. This strategic placement ensures that the capacitors can effectively buffer the supply voltage against rapid changes in current demand, thereby enhancing the overall stability and reliability of the IC.

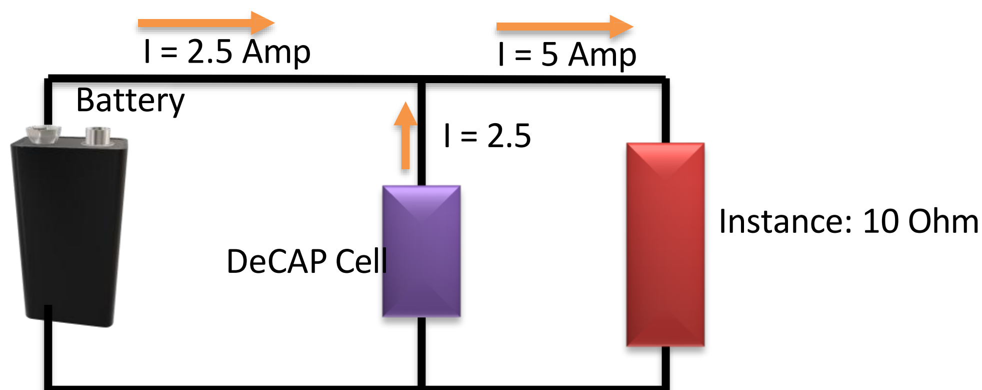

Figure 1.2: instance current requirement with decap

Motivation for Supply Noise Reduction

Reducing supply noise is essential for several reasons:

- **Signal Integrity**: Stable supply voltages are crucial for maintaining the correct operation of logic gates and minimizing timing errors.
- **Performance**: Lower supply noise enables higher operating frequencies and improved throughput.
- **Reliability**: Minimizing voltage fluctuations reduces the risk of logic failures and extends the operational lifespan of the chip.
- **Power Efficiency**: Effective noise reduction can also lead to lower power consumption by reducing

  unnecessary switching and error correction activity.

Chapter 2 : LITERATURE REVIEW

Decoupling Capacitor Planning and Optimization

Eric Wong, Jacob Minz, and Sung Kyu Lim (2006) pioneered strategies for decoupling capacitor (decap) planning and sizing to mitigate power supply noise and leakage in ICs. Their work, "Decoupling Capacitor Planning and Sizing for Noise and Leakage Reduction," introduced algorithms for integrating decaps into both 2D and 3D floorplanners. The findings demonstrated that significant reductions in decap budget and leakage power could be achieved with only minimal increases in area and wirelength. This research established the importance of early-stage decap planning and provided a foundation for subsequent CAD-based approaches.

Partha Mitra, Jaydeb Bhaumik, and Angsuman Sarkar (2021) extended this work to the system-on-chip (SoC) domain, proposing a computer-aided design (CAD) approach for estimating and allocating decaps during the physical design stage. Their method, detailed in "Power Supply Noise Aware Physical Design with Decoupling Capacitance Allocation in System-on-Chip," focused on optimal placement of decaps to reduce peak supply noise. Simulation results showed that their approach could achieve significant noise reduction with minimal impact on the cross-sectional area, making it suitable for a wide range of SoC architectures.

Partha Mitra, Prerna Alok, and Angsuman Sarkar (2020) further refined CAD methodologies for accurate decap estimation and allocation. Their research emphasized optimizing decap placement to enhance performance while minimizing power and delay penalties. The proposed approach demonstrated effective supply noise reduction with only marginal increases in delay and power consumption, underscoring the feasibility of integrating decap optimization into modern high-density VLSI design flows.

IR Drop Analysis and Power Grid Design

S. K. Nithin, Gowrysankar Shanmugam, and Sreeram Chandrasekar (2010) addressed the practical challenges of dynamic voltage (IR) drop analysis and design closure in advanced ICs. Their work highlighted the need for structured power distribution planning,

especially in power-managed designs. By analyzing industrial designs in the 45nm process, they underscored the importance of robust methodologies for power integrity and reliable operation. Their findings emphasized that effective IR drop management is essential for achieving design closure and ensuring the functional correctness of modern chips.

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Shreyasi Ghosh Dastidar and Dr. Sangeeta Nakhate (2022) investigated the impact of thermal effects on IR drop analysis in multilayered networks. Their study, "Effect of Thermal Incorporation in IR – Drop Analysis of Multilayered Network and Its Reduction Technique," evaluated how self-heating can exacerbate power supply noise and degrade reliability. By incorporating decoupling capacitors and considering temperature variations, they demonstrated improved design performance and thermal management. This work highlighted the interplay between electrical and thermal phenomena in advanced ICs and the need for holistic analysis techniques.

Key Findings from the Literature

- **Decap Planning is Essential:** Early and accurate planning of decap placement and sizing is critical for effective supply noise reduction, especially in high-density and high-speed designs.
- **CAD-Based Approaches are Effective:** Automated CAD methodologies enable optimal allocation of decaps,
  balancing noise reduction with area, power, and delay constraints.
- **IR Drop Analysis is Crucial:** Detailed IR drop analysis is necessary to ensure that all cells receive adequate supply voltage, particularly as power grids become more resistive with scaling.
- **Thermal Effects Matter:** Incorporating thermal analysis into IR drop and noise studies leads to more reliable
  and efficient chip designs.
- **Tool Support is Indispensable:** Advanced tools like RedHawk-SC facilitate comprehensive analysis and validation, supporting robust power delivery network (PDN) design.

CHAPTER 3: METHODOLOGY

3.1 IR Drop Analysis

The methodology for this research involves a comprehensive approach to IR drop analysis using the RedHawk- SC tool, a leading CAD tool widely used for power integrity and reliability analysis in advanced integrated circuits (ICs). The process begins with importing the IC design into the RedHawk-SC tool, which includes the physical layout, netlist, and relevant technology files. The design setup is configured to encompass power and ground networks, along with the initial placement of decoupling capacitors (decaps).

Once the design is set up, RedHawk-SC performs a detailed analysis of the power distribution network (PDN) to identify potential areas of IR drop. The tool simulates the power grid under various operating conditions, including different load scenarios and switching activities. This power grid analysis is crucial for understanding the distribution of voltage drops across the network and pinpointing hotspots where the voltage drop exceeds acceptable limits, potentially leading to performance degradation and logic failures.

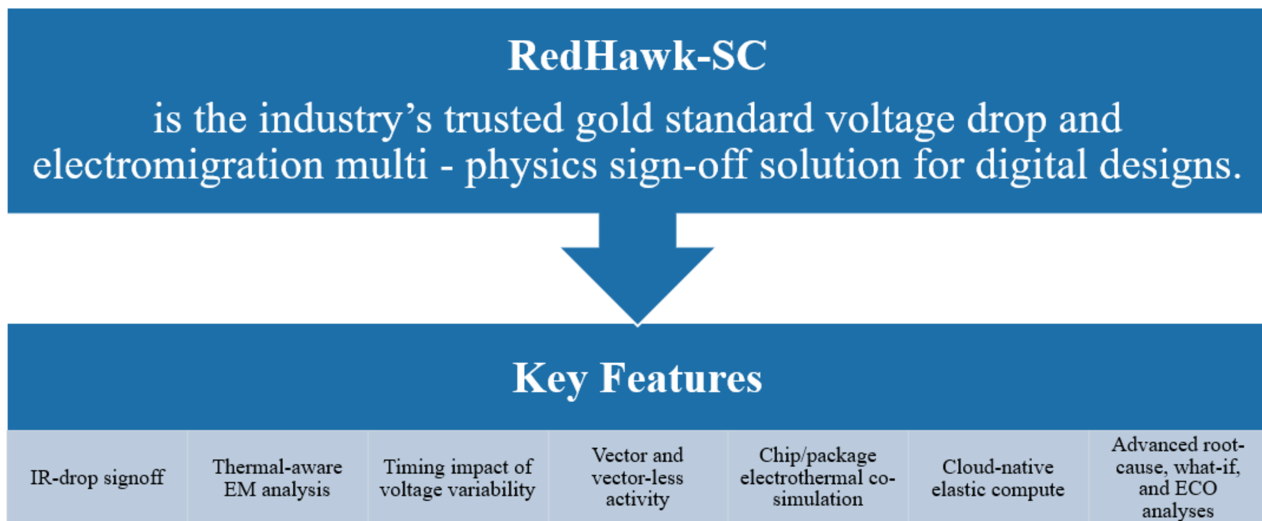

Fig 3.1 Redhawk-SC Tool overview

3.2 ANALYSIS FLOW CHART

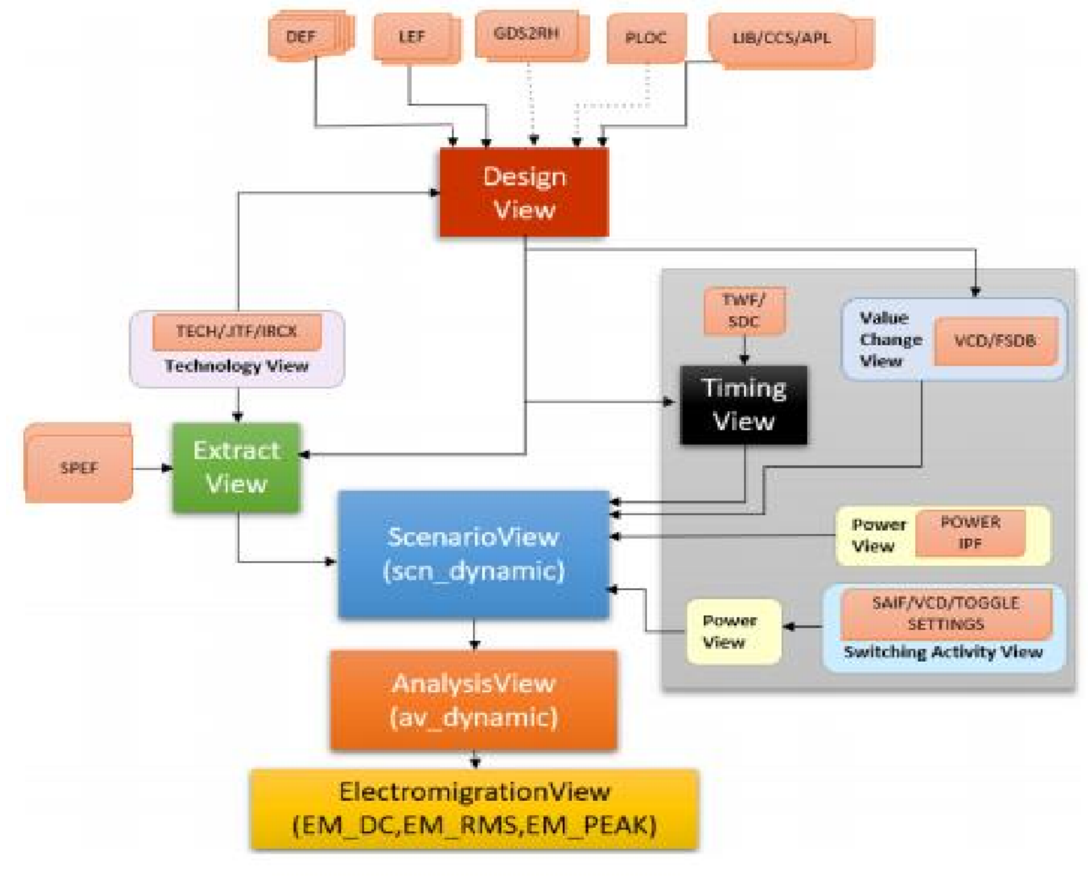

Fig 3.2 Redhawk-SC Tool Flow Analysis

3.3 SIMULATION WORK

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Data required for importing design and extracting R, C, L, leakage power, and timing information like slew , frequency , and toggle rate etc. are provided in the form of these files.

- **LIB File**
  The LIB file is a timing model that includes cell delays, transitions, and setup and hold time requirements. It is generated using CCS (Composite Current Source) and NLDM (Non-Linear Delay Model) techniques. The file contains essential units such as time, voltage, and current, among others.

- **LEF File (Library Exchange Format)**
  The LEF file provides an abstract representation of cells, detailing the physical boundary, pin positions, and metal layer information. It does not offer complete cell information; for that, the DEF (Design Exchange Format) file is necessary.

- **SPEF File (Standard Parasitic Exchange Format)**
  The SPEF file is a compact format that details parasitic elements. It specifies the units of parasitic resistance (R) and capacitance (C) at the beginning of the file, allowing for a detailed representation of these elements.

- **DEF File (Design Exchange Format)**
  The DEF file contains placement information for macros, standard cells, I/O pins, and other physical entities. It serves as a bridge between the logical design data and the physical design data, facilitating place and route processes.

- **Tech File**
  The tech file includes information about metal layers, via metal details, and the resistance values of different layers. This file is crucial for understanding the physical properties of the design.

- **VCD File**
  The VCD file records the toggling factor (α) of instances, representing switching activity. This data is used to calculate switching power, providing insights into the dynamic behavior of the design.

- **Pg.ploc File**
  The pg.ploc file lists the locations of power and ground bumps, including their names, coordinates, and the metal layer on which they are placed. This file is essential for defining the power distribution network.

- **STA or SDC File**
  The STA file contains information on slew, transition, frequency, and timing windows, which are used in power and IR drop calculations. The Verilog file provides connectivity and placement details for the logical elements of the design.

3.4 Script Design

Fig 3.3 IR script snapshot

Above script is written in python and it shows the Use of **APL Files** in IR Drop Analysis. These files contain detailed information about the switching activities and power consumption patterns of the IC components. When running the IR drop analysis, the APL files are imported into Redhawk-SC **to simulate realistic activity profiles**. This ensures that the power distribution network (PDN) is accurately modeled under various load conditions.

```
import package
gp.open_scheduler_window()
bsub_command = 'bsub -P dp085 -q reg -R "rusage[mem=30000]"'
ll = create_lsf_launcher('lsf_launcher', bsub_command)
register_default_launcher(ll, max_num_workers=200)

include('./options.py')
include('./input_files.py')

db = gp.open_db('./db')
lv = db.get('lv.latest')
dv0 = db.get('dv0.latest')
dv = db.get('dv.latest')

rename_pg_nets = []
voltage_levels = {'vdd' : 0.90, 'gnd' : 0, }
focus_pg_nets = ['vdd', 'gnd']

tv = db.create_timing_view (dv, timing_window_files=tw_files,
     tag = 'tv', options=options)


nv = db.create_tech_view (tech_file_name=tech_file,
     options=options, tag = 'nv')


default_period = 0.5e-09
data_toggle_rate = 0.5
clock_toggle_rate = 2.0

settings = {'default_clock_period'                      : default_period,
            'default_clock_pin_toggle_rate'             : clock_toggle_rate,
            'default_combinational_pin_toggle_rate'     : data_toggle_rate,
            'default_macro_output_pin_toggle_rate'      : data_toggle_rate,
            'default_sequential_output_pin_toggle_rate' : data_toggle_rate
           }
```

```
swa = db.create_switching_activity_view(timing_view=tv,
      vcd_files=vcd_files, value_change_data=None, tag='swa1',
      propagation_style='assign_default_activity', use_sta_clock_info=True,
      settings=settings, options=options)


evx = db.create_extract_view_from_files(dv, input_files=spef_files, tag='evx',
      options=options)


pwr = db.create_power_view_from_switching_activity(swa,
      timing_view=tv, options=options, voltage_levels=voltage_levels,
      external_parasitics=evx, tag='pwr',
      current_data_precedence=['APL','NLPM','CCSPOWER'])


ev =  db.create_extract_view(dv, tech_view=nv,
      calculate_spr=False, temperature=125, options=options, tag='ev', mode='pg')


ev_signal = db.create_extract_view(dv, tech_view=nv, calculate_spr=False,
            temperature=125, options=options, tag='ev_signal', mode='signal')


sv = db.create_simulation_view(ev, enable_reduction=True,
     options=options, tag='sv')


sv_sigem = db.create_simulation_view(ev_signal, enable_reduction=True,
           options=options, tag='sv_sigem', sim_type='sigem')
```

Fig 3.4 Input Files in the main run script

12
12
36

Views Created After the IR Drop Analysis with RedHawk-SC

After performing the IR drop analysis using the RedHawk-SC tool, several important views are generated to provide comprehensive insights into the power integrity and performance of the integrated circuit (IC). These views include the Design View, NV (Node Voltage) View, and EM (Electromigration) View, among others. Each of these views serves a specific purpose and offers detailed information that is crucial for further analysis and optimization.

1. **Design View:**
   - The Design View is the foundational view that includes the physical layout, netlist, and technology files of the IC. It provides a complete representation of the circuit's design, including the placement of components and interconnections. This view is essential for setting up the initial conditions for the IR drop analysis and serves as the basis for generating other views.
2. **NV (Node Voltage) View:**
   - 2 The NV View captures the voltage levels at various nodes within the power distribution network (PDN) after the IR drop analysis. It provides a detailed map of voltage drops across the circuit, highlighting areas where the voltage may fall below acceptable levels. This view is crucial for identifying hotspots and understanding the distribution of voltage drops, enabling targeted interventions to mitigate supply noise.
3. **EM (Electromigration) View:**
   - The EM View focuses on the analysis of electromigration, a phenomenon where high current densities cause the gradual displacement of metal atoms in interconnects, leading to potential failures. This view provides insights into the current densities and identifies areas at risk of electromigration. By analyzing the EM View, designers can implement strategies to enhance the reliability and longevity of the IC.
4. **Decap Placement View:**
   - The Decap Placement View shows the optimal locations for placing decoupling capacitors (decaps) based on the IR drop and thermal analysis. It provides a strategic map for placing decaps to stabilize the power supply voltage and minimize supply noise. This view helps in fine- tuning the design to achieve significant noise reduction with minimal impact on other performance parameters.

3.5 CONCEPT OF POWER/GROUND FILLS IN THE DESIGN

To strengthen the power grid (PG) in chip design, various techniques are employed, such as adding more metal layers to the PG, increasing the width of power rails, using thicker metal wires, and placing decoupling capacitors strategically to reduce IR drop. These techniques help to ensure that the power is distributed evenly across the chip, and the voltage drop is minimized. Additionally, simulations and tests are performed to evaluate the robustness and efficiency of the Power Grid design, and improvements are made accordingly. Traditionally, once the routing process is complete, vacant areas in the design are filled with dummy metal to prevent violation. Power Ground Fill addition is an alternative approach to inserting dummy metal Fills in empty spaces during chip design. Instead of dummy metal, PG fills put into vacant spaces to connect with the PG grid, as illustrated Figure. This method enhances the current distribution efficiency by ensuring that PG Fills are distributed evenly.

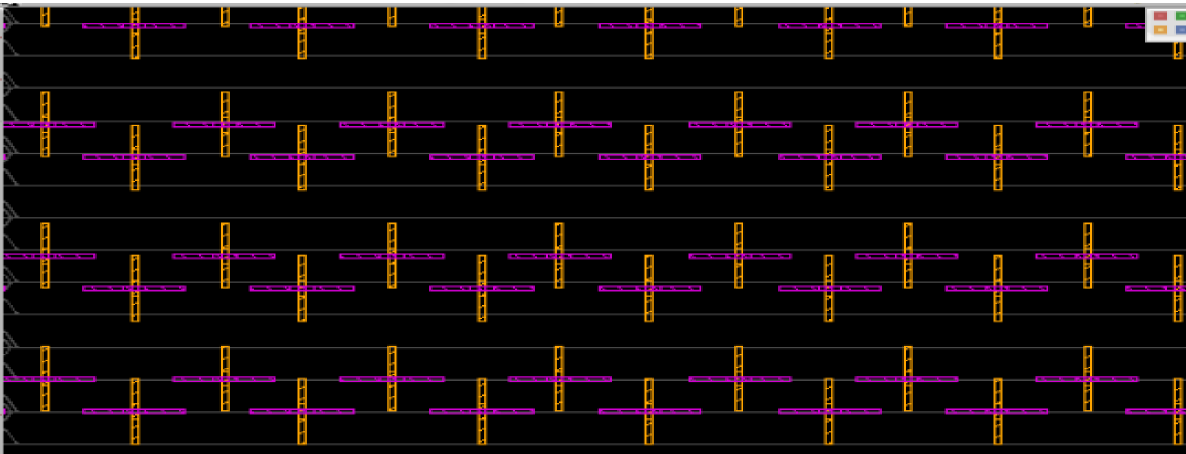

Fig 3.5 Before Smart PG fills

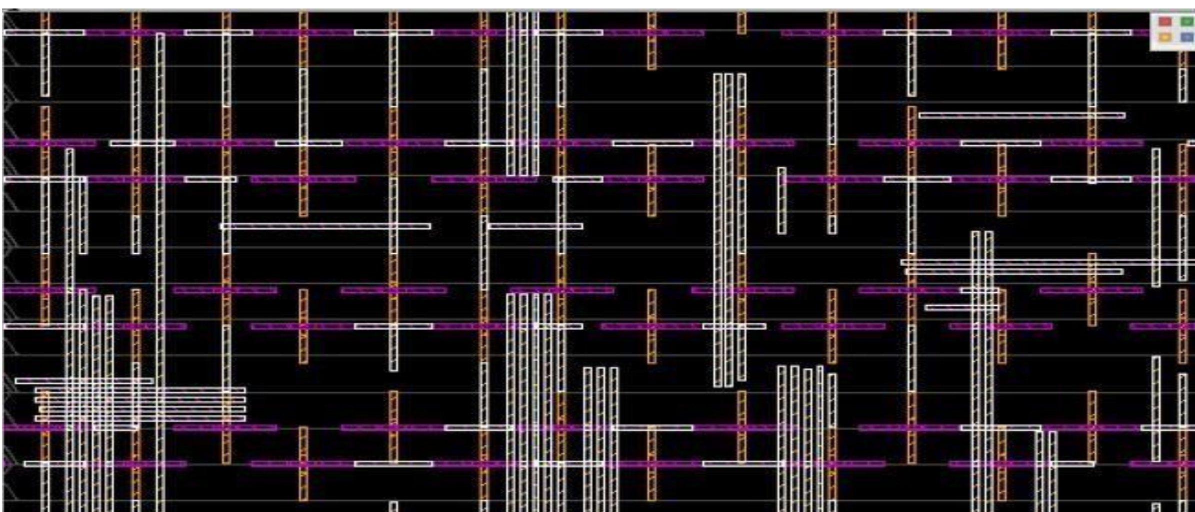

Fig 3.6 After Smart PG fills

4

Power Ground Grid Strengthening:

There are two types of grids strengthening methods as follows:

- **Manual Power Ground GRID Strengthening**: Manual PG (Power Grid) strengthening refers to the process of manually adding additional power grid structures to a design in order to improve its power distribution and alleviate IR drop issues. This approach involves identifying areas of the design that are experiencing high levels of dynamic power drop and manually adding additional power grid structures, such as metal straps, vias, or power rails, to those areas. Manual PG strengthening can be a time- consuming process that requires significant expertise and experience. It may also involve modifying the original design and running additional simulations to ensure that the new power grid structures do not introduce new issues or negatively impact the design's performance. Despite its challenges, manual PG strengthening can be an effective approach for addressing IR drop issues in some designs, particularly those with large or complex power grids. The problem with this method is that it is not efficient for larger designs that have a high degree of dynamic power drop and numerous instances with IR drop violations. In such cases, manual PG strengthening may not be a viable solution.

- **Power Ground Grid Strengthening with Pegasus flow** Traditionally, once the design has been routed, empty regions are filled with dummy metal fills to prevent Violations. In Power Ground fill insertion, alternatively putting dummy fills, power grid fills are put into empty spaces in conjunction with the Power Ground grid. The insertion of PG fills can enhance the current distribution in the power grid by generating supplementary parallel routes for the current to pass through. By doing so, it aids in identifying the shortest current path, which ultimately lowers the current density in the power net. This, in turn, can alleviate drop issues for the cells. Therefore, by implementing Power Ground fill insertion, the design can experience a more efficient distribution of current and improved performance.

3.6 CONCEPT OF SHDMIM CAPACITORS IN THE DESIGN

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A Super High-Density Metal-Insulator-Metal (SHDMIM) capacitor is an advanced type of capacitor designed to enhance power integrity and reduce noise in integrated circuits (ICs). SHDMIM capacitors are strategically
integrated into the power delivery network to address low-frequency noise and improve the overall stability of the power supply.

SHDMIM capacitors offer several advantages over traditional decoupling capacitors (decaps). They provide a high capacitance density, which allows for significant capacitance within a small footprint. This high density is crucial for maintaining stable power supply levels in densely packed IC designs, such as those found in
advanced FinFET nodes.

The primary function of SHDMIM capacitors is to act as local energy reservoirs, similar to decoupling capacitors, but with enhanced capabilities. They store and supply charge during transient events, such as

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switching activities, to prevent significant voltage drops in the power supply network. This stabilization of the power supply voltage is essential for ensuring the proper functioning of high-speed and high-frequency circuits.

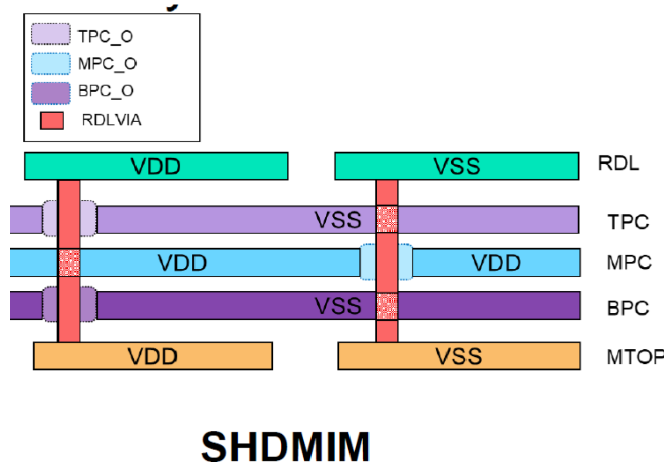

Fig 3.7 SHDMIM Capacitor Structure

Key Features and Benefits of SHDMIM Capacitors:

1. High Capacitance Density: SHDMIM capacitors provide a high capacitance per unit area, making them ideal for applications where space is limited. This high density helps in maintaining a stable power supply in compact IC designs.
2. Low Equivalent Series Resistance (ESR) and Inductance (ESL): SHDMIM capacitors exhibit low ESR and ESL, which are critical for effective noise filtering. Low ESR and ESL ensure that the capacitors can quickly respond to transient events and provide a low-impedance path for noise, thereby reducing voltage fluctuations.
3. Self-Healing Properties: SHDMIM capacitors possess self-healing properties, which enhance their reliability and longevity. This feature allows the capacitors to recover from dielectric breakdowns and continue functioning effectively, making them suitable for long-term use in IC designs.
4. Effective Low-Frequency Noise Reduction: SHDMIM capacitors excel in reducing low-frequency noise, which is often associated with power supply fluctuations and load variations. By mitigating low- frequency noise, these capacitors help maintain a clean and stable power supply, which is essential for the proper functioning of the entire system.
5. Improved Transient Response: The high capacitance density and low ESR/ESL of SHDMIM capacitors contribute to an improved transient response. This means that the capacitors can quickly stabilize the voltage levels after transient events, ensuring minimal disruption to the circuit operation.
6. Enhanced Power Integrity: By providing a stable power supply and reducing voltage noise, SHDMIM capacitors enhance the overall power integrity of the IC. This improvement leads to better performance, reduced error rates, and increased reliability of the system.

Integration into the Design:

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Designers incorporate SHDMIM capacitors into the power delivery network to mitigate the impact of noise on the power mesh. These capacitors are placed near critical components and power delivery paths to provide immediate charge during transient events. The strategic placement of SHDMIM capacitors ensures that they can effectively filter out low-frequency noise and stabilize the power supply voltage .

The integration of SHDMIM capacitors involves careful consideration of the capacitance values required to address the specific noise frequencies present in the design. A combination of capacitors with different values can provide effective filtering for a wide range of frequencies, ensuring comprehensive noise reduction .

The implementation of SHDMIM capacitors in IC designs offers a robust solution for enhancing power integrity and reducing noise. Their high capacitance density, low ESR/ESL, self-healing properties, and effective low-frequency noise reduction make them an indispensable component in modern high-performance IC designs. By incorporating SHDMIM capacitors, designers can achieve significant improvements in power stability, noise resilience, and overall circuit performance, addressing key challenges in advanced semiconductor technologies.

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Observations without Decap

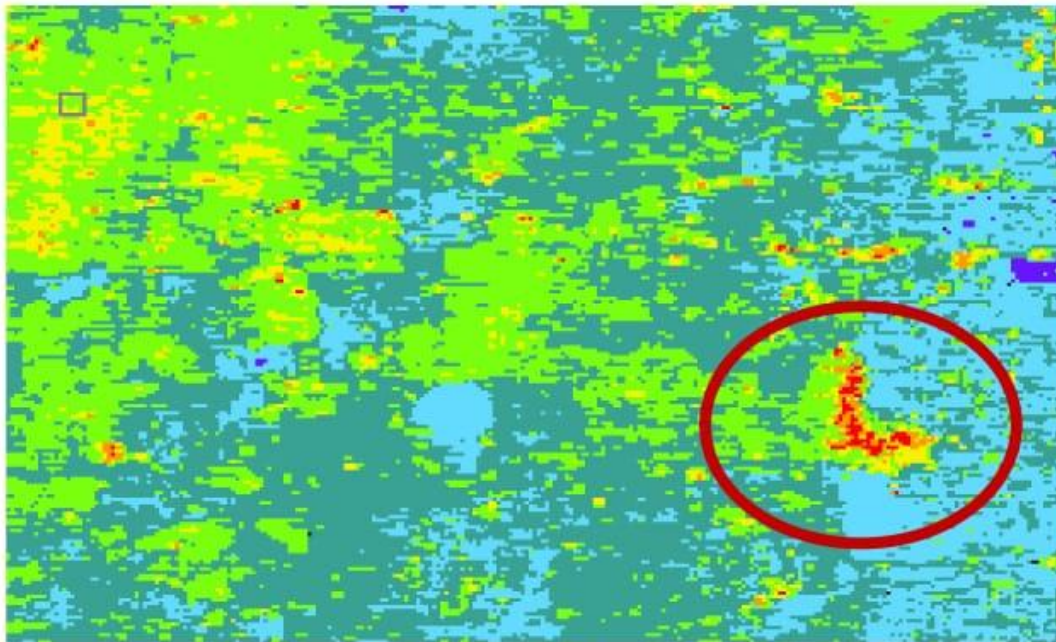

Fig 4.1 Worst Drop instance zoomed view

Key Observations:

1. **Worst IR Drop Region:**
   - The highlighted region in the figure indicates the area experiencing the highest voltage drop. An **IR drop of 156 mV** is significant and can adversely affect the performance and reliability of the circuit components in this region.
2. **Impact on Circuit Performance:**
   - Such a substantial IR drop can lead to various issues, including timing errors, signal integrity degradation, and potential logic failures. Components within this region may not receive sufficient voltage to operate correctly, leading to malfunctioning or reduced performance.
3. **Absence of Decoupling Capacitors:**
   - The figure represents the state of the design without the use of decoupling capacitors. Decaps are crucial for stabilizing the power supply voltage and mitigating voltage drops. Their absence in this scenario highlights the vulnerability of the power distribution network to significant IR drops.

4.2 Method 1: Implementing Decoupling Capacitors (Decaps) in the Design

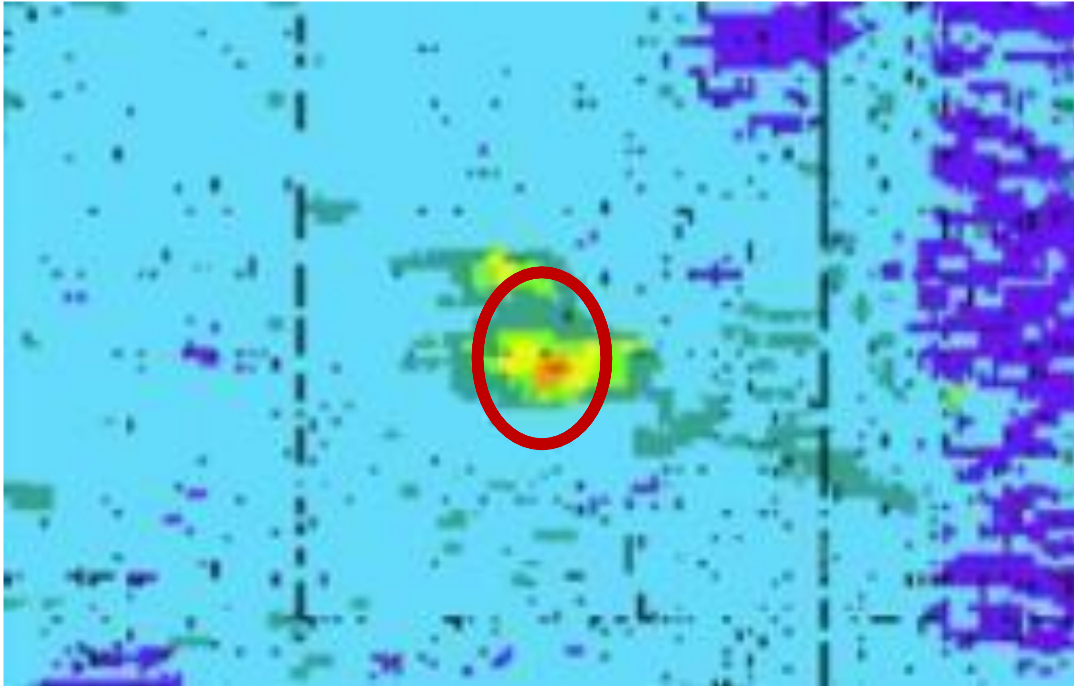

Fig 4.2 Worst Drop instance zoomed view after placing decaps

Key Observations:

1. **Reduced Worst IR Drop Region:**
    - The highlighted region in the figure indicates the area experiencing the highest voltage drop. The **IR drop has been reduced from 156 mV to 146 mV**, which is a notable improvement. This reduction demonstrates the effectiveness of decoupling capacitors in stabilizing the power supply voltage.

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2. **Decreased Red Region:**
    - **The red region**, which represents areas with severe voltage drops, **has also been significantly reduced**. This indicates a more uniform and **stable power distribution** across the IC, minimizing hotspots where voltage drops could adversely affect performance.

3. **Impact on Circuit Performance:**
    - The reduction in IR drop enhances the overall performance and reliability of the circuit components in this region. With a lower voltage drop, components are more likely to receive sufficient voltage, reducing the risk of timing errors, signal integrity issues, and logic failures.

4. **Effectiveness of Decoupling Capacitors:**

   - The figure illustrates the positive impact of incorporating decoupling capacitors into the design. Decaps act as local energy reservoirs, providing immediate current to the circuit components during transient events, thereby stabilizing the power supply voltage and mitigating voltage drops.

5. **Improved Power Integrity:**

   - The reduction in the worst IR drop and the decreased red region indicate improved power integrity within the IC. This improvement ensures that the circuit operates more reliably, with enhanced signal integrity and reduced risk of performance degradation.

4.13 Result Comparison

Parameter	Without DECAP (mV)	With DECAP (mV)
IR Drop	156	146

Table 1 Result comparison of with and without Decap

4.3 Method 2: Implementing Power Ground Fills (PG) in the Design

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The implementation of intelligent power-ground metals in the pg enables the efficient distribution of current design. When STA done data is taken into account for power noise analysis, the resulting IR map is shown in Fig. 4.3, with red dots indicating large voltage drops in certain parts of the chip.

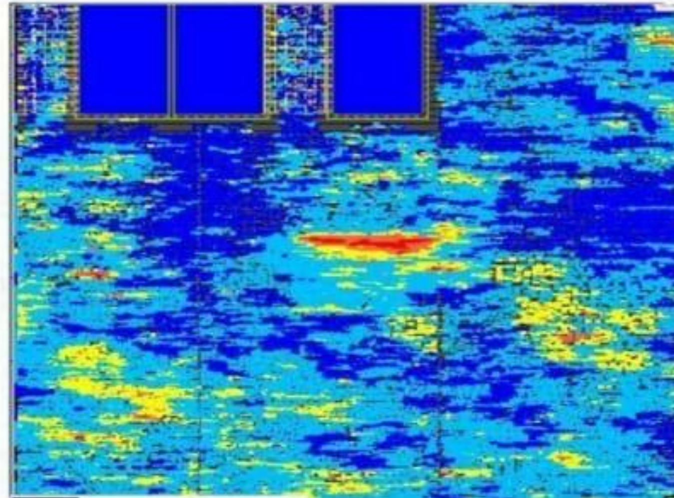

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Fig 4.3 IR Drop Before Smart PG Fills

The orange, yellow, and sky-blue spots all exhibit drops in the range of 75mV-93.75mV, 56.25mV-75mV, and 37.5mV-56.23mV, respectively, while the red spots show drops over or equal to 93.75%. Dark blue, on the other hand, exhibits a decrease below 37.5 mV.

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Adding PG fills with Pegasus considerably decreased the occurrences with larger voltage drop, as illustrated in

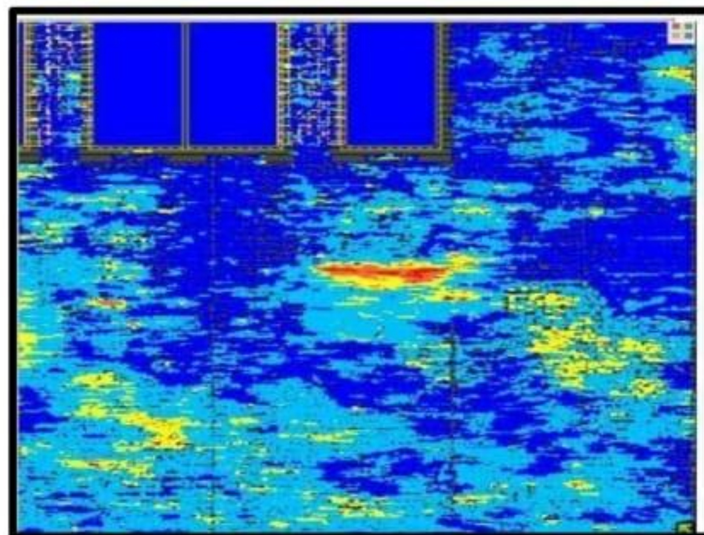

Fig. 4.4 IR Drop After Smart PG Fills

4.4 Result Comparison after PG fills

The implementation of intelligent power-ground metals in the pg enables the efficient distribution of current design. Table 2 and 3 below present a differentiation of the instance count with and without Power Ground fills, and the difference between the two is evident. In the case of block Block_1, the instances experiencing a drop of 100-150 millivolts have decreased to 42% compared to the previous value. Similarly, for Block_2, the decrease is 50.2%, and for Block_3, it is now 37.8% of the previous value.

Blocks	Before Power Ground Fill		
	Greater than150	100 to 150mV	50 to 100mV
Block_1	0	6870	1131833
Block_2	39	35189	1159503
Block_3	29	55070	4207388

Table 2: Dynamic drop before PG Fills

Blk	After Power Ground Fill		
	Greater than 150	100 to 150mV	50 to 100mV
Block_1	0	3929	939318
Block_2	7	17531	875330
Block_3	8	34290	3229656

Table 3: Dynamic Drop after PG Fills

Table 4: makes it evident that following PG fills, there were 54% fewer instances of decreases between 25 and 30 millivolts. Like this, the number of occurrences for drops between 30 and 35 millivolts has decreased by 69%, and instances for drops beyond 35 millivolts have decreased by 99%.'

	Before Power Ground Fill	After Power Ground Fill
25 to 30 mV	54534	25338 (54%)
30 to 35 mV	6488	2020 (69%)
Greater than 35 mV	305	5(98.8%)

Table 4: Static Drop before and after PG Fills

Fig 4.5 displays a comparison between the instance count that experienced more drop with and without Power Ground fills.

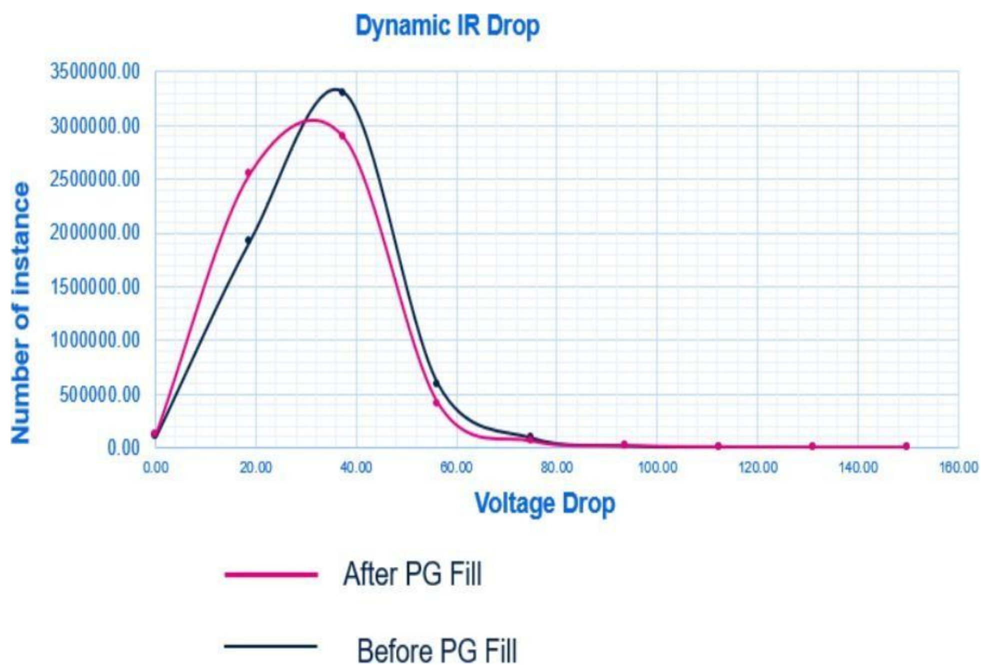

Fig 4.5 Instance count Vs drop with and without PG fills

Fig 4.6 Noise reduction after inserting PG fills

Below figure showing reduced supply noise in the SOC, the overlap is between high supply noise(orange) and reduced supply noise after assigning decaps and pg fills in the design.

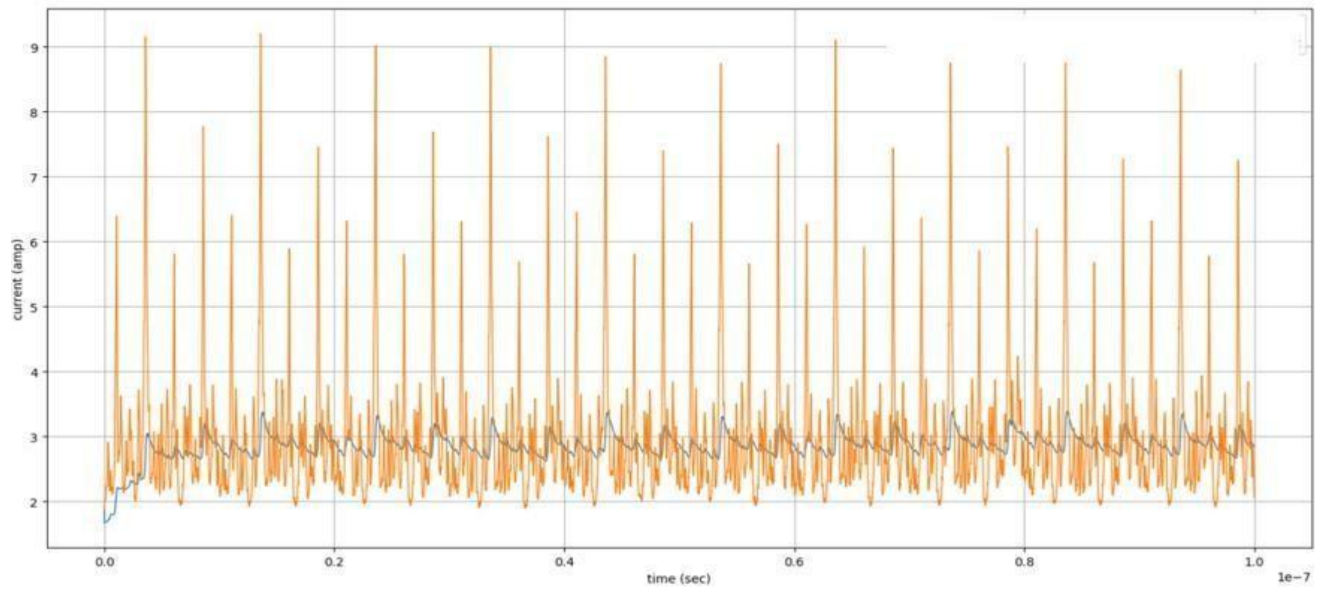

Fig 4.6 Noise reduction after inserting PG fills

Blue : showing supply noise reduction post assigning decap and PG fills

Orange: Showing high supply noise before assigning decap and pg fills

4.5 Method 3: Implementing SHDMIM Capacitors in the Design (SOC)

The integration of SHDMIM (Super High-Density Metal-Insulator-Metal) capacitors in the design significantly enhances power integrity and noise reduction. When Static Timing Analysis (STA) data is utilized for power noise analysis, the resulting IR map is depicted in Fig. 4.6. This figure shows red dots indicating areas with substantial voltage drops across various sections of the chip.

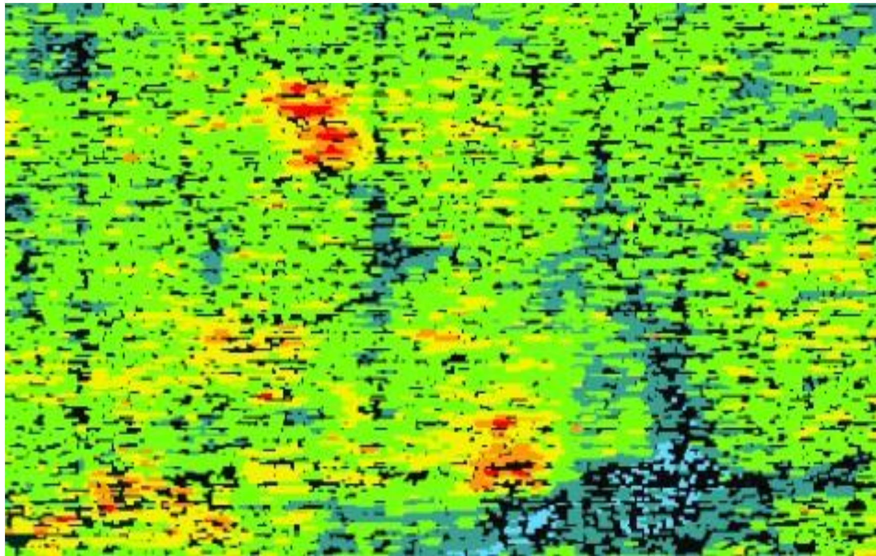

Fig 4.7 Before SHDMIM insertion

The red spots indicate voltage drops greater than or equal to 150 mV, while the orange, yellow, and sky-blue spots exhibit drops in the range of 110 mV to 150 mV, 90 mV to 110 mV, and 70 mV to 90 mV, respectively. Dark blue spots, on the other hand, show voltage drops below 70 mV.

By incorporating SHDMIM capacitors, the occurrences of larger voltage drops were significantly mitigated, as illustrated in Fig 4.7.

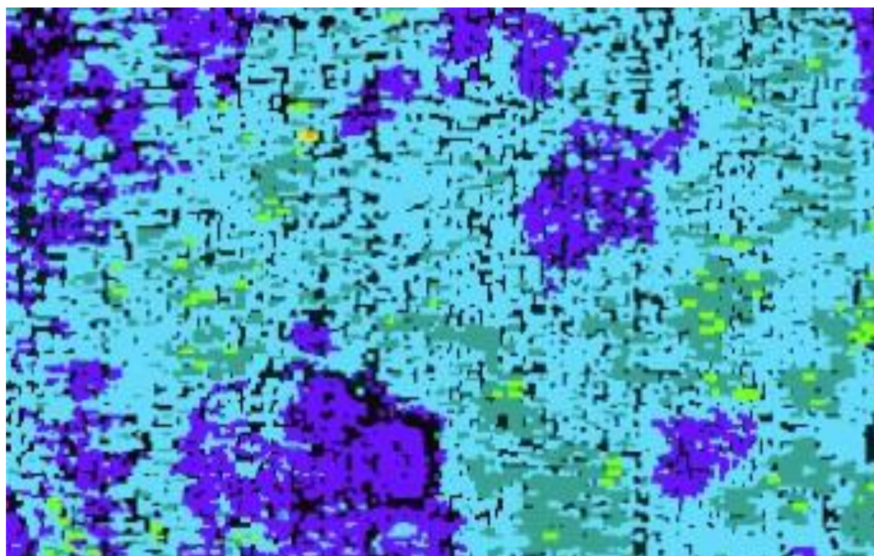

Fig 4.8 After SHDMIM insertion

4.6 Result Comparison after SHDMIM insertion

The implementation of SHDMIM capacitors in the design has significantly improved power integrity and noise reduction. Table 5 and Table 6 below present a comparison of key parameters with and without SHDMIM capacitors, highlighting the substantial improvements achieved.

In the case of voltage fluctuations in the integrated circuit (IC) or System-on-Chip (SOC), the implementation of SHDMIM capacitors has resulted in a reduction from 198.5 mV to 140 mV, which is a 29.45% decrease. Additionally, the settling time of these voltage fluctuations has been reduced from 20 ns to 8.6 ns, representing a 57% improvement. Furthermore, the peak-to-peak voltage of the SOC bump after stabilization has decreased from 98.5 mV to 71.5 mV, indicating a 27.41% reduction.

Parameter	Without SHDMIM Cap
Voltage fluctuations of IC/SOC (mV)	198.5
Settling time of voltage fluctuations (ns)	20
Peak-to-peak voltage of SOC bump (mV)	98.5

Table 5: Dynamic Drop before SHDMIM Capacitors

Parameter	With SHDMIM Cap
Voltage fluctuations of IC/SOC (mV)	140
Settling time of voltage fluctuations (ns)	8.6
Peak-to-peak voltage of SOC bump (mV)	71.5

Table 6: Dynamic Drop after SHDMIM Capacitors

Table 4 makes it evident that following the implementation of SHDMIM capacitors, there were significant reductions in voltage drops and noise. Specifically, the voltage fluctuations in the IC/SOC have decreased by 29.45%, the settling time of these fluctuations has improved by 57%, and the peak-to-peak voltage of the SOC bump after stabilization has reduced by 27.41%. These improvements underscore the effectiveness of SHDMIM capacitors in enhancing power integrity and reducing noise in the design.

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The implementation of SHDMIM capacitors has led to several noteworthy improvements in the design, making it a highly effective solution for enhancing power integrity and reducing noise. Here are the key reasons why the results after implementing SHDMIM capacitors are beneficial:

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1. **Reduction in Voltage Fluctuations**: The voltage fluctuations in the IC/SOC have decreased from 198.5 mV to 140 mV. This reduction of 29.45% is significant because it indicates a more stable power supply, which is crucial for the reliable operation of sensitive electronic components. Stable voltage levels help prevent malfunctions and improve the overall performance of the system.

2. **Improved Settling Time**: The settling time of voltage fluctuations has been reduced from 20 ns to 8.6 ns, a 57% improvement. Faster settling times mean that the system can stabilize more quickly after transient events, such as power surges or switching activities. This rapid stabilization is essential for maintaining the integrity of high-speed circuits and ensuring that they operate correctly without delays or errors.

3. **Enhanced SOC Bump Voltage Stability**: The peak-to-peak voltage of the SOC bump after stabilization has decreased from 98.5 mV to 71.5 mV, representing a 27.41% reduction. This improvement in SOC bump voltage stability ensures that the power delivered to various parts of the chip remains consistent, reducing the risk of voltage-related issues and enhancing the overall reliability of the SOC.

4. **Increased Reliability and Performance**: By reducing voltage fluctuations and improving settling times, SHDMIM capacitors contribute to the increased reliability and performance of the IC/SOC. These improvements help prevent potential failures and extend the lifespan of the electronic components, making the design more robust and dependable.

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5. **Low-Frequency Noise Reduction**: SHDMIM capacitors are particularly effective in reducing low- frequency noise, which is often associated with power supply fluctuations and load variations. By mitigating low-frequency noise, these capacitors help maintain a clean and stable power supply, which is essential for the proper functioning of the entire system.

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6. **Noise Reduction**: SHDMIM capacitors are highly effective in filtering out noise, which is critical for maintaining signal integrity in high-speed and high-frequency circuits. The reduction in noise levels ensures that the signals remain clean and free from interference, leading to better data transmission and processing accuracy.

7. **Power Integrity Enhancement**: The overall enhancement in power integrity due to the implementation of SHDMIM capacitors ensures that the power distribution network within the IC/SOC operates efficiently. This efficiency is vital for the optimal performance of the chip, as it minimizes power losses and ensures that all components receive the required power levels.

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CONCLUSION

This study demonstrates the effectiveness of decoupling capacitors in reducing IR drop and enhancing power integrity in advanced integrated circuits. Through detailed simulation and analysis, it was shown that the strategic placement of decaps leads to a measurable reduction in both the magnitude and distribution of IR drop across the power grid. The maximum IR drop was reduced by 10 mV, and voltage stability was improved throughout the chip.

These improvements translate directly into enhanced signal integrity, reduced error rates, and greater overall reliability of the IC. The findings underscore the necessity of integrating decap optimization into the standard design methodology for modern VLSI systems. Future work may focus on further optimizing decap placement using machine learning or hybrid approaches, as well as exploring the combined effects of decaps with other noise reduction techniques to address both high- and low-frequency supply noise. Additionally, extending the analysis to account for process variations, aging, and real-world operating conditions will further strengthen the robustness of power delivery networks in next-generation electronic systems.

FUTURE WORK

Building on the results achieved in this work, future research will focus on further enhancing power integrity through the optimized implementation of Metal-Insulator-Metal (MIM) capacitors in advanced integrated circuit designs. After integrating MIM capacitors within the power delivery network, a detailed **System-on-Chip (SoC) bump current analysis** will be performed to evaluate current distribution across package bumps and its impact on power grid reliability.

REFERENCES

[1] E. Wong, J. Minz, and S. K. Lim, "Decoupling capacitor planning and sizing for noise and leakage reduction," in *Proceedings of the International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, USA, Nov. 2006.

[2] P. Mitra, J. Bhaumik, and A. Sarkar, "Power supply noise aware physical design with decoupling capacitance allocation in system-on-chip," in *Proceedings of the Devices for Integrated Circuit (DevIC)*, 2021, doi: 10.1109/DevIC50843.2021.945591.

[3] P. Mitra, P. Alok, and A. Sarkar, "A CAD approach for accurate decap estimation and allocation for supply noise reduction in SoC," in *Proceedings of the IEEE VLSI Device, Circuit and System Conference (VLSI-DCS)*, Kolkata, India, July 2020.

[4] S. Ghosh Dastidar and S. Nakhate, "Effects of thermal incorporation in IR-drop analysis in multilayered network and its reduction techniques," in *Proceedings of the IEEE International Conference on Electrical, Electronics and Computer Science (SCEECS)*, Jan. 2022.

[5] S. K. Nithin, G. Shanmugam, and S. Chandrasekar, "Dynamic voltage (IR) drop analysis and design closure: Issues and challenges," in *Proceedings of the 11th International Symposium on Quality Electronic Design (ISQED)*, 2010, pp. 803–808.

[6] A. H. Ajami, K. Banerjee, A. Mehrotra, and M. Pedram, "Analysis of IR-drop scaling with implications for deep submicron power/ground network designs," in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, 2003, pp. 60–67.

[7] T. Karim, *On-Chip Power Supply Noise: Scaling, Suppression and Detection*, Ph.D. dissertation, Dept. of Electrical and Computer Engineering, University of Waterloo, 2012.

[8] M. Seok, "Decoupling capacitor design strategy for minimizing supply noise of ultra-low voltage circuits," in *Proceedings of the Design Automation Conference (DAC)*, 2012.

[9] S. Pant, *Design and Analysis of Power Distribution Networks in VLSI Circuits*, Ph.D. dissertation, Dept. of Electrical Engineering, University of Michigan, 2008.

[10] P. Oldiges, R. Vega, H. Utomo, N. Lanzillo, T. Wassick, J. Li, and J. Wang, "Chip power-frequency scaling in 10/7 nm node," *IEEE Access*, vol. PP, pp. 1–1, 2020, doi: 10.1109/ACCESS.2020.3017756.

[11] W. S. Song and L. A. Glasser, “Power distribution techniques for VLSI circuits,” *IEEE Journal of Solid-State Circuits*, vol. 21, no. 1, pp. 150–156, Feb. 1986.
[12] Y.-H. Huang, M.-S. Zhang, and H.-Z. Tan, “A novel method for IR-drop reduction in high-performance printed circuit boards,” in *Proceedings of the International Conference on Electronic Packaging Technology (ICEPT)*, 2014.
[13] M.-S. M. Lee, K.-S. Lai, C.-L. Hsu, and C.-N. J. Liu, “Dynamic IR-drop estimation at gate level with standard library information,” in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Paris, France, 2010, pp. 2606–2609.
[14] M.-S. Zhang and H.-Z. Tan, “IR-drop modeling and reduction for high-performance printed circuit boards,” *IEEE Electromagnetic Compatibility Magazine*, vol. 4, no. 4, pp. 90–101, 2015.