sagar_thesis.pdf

by Thomas Daniel Ardhali

Submission date: 09-Jun-2026 07:30PM (UTC+0530)
Submission ID: 2925561608
File name: sagar_thesis.pdf (2.25M)
Word count: 6477
Character count: 43802

Design and Performance Analysis of Gate All Around Nanowire FET for Suppression of Short Channel Effects

A Thesis Submitted in Partial Fulfilment of the Requirements for the Degree of

MASTER OF TECHNOLOGY

in

VLSI AND EMBEDDED SYSTEMS

by

Sagar Roy

(2K24/VLS/17)

Under the Supervision of

Sachin Dhariwal

Department of Electronics and Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daulatpur, Bawana Road, Delhi-110042

June, 2025

Department of Electronics and Communication Engineering
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Sagar Roy, Roll No. 2K24/VLS/17 hereby certify that the work which is being presented in the thesis entitled ***'Design and Performan Analysis of Gate All Around FET for Suppression of Short Channel Effects'*** in partial fulfilment of the requirements for the award of the Degree of Master of Technology (VLSI and Embedded Systems), submitted in the Department of Electronics and Communication Engineering, Delhi Technological University, is an authentic record of my own work carried out during the period from January 2026 to May 202 under the supervision of **Sachin Dhariwal.**

I have not submitted the matter presented in the thesis for the award of any other degree of this or any other Institute.

Candidate's Signature

Sagar Roy
(2k24/VLS/17)

Department of Electronics and Communication Engineering
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Bawana Road, Delhi-110042

CERTIFICATE BY THE SUPERVISOR

This is to certify that the work reported in this thesis entitled *"Design and Performance Analysis of Gate All Around FET for Suppression of Short Channel Effects"* has been carried out by Sagar Roy (2K24/VLS/17) under my supervision.

Supervisor's Signature

Sachin Dhariwal
ECE, DTU, Delhi

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Bawana Road, Delhi-110042

PLAGIARISM VERIFICATION

Title of the Thesis: **Design and Performance Analysis of Gate All Around FET for Suppression of Short Channel Effects**

Total Pages: _____

Name of the Scholar: **Sagar Roy**

Supervisor: **Sachin Dhariwal**

Department of Electronics and Communication Engineering

This is to report that the above thesis was scanned for similarity detection. The process and outcome is given below:

Software used: **Turnitin** Similarity Index: ____% Total Word Count: _____

Date: _____

Candidate's Signature **Signature of Supervisor(s)**

ACKNOWLEDGEMENT

I would like to express my sincere gratitude to all those who supported and guided me throughout the completion of this thesis work.

First and foremost, I would like to thank my supervisor and respected faculty members for their valuable guidance, continuous encouragement, and insightful suggestions during the course of this project. Their motivation and support helped me to successfully complete this research work.

I am also thankful to the Department of Electronics and Communication Engineering and my institute for providing the necessary facilities, laboratory support, and academic environment required for carrying out this work.

I would like to extend my heartfelt thanks to my friends and classmates for their cooperation, discussions, and constant encouragement during the preparation of this thesis.

Special thanks to my family members for their unconditional love, patience, and moral support throughout my academic journey. Their belief in me always motivated me to move forward during difficult times.

Finally, I, **Sagar**, express my gratitude to everyone who directly or indirectly contributed to the successful completion of this thesis.

Sagar Roy 2K24/VLS/17

ABSTRACT

The continual scaling of the semiconductor devices into the nanoscale regime has brought various issues in conventional planar MOSFET architectures. To mitigate these restrictions, new transistor topologies like Junctionless and Gate-All-Around (GAA) transistors have emerged as intriguing options for future nanoscale semiconductor applications.

Among the emerging device architectures, Junctionless Device and multi-gate transistor structures have attracted considerable attention due to their superior electrostatic characteristics and improved scalability. In these devices providing stronger control over the movement of charge carriers and reducing undesirable short-channel effects. The combination of this surrounding-gate configuration with a junctionless architecture offers an effective approach for enhancing device performance while simplifying fabrication complexity.

This work presents a detailed comparative study of Junctionless device employing different semiconductor channel materials and Proposed device structures were designed and analyzed using the SILVACO ATLAS 3D TCAD simulation platform. To ensure a fair comparison, identical geometrical dimensions, doping concentrations, and biasing conditions were maintained for all simulated devices [1].

The cylindrical GAA construction offers upgraded electrostatic since the gate electrode envelops the channel region, hence minimizing leakage current and suppressing short channel effects. The junctionless architecture also simplifies the manufacturing by avoiding abrupt source and drain junctions by homogeneous doping throughout the device structure.

A comprehensive evaluation of the selected semiconductor materials was carried out by extracting key electrical performance parameters, including V_{th}, SS, DIBL , $I_{ON, OFF}$, and the on off current ratio. The simulation results indicate that devices based on GaAs and InP exhibit enhanced current conduction capability and faster switching behavior owing to their high carrier mobility. In contrast, GaN-based devices demonstrate excellent leakage suppression and energy-efficient operation because of their wide bandgap characteristics. Silicon-based devices provide a balanced combination of performance, stability, and compatibility with existing semiconductor manufacturing technologies [5].

The comparative investigation shows that the suggested CGAA-JLFET architecture exhibits better electrostatic integrity, lower short channel effects and better switching performance.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

1.1 Study Background

One of the key driving forces for the speedy development of modern electron systems has been the constant downscaling of semiconductor devices. The transistor dimensions are constantly scaled down to obtain higher device density and better computing performance, with the need for compact, quicker and efficient integrated circuits increasing increasingly. Traditional mosfet have been an important component in the growth of microprocessors, memory circuits, communication systems and portable electronic devices for several decades [1].

Traditional field-effect transistors operate using p–n junctions formed through the selective introduction of dopant atoms into a semiconductor substrate, creating regions with different conductivity types. These junctions is vital role for regulating charge carrier transport between the S, D and channel regions. However, as device continue to scale into the small range, maintaining precise and abrupt junction boundaries becomes increasingly challenging. The continuous reduction of channel length brings the source and drain regions closer together, requiring extremely steep doping concentration profiles to ensure proper device operation. Achieving such highly controlled doping distributions is technologically demanding and introduces significant fabrication complexities. At advanced technology nodes, these challenges can adversely affect process variability, device performance, and manufacturing yield, thereby limiting the scalability of conventional transistor architectures [2].

Apart from the challenges associated with fabrication, continuous device miniaturization introduces several short-channel effects that degrade transistor performance. As the channel length decreases, the electrostatic influence of the gate over the channel weakens, resulting in undesirable phenomena such as threshold voltage instability, increased leakage current in the OFF state, DIBL, and deterioration of subthreshold characteristics. These effects adversely impact device reliability, switching behavior, and overall power efficiency, making further scaling of conventional transistor structures increasingly difficult. These effects degrade switching efficiency and increase static power dissipation and so standard planar transistor architectures are not suited for future applications.

To overcome the limitations associated with conventional transistor architectures, several advanced device structures have been proposed to enhance electrostatic control and reduce fabrication complexity. Among these, the Junctionless Device has emerged as a promising alternative for nanoscale applications. In contrast to traditional MOSFETs, which require carefully engineered pn junctions between the drain, source and channel regions, a junctionless transistor employs a uniformly doped semiconductor body throughout the device. Current conduction is controlled by the depletion and accumulation of charge carriers within the channel under the influence of the applied gate voltage. Since no abrupt junction formation is required, the fabrication process becomes less complex and less sensitive to variations in dopant distribution. This characteristic also helps mitigate random dopant fluctuation effects, thereby improving device scalability and reliability at advanced technology nodes [3].

A transistor architecture that combines a channel completely surrounded by the gate electrode with a uniformly doped junctionless channel offers significant advantages for nanoscale device applications. By integrating enhanced gate control with a simplified device structure, this architecture demonstrates excellent scalability, improved electrical performance, and suitability for future low-power and high-speed semiconductor technologies [4].

Hence, a complete examination of the CGAA-JLFET architectures employing different semiconductor materials is required to understand the applicability of the devices.

The main aim of this work is to investigate the comparative performance of Gate all around architectures employing different semiconductor channel materials. The paper studies the effect of Silicon (Si) and other materials on critical device characteristics under nanoscale operating circumstances.

The study mainly focuses on the analysis of threshold voltage behavior, characteristics, subthreshold performance via three-dimensional TCAD simulation. The effect of material qualities on electrostatic properties and switching efficiency is also studied in detail.

1.2 Purpose of the Work

The main aims of the present research endeavor are outlined as follows:

To design a 3D Gate-All-Around structure utilizing SILVACO ATLAS TCAD simulation software.

1. To research the influence of various semiconductor channel materials on the characteristics of nanoscale transistors.
2. For a comparative evaluation of several channel materials for switching capabilities, electrostatic stability and power efficiency. To examine the potential of the Cylindrical Gate-All-Around architecture For the suppression of SCE in nanoscale operation.

3. To find acceptable semiconductor materials for future low power, high speed and high frequency Junctionless transistor applications [6].

1.3 Thesis Structure

The thesis is break into six chapter, as follows:

- **Chapter_1** presents the background of the research, the motivation behind the study, the objectives of work.
- **Chapter_2** provides a detailed review of previous literature related to nanoscale technologies, junctionless devices, surrounding-gate architectures, and semiconductor material engineering techniques.
- **Chapter_3** explains the proposed device architecture, its operating mechanism, and the simulation methodology adopted for the investigation.
- **Chapter_4** describes the TCAD simulation framework, device specifications, physical models, and parameter extraction procedures employed in the study.
- **Chapter_5** presents the results and discusses the comparative performance of the proposed device using different semiconductor channel materials.
- **Chapter_6** summarize the major findings of the research and outlines potential directions for future work aimed at enhancing nanoscale transistor performance.

2. LITERATURE REVIEW

2.1 Introduction

The ever shrinking size of advanced semiconductor device is the the evolution of modern IC and electronic systems. In the nanoscale regime, the channel size of the MOSFET devices becomes compare to the device dimension and the conventional transistor designs are not expected to perform efficiently due to severe short channel effect (SCEs), leakage current, Vth degradation, and increased power dissipation. These issues restrict the performance and reliability of nanoscale devices and encourage researchers to design novel transistor topologies which can provide effective electrostatic control at shorter dimensions [7].

To avoid the limitations of earlier planar MOSFETs, several novel device topologies have been proposed such as FinFETs, Multi Gate FETs, Junctionless transistors, and Gaa transistors. Among these topologies, Junctionless Gate All Around transistors have attracted considerable attention due to their simplified fabrication process, improved electrostatic integrity, and excellent switching characteristics.

This chapter gives a detailed examination of traditional MOSFET structures, Junctionless transistors, FinFETs, Gate-All-Around devices, 3 dimensional GAA architectures, and semiconductor material engineering techniques reported in recent years. Furthermore, the limitations of present investigations and the research gap associated with cylindrical gate all around architectures are also discussed [8].

2.2 Standard MOSFET

The most important semiconductor devices utilized in modern digital and analog integrated circuits. A standard MOSFET consists of source, drain, gate, and substrate regions. The gate terminal controls the formation of inversion channel between the source and drain regions through an insulating oxide layer.

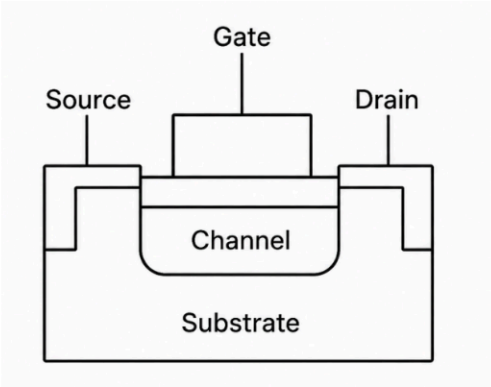

Figure 2.1: **Structure of conventional MOSFET**

In typical planar MOSFET architectures, the channel is controlled by the gate electrode from only one side. As device dimensions are reduced to the nanoscale regime, it becomes increasingly difficult to maintain proper electrostatic control over the channel. Consequently, several short channel effects arise, including threshold voltage reduction, increased leakage current, carrier mobility degradation, and drain-induced barrier lowering (DIBL). The major disadvantages of traditional MOSFETs are listed below:

1. Increased short channel effects at nanometer-scale dimensions.
2. Higher OFF-state leakage current.
3. Reduced electrostatic gate control.
4. Increased power dissipation.
5. Random dopant fluctuation effects.
6. Difficulty in forming abrupt source/drain junctions.

These constraints have encouraged the development of advanced transistor architectures with improved electrostatic confinement and reduced leakage characteristics.

2.3 Junctionless Transistor

The Junctionless Field Effect Transistor (JLFET) was proposed as an alternative to standard MOSFET architectures for simplifying fabrication and improving device scalability.

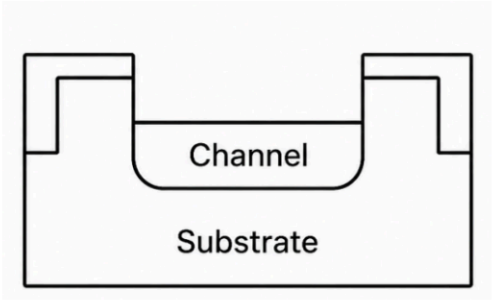

Figure 2.2: **Junctionless MOS transistor**

The operation of a Junctionless transistor relies on controlling the carrier concentration within a uniformly and heavily doped channel by means of gate-induced depletion and accumulation effects. By applying a gate voltage, the carrier concentration inside the channel can be controlled, thereby suppressing or enhancing current flow between the source and drain terminals.
Junctionless transistors advantages over conventional MOSFETs:

- Fabrication process due to elimination of abrupt junctions.
- Reduced process complexity and manufacturing cost.
- Improved electrostatic control.
- Better scalability for nanoscale technologies.
- Reduced random dopant fluctuation effects.
- Improved subthreshold characteristics.

These characteristics make Junctionless transistors promising candidates for future applications [11].

2.4 Gate-All-Around

GAA is most advanced transistor developed to overcome the limitation of conventional.

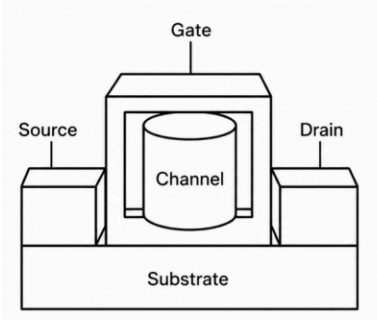

Figure 2.3: **Gate-All-Around transistor structure**

GAA transistors exhibit lessleakage current, reduced short channel effects, better SS, and enhanced current drivability.
Several studies have shown that GAA devices provide better electrostatic integrity compared to FinFET architectures, especially at highly scaled channel lengths. The surrounding gate configuration effectively suppresses drain-induced barrier lowering and improves switching performance [12].
The major advantages of GAA transistors are:

- Superior gate controllability.
- Reduced SCE.
- Lower off state.
- Improved ss
- Better scalability for sub-10 nm technologies.

These features make GAA architectures highly suitable for future improve performance transistor applications.

2.5 Semiconductor Materials

The electrical properties and performance of nanoscale transistors are heavily dependent on the semiconductor material utilized in the channel region. Semiconductor materials directly affect key device properties such as carrier mobility, leakage current, switching speed, thermal stability, power consumption, and breakdown voltage.
To overcome these limitations, researchers have investigated several alternative semiconductor materials. These materials exhibit superior carrier transport characteristics, thermal

conductivity, leakage current performance, and high-frequency operation compared to conventional silicon devices [10].

2.5.1 Silicon

Silicon is semiconductor material in modern electronic devices and integrated circuits. Its stable electrical characteristics, low fabrication cost, and compatibility with large-scale manufacturing technologies have made it the backbone of semiconductor technology. Silicon also forms a high-quality native oxide layer (SiO_2), which makes it highly suitable for MOSFET fabrication.

Silicon-based devices exhibit stable operation, moderate carrier mobility, and good thermal stability. The mature fabrication technology of silicon enables the production of highly integrated and cost-effective electronic circuits. These characteristics make silicon a preferred material for microprocessors, memory devices, sensors, and communication systems.

However, silicon also has certain limitations in nanoscale electronics. The electron and hole mobility of silicon are significantly lower than those of compound semiconductor materials. As a result, switching speed and current drivability are limited. As device dimensions shrink further, short channel effects and leakage current become more severe in silicon-based devices.

Despite these limitations, silicon continues to dominate the semiconductor industry due to its ease of fabrication, reliability, and low production cost.

2.5.2 Indium Gallium Arsenide InGaAs

Indium Gallium Arsenide is a another semiconductor material with extremely high electron mobility and excellent carrier transport properties.

The high electron mobility of InGaAs significantly improves switching speed and current conduction capability. InGaAs also reduces carrier scattering effects, thereby enhancing device performance at advanced technology nodes.

The properties of InGaAs-based transistors allow operation at higher frequencies and lower operating voltages compared to silicon devices. Therefore, the material is highly suitable for high-speed communication systems, radio frequency (RF) electronics, and advanced low-power integrated circuits.

Although InGaAs devices provide superior electrical performance, their fabrication is more complex and expensive than conventional silicon technology. Additionally, integrating InGaAs with existing silicon-based manufacturing processes remains a major challenge.

2.5.3 Gallium Nitride GaN

GaN exhibits excellent thermal stability, high breakdown voltage, and low leakage current characteristics.
Gallium Nitride is extensively used in RF amplifiers, radar systems, wireless communication devices, power electronics, and electric vehicle applications. Due to its superior power handling capability, GaN is considered a highly promising material for next-generation semiconductor devices.
Despite its excellent performance, GaN technology is comparatively more expensive and technically challenging to fabricate than silicon technology.
However, the high fabrication cost and material complexity of Indium Phosphide remain significant challenges for large-scale commercial applications.
Several studies have demonstrated that advanced semiconductor materials can significantly improve electrostatic control, subthreshold characteristics, switching speed, and leakage current behavior in nanoscale transistors compared to traditional silicon-based devices.

2.6 Research Gaps

To introduce a specific study on Junctionless transistors, FinFETs, and Gate-All-Around architectures, several limitations still exist in the available literature.
Most reported studies mainly focus on silicon-based devices or investigate only a limited number of semiconductor materials. Furthermore, systematic comparative studies involving multiple semiconductor materials under identical three-dimensional Gate-All-Around transistor structures remain limited [11].
Several previous works primarily concentrate on individual device parameters, whereas comprehensive TCAD-based analysis including short channel effects is still insufficient. Moreover, limited attention has been given to understanding the authority of alternative semiconductor materials on the electrostatic performance of 3-D Gate-All-Around Junctionless transistors [8].
Therefore, a detailed comparative TCAD simulation study involving Silicon, Gallium Nitride, Indium Phosphide, and Gallium Arsenide based 3-D structures is necessary to identify suitable channel materials for future nanoscale semiconductor applications. “‘

3. METHODOLOGY AND DEVICE STRUCTURE

Introduction

As semiconductor devices continue to scale into the nanometer regime, achieving effective control over the channel region becomes increasingly challenging. The reduction in device dimensions leads to several adverse effects. To address these limitations, advanced transistor structures have been developed to improve device performance and electrostatic control.

One such architecture is the Three Dimensional GAA layout. This configuration provides stronger gate control over charge carriers compared to conventional planar devices, thereby reducing leakage current and suppressing short-channel effects. Another Junctionless device, which employs a uniformly doped channel. [6].

This chapter describes the proposed structure, its operating principle, the criteria used for semiconductor material selection, and the simulation methodology adopted for performance evaluation. The overall framework employed for analyzing the Gate-All-Around architecture is also presented in detail.

Device Architecture

The proposed CGAA employs a cylindrical channel geometry surrounded entirely by the gate electrode, ensuring strong gate control and improved channel modulation. All the regions possess uniform doping of identical conductivity type and concentration. Consequently, the device operates without the formation of pn junction, which simplifies fabrication and minimizes junction-related effect.

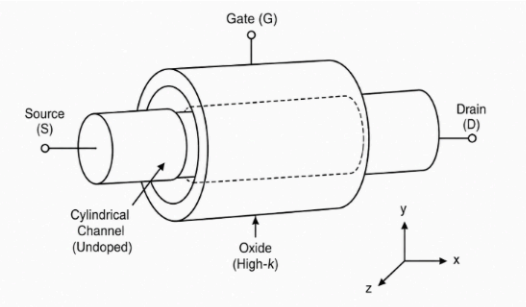

Figure 3.1: **Three dimensional Junctionless structure of Gate-All-Around FET**

The cylind geometry enables better electrostatic control,because the gate uniformly covers the channel from all directions.
The proposed structure is mostly composed of:

- Semiconductor channel (cylindrical construction)
- Source region
- Drain region
- Gate oxide layer
- Surrounding gate electrode

The uniformly doped channel simplifies production and mitigates the impact of random dopant fluctuation as compared to the typical MOSFET architectures.
The gate electric field depletes channel region and reduces the current conduction in the absence of any gate voltage.
The gate fully encloses the cylindrical channel, allowing for strong electrostatic confinement. These enhance switching properties and reduce leakage current significantly.

Advantages of the GAA Cylindrical Structure

The advantages of the Cylindrical Gate-All-Around (CGAA) structure over the conventional planar MOSFETs and FinFET architectures are summarized as follows:

- Enhanced electrostatic gate control
- Reduced leakage current

- Better subthreshold characteristics
- Better channel control
- Enhanced scalability to sub 10 nm technology

3.1 Choice of Semiconductor Material

The best possible quality of the semiconducting material has a strong effect on the performance of nanoscale transistors. In this work, four different semiconductor channel materials are considered for comparison [13].

3.1.1 Silicon

It is the bulk used material because of its advanced manufacturing technology, low price and stable electrical properties. It has very good reliability and good overall performance.

3.1.2 Gallium Arsenide

Gallium Arsenide exhibits superior carrier transport properties compared to conventional Silicon. The material possesses higher electron mobility and greater carrier saturation velocity, which facilitate faster charge within the channel region. These characteristics contribute to improved current conduction capability and enhanced switching performance.

3.1.3 Gallium Nitrde

Gallium Nitride is another semiconductor material having low leakage current, good thermal stability and better power efficiency.

3.1.4 Indium Phosphide (InP)

Indium Phosphide offers good carrier transport capabilities and high frequency performance. Therefore, it can be a good contender for RF and ultra-fast device applications.

3.2 Device Dimensions and Parameters

The suggested CGAA-JLFET dimensions and specifications are thoughtfully selected to improve electrostatic performance and short channel effect.

Parameter	Value
Channel Length	50 nm
Channel Radius	10 nm
Oxide Thickness	2 nm
Gate Material	Metal Gate
Channel Doping	Uniform Doping
Source/Drain Doping	Uniform Doping
Operating Temperature	300 K

Figure 3.2: **Simulation Guideline**

The electrostatic analysis is performed in cylindrical coordinate systems due to the cylindrical geometry of the device.

Drain Current Equation

The drain current is proportional to carrier mobility, channel dimensions and gate voltage.

$$I_D = q\mu_n nAE \tag{3.1}$$

3.3 Simulation Methodology

The major steps involved in the simulation process are described below.

1. **Definition of Cylindrical Device Geometry**

   The first stage of the simulation involves constructing the three-dimensional cylindrical structure of the proposed device.

2. **Definition of Material Parameters**

   After creating the device structure, the semiconductor material properties are specified. Different channel materials are incorporated individually into the device to evaluate their influence on electrical performance.

3. **Creation of a Mesh**

   A suitable mesh is generated throughout the device structure to enable accurate numerical computation. Fine mesh spacing is employed near critical regions such as the semiconductor-oxide interface and channel region, where large variations in electric field and carrier concentration are expected. A properly optimized mesh improves simulation accuracy while maintaining reasonable computational efficiency.

4. **Implementation of Doping Profiles**

   Uniform doping is applied to the source, drain, and channel regions of the junctionless transistor. The selected doping profile ensures proper device operation and facilitates the study of carrier transport characteristics.

5. **Selection of Physical Models**

   Appropriate physical models are activated in SILVACO ATLAS to accurately represent carrier transport and semiconductor behavior. These models account for various phenomena such as carrier mobility degradation, recombination mechanisms, concentration-dependent effects, and electric field variations. The selection of suitable physical models is essential for obtaining realistic simulation results and predicting device performance under practical operating conditions.

6. **Application of Bias Conditions**

   Electrical bias conditions is applied to investigate the device characteristics such as Id vs Vgs , Id vs Vds and other performance parameters are obtained by varying the terminal voltages over specified ranges. These biasing conditions allow the operating behavior of the transistor to be examined under different electrical environments.

7. **Extraction of Electrical Parameters**

   The simulated characteristics are analyzed to extract important device parameters provide valuable information regarding switching performance, power consumption, and overall device efficiency.

8. **Comparison of Different Semiconductor Materials**

   Finally, the extracted electrical parameters are compared for the different channel materials considered in this work. The comparative analysis helps identify the material that offers the most favorable combination of high current drive capability, low leakage current, improved electrostatic control, and enhanced switching performance. Based on these observations, the suitability of each semiconductor material for future nanoscale transistor applications is evaluated.

3.4 Used Models

Several important physical models have been integrate the simulation.

3.4.1 Auger Recombination Model

The model is valid for high carrier coint

3.4.2 Concentration Based Mobility Model

This model improves the accuracy of carrier transport study.
The drift-diffusion transport model describes the carrier transport due to electric fields and carrier concentration gradients.

3.5 Performance Parameters

The suggested device is tested on the basis of the important figure of merit such as cut in voltage, and other substhreshold effect.

4. SIMULATION SETUP AND EXECUTION

4.1 Introduction

Silvaco simulation plays a very essential role in the study and optimization of semiconductor devices. As the size of transistors shrinks, experimental manufacture becomes increasingly complicated and expensive.
In this study, numerical simulations are performed using the SILVACO ATLAS environment to analyze a three-dimensional Junctionless architecture, where the gate material encloses the channel from all directions. With semiconductor channel materials such as Silicon, Gallium Nitride, Gallium Arsenide. The simulations are done under various biasing settings to get figure of merit.
In this chapter, the detailed simulation setup, device implementation process, physical models, biasing conditions and extraction methods for the proposed Gate All Around analysis are presented.

4.2 Implementation of the Device Structure

The SILVACO ATLAS is used with cylindrical geometry in the case of the Three Dimensional Junctionless Structure. All region are uniformly with n impurities to avoid formation of junction.
The implementation procedure basically includes:

1. Device geometry definition
2. Mesh generation
3. Material specification
4. Doping profile determination
5. Electrode positioning

6. Physical model selection
7. Imposition of bias condition
8. Simulation run
9. Parameter extraction

4.3 Device Dimensions

The suggested device parameters are chosen carefully for better control.

Parameter	Value
Channel Length	50 nm
Source Length	25 nm
Drain Length	25 nm
Channel Radius	10 nm
Gate Oxide Thickness	2 nm
Gate Material	P^+ Polysilicon
Gate Work Function	5.4 eV
Oxide Material	SiO_2
Channel Doping	$1 \times 10^{18}\ cm^{-3}$
Source/Drain Doping	$1 \times 10^{18}\ cm^{-3}$
Operating Temperature	300 K

Figure 4.1: **Device Structural Parameter**

The adoption of a cylindrical channel configuration provides stronger electrostatic confinement. Such a structure contributes to efficient carrier modulation and reduced short-channel effects in nanoscale devices. For a meaningful comparative analysis, all investigated semiconductor channel materials are implemented using the same device geometry, doping concentration, and simulation conditions.
Semiconductor materials have diverse electrical properties such as Eg, un and saturation velocity. These factors substantially influence the performance of the gadget.

Property	Si	GaAs	GaN	InP
Bandgap (eV)	1.12	1.42	3.4	1.35
Electron Mobility (cm^2/Vs)	1400	8500	2000	5400
Dielectric Constant	11.8	13.1	9.5	12.5
Saturation Velocity (cm/s)	1×10^7	2×10^7	2.5×10^7	2.2×10^7

Figure 4.2: **Material Properties of Semiconductor Channel Materials**

The chosen materials show very varied carrier transport and electrostatic properties, which allow a comparative study of the speed, leakage current, and short-channel effects.
Higher carrier mobility of semiconductor materials leads to improved current drivability and switching speed, while wide bandgap materials such as GaN have reduced leakage current and improved thermal stability.

4.4 Device Structure

The three dimensional Cylindrical Gate All Around Junctionless layout.

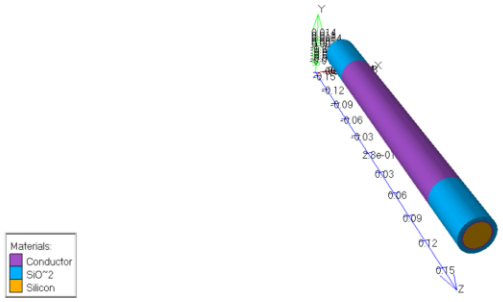

Figure 4.3: **Device Structure**

5. RESULTS AND DISCUSSIONS

5.1 INTRODUCTION

The execution of advanced nanoscale transistors is strongly influenced by factors such as device geometry, gate-to-channel electrostatic coupling, and the physical properties of the material. As dimension become small, the selection of an appropriate semiconductor material becomes increasingly important for achieving improved switching behavior, reduced leakage current, and enhanced overall device efficiency. In the present study, a three Dimensional strucutre is employed as the reference device structure to investigate the impact of different semiconductor channel materials on transistor performance. Calculation using the SILVACO ATLAS TCAD simulation platform to evaluate devices incorporating alternate channel materials.

The extracted results are subsequently compared to identify the channel material that offers the most favorable balance between high drive current, low power dissipation, and improved electrostatic control. This comparative analysis helps assess the potential of various semiconductor materials for implementation in next-generation 3D Structure based electronic devices.

5.2 Features of Si-Based 3D Gate all around Junctionless

The electrics characteristics of the Silicon-based were investigated by performing 3D TCAD simulations in SILVACO ATLAS.

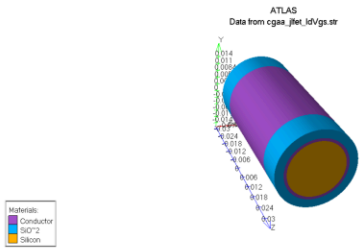

Figure 5.1: **Device Structure of Silicon**

The transfer characteristics ($I_D - V_{GS}$) were measured at $V_{DS} = 0.01$ V drain voltage.
The extracted threshold of Si-based Cylindrical gate all around is around:

$$V_{th} = 0.622\ v \tag{5.1}$$

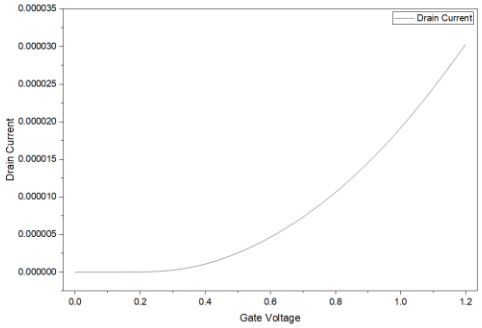

Figure 5.2: **Id versus Vgs**

The extracted subthreshold slope is:

$$SS = 64.96\ mV/dec. \tag{5.2}$$

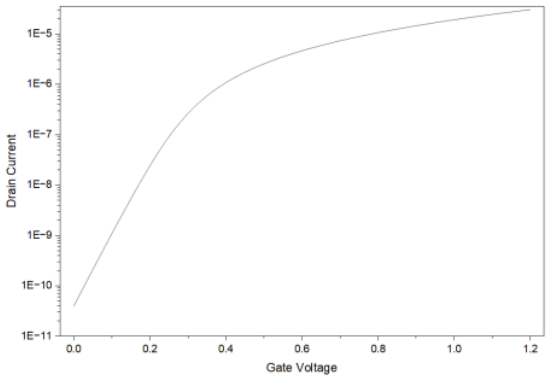

Figure 5.3: **Subthreshold slope of 3-D Si based**

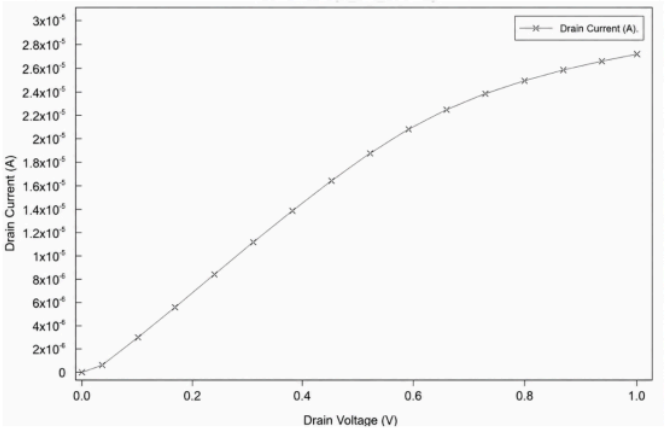

Figure 5.4: **Output characterisitcs of 3-D Si based**

The Drain-Induced Barrier Lowering is :

$$DIBL = 44.85\, mV/V \tag{5.3}$$

5.3 GaAs Based 3D Gate all around junctionless characteristics

The 3D structure of the GaAs based Cylindrical Gate All Around generated in SILVACO ATLAS.

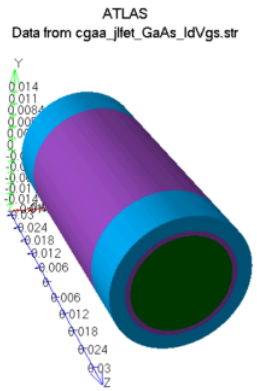

Figure 5.5: **Device layout (GaAs)**

Gallium Arsenide (GaAs) is a semiconductor material known for its superior electron mobility and high-speed carrier transport properties.

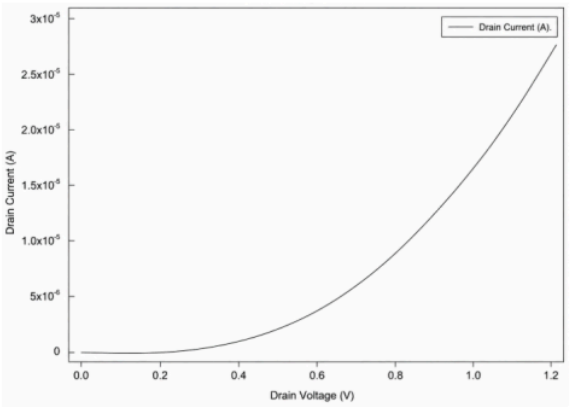

Figure 5.6: **Transfer characteristics of GaAs based Cylindrical GAA**

The extracted threshold voltage for the GaAs based device is:

$$V_{th} = 0.82\ V \tag{5.4}$$

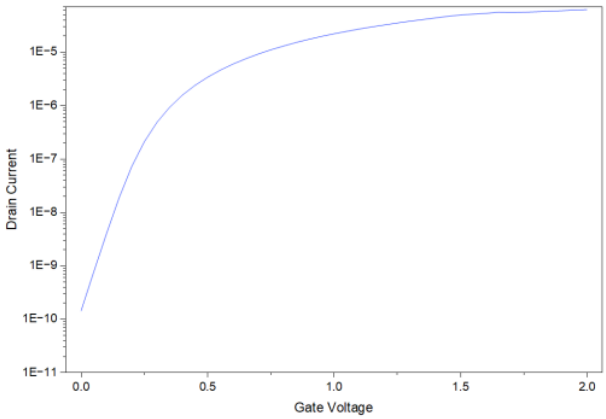

Figure 5.7: **GaAs Subthreshold Slope**

The subthreshold slope is computed as:

$$SS = 64.48\ \mu V/dec \tag{5.5}$$

The Drain Induced Barrier Lowering (DIBL) is computed as:

$$DIBL = 30.60\ mV/V \tag{5.6}$$

The ON-current of GaAs based devices is higher due to better carrier mobility and better carrier transport ability.

5.4 Characteristics of Gallium Nitride Based 3D Gate all around junctionless

The 3D structure of the Gallium Nitride based Cylindrical Gate All Around generated in SILVACO ATLAS.

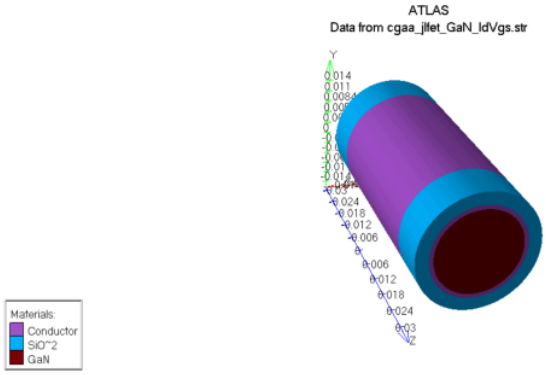

Figure 5.8: **Design of GaN**

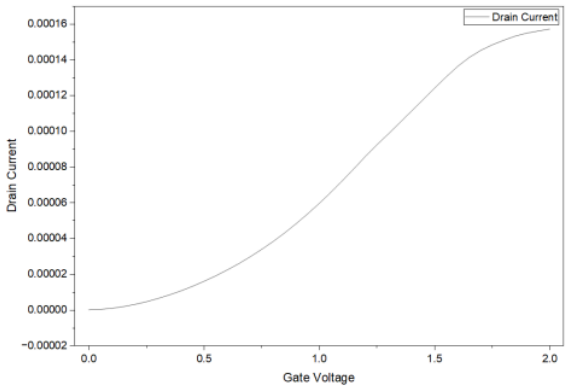

Figure 5.9: **GaN Cylindrical Gate All Around**

The take out threshold volt. by:

$$Vth = 0.734 \tag{5.7}$$

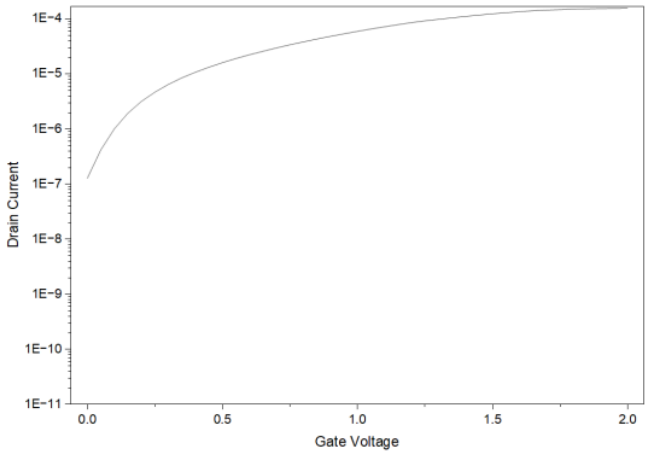

Figure 5.10: **Substhreshold slode of GaN Cylindrical Gate All Around**

The sub-threshold slope obtained is:
The slope SS is 68.35 mV/decade.

$$SS = 68.35\ mV/dec \tag{5.8}$$

The extracted value of DIBL is:

$$DIBL = 40.36\ mV/V \tag{5.9}$$

The wide bandgap nature of Gallium Nitride makes the OFF-current of GaN based devices substantially lower.

5.5 Characteristics of Indiun Phosphide 3D Gate all around junctionless

The 3D structure of the Indium Phosphide Gate All Around generated in SILVACO ATLAS.

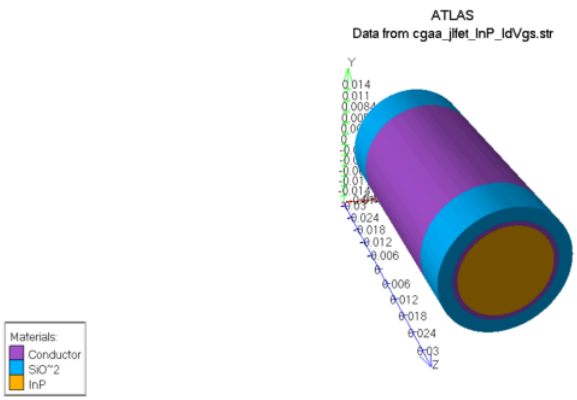

Figure 5.11: **Device Structure of INP**

Indium Phosphide is another key semiconductor material which has good carrier transport capabilities and high electron mobility.
The threshold voltage extracted is:

$$V_{th} = 0.581\ V \tag{5.10}$$

The subthreshold slope is given by:

$$SS = 66.84\ mV/d \tag{5.11}$$

The DIBL value is obtained as:

$$DIBL = 39.42\ mV/V \tag{5.12}$$

The obtained results indicate that InP based devices are very appropriate for high speed and RF semiconductor application.

5.6 Transfer Characteristics Analysis

This chapter, the comprehensive modelling results are presented and effect of several semiconductor channel materials on the performance of the proposed CGAA-JLFET structure are discussed.
The transfer characteristics are the depend of (I_D) on (V_{GS}) for a constant (V_D). These parameters give useful information with respect to threshold voltage, leakage current, switching behaviour.
GaAs and InP based devices have higher drain current due to higher carrier mobility and better carrier transport properties when compared to Silicon. Gallium Nitride based devices have relatively low leakage current because of the broad band gap nature of Gallium Nitride.

The surrounding gate structure gives very good electrostatic control to the cylindrical channel region, which results in a better switching behavior and minimized short channel effects.

5.7 Discussion

The simulation results clearly show that the choice of semiconductor material has a significant effect on the performance of proposed device (CGAA-JLFETs). Different semiconductor materials exhibit distinct electrical characteristics due to variations in carrier mobility, bandgap energy, and transport properties.

Diverse Materials provide better mobility compared to Silicon, resulting in improved carrier transport and enhanced ON-current performance. Among all the materials considered, InP demonstrates the highest ON-current and very high speed.

Gallium Nitride (GaN), owing to its wide bandgap nature, exhibits superior leakage current suppression and improved power efficiency. The lower OFF-current observed in GaN-based devices indicates better control over leakage mechanisms. The cylindrical Gate-All-Around (GAA) architecture further enhances electrostatic gate control by surrounding the channel region from all directions. This structure provides better device scalability for nanoscale transistor technologies.

5.8 Summary

This segment presents a equivalent study a three-dimensional Gate-All-Around Junctionless Device employing different semiconductor channel materials. In the Gate-All-Around architecture, the electrode completely surrounds the cylindrical channel region, providing enhanced electric controls. The performance of the device is evaluated through TCAD simulations, and the results obtained demonstrate the ascendancy of the properties of the channel on the characteristics of the proposed transistor. The study indicates that the 3D cylindrical GAA structure is improve performance nanoscale.

6. FUTURE SCOPE AND CONCLUSION

6.1 Summary

In the present work a detailed comparative analysis of Cylindrical Junctionless Transistor (CGAA-JLFETs) using different semiconductor channel materials using SILVACO simulation.

The cylinder Gate-All-Around construction gives the better control to the whole surrounding of the cylindrical channel region by the gate. This encircling gate shape considerably decreases short channel effects and enhances switching characteristics as compared to typical planar transistor architectures.

The Junctionless transistor configuration also simplifies the fabrication process, because it does not require abrupt source/drain junction creation.

Diverse semiconductor channel materials device performance, electrical characteristics of the proposed Junctionless FET architectures were investigated under the same simulation settings. Important electrical data such as threshold voltage, transfer characteristics, output characteristi, subthreshold slope, DIBL, and ONOFF current ratio were retrieved and compared.

The simulation results indicate the considerable influence of the semiconductor material selection on the performance of nanoscale transistor architectures.

Silicon based devices showed stable and balanced overall performance with minimal ON-current, good electrostatic control and dependable switching characteristics. Although the carrier mobility in Silicon is lower than in III–V semiconductor material, the established manufacturing process and reliable device properties of Silicon continue to make it an important semiconductor material for integrated circuit applications.

From the subthreshold slope study, it was found that the proposed architectures have sharp switching characteristics and reduced leakage behavior due to strong gate controllability. The cylindrical construction improves electrostatic confinement and greatly enhances device performance at nanoscale levels.

The comparative analysis provides evidence that:

- GaAs and InP based CGAA-JLFETs have superior switching speed and current drivability.
- GaN based devices have excellent leakage current suppression and improved power efficiency.
- Silicon based devices have balanced overall performance and stable device operation.
- The Cylindrical Gate-All-Around architecture strongly suppresses the short channel effects.
- Junctionless architectures ease the fabrication and improve the scalability for future nano-scale technologies.

6.2 Future Scope

The proposed CGAA-JLFET architectures exhibit the improved electrical and electrostatic characteristics, although a number of additional research opportunities still exist for future research.

Future works may cover the following areas:

Investigation of CGAA-JLFET devices below 10 nm for next-generation ultra-scaled semiconductor technologies.

- use of relative permitivity to enhance the cg and lower the leakage current.
- Temperature dependent features and thermal effect analysis for high power applications.
- Study of quantum confinement effects and ballistic transport mechanisms in the ultra-scaled dimensions.
- Optimization of channel dimensions, oxide thickness and gate work function for improved device performance
- Comparative analysis with other III–V semiconductor materials and two-dimensional materials.
- Reliability concerns including hot carrier effects, bias temperature instability are studied.
- Investigation on dual material gate and multi-oxide engineering strategies for further mitigation.

Continued scaling of nanoscale semiconductor technology will also demand new transistor topologies with superior electrostatic control, lower power consumption, and higher switching performance. The proposed Cylindrical Gate-All-Around Junctionless transistor architectures provide promising platform for future research and development of semiconductor devices.

Bibliography

[1] J. P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electronics*, vol. 48, no. 6, pp. 897–905, 2004.

[2] Jean-Pierre Colinge et al., "Nanowire transistors without junctions," *Nature Nanotechnology*, vol. 5, pp. 225–229, 2010.

[3] D. Hisamoto, W. Takeuchi, H. King, Y. Tosaka, and H. Iwai, "FinFET - A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Transactions on Electron Devices*, vol. 47, no. 12, pp. 2320–2325, 2000.

[4] C. Auth et al., "A 10 nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors," *IEEE International Electron Devices Meeting*, pp. 29.1.1–29.1.4, 2017.

[5] N. Singh et al., "High-performance fully depleted silicon nanowire (diameter 5 nm) gate-all-around CMOS devices," *IEEE Electron Device Letters*, vol. 27, no. 5, pp. 383–386, 2006.

[6] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 2009.

[7] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Wiley Publications, 2007.

[8] Silvaco International, *ATLAS User's Manual: Device Simulation Software*. Silvaco Inc., USA.

[9] M. Lundstrom, *Fundamentals of Nanotransistors*. World Scientific Publishing, 2017.

[10] D. J. Frank et al., "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, 2001.

[11] R. Chau et al., "Benchmarking nanotechnology for high-performance and low-power logic transistor applications," *IEEE Transactions on Nanotechnology*, vol. 4, no. 2, pp. 153–158, 2005.

[12] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, 2011.

[13] B. Razavi, *Fundamentals of Microelectronics*. Wiley Publications, 2014.

[14] D. A. Neamen, *Semiconductor Physics and Devices*. McGraw-Hill Education, 2012.

List of Abbreviations

Abbreviation	Full Form
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
GAA	Gate-All-Around
JLFET	Junctionless Field Effect Transistor
CGAA-JLFET	Cylindrical Gate-All-Around Junctionless FET
TCAD	Technology Computer-Aided Design
DIBL	Drain-Induced Barrier Lowering
SS	Subthreshold Slope
ON/OFF Ratio	ON-State to OFF-State Current Ratio
SRH	Shockley–Read–Hall
RF	Radio Frequency

sagar_thesis.pdf

ORIGINALITY REPORT

7%	5%	3%	6%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Submitted to Delhi Technological University Student Paper	3%
2	dspace.dtu.ac.in:8080 Internet Source	1%
3	Submitted to University of Wales Institute, Cardiff Student Paper	1%
4	Submitted to The Northcap University Student Paper	<1%
5	Santosh K. Kurinec, Krzysztof Iniewski. "Nanoscale Semiconductor Memories - Technology and Applications", CRC Press, 2017 Publication	<1%
6	arccjournals.com Internet Source	<1%
7	Pooja Srivastava, Aditi Upadhyaya, Shekhar Yadav, Chandra Mohan Singh Negi, Arvind Kumar Singh. "Analysis of Nanoscale Short Channel Effects in Cylindrical Gate-All-Around	<1%

Junctionless FETs and Performance Enhancement with GaAs and III–V Materials for Low-Power, High Frequency Applications", Electronics, 2025
Publication

8	Submitted to Liverpool John Moores University Student Paper	<1%
9	docplayer.net Internet Source	<1%
10	d-nb.info Internet Source	<1%

Exclude quotes	On	Exclude matches	< 14 words
Exclude bibliography	On		