ANALYSIS OF LOW-POWER 2:1 MULTIPLEXER USING DML AND LDML TECHNIQUES

by Nikita Anand

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ANALYSIS OF LOW-POWER 2:1 MULTIPLEXER USING DML AND LDML TECHNIQUES

A Thesis Submitted in Partial Fulfilment of the Requirements for the Degree of

MASTER OF TECHNOLOGY

in

VLSI AND EMBEDDED SYSTEMS

by

Nikita Anand

(2K24/VLS/18)

Under the Supervision of

Dr. Deva Nand

(Associate Professor)

DTU, Delhi

Department of Electronics and Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daulatpur, Bawana Road, Delhi-110042

June, 2026

Department of Electronics and Communication Engineering
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Nikita Anand, Roll No. 2K24/VLS/18 hereby certify that the work which is being presented in the thesis entitled *'Analysis of Low-Power 2:1 Multiplexer using DML and LDML Techniques'* in partial fulfilment of the requirements for the award of the Degree of Master of Technology (VLSI and Embedded Systems), submitted in the Department of Electronics and Communication Engineering, Delhi Technological University, is an authentic record of my own work carried out during the period from January 2026 to May 2026 under the supervision of Dr. Deva Nand.

I have not submitted the matter presented in the thesis for the award of any other degree of this or any other Institute.

Candidate's Signature

Nikita Anand
(2K24/VLS/18)

Department of Electronics and Communication Engineering
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Bawana Road, Delhi-110042

CERTIFICATE BY THE SUPERVISOR

This is to certify that the work reported in this thesis entitled *"Analysis of Low-Power 2:1 Multiplexer using DML and LDML Techniques"* has been carried out by Ms. Nikita Anand (2K24/VLS/18) under my supervision.

Supervisor's Signature

Dr. Deva Nand
Associate Professor
ECE, DTU, Delhi

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Date: Nikita Anand

Place: Delhi 2K24/VLS/18

ABSTRACT

Power leakage problem has become a challenging issue for modern CMOS digital logic circuits as it becomes more significant in deep-submicron technology due to sub-threshold currents. Here, a low power 2:1 multiplexer circuit is developed using the novel combination of two methodologies viz. Dual Mode Logic (DML) and LECTOR Dual Mode Logic (LDML). The basic concept of DML involves use of one MODE signal to switch a circuit between two modes namely low power static mode and fast dynamic mode. However, the LDML technique uses leakage control transistors of LECTOR method in combination with DML such that there will always be one transistor operating in its cutoff state independent of any input pattern. Both designs were realized and analyzed using LTspice by taking PTM library for 90 nm and 45 nm CMOS processes with a supply voltage of 1.2 V. The results have shown that LDML Type A consumes the least power of 246.1 nW and power-delay product (PDP) is 4.52 fJ in 90 nm technology—about ∼99% power savings compared to DML.

2:1 Multiplexer is one of the most common combinational modules found in processors, memory controllers, communication chips, and many other digital devices. Subthreshold leakage, defined as the current that flows through an OFF-state transistor, has become the main power dissipation factor when the gate channel lengths are less than 50 nm and can contribute 30–50% of the overall power consumption in standby or inactive conditions. The traditional solutions, like transistor stacking that uses the body effect to minimize leakage, cannot be employed anymore due to increased gate-oxide tunneling at advanced technology nodes. This paper starts by analyzing the basic structure of 2:1 Multiplexer based on NAND and NOT gates in conventional CMOS technology and then gradually applies the LECTOR (LEakage Control TransistOR) mechanism, Dual Mode Logic (DML) and their combination (LDML) to improve power dissipation, propagation delay, and Power-Delay Product (PDP). It was experimentally demonstrated that the most efficient design from all variants examined is LDML Type A which exhibits more than two orders of magnitude lower PDP than domino logic floor documented in scientific literature for both 90 nm and 45 nm process technologies.

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LIST OF SYMBOLS, ABBREVIATIONS AND NOMENCLATURE

CMOS : Complementary Metal-Oxide Semiconductor

DML : Dual Mode Logic

LDML : LECTOR-based Dual Mode Logic

LECTOR : LEakage Control TransistOR

LCT : Leakage Control Transistor

MUX : Multiplexer

PDP : Power-Delay Product

PTM : Predictive Technology Model

MCML : MOS Current Mode Logic

IoT : Internet of Things

FPGA : Field-Programmable Gate Array

DRC : Design Rule Check

LVS : Layout Versus Schematic

SoC : System-on-Chip

V_{DD} : Supply Voltage (1.2 V in this work)

V_{TH} : Threshold Voltage

t_{phl} : Propagation delay, high-to-low transition

t_{plh} : Propagation delay, low-to-high transition

CHAPTER 1

INTRODUCTION

The 2:1 Multiplexer is one of the simplest components of a digital circuit, taking two data inputs and selecting one for output depending on an individual selection line. But it pops up in a multitude of uses — from arithmetic circuits which select between operands, to memories which transfer data from many banks, to communication hardware which selects the required signals. As such, any small improvement in the energy efficiency of each instance would have considerable impact when designing chips that include hundreds or thousands of such circuits.

In this thesis, we examine the problem of designing a completely new architecture for the simple 2:1 multiplexer, but our aim is to minimize its energy consumption. Our goal is to create an implementation where we can lower the leakage current, which continuously drains energy from the device irrespective of whether the device is performing any operations. In doing so, we propose a novel methodology, which integrates dual mode logic circuits along with leakage control through LECTOR. We implement our proposal and test it through simulations in two separate technologies.

1.1 Motivation and Background

However, miniaturization to reach smaller channel sizes has introduced an issue that was of little importance for the past several decades — leakage. While in the case of larger microelectronic components, transistors were turned off completely, in nanometer-scale designs the leakage is unavoidable. Due to the need to reduce the threshold voltage to minimize switching times in modern designs, there is considerable current that passes through the transistors while the gate voltage is lower than its threshold value. As this leakage current depends on the threshold voltage exponentially, even slight lowering of it results in extremely high leakage values.

While leakage issues become crucial for mobile phones and computers operating in stand-by mode, they seem rather trivial in permanently working systems. How-

ever, for devices which are constantly turned on, leakage currents account only for a minor additional power consumption. Yet, for mobile applications, when a device consumes power during hours of operation in stand-by mode, the power consumption due to leakage exceeds that of normal operations. Thus, leaving a smartphone turned on on your desk drains the battery mainly due to the leakage from billions of idle transistors.

Multiplexers are in data paths that do not conduct data during certain clock cycles, so they are especially prone to this issue. If there is a steady state of the selection line signal, then the transistors in the inactive path leak constantly. Some solutions, such as stacking transistors into pairs in order to minimize their leakage by using the body effect, partially solve this issue. However, the effect is lost due to gate-oxide tunneling leakage, which appears in newer technology nodes.

This justifies looking into other alternatives outside of standard CMOS designs and logic families that take care of minimizing leakage currents as their inherent property.

1.2 Research Focus: DML and LDML-Based MUX Design

At the heart of this work lies the motivation to redesign one simple circuit, the 2:1 multiplexer, in what normally would have been done using the normal CMOS logic by employing two methods specifically devised to tackle the leakage issue in a more disciplined manner.

The first such technique is known as Dual Mode Logic or DML. DML works based on the observation that some gates do not need to always operate at maximum speed. If one could control a gate externally via a single MODE line to toggle between two operation modes, namely a power-conserving mode for use when speed is of no consequence and a high speed high power-consuming mode for when bursts of speed are required, then power savings could be achieved in those parts of the circuit where performance is secondary. DML accomplishes this feat by managing precharge and evaluation using footer transistors. During the static mode, a gate precharges its output and maintains it; however, upon being signaled by MODE signal, it executes the logic in a fast mode. Type-A and Type-B DML differ in terms of precharge method used, which is significant

for delay.

The second technique, known as LECTOR, works differently. Instead of varying the behavior of the gate temporally, LECTOR incorporates two carefully located transistors into every gate such that, irrespective of the input values, at least one transistor in the path remains close to cutoff. Consequently, the leakage current drops significantly – around 80%, as reported earlier in the literature – with a relatively small overhead in terms of both area and delay.

Together, the two techniques form LDML, a gate architecture that not only dynamically controls the mode of operation as DML does but also reduces leakage currents continuously as in LECTOR. Simulations confirmed this assumption and provided precise values for two process technologies.

1.3 Objectives and Contributions

Designing, developing, and evaluation of ultra-low-power consumption of 2:1 multiplexer using both DML and LDML approaches, along with a comparative study of these approaches and a CMOS approach will be the main objective of this thesis. The important objectives that are intended to be achieved from this research include the following:

- Constructing the 2:1 multiplexer using CMOS conventional circuits with NAND and NOT gates and analyzing its power, delay, and PDP at 90 nm and 45 nm technology nodes.
- Constructing 2:1 multiplexers with DML Type A and Type B approaches and measuring their power, delay, and PDP at 90 nm and 45 nm technology nodes.
- Developing 2:1 multiplexers with LDML Type A and Type B approaches by integrating the LECTOR transistor within the DML architecture and assessing the resulting performance.
- Simulating the above mentioned five circuits with LTspice using Predictive Technology Model (PTM) library and evaluating their performances at 1.2 V supply voltages.
- Comparing the outcomes from all of these circuits and nodes to find out the best design for ultra-low-power consumption.

- Placing these outcomes in context of previous researches and explaining how this research contributes further to the field, particularly by providing first PDP analysis of the LDML 2:1 multiplexer.

1.4 Structure of the Thesis

The thesis is structured in five chapters:

- Chapter **1** lays down the motivations, identifies the research objective, and sets up the scope.
- Chapter **2** reviews the related literature starting from the basic concepts of scaling, leakage in scaled CMOS technology, to traditional approaches, LECTOR, DML, and their hybridization.
- Chapter **3** explains the methods of designing and simulating the circuits — the way each circuit is designed, the choice of transistors' sizes, the procedure of simulations and the results obtained.
- Chapter **4** describes future work, suggests possible improvements, compares results with the previous work, and provides suggestions for application and layout design.
- Chapter **5** draws the conclusions of the thesis.

CHAPTER 2

LITERATURE REVIEW

2.1 The Problem of Power in Scaled CMOS Circuits

Smaller transistors were unambiguously an improvement for the vast majority of the history of semiconductors. Small transistors switched faster, had less capacitance, used less power, and provided more function per chip area than large transistors. For decades, this trend was reliable enough to guarantee predictable performance gains at each process technology advance. At some point, however, in the neighborhood of the 90 nm node, things started getting complicated — more complicated by the day.

However, reducing the size of the transistor is not a straightforward matter of shrinking the device's proportions. In addition, the threshold voltage — the value at which the device switches from its off state to on — should be reduced to make sure the gate overdrive is feasible and enable fast switching. Unfortunately, reducing the threshold voltage also results in an unwanted consequence, which is becoming increasingly hard to ignore: more current can flow through the device even when there is no charge applied to the gate. This effect, known as subthreshold leakage, occurs since the transistor does not shut off fully and is actually in a state of weak conduction.

The mathematical analysis for this phenomenon is thoroughly defined. As the leakage current below threshold increases dramatically with a lowering of the threshold voltage, even a difference of a few dozen millivolts could result in the leakage increasing significantly, perhaps even up to several times the original level. In today's complex chips, which have billions of transistors, the overall leakage current becomes a significant portion of the total energy consumed – even potentially larger than the power used for computing operations. That is why a phone left on the table without its screen operating still consumes energy from its battery throughout the day.

Furthermore, there is a second leakage source which comes into play in the case of advanced nodes, called gate-oxide tunneling current. As the thickness of the insulator under the gate becomes reduced in order to control the channel, electrons can

tunnel across the insulator from the gate terminal to the channel terminal, leading to a direct tunneling current leakage from the gate to the channel. Below 45 nm nodes, this effect cannot be ignored anymore [1].

2.2 How a Multiplexer Works

However, before delving into the reduction technique, one must know why the multiplexer makes for an interesting choice when it comes to power consumption reduction. The simplest definition of a multiplexer is an IC which selects between two different inputs depending on the value of a control signal and then connects whichever input was selected with the output. It can be described by the formula

$$Y = S \cdot A + \overline{S} \cdot B \tag{2.1}$$

where, if the signal S is set to 1, $Y = A$, and vice versa. The multiplexer described above is a purely combinational circuit — it contains no memory elements and operates in real time.

Nevertheless, multiplexers are some of the most common circuits used in the field of digital circuits. Within the data path of a processor, the multiplexer selects between registers, immediate operands, and the feedback paths. Within memory circuits, the multiplexer selects whether a particular memory bank or memory row is accessed. Within FPGA architectures, each logic circuit is essentially a multiplexer tree. Finally, within communication circuits, multiplexers route data streams between two different points.

2.3 Early Approaches to Leakage Control

Once the issue of leakage was realized to be a major problem from the point of view of power, there have been many ways used to solve this problem. The oldest one and most intuitive way is that of transistor stacking.

Transistor stacking works on a very simple principle: If there are two transistors that happen to be in the off state and these two are connected in a series manner, then there will be less leakage than when only one off state transistor is present in the conduct-

ing pathway. This principle is called the body effect, whereby when the first transistor stacks and allows a small amount of current through it, then this current develops some voltage across the intermediate node of these two transistors.

A reduction in leakage by an order of magnitude or more can be achieved through stacking for two transistor stacks in an ideal situation. Nonetheless, the effectiveness of stacking greatly relies on the input vector that will be applied to the gate. In some cases, the stacking action will be evident, but in other cases, not all the transistors will be off such that there is no stacking advantage realized. It must be pointed out that in advanced technology nodes, gate-oxide tunneling does not have a response to the body effect in the manner sub-threshold leakage has. When gate leakage equals sub-threshold leakage or exceeds it, as it does at 45 nm and below, stacking loses much of its effectiveness [1].

Another approach involves the use of multiple threshold CMOS where critical path circuits use low V_{TH} transistors, while noncritical path circuits use high V_{TH} transistors. The sleep transistor involves the insertion of a high threshold transistor in series with the power supply to stop leakage during the idle period. While this is a feasible method, it results in wake up time and ground bounce issues. However, each of these methods had certain strengths; unfortunately, there was no single method that met all of the required criteria. It was in this regard that the need arose for LECTOR.

2.4 The LECTOR Technique

LECTOR (LEakage Control TransistOR) method was put forward as an improvement on older leakage reduction techniques [2]. Its main feature is that it automatically reduces leakage, in the absence of any input signal, and is independent of the logic input signal value.

It works as described below. Two more transistors are added into the circuit in each gate; these are placed inside the pull up network and the pull down network, respectively. They are termed leakage control transistors, or LCTs. Their distinguishing features include the connections on their gate terminals, wherein the gate terminal of the PMOS LCT is connected to a point on the pull down network and that of the NMOS LCT is connected to a point on the pull up network.

As a result, whichever combination of inputs we consider, one of the two LCTs will be operating close to the cutoff voltage level. Transistor behavior near the cutoff voltage implies very high resistance, and thus, only a minute amount of current can flow through it. Since one of the two LCTs will be close to the cutoff voltage regardless of the input combination used, the resistance in the leakage path from the voltage supply source to the ground will be relatively high, no matter what. That is what input independence means.

As far as real life goes, the experiments done on the industry benchmark circuits have proven that, on average, LECTOR lowers the leakage current by about 79%, while some particular gates reduce leakage more than that, depending on their structure [2]. There is an area cost of two extra transistors per logic gate, and the increase in the propagation delay is negligible because of the additional series resistance introduced by LCTs.

One major benefit of LECTOR is that it can work with ordinary CMOS technology without threshold voltage tuning, body biasing, or any process changes. Thus, it can be readily implemented with standard design flows and technology libraries.

2.5 Dual Mode Logic: Background and Description

While DML is based on a different insight about energy consumption [3], it addresses another interesting case. Namely, in practice, often a lot of time in the operation of a circuit passes by without any computations taking place or with very little activity. Hence, if we could make a gate slow down during the idle periods to save energy, and then speed up again when necessary, we would achieve significantly reduced average energy consumption compared to circuits operating at peak capacity all the time.

This flexibility is made possible by the use of a unique external control signal called MODE. In static mode, MODE holds a low value, and therefore the gate functions in such a way that the output node is either precharged or predischarged to a predetermined voltage and then stabilized using very low power. The gate functions in evaluation mode when MODE takes a high value, hence triggering the activation of the footer transistor.

DML gates have been found to require minimal energy, with some consuming

0.7 fJ of energy per gate evaluation. This makes them suitable for use in energy harvesting circuits and IoT nodes, where the circuit operates for limited durations due to extremely low power consumption. Dynamic operation allows switching speeds up to 50% higher in DML gates as compared to normal CMOS gates while maintaining decent noise margins [3].

2.6 DML Type A and Type B Circuit Designs: What Differentiates Them?

In a DML-based design, there are two separate circuit designs depending on how the output node is handled in the static phase.

The static phase in type A circuits involves pre-charging the output node with the aid of a PMOS pre-charge transistor, placed at the top of the circuit, which brings the output node to the supply voltage level until the footer transistor turns off. On activation of the evaluate phase, the pre-charge transistor becomes inactive, and the footer transistor brings the pull down network to ground. The logic values decide on whether to hold the output at the high node or bring it to a low node level.

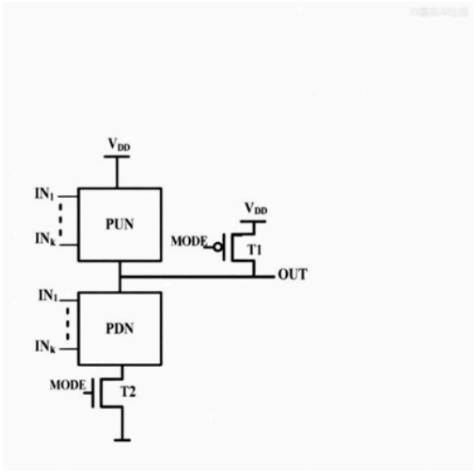

Figure 2.1: DML Footed Design — Type A

During static mode, transistor T1 charges the output node up to V_{DD} whereas T2 stays turned-off. An evaluation event can be set by changing the value of MODE to high, which in turn turns on T2 and lets the pull-down network decide the output.

On the other hand, Type B circuit performs the exact opposite. Instead of charging the output node up in the static phase, Type B pre-discharges the output node towards a low level. Additionally, one more transistor is needed within this circuit design for such behavior to happen. As far as achieving a known state at the output is concerned, pre-discharging also does that for the circuit. The problem that arises here, however, involves more leakage current because of the additional current paths created by the pre-discharge transistor at certain phases of operation. Most importantly, an extra transistor will contribute to the increase of node capacitance, which increases the propagation delay [3].

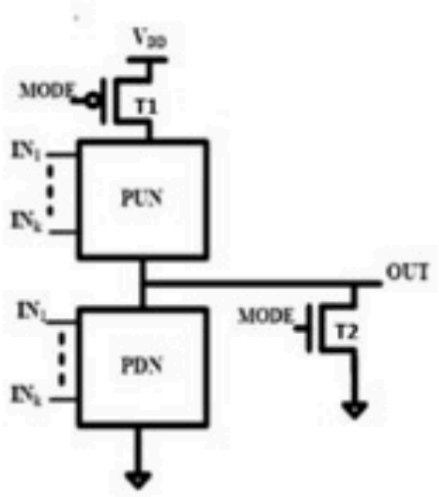

Figure 2.2: DML Footed Design — Type B

Another feature that is found here is the inclusion of an extra NMOS predischarge transistor, unlike Type A. As a result, subthreshold leakage currents and internal capacitance values increase in magnitude, leading to a larger leakage power dissipation and greater propagation delay [3].

As for the significance of such a design difference, it can hardly be overestimated. The results of simulations carried out on chips of 90 nm technology showed that the power consumption in both architectures was almost equal (the discrepancy was less than 1.2%), whereas the propagation delay of Type B was 4 times larger. With the product of the two being the Power-Delay Product, one gets that type B is about 4.4 times worse in this parameter than type A.

2.7 LDML: An Integration of LECTOR and DML

Following the explanation of LECTOR and DML independently, it will be logical to explore whether it is possible to integrate the two techniques to enjoy their respective advantages. This technique is called the LDML method. In this approach, the LECTOR transistors have been incorporated in the footed gate structure of the DML, ensuring that they work in both static and evaluation modes.

During the static phase, the LECTOR transistor behaves in the same way it is expected to, i.e., ensures that at least one transistor is kept close to cutoff during the leakage, thus minimizing the current through the transistor in the precharged mode. On the other hand, during the evaluation phase, the off-path leakage will be controlled by the LECTOR transistors.

Type A LDML and Type B LDML have similarities with DML, where similar architecture exists, too. Type A LDML keeps its LCTs in positions where they play minimal role in increasing capacitance at the internal nodes, but in case of Type B, extra transistors contribute to further loading. The saving on power consumption due to LDML, in comparison with conventional DML, is substantial — about 99% for the process of 90 nm—due to elimination of major part of leakage current in DML only [9].

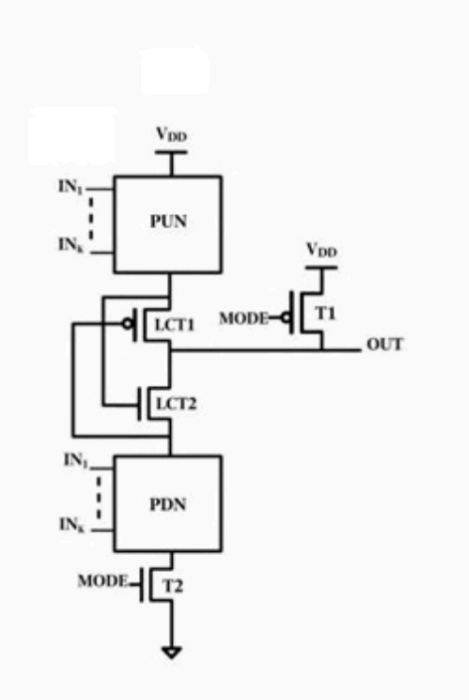

Figure 2.3: LDML Circuit — Type A

LECTOR Leakage Control Transistors (LCT) are incorporated in the pull up and pull down network of the Footed DML Type A logic gate. For any set of input states, at least one LCT will have a voltage close to its cut-off voltage, resulting in higher impedance of the leakage path and lower sub-threshold currents [2, 3].

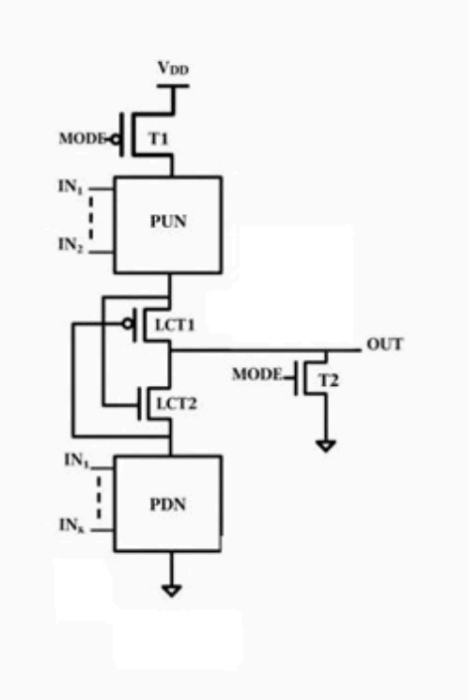

Figure 2.4: LDML Circuit — Type B

The LCTs are included in the DML Type B architecture. The added predischarge transistor carried over from DML Type B, together with the LCTs, leads to increased node capacitance and delay when compared to LDML Type A, leading to poor Power-Delay Product while consuming comparable amounts of power [3, 9].

2.8 Comparison Across Logic Families

Standard CMOS logic can be thought of as the most straightforward and process-friendly technology, being based on NAND and NOT gates that form a multiplexer. No extra control signals are needed and the design is compatible with all kinds of CMOS fabrication processes, although it does not make any attempt to reduce leakage currents past their

minimal value based on transistor sizes. In 90 nm technology, an implementation of a NAND gate consumes about 121 nW of average power, and a full multiplexer made out of such gates consumes about 210 nW of average power at a delay of 2.84 ns (PDP: 21 fJ).

Table 2.1: NOT Gate Results at 90 nm and 45 nm

Technology Node	Delay (s)	Average Power (nW)	PDP (fJ)
90 nm	1.056×10^{-8}	613.86	92.22
45 nm	1.056×10^{-8}	607.22	97.16

Table 2.2: NAND Gate Results at 90 nm and 45 nm

Technology Node	Delay (s)	Average Power (nW)	PDP (fJ)
90 nm	2.694×10^{-10}	121.37	12.14
45 nm	2.041×10^{-10}	102.06	10.21

Table 2.3: MUX (NAND + NOT) Results at 90 nm and 45 nm

Technology Node	Delay (s)	Average Power (nW)	PDP (fJ)
90 nm	2.838×10^{-9}	210.65	21.07
45 nm	2.822×10^{-9}	236.05	23.61

The comparison with literature confirms that the Power Dissipation per Transition (PDP) of LDML Type A, 4.52 fJ, is more than two orders of magnitude less than the lower bound of 1–10 pJ for standard Domino Logic families fabricated on the same technology node [7]. While the 2:1 MUX implemented with MCML provided very fast response—about 20 ps delay—the power consumption was 135.7 μW, almost 550 times greater than the one of LDML Type A [11]. In the case of applications with clock frequencies in the kilohertz to megahertz domain, e.g., IoT sensors, such high performance provides no advantage, whereas such high power makes it impractical.

2.9 A Reference MUX Design Based on NAND and NOT Gates

Within the context of this work, prior to delving into DML and LDML techniques, an example of a basic MUX design was created using the simplest combination possible of gates — NAND gates and NOT gates. For implementing a 2:1 MUX circuit, only three NAND gates and one NOT gate are needed, with the NOT gate providing the complement of the selection signal while each NAND gate processing an individual input signal.

Simulations were performed for the resulting circuit design with both 90 nm and 45 nm technology nodes using the same PTM libraries as other designs. As can be seen from the waveforms, the circuit is indeed working correctly — the output correctly switches depending on the active input signal, and there are no glitches. Thus, results in terms of power consumption and delays obtained in this case provide a clear point of reference.

From the baseline results, it is evident that even though CMOS is operable and straightforward, it does not have any mechanism for limiting leakages. The power increases significantly from 90 nm to 45 nm; hence, it can be seen that without a leakage control method, there is a significant reduction in performance as the technology scales.

2.10 What the Literature Has Overlooked

A review of the existing literature indicates a significant research gap. Even though the LECTOR technique has been used on basic logic gates such as inverters, NAND, and NOR, and even though the DML technique has been studied extensively among other gate circuits, the combined technique known as the LDML has only been tested on NAND and NOR gates before this research was conducted [9]. None of the published studies have performed an implementation of LDML on a 2:1 multiplexer gate circuit or provided Power-Delay Characterization of the technique at 90 nm and 45 nm.

CHAPTER 3
DESIGN METHODOLOGY

3.1 Overview of the Proposed Approach

The general methodology used in this paper is simulation-based bottom-up design flow. This is because the designs do not start with any specification, but rather the circuits were built right at the transistor level. Afterward, the schematic was verified by looking at the waveforms of the output logic gates. Characterization of the power, delays, and Power-Delay Product was done via transient simulation at all the technology nodes.

This design process involves designing the circuit schematic in LTspice $\rightarrow$ assigning appropriate transistor models from the PTM library $\rightarrow$ sizing of the transistors according to specific technology node dimensions $\rightarrow$ applying realistic waveforms as input stimulus $\rightarrow$ transient simulation $\rightarrow$ determination of power consumption, t_{phl}, t_{plh} and PDP $\rightarrow$ comparative analysis among all five versions and two technology nodes.

In total, five circuits were designed and simulated: CMOS MUX 2:1 with NAND gates and NOT gates, DML MUX type A, DML MUX type B, LDML MUX type A, and LDML MUX type B. Each of these circuits represents the same function, i.e., $Y = S \cdot A + \bar{S} \cdot B$ so that no difference can be found between the functions implemented by the considered designs, only the efficiency of their implementation.

The simulation environment used in this paper is the freely available software LTspice, a simulator based on the SPICE tool. Transistor models are taken from the Predictive Technology Model (PTM) library, which offers SPICE compatible libraries of devices fabricated according to the scaled CMOS technology from 180 nm to 16 nm nodes. For this project two technology nodes were selected — 90 nm and 45 nm — to provide information on both the existing technology generation and an aggressively scaled one and to see how different design approaches perform under the growing leakage. The supply voltage for all the circuits was chosen to be equal to 1.2 V.

3.2 Multiplexer Using NAND and NOT Gates

The first circuit that was made represented the basic design of the 2:1 MUX function using standard CMOS technology. This function was implemented through the use of three NAND logic gates and one NOT gate. The output of the NOT gate represents the complement of the select signal S, giving us $\bar{S}$. The first two NAND gates each accept an input signal (A or B) combined with the select signal and its complement, thus computing the terms $S \cdot A$ and $\bar{S} \cdot B$ accordingly. The inputs of the last NAND gate are then the results of the first two NAND gates, producing an output that is computed as $S \cdot A$ NAND $(\bar{S} \cdot B)$. Using De Morgan's law, the result can be expressed as $S \cdot A + \bar{S} \cdot B$.

The following are the dimensions of the transistors for each technology node:

For 90 nm: PMOS (L = 90 nm, W = 1 μm), NMOS (L = 90 nm, W = 0.5 μm)

For 45 nm: PMOS (L = 45 nm, W = 0.5 μm), NMOS (L = 45 nm, W = 0.25 μm)

A capacitor of value 5 fF was connected at the output port to account for the value of the capacitor present at the output of a typical subsequent logic gate. The input stimulus was a combination of three pulse waveforms applied at inputs A, B, and S having time periods of 20 ns, 40

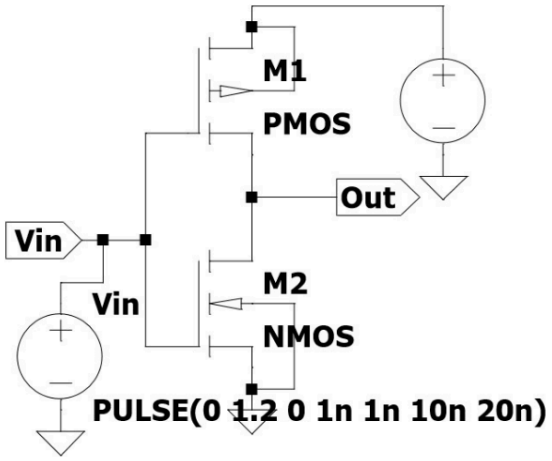

Figure 3.1: NOT Gate Schematic

Single PMOS pull-up and NMOS pull-down implement the inverter function. The output transitions cleanly between logic levels at both 90 nm and 45 nm technology nodes.

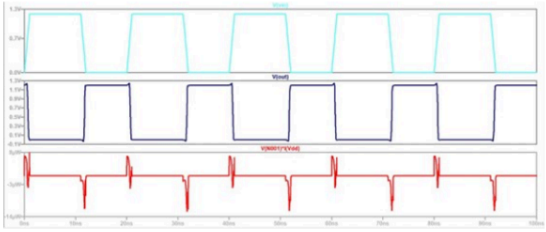

Figure 3.2: NOT Gate Output Waveform

Output transitions cleanly between logic levels with sub-nanosecond edges at both 90 nm and 45 nm. The inverted output confirms correct inverter behavior across all switching cycles.

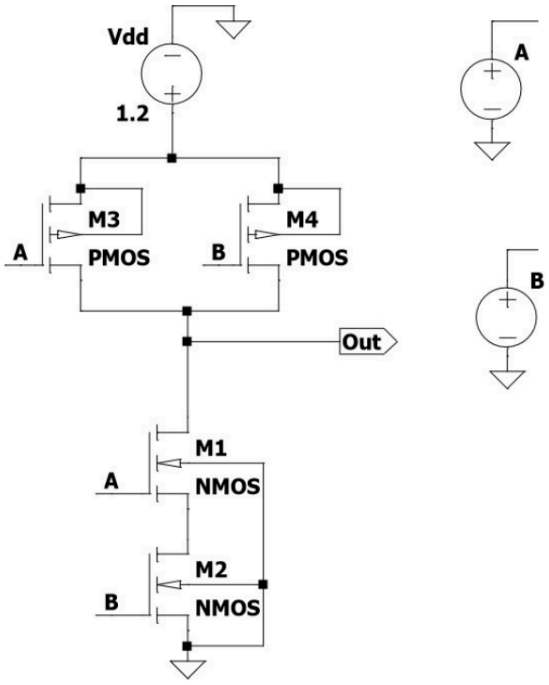

Figure 3.3: NAND Gate Schematic

Two PMOS transistors in parallel form the pull-up network; two NMOS transistors in series form the pull-down network, producing a NAND function. The output is LOW only when both inputs are simultaneously HIGH.

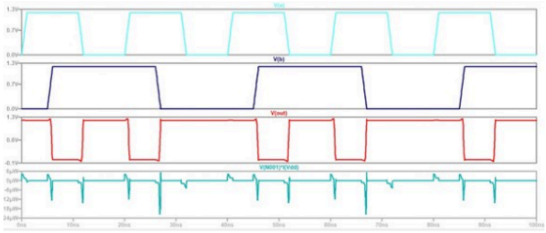

Figure 3.4: NAND Gate Output Waveform

Output is LOW only when both inputs are HIGH; all other input combinations hold the output HIGH. The waveform confirms correct NAND logic behavior across all four input combinations.

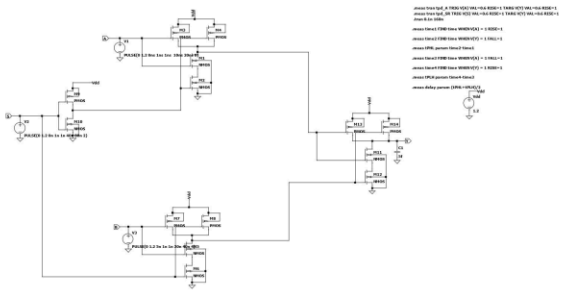

Figure 3.5: MUX Schematic using NAND and NOT Gates

Two NAND gates and one NOT gate implement the 2:1 select function $Y = \bar{S}A + SB$. A third NAND gate combines the two product terms to produce the final multiplexer output.

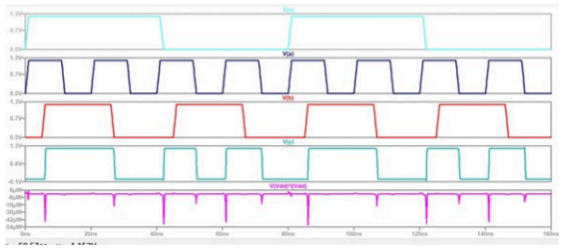

Figure 3.6: MUX Output Waveform

Output correctly tracks input A when $S = 0$ and input B when $S = 1$ across multiple switching cycles. The clean transitions confirm correct 2:1 multiplexer behavior with no glitches.

3.3 Implementation using DML Approach

Here the DML based implementation of 2:1 MUX is constructed using footed dynamic logic, in which the precharging and evaluation stage is triggered by the MODE signal

externally. The pull down circuit is designed in such a way that when there is an input to conduct from the evaluation node to ground if either (S,A) or $(\bar{S},B)$ demands a low level logic output.

The formula for leakage power for both the implementations is given below:

$$P_{leakage} = I_{leakage} \times V_{DD} \tag{3.1}$$

In the above formula $I_{leakage}$ refers to the overall subthreshold current flowing in the off-transistor, while V_{DD} = 1.2 V.

DML Type A – Precharge Circuit: In the MODE = 0 phase (the static phase), the output node is charged to V_{DD} by the precharge transistor, which works with the footer transistor open and the pull-down network disconnected from ground. In the MODE = 1 phase (the evaluation phase), the precharge transistor is turned off, and the footer transistor makes the connection between the pull-down network and ground. At this point, the input bits A, B, and S are responsible for the operation: if a low output is needed according to the present inputs, then the pull-down circuit is enabled and the output discharges; otherwise, the output remains at the precharged value.

DML Type B – Predischarge Circuit: DML Type B adds an extra NMOS transistor that forces a predischarge of the output node for part of the static phase. Consequently, this creates one extra subthreshold leakage current that is not accounted for in the design of Type A, thus increasing the static power dissipation. In addition, since the capacitance of the internal node has increased, more time is required for the evaluation to be completed, thus increasing the delay of propagation.

The measured performance data for both designs of the DML are presented below:

Table 3.1: Power, Delay and PDP for DML Circuits

Node	Circuit	Power (W)	Delay (s)	PDP (J)
90 nm	DML-TA	23.13×10^{-6}	1.06×10^{-8}	2.45×10^{-13}
90 nm	DML-TB	23.42×10^{-6}	4.56×10^{-8}	1.07×10^{-12}
45 nm	DML-TA	40.93×10^{-6}	1.02×10^{-8}	4.19×10^{-13}
45 nm	DML-TB	60.61×10^{-6}	4.54×10^{-8}	2.76×10^{-12}

The results confirm the expected correlation between these two classes of gates. With technology at 90 nm, Type B uses merely 1.2% more power than Type A yet has 331% higher delay, which translates into a PDP value that is 4.4 times worse. Moving from 90 nm to 45 nm, Type A increases its power consumption by 77%, whereas Type B's increase reaches 159%, indicating that Type B is more susceptible to technology scaling on account of greater exposure to leakage.

3.4 LDML Implementation

The LDML gates are built by modifying DML gates with leakage control transistors in the pull-up and pull-down paths. Placement of the LCTs is based on the LECTOR principles, whereby the gate terminals of all LCTs are attached to the internal nodes of the opposing networks. Thus, regardless of the input conditions, at least one of the LCTs would be biased near its cutoff point.

During the static phase of operation, the LCTs behave in LDML just as they do in LECTOR gates by increasing impedance of the leakage path and suppressing sub-threshold leakage currents. During the evaluation phase, the LCTs continue inhibiting leakage current from off-state branches of the pull-down path as the output is determined by the active branch.

LDML Type A: The selection of LCT placement in the Type A configuration is based on ensuring that its additional capacitance contribution to internal nodes is minimized. Hence, its placement in a manner such that the parasitic capacitances added to its output node are minimized allows for minimal increase in the LCT delay overhead. Therefore, there is an overwhelming increase in the leakage reduction but a slight increase in switching time.

LDML Type B: The Type B configuration uses the same extra predischarge transistor found in the DML Type B configuration, along with the addition of LCTs. The combination leads to increased capacitance of internal nodes compared to LDML Type A, hence increased propagation delay.

The measured performance results for both LDML types are presented below:

The most significant outcome of this is the power saving in favor of the LDML Type A when compared to the corresponding DML design. At 90 nm, the power con-

Table 3.2: Power, Delay and PDP for LDML Circuits

Node	Circuit	Power (W)	Delay (s)	PDP (J)
90 nm	LDML-TA	246.10×10^{-9}	1.84×10^{-8}	4.52×10^{-15}
90 nm	LDML-TB	255.39×10^{-9}	5.06×10^{-8}	12.92×10^{-15}
45 nm	LDML-TA	260.29×10^{-9}	2.02×10^{-8}	5.26×10^{-15}
45 nm	LDML-TB	216.46×10^{-9}	5.02×10^{-8}	10.88×10^{-15}

sumption reduces from 23.13 μW for DML-TA to 246.1 nW for LDML-TA, with a power savings of around 99%. Power dissipation per pulse decreases from 245 fJ in DML-TA to 4.52 fJ in LDML-TA, which constitutes a power savings of about 98.2%.

3.5 Simulation Procedure and Metrics Used for Performance Evaluation

To ensure consistency across the five circuits and two different technology nodes, the following method was used: **Supply voltage:** 1.2 V for all circuits and both technology nodes

Input stimulus: Three independent pulses fed to the input terminals A, B, and S:

- A: period 20 ns, rise/fall time 1 ns
- B: period 40 ns, rise/fall time 1 ns
- S: period 80 ns, rise/fall time 1 ns

Power calculation: Average power calculated using the internal power measurement capability in LTspice for the V_{DD} current source throughout the entire simulation time period, taking into account the dynamic power dissipation and the static power dissipation due to leakage current.

Delay Calculation: Two `.meas` statements measured t_{phl} and t_{plh}. The delay is then taken as their mean: delay $= (t_{phl} + t_{plh})/2$.

Power-Delay Product: Calculated as PDP $= P_{avg} \times$ delay. This represents the energy consumed per switching operation. It is the figure of merit that was used for the comparison between the five designs.

CHAPTER 4

FUTURE SCOPES

4.1 Future Research Direction

The findings generated in this study — namely the order of magnitude savings in power attained by LDML Type A compared to traditional DML — lead to a variety of areas for future study. The study conducted in this paper intentionally limited its scope to one type of circuit, two process nodes, and a simulation-based evaluation only. Each of these limitations is a direction in which this project could expand.

The first obvious follow-up direction is the extension of the LDML technique to multi-stage multiplexers. An N:1 multiplexer is just a tree of 2:1 multiplexers; the architecture, therefore, should easily extend to such a case. But the accumulation of the leakage current in such a tree structure, as well as the propagation of the MODE signal through it, creates design issues that were not encountered when designing the simpler 2:1 multiplexers. It would be interesting to quantify whether the 99% power savings advantage of the LDML over the DML persists when extending the circuit size.

In addition to multiplexers, there is no reason why LDML cannot also be used with other types of combinational gates. Adders, comparators, encoders, and similar devices that are common in power-constrained datapath circuitry would provide an excellent benchmark against many of the published low-power adder implementations. In fact, implementing a single LDML full adder or a ripple-carry adder using multiple such adders could offer an interesting comparison against several existing publications on low-power adders.

One potentially fruitful area for future development is extending the LDML concept to sequential circuit design. The problem of designing a sequential circuit that maintains a stable state over many clock cycles poses a unique challenge, since leakage plays an especially important role here due to the requirement for stability. To paraphrase the introductory quote by John Cocke, “every nanosecond of holding a state, leakage current is burning power”. A single-stage LDML flip-flop or master-slave latch utilizing

LECTORs to reduce hold-mode leakage while keeping the same fast setup and clock-to-Q times would make for an interesting project.

This concept of the future architecture consists in connecting several DFF chains one after another, where an XOR comparison function between each stage will check whether the input signal has stabilized, or it is just changing its state. The circuit will sample the input at five equidistant points, compare the first two and the last two of them with one another, and pass through the output only if the means are equal – essentially performing majority voting, but implemented using hardware and consuming LDML power consumption rates.

The protection from electrostatic discharge (ESD) should be considered when implementing such a circuit as well. This problem should be solved by adding special ESD protection devices for each input and output pin of the chip, clamping high voltages and thus protecting gate oxide from destruction. Designing an ESD structure for LCT technology based LDML gates without excessive parasitic capacitance or leakage would be quite a difficult task.

4.2 Comparison: CMOS vs DML vs LDML

The table below consolidates the key performance results from this work and provides a direct comparison between the conventional CMOS MUX, DML Type A, and LDML Type A.

Table 4.1: Comparison of MUX Implementations — CMOS, DML, and LDML

Circuit	Node	Power (W)	Delay (s)	PDP (J)
CMOS MUX (NAND+NOT)	90 nm	210.65×10^{-9}	2.84×10^{-9}	2.11×10^{-17}
CMOS MUX (NAND+NOT)	45 nm	236.05×10^{-9}	2.82×10^{-9}	2.36×10^{-17}
DML Type A	90 nm	23.13×10^{-6}	1.06×10^{-8}	2.45×10^{-13}
DML Type A	45 nm	40.93×10^{-6}	1.02×10^{-8}	4.19×10^{-13}
LDML Type A	90 nm	246.10×10^{-9}	1.84×10^{-8}	4.52×10^{-15}
LDML Type A	45 nm	260.29×10^{-9}	2.02×10^{-8}	5.26×10^{-15}

From this comparison, one can observe that LDML not only outperforms

Table 4.2: Comparison with Prior Published Work

Reference	Circuit	Power	Delay	PDP	Remarks
Yadav et al. [9]	NAND/NOR (LDML)	−58.9% saving	N/R	N/R	No PDP; gates only
Saxena et al. [10]	CMOS gates (LECTOR)	Leakage reduced	Slight increase	N/R	Basic gates; no MUX
Bhattacharyya et al. [11]	2:1 MUX (MCML)	135.7 μW	20.16 ps	2.736 fJ	551× higher power
Alioto & Palumbo [7]	Domino logic	—	—	1–10 pJ floor	LDML 2+ orders better
This Work (LDML-TA)	**2:1 MUX (LDML)**	**246.1 nW**	**18.4 ns**	**4.52 fJ**	**Best PDP; std. CMOS**

DML but actually exists in an entirely different area within the power-performance space. DML was designed to provide flexible performance via mode switching and did an excellent job at that. The price paid by this technique is excessive power consumption amounting to about 100 times more than simple CMOS MUX. The issue of high power consumption is solved by LDML that achieves power on the same level as simple CMOS — about 246 nW at 90 nm — and PDP is 54 times greater than that of DML.

4.3 Proposed Improvements

Although the LDML structure has provided very impressive outcomes in the current work, there still exist ways for improving the circuit in future implementations.

For instance, the use of an adaptive mode control scheme is one way to achieve better performance. The current circuit design features an externally-controlled MODE signal and a fixed mode changeover point between the static and dynamic modes. An improved circuit should detect the activity status of data and automatically enter into dynamic mode only when the switching frequency surpasses a certain threshold and enter into static mode otherwise.

Another possible direction to take when working further with the LDML circuit is the integration of MTCMOS structures and technologies. In particular, assuming that the LCTs can be designed from transistors with a higher threshold voltage than that of the usual transistors, it is possible to obtain a greater leakage reduction effect since high-threshold transistors feature lesser leakage. It should be noted that modern foundries usually support multiple threshold voltages per one technology node.

Another aspect in which freedom of design is achieved through the transistor sizes is the one where the width of the LCT transistors can be decreased. This will lower the amount of capacitance added by these transistors to the internal nodes, although it will also decrease the efficiency of leakage current protection. In addition, a sizing analysis, possibly through automated tools, may be conducted in order to determine an optimum point for a given application.

Finally, employing flip-flop stages which are different from the classic D flip-flop stages employed in this cascading structure — such as pulse triggered and sense amplifier flip-flops — will help decrease the dynamic power consumption of the flip-flop stages during the evaluation phase.

4.4 Possible Applications

LDML-based 2:1 Multiplexer designed here finds suitable applications in various products where size constraints as well as power consumption are critical issues.

Medical wearables: Devices such as heart-rate monitors, watches and fitness bands operate continuously with very little battery power over the course of days or even weeks in monitoring biological signals from sensors. Datapaths used in such devices involve tasks of multiplexing, routing of signals and performing simple mathematical computations — all areas which could benefit from reduced power consumption due to use of LDML technique.

Wireless sensor nodes for IoT applications: Wireless sensors used for monitoring conditions in farms or factories, or even those found in smart city infrastructures, may operate using energy collected from environmental sources such as light, vibrations, or heat, producing power ranging between microwatts and milliwatts. The standby power levels of less than 300 nW achieved by the LDML circuit architecture make it well-suited

for this type of application.

Consumer electronic devices: Televisions remote control units, wireless keyboards, calculators, and game controllers depend on batteries which should last several months. Circuits used to transfer data within these devices could also significantly improve their power efficiency due to reduced leakage enabled by LDML technology.

Industrial control systems: Most control systems that require circuits which are expected to react instantly upon receiving an input signal, yet can spend long intervals not operating, can benefit from LDMLs due to their low power consumption and rapid transition into evaluation mode.

Keypad and interface circuits: In all circuits whose primary input consists of physically pressed buttons or keys, there will be a need for circuits capable of properly decoding button presses and sending signals accordingly. It is particularly important for interface circuits in devices that must respond to button presses regardless of whether or not the rest of the circuitry is asleep.

4.5 Layout and Fabrication Scope

Design in this thesis has taken place only up till the schematic and simulation stages. The next logical step would involve doing the physical layout of the LDML Type A MUX, which will also permit post-layout simulations involving the inclusion of parasitics in the circuit, and will permit checking for compliance of the design rules in accordance with the fabrication process.

The physical layout of the LDML gates will have to be done taking into consideration the placement of the transistors. The leakage-control transistors need to be positioned very close to the corresponding logic transistors because the distance between them should not become too long since this would create parasitics, both in terms of resistance and capacitance.

The appropriate methodology to apply for implementation of the above design would be a standard cell approach, where each gate in the LDML structure would be treated as a standard cell, having certain predefined pin locations, power and ground rails, as well as timing arcs, thus making it easy to place-and-route into a larger circuit design. CAD tools like Cadence Virtuoso or Electric VLSI would be suitable for transistor level

circuit layout during the RD phase, while ensuring Design Rule Check (DRC) and Layout Versus Schematic (LVS) validation of the layout.

After proper physical implementation and validation of the circuit layout, post-layout simulation — which involves re-running the original schematics with parasitic extracted — would give a realistic estimation of the circuit behavior. For fabricating the design, 90 nm or 45 nm bulk CMOS technology at some foundry would be a good choice. Finally, a test chip with all 5 MUX types and power measuring circuits incorporated would serve as a means for experimental validation of the presented simulation results.

CHAPTER 5

CONCLUSIONS

Initially, the question was a very simple one: is there a feasible way to solve the problem of leakage current in a scaled CMOS multiplexer without giving up standard processes which keep chip manufacturing affordable? And it turns out that the answer to this question is affirmative — and the extent of improvements is greater than what I thought it would be initially.

As a baseline for our designs, we chose a 2:1 multiplexer made up of NAND and NOT gates in standard CMOS. Such design operates properly, is simple enough, and offers good performance to start with. However, such approach does not even try to address the issue of leakage, and in simulations at 45 nm process size it consumes more energy compared to the 90 nm design. After that, the implementation of DML, both Type A and Type B, showed one thing predicted by the literature but which is quite eye-catching when you see it in practice: the predischarge transistor in Type B, even if it appears to be a minor architecture change, introduces a delay penalty of over four times relative to Type A with no real power-saving advantage. This proves once again that in digital circuits, little changes may bring big effects.

The greatest discoveries were found in simulations of LDML. By incorporating LECTOR leakage-control transistors within the structure of DML circuits, power consumption was reduced from 23.13 μW for Type A to 246.1 nW for LDML Type A — 99% decrease! In other words, a circuit working in stand-by mode during a single second will consume 23 μJ if designed using DML approach. With LDML power saving circuits the same second of operation in stand-by mode costs only 0.246 μJ, which is almost a hundred times less! It means that with LDML approach the same IoT sensor node powered by a coin cell battery may work for many years as opposed to several weeks with DML approach.

The achievement of a PDP value of 4.52 fJ for LDML Type A at 90 nm technology is important within this perspective. The typical PDP floor of domino logic, which is one of the known high-performance dynamic logic circuits, is stated as being in the

range of 1–10 picojoules at the same process level [7]. LDML Type A performs significantly better, since it lies almost two orders of magnitude below this floor point, indicating that the combined use of static and dynamic modes can create a very distinct operating point in terms of performance and power efficiency.

It can be stated that the similar performance characteristics of the circuits at 45 nm technology level further prove this point. At this technology level, although there is leakage increase due to the smaller process, the power consumption of LDML Type A increases slightly to 260.3 nW. It can be inferred from this result that the proposed technique would be viable at 22 nm technology and below.

Then there is the modularity aspect of this research. One does not have to convert an entire chip to LDML, but only convert selectively some of its gates. A chip designer may choose to convert only the gates that contribute most to leakage power consumption, and retain the remainder as regular CMOS gates. The power benefits can still be achieved in the whole design thanks to this selective conversion capability.

Comparisons to the literature on this class of circuits are also supported by similar findings. While the most relevant work is done by Yadav et al. from the same group, using LDML to design NAND and NOR gates without any reports of PDP or extending the concept to MUX [9], Bhattacharyya et al. have designed a 2:1 MUX, however, using an entirely different class of logic (MCML), which is targeted for gigahertz applications and consumes approximately 551 times more average power compared to the proposed LDML Type A MUX [11]. It highlights the essential difference between the two classes of logic: MCML sacrifices power for maximum speed and thus is intended for use in high-frequency datapath implementations, whereas LDML makes a small sacrifice in terms of delay overhead in exchange for an enormous savings in the leakage current, rendering it a better fit for battery-powered and standby applications where a chip which burns through its power budget in hours is just as good as non-functional.

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ANALYSIS OF LOW-POWER 2:1 MULTIPLEXER USING DML AND LDML TECHNIQUES

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