M.TECH
THESIS

DESIGN OF TERNARY FULL ADDER AND COMPARATOR USING GAA-CNTFET

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JUNE
2026

DESIGN OF TERNARY FULL ADDER AND COMPARATOR USING GAA-CNTFET

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEM

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Certified that Keerti Singh 2K24/VLS/22 has carried out her research work presented in this thesis entitled **"Design of Ternary Full Adder and Comparator using GAA-CNTFET"** for the award of Master of Technology from Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student herself, and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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DECLARATION

I, Keerti Singh, Roll No. 2K24/VLS/22, hereby declare that the work which is being presented in the thesis entitled **"Design of Ternary Full Adder and Comparator using GAA-CNTFET "** in partial fulfilment of the award of degree of Master of Technology which is submitted in the Department of Electronics & Communication Engineering, Delhi Technological University is authentic record of my own work carried out during the period from **January 2026 to May 2026** under supervision of **Dr. Anurag Chauhan**. I have not submitted the matter presented in the thesis for the award of any other degree of this or any other Institute.

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PLAGIARISM VERIFICATION

Title of the Thesis: **Design of Ternary Full Adder and Comparator using GAA-CNTFET**

Total Pages: **51**

Name of the Scholar: **Keerti Singh**

Supervisor name: **Dr. Anurag Chauhan**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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ACKNOWLEDGEMENT

I would like to express my sincere gratitude to **Dr. Anurag Chauhan, Assistant Professor, Department of Electronics and Communication Engineering, Delhi Technological University**, for his valuable guidance, continuous encouragement, and unwavering support throughout the completion of this thesis entitled **"Design of Ternary Full Adder and Comparator using GAA-CNTFET."** His technical expertise, insightful suggestions, and constructive feedback helped me understand the concepts of CNTFET technology and ternary logic systems in greater depth. His constant motivation and supervision played a significant role in the successful completion of this research work. I am also thankful to all the faculty members of the Department of Electronics and Communication Engineering for their guidance, support, and the knowledge they imparted during my postgraduate studies.

I would also like to express my heartfelt gratitude to my parents, family members, friends, and classmates for their continuous encouragement, patience, and moral support throughout my academic journey. Their faith in my abilities motivated me to overcome challenges and complete this work successfully. I am grateful to Delhi Technological University for providing the necessary facilities, resources, and academic environment required for conducting this research. The support and cooperation received from everyone directly or indirectly associated with this work have been invaluable, and I acknowledge their contribution to the successful completion of this thesis.

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
CNTFET	Carbon Nanotube Field Effect Transistor
GAA-CNTFET	Gate-All-Around Carbon Nanotube Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
FinFET	Fin Field Effect Transistor
VLSI	Very Large-Scale Integration
PTL	Pass Transistor Logic
TG	Transmission Gate
GDI	Gate Diffusion Input
STI	Standard Ternary Inverter
NTI	Negative Ternary Inverter
PTI	Positive Ternary Inverter
STAND	Standard Ternary AND Gate
STOR	Standard Ternary OR Gate
STNAND	Standard Ternary NAND Gate
STNOR	Standard Ternary NOR Gate
STXOR	Standard Ternary XOR Gate
TFA	Ternary Full Adder
ALU	Arithmetic Logic Unit
CMOS	Complementary Metal Oxide Semiconductor
VDD	Supply Voltage
Verilog-A	Analog Hardware Description Language
TGDI	Transmission Gate Diffusion Input
EQ	Equality Output
ABIG	A Greater Than B
BBIG	B Greater Than A
CNTFET	Carbon Nanotube Field Effect Transistor
CADENCE	Simulation Program with Integrated Circuit Emphasis

ABSTRACT

Further advancements in semiconductor technology scaling and the increased need for fast and low-power consumption VLSI systems have led many scientists to consider multi-valued logic and nanoelectronics. Several types of multi-valued systems are available, but ternary logic has shown improved efficiency, decreased complexity, and better representation of data than binary logic systems. In this study, ternary comparators and ternary full adders are designed by employing gate-all-around carbon nanotube field-effect transistors (GAA-CNTFETs) at a 10 nm technology node. This study employs PTL logic, unary operators, and ternary standard logic gates to design the proposed circuits.

Owing to its excellent electrostatic characteristics, low leakage currents, enhanced switching, and better carrier transport characteristics, the GAA-CNTFET device structure is highly preferred over the conventional MOSFET and FinFET structures. Ternary standard logic gates, such as STAND, STOR, STNAND, STNOR, and STXOR, and unary operators, such as STI, NTI, and PTI, are implemented to perform arithmetic and comparison operations. The ternary full adder produces effective sum and carry operations through ternary logic values, whereas the ternary comparator performs A>B, A<B, and A=B through CNTFET switching paths. The proposed designs were simulated using the Stanford VS-CNTFET Verilog-A model in the Cadence Virtuoso simulator. The simulation results show that the proposed designs have lower power consumption, less complexity, better switching characteristics, and efficient ternary operations. The results indicate that the proposed GAA-CNTFET ternary system is ideal for low-power nanoelectronics and multivalued VLSI applications.

CHAPTER 1
INTRODUCTION

The carbon nanotube field-effect transistor (CNTFET) is one of the most promising nanodevices that can be used for next-generation VLSI systems because of its superior qualities, such as high carrier mobility, low power requirements, and switching capabilities, in comparison with silicon technology [5]. The technology behind CNTFET devices involves the use of carbon nanotubes that function as semiconductors and act as the conducting channel between the source and drain terminals [10]. Moreover, CNTFET devices demonstrate low leakage current and high integration capabilities, making them suitable for ternary and multivalued logic circuits [16]. This allows for the intensive application of CNTFETs in ternary adders, arithmetic circuits, comparators, and arithmetic logic units [22].

1.1 STRUCTURE OF CNTFET

The basic architecture of a CNTFET includes source, drain, and gate contacts, where a CNT is the conductive channel between the source and drain terminals [27]. In the case of CNTFETs, the gate terminal regulates carrier transport through the carbon nanotube channel by utilizing a dielectric material, like the common architectures of conventional MOSFETs [27].

The threshold voltage in a CNTFET is influenced primarily by the diameter and chirality of the carbon nanotube, which enables engineers to design various logic states effectively in ternary and quaternary systems [5]. Owing to their unique one-dimensional characteristics, carbon nanotubes facilitate ballistic carrier transport, leading to enhanced circuit performance and reduced short-channel effects in nanoelectronics circuits [20].

The electrostatic nature of CNTFET devices is excellent owing to the nanometre-scale dimensions and special electrical properties of carbon nanotubes [7].The special structure and electrical properties of CNTFET technology make it a useful option for creating advanced VLSI systems in nanoelectronics [25].

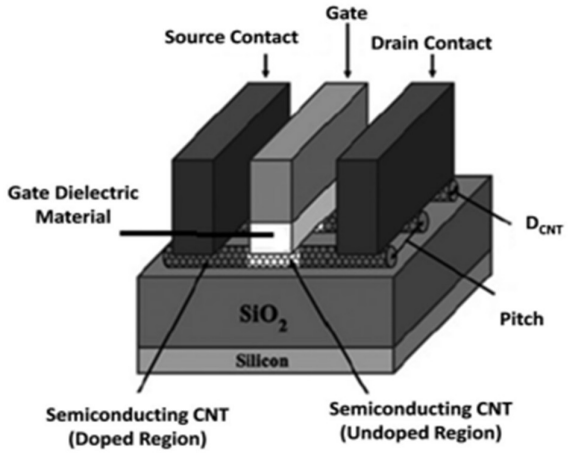

Figure 1.1 CNTFET structure [10]

1.2 GAA-CNTFET

GAAFET refers to a Gate-All-Around Field-Effect Transistor that is considered a recent breakthrough in nanoelectronics, where the gate electrode fully encapsulates the channel in all directions to offer better electrostatic control of the channel in highly scaled semiconductor devices [21]. GAAFET transistors allow the full encapsulation of the gate around the channel structure to ensure minimal impact of short-channel effects and leakage currents in semiconductor electronics [23].Compared to traditional planar transistors, GAAFETs exhibit improved electrical properties, including increased speed, higher current driving capability, and low power consumption in VLSI applications [21]. Owing to their improved electrical performance, GAAFET transistors have emerged as dependable candidates for future nanoelectronics applications, particularly in low power applications [20]. The better gate control of GAAFET devices results in improved stability of the threshold voltage in the device [26]. Moreover, GAAFET devices demonstrate lower power consumption and faster switching time, thus being very advantageous for the design of semiconductor circuits for future use [23]. As can be seen from the benefits, GAAFET transistors are among the most efficient transistor types that can be used in semiconductor circuits [21].

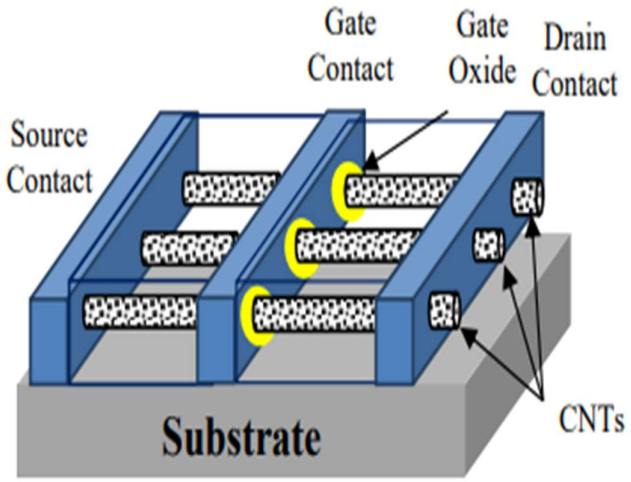

Figure 1.2 Schematic cross-sectional view of a GAACNTFET [6]

1.2.1 CHIRALITY

Chirality is one of the key characteristics of the physical nature of carbon nanotubes (CNTs). This characteristic affects the electrical performance of the carbon nanotube FETs which operate in ternary and multivalued logic gates [2]. Chirality of a carbon nanotube is denoted as (n, m). Values of n and m depend on how carbon atoms are positioned along the carbon nanotube.

They determine the conductive property of the CNT, whether metallic or semiconducting. CNT diameter depends directly on chirality vector (n, m). It is computed by the formula:

$$D_{CNT} = 0.0783\sqrt{n^2 + nm + m^2}$$

Table 1.1 Type of CNT with Chiral Vector (n, m)[3]

No.	Types of CNT	Value of n and m	Properties
1	Armchair	n=m	Metallic
2	Zigzag	m=0	Semiconducting
3	Chiral	n-m≠3*integer	Large band gap
4	Quasi Semiconducting	n-m=3*integer	Small Band gap

Important characteristics of chirality are:

- Indices n and m are referred to as the chirality indices or chiral vector components of carbon nanotubes [3].
- n and m values determine how the graphene sheets are wrapped into CNTs [2]
- Various combinations of n and m give rise to different CNT sizes and conductivity levels [26]

1.2.2 P AND N TYPE GAA-CNTFET

For P-type GAACNTFET, the majority carriers are holes whereas for N-type GAACNTFET, the majority carriers are electrons which can perform complementary function similar like CMOS technology [27]. The gate of both P-type and N-type GAACNTFET is located surrounding the carbon nanotube channel leading to better control over gates and less susceptibility to short-channel effects in transistor operation [26].GAACNTFET of both types is largely used for ternary adder, comparator, arithmetic logic unit, and multi-valued logic due to better electrical properties and nanometre scalability [25]. The complementary operation of the P-type and N-type GAACNTFET increases stability in nanoelectronics circuit architecture by reducing noise [19]. Features of P-type and N-type GAACNTFET are discussed:

- Both devices provide excellent electrostatic control because the gate surrounds the nanotube channel completely [26].
- P-type and N-type structures help achieve complementary switching operation in ternary logic circuits [5].
- These devices exhibit reduced leakage current and lower power dissipation in nanoscale applications [23].
- GAACNTFET structures provide higher switching speed and improved energy efficiency compared to conventional MOS technologies [2].

CHAPTER 2
LITERATURE REVIEW

Semiconductor technology has undergone tremendous evolution from traditional semiconductor devices to sophisticated nanoelectronics architecture designs to meet the need for faster speed and low-power consumption ICs [3]. Traditional semiconductor research was concentrated on MOSFET devices due to their easy manufacturability process and scalability in large-scale integrated circuit systems [1]. The constant reduction in device size has led to undesirable short-channel effects, excessive leakage current, and high-power dissipation in nanometre scale devices [21]. As an alternative to this problem, several modern designs for the next generation of transistors, including FinFET and Gate All Around CNTFET (GAA-CNTFET), have been proposed [23]. GAACNTFET transistors show better gate controllability, lesser leakage current, and greater switching capacity than the traditional planar transistors [26]. GAACNTFET technology is considered a potential technology for the development of future-generation nanoelectronics [23]. Another area of discussion in the existing literature pertains to the significance of the usage of P-type and N-type GAA-CNTFETs for efficient ternary and multivalued logic circuits [27]. Both P-type and N-type CNTFETs have been used for ensuring balanced switching behaviour along with stable operation at the threshold voltage level [20]. Many researchers rely on the principles of Pass Transistor Logic (PTL) and Transmission Gates (TG) because such techniques allow minimizing the number of transistors, lowering power dissipation and increasing speed in nano-devices [21]. The use of PTL and TG based logic circuitries proves useful when designing ternary adders, comparators and other arithmetical circuits utilizing CNTFET transistors [22].

Many papers highlight the importance of applying GDI and Dynamic Logic methods for achieving an optimal value of power delay product and enhancing circuit reliability [14].These techniques help in developing reliable VLSI circuits for future semiconductor technology applications [21]. It is further supported by recent research that the use of ternary logic and unary operators is quite important in simplifying the

complexity of hardware and providing efficient computation in the contemporary VLSI system [16]. In ternary logic systems, three levels of logic rather than the conventional two are used for processing information [20]. Various unary operator and inverter schemes, including Negative Ternary Inverter (NTI), Positive Ternary Inverter (PTI), and Standard Ternary Inverter (STI), are employed widely in building multivalued logic circuits [16]. These ternary logic cells can be exploited for building complex arithmetic circuits, comparators, and logic gates for multi-value logic circuits in nanoelectronics based on CNTFETs [19].

Also, several studies introduce various ternary NAND, NOR XOR, and universal logic gates to enhance the efficiency of operation and energy dissipation in multivalued logic circuitry [20]. Application of CNTFETs to build multi-valued logic circuits offers low leakage current, fast switching speed, and better scalability than in typical CMOS-based electronic systems [22].

Various papers discuss the design and realisation of ternary full adders (TFA) and ternary comparators for efficient arithmetic computations [18]. Compared to binary full adders, the CNTFET based TFAs have the advantages of less power consumption, less transistor usages and power-delay product [22]. Ternary comparators designed with the application of CNTFET technology help perform fast comparisons and efficient computations [19].

The implementation approaches are PTL, TG, GDI, and dynamic logic techniques to improve the overall performance and power saving in ternary arithmetic circuits [18]. The review of literature has indicated that CNTFET-based ternary circuits possess superior electrical properties, near-ballistic transport properties, and higher integration capability in future nanoelectronics applications [20]. This clearly indicates from the review of literature that both CNTFET and GAA-CNTFET technologies are highly influential in the development of the upcoming low power, high speed, and energy efficient VLSI technology.

Traditional MOSFET technology suffered from short-channel effects, leakage current, and increased power dissipation at nanoscale dimensions, which encouraged researchers to explore advanced transistor technologies for improved switching performance and electrostatic control [21].

2.1 COMPARISON AND EVOLUTION

2.1.1 EVOLUTION IN SEMICONDUCTOR

The invention of semiconducting diode and transistors was another revolutionary development in electronics due to their small size and fast functioning [3]. Later, the use of MOSFET technology helped to evolve modern VLSI systems due to their cost-effective fabrication, simple construction, and higher integration ability [1]. With the further decrease of device size based on Moore's law, there were numerous problems associated with the conventional MOSFET technology, such as short-channel effect, leakage current, and high-power dissipation in the case of nanoscale devices [21].To solve these problems, there have been developed new types of devices with three-dimensional fin-shaped channels and improved gate controllability, which are FinFETs [23]. Even though FinFETs had greater performance potential in comparison to other devices, their disadvantages included complex fabrication process and some additional problems in terms of scaling for deep-nanoscale technologies [21]. In contrast, CNTFET devices are known for their greater carrier mobility, near ballistic conduction, reduced short-channel effect, and reduced power dissipation compared with silicon transistor devices [22].

2.1.2 COMPARISON BETWEEN MOSFET, FINFET AND CNTFET

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been widely utilized in traditional VLSI systems due to its easy fabrication technique and compatibility with large-scale integration technology [3]. The FINFET technology is designed to address the weaknesses associated with the MOSFET device using a three-dimensional fin-like channel [21]. On the other hand, CNTFET technology exhibits high carrier mobility, ballistic electron transport, minimal leakage current, and scalability, making it ideal for use in future nanoelectronics systems [20]. One drawback associated with the MOSFET device is that it suffers from excessive leakage current and short-channel effects at nanometric scales [21]. FinFET technology improves gate controllability and reduces leakage current compared to MOSFET structures [23].

- CNTFET technology is ideal for constructing ternary and multivalued logic circuits due to the controllable threshold voltage feature [16].
- Power dissipation of CNTFET circuits and switching speed is much better than silicon-based transistor technologies [22].
- FinFET requires complicated fabrication process in compared with MOSFET, but CNTFET technology is a future prospect in the era of nanoelectronics [21].

2.2 PURPOSE OF WORK

The focus of the present study is on designing high performance nanoelectronics ternary logic circuits using CNTFET technology for energy efficient and low-power applications [20]. The current design methodology also attempts to achieve reduction in hardware complexity and improve the performance of the logic and arithmetic operations with application of latest ternary logic design techniques [22]. Performance benefits of using CNTFETs in terms of providing high packing density and lower power consumption are evident [5]. The present work, therefore, will contribute towards the research on high speed and energy efficient nanoelectronics architectures to meet the demands of future computing applications [20].

The current work also seeks to contribute to the research of designing and implementing highly optimized nanoelectronics architectures that can be utilized for future semiconductor technology and the applications in multivalued logic systems [21]. Fabrication of the work at nano-level using CNTFETs will be very advantageous in providing better electrostatic control and reducing the short channel effects occurring at nano-devices [3]. Its objectives are:

- Design low-power and high-speed ternary logic circuits using CNTFET technology [20]
- To reduce the leakage currents and short channel effects encountered in present CMOS technologies [21].
- For the power-delay performance and energy consumption improvement of arithmetic and logic circuits [10].

- For the ternary adders, comparators, and ALU circuits implementation with transistor reduction [18].
- Combine with chirality-based threshold voltage engineering to design compact [5].

2.3 ADVANTAGES AND DISADVANTAGES OF CNTFET

2.3.1 ADVANTAGES

By the application of CNTFET technology, switching characteristics, electrostatic control, short channel effects can be better optimized in contrast to those of MOSFET technology [21].

On the other hand, the CNTFET with tuneable threshold voltage is well suited for the design of multi-valued logic circuits such as STI, NTI, PTI and ternary full adder circuits [16]. Based on its excellent physical properties, CNTFET and GAACNTFET have been perceived as promising devices for future technology nodes [23]. Its benefits are:

- Better electrostatic control of the device provides improved device performance [26].
- Lower transistor count and simpler hardware increase the computational efficiency of the circuits [18].
- Better power-delay product and energy efficiency are crucial to the continuation of nanoelectronics systems [20].
- The leakage current and short channel effects decrease, making the circuits more reliable [23].

2.3.2 DISADVANTAGES

However, the CNTFET and the GAA-CNTFET face some challenges although there are many advantages associated with them due to the fabrication complexities, process variability and constraints of large scale manufacturing [23].It is very difficult to control the chiral structure and the diameter of the carbon nanotubes during fabrication of nanotubes [27].Stability of the threshold voltage and device reliability is degraded due to process variability [20].

- Large-scale integration and mass production are difficult [23].
- Fabrication difficulty is increased due to nanotubes placement and alignment issues [7].
- Contact resistance can lower the performance in nanoelectronics circuits [27].
- Limited compatibility with existing CMOS fabrication infrastructure [20].
- Lack of matured industrial fabrication and design infrastructure for CNTFET technology limits its large-scale commercialization [21].

2.4 SUMMARY OF LITERATURE REVIEW

Most parts of the review deals with development of electronics at semiconductor technology and particularly the enhancement of semiconductor technology from MOSFET to CNTFET and GAA-CNTFET nanoelectronics. In this review, it has been stated that short channel effects, power dissipation, and some of the above aspects like leakage current are increasing in scaled MOSFET technology which motivated the researcher to focus on FinFET and CNTFET for better electrostatics and switching behaviour.

Other than this the performance benefits from using CNTFET and GAA-CNTFET structures and trivalued logic were highlighted. The review also emphasizes the utilization of ternary logic, unary operators, and CNTFET based circuit for increasing the performance, reducing the hardware complexity. The various design techniques used here are Pass Transistor Logic (PTL), Transmission Gates (TG), GDI and some dynamic logic implementation. Unary operators like STI, NTI, PTI are also used by many researchers to design efficient multivalued logic. Again, from the comparative analysis of MOSFET, FinFET and CNTFET technologies, authors have stated that CNTFET and GAA-CNTFET are better in switching speed, power consumption, power delay product and for high density integration in future nanoelectronics devices. So, the usage of CNTFET based ternary logic circuits shows great possibility for designing new fast energy efficient semiconductor devices.

CHAPTER 3

SETUP AND SIMULATION

The proposed ternary circuit design is implemented using the CNTFET design scheme and Pass Transistor Logic (PTL) and Transmission Gates (TG). The purpose of using PTL in the design is because PTL has low transistor count and it has incredibly good switching characteristics for ternary circuits [20]. The main reason for implementing the TG scheme is the efficient and dependable signal transfer in ternary logic circuits [21]. The main goal of the design is to design ternary full adder circuits (TFA) and comparators. TFA and comparators are significant for modern day multi-valued logic systems [19].

3.1 PASS TRANSISTOR LOGIC

In the PTL method, the transistor devices are primarily used as switches. The switch either allows the logic level of a signal at one node to pass to the next node or blocks the signal without combining the transistor into the common pull-up and pull-down arrangement. This structure reduces significant power consumption, increases switching speed and reduces silicon area for advanced VLSI circuits [21]. Due to nearly ballistic transport properties and high carrier mobility, PTL based CNTFETs are extensively utilized in designs such as ternary full adders, arithmetic logic unit, comparators and multi-valued logic gates [20].

- PTL uses transistors as switches for direct logic signal transmission [1].
- PTL based CNTFET circuits provide lower power dissipation and improved switching speed [21].
- PTL is widely used in ternary full adders, comparators, and arithmetic logic units [10].

3.2 TRANSMISSION GATE

By applying TG to CNTFET technology, power-delay product is optimized, and power consumption is reduced along with increasing mobility and decreasing leakage current. This is due to the quasi-ballistic nature of transportation along the carbon nanotube [20].

Thus TG-based ternary circuits using CNTFET may be a possible efficient approach to implement low power high speed and small size devices of nanoelectronics systems of the future [21]. For logic design, logic circuitry complexity is reduced, and propagation delay decreases and logic stability increases when designing with TG based ternary logic.

Logic design using the TG method is well suited for application to ternary logic design [1].TG is applicable in many ternary circuits which includes adder, multiplier, comparator, and ALU circuit [18]. TG uses parallel N type and P type devices.

- TG allows strong transmission of both logic high and logic low signals without major voltage loss [1].
- TG reduces propagation delay and improves switching performance in ternary circuits [20].
- TG methodology minimises hardware complexity and transistor count in nanoelectronics systems [18].

3.3 UNARY GATES

Unary gates can be regard as basic building block of ternary logic that pass some logic operations with one input and generates modified ternary output value [5]. Unary gates are used in various CNTFETs based nano-circuits as the CNTFET has good controlling threshold voltage, low leakage and switching speed [20].

They have also used in ternary full adder, comparators, Arithmetic Logic Units (ALUs), multiplexers, and Universal logic gates design as it gives much greater logic flexibility and computation in multi-level system [22].

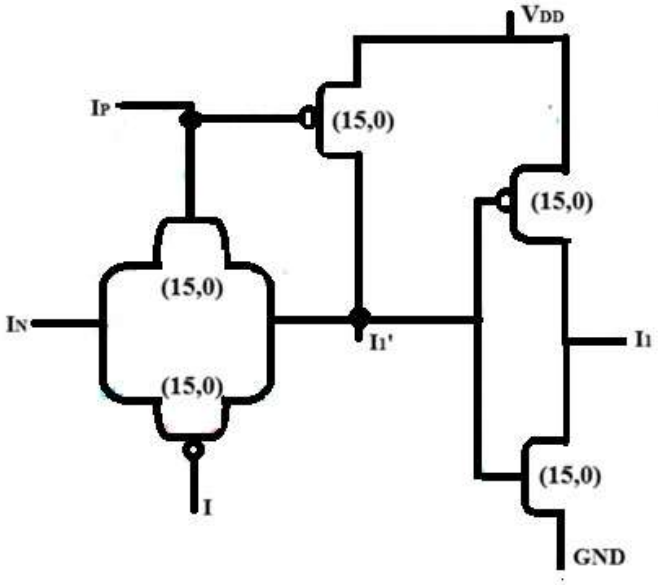

Figure 3.1 CNTFET-based design of unary operators I and I'

Another important unary function is decisive literal that produces "2" only if the input is identical to logic "1"; otherwise, it produces logic "0." This function can be described mathematically by equation, where *I* is a ternary input.

$$C_1 = \begin{cases} 2, & if\ I = 1 \\ 0, & if\ I \neq 1 \end{cases}$$

The unary operators are significant component of a ternary full adder, comparator, multiplexer, ALUs, and many multi-valued logic circuits for generating necessary control signals to make selection of a branch and for routing the signal [16].

Within the framework of GAA-CNTFET based implementation of a unary operator not only enhances the flexibility of the circuit but also supports implementation of a smaller design due to the use of PTL and TG approach [23].

Table 3.1 Truth table of Unary Operator

INPUT	NTI	PTI	C'	C_1
0	2	2	2	0
1	0	2	0	2
2	0	0	2	0

The unary output produced by the STI, PTI and NTI is used to turn on or off selected conducting paths and to realize proper ternary logic operation with smaller number of transistors. In that regard the unary operators are the basic component in the realization of low power and compact ternary nanoelectronics VLSI system [5] .

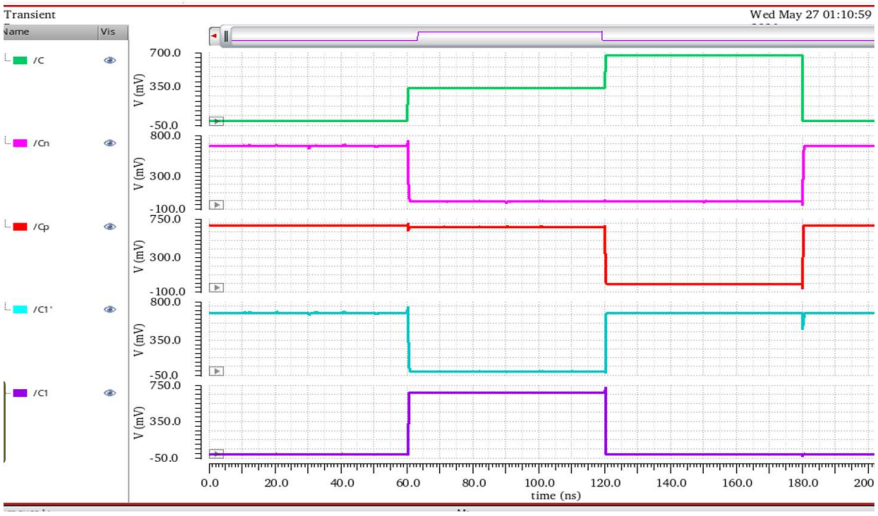

Figure 3.2 Input and Output waveforms of the Unary logic operator

3.4 TERNARY GATE

Ternary logic refers to multi-valued logics that employ three logic levels, commonly denoted as 0, 1, and 2, as opposed to the two logic levels that are typically employed in binary logic systems [10]. The use of ternary logic in circuits results in reduced interconnects, fewer transistors, and increased computational efficiency in VLSI designs [5]. Ternary logic also enhances energy efficiency and switching speeds in future nanoelectronics devices [22]. Unary operators in ternary logic refer to logic functions that operate on a single input signal variable and produce a modified ternary output based on specific logic rules [16]. Commonly implemented univariate operators in ternary logics include negative ternary inverters, positive ternary inverters and standard ternary inverters, which are basic components of ternary logic circuits [16]. Negative Ternary Inverter (NTI) partially inverts ternary logic states toward lower output levels [16]. Positive Ternary Inverter (PTI) partially inverts ternary logic states toward higher output levels [16]. Standard ternary inverter performs complete inversion of ternary input states [20].

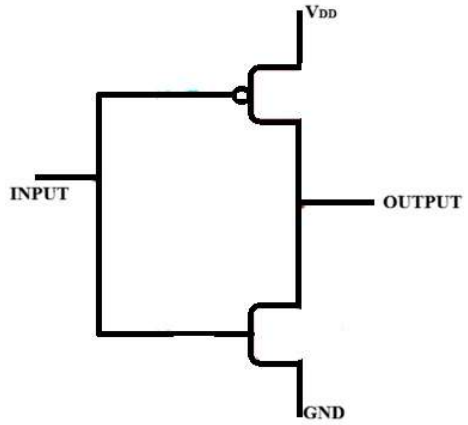

Figure 3.3 Schematic diagram for NTI and PTI

Table 3.2 Truth table for NTI, PTI and STI

INPUTS	NTI	PTI	STI
0	2	2	2
1	0	2	1
2	0	0	0

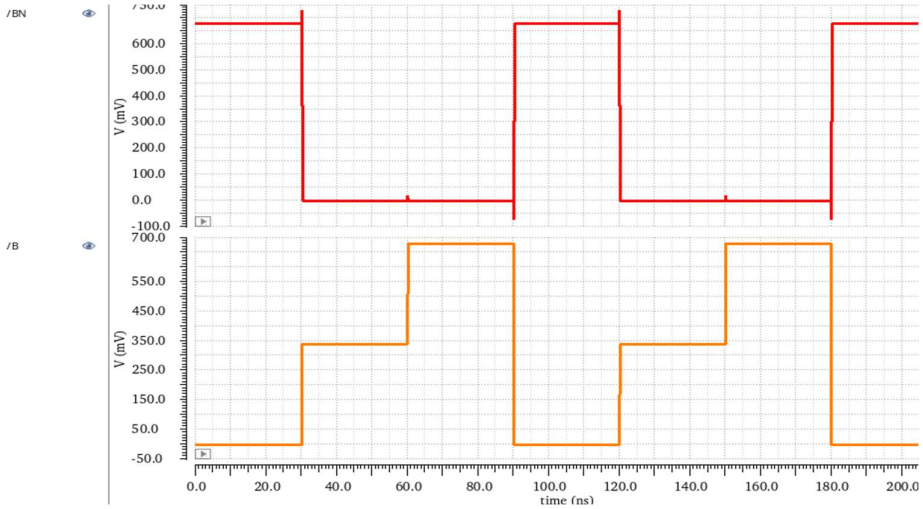

Figure 3.4 Input and Output waveforms of the circuits NTI

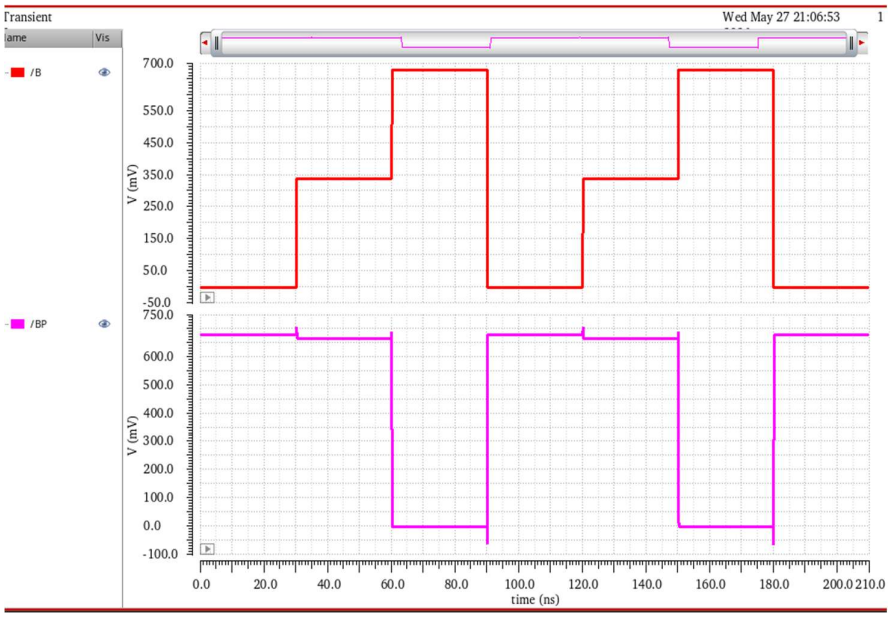

Figure 3.5 Input and Output waveforms of the circuit PTI

3.5 STANDARD TERNARY INVERTER

The Standard ternary inverter is usually more favoured than both the NTI and PTI due to the former's capability to provide full ternary inversion in all the three logic states, which enhances its logical behaviour and increases circuit flexibility [13]. Different from NTI and PTI that negatively cancel logic levels in certain aspects, STI can achieve a full inversion of logic and make multivalued logic systems simpler [5]. The advantage of using STI is to achieve high anti-noise ability and high signal stability for the system [13].

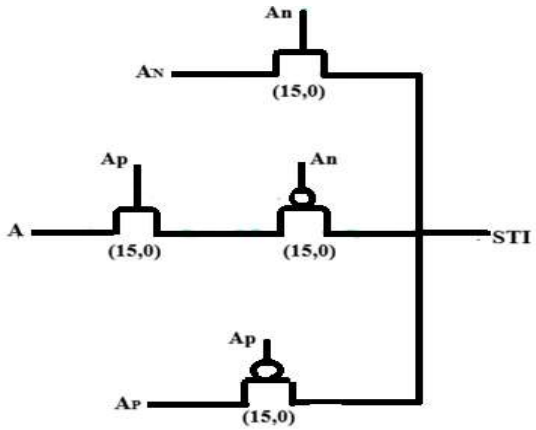

Figure 3.6 Schematic diagram of standard ternary inverter (STI)

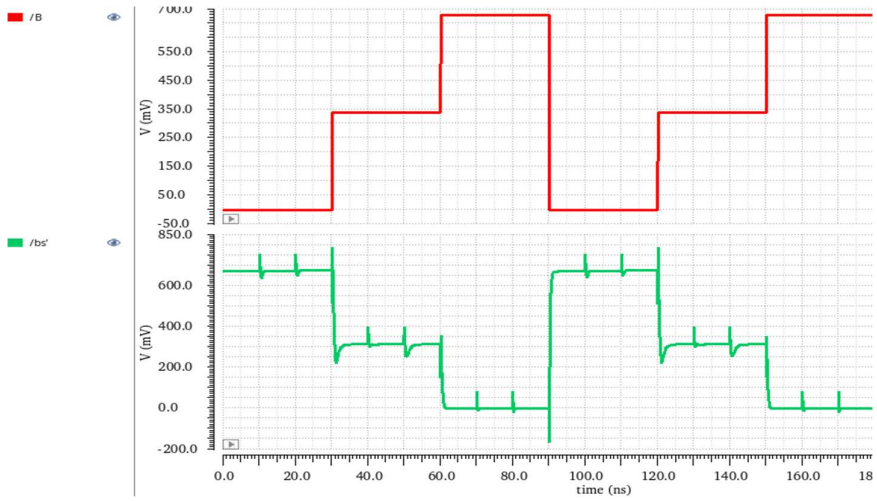

Figure 3.7 Input and Output waveforms of STI

As the STI circuit assigns the complementary state of the input state to the output state and so it is very suitable to build complex ternary arithmetic circuits, logic gates, comparators, Ternary Full Adders etc. [22] STI circuit has very important value to implement in future semiconductor technology and ternary computing technology in the CNTFET form [16].

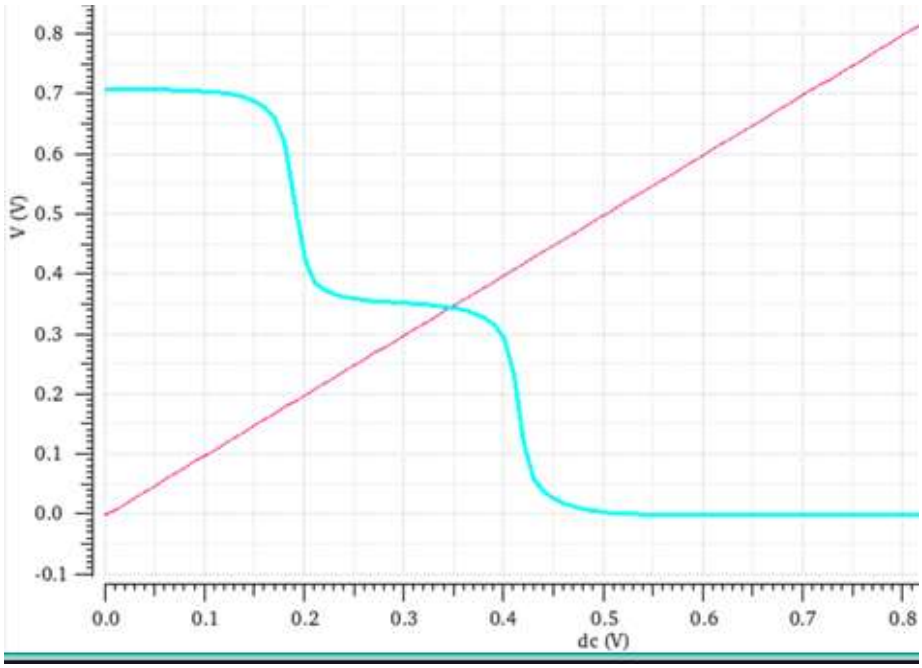

Figure 3.8 Voltage transfer characteristic curve of STI

3.5.1 STANDARD TERNARY AND GATE

Standard Ternary AND Gate is one of the significant multivalued logic gates for ternary logic that performs a logical AND operation on three logic states 0, 1 and 2 [5]. For this computation, minimum value rule has been adopted, and the minimum among the input logic states is taken as the output for the operation [5]. Likewise, CNTFET-based Standard Ternary AND Gates exhibit faster computation with a better power delay product and lower propagation delay compared with their CMOS-based logic gate circuits [23].

If A and B are two literals in ternary logic, which means.

A, B ϵ {0, 1, 2} then

AND/MIN {A, B} = A ● B = A, if **A ≤ B = B** otherwise.

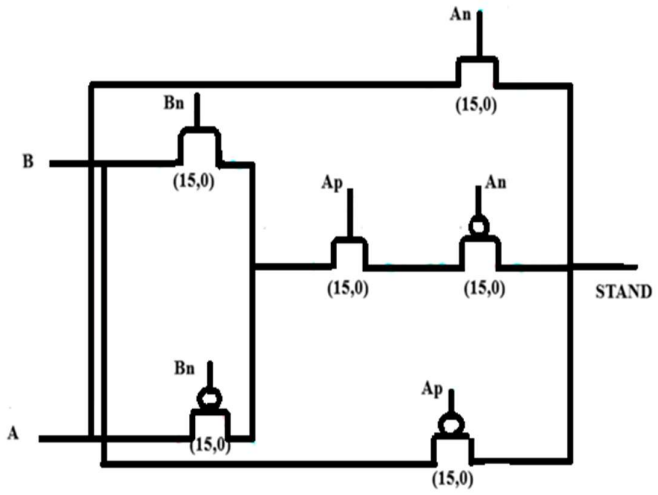

Figure 3.9 Schematic diagram of STAND Gate

Table 3.3 Truth table for STAND

INPUT A	INPUT B	AND
0	0	0
1	0	0
2	0	0
0	1	0
1	1	1
2	1	1
0	2	0
1	2	1
2	2	2

3.5.2 STANDARD TERNARY OR GATE

The output of a standard ternary OR gate usually follows the maximum value rule, according to which the output value is taken as that of the maximum-valued input for ternary operations [5]. It is frequently that STOR gates have been used in ternary full adders, ternary comparators, ternary ALU, ternary multiplexers, and other ternary arithmetic circuits to improve calculation performance and to simplify circuit composition [22].

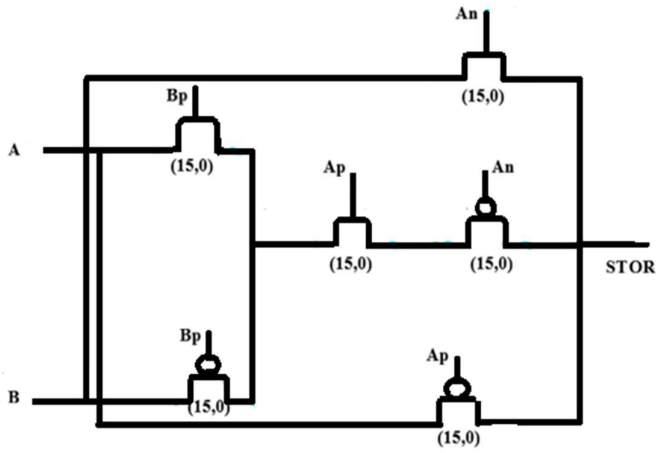

Figure 3.10 Schematic diagram of STOR gate

If A and B are two literals in ternary logic, which means,

A, B ϵ {0, 1, 2} then

MAX/OR {A, B} = A + B =A if **A ≥ B =B** Otherwise.

Table 3.4 Truth table for STOR

INPUT A	INPUT B	OR
0	0	0
1	0	1
2	0	2
0	1	1
1	1	1
2	1	2
0	2	2
1	2	2
2	2	2

3.5.3 STANDARD TERNARY NAND GATE

Standard ternary NAND Gate is one versatile multi-valued logic gate used in ternary logic systems to conduct ternary logic NAND operations using three logic states represented by 0, 1 and 2 [5].

If A and B are two literals in ternary logic, which means,

A, B ϵ {0, 1, 2} then

STNAND (A, B) = 2 – AND (A, B)

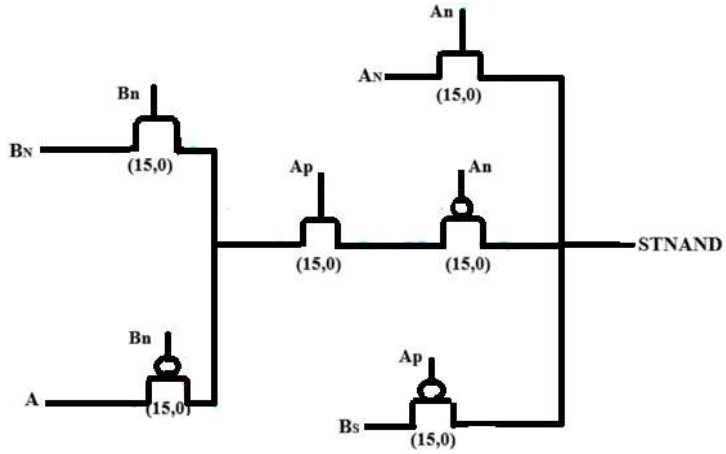

Figure 3.11 Schematic diagram of the proposed STNAND

Table 3.5 Truth table for STNAND

INPUT A	INPUT B	STNAND
0	0	2
1	0	2
2	0	2
0	1	2
1	1	1
2	1	1
0	2	2
1	2	1
2	2	0

The STNAND operation is based on using unary-derived inputs such as ***AP, AN, BP, BN, As and Bs*** generated by PTI, NTI and STI unary operations [16]. They enable certain PTL and TG conduction paths for corresponding applied input values, and thus

they achieve ternary logic level to the output node [16]. TG's ensure signals can travel across with full swing ternary logic levels and the GAA-CNTFET technology ensures good gate controllability and better switching characteristics [23].

3.5.4 STANDARD TERNARY NOR GATE

Standard Ternary NOR Gate is one of the ternary universal logic gates that can perform a NOR operation using three values [0, 1, 2] in ternary logic systems [5]. Output produced by Standard Ternary NOR Gate results in ternary OR followed by ternary complement [5].

If A and B are two literals in ternary logic, which means,

A, B ϵ {0, 1, 2} then

STNOR (A, B) = 2 – OR (A, B)

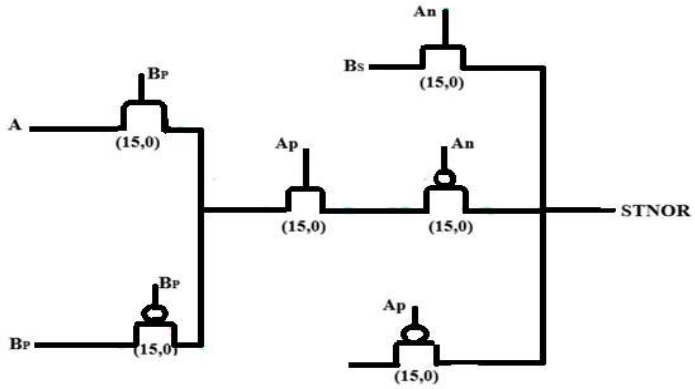

Figure 3.12 Schematic diagram of the proposed STNOR

Table 3.6 Truth table for STNOR

INPUT A	INPUT B	STNOR
0	0	2
1	0	1
2	0	0
0	1	1
1	1	1
2	1	0
0	2	0
1	2	0
2	2	0

3.5.5 STANDARD TERNARY XOR GATE

The presented STXOR is a ternary logic gate which is implemented using GAA-CNTFET and PTL and TG circuits to implement the ternary exclusive-OR operation [16]. The gate is built using multiple-threshold CNTFETs achieved through chirality engineering, to distinguish properly three ternary logic levels and produce the desired XOR output [5].

If A and B are two literals in ternary logic, which means,

A, B ϵ {0, 1, 2} then

STXOR (A, B) = AB' +A'B

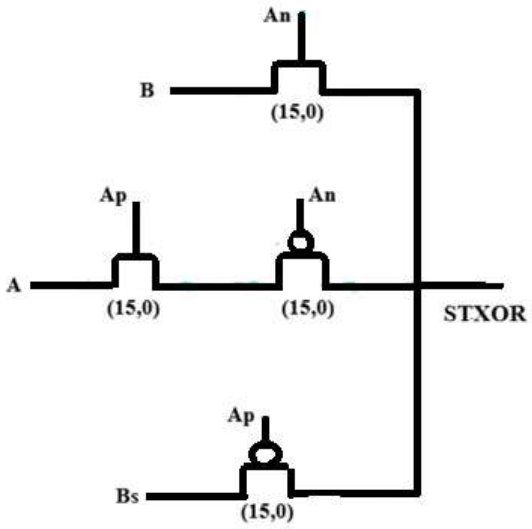

Figure 3.13 Schematic diagram of the proposed STXOR

Table 3.7 Truth table for STXOR

INPUT A	INPUT B	STXOR
0	0	0
1	0	1
2	0	2
0	1	1
1	1	1
2	1	1
0	2	2
1	2	1
2	2	0

Both PTL and TG circuitries make the ternary signals easy to propagate while keeping compact layout. [20]. The TG structures contribute dependable full-swing ternary signal propagation and the GAA-CNTFET structure provides enhanced switching performance and control over electrostatics [23]. As a result, the designed STXOR gate is a practical implementation of ternary XOR function in arithmetic and logic applications [20]

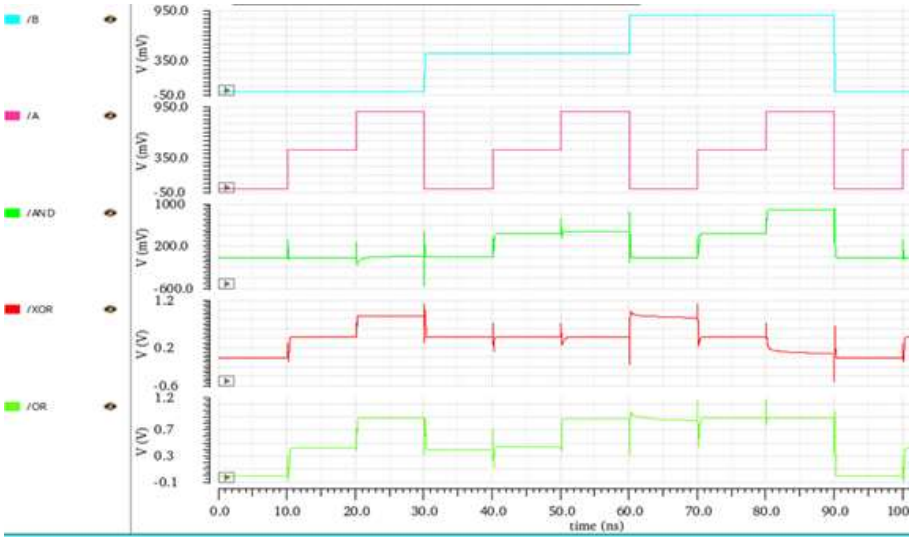

Figure 3.14 Input and Output waveforms of STAND, STOR, STXOR

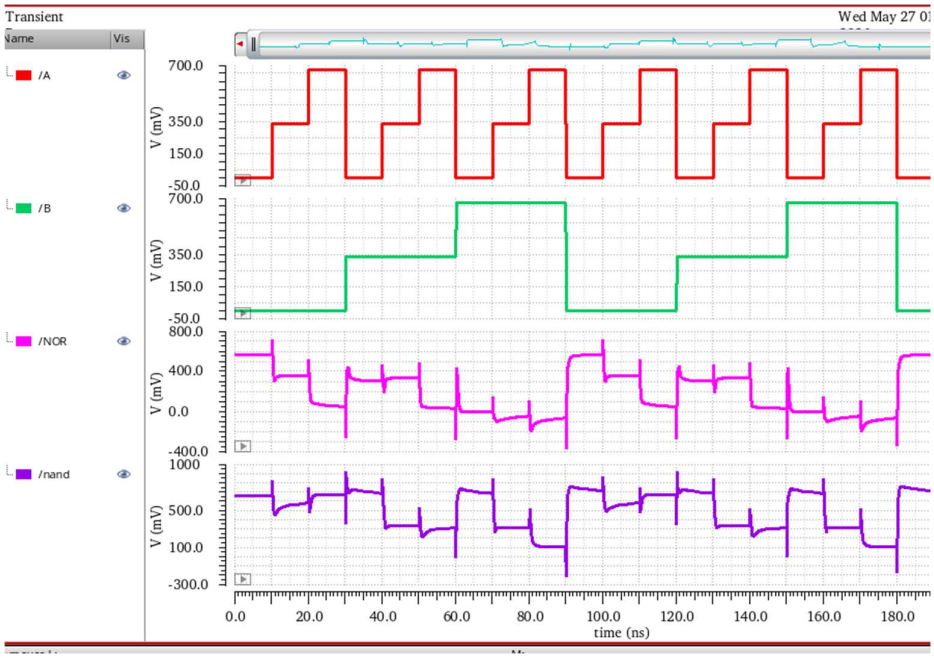

Figure 3.15 Input and Output waveforms of STNAND AND STNOR

CHAPTER 4

CIRCUIT AND RESULT

Improved electrostatic behaviour, lower leakage current and switching characteristics are displayed by GAA-CNTFET compared to that of MOSFET and Top-Gate CNTFET structures [23]. In the proposed ternary circuit structure PTL approach has been implemented because it provides a reduction of transistors count and minimal hardware resources and it improves power delay of the ternary circuit [17]. Furthermore, TG approach has been implemented to effectively transmit the ternary logic signals with low propagation delay [14]. TFA has been implemented because arithmetic ternary circuit has fewer die areas, interconnections and power consumptions than binary circuits [5].The unary operator gates used in the design include Standard Ternary Inverter (STI), Negative Ternary Inverter (NTI) and Positive Ternary Inverter (PTI) because it produce the ternary logic levels to help to effectively perform the operations of Multi-Valued Logic (MVL) signals [17].The ternary standard logic gates integrated with the design include ternary AND, OR, NAND, NOR and XOR gates [5]. Ternary comparator has also been used in the design by combining PTL and TG techniques to reduce the power consumption with higher comparison speed [19].

4.1 PARAMETER

GAA-CNTFET structure is superior in the aspects of electrostatic control, leakage current and switch ability to MOSFET and Top-Gate CNTFET technologies [23]. In this work PTL has been chosen due to its reduced transistor count, minimized complexity and optimized power-delay product for ternary systems [17]. Transmission Gate (TG) is implemented for proper transmission of ternary logic levels with reduced propagation delay [14]. The Proposed Ternary Full Adder (TFA) has been

implemented due to the effective features of ternary arithmetic circuits namely less area and reduced inter-connectivity and lower power dissipation [5].

Table 4.1 10 nm VS-CNTFET Characteristics and Parameters

PARAMETERS	DESCRIPTION	VALUES
L_{ch}	Physical channel length	10 nm
FET-type	P-type and N-type	1: N-type -1: P-type
L_{geff}	The mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering	10 nm
L_{ext}	Length of source/drain extension region outside the intrinsic channel.	3nm
K_{gate}	The dielectric constant of high-k top gate dielectric material HfO2 (planer gate)	23
E_{fsd}	Source/drain Fermi level parameter.	0.258 eV
T_{ox}	The thickness of high-k top gate dielectric material HfO2 (planer gate	3 nm
V_{DD}	Supply voltage	0.68V
Tube	The number of carbon nanotubes (CNTs) in the channel region of the CNTFET	1 to 3
Chirality	The chirality values of the CNTs used in the proposed designs	(9,0) (15,0) (19,0)
CADENCE	Tool used	

The model discussed above has chirality dependent CNT diameter determination, threshold voltage tuneable and quantum capacitance effect, which are the most important aspects for designing multi-valued logic circuits. Lg, tox, d, kox and type (1 for N-type, -1 for P-type) are the parameters which describe the device for simulation. Standard ternary inverter(STI), negative ternary inverter(NTI) and positive ternary inverter (PTI) are some of the unary gates that are utilized here to produce the ternary logic states [17].Ternary AND, OR, NAND, NOR and XOR are some of the standard ternary gates that are used with unary gates for logical and arithmetic operations [5].

To design ternary comparator with high speed, low power and less hardware requirement PTL and TG methods are used in [19].

4.2 CIRCUIT

4.2.1 PROPOSED TERNARY FULL ADDER

A Ternary Full Adder is a combinatorial logic circuit which implements addition of three ternary number bits. It takes three ternary inputs namely A, B and Cin, and outputs two ternary numbers namely Sum and Carry.

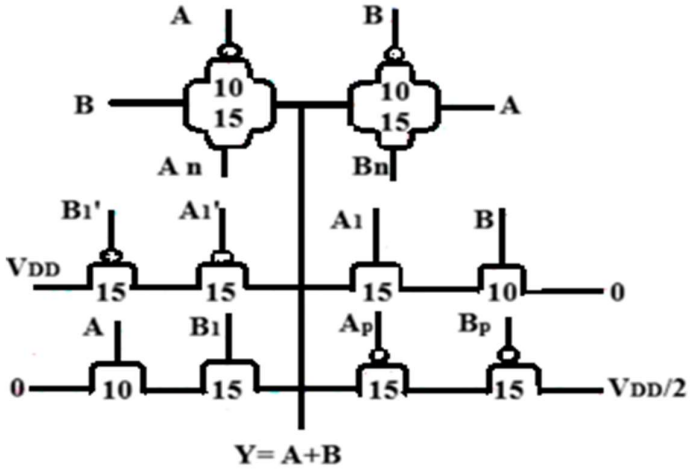

Figure 4.1 Schematic diagram of the Y=A+B logic

Table 4.2 Truth table for Y logic

INPUT A	INPUT B	Y
0	0	0
1	0	1
2	0	2
0	1	1
1	1	2
2	1	0
0	2	2
1	2	0
2	2	1

The Y logic (Y = A+B) is then implemented to make the generation of the SUM and CARRY output easier in the ternary full adder. First input values A and B are taken together to produce Y and then Y and Cin is taken as input to the SUM and CARRY circuit. Thus complexity of the circuit, number of transistors and power dissipation can be minimized to increase the speed and efficiency of the ternary full adder.

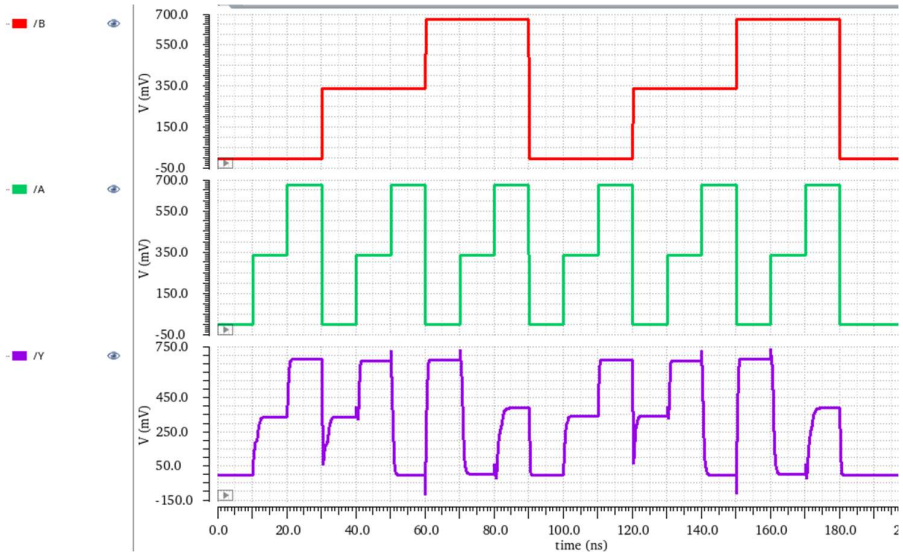

Figure 4.2 Input and Output waveforms of the Y=A+B logic

Here, the Sum generation circuit has been designed using CNTFET-based PTL and TG techniques to generate ternary Sum output. The PTL directly propagates 0, VDD/2 and VDD resulting in lesser transistors, and TG enhances signal transferring and output driving.

In the upper section of the circuit, the TG controlled by C and C_N get active when C=0 to directly send the signal Y to the sum node. Likewise, when $Y = 0$, the alternate PTL path controlled by $Y$and Y_N transfers the carry signal C toward the output node. The transistor located close to the Y1 signal is used as the control transistor to facilitate charge/discharge path when in the intermediate state of ternary operations.

Thus, depending on the waveform transitions, the activated CNTFET switching network either transfers $0, V_{DD}/2$, or $V_{DD}$to the Sum node to produce the required ternary sum output.

- When Y=0, the PTL line under control of Y and YN transfers C to Sum.

- When C=0, the TG line under control of C and C_N transfers Y towards output node.
- Transistor connected with Y_1 transfers into charging lines when the logic value 1.

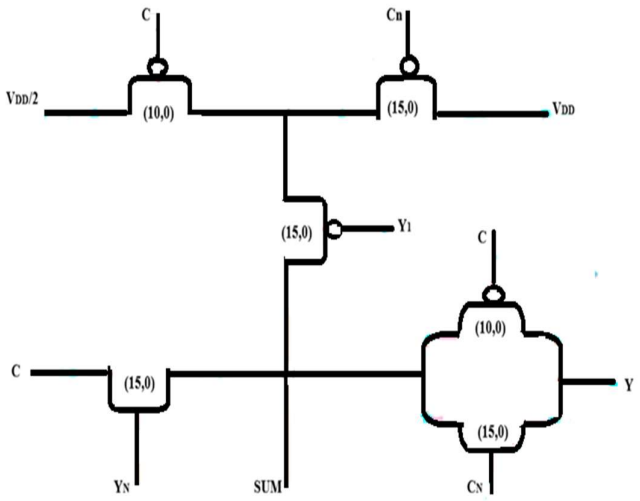

Figure 4.3 Schematic diagram of the SUM logic

Table 4.3 Truth table for Sum and Carry

A	B	Y	C = 0		C = 1		C = 2	
			Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	1	0	2	0
0	1	1	1	0	2	0	0	1
0	2	2	2	0	0	1	1	1
1	0	1	1	0	2	0	0	1
1	1	2	2	0	0	1	1	1
1	2	0	0	1	1	1	2	1
2	0	2	2	0	0	1	1	1
2	1	0	0	1	1	1	2	1
2	2	1	1	1	2	1	0	2

The carry generation circuit uses the intermediate signal Y and the input carry *C* to produce the carry output for ternary addition. The three control signals *Cn, Yn, and Y* determine which conductive branch will be enabled. The active branch would send

VDD, VDD/2 or 0 V to the carry node and therefore produce the desired ternary carry value.

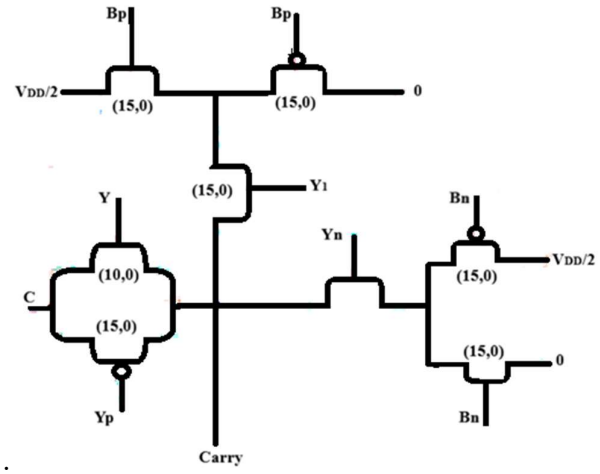

Figure 4.4 Schematic diagram of the CARRY logic

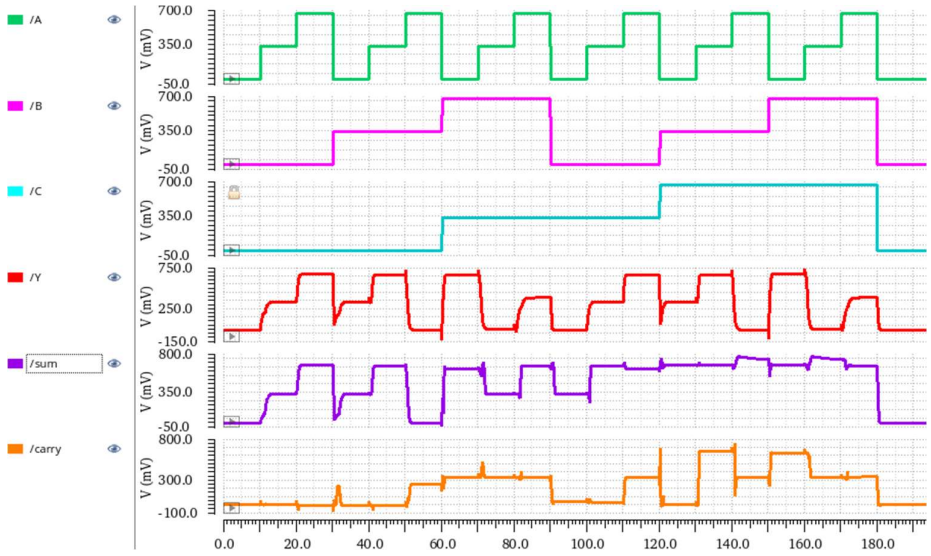

Figure 4.5 Input and Output waveforms of CARRY and SUM

4.2.2 COMPARATOR

In this circuit, there are different CNTFETs to provide the pull up to logic '0', logic '1' and logic '2' corresponding to the input. The above CNTFET near the signal mainly serves the purpose of pulling up to logic '2' (V_{DD}). It turns ON as the appropriate ternary state is applied and thereby pulls up the output towards VDD to get ternary logic '2'.

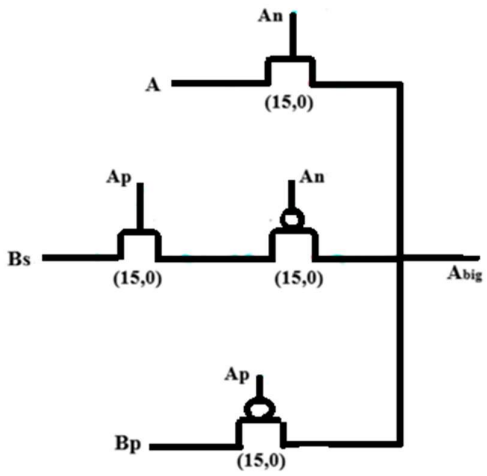

Figure 4.6 Schematic diagram of the A_{big}

Table 4.4 Truth table for A_{big}

INPUT A	INPUT B	A_{big}
0	0	0
1	0	2
2	0	2
0	1	0
1	1	0
2	1	2
0	2	0
1	2	0
2	2	0

The “1” middle logic level ($V_{DD}/2$) is generated by the central CNTFET network near the signal op. So, in this condition pull-up transistor is conducting and this intermediate voltage is given to the output node which will finally result in Ternary logic 1. Finally, the bottom CNTFET near signal up is acting as pull-down network for the logic 0. The CNTFET switching paths are driven appropriately to get the comparator output B_{BIG}. The upper CNTFET used near the signal bn V_{DD} ternary logic "2" if compare condition matches is to generate the pull-up path which charges up the output node. The centre

path of the CNTFETs near the signals *bp and bn* carries the intermediate voltage value $V_{DD}/2$ to generate ternary logic "1" during intermediate comparison states.

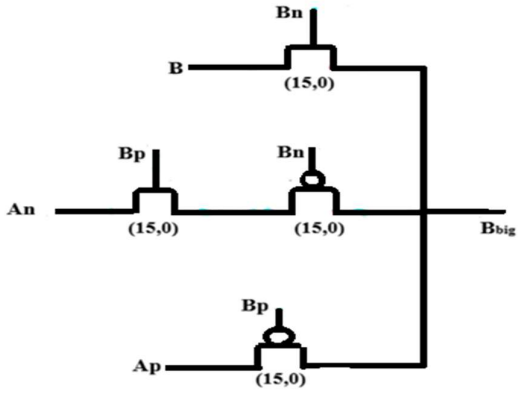

Figure 4.7 Schematic diagram of the B_{big}

Table 4.5 Truth table for B_{big}

INPUT A	INPUT B	B_{big}
0	0	0
1	0	0
2	0	0
0	1	2
1	1	0
2	1	0
0	2	2
1	2	2
2	2	0

Thus, only one path is activated at once based on the ternary input conditions to generate the desired logic "0","1","2" at the comparator output node BG. Three different conduction paths of the CNTFET perform the same operation to generate ternary logic levels "0", "1" and "2" at the output node based on the comparison condition. The upper CNTFET path serves as the equivalent pull-up network and charges the output to V_{DD} to create logic "2."

The middle CNTFET network acts as an equivalent intermediate path to transfer $V_{DD}/2$ for generating ternary logic "1". The lower CNTFET path acts as an equivalent pull-down network and pulls down the output node towards ground to generate logic "0.

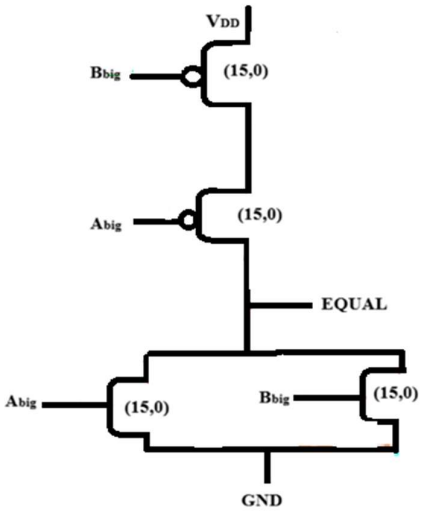

Figure 4.8 Schematic diagram of the EQUAL

In the proposed ternary comparator, there is only one conduction path active for a given input condition, so the output is stable and there is no conflict between charging and discharging networks. The circuit compares two ternary inputs and gives the states **"A>B", "A<B",** and **"A=B"** using controlled conduction paths of CNTFETs.

When "A>B", the pull-up path pulls the output to "V_{DD}" (logic 2). When "A<B", the pull-down path pulls the output to "0 V" (logic 0). For "A=B", the intermediate path goes through "$V_{DD}/2$", giving ternary logic "1".

Table 4.6 Truth table for Equal

INPUT A	INPUT B	EQUAL
0	0	2
1	0	0
2	0	0
0	1	0
1	1	2
2	1	0
0	2	0
1	2	0
2	2	2

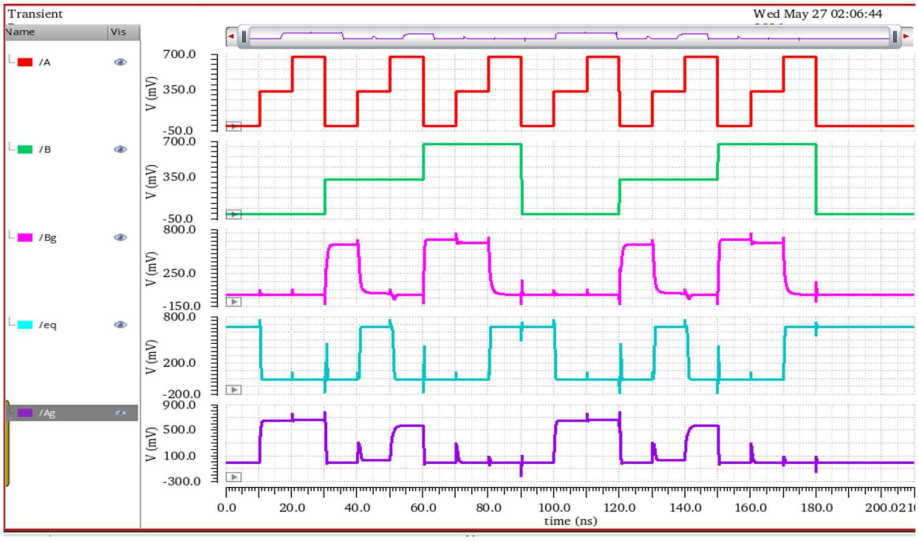

Figure 4.9 Input and Output waveforms of the circuits of A_{big}, B_{big}, Equal

4.3 POWER CALULATION

Table 4.7 Average power calculation

OPERATION	NUMBER OF TRANSISTORS	AVERGAGE POWER (nW)	POWER REDUCED
STAND	12	1.56	85.77%
STOR	12	4.16	73.5%
STNAND	18	5.42	75.62%
STNOR	18	2.32	89.66%
STXOR	16	3.11	84.96%
ABIG	20	1.94	94.70%
BBIG	20	1.90	94.81%
EQ	20	2.95	91.94%
SUM	18	4.49	80.9%
CARRY	18	1.95	75.67%

From the results of power analysis, the designed CNTFET based ternary logic circuits have presented satisfactory performance in power saving without losing its small dimension and high speed. It has seen from the simulation of proposed standard ternary logic gates STAND, STOR, STNAND, STNOR and STXOR, there is significant saving in power dissipation with lower utilization of transistors that implies reliable performance in logic operation for switching and also with its good ternary comparisons. As compared to the output from other ternary comparators such as A_{big}, B_{big}, Equal, they have the same advantage of power saving that represents good efficiency in switching, effective ternary comparison and better operation. With the SUM and CARRY of ternary full adder there has been good saving in power with simple hardware complexity.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

It can be seen from the work that ternary logic with GAA-CNTFET technology has a great promise to be a promising alternative to traditional binary circuit design for future nanoelectronics applications. Based on intermediate logic generation, unary operators, ternary gates, etc., the designed circuits are capable of implementing arithmetic and compare functionality with a simpler circuit and with less hardware. The full adder and comparator designed has stable functioning at all ternary input cases, and they possess smooth signal transition characteristics. It is concluded that ternary circuit based on GAA-CNTFET is the one of potential candidate for high performance VLSI systems and multi-valued logic application for its low power consumption and hardware efficient structure.

5.2 FUTURE SCOPE

The proposed GAA-CNTFET-based ternary circuits have strong potential for future semiconductor industries due to their ability to reduce power consumption, chip area, and interconnection complexity. As the demand for energy-efficient and high-performance computing systems continues to grow, ternary logic can be explored for applications in artificial intelligence hardware, edge computing devices, data centres, IoT systems, and next-generation processors. The adoption of GAA transistor technology by leading semiconductor manufacturers also creates opportunities for integrating multivalued logic circuits into future nanoscale chips. Further development of ternary arithmetic units, memory systems, and processor architectures can help industries achieve higher computational density and improved performance while maintaining low power operation.

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KEERTI SINGH

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OBJECTIVE

Motivated VLSI postgraduate seeking an entry-level position in Digital IC Design, Physical Design, or Verification, where I can apply my skills in Verilog , ASIC design flow, Cadence Virtuoso, and Xilinx Vivado to contribute to efficient and innovative semiconductor solutions while growing as a hardware design engineer.

EDUCATION

Master of Technology in VLSI	Delhi Technological University, New Delhi	7.04 (till 3rd sem)	2024-2026
Bachelor of Technology in ECE	Madhav Institute of Technology & Science, Gwalior	6.5	2017-2021
12th (ICSE)	St. Mark's College, Jhansi	6.01	2017

TECHNICAL SKILLS

Design Tools	Cadence Virtuoso, Xilinx Vivado, LTSpice , PROTEUS, MPLAB
Programming & Scripting	Verilog , Linux, System Verilog ,C++(basics),TCL
Interested Courses	Digital Electronics , CMOS Digital VLSI Design, Physical Design in VLSI, Low Power design, Static Time Analysis, ASIC Flow, IP Protocols(AMBA,SPI.UART)

EXPERIENCE

Research Assistant

Delhi Technological University | May 2025 – Present

- Implemented **ternary** comparators **and full**-adder using **GAA CNTFET** architectures.
- Simulated designs in **CADENCE virtuoso** with **10nm Stanford VS-CNTFET VerilogA** model including realistic load capacitances.
- Analyzed **delay, power and power delay product (PDP)** across 0-trit, 1-trit, and 2-trit comparators.

Software Developer Intern

X2infotech | Feb 2021 – May 2021

- Designed responsive frontend for an online bookstore using HTML, CSS, Bootstrap and javascript.
- Proposed and implemented UI enhancements such as product filters and real-time availability to improve user experience.
- Integrated frontend interfaces with backend APIs using PHP for dynamic content rendering and seamless user interaction.

ACADEMIC PROJECTS

IC Layout Design of 3x8 Decoder | Apr 2025 – May 2025

Developed a 3x8 Decoder in **Cadence Virtuoso**, covering schematic capture, layout design, and full simulation flow. Conducted pre- and post-layout simulations to evaluate delay and power consumption. Performed DRC, LVS, and parasitic extraction to ensure physical and functional correctness, and analysed the effect of layout optimization techniques on performance metrics.

Design and verify Synchronous FIFO using Verilog | Feb 2025 – Mar 2025

Designed a synchronous FIFO buffer using Verilog in **Xilinx Vivado** with proper read/write control logic. Handled full and empty conditions accurately for reliable data transfer within a single clock domain. Verified functionality through simulation and custom testbenches to ensure correct operation.

Traffic light Controller using Verilog | Dec 2024 – Jan 2025

Designed, implemented, and synthesized a Verilog-based traffic light controller for a two-way intersection using **Xilinx Vivado**, incorporating vehicle-detection input signals. Developed finite state machine (FSM) logic to manage signal transitions dynamically based on real-time sensor data, and validated functionality through simulation waveforms and timing analysis.

Design Frequency divider | Oct 2024 – Nov 2024

Designed and implemented a frequency divider circuit utilizing D flip-flops in **Cadence Virtuoso**, including schematic capture, transient simulation, and full-custom layout. Verified circuit functionality through extensive simulations and performed DRC and LVS checks to ensure compliance with design rules and layout accuracy.

CO-CURRICULAR

- Participated in a PCB Design Workshop organized by the IETE Student Forum, MITS Gwalior.
- Attended a DTMF-Controlled Mobile Robotics Workshop, exploring signal-based control mechanisms.

ACHIEVEMENTS AND LEADERSHIP

- Certified in **Physical Design** by **NPTEL**, under **Prof. Indranil Sengupta, IIT Kharagpur**.
- Teaching Assistant under Assistant Prof. Vinay Kumar, supporting Embedded Systems lab sessions.
- Qualified GATE 2024 (ECE) and CAT 2023.
- Solved Verilog HDL problems on HDLBits, strengthening RTL design skills.
- Member, IETE Student Forum, MITS; organized workshops on PCB design and robotics.