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CHAPTER 1 - INTRODUCTION

1.1 Background

The increasing use of smartphones, infotainment systems, navigation devices, and portable electronics in modern vehicles has increased the demand for efficient USB charging technologies. Earlier USB charging standards supported only fixed 5V operation with limited power capability, which became insufficient for modern fast-charging devices.

USB Type-C and USB Power Delivery (USB PD) technology introduced higher power transfer capability along with programmable voltage negotiation for modern electronic devices [1][2]. Several researchers and semiconductor manufacturers have previously worked on USB PD-based fast-charging systems for portable and automotive applications [3].

Researchers have examined fast-charging converter designs and methods for using USB PD. Yao et al. studied how buck converters operate in USB Power Delivery, focusing on efficiency improvements and current sensing [4]. Bryant and Kazimierczuk explored how buck converters switch and perform under different loads [5].

Recent studies have also looked at USB Type-C Power Delivery communication. Liu et al. examined how to use the USB-PD protocol and design fast-charge controllers for programmable charging [6]. Delshadpour et al. studied the communication architecture and BMC signaling in USB Type-C Power Delivery to ensure reliable communication [7].

Other research has focused on designing efficient USB-C charging converters. Mukherjee et al. explored resonant converter methods to improve efficiency in USB-C Power Delivery [8]. Tran et al. demonstrated how to build a battery charger using a USB Type-C Power Delivery interface for modern charging systems [9].

Automotive charging systems present additional challenges. Automotive charging systems face additional challenges, including changing battery conditions, electrical noise, heat, and the need for compact hardware. Dusmez and Khaligh discussed automotive power electronic systems and highlighted the importance of efficient power conversion and managing heat in vehicles [10]

Injoinic, Monolithic Power Systems (MPS), and Renesas have developed automotive USB PD charger ICs that support programmable-voltage operation, PPS functionality, integrated protection features, and compatibility with multiple charging protocols [11], [12], [13], [14].

However, most available studies mainly focus on theoretical converter analysis or individual charger implementation. Few practical comparisons exist of different automotive USB Type-C Power Delivery charger ICs tested in real lab conditions.

This study aims to evaluate various automotive USB PD charging s at the hardware level, focusing on efficiency, protocol support, protection, thermal performance, and integration with automotive TFT display systems.

1.2 Motivation for the work

Electric two-wheelers and scooters now feature advanced infotainment systems, TFT display clusters, wireless connectivity, and USB charging ports, allowing riders to charge their phones whenever needed.

Mobile devices are frequently used for navigation, communication, and infotainment purposes during vehicle operation, thereby necessitating onboard charging support, which becomes an important factor.

Conventional USB charging ports in many automotive systems offer limited power and can't support modern fast-charging smartphones. USB Type-C Power Delivery technology enables higher power transfer and faster charging of portable devices [15].

This work was driven by the need to develop a USB Type-C Power Delivery charging solution for an automotive system with a TFT display, intended for electric two-wheeler applications.

The objective was to develop a compact, efficient charging interface to power mobile devices during vehicle operation. Since automotive systems operate under fluctuating battery voltages and are exposed to electrical noise, thermal variations, and varying load levels, careful selection and evaluation of charger integrated circuits are necessary.

Another motivation for this work was to compare charger behavior through experimental hardware testing. While datasheets offer theoretical efficiency and protocol details, real-world performance is affected by passive component choices, thermal effects, switching behavior, and load characteristics [16], [17], [18].

Therefore, hardware testing was necessary to evaluate the suitability of different charger ICs for automotive applications.

This work also included schematic design, protocol analysis, load testing, oscilloscope waveform observation, and protection verification using laboratory instruments and evaluation boards.

1.3 Problem statement

Integrating USB Type-C Power Delivery (USB PD) chargers into 2 vehicle electric vehicle systems introduces several design and hardware challenges. Charging s must support a wide range of devices while maintaining stable functionality, high efficiency, and reliable protection during dynamic operating environments.

For automotive applications such as electric scooters and TFT displays, a compact, efficient USB PD charger is essential for reliable mobile device charging.

The main problem is how the charger IC will behave under different conditions, such as while driving or in heat, so we have to consider every possible damage that can be caused.

Choosing the charger IC involves considering several parameters, including buck converter efficiency, the components near the IC, and the inductor's DCR.

High-frequency converter operation can generate switching noise and voltage spikes, which may affect USB communication and nearby TFT circuitry in compact automotive systems [19].

Continuous high-power operation in compact TFT systems can raise temperatures within the converter power stage, making heat dissipation and thermal management important design considerations [20].

Automotive electrical systems are subject to battery voltage fluctuations, transient disturbances, load-dump conditions, and switching noise, which affect the reliability and protection performance of USB PD chargers [21].

Selection of an appropriate charger power rating is important for automotive USB PD integration. In this work, the primary focus was on implementing a 36W automotive USB PD charging solution suitable for mobile device charging in the S1X Electric scooter.

However, higher-power charger ICs were also evaluated to assess whether they provide better efficiency, protocol flexibility, and future scalability for automotive systems [22].

While charger IC datasheets provide theoretical efficiency curves for comparing with real-time data and protocol specs, hardware testing is essential for an accurate evaluation when selecting the best IC for our application.

This work compares three different USB PD charger ICs in terms of efficiency, protocol compatibility, hardware complexity, protection features, and suitability for TFT display integration in the SIX cluster board.

1.4 Objective of the work

- Design and construct an automotive USB Type-C Power Delivery charger using the Injoinic IC on a TFT display board.
- To experimentally evaluate the efficiency of MPS and Renesas Board.
- To analyze buck converters under various USB PD voltage profiles and constant current load levels during testing.
- To study load regulation and output voltage characteristics.
- Use the PD analyser to verify USB Power Delivery communication and available charging protocols.

- To assess the impact of passive components on IC selection.
- To examine the protection mechanisms, including overvoltage protection (OVP), under voltage protection (UVP), short-circuit protection (SCP), and hiccup mode behaviour.
- To evaluate automotive USB PD charger ICs based on efficiency, protocol compatibility, hardware complexity, and their fit for EV charging applications.

1.5 Scope of the work

This work encompasses practical hardware implementation and laboratory testing of EV USB Type-C Power Delivery charging systems. It primarily focuses on electric two-wheelers, aiming to develop a compact, efficient USB PD charging interface that enables mobile device charging while the vehicle is in use.

The study examines the experimental assessment and hardware validation of USB PD chargers built with a synchronous buck converter, using laboratory instruments. Additionally, includes analysis of PCB implementation considerations, passive component selection, switching stability, and thermal behavior affecting converter performance [7], [1].

USB Power Delivery communication over CC lines and legacy DP/DM-based charging protocol behavior were analyzed using PD analyzer tools. Protection analysis includes evaluation of overvoltage protection (OVP), under voltage protection (UVP), short-circuit protection (SCP), and hiccup mode restart behavior.

The scope of the present work is limited to laboratory-level evaluation and does not include automotive EMI/EMC compliance testing, environmental qualification testing, thermal chamber analysis, long-term reliability testing, or production-level hardware optimization.

Advanced automotive qualification testing, such as EMI/EMC compliance, environmental reliability testing, thermal chamber analysis, and large-scale production validation, is beyond the scope of the present work.

1.6 Organization of thesis

The thesis is organized from the basic understanding of USB charging technologies to the practical implementation and testing of automotive USB Type-C Power Delivery systems.

The first chapter introduces the background of automotive USB PD charging, as well as the motivation, problem statement, objectives, and scope of the present work.

Chapter 2 covers the development of USB charging technologies, including USB Type-C architecture, USB Power Delivery communication, PPS operation, and automotive

charging applications. It also reviews previous research on fast charging and conversion characteristics.

Chapter 3 primarily covers the hardware implementation of the chosen USB PD charging s. It discusses the architecture and operation of the Injoinic IC, MPS Board, and Renesas board, including schematic design, power stage setup, communication interfaces, and TFT display integration.

Chapter 4 outlines the experimental setup and testing procedures for practical validation, including efficiency testing, load regulation analysis, protocol verification, and protection testing across various operating conditions.

Finally, Chapter 5 offers a comparative analysis of the chosen chargers, focusing on efficiency, protocol support, implementation complexity, and practical performance. It also includes the overall conclusion and the future scope of the work.

CHAPTER 2 - LITERATURE REVIEW

2.1 Introduction

Modern portable electronic devices need charging systems that provide higher power, better efficiency, and faster charging times. Previously, USB charging standards primarily supported fixed-voltage, low-power configurations, which are no longer sufficient for today's smartphones, tablets, laptops, and automotive infotainment systems.

Consequently, fast-changing technologies and programmable power conversion systems have become increasingly important. Several researchers have investigated converter topologies suitable for USB PD applications.

Erickson and Maksimovic discussed the importance of switching converter design and regulation techniques for high-efficiency DC-DC power conversion systems [28].

Choi et al. studied thermal behaviour in high-power USB charging systems and reported that converter efficiency and PCB thermal management strongly influence charging reliability during continuous operation [18].

Converter switching performance and EMI have been widely studied for compact chargers. Matsuda and Ito analyzed and conducted noise in high-frequency DC-DC converters and proposed filtering to improve stability [19]. Wang and Blaabjerg discussed reliability issues under thermal and electrical stress [29]

Research related to USB Power Delivery communication and charging control has also increased significantly. Zhao et al. discussed PPS-based charging operation and demonstrated that programmable voltage adjustment can improve charging efficiency while reducing unnecessary thermal losses inside mobile devices [20].

Several studies have also focused on the practical implementation of USB Type-C charging systems. Kim et al. presented compact USB PD charger architectures for portable applications and highlighted the influence of switching frequency and passive component selection on converter efficiency [21].

Although earlier research has examined converter operation and USB PD communication methods, there remains a limited number of practical comparisons of various automotive USB Type-C Power Delivery charger ICs under laboratory conditions. Table 2.1 provides a comparison of fast charging protocols.

Therefore, this work focuses on the experimental evaluation of USB PD chargers with respect to efficiency, protocol capability, thermal behavior, protection performance, and suitability for implementation in automotive TFT display integration.

Table 2.1: Comparison of Fast Charging Protocols

Protocol	Communication Method	Voltage Profiles	Max Power	Control Method
USB 2.0	None	Fixed 5V	2.5W	Fixed Supply
USB BC1.2	DP/DM	Fixed 5V	7.5W	Current Detection
Qualcomm Quick Charge (QC 2.0/3.0)	DP/DM	5V / 9V / 12V / 20V	Up to 36W	Voltage Negotiation
Samsung AFC	DP/DM	5V / 9V / 12V	Up to 18W	Adaptive Voltage Control
Huawei SCP/FCP	DP/DM	5V / 4.5V / 10V	Up to 40W	Current-Based Fast Charging
USB Power Delivery (USB PD 3.0)	CC1 / CC2	5V / 9V / 12V / 15V / 20V	Up to 100W	PDO Negotiation
USB PD 3.1 EPR	CC1 / CC2	28V / 36V / 48V	Up to 240W	Extended PDO Negotiation
PPS (Programmable Power Supply)	CC1 / CC2	3.3V–21V (Programmable)	Up to 100W	APDO Based Dynamic Control

2.2 Evolution of USB Charging Technologies

USB standards such as USB 1.0 and USB 2.0 were developed for low power data communication and supported limited charging capability at fixed 5V operation only.

USB 2.0 provides a current up to 500mA, enabling around 2.5W of power. As smartphone batteries grew larger and their power needs increased, traditional USB charging no longer sufficed for fast and efficient charging.

To enhance charging performance, the USB Implementers Forum created the Battery Charging Specification (BC1.2), allowing charging currents up to 1.5A at 5V through dedicated ports. BC1.2 introduced charger detection via DP and DM lines. Nevertheless, charging remained dependent on a fixed 5V supply, resulting in higher cable currents and greater device heating during charging.

USB Power Delivery Revision 3.0 implemented Programmable Power Supply (PPS) operation, which dynamically adjusts charger output voltage according to battery

charging requirements. PPS operation improves charging efficiency and reduces thermal stress by minimizing internal conversion losses in mobile devices during fast charging.

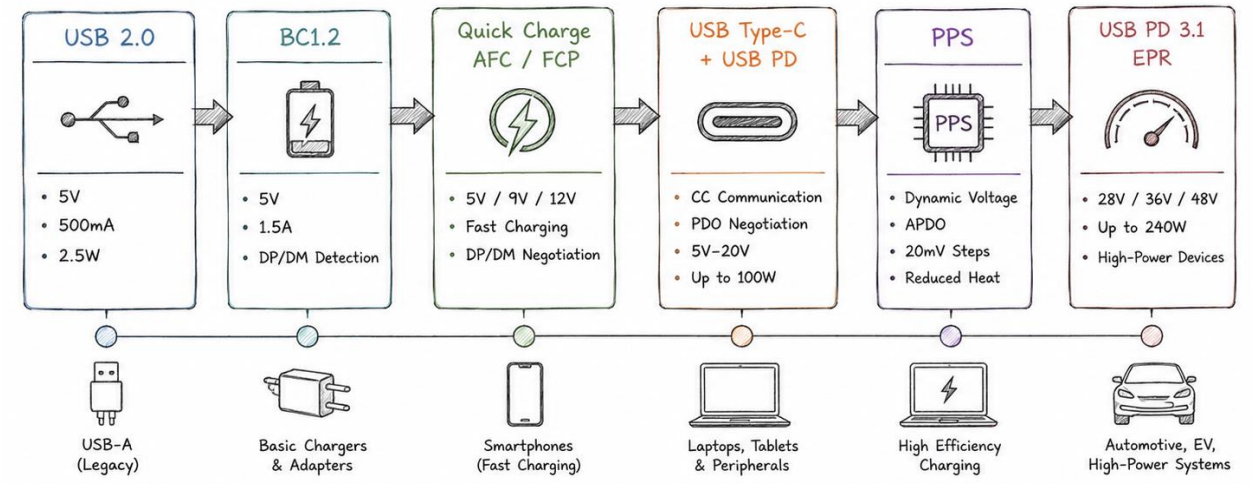

Figure 2.1: Evolution of USB Charging Technologies

USB Power Delivery Revision 3.1 further expanded charging capability through Extended Power Range (EPR) operation, supporting voltage levels up to 48V and power delivery capability up to 240W [22].

Table 2.2: Conventional USB Power Ratings

USB Standard	Output Voltage	Max Current	Max Power	Major Limitation
USB 1.0	5V	100mA	0.5W	Very low charging capability
USB 2.0	5V	500mA	2.5W	Slow charging
USB 3.0	5V	900mA	4.5W	Fixed voltage operation

2.3 Battery Charging Specifications (BC1.2)

To improve power capability beyond conventional USB standards, the USB Implementers Forum (USB-IF) introduced the Battery Charging Specification (BC1.2). Earlier USB standards were mainly intended for data communication and supported limited current capability. BC1.2 was later developed to support higher current delivery for smartphones and portable electronic devices.

The BC1.2 specification categorizes USB ports into types such as Standard Downstream Port (SDP), Charging Downstream Port (CDP), and Dedicated Charging Port (DCP). Among these, DCPS support current delivery up to 1.5A, enabling faster charging than traditional USB ports. Refer to table 2.3 for a discussion of BC1.2 port types.

BC1.2 also introduced charger detection through DP and DM communication lines. During detection, the connected device identifies the port type and determines the allowable current limit before starting higher current operation. This helped portable devices safely draw more current from compatible charging ports.

Table 2.3: BC1.2 Port Types

Parameter	SDP (Standard Downstream Port)	CDP (Charging Downstream Port)	DCP (Dedicated Charging Port)
Data Communication Support	Supported	Supported	Not Supported
Voltage	5 V	5 V	5 V
Current Capability	500 mA	Up to 1.5 A	Up to 1.5 A
Typical Application	PCs, USB devices	Laptops, USB hubs	Wall chargers, adapters
Main Limitation	Slow charging	Fixed 5 V only	No data communication

2.4 Quick Charge Technologies

Today, as smartphone battery capacities increase, standard 5V USB charging no longer sufficiently reduces charging times. Consequently, some manufacturers have adopted higher voltage charging techniques to accelerate the process. Table 2.4 compares different versions of Qualcomm Quick Charge.

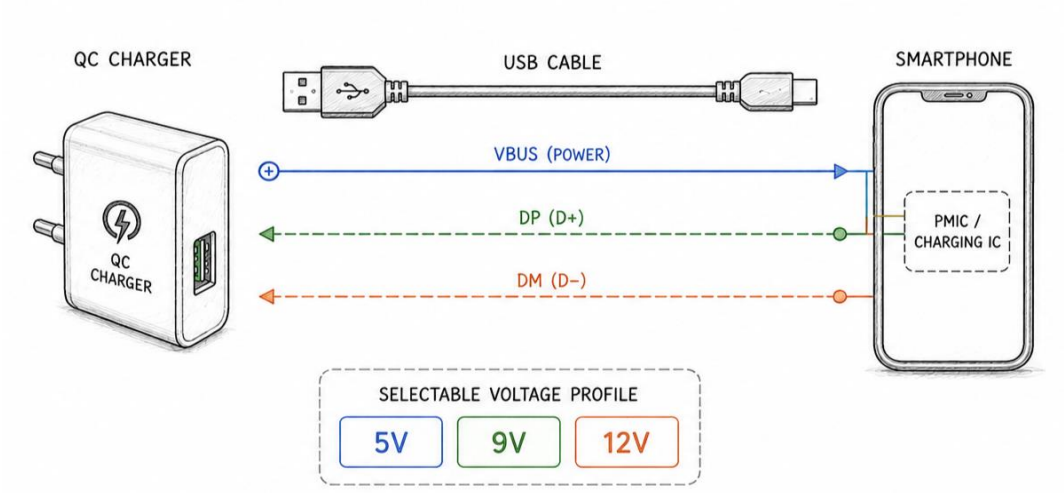

Figure 2.2: QC Voltage Negotiation through DP/DM communication

Quick Charge technology features variable voltage operation at 9V and 12V profiles, tailored to device needs. Increasing the voltage also enables higher power transfer without significantly raising the cable current. Figure 2.2 shows how the communication between the charger and phone works through QC protocol.

QC communication utilizes DP and DM signaling lines, enabling compatible devices to request specific voltage levels from the charger [1]. Various Quick Charge versions, such as QC2.0 and QC3.0, have enhanced voltage negotiation methods and added dynamic voltage adjustment to improve charging performance.

Table 2.4: Comparison of Qualcomm Quick Charge Versions

QC Version	Output Voltage	Max Power	Communication Method	Feature
QC1.0	5V	10W	DP/DM	Higher current charging
QC2.0	5V/9V/12V	18W	DP/DM voltage signaling	Variable voltage charging
QC3.0	3.6V–20V	18W	INOV algorithm	Dynamic voltage adjustment
QC4/QC4+	USB PD compatible	27W	USB PD + DP/DM	Improved efficiency & thermal performance

However, Quick Charge technology remained mainly proprietary and vendor-specific, like in Xiaomi, Asus, and Motorola, which led to compatibility issues across various charging systems. QC chargers can also charge devices such as MacBook and iPads at faster speeds than standard.

2.5 Introduction to USB C

USB Type-C was developed to overcome earlier USB connector limitations like orientation, current, size, and charging speed. It offers a compact, reversible interface capable of higher power and faster communication.

The reversible connector structure simplifies cable insertion, thereby enhancing user convenience. Additionally, the connector accommodates higher current levels necessary for fast-charging applications in smartphones.

USB Type-C features Configuration Channel pins that detect cable orientation, identify chargers, and facilitate communication between source and sink devices. These CC lines handle USB Power Delivery communication from battery to charger and enable voltage negotiation during charging.

In charging applications, USB Type-C also supports high-speed data transfer and alternative mode communication for display and multimedia uses. Its small size, combined with charging and communication functions, makes it a versatile choice.

2.5.1 USB Type-C Connector Architecture

USB Type-C is a reversible 24 pin connector standard used for high speed data transfer and USB Power Delivery operation. Unlike earlier USB connectors, the Type-C connector can be inserted in either orientation because of its symmetrical pin arrangement.

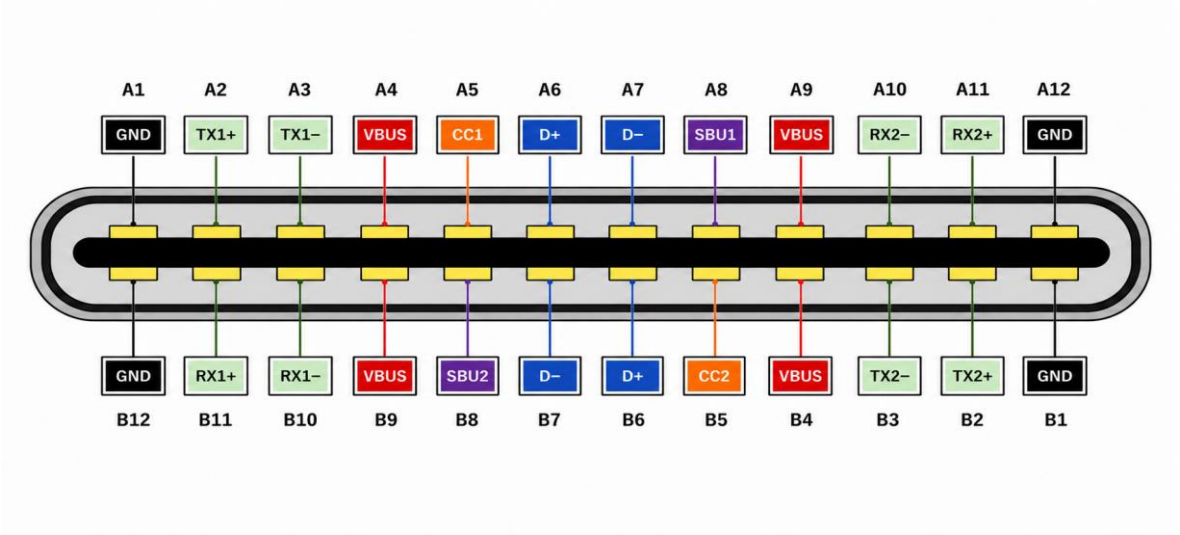

Figure 2.3: USB Type-C Connector Pin Diagram

Under USB PD 3.1 Extended Power Range (EPR) specifications, the connector can support power delivery up to 48V and 5A operation. The connector contains multiple functional pins including VBUS, GND, CC1, CC2, D+, D−, SBU, and SuperSpeed differential communication pairs.

In USB Type-C interfaces, the CC pins play an important role in enabling USB Power Delivery operation and cable orientation detection. During connection, the active CC line is selected automatically depending on the connector orientation, after which USB PD communication is established between the source and sink devices.

For electronically marked cables supporting higher current capability, the unused CC pin can provide a VCONN supply required for cable side circuitry operation

VBUS pins carry VBUS power, while ground pins provide the return current path. The CC1 and CC2 pins are mainly used for cable orientation detection, source and sink identification, and USB Power Delivery communication. Figure 2.3 shows the USB Type-C pin connector pin names.

Depending on cable orientation, one CC pin becomes active for communication while the other may provide VCONN supply for electronically marked cables. Multiple VBUS and GND pins help distribute current and reduce connector resistance during high-power charging.

2.5.2 Configuration Channel (CC) Communication

The Configuration Channel (CC) pins form the primary communication interface in USB Type-C charging systems. Two CC pins, namely CC1 and CC2, are available in the connector for cable orientation detection, device attachment detection, and USB Power Delivery communication.

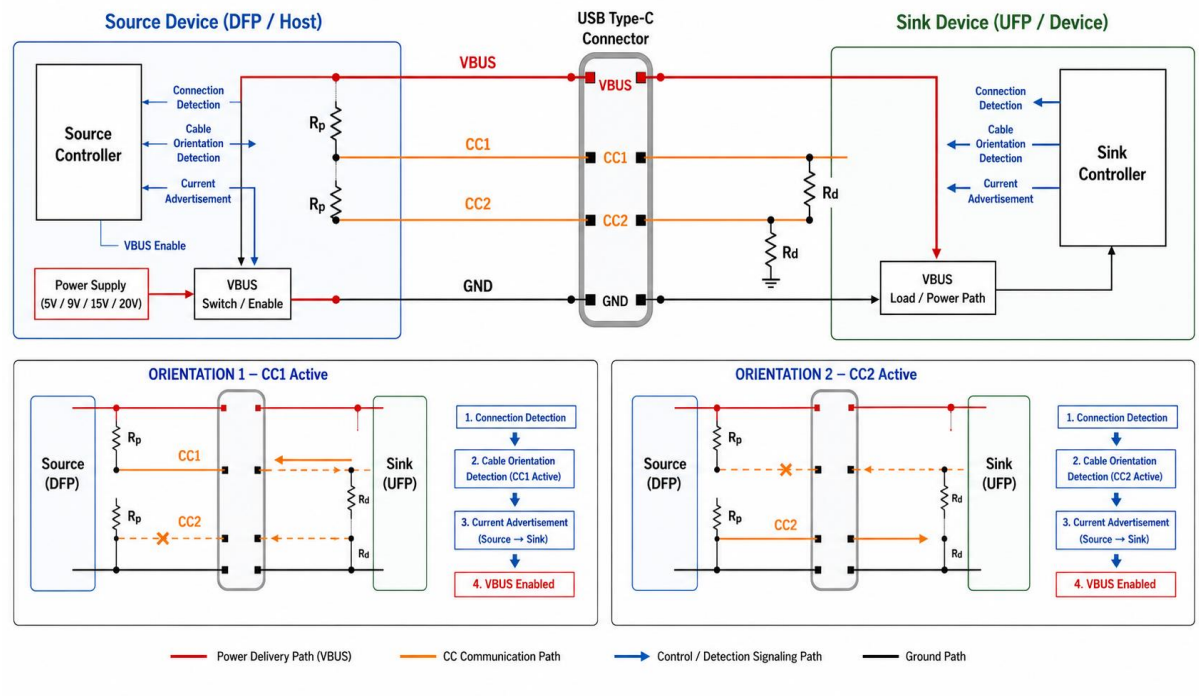

Figure 2.4: CC Communication and Connection Detection

Depending on cable orientation, either CC1 or CC2 becomes active for communication between the charger and the connected device. The source side has pull-up resistors (Rp), while the sink side uses pull-down resistors (Rd) as shown in Figure 2.4.

During USB PD operation, communication takes place over the active CC line using Biphase Mark Coding (BMC) signaling [7]. The sink device then requests the required power profile.

2.5.3 USB PD Voltage Profiles

USB PD supports multiple predefined voltage and current profiles called Power Data Objects (PDOs), allowing the charger and connected device to negotiate suitable operating conditions according to power requirements.

Unlike conventional fixed voltage USB charging systems, USB PD utilizes Configuration Channel (CC) communication for programmable power negotiation between source and sink devices.

During protocol negotiation, the source device advertises its supported PDO profiles, after which the sink device requests an appropriate voltage and current level according to device power requirements.

USB PD 3.1 introduced Extended Power Range (EPR) operation supporting voltage levels up to 48V. In addition to fixed PDO operation, USB PD also supports APDO-based PPS operation.

Table 2.5: USB PD voltages Profiles and Power Capability

USB PD Type	Voltage Profile	Maximum Current	Maximum Power	Applications
Standard Power Range (SPR)	5V	Up to 3A	15W	Smartphones, accessories
SPR	9V	Up to 3A	27W	Fast charging smartphones and tablets
SPR	12V	Up to 3A	36W	Tablets, portable devices
SPR	15V	Up to 3A	45W	Tablets
SPR	20V	Up to 3A	60W	Laptops, docking systems
SPR (E Marked Cable)	20V	Up to 5A	100W	High power laptops, monitors
Extended Power Range (EPR)	28V	Up to 5A	140W	Gaming laptops, workstations
EPR	36V	Up to 5A	180W	Industrial and power tools
EPR	48V	Up to 5A	240W	Automotive, high power systems

2.5.4 Programmable Power Supply (PPS)

PPS is a feature in USB Power Delivery that enables the charger to dynamically adjust its output voltage and current based on the device's charging needs. Unlike fixed PDO operation, which offers preset voltage levels such as 5V, 9V, 15V, and 20V, PPS allows for continuous voltage adjustment. Table 2.6 compares fixed PDO and PPS operation.

In PPS mode, the output voltage can be finely tuned in steps of about 20 mV, and the current adjustment typically has a resolution of 50 mA. The PPS operating ranges, which depend on the charger's capabilities and the Augmented Power Delivery Object setup, include 3.3V–12V, 3.3V–9V, and 3.3V–15V. Table 2.7 displays the ranges of PPS and their application [22].

During charging, the sink device communicates with the source via the CC line using APDOS to exchange USB PD messages.

Table 2.6: Comparison of fixed PDO and PPS Operation

Parameter	Fixed PDO Operation	PPS Operation
Voltage Type	Fixed voltage levels	Dynamically adjustable voltage
Voltage Profiles	5V, 9V, 15V, 20V	3.3V–11V / 16V / 21V
Voltage Resolution	Fixed only	20 mV steps
Current Resolution	Fixed current	50 mA steps
Communication Type	PDO	APDO
Charging Efficiency	Moderate	High
Thermal Performance	Higher heat generation	Reduced thermal losses
DC-DC Conversion Loss	Higher	Lower
Battery Optimization	Limited	Improved
Typical Applications	Laptops, tablets	Fast charging smartphones

Table 2.7: Typical PPS Voltage Ranges and Application

PPS Voltage Range	Maximum Power Capability	Applications
3.3V – 11V	Up to 45W	Smartphones
3.3V – 16V	Up to 65W	Tablets, ultrabooks
3.3V – 21V	Up to 100W	High power USB PD devices

2.5.5 USB PD Communication and Negotiation

USB PD communication starts only after the cc line communication is built. After connection establishment, the charger shows the supported voltages and current profiles to the connected device so that it can accept according to its needs.

The sink which is on the phone side selects PDO based on its required voltage and current level. Once the request is accepted, a power contract is established and the charger transitions VBUS to the negotiated voltage level.

Communication between the charger and connected device takes place over the active CC line using Biphase Mark Coding (BMC) signaling. During charging, the connected device may periodically request different voltage or current levels depending on battery condition and power requirement.

2.5.6 DP/DM Based Charging Communication

Earlier fast charging standards such as QC, AFC, FCP, and BC1.2 relied on DP and DM signaling for charger detection and voltage selection. Different charging protocols use specific voltage signaling methods on DP and DM pins to identify charger capability and supported charging modes.

In BC1.2 operations, DP and DM lines are used for charger type detection and higher current operation indication. QC protocols also support voltage selection through predefined DP/DM voltage combinations for different charging profiles.

Many automotive USB charger ICs continue to support DP/DM based communication in addition to USB PD operation in order to maintain compatibility with legacy charging devices.

During practical testing, protocol analyzers such as Charger LAB power z can monitor supported charging protocols, negotiated voltage profiles, and charging behavior under different operating conditions. Voltages at DP/DM pins can also be seen by this device.

2.6 Conclusion

In this chapter, I reviewed the development of USB charging technologies from conventional 5V USB charging to modern USB Type-C Power Delivery systems. Earlier charging methods provided limited power capability, while newer technologies such as USB PD and PPS that enabled higher power transfer, programmable voltage control, and improved charging efficiency.

The literature review showed that efficiency of the converter, thermal performance, communication stability, and passive component selection can play an important role in fast charging systems. It was also observed that automotive charging applications require reliable protection and stable operation due to fluctuating vehicle battery conditions and electrical noise.

Although many studies discussed USB PD communication and converter performance, limited practical comparison of charging controller ICs through hardware testing was found. This created the basis for the experimental work carried out in this thesis.

CHAPTER 3 - HARDWARE EXPERIMENTAL SETUP

3.1 Automotive USB PD Charging System Architecture

The automotive USB Type-C Power Delivery charging system developed in the work consists of a vehicle battery input stage, protection circuitry, synchronous buck converter based USB PD charger, USB Type-C communication interface. The system was designed for electric two wheeler applications requiring compact mobile charging support as shown in fig 3.1.

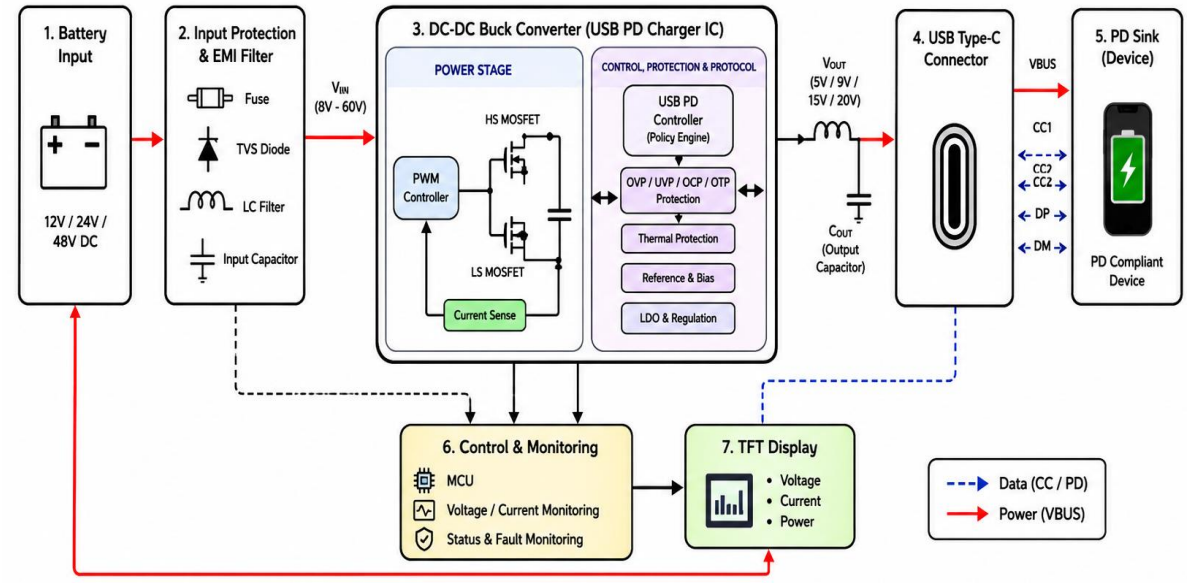

Figure 3.1: Overall architecture of the implemented USB PD charging system

Input power is sourced from the vehicle battery system through an input filtering section and a protection stage that includes reverse polarity protection. These protection circuits ensure stable operation despite automotive voltage fluctuations and help filter out noise.

The power conversion stage is implemented using a synchronous buck converter architecture integrated within the USB PD charger IC. The converter regulates output voltage according to negotiated USB PD operating profiles under varying load conditions.

USB PD communication and voltage negotiation occur via CC lines in the USB Type-C interface. Legacy DP/DM protocols also support compatibility with non-PD devices.

Protection features such as overvoltage protection (OVP), overcurrent protection (OCP), short circuit protection (SCP), and thermal shutdown are built into the charging system to ensure dependable performance.

3.2 Injoinic IC Architecture and Operating Principle

The Injoinic IC is an automotive-grade synchronous buck converter integrated circuit for USB Type-C Power Delivery chargers, tailored for fast charging. It operates within an input range of 7.3V to 29.5V and can be programmed to output up to 12V, delivering a maximum power of 36W [11], [24].

The pin diagram of Injoinic IC is in Figure 3.2, and the IC combines internal power MOSFETs, buck converter control, USB PD communication, current sensing, and protection in one chip. It regulates output voltage based on the charging profile under different loads.

The converter can operate in both constant-voltage and constant-current modes, depending on the charging conditions and load requirements. It also features a soft start function to minimise inrush current during startup and enhance transient stability.

The Injoinic IC supports multiple fast charging protocols, including USB PD, PPS, QC, AFC, FCP, and BC1.2. USB PD communication takes place via CC lines, while older protocols communicate through DP and DM lines.

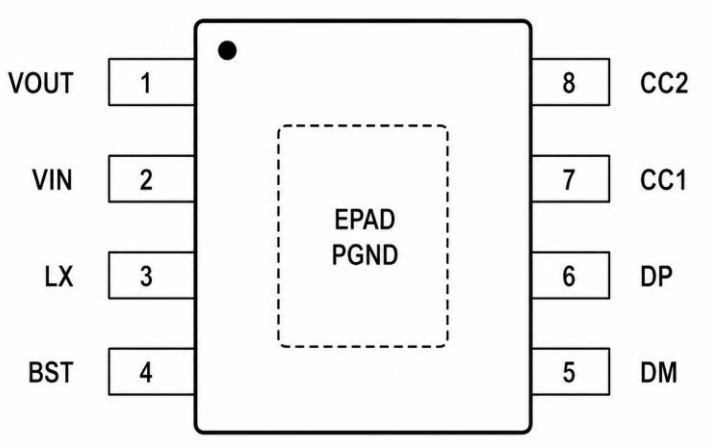

Figure 3.2: Pin Diagram of Injoinic IC

3.2.1 Injoinic IC Internal Architecture

The IC's internal architecture includes a synchronous buck converter stage, a USB PD communication controller, gate-driver circuitry, current-sensing blocks, feedback-control circuitry, and integrated protection modules [11], [24]. Figure 3.3 illustrates the functional block diagram of the Injoinic IC.

The synchronous buck converter controls VBUS output to follow the negotiated charging profile under different load conditions. USB PD communication and charging protocol detection are handled by the internal protocol controller via CC and DP/DM interfaces.

The IC includes internal monitoring and protection features for overvoltage, overcurrent, short circuits, and thermal faults, ensuring reliable operation in automotive charging applications.

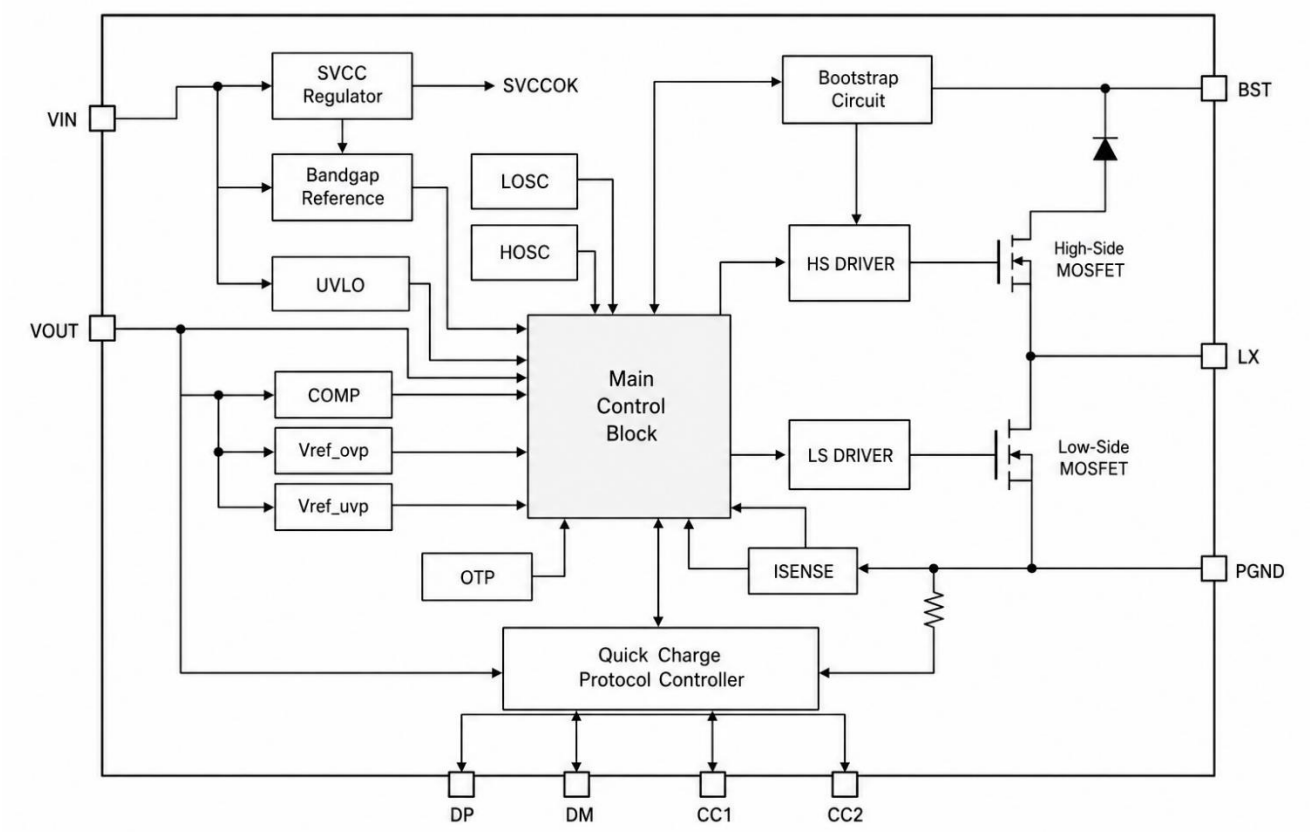

Figure 3.3: Functional Internal Architecture of Injoinic IC

3.2.2 Injoinic IC Functional Description

During startup, the IC begins by initializing its internal regulation and protocol control circuitry once it receives power from the automotive source. It then continuously monitors the USB Type-C interface via the CC communication lines to detect if a valid device is connected.

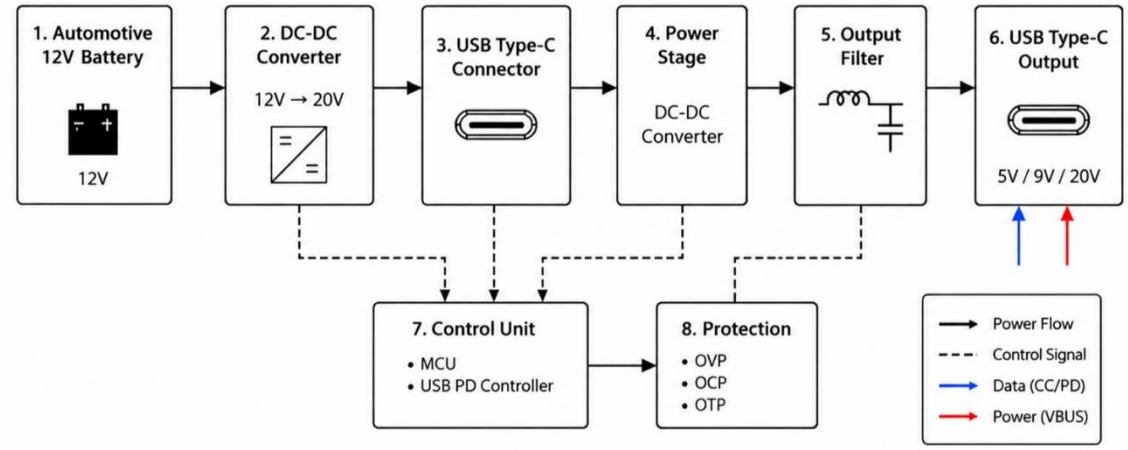

Figure 3.4: Functional flow diagram of Injoinic IC

Once a connection is successfully detected, the internal protocol controller determines the supported charging mode and shares the available charging profiles with the connected

device. Depending on the negotiated charging conditions, the converter adjusts the VBUS output to match the chosen voltage profile.

The converter continuously monitors output voltage, load current, and thermal conditions during operation to maintain stable regulation across various load scenarios. Figure 3.4 illustrates the flow of function. The IC enables USB PD communication via CC lines and supports legacy charging protocols through DP/DM interfaces, ensuring compatibility during device charging.

3.2.3 Schematic Design of Injoinic IC Based USB PD Charger

The schematic of the Injoinic IC was designed in Cadence and integrated into the S1X TFT cluster display board, which also features various functions. The circuit includes an input filtering stage that supplies 12V from the buck converter, a buck converter power stage inside the IC, communication interface circuitry that depends on the activation inputs, ESD protection, an output filtering stage, and a USB Type-C connector interface.

The VIN pin of the Injoinic IC was connected to a regulated 12V PD supply rail sourced from the vehicle power system. To reduce input ripple and enhance switching stability, input bypass capacitors of 10µF and 0.1µF were installed near the VIN pin.

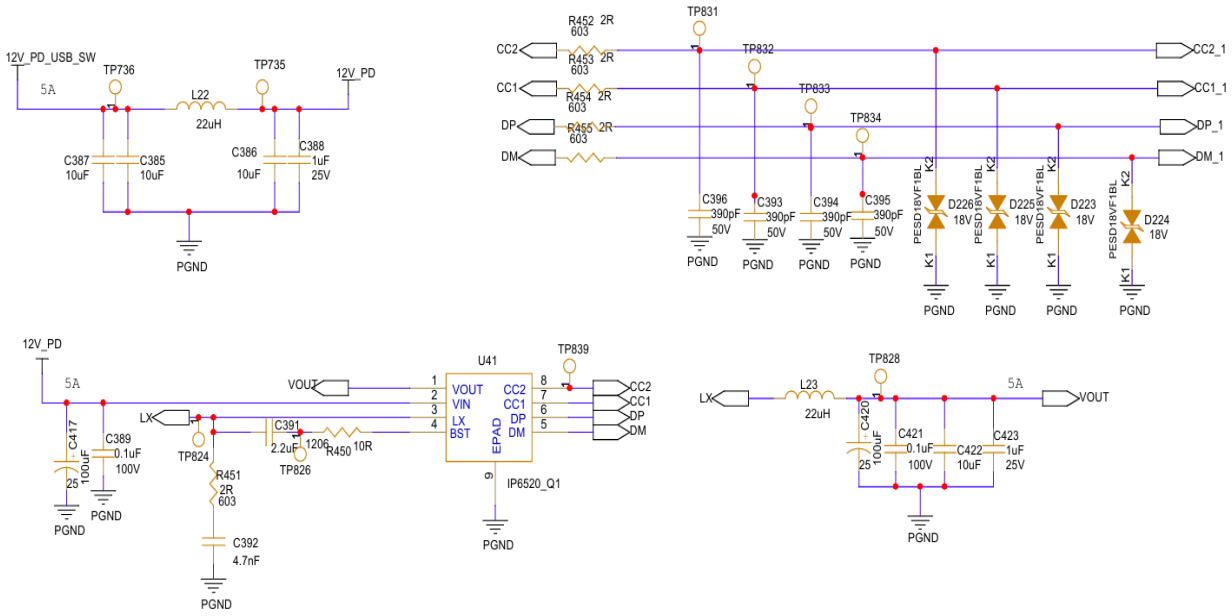

Figure 3.5: Injoinic IC Schematic Designed in Cadence

Figure 3.5 shows the Injoinic IC schematic, designed in Cadence. In the design, we have also included test points to verify whether the waveforms are correct. The LX pin shows the switching waveform when connected to a DSO.

The output stage features external inductors and filter capacitors positioned close to the switching node to decrease output ripple and enhance stability. RC snubber networks,

made of 390pF capacitors and 2Ω resistors, are connected near the LX switching node to minimise voltage ringing and overshoot caused by high-frequency switching.

ESD protection devices were connected across the CC1, CC2, DP, and DM communication lines using protection diodes to remove voltage or current spikes.

3.2.4 Input Power Stage Design

The input power stage is designed for fluctuating battery voltage caused by load changes, switching transients, and disturbances. It features bulk capacitors, EMI filters, reverse polarity protection, and transient suppression. Figure 3.6 shows the placement of capacitors and an inductor that filter the 12V input.

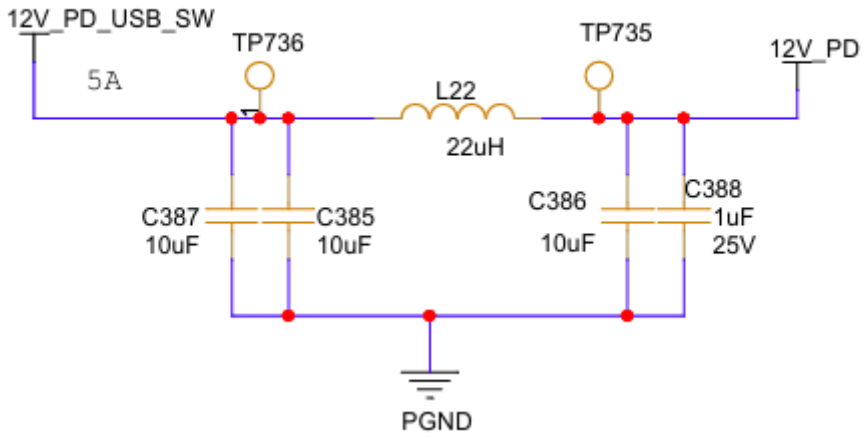

Figure 3.6: Injoinic IC Input LC Filter and Protection Circuit

3.2.5 Buck Converter Power Stage

The Injoinic IC's power conversion stage employs a synchronous buck converter design to transform automotive input voltage into stabilised USB PD output levels. It features internal high-side and low-side MOSFET switches, complemented by external inductors and output filter capacitors.

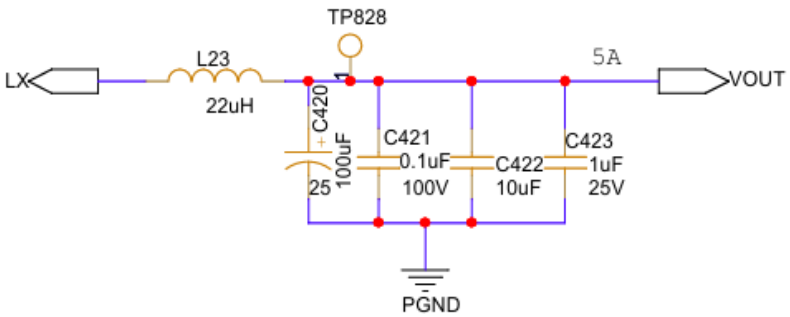

Figure 3.7: Injoinic IC Buck Converter Power Stage

The VIN pin draws input power from the automotive supply through filtering and protection circuitry. The SW node links to the external inductor and output filter stage for efficient power conversion and regulation. A bootstrap capacitor connects between the BST and SW pins to facilitate high-side gate drive operation.

The regulated VBUS output is produced after the inductor and output capacitor stage connected to the switching node. The FB pin monitors the output voltage via the feedback network to ensure a stable output under changing load conditions and various USB PD profiles.

3.2.6 Output Configuration and Passive Component Design

Output voltage regulation is managed via the feedback network connected to the FB pin, which monitors VBUS output to ensure stable operation across various USB PD voltage profiles.

The output voltage configuration depends on an external feedback resistor divider connected between VBUS, the FB pin, and ground. Figure 3.8 illustrates the passive components of the Injoinic IC in the schematic.

The chosen inductor value was based on switching frequency, ripple current, and load conditions. Selecting the inductor influences ripple current, transient response, and the overall stability of the converter during operation.

Input and output capacitors were selected considering voltage rating, ripple handling capability, and stability requirements during converter operation.

During testing, the ripple behavior of the output was heavily affected by how the capacitor was placed and routed near the switching node. Better stability was achieved after reducing the output power loop area close to the converter stage.

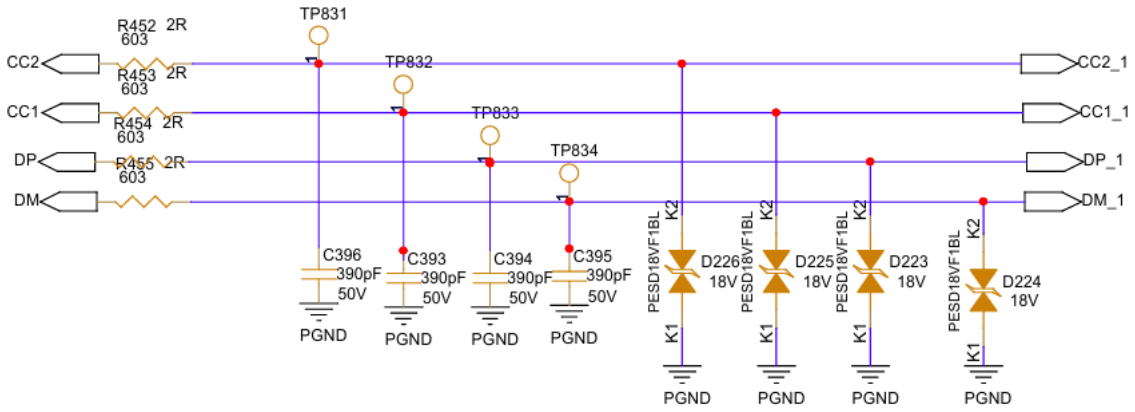

Figure 3.8: Injoinic IC Passive Component Placement in Schematic

3.2.7 TFT Display Board Integration

The Injoinic IC-based USB PD charging circuit was integrated into the 5-inch TFT cluster display board used for electric two-wheeler applications, as shown in Figure 3.9. The compact TFT enabled the implementation of the automotive USB Type-C charging interface within the vehicle dashboard system.

The USB Type-C connector near the display allowed convenient mobile charging while driving. Integrating the charging circuit into the TFT minimised separate hardware needs and supported compact system design.

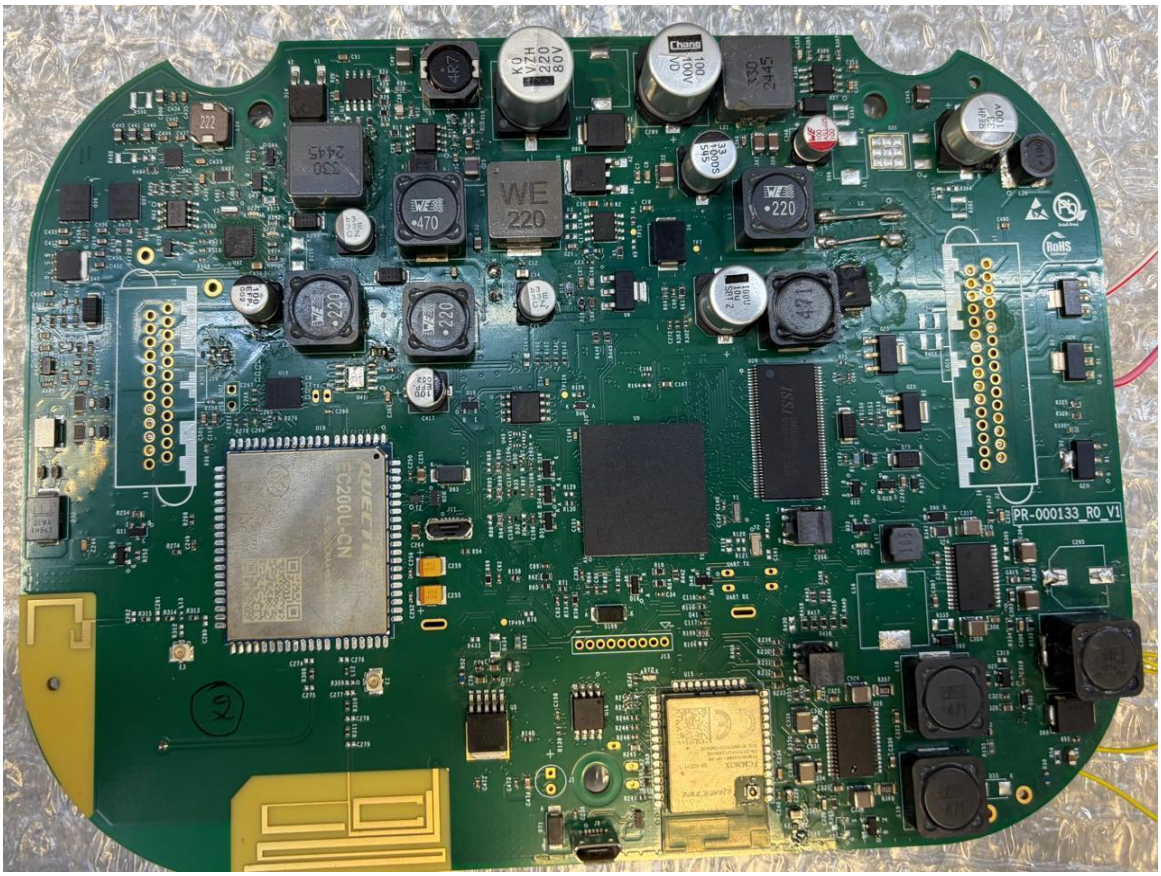

Figure 3.9: 5-Inch TFT Display Control Board with Injoinic IC

3.3 MPS Evaluation Board Architecture

The MPQ4241, developed by Monolithic Power Systems (MPS), is a comprehensive USB Type-C Power Delivery solution designed for automotive and high-power charging applications. It combines a synchronous buck converter, a USB PD 3.1 controller, integrated power MOSFETs, protocol detection circuitry, and protection features in a compact QFN 21 package.

Figures 3.10 and 3.11 display the front and rear sides of the MPS. The device operates within an input voltage range of 4.5V to 24V, with a tolerance up to 36V, and provides output voltage settings from 3.3V to 21V, capable of delivering up to 65W of power.

The evaluation for this thesis used the EVQ4241LE00A board from MPS, which includes the MPQ4241GLE0001AEC1 IC, passive components, EMI filtering, USB Type-C, and I2C support.

Figure 3.10: Front side of MPS Evaluation Board

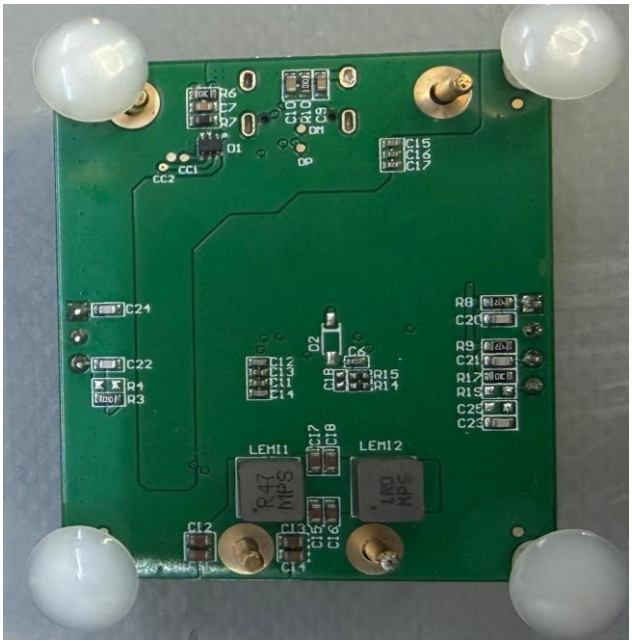

Figure 3.11: Rear side of MPS Evaluation Board

3.3.1 MPS Internal Architecture

The MPS is a compact USB Type-C Power Delivery controller for high-efficiency fast charging in automotive and industrial systems, combining a buck converter, communication controller, gate drivers, protection, and protocol functions.

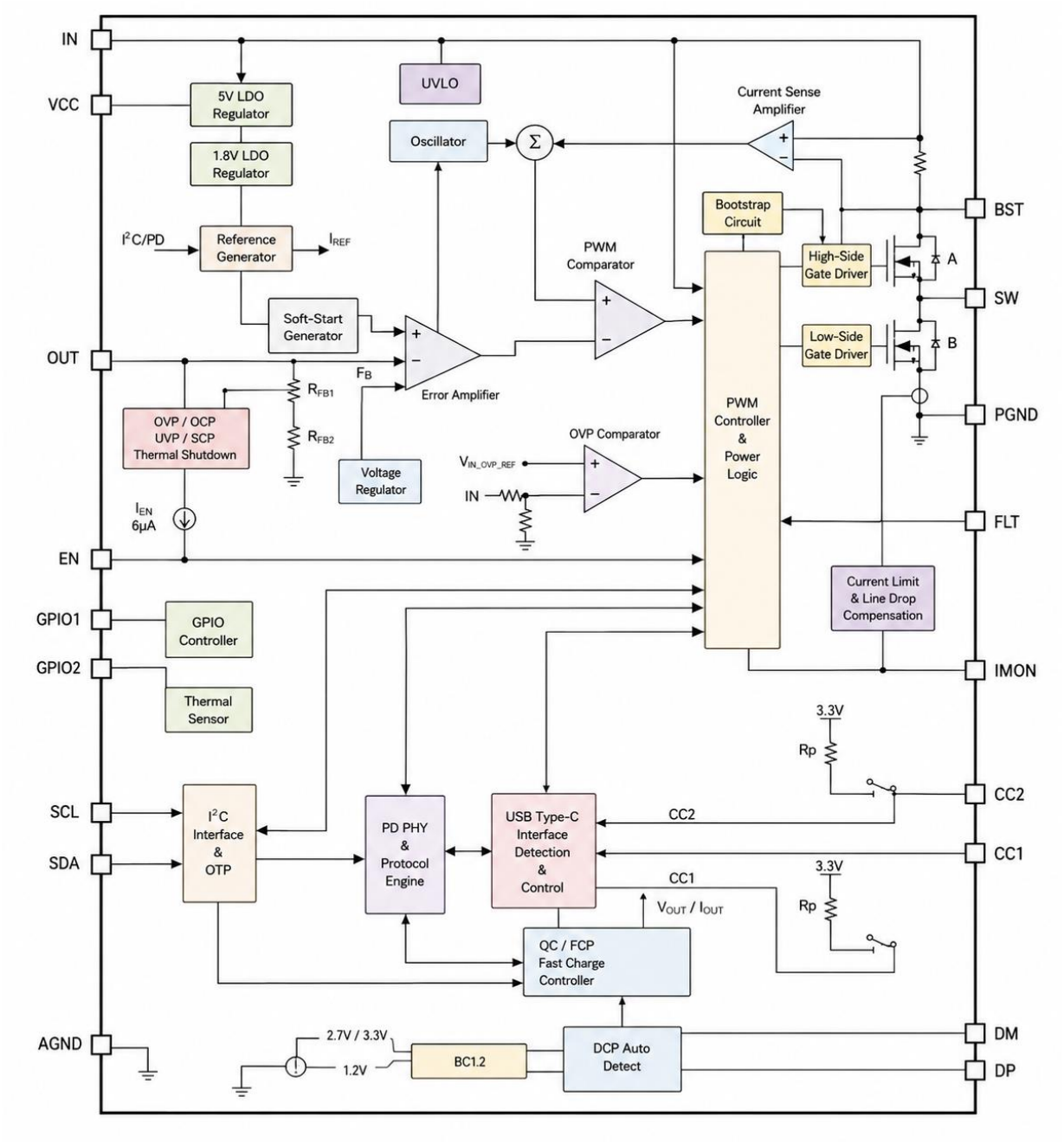

Figure 3.12: Internal Functional Architecture of MPS Evaluation Board

The controller supports wide input voltage operation and programmable USB PD output profiles for Type-C charging applications.

The internal power stage uses a synchronous buck converter with integrated high- and low-side MOSFETS. The IN pins supply voltage to the converter and control circuits.

The SW node connects to an external inductor for energy transfer and regulation. A bootstrap capacitor on the BST pin enables high-side gate drive. Figure 3.12 shows the MPS evaluation board's internal architecture.

Output voltage regulation is controlled by the internal feedback and PWM circuitry according to the negotiated USB PD profile and load conditions. The integrated low RDS(ON) MOSFET structure helps reduce switching and conduction losses during high-current operation.

The MPQ4241's communication section features CC1 and CC2 interfaces for USB Type-C attachment detection and USB PD signaling. It also includes DP and DM interfaces to support legacy charging protocols like QC, BC1.2, and FCP. Additionally, the controller supports I2C communication via SDA and SCL pins, enabling configuration of parameters such as PDO profiles, protection settings, switching frequency, and line compensation.

Additional GPIO features are included for external monitoring and control, such as thermal sensing, fault indication, and LED operation.

3.3.2 Functional Description of MPS

During startup, the MPQ4241 is powered via the VIN pins, which activate its internal regulation circuitry necessary for the converter and protocol functions. Once the EN pin is enabled, the controller checks the CC1 and CC2 lines to determine cable orientation and sink attachment through the USB Type-C interface.

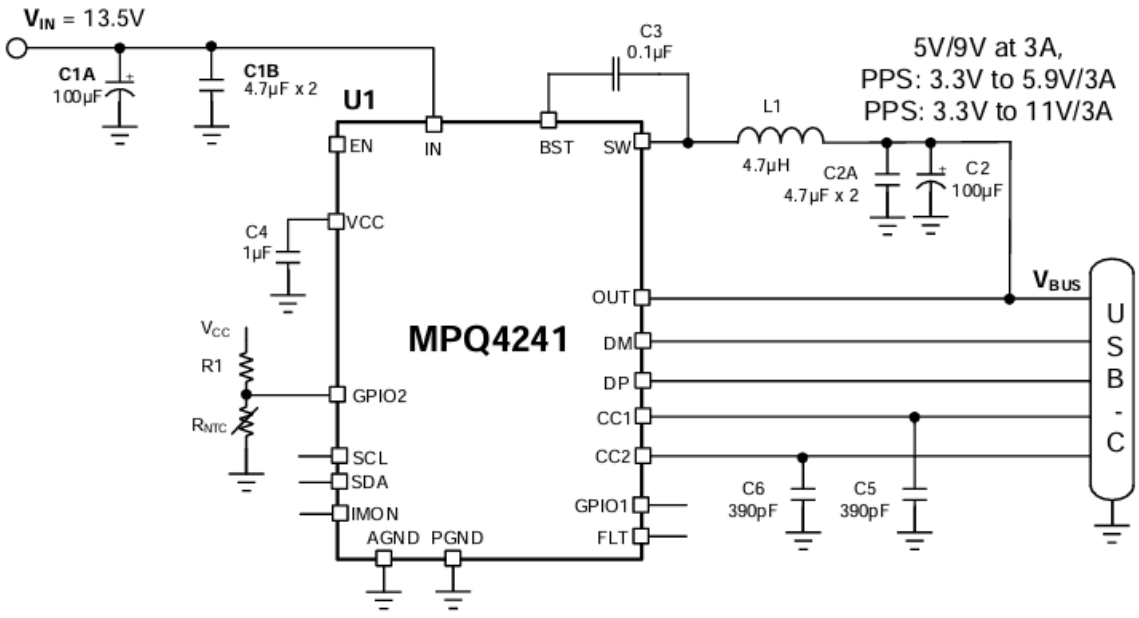

Figure 3.13: Application Circuit of MPQ4241 USB PD Controller

Once a valid connection is established, the controller begins USB PD communication and broadcasts supported PDO profiles to the connected device. The output voltage is then

adjusted based on the negotiated charging profile. Figure 3.13 displays the application circuit of the MPS USB PD controller IC.

The internal synchronous buck converter features integrated high-side and low-side MOSFET switches for VBUS power conversion. The SW node is linked to an external inductor and an output filter stage to produce a regulated voltage. Users can configure switching frequency and operating parameters via the I2C interface based on their specific needs.

The controller also includes power management and thermal protection features that operate under different input and temperature conditions. It automatically reduces output power during low input voltage or high temperature situations to ensure stable and safe operation.

3.3.3 Power Stage Architecture

The MPS employs a synchronous buck converter design for USB PD power conversion. Its power stage features integrated high-side and low-side MOSFETs, complemented by external passive components such as the bootstrap capacitor, output inductor, and output filter capacitors, as shown in Figure 3.14. The IN pins receive power from an automotive source, while the SW node connects to an external 4.7 µH inductor for output regulation.

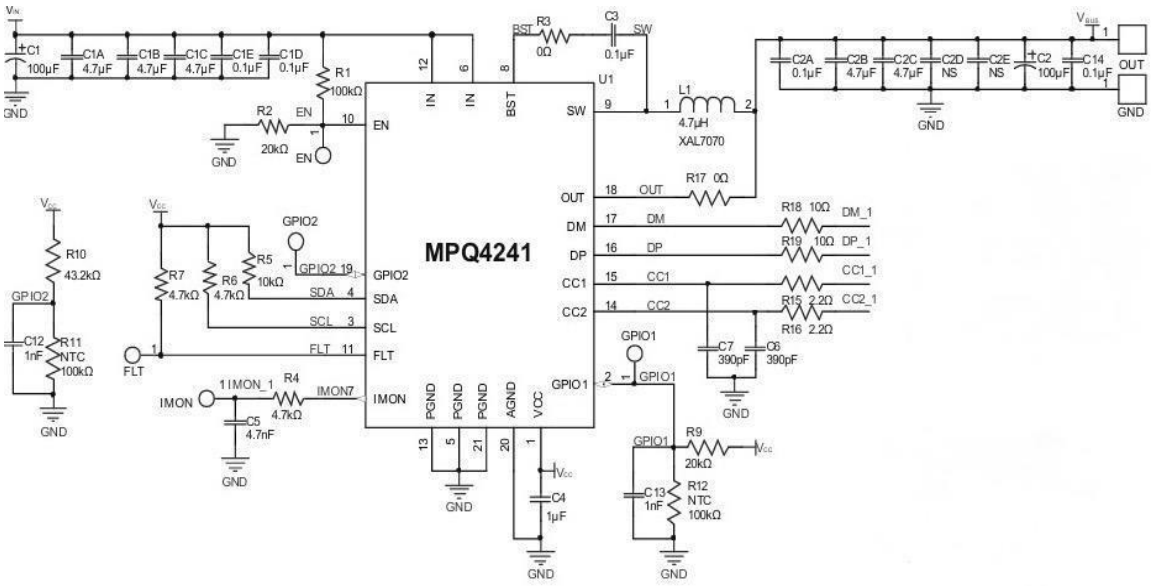

Figure 3.14: Schematic of MPQ4241

The converter can output programmable USB PD profiles ranging from 3.3V to 21V, depending on the negotiated charging conditions. It achieves high efficiency through synchronous rectification and an integrated MOSFET switching architecture.

3.3.4 USB PD Protocol Support

The MPQ4241 supports USB PD 3.1 with PPS and legacy protocols, offering fixed PDO profiles and adjustable voltage. The default board configuration includes 5V/3A, 9V/3A, and PPS options from 3.3V–12V/3A, as shown in Table 3.1.

The controller provides VCONN power for electronically marked cable functions. The DP and DM communication lines are compatible with BC1.2, QC3.0/QC4+, Apple Divider Mode, and Huawei FCP charging protocols, ensuring they work with legacy charging devices.

Table 3.1: MPS PDO Profiles

Mode	Voltage Range	Current
Fixed PDO	5V	3A
Fixed PDO	9V	3A
PPS APDO	3.3V–5.9V	3A
PPS APDO	3.3V–12V	3A

3.3.5 Virtual Bench Pro Configuration

The MPQ4241 evaluation board was configured and observed using Monolithic Power Systems' Virtual Bench Pro software. It communicated with the host PC through the USB to I2C interface on the MPS Evaluation Board, allowing direct access to the internal registers of the MPQ4241 IC controller.

The software interface was used to set USB PD voltage profiles, PPS configurations, switching frequencies, protection thresholds, and current limit parameters during testing. PDO profiles were configured via the graphical interface to meet testing requirements, as shown in figure 3.15, which illustrates the Virtual Bench Pro interface used for MPS configuration.

Virtual Bench Pro monitored output voltage, current, protocol status, faults, and thermal parameters during converter operation. Alongside the electronic DC load and PD analyzer, it examined the converter's behavior under different load conditions.

The GUI interface enabled monitoring of protection events such as over-current operation, thermal derating, and low VIN behavior. During testing, stable I2C communication relied on correct interface connections and proper initialization of the MPQ4241 digital control registers.

The software configuration approach simplified testing of various charging profiles without requiring any changes to the hardware on the evaluation board.

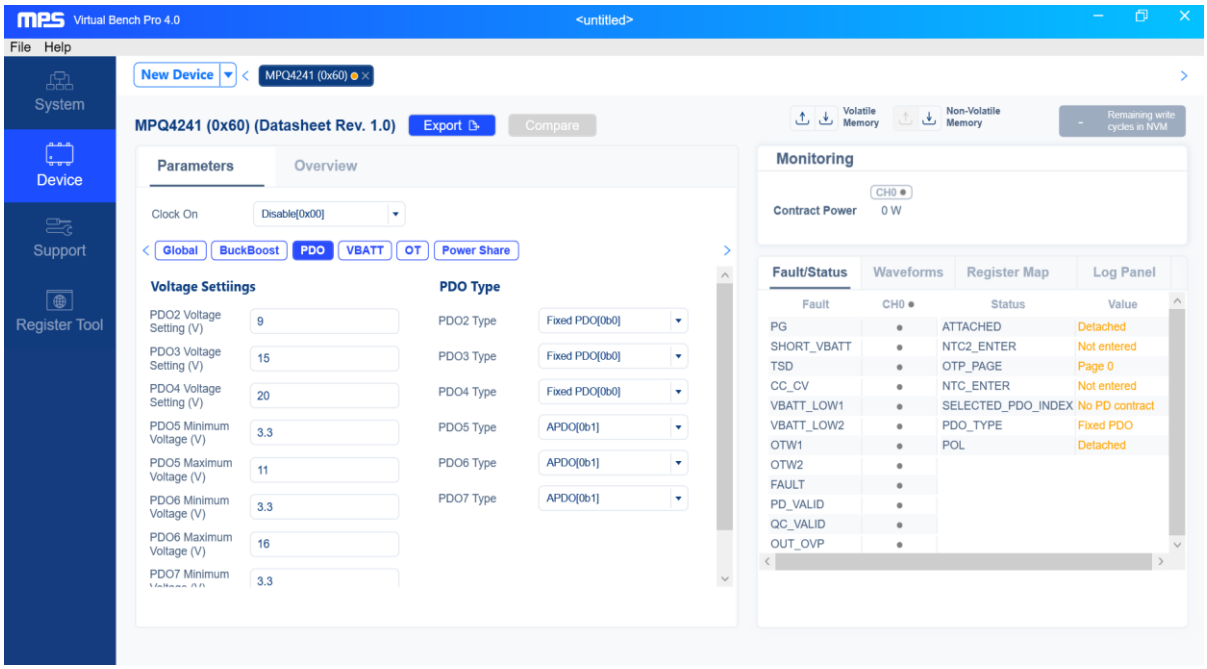

Figure 3.15: Virtual Bench Pro Interface Used for MPS Configuration

3.3.6 Protection Features

The MPQ4241 includes diverse protections such as UVLO, OVP, overcurrent, thermal shutdown, and short-circuit protection to ensure safe operation during electrical and thermal issues.

The datasheet states the VIN UVLO rises at about 4.1V with 300mV hysteresis; VIN over-voltage protection activates near 26.2V. Output over-voltage protection triggers when VBUS exceeds 117% of the set voltage, with an absolute OVP near 23.5V. The converter's peak current limit is 12A, and the valley limit is 11.2A.

Thermal shutdown occurs at approximately 170 °C with a 20 °C hysteresis. During overload or a short circuit, the converter enters hiccup mode, which involves repeatedly disabling and restarting the switching until the fault is resolved.

The FLT pin pulls low during faults to enable external monitoring. Additionally, the IC offers DP/DM/CC line-overvoltage protection up to 14 V, enhancing the interface's reliability.

3.4 Renesas Board Architecture

3.4.1 RAA489300 Evaluation board

The Renesas evaluation board is tailored for high power USB PD applications that demand high conversion efficiency and steady performance over a broad input voltage range. It employs a 3-level synchronous buck architecture, which minimizes switching losses and reduces voltage stress on the power MOSFETs during high-power operation.\ [13], [26].

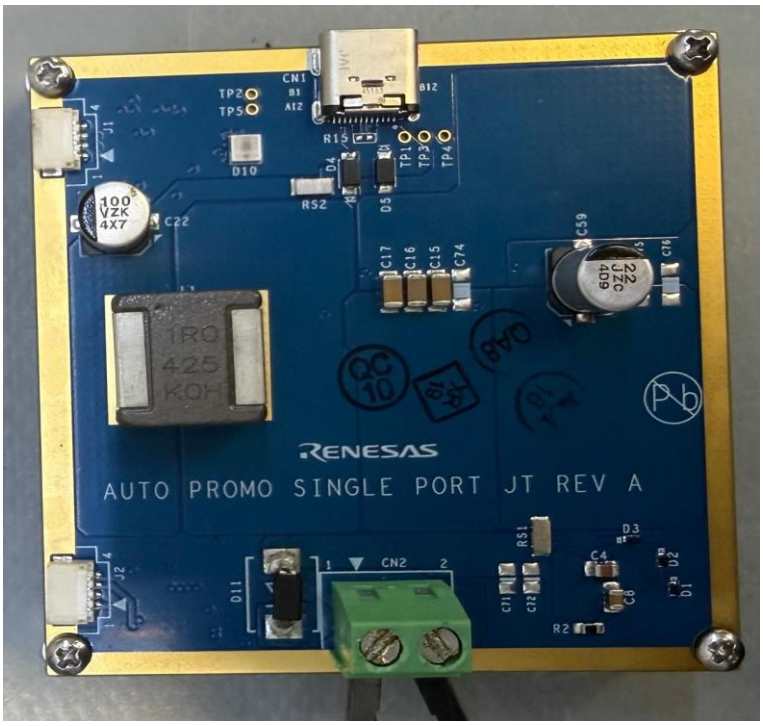

Figure 3.16: Front view of Renesas Evaluation Board

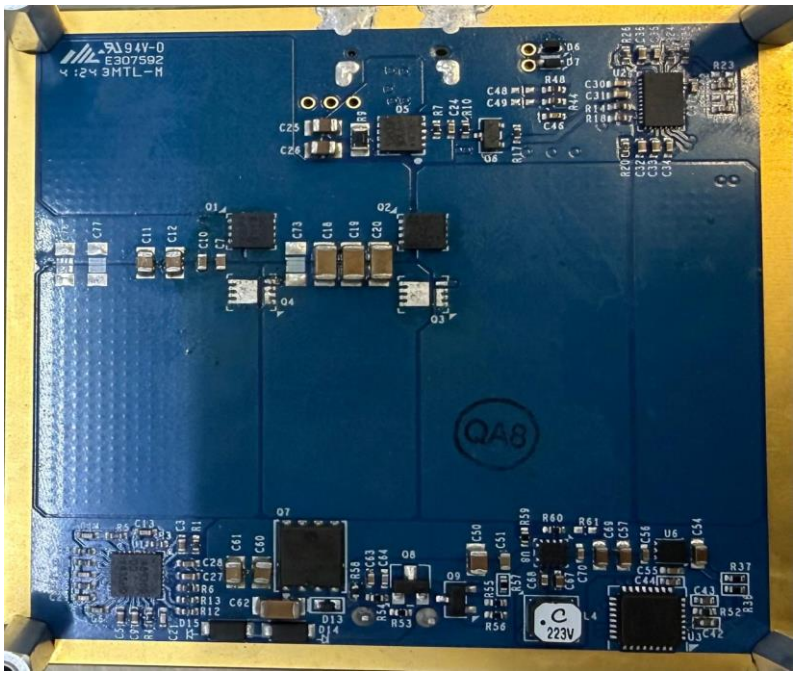

Figure 3.17: Rear view of Renesas Evaluation Board

The evaluation board comprises the RAA489300 controller, external MOSFET switches, output inductor, current-sensing circuitry, and USB Type-C interface for USB PD. The controller supports programmable output voltage and SMBus/I2C communication for configuration and monitoring.

The 3-level switching architecture enhances efficiency during high current operation and enables smooth transitions between CCM and DCM modes based on load. Protection and monitoring features ensure reliable operation during USB PD power delivery.

3.4.2 3-Level Buck Converter Architecture

The Renesas Board uses a 3-level buck converter for high-power USB PD up to 140W. Unlike a 2-level converter, it reduces voltage stress on MOSFETs by using a flying-capacitor topology, cutting switching losses and boosting efficiency at high frequency [14].

The microcontroller controls MOSFETs via gate-driver circuitry. When the USB is attached, it signals the IC to open the circuit and pass power from the IC to the USB-C. Its flying capacitor network ensures stable voltage at switching nodes. The architecture supports lower inductance and improved switching behavior at the output [27].

The evaluation board works on 48V automotive batteries and delivers USB PD outputs up to 28V/5A. It switches MOSFETs based on the duty cycle to achieve higher efficiency at high voltages. With over 98% efficiency at high loads, it reduces thermal stress, ideal for high-power automotive charging.

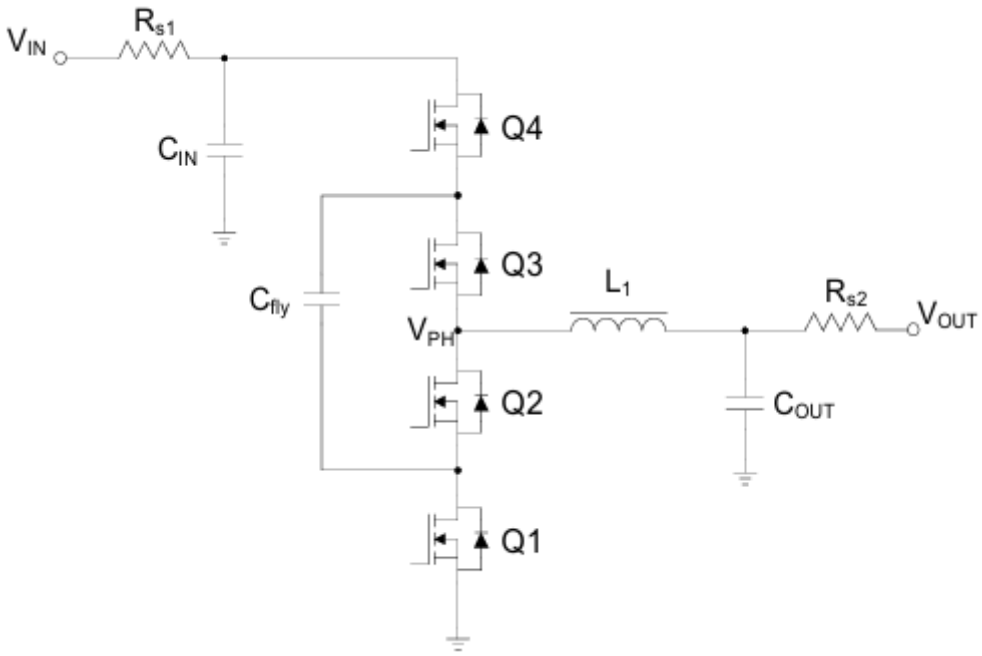

Figure 3.18: 3-Level Buck Converter Topology

3.4.3 Renesas Board USB Type-C Port Controller

The RAA489400 functions as the USB Type-C Port Controller within the Renesas USB PD . The controller is responsible for USB Type-C attachment detection, CC

communication, VCONN management, and USB PD protocol handling during charging. The device supports USB PD 3.1 communication and Extended Power Range operation for high-power USB Type-C applications.

Figure 3.19 shows the Renesas board's internal architecture, including VBUS monitoring, Fast Role Swap and dead battery support.

The RAA489400 also integrates protection functions for VBUS, CC lines, and VCONN operation to improve reliability during USB PD operation.

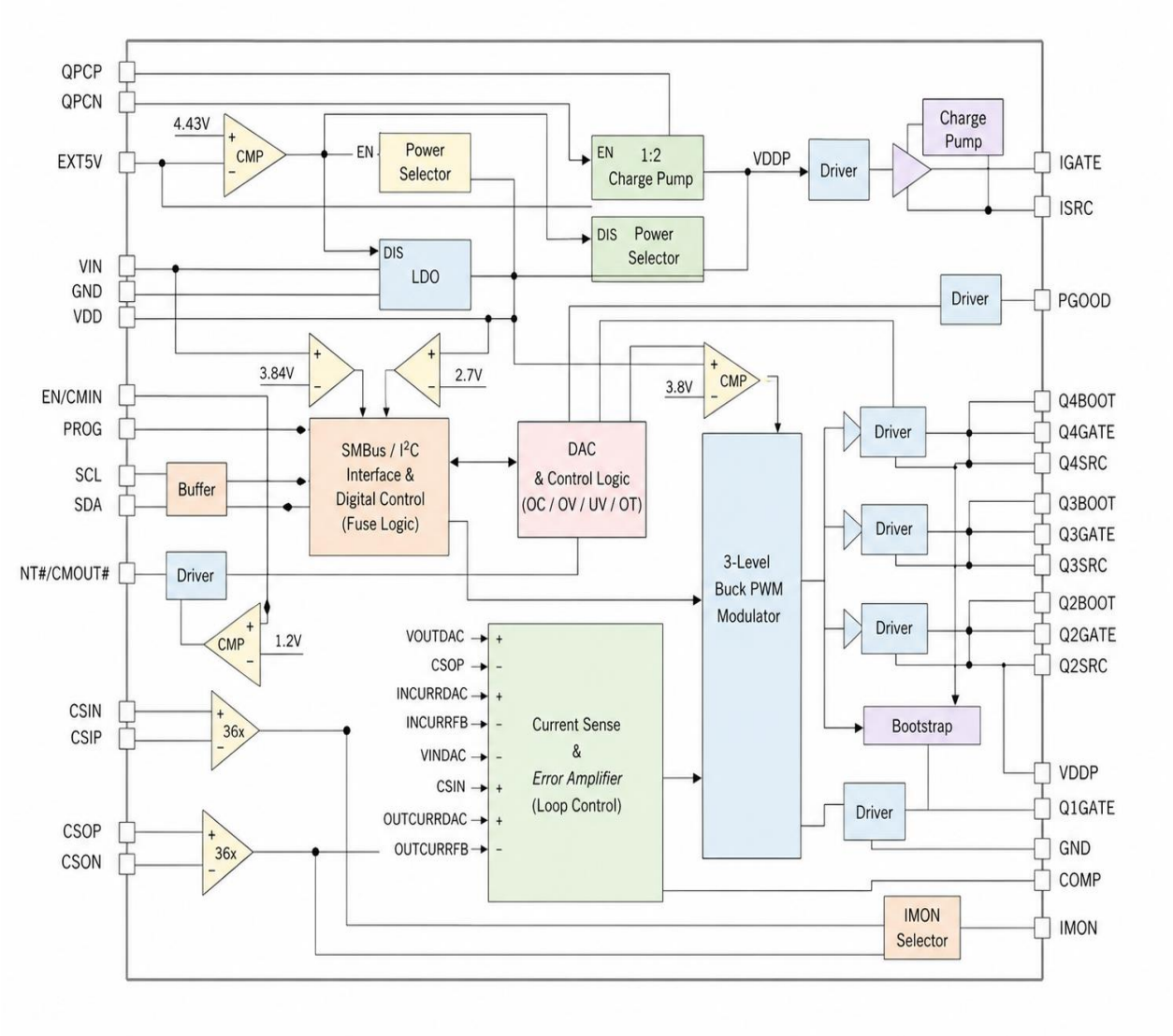

Figure 3.19: Renesas Board Internal Functional Architecture

3.5 Comparative Hardware Analysis of Selected Charger ICs

The evaluated USB PD charging s utilize different power conversion architectures and protocol management approaches depending on target power level and automotive application requirement. Table 3.2 summarizes the major hardware characteristics and electrical specifications of the selected charger s

Table 3.2: Hardware Comparison of Selected USB PD Charger ICs

Parameter	Injoinic IC	MPS Board	Renesas Board
Converter Topology	Synchronous Buck	Synchronous Buck	3-Level Buck
Input Voltage Range	7.3V – 29.5V	4.5V – 24V	4.5V – 57.6V
Max Input Voltage	36V	36V	60V
Output Voltage Range	3V – 12V	3.3V – 21V	3V – 54.9V
Max Output Power	36W	65W	140W
Max PDO Profile	9V/3A	20V/3.25A	28V/5A
USB PD Version	PD2.0 / PD3.1	PD3.1	PD3.1 EPR
PPS Support	Yes	Yes	Yes
PPS Voltage Range	3V – 11V	3.3V – 11V	Up to 48V
PPS Resolution	20mV	20mV	Software Configurable
Supported Charging Protocols	QC2.0, QC3.0, AFC, FCP, SCP, BC1.2	QC4+, BC1.2, Apple Divider, FCP	USB PD 3.1 EPR
MOSFET Configuration	Integrated	Integrated	External MOSFET Stage
High-Side MOSFET RDS(ON)	Internal	30mΩ	External
Low-Side MOSFET RDS(ON)	Internal	18mΩ	External
Switching Frequency	Internal PWM Control	250kHz / 420kHz / 2.2MHz	Up to 400kHz
Peak Efficiency	93.27%	98.22%	Approximately 98%
Thermal Derating	Internal OTP	Starts at 130°C	Programmable
Thermal Shutdown	Internal OTP	170°C	Supported
Target Application	Compact Automotive USB Charging	Mid Power Fast Charging	High Power Automotive Charging

3.6 Conclusion

This chapter delineated the hardware design and implementation of the selected automotive USB PD charging s. The Injoinic IC charger was successfully integrated onto the TFT display board with appropriate filtering, protection, and USB Type-C communication circuitry. Practical observations indicated that PCB routing, grounding, and passive component placement significantly influenced switching stability and output ripple.

The MPS MPQ4241 offered enhanced configurability and support for advanced USB PD features, including PPS operation and programmable PDO profiles. The Renesas board exhibited support for higher power USB PD operation through its three-level buck converter architecture.

Overall, the chapter emphasized that the actual performance of the converter is contingent not only upon the datasheet specifications but also on the quality of hardware implementation and component selection.

CHAPTER 4 - EXPERIMENTAL ANALYSIS

4.1 Experimental Test Setup

The experimental setup utilised for the performance assessment of the USB Type-C Power Delivery s is depicted in Figure 4.1. Testing was conducted employing a programmable DC power supply, a PD sink module, and an electronic DC load to evaluate efficiency, load regulation, and protection behavior under various operating conditions. The input power was supplied via the DC power supply, whereas the output load current was regulated using the electronic load.

During MPS evaluation testing, the board was connected directly to the PD sink module via USB Type-C. When using the Injoinic IC on the 5-inch TFT board, a custom converter PCB was used between the TFT and the PD sink to enable USB-C conversion and signal routing.

Different PDO voltage profiles and load currents were tested, with output monitored via oscilloscopes and lab instruments. Figure 4.1 depicts the USB PD performance hardware setup.

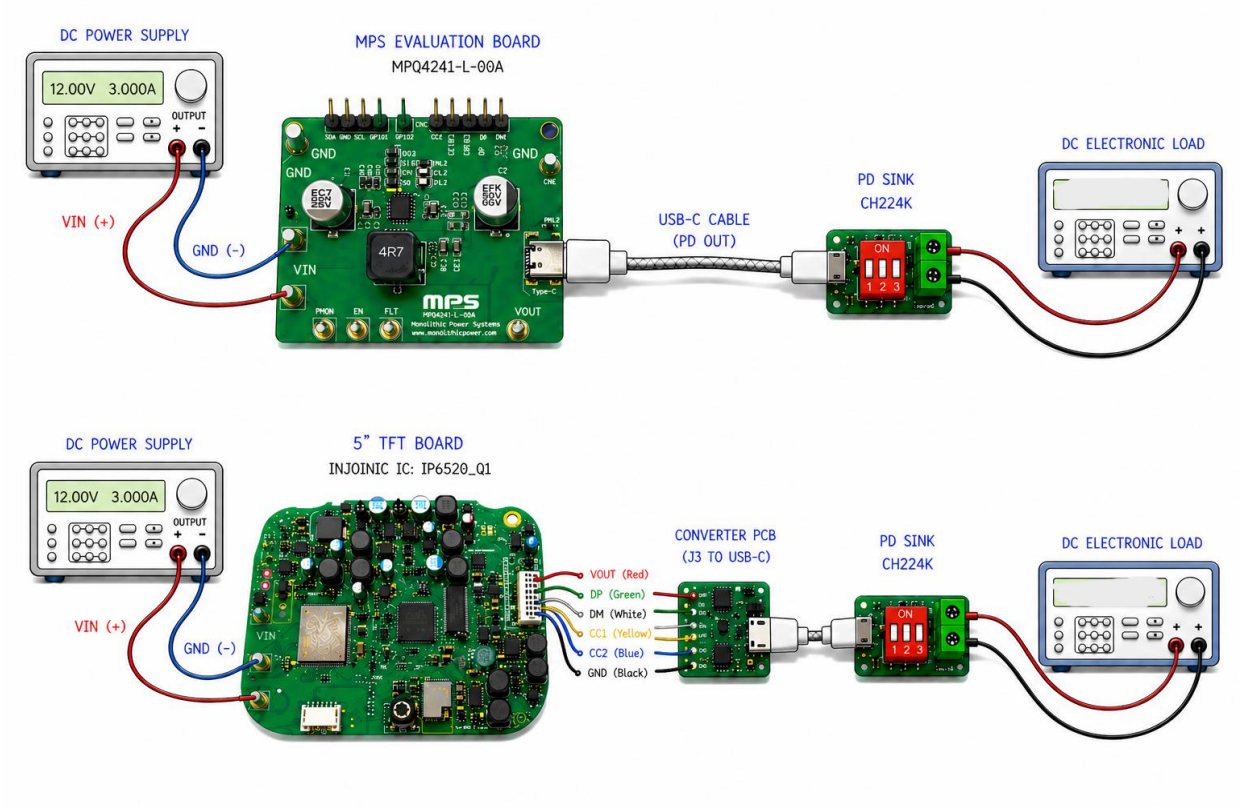

Figure 4.1: Hardware Setup for USB PD Performance Evaluation

4.1.1 Overall Hardware Test Bench

The experimental validation of the selected USB Type-C Power Delivery charger ICs used a hardware test bench with a programmable DC power supply, electronic load, oscilloscope, multimeter, USB PD sink trigger board, and Charger LAB protocol analyzer. The setup evaluated efficiency, load regulation, voltage negotiation, protocol compatibility, and protection performance under various conditions.

The programmable DC power supply was used to emulate various automotive battery voltages during converter testing. The input voltage ranged from 7.3v to 48v, depending on the charger architecture, to analyze converter behavior under low, nominal, and high voltage conditions. An electronic DC load in constant current mode evaluated load regulation and efficiency at different loads.

The CH224K USB PD sink trigger board was employed to request various USB PD voltage profiles from the charger under evaluation. By configuring the sink selection pins, fixed PDO profiles ranging from 5V to 20v, including 9V, 12V, and 15V, were selected during testing.

The Charger LAB KM003C analyzer was interfaced between the charger output and the sink device to monitor the USB PD protocol negotiation, output voltage, current, power delivery status, and permissible charging protocols.

Oscilloscope measurements were performed during protection testing and transient analysis for observing converter startup behavior, output voltage recovery, hiccup operation, and protection triggering response.

4.1.2 USB PD Sink Trigger Board Configuration

The CH224K USB PD sink trigger module shown in FIGURE 4.2 and 4.3 was used in experiments to request different USB Power Delivery voltage profiles from the charger under test. It functions as a USB PD sink device, communicating with the charger via the CC lines of the USB Type-C interface.

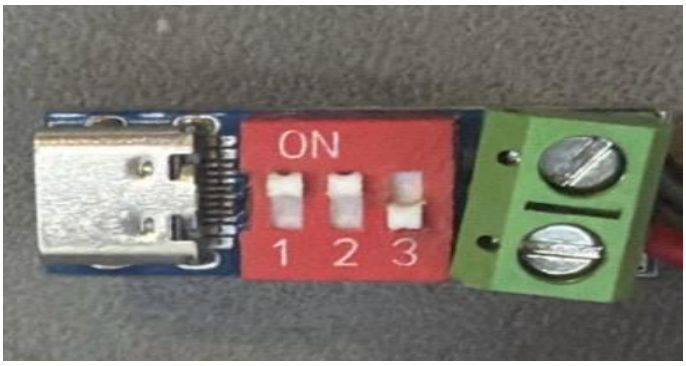

Figure 4.2: Front view of USB PD sink trigger module

Figure 4.3: Rear view of USB PD sink trigger module

The implemented CH224K sink board included DIP switch based voltage selection for requesting different PDO profiles including 5V, 9V, 12V, 15V, and 20V according to the configuration truth table shown in Table 4.1. During testing, the required voltage profile was selected manually through the DIP switch configuration before connecting the module output to the electronic DC load.

After successful USB PD negotiation, the selected output voltage became available at the output terminals of the module. The output was connected directly to the electronic DC load operating in constant current mode for load testing, efficiency measurement, and protection validation of the USB PD charger s.

The CH224K module was extensively used during testing of the INJOINIC IC, MPQ4241, and Renesas RAA489300 IC for verifying PDO negotiation, output stability, and USB PD communication behavior under different load conditions.

Table 4.1: CH224K PD Trigger Voltage Selection Table

SW3	SW2	SW1	Output Voltage
1	X	X	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

4.1.3 Charger LAB Protocol Analyzer Setup

The Charger LAB KM003C USB PD analyzer was used during experimental validation for monitoring USB Power Delivery negotiation, output voltage, output current, charging power, and protocol behavior of the charger s under test. The analyzer was connected

between the USB PD charger output and the CH224K sink trigger module in order to observe real time charging parameters during operation.

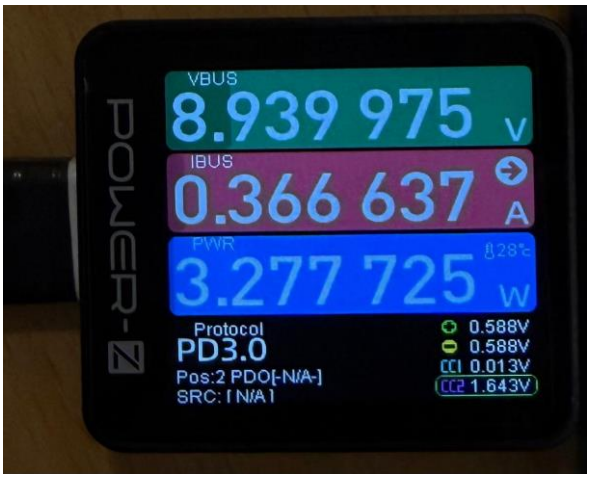

Figure 4.4: PD analyzer USB PD Output Monitoring

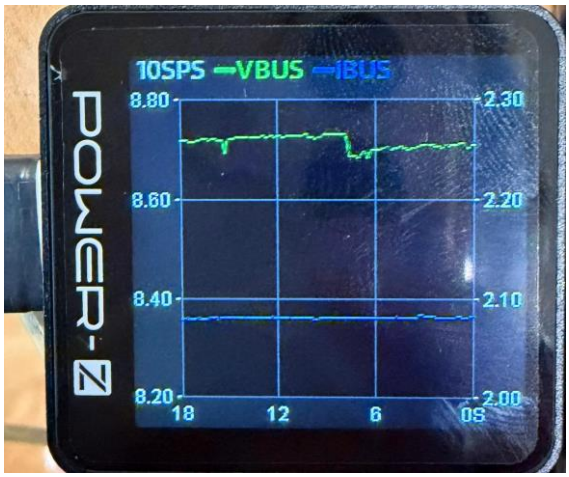

Figure 4.5: PD analyzer VBUS and IBUS Monitoring

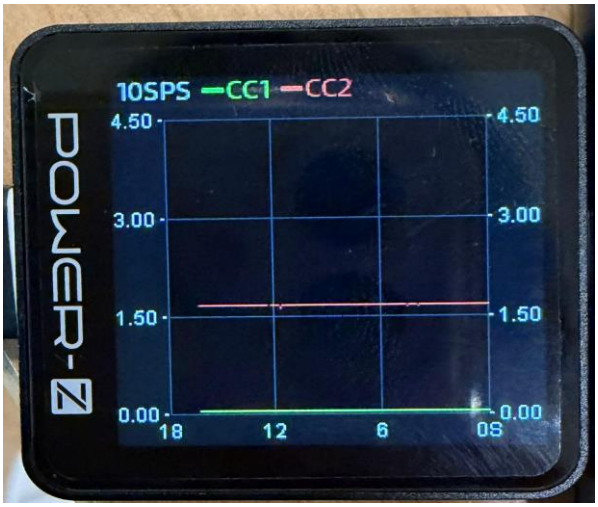

Figure 4.6: PD analyzer CC Line Monitoring

The analyzer provided monitoring of VBUS voltage, output current, output power, CC communication line voltage, negotiated PDO profile, and supported charging protocol during converter testing. During experimental evaluation, the KM003C was used for verifying successful USB PD negotiation under different operating conditions including 5V, 9V, PPS, and higher power load conditions.

The captured waveforms were used for observing voltage stability, current variation, and protocol behavior during load regulation testing.

The analyzer was also used for monitoring output behavior under different power levels during testing of the INJOINIC IC, MPQ4241, and Renesas RAA489300 charging s. Experimental observations obtained through the analyzer assisted in validation of PDO negotiation, PPS operation, and charging stability during load variation and high power testing conditions.

4.2 USB PD Voltage Profile Configuration

The INJOINIC IC based USB PD charger was validated under different USB Power Delivery voltage profiles using the CH224K sink trigger module and Charger LAB KM003C analyzer. Different PDO profiles were selected through the DIP switch configuration before USB PD negotiation.

After successful Type-C attachment detection, the charger advertised the supported PDO profiles through the CC communication line.

The negotiated output voltage was verified using the KM003C analyzer and digital multimeter before load testing. As shown in Figure 4.7 stable PPS operation was observed near 15W load condition during experimental testing. Output voltage and charging current remained stable during continuous operation..

Figure 4.7: PD analyzer PPS Output Monitoring (15W)

During lower load testing, stable PPS negotiation and output regulation were also observed, as shown in Figure 4.8. Minor variation in output current was observed due to load change conditions

Higher power testing was additionally performed near 20W operating condition. Figure 4.9 shows stable USB PD operation with proper voltage negotiation and power delivery behavior during load testing.

Experimental observations showed stable voltage regulation under different operating conditions. Higher output current during lower voltage operation increased conduction losses within the converter power stage.

Figure 4.8: PD analyzer PPS Output Monitoring (12W)

Figure 4.9: PD analyzer USB PD Monitoring (20W)

4.3 Experimental Evaluation of Injoinic IC

Experimental testing of the INJOINIC IC automotive USB PD charger was carried out under different input voltage and load conditions to evaluate converter efficiency and output regulation performance. Initial validation was performed using the 27W charger configuration, followed by testing of the upgraded 36W hardware after modification of the converter stage and passive components.

Efficiency was measured at 5V, 9V, and 12V USB PD using a programmable power supply and electronic load.

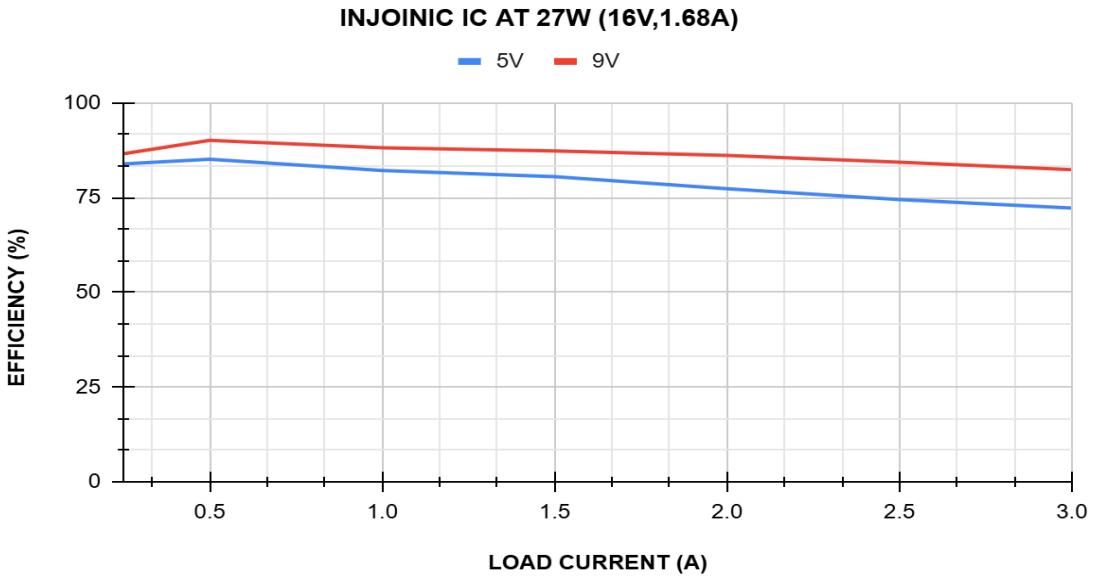

Figure 4.10: Injoinic IC Efficiency at 27 W and 16 V Vin

Efficiency variation of the 27W INJOINIC IC charger under 5V and 9V USB PD operation at vin at 16V. Maximum efficiency of 85.1% at 5V and 90.07% at 9V was observed near 0.5A load current. A gradual reduction in efficiency was observed under higher load-current conditions

Efficiency analysis was performed at Vin at 29.3V under 5V and 9V USB PD operation. Maximum efficiency of 83.6% at 5V was observed at 0.5A load current, while 9V operation achieved 85.6% efficiency at 1A load current.

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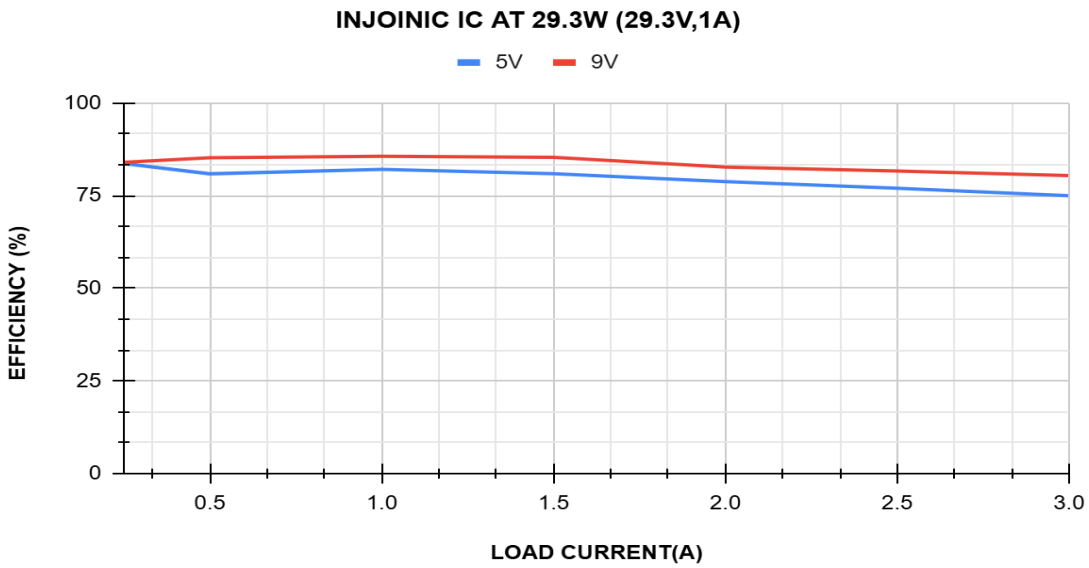

Figure 4.11: Injoinic IC Efficiency at 27W and 29.3V Vin

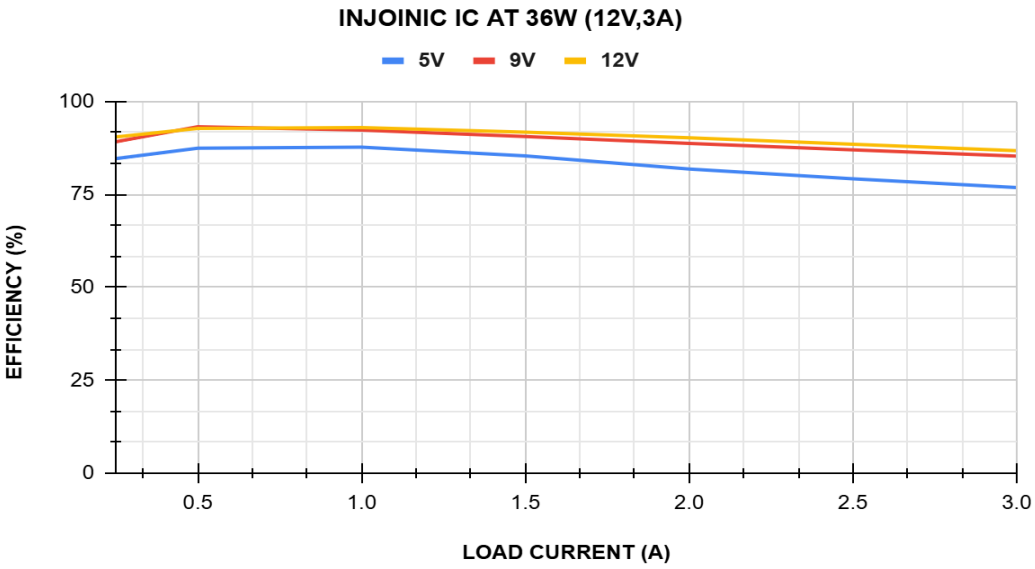

Figure 4.12: Injoinic IC Efficiency at 36W and 12V Vin

Figure 4.12 shows the efficiency performance of the upgraded 36W INJOINIC IC charger under 5V, 9V, and 12V USB PD operation at 12V vin.
Maximum efficiencies of 87.6% at 5V, 93.2% at 9V, and 92.9% at 12V were observed during experimental testing.

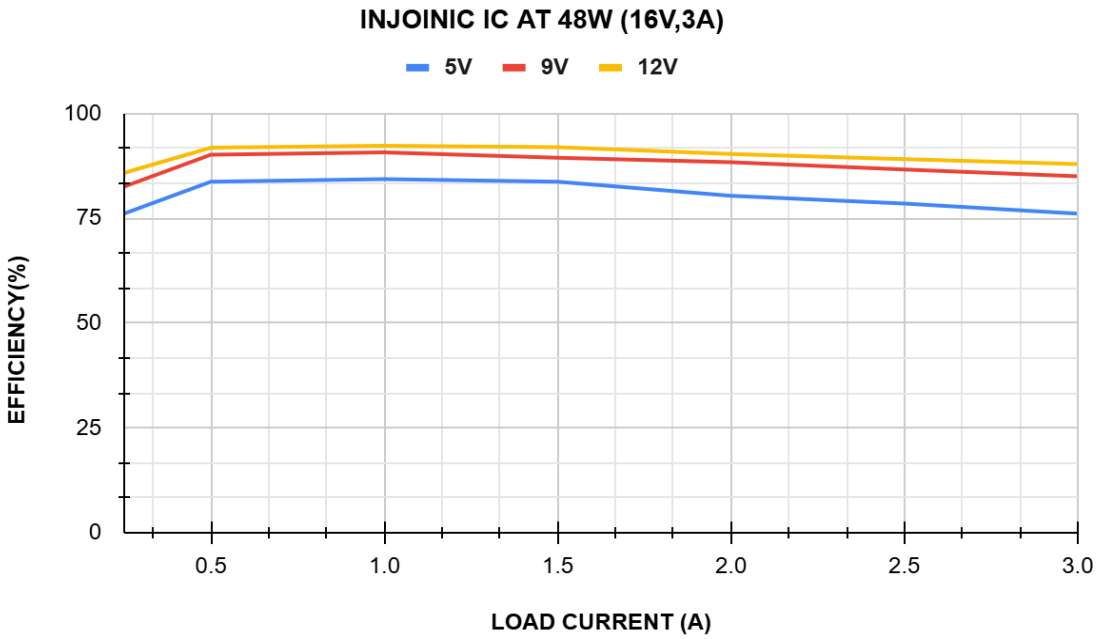

Figure 4.13: Injoinic IC Efficiency at 48W and 16V Vin

Efficiency analysis of the INJOINIC IC charger was performed at VIN = 16V and 3A under 5V, 9V, and 12V USB PD operation.
Maximum efficiency of 84.3% at 5V, 90.7% at 9V, and 92.2% at 12V was observed at 1A load current.

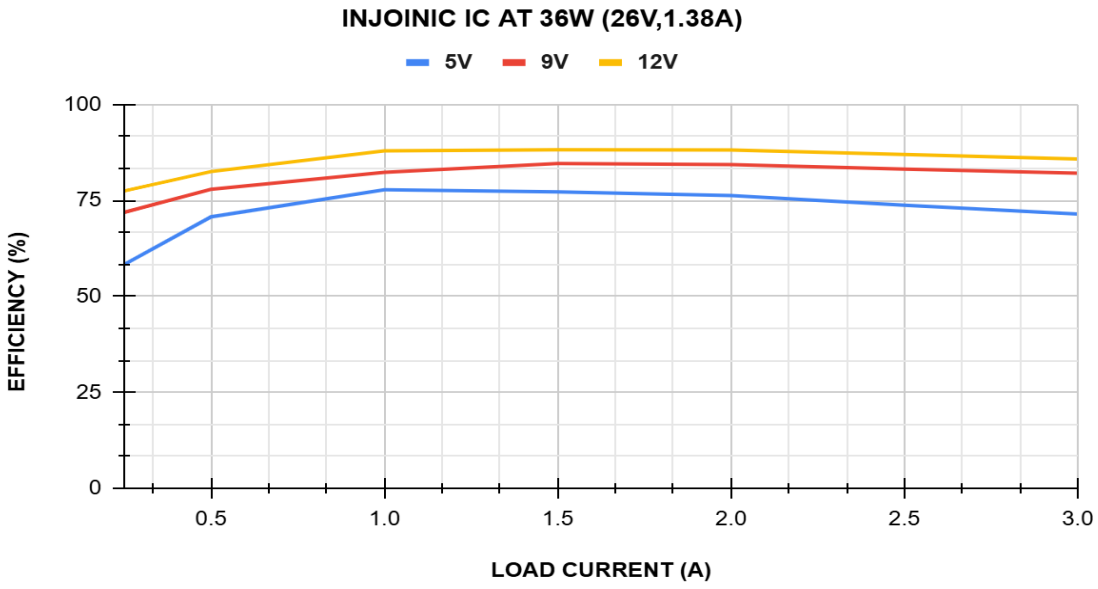

Figure 4.14: Injoinic IC Efficiency at 36W and 26V Vin

Efficiency analysis was performed at VIN at 26V and 1.38A under 5V, 9V, and 12V USB PD operation.
Maximum efficiency of 77.78% at 5V was observed at 1A load current, while 9V and 12V operation achieved 84.61% and 88.22% efficiency respectively at 1.5A load current.

4.4 Load Regulation Testing for Injoinic

Load regulation testing of the Injoinic IC charger was performed under different USB PD operating conditions by gradually increasing the electronic load current from 0.25A to 3A. Output voltage variation was monitored during 5V, 9V, and 12V USB PD operation to analyze converter stability under changing load conditions.

Figure 4.15 and Figure 4.16 show the load regulation characteristics of the initial 27W hardware configuration under 5V and 9V operation. A small reduction in output voltage was observed with increasing load current due to converter conduction and wiring losses.

After upgrading the hardware to the 36W configuration, improved output stability was observed under higher load conditions. Figure 4.17 and Figure 4.19 show stable load regulation during 5V, 9V, and 12V USB PD operation with lower voltage variation across the load range.

High-power testing was also conducted at elevated input voltage conditions. As illustrated in Figure 4.18, the converter sustained stable output voltage during 12V operation even under increased load current, thereby demonstrating enhanced load handling capability following hardware optimization.

Various combinations of inductors and capacitors were tested to enhance the efficiency and output stability of the Injoinic charger. Hardware modifications, including the use of shorter wires, parallel inductors, low DCR inductors, and supplementary output capacitors, were empirically assessed under different USB Power Delivery (PD) operating conditions.

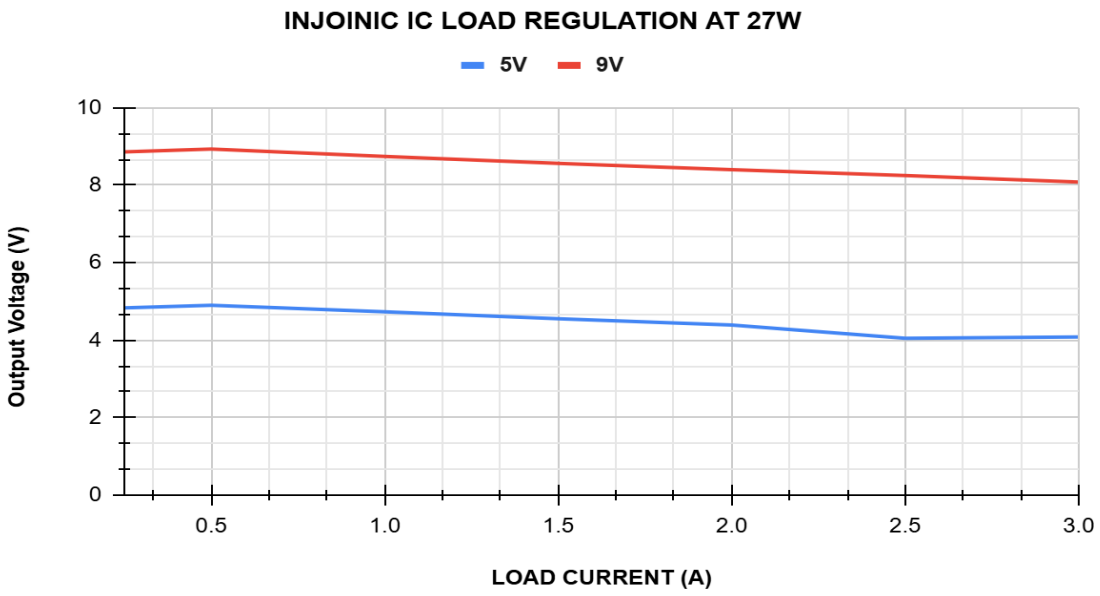

Figure 4.15: Injoinic Load Regulation at 27W

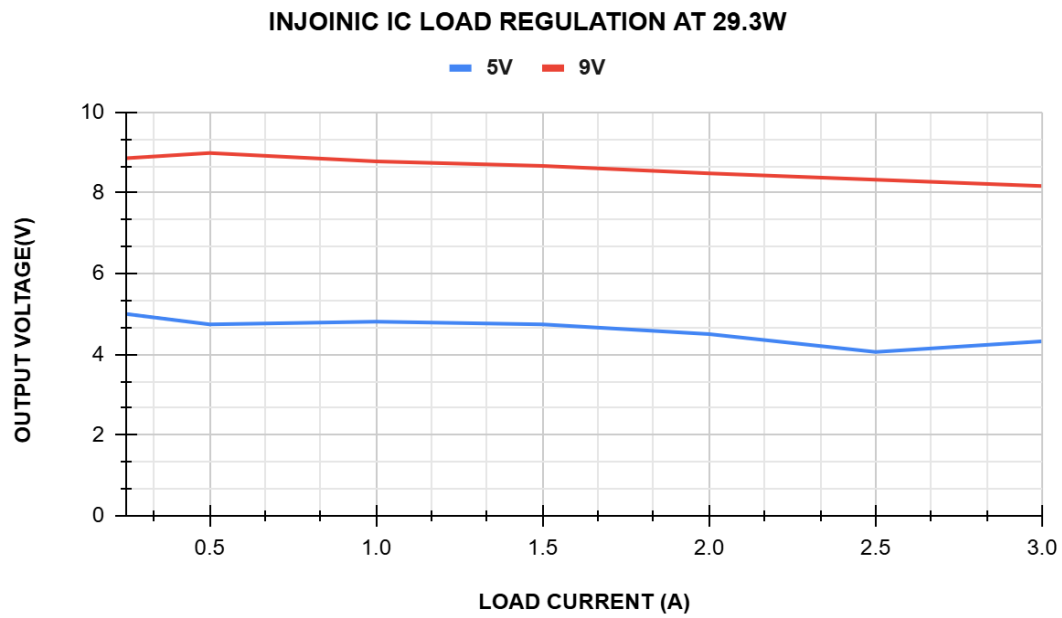

Figure 4.16: Injoinic IC Load Regulation at 29.3W

Figure 4.19 shows efficiency variation with a parallel inductor at 5V and 9V. Improved efficiency occurs at medium loads due to reduced current stress and lower conduction losses.

Further optimization used two low DCR inductors in series so that efficiency can be incresed. As shown in Figure 4.20, better efficiency and load performance occurred at higher load currents due to reduced resistive losses and improved current handling.

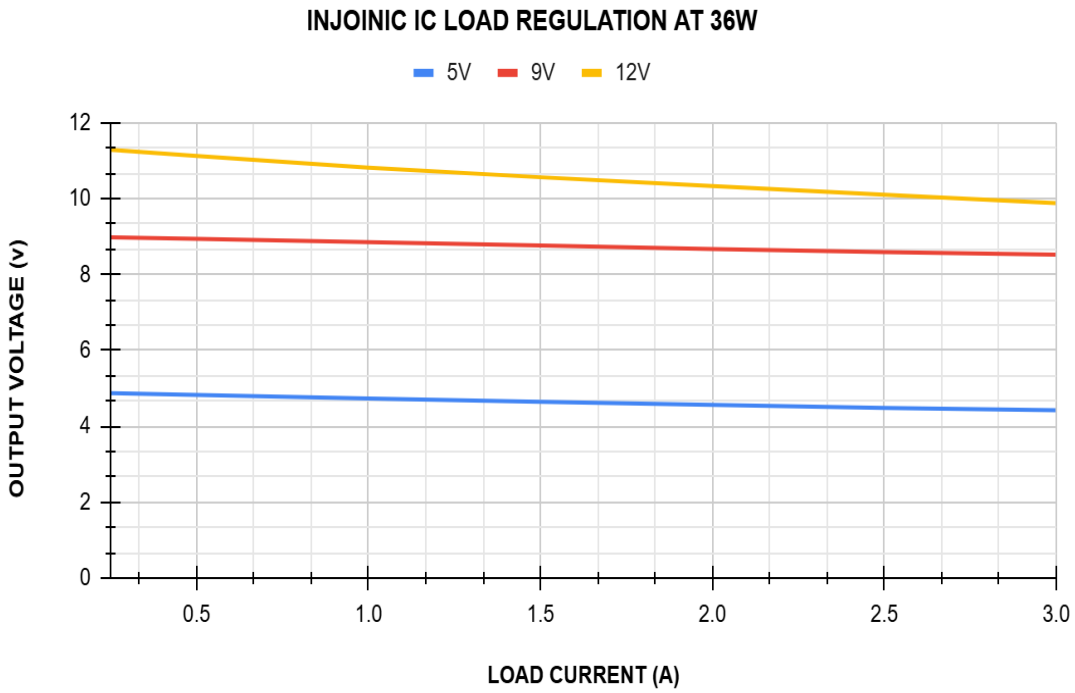

Figure 4.17: Injoinic IC Load Regulation at 36W

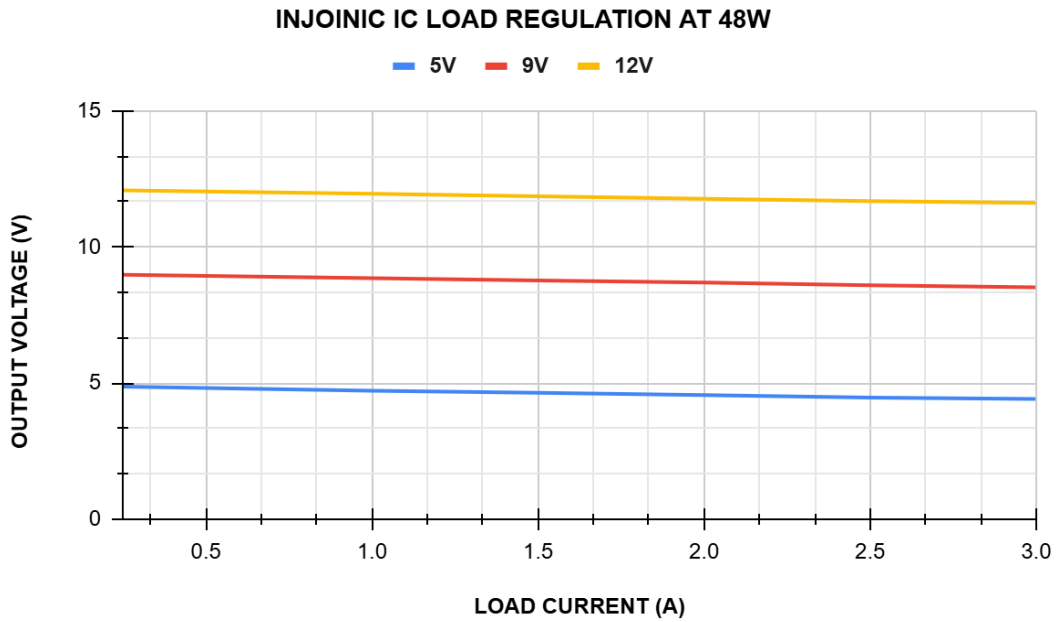

Figure 4.18: Injoinic Load Regulation at 48W

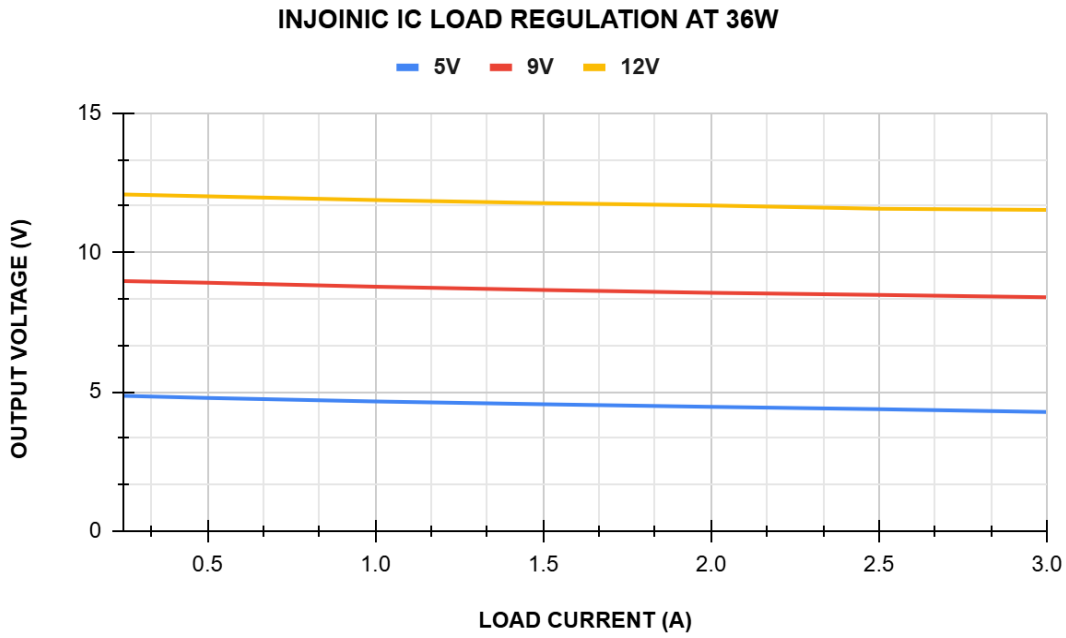

Figure 4.19: Injoinic Load Regulation at 36W (High VIN)

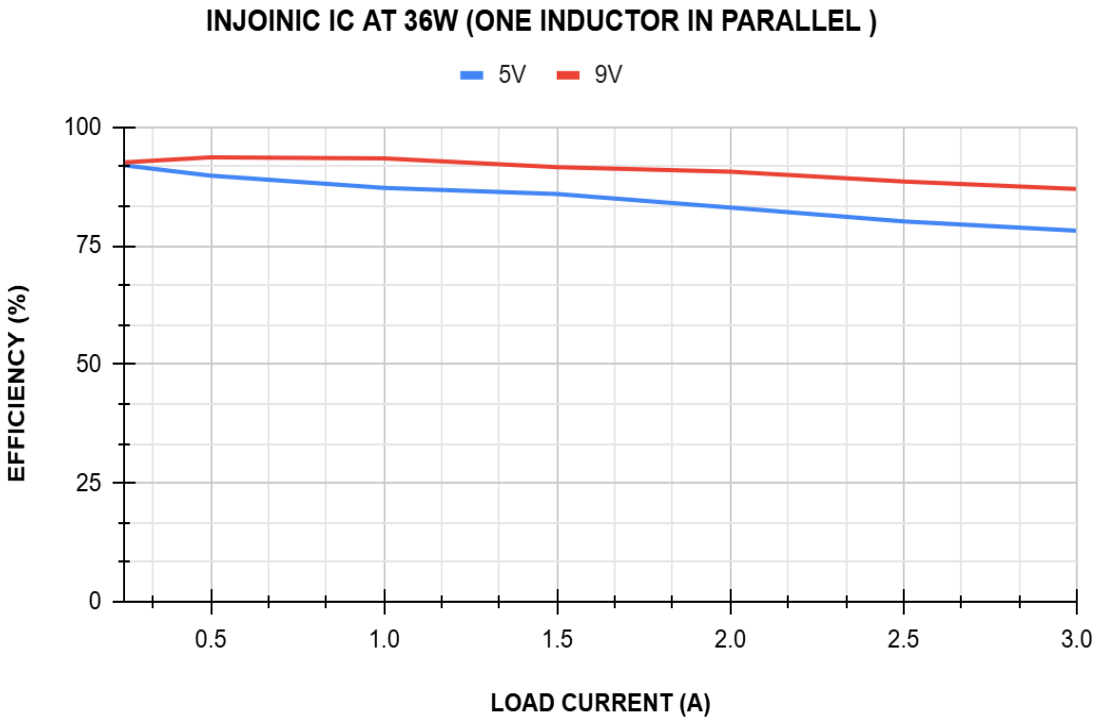

Figure 4.20: Injoinic Efficiency with Parallel Inductor Configuration

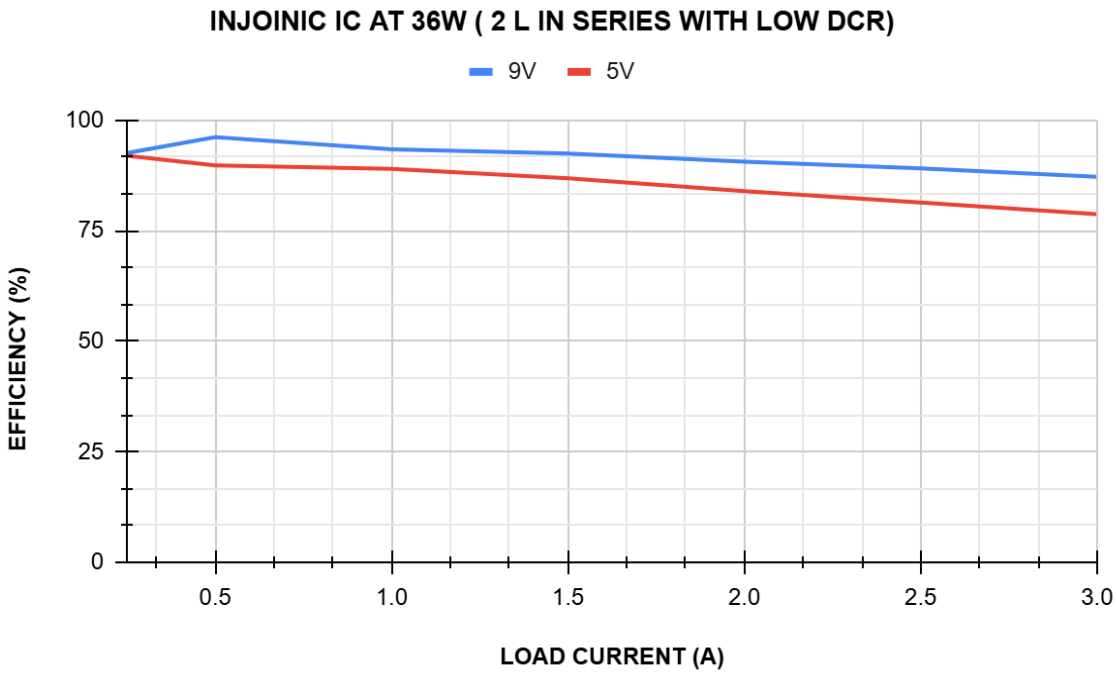

Figure 4.21: Injoinic Efficiency with Series Low DCR Inductor Configuration

4.5 Experimental Evaluation of MPS Board

Figures 5.1, 5.2, and 5.3 show the efficiency of the MPS board at 36W, 54W, and 72W. The 9V PDO profile consistently offered higher efficiency than 5V.

At 36W input (12V, 3A), the 5V profile's max efficiency was about 87.7% at 1A, while the 9V profile reached about 93.9% at 1A.

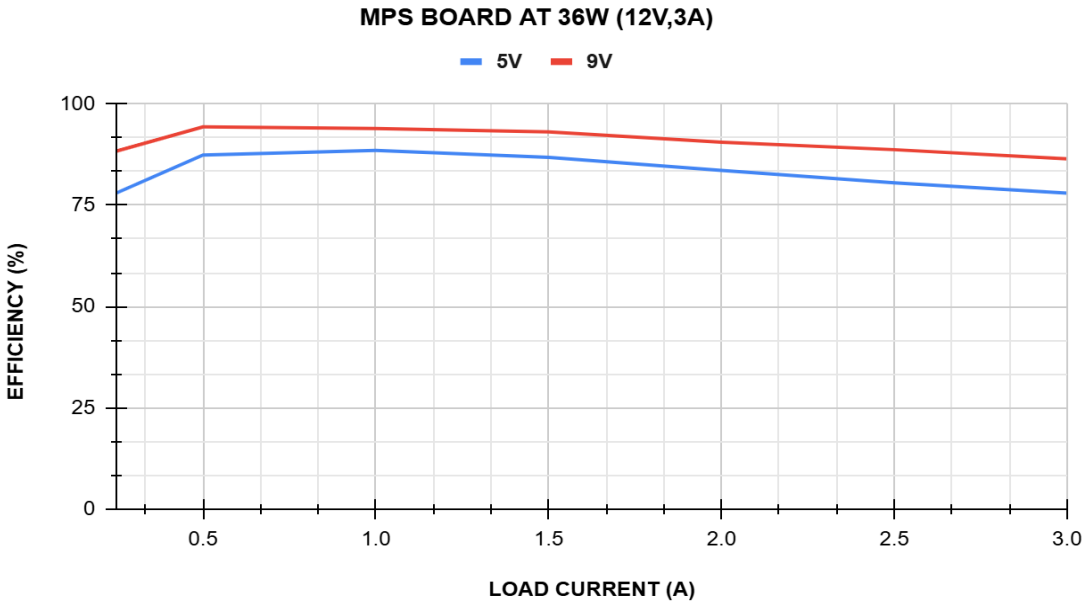

Figure 4.22: Efficiency Characteristics of MPS Board at 36W

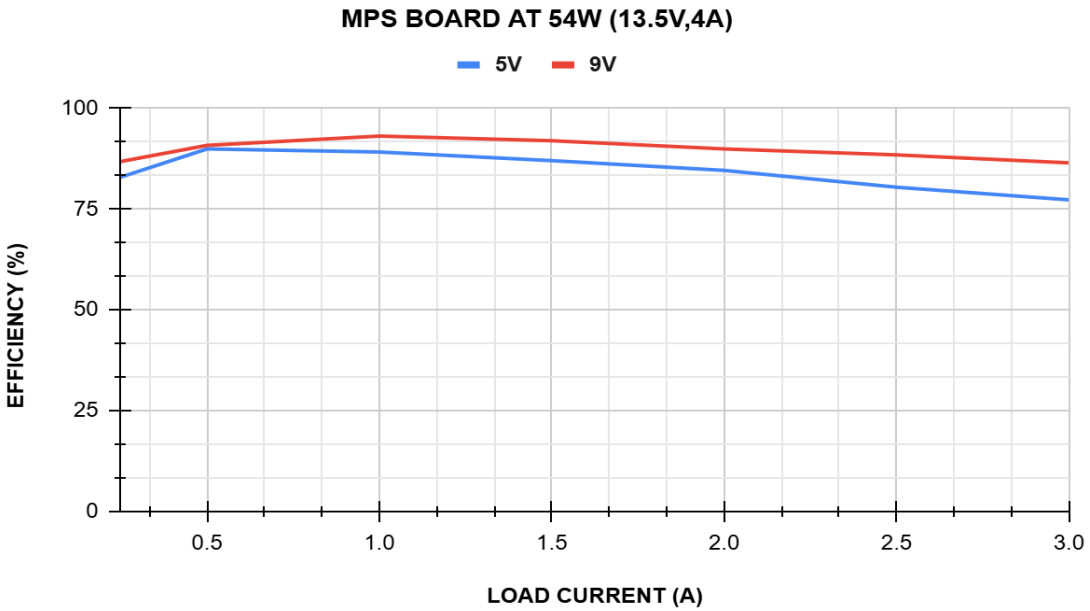

Figure 4.23: Efficiency Characteristics of MPS Board at 54W

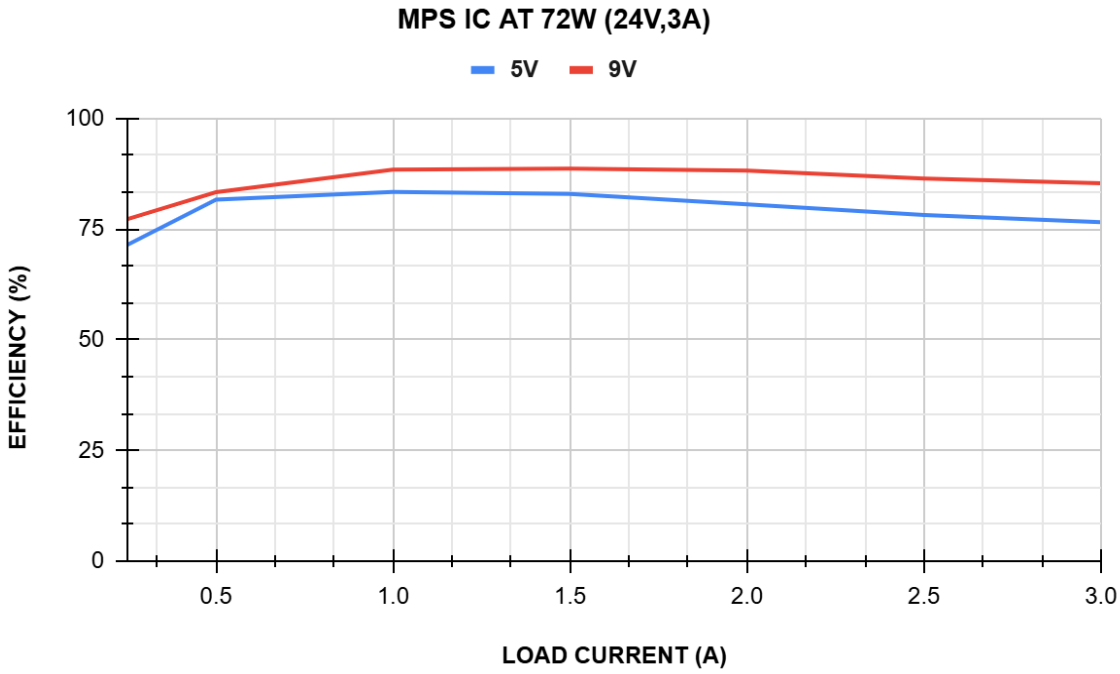

Figure 4.24: Efficiency Characteristics of MPS Board at 72W

Under an input condition of 54W (13.5V, 4A), the maximum efficiency observed for the 5V profile was approximately 87.3% at a load current of 1A, while the 9V profile achieved approximately 91.9% at the same load current.

Under 72W input (24V, 3A), the 5V profile's max efficiency drops to about 82.3% at 1A, while the 9V profile reaches about 87.6% at 1.5A.

Results show converter efficiency drops slightly at higher input voltages due to increased switching losses. Efficiency rises with load current, peaks at medium loads, and then declines at higher loads due to conduction and thermal losses.

4.6 Load Regulation Testing for MPS Board

Figures 5.4 and 5.5 show the load regulation of the MPS board at 36W and 72W. The output voltage gradually decreases with load current for both 5V and 9V PDO profiles.

At 36W operation, the 5V output voltage decreased from approximately 4.89V to 4.05V, while the 9V output reduced from approximately 8.9V to 8.05V as the load current increased up to 3A.

During 72W operation, the 5V profile dropped from 4.89V to 4.05V, and the 9V profile from 8.9V to 8.05V under full load.

The 9V profile showed better voltage regulation due to lower current for the same power, reducing losses in MOSFETs, inductor and capacitor. Almost Stable operation occurred across all load conditions.

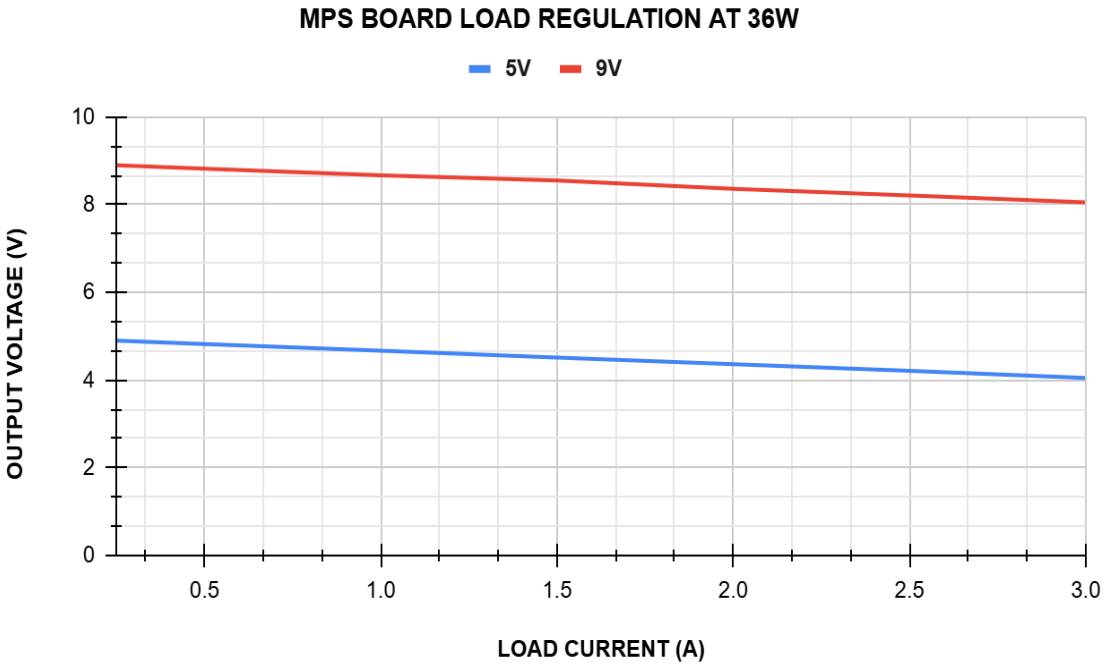

Figure 4.25: Load Regulation Characteristics of MPS Board at 36W

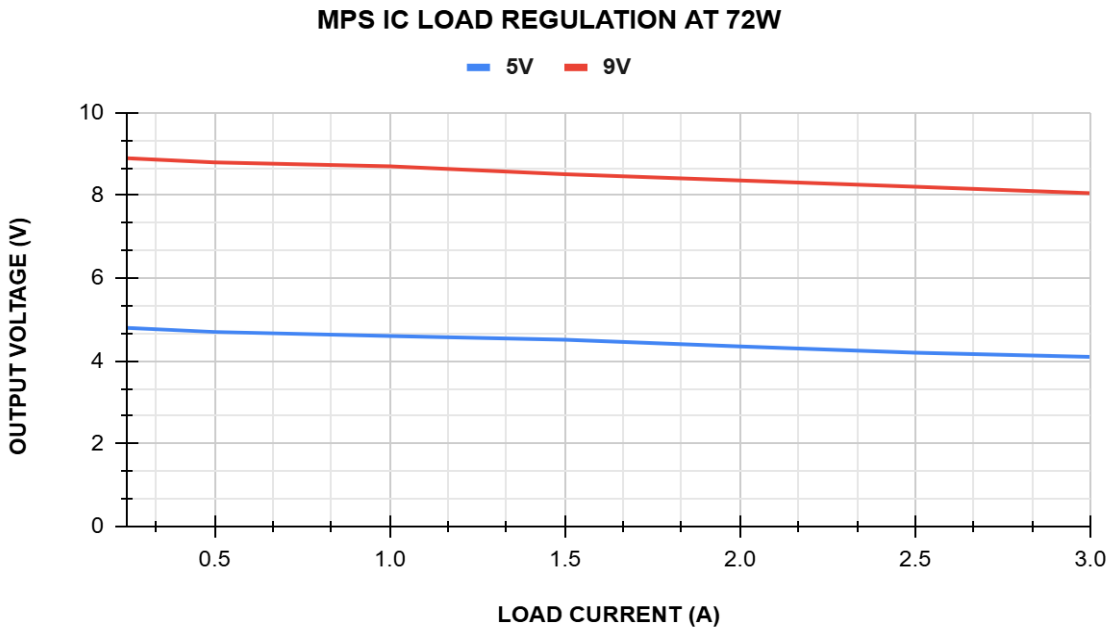

Figure 4.26: Load Regulation Characteristics of MPS Board at 72W

4.7 Experimental Evaluation of Renesas Board

Figures 4.27, 4.28, and 4.29 display the efficiency of the Renesas USB PD board at 84W, 108W, and 140W. Results show higher output voltages yield better efficiency, with the 20V PDO profile being the most efficient.

At 84W input (28V, 3A), the 5V profile reached about 84.5% efficiency at 1A, the 9V about 89.6%, the 15V about 91.9% at 1.5A, and the 20V the highest at 93.7% at 1A.

During operation at 108w (36V, 3A), the maximum efficiency observed for the 5V profile was approximately 82.2% at a load current of 1a. The 9V profile attained an efficiency of approximately 88.5% at the same load current, whereas the 15V and 20V profiles achieved efficiencies of approximately 92.1% and 93.6%, respectively, under medium load conditions.

Under 140W (48V, 2.91A), the 20V profile showed the best efficiency of about 92.2% at 1.5A. The 15V was about 90.1%, 9V around 85.5%, and 5V at 79.2%.

The results indicate that efficiency improves at higher output-voltage operation because a lower output current is required for the same power transfer, reducing conduction losses in the converter stage. It was also observed that efficiency increased initially with load current, reached a maximum value at medium load conditions, and then gradually decreased at higher load due to thermal and switching losses.

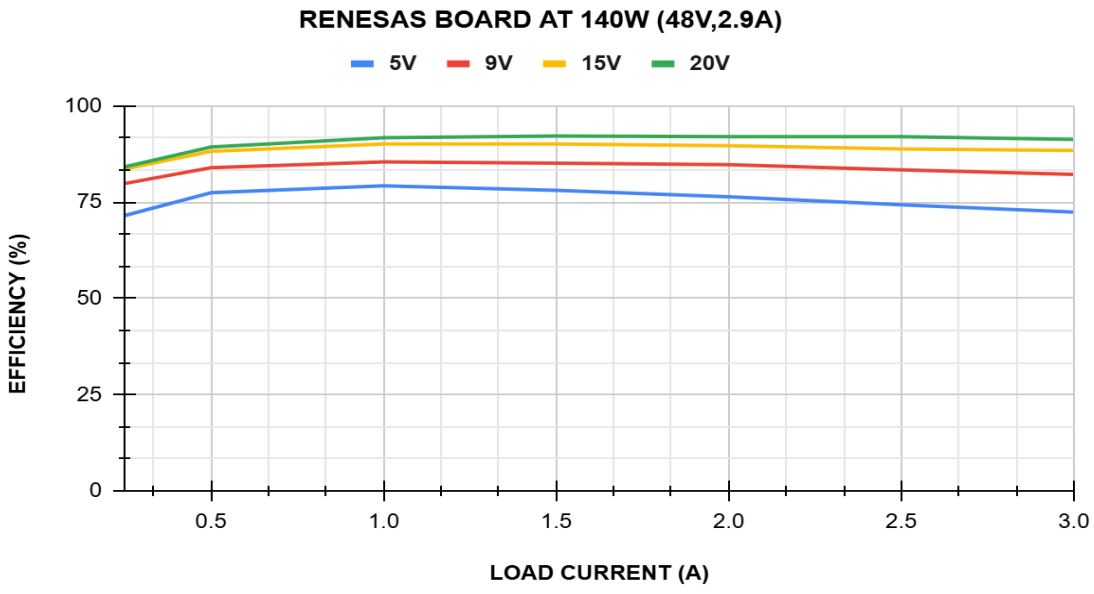

Figure 4.27: Efficiency Characteristics of Renesas Board at 84W

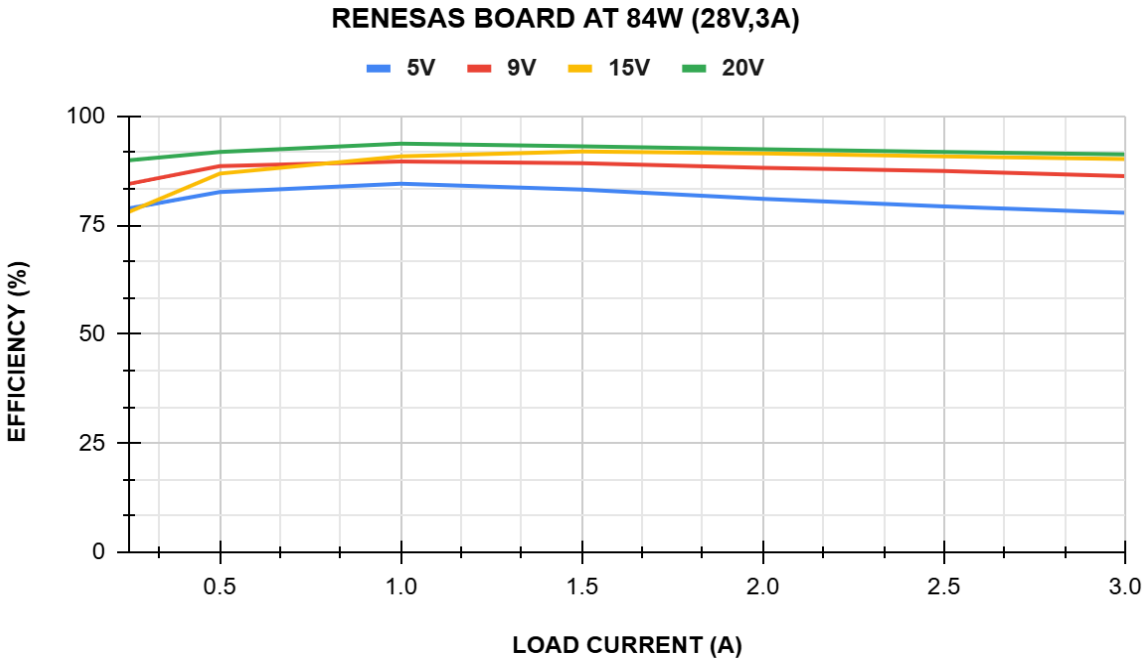

Figure 4.28: Efficiency Characteristics of Renesas Board at 108W

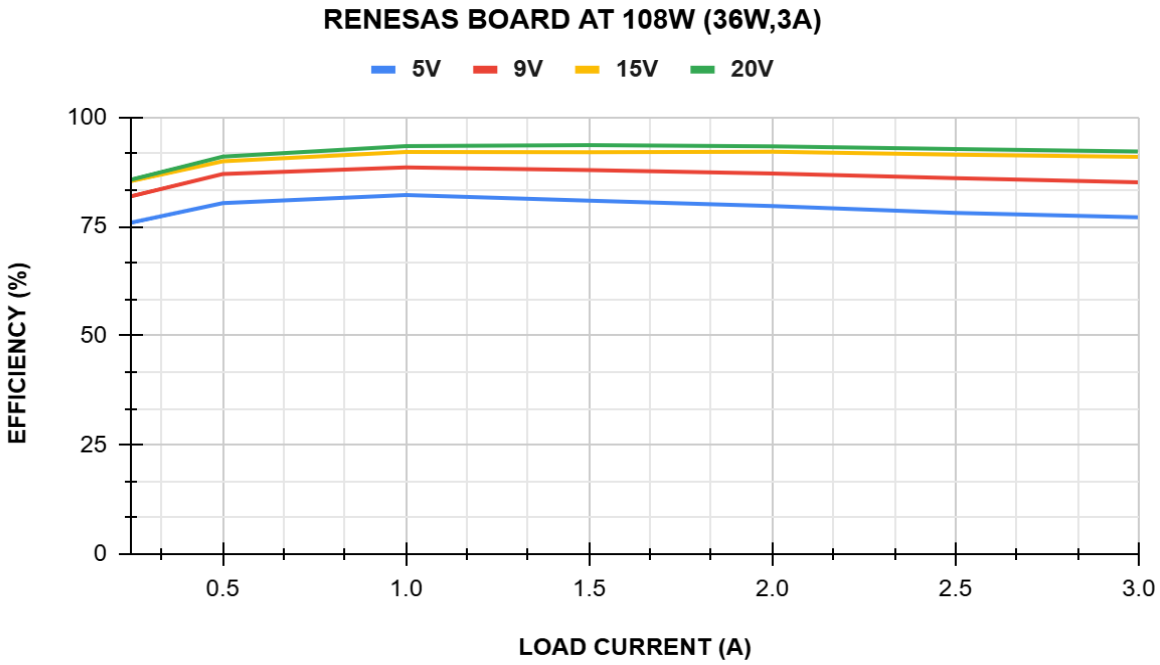

Figure 4.29: Efficiency Characteristics of Renesas Board at 140W

4.8 Load Regulation Testing for Renesas Board

Figure 4.30 and Figure 4.31 show the load regulation characteristics of the Renesas board under varying load current conditions. The output voltage gradually decreased with increasing load current for all tested PDO profiles.

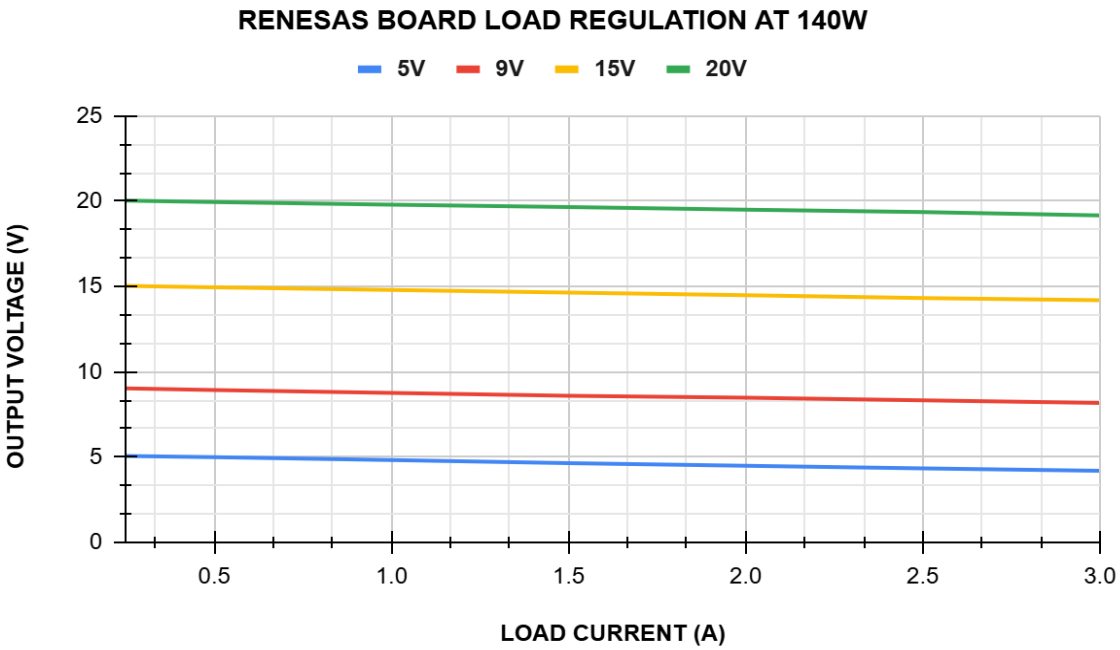

Figure 4.30: Load Regulation Characteristics of Renesas Board at 84W

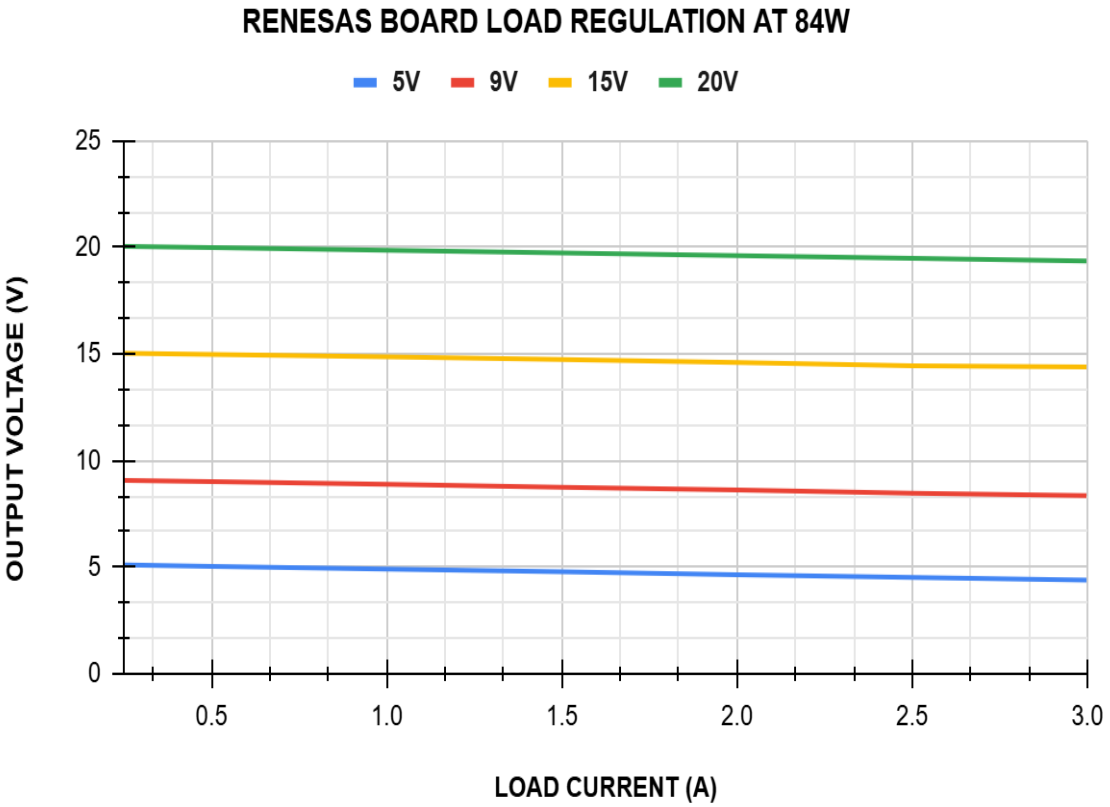

Figure 4.31: Load Regulation Characteristics of Renesas Board at 140W

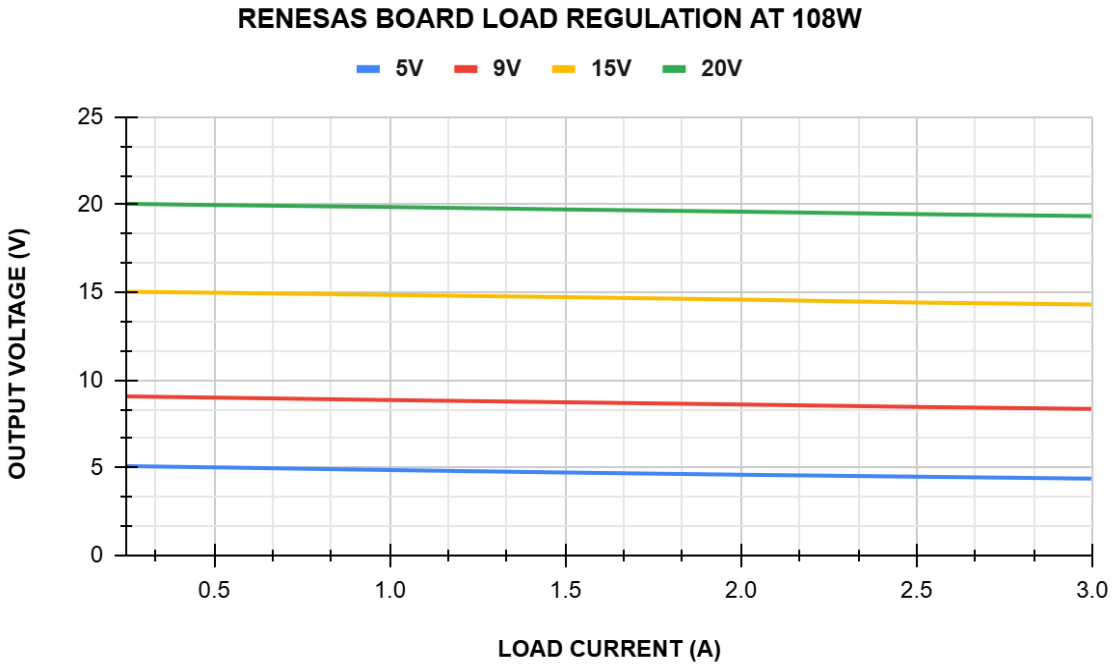

Figure 4.32: Load Regulation Characteristics of Renesas Board at 108W

During 140W operation, the 5V output voltage reduced from approximately 5.07V to 4.19V, while the 9V profile reduced from approximately 9.02V to 8.17V at full load condition. Similarly, the 15V profile decreased from approximately 15.03V to 14.2V, whereas the 20V profile reduced from approximately 20.03V to 19.17V as the load current increased up to 3A.

At 84W operation, similar load regulation behavior was observed, where higher voltage profiles showed comparatively better voltage stability than lower voltage profiles. The 20V output profile maintained the most stable regulation because lower current flow reduced conduction losses across MOSFETs, inductors.

4.9 Protection Testing

Figure 4.33 shows the Injoinic IC converter's short circuit protection. During a fault, the output voltage dropped below 4.1V, causing the IC to stop switching at the LX pin and shut down. After 2 seconds, it automatically restarted in hiccup mode.

Figure 4.33: SC Protection Response of Injoinic IC Observed on Oscilloscope

When input voltage dropped below 6.9V, the converter detected undervoltage, disabled switching at LX for 4 sec (see figure 4.34), causing output voltgae zero and protection mode. Normal operation resumed once input exceeded UVP threshold.

Figure 4.34: Input UnderVoltage Protection (UVP) Response of Injoinic IC

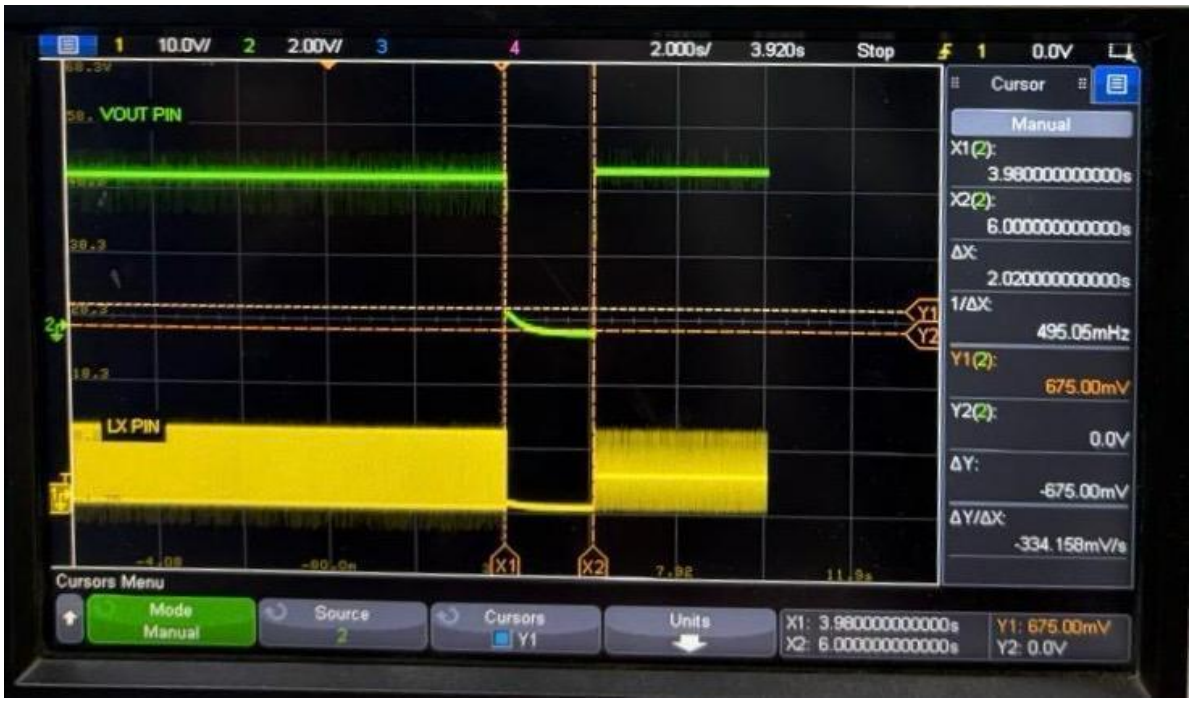

Figure 4.35: Output UVP and Hiccup Restart Response of Injoinic IC

Figure 4.35 shows that during heavy fault conditions, the output voltage fell below the 4.35 V under-voltage threshold. This caused the converter to disable the LX switching pulses for 2 sec and then restart again.

Figure 4.36: DP Pin OverVoltage Protection Response of Injoinic IC

Applying a 7.4V battery voltage to the DP pin triggered the overvoltage protection. This disturbance in the communication waveform caused the IC to go in over voltage protection of these lines. Refer to Figure 4.36.

Figure 4.37: CC Pin OverVoltage Protection Response of Injoinic IC

During CC pin protection testing, 7.4V from a battery was applied to CC1 pin. Fig 4.37 The communication waveform became unstable, and the IC stopped functioning after detecting overvoltage on the CC line.

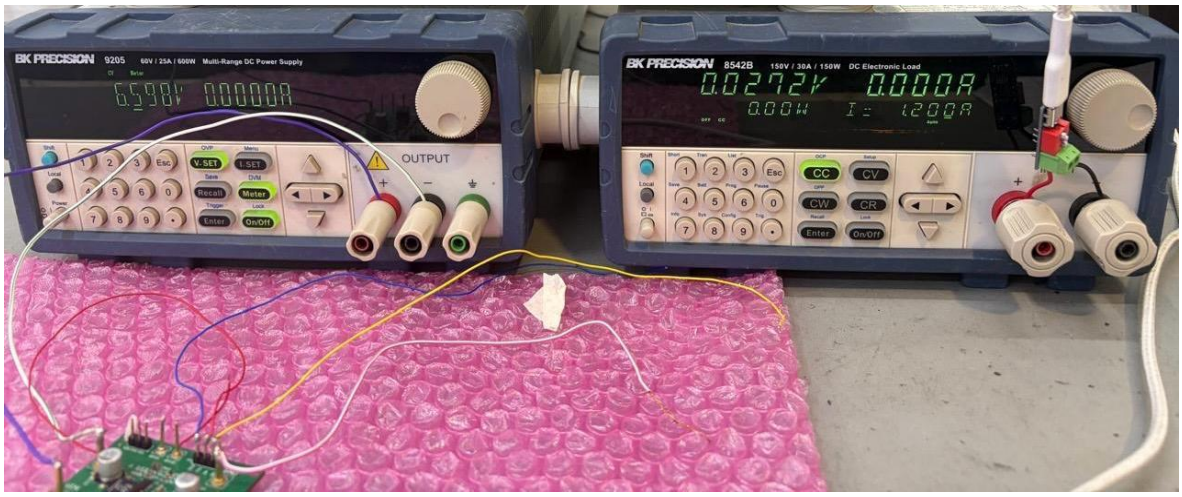

Figure 4.38: Input UnderVoltage Protection Testing of MPQ4241

During testing, the input power was lowered to 6.5V. Figure 4.38 illustrates this: at low input voltage, the converter ceased switching and disabled the output to prevent unstable operation. When the input voltage rose again, normal output function was automatically restored.

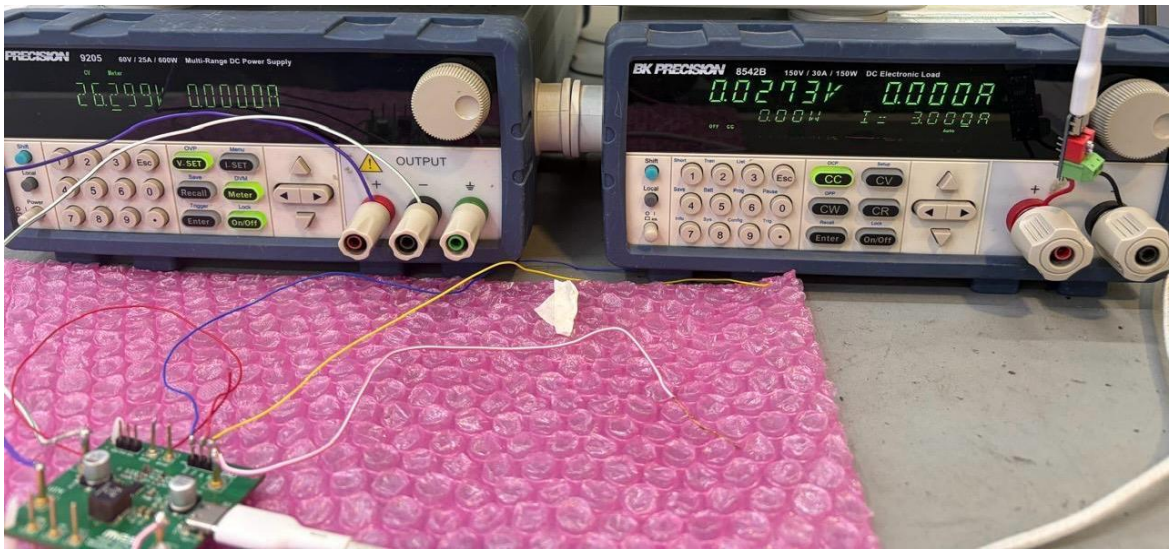

Figure 4.39: Input OverVoltage Protection Testing of MPQ4241

For OVP testing, the input voltage was raised near 27V, as shown in figure 4.39. Once it exceeded the protection limit, the IC shut down switching to protect the power stage from excessive input stress. The output automatically recovered once the input voltage was below the higher limit.

4.10 Conclusion

This chapter presented the experimental testing and performance evaluation of the selected USB PD charging s under different operating conditions. The Injoinic demonstrated stable USB PD operation and satisfactory efficiency for compact automotive charging applications. Converter behavior was found to vary with input voltage, load condition, and passive component configuration.

The MPS demonstrated higher efficiency, better load regulation, and increased flexibility during testing. Reliable USB PD negotiation and stable PPS operation were also confirmed with the PD analyzer setup. Initial tests on the Renesas Board showed strong high-power performance, though full validation was halted due to hardware damage encountered during testing.

The experimental results further demonstrated that the efficiency of the converter, its thermal behavior, and regulation characteristics are profoundly affected by the selection of the inductor, the placement of the capacitor, and the design of the switching loop.

CHAPTER 5 - COMPARATIVE ANALYSIS AND CONCLUSION

5.1 Comparative Analysis of Automotive USB PD s

The experimental efficiency curves from Figures 4.1 to 4.10 demonstrated discernible variations in converter performance across diverse load and voltage conditions. The Injoinic IC ensured stable operation for 36W automotive charging applications, featuring a compact hardware design and dependable protective functionalities which we required for our cluster board.

From Figures 4.3, 4.4, and 4.5, the MPS board exhibited superior efficiency during 9V PDO operation in comparison to 5V operation due to the inductor and capacitor they choose. The peak efficiency was observed under moderate load conditions, with a gradual decline at higher loads due to increased thermal and conduction losses.

Additionally, the load regulation plots in Figures 4.6 and 4.7 demonstrated stable output voltage regulation across varying load current conditions. The Renesas Board demonstrated the highest high-power performance among all tested s because of the buck combination used in that board.

As shown in Figures 4.8, 4.9, and 4.10, higher voltage PDO profiles like 15V and 20V achieved greater efficiency than lower voltage settings during 84W, 108W, and 140W tests.

Table 5.1 compares the performance of automotive USB PDs. The MPS had better efficiency at medium power, while the Renesas Board excelled at high power. The Injoinic IC offered a simpler setup for compact TFT automotive applications.

Table 5.1: Performance Comparison of USB PD s

Parameter	**INJOINIC IC**	**MPQ4241**	**Renesas**
Power Range	36W	72W	140W
Best Efficiency Observed	89%	94%	93%
Best PDO Efficiency	9V	9V	20V
Load Regulation	Higher voltage drop at full load	Stable regulation	Better regulation at high power
Converter Topology	Integrated buck converter	Synchronous buck converter	3-level buck converter
Protection Response	Stable UVP/OVP/SCP	Programmable protections	Stable high-power protection

5.2 Conclusion

The experimental evaluation of the automotive USB PD charger s was conducted under various load and operating conditions, utilizing laboratory instruments, oscilloscope analysis, and PD protocol testing. The study analyzed efficiency performance, load regulation characteristics, and protocol negotiation across multiple USB PD voltage profiles.

Results indicated that operating at higher PDO voltage levels improved efficiency, primarily due to lower output current and reduced conduction losses in the converter stage.

The Injoinic IC offered a compact solution appropriate for TFT-based automotive charging applications. Stable operation was confirmed during UVP, OVP, short circuit, and communication line protection tests.

The MPQ4241 exhibited enhanced efficiency and maintained stable regulation across diverse load conditions, with additional software-based configurability facilitated through the Virtual Bench Pro interface.

Initial testing of the Renesas Board demonstrated stable operation under high power conditions reaching up to 140W, with enhanced efficiency observed during 15V and 20V PDO operations.

However, comprehensive protection validation and extended testing were not possible due to damage incurred to the evaluation board during the experimental phase. The results obtained confirm that the converter topology, operating voltage profile, and load conditions substantially impact the practical performance of automotive USB PD charging systems.

5.3 Future Scope

Additional experimental efforts could focus on validating automotive-grade EMI/EMC, conducting thermal tests under prolonged high power conditions, and performing long-term reliability assessments across various battery types and environmental scenarios.

Future studies could explore USB PD 3.1 EPR for 28V, 36V, and 48V charging profiles, which are common in high-power automotive and industrial applications.

Additional research can be conducted on advanced converter architectures, such as GaN-based high-frequency converters, to improve power density and reduce switching losses during high-power operation.

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Future implementations can also integrate intelligent thermal monitoring, adaptive protection control, and real-time communication with automotive systems via CAN or LIN interfaces to improve charging management and system-level monitoring.