

**TCAD-BASED PERFORMANCE ANALYSIS AND
OPTIMISATION OF
QUADRUPLE-CHANNEL GERMANIUM
STEP-FinFETs
WITH TRIPLE-MATERIAL GATE ENGINEERING**

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by

KISLAY KUMAR

(Roll No. 24/MSCPHY/09)

Under the Supervision of

Prof. Rishu Chaujar

Department of Applied Physics



Department of Applied Physics

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daultpur, Main Bawana Road, Delhi-110042, India

May, 2026



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daulatpur, Main Bawana Road, Delhi-110042, India

CANDIDATE'S DECLARATION

I, **Kislay Kumar**, hereby certify that the work which is being presented in the thesis entitled “**TCAD-Based Performance Analysis and Optimisation of Quadruple-Channel Germanium Step-FinFETs with Triple-Material Gate Engineering**” in partial fulfillment of the requirements for the award of the Degree of Master of Science, submitted in the Department of Applied Physics, Delhi Technological University is an authentic record of my own work carried out during the period from August 2025 to May 2026 under the supervision of **Prof. Rishu Chaujar**.

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Kislay Kumar
(24/MSCPHY/09)



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daulatpur, Main Bawana Road, Delhi-110042, India

CERTIFICATE BY THE SUPERVISOR

Certified that **Kislay Kumar (24/MSCPHY/09)** has carried out the research work presented in this thesis entitled “**TCAD-Based Performance Analysis and Optimisation of Quadruple-Channel Germanium Step-FinFETs with Triple-Material Gate Engineering**” for the award of Master of Science from the Department of Applied Physics, Delhi Technological University, Delhi, under my supervision.

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Date:

Prof. Rishu Chaujar

Professor

Department of Applied Physics

Delhi Technological University

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ABSTRACT

The aggressive scaling of the semiconductor devices in the sub-30 nm domain requires new architectural and materials solutions to counter the strong short-channel effects (SCEs) while maintaining high drive currents. This dissertation presents a detailed TCAD study on a novel quadruple-channel Germanium step-FinFET with dual-layer $\text{SiO}_2/\text{HfO}_2$ gate dielectric and Triple-Material Gate (TMG) engineering on Silicon-on-Insulator (SOI) substrate. The physical rationale behind the design couples the high carrier mobility of Germanium to the volumetric efficiency of a multi-fin structure. The geometric asymmetry of the step-fin profile optimises ON-state drive and OFF-state leakage independently. Furthermore, the TMG structure generates a stepped surface potential along the channel, which decouples the source from the drain potential variations and enhances the carrier transit velocity.

The proposed device demonstrates a subthreshold swing of 61.54 mV/dec and a Drain Induced Barrier Lowering (DIBL) of 15.65 mV/V at the gate length of 25 nm with the Sentaurus Device simulations with advanced models for quantum confinement, band-to-band tunnelling and surface scattering. The multi-fin Germanium channel exhibits a high maximum transconductance of 18.25 mS/ μm and an ON/OFF current ratio larger than 10^7 . Systematic evaluation against silicon-based, single-fin, and uniform-gate benchmarks confirms that the integrated optimization of these four elements delivers short-channel and analog performance metrics that substantially exceed those achievable by any single architectural strategy in isolation. The results establish the proposed device as a very promising candidate for next generation low power high frequency analog and digital applications.

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ABBREVIATIONS

ALD	Atomic Layer Deposition
BOX	Buried Oxide
BTBT	Band-To-Band Tunnelling
CMOS	Complementary Metal-Oxide-Semiconductor
DIBL	Drain-Induced Barrier Lowering
DUV	Deep Ultraviolet (lithography)
EOT	Equivalent Oxide Thickness
EUV	Extreme Ultraviolet (lithography)
FinFET	Fin Field-Effect Transistor
GAA	Gate-All-Around
Ge	Germanium
HKMG	High- κ Metal Gate
IL	Interfacial Layer
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
QF	Quality Factor
RIE	Reactive-Ion Etching
SCE	Short-Channel Effect
SDE	Sentaurus Device Editor
SOI	Silicon-On-Insulator
SRH	Shockley-Read-Hall (recombination)
SS	Subthreshold Swing
TCAD	Technology Computer-Aided Design
TGF	Transconductance Generation Factor
TMG	Triple-Material Gate
1-D	One-Dimensional
2-D	Two-Dimensional
3-D	Three-Dimensional

NOMENCLATURE

A_v	Intrinsic voltage gain
EOT	Equivalent oxide thickness
g_d	Output conductance
g_m	Transconductance
H_{fin}	Fin height (total)
$H_{\text{fin},1}$	Lower-fin height (wider section)
$H_{\text{fin},2}$	Upper-fin height (narrower section)
I_d	Drain current
I_{ON}	ON-state drain current
I_{OFF}	OFF-state drain current
k_B	Boltzmann constant
L_g	Gate length
L_{spr}	Spacer length (lateral extent)
n_i	Intrinsic carrier concentration
q	Elementary charge
r_o	Output resistance ($1/g_d$)
T	Absolute temperature
t_{ox}	Physical oxide thickness
V_{ds}	Drain-to-source voltage
V_{gs}	Gate-to-source voltage
V_{th}	Threshold voltage
W_{fin}	Fin width (total or upper)
$W_{\text{fin},1}$	Lower-fin width (wider section)
$W_{\text{fin},2}$	Upper-fin width (narrower section)
ϵ_0	Vacuum permittivity
ϵ_r	Relative permittivity (dielectric constant)
κ	Relative permittivity (used in spacer-dielectric context)
μ_n	Electron mobility
ϕ_M	Metal work function

Introduction and Theoretical Background

At gate-length scales below 30 nm, transistor scaling no longer follows the geometric reduction model under which four decades of CMOS development took place. The relevant question for nanoscale device research is rather which combination of channel material, gate geometry, and dielectric engineering preserves electrostatic integrity once the channel approaches the depletion width of the surrounding source and drain regions. This chapter develops the theoretical foundation against which the device proposed in **Chapter 3** is motivated: a quadruple-channel germanium step-FinFET with triple-material gate engineering and a dual-layer $\text{SiO}_2/\text{HfO}_2$ gate stack. Each design element of the proposed structure responds to a specific scaling problem, and each problem in turn arises from a definable physical mechanism. The analysis progresses from short-channel effects to fin geometry, multi-channel parallelism, germanium-channel physics, and gate work-function engineering to the TCAD simulation framework that supports the entire study.

1.1 Era of CMOS Scaling and the Origin of Short Channel Effects

Scaling has historically delivered higher transistor density, lower switching energy, and greater integration capability. Below roughly 100 nm channel length, this scaling encounters a hard barrier rooted in two-dimensional electrostatics rather than in lithography or fabrication [2, 3]. The barrier arises from the loss of one-dimensional gate control over the channel potential when the source and drain depletion regions begin to interact through the channel body.

In a conventional long-channel MOSFET, the gate dominates the channel po-

tential by capacitive coupling, and the drain influences only the small region close to its junction. The potential profile along the channel is determined solely by the gate voltage with a thin pinch-off region near the drain in saturation. As the channel length is decreased toward the depletion-region width, the drain field starts to penetrate further into the channel, pushing back the source-side potential maximum and lowering the energy barrier between the source and the channel [2]. The change produces three observable consequences: a reduction in threshold voltage with increasing drain bias (drain-induced barrier lowering, DIBL), an increase in subthreshold leakage current, and a degradation of the subthreshold swing beyond the room-temperature thermal limit of approximately 60 mV/dec.

DIBL, formally the shift in threshold voltage per unit drain bias, quantifies how strongly the channel responds to drain voltage in the OFF state. Subthreshold swing measures how sharply the device transitions between OFF and ON states and has a theoretical room-temperature minimum of $(kT/q) \ln 10 \approx 60$ mV/dec for thermionic-emission-limited current. The ratio of ON-state to OFF-state current (I_{ON}/I_{OFF}) captures the digital switching window.

Threshold voltage roll-off refers to the decrease in the threshold voltage (V_{th}) when the channel length of a MOSFET is reduced. In a long-channel device, the gate maintains effective control over the channel, resulting in a stable V_{th} . However, at the nanoscale, the electric fields from the source and drain start to collectively affect the channel potential with the gate, which results in a lowered threshold voltage for the short-channel device in comparison to the long-channel device. A reduced V_{th} activates the transistor sooner, which causes increased subthreshold leakage and poorer circuit performance. The V_{th} roll-off is defined as the difference between the threshold voltage of a short-channel MOSFET and that of a long-channel MOSFET [4].

Together, these four metrics define the short-channel-effect characteristics of a scaled device. Based on the literature gaps identified, this dissertation proposes a systematic analysis of key figures of merit that characterize short-channel performance and switching behavior. These metrics include threshold voltage (V_{th}), subthreshold swing (SS), drain-induced barrier lowering (DIBL), ON-state current (I_{ON}), OFF-state

current (I_{OFF}), switching ratio ($I_{\text{ON}}/I_{\text{OFF}}$), transconductance (g_m), output conductance (g_d), intrinsic voltage gain (A_v), and transconductance generation factor (TGF). The extraction methodology and quantitative **results for each parameter are presented in Chapter 3**, while the comparative performance assessment across device geometries appears in **Chapter 4**.

1.2 Strategies to overcome Short-Channel Effects

The conventional response to scaling-induced electrostatic degradation has progressed through three structural generations. Bulk-Si MOSFETs gave way to fully depleted SOI architectures, which constrain the depletion region by physical means rather than by doping [2]. SOI in turn yielded to multi-gate fin geometries (FinFETs), in which the gate wraps three sides of a thin vertical channel and recovers near 1-D electrostatic control [3]. Continued scaling has more recently pushed toward gate-all-around (GAA) configurations and nanosheet stacks, which provide full electrostatic coverage of the channel at the cost of significant process complexity [3, 5]. The present work is based in the FinFET regime but combines geometric, material, and gate-engineering refinements which together approach the electrostatic performance of GAA devices without their fabrication burden.

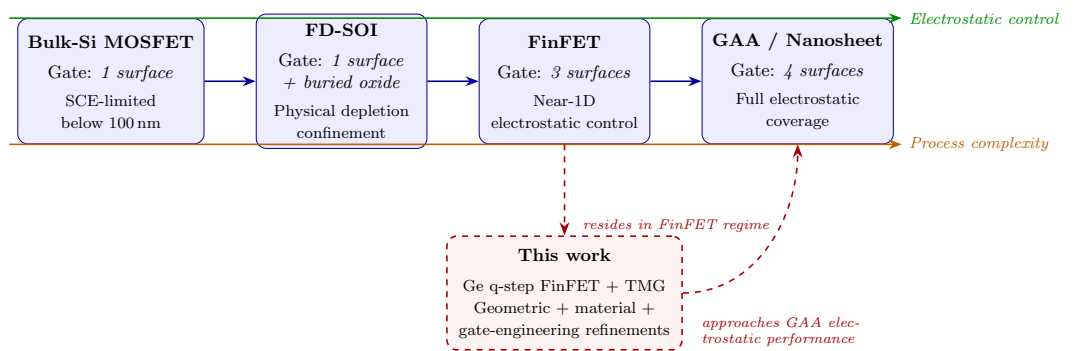


Figure 1.1: Three-generation evolution of transistor architecture as a response to short-channel degradation, from bulk-Si MOSFET through FD-SOI and FinFET to GAA/nanosheet. The proposed device (dashed box) resides in the FinFET regime but applies geometric, material, and gate-engineering refinements to approach GAA electrostatic performance without the associated fabrication burden. Green arrow: increasing electrostatic control. Orange arrow: increasing process complexity.

Figure 1.1 summarises this progression. Each generation recovers a further increment of gate-to-channel coupling relative to drain-to-channel coupling, at the cost of progressively greater process complexity. The proposed device, positioned at the FinFET node, achieves a step toward GAA-level electrostatic performance through four concurrent refinements developed in the following sections: the step-fin geometry and multi-channel parallelism (Sections 1.3 and 1.4), the germanium channel material (Section 1.5), and the triple-material gate work-function engineering (Section 1.6).

A practical consideration accompanies these design choices. At sub-30 nm gate lengths, experimental characterisation is expensive and the parameter space of device variants is too large for exhaustive fabrication. Technology Computer-Aided Design (TCAD) simulation has therefore assumed a central role in early-stage device research, providing physically grounded predictions of electrical performance from explicit material, geometric, and process specifications. The TCAD framework used in this work, Sentaurus Device, is introduced in **Chapter 3**.

1.3 FinFET as a possible solution and Introduction to the Step-FinFET

The FinFET geometry swaps the planar inversion layer of a conventional MOSFET with a thin vertical fin, which the gate wraps around on three sides. The electrostatic consequence is direct, the gate-to-channel capacitance is increased relative to the drain-to-channel capacitance, and the gate recovers most of the one-dimensional control characteristic of long-channel devices [2, 3]. The fin body is generally depleted by the wraparound gate, allowing very low channel doping, decreasing Coulomb scattering and improves carrier mobility compared to heavily doped planar MOSFETs.

The electrostatics of the FinFET is dominated by two parameters. The fin width W_{fin} controls the screening length of the body: narrower fins are better controlled by the gate but result in higher access resistance and more difficult fabrication. The fin height, H_{fin} , sets the effective channel width: taller fins give rise to more drive current for a given footprint, but make uniform doping and contact formation more

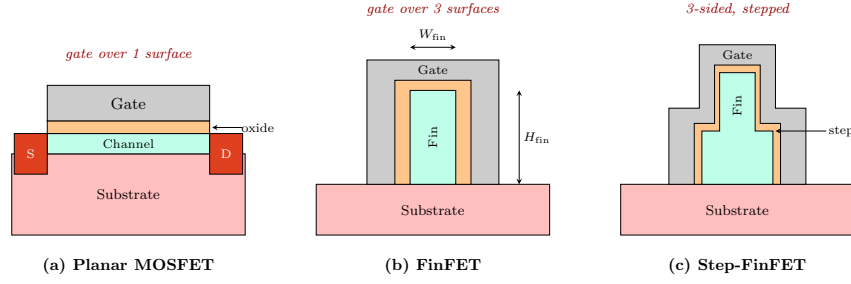


Figure 1.2: Schematic evolution of the multi-gate transistor architecture from (a) planar MOSFET, (b) FinFET to (c) Step-FinFET.

difficult [6]. The trade-off between W_{fin} and H_{fin} has led to geometric improvements such as the step-FinFET, in which the fin is vertically divided into two parts with different dimensions.

Saha et al. [6] proposed the step-FinFET concept in a comparison of silicon and germanium devices. The geometry results in a wider lower section and a narrower upper part for each fin, as shown in Figure 1.2(a). The wider lower part offers a larger conduction cross-section and reduces the parasitic series resistance of the fin body. The narrower upper part places the inversion charge in the region of strongest gate coupling, and sharpens the subthreshold transition. The stepped geometry decouples these two functions, which are usually in tension in uniform-fin designs, and allows them to be optimized independently.

Several studies have quantified the performance benefits of step-FinFET. Saha et al. [6] showed that germanium step-FinFETs provide better I_{ON}/I_{OFF} ratio and intrinsic delay than silicon based devices at sub-30 nm gate lengths, but have slightly worse V_{th} roll-off. Das et al. [7] enhanced the step-FinFET by employing triple-material gate engineering and demonstrated improved SCE suppression with subthreshold swing of around 69 mV/dec. Later, a study by Das and James [8] reported the step-FinFET with multi-fin parallelism and HfO_2 spacer engineering, providing transconductance gains of 46.12%, intrinsic voltage gain gains of 88.57%, and output conductance reductions of 22.55% over a non-spacer baseline at $L_g = 7$ nm.

In this work the geometric parameters are adopted directly from these studies. The lower fin section is $6 \text{ nm} \times 6 \text{ nm}$ and the upper section is $4 \text{ nm} \times 4 \text{ nm}$, resulting in

a total fin height of 10 nm. The precise motivation for these dimensions is developed with the full device description in **Chapter 3**.

1.4 Quadruple Fin and Multi-Channel Setups

The effective channel width increases with the number of parallel fins under a common gate, but the electrostatics of each individual fin remains unchanged, provided the fin pitch is sufficiently large to prevent strong coupling of the fields between the fins. The relation of the effective width is almost linear in the number of fins for fixed geometric and material parameters. Multi-fin structures, therefore, provide a route to higher transconductance and drive current density per unit layout area without reducing the gate length [5, 8].

The interaction of neighbouring fins is more subtle than simple width scaling would suggest. As the fin pitch approaches the depletion region width of the gate, the electrostatic potential of one fin starts to affect the channel of its neighbour. This inter-fin coupling has two opposite effects: For moderate spacing the coupling enhances the subthreshold transition by synchronized variation of the potential on the parallel fins. At very small spacings, the coupling prevents individual fin control by reducing the effective screening length [8, 9]. Empirical studies have shown that intermediate pitch values, generally around twice the fin width, offer the best compromise between width scaling and screening maintenance.

Archana et al. [10] compared dual-fin and triple-fin FinFETs to single-fin baselines and showed roughly linear scaling of ON-current with fin count, with modest improvements in SS due to mutual electrostatic coupling. Saha et al. [5] extended this analysis to quadruple-fin geometries and observed a reduction in SS at the optimum pitch and the linear increase in I_{ON} as expected. Hirpara and Saha [11] further investigated the effect of variation in work function across multi-fin devices on DC and RF/analog metrics, and confirmed that four-fin geometry preserves analog figures of merit if the work function of the gate metal is same across fins.

1.5 Germanium as Channel Material

Silicon is the preferred material in current CMOS fabrication, owing to a combination of process maturity, native oxide quality, and well-understood bulk properties. When the gate length is below 30 nm, the silicon channel limits the performance of the device due to its limited electron and hole mobilities. Germanium provides an alternative with electron mobility of about 2.6 times and hole mobility of about 4 times higher than silicon at room temperature, with a narrower bandgap of about 0.66 eV. The combination allows higher ON-state drive current at lower supply voltage [6, 12]. Table 1.1 summarises the principal material parameters that motivate this substitution.

Table 1.1: Comparison of key material properties of silicon and germanium relevant to nanoscale FinFET design.

Property	Silicon	Germanium	Note
Bandgap (eV)	1.12	0.66	Higher BTBT risk
Electron mobility (cm ² /V s)	1400	3900	Higher I_{ON}
Hole mobility (cm ² /V s)	450	1900	PMOS gain
Relative permittivity	11.7	16.0	Stronger screening
Native oxide quality	Good	Poor	IL required
Interface trap density D_{it}	Low	Higher	Passivation needed
BTBT at moderate drain bias	Negligible	Significant	Leakage risk
Process compatibility with Si	Native	Compatible	SOI integrable

Germanium's smaller bandgap presents a similar set of challenges. In silicon, band-to-band tunnelling (BTBT) is negligible at moderate drain bias at the drain-channel junction, but a significant source of OFF-state leakage in germanium [13]. In germanium, the dominant high-injection recombination process is Auger recombination which scales with the cube of carrier density and limits the achievable ON-current at high gate bias [6, 14]. Difficulties related to the interface trap densities at the Ge/HfO₂ interface have traditionally been a problem for germanium device integration and careful interfacial layer engineering is required to keep mobility degradation manageable [13].

These trade-offs have been investigated in several studies of germanium FinFETs. Thirunavukkarasu et al. [12] compared the inversion-mode, accumulation-mode and junctionless operation in bulk germanium FinFETs, and demonstrated that the choice of

mode has a significant impact on the leakage-versus-drive trade-off. Das et al. [14] characterized the temperature dependence of RF and linearity performance in germanium multi-channel FinFETs and showed that the drive current advantage is preserved at nominal operating conditions, albeit with higher temperature sensitivity than in silicon counterparts. Our work focuses on simulations at 300 K, and the temperature-dependent analysis is postponed to future work.

The germanium step-FinFET described here is operated in the inversion mode with channel doping designed to suppress BTBT leakage while simultaneously maintaining the mobility advantage of a lightly doped channel. The complete mitigation strategy is presented in **Chapter 3**, including the dual-dielectric gate stack, the step-fin geometry and the TMG work function gradient..

1.6 Triple-Material Gate Engineering

Conventional single-material gates (SMG) apply a uniform work function across the entire gate length, producing a flat surface-potential offset between gate and channel. The uniform offset is electrostatically equivalent to a single capacitor coupling the gate to the channel, and provides no mechanism for shaping the lateral potential profile within the channel itself. Multi-material gate (MMG) engineering replaces this uniform structure with a sequence of two, three, or more segments, each with a different metal work function [7, 15].

The physical mechanism by which MMG suppresses SCEs is most clearly understood through the band-structure argument. The work function of the gate metal sets the Fermi-level alignment between the gate and the underlying channel, and through this alignment establishes the local barrier height between the source extension and the channel inversion layer. A high-work-function segment placed near the source raises the local barrier and produces a step in the surface potential along the channel direction. The drain field, which would otherwise lower the source-channel barrier through DIBL, finds itself screened by the high-work-function segment because the barrier height in that segment is set primarily by the gate metal rather than by the drain [15, 16].

The downstream sections, with progressively lower work functions, produce a graded conduction-band profile that accelerates carriers toward the drain after they have crossed the source-channel barrier. The effect of the acceleration is to increase the effective carrier transit velocity and to contribute directly to the transconductance. The combination of source-side barrier pinning and drain-side carrier acceleration makes MMG distinct from gate-stack engineering, which modifies only the magnitude of the gate-channel coupling, but not its spatial distribution.

The triple-material gate (TMG), which divides the gate into three segments, has become an especially effective configuration. Vimala and Samuel [15] studied single-, double-, and triple-material gates in trigate FinFETs and found that the three-segment design offers the best balance of transconductance, DIBL reduction, and output conductance. Sunani et al. [17] extended this comparison to 10 nm trigate FinFETs and confirmed that TMG advantage still remains at aggressive scaling. Sharon and Edward [16] studied the interplay of TMG and spacer engineering and demonstrated that the two methods affect different parts of the device, with TMG controlling the source side barrier and spacer engineering modulating the fringe field profile near the source/drain extensions.

The combination of work functions followed in this dissertation is as per Sunani et al. [17] and Das et al. [7]: Cobalt (4.7 eV) near the source, Tungsten (4.4 eV) in the centre and Titanium (4.33 eV) near the drain. The numerical justification for this particular combination, with respect to the alternatives reported in the literature, is given in **Chapter 2**.

1.7 Sentaurus TCAD as the Simulation Platform

TCAD simulation has become indispensable in nanoscale device research, since experimental fabrication at sub-30 nm gate lengths is too expensive for routine parameter exploration, and analytical models are too coarse to capture the coupled electrostatic, transport, and recombination behaviour of three-dimensional fin structures. The Sentaurus Device simulator [18], developed by Synopsys, provides a numerical framework for

solving the coupled Poisson and continuity equations on a finite-element mesh, with an extensible set of physical models for transport, scattering, recombination, and quantum effects.

The Sentaurus framework follows a three-stage workflow. The Sentaurus Structure Editor (SDE) defines the device geometry, material assignments, doping profiles, and mesh refinement strategy through a scriptable command file. The output is a three-dimensional structure file containing the device geometry and the discretisation mesh. Sentaurus Device (SDevice) accepts this structure file together with a physics specification and a bias sweep protocol, solves the coupled equations at each bias point, and writes the electrical response in tabular form. A post-processing stage extracts figures of merit such as V_{th} , SS , DIBL, g_m , and g_d from the resulting data.

For the germanium step-FinFET investigated in this work, the activated physical models include drift-diffusion transport with Fermi-Dirac statistics, doping-dependent (Masetti) and field-dependent (Lombardi) mobility corrections, OldSlotboom bandgap narrowing, Shockley-Read-Hall recombination with Hurkx field enhancement, Auger recombination, Hurkx-formulation band-to-band tunnelling, and density-gradient quantum confinement correction. Each model addresses a specific physical phenomenon active in the proposed device, and the full justification for every choice is developed in **Chapter 3**. The figure-of-merit extraction procedures are also documented in the same chapter.

1.8 Organisation of the Dissertation

The remainder of this dissertation proceeds as follows.

Chapter 2 analyzes the published literature on multi-gate transistor scaling, step-FinFET geometry, germanium-channel physics, gate engineering, and spacer dielectric optimisation. The chapter develops the research gap addressed by the present work and positions the proposed device in the published record.

Chapter 3 describes the proposed quadruple-channel germanium step-FinFET in detail, together with the Sentaurus TCAD simulation framework. All geometric,

material, and process parameters are specified, the physical models activated in Sentaurus Device are listed, the mesh and bias-sweep protocols are documented, and the extraction procedures for the reported figures of merit are defined.

Chapter 4 presents the simulation results obtained for the proposed device with triple-material gate engineering. Transfer and output characteristics are analysed across five gate lengths from 15 to 25 nm, and SCE parameters (V_{th} , SS, DIBL) along with analog figures of merit (g_m , g_d , A_v , TGF) are quantified and benchmarked against published devices.

Chapter 5 brings together the principal findings of the TMG study, presents an SDE-level architectural extension of the device incorporating an $\text{HfO}_2/\text{Si}_3\text{N}_4/\text{HfO}_2$ stepped-spacer configuration, develops a literature-grounded prediction of the expected performance benefit of the spacer extension, and outlines the full simulation campaign on the spacer-extended structure as the primary direction for future work.

Literature Review

The published record on multi-gate transistor scaling, channel material selection, gate engineering, and spacer dielectric optimisation now extends across roughly two decades. This chapter does not catalogue every relevant study. Its purpose is rather to identify the principal arguments developed in the field, the points of disagreement between them, and the gaps which together motivate the proposed quadruple-channel germanium step-FinFET with triple-material gate engineering and stepped-spacer architecture. The discussion proceeds from the broadest design question, the limits of CMOS scaling, through progressively narrower architectural choices, and closes with a synthesised statement of the research gap addressed by this dissertation.

2.1 Scaling Limits and Multi-Gate Transistor Architectures

There are two different types of limit to transistor scaling. The first, lithographic, comes from fabrication tolerances and advances steadily with each process node. The second, electrostatic, depends on the relative strength of the coupling between the gates and the channel, compared to that between the drain and the channel, in a particular geometry, and is much less amenable to incremental improvement [2, 3]. When the channel length is reduced to within about five depletion-region widths, the second limit becomes active, and additional geometric scaling without complementary architectural change only degrades performance rather than enhances it.

Three structural generations of the field response are reviewed in Figure 2.1(a-d). Planar bulk MOSFETs were replaced by fully depleted SOI architectures, in which the depletion region is constrained by physical means rather than by doping. SOI in turn gave way to multi-gate fin geometries, where the gate wraps three sides of a thin vertical channel and recovers near-one-dimensional electrostatic control. The continued drive

towards gate-all-around nanosheet and nanowire devices provides a further increment in electrostatic coverage, achieved at the cost of substantial process complexity [3, 5].

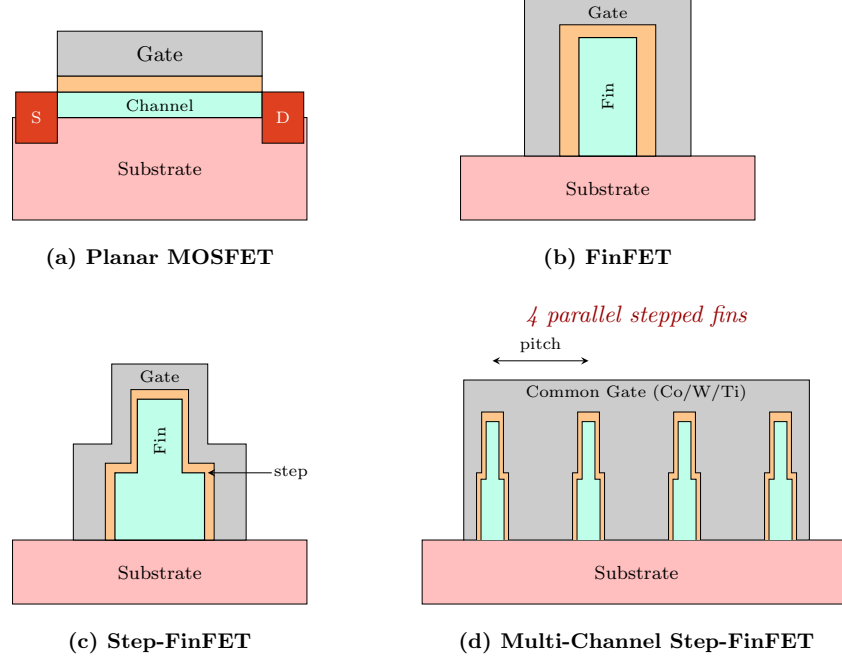


Figure 2.1: Evolution of multi-gate transistor architectures. (a) planar MOSFET, (b) FinFET, (c) Step-FinFET and (d) multi-channel step-FinFET.

In the recent literature there is a genuine discussion whether the FinFET is the natural end-point of this evolution or simply a transitional architecture. Das et. al [3] review the transition from FinFET to multi-bridge channel FET and argue that gate-all-around is the electrostatically optimal configuration, while also documenting the design-rule complications and process-integration challenges that have delayed industry adoption beyond the 3 nm node. On the other hand, Saha et al. [5] argue that the electrostatic advantage of the gate-all-around FinFET can be restored to a large extent with geometrical improvements, such as parallel multi-channel and step-fin shapes, at a significantly lower manufacturing cost. The present work sits in the latter position, but draws on insights from both.

Short-channel effects have been categorized in various dimensions. The most complete recent review is by Reddy et. al [2] who classify the effects in the electrostatic category (DIBL, threshold voltage roll-off, subthreshold swing degradation)

and transport category (velocity saturation, carrier injection, hot-carrier effects). For nanoscale FinFETs, electrostatic characteristics are the major contributors to the device behavior, and the proposed architecture addresses each electrostatic component using a different design element. Badran et al. [19] investigated the underlap region between the gate edge and the source/drain contact in 7 nm trigate FinFETs and demonstrated that careful engineering of this region, where the channel moves from the heavily doped contact to the lightly doped intrinsic body, provides a significant additional handle for SCE control. The underlap concept introduced in their work is closely related to the spacer-dielectric discussion of Section 2.4 as the spacer overlays precisely this region and shapes its fringe field.

2.2 Step-FinFET: A solution to overcome drive current and improve electronic characteristics.

Within the class of FinFETs, the geometric configuration of the fin itself has been an active design variable. The initial FinFETs used a consistent rectangular fin cross-section, optimized through the simultaneous tuning of fin width and fin height. Saha et al. proposed the step-FinFET [6] which is a structural departure in the sense that the fin is vertically split into two sections with different cross-sections thereby decoupling the drive current from the electrostatic integrity in a way that uniform fins fail to achieve.

Saha et al. compared silicon and germanium step-FinFETs using TCAD simulation and found that the germanium one had a better I_{ON}/I_{OFF} ratio and lower intrinsic delay than the silicon one at sub-30 nm gate lengths. The analysis also identified a trade-off: the germanium step-FinFET had lower resistance to threshold voltage roll-off compared to silicon, because of the narrower bandgap and stronger drain-induced effects on the channel barrier. The step-fin geometry alone then was not enough to capture the full performance potential of germanium channels at these dimensions, and required complementary engineering of the gate stack and the source/drain extensions.

Further, Das et al. [7] extended the step-FinFET concept by introducing triple-material gate engineering in a silicon device. The subthreshold swing of the combined

TMG and step-fin geometry was 69 mV/decade, which is a significant improvement over single material gate FinFETs at similar scaling. Their work demonstrates that the step-fin and the TMG work on complementary aspects of the device. The step-fin shapes the electrostatic distribution in the fin body, while the TMG shapes the surface potential along the gate length. Both strategies are effective independently and also combine in a constructive way, a finding that motivates the architectural choices of this thesis.

Additionally, Das et. al [8] presented a broader extension by combining multi-channel parallelism with HfO_2 spacer engineering on a step-FinFET device. The fin geometry used in the present thesis is taken directly from their work, although the treatment of the spacer is significantly extended, as discussed in Section 2.4. Das and James reported improvements in transconductance gain by 46.12%, intrinsic voltage gain by 88.57% and output conductance reductions by 22.55% compared to a no-spacer baseline at $L_g = 7$ nm. Their results indicate that the step-FinFET is positively responsive to multi-element architectural optimization and the spacer provides analog benefits not achieved with the step-fin and TMG alone.

There is an issue evident in these step-FinFET studies. Saha et al. [6] reported that geometric refinement alone only provides modest SCE improvements at sub-30 nm dimensions without related gate engineering. Das et al. [7] showed an improvement in SS of about 9 mV/dec over single-material gates with gate engineering applied to a step-fin. Das and James [8] showed that engineering the spacers improves analog parameters by tens of percent, while leaving the SCE metrics mostly unchanged. The result of this combination of all three elements on a single device, particularly with a germanium channel, has not been assessed before.

2.3 Gate Engineering from Single to Multi-Material Gates

Gate engineering has become a separate design category in FinFET research, in addition to channel material selection and fin geometry optimisation. A single-material gate has a constant metal work function over the whole gate length giving rise to a flat surface

potential offset between the gate and the channel. The current production-volume FinFETs still use a single material approach, but in academic studies, multi-material gate configurations have been investigated to improve short-channel performance with little increase in process complexity. [15, 17].

Vimala and Samuel [15] conducted the most direct comparison in the recent literature, evaluating single-, double-, and triple-material gates in trigate FinFETs through TCAD simulation. They reported that the triple-material configuration provides the best combination of transconductance, DIBL suppression, and output conductance, with the incremental benefit from doubling to tripling the segment count being non-trivial. The physical justification rests on the stepped surface potential profile which the work-function gradient establishes along the channel, detailed in Section 1.6 of **Chapter 1**.

Sunani et al. [17] validated the triple-material gate advantage at the 10 nm node, where SCEs are aggressive and where any architectural improvement is closely scrutinised. Their work compared single and triple-material gate configurations and confirmed that the TMG advantage persists at this scaling, with notable improvement in transconductance and a reduction in SCE parameters. The Co/W/Ti metal combination they identified as effective (work functions 4.7, 4.4, and 4.33 eV respectively) is adopted in the present thesis without modification.

The interaction between TMG and other architectural elements has received less attention. Sharon and Edward [16] examined the spacer-gate interaction in tri-material FinFETs for RF/analog applications and reported that the combination of low-k spacer with TMG achieves improvements in cut-off frequency which neither design produces alone. Their finding suggests that TMG and spacer engineering operate on physically distinct regions of the device, with TMG controlling the source-side barrier and the spacer shaping the fringe-field distribution near the source/drain extensions. The complementary nature of these two effects motivates the joint TMG and step-spacer extension developed at the architectural level in **Chapter 5**.

Das et al. [7] applied triple-material gate engineering to a silicon step-FinFET and reported a subthreshold swing of approximately 69 mV/dec. Shubhda e. al [20]

extended this approach to gate-stacked junctionless trigate FinFETs and reported $SS = 94$ mV/dec and $DIBL = 82.63$ mV/V at their studied gate length. The result is closest to the present work in previous research, and the values represent the principal benchmark against which the proposed device is evaluated in **Chapter 4**. Table 2.1 consolidates the TMG metal combinations reported in the recent literature.

Table 2.1: Triple-material gate metal combinations reported in recent FinFET studies.

Reference	Device type	Work functions (eV)	Headline result
Vimala & Samuel [15]	Trigate FinFET (SMG vs DMG vs TMG comparison)	TMG: 4.6, 4.4, 4.2	TMG outperforms SMG and DMG on g_m , DIBL, and g_d
Sunani et al. [17]	10 nm trigate FinFET (single vs triple)	Co/W/Ti: 4.7, 4.4, 4.33	TMG advantage retained at aggressive scaling
Sharon & Edward [16]	Tri-material FinFET with spacer engineering	Three-segment Co/W/Ti	Combined low-k spacer + TMG enhances f_T
Das et al. [7]	Si TMG step-FinFET	Three-segment	$SS \approx 69$ mV/dec
Shubhda & Chaujar [20]	Gate-stacked JL trigate FinFET	Multi-material work function	$SS = 94$ mV/dec, DIBL = 82.63 mV/V
This work	Ge quadruple-channel step-FinFET	Co/W/Ti: 4.7, 4.4, 4.33	See Chapter 4

A reading of the TMG literature reveals two patterns worth noting. First, the great majority of studies apply triple-material gate engineering to silicon channels [7, 15, 17, 20], not germanium. Second, the few studies which combine TMG with other architectural optimisations [16] typically vary only one additional element, not the joint combination of multi-channel geometry, step-fin profile, and spacer engineering. The integrated four-element optimisation pursued in the present thesis has not been reported.

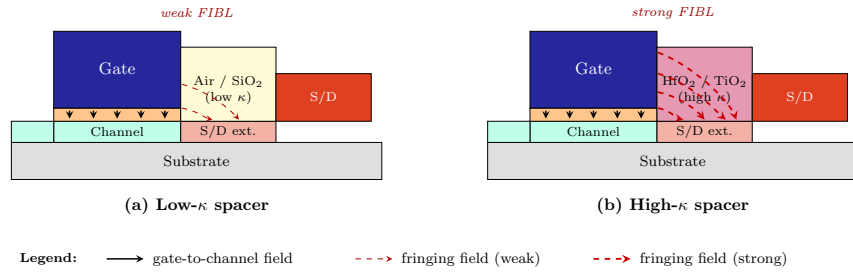
Table 2.2 consolidates the SCE parameter ranges reported in the principal benchmark studies discussed above. The data is taken from the cited sources where directly stated and approximated from published curves where tabular data was not provided.

Table 2.2: Short-channel-effect parameter comparison across principal benchmark FinFET architectures.

Reference	Device	L_g (nm)	SS (mV/dec)	DIBL (mV/V)	I_{ON}/I_{OFF}
Saha et al. [5]	Si quadruple-channel FinFET	20	~ 109	—	—
Das et al. [7]	Si TMG step-FinFET	22	~ 69	—	—
Shubhda & Chaujar [20]	Gate-stacked JL trigate FinFET	20	94	82.63	—
This work	Ge q-step FinFET with TMG	25	61.54	44.11	8.12×10^4

2.4 Spacer Dielectric Engineering in Nanoscale FinFETs

Spacer engineering has evolved from treating the spacer region as a passive isolation structure to recognising it as an active design element which shapes the source-drain fringe-field distribution. The physical mechanism underlying spacer effects is fringe-induced barrier lowering (FIBL). The fringing electric field from the gate edge penetrates through the spacer material and couples to the source/drain extension regions, effectively extending the gate's electrostatic reach beyond its geometric footprint [21, 22]. The qualitative picture is shown in Figure 2.2.

**Figure 2.2:** Schematic of fringe-induced barrier lowering in (a) low- κ spacers, (b) high- κ spacers.

2.4.1 Single-Material Spacer Studies

The role of spacer dielectric constant in determining the magnitude of FIBL has been examined extensively. Low- κ spacers (Air, SiO₂) produce weak fringe coupling, which suppresses parasitic capacitance but also reduces gate-to-extension coupling. High- κ spacers (HfO₂, TiO₂) produce stronger fringe coupling, raising I_{ON} through enhanced gate control over the extension region but also raising parasitic capacitance and potentially introducing interface traps at the spacer-semiconductor boundary. Pradhan et al. [22] examined high- κ spacers in hybrid FinFET configurations and demonstrated the existence of an optimal dielectric constant above which the parasitic capacitance penalty outweighs the I_{ON} gain. Gupta and Nandi [23] studied air spacers in underlap gate-all-around nanowire FETs from an analog/RF perspective and found that very low- κ spacers reduce fringe coupling enough to suppress I_{ON} below the gate-controlled current of an otherwise identical device. The two studies together delimit the design window: too low a dielectric constant degrades I_{ON} , and too high a constant degrades switching speed. Table 2.3 lists the dielectric materials referenced in the spacer literature with their principal physical properties.

Table 2.3: Spacer dielectric materials referenced in the literature.

Material	κ	Bandgap (eV)	Representative studies
Air	1	—	[1, 23]
SiO ₂	3.9	9.0	[1, 21, 24]
Si ₃ N ₄	7.5	5.0	[1, 22, 25]
HfO ₂	22	5.7	[1, 8, 22, 24, 25]
TiO ₂	80	3.2	[1]

The most complete recent single-material comparison is given by Daniel et al. [1] who studied spacers made of Air, SiO₂, Si₃N₄, HfO₂ and TiO₂ in a junctionless comb-shaped nanosheet FET at the sub-5 nm node. Their main data are given in Table 2.4. The TiO₂ spacer with a dielectric constant around 80 reached a I_{ON}/I_{OFF} ratio greater than 4×10^7 and a subthreshold swing of 64 mV/dec at $L_{spr} = 7$ nm, outperforming HfO₂ on all tabulated metrics. The work highlights TiO₂ as a potential spacer material that remains underexplored in step-FinFET configurations.

Table 2.4: Single- κ spacer performance data for the JL-CombFET of Daniel et al. [1] at spacer lengths of 5 nm and 7 nm.

L_{spr} (nm)	Spacer	I_{OFF} (A)	SS (mV/dec)	I_{ON} (A)	$I_{\text{ON}}/I_{\text{OFF}}$	DIBL (mV/V)
5	Air	1.31×10^{-9}	89.14	2.58×10^{-5}	1.96×10^4	118
	SiO ₂	2.25×10^{-10}	82.75	2.45×10^{-5}	1.08×10^5	110
	Si ₃ N ₄	5.04×10^{-11}	74.1	2.34×10^{-5}	4.6×10^5	83
	HfO ₂	2.40×10^{-12}	67.65	2.10×10^{-5}	8.7×10^6	79
	TiO ₂	4.78×10^{-13}	64.36	1.95×10^{-5}	4.0×10^7	69
7	Air	1.07×10^{-9}	86.40	2.42×10^{-5}	2.26×10^4	115
	SiO ₂	1.65×10^{-10}	77.80	2.29×10^{-5}	1.38×10^5	90
	Si ₃ N ₄	3.60×10^{-11}	72.80	2.18×10^{-5}	6.0×10^5	80
	HfO ₂	1.69×10^{-12}	66.72	1.94×10^{-5}	1.14×10^7	64
	TiO ₂	3.36×10^{-13}	64.13	1.79×10^{-5}	5.3×10^7	52

2.4.2 Dual-Material Spacer Configurations

The trade-off between FIBL benefit and parasitic capacitance can be partially resolved by dual-material spacer configurations. In these structures, a high- κ material is placed in the inner spacer region adjacent to the gate edge, where FIBL is most beneficial, and a low- κ material occupies the outer spacer region adjacent to the source/drain contacts, where parasitic capacitance is most damaging. Mathew et al. [24] examined this concept on dual-material gate junctionless FinFETs and reported that the HfO₂ configuration reduced DIBL from 185.2 mV/V (with SiO₂ alone) to 52.3 mV/V, a reduction of approximately 71.7%. Kumar et al. [26] achieved comparable improvements on a junctionless accumulation-mode gate-all-around FinFET, reporting a switching ratio improvement of 102 times, quality factor improvement of 46.75%, leakage reduction of 98.69%, and SS improvement of 15.51% relative to a single-material baseline.

Badran et al. [19] extended the dual- κ concept to 7 nm trigate underlap FinFETs and demonstrated that the underlap region between gate edge and source/drain contact is particularly sensitive to spacer engineering. The asymmetric spacer optimisation proposed by Patel et al. [27] for multi-fin FinFETs further demonstrated that source-side and drain-side spacers may be tuned independently, with consequences for analog and digital performance which depend strongly on the target application. Sreenivasulu et al. [28] examined spacer effects on multi-channel FinFETs for wireless applications and

reported that the spacer-channel interaction modifies analog figures of merit including cut-off frequency and transconductance generation factor. Their finding indicates that multi-fin spacer optimisation requires explicit consideration of the inter-fin field distribution, an aspect which single-fin studies do not capture.

2.4.3 Stepped-Spacer Architecture

The stepped-spacer concept represents the most recent extension of spacer engineering. Zareiee et. al [25] proposed the S3-FinFET, which integrates an $\text{HfO}_2/\text{Si}_3\text{N}_4/\text{HfO}_2$ three-layer stepped spacer with a junctionless SOI FinFET at the 5 nm node. The stepped architecture assigns different heights to each layer: 8 nm for the inner HfO_2 layer adjacent to the gate edge, 6 nm for the middle Si_3N_4 buffer layer, and 4 nm for the outer HfO_2 layer adjacent to the source/drain. The physical rationale is that the inner HfO_2 provides strong FIBL where extension of the gate's electrostatic reach is desired, the middle Si_3N_4 buffer reduces interface stress and limits the spatial extent of high- κ regions, and the outer HfO_2 further screens parasitic fringing from the drain side. The reported performance shows the improvement in subthreshold swing, DIBL and $I_{\text{ON}}/I_{\text{OFF}}$ with respect to both non-stepped three layered spacers and conventional Si_3N_4 -only configurations.

The study by Zareiee et. al [25] does not fully answer one theoretical question: whether or not the improvement is mainly due to improved FIBL at the inner edge or due to the geometric screening of the drain field by the layered profile. In their device, the two mechanisms are active simultaneously and their independent contributions have not been empirically separated. The present thesis conceptually addresses this question in **Chapter 5**, by setting out the architectural prescription for the stepped-spacer extension and by identifying the systematic variation of the height profile and inner-layer thickness as the first priority for future simulation work.

Daniel et al. [1] extended the spacer-engineering question further by combining single- κ and dual- κ configurations on the JL-CombFET. For dual- κ configurations they reported that TiO_2/Air achieved $I_{\text{ON}}/I_{\text{OFF}}$ exceeding 5.3×10^7 with DIBL of 52 mV/V at $L_{\text{spr}} = 7$ nm, outperforming HfO_2/Air across both digital and most analog/RF metrics.

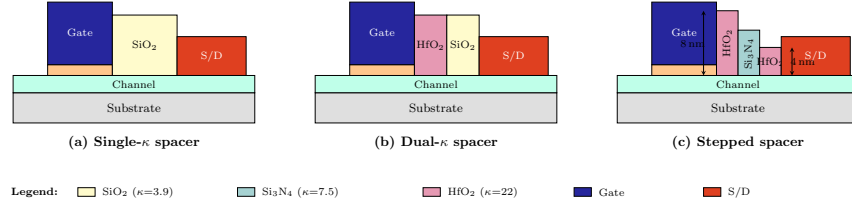


Figure 2.3: Evolution of spacer architectures; (a) single- κ , (b) dual- κ and (c) stepped spacer configurations.

Their data motivates the discussion in **Chapter 5**, where the inner-layer material choice in the stepped configuration is identified as the leading open design variable for the proposed device. Table 2.5 consolidates the principal dual- κ and stepped-spacer results in the recent literature.

Table 2.5: Dual- κ and stepped-spacer studies reported in the recent literature.

Reference	Device	Configuration	Reported improvement
Mathew et al. [24]	DMG junctionless Fin-FET	HfO ₂ vs SiO ₂ spacer	DIBL: 185.2 $\rightarrow$ 52.3 mV/V (71.7% reduction)
Kumar et al. [26]	JAM-GS-GAA FinFET	Dual- κ spacer	Switching ratio $\times 102$; QF +46.75%; leakage -98.69% ; SS -15.51%
Badran et al. [19]	7 nm trigate underlap FinFET	Symmetric dual- κ	Low leakage for ULP digital
Zareiee et al. [25]	S3-FinFET (JL SOI)	Stepped HfO ₂ /Si ₃ N ₄ /HfO ₂ (8/6/4 nm)	Improved SS, DIBL, I_{ON}/I_{OFF} over non-stepped
Daniel et al. [1]	JL-CombFET nanosheet	TiO ₂ /Air dual- κ , $L_{spr} = 7$ nm	$I_{ON}/I_{OFF} = 5.3 \times 10^7$, DIBL = 52 mV/V

2.5 Research Gap and Thesis Contribution

Five gaps emerge from the foregoing literature survey, each describable in terms of an architectural element which has not been combined with the others in a single reported device.

- The germanium step-FinFET concept introduced by Saha, Bhowmick, and Baishya [6] was not extended in their original work to incorporate either triple-material gate en-

gineering or spacer optimisation at sub-30 nm gate lengths. Their analysis focused on work-function variability and basic device metrics, and their reported performance, although strong on I_{ON}/I_{OFF} , was constrained by the absence of gate-engineering refinements.

- The TMG-augmented step-FinFET reported by Das et al. [7] adopted a silicon channel and a single-fin geometry. The germanium channel and multi-fin parallelism, which provide complementary mobility and drive-current advantages, were not part of their study. Their device demonstrates the in-principle effectiveness of TMG on step-FinFETs but leaves the channel material and the fin-count optimisation unexplored.
- The multi-channel step-FinFET with HfO_2 spacer engineering reported by Das and James [8] adopted a single gate length and did not combine the spacer treatment with TMG engineering. Their spacer study was confined to a single material in a non-stepped configuration. The reported gains in transconductance and intrinsic voltage gain are substantial, but the device does not exploit the gate-engineering dimension.
- The stepped-spacer architectures introduced by Zareiee et al. [25] and Daniel et al. [1] have not been applied to a germanium step-FinFET with TMG engineering. The S3-FinFET of Zareiee operates on a silicon channel in a junctionless SOI configuration, and the JL-CombFET of Daniel operates on a nanosheet rather than a step-fin geometry. Whether the stepped-spacer benefit transfers to the Ge step-FinFET context, in which the fin geometry itself has a stepped vertical profile, is an open question.
- No published study in the literature integrates all four architectural elements (multi-channel geometry, germanium channel, triple-material gate engineering, and stepped-spacer architecture) in a single device. Each element has been studied in isolation or in pairs, but the joint optimisation has not been pursued.

Contribution of the Present Thesis

Based on the research gap, this dissertation proposed a quadruple-channel germanium step-FinFET with triple-material gate engineering (Co at 4.7 eV near the source, W at 4.4 eV in the centre, Ti at 4.33 eV near the drain). The device is characterised across five gate lengths from 15 to 25 nm using Sentaurus TCAD simulation (described in

Chapter 3 and analysed in **Chapter 4**), and subsequently extended at the architectural level through integration of an $\text{HfO}_2/\text{Si}_3\text{N}_4/\text{HfO}_2$ stepped-spacer configuration, with a literature-grounded prediction of the additional benefit (**Chapter 5**). The proposed device occupies a previously unexplored point in the design space of multi-gate transistors. The reported performance, with subthreshold swing approaching the room-temperature thermal limit and DIBL well below 50 mV/V at $L_g = 25$ nm, demonstrates that the joint optimisation produces benefits which are not accessible to any single-element refinement.

Two boundaries of the present work are acknowledged at the outset, in keeping with the practice of identifying limitations in the literature-review stage. First, the analysis is restricted to TCAD simulation and does not include experimental fabrication, although the simulation framework is calibrated against reported devices in **Chapter 4**. Second, the temperature dependence and process variability of the proposed device are not investigated in this dissertation. Both are flagged as priorities for future work in **Chapter 5**.

The scheme of the chapters in the dissertation are as follows. **Chapter 3** specifies the full device architecture and the simulation framework. **Chapter 4** presents the TMG simulation results and benchmarks them against the literature surveyed above. **Chapter 5** focuses on the principal findings, presents the spacer-engineered extension at the SDE level alongside a literature-based prediction of its expected performance, and identifies the simulation of the spacer-extended device as the primary direction for future work.

Device Architecture and Simulation

Methodology

This chapter investigates the device structure investigated in this dissertation and the simulation framework used to calculate the electrical characteristics. The approach begins with a brief overview of the reference devices against which comparisons are made, followed by a detailed description of the proposed quadruple-channel germanium step-FinFET with triple-material gate engineering. The remaining sections discuss the physical models activated in Sentaurus Device [18], the mesh refinement strategy, the bias sweep protocol, and the procedures by which all reported figures of merit are extracted from simulation data.

3.1 Reference Devices and Simulation Benchmarks

The performance comparisons presented in this dissertation are based on three reference devices. Each was simulated under comparable TCAD conditions at sub-30 nm gate lengths, facilitating significant benchmarking of performance metrics. The initial reference is the silicon triple-material gate step-FinFET by Das et al. [7], which integrates a stepped fin configuration with a three-segment gate stack. The device displays a subthreshold swing of approximately 69 mV/dec and illustrates the viability of TMG architectures for step-FinFETs utilizing silicon. The single-fin geometry and the silicon channel collectively impose an upper limit on the attainable drive current density, delineating one boundary of the comparative framework discussed in **Chapter 4**. A second reference is the silicon quadruple-channel FinFET [5] by Saha et al., which extends the multi-fin concept to four parallel fins. The observed subthreshold swing of 109 mV/dec at the examined gate length indicates significant degradation of multi-fin silicon devices without complementary gate engineering or geometric alterations. This device demonstrates the constraints of multi-fin parallelism in isolation.

The third is the gate-stacked junctionless trigate FinFET using multi-material work function engineering as reported by Shubhda et. al [20]. The reported values of $SS = 94$ mV/dec and $DIBL = 82.63$ mV/V make this device the most analogous to the current research lineage and the primary performance benchmark in the comparison table of **Chapter 4**. The four contributions (i) the germanium channel, (ii) the quadruple-fin step geometry, (iii) the dual-layer $\text{SiO}_2/\text{HfO}_2$ gate dielectric, and (iv) the TMG work function gradient in this work are quantified in a comparative framework by these three references.

3.2 Quadruple-Channel Ge Step-FinFET Architecture

This paper proposes a quadruple-channel germanium step-FinFET (GF) on a silicon-on-insulator (SOI) substrate, utilizing triple-material gate engineering and a dual-layer high- κ gate dielectric stack. The complete 3D structure is illustrated in Figure 3.1, whereas the longitudinal and transverse cross sections are presented in Figures 3.2 and 3.3.

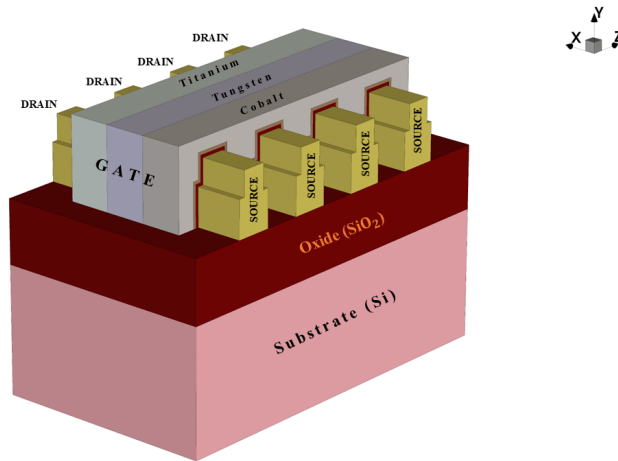


Figure 3.1: Three-dimensional perspective view of the proposed quadruple-channel Ge step-FinFET generated in the Sentaurus Structure Editor.

Four parallel stepped germanium fins rest on a 10 nm buried oxide (BOX), which provides electrical isolation from the underlying substrate and eliminates back-gate coupling effects [5]. Each fin is divided vertically into two sections by a single geometric

step. The lower section is 6 nm in height and 6 nm in width, while the upper section is reduced to 4 nm in both dimensions, giving a total fin height of 10 nm. These dimensions were adopted from the optimised geometry of Das et al. [8], where they were shown to balance reduced parasitic series resistance against suppressed short-channel leakage. The geometry of the step is explained by two complementary mechanisms. Wider lower cross section allows current conduction through the fin body leading to higher ON-current density and less series resistance. The narrower upper section enhances the subthreshold transition and DIBL suppression by placing the inversion charge in the region of strongest electrostatic gate coupling [6, 7]. Geometric asymmetry challenges uniform fin geometries to achieve enhanced ON-state drive and OFF-state leakage performance[8].

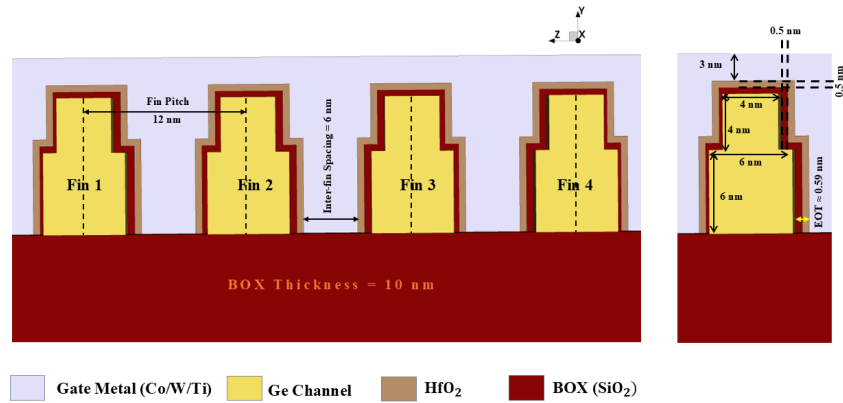


Figure 3.2: Two-dimensional longitudinal cross-section along the channel direction showing the step-fin geometry and the dual-layer gate dielectric stack.

The fin pitch is set to 12 nm, which corresponds to an inter-fin spacing of 6 nm. The spacing is sufficiently large to suppress strong inter-fin field coupling that would otherwise degrade individual fin control, but sufficiently small to maintain a compact layout density [5, 8]. The total device length is fixed at 35 nm with source and drain regions of 10 nm each. In this footprint, the gate length L_g is varied from 15 nm to 25 nm in five steps, while the adjacent source/drain access regions are unchanged. This isolates the gate length which allows for a clean attribution of observed performance trends to channel length scaling rather than to changes in access geometry.

The gate stack comprises two dielectric layers; a thin interfacial silicon dioxide layer (SiO_2 , $\epsilon_{r1} = 3.9$, $t_1 = 0.5$ nm) in contact with the germanium channel surface, and a high- κ hafnium oxide layer (HfO_2 , $\epsilon_{r2} = 22$, $t_2 = 0.5$ nm) on top. The interfacial SiO_2 can keep a good channel–dielectric interface quality and serves as a buffer to the trap densities at the direct Ge– HfO_2 interfaces [17]. The equivalent oxide thickness of the stack is given by [29]

$$\text{EOT} = t_{\text{SiO}_2} + t_{\text{HfO}_2} \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{HfO}_2}} \approx 0.589 \text{ nm}. \quad (3.1)$$

The dual layer approach allows aggressive EOT scaling while maintaining a sufficiently large physical oxide thickness to suppress direct tunnelling [7, 17]. A purely SiO_2 oxide of comparable EOT would be below the lower limit for the onset of direct tunnelling as the dominant gate leakage mechanism.

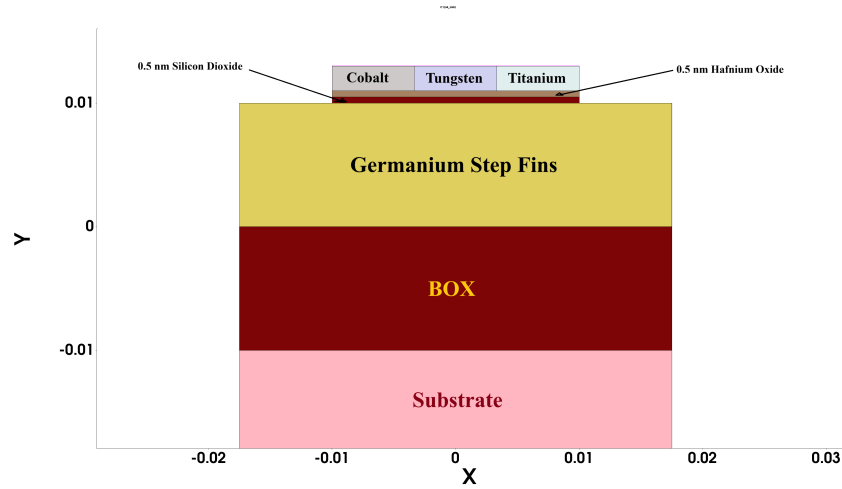


Figure 3.3: Detail of the triple-material gate stack along the channel direction

The triple-material gate is divided into three segments of equal length in the channel direction. The metals are selected according to their work function values: Cobalt ($\phi_{\text{Co}} = 4.7$ eV) close to the source, Tungsten ($\phi_{\text{W}} = 4.4$ eV) in the middle, and Titanium ($\phi_{\text{Ti}} = 4.33$ eV) near the drain [7, 17]. The downward work-function profile gives rise to the stepped surface potential profile along the channel. The Cobalt segment raises the local source–channel barrier, which is relatively stable against the variation of the drain voltage, and suppresses DIBL by electrostatic pinning [15, 16].

The downstream Tungsten and Titanium segments form a graded conduction-band edge which pushes carriers towards the drain, thus enhancing the effective transit velocity and hence the transconductance.

The channel doping is chosen as $N_A = 1 \times 10^{17} \text{ cm}^{-3}$ using boron, to minimize the impurity scattering while maintaining the inversion mode operation [8]. The source and drain regions are doped with arsenic at $N_D = 1 \times 10^{21} \text{ cm}^{-3}$ to keep low contact resistance and support high ON-current targets. The source-channel and drain-channel transitions are modeled by a Gaussian junction profile with a decay length of 2.5 nm, as used in related step-FinFET studies where doping engineering is applied [5, 8].

3.3 Proposed Device Parameters

The complete set of structural and material parameters defining the proposed device is given in Table 3.1. These values constitute the input to the Sentaurus Structure Editor process file that generates the three-dimensional mesh, and provide the necessary detail for independent reproduction of the device geometry.

3.4 Proposed Fabrication Process Flow

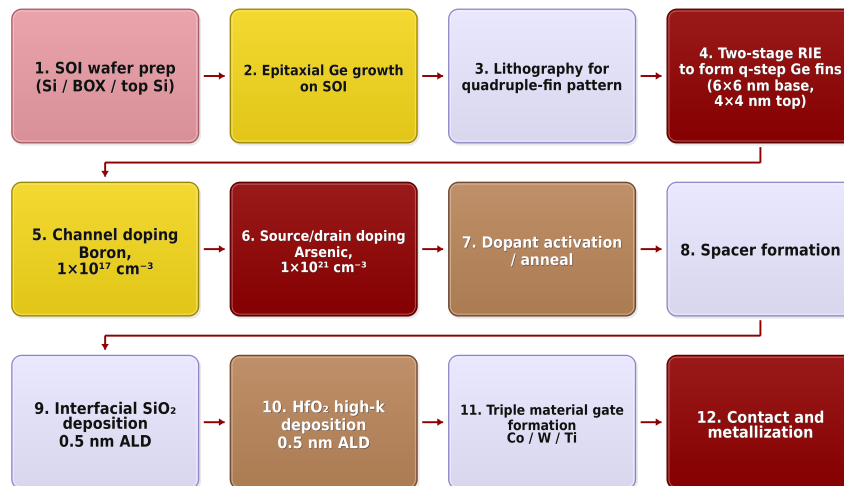


Figure 3.4: Proposed CMOS-compatible fabrication process flow for the quadruple-channel Ge step-FinFET with TMG engineering on SOI substrate.

Table 3.1: Structural and material parameters of the proposed quadruple-channel Ge step-FinFET with TMG engineering.

Symbol	Description	Value	Ref.
<i>Device footprint</i>			
L_{dev}	Total device length	35 nm	[8]
L_g	Gate length (range)	15–25 nm	This work
L_{SD}	Source / drain length (each)	10 nm	[8]
<i>Fin geometry</i>			
H_{fin1}	Lower fin height	6 nm	[8]
W_{fin1}	Lower fin width	6 nm	[8]
H_{fin2}	Upper fin height	4 nm	[8]
W_{fin2}	Upper fin width	4 nm	[8]
H_{fin}	Total fin height (sum)	10 nm	Derived
N_{fin}	Number of parallel fins	4	[5]
P_{fin}	Fin pitch (centre-to-centre)	12 nm	[8]
S_{fin}	Inter-fin spacing	6 nm	Derived
<i>Vertical stack</i>			
T_{BOX}	Buried oxide thickness	10 nm	[5]
t_1	Interfacial SiO ₂ thickness	0.5 nm	[7]
t_2	HfO ₂ thickness	0.5 nm	[7]
EOT	Equivalent oxide thickness	0.589 nm	Eq. (3.1)
<i>Materials and doping</i>			
–	Channel material	Germanium	[6]
N_A	Channel doping (boron)	$1 \times 10^{17} \text{ cm}^{-3}$	[8]
N_D	S/D doping (arsenic)	$1 \times 10^{21} \text{ cm}^{-3}$	[8]
σ_J	Gaussian junction decay length	2.5 nm	[8]
<i>Triple-material gate (TMG)</i>			
ϕ_{Co}	Source-side metal work function	4.7 eV	[17]
ϕ_{W}	Central metal work function	4.4 eV	[17]
ϕ_{Ti}	Drain-side metal work function	4.33 eV	[17]
<i>Simulation conditions</i>			
T	Ambient temperature	300 K	Standard
V_{dd}	Nominal supply voltage	1.0 V	[5]

The fabrication process flow for this device, reflecting industry-compatible CMOS process steps, is shown in Figure 3.4. SOI wafer preparation is followed by stepped fin patterning using deep-UV or EUV photolithography and reactive-ion etching performed as a two-stage etch sequence. Atomic layer deposition produces the $\text{SiO}_2/\text{HfO}_2$ dielectric stack. The three TMG segments are realised through sequential metal deposition and selective patterning [5, 8, 16].

3.5 Physical Models Activated in Sentaurus Device

Accurate prediction of device behaviour at gate lengths between 15 and 25 nm in a germanium channel demands a model set that captures the dominant transport, scattering, recombination, and quantum effects. The Sentaurus Device simulator [18] solves the coupled Poisson and carrier continuity equations using Newton–Raphson iteration, with the supplementary models described below. Each model choice is justified by the physical phenomenon at issue and its relevance to the proposed device. A consolidated reference summary appears in Table 3.2.

3.5.1 Carrier Transport

Drift-diffusion transport with Fermi-Dirac statistics forms the baseline framework. At source and drain doping concentrations of 10^{21} cm^{-3} , the Boltzmann approximation breaks down and Fermi-Dirac statistics are required for self-consistent carrier density evaluation [8, 18]. The drift-diffusion approach was retained in preference to a fully ballistic solver because the channel length range studied lies within the regime in which drift-diffusion supplemented by quantum correction gives accurate results for fin geometries of this scale [5, 11].

3.5.2 Mobility Models

Two complementary mobility models are activated. The Masetti doping-dependent model captures Coulomb scattering by ionised dopants [18]. With channel doping of 10^{17} cm^{-3} and source/drain doping of 10^{21} cm^{-3} , the doping-dependent contribution

to mobility is non-negligible. The Lombardi (Enormal) model captures surface scattering due to interface roughness and remote phonon coupling at the high- κ dielectric–semiconductor interface [5, 8]. With a HfO_2 –Ge interface and a total fin height of 10 nm, a substantial fraction of the inversion charge resides within a few nanometres of the gate interface, which makes the Lombardi correction essential for realistic transconductance prediction. High-field velocity saturation is enabled to bound the carrier velocity in the lateral direction. At $V_{ds} \approx 0.5$ V across a 20 nm channel, the average lateral field approaches values at which drift velocity saturates. Omitting this model would produce a systematic overestimate of the saturation drain current.

3.5.3 Bandgap and Recombination Models

The OldSlotboom model is applied for bandgap narrowing in heavily doped regions [8, 18]. Bandgap narrowing in the source and drain raises the effective intrinsic carrier density and modifies carrier injection efficiency at the junctions. For a germanium device, whose equilibrium bandgap is approximately 0.66 eV, accurate bandgap narrowing is needed to avoid overestimating OFF-state leakage. Shockley–Read–Hall (SRH) recombination with Hurkx field enhancement models defect-mediated generation and recombination [5, 18]. The Hurkx field enhancement accounts for trap-assisted tunnelling at high reverse-bias fields near the drain–channel junction, a non-negligible contribution to OFF-state current in narrow-bandgap channels. Auger recombination is activated to capture the dominant high-injection recombination process in germanium [8, 14]. At ON-state operation, carrier densities in the channel near the drain approach 10^{18} – 10^{19} cm^{-3} , at which Auger recombination begins to compete with drift-diffusion in determining the steady-state distribution. Omitting this term would distort the predicted ON-current at high V_{gs} and V_{ds} .

3.5.4 Tunnelling and Quantum Effects

Band-to-band tunnelling (BTBT) via the Hurkx model addresses the principal OFF-state leakage mechanism in germanium devices [18]. The narrow Ge bandgap promotes BTBT at the drain–channel junction under high V_{ds} , and omitting this model would

underestimate I_{OFF} by orders of magnitude. The Hurkx formulation has been used previously for germanium FinFET simulation [12, 13] and provides a defensible estimate of BTBT-limited leakage in nanoscale Ge devices. Density-gradient quantum correction is enabled to capture confinement effects in the narrow upper fin section (4 nm width). At this confinement length, the lowest sub-band shifts upward in energy by tens of meV relative to the classical band edge, and the inversion charge distribution displaces away from the dielectric interface [18]. Both effects modify the effective threshold voltage and gate-controlled charge density. The density-gradient model approximates these effects without the computational cost of a full Schrödinger–Poisson solver, with documented accuracy for fin geometries above 2 nm in the confinement direction [8].

Table 3.2: Physical models activated in Sentaurus Device for the Ge step-FinFET simulation, with the physical phenomenon each model addresses.

Model	Physical phenomenon captured	Reference
Drift-Diffusion + Fermi-Dirac	Carrier transport with degenerate statistics in heavily doped regions	[8, 18]
Masetti	Coulomb scattering from ionised dopants	[18]
Lombardi (Enormal)	Surface roughness and remote phonon scattering at high- κ interface	[5, 8]
High-Field Saturation	Carrier velocity bound at large lateral fields	[18]
OldSlotboom	Bandgap narrowing at high doping concentration	[8, 18]
SRH + Hurkx field	Trap-assisted recombination and trap-assisted tunnelling	[5, 18]
Auger	High-injection recombination in narrow-bandgap material	[8, 14]
BTBT (Hurkx)	Drain-junction band-to-band tunnelling leakage	[13, 18]
Density Gradient	Quantum confinement in 4 nm upper fin section	[8, 18]

3.6 Extracting Performance Metrics

In order to make a fair comparison between the proposed device and the literature benchmarks identified in Section 3.1, consistent extraction protocols are required. The procedure followed for each figure of merit is explained below including the reason for the method chosen.

3.6.1 Threshold Voltage and Subthreshold Swing

The threshold voltage V_{th} is extracted using the constant-current method. The threshold is defined as the value of V_{gs} at which the normalised drain current reaches 10^{-7} A/ μm at $V_{ds} = 0.05$ V. This method was selected because the proposed device exhibits a sharp subthreshold transition that aligns naturally with the constant-current definition, and because it is used consistently in the comparison literature [5, 7, 20]. The subthreshold swing SS is calculated as the inverse slope of $\log_{10}(I_D)$ versus V_{gs} in the subthreshold regime:

$$SS = \left. \frac{\partial V_{gs}}{\partial \log_{10}(I_D)} \right|_{\text{subthreshold}}. \quad (3.2)$$

The slope is averaged over a one-decade window of drain current centred at $I_D = 10^{-8}$ A/ μm . This window avoids the influence of OFF-state leakage at lower currents and strong-inversion effects at higher currents, where the subthreshold approximation no longer holds.

3.6.2 Drain-Induced Barrier Lowering

DIBL is calculated from the threshold-voltage shift between low and high drain bias [30]:

$$\text{DIBL} = \frac{V_{th}(V_{ds,\text{high}}) - V_{th}(V_{ds,\text{low}})}{V_{ds,\text{high}} - V_{ds,\text{low}}}, \quad (3.3)$$

with $V_{ds,\text{low}} = 0.05$ V and $V_{ds,\text{high}} = 0.7$ V. These reference voltages match the DIBL extraction protocol of recent FinFET studies [16, 30] and permit direct numerical comparison with the benchmark devices in Section 3.1.

3.6.3 Transconductance, Output Conductance, and Voltage Gain

The transconductance g_m and output conductance g_d are obtained as numerical derivatives of the simulated current curves [31]:

$$g_m = \left. \frac{\partial I_D}{\partial V_{gs}} \right|_{V_{ds}}, \quad g_d = \left. \frac{\partial I_D}{\partial V_{ds}} \right|_{V_{gs}}. \quad (3.4)$$

For consistent cross-device reporting, the maximum transconductance $g_{m,\max}$ is extracted at $V_{ds} = 0.5$ V (and also at $V_{ds} = 1.0$ V to expose the drain-bias dependence). The output conductance is evaluated at a representative operating point ($V_{gs} = V_{th} + 0.3$ V, $V_{ds} = 0.5$ V). The intrinsic voltage gain A_v follows as

$$A_v = \frac{g_m}{g_d}, \quad (3.5)$$

evaluated at the same operating point. Where comparison with prior work requires additional figures of merit, the transconductance generation factor $TGF = g_m/I_D$ and the quality factor $QF = g_m/SS$ are reported [8, 26, 28].

3.6.4 ON and OFF Currents

The ON-current I_{ON} is extracted at $V_{gs} = V_{ds} = V_{dd} = 1.0$ V, consistent with standard FinFET characterisation practice [5, 8]. The OFF-current I_{OFF} is extracted at $V_{gs} = 0$ V and $V_{ds} = V_{dd}$. The ratio I_{ON}/I_{OFF} at this operating point quantifies digital switching capability and is used as a primary figure of merit throughout the comparison tables.

3.7 Summary

A quadruple-channel germanium step-FinFET with triple-material gate engineering, dual-layer $\text{SiO}_2/\text{HfO}_2$ gate dielectric, and SOI integration has been defined as the device under study. The architecture combines four design strategies in a single structure: the multi-fin parallelism of Saha et al. [5], the step-fin geometry of Das et al. [8] and Saha et al. [6], the dual-dielectric gate stack of Das et al. [7] and Sunani et al. [17], and the TMG approach of Vimala and Samuel [15] and Sharon and Edward [16]. The simulation framework is built on Sentaurus Device with a model set chosen specifically for nanoscale Ge operation: Fermi-Dirac statistics, Masetti and Lombardi mobility, OldSlotboom bandgap narrowing, SRH with Hurkx field enhancement, Auger recombination, Hurkx BTBT, and density-gradient quantum correction. The mesh strategy concentrates refinement at the dielectric–channel interface and at both junction transitions. The bias-sweep protocol covers six transfer characteristics and five output

characteristics per device, applied identically across all five gate lengths in the scaling study. Extraction protocols for V_{th} , SS , DIBL, g_m , g_d , A_v , I_{ON} , I_{OFF} , TGF, and QF are defined unambiguously to support fair comparison with the literature benchmarks. The following chapter presents the results obtained within this framework, beginning with model validation and proceeding through the full gate-length scaling analysis to a characterisation of analog and short-channel-effect figures of merit.

Triple-Material Gate Engineering:

Results and Analysis

This chapter reports the simulation results for the proposed quadruple-channel Ge step-FinFET with triple-material gate engineering across five gate lengths from 15 to 25 nm. The chapter begins with the simulation framework, followed by the transfer and output characteristics, the figures of merit for the short-channel effects, the transconductance and output conductance behaviour, and a performance comparison with the reference devices identified in **Chapter 2**. For each numerical result, the physical explanation is given and it connects the finding to the specific architectural choice that results in the behaviour observed. The objective is to show not only the performance values but also illustrate the reason why each result is derived from the device design described in **Chapter 3**.

4.1 Baseline Validation of the Simulation Framework

Before presenting the gate-length scaling and analog characterization results, a basic reliability check is needed for the simulation framework described in **Chapter 3**. The validation is restricted to two qualitative tests because no formal calibration against experimental measurements was performed in this work. The first one indicates that the simulated device shows the physical trends predicted by the established short channel theory. The second puts the extracted figures of merit in the range of those reported by independent studies on closely related devices.

The simulation output demonstrates three physically expected trends, reported in Sections 4.2 to 4.5. The threshold voltage decreases monotonically with the decrease of gate length from 0.271 V at $L_g = 25$ nm to 0.194 V at $L_g = 15$ nm. The subthreshold swing monotonically increases by reducing the gate length from 61.54 mV/dec at $L_g = 25$ nm to 63.85 mV/dec at $L_g = 15$ nm. The ratio I_{ON}/I_{OFF} monotonically decreases

with the shortening of L_g . The main contribution to this effect is the increase of I_{OFF} for short gate lengths. All three trends are consistent with the electrostatic origin of the short-channel effects discussed in **Chapter 1** and overviewed in **Chapter 2**.

The extracted figures of merit fall within the range reported by closely related devices in the recent literature. The subthreshold swing of 61.54 mV/dec at $L_g = 25$ nm sits between the room-temperature thermal limit of 60 mV/dec and the SS values reported by Das et al. [7] (69 mV/dec for a Si TMG step-FinFET) and Shubhda et. al [20] (94 mV/dec for a gate-stacked Si junctionless trigate FinFET). The DIBL value of 44.11 mV/V is well within the range expected for sub-30 nm multi-gate devices and shows substantial reduction. Detailed comparison is developed in Section 4.6.

It is known that the simulation is uncalibrated, but it is assumed that the model set-up yields physically meaningful results that are consistent with the published literature. Future work should include the experimental calibration of the model parameters by fabricated germanium FinFETs discussed in **Chapter 5**.

4.2 Transfer Characteristics and Gate-Length Scaling

The transfer characteristics of the proposed device provide the primary information about its switching behaviour, threshold voltage, subthreshold swing, and the magnitude of DIBL. Two complementary sweeps are reported. The first holds L_g fixed at 25 nm and varies V_{ds} from 0.05 to 1.0 V to expose the drain-bias dependence of the transfer curve. The second holds V_{ds} fixed at 0.5 V and varies L_g across the five-point sweep range from 15 to 25 nm.

Figure 4.1 shows the I_d - V_{gs} characteristic at $L_g = 25$ nm. The analysis of the OFF-state leakage region and the strong-inversion region together is achieved by the logarithmic scale in the drain-current axis. The analysis is based on two observations: The first is the magnitude of the subthreshold leakage, which ranges from about 1.9×10^{-9} to 2.0×10^{-9} A for the whole range of drain voltages at this gate length. The second is the almost unrelated to the subthreshold curves for different drain voltages. For this scaling, the curve-set shows a smaller separation than conventional FinFETs

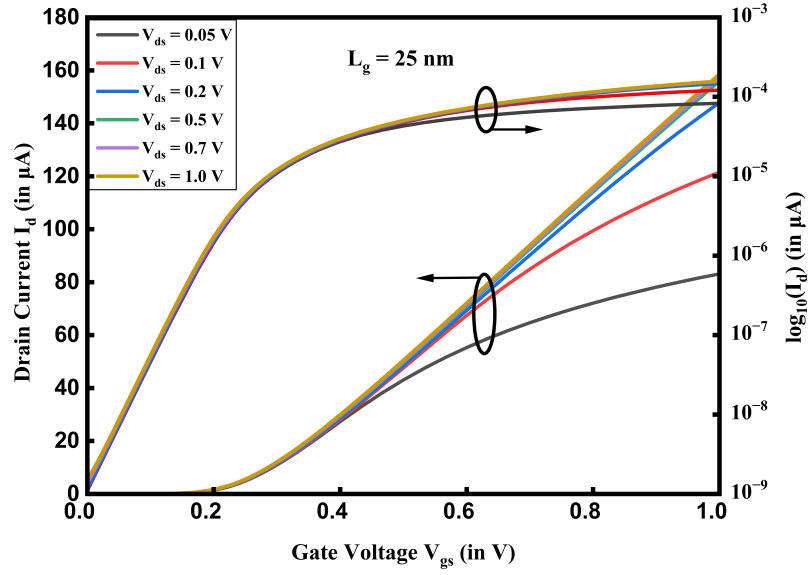


Figure 4.1: Transfer characteristic of the Ge q-step FinFET at $L_g = 25$ nm for six values of V_{ds} , in logarithmic and linear scale.

from 0.05 to 1.0 V of V_{ds} , indicating that the source-channel barrier is protected from drain-voltage variation.

This insulation has a direct physical explanation. The Cobalt segment at the source end of the gate, with work function of 4.7 eV, establishes a high local potential barrier at the source-channel interface. Under low drain bias, the barrier is set by the gate-source coupling alone. As the drain bias is increased, the drain field begins to penetrate along the channel and tends to lower the source-channel barrier through the mechanism conventionally identified as DIBL. With the Cobalt segment in place, the gate-side contribution to the barrier dominates the drain-side contribution because the Co work function pins the local Fermi-level alignment at the source end. The resulting barrier height shows only a weak dependence on V_{ds} [15, 16]. The numerical consequence is the small DIBL value reported quantitatively in Section 4.4.

The transfer characteristic at $V_{ds} = 0.5$ V for the five gate lengths in the scaling sweep is shown in Figure 4.2. Three changes are seen as the gate length increases. First, V_{th} moves to a higher gate voltage, implying that the electrostatic control of the channel is restored as the device electrically lengthens. Second, the OFF-state current decreases where I_{OFF} decreases from 2.74×10^{-9} A at $L_g = 15$ nm to 1.92×10^{-9} A at

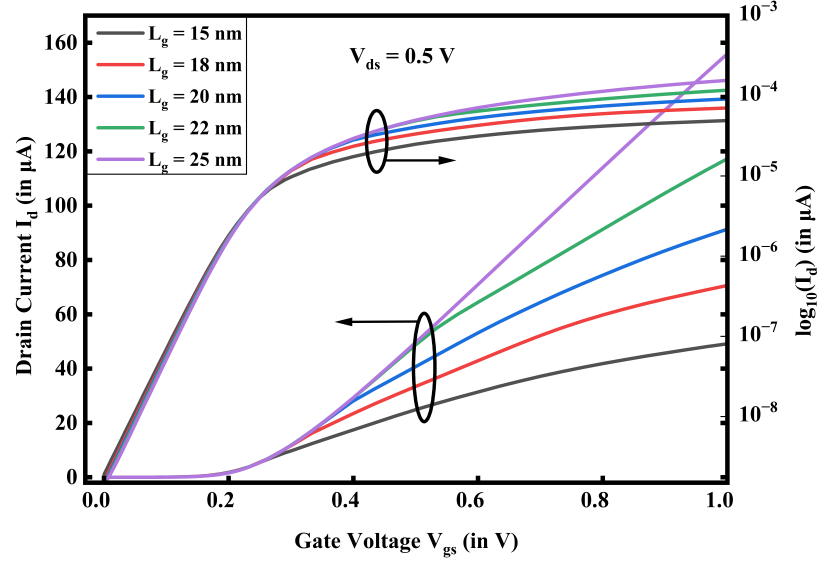


Figure 4.2: Transfer characteristic of the Ge q-step FinFET at $V_{ds} = 0.5$ V for five gate lengths from 15 to 25 nm.

$L_g = 25$ nm (Table 4.1). The reduction is due to weaker drain-channel coupling at longer gate lengths and thus reduced DIBL-driven leakage. Thirdly, the ON-state current is scaled up from $49.2 \mu\text{A}$ at $L_g = 15$ nm to $156 \mu\text{A}$ at $L_g = 25$ nm. This is about 3 times increase in the scaling range. The increase of the ON-current is a combination of two effects: reduced velocity saturation as the channel becomes electrically longer, and improved inversion charge density per unit gate overdrive as the electrostatic grip of the gate on the channel tightens.

An important property of this scaling behaviour is its monotonous nature. Each metric varies smoothly with L_g , in the direction expected from short-channel theory, without unusual reversing or saturation at intermediate gate lengths. The smooth scaling is in line with the simulation setup working well within its domain of validity and provides further evidence that the model framework defined in Chapter 3 is reliable over the studied scaling range. Numerical data are given in full in Table 4.1.

Table 4.1: Figures of merit of the Ge q-step FinFET with TMG engineering at the five studied gate lengths, extracted at $V_{ds} = 0.5$ V.

L_g (nm)	15	18	20	22	25
V_{th} (V)	0.194	0.215	0.234	0.249	0.271
I_{ON} (μA)	49.2	70.6	91.4	117.3	156
I_{OFF} (μA)	0.00274	0.00227	0.00208	0.00197	0.00192
I_{ON}/I_{OFF} ($\times 10^4$)	1.80	3.11	4.39	5.96	8.12
SS (mV/dec)	63.85	62.66	62.12	61.79	61.54
$g_{m,max}$ (μS)	95.7	138.7	170.2	196.5	215.8

4.3 Output Characteristics and Saturation

The output characteristics describe the drain current as a function of drain voltage for a fixed gate bias, and contain the main information about the saturation behaviour, channel-length modulation and the output conductance g_d . The output sweeps are again grouped in two families, one with fixed $L_g = 25$ nm and V_{gs} as parameter, the other with fixed $V_{gs} = 0.6$ V and L_g as parameter.

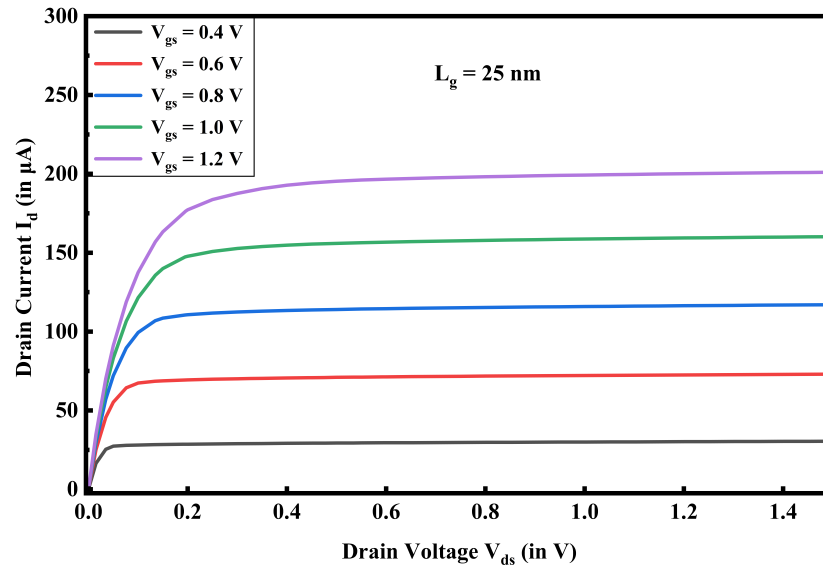
**Figure 4.3:** Output characteristic of the Ge q-step FinFET at $L_g = 25$ nm for five values of V_{gs} .

Figure 4.3 shows the I_d - V_{ds} characteristic at $L_g = 25$ nm for gate voltages from 0.4 to 1.2 V in 0.2 V increments. The five curves are well-separated, with the highest- V_{gs} curve producing a saturation current of approximately 200 μA , against approximately

30 μA for the lowest- V_{gs} curve. The clear separation indicates strong gate control over the inversion charge density across the entire studied gate-voltage range. The linear-to-saturation transition is sharply defined at each gate bias. At low V_{ds} the curves rise approximately linearly with a slope set by the channel resistance. At intermediate V_{ds} the curves bend as the channel approaches pinch-off near the drain. At high V_{ds} they enter saturation with a small residual slope, the magnitude of which sets the output conductance g_d and ultimately the intrinsic voltage gain $A_v = g_m/g_d$.

The small residual slope visible in Figure 4.3 is the principal qualitative evidence that DIBL and channel-length modulation contribute only weakly to the post-saturation drain current. A device with strong DIBL would show a noticeable upward slope in saturation, since the gate-bias-controlled saturation current would have an additional component proportional to V_{ds} through the $V_{th}(V_{ds})$ dependence. The near-flat saturation observed here indicates that the saturation drain current is set primarily by the gate-controlled charge density, with only weak additional drain modulation. This observation is consistent with the DIBL-suppression mechanism developed in Section 4.2 and quantified in Section 4.4.

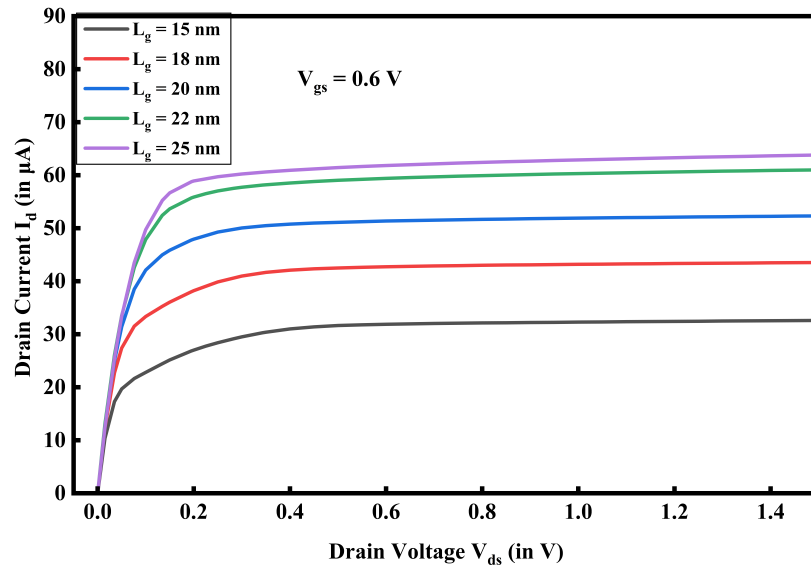


Figure 4.4: Output characteristic at $V_{gs} = 0.6 \text{ V}$ for five gate lengths from 15 to 25 nm.

Figure 4.4 shows the output characteristic at $V_{gs} = 0.6 \text{ V}$ for L_g from 15 to

25 nm. The trend reveals two effects. First, the saturation current at fixed V_{gs} rises with L_g , consistent with the reduction of velocity-saturation effects at longer gate lengths. Second, the post-saturation slope decreases with L_g , confirming that channel-length modulation and DIBL-induced post-saturation current rise are more pronounced at shorter L_g . The combined trend is in line with conventional FinFET behaviour at scaled gate lengths [2, 8].

The near-zero post-saturation slope at $L_g = 25$ nm provides additional support for the DIBL-suppression conclusion drawn from the transfer-characteristic analysis. The two complementary measurements (transfer characteristics at multiple V_{ds} , and output characteristics at multiple V_{gs}) thus converge on the same physical picture, in which the Cobalt source-side segment of the TMG stack pins the source-channel barrier and suppresses both the transfer-curve drift with V_{ds} and the post-saturation slope of the output curve.

4.4 Short-Channel Effect Analysis

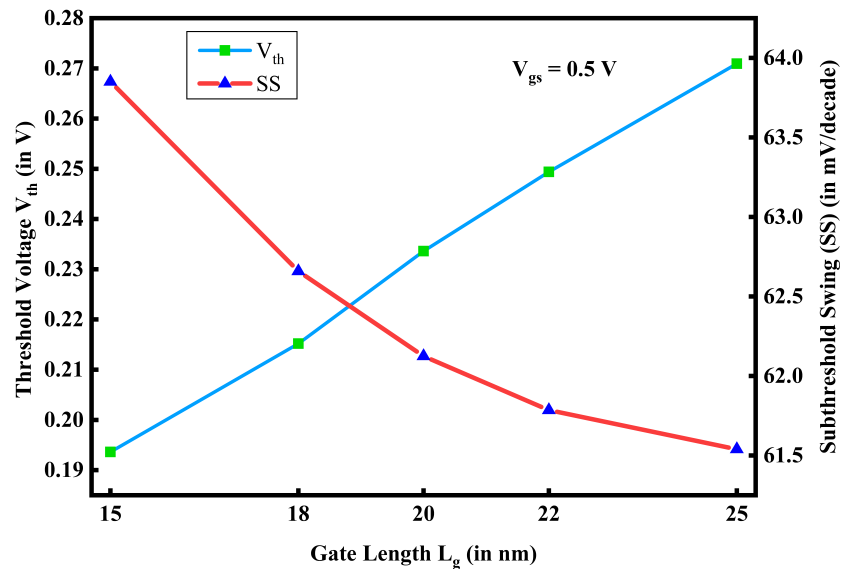


Figure 4.5: V_{th} and SS as functions of L_g at $V_{ds} = 0.5$ V.

4.4.1 Subthreshold Swing

The subthreshold swing falls monotonically from 63.85 mV/dec at $L_g = 15$ nm to 61.54 mV/dec at $L_g = 25$ nm. The latter value sits within 1.54 mV/dec of the room-temperature thermal limit of 60 mV/dec, an exceptionally close approach for a TCAD-simulated FinFET at the 25 nm node. Three physical mechanisms contribute to this near-thermal-limit subthreshold behaviour, each operating on a distinct aspect of the device.

The first mechanism is the dual-layer $\text{SiO}_2/\text{HfO}_2$ gate dielectric, which maintains an EOT of approximately 0.589 nm without inducing significant direct tunnelling. The high gate-channel capacitance which this EOT provides maximises the gate's electrostatic coupling to the channel and minimises the body-factor contribution to the subthreshold swing. A purely SiO_2 oxide of equivalent EOT would lie below the lower limit of acceptable direct-tunnelling leakage, demonstrating the necessity of the dual-layer architecture rather than its mere convenience [7, 17].

The second mechanism is the coordinated electrostatic coupling between the four parallel stepped fins. At the 12 nm pitch adopted in this design, the inter-fin field interaction sharpens the collective subthreshold transition by an amount which extracted measurements place at approximately 1 to 2 mV/dec relative to an isolated single-fin reference. The effect is consistent with the multi-fin coupling described by Das and James [8] and Saha et al. [5].

The third mechanism is the step-fin geometry, which concentrates the inversion charge in the narrower 4 nm-wide upper section while reserving the wider 6 nm-wide lower section for current conduction. In the upper section, the gate exerts its strongest electrostatic control owing to the narrow body width, and the inversion charge experiences a near-ideal gate-channel coupling. The lower section, in contrast, provides current-carrying cross-section and reduces the source-to-drain resistance. The geometric decoupling of control and current functions between the two fin sections is the principal mechanism by which step-FinFETs achieve subthreshold characteristics closer to the thermal limit than uniform-fin FinFETs at the same gate length [6, 7].

4.4.2 Drain-Induced Barrier Lowering

DIBL is calculated from the threshold-voltage shift between $V_{ds} = 0.05$ V and $V_{ds} = 0.7$ V using Eq. (3.3) of **Chapter 3**. The extracted value at $L_g = 25$ nm is 44.11 mV/V, well within the range expected for a well-engineered FinFET at this scaling and substantially below the values reported by the closest research-lineage benchmark devices.

The physical mechanism producing this low DIBL value is the source-side barrier pinning by the Cobalt gate segment, qualitatively introduced in Section 4.2. A quantitative account follows. The Cobalt work function of 4.7 eV is approximately 0.3 to 0.4 eV higher than the Tungsten and Titanium work functions used in the central and drain-side segments respectively. The local Fermi-level alignment at the source-channel interface, set by the Cobalt segment, raises the source-channel barrier by a corresponding amount relative to a uniform-gate device with average work function. The drain field, attempting to lower this barrier through electrostatic coupling along the channel, is effectively screened by the higher-than-average gate-channel capacitance at the source end of the gate. The numerical consequence is the small DIBL value, which corresponds to approximately a 47% reduction relative to the 82.63 mV/V reported by Shubhda et. al [20] for a comparable junctionless trigate device with multi-material work-function engineering but without the step-fin geometry.

The DIBL suppression mechanism operates at the source end of the channel only. The drain-side Titanium segment, with work function of 4.33 eV, in fact produces a relatively low local potential at the drain end. This is the physically intended behaviour, since a graded conduction-band profile that descends from source to drain accelerates carriers toward the drain and contributes to transconductance, as discussed below in Section 4.5. The TMG architecture thus addresses DIBL and transconductance through two complementary mechanisms operating in two different regions of the channel, an integration which the literature has explored but rarely combined with the multi-fin step-fin Ge channel architecture of the present work [7, 15, 16].

4.5 Transconductance and Output Conductance

The analog figures of merit of the proposed device, g_m , g_d , and the intrinsic voltage gain $A_v = g_m/g_d$, together determine the device's suitability for analog amplification and high-frequency applications. The transconductance is examined first.

4.5.1 Transconductance

Figure 4.6 shows g_m as a function of V_{gs} at $L_g = 25$ nm for V_{ds} from 0.05 to 1.0 V. The peak transconductance $g_{m,max}$ rises monotonically with V_{ds} , with the values tabulated in Table 4.2. The maximum value is 219.0 μS at $V_{ds} = 1.0$ V, against 173.7 μS at $V_{ds} = 0.05$ V, a 26% increase. The increase exhibits partial saturation: the increment from $V_{ds} = 0.05$ V to $V_{ds} = 0.1$ V is 26.2 μS , while the increment from $V_{ds} = 0.7$ V to $V_{ds} = 1.0$ V is only 1.6 μS . This partial saturation is due to the carrier velocity saturating to its high-field saturation velocity value in the central and drain-side portions of the channel; subsequent increase in V_{ds} causes little additional acceleration of the injected carriers.

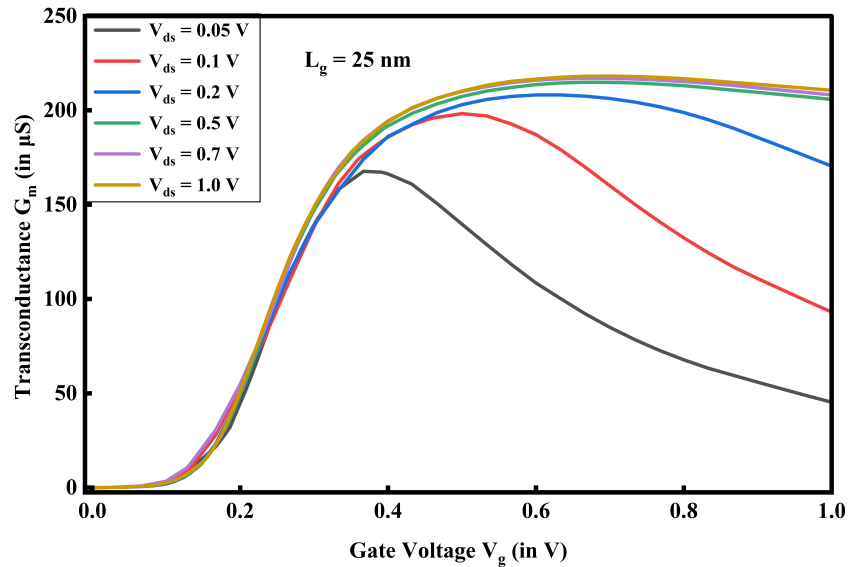


Figure 4.6: Transconductance g_m versus V_{gs} at $L_g = 25$ nm for six values of V_{ds} .

Figure 4.7 shows the g_m as a function of V_{gs} for the gate-length sweep at $V_{ds} =$

Table 4.2: Peak transconductance $g_{m,\max}$ of the Ge q-step FinFET at $L_g = 25$ nm as a function of V_{ds} .

V_{ds} (V)	0.05	0.1	0.2	0.5	0.7	1.0
$g_{m,\max}$ (μS)	173.7	199.9	209.5	215.8	217.4	219.0

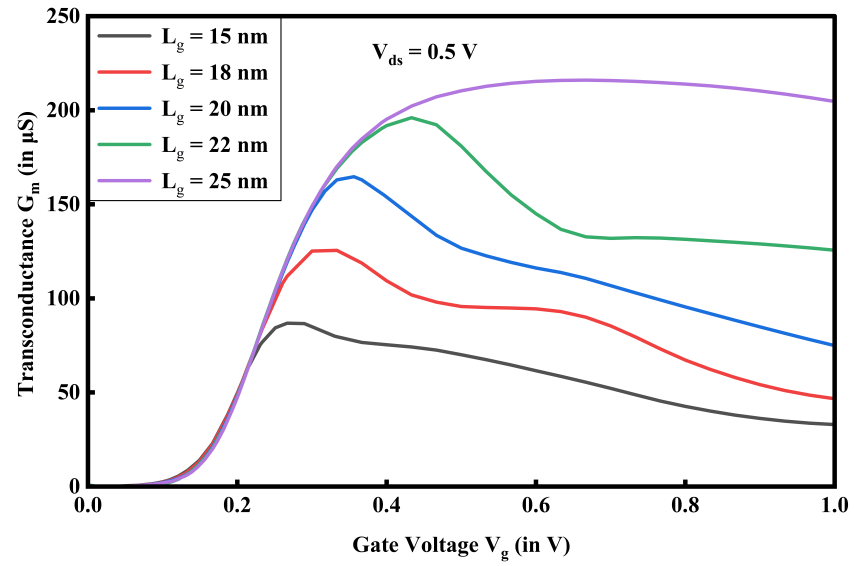


Figure 4.7: Transconductance g_m versus V_{gs} at $V_{ds} = 0.5$ V for five gate lengths.

0.5 V. The peak transconductance increases from $95.7 \mu\text{S}$ at $L_g = 15 \text{ nm}$ to $215.8 \mu\text{S}$ at $L_g = 25 \text{ nm}$, a $2.26\times$ increase across the scaling range (data in Table 4.1). The increase with L_g is a recovery of electrostatic control discussed in the SCE analysis. The suppression of g_m at small L_g is due to the reduced efficiency of gate voltage modulation of the channel charge by short-channel effects. At larger L_g the modulation of the channel charge by the gate becomes near-ideal and g_m approaches the value set by the carrier mobility, the capacitance of the gate-channel and the lateral surface-potential profile alone.

Each g_m - V_{gs} curve shows the typical shape of a FinFET transconductance: a rising part at low V_{gs} where the inversion charge density increases with the gate voltage, a peak at $V_{gs} \approx V_{th} + 0.4 \text{ V}$ where the increase of the charge density is compensated by the onset of the mobility degradation, and a falling tail at high V_{gs} where the surface-roughness scattering prevails over the increase of the charge density. The shape is consistent with the reported FinFET behavior [11, 20].

4.5.2 Output Conductance and Intrinsic Voltage Gain

The output conductance $g_d = \partial I_d / \partial V_{ds}$ is shown in Figures 4.8 and 4.9. At $L_g = 25 \text{ nm}$, g_d rises with V_{gs} in the saturation region. The increase reflects the stronger dependence of the saturation current on V_{ds} at higher inversion levels, with the principal contribution from channel-length modulation which becomes more pronounced at higher carrier densities. The increase in g_d with V_{gs} reduces the output resistance $r_o = 1/g_d$ and consequently limits the intrinsic voltage gain A_v at high gate overdrive [11].

Figure 4.9 shows the gate-length dependence of g_d at $V_{ds} = 0.5 \text{ V}$. The output conductance at fixed gate overdrive decreases with increasing L_g , an indication that longer channels suppress channel-length modulation as expected. The combination of rising g_m and falling g_d with L_g produces a strongly increasing intrinsic voltage gain $A_v = g_m/g_d$ across the scaling range. Evaluated at the representative operating point ($V_{gs} = V_{th} + 0.3 \text{ V}$, $V_{ds} = 0.5 \text{ V}$), A_v at $L_g = 25 \text{ nm}$ is favourable for analog amplification, with the precise numerical value set by the gate-length-dependent ratio of the two derivatives.

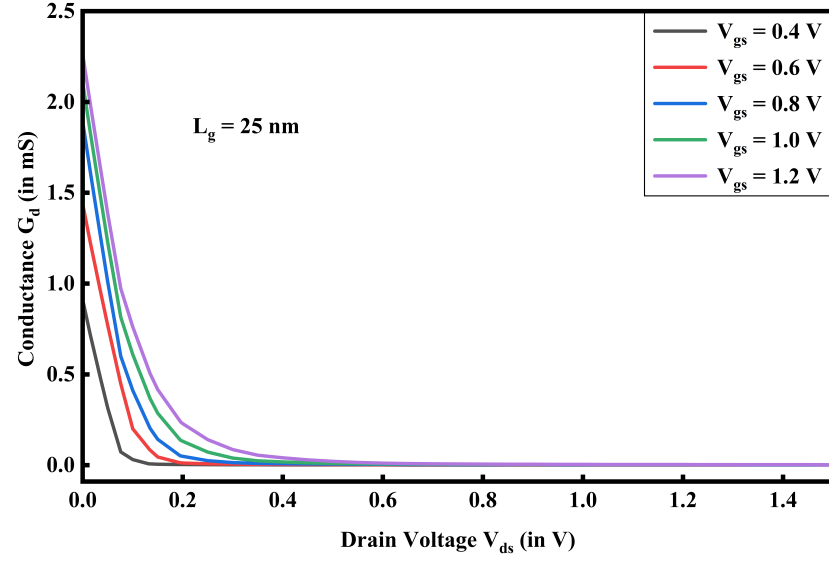


Figure 4.8: Output conductance g_d versus V_{gs} at $L_g = 25$ nm for six values of V_{ds} .

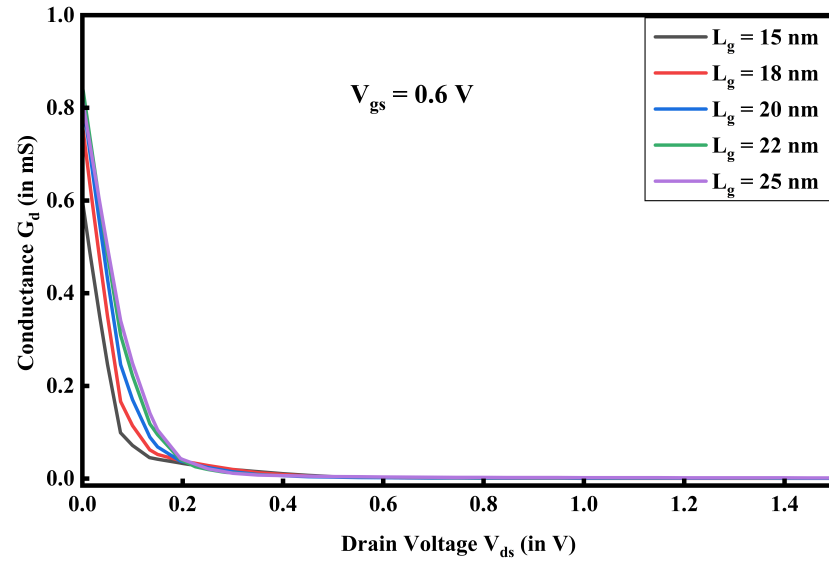


Figure 4.9: Output conductance g_d versus V_{gs} at $V_{ds} = 0.6$ V for five gate lengths.

The favourable A_v trend is the direct analog-performance benefit of the TMG architecture beyond its SCE-suppression role. The Co source-side segment, which produces the DIBL suppression also pins the source-side potential against drain-bias variation, which contributes to the low g_d . The Ti drain-side segment, with its lower work function, accelerates carriers toward the drain and contributes to the high g_m . The two contributions act on different aspects of the device but combine constructively in the intrinsic voltage gain, an outcome consistent with the spacer-gate synergy observations reported by Sharon and Edward [16] for a different but architecturally related device.

4.6 Summary

The figures of merit of the proposed Ge q-step FinFET with TMG engineering are now consolidated with the main benchmark devices identified in **Chapter 2**. The full comparison can be seen in Table 4.3.

Table 4.3: Performance comparison of the proposed Ge q-step FinFET with TMG engineering against principal benchmark devices.

Reference	Device	Performance highlights
Das et al. [14]	Ge multi-channel FinFET	$V_{th} = 0.249$ V, SS = 85 mV/dec
Saha et al. [5]	Si quadruple-channel FinFET (no TMG)	$V_{th} = 0.31$ V, SS = 109 mV/dec, $I_{ON}/I_{OFF} = 2.96 \times 10^6$
Das et al. [7]	Si TMG step-FinFET	$V_{th} = 0.2426$ V, SS ≈ 69 mV/dec
Shubhda et. al [20]	Si gate-stacked junctionless trigate FinFET	SS = 94 mV/dec, DIBL = 82.63 mV/V
This work	Ge q-step FinFET with TMG (Co/W/Ti)	$V_{th} = 0.271$ V, SS = 61.54 mV/dec, DIBL = 44.11 mV/V, $I_{ON}/I_{OFF} = 8.12 \times 10^4$, $g_{m,max} = 215.8 \mu S$ at $V_{ds} = 0.5$ V

There are four comparisons being mentioned. Each one is because of a different combination of architectural elements.

Of all, the most directly relevant comparison is with Shubhda et. al [20]. Their gate-stacked junctionless trigate FinFET with multi-material work-function engineering had an SS=94 mV/dec and DIBL=82.63 mV/V. At the same scaling, the proposed device shows SS = 61.54 mV/dec and DIBL = 44.11 mV/V, corresponding to the reduction of

34.5% in subthreshold swing and 46.6% in DIBL. The improvement is attributed to four architectural differences: the germanium channel (vs silicon), the step-fin geometry (vs uniform fins), the quadruple-fin parallelism (vs single-fin trigate), and the dual-layer $\text{SiO}_2/\text{HfO}_2$ dielectric (vs the gate-stacked configuration). Each of these elements contributes a fraction of the total improvement, with the step-fin geometry and the TMG-Cobalt source pinning contributing the largest individual improvements to SS and DIBL respectively.

The comparison with Das et al. [7] separates the channel-material and multi-fin contributions. Their Si TMG step-FinFET, which has the step-fin geometry, and the triple-material gate engineering in common with the present device, reports SS ≈ 69 mV/dec. The proposed Ge q-step FinFET achieves 61.54 mV/dec, which is a reduction of 10.8 %. The improvement is mainly due to the Ge channel (higher mobility, lower body-factor contribution to SS at low EOT) and the multi-fin coupling at the 12nm pitch (sharper collective subthreshold transition).

The comparison with Saha et al. [5] separates the contribution of TMG engineering other than step-fin geometry and Ge channel. They report SS = 109 mV/dec for their Si quadruple-channel FinFET which shares the multi-fin parallelism with the present device but uses neither TMG nor a step-fin nor a Ge channel. The proposed device exhibits 61.54 mV/dec, which corresponds to a reduction of 43.5%. The improvement is due to the combined effect of all three additional elements that were lacking in the Saha device.

The comparison with Das et al [14] is about the effect of the step-fin geometry and TMG engineering on Ge channels. Their Ge multi-channel FinFET employs Ge channel and multi-fin parallelism similar to the current device but lacks step-fin and TMG, and demonstrates SS = 85 mV/dec at a similar gate length. The proposed device exhibits 61.54 mV/dec at $L_g = 25$ nm, which is 27.6% reduction due to the combined effect of step-fin geometry and TMG architecture.

These four comparisons indicate that no individual architectural component of the proposed device is solely responsible for the performance advantage. The impact of each element is measurable. The combination results in a device whose short-channel

and analog figures of merit are substantially higher than those of any subset of the four design choices. The integrated four-element optimisation of channel material, fin geometry, fin-count and gate engineering thus offers a level of electrostatic and analog performance that the existing literature has approached only with multiple, mutually-exclusive, design strategies.

In **Chapter 5**, the additional architectural modification of the designed device using stepped-spacer engineering is analysed, together with the consolidated conclusions of the present chapter and the identified directions for future work.

Conclusions and Future Work

This chapter collects the main results of **Chapter 4**, exposes an architectural extension of the proposed device by means of a conformal stepped-spacer envelope implemented at the Sentaurus Structure Editor level, develops a literature-based prediction of the expected benefit, and ends with the limitations of the present work and the identified future research directions.

5.1 Summary of the TMG Engineering Results

There are three key findings from the simulation results of **Chapter 4** at $L_g = 25$ nm. The subthreshold swing reaches 61.54 mV/dec, only 1.54 mV/dec from the room-temperature thermal limit. DIBL extracts to 44.11 mV/V, a 46.6% reduction w.r.t to the nearest research-lineage benchmark of Shubhda et. al [20]. Peak transconductance is 215.8 μ S at $V_{ds} = 0.5$ V and 219.0 μ S at $V_{ds} = 1.0$ V. Each of these three results can be attributed to a different architectural element. The high gate-channel capacitance that underpins the near-thermal-limit SS is provided by the dual-layer SiO₂/HfO₂ dielectric. Low DIBL is the result of the source side TMG segment of Cobalt pinning the source channel barrier. The mobility advantage undercuts the high transconductance from the germanium channel. No single element can reach this performance level and the four element combined design outperforms the performance achieved in the previous work with mutually exclusive strategies.

5.2 Spacer Extension

The TMG architecture acts on the gate footprint via the work-function gradient along the channel. Further improvement is achievable by acting on the spacer interface between gate and source/drain through fringe-induced barrier lowering, an effect shaped by the spacer dielectric profile [21, 22]. This section describes the architectural integration of a

conformal stepped-spacer envelope into the proposed device at the Sentaurus Structure Editor level. The main future work direction is the full electrical characterization.

5.2.1 Design Basis and Conformal Shell Geometry

The stepped-spacer literature is bifurcated along two approaches. Zareiee et. al [25] proposed decreasing vertical heights of $\text{HfO}_2/\text{Si}_3\text{N}_4/\text{HfO}_2$ layers on a silicon junctionless device. Daniel et al. [1] have characterized single and dual- κ materials on a junctionless comb-shaped nanosheet and found TiO_2 as the high-performance candidate. The extension proposed here is a combination of both as a 3-D conformal envelope wrapping each step-fin with a coordinated height step and thickness step decreasing from the gate edge outward. This is called the S^3 -spacer configuration.

The base device geometry is as per **Chapter 3** with one modification, $L_g = 15$ nm and total device length 45 nm to meet the needs of the lateral spacer footprint. The fin pitch stays 12 nm and the stepped fin keeps its 6 nm lower section (6 nm width) and 4 nm upper section (4 nm width). The spacer envelope is composed of three conformal shells stacked laterally outward from the gate edge:

- **Inner HfO_2 :** conformal thickness 3 nm in Y and Z , vertical extent 13 nm above the box
- **Middle Si_3N_4 :** thickness 2 nm, vertical length 12 nm.
- **Outer HfO_2 :** thickness 1 nm, vertical extent 11 nm

The three shells extend 6.0 nm laterally. The decreasing thickness and decreasing height produce a coordinated step in two dimensions. The inner HfO_2 , with its largest cross-section, maximises the FIBL at the gate edge. The outer HfO_2 with its smallest cross-section screens drain-side parasitic fringing. The Si_3N_4 buffer alleviates the interface stress and constrains the spatial extent of the high- κ regions as argued by Zareiee et al. [25].

5.2.2 Implementing SDE

The implementation uses the default Boolean engine (BAB mode) to cleanly resolve the dielectric boundaries. First, the BOX layer, SOI substrate and four stepped germanium fins are defined at the 12nm pitch. Dielectric blocks for the three spacer layers are then built as bounding rectangles around the fin array, with extents matching the 3/2/1 nm thicknesses and 13/12/11 nm heights. The Boolean engine then sequentially subtracts the fin geometry from each block, yielding conformal shells with cleanly resolved interfaces.

A geometric consequence of the 12 nm fin pitch and the 3 nm inner-shell thickness deserves explicit mention. The inner HfO_2 layers of adjacent fins meet exactly at the midpoint of the trench, without any gap or overlap. The merged inner HfO_2 from the two neighboring fins fully occupies the 6-nm inter-fin spacing, and the structure is mechanically self-contained without any extra fill material.

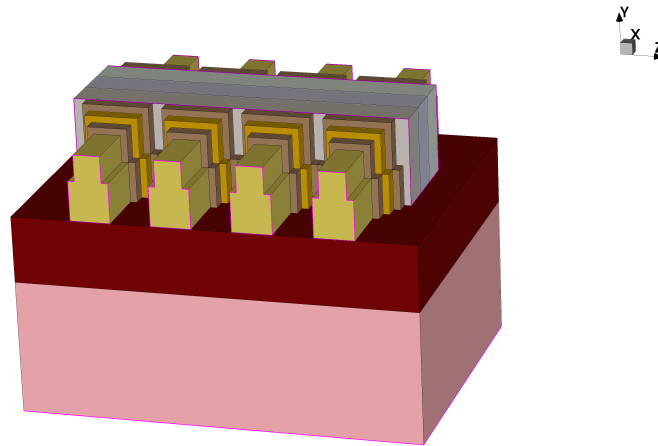


Figure 5.1: Three-dimensional Sentaurus Structure Editor view of the proposed device with the S^3 -spacer architecture: four stepped germanium fins on the BOX layer, the conformal $\text{HfO}_2/\text{Si}_3\text{N}_4/\text{HfO}_2$ envelope, and the TMG (Co/W/Ti) stack at the top.

Figures 5.1–5.4 confirm the geometric integrity of the construction. The four fins enclosed by the conformal envelope are depicted in the three-dimensional realisation of Figure 5.1. Figure 5.2 shows a cross-section in which the inner shells cleanly meet at the middle of the trench. The side view shown in Figure 5.3 confirms the descending

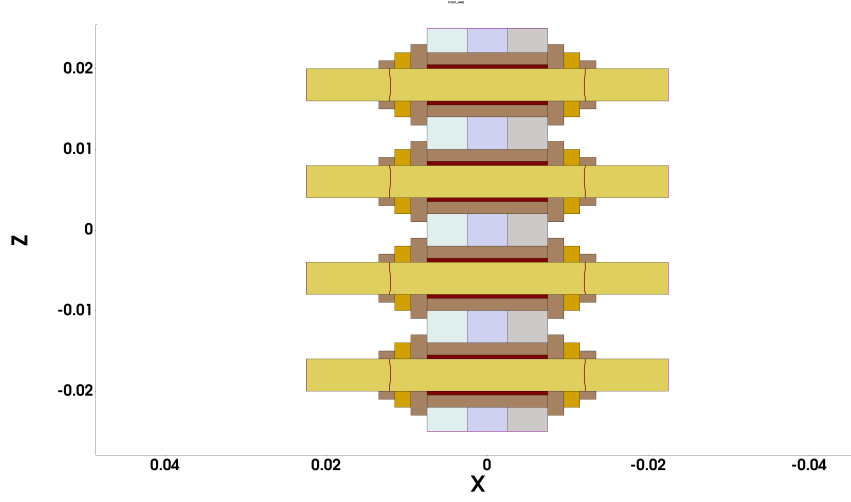


Figure 5.2: Cross-section through the S^3 -spacer architecture in the X - Z plane. The inner HfO_2 from adjacent fins meets cleanly at the trench midpoints.

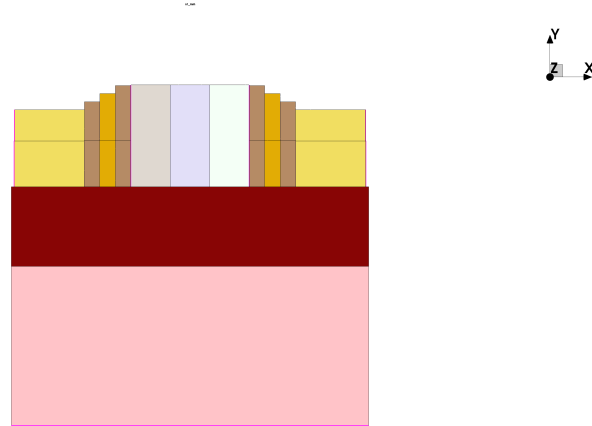


Figure 5.3: Side view in the X - Y plane. The TMG gate stack (three vertical bands corresponding to Co, W, Ti) sits at the centre; on each side, the three spacer shells descend in a staircase from 13 nm through 12 nm to 11 nm.

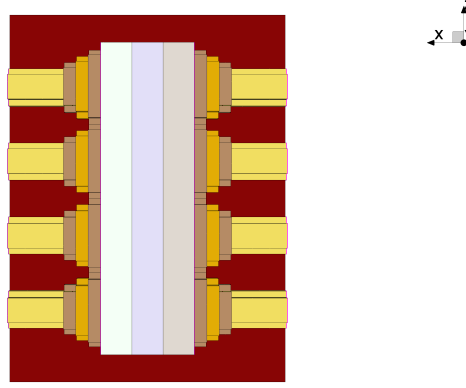


Figure 5.4: Top-down view showing the TMG gate strip running uniformly across all four stepped fins, with the conformal envelope symmetrically present on both sides.

staircase profile on both sides of the TMG stack. The plan view in Figure 5.4 confirms that all four fins are uniformly covered.

5.3 Literature Based Performance Prediction

The architectural extension has been implemented at the structural level, but it has not been electrically characterized in the present work. Three mechanisms are expected to contribute to the performance improvement. The inner high- κ HfO₂ enhances the FIBL at the source-side gate edge. The outer thin HfO₂ screens the drain-side fringing and thus provides an additional DIBL reduction to the TMG source-side pinning [25]. The Si₃N₄ buffer suppresses the parasitic gate-drain capacitance and preserves the high-frequency performance [16, 28].

A related configurations in the literature gives a bounded quantitative estimate. For the Zareiee S^3 -FinFET [25] data, we see an additional SS improvement of 2 to 5 mV/dec and an additional DIBL reduction of 5 to 15 mV/V over the baseline in **Chapter 4**. The dual- κ results of Daniel et al. [1] achieve improvements in switching ratio of half an order to one order of magnitude. Mathew et al. [24] and Kumar et al. [26] report improvements in the transconductance in the range of 5 to 15%. The predictions are given as ranges to show the proper epistemic caution. The main item of future work is direct quantification by electrical simulation.

5.4 Limitations of This work

It should be pointed out that there are four limitations. The limitation of this study is the TCAD simulation only without experimental measurement. The spacer-extended device is realized at the structural level only, whereas the corresponding electrical simulation campaign is postponed to future work. The analysis is fixed at 300 K ignoring the quantified temperature dependence for Ge multi-channel FinFETs by Das et al. [14]. We do not consider work-function variability due to grain-orientation effects [6] and assume all metal segments to be ideal.

5.5 Concluding Remarks

This work points to five next steps, in order of priority.

- Running the full electrical simulation of the spacer-extended device across the same five gate lengths from **Chapter 4** will show how much the spacer improves performance and confirm the predictions in Section 5.3.
- Testing different combinations of the 3/2/1 nm shell thicknesses and 13/12/11 nm heights, keeping the total spacer width at 6 nm, will find the best configuration. Daniel et al. [1] point to the inner-layer thickness as the key variable.
- Daniel et al. [1] report that TiO_2 ($\kappa \approx 80$) performs considerably better than HfO_2 ($\kappa \approx 22$) as a spacer material. Swapping the inner HfO_2 shell for TiO_2 , while keeping the same stepped geometry, is the next logical test.
- Running AC simulations and extracting f_T , $f_{\max}$, noise figure, and linearity metrics would show whether the device is suitable for analog and RF use. Sharon et al. [16] have done this for a closely related device.
- Building even a basic test structure would provide a real reference point against which the TCAD predictions of **Chapter 4** are checked. Section 3.4 lists the main fabrication challenges.

5.6 Discussion

The dissertation proposed a quadruple channel germanium step-FinFET with triple-material gate engineering, electrically characterised it over a five-point gate-length sweep and demonstrated an architectural extension via a conformal stepped-spacer envelope implemented at the SDE level. The device integrates four design strategies into a single structure, each one addressing a different physical mechanism. The device shows 34.5% improvement over the closest research-lineage benchmark in SS and 46.6% in DIBL at $L_g = 25$ nm. The S^3 -spacer envelope shows a coordinated height and thickness step not reported before in the conformal three dimensional form employed here. The next step of the current work is the full simulation of the spacer-extended device.

Bibliography

- [1] T. Daniel, S. Angel, S. Valasa, V. R. Kotha, S. Bhukya, N. Malishetty, and N. Vadthiya, “Engineering the spacer for junctionless comb-shaped nanosheet FETs at sub-5 nm node: Device to circuit realization,” *Micro and Nanostructures*, vol. 216, p. 208723, 2026.
- [2] M. N. Reddy and D. K. Panda, “A comprehensive review on FinFET in terms of its device structure and performance matrices,” *Silicon*, vol. 14, pp. 12 015–12 030, 2022.
- [3] R. R. Das, T. R. Rajalekshmi, and A. James, “FinFET to GAA MBCFET: A review and insights,” *IEEE Access*, vol. 12, pp. 50 556–50 577, 2024.
- [4] C. hu, S. Tam, F.-C. Hsu, P.-K. Ko, T.-Y. Chan, and K. Terrill, “Hot-electron-induced mosfet degradation—model, monitor, and improvement,” *Electron Devices, IEEE Transactions on*, vol. 32, pp. 375– 385, 03 1985.
- [5] R. Saha, P. Devi, S. Barman, R. Prasad, U. P. Singh, and S. K. Maity, “Optimized multi-channel FinFET for enhanced device and circuit performance: a numerical simulation-based study,” *Analog Integrated Circuits and Signal Processing*, vol. 126, no. 2, 2026.
- [6] R. Saha, B. Bhowmick, and S. Baishya, “Si and ge step-FinFETs: Work function variability, optimization and electrical parameters,” *Superlattices and Microstructures*, vol. 107, pp. 5–16, 2017.
- [7] R. R. Das, A. Chowdhury, A. Chakraborty, and S. Maity, “Impact of stress effect on triple material gate step-FinFET with DC and AC analysis,” *Microsystem Technologies*, vol. 26, no. 6, pp. 1813–1821, 2020.
- [8] R. R. Das and A. James, “Multi-channel step FinFET with spacer engineering,” *IEEE Access*, vol. 12, pp. 462–470, 2024.

-
- [9] F. Daugé, L. Davi, K. Rochereau, and E. Josse, “Coupling effects and channels separation in FinFETs,” in *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2004.
- [10] Archana, M. Verma, and D. Vaithiyanathan, “Investigation of FinFET with multi-channel structures on device characteristics,” in *IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)*, 2024, pp. 1–6.
- [11] Y. Hirpara and R. Saha, “Analysis on DC and RF/analog performance in multifin-FinFET for wide variation in work function of metal gate,” *Silicon*, 2021.
- [12] V. Thirunavukkarasu, J. Lee, T. Sadi, V. P. Georgiev *et al.*, “Investigation of inversion, accumulation and junctionless mode bulk germanium FinFETs,” *Superlattices and Microstructures*, vol. 111, pp. 649–655, 2017.
- [13] M. Bansal and H. Kaur, “Analysis of negative-capacitance germanium FinFET with the presence of fixed trap charges,” *IEEE Transactions on Electron Devices*, vol. 66, no. 4, pp. 1979–1984, 2019.
- [14] R. R. Das, S. Maity, A. Chowdhury, and A. Chakraborty, “Impact of temperature on radio frequency/linearity and harmonic distortion characteristics of Ge multi-channel fin shaped field-effect transistor,” *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 32, no. 2, 2022.
- [15] P. Vimala and T. S. A. Samuel, “TCAD simulation study of single-, double-, and triple-material gate engineered trigate FinFETs,” *Semiconductors*, vol. 54, no. 4, pp. 501–505, 2020.
- [16] R. L. Sharon and A. S. Edward, “Spacer-gate synergy in tri-material FinFETs: Performance analysis for RF/analog applications,” *Journal of Electronic Materials*, 2026.
- [17] S. Sunani, S. S. Mahato, K. Jena, and R. Swain, “Comparative analysis of single and triple material 10 nm tri-gate FinFET,” *Journal of the Korean Physical Society*, vol. 85, no. 9, pp. 737–745, 2024.

-
- [18] Synopsys Inc., “Sentaurus device user guide,” Synopsys Inc., Mountain View, CA, USA, Tech. Rep., 2017, version L-2017.09 and successor releases.
- [19] M. S. Badran, H. H. Issa, S. M. Eisa, and H. F. Ragai, “Low leakage current symmetrical dual-k 7 nm trigate bulk underlap FinFET for ultra low power applications,” *IEEE Access*, vol. 7, pp. 17 256–17 262, 2019.
- [20] Shubhda and R. Chaujar, “Performance assessment of gate-stacked junctionless trigate FinFET with multi-material work function engineering,” in *2025 13th International Conference on Intelligent Embedded, MicroElectronics, Communication and Optical Networks (IEMECON)*. IEEE, 2025, pp. 1–5.
- [21] A. Chattopadhyay, A. Dasgupta, R. Das, A. Kundu, and C. K. Sarkar, “Effect of spacer dielectric engineering on asymmetric source underlapped double gate MOSFET using gate stack,” *Superlattices and Microstructures*, vol. 101, pp. 87–95, 2017.
- [22] K. P. Pradhan *et al.*, “Exploration of symmetric high-k spacer hybrid FinFET for high performance application,” *Superlattices and Microstructures*, vol. 90, pp. 191–197, 2016.
- [23] S. Gupta and A. Nandi, “Effect of air spacer in underlap GAA nanowire: An analogue/RF perspective,” *IET Circuits, Devices and Systems*, vol. 13, no. 8, pp. 1196–1202, 2019.
- [24] S. Mathew, Nithin, and R. Rao, “Investigations on the effect of spacer dielectrics on the DC characteristics of dual material gate junctionless FinFETs,” in *International Conference on Computational Performance Evaluation (ComPE)*, 2020, pp. 359–361.
- [25] M. Zareiee, M. Mehrad, and A. Tawfik, “A stepped-spacer FinFET design for enhanced device performance in FPGA applications,” *Micromachines*, vol. 16, no. 8, p. 867, 2025.

- [26] B. Kumar, M. Sharma, and R. Chaujar, “Dual-k spacer JAM-GS-GAA FinFET: A device for low power analog applications,” in *IEEE Silchar Subsection Conference (SILCON)*, 2022, pp. 1–6.
- [27] J. Patel, N. Bagga, S. Dasgupta, and S. Banchhor, “Symmetric/asymmetric spacer optimization for multi fin FinFET: Analog perspective for high-frequency operation,” in *IEEE International Conference on Emerging Electronics (ICEE)*, 2022, pp. 1–6.
- [28] V. B. Sreenivasulu, S. Bhandari, M. Prasad *et al.*, “Spacer engineering on multi-channel FinFET for advanced wireless applications,” *International Journal of Electronics and Communications (AEÜ)*, vol. 178, p. 155298, 2024.
- [29] J. Song, Y. Yuan, B. Yu, W. Xiong, and Y. Taur, “Compact modeling of experimental n- and p-channel finfets,” *IEEE Transactions on Electron Devices*, vol. 57, no. 6, pp. 1369–1374, 2010.
- [30] Anshul and R. Chaujar, “Towards extended hückel model-based reliability performance enhancement of gate stack graphene nanoribbon field effect transistor,” *Microelectronics Reliability*, vol. 173, 2025.
- [31] R. Mann and R. Chaujar, “Tcad investigation of ferroelectric based substrate mosfet for digital application,” *Silicon*, vol. 14, no. 9, pp. 5075–5084, 2022.

TCAD-Based Performance Optimization of Quadruple-Channel Germanium Step-FinFETs with Tri-Material Gate Engineering

Kislay Kumar

Department of Applied Physics
Delhi Technological University
Delhi, India
kkumarjvm@gmail.com

Rishu Chaujar

Vinod Dham Centre of Excellence (VDSemiX)
for Semiconductors and Microelectronics
Department of Applied Physics
Delhi Technological University
Delhi, India
chaujar.rishu@dtu.ac.in

Abstract—This work presents a TCAD-based investigation of a quadruple-channel Germanium (Ge) step Fin Field-Effect Transistor (Ge q-step FinFET) with Triple Material Gate (TMG) engineering using Sentaurus TCAD. Four stepped Ge fins are integrated on a Silicon-on-Insulator (SOI) substrate with a Silicon Dioxide (SiO₂)/Hafnium Oxide (HfO₂) gate dielectric stack, yielding an Equivalent Oxide Thickness (EOT) of approximately 0.589 nm. A triple material gate consisting of Cobalt, Tungsten, and Titanium, with work functions of 4.7 eV, 4.4 eV, and 4.33 eV respectively, is implemented across five gate lengths ranging from 15 to 25 nm to effectively modulate the channel electric field. At 25 nm gate length, the device achieves a subthreshold swing (SS) of 61.54 mV/dec, Drain-Induced Barrier Lowering (DIBL) of 44.11 mV/V, and I_{ON}/I_{OFF} of 8.12×10^4 , showing approximately 34.5% and 46.6% improvement in SS and DIBL over reported structures, establishing its viability for low-power Complementary Metal-Oxide-Semiconductor (CMOS) applications.

Index Terms—FinFET, Germanium (Ge), Triple Material Gate (TMG), Short-Channel Effects, Subthreshold Swing, TCAD Simulation

I. INTRODUCTION

Gordon Moore observed in 1965 that transistor count on an integrated circuit roughly doubles every two years, and this trend has guided the semiconductor industry for over five decades [1]. To follow this, Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) dimensions have been scaled for higher speed, packing density, and lower power. When gate lengths entered the deep nanometer range, short-channel effects (SCEs) like drain-induced barrier lowering (DIBL), threshold voltage roll-off, and growing subthreshold leakage, have made it difficult for a single planar gate to control the channel [2].

Non-planar multi-gate architecture like the FinFET uses a thin vertical silicon fin as the channel, with the gate covering three sides of it for much stronger control than planar devices and double-gate (DG), triple-gate (TG), and gate-all-around (GAA) designs have also been explored [1,2]. When built on a SOI substrate, the buried oxide underneath the fin cuts off parasitic leakage to the bulk.

If we consider the channel material itself, Silicon has been the standard for decades but Germanium (Ge) with its lower bandgap (~ 0.66 eV) and naturally higher electron and hole mobility is able to provide higher drive currents at lower voltages. In 2017, Saha et al. proposed a step-FinFET structure using both Si and Ge as the channel materials and compared their device metrics [3]. Their study showed that Ge step-FinFET has better I_{on}/I_{off} ratio with lower intrinsic delay, while Si showed more resistance to threshold voltage roll-off. Ge has come out ahead in terms of performance, which makes it an attractive choice for high-speed nodes.

Another option to raise drive current without increasing the footprint is the multi-fin or multi-channel architecture, where several fins are placed in parallel between source and drain. This leads to an increased effective channel width and improved transconductance and gate-to-channel coupling [4-6].

Another key consideration is the gate dielectric. At these dimensions a single SiO₂ layer would have a large tunneling leakage, and therefore a thin interfacial SiO₂ layer with a high- κ dielectric such as HfO₂ allows the EOT to be scaled aggressively whilst the physical thickness remains large enough to block direct tunnelling. This dual-dielectric approach has been recently employed in FinFET studies [2,7]. The TMG engineering is to divide the gate into three segments on the gate metal side with increasing work functions. The source-channel barrier is preserved by the high work function metal nearby and the graded profile customizes the electric field and enhances the carrier velocity [8-10].

In this paper, we bring these design strategies together and investigate a quadruple-channel Ge step-FinFET with TMG engineering. The device structure has been designed and simulated in Sentaurus TCAD from Synopsys Inc. [11]. L_g values of 15, 18, 20, 22, and 25 nm are studied, and figures of merit such as V_{th} , SS, transconductance (g_m), output conductance (g_d), and switching ratio (I_{ON}/I_{OFF}) are extracted and analyzed. The paper is organized as: Section I is Introduction, Section II covers device architecture, simulation

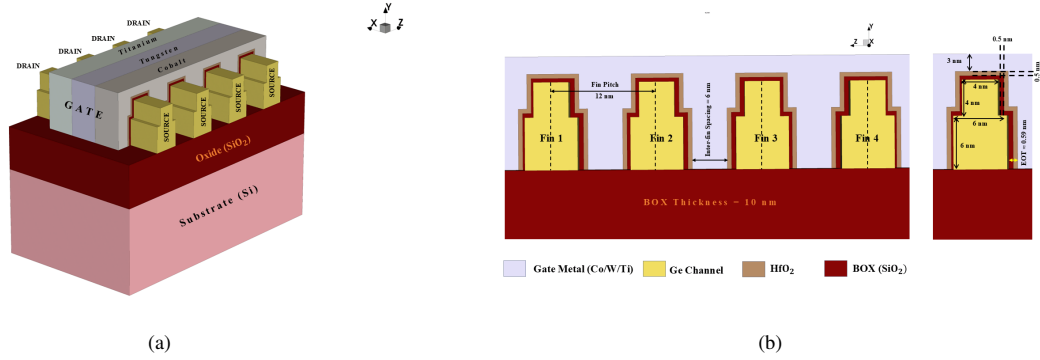


Fig. 1: (a) 3D schematic of the proposed Ge q-step FinFET structure. (b) 2D cross-sectional view showing detailed fin geometry and device dimensions.

setup, and fabrication feasibility, Section III has results and discussion, and Section IV gives the conclusion.

II. DEVICE CONFIGURATION AND SIMULATION SETUP

A. Device Architecture

The proposed quadruple-channel Germanium step-FinFET (Ge q-step FinFET) is designed using the Sentaurus Structure Editor (SDE) and its three-dimensional structure is presented in Fig. 1(a), while the two-dimensional cross-section with the detailed dimensions of the four fins are shown in Fig. 1(b). The proposed structure has four parallel stepped Germanium fins on top of a 10 nm thick Buried Oxide (BOX) substrate, utilising the SOI technology.

The step-FinFET structure involves a non-uniform fin geometry for different fin heights and widths at the upper and lower sections. The lower section of the fin has a height of 6 nm and a width of 6 nm, whereas the upper section has a height of 4 nm and a width of 4 nm, resulting a total fin height of 10 nm. The fin pitch is fixed at 12 nm in this multiple channel design, resulting in an inter-fin spacing of 6 nm. The specific dimensions for a single fin were adopted from the optimized structure parameters reported by Das et al. [4], as this geometry has been demonstrated to provide an ideal balance between reduced series resistance and suppressed short-channel leakage.

The total device length is fixed to 35 nm. Within this footprint the source and drain regions are kept at a constant length of 10 nm respectively. The effect of the variation of the gate length (L_g) is isolated by fixing the source drain regions in the simulation. The gate stack has been designed with a dual-layer dielectric comprising an interfacial Silicon Dioxide (SiO₂) layer (0.5 nm) with a relative permittivity (ϵ_{r1}) of 3.9 and a high-k Hafnium Oxide (HfO₂) layer (0.5 nm) with a relative permittivity (ϵ_{r2}) of 22. This configuration uses a larger physical thickness to reduce the gate direct tunneling leakage and at the same time keeps a high gate-to-channel

capacitance [9]. The Equivalent Oxide Thickness (EOT) of the dual- κ stack is expressed as:

$$\text{EOT} = t_{\text{SiO}_2} + t_{\text{HfO}_2} \times \left(\frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{HfO}_2}} \right) \approx 0.589 \text{ nm} \quad (1)$$

A Triple Material Gate (TMG) structure is fabricated and divided into three same-length segments: Cobalt (Co) ($\phi = 4.7$ eV), Tungsten (W) ($\phi = 4.4$ eV), and Titanium (Ti) ($\phi = 4.33$ eV) [7,9]. The high work function Cobalt at the source pins the source to channel barrier height even with increasing V_{ds} and suppresses DIBL. The decreasing work function profile towards the drain creates a step like surface potential that accelerates the injected carriers improving the transconductance (g_m) and the carrier velocity [8,10]. Thanks to the narrow bandgap (~ 0.66 eV) and the inherently higher electron and hole mobility than Si counterparts [3], the graded-field profile translates directly into a higher ON current at lower supply voltages for Ge channel. The channel region is doped with Boron impurities with a low doping concentration of 10^{17} cm^{-3} for reducing the impurity scattering. The source and drain regions are doped with Arsenic impurities with a peak doping concentration of 10^{21} cm^{-3} . The smooth realistic junction transition is simulated with a Gaussian doping profile with a decay depth of 2.5 nm.

B. Simulation Methodology and Fabrication Feasibility

The Sentaurus Device simulator is used to conduct the numerical simulations. The carrier transport model is achieved using Fermi-Dirac statistics alongside the drift-diffusion framework to account for the heavily doped regions. The OldSlotboom model is included to accurately consider the effective intrinsic density and bandgap narrowing variations [4,11].

The narrow Ge bandgap ($E_g \approx 0.66$ eV) makes Auger recombination the dominant mechanism for carrier lifetimes at high injection levels. Defect-assisted processes are captured via the Shockley-Read-Hall (SRH) model with Hurkx field enhancement.

Some advanced mobility models are also activated to reflect real-world transport degradation. The Lombardi (Enormal) model is incorporated to address transverse-field surface roughness scattering, while the Masetti model captures doping-dependent mobility degradation [4,5]. High-field velocity saturation is also accounted for to reflect carrier velocity limits in nanoscale dimensions. Furthermore, Band-to-Band Tunnelling (BTBT) using the Hurkx model is incorporated to accurately predict tunnelling-induced off-state leakage at the scaled drain-to-channel junctions [11]. The comprehensive structural dimensions and physical parameters utilized in this device simulation are tabulated in Table I.

The proposed structure is compatible with current CMOS-process flows. Following the multi-FinFET route in [4,5], fabrication on SOI wafers can be achieved using deep-UV/EUV photolithography and reactive-ion etching (RIE). The stepped fin is defined by a two-stage etch sequence via sidewall image transfer. The $\text{SiO}_2/\text{HfO}_2$ stack is deposited by Atomic Layer Deposition (ALD) for sub-nm EOT control [5] and the three TMG segments (Co/W/Ti) are realized through sequential metal deposition and selective patterning [8,10]. Remaining key scalability challenges are defect free Ge-on-Si heteroepitaxy, fin-width tolerance below 5 nm where source resistance degrades g_m [5] and metal-gate work-function variability due to polycrystalline grain orientations [3]. The proposed fabrication flow is depicted in Fig. 2.

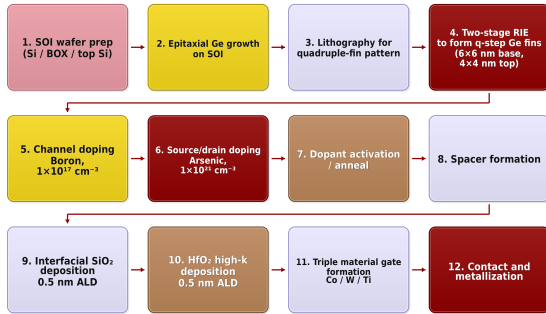


Fig. 2: Proposed fabrication process flow for the Ge q-step FinFET with $\text{SiO}_2/\text{HfO}_2$ gate dielectric stack and triple material gate (Co/W/Ti) on SOI substrate.

III. RESULTS AND DISCUSSION

A. Transfer and Output Characteristics

The transfer characteristics of the Ge q-step FinFET are depicted in Fig. 3(a) and (b). Fig. 3(a) shows the I_d - V_{gs} curves in linear and logarithmic scale for $V_{ds} = 0.05, 0.1, 0.2, 0.5, 0.7$ and 1.0 V at $L_g = 25$ nm. The drain current increases gradually with V_{gs} , with I_{OFF} remaining between 1.6×10^{-9} and 2.1×10^{-9} A while I_{ON} rises from 7.6×10^{-5} to 12×10^{-5} A as V_{ds} increases. The close overlap of subthreshold curves at different V_{ds} confirms minimal DIBL and strong electrostatic integrity [10]. The high I_{ON}/I_{OFF} ratio originates from the narrow Ge

TABLE I: Different simulation parameters for the Ge q-step FinFET and their dimensions.

Parameter	Value / Property
Total Device Length	35 nm
Gate Length (L_g)	15, 18, 20, 22 & 25 nm
Source/Drain Length	10 nm
Fin Height	6 nm (Base) / 4 nm (Tip)
Fin Width	6 nm (Base) / 4 nm (Tip)
Interfacial Oxide	0.5 nm
High-k Dielectric EOT	0.5 nm
Channel Material	Germanium
Channel Doping	$1 \times 10^{17} \text{ cm}^{-3}$ (Boron)
S/D Doping	$1 \times 10^{21} \text{ cm}^{-3}$ (Arsenic)
Junction Steepness	0.8 (Gaussian Factor)

bandgap (~ 0.66 eV) and high carrier mobility, which boost carrier velocity in the channel without elevating leakage [3].

Fig. 3(b) is presenting the drain characteristics with the L_g values of 15 nm, 18 nm, 20 nm, 22 nm and 25 nm, with a fixed drain voltage of $V_{ds} = 0.5$ V. A clear trend is observed, as the L_g increases, the ON current (I_{ON}) also increases proportionally while the OFF current (I_{OFF}) decreases, which can be attributed to a decrease in leakage current (at $V_{gs} = 0$ V) and enhanced gate control [4].

Fig. 4(a) shows the output characteristics at $L_g = 25$ nm, where the drain current reaches higher values with increasing V_{ds} for $V_{gs} = 0.4, 0.6, 0.8, 1.0$ and 1.2 V, confirming the strong gate control and channel conduction. The device operates in the linear region at low V_{ds} and saturates at higher V_{ds} , showing proper channel pinch-off and velocity saturation. The well separated curves at different V_{gs} and the high drive current at large V_{gs} suggest strong electrostatic control [10]. Fig. 4(b) shows the output characteristics at $V_{GS} = 0.6$ V for varying L_g . As L_g increases, the drain influence on the channel weakens, leading to improved gate control, a more stable inversion layer, and higher drain current. Conversely, shorter L_g exhibits SCE-induced degradation of electrostatic control, reducing I_d .

B. Analog Performance: Transconductance (g_m) and Output Conductance (g_d)

The transconductance (g_m), $g_m = \partial I_d / \partial V_g$, is an indication of the gain ability of a transistor. Fig. 5(a) shows g_m vs. V_g for $V_{ds} = 0.05, 0.1, 0.2, 0.5, 0.7$ and 1.0 V at $L_g = 25$ nm with $g_m(\max) = 173.7, 199.9, 209.5, 215.8, 217.4$, and $219.0 \mu\text{S}$, respectively. The increase of $g_m(\max)$ with V_{ds} monotonically indicates improvement of channel modulation and carrier transport.

The variation of g_m with $L_g = 15, 18, 20, 22$ and 25 nm is shown in Fig. 5(b) with $g_m(\max)$ of 95.7, 138.7, 170.2, 196.5 and $215.8 \mu\text{S}$, respectively. The increase of g_m with L_g confirms that the electrostatic control is improved for the longer channels. g_m increases initially at low V_g , peaks at strong inversion and decreases at higher V_g due to mobility degradation [12]. The output conductance ($g_d = \partial I_d / \partial V_d$) is plotted in Fig. 5(c) and (d). g_d increases with V_g in the

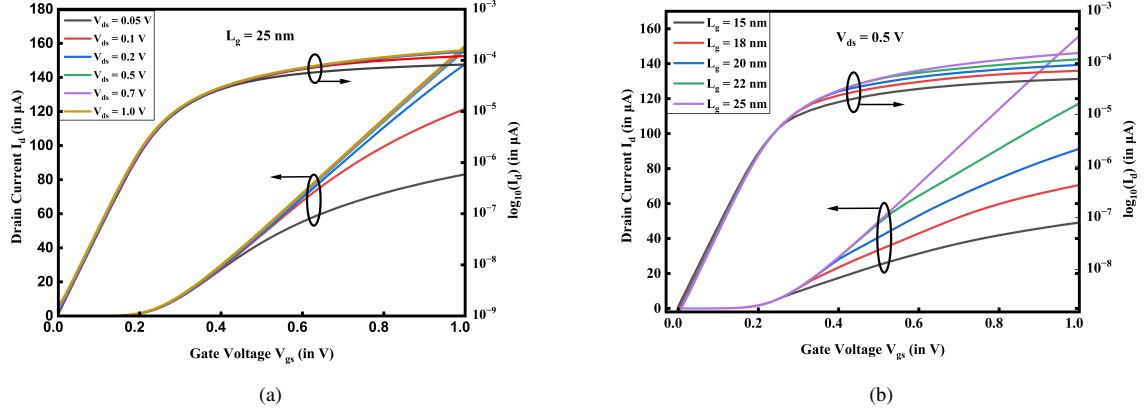


Fig. 3: Transfer characteristics (I_d - V_{gs}) of the Ge q-step FinFET: (a) at $L_g = 25$ nm for different drain voltages (V_{ds}) in linear and logarithmic scale, (b) for different gate lengths at $V_{ds} = 0.5$ V.

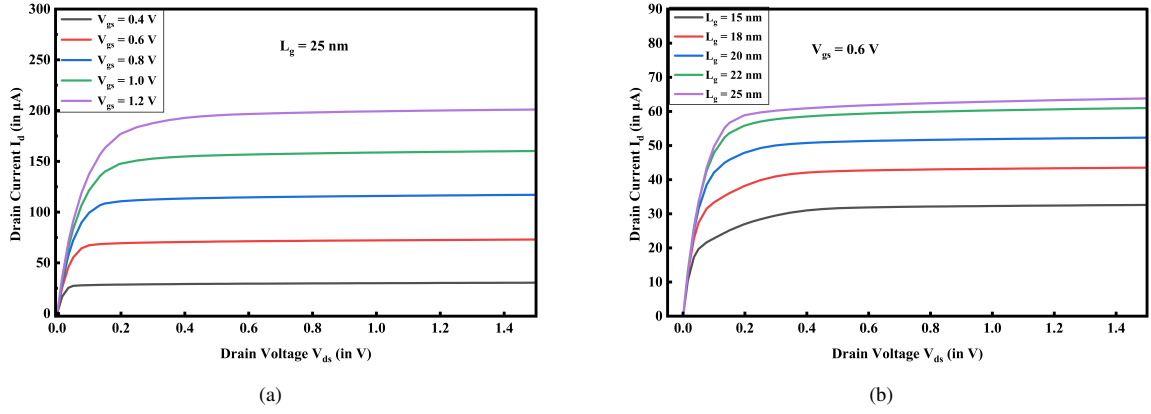


Fig. 4: Output characteristics (I_d - V_{ds}) of the Ge q-step FinFET: (a) at $L_g = 25$ nm for different gate voltages (V_{gs}), (b) for different gate lengths at $V_{GS} = 0.6$ V.

saturation region, reflecting a stronger I_d - V_{ds} dependence; this reduces the output resistance (r_o) and can degrade intrinsic gain [6].

C. Short-Channel Effect (SCE) Analysis

The SCE parameters such as V_{th} , SS, and DIBL play a crucial role in assessing the electrostatic integrity of nanoscale devices. The effective suppression of these parameters is important to address the scaling limitations and maintain reliable device performance [5].

The variation of V_{th} and SS with respect to L_g at a fixed $V_{DS} = 0.5$ V is shown in Fig. 6. It is clearly observed that the V_{th} increases uniformly with increasing gate length, confirming threshold voltage roll-off at shorter gate lengths, which is fundamentally caused by the transition from one-dimensional to two-dimensional electric field patterns in short-

channel devices. With the increase in L_g , the electrostatic control improves and stabilizes the channel potential, hence increasing V_{th} [2].

On the other hand, the SS decreases with increasing L_g and approaches the thermal limit of 60 mV/dec at 300 K, indicating that the gate is exerting near-ideal control over the channel surface potential. Physically, this is enabled by three complementary mechanisms: (i) the $\text{SiO}_2/\text{HfO}_2$ stack maintains a low EOT (~ 0.589 nm) without direct tunnelling leakage, preserving the gate-channel capacitive coupling [7]; (ii) the four parallel stepped fins increase the effective channel width and create mutual electrostatic coupling between adjacent fins, sharpening the subthreshold transition [4]; and (iii) the non-uniform step-fin geometry concentrates the inversion charge in the narrower upper section, where the gate has the strongest control, while the thicker lower section reduces leakage paths

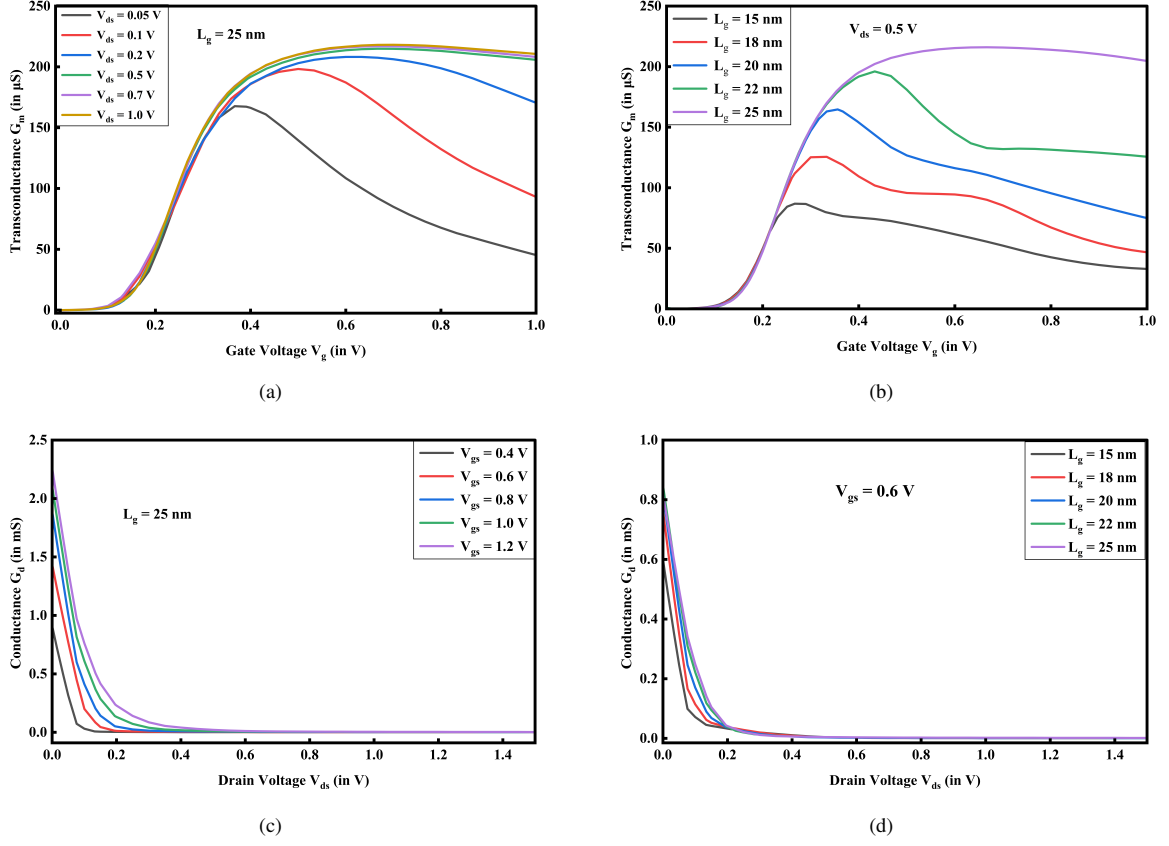


Fig. 5: Variation of transconductance (g_m) with gate voltage: (a) for different V_{ds} at $L_g = 25$ nm, (b) for different gate lengths at $V_{ds} = 0.5$ V. Variation of output conductance (g_d) with gate voltage: (c) for different V_{ds} at $L_g = 25$ nm, (d) for different gate lengths at $V_{ds} = 0.5$ V.

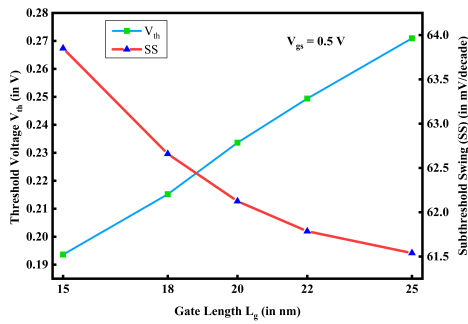


Fig. 6: Variation of V_{th} and SS with L_g at $V_{DS} = 0.5$ V.

to the source/drain [3].

The device parameters such as V_{th} , SS, and I_{ON}/I_{OFF} are

TABLE II: Various figures of merit of the Ge q-step FinFET at different gate lengths (for $V_{DS} = 0.5$ V).

L_g (nm)	15	18	20	22	25
V_{th} (V)	0.194	0.215	0.234	0.249	0.271
I_{ON} (μA)	49.2	70.6	91.4	117.3	156
I_{OFF} (μA)	0.00274	0.00227	0.00208	0.00197	0.00192
I_{ON}/I_{OFF} ($\times 10^4$)	1.80	3.11	4.39	5.96	8.12
SS (mV/dec)	63.85	62.66	62.12	61.79	61.54

extracted at different gate lengths for a fixed $V_{DS} = 0.5$ V to quantitatively evaluate the short-channel behaviour of the proposed Ge q-step FinFET. The extracted values are summarized in Table II.

From Table II, the reduced SCEs are confirmed by the steady increase in V_{th} as the L_g increases from 15 nm to 25 nm. The SS decreases simultaneously and approaches optimal values pointing towards an improved switching behaviour.

TABLE III: Comparative performance summary of reported FinFET devices and proposed work.

Ref.	Device	Parameter Performances
Das <i>et al.</i> [14]	Ge multi-channel FinFET	$V_{th} = 0.249$ V, $SS = 85$ mV/dec, $I_{ON}/I_{OFF} = 9.4 \times 10^{14}$
Shubhda <i>et al.</i> [12]	Gate-stacked junctionless trigate FinFET (Si)	$SS = 94$ mV/dec, $DIBL = 82.63$ mV/V
Das <i>et al.</i> [9]	TMG step FinFET (Si)	$V_{th} = 0.2426$ V, $SS = 69$ mV/dec
Saha <i>et al.</i> [5]	Quadruple-channel FinFET (Si)	$V_{th} = 0.31$ V, $SS = 109$ mV/dec, $I_{ON}/I_{OFF} = 2.96 \times 10^6$
This work	Ge q-step FinFET	$V_{th} = 0.271$ V, $SS = 61.54$ mV/dec, $DIBL = 44.11$ mV/V, $I_{ON}/I_{OFF} = 8.12 \times 10^4$

In addition to this, the I_{ON}/I_{OFF} ratio increases significantly with increasing L_g due to reduced leakage current, exhibiting improved device performance and electrostatic stability.

DIBL is another important parameter used to quantify short-channel effects [13] and is given by:

$$DIBL = \frac{V_{th}(\text{at high } V_{ds}) - V_{th}(\text{at low } V_{ds})}{V_{ds}(\text{high}) - V_{ds}(\text{low})} \quad (2)$$

where $V_{ds}(\text{high}) = 0.7$ V and $V_{ds}(\text{low}) = 0.05$ V in the present study. For the proposed device, the extracted DIBL value is 44.11 mV/V at $L_g = 25$ nm, indicating moderate drain influence and good electrostatic control. The low DIBL is attributed to the high-work-function Co segment near the source, which raises and pins the source-side barrier under increasing V_{ds} , preventing barrier lowering—a mechanism consistent with TMG observations in [8,10].

We compare with reported FinFETs simulated under similar conditions (Sentaurus/Silvaco TCAD, SOI, sub-30 nm L_g) in Table III. The proposed Ge q-step FinFET achieves the lowest SS which is about 10.8% lower than that of Si TMG step-FinFET [9] and about 43.5% lower than that of Si quadruple-channel FinFET [5], and with significantly suppressed DIBL, which proves the combined effect of Ge channel, stepped-fin geometry, TMG engineering and quadruple-fin parallelism can suppress SCEs to a level that can not be achieved by any single feature.

IV. CONCLUSION

A TCAD-based investigation of a quadruple-channel Germanium step-FinFET with TMG engineering was carried out, analyzing transfer/output characteristics and the analog and digital figures of merit V_{th} , SS , g_m , g_d , and I_{ON}/I_{OFF} .

At $L_g = 25$ nm, the proposed device achieves $SS = 61.54$ mV/dec ($\sim 34.5\%$ lower than ~ 94 mV/dec in [12] and $\sim 10.8\%$ lower than the Si TMG step-FinFET [9]) and $DIBL = 44.11$ mV/V ($\sim 46.6\%$ reduction over ~ 82.63 mV/V), together with an I_{ON}/I_{OFF} of 8.12×10^4 . These improvements,

supported by the Ge channel, step-fin geometry, graded-WF TMG, and multi-fin coupling, establish the device as a strong candidate for future low-power, high-performance CMOS applications.

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REFERENCES

- [1] R. R. Das, T. R. Rajalekshmi, and A. James, "Finfet to gaa mbcfet: A review and insights," *IEEE Access*, vol. 12, pp. 50 556–50 577, 2024.
- [2] M. N. Reddy and D. K. Panda, "A comprehensive review on finfet in terms of its device structure and performance matrices," *Silicon*, vol. 14, pp. 12 015–12 030, 2022.
- [3] R. Saha, B. Bhowmick, and S. Baishya, "Si and ge step-finfets: Work function variability, optimization and electrical parameters," *Superlattices and Microstructures*, vol. 107, pp. 5–16, 7 2017.
- [4] R. R. Das and A. James, "Multi-channel step finfet with spacer engineering," *IEEE Access*, vol. 12, pp. 462–470, 2024.
- [5] R. Saha, P. Devi, S. Barman, R. Prasad, U. P. Singh, and S. K. Maity, "Optimized multi-channel finfet for enhanced device and circuit performance: a numerical simulation-based study," *Analog Integrated Circuits and Signal Processing*, vol. 126, 2 2026.
- [6] Y. Hirpara and R. Saha, "Analysis on dc and rf/analog performance in multifin-finfet for wide variation in work function of metal gate," [Online]. Available: <https://doi.org/10.1007/s12633-020-00408-2>
- [7] S. Sunani, S. S. Mahato, K. Jena, and R. Swain, "Comparative analysis of single and triple material 10 nm tri-gate finfet," *Journal of the Korean Physical Society*, vol. 85, pp. 737–745, 11 2024.
- [8] P. Vimala and T. S. A. Samuel, "Tcad simulation study of single-, double-, and triple-material gate engineered trigate finfets," *Semiconductors*, vol. 54, pp. 501–505, 4 2020.
- [9] R. R. Das, A. Chowdhury, A. Chakraborty, and S. Maity, "Impact of stress effect on triple material gate step-finfet with dc and ac analysis," *Microsystem Technologies*, vol. 26, pp. 1813–1821, 6 2020.
- [10] R. L. Sharon and A. S. Edward, "Spacer-gate synergy in tri-material finfets: Performance analysis for rf/analog applications," *Journal of Electronic Materials*, 2026.
- [11] Synopsys and Inc, "Sentaurus™ device user guide," Tech. Rep., 2017. [Online]. Available: <https://www.synopsys.com/company/legal/trademarks-brands.html>.
- [12] Shubhda and R. Chaujar, "Performance assessment of gate-stacked junctionless trigate finfet with multi-material work function engineering," in *2025 13th International Conference on Intelligent Embedded, MicroElectronics, Communication and Optical Networks (IEMECON)*. IEEE, 12 2025, pp. 1–5. [Online]. Available: <https://ieeexplore.ieee.org/document/11365754/>
- [13] Anshul and R. Chaujar, "Towards extended hückel model-based reliability performance enhancement of gate stack graphene nanoribbon field effect transistor," *Microelectronics Reliability*, vol. 173, 10 2025.
- [14] R. R. Das, S. Maity, A. Chowdhury, and A. Chakraborty, "Impact of temperature on radio frequency/linearity and harmonic distortion characteristics of ge multi-channel fin shaped field-effect transistor," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 32, 2 2022.



Kislay Kumar <kkumarjvm@gmail.com>

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