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NOVEL SIGNAL-FEEDTHROUGH FLIP-FLOP OPERATION WITH LOW POWER CONSUMPTION AND HIGH SPEED

A Thesis Submitted
In Partial Fulfillment of The Requirements for The Degree of

MASTER OF TECHNOLOGY

in

VLSI DESIGN AND EMBEDDED SYSTEMS

by

Tushant Verma
(2K23/VLS/14)

Under the supervision of
Dr. Yashna Sharma
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CANDIDATE'S DECLARATION

I, Tushant Verma, Roll No. 2k23/VLS/14, student of M. Tech (VLSI and Embedded Systems), hereby certify that the thesis entitled "Novel Signal-Feedthrough Flip-Flop Operation with Low Power Consumption and High Speed" in partial fulfilment of the requirement for the award of the degree of Master of Technology submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period May 2024 to May 2025 under the supervision of Dr. Yashna Sharma. The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

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Tushant Verma
2k23/VLS/14

ABSTRACT

The paper gives an in-depth analysis of four different pulse-triggered flip-flop (PTFF) architectures, each distinguished by the inclusion of an explicit pulse generation system. The architectures explored are ep-DCOFF, CDFF, SCDFF, and SFTFF, each having various architectural innovations as well as functional advantages. Of particular interest are the inclusion of a conditional discharge method within the CDFF and SCDFF architectures, which successfully overcomes issues of high internal switching activity, output glitches, and input-to-output propagation delays. These enhancements facilitate better energy efficiency and signal integrity in digital circuits. In contrast, the SFTFF presents a new signal feed-through mechanism, which is embedded within a true single-phase clock (TSPC) latch-based architecture. This design feature overcomes the challenge that is inherent with long discharge paths typically found in traditional flip-flop topologies, thus enhancing timing performance as well as power efficiency.

The need for low-power and high-speed flip-flop designs is highlighted by the growing need for low-energy electronic systems, specifically in the face of contemporary VLSI (Very-Large-Scale Integration) design. Power dissipation and signal delay are fundamental measures that have a direct impact on the general performance and scalability of integrated circuits. Therefore, the design of proposed PTFFs is key to improving energy-aware digital design. To measure the performance of the suggested flip-flop designs, the research utilizes rigorous simulation techniques with Cadence design tools at the 90nm CMOS technology node. The comparative study shows that the proposed SFTFF design results in a significant power reduction—about 40% less power compared to its counterparts—in addition to reducing transistor numbers. This decrease not only results in reduced energy consumption but also allows for a more densely packed configuration, which is beneficial for high-density integration. Overall, the article emphasizes the key importance of power and delay optimization within flip-flop design and shows that proposed novel SFTFF structure has great potential for future digital systems with low power and high performance.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

This study introduces new insights that help advance the area of low-power digital circuit design, with a focus on flip-flop architectures. Through meticulous experimentation and analysis, the proposed flip-flop designs demonstrate remarkable reductions in power consumption compared to conventional counterparts, rendering them highly suitable for low power applications [1,2]. The experimental findings hold significant value not only for immediate applications but also as a driving force for further progress in low-power digital circuit design. These insights have practical implications for both optimization and future implementation, making them highly relevant to ongoing research.

The pursuit of performance optimization in digital circuit design necessitates a holistic understanding of the intricate interplay between temperature effects, power consumption, and speed performance [3]. Several experiments are carried out to determine ways to improve flip-flops that work well even if conditions are less ideal while still ensuring that they function fast and are reliable. The findings reveal options for maintaining high performance in high-temperature flip-flops, making low-power, high-speed digital circuits more resilient and dependable.

Innovation in digital circuit design continues to evolve, driven by various methodologies and technologies aimed at pushing the boundaries of efficiency and functionality [4]. One such innovation is the Conditional Discharge Flip-Flop (CDFF), engineered to deliver superior performance metrics while minimizing energy consumption [5]. Through the strategic application of conditional discharge techniques, the CDFF achieves faster switching speeds compared to conventional designs, underscoring its potential to enhance the efficiency and speed of digital circuits across diverse computing applications. The CDFF architecture integrates a dynamic conditional discharge path, a pivotal feature enabling efficient power management during flip-flop operation. Rigorous simulations and comparative analyses validate the CDFF's prowess in terms of speed and power efficiency.

Another notable innovation is the Conditional Feedthrough Pulsed Flip-Flop (CFTPFF), leveraging conditional feedthrough techniques to enhance efficiency and speed performance. By dynamically controlling the feedthrough path, the CFTPFF achieves reduced setup time and faster operation compared to conventional designs. Both simulations and evaluations prove that the CFTPFF performs well, helping it gain recognition as a top option in high-speed digital circuits with less power draw. The PTFF achieves greater power effectiveness than other designs by applying the SFT technique at the flip-flop circuit level. Extensive simulations and evaluations corroborate the effectiveness of the PTFF in reducing power consumption while sustaining performance levels, heralding a new era of low-power digital circuits and offering energy-efficient solutions for diverse computing applications.

Numerous studies have explored innovative approaches to design low-power explicit-type pulse-trigger generator flip-flops, showcasing significant advancements in reducing power consumption while maintaining optimal performance [6,7,8,9]. These efforts address the growing demand for energy efficient solutions in VLSI applications, contributing to the development of sustainable and high-performance integrated circuits.

By leveraging techniques such as dynamic circuit methodologies and signal feed-through mechanisms, researchers have demonstrated notable improvements in reducing power consumption and mitigating delay issues in pulse-triggered flip-flops [6,8]. These innovations optimize power usage and enhance performance, offering promising solutions for high-speed digital systems [9,10].

Clock signals are fundamental in VLSI design, acting as the synchronizing force that enables digital circuits to function in an orderly and predictable manner. Without reliable clocking, the coordination of circuit operations would be compromised. Clock management is essential for maintaining system stability and performance, accounting for a significant portion of total circuit power consumption [11-13]. Pulse generators and flip-flops together form the foundation of precise timing and data storage in modern digital circuits. Specifically, flip-flops are indispensable as memory elements, storing binary information at the heart of sequential logic systems. In such circuits, outputs are determined not just by current inputs, but also by prior states—a property that is essential for anything beyond the most basic digital functions.

1.1 Basic Concept and Terminologies

Combination circuits in digital electronics show output only based on the inputs they have, while sequential circuits also consider past input values when deciding their output. The memory function in sequential circuits depends on flip-flops which allow the circuit to dynamically and flexibly adapt. Because the previous condition helps flip-flops remember data and handle routines, they are needed and used in many kinds of digital equipment and large-scale designs. When designing digital circuits, knowing flip-flops well—what they do, how many there are and how they are used—is key to making the system effective and dependable. Circuits used in digital electronics are generally known as combinational or sequential logic. Combinational circuits produce an output that depends only on the input values taken at that moment. Unlike combinational circuits, sequential circuits have memory, so they can remember their previous states; this affects the outputs they produce. In this framework, flip-flops are indispensable as part of the memory system. Used mainly to preserve binary data, these devices make sequential processing possible in electronics. Being able to recover information is important for many digital systems, including counters, shift registers and finite state machines. In VLSI (Very Large-Scale Integration) design, flip-flops are essential and support the structure of memory and control systems. In digital circuit design, flip-flops are essential since they are the basis for constructing efficient and fault-free circuits. Knowing how flip-flops operate is key for people who want to improve the performance of their designs in multiple areas.

1.1.1. Sequential Logic:

Sequential logic, unlike combinational logic, is defined by its dependence on both current and past inputs. This characteristic is enabled through memory elements—most notably, flip-flops—which allow circuits to store and recall previous states.

It utilizes memory elements, such as flip-flops, to store information about past inputs or states. Sequential circuits are essential in scenarios where the order of inputs matters, such as in counters, shift registers, and state machines.

1.1.2. Latches vs. Flip-Flops:

Latches and flip-flops are included within memory elements that make up sequential logic circuits. A latch is a device that stores information when the enable signal has the selected logic signal (most often high or low). In contrast, flip-flops record data at just a specific period of the clock's signal—when it either increases or decreases.

Flip-flops provide more precise control over the timing of data storage and are found in synchronous sequential logic circuits.

1.1.3. Clock Signals:

The function of sequential logic circuits depends greatly on clock signals. They function as a reference to decide when data can be captured, processed or transferred.

Of all the flip-flops, those triggered by the edges of the clock are precise in their storage of information. Ensuring timing stays reliable and on time is necessary and this is why synchronization is key.

1.1.4. Memory Elements:

Memory elements, with flip-flops as a major example, enable digital systems to retain binary data information, thus allowing them to exhibit dynamic, state-dependent behavior.

The presence of Memory Elements saves previous input data which allows the circuit to be active and maintain previous events.

Flip-flops are a common type of memory element used in sequential logic circuits, providing the ability to store and recall binary data.

1.2 Different types of flip flop

1.2.1. SR Flip-Flop:

The SR (Set-Reset) flip-flop includes only two inputs (S and R) and two outputs (Q and Q'). The S set input and the R reset input are the most common names for these inputs.

When both S and R inputs are low (0), the flip-flop remains in its current state (either set or reset). When the S input is high (1) and the R input is low (0), the Q output is set to high (1), and the Q' output is set to low (0), putting the flip-flop in the "set" state. Conversely, when the R input is high (1) and the S input is low (0), the Q output is reset to low (0), and the Q' output is set to high (1), putting the flip-flop in the "reset" state. Should both S and R signals be high (1), the flip-flop goes into a state that is considered practical and should be avoided.

SR flip-flops can be designed using basic logic gates or more complex sequential logic circuits. Figure 1.1 shows circuit of SR Flipflop with its truth table where Q and Q` represent current output and its negated value respectively.

S	R	Q	Q`
0	0	0	1
0	1	0	1
1	0	1	0
1	1	∞	∞

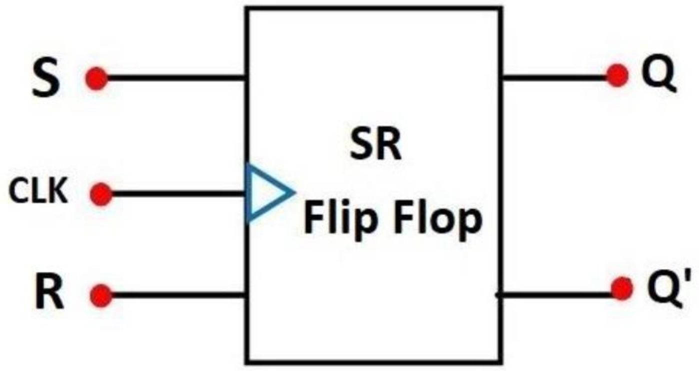

Figure 1.1 SR Flipflop

1.2.2. D Flip-Flop:

The D flip-flop uses a single input for data, a clock input and produces Q and Q'. These D flip-flops change their output after sensing D at the desired edge of the clock, depending on the circuit chosen. When the clock signal transitions from low to high (rising edge), the value of the D input is sampled and stored in the flip-flop. Until the following clock edge, the stored information is the same, at which time the flip-flop records the newly given D input value. Most of the time, data storage and synchronization systems use D flip-flops because they are not complicated and effective at storing and preserving binary data. Figure 1.2 shows circuit of D Flipflop with its truth table where Q and Q` represent current output and its negated value respectively.

D	CLK	Q	Q`
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

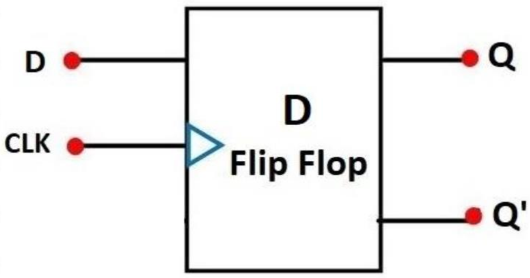

Figure 1.2 D Flipflop

1.2.3. JK Flip-Flop:

The JK flip-flop is a versatile type of flip-flop that combines features of both the SR and D flip-flops.This design uses J and K as inputs, CLK for clock pulses and it generates outputs called Q and Q'. Like the SR flip-flop, the J input plays the part of "set" and K serves as "reset".

However, unlike the SR flip-flop, the JK flip-flop also contains an additional logic to prevent the forbidden state (both J and K inputs high). The behavior of the JK flip-flop is determined by the values of its inputs and the clock signal, allowing it to function as a basic memory element or as a more complex sequential logic element, depending on the application. JK flip-flops are widely used in digital systems for tasks such as frequency division, data storage, and state machine implementation. Figure 1.3 shows circuit of JK Flipflop with its truth table where Q and Q` represent current output and its negated value respectively

C	J	K	Q	Q`
HIGH	0	0	Latch	Latch
HIGH	0	1	0	1
HIGH	1	0	1	0
HIGH	1	1	Toggle	Toggle
LOW	0	0	Latch	Latch
LOW	0	1	Latch	Latch
LOW	1	0	Latch	Latch
LOW	1	1	Latch	Latch

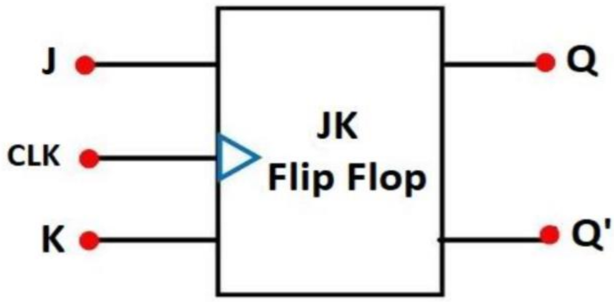

Figure 1.3 JK Flipflop

1.2.4. T Flip-Flop:

The T (Toggle) flip-flop is a specialized type of flip-flop with a single input (T), a clock input (CLK), and two outputs (Q and Q'). The T flip-flop toggles its output state (from high to low or low to high) whenever the value of its T input transitions from low to high (positive edge) while the clock signal is high. When the T input is low, the output state does not change at any clock signal.

T flip-flops are suitable for places where something needs to alternate or switch between two states such as in frequency division circuits, pulse generators and counters. Figure 1.4 shows circuit of T Flipflop with its truth table where Q and Q` represent current output and its negated value respectively

Truth Table of T Flip Flop

T	Q	Q`
0	0	0
1	0	1
0	1	0
1	1	0

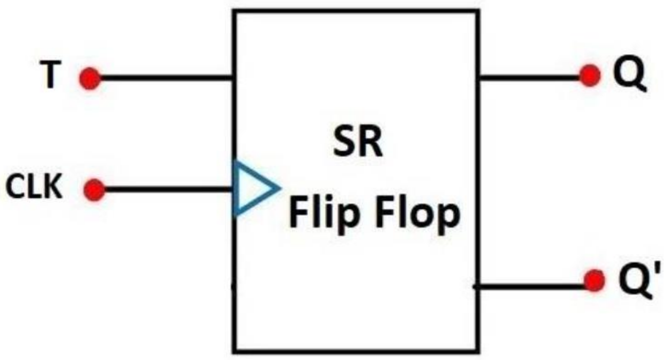

Figure 1.4 T Flipflop

26

1.2.5. Master-Slave Flip-Flop:

94
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These circuits consist of two linked flip-flops: a master flip-flop and a slave flip-flop which are called master-slave flip-flops as shown in figure 1.5. Using these flip-flops in a chain brings better timing and eliminates the issues with race conditions found in unsynchronized single flip-flop designs. The master-slave flip-flop is different from most types in that:

100
- A typical master flip-flop is activated either by the clock signal going high or low. It puts the input values into memory and holds them until the next transition in the clock.

36
34
- A slave flip-flop is set by the change in the clock signal that is the opposite of what triggers the master flip-flop. It takes the output from the master flip-flop and maintains it until the clock's next edge appears.

- The division gives the flip-flop circuit two sequential phases: master phase and slave phase. Separating the data movement in and out helps master-slave flip-flops avoid timing problems and guarantee smooth function in sequential circuits.

12
Reliable and properly timed operation is why master-slave flip-flops are used mostly in applications related to circuits based on clocked signals. They perform and remain stable better than single flip-flop circuits which makes them a good choice for systems that need to run quickly and dependably.

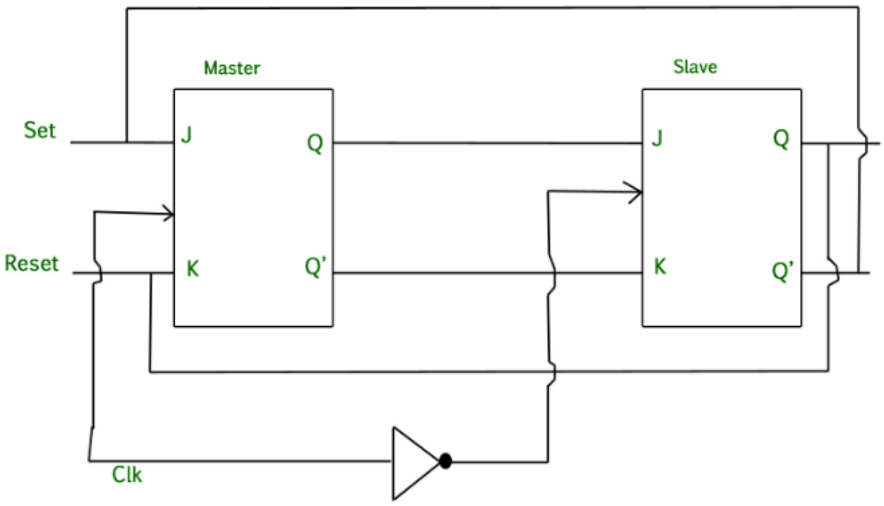

Figure 1.5 Master Slave Flipflop

1.2.6. Edge-Triggered vs. Level-Sensitive Flip-Flops:

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41
12
On the basis of how their signals change, edge-triggered and level-sensitive flip-flop are both distinct forms of flip-flops. Edge-triggered flip-flops capture the state of their input signals (e.g., data, clock) only at specific edges (rising or falling) of the clock signal.

23
The most common type of edge-triggered flip-flop is the D flip-flop, which captures the value of its data input at the rising (or falling) edge of the clock signal. These kinds of flip-flops make it easy to

control timing exactly and consequently, they are put to use in synchronous digital systems where strict synchronization and accurate timing matter a lot. Figure 1.6 describes the positive, negative edge triggering and level triggering for a pulse signal.

Two types of edge-triggered flip-flops are the D flip-flop, JK flip-flop and T flip-flop.

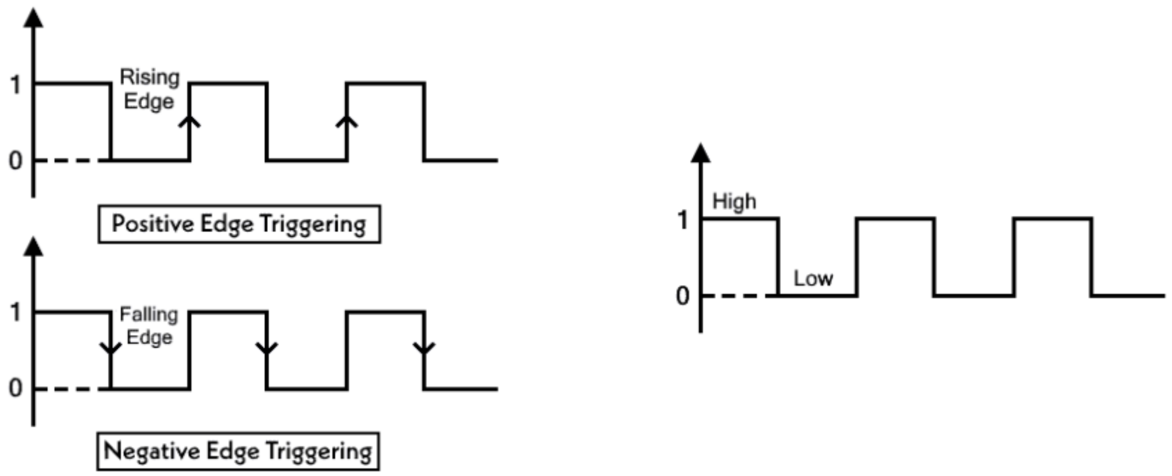


Figure 1.6 Edge and level triggered

Level-Sensitive Flip-Flops:

Level-sensitive flip-flops are also called transparent or latching flip-flops because they work with the continuous state of the input signals no matter the clock's condition.

Even though level-sensitive flip-flops are simple to build, they can cause timing and metastability problems. Level-sensitive versions of flip-flops are the SR latch and the gated latch.

In short, using two connected flip-flops enhances the timing and removes possible race conditions in master-slave flip-flops. Only when its clock reaches an edge does an edge-triggered flip-flop accept its input signals, making timing exact. A level-sensitive flip-flop, by contrast, always reacts to the current value of its input signal and does not require precise timing yet may be more likely to have timing problems. Flip-flop designs are selected according to the requirements of the digital system being built.

1.3 Design Constraints

Design Constraints refer to the parameters that needs to be considered while designing a circuit. This includes Setup time, hold time, clock skew, jitter and other parameters which are as discussed below in the following sections.

1.3.1. Setup Time and Hold Time:

Setup time and hold time are critical timing parameters that ensure the stable operation of flip-flops and prevent timing violations.

Setup Time:

Setup time refers to the minimum time interval before the active edge of the clock signal during which the data input (D) must remain stable for reliable capture by the flip-flop. Not meeting the setup window can result in metastability, where the fluid-flop changes to a state that is hard to predict which may result in errors in the response.

Hold Time:

Hold time is the minimum time interval after the active edge of the clock signal during which the data input (D) must remain stable to ensure correct data retention by the flip-flop. If the hold time requirement is not met, the flip-flop will move to the following state before the input data stabilizes, which could result in data loss or corruption.

Violating the hold time requirement can cause data to become corrupted or lost because the signal changes state before the data is stable. Ensuring adequate setup and hold times is essential for preventing timing violations and maintaining the integrity of data capture and retention operations in flip-flops. Both setup and hold time for a clock and data signal has been clearly mentioned in the below figure 1.7.

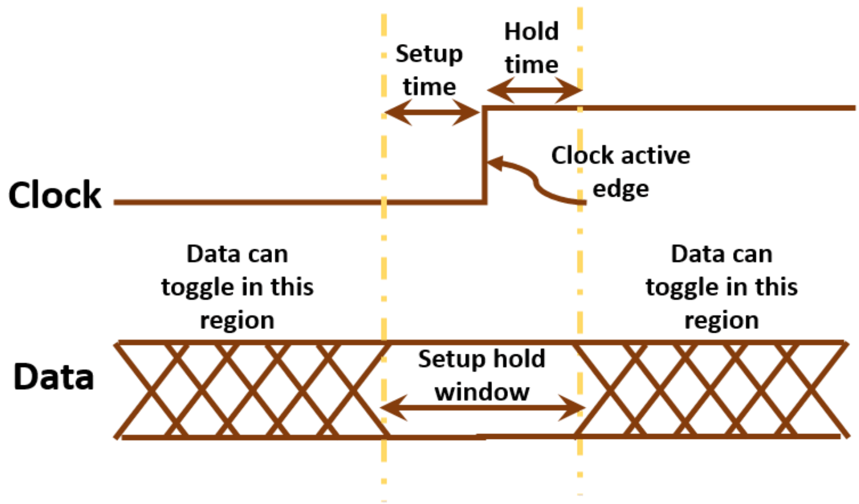


Figure 1.7 Setup and Hold time

1.3.2. **Clock Skew and Clock Jitter:**

Clock skew and clock jitter are sources of timing uncertainty that can affect the performance and reliability of flip-flops.

Clock Skew:

Clock skew refers to the variation in arrival times of the clock signal at different flip-flops or sequential elements within a digital circuit as shown in figure 1.8 where an extra inverter in the clock path to the data register B increases the delay in the path. Timing mistakes and data corruption can result from excessive clock skew, especially in synchronous digital systems where exact timing alignment is essential. Clock skew can be reduced and consistent clock distribution across the circuit can be ensured by using design strategies like clock buffering and balanced clock tree routing.

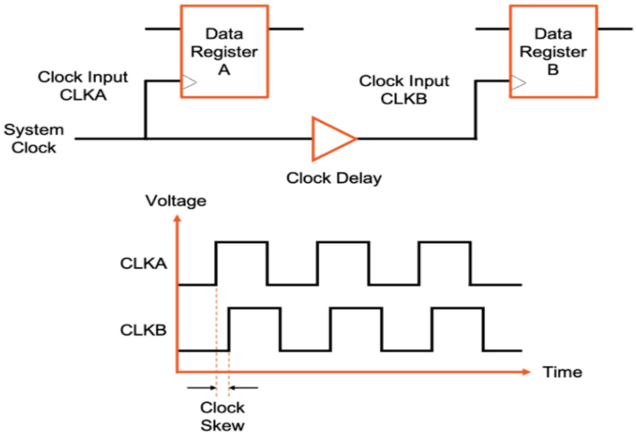


Figure 1.8 Clock Skew

Excessive clock skew can lead to timing errors and data corruption, particularly in synchronous digital systems where precise timing alignment is crucial. Design techniques such as balanced clock tree routing and clock buffering can help minimize clock skew and ensure uniform clock distribution across the circuit.

Clock Jitter:

Clock jitter refers to the random fluctuations or deviations in the period or frequency of the clock signal from ideal signal as seen in the figure 1.9. Clock jitter can degrade the timing accuracy of flip-flops, leading to timing uncertainty and potential data errors.

Addressing clock skew and clock jitter is essential for maintaining reliable timing relationships and ensuring the proper synchronization of flip-flops within a digital circuit.

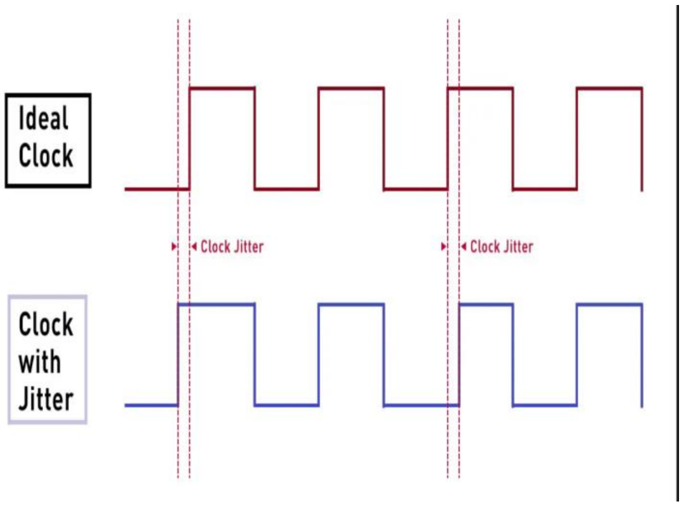


Figure 1.9 Clock Jitter

1.3.3. Power Consumption Optimization:

Power consumption optimization is a crucial consideration in flip-flop design, particularly in battery powered or energy-efficient applications.

Clock Gating:

Clock gating involves dynamically disabling the clock signal to flip-flops during idle periods or when their operation is unnecessary. By selectively gating the clock signal, designers can reduce the power dissipation associated with unnecessary clock transitions and flip-flop toggling.

Power Gating:

Power gating involves selectively shutting off power to flip-flops or portions of the circuit during standby or low-power modes. By powering down inactive flip-flops, designers can minimize static power consumption and extend battery life in power-sensitive applications.

Voltage Scaling:

Voltage scaling is the process of reducing the supply voltage provided to flip-flops to the level sufficient for correct operation. Reducing the supply voltage decreases power consumption but calls for careful optimization of timing margins and voltage-dependent phenomena.

Power consumption and performance must be balanced to maximize the energy efficiency of flipflops and the battery life or energy savings in digital systems.

1.3.4. Speed vs. Area Trade-offs:

Speed vs. area is a basic trade-off in the design of flip-flops since increasing the speed tends to require greater circuit area, and vice versa.

Speed Optimization:

Speed optimization is done by reducing the propagation delay and setup time of flip-flops to enhance speed. Pipelining the circuits, stage pipelining, and layout optimization can enhance flip-flop speed but can increase area and complexity.

Area Optimization:

Flip-flop design optimization in terms of area is essentially all about reducing the physical size of these components, which is extremely important in order to save silicon space and thereby lower production costs.

Engineers will normally investigate miniature flip-flop structures, lay out optimization approaches, and sometimes share resources. Although such methods can actually minimize area, they tend to create trade-offs—most significantly, possible sacrifices in operating speed or increments in power dissipation. Finding a proper balance between area and speed is thus at the heart of the design process, affecting performance goals as well as overall efficiency.

1.3.5. Noise Immunity:

Aside from spatial requirements, the stability of flip-flops under the influence of external perturbations is a fundamental necessity. Noise immunity is important for reliable operation, particularly in practical situations where interference is always present.

Signal Conditioning: - via noise filtering, signal amplification, or impedance matching—is an important first line of defense that increases the ruggedness of flip-flop inputs and outputs. Ground plane design, physical shielding, and isolation techniques can all be employed to minimize the impact of crosstalk and electromagnetic interference (EMI) on flip-flop operation.

Synchronization and Resynchronization synchronization and resynchronization circuits are critical to data integrity, especially where there is noise or timing irregularity. Timing constraints, power dissipation, space, and noise immunity must be addressed comprehensively for reliable, high-performance implementations of flip-flops. Only when all these factors with a bearing on each other are treated with caution can designers guarantee maximum reliability and efficiency and thus satisfy the needs of various digital applications. In real-world digital systems, flip-flops have basic functions, specifically in registers and counters. Registers, basically flip-flop arrays, supply temporary binary data storage essential to contemporary processors. Counters, conversely, are sequential circuits—also composed of flip-flops—that monitor events, frequency divide, and provide timing signals. Among the many types used to meet specialized application requirements are binary, decade, and ring counters.

1.4 Application of Flip Flop

67

1.4.1. Registers and Counters:

2

Registers and counters are the standard uses of flip-flops in digital circuits to store and manipulate binary information and tally events or actions. Given below in the figure 1.10 is the shift register which takes in serial input and gives out serial output.

47

Registers:

A register is a group of flip-flops employed to store data temporarily in the form of binary information. Registers are frequently utilized within microprocessors and digital signal processors (DSPs) to store intermediate or final results of computations, instruction operands, and program status information.

42 Registers can be implemented using different flip-flop configurations of registers, including shift registers, parallel-in-serial-out (PISO) registers, or serial-in-parallel-out (SIPO) registers.

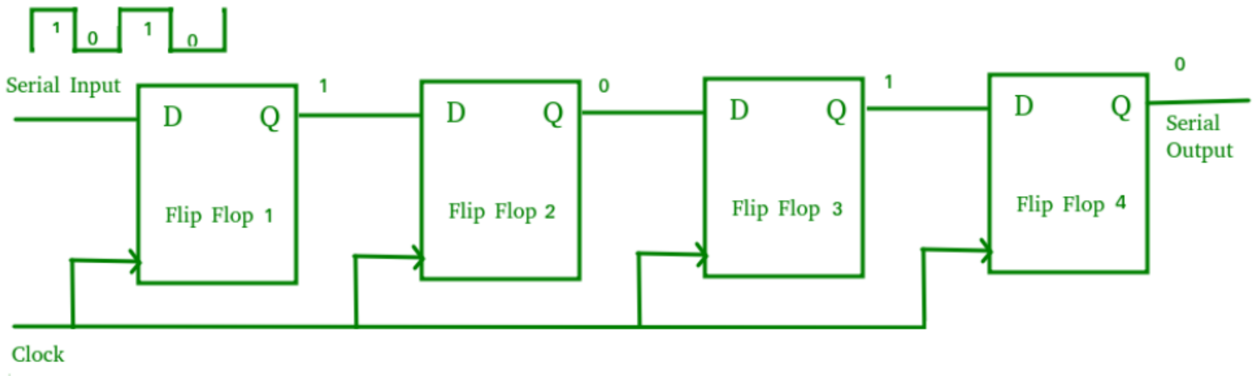


Figure 1.10 Shift Register

Counters:

49 A counter is a sequential circuit used to count pulses or events and provide an associated binary output. Counters are common in digital systems for frequency division, event counting, and generating a timing signal. Figure 1.11 shows an asynchronous counter made with JK flipflop.

91 60 Flip-flops are the key elements of counters, with each flip-flop deciding a binary digit (bit) of the counter output. Various kinds of counters, including binary counters, decade counters, and ring counters, may be designed by combining flip-flops and logic gates to fulfill particular applications. Registers and counters are critical components of many digital systems, offering basic storage and counting facilities that are required for performing arithmetic operations, data processing, and control operations.

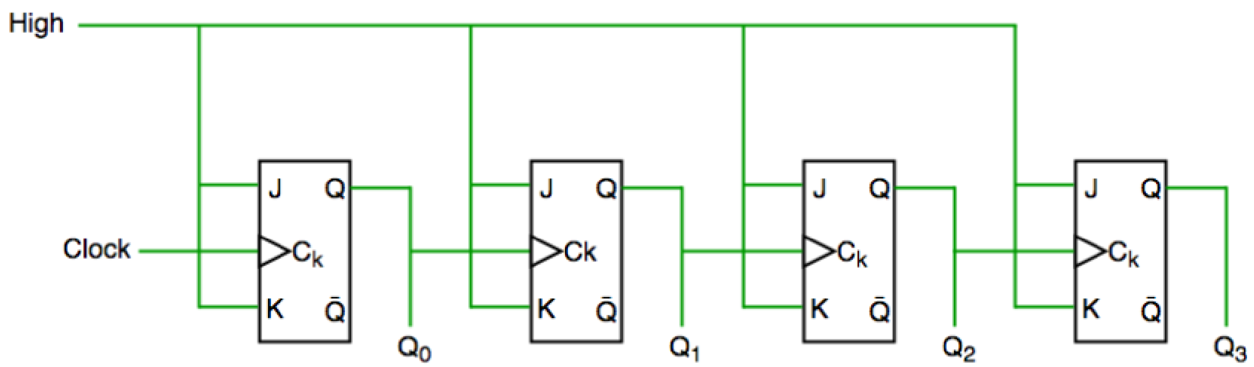


Figure 1.11 Counter

1.4.2. Memory Elements in Microprocessors:

Flip-flops are basic memory elements in microprocessor designs, storing and manipulating binary data while it passes through the CPU processing.

Registers in Microprocessors:

In microprocessors, many registers made up of flip-flops facilitate quick storage and retrieval of data during instruction execution. This ability is crucial in effective data movement and manipulation within the CPU.

Typical register types in microprocessors include accumulator, general-purpose registers (such as AX, BX, CX, DX in x86 architecture), and dedicated registers (such as program counter, stack pointer, status register). Registers' flip-flops allow rapid access to information and support effective data movement and manipulation activities within the CPU.

Cache Memory:
Cache memory flip-flops provide low-latency data access, which greatly enhances processor performance overall. Cache memory flip-flops allow for rapid retrieval and storage of data to reduce memory access latency and enhance overall CPU performance.

Flip-flops are responsible for the functioning of microprocessors, enabling data storage, transfer, and manipulation operations required for the execution of instructions and computation of tasks efficiently.

1.4.3. State Machines:

State machines are another important flip-flop application area. In state machines, the flip-flops are used as memory elements to store the state and allow for transitions based on input signals.

Finite State Machines (FSMs):

Finite state machines, based on sequential logic, are the basis of a vast range of applications, ranging from control systems to digital signal processing and communication protocols. State machines are another prominent use of flip-flops. In state machines, flip-flops are used as memory elements, holding the present state and causing state transitions in response to input signals.

Finite state machines, designed with sequential logic, form the basis for a vast number of applications such as control systems, digital signal processing, and communication protocols.

State Registers and Control Logic:

Flip-flops are employed to realize state registers in state machines, holding data related to the present state of the system.

Control logic circuits, typically implemented in terms of combinational logic, utilize the state information held in flip-flops to decide the next state and drive the behavior of the system.

Finite State Machine are of two types Mealy and Moore which are shown below in figure 1.12. Mealy machine depend on the state and input both whilst Moore machine output depends only on the current state.

102

In conclusion, flip-flops have various applications in digital systems such as registers and counters for data storage and counting, microprocessor data manipulation elements in memory, and state machines for modeling sequential control and behavior. It is crucial to know these applications when designing efficient and reliable digital circuits for any type of computing task.

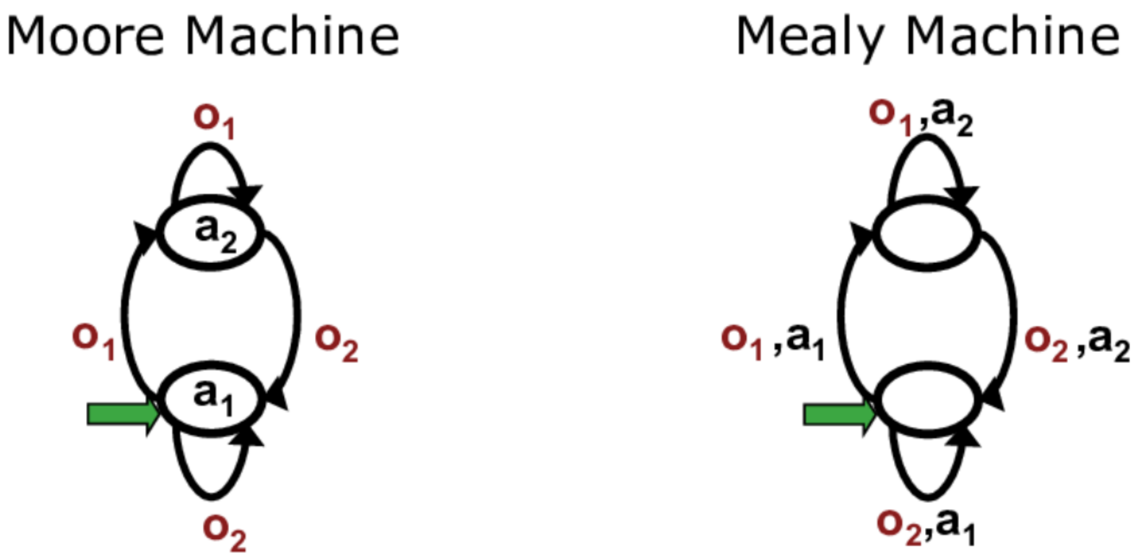


Figure 1.12 Generic Moore and Mealy Machine

CHAPTER 2
LITERATUTRE SURVEY

2.1 Literature Review

The field of digital circuit design has seen increased curiosity in Pulse Triggered Flip-Flops (PTFFs) because of their ability to greatly improve speed and power efficiency in contemporary integrated circuits. As the need for high-performance and low-energy systems continues to grow—especially in fields like portable electronics, high-speed computing, and low-power embedded systems—PTFFs have been found to be a viable replacement for conventional flip-flop structures.

One of the significant works in this area is the comparative study by K. John, V.K.R.S., and K.S.S., which compares different explicit pulsed flip-flop designs systematically on the basis of low power and high-speed applications. Their work gives a complete performance comparison between pulse-triggered flip-flops and master-slave latches based on important parameters like propagation delay, setup and hold times, clock-to-Q delay, and power dissipation. Through measurement of these parameters in several design implementations, the research presents useful feedback on each flip-flop type's operational efficiency and trade-offs. Their work's practical focus is one of its greatest strengths. The authors not only report empirical results but also explain the meaning of the results in terms of actual design situations. It covers advice on how to choose the best storage component for a given set of design objectives—whether minimizing power consumption, optimizing speed, or finding a fair compromise between the two is most important. These are especially useful to VLSI designers, who frequently have to deal with very tight constraints in terms of area, power, and timing. In addition, the research explores the design trade-offs that are inherent in the decision between master-slave latches and PTFFs. Although master-slave latches are conventionally preferred due to their simplicity and strength, PTFFs provide better performance with respect to clock gating and less switching activity, which translates directly into less dynamic power consumption. But these advantages are paid with penalties in the form of pulse width and clock jitter sensitivity that need to be properly dealt with during the design. Authors end with a conclusion of the main contributions and findings of their work and highlight the significance of well-informed storage element selection. Their results affirm the idea that flip-flop architecture selection has a significant influence on the performance and power efficiency of a digital system. Therefore, their research forms the basis for upcoming low-power high-speed digital design innovations, and emphasizes the changing role of PTFFs in future generation VLSI systems.[1]

In the quest for optimizing digital storage elements in terms of power efficiency and speed, the research work by Keerthana K., Shanmugaraja M., and MaheshKannan P. is a valuable contribution to flip-flop design science. Their work is a comparative study between traditional flip-flops and explicit pulse-triggered flip-flops (PTFFs), with reference to the signal feed-through approach as a solution for performance enhancement. Their work's focal point is the assessment of PTFFs' potential as a solution to the power-speed trade-off issue in sequential digital circuits. The authors set the stage with a detailed historical review of the evolution of flip-flop architectures, tracing the evolution from early edge-triggered architecture to more sophisticated pulse-triggered architectures. This history is important in understanding the reasoning behind the utilization of pulse-triggered mechanisms, whose goals are to eliminate unnecessary switching activity and thus diminish dynamic power dissipation. They set the stage for their literature review, which captures the richness of method in the design of flip-flops with many clocking schemes, logic styles, and transistor-level optimizations. Much of their work is the identification and discussion of existing limitations and issues in standard flip-flops' implementation. These consist of the added clock load, redundant transitions, and clock skew susceptibility—issues that all lead to performance degradation and increased energy consumption. The signal feed-through method, as utilized in their work, addresses these issues by enabling direct data propagation during the active clock pulse, thus lowering latency and energy efficiency improvement. Moreover, the authors situate their work in the design of low-power VLSI in general, and they draw on prior work that has sought to exchange speed for power through techniques such as clock gating, dual-edge triggering, and conditional capture. Situating their work in this stream, they can demonstrate convincingly how their solution builds on and extends what is already available. The research not only contrasts the performance of PTFFs with conventional designs but also introduces new design insights that are likely to be co-opted by future sequential logic circuit advances. Overall, the research by Keerthana K., Shanmugaraja M., and MaheshKannan P. is a critical examination of flip-flop selection and implementation design trade-offs.[4]

20 The research by N. K. Saini and K. K. Kashyap is a specialized study of low-power dual-edge triggered flip-flop (DETFF) design and implementation. The flip-flops are designed to record data on both the rising and falling edges of the clock signal, doubling the data rate without a rise in the clock frequency. This feature is specially beneficial for low-power applications, since it provides a lower clocking activity—a significant contributor to dynamic power in synchronous digital circuits. Their work highlights the design issues involved in optimizing the performance in DETFFs, such as transistor sizing, clock distribution, and timing synchronization. Since DETFFs trigger on both 1 clock edges, they are capable of achieving comparable performance levels to single-edge triggered flip-flops while dissipating much lower power. The authors also identify the energy-efficient 27 characteristics of positive-edge triggered D-type flip-flops, which are used as a building block in their introduced architecture. Their conclusion emphasizes the strengths of DETFFs in power-constrained applications, including battery-powered devices and portable devices. [5]

In another research study done by another complementary but independent research work, H. Panwar, N. S. Singha, and M. K. Singh has performed a comparative analysis of pulse-triggered flip-flops (PTFFs) and a specialized version called the Signal Feed-Through Flip-Flop (SFTFF) in detail. Their work is motivated by the necessity to ensure high-speed operation in conjunction with low power dissipation, an important requirement for contemporary VLSI circuits. Various PTFF architectures are compared and analyzed with the SFTFF from the viewpoints of propagation delay, power dissipation, and overall switching efficiency. Their findings indicate that the SFTFF outperforms conventional PTFF designs in all measured parameters consistently. Its better performance is due to the signal feed-through mechanism, which makes it possible for a fraction of the input signal to skip some internal stages of the flip-flop, resulting in faster data transition. Not only does this decrease latency, but also the number of active switching elements, hence reducing power consumption. The work offers a quantitative basis for the use of SFTFFs in high-speed digital circuits, especially in situations where the accuracy of timing and energy efficiency are essential. The authors conclude that the incorporation of signal feed-through techniques is a notable step forward in flip-flop design, providing an effective solution to the shortcomings of traditional PTFFs. [3]

In the ever-evolving world of digital circuit design, the search for low-power and high-performance flip-flop structures remains the underlying problem. Another paper by Chen Kong Teh, Mototsugu Hamada, Tetsuya Fujita; Hiroyuki Hara, Nobuyuki Ikumi and Yukihito Oowaki introduces a novel family of flip-flops known as Conditional Data Mapping Flip-Flops (CDMFFs), which are specifically designed to address the twin requirements of low power and high speed. The secret to CDMFFs lies in the fact that they dynamically map input data in such a manner that redundant internal transitions—those transitions, in conventional designs, that contribute to a large portion of dynamic power dissipation—are eliminated. The authors introduce two structural forms of CDMFFs: one with a differential structure and one with a single-ended structure. The designs are compared in depth with a variety of state-of-the-art flip-flop structures, including conditional capture and transmission-gate-based architectures. The comparison reveals that both forms of CDMFFs possess better power-delay product (PDP) values in their respective classes, which means their capacity to trade off speed and energy consumption. From the power dissipation perspective, the findings are quite impressive. At data activity levels of less than 50%—a reasonable assumption in many real-world systems—the single-ended and differential CDMFFs achieve power savings of 31% and 26%, respectively, over conditional capture flip-flops. The savings are quite spectacular at 25% data activity, a scenario that models idle or low-utilization modes in digital systems, where leakage of power needs to be avoided. On the performance front, CDMFFs achieve data-to-output delays comparable to some of the fastest known flip-flop designs, including the transmission-gate pulsed latch and the modified sense-amplifier flip-flop. This is a clue that the proposed designs do not compromise on speed to achieve power efficiency—a rare and valuable attribute in sequential logic design. Another important advantage of CDMFFs is their superior timing reliability. The article highlights that these flip-flops possess superior internal race immunity, a characteristic of particular importance in ensuring stable operation under a broad set of clock and data conditions. This makes CDMFFs particularly appealing to high-speed digital circuits where timing margins are tight and reliability is of paramount importance. To illustrate the practicality of their design, the authors provide a post-layout case study, comparing the single-ended CDMFF with a conventional transmission-gate flip-flop. The results are dramatic: the CDMFF offers a 34% reduction in data-to-output delay and a 28% reduction in power dissipation at 25% data activity. These improvements come at the cost of a 34% increase in silicon area, a trade-off quite easily acceptable in applications where power and speed are more significant factors than layout tightness. Overall, the invention of CDMFFs is a significant breakthrough in the design of sequential elements for low-power VLSI circuits. By ingeniously eliminating redundant transitions and optimizing internal logic paths, these flip-flops offer an appealing solution to designers interested in enhancing the energy efficiency and performance of modern digital circuits.[11]

Drawing from the idea of signal feed-through, J. Vishalakshmi and P. K. Suresh also explored the performance of PTFFs with increased signal feed-through techniques in great detail. Their study is especially concerned with overcoming delay-related issues that commonly hamper the performance of standard flip-flop design in high-speed settings. By intensive simulation and experimental verification, the authors show that the introduction of signal feed-through paths in the PTFF structure results in drastic clock-to-Q delay and setup time reduction. These reductions directly imply higher operating frequencies and improved timing closure in complex digital systems. In this regard, the research points to energy-saving capabilities of this approach, stating that the internal switching activity reduction helps reduce dynamic power consumption. The authors also delve into the general implications of these findings for VLSI design, especially in energy-constrained applications like IoT devices, wearable electronics, and mobile computing platforms. Through the demonstration of the utilitarian advantages of signal feed-through in PTFFs, their work reiterates the value of novel circuit-level methods to the twin objectives of speed and efficiency. [6]

In the ongoing pursuit of optimizing sequential blocks for today's digital systems, another paper by Jin-Fa Lin, introduces a new low-power flip-flop (FF) architecture that integrates an explicit pulse-triggered structure with a reworked true single-phase clock (TSPC) latch, augmented by a signal feed-through mechanism. This design represents a significant advancement over the weaknesses of conventional pulse-triggered flip-flops (P-FFs), the most significant of which are long discharge paths, long the nemesis of speed and energy efficiency. Standard explicit-type P-FFs are frequently beset by long discharge paths that are part of the critical path delay and contribute to high dynamic power dissipation. These inefficiencies are particularly pernicious in high-speed designs, where even minor delays can compound and undermine system performance. The proposed design confronts this issue head-on by adding a signal feed-through mechanism, which surprisingly shortens the discharge path and allows for faster signal transfer through the latch. The breakthrough is the reworking of the internal logic to facilitate selective and efficient data examination, sans unnecessary transitions and reduced switching activity. This not only boosts speed but significantly lowers power consumption as well—two numbers that are traditionally at cross-purposes in flip-flop design. The use of a true single-phase clocking scheme also reduces the clock distribution network, lessening clock skew and jitter, as well as overall system stability. To test the efficacy of the proposed architecture, the authors conducted post-layout simulations using TSMC 90-nm CMOS technology, an industry-standard process node for low-power digital design benchmarking. The result is edifying: the new flip-flop design achieves an 8.2% reduction in data-to-Q delay over the conventional explicit data-close-to-output (ep-DCO) flip-flop. This reduction in delay directly corresponds to faster clock cycles and higher throughput in synchronous circuits. In addition, the design is highly power efficient. Under normal operating conditions, the designed flip-flop shows a 22.7% reduction in power and a 29.7% reduction in power-delay product (PDP). These numbers are crucial in determining the viability of a flip-flop in real applications since they reflect the trade-off between speed and energy consumption—a consideration that is increasingly important in power-constrained applications such as mobile computing, IoT devices, and wearable electronics. This work, in summary, provides a holistic and viable solution to the problems bedeviling conventional P-FFs. By exemplary integration of pulse-triggered operation with signal feed-through and TSPC designs, the designed flip-flop boasts enhanced performance without sacrificing energy efficiency. It is a promising candidate for next-generation VLSI systems, where the demand for small, fast, and low-power sequential components is ever on the increase.[10]

This body of research collectively advances the understanding of explicit PTFFs, highlighting the critical role of signal feed through technique in enhancing speed, and reducing power consumption for future innovations.

2.2 Scope for Enhancement and Expansion

The comprehensive literature review revealed that power consumption and delay remain considerably high, underscoring the need for further analysis and optimization. In response to these challenges, a novel flip-flop design has been developed as part of this research, with detailed discussion provided in the following chapter.

CHAPTER 3

DIFFERENT FLIP FLOP DESIGN

Regarding pulse generation, Pulse-Triggered Flip-Flops (PT-FFs) can be categorized into two types: explicit and implicit. Explicit pulse signals are not produced independently in the implicit kind of P-FF; instead, the latch itself consists of the pulse generator circuit. On the contrary, the latch function and the pulse generator are distinct entities in the explicit type of PTFFs. A longer discharge path has a disadvantage in implicit PTFFs, which might lead to less desirable timing characteristics. Conversely, explicit pulse generation offers the FF design a distinct performance advantage, at the expense of increased power consumption. This benefit stems primarily from the distinct segregation of logic components from the latch design. It should be noted that sharing a single pulse generator across set of flip-flops can notably lower the circuit complexity and power consumption of explicit P-FFs.

3.1 Explicit Data Close to Output (epDCO)

The effectiveness of traditional flip-flop designs was evaluated and contrasted. An illustration of the explicit data-close-to-output design is presented in Figure 3(a).

The design described integrates a pulse generator utilizing NAND logic alongside a semi-dynamic True Single-Phase Clock (TSPC) structured latch. Within this configuration, the pulse generator's operation relies on a series of inverters, denoted as I1, I2, I3, and I4, each serving distinct purposes. Inverters I1 and I2 are strategically employed in an explicit Pulse-Driven Cross-Coupled (ep-DCO) configuration to sustain the state of the internal node X. Meanwhile, inverters I3 and I4 are tasked with the crucial function of latching the data.

The operation of this design hinges on the interaction between the pulse generator and the structured latch. Within the pulse generator circuit, the delay introduced by the three inverters (I1, I2, and I3) plays a pivotal role in determining the resulting pulse width. However, despite its functionality, a critical flaw is observed in this design. It is important to note, however, that non-idealities can arise. For instance, a persistent input of “1” can cause node X to discharge on every rising clock edge, leading to excessive switching power dissipation. This presents a clear drawback in terms of efficiency and performance. Even when advanced techniques such as NAND-based pulse generators and semi-dynamic TSPC latches are employed to enhance functionality and simplify design, careful validation remains crucial to avoid unintended power losses and ensure robust circuit operation.

In summary, designing high-quality flip-flops requires meticulous attention to area, speed, power, and noise immunity. When these factors are thoughtfully balanced, flip-flops can provide the reliable, efficient performance necessary for contemporary digital systems.

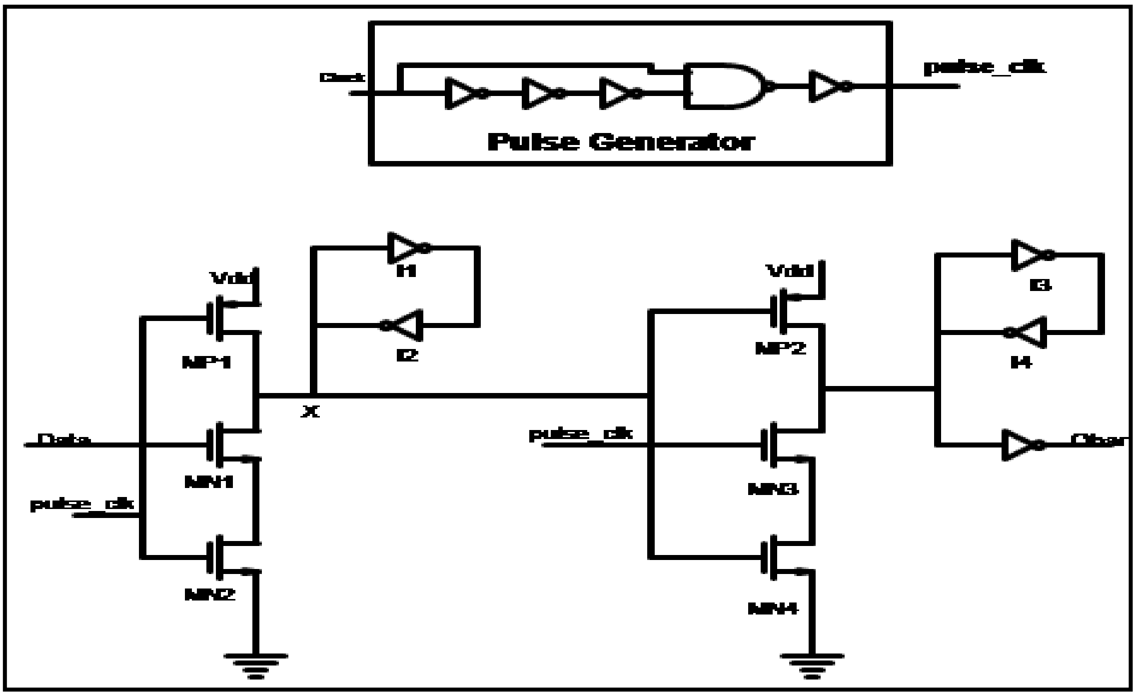


Figure 3(a). ep DCO

62

3.2 Conditional Discharge Flip Flop (CDFF)

The conditional discharge (CD) technique, depicted in Figure 3(b), introduces a mechanism for effectively managing the discharge process within the flip-flop circuitry. Central to this technique is the utilization of output data control to regulate the state of an additional n-MOS transistor, denoted as MN3. Unlike conventional flip-flop configurations, where discharge paths are typically static, the CD technique leverages the control of output data to dynamically control the behavior of MN3, thereby offering enhanced flexibility and efficiency in the discharge process.

7

The CD method includes a pull-up p-MOS transistor and an inverter at node X, both known as the keeper circuit. This setup plays an important role in holding the state of node X, thus guaranteeing flip-flop operation stability and reliability. The keeper circuit is not passive but is actively involved in controlling the state of MN3 according to the output data to optimize the discharge process. Through this, power consumption is reduced and overall circuit performance is enhanced.

Applications of the CD technique constitute a significant improvement in the design of flip-flops, bringing about more efficiency and higher functionality compared to conventional techniques. Incorporating dynamic discharge control mechanisms, like the keeper circuit, provides the original circuit designers with greater flexibility and scope for optimization. This eventually translates to better performance and reliability in digital circuit applications.

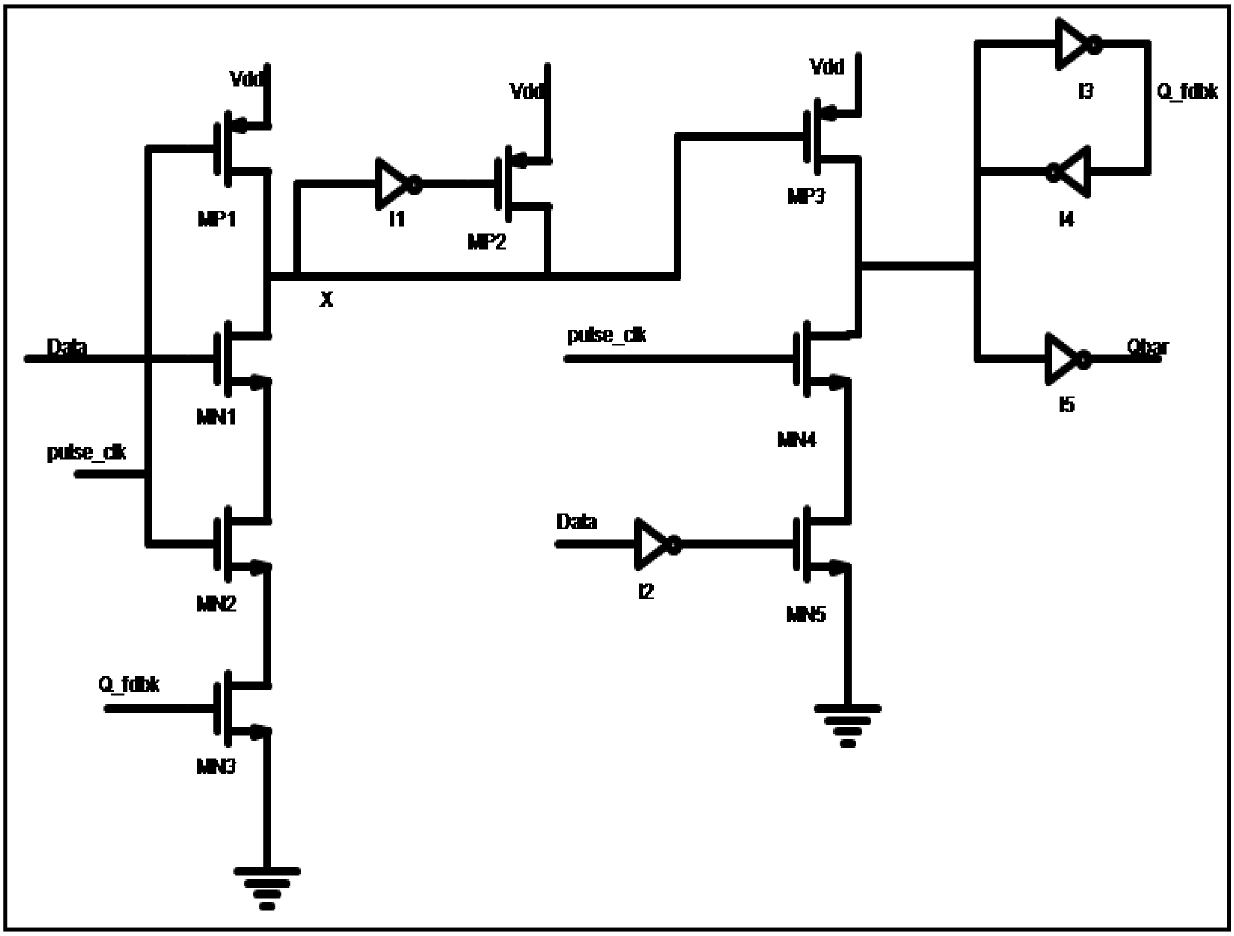


Fig 3(b). CDFF

3.3 Static Conditional Discharge Flip Flop (SCDFF)

The Static Conditional Discharge approach introduces a departure from the conventional Conditional Discharge Flip-Flop (CDFF) design by virtue of its use of a static latch structure, as shown in Figure 3(c). Such a structural characteristic obviates the need for regular pre-charging of node X, unlike the dynamic operation common to the CDFF design. However, while this static configuration offers advantages such as reduced power consumption and simplified operation, it also introduces certain trade-offs, notably in terms of data-to-Q (D-to-Q) latency.
It's essential to recognize that, unlike the CDFF design, the Static Conditional Discharge Flip-Flop (SCDFF) experiences a comparatively greater D-to-Q latency. Such latency is caused by the intrinsic nature of the static latch structure, which intrinsically involves a more sluggish response time than that of dynamic counterparts. In SCDFF structure, the lack of traditional pre-charging requires an alternate method of sustaining node X's state, which is partly responsible for the latency shown. Both CDFF and SCDFF circuits have one common feature in the shape of a three-transistor discharge path, that is, MNI, MN2, and MN3. Such a discharge path causes a delay in the flip-flop circuit, impacting its total performance indices like speed and efficiency. Despite these challenges, the SCDFF design offers unique advantages, including simplified circuitry and reduced power consumption, making it an attractive choice for certain applications where latency considerations are less critical compared to other performance factors.

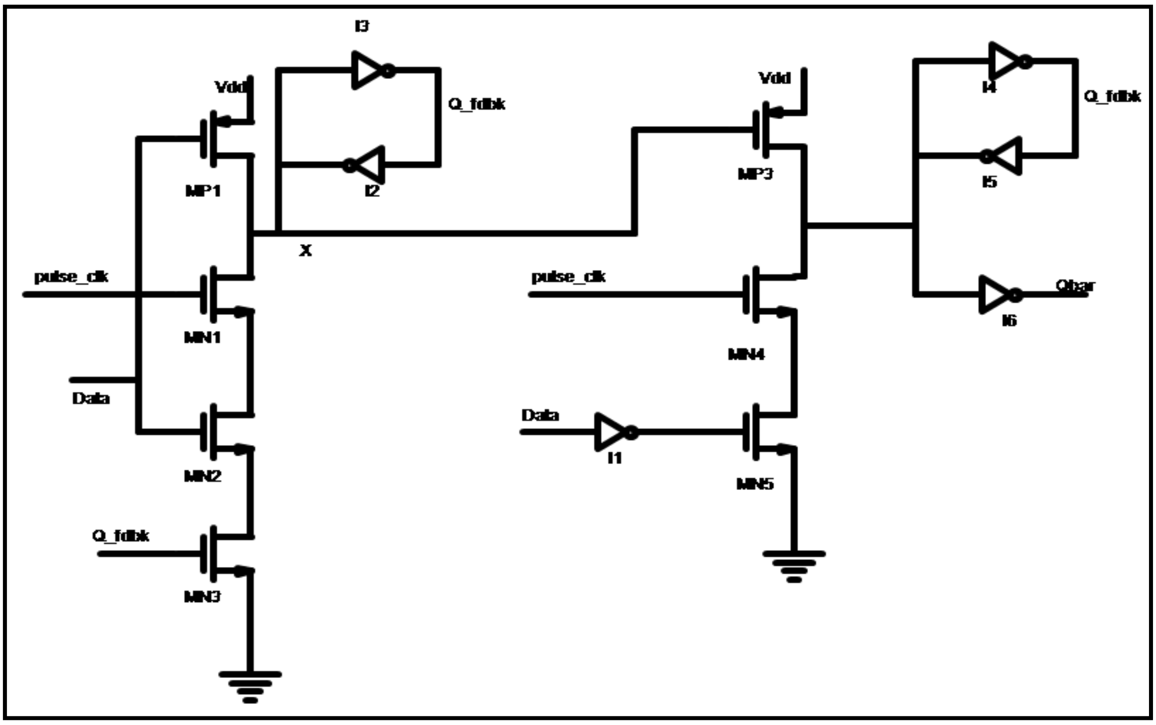


Fig 3(c). SCDFF

3.4 Signal Feed Through Flip Flop (SFTFF)

The circuit diagram depicted in Figure 3(d) illustrates the Explicit Pulsed Signal Feed-Through Flipflop (SFTFF), a flip-flop configuration designed to harness the advantages of explicit pulse generation and signal feed-through techniques. At the core of this design lies the explicit pulse generation unit, comprising NAND gates and a series of inverters. This unit is responsible for generating the necessary pulses to drive the flip-flop operation efficiently.

Traditional flip-flop designs, the SFTFF incorporates the signal feed-through technique, which leverages pseudo-n-MOS logic and a latch mechanism utilizing a real single-phase clock scheme. This innovative approach allows the clock pulse signal to activate an N-type pass transistor, denoted as MNx, within the Pulse-Triggered Flip-Flop (P-FF). By enabling direct feed-through of the input signal to the output, the SFTFF achieves enhanced efficiency and performance.

While operating, when the input data crosses from a LOW state to a HIGH state, the pass transistor MNx establishes a path for the output of the pass transistor to drain through MNx, along with an additional triggering capability in the output. But it's worth noticing that this mechanism of direct feedthrough can cause "glitches" in the output signal, which in turn can cause skew issues at the input. These are glitches caused by the extra triggering power delivered directly from the input D to the output, affecting the stability and dependability of In addition to the potential issues involved in glitch generation, the SFTFF design provides several benefits in terms of speed, efficiency, and simplicity. By incorporating explicit pulse generation and signal feed-through methods, the SFTFF is a major development in flip-flop design in response to the changing demands of contemporary digital circuitry. Future developments and further improvements on similar innovative strategies promise even greater performance and functionality of flipflop devices in new applications.

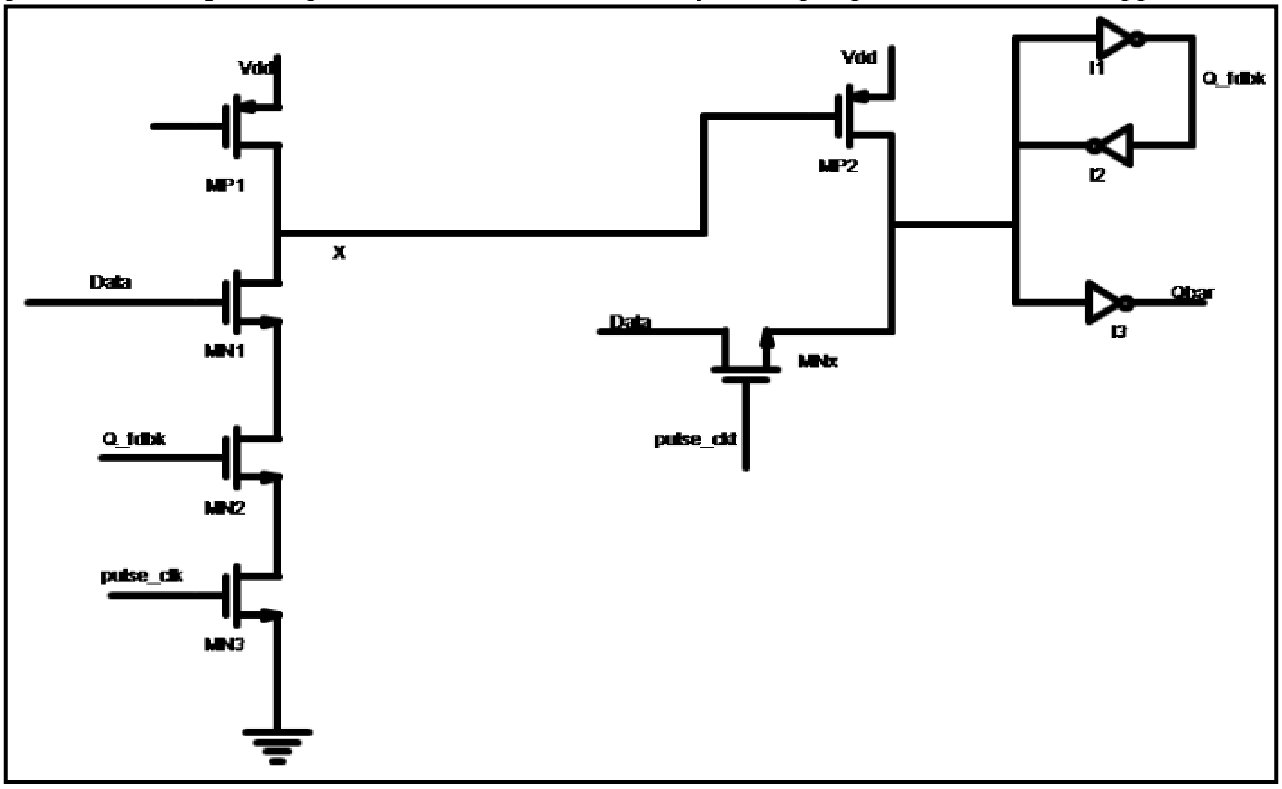


Fig 3(d). SFTFF

CHAPTER 4

PROPOSED CIRCUIT WITH LOW POWER AND HIGH SPEED

In the realm of Very Large-Scale Integration (VLSI) design, the clock signal serves as a fundamental pillar upon which the entire architecture is built. The clock coordinates the coordinated functioning of millions, employing perhaps billions, of transistors in a semiconductor chip, so that data is processed and transmitted with accuracy and effectiveness. This introduction examines the three-pronged role of the clock in VLSI design, examining its importance, concepts, and implications in contemporary electronic systems.

Essentially, the clock is an periodic signal that switches between two voltage levels, usually represented as high (logic 1) and low (logic 0). The oscillation is what the digital clocking scheme is based on, where every change of the clock signal represents a discrete time interval, often called a clock cycle or clock period. The duration of a clock cycle, determined by the frequency of the clock signal, dictates the operational speed and timing constraints of the VLSI circuit.

The clock signal is, in effect, the pulse of a VLSI system, providing the necessary timing reference which guides the systematic prosecution of operations between the components of the chip. Its presence ensures instructions are performed in an orderly manner, rather than dissolving into anarchy—just as an orchestra relies on its conductor to hold it together.

In particular, the clock does much more than simply track the passage of time. It establishes the precise points at which information is processed and transferred, so that flip-flops and other sequential circuits—registers, counters, and state machines—can execute with proper timing. Synchronization is key to the reliable operation of complex circuits.

Timing closure, a major challenge in VLSI design, is more or less ensuring that setup and hold times, clock-to-output delays, and propagation delays are all satisfied within each clock cycle.. The clock itself provides the basis for these constraints, determining the overall operating rhythm of the whole chip. Should there not be strict compliance with these timing demands, the system itself would be impaired. Failing to meet these constraints can lead to significant functional errors or system instability.

Efficient clock distribution is equally essential. The clock signal must propagate to all relevant circuit elements with minimal skew and delay. To this end, designers utilize clock trees, buffering, and various synthesis techniques to optimize distribution and maintain synchronous operation across the chip. Clock skew minimization, in particular, is crucial to ensuring that all parts of the system receive the signal at the intended moment, thus safeguarding signal integrity and correct timing.

Power management is yet another area in which the clock signal holds critical importance. Clock gating, for example, disables clock delivery to dormant parts of the circuit selectively, diminishing unnecessary power consumption. Dynamic voltage and frequency scaling (DVFS) also uses the clock to dynamically alter operational parameters based on demands from the workload, further optimizing performance against energy efficiency.

Even though it is indispensable, the clock signal presents problems. Clock skew, jitter, and noise can threaten timing dependability, requiring vigilant mitigation techniques throughout design. As clock frequencies rise to keep pace with continually increasing performance demands, the engineering challenges of dealing with heat dissipation and power consumption become more significant, compelling designers to find new clocking and power management solutions.

In conclusion, the clock signal is a cornerstone of VLSI design. It provides synchronization, accurate timing, and efficient power control—abilties that are essential to contemporary electronic systems. Its impact defines the architecture and performance of digital circuits, and as technology improves, the role and complexity of clock design continue to grow in the industry.

Pulse-triggered flip-flops (P-FFs) represent a distinctive class of sequential logic circuits integral to digital circuit design. Unlike conventional clocked flip-flops that depend on a steady, periodic clock to control state changes, pulse-triggered flip-flops (P-FFs) operate by capturing and storing data using brief, distinct pulses. This shift from standard clocked designs yields several significant advantages, explaining why P-FFs are gaining traction in modern digital systems.

72 One of the most notable benefits of P-FFs is their efficiency in power consumption. Because they do not consume a constant clock signal, P-FFs minimize power consumption in inactive states. This characteristic is particularly desirable for battery-operated systems, in which maximizing battery life and enhancing long-term system reliability are paramount considerations.

Aside from enhanced power efficiency, P-FFs also provide for accelerated operation. Their use of short-pulse durations facilitates quick data capture and storage, which becomes directly translated to faster processing and higher system throughput. This renders P-FFs well-adapted for applications requiring high-speed data management—like telecommunications, signal processing, and real-time control—where quick response is paramount.

Designing digital circuits also becomes simpler with P-FFs. Clocked flip-flops need complicated clock distribution networks, which can cause difficulties such as clock skew, jitter, or timing violations. P-FFs, however, need only short pulses to work, making design simpler and the overall system more reliable.

In conclusion, pulse-triggered flip-flops offer a cost-effective, general-purpose substitute for conventional clocked flip-flops in digital circuit design. Because they utilize short pulses, they result in reduced power consumption, increased speed, and reduced clocking requirements, yet they are becoming ever more critical in modern digital electronics. As high-performance, energy-saving devices continue to be in rising demand, P-FFs remain a mainstay of advancing digital circuit technology.

4.1 Proposed Clock

The major difference between the earlier pulsed flip-flop and the one suggested here is in clock circuit design. The earlier one used a NAND-based clock generator that consumed 12 transistors, while the new pulse generator circuit uses only 4 transistors. This dramatic decrease in the number of components goes a long way in reducing complexity and resource utilization in generating pulses and represents the enhanced efficiency of the suggested method.

This pulse generator revolves around a series of CMOS inverters, consisting of interlaced PMOS and NMOS transistors. The gate in each transistor within this series is powered by a common clock signal, making the circuit perform synchronously throughout. When the clock signal is low, the PMOS transistor within the first inverter is turned on, conducting current from supply to output. On the contrary, an increased clock signal turns on the NMOS transistor, allowing current to flow from ground to the output node. This switching results in a complementary output signal, which is necessary for further stages of circuits.

The output from the first inverter serves as the input to the subsequent NMOS transistor. As the inverter's output transitions, the corresponding NMOS transistor either enables or disables current flow, ensuring the output node is properly set to either the supply voltage or ground. This configuration maintains complementary signals at each stage, resulting in a continuous square wave with alternating states. The inherent inversion in CMOS inverter operation does not affect the pulse characteristics but provides an inverted representation of the input, thus sustaining consistent and reliable pulse generation.

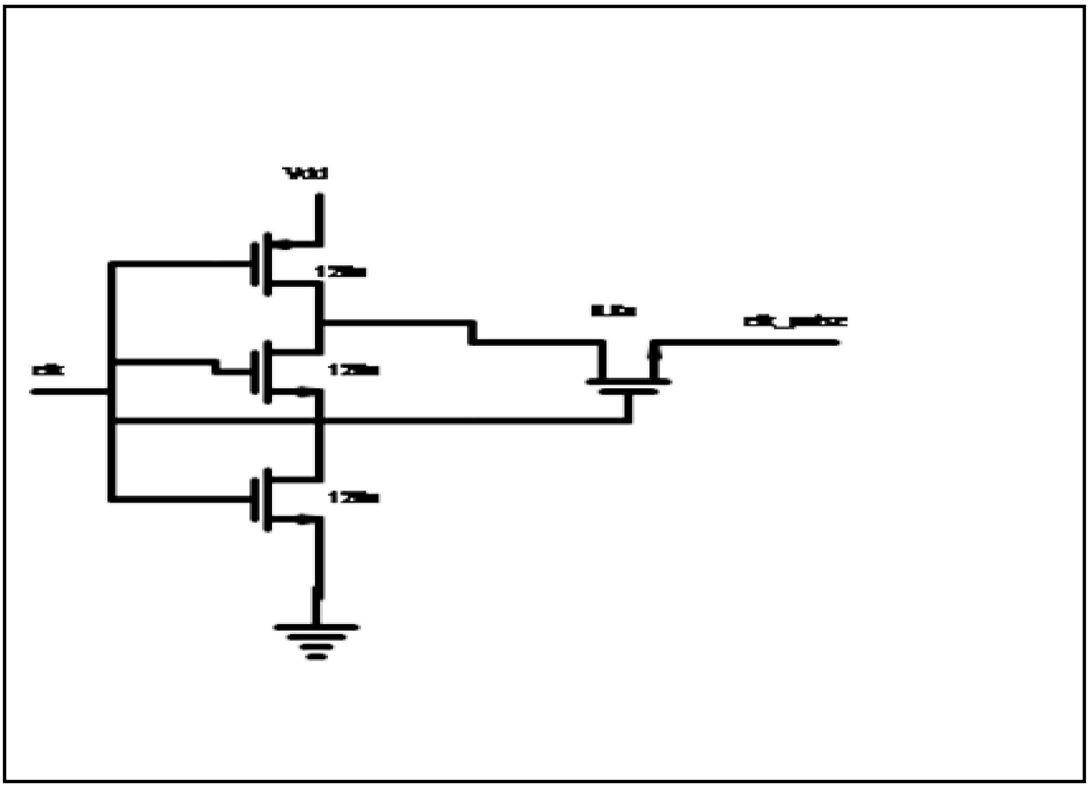


Fig4(a). Pulsed clock generation circuit

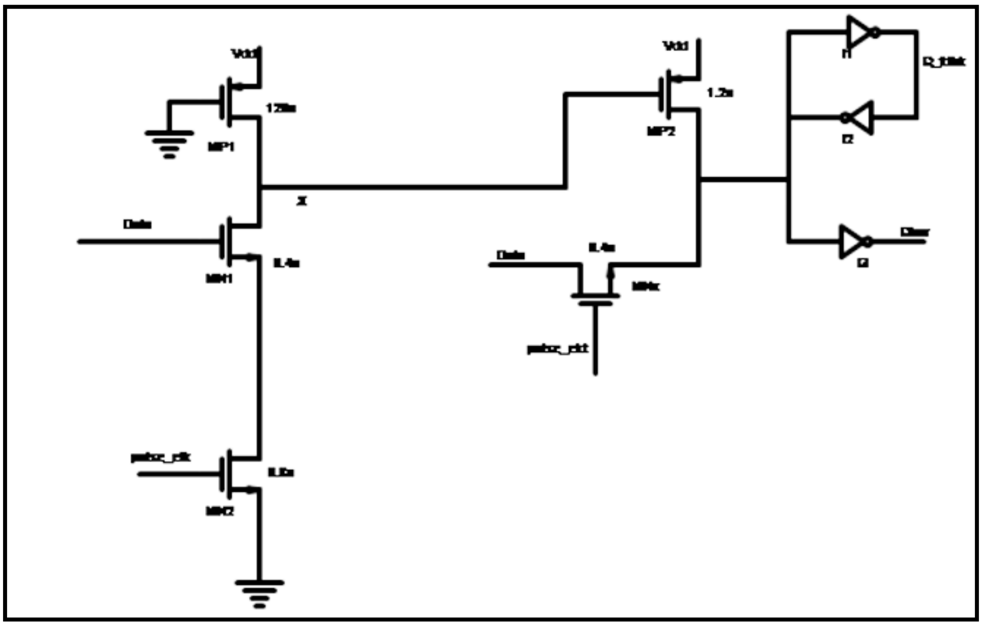
4.2 Proposed Flip Flop Circuit

The circuit diagram depicted in Figure 4(b) illustrates the Proposed Flip Flop design, which involves an explicit pulse generating unit that consists of an innovative pulse generator circuit. In this design, the key aspect is the use of the signal feed-through mechanism, in which a pulsed clock signal is passed to the NMOS logic and a PMOS transistor is tied to the ground, with it always remaining active.

In this Pulse-Triggered Flip-Flop (P-FF), the clock pulse signal is used as the trigger for an N-type pass transistor MNx. This MNx triggering allows the direct feed-through of the input to the output, making the operation more efficient and faster. The use of the pass transistor MNx also brings extra triggering power to the output of the pass transistor, maximizing the circuit performance

In operation, as the input data goes from LOW to HIGH level, the pass transistor MNx serves as a pathway through which the output of the transistor is allowed to discharge. The discharge is enabled by the extra triggering power of MNx, thereby enabling proper and effective transmission of signals in the flip-flop. Yet, it is important to recognize that the direct addition of initiating power from the input D to the transistor output can be a cause for the creation of "glitches," which can be a cause for skew problems at the input.

Introduction of the Proposed Flip Flop design is a breakthrough in flip-flop technology utilizing novel pulse generation methodologies to improve performance and efficiency. Although the direct feed-through mechanism provides significant advantages in speed and functionality, safety precautions must be exercised to counter possible issues like glitches and skewing to guarantee the reliability and stability of the flip-flop operation in real systems.



Fi 4(b). Proposed Circuit

CHAPTER 5

SIMULATION RESULTS

All the simulations were done on Cadence Virtuoso tool at 90nm technology node. Given below are the brief details of the different type of analysis i.e Transient Analysis, AC analysis, DC analysis, and small signal analysis.

5.1 Different types of simulations

5.1.1 Transient Analysis:

Spectre enables transient analysis, which simulates the dynamic behavior of a circuit over time in response to input stimuli.

Designers can analyze circuit startup behavior, transient response to input signals, and transient phenomena such as ringing, overshoot, and settling time.

Transient analysis in Spectre provides insights into circuit performance under different operating conditions and helps identify potential issues such as signal distortion or instability.

5.1.2 AC Analysis:

Spectre supports AC analysis, which characterizes the frequency response of a circuit by analyzing small-signal behavior at different frequencies. Designers can perform AC analysis to determine the gain, phase shift, bandwidth, and frequency response of amplifiers, filters, and other frequency-dependent circuits.

AC analysis helps optimize circuit performance, tune filter responses, and ensure stability in feedback systems by analyzing frequency-dependent effects.

5.1.3 DC Analysis:

DC analysis in Spectre evaluates the DC operating point and DC voltage and current distributions in a circuit. It calculates node voltages, branch currents, and power dissipation under DC bias conditions, allowing designers to verify biasing circuits and ensure proper DC voltage levels.

DC analysis is essential for setting up initial conditions, verifying bias points, and checking DC voltage margins in analog and mixed-signal designs.

5.1.4. Small-Signal Analysis:

Spectre supports small-signal analysis, which analyzes the linearized response of a circuit to small perturbations around a DC operating point.

Designers can analyze small-signal parameters such as gain, input impedance, output impedance, and bandwidth to assess circuit linearity and stability.

Small-signal analysis is crucial for designing amplifiers, filters, and feedback systems, where linear behavior is essential for proper functionality.

Overall, Cadence Spectre simulation provides a comprehensive platform for analyzing, verifying, and optimizing analog, RF, and mixed-signal circuit designs. Its wide range of analysis capabilities, accuracy, and efficiency make it a valuable tool for designers working on complex electronic systems.

In this study, simulations were carried out using GPDK 90nm technology node, the flip flops that are observed with this node are ep DCO, CDFF, SCDFF, SFTFF and the proposed flip flop is noticed with 90nm technology node, utilizing Spectre, a renowned simulator within the Cadence Analog Design Environment. Spectre is widely recognized for its accuracy and reliability in analyzing the performance of analog and mixed-signal circuits, making it a preferred choice for evaluating the behavior of flip-flops in different technological contexts.

The simulation setup involved defining specific parameters for the clock signal and input data to assess the performance of the pulse-triggered flip-flops under consideration. The clock signal was characterized by a pulse width of 2 nanoseconds and a period of 4 nanoseconds, representing the duration and frequency of the clock pulses, respectively. Meanwhile, the input data signal exhibited a pulse width of 4 nanoseconds and a period of 8 nanoseconds, reflecting the timing characteristics of the data transitions.

Both the clock and input data signals were simulated at a voltage level of 1 volt, ensuring consistency in the electrical characteristics across the simulation environment. By specifying these parameters, the simulation aimed to replicate real-world operating conditions and evaluate the response of the pulse-triggered flip-flops under varying input conditions and technology node specifications.

Overall, the simulation methodology employed in this study offers a robust framework for evaluating the performance of pulse-triggered flip-flops and understanding their behavior under different technological constraints. By leveraging Spectre within the Cadence Analog

Design Environment and carefully defining simulation parameters, researchers can gain valuable insights into the effectiveness and suitability of pulse-triggered flip-flops for various digital circuit applications.

5.2 Output Waveforms:

The below waveform shows the output waveforms of the different pulse-triggered flip-flops: Each of the figures below from fig 5(a) through fig 5 (e) represents Clock, Data pulse and their respective output Q and Qbar at the positive edge of the clock.

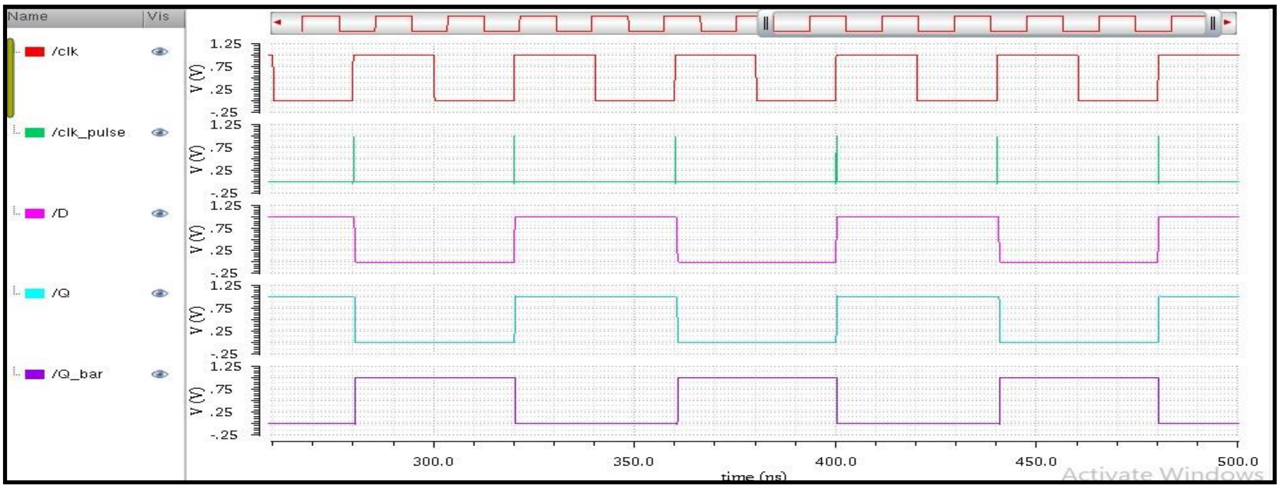


Fig 5.1 ep DCO

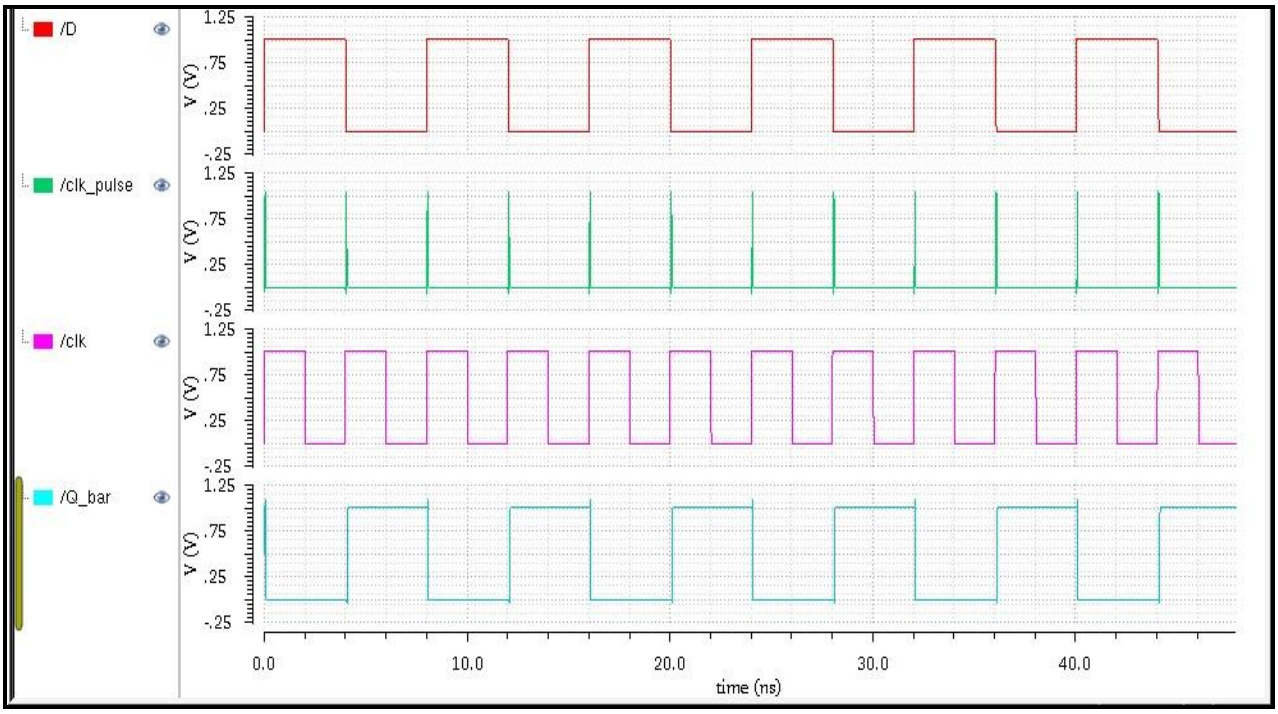


Fig 5.2 CDFF

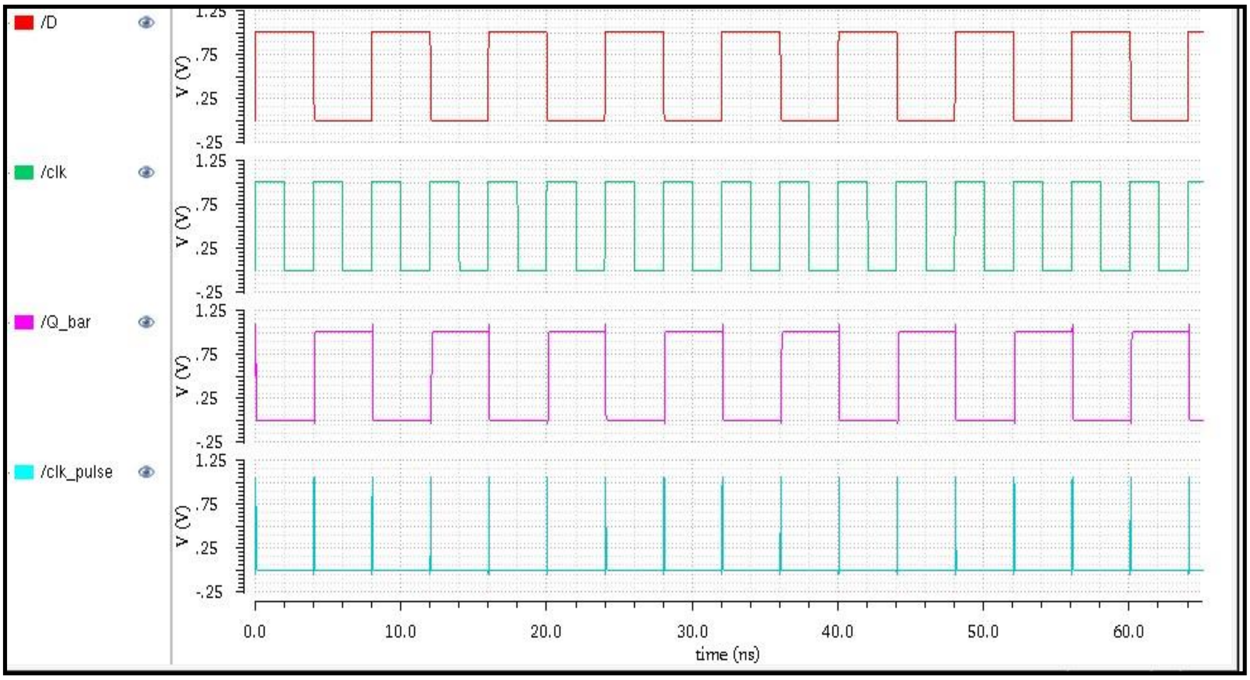


Fig 5.3 SCDFF

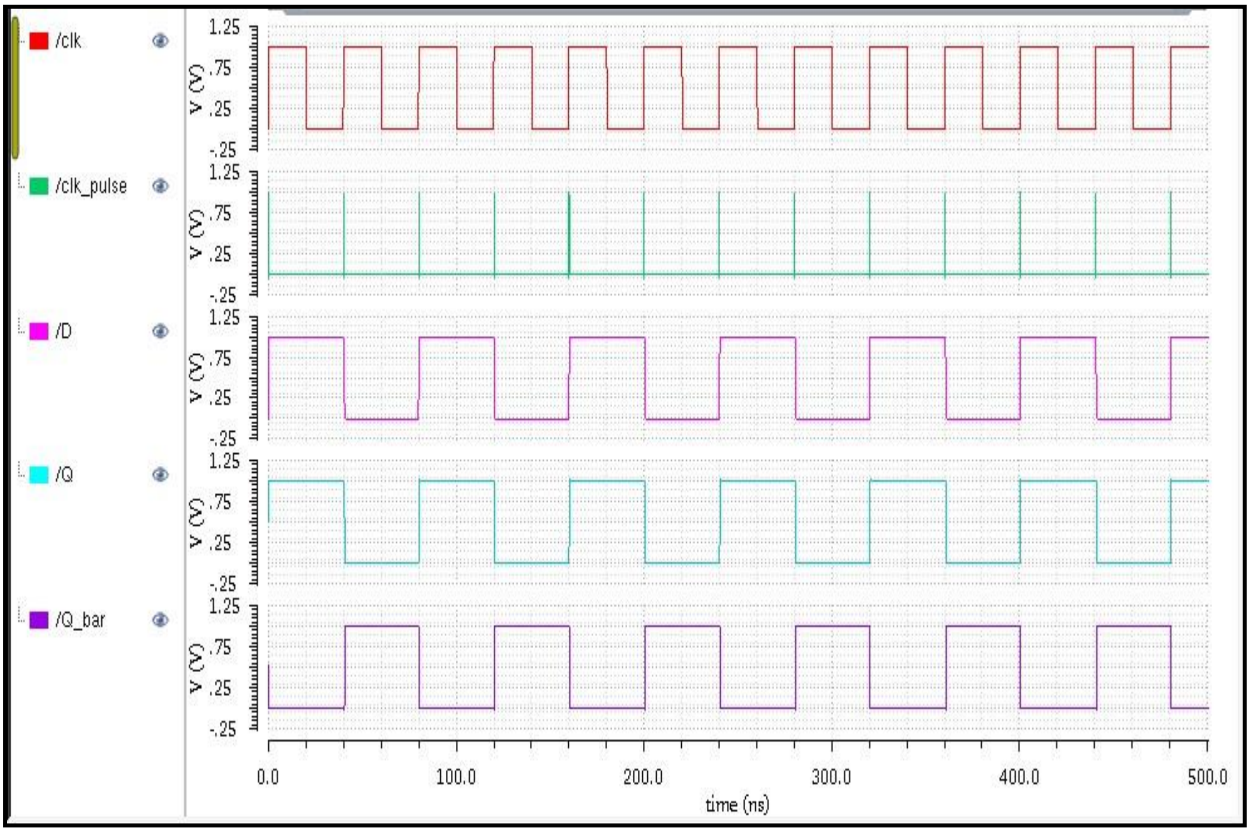


Fig5.4 SFTFF

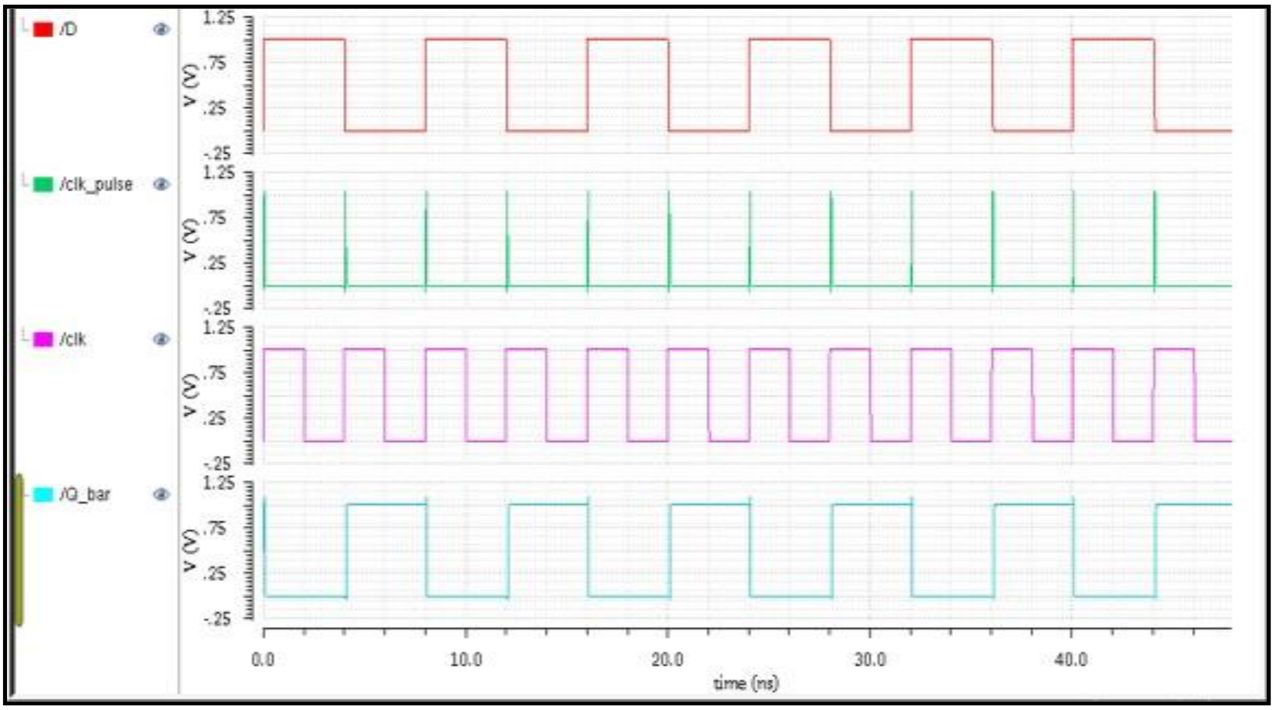


Fig 5.5 Proposed Flip Flop

5.3 Average Power Output Waveforms of different flip flops:

The below waveform in Fig. 5.6 to Fig. 5.10 shows the average waveforms of the different pulse-triggered flip-flops from this paper.

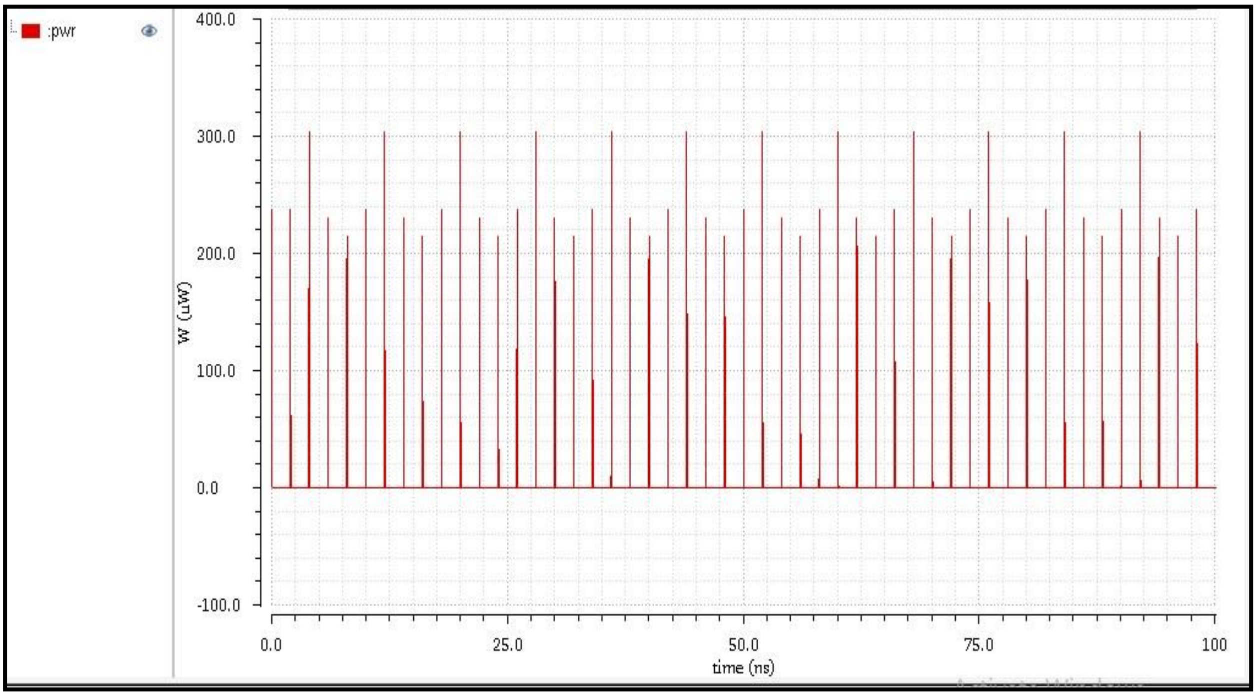


Fig 5.6 ep DCO

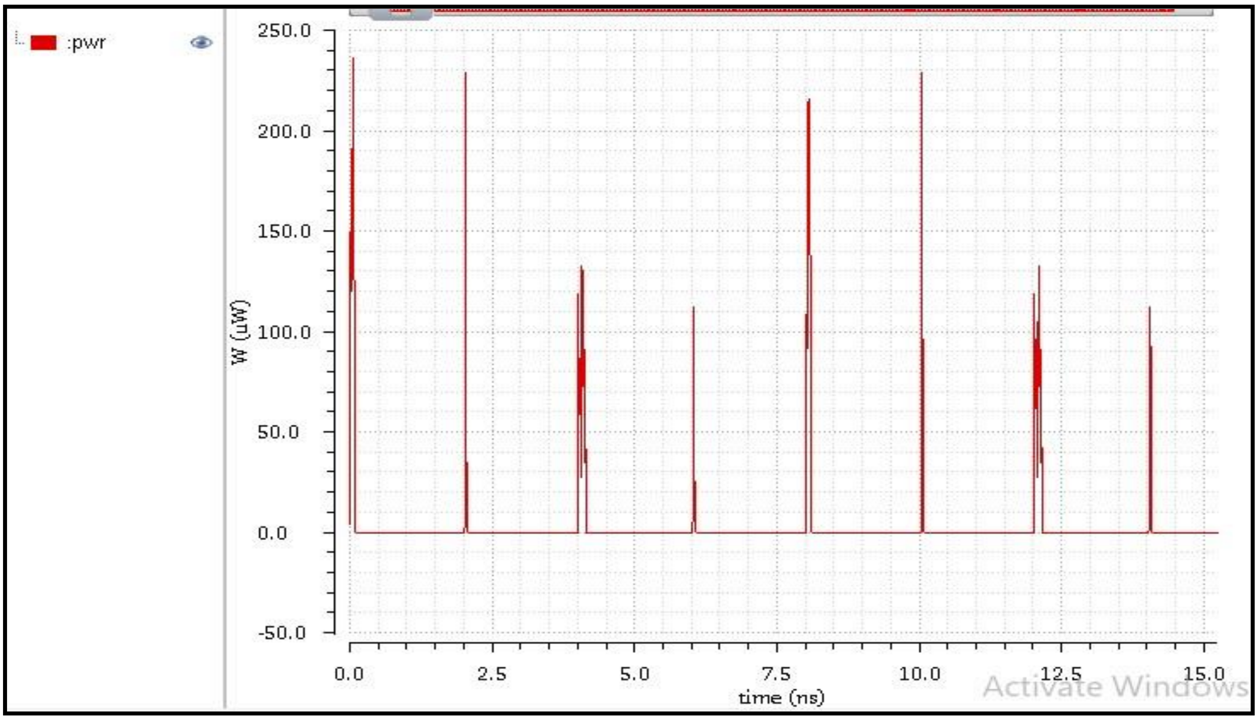


Fig5.7 CDFF

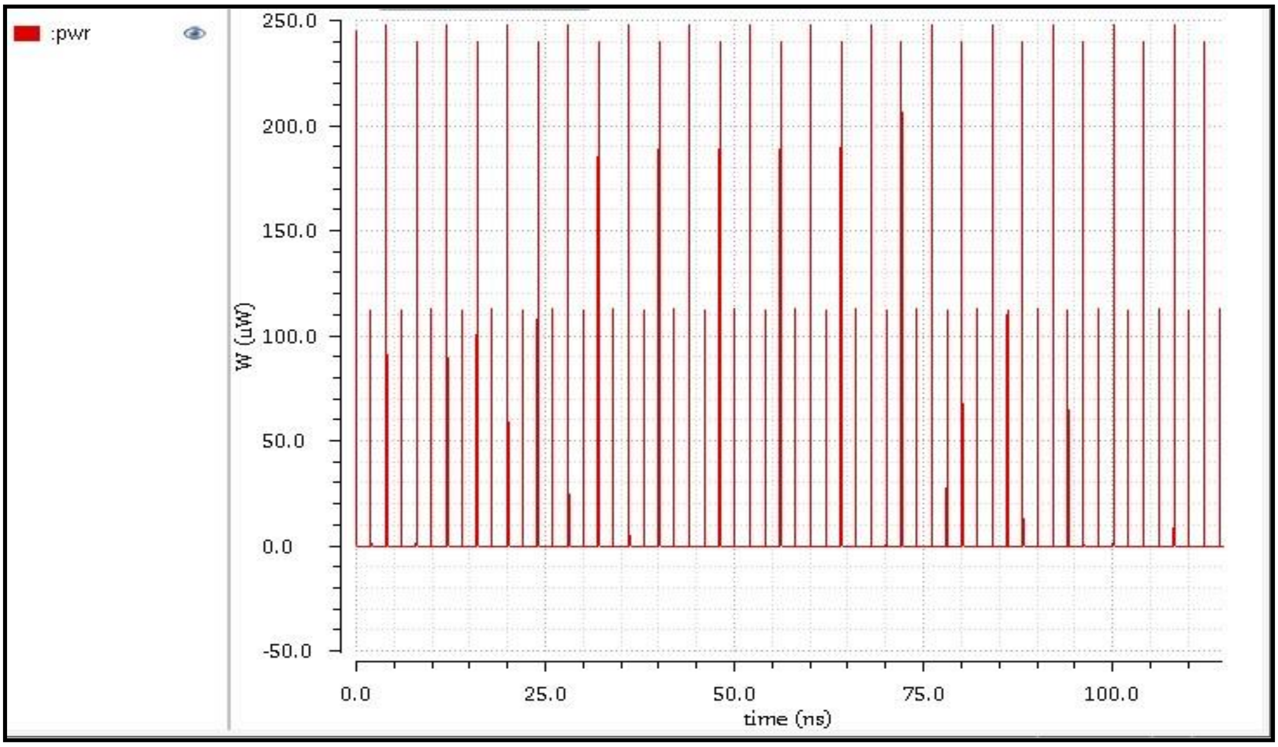


Fig5.8 SCDFF

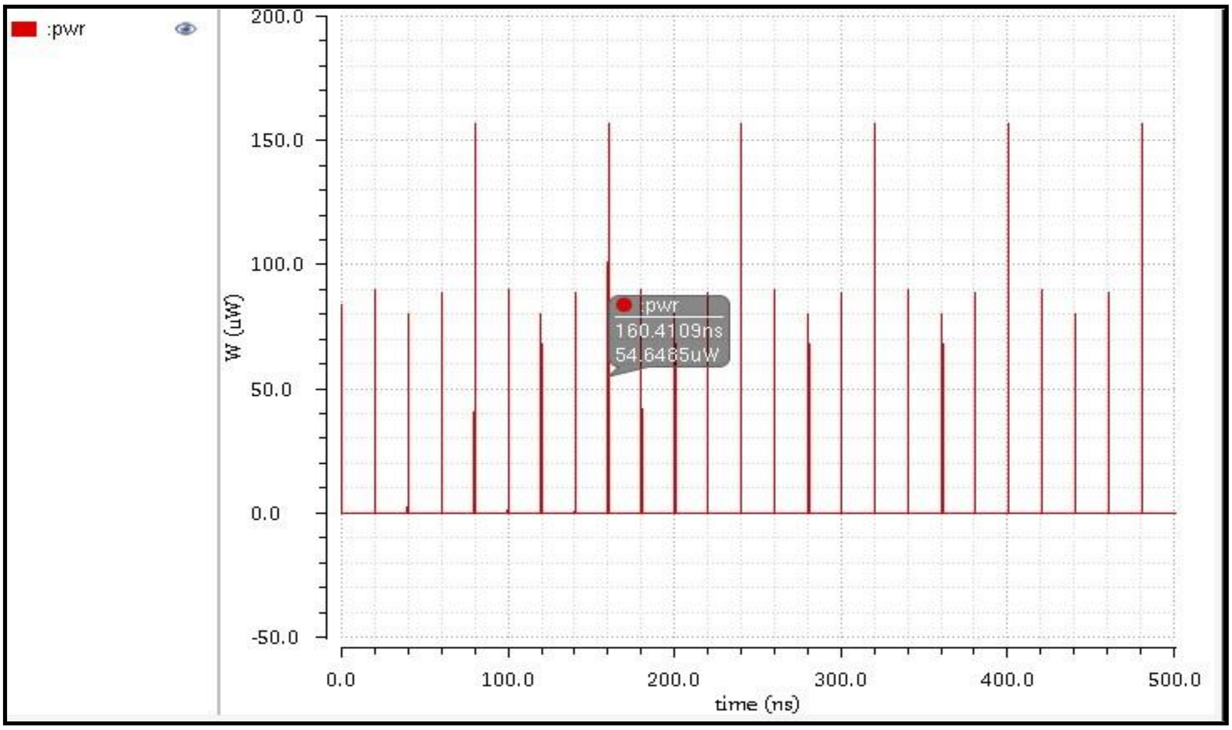


Fig 5.9 SFTFF

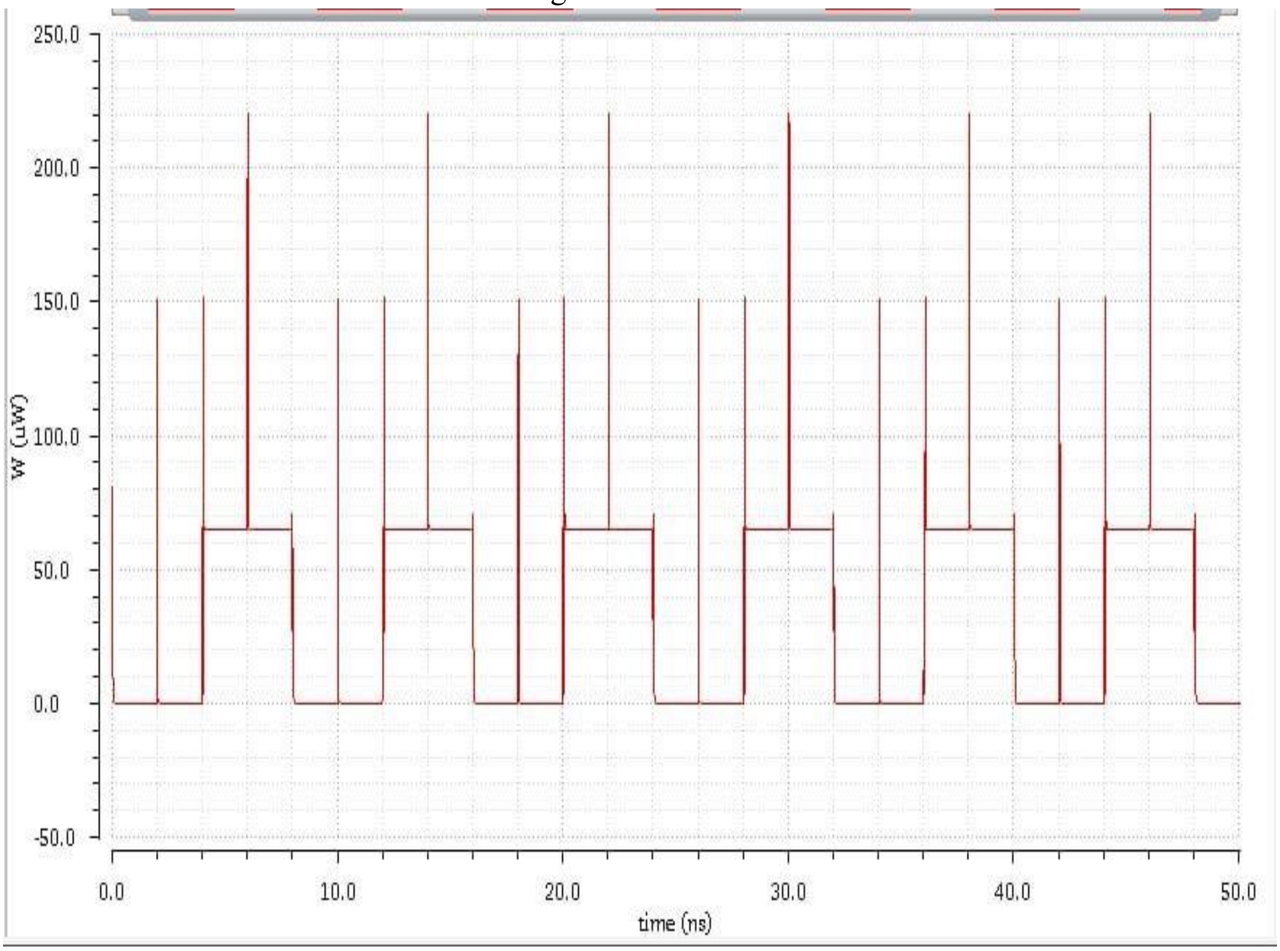


Fig 5.10 Proposed Circuit

MEASURED PARAMETERS

TABLE I. Observation table of Design Parameters at 90nm

P-FF	epDCO	CDFF	SCDFF	SFTFF	Proposed FF
Number of Transistor	28	30	31	24	15
Average power consumption(uW)	170.4	138.6	139.7	107.54	83.4
Minimum CLK-to-Q Delay (pS)	166.83	249.9	266.8	129.36	78
Minimum Data-to Q Delay (pS)	370.62	540	560	300	58.7
Power-Delay Product(fJ)	63.15	74.84	78.23	32.27	4.895

A. D-to-Q Delay Calculation (ps):

D2Q delay refers to the time required for input data (D) to propagate through the flip-flop and appear at the output (Q). It is primarily determined by the flip-flop's internal logic gate delays and interconnections, indicating the duration needed for the device to process and stabilize input data before it is reflected at the output. Figure 5(k) compares the D-to-Q latency of the Pulse triggered-FF design with the signal feed-through approach to that of other flip-flops, including ep-DCO, CDFF, and SCDFF. It is evident from the values provided in picoseconds that the P-FF architecture with signal feedthrough has lower latency.

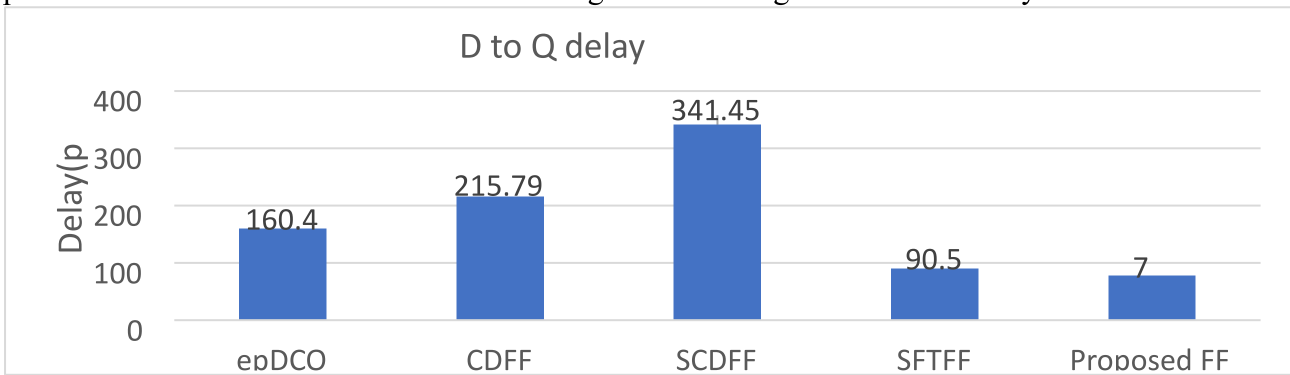


Fig 5.11 D to Q delay

B. Clk-to-Q Delay Calculation (ps):

48 68 CLK2Q delay refers to the time required for a change in the clock signal to travel through the flip-flop and influence the output (Q). It signifies the time interval between the clock edge activating the flip-flop and the subsequent alteration in the output. CLK2Q delay is essential for timing analysis in sequential circuits, as it establishes the maximum clock frequency and the overall efficiency of the circuit. Reduced CLK2Q delays facilitate higher clock frequencies and enhance circuit performance. Figure 5(l) compares the CLK-to-Q latency of the P-FF design using the signal 10 feedthrough technique to that of other flip-flops, particularly ep-DCO, CDFF, and SCDFF. It is evident from the values provided in picoseconds that the pulse-triggered FF architecture with signal feed-through has lower latency.

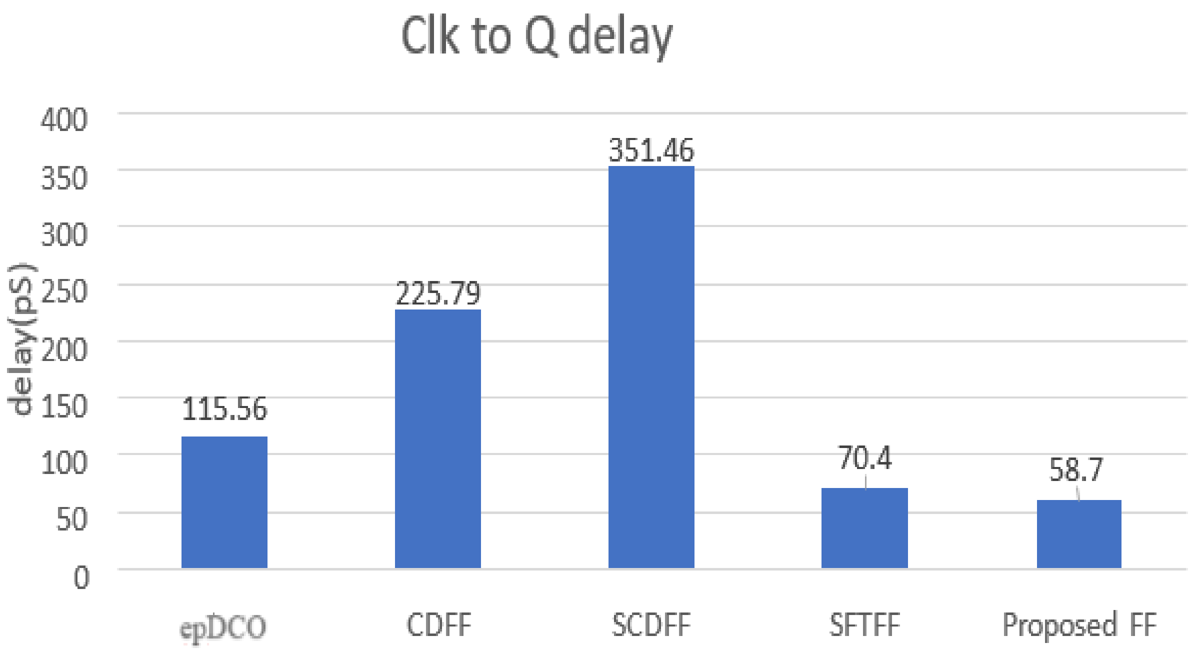


Fig 5.12 Clk to Q delay

C. Static Power Calculation:

21 Static power refers to the electrical energy consumed by a circuit even in the absence of switching activity—that is, when the circuit is in a quiescent state. Despite the removal of clock signals and constant input values, a persistent supply voltage ensures the circuit continues to draw 39 a certain amount of power, commonly known as static power consumption. Static power refers to the energy consumed when there is no activity within the circuit, or in other words, when the circuit is in a quiescent state. Even in the presence of a supply voltage, the circuit will continue to draw some power, known as static power consumption, even if the clocks are removed and the inputs remain unchanged. This power consumption primarily arises from leakage currents that occur when the transistor is in the off state. Figure 5(m) illustrates the conventional P-FF static power. The FF design, which employs the signal feed-through approach, consumes less average static power than the traditional pulsed flip-flop CDFF, SCDFF, and ep-DCO designs. Every value is stated in nanowatts(nW).

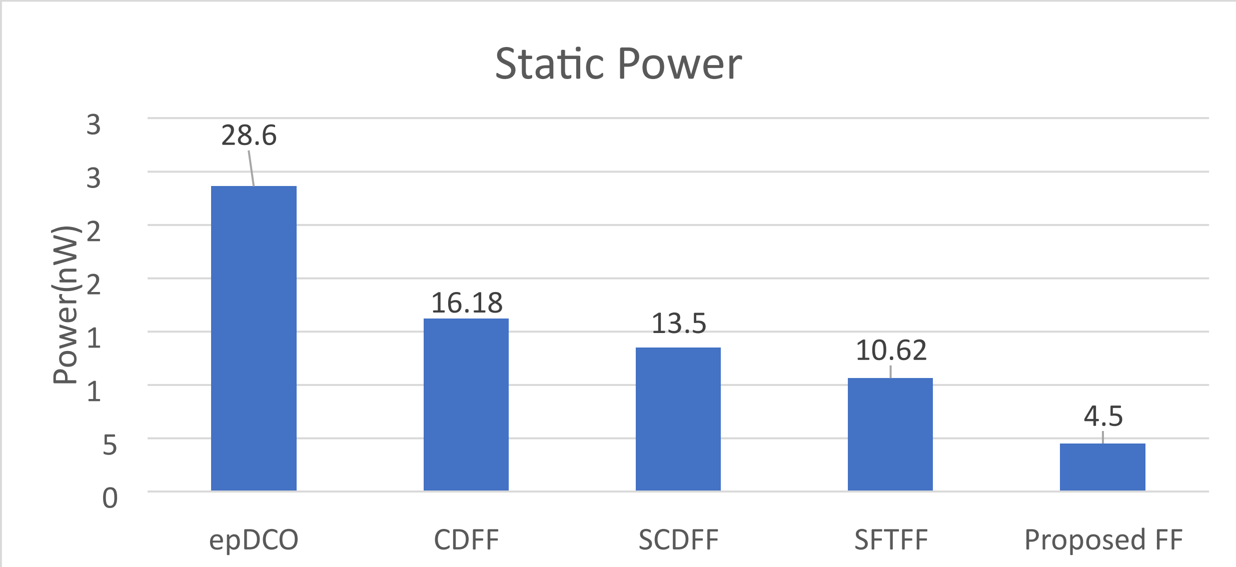


Fig 5.13 Static Power

D. Dynamic Power Calculation:

Dynamic power refers to the power utilized when the circuit is active, indicating that we have supplied voltage, applied a clock signal, and altered the inputs. This power primarily arises from dynamic currents, including capacitance currents (also known as switching power) and short-circuit currents (referred to as short-circuit power). As shown in Figure 5(n), both PTFF designs implemented using the signal feed-through technique utilize significantly less dynamic power than other pulse-triggered flip-flops, such as ep-DCO, CDFF, and SCDFF. All values are expressed in microwatts.

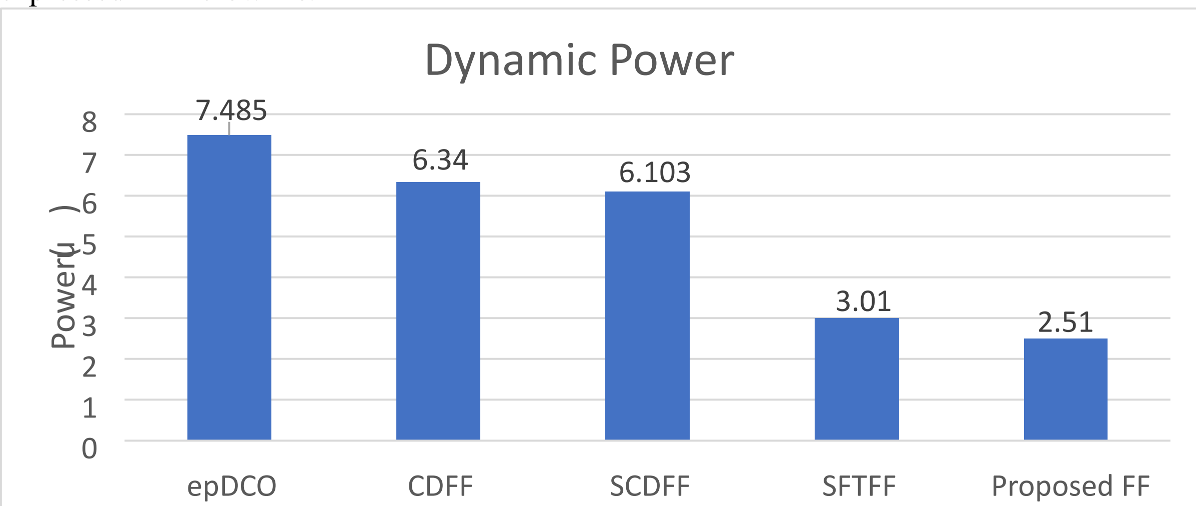


Fig 5.14 Dynamic Power

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1. Conclusion

This research undertakes a comprehensive comparison of four explicit pulsed flip-flops (P-FF) operating at 90nm technology nodes, shedding light on their efficacy through detailed analysis of experimental observations. Among the currently available flip-flops, the Signal Feedthrough Flip-Flop (SFTFF) emerges as a standout performer, boasting superior attributes across various metrics. The SFTFF implementation stands out in terms of efficiency, utilizing only 24 transistors—remarkably fewer than its contemporaries. This streamlined architecture yields significant benefits: the SFTFF achieves the lowest measured power consumption of 107.59µW and demonstrates the fastest operation at 300ps on the 90nm process node, outperforming other pulse flip-flop (P-FF) designs at this scale.

Furthermore, the study introduces a novel flip-flop design that offers compelling advantages over existing alternatives. With a minimalist structure utilizing just 15 transistors, this proposed flip-flop demonstrates notable improvements in power efficiency and operational speed. At the 90nm node, it achieves substantial power savings, consuming only 83.4µW.

In summary, the proposed circuit designs not only minimize transistor count and power consumption but also enhance performance, underscoring their potential impact in advanced digital systems. Furthermore, it achieves unparalleled operational speed, reaching an impressive 78ps, surpassing all current P-FF designs in this aspect.

In conclusion, the study's comparative analysis reveals the significant performance disparities among various explicit P-FF designs, with the SFTFF and the proposed flip-flop emerging as clear frontrunners. Both designs showcase remarkable efficiency, characterized by minimal transistor count, low power consumption, and high-speed operation. These findings underscore the importance of innovative design approaches in enhancing the performance and efficiency of flip-flop devices, particularly in power-sensitive and high-speed applications.

6.2. Future Scope

This research has laid the groundwork for understanding a few explicit PTFFs and designed a novel flipflop with lesser power and transistor count, but several opportunities remain for future exploration and development.

I. Design on different nodes: The proposed explicit PTFF design can be implemented across various technology nodes, such as 45nm and 22nm, to evaluate its scalability and adaptability. Further research can be conducted to analyze key performance metrics—including power consumption, propagation delay, and overall efficiency—under different technological conditions.

II. Potential for Design Optimization: The current design presents opportunities for further refinement aimed at reducing power consumption, minimizing delay, and lowering the overall transistor count. Future enhancements can focus on optimizing these parameters to achieve greater efficiency and performance.

III. Multi-Technology Node Evaluation: Beyond 45nm and 22nm, the design can undergo further evaluation on advanced nodes like 14nm, 7nm, and even technologies based on FinFET or GAAFET to assess its performance in state-of-the-art fabrication environments.

IV. Temperature and Voltage Scaling Analysis: Future research may investigate the performance of the novel PTFF design and others under different temperature and voltage conditions to guarantee reliable operation in a variety of real-world situations.

V. Integration in Larger Systems: The novel PTFF can be employed in larger system like processors or memory arrays to evaluate its impact on overall performance of the system , power consumption and timings.

VI. Clock Gating and Power Gating Techniques: The implementation of sophisticated low-power strategies, including clock gating and power gating, may be investigated to achieve additional reductions in dynamic and leakage power during idle states.

REFERENCES

1. K. John, V. K. R.S. and K. S.S., "Performance Comparison of Explicit Pulsed FlipFlops in Low Power and High-Speed Applications," 2018 International Conference on Circuits and Systems in Digital Enterprise Technology (ICCSDET), Kottayam, India, 2018, pp. 1-6, doi: 10.1109/ICCSDET.2018.8821226.

2. Peiyi Zhao, T. K. Darwish and M. A. Bayoumi, "High-performance and low-power conditional discharge flip-flop," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 5, pp. 477-484, May 2004, doi:10.1109/TVLSI.2004.826192.

3. H. Panwar, N. S. Singha and M.K. Singh, "Performance Comparison of high Speed and Low Power Pulse-Triggered Flip Flops and a Pulse Flip Flop with Signal Feed through Technique", 2024 Parul International Conference on Engineering and Technology(PICET), Vadodara, India, 2024, pp. 1-6, doi: 10.1109/PICET60765.2024.10716123

4. Keerthana K., Shanmugaraja M. and MaheshKannan P., "Comparison of conventional flip flops with pulse triggered generation using signal feed through technique," 2015 International Conference on Communications and Signal Processing (ICCSP), Melmaruvathur, India, 2015, pp. 0392-0397, doi: 10.1109/ICCSP.2015.7322915

5. Nitin Kumar Saini and Kamal K. Kashyap, " Low power dual edge triggered flip-flop" in 2014 International Conference on Signal Propagation and Computer Technology (ICSPCT 2014), Ajmer, India, July 2014, doi: 10.1109/ICSPCT.2014.6885022

6. J.VISHALAXMI and P.K. SURESH, "Performance of Pulse Triggered Flip-flop based on Signal Feed through Technique to Improve Delay", International Journal of advance Technology and Innovative Research, December 2016, pp. 4405-4409, Vol.08,Issue.23, ISSN 2348–2370

7. M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A lowpower stalic dual edge triggered flipflop using an output-controlled discharge configuration, " in Proc. IEEE Tnt. Symp. Circuits Syst., May 2005, pp. 2429- 2432.

8. Peiyi Zhao, T. K. Darwish and M. A. Bayoumi, "High-performance and low-power conditional discharge flip-flop," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 12, no. 5, pp. 477-484, May 2004, doi: 10.1109/TVLSI.2004.826192.

9. D. Pan, C. Ma, L. Cheng and H. Min, "A Highly Efficient Conditional Feedthrough Pulsed Flip-Flop for High-Speed Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 1, pp. 243-251, Jan. 2020, doi:10.1109/TVLSI.2019.2934899.

10. J. -F. Lin, "Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal FeedThrough," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 1, pp. 181-185, Jan. 2014, doi: 10.1109/TVLSI.2012.2232684.

11. C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi and Y. Oowaki, "Conditional Data Mapping Flip-Flops for Low-Power and High-Performance Systems," in IEEE

Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 12, pp. 1379-1383, Dec. 2006, doi: 10.1109/TVLSI.2006.887833.

12. Bai-Sun Kong, Sam-Soo Kim and Young-Hyun Jun, "Conditional-capture flip-flop technique for statistical power reduction," 2000 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056), San Francisco, CA, USA, 2000, pp. 290-291, doi: 10.1109/ISSCC.2000.839785.

13. P. Bikki and P. Karuppanan, "Analysis of low power feed through logic with leakage control technique," 2017 4th International Conference on Power, Control & Embedded Systems (ICPCES), Allahabad, India, 2017, pp. 1-6, doi: 10.1109/ICPCES.2017.8117631.

14. G. Shin, E. Lee, J. Lee, Y. Lee and Y. Lee, "A Differential Flip-Flop with Static Contention-Free Characteristics in 28 nm for Low-Voltage, Low-Power Applications," in IEEE Journal of Solid-State Circuits, vol. 58, no. 5, pp. 1496-1504, May 2023, doi: 10.1109/JSSC.2022.3219091.

15. P. Verma and A. K. Mishra, "Implementation and Analysis of Efficient Low Power Dynamic Circuit Technique," 2021 2nd International Conference on Smart Electronics and Communication (ICOSEC), Trichy, India, 2021, pp. 582-587, doi:10.1109/ICOSEC51865.2021.9591737.

16. F. Moradi, D. Wisland, J. Kargaard Madsen and H. Mahmoodi, "Flip-flop design using novel pulse generation technique," 2012 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012), Seville, Spain, 2012, pp. 685-688, doi: 10.1109/ICECS.2012.6463633.

17. I. P. Macfarlane, "Pulse Generator and Flip-Flops," in IEEE Transactions on Instrumentation and Measurement, vol. 21, no. 2, pp. 148-153, May 1972, doi: 10.1109/TIM.1972.4313985.

18. A. S. Seyedi, S. H. Rasouli, A. Amirabadi and A. Afzali-Kusha, "Clock gated static pulsed flip-flop (CGSPFF) in Annual Symposium on Emerging VLSI Technologies and Architectures (ISVLSI'06), Karlsruhe, Germany.