

DESIGN AND PERFORMANCE ANALYSIS OF SAR ADC FOR LOW POWER APPLICATIONS

**A Thesis Submitted
In Partial Fulfillment of the Requirements for the Degree of**

DOCTOR OF PHILOSOPHY

By

**MOHIT TYAGI
(2K18/PHDEC/510)**

Under the Supervision of

**Joint Supervisor
Prof. Parvin Kumar
Professor, ECE, KIET**

**Supervisor
Prof. Poornima Mittal
Professor, ECE, DTU**



Department of Electronics and Communication Engineering

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daulatpur, Main Bawana Road

Delhi-110042. India

April, 2026

ACKNOWLEDGEMENTS

I would like to express my deepest gratitude and sincere appreciation to all those who have contributed to the completion of my doctoral thesis. Their guidance, support, and encouragement have been invaluable throughout this journey.

First and foremost, I am sincerely thankful to my supervisor, Prof. Poornima Mittal, Professor, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India. I hereby acknowledge her exceptional guidance and continuous support throughout my research journey. I am truly grateful for her dedication, patience, and constant encouragement. Her valuable insights, extensive knowledge, and thoughtful suggestions have played a significant role in enhancing the quality of my work. What I value the most is her unwavering support—always being there to guide me, inspire me during difficult moments, and rejoice in every small milestone I achieved. I feel extremely fortunate and honored to have such a motivating and supportive mentor. Her commitment has illuminated my path, and her encouragement has empowered me to aim higher and achieve more.

I would like to extend my profound thanks to my joint supervisor, Prof. Parvin Kumar, Professor, Department of Electronics and Communication Engineering, KIET Group of Institutions, Delhi-NCR, Ghaziabad, India. His guidance and insightful feedback were crucial to the growth and completion of my research work. It has been a privilege to learn and work under his supervision. I am deeply thankful for their supportive nature and valuable contributions, which have been a source of motivation and inspiration throughout my journey.

I express my gratitude towards the distinguished faculty members who have, time and again, guided us in various aspects of our journey. I extend my sincere regards to HoD Madam, for her constant support. I wish to express my gratitude towards the DRC chairperson, the distinguished DRC members. Their expertise, constructive criticism, and valuable suggestions have significantly contributed to the refinement of my thesis. I am deeply grateful for the time and effort they devoted in reviewing and evaluating my work.

I am obliged to the esteemed faculty members of Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, who provided me with a rich academic environment and facilitated my cognitive growth. Their lectures, discussions and seminars have expanded my horizons and shaped my research interests.

I express my deepest regards for Prof. Brijesh Kumar, Department of Information Technology, Indira Gandhi Delhi Technical University, Delhi, India, for investing his valuable time and efforts in providing deep and insightful remarks.

I am also grateful to all my colleagues of the Electronics and Communication department, especially Ms. Sugandha Yadav, Mr. Paritosh Chamola, Mr. Ashish Raturi, Ms. Bhawna Rawat, Ms. Yogita Chopra, Mr. Ayush, Ms. Bharti, Ms. Aparna, and Ms. Archana. I am thankful to them as they have generously contributed their time and shared their insights, without whom my study would not have been possible.

Most importantly, I dedicate this work to my Father Late Shri Suresh Chand tyagi (Advocate) who will always remain a role model of my life. His teaching to remain calm even in the most challenging phase of our life will always be with me throughout my life. His words “keep doing good work for the wellbeing of not only ours but for others too” always remain close to me. I fondly remember my uncle, Late Shri Naresh Chandra Tyagi, who always showed keen curiosity about my Ph.D. journey, often asking, “When will your Ph.D. be completed?” Also, I am deeply grateful to my mother; Mrs. Savita Tyagi, who has dedicated her life for our wellbeing, my wife; Dr. Shaily, who is always a strong support system with me and my two lovable Son’s; Reyansh & Dakshith for their patience, understanding, love & encouragement during the research work. Finally, I would like to thank my elder brothers; Sachin & Sunil, my lovable nieces; Ishani & Nitya, my cousins; Divya & Shivam for the love and motivation they showed in my life to carry out the research in a light, easy-going atmosphere.

Finally, I gratefully acknowledge the financial support provided by Delhi Technological University, Delhi. Their assistance helped me to carry out my research effectively and ensured that I had the necessary resources to complete my thesis. Last but not the least, I express my heartfelt gratitude to the Almighty for granting me the inner strength, love, peace, and wisdom to always improve myself.

To all those who have directly or indirectly contributed to my doctoral thesis, I extend my deepest gratitude. Your support, whether big or small, has played a significant role in shaping my academic and personal growth. I am profoundly grateful for your presence in my life and for the impact you have had on my journey as a researcher.



MOHIT TYAGI

(Roll No. 2K18/PHDEC/510)



DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-42

CANDIDATE'S DECLARATION

I, **Mohit Tyagi (2K18/PHDEC/510)**, hereby certify that the work which is being presented in the thesis entitled “**Design and Performance Analysis of SAR ADC for Low Power Applications**”, in partial fulfilment of the requirements for the award of the Degree of **Doctor of Philosophy**, submitted in the Department of **Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **31st December 2018** to **28th April 2026** under the supervision of **Prof. Poornima Mittal, Professor, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India** and **Prof. Parvin Kumar, Department of Electronics and Communication Engineering, Krishna Institute of Engineering & Technology (KIET), Ghaziabad, Delhi-NCR, Uttar Pradesh, India**. The matter presented in the thesis has not been submitted by me for the award of any other degree of this or any other Institute.

Date: 28-04-2026

Place: Delhi, India

MOHIT TYAGI

(Roll No. 2K18/PHDEC/510)

This is to certify that the student has incorporated all the corrections suggested by the examiners in the thesis and the statement made by the candidate is correct to the best of our knowledge.

Signature of Jt. Supervisor

Signature of Supervisor

Signature of External Examiner



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daultpur, Main Bawana Road, Delhi-42

CERTIFICATE BY THE SUPERVISOR(s)

Certified that **Mohit Tyagi (2K18/PHDEC/510)** has carried out his research work presented in this thesis entitled “**Design and Performance Analysis of SAR ADC for Low Power Applications**”, for the award of **Doctor of Philosophy** from Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, under our supervision. The thesis embodies results of original work, and studies are carried out by the student himself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

A handwritten signature in blue ink, appearing to read "Parvin Kumar", with a horizontal line underneath.

PROF. PARVIN KUMAR

Joint Supervisor

Department of ECE

Krishna Institute of Engineering & Technology
(KIET)

Delhi-NCR, Uttar Pradesh, India

A handwritten signature in blue ink, appearing to read "Poornima", with a horizontal line underneath.

PROF. POORNIMA MITTAL

Supervisor

Department of ECE

Delhi Technological University
Delhi, India

Date: 28-04-2026

ABSTRACT

Analog to Digital Converter (ADC) is an important module in the analog front end system that exists between sensors and digital signal processing block. Different architectures of ADCs like Flash, Pipelined, Delta Sigma and Successive Approximation Register (SAR) exist in literature that are utilized for digitization of an analog signal. Moreover, parameters like power consumption, resolution, area, and design cost are considered for the comparison between different existing ADC architectures. Literature indicates that for medium resolution and medium speed applications at low power consumption, SAR ADC is the most suitable choice due to its predominantly digital architecture. In view of these considerations, design of an ultra-low power SAR ADC is undertaken in this research work.

A SAR ADC consists of three primary modules: a low-power dynamic comparator, a capacitor-based digital-to-analog converter (CDAC), and a control logic unit that governs the successive approximation process to convert the sampled analog input into its corresponding digital representation. Power consumption of each and every module is required to be reduced so as to reduce the power of complete designed ADC. However, DAC is the most power consuming block in a SAR ADC, design and parametric optimization of each and every module is considered stepwise. First of all, design and parametric simulation analysis of different low power dynamic comparators in CADENCE Virtuoso 45 nm technology node is carried out. In this, Strong arm latch dynamic comparator is considered as the baseline comparator consisting of preamplifier and regeneration latch. This comparator retains the direct path connection between V_{DD} and ground and due to this, the circuit consumes 51.38 nW of average transient power consumption. Further, double tail dynamic comparator and modified double tail dynamic comparator are considered for design, simulation & analysis and the transient analysis of both comparators is focussed. The observed delay, power consumption and kickback noise in these comparators required an architectural improvement in the design of existing comparators. Following this, first proposed dynamic comparator architecture design along with the simulation analysis is focussed.

Simulation of first proposed dynamic comparator observed average transient power of 33.81 nW at nn corner which is much reduced value compared to the other architectures like strong arm latch, double tail dynamic and modified double tail dynamic comparator. The power consumption is limited to 19.56 nW at ss corner as the architecture created an isolation between pre-amplifier and latch module when clk is low due to which leakage power is avoided. The

proposed comparator is simulated with capacitive loading of 5.1 pF which is the required value for utilizing the designed comparator module along with capacitive DAC. PDP of 0.4 fJ along with temperature variation from -40-degree centigrades to 110-degree centigrades is also measured for the first proposed comparator.

Further, a dynamic comparator based on charge sharing logic and kickback noise reduction logic is also proposed which is working well for few GS/s and power consumption of 9.36 μ W is observed at 1 GS/s. Proposed charge sharing logic based dynamic comparator is limiting offset voltage to 7.8 mV and delay within 48.2 ps. Proposed charge sharing logic-based circuit is less sensitive to V_{cm} variations as gm/I_D of input transistors is enhanced with the biasing of transistors in weak inversion region. The observed delay exhibits a reduction from 56.3 ps to 23.17 ps as the input differential voltage (V_{diff}) ranges from 10 mV to 200 mV for varying common-mode voltage levels (V_{cm}) in the proposed charge sharing dynamic comparator. The comparator demonstrated the reduction in kickback noise by employing auxiliary transistors M8 and M9 (Fig.3.12) to separate the output nodes. Additionally, this approach effectively mitigated the mismatch effect and minimized the impact of parasitic capacitance associated with the transistor design.

Further, designing of DAC module with reduced switching energy per conversion step drew attention of researchers in the design of ultra-low power SAR ADC. In literature many DAC switching schemes are implemented by the researchers like common mode switching scheme, monotonic switching scheme, capacitor splitted switching scheme, merged capacitor etc. Each switching scheme followed a different switching methodology and contributed to the saving of switching energy per conversion cycle compared to the conventional one. Traditional switching scheme consume $682.5 CV_{ref}^2$ while $427.66 CV_{ref}^2$ of switching energy is consumed by split capacitor technique. So, there exists a research scope in the design of DAC unit with zero switching energy in the first two MSB comparisons.

In view of above, inclusion of single ended topology-based switching scheme for the design of digital to analog converter (DAC) is considered. The proposed switching scheme utilized a single reference voltage of $V_{ref}/2$ and performed the first two MSB comparisons with zero switching energy. The scheme required average of $57.4 CV_{ref}^2$ of switching energy which is a much-reduced value, approximately reduced by a factor of 92 percent compared to conventional capacitor-based switching scheme. Also, compared to conventional switching scheme, the number of capacitors in the DAC array are reduced by 50 percent.

In the switching scheme, a single ended behaviour is obtained utilizing a dummy DAC at the positive input of comparator that facilitated first two comparisons without any switching power. Also, after first comparison of V_{in} with $V_{ref}/2$, the bottom plate of dummy DAC is switched either to ground or $V_{ref}/2$ and stayed in that state till the final digitization is performed with V_{ref} value of 1.1 V. Also, for the proposed DAC implementation, MOM capacitors are suggested to be the preferred choice to shift the design from schematic to final back-end stage.

Third Module of SAR ADC is the design of a low power control unit. The literature observed the necessity of SAR logic and DAC co-optimization, especially when advanced switching techniques such as monotonic, common-mode (V_{CM})-based, and capacitor-splitting schemes are employed for switching. Based on the above requirement to design a SAR logic-based control unit with better DAC-logic synchronization and to further reduce nonlinearity in SAR ADC, the design of low power SAR logic-based control unit is considered as further part of the research work. The design of the control unit began with the development of enhanced D flip-flops to improve setup and hold time performance. After this, the clocking system is designed using the main clock along with internally generated clock signals to achieve proper timing synchronization. In the initial stage, multiplexers and sampling logic are implemented to support accurate sampling and signal control. The SAR logic is then generated step by step in a bitwise manner to implement the proposed switching scheme. Finally, by using enhanced D flip-flops and multiplexers with proper synchronization, an improved control unit is developed to successfully implement the proposed switching scheme.

Enhanced D flip flop is working well for the required bandwidth and resolution of input signal at low power consumption. The proposed synchronous control unit has less complexity and better timing synchronizations due to which all the control signals are getting generated within time constraints. Sampling phase begins the digitization process when X_s is low and D_p (comparator output) is the digitized output bit which is generating digital data in synchronization with internal generated clock signals (Q1 to Q7) and providing better linearity in the digital data generation process. The control unit implemented the SAR logic in a bitwise manner. After the initial sampling operation triggered by the first clock signal (clk), the most significant bit (MSB) is resolved. Subsequently, the internal clock signal Q1 provides precise timing synchronization for the generation of the MSB-1 bit. The remaining bits are generated sequentially by the control unit with optimized timing coordination between the DAC and the comparator, thereby improving conversion accuracy. In this process, the internal clock signal Q2 synchronizes the generation of the MSB-2 bit, and the same sequence continued for the

lower-order bits. The resolved digital bits are stored in a shift register, and based on the clock timing, the stored data is finally read out as an 8-bit digital output of the designed SAR ADC.

Proper interfacing of the designed modules along with effective control of the common-mode V_{cm} is critical for achieving an ultra-low-power SAR ADC. In this work, non-linearities such as differential non-linearity (DNL) and integral non-linearity (INL) are minimized while maintaining low power consumption, in line with observations reported in the literature. The effectiveness of the proposed approach is reflected in the calculated INL and DNL values obtained from the digitized output. Based on these considerations, a fully interfaced 8-bit SAR ADC incorporating all optimized modules is designed.

Henceforth, finally, all the designed modules; comparator, DAC & control unit are interfaced to design an 8-bit SAR ADC with single reference voltage $V_r/2$ based dummy DAC designed along with bootstrap switch to give zero switching energy in first two MSB conversions. The reduced power consumption of the designed 8-bit SAR ADC is limited to the value of $5.38 \mu W$. Parametric simulation analysis shows that SNDR value of 46.08 dB, SFDR 47.89 dB, ENOB 7.38 bits, DNL $+0.13/(-0.12)$ LSB, INL $+0.52/(-0.90)$ LSB at sampling rate of 540 KS/s is obtained. The entire design is simulated in CADENCE 45 nm technology node. The Proposed SAR ADC is completely designed at transistor level implementation of each module including comparator, DAC unit and control logic. The DAC unit consumes zero switching energy in the first two MSB decisions as per proposed switching algorithm which results in the saving of 92 % of switching energy with respect to the conventional switching scheme at 540 KS/s. The research conducted herein shows that the proposed 8-bit SAR ADC is digitizing the analog sampled value in 8 bits with sampling frequency of the order 540 KS/s. The measured parameters validating that power consumption of the designed ADC is limited to $5.38 \mu W$ and other parameters like INL, DNL are also within permissible range to confirm the effectiveness of the design for low power sensor applications. The research widens the horizon to include adaptive decision algorithms in the design that can help mitigate non-idealities such as capacitor mismatch and comparator offset in further research.

Table of Contents

Title	Page No.
Acknowledgement	ii
Candidate's Declaration	iv
Certificate by the Supervisor(s)	v
Abstract	vi
List of Figures	xiv
List of Tables	xvii
List of Abbreviations	xviii
List of Symbols	xix
CHAPTER 1: INTRODUCTION	1 – 15
1.1 BRIEF OVERVIEW OF ANALOG TO DIGITAL CONVERTERS	1
1.2 ARCHITECTURAL DIVERSITY FOR DIFFERENT ADC	3
1.3 PERFORMANCE PARAMETERS OF ADC	5
1.4 PROBLEM STATEMENT	8
1.5 OBJECTIVES	9
1.6 OBJECTIVE-WISE METHODOLOGY	10
1.7 THESIS ORGANIZATION	12
CHAPTER 2: LITERATURE REVIEW	16 – 48
2.1 BRIEF INTRODUCTION ABOUT CHAPTER	16
2.2 OVERVIEW OF ANALOG-TO-DIGITAL CONVERTERS AND THEIR ARCHITECTURES	17
2.3 DIFFERENT MODULES OF SAR ADC	22
2.4 DIFFERENT EXISTING DYNAMIC COMPARATORS FOR SAR ADC	23
2.5 ARCHITECTURE OF MAJOR EXISTING DYNAMIC COMPARATORS	26
2.6 EXISTING LOW POWER SWITCHING TECHNIQUES FOR DAC DESIGN	32
2.7 DIFFERENT CAPACITOR LAYOUTS FOR DAC DESIGN IN LITERATURE	37

2.8	CAPACITOR MISMATCH REDUCTION TECHNIQUES	38
2.9	REVIEW OF SAR LOGIC BASED CONTROL UNIT DESIGNS	39
2.10	REVIEW OF EXISTING SAR ADC DESIGNS AND TECHNIQUES	42
2.11	RESEARCH GAPS	47
CHAPTER 3: DESIGN AND ANALYSIS OF LOW POWER DYNAMIC COMPARATOR FOR SAR ADC		49-84
3.1	BRIEF INTRODUCTION ABOUT CHAPTER	49
3.2	OVERVIEW OF DYNAMIC COMPARATORS FOR ANALOG TO DIGITAL CONVERTERS (ADCS)	51
3.3	WORKING AND PERFORMANCE OF EXISTING DYNAMIC COMPARATORS	52
	3.3.1 Strong-Arm latched comparator	52
	3.3.2 Double Tail dynamic comparator	53
	3.3.3 Modified Double Tail latched comparator	55
3.4	DESIGN AND ANALYSIS OF PROPOSED DYNAMIC COMPARATOR	56
	3.4.1 Parametric analysis of proposed dynamic comparator	58
	3.4.2 Monte carlo and corner analysis of proposed dynamic comparator	64
3.5	ARCHITECTURE AND WORKING OF THE PROPOSED CHARGE SHARING DYNAMIC COMPARATOR	68
	3.5.1 Kickback noise analysis in proposed charge sharing dynamic comparator	72
	3.5.2 Statistical analysis of noise and input referred offset voltage in proposed charge sharing comparator	74
	3.5.3 Simulation and parametric analysis of proposed charge sharing comparator	76
	3.5.4 Variation of kickback noise as function of input differential voltage in the proposed charge sharing comparator	80
	3.5.5 Corner analysis of proposed charge sharing comparator	81
3.6	SUMMARY OF THE IMPORTANT RESULTS	82

CHAPTER 4: DESIGN AND ANALYSIS OF DAC WITH IMPROVED SWITCHING SCHEME FOR REDUCTION IN SWITCHING ENERGY PER CONVERSION CYCLE **85-104**

4.1	BRIEF INTRODUCTION ABOUT CHAPTER	85
4.2	OVERVIEW OF DIGITAL TO ANALOG CONVERTERS (DACS)	86
4.3	EXISTING DIFFERENT MAJOR SWITCHING SCHEMES OF DIGITAL TO ANALOG CONVERTER	88
4.3.1	Bottom plate sampling-based Charge Redistribution DAC (CDAC) switching	88
4.3.2	Common mode (V_{cm}) based switching scheme and monotonic switching scheme for DAC	90
4.3.3	Capacitor Splitted switching scheme for DAC	93
4.4	A COMPREHENSIVE VIEW OF PROPOSED SINGLE ENDED SWITCHING SCHEME	93
4.5	CHOICE AMONG DIFFERENT CAPACITORS FOR UTILIZATION IN DAC CAPACITOR ARRAY	100
4.6	ARCHITECTURAL DESIGN OF SAMPLE AND HOLD CIRCUIT	101
4.7	SUMMARY OF THE IMPORTANT RESULTS FOR THE PROPOSED DAC	103

CHAPTER 5: DESIGN OF IMPROVED CONTROL UNIT FOR SAR ADC **105-119**

5.1	BRIEF INTRODUCTION ABOUT CHAPTER	105
5.2	OVERVIEW OF SYNCHRONOUS AND ASYNCHRONOUS SAR LOGIC BASED CONTROL UNITS	106
5.3	ENHANCED D FLIP FLOP CIRCUIT AND TIMING CLOCK SIGNALS OF CONTROL UNIT	109
5.4	SAMPLING PHASE AND BITWISE CONTROL SIGNAL GENERATION IN PROPOSED CONTROL UNIT	113
5.5	SUMMARY OF THE IMPORTANT RESULTS	118

CHAPTER 6: DESIGN AND ANALYSIS OF ULTRA LOW POWER 8 BIT SAR ADC		120-139
6.1	BRIEF INTRODUCTION ABOUT CHAPTER	120
6.2	OVERVIEW OF SUCCESSIVE APPROXIMATION REGISTER (SAR) TYPE ADC DESIGN	121
6.3	ARCHITECTURE OF PROPOSED 8-BIT SAR ADC	123
6.4	DYNAMIC COMPARATOR AND DAC MODULE UTILIZED IN DESIGN OF PROPOSED SAR ADC	125
6.5	RESULT AND SIMULATION ANALYSIS OF PROPOSED 8 BIT SAR ADC	130
6.6	SUMMARY OF THE IMPORTANT RESULTS	138
CHAPTER 7: CONCLUSIONS AND FUTURE SCOPE		140-145
7.1	CONCLUSIONS	140
7.2	FUTURE SCOPE	144
REFERENCES		146
LIST OF PUBLICATIONS		157

List of Figures

S. No.	Figure Caption	Page No.
Fig. 1.1	Basic architecture of Counter type ADC	3
Fig. 1.2	Block diagram of SAR ADC architecture	4
Fig. 1.3	Block diagram of Flash type ADC architecture	4
Fig. 1.4	DNL representation in an ADC output	5
Fig. 1.5	INL representation in an ADC output	6
Fig. 1.6	Gain error representation in an ADC output	7
Fig. 1.7	Offset error representation in an ADC output	7
Fig. 2.1	Electronic system interfacing of practical analog world with digital system	17
Fig. 2.2	(a) SAR ADC block diagram (b) Clock timing pulses	23
Fig. 2.3	Architecture of strong-Arm latch dynamic comparator	27
Fig. 2.4	Architecture of Double Tail dynamic comparator	28
Fig. 2.5	Architecture of Modified Double Tail dynamic comparator	28
Fig. 2.6	Architecture of Bi-directional dynamic comparator	29
Fig. 2.7	Architecture of Floating Inverter Amplifier based comparator	30
Fig. 2.8	Switching energy comparison of different DAC switching schemes	34
Fig. 2.9	SNDR and power consumption observation in existing SAR ADCs	45
Fig. 2.10	Pie chart of operating frequency and power consumption in existing SAR ADCs	46
Fig. 3.1	Transient output of basic latched comparator	53
Fig. 3.2	Transient output plot of DTDC for (a) $INN > INP$ (b) $INP > INN$	54
Fig. 3.3	Transient plot of modified comparator for (a) $INN > INP$, (b) $INP > INN$ (c) $INN = INP$	55-56
Fig. 3.4	Architecture of proposed dynamic comparator	57
Fig. 3.5	Transient output of proposed comparator for $inn > inp$, $T_{clk} = 1.2 \mu s$, $inn = 210 mV$, $inp = 200 mV$	59
Fig. 3.6	Transient output of proposed comparator for sawtooth input with $inp > inn$	60
Fig. 3.7	Transient output of parametric sweep for proposed comparator with $inp > inn$	61

Fig. 3.8	Transient power plot of proposed comparator with average value 33.81 nW	62
Fig. 3.9	ΔV_{out} (outn – outp) analysis for delay simulation of proposed comparator	63
Fig. 3.10	Montecarlo analysis of proposed comparator at different corners (a) NN (b) FF (c) SS	64-66
Fig. 3.11	Transient power plot vs temperature at (a) NN (b) SS corner for the designed comparator	67
Fig. 3.12	Architecture of Proposed charge sharing comparator	69
Fig. 3.13	Kickback noise paths in Proposed charge sharing comparator	73
Fig. 3.14	Transient analysis simulation of Proposed charge sharing comparator	75
Fig. 3.15	(a) Gain (G) vs V_{cm} (b) gm/ID vs V_{cm} (c) σ_{os} vs V_{cm} (d) σ_n vs V_{cm} of proposed comparator	76
Fig. 3.16	Delay versus input differential voltage (V_{diff}) of the Proposed charge sharing comparator at different V_{cm} values	78
Fig. 3.17	Power consumption versus input differential voltage (V_{diff}) of the Proposed charge sharing comparator at different V_{cm} values	78
Fig. 3.18	(a) Delay versus input supply voltage (b) Power consumption versus input supply voltage at $V_{cm} = 0.5$ V, $clk = 1$ GHz	79
Fig. 3.19	Variation of kickback noise w.r.t V_{cm} voltage in Proposed charge sharing comparator	80
Fig. 3.20	Process corner variations on (a) power consumption and (b) delay for the proposed comparator	82
Fig. 3.21	Variation of delay versus input differential voltage of proposed comparator for multiple V_{cm} values	82
Fig. 4.1	Bottom plate sampling based CDAC architecture	89
Fig. 4.2	Bottom plate sampling based CDAC architecture	91
Fig. 4.3	Monotonic switching scheme of capacitive DAC	92
Fig. 4.4	Flow chart of proposed single ended switching scheme	94
Fig. 4.5	Implemented proposed switching scheme for 4-bit DAC	95
Fig. 4.6	Proposed single ended switching scheme (a) – (f) for generation of multiple states	96
Fig. 4.7	Extension of last implemented switching step of proposed switching scheme	97
Fig. 4.8	Energy comparison of multiple existing switching methods with proposed switching scheme	99
Fig. 4.9	Architecture of designed sample and hold circuit	102
Fig. 5.1	Synchronous SAR logic-based control unit	108

Fig. 5.2	Synchronous SAR logic utilizing D flip flop and OR Gate	109
Fig. 5.3	Designed D flip flop circuit for control unit	110
Fig. 5.4	Transient output of Enhanced type D flip flop	111
Fig. 5.5	DAC control signals representation in DAC capacitor array	111
Fig. 5.6	Clock and internal signals utilized for timing synchronization in SAR logic	112
Fig. 5.7	Timing of clock and internal signals utilized in SAR logic	112
Fig. 5.8	Sampling phase representation in designed control unit	113
Fig. 5.9	Control signals for second bit generation (Z1a- Z8a) in designed control unit	114
Fig. 5.10	Control signals for second bit generation (Z9a- Z16a) in designed control unit	114
Fig. 5.11	Control signals for third bit generation (Z1b- Z8b) in designed control unit	115
Fig. 5.12	Control signals for third bit generation (Z9b- Z16b) in designed control unit	115
Fig. 5.13	Multiplexing of bits (a) For States A to H and (b) For States I to P in SAR logic unit	116
Fig. 6.1	SAR ADC interfaced circuit block diagram	122
Fig. 6.2	Block diagram of complete interfaced SAR ADC circuit	124
Fig. 6.3	Transient output of first proposed dynamic comparator	126
Fig. 6.4	Transient power graph of proposed comparator	127
Fig. 6.5	Comparison of proposed switching scheme with existing schemes	128
Fig. 6.6	Final digitized output of 8-bit SAR ADC for 620 mV within 540 KS/s	131
Fig. 6.7	Final digitized output of 8-bit SAR ADC for 115 mV above 540 KS/s	132
Fig. 6.8	Final digitized output of 8-bit SAR ADC for 89 mV above 540 KS/s	133
Fig. 6.9	Scaled spectrum output of designed 8-bit SAR ADC	134
Fig. 6.10	INL measurement in designed 8-bit SAR ADC for frequency within 540 KS/s	134
Fig. 6.11	DNL measurement in designed SAR ADC for frequency within 540 KS/s	135
Fig. 6.12	INL and DNL measurement of designed SAR ADC at frequency 1MS/s	136
Fig. 6.13	Power consumption breakdown for each module of SAR ADC	137
Fig. 6.14	Power consumption vs frequency plot of designed SAR ADC	138

List of Tables

S. No.	Table Caption	Page No.
Table 2.1	Comparison of different architectures of ADCs	19
Table 2.2	Parametric comparison of different ADC architectures in literature	20
Table 2.3	Comparative study of existing dynamic comparators	24
Table 2.4	Performance analysis of pre-amplifier module in different dynamic comparators	30
Table 2.5	Comparison of kickback noise in different dynamic comparators	31
Table 2.6	Comparison of multiple DAC switching schemes in literature	33
Table 2.7	Parametric representation of low power switching techniques in DAC	35
Table 2.8	Different capacitor layouts for DAC design in literature	37
Table 2.9	Different existing control units designed to implement SAR logic	40
Table 2.10	Different designed SAR ADCs in literature with their parametric outputs	42
Table 2.11	Parametric analysis of existing 8 and 10-bit SAR ADCs	46
Table 3.1	Performance comparison of existing dynamic comparators with proposed comparator	68
Table 3.2	Transistor sizes for the Proposed charge sharing comparator	71
Table 3.3	Performance of the Proposed charge sharing comparator	77
Table 3.4	Comparison of Proposed charge sharing with the existing comparators using pre layout simulation	77
Table 3.5	Summmary of obtained parameters at multiple corners of proposed comparator	81
Table 4.1	Comparison of existing schemes with proposed single ended switching scheme	98
Table 4.2	Different output logic states of 4-bit DAC in proposed switching	99
Table 5.1	Comparative study of synchronous and asynchronous SAR logic units	107
Table 5.2	Comparison of proposed SAR control unit with existing SAR logic units	117
Table 6.1	Parametric summary of proposed 8-bit SAR ADC	136
Table 6.2	Comparative analysis of different 8-bit SAR ADCs	137

List of Abbreviations

Abbreviation	Full Form
DSP	Digital Signal Processor
ADC	Analog to Digital Converter
SAR	Successive Approximation Register
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
LSB	Least Significant Bit
SNDR	Signal to Noise and Distortion Ratio
NMOS	N channel MOSFET
PMOS	P channel MOSFET
DAC	Digital to Analog Converter
MSB	Most Significant Bit
ENOB	Effective Number of Bits
SFDR	Spurious Free Dynamic Range
CMOS	Complementary Metal–Oxide–Semiconductor
FPGA	Field Programmable Gate Array
GSPs	Giga Samples Per Second
DSM	Delta Sigma Modulation
TI	Time Interleaved
VCO	Voltage Controlled Oscillator
FOM	Figure of Merit
IOT	Internet of Things
PVT	Process Voltage Temperature
pW	Pico Watt
SNR	Signal to Noise Ratio
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal
TSPC	True Single -Phase Clock
EDA	Electronic Design Automation
fJ	Femto Joule
nW	Nano Watt
pF	Pico Farad
PDP	Power Delay Product
CDAC	Charge Redistribution Digital to Analog Converter
CAS	Comparator and Switch
PIP	Polysilicon Insulator Polysilicon

List of Symbols

Symbol	Meaning
V_{in}	Input Voltage
V_{cm}	Common Mode Voltage
C	Capacitance
V_r	Reference Voltage
N	Number of bits in ADC
KS/s	Kilo Samples Per Second
ns	Nano seconds
Clk	Clock Signal
8b	8 bits
NCLK	Inverted Clock
INN/inn	One of the Comparing Input
INP/inp	Second Comparing Input
outn	Output of Comparator from INN end
outp	Output of Comparator from INP end
V_{DD}	Supply Voltage
V_{cm}	Common Mode Voltage
$g_{M,eff}$	Effective Transconductance
F_s	Sampling Frequency
F_{in}	Input Signal Frequency
SS/ss	Slow Slow
SF/sf	Slow Fast
FF/ff	Fast Fast
FS/fs	Fast Slow
T_{clk}	Time period of clk signal
W/L	Width to length Ratio
σ_{os}	Noise due to total input referred offset
σ_n	Root mean square value of comparator noise
tt	Typical Typical
S/H	Sample and Hold
Ack	Acknowledge
Clkc	Comparator Clock
Xs	Sampling Pulse

Chapter 1

Introduction

1.1 BRIEF OVERVIEW OF ANALOG TO DIGITAL CONVERTERS

The modern era is widely regarded as the digital age, driven by rapid advancements in electronic industries that have transformed diverse fields through the widespread use of digital technologies. Among the technological innovations, the Digital Signal Processor (DSP) has emerged as a key component that utilizes the power of digital technology to execute advanced algorithmic frameworks and signal processing operations with exceptional computation-oriented accuracy and speed. Furthermore, improvements in noise immunity, combined with the implementation of error detection and correction mechanisms, have significantly enhanced the robustness of digital signal transmission and storage, making them less susceptible to interference [1]. Consequently, analog circuit techniques in many domains have been progressively replaced by digital and mixed-signal architectures that offer superior flexibility, scalability, and efficiency. However, since real world signals inherently exist in analog form so to felicitate the advantage of digital signal storage, the most important module to convert analog signal into the digital equivalent is Analog to Digital converter (ADC).

Moreover, continuous research in this area has led to the development of several ADC architectures such as Flash, Pipeline, Delta-Sigma, and Successive Approximation Register (SAR) ADCs. The choice of an appropriate ADC architecture largely depends on the resolution, operating speed and power efficiency of target application since these parameters often involve trade-offs during the design of ADCs and Digital to Analog Converters (DACs) [2]. One commonly used architecture is the Flash ADC, which is preferred for high-speed applications because it simultaneously compares the input signal against multiple reference levels. However, increasing the resolution leads to an exponential rise in the number of comparators, making the design significantly more complex. Delta-Sigma ADCs, on the other hand are suitable for applications that require very high resolution at low to moderate speeds while maintaining moderate power consumption. They can achieve resolutions of 20 bits or more by using oversampling and noise-shaping techniques [3–5]. The drawback, however, is that oversampling pushes the internal circuits of the Delta-Sigma modulator to operate at much higher speeds, which in turn increases power consumption. Among the various architectures,

the SAR ADC has gained the most advantage from technology scaling, as its largely digital structure allows significant reductions in power consumption. It provides low to medium resolution and is suitable for applications that operate at low to moderate speeds, especially where achieving ultra-low power consumption is a primary requirement for the ADC. In a SAR ADC, both analog and digital design approaches work together to deliver the desired performance. Achieving this balance requires well-optimized circuit architectures, low-power design methods, and accurate switching techniques to maintain high precision and energy efficiency in modern mixed-signal systems [6]. To achieve higher resolution and faster conversion rates within the SAR framework presents challenges related to capacitor matching, switching energy consumption, and digital control complexity. Consequently, recent research efforts in literature have concentrated on improving SAR control logic, developing more efficient capacitor switching schemes, and exploring hybrid analog–digital approaches to boost conversion efficiency and minimize energy loss [7].

Furthermore, over the past decade extensive research has been conducted to enhance the performance metrics of the SAR ADC in terms of energy efficiency, speed, and resolution. Conventional SAR architectures, while simple and power-efficient, often suffer from large switching energy and capacitor mismatch issues, which limit their scalability in advanced technology nodes [8]. To address these limitations, multiple energy-optimized capacitor switching schemes have been introduced that significantly lower the overall switching energy compared to the conventional binary-weighted approach [9, 10]. Further optimization through merged capacitor switching (MCS) and hybrid capacitor arrays has contributed to achieving up to 90% reduction in switching energy and improved linearity [11, 12].

In addition to switching strategies, advancements in digital control logic and comparator design have also played a vital role in improving SAR ADC performance. Low-power dynamic comparators with offset calibration and reduced kickback noise is presented in existing work to enhance decision accuracy at lower supply voltages [13]. Similarly, asynchronous SAR logic and clock-optimized architectures have proven to improve conversion speed without significantly increasing power consumption [14]. Recent research trends also emphasize hybrid and time-interleaved SAR ADCs, which combine multiple sub-ADCs or integrate oversampling techniques to achieve higher throughput suitable for high-speed data acquisition systems [15]. Overall, these developments highlight the continuous evolution of SAR ADC architectures toward achieving an optimal balance among speed, resolution, power, and area efficiency. Despite these advancements, further improvements in switching energy reduction,

capacitor matching, and low-power logic design remain critical for next-generation mixed-signal applications of SAR ADC. Keeping this in view, block diagram representation of major ADCs architecture is given in next section for better exploration of ADC designs.

This chapter is arranged in total seven sections. Brief overview of analog to digital converters is presented in section 1.1. The introduction about architectural diversity of different existing ADCs is included in section 1.2. Further, the key performance parameters of an ADC are focussed in section 1.3. Problem statement is incorporated in section 1.4. Subsequently, sections 1.5 and 1.6 include research objectives and their methodologies, respectively. Finally, section 1.7 comprises the thesis organization.

1.2 ARCHITECTURAL DIVERSITY FOR DIFFERENT ADC

Different architectures of ADCs like Counter type, Flash, Dual-Slope, Delta-Sigma, Pipelined, SAR ADC etc. are available but for medium accuracy and low power applications, SAR ADC holds a great importance among available designs as technology scaling has benefitted this architecture the most in terms of reduced power [16]. However, it is also presented in literature that for low to medium-speed applications, integrating and oversampling ADC architectures are also used as they provide good accuracy, but their long conversion delay makes them unsuitable for high-speed systems [17].

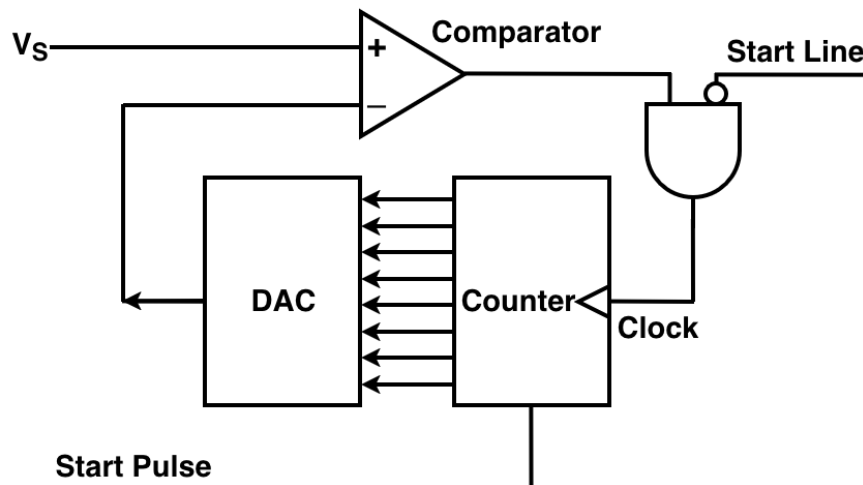


Fig. 1.1 Basic architecture of Counter type ADC

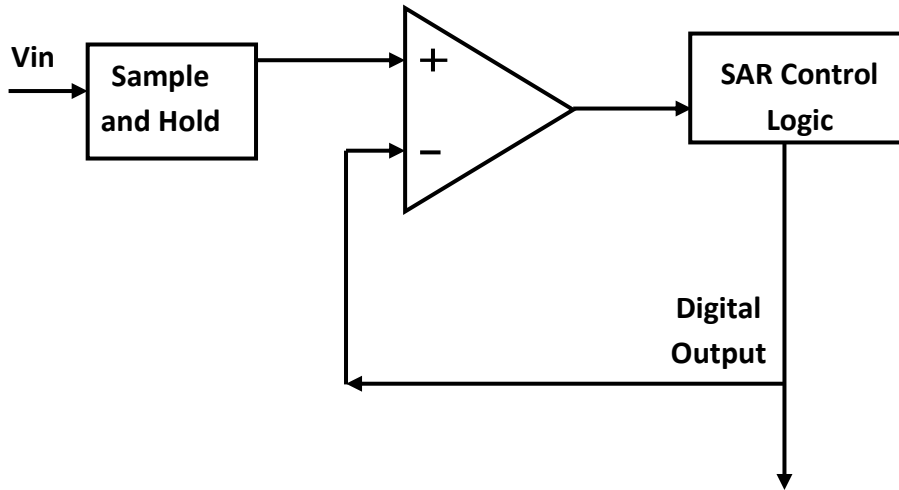


Fig. 1.2 Block diagram of SAR ADC architecture

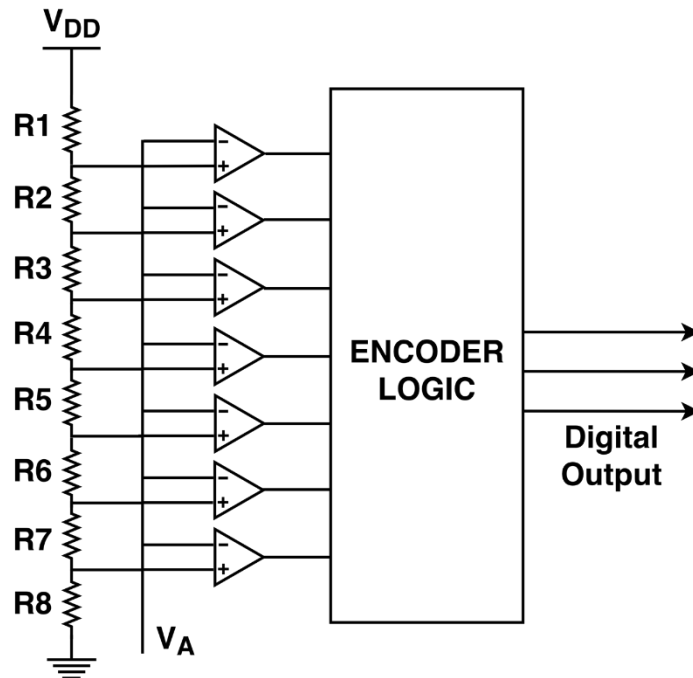


Fig. 1.3 Block diagram of Flash type ADC architecture

Also, when power consumption is not a major concern, but high-speed operation is required, the Flash ADC architecture is also widely adopted by researchers. The block diagrams of the major ADC architectures are illustrated in Fig. 1.1 for the Counter type ADC, Fig. 1.2 depicts basic block diagram of SAR ADC and in Fig. 1.3 Flash type ADC architecture is represented. A Flash ADC offers high conversion speed because it checks all voltage levels at the same time using many comparators, but this also makes it large, costly, and power-hungry [18]. A counter-type ADC works by slowly counting up until the output voltage matches the input voltage, which makes the design simple but the conversion very slow. A SAR ADC works in a smarter

way by using a step-by-step guessing method (like a binary search), which makes it faster than the counter type and much more power-efficient than the Flash type. Good balance between speed, power, and size makes the SAR ADC as most utilized architecture in many modern electronic devices.

1.3 PERFORMANCE PARAMETERS OF ADC

To analyze the performance characteristics of the designed ADC, it is essential to understand the parameters that define the behavior of analog-to-digital converters. The key performance parameters considered for the optimization of the proposed ADC are discussed in this section.

1.3.1. Differential Non-Linearity (DNL)

DNL is the measure of how much each step size of an ADC differs from the ideal value of one Least Significant Bit (LSB). DNL indicates the error in the width of each digital code compared to the ideal step size. The DNL representation as a specific case is shown in Fig. 1.4, wherein, the step width of a non-ideal ADC with DNL is extending to the maximum of 1.5 LSB which is representing a DNL of +0.5 LSB. Whereas in a minimum case, the width of the step with output value 001 is only 0.5 LSB which is 0.5 LSB less than the expected width. So, the DNL here would be - 0.5 LSB.

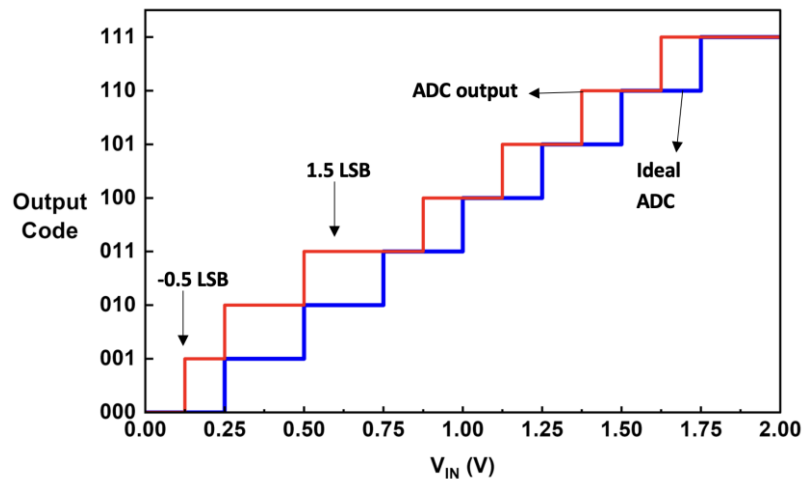


Fig. 1.4 DNL representation in an ADC output

In an ideal analog-to-digital converter (ADC), each quantization step is uniform, ensuring equal spacing between successive digital codes. However, in practical implementations, non-idealities such as capacitor mismatch, comparator offset, and noise introduce variations in step size, causing certain code transitions to deviate from their ideal values.

1.3.2. Integral Non-Linearity (INL)

Integral Non-Linearity (INL) is considered as the accumulated effect of Differential Non-Linearity (DNL) errors over multiple code transitions [19]. When several consecutive DNL values are negative, the actual transfer characteristic tends to shift upward from the ideal curve, resulting in a positive INL as shown in Fig. 1.5. Conversely, a negative INL occurs when the practical transfer curve deviates downward from the ideal characteristic.

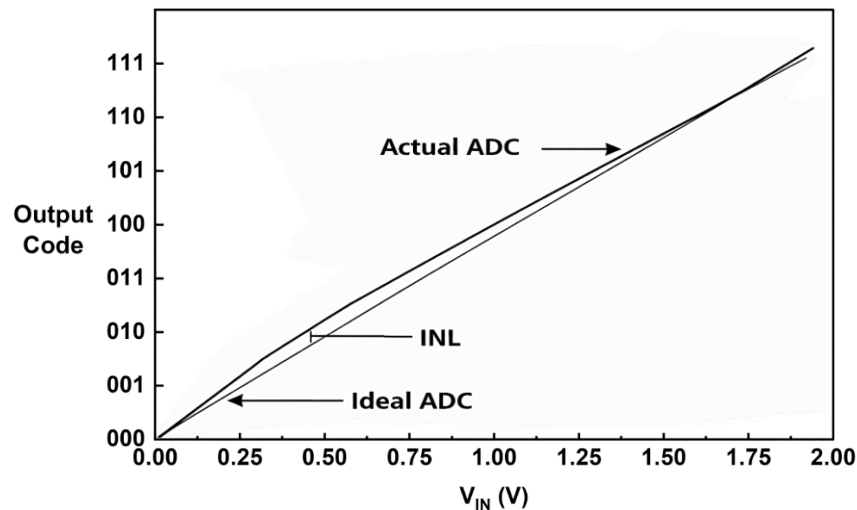


Fig. 1.5 INL representation in an ADC output

When the INL value is small, it means the ADC output closely follows the ideal straight line and the conversion is accurate. But when the INL value becomes large, it creates distortion in the digital output, especially for mid-range input signals.

1.3.3 Gain error

Gain error in an Analog-to-Digital Converter (ADC) refers to the difference in slope between the actual transfer function and the ideal characteristic after offset error correction. Once the offset compensation is applied, an input voltage of zero should ideally produce a digital output of zero [20]. However, due to gain error, the end point of the actual transfer characteristic does not align with the end point of the ideal transfer curve as shown in Fig. 1.6. Therefore, the gain error is defined as the difference between the midpoint of the final output step in the actual transfer characteristic and that of the ideal response. When the gain error is small, the spacing between the lowest and highest codes matches the ideal value. But if the gain error is large, the ADC either “compresses” or “expands” the input range.

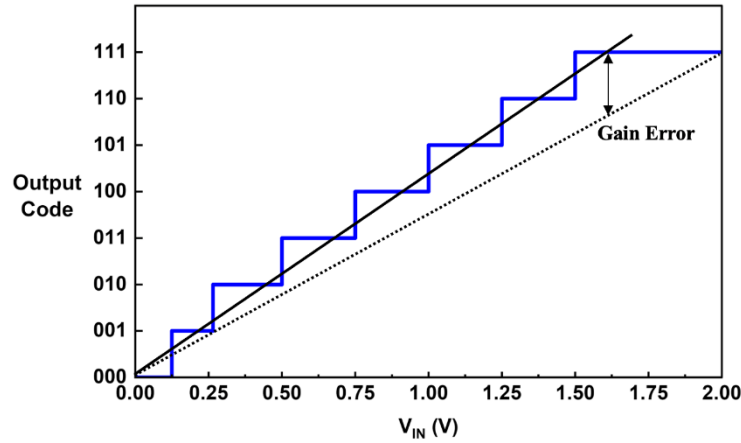


Fig. 1.6 Gain error representation in an ADC output

This means the output codes do not accurately represent the real input voltage, especially near the full-scale range.

1.3.4 Offset Error

Offset error is the deviation of the actual ADC's transfer function from the perfect ADC's transfer function at the point of zero to the transition measured in the least significant bit (LSB).

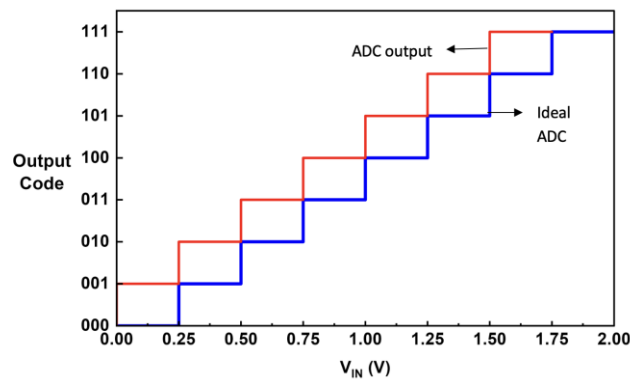


Fig. 1.7 Offset error representation in an ADC output

Offset error shifts the entire transfer curve of the ADC either upward or downward without changing its slope as represented in Fig. 1.7. This means that every digital output code is moved by the same amount, which affects the accuracy of low-level signals.

1.4 PROBLEM STATEMENT

The researchers have devoted significant contribution to improve the performance of ADC architectures for conversion of analog signal into the digital equivalent for many sensor applications. Different ADCs architectures like flash type, counter type, delta sigma and SAR ADC got utilized by the researchers depending upon the application requirement of resolution, speed and power. For applications characterized by moderate speed and mid-range resolution, SAR ADCs are widely preferred by researchers. This is mainly because their architecture is largely digital in nature, which supports low power operation with enhanced scalability in advanced technology nodes.

The optimization of SAR ADC architecture in regard to reduced power, area and non-linearities like INL and DNL is always an area of consideration for the researchers. A SAR ADC mainly comprises three key blocks: a comparator, a capacitor-based digital-to-analog converter (DAC), and a SAR logic control unit. The control unit drives the DAC module in accordance with the selected switching scheme to complete the conversion process. The design of ultralow power SAR ADC becomes the requirement of modern era for reducing on chip power dissipation of designed ADC in the applications like pacemakers where power is supplied through non rechargeable batteries.

Furthermore, the comparator module is designed to minimize both static and dynamic power consumption, thereby enabling its suitability for ultra-low-power applications. In this view, dynamic comparators are utilized in ADCs against static comparators. A dynamic comparator comprises a pre-amplifier stage that amplifies the input analog signal, followed by latch-based regeneration which is initiated by turning ON of PMOS cross-coupled pair of latch facilitating positive feedback. Many researchers worked on the different architectural variations of dynamic comparators to reduce power consumption, kickback noise and offset voltage at different technology nodes and clock frequency. To design an ultra-low power dynamic comparator with good resolution, low power, better noise immunity and reduced delay is an area of consideration. In this view, isolation of pre-amplifier and latch regeneration stage with proper analysis of pre-amplifier gain (G) on the performance of dynamic comparator is a design consideration. To reduce delay of the comparator, biasing of pre-amplifier transistors in the region supporting higher gain is also a consideration in the design. Further, Kickback noise effect in a dynamic comparator can be reduced by limiting the slew rate of clock signal. Moreover, second important module of SAR ADC is Digital to Analog converter (DAC).

Designing of DAC unit with reduced switching energy has become the core area of working for the researchers in the design of ultra-low power SAR ADC. DAC module is the most power hunger module of SAR ADC and it is designed using capacitive array incorporating low power switching scheme to establish intermediate voltage levels used for the comparison in the digitization process of an analog sample. Conventional DAC switching techniques often suffer from large switching energy, complex control logic, and unequal reference voltage utilization, which degrade the converter's overall energy efficiency. To address these challenges, recent research has focused on innovative switching algorithms and capacitor array optimizations that minimize the average switching energy and enhanced conversion speed without compromising accuracy. Efficient DAC design in SAR ADCs requires careful minimization of both switching energy and total capacitance. By employing energy-aware switching strategies, the initial comparison steps can be executed without engaging the capacitive network, effectively eliminating switching losses for the most significant bits. Furthermore, differential DAC implementations augmented with dummy capacitors provide improved matching and symmetry, leading to lower noise interference and enhanced energy performance.

Moreover, design of SAR logic unit often termed as control unit is one of the important considerations in the design of SAR ADC. The conversion speed, proper timing synchronization and error robustness are the key requirements from a SAR logic-based control unit. The literature highlights the necessity of SAR based logic unit and DAC co-optimization, especially when advanced switching techniques such as monotonic, common-mode (V_{cm}) based, and capacitor-splitting schemes are employed for switching. Based on these observations, there is a need to design a SAR logic-based control unit with improved synchronization between the DAC and the control logic in order to reduce nonlinearity errors such as INL and DNL. In addition, proper interfacing of all the designed modules, along with accurate control of the common-mode voltage (V_{cm}), is essential to achieve an overall ultra-low-power SAR ADC.

The minimization of differential non linearity (DNL) and integral non linearity (INL) in designed SAR ADC along with reduced power consumption holds the major design projection. In view of this, the primary objective of this work is to develop an ultra-low-power 8-bit SAR ADC with better performance in terms of reduced power consumption along with minimized integral and differential non linearities. This project considers designing all the main modules of the SAR ADC, namely the comparator, the DAC, and the SAR logic-based control unit, with

improved architectural performance using Cadence in the 45 nm technology node. To achieve the improved SAR ADC design, specific objectives have been defined in the following section.

1.5 OBJECTIVES

The proposed ultra-low power single ended 8-bit SAR ADC is required to be designed with emphasis on reducing power consumption along with improvement in ADC performance through optimized circuit design. Further, each building block of SAR ADC is carefully reviewed and based on the identified research gaps, design and analysis objectives are formed. In this view, the novel architecture is proposed with improved dynamic comparator, DAC unit utilizing proposed switching scheme with reduced switching energy per conversion step and control unit with better synchronization timing logic. Furthermore, to carry out the whole research work, following four objectives are formulated:

- Objective 1:** Comprehensive analysis of existing comparators to design a novel dynamic comparator with reduced leakage power and enhanced noise immunity.
- Objective 2:** Design and analysis of DAC with improved switching scheme based on capacitive splitting for reduction in switching energy per conversion cycle.
- Objective 3:** Characteristic analysis of Low power D flip flop and multiplexer modules to design an improved control unit for SAR ADC.
- Objective 4:** Interconnection of all designed modules and performance optimization of proposed ultra-low power SAR ADC unit and its validation for application in biomedical domain.

To attain these objectives, the systematic methodologies are followed, encompassing design & simulation of each module along with complete interfaced proposed SAR ADC. The methodologies are aligned with the overall goal of this work so that the objectives can be effectively addressed and assessed.

1.6 OBJECTIVE-WISE METHODOLOGY

The following methodologies are followed to attain the formulated objectives:

1.6.1 Methodology for Objective 1:

Objective 1 is focussed on the designing and simulation of proposed dynamic comparator with reduced power consumption compared with existing designs. Also, parametric analysis of

delay, power delay product, resolution and kickback noise for the designed comparator is carried out. The methodology followed to achieve this objective is given as:

- Design of major existing dynamic comparators in CADENCE virtuoso and simulation analysis of parameters like power, delay, and offset voltage of existing comparators.
- Design of improved dynamic comparator incorporating power reduction logic at good resolution.
- Simulation of designed dynamic comparator in CADENCE Virtuoso 45 nm.
- Parametric analysis of designed comparator in terms of power dissipation, delay and operating frequency.
- Comparative study with existing dynamic comparators for validation of the designed comparator.

1.6.2 Methodology for Objective 2:

Digital to analog converter is the most power-hungry module of SAR ADC. The switching of capacitors in the capacitive array of DAC consumes energy in the conversion process. Also, DAC performs sampling of input signal in which bottom plate sampling and top plate sampling are two major approaches. To design a DAC unit incorporating proposed switching scheme with zero switching energy in first two MSB comparisons along with reduced total capacitance, the following methodology is followed:

- Literature review and analysis of existing switching schemes to insight the switching energy per conversion step in existing DACs.
- Designing of improved DAC with reduced switching energy per conversion cycle with zero switching energy in atleast two MSB comparisons.
- Simulation and analysis of designed DAC circuit in CADENCE Virtuoso 45 nm technology node.
- Comparison of improved switching scheme with existing switching schemes like capacitive splitting, charge redistribution, level switching in terms of switching energy and number of capacitors used.

1.6.3 Methodology for Objective 3:

In this objective, design of control unit incorporating improved synchronization timing logic multiplexers, D Flip is considered. The methodology followed to attain this objective is as follows:

- Design of low power D flip flops and multiplexer modules in CADENCE Virtuoso 45 nm technology node.
- Utilization of the designed D flip flop and multiplexer modules in the designing of SAR logic-based control unit.
- Proper timing synchronization between multiple stages of control unit to get proper timing order with comparator output.

1.6.4 Methodology for Objective 4:

After, designing all major modules of SAR ADC, the interfacing to achieve final design of 8-bit SAR ADC is equally important. In this objective, design of complete 8-bit SAR ADC is focussed. The parametric analysis of complete design in terms of INL, DNL, power consumption, signal to noise and distortion ratio (SNDR) and ENOB is carried out. Also, parametric analysis and comparative study with state of art SAR ADCs is presented. The methodology followed to attain the final objective is as follows:

- Interconnection of all the designed modules of SAR ADC i.e dynamic comparator, DAC and control unit with proper timing synchronizations for sampling rate of 540 KS/s.
- Simulation and analysis of designed SAR ADC in terms of Power, INL, DNL, SNDR at 540 KS/s.
- Comparative analysis of optimized designed SAR ADC with existing circuits on measured parameters.

1.7 THESIS ORGANIZATION

This thesis is structured in total seven chapters. Chapter 1 discusses the introduction where the importance of analog to digital converters is discussed. Afterwards, Chapter 2 provides the literature survey of the research work. Moreover, from Chapter 3 to Chapter 6 all the objectives are discussed in detail. Eventually, Chapter 7 is dedicated to the conclusion and future scope. A brief overview of contents of each chapter is outlined as follows –

Chapter 1: Introduction

In this chapter, a brief discussion about analog to digital converters is carried out. Also, performance parameters of ADCs are incorporated. Following this, a problem statement highlighting complete view of the proposed SAR ADC project is presented. The chapter also includes the objectives and their methodologies for the research work. The chapter concludes with an organization of complete thesis work as well.

Chapter 2: Literature Review

In this chapter, literature review of each module as of comparator, DAC, control unit along with complete SAR ADC is included. The chapter begins with discussion of different existing architectures of ADCs followed by the brief view of different modules of SAR ADC. Further, different existing dynamic comparators are reviewed, and major architectures of existing dynamic comparators are presented for better exploration of dynamic comparators. Furthermore, DAC module is reviewed along with the low power switching schemes like conventional switching, monotonic scheme, V_{cm} based, merged capacitor etc. A comparative study of these switching schemes is presented. Also, chapter includes the capacitor design consideration for DAC unit along with capacitor mismatch reduction techniques. Following this, review for control logic of SAR ADC is focussed and review of existing SAR ADC designs and techniques is also incorporated. Finally, this chapter is concluded with inclusion of the identified research gaps based on the literature review.

Chapter 3: Design and Analysis of Low Power Dynamic Comparator for SAR ADC

In this chapter, design and parametric simulation analysis of different low power dynamic comparators in CADENCE Virtuoso 45 nm technology node is carried out. Strong arm latch dynamic comparator is considered as the baseline comparator that does not avoid the direct path connection between V_{DD} and ground due to which it lead to transient power consumption. Further, double tail dynamic comparator and modified double tail dynamic comparator are also considered for simulation & analysis and the transient analysis of both comparators is included. Following this the chapter includes first proposed dynamic comparator architecture design along with the simulation parametric analysis. Rigorous analysis in terms of power, delay, monte carlo simulation at different corners like ss, sf, ff etc. and temperature analysis from -40 degree centigrade to 110 degrees centigrade is carried out to validate the utilization of designed comparator in analog to digital converter. Proposed comparator outperforms the state of art

dynamic comparators in terms of power, delay and PDP which is included as comparative analysis of proposed with other existing dynamic comparators. Finally, second proposed dynamic comparator for high frequency applications based on charge shared logic is carried out and its detailed analysis is also included.

Chapter 4: Design and Analysis of DAC with Improved Switching Scheme for Reduction in Switching Energy per Conversion Cycle

In this chapter, the design and analysis of a Digital-to-Analog Converter (DAC) with an improved switching scheme aimed at reducing the switching energy per conversion cycle is presented. The chapter begins with a brief introduction to the DAC and provides an overview of the major switching schemes commonly used in DAC design. Existing approaches, including the bottom-plate sampling-based charge redistribution (CDAC) switching scheme, common-mode (V_{cm}) based switching scheme, monotonic switching scheme, and capacitor-split switching scheme, are analyzed in terms of their average switching energy and the total capacitance required. The chapter further presents a detailed discussion of the proposed single-ended switching scheme used in the design of the 8-bit SAR ADC. Additionally, a section is included to support the selection of suitable capacitor types, along with a brief overview of the sample-and-hold circuit design. Finally, the key results and important outcomes of this chapter are summarized.

Chapter 5: Design of Improved Control Unit for SAR ADC

In this chapter, the design of the control unit for the SAR ADC is presented. The chapter begins with a brief introduction to SAR logic-based control unit architectures. It then discusses the enhanced D flip-flop circuit used in the design of the control unit, along with the associated timing clock signals. Furthermore, a detailed description of the different operating phases of the implemented SAR logic-based control unit is provided, including the sampling phase and the generation of bit-wise control signals. Finally, the key results and major conclusions of this chapter are summarized at the end.

Chapter 6: Design and Analysis of Ultra Low Power 8 Bit SAR ADC

In this chapter, all the designed modules namely the comparator, DAC, and control unit are integrated to realize an 8-bit SAR ADC operating with a single reference voltage of $V_{ref}/2$. The chapter begins with a brief overview of the SAR ADC design and then presents the architecture of the proposed 8-bit SAR ADC which is developed by interfacing the proposed

dynamic comparator, the single-ended switching-scheme DAC, and the designed control unit. The proposed DAC employs a dummy capacitive array along with a bootstrap switch at the positive input of the comparator, which enables zero switching energy during the first two MSB conversion steps. Furthermore, the 8-bit SAR ADC is simulated to perform parametric analysis in terms of power consumption, INL, DNL, SNDR, and ENOB. Finally, a comparative study with existing state-of-the-art 8-bit SAR ADCs is presented and the summarized results are included at the end of the chapter.

Chapter 7: Conclusion & Future Scope

In this chapter, the key findings of each chapter are summarized point-by-point to explain how each objective is achieved and their key features are reiterated. In the future scope section, the different aspects that can be worked upon are highlighted.

The chapter is followed by the list of publications and references. All the papers published for the completion of this work are listed. While all the books and papers that were referred during the study to form the basis for this work are listed in the reference section.

Chapter 2

Literature Review

2.1 BRIEF INTRODUCTION ABOUT CHAPTER

In this chapter, the recent advancements and ongoing developments in Analog-to-Digital Converters (ADCs) is focussed. ADC is an important module in the analog front end system that exists between sensors and digital signal processing block. This chapter starts with a comparative study of different existing architectures of ADCs like Flash, Pipelined, Delta Sigma and Successive Approximation Register (SAR) ADC. Parameters like resolution, area, power requirement, sampling frequency and design cost are considered for the comparison of different existing ADC architectures. Further, for moderate resolution and operating speed applications, design of 8-bit SAR ADC for low power applications is considered as main focus of research in this work. Therefore, an exhaustive literature survey of each and every module for SAR ADC including comparator, Digital to Analog Converter (DAC), SAR logic-based control unit and final designed SAR ADC is carried out.

In the comparator section, a review of different dynamic comparator designs reported in the literature is presented, considering key performance parameters such as fabrication technology, input-referred offset voltage, chip area, power consumption, and supply voltage. Furthermore, a detailed literature review of the DAC module is provided, highlighting various low power switching schemes used in recent designs along with a brief discussion of capacitor layout techniques employed in capacitive DAC arrays. Further, the review gets focussed on different SAR logic-based control unit designs and finally, an exhaustive literature survey of existing architectures is carried out to design a low-power SAR ADC. Researchers usually choose an ADC architecture depending on the resolution and bandwidth needed for their application. From the literature, it is well intimated that SAR ADC is commonly used architecture in the application areas requiring medium resolution and moderate conversion speed.

This chapter is structured into eleven different subsections. It begins with a brief chapter introduction in section 2.1, followed by section 2.2 focussing overview of ADCs and the different existing architectures of ADCs. In the next section 2.3 different modules of SAR ADC are described, while section 2.4 focuses on different existing dynamic comparators. The section 2.5 details the major architectures of existing dynamic comparators and section 2.6 covers the

low power switching techniques for DAC design. The capacitor design consideration for DAC unit is discussed in section 2.7. The section 2.8 delves into capacitor mismatch reduction techniques, while sections 2.9 focus on the review for control logic of SAR ADC and 2.10 focus on the review of existing SAR ADC designs and techniques. Finally, the section 2.11 addresses the identified research gaps based on the literature review.

2.2 OVERVIEW OF ANALOG-TO-DIGITAL CONVERTERS AND THEIR ARCHITECTURES

Analog to Digital Converter is the most fundamental block in the process of sensor interfacing with the practical analog world signal for digital signal processing. Advancement in digital technologies has simplified the signal processing in the digital domain to create the essential need of conversion of practical analog signal into its digital equivalent [21]. Further, improved noise margins along with error detection and correction techniques in digital domain have enhanced the reliability of digital signal transmission and storage compared to analog processing of signals [22]. Additionally, complex algorithms and functions have been realized utilizing the most fundamental approach in digital signal processors which has revolutionized the electronic industry to work on the design and implementation of analog to digital converters for conversion of practical existing analog signal into its digital equivalent.

As a result, many applications have moved away from traditional analog circuits and shifted toward digital solutions because they provide better efficiency, higher speed, more flexibility, and improved reliability.

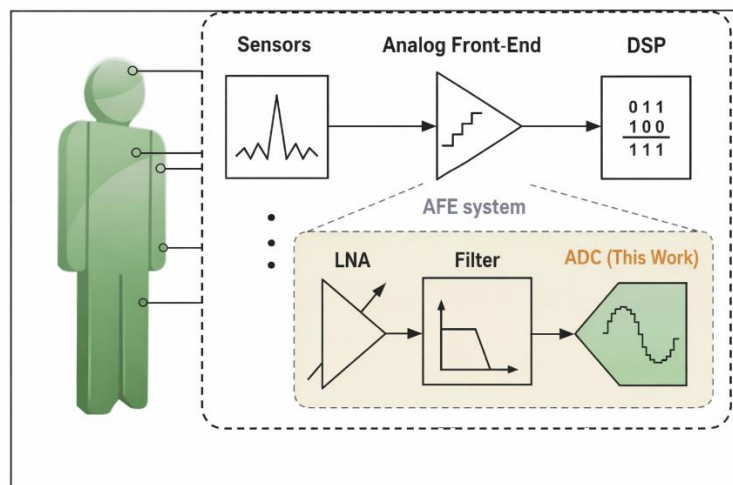


Fig. 2.1 Electronic system interfacing of practical analog world with digital system

Following Moore's Law, continuous improvements in CMOS fabrication technology have increased integration density with enhanced performance and power efficiency. Further, technology scaling has not benefited analog circuits much but its counterpart; design of digital circuits has become more simple utilizing characteristics of FPGA, automatic placement & routing, gate level netlist generation from behavioural simulation along with modelling a task utilizing hardware description language. All these qualities of signal processing have limited the analog signal processing domain for filtering, referencing of supplies and amplification of signals only and major signal processing has been shifted into digital processing. Thus, to avail benefits of digital signal processing, analog world requires analog to digital converters (ADCs) and digital to analog converters (DACs). The practical block diagram of electronic system interfacing practical analog world with digital system is given as in Fig. 2.1 that shows that ADC is an important module in the analog front end system exists between sensors and digital signal processing block.

Over the last many decades, many ADC architectures like Flash, Pipeline, Delta Sigma & SAR ADCs etc. have been emerged due to continuous research of scientists in this field. The choice of ADC architecture to be utilized is broadly dependent as per the resolution, speed and power efficiency requirement of application as there exists trade-off between the mentioned parameters in the design of ADCs/DACs [23-24]. Table 2.1 provides a brief comparison of different ADC architectures like Flash, Pipelined, Delta Sigma Modulator and SAR ADC. Flash ADCs are commonly used for high-speed applications because they perform simultaneous comparison of the input signal with multiple reference levels. However, their design complexity increases exponentially with resolution, as the number of required comparators doubles with each added bit. This results in significantly higher power consumption for higher-bit designs [25].

In addition, the increased number of comparators in Flash ADC leads to larger input capacitance and greater kickback noise, which can adversely affect the accuracy of the reference voltages. Therefore, flash ADC is used for low to medium resolution & high-speed applications upto 1 GSPs with resolution limited to 6 bits. However, techniques like interleaving and folding can offer slight improvements in resolution. Further, Pipelined ADC offers medium resolution at the cost of increased time of conversion. This ADC quantize the analog signal using its individual stage with next stage utilized to sample the residue. Summing amplifiers in the design lead to increase in power consumption of the pipelined ADC even if the number of comparators required in the design gets reduced [26]. Further, Delta Sigma ADC

is used for very high resolution at low to medium speed applications with medium power consumption. These ADCs achieve high resolution (≥ 20 bits) through oversampling and noise shaping techniques.

Table 2.1: Comparison of different architectures of ADCs [27]

Parameter	Flash ADC	Pipeline ADC	DSM ADC	SAR ADC
Working Principle	Require $2^n - 1$ number of comparators for comparison of input signal with reference value	A minimal parallel system where each stage handles a small number of bits.	Noise shaping along with oversampling	Binary search algorithm
Sampling rates	≤ 1 Giga samples per sec	≤ 500 Mega samples per sec	≤ 10 Mega samples per sec	≤ 3 Mega samples per sec
Resolution (bits)	6–8	10–14	16–24	8–18
Power Consumption	High	High	Moderate	Low
Area	Large	Medium	Medium	Low
Cost	High	High	Moderate	Low

However, oversampling increases the operating speed of internal DSM ADC components, leading to higher power consumption. Architecture of interest in this research is SAR ADC, this architecture has benefitted most with technology scaling in terms of reduced power consumption because of its maximum digital architecture. Also, it offers low to medium resolution with low to medium speed applications where ultra-low power consumption is prime requirement from chosen ADC architecture. However, the circuit is prone to be affected by noise which results in usage of this architecture in the low to medium resolution (8 bits to 18 bits) and slow to medium speed applications at low power consumption. It is most suitable for conversion of biopotential signals of low frequency range into digital equivalent value for multiple applications like wearable smart watches, pacemakers etc.

In Table 2.2 [28-31], a summary of various ADC architectures is presented, comparing key design parameters such as chip area, input signal frequency (F_{in}), SFDR, SNDR, power consumption, and sampling frequency (F_s). The results indicate that power consumption generally increases with higher sampling frequencies. Flash ADCs are typically used for very high sampling rates of around 1 GHz. However, advancements in semiconductor technologies have enabled other architectures to achieve high resolution with reduced power consumption

that makes them suitable for high-frequency applications as well. As observed from Table 2.2 the highest reported sampling frequency of 56 GHz in serial number 38 is achieved using a time-interleaved SAR ADC (TI-SAR ADC) implemented in 4 nm technology with power consumption of 0.24 Watt.

Table 2.2: Parametric comparison of different ADC architectures in literature [9-11, 28-31]

S.No.	Year	Architecture	Technology (nm)	Area [mm ²]	fin_hf [GHz]	SFDR [dB]	SNDR [dB]	P[W]	fs [GHz]
1	2013	Pipe, TI	0.028	0.4	2.70	65	50	0.5	5.4
2	2013	Pipe	0.065	0.26	0.10	63	57.6	0.0115	0.2
3	2013	SAR, TI	0.032	0.025	3.81	48.8	37	0.035	8.8
4	2014	Pipe	0.18	3.06	0.02	86	72	0.006	0.03
5	2014	Subranging	0.065	0.087	0.41	46.2	37.4	0.0043	0.82
6	2014	Pipe, SAR	0.065	0.48	0.10	74.8	60.1	0.0053	0.21
7	2014	SAR	0.028	0.1	0.05	76	67.1	0.008	0.1
8	2014	Pipe, SAR	0.04	0.042	0.08	85	65.3	0.005	0.16
9	2015	SAR	0.014	0.019	0.04	82	68.1	0.0043	0.07
10	2015	SAR, VCO	0.045	0.06	0.10	70	68	0.0034	0.2
11	2015	Two-Step, binary search, TI	0.065	0.24	12.50	40	29.7	0.088	25
12	2015	SAR, TI	0.028	0.14	23.00	32	25.2	0.381	46
13	2016	SAR, TI	0.016	NA	14.00	39.1	31.5	0.28	28
14	2016	SAR, TI	0.065	0.9	1.00	72.1	65	0.0377	1.6
15	2016	Pipe, SAR, TI	0.028	0.0928	0.40	76	60.8	0.0146	0.8
16	2016	SAR, TI	0.028	0.03	12.00	41	29	0.023	24
17	2016	SAR, TI	0.016	0.023	0.70	61	50.3	0.0082	1.6
18	2016	Pipe, TI	0.028	NA	2.00	70	58	2.3	5
19	2017	SDCT	0.04	0.45	0.10	83.3	64	0.233	5
20	2017	Pipe, SAR, TI	0.016	0.11375	0.15	73.6	64	0.0036	0.303
21	2017	Pipe	0.028	0.015	0.25	69.2	56.6	0.006	0.5
22	2017	Pipe	0.028	0.62	0.29	69.2	56.3	0.0142	0.6
23	2017	SAR	0.014	0.006	0.15	78.72	60.5	0.0033	0.3
24	2017	SAR, TI	0.016	0.014	1.00	56	50.1	0.0104	2
25	2017	Flash	0.065	0.08	1.00	49	40.7	0.021	2
26	2018	SAR	0.04	0.073	0.00	100.4	66.6	0.000031	0.001
27	2018	Subranging, Time-Based	0.065	0.007	0.48	62.1	45	0.0023	0.95
28	2018	SAR, TI	0.016	1.1	2.50	61.9	57	0.641	5
29	2019	SAR, TI	0.028	0.103	2.50	59.6	48.5	0.029	5
30	2019	SAR, TI	0.007	0.09	13.50	39.1	29.4	0.15	28
31	2020	Pipe	0.016	0.095	0.50	75.9	59.5	0.0109	1
32	2020	SAR	0.04	0.027	0.05	76.3	56.3	0.0014	0.1

33	2021	Time-Based, TI	0.065	0.22	10.00	52.5	38.8	0.129	20
34	2021	SAR, TI	0.016	0.023	4.00	46	42.4	0.026	8
35	2021	SAR, Pipe	0.028	0.134	0.50	67.09	59.3	0.0192	1
36	2022	SAR	0.008	0.0036	0.10	78.1	62	0.0006	0.25
37	2022	Subranging	0.028	0.024	1.15	60.6	44.8	0.0035	2.5
38	2022	SAR, TI	0.004	0.078	26.90	42	32.8	0.24	56
39	2022	SAR, TI	0.022	0.0045	1.90	50.9	38	0.006	3.8
40	2023	SAR [9]	0.065	NA	10^{-6}	62.47	53.13	1.2×10^{-9}	2×10^{-6}
41	2024	SAR [10]	0.065	NA	0.02	NA	72.2	402 μ	0.04
42	2025	SAR [11]	0.180	0.07	0.002	NA	69	110 μ	0.004

Furthermore, time-interleaved SAR ADCs have emerged as a preferred solution for high-frequency applications above 1 GHz, offering power consumption in the range of 19.2 mW to 240 mW for sampling rates between 1 GHz and 56 GHz, as summarized in Table 2.2. Additionally, in 2018, a highly energy-efficient 12-bit SAR ADC architecture operating at 1 MS/s was introduced in 40 nm technology, achieving a low power consumption of just 31 μ W. This design incorporated an on-chip input-independent calibration technique, resulting in a SFDR of 100.4 dB. The proposed calibration technique addresses the limitations of conventional split-ADC calibration while achieving rapid convergence. It requires only a single ADC and operates independently of the input signal. To achieve the required performance, three techniques were implemented, including the shuffling of mismatched MSB capacitors. The silicon prototype measurements validate the effectiveness of the proposed design, achieving 16-bit linearity with a total sampling capacitance of only 256 fF.

Further, a 2-GS/s, 8-bit flash ADC based on the remainder number system, implemented in 65-nm CMOS, has been reported in the literature [32]. This design achieves a sampling frequency of 2 GHz and exhibits power consumption of 0.0210 W. In addition, several subranging time-based ADCs implemented in 28-nm and 65-nm technologies have been presented by researchers [28–31], offering sampling frequencies ranging from 0.82 GHz to 2.5 GHz while consuming 0.0043 W to 0.0035 W. These designs are particularly suitable for mobile communication applications due to their high sampling speed and low-power operation. It is also worth mentioning that Signal-to-Noise-and-Distortion Ratio (SNDR) is a key performance parameter in ADC design. As observed in the literature, SNDR tends to degrade at higher sampling frequencies because parasitic effects become more prominent, limiting the overall dynamic performance. For instance, a SNDR of 25.2 dB is reported at a sampling frequency of

46 GHz in a SAR–TI based ADC implemented in 28-nm technology [33]. In contrast, the work presented in [34] demonstrates a significant improvement, achieving an SNDR of 61.9 dB in a 13-bit, 5-GS/s time-interleaved SAR-TI ADC fabricated using a 16-nm technology node. This enhancement is attributed to the use of a chopping technique, which effectively suppresses interleaved flicker noise and improves the ADC’s immunity to input signal variations. It is summarized that major utilized ADC architecture over the last 15 years is SAR and its hybrid including SAR-pipeline and SAR-TI. Figure of Merit (FoM) majorly characterize the energy efficiency of analog to digital converters which is also named as Walden figure of merit [23] given as an equation (2.1):

$$FoM = \frac{Power}{2^{Bandwidth} 2^{ENOB}} \quad (2.1)$$

FoM signifies the energy needed for each conversion step given in Joule/conversion step. Further, designs summarised in Table 2.2 infers that energy/conversion step has reduced drastically over the last two decades with value of 3 pJ/conversion step as the best FOM value noted in year 2000 to 0.4 pJ/conversion step as noted in 2019. This indicates a remarkable improvement in energy efficiency, achieving nearly seventy-five hundred times enhancement over the evaluated period. It is also evident that SAR ADCs rank among the most energy-efficient architectures, making them a preferred choice for applications such as biomedical devices and Internet of Things (IoT) systems, where minimizing power consumption is a key requirement. Furthermore, the energy consumption is given by CV^2 in which due to technology scaling, there is 100 times reduction in energy (As V has been reduced to $V/3$ and C has been reduced to $C/10$), remaining energy reduction is obtained from improvement of architecture in the designed circuit of analog to digital converters. Considering the need for an energy-efficient design suitable for biomedical signal processing applications operating around 540 KS/s, this research presents a comprehensive review, design, and analysis of a SAR ADC architecture. Additionally, a detailed literature review is presented for each primary module of the SAR ADC namely, the comparator, DAC, and SAR logic along with a concise overview of their functional roles.

2.3 DIFFERENT MODULES OF SAR ADC

SAR ADC comprises major subblocks as: comparator, a capacitor based digital to analog converter and a SAR logic-based control unit for conversion of analog sampled value to its digital equivalent as shown in Fig. 2.2 (a) as the basic block diagram of SAR ADC. Power

consumption of every module is required to be reduced so as to reduce the power dissipation in complete designed ADC. SAR ADC works on the principle of successive approximation for the conversion of analog signal into its digital equivalent [35] and its core principle resides on binary search algorithm in which a DAC generates the voltage V_{DAC} to be compared with input voltage, control unit configures the DAC based on comparator decision output and comparator makes the decision. In addition to three core blocks: comparator, DAC & control logic, input buffer and reference buffer are also used to make sure about proper driving capacity of input voltage V_{in} and to provide noise free reference voltage V_{ref} for digital to analog converter.

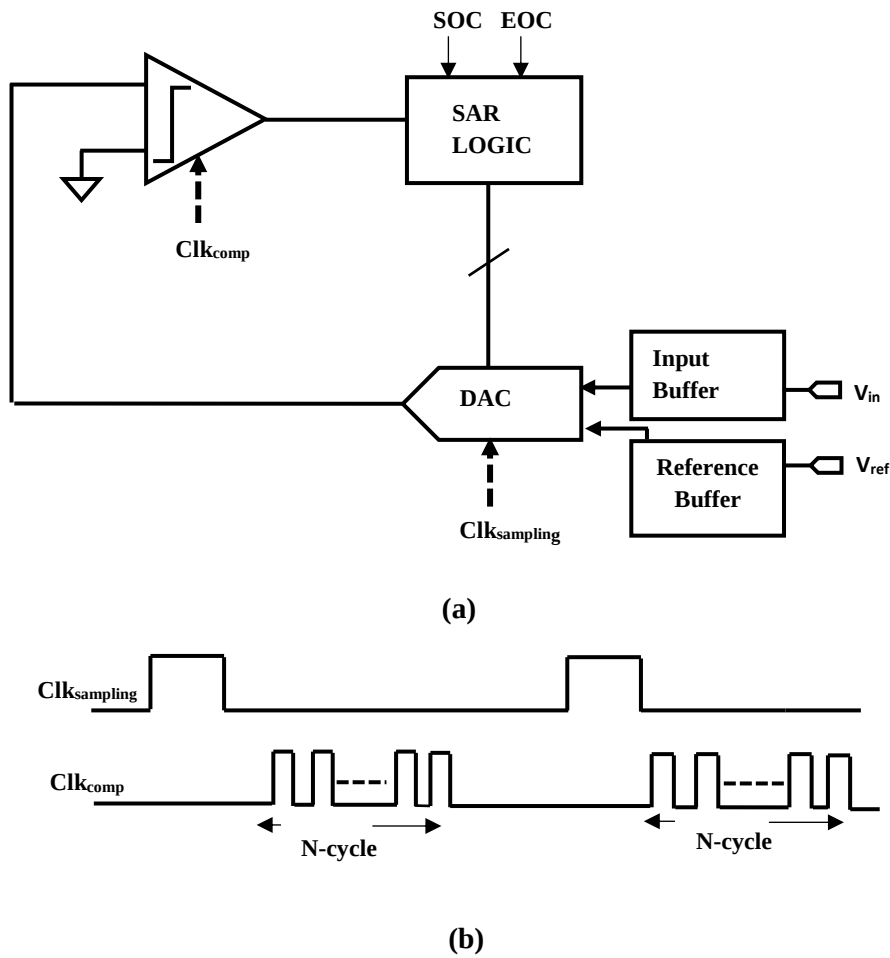


Fig. 2.2 (a) SAR ADC block diagram and (b) Clock timing pulses

The Fig. 2.2 (b) shows that in one $Clk_{sampling}$ period, N cycles of Clk_{comp} are used to convert an analog sampled value into its digital equivalent. Now, this research review is directed to each module of SAR ADC and the review is organized by focusing separately on the key modules of the SAR ADC, enabling a clear understanding of how each contributes to overall performance and efficiency of SAR ADC.

2.4 DIFFERENT EXISTING DYNAMIC COMPARATORS FOR SAR ADC

Comparator is the main block of a SAR ADC that converts sampled analog voltage into digital equivalent output. A comparator is designed to avoid the consumption of static power so as to make it employable for ultra-low power applications. In this view, dynamic comparators in comparison to static comparators are designed to be utilized in analog to digital converters (ADCs) with their key benefit of low power applications. A dynamic comparator consists of a pre-amplifier to amplify input analog signal, followed by latch regeneration initiated by turning ON of PMOS cross-coupled pair of latches facilitating positive feedback [36]. Many researchers worked on the different architectural variations of dynamic comparators to reduce noise, offset voltage, power consumption at different technology nodes and clock frequency [37-39]. Major literature work of dynamic comparators is briefed in Table 2.3 along with the key finding and the major contribution of each work in the field of dynamic comparators design.

Table 2.3: Comparative study of existing dynamic comparators

S.No.	Year	Reference	Structure	Tech.	V _{DD}	Energy per conversion / power consumption	Input referred offset voltage	Area
1	2009	Bernhard Goll <i>et al.</i> [40]	Dynamic Comparator (Bernhard)	65 nm	1.2 V	128 μ W	6.1 mV	1394.44 μ m ²
2	2011	Ili Shairah Abdul Halim <i>et al.</i> [41]	CMOS Charge Sharing Dynamic Comparator	180 nm	1.8 V	0.46 mW	NA	2220 μ m ²
3	2014	Samaneh Babayan - Mashhadi <i>et al.</i> [42]	Modified Dynamic Comparator	180 nm	0.8 V	0.24 pJ/conv.	7.8 mV	392 μ m ²
4	2016	P. Bahmanyar <i>et al.</i> [43]	Double tail Latched Comparator	180 nm	0.6 V	1.56 nW	7.57 mV	209 μ m ²
5	2017	Harijot singh Bindra <i>et al.</i> [44]	Dynamic Bias Comparator	65 nm	1.2 V	32 fJ/conv.	5.4 mV	125 μ m ²

6	2017	G. De La Fuente-Cortes <i>et al.</i> [45]	CMOS Comparator	65 nm	1.2 V	3,76,000 nW	0.0367 mV	NA
7	2018	V. Savani <i>et al.</i> [46]	Charge Reset Technique Comparator	90 nm	1 V	32,620 nW	7.7 mV	58.32 μm^2
8	2018	A.K. Dubey <i>et al.</i> [47]	CMOS Double Tail Dynamic Comparator	45 nm	0.8 V	1728 nW	2.78 mV	49.35 μm^2
9	2018	Harijot singh Bindra <i>et al.</i> [48]	Dynamic Bias Latch Type Comparator	65 nm	1.2V	30 fJ/conv.	0.4 mV	125 μm^2
10	2020	Xiyuan Tang <i>et al.</i> [49]	Comparator With Dynamic Floating Inverter Amplifier	180 nm	1.2V	1 pJ/conv.	46 μV	9800 μm^2
11	2020	N. Shahpari <i>et al.</i> [50]	High Precision Dynamic Comparator	180 nm	1.8 V	41,000 nW	0.628 mV	5100 μm^2
12	2022	S. Nejadhasan <i>et al.</i> [51]	Dynamic ADC Comparator IOT	65 nm	1 & 0.5 V	3550 nW	NA	230 μm^2
13	2023	M. Vafaei <i>et al.</i> [52]	Dynamic Comparator (biomedical)	65 nm	0.2 V	0.0531 nW	8.74 mV	NA
14	2024	Zahra Mehrabi Moghadam <i>et al.</i> [53]	Ultra-Low Power Dynamic Comparator	65 nm	NA	141.4 pW	3.32 mV	106.8 μm^2
15	2025	Nidhi Sharma <i>et al.</i> [54]	Rail-to-Rail Dynamic Comparator	65 nm	1.2 V	232 fJ/conv.	1.85 mV	389 μm^2

As from Table 2.3, in 2009, Bernhard Goll *et al.* [40] implemented a dynamic comparator with reduced delay time in 65nm CMOS at supply voltage of 1.2 V. In the Bernhard design, circuit of conventional latch comparator including two cross coupled inverters is modified to reduce the delay taken by latching operation of dynamic comparator. Due to this, delay time was reduced to 104 ps for 15 mV input at 1.2 V supply with reduced offset voltage to 6.1 mV. Further, it is also validated in the existing designs that power consumption of dynamic comparator increases with increase in clock frequency which is 1.56 nW at 0.01 MHz for the

comparator designed by P. Bahmanyar *et al.* [43] and it increases to 2.65 mW at 6 GHz in the dynamic comparator designed by Bernhard Goll *et al.* [38]. Also, pre-amplifier gain of dynamic comparator works to attenuate the kickback, noise, and offset voltage to reduce the overall noise of comparator.

However, static comparator offers high gain, more rigidity towards process, voltage, and temperature (PVT) variations but at the cost of higher power consumption. For low power applications, comparators with dynamic pre-amplifiers became popular. One of the unresolved issues was pre-amplifier input transistors were starting from linear region due to which gain of preamplifier was not being of appropriate value as required to minimize the comparator's noise and offset. To resolve this, one of the modified architectures was developed by Miyahara *et al.* [39] to ensure that the latch input transistors initially operate in the saturation region, resulting in increased gain and decreased noise of comparator along with reduced offset voltage upto 1.69 mV at 250 MHz while dissipating 40 μ W/GHz (20 fJ/conv.) at 1V supply. Further, as per recent advancement in 2024, Zahra Mehrabi *et al.* [53] presented an ultra-low power comparator with intermediate switches to break the connection between latch & pre-amplifier during the precharge phase, thereby lowering overall power consumption. Also, it served the target of reducing parasitic resistance of the discharge path during the evaluation phase to increase the effective transconductance of the latch. The design was implemented in 65 nm technology node to limit the power consumption of 141.4 pW along with good delay and offset voltage of 357 ns and 3.32 mV respectively. Now, existing major architectures of dynamic comparators are presented in the next sub section 2.5 for better visualization of the designs.

2.5 ARCHITECTURES OF MAJOR EXISTING DYNAMIC COMPARATORS

In the literature, different architectures of designed dynamic comparators have been presented by the researchers to employ their utilization for SAR ADC. Maximum of existing architectures are voltage mode dynamic comparators consisting of pre-amplifier and latch. In dynamic comparators clock (clk) signal plays an important role as circuit works in synchronization to the clock signal. Strong arm latch also known as conventional dynamic comparator [37] shown in Fig. 2.3 is the baseline comparator design that compares two sampled values, but it has limitation in the performance including energy efficiency and speed. However, its performance is limited in terms of energy efficiency and operating speed. Consequently, over the past decade, researchers have introduced several advanced dynamic comparator architectures that surpass the Strong-Arm latch across multiple performance metrics. One notable example is the

two-stage dynamic comparator proposed by Bernhard Goll et al. [38]. This topology shown in Fig. 2.4 has reduced the stacking of transistors due to which it can operate at lower supply voltages compared to conventional one and also lowers the overall power consumption of the circuit. The architecture separates the preamplifier stage from latch stage, which significantly enhances latch regeneration speed and consequently reduces the comparator delay.

Fig. 2.3 Architecture of Strong-Arm Latch dynamic comparator

However, a key drawback is that the latch input transistors initially operate in the linear region, which lowers the effective interstage gain. This degradation results in increased noise and offset contributions originating from the latch. To reduce the noise effect, the pre-amplifier gain of the comparator is increased by Samaneh Babayan-Mashhadi *et al.* [42] by inclusion of additional transistors M3 and M4 in the modified double tail dynamic comparator as shown in Fig. 2.5. Also, with inclusion of transistors M3/M4 with input as F_n/F_p , the voltage difference generated at the first stage ($\Delta F = F_p - F_n$) is increased, which consequently enhances the initial differential voltage at the latch stage ($\Delta V_{out} = out_p - out_n$) during regeneration. This larger voltage difference accelerates the latch regeneration process, thereby reducing the overall delay of the comparator. Designing of new architectures of dynamic comparator continued by the researchers in the literature but still there is scope to further reduce the power consumption of dynamic comparator with proper isolation between preamplifier and latch stage. It is good to add transistor in the series of pre-amplifier transistors that Hsieh and Hsieh [55] used as vertical

The diagram illustrates a 1T1R1C1 SRAM cell. The top section shows a 1T1R1C1 structure with access transistors M5 and M6, storage transistors M3 and M4, and a read current source M8. The bottom section shows a 1T1R1C1 structure with access transistors M9 and M10, storage transistors M1 and M2, and a read current source M12. The circuit is powered by VDD and ground, with inputs CLK, INN, INP, and outputs outn, outp.

[illegible]

28

Mentioned techniques improved the energy efficiency by improving pre-amplification gain. In designs, pre-amplifier load C_L gets completely discharged to ground during the process of comparison which consumes energy of $2 C_L V_{DD}^2$ which is fixed. It leads to the evaluation that pre-amplifier is the major power-hungry block in dynamic comparator which consumes approximately 80% of total consumed power in dynamic comparator. This created an important requirement to improve the energy efficiency of pre-amplifier itself. So, reduction of energy consumption of dynamic comparator is always an area of concern for the researchers. In addition to low energy consumption, reduction of noise and offset of comparator attracted researchers to work in this domain.

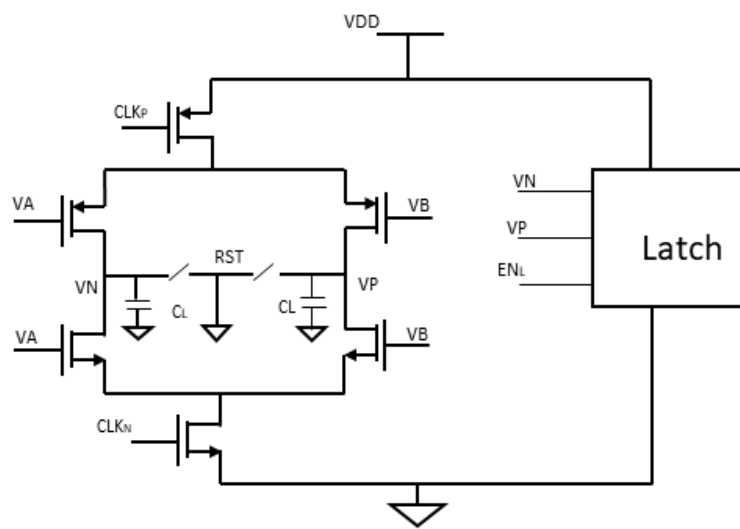


Fig. 2.6 Architecture of Bi-directional dynamic comparator

Two stage dynamic comparator proposed by Schinkel *et al.* [56] as a low power dynamic comparator in which latch stage was separated from pre-amplifier stage to disconnect direct connection between supply and ground. In this design, the separation increased the latch regeneration speed that reduces comparator delay in the design, but preamplifier stage of input transistors starts from the linear region which still reduces the interstage gain and lead to the increased noise and offset of the comparator. To overcome this issue, Van Elzakker *et al.* [57] changed the design in which input latch transistors made to start from the saturation region leading to increased gain and reduced comparator noise. Further, in 2016 Liu *et al.* [58] developed a dynamic comparator based on bidirectional pre-amplifier stage in Fig. 2.6. In the architecture, pre-amplifier includes both PMOS & NMOS input transistors. PMOS transistors in input pair gets charged from potential zero in the first half phase of pre-amplification and as soon as their output crosses mark of half V_{DD} , PMOS pair gets turn off and NMOS pair switches

ON to continue the second half phase of pre-amplification. In this way, load capacitance of preamplifier gets returned to the original voltage stage to avoid the power consumed in resetting and with energy consumption of $C_x V_{DD}^2$ with same preamplification gain and offset at an energy efficiency improvement by approximately one and half times with inclusion of extra power cost in extra needed circuit. Further, powering the FIA using a floating reservoir capacitor ensures a constant output common-mode voltage, which extends the preamplification duration and enhances the gain, as illustrated in Fig. 2.7. Additionally, it prevents common-mode discharge of the load capacitor, resulting in significant energy savings.

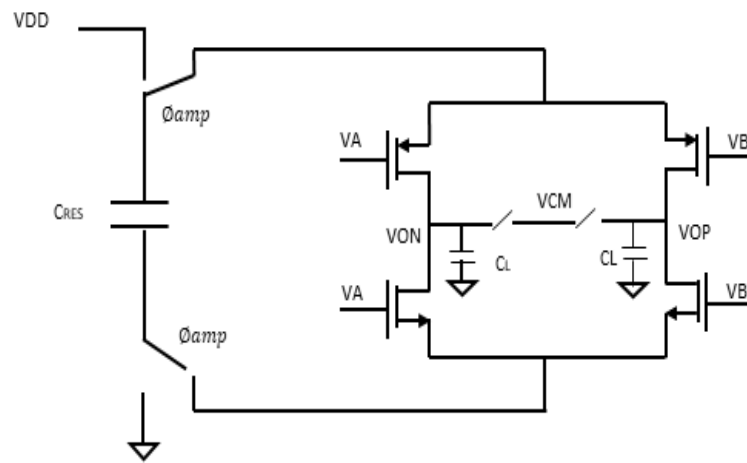


Fig. 2.7 Architecture of Floating Inverter Amplifier based comparator

Table 2.4: Performance analysis of pre-amplifier module in different dynamic comparators

S.No.	Architecture	Energy Saving Efficiency	Pre-Amp Gain	Area Efficiency	Speed	Sensitivity
1	Conventional Double Arm Latch	Poor	Poor	Good	Good	Very Good
2	Dynamic Biasing	Medium	Medium	Good	Poor	Very Good
3	Floating Inverter Amplifier	Good	Good	Poor	Poor	Medium
4	Bidirectional	Medium	Poor	Good	Good	Poor

In Table 2.4, a comparative overview of recent comparator pre-amplifiers is presented. The conventional design continues to be widely adopted for its straightforward structure and rapid operation, whereas the FIA demonstrates clear advantages for low-power systems by offering high gain, energy efficiency, and reliable performance. Further, many researchers considered the reduction of kickback noise which arises from the large voltage swing at the drain of input pair transistors in the design of dynamic comparator. High voltage switching give rise to current flow to pass through the drain-gate parasitic capacitor to the input voltage. Kickback noise is also an important parameter to improve the resolution of a dynamic comparator.

Pedro M. Figueiredo *et al.* [59] proposed kickback reduction techniques as (i) Reducing the variations in voltage at the drain of the differential pair. (ii) The differential pair drains are disconnected from the regeneration nodes using switches which are opened during regeneration phase using neutralization techniques: When drain voltages of input differential pair vary, the circuit preceding the comparator, retains nonzero impedance, in this technique two capacitances with value $C_N = C_{GD}$ are added in the way to cancel the kickback noise. Mansoure Yousefirad *et al.* [60] presented a method to reduce both common mode and differential mode components of kickback noise in the dynamic latched comparator. In this research, kickback noise of dynamic comparators is reduced by decreasing the slew-rate of drain and source voltages of the input transistor pair. Using the above method both differential and common mode component of kickback noise gets reduced as given in Table 2.5. The technique was implemented in conventional dynamic latch comparator.

Table 2.5: Comparison of kickback noise in different dynamic comparators [59-60]

Parameter	Conventional dynamic Latch Comparator	After Kickback Noise reduction [60]	After Kickback noise reduction & offset calibration [60]	Pedro M. Figueiredo [59]
Max Kickback Noise Current/voltage	4.37 μ A	1.4 μ A	1.4 μ A	4 mV
DC Offset	12.3 mV	13.8 mV	0.3 mV	NA
Power Dissipation	2.89 μ W	2.86 μ W	2.86 μ W	NA

The summarized view of this literature depicts that in a dynamic comparator, pre-amplifier and latch both are clocked and given as clk and inverted clk signal to create precharging of required output nodes in which generation of inverted clk signal may be avoided. Further, for reduction of power consumption of comparator circuit, the isolation between preamplifier and regeneration latch is required to avoid the power dissipation in the circuit. Further, the delay of the comparator is given as $t_{\text{delay}} = t_o + t_{\text{latch}}$, t_o is the time taken by the comparator circuit till one of its regenerative PMOS latch transistor gets switched ON and t_{latch} is the time taken by regeneration latch when $V_{\text{outp}} - V_{\text{outn}}$ creates a difference of $V_{\text{DD}}/2$ given as eq. (2.2) and eq. (2.3)

$$t_{\text{latch}} = \frac{C_L}{g_{M,\text{eff}}} \ln \frac{\Delta V_{\text{out}}}{\Delta V_o}, \quad (2.2)$$

$$t_{\text{latch}} = \frac{C_L}{g_{M,\text{eff}}} \ln \frac{|\Delta V_{\text{outp}}(t=t_1) - \Delta V_{\text{outn}}(t=t_1)|}{|\Delta V_{\text{outp}}(t=t_0) - \Delta V_{\text{outn}}(t=t_0)|}. \quad (2.3)$$

So, to reduce the delay of dynamic comparator, the pre-amplifier gain stage must have high gain which is possible by its biasing in the linear region or including cascade transistors in series with the pre-amplifier stage transistors. Fluctuation in the output causes kickback effect on the input due to which minimum difference voltage between two compared inputs gets affected and comparator may produce erroneous output. These highlights have formed the basis in design of low power comparator in the proposed project. Further, in the next subsection 2.6, detailed literature review of next module of SAR ADC that is Digital to Analog Converter (DAC) is considered.

2.6 EXISTING LOW POWER SWITCHING TECHNIQUES FOR DAC DESIGN

As already discussed, that comparator, digital to analog converter (DAC) and SAR logic-based control unit are the three major modules of SAR ADC. Among these modules, DAC unit consumes the maximum energy and area compared to other modules. Therefore, implementation of digital to analog converter (DAC) unit with reduced switching energy and area became the core interest of working for the researchers in the design of ultra-low power SAR ADC. Based on design and switching scheme of DAC, the single ended and differential SAR ADC architectures become two prominently available designs incorporating SAR logic. Single ended SAR ADC is best utilized for the applications requiring low power consumption as major constraint compared to high SNR while differential architecture is preferred for high acceptable SNR in the digitized output. Further, many differential and single ended designs have been developed with the help of several low power switching schemes considered for the

design of low power SAR ADC [61-67] with an aim to reduce the energy dissipation in switching process of implemented capacitive DAC to reduce the energy consumption of overall conversion process. To start with, a fully differential conventional switching scheme for n bit SAR ADC [21] using 2^{n+1} unit capacitors (single ended prototype) is presented in literature. In that design, the differential inputs are sampled using the bottom plates of capacitor array. Once sampling is completed, the DAC network is rearranged so that the comparator receives V_{in} , with the MSB capacitor tied to V_{refp} while the remaining capacitors are linked to V_{refn} . The comparator's output then iteratively adjusts the differential DAC, gradually driving both top-plate voltages toward V_{cm} , thus accomplishing the SAR conversion [68].

However, this conventional switching approach is not energy efficient because of the repeated switching in the differential DAC. Moreover, nearly half of the output codes require preset–evaluate–reset cycles, which further increase power consumption. While [21] employs bottom-plate sampling, a top-plate sampling scheme would consume a similar amount of energy. Although top plate switching can reduce the energy required for MSB reconfiguration, it still incurs additional reset power overhead. To work out with this issue, Liu *et al.* [69] worked on the monotonic switching scheme.

Table 2.6: Comparison of multiple DAC switching schemes in literature

S.No.	Architecture	Energy Conversion (CV^2_{ref})	Normalized Total Energy	No. of Unit Capacitors (C)
1	Traditional single ended [68]	682.5	1	2^{N+1}
2	Split Capacitor [75]	427.66	0.62	2^N
3	Monotonic [69]	255.5	0.37	2^N
4	Vcm-based, Zhu [76]	170.17	0.249	2^N
5	CAS based [77]	88.6	0.129	2^N
6	Merged Capacitor [78]	84.7	0.124	2^{N-1}
7	Weibu Hu [79]	84.7	0.124	2^N
8	Bi-directional [70]	42.7	0.062	2^{N-1}

Multiple DAC architectures are reviewed in literature for SAR ADC [70-89] by the researchers which are further discussed. In monotonic switching scheme the overall capacitance of DAC arrays is limited to $2^N C$ which is 50 percent reduced value compared to conventional scheme. Also, in the switching scheme, top plate sampling is utilized, and scheme facilitates the first MSB comparison with zero switching energy. Consequently, the proposed scheme realizes a

63% reduction in switching energy per conversion step when compared with the conventional switching approach. However, in the switching all the capacitors can switch from V_{refp} to V_{refn} due to this, the common mode voltage reduces from V_{cm} to zero which in turn decreases the comparator performance and several factors like noise, offset gets affected in the undesirable direction. Further, common mode variations reduction was kept on priority in the switching scheme presented by A. Sanyal *et al.* [70] as bidirectional single side switching technique. This approach follows the single-sided capacitor switching method described in [69] but extends it by allowing the DAC bottom plates to reset to either V_{refp} or V_{refn} . Consequently, the DAC output common-mode voltage can shift in both directions, which helps minimize variation. When combined with a redundancy mechanism, this strategy alleviates the adverse effects of common-mode variation on ADC performance [71-72].

By adjusting the reset voltages, different output common-mode variation patterns can be achieved, enabling optimization for either higher speed or lower noise [73-74]. Table 2.6 incorporates a comparative study of several DAC switching schemes in terms of energy and no. of used capacitors. The incorporation of V_{cm} significantly lowers switching energy, achieving a 66% reduction in switching power compared to the conventional approach. However, this method necessitates an additional reset circuit and a dedicated V_{cm} generation circuit if one is not already present. Zhu *et al.* [76] proposed a V_{cm} -based switching scheme in which the bottom plates are maintained at the V_{cm} potential during the sampling phase.

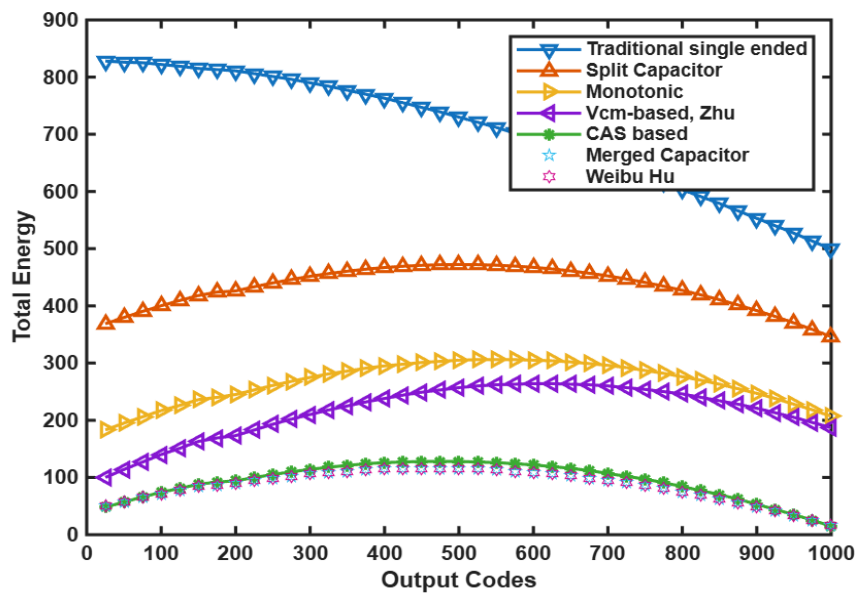


Fig. 2.8 Switching energy comparison of different DAC switching schemes

Further, during switching, keeping bottom plates at V_{cm} instead of ground, reduces energy

consumption from V_{ref} and as a result, it achieved 75% reduction in switching energy compared to traditional single ended at the increased value of driving energy required by switches. Further, to remove V_{cm} , Ginsberg *et al.* [75] splitted the capacitor array into two equal sub capacitors that are reset to V_{refp} and V_{refn} .

Table 2.7: Parametric representation of low power switching techniques in DAC

S.No.	Year	Reference	Contribution	Key Finding
1	2016	Wan Kim <i>et al.</i> [89]	A time-interleaved SAR ADC architecture enhanced with asynchronous SAR assistance (SATI-SAR)	1. DNL = 0.24 LSB, INL = 0.45 LSB, 2. ENOB =10.4 bits, Power = 83 μ W, 3. Fs= 10 MS/s , Resolution =12 bits, 4. FOM = 79.9 fJ/ conv.step.
2	2018	Sreenivasulu Polineni <i>et al.</i> [83]	Enhanced MSB capacitor split switching technique	1. 90nm technology node, 2. Sampling frequency = 10 KS/s, 3. Power consumption = 337.66 nW.
3	2020	Babita Jajodia <i>et al.</i> [84]	Energy efficient DAC switching technique	1. 10-bit SAR ADC, 40 MS/s, 2. SNDR = 55.97 dB at 2 MHz, 3. ENOB = 9 bits, 4. DNL = -0.23/0.32 LSB, INL = 0.31/0.04 LSB.
4	2022	Xin Zhao <i>et al.</i> [88]	A single-ended SAR ADC architecture tailored for low-power implantable biosensor systems	1. 65nm CMOS tech., 0.6V & 200KS/s, 2. SNDR = 56.42 dB, SFDR = 66.14 dB, 3. FOM=0.87 fJ/conv step, 4. Power = 94 nW.
5	2022	Pieter Harpe [87]	Noise shaping SAR and pipelined ADCs	1. Bootstrapped switch for better linearity 2. Capacitor array with reduced energy.
6	2024	Dina M. Ellaithy [86]	8-bit 1-MS/s single-ended design	1. 130 nm CMOS , 1.2 V & 1 MS/s, 2. SNDR = 45.7 dB, ENOB = 7.3, 3. Power = 28.51 μ W, 4. Resolution = 10 bits.
7	2025	Zhijie yang <i>et al.</i> [85]	Noise shaping SARADC with data weighted averaging	1. 40 nm, 1.1 V, 2. 5 MS/s, Power = 303.2 μ W, 3. SNDR = 76.05 dB, 4. SFDR = 90.11 dB.

This method keeps the output common-mode level stable while minimizing dependence on V_{cm} . Functionally, the switching operation is similar to V_{cm} -based schemes, though it incurs extra reset energy. In total, it achieves about a 37% reduction in power consumption compared to the traditional single ended design. Further, Liou *et al.* [77] introduced the charge-average switching (CAS) method, where the DAC output voltage transition is achieved through charge sharing between the bottom plates of the differential DACs rather than traditional charging or discharging. This approach cuts power usage to nearly half of that in conventional designs. Fig. 2.8 depicts the comparison of major DAC switching schemes exists in literature. However, it relies on locally boosted switches to enable charge averaging, which becomes particularly difficult to implement in low-voltage systems. Majority of switching energy is consumed by the switching of MSB capacitor, reduction of MSB switching power holds prime importance specifically. Hsieh *et al.* [80] come up with a new technique known as semi resting switching method in which two identical sub-ADCs are employed to process the positive and negative inputs separately. This approach eliminates the highly energy intensive MSB DAC switching.

Further, Tai *et al.* [81] reported an ADC into coarse and fine submodules, the conversion process is divided such that the MSBs are obtained using a coarse ADC, while the LSBs are refined by a fine ADC. In this manner, unnecessary MSB switching within the fine ADC is completely eliminated. To further minimize overall energy consumption, a low-power ADC is employed as the coarse stage, enabling the design to achieve an energy efficiency of 1 fJ per conversion step. Alternatively, Lee *et al.* [82] reported a 2-bit coarse ADC implementation based on a single comparator, in which the polarity of the MSB is first identified, and the subsequent bit is resolved by evaluating the comparator decision time using an accurately calibrated delay element. Moreover, incorporating suitable reference voltage also drew attention to the researchers for reduction of further switching energy of capacitive DAC. In this regard, scaling of reference voltage from V_{ref} to $V_{ref}/2$ is adopted in single ended SAR ADC for the conversion of input signal with range $[0, V_{ref}]$. In [83], a fully differential switching scheme is presented to reduce energy consumption. A single reference voltage was utilized in the DAC switching [84] to perform digitization. Liu *et al.* worked on monotonic capacitor switching approach [64] which saved 81 percent of switching energy compared to conventional switching and 50% of total capacitance was reduced. Further, incorporation of multiple switching techniques results in obtained parameters as given in Table 2.7.

Among the switching schemes, split capacitor [75] and common mode voltage based [76] based are adopted majorly by the designers due to balanced approach of energy efficiency,

implementation simplicity and good control over common mode voltage shift for better linearity of comparator. As summarized from literature review of low power switching technique in Table 2.7, DAC module usually utilize the charge- redistribution techniques to create the comparison voltages stagewise with the input analog sampled voltage. A differential DAC consists of symmetric DAC arrays at the positive and negative input terminal of comparator to create the mentioned comparison voltage which digitize voltage between $[-V_{ref}$ to $V_{ref}]$ and single ended DAC digitize voltage from $[0, V_{ref}]$. In every stage, the switching of capacitors is required so as to achieve the required comparison voltage and this switching consumes switching energy/conversion step. The MSB switching consumes maximum energy. Keeping above in considerations, to reduce the power consumption of ADC, the switching energy in atleast first two MSB comparisons must be carried out without any switching energy per conversion step. Number of capacitors limit the area of DAC module which is also a consideration to be taken care in the design of an energy efficient DAC.

2.7 DIFFERENT CAPACITOR LAYOUTS FOR DAC DESIGN IN LITERATURE

In addition to lowering switching activity, the DAC capacitor size should be minimized toward the thermal noise boundary to achieve better power and area efficiency. However, this goal is often restricted by the smallest feasible unit capacitor size and the requirements for mismatch tolerance. A brief view of capacitor layout and advantage is presented to implement the DAC array of ADC in Table 2.8. Layout of used capacitor like strip capacitance, metal-insulator-metal (MIM) based, metal-oxide-metal (MOM) based are chosen by the researchers to mainly reduce the parasitics along with edge & fringe field coupling effect.

Table 2.8: Different capacitor layouts for DAC design in literature

S.No.	Year	Author	Capacitor Layout	Advantage
1	2010	Liu <i>et al.</i> [69]	MIM & MOM , multi layered sandwiched capacitor	Simplified layout routing
2	2011	P. J. A. Harpe <i>et al.</i> [90]	0.5 fF finger capacitors with top metal layers	Reduction of parasitic Capacitance
3	2012	C.-H. Chan <i>et al.</i> [91]	Multiple layered crossing metal	Reduction of fringe field Coupling
4	2013	G.-Y. Huang <i>et al.</i> [92]	Encapsulated MOM	Reduction of parasitic

			capacitor design	Capacitance
5	2017	Wenbin Bai <i>et al.</i> [93]	MIM capacitor	Unit capacitor is 24.3 fF with reduced parasitics
6	2019	P. Harpe <i>et al.</i> [94]	Strip capacitance	Reduction of Relieves edge effect
7	2022	Xin Zhao <i>et al.</i> [88]	Customized MOM capacitor	Improve consistency of CDAC
8	2024	Mirosław Firlej <i>et al.</i> [30]	large Metal-Insulator-Metal (MIM) capacitors	Reduced parasitics
9	2025	Zhijie yang <i>et al.</i> [85]	FWS technology	Capacitor mismatch reduction

MOM based capacitors offers major area efficiency compared to MIM capacitors. Mismatching of capacitors creates nonlinearity in the output converted voltage which requires proper attention to be considered. Also, in conventional switching scheme, 2^{N+1} unit capacitors are required in the capacitor array of designed DAC. Switching of MSB capacitor consumes maximum switching energy [95]. First few comparisons are required to be carried out without any switching energy consumption from supply. So, layout of capacitors plays an important role in the overall performance of DAC design in terms of area requirement. For low power applications, Metal-oxide-metal (MOM) capacitors are the best choice among researchers as they can be fabricated using the existing metal layers of a standard CMOS process, which removes the need for any additional steps and keeps fabrication cost-effective. Their structure also results in lower parasitic effects and better voltage linearity, making them suitable for precision analog and mixed-signal circuits. MOM capacitors offer good matching performance, low leakage, and stable operation across a wide range of voltages and frequencies. These advantages make them a reliable choice for applications such as ADC capacitor arrays, filters, and RF circuits.

2.8 CAPACITOR MISMATCH REDUCTION TECHNIQUES

Low power switching technique demands the reduced size of unit capacitor but with reduction in capacitor minimum size, the utilization of binary weighted capacitors of such reduced value of the order of femto farads led to increase in the mismatch issue of capacitors which in turn

affect the linearity of analog to digital converter. To resolve such issues and for higher precision, many solutions are considered by the researchers in the literature. Analog compensation technique was reported by Lee *et al.* [96] In this approach, mismatch in an individual capacitor of the main DAC is converted into an equivalent error voltage by interchanging the bottom-plate voltages between the capacitor under evaluation and the reference capacitors. Ding *et al.* [97] proposed an analog calibration technique based on stepwise feedback-loop correction through sign-error detection. The method identifies only the polarity of the error by introducing an additional trial at the end of the SAR conversion phase, after which accurate analog correction is achieved using a multi-step feedback mechanism that relies on repeated error detections. Apart from analog calibrations researchers also worked upon the digital calibration techniques in which weight of capacitor can be varied to minimize the mismatch cost function using least mean squares (LMS) adaptive algorithm off chip [98] or on chip [99].

Along with calibration strategies, error-shaping approaches are used to compensate for capacitor mismatch, taking advantage of the fact that Nyquist-rate ADCs are generally sampled at rates that are multiples of the Nyquist frequency, thereby easing anti-aliasing requirements. Dynamic element matching (DEM) offers the mismatch error shaping methodology in delta - sigma ADCs. But with increase in resolution, the complexity of DEM technique increases. To address this limitation, Shu *et al.* [100] introduced an error-feedback (EF) mismatch error shaping (MES) technique that is especially well suited for high-resolution SAR ADCs. In this method, the residue from the previous conversion cycle is fed back and reused during the subsequent sampling phase.

This mechanism feeds the mismatch error from the earlier cycle back into the system and cancels it in the current cycle, effectively shaping the mismatch error with first-order characteristics. With reduction in unit capacitor size and to make sure about the DAC linear behaviour, capacitor mismatch reduction holds major concern to be taken care by the researchers. However, digital calibration has been widely adopted by the industries with increase in computational power [98]. Finally, it is inferred that reduction of switching energy per conversion step in the DAC design along with proper layout of capacitors and mismatching consideration so as to reduce the area requirement design are major design factors to be taken care while designing an ultra-low power SAR ADC.

2.9 REVIEW OF SAR LOGIC BASED CONTROL UNIT DESIGNS

SAR logic implementation using a control unit is one of the important modules in the design of SAR ADC. Based on the comparator output, the control unit has to perform switching of the DAC unit in accordance with bottom plate sampling or top plate sampling approach so as to achieve the proper comparison voltage in the process of digitization of an analog sampled signal. There exist multiple control unit designs like counter based, shift register based, and internal clock signal generation based. Some of the major control unit designs presented in literature are summarised in Table 2.9.

Table 2.9: Different existing control units designed to implement SAR logic

S.No.	Year	Author/Year	Contribution	Key Finding
1	2016	Dai Zhang <i>et al.</i> [101]	Synchronous control logic including shift registers.	1. Comparator output stored in Latch with combinational logic generates control signals, 2. Single conversion = 17 clock cycles, 3. Power consumption is 100 nW.
2	2017	Wenbin Bai <i>et al.</i> [93]	A synchronous control logic for the 10-bit SAR ADC is adopted.	1. Bit slice unit incorporation, 2. Two latches each comprised by two inverters, are used to keep the digital codes P_i and N_i for a long time.
3	2018	Sreenivasulu Polineni <i>et al.</i> [83]	A synchronous SAR logic for SAR ADC.	1. Uses total 12 clock cycles for the one sample conversion, 2. Sampling need 02 clock cycles (initial), Data conversion = 10 clock cycles.
4	2022	Xin Zhao <i>et al.</i> [88]	Single-Ended SAR ADC.	1. 0.6 V, 94 nW, Implantable Biosensor applications, 2. Shift register based control unit designed, 3. 200 KS/s, 10-bit design.
5	2024	Dina M. Ellaithy [86]	8-bit 1-MS/s single-ended SAR ADC.	1. 130 nm CMOS technology, 2. SAR logic consists of a code register and a ring counter.

SAR logic design summarized in Table 2.9 depicts that logic is created to control the switching of capacitors and it is completed required to synchronize with the DAC switching scheme. It is implemented with the help of D flip flops and multiplexers so that technology scaling plays a

good role to create its impact on the low power implementation. Proper flow of digitized data and performing proper switching of capacitor arrays are the major tasks of control unit. Researchers have worked on the consideration of low power supply for the ultra-low power circuit designing. Digital circuits exhibit two primary components of power consumption as active power and leakage power. Active power is directly proportional to $C_{\text{total}} V_{\text{DD}}^2$, where C_{total} denotes the effective capacitance of the digital circuit, incorporating both interconnect routing capacitance and intrinsic transistor parasitics, and V_{DD} is the supply voltage. Technology scaling inherently reduces C_{total} due to smaller feature sizes and decreased routing overhead. Furthermore, the reduction in transistor threshold voltages in advanced technology nodes enables the adoption of lower supply voltages, thereby reducing dynamic power dissipation [102 -103]. Low power designed techniques for SAR ADC is presented by Xiyuan Tang *et al.* [104] in detailed way along with the algorithm inclusion in the design approach is suggested by Hao-wei Lu *et al.* [105].

Consequently, modern low-power designs routinely employ aggressively scaled V_{DD} levels, with representative examples including 0.45 V in [81], 0.40 V in [80], and 0.30 V in [106]. Further, different techniques have been developed in literature to reduce the complexity of SAR logic and to further reduce the C_{total} . In a conventional system, sampling clock and comparator clock is generated by system clock. For N bit SAR ADC design, atleast one clock cycle is required for sampling and N cycles are required for comparison. System clock of $(N+1) F_s$ clock frequency is required for ADC running at F_s sampling frequency. Shift registers, D flip flops and multiplexers are the major blocks of SAR logic. Each clock cycle requires to trigger one D flip flop in the clock counter, one D flip in the sequence creation process and another one D flip flop to store data.

Further, research work has been continuously progressed to simplify SAR logic [107] for utilization in analog to digital converters. SAR sequencer is integrated with the clock-generation circuitry, resulting in an implementation that requires only a single shift-register chain. Moreover, a latch is employed for data storage in place of conventional D flip-flops (DFFs), thereby reducing the overall SAR logic power by approximately a factor of two, since only one DFF and one latch contribute switching activity per bit. Further, D flip flops can be implemented with dynamic logics as true single-phase clock (TSPC) [108-109]. In addition to active power, leakage power is also an area of concern in the design of ultra-low power SAR ADC within nW power restriction. To consider this issue, low leakage power circuit optimizations have been considered by the researchers. To reduce leakage, high threshold

voltage consideration, low supply voltage, increased stacking and long channel devices are the major possibilities available for the ADC designers. With proper consideration of these factors, still 25% fraction of total power comes out as leakage power [110]. To resolve this, power gating is one of the techniques implemented to reduce leakage in the designed circuit [111]. Also, after SAR conversion, circuit may be switched to a predefined logic state with minimum leakage power [112]. Further, after detailed literature review of comparator module in section 2.4, DAC module in sections 2.5 to 2.8 and SAR logic in section 2.9, work is further progressed to the literature review of complete SAR ADC design as presented in section 2.10.

2.10 REVIEW OF EXISTING SAR ADC DESIGNS AND TECHNIQUES

A complete SAR ADC design consists interfaced comparator, DAC and control unit with proper control of common mode voltage so that each module works in proper synchronization with an objective to digitize the input sampled analog signal. Design of SAR ADC includes low power dynamic comparator as one of its modules, resolution of comparator must be in accordance with the output digital bits of ADC. For n bit ADC, resolution is required to be $V_r/(2^n-1)$. DAC design require the utilization of low power switching technique and reduced capacitances. Some major existing designs of SAR ADC in literature with their output parameters are summarised in Table 2.10.

Table 2.10: Different designed SAR ADCs in literature with their parametric outputs

S.No.	Year	Reference	Contribution	Key Finding
1	2008	V. Giannini <i>et al.</i> [121]	Noise-Tolerant Dynamic-SAR ADC	1. ENOB = 8.23 bits, 2. SNDR = 51.31 dB, 3. F_{in} = 18.18 MHz, F_s = 40 MS/s, 4. INL = 1.2 LSB/ -1.2 LSB, DNL = 1.52 LSB/ -1 LSB.
2	2010	C. -C. Liu <i>et al.</i> [120]	SAR ADC with binary-scaled error compensation	1. 65 nm, 1.2 V, 2. 100 MS/s, 10-bit resolution, 3. ENOB = 9.51, 4. 1.13 mW power, FOM = 15.5.
3	2014	Pieter Harpe <i>et al.</i> [119]	Oversampled 12/14 bits SAR ADC with Noise Reduction	1. 65nm, 0.8V, 2. Resolution = 12 bits, 3. Sampling rate = 32 KS/s, 4. INL = 0.82 LSB, 5. DNL = 0.58 LSB, 6. SNDR = 67.8 , SFDR = 78.4.

4	2015	Reza Inanlou <i>et al.</i> [118]	Noise-shaping SAR ADC in 90 nm	1. 5-bit resolution, 2. Sampling rate = 1.6 MS/s, 3. Supply Voltage = 0.5 V, 4. Power Consumption = 4.4 μW, 5. SNDR = 59.6 dB, 6. ENOB = 9.6 bits.
5	2015	Z Zhu <i>et al.</i> [117]	Reconfigurable 2 MS/s power scalable SAR ADC	1. 8-bit SAR ADC, 2. Supply Voltage = 1 V, 3. SNDR = 48.11 dB, 4. Power Consumption = 15.98 μW, ENOB = 7.9 bits.
6	2018	Tayebeh Yousef [116]	Energy-Efficient DAC Switching Method	1. 10-bit ADC, 90 nm technology, 2. 100 KS/s, 3. ENOB = 8.5 bits, 4. Power = 0.5 μW, 5. SNDR = 52.84 dB.
7	2018	S. Chaput <i>et al.</i> [115]	Area-efficient 8-bit single-ended ADC	1. 8-bit SAR ADC at 1 MS/s. 2. Supply Voltage = 0.9 V 3. SNDR = 45.64 dB 4. Power Consumption = 29.7 μW 5. ENOB = 7.29 bits
8	2018	Sreenivasulu Polineni <i>et al.</i> [83]	An Enhanced MSB Capacitor split switching for SAR ADC	1. 90nm technology node, 2. Sampling frequency = 10 KS/s, 3. Power consumption = 337.66 nW.
9	2019	Yushi Chen <i>et al.</i> [114]	Energy efficient switching-scheme based SAR ADC	1. Capacitance reduction = 87 %, 2. DNL = 0.297 LSB, 3. INL = 0.310 LSB.
10	2020	Hao-wei Lu <i>et al.</i> [105]	Energy reduction algorithm for SAR ADC	1. Energy saving by reducing bit trials, 2. A new self-adaptive sub range window scheme to resolve issues of low success rate and weak adaptability of predicting SAR ADCs.
11	2020	Babita Jajodia <i>et al.</i> [84]	Single ended switching scheme for 10-bit SAR ADC	1. 10-bit SAR ADC at 40 MS/s, 2. SNDR = 55.97 dB at 2 MHz, 3. ENOB value of 9 bits, 4. DNL = -0.23 LSB/0.32 LSB, 5. INL = -0.31 LSB/0.04 LSB.
12	2021	G. A.,Fahmy <i>et al.</i> [113]	Memristor-based digital to analog converter (DAC) Design	1. 8-bit SAR ADC, 2. Supply Voltage = 1.2 V, 3. SNDR = 49.8 dB, 4. Power Consumption = 21 μW, 5. ENOB = 7.9 bits.

13	2022	Xiyuan Tang <i>et al.</i> [104]	A Comprehensive Review of State-of-the-Art Techniques in Low-Power SAR ADC Design	1. Voltage & Time Domain Comparators, 2. Noise Analysis in Comparators, 3. Multiple switching schemes comparative study.
14	2022	Xin Zhao <i>et al.</i> [88]	A SAR-Based Single-Ended ADC Targeted at Implantable Biosensing Applications	1. 65nm CMOS at 0.6V, 2. Sampling rate = 200KS/s, 3. SNDR= 56.42 dB, 4. FOM=0.87 fJ/conv step, 5. SFDR= 66.14 dB, 6. Power = 94 nW, 7. Resolution = 10 bits.
15	2023	M. Vafaei <i>et al.</i> [29]	A 0.2-V 1.2 nW 1-KS/s SAR ADC for biomedical applications.	1. 65 nm technology with 1KS/s, 2. Power= 1.21 nW, 3. Resolution= 10 bits, 4. DNL= 0.46/-0.95 LSB, 5. INL = 2.54 LSB /-2.74 LSB, 6. SNDR = 53.13 dB, 7. FOM= 3.2 fJ/conv-step, 8. SFDR = 62.47 dB.
16	2024	Mirosław Firlej <i>et al.</i> [30]	Ultra-low power with 50–90 MSPs SAR for ASICs.	1. 10-bit, 65nm technology, 2. ENOB= 8.9-9.2 bits at 50 MSPS, 3. ENOB = 9.3 bits at 40 MSPS, 4. Power consumption= 400 μW. 5. INL = 0.89 LSB, DNL =0.52 LSB.
17	2025	Sanchari Das <i>et al.</i> [31]	CDAC-based noise-shaping SAR ADC.	1. 8-bit split capacitor-based DAC, 2. SNDR = 69 dB, Sampling rate = 2 MSPS, 3. Power= 110 μW, Area = 0.07 mm² 4. Supply voltage = 1.8 V, 2 MHz for a bandwidth (BW) of 31 Hz.

In summary, the overall efficiency of a SAR ADC largely depends on the capacitor switching scheme used in the DAC, as this block contributes most to the power consumption and layout area. The DAC capacitor array must therefore use an optimized charge-redistribution switching technique, along with a comparator that provides good resolution at low power and a SAR logic unit designed to minimize leakage and reduce complexity. SAR ADCs based on this logic operate across a wide frequency range, from a few KHz up to several MS/s. As the operating frequency increases, key performance parameters such as power consumption, INL, and DNL must be carefully evaluated. Additionally, the SNDR and ENOB of the design determine the

effectiveness and accuracy of the ADC's conversion process. It has been inferred from literature that many different 8 bits and 10 bits SAR ADCs have been designed with sampling rate varying from few KS/s [29] to MS/s [30]. The power dissipation increases with increase in the sampling rate. To preserve the linearity of the device with increase in sampling frequency creates a major challenge for the researchers.

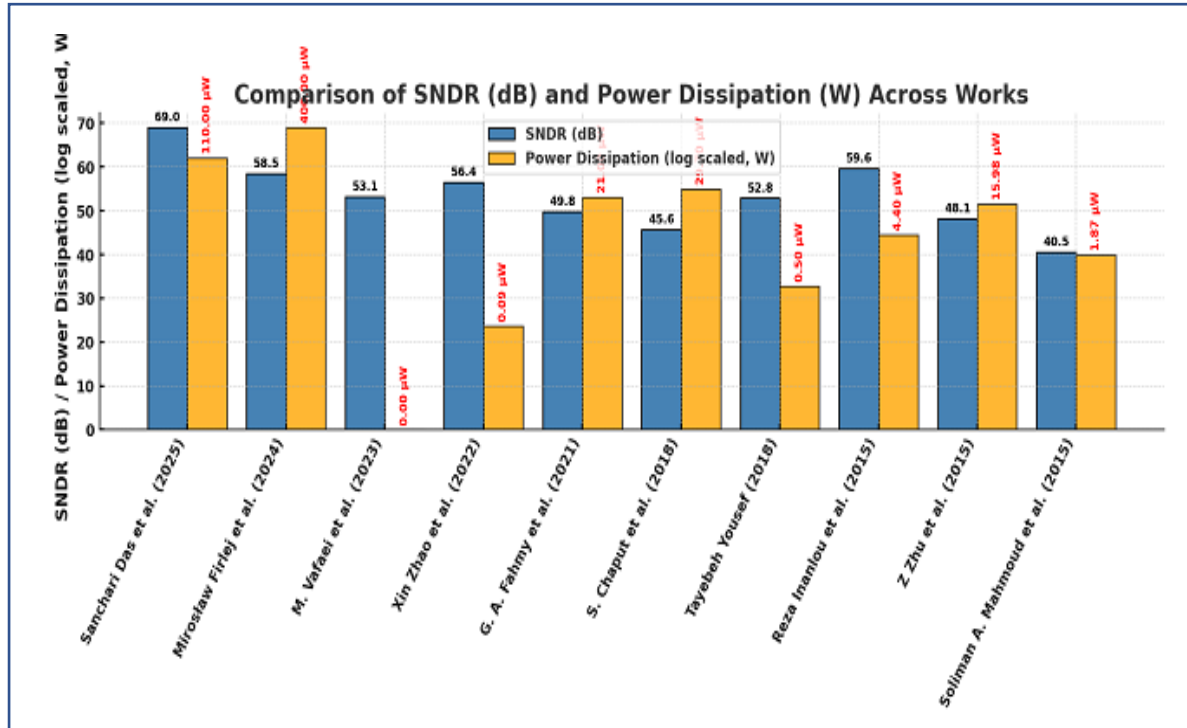


Fig. 2.9 SNDR and power consumption observation in existing SAR ADCs

As per recent advancements, for low sampling rate of the order of KS/s, power dissipation of the circuit is limited within few nW range, and it increase to the microwatt range as sampling rate gets increased to the order of MS/s as shown in Fig. 2.9. Also, Fig. 2.10 presents a summarized power consumption of different SAR ADCs at different sampling rates for the different major SAR ADCs designed in literature.

Table 2.11 summarises some major designs of SAR ADCs in literature carried out for 8 bit and 10-bit SAR ADCs. With inclusion of optimization techniques at architecture level of dynamic comparator, DAC and SAR logic, designed SAR ADC is analyzed for its power dissipation, INL, DNL, FOM, ENOB and the target sampling rate. In addition to the innovations in circuit design, researchers have started to explore the search algorithm to further reduce the power consumption of ADC. In reference to this, Liu *et al.* [123] and Huang *et al.* [92] reported the bypass window technique that allow SAR logic to bypass certain comparison steps when the input signal is known to fall within a predefined, narrow voltage range. This approach

minimizes unnecessary operations, leading to faster and more power-efficient conversions. Similar strategies have been explored in prior works [124], [125], [126].

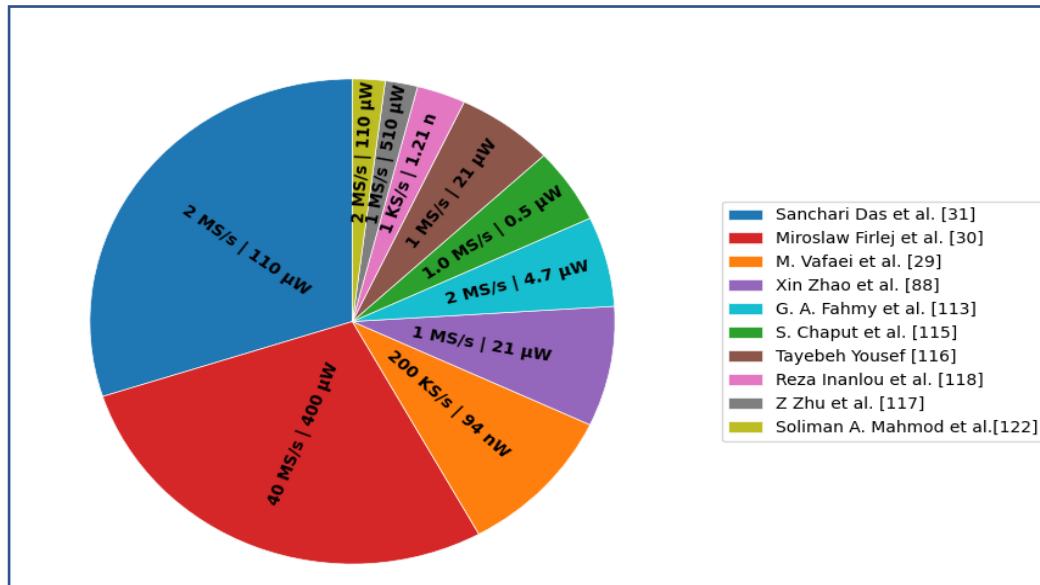


Fig. 2.10 Pie chart of operating frequency and power consumption in existing SAR ADCs

Further, investigations to reduce the switching activity by tracking the prior information about signal behaviour haven also been considered in the literature.

Table 2.11: Parametric analysis of existing 8 and 10-bit SAR ADCs

S.NO.	Year	Reference	Bits	Sampling Rate	Power Dissipation	SNDR
1	2025	Sanchari Das <i>et al.</i> [31]	8	2 MS/s	110.0 μ W	69.00 dB
2	2024	Miroslaw Firlej <i>et al.</i> [30]	10	40 MS/s	400.0 μ W	58.50 dB
3	2023	M. Vafaei <i>et al.</i> [29]	10	1KS/s	1.21 nW	53.13 dB
4	2022	Xin Zhao <i>et al.</i> [88]	10	200 KS/s	94.0 nW	56.42 dB
5	2021	G. A. Fahmy <i>et al.</i> [113]	8	1 MS/s	21.0 μ W	49.80 dB
6	2018	S. Chaput <i>et al.</i> [115]	8	1 MS/s	29.7 μ W	45.64 dB
7	2018	Tayebeh Yousef [116]	10	100 KS/s	0.5 μ W	52.84 dB
8	2015	Reza Inanlou <i>et al.</i> [118]	8	1.6 MS/s	4.4 μ W	59.60 dB
9	2015	Z Zhu <i>et al.</i> [117]	8	2 MS/s	15.98 μ W	48.11 dB
10	2015	Soliman A. Mahmoud <i>et al.</i> [122]	8	10 KS/s	1.87 μ W	40.50 dB

F.M. Yaul *et al.* [127] worked on analysing the signal pattern and proposed an ADC to decide LSB bit first. With emerging trends of VLSI design, researchers have analysed that 60 % to 70 % of total power consumption of ADC is consumed by DAC. The efficient energy schemes of DAC [128-129] reduces the energy per conversion step of the module which in turn reduces the overall power consumption of the ADC. Finally, designed ADC has to work in integration with other systems. Therefore, it is required to include the energy efficiency optimizations from system integration perspective. The overhead in the power consumption included by reference and input buffers also required to be worked upon. H. S. Bindra *et al.* [130] to reduce input drive energy of buffers, range pre-selection sampling techniques are presented. Also, H. S. Bindra *et al.* [131] included class A buffers to boost their driving capability at low energy requirement.

In a combined successive approximation register (SAR) analog-to-digital converter (ADC), the switching scheme of the DAC capacitor array constitutes the primary contributor to both the power consumption and silicon area. Therefore, the DAC requires an energy-efficient charge-redistribution switching strategy to reduce dynamic power dissipation and minimize area overhead. Furthermore, the comparator must be optimized to achieve high resolution with minimal energy consumption, while the SAR logic must be carefully designed to suppress leakage power and ensure robust and reliable conversion performance. Combining design techniques with electric design automation techniques (EDA), SAR design efficiency can also be improved. M. J Seo *et al.* [132] included synthesizable digital blocks with CDAC compiler in the design of SAR ADC to boost its energy efficiency.

2.11 RESEARCH GAPS

Based on the literature review of each module of SAR ADC, it is imperative to consider the figure of merit for the dynamic comparator module with the required resolution. Also, inclusion of energy efficient scheme for DAC design and proper switching control of SAR logic to design a SAR ADC for ultra-low power applications. Herein, some research gaps are identified and discussed in the following points:

- Need to design a dynamic comparator with improved architecture to eliminate connection between preamplifier and latch in reset mode to reduce power consumption of comparator. A comparator with single clock signal inspite of clock and inverted clock will surely eliminate the extra power consumption in generation of inverted clock signal. Also, the analysis of effect of differential voltage gain and g_m/I_d of input pre-amplifier transistors to

handle V_{cm} variations in a dynamic comparator is also a major aspect to be considered in the design of ultra-low power dynamic comparator for SAR ADC.

- Reduction of DAC switching energy per conversion step in the design of digital to analog converter holds major design consideration. In view of this, top plate sampling switching schemes needs to be incorporated to perform atleast first two comparisons without any switching activity to reduce the energy per conversion step. Also, reduced size of capacitor array in the implementation of considered switching scheme holds significant importance to be taken care in the DAC design.
- The literature highlights the necessity of SAR logic-based control unit and DAC co-optimization, especially when advanced switching techniques such as monotonic, common-mode (V_{cm})-based, and capacitor-splitting schemes are employed for switching. There exists a design requirement to reduce the complexity of control unit architecture to simplify the implementation of SAR logic and further, timing synchronization of control unit and the switching of capacitive DACs before next sampling pulse holds major design considerations so as to avoid non-linearity in the output.
- With inclusion of all optimized blocks of comparator, control unit and DAC, final interfaced low power SAR ADC with sampling rate of the order of KS/s is required to be designed with good FOM value. The proper interfacing of designed modules along with proper controlling of common mode voltage V_{cm} is equally important to result the interfaced circuit into an ultra-low power SAR ADC. The minimization of non-linearities in designed SAR ADC in terms of reduced differential non linearity (DNL) and integral non linearity (INL) with low power consumption holds the major design projection as literature highlights. Also, reduced power consumption and proper synchronization between the designed modules i.e comparator, DAC and control unit is highly required to design an ultra-low power SAR ADC.

CHAPTER-3

DESIGN AND ANALYSIS OF LOW POWER DYNAMIC COMPARATOR FOR SAR ADC

3.1 BRIEF INTRODUCTION ABOUT CHAPTER

Design of optimized comparator with reduced kickback noise, low power consumption along with reduced input referred offset voltage are the major designing assignments required for low power comparator module in a SAR ADC. A comparator is designed to avoid the consumption of static power to make it employable for ultra-low power applications. In this view, dynamic comparators compared to static comparators are designed to be utilized in analog to digital converters. A dynamic comparator comprises a pre-amplifier stage that amplifies the input analog signal, followed by a regenerative latch, in which positive feedback is initiated by activating the cross-coupled PMOS pair. Many researchers worked on the different architectural variations of dynamic comparators to reduce power consumption, kickback noise and offset voltage at different technology nodes and clock frequency.

Numerous power-saving methodologies have been proposed in scholarly works, including the imposition of voltage limitations at the preamplifier's output and the constraint of the preamplifier's output swing is observed in the literature. The analysis of effect of differential voltage gain and g_m/I_d of input pre-amplifier transistors to handle V_{cm} variations in a dynamic comparator is also a major aspect to be considered in the design of ultra-low power dynamic comparator for SAR ADC. Therefore, to design an ultra- low power dynamic comparator with good resolution, low power, better noise immunity and reduced delay following objective is framed:

Comprehensive analysis of existing comparators to design a novel dynamic comparator with reduced leakage power and enhanced noise immunity.

The methodology used to achieve desired objective involved following steps: -

- Design of major existing dynamic comparators in CADENCE virtuoso and simulation analysis of parameters like power, delay, and offset voltage of existing comparators.
- Design of novel dynamic comparator incorporating power reduction logic at good resolution.

- Simulation of designed dynamic comparator in CADENCE Virtuoso 45 nm.
- Parametric analysis of designed comparator in terms of power dissipation, sensitivity, delay and operating frequency.
- Comparative study with existing dynamic comparators for validation of the designed comparator.

This chapter includes the design and parametric simulation analysis of different low power dynamic comparators in CADENCE Virtuoso 45 nm technology node. Strong Arm latch dynamic comparator is considered as the baseline comparator that does not avoid the direct path connection between V_{DD} and ground due to that the circuit possess 51.38 nW of average transient power consumption. Further, Double Tail Dynamic comparator and Modified Double Tail Dynamic comparator are also considered for simulation & analysis and the transient analysis of both comparators is included. Following this, first proposed dynamic comparator architecture design along with the simulation parametric analysis is focussed.

Rigorous analysis in terms of power, delay, monte carlo simulation at different corners like ss, sf, ff etc. and temperature analysis from -40 degree centigrade to 110 degrees centigrade is carried out to validate the utilization of designed comparator in analog to digital converter. Proposed comparator outperforms the state of art dynamic comparators in terms of power, delay and PDP which is included as comparative analysis of proposed with other existing dynamic comparators. Finally, second proposed dynamic comparator for high frequency applications based on charge shared logic is carried out and its detailed analysis is also included.

The present chapter is divided into 6 sections, starting with an introduction of chapter as first section 3.1, an overview of dynamic comparators for ADCs is focussed in section 3.2, section 3.3 considers the design, simulation and parametric analysis of major existing dynamic comparators. Section 3.4 includes design and analysis of first proposed dynamic comparator. Subsection 3.4.1 focusses on the transient parametric analysis of first proposed dynamic comparator and subsection 3.4.2 includes the monte-carlo, corner & temperature analysis of first proposed dynamic comparator. Further, section 3.5 consists of the design, simulation and analysis of the second proposed comparator based on charge sharing logic for fast regeneration, low power and reduced kickback noise. Finally, all the important outcomes are summarized in section 3.6.

3.2 OVERVIEW OF DYNAMIC COMPARATORS FOR ANALOG TO DIGITAL CONVERTERS (ADCS)

Comparator design for ADCs is required at reduced consumption of static and transient power to make it employable for ultra-low power applications. Many researchers worked on the different architectural variations of dynamic comparators to achieve reduced power consumption along with better resolution and reduced delay at different technology nodes and sampling frequency. A SAR ADC is composed of several key building blocks, including an optimized comparator, SAR control logic, and a DAC, which together generate a digital output corresponding to the applied analog input. Although power optimization of each individual module is critical, this chapter primarily concentrates on the design and performance analysis of low-power dynamic comparator architectures. Specifically, it examines the basic Strong-Arm latched comparator [37], the Double-Tail dynamic comparator [38], and the Modified Double-Tail dynamic comparator [42], in addition to two newly proposed comparator designs. Initially, advanced state-of-the-art dynamic comparators [40–54] are reviewed and evaluated in terms of architecture, delay, power consumption, resolution, and offset voltage. Based on their comprehensive simulation and analysis, two novel dynamic comparator designs are subsequently proposed with further improved performance.

Furthermore, it is good to mention that dynamic comparators have been the focus of extensive research due to their critical role in high-speed and low-power analog-to-digital converters (ADCs). Several approaches have been proposed to enhance their performance. As per the literature, in [57], the authors introduced a dynamic comparator with an offset-cancelling circuit capable of detecting minute voltage fluctuations, though at the cost of relatively high-power consumption. Kick-back noise, a well-known source of nonlinearity resulting from distortion, has been widely studied [59-60], along with detailed analyses of common-mode variation effects [71]. To mitigate noise and offset voltage issues, researchers have explored the influence of differential voltage gain and the g_m/I_D ratio of input pre-amplifier transistors to improve common-mode variation tolerance in dynamic comparators. Comprehensive evaluation of different dynamic latch comparator configurations is conducted, comparing key performance parameters such as power consumption, kick-back noise, input-referred offset voltage, and speed [87]. When power consumption and delay are prioritized, the double-tail dynamic latched comparator has been shown to achieve superior energy efficiency and lower delay compared to conventional Strong Arm latch design [38, 42]. Further advancements, including charge-sharing techniques to preserve node voltages and reduce delay time, have been presented in

[123]. Additionally, studies have analyzed the common-mode component of kick-back noise in transconductance-enhanced latch and Strong-Arm latch comparators. Innovative methodologies such as dynamic floating inverter amplifiers have been proposed for improved comparator design [104], while various dynamic comparison techniques for ultra-low-power applications have been reported in [43]. Despite significant advancements, there remains a strong need to develop a dynamic comparator that offers enhanced transconductance gain in the pre-amplifier, while simultaneously minimizing switching and leakage power and ensuring proper isolation between the pre-amplifier and the regeneration latch. Furthermore, enabling all switching operations using a single clock (clk) signal instead of its inverted counterpart can contribute to additional power savings. Considering these design priorities, a new dynamic comparator architecture has been proposed to achieve ultra-low-power operation in SAR ADC applications.

3.3 WORKING AND PERFORMANCE OF EXISTING DYNAMIC COMPARATORS

The latched comparator is a core building block in nearly all ADC architectures. Its energy efficiency is strongly influenced by factors such as thermal noise, kickback noise, and offset voltage. In cardiac implantable medical device (IMD) ADCs, kickback noise introduced by the latched comparator can adversely affect resolution, accuracy, and settling behavior. Accordingly, this section focuses on the major dynamic comparator architectures reported in the literature, which serve as the foundation for the design of low-power SAR ADCs.

3.3.1 Strong-Arm Latched Comparator

In architecture design of basic latched comparator [37], a cross coupled CMOS is used to create pre-charge nodes; *outn* and *outp*, as depicted in Fig.2.3. Transistors: *M3* and *M4* switch to ‘ON’ state at a low clock signal and thus *outn* and *outp* attains the levels equal to V_{DD} . The pulsating clock signal (clk) establishes a timing reference in the circuit. The inputs are applied to the gate terminal of transistors *M7* and *M8*, whereas; *M1*, *M2*, *M5* and *M6* form a cross coupled CMOS structure. The transistor *M9* is utilized to create the path between given inputs and ground. On the contrary, *M3* and *M4* become ‘OFF’ while clock switches to a high logic. Now, if $INA > INB$, then the *outn* node will discharge at an elevated rate as compared to *outp*. Owing to this, the *outn* node turns *M2* in ‘ON’ condition and consequently, *M1* switches in ‘OFF’ condition.

Thus, the *outn* node attains a logic low state while *outp* node charges to V_{DD} level. This circuit is designed at 45 nm node to seek the possible application of ADC in MHz frequency range. Along with transient output response the static power analysis is carried out. The clock

parameters for analysis are taken as: 1.8 μ s and 900 ns for total time period and pulse width, respectively, however the rise and fall delay times are kept as 100 ns. The output transient response of basic latched comparator is illustrated in Fig. 3.1. The transient outputs at nodes; outn and outp are plotted relating to all possible combinations of input signals *INA/INN* and *INB/INP*. The discharging rate of initially pre-charged nodes; outn and outp is contingent to the sampled voltage amplitude level of inputs. On higher *INA* as compared to *INB*, the *outn* discharges at a faster rate than that of *outp* and for this input combination, the cross coupled CMOS latch pulls up the *outp* node again.

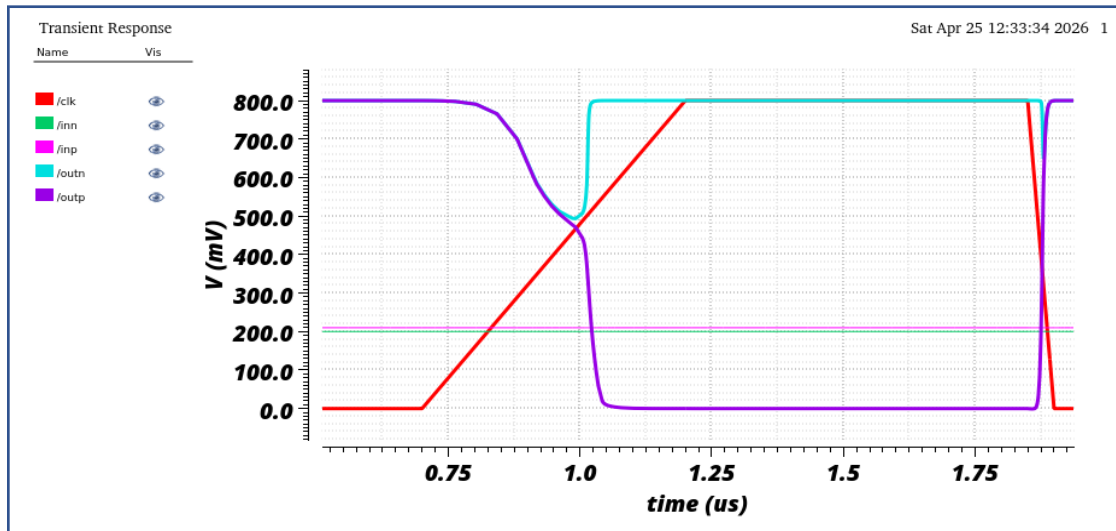


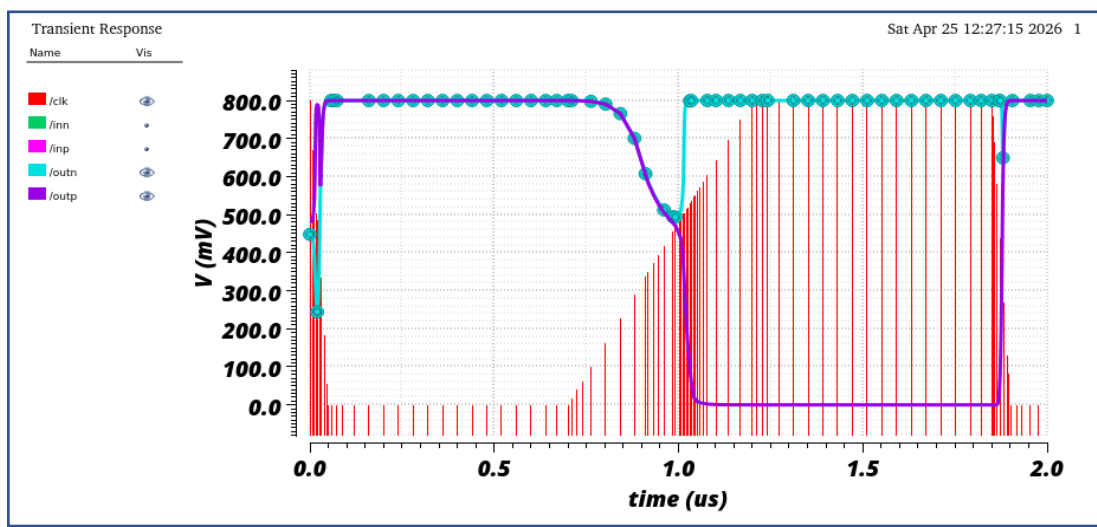
Fig. 3.1 Transient output of basic latched comparator

In basic comparator, the reduction of static power is not given much significance. The average transient power consumption is obtained as 51.38 nW. This comparator fails to eliminate a direct conduction path between V_{DD} and ground, resulting in a static power dissipation of approximately 51.38 nW under the specified operating conditions.

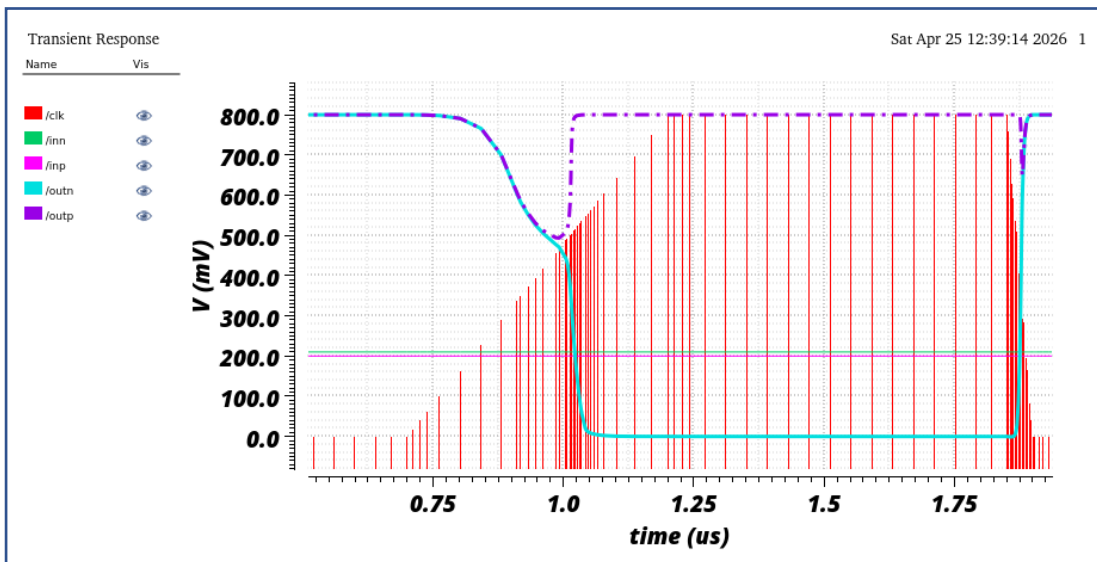
3.3.2 Double Tail Dynamic Comparator

The double tail dynamic comparator [38] employs two stacks of transistor modules, depicted as *M1-M2-M9-M10* and *M3-M4-M7-M8* in Fig. 2.4. In comparison to the basic comparator, this design utilizes two tail transistors as *Mtail1* and *Mtail2* to control the straight connection between V_{DD} and ground. This strategy reduces static power consumption by limiting the direct standby current. Latch regeneration capabilities for speed enhancement have not been inculcated in this architecture compared to controlled comparator which makes this design a bit slower than that of controlled comparator. Now, on logic low of *clk* signal the output node F_p and F_n precharges to V_{DD} which in turn pull down the *outn* and *outp* nodes to ground. As *clk*

switches to logic high state, tail transistors M_{tail1} and M_{tail2} switches to ON state and consequently nodes $outn$, $outp$ pre-charge to V_{DD} . further, this pre-charged status of $outn$ and $outp$ will be prohibited by the sampled voltage levels of inputs to be compared i.e., INN and INP . Output transient behavior of the design is analyzed for all possible input combinations which depicts that the switching of output node to logic high depends on the corresponding input sampled voltage level. The simulated transient behavior of the design for $INN > INP$ is depicted in Fig. 3.2 (a) which signifies that switching of output node to logic high would be having solely dependence on the amplitude of sampled signal values; higher of the sampled input results in pull up of corresponding output node.



(a)



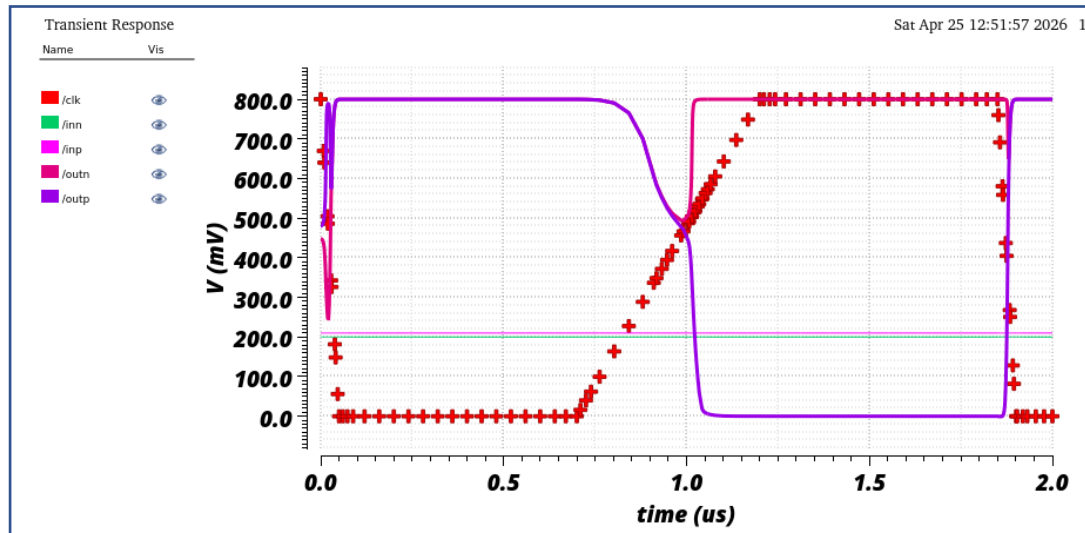
(b)

Fig. 3.2 Transient output plot of DTDC for **(a)** $INN > INP$ and **(b)** $INP > INN$

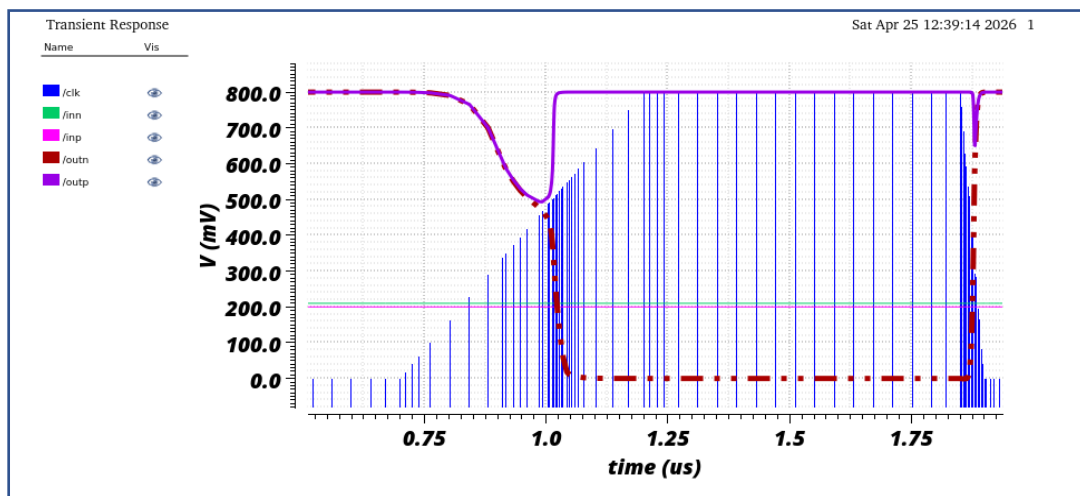
A minimum difference of 0.2 V between sampled voltages can be compared satisfactorily by the design. Transient response at output nodes *outn* and *outp* for $INP > INN$ is shown in Fig. 3.2 (b). It is also mentioned that *clk* signal is a continuous signal, only it's representation is taken as histogram for better representation of three signals in a simulated output graph.

3.3.3 Modified Double Tail Latched Comparator

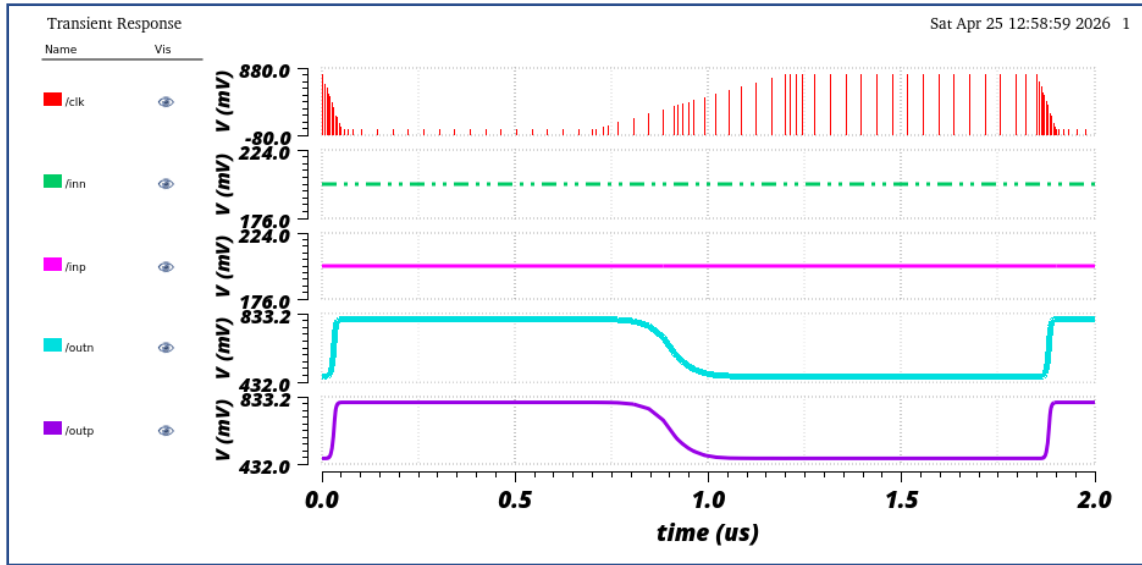
The Fig. 2.5 illustrates the Modified Dynamic Tail Latched comparator architecture [42], featuring latch regeneration capabilities facilitated by the feedback connection of transistors; *MP1* and *MP2*, placed in parallel to *M5* and *M6*. This design incorporates a cross-coupled CMOS latch formed by *M7*, *M8*, *M9*, and *M10* with *outn* and *outp* serving as output nodes. In comparison to a basic comparator, this design integrates two tail transistors, *Mtail1* and *Mtail2*, to enable static power reduction capabilities.



(a)



(b)



(c)

Fig. 3.3 Transient Plot of Modified Comparator (a) $INN > INP$, (b) $INP > INN$ and (c) $INN = INP$

low logic first and recharge outp again to logic high. Similarly, at input condition, $INN > INP$, the outn node is recharged to logic high, observing logic low at outp which is depicted in Fig. 3.3 (a). Output transient behaviour of controlled dynamic latched comparator for all possible input combinations is analyzed and resulting output response at outp and outn for $INP > INN$ is given in Fig. 3.3 (b). Further, on higher sampled voltage at INP as compared to INN , F_n switches to low state more speedily than that of F_p , which in turn switches $MT2$ to OFF state prior to $MT1$ and consequently outn will switch to Further, the output nodes; outn and outp, both will observe logic low level under the constraint of $INN = INP$, as shown in Fig. 3.3 (c). In this comparator, inclusion of $M3$ and $M4$ in series with $M1$ and $M2$ augments the switching speed and reduces the comparison time against the conventional design.

3.4 DESIGN AND ANALYSIS OF PROPOSED DYNAMIC COMPARATOR

Figure 3.4 depicts the design of the suggested comparator with the kickback noise reduction approach simulated for the frequency of 540 KS/s. The suggested dynamic comparator operates in two modes: comparison/evaluation mode and reset mode. Once the clock ($clk = '0'$) is zero during the reset or precharge phase, the kickback noise reduction approach reliant transistors $M7$ - $M8$, $M12$ are turned off to prevent the circuitry from using static power. During this process, the transistors $M3$, $M4$ are turned ON, resulting in a short circuit between V_{DD} and the comparator's output nodes. Consequently, V_{DD} is coupled to the Comparator outputs outp and outn. When the kickback noise reduction technique transistors $M7$ and $M8$ are switched off, the

comparator's output terminals are no longer connected to the comparator's inputs. The latch outputs have no effect on the transistors $M9$ and $M10$, which are linked to input signals. During the evaluation phase, the clock signal is set to V_{DD} ($\text{clk} = V_{DD}$), the tail transistor $M11$ and the $M3$, $M6$ PMOS transistors are turned off, and the Kickback noise mitigation method transistors are turned on. When the transistors $M7$ - $M8$ connected to the kickback noise reduction approach are turned on, the differential voltage created at the inputs is fed into cross-coupled inverter-based latches, which then make the needed choice.

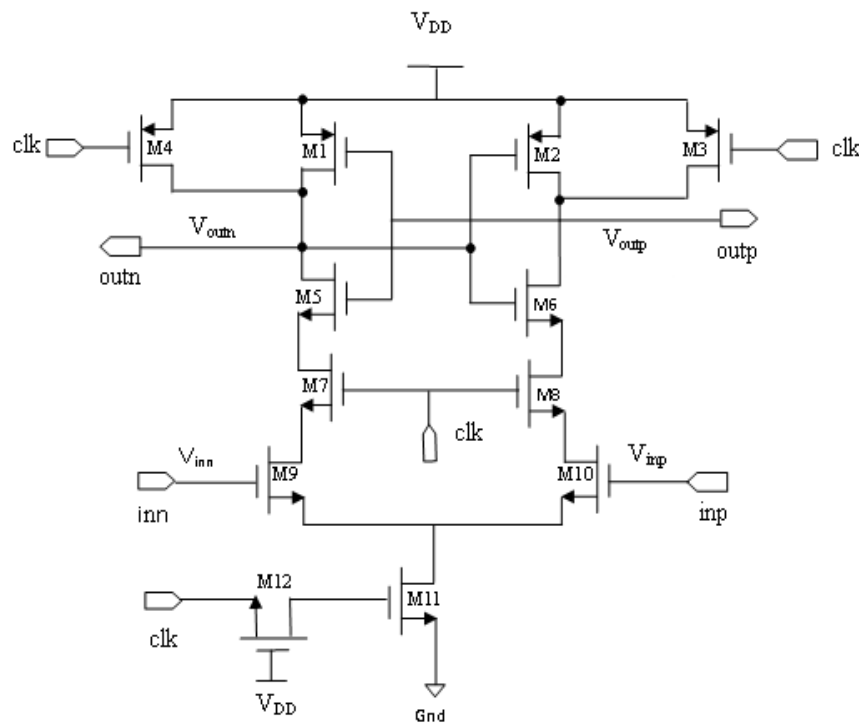


Fig. 3.4 Architecture of proposed dynamic comparator

Moreover, the comparator's output terminals outp, outn begin to discharge the voltage at varied rates dependent on the different input voltages provided to the transistors $M9$ - $M10$, as well as the tail transistor $M11$. If the input voltage fed to inn is greater than the input voltage fed to inp, the corresponding voltage in the output terminal outp falls quicker than the voltage in the output node outn, and vice versa. When compared to other terminals, the voltage of the output terminal outp approaches $|V_{DD} - V_{th}|$ relatively quickly. The regeneration of inverter latches ($M1$ - $M5$ & $M2$ - $M6$) activates the associated PMOS transistor $M1$. As a consequence, the output outn becomes V_{DD} . As a result of this PMOS transistor $M2$, the output outp equals 0.

The key advantage of the proposed comparator architecture is that it operates using a single regulating clock signal, thereby eliminating the need for synchronization among multiple

control signals and enhancing overall circuit efficiency. Moreover, the proposed circuits provide good delay and power reduction. The tail transistor is small in size to give the required lower tail current for the differential input transistor stage. Since extra transistors are not required for configuring or resetting the circuitry, the circuit's complexity is reduced, and comparator is giving correct output for even the difference of 2.5 mV between the two inputs to be compared.

3.4.1 Parametric Analysis of Proposed Dynamic Comparator

Transient output of proposed comparator for inputs to be compared as inn and inp is given in Fig. 3.5. Herein, $inn > inp$ with inn as 210 mV and inp as 200 mV. The result shows that inputs to be compared has difference of 10 mV in between and the comparator is comparing inn and inp as per the requirement. The red curve is the $outn$ voltage and green curve represents the $outp$. When clk is low, both $outn$ and $outp$ are at high logic state i.e 0.8 V which is the dc biasing voltage of the comparator. As soon as clk switches to high state and inputs are applied, the $outn$ and $outp$ terminal both starts discharging but with a different discharging rate and as soon as $outn$ falls to $V_{DD} - V_{thp}$, PMOS in the cross coupled latch in series with $outp$, gets switched ON and $outp$ node gets pulled back to V_{DD} and $outn$ node gets discharged to ground. The transient output for sawtooth input pulse as inp is given in Fig. 3.6. The output nodes $outn$ and $outp$ are showing transient behaviour as per the amplitude of inn and inp signals. The comparator is showing the resolution of 2.5 mV. Circuit is simulated with clk signal of period 1.2 μs . With $V_1 = 0$ mV and $V_2 = 800$ mV, V_{DD} is of 1.1 V and input signals as inn and inp to be compared are 200 mV and 210 mV. The output transient response for $inp > inn$ is shown in Fig. 3.6. With $V_1 = 0$ mV and $V_2 = 800$ mV, V_{DD} is of 1.1 V and input signals as inn and inp to be compared are 200 mV and 210 mV. The output transient response for $inp > inn$ is shown in Fig. 3.6. The differential output between $outn$ and $outp$ at the end of preamplification phase decides the latch delay of the comparator. This differential voltage is required to be at the higher end so that the regeneration latch delay time of comparator gets limited to certain reduced values of few nano seconds. The parametric sweep output for proposed comparator for varying V_{DD} is represented in Fig. 3.7.

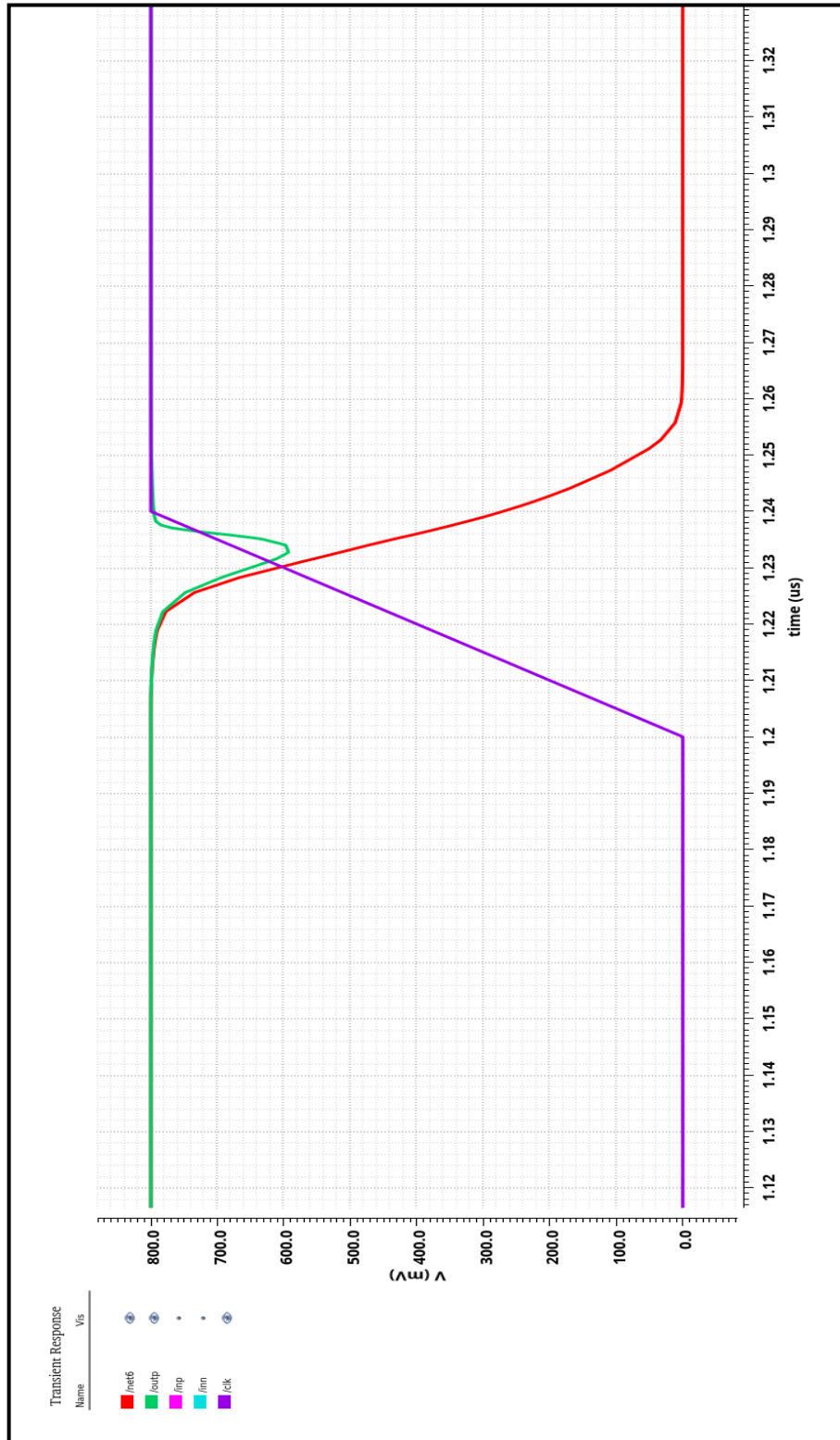


Fig. 3.5 Transient output of proposed comparator for $inn > inp$, $T_{clk} = 1.2 \mu s$, $inn = 210 mV$, $inp = 200 mV$

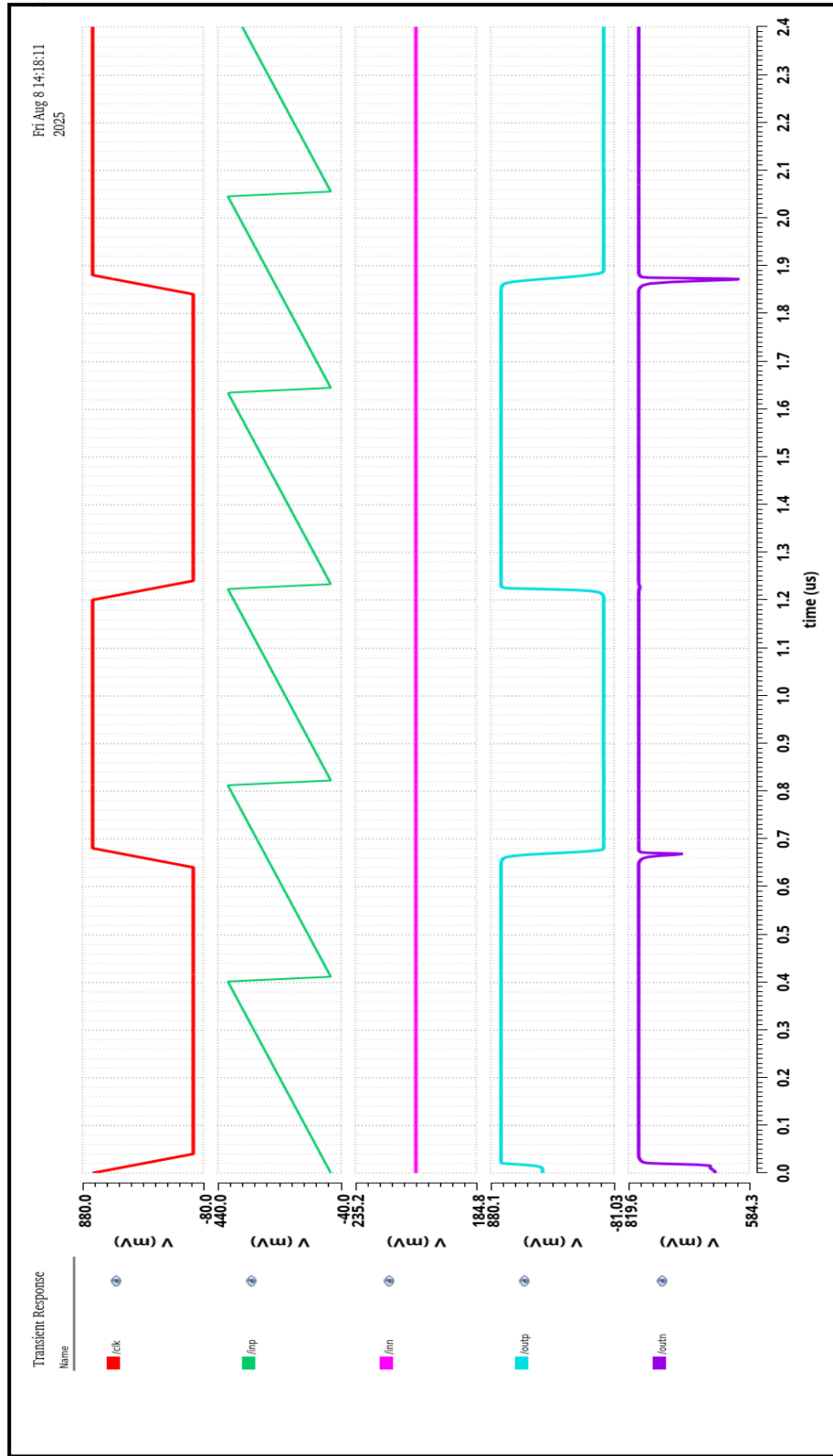


Fig. 3.6 Transient output of proposed comparator for sawtooth input with $\text{inp} > \text{inn}$

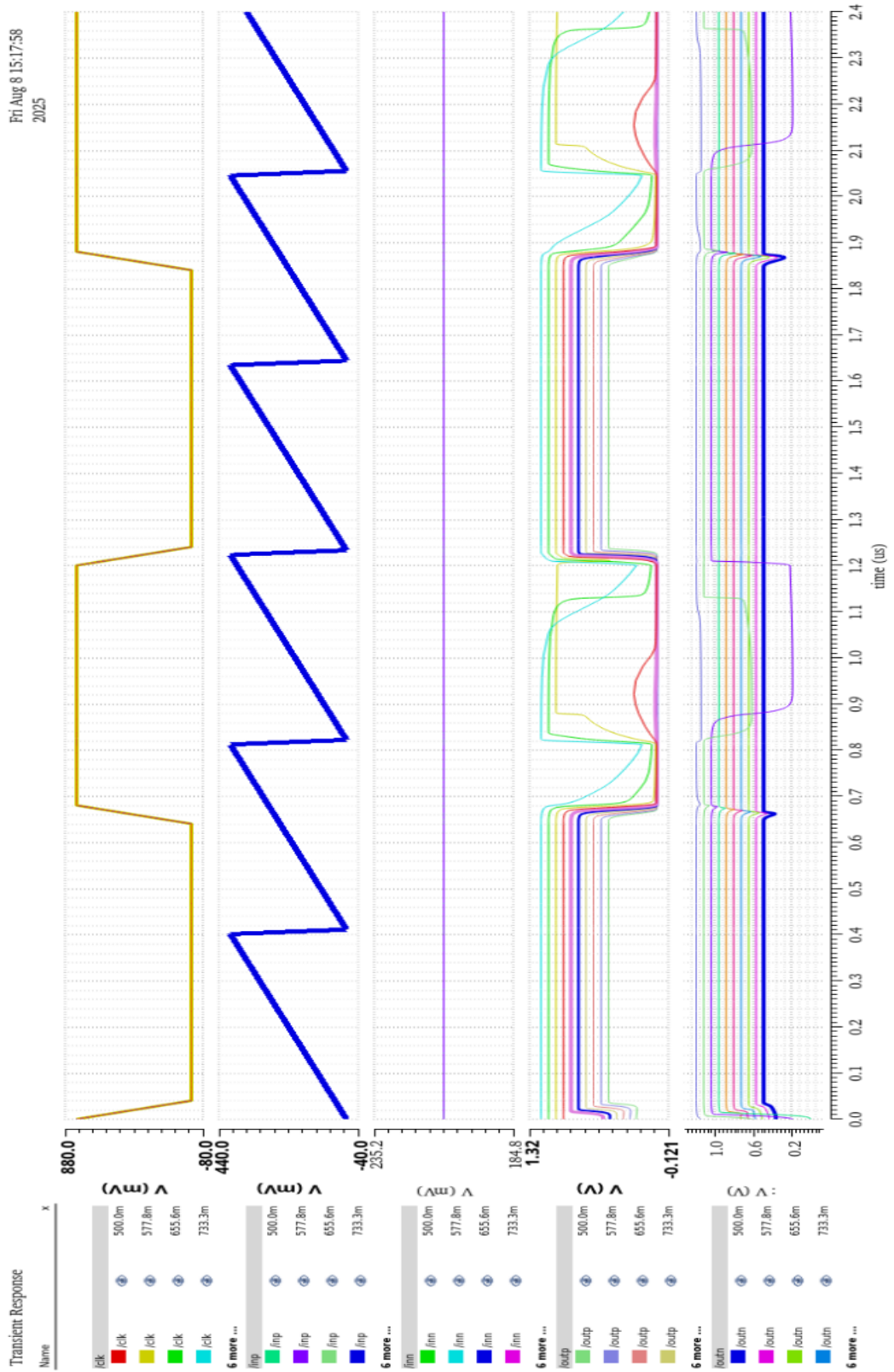


Fig. 3.7 Transient output of parametric sweep for proposed comparator with $inp > inn$

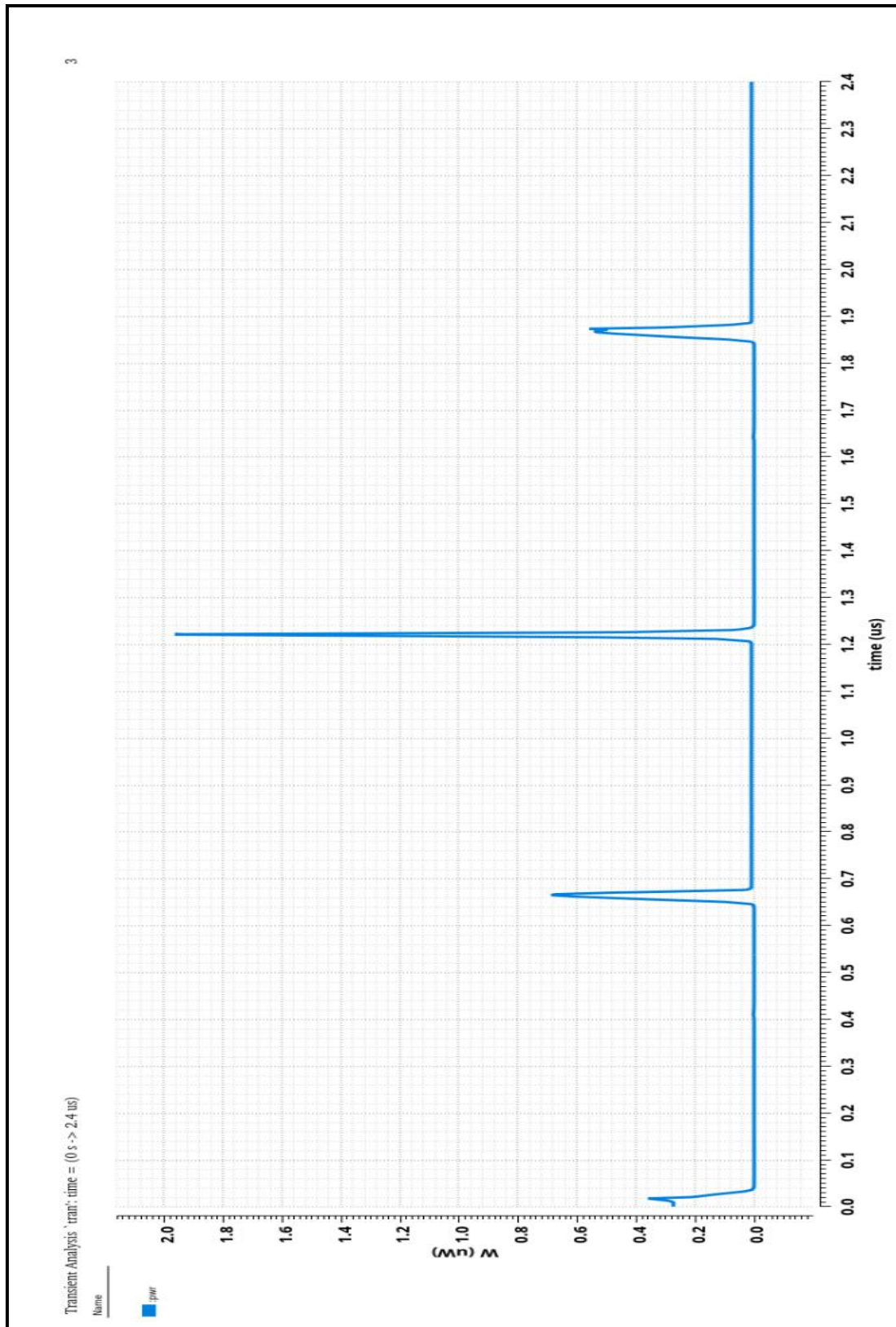


Fig. 3.8 Transient power plot of proposed comparator with average value 33.81 nW

Transient power is one of the major aspect in the design of a dynamic comparator. The switching of output nodes causes transients in the output which in turn led to transient power peaks consumption in the output. Proposed comparator is showing the average transient power of 33.81 nW which is much reduced value compared to the other architectures considered from the literature as shown in Fig. 3.8.

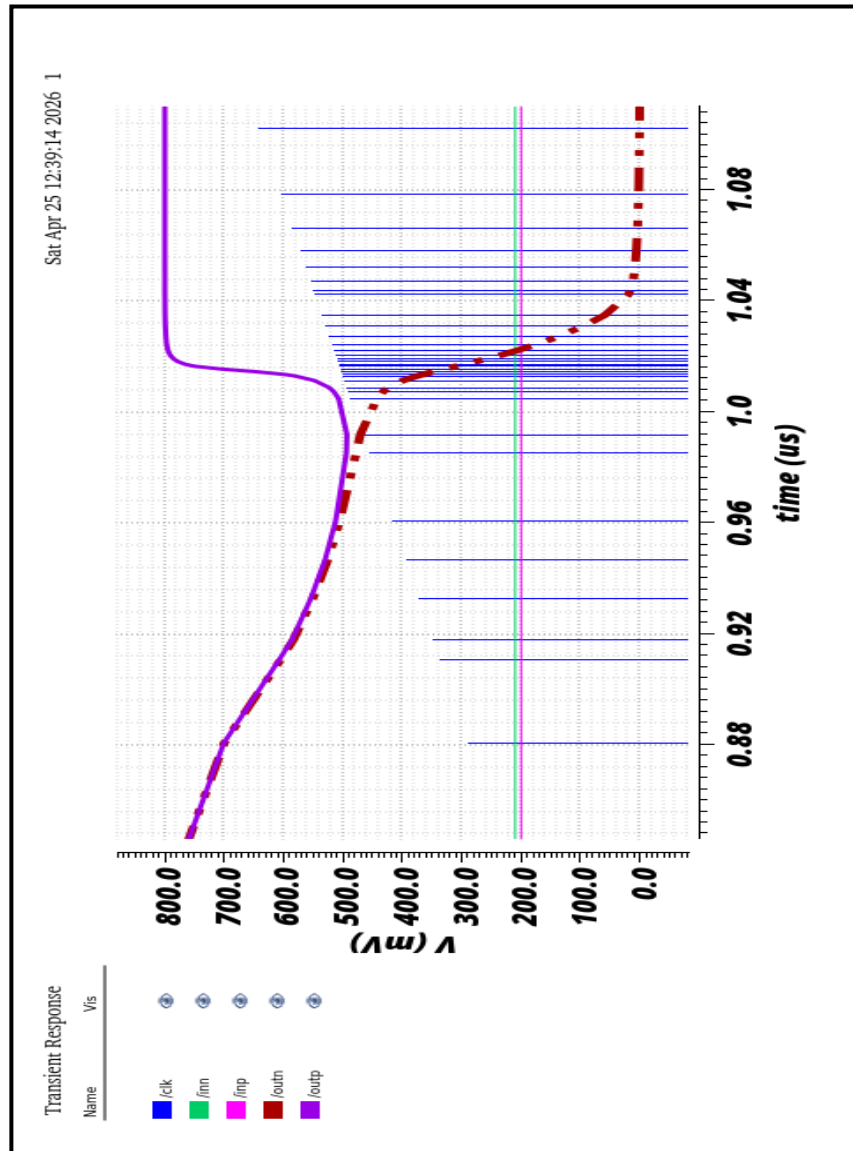
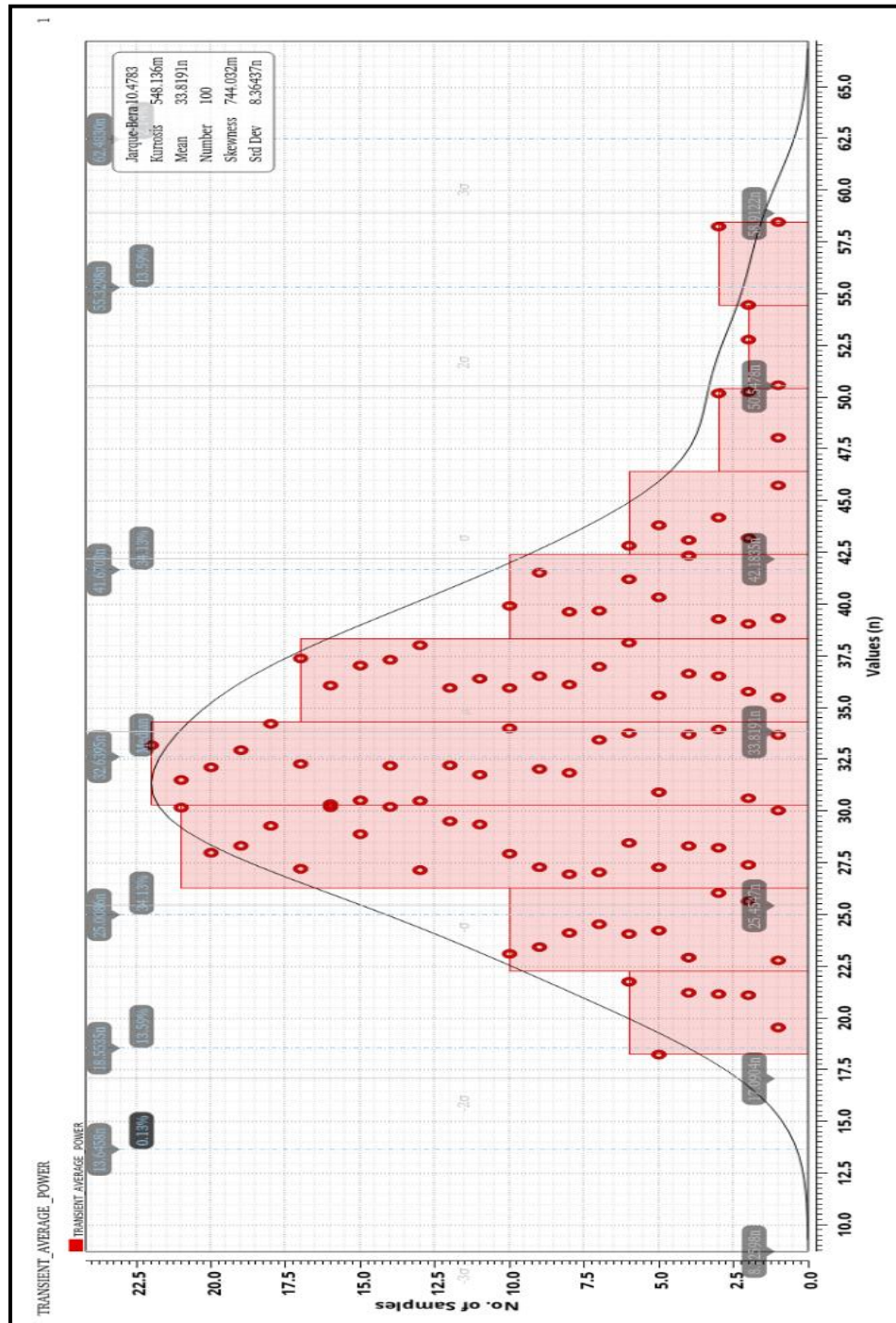


Fig. 3.9 ΔV_{out} (outn – outp) analysis for delay simulation of proposed comparator

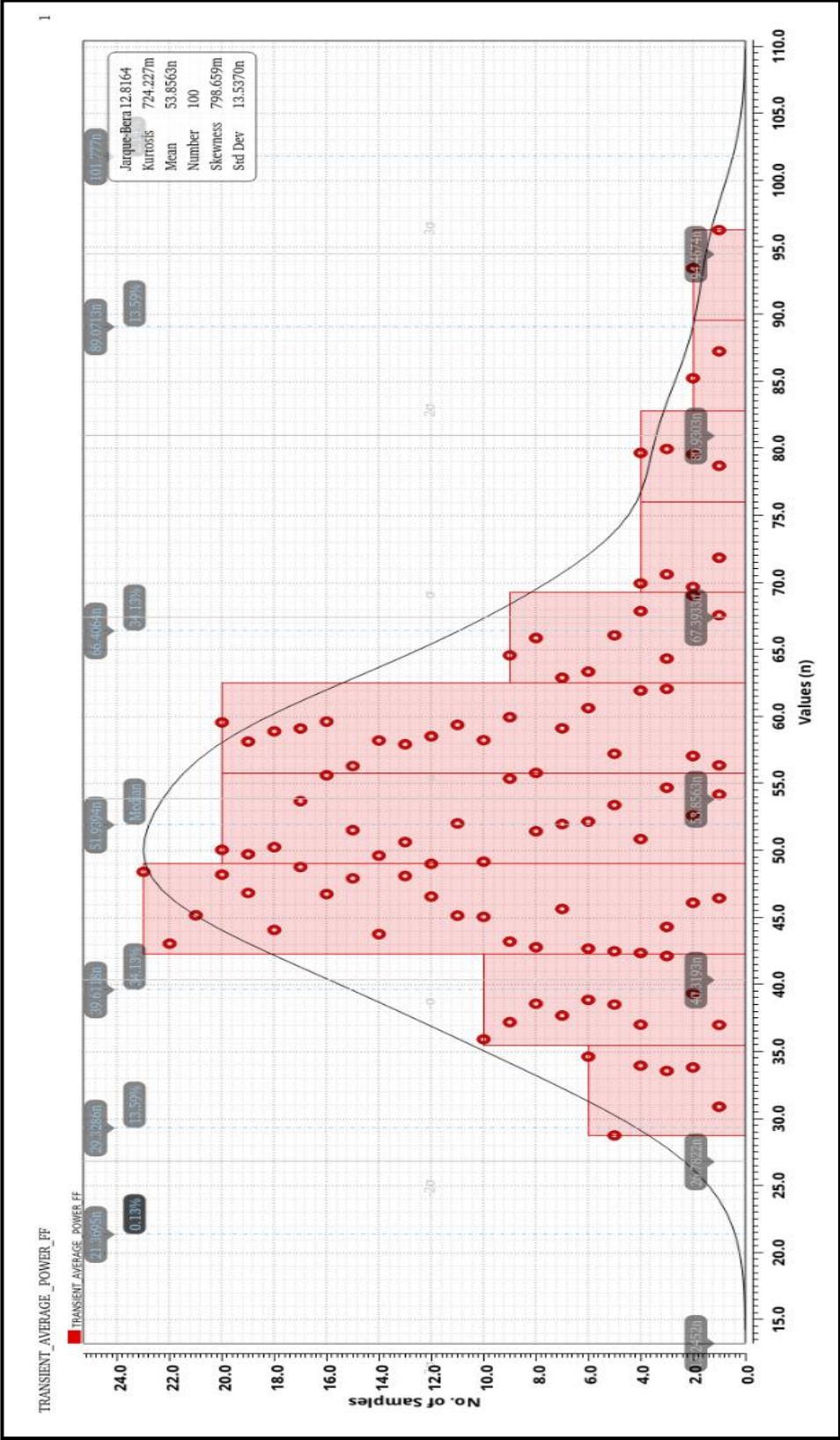
Delay of the proposed comparator is calculated to be below 40 ns for supply voltage 1.1 V. Delay of the comparator depends on ΔV_{out} which is around 55 mV between outn and outp at time t_1 at which one of the PMOS in the latch gets switched ON as shown in Fig. 3.9.

3.4.2 Monte Carlo and Corner Analysis of Proposed Dynamic Comparator

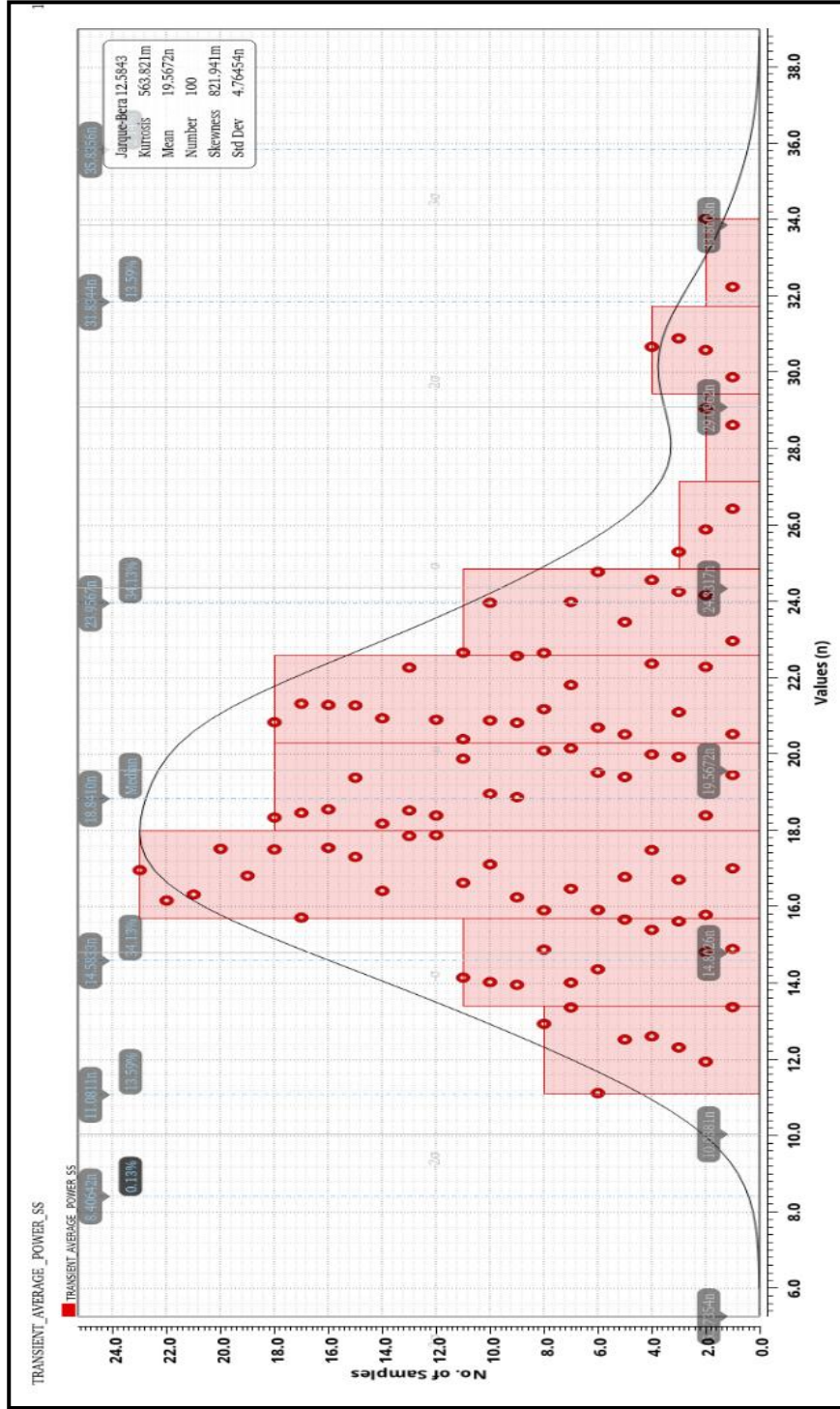
Monte Carlo simulations of the transient power for the designed comparator verifies that average mean power of 33.81 nW is consumed by the comparator in NN process corner whereas this power consumption is limited to 19.56 nW at SS corner and 53.85 nW for FF corner as shown in Fig. 3.10 (a) - (c).



(a)



(b)

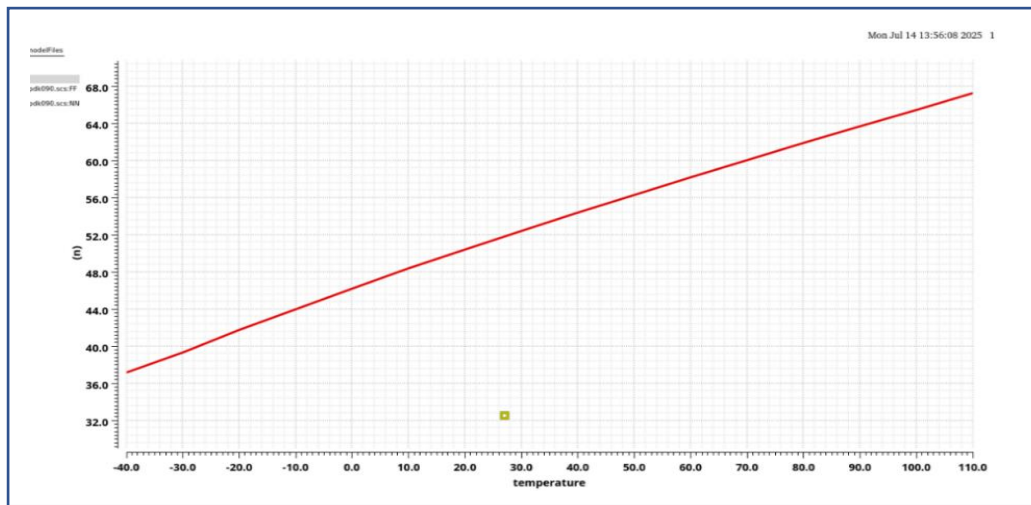


(c)

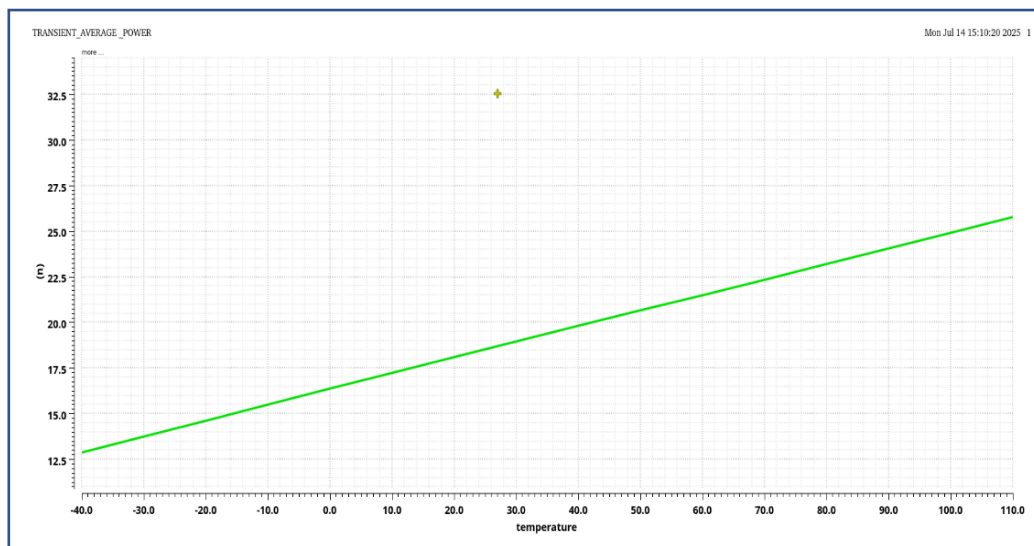
Fig. 3.10 Montecarlo analysis of proposed comparator at different corners **(a)** NN, **(b)** FF and **(c)** SS

Transient power in the designed comparator is limited to this reduced value as the architecture creates an isolation between pre-amplifier and latch module when clk is low due to which leakage power is avoided. Also, the W/L of tail transistors is optimized so as to optimize the comparator output. Fig. 3.10 (c) shows the montecarlo simulation of transient power in SS

corner is restricting to the mean average of 19.56 nW. The avoidance of inverted clk signal in the comparator circuit along with disconnection of preamplifier and latch subsections has



(a)



(b)

Fig. 3.11 Transient power plot vs temperature at (a) NN and (b) SS corner for designed comparator restricted the power consumption to this reduced value. The output transient power of the designed comparator shows that the peak of transient power is moving around 780 nW but the average transient power of the circuit is 33.81 nW. The preamplifier and latch modules disconnection with the help of controlling transistors has limited the switching of intermediate nodes due to which the average transient power has been reduced to the value of 33.81 nW.

Table 3.1: Performance comparison of existing dynamic comparators with proposed comparator

S.No.	Parameter	Proposed Dynamic Comparator	[47]	[46]	[50]	[51]
1	Operating Voltage (V)	0.8	0.8	1	1.8	1 & 0.5
2	Clock Frequency (MHz)	0.54	250	1000	333	50
3	Technology (nm)	45	45	90	180	65
4	Power Consumption (nW)	33.81	1728	32,620	41,000	3550
5	PDP (fJ)	0.4	0.56	1.69	10.04	1.2

The design shows stable behaviour for the temperature variation of -40°C to 110°C . Proposed designed is simulated with temperature variation from -40°C to 110°C at nn and ss corner as shown in Fig. 3.11 to validates the temperature sensitivity of the proposed design. Finally, the proposed comparator is simulated with capacitive loading of 5.1 pF which is the required values for using this module along with capacitive DACs. Table 3.1 gives the comparative study of our design with existing comparators in literature which signifies that inclusion of isolation between pre-amplifier & regeneration latch along with kickback noise reduction logic has resulted in the reduced power consumption value of 33.81 nW with PDP value of 0.4 fJ at clock frequency of 540 KS/s in the proposed comparator.

3.5 ARCHITECTURE AND WORKING OF THE PROPOSED CHARGE SHARING DYNAMIC COMPARATOR

First proposed dynamic comparator given in section 3.3 is showing power consumption of 33.81 nW with PDP value of 0.4 fJ at 540 KS/s incorporating isolation between pre-amplifier and regeneration latch in reset state. A second proposed dynamic comparator (Proposed charge sharing) with charge sharing logic for high frequency applications operating in the frequency range of GHz is further presented in this section. Dynamic latched comparators have shown superior performance compared to other comparator designs in terms of optimizing speed, power consumption, delay and input referred offset voltage [40-54]. Moreover, the proposed charge sharing logic-based circuit's architectural design shown in Fig. 3.12 offers enhanced

isolation between the input and output along with reduced undesirable noise. The feature makes it highly suitable for low-voltage applications within the realm of biomedical implants. The circuit incorporates the kickback noise reduction mechanism with the inclusion of two clocked transistors M8 and M9 to ground the input pair source transistors. The Proposed charge sharing comparator successfully resolves the issue of kickback noise by reducing the effect of switching of f_n and f_p node voltages on the input voltage. The comparator operates in two distinct phases: the reset mode and the comparison (evaluation) mode. During the reset phase, the circuit employs two dedicated reset mechanisms to ensure that the correct logical levels are established prior to the evaluation stage, thereby enabling accurate and reliable comparison results. Generally, the reset mechanism operates by either charging or discharging the output nodes to predefined voltage levels, i.e., V_{DD} or ground. In the case of the STDLC architecture, the output nodes are driven to V_{DD} during the reset phase. Conversely, in the DTDLC architecture, the output terminals are pulled down to ground. After the evaluation phase of the comparator, one output node settles at the ground reference level, while the complementary output rises to the supply voltage (V_{DD}), representing the decision made by the comparator.

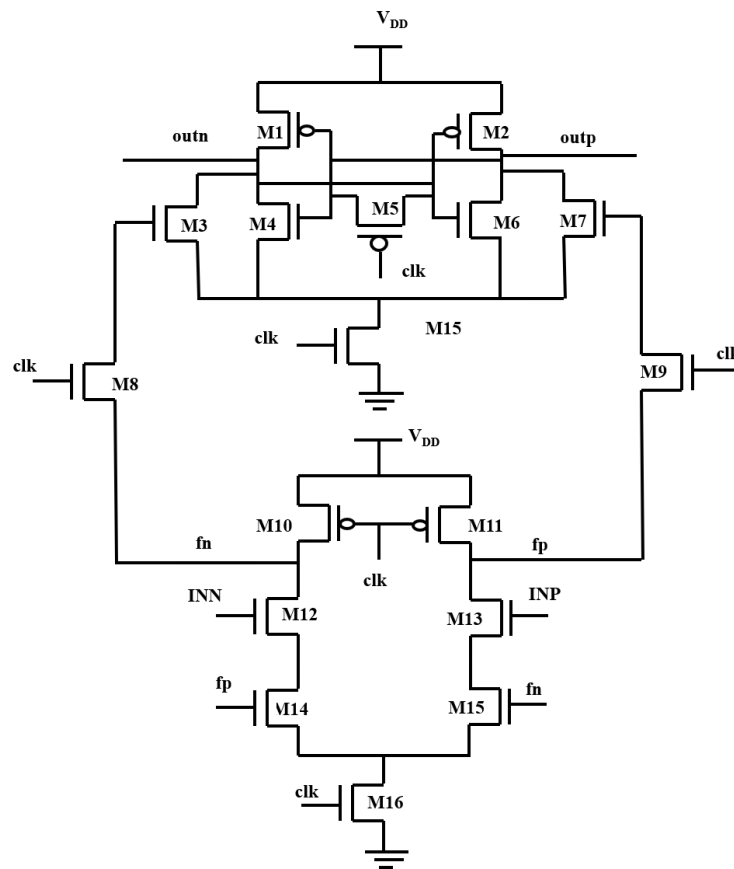


Fig. 3.12 Architecture of proposed charge sharing dynamic comparator

The Proposed charge sharing comparator core premise is the use of a unique resetting mechanism and kickback noise approach to preserve the charge and kickback noise respectively. This shared charging logic approach makes it easier to reduce latency, power consumption, and kickback noise. The charging-sharing approach employs a single-pass transistor strategically positioned between two output nodes. During the reset phase, the pass transistor guarantees that charge is distributed uniformly across two output nodes. The voltage at the output nodes will stay over the chosen threshold value due to the collective charging of the load capacitances. As a result, the input signal may be evaluated more efficiently during the regeneration phase which speeds up the process. The implementation results show a significant improvement in power and latency as a consequence of using this approach.

The use of sample switches is a very effective approach for reducing kickback noise and improving comparator operating performance. The clk signal is linked to ground during the reset or recharge phase due to which tail transistors $M15$ and $M16$ are disabled, reducing static power consumption. During this phase, transistors $M10$ and $M11$ boost the voltage levels of nodes fn and fp to the V_{DD} potential. As a result, it starts the activation of transistors $M3$ and $M7$. During the reset phase, the shared transistor $M5$ is used to link the outputs $outp$ and $outn$, allowing it to serve as a shared charging logic transistor. After the previous comparison step, charge is shared between the two nodes because one node is at V_{DD} while the other is at ground. At this time, the transistors $M8$ and $M9$ used for kickback noise reduction are switched off. As a result, the input side of the comparator is separated from the output nodes, helping to avoid any unwanted charge from feeding back to the input. The latch outputs had no effect on the transistors $M12$ and $M13$, which were coupled to the input signals. Once the clk signal attains the V_{DD} supply voltage threshold, the circuit undergoes a transition into the evaluation phase. This transition triggers the activation of transistors $M8$ and $M9$, which are integral components of the Kickback noise mitigation system. The activation of transistors $M8$ - $M9$ contributes to the mitigation of kickback noise. The differential voltage generated at the inputs is subsequently routed to cross-coupled latches based on inverters, which facilitate the required decision-making process.

During this phase, transistors $M14$ and $M15$ are in an active state, whereas reset transistors $M10$ and $M11$ are in a deactivated state. Assume that $V_{inn} > V_{inp}$, then the potential of fp lowers at a higher rate than fn . The results of the implementation demonstrate a notable enhancement in power and latency as a result of employing this technique. Using sample switches is an effective way to reduce kickback noise and improve the comparator's performance. During the

reset or recharge phase, the clock signal (clk) is pulled to ground, which turns off the tail transistors $M14$ and $M15$ and helps save static power. In this phase, the voltages at nodes f_n and f_p are boosted to V_{DD} through transistors $M10$ and $M11$, which then activate transistors $M3$ – $M7$. Also, during reset, the shared transistor CSL connects the outputs outp and outn, allowing it to work as a shared charging logic element.

The distribution of charge occurs between two nodes when one node is at a voltage of V_{DD} and the other node is at the ground potential, subsequent to the preceding evaluation stage. The nature of this occurrence would be altered if we were to take into account the inverse state of the input voltage. The sole distinction in functioning within this design lies in the fact that, during the assessment phase, the decision does not stem from two voltage levels situated at opposite extremes. In contrast, it can be observed that the voltage level at both output terminals is approximately half of the level of the source voltage. When the output terminal is initially set to a voltage equal to half of the supply voltage, the evaluation time is reduced, and power consumption is decreased. The delay analysis provides empirical evidence that aligns with this theoretical concept.

The main benefit of the proposed comparator design is in its only reliance on a single regulating clock signal. The efficiency of the circuit is boosted by removing the need for synchronization among many control signals. The circuit under consideration additionally provides reduced latency and power optimization. The tail transistors possess dimensions that are sufficiently small to provide the diminished tail current required for the differential input transistor stage. The circuit complexity has been reduced due to the absence of any requirement for additional transistors to configure or reset the device. In the process of regeneration, it is imperative to ensure the isolation of the drain terminals of the transistors comprising the input differential pair from the regeneration nodes.

Table 3.2: Transistor sizes for the proposed charge sharing comparator

S.No.	Name of the Transistor	W/L ratio
1	M3-M4-M5-M6-M7-M12-M13	2/1
2	M1- M2-M10- M11	4/1
3	M14- M15	4/1
4	M8-M9	4/1

This approach is applied to mitigate the incidence of kickback noise that arises from transients at the regeneration nodes. To execute this procedure, the regeneration node is linked to the drains of the input differential pair through the utilization of switching transistors M8 and M9. Switches that are intended to operate in a condition of strong inversion have been developed with enlarged dimensions in order to achieve a higher transconductance, thereby mitigating the impact of thermal noise. Therefore, in the process of regeneration, the isolation of the regeneration node and the drains of the input differential pair is achieved by employing *M8-M9*. In order to mitigate the effects of mismatch and manufacturing uncertainty, the design process incorporates customized transistor sizing and matching methodologies aimed at reducing offset voltage as shown in Table 3.2.

3.5.1 Kickback Noise Analysis in Proposed Charge Sharing Dynamic Comparator

The input voltage in CMOS latched comparators can be adversely affected by the output voltage variation connected to the input transistors. The reduction of kickback noise is necessary to achieve a higher level of precision. The input of the comparator is represented by a thevenin equivalent circuit, whereby the resistor value is 8 k Ω . The comparator under consideration exhibits significant kickback noise due to its resemblance to the single-tail comparator's construction. Furthermore, as stated in the study conducted by reference [47], the increased speed of output settling in dynamic comparators results in a more significant disruption at the input nodes. As a result, kickback noise in high-speed comparators is unavoidable. Specific noise reduction approaches, such as neutralization, as proposed in reference [82, 133] have the potential to mitigate the impact of kickback noise significantly. Typically, the reference nodes exhibit low impedance characteristics, resulting in fewer voltage disturbances on the reference voltages than the inputs.

Furthermore, the primary disruption occurs during the initiation of the amplification stage, allowing the reference voltages sufficient time to stabilize at their standard level before the commencement of the comparison stage [13, 134]. The proposed comparator demonstrated a reduced level of kickback noise mainly due to the utilization of auxiliary clocked transistors *M8* and *M9*. Utilizing these transistors served the purpose of isolating the output nodes, thus reducing the mismatch effects which also influence alongside the transistor's parasitic capacitance in the circuit design stage. Further, offset reduction in the feedback loop is achieved through appropriate transistor sizing that operates in the weak inversion region and works for the optimization of mismatch. Further, common mode component of kickback noise occurs

when switching of clock signal (clk) affects the input signal due to coupling with parasitic capacitances.

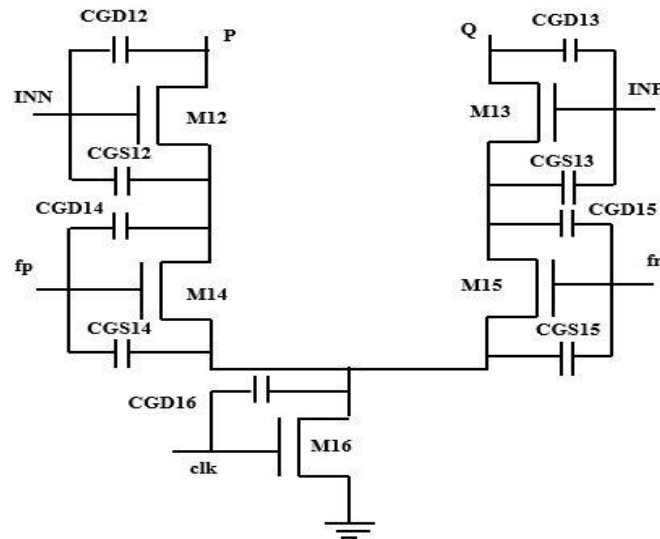


Fig. 3.13 Kickback noise paths in proposed charge sharing comparator

From [39, 47, 71] It is confirmed that to reduce the common mode component of kickback noise, slew rate of source and drain terminal voltages of input transistor pair is required to be reduced. For this inclusion, we may reduce the slew rate of clk signal which in turn reduce the slew rate of source and drain terminal of input transistor pair. This can be done by incorporating a R-C circuit just after the generation of clock signal to increase its rise and fall time which in turn reduces the slew rate of node voltages fn and fp which decreases the kickback noise current to reduce the kickback noise current. Also, resistance can be created by using bypass transistor. It is also worth mentioned that this technique will result in increase in offset voltage of the proposed design. The initial phenomenon often occurs when fn (labelled as P) and fp (labelled as Q) in Fig. 3.13 reduced towards the ground potential at different rates due to different INN and INP . This switching of voltages at P and Q node affects the input voltages INN and INP due to the coupling of these nodes with the inputs through parasitic capacitances $CGD12$ and $CGD13$.

The significance of this effect increases when $M12$ and $M13$ enter the triode region, leading to an increase in their gate-drain capacitances and causes differential kickback noise but due to inclusion of $M8$ and $M9$, direct connection between the transiting nodes $fn(P)$ and $fp(Q)$ with the input is avoided which results in reduced kickback noise current. Furthermore, the common-mode kickback noise currents are significantly stronger and predominantly occur during the low-to-high transition of the clock signal, which coincides with the turn-on of transistor $M14$,

as illustrated in Fig. 3.13. Specifically, at the onset of the evaluation phase, M14 draws drain current from the gate-to-source capacitances of transistors M12 and M13 (CGS12 and CGS13). In addition, when the clock signal subsequently transitions to the low state, the change in clk level is sent by CGD7 to both CGS12 and CGS13 and results in change in input voltage and this is avoided by increasing rise and fall time of clock signal which in turn reduces the slew rate of node $fn(P)$ and $fp(Q)$. Pass-transistors are utilized to increase the rise and fall time of clk signal. However, this will increase mismatch in the proposed design and will lead to increase in the input referred offset voltage.

3.5.2 Statistical Analysis of Noise and Input Referred Offset Voltage in Proposed Charge Sharing Comparator

keeping consideration, the effect of variation of input common mode voltage on noise, proposed circuit is less sensitive to V_{cm} variations as gm/I_D of input transistors M12 and M13 is increased with the biasing of transistors in weak inversion region. An input referred comparator noise generated due to threshold voltage ($V_{thn12,13}$) mismatch of transistors M12 and M13 is inversely proportional to the gm/I_D of these transistors as given by the eq. (3.1) [104]:

$$\sigma_{n,int}^2 \approx \frac{I_D}{g_m} \cdot \frac{4kT\gamma}{V_{THN}C_X} \quad (3.1)$$

From equation (3.1) it is verified that the noise is inversely proportional to the gm/I_D of input transistors and with proper biasing of input transistors in weak inversion region, this ratio is increased to limit the effect of noise. Also, it is worth mentioned that in conventional strong-ARM latch-based comparators, the gm/I_D ratio of around 20/V remains constant but in the proposed comparator due to tail capacitor C_{tail} potential of source voltage V_s is increased which in turn reduces the overdrive voltage and increased value of gm/I_D is obtained. Further, pre-amplification gain G affects the input referred offset voltage of the comparator. Gain (G) defines the differential voltage gain of comparator when the pre-amplification phase ends. Input referred voltage in preamplification phase can be modelled as $\sigma_{os,preamp}$ which is mainly due to threshold mismatch $V_{Th12,13}$ of input transistors M12 and M13 and $\sigma_{os,latch}$ is the input referred offset due to latch regeneration phase caused by the $V_{Th1,2}$ mismatch of M1 and M2. Now, noise due to total input referred offset [71] is given by σ_{os} given by eq. (3.2)

$$\sigma_{os} = \sqrt{\sigma_{os,preamp}^2 + \frac{\sigma_{os,latch}^2}{G^2}} \quad (3.2)$$

Equation (3.2) shows that increased value of pre-amplification gain G attenuates the offset voltage due to latch regeneration phase to a greater extent which in turn reduces the dependence

of proposed comparator on common mode voltage variation. Also, from [71] root mean square value of comparator noise (σ_n) is given by eq. (3.3) as:

$$\sigma_n = \sqrt{\sigma_{n,preamp}^2 + \frac{\sigma_{n,latch}^2}{G^2}} \quad (3.3)$$

Keeping in view these considerations, pre-amplification gain G which is the differential voltage gain at end of pre-amplification phase which affects the comparator offset and noise is optimized for the improved performance of proposed comparator in biomedical scenarios. Gain (G) is given by eq. (3.4) as:

$$G \approx \frac{\Delta V_{out}}{\Delta V_{in}} \quad (3.4)$$

At the end of pre-amplification phase maximum charge variation occurs at outp and outn node is shown by eq. (3.5) as given by:

$$G \approx \frac{\frac{\Delta Q}{C_O}}{\Delta V_{in}} \quad (3.5)$$

$$G \approx \frac{g_m}{I_D} \left\{ V_{Tp1,2} + \frac{C_X}{C_O} (V_{Tp1,2} + V_{Tn4,6}) \right\} \quad (3.6)$$

Equation (3.6) depicts that Gain G also depends on the g_m/I_D which is a function of common mode voltage variation. Also, preamplification Gain G affects the offset voltage and noise in the comparator. Capacitor C_{tail} has given the increased value of differential gain by increasing the source potential of transistors $M12$ and $M13$ which in turn also improve the g_m/I_D of input transistors $M12$ and $M13$ in the proposed circuit. Transient analysis of proposed comparator is given in Fig. 3.14.

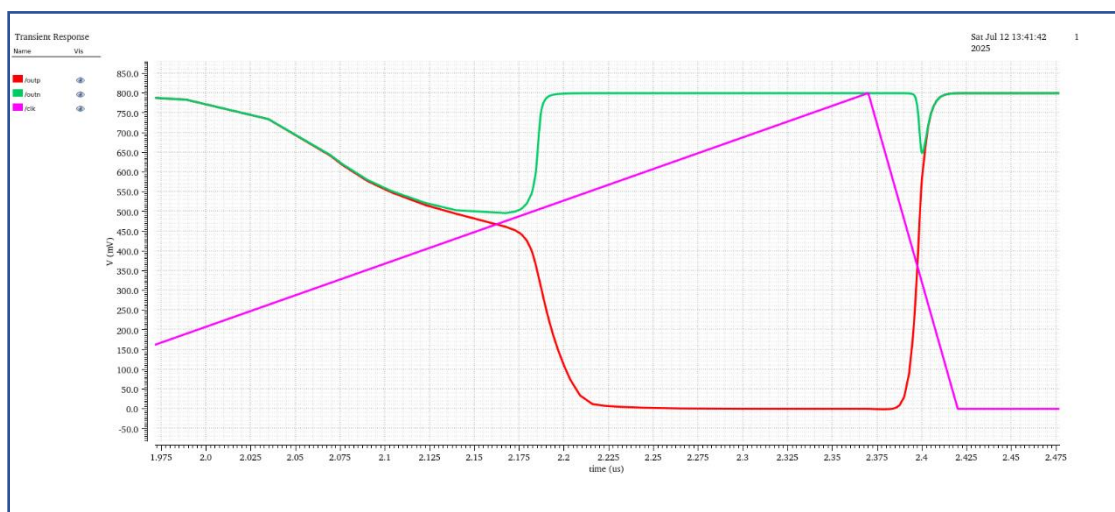


Fig. 3.14 Transient analysis simulation of proposed charge sharing comparator

Proposed comparator handles common mode voltage (V_{cm}) variations as gm/I_D of input transistors $M12$ and $M13$ is increased with the biasing of transistors in weak inversion region with the help of optimized voltage differential gain (G).

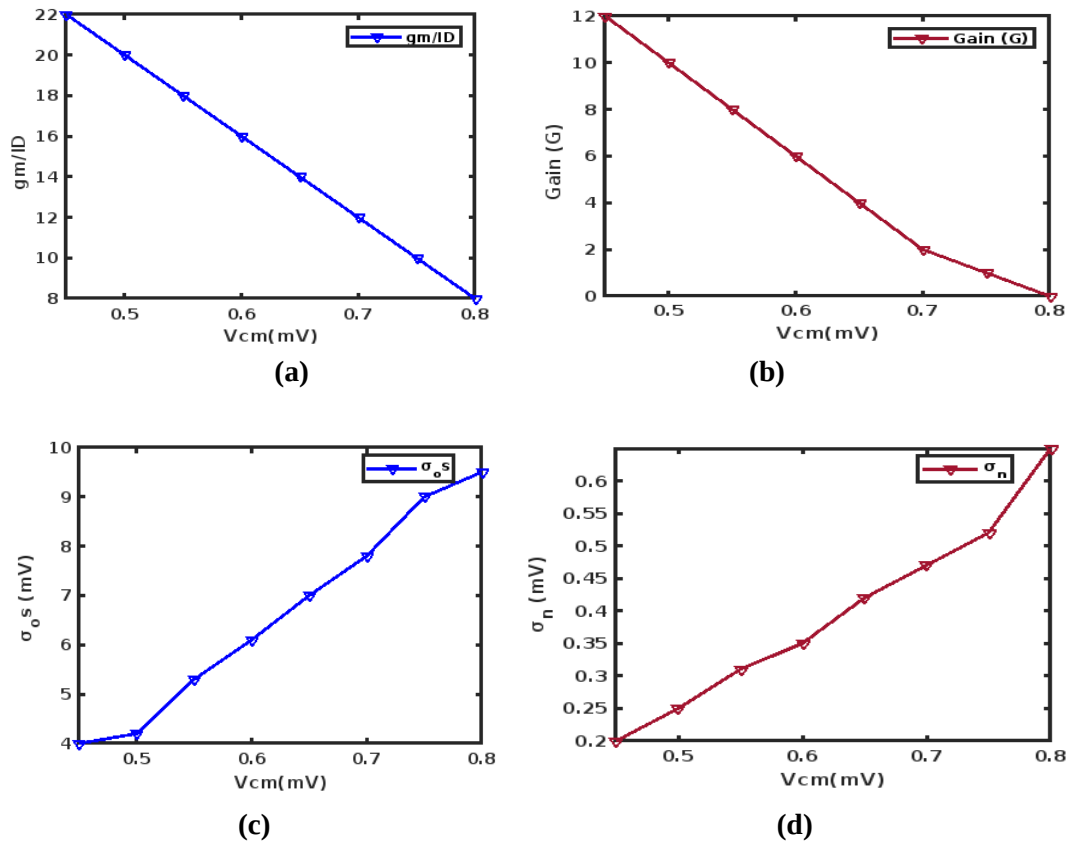


Fig. 3.15 (a) Gain (G) vs V_{cm} (b) gm/I_D vs V_{cm} (c) σ_{os} vs V_{cm} (d) σ_n vs V_{cm} of proposed comp.

With increased value of differential gain and gm/I_D , the input referred offset voltage gets reduced along with increase in the noise rejection capability of the proposed design as also verified by the equation. Fig. 3.15 shows the gain(G), gm/I_D , rms value of input referred offset voltage (σ_{os}) and rms value noise (σ_n) variations with respect to the common mode voltage.

3.5.3 Simulation and Parametric Analysis of Proposed Charge Sharing Comparator

Table 3.3 comprises of summary of the results obtained after simulation and parametric analysis of proposed charge sharing comparator with the considered specifications as $V_{cm} = 0.7$ V, $V_{diff} = 20$ mV, $clk = 1$ GHz, $V_{DD} = 1$ V. The proposed comparator is limiting the kickback noise to 0.47 mV and power dissipation as of 9.36 μ W at frequency of 1 GHz. The charge sharing approach and isolation of input and clock signals using additional transistors has resulted in the reduced kickback noise in the proposed comparator. In contrast, Table 3.4 presents a comparative evaluation of performance metrics for the proposed comparator architectures,

including delay, power consumption, and power–delay product (PDP), alongside existing comparator designs.

Table 3.3: Performance of proposed charge sharing comparator

S.No.	Parameter	Value
1	Supply voltage (V)	1
2	Technology(nm)	45
3	Operating frequency (GHz)	1
4	Power dissipation (μ W)	9.36
5	Offset voltage (mV)	7.8
6	Delay(ps)	48.2
7	Power delay product (PDP) (fJ)	0.451
8	Kickback Noise(mV)	0.47

Table 3.4: Comparison of proposed charge sharing with the existing comparators

S.No.	Properties	[42]	[46]	[135]	[136]	Proposed comparator
1	Technology (nm)	180	90	45	40	45
2	Power dissipation(μ W)	329	33.62	2.3	110	9.36
3	Delay (ps)	200	51.7	166.29	84	48.2
4	Kickback noise (mV)	43	NA	NA	NA	0.47
5	Offset voltage(mV)	7.8	7.7	3.15	8.9	7.8
6	Power Delay Product (PDP) (fJ)	0.653	1.62	0.382	1.147	0.451

The comparison is carried out in terms of power consumption, kickback noise, offset voltage, and PDP. It can be observed that the suggested comparator has a lower latency in comparison to the current systems. In the context of double tail topologies, it is observed that the impact of changes in the input common mode voltage on delay during the comparison phase is quite minimal compared to other topologies. To ensure stable operation, a wider input common-mode voltage range is selected for the comparator. The proposed design is evaluated through simulations across various common-mode and differential input conditions, using a supply voltage of 1 V and a clock frequency of 1 GHz. Although the power consumption is slightly higher than the comparator reported in [40], the proposed design achieves a significant power reduction of at least 66.98 % when compared with the work in [135]. The low-power

performance of the proposed approach is validated through analytical derivations, process–voltage–temperature (PVT) corner analysis, and post-layout simulations. Furthermore, Fig. 3.16 graphically depicts the relationship between comparator delay and input differential voltage for different common-mode voltage levels.

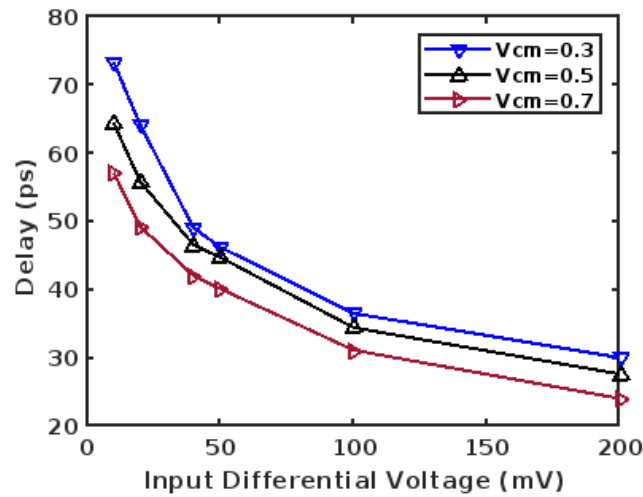


Fig. 3.16 Delay versus input differential voltage (V_{diff}) of the proposed charge sharing comparator at different V_{cm} values

At a specified V_{DD} of 1 V, the delay is found to be 48.2 ps when the differential input voltage level (V_{diff}) is maintained at 20 mV for a common mode voltage of 0.7 V. The observed delay exhibits a reduction from 56.3 ps to 23.17 ps as the input differential voltage (V_{diff}) ranges from 10 mV to 200 mV as depicted in Fig. 3.16 for varying common-mode voltage levels (V_{cm}).

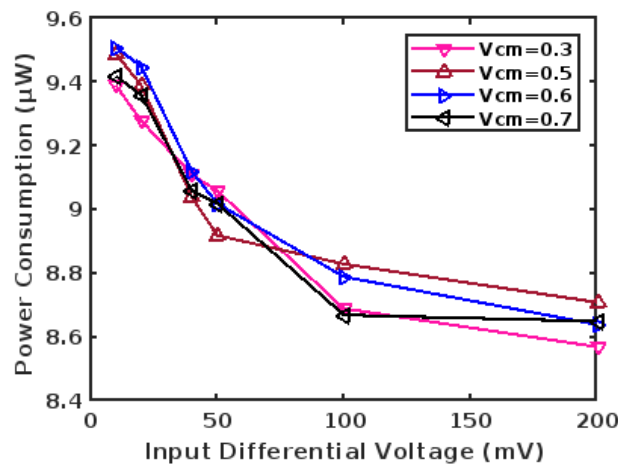
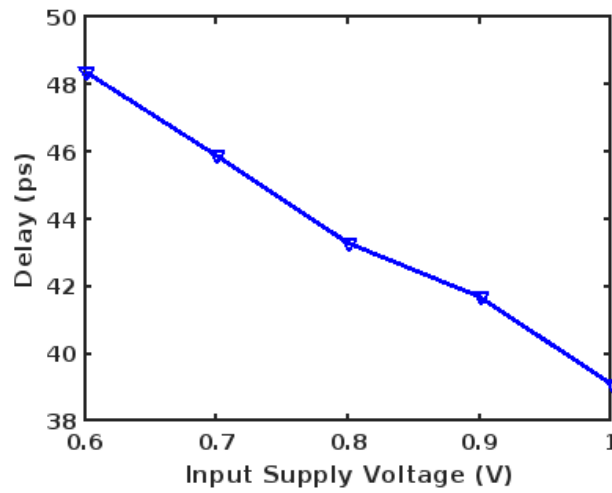


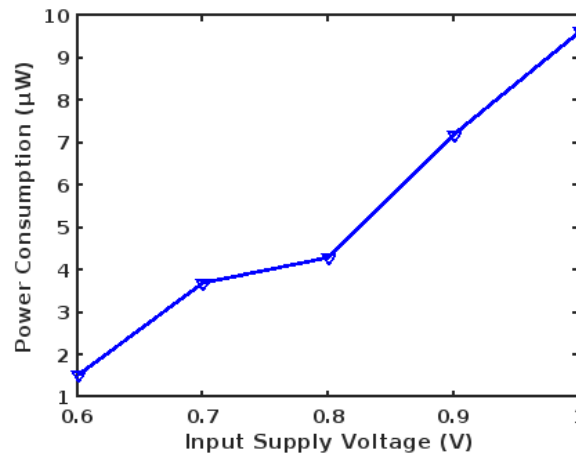
Fig. 3.17 Power consumption versus input differential voltage (V_{diff}) of the Proposed charge sharing comparator at different V_{cm} values

The delay is found to follow a decreasing behaviour with larger differential voltage difference. The impact of the common-mode voltage (V_{cm}) on power dissipation at different values of V_{diff}

has been simulated and the result outcomes have been depicted in Fig. 3.17. The observation can be made that power dissipation shows a decreasing behaviour as the value of V_{cm} rises from 0.5 to 1 V for a specific value of input differential voltage V_{diff} . Nevertheless, when the V_{cm} swing ranges from 0.7 to 1 V, there is an increase in power dissipation although still lower than that observed for the preceding amplitude. When the differential input voltage variation (V_{diff}) is 20 mV, the power dissipation decreases from 9.36 μ W at a common-mode voltage (V_{cm}) of 0.7 V to 10.06 μ W at a V_{cm} of 0.8 V.



(a)



(b)

Fig. 3.18 (a) Delay versus input supply voltage and (b) Power consumption versus input supply voltage at $V_{cm} = 0.5$ V, $\text{clk} = 1\text{GHz}$

As illustrated in Fig. 3.17, the proposed comparator under consideration exhibits reduced dependence on V_{cm} owing to the lack of static power dissipation. The simulation examines the impact of varying supply voltages V_{DD} on power dissipation and delay. The result outcomes

are depicted in Fig. 3.18 (a) that demonstrates a significant relationship between the supply voltage and the delay exhibited by the circuit. It is observed that a rise in the V_{DD} leads to the decrease in delay exhibited by the circuit. In this work, the supply voltage V_{DD} is varied from 0.6 V to 1 V and variation of power consumption along with supply voltage is shown in Fig. 3.18 (b).

3.5.4 Variation of Kickback Noise as Function of Input Common Mode Voltage in The Proposed Charge Sharing Comparator

The relationship between increasing input common mode voltage and reduced impact of kickback noise in our system is evident from the Fig. 3.19. During the pre-charged period, the input differential voltage can be applied and amplified without any occurrence of disruption as the process of regeneration has not yet commenced. During the first stage of the comparison stage, the activation of these auxiliary transistors facilitates the commencement of the decision-making and subsequent regeneration process. Additionally, the transistors operating in the triode region are connected in parallel with the input differential pair transistors. This arrangement aids in maintaining a reduced voltage variation at the drain of the input transistors, hence resulting in decreased kickback noise. Comparators operating at fast speeds and exhibiting high power efficiency tend to emit a more significant amount of kickback noise [34]. An increase in V_{cm} leads to a reduction in the noise impact in our design. As the input common mode voltage increases, there is a reduction in the kickback noise due to the impact of less voltage variations on the input transistors of the comparator.

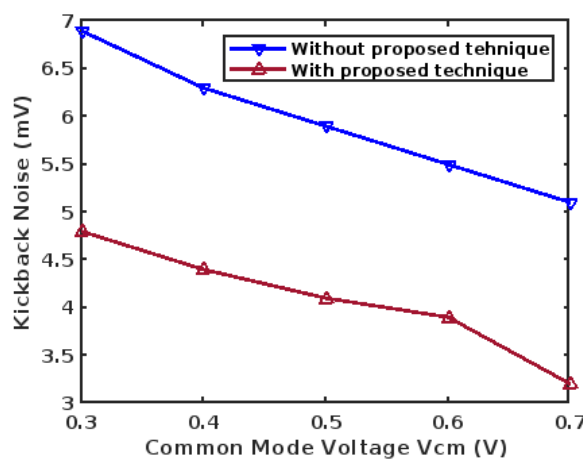


Fig. 3.19 Variation of kickback noise w.r.t V_{cm} voltage in proposed charge sharing comparator

The input differential voltage can be applied and amplified during the pre-charged period without disturbance, as the regeneration process has not yet commenced. During the first stage

of the comparison phase, the activation of auxiliary transistors facilitates the initiation of the decision-making and subsequent regeneration process [1,33]. Additionally, the transistors operating in the triode region are connected in parallel with the input differential pair transistors. This configuration aids in maintaining a lower voltage variation at the drain of the input transistors, hence reducing the occurrence of kickback noise.

Table 3.5: Summary of obtained parameters at multiple corners of proposed comparator

S.No.	Parameter	tt	ss	sf	fs	ff
1	Power Consumption (μ W)	9.5604	3.8121	8.6104	9.929	17.3914
2	Standard deviation (n)	468.26	319.51	520.92	658.77	658.77
3	Delay (ps)	48.2	107.67	101.54	44.27	40.229

The proposed comparator demonstrated reduced kickback noise by employing auxiliary transistors M8 and M9 to separate the output nodes. Additionally, this approach effectively mitigated the mismatch effect and minimized the impact of parasitic capacitance associated with the transistor design. Similarly, the monte carlo power analysis results for other corners like tt, sf and ss are summarised in Table 3.5, so for biomedical applications, under tt corner analysis the mean power of propsoed design is 9.56 μ W.

3.5.5 Corner Analysis of Proposed Charge Sharing Comparator

This section presents corner simulations to validate the efficacy of the proposed strategy across several corners, as depicted in Fig. 3.20. Simulations are conducted using extreme process, volume, and temperature (PVT) conditions. For this test set up is utilized, the simulation time is considered as of 1000 ns and for each 50 ns a test sequence is given as an input. The inputs inn and inp are given such that the differential input voltage lies in boundary conditions of either very small or very high i.e 300 mV and 300 μ V. In corner simulation PVT values are set to different process (ff, fs, ss, sf, tt), and temperature ranging from -20°C to 80 °C (-20 °C, 30 °C and 80 °C). First, the circuit was simulated for slow-slow (ss) process at T (-20 °C, 30 °C and 80 °C), then followed by process variations of slow-fast (sf), typical -typical (tt), slow-fast (sf) and fast-fast (ff) at (-20 °C, 30 °C and 80 °C).

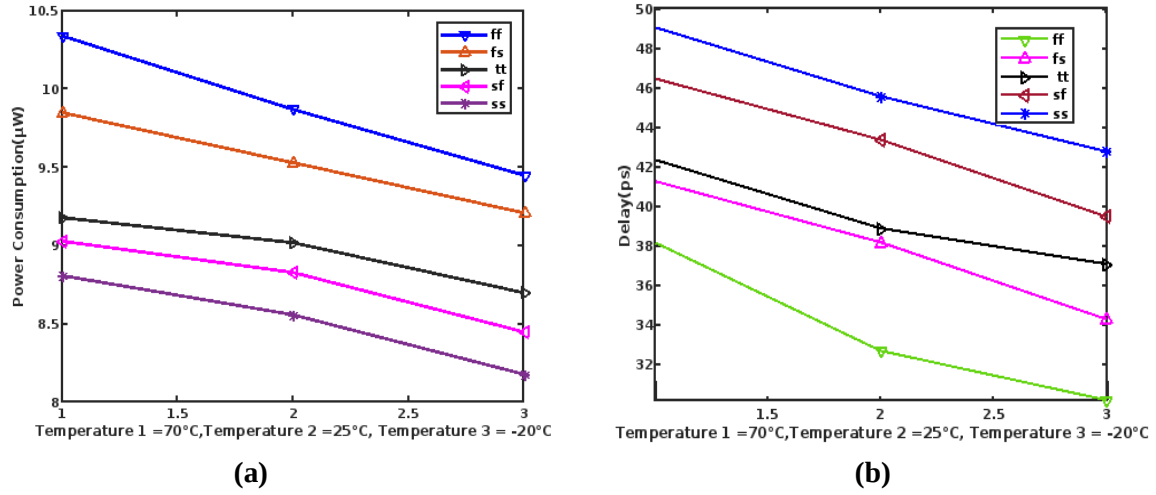


Fig. 3.20 Process corner variations on (a) Power Consumption and (b) Delay for the proposed comparator

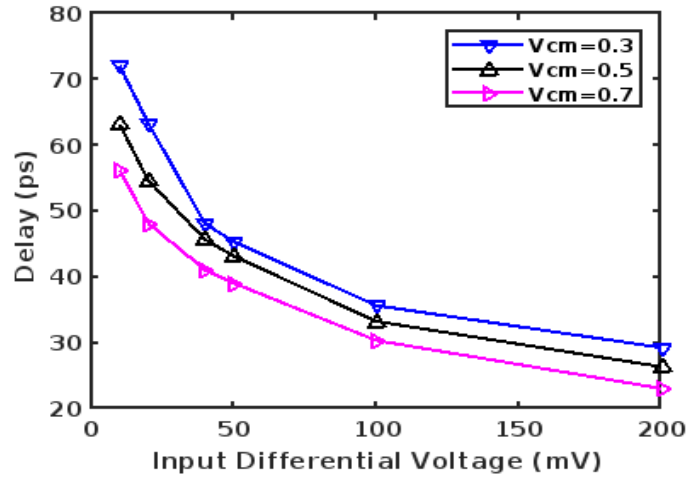


Fig. 3.21 Variation of delay versus input differential voltage of proposed comparator for multiple V_{cm} values

Also, Fig. 3.20 demonstrates that at ff, there is a significant increase in power consumption and a decrease in delay, but at ss, there is a decrease in power consumption and an increase in delay. Fig. 3.21 demonstrates an inverse correlation between the delay of the suggested comparator and input differential voltage for multiple V_{cm} .

3.6 SUMMARY OF THE IMPORTANT RESULTS

The design and parametric simulations of different low power dynamic comparators in CADENCE Virtuoso 45 nm technology node for SAR ADC is carried out. Strong Arm latch, Double Tail Dynamic comparator and Modified Double Tail Dynamic comparator are the

major architectures considered for simulation and analysis from literature. Following this, first proposed dynamic comparator architecture design along with the parametric analysis is focussed in 45 nm technology node. Rigorous analysis in terms of power, delay, monte carlo simulation at different corners like ss, sf, ff etc. and temperature analysis from -40 degree centigrade to 110 degrees centigrade is conducted for the proposed comparator. Proposed comparator outperforms the state of art dynamic comparators which is included as comparative analysis. Further, second proposed dynamic comparator based on charge shared logic is presented and its detailed analysis is included. The results obtained after simulation are summarized as follows:

1. Transient output of first proposed comparator validates that the proposed comparator is comparing two inputs even with a voltage difference of 2.5 mV.
2. The first proposed comparator is showing an average transient power of 33.81 nW at NN corner which is much reduced value compared to the other architectures like strong arm latch, double tail dynamic and modified double tail dynamic comparator considered from the literature as shown in table .
3. The power consumption is limited to 19.56 nW at SS corner and 53.85 nW for FF corner as the architecture creates an isolation between pre-amplifier and latch module when clk is low due to which leakage power is avoided.
4. The proposed comparator is simulated with capacitive loading of 5.1 pF which is the required values for utilizing this module along with capacitive DACs.
5. PDP of 0.4 fJ along with temperature variation from -40-degree centigrades to 110-degree centigrades is carried out for the first proposed comparator.
6. The Second dynamic comparator based on charge shared logic (proposed charge sharing) and kickback noise reduction logic is also proposed which is working well upto few GS/s and power consumption of 9.36 μ W is observed at 1 GS/s.
7. Proposed charge sharing logic based dynamic comparator is limiting offset voltage to 7.8 mV and the delay is limited to 48.2 ps.
8. Kickback noise analysis and statistical analysis of noise and input referred offset voltage due to common mode voltage variation (V_{cm}) shows that the effect of variation of input common mode voltage on noise, proposed charge shared logic-based circuit is less sensitive to V_{cm} variations as gm/I_D of input transistors M12 and M13 (Fig. 3.15) is increased with the biasing of transistors in weak inversion region.

9. The observed delay exhibits a reduction from 56.3 ps to 23.17 ps as the input differential voltage (V_{diff}) ranges from 10 mV to 200 mV for varying common-mode voltage levels (V_{cm}) in charge shared circuit as second proposed dynamic comparator.
10. The comparator demonstrated reduced kickback noise by employing auxiliary transistors M8 and M9 to separate the output nodes. Additionally, this approach effectively mitigated the mismatch effect and minimized the impact of parasitic capacitance associated with the transistor design.

It is summarized that dynamic comparators are the clocked comparators, and their architecture includes preamplifier and regeneration latch to compare two inputs. Pre-amplifier gain (G) of a dynamic comparator depends on the g_m/I_D of pre-amplifier transistors which is a function of common mode voltage variations where g_m is the transconductance of pre-amplifier transistors and I_D is the drain current. To improve the noise rejection capability of a dynamic comparator, the differential pre-amplifier Gain (G) has to be high. Also, to limit power consumption of a dynamic comparator, techniques like charge shared approach, isolation between preamplifier and regeneration latch in reset mode has surely reduced the power consumption of a dynamic comparator. Delay of a dynamic comparator depends on the pre-amplifier gain which in turn depends on the ΔV between outp and outn at the start of latch regeneration. With increase in the ΔV , the regeneration delay time has been reduced. These considerations resulted in the two proposed comparators in this chapter as first proposed dynamic comparator based on isolation between preamplifier and regeneration latch in reset mode and second one is based on charge shared approach technique.

CHAPTER 4

Design and Analysis of DAC with Improved Switching Scheme for Reduction in Switching Energy per Conversion Cycle

4.1 BRIEF INTRODUCTION ABOUT CHAPTER

Designing of DAC unit with reduced switching energy has become the core area of working for the researchers in the design of ultra-low power SAR ADC. Based on designed DAC unit, the single ended and differential SAR ADC architectures became two prominently available designs incorporating SAR logic. Single ended SAR ADC is best utilized for the applications requiring low power consumption as major constraint compared to high SNR while differential architecture is preferred for high acceptable SNR in the digitized output. The Digital-to-Analog Converter (DAC) is tasked with the conversion of digital code emanating from the Successive Approximation Register (SAR) logic to an analog voltage level that is subsequently utilized by the comparator [137] in digitization. As the resolution of the system grows, there is an increase in the mismatch of the capacitor array [138] and as a result, the linearity of the SAR ADC gets reduced. The reduction in size of CMOS technologies facilitates the augmentation of sampling frequency. It is worth noting that most of the overall power consumption is attributed to the digital-to-analog converter (DAC), which is specifically allocated for the capacitor array as well as switching mechanism [139]. One of the primary concerns in mitigating energy consumption involves the shrinking of array capacitors along with the implementation of alternative approaches [140]. With an aim to reduce switching energy per conversion cycle in digital to analog converter, which is the most power-hungry module of SAR ADC, following objective is framed:

Design and Analysis of DAC with improved switching scheme based on capacitive splitting for reduction in switching energy per conversion cycle.

The methodology used to achieve desired objective involved following steps: -

- Literature review and analysis of existing switching schemes to insight the switching energy per conversion step in existing DACs.
- Designing of novel DAC with reduced switching energy per conversion cycle with zero switching energy in atleast two MSB comparisons.

- Simulation and analysis of designed DAC circuit in CADENCE Virtuoso 45 nm technology node.
- Comparison of novel switching scheme with existing switching schemes like capacitive splitting, charge redistribution, level switching in terms of switching energy and number of capacitors used.

In this chapter, design of digital to analog converter (DAC) which is to be utilized in the design of 8-bit SAR ADC is considered. DAC module is the most power hungry module of SAR ADC and it is designed using capacitive array incorporating low power switching scheme to create intermediate voltage levels used for the comparison in the digitization process of an analog sample. Based on the DAC design, single ended SAR ADC which quantize the sampled value between zero to V_{ref} and differential SARADC that quantizes the sampled value between V_{ref} to V_{ref} exists in the literature. In this work, design of single ended technique is considered which is more desirable for the low power DAC design. Proposed switching scheme utilize single reference voltage of $V_{ref}/2$ and perform first two MSB comparisons with zero switching energy. Proposed scheme required average of $57.4 CV_{ref}^2$ of switching energy which is much reduced value approximately reduced by 92 percent compared to conventional capacitor-based switching scheme. Also, compared to conventional switching scheme, number of capacitors in the DAC array have been reduced by 50 percent.

The present chapter is divided into seven sections, starting with a brief introduction of chapter as first section 4.1 and section 4.2 presents an overview of digital to analog converters. In third section as 4.3, existing different major switching schemes of digital to analog converters are focussed in which subsection 4.3.1 includes the bottom plate sampling-based charge redistribution DAC (CDAC), subsection 4.3.2 presents the common mode (V_{cm}) based switching scheme and monotonic switching scheme for DAC and in subsection 4.3.3 capacitor splitted switching scheme is discussed. Further, section 4.4 includes comprehensive view of proposed single ended switching scheme. In Section 4.5 choice among different available capacitors is included and section 4.6 includes brief view of sample & hold circuit design and its architecture . Finally, all the important outcomes are summarized in section 4.7.

4.2 OVERVIEW OF DIGITAL TO ANALOG CONVERTERS (DACs)

In Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs), the Digital-to-Analog Converter (DAC) constitutes one of the most critical building blocks,

directly influencing both the accuracy and power efficiency of the overall system. The primary role of the DAC in a SAR ADC is to iteratively generate reference voltages corresponding to the successive bit decisions during the conversion process. This charge redistribution operation forms the core mechanism that enables SAR ADCs to achieve medium-to-high resolution with moderate speed and low power consumption [104]. Among various DAC implementations, the capacitive charge redistribution DAC architecture is widely adopted due to its excellent matching characteristics, inherent sample and hold functionality offering compatibility with CMOS technology [138]. However, in such architectures, the capacitor array occupies a substantial portion of the total area and contributes significantly to dynamic power consumption during the bit-cycling process. As technology scales and power constraints become more stringent especially in portable and energy-efficient systems, the optimization of the DAC switching scheme becomes a crucial design objective. Conventional DAC switching techniques often suffer from large switching energy, complex control logic, and unequal reference voltage utilization, which degrade the converter's overall energy efficiency.

To address these challenges, recent research has focused on innovative switching algorithms and capacitor array optimizations that minimize the average switching energy, reduce reference buffer loading, and enhance conversion speed without compromising accuracy. Therefore, it is worth mention that the design of an energy-efficient, low-area and high-linearity DAC remains a key factor in improving the overall performance of SAR ADCs. Continued exploration in this domain aims to achieve optimal trade-offs among power, area, resolution, and conversion speed that establish DAC design a central aspect of modern low-power data converters research work. Further, an energy efficient switching scheme based capacitive digital to analog converter (CDAC) is the major requirement for ultra-low power design of SAR ADC [83] which in turn creates a significant importance in the domain of bio-medical signal acquisition. This chapter explores the design of capacitor array-based DAC unit with switching scheme felicitating atleast first two MSB comparisons with zero switching energy and serves utilization in an eight-bit SAR-ADC for integration into the analog front end of bio-signal acquisition. The focus of this technology pertains to the monitoring of implanted bio-signal devices, with a specific emphasis on ECG/EEG signals. A capacitive digital-to-analog converter (DAC) is suggested as a means to attain power consumption in the microwatt range. An energy efficient switching enables comparisons to be made without any energy consumption, leading to a substantial enhancement in energy efficiency.

The DAC design that employs the reduction in the amount of total capacitance resulting in the reduction in power usage and DAC area. The array capacitance value within DAC gets adjusted down to the closest integer value, resulting in uniform geometries. Instead of a single level voltage, the concept of multi-level voltages is also considered. Primarily, power consumption reduction has been achieved by employing two parameters: (i) Reducing capacitance in DAC array and (ii) by employing varying voltage levels. The use of CDAC is deemed appropriate for the low-power SAR ADC. Nevertheless, several voltage switching techniques have the potential to enhance the efficiency of power usage during switching operations as switching schemes work to switch the voltage level without any energy consumption of supply. As a result, there is an improvement in energy conservation for ultra-low power design.

4.3 EXISTING DIFFERENT MAJOR SWITCHING SCHEMES OF DIGITAL TO ANALOG CONVERTER

Diverse switching schemes of DAC like traditional single ended [68], split capacitor[75], monotonic [69], V_{cm} based [76], CAS based [77], merged capacitor [78] and Weibu hu [79] creates switching of voltage level with reduced switching energy and facilitate a reduction in the area occupied by capacitors. It is worth noting that the choice of CDAC structures as well as voltage switching methods is crucial in order to design an energy efficient digital to analog converter. The charge-sharing voltage switching strategy including two arrays (most significant bit and least significant bit) in the CDAC structure has found its good utilization in the ultra-low-power SAR ADC designed for biomedical applications. Energy efficient switching schemes utilized in the designing of ultra-low power DAC to be utilized in low power SAR ADC design are presented in next section.

4.3.1 Bottom Plate Sampling Based Charge Redistribution DAC (CDAC) Switching

In a CDAC, the total capacitance serves both as a sampling network and as a charge storage element during the conversion process as shown in Fig. 4.1 corresponds to the bottom plate sampling based CDAC architecture. Initially, the input signal is sampled across the capacitor array, and during each bit cycle, selected capacitors are switched between reference voltages (usually V_{ref} and ground) according to the SAR logic decisions. The redistribution of charge among capacitors produces a corresponding analog voltage that represents the digital code being tested. During the initial phase of a conversion process, the signal from the input V_{IN} has subjected to sampling by means of the S switches, whereby the bottom capacitive plates of each

capacitor are utilised. Meanwhile, the upper plate, also known as node V_X , has a connection to V_{CM} .

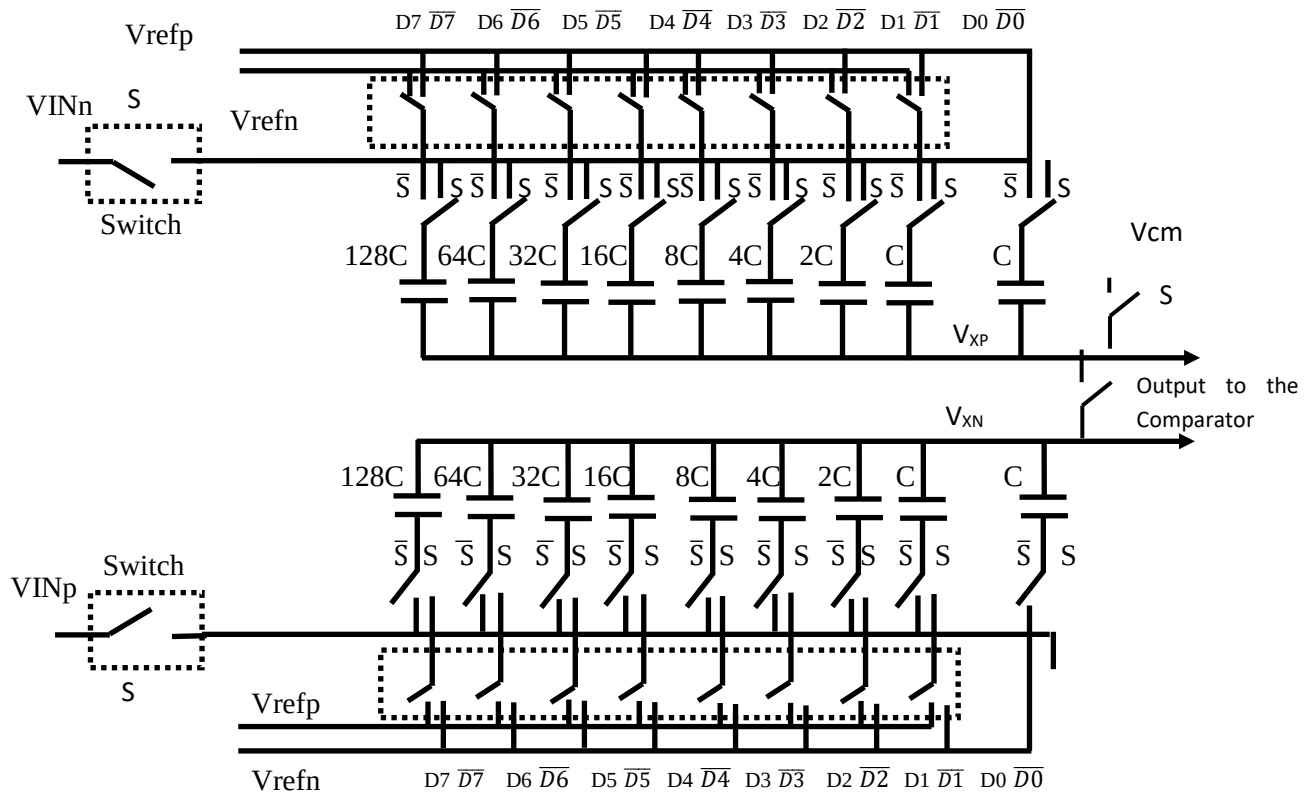


Fig. 4.1 Bottom plate sampling based CDAC architecture

The total charge stored on the capacitive array becomes equal to the product of the input voltage V_{IN} and the sum of all the capacitors present. Equation (4.1) depicts the voltage along with charge in the node V_X , respectively. In the sampling stage,

$$V_x = V_{CM} = 0 \quad (4.1)$$

$$Q_x = -V_{IN} \cdot 8C \quad (4.2)$$

Eq. (4.2) represents the net charge on the capacitor array. Following the sampling phase, the upper plates of the capacitor array are disconnected from V_{CM} , while the lower plates are disconnected from V_{IN} and subsequently switched according to the digital code generated by the SAR logic. In the first comparison cycle, the digital-to-analog converter (DAC) is initialized to the code 10000000 by setting the most significant bit (MSB) to logic '1'. Equations (4.3-4.4) describes the resulting variation in node voltage V_X , which arises due to charge redistribution and voltage division with respect to V_{CM} (assumed to be zero in this case). This operation

effectively compares V_{IN} with half of the reference voltage V_{ref} . The comparator outputs a logic ‘1’ when $V_{IN} > V_{ref}/2$, resulting in $V_X < 0V$. Otherwise, when this condition is not satisfied, the comparator output is ‘0’.

$$\text{For DAC} = 10000000, \Delta v = \frac{4c}{4c+2c+c+c} \quad (4.3)$$

$$V_X = -V_{IN} + \Delta v = -V_{IN} + \frac{V_{ref}}{2} \quad (4.4)$$

In the subsequent comparison cycle, the most significant bit (MSB) retains the value of the comparator output D_2 , while the second most significant bit (MSB–1) is tentatively set to logic ‘1’. The input voltage V_{IN} is then compared with either the upper half of V_{ref} when $D_2 = 1$, or the lower half of V_{ref} when $D_2 = 0$. After this comparison, the MSB–1 bit is updated based on the comparator output D_1 , and the next lower-order bit (MSB–2) is set to logic ‘1’ for the following trial. This successive approximation process continues for all remaining bits. After performing $N = 8$ comparison cycles, the SAR ADC generates the final digital output code $D_7D_6D_5D_4D_3D_2D_1D_0$, which corresponds to the analog voltage level V_{DAC} as defined by the DAC transfer characteristics.

This switching scheme implementation utilizes larger area as each capacitor value doubles successively from C , $2C$, $4C$, $8C$, $16C$ and so on. This leads to a large total capacitance and hence a large silicon area, especially for higher resolution. For an n -bit SAR ADC, the total capacitance $\approx 2^n \times C$, which grows exponentially with resolution. Also, switching energy per conversion for this scheme is high as during each bit decision, capacitors are charged and discharged repeatedly, leading to dynamic switching energy loss. Also, capacitor mismatch due to process variations can cause Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) errors. So, reduction of area in capacitor array by reducing the size of MSB capacitor along with the inclusion of optimized switching scheme is required to design a low power digital to analog converter. Discussion regarding improvement in switching scheme is carried forward in the next section.

4.3.2 Common Mode (Vcm) Based Switching Scheme and Monotonic Switching Scheme for DAC

In a SAR ADC, the Capacitor Digital-to-Analog Converter (CDAC) determines the conversion accuracy and power consumption. While the conventional switching scheme requires full-scale transitions between V_{ref} and ground, resulting in high switching energy and large reference

voltage swing, the V_{cm} based switching scheme (also called common-mode-based switching) was introduced to reduce power consumption and reference voltage variation. This scheme maintains the common-mode voltage V_{cm} at the comparator input nearly constant throughout the conversion process, thereby minimizing dynamic power and improving conversion linearity. Fig. 4.2 illustrates 3-bit examples comparing the V_{cm} based switching scheme [76] and monotonic capacitor switching techniques [69]. The common mode-based switching scheme relies on a trial-and-error process. As shown in Fig. 4.2 it depicts all possible conversion scenarios along with the corresponding energy consumption for each switching phase. This method proves efficient only when every comparison attempt is successful, as demonstrated in the upper cases. However, when comparisons fail, as in the lower cases, the energy consumption increases significantly. In contrast, Fig. 4.3 presents the switching sequence of the monotonic switching method. Once the sampling switches are turned off, the comparator executes the first comparison directly, without performing any capacitor switching

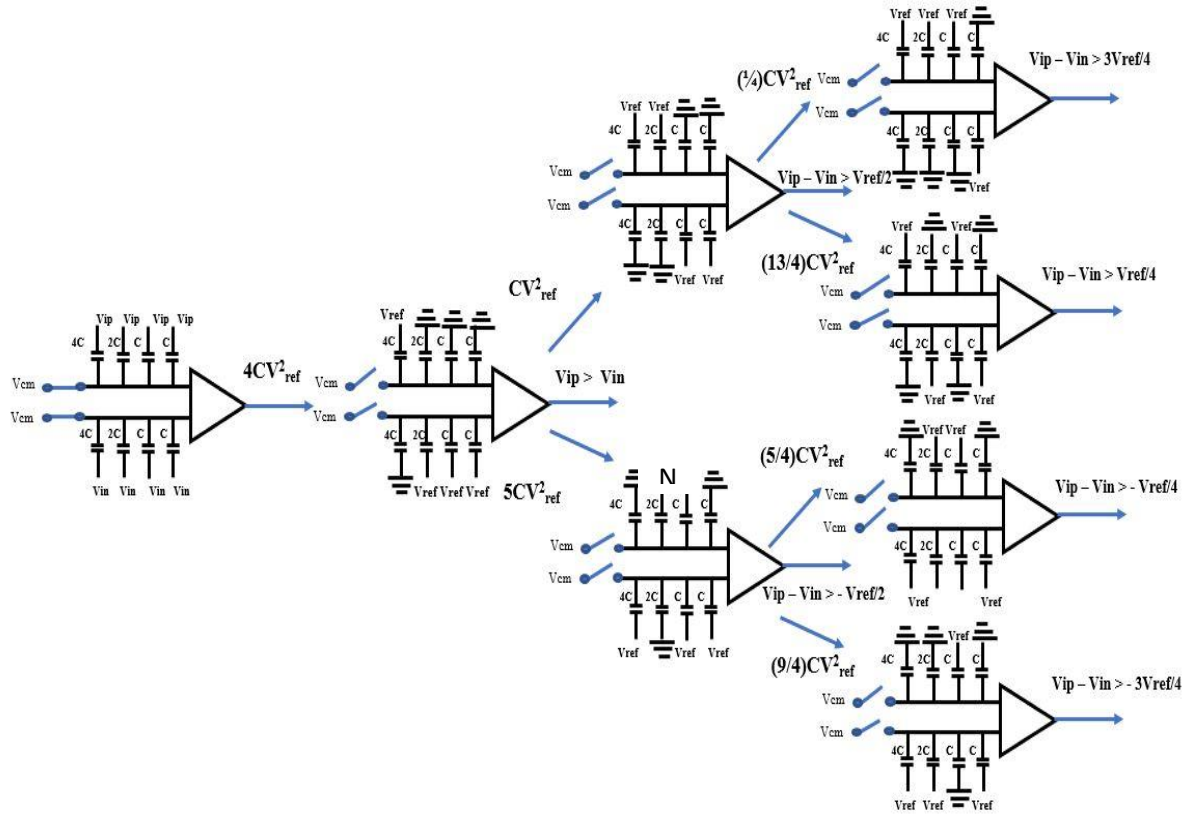


Fig. 4.2 Conventional switching scheme of capacitive DAC

beforehand. Hence, no energy is consumed prior to the first comparison. On the other hand, the common mode-based technique dissipates energy even before the initial comparison occurs. Furthermore, the subsequent switching stages in the proposed scheme are designed to be more energy-efficient compared to those in the traditional approach. Advantages of common mode-

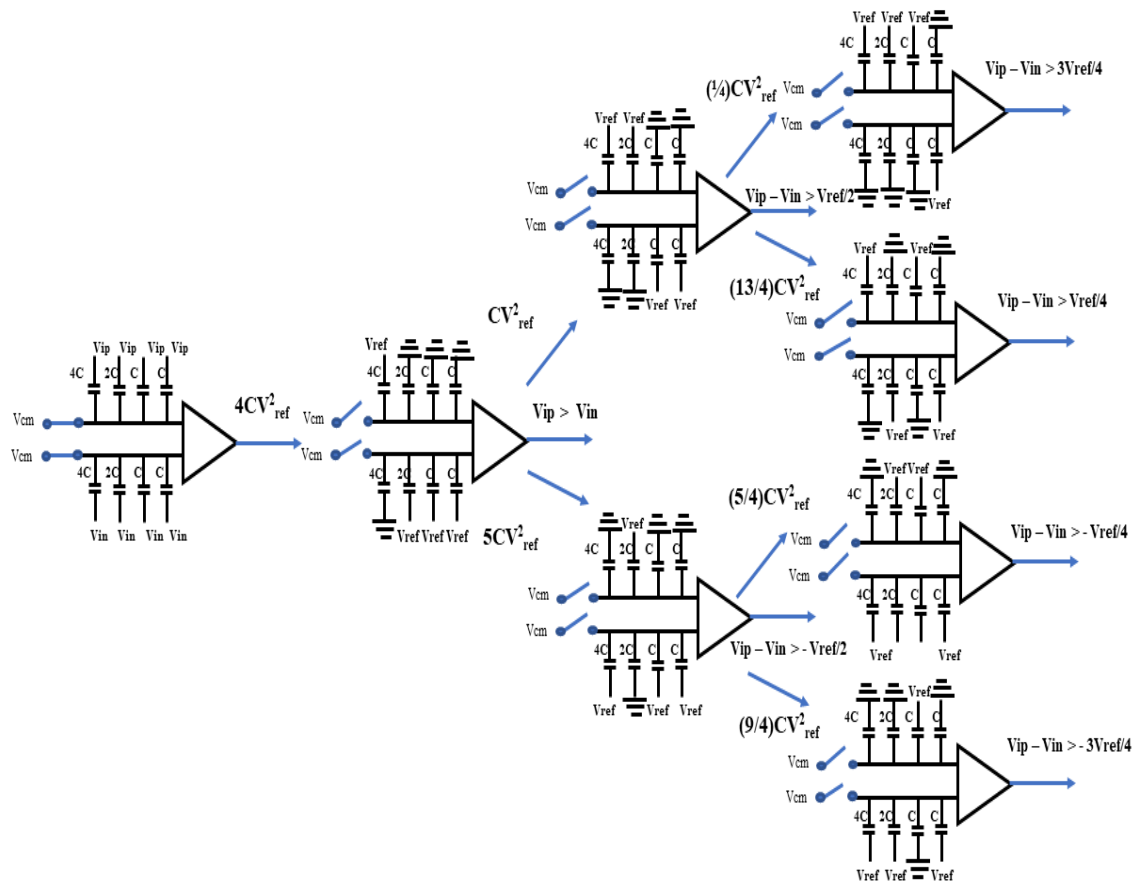


Fig. 4.3 Monotonic switching scheme of capacitive DAC

based switching scheme is that power consumption gets reduced by 75% compared to conventional switching due to smaller voltage swing. Its RC delay is also reduced by smaller voltage steps, but its control logic is slightly more complex. Also, capacitance parasitics still exist which leads to common mode voltage offset. The conventional V_{cm} based switching scheme is an effective solution to the limitations of traditional SAR ADC switching. By maintaining a constant common-mode voltage and reducing the switching amplitude, it provides substantial power savings, enhanced speed, and improved linearity, making it ideal for low-power, high-speed, and medium-resolution SAR ADCs.

4.3.3 Capacitor Splitted Switching Scheme of DAC

In a Capacitor-Splitting Technique [75], the total DAC capacitor array is divided into two sub-arrays a MSB array and a LSB array, typically connected via a bridge capacitor C_{bridge} . The major objective is to reduce total capacitance which saves area and power of designed DAC. The MSB array is of N_1 bits, MSB array is of N_2 bits and $N_1 + N_2 = N$ which is the total number of bits of designed ADC. Switching technique includes the sampling phase in which input V_{in} is sampled across the full capacitor network (both arrays). All bottom plates connect to V_{INV} (or V_{CM} in differential design). MSB bits are resolved first using the MSB array. After MSB decisions are made, the bridge capacitor and LSB array handle fine-tuning for lower bits. Switching follows similar rules to conventional SAR but involves smaller effective capacitance for LSBs leads to the reduced energy. The total capacitance of DAC array gets reduced which in turns gives advantage of smaller chip area. Also, due to smaller switches nodes the dynamic power dissipation is reduced at higher resolution of 12 bits to 14 bits. Also, the switching scheme maintains monotonicity and linearity with the careful bridge capacitor matching.

However, the switching scheme shows missing code error if there occurs any slight mismatch between bridge capacitance and DAC array capacitance so mismatching and linearity errors are far more in this switching scheme. Also, its layout is very complex and parasitics capacitances effects are far more. Also, these parasitic capacitances cause gain error, reduced accuracy and nonlinear charge transfer. Unlike V_{cm} based switching, the capacitor-split technique does not inherently maintain a constant common-mode voltage at the comparator input. Common-mode variations increase comparator kickback noise and can degrade comparator accuracy. A slight small deviation (1-2 %) causes noticeable gain error for higher resolutions. Keeping these important considerations, a new switching technique for single ended SAR ADC with zero switching energy in first two MSB comparisons with 50 % reduced total capacitance value compared to conventional switching is hereby presented in the next section.

4.4 A COMPREHENSIVE VIEW OF PROPOSED SINGLE ENDED SWITCHING SCHEME

Proposed DAC unit consists of $2 \times 2^{N-1} C = 2^N C$ total capacitance value. Based on SAR control unit decision, the DAC capacitances are to be switched between ground and $V_r/2$ which in turns creates the switching energy dissipation in the ADC architecture. This work includes a digital to analog converter with a single voltage of $V_r/2$ where V_r is the reference voltage which is taken as 1.2 V in the proposed design . The DAC unit consumes zero switching energy in the

first two MSB decisions as per given switching algorithm. Initially, $V_r/2$ and V_{in} is sampled onto the capacitances of DAC X and DAC Y respectively. In DAC X in the sampling phase, only MSB capacitance is charged otherwise all remaining capacitances in the DAC X unit are kept uncharged. Similarly, input voltage is sampled completely onto the MSB capacitance of DAC Y and direct comparison of $V_r/2$ with V_{in} is evaluated in the first comparison cycle with no switching energy required in MSB bit decision. Flow chart of implemented switching scheme is given in Fig. 4.4.

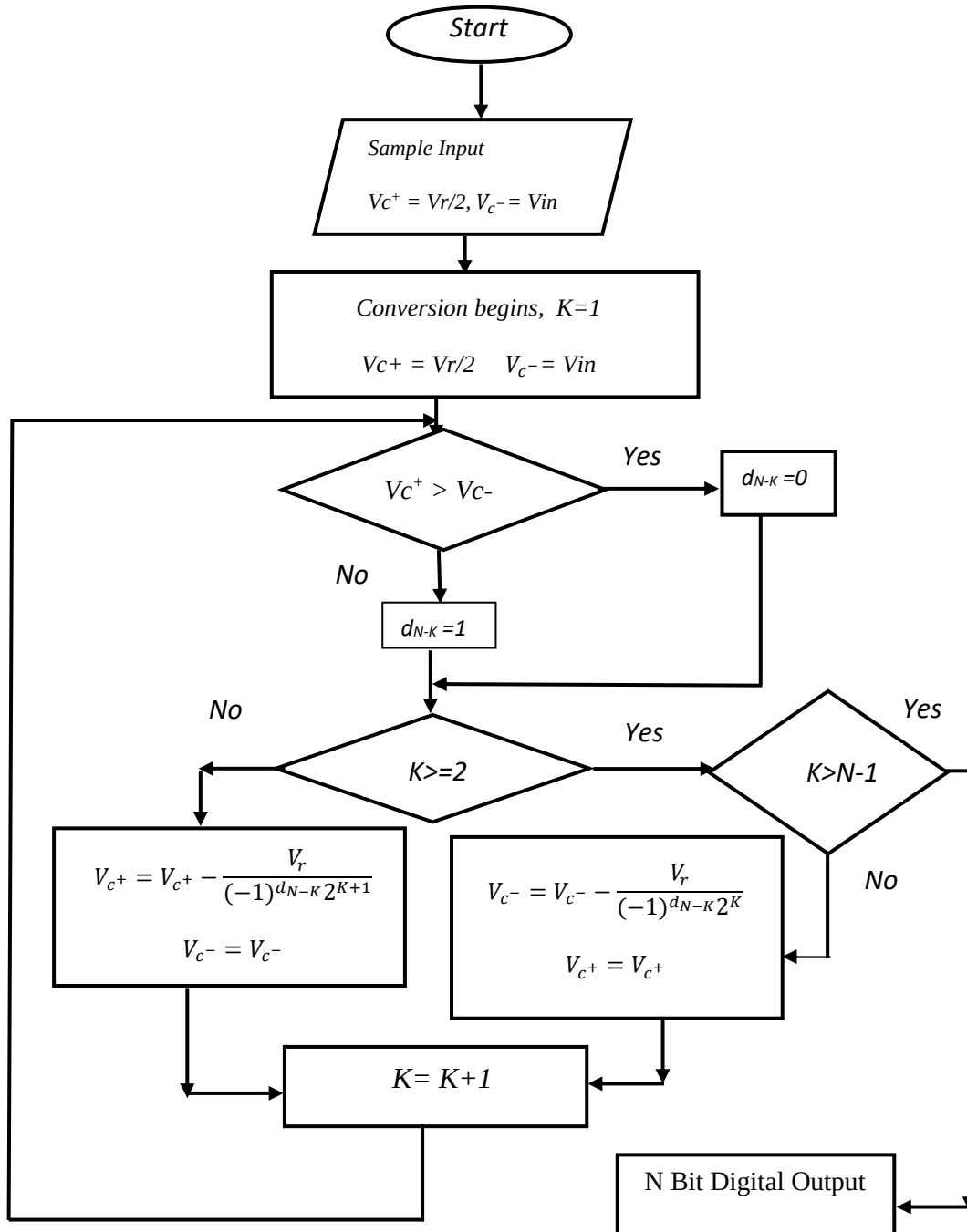


Fig. 4.4 Flow chart of proposed single ended switching scheme

In the first stage when $K=1$, $V_r/2 > V_{in}$ is directly compared by the comparator. After comparison out, d^{N-1} bit will be either 0 or 1. Further, $K > 2$ condition will be checked, and further switching will take place. The lower plates of DAC X capacitors and DAC Y capacitors will be switched to either ground or $V_r/2$ depending upon the output of $V_r/2 > V_{in}$ as shown in implemented switching scheme Fig. 4.5. If $V_r/2 > V_{in}$ condition gets true, then lower plates of DAC X will be switched to ground otherwise lower plate of DAC X will be switched to $V_r/2$. Further, if $K > 2$ condition gets failed, switching is done to follow $V_{c+} = V_{c+} - \frac{V_r}{(-1)^{d_{N-K-2K+1}}}$ and $V_{c-} = V_{c-}$ while for $K > 2$ gets true and $K < N-1$ then switching is done to follow $V_{c-} = V_{c-} - V_r - 1d_{N-K-2K}$ and $V_{c+} = V_{c+}$. Finally, when $K < N-1$ condition gets failed, N bit digital output will be obtained.

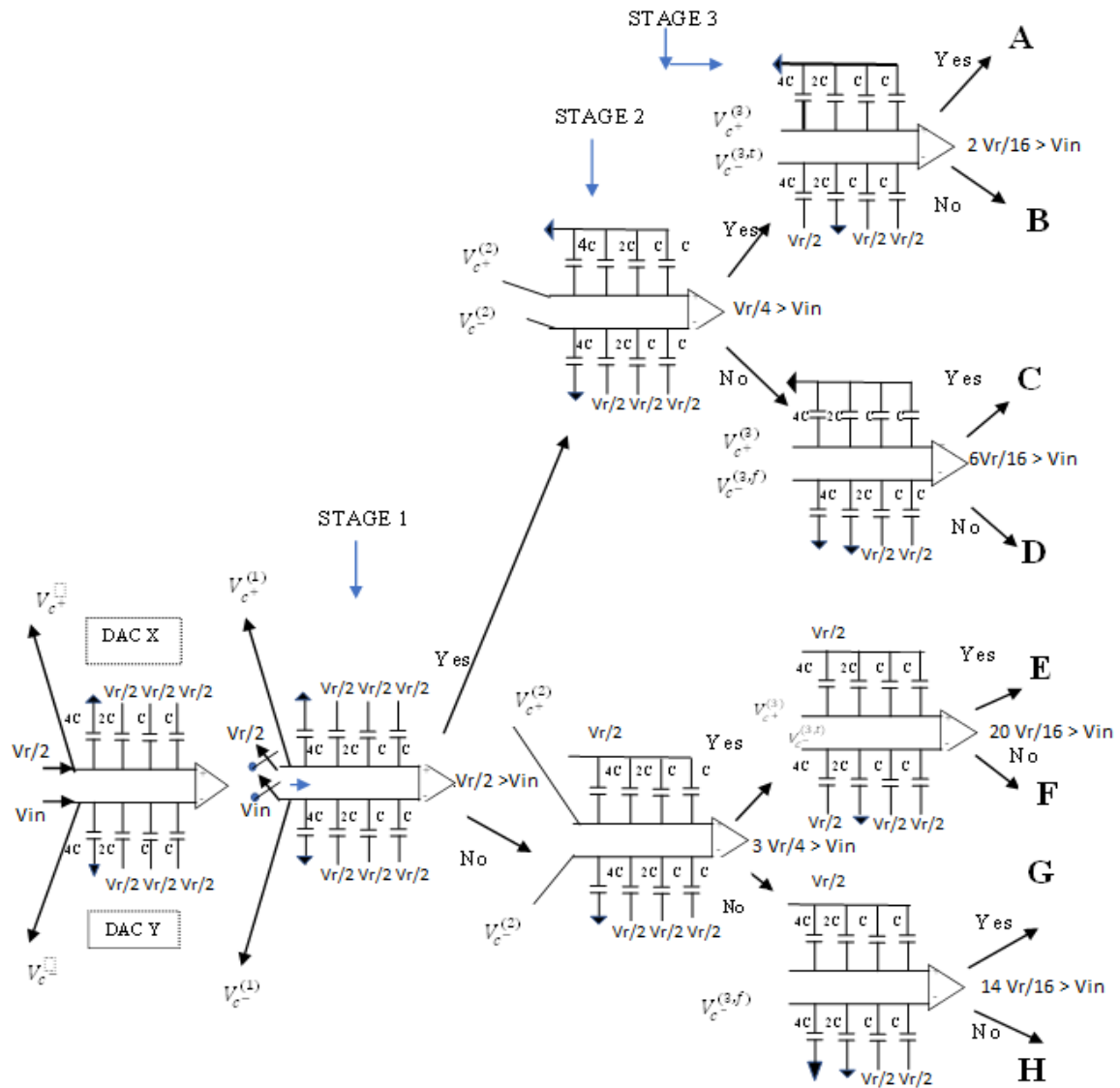
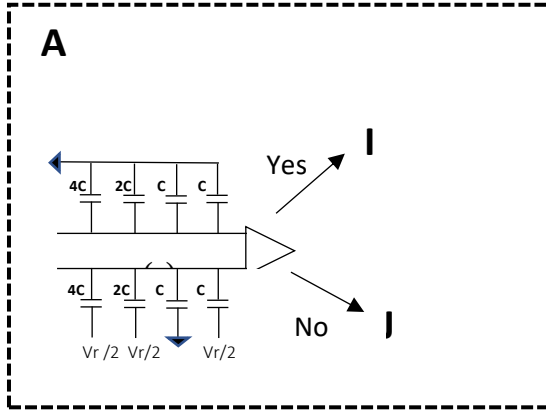
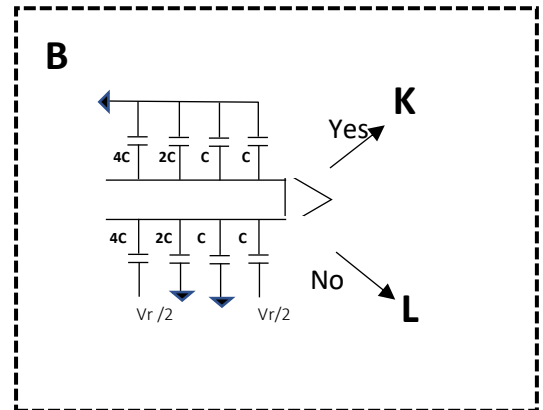


Fig. 4.5 Implemented proposed switching scheme for 4-bit DAC

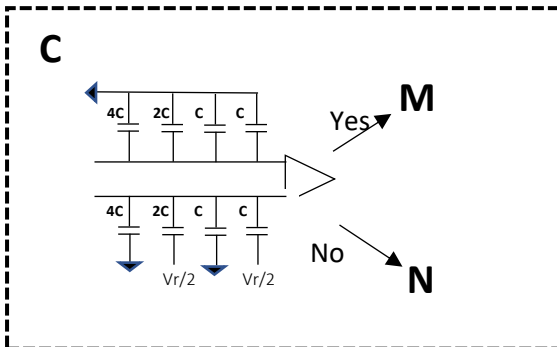
After sampling, conversion process gets started and applied $V_r/2$ along with V_{in} gets switched off using switch. The initial stage 1 directly compares $V_r/2$ with V_{in} with zero switching energy. Further, if $V_r/2 > V_{in}$ condition is satisfied then, lower plate of DAC X capacitors gets switched to ground otherwise lower plate of DAC X capacitors gets switched to $V_r/2$ and circuit is transferred to stage 2 of the conversion process.



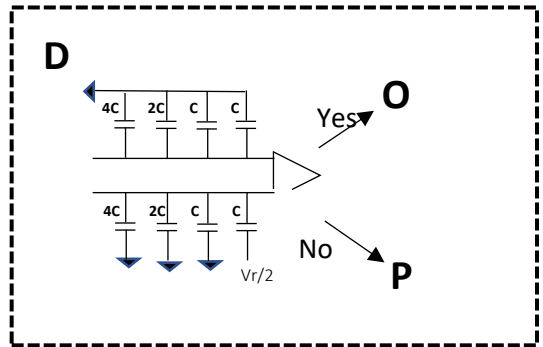
(a)



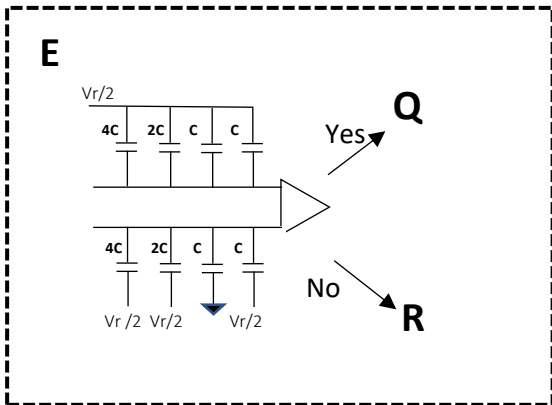
(b)



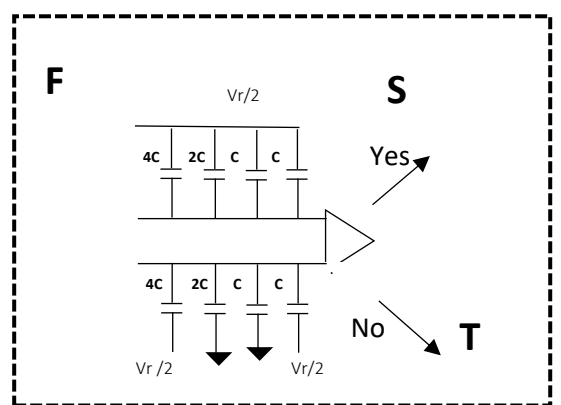
I



(d)



(e)



(f)

Fig. 4.6 Proposed single ended switching scheme (a) – (f) for generation of multiple states

The switching methodology suggests that $V_r/2$ is sampled as V_{c+} onto the top plate of DAC X capacitors in which only MSB capacitor $4C$ is charged while other remaining capacitors in DAC X remains uncharged. Similarly, in DAC Y, V_{in} is sampled onto the MSB capacitor $4C$. Further, the ‘Yes’ state with this switching evaluates $V_r/4 > V_{in}$ condition while ‘No’ state evaluates $3V_r/4 > V_{in}$. In stage 1, switching condition equations is given by eq. (4.5 to 4.18):

$$V_{c+}^{(1)} = \frac{V_r}{2}, V_{c-}^{(1)} = V_{in} \text{ and } \frac{V_r}{2} > V_{in} . \quad (4.5)$$

Similarly, after second stage of conversion the circuit gets switched to third stage with multiple evaluation conditions of $2V_r/16 > V_{in}$, $6V_r/16 > V_{in}$, $20V_r/16 > V_{in}$, $14V_r/16 > V_{in}$ which in turn gets switched to conditions of stage A,B; stage C,D; stage E,F; stage G,H which are represented in Fig. 4.6 (a) to Fig. 4.6 (f) and Fig. 4.7. In stage 2, for condition $\frac{V_r}{2} > V_{in}$ gets true, switching is carried out to satisfy: $Q_{initial} = Q_{final}$, we get:

$$4C. V_{c+}^{(1)} + 4C (V_{c+}^{(1)} - V_r/2) = 8C V_{c+}^{(2)}, \quad (4.6)$$

$$V_{c+}^{(2)} = \frac{V_r}{4} \Rightarrow V_{c+}^{(2)} = \frac{V_r}{4} = V_{c+}^{(1)} - \frac{V_r}{4} . \quad (4.7)$$

Further, in stage 2, $V_{c-}^{(1)} = V_{c-}^{(2)} = V_{in}$ so, for yes condition in stage 2, $\frac{V_r}{4} > V_{in}$ is checked for yes condition from stage 1 and for no condition from stage 1,

$$V_{c+}^{(1)} + \frac{V_r}{4} = V_{c+}^{(2)} \Rightarrow \frac{3}{4} V_r, V_{c-}^{(2)} = V_{c-}^{(1)} \Rightarrow V_{in}. \quad (4.8)$$

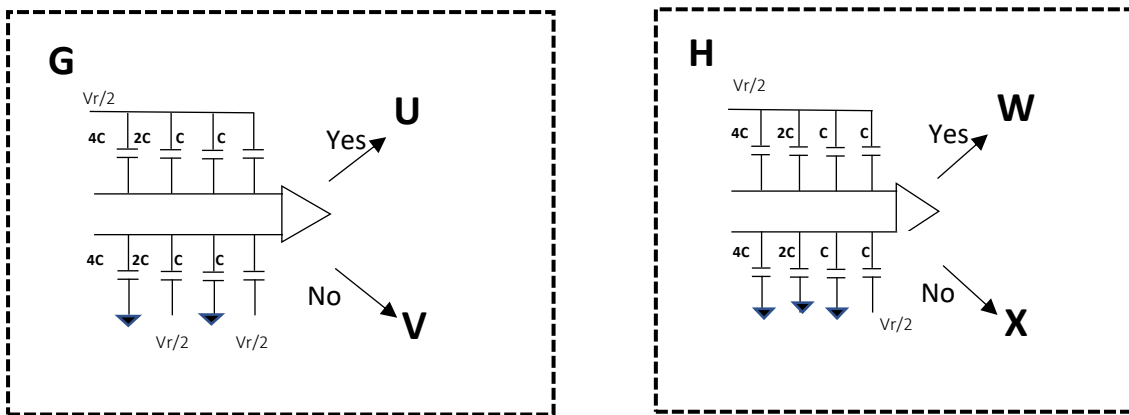


Fig. 4.7 Extension of last implemented switching step of proposed switching scheme

So, for no condition from stage 1, $\frac{3}{4} V_r > V_{in}$ will be checked to digitize. In stage 3, $V_{c+}^{(3)} = V_{c+}^{(2)}$ this is same for either true or false condition from stage 2, now the differentiated voltages will be of negative terminal. For true condition from stage 2:

$$2c V_c^{(2)} + 2c \left(V_c^{(2)} - \frac{V_r}{2} \right) = c V_c^{(3)} + 3c \left(V_c^{(3,t)} - \frac{V_r}{2} \right), \quad (4.9)$$

$$4c V_c^{(2)} - 2c \frac{V_r}{2} = 4c V_c^{(3,t)} - \frac{3c V_r}{2}, \quad (4.10)$$

$$4c V_c^{(2)} - 2c \frac{V_r}{2} + \frac{3c V_r}{2} = 4c V_c^{(3,t)}, \quad (4.11)$$

$$4 V_c^{(2)} + \frac{V_r}{2} = 4 V_c^{(3,t)}, \quad (4.12)$$

$$V_c^{(3,t)} = V_c^{(2)} + \frac{V_r}{8}. \quad (4.13)$$

For false condition from stage 2:

$$2c V_c^{(2)} + 2c \left(V_c^{(2)} - \frac{V_r}{2} \right) = 3c V_c^{(3)} + c \left(V_c^{(3,f)} - \frac{V_r}{2} \right), \quad (4.14)$$

$$4c V_c^{(2)} - 2c \frac{V_r}{2} = 4c V_c^{(3,f)} - \frac{c V_r}{2} \quad (4.15)$$

$$4c V_c^{(2)} - 2c \frac{V_r}{2} + \frac{c V_r}{2} = 4c V_c^{(3,f)}, \quad (4.16)$$

$$4 V_c^{(2)} - \frac{V_r}{2} = 4 V_c^{(3,f)}, \quad (4.17)$$

$$V_c^{(3,f)} = V_c^{(2)} - \frac{V_r}{8}. \quad (4.18)$$

Table 4.1: Comparison of existing schemes with proposed single ended switching scheme

S.No.	Architecture	Energy Conversion (CV ² _{ref})	Normalized Total Energy	No. of Unit Capacitors
1	Traditional single ended [68]	682.5	1	2 ^{N+1}
2	Split Capacitor [75]	427.66	0.62	2 ^N
3	Monotonic [69]	255.5	0.37	2 ^N
4	Vcm-based, Zhu [76]	170.17	0.249	2 ^N
5	CAS based [77]	88.6	0.129	2 ^N
6	Merged Capacitor [78]	84.7	0.124	2 ^{N-1}
7	Weibu Hu [79]	84.7	0.124	2 ^N
8	Bi-directional [70]	42.7	0.062	2 ^{N-1}
9	This Work	57.4	0.084	2 ^N

In this way the switching is continued till n bits gets generated for a sampled analog value. Table 4.1 depicts that total number of unit capacitors required in the proposed capacitive

switching scheme is $2^N C$ which is 50 percent reduced value compared to conventional switching. Additionally, switching energy factor has been reduced to $57.4 CV_{ref}^2$ compared to $682.5 CV_{ref}^2$ in traditional single ended as shown in same Table 4.1. In this fashion, stage 3 will generate further outputs as true (Yes) condition and false (No).

Table 4.2: Different output logic states of 4-bit DAC in proposed switching

S. No.	Stage	Comparator Output	Vin Range	Output Code
1	I	YES	$0 < V_{in} < V_{ref}/16$	0000
2	J	NO	$V_{ref}/16 < V_{in} < 2V_{ref}/16$	0001
3	K	YES	$2V_{ref}/16 < V_{in} < 3V_{ref}/16$	0010
4	L	NO	$3V_{ref}/16 < V_{in} < 4V_{ref}/16$	0011
5	M	YES	$4V_{ref}/16 < V_{in} < 5V_{ref}/16$	0100
6	N	NO	$5V_{ref}/16 < V_{in} < 6V_{ref}/16$	0101
7	O	YES	$6V_{ref}/16 < V_{in} < 7V_{ref}/16$	0110
8	P	NO	$7V_{ref}/16 < V_{in} < 8V_{ref}/16$	0111
9	Q	YES	$8V_{ref}/16 < V_{in} < 9V_{ref}/16$	1000
10	R	NO	$9V_{ref}/16 < V_{in} < 10V_{ref}/16$	1001
11	S	YES	$10V_{ref}/16 < V_{in} < 11V_{ref}/16$	1010
12	T	NO	$11V_{ref}/16 < V_{in} < 12V_{ref}/16$	1011
13	U	YES	$12V_{ref}/16 < V_{in} < 13V_{ref}/16$	1100
14	V	NO	$13V_{ref}/16 < V_{in} < 14V_{ref}/16$	1101
15	W	YES	$14V_{ref}/16 < V_{in} < 15V_{ref}/16$	1110
16	X	NO	$15V_{ref}/16 < V_{in} < V_{ref}$	1111

condition to give states as I,J,K,L,M,N,O,P,Q,R,S,T,U,V,W,X that depicts the unique sixteen different digitized codes for each state between 0000 to 1111 for the input voltage between 0 to V_r which is represented in Table 4.2.

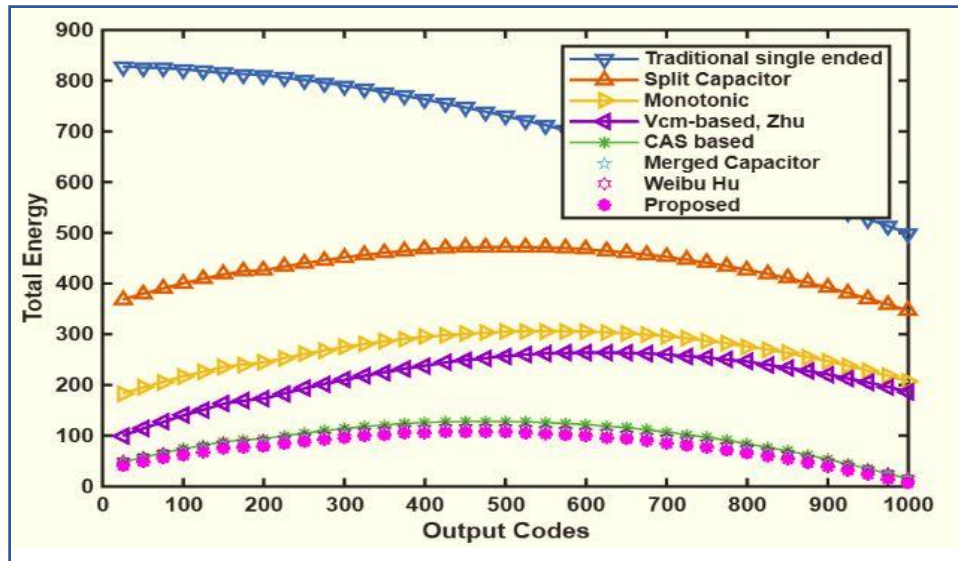


Fig. 4.8 Energy comparison of multiple existing switching methods with proposed switching scheme

The proposed switching scheme incorporating switching logic with zero switching energy in first two MSB comparisons with average switching energy of $57.4 CV_{\text{ref}}^2$ has achieved reasonably reduced switching energy approx. 92 percent compared to conventional switching scheme as shown in Fig. 4.8. Further, the number of capacitors in designed DAC have been reduced 50 percent compared to conventional switching scheme. Also, a single reference voltage utilization of $V_{\text{ref}}/2$ has felicitated reduction of the SAR logic complexity. The design shift from schematic to layout requires proper choice of capacitors to obtain area efficiency and good compatibility with the process technology. In the next section, choice among different available capacitors to be utilized in GPDK 45 nm technology node is discussed.

4.5 CHOICE AMONG DIFFERENT CAPACITORS FOR UTILIZATION IN DAC CAPACITOR ARRAY

Analog integrated circuits (AIC) employ various types of on-chip capacitors, including Metal–Oxide–Semiconductor (MOS), p–n junction, Metal–Insulator–Metal (MIM), Polysilicon–Insulator–Polysilicon (PIP), and Metal–Oxide–Metal (MOM) structures. The choice of capacitor type depends on linearity, area efficiency, matching, and process technology compatibility.

- MOS and p–n junction capacitors exhibit highly non-linear capacitance–voltage (C–V) characteristics. Because of this nonlinearity, they are not suitable for precision applications such as DACs or filters, but are often used in compensation networks, bypass and decoupling circuits, delay elements.
- PIP capacitors provide high capacitance density and excellent matching characteristics. However, they are no longer supported in most advanced semiconductor technologies below 180 nm, due to process complexity and limited compatibility with deep submicron CMOS processes.
- MIM capacitors are widely used in mixed-signal and analog ICs because of their high capacitance density, good linearity, and superior matching. However, they have some limitations • Strict layout rules limit the minimum achievable capacitance (typically a few to tens of femtofarads) • Additional process steps are required, including dedicated metal layers and high dielectrics • Not all CMOS process technologies support MIM fabrication layers, which can constrain design portability.

From the state of the art, MIM capacitors are generally preferred in analog and mixed-signal IC design because they provide larger on-chip capacitance values with good linearity and

matching characteristics. Conversely, MOM capacitors are well suited for small capacitance applications (in the femtofarad or sub-femtofarad range), offering adequate matching performance and low parasitic coupling. Typically, in GPDK 45 nm process technology, MOM structures are available in both symmetric and asymmetric configurations. Metal Oxide Metal (MOM) capacitors utilize the electrostatic coupling between adjacent metal interconnects created through standard CMOS metallization processes. The coupling primarily occurs between lateral metal lines, where the electric field is confined within the inter-metal dielectric. This lateral field coupling is preferred over vertical coupling since lateral geometries such as line width and spacing can be controlled more precisely during fabrication compared to the variations in metal and dielectric thicknesses.

In symmetric MOM capacitors, the two terminals are mirrored with respect to each other, and the number of fingers per metal layer is kept even to maintain symmetry. In asymmetric MOM capacitors, the bottom terminal is connected to Metal-1 (M1), which acts as an electrostatic shield for the top terminal from the substrate similar in behavior to a conventional planar MIM capacitor. The number of fingers per metal layer in asymmetric MOM structures is therefore odd. To minimize external parasitic coupling effects, a guard ring (ground ring) is placed around the MOM capacitor structure. This improves isolation and enhances the capacitor's overall stability in high-frequency and precision analog designs. Further, Sampling of data incorporated in a switching scheme takes place with the inclusion of switches in which sample and hold circuit consumes approx. 6 % to 8 % of total power consumption of an ADC. Sample and hold switch must incorporate the low power logic to perform switching with reduced power consumption and better linearity. The circuit of low power sample and hold circuit designed for low power DAC design is discussed in the next section.

4.6 ARCHITECTURAL DESIGN OF SAMPLE AND HOLD CIRCUIT

In successive approximation register (SAR) analog-to-digital converters (ADCs), the sample and hold (S/H) circuit, integrated with the capacitive digital-to-analog converter (CDAC) array, serves as the interface between the analog input and the digital conversion process. Its primary function is to accurately capture and maintain the instantaneous value of the input signal during the bit-by-bit comparison phases of the SAR operation. Fig. 4.9 depicts the proposed S/H circuit. The MOSFET transistors $M_{n1,2}$, $M_{p1,2}$, function as toggles and maintain the sampled voltage in the offset capacitance C_{offset} throughout the hold stage (i.e clk becomes 0) . Also, adjustment of the gate to source voltage (V_{GS}) of the primary switching device M_{nSW}

throughout the sampling or tracking stage (clk equals 1) will take place. When the source voltage of the transistor MnSW changes, the enormous value V_{GS} guarantees that it is entirely ON and remains significantly larger than the value of the threshold voltage V_{th} .

Fig. 4.9 Architecture of designed sample and hold circuit

MnSW gate node as well as Mp2 gate node have a common connection as Vg & Mp2's sources are kept at V_{DD} throughout sampling. To be entirely off, Mp2's gate needs to be connected to the most significant value in the entire circuit, which is Vg. In the hold stage, Mn4 couples Vg to the minimum value in the circuit to guarantee that MnSW is completely turned off. Whenever Mn4 is turned off, Mn3 is given to keep it from getting an extremely high V_{GD} . Transistor Mn3's gate voltage is maintained as V_{DD} , Mn3 will not function as an efficient pass device, therefore Mn4's drain will have to be restricted to a max value $V_{DD}-V_{th}$ throughout the sampling procedure, but at the cost of a wider area. Mn1 and Mn2 use two opposing clocks (clk and clk_b), the clock feedthrough impact is balanced out when MpSW is introduced in parallel to MnSW. During the sampling phase, all bottom plates of the CDAC capacitors are connected to the analog input voltage through the sampling switch, while the top plate is typically held at the common-mode potential. The switch remains closed long enough to ensure the CDAC array fully charges to the input potential. Once the sampling is complete, the hold phase begins by

opening the sampling switch, thereby isolating the CDAC array and preserving the sampled charge. The SAR logic then performs binary search operations by successively switching capacitor bottom plates between the reference voltage and ground.

4.7 SUMMARY OF THE IMPORTANT RESULTS FOR THE PROPOSED DAC

Design of an energy-efficient, low-area, and high-linearity DAC remains a key factor in improving the overall performance of SAR ADCs. Based on designed DAC unit, the single ended and differential SAR ADC architectures became two prominently available designs incorporating SAR logic. Single ended SAR ADC is best utilized for the applications requiring low power consumption as major constraint compared to high SNR while differential architecture is preferred for high acceptable SNR in the digitized output. In this work, single ended DAC architecture with dummy DAC at the positive input of comparator is proposed and following results are obtained:

1. Proposed switching scheme utilize single reference voltage of $V_{\text{ref}}/2$ and perform first two MSB comparisons with zero switching energy.
2. Proposed scheme required average of $57.4 CV_{\text{ref}}^2$ of switching energy which is much reduced value approximately reduced by 92 percent compared to conventional capacitor-based switching scheme.
3. Compared to conventional switching scheme, number of capacitors in the DAC array have been reduced by 50 percent. Proposed DAC unit consists of $2 \times 2^{N-1} C = 2^N C$ total capacitance value.
4. In proposed switching scheme, a single ended behaviour is obtained utilizing a dummy DAC at the positive input of comparator. The first comparison is performed without any switching power. Also, after first comparison of V_{in} with $V_{\text{ref}}/2$, the bottom plate of dummy DAC is switched either to ground or $V_{\text{ref}}/2$ and will remain at that state till the final digitization is performed with $V_{\text{ref}} = 1.1 V$.
5. MOM capacitors will be the preferred choice to shift the design from schematic to final back-end stage.
6. From second iteration before N-1 stage, the capacitor voltage follows the $V_{c+} = V_{c+} - \frac{V_r}{(-1)^{d_{N-K}2^{K+1}}}$ and $V_{c-} = V_{c-}$.
7. After, N-1 iteration, $V_{c-} = V_{c-} - V_r(-1)^{d_N - K2^K}$ and $V_{c+} = V_{c+}$, capacitor voltage is followed in the switching scheme to create comparison voltages in the digitization process.

8. Low power sample and hold circuit with transistors $M_{n1,2}$, $M_{p1,2}$ that function as toggles switches and maintain the sampled voltage in the offset capacitance C_{offset} throughout the hold stage (i.e clk becomes 0) are utilized. Also, adjustment of the gate to source voltage (V_{GS}) of the primary switching device M_{nSW} throughout the sampling or tracking stage (clk equals 1) will take place to avoid leakage power.

It can be concluded that the digital-to-analog converter (DAC) is the most power-hungry block in a SAR ADC, accounting for approximately 60% of the total power consumption. Therefore, the design of an energy-efficient capacitor switching scheme plays a crucial role in improving the overall performance of SAR ADCs in terms of power consumption, linearity, and silicon area. Based on the DAC configuration, single-ended and differential SAR ADC architectures have emerged as the two most widely adopted design approaches incorporating SAR logic, as reported in the literature. Single ended SAR ADC is best utilized for the applications requiring low power consumption as major constraint compared to high SNR while differential architecture is preferred for high acceptable SNR in the digitized output. Proposed switching scheme utilize single reference voltage of $V_{ref}/2$ and perform first two MSB comparisons with zero switching energy. The scheme required average of $57.4 CV_{ref}^2$ of switching energy which is much reduced value approximately reduced by 92 percent compared to conventional capacitor-based switching scheme. Compared to conventional switching scheme, number of capacitors in the DAC array have been reduced by 50 percent as the DAC unit consists of $2 \times 2^{N-1} C = 2^N C$ total capacitance value. Finally, the proposed scheme is switching the voltage levels as per the required resolution of ADC and limiting the non-linearities within the acceptable range.

CHAPTER 5

DESIGN OF IMPROVED CONTROL UNIT FOR SAR ADC

5.1 BRIEF INTRODUCTION ABOUT CHAPTER

SAR logic unit often termed as control unit is one of the important modules in the design of SAR ADC. The Successive Approximation Register (SAR) logical control unit plays a pivotal role in determining the performance, efficiency, and robustness of SAR analog-to-digital converters (ADCs). Initial analysis emphasized the SAR logic-based control unit primarily as a binary search controller that sequentially resolves each bit from the most significant bit (MSB) to the least significant bit (LSB) using comparator feedback [141]. However, recent advancements have shown that the design of SAR logic significantly influences timing behavior, switching energy, and tolerance to analog imperfections. Based on the comparator output the control unit has to switch the DAC bottom plate state between $V_r/2$ where V_r is the reference voltage and ground so as to achieve the proper in between comparison voltage in the process of digitization of an analog sampled signal [142].

Further, there exists multiple control unit designs like counter based, shift register based, and SAR logic based on internal clock signal generations. The conversion speed, proper timing synchronization and error robustness are the key requirements from a SAR logic-based control unit and the classical binary search remains dominant for its simplicity; however, non-binary and redundant SAR logic architectures have been introduced to mitigate the impact of incomplete DAC settling and comparator metastability. The literature further highlights the necessity of SAR logical control unit and DAC co-optimization, especially when advanced switching techniques such as monotonic, common-mode (V_{CM})-based, and capacitor-splitting schemes are employed for switching. Based on the above requirement to design a SAR logic-based control unit with better DAC and logical unit synchronization to further reduce nonlinearity in form of reduced INL and DNL in designed SAR ADC gives the way to form third objective as:

Characteristic Analysis of Low power D flip flop and multiplexer modules to design an improved control unit for SAR ADC

The methodology used to achieve desired objectives involved following steps: -

- Design of low power D flip flops and multiplexer modules in CADENCE Virtuoso 45 nm technology node.
- Utilization of the designed D flip flop and multiplexer modules in the designing of SAR logic-based control unit.
- Proper timing synchronization between multiple stages of control unit to get proper timing order with comparator output.

This chapter includes the design of SAR logic-based unit with better DAC-control unit synchronization to reduce non linearities with reduced power consumption at sampling rate of 540 KS/s. Modern research trends view SAR logic not merely as a digital binary controller but as an integral component co-designed with comparator and DAC to design a low power analog to digital converter. So, the designing process of control unit includes designing of enhanced D flip flops with improved set up/hold time constraints, clock and internal clock signals for better timing synchronization, multiplexer, sampling logic as the beginning step and SAR logic generation bitwise to implement the proposed switching scheme control unit is presented in this chapter. Finally, based on enhanced D flip flops and multiplexers with proper timing synchronization, an improved control unit for utilization in SAR ADC and to implement proposed switching scheme is designed in this chapter.

The present chapter is divided into 5 sections, starting with a brief chapter introduction as first section 5.1. In section 5.2, overview of synchronous and asynchronous SAR Logic based control units is focussed. Further, in section 5.3, Enhanced type D flip flop circuit and timing clock signals of control unit is focussed. Section 5.4 includes sampling phase & bitwise control signal generation in the proposed control unit. Finally, all the important outcomes are summarized in the conclusion section as 5.5.

5.2 OVERVIEW OF SYNCHRONOUS AND ASYNCHRONOUS SAR LOGIC BASED CONTROL UNITS

Traditional SAR ADCs employ synchronous SAR logic, wherein bit decisions are governed by a global clock. This method offers deterministic timing and ease of digital integration but often results in conservative clock periods to accommodate worst-case comparator delays [143]. To overcome this limitation, researchers have explored asynchronous or self-timed SAR logic, which eliminates dependence on a fixed clock and progresses through bit decisions using handshake signals between the comparator and register. Asynchronous approaches demonstrate superior power efficiency and adaptability to variable sampling rates, making them suitable for

low-power and biomedical applications [144]. In addition to timing strategies, the evolution of search algorithms within the SAR logic has played a critical role in improving conversion speed and error robustness. Several recent studies focus on minimizing digital activity within the SAR logic to enhance overall energy efficiency. Techniques such as clock-gated dynamic SAR registers, compact finite state machines (FSMs), and event-driven logic structures have been reported to reduce unnecessary switching and glitch power [104]. These methods, combined with asynchronous control, have enabled high-resolution SAR ADCs to meet stringent power constraints in portable and implantable systems. Further, asynchronous control logic has traditionally been utilised to attain high speed, as referenced in sources [144]. Regrettably, the comparison circles generated by the propagation of internal logical signals exhibit a significant reliance on variations in process, voltage, and temperature (PVT). A brief comparative study of synchronous and asynchronous SAR logic units along with utilisation of synchronous control system logic is presented in Table 5.1.

Table 5.1: Comparative study of synchronous and asynchronous SAR logic units

S.No.	Feature	Synchronous SAR	Asynchronous SAR
1	Control Type	Clock-based	Self-timed (event-driven)
2	Clock Dependency	Requires clock	No global clock
3	Speed	Limited by clock period	Faster (depends on comparator delay)
4	Power Consumption	Higher	Lower
5	Design Complexity	Simple FSM	Complex handshaking logic
6	Timing Robustness	Easy to verify	Sensitive to delay mismatches
7	Best Use	Moderate speed, simple systems	High speed, energy-efficient ADCs

The control logic operates synchronously to produce output codes that encompass switching control signals for the digital-to-analog converter (DAC). The Fig. 5.1 depicts a synchronous SAR logic-based control unit. The control signals are generated based on the comparison outcome, clk and sample which serve as the inputs to the system. The SAR logic has been developed to provide digital code to DAC depending on the output of the comparator. It is made up of digital cells that execute a binary search algorithm that produces the ADC output

alongside the end of conversion (EOC) output at the end of the process [145]. Shift registers, as well as a combinational switch, are the primary components of the control unit.

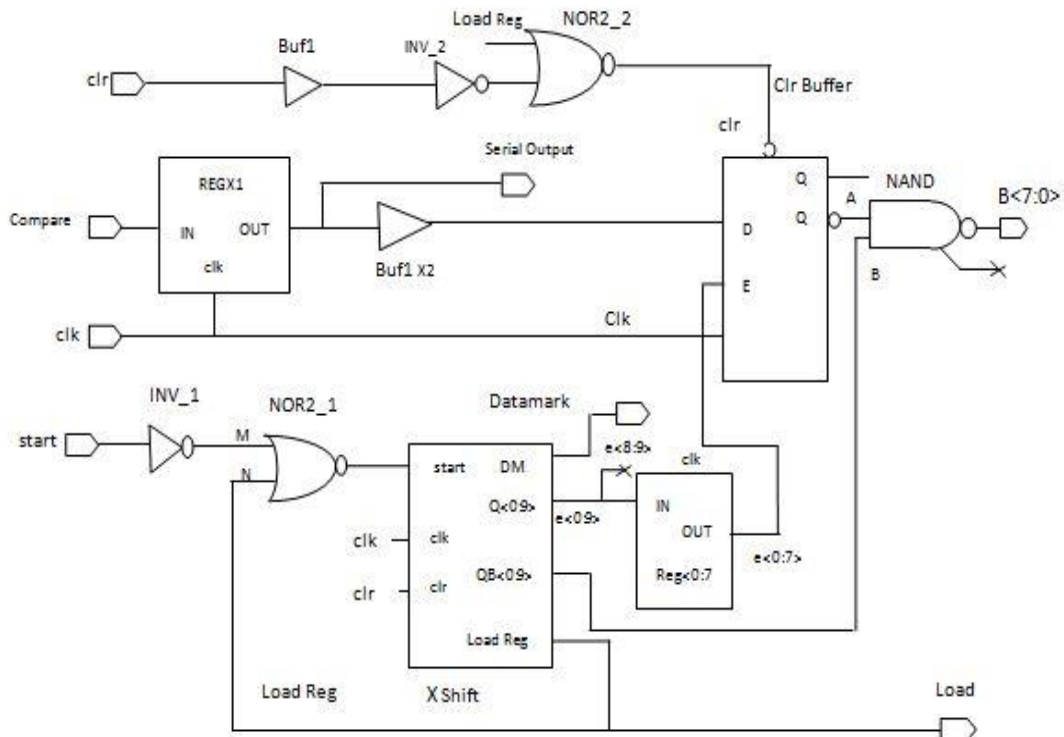


Fig. 5.1 Synchronous SAR logic-based control unit

The latch serves to record the comparator's decisions, the combinational switch serves as a source of the control signals needed for the differentiating DAC, and the shift register is employed to generate pulses. So, it is worth mention that the speed of synchronous SAR logic-based control unit is moderate with moderate to high power consumption and facilitates a lower complex circuit. On the other hand, the speed of asynchronous control units is high and power consumption is low, but their complexity is very high. Also, it is mentioned that verification of any error in asynchronous control units is very complex compared to synchronous units. Keeping in view of easy verification of any timing error and good timing synchronization with comparator and DAC at moderate power consumption, a synchronous control unit is designed in this project. The Fig. 5.2 also illustrates an 8-bit SAR logic control unit constructed using a chain of D-type flip-flops (FFs) and combinational OR gates, which collectively form the successive approximation register (SAR) block of the ADC. The SAR logic operates in synchronization with a global clock and receives signals from the comparator (Comp) and shift/enable input.

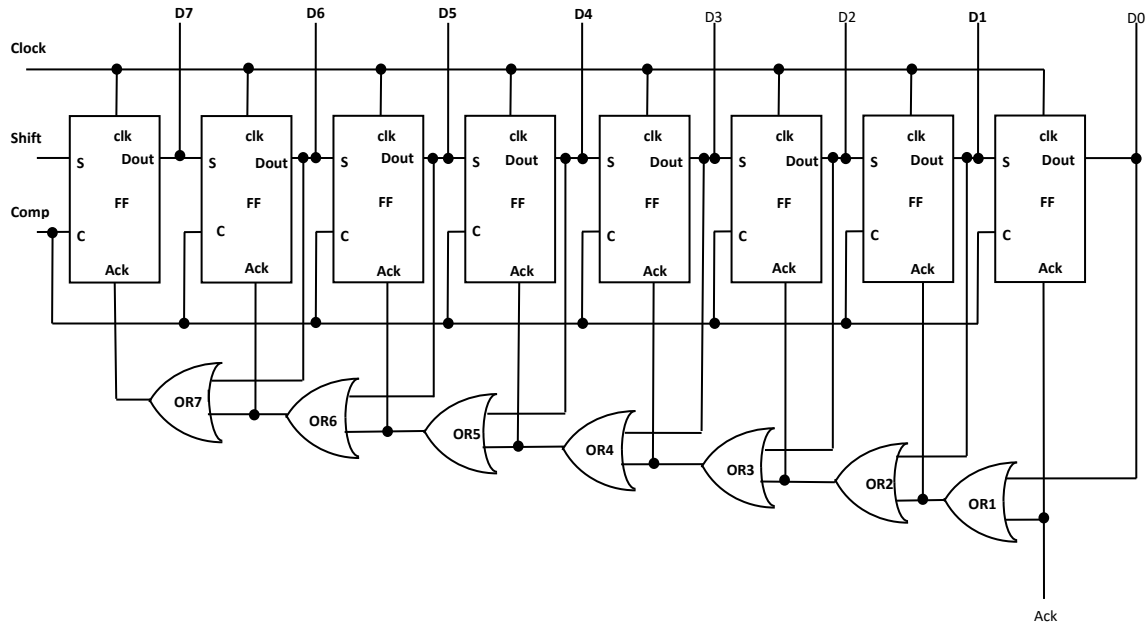


Fig. 5.2 Synchronous SAR logic utilizing D flip flop and OR Gate

Each flip-flop stage (D0–D7) corresponds to a specific bit of the digital output. The shift input governs the bit progression through the flip-flop chain, while the comparator output determines whether the corresponding bit should be set or cleared during the conversion process. The OR gates (OR1–OR8) are cascaded to propagate the decision signal through each bit stage, enabling the sequential approximation process from the most significant bit (MSB) to the least significant bit (LSB). During operation, the SAR logic begins by setting the MSB flip-flop high, and based on the comparator's feedback, it either retains or resets the bit before proceeding to the next lower bit. This iterative process continues until all bits are resolved, thereby completing one full conversion cycle. The Ack (Acknowledge) output signal indicates the completion of the conversion and triggers data readout or digital output transfer. This architecture exemplifies a synchronous SAR control logic, offering a compact and systematic structure with predictable timing behavior, making it suitable for medium- to high-resolution SAR ADCs. Further, as a mandatory requirement for the control unit, a low power D flip flop is hereby considered to be designed in the next section 5.3.

5.3 ENHANCED D FLIP FLOP CIRCUIT AND TIMING CLOCK SIGNALS OF CONTROL UNIT

In the DFF circuits shown in Fig. 5.3, an Enhanced type DFF logic is considered in the design of flip flop, which highlights the current path in the flip-flop that is needed to charge PM7 and

PM8 mosfet path, and the path of the current needed to discharge A voltage from PM6, when the data changes its value from low to high. It shows that B node is not affected while charging X2 node as there is no signal conditioning presented on B node as shown in Fig. 5.4. This reduces the time needed to charge PM7 and PM8 MOSFET. Also, the waveform, it shows the current drawn from PM2 transistor in order to charge X2, the average current drawn from both PM5 and PM7 transistors when the clock is low, and the current drawn from NM5 transistor when the clock is high.

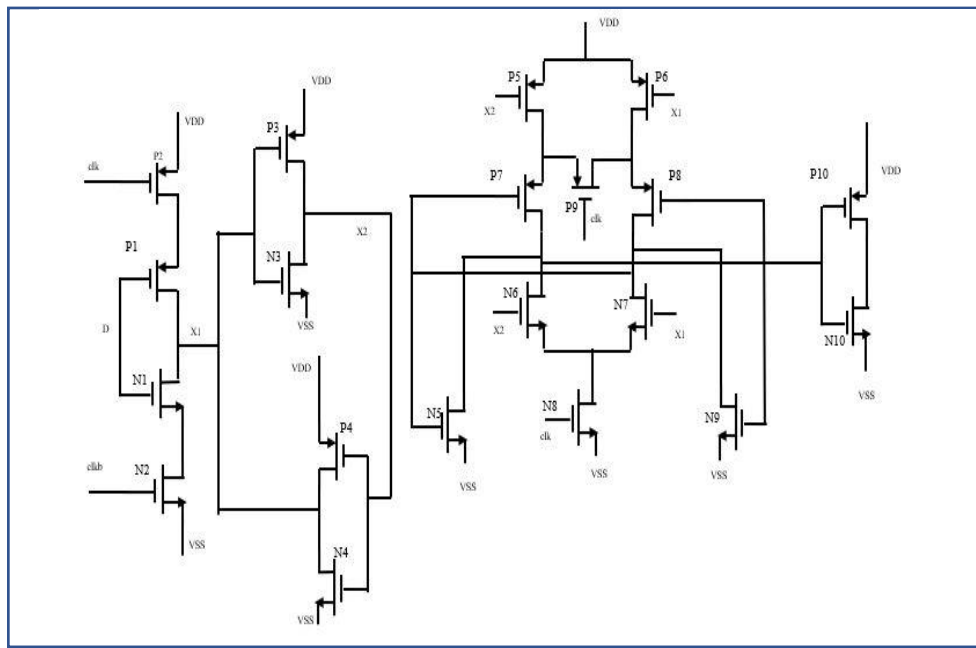


Fig. 5.3 Designed D flip flop circuit for control unit

As a result, the average current being consumed in the slave latch in the proposed design is less than TCFF, because B is not being re-charged while charging PM7 and PM8 path. In EDFFs only active data paths are charged or discharged. Leakage and redundant switching currents are minimized, and speed of node charging/discharging is improved by carefully placing *boosted PMOS/NMOS paths*. The normal D flip flop requires high set up/ hold margin, but the designed enhanced D flip flop is working with improved set up/hold timings. The enhanced D flip-flop offers significant advantages over the conventional design by improving both speed and power efficiency.

Unlike a standard DFF, which consumes energy during every clock transition regardless of data change, the enhanced version activates current paths only when the input data toggles. This selective charging and discharging mechanism minimize unnecessary switching activity, thereby reducing dynamic power consumption. Additionally, optimized transistor paths

provide faster data propagation and stronger noise immunity, resulting in improved stability and timing accuracy. These features make enhanced D flip-flops especially suitable for high-speed and low-power applications such as SAR ADC control logic, where efficient and precise bit decisions are crucial.

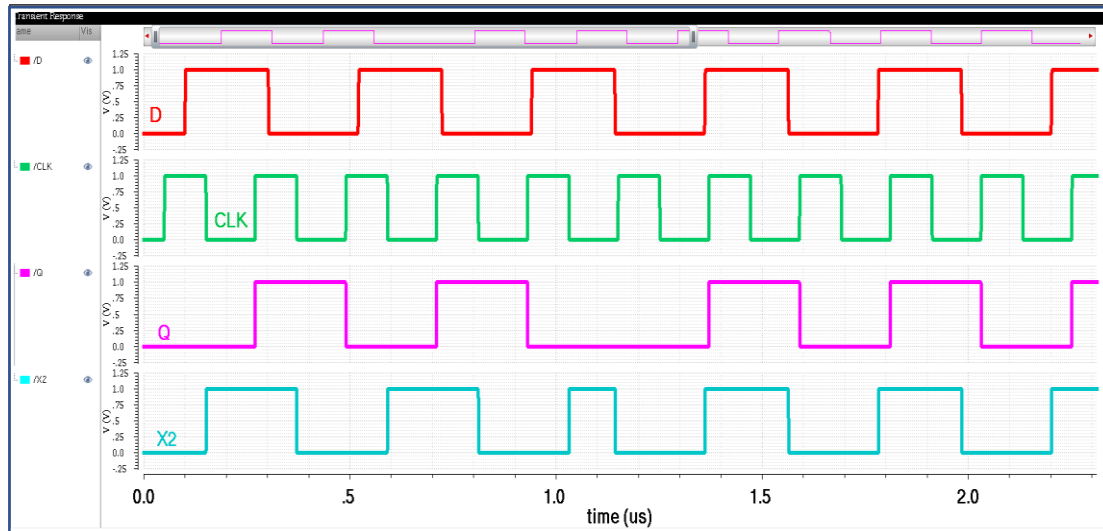


Fig. 5.4 Transient output of Enhanced type D flip flop

Designed control unit is implemented using MOSFET based D flip flops and multiplexers. Logic switching variables are shown in Fig. 5.5 and Fig. 5.6 represents the clock & control signals to realise the SAR logic in implemented control unit. The timing sequence is generated to perform the digitization at sampling rate of 540 KS/s.

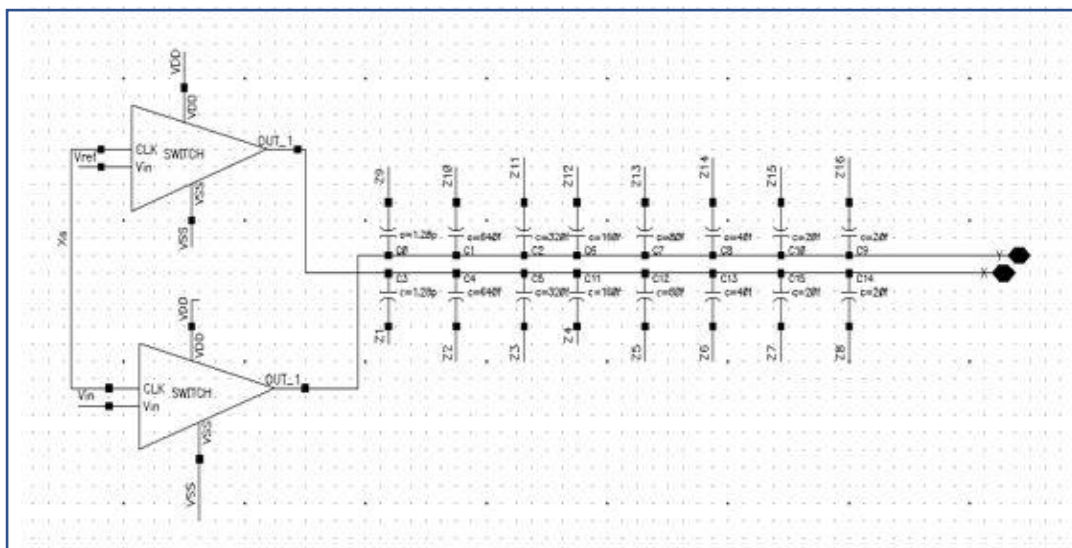


Fig. 5.5 DAC control signals representation in DAC capacitor array

The clk signal is given with a delay of 260 ns and period of 240 ns. Xs signal is turned high at 250 ns so 10 ns is given as time window for sampling of input signal. Further, with the maximum delay of 40 ns as of comparator, the MSB -1 bit is generated by 300 ns.

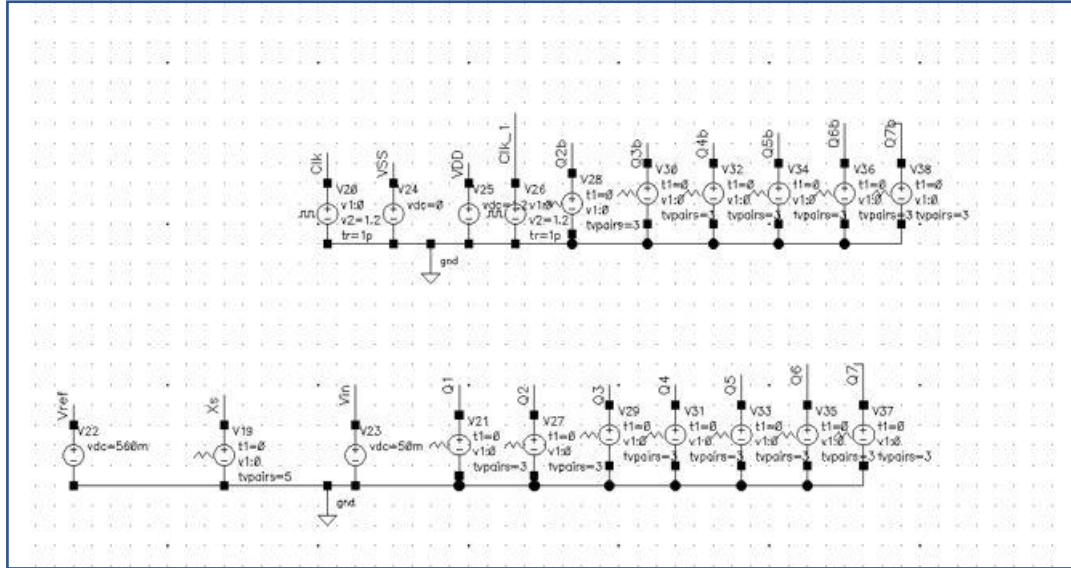


Fig. 5.6 Clock and internal signals utilized for timing synchronization in SAR logic

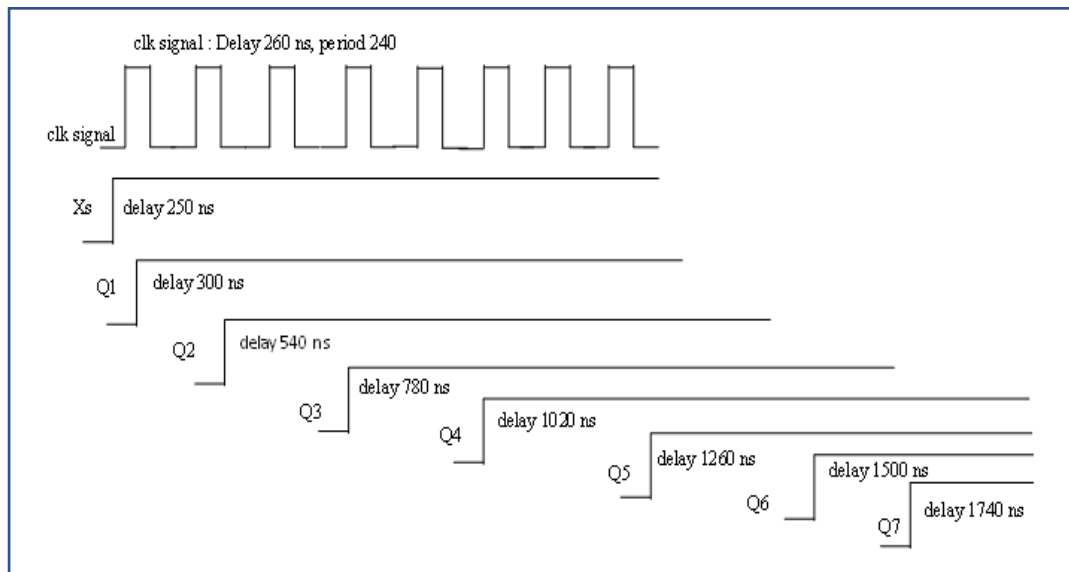


Fig. 5.7 Timing of clock and internal signals utilized in SAR logic

The clk signal along with internal generated clk signals for timing synchronizations is given in Fig. 5.7. Sampling phase begins the digitization process when Xs is low and Dp (comparator output) is the digitized output bit which is generating digital data in synchronization with internal generated clock signals (Q1 to Q7) which is providing better linearity in the digital

data generation process. The control unit is implementing SAR logic bitwise, first internal clock Q1 is providing timing synchronization to MSB-1 bit, just after the sampling on first clk, MSB bit gets generated. Remaining bits are also being generated by the control unit with better timing optimization between DAC and comparator, Q2 is providing timing synchronization to MSB-2 bit and so on. Generated data is stored in shift register and as clk timings, it is fetched as digitized 8-bit output for the designed SAR ADC.

5.4 SAMPLING PHASE AND BITWISE CONTROL SIGNAL GENERATION IN PROPOSED CONTROL UNIT

Positive input DAC array consists of capacitors with bottom plate controlling signals as Z1 to Z8 and negative input of comparator relates to DAC array with bottom plate connections as Z9 to Z16. The sampling phase is carried out in synchronization with signal X_s . When X_s is low, Z1 is switched to ground, Z2 to Z8 switched to $V_{ref}/2$. Similarly, Z9 is switched to ground and Z10 to Z16 is switched to $V_{ref}/2$ as per the switching scheme as shown in Fig. 5.8. When, X_s gets switched to logic high state, the control signals A, B, C H and I, J, L...P will be transferred to Z1, Z2, Z3....Z8 and Z9, Z10, Z11.....Z16 respectively.

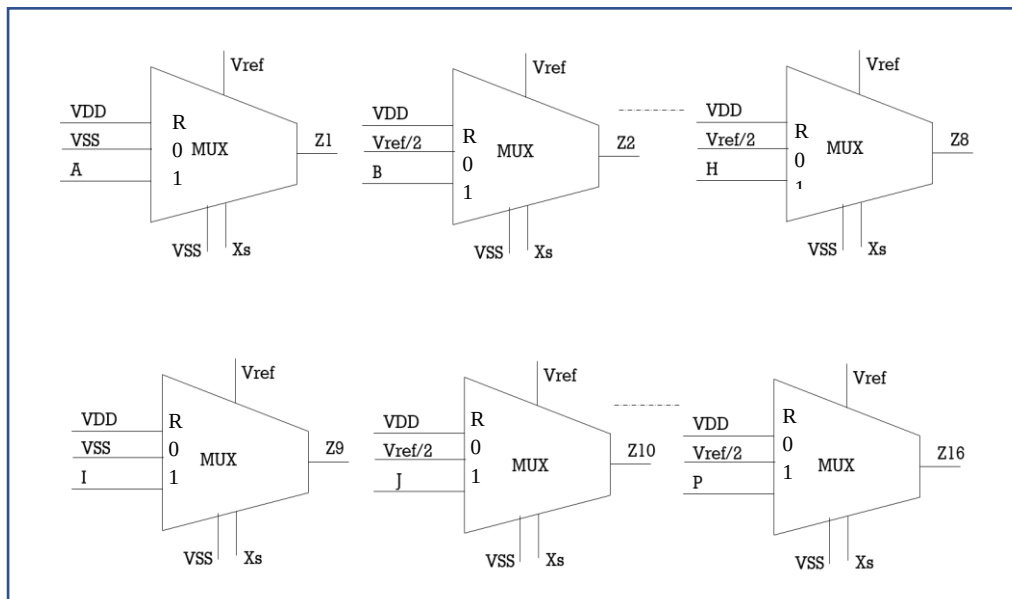


Fig. 5.8 Sampling phase representation in designed control unit

MSB bit D_{n-1} will be generated by direct comparison of $V_{ref}/2$ and V_{in} . After decision of first MSB bit, based on the comparator output D_p , Z1a to Z8a will be either switched to ground or $V_{ref}/2$ as shown in Fig. 5.9.

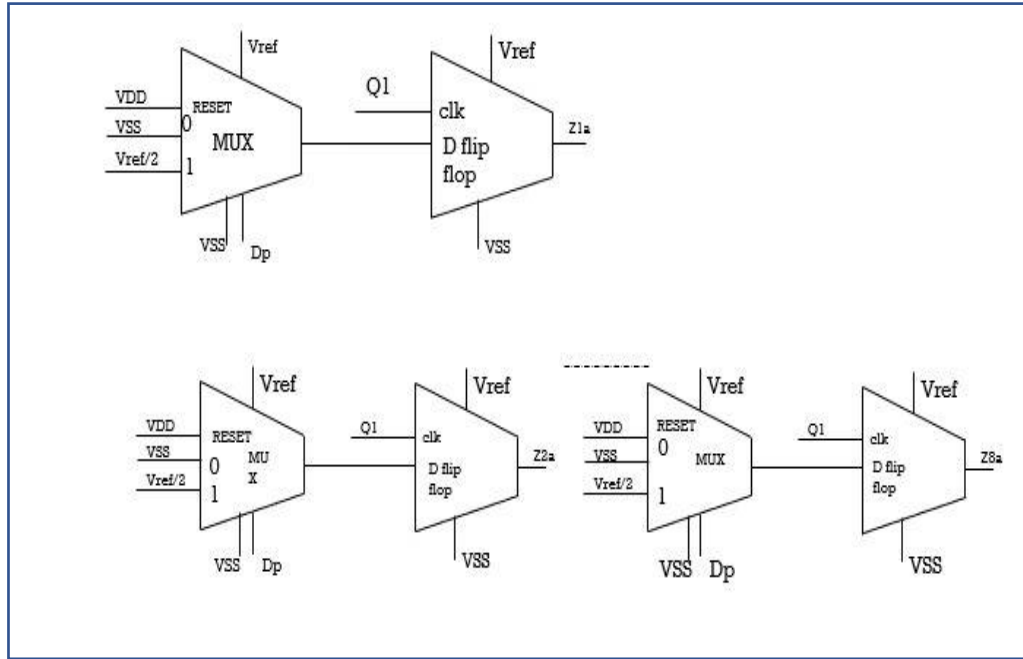


Fig. 5.9 Control signals for second bit generation (Z1a- Z8a) in designed control unit

Irrespective of D_p output, $Z9a$ will be grounded only in this stage and $Z10a$ to $Z16a$ will be at $V_{ref}/2$ as shown in Fig. 5.10. The entire logic is created using D flip flops and multiplexers. The outputs in this stage are observed in synchronization with internal control pulse $Q1$ which is generated with delay of 300 ns. X_s is applied with delay of 250 ns and first clock signal is given with delay of 260 ns.

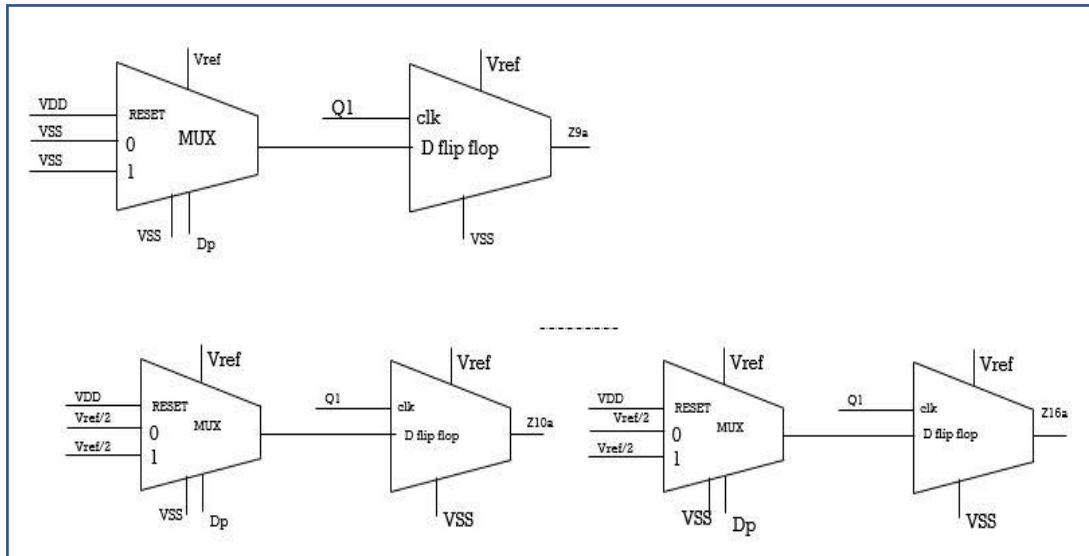
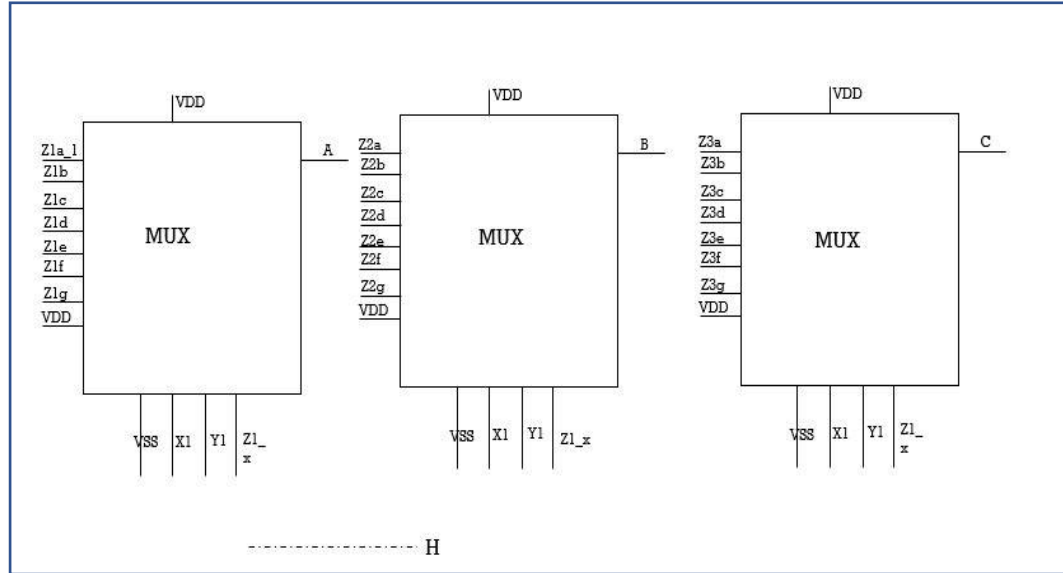


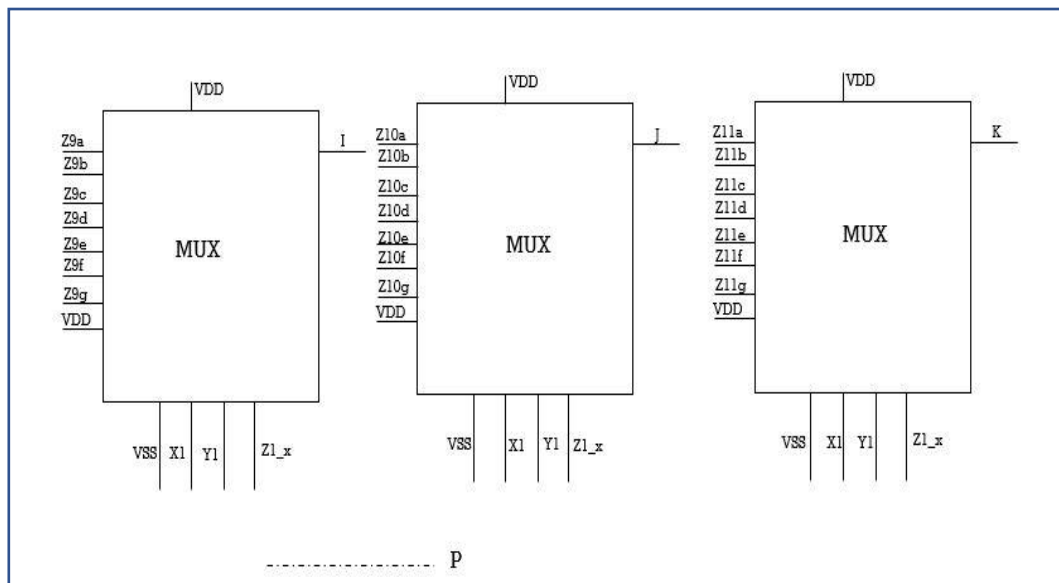
Fig. 5.10 Control signals for second bit generation (Z9a- Z16a) in designed control unit

The created signal at Z terminals in this stage will establish comparison voltage $V_{in} < V_{ref}/4$ or $V_{in} < 3 V_{ref}/4$ at the comparator output to create second bit of digitized output. $Z1a_1$ signal

Finally, Z1a, Z1b, Z1c..., Z1g are multiplexed by control signals X1, Y1 and Z1_x to generate A, similarly Z2a, Z2b, Z2c ..., Z2g are multiplexed to get B. Similarly, we obtain A, B, C, D..., H and I, J, K, L..., P as control signals to implement the switching scheme in design of 8-bit SAR ADC.



(a)



(b)

Fig. 5.13 Multiplexing of bits **(a)** For States A to H and **(b)** For States I to P in SAR logic unit

Digitized output of comparator at multiple instants in synchronization with Q1 to Q7 is multiplexed and taken as output as shown in Fig. 5.13 (a) and (b). The Digitized output is stored in the register and taken at output in proper synchronization. The designed control unit has utilized internal control signals along with external clk signal to implement the entire control

logic. In the proposed D flip-flop (DFF) circuit, an enhanced-type DFF logic is employed, which efficiently defines the current paths responsible for charging and discharging within the flip-flop structure.

Table 5.2: Comparison of proposed SAR control unit with existing SAR logic units

S.No.	Control Unit Architecture	Timing Method	Main Building Blocks	Speed / Throughput	Power Efficiency	Design Complexity
1	Proposed DFF + MUX Synchronous SAR Logic	Fully Clocked (Global Clk)	D-Flip-Flops, OR-Gates, Shift & Ack Logic	Moderate – 1 cycle / bit	Moderate (power from global clk activity)	Simple
2	Asynchronous / Self-Timed SAR Logic [90]	Event-Driven (Comparator Ready Signal)	Handshake Network, C-Elements, Delay Lines	High – adapts to comparator speed	Very High – no global clock toggling	High – complex timing verification
3	Hybrid (Quasi-Asynchronous) SAR Logic [146]	Mixed (Clock + Self-Timed Bit Cycle)	Global Clock Controller, Handshake Logic	High – close to async speed	High – reduced clk switching	Medium
4	Pipelined / SAR-Assisted Pipelined Control [147]	Multi-Stage Timing	Multiple Stage Controllers, Global Sequencer	Very High (>100 MSPS)	Medium – more stages active	High – stage coordination + calibration
5	Redundant / Non-Binary SAR Logic [148]	Clocked + Error Correction	Non-Binary Decoder, Redundant Bits, Correction Logic	Medium – extra cycles for redundancy	Medium	Medium – extra logic
6	Time-Interleaved SAR Control [149]	Multi-Phase Clock	Master Sequencer, Channel Controllers, Phase Generator	Extremely High (GSPS range)	Low–Medium (many channels)	Very High – requires calibration
7	Digital-Assisted SAR Control [150]	Clocked + Calibration Loops	DSP Block, Calibration Logic, Adaptive SAR Reg.	Medium	Medium	High – digital processing included

Specifically, the design emphasizes the charging path associated with the PM7 and PM8 MOSFETs, as well as the discharging path of node A through the PM6 transistor when the input data transitions from a low to a high level. It is inferred from Table 5.2 that inclusion of internal clock signals (Q1 to Q7) along with global clock (clk) in the proposed control unit is providing a simple control unit design with better timing synchronization as compared to other existing designs at moderate power consumption. Also, enhanced D flip flops are avoiding the leakage power to reduce the power consumption of the control unit.

5.5 SUMMARY OF THE IMPORTANT RESULTS

The design of SAR logic-based unit with better DAC-control unit synchronization to reduce non linearities with reduced power consumption at sampling rate of 540 KS/s is carried out. Keeping in view of better timing synchronization at moderate power consumption, synchronous design is considered to design SAR logic control unit. In addition to global clock signal (clk), comparator clock (clkc), seven internal clock signals (Q1 to Q7) are utilized for timing synchronization in the SAR logic control unit including D flip flops and multiplexers. The summary of important results is given below:

1. Enhanced D flip flop is working well for the required bandwidth and resolution of input signal at low power consumption.
2. The proposed synchronous control unit has less complexity and better timing synchronizations due to which all the control signals are getting generated within time constraints.
3. Sampling phase begins the digitization process when X_s is low and D_p (comparator output) is the digitized output bit which is generating digital data in synchronization with internal generated clock signals (Q1 to Q7) which is providing better linearity in the digital data generation process.
4. The control unit is implementing SAR logic bitwise, first internal clock Q1 is providing timing synchronization to MSB-1 bit, just after the sampling on first clkc, MSB bit gets generated.
5. Remaining bits are also being generated by the control unit with better timing optimization between DAC and comparator, Q2 is providing timing synchronization to MSB-2 bit and so on.
6. Generated data is stored in shift register and as clk timings, it is fetched as digitized 8-bit output for the designed SAR ADC.

It is summarized that chapter includes the design of SAR logic-based unit with better DAC-control unit synchronization to reduce non linearities with reduced power consumption at sampling rate of 540 KS/s. The designing process of control unit includes designing of D flip flop, clock and internal signals for timing synchronization, multiplexer, sampling logic creation and SAR logic generation bitwise to implement the proposed switching scheme control unit is included in this chapter. Finally, based on D flip flops and multiplexers with proper synchronization a novel control unit for utilization to implement proposed switching scheme is designed in this chapter. The timing sequence is generated to perform the digitization at sampling rate of 540 KS/s. The clk signal is given with a delay of 260 ns and period of 240 ns. Xs signal is turned high at 250 ns so 10 ns is given as time window for sampling of input signal. Further, with the maximum delay of 40 ns as of comparator, the MSB -1 bit is generated by 300 ns. Also, it is inferred from table 5.2 that inclusion of internal clock signals (Q1 to Q7) along with global clock (clk) in the proposed control unit is providing a simple control unit design with better timing synchronization as compared to other existing designs at moderate power consumption. Enhanced D flip flops are avoiding the leakage power to reduce the power consumption of the control unit.

CHAPTER 6

DESIGN AND ANALYSIS OF ULTRA LOW POWER 8 BIT SAR ADC

6.1 BRIEF INTRODUCTION ABOUT CHAPTER

The Successive Approximation Register (SAR) ADC design is best utilized architecture for medium resolution and medium speed applications. SAR ADC includes comparator, DAC and SAR logic-based control unit. Compared to comparator and control unit, the capacitive DAC unit is major contributor of power-hunger. Designing of low power dynamic comparator, DAC unit with reduced switching energy and SAR logic-based control unit is already included in chapter numbers 3, 4 and 5 respectively. The proper interfacing of designed modules along with proper controlling of common mode voltage V_{cm} is equally important to result the interfaced circuit into an ultra-low power SAR ADC. The minimization of non-linearities in designed SAR ADC like reduced differential non linearity (DNL) and integral non linearity (INL) with low power consumption holds the major design projection from the literature which is required to be accomplished with reduced INL & DNL values in the digitized output. Also, reduced power consumption and proper synchronization between the designed modules i.e comparator, DAC and control unit is highly required from finally designed SAR ADC. Based on that, fourth and final objective is framed as:

Interconnection of all designed modules and performance optimization of proposed ultra-low power SAR ADC unit and its validation for application in biomedical domain

The methodology used to achieve desired objectives involved following steps: -

- Interconnection of all the designed modules of SAR ADC i.e dynamic comparator, DAC and control unit with proper timing synchronizations for sampling rate of 540 KS/s.
- Simulation and analysis of designed SAR ADC in terms of Power, INL, DNL, SNDR at 540 KS/s.
- Comparative analysis of optimized designed SAR ADC with existing circuits on measured parameters.

So, this chapter includes the fourth objective of the project that is interfacing of all the designed modules i.e comparator, DAC and control unit to design an 8-bit ultra -low power SAR ADC

with reduced INL and DNL values along with reduced power consumption at sampling rate of 540 KS/s. Modern research trends view SAR logic not merely as a digital binary controller but as an integral component co-designed with comparator and DAC to result into a desired low power analog to digital converter. In this chapter, ultra-low power 8-bit SAR ADC is proposed with incorporating single reference voltage $V_{r/2}$ using dummy DAC designed along with bootstrap switch at positive input of comparator implemented to give zero switching energy in first two MSB conversions. Also, the implemented switching scheme is incorporated with novel SAR logic in the designed control unit using flip flops and multiplexers to get the better DAC-logic synchronization and reduced power.

The present chapter is divided into 6 sections, starting with brief introduction of chapter as first section 6.1. In second section 6.2, an overview of SAR design is focussed. In third section 6.3, architecture of proposed 8-bit SAR ADC is focussed. Section 6.4 includes comparator and DAC modules for SAR ADC. Section 6.5 includes result and simulation analysis of 8-bit SAR ADC. Finally, all the important outcomes are summarized in the conclusion section 6.6.

6.2 OVERVIEW OF SUCCESSIVE APPROXIMATION REGISTER (SAR) TYPE ADC DESIGN

The Successive approximation register analog-to-digital converter (SAR ADC) is one of the most widely adopted ADC architectures in modern mixed-signal systems due to its excellent balance between speed, accuracy, and power efficiency. It operates on a binary search principle, where the analog input voltage is successively compared with a series of reference voltages generated by an internal digital-to-analog converter (DAC). Through iterative decision-making controlled by the SAR logic unit, each comparison resolves one bit of the digital output, resulting in a compact and energy-efficient conversion process [151]. Unlike high-speed architectures such as flash ADCs, which require a large number of comparators, or high-resolution sigma-delta converters that demand complex filtering, the SAR ADC achieves moderate-to-high resolution with minimal hardware complexity.

A SAR ADC is composed of major subblocks as: comparator, a capacitor-based charge redistribution digital to analog converter and a control logic to implement binary search in conversion of analog sampled value to its digital equivalent. This configuration enables precise voltage quantization while maintaining low static and dynamic power consumption [152]. With continuous scaling of CMOS technologies, SAR ADCs have become the preferred choice for low-power and medium-to-high-resolution applications such as wireless sensor networks,

biomedical instrumentation, portable devices, and data acquisition systems [153-156]. Their ability to adapt to asynchronous and hybrid timing schemes further enhances their energy efficiency and speed. Owing to these advantages, the SAR ADC continues to be a dominant research focus in the design of modern analog and mixed-signal integrated circuits. A complete SAR ADC design consists interfaced comparator, DAC and control unit with proper control of common mode voltage so that each module works in proper synchronization with an objective to digitize the input sampled analog signal at reduced power and non-linearities. Architecture of SAR ADC includes low power dynamic comparator as one of its modules with its resolution in accordance with the output digital bits of ADC. For n bit ADC, resolution is required to be $V_T/2^n - 1$. Further, DAC design requires the utilization of low power switching technique to perform switching with minimum switching energy per conversion step and reduced capacitances. Control unit is designed with an objective to felicitate switching as per the implemented proposed switching scheme with timing synchronization between DAC and comparator. Basic block diagram of SAR ADC is shown in Fig. 6.1. Power consumption of each module i.e comparator, DAC and control logic is important, however reduction of switching energy in capacitor arrays of DAC holds the major importance.

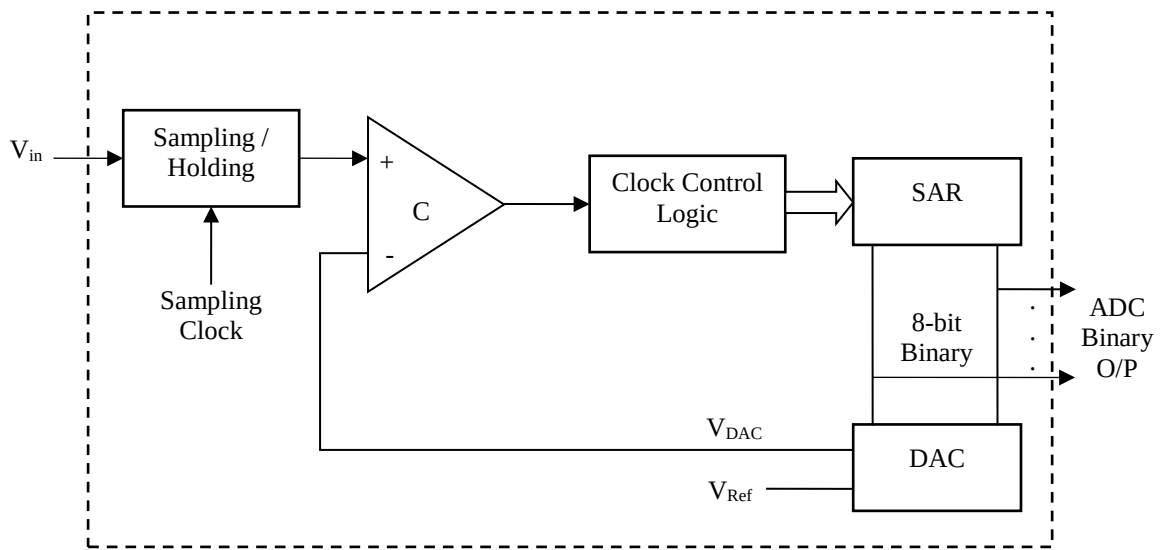


Fig. 6.1 SAR ADC interfaced circuit block diagram

Thus, it is required to reduce the power consumption of each block to design an ultra-low power SAR ADC. SAR core principle resides on binary search algorithm in which a DAC generates the voltage to be compared with input voltage as V_{dac} , control unit configures the DAC based on comparator decision output and comparator makes the decision. Architecture of proposed 8-bit SAR ADC is presented in next section 6.3.

6.3 ARCHITECTURE OF PROPOSED 8-BIT SAR ADC

In the proposed architecture, single ended SAR ADC is proposed with dummy DAC1 at positive input of comparator. Total capacitance is $2 * 2^{N-1} C = 2^N C$ which is 50 percent reduced value compared to [68]. The switching method given in [75] reduced the switching energy by 37.5 % against the conventional architecture. Energy reduction of 56 % achieved in [21] with the implementation of energy reduction procedure in first two comparison cycles. After that, switching energy saving of 81 % was achieved by [69] using monotonic energy reduction procedure. Further, many researchers [85-89] worked to achieve further energy saving in the range of 85 % to 96 % by inclusion of varying reference voltages. However, further energy saving could be done with proper implementation of DAC, comparator, and control unit. Common mode voltage variation at the DAC output in the single ended SAR DAC architecture creates the input voltage variation at the comparator input due to which nonlinearity increases in the ADC output. The present work presents a dummy differential SAR ADC architecture which resembles to single ended SAR ADC but reject the common mode noise to prevent the non-linearity in the DAC output.

Complete 8-bit SAR ADC is designed with the interconnection of all designed modules i.e comparator, capacitive DAC and control logic unit is shown in Fig. 6.2. Each module is designed keeping in view the requirement of 8-bit SAR ADC and the design is implemented with V_{DD} of 1.1 V and resolution of 4 mV. In proposed SAR ADC, the utilized dynamic comparator as proposed dynamic comparator one shown in Fig. 3.4 is working well as per the required resolution requirements. D_p and D_n are two outputs of comparator and DAC unit shown in Fig. 4.5 consists of two capacitor arrays. The DAC1 subarray output is connected at the positive input of comparator and DAC2 subarray output is connected at the negative input of comparator. DAC1 is a dummy capacitor array in the design of proposed switching scheme. Control logic is implemented in synchronization with external clk signal and internal generated control signals Q1 to Q7 and Q2b to Q7b, the switching of Z1 to Z8 along with Z9 to Z16 is controlled.

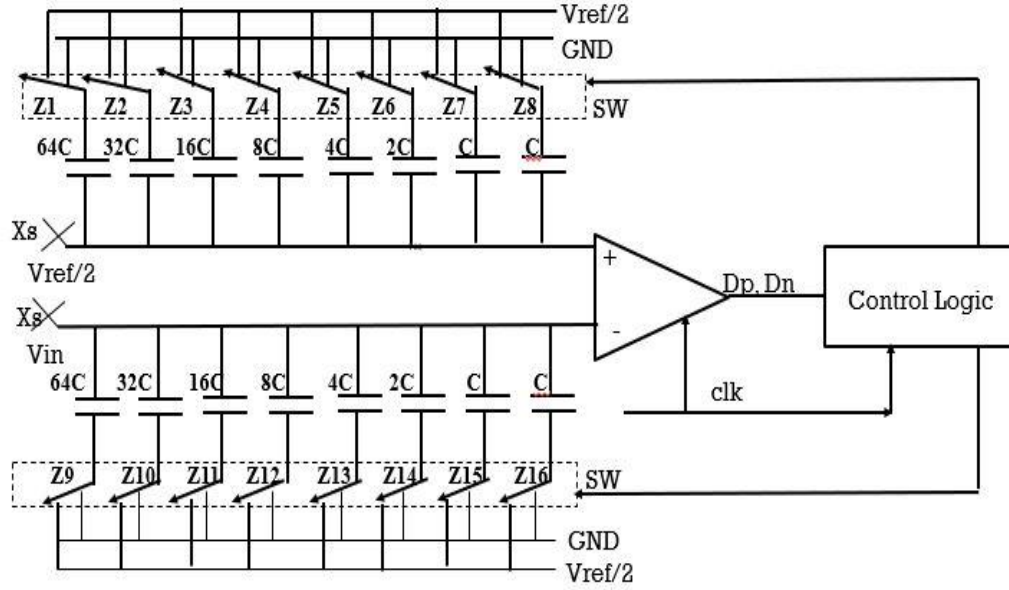


Fig. 6.2 Block diagram of complete interfaced SAR ADC circuit

Proposed DAC unit consists of $2 \times 2^{N-1} C = 2^N C$ total capacitance value as explained in chapter 4. Based on SAR control unit decision, the DAC capacitances are to be switched between ground and $V_r/2$ which in turns creates the switching energy dissipation in the ADC architecture. This work includes a digital to analog converter with a single voltage of $V_r/2$ where V_r is the reference voltage which is taken as 1.2 V in the proposed design. The DAC unit consumes zero switching energy in the first two MSB decisions as per proposed switching algorithm in chapter 4. Initially, $V_r/2$ and V_{in} is sampled onto the capacitances of DAC X and DAC Y respectively. In DAC X in the sampling phase, only MSB capacitance is charged otherwise all remaining capacitances in the DAC X unit are kept uncharged. Similarly, input voltage is sampled completely onto the MSB capacitance of DAC Y and direct comparison of $V_r/2$ with V_{in} is evaluated in the first comparison cycle with no switching energy required in MSB bit decision. Flow chart of implemented switching scheme is given in Fig. 4.4.

Similarly, after MSB bit generation, switching energy dissipation in next bit generation is zero as per the proposed switching logic. Flow chart depicts that initially, sampling of input is carried out by implemented DAC module at the negative end of as $V_{c+} = V_r/2$, $V_{c-} = V_{in}$, after that conversion process gets started with variable K value as 1. In the first stage when $K=1$, $V_r/2 > V_{in}$ is directly compared by the comparator. After comparison out, d_{N-1} bit will be either 0 or 1. Further, $K>2$ condition will be checked, and further switching will take place. The lower plates of DAC X capacitors and DAC Y capacitors will be switched to either ground or $V_r/2$ depending upon the output of $V_r/2 > V_{in}$ as shown in implemented switching scheme Fig. 4.5.

If $V_{r/2} > V_{in}$ condition gets true, then lower plates of DAC X will be switched to ground otherwise lower plate of DAC X will be switched to $V_{r/2}$. A brief view of individual modules in proposed SAR ADC is given in next section 6.4.

6.4 DYNAMIC COMPARATOR AND DAC MODULE UTILIZED IN DESIGN OF PROPOSED SAR ADC

Dynamic comparator is one of the modules in the design of ultra-low power SAR ADC. Proposed dynamic comparator given in chapter 3 as Fig. 3.7 is utilized in the final interfaced design of ultra-low power SAR ADC. The primary advantage of the proposed comparator architecture lies in its simplified control mechanism, which requires only a single regulating clock signal which eliminates the need for synchronization among multiple control signals, thereby enhancing the circuit's overall operational efficiency. Furthermore, the proposed design achieves significant reductions in both delay and power consumption. The use of a compact tail transistor ensures a lower tail current for the differential input stage, optimizing power usage without compromising performance. As the configuration does not require additional transistors for resetting or reconfiguring the circuit, structural complexity is minimized. Consequently, the comparator demonstrates reliable operation, accurately resolving even a minimal input voltage difference of 2.5 mV between the compared signals. The transient output of proposed dynamic comparator showing transition of output nodes Dp and Dn is given in Fig. 6.3 and output transient power for the proposed comparator is depicted in Fig. 6.4. The transient behaviour is depicted for input condition of $inn > inp$, under this condition precharged node outn will be discharged to ground and precharged outp will initially tend to discharge but later pulled back again to high state. The next module i.e digital to analog converter (DAC) utilized in designed SAR ADC is discussed further. Proposed DAC switching scheme presented in chapter 4 as shown in Fig. 4.5 is utilized in the design of 8-bit SAR ADC.

The proposed DAC unit is designed with a total capacitance of $2 \times 2^{N-1}C = 2^N C$ times, where N represents the ADC resolution. Based on the decisions generated by the SAR control logic, the DAC capacitors are alternately switched between ground and $V_{r/2}$ resulting in energy dissipation during the bit transition phases. In this work, a digital-to-analog converter employing a single reference voltage of $V_{r/2}$ is implemented, where $V_r = 1.2$ V serves as the design reference.

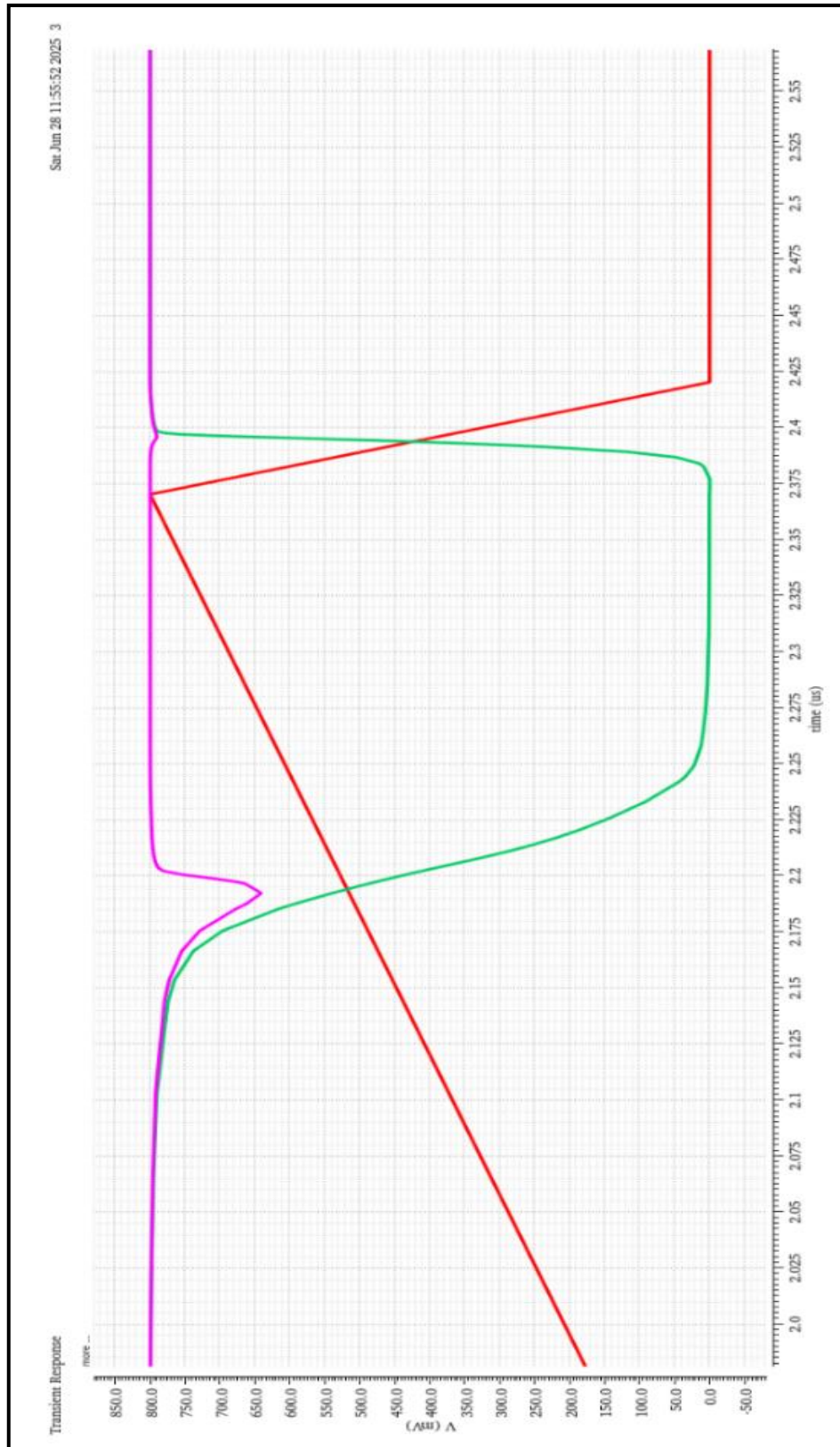


Fig. 6.3 Transient output of first proposed dynamic comparator

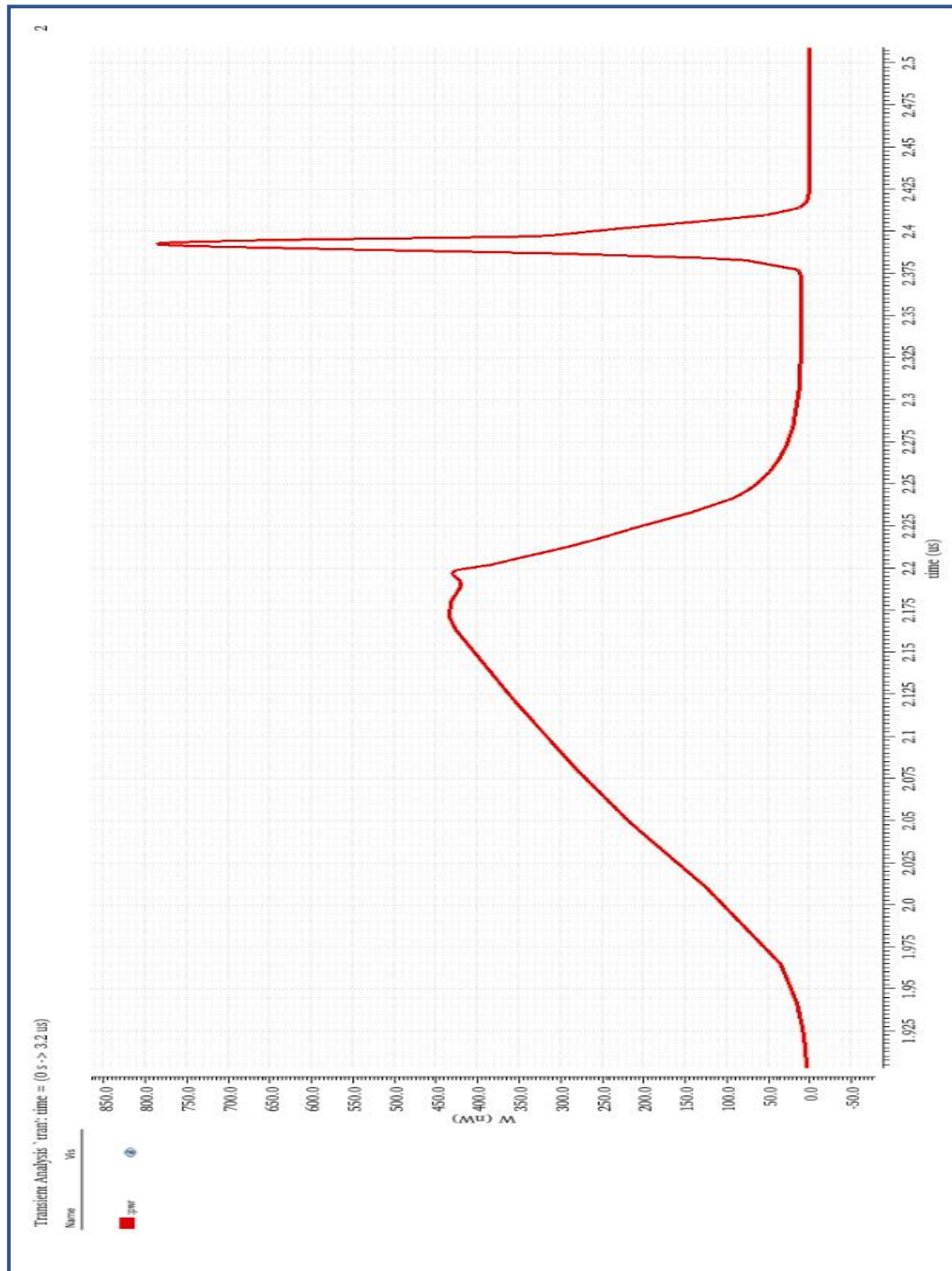


Fig. 6.4 Transient power graph of proposed comparator

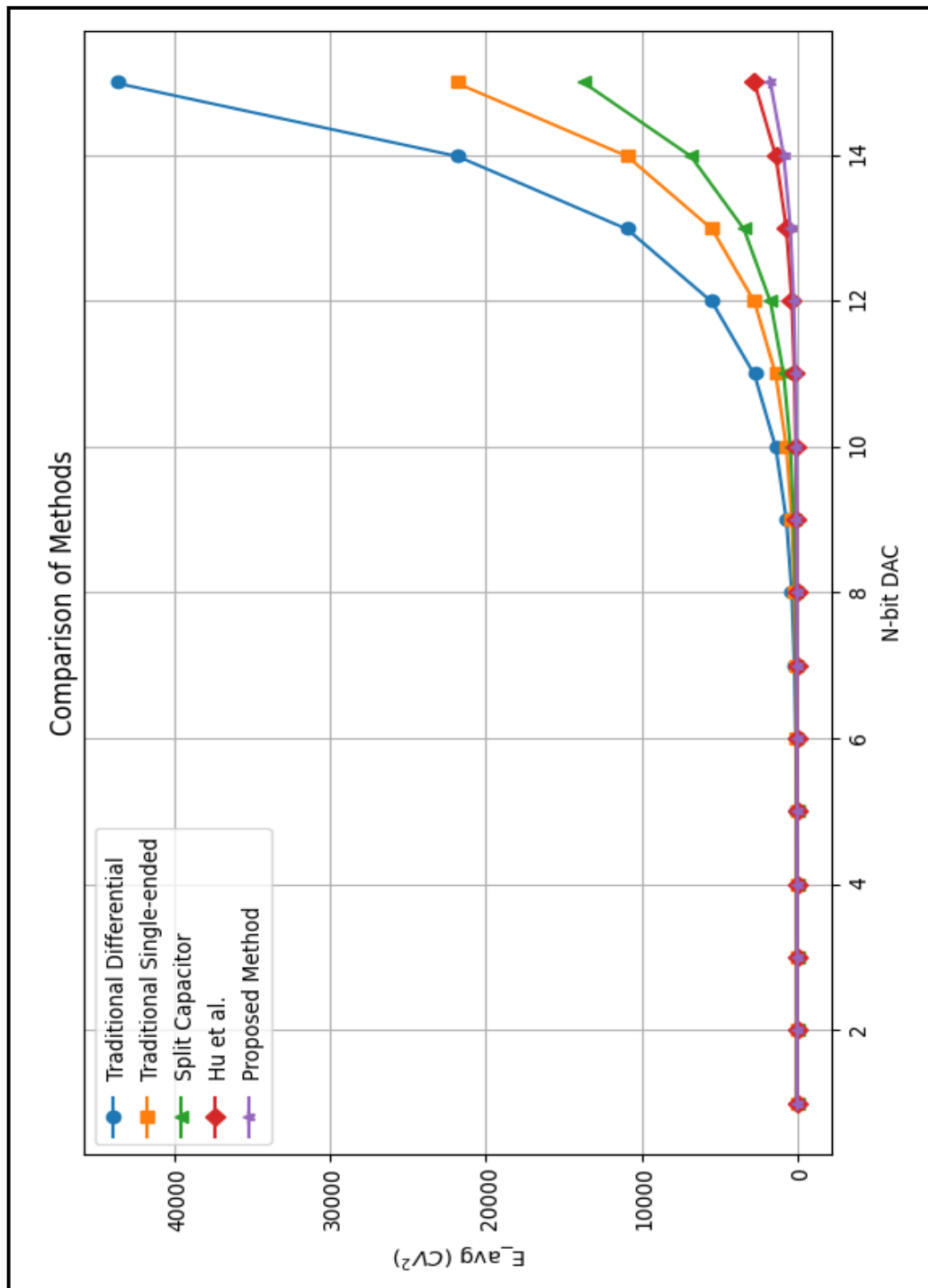


Fig. 6.5 Comparison of proposed switching scheme with existing schemes

The proposed DAC configuration achieves zero switching energy consumption during the first two most significant bit (MSB) decisions by utilizing an optimized switching algorithm. The proposed switching scheme achieves an energy saving of approximately 92% compared to the conventional approach as shown in Fig. 6.5. Additionally, the capacitor count in the designed DAC is reduced by nearly 50% relative to the traditional switching scheme. During the sampling phase, the reference voltage $V_r/2$ and the input voltage V_{in} are sampled onto the capacitors of DAC X and DAC Y, respectively. In DAC X, only the MSB capacitor is charged, while the remaining capacitors remain uncharged. Similarly, in DAC Y, the entire input voltage is sampled onto its MSB capacitor. Consequently, the initial comparison between $V_r/2$ and V_{in} occurs without any switching activity, resulting in a zero-energy transition during the MSB bit decision.

In subsequent conversion stages, when the condition $V_r/2 > V_{in}$ holds true, the lower plates of DAC X capacitors are switched to ground; otherwise, they are switched to $V_r/2$ thereby initiating stage 2 of the conversion process. In this switching approach, $V_r/2$ is sampled as V_{c+} onto the top plates of the DAC X capacitors, where only the MSB capacitor ($4C$) is charged, and the remaining capacitors remain uncharged. Likewise, in DAC Y, V_{in} is sampled onto its MSB capacitor ($4C$). The “Yes” state in this switching scheme evaluates the condition $V_r/4 > V_{in}$ while the “No” state corresponds to $3V_r/4 > V_{in}$. As the conversion progresses to the third stage, multiple comparison conditions are evaluated, including $2V_r/16 > V_{in}$, $6V_r/16 > V_{in}$, $20V_r/16 > V_{in}$, and $14V_r/16 > V_{in}$. These conditions correspond to different switching stages labelled A–H, as illustrated in Fig.4.6 (a)–(f) and Fig. 4.7 in chapter 4. In this manner, the proposed scheme effectively governs the successive switching operations throughout the conversion process.

Further, the next module in designed SAR ADC is SAR logic-based control unit. the designing process of control unit includes designing of enhanced D flip flops with improved set up/hold time constraints, clock and internal clock signals for better timing synchronization, multiplexer, sampling logic as the beginning step and SAR logic generation bitwise to implement the proposed switching scheme control unit is presented in this chapter. The D flip-flop (DFF) as shown in Fig. 5.3 in the proposed design incorporates an enhanced logic mechanism that emphasizes efficient current flow during switching operations. Specifically, the circuit highlights the current paths responsible for charging the PM7 and PM8 transistors and discharging node A through PM6 when the input transitions from a low to high logic state. As illustrated in Fig. 5.3, node B remains unaffected during the charging of node X2, as no signal

conditioning occurs at this node. This functional isolation minimizes unnecessary charging activity and reduces the time required to charge the PM7 and PM8 branches. The corresponding current waveform demonstrates the current drawn from PM2 to charge node X2, the average current drawn by PM5 and PM7 when the clock is low, and the discharge current through NM5 when the clock is high. Consequently, the proposed design exhibits a lower average current consumption in the slave latch compared to a traditional conventional flip-flop (TCFF), primarily due to the absence of redundant charging at node B. This contributes to reduced dynamic power dissipation and improved switching efficiency. In addition to global clock signal (clk), comparator clock (clkc), seven internal clock signals (Q1 to Q7) are utilized for timing synchronization in the SAR logic control unit including D flip flops and multiplexers as given in chapter 5 as proposed control unit. Finally, interfacing of all the designed modules i.e proposed dynamic comparator, proposed switching scheme with reduced switching energy per conversion step and proposed control unit, an 8-bit SAR ADC is designed and simulated in CADENCE 45nm technology node. The results and simulation of designed 8-bit SAR ADC is given in next section as 6.5.

6.5 RESULT AND SIMULATION ANALYSIS OF PROPOSED 8 BIT SAR ADC

The complete designed 8-bit SAR ADC utilizing interfaced modules of proposed dynamic comparator, proposed DAC and control unit is simulated in CADENCE Virtuoso 45nm technology node. The waveform in Fig. 6.6 shows that the input to be digitized is given as V_{in} of 110 mV within sampling frequency range of 540 KS/s. The V_{in} is compared with $V_r/2$ voltage in first cycle and the comparator output D_p will be obtained terms of logic 0 or 1. Fig. 6.6 shows that X_s is the sampling pulse when X_s is at logic 0, the input is sampled. Here, X is $V_r/2$ as reference voltage is of 1.2 V so X is 600 mV and Y is the input signal to be converted into digital equivalent. Further, Y for the simulation is taken as 620 mV. So, after sampling, when positive edge of clock pulse will be arrived, X will be compared with input Y and as X is lesser than Y so output D_p will give 1 as MSB bit and X will be switched to $V_r/4$ as $X/2$. So, now input will be compared to $V_r/4$ in subsequent clk cycle. Output is shown after 2nd clk cycle i.e from 3rd cycle. So, from the given output, it is inferred that for given input of 620 mV the equivalent generated digital output is 10000101 i.e., count 133 so as per generated digital output equivalent analog value is resolution multiplied by decimal equivalent of input digital value which will be $1.2/256 \times 133V = 623.4$ mV which is showing an error of 3.4 mV which is lesser than 1 LSB.

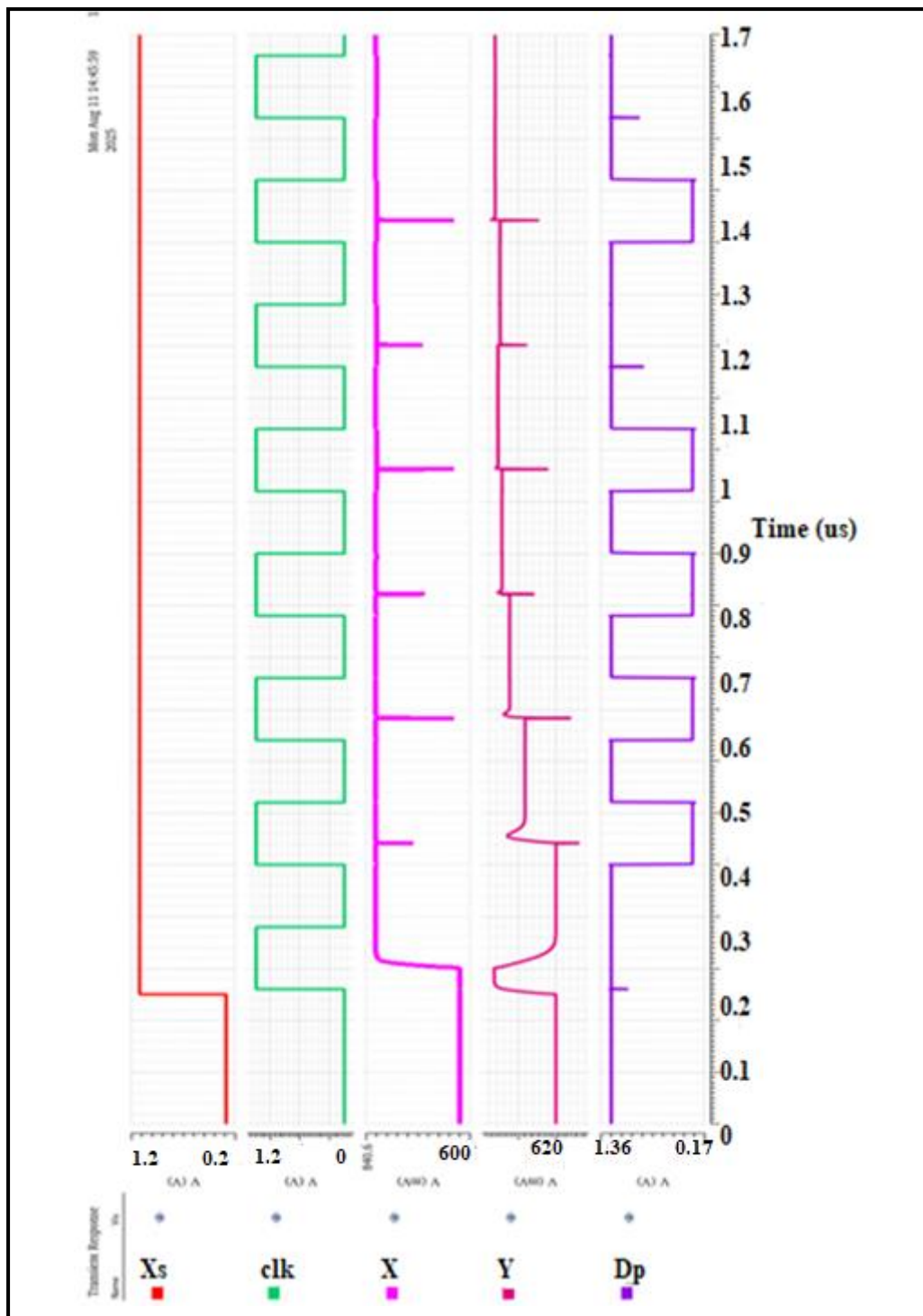


Fig. 6.6 Final digitized output of 8-bit SAR ADC for 620 mV within 540 KS/s

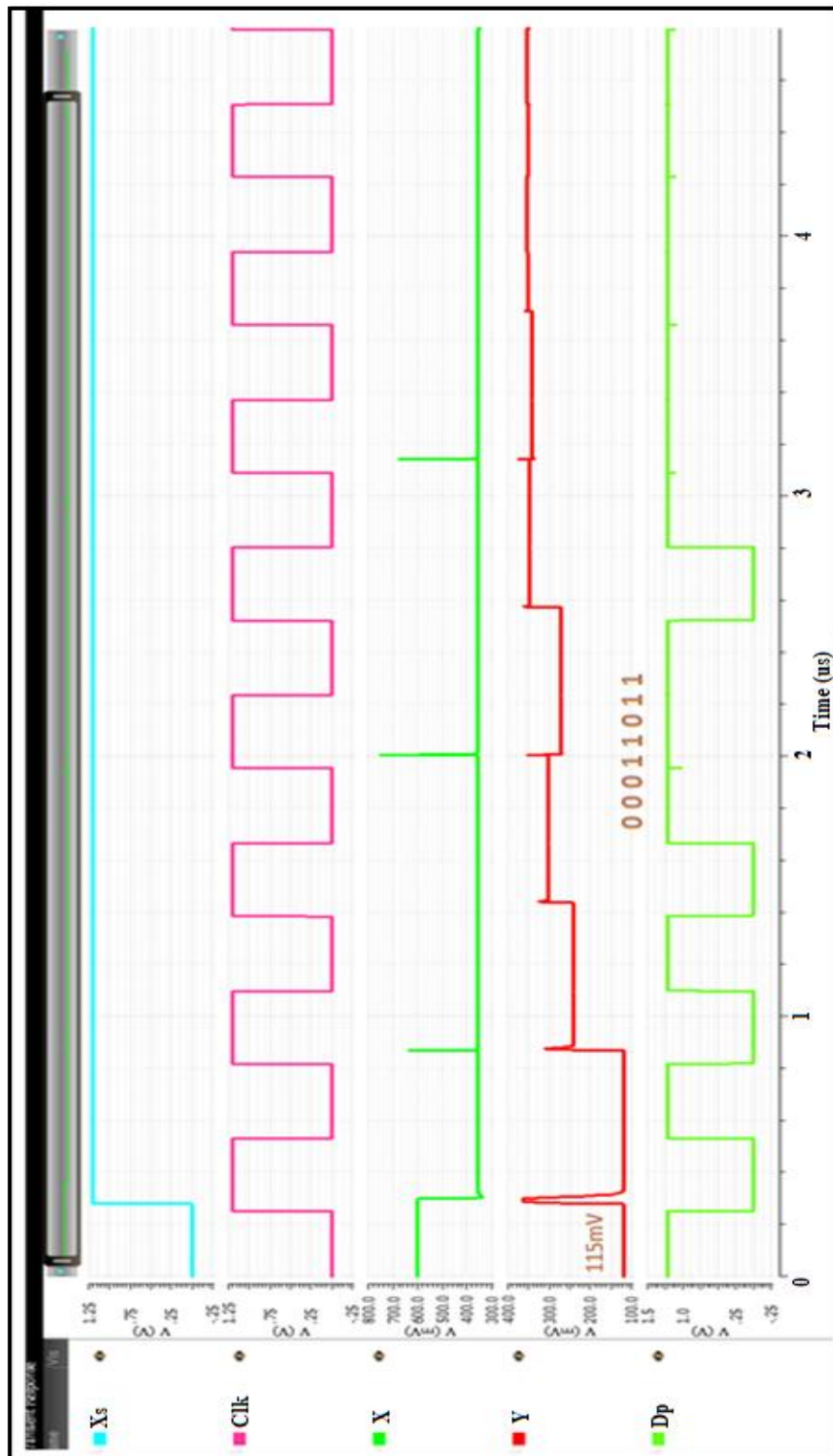


Fig. 6.7 Final digitized output of 8-bit SAR ADC for 115 mV above 540 KS/s

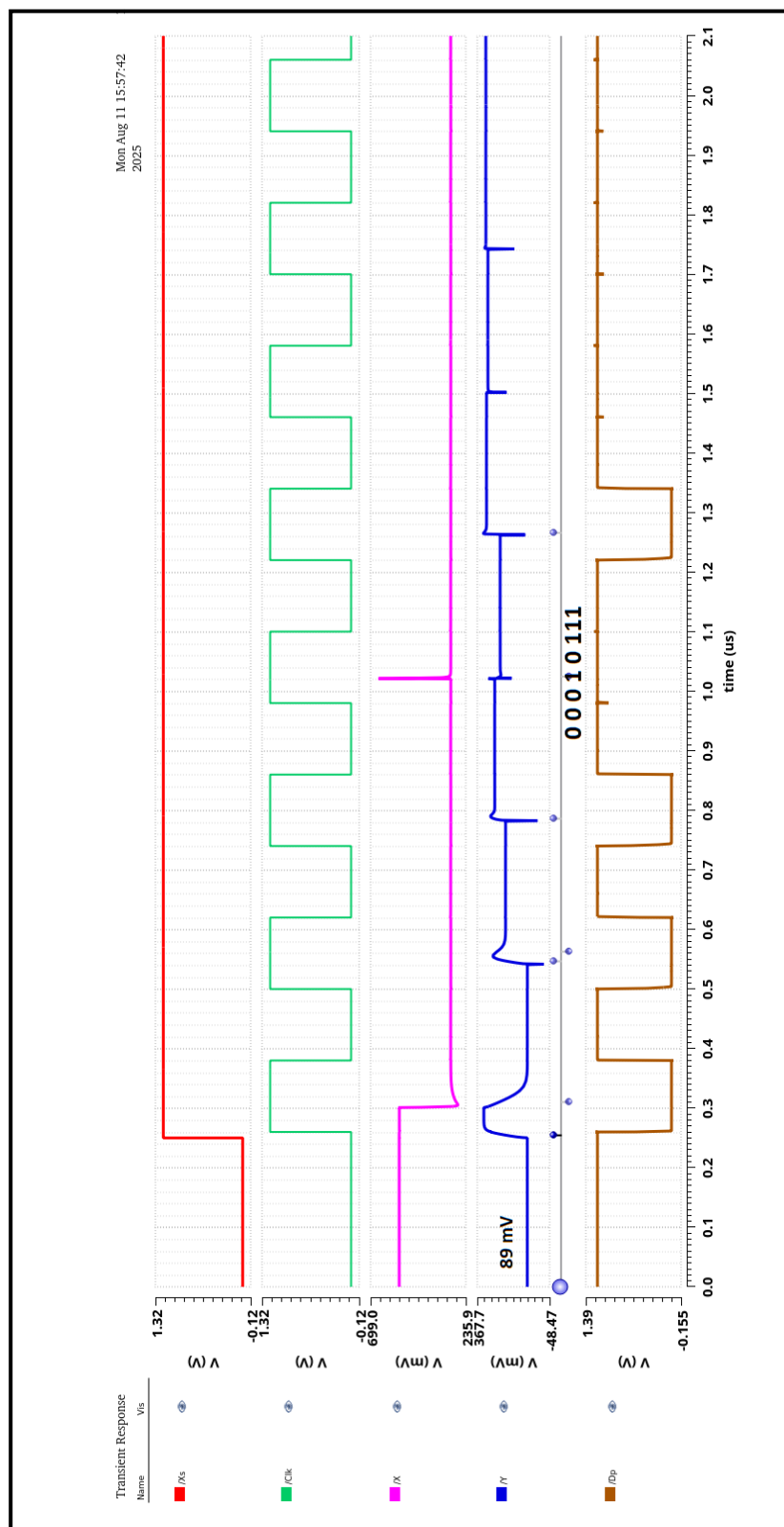


Fig. 6.8 Final digitized output of 8-bit SAR ADC for 89 mV above 540 KS/s

Fig. 6.7 shows the digitized output of designed SAR ADC for 115 mV with sampling frequency above 540 KS/s i.e around 1 MS/s. The digitized output is 00011011 that results into the count of 27 which in turn showing analog sampled value of 126.56 mV so there occurs an error of 11.56 mV with respect to the input signal and as a result increased nonlinearity is observed with increase in the input signal frequency arises due to capacitor mismatch and increase in the parasitics effect at higher frequency. Further, Fig. 6.8 shows the digitized output for 89 mV and the final digitized output is 00010111.

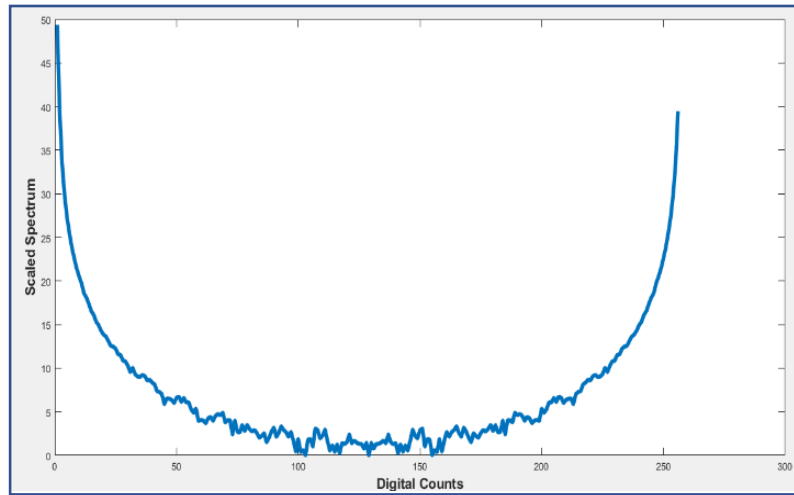


Fig. 6.9 Scaled spectrum output of designed 8-bit SAR ADC

Further, Behavioral simulations is conducted to assess the static performance of the proposed 8-bit single-ended successive approximation register (SAR) analog-to-digital Converters (ADCs) using logical testing methods. The results are illustrated in the Fig. 6.9 and Fig. 6.10, which display the scaled spectrum and the integral non-linearity (INL) of the prototype ADC

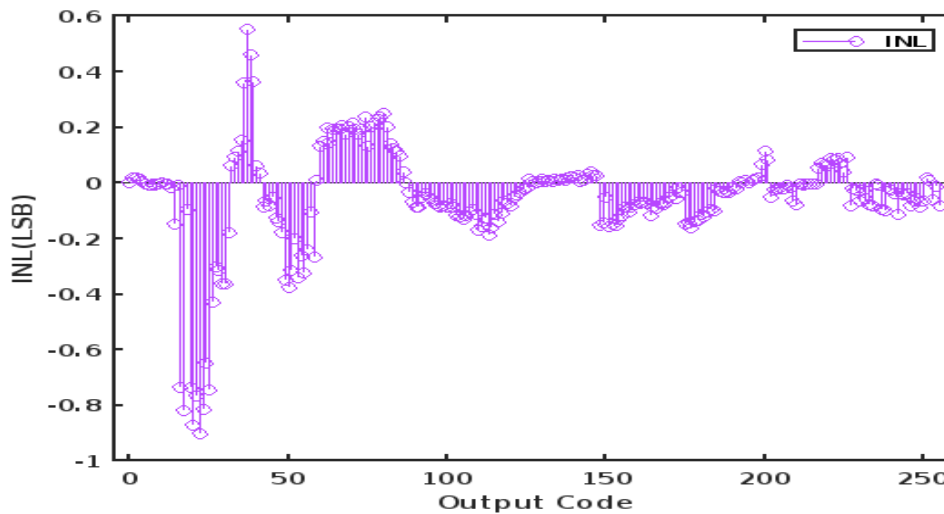


Fig. 6.10 INL measurement in designed 8-bit SAR ADC for frequency within 540 KS/s

for all possible 256 output codes values. This behaviour is attributed to the largest capacitor in the capacitor array, which undergoes transitions between $V_r/2$ and ground (GND) at these output levels. SFDR i.e difference between the first and the second harmonic is calculated to be of the order of 47.89 dB. Effective number of bits (ENOB) is specified by $(\text{SINAD} - 1.76)/6.02$ where SINAD specifies signal to noise ratio plus distortion. Further, the followed scheme implemented an 8-bit SAR ADC incorporating a single ended DAC designed using a single reference voltage along with a bootstrap switch is implemented to give zero switching energy in first two MSB conversions. Also, SAR logic includes a counter-based SAR controller. The master 1 switch connects the top plates of the capacitive DAC [$Z1_{(\text{MSB})}$, $Z2$, ... $Z8_{(\text{LSB})}$] to ground at the beginning of the ADC conversion.

The DAC capacitors use binary weighting, represented as $[2^{N-2}C, 2^{N-3}C, \dots, 2C, C, C]$, where C is the unit capacitor and N is the number of bits. When the master 2 cap switch closes with [$Z9_{(\text{MSB})}$, $Z10 \dots Z16_{(\text{LSB})}$], the top plates of both DAC capacitors link to $V_r/2$ and V_{IN} through capacitive switching. It is important to have a comparator with low offset and fast decision time for the SAR ADC design. This design works well up to 500 MHz, has zero static power loss, and does not require a preamplifier. Additionally, the design supports a wide input common-mode range and allows for quick decisions with small differential input voltages, which can be managed using some proposed analog techniques

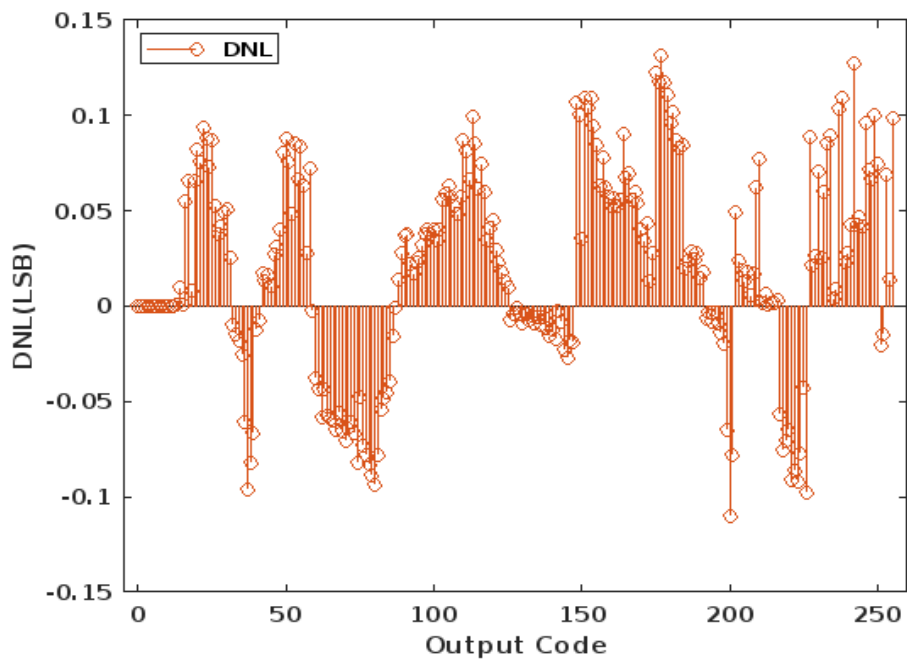


Fig. 6.11 DNL measurement in designed SAR ADC for frequency within 540 KS/s

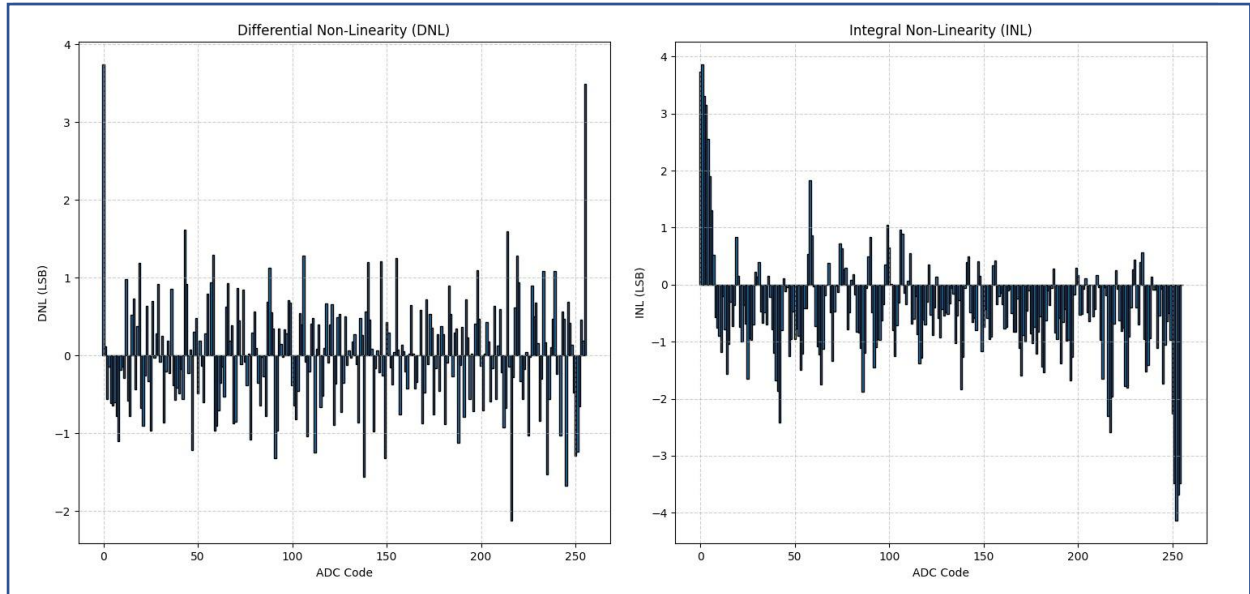


Fig. 6.12 INL and DNL measurement of designed SAR ADC at frequency 1MS/s

Fig. 6.11 gives the DNL plot of designed SAR ADC for sampling frequency 540 KS/s, and the output parameters are represented in Table 6.1. Also, circuit is simulated with increased frequency range upto 1 MS/s and results have verified that increased non linearities values have been observed in the output as shown in Fig. 6.12 as an effect of increased parasitics in terms of increased INL and DNL.

Table 6.1: Parametric summary of proposed 8-bit SAR ADC

S.No.	Parameter	Obtained Value
1	Supply Voltage	1.2 V
2	Sampling Rate	540 KS/s
3	Resolution	8 bits
4	SNDR	46.08 dB
5	Max DNL	+0.13/-0.12 LSB
6	Max INL	+0.52/-0.90 LSB
7	Power Consumption	5.38 μ W
8	ENOB	7.38

So, from the given output, it is inferred that for given input of 110 mV the equivalent generated digital output is 00010111 i.e 23 so as per generated digital output equivalent analog value is resolution multiplied by decimal equivalent of input digital value which will be $1.2/256 \times 23V$ equivalent to 107.8 mV. It represents the probability of delay within number of samples. With

ENOB value of 7.38, designed 8-bit SAR ADC is showing SNDR value of 46.08 dB with max DNL value of +0.13/(-0.12) LSB and max INL as of +0.52/(-0.90) LSB.

Table 6.2: Comparative analysis of different 8-bit SAR ADCs

S.No.	Parameter	This Work	[115]	[113]	[157]
1	Supply Voltage (V)	1.1	0.9	1.2	1
2	Fs (MS/s)	0.54	1	1	2
3	Resolution (bits)	8	8	8	8
4	SNDR (dB)	46.08	45.64	49.3	48.11
5	Power Consumption (μ W)	5.38	29.7	21	15.98
6	ENOB (bits)	7.38	7.29	7.9	NA

Table 6.2 depicts the comparative analysis of different designed 8-bit SAR ADCs with the proposed SAR ADC. The designed ADC is consuming 5.38 μ W of power which is reasonably a good value at 540 KS/s. The power distribution of each block is shown in Fig. 6.13. In the designed SAR ADC, 62.80% power consumption is of capacitor DAC array, 23.50% of power consumption is of SAR logic.

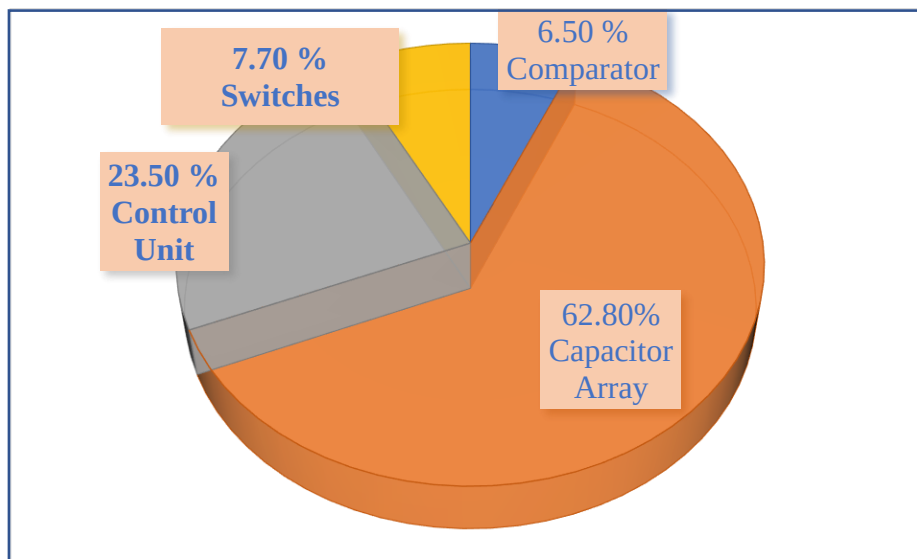


Fig. 6.13 Power consumption breakdown for each module of SAR ADC

6.50 % power consumption is possessed by dynamic comparator and 7.70 % of power switches is carried out by switches. So, each block optimization in terms of energy efficiency is considered to finally design an energy efficient 8-bit SAR ADC.

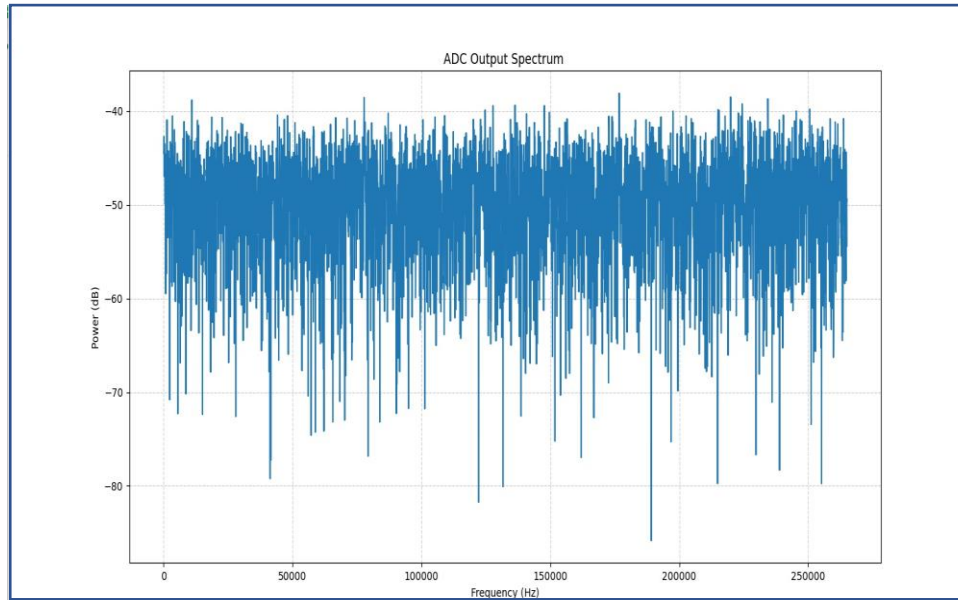


Fig. 6.14 Power consumption vs frequency plot of designed SAR ADC

Fig. 6.14 depicts the ADC output frequency spectrum as the power distribution with frequency variation in designed SAR ADC. Designed ADC is converting an analog sample value between 0 to 1.2V with power consumption of 5.38 μ W at 540 KS/s. INL and DNL values are also restricting between ± 1 LSB for simulation of circuit upto 540 KS/s. With increase in frequency of the input signal, the parasitic effect gives an increased value of INL and DNL values.

6.6 SUMMARY OF THE IMPORTANT RESULTS

An 8-bit SAR ADC incorporating a single ended DAC designed using a single reference voltage along with a bootstrap switch is implemented to give zero switching energy in first two MSB conversions. In addition, a novel dynamic comparator is also utilized in the complete SAR design incorporating reset switch disconnecting preamplifier and latch modules in reset state to avoid the power wastage in this mode. Also, the implemented switching scheme is incorporated with novel SAR logic for the control unit using flip flops and multiplexers. Brief view of important results is given below:

1. All the designed modules; comparator, DAC & control unit are interfaced to design an 8-bit SAR ADC with single reference voltage $V_r/2$ using dummy DAC designed along with bootstrap switch at positive input of comparator implemented to give zero switching energy in first two MSB conversions.

2. The reduced power of the complete SAR ADC of the order of 5.38 μ W is obtained due to inclusion of low power proposed dynamic comparator and DAC unit with reduced switching energy per conversion step.
3. Parametric analysis shows that SNDR value of 46.08 dB, SFDR 47.89 dB, ENOB 7.38, DNL +0.13/(-0.12) LSB, INL +0.52/(-0.90) LSB at sampling rate of 540 KS/s is obtained.
4. The entire design is simulated in CADENCE 45 nm technology node. Proposed SAR ADC is completely designed at transistor level implementation of each module including comparator, DAC unit and control logic.
5. The DAC unit consumes zero switching energy in the first two MSB decisions as per proposed switching algorithm which results saving of 92 % of switching energy with respect to the conventional switching scheme at 540 KS/s.
6. Control logic also termed as SAR logic is created and implemented for SAR ADC. D flip flops and multiplexers-based logic is created. Q1 to Q7 internally generated signals are utilized along with clk signal and sample signal to provide timing synchronization between comparator and DAC module.

An 8-bit SAR ADC incorporating a single ended DAC designed using a single reference voltage along with a bootstrap switch is implemented to give zero switching energy in first two MSB conversions. In addition, a novel dynamic comparator is also utilized in the complete SAR design incorporating reset switch disconnecting preamplifier and latch modules in reset state to avoid the power wastage in this mode. Also, the implemented switching scheme is incorporated with novel SAR logic for the control unit using flip flops and multiplexers to get the reduced power of the complete SAR ADC of the order of 5.38 μ W, SNDR 46.08 dB, SFDR 47.89 dB, ENOB 7.38 bits, DNL +0.13/(-0.12) LSB, INL +0.52/(-0.90) LSB at sampling rate of 540 KS/s. The entire design is simulated in CADENCE 45 nm technology node.

Designed SAR ADC is completely designed at transistor level implementation of each module including comparator, DAC unit and control logic. Each unit has its own parameters of importance like comparator unit includes the minimization of power, delay, offset voltage and kickback noise. DAC unit requires minimization of DAC area and switching energy required in comparisons and control unit has to optimally work so that before next clk cycle all required switching's has to be completed to provide root to the next stage. Keeping all these parameters and designing constraints as on priority in our design, a reasonably good 8-bit SAR ADC is designed in CADENCE Spectre.

CHAPTER - 7

CONCLUSIONS AND FUTURE SCOPE

The present research work is focused on the design and analysis of 8-bit SAR ADC for low power applications. Among different available architectures of ADCs, for medium resolution of 8 bits and medium speed of 540 KS/s at low power consumption, design of low power 8-bit SAR ADC is considered in the research project. SAR ADC consists of major modules as comparator, digital to analog converter and SAR logic-based control unit. Each module is designed and simulated individually in CADENCE virtuoso 45 nm technology node and finally the resulting interfaced circuit of 8-bit SAR ADC is simulated at same technology node. This chapter concludes the important results of each individual proposed module of SAR ADC along with final 8-bit designed SAR ADC for low power applications. Moreover, it also presents some specific directions for future research work.

7.1 CONCLUSIONS

A SAR ADC is composed of major modules as a low power dynamic comparator, a capacitor based digital to analog converter (CDAC) and a control logic for conversion of analog sampled value to its digital equivalent. Design and parametric optimization of each module is considered stepwise. Keeping in view, at first, design and parametric simulation analysis of different low power dynamic comparators in CADENCE Virtuoso 45 nm technology node is carried out. Strong arm latch dynamic comparator is considered as the baseline comparator consisting of preamplifier and regeneration latch. However, this comparator does not avoid the direct path connection between V_{DD} and ground and circuit possess 51.38 nW of average transient power consumption. Further, double tail dynamic comparator and modified double tail dynamic comparator are considered for simulation & analysis and the transient analysis of both comparators is carried out. Despite significant advancements, there was a strong need to develop a dynamic comparator that offers enhanced transconductance gain in the pre-amplifier, while simultaneously minimizing switching and leakage power and ensuring proper isolation between the pre-amplifier and the regeneration latch. Furthermore, enabling all switching operations using a single clock (clk) signal instead of its inverted counterpart can contribute to additional power savings. For above required technical advancement in dynamic comparator, first proposed dynamic comparator architecture design along with the simulation analysis is focussed.

Simulation of proposed comparator shown in Fig. 3.4 observed average transient power of 33.81 nW at nn corner which is much reduced value compared to the other architectures like strong arm latch, double tail dynamic and modified double tail dynamic comparator. The power consumption is limited to 19.56 nW at ss corner and 53.85 nW for ff corner as the architecture creates an isolation between pre-amplifier and latch module when clk is low due to which leakage power is avoided. The proposed comparator is simulated with capacitive loading of 5.1 pF which is the required values for using this module along with capacitive DACs. PDP of 0.4 fJ along with temperature variation from -40-degree centigrades to 110-degree centigrades is carried out for the first proposed comparator.

Further, charge sharing based dynamic comparator is also proposed which is working well upto few GS/s and power consumption of 9.36 μ W is observed at 1 GS/s. Proposed charge sharing logic based dynamic comparator is limiting offset voltage to 7.8 mV and the delay is limited to 48.2 ps. Kickback noise analysis and statistical analysis of noise and input referred offset voltage due to common mode voltage variation (V_{cm}) has validated that the effect of variation of input common mode voltage on noise in proposed charge shared logic-based circuit is less sensitive to V_{cm} variations as g_m/I_D of input transistors M12 and M13 (Fig. 3.12) has been increased with the biasing of transistors in weak inversion region. The observed delay exhibits a reduction from 56.3 ps to 23.17 ps as the input differential voltage (V_{diff}) ranges from 10 mV to 200 mV for varying common-mode voltage levels (V_{cm}) in charge shared circuit as second proposed dynamic comparator. The comparator demonstrated reduced kickback noise by employing auxiliary transistors M8 and M9 to separate the output nodes. Additionally, this approach effectively mitigated the mismatch effect and minimized the impact of parasitic capacitance associated with the transistor design.

Further, designing of DAC unit with reduced switching energy is also considered as DAC unit is the most power-hungry module of SAR ADC. In literature many DAC switching schemes are designed by the researchers like common mode switching scheme, monotonic switching scheme, capacitor splitted switching scheme, merged capacitor etc. Each switching scheme followed a different switching methodology and contributed to the saving of switching energy per conversion cycle compared to the conventional one. Traditional switching scheme consumes $682.5 CV_{ref}^2$, 427.66 CV_{ref}^2 of switching energy is consumed by split capacitor technique and many more. Literature highlights that reduction of switching energy per conversion cycle in DAC capacitor array is considered as a focussed domain be the researchers. But still there was a need to design a DAC unit with zero switching energy in first two MSB

comparisons for significant reduction of switching energy. In view of this, switching scheme utilized with single reference voltage of $V_{ref}/2$ is proposed which perform first two MSB comparisons with zero switching energy. Switching scheme require average of $57.4 CV_{ref}^2$ of switching energy which is much reduced value approximately by 92 percent compared to conventional capacitor-based switching scheme. Also, compared to conventional switching scheme, number of capacitors in the DAC array have been reduced by 50 percent. Moreover, proposed DAC unit consists of $2 \times 2^{N-1} C = 2^N C$ total capacitance value. In proposed switching scheme, a single ended behaviour is obtained utilizing a dummy DAC at the positive input of comparator. The first comparison is performed without any switching power. Also, after first comparison of V_{in} with $V_{ref}/2$, the bottom plate of dummy DAC is switched either to ground or $V_{ref}/2$ and will remain at that state till the final digitization is performed with $V_{ref} = 1.1 V$. MOM capacitors are observed to be the preferred choice to shift the design from schematic to final back-end stage.

Third module of SAR ADC is design of low power control unit for SAR ADC. The literature highlights the necessity of SAR logic and DAC co-optimization, especially when advanced switching techniques such as monotonic, common-mode (VCM)-based, and capacitor-splitting schemes are employed for switching. The designing process of control unit includes designing of enhanced D flip flops with improved set up/hold time constraints, clock and internal clock signals for better timing synchronization, multiplexer, sampling logic as the beginning step and SAR logic generation bitwise to implement the proposed switching scheme control unit is included in the project. Finally, based on enhanced D flip flops and multiplexers with proper synchronization a novel control unit for utilization to implement proposed switching scheme is designed.

Enhanced D flip flop is working well for the required bandwidth and resolution of input signal at low power consumption. The proposed synchronous control unit has less complexity and better timing synchronizations due to which all the control signals are getting generated within time constraints. Sampling phase begins the digitization process when X_s is low and D_p (comparator output) is the digitized output bit which is generating digital data in synchronization with internal generated clock signals (Q1 to Q7) that is providing better linearity in the digital data generation process. The control unit is implementing SAR logic bitwise, first internal clock Q1 is providing timing synchronization to MSB-1 bit, just after the sampling on first clk_c , MSB bit gets generated. Remaining bits are also being generated by the control unit with better timing optimization between DAC and comparator, Q2 is providing

timing synchronization to MSB-2 bit and so on. Generated data is stored in shift register and as clk timings, it is fetched as digitized 8-bit output for the designed SAR ADC. The timing sequence is generated to perform the digitization at sampling rate of 540 KS/s. The clk signal is given with a delay of 260 ns and period of 240 ns. Xs signal is turned high at 250 ns so 10 ns is given as time window for sampling of input signal. Further, with the maximum delay of 40 ns as of comparator, the MSB -1 bit is generated by 300 ns. Also, it is inferred from that inclusion of internal clock signals (Q1 to Q7) along with global clock (clk) in the proposed control unit, a better timing synchronization is achieved as compared to other existing designs at moderate power consumption. Enhanced D flip flops are avoiding the leakage power to reduce the power consumption of the control unit.

The proper interfacing of designed modules along with proper controlling of common mode voltage V_{cm} is equally important to result the interfaced circuit into an ultra-low power SAR ADC. The minimization of non-linearities in designed SAR ADC like reduced differential non linearity (DNL) and integral non linearity (INL) with low power consumption holds the major design projection as literature highlights which is reflected in calculated INL & DNL values from the digitized output. Keeping this view, design of final interfaced 8-bit SAR ADC including all the optimized modules is carried out.

All the designed modules; comparator, DAC & control unit are interfaced to design an 8-bit SAR ADC with single reference voltage $V_{r/2}$ using dummy DAC designed along with bootstrap switch at positive input of comparator implemented to give zero switching energy in first two MSB conversions. The reduced power of the complete SAR ADC of the order of 5.38 μ W is obtained due to inclusion of low power proposed dynamic comparator and DAC unit with reduced switching energy per conversion step. Parametric analysis shows that SNDR value of 46.08 dB, SFDR 47.89 dB, ENOB 7.38, DNL +0.13/(-0.12) LSB, INL +0.52/(-0.90) LSB at sampling rate of 540 KS/s is obtained. The entire design is simulated in CADENCE 45 nm technology node.

To conclude, Proposed SAR ADC is completely designed at transistor level implementation of each module including comparator, DAC unit and control logic. Proposed low power dynamic comparator, DAC unit with zero switching energy in the first two MSB decisions including proposed switching algorithm which results saving of 92 % of switching energy with respect to the conventional switching scheme at 540 KS/s. Control logic based on SAR logic is designed using D flip flops and multiplexers-based logic in which Q1 to Q7 internally generated signals are utilized along with clk signal and sample signal to provide timing synchronization

between comparator and DAC module. The final designed 8-bit SAR ADC is limiting power dissipation to $5.38 \mu\text{W}$ with reasonably good INL, DNL, SNDR and SFDR values as $+0.52/(-0.90)$ LSB, $+0.13/(-0.12)$ LSB, 46.08 dB and 47.89 dB respectively.

7.2 FUTURE SCOPE

The present research depicts the design and performance analysis of 8-bit SAR ADC for low power applications. The proposed SAR ADC based on single ended switching scheme in DAC unit is providing zero switching energy in the first two MSB decisions which results saving of 92 % of switching energy with respect to the conventional switching scheme for the sampling rate of 540 KS/s. Also, inclusion of proposed dynamic comparator with kickback noise reduction logic is providing good resolution of as good as 2 mV for the 8-bit SAR ADC with better linearity but parasitics restricts the capacitive DAC unit to generate the exact required in between comparison voltage levels.

There are always some literatures which forms the basis for the future work., so yes, our designed SAR ADC may be the good base for the new optimizations. Future work is suggested to be carried out on some new architectures of comparators to optimize its figure of merit. For FOM, its power and delay (hold delay + latch delay) will be the parameters to be worked upon. Further work on the capacitance mismatch avoidance to improve the nonlinearity of designed ADC will be the major aspect for the researchers with switching energy reduction in third comparison too will be the major prominent area to be worked upon. Control logic with reduced architecture is also one grey area which holds more work options for the researchers. Also, significant future research direction lies in the development of ultra-energy-efficient capacitor switching schemes for the DAC unit. Since the capacitive DAC accounts for a major portion of SAR ADC power consumption, advanced charge-recycling, monotonic, and multi-reference switching techniques can be explored to further minimize switching energy without degrading linearity. Additionally, hybrid DAC structures combining capacitive and resistive elements may offer improved energy–area trade-offs for medium-resolution designs.

Another important scope is the design of adaptive and intelligence-assisted SAR control logic. Incorporating digitally assisted calibration, background error correction, and adaptive decision algorithms can help mitigate non-idealities such as capacitor mismatch, comparator offset, and timing skew. The integration of machine-learning-assisted calibration techniques at the digital back end also presents a potential research avenue for enhancing robustness while maintaining low power operation. Further improvements can be achieved through comparator architecture

optimization, particularly by exploring dynamic and asynchronous comparator designs with near-zero static power consumption. Future work may focus on comparator designs that maintain high sensitivity at ultra-low supply voltages while suppressing noise and offset variations across process, voltage, and temperature (PVT) corners. With continued technology scaling, near-threshold and sub-threshold SAR ADC operation represents another promising research direction. Operating the ADC at reduced supply voltages can drastically lower power consumption; however, it introduces challenges related to reduced signal swing, increased noise sensitivity, and slower settling behavior. Addressing these challenges through co-optimized analog–digital design methodologies can significantly enhance the applicability of SAR ADCs in battery-operated systems.

Moreover, time-interleaved and hybrid SAR architectures offer scope for achieving higher sampling rates at low energy per conversion. Future research may focus on minimizing interleaving-related errors through efficient background calibration techniques while preserving the inherent low-power advantage of SAR ADCs. Finally, the integration of reconfigurable and application-aware SAR ADCs capable of dynamically adjusting resolution, sampling rate, and power consumption based on workload requirements is a promising future direction. Such adaptive ADCs can substantially improve overall system-level energy efficiency in heterogeneous and multi-mode electronic systems.

Designing an 8-bit Successive Approximation Register (SAR) ADC operating at 540 KS/s offers a practical balance between speed, resolution, and power efficiency, making it highly suitable for modern embedded and data acquisition systems. Such converters play a vital role in biomedical devices, wearable sensors, and portable monitoring systems, where real-time signal conversion with low energy consumption is essential. Their relatively simple architecture enables cost-effective implementation, which supports the development of affordable healthcare technologies and promotes wider accessibility, especially in resource-constrained environments.

Beyond healthcare, this design contributes to broader societal advancements by supporting Internet of Things (IoT) applications, smart infrastructure, and energy-efficient electronics specially in pollution monitoring sensor nodes and smart grids. Its low-power operation aligns with sustainable design goals by reducing energy consumption and extending device lifetimes. Additionally, research and development in SAR ADC design strengthen academic and industrial progress in VLSI and semiconductor technologies, fostering innovation and skill development.

REFERENCES

1. S. H. Jo, H. W. Cho, and H. J. Yoo, "A fully reconfigurable universal sensor analog front-end IC for the Internet of Things era," *IEEE Sensors Journal*, vol. 19, no. 7, pp. 0000–0000, 2019.
2. B. M. Kelly, A. T. DiLello, and D. W. Graham, "Reconfigurable analog pre-processing for efficient asynchronous analog-to-digital conversion," *Journal of Low Power Electronics and Applications*, vol. 9, no. 3, pp. 1–18, 2019.
3. K. Seong, J. S. Han, Y. Shim, and K. H. Baek, "A 2.5 GS/s 7-bit 5-way time-interleaved SAR ADC with on-chip background offset and timing-skew calibration," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 10, pp. 4043–4047, 2022.
4. J. Lee, M. Kim, S. Hong, J. Park, H. Kim, and B. Kim, "A 0.56-mW 63.6-dB SNDR 250-MS/s two-step SAR ADC in 8-nm FinFET," in *Proc. IEEE Symp. VLSI Technology and Circuits*, Honolulu, HI, USA, pp. 1–2, 2022.
5. W. Sansen, "Minimum power in analog amplifying blocks," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 4, pp. 44–53, 2015.
6. X. Zhang, W. Fan, J. Xi, and L. He, "14-bit fully differential SAR ADC with PGA used in readout circuit of CMOS image sensor," *Journal of Sensors*, vol. 2023, Art. ID 6651642, pp. 1–17, 2023.
7. H. Aminzadeh, "A low-cost tiny-size successive approximation ADC for applications requiring low-resolution conversion with moderate sampling rate," *Circuits, Systems, and Signal Processing*, vol. 38, no. 1, pp. 242–258, 2019.
8. C. Yang, Y. Chen, X. Zhang, J. Wang, and Z. Wang, "An area-efficient SAR ADC with mismatch error shaping technique achieving 102-dB SFDR and 90.2-dB SNDR over 20-kHz bandwidth," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 29, no. 8, pp. 1575–1585, 2021.
9. Y. Chen, Y. Zhuang, and H. Tang, "An ultra-low power consumption high-linearity switching scheme for SAR ADC," *Journal of Circuits, Systems, and Computers*, vol. 29, no. 6, pp. 2050086-1–2050086-14, 2020.
10. L. Xie, J. Su, J. Liu, and G. Wen, "Energy-efficient capacitor-splitting DAC scheme with high accuracy for SAR ADCs," *Electronics Letters*, vol. 51, no. 6, pp. 460–462, 2015.
11. S. Weaver, B. Hershberg, and U.-K. Moon, "Digitally assisted comparator calibration for high-speed ADCs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1202–1213, 2013.
12. Z. Y. Deng, Y. Zhu, X. Tang, and N. Sun, "A hybrid switching scheme for SAR ADC with capacitor segmentation and reference modulation," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 1, pp. 51–55, 2020.

13. T. Miki, T. Morie, and Y. Matsuzawa, "A 10-bit 50-MS/s pipelined ADC using time-domain comparator," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 11, pp. 2774–2783, 2012.
14. A. Verma and B. Razavi, "A 10-bit 500-MS/s pipelined ADC with split ADC architecture," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3380–3389, 2009.
15. J. Liu, S. Liu, R. Ding, and Z. Zhu, "A conversion-mode reconfigurable SAR ADC for multistandard systems," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 29, no. 5, pp. 0000–0000, 2021.
16. Y. Chiu, "An 11-bit 1.2-V 50-MS/s SAR ADC with redundant bit and digital calibration," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1661–1670, 2010.
17. T. Yang, Y. Chen, H. Zhang, J. Li, and Z. Wang, "A configurable 5.9- μ W analog front-end for biosignal acquisition," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, USA, pp. 1–4, 2015.
18. A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1 V 3.8 μ W 100 kS/s SAR ADC with time-domain comparator," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1607–1616, 2012.
19. J. Craninckx and G. Van der Plas, "A 65 fJ/conversion-step 0-to-50 MS/s 0-to-0.7 mW 9-bit charge-sharing SAR ADC in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2647–2656, 2007.
20. R. Kapusta, S. L. Hsu, P. Y. Wu, and C. C. Liu, "A 14-b 80-MS/s SAR ADC with 73.6-dB SNDR in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3059–3066, 2013.
21. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion technique—Part I," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 6, pp. 371–379, 1975.
22. B. Razavi, "Charge steering: A low-power design paradigm," *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 1–8, 2013.
23. R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 539–550, Apr. 1999.
24. B. Razavi, "A tale of two ADCs: Pipelined versus SAR," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 3, pp. 38–46, 2015.
25. B. Razavi, "The flash ADC [A circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 9–13, 2017.
26. T. Oh, H. Venkatram, and U. K. Moon, "A 70-MS/s 69.3-dB SNDR 38.2-fJ/conversion-step time-based pipelined ADC," *Proc. IEEE Symp. VLSI Circuits*, pp. C96–C97, 2013.
27. N. N. Çikan and M. Aksoy, "Analog-to-digital converters performance evaluation using figures of merit in industrial applications," *Proc. European Modelling Symp. (EMS)*, Pisa, Italy, pp. 205–209, 2016.

28. B. Murmann, "ADC performance survey 1997–2016," online database. Available: <http://www.stanford.edu/~murmman/adcsurvey.html>.
29. C. H. Lin and K. A. Wen, "An innovative SAR ADC for a nine-axis sensing system," *Journal of Low Power Electronics and Applications*, vol. 11, no. 1, pp. 1–24, 2021.
30. M. Firlej, P. Grybos, P. Maj, T. Gromek, and R. Szczygiel, "Ultra-low power 10-bit 50–90 MS/s SAR ADCs in 65-nm CMOS for multichannel ASICs," *Journal of Instrumentation*, vol. 19, 2024.
31. S. Das, A. Banerjee, S. Chatterjee, and S. Sen, "An 8-bit split CDAC-based noise-shaping SAR ADC in 180-nm CMOS for power-efficient digitization of sensor signals," *IEEE Transactions on Instrumentation and Measurement*, vol. 74, Art. no. 2007211, 2025.
32. S. Zhu, Y. Wang, J. Lin, and H. Chen, "A 2-GS/s 8-bit flash ADC based on remainder number system in 65-nm CMOS," in *Proc. IEEE Symp. VLSI Circuits*, Kyoto, Japan, pp. C284–C285, 2017.
33. Y. Duan and E. Alon, "A 6-bit 46-GS/s ADC with >23-GHz BW and sparkle-code error correction," *Proc. IEEE Symp. VLSI Circuits*, Kyoto, Japan, pp. C162–C163, 2015.
34. B. Vaz, J. Goes, N. Van Helleputte, and J. Craninckx, "A 13-bit 5-GS/s ADC with time-interleaved chopping calibration in 16-nm FinFET," in *Proc. IEEE Symp. VLSI Circuits*, pp. 99–100, 2018.
35. K. K. Mandrumaka and F. Noorbasha, "A low-power 10-bit SAR ADC with variable threshold technique for biomedical applications," *SN Applied Sciences*, vol. 1, no. 8, pp. 918–919, 2019.
36. P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 6, pp. 1441–1454, 2008.
37. B. Wicht, M. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, 2004.
38. B. Goll and H. Zimmermann, "A 0.12- μm CMOS comparator requiring 0.5 V at 600 MHz and 1.5 V at 6 GHz," *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, pp. 316–317, 2007.
39. M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Fukuoka, Japan, pp. 269–272, 2008.
40. B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65 V," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.
41. I. S. Abdul Halim, M. F. M. Salleh, and M. N. Hamidon, "Low-power CMOS charge-sharing dynamic latch comparator using 0.18- μm technology," in *Proc. IEEE Regional Symp. Micro and Nano Electronics (RSM)*, Kota Kinabalu, Malaysia, pp. 156–160, 2011.

42. S. Babayan-Mashhadi and R. Lotfi, "Analysis and design of a low-voltage low-power double-tail comparator," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 22, no. 2, pp. 343–352, 2014.
43. P. Bahmanyar, M. Maymandi-Nejad, S. Hosseini-Khayat, and M. Berekovic, "Design and analysis of an ultra-low-power double-tail latched comparator for biomedical applications," *Analog Integrated Circuits and Signal Processing*, vol. 86, no. 2, pp. 159–169, 2016.
44. H. S. Bindra, C. E. Lokin, A.-J. Annema, and B. Nauta, "A 30-fJ/comparison dynamic bias comparator," *Proc. 43rd IEEE European Solid-State Circuits Conf. (ESSCIRC)*, Leuven, Belgium, pp. 71–74, 2017.
45. G. De La Fuente-Cortes, G. Espinosa Flores-Verdad, V. R. Gonzalez-Diaz, and A. Diaz-Mendez, "A new CMOS comparator robust to process and temperature variations for SAR ADC converters," *Analog Integrated Circuits and Signal Processing*, vol. 90, no. 2, pp. 301–308, 2017.
46. V. Savani and N. Devashrayee, "Design and analysis of low-power high-speed shared-charge-reset technique based dynamic latch comparator," *Microelectronics Journal*, vol. 74, pp. 116–126, 2018.
47. A. K. Dubey and R. Nagaria, "Optimization for offset and kickback-noise in a novel CMOS double-tail dynamic comparator: A low-power high-speed design approach using bulk-driven load," *Microelectronics Journal*, vol. 78, pp. 1–10, 2018.
48. H. S. Bindra, C. E. Lokin, D. Schinkel, A. Annema, and B. Nauta, "A 1.2-V dynamic bias latch-type comparator in 65-nm CMOS with 0.4-mV input noise," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1902–1912, Jul. 2018.
49. X. Tang, L. Chen, J. Song, and N. Sun, "An energy-efficient comparator with dynamic floating inverter amplifier," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1011–1022, 2020.
50. N. Shahpari, M. Habibi, and P. Malcovati, "An early shutdown circuit for power reduction in high-precision dynamic comparators," *AEU – International Journal of Electronics and Communications*, vol. 118, Art. no. 153144, 2020.
51. S. Nejadhasan, Z. Mehrabi-Moghadam, E. Abiri, and M. R. Salehi, "Design of a dynamic ADC comparator with low power and low delay time for IoT applications," *Wireless Personal Communications*, vol. 123, no. 2, pp. 1573–1591, 2022.
52. M. Vafaei, M. Hosseini, E. Abiri, and M. Salehi, "A 0.2-V 1.2-nW 1-kS/s SAR ADC with a novel comparator structure for biomedical applications," *Integration*, vol. 88, pp. 362–370, 2023.
53. Z. M. Moghadam, M. R. Salehi, S. R. Nashta, and E. Abiri, "Design and analysis of a power-efficient dynamic comparator with improved transconductance in ultra-low-power SAR ADC applications," *Circuits, Systems, and Signal Processing*, vol. 43, pp. 7498–7520, 2024.

54. N. Sharma, R. K. Srivastava, D. Sehgal, and D. M. Das, "A low-power common-mode insensitive rail-to-rail dynamic comparator for ADCs," *Integration*, vol. 100, Art. no. 102288, 2025.
55. S.-E. Hsieh and C.-C. Hsieh, "A 0.44-fJ/conversion-step 11-bit 600-kS/s SAR ADC with semi-resting DAC," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2595–2603, Sep. 2018.
56. D. Schinkel, E. Mensink, E. A. M. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18-ps setup+hold time," in *IEEE ISSCC Digest of Technical Papers*, pp. 314–315, 2007.
57. M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 μ W at 1 MS/s," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, 2010.
58. M. Liu, H. Zhu, Y. Wang, and Z. Wang, "A 106-nW 10-bit 80-kS/s SAR ADC with duty-cycled reference generation in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2435–2445, 2016.
59. P. M. Figueiredo and J. C. Vital, "Low kickback-noise techniques for CMOS latched comparators," *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. I-537–I-540, 2004.
60. M. Yousefirad and M. Yavari, "Kick-back noise reduction and offset cancellation technique for dynamic latch comparator," *Proc. 29th Iranian Conf. Electrical Engineering (ICEE)*, 2021.
61. H. Song and M. Lee, "Asymmetric monotonic switching scheme for energy-efficient SAR ADCs," *IEICE Electronics Express*, vol. 11, pp. 1–5, 2014.
62. B. P. Ginsburg and A. P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. 184–187, 2005.
63. Y. K. Chang, C. S. Wang, and C. K. Wang, "An 8-bit 500-kS/s low-power SAR ADC for biomedical applications," *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, pp. 228–231, 2007.
64. C. C. Lu and D. K. Huang, "A 10-bit 50-MS/s SAR ADC based on area-efficient and low-energy switching scheme," *IEEE Access*, vol. 8, pp. 28257–28266, 2020.
65. M. Sotoudeh and F. Rezaei, "A four-level switching scheme for SAR ADCs with 87.5% area saving and 97.85% energy reduction," *Circuits, Systems, and Signal Processing*, vol. 39, no. 10, pp. 4792–4809, 2020.
66. C. Yuan and Y. Lam, "Low-energy and area-efficient tri-level switching scheme for SAR ADC," *Electronics Letters*, vol. 48, no. 9, pp. 482–483, 2012.
67. E. Rahimi and M. Yavari, "Energy-efficient high-accuracy switching method for SAR ADCs," *Electronics Letters*, vol. 50, no. 7, pp. 499–501, 2014.

68. S. U. Baek, K. Y. Lee, and M. Lee, "Energy-efficient switching scheme for SAR ADC using zero-energy dual-capacitor switching," *Analog Integrated Circuits and Signal Processing*, vol. 94, no. 2, pp. 317–322, 2018.
69. C. C. Liu, S. J. Chang, G. Y. Huang, and Y. Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.
70. A. Sanyal and N. Sun, "SAR ADC architecture with 98% reduction in switching energy over conventional scheme," *IET Electronics Letters*, vol. 49, no. 4, pp. 248–250, Feb. 2013.
71. L. Chen, X. Tang, J. Song, and N. Sun, "Comparator common-mode variation effects analysis and its application in SAR ADCs," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. 2014–2017, 2016.
72. L. Chen, A. Sanyal, J. Ma, and N. Sun, "A 24- μ W 11-bit 1-MS/s SAR ADC with a bidirectional single-side switching technique," *Proc. 40th European Solid-State Circuits Conf. (ESSCIRC)*, pp. 219–222, Sep. 2014.
73. X. Tang, L. Chen, J. Song, and N. Sun, "A 10-bit 750- μ W 200-MS/s fully dynamic single-channel SAR ADC in 40-nm CMOS," *Proc. 42nd European Solid-State Circuits Conf. (ESSCIRC)*, pp. 413–416, Sep. 2016.
74. L. Chen, X. Tang, J. Song, and N. Sun, "A 0.95-mW 6-bit 700-MS/s single-channel loop-unrolled SAR ADC in 40-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 3, pp. 244–248, 2017.
75. B. P. Ginsburg and A. P. Chandrakasan, "A 500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 4, pp. 739–747, Apr. 2007.
76. Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, and R. P. Martins, "A 10-bit 100-MS/s reference-free SAR ADC in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, 2010.
77. C.-Y. Liou and C.-C. Hsieh, "A 2.4-to-5.2-fJ/conversion-step 10-bit 0.5-to-4-MS/s SAR ADC with charge-average switching DAC in 90-nm CMOS," *IEEE ISSCC Digest of Technical Papers*, pp. 280–281, Feb. 2013.
78. V. Hariprasath, J. Guerber, S. H. Lee, and U. K. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electronics Letters*, vol. 46, no. 9, pp. 620–621, 2010.
79. W. Hu, Y. Chiu, and B. Razavi, "An 8-bit single-ended ultra-low-power SAR ADC with a novel DAC switching method and counter-based digital control circuitry," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 7, pp. 1726–1739, 2013.
80. S.-E. Hsieh and C.-C. Hsieh, "A 0.4-V 13-bit 270-kS/s SAR-ISDM ADC with opamp-less time-domain integrator," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 6, pp. 1648–1656, Jun. 2019.

81. H.-Y. Tai, Y.-S. Hu, H.-W. Chen, and H.-S. Chen, "A 0.85 fJ/conversion-step 10-bit 200 kS/s subranging SAR ADC in 40 nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 196–197, Feb. 2014.
82. P.-C. Lee, J.-Y. Lin, and C.-C. Hsieh, "A 0.4 V 1.94 fJ/conversion-step 10-bit 750 kS/s SAR ADC with input-range-adaptive switching," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 12, pp. 2149–2157, Dec. 2016.
83. S. Polineni, M. S. Bhat, and A. Rajan, "A 10-bit differential ultra-low-power SAR ADC with an enhanced MSB capacitor-split switching technique," *Arabian J. Sci. Eng.*, vol. 44, no. 3, pp. 2345–2353, 2019.
84. B. Jajodia, A. Mahanta, and S. R. Ahamed, "Energy-efficient DAC switching technique for single-ended SAR ADCs," *AEU-Int. J. Electron. Commun.*, vol. 124, Art. no. 153334, 2020.
85. Z. Yang and J. Sun, "A 76.05 dB SNDR 0.303 mW noise-shaping SAR ADC with data-weighted averaging in 40 nm CMOS," *Microelectronics J.*, vol. 163, Art. no. 106750, 2025.
86. D. M. Ellaithy, "A low-power 8-bit 1-MS/s single-ended SAR ADC in 130-nm CMOS for medical devices," *J. Electr. Syst. Inf. Technol.*, vol. 11, Art. no. 21, 2024.
87. P. Harpe, "Low-power SAR ADCs: Basic techniques and trends," *IEEE Open J. Solid-State Circuits Soc.*, vol. 2, pp. 73–81, 2022.
88. X. Zhao, D. Li, X. Zhang, S. Liu, and Z. Zhu, "A 0.6-V 94-nW 10-bit 200-kS/s single-ended SAR ADC for implantable biosensor applications," *IEEE Sensors J.*, vol. 22, no. 18, pp. 17904–17913, Sept. 2022.
89. W. Kim, H. K. Hong, Y. J. Roh, H. W. Kang, S. I. Hwang, and D. S. Jo, "A 0.6 V 12-bit 10 MS/s low-noise asynchronous SAR-assisted time-interleaved SAR ADC," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1826–1839, Aug. 2016.
90. P. J. A. Harpe, E. Cantatore, and A. van Roermund, "A 26 μ W 8-bit 10 MS/s asynchronous SAR ADC for low-energy radios," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585–1595, 2011.
91. C.-H. Chan, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A 3.8 mW 8-bit 1 GS/s 2 b/cycle interleaving SAR ADC with compact DAC structure," *Proc. Symp. VLSI Circuits*, pp. 86–87, Jun. 2012.
92. G.-Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "A 1- μ W 10-bit 200-kS/s SAR ADC with a bypass window for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2783–2795, Nov. 2012.
93. W. Bai and Z. Zhu, "A 0.5-V 9.3-ENOB 68-nW 10-kS/s SAR ADC in 0.18- μ m CMOS for biomedical applications," *Microelectronics J.*, vol. 59, pp. 40–46, 2017.
94. P. Harpe, "A compact 10-bit SAR ADC with unit-length capacitors and a passive FIR filter," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 636–645, Mar. 2019.

95. S. U. Rehman and M. Kamboh, "A CMOS micropower and area-efficient neural recording and stimulation front-end for biomedical applications," *Circuits Syst. Signal Process.*, vol. 34, pp. 1725–1746, 2015.
96. H.-S. Lee, D. A. Hodges, and P. R. Gray, "A self-calibrating 15-bit CMOS A/D converter," *IEEE J. Solid-State Circuits*, vol. SSC-19, no. 6, pp. 813–819, Dec. 1984.
97. M. Ding, X. Tang, J. Song, and N. Sun, "A 46 μ W 13-bit 6.4 MS/s SAR ADC with background mismatch and offset calibration," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 2, pp. 423–432, 2017.
98. S.-W. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.
99. W. Liu, P. Huang, and Y. Chiu, "A 12-bit 45-MS/s 3-mW redundant SAR ADC with digital calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2661–2672, Aug. 2011.
100. Y.-S. Shu, L.-T. Kuo, and T.-Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, Dec. 2016.
101. D. Zhang and A. Alvandpour, "A 12.5-ENOB 10-kS/s redundant SAR ADC in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 3, pp. 244–248, Mar. 2016.
102. B. Yazdani, A. Khorami, and M. Sharifkhani, "Low-power DAC with charge redistribution sampling method for SAR ADCs," *Electron. Lett.*, vol. 52, pp. 187–188, 2015.
103. M. Kramer, M. Ortmanns, and Y. Manoli, "A 14-bit 35 MS/s SAR ADC achieving 75 dB SNDR and 99 dB SFDR in 40 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 1–10, 2015.
104. X. Tang, L. Chen, J. Song, and N. Sun, "Low-power SAR ADC design: Overview and survey of state-of-the-art techniques," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 6, pp. 2249–2262, 2022.
105. H. Lu, X. Tang, and N. Sun, "A data-dependent energy reduction algorithm for SAR ADC using self-adaptive window," *Microelectronics Journal*, vol. 100, Art. no. 104754, 2020.
106. J. Y. Lin and C. C. Hsieh, "A 0.3-V 10-bit 1.17-fJ SAR ADC with merge-and-split switching," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 1, pp. 70–79, Jan. 2015.
107. X. Tang, L. Chen, J. Song, and N. Sun, "A 1.5 fJ/conversion-step 10-bit 100 kS/s SAR ADC with gain-boosted dynamic comparator," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, pp. 229–232, 2017.

108. J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 62–70, Feb. 1989.
109. B. Razavi, "TSPC logic [A circuit for all seasons]," *IEEE Solid-State Circuits Mag.*, vol. 8, no. 4, pp. 10–13, Nov. 2016.
110. D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, Jul. 2012.
111. M. Yip and A. P. Chandrakasan, "A resolution-reconfigurable 5-to-10-bit 0.4-to-1 V power-scalable SAR ADC," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1453–1464, Jun. 2013.
112. P. Harpe, E. Cantatore, and A. van Roermund, "A 30 fJ/conversion-step 8-bit 0–10 MS/s asynchronous SAR ADC in 90 nm CMOS," in *IEEE ISSCC Digest of Technical Papers*, pp. 388–389, 2010.
113. G. A. Fahmy and M. Zorkany, "Design of a memristor-based digital-to-analog converter," *Electronics*, vol. 10, no. 5, pp. 1–17, 2021.
114. Y. Chen, Y. Zhuang, and H. Tang, "A highly energy-efficient, area-efficient switching scheme for SAR ADC in biomedical applications," *Analog Integrated Circuits and Signal Processing*, vol. 101, no. 1, pp. 133–143, 2019.
115. S. Chaput, D. Brooks, and G. Y. Wei, "An area-efficient 8-bit single-ended ADC with extended input voltage range," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 11, pp. 1549–1553, Nov. 2018.
116. T. Yousefi, A. Dabbaghian, and M. Yavari, "An energy-efficient DAC switching method for SAR ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 1, pp. 41–45, Jan. 2018.
117. Z. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, and R. P. Martins, "A 6-to-10-bit 0.5–0.9 V reconfigurable 2 MS/s power-scalable SAR ADC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 689–696, 2015.
118. R. Inanlou and M. Yavari, "A simple structure for noise-shaping SAR ADC in 90 nm CMOS," *AEU-Int. J. Electron. Commun.*, vol. 69, no. 8, pp. 1085–1093, 2015.
119. P. Harpe, E. Cantatore, and A. van Roermund, "An oversampled 12/14-bit SAR ADC with noise reduction achieving 79.1 dB SNDR," in *IEEE ISSCC Digest of Technical Papers*, pp. 194–195, 2014.
120. C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 100 MS/s 1.13 mW SAR ADC with binary-scaled error compensation," in *IEEE ISSCC Digest of Technical Papers*, pp. 386–387, 2010.
121. V. Giannini, P. Nuzzo, V. Chironi, A. Baschiroto, G. Van der Plas, and J. Craninckx, "An 820- μ W 9-bit 40-MS/s noise-tolerant dynamic SAR ADC in 90-nm digital CMOS," *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, pp. 238–239, 2008.

122. S. A. Mahmoud, H. A. Salem, and H. M. Albalooshi, "An 8-bit 10-kS/s 1.87- μ W SAR ADC in 0.25- μ m CMOS for ECG detection systems," *Circuits Syst. Signal Process.*, vol. 34, pp. 2419–2439, 2015.
123. C.-C. Liu, S.-J. Chang, G.-Y. Huang, Y.-Z. Lin, and C.-M. Huang, "A 1-V 11-fJ/conversion-step 10-bit 10-MS/s asynchronous SAR ADC in 0.18- μ m CMOS," *Proc. Symp. VLSI Circuits*, pp. 241–242, Jun. 2010.
124. Z. Ding, X. Zhou, and Q. Li, "A 0.5–1.1-V adaptive bypassing SAR ADC utilizing oscillation-cycle information of a VCO-based comparator," *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 968–977, Apr. 2019.
125. J. Guerber, H. Venkatram, M. Gande, and U. Moon, "A 10-bit ternary SAR ADC with quantization-time information utilization," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2604–2613, Nov. 2012.
126. T.-Y. Wang, H.-Y. Li, Z.-Y. Ma, Y.-J. Huang, and S.-Y. Peng, "A bypass-switching SAR ADC with a dynamic proximity comparator for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1743–1754, Jun. 2018.
127. F. M. Yaul and A. P. Chandrakasan, "A 10-bit SAR ADC with data-dependent energy reduction using LSB-first successive approximation," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2825–2834, Dec. 2014.
128. D. Osipov and S. Paul, "Two-step reset method for energy-efficient SAR ADC switching schemes," *Electron. Lett.*, vol. 52, no. 10, pp. 816–817, 2016.
129. X. Tong and M. Ghovanloo, "Energy-efficient switching scheme in SAR ADC for biomedical electronics," *Electron. Lett.*, vol. 51, pp. 676–678, 2015.
130. H. S. Bindra, C. E. Lokin, A.-J. Annema, and B. Nauta, "Range pre-selection sampling technique to reduce input drive energy for SAR ADCs," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, pp. 217–220, 2017.
131. H. S. Bindra, C. E. Lokin, A.-J. Annema, and B. Nauta, "A 4-MS/s 10-bit SAR ADC with integrated class-A buffers in 65-nm CMOS using a single 1.2-V supply," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1–4, 2019.
132. M.-J. Seo, J. Kim, S. Hong, and B. Kim, "A reusable code-based SAR ADC design with CDAC compiler and synthesizable analog building blocks," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 12, pp. 1904–1908, 2018.
133. P. Harpe, E. Cantatore, and A. van Roermund, "A 2.2/2.7-fJ/conversion-step 10/12-bit 40-kS/s SAR ADC with data-driven noise reduction," *IEEE ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, pp. 270–271, 2013.
134. X. Tong, J. Liu, and M. Ghovanloo, "A 0.6-V 12-bit 13.2-fJ/conversion-step SAR ADC with time-domain VCDL-based comparator," *Microelectronics Journal*, vol. 122, Art. no. 105406, 2022.
135. A. K. Dubey and R. K. Nagaria, "Low-power high-speed CMOS double-tail dynamic comparator," *Analog Integr. Circuits Signal Process.*, vol. 101, pp. 307–317, 2019.

136. M. Cao and W. Tang, "The high-speed low-power dynamic comparator," *J. Phys.: Conf. Ser.*, vol. 2113, Art. no. 012064, 2021.
137. P. Harpe, E. Cantatore, and A. van Roermund, "A 0.7-V 7-to-10-bit 0–4-MS/s flexible SAR ADC for ultra-low-power sensors," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3018–3028, 2013.
138. K. Vora and N. Sun, "A 12-bit digital-assisted SAR ADC using adaptive calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1465–1474, Sept. 2016.
139. X. Zhao and N. Sun, "A 13-bit 2.5-MS/s SAR ADC with background digital calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 7, pp. 1008–1017, Jul. 2016.
140. H. K. Hong, H. W. Kang, and C. H. Kim, "A 62-dB SNDR 40.2- μ W 10-MS/s ADC for IoT and biomedical systems," *Proc. IEEE ISCAS*, Seville, Spain, pp. 1–4, 2020.
141. S. Konwar, A. Roy, and S. Wairya, "Deterministic dithering-based 12-bit 8-MS/s SAR ADC in 0.18- μ m CMOS," *IEEE Solid-State Circuits Letters*, vol. 5, pp. 243–246, 2022.
142. M.-J. Tsai and Y.-Z. Lin, "A 6-bit 2.5-GS/s time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1015–1026, Apr. 2017.
143. N. Rai, A. Yadav, and S. Wairya, "Design of a high-speed low-power charge-sharing dynamic comparator," *Proc. ICACFCT*, Meerut, India, pp. 125–130, 2021.
144. H. Hong, J. Lee, and G. Cho, "A 10-bit 200-MS/s low-power SAR ADC with timing-error-tolerant asynchronous control," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2928–2938, Dec. 2015.
145. C.-C. Liu, S.-J. Huang, and Y.-Z. Lin, "A 12-bit 3-MS/s redundant SAR ADC with digital error correction," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 8, pp. 602–606, Aug. 2014.
146. C.-C. Liu, S.-J. Chang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a power-efficient quasi-asynchronous architecture," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 7, pp. 1532–1541, 2010.
147. D. Zhang, A. Bhide, and A. Alvandpour, "A 14-bit 200-MS/s subrange SAR ADC with pipelined structure," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 4, pp. 809–820, 2016.
148. Y. Zhu, C. H. Chan, U. F. Chio, S. W. Sin, S. P. U, and R. P. Martins, "A 10-bit 100-MS/s reference-free SAR ADC with nonbinary redundant calibration," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 7, pp. 1531–1541, 2011.
149. S. Shikata, Y. Osaki, T. Miki, and Y. Matsuzawa, "A 1.4-GS/s 12-bit time-interleaved SAR ADC with background timing skew calibration," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2920–2930, 2016.

150. S. Oh, M. Choi, S. Jeong, and S. Cho, "A 0.6-V 12-bit 13.2-fJ/conversion-step SAR ADC with time-domain comparator," in *IEEE ISSCC Digest of Technical Papers*, pp. 474–475, 2014.
151. Y. Huang, X. Zhang, and Z. Zhu, "A high-speed low-power SAR ADC in 40-nm CMOS using combined energy-efficient techniques," *IEICE Electronics Express*, vol. 18, no. 11, 2021.
152. Z. Song, Y. Liu, and X. Wang, "An ENOB 10.3-bit 103- μ W on-chip calibration SAR ADC," *Journal of Physics: Conference Series*, vol. 2524, Art. no. 012019, 2023.
153. T. Morie, T. Miki, and Y. Matsuzawa, "A 71-dB SNDR 50-MS/s 4.2-mW CMOS SAR ADC," in *IEEE ISSCC Digest of Technical Papers*, pp. 272–273, 2013.
154. T. Lee, J. Kim, and S. Cho, "A multimodal neural-recording IC with reconfigurable analog front-ends," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 16, no. 2, 2022.
155. Z. Li, X. Tang, and N. Sun, "A SAR ADC with reduced kT/C noise by decoupling noise PSD and bandwidth," in *Proc. IEEE Symp. Circuits*, pp. 1–4, 2020.
156. S. Xue, "An energy-efficient Flash–SAR ADC with two-step flash structure in 0.18- μ m CMOS," *Scientific Reports*, 2026.
157. J. Kim, H. Park, and S. Lee, "A 1-V 2-MS/s 8-bit SAR ADC with low switching energy," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, pp. 1120–1123, 2017.

LIST OF PUBLICATIONS

SCI/SCIE Indexed Journal Papers Published (03)

1. Mohit Tyagi, Poornima Mittal and Parvin Kumar, “Design of 8 -bit low power SAR ADC in 45nm for biomedical implants”, *Physica Scripta (IOP Sciences)*, vol. 98, pp. 116101, 2023 (**Impact Factor: 2.6**), doi :10.1088/1402-4896/ad01f7.
2. Mohit Tyagi, Poornima Mittal and Parvin Kumar, “Performance Optimization of SAR ADC using Dynamic Controlled Comparator at 45 nm Technology for Biomedical and IoT Applications”, *Wireless & Personal Communications (Springer)*, vol. 134, pp. 1035-1057, 2024 (**Impact Factor: 2.2**), doi: 10.1007/s11277-024-10971-1.
3. Mohit Tyagi, Poornima Mittal and Parvin Kumar, “Design of a low-power dynamic latched comparator for biomedical applications”, *Physica Scripta (IOP Sciences)*. vol. 100, pp. 016103, 2025 (**Impact Factor: 2.6**), doi: 10.1088/1402-4896/ad9b55.

Papers Submitted in SCI/SCIE International Journals (02)

1. Mohit Tyagi, Poornima Mittal and Parvin Kumar, “A Comprehensive Review on Recent Advances in SAR ADC Design: Circuits, Architectures, and Simulation”, *Integration-The VLSI Journal (Elsevier, Manuscript Id: VLSIJ-D-26-00473)*.
2. Mohit Tyagi, Poornima Mittal and Parvin Kumar, “ Design and Analysis of Single Ended SAR ADC for Biomedical Signal Processing Applications”, *Arabian Journal for Science and Engineering (Springer, Manuscript Id: AJSE-D-26-05062)*.

International Conference Papers (03)

1. Mohit Tyagi, Poornima Mittal, “MOSFET based Comparator with static reduction logic for SAR ADC in biomedical applications”, *International Conference on Recent Trends in Communication & Electronics (ICCE-2020)*, organized by KIET Group of Institutions, Delhi-NCR, Ghaziabad, UP, 28-29 Nov 2020. (**Taylor & Francis**), Scopus Indexed.
2. Mohit Tyagi, Poornima Mittal and Parvin Kumar, “Simulation and comparative analysis of dynamic comparators at 1MHz for biomedical applications”, *IEEE International Conference on Issues and challenges in Intelligent Computing Techniques (ICICT 2022)*, organized by

KIET Group of Institutions, Delhi-NCR, Ghaziabad, India, Nov 11-12,2022 (**IEEE, Scopus Indexed**).

3. Mohit Tyagi, Poornima Mittal and Parvin Kumar, “Design of ultra-low power dynamic comparator with resolution 2.5 mV for SAR ADC,” 9th International Conference on Microelectronics and Telecommunications Engineering (**ICMETE 2025**), organized by Department of Electronics & Communication Engineering, SRM Institute of Science and Technology, Delhi-NCR Campus, Ghaziabad, UP, India, December 4th -5th 2025. (**Springer Nature Link**).



PAPER

Design of 8-bit low power SAR ADC in 45 nm for biomedical implants

Mohit Tyagi^{1,2}, Poornima Mittal¹  and Parvin Kumar²¹ Department of Electronics and Communication Engineering, Delhi Technological University, Delhi-110042, India² Department of Electronics and Communication Engineering, KIET Group of Institutions, Delhi-NCR, Ghaziabad, 201206, India

* Author to whom any correspondence should be addressed.

E-mail: mohit.tyagi@kiet.edu, poornimamittal@dtu.ac.in and parvin.kaushik@kiet.edu**Keywords:** successive approximation register (SAR) – analog to digital converters (ADC), digital to analog converter (DAC), sample & hold circuitry (S&H), integral non-linearity (INL), differential non-linearity (DNL)**Abstract**

The utilisation of low power SAR (Successive Approximation Register) Analog-to-Digital Converters holds significant importance in the domain of bio-medical signal acquisition. The present study showcases the utilisation of an 8-bit CMOS SAR-ADC for integration into the analog front end of bio-signal acquisition. The focus of this technology pertains to the monitoring of implanted bio-signal devices, with a specific emphasis on ECG/EEG signals. A capacitive digital-to-analog converter (DAC) is suggested as a means to attain power consumption in the microwatt range. This approach enables comparisons to be made without any energy consumption, leading to a substantial enhancement in energy efficiency. Furthermore, a comprehensive theoretical examination of comparator offset voltages has been conducted to enhance the offset performance of the comparator operating at low supply voltage. The analysis indicates that optimization of the comparator is achieved solely through the adjustment of transistor sizes, without the implementation of any specific offset cancellation techniques. Simulations indicate that the optimization of the offset voltage to approximately 5 mV occurs when there is variation in the common-mode input voltage at a 1 V supply. The proposed Analog-to-Digital Converter (ADC) layout has been successfully executed utilizing the 45 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology. The Analog-to-Digital Converter (ADC) attains a Spurious-Free Dynamic Range (SFDR) of 64.02 dB and consumes 1.9 μ W of power at a sampling rate of 1.1 MHz and a supply voltage of 1 V.

1. Introduction

As CMOS technology advances, there is a greater need for integrated low power cardiac implanted medical devices such as defibrillators as well as pacemakers. It demands circuit implementation with low power consumption for these biomedical devices. The state-of-the-art for low-power bio-signal acquisition and processing is generally recognized as being a physiologically detecting analog front-end (AFE), which consists of a low-noise amplification circuit, an ADC, and prime actual bio-feature filters utilizing analog circuitry [1, 2].

Analog-to-Digital Converters represent the most power hungry and crucial component in monitoring cardiovascular signals among the different components present in implanted devices. Biomedical cardiac signals require analog to digital converter to perform with medium to high resolution at low to medium speed conditions [3]. As a result, creating an ADC in cardiac devices with minimal power consumption and satisfying the required conversion precision is a significant problem. In this view, low power Architecture design of 8-bit SAR ADC is the best choice to design among the available ADC architectures like flash, delta-sigma and two step ADCs due to the simple construction of SAR ADC along with the usage of maximum digital circuitry in its implementation [4]. Technology scaling has reduced the energy consumption of ADC to a great extent. The energy efficiency of ADC is characterised by a Walden figure of merit as:



Performance Optimization of SAR ADC using Dynamic Controlled Comparator at 45 nm Technology for Biomedical and IoT Applications

Mohit Tyagi^{1,2} · Poornima Mittal¹ · Parvin Kumar²

Accepted: 10 March 2024 / Published online: 30 March 2024

© The Author(s), under exclusive licence to Springer Science+Business Media, LLC, part of Springer Nature 2024

Abstract

The Emerging biomedical applications such as electrocardiography, electroencephalogram, wireless implantable devices have required optimized power-based SAR ADC in them to reduce package cost and to extend battery life. In view of power optimized SAR ADC, a dynamic controlled comparator with novel static power reduction logic incorporated with common mode kickback noise reduction technique is designed at 45 nm technology in CADENCE Virtuoso in this paper. Designed comparator is analyzed in terms of performance parameters; static power dissipation, transient power dissipation, maximum sampling rate, offset voltage and delay. Simulation and behaviour modeling analyses of proposed dynamic comparator has resulted in five times reduction in static power dissipation along with optimization of transient power and sampling rate as well compared to previously available double tail dynamic comparator. Moreover, it has been mentioned that proposed dynamic comparator is dissipating 2.36 pW of static power and 3.59 nW of transient power with sampling rate of 240 KS/s at 0.5 V. Further, the kickback noise of proposed design is limited to 4.7 mV with maximum delay of 124 ps. Finally, the novel outcomes of proposed comparator are the optimization in required parameters such as power, delay, offset voltage and kickback noise for biomedical applications as compared to double tail dynamic comparator. The proposed consideration for SAR ADC can become a backbone for low power biomedical applications.

Keywords Controlled dynamic latched comparator · Low voltage · Static power · Double tail dynamic comparator · Power consumption · Internet of things (IoT) · Kickback noise · Offset voltage

✉ Poornima Mittal
poornimamittal@dtu.ac.in

Mohit Tyagi
mohit.tyagi@kiet.edu

Parvin Kumar
parvin.kaushik@kiet.edu

¹ Department of Electronics and Communication Engineering, Delhi Technological University, Delhi 110042, India

² Department of Electronics and Communication Engineering, KIET Group of Institutions, Delhi-NCR, Ghaziabad 201206, India



PAPER

Design of a low-power dynamic latched comparator for biomedical applications

Mohit Tyagi^{1,2} , Poornima Mittal^{1,*} and Parvin Kumar² ¹ Department of Electronics and Communication Engineering, Delhi Technological University, Delhi-110042, India² Department of Electronics and Communication Engineering, KIET Group of Institutions, Delhi-NCR, Ghaziabad, 201206, India

* Author to whom any correspondence should be addressed.

E-mail: mohit.tyagi@kiet.edu, poornima2822@gmail.com and parvin.kaushik@kiet.edu**Keywords:** latched comparator, ADC topologies, cardiac IMDs, 45-nm CMOS technology, power delay product (PDP), biomedical applications**Abstract**

The latched comparator is a fundamental component of all ADC topologies. Thermal noise, kickback noise, and offset voltage impact the energy efficiency of the comparator significantly. In cardiac IMD ADCs, latched comparator kickback noise may impact resolution, accuracy, and settling time. This paper describes the design and development of an a low-power dynamic latched comparator optimised for biomedical applications and running at 1V. The suggested comparator is achieved on a 45 nm CMOS technology node, having the main goal of reducing kickback noise. The main concept of the recommended comparator has been utilizing the novel resetting approach and kickback noise reduction approach to preserve the charge and kickback noise, respectively. This approach aids in minimizing delay, power consumption, and kickback noise using shared charging logic. The charging-sharing technique involves using a single-pass transistor positioned across two output nodes. The pass transistor distributes the charge evenly across two output nodes throughout the reset phase. Due to the shared charging of the load capacitances, the voltage at the output nodes would not drop under the threshold value. As a result, the input signal could be evaluated more quickly during the regenerative stage. The comparator's delay is calculated using a rigorous statistical analysis considering the circuit's random factors. The offset of the proposed comparator is verified using thorough Monte Carlo simulations. The comparator reduces power while preserving noise. Also, the measured simulation results of recommended comparator outperform state-of-the-art comparators regarding kickback noise, delay, power consumption, and power delay product (PDP). The input voltage inversely affects the comparator's delay. Further, the simulation shows that the comparator consumes 9.36 μ W at 1 V and 1 GHz sampling frequency. The simulation results confirm that the suggested comparator effectively reduces power consumption by at least 66.98%. The proposed comparator has less PDP value by 44.44%. Also, suggested comparator effectively reduces offset voltage by 7.6% but with a corresponding increase in the area by 5%. Additionally, the comparator successfully reduces kickback noise by 44.6%. The obtained results are not silicon proven and bound to be in the pre-silicon stage. The low-power behaviour of the suggested technique is validated using analytical derivations, PVT corner analysis, and post-layout simulation.

1. Introduction

The semiconductor sector has experienced substantial expansion and is currently extensively utilised in several domains owing to its unique circuitry, which offers solutions for a diverse array of biomedical applications. In the present electronic era, a multitude of applications incorporates an analog to digital converter for transforming analog signal information into its equivalent digital code, thereby facilitating the transmission and storage of digital data. The growing demand for electronic devices that consume less power has led to the

MOSFET based comparator with static reduction logic for SAR ADC in biomedical applications and its comparison with conventional comparator

Mohit Tyagi

KIET Group of Institutions, Delhi-NCR, India

Poornima Mittal

Delhi Technological University, New Delhi

ABSTRACT: In this paper we have designed and compared MOSFET based conventional comparator (without static power reduction logic) and controlled comparators (with static power reduction logic) for Low Power SAR ADC at 45nm technology. The peculiar advantage obtained after simulating controlled comparator with conventional comparator is power consumption gets reduced by forty four times with almost same propagation delay as of conventional comparator. Both comparators are simulated at 0.6V in 45nm CADENCE Virtuoso technology node. Dynamic power dissipation has come out to be 1.6u and 20u for conventional and controlled comparator respectively. Simulated controlled comparator is suitable for comparison of two signals of the order of 50 MHz frequency range. Minimum voltage difference between two signals to be compared is 0.3 volt for conventional comparator and its value is 0.2 volt for controlled comparator.

Keywords: SAR ADC, conventional comparator, controlled comparator, SNR

1 INTRODUCTION

ADC needs to be optimized for ultra-low power applications. A SAR ADC comprises of an assortment of vital blocks; such as, comparator, ring counter, DAC and controlling unit. Though, the power optimization of each individual module is imperative, nevertheless, for now conventional MOSFET based comparator and comparator with static power reduction using controlled comparators are designed and compared to achieve an efficient one for ultra-low power SAR ADC.

(Goll B. et al. 2000) has worked on a comparator with reduced delay time in 65nm CMOS for supply voltage reduced to 0.65V. Further, (Cheong Jia Hao et al. 2011) designed a SAR ADC based on trilevel switching scheme and time domain comparison for biomedical application. Further, (Harpe Pieter et al. 2013) worked on segmented charge redistribution DAC for sensor applications. (Ahmadi et al. 2015) has developed an accurate and simple model to accomplish the noise analysis of comparator so as to model the noise effect which may deteriorate the performance of SAR ADC. Further, (Wang et al. 2018) has developed a dynamic proximity comparator for bypass switching SAR ADC.

Simulation and Comparative Analysis of Dynamic Comparators at 1MHz for Biomedical applications

Mohit Tyagi
Department of Electronics and
Communication Engineering
KIET Group of Institutions,
Ghaziabad, India
mohit.tyagi@kiet.edu

Poornima Mittal
Delhi Technological University,
New Delhi, India
poornimamittal@dtu.ac.in

Parvin Kumar
Department of Electronics and
Communication Engineering
KIET Group of Institutions,
Ghaziabad, India
parvin.kaushik@kiet.edu

Abstract— SAR ADC is one of the most demanding Analog to digital converter for medium speed, medium resolution applications like ECG, EEG, and related biomedical applications. In this paper we have designed and simulated the dynamic comparators with noise rejection and amplification capability in CADENCE Virtuoso 45 nm technology node. Designed Comparators are simulated at 0.8V and various parameters like power dissipation, maximum operating frequency, delay and offset voltage are compared. Designed comparators are well employable in SAR ADC with maximum operating frequency of 1MS/s. comparators are operated at varying supply voltage from 0 to 1 V. Basic comparator dissipates 9.17 pW as static power and 520.2 nW as dynamic power at VDD of 1 V and INN, INP difference of 0.9 V. Compared to basic comparator, dynamic comparator with tail transistors can be operated at 0.5 V with static power of 4.143 pW and 3.720 nW as dynamic power dissipation. Operating frequency of designed comparators is of 1 MHz with propagation delay of 522 ns by dynamic comparator with tail transistors and 480 ns as of basic comparator.

Keywords— Successive Approximation Register (SAR) – Analog to Digital Converters (ADC), Digital to Analog Converter (DAC), Supply Voltage (VDD), Propagation delay (tpd).

I. INTRODUCTION

The biomedical electronics is one of the most interested domain for the researchers in the present scenario due to its significant features and widespread capability for the healthy society [1]. A single portable device comes with the best features to present significant health parameters required to monitor health condition [2]. Analog to digital converters are designed using improved CMOS technology to achieve better sampling rates with high power efficiency [3, 4]. Multiple switching schemes have been incorporated in ADC design to improve power efficiency [5]. By creating a window to locate input voltage in a specific range bypass logic is of prominent importance in such designs [6].

In the design of ultra-low power SAR ADC, the design of its comparator module holds great point of concern for the designers. We must have power optimized comparator with noise rejection and preamplification capabilities for the design of are an essential block of ADC that is used to reduce the power consumption in an efficient manner. Among available ADCs, SAR ADC is most widely used in energy efficient applications which make them prominent choice in biomedical domain [7]. Further, dynamic comparators are also referred to as clocked comparators.

Full scale digital level output is achieved by the positive feedback achieved by the ring structure of connected back-to-back inverter blocks.

Zhang, et al. [8] proposed an innovative 12-bit dynamic tracking algorithm-based SAR ADC with real-time qrs detection. H. Lu. et al. [9] worked on the data-dependent energy reduction algorithm for SAR ADC using self-adaptive window. Furthermore, (Q. Fan et al. [10] worked on a time-interleaved SAR ADC With bypass-based opportunistic Adaptive Calibration. J. Li et al. [11] explored an energy-efficient switching scheme with low common-mode voltage variation and no-capacitor-splitting DAC for SAR ADC. N. Guangshan et al. [12] worked on research progress of time interleaved analog to digital converters.

This paper shows the designing and comparative analysis of dynamic comparator structures. Further Section 2 includes the different architecture of dynamic comparators. Results and Simulation Analysis is presented in section 3. Lastly, Conclusion is given in section 4.

II. ARCHITECTURE OF DYNAMIC COMPARATORS

Comparators are designed with varying architecture diversity in order to reduce the power dissipation and delay of the circuit. Designed Comparators are incorporated with basic preamplification stage with differential stage in order to reject the common mode noise signal.

A. Dynamic Comparator with Tail Transistors

Dynamic comparator with tail transistors employs the two stages of connected transistors M1, M2, M9 and M10 along with M3, M4, M7 and M8 as shown in Fig. 1. Tail Transistors Mtail1 and Mtail2 prevents the direct current path between supply VDD and ground. In this stacking of transistors has been eliminated and due to this it can be used at low voltages. When clock signal (clk) is in logic 0 state, both tail transistors M tail1 and Mtail2 are in off state which eliminates the direct current path but Fp and Fn nodes will be precharged to Vdd in this logic state which in turn turns on M5 and M6 and pull down the outn and outp state to logic 0 and this logic 0 state will turn on the M3 and M4 transistors. Further when Clock signal switches to logic 1 i.e. high state outn and outp switches to logic high. Now, INN and INP are the input voltages to be compared. If $INN > INP$, in this case outn will be discharged at slower rate compared to outp which in turn makes outp to discharge at faster rate. Transient behaviour of comparator is shown in Fig. 2.



CRC PRESS
Taylor & Francis Group



KIET
GROUP OF INSTITUTIONS

Affiliated to Dr. A.P.J. Abdul Kalam Technical Univ., Lucknow
Accredited by NAAC with Grade 'A' (5 yrs) | NBA accredited courses
Delhi-NCR, Meerut Road (NH-58), Ghaziabad - 201206



www.aicte-india.org

4th International Conference (Online)
on
Recent Trends in Communication & Electronics (ICCE-2020)
28th-29th November, 2020

Organized by
Department of Electronics & Communication Engineering,
KIET Group of Institutions, Delhi-NCR, Ghaziabad (U.P.) - 201206

CERTIFICATE

This is to certify that Mr./Ms./Dr. Mohit Tyagi of
KIET Group of Institutions, Delhi-NCR, Ghaziabad has presented /attended a paper titled
MOSFET based Comparator with static reduction logic for SAR ADC in biomedical
in the conference.

Sanjay

Dr. Sanjay Sharma
(HoD, ECE)

Mohit Tyagi

A. Garg

Dr. A. Garg
(Director)

Sponsored by :



www.aicte-india.org





KIET
GROUP OF INSTITUTIONS
Connecting Life with Learning



NIRF-2022
Engineering Rank - 187
Pharmacy Rank Band - 97



Accredited by
NAAC with Grade "A+"



NBA Accredited Courses
CSE, ECE, EEE, IT, ME, CE, MCA,
MBA and B.Pharm



ARIIA
3rd Rank
"Private Institutions (Technical)"
in India by ARIIA 2021 Ranking



Diamond Rating with QS I-GAUGE
An exemplary ode to quality
education

3rd International Conference
Issues & Challenges in Intelligent Computing Techniques



ICICT-2022

11th & 12th November 2022

Organized by Department of Information Technology

This is to certify that Dr./Mr./Ms. Mohit Tyagi of
Delhi Technological University, Delhi-110042 (India)

has presented a paper titled Simulation and Comparative Analysis of Dynamic Comparators at 1MHz for SAR ADC in Biomedical Applications in the conference.

Dr. Jitendra Kr. Seth
(Conference Convener)

Dr. Adesh Kr. Pandey
(Conference Chair)

Mohit Tyagi

Dr. A Garg
(Director)

Paper Id-02

CERTIFICATE OF APPRECIATION

Presented to

Mohit Tyagi, Poornima Mittal, Parvin Kumar

has presented a paper on

"Design of Ultra Low Power Dynamic Comparator with Resolution 2.5 mV for SAR ADC"

in the 9th International Conference on

"Micro-electronics and Telecommunication Engineering" (ICMETE 2025)

organized by the Department of Electronics and Communication Engineering,
SRM Institute of Science and Technology, Delhi-NCR Campus, Ghaziabad, U.P., India on
4th-5th December 2025.


Dr. Rupali Singh

HOD / Conference Organizing Co-Chair


Dr. R.P. Mahapatra
Dean



DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Shahbad Daultapur, Main Bawana Road, Delhi-42

PLAGIARISM VERIFICATION

Title of the Thesis: **DESIGN AND PERFORMANCE ANALYSIS OF SAR ADC FOR
LOW POWER APPLICATIONS**

Total Pages: **178**

Name of the Scholar: **Mr. Mohit Tyagi**

Supervisor (s):

(1) **Prof. Poornima Mittal**, Professor, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, India

(2) **Prof. Parvin Kumar**, Department of Electronics and Communication Engineering, Krishna Institute of Engineering & Technology (KIET), Ghaziabad, Delhi-NCR, Uttar Pradesh, India.

Department: **Electronics and Communication Engineering**, Delhi Technological University

This is to report that the above thesis was scanned for similarity detection. Process and outcome is given below:

Software used: **Turnitin**

Similarity Index: **5%**

Total Word Count: **52,899**

Date: 28-04-2026

A handwritten signature in blue ink, appearing to be 'Mohit Tyagi'.

Candidate's Signature

A handwritten signature in blue ink, appearing to be 'Kaushik'.

Signature of Joint Supervisor

A handwritten signature in blue ink, appearing to be 'Poornima'.

Signature of Supervisor

Poornima Mittal

Final Thesis_Print

 Thesis backup

Document Details

Submission ID

trn:oid:::27535:137215928

Submission Date

Apr 30, 2026, 5:26 PM GMT+5:30

Download Date

Apr 30, 2026, 5:35 PM GMT+5:30

File Name

Final Thesis_Print.pdf

File Size

6.8 MB

178 Pages

52,899 Words

272,234 Characters



5% Overall Similarity

The combined total of all matches, including overlapping sources, for each database.

Filtered from the Report

- Bibliography
- Quoted Text
- Cited Text
- Small Matches (less than 10 words)

Exclusions

- 5 Excluded Sources

Match Groups

- 180 Not Cited or Quoted 5%**
Matches with neither in-text citation nor quotation marks
- 0 Missing Quotations 0%**
Matches that are still very similar to source material
- 0 Missing Citation 0%**
Matches that have quotation marks, but no in-text citation
- 0 Cited and Quoted 0%**
Matches with in-text citation present, but no quotation marks

Top Sources

- 2% Internet sources
- 3% Publications
- 2% Submitted works (Student Papers)

Integrity Flags

0 Integrity Flags for Review

Our system's algorithms look deeply at a document for any inconsistencies that would set it apart from a normal submission. If we notice something strange, we flag it for you to review.

A Flag is not necessarily an indicator of a problem. However, we'd recommend you focus your attention there for further review.

Match Groups

- 180 Not Cited or Quoted 5%**
Matches with neither in-text citation nor quotation marks
- 0 Missing Quotations 0%**
Matches that are still very similar to source material
- 0 Missing Citation 0%**
Matches that have quotation marks, but no in-text citation
- 0 Cited and Quoted 0%**
Matches with in-text citation present, but no quotation marks

Top Sources

- 2% Internet sources
- 3% Publications
- 2% Submitted works (Student Papers)

Top Sources

The sources with the highest number of matches within the submission. Overlapping sources will not be displayed.

- 1** Student papers
Uttar Pradesh Technical University on 2025-07-01 <1%
- 2** Internet
labs.engineering.asu.edu <1%
- 3** Publication
Sanjay Sharma, Astik Biswas, Brajesh Kumar Kaushik, Vibhav Sachan. "Recent Tre... <1%
- 4** Internet
internationalpubs.com <1%
- 5** Internet
idr.nitk.ac.in <1%
- 6** Student papers
South University of Science and Technology of China on 2024-10-08 <1%
- 7** Internet
gyan.iitg.ac.in <1%
- 8** Publication
Jinka Pradeep, Tirumala Ramashri. "Design of CMOS 45nm SAR ADC for ECG Signa... <1%
- 9** Publication
Babita Jajodia, Anil Mahanta, Shaik Rafi Ahamed. "Energy-Efficient DAC Switching ... <1%
- 10** Student papers
CSU, San Jose State University on 2020-11-11 <1%

Handwritten signatures: dt, Kaushik, Babita

11	Publication	Gusev, Aleksandr. "Adiabatic Charging in SAR ADCs", Universitaet Bremen (Germ...	<1%
12	Internet	core.ac.uk	<1%
13	Internet	tudr.thapar.edu	<1%
14	Student papers	University of Macau on 2020-07-18	<1%
15	Student papers	PEC University of Technology on 2022-05-19	<1%
16	Publication	Chung, Chi-Heng. "The Design of two Low Power 10-bit/12-Bit 100-KS/s Hybrid/Spl...	<1%
17	Student papers	CSU, Long Beach on 2024-03-19	<1%
18	Publication	Wu, Brian G.. "Computationally Efficient Order Identification for Models of Big Ti...	<1%
19	Publication	Talluri, Ashmitha. "Design, Implementation, and Analysis of a Low-Power Success...	<1%
20	Publication	Tejender Singh, Suman Lata Tripathi. "Design of a 16-bit 500-MS/s SAR-ADC for Io...	<1%
21	Student papers	Thapar University, Patiala on 2017-06-20	<1%
22	Publication	MoonHyung Jang, Xiyuan Tang, Yong Lim, John G. Kauffman, Nan Sun, Maurits Or...	<1%
23	Publication	Zhangming Zhu, Yuhua Liang. "A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-<f...	<1%
24	Student papers	Indian School of Mines on 2020-05-08	<1%

25	Publication	M. Vafaei, M.R. Hosseini, E. Abiri, M.R. Salehi. "A 0.2-V 1.2nW 1-KS/s SAR ADC with ...	<1%
26	Publication	Armin Tehranian, Ali Peiravi. "A 10-bit 33.3-kS/s 3.2-fJ/conversion-step single-ende...	<1%
27	Student papers	National Taiwan University on 2022-09-18	<1%
28	Publication	Sun, Lei. "High Performance SAR-based ADC Design in Deep Sub-micron CMOS.", ...	<1%
29	Student papers	Associatie K.U.Leuven on 2016-06-07	<1%
30	Publication	Chi-Chang Lu, Ding-Ke Huang. "A 10-Bits 50-MS/s SAR ADC Based on Area-Efficient...	<1%
31	Internet	www.repository.cam.ac.uk	<1%
32	Publication	Chen, Ping-Liang. "Single-Ended Rail-to-Rail Low Power SAR ADC Design.", Proque...	<1%
33	Publication	Ganji, Mona. "Analog and Mixed-signal Design and Test Techniques for Improved ...	<1%
34	Student papers	UT, Dallas on 2013-05-24	<1%
35	Student papers	Indian Institute of Technology on 2018-05-01	<1%
36	Publication	Suman Lata Tripathi, Sobhit Saxena, Sushanta Kumar Mohapatra. "Advanced VLSI...	<1%
37	Internet	ebin.pub	<1%
38	Student papers	Visvesvaraya National Institute of Technology on 2017-05-25	<1%




39	Student papers	Visvesvaraya Technological University on 2014-10-16	<1%
40	Publication	Junhua Shen, Akira Shikata, Anping Liu, Baozhen Chen, Frederick Chalifoux. "A 12...	<1%
41	Publication	Koçak, Serhat. "A Low-power Succesive Approximation Register Analog-To-Digital...	<1%
42	Publication	Robert Simpson. "Lighting Control - Technology and Applications", Routledge, 2019	<1%
43	Student papers	University of Glasgow on 2024-04-24	<1%
44	Publication	Al-Obaidi, Zainab M.. "The Vertebral Endplate-Facet Joint Complex: New Insights i...	<1%
45	Publication	Fatah Mochamad, Rian. "Stability Assessment of Uncertain AC/DC System", The U...	<1%
46	Publication	Hanoi National University of Education	<1%
47	Publication	Hongshuai Zhang, Hong Zhang, Yan Song, Ruizhi Zhang. "A 10-Bit 200-kS/s 1.76- μ W...	<1%
48	Student papers	University of Macau on 2015-04-21	<1%
49	Student papers	University of Macau on 2016-08-23	<1%
50	Publication	Xie, Tian. "Signal-Chain Optimized Analog-To-Digital Converter Design.", Georgia I...	<1%
51	Internet	tdr.lib.ntu.edu.tw	<1%
52	Internet	www.journal.uestc.edu.cn	<1%




53	Publication	Akbarzadeh, Mehdi. "Non-Contact Acoustic Excitation and Associated Nonlinear ..."	<1%
54	Publication	Anurag Yadav, Subodh Wairya. "Performance and Design analysis of High Speed ..."	<1%
55	Student papers	Bogazici University on 2023-09-16	<1%
56	Publication	Chen, Kairang. "Energy-Efficient Data Converters for Low-Power Sensors", Linkopi...	<1%
57	Publication	Deepika Kumaradasan, Sougata Kumar Kar, Santanu Sarkar. "An 8-bit 100 kS/s Lo..."	<1%
58	Publication	Espejo, Caterina M.. "Computationally Inexpensive Parallel Parking Supervisor Ba..."	<1%
59	Publication	John D. Cressler, H. Alan Mantooth. "Extreme Environment Electronics", CRC Pres...	<1%
60	Student papers	KTH - The Royal Institute of Technology on 2014-09-28	<1%
61	Publication	Marcel J.M. Pelgrom. "Analog-to-Digital Conversion", Springer Science and Busine...	<1%
62	Publication	Naoaki Yamanaka. "High-Performance Backbone Network Technology", CRC Pres...	<1%
63	Publication	Naveen Kandpal, Anil Singh, Alpana Agarwal. "An input signal dependent 8-to-12 ..."	<1%
64	Publication	Pereira, Nuno Ruben Ferreira. "Design of Analog-to-digital Converters with Embe..."	<1%
65	Student papers	Sabancı Universitesi on 2017-08-23	<1%
66	Publication	Sung-En Hsieh, Chih-Cheng Hsieh. "A 0.44-fJ/Conversion-Step 11-Bit 600-kS/s SAR ..."	<1%

Handwritten signatures: Kaushik, Parvina, and another signature.

67	Student papers	University of Newcastle upon Tyne on 2022-08-19	<1%
68	Internet	de.scribd.com	<1%
69	Internet	ele.aut.ac.ir	<1%
70	Internet	era.library.ualberta.ca	<1%
71	Internet	escholarship.org	<1%
72	Internet	iris.unipv.it	<1%
73	Internet	repository.ntu.edu.sg	<1%
74	Internet	www.diva-portal.org	<1%

MOHIT TYAGI

Mohan Niwas, Near Laxmi Narayan
Mandir, Duhai, Ghaziabad, UP, 201001

mohittyagi9634@gmail.com

(+91) 9643142808

OBJECTIVE

I aim to secure a full-time academic role that allows me to contribute meaningfully to research and development in science and technology.

TEACHING EXPERIENCE

SN	Institute Name	Designation	Mode	Duration
1.	KIET (Deemed to be University)	Assistant Professor	Full Time	July 2014 to Present

EDUCATIONAL QUALIFICATIONS

S.No.	Course	Institute	Specialization	Duration	Division
1.	PhD.	Delhi Technological University, Delhi	Low Power VLSI	Pursuing (From December 2018)	Status: Thesis submitted
2.	M. Tech.	NIT Kurukshetra	VLSI Design	2012-2014	1st
3.	B. Tech.	R.D Engineering College, UPTU India	Electronics & Communication Engineering	2007-2011	1st
4.	Intermediate	Dehra Dun Public School, Ghaziabad, UP	Physics, Chemistry, Mathematics, Physical Education, English	2006-2007	1st
5.	High school	Green Land Public School, Ghaziabad, UP	Hindi, English, Mathematics, Science, Social Science	2004-2005	1st

RESEARCH EXPERIENCE

Ph.D. Research Scholar, DTU Delhi (Pursuing from December 2018)

Supervisor: Prof. Poornima Mittal (DTU Delhi).

- Research topic: Design and Performance Analysis of SAR ADC For Low Power Applications
- Published 03 SCI/SCIE research papers as first author.

Post Graduate Student, NIT Kurukshetra (2012-2014)

Supervisor: Dr. Bikash Rout (Assistant Professor (Contract), NIT Kurukshetra).

- Conducted research in PLL Design.
- Successfully designed low power PLL for utilization in clock synchronization.