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STUDY AND DESIGN OF LOW LEAKAGE NANOWIRE FIELD EFFECT TRANSISTOR

Thesis Submitted
in Partial Fulfillment of the Requirements
for the Degree of

DOCTOR OF PHILOSOPHY

by

AAPURVA KAUL
(Enrollment No.: 2K21/PHDEC/15)

Under the supervision of
DR. SONAM REWARI
(Supervisor)
Assistant Professor
DR. DEVA NAND
(Joint Supervisor)
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Shahbad Daulatpur, Main Bawana Road, Delhi-110042, India

October, 2025

ACKNOWLEDGEMENTS

"A veena cannot exist without its strings. A chariot cannot exist without its wheels. No one who achieves success does so without the help of others. The wise and confident acknowledge this help with gratitude."

----Lord Rama

As I stand at the threshold of completing this doctoral journey, I find myself overwhelmed with gratitude and humility. This thesis is not just a document of research and results; it is a story of countless sacrifices, encouragements, prayers, and blessings that carried me through. The people who walked alongside me have illuminated every step of this journey with immense joy, wisdom, support, and love, and it's my honor to take this opportunity to acknowledge them.

First and foremost, I bow my head to the Almighty for granting me life, health, and strength and for filling me with resilience and hope whenever the road seemed difficult. Without his guiding light and divine blessings, none of this would have been possible.

I express my profound gratitude to my supervisor, **Dr. Sonam Rewari**, whose wisdom, brilliance, and patient guidance have been my constant source of inspiration. From the very idea of pursuing doctoral research, she stood by me with conviction, ensuring that I stayed motivated and focused even when the challenges arose. Her unwavering encouragement, her insistence on professionalism, and her gentle yet firm mentorship have shaped me in ways that extend beyond academics. From her, I learned that one should nurture a *wide vision*, embrace it with *courage*, and walk towards it with *humility*. I consider myself truly fortunate to have had her as my guide, and words will fall short of expressing my gratitude towards her.

My heartfelt thanks also go to my joint supervisor, **Dr. Deva Nand**, who has been a mentor in every sense of the word. His immense knowledge, patience, encouragement, and patience enriched my research journey at every step. He was always there through both small hurdles and major challenges, with timely guidance and inspiring words. From him, I learned life's most valuable lessons, I learned how to remain *humble* in all circumstances, and the art of maintaining proper

documentation with *precision*. He has been a true *inspiration* throughout my journey, and no words could ever do justice to the gratitude and respect I hold for him. Having him as a supervisor has been one of the greatest blessings of my academic career.

I am sincerely indebted to the members of my **Doctoral Research Committee (DRC)** for their valuable insights, thoughtful critiques, and constructive suggestions, all of which have greatly enhanced the depth and quality of my research. I also extend my heartfelt thanks to the Head of the Department, **Prof. Neeta Pandey**, along with the faculty and staff of the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi. Their expertise, critical evaluation, and encouragement consistently challenged me to refine my work, think beyond conventional approaches, and venture into new and promising directions.

I would like to express my deepest gratitude to two of my dearest friends, **Dr. Shivani Yadav** and **Mrs. Divya Arora Bhayana**, whose presence has been nothing short of a blessing throughout this journey. **Mrs. Divya Arora Bhayana**, your unwavering support, comforting words, and constant encouragement have always lifted me during moments of doubt. You have been more than a friend; you have been a sister, a confidante, and a steady hand guiding me through challenges, making this path not only easier but also filled with warmth and laughter. To **Dr. Shivani Yadav**, I owe heartfelt thanks for being an endless source of inspiration and positivity. Your wisdom, kind counsel, and ability to see hope even in difficult times have been invaluable. You stood by me with patience and compassion, motivating me to persevere and believe in my strengths when the road ahead seemed uncertain. Together, you both have added meaning, joy, and resilience to this journey. The bond we share goes far beyond friendship; it is a treasure I will carry with me for a lifetime. Without your strength, love, and unwavering faith, this milestone would not have been the same.

My heartfelt gratitude goes to my dearest friends **Dr. Snehlata Yadav**, **Dr. Palak Handa**, **Ms. Yashika Chauhan**, **Mrs. Himanshi Chugh**, **Mr. Vishal Chaudhary**, **Mr. Arjun Kumawat**, **Mr. Rohit Khandekar**, **Mr. Kamal Yadav**, **Mr. Vijay Thakur**, and **Mr. Anil Kumar** for filling my days with colors of joy, laughter, and boundless motivation. Each of you has touched my journey in your own beautiful way, leaving behind memories that I will forever cherish. A special word of love goes

to my **Labbies** WhatsApp Group, whose companionship was like warm light in the moments of darkness. Your endless chatter, playful banter, and comforting words turned even the toughest days into something lighter, reminding me always of the blessing of belonging. You were the melody that tuned my struggles into a song, and the colors that painted my journey of joy. In your laughter, I found strength, in your words, I found hope, and in your presence, I found the courage to keep moving forward. Friends like you are not just companions of the present, but treasures I will carry in my heart for a lifetime.

This dissertation is lovingly dedicated to my family, the roots of my strength, and the wings of my dreams. To my beloved mother, **Mrs. Amita Kaul**, whose dream it always was to see her daughter shine; mumma, this achievement belongs to you more than to me. To my father, **Mr. Sudesh Kaul**, your faith and steady support have been my guiding light. I extend my gratitude to my uncle and aunt, **Mr. Rakesh Kaul** and **Mrs. Sunita Kaul**; your blessings and guidance have been an anchor on this journey. Each of you has shaped me in ways words can never fully capture. My in-laws, **Dr. Rakesh Miskeen** and **Mrs. Sunita Miskeen**, have showered me with care, affection, and guidance, making me feel truly blessed to have such a supportive family. I wish to thank my sister, **Mrs. Aarushi Koul**, and her husband, **Dr. Akshit Peer**, whose affection, support, and constant motivation have always pushed me forward. My brothers, **Mr. Aayush Kaul** (and his wife, **Mrs. Antara Janjire**), and **Mr. Aneesh Kaul**, along with my sister-in-law, **Dr. Aayushi Miskeen**, have been my pillars of encouragement, filling my journey with warmth, care, fun, and joy.

I remain ever thankful to my husband, **Mr. Sidhant Miskeen**, whose love, unwavering support, and patience have been the foundation of my strength. His encouragement and belief in me have made the toughest days bearable and the milestones brighter. To my precious daughter **Aarya Miskeen**, you are the light of my life. Even at such a young age, you bore with my long hours of absence with love and innocence, and your smile was always my greatest source of energy and inspiration. My every achievement is a gift I dedicate to you, with the hope that one day it inspires you to pursue your dreams fearlessly and passionately.

Finally, I bow with gratitude to every individual, whether mentioned here or not, who, directly or indirectly, contributed in any way to my journey. Each of you

holds a part in this accomplishment, and for that, I remain forever indebted.

"Not getting dejected or depressed, skill in doing one's job, and not losing heart in the face of difficulties, these are the qualities which enable one to achieve one's goals."

This work is not only mine but a reflection of the love, sacrifice, and blessings of all those who stood beside me. As ***Maya Angelou*** beautifully said, "***I sustain myself with the love of family***". Truly, this achievement belongs to all of you.

AAPURVA KAUL

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CANDIDATE'S DECLARATION

I **Aapurva Kaul** hereby certify that the work which is being presented in the thesis entitled **"Study and Design of Low Leakage Nanowire Field Effect Transistor"** in partial fulfillment of the requirements for the award of the Degree of Doctor in Philosophy, submitted in the Department of **Electronics and Communication Engineering**, Delhi Technological University is an authentic record of my own work carried out during the period from **August 2021** to **October 2025** under the supervision of **Dr. Sonam Rewari** and **Dr. Deva Nand**.

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Certified that **Aapurva Kaul** (Enrollment No.: 2K21/PHDEC/15) has carried out their research work presented in this thesis entitled **"Study and Design of Low Leakage Nanowire Field Effect Transistor"**, for the award of **Doctor of Philosophy** from the Department of Electronics and Communication Engineering, Delhi Technological University, under my guidance and supervision. The thesis embodies results of original work, and studies are carried out by the student herself and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

Dr. Sonam Rewari
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Dr. Deva Nand
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Place: Delhi
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Dedicated to my Parents, Husband, and Daughter

For their endless love,
support and encouragement

ABSTRACT

The continuous downscaling of semiconductor devices, as predicted by the Moore's law, has significantly improved computational capability, power efficiency and integration density over the past five decades. However, with the transition into the deep sub-nanometer regime, conventional CMOS technology has encountered formidable challenges such as increased leakage currents, degraded subthreshold swing, escalating power dissipation and short channel effects (SCEs). The inability of traditional transistor architectures to maintain electrostatic integrity at reduced dimensions has motivated the exploration of novel device geometries and materials capable of sustaining high performance while ensuring low-power operation.

In this context, the present research investigates the design, modelling and performance evaluation of advanced nanowire field effect transistors (FETs) that combine dielectric, ferroelectric and electrostatic engineering to overcome the limitations of conventional MOSFETs. The study is centred on the progressive development of five distinct nanowire FET architectures, each addressing specific challenges of device scaling through geometric and material innovation. The overarching objective of this work is to achieve superior gate controllability, enhanced current drivability and reduced subthreshold swing, thereby paving the way for energy-efficient transistors suitable for next-generation nanoelectronics applications.

The initial part of the research presents the Double Metal Gate Macaroni Nanowire Field Effect Transistor (DMGM-NFET), where two metals with different work functions are used within the gate stack to modulate the channel potential. This configuration enables a stepwise potential distribution that effectively reduces gate induced drain leakage (GIDL) and drain induced barrier lowering (DIBL). The macaroni type hollow nanowire geometry further enhances gate coupling, allowing improved electrostatic control over the channel region. Simulation results confirm a substantial improvement in subthreshold swing and ON/OFF current ratio when compared to the conventional FETs. This device establishes the foundation for electrostatic optimization through multi metal gating.

Building upon this concept, the study extends to the Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET), which employs a dual-dielectric gate stack consisting of high-κ (HfO_2) and low-κ (SiO_2) materials. The heterogeneous dielectric configuration redistributes the gate electric field, enhancing potential control near the source end while minimizing fringing field effects at the drain. This selective field enhancement results in reduced subthreshold slope and improved channel confinement. Comparative analysis with single-dielectric and single-metal counterparts demonstrates that the hero-dielectric approach yields higher transconductance, improved current and stringer immunity to short channel effects. These findings confirm that dielectric heterogeneity, combined with cylindrical symmetry, can significantly improve device performance at nanoscale dimensions.

The research then transistors from electrostatic to material-based innovation through the incorporation of ferroelectric materials in the gate stack. The Negative Capacitance Nanowire FET (NC-NW FET) introduces a ferroelectric $HfZrO_2$ layer in series with a high-κ dielectric, harnessing the negative capacitance (NC) effect to achieve internal voltage amplification. This phenomenon allows the device to operate with a subthreshold swing below the Boltzmann limit of 60 mV/decade, leading to lower operating voltages and energy efficient switching. The simulation analysis confirms a marked reduction in power dissipation and a significant improvement in drive current. Furthermore, the hysteresis behaviour is optimized through careful tuning of the ferroelectric layer thickness and capacitance matching with the underlying dielectric stack. The results validate that ferroelectric integration can effectively address the fundamental trade-off between switching speed and power consumption in nanoscale transistors.

To further enhance device controllability and eliminate residual instability, the work explores cylindrical ferroelectric architectures, resulting in the Cylindrical Ferroelectric Dual Metal Nanowire FET (C-FE-DM-NW FET). This design combines the advantages of dual metal configuration allows precise control of the potential barrier near the source and drain, while the ferroelectric layer enhances surface potential modulation through polarization-driven voltage amplification. The resulting device exhibits a subthreshold swing below 55 mV/decade, negligible DIBL, and an ON/OFF current ration in the range of 10^8-10^9, confirming excellent electrostatic integrity. Moreover, the transconductance and drain current are significantly improved, validating that the synergy of dual-metal and ferroelectric gate engineering is crucial for achieving both steep-slope and high-drive devices.

The final and most advanced device proposed in this work is the Cylindrical Gate Engineered Ferroelectric Nanowire FET (CGEF-NW FET). This architecture introduces gate-length partitioning and optimized ferroelectric layer placement within the cylindrical structure to achieve near-ideal electrostatic control and hysteresis free operation. The CGEF-NW FET demonstrates an exceptionally low subthreshold swing of approximately 50 mV/decade, a high ON/OFF current ratio exceeding 10^9, and minimal power dissipation. The optimization of gate geometry and ferroelectric parameters allows superior potential modulation while maintaining capacitance stability, thereby providing the most balanced performance among all proposed designs. The CGEF-NW FET thus represents the culmination of this research efforts combining geometry, field and material engineering to achieve a scalable and energy efficient transistor for sub-5 nm technology nodes.

A comprehensive comparative analysis among all the proposed devices illustrates a clear performance improvement trend: the subthreshold swing decreases from approximately 70 mV/decade in the DMGM-NFET to nearly 50 mV/decade in CGEF-NW FET, while the ON/OFF current ratio increases by more than three orders of magnitude. The DIBL is reduced to nearly negligible levels in ferroelectric devices, and the drain current performance is significantly enhanced. These improvements are attributed to the synergistic interplay between electrostatic optimization, dielectric engineering and ferroelectrics voltage amplification, confirming that the strategic integration of these techniques can collectively surpass the scaling limitations of

conventional CMOS transistors.

The thesis also discusses the future research prospects and practical realization pathways for the proposed devices. Experimental fabrication using Atomic Layer Deposition (ALD) and Chemical Vapor Deposition (CVD) is recommended for producing high-quality HfO_2 and $HfZrO_2$ films with nanometre-scale precision. Structural and phase characterization through Transmission Electron Microscopy (TEM) and X0Ray Diffraction (XRD) will enable validation of the simulated results, while Piezo response Force Microscopy (PFM) can be employed to verify ferroelectric polarization and stability. Further optimization of doped ferroelectric materials could improve endurance and minimize coercive voltage, making these designs more robust for integrated circuit applications.

The proposed devices are also highly promising for circuit-level and system-level integration, particularly in low-power digital logic, non-volatile memory and neuromorphic computing architectures. Their ability to operate at low supply voltages and high switching speeds positions them as potential enablers for energy-efficient processors, artificial intelligence hardware, and edge computing systems. Additionally, due to their low energy consumption and compact footprint, these devices could be extended to flexible electronics and biomedical sensor platforms, paving the way for green and sustainable nanoelectronics systems.

From a broader perspective, the innovations presented in this thesis hold substantial technological and societal impact. By significantly reducing the power requirements of electronic systems, the proposed nanowire FETs contribute to global efforts toward energy conservation and sustainable electronics manufacturing. Their compatibility with existing CMOS fabrication processes ensures a practical transition path for semiconductor industries towards post-CMOS device paradigms. Furthermore, the reduction in energy consumption directly aligns with global objectives such as carbon footprint minimization and sustainable digital transformation.

In conclusion, this thesis provides a comprehensive and systematic exploration of next-generation nanowire transistor architectures that transcend conventional scaling barriers through a combination of electrostatic design and ferroelectric innovation. The research demonstrates that by co-optimizing gate geometry, dielectric heterogeneity, and ferroelectric polarization, it is possible to achieve sub thermal switching, low leakage, and exceptional electrostatic control all within a CMOS compatible framework. The proposed devices collectively form a technologically feasible and environmentally sustainable foundation for the development of ultra-scaled, low power, and high-performance electronics in the post-CMOS era.

This work not only advances the scientific understanding of ferroelectric and nanowire device physics but also contributes meaningfully to the realization of energy-efficient semiconductor technologies that align with both industrial evolution and societal responsibility.

LIST OF PUBLICATIONS

SCI/SCIE Journal Papers

1. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Hetero-dielectric macaroni channel cylindrical gate all around field effect transistor (HD-MC CGAA FET) for reduced gate leakage analog applications" Microsystem Technologies, vol. 30, no. 5, 2024, p. 599-611, doi: 10.1007/s00542-023-05577-9 (Springer, SCIE) (accepted and published).
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3. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Double metal gate macaroni nanowire FET (DMGM-NFET) for improved performance and off-state leakage reduction" ECS Journal of Solid State Science and Technology, vol. 13, no. 10, 2024, 103010, doi: 10.1149/2162-8777/ad775d (IOP Science, SCIE) (accepted and published).
4. **Aapurva Kaul,** Snehlata Yadav, Sonam Rewari, and Deva Nand, "Analytical Modelling of Temperature Resilient Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor" IEEE Transactions on Dielectrics and Electrical Insulation, vol. 32, no. 5, p. 2674-2682, 2025, doi: 10.1109/TDEI.2025.3538754 (IEEE Transaction, SCIE) (accepted and published).
5. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Performance-Oriented Analytical Modelling of Channel Engineered-Macaroni Induced Gate All Around Field Effect Transistor for Off-State Leakage Mitigation" ECS Journal of Solid State Science and Technology, vol. 14, no. 10, 2025, 103002, doi: 10.1149/2162-8777/ae09d8 (IOP Science, SCIE) (accepted and published).

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1. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Macaroni channel-nanowire-field effect transistor (MC-NW-FET) for gate induced drain leakage (GIDL) reduction application" In 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), pp. 35-38, 2022, doi: 10.1109/EDKCON56221.2022.10032964.

2. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Field Effect Transistor Incorporating Negative Capacitance and Nanowire Structures for the Attenuation of Gate Leakage Phenomena" In 2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), pp. 607-611, 2024, doi: 10.1109/EDKCON62339.2024.10870658.

3. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Mathematical Modelling of Gate Leakage in Channel Interface Engineered-Electrostatic Potential Modulated Field Effect Transistor for Advanced Digital Applications" In 2025 International Conference on Electrical, Computer and Energy Technologies (ICECET), 2025.

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LIST OF ABBREVIATIONS

Al_2O_3	Aluminum Oxide
SMGM-NFET	Single Metal Gate Macaroni Nanowire Field Effect Transistor
CGEF-NW FET	Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor
C-FE-DM-NW FET	Cylindrical Ferroelectric Dual Metal Nanowire Field Effect Transistor
ASIC	Application Specific Integrated Circuit
BTBT	Band to Band Tunneling
CAD	Computer Aided Design
CBE	Conduction Band Energy
BJT	Bipolar Junction Transistor
BTI	Bias Temperature Instability
NC-NW FET	Negative Capacitance Nanowire Field Effect Transistor
CGAA	Cylindrical Gate-All-Around
CLM	Channel Length Modulation
CMOS	Complementary Metal Oxide Semiconductor
CONMOB	Concentration Dependent Mobility Model
CVD	Chemical Vapor Deposition
DG	Double Gate
DIBL	Drain Induced Barrier Lowering
DM	Dual Modulated
DM-FET	Dielectric Modulated-Field Effect Transistor
CE-MI-GAA FET	Channel Engineered Macaroni Induced Gate-All-Around Field Effect Transistor
DRAM	Dynamic Random Access Memory
E_F	Fermi Level
EOT	Equivalent Oxide Thickness
eV	Electron Volt
FET	Field Effect Transistor
FINFET	Fin Field Effect Transistor
FLDMOB	Field Dependent Mobility Model
GAA	Gate-All-Around
DMGM-NFET	Double Metal Gate Macaroni Nanowire Field Effect Transistor
GAA-FET	Gate-All-Around Field Effect Transistor
HD-MC CGAA FET	Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor
CIE-EPM FET	Channel Interface-Engineered Electrostatic Potential Modulated Field Effect Transistor
GaN	Gallium Nitride
TDDB	Time-Dependent Dielectric Breakdown
GIDL	Gate Induced Drain Leakage
MC FET	Macaroni Channel Field Effect Transistor

GME	Gate Metal Engineered
HCE	Hot Carrier Effects
MBE	Molecular Beam Epitaxy
HfO_2	Hafnium Oxide
IC	Integrated Circuit
RDF	Random Dopant Fluctuation
I_{OFF}	Off Current
I_{ON}	On Current
JAM	Junction Accumulation Mode
JGAA	Junctionless Gate-All-Around
JL	Junction Less
LSI	Large Scale Integration
MSI	Medium Scale Integration
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-Channel Metal Oxide Semiconductor Field Effect Transistor
NW	Nano Wire Field Effect Transistor
R_{ch}	Channel Resistance
NWFET	Nano Wire Field Effect Transistor
PMOS	P-Channel Metal Oxide Semiconductor Field Effect Transistor
SCE	Short Channel Effects
RF	Radio Frequency
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon Dioxide
NBTI	Negative Bias Temperature Instability
SRH	Shockley-Read-Hall
SS	Subthreshold Slope
SOI	Silicon On Insulator
VLS	Vapour Liquid Solid
TCAD	Technology Computer Aided Design
TFET	Tunnel Field Effect Transistor
UTB	Ultra-Thin Body
VBE	Valence Band Energy
V_{GS}	Gate to Source Voltage
V_{DS}	Drain to Source Voltage
VLSI	Very Large-Scale Integration
WF	Work-Function
NC FET	Negative Capacitance Field Effect Transistor
ZrO_2	Zirconium Dioxide

CHAPTER 1

INTRODUCTION

1.1 Historical Genesis of MOSFET Technology

Since the invention of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) by Dawon Kahng and Martin Atalla in 1959 at Bell Telephone Laboratories [1], the MOSFET has become the most fundamental building block of modern digital integrated circuits, which has enabled the growth of the semiconductor industry, mainly due to its manufacturability, scalability, and compatibility with the Complementary Metal Oxide Semiconductor technology (CMOS) [1]. In the MOSFET structure, the gate electrode, insulated from the semiconductor channel by a thin layer of dielectric (SiO_2), controls the formation of a conductive inversion channel. MOSFETs are classified into two types: p-channel MOSFETs (PMOS) and n-channel MOSFETs (NMOS) depending on the type of charge carriers in the channel. The PMOS device is constructed on an n-type silicon substrate, featuring a p-type source and drain region. In this, the conduction channel is formed by the holes when a negative gate-to-source voltage is applied. In this case, conduction is primarily carried out via holes, which serve as the majority carriers when a negative gate-to-source voltage is applied. Conversely, an NMOS device is constructed on a p-type silicon substrate, featuring an n-type source and drain region using diffusion or ion implantation. In this case, conduction is primarily carried out via electrons, which will serve as the majority carriers when a positive voltage is applied at the gate terminal. The structural schematics of PMOS and NMOS transistors are shown in Figure 1.1.

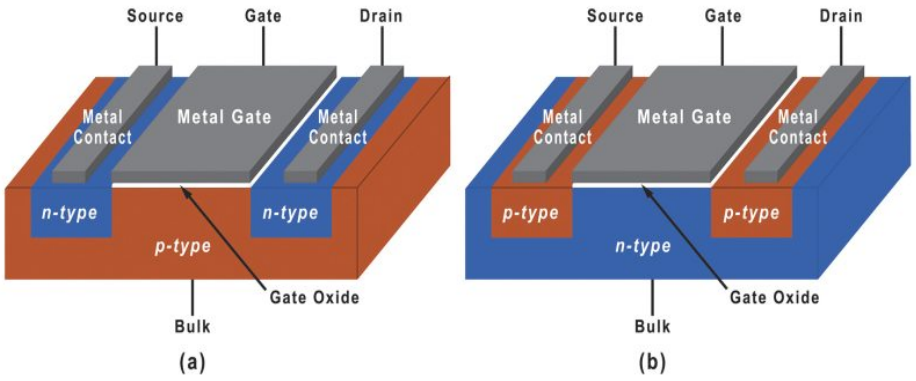


Figure 1.1 Structural Schematics of (a) NMOS Transistor and (b) PMOS Transistor [2]

The MOSFET operates as a voltage-controlled device in which the application of a gate voltage modulates the conductivity of a channel between the source and drain terminals, hence allowing efficient control of current flow. MOSFETs are preferred over Bipolar Junction Transistors (BJTs) because of their simpler planar structure, low static power consumption, and high input impedance. The gate terminal of MOSFETs is insulated, thus the device exhibits extremely low input current, enabling high input impedance. Moreover, MOSFETs are inherently more scalable, as their operations

primarily depend on electrostatic control rather than minority carrier transport [3]. This scalability played a very important role in large-scale integration, where thousands, millions, and even billions of transistors could be placed on a single silicon chip. In the 1960s, MOSFETs began to find applications in digital integrated circuits (ICs). However, due to the instabilities in the Si-SiO_2 interface, many devices were considered unstable. Martin Atalla's pioneering work on surface passivation using thermal oxidation of silicon was very helpful in solving challenges in creating a stable and reliable gate dielectric [4]. After the invention of Complementary Metal Oxide Semiconductor (CMOS) logic by Frank Wanlass in 1963, MOSFETs were replacing BJTs in logic circuits [5]. CMOS technology was considered highly suitable for very large-scale integration (VLSI) because of its complementary switching of NMOS and PMOS transistors, which drastically reduces static power dissipation. Figure 1.2 illustrates the evolution of VLSI technology over the past few decades.

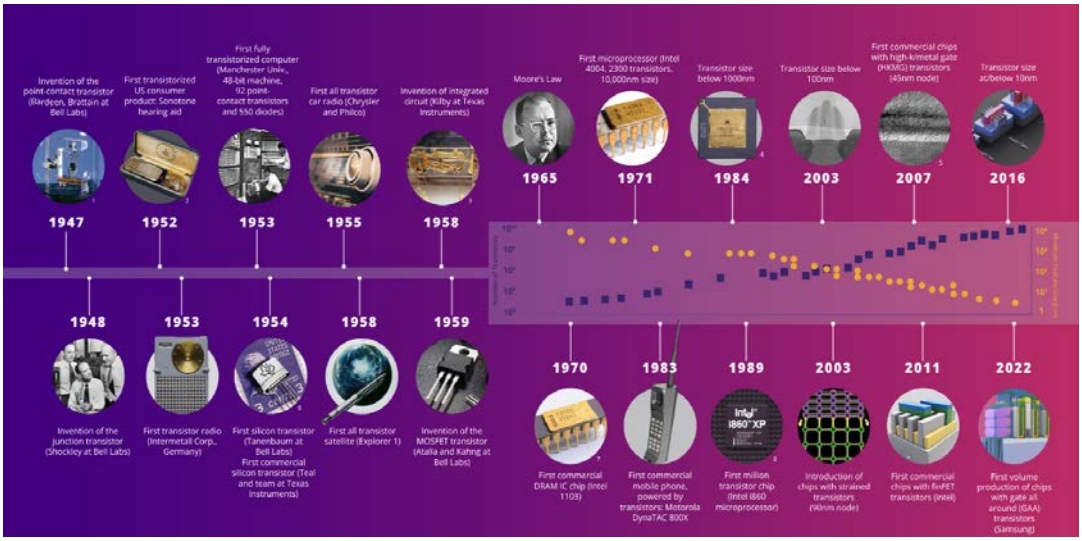


Figure 1.2 Evolution of VLSI Technology [6]

In the 1960s, the integration of MOSFETs started with Small Scale Integrations (SSI), where a handful of transistors were integrated using logic gates. Soon, the designing of arithmetic logic units (ALUs) and memory registers led the integration progress towards Medium Scale Integration (MSI). In 1968, dynamic random-access memory (DRAM) was introduced, and in 1970, microprocessors were introduced, marking the beginning of MOSFETs' dominance in logic applications and memory applications and leading the progress of integration towards Large Scale Integration (LSI) [7]. The era of scaling began with Intel's first commercial microprocessor, released in 1971 under the name Intel 4004. This microprocessor was designed using 2,300 MOSFETs with a minimum feature size of 10 µm [4]. In the late 1970s and early 1980s, Very Large-Scale Integration (VLSI) emerged, and in this, tens of thousands to millions of MOSFETs can be integrated. Moore's Law predicted that the number of transistors on an integrated circuit would double approximately every two years [8]. Over the decades, MOSFETs' dimensions have steadily reduced as the ion implantation, self-aligned gate processes, and photolithography techniques advance. The transistor channel length scaled from the micrometer regime in the 1970s to the nanometer regime in the early 2000s, with devices at the 90 nm and 65 nm nodes introducing new

performance benchmarks by advancing to the 30 nm regime [9]. These advancements are complemented by the challenges of short channel effects, process variability, and leakage currents. These challenges eventually motivated the transition of MOSFETs from planar to three-dimensional device architectures.

1.2 Scaling Theory: Dennard's Fundamentals

Transistor scaling is a very important principle on which the growth of the semiconductor industry is dependent, enabling improvement in power efficiency, integration density, and performance. In 1974, Robert H. Dennard articulated in a seminal paper the cornerstone of advancement in Dennard's Scaling Theory at IBM [7][6]. This theory provides the guidelines describing the miniaturization of MOSFETs while maintaining electrical similarity across technology nodes. Progressive reduction of gate length across different technology nodes can be observed in Figure 1.3.

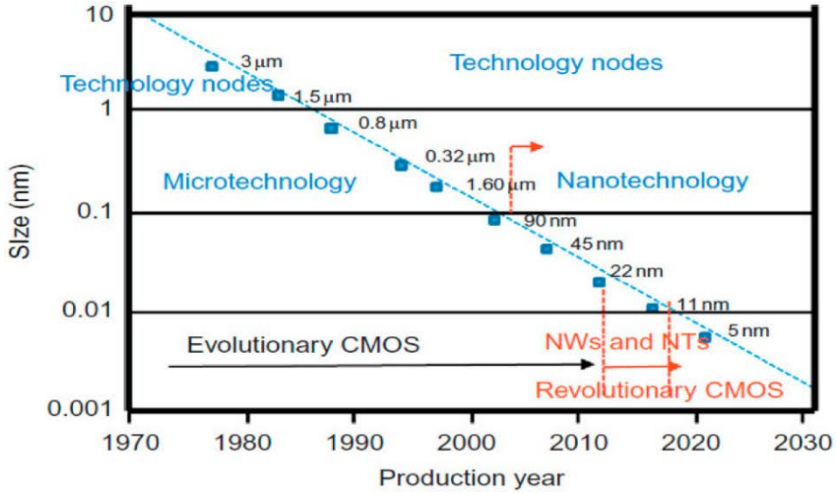


Figure 1.3 MOSFET Scaling: Progressive Reduction of Gate Length Across Successive Technology Nodes [10]

According to Dennard's Scaling Theory, the dimensions of a transistor are scaled down by a constant factor, doping concentration, and voltage. This scaling is done keeping in mind to preserve the device behaviors. In this, if device dimensions are reduced by a factor of κ (>1), then the supply voltage and threshold voltage are reduced by the same factor, whereas doping concentrations are increased by the same factor, i.e., κ. Various scaling relationships emerged under these conditions, such as device current and switching delay being reduced by $1/\kappa$, power dissipation scaled down to $1/\kappa^{2,}$ but the power density remains constant. According to this scaling theory, it was concluded that smaller MOSFETs would consume less energy, operate faster, and enable higher integration without increasing power density. The combination of Moore's Law with Dennard's Scaling Theory laid the foundation of the integrated circuit industry [11][8].

1.2.1 Impact of Dennard Scaling

The impact of Dennard Scaling theory was seen for generations, enabling the technology to deliver exponential improvements in energy efficiency and processor speed. Throughout the 1980s and 1990s, this was reflected in the rapid increase of

clock frequencies, which rose from a few megahertz (MHz) in early microprocessors to several gigahertz (GHz) by the early 2000s [12]. During the same time duration, the cost per transistor was decreasing steadily, whereas the transistor sizes were reduced from several micrometers down to deep submicron and nanometer scales. This scaling theory also laid the foundation of low-power electronics by reducing operating voltage and capacitances, and reducing energy consumption per switching event. This is a critical factor for portable devices and mobiles, where battery life is dependent on the power efficiency of the transistor. The balance between energy efficiency and high performance made possible by scaling ensured the pervasiveness of MOSFET-based systems in applications ranging from high-performance computing to consumer electronics.

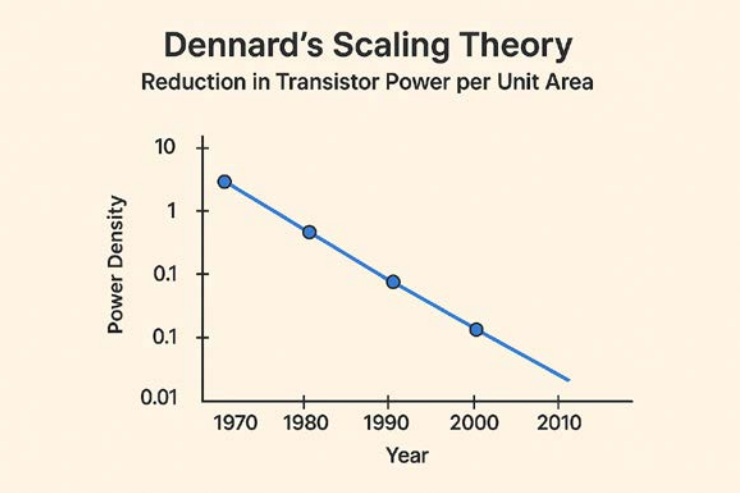


Figure 1.4 Dennard's Scaling Theory [8]

1.2.2 Breakdown of Dennard Scaling

In the 2000s, Dennard Scaling Theory faced serious limitations as the device approached the deep submicron regime, i.e., below 90 nm. The fundamental assumptions of the theory break down due to the short-channel effects and quantum-mechanical effects [3]. The inability of the scaling theory to scale supply voltage proportionally with channel length resulted in increased power density and thermal issues. Severe gate leakages were introduced due to thinner gate oxides. The short channel devices suffer from short channel effects (SCEs) such as drain-induced barrier lowering (DIBL) and voltage roll off. Additionally, higher variability from random dopant fluctuations and increased subthreshold leakage currents disrupted predictable device behaviour. Due to these challenges, the Dennard Scaling Theory marked its end. To sustain Moore's Law, new device architectures such as FinFETs, Nanowire Transistors, and Gate All Around (GAA) FETs were designed.

1.3 Planar Bulk MOSFET Regime

The planar bulk MOSFET technology originated from MOS technology, which was introduced in the 1960s. This architecture dominated the semiconductor industry for the past four decades. This architecture consists of a conducting channel of silicon

between source and drain terminals, controlled by the gate electrode, which is separated by a thin insulating oxide layer from the substrate [3]. The planar MOSFET became the workhorse for large-scale integration (LSI) and very large-scale integration (VLSI) because of its simple fabrication, compatibility with CMOS, and scalability.

1.3.1 Advances in Planar Bulk MOSFETs

The scaling of planar MOSFETs from micrometer to nanometer dimensions led to unprecedented growth in the performance of integrated circuits (ICs). Several technological innovations underpinned these advances:

1.3.1.1 Scaling to Submicron Regime

During the 1980s to 1990s, the planar bulk MOSFETs were scaled from 1 µm to 100 nm dimensions, in line with Moore's Law [8]. This scaling led to improvement in ion implantation, thin oxide growth, and lithography. The precision in small geometries is dependent mainly on etching techniques.

1.3.1.2 Self-Aligned Gate Technology

To reduce the parasitic overlap capacitances, in the 1960s, self-aligned polysilicon gates were introduced, which enabled high switching speed in the devices [13]. This served as a milestone, allowing for tighter packing of transistors, which became a standard in MOS fabrication. This innovation was pioneered at Fairchild and Intel.

1.3.1.3 High-κ Metal Gate Integration

In the case of planar MOSFETs, the replacement of the SiO_2 layer with a high-κ dielectric and the adoption of metal gates around the 45 nm regime was a breakthrough. This helps reduce leakage current in the MOSFETs, which is caused by carrier tunneling through the channel. The leakage current is reduced via gate control [14]. This integration marked the end of the polysilicon/SiO_2 era and prolonged the viability of planar MOSFETs into the nanometer node. Figure 1.5 demonstrates the high-κ dielectric and dual metal gate integration of an FET.

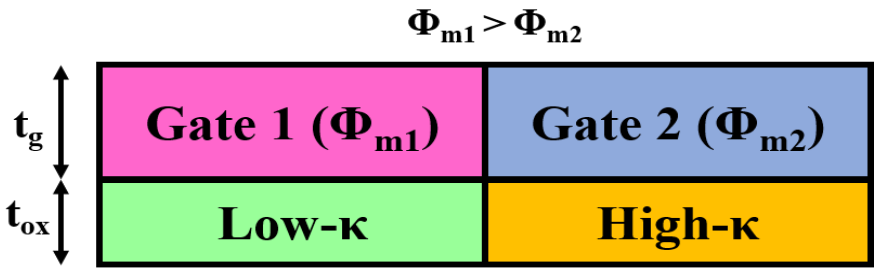


Figure 1.5 High-κ Dielectric and Dual Metal Gate Integration

1.3.1.4 Strained Silicon Technology

In the 2000s, this strain engineering was introduced, and in this, tensile strain was applied to the nMOSFET channel, and compressive strain was applied to the

pMOSFETs. This technology helps in improving carrier transport properties and restoring performance [13].

1.3.1.5 Low Power CMOS Design Techniques

The static and dynamic power consumption in CMOS circuits is the focus of research as portable electronics are gaining popularity. Multi-threshold CMOS, voltage scaling, and clock-gating were widely employed in conjunction with transistor scaling to achieve energy-efficient operations [15].

Collectively, these advances have kept planar bulk MOSFETs relevant as the foundation of communication and computing systems well into the deep submicron technology generations.

1.3.2 Constraints of Planar Bulk MOSFETs

Despite the steady advancement, fundamental physical and technological constraints surfaced as planar MOSFETs got closer to the 30 nm regime, ultimately causing a paradigm shift towards new device architectures. The primary constraints are as follows:

1.3.2.1 Short Channel Effects (SCEs)

Electrostatic control of the channel by the gate is weakened as the channel length reduces below 100 nm, which leads to Drain Induced Barrier Lowering (DIBL), threshold voltage roll-off, and degradation in subthreshold slope [6]. These parameters affect the transistor performance and increase leakage currents.

1.3.2.2 Gate Leakage due to Ultra-Thin Oxide

In the case of a 90 nm node, the oxide thickness has been reduced approximately to 2 nm. Due to a thin layer of oxide, the tunnelling currents through SiO_2 lead to an increase in static power dissipation and reduced device reliability [16]. To overcome this problem, high-κ dielectrics were introduced, but they lead to different challenges such as threshold instability and quality degradation [16].

1.3.2.3 Leakage Power and Standby Current

Maintaining the lower supply voltage leads to aggressive scaling of threshold voltage, which in turn leads to an exponential increase in subthreshold leakage current. In large-scale system on chip (SoCs), leakage power becomes a major contributor to standby power consumption [17].

1.3.2.4 Variability and Process Sensitivity

Random dopant fluctuations (RDFs), lithographic variations, and line-edge roughness plagued nanoscale planar MOSFETs, causing significant device-to-device variability in drive current and threshold voltage [18]. Since it restricted yield and necessitated conservative design margins, this variability became a scaling bottleneck.

1.3.2.5 Thermal and Power Density Challenges

Localized anomalies resulted from on-chip power density reaching critical levels as transistor density rose. This made reliability issues like negative bias temperature instability (NBTI), time-dependent dielectric breakdown, and electromigration exacerbated [12].

1.3.2.6 Performance Saturation

Drive current scaling is failing to keep pace with dimensional scaling because at high electric field, mobility degradation and velocity saturation effects become more pronounced. Despite continuous miniaturization, these effects slow down the performance gain of the device [19].

1.3.3 Transition Beyond Planar Bulk MOSFETs

By the 2000s, these constraints collectively marked the end of the planar Bulk MOSFETs regime as the industry's prime scaling solution. FinFET structure was first adopted by Intel in 2011 at the 22 nm technology node in mass production as it offers superior electrostatic control and reduces leakages [20]. Since 2011, multi-gate devices such as FinFETs and Gate-All-Around (GAA) Nanowire/Nanosheet FETs have emerged as a promising candidate that ensures the continuation of Moore's Law beyond classical scaling limits. The planar Bulk MOSFET remains a historical architecture that has driven the digital revolution and established the foundation of modern transistor technology [21].

1.4 Short-Channel Effect (SCEs) and Their Implications

The ideal assumptions of long-channel device physics are no longer valid once the MOSFET channel length enters the deep sub-micron regime. In this, the gate terminal exerts dominant control over the channel potential, ensuring efficient switching between ON and OFF states. But as the channel length gets closer to the characteristic depletion width, the source and drain junctions' competing effects cause the gate electrostatic control to wane. By rising leakage current impairing subthreshold behavior and lowering threshold voltage, this phenomenon is referred to as short channel effects [11], [3].

1.4.1 Mechanisms of Short Channel Effects

The two-dimensional electrostatics of scaled MOSFETs are fundamental components of SCEs. The depletion regions from source and drain encroach into the channel when the channel length approaches the depletion width, which causes the gate and junctions to share charge [6]. This reduces the gate control over the channel potential. The important SCE mechanisms include:

1.4.1.1 Gate Induced Drain Leakage (GIDL)

In aggressively scaled MOSFETs, as channel length decreases and the electric field near the drain side increases, a critical leakage phenomenon known as Gate Induced Drain Leakage (GIDL) becomes prominent. This short channel effect occurs when a

high drain to gate voltage is applied while the gate voltage remains low or negative. Under these conditions the strong electric field developed in the drain gate overlap region causes band-to-band tunnelling (BTBT) between the valance band and conduction band in the depletion region [22]. Figure 1.6 illustrates the band-to-band tunnelling phenomenon in FETs. As a result, electron-hole pairs are generated with electrons moving into the drain and holes toward the substrate, leading to an undesirable drain leakage current even when the device is in OFF state. The magnitude of the GIDL current increases exponentially with oxide field strength and is further influenced by drain doping concentration, dielectric quality and oxide thickness [23].

In short channel devices, the electric field coupling between the gate and drain is intensified due to the reduced separation between junctions, making GIDL effect more pronounced. This not only contributes to standby power dissipation but also degrades device reliability, causing instability in threshold voltage and accelerating oxide wear out. The use of high-κ gate dielectrics, graded drain doping profiles and gate overlap helps to redistribute the electric field at the drain junction and suppress tunnelling induced leakage [24]. In modern GAA and Nanowire FET architectures, the 3D gate control significantly reduces field crowding near the drain edge, thereby mitigating GIDL effect while maintaining high drive capability. Figure 1.7 demonstrates the GIDL phenomenon in nanowire FETs.

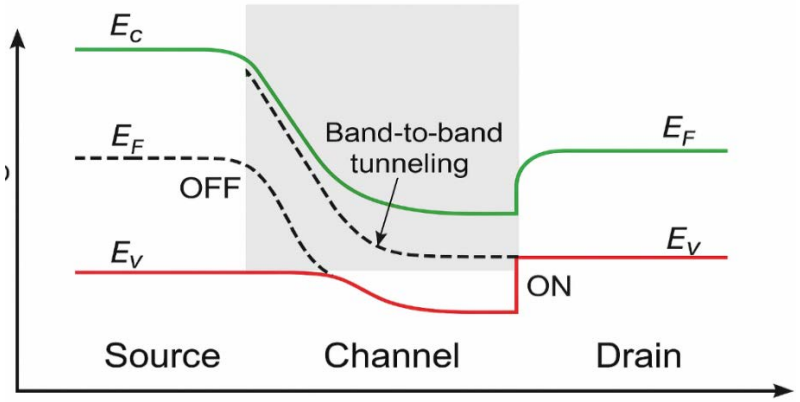


Figure 1.6 Band-to-Band Tunnelling in Nanowire FET.

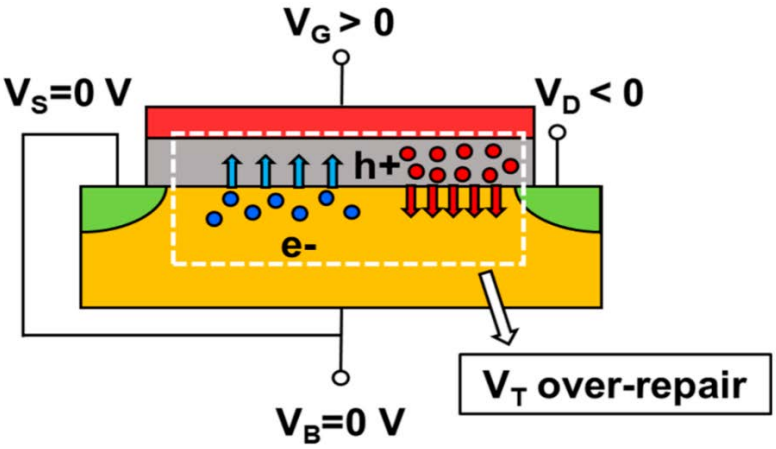


Figure 1.7 Representation of GIDL in MOSFET.

1.4.1.2 Hot Carrier Effects (HCE)

The high electric field near the drain accelerates the carriers, thus creating hot carriers in short-channel devices, which are trapped in the gate oxide or at the Si-SiO_2 interface. This reduces the reliability, threshold voltage shifts, and degrades the device [25]. Figure 1.8 illustrates the hot carrier effects of FETs.

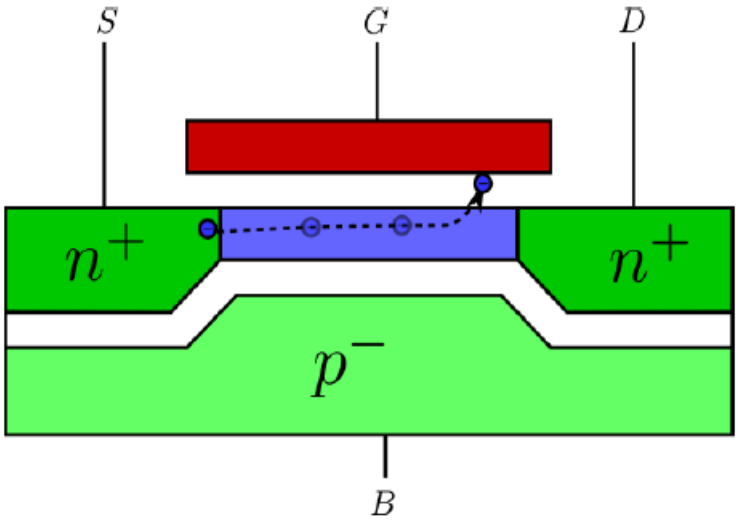


Figure 1.8 Representation of Hot Carrier Effect

1.4.1.3 Channel Length Modulation (CLM)

In this phenomenon, as the channel length shrinks, the effective channel region modulated by the gate reduces with increasing drain bias. This effect increases drain current beyond saturation, impairing output resistance and limiting the intrinsic gain of the device [26]. Figure 1.9 represents the channel length modulation phenomenon. The reduction in channel length is negligible when compared to the overall channel length in the case of long channel devices; this reduction is significant and can reduce the channel length to zero.

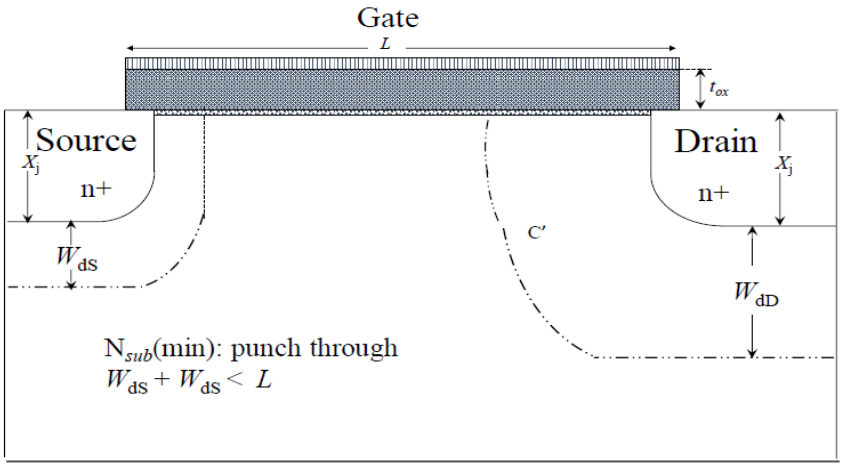
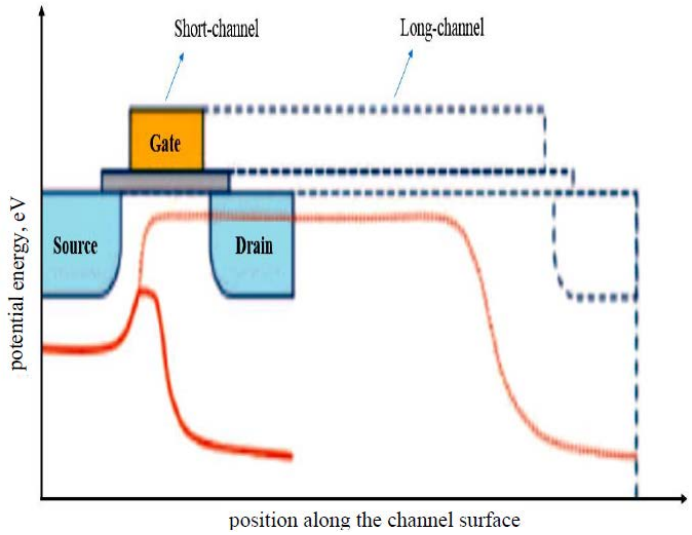


Figure 1.9 Representation of Channel Length Modulation [27]

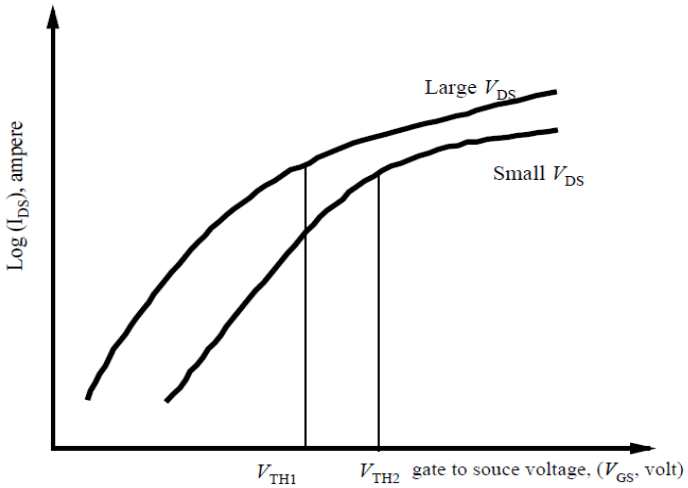
1.4.1.4 Drain Induced Barrier Lowering (DIBL)

This phenomenon occurs when, at high drain voltage, the source channel barrier is lowered, allowing carriers to surmount it more easily. This effect reduces the threshold and increases the OFF-state leakage at high drain current [28]. DIBL affects the device reliability in logic circuits when ultra-scaled MOSFETs are considered. Figure 1.10 illustrates the effect of DIBL and the effect on current characteristics of the FET.



(a)

Figure 1.10 Illustrates (a) DIBL Effect [29]



(b)

Figure 1.10 Illustrates (b) Effect on Current Characteristics [29].

1.4.1.5 Subthreshold Slope Degradation

The subthreshold slope (SS) of an ideal MOSFET is limited to 60 mV/decade at room temperature. In case of short channel devices, the coupling between the drain and

channel deteriorates the subthreshold swing, requiring higher gate voltages to switch the transistor effectively [30]. This degrades the energy efficiency of logic circuits.

1.4.1.6 Threshold Voltage Roll-Off

38

The threshold Voltage (V_{th}) of the device is dependent on the length of the channel in the case of long-channel devices. However, in the case of short-channel devices, as the channel length reduces, so does the threshold voltage. This occurs due to the source and drain assist in channel inversion [31], increasing leakage current, particularly the OFF-state current. Figure 1.11 shows the effect of a reduction in channel length on the threshold voltage of an FET.

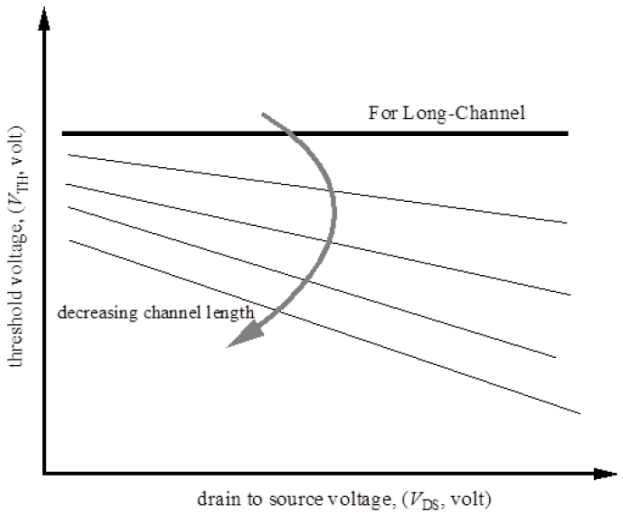


Figure 1.11 Effect of Channel Length Reduction on Threshold Voltage [32].

1.4.2 Implications for Device Scaling

The SCEs posed a challenge to the continuation of Dennard Scaling Theory. Scaling increased integration density and switching speeds, but SCEs' excessive leakage and variability increased static power dissipation and decreased logic circuit noise margins [33]. For instance, DIBL and threshold voltage roll-off were directly responsible for the dramatic increase in standby power consumption, which emerged as a major issue in portable and battery-powered devices.

Additionally, the ability to lower supply voltage (V_{DD}) was constrained by subthreshold slope degradation without compromising functionality. Concerns about reliability also intensified. High fields damage oxide integrity, and hot carrier degradation reduces device life. These difficulties highlighted how urgently alternative architectures are needed to suppress leakage, restore electrostatic integrity, and enhance gate control [7].

1.4.3 Path Toward Solutions

The innovation of device designs and material engineering for mitigating SCEs is an essential step. Several methods to carve that path are:

1.4.3.1 Multi-Gate Architectures

Various architectures, such as Double Gate MOSFETs, FinFETs, and Gate All Around FETs, were studied as they provide superior electrostatic control [34]. Figure 1.12 Shows various multi-gate structures such as Double Gate, Tri Gate, Omega Gate, Pi Gate, Cylindrical Surrounding Gate, Cylindrical Double Surrounding Gate, and Gate All Around FETs.

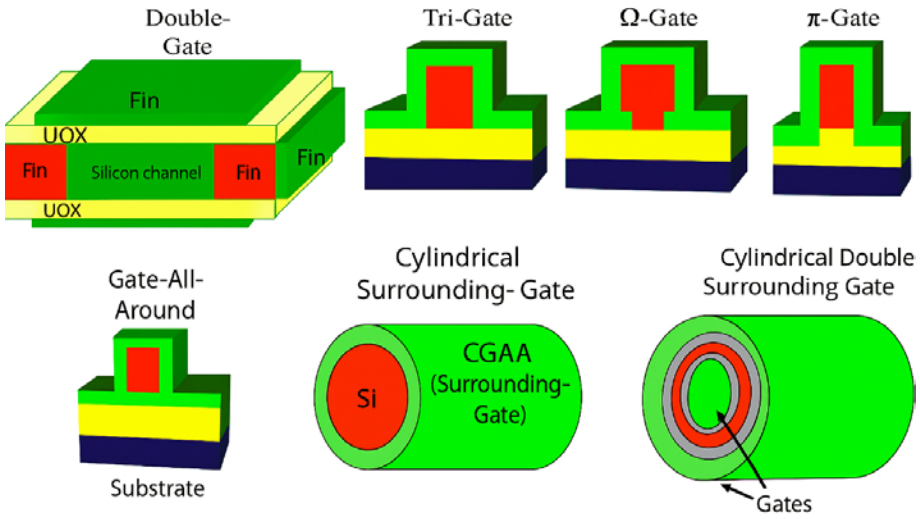


Figure 1.12 Multi-Gate FET Structures [35].

1.4.3.2 Ultra-Thin Body (UTB) and Silicon-on-Insulator (SOI) Devices

Drain Induced Barrier Lowering is a major concern when the thickness of the body is reduced. In this scenario, fully depleted SOI devices are used as they enhance gate control by confining carriers to a thin film [36].

1.4.3.3 High-κ Dielectrics and Metal Gates

Replacing SiO_2 with high-κ dielectric reduced equivalent oxide thickness without increasing leakage, mitigating SCEs, and improving gate control [14]. These innovations have collectively taken the semiconductor industry away from planar bulk MOSFETs towards three-dimensional device structures, setting the stage for nanowire transistors and FinFETs.

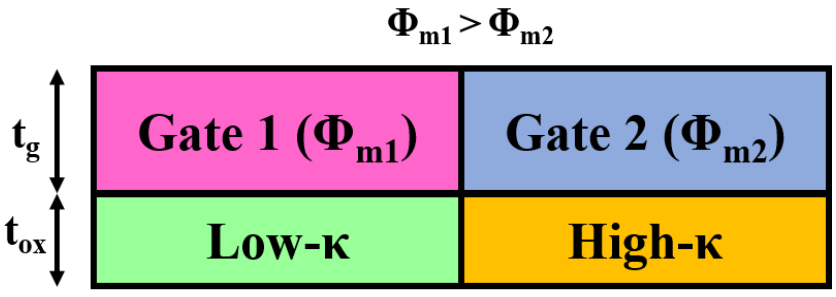


Figure 1.13 High-κ Dielectric and Dual Metal Gate Integration

1.5 Multi-Gate Transistors

Beyond the 65 nm technology node, it was necessary to rethink the device architecture due to the persistent challenges of short-channel effects (SCEs) in planar MOSFETs. Traditional scaling methods, such as channel length and oxide thickness reduction, were insufficient in maintaining electrostatic integrity without affecting leakage current and power dissipation [11]. The gate-all-around structure is a promising one, as in this gate-to-channel coupling is achieved by surrounding the channel. This led to the development of multi-gate transistor architectures like FinFETs, Tri-Gate MOSFETs, and Gate-All-Around (GAA) FETs [31].

1.5.1 Concept and Motivation

The multi-gate devices were designed to increase the control of the gate by maximizing the effective gate-to-channel capacitance. In the case of a planar MOSFET, the gate controls the channel from the top surface, leaving lateral electrostatics dominated by the drain and source. By introducing various architectural changes such as vertical channels, nanowires, or fins, the gate can control multiple sides of the channel, hence suppressing SCEs, improving subthreshold swing (SS), and reducing DIBL [30], [3].

In the late 1990s and early 2000s, researchers demonstrated a breakthrough when double-gate MOSFETs were fabricated using SOI technology. This helps in significantly reducing the threshold voltage roll-off and leakage [36]. In 2011, Intel designed a Tri-Gate FinFET technology of 22 nm node, making the highest first high-volume commercial deployment [20].

1.5.2 Types of Architectures

Several structural variations of multi-gate MOSFETs have been explored, each structure has having different trade-off in terms of performance, manufacturability, and electrostatics:

1.5.2.1 Double Gate MOSFETs (DG-MOSFETs)

In this structure, a gate is placed at both sides, i.e., the top and bottom of the channel. This structure provides gate control, but its fabrication complexity (requiring ultra-thin SOI wafer with alignment accuracy) [37].

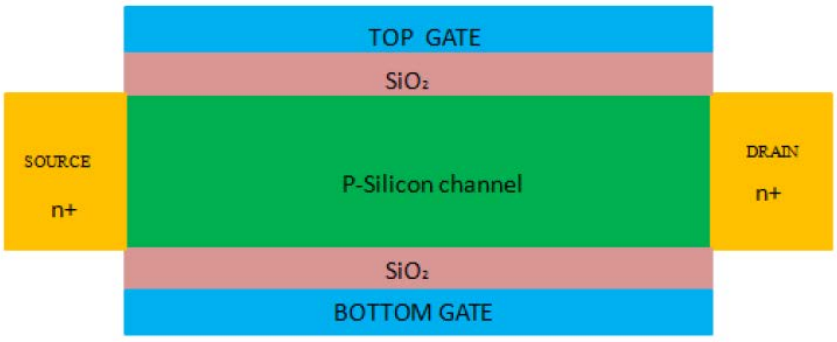


Figure 1.14 Double Gate MOSFETs

1.5.2.2 FinFETs

The FinFET structure consists of a thin vertical fin with a gate wrapped around from three sides. This structure improves the electrostatic control while remaining compatible with existing CMOS fabrication processes. For the 22 nm node to 5 nm node technology, FinFET is an ideal candidate [20], [37].

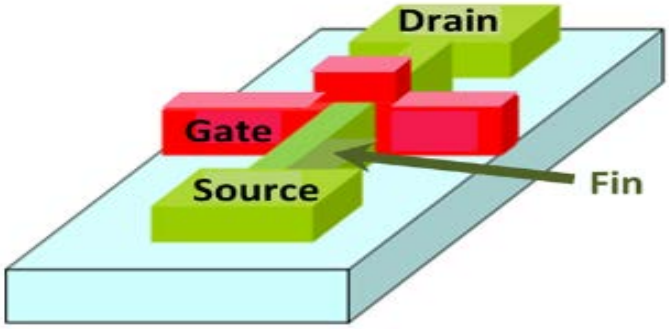


Figure 1.15 FinFET Structure [38]

1.5.2.3 Tri-Gate FETs

It is a variant of FinFET, in which the gate provides three-sided control of the channel. It provides higher driver current and improved performance when compared with planar MOSFETs; it was implemented by Intel [37].

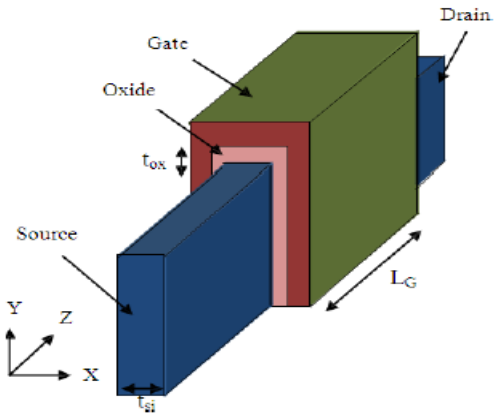
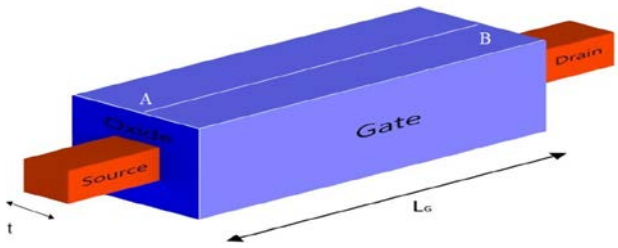


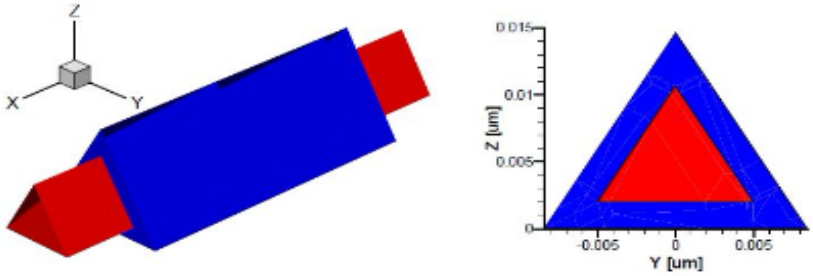
Figure 1.16 Tri-Gate Structure [39].

1.5.2.4 Gate-All-Around (GAA) FETs

In this architecture, the gate controls the channel by surrounding it from all sides and provides the strongest possible electrostatic control. This architecture is considered the most scalable multi-gate structure. This implementation includes nanowire FETs and nanosheet FETs, which are implemented by Samsung and TSMC at the 3 nm technology node [40].



(a)



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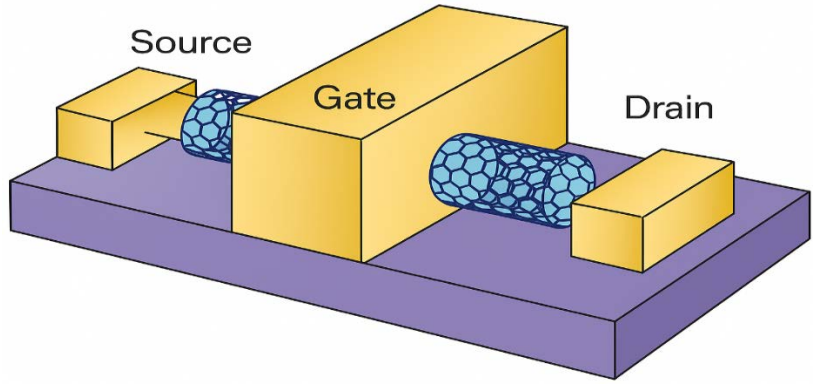

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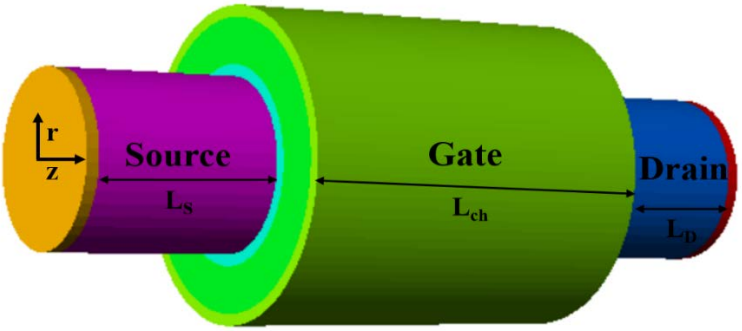


(d)

Figure 1.17 Represents (a) Rectangular FET, (b) Triangular FET, (c) Nanotube FET and (d) Cylindrical FET [41], [42]

1.5.3 Benefits of Multi-Gate Devices

The evolution from traditional planar MOSFETs to multi gate device architectures represents a pivotal advancement in addressing the electrostatic limitations encountered at deeply scaled technology nodes. The multi-gate configuration, such as FinFETs, Tri gate and gate all around structures, enables superior electrostatic gate control by wrapping the gate electrode around multiple sides of the channel, thereby offering enhanced immunity against short channel effects (SCEs) and improved scalability. One of the most significant advantages of this geometry is the suppression of DIBL and threshold voltage roll-off, phenomenon that are particularly pronounced in planar devices under high drain bias. In multi gate devices the lateral and vertical electrostatic fields are better confined within channel, reducing potential barrier modulation and ensuring stable threshold voltage operation even at high drain voltage [43].

Another critical benefit is the improvement in subthreshold swing (SS), where multi gate structures achieve near-ideal thermal limits of 60 mV/decade at room temperature. This enables aggressive supply voltage scaling while maintaining reliable switching performance and reduced subthreshold leakage currents [44]. The stronger gate to channel coupling effectively suppresses parasitic charge sharing and improves the transistor's ability to switch sharply between ON and OFF states, which is fundamental for energy efficient logic design. Moreover, the scalability of multi gate devices provides a viable pathway towards sub-5 nm technology nodes, as their performance becomes independent of planar channel thickness. This three-dimensional gate control allows continued scaling of both channel length and oxide thickness, extending the Moore's law while mitigating electrostatic degradation [45].

In addition to improve scaling behaviour, multi gate devices exhibit enhanced drive current characteristics. The introduction of multiple fins or stacked nanosheets increase effective channel width without enlarging the device footprint, leading to higher current drivability and improved transconductance [45]. This characteristic makes multi-gate devices particularly advantageous for high speed and high-density circuit applications, where compactness and performance must coexist. Finally, these architectures are inherently compatible with high-κ/metal gate stacks, which further enhance their electrostatic integrity. The integration of the high-κ dielectrics such as HfO_2 and ZrO_2 with metal gate electrodes allows better control over work function tuning, reduces gate leakage, and enhances device reliability under low-power operation [14].

Collectively the multi-gate transistor architectures offer a balanced solution for scaling, performance and power efficiency. Their ability to deliver suppressed short channel effects, low leakage, high drive capability and compatibility with advanced materials positions them as the fundamental device architectures for next generation CMOS technologies and a critical enabler for the continued evolution of ultra scaled nanoelectronics.

1.5.4 Challenges and Industry Adoption

In the multi-gate structure fabrication is always a challenging task despite its various advantages. FinFETs require precise fin height and width, and variability due to line edge roughness and quantum confinement in ultra-thin fins [46]. GAA FETs are complex when it comes to fabrication, whereas it has superior electrostatic control. Nevertheless, industry adoption has been rapid:

- Intel commercialized Tri-Gate FinFETs at 22 nm in 2011 [20].
- TSMC and Samsung commercialized FinFET-based 16/14 nm node in 2014-2015.
- Samsung commercialized GAA nanosheet at 3 nm node in 2022 [40].

This ensures the multi-gate FETs as the backbone of CMOS scaling in the nanoscale regime.

1.5.5 Future Outlook

FinFETs were dominating the production till now, but GAA FETs are expected to extend CMOS scaling to the sub-3 nm regime with complementary FET and nanosheet architectures under research [34]. Integration of two-dimensional semiconductors with ferroelectric materials and negative capacitance is a promising field to enhance the electrostatic and energy efficiency of traditional FETs [47].

1.6 Gate-All-Around (GAA) FETs

As conventional planar MOSFETs and FinFETs reached their scaling and electrostatic limits, the Gate All-Around (GAA) Field-Effect Transistors have emerged as a very promising successor for sub-7 nm and beyond technology. In GAA FETs, because of the gate electrode surrounding the channel, superior electrostatic control is exhibited, which provides an enhanced short channel immunity and reduced leakage when compared to multi-gate structures [37]. By wrapping the gate around the channel, the GAA structure ensures that the potential in the channel is strongly controlled by the gate, and in return, drain-induced barrier lowering (DIBL) is suppressed, subthreshold slope (SS) is degraded, and other short-channel effects (SCEs) are limited in the nanometer regime.

The double gate and FinFET structures provide improved electrostatic control by placing gates on two or three sides of the channel, but GAA structures achieve maximum gate control by surrounding the channel in a coaxial manner, hence it is considered the ultimate extension of multi-gate FETs [48]. Among various structures of Gate-All-Around (GAA) FETs, the Cylindrical Nanowire Field Effect Transistor (NW FET) is the most promising architecture due to its scalability and perfect electrostatic symmetry. In this, the gate is allowed to wrap uniformly around the channel from all directions, which is different from rectangular or triangular GAA FETs. Due to this configuration, cylindrical NW FETs have nearly ideal subthreshold slope, reduced short channel effects, and maximized electrostatic control [49], [31]. This geometry helps in overcoming the limitations of planar and FinFET technologies at sub 5 nm regime, where variability and short channel effects (SCEs) like Gate

Induced Drain Leakage (GIDL) and Drain Induced Barrier Lowering (DIBL) pose a critical challenge [43]. Figure 1.18 demonstrates the cylindrical Nanowire Field Effect Transistor structure.

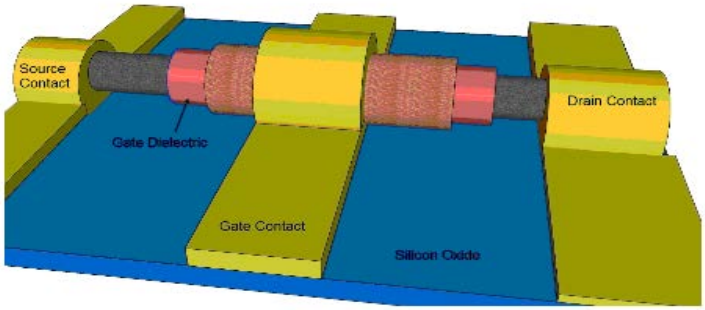


Figure 1.18 Cylindrical Nanowire FET [27]

1.6.1 Electrostatics of Cylindrical Nanowire FETs

In contrast to double gate and FinFET structures, the cylindrical cross-section guarantees that the gate exerts uniform control of the channel potential. Cylindrical NW FETs' electrostatic integrity allows for a subthreshold swing that approaches the thermionic limit of 60 mV/decade with little degradation as the channel length is below 10 nm, according to analytical and numerical studies [50]. In this smoother carrier transport and reduced parasitic effects can be observed as the cylindrical geometry reduces corner effects that are observed in rectangular and triangular nanowire FETs [51].

Cylindrical NW FET provides enhanced scalability, and due to its excellent electrostatic profile scaling length (λ) depends on the channel diameter and gate dielectric properties. Better SCE immunity is directly correlated with a lower λ, which allows for channel lengths as short as 5 nm while still preserving respectable I_{ON}/I_{OFF} ratios [52].

1.6.2 Fabrication of Cylindrical Nanowire FETs

The cylindrical NW FETs can be fabricated by two approaches: top-down or bottom-up fabrication methods. The top-down method defines nanowires by patterning silicon-on-insulator (SOI) substrates or epitaxially grown films using sophisticated lithography and etching techniques [46]. On the contrary, the bottom-up method uses molecular beam epitaxy (MBE) or vapor-liquid-solid (VLS) growth to directly create a nanowire with exact control over composition and diameter [53]. Surface roughness and variability control are a few limitations that are faced by the top-down approach, whereas the bottom-up approach requires sophisticated alignment and integration strategies and offers crystallinity.

The drive (I_{ON}) current of the III-V and Ge-based cylindrical NW FETs can be improved because of their higher carrier mobility and reduced effective mass. In the case of InGaAs nanowire FETs are considered ideal for high-speed and low-power applications because of high drive current [54].

1.6.3 Gate Engineering in Cylindrical Nanowire FETs

By modifying the gate material, dielectric characteristics, work function, and structural design, gate engineering techniques can further optimize the electrostatic superiority of cylindrical NW FETs and improve device performance.

1.6.3.1 Dual-Material Gate (DMG) Structures

The electric field redistribution is achieved in nanowire FETs by introducing two gate metals with different gate functions along the channel length. The dual gate material helps in reducing hot carrier effects, improving transconductance (g_m), intrinsic gain, and suppressing DIBL [55]. When compared with conventional single metal gate the dual metal gate structures have shown significant improvement in analog/RF performance and I_{ON}/I_{OFF} ratio.

1.6.3.2 Gate Dielectric Engineering

The subthreshold characteristics of the FETs are improved by using high-κ dielectrics (like HfO_2, ZrO_2, Al_2O_3), which reduces gate leakages and enhances gate capacitance. Furthermore, in order to balance electrostatic integrity and gate fringing capacitance and achieve optimal performance, hetero-dielectric gate stacks which combine high-κ and low-κ layers have been investigated [56].

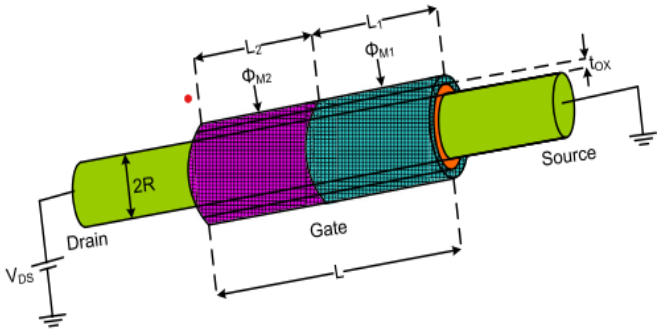


Figure 1.19 Dual Metal Gate Cylindrical FET Structure [57]

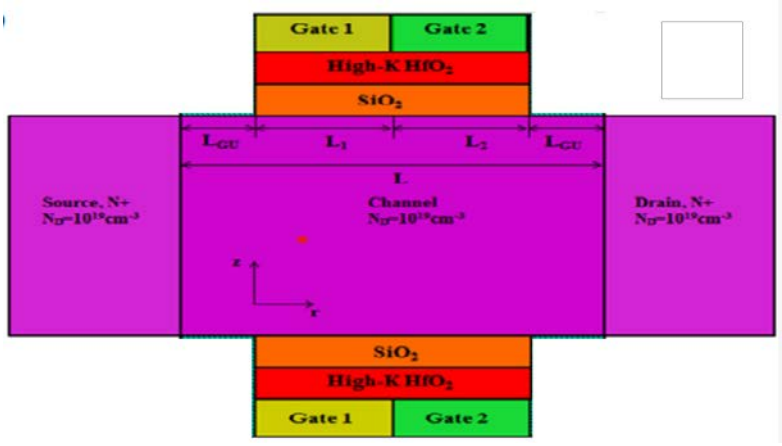


Figure 1.20 Gate Dielectric Engineering Structure [58]

1.6.3.3 Ferroelectric Gate Stacks (Negative Capacitance)

The negative capacitance effect (NC FETs) present in ferroelectric material, when integrated with cylindrical NW FETs, enables a sub-60 mV/decade subthreshold swing, reduces power consumption, and ensures higher I_{ON}. Steep slope transistors that can overcome conventional thermal limits are made possible by this method [47].

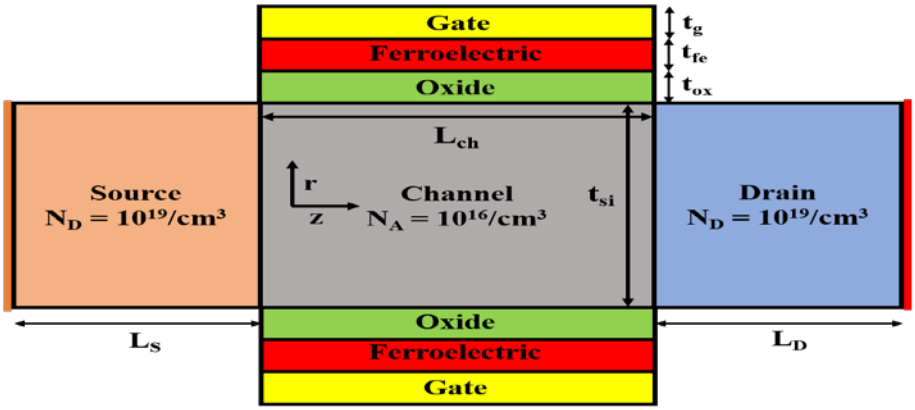


Figure 1.21 Ferroelectric Stack Structure [59]

1.6.3.4 Source/Drain Engineering with Gate Overlap

To reduce access resistance and preserve electrostatic integrity, advanced cylindrical NW FETs make use of optimized gate overlap and raised source/drain contacts. This lowers the parasitic resistance, which is a major drawback of nanoscale transistors [27].

1.6.4 Advantages and Challenges

Cylindrical Nanowire Field-Effect Transistors (NW FETs) have emerged as one of the promising architectures for extending Moore's law beyond the limitations of planar MOSFETs and FinFETs. The cylindrical nanowire FETs are considered as a crucial candidate because of their superior electrostatic control over the channel potential and effective suppression of short channel effects such as Drain Induced Barrier Lowering (DIBL), subthreshold slope degradation, and Gate Induced Drain Leakages (GIDL) [24]. This cylindrical NW FET configuration allows efficient scaling into the sub-5 nm regime because of its electrostatic control over the channel as the gate surrounds the channel, whereas conventional architectures fail to maintain gate control [26].

The cylindrical NW FETs are considered reliable because of their structure, which helps in reducing variability and parasitic effects. The Cylindrical NW FETs are considered over FinFETs because FinFETs suffer from corner effects due to sharp fin edges, whereas because of the cylindrical structure cylindrical NW FETs have predictable behaviour independent of edge-dependent non-uniformities [23]. Furthermore, new channel materials like SiGe, III-V semiconductors, and even newly developed two-dimensional materials like MoS_2 and WS_2 are naturally compatible with the NW FETs. This compatibility opens avenues for high mobility channels allowing increased ON-state current (I_{ON}) and switching in future VLSI systems that use less energy [60].

Despite these advantages, the large-scale integration of NW FETs faces several challenges. In the case of cylindrical NW FETs, it is difficult to achieve uniform nanowire diameters because of their fabrication complexity, which is the main challenge. Surface roughness and process-induced fluctuations can lead to variability that impairs subthreshold swing performance and has a substantial effect on the threshold voltage stability [61]. Furthermore, contact resistance is still a limiting factor; the drive current is negatively impacted by the high parasitic resistance at the source/drain interfaces caused by the smaller contact area in the nanowires [62]. Thermal management is a critical issue because heat dissipation is limited because of the geometry of the nanowires. In high-performance operating conditions can lead to noticeable self-heating effect that lower device reliability and impair the carrier mobility [63].

Consequently, although cylindrical NW FETs offer exceptional potential for producing ultra-scaled, high-performance and low-leakage transistors, their widespread integration in semiconductor manufacturing necessitates advancements in contact engineering, nanofabrication techniques, and thermal management. The feasibility of NW-FET for upcoming technology nodes is being pushed further by research in these areas.

1.6.5 Future Perspectives

Advanced gate engineering combined with cylindrical NW FETs is expected to play a central role in the sub-3 nm technology regime. Cylindrical NW FETs are considered a low-power and high-performance solution for next-generation MOS technology because they integrate dual metal and hetero dielectric gates, high mobility channels, and ferroelectric stacks. Post FinFETs era, the cylindrical NW FETs are considered a crucial device while researching material integration, variability reduction, and process scalability.

1.7 Oxide Stack Engineering

Since the gate oxide directly controls the electrostatic coupling between the gate terminal and the underlying channel, it has always been a crucial component of MOSFET technology. Thermally grown silicon dioxide (SiO_2) was used as the gate dielectric in traditional MOSFETs because of its superior interface quality, chemical stability, and capacity to form a low defect density, near ideal Si/SiO_2 interface [3]. To maintain adequate gate capacitance and channel control, the oxide thickness had to be continuously decreased due to the relentless scaling of MOSFETs. Severe direct tunnelling leakage currents through the ultra-thin oxide layer were caused by the oxide thickness reaching ~1.5 nm -2 nm by the 1990s [64]. Oxide stack engineering has emerged as a key component of advanced device design because of this problem.

11

The ultra-thin SiO_2 layers are susceptible to reliability and breakdown issues such as Time-Dependent Dielectric Breakdown (TDDB) and Bias Temperature Instability (BTI) [64]. The gate capacitance of a MOSFET is given by:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{1.1}$$

Here $t_{ox}$is the physical thickness and $\varepsilon_{ox}$is the permittivity of the oxide layer. As the device is scaled, the t_{ox}should decrease to maintain high gate capacitance and reduce short-channel effects. Quantum mechanical tunnelling dominates electron control as the physical thickness falls below ~1.2 nm, which leads to high standby power consumption and unacceptable gate leakage [25]. These challenges create an urgent need for alternative dielectric materials with higher permittivity values.

1.7.1 High-κ Dielectrics and Equivalent Oxide Thickness

To overcome the previous challenges, the industry transitioned to high-κ dielectrics. In 2007, Intel's 45 nm technology mode was commercialized, which employed HfO_2-based stacks [43]. A small equivalent oxide thickness (EOT) was achieved by introducing a high-κ dielectric material, which physically maintains the thickness of the dielectric layer, and tunnelling is suppressed. EOT was defined as:

$$EOT = t_{ox} \times \frac{k_{SiO2}}{k_{ox}} \tag{1.2}$$

here $k_{SiO2}$is the dielectric constant of silicon dioxide and $k_{ox}$is the dielectric constant of the alternative oxide. The dielectric constant of HfO_2 is ~20, which enables a physical thickness ~5 times larger than SiO_2 while maintaining the same electrostatic control [14]. This innovation extended the scaling of MOSFETs into the sub-20 nm regime and mitigated leakage.

The integration of high-κ dielectrics introduces new challenges such as interface states, fixed charges, and mobility degradation due to remote phono scattering [16]. Due to these effects, high-κ dielectrics are necessarily combined with an ultrathin interfacial SiO_2 layer to preserve the high-quality Si-oxide interface.

1.7.2 Gate Stack Engineering with Metal Gates

Another significant development in oxide stack engineering was the substitution of metal gates for polysilicon gates. High-temperature processing was necessary for poly-Si gates due to poly-depletion effects, which weakened the high-κ dielectrics. Engineers were able to improve channel mobility, remove depletion, and fine-tune the work function for threshold voltage control by implementing metal gates and eliminating depletion [65]. As a result, high-κ/Metal Gate (HKMG) stack became the industry standard at the 45 nm node.

1.7.3 Advanced Oxide Stacks in Nanowire and GAA Devices

As the device architectures evolved because of the scaling from planar MOSFETs to FinFETs and then to Gate-All-Around Nanowire FETs, the oxide stacking had to be adopted for conformal deposition around three-dimensional channels. The deposition of high-κ dielectrics and metal gates in the nanoscale geometries is done by using Atomic Layer Deposition (ALD) as it provides excellent thickness uniformity and interface control [18]. The high-κ deposition is a critical factor as it suppresses the short channel effects (SCEs) and subthreshold leakages in cylindrical nanowire FETs.

Moreover, multi-layer oxide stacks combining materials such as HfO_2, Al_2O_3, and La_2O_3 have been explored to optimize trade-offs between dielectric constants, band alignment, and thermal stability [16]. The device reliability can be improved by incorporating a thin Al_2O_3 layer, which will suppress oxygen vacancies in HfO_2 and reduce the interface states.

1.7.4 Emerging Trends: Ferroelectric Oxide and Negative Capacitance

Recently, ferroelectric high-κ oxides, like HfO_2, have also been subjected to oxide stack engineering in order to achieve Negative Capacitance FETs (NCFETs) [47]. The traditional thermionic limit of sub-60 mV/decade subthreshold slopes can be broken, and leakage can be further reduced by taking advantage of the intrinsic negative capacitance effect of ferroelectric materials. At the forefront of low-power and ultra-scaled nanowire FET design at the moment, these oxide engineering techniques provide avenues for technologies beyond CMOS.

1.8 Motivation for Low Leakage Nanowire FETs

For over five decades the Moore's Law has predicted the scaling of MOSFETs accurately, and since then, this scaling phenomenon has been the driving force behind the exponential growth of the semiconductor industry. As the technology nodes have entered the sub-20 nm regime, they are experiencing challenges that are limiting the device performance, such as leakage currents and other short-channel effects (SCEs). These challenges are also affecting the reliability and energy efficiency of the device. In modern applications, leakage minimization is an important parameter as maximizing ON-state current for various applications like ultra-low power processors, wearable electronics, Internet of Things (IoT) devices, and biomedical sensors. Various architectures are discussed nowadays, among all these, nanowire field effect transistors (NW-FETs) with gate-all-around (GAA) geometry offer superior electrostatic control that mitigates the leakage currents [37], [48]. Here, the source of leakage, its impact on device performance, and the motivation for exploring low leakage nanowire FETs for future electronics are elaborated.

1.8.1 Source of Leakage in Nanoscale Devices

In nanoscale MOSFETs, the presence of multiple leakage current mechanisms has become one of the most critical concerns influencing static power dissipation, overall circuit stability and device reliability. As transistor dimensions continue to scale down aggressively into the sub-10 nm regime, various electrostatic effects and quantum mechanical effects begin to dominate, resulting in non-ideal leakage behaviour that limits further performance enhancement. One of the major sources of leakage is gate oxide tunnelling, which arises due to the ultra-thin gate dielectric layers used in the modern transistors. When the oxide thickness is reduced below 2 nm, the potential barrier between gate and channel becomes sufficiently thin to permit direct tunnelling of carriers through the dielectric leading to exponential increase in gate leakage currents [3]. The introduction of high-κ dielectric materials, such as ZrO_2 or HfO_2 has mitigated this issue to some extent by allowing physically thicker layers while maintaining high capacitance. However, the defects and trap states with in high-κ films often act as leakage pathways, contributing to trap assisted tunnelling and long-term

dielectric degradation [14]. Another dominant mechanism is subthreshold leakage, which originates from the finite subthreshold slope (SS) in MOSFETs. Aven when the transistor is in OFF-sate, thermally generated carriers in the channel diffuse between the source and drain, producing a weak but non-negligible current. In an ideal case, the subthreshold slope of a device should be 60 mV/decade at room temperature for thermionic emission. However, due to the short channel effects (SCEs) such as DIBL, the subthreshold slope becomes steeper, resulting in worsening the leakages and reducing the switching efficiency [16].

A further source of leakage, known as Gate Induced Drain Leakage (GIDL), occurs primarily at the drain-gate overlap region when a higher drain bias is applied while the gate voltage is low or zero. The resulting band bending in the surface potential promotes tunnelling-assisted carrier generation from valence band to the conduction band, leading to excess drain current even when the device is normally turned off. This mechanism becomes more prominent with thinner gate dielectrics and higher electric fields, directly increasing standby power dissipation [66]. Similarly, Band-to-Band Tunnelling (BTBT) is another critical leakage pathway, especially in ultra-thin body devices or steeply doped junctions, where high local electric fields enable electrons to tunnel directly from the valence band to the conduction band across the drain junction. This process dominates the OFF-state leakage at aggressive technology nodes and is highly sensitive to both channel doping profiles and gate dielectric integrity [11].

Collectively these leakage mechanisms like gate oxide tunnelling, subthreshold conduction, BTBT and GIDL significantly impact static power consumption, long term reliability and device variability in deeply scaled MOSFETs. The effective mitigation of these leakages requires a multifaceted strategy involving advanced dielectric materials, optimized doping, novel transistor architectures and channel engineering such as multi gate FETs, FinFETs and nanowire-based transistors. Understanding and suppressing this leakage phenomena remain fundamental research challenges in the continuous pursuit of energy efficient nanoscale device design.

1.8.2 Impact of Leakage on System Performance

In modern semiconductor technology, leakage currents account for a significant portion of total chip power when sub-100 nm technology nodes are considered, influencing device reliability, system performance and power efficiency. The International Technology Roadmap for Semiconductors (ITRS) identifies leakage power as major contributor to total chip power consumption, especially for devices operating near and below the 90 nm node, where short channel effects (SCEs), high electric field intensities and thin gate oxides exacerbate parasitic conduction paths [9]. As devices scale down further, the contribution of leakage power to overall power dissipation continues to grow, sometimes accounting for over 50% of total power in low-activity or standby states [61]. This results in serious implications at both device level and system level affecting thermal management, static power dissipation, voltage scaling feasibility and signal integrity.

One of the primary consequences of high leakage is the emergence of thermal management issues. The power lost through leakage manifests as unwanted heat generation, which elevates the junction temperature and accelerates self-heating

effects within densely packed transistor arrays. Such localized heating can degrade carrier mobility, alter threshold voltage and induce thermal runaway, which collectively reduce device lifespan and increase cooling overheads [43]. Additionally, reduced noise margins and reliability are major side effects of persistent leakage. The continuous flow of subthreshold or gate tunnelling currents can distort voltage levels, compromise signal integrity and increasing logic error susceptibility. Over prolonged operation, this degradation accelerates failure mechanisms such as time-dependent dielectric breakdown (TDDB) and negative bias temperature instability (NBTI), leading to long-term instability in circuit behaviour [60].

Excessive leakage also results in increased static power dissipation, a serious problem from battery-operated systems, large scale data centers and portable electronics, where a significant portion of transistors remain in ideal or standby conditions. Even without switching activity, GIDL, BTBT and subthreshold leakages continue to consume power leading to energy insufficiency, increased cooling requirements and higher operational costs [67]. Furthermore, leakage presents a barrier to ultra-low voltage operation, which is critical for next generation energy efficient computing such as Internet of Things (IoT) devices, near threshold logic and neuromorphic systems. As the supply voltage (V_{DD}) scales below 0.5 V the ratio of leakage to active current increases dramatically, effectively offsetting the energy savings expected from voltage scaling and limiting the scope pf low-power designs [48].

Hence leakage minimization has become a multi-dimensional design challenge spanning materials, system architectures and device physics. At the material level, innovations such as high-κ/metal gate stacks and strain-engineered channels aim to reduce gate and subthreshold leakage. At the device level, architectures like FinFETs, gate-all-around (GAA) FETs, and nanowire transistors provide superior electrostatic control, thereby suppressing SCE induced leakages. At the circuit and system level, multi threshold design, power gating techniques and adaptive body biasing are employed to reduce standby power dynamically [68]. Therefore, in advanced semiconductor systems, controlling leakage is not merely a device optimization problem but a system level imperative that dictates the future of scalable, energy efficient and reliable nanoelectronics.

1.8.3 Motivation for Nanowire FETs

With the progressive miniaturization of semiconductor devices, traditional transistor architectures such as planar MOSFETs and FinFETs face serious limitations in maintaining leakage suppression, scalability and electrostatic control at technology nodes below 5 nm. Among the various emerging device architectures, the Cylindrical Nanowire Field Effect Transistor (NW FETs) has gained significant attention as a next generation transistor design capable of addressing these challenges through its unique three-dimensional geometry and superior electrostatics.

A major advantage of nanowire FETs lies in their excellent scalability to sub-5 nm regime. Both experimental and simulated studies have demonstrated that nanowire-based transistors can sustain strong electrostatic integrity, low DIBL and superior leakage control, even under extreme scaling conditions where FinFETs begin to exhibit degraded performance [69]. The cylindrical geometry of the nanowire channel offers

nearly ideal electrostatic gate control, enabling a significant reduction in short channel effects (SCEs) while maintaining high ON current and low OFF current. This intrinsic advantage makes nanowire FETs highly suitable for ultra scaled CMOS technology nodes, ensuring both power efficiency and device reliability.

A second key feature is the Gate-All Around (GAA) electrostatics, which distinguishes nanowire FETs from other transistor geometries. In this structure, the gate electrode completely wraps around the channel, providing maximum gate-to-channel coupling. This 360° gate coverage allows for uniform potential control along the entire channel surface, resulting in the steepest subthreshold slope (SS) and minimal DIBL among all GAA architectures [48]. Comparative studies have shown that cylindrical GAA NW FETs exhibits improved subthreshold behaviour and higher current drivability than FinFETs and nanosheet FETs, making them a preferred option for leakage limited applications.

Additionally, engineered oxide stacks play a crucial role in minimizing gate tunnelling leakage. By employing high-κ dielectric materials such as HfO_2, ZrO_2 or $HfZrO_x$ composites, a larger physical oxide thickness can be maintained while achieving a low equivalent oxide thickness, effectively suppressing direct tunnelling currents through the gate dielectric [49]. Moreover, advanced multi-layer oxide engineering enables bans offset tailoring, which reduces trap assisted tunnelling and enhanced dielectric reliability. The GAA geometry further complements this effect by providing uniform electric field distribution, thereby reducing oxide stress and hot carrier degradation.

Another promising aspect is the potential for bandgap and strain engineering in nanowire-based transistors. By selecting appropriate channel materials such as SiGe, II-V compound semiconductors (InGaAs, GaN), or 2D materials (MoS_2, WS_2) and applying uniaxial strain, it is possible to enhance carrier mobility, modulate band alignment and optimize effective mass all of which contribute to lower leakage currents without compromising on state performance [27]. These design freedoms allow nanowire FETs to outperform conventional architectures in analog/RF performance, energy efficiency and scalability while remaining compatible with CMOS integration processes.

In summary, the Cylindrical Nanowire FET effectively combines superior electrostatic control, optimized gate stack engineering and material adaptability, offering a robust platform for the continued scaling of transistors beyond the 5 nm technology node. Its inherent capability to mitigate short channel effects, suppress gate and subthreshold leakages and accommodate heterogeneous materials positions it as one of the most promising architectures for future energy-efficient nanoelectronics devices.

1.8.4 Towards Low-Power Applications

With the growing demand for energy-efficient electronics, the development of low-leakage nanowire field effect transistors (NW FETs) has become a cornerstone of modern device research, enabling sustainable operation across diverse application domains. As transistor dimensions shrink and conventional architectures struggle with leakage-induced power loss, nanowire FETs owing to their superior electrostatic control, gate-all-around (GAA) structure and scalable geometry emerge as promising

candidates for ultra-low power electronics. Their ability to operate with minimal standby power consumption, enhanced thermal stability and reduced subthreshold leakage makes them particularly attractive in domains that demand continuous operation under constrained energy budgets.

One of the most prominent domains is the Internet of Things (IoT) and wearable electronics, where devices often function in ON modes and rely on limited power source such as miniature batteries or energy harvesters, in such scenarios, standby power consumption becomes a determining factor for device lifetime and operational efficiency. The leakage-resilient characteristics of nanowire FETs significantly extend battery endurance and support near threshold voltage operation, which is essential for low-frequency sensing and intermittent communication systems [70]. Similarly, biomedical and implantable devices benefit immensely from low leakage transistors, as excessive leakage current not only wastes energy but also generates localized heat, which can adversely affect biocompatibility and sensor reliability. The thermal efficiency and low static power dissipation of nanowire-based transistors ensure safer operation in bio-implantable electronics, bio signal amplifiers and neural interfaces, where even slight temperature variations can influence biological tissues [71].

In the domain of edge computing and artificial intelligence (AI) accelerators, energy-efficient engines are deployed close to data sources to minimize latency and power overheads. These systems demand high computational throughput under strict power constrains, where leakage current minimization directly correlates with sustained inference efficiency and thermal reliability [66]. The nanowire architecture, with its enhanced electrostatic and reduced parasitic capacitances enables voltage scaling without performing degradation, aligning with the needs of edge AI hardware for low-power inferencing and event-driven computation. Furthermore, in large-scale data centers, the cumulative energy impact of leakage becomes enormous due to the billions of transistors operating simultaneously. Even marginal reductions in per device leakage translates into significant reductions in static power and global energy savings, addressing both economic costs and environmental sustainability concerns [72].

Hence the development of low-leakage nanowire FETs is not merely a continuation of transistor scaling trends but a strategic step towards sustainable semiconductor design. These architectures enable operation under near threshold or subthreshold regimes, ensuring long term reliability, thermal stability and power efficiency. By addressing both scaling induced physical limitations and system level energy demands, nanowire-based devices represent a key enabler of next generation low-power electronics, driving innovation across IoT, health care, AI computing and green data infrastructures.

1.9 Thesis Organization

The thesis entitled "***Study and Design of Low Nanowire Field Effect Transistor***" is structured into six chapters. Each chapter is designed to build upon the previous one, thereby providing a logical flow from fundamental concept to advanced device modelling and concluding perspectives. The overall organization is summarized below:

- **Chapter 1: Introduction**

The opening chapter sets the foundation of the research by highlighting the motivation, scope, and objectives of the work. It reviews the evaluation of nanoscale FETs, scaling issues in conventional MOSFET architectures, and the transition towards Gate-All-Around (GAA) nanowire transistors as a potential solution. This chapter also surveys current developments and outlines the significance of GAA-FETs in future sensing and electronic applications, along with a survey of state-of-the-art developments in this domain.

- **Chapter 2: Literature Review**

Building on the introductory framework, this chapter includes a thorough overview of the literature, which is provided for a variety of devices that aim to either replace or supplement conventional complementary MOSFETs. It is demonstrated that several devices have some merits that outperform MOSFETs. Due to the significant variations between simulated and manufactured devices, GAA FETs are the focus of continuing study. Further, the study of different transistors has been incorporated with GAA FETs to overcome their limitations. This section presents a detailed survey on Short Channel Effects (SCEs), with a primary focus on Gate-Induced Drain Leakage (GIDL) and the temperature-dependent impact of GIDL in nanowire Field-Effect Transistors (FETs). The main focus of this study is to combine the macaroni-induced structure and ferroelectric structure with GAA FETs to get enhanced performance and fabrication feasibility. To bridge these limitations, the chapter introduces the rationale for incorporating macaroni-type structures and ferroelectric layers into GAA FETs, an idea that becomes central to the modelling and design efforts explored in the subsequent chapters.

- **Chapter 3: Analytical Modeling of Channel Engineered Macaroni Induced Gate-All-Around Field Effect Transistor (CE-MI-GAA FET)**

Following the review of literature and identification of research gaps, this chapter includes the design analysis and modelling of the first proposed structure: Channel Engineered Macaroni Induced Gate-All-Around Field Effect Transistor (CE-MI-GAA FET). It contains a detailed analysis of a single-gate FET and with single-gate macaroni FET. Here, all the methods and models used for simulation in Silvaco TCAD are discussed in depth. Several performance parameters are discussed that are crucial for reducing Short Channel Effects (SCEs). Various parameters like Gate Induced Drain Leakage (GIDL), Drain Induced Barrier Lowering (DIBL), and Subthreshold Slope (SS). Various simulated parameters of the FETs are analytically verified. This chapter sets the stage for advancing towards more complex device structures by demonstrating the benefits of channel engineering in suppressing SCEs.

- **Chapter 4: Analytical Modeling and Numerical Simulation of Double-Gate Macaroni Channel Field Effect Transistor**

Expanding upon the concepts introduced in Chapter 3, this chapter includes the design analysis and modelling of the Double Gate Engineered Macaroni Induced FET to further enhance the electrostatic control. Here, all the methods and models used for simulation in Silvaco TCAD are discussed in depth. Several performance parameters are discussed that are crucial for reducing Short Channel Effects (SCEs). Various parameters like Gate Induced Drain Leakage (GIDL), Drain Induced Barrier Lowering (DIBL), Surface Potential, and Subthreshold Slope (SS). Various parameters are analytically derived, such as Gate Induced Drain Leakage (GIDL) and surface potential, using 2D Poisson's equation. The analytical results derived from the model in this way were validated with simulation results obtained using the ATLAS TCAD simulator, which shows good agreement. This progression from single gate to double gate design demonstrates how structural modifications can systematically mitigate short channel degradation, thereby preparing the ground for incorporating ferroelectric effects.

- **Chapter 5: Design and Modelling of Negative Capacitance Ferroelectric Nanowire Field Effect Transistor for Leakage Minimization**

Building upon the double gate macaroni device framework, this chapter integrates ferroelectric materials into the gate stack to exploit the negative capacitance effect. It involves the design and analysis of the Single Gate and Dual Gate Ferroelectric FET in detail. The impact of temperature variation has also been studied on various parameters. The analytical surface potential model for different regions of the proposed structure has been developed by using Poisson's equation and Landau-Khalatnikov equation. Analytical results derived from the model in this way were validated with simulation results obtained using the ATLAS TCAD simulator, which shows good agreement. This chapter thus represents the culmination of the proposed design strategies, linking structural engineering with material innovation.

- **Chapter 6: Conclusion, Future Directions, and Social Impact**

The final chapter provides a consolidated summary of the major findings from the thesis. This chapter underscores the contributions of macaroni-channel engineering and ferroelectric integration in improving nanowire FET performance. It highlights the analytical and simulation-based contributions of the work, reflects on the advantages of the proposed nanowire GAA FET designs, and suggests potential directions for future research. Beyond the technical achievements, the chapter also highlights the broader societal and technological implications of adopting such devices in next-generation electronics and sensing platforms, thereby completing the narrative of the thesis. The flow chart of thesis organization is shown in figure 1.22.

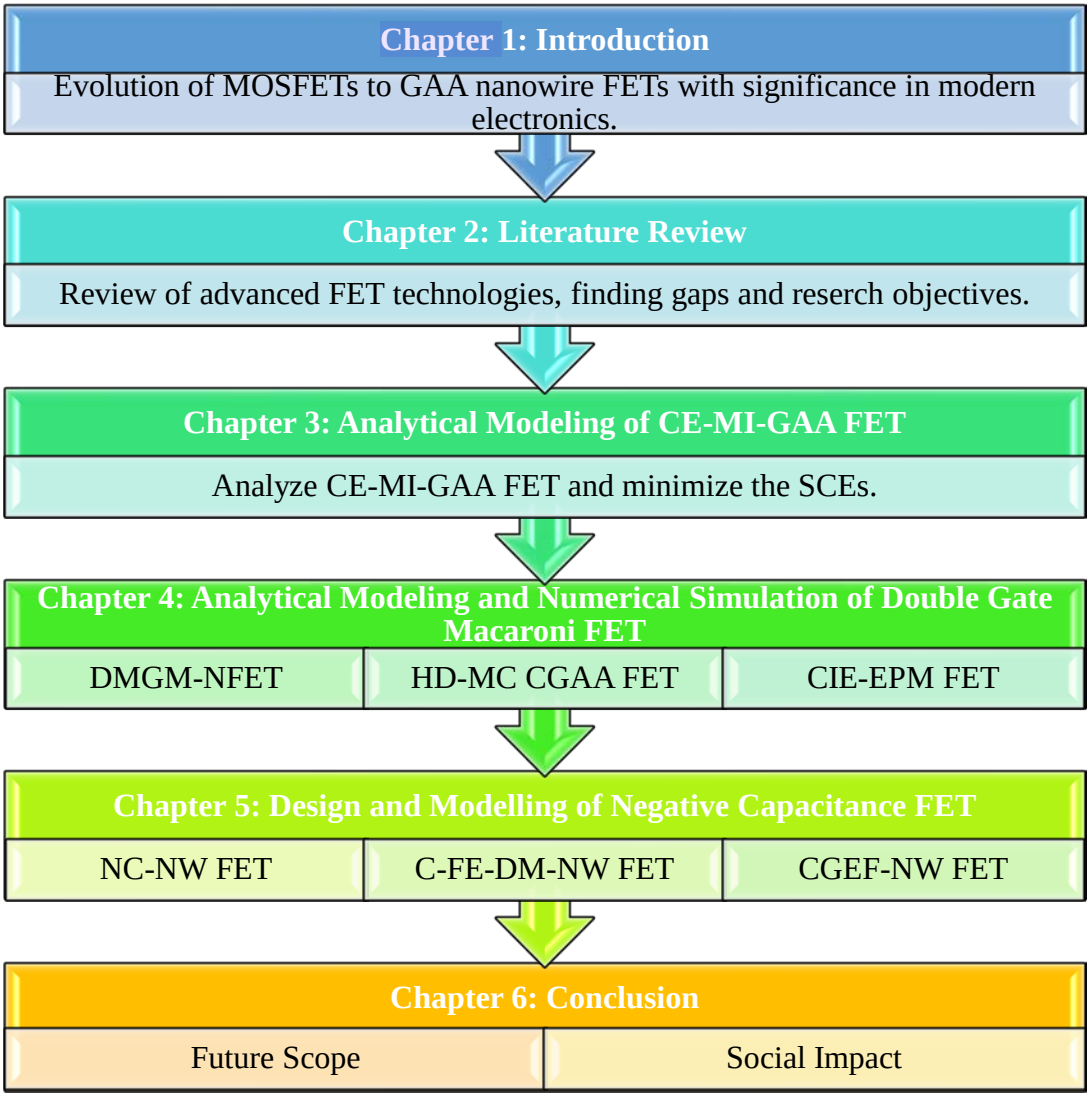


Figure 1.22 Thesis Organization Flow Chart.

CHAPTER 2

LITERATURE SURVEY

In the previous chapter, the introduction outlined the motivation for this research, focusing on the challenges encountered in modern CMOS technology as dimensions of the devices continue to scale down. With each new node of technology, maintaining device reliability and performance becomes increasingly complex due to the increasing influence of band-to-band tunnelling (BTBT), variability issues, short channel effects (SCEs) and gate induced drain leakage (GIDL). Simultaneously the demand for high frequency and low power applications requires device architectures that can deliver both robust analog/RF and improved electrostatic characteristics [73].

Among several device structures investigated over the past two decades, nanowire and gate all around (GAA) FETs have emerged as strong candidates owing to their excellent electrostatic integrity. Further enhancement through hollow body macaroni channels, hetero dielectric stacking, dual metal gate (DMG) engineering and negative capacitance (NC) integration have also been discussed aiming to suppress leakage currents and improve device scalability. While these innovations have provided significant improvements, they also bring new challenges related to hysteresis, fabrication complexity and temperature stability leaving important gaps in the literatures [74].

To build a better understanding of these developments, the present chapter surveys the existing body of work in a structured manner. The review begins with the discussion of analytical and compact modelling approaches, since these models provide the essential framework for understanding device physics at nanoscale dimensions. Analytical solutions of Poisson's equation, charge based models and compact formulations have been widely used to predict subthreshold slope, drain current, leakage mechanism and threshold voltage [75]. These models not only explain the fundamental electrostatics of cylindrical, nanowire and macaroni devices but also act as the basis for developing circuit compatible compact models, which are indispensable for design and simulation at system level.

2.1 Analytical and Compact Modeling Approaches

Scaling of MOSFET devices into nanometer dimensions has created the urgent need for accurate analytical and compact models that can capture electrostatics, short channel effects (SCEs) and transport for advanced structures such as nanotubes, nanowires, negative capacitance FET and macaroni MOSFETs [76]. Unlike purely numerical TCAD simulations, analytical frameworks allow faster design space exploration, suitability and deeper physical insight for circuit level SPICE simulations. Over the past decade several works have progressively improved analytical models to include effects such as DIBL, GIDL, NC induced amplification, variability and quantum confinement, which are essential for reliable nanoscale CMOS design.

Early models for fully depleted cylindrical MOSFETs [77], [78] derived threshold voltage and I-V characteristic expression by using Poisson's equation in cylindrical coordinates. These models explained that the cylindrical symmetry provides superior electrostatic control when compared with the planar geometries, resulting in reducing SCEs. Subsequent refinements [79] incorporated quantum confinement using Green's function-based methods, demonstrating that quantization raises threshold voltage but can be stabilized through ferroelectric negative capacitance layers.

Macaroni MOSFETs which employ hollow cylindrical channel motivated the development of semi-analytical models [80], [81], [82]. These works highlighted the concept of characteristic length as a scaling parameter, showing that thinner silicon shells improve gate control but exacerbate variability. Later work introduced compact BSIM-CMG compatible models for circuit simulation of macaroni NAND arrays enabling realistic assessment of delay coupling effects and gain.

Analytical work also extended to reconfigurable and biosensing devices [83]. Spacer engineering nanowire Schottky barrier FETs were modeled to show how biomolecules immobilization alters electrostatics, drain current and shifting threshold voltage. These studies provided frameworks for extending compact models beyond digital logic into bioelectronics and sensing.

Short-channel and leakage effects were integrated into several models. An analytical formulation of temperature-dependent GIDL currents in dual metal nanowire FETs solving Poisson's equation under non uniform boundary conditions is presented [84], [85]. Similarly recessed gate cylindrical JL-NW FE FET that incorporated ferroelectric effects into SCE modelling, showing that ferroelectric layer helps in mitigating threshold roll off at scaled lengths [86].

Collectively these modeling efforts demonstrated a clear trajectory from basic electrostatics of cylindrical MOSFETs to macaroni and JL structures and finally NC and ferroelectric enhanced FETs. The analytical frameworks not only explain physical device phenomenon but also provide compact models usable in circuit simulation platforms bridging the gap between device physics and VLSI design.

TABLE 2.1 ANALYTICAL AND COMPACT MODELLING APPROACHES

First Author (Year)	Paper Title	Summary
Colinge et al. (2002)	Analytical Model for Threshold Voltage of Cylindrical Fully Depleted MOSFETs.	Derives threshold voltage model using Poisson's equation in cylindrical coordinates.
Chattopadhyay et al. (2014)	Analytical Model for Threshold Voltage and I-V characteristics of Fully Depleted Cylindrical MOSFETs.	Extracts cylindrical MOSFET model with explicit I-V characteristics under short channel effects.
Banerjee & Chauhan (2020)	Analytical Modeling of SCEs in MFIS NCFET Including Quantum Effects.	Provides Green's function-based model integrating NC and quantum confinement effects.
Nguyen-Gia et al. (2019)	Characteristic Length of Macaroni Channel MOSFET	Analytical model of characteristic length showing improved SCE immunity in macaroni MOSFETs.

Paolucci et al. (2016)	Semi-Analytical Model for Macaroni MOSFETs for 3D NAND Applications.	Uses exact Poisson solution and Pao-Sah to model subthreshold and tunnelling currents.
Nguyen-Gia et al. (2020)	Models of Threshold Voltage and Subthreshold Slope for Macaroni MOSFETs.	Derives compact models for threshold and subthreshold slope under scaling conditions.
Kim et al. (2019)	BSIM-CMG Modelling for 3D NAND Cell with Macaroni Channel.	Develops compact BSIM-CMG model for macaroni NAND cells validated against TCAD.
Shafizade et al. (2021)	Charge-Based Modelling of Ultra Narrow JL Nanowire FETs.	Proposes a quantum corrected charge-based model for JL-NW FETs.
Raut & Nanda (2022)	Charge Based Analytical Model for GAA JL-FET Including Interface Traps.	Captures trap-induced effects on drain current, electrostatics and RF metrics.
Thakur et al. (2024)	Analytical Modelling of Spacer Engineered Reconfigurable SiNW SBT for Biosensing.	Demonstrates spacer engineered SiNW model for dual mode biomolecule detection.
Goel et al. (2019)	Temperature Dependent GIDL Modelling of DM-NWFETs.	Derives analytical framework for GIDL current under thermal variation.
Singh et al. (2025)	Modelling of Recessed Gate Cylindrical JL- Nanowire FE-FETs.	Proposes recessed gate model showing improved SS, linearity and leakage control.

2.2 Gate Induced Drain Leakage (GIDL) and Leakage Suppression Techniques

As MOSFETs are scaled below 20 nm regime, Gate Induced Drain Leakage (GIDL) became one of the most critical parasitic phenomena limiting device performance. GIDL arises due to band-to-band tunnelling (BTBT) at the drain gate junction overlap, especially under high drain bias and weak gate control. It contributes significantly towards the I_{OFF}, increases static power dissipation and comprises subthreshold behaviour. Suppressing the GIDL therefore remains a core focus of advanced device design, particularly for nanosheet, nanowire and negative capacitance-based FETs [87].

One of the earlier works in these areas provided an analytical study of GIDL in GAA nanowire MOSFETs, thereby identifying tunnelling mechanisms and field dependencies [88]. The analysis showed that the cylindrical architecture enhances the gate control and reduce leakage current compared to the planar MOSFETs. Subsequent refinements introduced dual metal gates and hetero dielectric engineering [89], [90], demonstrating how electrostatic optimization could redistribute the electric field at the drain junction thereby lowering tunnelling probability.

Cylindrical dual metal hetero dielectric GAA MOSFETs [91] in particular demonstrated strong leakage suppression while improving ON current, indicating the multi material gate engineering is a promising route. Furthermore, improvements were made by employing shallow extension engineering [92], which reduces the vertical electric field at the drain junction suppressing BTBT while simultaneously enhancing analog figure of merit and intrinsic gain.

Other architectural strategies included the design of dual metal insulated shallow extension (ISE) MOSFETs [93] and asymmetric gate stack triple metal GAA MOSFETs [94], both of which supported the gate stack engineering as a prominent candidate for suppression of leakages without compromising scalability. Similarly, gate stack dual metal nanowire MOSFETs [95] were proposed for high frequency applications, balancing analog gain and leakage reduction.

Beyond structural approaches, material engineering also played a significant role. Experimentally, analyzed GIDL in SiGe pFETs confirmed phonon assisted BTBT as the dominant mechanism [96]. A detailed electric-field and temperature dependent model of GIDL activation energy, showing the coexistence of tunnelling and trap charge mechanisms [97]. Most recently an experimental study of GIDL in stacked nanowire and nanosheet SOI nMOSFETs, confirming that leakage worsens with temperature [94].

Integration of nanowire with negative capacitance (NC) device has introduced additional complexity. GIDL in MFIS verses MFMIS NC FinFETS were analyzed [47], showing that polarization gradients can either exacerbate leakage or relax. The improper capacitance matching destabilized NC operation and worsen GIDL [98]. Hence NC FETs require careful optimization of gate stack and ferroelectric design to maintain steep slopes without leakage penalties.

Collectively the literature suggests that GIDL suppression is a multi-dimensional challenge. Approaches span structural engineering (dual metal, asymmetric gates, shallow extension), material optimization (SiGe, ferroelectrics, high-κ oxides) and variability- aware design (trap-assisted, thermal effects). While significant suppression has been achieved, hysteresis in NC devices, process variability in poly-Si and thermal degradation in nanosheets still remain open challenges.

TABLE 2.2 GATE INDUCED DRAIN LEAKAGE (GIDL) AND LEAKAGE SUPPRESSION TECHNIQUES

First Author (Year)	Paper Title	Summary
Chattopadhyay et al. (2012)	Analysis of GIDL in Gate-ALL Around Nanowire MOSFETs.	Identifies tunnelling based leakage mechanism in GAA nanowires.
Dasgupta et al. (2017)	GIDL Reduction in Cylindrical Dual Metal Hetero Dielectric GAA MOSFET.	Shows dual metal and dielectric engineering reduced GIDL while boosting I_{ON}.
Goel at al. (2018)	Novel Design to Improve Band-to-Band Tunnelling and GIDL in Cylindrical GAA MOSFETs.	Proposes modified GAA MOSFET structures to minimize tunnelling leakage.
Roy et al. (2018)	Dual Metal Insulated Shallow Extension GAA MOSFET for Reduced GIDL.	Introduces ISE techniques to suppress leakage and improve analog gain.
Sarkar et al. (2019)	Asymmetric Gate Stack Triple Metal GAA MOSFET.	Uses asymmetric triple metal gate stack to suppress GIDL.
Roy et al. (2020)	Gate Stack Dual Metal Nanowire FET for RF Applications.	Reduces leakage and enhances RF figure of merit with dual metal stacks.

Mishra et al. (2019)	SEE-DM-SG MOSFET GIDL Modelling.	Develops analytical GIDL model for shallow extension engineered devices.
Tiwari et al. (2014)	Analysis of GIDL in SiGe Channel pFETs.	Experimental study confirming phonon assisted BTBT in SiGe channels.
Alnuaimi et al. (2013)	Electric Field & Temperature Dependence of GIDL Activation Energy.	Explains GIDL via Poole-Frenkel, TAT and BTBT effects.
De Souza et al. (2023)	GIDL in SOI Stacked Nanowire and Nanosheet MOSFETs.	Experimental assessment showing leakage worsens with temperature and fin width.
Min et al. (2020)	GIDL in MFMIS vs MFIS NC FinFETs.	Shows polarization gradient effects govern leakage tradeoffs in NC-FinFETs.

2.3 Negative Capacitance and Ferroelectric FETs (NC FETs)

The introduction of negative capacitance (NC) in ferroelectric materials represents one of the most transformative concepts in transistor research. First proposed by Salahuddin and Datta on 2008, the idea was by exploring the unstable region of ferroelectric polarization, a ferroelectric capacitor can provide voltage amplification when placed in series with the gate dielectric. This mechanism allows reduction of subthreshold swing (SS) below the Boltzmann limit of 60 mV/decade thus addressing one of the most fundamental barriers to low power device scaling.

The earliest theoretical foundation was provided by Landau-Khalantnikov (LK) modelling [47], [99], [100]. Experimental validation followed in nanoscale PZT-STO heterostructures [101], where capacitance enhancement confirmed the NC effect, and later in epitaxial ferroelectric capacitors [102], where transient measurements captured negative differential capacitance during polarization switching. The hysteresis free NC in $HfZrO_2$ (HZO) with thin Al_2O_3 interlays, providing that CMOS compatible ferroelectrics could stabilize NC at high speeds.

Building on these foundations, various device level demonstrations emerged. Fabricated NC FinFETs with HZO gate stacks [103], reported bi-directional sub-60 mV/decade SS, negative DIBL and improved short channel effects (SCEs). This was extended to junctionless nanowire NC-FETs, showing enhanced I_{ON}/I_{OFF} ratios and guidelines for HfO_2 ferroelectric thickness optimization [104]. Junctionless Accumulation Mode FE FETs (JAM FE FETs) demonstrated improvements in transconductance, cutoff frequency and gain, positioning NC devices as promising candidates for high frequency mixed signal design [105].

At the modelling level, compact and analytical models were developed to predict NC behaviour under scaling. A compact NC FET model that captures sub kT SS, negative differential resistance (NDR) and reverse DIBL was build [106]. A surface potential based I-V model for MFIS NC-GAA FETs was developed explicitly incorporating interface trap effects [107]. Analytically quantum confinement effects were introduced in double gate MFIS-NCFETs showing that confinement elevates threshold voltage but is offset by NC amplification [108].

Temperature dependence became a key research focus. NC effects degrade with increasing temperature due to weakened ferroelectric polarization was experimentally shown [109], though NCFETs still out perform conventional MOSFETs. A fully coupled TCAD LK framework showing NC vanishes above 500 K but strengthens at cryogenic conditions was introduced [110]. This was extended to JAM FE FETs confirming SS degradation with temperature rise [111].

In addition to digital switching, NC devices were also studied for RF and analog performance. NC FETs exhibit negative output differential resistance which if engineered can enhance intrinsic gain was also shown [112]. Electrostatically doped FE Schottky Barrier TFETs with PZT gates were proposed for achieving improved g_m/I_d and cutoff frequencies [113]. HDDP-DG NC FETs with terahertz cutoff frequencies (2.65 THz) and superior linearity metrics were demonstrated [114].

Another critical research concerns hysteresis suppression. A hysteresis free NC effects can arise not only from capacitance matching but also from leakage and trap assisted charge boosting, offering an alternate expiation for experimental observations was discussed [115]. A variability aware conservative design strategy, ensuring hysteresis free operation under ±3% material variation was provided [116].

In summary, NC FET research has rapidly evolved from theoretical proposals to experimental demonstrations and system level modelling. Ferroelectric integration with CMOS compatibility oxides like HZO is particularly promising but challenges remain in hysteresis control, variability and thermal stability. Nonetheless, NC FETs consistently achieve steep slopes, enhanced analog performance and improved SCE immunity, making them as front runners for next generation low power VLSI and RF technologies.

TABLE 2.3 NEGATIVE CAPACITANCE AND FERROELECTRIC FETS (NC FETS)

First Author (Year)	Paper Title	Summary
Salahuddin & Datta (2008)	Use of NC to Provide Voltage Amplification for Low Power Devices.	Proposes NC as a voltage amplifier enabling SS < 60 mV/decade.
Khan et al. (2011)	Experimental Evidence of Ferroelectric NC in Heterostructures.	First proof of stabilized NC in PZT-STO bilayers.
Khal et al. (2014)	Negative Capacitance in a Ferroelectric Capacitor.	Demonstrates transient NC during polarization switching.
Hoffmann et al. (2018)	High Speed Hysteresis Free NC in HZO.	Shows hysteresis free NC in HZO/Al_2O_3 stacks.
Zhou et al. (2018)	NC n-Channel Si FinFETs with Sub-60 mV/decade.	Fabricates NC-FinFETs with negative DIBL and improved SCEs.
Choi et al. (2019)	Design Guidelines for JL-NW NCFETs with HfO_2.	Provides design rules for JL-NCFETs with HfO_2 ferroelectrics.
Yadav et al. (2022)	JAM-FE-FET for High Frequency Applications.	Proposes JAM-FE-FET with enhanced gain, cutoff frequency and transconductance.
Dong & Guo (2017)	Compact NC FET Model with Electrostatic SCEs.	Compact model predicting NDR, SS and reverse DIBL.

Kim et al. (2021)	Analytical I-V Modelling of MFIS NC GAA FET.	Surface potential based I-V model with interface traps.
Pandey & Chauhan (2020)	Analytical Modelling of SCEs in MFIS NCFETs with Quantum Effects.	Included quantum confinements in NC electrostatics.
Jo & Shin (2015)	Impact of Temperature on NCFETs.	Shows SS degradation from 14.8 to 24.3 mV/decade between 300-400 K.
Wang et al. (2020)	Temperature Effects on HZO Based NCFETs.	Shows faster SS and I_{ON} degradation in HZO-NCFETs.
Raol et al. (2021)	Fully Coupled Simulation of Temperature Effects in NC Devices.	Shows NC vanishes above 500 k, strengthens at cryogenic temperatures.
Yadav et al. (2023)	Temperature Effects on JAM-FE FETs.	Demonstrates SS degradation and I_{ON}/I_{OFF} reduction with temperature.
Agarwal et al. (2018)	Engineering NDR in NCFETs for Analog Applications.	Explores NDR tuning to improve analog gain.
Singh et al. (2019)	PZT Gate Stack NC TFETs for RF Applications.	Shows improved g_m/I_d and f_T in ED FE SBTFETs.
Malvika et al. (2024)	HDDP-DG NCFET for Terahertz Applications.	Demonstrates f_T = 2.65 THz with superior linearity.
Upadhyay et al. (2022)	Review on NC Tunnel FETs.	Reviews NC-TFET architectures and low power prospects.
Singh et al. (2014)	Charge-Plasma NC JLTFET.	Proposes NC-JLTFET achieving 11.5 mV/decade SS.
Apoorva at al. (2020)	NC-Based Core Shell Doping Less Nanotube TFET.	Demonstrates SS = 18 mV/decade in NC-DL-NT TFET.
Hsu et al. (2021)	Hysteresis Free NC in MFIM Capacitors.	Attributes hysteresis free NC to leakage/trap assisted effects.
Lin et al. (2016)	Effects of Ferroelectric Variability on NCFETs.	Proposes conservative design rules ensuring hysteresis free NC.

2.4 Nanowire, Nanotube and Junctionless FETs

As CMOS technology approached the sub-10 nm regime, junction-based transistors faced increasing challenges in terms of dopant variability, fabrication complexity and leakage currents. To overcome these limitations researchers introduced junction less (JL) architectures, where the channel is uniformly doped and conduction is controlled entirely by the gate. This concept proved particularly effective in nanotube and nanowire structures, which provide excellent gate electrostatic control.

Nanotube junction less FETs (NJLFETs) have hollow nanowire core, thereby reducing parasitic capacitance and improving surface to volume ratio. NJLFETs significantly enhance AC and analog performance with higher cutoff frequency, reduced harmonic distortions and lower noise figure [84]. Further a dual metal junctionless nanotube FETs (DMJN-TFETs) combined gate material engineering with nanotube geometry to reduce the leakage while boosting gain and transconductance is proposed [117].

Junctionless Nanowire FETs (JL-NWFETs) were among the first devices modelled and fabricated to demonstrate these benefits. Charge based analytical models demonstrated hoe eliminating source drain junctions reduces random dopant fluctuations, enhances subthreshold swing control and lowers variability [118], [119]. Compared to inversion

mode nanowire MOSFETs JL-NWFETs exhibit higher I_{ON}/I_{OFF} ratios and reduced DIBL, confirming their scalability advantages.

Beyond static metrics, NJL and JL devices were also studied for high frequency and RF applications. Gain bandwidth trade off and noise immunity were explored with NJLFETs demonstrating strong potential for low noise amplifiers (LNAs). Gate all around tunnel FETs (GAA-TFETs) were studied in the RF domain, and were seen achieving f_T ~ 22 GHz and f_{max} ~ 250 GHz, providing the suitability of nanoscale JL/GAA devices for next generation RF electronics.

Structural technology boosters further enhanced JL-FET performance. Multi-gate structures, dielectric pocket designs and heterostructures were reviewed and studied for their properties that improve SCE suppression [120]. Recessed gate cylindrical JL-NW FE FETs was modelled which demonstrated better linearity and reduced leakage compared to conventional JL-FETs [121]. Junctionless Accumulation Mode FE FETs (JAM-FE FETs) were introduced which will improve the g_m/I_d and higher cutoff frequencies as the JL operation is combined with negative capacitance to achieve steep slopes.

At the material levels, NJL and JL devices have been demonstrated using Si, GaN and SiC. Studies confirmed that wide bandgap semiconductors in JL geometries achieve lower leakage and higher breakdown voltages, making them attractive for power and RF applications [118].

In summary, JL, nanotube and nanowire FETs offers a fabrication-friendly, variability resilient and high-performance alternative to conventional MOSFETs. Their ability to integrate with ferroelectric NC effects, leverage gate material engineering and deliver high frequency operation positions them as key candidates for ultra scaled CMOS and mixed signal electronics.

TABLE 2.4 NANOWIRE, NANOTUBE AND JUNCTIONLESS FETS

First Author (Year)	Paper Title	Summary
Shafizade et al. (2021)	Charge Based Modelling of Ultra Narrow JL Nanowire FETs.	Quantum corrected charge model showing improved electrostatics in JL0NW FETs.
Raut & Nanda (2022)	Charged Based Analytical Model for JL-GAA FETs.	Models trap effects and mobility degradation in JL FETs.
Rewari et al. (2016)	NJLFET with Improved Analog and AC Noise Immunity.	Demonstrates NJLFETs with higher cutoff frequency, better linearity and lower noise.
Goel et al. (2020)	Dual Metal Junctionless Nanotube FETs.	Combines dual metal gates with nanotube geometry for leakage suppression and RF gain.
Kalaivani & Usharani (2013)	Design of GAA Tunnel FET for RF Performance.	Proposes GAA TFET achieving f_T ~ 22 GHz and f_{max} ~ 250 GHz.
Narula et al. (2024)	Review on Technology Boosters for JL-FETs.	Surveys multi gate, heterostructures, and dielectric pocket methods for SCE suppression.

Singh et al. (2025)	Recessed Gate Cylindrical JL-NW FE FETs.	Recessed design enhances linearity and reduces leakage in JL-NWFETs.
Yadav et al. (2022)	JAM-FE FET for High Frequency Applications.	JL Accumulation Mode FE FETs improves gm, gain and cutoff frequency.
Yadav et al. (2023)	Temperature Effects on JAM-FE FETs.	Shows SS degradation and I_{ON}/I_{OFF} drop with temperature scaling.

2.5 Macaroni MOSFETs and 3D NAND Memory Devices

The macaroni MOSFET (hollow thin shell cylindrical channel surrounding an inner filler) emerged from vertical NAND flash memory development as an elegant compromise between manufacturability and excellent electrostatics in ultra high aspect ratio stacks. Semi analytical foundations [81] solved Poisson's equation exactly in cylindrical coordinates and coupled it with Pao-Sah transport to capture both subthreshold and ON state operation including Fowler Nordheim tunnelling relevant for programming showing how shell thickness, oxide thickness and filler radius co determine the threshold, subthreshold slope and write efficiency. Follow on theory established characteristic length formulas [80] and compact threshold/SS models [82], explaining why a thinner silicon shell gives shorter electrostatic length and stronger SCE immunity than full solid nanowires.

Cell-to-cell interference and array-level electrostatics are central in vertical NAND strings. An analytical inner vs surface potential relation was derived [122], clarifying the volume inversion at low gate bias and potential decoupling above threshold. Later a triple cell strings in subthreshold to predict neighbor induced shifts and read disturb the trends was modelled [123]. Doping profiles strongly affect layer-to-layer uniformity and the gaussian channel doping mitigates threshold skew across tall stacks compared with uniform doping [124]. To bridge the device physics with circuit analysis a BSIM-CMG methodology for macaroni cells and full strings was designed [83], enabling SPICE accurate prediction of string current, threshold roll off and transconductance variation.

On the integration side, BiCS technology [125] demonstrated a punch and plug flow using undoped plot Si channels and SiN based dielectrics, where macaroni bodies reduced grain boundary variability, delivered $I_{ON}/I_{OFF} > 10^6$ and sub 100 mV/decade SS, and scaled the array to ultra high bit densities. Recent compact variability studies [126] quantified random dopant fluctuation (RDF) and confirmed macaroni shells exhibit lower threshold variance than solid nanowires at comparable radii due to stronger gate control, grain aware transport modelling for poly Si channels [127] further showed subthreshold model convergence but ON state sensitivity to grain boundary electrostatics key for read reliability.

Macaroni concepts also migrated beyond memory into logic/analog and sensing. High-κ/metal gate and dual material gate (DMG) stacks on cylindrical shells improved threshold control, RF figures of merit and early voltage [128], [129]. A comparative threshold model [130] reported junctionless vs junction-based macaroni devices with high-κ DMG, finding JL variants offer lower roll off and better SCE immunity at small filler radii. For biosensing DMG macaroni with dielectric modulation [131] uses a

nanogap under the gate to transduce biomolecule permittivity into threshold shifts with improved sensitivity over full channel cylinders.

Across these works, consisted themes emerge: shell thickness and oxide thickness dominate electrostatic length and thus SCE, array aware modelling is essential for vertical NAND uniformity, compact BSIM compatible extractions are now mature enough for circuit co-design and DMG/high-κ technology boosters port macaroni advantages to analog/RF and sensing while maintaining low leakage and strong gate control.

TABLE 2.5 MACARONI MOSFETS AND 3D NAND MEMORY DEVICES

First Author (Year)	Paper Title	Summary
Paolucci et al. (2016)	A Semi Analytical Model for Macaroni MOSFETs With Application to Vertical Flash Memories.	Exact Poisson and Pao-Sah model linking shell/oxide/filler to threshold voltage, FN programming and SS.
Nguyen Gia et al. (2019)	Characteristics Length of Macaroni Channel MOSFET.	Derives 2D electrostatic length, thin shells which gives shorter wavelength and stronger SCE immunity.
Nguyen Gia et al. (2020)	Models of Threshold Voltage and Subthreshold Slope for Macaroni Channel MOSFET.	Compact threshold/SS formulas vs gate length, shell, bias and oxide.
Kim & Kim (2018)	Electric Potential of Vertical Flash Memory with a Macaroni Structure.	Analytical inner/surface potential coupling, volume inversion in subthreshold.
Nguyen Gia & Shin (2021)	Potential Model of Triple Macaroni Channel MOSFETs in Subthreshold.	Predicts neighbour cell interference and read disturb in strings.
Kumar et al. (2017)	Analytical Modelling of 3D NAND Call with Gaussian Doping Profile.	Shows Gaussian channel doping improves layers-to-layer threshold uniformly.
Kim et al. (2019)	BSIM-CMG Modelling for 3D NAND Cell with Macaroni Channel.	Three step parameter extraction enabling SPICE level string simulation.
Fukuzumi et al. (2007)	Optimal Integration BiCS Flash Memory.	BiCS integration with macaroni bodies high I_{ON}/I_{OFF} and scalable $4F^2$ arrays.
Aochi (2009)	BiCS Flash as a Future 3D Non-Volatile Memory.	Reviews BiCS process and macaroni FET benefits for ultra dense storage.
Spinelli et al. (2020)	Variability Effects in Nanowire and Macaroni MOSFETs- Part 1: RDF.	3D MC shows lower threshold variance in macaroni vs solid nanowires.
Mannara et al. (2020)	Comparison of Modelling for Poly-Si NW & Macaroni GAA MOSFETs.0	Grain aware transport indicates ON state sensitivity to GB electrostatics.
Banerjee & Das (2024)	GWFE Graded Channel Macaroni MOSFET with GIDL Analysis.	DMG and graded channel improves SCE, reliability and GIDL robustness (100-500 K).
Banerjee & Das (2024)	Threshold Voltage Modelling JL vs JB High-κ DMG Cylindrical Macaroni.	JL macaroni shows smaller roll off and better scaling than JB counterparts.

Banerjee & Das (2022)	DMG Macaroni MOSFET Biosensor via Dielectric Modulation.	Nanogap based DMG macaroni achieves higher sensing sensitivity.

2.6 Advanced Materials and Novel Device Concepts

As CMOS approaches its physical and economical scaling limits, new materials and novel device concepts have been introduced to maintain performance, reliability and energy efficiency. This section reviews research on SiC, GaN, drain extended MOS (DeNMOS), vacuum dielectrics and source/drain engineered extensions, as well as physics based exploratory devices that extend beyond conventional silicon.

2.6.1 Wide-Bandgap Semiconductors (SiC, GaN): Galliun Nitride (GaN) and Silicon Carbide (SiC) have been proposed for RF applications, high voltage and high temperature applications due to their wide bandgaps, high thermal conductivity, large critical electric fields. In a study of lightly doped cylindrical SiC nanowire FETs, these device structure report reduced leakage and higher breakdown voltage when compared to silicon counterparts [132], making them suitable for harsh environments. Similarly, when GaN FETs are compared with silicon MOSFETs, they demonstrate superior high frequency figure of merit and lower output capacitances for power switching.

2.6.2 Vacuum Gate Dielectric MOSFETs: Another unconventional approach is the vacuum gate dielectric FET (VacuFET), which replace solid dielectric with vacuum to eliminate interface traps. A GAA MOSFET with vacuum gates design was proposed [133], [134], showing reduced hot carrier injection, lower electron temperature and improved RF reliability. Although ON current suffers due to lower capacitance, gate engineering strategies such as dual material gate (DMG) and graded channel doping partially restore drive strength, making VacuFET promising for radiation hardened and RF systems.

2.6.3 Drain-Extended MOS (DeNMOS): To handle high drain voltages in scaled nodes, drain extended MOS devices with high-κ dielectrics have been developed. A high-κ DeNMOS design, demonstrating improved suppression of off-state band-to-band tunnelling (BTBT), better reliability and enhanced switching compared to traditional DeNMOS was presented [135]. These devices provide robust ESD protection and high voltage tolerance while maintaining CMOS compatibility.

2.6.4 Engineered Source/Drain Extensions: For nanoscale double SOI MOSFETs introduced engineered shallow source/drain extensions, combining doping engineering and dielectric modulation [136]. Analytical modelling confirmed that extension optimization reduces SCEs, enhances circuit reliability and improves g_m/I_d efficiency in sub-20 nm technologies.

2.6.5 Physics Based Exploratory Devices: Exploratory devices have also pushed the boundaries of transistor physics. For instance, damage immune FETs with vacuum directrices [137], demonstrates radiation hardness and resilience to hot carrier stress. Similarly, fully coupled physics-based simulations of nanoscale dielectrics provided new insights into tunnelling and interface trap behaviour [138], [139]. These studies are essential to understand reliability bottlenecks in future device scaling.

TABLE 2.6 ADVANCED MATERIALS AND NOVEL DEVICE CONCEPTS

First Author (Year)	Paper Title	Summary
Vasanth et al. (2019)	Study on Lightly Doped Cylindrical Surrounding Gate 6H-SiC Nanowire FET.	Shows SiC-NWFETs achieve higher breakdown and lower leakage than Si devices.
Mishra et al. (2020)	Performance Comparison of GaN FET and Si MOSFET.	Demonstrates GaN FETs offer superior high-frequency FoMs and power efficiency.
Gautam et al. (2013)	GAA MOSFET with Vacuum Gate Dielectric for RF Reliability.	Proposes VacuFETs with reduced hot carrier injection and better RF reliability.
Singh et al. (2017)	VacuFET with DMG and Graded Channels.	Enhance ON current of VacuFETs using gate engineering strategies.
Sharma et al. (2018)	Drain Extended MOS with High-κ Dielectrics.	Improves off state BTBT suppression and switching performance in DeNMOS.
Yadav et al. (2019)	Engineering Source-Drain Extension in Nanoscale Double SOI MOSFETs.	Models optimized shallow extensions to reduce SCEs and improve analog/RF metrics.
Vishnoi et al. (2017)	Damage-Immune FET with Vacuum Gate Dielectrics.	Demonstrates radiation hard, hot carrier resilient vacuum-gate FETs.
Park et al. (2018)	Physics Based Numerical Model of Nanoscale Dielectrics.	Simulates dielectric tunnelling and trap behaviour for reliability prediction.

2.7 Variability, Reliability and Temperature Studies

Variability and reliability define boundary between device concepts and manufacturable technologies. In ultra scaled GAA nanosheets/nanowires and macaroni structures, variability stems from random dopant fluctuations (RDF) in inversion mode channels, grain boundary (GB) statistics in poly-Si vertical NAND channels, trapped charges at interfaces and thermal stability of leakage, mobility and ferroelectric polarization. Reliability further intertwines with hot carrier degradation, radiation/ESD exposure and BTBT driven GIDL, temperature in turn amplifies or reshapes these mechanisms.

A comprehensive Monte-Carlo study quantified RDF in solid nanowires versus macaroni structure [127], [134], showing that for comparable outer radii, macaroni MOSFETs exhibit lower threshold spreads because the thin silicon enforces stronger gate control and volume inversion that averages dopant placement. In poly-Si channels [128], comparison of effective medium vs grain aware transport was studied and it was observed that while subthreshold predictions largely agree, ON state current is highly sensitive to GB electrostatics, explaining read current dispersion in tall vertical NAND stack. Complementing this a separate study of impact of GB width and trap density in GAA poly-Si transistors was done [76], [140].

Temperature also governs NC/ferroelectric behaviour. Early experiments already showed SS rising from ~ 15 to ~ 24 mV/decade between 300- 400 K in polymer capacitor-based NC FETs as internal gain collapses [95]. A faster SS and I_{ON}

degradation in HZO-NC pFETs was observed than in MOSFET controls [141], due to pyroelectric polarization loss, yet NCFETs maintained an advantage over the whole -50 °C to 85 °C range. A fully coupled TCAD LK framework [96], [130] revealed that NC strengthens at cryogenic (100 K) but vanishes > 500 K, and that high-κ interlayers are essential to keep sub-kT/dec SS at room temperature. Extending to specific architectures JAM-FE FETs showed degrade with temperature but still out performs JL-FE FETs [142]. In Fe-FinFETs RF/analog FoMs degrade with temperature while linearity improves, an important circuit level trade off [143]. The spacer assisted NC stacks moderate I_{OFF} and stabilize threshold up to 500 K.

Analytical models help design for thermal robustness and leakages. A temperature aware GIDL model for dual meatal nanowires was derived [144], capturing field redistribution and tunnelling effects statistics. GIDL with trap charges and temperature was analyzed in graded channel [109], [138] and DMG macaroni MOSFETs oxide and gate work function combinations that retain low leakage up to 500 K. Reliability centric device concepts further reduce stress sensitivities vacuum gate GAA MOSFETs eliminate interface traps cutting hot carrier injection and radiation induced drift [145], [146]. In power interfaces, high-κ DeNMOS [147], suppresses off-state BTBT and improves switching energy translating to lower self-heating and better high temperature stability [148].

TABLE 2.7 VARIABILITY, RELIABILITY AND TEMPERATURE STUDIES

First Author (Year)	Paper Title	Summary
Spinelli et al. (2020)	Variability Effects in Nanowire and Macaroni MOSFETs Part I: RDF.	3D MC: macaroni shell shows lower threshold variance that solid NWs due to stronger gate control.
Mannara et al. (2020)	Modelling Transport in Poly-Si NW and Macaroni GAA MOSFETs.	Grain aware modelling: ON-state current sensitive to Grain Boundary electrostatics; subthreshold models converge.
Lin et al. (2021)	Instability vs Grain Boundary Width and Trap Density in GAA Poly-Si Transistors.	Weak inversion set by the product of grain boundary width and trap density whereas strong inversion current is limited by trap density
Alnuaimi et al. (2013)	Field/Temperature Dependence of GIDL Activation Energy.	Maps PF/TAT/BTBT regimes; Ea. transitions with field and temperature.
Tiwari et al. (2014)	GIDL Mechanism in SiGe pFET.	SiGe bandgap reduction enhances BTBT driven GIDL, temperature and bias aggravate leakage.
DeSouza et al. (2023)	GIDL in SOI Stacked Nanowire/Nanosheet nMOSFETs at High Temparature.	Wider nanosheets show stronger temperature induced GIDL, nanowires fare better.
DeSouza et al. (2023)	High Temperature & Width Influence on GIDL.	Confirms width as a primary thermal reliability knob in stacked multi gate devices.
Jo & Shin (2015)	Impact of Temperature on NCFET.	SS degrades (15→24 mV/decade from 300→400 K) as internal gain falls.

Wang et al. (2020)	$Hf_{0.5}Zr_{0.5}O_2$ Based NCFETs vs Temperature.	Faster SS/ION degradation than MOSFET control yet net advantage across -50 – 85 °C.
Raol et al. (2021)	Fully coupled Simulation of Temperature Effect on NC Devices.	NC strengthens at cryogenic temperature, vanishes >500 K, high-κ needed for room temperature sub kT/ decade SS.
Yadav et al. (2022)	Impact of Temperature on JAM-FE FET.	JAM-FE FET degrades with temperature nut remains superior to JL-FE FET.
Saha et al. (2020)	Temperature Dependence of RF/Analog & Linearity in Fe-FinFET.	RF FoMs degrades with temperature while linearity improves, circuit design trade off.
Parthak et al. (2023)	TCAD Study: Temperature Impact on Spacer Assisted NC FET.	Spacer-assisted MFMIMOS reduces I_{OFF} and stabilizes threshold up to 500 K.
Goel et al. (2019)	Temperatures dependent GIDL Model for Dual Metal Nanowire FETs.	Analytical GIDL with thermal field statistics and is validated by TCAD simulations.
Banerjee & Das (2022/2024)	Macaroni DMG/Graded Channel: Temperature & Trapped Charge GIDL.	Shows shell/oxide/DMG choices that sustain low GIDL across 100-500 K.
Han et al. (2011)	Damage-Immune FET with Vacuum Gate Dielectric.	Eliminates interface traps, radiation/hot carriers hardening with some drive loss.
Gautam et al. (2013)	GAA VacuFET for Reliability & RF.	DMG/graded channels reclaim I_{ON} while preserving hot-carriers robustness.
Pali et al. (2022)	High-κ DeNMOS for BTBT Control.	High-κ dielectric and floating plates suppress off-state BTBT and improve switching energy.

2.8 Conclusion

The extensive literature survey conducted in this chapter covers a broad spectrum of device architectures, material innovations, modelling techniques and application specific enhancements. Together, these works portrayed a clear picture of the current state-of-the art in nanoscale FET research and provide valuable insights into the challenges of further device scaling.

In the domain of analytical and compact modelling, researchers have successfully developed frameworks for predicting threshold voltage, I-V characteristics, subthreshold slope and short channel effects (SCEs) in cylindrical junction less and macaroni MOSFETs. These models not only deepen the understanding of electrostatics but also established circuit compatible compact models, bridging physics with design. However, while analytical models offer clarity and computational efficiency, they often simplify complex phenomenon such as variability, ferroelectric dynamics and trap assisted tunnelling leaving scope for refinement.

Band-to-band tunnelling (BTBT) and Gate Induced Drain Leakage (GIDL) emerged as two of the most persistent leakage mechanisms in scaled MOSFETs. Multiple works proposed hetero-dielectric engineering, shallow extensions and dual-metals to mitigate

GIDL, while material innovations such as SiGe channels and high-κ dielectrics showed partial improvements. Yet, a consistent theme across these studies is that leakage suppression strategies often come at the expense of ON state performance or analog gain, indicating the need for balanced architecture.

The field of negative capacitance and ferroelectric FETs (NC FETs) represents one of the most promising directions for low-power electronics. Experimental demonstrations of NC in HZO based stacks, as well as analytical and compact models, have shown sub-60 mV/decade slopes, enhanced analog performance and negative DIBL. However, the issues of hysteresis, capacitance matching and thermal instability persist, particularly under realistic operating conditions. The literature also highlights trade-offs between achieving steep slopes and maintaining RF/analog reliability, suggesting that NC integration must be carefully optimized.

Nanotubes, nanowires and junction less FETs have been explored as scalable alternatives to conventional inversion mode MOSFETs. Their uniform doping and strong gate control simplify fabrication and reduced variability, while hollow nanotube structures further enhance analog and RF figure of merit. Despite these advantages, short channel effects such as DIBL remain significant, particularly at reduced channel lengths. The research consensus is that geometry engineering and gate material modulation are effective but incomplete solutions.

In the context of macaroni MOSFETs and 3D NAND flash memory, literature emphasizes the importance of shell thickness, compact BSIM-CMG models and doping profiles for device and circuit level optimizations. Macaroni structures improve electrostatics and suppress variability, making them attractive for dense vertical integration. However, cell-to-cell interference, grain-boundary effect and RDF in poly-Si channels remain unresolved bottlenecks for NAND scaling.

Advanced materials and unconventional concepts such as GaN, SiC, high-κ drain extended MOS, vacuum gate dielectrics have broadened the design landscape. These devices demonstrate superior high-voltage tolerance, reliability and radiation hardness but still face integration challenges with main stream CMOS.

Finally, temperature studies and variability consistently revel that advanced architectures such as macaroni and nanowires offer improved electrostatic control, but reliability strongly depends on grain-boundary control, thermal effects and trap densities. NC devices, in particular, are highly sensitive to temperature with polarization weakening at elevated conditions and disappearing above 500 K. these findings underscore that thermal stability is as important as electrostatics in practical development.

2.9 Synthesis of Literature Insights

From the cumulative body of research, several overarching themes emerge:

2.9.1 Electrostatic vs. Leakage Trade-off: Most device innovations improve gate control and reduce SCEs but often worsen BTBT or GIDL, indicating that leakage suppression without performance degradation remains unresolved.

2.9.2 Ferroelectric/NC Promise and Challenge: NC integration offers steep slopes and analog gains, yet hysteresis, temperature sensitivity and stability hinder the practical implementation.

2.9.3 Geometry and Material Engineering Synergy: Nanowires, nanotubes and macaroni structures provide superior control, but complementary approaches are required like dual material gates, shallow extensions and high-κ dielectrics to fully realize the benefits.

2.9.4 Temperature and Reliability: Many research papers examine the SCEs and leakages under nominal conditions, but only few provide comprehensive insights into temperature dependent behaviour, reliability and variability over device lifetime.

2.9.5 Application Extensions: While RF applications show potential, systematic design frameworks to balance low leakage, robust reliability and high sensitivity are still missing.

2.10 Research Gaps

Based on the above-mentioned literature review, the following research gaps were identified:

1. As per the literature review, the Band-to-Band Tunnelling (BTBT) problem is a critical issue that must be addressed to enhance device performance.
2. To increase reliability, it is important to thoroughly examine Gate-Induced Drain leakage (GIDL) in nanowire FETs.
3. The effect of Drain-Induced Barrier Lowering (DIBL) on FET devices is not thoroughly investigated.
4. The impact of temperature on the SCEs for correct and better functioning of FET has not been examined critically.

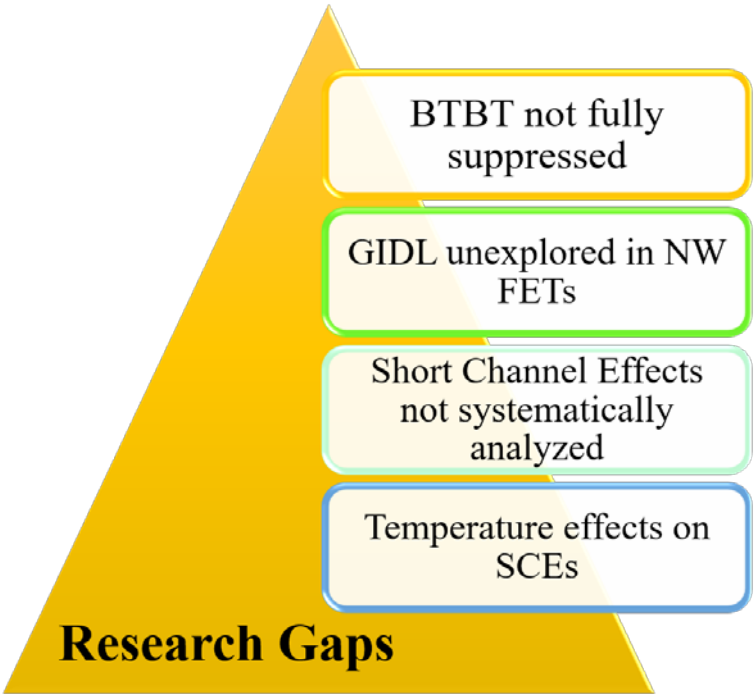


Figure 2.1 Pictorial Representation of Research Gaps.

2.11 Research Objectives

From the foregoing discussion the following objectives have been achieved in our thesis:

Research Objective 1:

- To propose a novel Nanowire Field Effect Transistor with reduced gate leakages.

Research Objective 2:

- To study the impact of temperature on gate leakages and to propose structures to minimize the effect on the Nanowire Field Effect Transistor.

Research Objective 3:

- To design a novel Nanowire Field Effect Transistor to reduce Short Channel Effects.

Research Objective 4:

- To design a novel Nanowire Field Effect Transistor for analog applications.

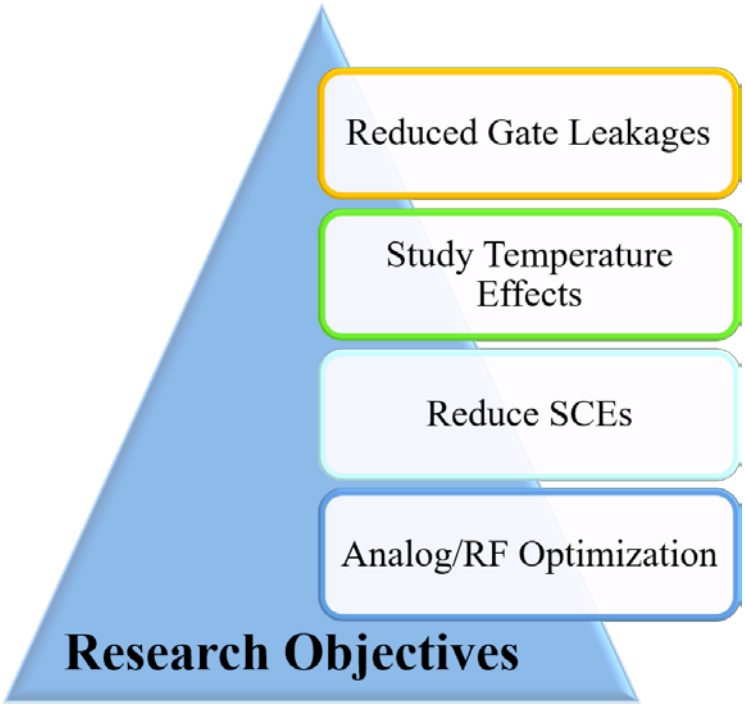


Figure 2.2 Pictorial Representation of Research Objectives.

Chapter 3

ANALYTICAL MODELING OF CHANNEL ENGINEERED MACARONI INDUCED GATE-ALL-AROUND FIELD EFFECT TRANSISTOR (CE-MI-GAA FET)

The semiconductor industry has been undergoing rapid transformation, driven by the continuous demand for lower power consumption, enhanced performance, and higher integration density in modern electronic systems. According to Moore's law, the number of transistors on a chip doubles approximately every two years. However, significant challenges are faced by the traditional transistor architectures well as the device dimensions scale below the sub-10 nm regime [8], [149]. The performance of the transistor is affected by the increasing static power dissipation, short channel effects (SCEs), and gate-induced drain leakage (GIDL) [150], [151].

In conventional planar MOSFETs, as the channel lengths of the devices decrease to the nanoscale, electrostatic control weakens drastically, leading to excessive leakage and scalability loss. This issue is addressed by shifting the architecture of the devices towards multi-gate structures such as FinFETs, Double Gate FETs, and Gate All Around (GAA) FETs [80], [131]. Among these GAA FET structures, the ones considered the most promising are those in which the channel is surrounded by the gate, thereby offering superior electrostatic control and reduced SCEs compared to planar FinFET designs.

Despite these advantages, leakage currents remain a critical issue, particularly OFF-state leakage due to GIDL. GIDL originates from band-to-band tunnelling (BTBT) between the conduction band of the drain and the valence band of the channel under high drain bias and low gate bias conditions [87], [152]. This leakage not only leads to power dissipation but also compromises the functionality of the devices, such as Dynamic Random Access Memory (DRAM), where low standby current is crucial [153]. While scaling the nanowire devices, GIDL is more prominent because of the overlapping of conduction and valence bands, exacerbating the tunnelling phenomena [154], [155].

The macaroni channel nanowire device represents an advanced Gate-All-Around (GAA) transistor configuration in which the conventional solid nanowire core is replaced by a hollow filler. This unique macaroni structure provides a continuous gate enclosure around the active region, ensuring superior electrostatic control and an enhanced gate to channel coupling efficiency. This reduction in active silicon volume effectively suppresses short channel effects. Moreover, the hollow-core design eliminates defect prone central regions, thereby reducing trap-assisted tunnelling and interface related instability [81], [156]. To overcome all these issues, various advanced designs of transistors were explored. A few such designs of transistors are: Double Metal Gate Macaroni Nanowire FETs (DMGM-NW FETs), is a novel device

architecture that combines dual work function gate electrodes with a partially hollow (macaroni like) silicon channel to achieve improved electrostatic control and reduced leakage [131]. In this structure, a thin silicon channel surrounds a low-κ or air-filled hollow core, effectively minimizing parasitic capacitance and enhancing the gate-to-channel coupling. The use of two metals with distinct work functions typically one near the source and another near the drain allows localized tuning of the surface potential, thereby reducing DIBL and improving subthreshold slope. The filler material within the hollow region acts as a thermal and dielectric barrier, limiting leakage pathways while maintaining sufficient mechanical stability. The figure 3.1 pictographically represent the DMGM-NW FET structure.

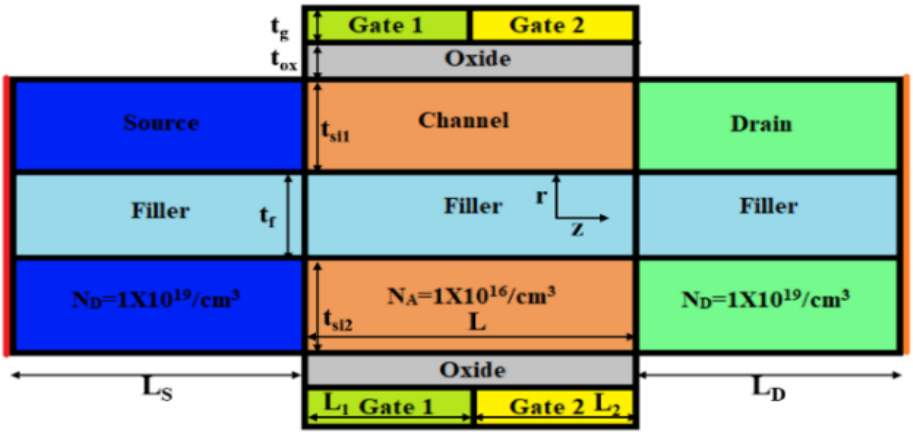


Figure 3.1 Pictorial Representation of DMGM-NFET [157].

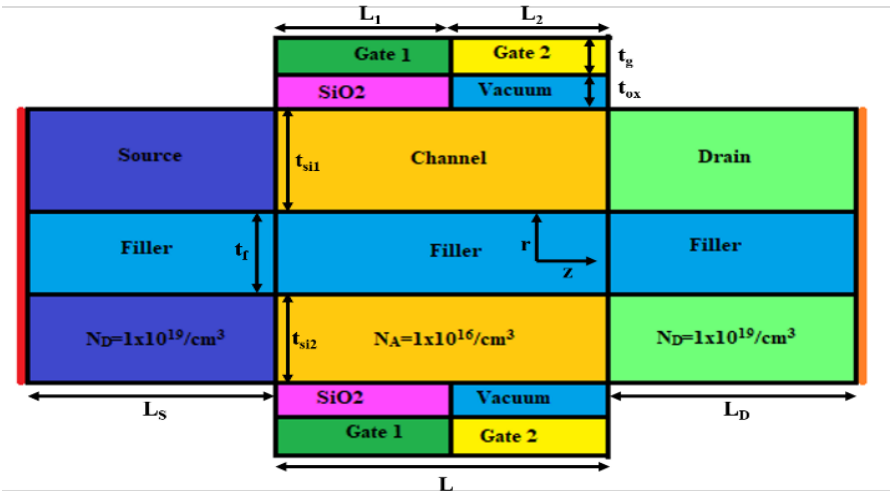


Figure 3.2 Pictorial Representation of HD-MC NWFET [158].

Hetero-Dielectric Macaroni Channel NWFETs (HD-MC NWFET) is an advanced gate-all-around (GAA) architecture that employs dielectric engineering to enhance analog and RF performance metrics while suppressing the leakage current. The device features a macaroni style channel, where a thin semiconductor shell surrounds a hollow dielectric filled core. In this the key distinction lies in the use of heterogeneous dielectric materials like combining high-κ and low-κ dielectrics to achieve graded

electric field along the channel. The dielectric heterogeneity enhances various parameters and by optimizing the permittivity profile the electric field at the drain end can be reduced effectively. The proposed structure is an ideal device for next generation analog and mixed circuits [150], [158]. Figure 3.2 pictographically represents the HD-MC NWFET.

The effect of dielectric modification, channel modification, and gate engineering can be observed from the architectures of these devices. Yet achieving a balance between low OFF-state leakage, analog performance, and ON-state current remains a challenge.

The Macaroni Induced Gate All Around FETs (MI-GAA FETs) structure has attracted attention due to its unique geometry. This device structure employs a hollow cylindrical channel at the center filled with a vacuum [159], [160]. This modification in the structure of the FET helps in improving the electrostatic control, offers stability, and reduces parasitic capacitance. However, even Macaroni-Channel devices still suffer from leakage issues when scaled aggressively, mainly because of tunnelling and hot carrier effects [161], [162].

To overcome all these limitations, this chapter contains the simulated results as well as the analytical model of Channel Engineered-Macaroni Induced Gate All Around FET (CE-MI-GAA FET). The novelty lies in using the vacuum filler at the core of the channel, which fundamentally alters the device physics by:

1. Mitigating hot-carrier effects by trapping energetic carriers at the interface of vacuum and semiconductor [151].
2. Suppressing GIDL by increasing the tunnelling distance and reducing the overlapping of conduction and valence bands.
3. Improving analog performance by enhancing quality factor, transconductance, and cut-off frequency [163], [164].

This chapter provides a comprehensive overview of the Channel Engineered-Macaroni Induced Gate All Around FET (CE-MI-GAA FET) structure, fabrication process, simulation framework, analytical modelling approach with validation results, concluding with a comparative performance analysis against traditional GAA FETs.

3.1 Channel Engineered-Macaroni Induced Gate All Around FET (CE-MI-GAA FET)

3.1.1 Working Principle and Operating Mechanism

The CE-MI-GAA FETs performance enhancements are rooted in three primary operating mechanisms:

3.1.1.1 Hot Carrier Trapping

The carriers in the nanodevice accelerate towards the drain at high V_{DS} in the process acquiring sufficient kinetic energy to initiate tunnelling or causing impact ionization. In the proposed device the filler silicon interface acts as a scattering and trapping site for these carriers, reducing hot carrier effect and dissipating energy [161].

3.1.1.2 Electrostatic Potential Modulation

The presence of vacuum filler at the center modifies the radial potential distribution, weaking drain to source field coupling. This maintains a higher effective barrier in OFF-state and hence suppresses leakage current and Drain Induced Barrier Lowering (DIBL) is also reduced [151].

3.1.1.3 Tunnelling Distance

GIDL is driven by lateral BTBT between valance and conduction bands in the high field drain region [152], [165]. The tunnelling probability is reduced by introducing filler and increasing the tunnelling path length by modifying band profile [131], [166].

Due to the presence of silicon shell and surrounding gate the proposed device ensures high transconductance and competitive ON current in ON state operations. The dual benefit of low OFF state leakage and high ON state current makes CE-MI-GAA FET structure a promising candidate for low power applications.

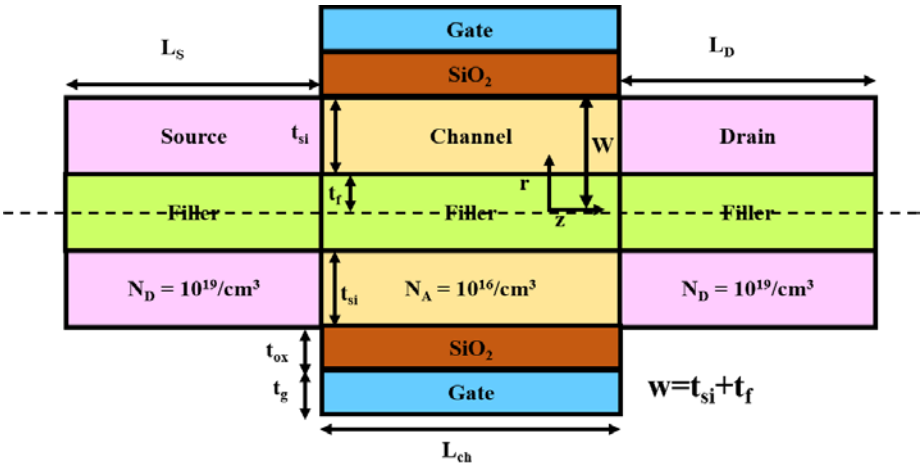
3.1.2 Device Architecture

Figure 3.3 of this manuscript contains the three-dimensional, two-dimensional, cut-view schematics of the proffered CE-MI-GAA FET. The proposed device is built on the foundation of a traditional gate all around FET (TGAA FET) design, which has superior electrostatic control due to the full encapsulation of the channel by the gate. The proffered device has a gate thickness t_g (=2 nm), filler thickness t_f (=5 nm), and oxide thickness t_{ox} (=2 nm) is designed using Molybdenum as the metal, having a work function of 4.72 eV. Table I contains a detailed description of the architectural parameters of the CE-MI-GAA FET and TGAA FET. The channel of the proffered CE-MI-GAA FET is modified by using diluted Hydrofluoric acid to create a hollow filler. The width (w) of the channel is constant where $W = t_{si}+t_{f,}$ and here $\theta = 0^{o}$.

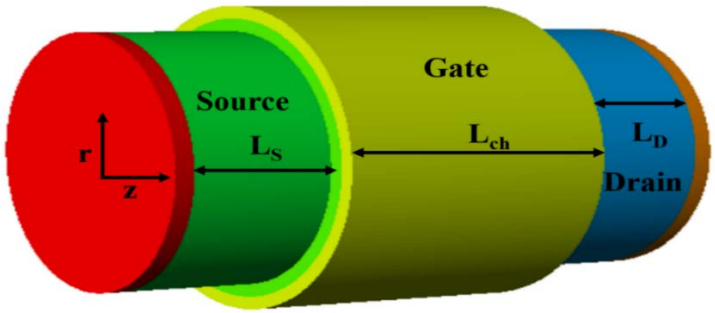
3.1.3 Simulation Setup

A device simulator for ATLAS 3D Silvaco is used to run numerical simulations [167]. Among the models considered are the Shockley-Read-Hall (SRH) model, the concentration-dependent mobility (CONMOB) model, the parallel electric field-dependent mobility (FLDMOB) model, the hot electron injection (HEI) model, the Concannon nonlocal gate current (N. CONCAN) model, the band gap narrowing (BBT.STD) model, and the drift diffusion model [168]. In Table 3.2, these models' descriptions are provided. The Newton-Gummel approach is used to solve the carrier transport issue numerically. To incorporate the effects of recombination, it is imperative to utilize the Shockley-Read-Hall (SRH) model. This model is instrumental in simulating leakage currents induced by thermal generation processes. Additionally, it is crucial to account for the presence of interface traps situated at the silicon/oxide junction. For precise simulation, the direct recombination model (AUGER) must also be activated. The parameters governing these models are modifiable within the MOBILITY statement. For the scenario of velocity saturation induced by the high electric field, the field-dependent mobility model (FLDMOB) should be employed. Alternatively, CONMOB can be utilized to relate the low-field mobility at 300 K to the impurity concentration. Furthermore, the HEI Models are employed to address the

tunneling of energetic carriers through insulators, which is significant for phenomena such as gate current and Flash EEPROM programming. The N. CONCAN model is a non-local gate model aligned with the Concannon substrate current model, specifically developed for Flash EEPROM technologies. Choosing the appropriate parameters will automatically activate the Energy Balance Transport Model. The BBT.STD model addresses band-to-band tunneling phenomena and computes the recombination-generation rate based on the local electric field, particularly under conditions of exceptionally high field strengths. The drift-diffusion model, an isothermal framework, necessitates the resolution of three distinct equations about the electron concentration, potential, and hole concentration., Charge transport models or current density equations are derived from approximations and simplifications of the Boltzmann Transport Equation, resulting in a range of models such as the drift-diffusion model, the Energy Balance Transport Model, and the hydrodynamic model. Among these, the Drift-Diffusion Model is distinguished by its simplicity and practicality, operating with a limited set of variables: ψ (electric potential), p (hole density), and n (electron density), thereby obviating the need for additional independent variables [167].



(a)



(b)

Figure 3.3 (a) Two-dimensional diagram of CE-MI-GAA FET, (b) Three-dimensional Diagram of CE-MI-GAA FET [150]

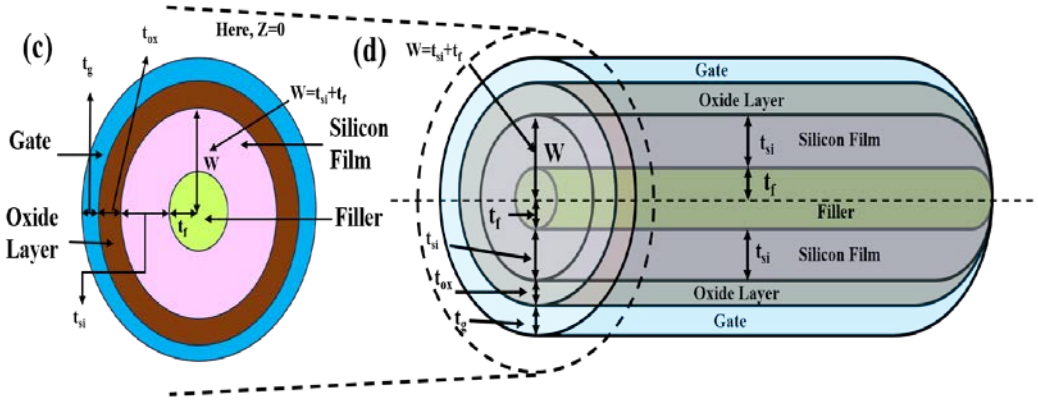


Figure 3.3 (c) One-Dimentional Cut-View Diagram of CE-MI-GAA FET and (d) Three-Dimentional Cut-View Diagram of CE-MI-GAA FET [150]

TABLE 3.1: ARCHITECTURAL SPECIFICATION

Parameters	TGAA FET	CE-MI-GAA FET
Channel Length (L_{ch})	30 nm	30 nm
Channel Doping	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$
Oxide Thickness (t_{ox})	2 nm	2 nm
Silicon Thickness (t_{si})	10 nm	10 nm
Length of S/D	15 nm	15 nm
Filler Thickness (t_f)	5 nm	5 nm
Φ_m	4.86 eV	4.72 eV
Gate Thickness (t_g)	2 nm	2 nm

In our proposed device, CE-MI-GAA FET, the simulation and structural design both address the hot carrier effects. The macaroni-induced vacuum filler serves a dual role by trapping hot carriers at the semiconductor vacuum interface, mitigating their detrimental impact, and by providing an electrostatic barrier that inhibits high-energy carrier injection into the drain. The following models are used to achieve the hot carrier effect:

1. HEI (high-Field Electron Injection) Model: This model is used to approximate the tunnelling of energetic carriers through the gate oxide, which is indirectly related to the hot carrier injection mechanism.
2. BBT.STD (Band-to-Band Tunnelling) Model: This model accounts for the tunnelling of electrons under high-energy conditions, relevant to hot carrier-induced effects.
3. FLDMOB (Field-Dependent Mobility) Model: This model is used to capture velocity saturation and reduced mobility under high electric fields, which is a typical condition for hot carrier generation.

For the proposed CE-MI-GAA FET device, the SRH (Shockley-Read-Hall) recombination model is used in the simulation, which specifically considers the presence of interface traps and their role in the recombination-generation mechanism at the oxide semiconductor interface. This analysis is critical for Gate-Induced Drain

Leakage (GIDL), subthreshold leakage current, and reliability degradation due to trap-assisted tunnelling.

TABLE 3.2: MODELS UTILIZED FOR SIMULATION

Models	Details
SRH	Employed to integrate the impact of carrier recombination phenomena.
Drift Diffusion	Contains Boltzmann statistics.
CONMOB	Employed to address the influence of mobility concentration within MOSFETs.
BBT.STD	Utilized to quantify the influence of tunnelling phenomena on charge carriers.
FLDMOB	Employed to incorporate the effects of velocity saturation into the analysis.
N. CONCAN	Utilized to scrutinize the substrate current.
HEI	Employed to account for the tunnelling carriers that contribute to the gate current.

Figure 3.4 comprises the assessment of empirical data obtained from previous fabrications of the proposed design. From this, it can be inferred that the outputs of fabricated work and proposed work are very close. The simulation of the device is done using Silvaco ATLAS 3D software. [167] As the channel length is greater than 20 nm and the radius is in the 5 nm range, the quantum and ballistic transport effects are not included. [169][170].

3.1.4 Fabrication

The fabrication process of the proffered CE-MI-GAA FET is discussed in detail in Figure 3.5. [171][80][172] A silicon substrate layer is used, which has a dielectric layer embedded within it and is then covered by an additional silicon layer. The uppermost silicon stratum undergoes an initial doping process wherein it is infused with a sparse concentration of either boron or phosphorus atoms. This arrangement of layers is commonly referred to as silicon-on-insulator (SOI) [173][174]. After this, the nanowire is designed on SOI using the VLS method [86]. Isotropic etching of the center of the nanowire using diluted Hydrofluoric (HF) Acid [172][173]. This sacrificial oxide layer is created using the low-temperature tetraethyl orthosilicate method [126][125]. Source and drain terminals are etched in the wafer using selective etching. A layer of photomask is grown on the wafer, which further helps in the ion implantation process of the source and drain sides. After this, the sacrificial oxide layer is removed with the help of diluted HF acid. Metal contacts for the source and drain are deposited. The gate electrode is deposited using lithography and E-beam evaporation.

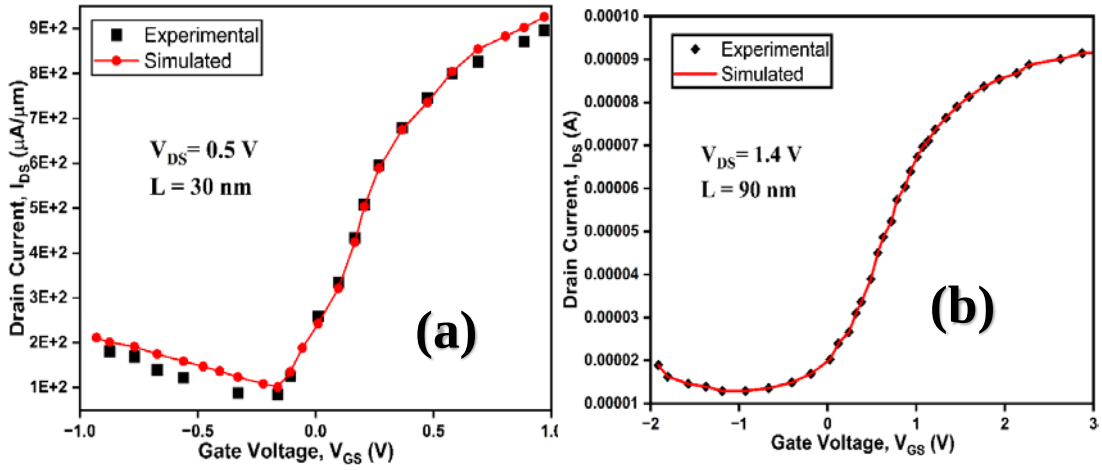


Figure 3.4 Calibrated work with Experimental work evaluation of (a) Transfer Characteristics of Nanowire FET [4], and (b) Transfer Characteristics of the Macaroni Channel FET [125][126].

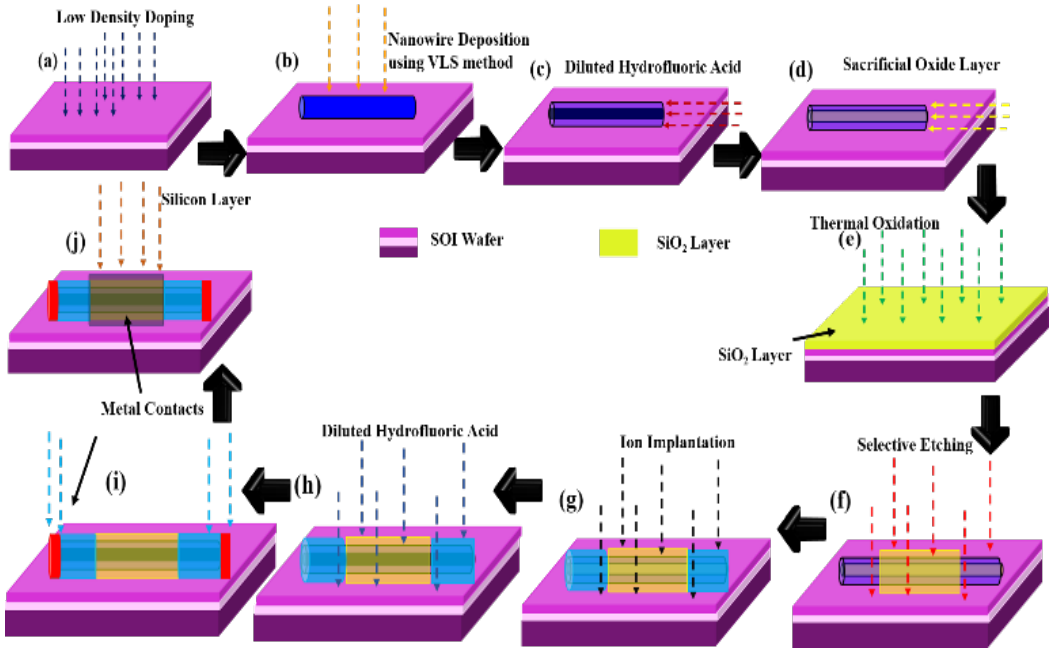


Figure 3.5 Process Stages for Manufacturing the CE-MI-GAA FET [150].

3.1.5 Analytical Modelling

The electrical features of the proffered CE-MI-GAA FET device can be investigated in detail with the two-dimensional Poisson equation. The potential $\Psi_T(r,\theta,z)$ does not exhibit any dependence on the radial plane, remaining invariant along the dimension. [175][176][177] Consequently, the corresponding two-dimensional Poisson equation that requires resolution is formulated as follows:

$$\frac{1}{r}\frac{\partial\Psi}{\partial r}+\frac{\partial^2\Psi}{\partial r^2}+\frac{\partial^2\Psi}{\partial z^2}=\frac{qN_A}{\varepsilon_{si}} \quad (3.1)$$

where N_A is the concentration of doping in the channel region, ε_{si} is constant for the representation of dielectric in silicon, q is the electron charge and Ψ is the distribution of potential in the silicon film.

Within the framework of the superposition method, the overall potential can be bifurcated into a one-dimensional long channel solution ($V(r)$) governed by the Poisson equation and a two-dimensional short channel solution ($U(r, z)$), governed by two-dimensional Laplace's equation [178] [86]as:

$$\Psi(r, z) = V(r) + U(r, z) \tag{3.2}$$

From equation (3.1):

$$\frac{1}{r}\frac{\partial V(r)}{\partial r} + \frac{\partial^2 V(r)}{\partial r^2} = \frac{qN_A}{\varepsilon_{si}} \tag{3.3}$$

and

$$\frac{1}{r}\frac{\partial U(r,z)}{\partial r} + \frac{\partial^2 U(r,z)}{\partial r^2} + \frac{\partial^2 U(r,z)}{\partial z^2} = 0 \tag{3.4}$$

Boundary conditions utilized for determining the two-dimensional potential solution denoted as $\Psi(r, z)$ are outlined as:

- The electric potential at the inner surface of the silicon film remains invariant.

$$\Psi(r=r_1, z) = \Psi_C(z) \tag{3.5}$$

- At the inner surface of the silicon film, the electric field magnitude is nullified, effectively becoming zero.

$$\left.\frac{\partial \Psi(r,z)}{\partial r}\right|_{r=r_1} = 0 \tag{3.6}$$

- The potential observed at the surface of the silicon film is expressed as:

$$\Psi(r,z)|_{r=r_2} = \Psi_I(r_2, z) \tag{3.7}$$

- The electric field present at the surface interface of the silicon film is characterized as:

$$\left.\frac{\partial \Psi(r,z)}{\partial r}\right|_{r=r_2} = \check{\exists}[V_{GS} - V_{FBI} - \Psi_I(r_2, z)] \tag{3.8}$$

where V_{FBI} is flat band voltage.

- Potential at the source terminal is:

$$\Psi(r,z)|_{z=0} = V_{BI} \tag{3.9}$$

- Potential at the drain terminal is:

$$\Psi(r,z)|_{z=L} = V_{BI} + V_{DS} \tag{3.10}$$

- Potential at different material interface is:

$$\Psi(r,0) = \Psi(r,L) \tag{3.11}$$

Here,

$$\check{\mathfrak{Z}} = \frac{C_{ox}}{\varepsilon_{si}},\ C_{ox} = \frac{\varepsilon_{ox}}{r_2\, ln\left(1+\frac{t_{ox}}{r_2}\right)}$$

From equation (3.3) $\Psi_C(r)$ can be assumed as a parabolic solution, hence

$$\Psi_C(r) = P_0 + P_1 r + P_2 r^2 \tag{3.12}$$

Substituting equation (3.12) in equation (3.3) and then applying boundary conditions,

$$P_0 = \Psi_I(r_2, \mathfrak{z}) - (a^2 - r_1^2)[V_{GS} - V_{FBI} - \Psi_I(r_2, \mathfrak{z})\,] \tag{3.13}$$

$$P_1 = -2r_1 P_2 \tag{3.14}$$

$$P_2 = \frac{\check{\mathfrak{Z}}}{a}[V_{GS} - V_{FBI} - \Psi_I(r_2, \mathfrak{z})\,] \tag{3.15}$$

The solution to the two-dimensional Laplace equation (3.4), derived by applying the specified boundary conditions, can be formulated as:

$$\Psi_I(r, \mathfrak{z}) = \sum_{n=1}^{\infty} J_0(\lambda_S)\left[Ae^{\lambda \mathfrak{z}} + Be^{-\lambda \mathfrak{z}}\right] \tag{3.16}$$

Here, $J_0$is the Bessel function, while A and B are the constants determined through the application of boundary conditions, equations (3.9) -(3.11), and additionally $\lambda_S$corresponds to eigenvalues.

Solving equation (3.1) using equations (3.12) -(3.16), we get:

$$\Psi(r, \mathfrak{z}) = V_{GS} - V_{FBI} - \frac{qN_A t_{si}}{4C_{ox}} + \frac{qN_A t_{si}^2}{16\varepsilon_{si}} + \frac{qN_A r^2}{4\varepsilon_{si}} + \sum_{n=1}^{\infty} J_0(\lambda_S)\left[Ae^{\lambda \mathfrak{z}} + Be^{-\lambda \mathfrak{z}}\right] \tag{3.17}$$

The variables from equation (3.17) are discussed in the Appendix. Therefore, by determining the surface potential $\Psi(r, \mathfrak{z})$, the corresponding distribution of the electric fields across various regions can be subsequently calculated as:

$$E(r, \mathfrak{z}) = \frac{d\Psi\,(r, \mathfrak{z})}{d\mathfrak{z}} \tag{3.18}$$

A comprehensive expression for the drain current, applicable across various operational regions, can be formulated as:

$$I_{DS} = \begin{cases} I_{GIDL}\ for -1.0 \le V_{GS} \le 0 \\ I_{SUB}\ for\ 0 \le V_{GS} \le V_{TH} \\ I_{LIN}\ for\ V_{TH} \le V_{GS} \le V_{SAT} \\ I_{SAT}\ for\ V_{SAT} \le V_{GS} \le 0.1V \end{cases} \tag{3.19}$$

Here OFF state leakage current (I_{GIDL}) is expressed as:

$$I_{GIDL} = XE^2(a, L)exp\left(\frac{-Y}{E(a, L)}\right) \tag{3.20}$$

Here,

$$X = \frac{q^2 m_r^{0.5}}{18\pi h^2 E_g^{1.5}},\ Y = \frac{\pi m_r^{0.5} E_g^{1.5}}{\sqrt[2]{2}qh},\ m_r = 0.2m_o$$

where, Planck's constant is denoted by h, represents a fundamental physical constant, while E_g symbolizes the energy band gap. The parameter m_r signifies the effective mass of the charge carrier, whereas m_o corresponds to the electron's rest mass.

The subthreshold current I_{SUB} is mathematically defined as:

$$I_{SUB} = \frac{t_{si}\pi\mu kT\eta_i^{1-e^{\frac{-V_{DS}}{V_{TH}}}}}{\int_0^L \frac{1}{\int_0^a e^{\frac{\Phi_i(\rho,z)}{kT}}}} \tag{3.21}$$

where the symbol μ characterizes the mobility of electrons, whereas k denotes Boltzmann's constant.

The expression for the current in the linear operating region, I_{LIN}, is articulated as:

$$I_{LIN} = \frac{t_{si}\pi\mu C_{OX}E_C}{(E_C L + V_{DS})}[(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \tag{3.22}$$

The expression for the current in the saturation region, I_{SAT} is articulated as:

$$I_{SAT} = \frac{t_{si}\pi\mu C_{OX}}{\left(1 + \frac{ß}{E_C L}(L - L_{SAT})\right)}[\lambda(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \tag{3.23}$$

Here,

$$\lambda = V_{DS} = V_{GS} - V_{TH}$$

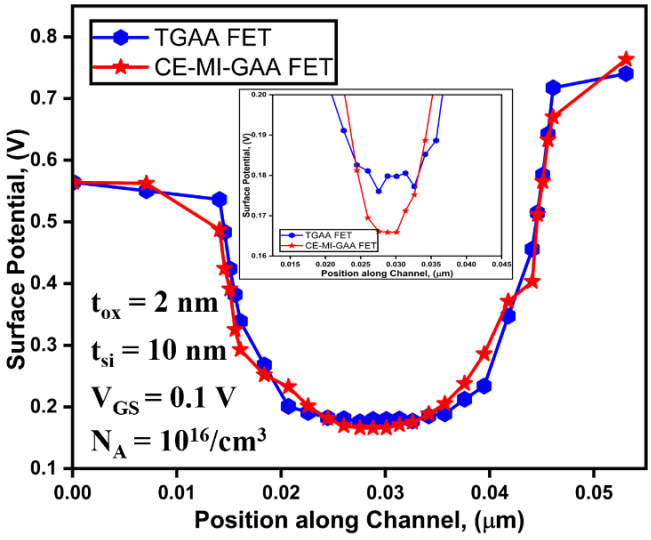
where L_{SAT} signifies the characteristic length while E_C refers to the energy of the conduction band, the variable λ is an empirical coefficient, with its value constrained from 0 to 1.

3.1.6 Results and Discussion

3.1.6.1 Comparative Simulation of TGAA FET and CE-MI-GAA FET

Figure 3.6 (a) comprises the disparity in potential along the orientation of the channel. In this, the potential of TGAA FET and CE-MI-GAA FET is almost the same, and a slight change in the potential of CE-MI-GAA FET is seen because of the presence of a vacuum filler in the center of the channel. The vacuum filler and vacuum oxide aid in capturing hot carrier injection, which greatly reduces electron tunnelling from the valence band to the conduction band. This reduction in electron tunneling results in a lower rate of BTBT. Figure 3.6 (b) contains the potential contour plots of TGAA FET and CE-MI-GAA FET along the orientation of the channel. Figure 3.6 (c) comprises the disparity in the vertical electric field along the orientation of the channel.

Figure 3.7 indicates the hole concentration along the orientation of the channel for TGAA FET and CE-MI-GAA FET. In the CE-MI-GAA FET, the central vacuum filler leads to a lower hole concentration. This reduction in hole concentration minimizes tunnelling effects and subsequently decreases GIDL. The parameter of hole concentration in these devices is calculated at V_{GS} = -1.0 V and V_{DS} = 1.0 V.



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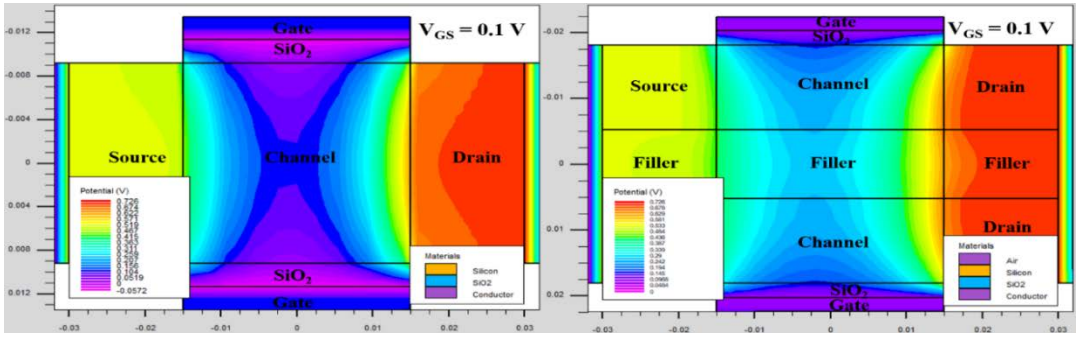

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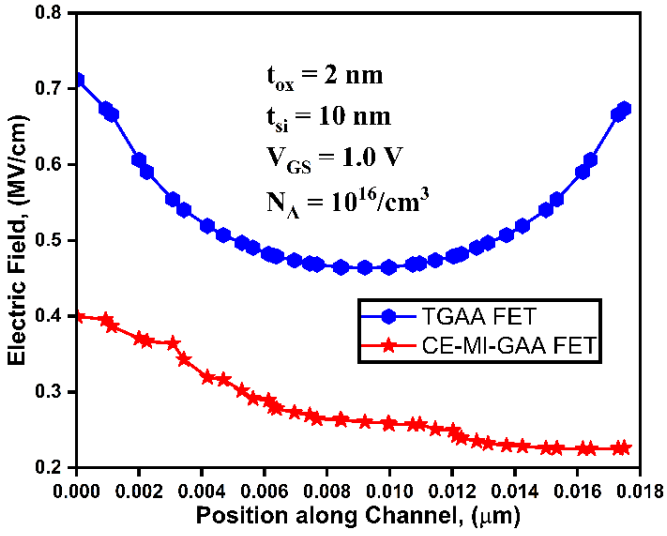


(c)

Figure 3.6 (a) Potential of TGAA FET and CE-MI-GAA FET along the orientation of the channel, (b) Potential contour of TGAA FET and CE-MI-GAA FET along the orientation of the channel, (c) Electric Field of TGAA FET and CE-MI-GAA FET along the orientation of the channel.

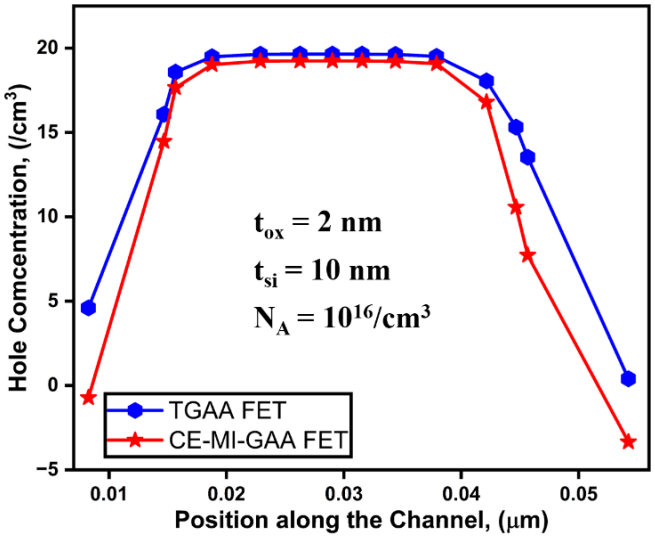


Figure 3.7 Concentration of Holes for TGAA FET and CE-MI-GAA FET along the orientation of the channel.

Figure 3.8 carries the details of the Band Energy of CE-MI-GAA FET at two different V_{DS} (0.0 V and 1.0 V). At V_{DS} = 1.0 V, a band bending is observed at the drain side. This is because of the presence of a vacuum filler at the center of the FET, which traps the hot ions traveling to the drain region. Due to this, DIBL is also reduced as the barrier between the channel and drain side is reduced, and the energy profile is altered in the proposed device.

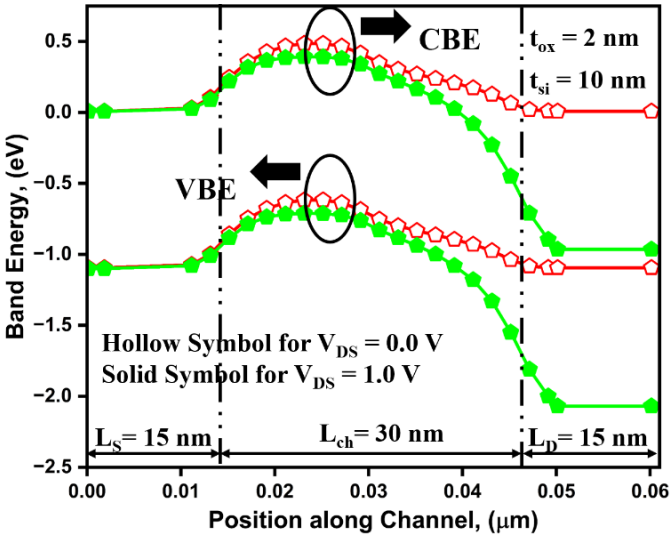
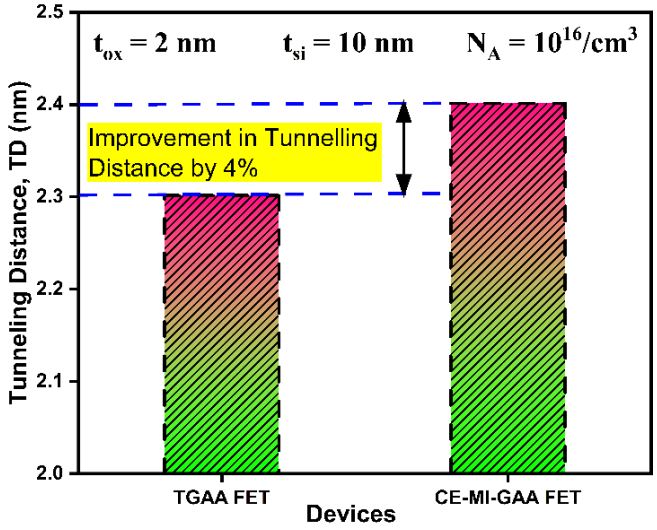


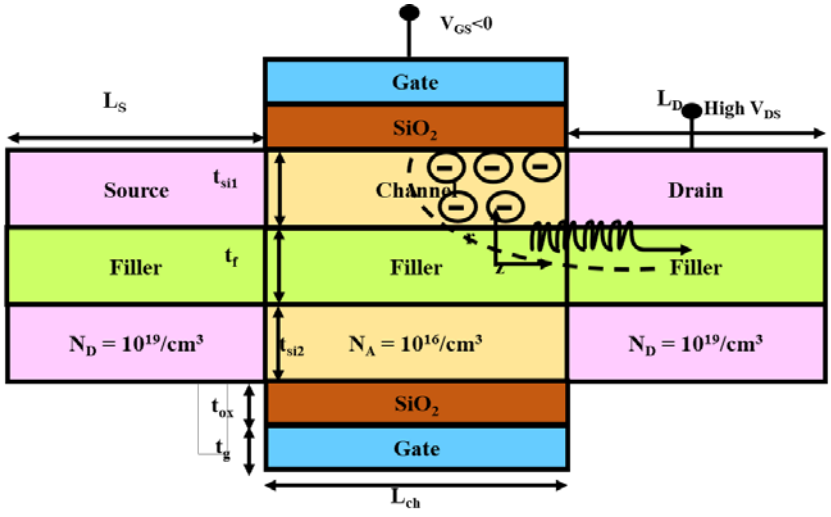
Figure 3.8 Energy Band Diagram of CE-MI-GAA FET.

Figure 3.9 demonstrates the tunnelling distance, which is the distance that an electron has to traverse while travelling from the valence band to the conduction band at V_{DS} = 1.0 V. In this manuscript, the tunnelling distance of the proffered CE-MI-GAA FET is 0.02301μm, whereas the TGAA FET has a tunnelling distance of 0.02401 μm. CE-MI-GAA FET has better results in comparison to TGAA FET because of the presence of a vacuum filler, which reduces the hot carrier effect, which in turn helps in reducing the BTBT. In this, the tunnelling distance of the proffered CE-MI-GAA FET is 4%

better than the traditional TGAA FET. Within the macaroni channel architecture, the incorporation of a vacuum filler establishes the potential barrier that intricately modulates carrier transport dynamics. This is so because the speed of trap charges (hot carriers) under the channel region is reduced towards the drain terminal. This inhibition of hot carriers under high electric fields leads to subsequent confinement at the vacuum semiconductor interface. This trapping mechanism effectively diminishes the population of hot carriers by mitigating their impact on device performance [175][59]. The trapping mechanism is detailed in Figure 3.9 (b).



(a)



(b)

Figure 3.9 (a) Tunnelling Distance of TGAA FET and CE-MI-GAA FET, (b) Hot carrier trapping mechanism for CE-MI-GAA FET.

Figure 3.10 indicates the variation in GIDL of TGAA FET and CE-MI-GAA FET at V_{DS} = 1.0 V. The phenomenon of leakage current is observed when the voltage of the drain is higher, and simultaneously, the gate is at a low voltage. In the figure, GIDL

of CE-MI-GAA FET is observed to be at 10^{-11} A whereas the TGAA FET has having GIDL of 10^{-9} A. This is because of the presence of a vacuum filler in the proffered device; it has an improvement of 202% when compared with TGAA FET.

Figure 3.11 contains the details of the Transfer Characteristics of an array of distinct device architectures. Due to the presence of a vacuum filler, the transfer characteristics of the proffered CE-MI-GAA FET are higher than TGAA FET. Because of the reduction of the leakage currents in the proposed device, the performance of the device is enhanced, and the device is considered best for analog applications.

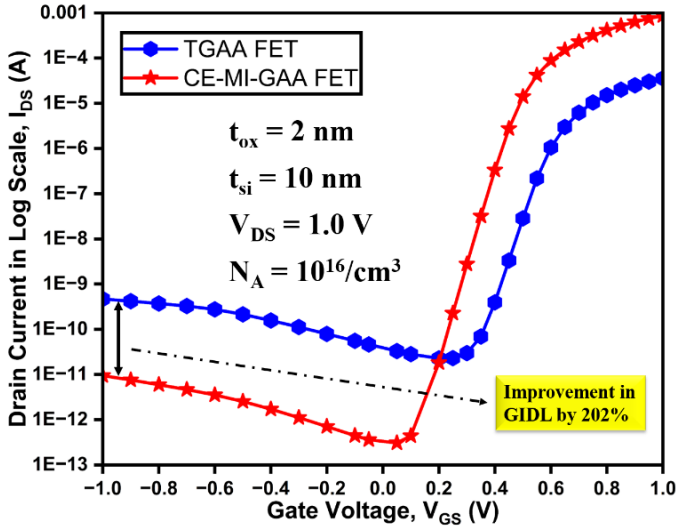
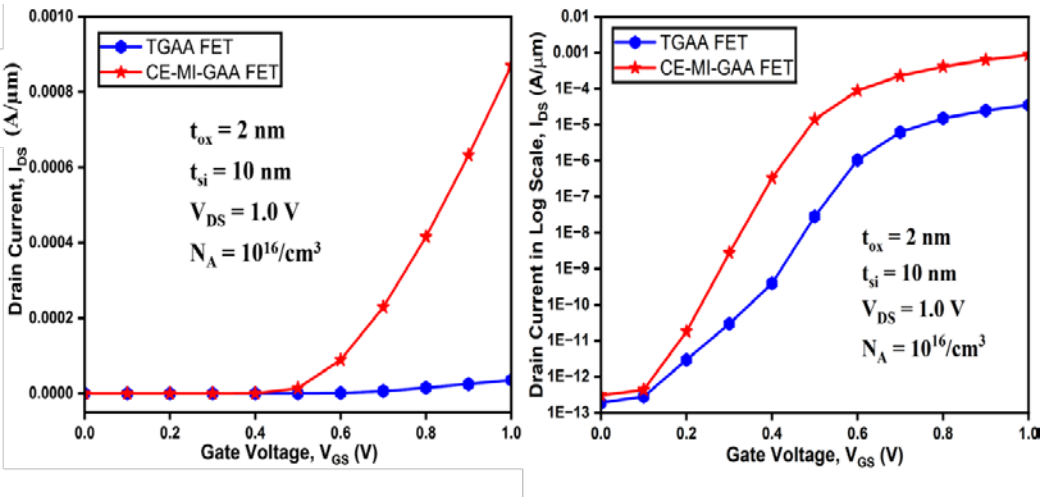


Figure 3.10 GIDL of TGAA FET and CE-MI-GAA FET along Gate Voltage.



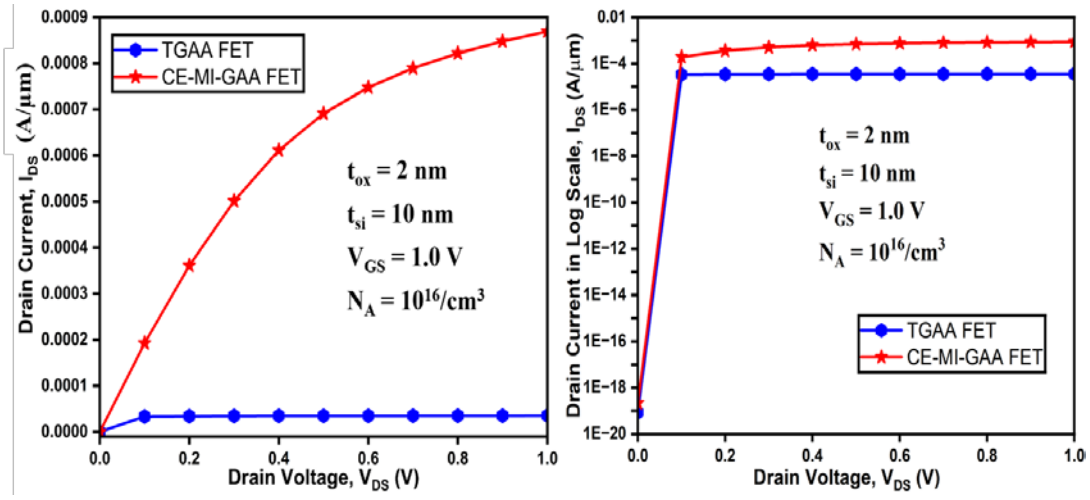
(a) (b)

Figure 3.11 (a) Transfer Characteristics along Gate Voltage, and (b) Transfer Characteristics in log scale along Gate Voltage.

Figure 3.12 depicts the Output Characteristics of the TGAA FET and CE-MI-GAA FET at V_{GS} = 1.0 V. The output characteristic of the proffered device is observed to be higher than the traditional FET because of the presence of filler at the centre of the nanowire FET, as it reduces the hot electron effect.

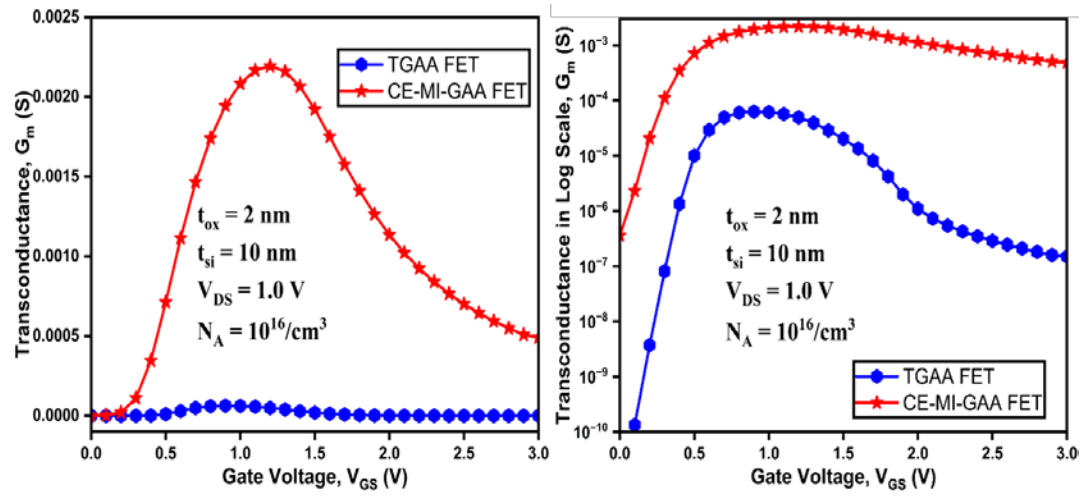
Figure 3.13 illustrates the Transconductance (g_m) of the different arrays of architectures discussed in this manuscript. g_m holds paramount importance not only within the domain of analog and RF applications but also in the precise determination of the optimal biasing condition. At the ideal bias point, each device exhibits a minimised cut-off frequency. The enhanced capability for current modulation, coupled with an elevated drain current, collectively contributes to achieving a significantly high transconductance value. g_m can be assessed as:

$$g_m = \left|\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \quad (3.24)$$



(a) (b)

Figure 3.12 (a) Output Characteristics of TGAA FET and CE-MI-GAA FET, and (b) Output Characteristics of TGAA FET and CE-MI-GAA FET in log scale.



(a) (b)

Figure 3.13 (a) Transconductance of TGAA FET and CE-MI-GAA FET, and (b) Transconductance of TGAA FET and CE-MI-GAA FET in log scale.

Figure 3.14 illustrates the Output Conductance (g_d) of the different arrays of architectures discussed in this manuscript. The presented data reveal that the CE-MI-GAA FET displays attributes that more closely approximate the ideal performance framework. This device showcases superior output conductance and an increased drain current, which can be ascribed to the incorporation of filler material and the variation in metalwork function disparities. g_d can be assessed as:

$$g_d = \left|\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}} \tag{3.25}$$

Figure 3.15 indicates the parameter, which is known as the subthreshold slope, which is also described as the flipping of devices from the OFF state to the ON state. The optimum value of SS in an ideal nanowire is considered close to 60 mV/decade. In this manuscript, the subthreshold slope values for the TGAA FET and CE-MI-GAA FET are 73.83 mV/decade and 65.86 mV/decade, respectively. The gate leakage current originates solely from the channel, reducing leakage due to the filler, which forms the macaroni channel structure within the channel region.

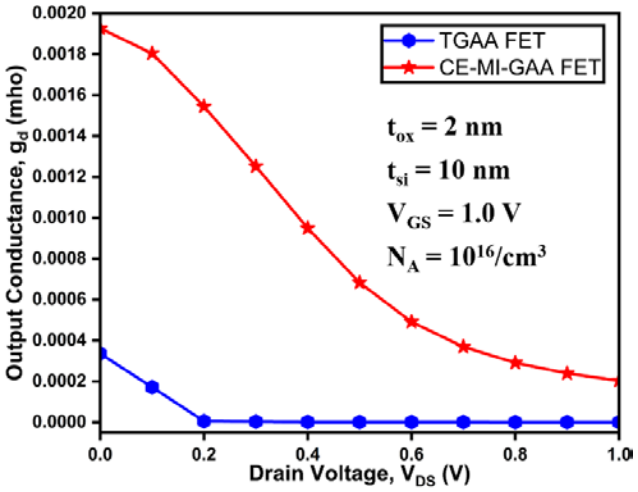


Figure 3.14 Output Conductance changes along Drain Voltage.

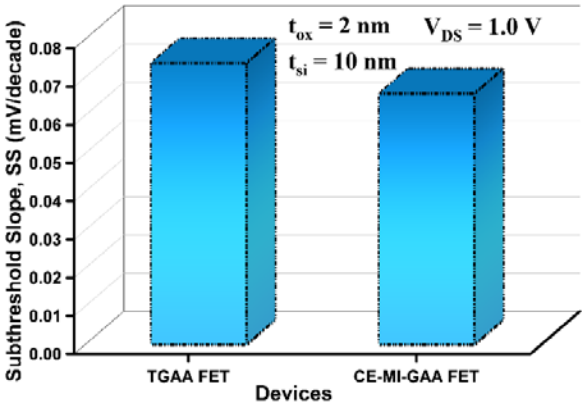


Figure 3.15 Subthreshold Slope for an array of distinct device architectures.

Figure 3.16 describes the I_{ON}/I_{OFF} ratio for TGAA FET and CE-MI-GAA FET. The I_{ON}/I_{OFF} ratio is the ratio of the ON current to the OFF current of the devices. The I_{ON}/I_{OFF} ratio for CE-MI-GAA FET shows a 2638-fold improvement over TGAA FET. For better performance of the device, the I_{ON}/I_{OFF} ratio of the proffered device should be higher than other devices. In CE-MI-GAA FET I_{ON} current of the device is higher because of the filler at the centre of the nanowire, hence the I_{ON}/I_{OFF} ratio of the device is higher.

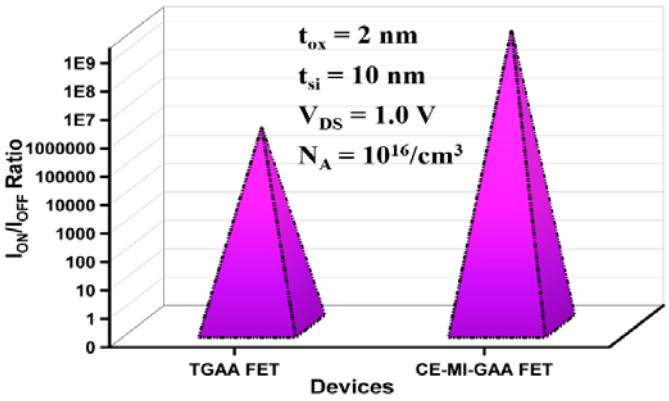


Figure 3.16 I_{ON}/I_{OFF} for an array of distinct device architectures.

Figure 3.17 contains a detailed comparison of TGAA FET and CE-MI-GAA FET in terms of Drain-Induced Barrier Lowering (DIBL). When a drain-source voltage (V_{DS}) is applied, Drain-Induced Barrier Lowering (DIBL) results in a decline of the threshold voltage (V_{th}). In the case of CE-MI-GAA FET, the use of a vacuum filler significantly diminishes the electric field within the drain region, thereby reducing the impact of DIBL and minimizing the associated drop in threshold voltage. As illustrated in the figure, the reduction of DIBL is noted to be 1.5 times in the CE-MI-GAA FET when compared to the TGAA FET device. DIBL can be assessed as:

$$DIBL = -\frac{V_{th}(V_{DD}) - V_{th}(V_{DDlow})}{V_{DD} - V_{DDlow}} \quad (3.26)$$

Figure 3.18 indicates the Transconductance Generation Factor (TGF), which can also be described as the reflection of the steepness of the Subthreshold Slope (SS). TGF serves as an indicator of the efficiency of semiconductor devices. In the design of low-power analog circuits, it is imperative to maintain a high TGF. Elevated TGF confers the advantage of enabling circuit functionality at reduced supply voltages, thus enhancing operational efficiency. TGF is assessed as:

$$TGF = \frac{g_m}{I_{DS}} \quad (3.27)$$

Figure 3.19 demonstrates the Total Gate Capacitance (C_{GG}) for TGAA FET and CE-MI-GAA FET, and C_{GG} is inversely proportional to f_T; hence, for high-frequency and high-speed applications, C_{GG} should be lower. The permittivity of FET is directly correlated with its capacitance. More precisely, the total gate capacitance (C_{GG}) of the FET represents the summation of the gate-to-source capacitance (C_{GS}) and the gate-

to-drain capacitance (C_{GD}). This figure demonstrates that the proffered CE-MI-GAA FET has lower C_{GG} when compared to the TGAA FET. This is because of the filler vacuum at the centre of the proffered device. C_{GG} can also be assessed as:

$$C_{GG} = C_{GS} + C_{GD} \tag{3.28}$$

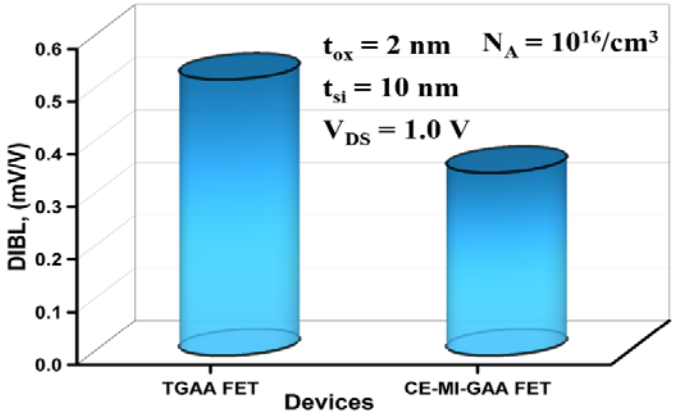


Figure 3.17 DIBL for an array of distinct device architectures.

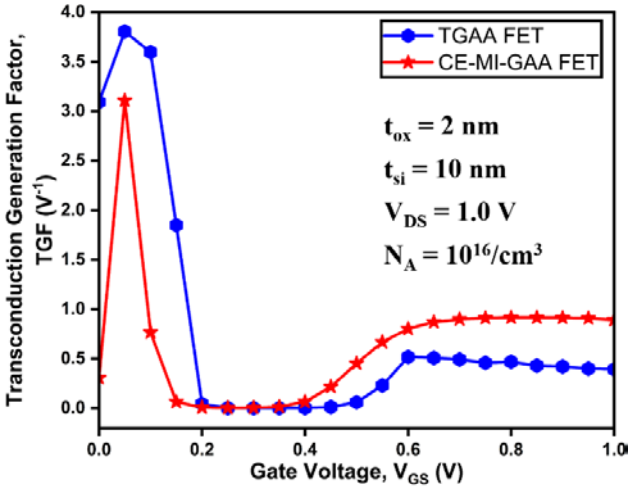


Figure 3.18 Transconductance Generation Factor for CE-MI-GAA FET.

Figure 3.20 illustrates the Cut-Off Frequency (f_T) of various distinct device architectures. Cut-off frequency is a very important parameter for high-frequency applications. The Cut-Off Frequency (f_T) governs the high-frequency performance of a device. To ensure optimal functionality at elevated frequencies, the value of f_T must be sufficiently high. It exhibits a direct proportionality to the transconductance (g_m) while maintaining an inverse relationship with the total gate capacitance (C_{GG}). f_T can be assessed as:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{3.29}$$

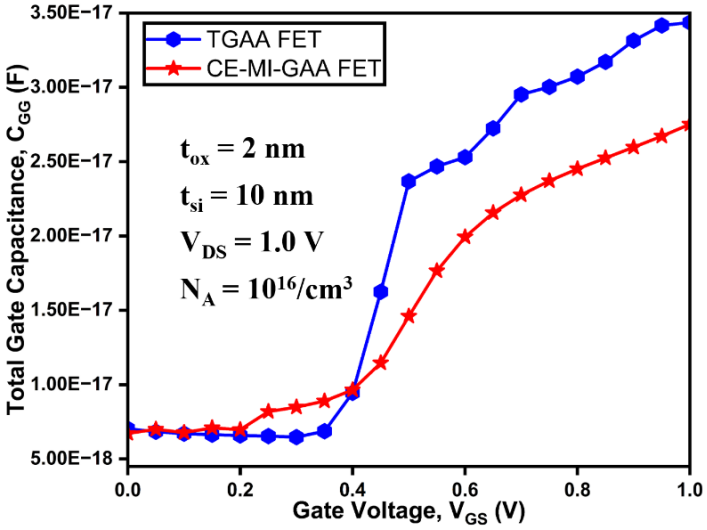
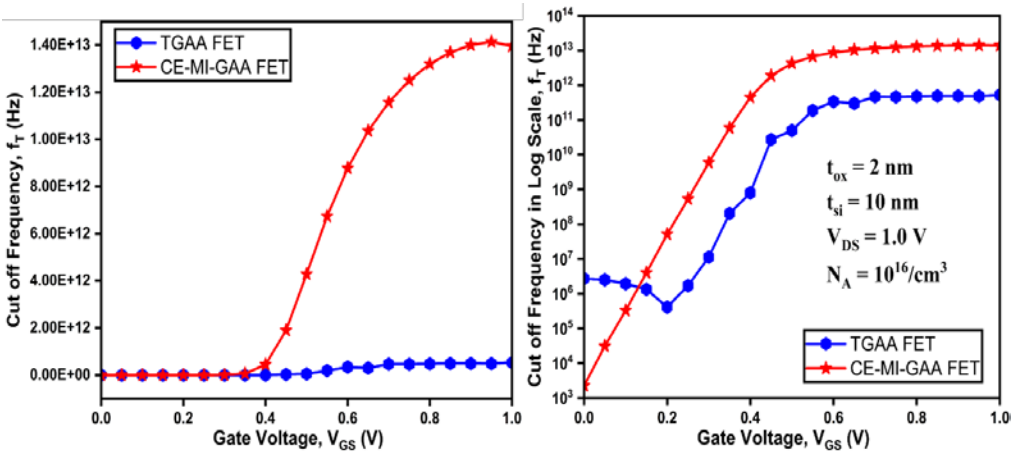


Figure 3.19 Total Gate Capacitance for CE-MI-GAA FET.

Figure 3.21 represents the phenomenon known as Early Voltage, which is also denoted as V_{EA}. In this figure, the V_{EA} of CE-MI-GAA FET is higher than the traditional FET because of the presence of a vacuum filler at the centre, which helps in reducing the hot carriers by trapping them, and in turn, V_{EA} is increased. In the case of MOSFETs, the corresponding phenomenon is called Channel Length Modulation (CLM). It occurs when to source voltage is increased, which in turn shortens the effective length, leading to a slight increase in the drain current even in saturation. CE-MI-GAA FET has a higher early voltage when compared with TGAA FET. This leads to enhanced gain, and hence, this device can be considered an ideal device for amplifiers [179][180][181][182]. V_{EA} is assessed by:

$$V_{EA} = \frac{I_{DS}}{g_d} \tag{3.30}$$



(a) (b)

Figure 3.20 (a) Cut-off Frequency for CE-MI-GAA FET, and (b) Cut-off Frequency in log scale for CE-MI-GAA FET.

Figure 3.22 describes the Intrinsic Gain (A_v) of TGAA FET and CE-MI-GAA FET at V_{GS} = 1.0 V. Intrinsic Gain (A_v) is defined as the proportional relationship between transconductance and output conductance. As gate voltage increases, the decline in carrier mobility leads to a consequent deterioration in the gain. This situation aligns with the principle that "every action has an equal and opposite reaction," as described by Newton, highlighting the delicate balance between electrical properties in semiconductor devices. A_v can be assed by:

$$A_v = \frac{g_m}{g_d} \tag{3.31}$$

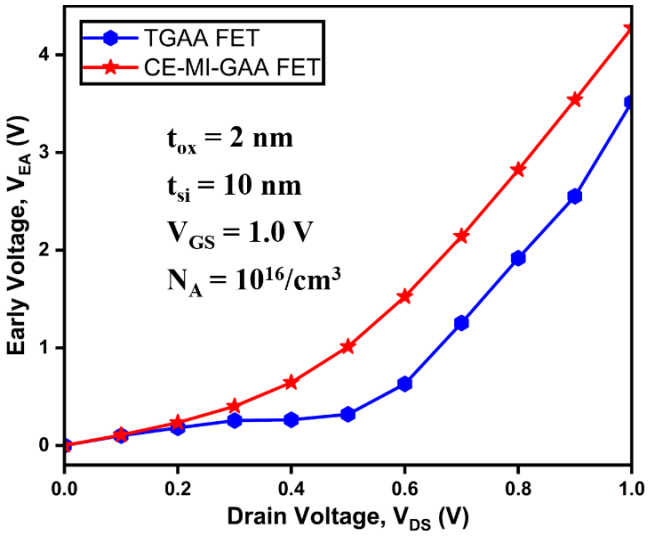


Figure 3.21 Variation in Early Voltage as a function of Drain Voltage.

Figure 3.23 illustrates the Quality Factor for TGAA FET and CE-MI-GAA FET. The Quality Factor (Q-factor) serves as an analytical metric to assess and quantify both the switching efficiency and performance characteristics of the devices. The CE-MI-GAA FET exhibits a Q-factor that is elevated by a factor of 27 when contrasted with that of the TGAA FET. This elevated output is observed because of the presence of filler at the centre of the channel that helps in trapping the hot carriers. It poses a significant hindrance in the assessment of device performance within mixed-signal application contexts. Q-factor can also be assessed by:

$$Q = \frac{g_m}{SS} \tag{3.32}$$

Figure 3.24 contains the details of the fluctuation of Channel Resistance (R_{ch}) of TGAA FET and CE-MI-GAA FET with V_{GS}. The CE-MI-GAA FET exhibits a markedly reduced channel resistance (R_{ch}) relative to the TGAA FET. The integration of a vacuum as a filler effectively suppresses both impact ionization and tunnelling phenomena, while simultaneously contributing to an increase in subthreshold leakage currents.

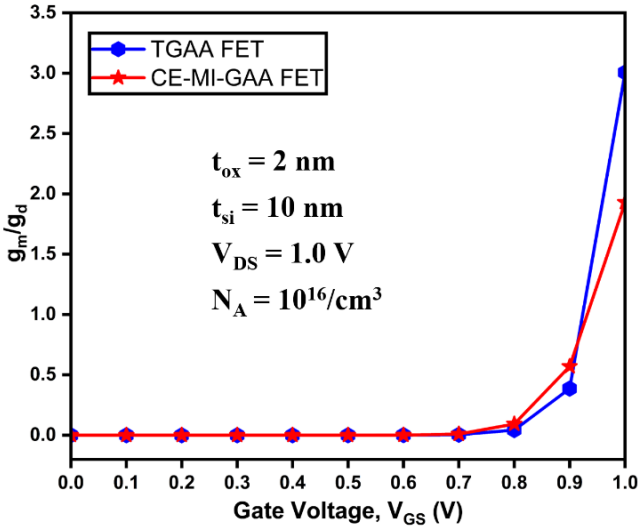


Figure 3.22 Intrinsic Gain for an array of distinct device architectures.

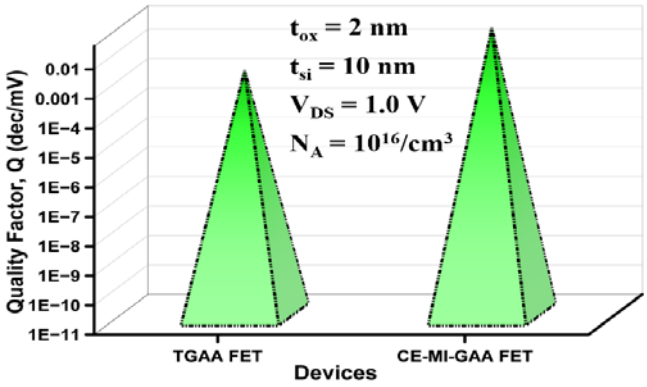


Figure 3.23 Q-Factor for an array of distinct device architectures.

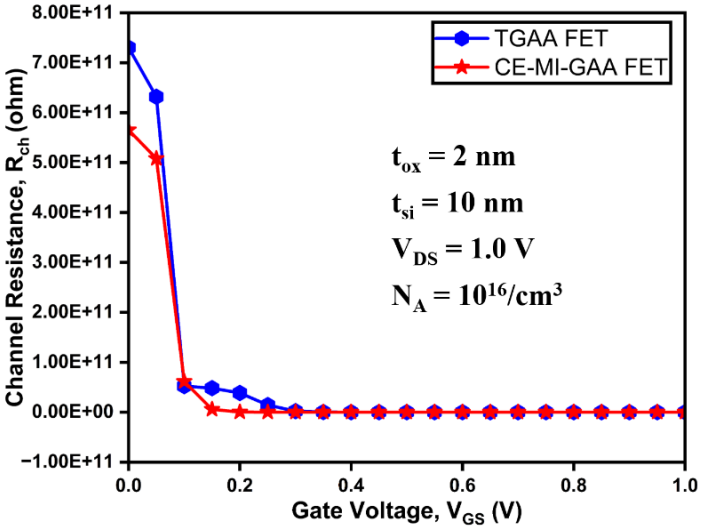


Figure 3.24 Channel Resistance for an array of distinct device architectures.

3.1.6.2 Mathematical Validation of *CE-MI-GAA FET*

Figure 3.25 contains the simulated GIDL result of the CE-MI-GAA FET in comparison with the analytical result. It can be concluded from the figure that the simulated result and analytical results are in agreement with each other. GIDL of CE-MI-GAA FET is observed to be at 10^{-11} A. This is because of the presence of a vacuum filler in the proffered device.

Figure 3.26 illustrates the disparity in potential along the orientation of the channel. In this, the potential of the simulated result is in agreement with the analytical result. This change in potential is seen because of the presence of a vacuum filler in the center of the channel. The vacuum filler and vacuum oxide aid in capturing hot carrier injection, which greatly reduces electron tunnelling from the valence band to the conduction band. This reduction in electron tunneling results in a lower rate of BTBT.

Table 3.3 and Table 3.4 present a detailed comparative analysis between the proffered structure CE-MI-GAA FET and TGAA FET, as well as with other leading-edge devices. This comparison highlights the performance distinctions, showcasing the advantages of CE-MI-GAA FET architecture in the field of cutting-edge transistor technologies.

Table 3.3 and Table 3.4 present a detailed comparative analysis between the proffered structure CE-MI-GAA FET and TGAA FET, as well as with other leading-edge devices. This comparison highlights the performance distinctions, showcasing the advantages of CE-MI-GAA FET architecture in the field of cutting-edge transistor technologies.

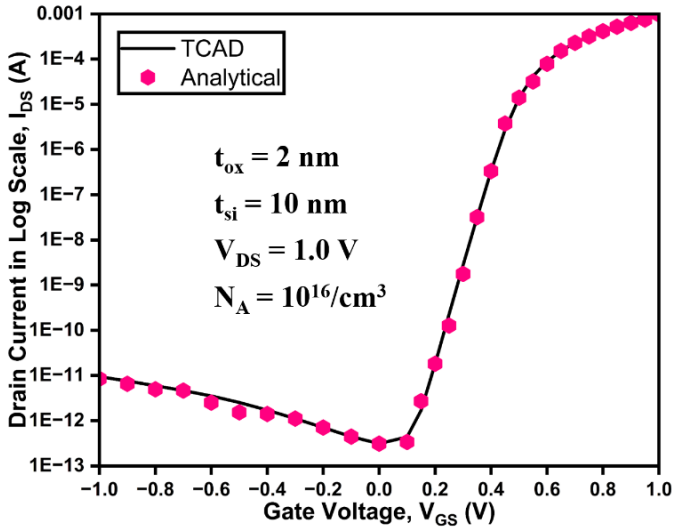


Figure 3.25 GIDL of CE-MI-GAA FET along Gate Voltage.

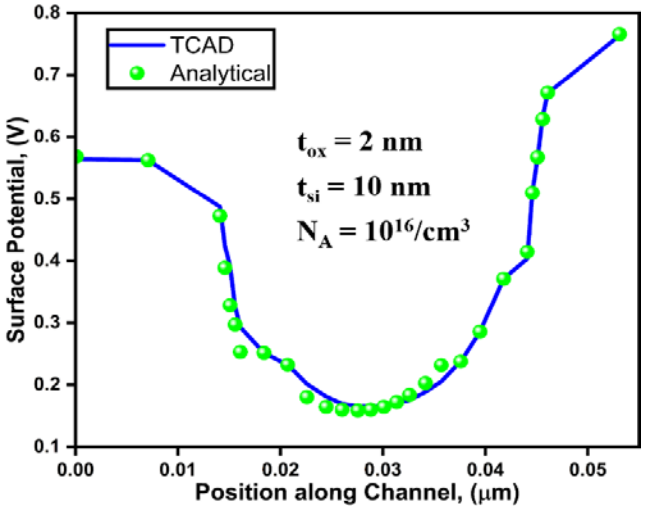


Figure 3.26 Potential of CE-MI-GAA FET along the orientation of the channel.

TABLE 3.3: COMPARISON OF CE-MI-GAA FET AND TGAA FET

Parameters	TGAA FET	CE-MI-GAA FET
I_{ON}/I_{OFF} ratio	1.08E+06	2.84E+09
Tunnelling Distance (*nm*)	24	23
GIDL (*A/μm*) at V_{GS} = -1.0 V	4.69E-10	1.10E-11
Channel Resistance (*ohm*) at V_{GS} = 0.0 V	7.30E+11	5.65E+11
Hole Concentration (*/cm^3*) at L = 15 nm	1.96E+01	1.92E+01
Transconductance (*S*) at V_{GS} = 1.0 V	2.15E-06	3.93E-04
Transconductance Generation Factor (*/V^{-1}*) at V_{GS} = 0.0 V	3.93E-01	8.91E-01
Subthreshold Slope (*mV/decade*)	73.83	65.86
Early Voltage at V_{DS} = 1.0 V	3.52E+00	4.28E+00
Output Conductance (*mho*) at V_{DS} = 1.0 V	7.17E-07	2.03E-04
Cut-off Frequency (*Hz*) at V_{GS} = 1.0 V	5.30E+11	1.40E+13
Intrinsic Gain at V_{GS} = 1.0 V	1.48E+01	1.19E+01
Total Gate Capacitance (F) at V_{GS} = 1.0 V	3.44E-17	2.75E-17

TABLE 3.4: COMPARISON OF CE-MI-GAA FET WITH LEADING-EDGE DEVICES

Parameters	DMISE GAA MOSFET [183]	NW FET [42]	GAA MOSFET [184]	CE-MI-GAA FET (this work)
Tunnelling Distance *(nm)*	13	19.5	5	23
GIDL *(A/μm)* at V_{GS} = -1.0 V	3.17E-13	3.38E-10	1.99E-10	1.10E-11
I_{ON}/I_{OFF} ratio	9.37E+06	1.44E+07	2.36E+06	2.84E+09
Transconductance *(S)* at V_{GS} = 1.0 V	1.58E-03	1.96E-03	1.11E-03	3.93E-04
Subthreshold Slope *(mv/decade)*	71.7	60	72.9	65.86
Cut-off Frequency *(Hz)* at V_{GS} = 1.0 V	1.22E+13	1.50E+13	9.03E+12	1.19E+01

3.1.7 Comparative Analysis

CE-MI-GAA FET exhibits significant advantages when benchmarked against TGAA FETs and other leading-edge designs. The GIDL of CE-MI-GAA FET is 202% lower at V_{GS} = -1.0 V due to the filler-induced tunnelling suppression when compared with TGAA FET. The tunnelling distance of the proposed structure is to have 4% improvement, thus lowering the BTBT current. The I_{ON}/I_{OFF} Ratio of CE-MI-GAA FET is showing three orders of magnitude improvement with a value of 2.84 x $10^{9,}$ whereas the I_{ON}/I_{OFF} ratio of TGAA FET is 1.08 x 10^{6}. The subthreshold Slope of CE-MI-GAA FET is observed to be 65.86 mV/decade, which is close to the ideal value. The quality factor, early voltage, and cut-off frequency of the proposed structure are showing promising results [150]. When comparing with other advanced devices such as DMISE GAA MOSFETs [183] and NW-FETs, the proposed CE-MI-GAA FET demonstrates competitive and superior leakage suppression while maintaining robust analog performance, which is an uncommon combination when nanoscale device engineering is considered. Figure 3.27 contains the comparative performance of TGAA FET, CE-MI-GAA FET, and other advanced devices discussed in this chapter. This graph provides a holistic visualization of the performance metrics. This plot clearly demonstrates the dominance of the CE-MI-GAA FET, particularly in leakage suppression, analog stability, and frequency response, thereby validating its architectural advantages over conventional devices.

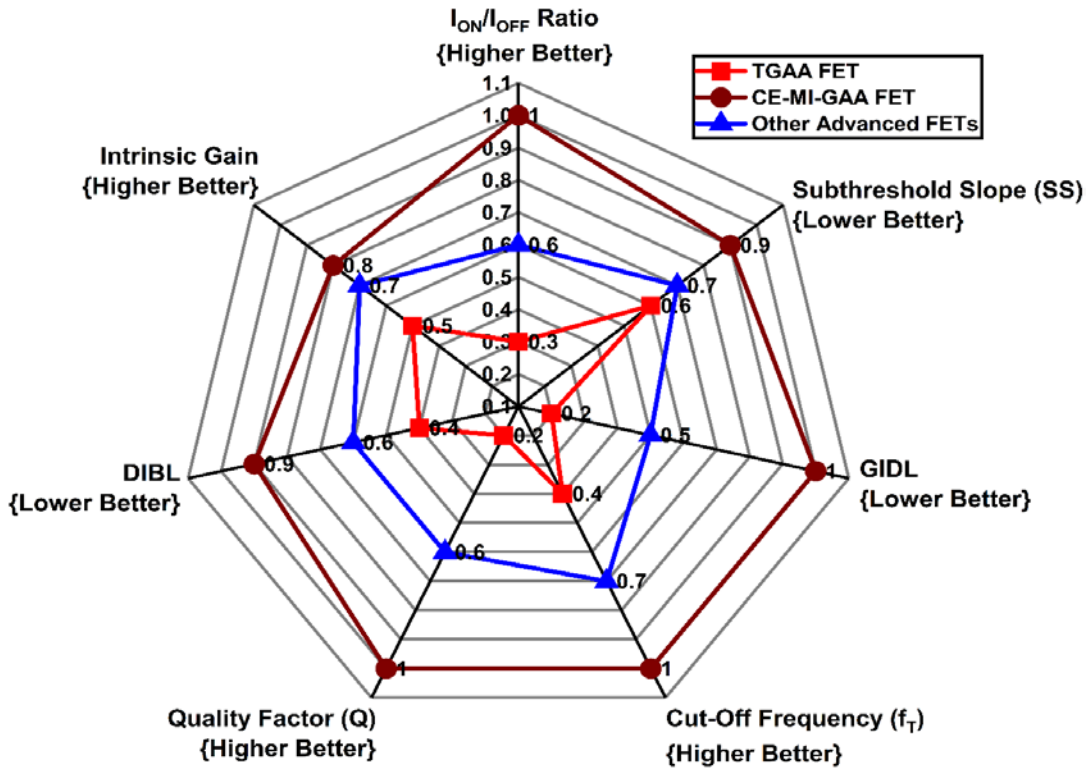


Figure 3.27 Comparative Analysis of Devices in Radar Graph

3.1.8 Challenges and Considerations

While the Channel-Engineered Macaroni Gate-All-Around Field Effect Transistor (CE-MI-GAA FET) shows compelling benefits in terms of leakage suppression, design flexibility and electrostatic control, a number of practical and theoretical challenges still need to be carefully addressed for its successful realization. One of the primary concerns involves thermal effects, as the incorporation of vacuum or low-κ dielectric fillers within the hollow channel significantly alters the heat dissipation pathways. Under high drain bias or dense circuit operation, the limited thermal conduction through these fillers can lead to localized self-heating, which leads to degradation of mobility and increases junction leakage. Therefore, thermal interface engineering and multi physics based thermal simulations become essential to ensure uniform temperature distribution and prevent reliability [185].

Another critical issue is the fabrication complexity associated with creating a uniform hollow core surrounded by precise filler material at nanometer scales. Achieving consistent etch depth, filler uniformity, and conformal coating across all nanowires requires advanced isotropic etching control, high aspect-ratio process management and accurate deposition through atomic layer deposition (ALD) techniques [186].

Furthermore, device variability and reliability are emerging challenges for CE-MI-GAA FETs. The interface states and trapped charges at the filler silicon interface could introduce threshold voltage fluctuations, increase trap-assisted leakage and increase subthreshold leakage especially under bias stress or high temperature conditions. Long term reliability must also consider potential filler induced mechanical stress, which can modify channel strain and lead to performance inconsistency [187].

Another obstacle is process integration, as the fabrication of the hollow region and filler insertion must be compatible with standard CMOS manufacturing flows. The inclusion of new materials or etching steps must not introduce cross-contamination risks, nor should it disrupt backend of line reliability or gate dielectric integrity. Achieving this integration demands optimized cleaning, contamination control protocols and encapsulation to ensure process stability across large wafers [188].

Finally, scalability limits become a major concern as the proposed CE-MI-GAA FET approaches sub-5 nm technology node, where surface scattering, quantum confinement and ballistic transport effects begin to dominate device behaviour [189]. The advantages derived from filler induced electrostatic modulation may diminish or become unpredictable in this regime, necessitating details quantum-corrected simulations and experimental verification. Addressing these challenges requires a synergistic approach involving interface defect passivation, device level thermal and electrical design and advanced process optimization. Continued research into reliable filler materials, scalable integration methodologies and etching selective enhancement will be crucial for translating the theoretical C-MI-GAA FET into robust and manufacturable semiconductor technology.

Summary

In this chapter the simulation and analytical modelling of the proposed Channel Engineered Macaroni Induced Gate All Around Field Effect Transistor (CE-MI-GAA FET) has revealed the potential of the device in tackling one of the most pressing

challenges in modern nanoelectronics: the suppression of leakage current without reducing the ON-state performance of the device. This chapter includes a methodical account of the operating principle, device architecture, modelling framework, and comparative evaluation of CE-MI-GAA FET, which is validated by the calibrated simulation and analytical formulations.

The electrostatics and the transport properties of the proposed device are fundamentally altered by the inclusion of a hollow macaroni channel filled with vacuum. The inclusion of the hollow macaroni layer in CE-MI-GAA FET helps in reducing the field penetration, increases tunnelling path length, and traps high-energy charge carriers at the filler semiconductor interface, whereas in the traditional GAA FETs, the drain to source coupling enhances the Gate Induced Drain Leakage (GIDL) and degrades the subthreshold. This innovative channel modification strategy resulted in a 202% reduction in GIDL, a 2638-fold improvement in I_{ON}/I_{OFF} ratio, and a 27 times improvement in the quality factor of the CE-MI-GAA FET device compared with TGAA FET. These improvements not only underscore the effectiveness of the filler-based electrostatic modulation but also highlight the importance of structural and material innovations in scaling transistors beyond conventional and Fin FET technologies.

When device physics is taken into account, the CE-MI-GAA FET bridges the gap between the conventional GAA architecture and next-generation channel-engineered architectures. By using a low permittivity filler, the capacitive coupling of the device is reduced within the core, which contributes to lowering the subthreshold slope (65.86 mV/decade) and improves the immunity towards the Drain Induced Barrier Lowering (DIBL). These metrics bring the device performance closer to the ideal electrostatic limits of nanoscale devices, where leakage suppression and subthreshold switching efficiency are simultaneously optimized.

When the proposed CE-MI-GAA FET is benchmarked against other cutting-edge technologies such as Dual Metal Insulated Shallow Extension (DMISE) GAA MOSFETs [183], Nanowire FETs (NW FETs) [42], and Hetero-dielectric Macaroni Channel FETs [184], the CE-MI-GAA FET exhibits superior or comparable performance. In DMISE, the analog performance of the device is improved due to the dual metal gate engineering, and in NW FETs, the leakage reduction is observed due to the tighter gate channel coupling; neither approach demonstrates the holistic combination of leakage suppression, frequency response, and analog suitability achieved by CE-MI-GAA FET. The CE-MI-GAA FET device is a viable choice for RF and analog circuit applications because of its high intrinsic gain, low output conductance, and cutoff frequency of 1.4×10^{13} Hz. In digital logic circuits, the high I_{ON}/I_{OFF} ratio translates to reduced standby power consumption, enabling more energy-efficient memory arrays and processors. In analog and RF circuits, a high transconductance generation factor (TGF), quality factor, and early voltage ensure better noise immunity and signal amplification. These characteristics position it as a multi-domain device, capable of both low-power portable and high-performance computing electronics.

The fabrication of the proposed CE-MI-GAA FET is a challenge that cannot be overlooked. Achieving precise isotropic etching to create a uniform hollow filler and integrating this filler into standard CMOS processing is a trivial task. While etching, the structural stability of the silicon shell is also to be maintained. The thermal limitations of the device must be studied in detail, which occurs due to reduced heat dissipation pathways in hollow filler structures. Addressing these challenges is critical for transitioning the CE-MI-GAA FET from a research concept to a manufacturable technology.

In conclusion, CE-MI-GAA FET device architecture stands as a strong candidate for the future of scaling in semiconductors. Its ability to simultaneously address leakage suppression, high-frequency operation, and analog performance validated through analytical modelling and TCAD simulations reflects its technological promise and scientific novelty. This structure introduces a new design paradigm, but fabrication remains a challenge where channel engineering is exploited not merely as geometry but as a mechanism that can modulate carrier dynamics. This position CE-MI-GAA FET at the forefront of post-FinFET device research, contributing to the ongoing evolution of Gate-All-Around architectures for the nanoscale era.

Annexure-I

$$A = \delta - \frac{e^{L\lambda}}{M(e^{2L\lambda}-1)}\left[e^{L\lambda}[2\varepsilon_{si}V_{BI}J_1(\lambda a)]\right] - [2\varepsilon_{si}(V_{BI}-V_{DS})J_1(\lambda a)] \tag{3.33}$$

$$B = \frac{e^{L\lambda}}{M(e^{2L\lambda}-1)}\left[e^{L\lambda}[2\varepsilon_{si}V_{BI}J_1(\lambda a)]\right] - [2\varepsilon_{si}(V_{BI}-V_{DS})J_1(\lambda a)] \tag{3.34}$$

$$\delta = \frac{2}{a^2J_1^2(\lambda a)}\left[\frac{V_{BI}aJ_1(\lambda a)}{\lambda} - \frac{aV(a)J_1(\lambda a)}{\lambda} + \frac{qN_Aa^2J_2(\lambda a)}{2\lambda\varepsilon_{si}}\right] \tag{3.35}$$

$$M = \frac{1}{aJ_1^2(\lambda a)\lambda\varepsilon_{si}} \tag{3.36}$$

CHAPTER 4

ANALYTICAL MODELING AND NUMERICAL SIMULATION OF DOUBLE-GATE MACARONI CHANNEL FIELD EFFECT TRANSISTOR

In chapter 3, the primary focus was on the architectural design, operating principles, and comparative advantages of the proposed nanowire transistor structure. Th this chapter, the emphasis is on the analytical modelling and performance evaluation of the proposed nanowire transistor structure. Chapter 3 laid all the groundwork by establishing the theoretical foundation of device architectures and their relevance in addressing the limitations of conventional nanowire transistors. To transform the architectural concepts into verifiable and practically realizable solutions, it is imperative to develop analytical models and validate them against simulation outcomes. Chapter 4 introduces the detailed mathematical formulations that describe the charge transport mechanism and electrostatic behavior in the proposed architectures. This progression of conceptual architecture to analytical and simulation-based validation bridges the gap between theoretical design and practical applicability.

34 The relentless scaling of metal oxide semiconductor field-effect transistors (MOSFETs) has underpinned advancements in the semiconductor industry, aligning with Moore's law for over fifty years. Conventional bulk MOSFETs face critical performance barriers as the technology node sinks into the sub-10 nm domain. These include elevated subthreshold leakage, quantum phenomena, increased variability from random dopant distribution, diminished gate control, and short channel effects (SCEs) [20]. Such limitations have spurred the exploration of novel device architectures that can continue this scaling trend while maintaining high performance, manufacturability, and low power consumption.

95 Among various breakthroughs, the most significant have been the multi-gate transistor devices such as Gate All Around (GAA) nanowire transistors and FinFETs. FinFETs mark a substantial improvement over planar MOSFETs in terms of electrostatics, but their control deteriorates at extremely short channel lengths, i.e., below 7 nm [190]. By enveloping the channel entirely with the gate, GAA FETs offer reduced SCEs and superior electrostatic integrity. This surrounding gate architecture improves threshold stability, yields a steeper subthreshold slope, improves gate to channel coupling, and lowers drain induced barrier lowering (DIBL) [191].

Within the GAA FET family, the Macaroni Channel-induced Nanowire FET (MC NW FET) has emerged as a promising innovation. In this configuration, the silicon channel is formed with a hollow channel in the center, which is then surrounded by an oxide layer and gate metal, which resembles a piece of macaroni, hence the name. With the presence of this hollow center, the hot carriers are trapped, which in turn helps in reducing the leakage current and thus helps in enhancing the performance of the device. A comparative study of MC NW FET and conventional nanowire FET reveals

the advantages of the Macaroni channel device. This unique design aids in offering better pathways for heat dissipation and thus mitigating self-heating issues [42]. The presence of dual metal gates results in better electrostatic control, which helps in reducing the SCEs and improves the device outcomes. Hence, the device architecture is well-suited for high-speed digital logic and ultra-low power analog and RF circuit applications.

In this chapter, various structural modifications have been proposed:

Double Metal Gate Macaroni Nanowire FET (DMGM-NFET) incorporates two metal gates with different work functions to fine-tune threshold voltage and suppress leakage currents. In this configuration, the metal gate near the source possesses a higher work function while the gate adjacent to the drain has a lower work function resulting in a built-in step potential along the channel [192]. The hollow cylindrical macaroni channel allows gate to surround the channel completely, ensuring uniform field distribution and excellent control over channel inversion. The dual metal combination enhances carrier transport efficiency, improves ON state current and reduces OFF state leakage making it a promising architecture for mixed signal nanoscale and high-performance digital applications. The Figure 4.1 illustrates the pictorial representation of DMGM-NFET.

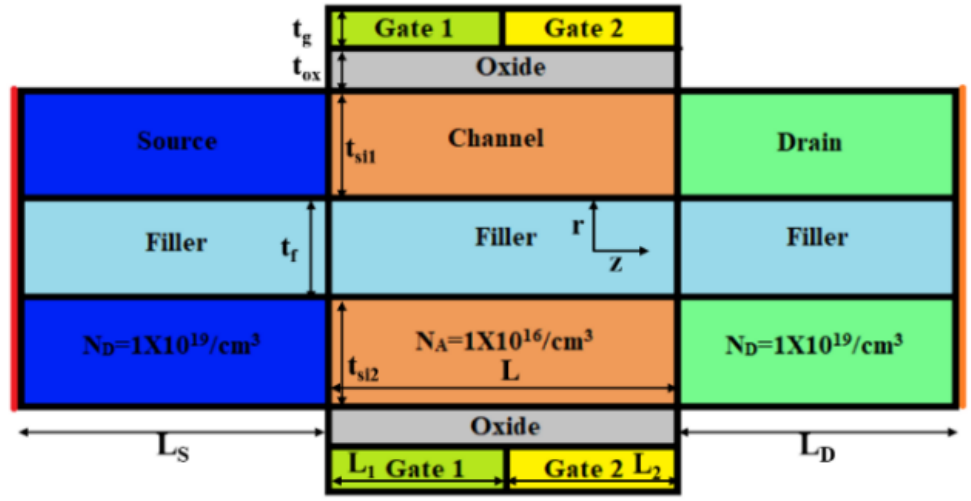


Figure 4.1 Pictorial representation of DMGM-NFET [192].

Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET) incorporates two metal gates with different work functions, with symmetrical dual oxides with different permittivity to reduce the gate leakage and enhance analog parameters [193]. The hetero dielectric structure helps in improving subthreshold swing, intrinsic gain and transconductance while maintaining low gate leakage. The macaroni hollow cylindrical channel improves the device stability and analog performance. Owing to its optimized gate stack and electrostatic symmetry, the HD-MC-CGAA FET is well suited for low power analog and sensor applications, where high gain and low leakage are critical performance parameters. The Figure 4.2 illustrates the pictorial representation of HD-MC CGAA FET.

Channel Interface Engineered-Electrostatic Potential, Modulated Field Effect Transistor (CIE-EPM FET) incorporates two metal gates with different work functions to fine-tune threshold voltage and suppress leakage currents. In this, the results are validated by comparing them with the analytical results. The Figure 4.3 illustrates the pictorial representation of CIE-EPM FET.

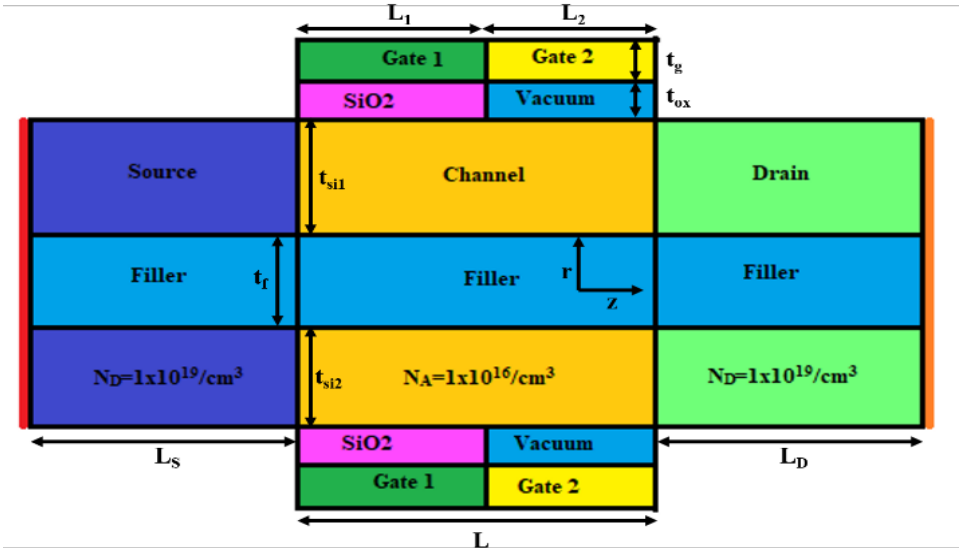


Figure 4.2 Pictorial representation of HD-MC CGAA FET [193].

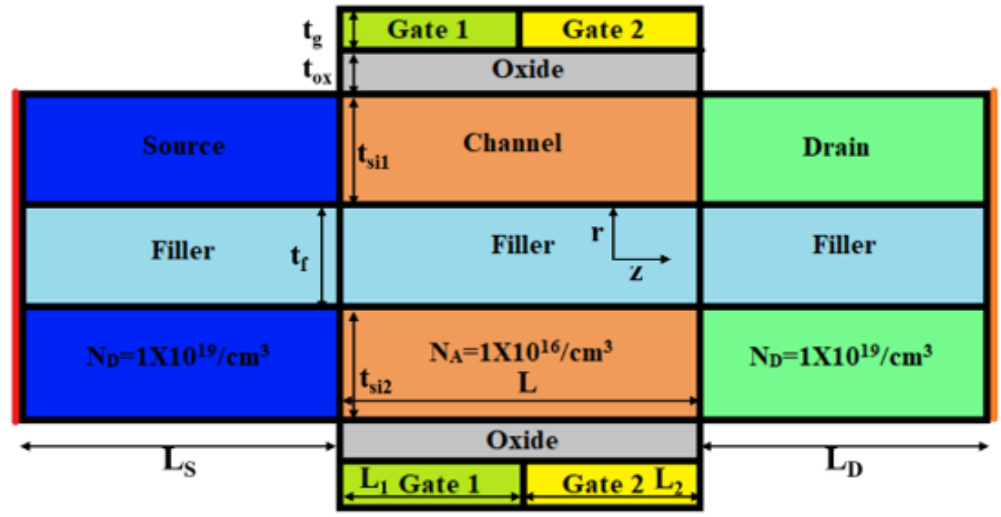


Figure 4.3 Pictorial representation of CIE-EPM FET [42].

The Double Metal Gate Macaroni Nanowire FET (DMGM-NFET) incorporates a dual metal strategy with tailored work functions, resulting in improved digital performance, reduced SCEs, and stronger electrostatic control. Conversely, the Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET) incorporates two metal gates with different work functions, with symmetrical dual oxides having a combination of high-k and low-k dielectrics. This reduces gate leakage while optimizing analog performance, making it ideal for high-

frequency circuits and low-noise amplifiers. The Channel Interface Engineered-Electrostatic Potential, Modulated Field Effect Transistor (CIE-EPM FET) architecture incorporates two metal gates with different work functions to fine-tune threshold voltage and suppress leakage currents. In this, the results are validated by comparing them with the analytical results. As semiconductor devices continue to evolve towards miniaturization and efficiency, the architectural innovations seen in Macaroni Channel Field Effect Transistors, such as dual metal and hetero dielectric designs, represent a critical pathway forward. These architectures extend the benefits of GAA FETs and enable specialized optimizations tailored to the domains.

4.1 Double Metal Gate Macaroni Nanowire FET (DMGM-NFET)

4.1.1 Working Principle and Operating Mechanism

The Double Metal Gate Macaroni Nanowire FET (DMGM-NFET) is an advanced evolution in transistors, combining dual metal gate engineering with the superiority of gate all around (GAA) architecture. This architecture offers a reduction in leakage current, suppression of short channel effects (SCEs), and exceptional control over channel electrostatics [192].

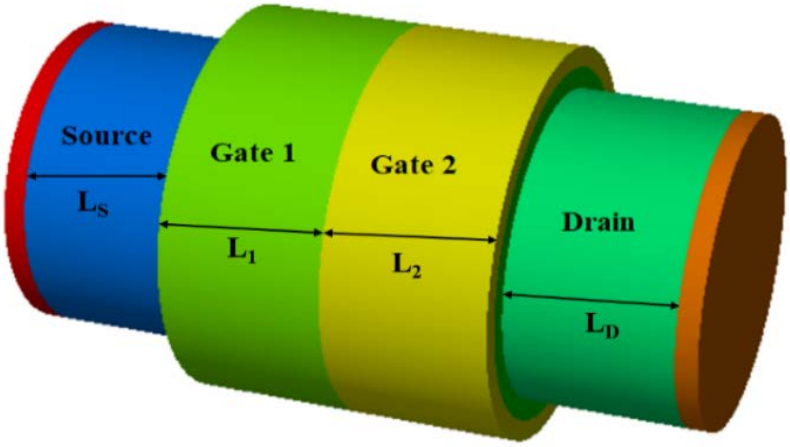
The operating mechanism of the DMGM-NFET can be understood through a combination of quantum mechanical effects and electrostatic modulation inherent to nanoscale devices. Dual Metal Gate induces a step potential because of the difference in the work function of the metal gate. This results in the reduction of electric field penetration from the drain to the source side. Hence, the source to drain tunnelling is reduced, and drain induced barrier lowering (DIBL) is suppressed because the electric field near the drain is uniformly distributed. Leakage current increases as the gate length decreases, and due to the presence of a dual metal gate high potential barrier is provided at the source side, which reduces the subthreshold swing (SS) and reduces the band-to-band tunnelling at the drain side. Subthreshold swing and DIBL are reduced due to the better gate control in the GAA architecture, and also because of the presence of dual metal gates [194]. The GAA architecture ensures maximum gate control over the channel. This ensures uniform distribution of potential between the gate and channel. This helps in electrostatic control and significantly suppresses SCEs.

4.1.2 Device Architecture

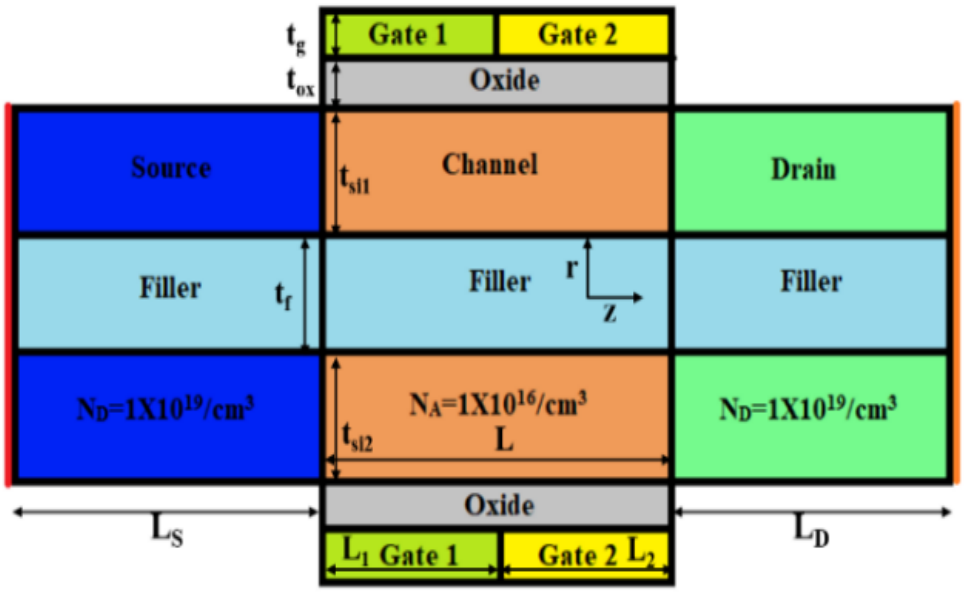
A DMGM-NFET has a dual metal gate having work functions Φ_{m1} = 4.8 eV and Φ_{m2} = 4.4 eV. The proffered DMGM-NFET device is a symmetrical gate structure with gate thickness t_g (= 2 nm) and gate length $L_1 = L_2$ (= 15 nm). A hollow filler with a thickness of t_f (= 5 nm) runs along the channel L (= 30 nm) center of the proffered macaroni FET's cylindrical body. The hollow filler in the proposed macaroni FET is created using a diluted-HF approach [126][125]. The preferred macaroni FET contains Molybdenum metal, having different work functions, which is used to manipulate the nitrogen implant. The metal used as the gate is Molybdenum (Mo), and its work function varies between 4.36 eV - 4.95 eV. The optimum value of 4.4 eV and 4.8 eV is used in DMGM-NFET to enhance the electrostatic control on the channel, which results in the reduction of OFF state leakage and increases the stability of the proffered

device. Schematics of the device under examination are shown in 3-D and 2-D in Figure 4.4 (a) and (b), respectively.

Table 4.1 lists all of the structural parameters. In this manuscript, DMGM-NFET is equated with a traditional nanowire device having a single gate structure (SMG-NFET) and a dual metal gate structure (DMG-NFET) [23][88]. All the device framings are mentioned in detail in Table 4.1. We are integrating an assessment of our proposed design with the empirical data from prior fabrication, as illustrated in Figure 4.5, to substantiate the validity of our simulated outcomes against the results obtained from the actual fabrication process [24][168]. From Figure 4.5, it can be inferred that the simulated outcomes closely resemble the created work.



(a)



(b)

Figure 4.4 (a) 3-D representation of DMGM-NFET, and (b) 2-D representation of DMGM-NFET

TABLE 4.1: ARCHITECTURAL SPECIFICATION OF THE DEVICE

Parameters	SMG-NFET	DMG-NFET	SMGM-NFET	DMGM-NFET
Channel Doping	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$
t_{si1}	5 nm	5 nm	5 nm	5 nm
Channel Length (L)	30 nm	30 nm	30 nm	30 nm
t_{si2}	5 nm	5 nm	5 nm	5 nm
Oxide Thickness (t_{ox})	2 nm	2 nm	2 nm	2 nm
M_S	4.86 eV	4.8 eV	4.72 eV	4.8 eV
Silicon Thickness (t_{si})	10 nm	10 nm	10 nm	10 nm
M_D	--	4.48 eV	--	4.4 eV
Length of S/D	15 nm	15 nm	15 nm	15 nm
L_1	15 nm	15 nm	15 nm	15 nm
Filler Thickness (t_f)	5 nm	5 nm	5 nm	5 nm
L_2	15 nm	15 nm	15 nm	15 nm
Gate Thickness (t_g)	2 nm	2 nm	2 nm	2 nm

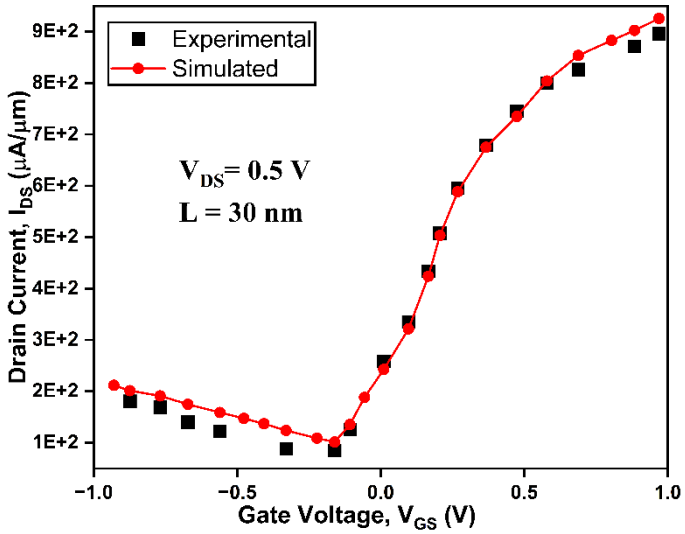


Figure 4.5 Evaluation with experimental work [24].

4.1.3 Simulation Setup

A device simulator for ATLAS 3D Silvaco is used to run numerical simulations [167]. Among the models considered are the Shockley-Read-Hall (SRH) model, the concentration dependent mobility (CONMOB) model, the parallel electric field dependent mobility (FLDMOB) model, the hot electron injection (HEI) model, the Concannon nonlocal gate current (N. CONCAN) model, the band gap narrowing (BBT.STD) model, and the drift diffusion model [168]. In Table 4.2, these models' descriptions are provided. The Newton-Gummel approach is used to solve the carrier transport issue numerically. To incorporate the effects of recombination, it is imperative to utilize the Shockley-Read-Hall (SRH) model. This model is instrumental in simulating leakage currents induced by thermal generation processes. Additionally, it is crucial to account for the presence of interface traps situated at the silicon/oxide junction. For precise simulation, the direct recombination model (AUGER) must also

be activated. The parameters governing these models are modifiable within the MOBILITY statement. For the scenario of velocity saturation induced by the high electric field, the field-dependent mobility model (FLDMOB) should be employed. Alternatively, CONMOB can be utilized to relate the low-field mobility at 300 K to the impurity concentration. Furthermore, the HEI Models are employed to address the tunneling of energetic carriers through insulators, which is significant for phenomena such as gate current and Flash EEPROM programming. The N. CONCAN model is a non-local gate model aligned with the Concannon substrate current model, specifically developed for Flash EEPROM technologies. Choosing the appropriate parameters will automatically activate the Energy Balance Transport Model. The BBT.STD model addresses band-to-band tunneling phenomena and computes the recombination-generation rate based on the local electric field, particularly under conditions of exceptionally high field strengths. The drift-diffusion model, an isothermal framework, necessitates the resolution of three distinct equations about the electron concentration, potential, and hole concentration., Charge transport models or current density equations are derived from approximations and simplifications of the Boltzmann Transport Equation, resulting in a range of models such as the drift-diffusion model, the Energy Balance Transport Model, and the hydrodynamic model. Among these, the Drift-Diffusion Model is distinguished by its simplicity and practicality, operating with a limited set of variables: ψ (electric potential), p (hole density), and n (electron density), thereby obviating the need for additional independent variables [167].

TABLE 4.2: MODELS UTILIZED FOR SIMULATION

Models	Details
SRH	Employed to integrate the impact of carrier recombination phenomena.
Drift Diffusion	Contains Boltzmann statistics.
CONMOB	Employed to address the influence of mobility concentration within MOSFETs.
BBT.STD	Utilized to quantify the influence of tunnelling phenomena on charge carriers.
FLDMOB	Employed to incorporate the effects of velocity saturation into the analysis.
N. CONCAN	Utilized to scrutinize the substrate current.
HEI	Employed to account for the tunnelling carriers that contribute to the gate current.

4.1.4 Results and Discussion

For various device topologies, Figure 4.6 demonstrates the disparity in surface potential with channel orientation. As demonstrated in Figure 4.6, a modification in the metal gate's work function for the DMGM-NFET causes an alteration in surface potential. This abrupt change in surface potential is due to the change in the work function due to the presence of the control gate with Φ_{m2} = 4.4 eV and Φ_{m1} = 4.8 eV. The potential changes as the electron velocity of the charge carrier changes from the source side to the drain [184] side owing to a drop in work function at the drain side to reduce impact ionization [88][195].

The potential contour map of SMG-NFET and DMGM-NFET at V_{GS} = 0.1 V and V_{DS} = 0.2 V is displayed in Figure 4.7. The NW-FET is switched OFF in the absence of any applied gate voltage (V_{GS} = 0.0 V), inhibiting the creation of a conduit for current to flow between the source and drain across the channel and the depletion layer. The depletion layer completely disappears as a result of the gate voltage being applied being higher than the threshold voltage [184][156], forming a conduction route from the source to the drain side. As a result, the NW-FET is switched ON and current flows. The potential contour map of DMGM-NFET shows the rise in the channel area controlled by a second gate (Gate 2) because of the difference in the metal work function and the dual metal gate structure.

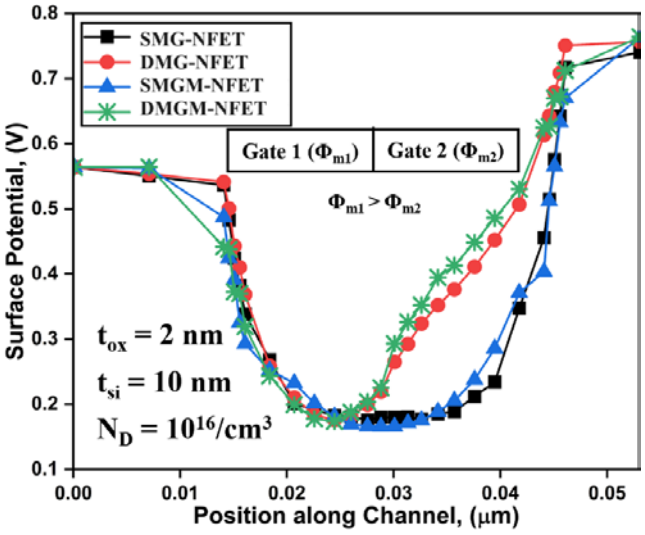


Figure 4.6 Surface Potential of SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET.

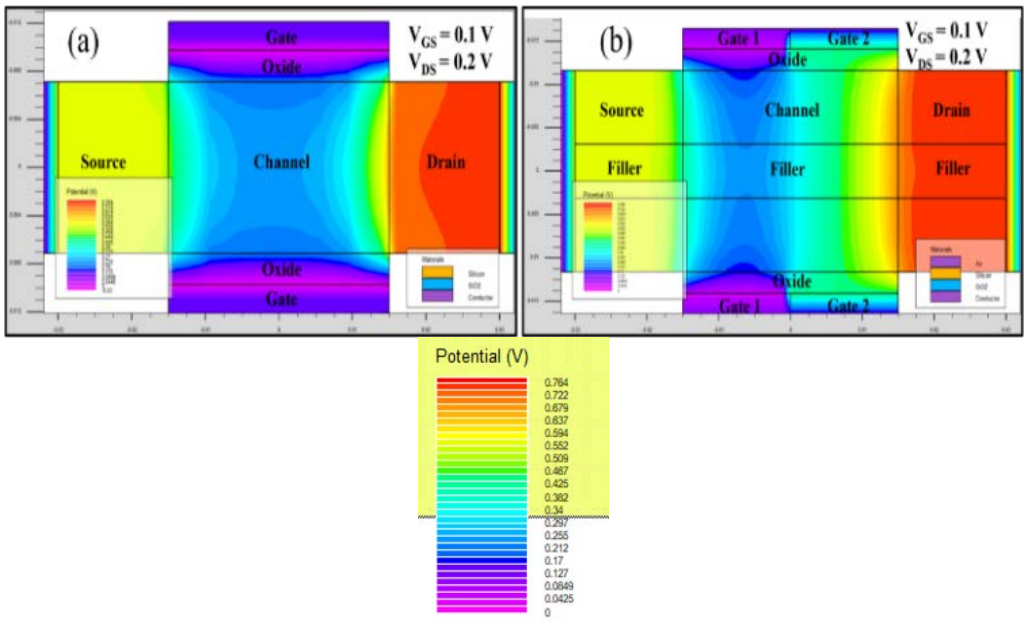


Figure 4.7 Potential contour of (a) SMG-NFET, (b) DMGM-NFET and (c) Scale of Potential contour.

For various SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET, Figure 4.8 illustrates how the electric field varies across the channel. The direction of the potential shift along the channel is controlled by the electric field (E_z), which can be seen in Figure 4.8. The electric field is measured at V_{GS} = 0.1 V and V_{DS} = 0.2 V for all the device configurations. Here, due to low gate voltage, the device is in the OFF state, and no conduction path is generated between the source side and the drain side through the channel [184]. Since the filler in SMGM-NFET and DMGM-NFET is vacuum, the hot carriers are attracted to the filler rather than being trapped by the gate dielectric. This trapping of hot carriers leads to a lowering of the impact ionization effect, which lessens the OFF-state leakages at the drain end.

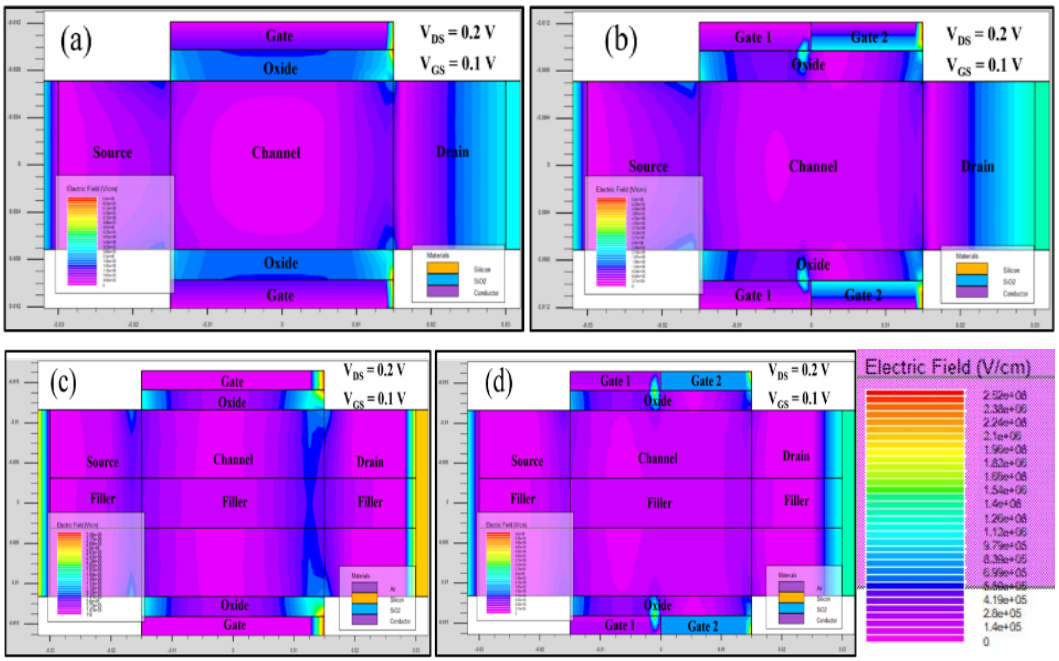


Figure 4.8 Electric Field of (a) SMG-NFET, (b) DMG-NFET, (c) SMGM-NFET, (d) DMGM, and (e) Scale of Electric Field.

The contour plots in Figure 4.9 indicate the hole concentration (/cm^3) at the channel center for V_{GS} = -1.0 V, V_{DS} = 1.0 V for (a) SMG-NFET, (b) DMG-NFET, (c) SMGM-NFET, and (d) DMGM-NFET. As per Figure 4.9 (f), because of the shift in mobility throughout the channel generated by the vacuum filler in the middle, DMGM-NFETs have the lowest hole concentration. Figure 4.9 (f) depicts the relative analytics for the hole concentration for SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET devices under consideration. The graph demonstrates that the DMGM-NFET has the lowest hole concentration, inhibiting band tunnelling and hence GIDL.

To assess the operational efficacy of the device, Band-to-Band Tunneling (BTBT) serves as a critical reliability parameter. The exacerbation of depletion and elevated drain bias results in a pronounced overlap between the valence and conduction bands. This overlap in the OFF state facilitates electron tunneling from the valence band to the conduction band, indicating that BTBT significantly elevates leakage current in the OFF state. Figure 4.10 illustrates the variation in band energy as a function of position along the channel length. It demonstrates the valence band energy (VBE) and

conduction band energy (CBE) of the DMGM-NFET at drain voltages of 1.0 V and 0.0 V, respectively. According to Figure 4.10, there is a decrease in band energy at the drain end for DMGM-NFET [168]. This drop is caused by a decline in the gate material work function near the drain end, as well as the presence of a vacuum filler in the center. As a result, the electron tunnelling from VBE to CBE is reduced, which lowers the BTBT.

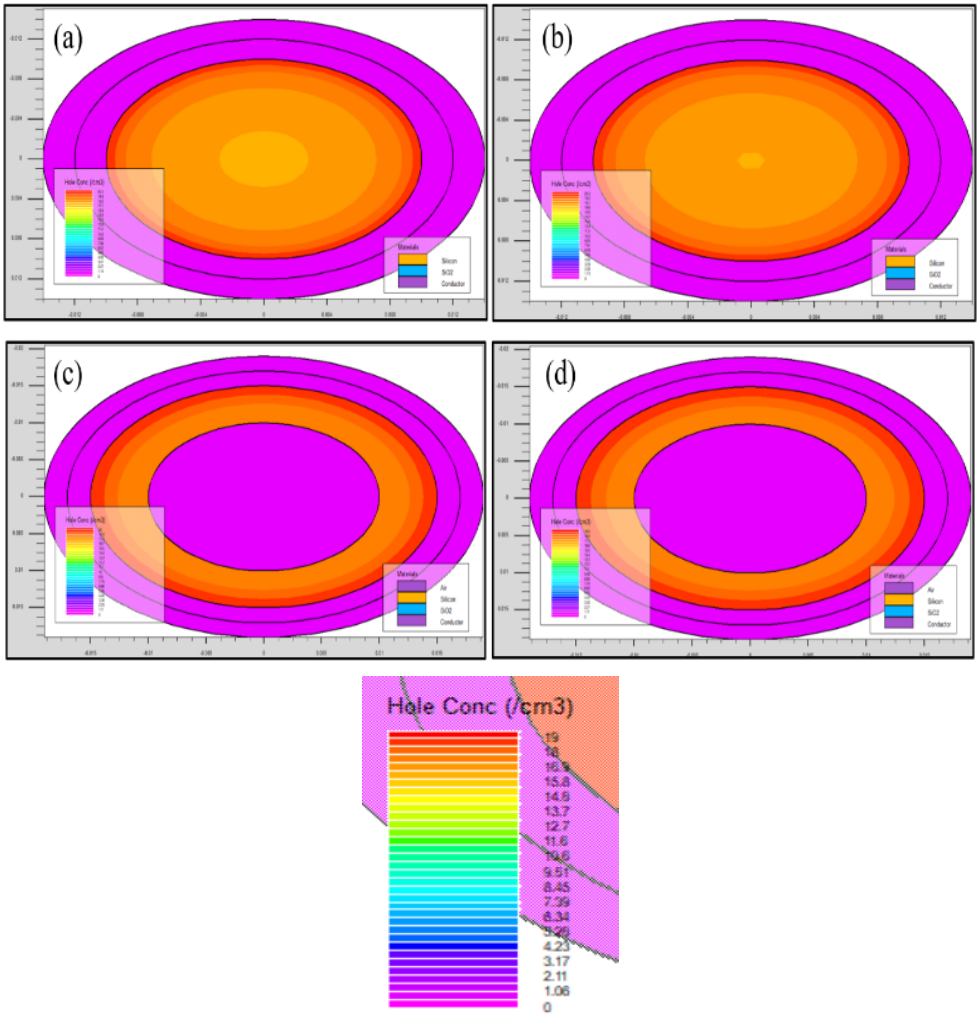
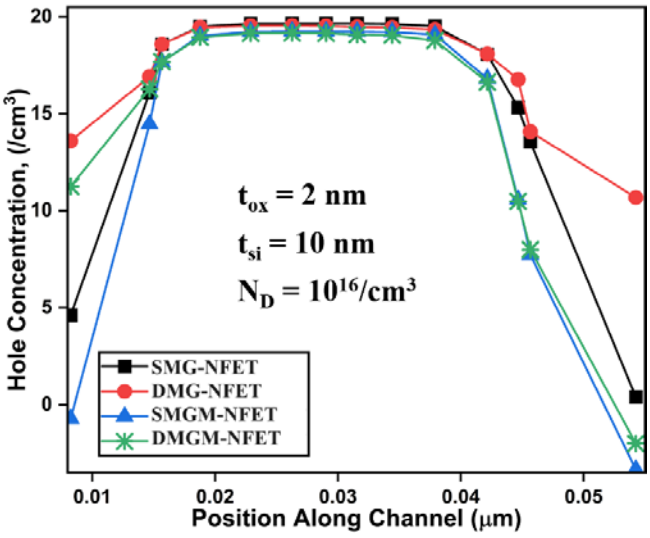


Figure 4.9 Hole Concentration of (a) SMG-NFET, (b) DMG-NFET, (c) SMGM-NFET, (d) DMGM-NFET, (e) Scale of Hole Concentration.

The distance that electrons must traverse between VBE and CBE when V_{DS} is 1.0 V is known as the tunnelling distance. Figure 4.11 depicts the tunnelling distance of all the device topologies studied in this manuscript. The decrease in tunnelling distance of DMG-NFET and DMGM-NFET can be seen in Figure 4.11 because of the difference in the work function of the gates [196]. Among various topologies of FET, DMGM-NFET has having lowest tunnelling distance of 0.0185 µm because of the difference in work function and due to the presence of filler at the center, the hot carrier effect is also reduced. This reduction of the hot carrier effect reduces the BTBT of electrons in DMGM-NFET.



(f)

Figure 4.9 (f) Hole Concentration.

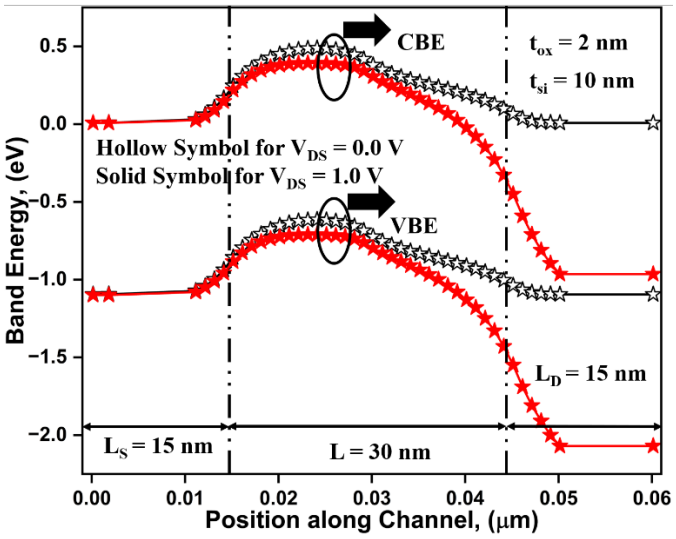


Figure 4.10 Band-to-band Tunneling in DMGM-NFET.

In diverse device topologies, Figure 4.12 depicts how the GIDL current changes with gate voltage [168]. Figure 4.12 makes it abundantly evident that the GIDL current in a DMGM-NFET has decreased from an order of 10^{-10} A to an order of 10^{-11} A. The phenomenon known as GIDL is a subthreshold leakage phenomenon [88]. It happens when the gate voltage towards the source is modest, and the drain is kept at a higher positive bias [168]. To induce a more substantial potential gradient between the drain and the channel, the gate is maintained at a reduced voltage while the drain is elevated to a higher voltage. This potential disparity generates a robust electric field, which facilitates the emission of charge carriers. Consequently, this electric field induces band bending between the gate and the drain, further modulating the device's electrical behavior [23][171]. As the GIDL current traverses, the carriers migrate towards the drain. In the case of the DMGM-NFET, considerable measures are undertaken to

minimize the GIDL current. This attenuation of OFF-state leakage [22] is primarily attributable to a significant diminution in the generation of hot carriers, which is facilitated by the incorporation of a vacuum filler positioned centrally within the device structure. [184]. SMGM-NFET is compared with SMG-NFET; the device shows a 202% improvement, and when DMGM-NFET is compared with SMG-NFET, the device shows a 236% improvement in GIDL current. GIDL current of DMGM-NFET is 117-fold improved when compared with SMGM-NFET.

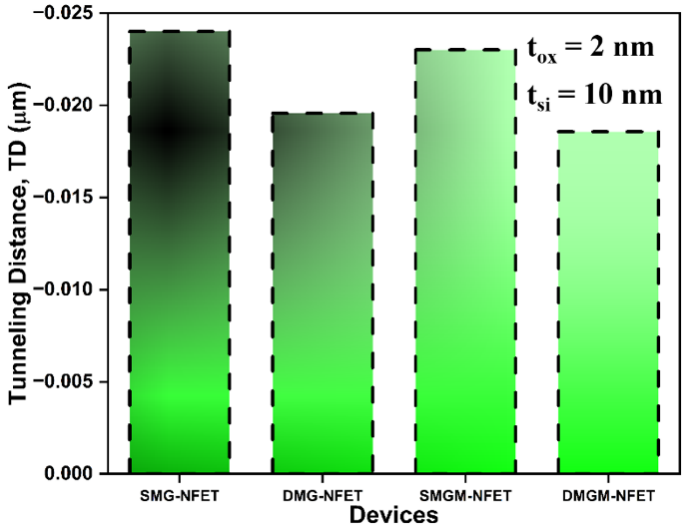


Figure 4.11 Tunneling Distance of different archutectures.

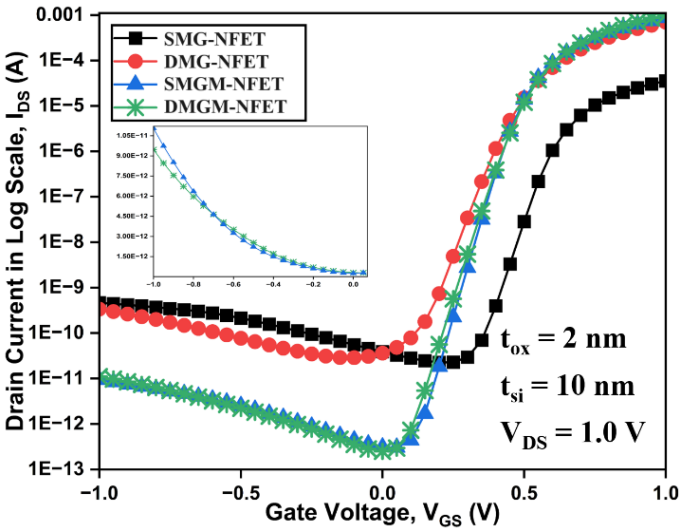


Figure 4.12 GIDL changes along Gate Voltage.

Figure 4.13 depicts the transfer characteristics (I_{DS} v/s V_{GS}) of DMGM-NFET in comparison to SMG-NFET, DMG-NFET, and SMGM-NFET. In this, the characteristics are measured at V_{DS} = 1.0 V for all the devices [168]. From Figure 4.13, we can conclude that transfer characteristics (I_{DS} v/s V_{GS}) of DMGM-NFET are higher as compared to other devices. The presence of dual metal gates helps in having better

control of the gate on the channel, and the vacuum filler at the centre of the device is are important factor affecting the transfer characteristics of DMGM-NFET.

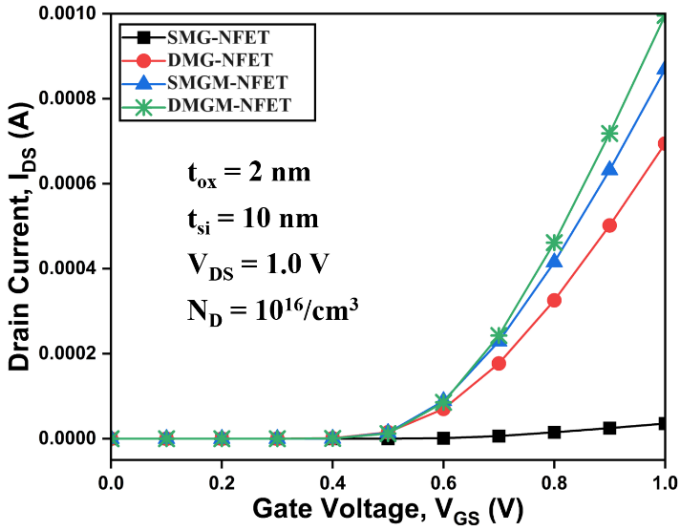


Figure 4.13 Transfer Characteristics along Gate Voltage.

Figure 4.14 shows the output characteristics (I_{DS} v/s V_{DS}) of DMGM-NFET. The output characteristics are measured at V_{GS} = 1.0 V for all the devices. In this manuscript, the output characteristics of DMGM-NFET are higher than compared of other device topologies. The output characteristics of DMGM-NFET are better because of the dual metal gate and vacuum filler at the centre of the device, which helps in reducing the hot electron effect [156].

Figure 4.15 depicts the variation in gate voltage-dependent drain current is referred to as “transconductance”. The mathematical formula for transconductance is as follows [23]:

$$g_m = \left|\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \quad (4.1)$$

The outcomes are evaluated against SMG-NFET, DMG-NFET, and SMGM-NFET in Figure 4.15. Transconductance is vital not just for analog/RF applications, but also for determining the best bias point. The cut-off frequency for every device is minimal at the optimal bias point. The improved current drivability and higher drain current result in a high transconductance value in DMGM-NFET [197].

The fluctuation of output conductance (g_d) with V_{DS} for SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET at V_{GS} = 1.0 V is shown in Figure 4.16. Output conductance (g_d) is defined as the variation in drain current (I_{DS}) in response to alterations in the drain voltage (V_{DS}). The depicted data indicate that the DMGM-NFET exhibits characteristics that align more closely with the ideal performance profile. The DMGM-NFET demonstrates enhanced output conductance and elevated drain current, attributed to the presence of a filler material and the disparity in metal work functions. It can mathematically be described as [197][175]:

$$g_d = \left|\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}} \quad (4.2)$$

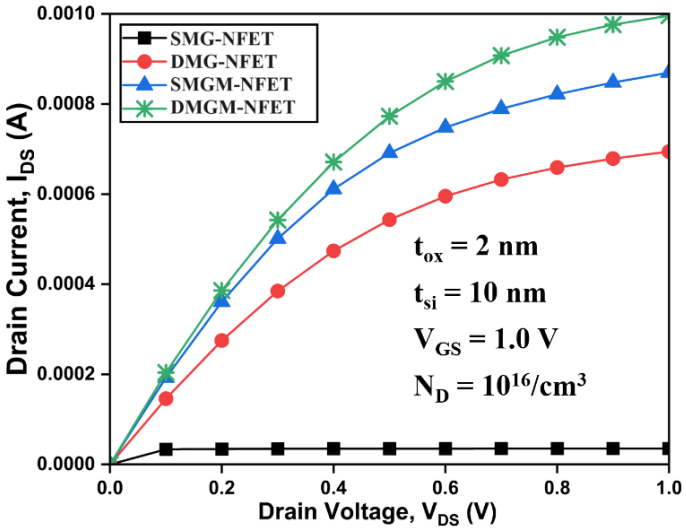


Figure 4.14 Output Characteristics along Drain Voltage.

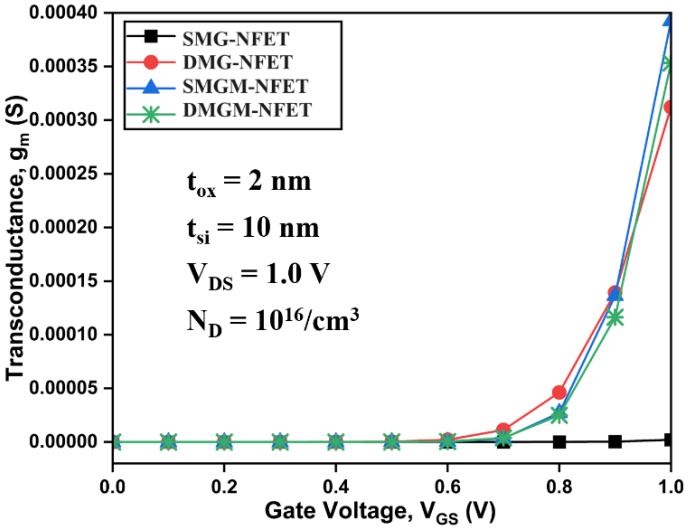


Figure 4.15 Transconductance changes along Gate Voltage.

The subthreshold slope is demonstrated in Figure 4.17 for many device setups. The term "subthreshold slope" describes how quickly a gadget may flip between its OFF and ON states (SS). The SS needs to be closer to 60 mV/decade to quickly transition from the OFF to the ON state [23][168]. Figure 4.17 shows how close to the ideal value the SMG-NFET's subthreshold slope is. A 9.7 mV/decade deviation from ideal exists in the subthreshold slope of the DMGM-NFET. The impact ionization effect significantly diminishes in the DMGM-NFET due to the filler [88], which further improves the switching from the OFF-state to the ON-state and lowers the SS.

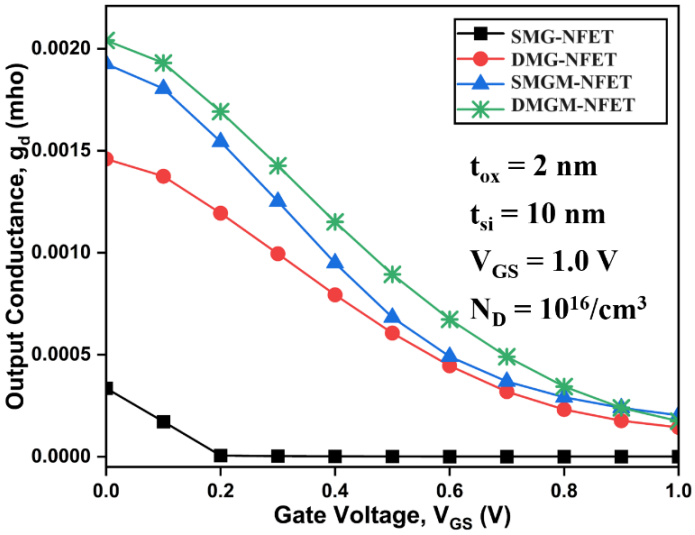


Figure 4.16 Output Conductance changes along Gate Voltage.

Figure 4.18 illustrates the I_{ON}/I_{OFF} for various device topologies. The device's I_{ON}/I_{OFF} ratio, which controls the device's usefulness for digital applications and is a crucial performance characteristic. For the device to operate better digitally, the I_{ON}/I_{OFF} ratio should be as high as is practical. It quantifies the ratio of the ON-state current to the OFF-state current [198]. It is worth noting that the I_{ON}/I_{OFF} ratio for DMGM-NFET is greatest, with a 3109-fold improvement over SMG-NFET, a 233-fold improvement over DMG-NFET, and a 2-fold improvement over SMGM-NFET. Due to the dual metal gate architectures, decreased OFF-state leakages, and enhanced ON-state performance [184] the I_{ON}/I_{OFF} ratio is greater for DMGM-NFET.

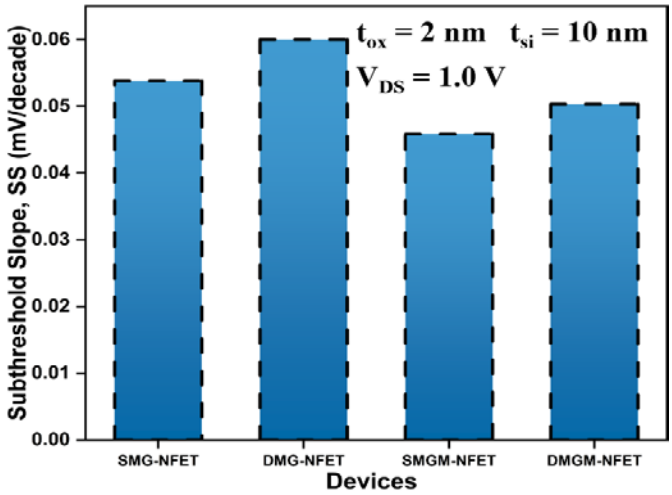


Figure 4.17 Subthreshold Slope for an array of distinct device architectures.

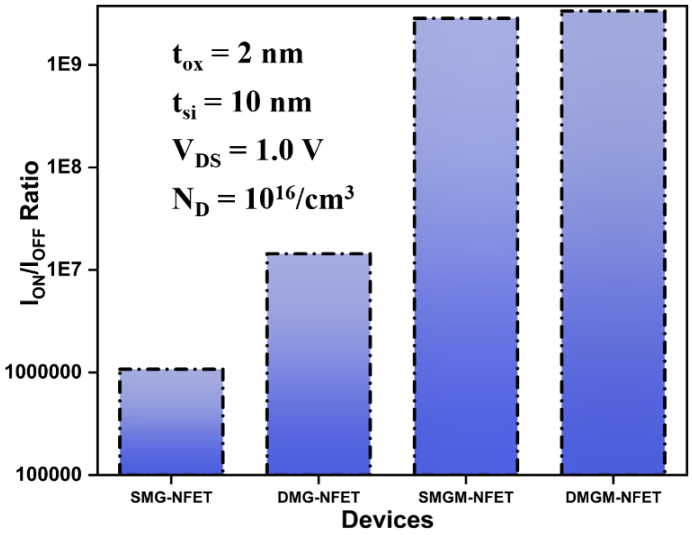


Figure 4.18 I_{ON}/I_{OFF} for various device designs.

Figure 4.19 compares the four distinct topologies, namely SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET, in terms of drain-induced barrier lowering (DIBL) [199]. DIBL is mathematically defined as [197]:

$$\text{DIBL} = \frac{V_{th}(V_{DD}) - V_{th}(V_{DDlow})}{V_{DD} - V_{DDlow}} \tag{4.3}$$

Upon the application of the V_{DS}, DIBL induces a reduction in the threshold voltage (V_{th}). In the case of the SMGM-NFET, the incorporation of a vacuum filler substantially attenuates the electric field in the drain region, thereby mitigating the effects of DIBL and leading to a lower degree of threshold voltage reduction. [156]. This is evident from Figure 4.19 that the DIBL is remarkably reduced in SMGM-NFET as compared to other devices.

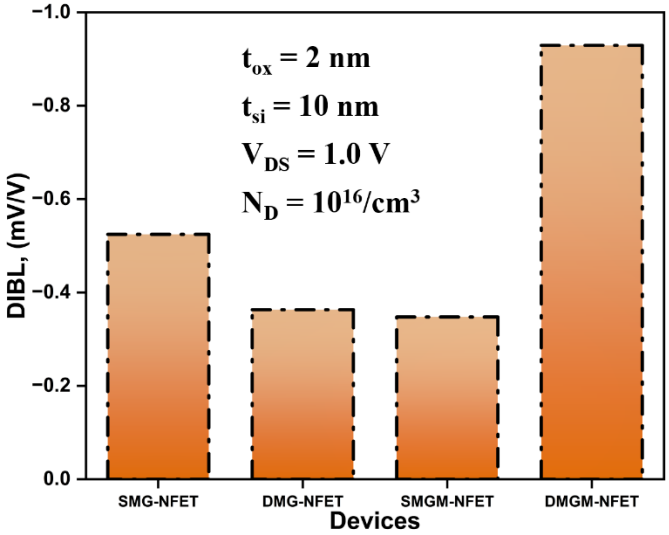


Figure 4.19 DIBL for various device designs.

The fluctuation in transconductance generation efficiency (TGF) is seen in Figure 4.20. The steepness of the subthreshold slope is reflected in the slope of the TGF ratio. TGF is the measure of efficiency of any semiconductor device. TGF should be high while designing any low-power analog circuitry. High TGF has the advantage of allowing circuits to operate with a low supply voltage. TGF may be expressed mathematically as [73]:

$$TGF = \frac{g_m}{I_{DS}} \tag{4.4}$$

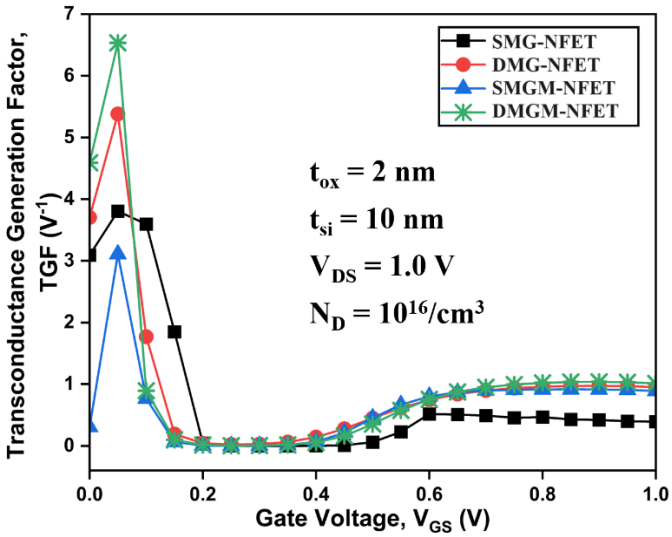


Figure 4.20 Transconductance Generation Efficiency of DMGM-NFET.

Figure 4.21 illustrates the variation in total gate capacitance for different device topologies as a function of the gate-to-source voltage (V_{GS}). The permittivity of a Field-Effect Transistor (FET) exhibits a direct proportionality to its capacitance. Specifically, the total gate capacitance (C_{GG}) of a FET is the aggregate of the gate-to-source capacitance (C_{GS}) and the gate-to-drain capacitance (C_{GD}). [200][201]. Mathematically, C_{GG} can be expressed as [197]:

$$C_{GG} = C_{GS} + C_{GD} \tag{4.5}$$

C_{GG} of a device greatly influences its high-frequency and high-speed functioning. C_{GG} of DMGM-NFET is less than SMG-NFET and SMGM-NFET. As the cut-off frequency is inversely proportional to C_{GG} [184][50] lower C_{GG} would also guide DMGM-NFET functioning at high frequencies.

Figure 4.22 depicts the cut-off frequency (f_T) of DMGM-NFET in comparison to other device topologies. The f_T controls the high-frequency operation of a gadget. To guarantee that the gadget operates at a high frequency, f_T should be sufficiently high. It is directly proportional to g_m and inversely proportional to C_{GG} and can mathematically be expressed as [23][56]:

$$f_T = \frac{g_m}{2\pi C_{GG}} \tag{4.6}$$

Here, DMGM-NFET has a greater f_T, making it more suitable for high-frequency applications compared to SMG-NFET, DMG-NFET, and SMGM-NFET.

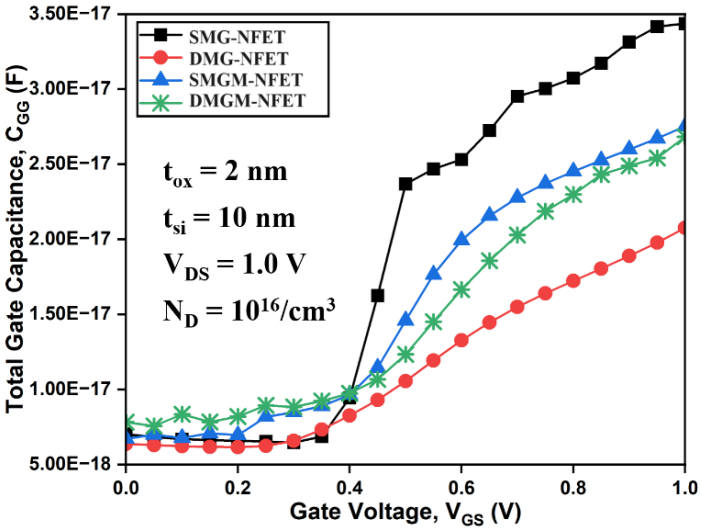


Figure 4.21 Total Gate Capacitance of DMGM-NFET.

For SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET at V_{GS} = 1.0 V, Figure 4.23 illustrates the fluctuation of early voltage (V_{EA}) with V_{DS}. The ratio of the drain current (I_{DS}) to the output conductance is known as the early voltage [198]. It can mathematically be expressed as [202][56]:

$$V_{EA} = \frac{I_{DS}}{g_d} \tag{4.7}$$

DMGM-NFET has been shown to have a greater early voltage. This is caused by the presence of a metal gate with a decreased work function that acts as a screen gate [198] screening hot carriers and enhancing V_{EA}.

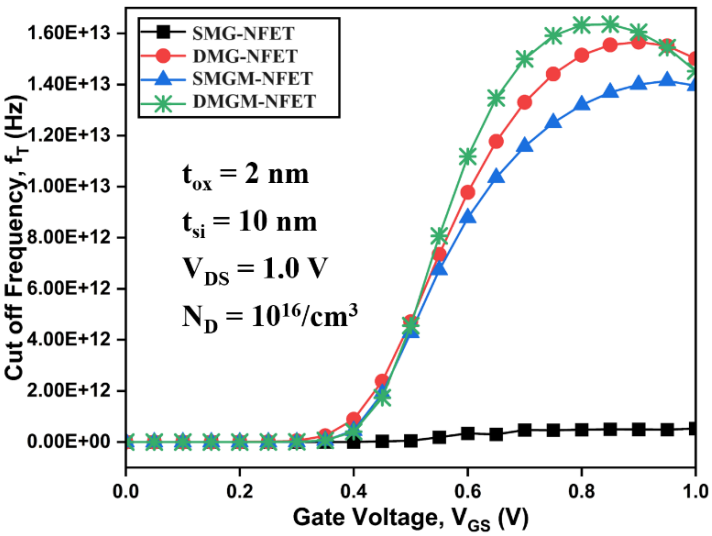


Figure 4.22 Cut-off Frequency of DMGM-NFET.

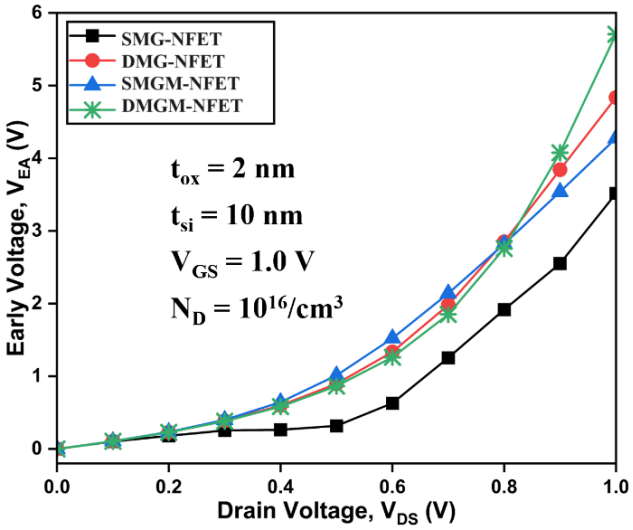


Figure 4.23 Variation in Early Voltage as a function of Drain Voltage.

Intrinsic gain is characterized as the ratio between transconductance and output conductance [73]. It can mathematically be written as [203]:

$$A_v = \frac{g_m}{g_d} \tag{4.8}$$

As the carrier mobility diminishes with increasing gate voltage, a corresponding degradation in gain is observed. Analysis of Figure 4.24 reveals that the intrinsic gain of the DMGM-NFET surpasses that of the SMG-NFET, DMG-NFET, and SMGM-NFET. This enhancement is attributed to the diminished electric field towards the drain region in DMGM-NFETs, a result of the improved gate control over the channel, which in turn augments carrier mobility [168][184]. This lower electric field decreases subthreshold leakages in DMGM-NFET.

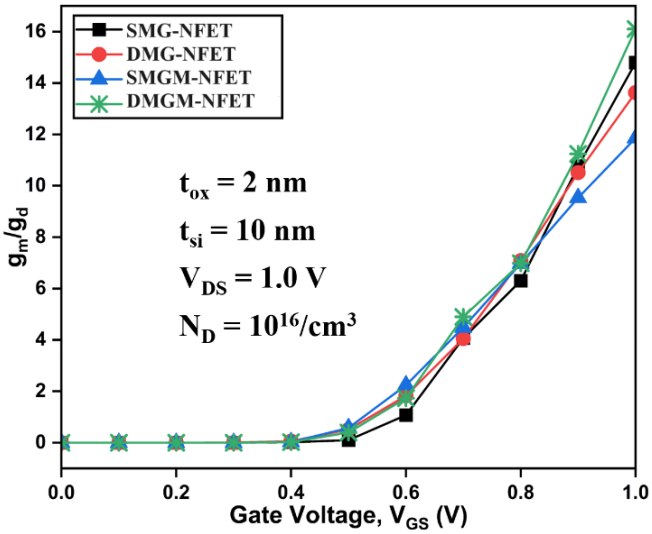


Figure 4.24 Intrinsic Gain changes for various device designs.

The Quality Factor evaluates and measures the devices' switching capacity and qualitative behavior. Q-factor for SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET is shown in Figure 4.25. It is detrimental to evaluating device performance for mixed-signal applications. Mathematically, "Q" can be defined as [73]:

$$Q = \frac{g_m}{SS} \tag{4.9}$$

For the SMG-NFET, DMG-NFET, SMGM-NFET, and DMGM-NFET, the fluctuation of the Channel Resistance (R_{ch}) with V_{GS} is shown in Figure 4.26. R_{ch} directs the current flow in the opposite direction. Enhanced drain currents and superior analog performance are achieved through the reduction of R_{ch}. The DMGM-NFET demonstrates a significantly lower R_{ch} in comparison to the SMG-NFET, DMG-NFET, and SMGM-NFET, as illustrated in Figure 4.26. The incorporation of a dual metal gate structure facilitates improved carrier transport efficiency. Concurrently, the employment of a vacuum filler mitigates impact ionization and tunnelling effects, while concurrently augmenting subthreshold leakage currents. As a result, R_{ch} in DMGM-NFET is lower than in S0MG-NFET, DMG-NFET, and SMGM-NFET.

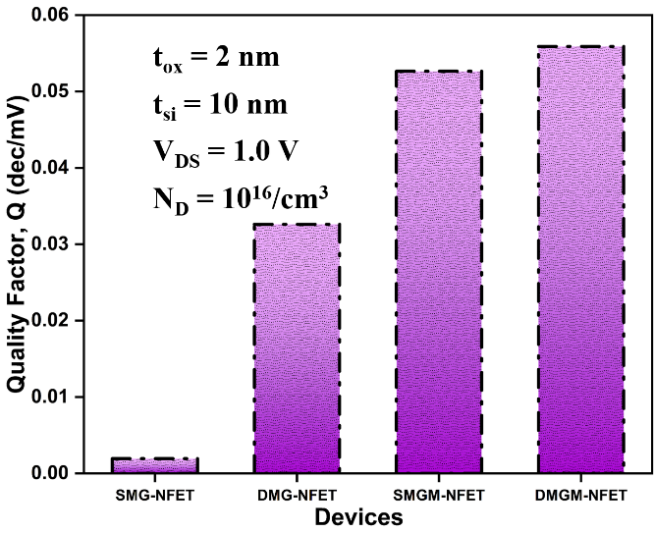


Figure 4.25 Q-Factor for various device designs.

Comparison of the results of the proffered structure of DMGM-NFET with SMG-NFET, DMG-NFET, and SMGM-NFET is discussed in Table 4.3. Table 4.4 comprises the comparisons of DMGM-NFET with the leading-edge devices.

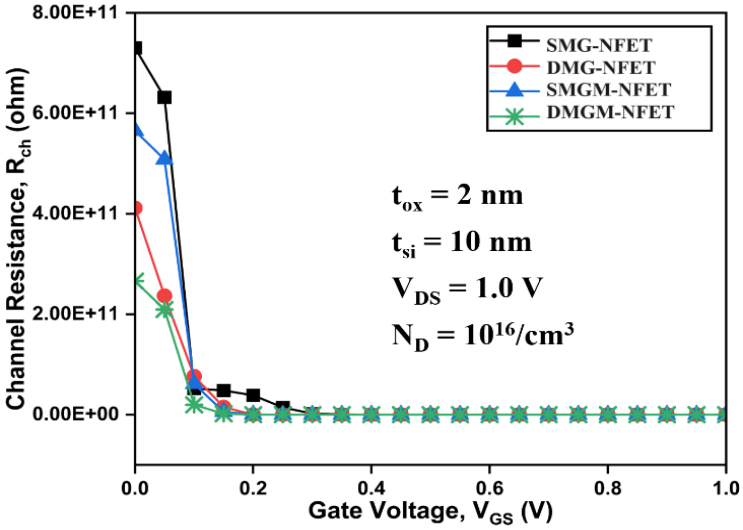


Figure 4.26 Channel Resistance for various device designs.

TABLE 4.3: COMPARISON OF SIMULATED RESULTS

Parameters	SMG-NFET	DMG-NFET	SMGM-NFET	DMGM-NFET
Tunnelling Distance (nm)	24	19.5	23	18.5
Intrinsic Gain at V_{GS} = 1.0 V	1.48E+01	1.36E+01	1.19E+01	1.61E+01
Drain Current (A) at V_{GS} = 1.0 V	3.55E-05	6.94E-04	8.70E-04	9.96E-04
Total Gate Capacitance (F) at V_{GS} = 1.0 V	3.44E-17	2.08E-17	2.75E-17	2.68E-17
Drain Current (A) at V_{DS} = 1.0 V	3.55E-05	6.94E-04	8.70E-04	9.96E-04
GIDL (A) at V_{GS} = -1.0 V	4.69E-10	3.38E-10	1.10E-11	9.46E-12
Hole Concentration (/cm^3) at L = 15 nm	1.96E+01	1.95E+01	1.92E+01	1.92E+01
Transconductance (S) at V_{GS} = 1.0 V	2.15E-06	3.12E-04	3.93E-04	3.53E-04
Subthreshold Slope (mV/decade)	53	60	45	50
Transconductance Generation Factor (/V) at V_{GS} = 0.0 V	3.93E-01	9.50E-01	8.91E-01	1.01E+00
I_{ON}/I_{OFF} ratio	1.08E+06	1.44E+07	2.84E+09	3.35E+09
Output Conductance (mho) at V_{DS} = 1.0 V	7.17E-07	1.44E-04	2.03E-04	1.75E-04
Channel Resistance (W) at V_{GS} = 0.0 V	7.30E+11	4.12E+11	5.65E+11	2.66E+11
Early Voltage at V_{DS} = 1.0 V	3.52E+00	4.84E+00	4.28E+00	5.71E+00
Cut off Frequency (Hz) at V_{GS} = 1.0 V	5.30E+11	1.50E+13	1.40E+13	1.45E+13

TABLE 4.4: COMPARISON OF DMGM-NFET WITH STATE-OF-THE-ART DEVICES

Parameters	NW FET [42]	DMISE GAA MOSFET [183]	DM GAA MOSFET [183]	GAA MOSFET [183]	DMGM-NFET (this work)
Tunnelling Distance (nm)	19.5	13	8	5	18.5
GIDL (A) at V_{GS} = -1.0 V	3.38E-10	3.17E-13	7.31E-11	1.99E-10	9.46E-12
Drain Current (A) at V_{GS} = 1.0 V	6.94E-04	4.91E-04	4.45E-04	4.17E-04	9.96E-04
Drain Current (A) at V_{DS} = 1.0 V	6.94E-04	4.91E-04	4.45E-04	4.17E-04	9.96E-04
Transconductance (S) at V_{GS} = 1.0 V	1.96E-03	1.58E-03	1.20E-03	1.11E-03	3.53E-04
Subthreshold Slope (mV/decade)	60	71.7	75.9	72.9	50
I_{ON}/I_{OFF} ratio	1.44E+07	9.37E+06	3.53E+06	2.36E+06	3.35E+09
Cut off Frequency (Hz) at V_{GS} = 1.0 V	1.50E+13	1.22E+13	9.31E+12	9.03E+12	1.45E+13

4.1.5 Comparative Analysis

On comparing Double Metal Gate Macaroni Nanowire FET (DMGM-NFET) to Conventional Nanowire FET a clear demonstration of superiority was portraited by the DMGM-NFET in terms of electrostatic performance and device reliability. The threshold voltage (V_{th}) control of the DMGM-NFET architecture is better because of the tunability of the effective work functions of the gate metals. This dual metal configuration enables fine adjustment of the surface potential along the channel, ensuring better gate modulation and stable device operation. Furthermore, due to enhanced carrier mobility and optimized electric field distribution, the driver current is higher. The subthreshold swing of the DMGM-NFET architecture is improved indicating stronger gate control and reduced leakage current, making it suitable for low-power and energy efficient applications [192], [204]. Additionally, short channel immunity is significantly better because of the Gate All Around (GAA) engineering due to the geometry of DMGM-NFET, effectively minimizing short channel effects that degrade transistor performance at deep sub-nanometres dimensions.

4.1.6 Challenges and Considerations

Despite its promising characteristics, the DMGM-NFET architecture presents certain fabrication challenges that must be addressed for practical implementation. One of the primary concerns is maintaining precise control over the inner radius of the hollow cylindrical channel, as any deviation in geometry can lead to variations in capacitance and electrical characteristics, impacting overall device uniformity. Another significant challenge involves the alignment of two different metals at the gate, which requires nanometer level precision to prevent interfacial defects or work function irregularities.

Achieving such control demand advanced fabrication techniques such as atomic layer deposition for conformal coating and a selective etching process to define the inner and outer gate region accurately [165]. With the refinement of these nanoscale manufacturing methods the DMGM-NFET can be realized with high reproducibility, paving the way for scalable and high-performance nanowire transistor technologies.

4.2 Channel Interface Engineered-Electrostatic Potential, Modulated Field Effect Transistor (CIE-EPM FET)

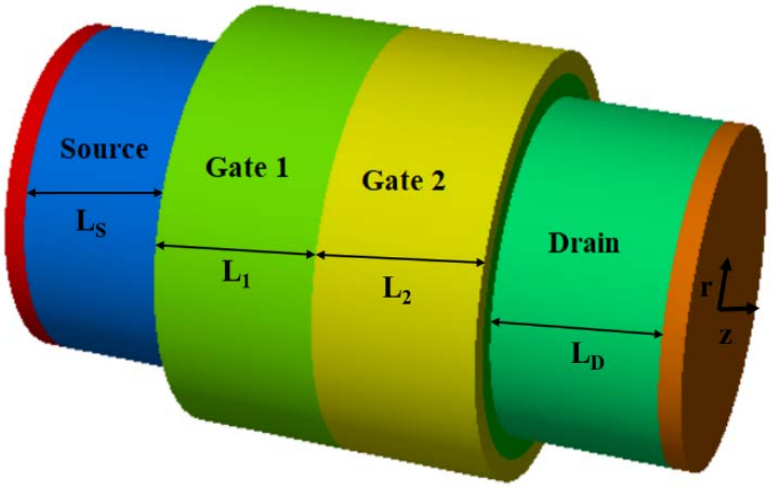
4.2.1 Working Principle and Operating Mechanism

The Channel Interface-Engineered Electrostatic Potential Modulated Field Effect Transistor (CIE-EPM FET) is an advanced evolution in transistors, combining dual metal gate engineering with the superiority of gate all around (GAA) architecture. This architecture offers a reduction in leakage current, suppression of short channel effects (SCEs), and exceptional control over channel electrostatics [165].

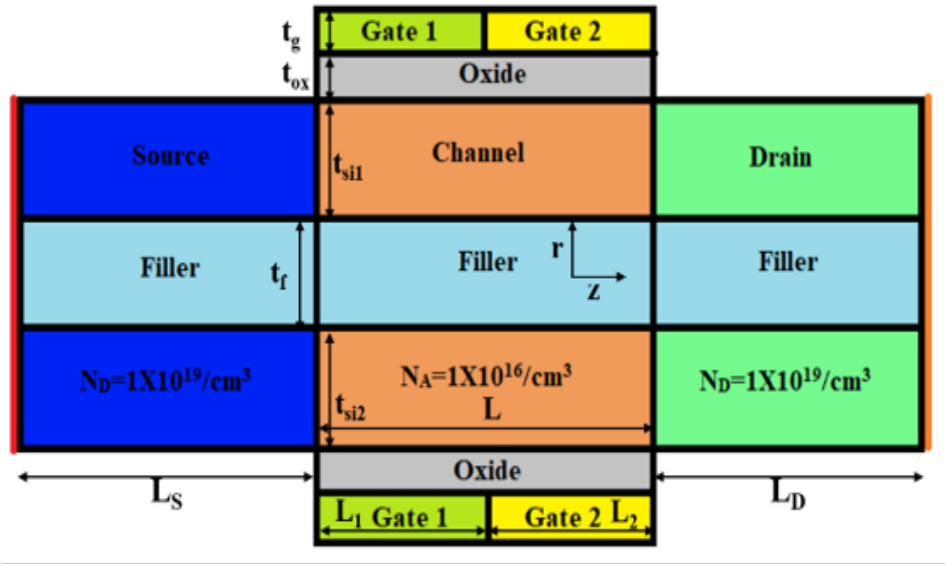
The operating mechanism of the CIE-EPM FET can be understood through a combination of quantum mechanical effects and electrostatic modulation inherent to nanoscale devices. The dual Metal Gate induces a step potential because of the difference in the work function of the metal gate. This results in the reduction of electric field penetration from the drain to the source side. Hence, the source to drain tunnelling is reduced, and drain induced barrier lowering (DIBL) [205], [206] is suppressed because the electric field near the drain is uniformly distributed. Leakage current increases as the gate length decreases, and due to the presence of a dual metal gate high potential barrier is provided at the source side, which reduces the subthreshold swing (SS) and reduces the band-to-band tunnelling at the drain side [207], [208]. The subthreshold swing and DIBL are reduced due to the better gate control in the GAA architecture, and also because of the presence of dual metal gates. The GAA architecture ensures maximum gate control over the channel. This ensures uniform distribution of potential between the gate and channel. This helps in electrostatic control and significantly suppresses SCEs [209], [210].

4.2.2 Device Architecture

Figure 4.27 meticulously illustrates the three-dimensional and two-dimensional Channel Interface-Engineered Electrostatic Potential Modulated Field Effect Transistor (CIE-EPM FET) schematic representation. The proffered architecture embodies a symmetrical dual metal gate framework characterised by a uniform gate thickness t_g (= 2 nm), an oxide thickness t_{ox} (= 2 nm), and silicon thickness t_{si1}=t_{si2} (= 5 nm). Additionally, the device incorporates a filler thickness t_f (= 5 nm), contributing to the transistor's structural integrity and electrostatic control. The channel lengths L_{ch} vary at 30 nm, 40 nm, and 50 nm, providing a spectrum of dimensional configurations to optimise performance across different operational conditions.



(a)



(b)

Figure 4.27 (a) Three-dimensional view of CIE-EPM FET, and (b) Two-dimensional view of CIE-EPM FET.

4.2.3 Simulation Setup

Silvaco ATLAS 3D simulator is utilized for the numerical simulation of the proposed device meticulously [167][211]. The challenge of carrier transport is addressed through the numerical implementation of the Gummel and Newton iterative approaches, ensuring convergence and accuracy in the solution. Table 4.5 contains the simulation models. Quantum mechanical effects are not included as they occur in devices with channel sizes much smaller than 30 nm, and the radius in the 5 nm range [59].

TABLE 4.5: SIMULATION SPECIFICATIONS

Models	Details
SRH	Used to incorporate the carrier recombination effect
CONMOB	Used to account for the effect of MOSFET mobility concentration
FLDMOB	Used to account for the influence of velocity saturation
HEI	Used to include tunnelling carriers that charge the gate current
N. CONCAN	Used to analyse substrate current
BBT.STD	Used to measure the tunnelling impact of charge carriers
Drift Diffusion	Contains Boltzmann statistics

Figure 4.28 encapsulates the evaluation of results derived from prior fabrication endeavours, executed in alignment with the stipulated design parameters [171][212]. A meticulous examination of these findings reveals a striking congruence between the performance metric of the fabricated structure and the projections delineated in the proposed conceptual framework. The simulation process underpinning this investigation was conducted utilizing Silvaco ATLAS 3D software, a robust tool for modelling semiconductor devices. It is noteworthy that, given that the channel length surpasses the 20 nm threshold and the radius resides within the nanometric confines of approximately 5 nm, the influence of quantum mechanical phenomena and ballistic transport effects has been judiciously excluded from the computational model, as their contribution is deemed negligible under these specific dimensional constraints.

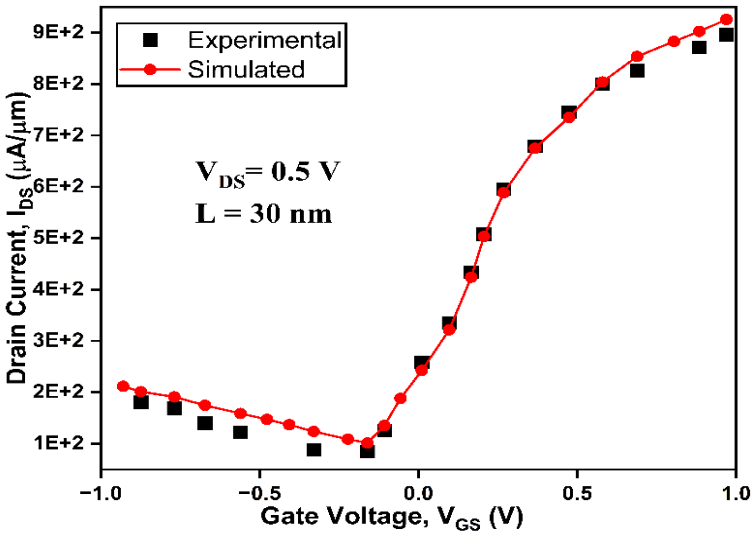


Figure 4.28 Evaluation of calibrated work with experimental work.

4.2.4 Fabrication

Figure 4.29 contains the comprehensively delineated fabrication methodology for the proposed Channel Interface Engineered-Electrostatic Potential Modulated Field Effect Transistor (CIE-EPM FET). A silicon on insulator (SOI) substrate consisting of a dielectric layer between two silicon layers is taken. The top silicon layer undergoes light doping with boron or phosphorus. A nanowire is formed using the VLS method

[86], followed by isotropic etching with dilute HF acid. A sacrificial oxide layer is grown using the low-temperature tetraethyl orthosilicate method. Source and drain terminals are selectively etched, and ion implantation is done to activate the dopants. After the sacrificial layer is removed with HF acid, metal contacts are added, and the gate electrode is formed using lithography and e-beam evaporation.

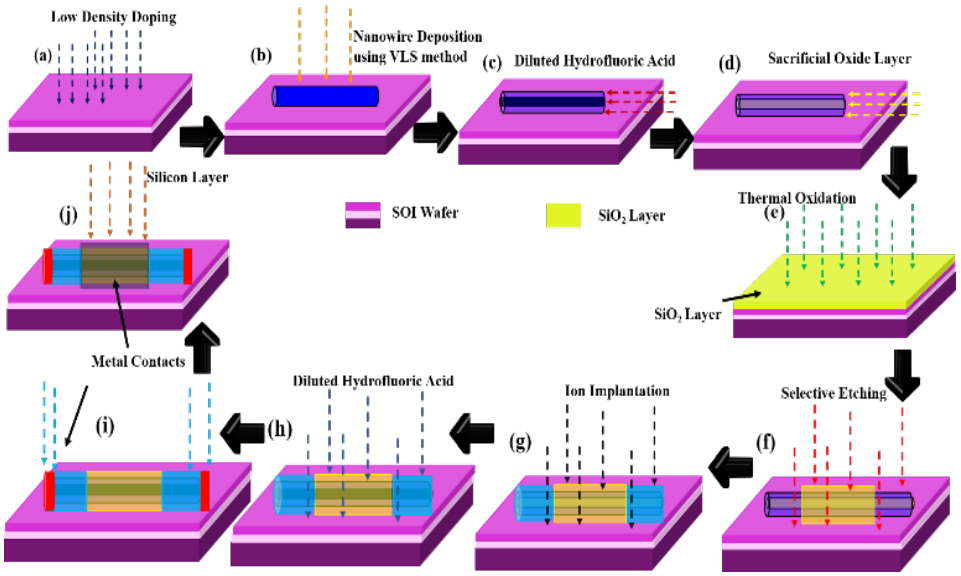


Figure 4.29 Process stages for manufacturing the CIE-EPM FET.

4.2.5 Analytical Modelling

The proffered CIE-EPM FET device can be investigated in detail by using the superposition method for solving two-dimensional Poisson's equation [88][176][86][213]. The 2D Poisson equation is formulated as:

$$\frac{1}{r}\frac{\partial \Psi}{\partial r} + \frac{\partial^2 \Psi}{\partial r^2} + \frac{\partial^2 \Psi}{\partial z^2} = \frac{qN_A}{\varepsilon_{si}} \tag{4.10}$$

Where N_A is the doping concentration in the channel, ε_{si} is the dielectric constant, q is the electron charge and Ψ is the distribution of potential in the silicon film. Using the superposition method, the Poisson equation is used for long channel solution (V(r)), and the short channel solution (U (r, z)) is used for the solution of the 2D Laplace equation as [171][88]:

$$\Psi_i(r, z) = V_i + U_i(r, z) \tag{4.11}$$

Using equation (4.10):

$$\frac{1}{r}\frac{\partial V_i(r)}{\partial r} + \frac{\partial^2 V_i(r)}{\partial r^2} = \frac{qN_A}{\varepsilon_{si}} \tag{4.12}$$

And

$$\frac{1}{r}\frac{\partial U_i(r,z)}{\partial r}+\frac{\partial^2 U_i(r,z)}{\partial r^2}+\frac{\partial^2 U_i(r,z)}{\partial z^2}=0 \quad (4.13)$$

The Boundary Conditions for the potential solutions are:

- The electric potential at the inner surface of silicon remains invariant.

$$\Psi_i\,(r=r_1,\,z)=\Psi_{Ci}\,(z) \quad (4.14)$$

- The electric field at the inner surface of silicon effectively becomes zero.

$$\left.\frac{\partial \Psi_i\,(r,z)}{\partial r}\right|_{r=r_1}=0 \quad (4.15)$$

- Surface potential of silicon film.

$$\Psi_i\,(r,z)|_{r=r_2}=\varphi_S(r_2,z) \quad (4.16)$$

- Electric field at the silicon interface.

$$\left.\frac{\partial \Psi_i\,(r,z)}{\partial r}\right|_{r=r_2}=\check{\jmath}[V_{GS}-V_{FBi}-\Psi_{Ci}(r_2,z)\,] \quad (4.17)$$

Where $\check{\jmath}=\frac{C_{ox}}{\varepsilon_{si}}$, $C_{ox}=\frac{\varepsilon_{ox}}{r_2\ln\left(1+\frac{t_{ox}}{r_2}\right)}$, V_{FBi} is the flat band voltage.

- Potential at the source is

$$\Psi_1\,(r,z)|_{z=0}=V_{Bi} \quad (4.18)$$

- Potential at the drain is

$$\Psi_2\,(r,z)|_{z=L_{1+}L_2}=V_{Bi}+V_{DS} \quad (4.19)$$

- The potential at the two-gate interface is uniform

$$\Psi_1\,(r,L_1)=\Psi 2\,(r,L_2) \quad (4.20)$$

- The electric field at the interface of the gate is uniform

$$\left.\frac{\partial \Psi_1\,(r,z)}{\partial r}\right|_{r=L_1}=\left.\frac{\partial \Psi_2\,(r,z)}{\partial r}\right|_{r=L_2} \quad (4.21)$$

where i=1,2 depending upon the gate of the source side and the drain side. The parabolic solution of equation (4.13) can be:

$$\Psi_{Ci}(r) = P_{0i} + P_{1i}r + P_{2i}r^2 \tag{4.22}$$

Substituting the value of equation (4.22) in equation (4.13), we get

$$P_{0i} = \Psi_I i(r_2, z) - (a^2 - r_1^2)[V_{GS} - V_{FBi} - \Psi_{Ii}(r_2, z)\,] \tag{4.23}$$

$$P_{1i} = -2r_1 P_{2i} \tag{4.24}$$

$$P_{2i} = \frac{\check{3}}{a}[V_{GS} - V_{FBi} - \Psi_{Ii}(r_2, z)\,] \tag{4.25}$$

Solving equation (4.14), we get:

$$\Psi_{I1}(r, z) = \sum_{n=1}^{\infty} J_0(\lambda_S r)\left[Ae^{\lambda_n z} + Be^{-\lambda_n z}\right] \tag{4.26}$$

$$\Psi_{I2}(r, z) = \sum_{n=1}^{\infty} J_1(\lambda_S r)\left[Ce^{\lambda_n z} + De^{-\lambda_n z}\right] \tag{4.27}$$

The electric field across various regions can be calculated as:

$$E_i(r, z) = \frac{d\Psi_i\,(r, z)}{dz} \tag{4.28}$$

Drain current across various regions is expressed as:

$$I_{DS} = \begin{cases} I_{GIDL} \text{ for } -1.0 \le V_{GS} \le 0 \\ I_{SUB} \text{ for } 0 \le V_{GS} \le V_{TH} \\ I_{LIN} \text{ for } V_{TH} \le V_{GS} \le V_{SAT} \\ I_{SAT} \text{ for } V_{SAT} \le V_{GS} \le 0.1V \end{cases} \tag{4.29}$$

Leakage current I_{GIDL} is expressed as:

$$I_{GIDL} = AE_i^2(a, L_1 + L_2)\exp\left(\frac{-B}{E_i(a, L_1 + L_2)}\right) \tag{4.30}$$

here, $A = \frac{q^2 m_r^{0.5}}{18\pi h^2 E_g^{1.5}}$, $B = \frac{\pi m_r^{0.5} E_g^{1.5}}{\sqrt[2]{2}qh}$, $m_r = 0.2m_o$, $a = \frac{t_{si}}{2}$

where h is Planck's constant, E_g is the energy band gap, m_r is the effective mass of the charge carrier, and m_0 is the electron's rest mass.

Subthreshold current I_{SUB} is expressed as:

$$I_{SUB} = \frac{t_{si}\pi\mu kT\eta_i^{\,1-e^{\frac{-V_{DS}}{V_{TH}}}}}{\int_0^L \frac{1}{\int_0^a e^{\frac{\Phi_i(\rho,z)}{kT}}}} \tag{4.31}$$

where μ is the electron mobility and k is the Boltzmann constant.

The expression of the current in the linear region is:

$$I_{LIN} = \frac{2\pi(r_2 - r_1)\mu C_{OX} E_C}{(E_C L + V_{DS})}\left[(V_{GS} - V_{TH})^{\frac{\alpha}{2}} V_{DS} - \frac{\theta_{short} V_{DS}^2}{2}\right] \quad (4.32)$$

The saturation current is articulated as:

$$I_{SAT} = \frac{2\pi(r_2 - r_1)\mu C_{OX}}{\left(1 + \frac{ß}{E_C L}(L - L_{SAT})\right)}\left[\lambda(V_{GS} - V_{TH})^{\frac{\alpha}{2}} V_{DS} - \frac{\theta_{short} V_{DS}^2}{2}\right] \quad (4.33)$$

where $ß = V_{GS} - V_{TH}$, L_{SAT} is characteristic length, E_C is conduction band energy, λ is an empirical coefficient ranging from 0 to 1, $\theta_{short} = \frac{0.1}{\left[\frac{\partial \Psi_{01\,min}}{\partial V_{GS}}\right]}$.

4.2.6 Results and Discussion

4.2.6.1 Comparative Simulation of TNW FET and CIE-EPM FET

Figure 4.30 depicts the GIDL current of CIE-EPM FET and TNW FET at different channel lengths. GIDL represents a notable form of subthreshold leakage, manifesting under conditions where the gate voltage is low while the drain is subjected to heightened positive bias. In this, the field-induced band bending at the gate-drain junction amplifies carrier mobilization, which influences the device's electrical characteristics [176]. In CIE-EPM FET, design interventions are employed to mitigate the GIDL current, thus curbing OFF-state leakage. This structural refinement alleviates the electric field intensity and diminishes the prevalence of leakage pathways, fostering enhanced device reliability and energy efficiency. In the case of a 30 nm channel length CIE-EPM FET, the GIDL is 10^{-11} A, whereas the TNW FET has a GIDL of 10^{-10} A. In the case of 40 nm, the GIDL of CIE-EPM FET is 10^{-12} A, whereas TNW FET has 10^{-11} A. In the case of 50 nm channel length, CIE-EPM FET shows an improvement of 11551% when compared with TNW FET.

Figure 4.31 portrays the transconductance of TNW-FET and CIE-EPM FET at varying V_{GS} at different channel lengths. It is a critical parameter, which is significant not only in analog and RF applications but also in identifying the optimal bias point for device operation. At this ideal bias point, the cut-off frequency for each device is observed to reach a minimal value, signifying maximum stability. Because of the structural advancements in CIE-EPM FET, current conduction is enhanced, and the drain current is elevated, contributing to superior transconductance.

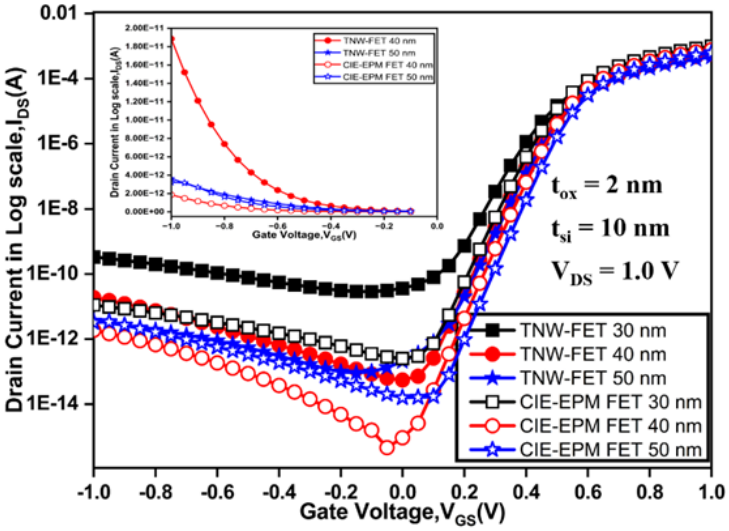


Figure 4.30 GIDL of CIE-EPM FET and TNW-FET along Gate Voltage.

Figure 4.32 illustrates the I_{ON}/I_{OFF} Ratio for TNW FET and CIE-EPM FET at different channel lengths. It is a fundamental parameter dictating the variability and efficacy of a device within digital applications, representing a cornerstone in evaluating performance metrics. This ratio signifies the relationship between the current flowing through the device in its conductive state and the residual leakage current in its non-conductive state. A maximized I_{ON}/I_{OFF} ratio is imperative for enhancing digital functionality. In this, CIE-EPM FET has a 233-fold improvement in the case of 30 nm channel length, whereas in the case of 40 nm, CIE-EPM FET is 38-fold better, and in the case of 50 nm, CIE-EPM FET is 30-fold better than traditional nanowire FET.

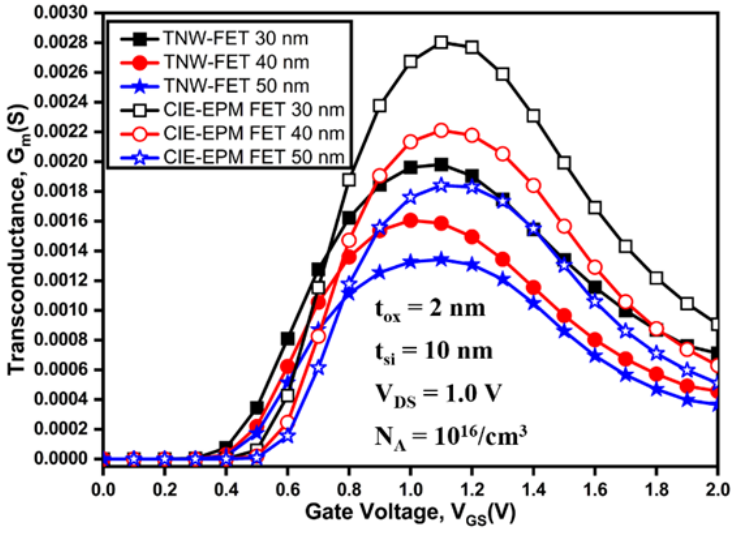


Figure 4.31 Transconductance of TNW-FET and CIE-EPM FET along Gate Voltage.

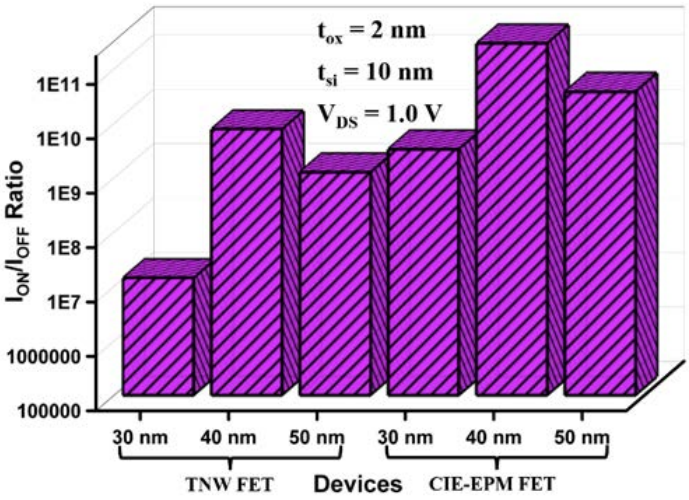


Figure 4.32 I_{ON}/I_{OFF} Ratio for an array of distinct device architectures.

4.2.6.2 Mathematical Validation of CIE-EPM FET

Figure 4.33 describes the simulated GIDL current of CIE-EPM FET juxtaposed with the corresponding analytical findings. A clear correlation between simulated data and mathematical predictions can be seen, affirming their consistency. GIDL for CIE-EPM FET is observed at approximately 10^{-11} A because of the presence of a vacuum filler at the center and dual gate structure for better gate control.

Figure 4.34 showcases the variation in the electric field along the channel direction for CIE-EPM FET. The electric field distribution obtained from the simulation exhibits a strong concordance with the corresponding analytical results. A pronounced discontinuity in the electric field is discernible at the midpoint of the channel length, attributed to the variation in the metal gate work function and vacuum filler.

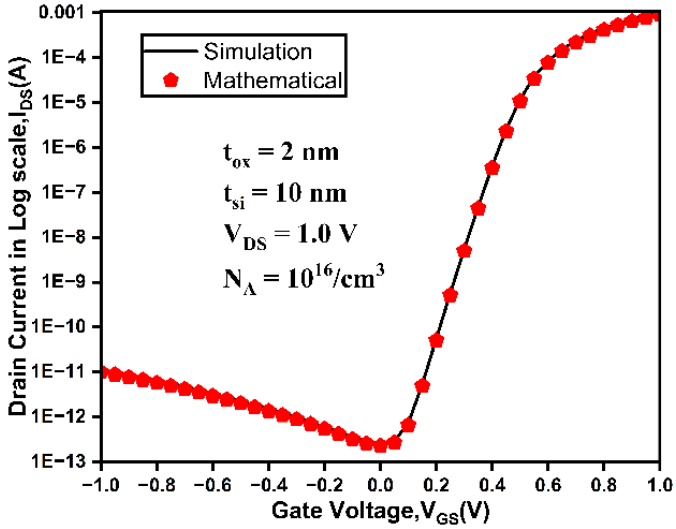


Figure 4.33 GIDL Current of CIE-EPM FET along Gate Voltage.

Figure 4.35 showcases the variation in potential along the direction of the channel. Here, the simulations align closely with the analytical outcomes of the surface potential due to the presence of a vacuum filler, which traps the hot carriers. This combination of vacuum filler and dual metal gate serves to trap the hot carriers and simultaneously provides better control, thereby mitigating electron tunnelling.

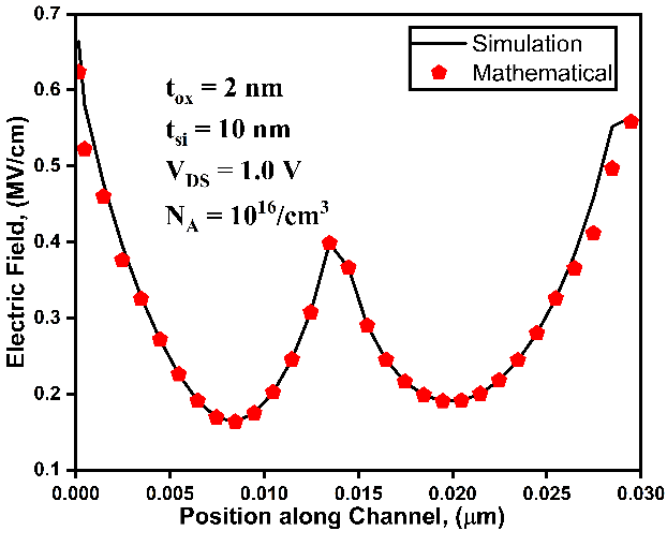


Figure 4.34 Electric Field of CIE-EPM FET along Channel.

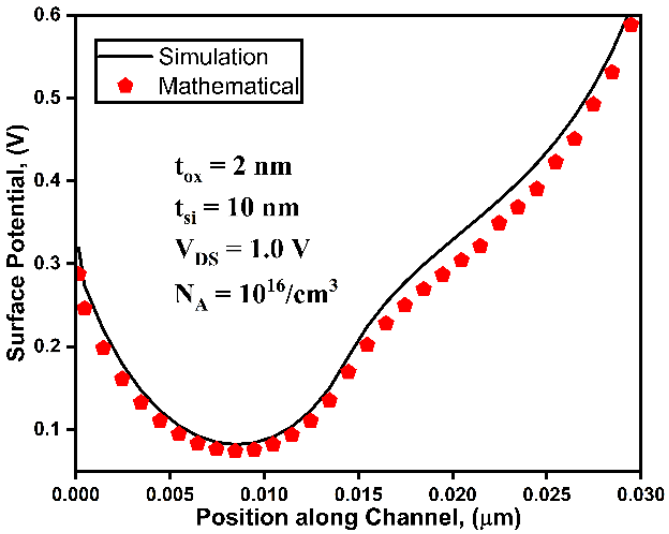


Figure 4.35 Surface Potential of CIE-EPM FET along Channel.

4.2.7 Comparative Analysis

On comparing Channel Interface-Engineered Electrostatic Potential Modulated Field Effect Transistor (CIE-EPM FET) to Conventional Nanowire FET reveals that the proposed device exhibits substantial improvements in overall electrostatic integrity and current driving capability. Short channel immunity is significantly better because of the Gate All Around (GAA) engineering which effectively minimizes drain induced barrier lowering and maintaining strong control over the channel potential even at reduced channel lengths. Furthermore, the incorporation of interface engineered electrostatic

modulation allows for enhanced threshold voltage (V_{th}) control of the CIE-EPM FET architecture enabling precise tuning of the device operation point through optimization of effective work functions of the gate [206]. The subthreshold swing of the CIE-EPM FET architecture is improved, ensuring sharper switching behaviour and lower leakage currents which are essential in making it suitable for low-power applications. In addition the optimized channel potential and smooth electric field distribution contribute to enhanced carrier mobility and optimized electric field distribution, the driver current is higher. This results in improved transconductance and better performance in both digital and analog regime. Collectively, these attributes demonstrate that the CIE-EPM FET architecture outperforms the conventional nanowire FETs in terms of energy efficiency, electrostatic control and scalability.

4.2.8 Challenges and Considerations

Despite its promising characteristics, the CIE-EPM FET architecture presents certain fabrication challenges that must be addressed for practical implementation. One of the primary concerns is maintaining precise control over the inner radius of the hollow cylindrical channel, as any deviation in geometry can lead to variations in capacitance and electrical characteristics, impacting overall device uniformity. Another significant challenge involves the alignment of two different metals at the gate, which requires nanometer level precision to prevent interfacial defects or work function irregularities [214]. Achieving such control demand advanced fabrication techniques such as atomic layer deposition for conformal coating and a selective etching process to define the inner and outer gate region accurately. With the refinement of these nanoscale manufacturing methods the CIE-EPM FET can be realized with high reproducibility, paving the way for scalable and high-performance nanowire transistor technologies.

4.3 Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET)

4.3.1 Working Principle and Operating Mechanism

The Hetero Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET) is an innovative architectural advancement in the domain of nanoscale transistors, particularly in the case of Gate All Around (GAA) FETs. In this, a cylindrical nanowire is taken with a hollow center, and a symmetrical hetero dielectric is taken, which will provide an upper hand in controlling the SCEs and improving the gate leakages.

The operating principle of the device is similar to the traditional FET in terms of charge transport, but because of the structural modifications, the electrostatics are enhanced. The GAA structure ensures full control of the gate on the channel region, hence controlling the charge carriers. Gate control ensures the depletion and accumulation of charge carriers in the channel region, hence helps in minimizing the gate leakage and steeper subthreshold swing [215], [216]. The presence of a hollow macaroni core helps in reducing the hot carriers and allows sharper transitions between ON and OFF states, thereby optimizing cutoff frequency and transconductance. The presence of a hetero

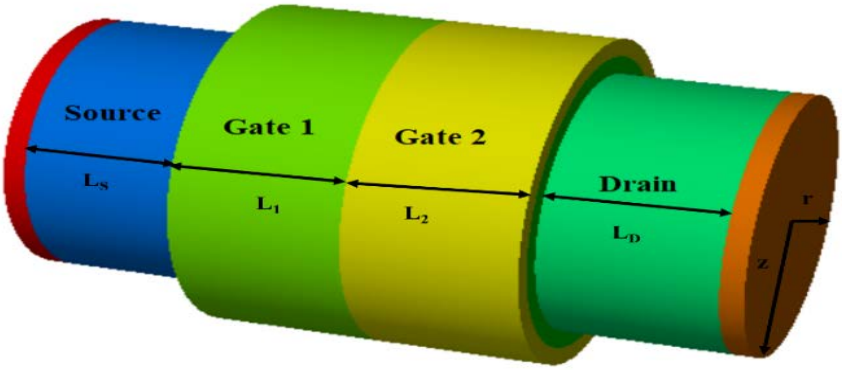
dielectric increases the effective gate capacitance without proportionally increasing the gate leakages.

4.3.2 Device Architecture

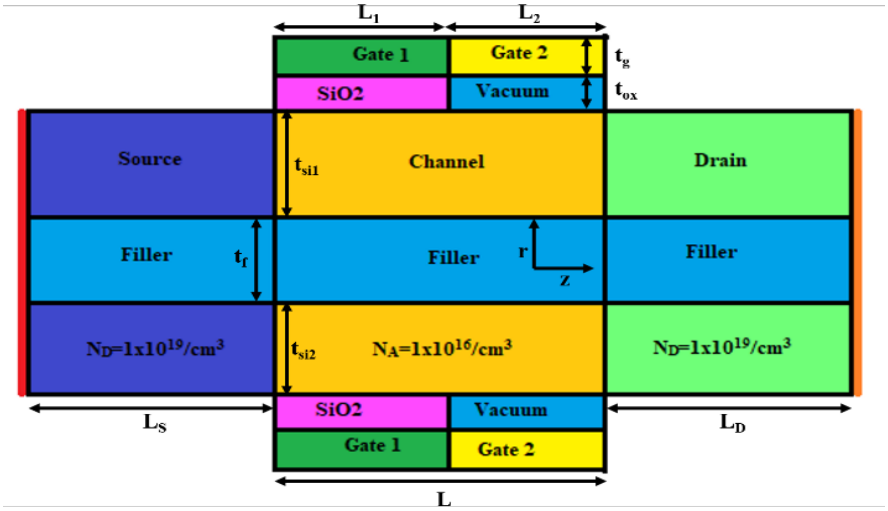
3-D schematic of the HD-MC CGAA FET is presented in Figure 4.36 (a), and Figure 4.33 (b) represents its 2-D cross-sectional schematics. As illustrated in Figure 4.36 (b), the HD-MC CGAA FET has a symmetrical dual metal gate with gate length $L_1 = L_2 =$ 15 nm (total gate length, L = 30 nm) and a symmetrical dielectric oxide layer, which consists of silicon dioxide on the source and vacuum at the drain. We used diluted hydrofluoric acid (HF) to remove the buried oxide from underneath the silicon nanowire channel after patterning it, resulting in a suspended nanowire structure. A conformal sacrificial oxide layer was then created using a low-temperature tetraethyl orthosilicate method. After this, we patterned and deposited polysilicon, implanted source/drain elements, and activated the device [217]. The sacrificial oxide layer was then removed with precision using diluted HF. A vacuum ambient of less than $<10^{-6}$ Torr was maintained throughout the research. The sacrificial oxide layer's thickness, which could be precisely regulated using well-established chemical vapour deposition techniques, was what dictated the thickness of the vacuum gate dielectric [218] [88]. With the aid of gate engineering, dual metal gates are utilized in this, and by manipulating the nitrogen implant, it is possible to modify the work function of these gates. Molybdenum is the gate material utilized in this (Mo). Dielectric engineering has been performed with the silicon dioxide ($\varepsilon_0 = 3.9$) at the source side and vacuum ($\varepsilon_0 = 1$) at the drain side. The thickness of the gate is $t_g = 2$ nm, and the oxide thickness is $t_{ox} = 2$ nm. The macaroni channel structure consists of a vacuum/air filler at the centre with a thickness $t_f = 5$ nm. The short channel effects in the nanowire can either be reduced by reducing the gate oxide's thickness or modifying the silicon's thickness by lowering the outer ($r_2 = t_{si}$) or raising the inner ($r_1 = t_f$) radius [80]. The "macaroni structure" has gained popularity due to its capacity to demonstrate the "macaroni body effect," which helps to lessen oscillations in the threshold voltage. Therefore, it is advised to favour a lower r_2/r_1 ratio while taking into account moderate values for both r_1 and r_2, to guarantee that there are enough mobile charges in the channel [122]. According to the proposed macaroni structure (HD-MC CGAA FET), the r_2/r_1 ratio is 5 nm, which is moderately low and will help in reducing oscillations in the threshold voltage. Total silicon substrate thickness ($t_{si} = t_{si1} + t_{si2}$) of HD-MC CGAA FET is $t_{si1} = t_{si2} = 5$ nm.

Table 4.6 includes the structural layers, viz, details of the materials with their respective properties used for the simulation in ATLAS Silvaco TCAD [219]. Impact ionization happens when energetic electrons clash with silicon atoms close to the drain area while being given kinetic energy by the channel electric field. Electron-hole pairs are produced during this impact ionization process. Most of the electrons that are produced as a result of the holes are added to the drain current at the substrate terminal. A small percentage of extremely energetic electrons, nevertheless, are capable of overcoming SiO_2's energy barrier. These carriers move over the Si and SiO_2 interface and/or the SiO_2 layer, breaking atomic bonds as they go. This causes interface traps and bulk oxide traps to form. These trapped electrons create a positive change in the threshold voltage (V_{th}). Devices operating in a radiative environment might suffer from ionizing stress, similar to hot-carrier effects. The nuclear industry, radiation therapy,

biomedical imaging, and space applications can all benefit from the use of radiation immune technologies [218].



(a)



(b)

Figure 4.36 (a) 3-D schematics of HD-MC CGAA FET, (b) 2-D schematics of HD-MC CGAA FET

To validate our work, we are adding the calibration of our design with previously fabricated work [24] in Figure 4.37. The calibrations done in this manuscript are dependent on the experimental work done in [24], and there is no experimental work done concerning the temperature variation. The findings of the simulated work are quite similar to the earlier manufactured work, as shown by Figure 4.37 [24]. Table 4.7 includes a summary of the device parameters for NW-FET (conventional Nanowire FET), DM-HD CGAA FET (Dual Metal Hetero-Dielectric Cylindrical Gate All Around FET), and HD-MC CGAA FET (Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around FET) [88]. The disadvantage of this design is that its fabrication is costly and complicated. The fabrication difficulties for using vacuum dielectric are that precise temperature is difficult to achieve and maintain, specific doping concentrations are difficult to insert, and fabrication equipment is expensive.

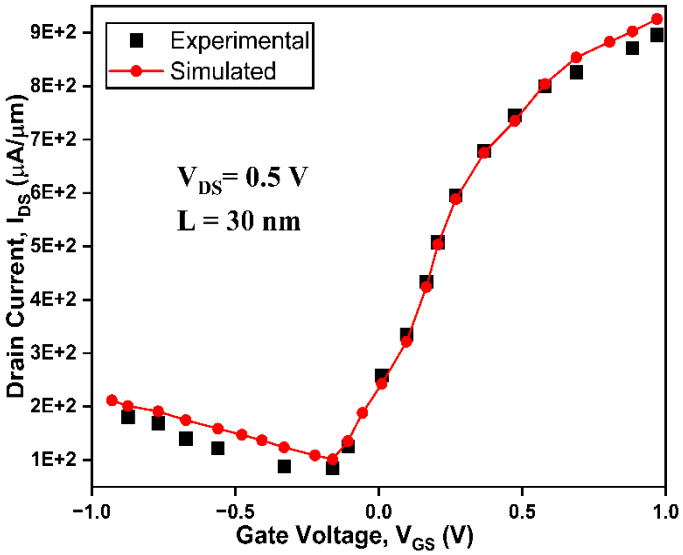


Figure 4.37 Calibration with experimental work [24]

Random dopant fluctuation (RDF) is caused by changes in the relative number of implanted impurities, which contributes to process irregularities and also by variation at the atomic level [127]. As per [127] in macaroni devices, RDF plays a non-negligible role. Also, as per [220] [221] [222] RDF have a limited effect on nanowire implementation.

TABLE 4.6: PHYSICAL PROPERTIES OF MATERIAL STRUCTURE

Structure Layer	Material	Properties
Gate	Molybdenum	Used because by manipulating the nitrogen implant, it is possible to modify the work function and, in turn, can effectively control the channel.
Oxide	Silicon Dioxide	Used because of its electrical and thermal stability at the interface
	Vacuum/Air	Used as it helps in trapping hot carriers; hence, it is useful for reducing gate leakages.
Substrate	Silicon	Used because of its thermal stability, and it is readily available.

TABLE 4.7: STRUCTURAL CHARACTERISTICS OF THE DEVICE

Parameters	NW FET	DM-HD CGAA FET	HD-MC CGAA FET
Channel Length (L)	30 nm	30 nm	30 nm
Channel Doping	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$
Oxide Thickness (t_{ox})	2 nm	2 nm	2 nm
Silicon Thickness (t_{si})	10 nm	10 nm	10 nm
Length of S/D	15 nm	15 nm	15 nm
Filler Thickness (t_f)	5 nm	5 nm	5 nm

Gate Thickness (t_g)	2 nm	2 nm	2 nm
t_{si1}	5 nm	5 nm	5 nm
t_{si2}	5 nm	5 nm	5 nm
L_1	15 nm	15 nm	15 nm
L_2	15 nm	15 nm	15 nm
M_S	4.8 eV	4.8 eV	4.8 eV
M_D	4.48 eV	4.56 eV	4.48 eV

4.3.3 Simulation Setup

Numerical simulations are performed with the aid of an ATLAS 3D device simulator (ATLAS 2019). Several models are employed, including the Shockley-Read-Hall (SRH) model, the concentration-dependent mobility (CONMOB) model, the parallel electric field-dependent mobility (FLDMOB) model, the hot electron injection (HEI) model, the Concannon nonlocal gate current (N. CONCAN) model, the band gap narrowing (BBT.STD) model, and the drift diffusion models [156] [168]. The syntax of Band to Band Tunnelling (BTBT) BBT.STD model has been used for an accurate study and implementation of our proposed device (HD-MC CGAA FET) close to the fabricated devices, studying GIDL [24] [22] [224] [88] (ATLAS 2019). Narration of these models is given in Table 4.8. The carrier transport problem is numerically solved using the Newton-Gummel technique [156].

TABLE 4.8: MODELS EMPLOYED FOR SIMULATION

Models	Details
SRH	Used to incorporate the carrier recombination effect
CONMOB	Used to account for the effect of MOSFET mobility concentration
FLDMOB	Used to account for the influence of velocity saturation
HEI	Used to include tunnelling carriers that charge the gate current
N. CONCAN	Used to analyse substrate current
BBT.STD	Used to measure the tunnelling impact of charge carriers
Drift Diffusion	Contains Boltzmann statistics

4.3.4 Results and Discussion

For HD-MC CGAA FET, DM-HD CGAA FET, and NW-FET with V_{DS} = 1.0 V, the fluctuation in band energy with a change in location along the length of the channel is depicted in Figure 4.38. A drop in band energy can be deduced at the drain end from Figure 4.38. This drop in band energy is primarily caused by the vacuum used as gate dielectric at the drain side of the FET, which significantly diminishes electron tunnelling from the valence band to the conduction band [23]. Hence, because of this movement of electrons from the valence band to the conduction band being truncated, which results in lowering the band-to-band tunnelling.

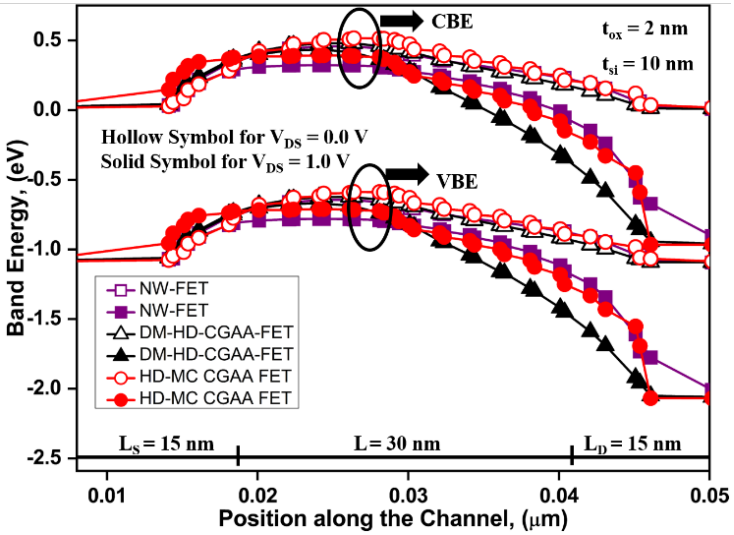


Figure 4.38 Band energy changes along the channel.

The distance covered by electrons while moving from VBE (Valence Band Energy) to CBE (Conduction Band Energy) at V_{DS} = 1.0 V is known as the Tunnelling Distance of the device. Tunnelling Distance for HD-MC CGAA FET, DM-HD CGAA FET, and NW-FET with V_{DS} = 1.0 V and channel length, L = 30 nm, is illustrated in Figure 4.39. Our work is focusing on the reduction of gate leakages, in particular Gate Induced Drain Leakages (GIDL), and we have also calibrated with the fabricated work of (Fan et al. 2015) to give it a realistic stance. GIDL is a subthreshold leakage phenomenon generated by BTBT. It occurs when the gate voltage (V_{GS}) is reduced, and the drain is biased more positively. The emitted carriers travel to the drain end as GIDL current [168]. BTBT (Band-to-Band Tunnelling) is an important reliability metric for evaluating device performance. As the depletion zone deepens and the drain bias increases, the valence and conduction bands overlap significantly. In the OFF-state, the bands' overlap leads electrons to tunnel from the valence to the conduction band. In practice, the BTBT phenomenon causes a considerable increase in leakage current during the OFF-state, which results in significant static power loss [88] [224]. From Figure 4.36, it is evident that the tunnelling distance of HD-MC CGAA FET is less than DM-HD CGAA FET and NW-FET. There are two reasons for the decrease in band energy at the drain end. First of all, it results from the gate's metalwork function degrading as it gets closer to the drain end. Second, it is impacted by the existence of a vacuum gate dielectric at the drain end [175]. Even in the fabricated/experimental work of [24] BTBT model has been used.

For the HD-MC CGAA FET, DM-HD CGAA FET, and NW-FET at V_{DS} = 0.2 V, Figure 4.40 presents the Surface Potential contours. The CGAA FET is in the OFF state because of the absence of V_{GS}. Due to the lack of a conduction path between the source and drain sides via the channel, no current or electron conduction will occur. Hence, in the contour of surface potential, we can see that the drain side has the highest value of surface potential, followed by the source side, and the channel has the lowest surface potential.

Figure 4.41 depicts the variation of surface potential at V_{DS} = 0.2 V and V_{GS} = 0.1 V with the position of the channel for HD-MC CGAA FET, DM-HD CGAA FET, and NW-FET. The change in the work function of the metal gate, as shown in Figure 4.41,

affects the surface potential at L = 15 nm. The work function of the metal gate at the source side is Φ_{m1} = 4.8 eV, and the drain side is Φ_{m2} = 4.48 eV in the HD-MC CGAA FET device. From Figure 4.29, it can be concluded that the surface potential of the HD-MC CGAA FET device is lowest because of the presence of vacuum filler at the center of the channel. The vacuum filler and the vacuum oxide help in trapping the hot carrier injection, which significantly diminishes electron tunnelling from the valence band to the conduction band. This diminished tunnelling of electrons leads to reduced BTBT.

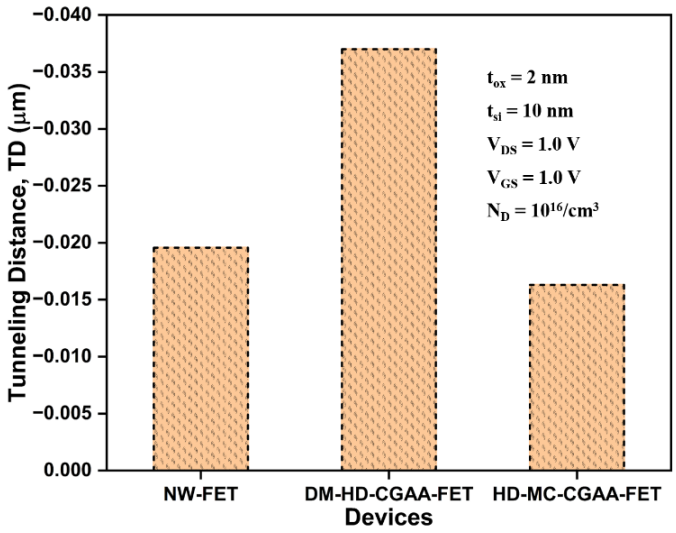


Figure 4.39 Tunnelling Distance for various device designs.

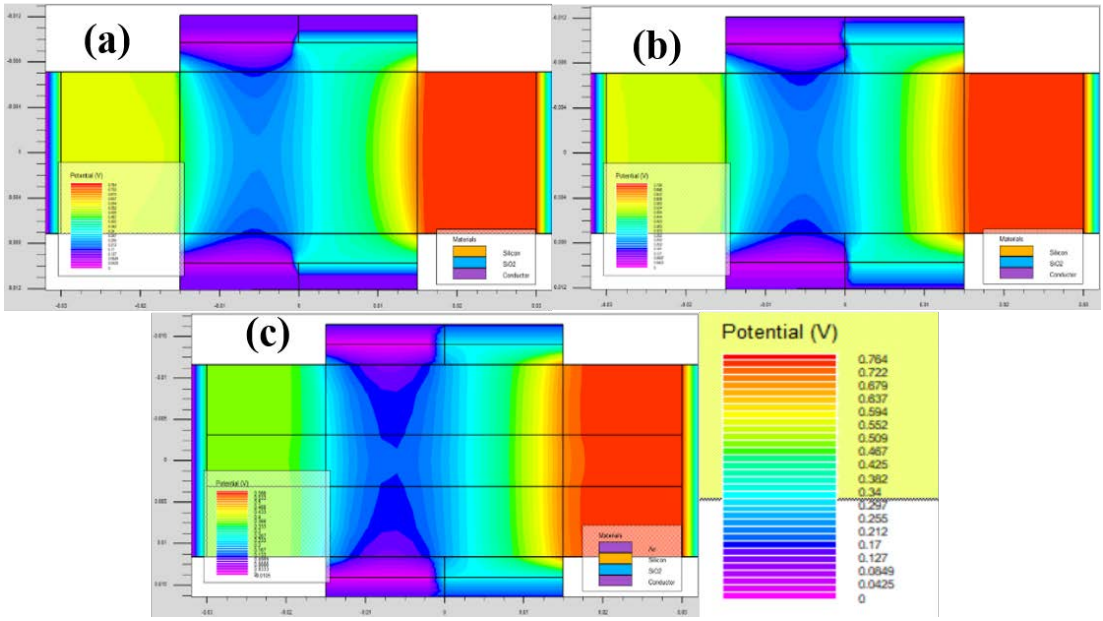


Figure 4.40 Contour Plot of Surface Potential for (a) NW-FET, (b) DM-HD CGAA FET, (c) HD-MC CGAA FET, and (d) Scale of Surface Potential.

The variation of the electric field for HD-MC CGAA FET, DM-HD CGAA FET, and NW-FET at various channel lengths is illustrated in Figure 4.42. The electric field is

measured at V_{GS} = 0.0 V and V_{DS} = 0.2 V for all the device configurations. Here, due to zero gate voltage, the device is in the OFF state, and no conduction path is generated between the source and drain sides through the channel. As HD-MC CGAA FET uses vacuum as a dielectric at the drain end and filler, it considerably weakens the impact ionization effect, lowering the electric field at the drain side and also the OFF-state leakages [88]. HD-MC CGAA FET is operating in the velocity saturation region at the channel length L = 30 nm, and the magnitude of saturation velocity of HD-MC CGAA FET will significantly increase.

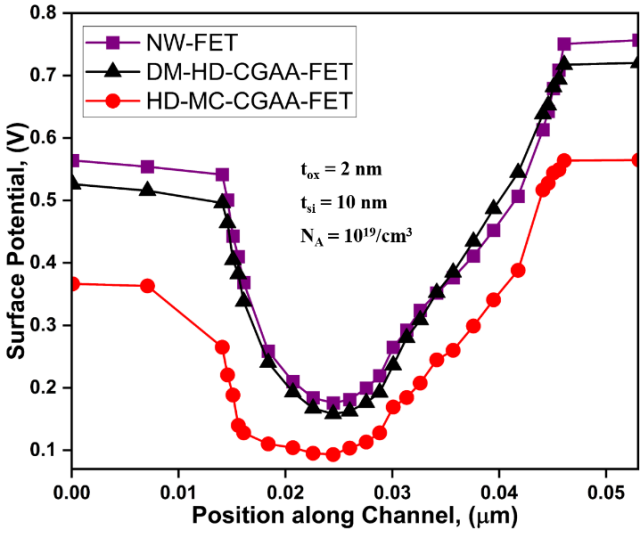


Figure 4.41 Surface Potential for various device designs at V_{GS} = 0.1 V and V_{DS} = 0.2 V.

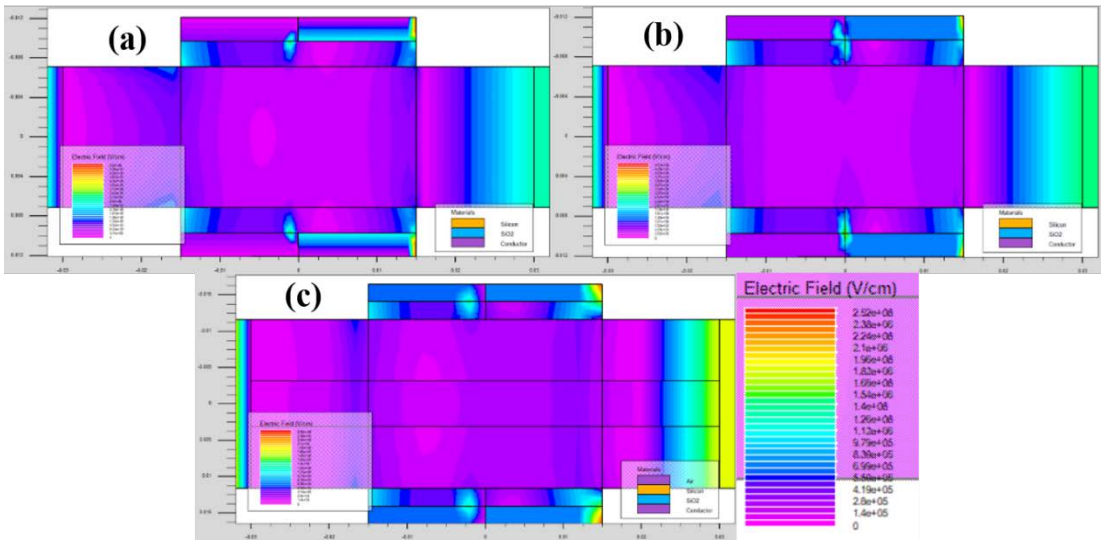


Figure 4.42 Contour Plot of Electric Field for (a) NW-FET, (b) DM-HD CGAA FET, (c) HD-MC CGAA FET, and (d) Scale of Electric Field.

Variation in hole concentration is illustrated in Figure 4.43 for HD-MC CGAA FET, DM-HD CGAA FET, and NW-FET at V_{DS} = 1.0 V and V_{GS} = -1.0 V. In the case of HD-MC CGAA FET and DM-HD CGAA FET, the hole concentration graph bends at

L = 15 nm because of the presence of a dual hetero dielectric structure where the work function of the dielectric at the drain side is comparatively lower than the work function of the dielectric at the source side. The hole concentration in the HD-MC CGAA FET is lower at the center due to the presence of a vacuum filler at the center of the channel. The comparison statistics for the hole concentration for all three devices are displayed in Figure 4.43. The HD-MC CGAA FET displays the minimal hole concentration, restricting the band tunnelling and therefore GIDL, as is seen from the figure.

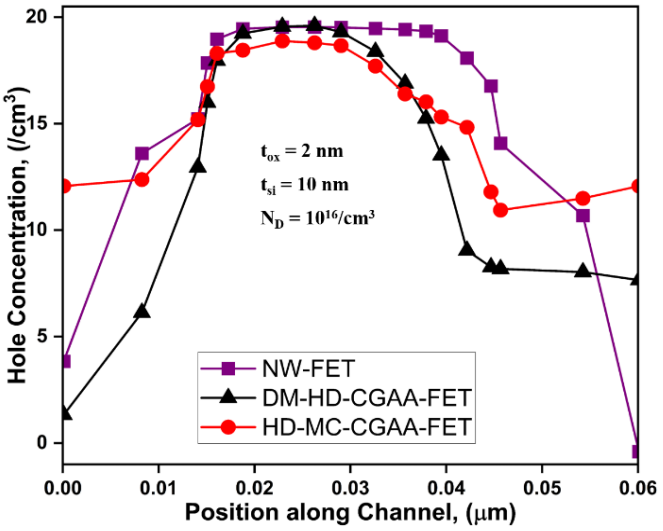


Figure 4.43 Hole Concentration for various device designs at V_{GS} = -1.0 V and V_{DS} = 1.0 V.

Figure 4.44 describes the Hole Concentration of NW-FET, DM-HD CGAA FET, and HD-MC CGAA FET at V_{GS} = -1.0 V and V_{DS} = 1.0 V. The increase in hole concentration in the channel region can be interpreted from Figure 4.41 (c). It is because of the vacuum filler present at the center of the channel.

From Figure 4.45, it is evident that the GIDL current in HD-MC CGAA FET has decreased from an order of 10^{-10} A of NW-FET and 10^{-12} A of DM-HD CGAA FET to an order of 10^{-14} A. By tunnelling from one band to another, electrons cause the subthreshold leakage event known as GIDL. In this case, the drain bias is positively charged, and the gate voltage (V_{GS}) is reduced, and the emitted electrons travelling to the drain comprise the GIDL. The decay in off-state leakage current is mostly due to the presence of hot carriers in the filler and vacuum as the gate dielectric at the drain side.

The drain current (I_{DS}) characteristics of all the devices with gate voltage (V_{GS}) are exhibited in Figure 4.46. The graph demonstrates that HD-MC CGAA FET exhibits better I_{DS} characteristics than the other designs, and the increase in drain current is dependent on the dual metal gate and the vacuum gate dielectric of the device.

The I_{ON}/I_{OFF} ratio for the proposed HD-MC CGAA FET device designs is shown in Figure 4.47. Another critical element determining a device's suitability for use is the speed at which it may flip between states is important in digital applications. The current ratio of ON to OFF states should reach the highest as practically possible to

maximize digital performance. Figure 4.44 shows that the HD-MC CGAA FET has an I_{ON}/I_{OFF} ratio that is 309 times greater than the DM-HD CGAA FET and 856 times greater than the NW-FET. HD-MC CGAA FET is a paradigm device for digital applications.

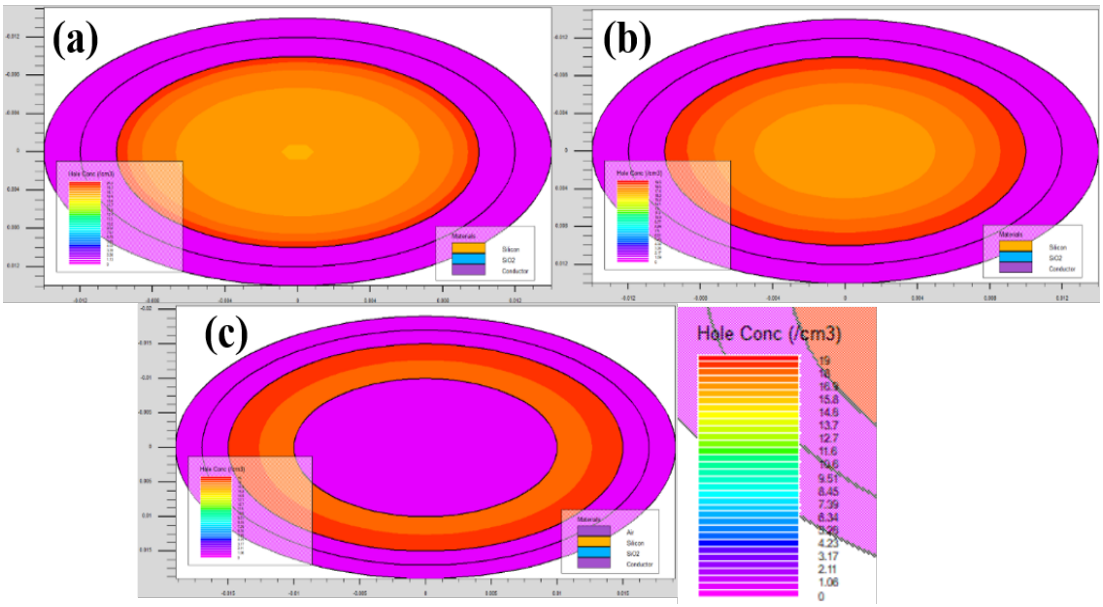


Figure 4.44 Contour Plot of Hole Concentration for (a) NW-FET, (b) DM-HD CGAA FET, (c) HD-MC CGAA FET, and (d) Scale of Hole Concentration.

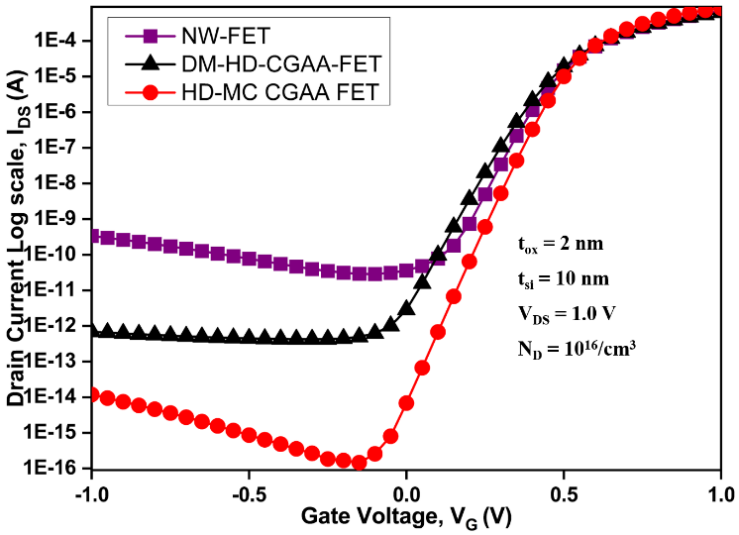


Figure 4.45 GIDL current changes along Gate Voltage.

Subthreshold slope, abbreviated SS, is shown for several devices in Figure 4.48. A device's capacity to transition from an OFF state to an ON state is described by the concept of subthreshold slope. The appropriate subthreshold slope for any device is 60 mV/decade [68]. Figure 4.48 illustrates that the NW-FET's subthreshold slope is at an optimal value of 60 mV/decade, and the DM-HD CGAA FET's subthreshold slope is slightly higher than the optimal value at 64 mV/decade. The HD-MC CGAA

FET has a subthreshold slope of 49.6 mV/decade, which is 10.3 mV/decade less than the optimal value. Because of the existence of a vacuum at the drain end and filler in HD-MC CGAA FET, the impact ionization effect considerably decreases [168], which further enhances the switching from OFF-state to ON-state, hence lowers the SS.

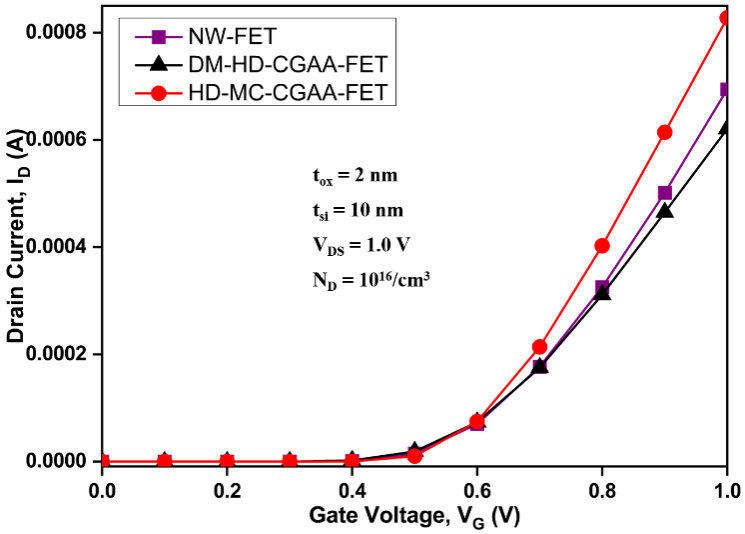


Figure 4.46 Drain Current changes along with Gate Voltage.

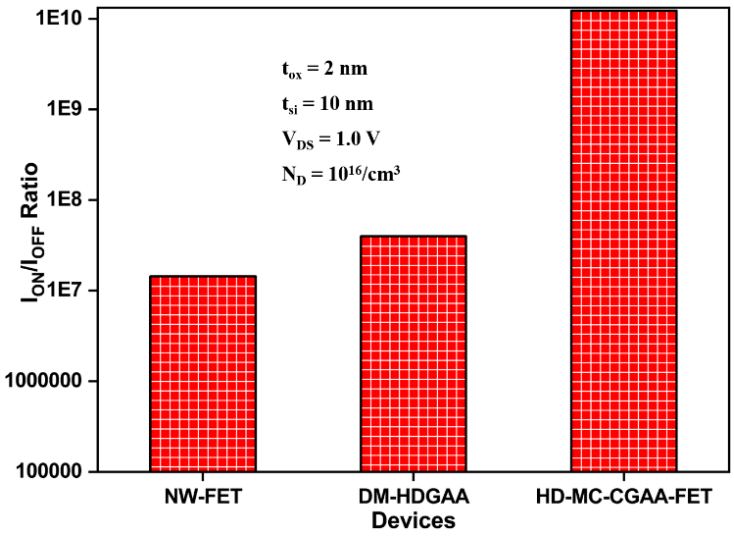


Figure 4.47 I_{ON}/I_{OFF} ratio for various device designs.

Transconductance (g_m) is shown concerning V_{GS} for all the designs in Figure 4.49 at V_{DS} = 1.0 V, which demonstrates that the HD-MC CGAA FET has the best gm profile when compared to the other devices due to the advantages of the architecture it inherits. Transconductance is obtained by calculating the current at the drain side concerning the gate side voltage and maintaining the drain voltage constant. It can also be written as [23]:

$$g_m = \left|\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \quad (4.34)$$

To make a device more effective and have a higher cutoff frequency, the transconductance should be high. By using lateral channel engineering, it is possible to reduce charge sharing while increasing transconductance.

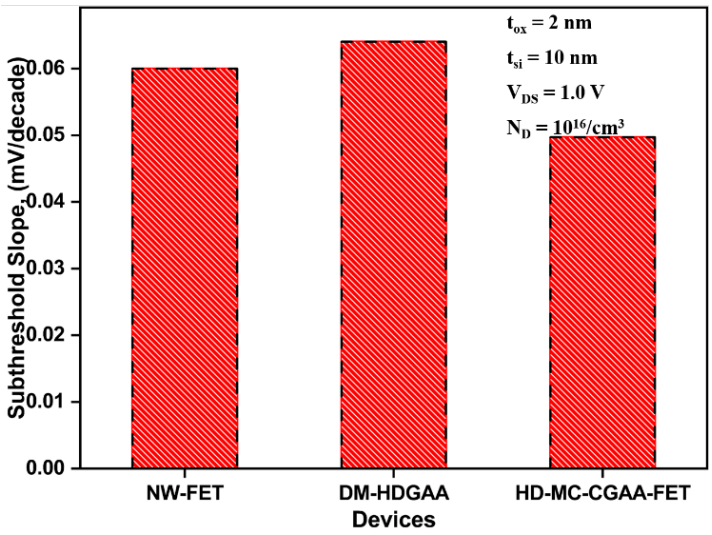


Figure 4.48 Subthreshold Slope for various device designs.

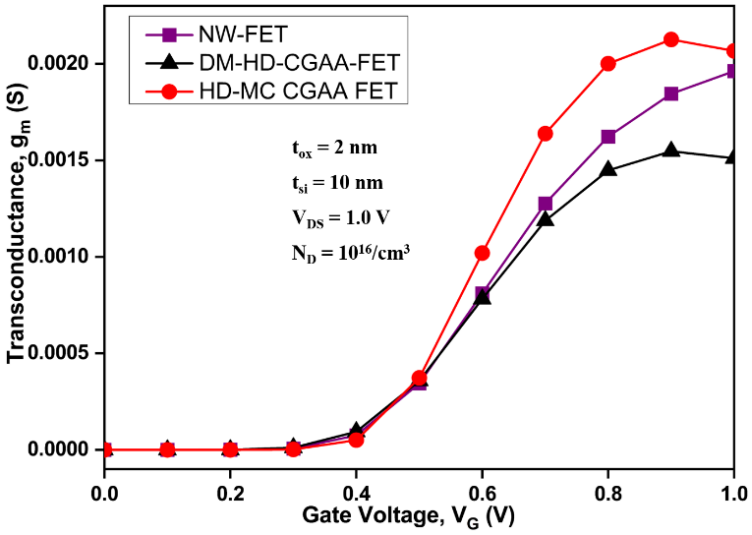


Figure 4.49 Transconductance changes along Gate Voltage.

Transconduction Generation Factor (TGF) for NW-FET, DM-HD CGAA FET, and HD-MC CGAA FET along V_{GS} is shown in Figure 4.50. HD-MC CGAA FET has the highest TGF over NW-FET, DM-HD CGAA FET, resulting in a higher ac gain of HD-MC CGAA FET. TGF of HD-MC CGAA FET is higher because of the oxide present at the drain side with low permittivity than the source side oxide, which helps in the

reduction of ionization, hence increases the TGF. Mathematically, TGF is defined as [23]:

$$TGF = \frac{g_m}{I_{DS}} \tag{4.35}$$

For all of the studied designs, the I_{DS} characteristics that correlate to V_{DS} are shown in Figure 4.51. As can be seen from the image, the construction of HD-MC CGAA FET results in a superior profile.

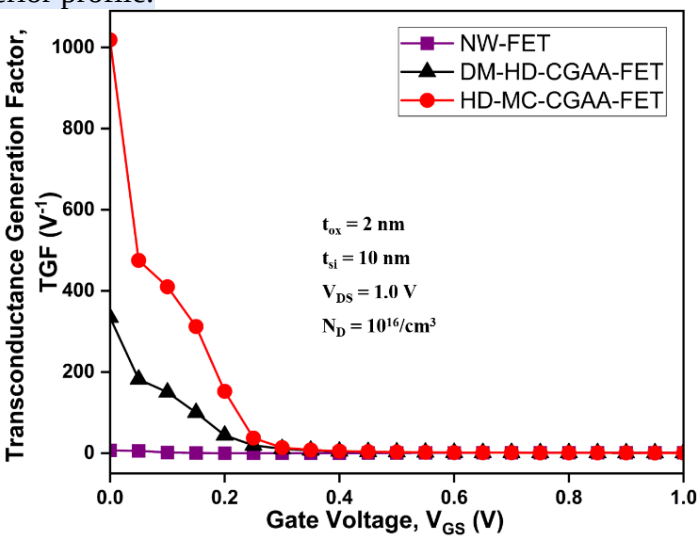


Figure 4.50 Transconductance Generation Factor changes along Gate Voltage.

The output conductance (g_d) for each of the compared devices' NW-FET, DM-HD CGAA FET, and HD-MC CGAA FET is shown in Figure 4.52 at V_{GS} = 1.0 V. Output conductance is defined as the change in drain current when the drain voltage changes. The figure suggests that HD-MC CGAA FET reveals profiles that are substantially more in line with the optimum profile. The HD-MC CGAA FET features a bigger output conductance and a higher drain current due to filler and vacuum as the dielectric. It is mathematically expressed as [23]:

$$g_d = \left|\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS}} \tag{4.36}$$

Channel Resistance (R_{ch}) is measured between the drain and source of the device. For better analog performance of a device, the R_{ch} should be as low as possible. From Figure 4.53, we can deduce that the R_{ch} of DM-HD CGAA FET is lower than NW FET and HD-MC CGAA FET. R_{ch} is inversely proportional to the subthreshold slope; hence, the SS of DM-HD CGAA FET is better than NW FET and HD-MC CGAA FET. Utilizing a dual metal gate in DM-HD CGAA FET enhances carrier transport efficiency, while using a drain end vacuum dielectric lowers impact ionization and tunnelling while simultaneously enhancing subthreshold leakages. In HD-MC CGAA FET, the impact ionization effect considerably decreases [88], which further enhances the switching from OFF-state to ON-state, hence lowers the SS, which in turn results in higher channel resistance.

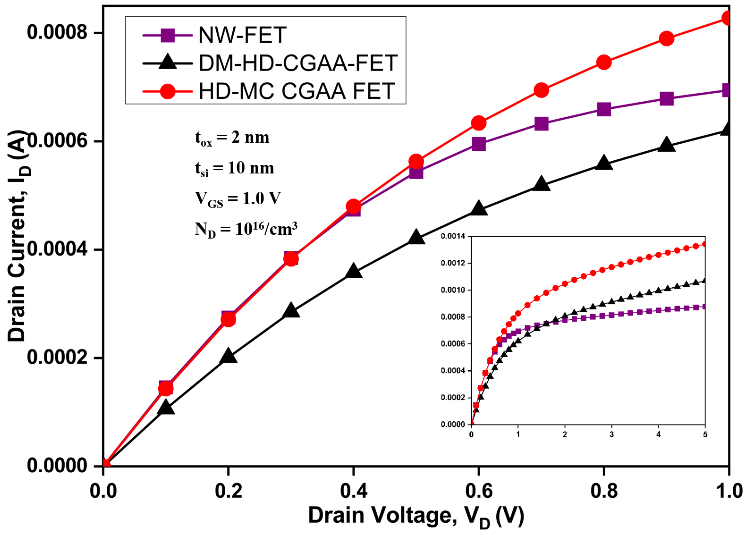


Figure 4.51 Drain Current changes along Drain Voltage.

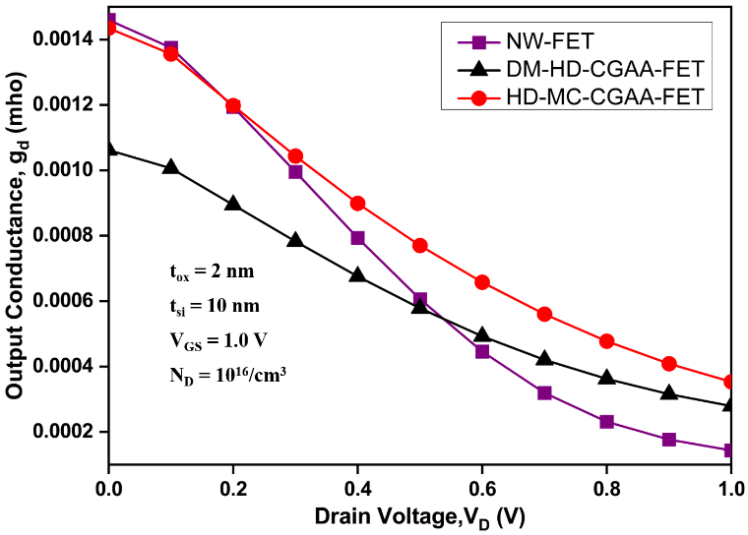


Figure 4.52 Output Conductance changes along Drain Voltage.

Intrinsic gain is defined as the relationship between transconductance and output conductance. At increasing gate voltages, when carrier mobility diminishes, so does gain. Intrinsic gain for NW FET, DM-HD CGAA FET, and HD-MC CGAA FET can be observed in Figure 4.54. With the help of the graph in Figure 4.54, it can be deduced that the intrinsic gain of HD-MC CGAA FET is higher than DM-HD CGAA FET and lower than the NW FET. Due to improved gate control over the channel, which boosts carrier mobility and gate dielectric engineering, a lower electric field is generated towards the drain in HD-MC CGAA FETs. This lower electric field decreases subthreshold leakages. Mathematically, it can be expressed as [203]:

$$A_v = \frac{g_m}{g_d} \tag{4.37}$$

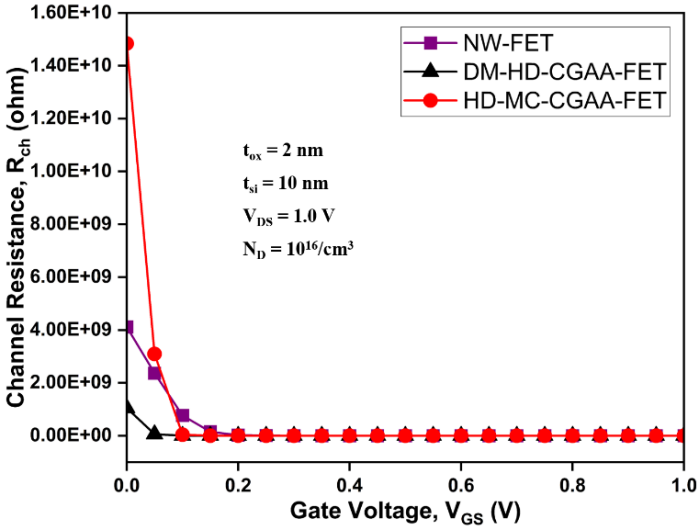


Figure 4.53 Channel Resistance changes along Gate Voltage.

Early Voltage is the ratio of output conductance to the drain current at V_{GS} = 1.0 V. Early Voltage for NW FET, DM-HD CGAA FET, and HD-MC CGAA FET is illustrated in Figure 4.55. V_{EA} of HD-MC CGAA FET is higher than DM-HD CGAA FET because of the vacuum filler at the center of the channel. The inclusion of a metal gate in HD-MC CGAA FET with a lower work function, which serves as a screen gate, and the presence of vacuum filler at the center, prevents the hot carriers from passing through and boost the early voltage. To increase the early voltage for HD-MC CGAA FET, the gate dielectric engineering further reduces the impact of ionization effect at the drain side. The gain of the device is also directly proportional to the early voltage. The mathematical expression is [203]:

$$V_{EA} = \frac{I_{DS}}{g_d} \tag{4.38}$$

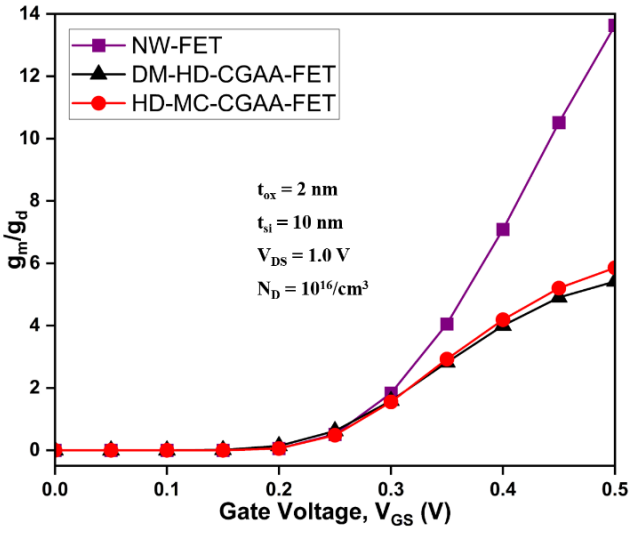


Figure 4.54 Intrinsic Gain changes along Gate Voltage.

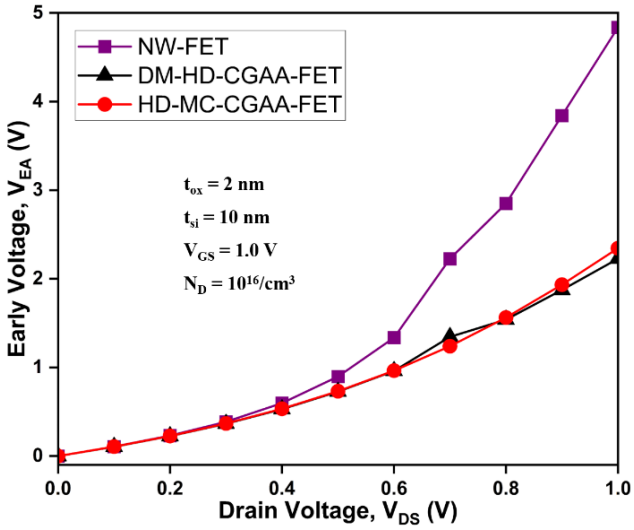


Figure 4.55 Early Voltage changes along Drain Voltage.

The permittivity of a FET is closely correlated with its capacitance. Gate to source and gate to drain capacitances together make up the FET's total gate capacitance (C_{GS} and C_{GD}). Mathematically C_{GG} is [23]:

$$C_{GG} = C_{GS} + C_{GD} \tag{4.39}$$

From Figure 4.56, it can be concluded that the C_{GG} of DM-HD CGAA FET is less than NW FET and HD-MC CGAA FET. A device's Total Gate Capacitance has a significant impact on both its high-frequency and high-speed functioning. To operate quickly, a device's C_{GG} should be as low as possible.

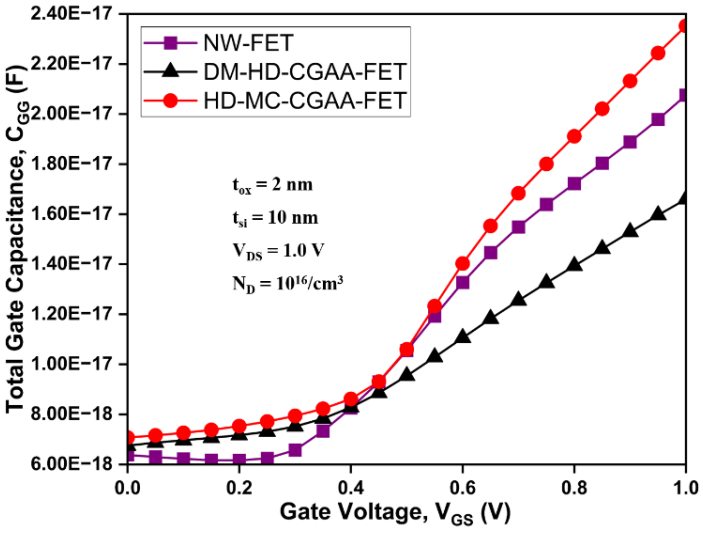


Figure 4.56 Total Gate Capacitance changes along Gate Voltage.

A device's cut-off frequency controls its high-frequency functioning. The device's high-frequency operation must be ensured by f_T being large enough. It has an inverse relationship with CGG and directly depends on gm. The f_T of NW-FET, DM-HD

CGAA FET, and HD-MC CGAA FET are illustrated in Figure 4.57. f_T is inversely proportional to CGG; hence f_T of DM-HD CGAA FET is higher than NW FET and HD-MC CGAA FET. Mathematically f_T is [23]:

$$f_T = \frac{g_m}{2\pi C_{gg}} \tag{4.40}$$

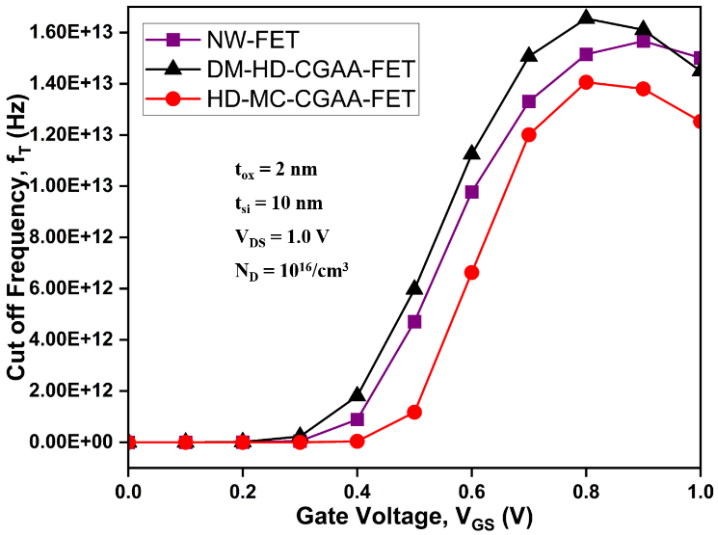


Figure 4.57 Cut-off Frequency changes along Gate Voltage.

The Gate Induced Drain Leakage (GIDL) analysis of the proposed device (HD-MC CGAA FET), conventional nanowire FET (NW-FET), and Dual Metal Hetero-Dielectric Cylindrical Gate All Around FET (DM-HD CGAA FET) device concerning gate voltage at different densities of trapped charges, positive (Q_f = 1x10^{11} /cm^3), negative (Q_f = -1x10^{11} /cm^3), and without any trap charge, is depicted in Figure 4.58. In situations where positive trapped charges are used, the GIDL for NW-FET is 1.69 x 10^{-10} A, for DM-HD CGAA FET is 7.23 x 10^{-13} A, and for HD-MC CGAA FET is 1.11 x 10^{-14} A. In case of negative trapped charges, the GIDL for NW-FET is 1.82 x 10^{-10} A, for DM-HD CGAA FET is 7.49 x 10^{-13} A, and for HD-MC CGAA FET is 1.52 x 10^{-14} A. On comparing the GIDL of all the devices having no trap charge with the GIDL of all the devices having positive and negative charges, there is no significant change. As interpreted, a minimal variation in I_{DS} has been observed in the proposed device over the existing devices under the impact of interface trap charges (ITCs). This is due to the presence of a vacuum dielectric layer and a vacuum filler at the center in the HD-MC CGAA FET, which will reduce the impact of trap charges on the device.

The influence of temperature changes on GIDL (Gate-Induced Drain Leakage) for NW-FET, DM-HD-CGAA FET, and HD-MC-CGAA FET is shown in Figure 4.59. T = 200 K, T = 300 K, T = 400 K, and T = 500 K are the temperatures considered, with a fixed V_{DS} of 1 V. The NW-FET's OFF-state leakage current is 10^{-10} A, the DM-HD-CGAA FET's is 10^{-13} A, and the HD-MC-CGAA FET's is 10^{-14} A at 200 K. The GIDL of the NW-FET stays at 10^{-10} A at T = 300 K, but the GIDL of the DM-HD-CGAA FET drops to 10^{-12} A, and the GIDL of the HD-MC-CGAA FET stays at 10^{-14} A. At T = 400 K, the GIDL for NW-FET and DM-HD-CGAA FET remains stable at 10^{-10} A and 10^{-12} A, respectively, while HD-MC-CGAA FET remains at 10^{-14} A. Lastly, at T =

500 K, the GIDL for the HD-MC-CGAA FET falls to 10^{-13} A, the GIDL for the NW-FET rises to 10^{-11} A, and the GIDL for the DM-HD-CGAA FET stays at 10^{-12} A.

Comparison of the results of the proposed structure of HD-MC CGAA FET with DM-HD CGAA FET and NW-FET is discussed in Table 4.9.

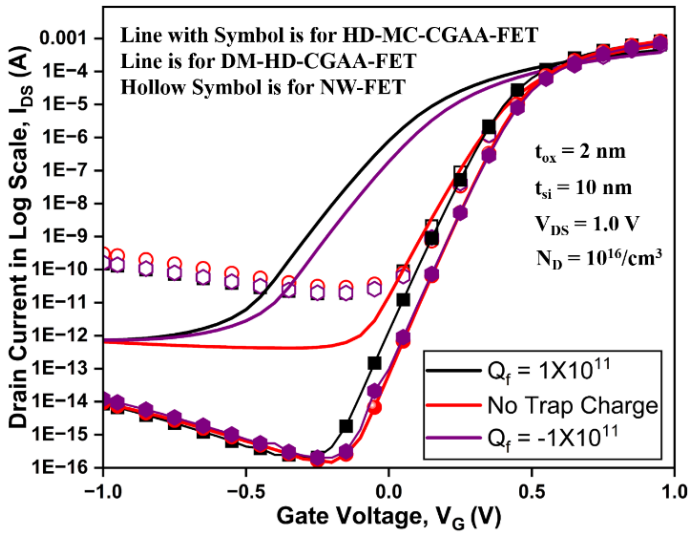


Figure 4.58 Effect of Trap Charges on HD-MC CGAA FET.

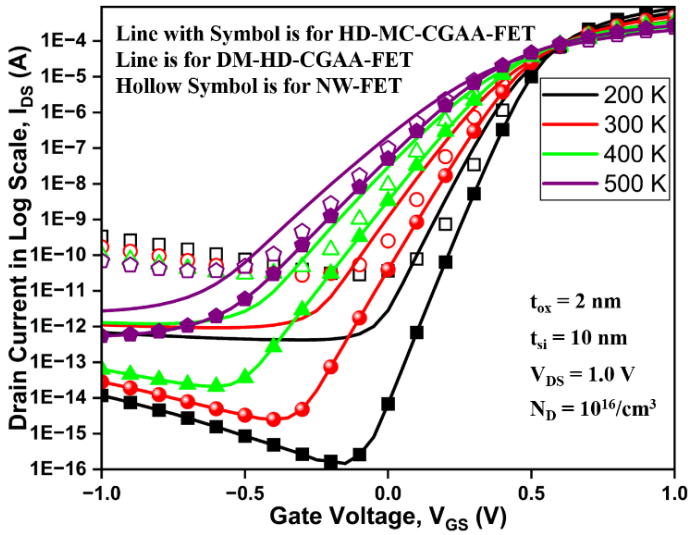


Figure 4.59 Variation in GIDL concerning Temperature.

TABLE 4.9: RESULT COMPARISON

Parameters	NW FET	DM-HD CGAA FET	HD-MC CGAA FET
Tunnelling Distance (nm)	19.5	37	16.3
Drain Current (A) at V_{GS} = 1.0 V	6.94E-04	6.21E-04	8.28E-04
Drain Current (A) at V_{DS} = 1.0 V	6.94E-04	6.21E-04	8.28E-04

GIDL (A) at V_{GS} = -1.0 V	3.38E-10	6.89E-13	1.18E-14
Hole Concentration (/cm^3) at L = 15 nm	1.95E+01	1.93E+01	1.87E+01
Transconductance (S) at V_{GS} = 1.0 V	1.96E-03	1.51E-03	2.07E-03
Transconductance Generation Factor (/V) at V_{GS} = 0.0 V	6.70E+00	3.34E+02	1.02E+03
Subthreshold Slope (mV/decade)	60	64	49.6
I_{ON}/I_{OFF} ratio	1.44E+07	3.98E+07	1.23E+10
Output Conductance (mho) at V_{DS} = 1.0 V	1.44E-04	2.79E-04	3.53E-04
Channel Resistance (W) at V_{GS} = 0.0 V	4.12E+09	1.05E+09	1.48E+11
Intrinsic Gain at V_{GS} = 1.0 V	1.36E+01	5.42E+00	5.85E+00
Early Voltage at V_{DS} = 1.0 V	4.84E+00	2.23E+00	2.34E+00
Total Gate Capacitance (F) at V_{GS} = 1.0 V	2.08E-17	1.66E-17	2.35E-17
Cut off Frequency (Hz) at V_{GS} = 1.0 V	1.50E+13	6.00E+12	5.69E+12

4.3.5 Comparative Analysis

The nanoscale transistor evolution is driven by the demand for better control of SCEs and high performance. Among various emerging devices, the Double Metal Gate Macaroni Nanowire Field Effect Transistor (DMGM-NFET), Hetero Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET), and Channel Interface-Engineered Electrostatic Potential Modulated Field Effect Transistor (CIE-EPM FET) stand out due to their distinctive architecture. Table 4.10 contains the details of the comparison of the two-device architecture and its parameters.

TABLE 4.10: RESULT COMPARISON OF DEVICES

Parameters	DMGM-NFET	HD-MC CGAA FET	CIE-EPM FET
Gate Configuration	Double Metal Gate	Double Metal + Hetero Dielectric	Double Metal Gate
Channel Shape	Cylindrical Hollow Macaroni	Cylindrical Hollow Macaroni	Cylindrical Hollow Macaroni
Subthreshold Slope (mV/decade)	~ 62 mV/decade	~ 60 mV/decade	~ 62 mV/decade
I_{ON}/I_{OFF} ratio	>10^6	Moderate	>10^6
GIDL (A) at V_{GS} = -1.0 V	Moderate (~10^{-12})	Very Low (~10^{-14})	Moderate (~10^{-12})
Transconductance (S) at V_{GS} = 1.0 V	High (3.53E-04)	Higher (2.07E-03)	High (3.53E-04)
Intrinsic Gain at V_{GS} = 1.0 V	Moderate (1.61E+01)	High (5.85E+00)	Moderate (1.61E+01)
Application	Digital Logic	Analog/RF	Digital Logic
Leakage Control	Via Dual Work Function	Via Low-k Dielectric	Via Dual Work Function
Threshold Tuning Flexibility	High	Moderate	High

Figure 4.60 contains the comparative analysis of the devices discussed in the chapter. The graph clearly represents that conventional NW FET lags in many aspects, whereas a few parameters of DMG Macaroni NW FET, like cut-off frequency, transconductance, and drive current, make it a suitable candidate for high-performance applications. In contrast, the Hetero Dielectric Macaroni NW FET demonstrates superior control over leakage and improved subthreshold performance, hence making it a prime candidate for low-power and energy-sensitive applications.

4.3.6 Challenges and Considerations

The HD-MC CGAA FET demonstrates significant improvements in electrostatic performance and leakage suppression; its practical realization poses certain fabrication challenges. Achieving precise control over the thickness and uniformity of the dual dielectric layers is essential to maintain consistent electrical behaviour and minimize interfacial defects between the dielectric materials. Any variation in the dielectric may lead to instability in threshold voltage and degradation of device reliability. Nevertheless, the HD-MC CGAA FET is inherently more compatible with modern thin film deposition techniques, particularly atomic layer deposition, which offers excellent conformality and atomic scale precision in film growth. This compatibility facilitates accurate layer formation around cylindrical channel and ensures reproducibility during large scale manufacturing. Consequently, the architecture is considered highly scalable for mass production, provided the process optimization is employed to control interface quality and minimize parasitic effects.

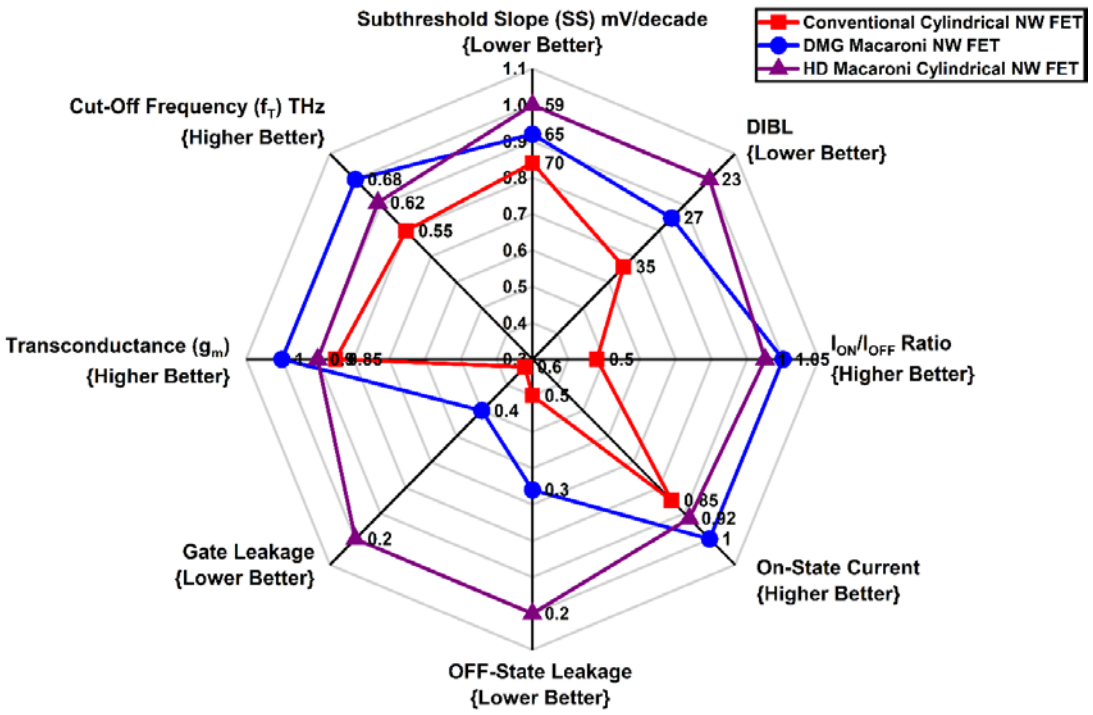


Figure 4.60 Comparative Analysis of Devices in Radar Graph

Summary

In this chapter, an in-depth investigation and comparative analysis of advanced nanowire transistor structures is done. These structures employ material as well as architectural engineering to overcome the limitations of conventional NW FETs. This chapter focuses on three advanced device architectures- Double Metal Gate Macaroni Nanowire Field Effect Transistor (DMGM-NFET), Hetero Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET), and Channel Interface-Engineered Electrostatic Potential Modulated Field Effect Transistor (CIE-EPM FET). The devices introduced in this chapter have used an innovative approach to suppress the leakage current, improve analog/RF performance metrics, and enhance subthreshold behavior. In this section, the device findings, highlighted in their technological significance in the nanoscale devices era.

The conventional NW FET was adopted as the baseline reference, and some major drawbacks were inherent in this, such as high subthreshold slope (~70 mV/decade), moderate drain-induced barrier lowering (DIBL ~35 mV/V), significant gate leakage, and limited I_{ON}/I_{OFF} ratio. The DMGM-NFET and CIE-EPM FET architecture demonstrates strong control over SCEs such as GIDL, DIBL, and SS. In this, a step potential is created along the channel, which improves the drive current and increases the carrier injection, hence making this device suitable for high-frequency and high-performance circuits. The DMGM-NFET incorporated dual metal gate electrodes, thereby enabling potential modulation across the channel. This resulted in an improvement in the subthreshold slope of the device to ~65 mV/decade and a reduction of DIBL to ~27 mV/V. The switching behavior of this device can be observed by the subthreshold slope and I_{ON}/I_{OFF} ratio.

Whereas HD-MC CGAA FET architecture leverages dielectric engineering and combining symmetrical high-κ and low-κ materials under the gate. This helps in minimizing gate leakages by reducing DIBL. These devices are suitable for ultra-low power logic and memory applications because of their ideal SS and reduced SCEs. In this device, a suppression of gate leakage current (~0.20 normalized value), better subthreshold of ~59 mV/decade, and DIBL of ~23 mV/V was observed. In addition to this better I_{ON}/I_{OFF} ratio and a significant reduction in the OFF-state leakage were observed.

Comparative analysis revealed that the DMGM-NFET and CIE-EPM FET excel in ON current, transconductance, and RF characteristics, whereas the HD-MC CGAA FET excels in leakage suppression, subthreshold characteristics, and scalability. Both devices support the THz range of cutoff frequencies, hence they are viable for analog and RF applications. This chapter emphasizes the fact that no single architecture can dominate across all performance metrics; hence, they are targeted based on the desired applications. For RF/ analog circuits, DMGM-NFET and CIE-EPM FET are preferred because of the frequency response and high drive strengths. Conversely, HD-MC CGAA FET is preferred for ultra-low power or subthreshold digital logic applications because of its low gate leakage and better energy efficiency.

In conclusion to this chapter, it is revealed that gate and dielectric engineering are effective approaches to overcome the electrostatic challenges of nanoscale FETs. The DMG structure is more suitable for high-speed, high-performance circuits, whereas the hetero-dielectric structure is better suited for low-power and leakage-sensitive applications. Future work in these designs may extend by integrating ferroelectric layers for negative capacitance effects, stacked nanowire arrays for higher drive current, and heterostructure channels for suppressing the band-to-band tunnelling.

CHAPTER 5

DESIGN AND MODELLING OF NEGATIVE CAPACITANCE FERROELECTRIC NANOWIRE FIELD EFFECT TRANSISTORS FOR LEAKAGE MINIMIZATION

Following the analytical formulation and simulation validation presented in Chapter 4, the thesis now progresses towards the exploration of performance-driven device engineering strategies in Chapter 5. Chapter 4 primarily focuses on establishing rigorous mathematical models, analyzing electrostatic behaviours and verifying their accuracy through comparison. It is critical to extend this framework to more complex and application-oriented transistor architectures. Chapter 5 is based on the validated modelling approaches by symmetrically investigating advanced nanowire FET configuration, mainly focusing on the Negative Capacitance Nanowire FET (NC-NW FET), Cylindrical Ferroelectric Dual Metal Nanowire FET (C-FE-DM-NW FET) and Cylindrical Gate Engineered Ferroelectric Nanowire FET (CGEF-NW FET). Chapter 5 represents a decisive step in bridging the gap between fundamental modelling and exploration of next-generation device paradigms.

The rapid advancement of microelectronics, driven by the continuous miniaturization of transistors, has raised demands for high-performing and energy-efficient devices. Traditional MOSFET architectures face several critical challenges when the feature size is below 10 nm, including increased gate leakage currents, elevated static power consumption, and short-channel effects (SCEs) [225], [226]. Among all these SCEs, Gate Induced Drain Leakage (GIDL) has emerged as a dominant factor that deteriorates the device performance due to the excessive band-to-band tunnelling (BTBT) at the gate drain terminal, particularly in the OFF State of the device. Nanowire FETs have gained considerable attention because of their high surface-to-volume ratio, high electrostatic control, and excellent scalability for addressing the scaling limitations [227], [228].

A particularly promising strategy to mitigate these challenges is the incorporation of ferroelectric materials into the gate stack to exploit the negative capacitance (NC) effect. This approach allows the internal voltage amplification across the gate dielectric, potentially achieving subthreshold slopes (SS) below the Boltzmann limit of 60 mV/decade at room temperature [229], [230]. Salahuddin and Datta originally proposed this concept [47], which leverages the unique polarization electric field hysteresis properties of ferroelectric materials such as hafnium zirconium oxide (HZO), which is also compatible with the traditional CMOS processes [231]. The resultant negative capacitance field effect transistors (NCFETs) have proven a dramatic reduction in SS, voltage amplification, enhanced gate control, and OFF state leakage currents, making them ideal candidates for ultra-low power applications [232].

Based on this foundation, the chapter explores three advanced device architectures that synergistically combine three-dimensional nanowire geometry, dual metal gates, and ferroelectric integration for leakage current attenuation:

First investigation presents a Negative Capacitance Nanowire Field Effect Transistor (NC-NW FET) structure incorporating a ferroelectric HZO layer between a single gate and oxide layer [59].

The second study introduces a more advanced architecture, Cylindrical Ferroelectric Dual Metal Nanowire Field Effect Transistor (C-FE-DM-NW FET), incorporating a ferroelectric HZO layer between the dual metal gate and the oxide layer [171].

The third investigation presents a Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor (CGEF-NW FET) architecture, analyzing the effect of temperature on the device [176].

The Negative Capacitance Nanowire Field Effect Transistor (NC-NW FET) demonstrates the significant reduction of GIDL current up to six orders of magnitude, along with reduced tunnelling distance and improved electron velocity when compared with traditional nanowire FET. Conversely, the Cylindrical Ferroelectric Dual Metal Nanowire Field Effect Transistor (C-FE-DM-NW FET) integrates a dual metal gate along with a ferroelectric layer modelled using the Landau-Khalatnikov (LK) formalism. The substantial suppression of OFF state leakage and enhanced gate modulation is confirmed by analytical modelling based on two two-dimensional Poisson equations, validated by numerical simulations. The Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor (CGEF-NW FET) architecture addresses the thermal reliability. The temperature-dependent parameters are analyzed from 250 K to 400 K, and the CGEF-NW FET architecture retains its leakage suppression and switching efficiency under elevated temperatures. This robustness makes it particularly suitable for energy-constrained and harsh environment applications such as IoT, biomedical electronics, and automotive systems.

Collectively, these studies establish that the confluence of ferroelectric layering, cylindrical nanowire geometry and dual metal gate engineering leads to a class of nanoscale transistors capable of circumventing the fundamental limitations imposed by Boltzmann tyranny. These architectures offer superior electrostatic control, enhanced energy efficiency and reduced leakages, all are crucial for the evolution of next-generation low-power semiconductor devices [233]. In the subsequent sections, each architecture will be explored in detail, with an emphasis on analytical modelling, simulation methodology, comparative analysis, and performance metrics. The integration of these findings will support the development of robust design guidelines for next-generation transistor technologies.

5.1 Negative Capacitance Nanowire Field Effect Transistor (NC-NW FET)

5.1.1 Working Principle and Operating Mechanism

The Negative Capacitance Nanowire Field Effect Transistor (NC-NW FET) is an evolution in the field of transistors in which a ferroelectric material layer is stacked on the oxide layer so that the device can exhibit the negative capacitance effect. This architecture offers a reduction in leakage current, suppression of short channel effects (SCEs) and reduction in subthreshold slope.

The operating mechanism of NC-NW FET is based on the negative capacitance effect exhibited by the ferroelectric materials. The ferroelectric material like hafnium zirconium oxide (HZO) can transiently exhibit a negative differential capacitance in its polarization-electric field (P-E) curve, governed by the Landau-Khalatnikov (L-K) theory. The negative capacitance effect helps enhance the device's performance, particularly in terms of leakage suppression, energy efficiency, and switching behaviour.

5.1.1.1 Principle of Negative Capacitance

In capacitors, the charge (Q) and voltage (V) exhibit linear behaviour governed by

$$C = \frac{dQ}{dV} \propto \frac{dP}{dE} \tag{5.1}$$

where C is the capacitance, and this is always positive. The ferroelectric materials, such as HfO_2 doped with Zr (HZO)exhibit a region in the polarization-electric field (P-E) curve, where $\frac{dE}{dP} < 0$, indicating negative differential capacitance. This phenomenon occurs due to the double-well shape of the Gibbs free energy curve $U(P)$associated with the ferroelectric material. Using the Landau expansion, this free energy curve can be described as:

$$U(P) = \alpha P^2 + \beta P^4 + \gamma P^6 \tag{5.2}$$

where α, β and γ are the Landau coefficient that depends on the ferroelectric material properties and the temperature. The negative second derivative of $U(P)$, i.e. $\frac{d^2U}{dP^2} < 0$, indicates that the system is in a negative capacitance state. In this region, an increase in polarization reduces the internal electric field, thus creating voltage amplification across the gate dielectric. Figure 5.1 illustrates the polarization-electric field curve of a ferroelectric hysteresis explaining the concept of negative capacitance.

5.1.1.2 Gate Stack Integration

37

The proposed device, NC-NW FET, uses the MFIS (Metal-Ferroelectric-Insulator-Semiconductor) configuration. In this, the ferroelectric layer is placed directly beneath the gate electrode and on top of a conventional oxide layer (SiO_2). In this, the total gate voltage (V_{GS}) is distributed across the ferroelectric (V_{FE}), oxide (V_{ox}) and semiconductor surface potential (Φ_s) as:

$$V_{GS} = V_{fe} + V_{ox} + \Phi_s \tag{5.3}$$

The ferroelectric capacitance becomes negative in the NC region. When this is connected with the positive capacitance of the oxide (C_{ox}) and channel (C_{ch}), the overall gate capacitance increases. The effective capacitance (C_{eff}) is given by:

$$\frac{1}{C_{eff}} = \frac{1}{C_{fe}} + \frac{1}{C_{ox}} + \frac{1}{C_{ch}} \tag{5.4}$$

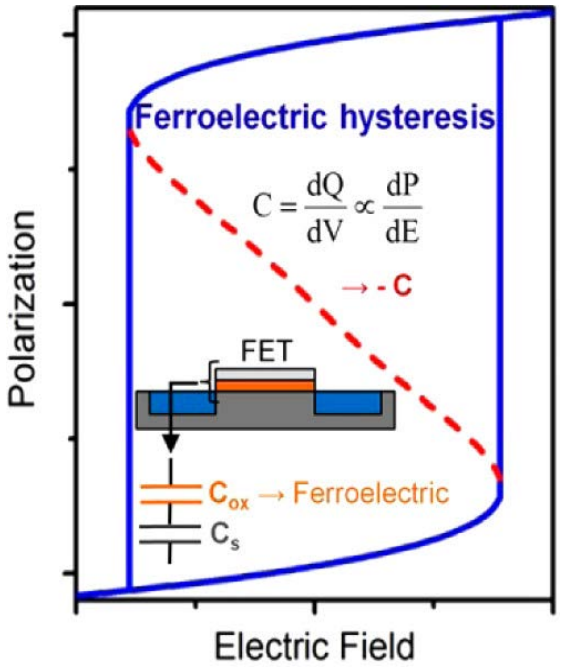


Figure 5.1 Schematic ferroelectric polarization-electric field (P-E) hysteresis loop [234]

A steeper increase in the surface potential can be observed for a small change in the gate voltage if the ferroelectric capacitance is negative, which in turn enhances the effective capacitance. This phenomenon is termed internal voltage amplification, which helps overcome the subthreshold limit of 60 mV/decade imposed by Boltzmann's tyranny.

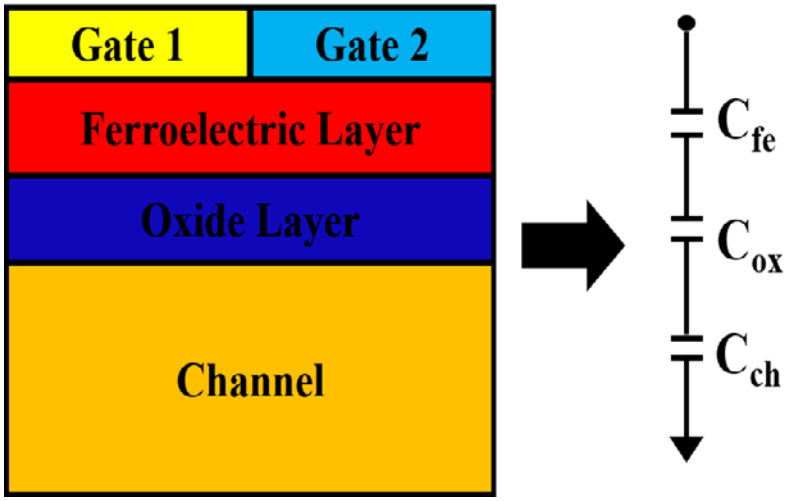


Figure 5.2 Depicting gate stack integration using MFIS schematics [176]

5.1.1.3 Subthreshold Swing and Switching Impact

In traditional MOSFETs, the minimum subthreshold slope (SS) is limited to 60 mV/decade at room temperature due to thermal limits on carrier activation. However, in NC-NW FET, the voltage amplification leads to:

$$SS = \left(\frac{dV_{GS}}{d\log I_D}\right) = \frac{kT}{q}.\ln(10).\left(1+\frac{C_{dep}}{C_{ox}}\right) \quad (5.5)$$

The internal amplification caused by the negative capacitance effectively reduces the factor $\left(1+\frac{C_{dep}}{C_{ox}}\right)$, potentially lowering SS to the values <20 mV/decade, as observed in the NC-NW FET simulations (13.4-14.1 mV/decade). This steep switching is crucial for IoT and battery-powered applications, as it improves energy efficiency, enabling operation at lower supply voltage without affecting the performance of the device.

5.1.1.4 Tunnelling Suppression and Carrier Transport

The architecture of the NC-NW FET is a gate all around (GAA) structure, which provides uniform electrostatic control over the channel. The cylindrical symmetry ensures that the gate field influences the entire channel, reducing the drain-induced barrier lowering (DIBL) and improving the threshold voltage control. The internal voltage amplification steepens the channel potential barrier, which helps suppress band-to-band tunnelling (BTBT) and gate-induced drain leakage (GIDL). As discussed in the simulations, the presence of a ferroelectric layer reduced the GIDL currents from ~10^{-8} A to ~10^{-14} A, and the tunnelling distance is reduced by up to 75%. This enhanced barrier control is particularly effective during the OFF state, preventing the unwanted flow of minority carriers that contribute to the static leakage.

5.1.1.5 Hysteresis Consideration and Dynamic Behaviour

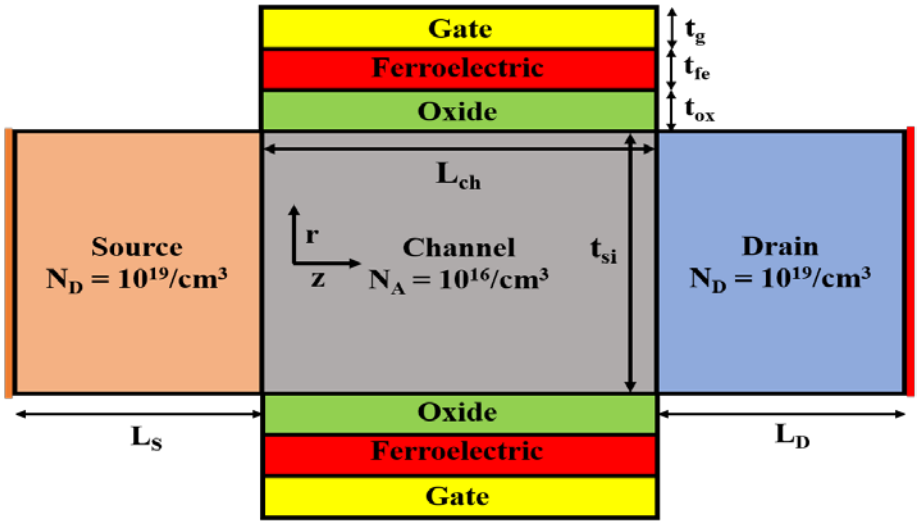
The negative capacitance effects lead to improved device performance as well as introduce potential dynamic effects such as hysteresis, which is due to the energy barriers between the ferroelectric polarization states. The hysteresis width depends on the material's coercive field and the matching of capacitances in the gate stack. If the ferroelectric capacitance is not appropriately matched with the oxide and channel capacitances, it may not operate in the unstable negative region, of could result in excessive hysteresis, resulting in a reduction in reliability in high-speed logic applications. Hence, capacitance matching is a critical design criterion for practical NC-NW FET implementation.

5.1.2 Device Architecture

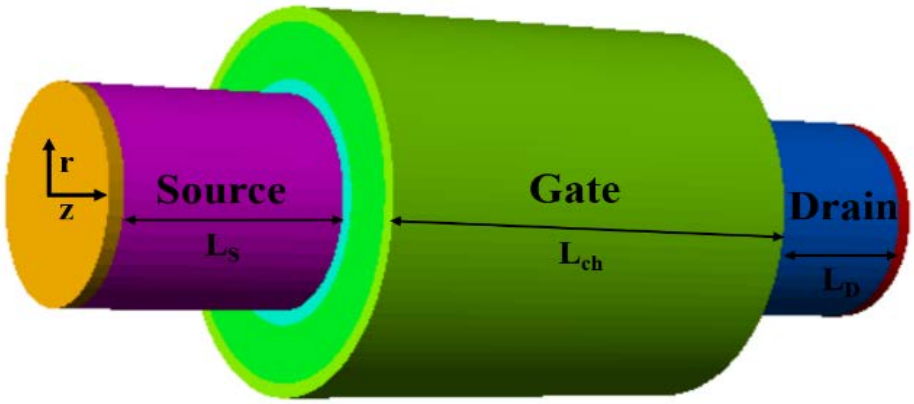
Figure 5.3 consists of the 2D and 3D schematics of the NC-NW FET, respectively. The NC-NW FET consists of a single layer of ferroelectric material (HZO) with a thickness t_{fe} (= 8 nm), a single metal gate with a thickness t_g (= 2 nm), and a dielectric oxide layer with a thickness t_{ox} (= 2 nm). The proposed NC-NW FET has a radius R (= 15 nm) and is p-type, with a doping concentration of N_D (= 10^{19}/cm^3) at both the source

and drain regions [235]. Table I contains detailed structural specifications of the devices used in the manuscript.

The confinement of energy within devices featuring channel dimensions is considerably smaller than 30 nm, coupled with radii on the order of 5 nm, which induces significant quantum mechanical effects, as noted in prior studies [14][15]. However, given the scope and focus of our current investigation, these quantum mechanical effects have been deemed negligible and, consequently, omitted from consideration in this analysis. [23][24]. As illustrated in Figure 5.4, our validation efforts are grounded in aligning the design methodology with pre-existing frameworks, thereby facilitating a practical and coherent integration of our approach with previously established works. [235][58]This alignment not only reinforces the credibility of our results but also demonstrates the feasibility of extending conventional models to elucidate device behaviour in a similar context.



(a)



(b)

Figure 5.3 (a) Two-Dimensional view of NC-NW FET, (b) Three-Dimensional view of NC-NW FET.

TABLE 5.1: DEVICE SPECIFICATION

Parameters	CNW FET	NC-NW FET
Ferroelectric Thickness (t_{fe})	-----	8 nm
Radius (r)	15 nm	15 nm
Gate Thickness (t_g)	2 nm	2 nm
Channel Length (L)	50 nm & 60 nm	50 nm & 60 nm
Length of S/D	30 nm	30 nm
Channel Doping	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$
Work Function	4.86 eV	4.8 eV
Oxide Thickness (t_{ox})	2 nm	2 nm
Silicon Thickness (t_{si}=2r)	30 nm	30 nm

TABLE 5.2: FERROELECTRIC SPECIFICATION

Parameters	Symbol	Values
Coercive Field	E_c	1-2 MV/cm
Spontaneous Polarization	P_s	10-40 μC/cm^2
Remnant Polarization	P_r	1-40 μC/cm^2
Dielectric Constant	ε	30

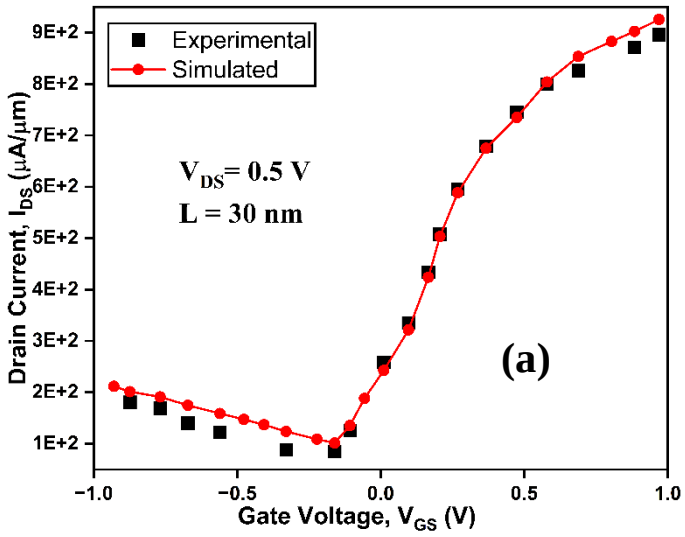


Figure 5.4 Calibration of transfer characteristics of (a) Nanowire FET [24]

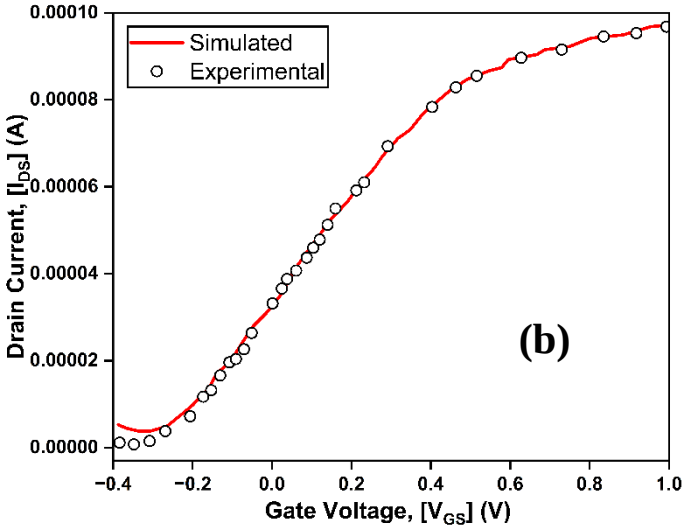


Figure 5.4 Calibration of transfer characteristics of (a) Nanowire FET, (b) Ferroelectric FET [234]

5.1.3 Simulation Setup

The ATLAS 3D TCAD simulation tool was employed to perform the numerical simulations [21]. The simulator was employed with a suite of advanced physical models tailored for nanowire ferroelectric FETs. The Newton-Gummel iterative approach was used for solving the carrier transport equations. This approach is well known for its effectiveness in handling the nonlinearities associated with semiconductor device modelling [22]. The models are chosen based on their relevance to the proposed device structure.

The Concentration-Dependent Mobility (CVT) model [236] considers the degradation of charge carrier mobility due to impurity scattering in highly doped regions. This model enables accurate estimation of drift current by adjusting mobility as a function of electric field and doping concentration. Shockley Read Hall (SRH) recombination model [232] accounts for the generation and recombination of carriers through mid-gap defect states. This model is used for simulating trap-assisted processes in semiconductor materials, which have a significant influence on OFF-state leakages and subthreshold behavior in nanoscale devices.

TABLE 5.3: SIMULATION MODELS

Models	Details
SRH	Employed to integrate the impact of carrier recombination phenomena.
CVT	A comprehensive model incorporating the effects of doping concentration (N), temperature (T), and electric field (E) is particularly well-suited for analyzing non-planar devices.
FERMI	In regions of substantial doping, carrier concentrations exhibit a pronounced diminution.

BBT.STD	Utilized to quantify the influence of tunneling phenomena on charge carriers.
FERRO	Facilitates the application of the ferroelectric permittivity model.
LK	It permits the establishment of the interface between the gate electrode and the oxide layer.
CONMOB	Employed to address the influence of mobility concentration within MOSFET.

5.1.4 Results and Discussion

Figure 5.5 displays contour plots depicting the hole concentration (/cm³) of CNW FET and NC-NW FET at V_{GS} = -1.0 V and V_{DS} = 1.0 V. In this, because of the presence of the ferroelectric layer, the hole concentration at the centre of the NC-NW FET is high when compared with the CNW FET.

Figure 5.6 displays the variability in band energy as a function of position along the channel length. [195]. Band-to-band tunnelling (BTBT) serves as a pivotal metric for assessing the reliability and operational efficacy of electronic equipment. When depletion worsens and drains bias increases, there are a lot of crossovers between the bands of valence and conduction. In the OFF state, electrons tunnel from the valence to the conduction bands because the bands overlap. It denotes that the BTBT creates a significant rise in leakage current when turned off. Because of the dielectric layer, this decrease has occurred owing to the ferroelectric capacitance.

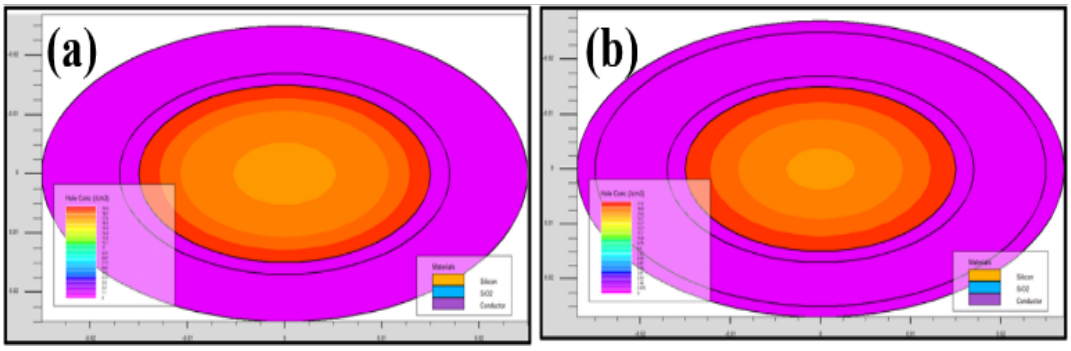


Figure 5.5 Concentration of Holes for (a) CNW FET, (b) NC-NW FET.

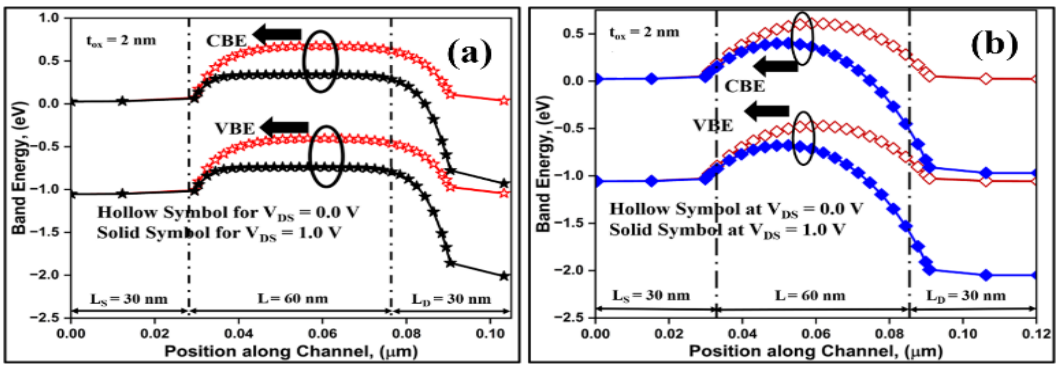


Figure 5.6 Band-to-band tunnelling of (a) CNW FET, (b) NC-NW FET.

Figure 5.7 describes the tunnelling distance of CNW FET and NC-NW FET at 50 nm and 60 nm, respectively. The tunnelling distance in terms of the 50 nm channel length of NC-NW FET is 75% less than CNW FET, and in the 60 nm channel length tunnelling distance of NC-NW FET is 54% reduced. As shown in Figure 5.6, there is a considerable lowering of band energies in the NC-NW FET in comparison to the CNW FET, and this leads to a reduction in tunnelling distance for the NC-NW FET.

Figure 5.8 contains the electron velocity contour map of (a) CNW FET and (b) NC-NW FET. From the contour map, it can be concluded that the electron velocity of NC-NW FET is higher in the channel region, whereas the electron velocity of CNW FET is present in the source side and drain side as well.

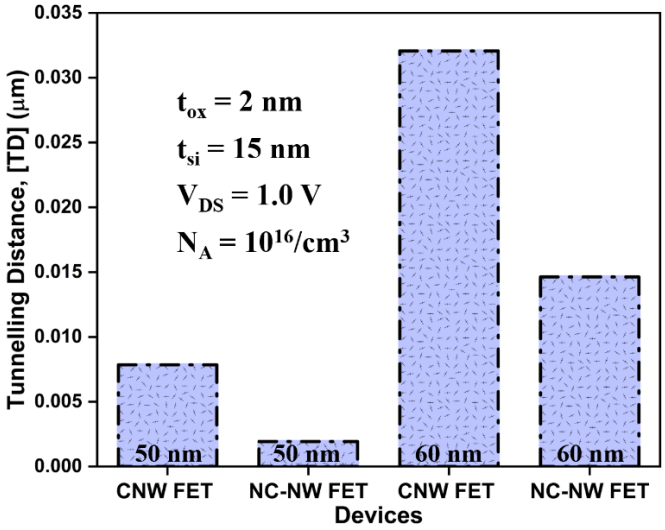


Figure 5.7 Tunnelling distance for various devices.

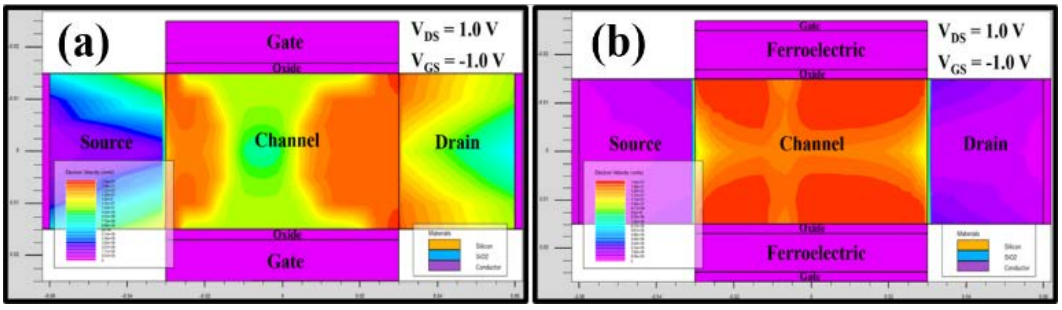


Figure 5.8 Electron velocity contour of (a) CNW FET, (b) NC-NW FET.

Figure 5.9 displays the CNW FETs and NC-NW FETs potential contour at V_{GS} = -1.0 V and V_{DS} = 1.0 V. In the absence of any input gate voltage (V_{GS} = 0.0 V), the CNW FET is turned off, preventing current from flowing from the source side and the drain side throughout the channel and the depletion layer.

Figure 5.10 illustrates the variation of GIDL current with V_{GS} across different device configurations. It is evident from Figure 8 that for an NC-NW FET with a 50 nm channel length, the GIDL current has decreased from approximately 10^{-8} A to around 10^{-13} A. Similarly, for a channel length of 60 nm, the GIDL current in an NC-NW FET

has reduced from about 10^{-8} A to approximately 10^{-14} A. GIDL, which represents subthreshold leakage, occurs when a moderate V_{GS} is applied to the source side while the drain side is maintained at a higher positive bias. The inclusion of a ferroelectric layer between the gate and oxide significantly reduces the generation of hot carriers, thereby reducing OFF-state leakages.

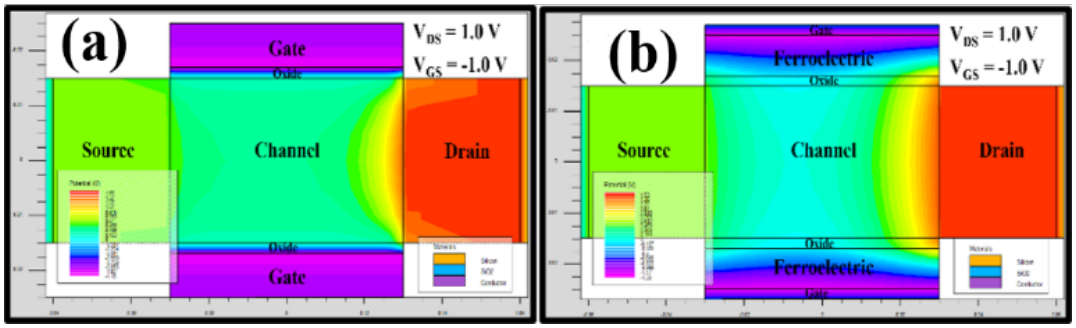


Figure 5.9 Potential contour of (a) CNW FET, (b) NC-NW FET.

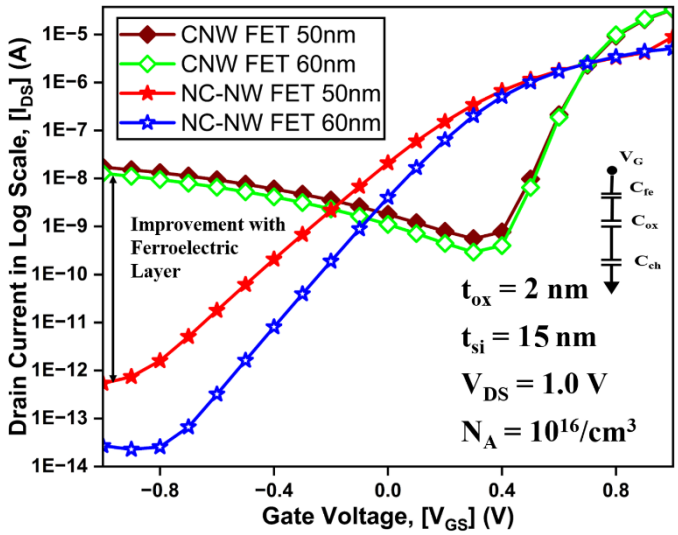


Figure 5.10 Gate-Induced Drain Leakage of various devices.

In Figure 5.11 the results of first-order transconductance are equated to CNW FET and NC-NW FET for channel lengths of 50 nm and 60 nm. Transconductance plays a critical role in choosing the ideal bias point and in analog/RF applications. At the ideal bias point, each device's cut-off frequency is at its lowest.

Figure 5.12 depicts how closely the subthreshold slope of the CNW FET and NC-NW FET at 50 nm and 60 nm channel lengths is similar to the ideal value. A 50 nm NC-NW FET has a subthreshold slope of 14.1 mV/decade, whereas a 60 nm NC-NW FET has a subthreshold slope of 13.4 mV/decade. In comparison to this, 50 nm CNW FET has a subthreshold slope of 26.7 mV/decade, and 60 nm CNW FET has a subthreshold slope of 18.1 mV/decade.

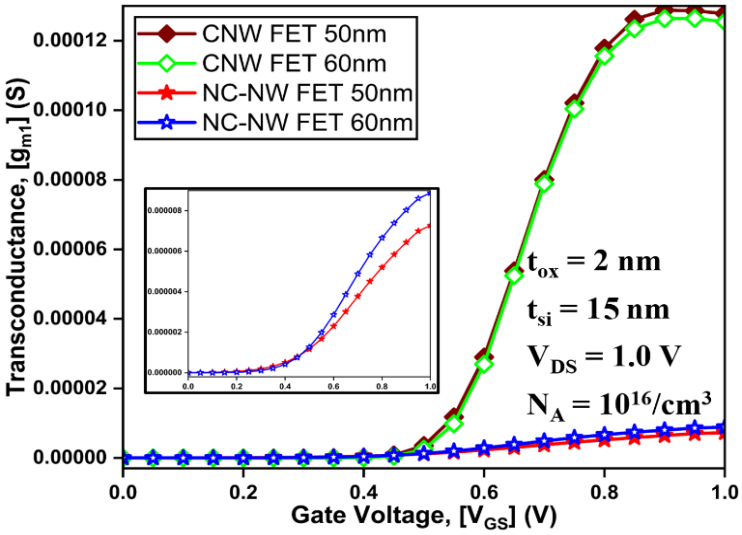


Figure 5.11 Transconductance of various devices.

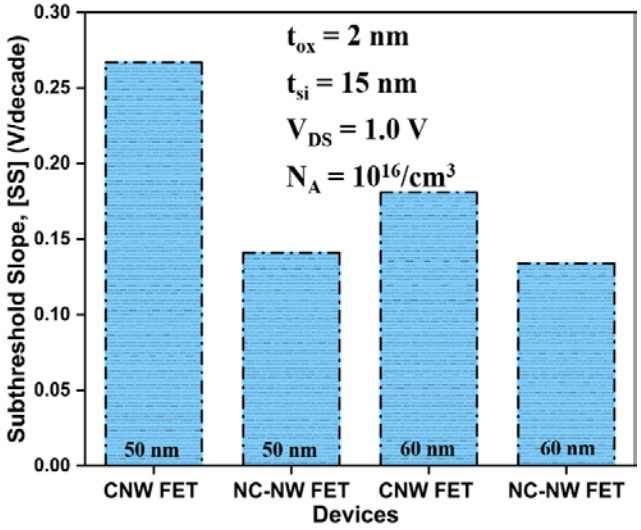


Figure 5.12 The subthreshold slope of various devices.

5.1.5 Comparative Analysis

On comparing the traditional NW FETs with the NC-NW FET, various superior traits of the NC-NW FET are observed. The presence of the NC layer in the gate stack creates a virtual voltage booster, which enhances the channel inversion and reduces the gate voltages. This will effectively reduce the leakage current and energy dissipation, which is crucial for next-generation AI and IoT hardware.

The NC-NW FET retains excellent electrostatic integrity over FinFETs or planar devices because of the gate all around (GAA) configuration and radial symmetry. This helps NC-NW FET in becoming more suitable for ultra-scaled logic and analog/RF applications where short-channel control is paramount.

5.1.6 Challenges and Considerations

Despite the promising performance demonstrated by negative capacitance nanowire field effect transistors (NC-NE FETs) in reducing power consumption, achieving steep subthreshold slopes and enhanced drive currents, several practical challenges remain in deploying NC-NW FETs for commercial use.

The foremost difficulty lies in fabrication of the device. The deposition of ultra-thin hafnium zirconium oxide (HZO) layers with precision and uniform ferroelectric polarization characteristics is demanding. The atomic layer deposition (ALD) method, although widely used, requires precise control of precursor dosing and cycle timing to ensure conformality and reproducibility. Moreover, the annealing process significantly affects the stabilization of the orthorhombic ferroelectric phase, crystallinity and grain structure, all of which are crucial for consistent device operation [237].

The second challenge arises from the ferroelectric hysteresis. The negative capacitance (NC) effect enhances the performance of the device by enabling sub-60 mV/decade subthreshold swing, it simultaneously introduces the hysteresis in the transfer characteristics (I-V curve). Such hysteresis led to threshold voltage variability and compromise system stability in digital logic circuits which demand predictable and reliability operation's [236].

Material reliability also poses significant concerns. The ferroelectric behaviour of HZO is sensitive to thermal fluctuations and scaling effects. At elevated operating temperatures, the remaining coercive field (E_c) and polarization (P_r) may degrade at elevated temperatures, causing device instability and shifting in threshold voltage over prolonged operation [238].

Another major issue is scalability and integration of CMOS technology with the ferroelectric material. Although HZO offers intrinsic material due to its compatibility with CMOS, the long-term stability of ferroelectric- semiconductor interfaces are uncertain. Problems such as oxygen vacancies, interfacial trap formation and diffusion defects can degrade the device performance. Hence, process optimization and interfacial engineering remain essential for realizing practical VLSI integration [239].

Finally, voltage instability presents a fundamental design challenge. The material and insulator capacitances should be carefully matched as the NC region operates in a metastable state. This helps in avoiding amplification-induced instability. Any mismatch can trigger amplification induced instability, leading to oscillations or abrupt switching, which compromise both device and circuit reliability [240].

These challenges can be addressed by further exploration into doped or alloyed variants of HZO, that stabilize the ferroelectric phase, advanced modelling approaches the capture complex ferroelectric switching dynamics, and process optimization aimed at reproducibility and large-scale manufacturability. These advancements will be indispensable for transforming NC-NW FETs from laboratory prototypes into mainstream semiconductor devices.

5.2 Cylindrical Ferroelectric Dual Metal Nanowire Field Effect Transistor (C-FE-DM-NW FET)

5.2.1 Working Principle and Operating Mechanism

The Cylindrical Ferroelectric Dual Metal Nanowire Field Effect Transistor (C-FE-DM-NW FET) is an evolution in the field of transistors in which a ferroelectric material layer is stacked on the oxide layer so that the device can exhibit the negative capacitance effect. The presence of dual metal gates in this architecture helps in better electrostatic control of the channel. This architecture offers a reduction in leakage current, suppression of short channel effects (SCEs), and reduction in subthreshold slope.

The operation of the C-FE-DM-NW FET is driven by the synergistic interplay between the dual metal-induced electrostatic modulation and ferroelectric negative capacitance.

5.2.1.1 Negative Capacitance Effect

As in NC-NW FETs, the ferroelectric HZO layer exhibits a region of negative differential capacitance in its polarization-electric field curve, governed by Landau-Khalatnikov (L-K) theory. This leads to internal voltage amplification and enhances the channel potential for a given gate bias. The total gate voltage (V_{GS}) is partitioned among the voltage at the ferroelectric layer (V_{FE}), the voltage at the gate oxide (V_{ox}), and the semiconductor surface potential (Φ_s) for a given V_{GS}. At a given V_{GS}, when ferroelectric capacitance attains a negative value, it amplifies the surface potential [98]. This amplification in surface potential enables stronger channel inversion at lower gate voltages, thereby reducing the turn-on voltage and suppressing the subthreshold slope.

5.2.1.2 Dual Metal Gate Modulation

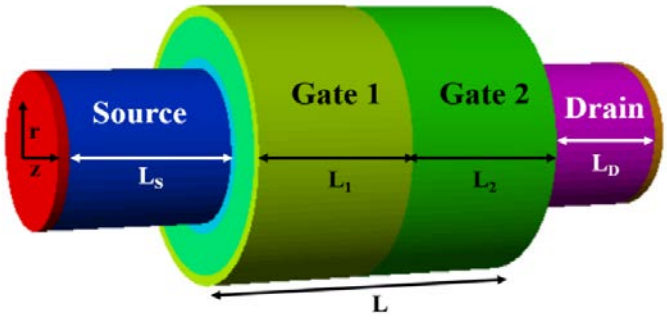
The inclusion of two different work functions within the gate creates a longitudinal potential asymmetry. This asymmetry allows localized tuning of the electric field across the channel. The higher work function near the drain side raises the potential barrier, which will help in suppressing band-to-band tunnelling (BTBT) and gate-induced drain leakage (GIDL). The lower work function of the gate near the source side enhances carrier injection, thereby improving the ON-state performance of the device. The dual metal configuration enables better channel control and mitigates leakage current [241].

5.2.2 Device Architecture

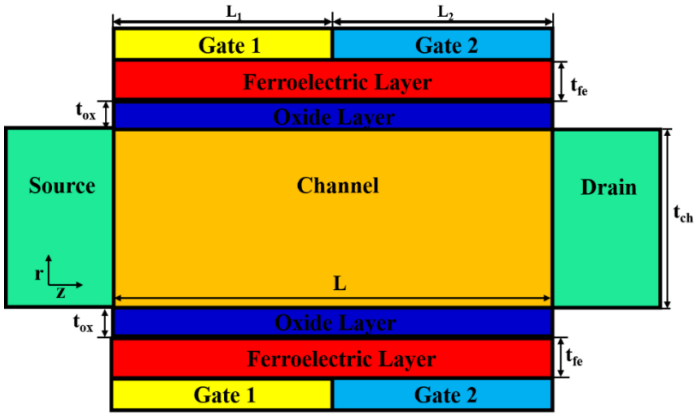
In this manuscript, the proffered device C-FE-DM-NW-FET is a symmetrical dual metal gate structure having a ferroelectric layer between the gate and oxide layer. In this C-FE-DM-NW-FET structure comprises of the dual metal gates with lengths L_1 = L_2 (= 25 nm) and thickness t_g (= 2 nm), the ferroelectric material (HZO) has thickness t_{fe} (= 8 nm), and a single dielectric oxide layer has thickness t_{ox} (= 2 nm). Figure 5.13(a) and (b) portray the 3-D schematics of the C-FE-DM-NW-FET and 2-D schematics. The proffered C-FE-DM-NW-FET has a radius of R (= 15 nm). This n-type device has

an N_D (= 10^{19}/cm^3) doping concentration at the source edge and the drain side. Figure 5.13(c) shows the proper energy bands in the channel-normal direction when the device is used in the NC region. The channel area is P-doped, curved downward, and inverted. The inherent Fermi level, E_i, is implied, and the energy band gap, E_C/E_V, which stands for the band of conduction and band of valence, respectively, is what determines the energy band gap.

Molybdenum was utilized as the gate component in several topologies in this text. The gate metal's work function differs in various topologies because it manipulates the nitrogen implantation, which modifies the threshold voltage of the devices. Table 5.4 contains all the structural specifications for the Cylindrical-Nanowire Field Effect Transistor (C-NW FET) and the C-FE-DM-NW FET. The present research has ignored the quantum effects since they don't exhibit any change in the I_D–V_G attributes down to 20 nm channel length [242] and our work is at L = 50 nm and 60 nm, respectively. Quantum and ballistic transport effects are not included as they occur in devices with channel sizes much smaller than 30 nm and a radius in the 5-nm range. The dependency of the device on various parameters, such as doping, gate work function, and temperature, will have a crucial effect on the performance of the device [243][244][245]. Additionally, the non-ideal conditions, such as gate oxide leakage, fringing field, or trap charges, are not taken into account.

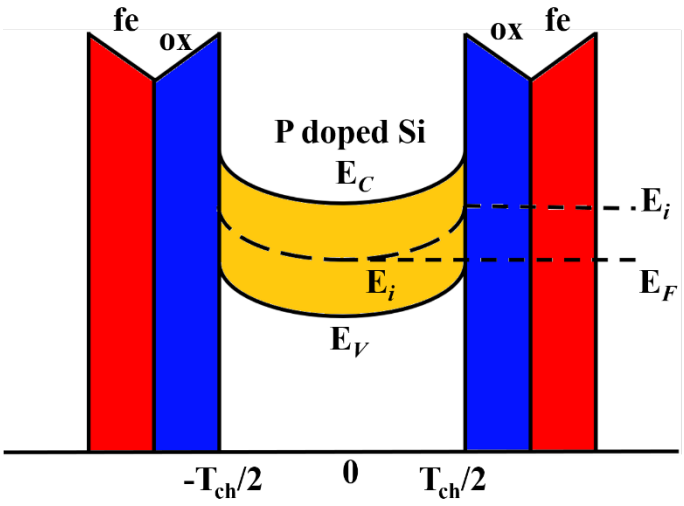


(a)



(b)

Figure 5.13 (a) 3-D schematics of C-FE-NW FET, (b) 2-D schematics of C-FE-NW FET



(c)

Figure 5.13 (c) Energy Band of C-FE-DM-NWFET in NC Region.

TABLE 5.4: STRUCTURAL SPECIFICATION

Parameters	C-NW-FET	C-FE-DM-NW-FET
Channel Length (L)	50 nm & 60 nm	50 nm & 60 nm
Channel Doping	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$
Oxide Thickness (t_{ox})	2 nm	2 nm
Silicon Thickness (t_{si})	30 nm	30 nm
Length of S/D	30 nm	30 nm
Ferroelectric Thickness (t_{fe})	-----	8 nm
Gate Thickness (t_g)	2 nm	2 nm
Work Function (Φ_{m1})	4.84 eV	5.62 eV
Work Function (Φ_{m2})	4.36 eV	4.4 eV

Ferroelectric material specifications for HZO are listed in Table 5.5 In Figure 5.14, we validate our efforts by combining the alignment of our arrangement with previously created work. Figure 5.14 (a) contains the calibration of the nanowire FET [24] whereas (b) contains the calibration of the ferroelectric FET. The manufacturing process for this design is challenging and costly.

TABLE 5.5: FERROELECTRIC MATERIAL SPECIFICATIONS

Parameters	Symbol	Values
Remnant Polarization	P_r	$10\mu C/cm^2$
Coercive Field	E_c	1MV/cm
Dielectric Constant	ε	30

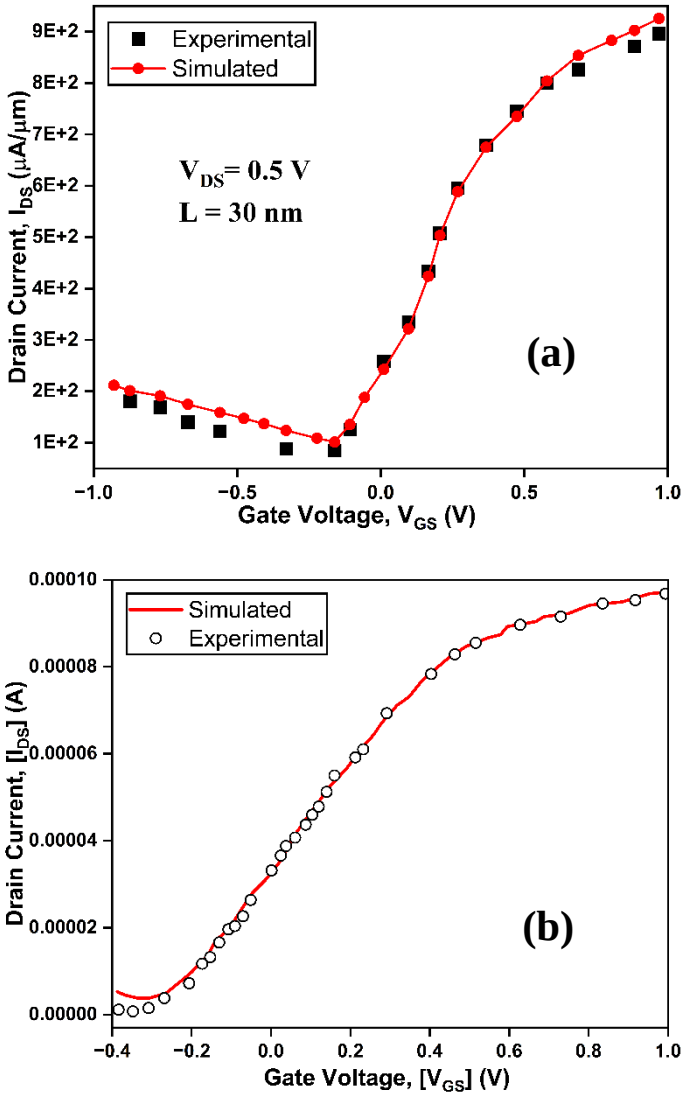


Figure 5.14 Calibration with experimental work of (a) transfer characteristics of nanowire FET, (b) transfer characteristics of ferroelectric FET [24][235]**.**

5.2.3 Simulation Setup

The ATLAS 3D TCAD simulation tool was employed to perform the numerical simulations [21]. The simulator was employed with a suite of advanced physical models tailored for nanowire ferroelectric FETs. The Newton-Gummel iterative approach was used for solving the carrier transport equations. This approach is well known for its effectiveness in handling the nonlinearities associated with semiconductor device modelling [22]. The models are chosen based on their relevance to the proposed device structure.

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gap defect states. This model is used for simulating trap-assisted processes in semiconductor materials, which have a significant influence on OFF-state leakages and subthreshold behavior in nanoscale devices.

Table 5.6: MODEL DETAILS

Models	Details
SRH	Used to incorporate the carrier recombination effect
FERMI	Carrier concentrations are lower in extensively doped areas.
FERRO	Allows the ferroelectric permittivity model to be used.
CVT	Complete model including N, T, E effects. Good for non-planar devices
LK	It enables the interface between the gate and the oxide layer.
CONMOB	Used to account for the effect of MOSFET mobility concentration
BBT.STD	Used to measure the tunnelling impact of charge carriers

5.2.4 Fabrication

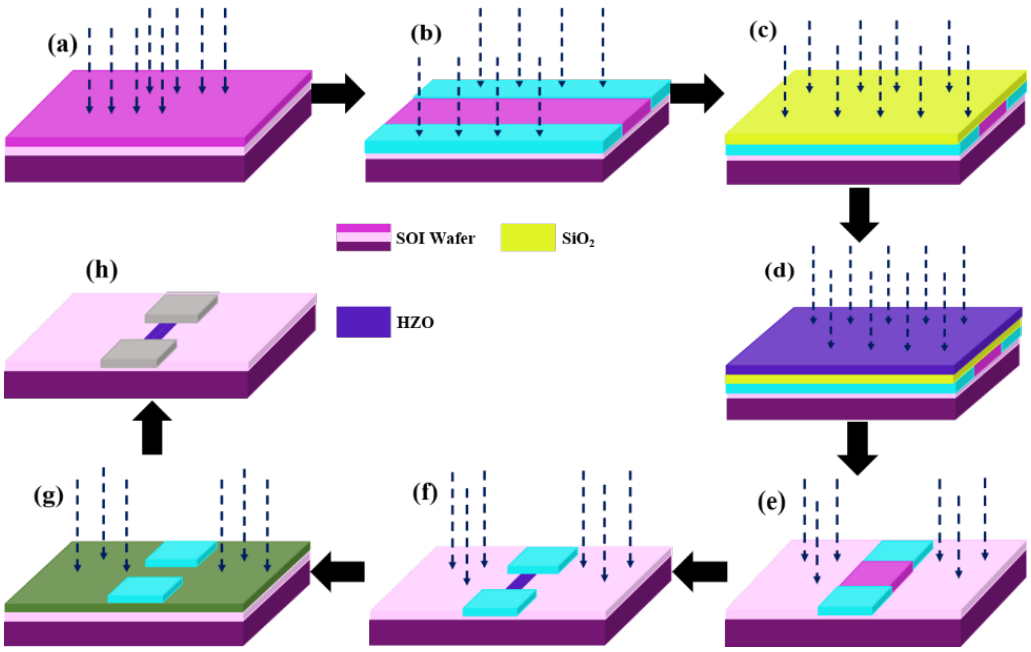


Figure 5.15 Fabrication steps of C-FE-DM-NW FET

A silicon-on-insulator (SOI) wafer is taken, which contains the substrate layer of silicon, which is buried with a dielectric layer, and the top is layered with silicon. The top silicon layer is initially doped with low-density boron/phosphorus. Patterns are drawn using the photomask, and the source and drain sides are heavily doped. A SiO_2 layer is grown on the wafer by using the rapid thermal annealing (RTA) process. A ferroelectric (HZO) layer is also deposited with the help of the atomic layer deposition process. Micro-sized source and drain terminals are finished by reactive ion etching. The nanowire structure is formed by the electron beam etching process. Ion implantation of the source and drain side is done, and after this, annealing is done to activate the dopants. Finally thermal evaporation process is used for making metal

contacts [246]. The fabrication steps of the proposed device are shown in Figure 5.15. Varying doping, gate work function, and temperature can have significant effects on the performance of the device. Doping can impact the polarization switching dynamics of the ferroelectric material, as well as the charge carrier transport across the nanowire channel [20]. Variations in the gate work function can influence the threshold voltage, the subthreshold swing, and the overall conductivity of the device [21]. Temperature variations can alter carrier mobility, scattering mechanisms, and interface states, thereby affecting the overall conductivity and switching behavior of the nanowire device [22].

5.2.5 Analytical Modelling

With the aid of the parabolic approximation method, the 2D Poisson's equation for cylindrical coordinates of a cylindrical nanowire is given as follows [184]:

$$\frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\phi_i(\rho,z)\right)+\frac{\partial^2}{\partial\rho^2}\left(\phi_i(\rho,z)\right)+\frac{\partial^2}{\partial z^2}\left(\phi_i(\rho,z)\right)=\frac{qN_A}{\varepsilon_{Si}} \tag{5.6}$$

where $\phi_i(\rho, z)$ is the electric potential in the channel region, ρ is the radius of the nanowire, z is the length coordinate along the channel region, ε_{Si} is the permittivity of silicon, and the doping concentration is denoted by N_A. The solution of the equation (5.6) can be assumed as a combination of solutions of 1D Poisson's equation and 2D Laplace equation, respectively:

$$\phi_i(\rho,z)=A_i(\rho)+B_i(\rho,z) \tag{5.7}$$

The channel potential is obtained by applying the following boundary conditions:

$$\text{I.}\quad \phi_i(\rho,z)|_{\rho=0}=\phi_o(z) \tag{5.8}$$

$$\text{II.}\quad \phi_i(\rho,z)|_{\rho=\frac{t_{Si}}{2}}=\phi_s\left(\frac{t_{Si}}{2},z\right) \tag{5.9}$$

$$\text{III.}\ \frac{\partial\phi_i(\rho,z)}{\partial\rho}\Big|_{\rho=0}=0 \tag{5.10}$$

$$\text{IV.}\ \frac{\partial\phi_i(\rho,z)}{\partial\rho}\Big|_{\rho=\frac{t_{Si}}{2}}=\vartheta_i\left(V_{gs}-V_{fbi}-\phi_i\left(\rho=\frac{t_{Si}}{2},z\right)\right) \tag{5.11}$$

$$\text{V.}\quad \phi_1(\rho,0)=V_{bi} \tag{5.12}$$

$$\text{VI.}\ \phi_2(\rho,L_1+L_2)=V_{bi}+V_{ds} \tag{5.13}$$

VII. Surface potential at the interface of both gates is continuous:

$$\phi_1(\rho,L_1)=\phi_2(\rho,L_2) \tag{5.14}$$

VIII. $$\left.\frac{\partial \phi_1(\rho,z)}{\partial \rho}\right|_{z=L_1} = \left.\frac{\partial \phi_1(\rho,z)}{\partial \rho}\right|_{z=L_1+L_2} \quad (5.15)$$

where, $\vartheta_i = \frac{C_{oxeff}}{\varepsilon_{Si}}$ and $C_{oxeff} = \frac{2\varepsilon_{ox}}{t_{Si}\, ln\left(1+\left(\frac{2t_{ox}}{t_{Si}}\right)\right)}$

i=1 represents the work function for Gate 1 and i=2 for Gate 2. The surface potential (ϕ_s), flat-band voltage (V_{fbi}), ferroelectric layer (V_{fe}), oxide layer (V_{ox}), and flat-band voltage combine to form the total applied gate voltage:

$$V_{gs} = V_{fe} + V_{ox} + V_{fbi} + \phi_s \quad (5.16)$$

where, $V_{ox} = \frac{Q}{C_{ox}}$.

The negative capacitance offered by the ferroelectric layer is employed by using the L-K equation [47] according to which the Gibbs free energy (U) is represented as follows:

$$U = \alpha t_{fe} Q^2 + \beta t_{fe} Q^4 + \gamma t_{fe} Q^6 - V_{fe} Q \quad (5.17)$$

The voltage drops across the ferroelectric layer is obtained from the minima of U:

$$V_{fe} = 2\alpha t_{fe} Q + 4\beta t_{fe} Q^3 + 6\gamma t_{fe} Q^5 \quad (5.18)$$

α, β, and γ are the Landau parameters determined by the material properties particular to HZO [247]. Q represents the total charge density over the entire channel and is expressed as follows [248]:

$$Q = qN_A t_{Si}\left\{1 - \left(\frac{e^{\frac{(\phi_o - V)}{V_t}}}{2}\right)\sqrt{\frac{\pi V_t}{\phi_o(z) - \phi_s(z)}}\right\} \quad (5.19)$$

The gate metal consists of two metals with distinct work functions. To solve (5.6), the parabolic approximation is utilized and given by:

$$A_i(\rho) = X_{0i} + X_1\rho + X_2\rho^2 \quad (5.20)$$

Substituting (5.20) in (5.6) and using the boundary conditions, we obtain:

$$X_{01} = V_{gs} - V_{fb1} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\vartheta_i}\right) \quad (5.21)$$

$$X_{02} = V_{gs} - V_{fb2} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\vartheta_i}\right) \tag{5.22}$$

where X_1=0 and X_2=$qN_A/4\varepsilon_{Si}$.

The 2D Laplace equation is given as:

$$B_i(\rho, z) = \begin{bmatrix} B_1(\rho, z) for\ 0 < z < L_1 \\ B_2(\rho, z) for\ L_1 < z < L_1 + L_2 \end{bmatrix} \tag{5.23}$$

$$B_1(\rho, z) = \sum_{n=1}^{\infty} J_n(\zeta_n \rho)[P_n e^{\zeta_n z} + Q_n e^{-\zeta_n z}] \tag{5.24}$$

$$B_2(\rho, z) = \sum_{n=1}^{\infty} J_n(\zeta_n \rho)[R_n e^{\zeta_n z} + S_n e^{-\zeta_n z}] \tag{5.25}$$

The coefficients are calculated in the same way as in [184]. J_n is the Bessel function and ζ_n is the eigenvalue.

$$J_n = \frac{C_{ox}}{\zeta_n \varepsilon_{Si}} J_0 \tag{5.26}$$

The final solution of (5.6) can now be expressed as:

$$\phi_1(\rho, z) = V_{gs} - V_{fb1} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\zeta_1} - \rho^2\right) + \sum_{n=1}^{\infty} J_n(\zeta_n \rho)[P_n e^{\zeta_n z} + Q_n e^{-\zeta_n z}] \tag{5.27}$$

$$\phi_2(\rho, z) = V_{gs} - V_{fb2} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\vartheta_i}\right) + \sum_{n=1}^{\infty} J_n(\zeta_n \rho)[R_n e^{\zeta_n z} + S_n e^{-\zeta_n z}] \tag{5.28}$$

The electric field E_i for different regions is formulated as:

$$E_i(\rho, z) = -\frac{\partial \phi_i(\rho, z)}{\partial z} \tag{5.29}$$

The drain to source current for the proposed structure is given as [20]:

$$I_{ds} = \begin{bmatrix} I_{gidl} \ for \ -1.0V \le V_{gs} \le 0 \\ I_{sub} \ for \ 0 \le V_{gs} \le V_{th} \\ I_{lin} \ for \ V_{th} \le V_{gs} \le V_{sat} \\ I_{sat} \ for \ V_{sat} \le V_{gs} \le 1.0V \end{bmatrix} \quad (5.30)$$

Where V_{th} is the threshold voltage.

The GIDL (Gate-induced drain leakage) current in a cylindrical nanowire transistor is given by the following equation:

$$I_{gidl} = AE_i{}^2\left(\frac{t_{Si}}{2}, L_1 + L_2\right) exp\left[\frac{-B}{E_i\left(\frac{t_{Si}}{2}, L_1 + L_2\right)}\right] \quad (5.31)$$

where, $A = \frac{q^2 m_r^{0.5}}{18\pi h^2 E_g^{1.5}}$ $B = \frac{\pi m_r^{0.5} E_g^{1.5}}{\sqrt[2]{2}qh}$, $m_r = 0.2m_o$

where h is Planck's constant, E_g is the energy band gap, m_r depicts the effective mass, and m_0 depicts the rest mass of the electron. The subthreshold current, I_{sub} is given by:

$$I_{sub} = \frac{t_{si}\pi\mu kT\eta_i{}^{1-e^{\frac{-V_{ds}}{V_T}}}}{\int_0^{L_1+L_2} \frac{1}{\int_0^{\frac{t_{si}}{2}} e^{\frac{\phi_i(\rho,z)}{kT}}}} \quad (5.32)$$

Here, μ represents the electron mobility, and k depicts Boltzmann's constant. The linear region current, I_{lin} is given as:

$$I_{lin} = \frac{t_{si}\pi\mu C_{oxeff1}E_c}{(E_c L + V_{ds})}\left[(V_{gs} - V_{th})V_{ds} - V_{ds}^2\right] \quad (5.33)$$

Saturation region current is obtained by substituting $V_{ds}=V_{dsat}=V_{gs}-V_{th}$ and expressed as:

$$I_{sat} = \frac{t_{si}\pi\mu C_{oxeff2}}{\left(1 + \frac{V_{dsat}}{E_c L}(L - L_{sat})\right)}\left[\xi(V_{gs} - V_{th})V_{ds} - V_{ds}^2\right] \quad (5.34)$$

where L_{sat} is the characteristic length, E_c is the conduction band energy, and ξ is an empirical parameter, whose value is taken between 0 and 1. Equations 5.31,5.32, 5.33 and 5.34 represent the current model in different regions, such as the subthreshold, linear, and saturation regions. Subthreshold conduction is exploited in this device to process or operate without fully turning ON or OFF. The linear current is important because it indicates how effectively the device can modulate current flow based on changes in the gate voltage. Saturation current represents the maximum current that the device can deliver while operating in the saturation region. Understanding and controlling these currents are crucial for optimizing the performance of nanowire FETs

in various applications, including digital and analog circuits, sensors, and low-power devices.

5.2.6 Results and Discussion

5.2.6.1 Comparative simulation of C-NW-FET and C-FE-DM-NW-FET

With V_{GS} = 0.01 V and V_{DS} = 1.0 V for (a) C-NW FET and (b) C-FE-DM-NW-FET, the contour plots in Figure 5.16 show the hole concentration (/cm^3) at the channel center. Comparing the C-FE-DM-NW-FET to the C-NW FET, the contour clearly shows that the C-FE-DM-NW-FET has a lower hole concentration near the center. The low concentration of holes leads to low BTBT because of the alteration in capacitance due to the ferroelectric layer, which results in lower GIDL.

The hole velocity contour of C-NW FET and C-FE-DM-NW-FET at V_{GS} = 0.01 V and V_{DS} = 1.0 V is displayed in Figure 5.17 (a) and (b), respectively. It can be assessed from Figure 5.17 (a) and (b) that the velocity of holes in C-FE-DM-NW-FET is higher in the channel region, whereas the hole velocity in C-NW FET can be seen in the source and drain regions. It is due to the presence of a ferroelectric layer between the gate and oxide, which alters the capacitance due to the inclusion of the C_{fe} layer. Low gate voltage has been used in this Figure to observe the band-to-band tunnelling.

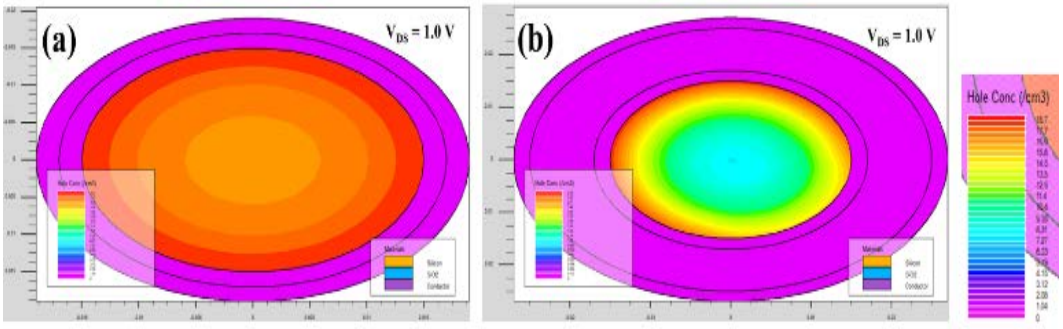


Figure 5.16 Hole Concentration of (a) C-NW FET, (b) C-FE-DM-NW-FET.

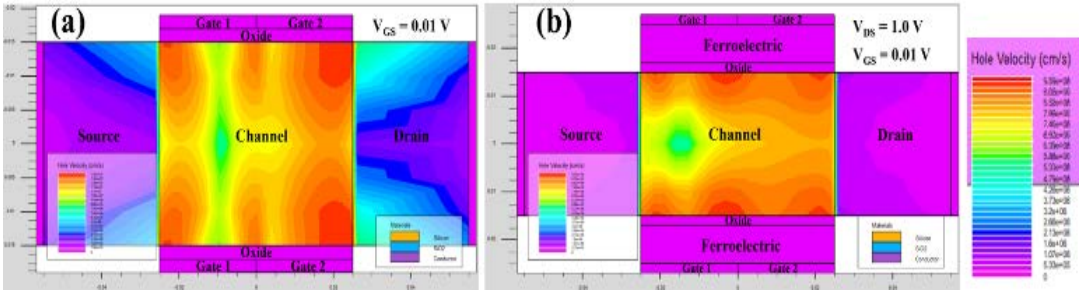


Figure 5.17 Hole Velocity of (a) C-NW FET, (b) C-FE-DM-NW-FET.

BTBT is a crucial reliability metric for assessing the effectiveness of equipment. The valence and conductance bands overlap in the OFF state, causing electrons to tunnel between them. When the BTBT is switched off, it causes a considerable increase in leakage current. As a function of location along the channel length, Figure 5.18 shows

the variation in band energy. The (a) C-NW FET and (b) C-FE-DM-NW-FET's valence energy band (VBE) and conduction energy band (CBE), at V_{DS} = 1.0 V and 0.0 V, respectively, have been securely established.

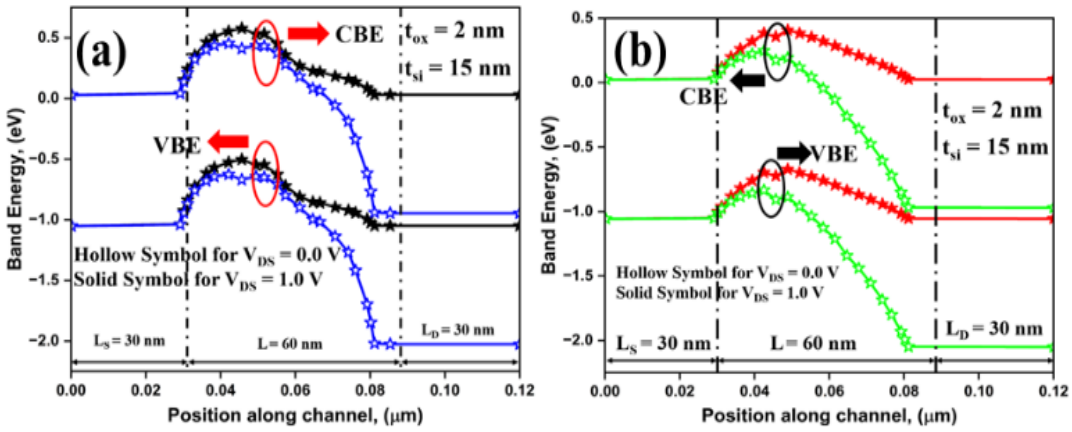


Figure 5.18 Band-to-band Tunneling in (a) C-NW FET and (b) C-FE-DM-NW-FET.

Figure 5.18 (b) illustrates how C-FE-DM-NW-FETs have a decreasing band energy at the drain end because of the presence of a dual metal gate having a lower work function gate on the drain side. This drop has also happened as a result of the ferroelectric material and the ferroelectric capacitance.

Tunnelling distance is defined as the distance electrons cross when migrating from one energy band to the other at V_{DS} = 1.0 V [168]. Figure. Figure 5.19 depicts the tunnelling distance of a C-NW FET and a C-FE-DM-NW-FET at 50 and 60 nm, respectively. The proposed C-FE-DM-NW-FET has demonstrated promising tunnelling distance findings for both channel lengths. C-NW FETs with 50 nm channel length have a tunnelling distance of 0.011 µm, while 60 nm devices have a tunnelling distance of 0.006 µm. Whereas a C-FE-DM-NW-FET with a channel length of 50 nm has a tunnelling distance of 0.011 µm, a 60 nm device has a tunnelling distance of 0.004 µm. C-FE-DM-NW-FET has a 28% reduction in tunnelling distance when compared to a 60 nm channel length. This decrease in tunnelling distance is due to the existence of a ferroelectric layer between the oxide and the gate terminal.

The potential contour of C-NW FET and C-FE-DM-NW-FET at V_{GS} = 0.01 V and V_{DS} = 1.0 V is displayed in Figure 5.20 (a) and (b), respectively. Comparing the C-FE-DM-NW-FET to the C-NW FET, the contour clearly shows that the C-FE-DM-NW-FET has higher potential across the whole channel. This is because of the ferroelectric layer and because of the presence of a lower work function gate at the drain side. Figure 5.20 (d) depicts the variation of surface potential at V_{DS} = 1.0 V and V_{GS} = 0.01 V with the position of the channel for C-NW FET and C-FE-DM-NW-FET. From Figure 5.18 (d), it can be concluded that the surface potential of the C-FE-DM-NW-FET device changes at the center of the channel; this is because the capacitance is altered. The capacitance of C-FE-DM-NW-FET is connected in series:

$$\frac{1}{C_{eff}} = \frac{1}{C_{fe}} + \frac{1}{C_{ox}} + \frac{1}{C_{ch}} \tag{5.35}$$

where C_{eff} is the total capacitance, C_{fe} is the capacitance of the ferroelectric layer, C_{ox} is the capacitance of the oxide layer, and C_{ch} is the channel capacitance.

$$q = CV \tag{5.36}$$

where q is the charge, C is the total capacitance, and V is the potential. According to (31), as the C_{eff} decreases in C-FE-DM-NW-FET, the potential increases.

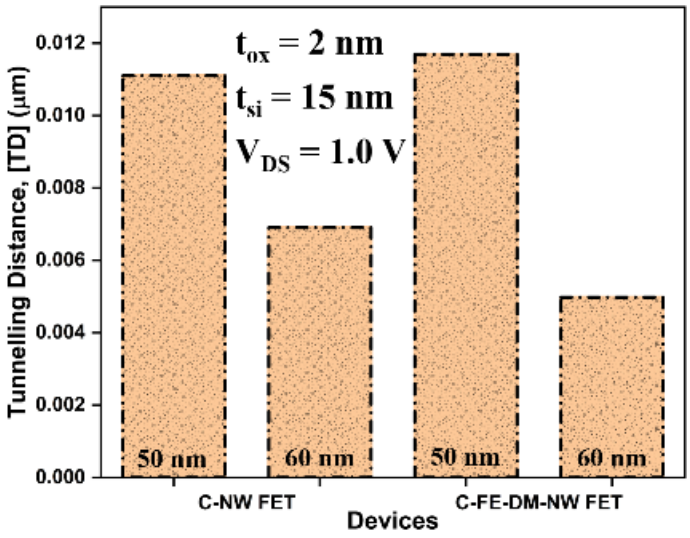


Figure 5.19 Tunnelling Distance for various device designs.

Figure 5.21 (a) illustrates the electric field (E_z) for different channel lengths (L = 50 nm and 60 nm) for C-NW FET and C-FE-DM-NW-FET. An abrupt change in E_z can be observed in the graph of C-NW FET because of the dual metal gate, which has a lower work function at the drain side. Figure 5.21 (b) demonstrates how the GIDL current varies with V_{GS} in various device topologies. This clearly shows that the GIDL current of a C-FE-DM-NW-FET with a channel length of 50 nm has fallen from an order of 10^{-8} A to an order of 10^{-12} A. In the case of a channel length of 60 nm, the GIDL current of a C-FE-DM-NW-FET has lowered from an order of 10^{-8} A to an order of 10^{-15} A.

Subthreshold leakage is a term used to describe the phenomenon known as GIDL. When the drain side is kept at a higher positive bias while the source side receives a moderate V_{GS}, this situation arises [23]. The reduction in OFF-state leakages was because a ferroelectric layer was put between the gate terminal and the oxide, which resulted in the production of many fewer hot carriers.

Figure 5.22 (a) illustrates the I_{GIDL} concerning different drain voltages for C-NW FET and C-FE-DM-NW-FET at different channel lengths. It can be concluded from the Figure 5.22 that C-FE-DM-NW-FET has lower I_{GIDL} at lower values of drain biases. This happens because of the lower work function of the gate on the drain side and because of the presence of the ferroelectric layer in this topology. Figure 5.22 (b) contains the comparison of I_{GIDL} at various higher values of temperature. In this, the presence of ferroelectric material and ferroelectric capacitance reduced the BTBT, which in turn reduces the I_{GIDL} at higher values of temperature for C-FE-DM-NW-FET

at both 50 nm and 60 nm when compared with C-NW FET at 50 nm and 60 nm. To evaluate how temperature affects any physical quantity, the Arrhenius plot is utilized. Since its slope controls activation energy, understanding the Arrhenius plot is crucial [224].

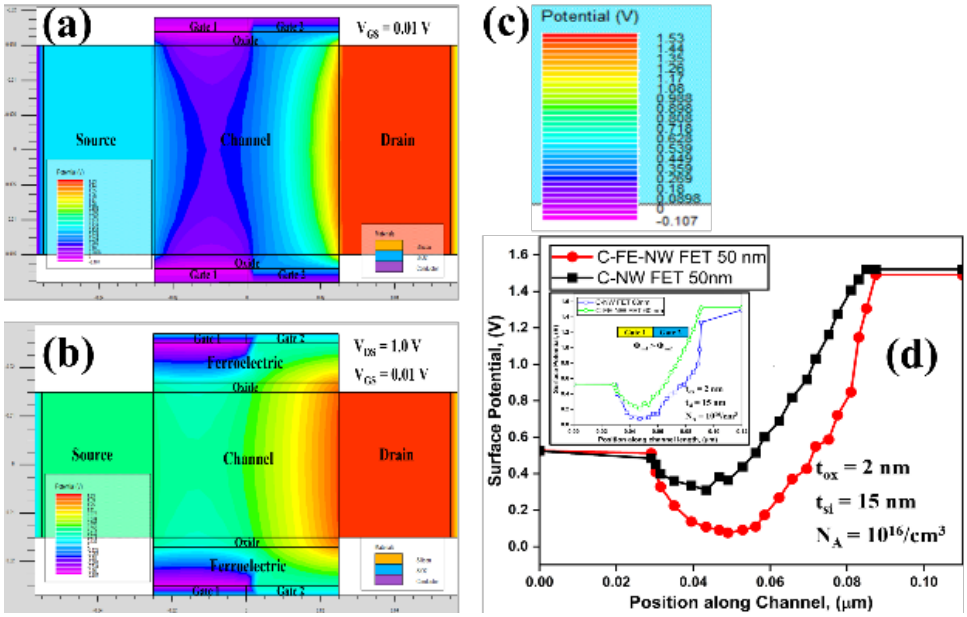


Figure 5.20 Potential contour of (a) C-NW FET, (b) C-FE-DM-NW-FET at V_{GS} = 0.01 V and V_{DS} = 1.0 V, (c) Scale of Potential contour, and (d) Surface Potential at V_{GS} = 0.01 V and V_{DS} = 1.0 V.

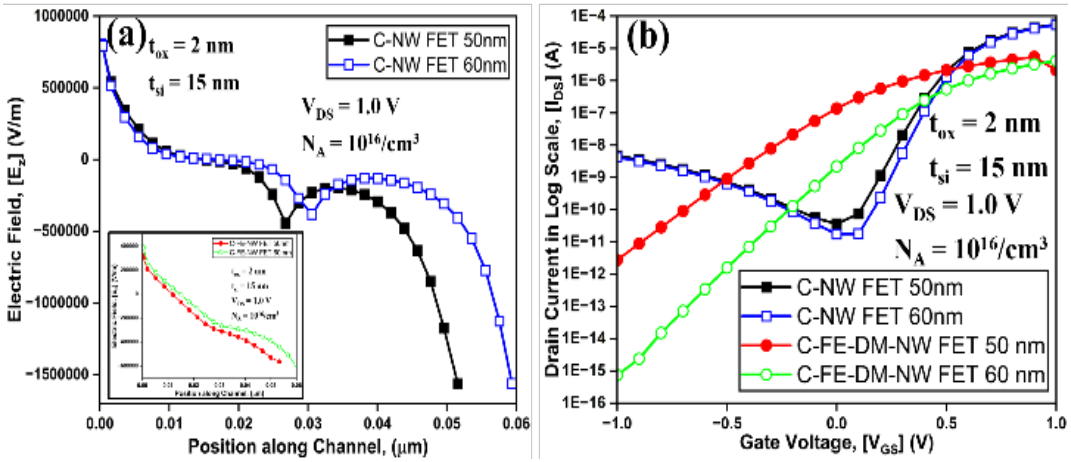


Figure 5.21 (a) Electric Field for C-NW FET, C-FE-DM-NW-FET at V_{GS} = 0.01 V and V_{DS} = 1.0 V, and (b) I_{GIDL} for C-NW FET, C-FE-DM-NW-FET.

The Arrhenius curve for GIDL current with temperature shift (1/kT) at V_{GS} = -1.0 V is shown in Figure 5.22 (c). The presence of ferroelectric material between the gate terminal and oxide can be shown in Figure 5.22 to explain why the I_{GIDL} of C-FE-DM-NW-FET is lower than that of C-NW FET.

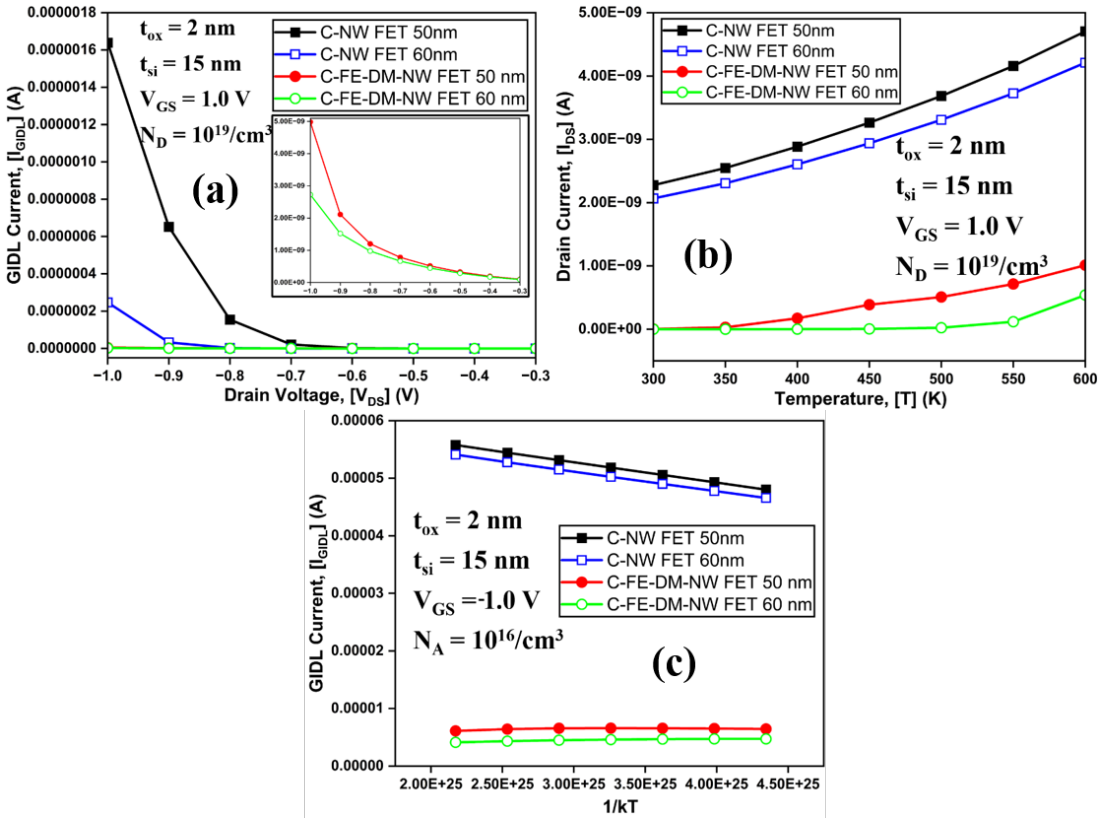


Figure 5.22 (a) I_{GIDL} changes along V_{DS}, (b) I_{GIDL} changes along with Temperature, and (c) Arrhenius Plot for different devices.

5.2.6.2 Analytical Results and Validation

Figure 5.23 (a) shows the analytical results of surface potential against position along the channel for different channel lengths of C-FE-DM-NW-FET. The analytical findings are in good agreement with the numerical simulations, as evident from the results, which verify the model. Figure 5.23 (b) depicts the analytical data on the variation in the electric fields of C-FE-DM-NW-FET at channel lengths of 50 nm and 60 nm. The electric field is obtained from the derivative of the surface potential as shown in (15). The analytical results coordinate with the simulated findings precisely. Figure 5.23 (c) represents analytically the GIDL current (I_{GIDL}) of a C-FE-DM-NW-FET and its validation with the simulated results. The I_{GIDL} is calculated with the help of (16), which clearly shows the dependence of I_{GIDL} on channel lengths. The analytical results coordinate with the simulated findings precisely.

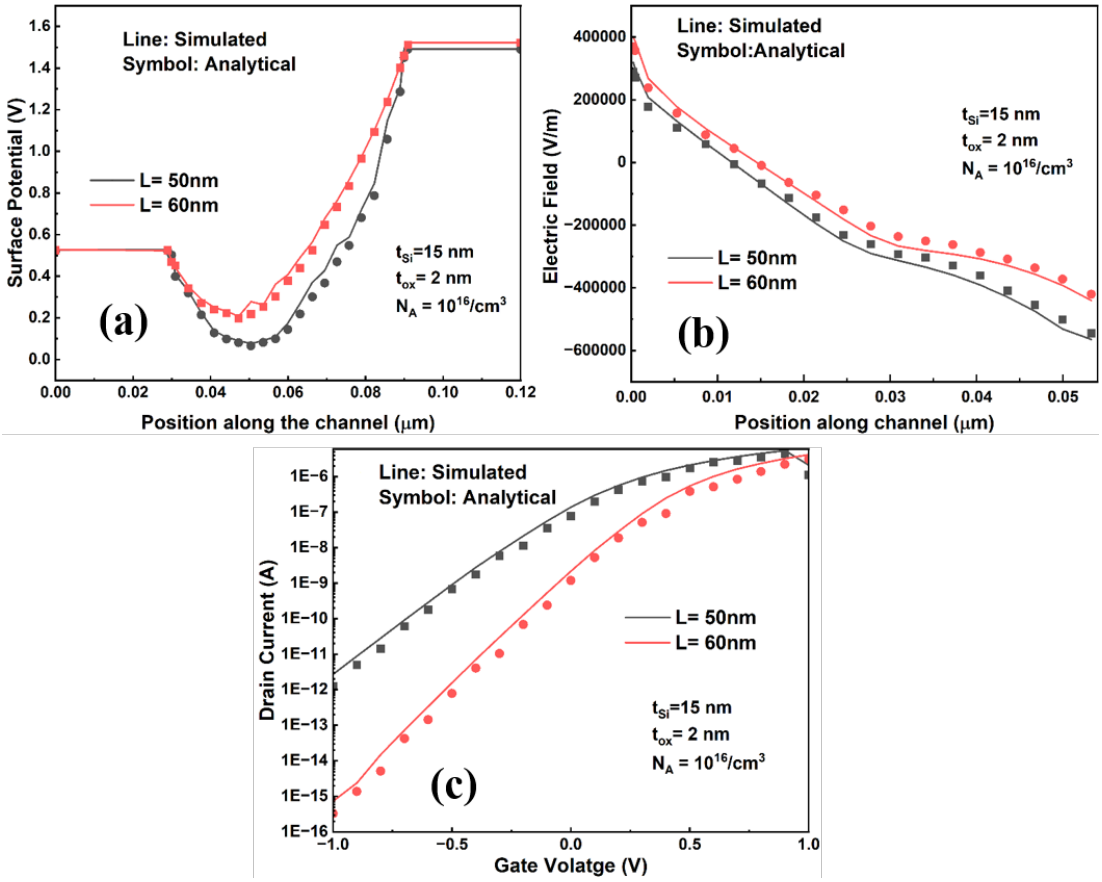


Figure 5.23 Analytical result of (a) Surface Potential at V_{GS} = 0.01 V and V_{DS} = 1.0 V, (b) Electric Field for C-NW FET, C-FE-DM-NW-FET at V_{GS} = 0.01 V and V_{DS} = 1.0 V, and (c) I_{GIDL} for C-NW FET, C-FE-DM-NW-FET.

5.2.7 Comparative Analysis

On comparing the conventional Cylindrical Nanowire FETs (NW FETs) and Negative Capacitance Nanowire FETs (NC-NW FETs) with the proposed Cylindrical Ferroelectric Dual Metal Nanowire FET (C-FE-DM-NW-FET), it is observed that the proposed C-FE-DM-NW-FET demonstrates superior performance. The GIDL of C-FE-DM-NW-FET is 10^{-15} A, outperforming 10^{-14} A of NC-NW FET and significantly surpassing the conventional FET at 10^{-8} A. The subthreshold slope remains below 15 mV/decade, compared to 13-14 mV/decade in NC-NW FET and ~60 mV/decade in conventional NW FET. Both NC-NW FET and C-FE-DM-NW-FET exhibit reduced tunnelling distances relative to conventional devices; the latter achieves this through spatially tuned gate modulation rather than uniform control, enhancing leakage suppression without compromising ON state performance. In this, the proposed device delivers the highest ON state stability among other architectures. C-FE-DM-NW-FET achieves an optimal trade-off between OFF state leakage control and strong ON state current, making it a prime candidate for high-performance and low-power electronics applications.

5.2.8 Challenges and Considerations

While the cylindrical ferroelectric dual metal nanowire FET (C-FE-DM-NW-FET) offers remarkable theoretical and simulated advantages, practical implementation still poses several challenges.

A fundamental limitation arises from capacitance matching and stability, since the effectiveness of the device in the negative capacitance (NC) regime relies heavily on accurate matching between the ferroelectric layer capacitance and the underlying gate oxide capacitance. Any deviation from this delicate balance can result in operational instability, the emergence of undesirable hysteresis and a reduction in voltage amplification efficiency [249].

Another critical difficulty involves fabrication complexity, specifically in designing of dual metal gate with a specific work function across nanometric dimensions. The device consistency, scalability and repeatability are dependent on the controlled metal deposition, high precision lithography and reliable defect free ferroelectric integration across the gate [250].

Moreover, the issue of material and interface reliability remains unsolved, as long-term material reliability of HZO is still an ongoing research topic, and hence, it's an area of concern. The presence of trap charges, defect states and charge accumulation at the interface of oxide and semiconductor or oxide and ferroelectric junctions can introduce threshold voltage variability, reduced endurance and degrade performance with time [251].

A further concern is scalability for mass production, since the integration of dual metal gates in high-volume manufacturing lines requires aligning with CMOS-compatible processes, including etching, metal deposition, and planarization, all while ensuring that the ferroelectric phase stability of HZO is preserved during the processing [100].

Finally, modelling limitations continue to constrain predictive accuracy. Current device simulations often are based on the idealized assumptions such as smooth interfaces, ideal ferroelectric switching and uniform material properties. The 3D simulation provides valuable insight, into electrostatic behavior and performance scaling, these models require experimental validations, to ensure that they accurately capture non-ideal effects, parasitic interactions and variability encountered in fabricated devices [252].

Collectively, these challenges highlight the need for advanced interface engineering, process innovations and refined compact models to transition the C-FE-DM-NW FET from promising simulations to robust, manufacturable technology.

5.3 Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor (CGEF-NW FET)

5.3.1 Working Principle and Operating Mechanism

The Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor (CGEF-NW FET) is an evolution in the field of transistors in which a ferroelectric material layer is stacked on the oxide layer so that the device can exhibit the negative capacitance effect. The presence of dual metal gates in this architecture helps in better electrostatic control of the channel. This architecture offers a reduction in leakage current, suppression of short-channel effects (SCEs), and a reduction in subthreshold slope.

The CGEF-NW FET operates on three synergistic mechanisms:

5.3.1.1 Negative Capacitance Effect

As in CGEF-NW FETs, the ferroelectric HZO layer exhibits a region of negative differential capacitance in its polarization-electric field curve, governed by Landau-Khalatnikov (L-K) theory. This leads to internal voltage amplification and enhances the channel potential for a given gate bias. The total gate voltage (V_{GS}) is partitioned among the voltage at the ferroelectric layer (V_{FE}), the voltage at the gate oxide (V_{ox}), and the semiconductor surface potential (Φ_s) for a given V_{GS}. At a given V_{GS}, when ferroelectric capacitance attains a negative value, it amplifies the surface potential. This amplification in surface potential enables stronger channel inversion at lower gate voltages, thereby reducing the turn-on voltage and suppressing the subthreshold slope [111].

5.3.1.2 Dual Metal Gate Modulation

The inclusion of two different work functions within the gate creates a longitudinal potential asymmetry. This asymmetry allows localized tuning of the electric field across the channel. The higher work function near the drain side raises the potential barrier, which will help in suppressing band-to-band tunnelling (BTBT) and gate-induced drain leakage (GIDL). The lower work function of the gate near the source side enhances carrier injection, thereby improving the ON-state performance of the device. The dual metal configuration enables better channel control and mitigates leakage current [253].

5.3.1.3 Temperature Sensitive Electrostatics

Temperature is a key factor affecting the ferroelectric polarization of the device. Across a wide range of temperatures ranging from 250 K to 400 K, the proposed device maintains its negative capacitance behaviour, owing to the thermal stability of HZO [147], [175]. The internal field of the device is affected as the temperature rises, and a reduction in polarization is observed without eliminating the NC effect. The total gate voltage is expressed as:

$$V_{GS} = V_{FE} + V_{ox} + \Phi_s \tag{5.37}$$

Where temperature affects both V_{FE} and Φ_s, requiring optimization of channel potential for leakage suppression at higher thermal loads.

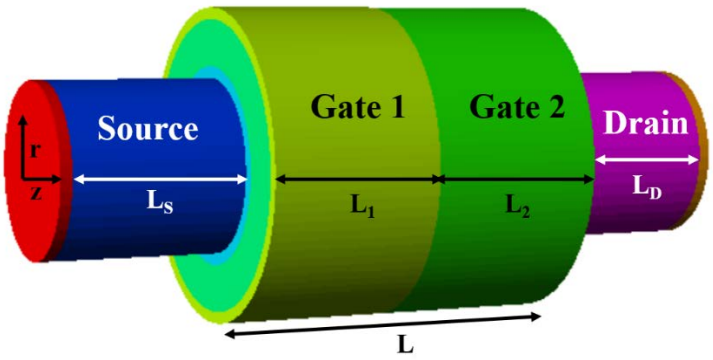
5.3.2 Device Architecture

The suggested CGEF-NW-FET device is the focal point of this manuscript. This symmetrical twin metal gate arrangement includes a layer of ferroelectric material in the gate stack. Identical gate lengths of 30 nm and thicknesses of 2 nm are a distinctive feature of the CGEF-NW-FET structure. The thickness of the ferroelectric material (HZO) is t_{fe} (8 nm), whereas the thickness of the single dielectric oxide layer is t_{ox} (2 nm). The visual representations of the 3-D and 2-D schematics of the proposed structure are depicted in Figure 5.24 (a) and (b). The proposed device has a radius of 15 nm, and is doped at both the source and drain sides with N_D ($10^{19}/cm^3$), and is configured as an n-type semiconductor.

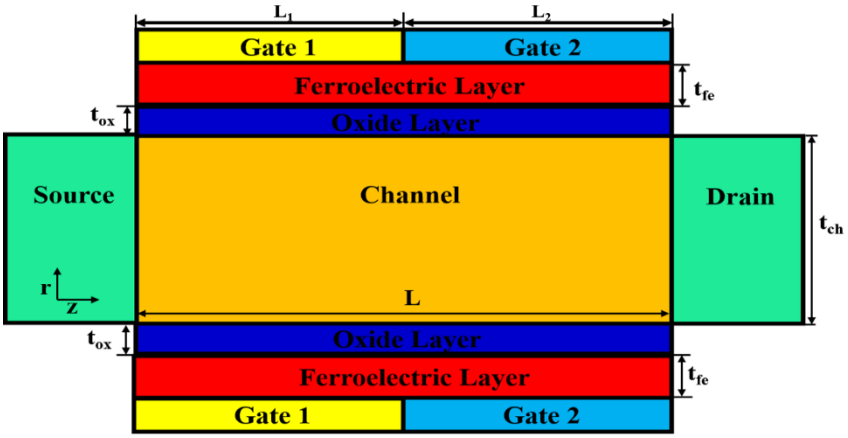
When the device is operating in the negative capacitance (NC) area, the energy bands in the channel-normal direction are shown in Figure 5.24 (c). The doping in the channel region is P-type, with an inversion and downward curvature. The energy band gap, represented by the symbols E_C/E_V, separates the conduction and valence bands, respectively, and shapes the energy band structure. The intrinsic Fermi level, E_i, is also displayed. Throughout this paper, molybdenum has been used as the gate material in a variety of combinations. The decision to use molybdenum is explained by its influence on the work function of the gate metal in various settings, an effect brought on by the adjustment of nitrogen implantation. This modification, in turn, alters the threshold voltages of both structures. The detailed structural characteristics for the proposed and the conventional structures are given in Table 5.7.

In this work, Quantum effects have been discarded since they do not appear to have any appreciable influence on the I_D-V_G characteristics for channels as short as 20 nm [184].

Complete description of the simulation models used. Table 5.8 summarizes the properties of the ferroelectric material HZO. To ensure the correctness of our efforts, we link our setup with previously known research, as shown in Figure 5.25. Figure 5.25 (a) shows the alignment with the calibration of the nanowire FET [24], whereas (b) shows the alignment with the ferroelectric FET calibration. Especially noteworthy are the difficulties and high costs associated with this design's manufacturing process. Quantum and ballistic transport phenomena are excluded from consideration in this analysis, as these effects predominantly manifest in devices with ultra-scaled channel dimensions below 30 nm and nanowire radii on the order of 5 nm. The exclusion is justified by the fact that such quantum mechanical and collision-free carrier transport mechanisms become significant only within these critical geometrical thresholds, where wave-particle duality and phase-coherent transport dominate charge carrier dynamics.



(a)



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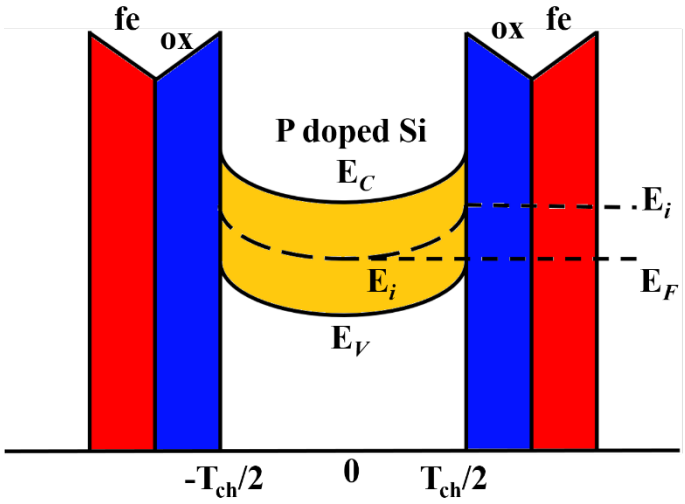

(c)

Figure 5.24 (a) 3-D schematics of CGEF-NW-FET, (b) 2-D schematics of CGEF-NW-FET, and (c) Energy Band of CGEF-NW-FET in NC Region.

TABLE 5.7: Structural Characteristics

Parameters	C-NW-FET	CGEF-NW-FET
Gate Thickness (t_g)	2 nm	2 nm
Channel Length (L)	60 nm	60 nm
Oxide Thickness (t_{ox})	2 nm	2 nm
Ferroelectric Thickness (t_{fe})	-----	8 nm
Channel Doping	$1x10^{16}/cm^3$	$1x10^{16}/cm^3$
Work Function (Φ_{m1})	5.0 eV	5.4 eV
Silicon Thickness (t_{si})	30 nm	30 nm
Work Function (Φ_{m2})	4.36 eV	4.4 eV
Length of S/D	30 nm	30 nm

TABLE 5.8: Ferroelectric Material Specifications

Parameters	Symbol	Values
Dielectric Constant	E	30
Coercive Field	E_c	1MV/cm
Remnant Polarization	P_r	$10\mu C/cm^2$

5.3.3 Simulation Setup

The ATLAS 3D TCAD simulation tool was employed to perform the numerical simulations [21]. The simulator was employed with a suite of advanced physical models tailored for nanowire ferroelectric FETs. The Newton-Gummel iterative approach was used for solving the carrier transport equations. This approach is well known for its effectiveness in handling the nonlinearities associated with semiconductor device modelling [22]. The models are chosen based on their relevance to the proposed device structure.

The Concentration-Dependent Mobility (CVT) model [254] considers the degradation of charge carrier mobility due to impurity scattering in highly doped regions. This model enables accurate estimation of drift current by adjusting mobility as a function of electric field and doping concentration. Shockley Read Hall (SRH) recombination model [219] accounts for the generation and recombination of carriers through mid-gap defect states. This model is used for simulating trap-assisted processes in semiconductor materials, which have a significant influence on OFF-state leakages and subthreshold behavior in nanoscale devices.

TABLE 5.9: Model Details

Models	Details
FERRO	Allows the ferroelectric permittivity model to be used.
SRH	Used to incorporate the carrier recombination effect
BBT.STD	Used to measure the tunnelling impact of charge carriers
FERMI	Carrier concentrations are lower in extensively doped areas.
CVT	Complete model including N, T, and E effects. Good for non-planar devices
LK	It enables the interface between the gate and the oxide layer.

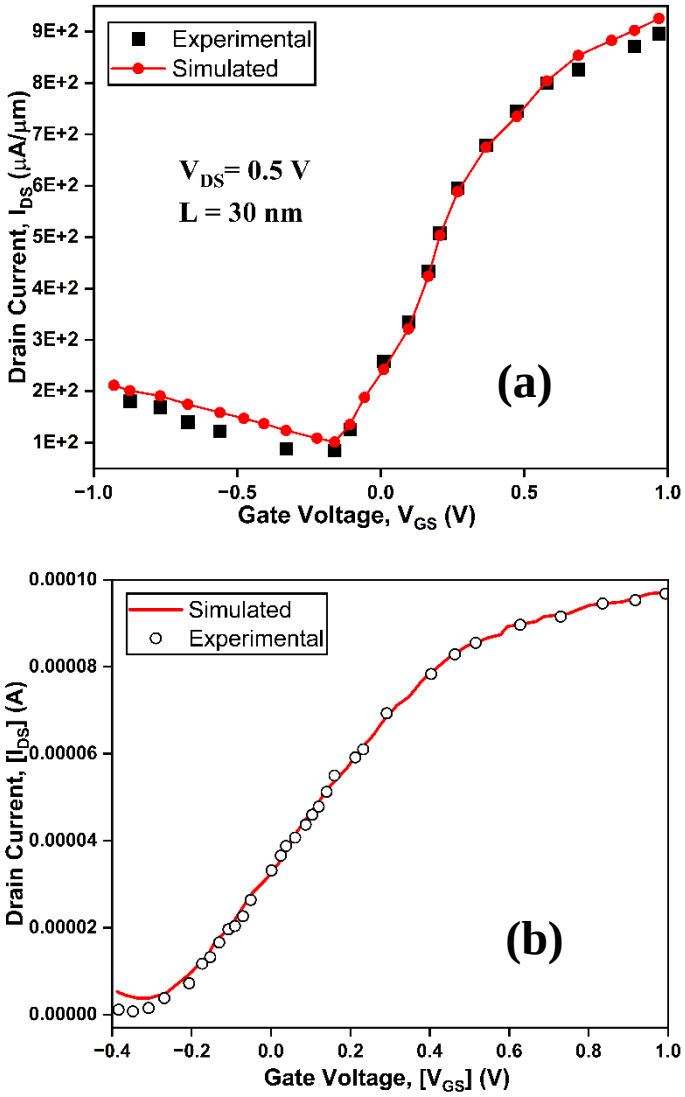

Figure 5.25 Comparison with experimental data showing (a) transfer characteristics of nanowire FET, (b) transfer characteristics of ferroelectric FET [9][10].

5.3.4 Fabrication

The substrate layer of silicon on a silicon-on-insulator (SOI) wafer is coated by a dielectric layer, and silicon is stacked on top. Initial low-density boron/phosphorus doping is applied to the top silicon layer. The photomask is used to generate patterns, and the source and drain ends are extensively doped. RTA, or rapid thermal annealing, is a method used for developing a SiO_2 layer on a wafer. With the aid of the atomic layer deposition method, a ferroelectric (HZO) layer is also deposited. Reactive ion etching is used to finalize the micro-sized source and drain terminals. The method of electron beam etching produces nanowire structures. Ion implantation is performed on the source and drain sides, followed by annealing to activate the dopants. Finally, metal contacts are created via a thermal evaporation technique [246]. Figure 5.26 depicts the manufacturing stages for the proposed device.

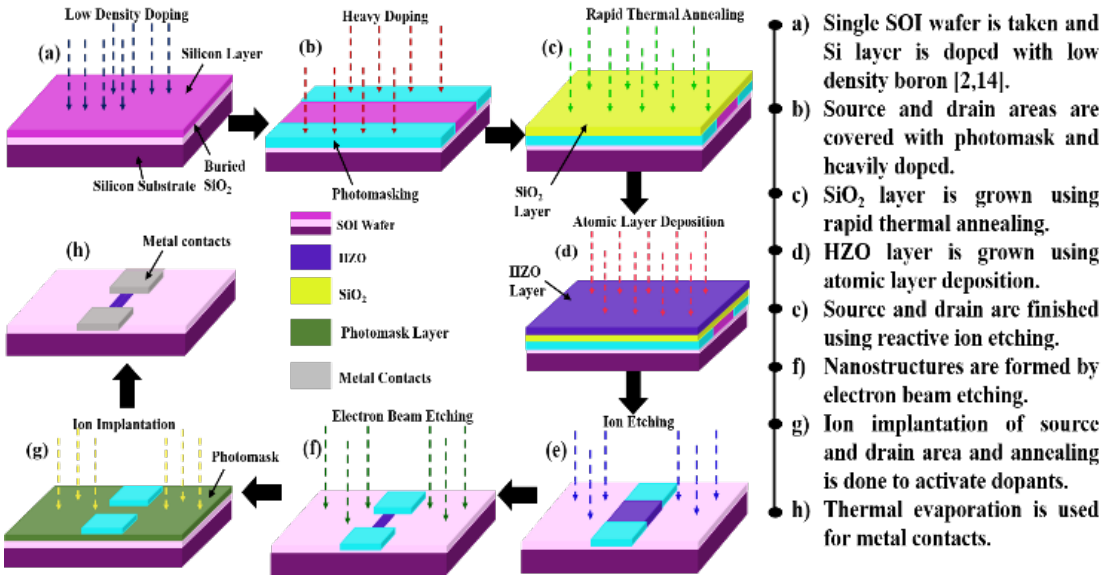

Figure 5.26 Fabrication steps of CGEF-NW-FET

5.3.5 Analytical Modelling

Utilizing the parabolic approximation technique, the following is the 2D Poisson's equation for the cylindrical nanowire [175]:

$$\frac{1}{\rho}\frac{\partial}{\partial\rho}\left(\phi_i(\rho,z,T)\right)+\frac{\partial^2}{\partial\rho^2}\left(\phi_i(\rho,z,T)\right)+\frac{\partial^2}{\partial z^2}\left(\phi_i(\rho,z,T)\right)=\frac{qN_A}{\varepsilon_{Si}} \tag{5.38}$$

The electric potential in the channel region is represented by $\phi i\ (\rho,\ z)$, where ρ is the nanowire's radius, z axis is the length along the channel region, ε_{Si} denotes the silicon's permittivity, and N_A stands for the doping concentration. One may assume that the solution to equation (1) is a combination of the answers to the 1D Poisson's equation and the 2D Laplace equation, respectively:

$$\phi_i(\rho,z,T)=A_i(\rho,T)+B_i(\rho,z,T) \tag{5.39}$$

The channel potential is obtained by applying the following boundary conditions:

$$\text{I.}\quad \phi_i(\rho,z,T)|_{\rho=0}=\phi_o \tag{5.40}$$

$$\text{II.}\quad \phi_i(\rho,z,T)|_{\rho=\frac{t_{Si}}{2}}=\phi_s\left(\frac{t_{Si}}{2},z,T\right) \tag{5.41}$$

$$\text{III.}\quad \frac{\partial\phi_i(\rho,z,T)}{\partial\rho}\Big|_{\rho=0}=0 \tag{5.42}$$

$$\text{IV.}\quad \frac{\partial\phi_i(\rho,z,T)}{\partial\rho}\Big|_{\rho=\frac{t_{Si}}{2}}=\vartheta_i\left(V_{gs}-V_{fbi}-\phi_i\left(\rho=\frac{t_{Si}}{2},z,T\right)\right) \tag{5.43}$$

Here, $\vartheta_i = \frac{C_{eff}}{\varepsilon_{Si}}$ and $\frac{1}{C_{eff}} = \frac{1}{C_{oxeff}} + \frac{1}{C_{feeff}}$

where $C_{oxeff} = \frac{2\varepsilon_{fe}}{t_{Si}\, ln\left(1+\left(\frac{2t_{fe}}{t_{Si}}\right)\right)}$ and $C_{feeff} = \frac{\varepsilon_{fe}\varepsilon_{Si}}{t_{fe}\varepsilon_{ox}+t_{ox}\varepsilon_{fe}}$

The total effective capacitance (C_{eff}) is the capacitance offered by both oxide and ferroelectric layer. ε_{fe} and ε_{ox} denotes the ferroelectric and oxide permittivity.

For Gate 1, the work function is represented by i=1, and for Gate 2, by i=2.

V. $\phi_1(\rho, 0, T) = V_{bi}$ (5.44)

VI. $\phi_2(r, L_1 + L_2, T) = V_{bi} + V_{ds}$ (5.45)

VII. At the junction of both gates, the surface potential is continuous:

$$\phi_1(\rho, L_1, T) = \phi_2(\rho, L_2, T) \quad (5.46)$$

VIII. $$\frac{\partial\phi_1(\rho,z,T)}{\partial\rho}\Big|_{z=L_1} = \frac{\partial\phi_1(\rho,z,T)}{\partial\rho}\Big|_{z=L_1+L_2} \quad (5.47)$$

The impact of temperature on the device parameters has been analyzed using the following equations [255]:

$$\varepsilon_{si}(T) = 11.4 + (1 + 1.2 \times 10^{-4}T) \quad (5.48)$$

$$\eta_i(T) = 1.76 \times 10^{25}\left(\frac{T}{300}\right)^{\frac{3}{2}} exp\left(\frac{-qE_g(T)}{kT}\right) \quad (5.49)$$

$$E_g(T) = E_g(300) + \left(\frac{300^2}{300 + E_{g\alpha}} - \frac{T^2}{T + E_{g\beta}}\right) \quad (5.50)$$

where, $E_g(300)$ =1.08eV, $E_{g\alpha}$=4.73×10^{-4}eV/K, and $E_{g\beta}$=636K. The total applied gate voltage is sum of ferroelectric layer (V_{fe}), surface potential (ϕ_s), flat-band voltage (V_{fbi}) and oxide layer (V_{ox}):

$$V_{gs}(T) = V_{fe}(T) + V_{ox}(T) + V_{fbi}(T) + \phi_s(T) \quad (5.51)$$

where, $V_{ox} = \frac{Q(T)}{C_{ox}}$

The ferroelectric layer's negative capacitance is utilized through the application of the L-K equation [19], which gives the following representation of the Gibb's free energy (U):

$$U = \alpha(T)t_{fe}Q(T)^2 + \beta t_{fe}Q(T)^4 + \gamma t_{fe}Q(T)^6 - V_{fe}(T)Q(T) \quad (5.52)$$

The minima of U determine the voltage drop across the ferroelectric layer:

$$V_{fe}(T) = 2\alpha(T)t_{fe}Q(T) + 4\beta t_{fe}Q^3(T) + 6\gamma t_{fe}Q^5(T) \tag{5.53}$$

The material characteristics of HZO determine the landau parameters α, β, and γ [20]. Q reflects the overall charge density throughout the whole channel and is expressed as follows [256]:

$$Q(T) = qN_A t_{Si}\left\{1 - \left(\frac{e^{\frac{(\phi_o - V)}{V_t}}}{2}\right)\sqrt{\frac{\pi kT/q}{\phi_o(z) - \phi_s(z)}}\right\} \tag{5.54}$$

The gate metal is composed of two metals with different work functions. To solve (1), the parabolic approximation is utilized and given by:

$$A_i(\rho, T) = X_{0i} + X_1\rho + X_2\rho^2 \tag{5.55}$$

Utilizing the boundary conditions and substituting (5.55) in (5.38), the following expressions are obtained:

$$X_{01} = V_{gs} - V_{fb1} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\vartheta_i}\right) \tag{5.56}$$

$$X_{02} = V_{gs} - V_{fb2} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\vartheta_i}\right) \tag{5.57}$$

where X_1=0 and X_2=$qN_A/4\varepsilon_{Si}$.

The 2D Laplace equation is given as:

$$B_i(\rho, z, T) = \begin{bmatrix} B_1(\rho, z, T) for\ 0 < z < L_1 \\ B_2(\rho, z, T) for\ L_1 < z < L_1 + L_2 \end{bmatrix} \tag{5.58}$$

$$B_1(\rho, z, T) = \sum_{n=1}^{\infty} J_n(\zeta_n\rho)[P_n e^{\zeta_n z} + Q_n e^{-\zeta_n z}] \tag{5.59}$$

$$B_2(\rho, z, T) = \sum_{n=1}^{\infty} J_n(\zeta_n\rho)[R_n e^{\zeta_n z} + S_n e^{-\zeta_n z}] \tag{5.60}$$

The formula for the coefficients is the same as it is in [22]. ζn is the Eigen value, and Jn is the Bessel functions.

$$J_n = \frac{C_{ox}}{\zeta_n \varepsilon_{Si}} J_0 \tag{5.61}$$

Now, the ultimate solution to (5.38) is as follows:

$$\phi_1(\rho,z,T) = V_{gs} - V_{fb1} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\zeta_1} - \rho^2\right) + \sum_{n=1}^{\infty} J_n(\zeta_n\rho)[P_n e^{\zeta_n z} + Q_n e^{-\zeta_n z}] \quad (5.62)$$

$$\phi_2(\rho,z,T) = V_{gs} - V_{fb2} - \frac{qN_A}{4\varepsilon_{Si}}\left(\frac{t_{Si}^2}{4} + \frac{t_{Si}}{\vartheta_i}\right) + \sum_{n=1}^{\infty} J_n(\zeta_n\rho)[R_n e^{\zeta_n z} + S_n e^{-\zeta_n z}] \quad (5.63)$$

The formulation of electric field E_i for different regions is:

$$E_i(\rho,z,T) = -\frac{\partial\phi_i(\rho,z,T)}{\partial z} \quad (5.64)$$

For the specified device structure, the drain to source current is provided as [257]:

$$I_{ds} = \begin{bmatrix} I_{gidl}\ for\ -1.0V \le V_{gs} \le 0 \\ I_{sub}\ for\ 0 \le V_{gs} \le V_{th} \\ I_{lin}\ for\ V_{th} \le V_{gs} \le V_{sat} \\ I_{sat}\ for\ V_{sat} \le V_{gs} \le 1.0V \end{bmatrix} \quad (5.65)$$

The following formula provides the GIDL current for a cylindrical nanowire:

$$I_{gidl}(T) = AE_i{}^2\left(\frac{t_{Si}}{2}, L_1 + L_2, T\right) exp\left[\frac{-B}{E_i\left(\frac{t_{Si}}{2}, L_1 + L_2, T\right)}\right] \quad (5.66)$$

where, $A = \frac{q^2 m_r^{0.5}}{18\pi h^2 E_g^{1.5}}$ $B = \frac{\pi m_r^{0.5} E_g^{1.5}}{\sqrt[2]{2}qh}$, $m_r = 0.2m_o$

where m_0 represents the electron's rest mass, E_g is the energy band gap, and h is the Plank's constant. The subthreshold current (I_{sub}) can be found using:

$$I_{sub}(T) = \frac{t_{si}\pi\mu kT\eta_i{}^{1-e^{\frac{-V_{ds}}{V_T}}}}{\int_0^{L_1+L_2} \frac{1}{\int_0^{\frac{t_{si}}{2}} e^{\frac{\phi_i(\rho,z,T)}{kT}}}} \quad (5.67)$$

In this case, k for Boltzmann's constant and μ stands for electron mobility. The following is the current in linear region, I_{lin}:

$$I_{lin}(T) = \frac{t_{si}\pi\mu C_{oxeff1}E_c}{(E_c L + V_{ds})}\left[(V_{gs} - V_{th})V_{ds} - V_{ds}^2\right] \quad (5.68)$$

The current in the saturation region is calculated by putting V_{ds}=V_{dsat}=V_{gs}-V_{th} and given by:

$$I_{sat}(T) = \frac{t_{si}\pi\mu C_{oxeff2}}{\left(1 + \frac{V_{dsat}}{E_c L}(L - L_{sat})\right)}\left[\xi(V_{gs} - V_{th})V_{ds} - V_{ds}^2\right] \quad (5.69)$$

where L_{sat} is the characteristic length and ξ denotes empirical parameter that ranges between 0 and 1.

5.3.6 Results and Discussion

(a). Effects of temperature on P-E curve, hole concentration and velocity, and band energy

In LG theory, the dielectric response of ferroelectric materials is described as a function of temperature [258]. This theory defines the Gibbs free energy (F) as a function of the macroscopic polarization (P) as:

$$F = \frac{\alpha}{2}P^2 + \frac{\beta}{4}P^4 + \frac{\gamma}{6}P^6 \quad (5.70)$$

The relationship between the electric field (E) and polarization (P) is defined by the equation $\frac{dF}{dP} = E$

$$E = \alpha P + \beta P^3 + \gamma P^5 \quad (5.71)$$

Therefore, the relative dielectric permittivity of the ferroelectric material can be expressed as

$$\varepsilon_{FE} = \frac{1}{\varepsilon_0}\frac{dP}{dE} = \frac{1}{\varepsilon_0}\frac{1}{(\alpha + 3\beta P^2 + 5\gamma P^4)} \quad (5.72)$$

Here, ε_0 represents the dielectric constant of vacuum, and $\alpha, \beta, and\ \gamma$ are the Landau coefficients. In L-K theory, the coefficient α is a linear function of temperature as: $\alpha = \alpha_0(T - T_c)$, which becomes zero at the Curie-Weiss Temperature (T_c) and other parameters $\beta\ and\ \gamma$ are assumed to be independent of temperature[259]. Increasing the temperature above the Curie point decreases α which results in the ferroelectric material transitioning into a non-ferroelectric or paraelectric phase. From Figure 5.27, it is clear that the NC-region is larger for $T < T_c$, which shows NC behavior, and it decreases as the temperature rises to Curie temperature. At this temperature, the device starts showing paraelectric behavior as the temperature rises beyond T_c.

Figure 5.28 describes the detailed study of hole concentration phenomenon of the channel of C-NW-FET (Figure 5.28 (a)-(d)) and CGEF-NW-FET (Figure 5.28 (e)-(h)) having V_{GS} = 0.09 V and V_{DS} = 1.0 V with the help of contour plots for temperatures ranging from 250 K to 400 K. From Figure 5.26, we can conclude that the hole concentration of CGEF-NW-FET increases as the temperature increases from T = 250

K to T = 400 K. From the contour plots, Figure 5.28 (e)-(h) an abrupt increase in the hole concentration is observed, because of the change in mobility of electrons in the channel. This sudden increase in the hole concentration is because of the movement of fermi level towards the bandgap [175] due to the presence of the ferroelectric layer. Due to thermal perturbations, electron excitation surpasses that observed in conventional nanowire FETs, precipitating an augmented generation of electron-hole pairs and culminating in an elevated hole concentration at elevated temperatures.

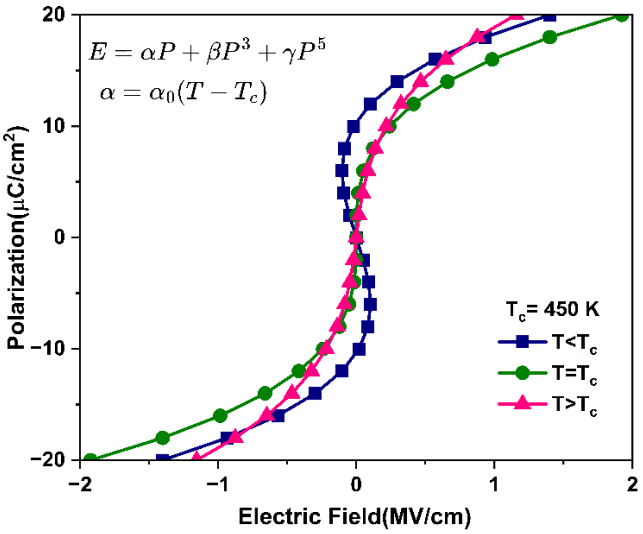

Figure 5.27 Polarization-Electric Field curve at $T < T_c$, $T = T_c$, and $T > T_c$, showing the phase transition above the Curie Temperature.

The contour plot of hole velocity for C-NW-FET and CGEF-NW-FET having V_{GS} = 0.09 V and V_{DS} = 1.0 V is described in Figure 5.29 (a)-(h) for temperatures ranging from 250 K to 400 K. In Figure 5.29 (a)-(d) contains the hole velocity for C-NW-FET, and Figure 5.29 (e)-(h) contains the hole velocity for CGEF-NW-FET. From Figure 5.29. In conclusion, in CGEF-NW-FET velocity of holes is greater in the channel region when compared with C-NW-FET at any given temperature ranging from T = 250 K to T = 400 K. This increase in velocity of holes is because the presence of a ferroelectric material in the gate stack modifies the capacitance of the device. A reduced voltage bias has been applied in Figure 5.29 to facilitate the observation and analysis of the band-to-band tunnelling phenomenon. This approach enables the manifestation of Interbrand quantum tunnelling, which occurs when electrons traverse the energy barrier between the valence and conduction bands, a process that becomes more pronounced under low gate electric field conditions.

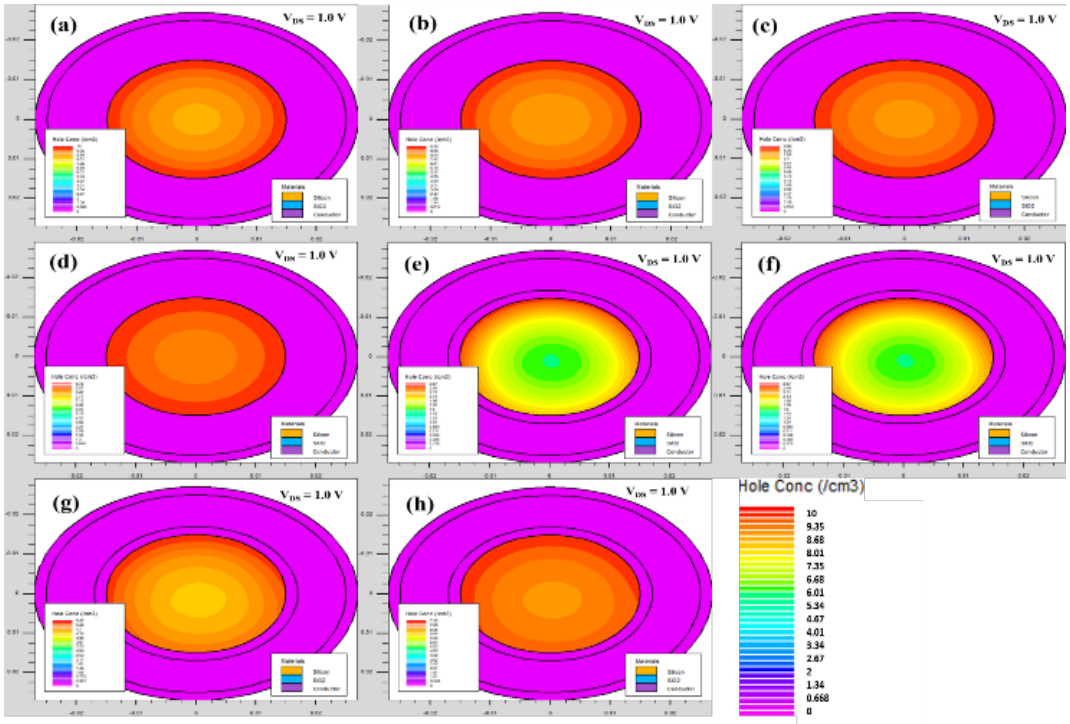

Figure 5.28 Contour plots for hole concentration of C-NW-FET and CGEF-NW-FET at T = 250 K, T = 300 K, T = 350 K and T = 400 K

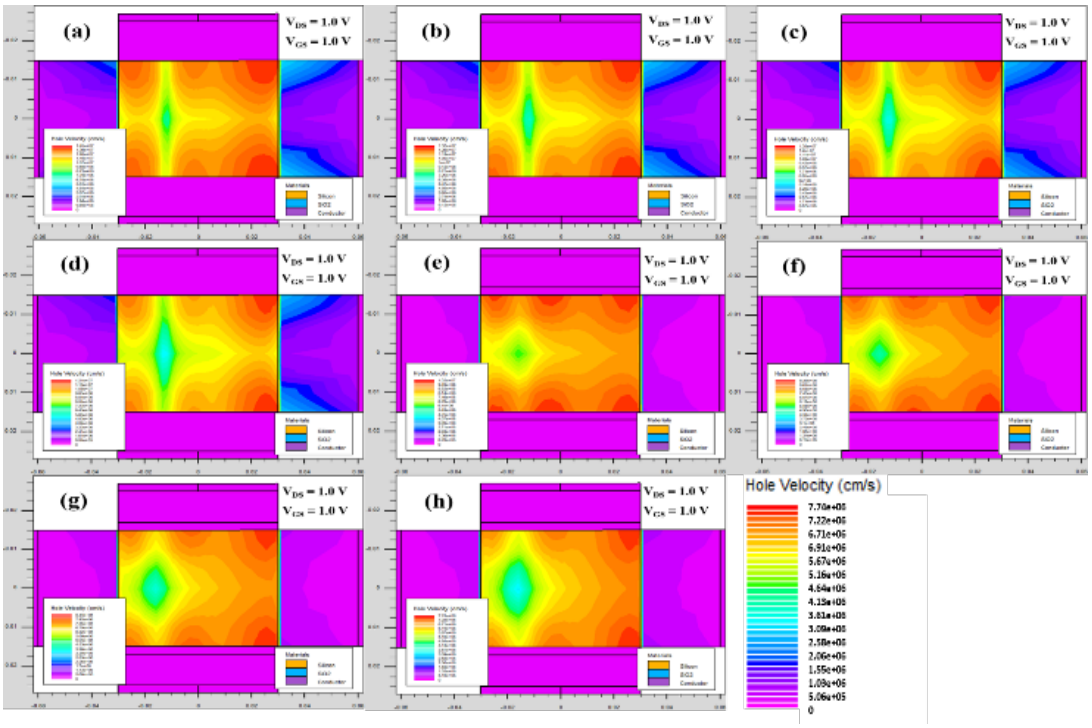

Figure 5.29 Contour plots for hole velocity of C-NW-FET and CGEF-NW-FET at T = 250 K, T = 300 K, T = 350 K and T = 400 K

Band-to-Band Tunnelling (BTBT) is a crucial dependability indicator for assessing the operation of devices. There is a substantial overlap between the valence and conduction bands as a result of depletion being exacerbated and a high drain bias. When this overlap happens in the OFF-state, it causes electrons to tunnel from the valence to the conduction band [168]. This phenomenon indicates that BTBT causes a significant rise in leakage current during the OFF-state, culminating in significant static power loss [175][168]. This static power dissipation increases as the gate length decreases, making BTBT a substantial issue for low-power standby applications. In relation to the point along the channel length, Figure 5.30 (b) shows how the band energy has changed over time. For the CGEF-NW-FET, when V_{DS} = 1V and 0V, respectively, it demonstrates the valence band energy (VBE) and conduction band energy (CBE). The band energy is seen to decrease for the drain end in Figure 5.30, which is related to the existence of a lower gate metal work function towards the drain end. As a result, this truncates the electron tunnelling from VBE to CBE, ultimately lowering BTBT. The band energy of CGEF-NW-FET is declining near the center of the channel length because of the ferroelectric capacitance generated by the presence of ferroelectric material.

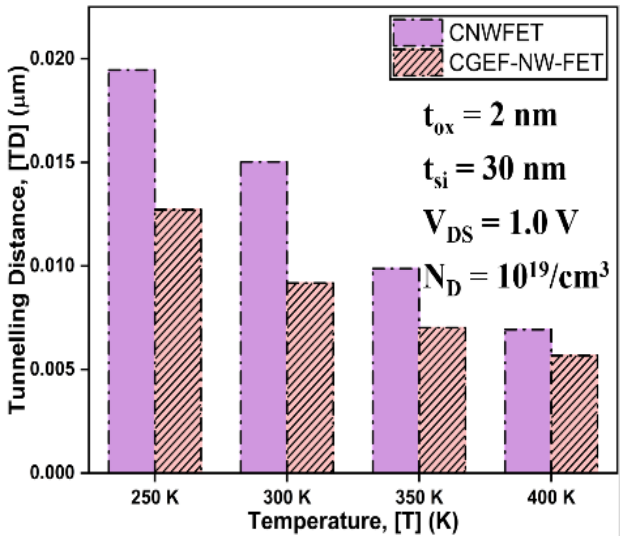

Figure 5.30 The band energy demonstrating the valence band energy (VBE) and conduction band energy (CBE) for both C-NW FET and C-FE-DM-NW-FET.

(b) Effects of temperature on tunnelling distance, surface potential, electric field, and GIDL current

The distance that an electron must travel in order to get from the high V_{DS} valence band energy to the high V_{DS} conduction band energy is referred to as the tunnelling distance. The fluctuation in band energy with temperature is principally caused by changes in carrier mobility, which increase owing to a shift in the Fermi level [175]. The tunnelling distance at different temperatures is shown in Figure 5.31. Figure 5.31 analysis demonstrates that the tunnelling distance decreases with increasing temperature. This decline is due to band bending at higher temperatures.

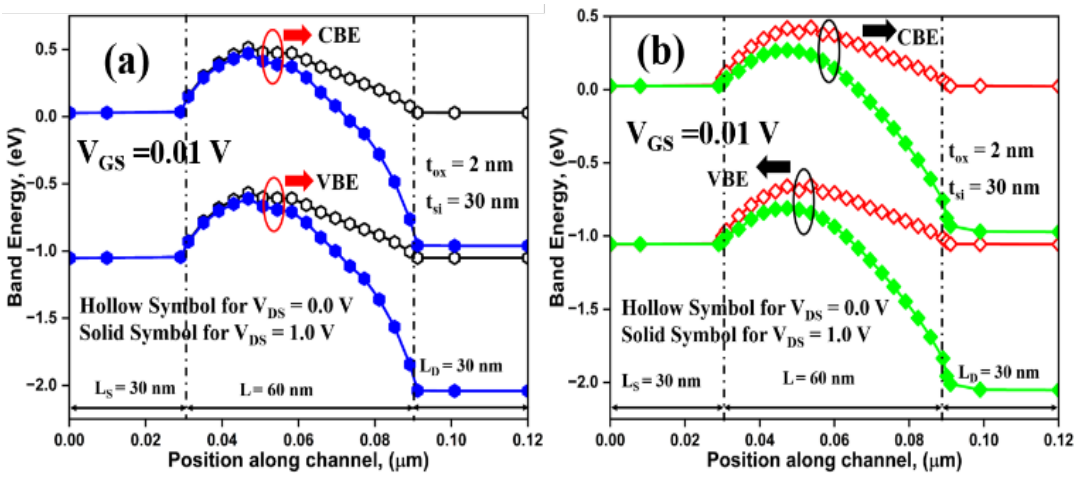

Figure 5.31 Tunnelling Distance for C-NW-FET and CGEF-NW-FET at various temperatures.

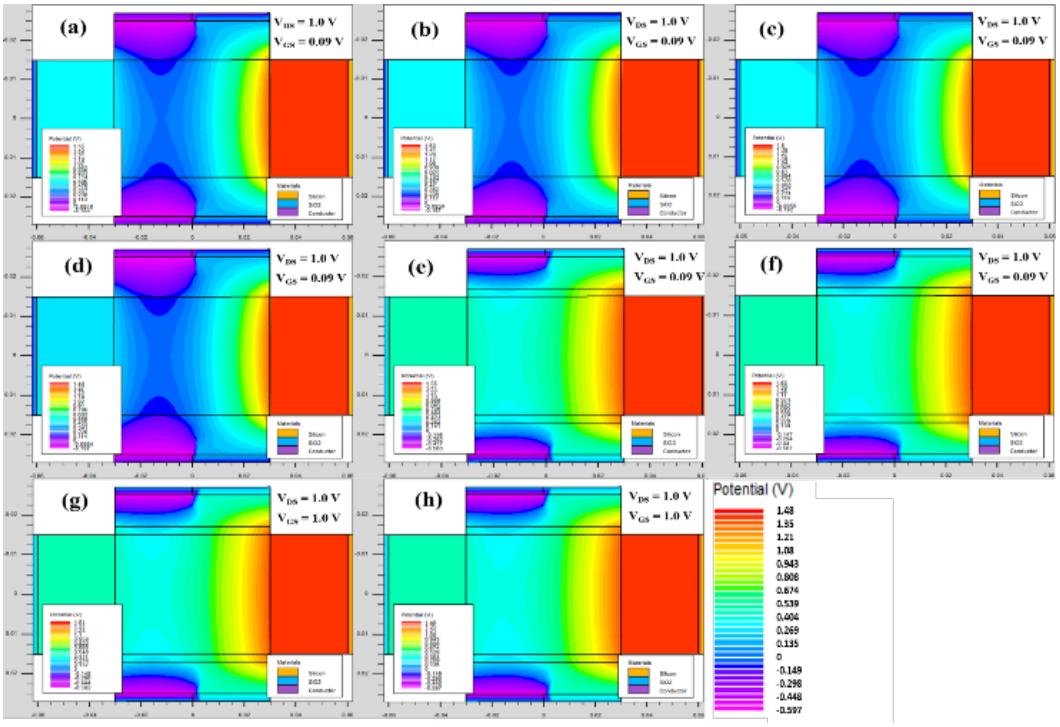

Figure 5.32 The contour plot of potential for C-NW-FET and CGEF-NW-FET at various temperatures.

The contour plot of potential for C-NW-FET and CGEF-NW-FET having V_{GS} = 0.09 V and V_{DS} = 1.0 V is described in Figure 5.32 (a)-(h) for temperatures ranging from 250 K to 400 K. The contour analysis shows that the CGEF-NW-FET exhibits a consistently greater potential over the whole channel when compared to the C-NW FET. This phenomenon is explained by the existence of a ferroelectric layer and a drain-side gate with a reduced work function.

Concerning the channel location for both the C-NW FET and CGEF-NW-FET, Figure 5.33 shows the change in surface potential at V_{DS} = 1.0 V and V_{GS} = 0.09 V. A closer

look at Figure 5.33 reveals that the surface potential of the CGEF-NW-FET device changes in the channel's center and is higher than the C-NW FET. An increase in the potential near the drain side can also be seen, it is because of the existence of a ferroelectric layer, which results in ferroelectric capacitance.

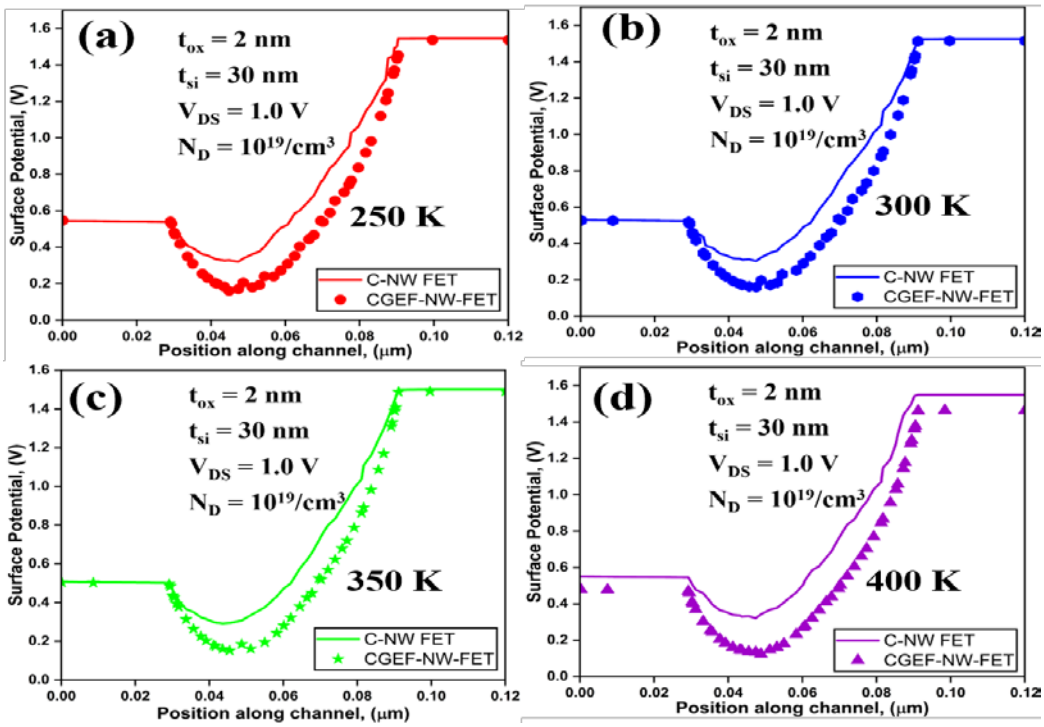

Figure 5.33 The surface potential of C-NW FET and CGEF-NW-FET at different temperatures.

In CGEF-NW-FET, the mobility of electrons is increased because of the ferroelectric layer and an increase in temperature, which increases the carrier mobility, decreases the tunnelling distance, and leakage current. Figure 5.34 shows the analytical results for CGEF-NW-FET and its validation with the simulation results. Figure 5.35 demonstrates the electric field (E_z) distribution for C-NW-FET and CGEF-NW-FET having V_{GS} = 0.09 V and V_{DS} = 1.0 V, is described in Figure 5.34 (a)-(d) for temperatures ranging from 250 K to 400 K.

The electric field (E_z) of CGEF-NW-FET is less than the C-NW FET at different temperatures. This is because of the presence of Ferroelectric capacitance in CGEF-NW-FET. The analytical formulation of the electric field and its validation with the simulation data are shown in Figure 5.36. Both results are in good agreement with each other.

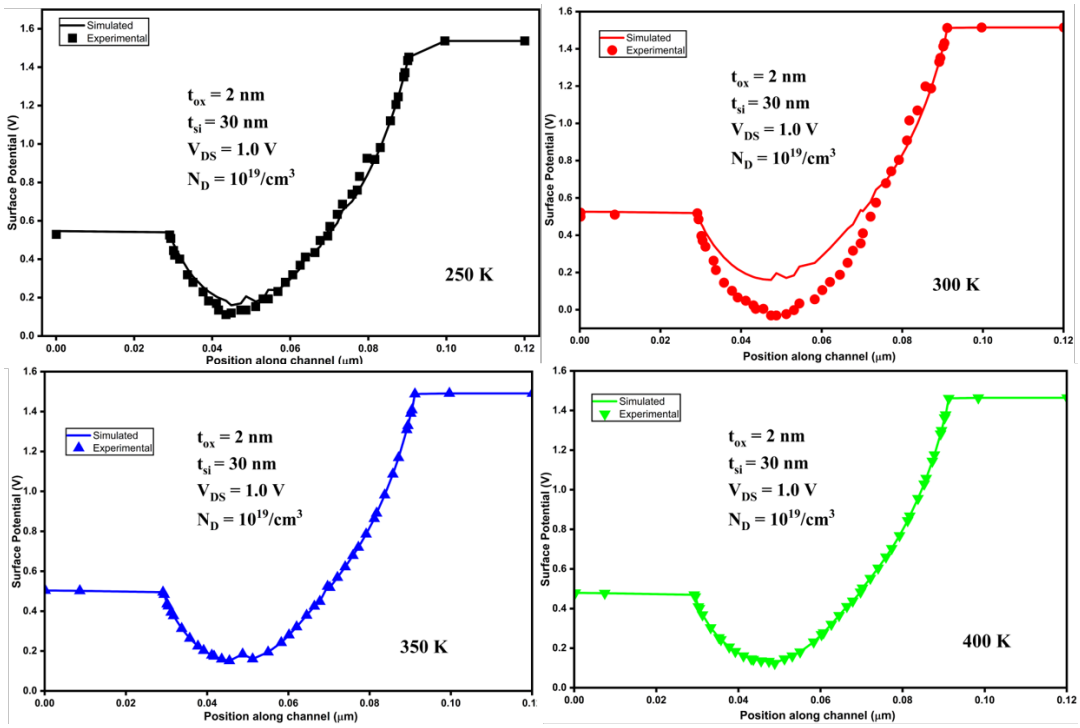

Figure 5.34 The analytical and simulated results for the surface potential of CGEF-NW-FET at different temperatures.

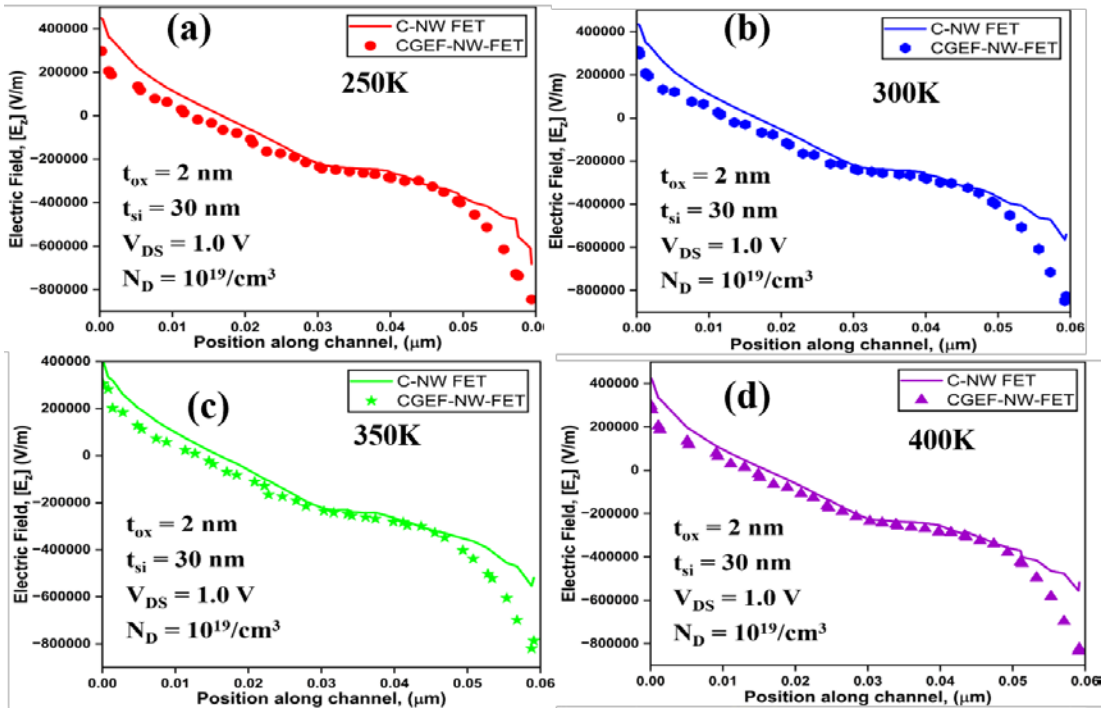

Figure 5.35 The electric field of C-NW FET and CGEF-NW-FET at different temperatures.

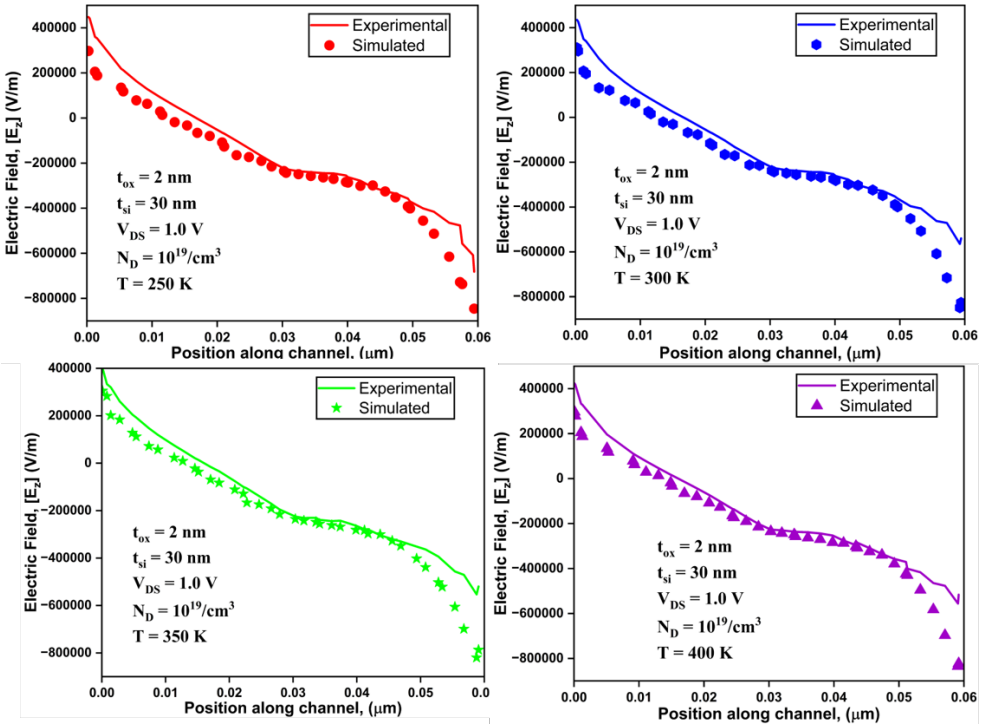

Figure 5.36 The analytical and simulated results for Electric Field of CGEF-NW-FET at different temperatures.

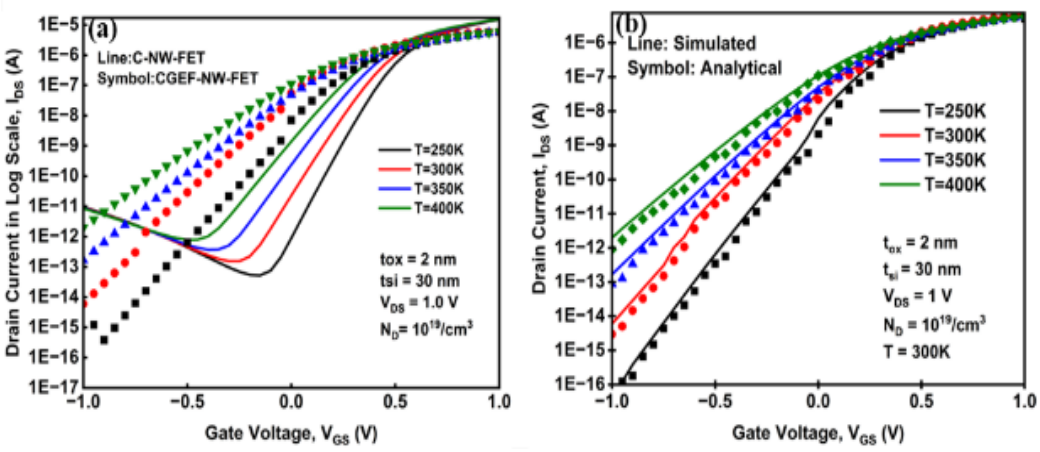

Figure 5.37 (a) GIDL current for C-NW FET and CGEF-NW-FET, (b) Analytical and simulated results of GIDL current for CGEF-NW-FET at various temperatures.

Figure 5.37 (a) exhibits the fluctuation of GIDL current with gate voltage for C-NW FET and CGEF-NW-FET, all at a drain voltage of V_{DS} = 1 V for T = 250 K, T = 300 K, T = 350 K, and T = 400 K. Notably, the CGEF-NW-FET has a significant decrease in GIDL current. When compared to the C-NW FET, the OFF-state GIDL current for the CGEF-NW-FET is -1.13 x 10^{-15} A for T = 250 K, 5.97 x 10^{-15} A for T = 300 K, 1.66 x 10^{-13} A for T = 350 K and 1.97 x 10^{-12} A for T = 400 K. Whereas the OFF-state GIDL current for the C-NW FET is 9.57 x 10^{-12} A for T = 250 K, 9.19 x 10^{-12} A for T = 300 K, 8.83 x 10^{-12} A for T = 350 K and 8.51 x 10^{-12} A for T = 400 K. It is also

observed from Figure 5.37 (b) that the analytical and simulated data for CGEF-NW-FET goes well with each other.

5.3.7 Comparative Analysis

The comparative evaluation of CGEF-NW-FET with the conventional cylindrical nanowire reveals substantial improvements, particularly under elevated temperature conditions. At 400 K, the CGEF-NW-FET demonstrates significantly lower GIDL of ~1.9 X 10^{-12} A as compared to 8.5 X 10^{-12} A for C-NW FET. The tunnelling distance of CGEF-NW-FET is reduced notably and further keeps decreasing with rising temperatures. The device achieves a higher surface potential and exhibits increased hole velocity with temperature, enhancing the ON state performance. The electric field helps in suppressing the leakage due to the lower work function at the drain side. Collectively, these characteristics translate into excellent temperature stability, surpassing the conventional FETs. Hence, CGEF-NW-FET is a promising candidate in terms of high temperature and low power applications where performance and reliability are essential.

Figure 5.38 contains the comparative analysis of CNW FET, NC-NW FET, C-FE-DM-NW FET and CGEF-NW FET. In this NC-NW FET, which demonstrates excellent switching efficiency, the CGEF-NW FET excels under high temperature conditions, and the C-FE-DM-NW FET achieves the strongest trade-off between ON-state current and leakage suppression.

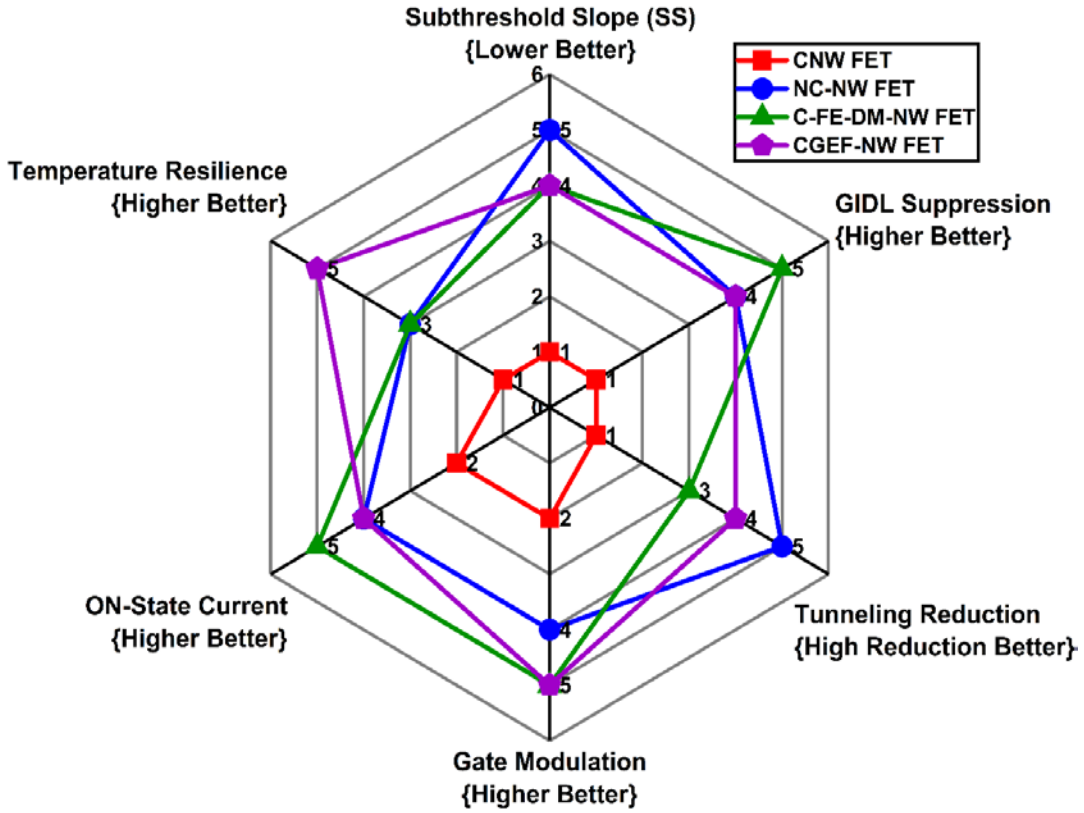

Figure 5.38 Comparative Analysis of Devices in Radar Graph

5.3.8 Challenges and Considerations

Despite the promising performance of the cylindrical gate engineered ferroelectric nanowire FET (CGEF-NW-FET) in terms of achieving steep subthreshold slopes, energy efficient switching and enhanced electrostatic control, several critical challenges still remain that must be carefully addressed before considering the practical applications of the device.

One of the foremost concerns is temperature dependent material degradation. The ferroelectric properties of hafnium zirconium oxide (HZO) are particularly sensitive to thermal stress and prolonged operation above ~400 K often leads to a reduction in residual polarization and a simultaneous increase in the coercive field. Such degradation significantly weakens the negative capacitance (NC) effect, thereby limiting device performance and stability at high operating temperatures [260].

Another important difficulty lies in achieving precision in work function engineering since the CGEF-NW FET relies on a dual metal gate stack with distinct work functions to control channel potential effectively. The accurate fabrication of a dual metal gate with different work functions is a very intensive process and is susceptible to variability and misalignment, which can result in threshold voltage mismatch and compromised device uniformity [261].

In addition, ferroelectric hysteresis and reliability issue becomes increasingly critical under elevated temperature, where the reliability of the NC behaviour and ferroelectric hysteresis can degrade if it is not properly stabilized via capacitance matching. This mismatch may lead to threshold drift, instability or reduced memory window retention, all of which threaten the consistency of device operation [262].

Another limitation arises from modelling complexity, as thermal-based modelling of the device must account for multiple coupled effects such as Fermi level shifts, field redistribution and mobility degradation which are not fully discussed by the traditional analytical approaches. This highlights the need for Multiphysics modelling frameworks and machine learning based calibration methods to provide accurate predictive capabilities [263].

Finally complex fabrication poses as a major obstacle. The realization of a cylindrical nanowire integrated with high-k ferroelectric stack requires high-resolution lithography, atomic layer deposition and precise etching. These steps are prone to variability, technologically intensive and introduce potential defects that can lower overall yield and reproducibility [99].

Hence, future progress in CGEF-NW FET relies on advanced material engineering strategies, process optimization techniques and device reliability enhancements aimed at overcoming these multifaceted challenges and ensuring compatibility with large scale CMOS integration.

Summary

This Chapter presented an in-depth exploration of the advanced nanowire transistors, which are designed based on the negative capacitance effect of ferroelectric materials.

This chapter detailed discussion of the Negative Capacitance Nanowire Field Effect Transistor (NC-NW FET), Cylindrical Ferroelectric Dual Metal Nanowire Field Effect Transistor (C-FE-DM-NW FET) and Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor (CGEF-NW FET). The framework of all these devices is the conventional cylindrical nanowire, but an innovative structural and material engineering approach is used in these to overcome long-standing limitations of nanoscale devices associated with leakage control, scaling and energy efficiency.

The NC-NW FET exploits the principle of negative capacitance using hafnium zirconium oxide (HZO) as ferroelectric material integrated in a cylindrical gate-all-around (GAA) FET architecture. The NC-NW FET achieves a significant reduction in subthreshold slope by harnessing the internal voltage amplification effect induced by negative capacitance. In this, a remarkably steep switching behaviour is observed, which translates to a subthreshold slope of ~13.4-14.1 mV/decade, which will reduce the power consumption. The gate-induced drain leakage (GIDL) current is also suppressed in this to the order of ~10^{-14} A, making it a highly efficient design for low power applications. The performance of this device remains moderate under varying thermal conditions. In this, further engineering can be helpful for effective high-temperature operations.

The C-FE-DM-NW FET extends the NC approach by introducing dual metal gate electrodes in conjunction with the ferroelectric gate dielectric. The source and drain controls are optimized in this device architecture because of the dual metal modulation, which enables spatially tuned electrostatics along the channel. Quantitatively, the C-FE-DM-NW FET suppresses the GIDL current further to ~10^{-15} A while maintaining the subthreshold slope of 15 mV/decade. In this, the C-FE-DM-NW FET demonstrates a significantly improved ON-state current when compared with the NC-NW FETs and conventional FETs. The tunnelling distance is shortened by ~28% relative to the baseline devices; the FET structure suppresses the undesirable tunnelling while preserving efficient carrier transport. Hence strong potential for high-performance applications where both high current and low leakage are critical is demonstrated by the C-FE-DM-NW FET.

The CGEF-NW FET was designed to address one of the persistent challenges in advanced transistors, i.e. temperature resilience. As devices are required to operate reliably in increasingly harsh environments, including aerospace, defence and automotive electronics, thermal robustness is as critical as electrical efficiency. CGEF-NW FET achieves excellent suppression of temperature-induced leakage and maintains performance stability up to 400K by incorporating ferroelectric (HZO) gate materials alongside engineered gate work functions. At elevated temperatures, the leakage currents increase, the tunnelling distance shrinks, and rapid performance degradation is seen in the conventional devices. The contrast, the CGEF-NW FET reduced GIDL currents to ~1.9 x 10^{-12} A at 400 K and preserves enhanced surface potential and carrier velocity. This makes a strong candidate for high-temperature applications where conventional devices fail to maintain acceptable performance.

In conclusion, this chapter demonstrates the ferroelectric integration and gate engineering, providing powerful pathways for overcoming the scaling-induced

limitations of nanowire FETs. The NC-NW FET, C-FE-DM-NW FET and CGEF-NW FET each highlight different strengths, such as optimizing leakage performance trade-off, steep switching and temperature robustness. The collective insight gained in this work underlines the versatility of ferroelectric nanowire architectures as a promising candidate for ultra-low power, thermally stable and high-performance nanoelectronics. These advancements address the short channel effects and also pave the way for reliable integration in emerging fields such as high temperature electronics, next generation communication systems and energy efficient computing.

CHAPTER 6

CONCLUSION, FUTURE SCOPE AND SOCIAL IMPACT

6.1 Conclusion

The present research work has been driven by the pressing need to overcome the fundamental limitations of conventional CMOS technology in the deep sub nanometer regime. The study commenced by identifying, through the introduction and literature review that continuous device scaling has resulted in significant challenges such as short channel effects (SCEs), degraded subthreshold swing, increased leakage currents and elevated power dissipation. Despite the evolution from planar MOSFETs to FinFETs and then to Gate-All-Around (GAA) FETs, the demand persists for novel architectures capable of delivering both high performance and low power consumption.

In response to these limitations, the thesis explores a sequence of advanced nanowire FET architectures, emphasizing dielectric optimization, electrostatic control and ferroelectric integration. The progressive device designs introduced in this work collectively demonstrate hoe careful manipulation of gate materials, dielectric constants and ferroelectric properties can substantially enhance transistor performance beyond that of traditional MOSFETs.

The initial phase focused on macaroni type nanowire structures employing double metal gates and hetero-dielectric channels, which provided improved gate to channel coupling and reduced leakage through potential modulation. These devices established a foundation for electrostatic optimization and revealed that multi-material and multi-dielectric strategies can effectively suppress short channel degradation.

Building upon this, the research incorporated ferroelectric materials within the gate stack, introducing negative capacitance (NC) behaviour to achieve sub-60 mV/decade subthreshold swing, thereby enabling steep-slope and energy efficient switching. The NC nanowire configurations not only reduced power consumption but also improved current drivability through internal voltage amplification effects.

The final stage involved the development of cylindrical ferroelectric nanowire devices incorporating dual metal and gate engineering schemes. These designs offered remarkable improvements in electrostatic integrity, drain current and transconductance performance, with minimal DIBL and negligible hysteresis. The combination of cylindrical geometry with ferroelectric and dual metal gates marked a significant step toward achieving the desired balance between energy efficiency, high performance and scalability.

The first design stage explored DMGM-NFET and HD-MC CGAA FET. These devices introduced multi-metal gate and multi dielectric configurations that effectively modulated the channel potential and improved gate control through tailored work function and permittivity profiles. The findings demonstrated reduced short channel degradation, improved subthreshold swing, and enhanced current modulation

compared to conventional single-gate nanowire FETs. Subsequent research phases extended the device concept into ferroelectric domain engineering, resulting in the development of NC-NW FETs. By incorporating a ferroelectric layer within the gate stack, the negative capacitance phenomenon was harnessed to achieve internal voltage amplification. This led to sub-thermal subthreshold swing (<60 mV/decade), reduced power consumption, and faster switching speed. These results validated that the introduction of ferroelectric materials, specifically HZO, can revolutionize transistor operation by providing self-boosting gate control without additional voltage overhead.

Overall, the comprehensive simulation-based investigation confirmed that through that co-optimization of electrostatic engineering (via gate geometry and material control) and ferroelectric layer integration, it is possible to develop next generation nanowire FETs that surpass the thermionic limit 60 mV/decade while maintaining robust short channel immunity. The cumulative outcomes indicate a clear performance evolution from electrostatically optimized designs to energy efficient, steep slope, ferroelectric-based configurations forming a complete pathway for sustainable transistor scaling in the post CMOS era.

6.1.1 Comparative Summary of Proposed Devices

The sequence of device architectures proposed and analyzed in this research reflects a methodical design evolution intended to enhance the electrostatic and energy performance of nanowire FETs. Building upon the challenges identified in the Introduction and Literature Review, the study systematically addressed the shortcomings of existing transistor structures by combining dual-metal gating, dielectric engineering and ferroelectric integration.

The comparative evaluation presented in Table 6.1 encapsulates this evolution and highlights the progressive improvements achieved in subthreshold swing (SS), On/Off current ratio, drain current and DIBL across all designs.

TABLE 6.1 COMPARATIVE SUMMARY OF PROPOSED DEVICES

PARAMETERS	DMGM-NFET	HD-MC CGAA FET	NC-NW FET	C-FE-DM-NW FET	CGEF-NW FET
Gate Configuration	Dual Metal Gate (Macaroni Structure)	Dual Metal Gate (Macaroni Structure)	Single Gate (Cylindrical)	Dual Metal (Cylindrical)	Dual Metal (Cylindrical)
Dielectric/Ferroelectric Stack	SiO_2	SiO_2 + Vacuum	SiO_2 + HZO (Ferroelectric)	SiO_2 + HZO (Ferroelectric)	SiO_2 + HZO (Ferroelectric)
Electrostatic Efficiency	High	Very High	Excellent	Outstanding	Exponential
Subthreshold Swing (SS)	~ 70 mV/decade	~ 68 mV/decade	< 60 mV/decade	< 55 mV/decade	~ 50 mV/decade
DIBL	Low	Very Low	Very Low	Negligible	Negligible
GIDL	10^{-11} A	10^{-14} A	10^{-14} A	10^{-15} A	10^{-15} A
I_{ON}/I_{OFF} Ratio	10^6	10^7	10^8	10^8-10^9	>10^9
Drain Current	Moderate	High	High	Very High	Very High

Distinctive Feature/Advantage	Improved potential modulation, reduced leakage	Enhanced gate coupling and carrier confinement	Sub-thermal SS, improved energy efficiency	Excellent control, enhanced transconductance	Superior stability and electrostatic integrity

The comparative results demonstrate a consistent and measurable trend of performance enhancement with each successive device generation. The subthreshold swing steadily decreases from approximately 70 mV/decade in the in the DMGM-NFET to nearly 50 mV/decade in the CGEF-NW FET, confirming the successful implementation of steep-slope switching behaviour. Simultaneously, DIBL values decrease from low to nearly negligible levels, indicating effective suppression of short channel effects. The ON/OFF current ratio improves by more than three magnitudes from 10^6 to beyond 10^9 while drain current and transconductance shoe significant enhancement due to improved charge confinement and channel control. The GIDL values decreased from 10^{-11} A in DMGM-NFET to nearly 10^{-15} A in CGEF-NW FET, confirming the successful reduction of gate leakages.

These improvements are driven by the three core physical mechanisms; one is enhanced electrostatics which was achieved by incorporating the dual metal and cylindrical gate designs. The second one is material innovation in these dual dielectric designs are incorporated via high-κ and ferroelectric integration leading to internal voltage amplification. The last one is geometrical optimization in these fully wrapped cylindrical architectures providing superior gate coupling are discussed.

These findings validate the central hypothesis established in chapter 1 and supported by the literature review: that synergistic engineering of gate geometry and material interfaces enables transistors to achieve both scalability and energy efficiency beyond conventional MOSFET paradigm. Collectively, these results form a technological bridge from electrostatically optimized designs to negative capacitance driven steep slope architectures. The insights gained here naturally extend to the future directions of this work, as outlined in the following section.

6.2 Future Scope

The promising simulation outcomes and theoretical insights obtained from this research open a wide spectrum of future opportunities for the practical realization and technological translation of the proposed devices. The future scope of the work can be classified into five major domains:

6.2.1 Experimental Realization

While the proposed designs have been comprehensively validated through TCAD simulations, experimental fabrication is essential to demonstrate their real-world feasibility. Techniques such as Atomic Layer Deposition (ALD) and Chemical Vapor Deposition (CVD) can be employed for precise deposition of high-κ and ferroelectric layers. Dual metal gate fabrication using TiN, W or Mo must be optimized for uniform work function control. Structural and electrical characterization through Transmission Electron Microscopy (TEM), X-ray Diffraction (XRD), Scanning Electron Microscopy (SEM) and Piezo response Force Microscopy (PFM), combined with

electrical testing, will validate the predicted characteristics such as subthreshold swing, current drivability and hysteresis width.

6.2.2 Material Engineering and Interface Optimization

Research can extend into the development of doped ferroelectric materials such as $Hf_{1-x}Al_xO_2$ and $Hf_{1-x}Si_xO_2$ which exhibit superior ferroelectric stability and lower coercive fields. Further, interface trap density minimization through improved interface passivation and capacitance matching optimization will ensure hysteresis-free negative capacitance operation. Studies on ferroelectric fatigue, retention and endurance under high-field conditions will be crucial to ensure long-term reliability.

6.2.3 Circuit-Level Integration and System Design

The integration of these devices into combinational and sequential logic circuits such as inverters, SRAM cells and flip-flops will demonstrate their real-world applicability. The sub-60 mV/decade switching characteristic offers substantial power savings at reduced supply voltages, making them ideal for low-power VLSI design. Hybrid architectures combining ferroelectric nanowire FETs with CMOS can yield ultra-low power systems for embedded and mobile computing.

6.2.4 Analytical Modelling and Compact Simulation

Development of analytical compact models capturing ferroelectric polarization, quantum confinement and negative capacitance dynamics is essential. These models can be integrated into SPICE or Verilog platforms for circuit level design. Advanced modelling using quantum transport and non-equilibrium Green's function (NEGF) approaches can be used to evaluate device behavior at sub-5 nm dimensions.

6.2.5 Emerging and Interdisciplinary Applications

The proposed devices can be extended to neuromorphic computing, non-volatile memory and biosensing applications. The intrinsic polarization hysteresis of ferroelectric layers can be emulating synaptic learning, while the cylindrical geometry ensures high current sensitivity suitable for low power analog neural hardware. Their compatibility with flexible substrates also opens opportunities for wearable and biomedical systems.

In summary, the future of this research lies in the experimental realization, material enhancement and circuit integration of these nanowire ferroelectric FETs, thereby transforming simulation-based insights into scalable, tangible and sustainable technologies.

6.3 Social Impact

The impact of this research extends beyond scientific innovation, it represents a meaningful step toward sustainable semiconductor technology with far reaching social, environmental and industrial implications.

From a technological standpoint the introduction of ferroelectric based nanowire FETs enables ultra-low power operation with sub thermal switching capability. This is

instrumental for next generation computing systems, 5G communication devices and artificial intelligence hardware, where efficiency and speed are paramount. The use of CMOS compatible ferroelectrics (HZO) endures industrial scalability, bridging the gap between emerging physics and manufacturable technologies. The research outcomes also have transformative implications for non-volatile memory and neuromorphic computing.

From a societal and environmental perspective, the proposed devices contribute significantly to energy sustainability. Reduced leakage and low-voltage operation directly translate into lower energy consumption across electronic systems, helping mitigate the growing energy demands of global data centers and portable electronics. These advances align strongly with the United Nations Sustainable Development Goals promoting affordable clean energy and sustainable industry.

Furthermore, integrating these devices in IoT, biomedical and wearable platforms can enable energy autonomous sensing and computing systems, reducing electronics waste and enhancing quality of life. The potential for green electronics thus represents a convergence of technological progress with environmental responsibility.

This thesis establishes a complete evolutionary pathway for nanowire transistor innovation beginning with electrostatic optimization and culminating in ferroelectric negative capacitance integration. Each design iteration demonstrates measurable progress towards achieving steep-slope, low power and scalable nanoelectronics devices.

The outcomes not only advance semiconductor device physics but also embody the principle of technology serving sustainability. The proposed architectures have the potential to revolutionize future computing paradigms by uniting high performance, energy efficiency and environmental consciousness as essential triad for the post CMOS era.

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Ballistic Transport," *4th Electron Devices Technol. Manuf. Conf. EDTM 2020 - Proc.*, 2020, doi: 10.1109/EDTM47692.2020.9117841.

List of Publications

SCI/SCIE Journal Papers

1. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Hetero-dielectric macaroni channel cylindrical gate all around field effect transistor (HD-MC CGAA FET) for reduced gate leakage analog applications" Microsystem Technologies, vol. 30, no. 5, 2024, p. 599-611, doi: 10.1007/s00542-023-05577-9 (Springer, SCIE) (accepted and published).
2. **Aapurva Kaul,** Snehlata Yadav, Sonam Rewari, and Deva Nand "Computational modelling of cylindrical-ferroelectric-dual metal-nanowire field effect transistor (C-FE-DM-NW FET) using landau equation for gate leakage minimization" Micro and Nanostructures, vol. 191, 2024, 207851, doi: 10.1016/j.micrna.2024.207851 (Elsevier, SCIE) (accepted and published).
3. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Double metal gate macaroni nanowire FET (DMGM-NFET) for improved performance and off-state leakage reduction" ECS Journal of Solid State Science and Technology, vol. 13, no. 10, 2024, 103010, doi: 10.1149/2162-8777/ad775d (IOP Science, SCIE) (accepted and published).
4. **Aapurva Kaul,** Snehlata Yadav, Sonam Rewari, and Deva Nand, "Analytical Modelling of Temperature Resilient Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor" IEEE Transactions on Dielectrics and Electrical Insulation, vol. 32, no. 5, p. 2674-2682, 2025, doi: 10.1109/TDEI.2025.3538754 (IEEE Transaction, SCIE) (accepted and published**).**
5. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Performance-Oriented Analytical Modelling of Channel Engineered-Macaroni Induced Gate All Around Field Effect Transistor for Off-State Leakage Mitigation" ECS Journal of Solid State Science and Technology, vol. 14, no. 10, 2025, 103002, doi: 10.1149/2162-8777/ae09d8 (IOP Science, SCIE) (accepted and published).

IEEE International Conference Papers

1. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Macaroni channel-nanowire-field effect transistor (MC-NW-FET) for gate induced drain leakage (GIDL) reduction application" In 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), pp. 35-38, 2022, doi: 10.1109/EDKCON56221.2022.10032964.

2. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Field Effect Transistor Incorporating Negative Capacitance and Nanowire Structures for the Attenuation of Gate Leakage Phenomena" In 2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON), pp. 607-611, 2024, doi: 10.1109/EDKCON62339.2024.10870658.

3. **Aapurva Kaul,** Sonam Rewari, and Deva Nand, "Mathematical Modelling of Gate Leakage in Channel Interface Engineered-Electrostatic Potential Modulated Field Effect Transistor for Advanced Digital Applications" In 2025 International Conference on Electrical, Computer and Energy Technologies (ICECET), 2025.

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EDUCATION

Ph.D. in Electronics and Communication Engineering — AUGUST 2021 - PRESENT (Thesis Submitted)
Delhi Technological University, Delhi
Thesis Title: Study And Design of Low-Leakage Nanowire Field-Effect Transistor
Supervisor: Dr. Sonam Rewari, Assistant Professor
Joint Supervisor: Dr. Deva Nand, Associate Professor

M.Tech. in VLSI Design — JULY 2014 – JUNE 2016
Maharishi Markandeshwar Engineering College, Mullana, Ambala — CGPA:8.97
Thesis Title: Design Of 64-Bit Mac Unit Using Reversible Logic Gate and Ancient Mathematics
Supervisor: Mr. Abhijeet Kumar, Assistant Professor

B.Tech. In Electronics and Communication Engineering — JULY 2009 - JUNE 2013
Jaipur Engineering College and Research Center, Jaipur — Percentage: 66
Project Title: Modified Solar Water
Heater Supervisor: Mr. Anil Jain,
Assistant Professor Project Title:
Modern Lighthouse
Supervisor: Mr. Vikas Sharma, Assistant Professor

SKILLS

- Device Simulation Tool: Silvaco TCAD
- Circuit Simulation Tool: LtSpice and Xilinx 8.2i
- Programming Languages: Verilog HDL, VHDL
- Software Tool: MS Office and Origin
- Speaking and Writing Proficiency: English (Advance) and Hindi (Advance)
- Miscellaneous: Academic Research, Teaching, Mentoring, and Reviewing Technical Skills

RESEARCH INTEREST

- FET-based Biosensor, Gas Sensor, and pH Sensor
- VLSI Design, HDL
- Simulation and Modelling of FET-based Devices
- Negative capacitance FET
- Si-Nanowire FET

PROFESSIONAL EXPERIENCE

ASSISTANT PROFESSOR | Jaipur Engineering College and Research Centre | Jaipur, Rajasthan July 2017 – October 2019

- Instruct undergraduate Electronics and Communication Engineering courses, ensuring alignment with academic objectives.
- Design and develop course syllabi, curricula, reading materials, assessments, and quizzes.
- Organize and conduct practical exams and arrange industrial visits to bridge the gap between theoretical knowledge and real-world applications.
- Develop course content in line with departmental guidelines and industry standards.
- Deliver engaging lectures and lead thought-provoking classroom discussions.
- Contribute to academic research and publish articles in professional journals.

Additional Roles and Responsibilities:

- Department Time-Table Coordinator (2018-2019)
- Training and Placement Officer (TPO) and HR Associate (2017-2019)
- Practical Examination Coordinator (2017-2019)
- Industrial Visit Coordinator (2017-2019)
- Cultural Coordinator - College Tech Fest (2018)
- Coordinator - Smart India Hackathon (2018)
- Alumni Cell Coordinator (2017-2018)

ACHIEVEMENTS

Awarded the University Gold Medal for securing First Class First Position with Distinction in Master of Technology, specializing in VLSI Design.

THESIS & PROJECTS

Design of 64-Bit MAC Unit using Reversible Logic Gate and Ancient Indian Mathematics

Supervisor: Mr. Abhijeet Kumar Assistant Professor

- Studied Reversible Logic Gate, Vedic Mathematics, and Kogge Stone Adder.
- In this the designed 64-bit MAC Unit is High speed unit.

Design and Simulation of Vedic Multiplier using

HDL Supervisor: Mr. Abhijeet Kumar Assistant

Professor

- Built a multiplier unit
- Studied Vedic mathematics, multiplier and various adder unit's designs.
- Designing and simulation of Vedic multiplier using Xilinx software.
- Can be used in various electronic applications for fast multiplication purposes.

Modified Solar Water Heater

Supervisor: Mr. Anil Jain Assistant Professor

- Build a modified version of the solar water heater
- Worked designing solar water heaters, buzzer system, and temperature measuring systems.
- Built overflow detector system and temperature measurement system.

Modern Lighthouse

Supervisor: Mr. Vikas Sharma Assistant Professor

- Build a modified version of the lighthouse.
- Worked on designing a lighthouse and timing control system.
- Can be used at various ports and islands after dawn.

RESEARCH PUBLICATIONS

Peer-reviewed articles

- Kaul, A., Rewari, S., & Nand, D. (2025). Performance-Oriented Analytical Modelling of Channel Engineered-Macaroni Induced Gate All Around Field Effect Transistor for Off-State Leakage Mitigation. ECS Journal of Solid State Science and Technology.
- Kaul, A., Yadav, S., Rewari, S., & Nand, D. (2025). Analytical Modelling of Temperature Resilient Cylindrical Gate Engineered Ferroelectric Nanowire Field Effect Transistor. *IEEE Transactions on Dielectrics and Electrical Insulation*, doi: 10.1109/TDEI.2025.3538754.
- Das, A., Bhardwaj, A., Das, K., Yadav, S., Kaul, A., Goyal, P., ... & Gupta, R. S. (2025). Numerical Simulation on Sensitivity Modulation in Nanowire MOSFEB Detector for Biomedical Applications. *Indian Journal of Pure & Applied Physics (IJPAP)*, 63(4), 281-300.

- Kaul, A., Rewari, S., & Nand, D. (2024). Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET) for Reduced Gate Leakage Analog Applications. *Microsystem Technologies,* 30(5), 599-611.
- Kaul, A., Yadav, S., Rewari, S., & Nand, D. (2024). Computational Modelling of Cylindrical-Ferroelectric-Dual Metal-Nanowire Field Effect Transistor (C-FE-DM-NW FET) Using Landau Equation for Gate Leakage Minimization. *Micro and Nanostructures*, 191, 207851.
- Kaul, A., Rewari, S., & Nand, D. (2024). Double Metal Gate Macaroni Nanowire FET (DMGM-NFET) for Improved Performance and Off-State Leakage Reduction. *ECS Journal of Solid State Science and Technology*, 13(10), 103010.
- Kaul, A., & Kumar, A. (2016). Simulation of 64-bit MAC Unit using Kogge Stone Adder and Ancient Indian Mathematics. *Journal of Engineering Research and Application*, *6*(6), 01-05.
- Kaul, A., Vyas, R., Ritambhara., & Sharda M, K., (2019, May). A Review of Fiber Tapping Mechanisms. *International Journal of Scientific & Engineering Research,* 10(5), 73-80.
- Kaul, A., Yogita., Ritambhara., & Gupta, D., (2019, May). Comparative study of the characteristics of the Rectangular Waveguide on the basis of Dimension, Frequency and Mode. *International Journal of Scientific & Engineering Research,* 10(5), 18-22.

International Conferences

- Kaul, A., Rewari, S., & Nand, D. (2025, July). Mathematical Modelling of Gate Leakage in Channel Interface Engineered- Electrostatic Potential Modulated Field Effect Transistor for Advanced Digital Application. *In 2025 International Conference on Electrical, Computer and Energy Technologies (ICECET)*.
- Yadav, S., Thakur, V., Kaul, A., Rewari, S., & Nand, D. (2025, May). Gallium Nitride Gate-All-Around Macaroni Field Effect Transistor (GaN-GAA-MCFET): Biosensor for DNA detection. *In 2025 Devices for Integrated Circuit (DevIC)* (pp. 348-352).
- Kaul, A., Rewari, S., & Nand, D. (2024, November). Field Effect Transistor Incorporating Negative Capacitance and Nanowire Structures for the Attenuation of Gate Leakage Phenomena. In *2024 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)* (pp. 607-611). IEEE.
- Kaul, A., Rewari, S., & Nand, D. (2022, November). Macaroni Channel-Nanowire-Field Effect Transistor (MC-NW-FET) for Gate Induced Drain Leakage (GIDL) Reduction Application. *In 2022 IEEE International Conference of Electron Devices Society Kolkata Chapter (EDKCON)* (pp. 35-38). IEEE.
- Kaul, A., Rewari, S., & Nand, D. (2022, September). Hetero-Dielectric Macaroni Channel Cylindrical Gate All Around Field Effect Transistor (HD-MC CGAA FET) for Reduced Gate Leakage Analog Applications. *In 11th International Conference on Computing, Communication and Sensor Networks (CCSN)*.
- Kaul, A., Yogita., Ritambhara., & Gupta, D., (2019, April). Comparative study of the characteristics of the Rectangular Waveguide on the basis of Dimension, Frequency, and Mode. *In 2019 International Conference on Communication, Optical and Microelectronics:" The Emerging Trends" (ICCOMET)*.
- Kaul, A., Vyas, R., Ritambhara., & Sharda M, K., (2019, April). A Review of Fiber Tapping Mechanisms. *In 2019 International Conference on Communication, Optical and Microelectronics:" The Emerging Trends" (ICCOMET)*.
- Kaul, A., (2019, January). Design and Simulation of MAC Unit using Kogge Stone Adder and Ancient Indian Mathematics. In 2019 2nd International Conference on Emerging Trends & Applied Sciences (ICETEAS).
- Kaul, A., (2018, April). Simulation of high Speed MAC Unit using KSA, *In 2nd International Conference on Recent Technological Developments in Electronics and Electrical Engineering (RTDEEE)*.
- Kaul, A., & Kumar, A. (2016, April). Novel Approach for Mac Unit Using Vedic Mathematics. *In 3rd International Conference on Recent Trends in Engineering, Sciences and Management* (pp. 736-742).

Book Chapter

- Kaul, A., Das, A., Yadav, S., Rewari, S., & Nand, D. Design and Performance Exploration of Macaroni Channel-Based Ge/Si Interfaced Nanowire FET for Analog and High-Frequency Applications Using Machine Learning. In Machine Learning for Semiconductor Materials (pp. 172-200). CRC Press.

National Patents

- Kaul, A. et al. (2024). Dielectric Modulated Dual Cavity Negative Capacitance Junction Accumulation (DM-DC-NC-JAM) FET-based Biosensor for DNA Biomolecules Detection – Analytical Model. (*Patent Published*)

- Kaul, A. et al. (2025). Germanium Source Step Graded Biotube FET for Dielectric Modulated Biosensing. (*Patent Submitted*)

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