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Chapter 1

Introduction

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* This chapter provides a comprehensive background to the present research work, with a particular focus on the growing significance of Ferroelectric based FinFET (FeFinFET) in the modern integrated circuit industry.

* The discussion begins with a reassessment of the scaling constraints of MOSFETs, highlighting various adverse effects such as short-channel effects (SCEs) that arise as devices are pushed toward smaller geometries.

* Following that, this chapter includes a review of several device engineering strategies reported in literatures such as gate engineering, channel engineering, and bandgap engineering techniques, which have been proposed to mitigate SCEs and enhance device reliability.

* Moreover, Ferroelectric based devices and specifically FeFinFET are covered in the chapter as a possible solution to mitigate these issues. The chapter then goes on to discuss the basic design of FeFinFET, their classification, their basic operation, potential advantages, and the technological difficulties incurred in FeFinFET.

* Finally, the chapter provides an overview of the thesis research objectives, followed by a summary of all the chapters.

1.1 Background

In 1958, Jack Kilby, working at Texas Instruments, independently introduced the concept of the integrated circuit (IC), a breakthrough that revolutionized the electronics industry (Sax09). The continuous progress of ICs was largely driven by Moore's Law, which emerged from advances in Complementary Metal-Oxide-Semiconductor (CMOS) technology. Formulated by Intel co-founder Gordon Moore, the law predicts that the number of transistors on a chip doubles approximately every two years (Moo98). As illustrated in Figure 1.1, the consistent downscaling of MOSFET gate length in accordance with the International Technology Roadmap for Semiconductors (ITRS) projections and the exponential rise in transistor count per processor chip over time, are evident (Rad13). This progressive miniaturization has significantly boosted IC performance, enabling higher integration density, lower cost, and reduced power consumption. Consequently, IC technology has become the backbone of a wide spectrum of applications, ranging from personal computers and mobile phones to advanced medical systems and autonomous vehicles (KA08).

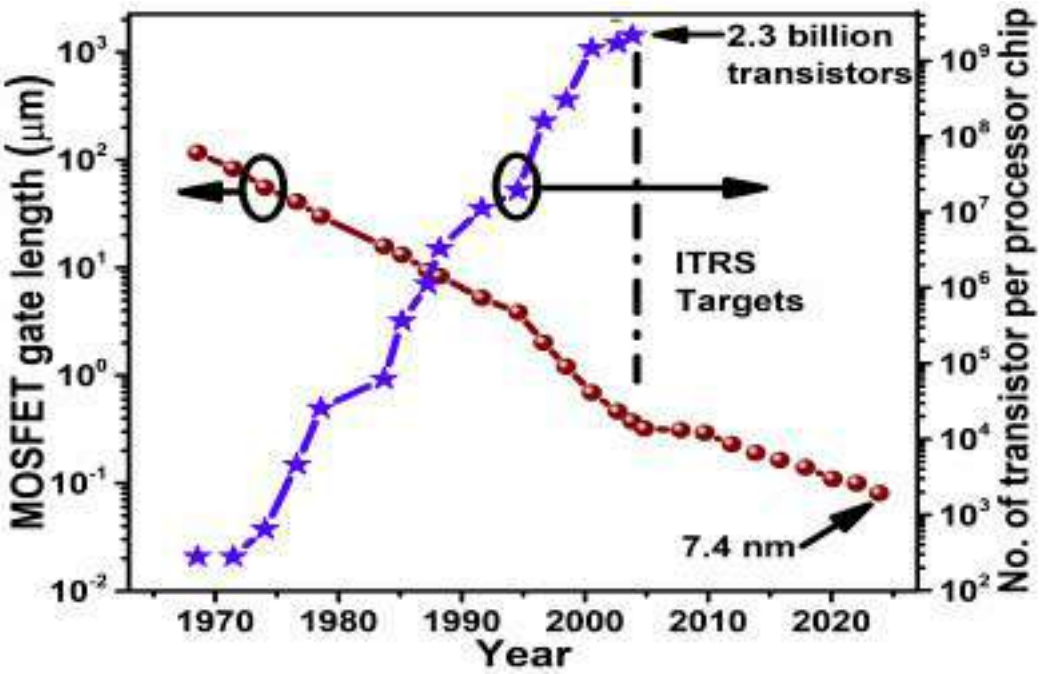

Figure 1.1: The plot of MOSFET gate length vs Year and No. of Transistor per processor chip vs Year(Rad13).

However, scaling devices down to the nanoscale presents formidable challenges due to issues such as increased leakage currents, higher power dissipation, pronounced short-channel effects (SCEs), quantum mechanical influences, and thermal management concerns (Kuh11; RMMM03). In con-

ventional transistors, aggressive gate length scaling enhances drive current (I_{on}) but deteriorates electrostatic control, leading to increased subthreshold leakage (I_{off}). Due to narrow channel length in deeply scaled MOSFETs, the drain potential begins to influence the electrostatics of the channel, and consequently, the gate loses adequate control over the channel. As a result, the gate cannot shut off the channel completely in the off-mode of operation, which leads to an increased I_{off} between the drain and the source as showcased in Figure 1.2 (hpm). Moreover, these devices exhibit prominent SCEs, such as threshold voltage (V_{th}) roll-off, drain-induced barrier lowering (DIBL), and degradation of the subthreshold slope, all of which contribute to higher power consumption. Among the most pressing concerns in conventional CMOS-based integrated circuits and systems is the continuous rise in power demand. To address this, steep-subthreshold swing transistors have been proposed due to their ability to operate at reduced supply voltages makes them attractive candidates for future energy-efficient circuit and system design (RGK+21).

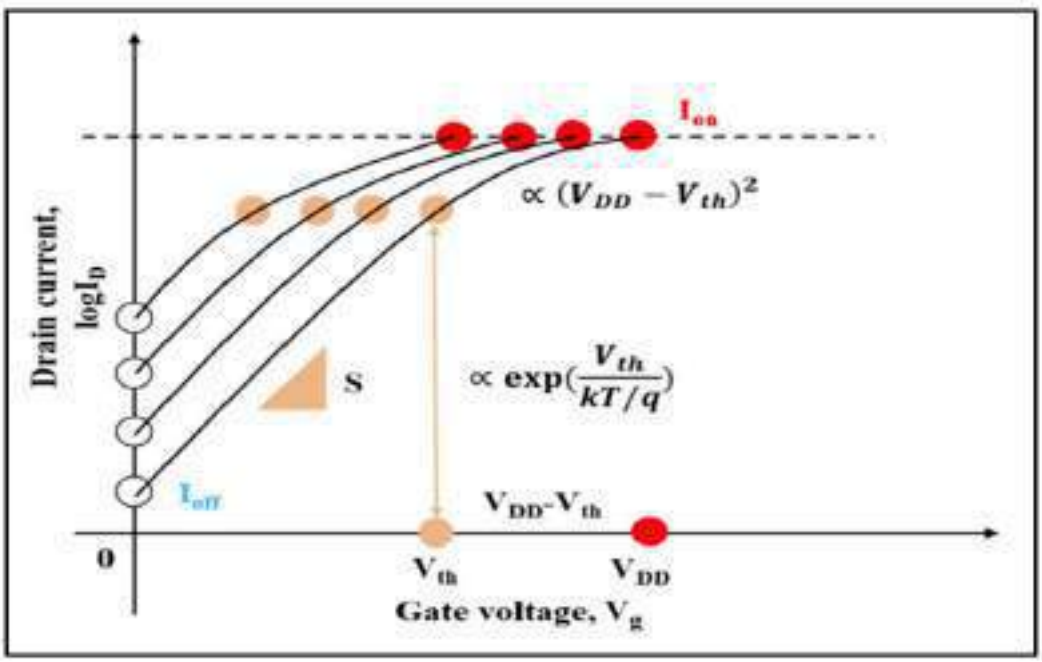

Figure 1.2: The I_d -V_g characteristics for conventional transistor with scaling of gate length (hpm).

1.2 Literature Review

The fundamental goal of VLSI and ULSI technology has consistently been to enhance the switching speed of logic circuits while simultaneously reducing the cost per logic function. The most direct pathway to achieving this objective has been the systematic downscaling of device dimensions,

which has enabled successive generations of integrated circuits with reduced power dissipation, higher operational speed, and increased packing density of transistors (XLX+13; CK04).

1.2.1 Device Scaling

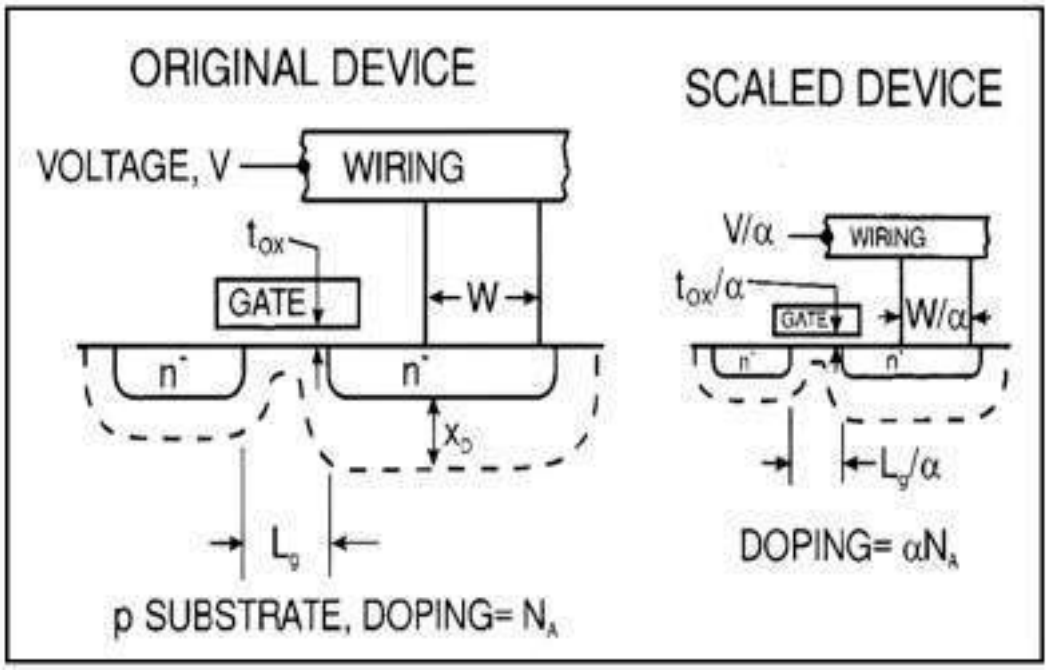

Figure 1.3: Principles of constant field scaling for MOSFETs and integrated circuits (RGK+21).

The concept of scaling theory was first formalized by Dennard et al., who demonstrated that the dimensions of MOS transistors could be reduced without adversely affecting their voltage–current characteristics. They proposed scaling rules that preserve device functionality while improving performance, leading to the development of two primary methodologies: constant field scaling and constant voltage scaling. Under constant field scaling , all device dimensions and supply voltages are reduced by a factor α (>1). This proportional scaling maintains the electric field within the transistor at the same level as that of the original device as showcased in Figure 1.3(Kuh11; RGK+21). Such scaling achieves significant reductions in the power-delay product, enhances switching speed, and lowers overall power consumption. However, a key implication is that reducing the minimum feature size also necessitates a proportional reduction in supply voltage, which complicates compatibility with existing technologies(XLX+13). In constant voltage scaling, the device dimensions are scaled down while the supply voltage is kept constant. The primary advantage lies in voltage compatibility with previous generations of circuits, ensuring easier technology integration. However,

this comes at the expense of increased internal electric fields as the feature size shrinks, which results in adverse effects such as carrier velocity saturation, enhanced leakage currents, lower breakdown voltages, and mobility degradation. When developed in 1960, the channel length of the MOSFET was around 10 μm. Today most of the integrated circuits utilize CMOS technology with channel length around sub-nm range.

Scaling down offers the subsequent benefits such as(Rad13; KA08):

(a) Higher Integration Density: Shrinking feature sizes allow more transistors to be fabricated per silicon wafer, thereby reducing the cost per function and enabling complex, large-scale circuits.

(b) Improved Switching Speed: Scaling reduces parasitic capacitances, which directly enhances the operational speed of ICs and minimizes propagation delays.

(c) Reduced Power Consumption: Lower supply voltages and smaller capacitances contribute to reduced dynamic power dissipation, thereby improving energy efficiency.

Nevertheless, scaling down has its own set of challenges such as(XLX$^+$13; RGK$^+$21):

(a) Increased Electric Fields and Gate Leakage: As oxide thickness reduces, the electric field within the gate dielectric rises significantly, leading to gate tunneling currents and reliability concerns.

(b) Escalating Power Dissipation: Both static power (due to leakage currents) and dynamic power (due to high switching activity) rise sharply with scaling, leading to thermal management challenges.

(c) Heat Generation and Reliability Issues: Elevated power densities can cause overheating, potential device degradation, and in extreme cases, material evaporation, which limit further downscaling.

Beyond these classical limitations, quantum mechanical effects such as direct tunneling through ultrathin gate oxides, random dopant fluctuations, and variability in threshold voltage become increasingly prominent at nanometer nodes. These effects degrade device reliability and pose major obstacles for continued CMOS scaling. Furthermore, thermal management becomes a dominant concern, as the localized heating in densely packed transistors severely impacts lifetime and performance.

1.2.2 Short Channel Effects

The aggressive downscaling of transistor dimensions has introduced several critical challenges, the most prominent being SCEs. These effects arise when the channel length of a MOSFET becomes comparable to, or smaller than the depletion layer widths of the source and drain junctions. Under such conditions, the gate loses complete control over the channel potential, and the electrostatics of the device are strongly influenced by the drain bias. As the channel length is further reduced, SCEs intensify, leading to substantial deviations in the device's electrical behavior. This not only degrades performance metrics such as switching speed, leakage current, and subthreshold slope but also complicates compact modeling and long-term reliability analysis(XLX+13; RGK+21).

1.2.2.1 Threshold Voltage Roll-off

Threshold voltage (V_{th}) roll-off is one of the most critical short-channel effects observed in nanoscale MOSFETs. It refers to the reduction in the threshold voltage as the channel length is scaled down. In long-channel devices, the gate electric field exerts strong control over the channel potential, ensuring stable threshold characteristics. However, as the channel length approaches the depletion widths of the source and drain junctions, the drain and source fields begin to penetrate into the channel region. This weakens the gate's ability to control carrier transport, leading to a noticeable decrease in threshold voltage. The physical origin of this effect lies in the two-dimensional electrostatic interaction within short-channel devices. In particular, the lateral field from the drain lowers the source-channel potential barrier, which effectively reduces the gate voltage required to induce conduction. As a result, a short-channel MOSFET exhibits a smaller threshold voltage as compared to its long-channel counterpart, thereby increasing leakage current and reducing noise margins in circuits. Mathematically, threshold voltage roll-off can be expressed as the difference between the threshold voltage of a short-channel MOSFET and that of a long-channel MOSFET. The severity of roll-off depends on several device parameters, including channel length, oxide thickness, junction depth, and dielectric constant of the gate material(RGK+21; Kha16).

1.2.2.2 Drain-Induced Barrier Lowering

The phenomenon of drain-induced barrier lowering (DIBL) can be understood by analyzing the potential barrier profile that an electron encounters while traveling from the source to the drain. In the equilibrium state, when both the gate-to-source voltage (V_{gs}) and drain-to-source voltage (V_{ds}) are zero, a potential barrier exists between the source and the channel, effectively preventing electron flow from the source to the drain. When a positive gate voltage is applied, this barrier is reduced, allowing electrons to surmount it and establish conduction through the channel. In an ideal long-channel device, the gate is the sole terminal responsible for modulating this barrier. However, as MOSFETs are aggressively scaled to shorter channel lengths, the situation changes drastically. A higher V_{ds} causes the drain depletion region to extend significantly into the channel, which reduces the source-channel barrier height even before the gate voltage reaches the threshold value as showcased in Figure 1.4. As a result, the drain voltage indirectly lowers the barrier, enabling carriers to flow from the source to the drain at gate voltages lower than the threshold voltage. This undesired leakage mechanism is termed as DIBL(RMMM03; YWN+97).

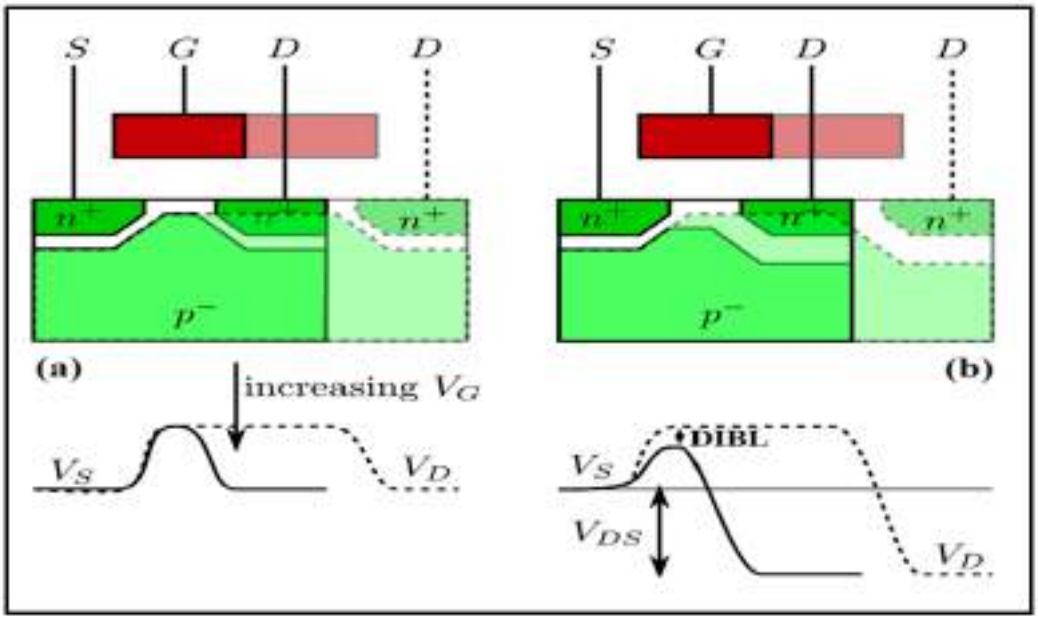

Figure 1.4: Drain Induced Barrier Lowering (DIBL) (YWN+97).

1.2.2.3 Hot-Carrier Effects

Hot-Carrier Effects (HCEs) encompass a class of reliability-degrading phenomena that occur when charge carriers (electrons or holes) acquire excess kinetic energy due to the presence of strong

electric fields or high applied voltages within a MOSFET channel. These highly energized carriers—commonly referred to as hot carriers that can damage the device structure and progressively degrade its electrical performance over time, posing a major challenge to transistor scaling.

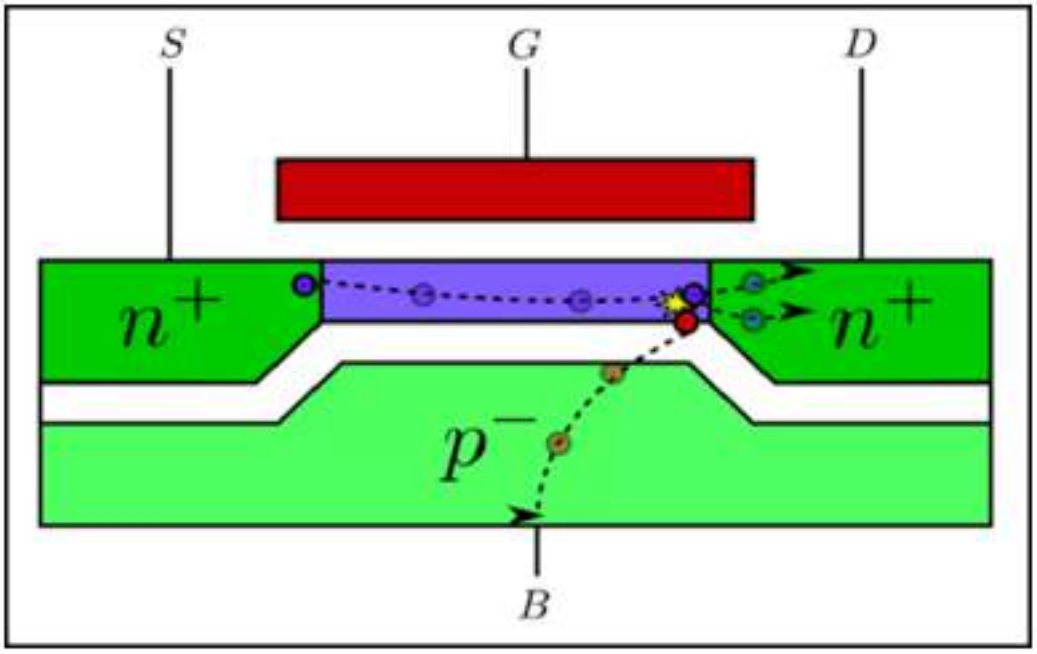

Figure 1.5: Hot Carrier Effects (hpm)

Among the various manifestations of HCEs, the two most prevalent are Hot-Carrier Injection (HCI) and Channel Hot-Carrier Injection (CHCI). In the case of HCI, energetic carriers either remain within the channel or gain sufficient energy to surmount the energy barrier at the semiconductor–gate oxide interface, enabling them to enter the gate oxide layer as showcased in Figure 1.5. Once injected into the oxide, they may become trapped in pre-existing or newly generated defect states, leading to permanent shifts in threshold voltage (V_{th}), mobility degradation, and transconductance reduction. In contrast, in CHCI, the carriers gain substantial energy but do not penetrate the oxide. Instead, they impact the channel region, altering its properties through localized damage mechanisms(Sax09; hpm).

A critical sub-mechanism associated with HCI is impact ionization. When a carrier's kinetic energy exceeds the semiconductor bandgap energy, it can disrupt covalent bonds by colliding with lattice atoms, thereby generating additional electron–hole pairs. The resulting excess holes often flow into the substrate, producing a substrate current, while the newly generated electrons can either contribute to channel conduction or become injected into the oxide, compounding device degradation. Another important variant is Hot-Electron Injection (HEI), in which electrons gain

sufficient energy to overcome the potential barrier at the semiconductor–oxide interface. These injected electrons, once trapped within the oxide, cause a build-up of localized charge that permanently alters the gate control mechanism(TMT$^+$05; WSZ$^+$24). This results in V_{th} instability, increased subthreshold leakage, degraded drive current, and reduced switching speed.

1.2.2.4 Surface scattering

Surface scattering is a key mobility-limiting mechanism in MOSFETs that arises when charge carriers (electrons or holes) traveling through the channel collide with the irregularities present at the semiconductor–oxide interface, as illustrated in Figure 1.6. These irregularities, often referred to as surface roughness, originate from imperfections during device fabrication, interface traps, or intrinsic structural variations. As MOSFET dimensions continue to shrink and the channel region becomes increasingly thin, the carriers are forced to move closer to the interface, thereby experiencing stronger interactions with surface roughness. Each collision randomizes the momentum of carriers, effectively scattering them and reducing their effective mobility (μ_{eff}). This mobility degradation leads to lower current drive capability, reduced transconductance (g_m), and deterioration of switching performance(RGK$^+$21; Kha16).

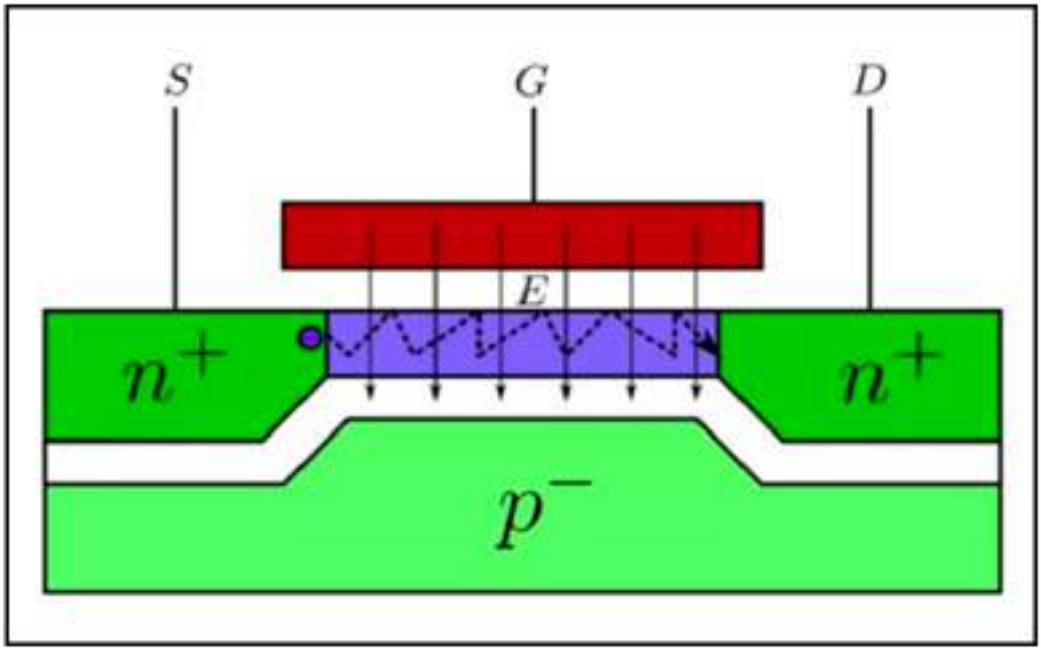

Figure 1.6: Surface Scattering (RGK$^+$21).

In short-channel devices, where the gate oxide thickness is minimal and the inversion layer lies extremely close to the surface, surface scattering becomes particularly dominant compared to other

scattering mechanisms such as phonon or ionized impurity scattering. Consequently, it emerges as a critical performance bottleneck in nanometer-scale CMOS technologies. Moreover, surface scattering not only degrades carrier transport efficiency but also impacts analog and RF circuit performance, as it reduces linearity and gain. In high-performance and low-power applications, this effect translates into higher delay, degraded drive currents, and increased susceptibility to variability(RGK+21; Kha16).

Hence, while device scaling has historically delivered enormous benefits in terms of performance, cost, and integration, its continued application faces physical and technological barriers that demand innovative device architectures, such as FinFETs and ferroelectric-gated structures, to sustain progress in VLSI/ULSI technology.

1.2.3 Strategies for Mitigating Short-Channel Effects

To ensure that a physical short-channel device continues to exhibit the desirable electrical characteristics of a long-channel MOSFET, it is essential to minimize or suppress SCEs, as they significantly hinder device operation and overall performance. Extensive device engineering approaches have been investigated to effectively suppress SCE-induced performance degradation and enhance device reliability in advanced transistors. Here are some engineering techniques to address SCEs as discussed below.

1.2.3.1 Channel based Engineering

Channel engineering refers to the techniques used to modify or engineer the channel region of field-effect transistors (FETs). Channel engineering schemes aim to improve FET performance by manipulating the channel properties, carrier mobility, and electrostatic control thus improve the device performance, achieve specific electrical characteristics, and address limitations in conventional FET structures. Here are some common channel engineering schemes employed in FETs(TMT+05; MSS10; FLLA03; Kim10).

(A) Doping Profile Engineering

(i) Doping Concentration Control: Precise modulation of doping levels within the channel

allows for fine-tuning of carrier density, mobility, and threshold voltage. By optimizing these parameters, devices can achieve improved subthreshold behavior and reduced variability. For instance, in junctionless transistors, careful adjustment of uniform doping ensures consistent conductivity throughout the channel, thereby simplifying fabrication while maintaining effective electrostatic control.

(ii) Graded Channel Doping: As as showcased in Figure 1.7, introducing a non-uniform or graded doping profile across the channel region helps to smooth out potential barriers, thereby enhancing carrier transport.

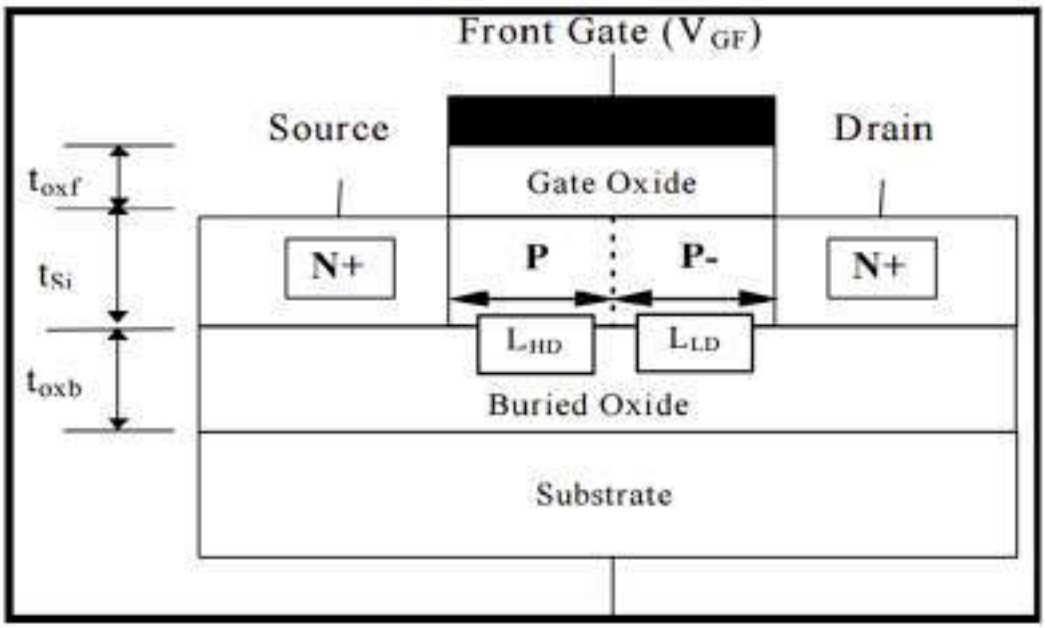

Figure 1.7: Schematic view of n-channel SOI-MOSFET showing graded channel doping (TMT+05).

(iii) Delta Doping: Incorporating ultra-thin, highly localized layers of dopants enables strong confinement of carriers near the intended region. This reduces carrier scattering and enhances mobility by maintaining a high-quality transport path. Delta doping is particularly useful in high-speed and low-power applications, where superior channel conductivity and reduced noise are required.

(iv) Halo Implants: Introducing localized halo (or pocket) doping near the source and drain junctions using angled implantation. The presence of this halo region helps to strengthen the channel's potential barrier, thereby suppressing undesirable short-channel effects such as threshold voltage roll-off and DIBL.

(B) Strained Channel Engineering

(i) Strain Engineering: By applying mechanical strain to the silicon lattice, the band structure of the material can be modified to favor higher carrier mobility. Tensile strain enhances electron mobility in n-channel MOSFETs, while compressive strain improves hole mobility in p-channel MOSFETs. This engineering approach increases drive current, reduces delay, and significantly boosts transistor performance without altering device dimensions.

(ii) Alloy-Based Channels: The use of alternative semiconductor materials, such as germanium (Ge) or silicon-germanium (SiGe) alloys, offers superior carrier mobility compared to pure silicon. Ge-rich channels, for instance, reduce effective carrier mass, thereby improving transport properties. These alloy-based channels are especially advantageous in high-frequency, analog, and RF circuits, where faster carrier dynamics are critical.

(C) Bandgap Engineering

Heterostructure FETs: Incorporating heterostructures or using different semiconductor materials with varying bandgaps enables better confinement and control of carriers within the channel. By creating tailored energy barriers, heterostructure-based devices reduce leakage, suppress short-channel effects, and achieve enhanced current drive. Examples include GaAs/AlGaAs HEMTs and III-V channel MOSFETs, which exploit the superior transport properties of wide and narrow bandgap materials for high-speed and low-power applications [24].

1.2.3.2 Gate Engineering

Gate engineering refers to a collection of techniques aimed at modifying and optimizing the gate structure, geometry, and materials of field-effect transistors (FETs) to achieve superior device performance. Since the gate serves as the primary control terminal governing channel conduction, its design has a profound impact on parameters such as threshold voltage, leakage current, subthreshold swing, and overall electrostatic integrity. In advanced CMOS technologies, gate engineering has become indispensable for extending device scaling and addressing the challenges associated with short-channel effects, power dissipation, and variability. By introducing novel gate architectures and materials, it is possible to achieve higher switching speeds, reduced

operating voltages, and improved energy efficiency, while ensuring compatibility with large-scale integration(SSS18; SGG11; SB12; Ren01).

(A) Gate Dielectric Engineering

(i) High-k Dielectrics: The replacement of conventional silicon dioxide (SiO_2) with high-permittivity (high-k) materials, such as hafnium oxide (HfO_2), zirconium oxide (ZrO_2), or lanthanum oxide (La_2O_3), significantly enhances gate capacitance while allowing the use of a physically thicker dielectric layer as showcased in Figure 1.8. This reduces direct tunneling leakage currents, thereby improving device reliability and scalability at nanometer dimensions.

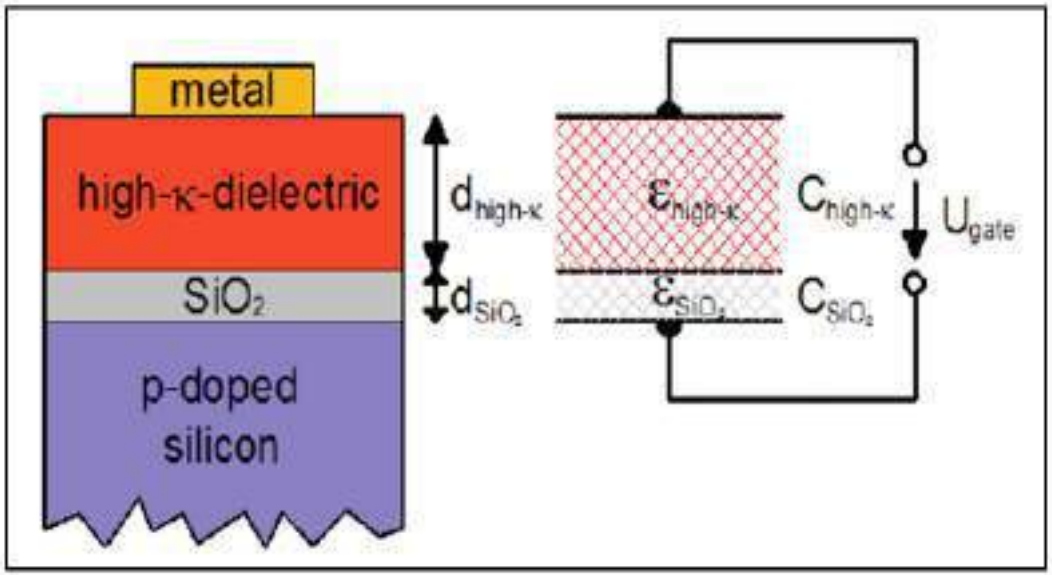

Figure 1.8: Schematic structure of a gate stack with a high-k dielectric layer (SGG11).

(ii) Dual Gate Oxides: Employing two different gate oxide thicknesses within the same device enables optimization of trade-offs between gate control and leakage suppression. Thicker oxides can minimize leakage in certain regions, while thinner oxides allow stronger electrostatic control of the channel, thereby enhancing subthreshold behavior.

(B) Gate Electrode Material Optimization

(i) Metal Gate Technology: Traditional polysilicon gates suffer from depletion effects and high resistivity, which limit performance in scaled devices. Transitioning to metal gate electrodes eliminates polysilicon depletion, reduces gate resistance, and provides better compatibility with high-k dielectrics, thereby improving overall transistor switching speed and reliability.

(ii) Work-Function Engineering: Selecting appropriate gate materials with tailored work

functions allows precise adjustment of the transistor's V_{th}. This ensures improved power-performance trade-offs across both nMOS and pMOS devices, enabling balanced operation in complementary MOS (CMOS) circuits.

(iii) Dual Material Gate Engineering: As showcased in Figure 1.9, Dual Material Gate (DMG) MOSFET is a novel device structure designed to reduce SCEs while simultaneously improving carrier transport velocity. Its gate consists of two adjoining materials with different work functions: the source-side metal possesses a higher work function, whereas the drain-side metal has a comparatively lower one. This leads to a threshold voltage relationship of $V_{th1} > V_{th2}$, which promotes efficient carrier movement. Additionally, employing a lower work function metal near the drain reduces the electric field intensity in that region, thereby minimizing hot-carrier effects.

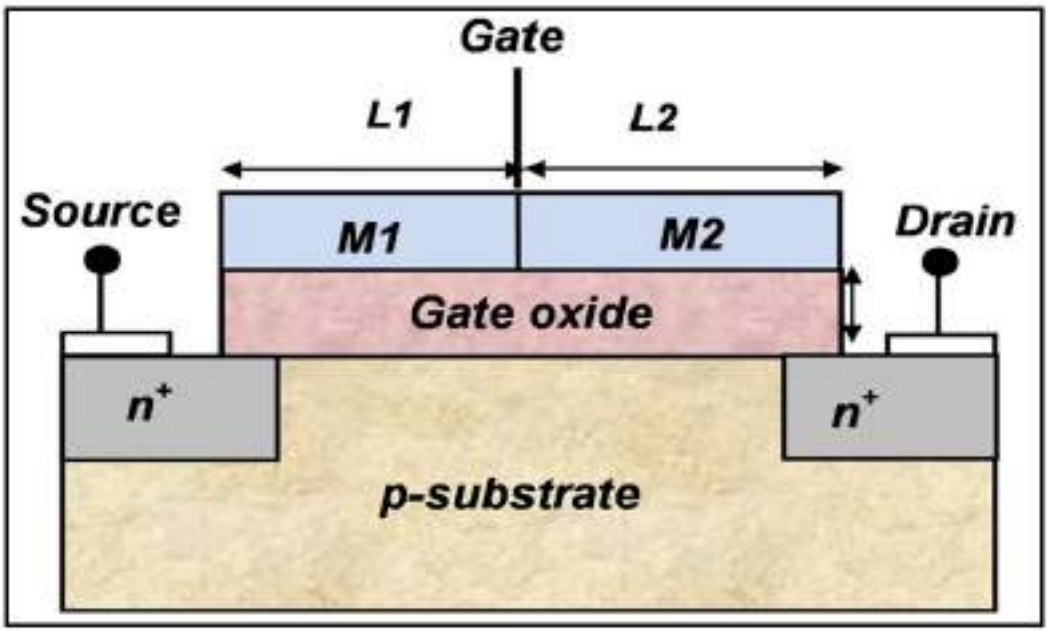

Figure 1.9: Schematic structure of Dual Material Gate MOSFET (SB12).

(C) Multigate Transistor Architectures

(i) Double Gate MOSFET: The Double Gate MOSFET is considered a highly promising device structure because the dual-gate configuration provides an effective shielding effect, significantly reducing DIBL and limiting the threshold voltage dependence on channel length. In this design, the silicon channel is placed between two separately fabricated gate/oxide stacks as showcased in Figure 1.10. By keeping the silicon channel width extremely small and applying gate contacts on both sides, the channel can be controlled more effectively, which suppresses short-channel effects and enables higher drive currents compared to single-gate MOSFETs.

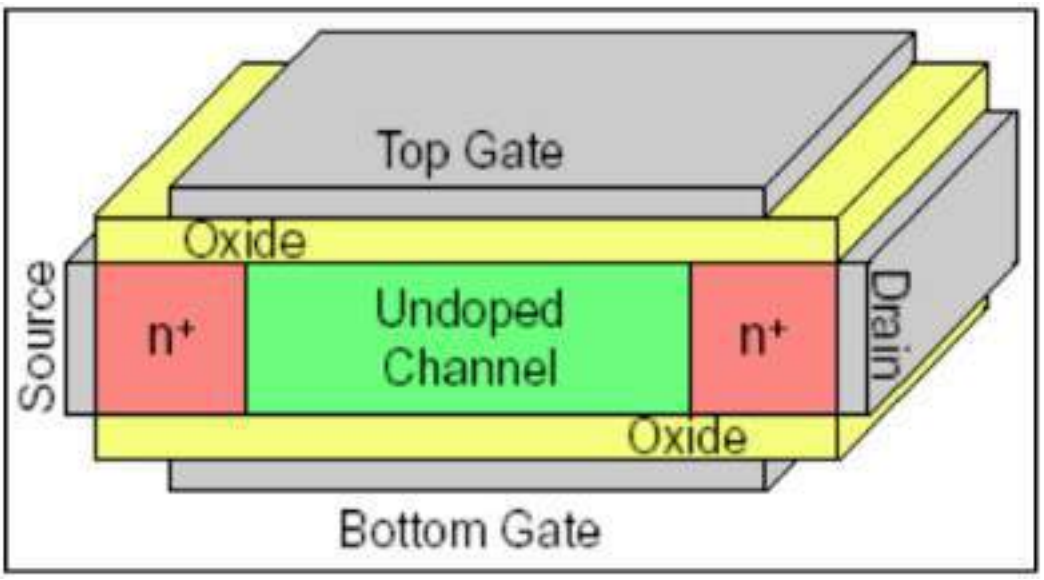

Figure 1.10: Schematic view of n-channel Double gate MOSFET (Ren01).

(ii) FinFET: By extending the gate to wrap around a vertical silicon fin, FinFETs provide superior electrostatic control over the channel from multiple sides as showcased in Figure 1.11. This three-dimensional structure effectively suppresses SCEs, enhances drive current, and reduces leakage, making FinFETs a dominant technology for sub-10 nm nodes.

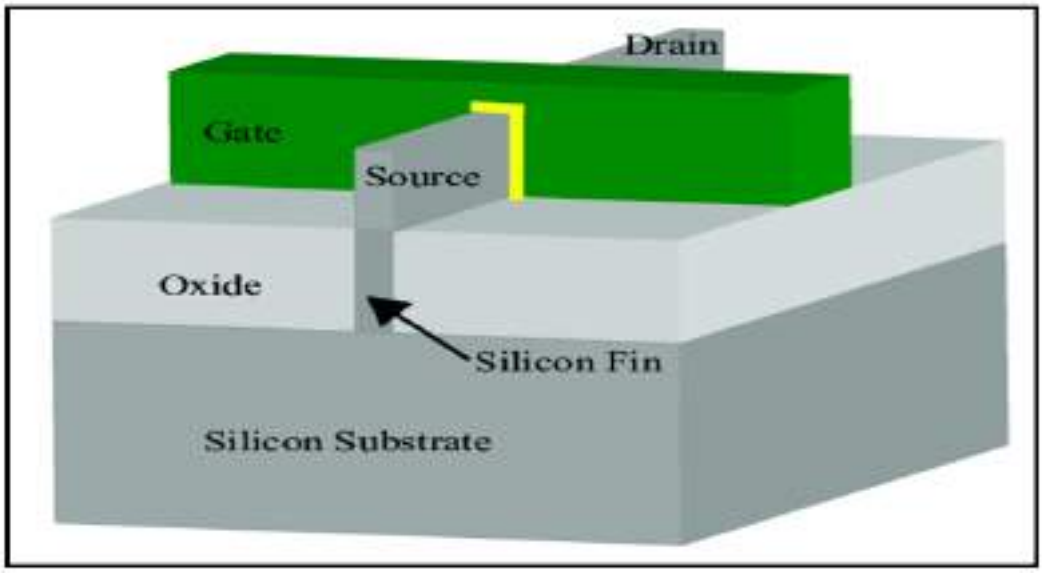

Figure 1.11: Schematic view of 3D FinFET (SGG11).

(iii) Gate-All-Around (GAA): GAA devices extend the multigate concept further by completely surrounding the channel, whether in the form of nanowires or nanosheets, with the gate electrode as showcased in Figure 1.12. This configuration offers near-ideal electrostatic control, scalability beyond FinFETs, and significantly reduced off-state leakage.

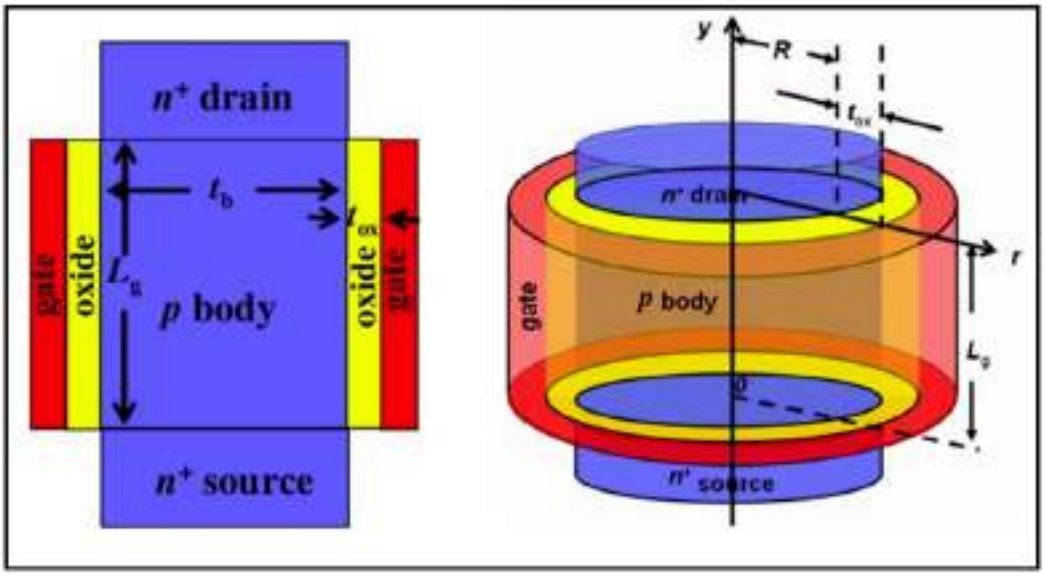

Figure 1.12: Cross-sectional view of Gate-All-Around MOSFET with the coordinate system (SB12).

(D) Gate Sidewall Spacer Engineering Sidewall spacers are dielectric materials deposited alongside the gate electrode as showcased in Figure 1.13. These spacers not only help define source/drain extension regions during fabrication but also play a crucial role in suppressing SCEs by adjusting fringing fields. Additionally, they aid in reducing parasitic capacitances and improving channel control in nanoscale devices.

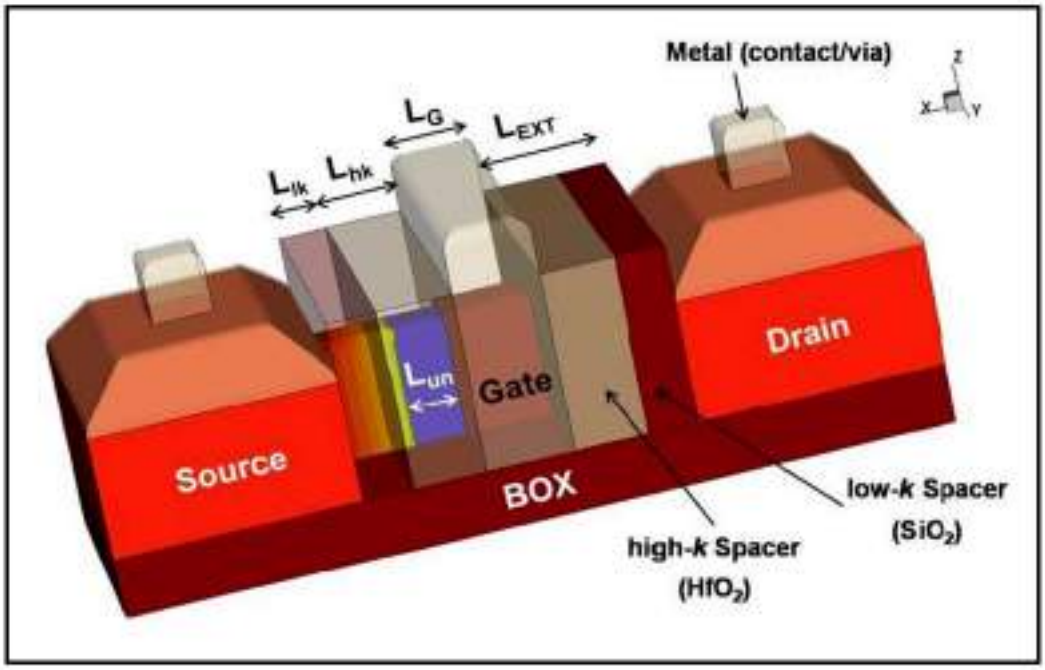

Figure 1.13: Schematic structure of FinFET with gate sidewall spacers (Ren01).

1.2.4 Research Gaps

Research gaps identified after reviewing the literature are as follows, which will be attempted to address via possible solutions:

(i) Scaling devices down to a few nanometers is a regime challenging to achieve with conventional device architectures. As, devices are scaled down, the benefits of higher electric fields saturate while the associated reliability problems get worse. Addressing these challenges is essential for sustaining device performance and ensuring efficient operation at the nanoscale.

(ii) The rise in off-state leakage current with the decreasing gate oxide thickness is another severe issue. This leakage results from quantum mechanical tunnelling, which limits the device scaling and negatively impacts the performance of the device.

(iii) Densely packed VLSI and ULSI circuits often run at high temperatures due to heat production, and excessive temperatures might harm or influence the functioning of the nanoscaled devices. Therefore, device reliability must be inspected to guarantee long-term endurance and stability.

(iv) The parasitic capacitance and SCEs become more significant at the sub-nm range, deteriorating device performance. Thus, thoroughly examining these impacts is essential to improve the device's performance.

(v) FET-based electronic devices are extensively employed in fundamental circuit elements such as inverters, logic gates, and other building blocks of digital systems due to their superior switching characteristics and scalability. With the continuous push toward miniaturization and high-performance computing, there is an increasing demand for advanced FET architectures that can deliver enhanced speed, reduced power consumption, and improved reliability for next-generation integrated circuits.

1.2.5 Possible Solution-Ferroelectric based FinFET

1.2.5.1 Development and Prospects

It is generally accepted that the ongoing scaling of field effect transistors will be eventually limited by the inability to reduce the heat generated in the switching process, making it very important to find ways to reduce the power dissipated per switching event. It is also clear that the power

dissipation would be lowered significantly if FETs could be operated at lower voltage(hpm; Rad13). Multiple device topologies have been engineered to alleviate these difficulties, including multi-gate MOSFET, TFETs, HEMTs, and FinFETs, but failed to meet the requirements(WSZ+24; RGK+21; SB12). In this regard, steep subthreshold slope transistors are critical for reducing the supply voltage and achieving low power requirements. TFET and FeFET, both are steep-slope transistors developed to overcome the subthreshold swing limitation of conventional MOSFETs, enabling low-power operation. While TFET operates on band-to-band tunneling, it suffers from low ON-current due to limited tunneling efficiency, especially at low supply voltages. In contrast, FeFET utilizes ferroelectric polarization to achieve internal voltage amplification, resulting in significantly higher ON current and lower OFF-current as showcased in Figure 1.14(WSZ+24; WYSK15). Additionally, FeFETs are CMOS-compatible and can function as both logic and non-volatile memory devices, making them more versatile and better suited for high-performance, low-power applications as compared to TFETs. The ON current of FeFET is enhanced by implementing a ferroelectric layer placed between metal gate and an interfacial or insulating layer that is completely compliant with conventional MOSFETs or FinFETs as showcased in Figure 1.15(RAT07; WYSK15).

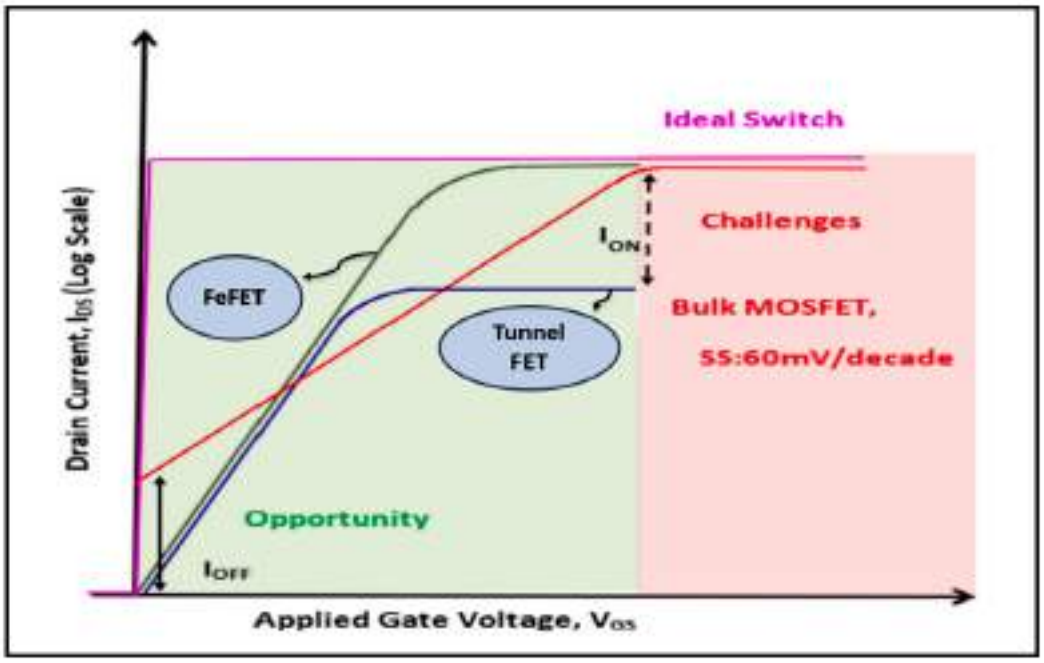

Figure 1.14: Comparison of transfer characteristics of TFET and FeFET with conventional MOSFET (WYSK15).

Ferroelectric materials are characterized by the presence of spontaneous electric polarization even in the absence of an external stimulus and the direction of polarization can be switched by

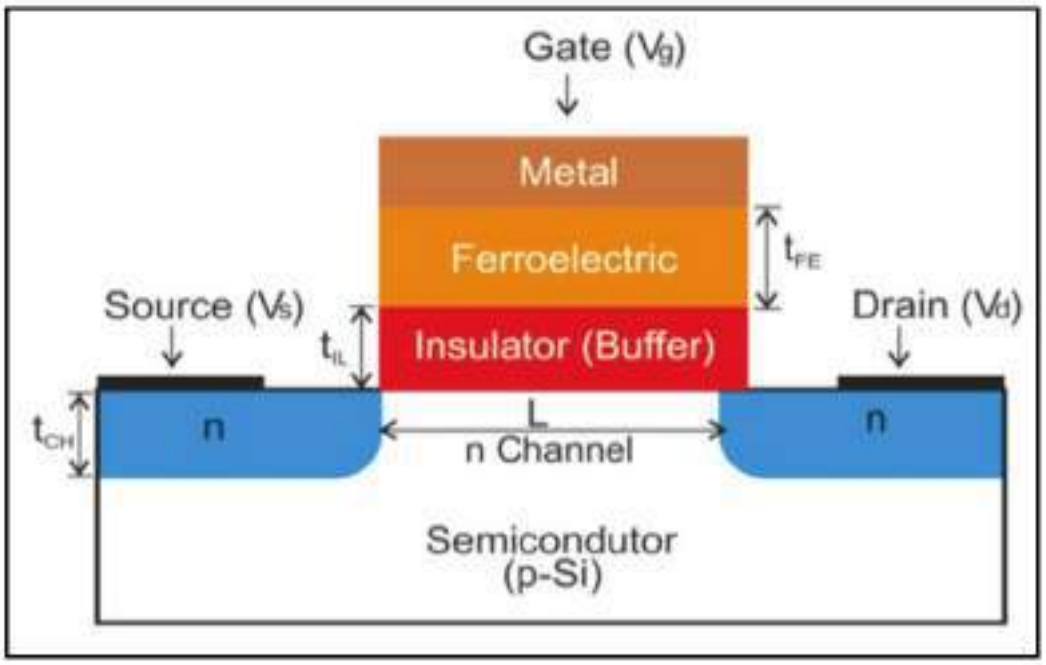

Figure 1.15: Schematic image of an FeFET with ferroelectric and conventional dielectric as the gate stack (RAT07).

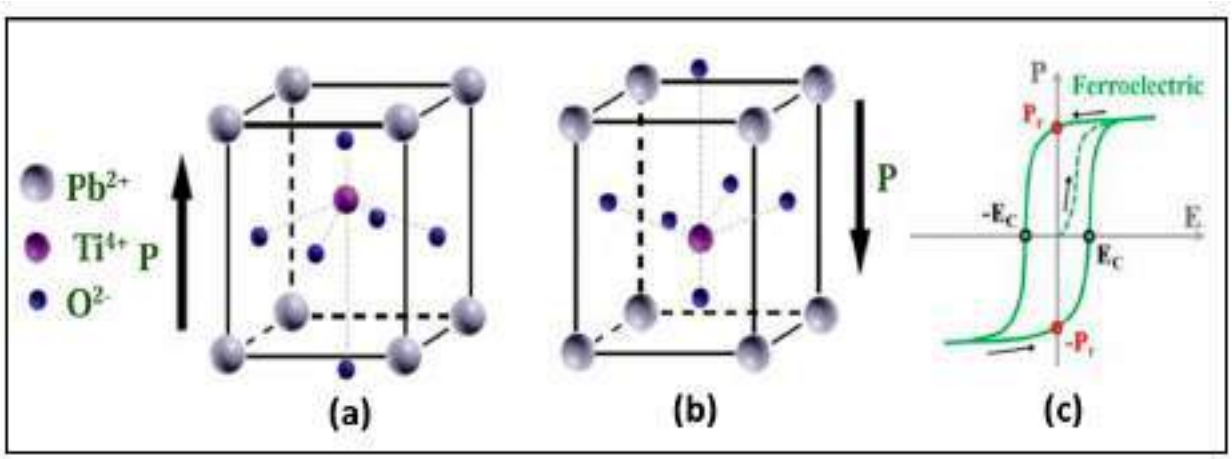

Figure 1.16: Atomic structure of $Pb^{2+}Ti^{4+}O_3{}^{6-}$ for (a) ferroelectric with up polarisation and (b) ferroelectric with down polarisation (c) The plot of polarisation vs electric field for ferroelectric (Uch18).

applying an external electric field. For a material to exhibit ferroelectricity, its crystal structure must lack inversion symmetry, i.e., it should be non-centrosymmetric which result in polarization switching under an applied field as showcased in Figure 1.16(WYSK15; Uch18; JGTY22).

A wide range of bulk ferroelectric materials have been synthesized, many lose their ferroelectric behavior when scaled down to very thin dimensions due to the influence of depolarization fields. Some materials such as perovskites, have demonstrated the ability to sustain ferroelectricity even

at the nanometer or unit-cell level. For example, $PbTiO_3$ thin films with thicknesses between 6–80 nm, synthesized by (LTGJ05), retained ferroelectricity at such scales. Similarly, (BFD$^+$98) prepared ultrathin monolayers of P(VDF-TrFE) only 10 Å thick with ferroelectric properties. (TAT99) reported ferroelectricity in tetragonal perovskite $Pb(Zr_{0.2}Ti_{0.8})O_3$ films at a thickness of 40 Å, and (JG03) observed such behavior in four-unit-cell-thick $BaTiO_3$ films. Later, (KKD20a) demonstrated that ultrathin (2.5 nm) $Hf_{0.5}Zr_{0.5}O_2$ layers on Si substrates remain ferroelectric, and (Pea20) fabricated freestanding $BiFeO_3$ with thicknesses of only a few unit cells, exhibiting a tetragonal phase with robust ferroelectricity. In certain systems, ferroelectricity persists at low thicknesses but with a weakened polarization strength to compensate for the depolarization field, which results from charge accumulation at surfaces. This effect is strongly dependent on thickness, surface conditions, and substrate interactions. Consequently, achieving stable ferroelectric properties at the ultrathin scale continues to be a critical research challenge. A major drawback of conventional ferroelectrics, particularly perovskite oxides, is the progressive suppression of polarization when the film thickness is reduced to just a few nanometers(MRVB97; KMG$^+$05; KKD20a). This suppression originates mainly from depolarization fields which limit the scalability of such materials for modern nanoelectronic devices. Thus, as device dimensions continue to shrink as per the scaling trend, the inability of classical ferroelectrics to retain stable polarization at ultrathin levels presents a critical bottleneck for their practical integration(BYJ$^+$22).

This limitation was addressed through the discovery of ferroelectricity in hafnium oxide (HfO_2)-based thin films, particularly when doped with elements such as zirconium, silicon, yttrium, or aluminium. Unlike perovskites, doped HfO_2 maintains ferroelectricity even at thicknesses below 10 nm, making it fully compatible with advanced CMOS technology nodes(SSG$^+$19). The origin of ferroelectricity in these films lies in the stabilization of a non-centrosymmetric orthorhombic phase through appropriate doping, mechanical stress, and interface engineering. The scalability, robustness, and silicon process compatibility of HfO_2-based ferroelectrics mark a turning point in the search for materials suitable for next-generation ferroelectric devices and logic applications. As a result, HfO_2-based ferroelectrics are now considered prime candidates for advanced FeFETs(TIW$^+$21).

The integration of HfO_2 ferroelectrics into devices led to the development of the Ferroelectric Field-Effect Transistor (FeFET), where a ferroelectric thin film replaces the conventional gate

dielectric. The remanent polarization in the ferroelectric layer modulates the channel charge, allowing the device to function as a low-power, non-volatile memory element with fast switching speeds. FeFETs thus combine memory and logic in a single device structure, but planar designs encounter limitations at deeply scaled nodes, including short-channel effects, increased leakage, and restricted drive currents(MRVB97; SSS18; BYJ+22). To address these challenges, ferroelectric transistors have evolved into the Ferroelectric FinFET (FeFinFET) architecture. In this configuration, the fin-shaped channel offers superior electrostatic control and enhanced gate coupling, which strengthens polarization switching and improves device characteristics. At the same time, the three-dimensional geometry reduces leakage currents and boosts drive strength, making FeFinFETs more scalable and power efficient than their planar counterparts(RZN19; BK19). The transition from FeFETs to FeFinFETs therefore represents a natural progression in device engineering, combining the advantages of nanoscale ferroelectrics with advanced transistor architectures. In summary, the emergence of HfO_2-based ferroelectrics solved the long-standing problem of polarization suppression at nanoscale thickness, enabling the realization of ferroelectric transistors(LFH+18). Also, the subsequent shift from planar FeFETs to three-dimensional FeFinFETs reflects both material-level and device-level innovations, paving the way for highly scalable, energy-efficient, and multifunctional electronic systems.

1.2.5.2 Classification of FeFinFET

FeFinFETs can be further investigated in two distinct configurations, depending on the placement of the ferroelectric material within the gate stack as shown in Figure 1.17 as follows:

(a)MFMIS (Metal-Ferroelectric-Metal-Insulator-Semiconductor): In this structure, the ferroelectric material is positioned between two metal layers, followed by an insulator and a semiconductor layer. This configuration aims to leverage the properties of the ferroelectric material to control the behavior of the semiconductor channel through the polarization state of the ferroelectric layer.

(b) MFIS (Metal-Ferroelectric-Insulator-Semiconductor): This structure represents a type of FeFinFET where the ferroelectric layer is sandwiched between a metal layer (often used for electrodes), an insulator, and a semiconductor layer. The ferroelectric material's polarization state in the MFIS configuration can influence the conductivity or other properties of the semiconductor

channel, allowing for non-volatile memory or low-power logic applications(WSZ+24; MB24).

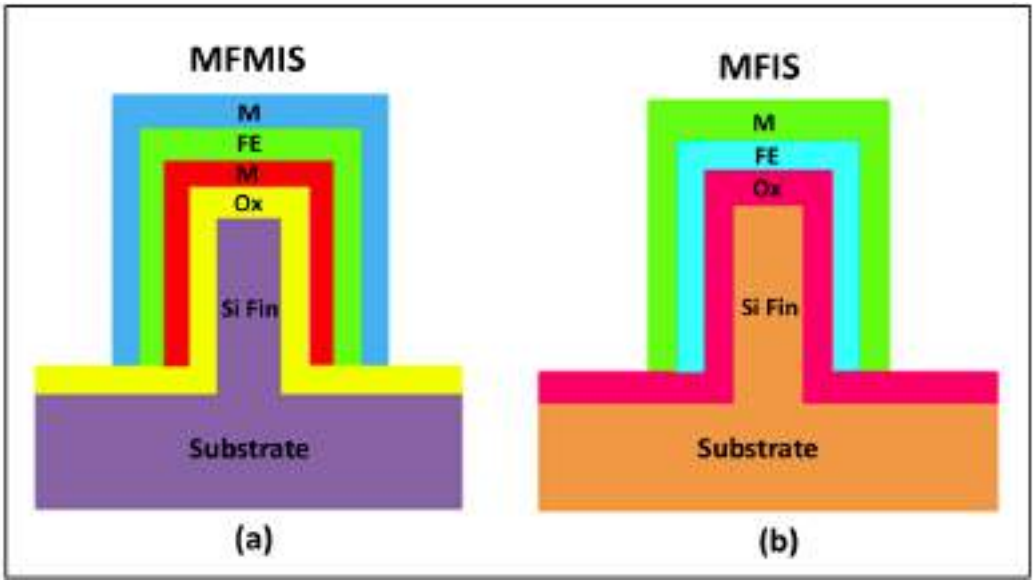

Figure 1.17: Structural view of FeFinFET in distinct configurations (a) MFMIS and (b) MFIS (WSZ+24).

1.2.5.3 FeFinFET Operation

(i) **Ferroelectric Effect in Gate**: Ferroelectric materials possess remanent polarization — they retain polarization even after the removal of the external electric field. When voltage is applied at the gate, the ferroelectric layer switches its polarization, which influences the channel charge.

(ii) **Channel Control**: The polarization of the ferroelectric layer modulates the surface potential in the channel. It leads to charge accumulation or depletion in the channel depending on the direction of polarization.

Case (a): When a positive gate voltage (V_{gate}) is applied: ON Condition: $V_{gate} > V_{th}$, V_{drain} = '+'ve, V_{source} = 0V

The physics of ferroelectric layer is modeled with time-dependent Landau–Khalatnikov (LK) equation for relating electric field used for the ferroelectric layer (E_{FE}) as a function of polarization (P) as given by Eq. 1.1(YWN+97; MSS10),

$$E_{\mathrm{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho(\frac{\partial P}{\partial t}) \tag{1.1}$$

where α, β, and γ are the static landau material-dependent coefficients while g is dipole interaction coefficient and ρ is viscosity coefficient. The polarization can amplify the surface potential in the

channel, effectively reducing the voltage required to switch the transistor. The ferroelectric dipoles align, enhancing the surface potential of the channel. This lowers the energy barrier for carriers (electrons/holes), allowing current to flow (ON-state)(TIW$^+$21; SR15; MB24).

Case (b): When $\mathbf{V}_{gate}$ is removed or reversed: OFF Condition: $\mathbf{V}_{gate} < \mathbf{0V}$, $\mathbf{V}_{drain}$ = '+' ve, $\mathbf{V}_{source} = \mathbf{0V}$

Due to remanent polarization, the ferroelectric layer retains its polarization temporarily. When the polarization opposes channel charge accumulation, the surface potential is reduced thus the channel is depleted, and the device remains in the OFF-state(TIW$^+$21; SR15).

1.2.5.4 Advantages of FeFinFET

FeFinFET provide numerous notable benefits compared to ordinary FETs, principally attributable to the distinctive characteristics of the ferroelectric material used in their gate stack. The following are the primary benefits:

(i) Steep Subthreshold Swing: FeFinFET can achieve a steep subthreshold swing. This enables quicker transitions between the ON and OFF state by means of smaller changes in voltage.

(ii) Lower operating voltage: Reduced subthreshold slope allows FeFinFET to function at lower voltages without compromising performance, resulting in substantial use for low power applications.

(iii) Enhanced Energy Efficiency: The capacity to function at lower voltages results in less dynamic power. This is essential for devices that rely on batteries and for applications that need significant computational power. FeFinFET have the ability to reduce leakage currents by effectively managing the channel at lower voltages. This capability aids in minimizing static power usage.

(iv) Improved Performance: FeFinFET have enhanced electrical performance in comparison to conventional transistors. These devices offer enhanced regulation of electron movement, leading to faster switching speeds and improved circuit performance. FeFinFET also provide superior control over SCEs, including DIBL and subthreshold slope degradation as compared to planar transistors.

(v) Scalability: The scalability of FeFinFET technology enables its seamless integration into smaller technology nodes such as 15 nm, 10 nm, and beyond. FeFinFET have been crucial in preserving Moore's law and enhancing transistor density as semiconductor manufacturers shift towards lower lithography nodes.

(vi) Compatibility with Existing Technology: FeFinFET may be seamlessly incorporated into current CMOS production methods with few modifications. This makes them a viable choice for the semiconductor industry seeking to improve existing technology without the need for a total restructuring of fabrication facilities.

(vii) Possibility for Innovative Applications: FeFinFET provide significant benefits for low-power applications, including as portable electronics, IoT devices, and other power-sensitive applications. FeFinFET are well-suited for high-performance computing workloads because to their enhanced performance characteristics, which are crucial for achieving both speed and power efficiency.

FeFinFET have a significant benefit in a way that they can operate at lower voltages and achieve improved performance. FeFinFET provide substantial energy efficiency, enhanced drive current, increased transconductance, and greater electrostatic control, positioning them as a very promising technology for forthcoming low-power and high-performance electronic devices.

1.2.5.5 Challenges Confronted by FeFinFET

Although FeFinFET have certain benefits, they also encounter several problems that must be resolved in order to fully exploit their potential in practical applications. The FeFinFET face many significant challenges such as:

(i) Stability and Material degradation in Ferroelectric Materials: Material degradation refers to the deterioration of ferroelectric materials, particularly when exposed to electric fields and heat conditions often seen in semiconductor devices. It is important to guarantee the enduring stability and dependability of these materials.

(ii) Thermal Budget: Ferroelectric materials sometimes need precise thermal treatments to get the appropriate characteristics. In order to prevent any harm to other components of the

device, it is essential that these treatments be consistent with the temperature budget of the CMOS process.

(iii) Uniformity of Ferroelectric Characteristics: It is difficult to achieve consistent ferroelectric characteristics across a wafer. Differences in device configurations might result in unreliable device functionality.

(iv) Parameter Extraction: Parameter extraction for FeFinFET from experimental data is difficult owing to the intricate interaction between the ferroelectric layer and the underlying FET structure.

(v) Variability and Reliability: Ensuring consistent performance across various devices on a chip is a significant challenge. Inconsistencies in device properties might arise from variations in the ferroelectric layer or its contact with other materials.

Although FeFinFET show potential benefits, there are still notable obstacles regarding material stability, control of ferroelectric properties, power-performance trade-offs, ferroelectric layer engineering, temperature sensitivity, and overall device reliability. To ensure the effective integration of FeFinFET technology in future electronic devices, it is crucial to address these problems by conducting more research and development.

1.3 Thesis Objectives

In the modern era, CMOS integrated circuits have become indispensable, powering technologies from portable electronics to communication systems and transportation. To continue extending Moore's Law, it is essential to explore advanced device architectures and their potential applications. The primary objective of this thesis is to investigate the combined benefits of an innovative device structure, namely the Ferroelectric FinFET (FeFinFET), together with engineering approaches such as gate, channel, and substrate engineering, in order to evaluate its suitability for both analog and circuit applications. This work critically addresses scaling-related challenges including short-channel effects and reliability concerns by proposing a SiGe/Si Strained Vertically Stacked FeFinFET (VS-FeFinFET). The performance of this structure is thoroughly compared against that of conventional devices using three-dimensional device and circuit simulations carried out with the Cogenda Visual

TCAD simulator. The findings demonstrate that the proposed architecture effectively mitigates the limitations of standard designs, while enhancing overall device characteristics. Furthermore, a detailed investigation is performed to optimize the device along with assessing its reliability and robustness at both the device and circuit level. The entire work in the present thesis is divided into six chapters based on the following objectives listed below:

1. To optimize and analyse the SiGe/Si strained vertically stacked FeFinFET (VS-FeFinFET) for high performance analog and RF applications.
2. To examine the effect of variation of mole fraction of alloy-based channel and fin dimensions on VS-FeFinFET to achieve a high-performance transistor.
3. Gate dielectric engineering with high-k dielectrics and oxide stacking can be investigated for VS-FeFinFET to improve the device performance.
4. To investigate the interfacial trap charges associated reliability performance of VS-FeFinFET and its interdependence on temperature and density variation with circuit-based digital applications.
5. To explore the material level and device level behavior in doped HfO2 based hetero dielctric VS-FeFinFET with self-heating and logic circuit perspectives.

The underlying goal of these objectives is to design and optimize a new FeFinFET device that can surmount the challenges encountered by conventional FeFinFET and become a viable option for high performance analog and circuit applications.

1.4 Thesis Organisation

This thesis is organized into six chapters, each designed to systematically address the research objectives. Every chapter is presented in a self-contained manner for clarity and coherence.

Chapter 1 discusses the limitations of conventional MOSFETs and establishes the motivation for transitioning toward FeFET technology. It begins with an overview of MOSFET scaling challenges and SCEs, followed by strategies proposed in the literature to address these issues through various engineering approaches, including channel, gate engineering and band engineering. The

chapter then introduces the FeFinFET device as a solution to combat the challenges faced by the scaling in conventional FETs, covering its structure, classification, basic operating mechanism, and associated advantages and challenges. Finally, it defines the research objectives and outlines the overall organization of the thesis, emphasizing the significance of the work undertaken.

Chapter 2 provides a detailed description of the proposed device architecture along with the design specifications and material parameters considered for simulation. It then outlines the simulation models employed in this work. To establish the practical viability of the concept, the chapter also presents a step-by-step outline of the possible fabrication process for the proposed device. Further, the chapter focuses on the optimization of the proposed device, beginning with a comparative analysis between the conventional FeFinFET and proposed VS-HOI-FeFinFET. To further refine the device performance, gate stacking with high-k/low-k dielectric combinations is introduced, and various configurations are examined to know their impact on analog and RF characteristics. The role of germanium mole fraction in the strained channel along with geometric dimensions of Fin, thickness of ferroelectric layer and oxide layer are also explored for various analog metrics. Thus, collectively, a comprehensive evaluation establishes the suitability of the proposed VS-HOI-FeFinFET architecture for high performance analog and RF applications.

Chapter 3 presents a device-to-circuit level analysis of proposed VS-FeFinFET, focusing on the impact of interface trap charges (ITCs) on reliability. To mitigate these effects, gate engineering is introduced, leading to the development of hetero-dielectric vertically stacked ferroelectric FinFETs (HD-VS-FeFinFETs). The proposed structure demonstrates enhanced analog behavior, improved linearity, and reduced distortion performance as compared to conventional design, along with showcasing improved reliability under varying ITCs conditions. Furthermore, the application of the HD-VS-FeFinFET in CMOS inverter circuits is also explored, showing its superior noise tolerance, switching characteristics, and overall functional reliability. These results highlight the potential of the proposed architecture with enhanced functionality, reliability, and performance for low-power, distortion-free, and high-performance modern electronics systems.

Chapter 4 provides a detailed device-level and circuit-level analysis of HD-VS-FeFinFET under coupled thermal and ITCs dynamics to capture. Unlike prior studies offering general ITC evaluations, this work isolates the dynamic behavior of ITCs across a wide thermal range, varying

ITCs density and varying charge polarities. Results demonstrate that HD-VS-FeFinFET has better immunity against ITCs with minimun variation at all considered operating temperatures. Further, the study done to analyze the impact of ITCs density and polarity reveals that device performance alters significantly with rising density of ITCs for both PITC(NITC) but this deviation is very much less in HD-VS-FeFinFET in comparison to VS-FeFinFET. The findings also demonstrate that HD-VS-FeFinFET exhibits superior thermal stability, reduced sensitivity to ITC density, and enhanced robustness under electrical stress compared to conventional structures. Furthermore, circuit simulations validate its improved immunity to ITCs, confirming its suitability for advanced logic circuits and low-power applications in dynamic operating conditions.

Chapter 5 presents a comprehensive investigation of HfO_2-based ferroelectric devices, integrating material-level, device-level, and circuit-level analyses. At the device level, the impact of different dopants on the transfer characteristics of HD-VS-FeFinFETs is examined, demonstrating dopant-driven modulation of key performance parameters. Density Functional Theory (DFT) simulations are also carried out to explore the structural and electronic properties of undoped and doped HfO_2, identifying suitable dopants and analyzing their influence on band structure and projected density of states. The effect of dopant concentration on ferroelectric HfO_2 is also evaluated to optimize ferroelectric behavior. In addition, self-heating effects (SHE) are analyzed under varying operating conditions to assess their influence on device reliability and electrical characteristics. Finally, CMOS inverter circuits based on the proposed device are also studied with performance metrics such as switching behavior and timing parameters assessed to capture circuit-level implications. Overall, this integrated multi-scale analysis provides valuable insights into the role of material doping, thermal effects, and device optimization for advancing next-generation low-power, high-speed lodic circuit applications.

Chapter 6 offers a consolidated overview of the research carried out in this thesis, highlighting the key findings and conclusions drawn from the study. It further discusses and outlines possible directions for extending and advancing the research in future studies. Thereafter, this chapter discusses the social impact of the research and its potential benefits to society.

Chapter 2

Optimization and Analysis of Si/SiGe Strained Vertically Stacked Heterostructure on Insulator FeFinFET for High Performance Analog and RF Applications

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* This chapter discusses the extensive analysis done to optimize the Vertically Stacked Heterostructure on Insulator Ferroelectric based FinFET (VS-HOI-FeFinFET) for achieving high performance analog and RF applications.

* Initially, on comparison with baseline FeFinFET, VS-HOI-FeFinFET is found to show remarkable improvements in terms of various measured parameters such as 97.84% reduction in leakage current and 35.98% increment in drain current which consequently results the switching ratio to increase around 61 times along with substantial improvement in threshold voltage and subthreshold swing.

* Further, four multi-material gate stack configurations (C1–C4) are incorporated and observed with the sequential enhancement in static and analog performance — upto 5 times improvement in switching ratio, 41% reduction in DIBL, and 58% better quality factor for C4 over C1 configuration along with achieving remarkable improvements in early voltage, intrinsic gain, device efficiency, output resistance, and conductance, highlighting suitability for analog circuit applications.

* In addition, the optimization with variation in mole fraction, fin geometry and oxide-ferroelectric

layer thickness is proved as critical levers for tuning the electrostatics of the device to achieve lower leakage, improved switching ratio with enhanced gate control, thereby ensuring energy-efficient, reliable, and scalable device design for improved performance.

* RF analysis revealed three times improvement in GFP and GTFP, along with 16% reduction in unity gain cut-off frequency for C4 over C1 configuration, enabling high-frequency amplification with minimized noise distortion.

* Collectively, these optimizations provide a robust design strategy for achieving energy-efficient, reliable, and high-performance VS-HOI-FeFinFET tailored for future high performance analog and RF applications.

2.1 Introduction

Advancement in technology such as logic in memory (LiM) computing, mobile smart devices and Internet of things have led to increasing demand for low power and high-performance electronic devices(ZPPA23). To meet the growing demands, devices under CMOS technology are being aggressively scaled down and are reaching their fundamental limits. At submicron dimensions, short channel effects (SCEs) such as gate leakage current, drain induced barrier lowering (DIBL), and fluctuation of device characteristics due to random channel dopant, start dominating and deteriorates the device performance(Hol16). To overcome these limitations, different device designs and engineering schemes are reported in literature such as Dual Gate, Trigate FinFET, Recessed channel, FeFETs etc (RMZ$^+$24; GKG$^+$24).

Among these structures, FeFinFET is considered as a promising contender for ultimate CMOS device structure because the device has robustness against short channel effects (SCEs) and improved overall transistor performance(ZLX$^+$24). The conductivity at the surface of a semiconductor can be modulated by integrating ferroelectric materials, which provide non-volatile and electrically controllable polarization charges. These polarization charges act as an effective gate field, altering the carrier concentration at the semiconductor interface and thereby tuning its surface conductivity(SV57). The n-channel FeFET was successfully demonstrated at Research laboratory by Shu-Yau We et al. for the first time in Pittsburgh in 1974 with Bismuth Titanate ($Bi_4Ti_3OI_2$) ferroelectric film(AMN$^+$23). The Ferroelectric FinFET represents a paradigm shift in the realm of electronic devices, blending the advantages of FinFET technology with the unique properties of ferroelectric materials(VM23). Traditional FinFETs have long been the backbone of modern semiconductor manufacturing, delivering superior control over electronic channels(MB24). However, the introduction of ferroelectricity introduces an additional dimension, allowing for non-volatile memory capabilities and unprecedented control over the transistor's state(RNP22; YNJ$^+$24). When combined with the advantages of Silicon-on-Insulator (SOI) technology, which involves placing a thin layer of insulating material beneath the transistor channel, the resulting SOI FeFinFET mitigates the adverse effects of parasitic capacitance and reduces the susceptibility to various SCEs(CS23a; HSS$^+$24). This isolation enhances the transistor's electrostatic control, enabling more efficient switching and reducing power consumption which is a critical requirement in the era

of energy-efficient computing(CSB23).

To further improve the performance of SOI FeFinFET and to minimize SCEs, there is need to go beyond silicon channel materials such as SiGe, GaAs, and group III-IV materials(LZC+21a). The performance of Vertically Stacked Ferroelectric based FinFET (VS-FeFinFET) using a compound semiconductor material (SiGe) with a strained-silicon channel system has been analysed in previous work and it is found that VS-FeFinFET shows improved performance and can be further scaled down compared to FeFinFET(VC23). Strained silicon is a form of silicon where the silicon atoms are stretched or compressed out of their natural lattice positions. This is usually achieved by placing a layer of silicon along with another material with a slightly different lattice constant, such as silicon-germanium (SiGe). The mismatch between the lattice constants causes the silicon atoms to either stretch or compress, depending on another material. To develop strain in the channel region in VS-HOI-FeFinFET, a SiGe layer is sandwiched between two silicon layers. Straining the silicon changes the energy band structure, which reduces the effective mass of the charge carriers (electrons and holes). This allows them to move faster, increasing the mobility of the carriers. Higher mobility leads to faster switching speeds in transistors and lower power consumption(FWI+10; DDD+19). On the other hand, unstrained silicon is silicon in its natural state, where the atoms are in their regular, unmodified lattice positions. There is no external stress applied to the silicon crystal structure . In unstrained silicon, the charge carriers (electrons and holes) move at their normal speeds, which is slower compared to strained silicon. While it works well for standard electronic applications, it doesn't provide the performance enhancements that strained silicon does(Cre05). With the development of strained tri-layered channel in the device, its performance is significantly improved as compared to unstrained one. This is attributed mainly to two following phenomenon: energy band shifting and degenerate splitting of electronic states. These two effects collectively improve the carrier's mobility and led significant enhancement in drive current.

Even though the on current is improved with a strained-silicon channel, still another major concern in the continued scaling is the increment of gate direct tunneling current with decreasing gate oxide thickness, thus resulting in enhanced off-state leakage current(ÜUS+24). The most technological solution is the use of high-k dielectric materials. However, there are certain drawbacks of direct deposition of high-k dielectrics on silicon such as maintaining the interface's quality between silicon and high-k dielectric, mobility degradation with threshold voltage instability(BSAP24; HWCF23).

The implementation of the Gate Stack (GS) configuration tackles the problem. GS architecture consists of a thin low-k dielectric layer between the high-k dielectric and silicon(KSC23). Thus, taking all these considerations into account, we propose a Vertically Stacked Heterostructure on Insulator Gate Stacked Ferroelectric based FinFET (VS-HOI-GS-FeFinFET) with strained tri-layered heterostructure channel system. It is formed with the amalgamation of several advanced technologies such as integration of ferroelectric layer in multigate FinFET along with the adaptation of SOI technology. Further strain engineering is incorporated in doing the vertical stacking of strained tri-layered channel forming heterostructure channel system with the help of Si/SiGe. Subsequently gate stack engineering is also employed in the structure with the help of materials of different dielectric constants for gate oxide. Thus, the resulting VS-HOI-GS-FeFinFET is further optimized and analysed in this research work in the subsequent sections to make the device suitable for various high performance Analog and RF applications. This chapter is organized as follows: Section 2.2 includes all the specifications regarding the device structure. The simulation framework mentioning the physical models used and fabrication feasibility for the device are discussed in section 2.3. Section 2.4 provides the results and discussion for the optimization of the device considering various performance parameters. Section 2.5 provides a complete summary of the chapter.

2.2 Device Architecture

Three dimensional structure of VS-HOI-GS-FeFinFET is shown in Figure 2.1(a) and its vertical two-dimensional view slit through the fin of the device is illustrated in Figure 2.1(b). Further Figure 2.1(c) displays the step by step fabrication process flowchart for VS-HOI-GS-FeFinFET. As the starting material SOI wafer is used with a thick buried oxide layer and thick silicon film followed by silicon film thinning for fin. Afterwards stacked SiGe/Si tri-layer were epitaxially grown by reduced-pressure chemical vapor epitaxial deposition. Thereafter, fin patterning is done using the self-aligned quadruple patterning (SAQP) method followed by shallow trench isolation (STI) filling and an optimized STI densification annealing which is performed with a rapid thermal annealing (RTA) at an optimized temperature. The gate dielectric is deposited on the silicon interfacial layer by atomic layer deposition (ALD) followed by ferroelectric layer deposition by chemical vapor deposition (CVD). The drain and source regions are implanted, and the dopants of these regions are

activated using spike annealing followed by chemical mechanical planarization for smoothening the surface. Metal gate is deposited using electron beam evaporation at room temperature on the top of the ferroelectric layer. The source/drain metal contacts are also deposited by electron beam evaporation followed by lift-off process. Thus, the VS-HOI-GS-FeFinFET is formed and continues processing(LZC+21b; AAAea17; CMY20).

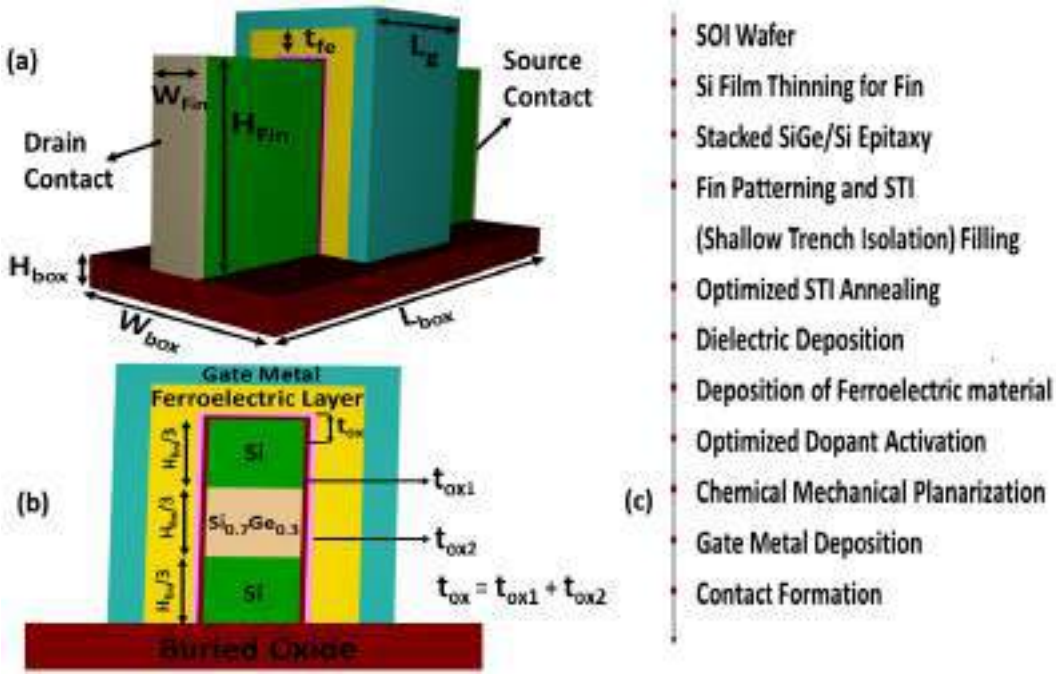

Figure 2.1: (a) 3D schematic view of VS-HOI-GS-FeFinFET (b) Inset of vertical cross-sectional view of VS-HOI-GS-FeFinFET (c) Fabrication process flowchart (VC24a).

Table 2.1: Dielectric Materials

Material and Properties	SiO_2	Al_2O_3	HfO_2
Dielectric Constant	3.9	9	22
Band gap [eV]	9	8.8	5.8
Conduction band offset [eV]	3.5	2.8	1.5

Table 2.2: Gate Stack Configurations

Gate Stack Configuration of VS-HOI-GS-FeFinFET	Gate Stack Materials
C1	SiO_2+Al_2O_3
C2	SiO_2+HfO_2
C3	Al_2O_3
C4	Al_2O_3+HfO_2

Table 2.3: Device parameters

Device parameters	VS-HOI-GS-FeFinFET
Gate length (L_g)	20nm
Drain/Source ($L_{d/s}$)	20nm
Channel material	Si-$Si_{0.7}Ge_{0.3}$-Si
Oxide thickness (t_{ox})	1nm
Ferroelectric thickness (t_{fe})	4nm
Background dielectric constant of Ferroelectric layer	27
Width of fin (W_{Fin})	8nm
Height of fin (H_{Fin})	30nm
Height of box (H_{box})	5nm
Width of box (W_{box})	32nm
Length of box (L_{box})	62nm
Doping concentration of drain/source ($N_{d/s}$) (cm^{-3})	1×10^{20}
Doping concentration of channel (N_{ch}) (cm^{-3})	1×10^{16}
Gate work function (ϕ)	4.53eV

The gate length considered for the device is fixed at 20nm where the gate stack consists of silicon doped hafnium oxide (HfO_2FE) as the ferroelectric material with thickness fixed at 4nm and different combinations of high-k/low-k gate dielectric materials are used as gate oxide material with total physical thickness fixed at 1nm. Table 2.1 displays the different dielectric materials used for the simulations and their properties. Four Gate Stack Configuration C1 to C4 are considered in this study. The combinations taken for gate oxide in different configurations are C1(SiO_2+Al_2O_3), C2(SiO_2+HfO_2), C3(Al_2O_3), and C4(Al_2O_3+HfO_2), as also summarized in Table 2.2. Each configuration involves different combinations of interfacial layers, combinedly making gate oxide in between the ferroelectric layer and the semiconductor. Four different combinations C1 to C4 are taken in such a way that each subsequent combination improves the performance of the device in terms of various analog/RF parameters. The height and width of the fin are taken as 30nm and 8 nm respectively. A tri-layered strained-silicon channel system is formed with the help of SiGe as channel is stacked with silicon germanium sandwiched between two silicon layers as Si-$Si_{0.7}Ge_{0.3}$-Si (where $Si_{0.7}Ge_{0.3}$ represents that the mole fraction of Si and Ge is taken as 0.7 and 0.3 respectively)

with each stacked layer having the same height of 10nm. The doping concentration of source/drain is taken as 1×10^{20} cm^{-3} with donor type and that of channel is 1×10^{16} cm^{-3} with acceptor type with uniform profile. The length of the source/drain regions is fixed at 20nm as shown in in Table 2.3. Besides that, to avoid any poly-depletion effect seen in polysilicon gates, metal gate with work function 4.53 eV is used in this device which is having high thermal stability and is also compatible with CMOS processing(PGP+20a; RCK24). Further the entire heterostructure is built on an insulator SiO_2 box whose length, width and height are kept 62nm, 32nm and 5nm respectively to add the advantages of SOI technology such as improved subthreshold characteristics, minimum parasitic capacitances and suppressed threshold voltage (V_{th}) variations.

2.3 Simulation Framework and Physical Models

All the simulations are carried out by Genius 3D TCAD simulator by Cogenda. The gate to source voltage is varied from 0 to 1 V while drain to source voltage and temperature are fixed at 0.4 V and 300K respectively during the entire simulation. The simulation setup includes the drift-diffusion model level 1 (DDML1) to solve the set of partial differential equations coupled with Poisson's equation as given by Eq. 2.1 and continuity equations to govern the carrier transport phenomena for the electrons and the holes as given by Eq. 2.2 and 2.3 respectively,

$$\nabla.\epsilon\nabla\psi = -q(p - n + N_{\mathrm{D}}{}^{+} - N_{\mathrm{A}}{}^{-}) \tag{2.1}$$

$$\frac{\partial n}{\partial t} = \nabla.(\mu_{\mathrm{n}} n\vec{E}_{\mathrm{n}} + \mu_{\mathrm{n}}\frac{k_{\mathrm{b}}T}{q}\nabla n - (U - G) \tag{2.2}$$

$$\frac{\partial p}{\partial t} = -\nabla.(\mu_{\mathrm{p}} p\vec{E}_{\mathrm{p}} + \mu_{\mathrm{p}}\frac{k_{\mathrm{b}}T}{q}\nabla p - (U - G) \tag{2.3}$$

where ψ is the electrostatic potential of the vacuum level, n and p are the electron and hole concentration, $N_D{}^+$ and $N_A{}^-$ are the ionized impurity concentrations, q is the magnitude of the charge of an electron, E_n and E_p are the efective driving electrical feld for electrons and holes, μ_n

and μ_p are mobilities of electrons and holes, U and G are the recombination and generation rates for both electrons and holes(MC24).

Also Shockley-Read-Hall (SRH) recombination model is used to incorporate generation and recombination of electrons and holes. Further to consider the mobility degradation at silicon to oxide interface due to various factors, Lombardi mobility model is used for silicon which takes into account three components related to carrier mobility such as doping-dependent bulk mobility (μ_b), the mobility degradation due to acoustic phonon scattering in the inversion layer (μ_{ac}) and the mobility degradation due to the surface roughness scattering (μ_{sr}) as given by Eq. 2.4, to collectively give the total mobility (μ_t). Similarly, Philips mobility model is used for SiGe that takes into account the distinct acceptor (a) and donor (d) scattering, carrier-carrier scattering and carrier screening effects (p) as given by Eq. 2.5, where $\mu_{0,n}$ is the total low field electron mobilities, $\mu_{lattice,n}$ is the electron mobilities due to lattice scattering(PGP$^+$20a).

$$\frac{1}{\mu_t} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \tag{2.4}$$

$$\frac{1}{\mu_{0,n}} = \frac{1}{\mu_{lattice,n}} + \frac{1}{\mu_{d+a+p}} \tag{2.5}$$

The density gradient method is also used to consider quantum confinement phenomena along with Fermi-Dirac carrier statistics model. The physics of ferroelectric layer is modeled with time-dependent Landau–Khalatnikov (LK) equation for relating electric field used for the ferroelectric layer (E_{FE}) as a function of polarization (P) as given by Eq. 2.6,

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho(\frac{\partial P}{\partial t}) \tag{2.6}$$

where α, β, and γ are the static Landau material-dependent coefficients taken as -1.23×10^{11} cm/F, 3.28×10^{20} cm^5/FC^2, 0.0 cm^9/FC^4 while g is dipole interaction coefficient and ρ is viscosity coefficient(PGP$^+$20a). The background dielectric constant of ferroelectric layer is fixed at 27. Also, the polarization parameters are adjusted as coercive field (E_c) equals to 1.29 MV/cm, and remnant polarization (P_r) equals to 13.69 μC/cm^2(PGP$^+$20a). Further Lucent model is used

to capture the high-field mobility effects along with hot carrier models to consider the effect of hot carriers. The various device parameters considered for the simulation are displayed in Table 2.1 and Table 2.3.

2.4 Result & Discussion

2.4.1 Performance comparison between FeFinFET and VS-HOI-FeFinFET

In this section, the performance of FeFinFET and VS-HOI-FeFinFET is compared for different parameters. Instead of gate oxide stack, only single layer of oxide is used as gate oxide for this comparison. Firstly, the VS-HOI-FeFinFET is compared with FeFinFET with SiO_2 as gate oxide and then simultaneously the performance of VS-HOI-FeFinFET is analysed with Al_2O_3 as gate oxide instead of SiO_2.

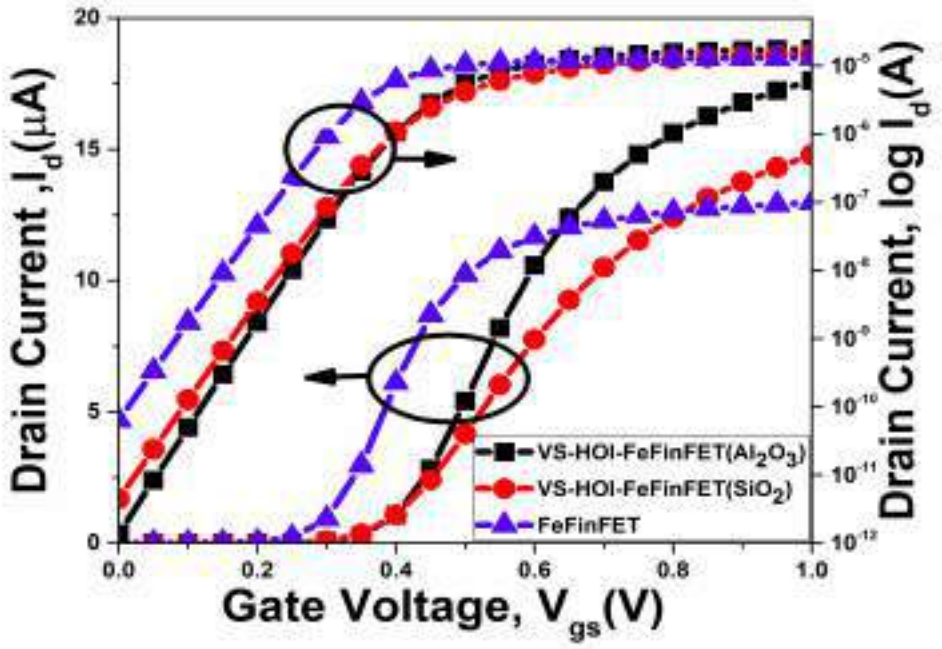

Figure 2.2: Variation in transfer characteristic of VS-HOI-FeFinFET and FeFinFET in linear and log scale. (VC24a).

The I_d-V_{gs} characteristics of all configurations are depicted in Figure 2.2, which shows significant increment in ON current (I_{on}) for VS-HOI-FeFinFET(Al_2O_3) as compared to VS-HOI-FeFinFET(SiO_2) and FeFinFET(SiO_2). Further, Figure 2.3 shows 97.84% reduction in leakage current in VS-HOI-FeFinFET(Al_2O_3) due to enhanced control over the channel and reduced tun-

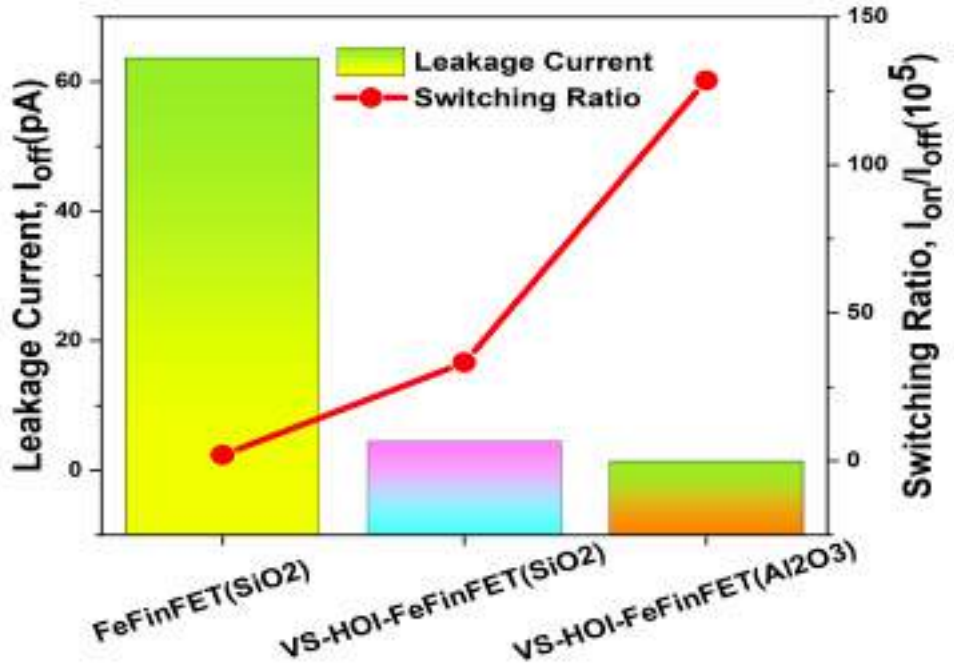

Figure 2.3: Comparison of Switching Ratio and Leakage Current. (VC24a).

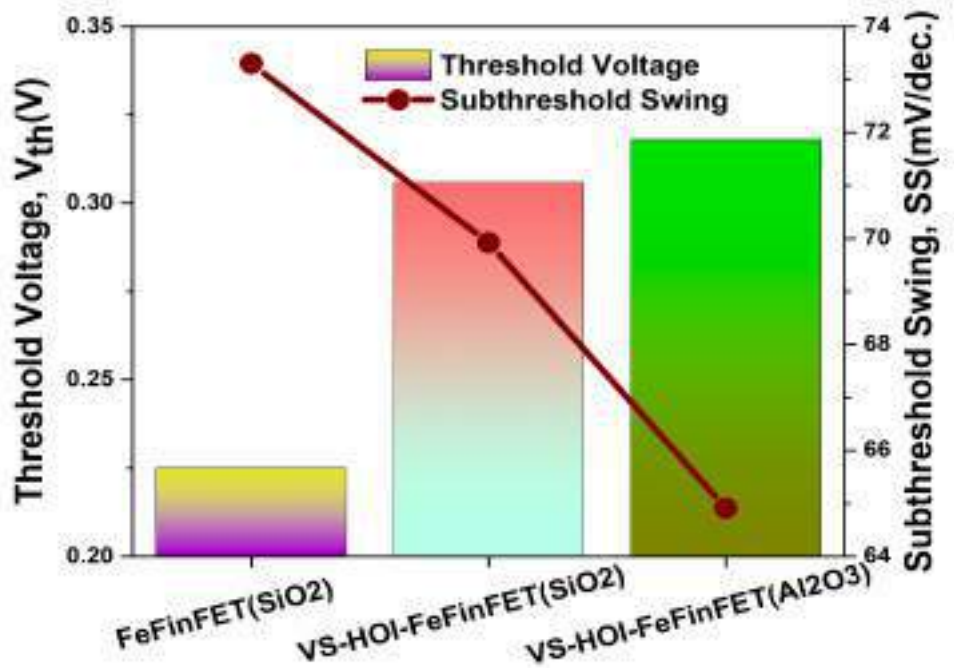

Figure 2.4: Comparison of Threshold Voltage and Subthreshold Swing. (VC24a).

nelling current which results in 61.74 times increment in its switching ratio as compared to FeFinFET. The improved controllability over the channel in VS-HOI-FeFinFETs(Al_2O_3) arises primarily from the high-k Al_2O_3 gate dielectric and the Si/SiGe strained channel. The high dielectric constant of Al_2O_3 enhances gate-to-channel capacitive coupling, allowing more effective modulation of the channel potential. Simultaneously, the strained Si/SiGe channel increases carrier mobility, enabling a stronger and more responsive channel conduction. Together, these factors improve gate

control and result in sharper subthreshold characteristics. This also led to improved performance in terms of threshold voltage and subthreshold swing for VS-HOI-FeFinFET(Al_2O_3) with increment by 41.33% and decrement by 11.45% respectively as compared to FeFinFET as depicted in Figure 2.4. Figure of merit (FOM) of VS-HOI-FeFinFET(Al_2O_3) over FeFinFET(SiO_2) is also shown in Table 2.4, which is a performance metric and used to characterize the performance of a device relative to its alternatives. Here, it gives the improvement in the performance of VS-HOI-FeFinFET(Al_2O_3) over FeFinFET(SiO_2) in terms of various analysed parameters. On account of these advantages of VS-HOI-FeFinFET over FeFinFET, the impact of various gate dielectric materials in gate oxide stack configuration for VS-HOI-FeFinFET is analysed for static, analog and RF performance in the next section.

Table 2.4: Performance Comparison between FeFinFET and VS-HOI-FeFinFET

Parameter	FeFinFET(SiO_2)	VS-HOI-FeFinFET(SiO_2)	VS-HOI-FeFinFET(Al_2O_3)	Figure of Merit (FOM)
I_{on} (A)	1.29×10^{-5}	1.47×10^{-5}	1.76×10^{-5}	35.98%
I_{off} (A)	6.36×10^{-11}	4.44×10^{-12}	1.37×10^{-12}	97.84%
I_{on}/I_{off}	$2.03\times10^{+5}$	$3.32\times10^{+6}$	$1.28\times10^{+7}$	63.12 times
$V_{th}(V)$	0.22	0.30	0.31	41.33%
$SS(mV/dec.)$	73.30	69.92	64.91	11.44%

2.4.2 Gate Stack Optimization for Static and Analog Performance

In this section, various vital static and analog parameters are examined to optimize the gate stack with different dielectric materials to further improve the performance of VS-HOI-GS-FeFinFET over VS-HOI-FeFinFET(Al_2O_3) which showed best performance for single oxide layer as discussed in section 2.4.1. Four Gate Stack configurations taken for gate oxide are C1(SiO_2+Al_2O_3), C2(SiO_2+HfO_2), C3(Al_2O_3), and C4(Al_2O_3+HfO_2), as also summarized in Table 2.2. Figure 2.5 shows the comparison of I_d-V_{gs} characteristics for different configurations in both linear and log scale. It shows increase in ON current and decrease in leakage current due to improved gate control, when the gate stack configuration changes from C1 to C4. Improved gate control means the gate can more effectively modulate the flow of current through the channel, which is crucial in switching the transistor between the ON and OFF states. High-k materials have a higher dielectric constant

compared to traditional SiO_2 which led to increase in the gate capacitance as related by Eq. 2.7, where k is the dielectric constant of the material, ϵ_0 is the permittivity of free space, A is the area of the gate, and d is the thickness of the dielectric layer(LSCK07).

$$C = \frac{k\epsilon_0 A}{d} \tag{2.7}$$

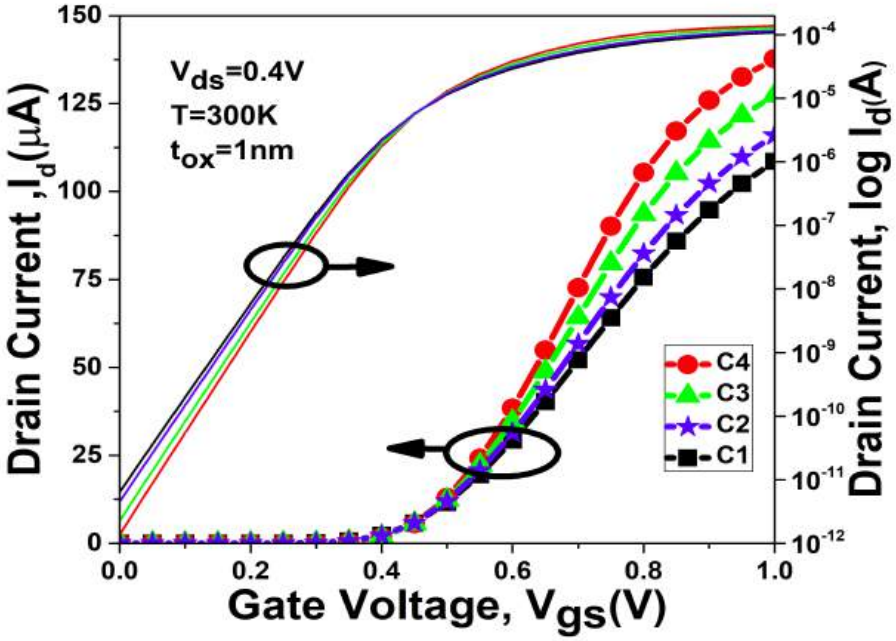

Figure 2.5: Variation in transfer characteristic of VS-HOI-GS-FeFinFET for different configurations in linear and log scale. (VC24a).

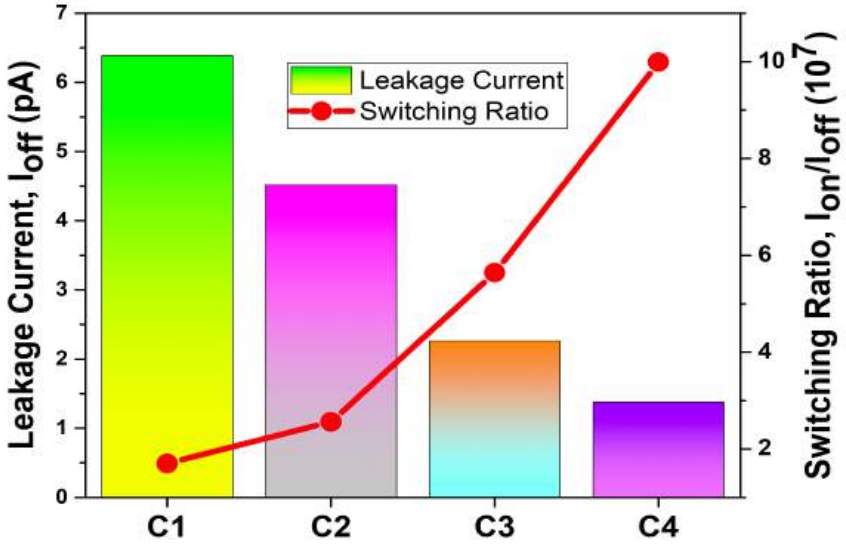

Figure 2.6: Comparison of Leakage Current and Switching Ratio for different configurations. (VC24a).

A higher capacitance means that for a given gate voltage, more charge is induced in the channel which results into stronger electric field. This stronger electric field more effectively controls the number of carriers in the channel. This leads higher carrier density in the channel, thereby increasing the ON-state current. Also, gate leakage current is the undesired current that flows through the gate dielectric when the transistor is in the OFF state. A higher dielectric constant allows for a larger capacitance. This is beneficial because it reduces gate leakage current while maintaining strong gate control over the channel. The reduction in gate leakage current directly lowers the overall leakage current in the transistor as shown in the Figure 2.5.

This results in increase in the switching ratio upto 5.87 times for C4 configuration over C1 configuration as shown in Figure 2.6. Further, Figure 2.7 displays the sequential increase in threshold voltage and improved subthreshold swing as the configuration changes from C1 to C4 thus enhancing the subthreshold device characteristics.

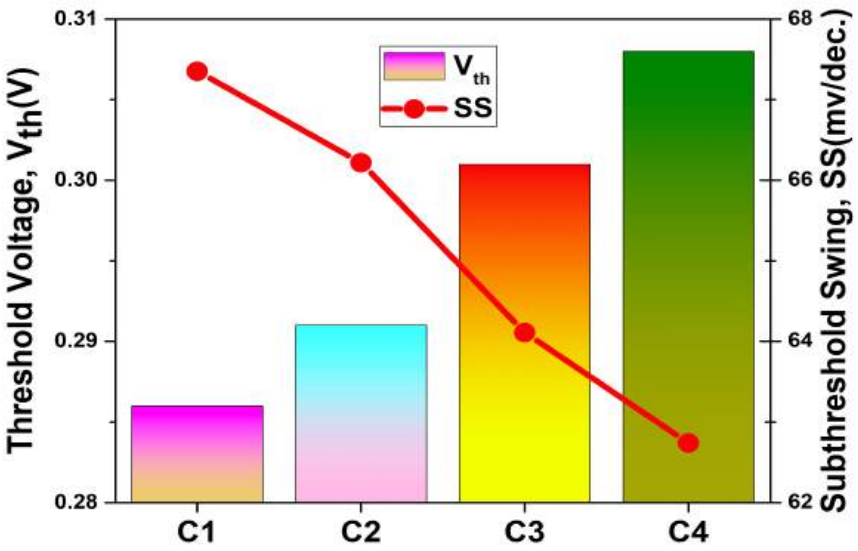

Figure 2.7: Comparison of Threshold Voltage and Subthreshold Swing for different configurations. (VC24a).

Transconductance (g_m), which is given by Eq. 2.8, measures the effectiveness of the FET device in converting variations in the gate-to-source voltage into changes in the drain current(KMR$^+$23). Figure 2.8 confirms that transconductance rises with rise in dielectric constant and shows maximum peak for C4 because of the enhanced drain current thus exhibits better amplification capabilities over

others. Further C4 also displays the improved device efficiency which is also known as Transconductance Generation Factor (TGF)(JR18). It is an important parameter in the design of analog circuits and higher TGF shown by C4 depicts its enhanced efficiency of converting DC parameter (I_d) into AC parameters (g_m) as showcased in Figure 2.8.

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{d}}}{\partial V_{\mathrm{gs}}} \tag{2.8}$$

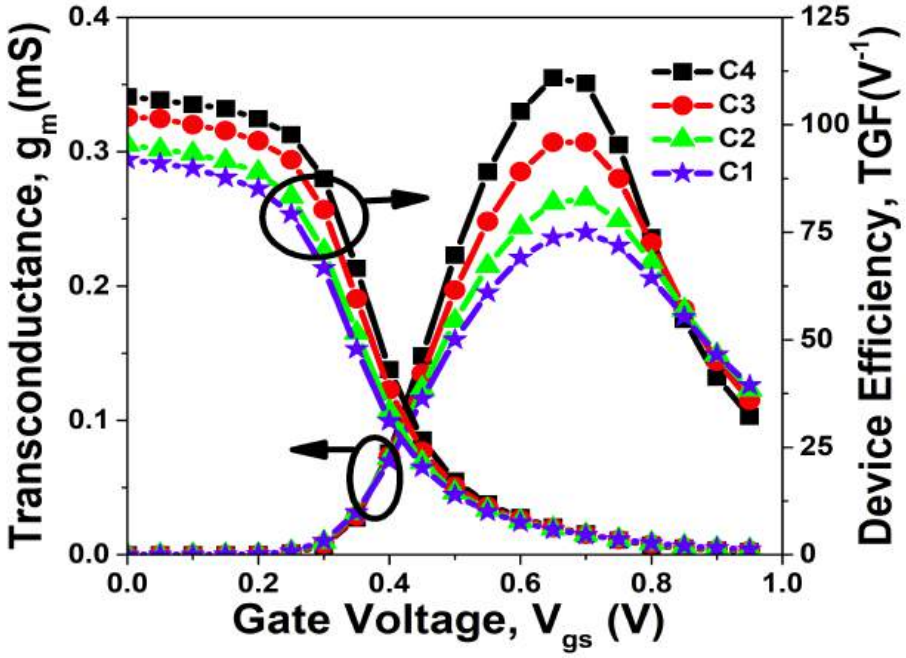

Figure 2.8: Variation in transconductance and device efficiency for different configurations.(VC24a).

Quality factor (QF) is an indicator of the transistor's overall performance, as defined by Eq. 2.9, combining both the efficiency of switching (represented by g_m) and how quickly the device can switch from OFF to ON that is the speed of transition from OFF to ON (represented by SS). In many FETs, there is a trade-off between achieving a high transconductance and a low subthreshold swing. The QF encapsulates this trade-off into a single parameter. Optimizing for a higher QF involves balancing these aspects to design a transistor that is both highly responsive to gate voltage changes and capable of efficient switching, making it a key figure of merit in advanced semiconductor device design. The maximum value of g_m considered for the QF evaluation is obtained at V_{gs} = 0.65V. As shown in Figure 2.9, C4 gives maximum quality factor which is 58.98% increment over C1. This improvement in the QF value with increasing dielectric constant is due to the enhanced

transconductance and reduced subthreshold swing for C4. The DIBL is another vital subthreshold performance metric and minimum DIBL values are preferred for optimum device performance in advanced technology nodes thus Figure 2.9 successfully depicts C4 a better configuration with smaller DIBL over other structures.

$$QF = \frac{g_{\mathrm{m}}}{SS} \tag{2.9}$$

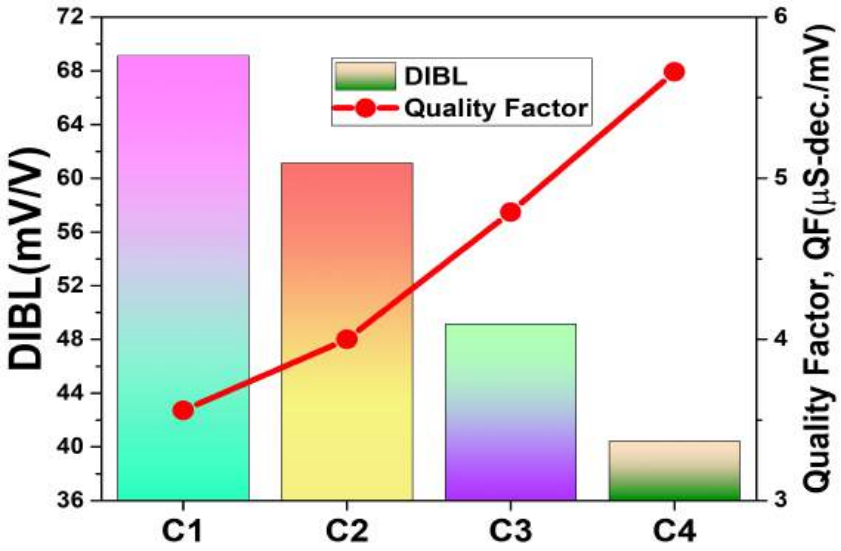

Figure 2.9: Comparison of DIBL and Quality factor for different configurations.(VC24a).

The potential contours of all the four configurations considered for VS-HOI-GS-FeFinFET are displayed in Figure 2.10(a). Further, the potential profile for silicon and SiGe is also presented in Figure 2.10(b) and Figure 2.10(c) which shows the variation of electric potential along the channel for all configurations. It shows that higher electric potential is acquired at the drain end as compared to the source end for all the four configurations. It also shows the improvement in potential significantly in the channel region for C4 configuration as compared to its counterparts due to the ability of high-k dielectrics in the gate oxide to improve the electrostatic control over the channel and the effect is more prominent in the strained layers of SiGe in the middle of channel due to higher carrier mobility and narrower bandgap in SiGe as compared to silicon material. Subsequently, there is decrease in potential in C4 configuration from channel-drain junction towards drain side as compared to other configurations. This is due to the reduction in DIBL in the C4

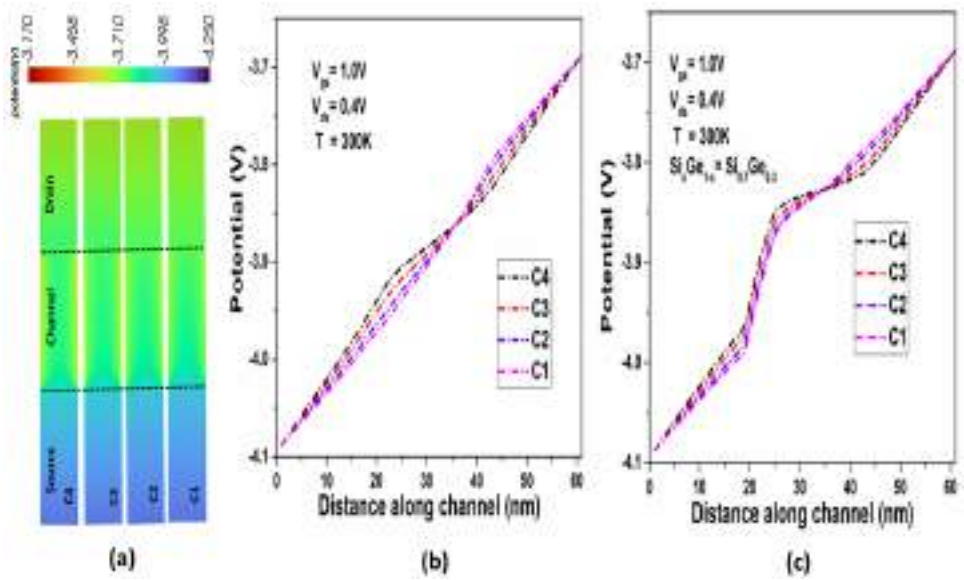

Figure 2.10: (a) Potential contour of all the four configurations (b) Potential profile variation in silicon with distance along the channel (c) Potential profile variation in SiGe with distance along the channel(VC24a).

configuration, that reduces the flattening of the potential profile, resulting in a steeper potential drop between the channel-drain junction and the drain terminal. Thus, this configuration leads to better switching characteristics, making the device more efficient and reliable, particularly in low-power and high-speed applications(KAD20).

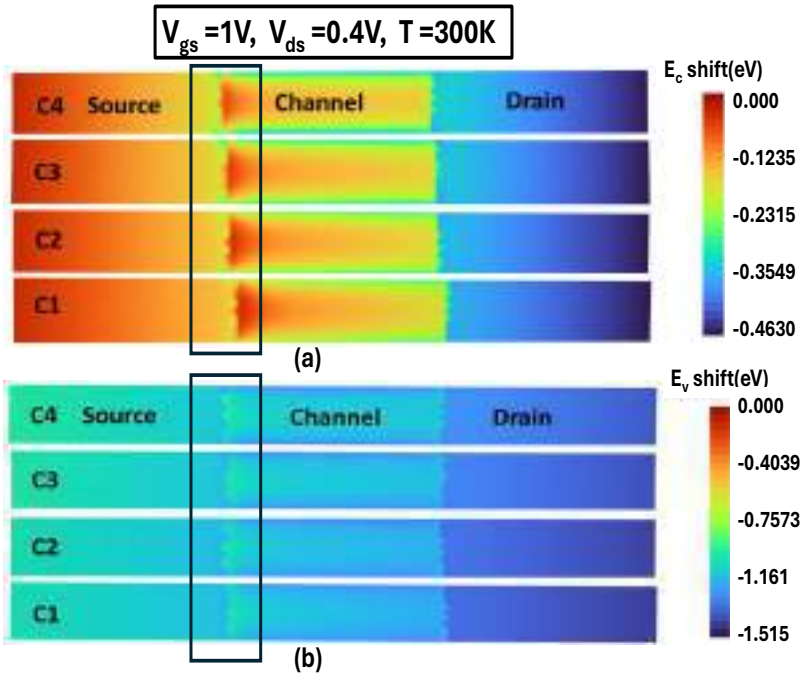

Figure 2.11: Contour of band energy shift for (a) Conduction band (b) Valence band for all the four configurations(VC24a).

Further, Figure 2.11(a) and Figure 2.11(b) respectively shows the contour plot of shift in conduction band energy and valence band energy for all the configurations considered at V_{gs}=1V, V_{ds}=0.4V and T=300K. Due to the shift, the conduction band of C4 configuration is lower than the other configurations across the channel, which reveals the improved conductivity with more band bending, and enhanced band to band tunnelling rate of the carriers from valence band to conduction band for C4 configuration.

Understanding and controlling the output conductance is crucial in optimizing the performance of the device, especially in applications where precise control of the transistor behaviour is necessary. Figure 2.12 displays a combined plot showing variation in drain current and output conductance as a function of V_{ds} at constant V_{gs}=0.4V. Initially, g_d is large while device is operating in linear region but it keeps on decaying with increase in drain to source voltage. In the saturation region, g_d maintains almost constant value. Also, due to improved gate controllability and suppressed SCEs, g_d is minimum for C4 configuration when compared to other counterparts.

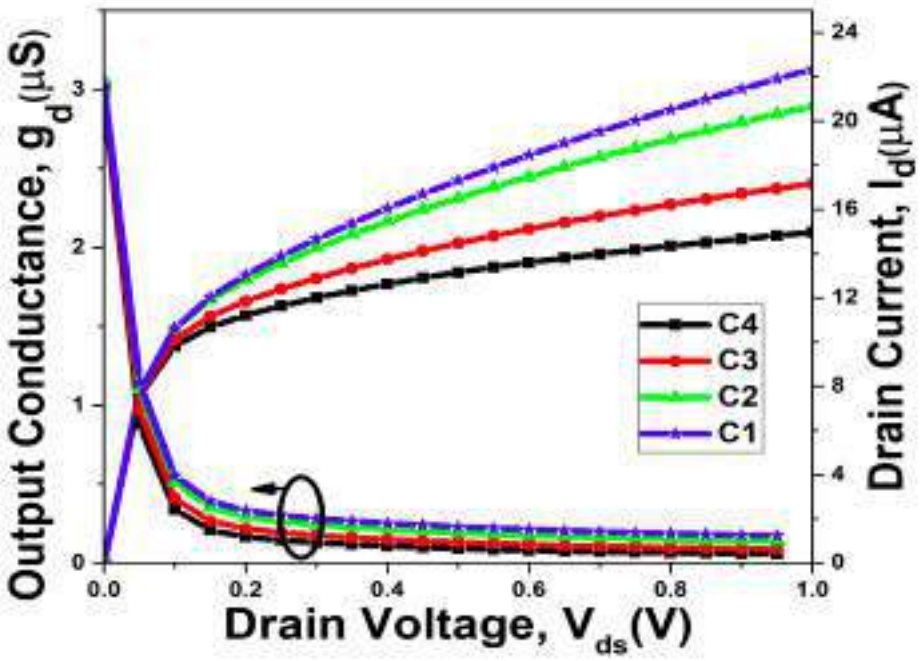

Figure 2.12: Variation in output characteristic and output conductance for different VS-HOI-GS-FeFinFET configurations (VC24a).

Also, channel length modulation (CLM) is a phenomenon that occurs when the effective channel length of a FET device changes with variations in the drain voltage, especially in short-channel devices. This effect causes the I_d to vary with the V_{ds}, even when the V_{gs} is constant, which leads to an increase in the output conductance (g_d). When g_d is low, it means that the drain

current is less sensitive to changes in the drain voltage. This indicates that the effective channel length is not significantly modulated by the drain voltage, implying reduced channel length modulation. Reduced CLM helps in stabilizing the current output, ensuring that the FET device can provide a more constant current, which is essential for certain applications such as constant current sources(PMC22). Thus, lower g_d ensures reduced channel length modulation which is useful for driving constant current source applications.

Intrinsic gain and early voltage are evaluated using Eq. 2.10 and Eq. 2.11 respectively, and they must be as high as possible for enhanced analog performance of the device(PMC22). Figure 2.13 shows the variation of Intrinsic gain and early voltage against gate to source voltage for all the configurations. The maximum value of early voltage and highest peak of intrinsic gain is achieved for C4 configuration thus making it suitable for high-speed analog circuits, where both amplification efficiency and stability are critical(TN17).

$$A_{\mathrm{v}} = \frac{g_{\mathrm{m}}}{g_{\mathrm{d}}} \tag{2.10}$$

$$V_{\mathrm{EA}} = \frac{I_{\mathrm{d}}}{g_{\mathrm{d}}} \tag{2.11}$$

Output resistance (R_{out}) is a measure of how much a device's output voltage changes in response to variations in the load resistance. In electronic circuits, it plays a vital role in maintaining signal integrity and stability. High output resistance ensures better signal fidelity by minimizing voltage variations in response to changes in load resistance(Nar18). The variation in R_{out} for different configurations is displayed in Figure 2.14. Compared to the C1 configuration, the C4 configuration acquires higher R_{out} because channel-length modulation is strongly suppressed in it due to better gate electrostatic control, which reduces the dependence of drain current on V_{ds}. In the C4 configuration, optimized gate stack and channel engineering lead to lower DIBL and weaker short-channel effects as compared to C1. This results in a reduced slope of the I_d-V_{ds} curve in saturation, giving a much higher R_{out} for C4 configuration.

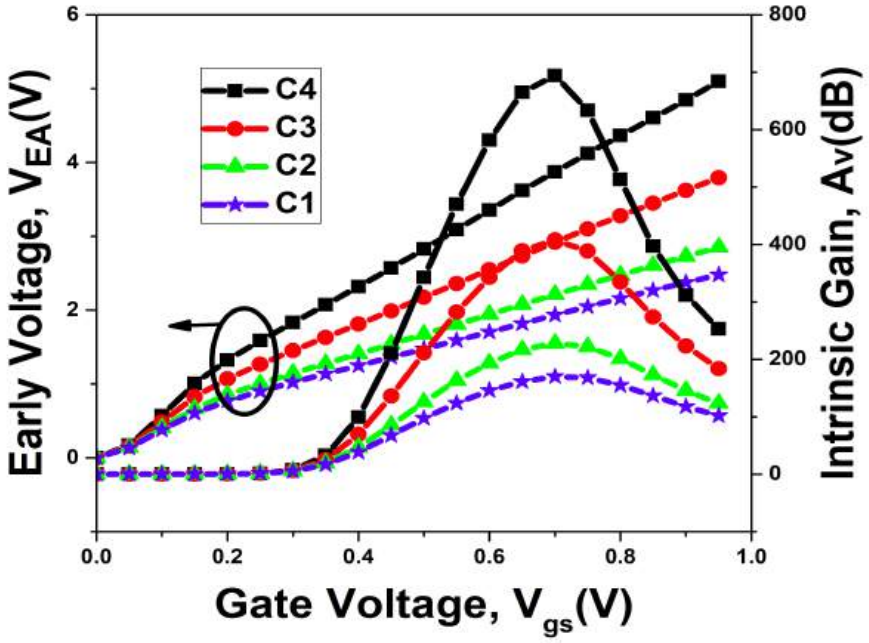

Figure 2.13: Variation in early voltage and early voltage for different VS-HOI-GS-FeFinFET configurations (VC24a).

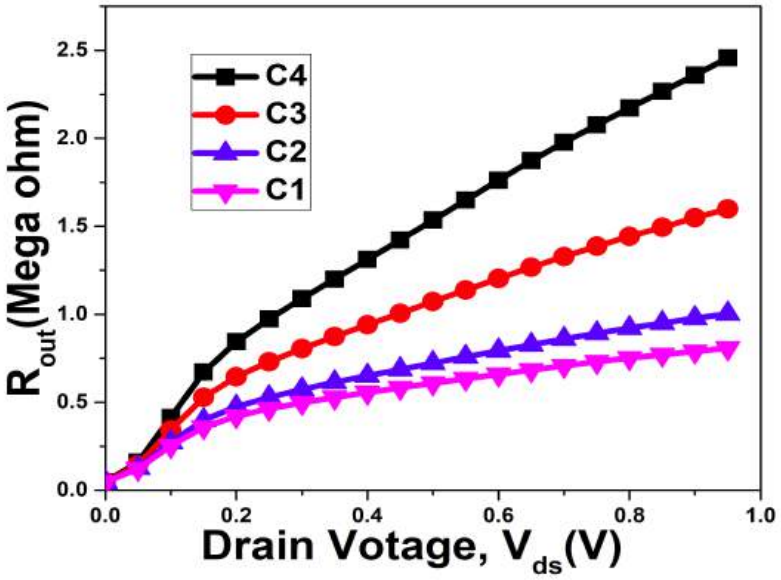

Figure 2.14: Variation in output resistance for different VS-HOI-GS-FeFinFET configurations (VC24a).

2.4.3 Performance optimization for variation in mole fraction of the channel material

Compound materials are defined with mole fraction (x) that depicts the amount of composition present in the mixture. It influences the properties of the channel material and performance of the

device, thus for an optimized device response, its impact needs to be analyzed. As C4 configuration has given the most improved performance out of four considered configurations in previous section, it is considered for the analysis in this section. Figure 2.15 displays the impact of germanium mole fraction in the form of turn on characteristics of VS-HOI-GS-FeFinFET by varying the Ge-mole fraction from 0.1 to 0.9.

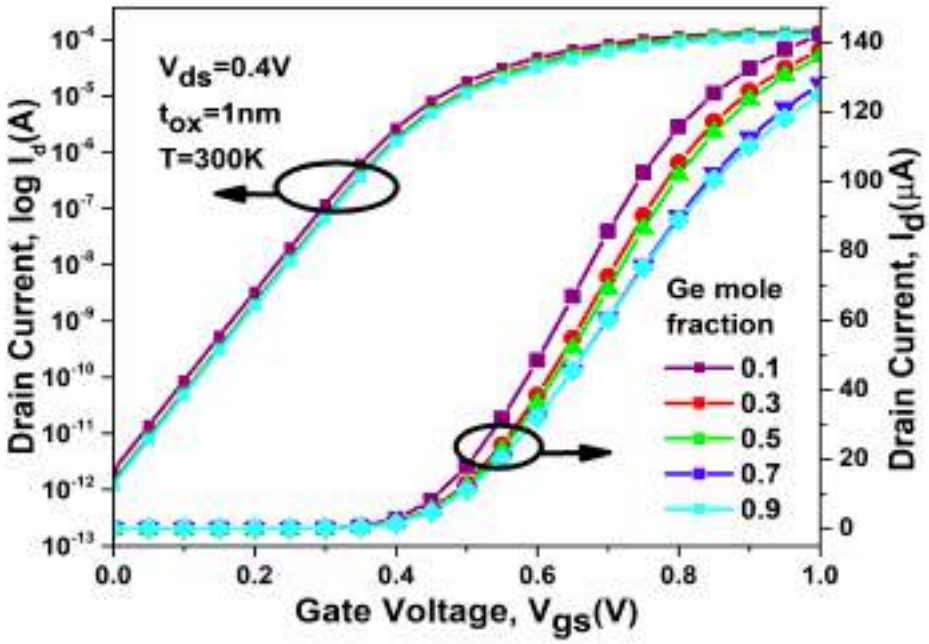

Figure 2.15: Turn on characteristics of VS-HOI-GS-FeFinFET for different Ge mole fraction in channel (VC24a).

It is apparent from the Figure 2.16 that as we increase the mole fraction, I_{on} starts decreasing but there is reduction in leakage current (I_{off}) which decreases from 2.20 pA at x=0.1 to 1.22 pA at x=0.9 that amounts to total decrement by 44.8%. On the other hand, switching ratio for the device is increased from 6.46×10^7 at x=0.1 to 10.3×10^7 at x=0.9 implies enhancement by 58.9%. It also shows the variation of peak transconductance with mole fraction which show better performance with 376 μS at low value of x=0.1 as compared to 298 μS at high value of x=0.9 for lower V_{gs}. But as the gate voltage is increasing, the g_m increases for large value of mole fraction as depicted in Figure 2.17, indicating that the device can be optimized for variable mole fraction as per the design and application's requirements with balancing the trade offs between different performance metrics.

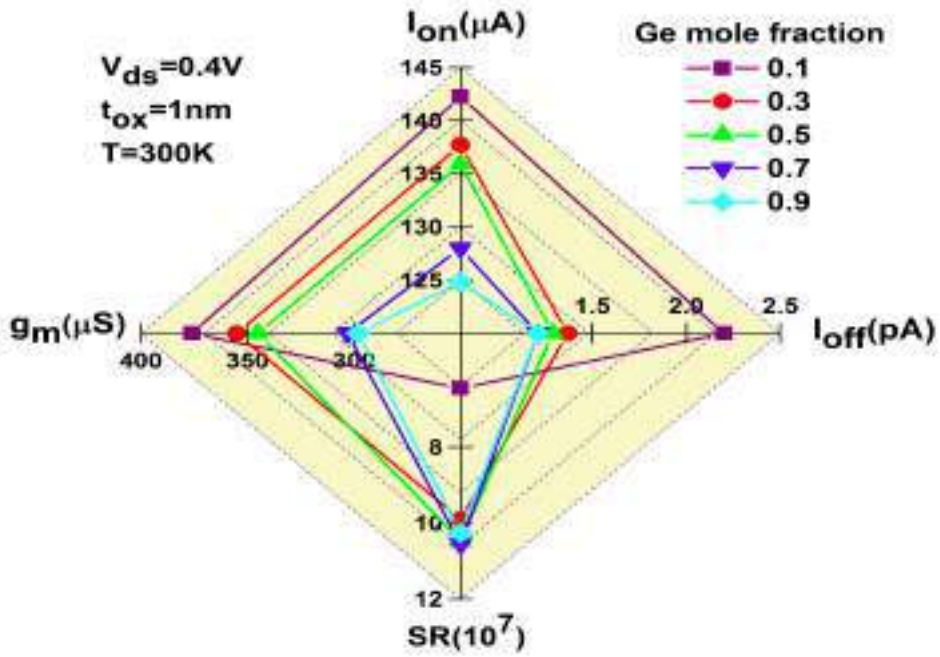

Figure 2.16: Variation in I_{on}, I_{off}, Switching Ratio (SR), transconductance (g_m) of VS-HOI-GS-FeFinFET for different Ge mole fraction (VC24a).

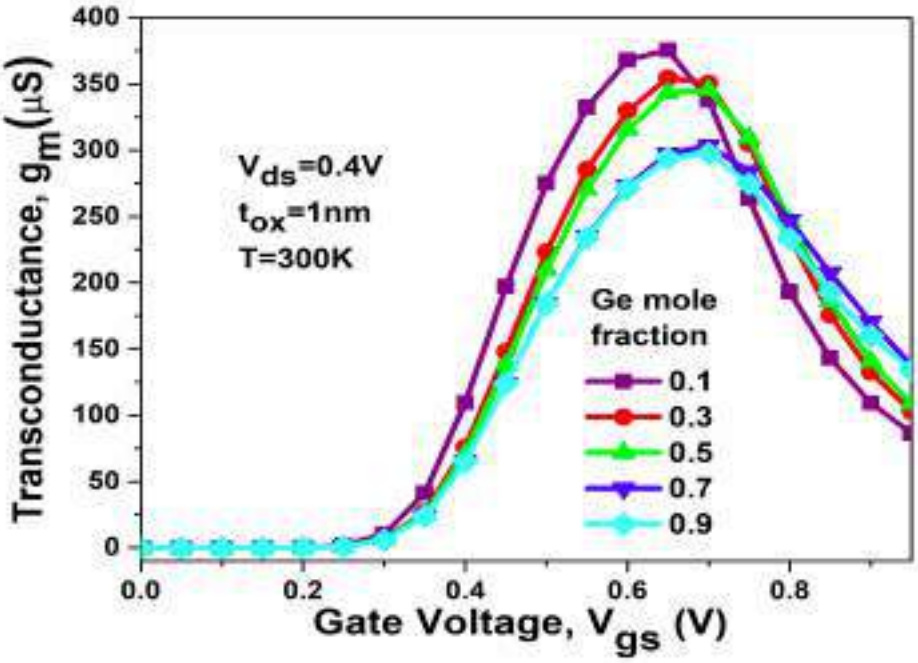

Figure 2.17: Variation in transconductance of VS-HOI-GS-FeFinFET with gate voltage for different Ge mole fraction (VC24a).

2.4.4 Performance optimization for variation in height and width of the Fin

Performance optimization of a FeFinFET with respect to variations in the height (H_{Fin}) and width (W_{Fin}) of the fin is a crucial aspect of device design. These geometrical parameters significantly

influence the electrical characteristics of the FeFinFET, such as threshold voltage (V_{th}), leakage current (I_{off}), switching ratio etc., thus needs to be optimized for improving the performance of the device. C4 configuration is considered for the analysis in this section. Figure 2.18 displays the variation in drain current with variation in gate voltage for different heights of the fin of VS-HOI-GS-FeFinFET. It is visible from the figure that the variation in transfer characteristics of VS-HOI-GS-FeFinFET is very less with variation in H_{Fin}. Several reasons are responsible for this such as, although H_{Fin} influences the effective channel area (thus affecting current-carrying capability of the device), it doesn't impact gate control as much as the width. The gate's ability to control the channel is more sensitive to lateral dimensions (W_{Fin}) rather than vertical dimension(KHS$^+$20). Also, the behavior of the ferroelectric material is sensitive to the electric field, which is influenced more by the gate-channel coupling. Since the coupling is strongly affected with changes in W_{Fin} in comparison to changes in H_{Fin}, the ferroelectric behavior is more affected by width variations. Therefore, H_{Fin} doesn't influence the gate control as strongly as fin width, leading to a smaller overall impact on device performance when it is varied. It clearly shows that as height is reducing from 39nm to 30nm, there is decrement in leakage current from 1.86 pA to 1.38 pA which is 25.8% reduction in I_{off}. It leads to increase in switching ratio from 9.47×10^7 to 9.98×10^7 and minimal increase in V_{th} from 0.30V to 0.31V due to better electrostatic control of gate over the carriers in the channel with decreasing H_{Fin} from 39nm to 30nm.

Figure 2.19 shows the contour plot of potential for VS-HOI-GS-FeFinFET at various fin heights such as (a) H_{Fin}=30nm (b) H_{Fin}=33nm (c) H_{Fin}=36nm and (d) H_{Fin}=39nm, at V_{gs}=1V, V_{ds}=0.4V and T=300K. A reduction in fin height brings the entire fin closer to the gate, allowing the gate to exert stronger electrostatic control over the channel. This results in higher electric potential gradients near the top surface of the fin, with a more uniform and tightly controlled potential distribution across the channel, particularly near the source and drain regions, as visible in Figure 2.19. Also, lowering the fin height also reduces the vertical distance that the gate potential must cover to control the channel. This leads to a more uniform potential drop from the gate towards the bottom of the fin as shown in the contour plot for H_{Fin}=30nm. Figure 2.19 also shows that higher electric potential is acquired at the drain end as compared to the source end which leads to an increased drain-source voltage and results in a stronger electric field in the channel. Thus, it makes the device to work with improved current, faster switching, and better on-state performance.

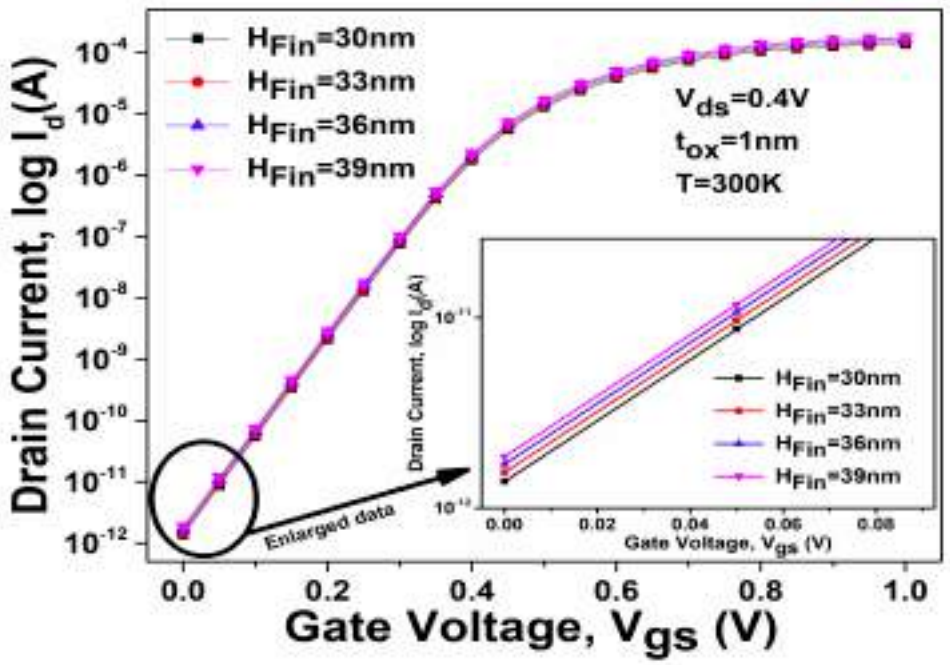

Figure 2.18: Variation in drain current with variation in gate voltage for different height of the Fin of VS-HOI-GS-FeFinFET with fixed width of Fin at 8nm (VC24a).

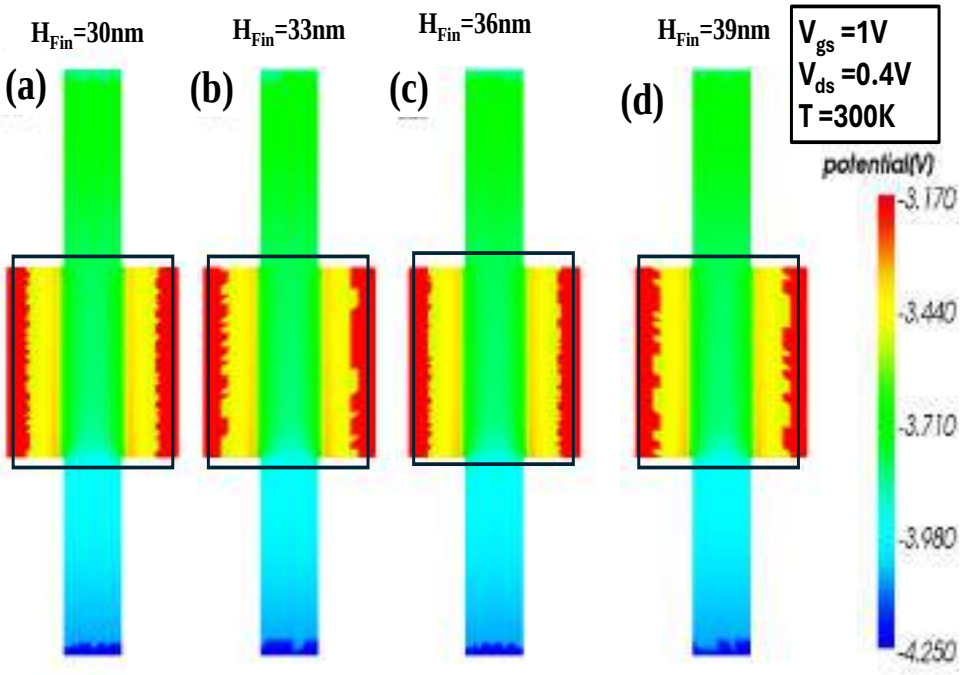

Figure 2.19: The contour plot of potential for (a) H_{Fin}=30nm (b) H_{Fin}=33nm (c) H_{Fin}=36 (d) H_{Fin}=39nm for VS-HOI-GS-FeFinFET with W_{Fin} fixed at 8nm.(VC24a).

Figure 2.20 displays the variation in drain current with variation in gate voltage for different width of the Fin of VS-HOI-GS-FeFinFET. It shows that as width is reducing from 14nm to 8nm, there is decrement in I_{off} from 1.64×10^{-10} A to 1.38×10^{-12} A, thus led to 99.15% reduction in leakage current. This also ensures substantial improvement in switching speed of the device with

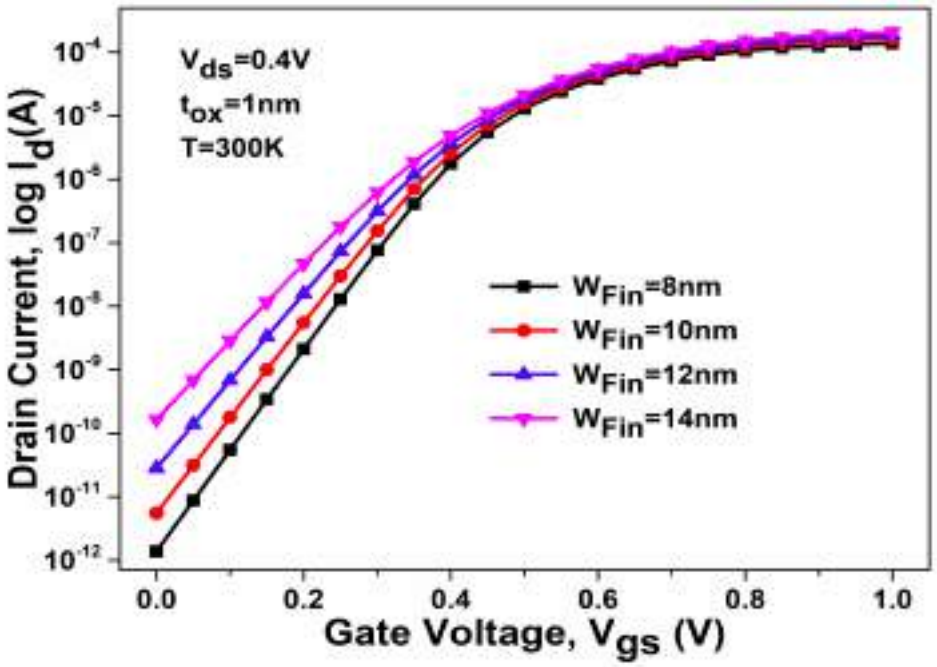

Figure 2.20: Variation in drain current with variation in gate voltage for different width of the Fin of VS-HOI-GS-FeFinFET with fixed height of Fin at 30nm (VC24a).

improvement in switching ratio from 1.26×10^{6} to 9.98×10^{7} and increment in V_{th} from 0.23V to 0.31V as the width of fin is decreased from 14nm to 8nm. Thus, combinedly, it can be summarized that the width and height of the fin as 8nm and 30nm respectively give the most improved performance for VS-HOI-GS-FeFinFET.

2.4.5 Impact of variation in ferroelectric layer on the device performance and its interdependance on the geometric variations of Fin and oxide layer

The performance of ferroelectric based devices is significantly influenced by the thickness of the ferroelectric layer. In a FeFinFET structure, the ferroelectric layer's behavior is intertwined with several key geometric parameters like fin height, fin width, and oxide thickness. In this section, a brief analysis has been done to understand the dependence of ferroelectric layer on the variations in geometric parameters of the fin and oxide layer. C4 configuration is considered for the analysis in this section. Figure 2.21 shows the variation in transfer characteristics and subthreshold swing of VS-HOI-GS-FeFinFET with the variation in thickness of ferroelectric layer. It shows the improvement in subthreshold characteristics like reduction in I_{off} from 2.47×10^{-12} A to 3.39×10^{-14} A, improvement in SS from 63.97 mV/dec. to 55.1 mV/dec., and enhancement in V_{th} from 0.3

V to 0.36 V as t_{fe} is increased from 2nm to 14nm. This happens due to improved electrical field coupling between gate and channel with enhanced polarization on increasing t_{fe}. This improves the transition between the off and on states, ensuring a smoother turn-on behavior which is important in minimizing power loss and ensuring the device functions properly in low-power or high-reliability environments(SBB21).

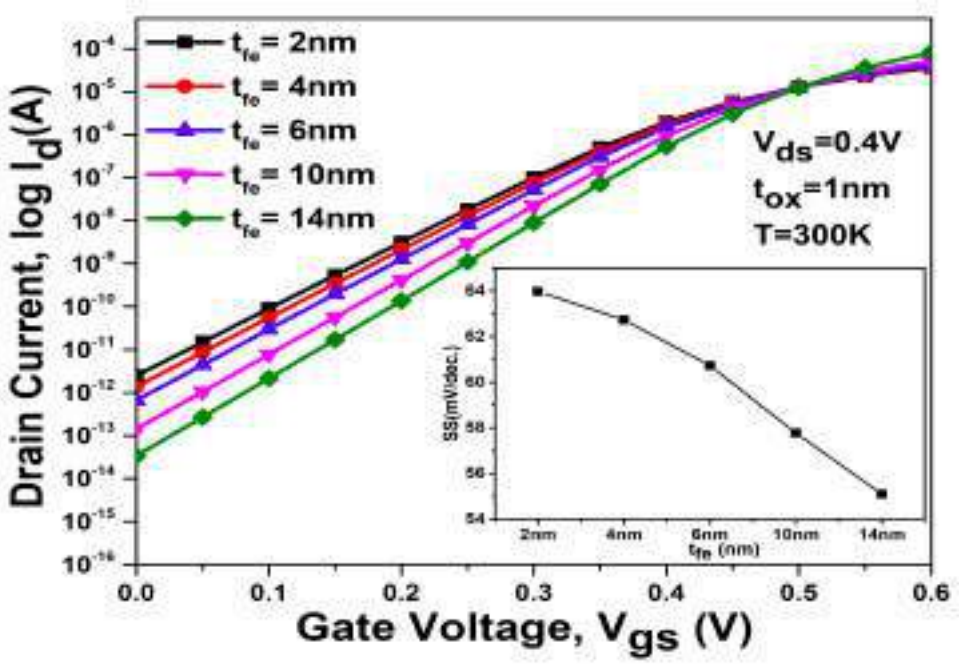

Figure 2.21: Variation in transfer characteristics and subthreshold swing of VS-HOI-GS-FeFinFET for different ferroelectric thickness at fixed height, width and oxide thickness (VC24a).

Further, Figure 2.22 and Figure 2.23 respectively shows the interdependent effect of variation in ferroelectric layer thickness with variation in fin height and fin width. The minimum effect of geometric variation on t_{fe} is displayed by the variation in H_{Fin} as shown in Figure 2.22 while the variation in W_{Fin} shows significant effect on t_{fe} as shown in Figure 2.23. A change in W_{Fin} alters the gate-to-channel capacitance and electrostatic distribution, which directly influences the polarization behavior of the ferroelectric layer thus causing noticeable shifts in I_d-V_{gs} curve unlike H_{Fin}, whose impact remains minimal. The most improved performance is achieved at H_{Fin}=30nm, W_{Fin}=8nm, and t_{fe}=6nm with reduced leakage current and improved switching subthreshold characteristics based on several geometric variations of fin and oxide layer. Figure 2.23 also shows the variation in the transfer characteristics of the device for rising gate voltage (Forward Sweep) and falling gate voltage (Reverse Sweep) with t_{fe}=6nm. It is seen that hysteresis loop is formed be-

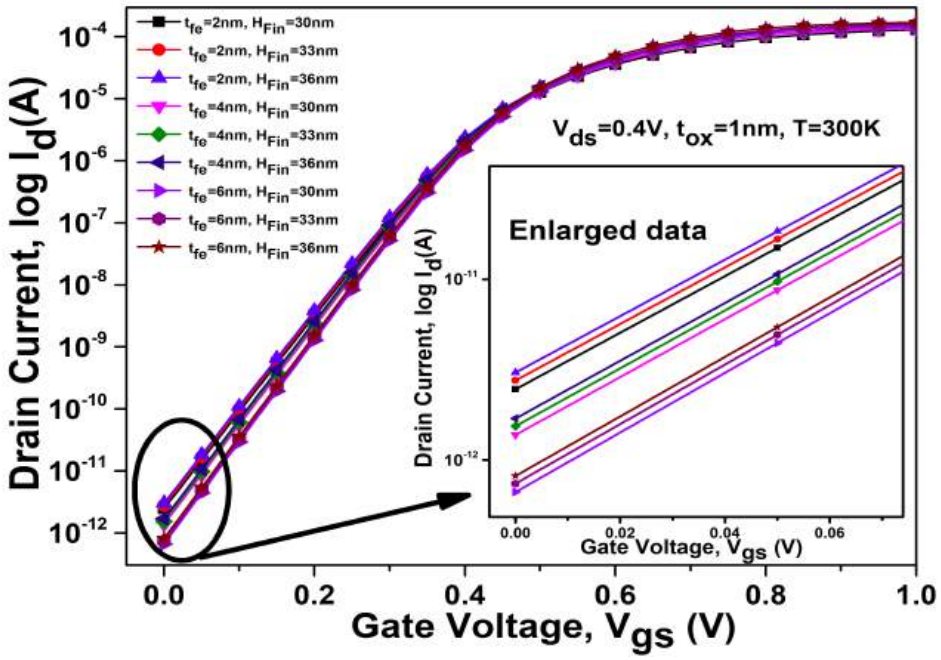

Figure 2.22: Variation in drain current with variation in gate voltage for different ferroelectric thickness and height of the fin in VS-HOI-GS-FeFinFET at fixed width and oxide thickness (VC24a).

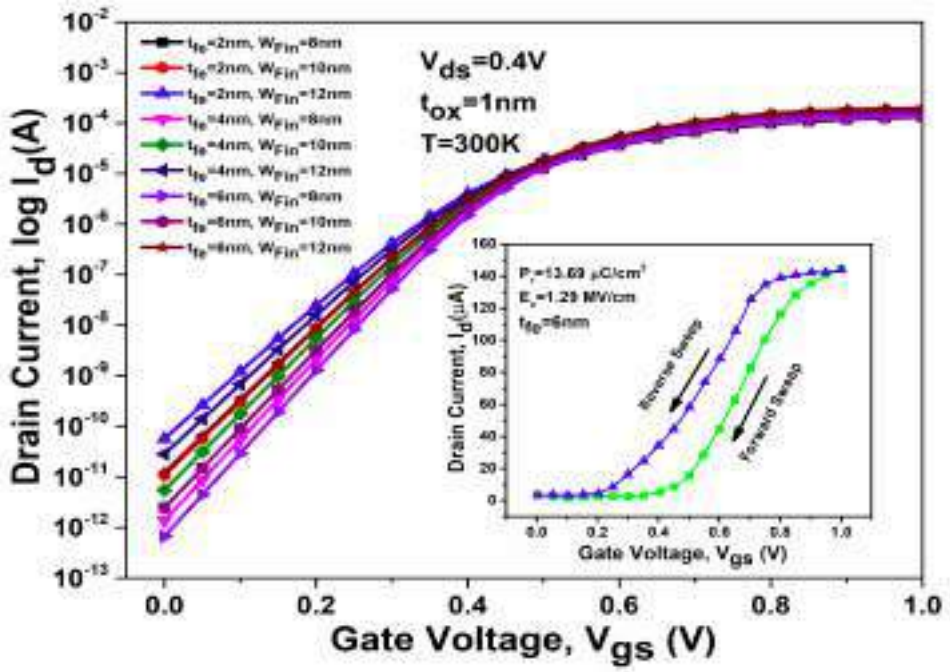

Figure 2.23: Variation in drain current with variation in gate voltage for different ferroelectric thickness and width of the fin in VS-HOI-GS-FeFinFET at fixed height and oxide thickness (VC24a).

tween the forward sweep and reverse sweep, which arises due to bistable polarization states of the ferroelectric material.

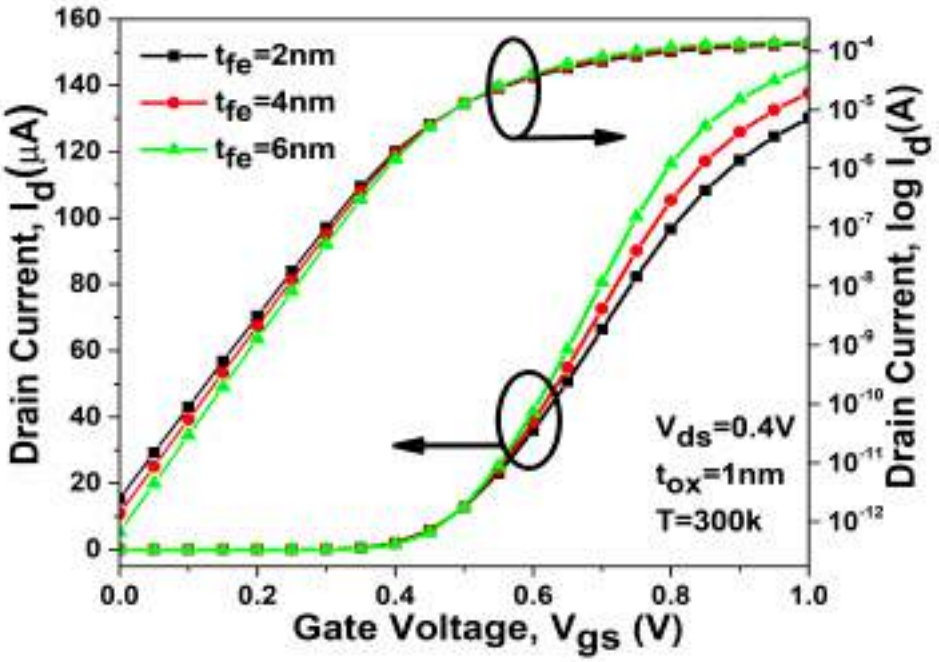

Figure 2.24: Variation in transfer characteristics of VS-HOI-GS-FeFinFET for different ferroelectric layer thickness (VC24a).

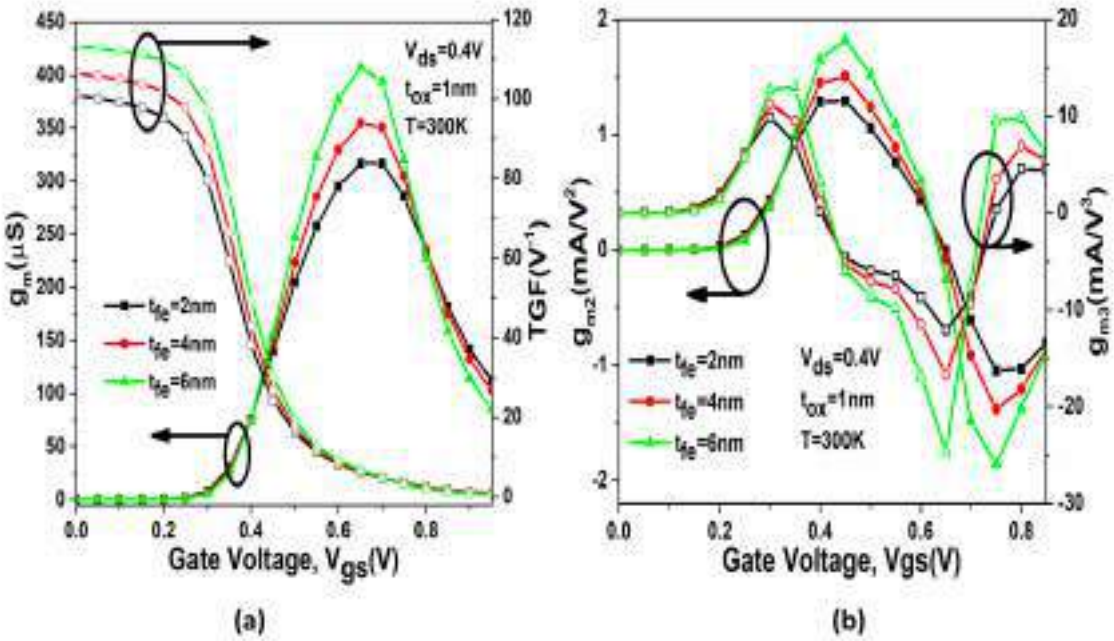

Figure 2.25: Variation in (a) transconductance and device efficiency (b) g_{m2} and g_{m3} of VS-HOI-GS-FeFinFET for various thickness of ferroelectric layer (VC24a).

Figure 2.24 displays the variation in transfer characteristics of VS-HOI-GS-FeFinFET with variation of ferroelectric thickness. It shows that as thickness is increased from 2nm to 6nm, the device's performance improves in terms of ON current and leakage current due to better charge

accumulation in the channel via stronger coupling of the channel and the gate with enhanced polarization, leading to the enhancement of switching ratio from 5.27×10^7 at 2nm to 2.19×10^8 at 6nm. This also results in increment in g_m and TGF of the device with increase in t_{fe} from 2nm to 6nm as displayed by Figure 2.25(a), indicating improved analog performance of the device with increase in ferroelectric thickness. Further, Figure 2.25(b) shows the higher-order coefficients of transconductance (g_{m2} and g_{m3}) which are defined as (second and third) order derivative of drain current with respect to V_{gs} at constant V_{ds}(PVMC24). The higher-order coefficients of transconductance provide an estimate about the non-linearity in a device. It confirms the improvement in linearity characteristics of the device with low values of g_{m2} and g_{m3} due to more uniform polarization switching as t_{fe} decreases from 6nm to 2nm.

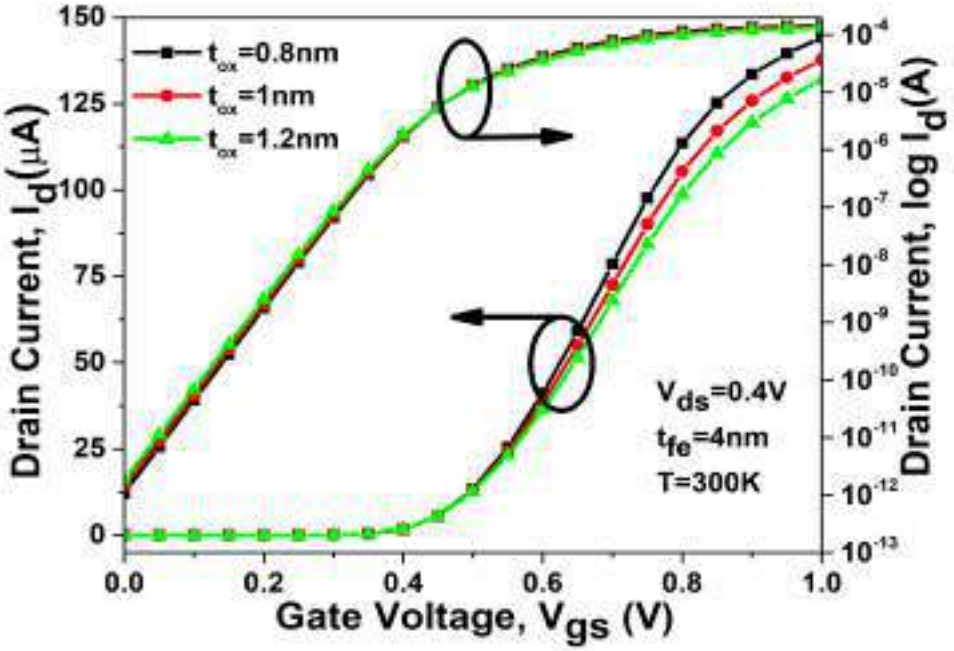

Figure 2.26: Variation in transfer characteristics of VS-HOI-GS-FeFinFET for different oxide layer thickness (VC24a).

Figure 2.26 also shows the variation in transfer characteristics of VS-HOI-GS-FeFinFET with variation in the thickness of oxide layer. It shows that as the oxide layer thickness decreases, the device performance improves with increment in ON current and reduction in leakage current due to better electrostatic control, thus leading enhancement in switching ratio from 7.29×10^7 at 1.2nm to 1.35×10^8 at 0.8nm. Further, Figure 2.27(a) also displays the improving trend for g_m and TGF due to improved amplification effect of ferroelectric layer with decreasing t_{ox}. But Figure 2.27(b) displays the opposite trend in the linearity performance of the device with degradation in g_{m2} and g_{m3}

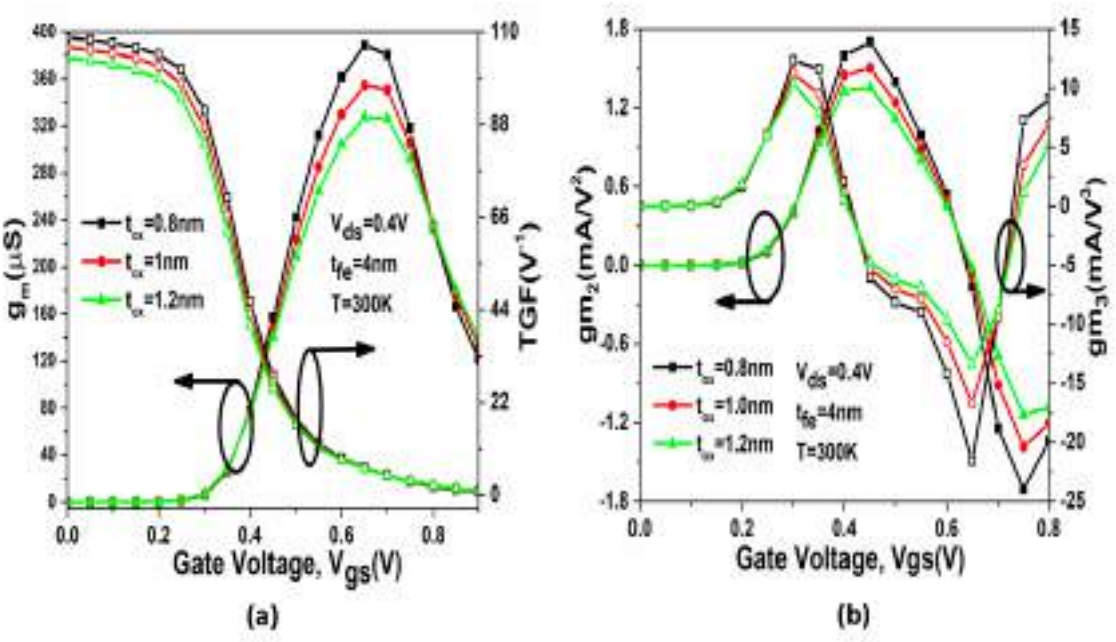

Figure 2.27: Variation in (a) transconductance and device efficiency (b) g_{m2} and g_{m3} of VS-HOI-GS-FeFinFET for various thickness of oxide layer (VC24a).

when t_{ox} decreases from 1.2nm to 0.8nm. As, it is observed that a noticeable analog performance is achieved at t_{fe}=4 nm and and t_{ox}=1 in VS-HOI-GS-FeFinFET without compromising linearity performance. Therefore, t_{fe}=4 nm and t_{ox}=1 nm are respectively considered as the optimum thickness of ferroelectric and oxide layer for VS-HOI-GS-FeFinFET.

2.4.6 Gate Stack Optimization for RF performance

From the RF application's point of view, various RF parameters of vital interest such as cut-off frequency, gain frequency product, transconductance frequency product, and gain transconductance frequency product are analysed. Figure 2.28 shows combined plot of total gate capacitance (C_{gg}) and unity gain cut-off frequency (f_T) as a function of gate to source voltage, V_{gs}. It is observed that C_{gg} increases very slowly with V_{gs} in the subthreshold region, but with further increase in V_{gs}, C_{gg} increases swiftly due to the enhanced lateral field, which enhances the movement of charge carriers from source to drain side. In radio frequency (RF) applications, high gate capacitance can be advantageous for achieving higher gain in RF amplifiers(KTP+24). So, Figure 2.28 well confirms the C4 configuration's ability to amplify high-frequency signals effectively as compared to its other counter parts.

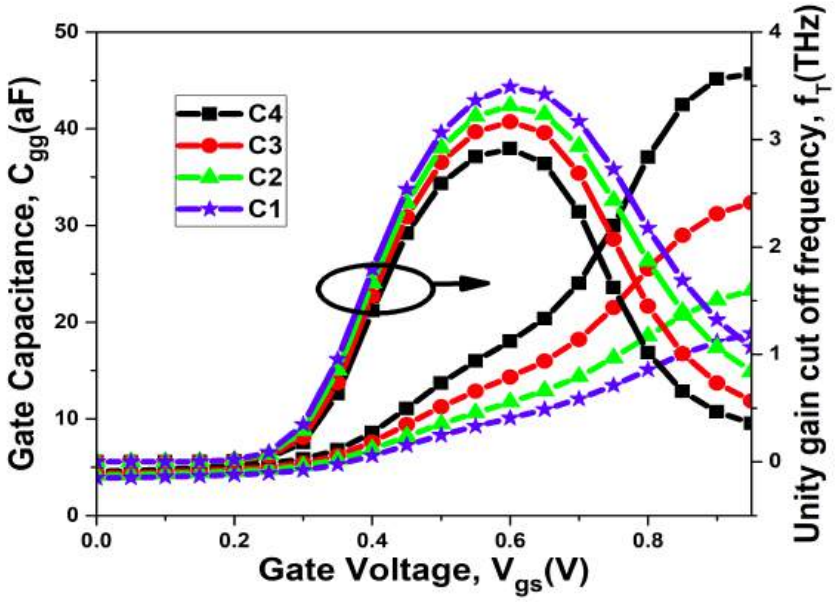

Figure 2.28: Variation in Gate Capacitance and Unity gain cut off frequency for different configurations (VC24a).

Unity gain cutoff frequency (UGCF) is a key parameter for understanding the bandwidth and frequency response characteristics of the system. In electronic systems, it is the point at which the gain of a device or circuit becomes 1 or 0 dB. Figure 2.28 shows that C4 showcase low UGCF as compared to other configurations because of high gate capacitance due to the high-k dielectric stack in C4 configuration, which is generally preferred to minimize the impact of noise and distortion on the output signal(JRG$^+$22).

The Gain Frequency Product (GFP), as given by Eq. 2.12 is a critical parameter characterizing the relationship between the gain and frequency response of a FET device and MOSFETs with a higher GFP are capable of amplifying signals across a broader range of frequencies(APG$^+$20). Figure 2.29 displays the peak values of GFP of all the four configurations considered for VS-HOI-GS-FeFinFET and attaining maximum peak value for C4 with 1.84 PHz as compared to 0.55 PHz for C1, makes C4 preferable for applications where a wide frequency range is crucial, such as in radio-frequency (RF) amplifiers and high-frequency communication systems. Transconductance Frequency Product (TFP), given by Eq. 2.13 also known as transit frequency represents the frequency at which the transconductance gain of the device starts to decrease, indicating its high-frequency performance limitations. Therefore, as shown in Figure 2.29, devices with higher TFP as offered by C4 with 60.6 THz/V as compared to 55.6 THz/V by C1 configuration, are desirable

for various RF applications.

$$GFP = \frac{g_{\mathrm{m}}}{g_{\mathrm{d}}} \times f_{\mathrm{T}} \tag{2.12}$$

$$TFP = \frac{g_{\mathrm{m}}}{I_{\mathrm{d}}} \times f_{\mathrm{T}} \tag{2.13}$$

$$GTFP = \frac{g_{\mathrm{m}}}{g_{\mathrm{d}}} \times \frac{g_{\mathrm{m}}}{I_{\mathrm{d}}} \times f_{\mathrm{T}} \tag{2.14}$$

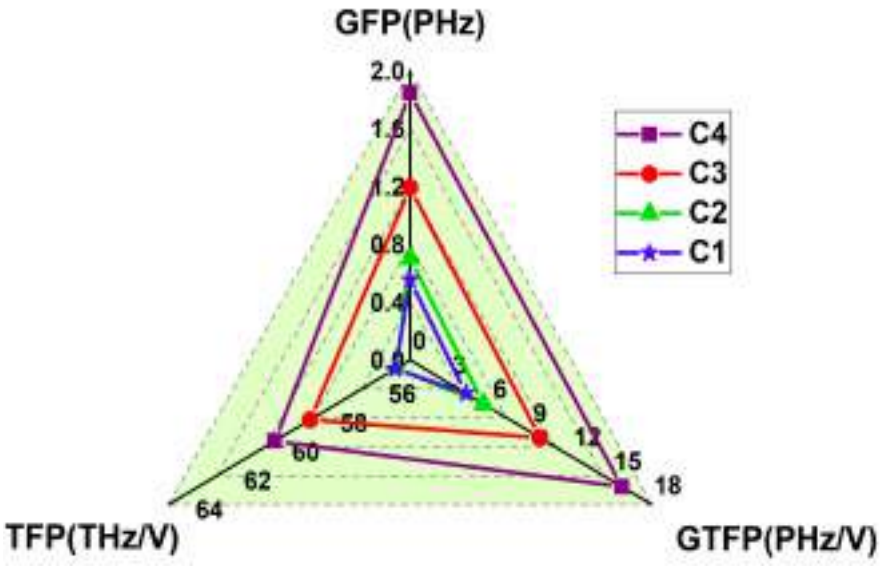

Figure 2.29: Variation in TFP, GFP and GTFP for different VS-HOI-GS-FeFinFET configurations. (VC24a).

Further, it also shows another important RF parameter, gain transconductance frequency product (GTFP) that combines the transconductance and the unity-gain frequency of a MOSFET as given by Eq. 2.14. Highest GTFP for C4 with 15.8 PHz/V as compared to 4.16 PHz/V for C1 contributes to improved signal fidelity, ensuring that the amplified output faithfully replicates the input signal. Therefore, with high desired value of GFP, TFP and GTFP, C4 can be very well integrated in fields like wireless communication, radar systems, and other RF applications where rapid signal processing is essential(PdNN24). Thus, C4 configuration exhibits the most enhanced performance in terms of different analog and RF metrics as compared to the other three configurations as shown in Table 2.5. In addition, the performance metrics obtained in this work have

been compared with several different devices in existing literatures, as shown in Table 2.6. It can be seen that the results obtained in this work stand out from the previously published work.

Table 2.5: Summary of different Analog and RF parameters for different configurations of VS-HOI-GS-FeFinFET

Parameter	C1	C2	C3	C4	Figure of Merit (FOM)
I_{on} (A)	1.08×10^{-4}	1.15×10^{-4}	1.27×10^{-4}	1.37×10^{-4}	26.91%
I_{off} (A)	6.39×10^{-12}	4.52×10^{-12}	2.26×10^{-12}	1.38×10^{-12}	78.40%
I_{on}/I_{off}	$1.69\times10^{+7}$	$2.56\times10^{+7}$	$5.63\times10^{+7}$	$9.97\times10^{+7}$	487.97%
$V_{th}(V)$	0.28	0.29	0.30	0.31	7.69%
SS (mV/dec)	67.35	66.21	64.11	62.73	6.84%
DIBL (mV/V)	69.14	61.14	49.14	40.14	41.52%
QF $(uS-dec/mV)$	3.56	4.0	4.79	5.66	58.98%
g_m (S)	2.36×10^{-4}	2.62×10^{-4}	3.07×10^{-4}	3.55×10^{-4}	50.42%
TGF (V^{-1})	$0.91\times10^{+2}$	$0.95\times10^{+2}$	$1.02\times10^{+2}$	$1.07\times10^{+2}$	17.58%
A_v (dB)	$1.70\times10^{+2}$	$2.28\times10^{+2}$	$4.08\times10^{+2}$	$6.94\times10^{+2}$	308.23%
$V_{EA}(V)$	2.48	2.85	3.79	5.10	105.64%
R_{out} (ohm)	$0.80\times10^{+6}$	$1.0\times10^{+6}$	$1.60\times10^{+6}$	$2.46\times10^{+6}$	204.45%
C_{gg} (F)	1.91×10^{-17}	2.37×10^{-17}	3.27×10^{-17}	4.55×10^{-17}	138.21%
F_t (Hz)	$3.49\times10^{+12}$	$3.31\times10^{+12}$	$3.17\times10^{+12}$	$2.92\times10^{+12}$	16.33%
GFP (Hz)	$5.52\times10^{+14}$	$7.0\times10^{+14}$	$11.90\times10^{+14}$	$18.40\times10^{+14}$	233.33%
TFP (Hz/V)	$5.56\times10^{+13}$	$5.56\times10^{+13}$	$5.91\times10^{+13}$	$6.06\times10^{+13}$	8.99%
GTFP (Hz/V)	$4.16\times10^{+15}$	$5.47\times10^{+15}$	$9.68\times10^{+15}$	$15.80\times10^{+15}$	279.80%

2.5 Summary

In this chapter, initially, performance of FeFinFET and VS-HOI-FeFinFET is compared for different performance parameters and it is found that VS-HOI-FeFinFET with Al_2O_3 as gate oxide performed better in comparison to FeFinFET on all examined parameters such as drain current, threshold voltage and subthreshold swing. Thus, VS-HOI-FeFinFET is further analysed for gate

Table 2.6: Comparison of the performance parameters of VS-HOI-GS-FeFinFET with the existing literature

Reference	$V_{ds}(V)$	Device structure	$I_{off}(A)$	$I_{on}(A)$	t_{fe}(nm)
This work	0.4	VS-HOI-GS-FeFinFET	1.38×10^{-12}	1.37×10^{-4}	4
(KAD20)	1	NC-FinFET	1.43×10^{-12}	1.80×10^{-5}	1.7
(STT^{+}17)	0.1	Fe-HZO-GeFinFET	0.88×10^{-10}	5.0×10^{-5}	-
(BNM^{+}20)	-	Fe-FinFET	2.10×10^{-10}	3.30×10^{-6}	7
(YLS^{+}21)	0.1	HZO Fe-FinFET	8.90×10^{-12}	1.0×10^{-6}	9
(OIH^{+}16)	0.5	NC-FinFET	4.20×10^{-11}	3.0×10^{-5}	5

stacked configuration for different gate stacked dielectric materials. In subsequent parts, this chapter presents the study of VS-HOI-GS-FeFinFET over VS-HOI-FeFinFET(Al_2O_3) while optimizing the gate stack material for upgraded static, analog, and RF performance. The C4 configuration exhibits the most enhanced performance as compared to the other three configurations as shown in Table 2.5 with stated figure of merit (FOM) of C4 over C1. In comparison to C1, C4 shows an increase in I_{on} by 26.91% and reduction in I_{off} by 78.4% thus results in significant increment in switching ratio. Further an increment in peak transconductance by 50.42% is observed in C4 over C1 along with improved subthreshold swing with reduction by 6.86%. As compared to C1, device efficiency (TGF) and V_{th} are also enhanced in C4 configuration by 17.58% and 7.69%. Other analog parameters such as A_V, V_{EA} and R_{out} also shows remarkable improvement in C4 with increment by 308.23%, 105.64% and 204.45% respectively as compared to C1. Also performance optimization of VS-HOI-GS-FeFinFET with variation in mole fraction of germanium, geometric dimensions of Fin, thickness of ferroelectric layer and oxide layer is explored for various analog metrics. Further, RF parameters like GFP also gets enhanced by 233.33% and GTFP by 279.80% for C4 over C1 configuration. Along with these parameters, improved ability of C4 for enhanced amplification with minimum distortion is depicted by increased gate capacitance and reduced unity gain cut off frequency by 138.21% and 16.33% respectively over C1, makes the device suitable for high performance analog and RF applications.

After thorough investigation of the device optimizations towards achieving superior electrostatic control and performance in VS-HOI-FeFinFETs, the next chapter extends the focus from device-level enhancements to reliability and circuit-level assessment. Since real-world devices inevitably

suffer from interfacial trap charges at the semiconductor/oxide interface, it becomes imperative to examine their impact on device behavior. By incorporating gate engineering and developing hetero dielectric vertically stacked ferroelectric based FinFET (HD-VS-FeFinFET), the study not only mitigates the adverse effects of ITCs but also demonstrates significant improvements in analog, linearity, and circuit-level performance. This transition from geometry-driven optimization to reliability-centric design completes the continuum of work, establishing a holistic framework that ensures both high performance and robust functionality of the device. This will be the main area of emphasis in the next chapter.

Chapter 3

Unveiling the Impact of Interfacial Trap Charges on Strained Vertically Stacked FeFinFETs for Improved Reliability:Device to Circuit Level Assessment

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* This chapter focuses on the device to circuit level assessment of Si/SiGe strained vertically stacked ferroelectric based FinFETs (VS-FeFinFET) for improved reliability under the influence of interfacial trap charges (ITCs) at the semiconductor/oxide interface.

* Gate engineering has also been incorporated to form hetero dielectric vertically stacked ferroelectric based FinFET (HD-VS-FeFinFET), which results to 91.48% reduction in leakage current, led to 13 times increment in switching ratio along with improvement in quality factor by 46.01%, transconductance by 32.77%, and device efficiency by 26.54% with negligible variations due to ITCs as compared to VS-FeFinFET.

* Various linearity and harmonic parameters also improved and showed negligible average variations like 4.72% (177.15%) in VIP2 and 6.52% (25.3%) in 1-dB compression point for HD-VS-FeFinFET (VS-FeFinFET) against different ITCs polarity making it more reliable for low power microwave and distortionless wireless communication applications.

* Further, logic circuit application of HD-VS-FeFinFET based CMOS inverter has been analysed and it shows improvement by 17.9% in transition range, 51.67% in voltage gain along with

minimal ITCs induced average variation of 3.66% (15.88%) in noise margin for HD-VS-FeFinFET(VS-FeFinFET) based circuit, showcasing its enhanced reliability at circuit level.

* Thus, with the comprehensive analysis done on the intricacies of ITCs from device to circuit level, this chapter provides insights into the development of HD-VS-FeFinFET with enhanced functionality, reliability, and performance, poised to shape the landscape of modern electronics.

3.1 Introduction

Chapter 2 showcased that the optimization analysis carried out on the VS-FeFinFET has established the device as a highly promising candidate for next-generation nanoelectronics, by demonstrating remarkable improvements across static, analog, and RF performance metrics. The results of this multi-faceted optimization highlight the potential of the VS-FeFinFET as a high-performance, energy-efficient device architecture that successfully addresses several limitations of conventional CMOS scaling. However, while these enhancements underline the device's promise under ideal conditions, a comprehensive evaluation also requires addressing its reliability under practical operating scenarios. In particular, the role of interfacial trap charges (ITCs) at the semiconductor–oxide boundary becomes critical, as these traps are unavoidable in real devices and can influence threshold stability, switching behavior, and long-term performance(Hol16; Chi11). Thus, having established its optimized static and dynamic performance, it becomes imperative to investigate the reliability of the device under ITC-induced effects, ensuring its robustness for future applications in advanced electronic systems.

The continuous increase in the packing density of integrated circuits raises serious concerns regarding device reliability, primarily due to the higher probability of interface trap generation(RFT16; Chi11). In nanoscale device fabrication, process-induced imperfections, stress-related damage, and radiation exposure often lead to the formation of ITCs(MC16). These traps have been widely recognized as one of the major factors contributing to the degradation of device reliability and operational lifetime.

Earlier studies on nanoscale devices often overlooked the effect of ITCs by assuming that compound oxide, commonly used as a gate dielectric or interfacial layer, behaves as an ideal insulator free from defect states. In reality, however, a substantial density of charged defects exists either at the interface or within the oxide layer itself. These include fixed oxide charges, mobile ionic charges, oxide-trapped charges, and interface traps(Hil81; NB02). Although advances in fabrication technology have significantly reduced their concentration, such charges are unavoidable in highly scaled devices and continue to affect device operation, especially under conditions of high packing density(JXS$^+$17).

From a microscopic perspective, interface traps arise due to the presence of unsaturated bonds at the semiconductor/oxide interface. These unsatisfied bonds create localized states within the silicon bandgap, distinct from the conduction or valence band. Carriers occupying these localized states—electrons or holes—remain immobilized, leading to charge trapping and de-trapping events that manifest as instabilities in device parameters. Specifically, donor-type traps may behave as positively charged when unoccupied and neutral when filled with electrons, whereas acceptor-type traps exhibit negative charge when occupied and remain neutral when vacant. Typically, donor traps are situated close to the valence band edge, while acceptor traps are positioned near the conduction band edge(Shl20; OK18).

While extensive studies exist on the influence of ITCs in MOSFETs, investigations into their impact on ferroelectric FinFET (FeFinFET) devices remain limited, despite their growing importance. For FeFinFET devices, the presence of these traps becomes even more critical due to the combined effects of ferroelectric switching and interface state dynamics. The additional coupling between ferroelectric polarization and interface charges may lead to hysteresis broadening, threshold voltage fluctuations, degraded subthreshold swing, and reduced current drivability(ZPPA23; Hol16; DZK$^+$22). Therefore, unlike conventional MOSFETs where ITC effects are relatively well understood, FeFinFETs demand a more comprehensive reliability study to capture the interplay between ferroelectric, multigate electrostatics, and interfacial defect states. This makes ITC analysis an essential step toward validating the long-term stability and practical applicability of FeFinFET technology for future high-performance and energy-efficient electronic systems.

At the heart of FeFinFETs lies the interface between oxide and semiconductor layers, where the dynamics of interfacial trap charges (ITCs) exert a profound influence on device performance and functionality. The dynamics of these ITCs are affected by various elements such as material composition, processing techniques, and operational environment(Chi11). There are various factors responsible for occurrence of these ITCs. Firstly, the creation of dangling bonds due to disruption of atomic lattice at the S/O interface which leads to creation of energy states with in the bandgap of the semiconductor. Secondly, contamination of the surface with impurities can introduce localized states that trap charges(SBKM88). Further, other factors may be thermal oxidation process during growth of oxide layer, high energy radiation during ion implantation, electrical stress during operation or testing, mechanical stress during deposition or thermal expansion can break bonds

or introduce defects, ultimately creating ITCs. Thus, the complexity introduced by ITCs at the semiconductor-oxide (S/O) interface in FeFinFETs calls for careful research to investigate their impact on device behavior and explore effective mitigation strategies. Proper management of ITCs is key to unlocking their full potential and enhancing the reliability of these devices across diverse applications. Various potential methods can be incorporated in the devices to mitigate these ITCs such as passivation techniques, optimized thermal oxidation, surface cleaning before deposition, high-k dielectric materials, low-damage deposition techniques like atomic layer deposition (ALD), etc(QWHH14a; Mir15; HJCK20).

In this chapter, gate stack engineering with heterogeneous gate dielectric (Al_2O_3+HfO_2) is incorporated in VS-FeFinFET to form HD-VS-FeFinFET, a novel combination of Si/SiGe strained tri-layered channel-engineered, heterostructure on insulator FeFinFET, and has been examined to minimize the effect of ITCs. The combination leverages the passivation properties of Al_2O_3 and the high-k benefits of HfO_2(ZPB$^+$19). Al_2O_3 is used as an interfacial layer (t_{ox1}), which is known for high-quality interface with semiconductors leading to reduced dangling bonds and ITCs. Al_2O_3 has a high bandgap (∼9 eV), which minimizes creation of energy states, further reducing trap density at the interface(QWHH14b). Then, the high-k nature of HfO_2 reduces the electric field stress at the interface, thereby minimizing the generation of new traps. HfO_2 also exhibits good thermal stability, reducing defect formation during high-temperature processing. Thus, the stacked structure minimizes the density of trap charges at both the interface and within the dielectric layers. These dielectrics are also compatible with ALD processes, allowing precise thickness and composition control(CSF$^+$21). Thus, the combination of Al_2O_3 and HfO_2 uses their complementary properties, such as Al_2O_3's superior passivation and HfO_2's high-k dielectric performance, make them ideal for next-generation electronic devices requiring high efficiency and robust reliability(ZPB$^+$19).

In this chapter, the detailed analysis of static, analog, linearity, and harmonic distortion performance under the influence of ITCs is done for HD-VS-FeFinFET to examine how the gate stack engineering combining the complementary properties of Al_2O_3 and HfO_2 mitigates the influence of ITCs and its performance is compared with VS-FeFinFET. Further, the work is extended to discuss the influence of ITCs at the circuit level by comparing the performance of HD-VS-FeFinFET based CMOS inverter with VS-FeFinFET based CMOS inverter for improved efficiency and reliability. This chapter is organized as follows: Section 3.2 includes all the specifications regarding the device

structure. The simulation framework mentioning the physical models used and fabrication feasibility for the device are discussed in section 3.3. Section 3.4 provides the results and discussion for the analog, linearity, and harmonic distortion performance at the device level along with discussion at circuit level. Section 3.5 provides a complete summary of the chapter.

3.2 Device Structure

Figure 3.1(a) depicts the 3-dimensional structure of HD-VS-FeFinFET, while Figure 3.1(b) and Figure 3.1(c) respectively shows the device's vertical 2-dimensional view chopped through its fin and inset of trap-carrier interaction at the semiconductor-oxide interface of HD-VS-FeFinFET. The gate length (L_g) considered for the device is fixed at 20nm where silicon-doped hafnium oxide (HfO_2FE) is used as the ferroelectric material with thickness (t_{fe}) fixed at 6 nm with total gate oxide dielectric thickness (t_{ox}) fixed at 1nm. The total gate oxide is composed of a heterogeneous dielectric stack consisting of equal proportion of Al_2O_3 and HfO_2, each with a thickness of 0.5nm. The height and width of the fin are taken as 30nm and 8 nm respectively. A tri-layered strained-silicon channel system is formed with the help of SiGe sandwiched between two silicon layers as Si-$Si_{0.7}Ge_{0.3}$-Si (where $Si_{0.7}Ge_{0.3}$ represents that the mole fraction of Si and Ge is taken as 0.7 and 0.3 respectively). The doping concentration of source/drain is fixed as 1×10^{20} cm^{-3} with n-type and that of channel is 1×10^{16} cm^{-3} with p-type. The length of the source/drain electrodes ($L_{s/d}$) is fixed at 20nm. In addition, a metal gate with a work function of 4.65 eV, which has excellent thermal stability and is compatible with CMOS processing, is utilized in this device to prevent any poly-depletion effect that is common in polysilicon gates. Further, to exploit the advantages of SOI technology, the entire heterostructure FeFinFET is built on an insulator SiO_2 box whose width, height, and length are kept 32nm, 5nm, and 62nm respectively. To unveil the intricacies of ITCs on the device reliability and performance, ITCs with different polarity have been introduced at the S/O interface with trap charge density to be fixed at 10^{12} cm^{-2} based on formerly reported literature(Chi11; SBKM88; QWHH14b).

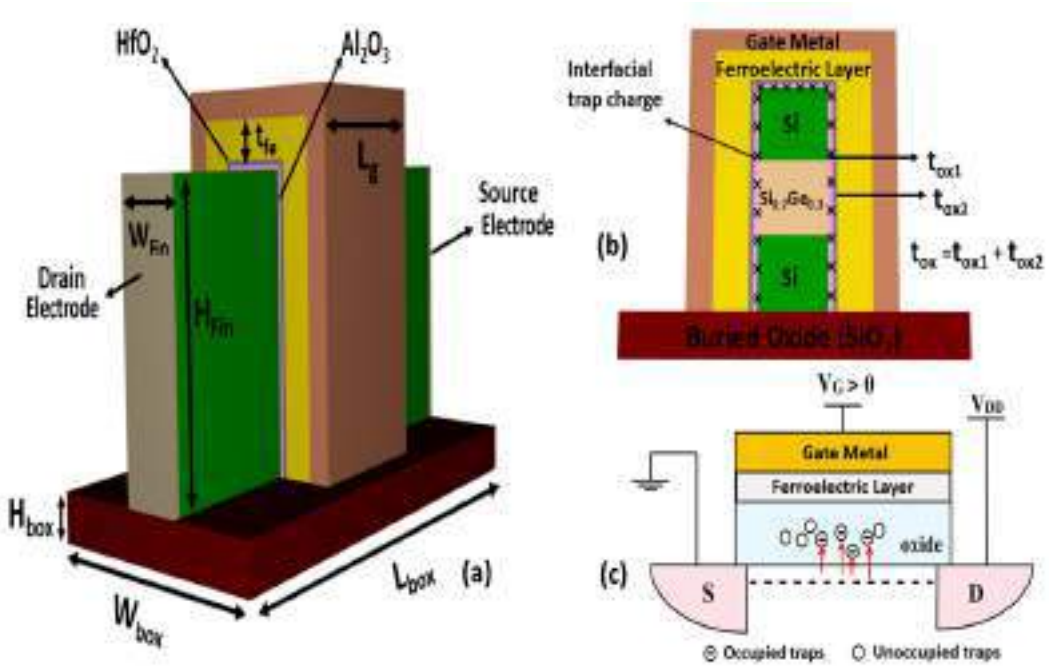

Figure 3.1: (a) 3D schematic view of HD-VS-FeFinFET (b) vertical cross-sectional view of HD-VS-FeFinFET (c) inset of trap-carrier interaction at the semiconductor-oxide interface of HD-VS-FeFinFET(VC25b).

3.3 Simulation Methodology and Fabrication Feasibility

All the simulations have been carried out using Genius 3D TCAD simulator by Cogenda. For the validation of the models used in the simulator tool, the TCAD simulation result for Silicon on Insulator (SOI) FinFET structure has been calibrated with experimental data(LGN$^+$14), and a reasonably good agreement between the two results validates the various models used in the study as displayed by Figure 3.2. The simulation setup includes the drift-diffusion model level 1 (DDML1) which keeps the lattice temperature constant throughout the solving procedure, coupled with consistent Poisson and continuity equations to govern the carrier transport phenomena for the holes and the electrons. The temperature and doping-dependent carrier recombination-generation phenomenon are accurately captured by Shockley-Read-Hall (SRH) recombination and Auger models(PMC23). Further, Lombardi mobility model for silicon and Philips mobility model for SiGe are used to consider the mobility degradation at the S/O interface(VC23). Lucent model is used to consider the high-field mobility effects along with hot carrier models for capturing the effect of hot carriers. To check the velocity saturation and mobility of carriers, the velocity saturation model, and Esurface models are activated. The density gradient method is also used to incorporate

quantum confinement phenomena along with the Fermi-Dirac carrier statistics model(Ref). Further, the position and polarity of ITCs in the device are mentioned using the INTERFACE statement along with Trap models to capture the associated mechanisms(QWHH14a). A few abbreviations are used in this paper such as PITC - positive interfacial trap charge, NITC - negative interfacial trap charge, WITC - without (neutral) interfacial trap charge.

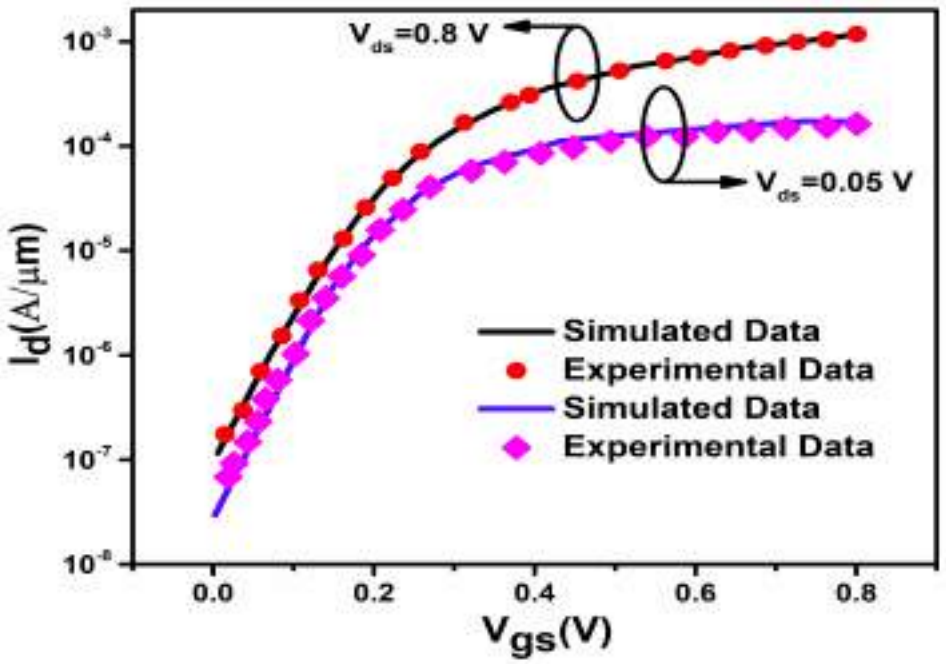

Figure 3.2: Experimental and simulated transfer characteristic for Silicon on Insulator (SOI) FinFET at V_{ds}=0.05V and V_{ds}=0.8V (VC25b).

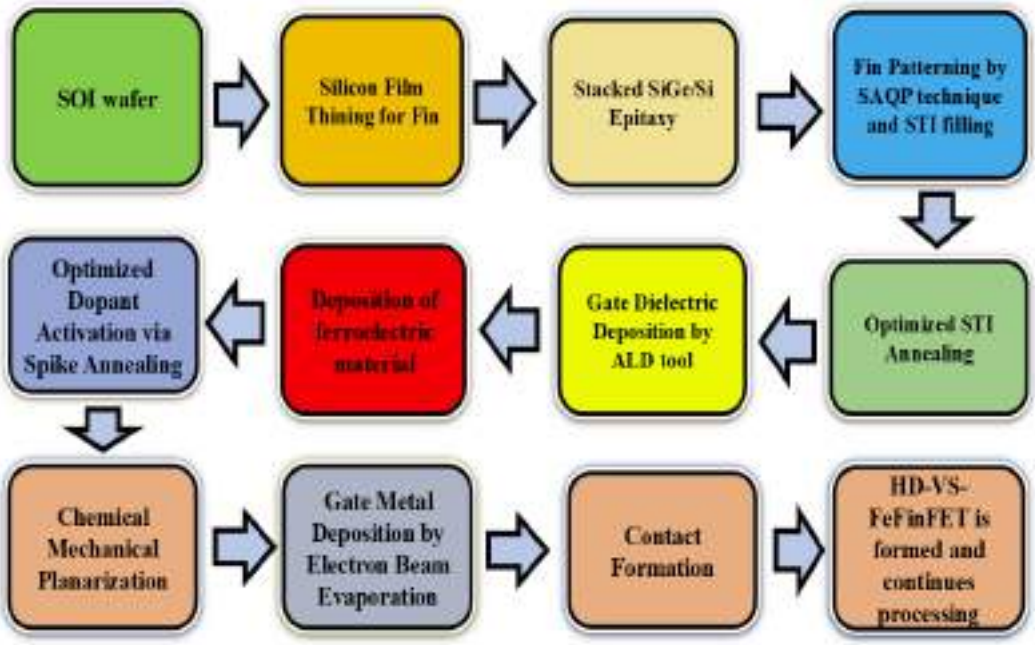

Figure 3.3: Fabrication process flow chart for HD-VS-FeFinFET (VC25b).

Figure 3.3 displays the fabrication feasibility of the HD-VS-FeFinFET using a step-by-step

fabrication process flowchart. As the starting material SOI wafer is used with a thick buried oxide layer and thick silicon film followed by silicon film thinning for fin. Afterwards stacked SiGe/Si tri-layer were epitaxially grown by reduced-pressure chemical vapor epitaxial deposition. Thereafter, fin patterning is done using the self-aligned quadruple patterning (SAQP) technique followed by shallow trench isolation (STI) filling and an optimized STI densification annealing which is performed with a rapid thermal annealing (RTA) at an optimized temperature. The gate dielectric is deposited on the silicon interfacial layer by atomic layer deposition (ALD) followed by ferroelectric layer deposition over the gate oxide using ALD technique. The drain and source regions are implanted, and the dopants of these regions are activated using spike annealing followed by chemical mechanical planarization for smoothening the surface. Metal gate is deposited using electron beam evaporation at room temperature on the top of the ferroelectric layer. The source/drain metal contacts are also deposited by electron beam evaporation followed by lift-off process. This completes the process of manufacturing the HD-VS-FeFinFETs(AAAea17)(CMY20).

3.4 Result and Discussion

3.4.1 Influence of ITCs on static and analog performance

In this section, the effect of ITCs polarity at the S/O interface is analysed to study the static and analog performance for both the devices (HD-VS-FeFinFET and VS-FeFinFET) at supply voltage V_{ds}=0.4V and at constant temperature 300K. Figure 3.4 displays the transfer characteristics of both the devices with different polarity. The presence of ITCs leads to altercation in flat band voltage (V_{fb}) as given by Eq. 3.1, where q is the electronic charge, N_{it} is the ITCs density and C_{ox} is gate oxide capacitance.

$$V_{\mathrm{fb}} = \frac{qN_{\mathrm{it}}}{C_{\mathrm{ox}}} \tag{3.1}$$

The changes in V_{fb} caused by PITC/NITC leads to modification in threshold voltage (V_{th}) as related by Eq. 3.2, where x_t is maximum space charge width, N_a is accumulated charge and ψ_{fp} is built in potential.

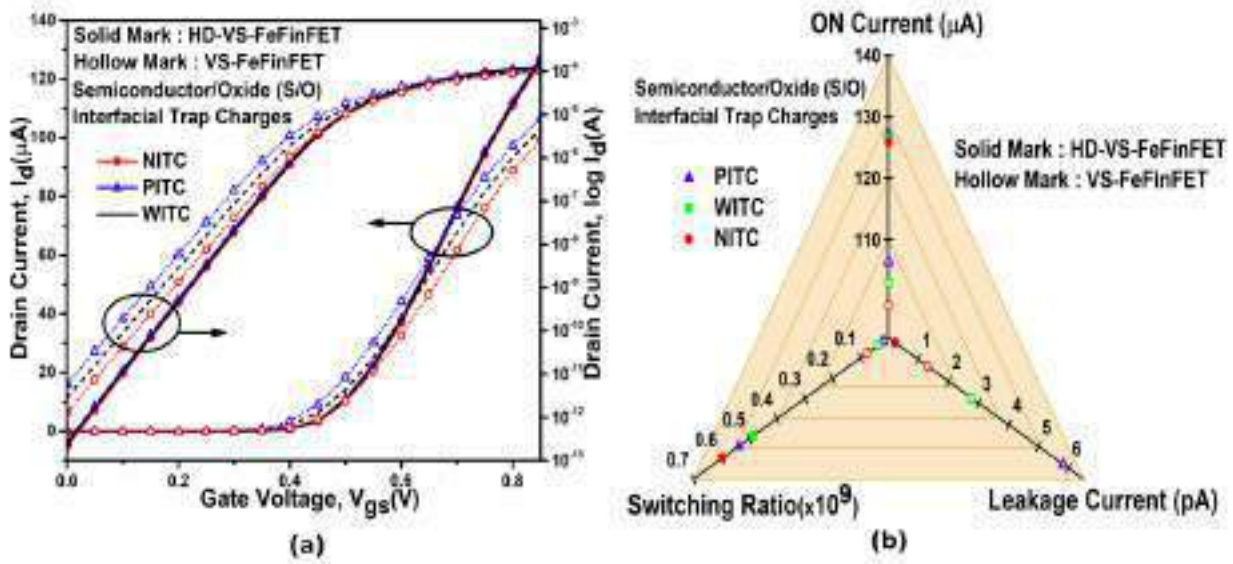

Figure 3.4: Transfer characteristics of HD-VS-FeFinFET and VS-FeFinFET in (a) linear and log scale at V_{ds}=0.4V (b) Comparison of different device characteristics such as ON current (I_{on}), leakage current (I_{off}) and switching ratio (I_{on}/I_{off}) in presence of different ITCs at V_{ds}=0.4V (VC25b).

$$V_{\mathrm{th}} = V_{\mathrm{fb}} + \psi_{\mathrm{fp}} + \frac{qN_{\mathrm{a}}x_{\mathrm{t}}}{C_{\mathrm{ox}}} \tag{3.2}$$

This modification in V_{th} leads to change in device characteristics thus change the ON current (I_{on}) and leakage current (I_{off}) of the device as shown in Figure 3.4(a) (AYA23). The use of high-k dielectric led to reduced interface states and traps at the S/O interface which improves the carrier mobility within the channel region as can be very well observed in elevated I_{on} of HD-VS-FeFinFET. The PITC (NITC) increases (decreases) the ON current by 0.59% (0.62%) and 3.35% (3.64%) in HD-VS-FeFinFET and VS-FeFinFET respectively. I_{off} with NITC (PITC) decreases (increases) by 11.01% (10.02%) in HD-VS-FeFinFET in comparison to deviation in VS-FeFinFET in presence of PITC (NITC) by 111% (53.1%), as depicted in Figure 3.4(b) which confirms that the transfer characteristics of HD-VS-FeFinFET are less affected by ITCs, proving it more reliable in contrast to VS-FeFinFET. Figure 3.5(a) shows the variation of output characteristics with drain bias for different ITC polarity. Owing to the suppression of channel hot carrier injection with the incorporation of hetero dielectric gate engineering in HD-VS-FeFinFET, there is negligible impact on output conductance (g_d) due to ITCs as showcased in Figure 3.5(b), thereby confirming its improved reliability.

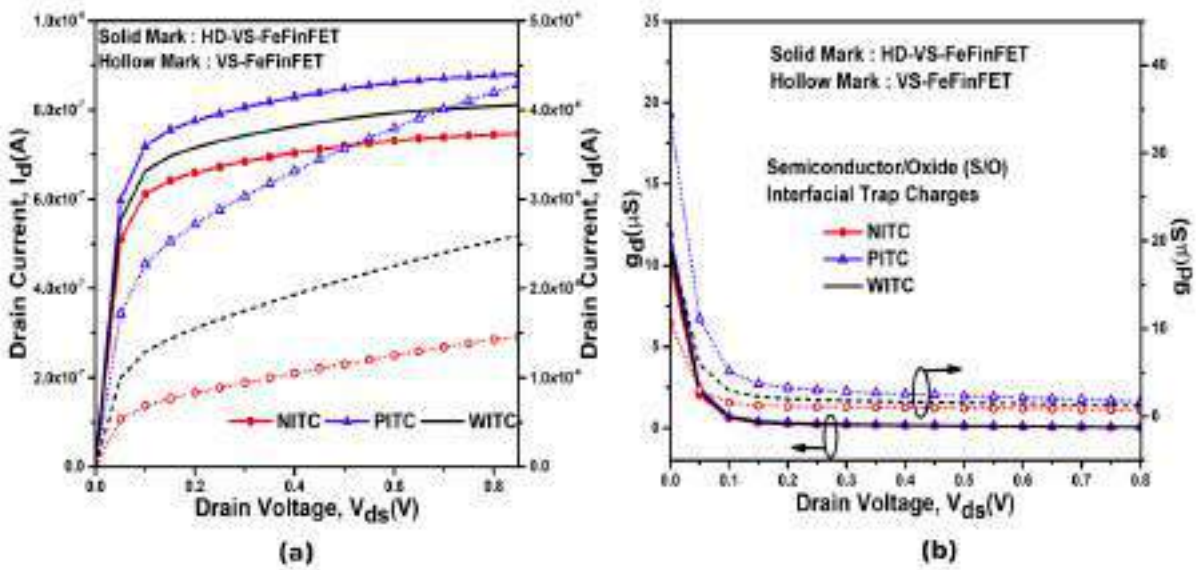

Figure 3.5: Effect of ITCs on (a) drain current (I_d) and (b) output conductance (g_d) for HD-VS-FeFinFET and VS-FeFinFET at V_{ds}=0.4V (VC25b).

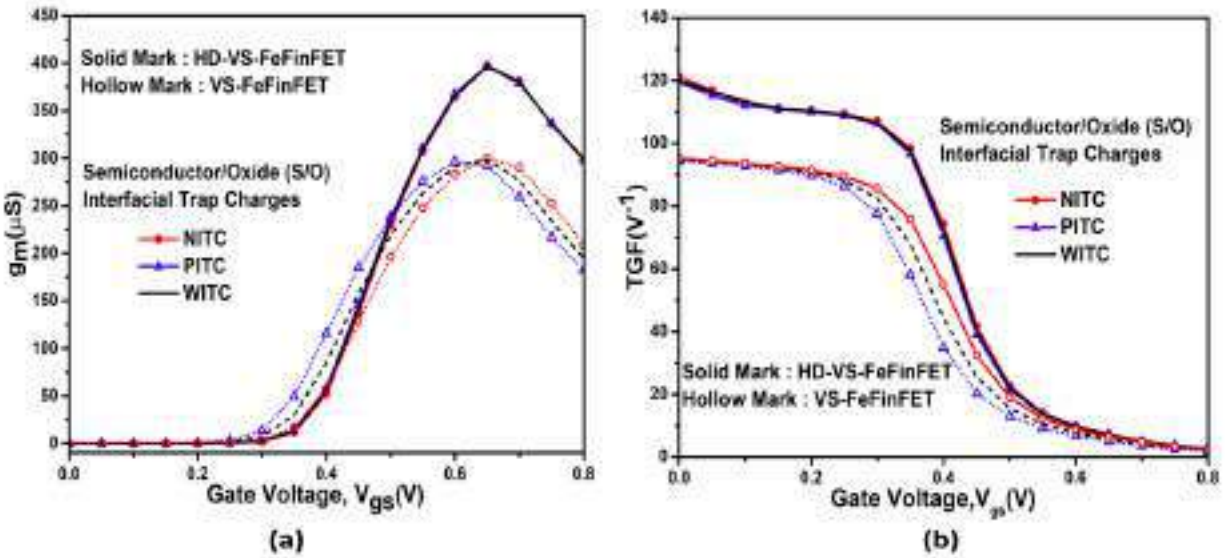

Figure 3.6: Variation in (a) transconductance (g_m) and (b) device efficiency (TGF) in presence of different ITCs at V_{ds}=0.4V (VC25b).

Figure 3.6(a) and Figure 3.6(b) respectively shows the variation of transconductance (g_m) and device efficiency, also known as Transconductance Generation Factor (TGF) of both the devices for different ITC polarity. HD-VS-FeFinFET achieves higher g_m and TGF because the heterogeneous dielectric improves electrostatic control and enhances carrier mobility at the interface. This allows more efficient modulation of the drain current with gate voltage, thereby improving the conversion of DC characteristics into AC performance metrics(LFH$^+$18). Moreover, the stronger dielectric screening minimizes the impact of ITCs, leading to smaller variations in g_m and TGF as compared

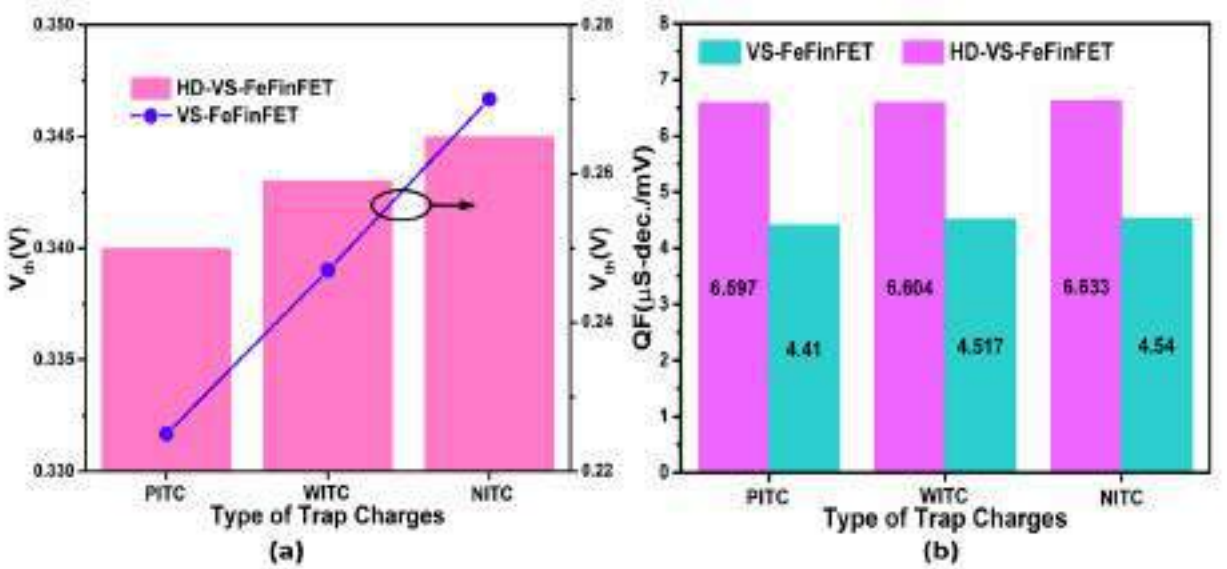

Figure 3.7: Effect of ITCs on (a) threshold voltage (V_{th}) (b) quality factor (QF) of HD-VS-FeFinFET and VS-FeFinFET at V_{ds}=0.4V (VC25b).

to its counterpart, thus highlighting the improved efficiency and reliability of the HD-VS-FeFinFET Also, in the case of NITCs, the repulsion of electrons from the interface further reduces trap-assisted scattering, enhancing carrier transport and preserving mobility. As a result, both g_m and TGF attain even higher values under NITC conditions.

PITC(NITC) acts to decrease (increase) the threshold voltage (V_{th}) but the variation in V_{th} is minute in case of HD-VS-FeFinFET whereas the V_{th} for PITC(NITC) is decreased (increased) by 8.9% (9.3%) in VS-FeFinFET as displayed in Figure 3.7(a). ITCs introduce additional energy states within the bandgap of semiconductor material which can capture and release charge carriers leading to energy dissipation(AYA23)(VC24a). This energy loss affects the overall Quality factor (QF) as showcased by both the devices in Figure 3.7(b), as energy stored in the system is dissipated due to trap-assisted recombination and scattering mechanisms. Also, NITCs repel electrons from the interface thus reducing the trap-assisted recombination. As a result, more energy is preserved in the system, leading to a higher quality factor in case of NITCs as compared to the case with PITCs, which tend to attract carriers and enhance energy loss.

Figure 3.8(a) shows the output resistance (R_{out}) for both the devices in presence of ITCs and higher R_{out} ensures better signal fidelity by suppressing voltage variations for changes in load resistance as shown by HD-VS-FeFinFET. High-k dielectric materials help in minimizing the variation in R_{out} caused by ITCs due to their ability to lower interface trap density and provide stronger

electrostatic control over the channel(SSP22)(YMM^{+}16). The peak value of R_{out} is increased (decreased) by 56% (29.9%) on introduction of NITC(PITC) at S/O interface of VS-FeFinFET as compared to increase (decrease) by 12% (10.6%) showing more immunity of HD-VS-FeFinFET towards ITCs.

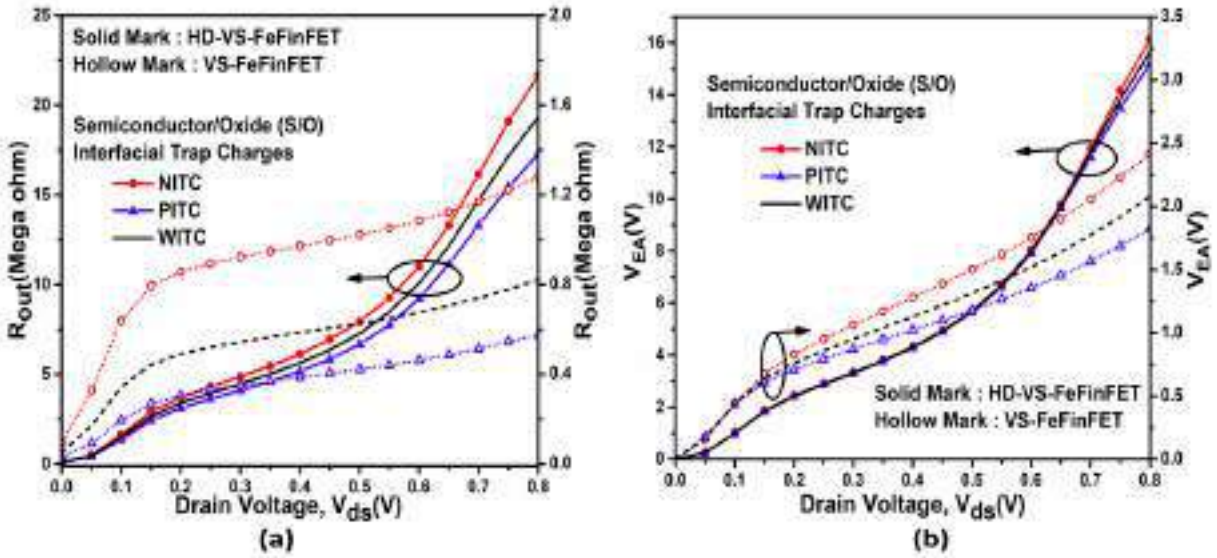

Figure 3.8: Impact of ITCs on (a) output resistance (R_{out}) (b) early voltage (V_{EA}) of HD-VS-FeFinFET and VS-FeFinFET at V_{ds}=0.4V (VC25b).

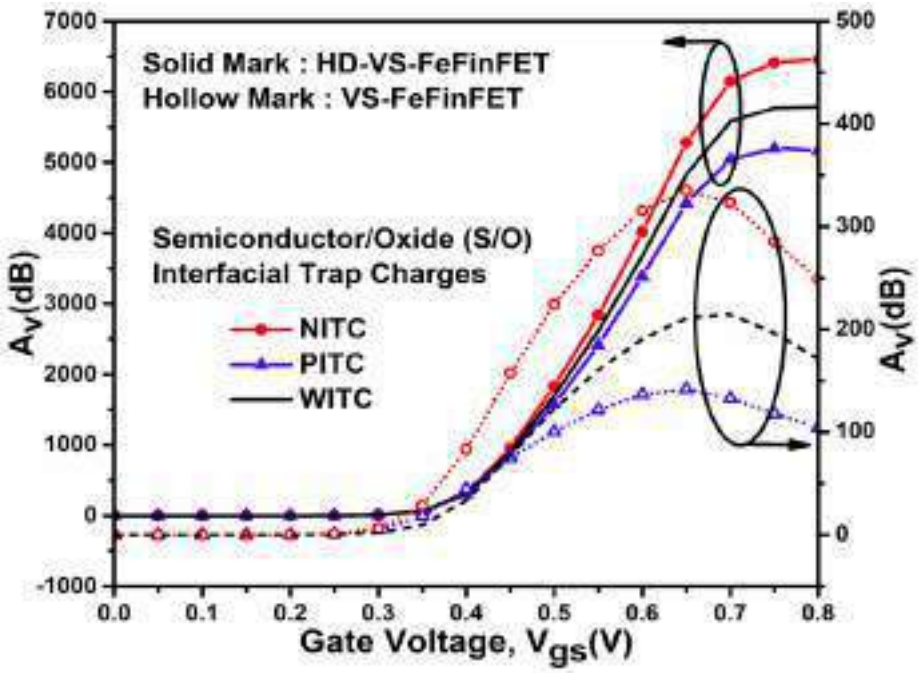

Figure 3.9: Variation of intrinsic gain (A_v) for HD-VS-FeFinFET and VS-FeFinFET in presence of different ITCs at V_{ds}=0.4V (VC25b).

Further, early voltage (V_{EA}) measures how quickly the output current increases in response

Table 3.1: Summary of different Analog parameters for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	1.06×10^{-4}	1.03×10^{-4}	9.92×10^{-4}	1.27×10^{-4}	1.26×10^{-4}	1.25×10^{-4}
I_{off} (A)	5.83×10^{-12}	2.77×10^{-12}	1.30×10^{-12}	2.62×10^{-13}	2.36×10^{-13}	2.12×10^{-13}
I_{on}/I_{off}	$1.83\times10^{+7}$	$3.72\times10^{+7}$	$7.65\times10^{+7}$	$5.37\times10^{+8}$	$4.86\times10^{+8}$	$5.94\times10^{+8}$
$V_{th}(V)$	0.225	0.247	0.270	0.340	0.343	0.345
QF ($\mu S-dec/mV$)	4.41	4.52	4.54	6.60	6.60	6.63
g_m (S)	2.92×10^{-4}	2.99×10^{-4}	3.0×10^{-4}	3.97×10^{-4}	3.97×10^{-4}	3.97×10^{-4}
TGF (V^{-1})	94.43	94.76	95.10	119.46	119.91	121.23
A_v (dB)	$1.42\times10^{+2}$	$2.11\times10^{+2}$	$3.35\times10^{+2}$	$5.16\times10^{+3}$	$5.78\times10^{+3}$	$6.45\times10^{+3}$
$V_{EA}(V)$	1.82	2.07	2.41	15.17	15.63	16.12
R_{out} (ohm)	$5.74\times10^{+5}$	$8.19\times10^{+5}$	$1.27\times10^{+6}$	$1.72\times10^{+7}$	$1.93\times10^{+7}$	$2.16\times10^{+7}$

to V_{ds} and trap charges in localized states within the semiconductor leading to deviations from ideal transistor behaviour. But owing to the implementation of heterogeneous dielectric in HD-VS-FeFinFET, which provides stronger electrostatic control and better charge screening, there is only 3.09% (2.98%) increase (decrease) in presence of NITC (PITC) as compared to 12.3% (16.3%) increase(decrease) in its counterpart as shown in Figure 3.8(b), making it more apt for high-speed analog circuits(PVMC24). Figure 3.9 displays the comparison plots of intrinsic gain (A_v) for both the devices in presence of ITCs. Heterogeneous dielectric and ferroelectric material stack in HD-VS-FeFinFET provides internal voltage amplification that boosts g_m, plus it improves electrostatics which reduces g_{ds} thus ultimately led to higher A_v along with less variability due to ITCs. So, HD-VS-FeFinFET is more immune and reliable for analog performance as compared to VS-FeFinFET that shows huge deviations of 45.4% (38.8%) increment (decrement) for NITC(PITC). Table 3.1 showcases the parametric value of different performance metrics under the influence of ITCs.

3.4.2 Influence of ITCs on linearity, harmonic and intermodulation distortion performance

Designing modern circuits and communication systems requires improved linearity and minimal distortion of signals to ascertain desired output at the receiver end. To take into account the non linearity issue, the influence of ITCs at S/O is investigated on various linearity and distortion parameters such as g_{m2}, g_{m3}, VIP2, VIP3, 1 dB compression point, IMD3, IIP3, etc for both the devices, HD-VS-FeFinFET and VS-FeFinFET. The importance of these higher-order derivatives lies in their direct influence on circuit gain, distortion, linearity, wireless performance, and power consumption. Designers must precisely analyze and optimize these parameters to meet the particular requirements of the application, thereby guaranteeing the circuit's reliability and overall success(LC20).

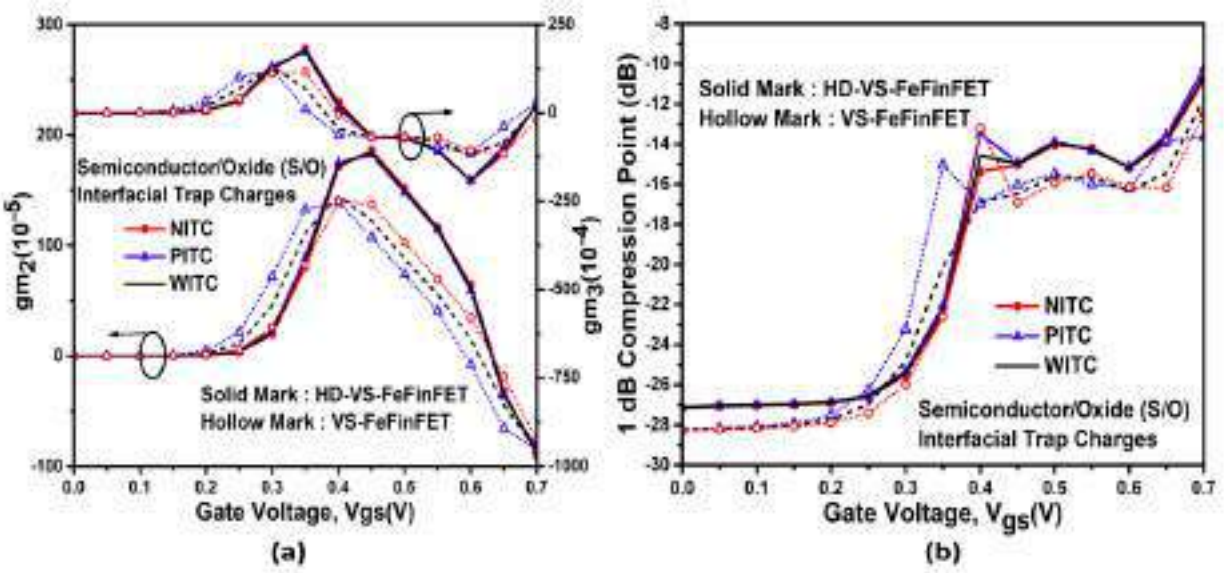

Figure 3.10: Impact of ITCs on (a) higher order transconductance coefficient (g_{m2} and g_{m3}) (b) 1-dB Compression Point of HD-VS-FeFinFET and VS-FeFinFET at V_{ds}=0.4V (VC25b).

The higher-order coefficients of transconductance provide an estimate about the non-linearity in a device. g_{m2} (g_{m3}) is the second (third) order transconductance coefficient that quantifies the second (third) order nonlinearity in a MOSFET, affecting even (odd) order distortion in circuits(DMC22). Figure 3.10(a) displays that the incorporation of heterogeneous dielectric in HD-VS-FeFinFET results into negligible deviation in g_{m2} and g_{m3} due to ITCs as compared to in-

crease (decrease) in peak value in VS-FeFinFET in presence of NITC (PITC). Figure 3.10(b) shows another important parameter, 1 dB compression point which denotes the level of input power at which shifting of output power from linearity by 1 dB occurs(WS78). The figure displays higher value of 1 dB compression point for HD-VS-FeFinFET due to enhanced g_m thus ensures reduced signal distortion. Also, there is negligible increase (decrease) of 7.57% (5.48%) in 1dB compression point on existence of PITC(NITC) in HD-VS-FeFinFET as compared to 27% (23.6%) variation in VS-FeFinFET for PITC(NITC).

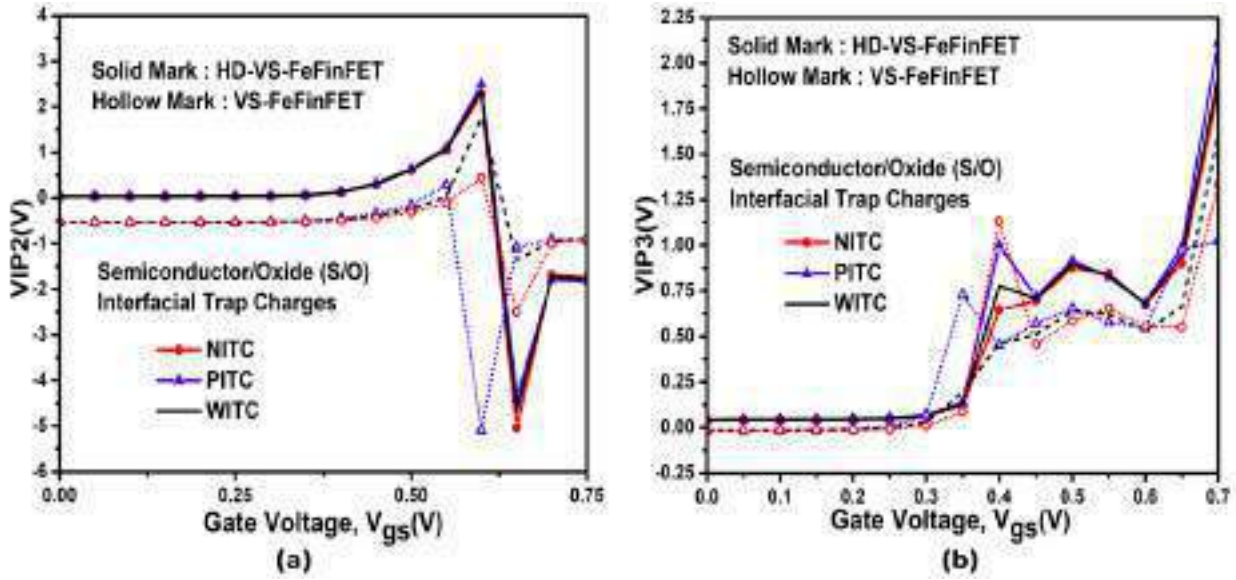

Figure 3.11: Effect of ITCs on voltage intercept point (a) VIP2 (b) VIP3 of HD-VS-FeFinFET and VS-FeFinFET at V_{ds}=0.4V (VC25b).

Voltage intercept point (VIP) is an important parameter used to describe the linearity of the device. VIP2 (VIP3) is the second (third) order voltage intercept point that depicts input voltage level at which the second (third) order harmonics equals the fundamental signal(PVMC24). Higher VIP2 and VIP3 indicates better linearity and reduced distortion. Figure 3.11(a) displays that along with higher value of VIP2, the influence of ITCs is negligible on HD-VS-FeFinFET due to hetero dielectric engineering, providing high quality interface along with minimized traps. The presence of PITC(NITC) increases (decreases) the amplitude of VIP2 by 5.31% (4.14%) in case of HD-VS-FeFinFET. However, for VS-FeFinFET, the decrement in VIP2 is 57.3% (297%) in presence of NITC(PITC) in terms of WITC. Similar pattern is noticed in case of VIP3, its peak increases (decreases) only by 2.1%(2.03%) in presence of PITC(NITC) with respect to WITC whereas PITC(NITC) varies the VIP3 by 2.15% (7.57%) in VS-FeFinFET as showcased in Figure 3.11(b).

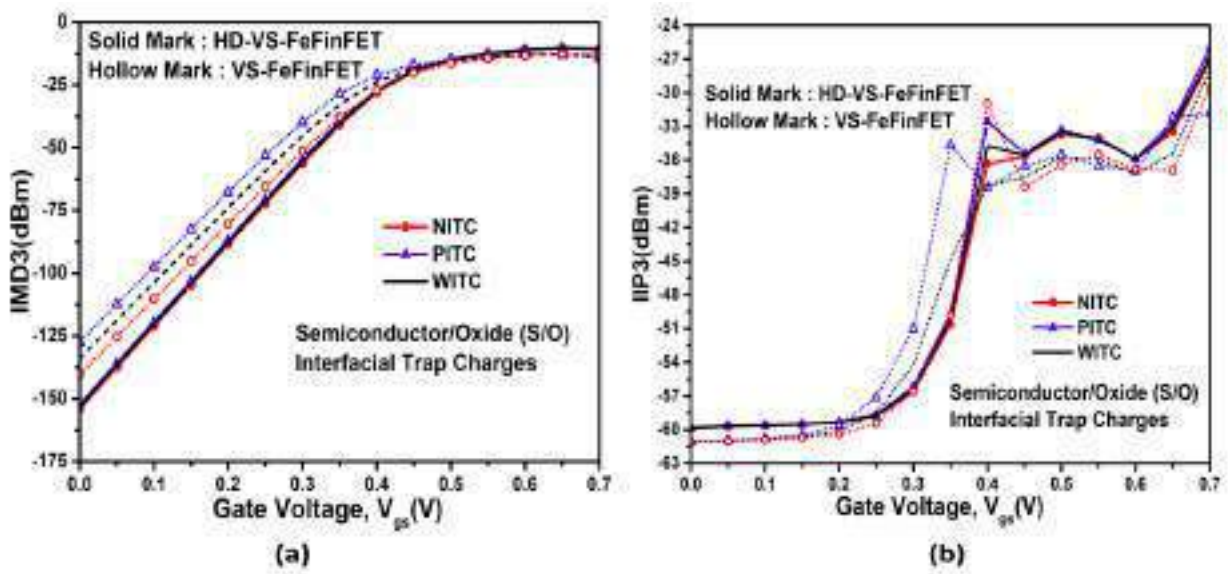

Figure 3.12: Impact of ITCs on (a) third order intermodulation distortion power (IMD3) (b) third order intercept input power (IIP3) of HD-VS-FeFinFET and VS-FeFinFET at V_{ds}=0.4V (VC25b).

Third order intermodulation distortion power (IMD3) and third order intercept input power (IIP3) are other critical parameters of linearity in wireless applications. IMD3 refers to the distortion caused by third-order non linearities when two signals mix, producing undesired spectral components near the fundamental frequencies(DMC22). For better linearity, minimum value of IMD3 is desired as depicted by HD-VS-FeFinFET in Figure 3.12(a). Further, the influence of ITCs on carrier mobility is less pronounced with high-k dielectrics which results in negligible influence on IMD3 in comparison to rise(fall) by 4.81% (4.89%) for PITC(NITC) in VS-FeFinFET. IIP3 is that extrapolated input power point where 1^{st} and 3^{rd} order harmonic power become equal. Higher IIP3 indicates better linearity(WS78). Figure 3.12(b) shows that higher value of IIP3 is shown by HD-VS-FeFinFET along with minimum variation, thus making it more reliable as compared to its counterpart. Furthermore, at low V_{gs}, IIP3 of HD-VS-FeFinFET is higher than the IMD3, which implies improved device power and performance by minimizing the hot carrier effect. On the other hand, at high V_{gs}, IIP3 of HD-VS-FeFinFET is lower than the IMD3, which is opposite to the trend at low V_{gs}. This occurs due to voltage-dependent non-linearities. Gate voltage significantly affects the channel's electrostatic potential, carrier mobility, and the non-linear terms in the device's transconductance. At low V_{gs}, the device operates in the subthreshold or near-threshold region, where second-order nonlinearities dominate due to weak inversion effects. These distortions influence IMD3 more strongly, making IIP3 appear relatively higher. On the other hand, at high

V_{gs}, the device is in strong inversion, where third-order nonlinearities become more prominent. This increases the impact on IIP3, reducing its relative value compared to IMD3(WS78; SKSG21).

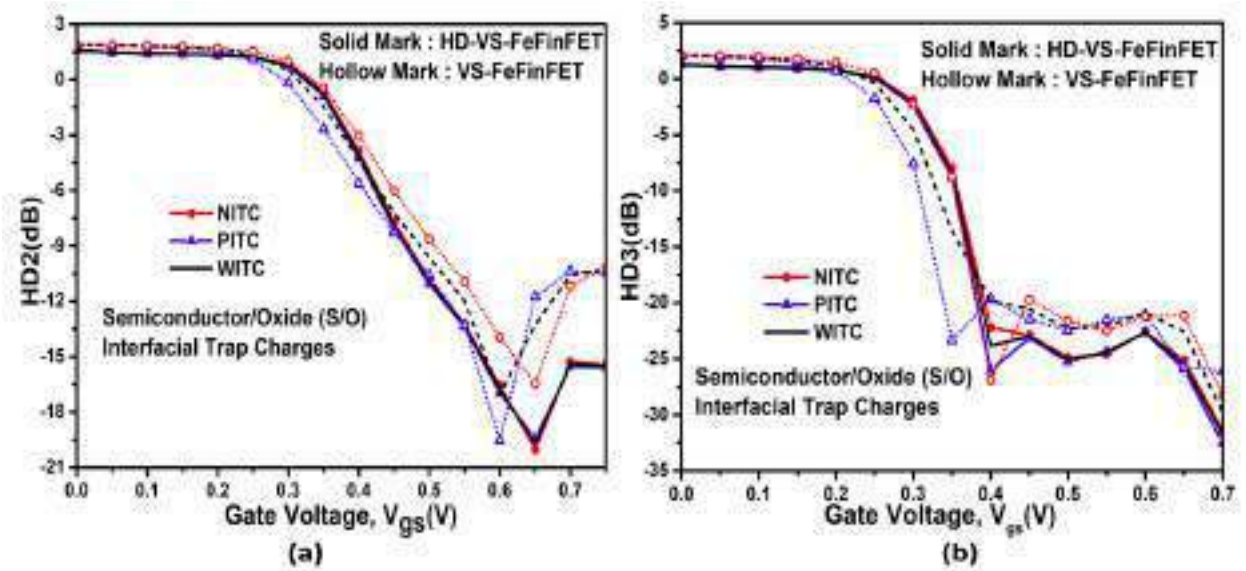

Figure 3.13: Effect of ITCs on harmonics distortion (a) HD2 and (b) HD3 for HD-VS-FeFinFET and VS-FeFinFET at V_{ds}=0.4V (VC25b).

To evaluate the intricacies of ITCs on the harmonics distortion characteristics, 2^{nd} order harmonics (HD2) and 3^{rd} order harmonics (HD3) of both the devices are analyzed in presence of ITCs with different polarity as given by Eq. 3.3 and 3.4 respectively where amplitude of V_a is taken as 50mV. HD2 (HD3) measures of the second (third) order nonlinearities producing signals at twice (thrice) the input frequency(SKSG21).

$$HD2 = \frac{1}{2} V_{\mathrm{a}} \frac{(\partial g_{\mathrm{m}} / \partial V_{\mathrm{gs}})}{2 g_{\mathrm{m}}} \tag{3.3}$$

$$HD3 = \frac{1}{4} {V_{\mathrm{a}}}^2 \frac{(\partial^2 g_{\mathrm{m}} / \partial {V_{\mathrm{gs}}}^2)}{6 g_{\mathrm{m}}} \tag{3.4}$$

Figure 3.13(a) and Figure 3.13(b) respectively displays the impact of ITCs on HD2 and HD3 with change in V_{gs} and it is found that HD-VS-FeFinFET shows negligible variations due to ITCs as compared to increment(decrement) in harmonic distortions with rise in V_{gs} for VS-FeFinFET due to PITC(NITC). High-k materials tend to reduce the density of interface traps as compared to conventional dielectrics due to reduced dangling bonds at the interface. This reduction minimizes

charge-trapping and de-trapping, leading to lower variations in harmonic distortions caused by PITC or NITC. Also, the high-k dielectric in HD-VS-FeFinFETs increases the gate capacitance, strengthening the gate's control over the channel potential. As a result, the channel becomes less sensitive to perturbations caused by ITCs. Thus, HD-VS-FeFinFET is proved to be more immune against any nonlinearity and distortion that arise from ITCs.

3.4.3 Circuit Level Analysis

To analyze the impact of ITCs of different polarity on HD-VS-FeFinFET based CMOS inverter, a required setup is designed on Cogenda Visual TCAD simulator with n-channel and p-channel HD-VS-FeFinFET isolated electrically with the help of 60nm SiO_2 spacer and later its performance has been compared with VS-FeFinFET based CMOS inverter. Figure 3.14(a) shows the schematic of the CMOS inverter circuit where V_{dd}, V_{out} and V_{in} are the supply voltage, output voltage, and input voltage respectively. Initially threshold matching of the n-channel and p-channel configuration is done for both the devices as displayed in Figure 3.14(b) in presence of different ITCs. The V_{gs} is varied from -0.85 to 0.85V with dual work function metal (DWFM) integration scheme.

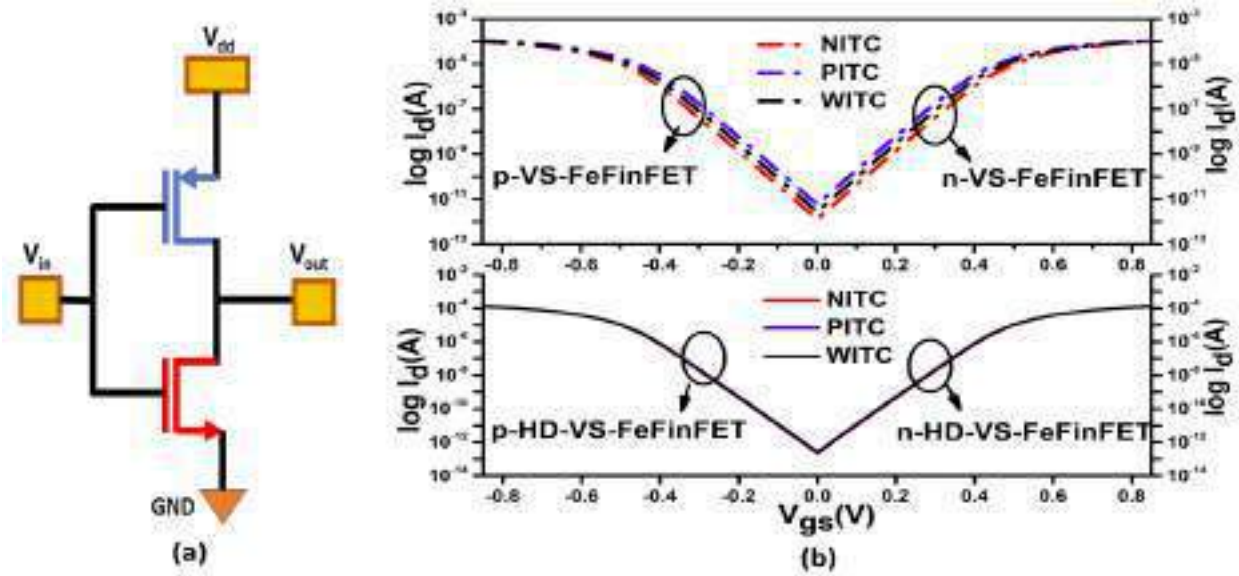

Figure 3.14: (a) Schematic diagram of CMOS Inverter (b) threshold voltage matching curve for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs (VC25b).

It is very much required to examine the crucial parameters to estimate the performance of inverter and for this, voltage transfer characteristics (VTC) for both the inverters in presence of ITCs of different polarity is analyzed as shown in Figure 3.15. It is visible that the transition range

(TR) of HD-VS-FeFinFET based inverter is more sharper than the VS-FeFinFET based inverter due to improved electrostatic control and reduced SCEs of HD-VS-FeFinFET device, which ensures high speed switching(KNSVS23; PGP^{+}20b). Further, the switching threshold voltage (V_{TH}) or the transition voltage, at which V_{in}=V_{out} on the VTC curve, is examined and it is found to be 0.247V for HD-VS-FeFinFET with minimal variation due to ITC's polarity as compared to 0.238V for VS-FeFinFET in case of WITC. It indicates enhanced noise immunity and stability in HD-VS-FeFinFET based inverter as require stronger input signals for logic transition.

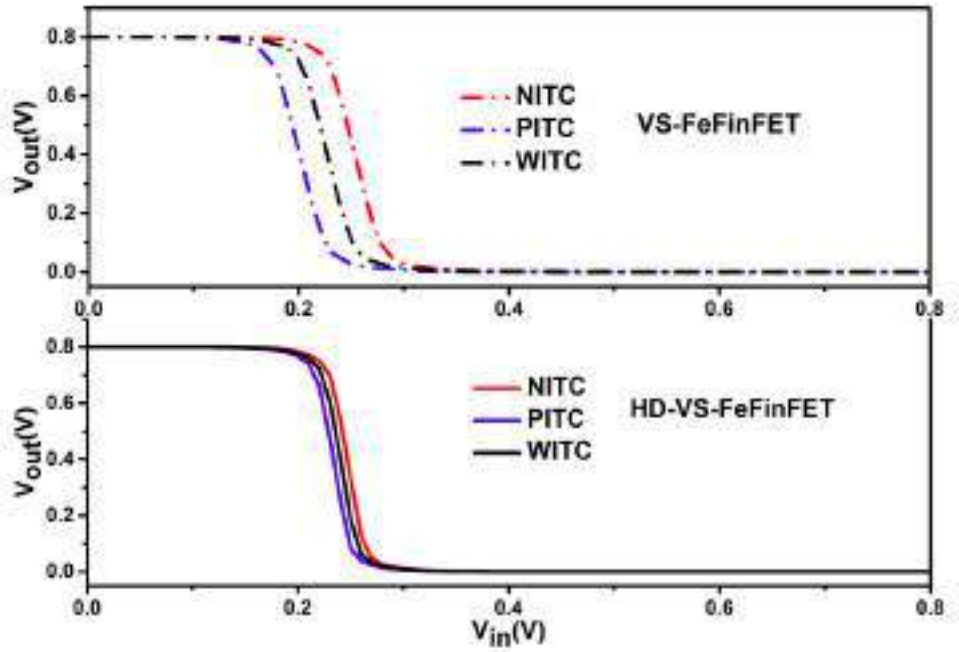

Figure 3.15: Effect of ITCs on voltage transfer characteristics of HD-VS-FeFinFET and VS-FeFinFET based inverter (VC25b).

Table 3.2: Performance Comparison between HD-VS-FeFinFET and VS-FeFinFET based inverter under the influence of ITCs with different polarity

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
V_{IL} (mV)	143.473	169.841	196.792	183.994	191.341	198.031
V_{IH} (mV)	270.794	285.762	297.713	267.452	274.142	280.174
V_{OL} (mV)	5.77×10^{-8}	1.39×10^{-7}	3.41×10^{-7}	3.60×10^{-8}	4.58×10^{-8}	3.35×10^{-8}
V_{OH} (mV)	799.99	800	800	800	800	800
NM_L (mV)	1.43×10^{2}	1.70×10^{2}	1.97×10^{2}	1.84×10^{2}	1.91×10^{2}	1.98×10^{2}
NM_H (mV)	529.196	514.238	502.287	532.548	525.858	519.826
TR (mV)	102.321	100.921	100.921	83.458	82.801	82.143

ITCs can generate additional spurious signals that can interfere with the proper functioning of the inverter. Noise Margin (NM) is a crucial parameter to depict the noise immunity of the circuit and its value should be higher for better tolerance to undesirable variations with more reliable operation. The noise margin for low signal levels (NM_L) and the noise margin for high signal levels (NM_H) is defined by Eq. 3.5 and 3.6. Here, V_{OL} and V_{OH} are minimum and maximum output voltage when corresponding output levels are logic 0 and logic 1 respectively. V_{IL} and V_{IH} are maximum and minimum input voltage which can be interpreted as logic 0 and logic 1 respectively(SNP$^+$24). As shown in Table 3.2, it is found that with higher NM due to sharper switching characteristics along with negligible deviation under the influence of ITCs, HD-VS-FeFinFET is more reliable for digital circuits and applications.

$$NM_{\mathrm{L}} = V_{\mathrm{IL}} - V_{\mathrm{OL}} \tag{3.5}$$

$$NM_{\mathrm{H}} = V_{\mathrm{OH}} - V_{\mathrm{IH}} \tag{3.6}$$

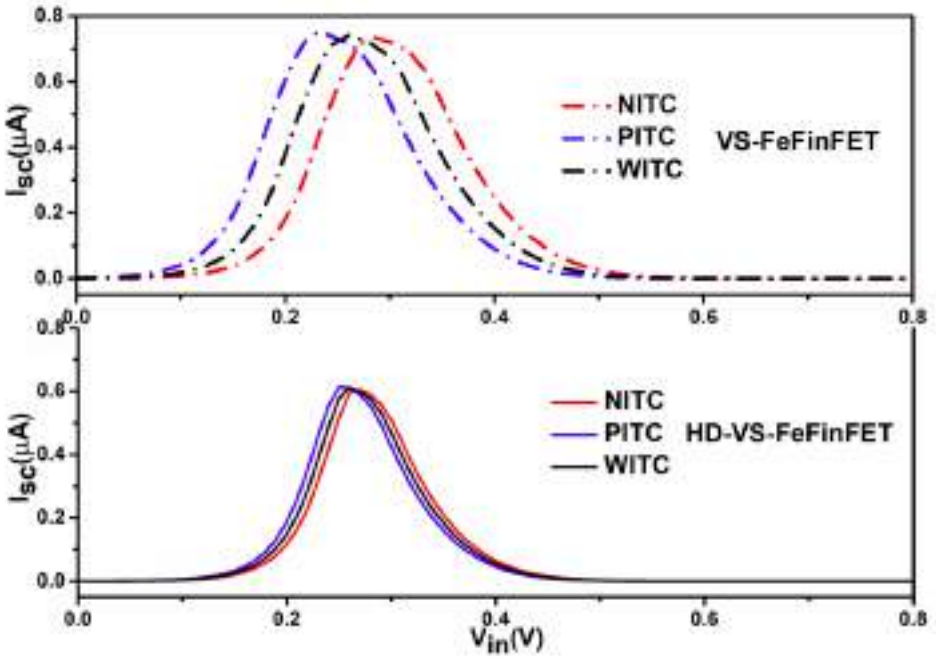

Figure 3.16: Effect of ITCs on switching current of HD-VS-FeFinFET and VS-FeFinFET based inverter (VC25b).

Figure 3.16 displays the switching current (I_{sc}) of both the logic circuits in presence of different

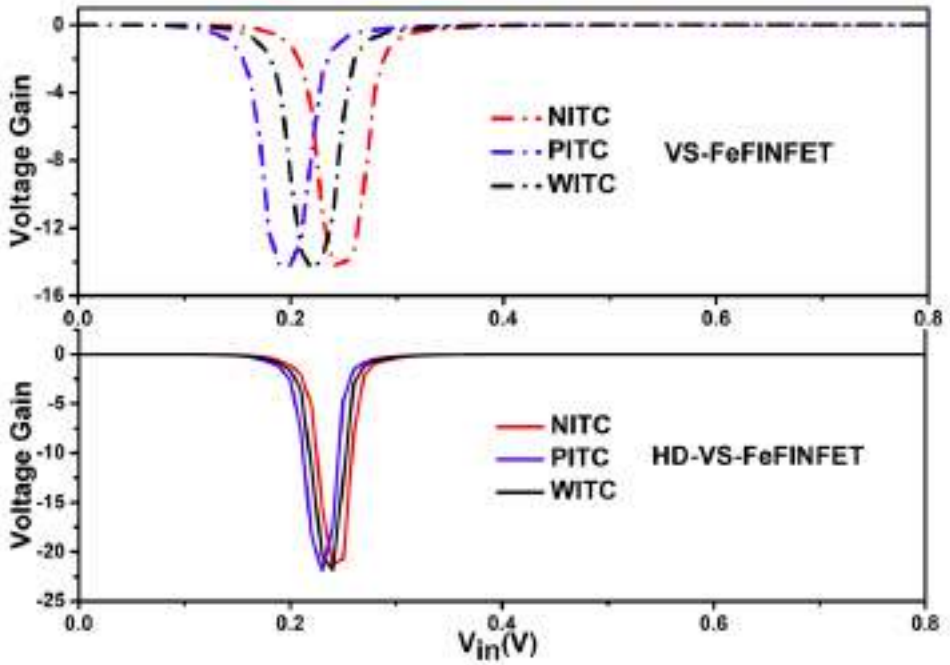

Figure 3.17: Impact of ITCs polarity on voltage gain of HD-VS-FeFinFET and VS-FeFinFET based inverter. (VC25b).

ITCs. The static current (at V_{in} = 0V, V_{in} = V_{dd}) is less than 1 pA, confirming significantly lower static power dissipation and improved energy efficiency for HD-VS-FeFinFET along with negligible variations under the influence of ITCs with different polarity(KNSVS23). The effect of ITCs on inverter gain for both the devices is shown in Figure 3.17. An increase of 51.674% in gain due to higher g_m and R_{out} along with minimum deviations due to ITCs is observed in HD-VS-FeFinFET based inverter as compared to VS-FeFinFET based inverter thus proved to be more desirable in various applications where signal fidelity and amplification are crucial.

3.5 Summary

This chapter presented a comprehensive assessment from device to circuit level showing the influence of ITCs on various analog, linearity, and distortion parameters of strained hetero dielectric vertically stacked ferroelectric based FinFET (HD-VS-FeFinFET). The strained channel system and engineering modify the band structure and increase the carrier mobility thus improving the transistor's performance and making it more desirable for many electronic applications. The process improves the device performance in terms of various metrics such as I_{on}, I_{off}, V_{th}, g_m, VIP2, VIP3, IIP3, IMD3, 1-dB compression point, and harmonic distortion parameters. At the device

level, HD-VS-FeFinFET outperforms VS-FeFinFET with improvement in various analog parameters like A_v by 27 times, V_{EA} by 7.5 times, and R_{out} by 23 times along with minimal average variations of 11.15%, 3.03% and 11.39% respectively in contrast to 45.73%, 14.24% and 42.48% for VS-FeFinFET under the influence of ITCs. Thus, the heterogeneous dielectric engineering approach effectively strengthens device immunity against ITCs, leading to enhanced performance and reliability for advanced nanoelectronic applications. Further, circuit level comparison has also been made for CMOS inverter and it is found that HD-VS-FeFinFET based inverter offers improved performance in terms of noise margin, I_{sc}, and transition range along with more tolerance against ITCs. With the comprehensive analysis done on the intricacies of ITCs from device to circuit level, this work provides insights into the development of HD-VS-FeFinFET with enhanced functionality, reliability, and performance, poised to shape the landscape of modern electronics.

In conclusion, this study established the inevitability of interfacial trap charges (ITCs) arising from dangling bonds at the semiconductor surface and demonstrated how gate engineering through hetero dielectric stacking in HD-VS-FeFinFETs effectively suppresses ITC-induced degradations to achieve superior device and circuit performance. While this chapter focused on mitigating ITC effects through device-level engineering, it is equally important to recognize that the influence of ITCs is not constant but strongly dependent on operating conditions. Their occupancy and activity vary with temperature due to changes in carrier emission and capture rates, while their impact on device characteristics further depends on density and polarity. Hence, the next chapter extends the analysis by investigating the coupled effects of temperature and ITC density/polarity, thereby providing a more realistic evaluation of HD-VS-FeFinFET reliability under practical operating conditions. Such an evaluation not only deepens the understanding of device response under practical stress conditions but also provides valuable insights for optimizing design strategies, improving thermal robustness, and ensuring long-term reliability in real-world applications such as low-power and high-performance nanoelectronics.

Chapter 4

Reliability Analysis of Hetero Dielectric Vertically Stacked FeFinFET under Coupled Thermal and Trap Dynamics with its Applicability as CMOS Inverter

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* This chapter provides an in-depth analysis of the coupled influence of temperature and interfacial trap charges (ITCs) density, considering the dynamic response of ITCs over a broad thermal range and different charge concentrations. The study highlights their impact on the performance of the hetero dielectric vertically stacked FeFinFET (HD-VS-FeFinFET) device, thereby reinforcing its potential for CMOS inverter applications.

* Temperature affectability reveals that HD-VS-FeFinFET exhibits better reliability with less average variations against ITCs at all operating temperatures such as 10.65% in leakage current (I_{off}) and 11.39% in output resistance (R_{out}) at 300K which further decreases to 8.13% in I_{off} and 7.76% in R_{out} at 400K in contrast to huge variation shown by VS-FeFinFET like 82.05% in I_{off} and 43.10% in R_{out} at 300K along with 59.35% in I_{off} and 29.86% in R_{out} at 400K.

* Further, the analysis done at various ITCs densities and polarities reveals that, at higher donor trap charge density of 10^{13} cm^{-2}, the device performance alters significantly for VS-FeFinFET with degradation in I_{off} by 552 times in comparison to HD-VS-FeFinFET which degrades only by 2.52 times, thus making it more reliable under varying environmental conditions.

* Subsequently, HD-VS-FeFinFET based CMOS inverter demonstrates high reliability and robustness under combined effects of temperature variation and ITCs. Simulation results reveal only a moderate shift of 34.6 mV in switching threshold voltage and 6.8% reduction in noise margin when temperature rises from 300 K to 400 K along with improved immunity towards ITCs with negligible variations at all operating temperatures, thus making it a reliable choice for digital circuits, particularly in thermally varying and power-critical applications.

* Comprehensively, by shedding light on the coupled effects of temperature and ITCs studied with different polarity/density, this work paves the way for the development of HD-VS-FeFinFET as a more reliable, efficient, and adaptable device to the increasingly demanding and dynamic environments of the future.

4.1 Introduction

The investigations carried out in Chapter 3 clearly establish that the proposed HD-VS-FeFinFET exhibits remarkable improvements in device and circuit performance under the influence of interfacial trap charges (ITCs). By employing heterogeneous dielectric gate engineering and strained channel design, significant enhancement was observed in crucial analog, linearity and distortion parameters along with reduced variations under the influence of ITCs. Moreover, circuit-level evaluation with a CMOS inverter confirmed that HD-VS-FeFinFETs not only outperform conventional VS-FeFinFETs but also demonstrate higher tolerance to ITC-induced degradations. These outcomes highlight the potential of HD-VS-FeFinFETs as a reliable and high-performance device solution for future nanoelectronic applications.

Despite these encouraging outcomes, the analysis in Chapter 3 was limited to nominal operating conditions and assumed ITCs to be static. In reality, ITCs exhibit temperature-sensitive dynamics due to thermally activated carrier capture and emission processes(NB02; Fle13). Additionally, ITC's density and polarity strongly affect device reliability, leading to threshold voltage shifts, variations in transconductance, and distortions in device performance (RJKB23). Therefore, a realistic evaluation of device robustness requires an in-depth investigation of ITCs under different temperatures, densities, and polarities—dimensions that were not addressed in Chapter 3.

The influence of ITCs is inherently temperature-dependent because their occupancy is governed by thermally activated capture and emission of carriers. (PCT$^+$15; KFW$^+$16) showed that traps within the bandgap exchange carriers with the channel over an energy window proportional to k_BT. As the temperature increases, both the capture and emission rates rise, modifying trap occupancy and thereby impacting threshold voltage, subthreshold swing and transconductance. (Vel16) further demonstrated that radiation or process-induced traps in MOS devices exhibit strong temperature sensitivity, producing noticeable shifts in device parameters across varying thermal conditions.

Modern reliability studies emphasize that temperature plays a central role in bias temperature instability (BTI). In particular, negative-bias temperature instability (NBTI) in p-MOSFETs is aggravated at elevated temperatures, as higher thermal energy accelerates Si–H bond breaking and trap generation (MKA04; BRH$^+$13). Recovery processes are also temperature-dependent, governed

by thermally activated detrapping. These findings underline that ITCs cannot be evaluated meaningfully at a single temperature, instead, they require systematic analysis across a range of thermal conditions. This forms one of the primary motivations of Chapter 4.

Till now, mainly the device performance has been investigated for various novel device architectures and engineering of FeFinFET to enhance the performance, but to ensure the device reliability and applicability over dynamic environments, the temperature affectability as well as impact of ITCs needs to be analyzed. Moreover, it has been reported that the reliability of the device is more prominent problem due to limited adaptability of the devices in environmental variations(CBV$^+$23; GPGK21).

Also, the on-chip performance of the device is always subject to operating temperatures. The chip's working temperature rises dramatically as a result of the increased number of transistors, which enhanced the heat dissipation(LHW$^+$17; Kha17). Furthermore, because the characteristics of semiconductors are temperature-dependent, it is necessary to examine the impact of temperature to ensure the stability of the device at various operating temperatures. Therefore, understanding and mitigating the combined effects of temperature and ITCs on the device performance is not only crucial for current applications but also paves the way for the development of next-generation semiconductor devices that are more resilient, efficient, and adaptable towards dynamic environments.

Also, the effect of ITCs is also strongly determined by their density and charge polarity. A higher density of traps increases the likelihood of carrier scattering, leading to degraded mobility and transconductance, while also inducing significant threshold voltage shifts(LHW$^+$17; MC17). (SA14) reported that the density of generated traps directly correlates with the severity of BTI-related degradation, while (Cou18; Buk11) demonstrated that fluctuations in trap density contribute to device-to-device variability in nanoscale devices.

Polarity introduces another dimension of complexity, as positive and negative ITCs shift device parameters in opposite directions. Positive interface trap charges (PITCs) typically lower V_{th} in n-FETs, increasing leakage currents whereas negative interface trap charges (NITCs) push V_{th} upward, reducing drive current. These shifts directly impact the device performance. For ferroelectric-based FETs, polarity effects are particularly significant, as trap-assisted asymmetries

can couple with polarization switching and amplify device variability(Cou18; Buk11). These insights highlight the need for a detailed evaluation of trap density and polarity effects, a focus of Chapter 4.

So, building upon the insights of Chapter 3, which demonstrated the superiority of the HD-VS-FeFinFET in mitigating the influence of ITCs under nominal conditions, this chapter advances the analysis toward realistic and varying operating scenarios. In practical applications, semiconductor devices are seldom exposed to constant environments; instead, they encounter temperature variations, fluctuating bias conditions, and different trap densities and polarities that jointly determine long-term reliability and performance stability. Since ITCs exhibit temperature-sensitive carrier capture and emission dynamics, along with polarity- and density-dependent modulation of threshold voltage and mobility, their impact cannot be captured adequately by static room-temperature analysis alone.

Therefore, this chapter systematically investigates the coupled effects of temperature, ITC density, and ITC polarity on the performance of HD-VS-FeFinFETs. The focus is on evaluating variations in threshold voltage, transconductance, and other analog figures-of-merits. By benchmarking against conventional VS-FeFinFETs, the study further highlights the robustness of the heterogeneous dielectric engineering approach. Through this extended reliability-oriented assessment, Chapter 4 provides a more holistic understanding of ITC-induced variability, thereby reinforcing the practical viability of HD-VS-FeFinFETs for future technology nodes.

So, the main aim of this chapter is to investigate the reliability of HD-VS-FeFinFET with extensive analysis from device to circuit level under the combined influence of operating temperature and ITCs. This is done by analyzing the influence of PITCs and NITCs on various static and analog performance parameters of HD-VS-FeFinFET and compared to VS-FeFinFET at different operating temperatures. This gives the insights about how the various figures of merit of both the devices will be affected due to combined effect of temperature and ITCs. Further, the reliability of the both devices with a fair comparison is also explored in terms of variation in several device characteristics at different densities along with different polarities of ITCs. Later, the work is extended to discuss the reliability at the circuit level by analysing the performance of HD-VS-FeFinFET based CMOS inverter under the influence of ITCs at various operating temperatures and examined its capability

to work under varying environmental conditions. Thus, the chapter bridges both device-level physics and circuit-level implications, providing a holistic view of reliability across operational scenarios.

This chapter is organized as follows: Section 4.2 includes all the specifications regarding the device structure. The simulation framework mentioning the physical models used for the device are discussed in section 4.3. Section 4.4 provides the results and discussion for the affectability of temperature and ITCs density/polarity on performance at the device and circuit level. Section 4.5 provides a complete summary of the chapter.

4.2 Device Structure

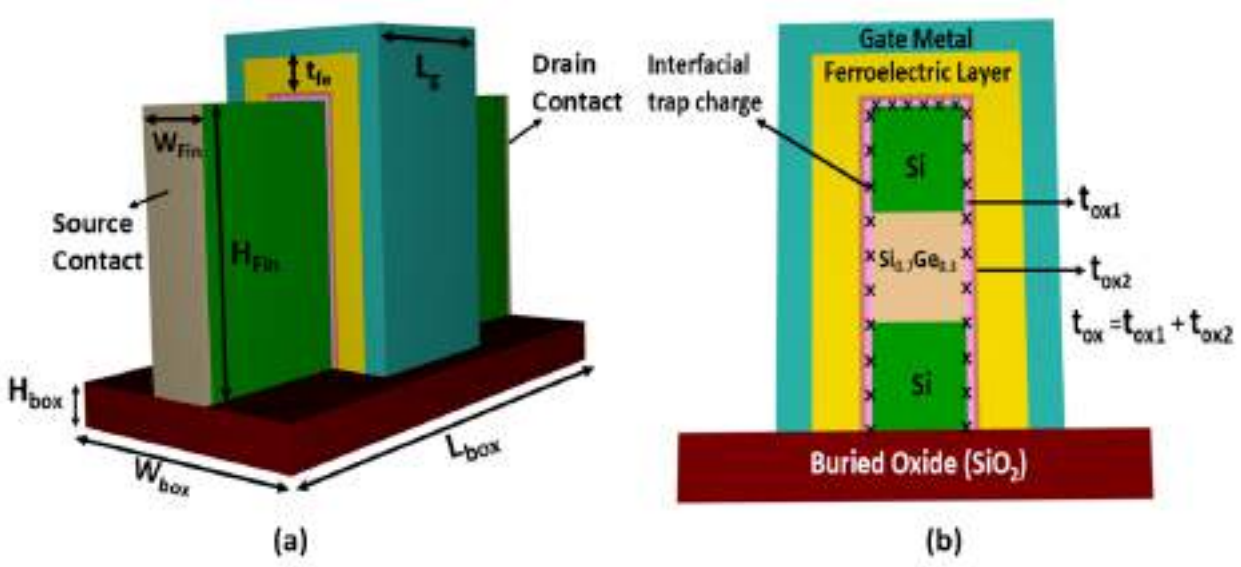

Figure 4.1: (a) 3D schematic view of HD-VS-FeFinFET (b) inset of vertical cross-sectional view of HD-VS-FeFinFET (VC25a).

Figure 4.1(a) displays the three-dimensional structure of HD-VS-FeFinFET, while Figure 4.1(b) shows its vertical 2-dimensional view chopped through the fin. The device is designed with a fixed gate length of 20 nm, while the ferroelectric layer thickness is maintained at 6 nm, combined with a total gate oxide thickness of 1 nm. Silicon-doped hafnium oxide (HfO_2-FE) is taken as the ferroelectric material. The total gate oxide (t_{ox}) is composed of a heterogeneous dielectric stack consisting of equal proportion of Al_2O_3 (t_{ox1}) and HfO_2 (t_{ox2}), each with a thickness of 0.5nm. The height and width of the fin are taken as 30nm and 8 nm respectively. A tri-layered strained-silicon channel system is formed with the help of SiGe sandwiched between two silicon layers as Si-$Si_{0.7}Ge_{0.3}$-Si

(where $Si_{0.7}Ge_{0.3}$ represents that the mole fraction of Si and Ge is taken as 0.7 and 0.3 respectively). The doping concentration of source/drain is fixed as 1×10^{20} cm^{-3} with n-type and that of channel is 1×10^{16} cm^{-3} with p-type.

Table 4.1: Device specifications

Parameters	Dimension
Gate length (L_g)	20nm
Drain/Source ($L_{d/s}$)	20nm
Channel material	Si-$Si_{0.7}Ge_{0.3}$-Si
Oxide thickness (t_{ox})	1nm
Ferroelectric thickness (t_{fe})	6nm
Background dielectric constant of Ferroelectric layer	27
Landau coefficient (α)	-1.23×10^{11} cm/F
Landau coefficient (β)	3.28×10^{20} cm^5/FC^2
Landau coefficient (γ)	0.0 cm^9/FC^4
Dipole interaction coefficient (g)	1×10^{-4} cm^3/F
Viscosity coefficient (ρ)	2.25×10^4 Ωcm
Width of fin (W_{Fin})	8nm
Height of fin (H_{Fin})	30nm
Height of box (H_{box})	5nm
Width of box (W_{box})	32nm
Length of box (L_{box})	62nm
Interfacial trap charge density	1×10^{11} (cm^{-2}) to 1×10^{13} (cm^{-2})
Doping concentration of drain/source ($N_{d/s}$)	1×10^{20} (cm^{-3})
Doping concentration of channel (N_{ch})	1×10^{16} (cm^{-3})
Gate work function (ϕ)	4.65eV

The length of the source/drain regions is fixed at 20nm. In addition, a metal gate with a work function of 4.65 eV, which has excellent thermal stability and is compatible with CMOS processing, is utilized in this device to prevent any poly-depletion effect that is common in polysilicon gates(Rao20; MC24). Further, to exploit the advantages of SOI technology such as improved subthreshold characteristics, suppressed threshold voltage (V_{th}) variations, and minimum parasitic capacitances in the considered structure, the entire heterostructure FeFinFET is built on an insulator SiO_2 box whose width, height, and length are kept 32nm, 5nm, and 62nm respectively. Also, to unveil the intricacies of ITCs on the device reliability and performance, ITCs with different polarity have been introduced at the semiconductor-oxide interface with trap charge density as 10^{11} cm^{-2} -

10^{13} cm^{-2} based on formerly reported literature(QWHH14b; PGP+20b; DMC22; CS23b). All the device specifications are also mentioned in Table 4.1.

4.3 Simulation Framework and Physical Models

All the simulations have been carried out using Cogenda's Genius 3D TCAD simulator. The simulation setup includes the drift-diffusion model level 1 (DDML1) which maintains the lattice temperature constant throughout the solving procedure, coupled with consistent Poisson's equation as given by Eq. 4.1(VC24b), and continuity equations to govern the carrier transport phenomena for the electrons and the holes as given by Eq. 4.2 and 4.3 respectively(VC24b),

$$\nabla.\epsilon\nabla\psi = -q(p - n + N_{\mathrm{D}}{}^{+} - N_{\mathrm{A}}{}^{-}) \tag{4.1}$$

$$\frac{\partial n}{\partial t} = \nabla.(\mu_{\mathrm{n}} n\vec{E_{\mathrm{n}}} + \mu_{\mathrm{n}}\frac{k_{\mathrm{b}}T}{q}\nabla n - (U - G) \tag{4.2}$$

$$\frac{\partial p}{\partial t} = -\nabla.(\mu_{\mathrm{p}} p\vec{E_{\mathrm{p}}} + \mu_{\mathrm{p}}\frac{k_{\mathrm{b}}T}{q}\nabla p - (U - G) \tag{4.3}$$

where ψ is the electrostatic potential of the vacuum level, ϵ is the permittivity of material, $N_D{}^+$ and $N_A{}^-$ are the ionized impurity concentrations, n and p are the concentration for electron and hole respectively, q is the electroic charge, μ_n and μ_p are mobilities of electrons and holes, E_n and E_p are the effective driving electrical field for electrons and holes, U and G are the recombination and generation rates considered for both electrons and holes.

The temperature and doping-dependent recombination-generation phenomenon for carriers are accurately captured by Shockley-Read-Hall (SRH) recombination and Auger models(VC24b). Further, Philips mobility model for SiGe and Lombardi mobility model for silicon are used to consider the mobility degradation at the semiconductor-oxide interface(VC23; VKV24). Lucent model is used to take into account the high-field mobility effects along with hot carrier models for capturing the effect of hot carriers. To check the velocity saturation and mobility of carriers, the

velocity saturation model along with Esurface models are activated. The density gradient method is also used to incorporate quantum confinement phenomena along with the Fermi-Dirac carrier statistics model(PVMC24). The physics of ferroelectric layer is modeled with the time-dependent Landau–Khalatnikov (LK) equation for relating electric field used for the ferroelectric layer (E_{FE}) as a function of ploarization (P), which is given by Eq. 4.4(PGP$^+$20a),

$$E_{\mathrm{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho(\frac{\partial P}{\partial t}) \tag{4.4}$$

where α, β, and γ are the static Landau FE material-dependent coefficients taken as -1.23×10^{11} cm/F, 3.28×10^{20} cm^5/FC^2, 0.0 cm^9/FC^4 while g as dipole interaction coefficient and ρ as viscosity coefficient are taken as 1×10^{-4} cm^3/F and 2.25×10^4 Ωcm respectively(VC24b). Further, the position and polarity of ITCs in the device are mentioned using the INTERFACE statement along with trap models to capture the associated phenomena(ZLX$^+$24)(VC25b). A few abbreviations are used in this paper such as PITC - positive (donor) interfacial trap charge, NITC - negative (acceptor) interfacial trap charge, WITC - without (neutral) interfacial trap charge.

4.4 Result and Discussion

4.4.1 Impact of ITCs and Temperature Affectability

This subsection discusses the temperature affectability on both the devices under the influence of ITCs to analyse the reliability through various static and analog metrics. ITCs with different polarity have been introduced at the semiconductor-oxide interface with trap charge density fixed at 10^{12} cm^{-2} in this section. Figure 4.2(a) and Figure 4.2(b) shows the transfer characteristics of both the devices (HD-VS-FeFinFET and VS-FeFinFET) at various operating temperatures. Characteristics of FET devices changes with change in temperature. As temperature increases, the carrier mobility decreases as given by Eq. 4.5(KTC18; KB16),

$$\mu(T) = \mu(T_0)(\frac{T}{T_0})^{\text{-n}} \tag{4.5}$$

where $\mu(T_0)$ is carrier mobility at room temperature, $\mu(T)$ is carrier mobility at temperature T, n is the mobility temperature exponent, T_0 is room temperature.

It can be observed from Figure 4.2(a) and 4.2(b) respectively that HD-VS-FeFinFET showcases more driving current (I_{on}) and less leakage current (I_{off}) at various operating temperatures in comparison to VS-FeFinFET. Also, both I_{on} and I_{off} are degrading with increasing temperature for both the devices due to decreasing mobility as related by Eq. 4.5.

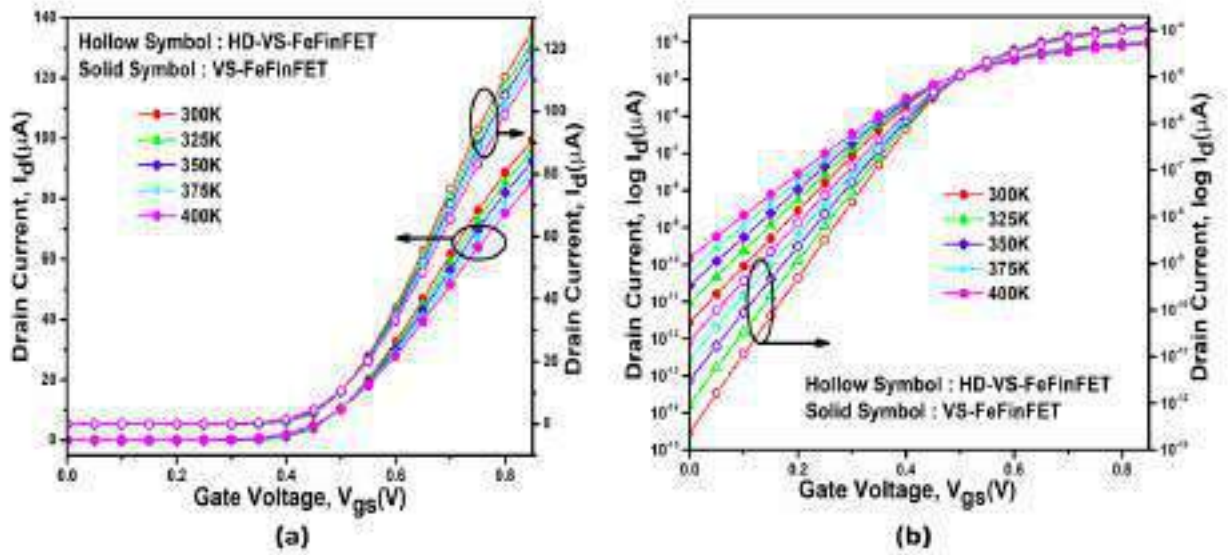

Figure 4.2: Impact of temperature on transfer characteristics of HD-VS-FeFinFET and VS-FeFinFET in (a) linear and (b) log scale (VC25a).

Further, the presence of ITCs leads to altercation in flat band voltage (V_{fb}) as given by Eq. 4.6(Chi11), where q is the electronic charge, N_{it} is the ITCs density and C_{ox} is gate oxide capacitance.

$$V_{\mathrm{fb}} = \frac{qN_{\mathrm{it}}}{C_{\mathrm{ox}}} \tag{4.6}$$

$$V_{\mathrm{th}} = V_{\mathrm{fb}} + \psi_{\mathrm{fp}} + \frac{qN_{\mathrm{a}}x_{\mathrm{t}}}{C_{\mathrm{ox}}} \tag{4.7}$$

The changes in V_{fb} caused by PITC/NITC leads to modification in threshold voltage (V_{th}) as related by Eq. 4.7(AYA23), where x_t is maximum space charge width, N_a is accumulated charge and ψ_{fp} is built in potential. This modification in V_{th} leads to change in device characteristics thus change the ON current (I_{on}) and leakage current (I_{off}) of the device(AYA23).

Figure 4.3 and Figure 4.4 respectively shows the impact of ITCs with different polarity on the transfer characteristics of HD-VS-FeFinFET and VS-FeFinFET at different operating temperatures

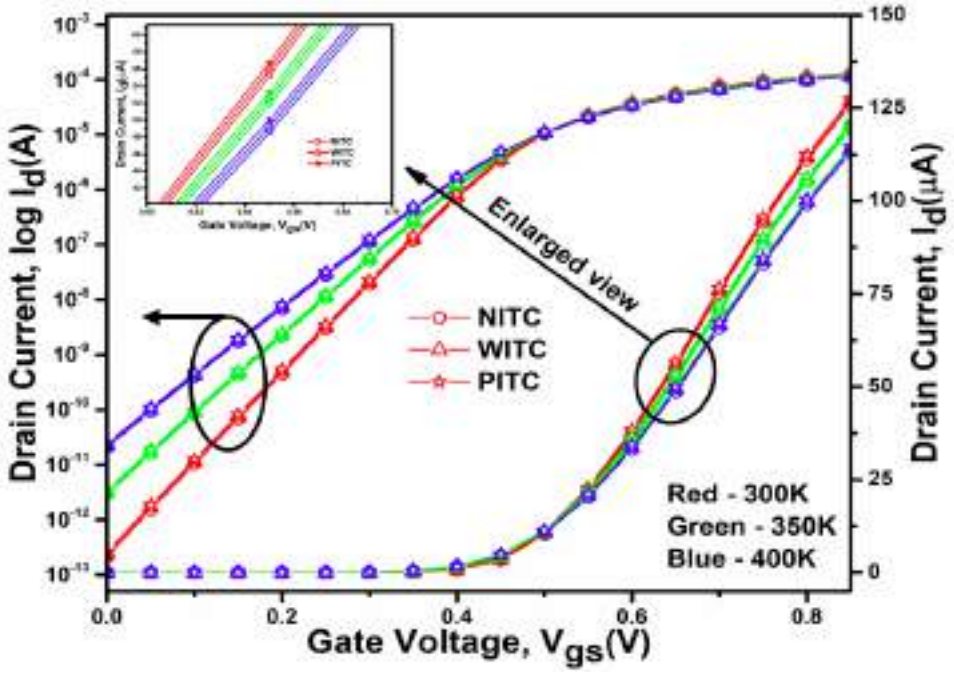

Figure 4.3: Impact of ITCs on transfer characteristics of HD-VS-FeFinFET under different operating temperatures (VC25a).

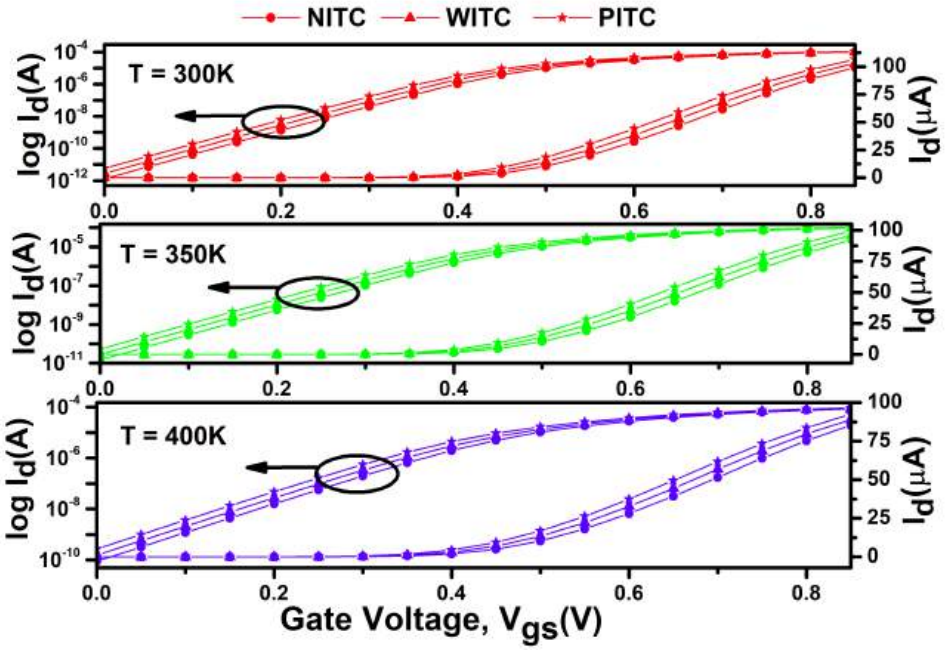

Figure 4.4: Impact of ITCs on transfer characteristics of VS-FeFinFET under different operating temperatures (VC25a).

in linear and log scale. It is inferred from the Figure 4.3 that the drain current of HD-VS-FeFinFET is minimally gets affected due to PITC and NITC with respect to WITC. The variation in I_{on} is 0.58% rise(0.61% fall) with increase(decrease) in leakage current by 11.2%(10.1%) in presence of PITC(NITC) at 300K. With the rise in temperature to 400K, there is only 0.62% rise(0.65% fall)

in I_{on} along with increment(decrement) in leakage current by 8.47%(7.8%) under the influence of PITC (NITC). With temperature rise, carrier mobility decreases, but ferroelectric polarization assists in maintaining electrostatic control. Hence, I_{on} variation increases only a little (less than 1%), showing robust ON-state conduction. Also, relative perturbation caused in leakage current by ITCs becomes smaller at higher temperature because thermally activated carriers dominate the subthreshold leakage behavior, making the impact of ITCs (PITC/NITC) relatively less significant. So, collectively, it can be inferred that the tolerance in the HD-VS-FeFinFET towards different ITCs is almost consistent with variation in temperature from 300K to 400K in contrast to VS-FeFinFET which displays large variations with rise(fall) in I_{on} by 3.35%(3.64%) along with increase(decrease) in leakage current by 111%(53.1%) at 300K and rise(fall) of 3.88%(4.22%) in I_{on} along with increment(decrement) in leakage current by 75.2%(43.5%) at 400K in presence of PITC(NITC) as showcased in Figure 4.4, thus confirms HD-VS-FeFinFET to be more reliable in presence of ITCs even with increasing temperature.

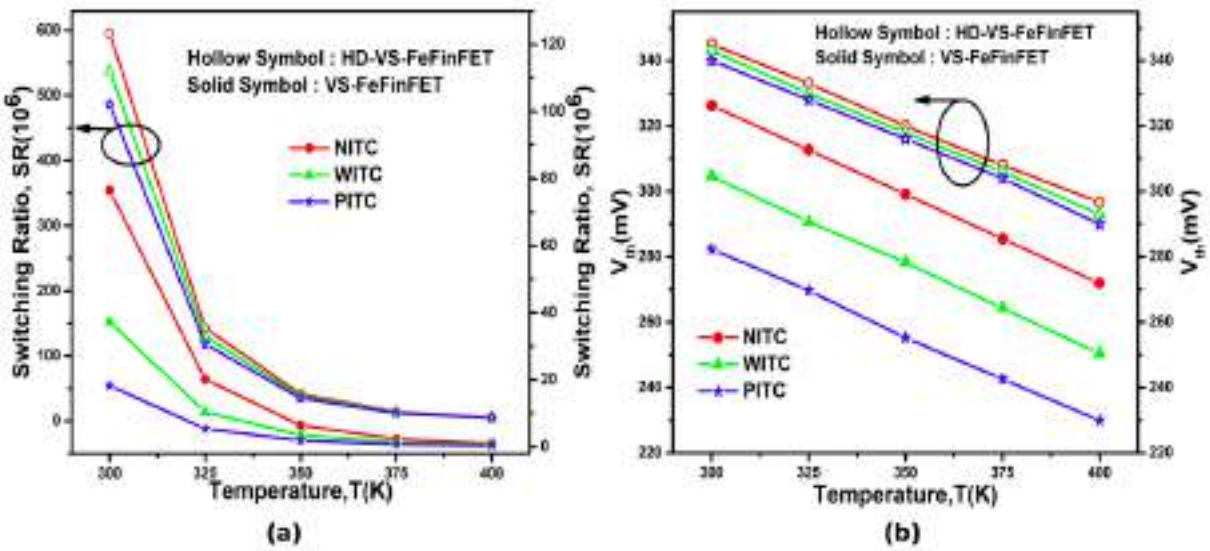

Figure 4.5: Variation in (a) switching ratio and (b) threshold voltage of both the devices under the influence of ITCs at different operating temperatures (VC25a).

Figure 4.5(a) and Figure 4.5(b) respectively displays the variation of switching ratio (SR) and threshold voltage (V_{th}) of both the devices under the influence of ITCs of different polarities at various range of temperature. Figure 4.5(a) shows that HD-VS-FeFinFET exhibits higher SR with minimal deviations under the influence of ITCs in comparison to VS-FeFinFET. It also showcases that although there is decrease in SR with rise in temperature from 300K to 400K for both the devices but the variations due to ITCs also gets suppressed with increasing temperature thus

favoring the switching performance of the device. Further, the enhanced(reduced) effective gate voltage i.e. (V_{gs}-V_{fb}) due to presence of PITC(NITC) results in decrease(increase) in V_{th} of both the devices. Also the V_{th} is inversely proportional to temperature that led to its decrement by 14.57%(17.8%) for HD-VS-FeFinFET(VS-FeFinFET) with increase in temperature from 300K to 400K as displayed in Figure 4.5(b).

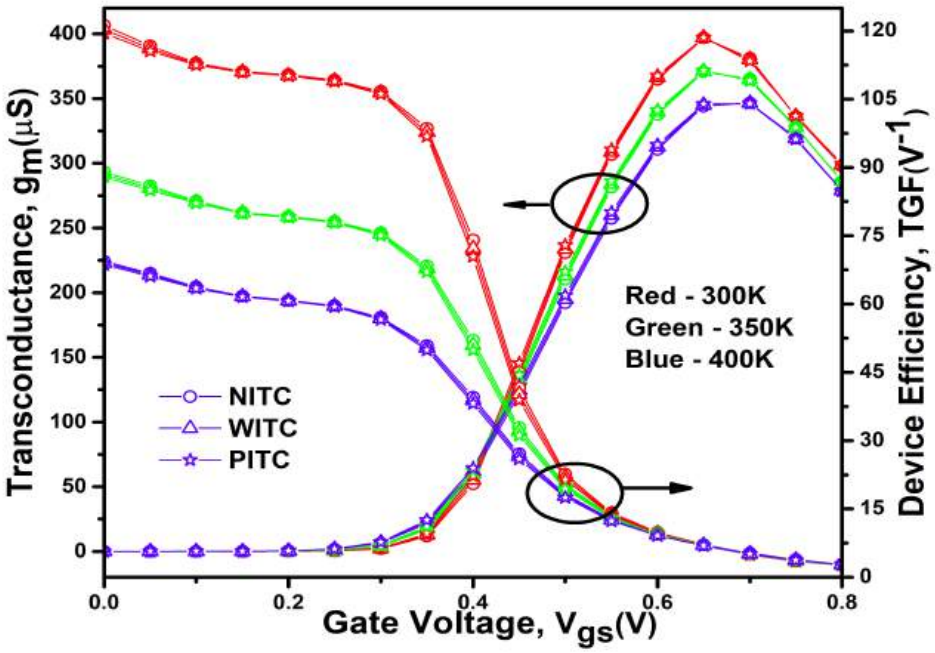

Figure 4.6: Impact of ITCs on transconductance and device efficiency of HD-VS-FeFinFET at different operating temperatures (VC25a).

Figure 4.6 and Figure 4.7 respectively shows the variation of transconductance (g_m) and device efficiency, also known as Transconductance Generation Factor (TGF) of HD-VS-FeFinFET and VS-FeFinFET for different ITCs polarity at various operating temperatures. These are the important parameters in the design of analog circuits and Figure 4.6 shows that, at high gate bias, g_m increases with decrease in temperature because the channel is in strong inversion where conduction is mobility-driven and reduced phonon scattering at lower temperatures enhances mobility, causing g_m to increase. In contrast, at low gate bias, an opposite behavior is observed. As, operation lies in the subthreshold region where conduction relies on thermally generated carriers, so a drop in temperature reduces carrier availability and lowers g_m. While analysing the impact of temperature on TGF, it is found that at higher gate bias, temperature has negligible impact on TGF as compared to large variation at lower gate bias because at high gate bias, strong inversion ensures strong electrostatic control, so temperature has little effect on TGF. In contrast, at low gate bias,

conduction relies on thermally activated carriers, making TGF highly sensitive to temperature variations. Also, it is clearly visible from the Figure 4.6 that HD-VS-FeFinFET showcases higher g_m and TGF along with negligible variations due to ITCs at all temperature ranges in contrast to visible increase(decrease) caused by NITC(PITC) in VS-FeFinFET as depicted in Figure 4.7.

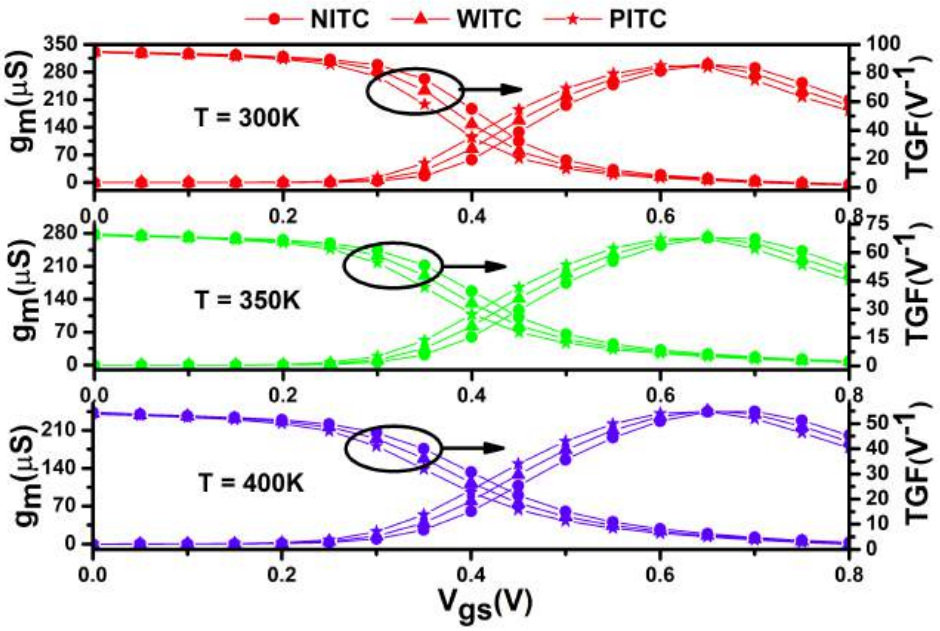

Figure 4.7: Influence of ITCs on transconductance and device efficiency of VS-FeFinFET at different operating temperatures (VC25a).

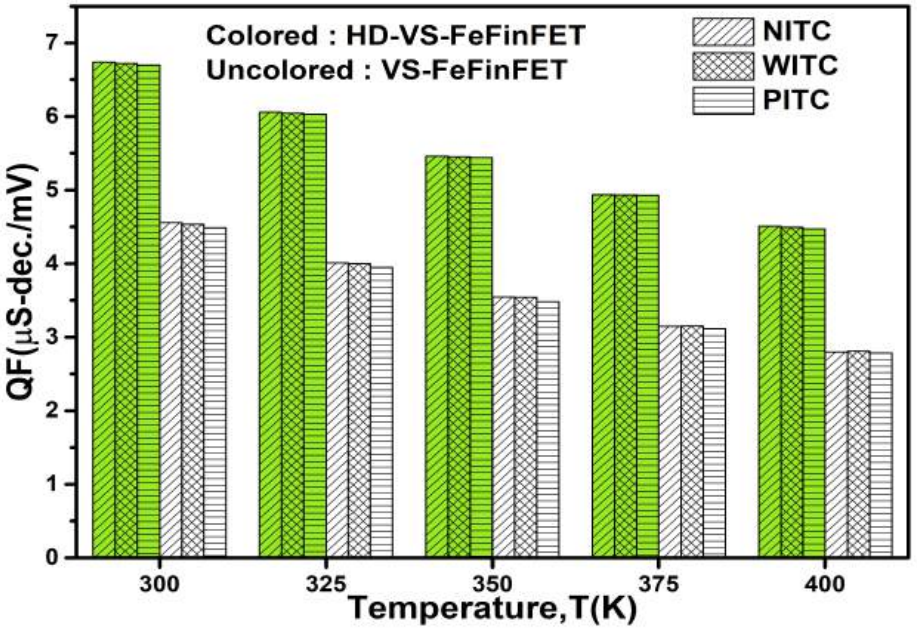

Figure 4.8: Variation in quality factor of HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs at different operating temperatures (VC25a).

Figure 4.8 shows the variation of quality factor (QF) of both the devices with variation in

temperature in presence of ITCs of different polarities. Dependence of QF on temperature is a critical consideration in the design and application of FETs in electronic circuits. It is inferred from the figure that, for rise in temperature from 300K to 400K, there is reduction in QF by 33.16% and 38.1% for HD-VS-FeFinFET and VS-FeFinFET respectively due to reduced transconductance at elevated temperature, attributed to the combined effects of increased carrier scattering and thermally induced leakage, which slightly degrade the device's performance. Further, the figure indicates that the presence of ITCs has only a minimal impact on the QF, demonstrating the robustness of the device against interfacial trap disturbances.

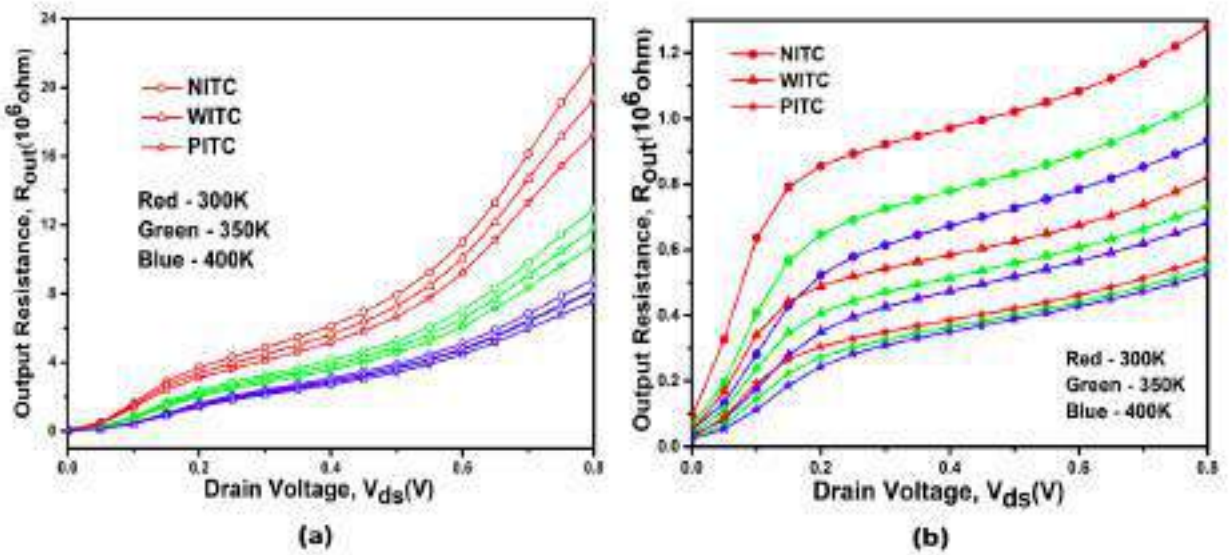

Figure 4.9: Variation in output resistance of (a) HD-VS-FeFinFET and (b) VS-FeFinFET under the influence of ITCs at different operating temperatures (VC25a).

Further, Figure 4.9(a) and Figure 4.9(b) displays the influence of ITCs of different polarities on the output resistance (R_{out}) of both the devices at different temperatures. Higher R_{out} ensures better signal fidelity by suppressing voltage variations for changes in load resistance as shown by HD-VS-FeFinFET at all the considered temperatures. Also, both the devices exhibit the behavior of negative temperature coefficient of resistance because the rise in carrier density with temperature due to intrinsic thermal generation and trap ionization overpowers the mobility degradation caused by phonon scattering, resulting in net decrease in R_{out} with increase in temperature. Further, High-k dielectric materials help in minimizing the average variation in R_{out} caused by ITCs (i.e. 11.3%) due to their ability to lower interface trap density and provide stronger electrostatic control over the channel in comparison to VS-FeFinFET, that showcases wide variation of 43% at 300K. Further, with rise in temperature to 400K, this average variation induced due to ITCs reduces to

Table 4.2: Summary of different static and analog parameters for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs at 300K

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	1.06×10^{-4}	1.03×10^{-4}	9.92×10^{-4}	1.27×10^{-4}	1.26×10^{-4}	1.26×10^{-4}
I_{off} (A)	5.83×10^{-12}	2.77×10^{-12}	1.30×10^{-12}	2.62×10^{-13}	2.36×10^{-13}	2.12×10^{-13}
I_{on}/I_{off}	$1.83\times10^{+7}$	$3.72\times10^{+7}$	$7.65\times10^{+7}$	$4.86\times10^{+8}$	$5.38\times10^{+8}$	$5.95\times10^{+8}$
$V_{th}(V)$	0.28	0.30	0.32	0.34	0.34	0.34
QF $(uS-dec/mV)$	4.49	4.53	4.56	6.70	6.60	6.74
g_m (S)	2.96×10^{-4}	2.99×10^{-4}	3.0×10^{-4}	3.97×10^{-4}	3.97×10^{-4}	3.97×10^{-4}
TGF (V^{-1})	94.42	94.75	95.10	119.43	120.29	121.21
R_{out} (ohm)	$5.74\times10^{+5}$	$8.19\times10^{+5}$	$1.28\times10^{+6}$	$1.73\times10^{+7}$	$1.93\times10^{+7}$	$2.17\times10^{+7}$

Table 4.3: Summary of different static and analog parameters for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs at 350K

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	9.95×10^{-5}	9.61×10^{-5}	9.23×10^{-5}	1.21×10^{-4}	1.20×10^{-4}	1.19×10^{-4}
I_{off} (A)	5.24×10^{-11}	2.76×10^{-11}	1.44×10^{-11}	3.46×10^{-12}	3.15×10^{-12}	2.87×10^{-12}
I_{on}/I_{off}	$1.90\times10^{+6}$	$3.47\times10^{+6}$	$6.40\times10^{+6}$	$3.49\times10^{+7}$	$3.81\times10^{+7}$	$4.16\times10^{+7}$
$V_{th}(V)$	0.25	0.27	0.29	0.31	0.32	0.32
QF $(uS-dec/mV)$	3.48	3.54	3.55	5.44	5.45	5.46
g_m (S)	2.69×10^{-4}	2.73×10^{-4}	2.72×10^{-4}	3.72×10^{-4}	3.71×10^{-4}	3.71×10^{-4}
TGF (V^{-1})	69	69.32	69.76	87.91	88.47	89.03
R_{out} (ohm)	$5.44\times10^{+5}$	$7.33\times10^{+5}$	$1.06\times10^{+6}$	$1.08\times10^{+7}$	$1.18\times10^{+7}$	$1.29\times10^{+7}$

7.78% and 29.8% for HD-VS-FeFinFET and VS-FeFinFET respectively because thermal effects like increased phonon scattering and carrier generation dominate device behavior with rising temperature, reducing the relative impact of ITCs and thus lowering the variation in R_{out}. The parametric values of device characteristics under the influence of ITCs at various operating temperatures are tabulated in Table 4.2 to Table 4.4.

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Table 4.4: Summary of different static and analog parameters for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs at 400K

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	9.25×10^{-5}	8.91×10^{-5}	8.53×10^{-5}	1.14×10^{-4}	1.14×10^{-4}	1.13×10^{-4}
I_{off} (A)	2.70×10^{-10}	1.54×10^{-10}	8.71×10^{-11}	2.43×10^{-11}	2.24×10^{-11}	2.07×10^{-11}
I_{on}/I_{off}	$3.42\times10^{+5}$	$5.77\times10^{+5}$	$9.79\times10^{+5}$	$4.70\times10^{+6}$	$5.07\times10^{+6}$	$5.46\times10^{+6}$
$V_{th}(V)$	0.22	0.25	0.27	0.29	0.29	0.29
QF $(uS-dec/mV)$	2.78	2.81	2.80	4.47	4.49	4.51
g_m (S)	2.42×10^{-4}	2.47×10^{-4}	2.45×10^{-4}	3.46×10^{-4}	3.45×10^{-4}	3.44×10^{-4}
TGF (V^{-1})	53.79	54.14	54.63	68.63	68.99	69.35
R_{out} (ohm)	$5.25\times10^{+5}$	$6.83\times10^{+5}$	$9.33\times10^{+5}$	$7.58\times10^{+6}$	$8.18\times10^{+6}$	$8.85\times10^{+6}$

4.4.2 Impact of ITCs with Variation in Density and Polarity

In this section, the effect of variation in ITCs density and polarity on both the devices is investigated at constant temperature of 300K. Three different ITCs densities are considered with positive and negative polarities as N_{it1}, N_{it2}, and N_{it3} equals to 1×10^{11} cm^{-2}, 1×10^{12} cm^{-2} and 1×10^{13} cm^{-2} respectively to analyse their impact on both the devices.

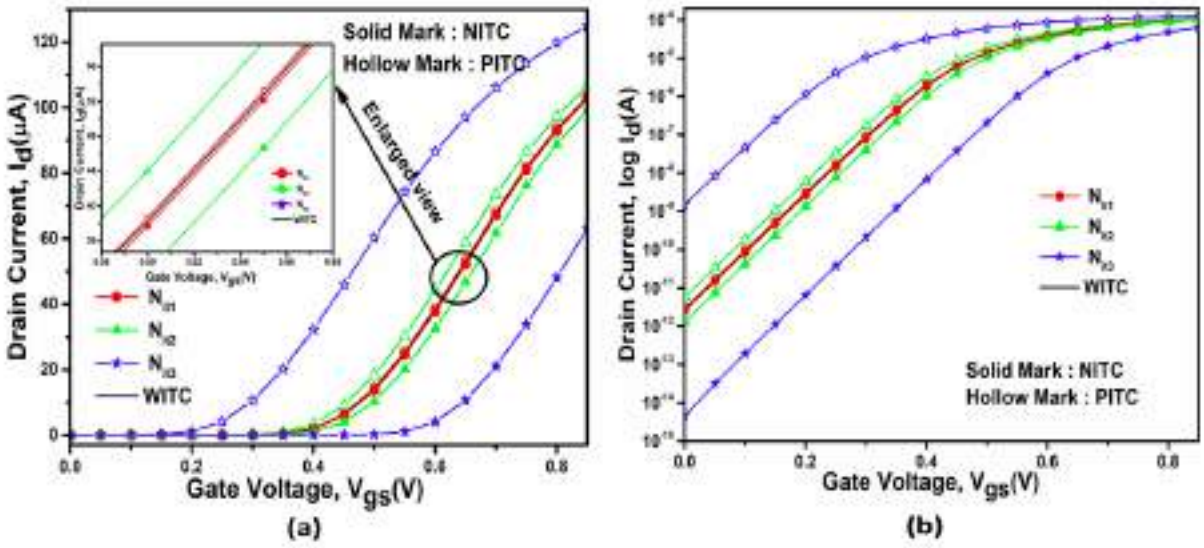

Figure 4.10: Impact of ITC's density and polarity on transfer characteristics of VS-FeFinFET in (a) linear and (b) log scale (VC25a).

Figure 4.10(a) and Figure 4.10(b) shows the impact of ITCs density of different polarity on

the transfer characteristics of VS-FeFinFET. It is clearly visible from the Figure 4.10(a) that with an increase in PITC(NITC) density to N_{it1}, N_{it2}, and N_{it3} , drain current increases(decreases) with respect to the case of WITC. This increase(decrease) in drain current is attributed to the decrease(increase) in the flatband voltage (V_{fb}) caused by the PITC(NITC) in proportionality to N_{it}, as defined previously by Eq. 4.6. Also, the degradation in I_{off} caused by PITC becomes more pronounced as the ITCs density increases. Quantitatively, when the PITC density rises from N_{it1} to N_{it2} and N_{it3}, I_{off} worsens by approximately 1.06 times, 2.11 times, and 552 times with respect to WITC, as shown in Figure 4.10(b). This occurs because higher trap densities introduce more localized states that enhance carrier recombination and leakage paths, significantly increasing the I_{off}.

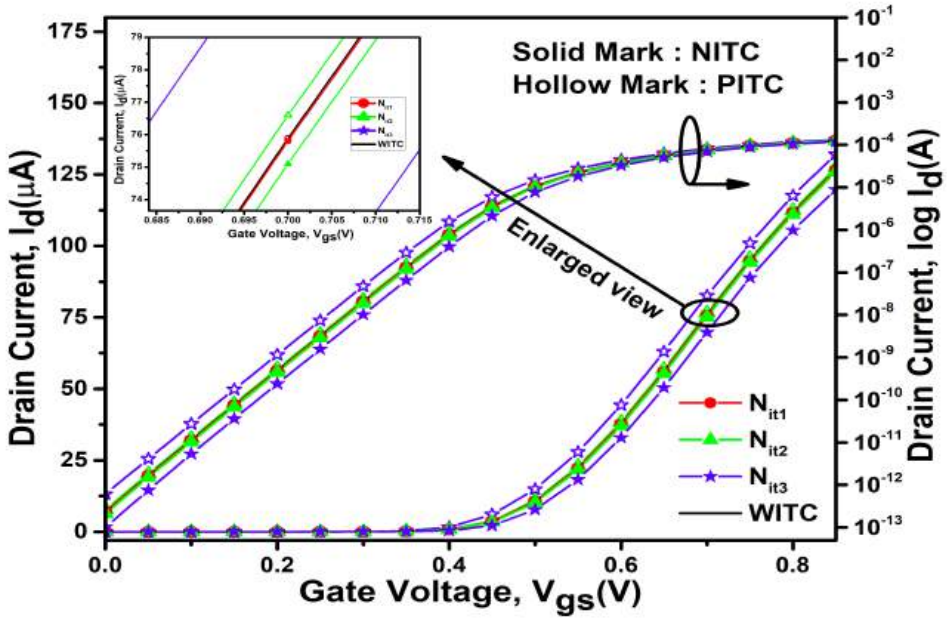

Figure 4.11: Effect of ITC's density and polarity on transfer characteristics of HD-VS-FeFinFET (VC25a).

In contrast to VS-FeFinFET, the implementation of heterogeneous gate dielectric engineering in HD-VS-FeFinFET not only helps in minimizing the variations caused by ITCs due to its ability to lower interface trap density, but also provides stronger electrostatic control over carrier transport. The improvement in the performance of the device is evident in Figure 4.11, where leakage current shows negligible degradation with increasing trap density. Specifically, as the PITC density increases to N_{it1}, N_{it2}, and N_{it3}, I_{off} degrades only marginally by around 1.01 times, 1.11 times, and 2.58 times, respectively with respect to WITC, thereby confirming that HD-VS-FeFinFET is more immune and reliable against ITCs than VS-FeFinFET.

Further, the presence of PITC (NITC) introduces additional positive (negative) charges at the interface, which alters the surface potential and shifts the energy band alignment. This modification influences carrier injection efficiency at the channel interface in proportionality to N_{it}, leading to a proportional increase (decrease) in I_{on}. It is evident by the increase(decrease) in I_{on} by 0.26% (0.32%), 3.35%(3.69%) and 21.3%(38.7%) for VS-FeFinFET with increase in PITC(NITC) density to N_{it1}, N_{it2}, and N_{it3} respectively, as shown in Figure 4.12. However the increase(decrease) in I_{on} for HD-VS-FeFinFET is negligibly very less that is only by 0.04%(0.05%), 0.58%(0.61%) and 4.3%(5.45%) with increase in PITC(NITC) density to N_{it1}, N_{it2}, and N_{it3} respectively, thereby confirming its improved reliability.

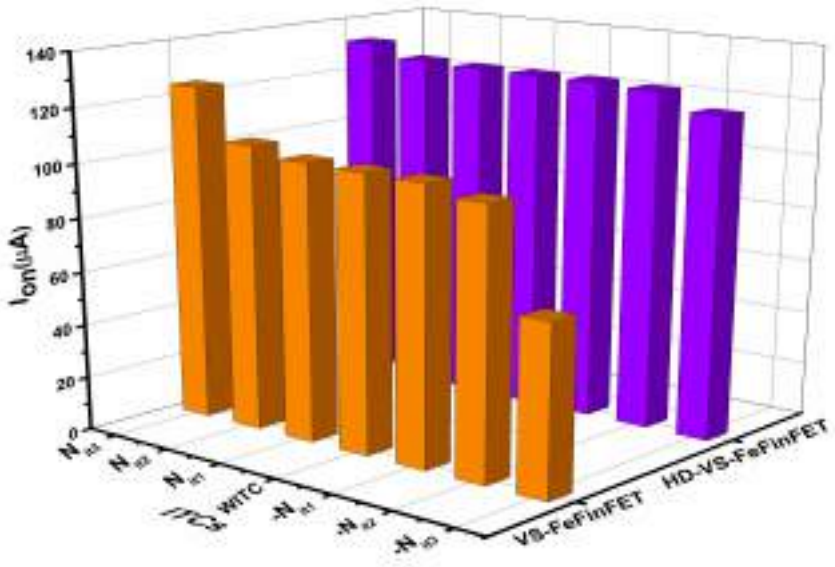

Figure 4.12: Effect of ITC's density and polarity on the ON current of HD-VS-FeFinFET and VS-FeFinFET (VC25a).

The impact of ITC density and polarity on V_{th} for both the devices is displayed in Figure 4.13. The reduced(enhanced) V_{th} for PITC(NITC) is the result of the increased(decreased) band bending caused by PITC(NITC)(GCS22). For VS-FeFinFET, V_{th} decreases (increases) significantly, by 59.69%(56.65%) at N_{it3}. In contrast, HD-VS-FeFinFET exhibits only minor variations, with V_{th} decreasing (increasing) by 6.56% (5.46%) under the same conditions. This minimal sensitivity arises from heterogeneous gate dielectric engineering, which lowers interface trap density and suppresses trap-assisted charge modulation, thereby making HD-VS-FeFinFET more immune to ITC-induced distortions in device performance. The parametric values of different performance parameters for VS-FeFinFET and HD-VS-FeFinFET under the influence of ITCs with varying density and polarity are tabulated in Table 4.5 and Table 4.6.

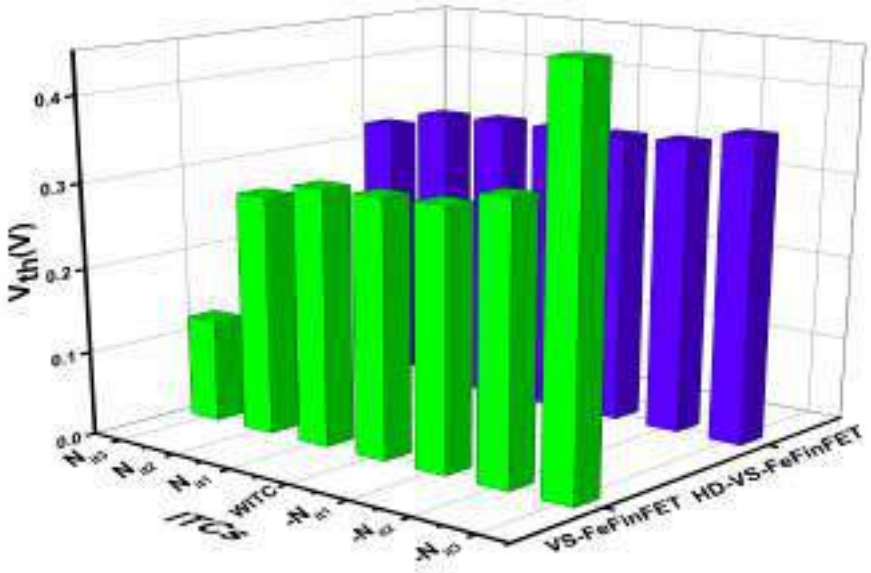

Figure 4.13: Effect of ITC's density and polarity on threshold voltage of HD-VS-FeFinFET and VS-FeFinFET (VC25a).

Table 4.5: Summary of different performance parameters for VS-FeFinFET under the influence of ITCs with varying density and polarity

Parameter	N_{it3}	N_{it2}	N_{it1}	WITC	-N_{it1}	-N_{it2}	-N_{it3}
I_{on} (A)	1.25×10^{-4}	1.06×10^{-4}	1.03×10^{-4}	1.03×10^{-4}	1.03×10^{-4}	9.92×10^{-5}	6.31×10^{-5}
I_{off} (A)	1.53×10^{-9}	5.83×10^{-12}	2.93×10^{-12}	2.77×10^{-12}	2.58×10^{-12}	1.30×10^{-12}	4.51×10^{-15}
I_{on}/I_{off}	$8.18\times 10^{+4}$	$1.83\times 10^{+7}$	$3.53\times 10^{+7}$	$3.72\times 10^{+7}$	$3.98\times 10^{+7}$	$7.63\times 10^{+7}$	$1.40\times 10^{+10}$
$V_{th}(V)$	0.12	0.28	0.30	0.30	0.30	0.32	0.47

Table 4.6: Summary of different performance parameters for HD-VS-FeFinFET under the influence of ITCs with varying density and polarity

Parameter	N_{it3}	N_{it2}	N_{it1}	WITC	-N_{it1}	-N_{it2}	-N_{it3}
I_{on} (A)	1.32×10^{-4}	1.27×10^{-4}	1.27×10^{-4}	1.27×10^{-4}	1.27×10^{-4}	1.26×10^{-4}	1.20×10^{-4}
I_{off} (A)	6.09×10^{-13}	2.62×10^{-13}	2.37×10^{-13}	2.36×10^{-13}	2.33×10^{-13}	2.12×10^{-13}	1.02×10^{-13}
I_{on}/I_{off}	$2.17\times 10^{+8}$	$4.86\times 10^{+8}$	$5.35\times 10^{+8}$	$5.38\times 10^{+8}$	$5.43\times 10^{+8}$	$5.94\times 10^{+8}$	$1.17\times 10^{+9}$
$V_{th}(V)$	0.32	0.34	0.34	0.34	0.34	0.34	0.36

4.4.3 Impact of ITCs and Temperature Affectability : Circuit Level Analysis

Increasing density of transistors per unit area of chip with advancing technologies results into huge amount of heat dissipation, which seriously affects the transistor's performance and causes variations in device's parameters such as threshold voltage (V_{tn}, V_{tp}) and carrier mobility (μ_n, μ_p)(SZV+13a).

The switching threshold voltage (V_{TH}) of a CMOS inverter can be explained by the well known Eq. 4.8, 4.9, and 4.10(JS21), as given below,

$$V_{\mathrm{TH}} = \frac{V_{\mathrm{dd}} - |V_{\mathrm{tp}}| + V_{\mathrm{tn}}\sqrt{\frac{(W/L)_{\mathrm{n}}\mu_{\mathrm{n}}C_{\mathrm{ox}}}{(W/L)_{\mathrm{p}}\mu_{\mathrm{p}}C_{\mathrm{ox}}}}}{1+\sqrt{\frac{(W/L)_{\mathrm{n}}\mu_{\mathrm{n}}C_{\mathrm{ox}}}{(W/L)_{\mathrm{p}}\mu_{\mathrm{p}}C_{\mathrm{ox}}}}} \tag{4.8}$$

$$\mu_{(\mathrm{n,p})} = \mu_0\left(\frac{T_0+\delta T}{T_0}\right)^{-\mathrm{m}} \tag{4.9}$$

$$V_{\mathrm{t(p,n)}} = V_{\mathrm{th0}} - k(T_0+\delta T) \tag{4.10}$$

where V_{tn} and V_{tp} respectively are the threshold voltages for n-channel and p-channel device, C_{ox} is the oxide capacitance, μ_n and μ_p are the electron and hole mobilities respectively, $(W/L)_n$ and $(W/L)_p$ are the aspect ratio of n-channel and p-channel device respectively, μ_0 is carrier mobility at room temperature, m is the mobility temperature exponent, T_0 is room temperature, dT is the temperature change from T_0, V_{th0} is the threshold voltage at absolute zero temperature, and k is the temperature coefficient of the threshold voltage.

The carrier mobilities and threshold voltages of n-type and p-type configurations are two major metrics which are strongly dependent on operating temperatures, thus the characteristics of inverter are also temperature dependent(JS21).

Also ITCs can generate additional spurious signals that can have a detrimental effect on the performance of CMOS inverter, influencing parameters like threshold voltage, mobility, leakage current, noise margin, and overall reliability of the circuits(KNSVS23; PGP+20b). These effects

are critical in advanced and scaled-down CMOS technologies, thus it is necessary to analyze the impact of ITCs of different polarity on HD-VS-FeFinFET based CMOS inverter at various operating temperatures.

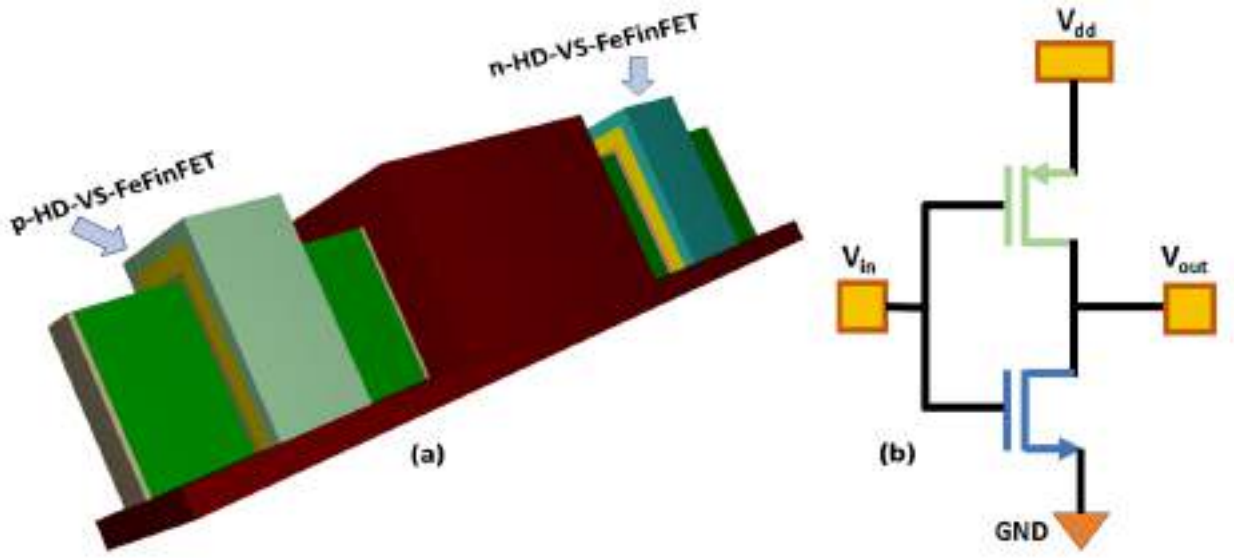

Figure 4.14: (a) 3D structure and (b) Schematic diagram of HD-VS-FeFinFET based CMOS inverter (VC25a).

For this, a required setup is designed on Cogenda Visual TCAD simulator with n-channel and p-channel HD-VS-FeFinFET isolated electrically with the help of 60nm SiO_2 spacer. Figure 4.14(a) and Figure 4.14(b) respectively shows the 3D simulated structure and schematic of the CMOS inverter circuit where V_{dd}, V_{in}, and V_{out} are the supply voltage, input voltage and output voltage respectively.

Initially, threshold matching of both the n-channel and p-channel structure is done for HD-VS-FeFinFET based CMOS inverter as displayed in Figure 4.15(a) and Figure 4.15(b) at different operating temperatures and in presence of different ITCs respectively. The V_{gs} is varied from -0.85 to 0.85V with dual work function metal (DWFM) integration scheme, which employs two different gate metals with distinct work functions such that low for nMOS and high for pMOS, to independently tune their threshold voltages. Also, ITCs with different polarity have been introduced at the semiconductor-oxide interface with trap charge density fixed at 10^{12} cm^{-2} in this section.

The voltage transfer characteristic (VTC) is a key metric for evaluating the switching behavior and overall stability of a CMOS inverter and for this, VTC for HD-VS-FeFinFET based CMOS inverter under the influence of ITCs with different polarities and at various operating temperatures

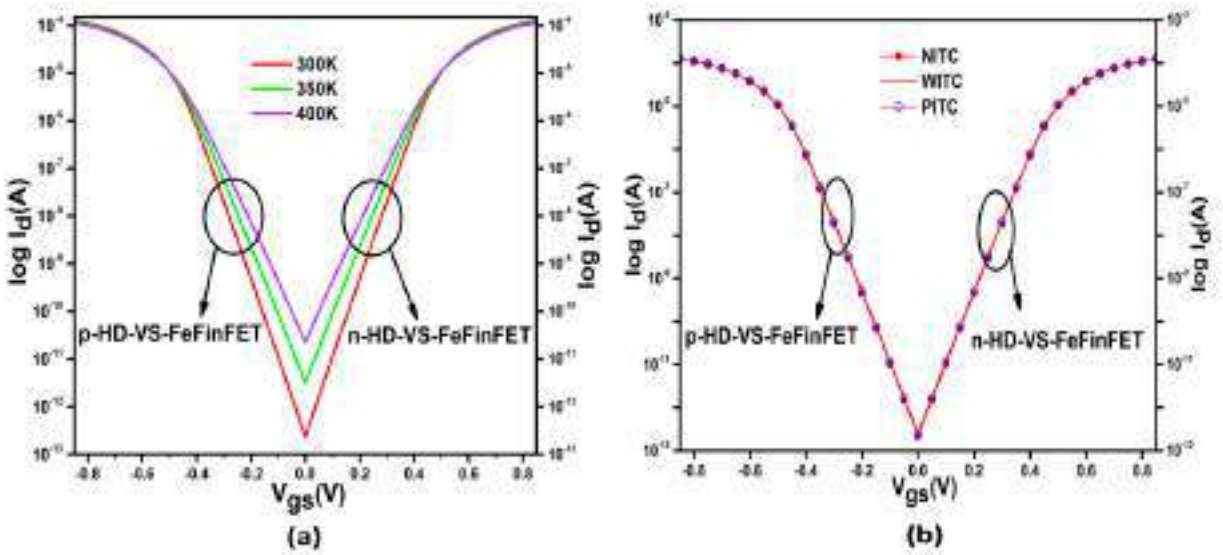

Figure 4.15: Influence of (a) temperature and (b) ITCs on threshold voltage matching curve for HD-VS-FeFinFET based CMOS inverter (VC25a).

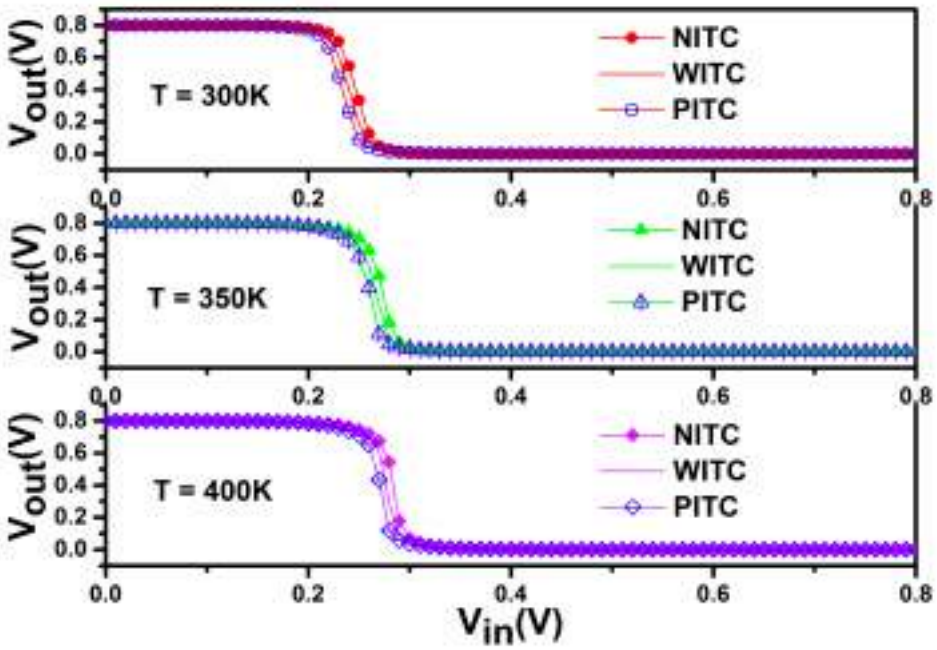

Figure 4.16: Impact of ITCs polarity on voltage transfer characteristics of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures (VC25a).

is analysed as shown in Figure 4.16. Simulation results a rightward shift of approximately 34.62 mV in the inverter switching threshold voltage (V_{TH}) when the temperature rises from 300K to 400K. This occurs due to reduced carrier mobility at higher temperatures, which requires a higher input voltage to switch the inverter. While this shift slightly slows the switching speed, it improves noise immunity and ensures more reliable operation over a wide temperature range. Also, as we have very well discussed about the improved reliability of HD-VS-FeFinFET under the influence of

ITCs in previous sections, this is very well maintained in HD-VS-FeFinFET based CMOS inverter as confirmed from the Figure 4.16, which displays only negligible average variations of 1.45% for NITC(PITC) in V_{TH} at 300K and that too decreases to 0.73% with increasing temperature to 400K.

Further, Noise Margin (NM) is a crucial parameter to depict the noise immunity of the circuit and this value should be high enough for better tolerance to variations and more reliable operation(SNP$^+$24). Modification in threshold voltage of MOSFETs due to variation in temperature can cause the input and output levels to either rise or fall from their ideal state at room temperature, which leads to variation in noise margin. It is found as shown in Table 4.7 that with increase in temperature to 400K, noise margin decreases by 6.8%. Also improved immunity of HD-VS-FeFinFET towards ITCs is very well confirmed in its CMOS inverter circuits with negligible variation in noise margin by 1.13%(1.26%) at 300K, 1.29%(1.48%) at 350K and 1.39%(1.32%) at 400K under the influence of NITC(PITC), making it reliable for digital circuits and applications.

Table 4.7: Summary of different performance parameters of HD-VS-FeFinFET based CMOS inverter under the influence of ITCs at various operating temperature

T (K)	ITCs	V_{IL} (mV)	V_{IH} (mV)	V_{OL} (mV)	V_{OH} (mV)	NM_L (mV)	NM_H (mV)	V_{TH} (mV)	TR (mV)
300	PITC	183.77	267.27	4.33×10^{-7}	800	1.84×10^{2}	532.72	242.13	83.50
	WITC	191.06	273.89	5.51×10^{-7}	800	1.91×10^{2}	526.10	246.92	82.83
	NITC	197.68	279.86	7.04×10^{-7}	800	1.98×10^{2}	520.13	249.31	82.17
350	PITC	201.22	289.09	8.18×10^{-6}	800	2.01×10^{2}	510.90	265.93	87.86
	WITC	207.42	296.58	1.01×10^{-5}	800	2.07×10^{2}	503.41	271.82	89.16
	NITC	213.78	303.09	1.24×10^{-5}	800	2.14×10^{2}	496.90	270.42	89.31
400	PITC	213.38	303.19	7.70×10^{-5}	799.98	2.13×10^{2}	496.78	276.25	89.81
	WITC	220.51	309.67	9.25×10^{-5}	799.99	2.21×10^{2}	490.31	281.55	89.16
	NITC	226.72	316.53	1.11×10^{-4}	799.99	2.27×10^{2}	483.45	280.40	89.81

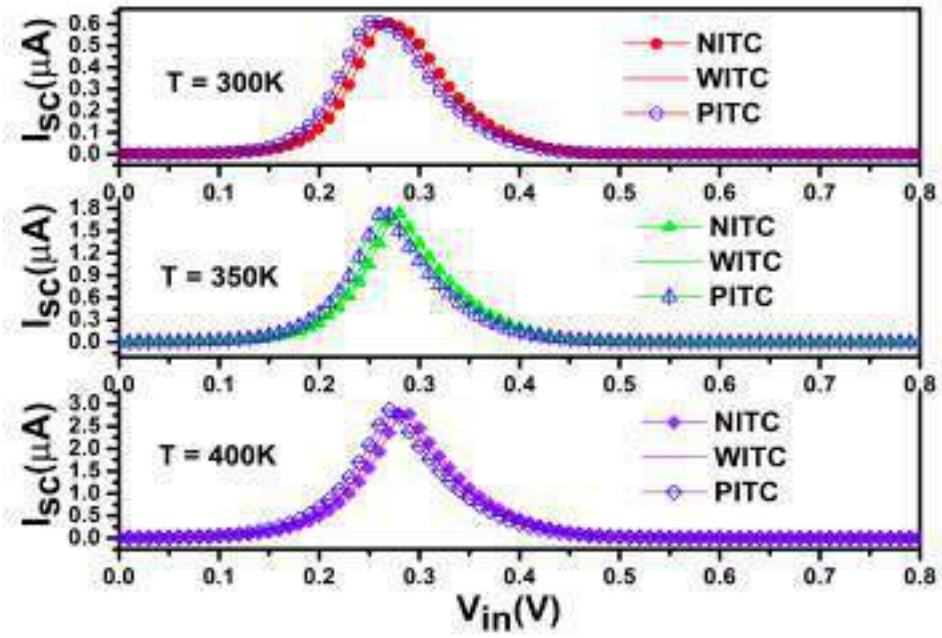

Figure 4.17: Impact of ITCs polarity on switching current of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures (VC25a).

Figure 4.17 displays the variation of switching current (I_{sc}) under the influence of ITCs with different polarities and at various operating temperatures. It shows the increasing trend of I_{sc} with temperature such that peak I_{sc} increases upto 4.66 times along with rightward shift when temperature increases from 300K to 400K. It also shows the slight increase (decrease) in I_{sc} for NITC (PITC) at lower V_{in} occurs because ITC-induced modulation of the channel potential lowers (raises) the effective threshold voltage, allowing conduction at lower (higher) V_{in}. At higher V_{in}, the trend reverses as the channel is fully turned on, and the dominant effect is the reduced (enhanced) carrier injection efficiency due to ITC-induced scattering or trap-assisted charge modulation, leading to a slightly lower (higher) I_{sc}. Also, it confirms the improved reliability of HD-VS-FeFinFET based CMOS inverter with neglible variation in peak value I_{sc} from 0.99%(0.31%) at 300K to 2.41%(0.81%) at 400K in presence of NITC(PITC).

Further, Figure 4.18(a) and Figure 4.18(b) respectively displays the performance comparison of HD-VS-FeFinFET based CMOS inverter for its transition range and voltage gain at various operating temperatures. HD-VS-FeFinFET based CMOS inverter exhibits a sharper transition and higher voltage gain at 300K due to enhanced carrier mobility and reduced leakage currents, enabling faster and more efficient switching. The higher gain improves the inverter's ability to sharply distinguish between logic '0' and '1', enhancing noise margins, signal integrity, and overall

circuit reliability.

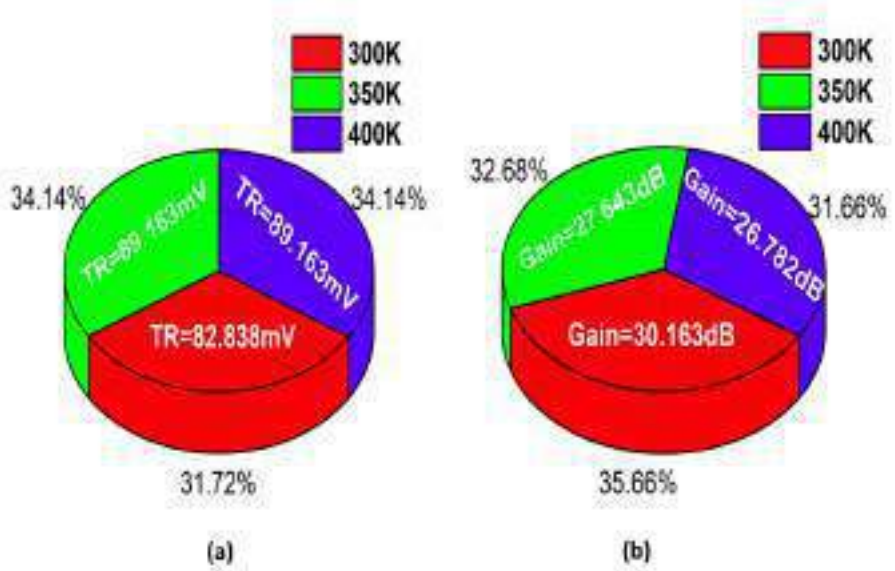

Figure 4.18: Comparison chart of (a) transition region (b) voltage gain of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures (VC25a).

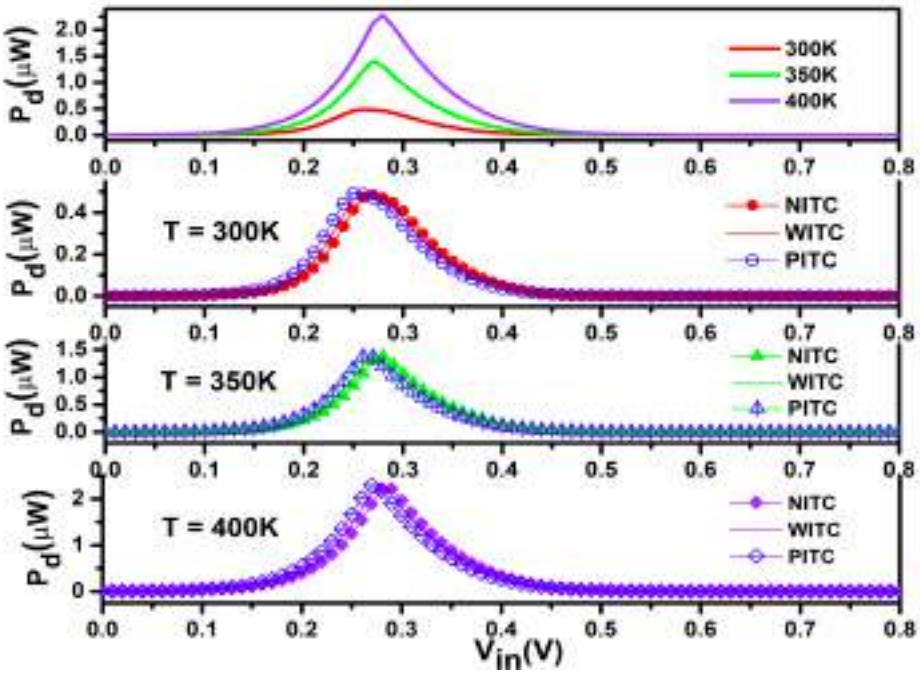

Figure 4.19: Impact of ITCs polarity on power dissipation of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures (VC25a).

Although dissipation of power was traditionally negligible in CMOS technology, it has become a significant factor in modern, scaled-down technologies due to increased leakage currents(KNSVS23). Figure 4.19 displays the variation of power dissipation (P_d) in HD-VS-FeFinFET based CMOS inverter under the influence of ITCs with different polarity and at various operating temperatures.

It is inferred from the figure that with increase in temperature from 300K to 400K, P_d increases upto 3 times due to stronger thermally activated carrier transport and increased leakage paths at elevated temperatures, a predictable behavior that can be leveraged in designing thermal-aware circuits for reliable operation. Also, the graph shows that NITC(PITC) minimally affects the power performance of the inverter with variations by 0.99%(0.31%) at 300K to 2.41%(0.81%) at 400K, thus confirming its reliability especially for applications that operate in variable temperature environments and where power efficiency is critical.

4.5 Summary

Interface trap charges result from dangling bonds created by the abrupt end of the semiconductor surface, hence they are unavoidable. Since trap charges are always present in real devices and are never zero, it is crucial to understand and mitigate their effects for the design of reliable and efficient semiconductor devices, particularly in applications that demand high performance under varying environmental conditions. So, this chapter presented a comprehensive analysis from device to circuit level to encompass the reliability of HD-VS-FeFinFET in terms of : 1) temperature affectability on impact of ITCs to understand their effect at various operating temperatures 2) impact of ITCs density with different polarity, over various figure of merits. Results demonstrate that HD-VS-FeFinFET has better immunity against ITCs with minimun variation at all considered operating temperatures such as average variation of 0.6% in I_{on} at 300K and 0.64% in I_{on} at 400K in contrast to variation shown by VS-FeFinFET like 3.5% in I_{on} at 300K and 4% in I_{on} at 400K. Further, the study done to analyze the impact of ITCs density and polarity reveals that device performance alters significantly with rising density of ITCs for both PITC(NITC) but this deviation is very much less in HD-VS-FeFinFET with 4.3%(5.45%) in I_{on}, and 6.56% (5.46%) in V_{th} for PITC(NITC) in comparison to 21.3%(38.7%) and 59.69% (56.65%) respectively in VS-FeFinFET. Further, the extensive performance analysis done at circuit level for HD-VS-FeFinFET based CMOS inverter under the influence of ITCs at various operating temperatures confirmed its improved immunity towards ITCs and makes it an ideal choice for advanced digital circuits and low-power electronic applications. Thus, this study highlights how HD-VS-FeFinFET maintains high reliability and performance under coupled thermal and trap dynamics, establishing it as a robust and efficient

candidate for CMOS inverter applications in increasingly demanding and dynamic environments of the future.

While this chapter provided an in-depth exploration of the reliability of HD-VS-FeFinFETs under the coupled influence of temperature variations, interfacial trap charges (ITCs), and their polarity/density effects, the analysis also underscored a critical insight—device performance and reliability are not solely governed by interface phenomena but are equally dependent on the intrinsic material properties of the ferroelectric layer. Since the ferroelectric HfO_2 layer forms the core of polarization switching and charge control, its structural, electronic, and thermal characteristics directly dictate the overall efficiency and stability of the device. Hence, to establish a more fundamental and holistic understanding, it becomes essential to extend the investigation from interface-related reliability concerns to the intrinsic material-level properties and their translation into device and circuit performance.

Therefore, the next chapter shifts the focus towards a comprehensive investigation of ferroelectric HfO_2-based devices, incorporating both material-level (through DFT-based analysis of dopants and structural modifications) and device-level (through performance characterization under varying conditions) perspectives. This transition allows for a deeper understanding of how dopant engineering, thermal effects, and self-heating mechanisms influence the electrical behavior of HD-VS-FeFinFETs and their circuit-level applications. By bridging the gap between interface-driven reliability issues and intrinsic material-driven performance modulation, this chapter builds a coherent pathway towards the optimized design of robust, energy-efficient, and scalable ferroelectric devices for next-generation electronic systems.

Chapter 5

Investigating DFT and Device Level Behavior in Doped Ferroelectric HfO_2 based Hetero Dielectric Vertically Stacked FeFinFET with Self-Heating and Logic Circuit Perspectives

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* In this chapter, a comprehensive investigation of doped ferroelectric HfO_2 based device is presented, encompassing atomic-level, device-level, and circuit-level analysis.

* At the device level, the impact of various doped ferroelectric materials on the transfer characteristics of Hetero Dielectric Vertically Stacked Ferroelectric FinFET (HD-VS-FeFinFET) is studied, highlighting dopant-driven modulation of the performance parameters with enhancement in drain current (I_{on}) by 24%, transconductance (g_m) by 29% and transconductance generation factor (TGF) by 10.8% for silicon doped HfO_2 over lanthanum doped HfO_2 as ferroelectric layer.

* Subsequently, Density Functional Theory (DFT) simulations are performed to examine the structural and electronic properties of undoped HfO_2 and its doped variants using Gadolinium (Gd) and Silicon (Si), which have been found as two best performing ferroelectric materials at the device level. The influence of different dopants material on band structure and projected density of states is analyzed to evaluate their suitability for ferroelectric applications. The

influence of increasing dopants concentration for silicon doped HfO_2 is also studied at DFT level.

* Further, self-heating effects (SHE) are critically examined in HD-VS-FeFinFET structure across varying biasing voltages and ambient temperatures. The analysis reveals influence on transconductance with its peak shifts leftwards towards lower V_{gs}, along with lattice temperature contour evolution due to SHE, emphasizing its impact on device reliability. Further, the output characteristics also show alteration in drain current by 33.3% at V_{gs} equals to 0.6V due to SHE which decreases to 0.03% with reduction in V_{gs} to 0.2V.

* Finally, CMOS inverter circuits utilizing these advanced technologies are analyzed in terms of switching characteristics under different biasing voltages and thermal conditions. Key performance metrics such as switching current, propagation delay, rise time, and fall time are evaluated to assess circuit-level implications of material and device-level effects.

* Thus, the integrated multi-scale analysis provides a holistic understanding of material doping and thermal effects on device and circuit performance, establishing a pathway for the optimized design of ferroelectric-based next-generation device for advanced low-power, high-speed electronic applications.

5.1 Introduction

Chapter 4 provided a comprehensive reliability analysis of HD-VS-FeFinFET devices under the coupled effects of temperature variations and interface trap charges (ITCs), which are unavoidable due to the intrinsic nature of dangling bonds at the semiconductor–dielectric interface. This study provided valuable insights into how unavoidable ITCs can degrade device and circuit performance, while also proving that HD-VS-FeFinFET exhibits superior immunity to ITCs as compared to VS-FeFinFET by clearly demonstrating the robustness of the hetero-dielectric stacked design and confirmed its potential for future nanoelectronic systems operating under thermally varying and trap-prone environments. This robustness was further validated at the circuit level, where HD-VS-FeFinFET-based CMOS inverters maintained stable switching characteristics across a range of temperatures under the influence of ITCs. Such findings clearly demonstrated the device's potential for energy-efficient and reliable operation in next-generation digital circuits. However, this investigation focused primarily on the electrical reliability aspect without delving into the material-level origins of ferroelectric behavior in HfO_2, which forms the active layer of these devices.

It is well established in the literature that the ferroelectric properties of HfO_2 are not intrinsic but strongly dependent on doping(PS25; ZCL+22; RK23). Later, (SHF25) demonstrated that introducing dopants such as Silicon, Gadolinium, or Zirconium directly influences switching properties and reliability of HfO_2-based ferroelectric devices. Similarly, (KCL+25) studied ultra-thin $Hf_{0.5}Zr_{0.5}O_2$ films and showed that scaling effects coupled with dopant engineering play a crucial role in maintaining the performance in ferroelectric based devices. Moreover, (PKD+25; DK21) emphasized that dopant selection and concentration are decisive factors in doped HfO_2 based ferroelctric devices, thereby controlling leakage current in the device. (Alr24; IJF22) further highlighted that doping is directly correlated with leakage suppression, making it one of the most effective knobs for optimizing device performance.

Considering these evidences, it becomes clear that trap reliability analysis alone cannot provide a complete picture of device behavior. While Chapter 4 addressed how HD-VS-FeFinFETs respond to unavoidable ITCs and thermal conditions, the microscopic origins of ferroelectric switching and its enhancement through dopant engineering were not explored. This forms a critical research gap

because the overall performance metrics such as drain current (I_{on}), transconductance (g_m), and circuit-level switching characteristics are directly linked to dynamics of doped HfO_2 ferroelectric layer, which in turn are governed by material-level properties(SGS$^+$15; TXM$^+$19).

Thus, Chapter 5 builds upon the findings of Chapter 4 by investigating how different dopants (Silicon, Gadolinium, Lanthanum, Zirconium, etc.) influence the structural and electronic properties of HfO_2 using Density Functional Theory (DFT) simulations, and how these material-level changes translate into improved device performance in terms of drain current and analog performance metrics. By bridging this gap between trap reliability and dopant-driven material engineering, the work offers a more holistic understanding of HD-VS-FeFinFET reliability.

While dopant driven material engineering offers promising pathways for enhancing device reliability and performance, the choice of ferroelectric material itself also plays a critical role. In aggressively scaled devices, however, traditional perovskite-based ferroelectrics face significant limitations due to their relatively large physical thickness, incompatibility with standard CMOS fabrication processes, and associated environmental concerns(IHK$^+$16). To overcome these limitations, doped hafnium oxide (HfO_2) thin films are adopted as the ferroelectric layer, offering better integration with existing semiconductor manufacturing techniques(RC23). In this work, a detailed study has been carried out by varying the Landau coefficients (α_x and β_x) to capture the ferroelectric behavior of different doped HfO_2-based ferroelectric materials, each characterized by specific α_x and β_x parameters, as given here. For lanthanum (La) doping, α_x was taken as –3.46 $\times$ 10^{10} cm/F and β_x as 8.55 $\times$ 10^{18} cm^5/F/C^2. Zirconium (Zr)-doped layers used α_x of –8.6 $\times$ 10^{10} cm/F and β_x of 1.3 $\times$ 10^{20} cm^5/F/C^2, while aluminum (Al) doping applied α_x of –1.05 $\times$ 10^{11} cm/F with β_x of 2.06 $\times$ 10^{20} cm^5/F/C^2. Similarly, for strontium (Sr), α_x was –1.12 $\times$ 10^{11} cm/F and β_x was 1.06 $\times$ 10^{20} cm^5/F/C^2. Gadolinium (Gd)-doped layers used α_x of –1.13 $\times$ 10^{11} cm/F and β_x of 1.42 $\times$ 10^{20} cm^5/F/C^2, for silicon (Si)-doped layers α_x was –1.29 $\times$ 10^{11} cm/F and β_x of 6.49 $\times$ 10^{20} cm^5/F/C^2 (BGKG05; JHS22). These dopant-specific Landau parameters directly impact the ferroelectric free energy landscape, enabling a comparative evaluation of each dopant's effect on the ferroelectric phase formation and switching dynamics within the HfO_2 matrix. This investigation provides a critical groundwork for optimizing dopant selection to augment ferroelectric FinFET performance(BGKG05).

Thereafter, this work presents a systematic DFT analysis for the structural and electronic properties of HfO_2 as a ferroelectric material layer in FeFET devices. We investigate the pristine (undoped) HfO_2 structure as well as HfO_2 doped with gadolinium (Gd) and silicon (Si) atoms to understand the impact of doping on its structural and electronic behavior. Specifically, we analyze four configurations: pure HfO_2, Gd-doped HfO_2, singly Si-doped HfO_2, and doubly Si-doped HfO_2. For each of these material systems, we evaluate the band structure and projected density of states (DOS) to gain insights into their potential suitability as ferroelectric layers. The comparative analysis of these parameters enables us to assess how doping modifies the electronic properties of HfO_2, which is critical for optimizing its performance in next-generation ferroelectric FET devices.

In addition to the dopant-dependent ferroelectric behavior analyzed through varying Landau parameters, the present study also addresses the critical impact of self-heating effects (SHE), particularly in the context of Si-doped HfO_2-based FeFinFETs. As device scaling advances, SHE has become a major reliability concern due to restricted thermal dissipation pathways in nanoscale 3D structures like FeFinFETs(PRJ17; Sha16). The combination of high current densities and the inherently low thermal conductivity of gate stack materials leads to localized heat accumulation within the channel and surrounding regions(KSM$^+$18; PDCA21a). This temperature rise not only degrades carrier mobility and induces threshold voltage shifts but also accelerates degradation mechanisms such as time-dependent dielectric breakdown (TDDB), where prolonged electrical stress progressively weakens the gate dielectric until eventual failure, thereby threatening long-term device reliability(AMC$^+$19).

Recognizing the significance of this issue, a detailed electrothermal analysis has been performed specifically for Si-doped HfO_2 ferroelectric FinFET structures within this work. The choice of silicon as a dopant, which was shown to exhibit the highest β_x value (6.49×10^{20} cm^5/F/C^2) and the most negative α_x (-1.299×10^{11} cm/F), directly influences the polarization behavior and energy landscape of the ferroelectric layer. However, the influence of localized heating on polarization stability and switching efficiency is critical, as elevated temperatures can modify the ferroelectric response and exacerbate thermal reliability issues(EYKM22; YXH$^+$22). Therefore, this study integrates self-heating effect with ferroelectric domain analysis to evaluate how temperature rise affects electrical characteristics in Si-doped HfO_2 gate stacks. The combined dopant-dependent and electrothermal investigation provides a comprehensive understanding of Si-doped HfO_2-based

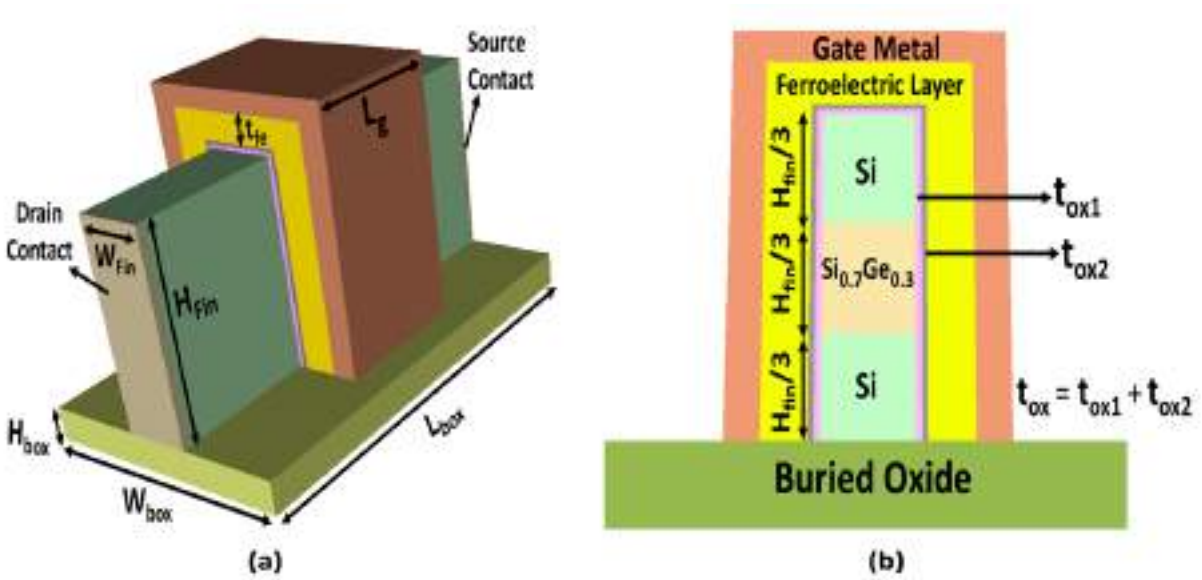

Figure 5.1: (a) 3D schematic view of HD-VS-FeFinFET (b) inset of vertical cross-sectional view of HD-VS-FeFinFET.(VC25a)

FeFinFET performance, highlighting the necessity of addressing SHE for the development of thermally robust, high-performance ferroelectric devices.

Beyond atomic-level and device-level analysis, it is equally important to assess the circuit-level implications of dopant incorporation and electrothermal effects in FeFinFETs. In particular, the CMOS inverter being the fundamental building block of digital logic, serves as a benchmark for evaluating device performance under realistic operating conditions. Prior studies have shown that inverter characteristics such as voltage transfer characteristics, propagation delay, and dynamic switching behavior are highly sensitive to thermal variations and supply voltage scaling, which directly influence the reliability and energy efficiency of nanoscale circuits(KK07; LHL05). Therefore, analyzing inverter-level performance of Si-doped HfO_2-based HD-VS-FeFinFET across different biasing voltages and ambient temperatures is essential to capture their thermal stability, scalability, and suitability for low-power, high-speed digital applications.

This chapter is organized as follows: Section 5.2 includes all the specifications regarding the device structure. The simulation framework mentioning the physical models used for the device are discussed in section 5.3. Section 5.4 provides the results and discussion for the suitability of dopant material for HfO_2 based ferroelectric layer, studying the influence of electrothermal SHE on the device performance, and later device based circuit is also analyzed for its switching performance. Section 5.5 provides a complete summary of the chapter.

5.2 Device Structure

Figure 5.1(a) shows the 3D structure of HD-VS-FeFinFET while Figure 5.1(b) shows the 2D structure of the device chopped vertically through its fin. The gate length is fixed at 20nm along with height and width of the fin is taken as 30nm and 8nm respectively. Various ferroelectric material are chosen for the simulation with thickness of ferroelectric layer fixed at 6nm. The total gate oxide thickness is taken as 1nm. Also, a trilayered strained silicon channel is formed with the stacking of silicon and silicon-germanium having their mole fraction in the ratio of 0.7 and 0.3 respectively. The doping concentration considered for channel is 1×10^{16} cm^{-3} with p-type and that of source/drain is 1×10^{20} cm^{-3} with n-type. In addition, a metal gate with work function set at 4.65 eV, having exceptional thermal stability and is well-suited with CMOS processing, is used in this device to avert any poly-depletion effect(MC24; ZLX$^+$24). Further, to exploit the benefits of SOI technology, the entire strained FeFinFET is built on an insulator box with width, height, and length fixed at 32 nm, 5 nm, and 62 nm respectively(VC24a). All the device specifications are also mentioned in Table 5.1.

Table 5.1: Device parameters

Parameters	Dimension
Gate length (L_g)	20nm
Drain/Source ($L_{d/s}$)	20nm
Channel material	Si-$Si_{0.7}Ge_{0.3}$-Si
Oxide thickness (t_{ox})	1nm
Ferroelectric thickness (t_{fe})	6nm
Background dielectric constant of Ferroelectric layer	27
Width of fin (W_{Fin})	8nm
Height of fin (H_{Fin})	30nm
Doping concentration of drain/source ($N_{d/s}$)	1×10^{20} (cm^{-3})
Doping concentration of channel (N_{ch})	1×10^{16} (cm^{-3})
Gate work function (ϕ)	4.65eV

5.3 Simulation Framework and Physical Models

All the simulations are done using Cogenda's Genius 3D TCAD simulator. The simulation process includes the drift–diffusion model level 2 (DDML2), which incorporates the effect of lattice temperature by simultaneously solving the additional thermal equation along with the electrical equations. These equations are solved self-consistently with Poisson's equation as given by Eq. 5.1 and continuity equations for electrons and holes as given by Eq. 5.2 and Eq. 5.3 respectively(VC24a; LKLK24). With the inclusion of the thermal component, the governing framework of DDML2 is extended by the heat conduction equation as given by Eq. 5.4, thereby enabling accurate modeling of self-heating effects(MC24; PDCA21b).

$$\nabla.\epsilon\nabla\psi = -q(p - n + N_{\mathrm{D}}{}^{+} - N_{\mathrm{A}}{}^{-}) \tag{5.1}$$

$$\frac{\partial n}{\partial t} = \nabla.(\mu_{\mathrm{n}} n\vec{E}_{\mathrm{n}} + \mu_{\mathrm{n}}\frac{k_{\mathrm{b}}T}{q}\nabla n + \mu_{\mathrm{n}}\frac{k_{\mathrm{b}}\nabla T}{q}n) - (U - G) \tag{5.2}$$

$$\frac{\partial p}{\partial t} = -\nabla.(\mu_{\mathrm{p}} p\vec{E}_{\mathrm{p}} - \mu_{\mathrm{p}}\frac{k_{\mathrm{b}}T}{q}\nabla p - \mu_{\mathrm{p}}\frac{k_{\mathrm{b}}\nabla T}{q}p) - (U - G) \tag{5.3}$$

$$\rho c_{\mathrm{p}}\frac{\partial T}{\partial t} = \nabla.\kappa\nabla T + \vec{J}.\vec{E} + (E_{\mathrm{g}} + 3k_{\mathrm{b}}T).(U - G) \tag{5.4}$$

where ψ is the electrostatic potential associated with vacuum level, ϵ is the permittivity for the material, $N_D{}^{+}$ and $N_A{}^{-}$ are the concentrations for the ionized impurities, n and p are the concentration considered electron and hole respectively, q is the electric charge, μ_n and μ_p are mobilities for electrons and holes, U and G are the recombination and generation rates associated for both electrons and holes, E_n and E_p are the effective driving electrical field for electrons and holes, ρ is the mass density of the semiconductor material considered, c_p is the heat capacity, κ is the thermal conductivity of the material, $\vec{J}.\vec{E}$ Joule heating of the current (LKLK24; WSZ+24).

Further, Shockley-Read Hall (SRH) recombination and Auger models accurately capture the

temperature and doping-dependent recombination-generation phenomenon for carriers(WSZ+24; KKD20b). Then, Philips mobility model for silicon-germanium and Lombardi mobility model for silicon are considered to take into account the mobility degradation at the semiconductor-oxide interface. Lucent model and Esurface model are used to capture the high field mobility effects along with hot carrier models for considering the effect of hot carriers(ZLX+24). The density gradient method is also used to consider quantum confinement phenomena along with the Fermi–Dirac carrier statistics model(VC24a). These models together provide a complete framework to accurately capture the key physical effects in the device.

5.4 Result and Discussion

5.4.1 Impact of material specific dopants in HfO_2 doped ferroelectric layer on the device performance

The physics of ferroelectric layer is modeled with the time-dependent Landau–Khalatnikov (LK) framework for associating electric field used for the ferroelectric layer (E_{FE}) as a function of polarization (P) as given by Eq. 5.5,

$$E_{\mathrm{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho(\frac{\partial P}{\partial t}) \tag{5.5}$$

where α, β, and γ are the static Landau ferroelectric material-dependent coefficients while g as dipole interaction coefficient and ρ as viscosity coefficient are taken as 1×10^{-4} cm^3/F and 2.25×10^4 Ω cm respectively(VC24a). In this study, different material dopants are considered for HfO_2 as mentioned in Table 5.2 and they are modelled with their associated values of α and β.

Figure 5.2 shows the impact of various dopants in HfO_2 ferroelectric layer on the transfer characteristics of HD-VS-FeFinFET in linear and log scale. The enhanced ON-state drain current (I_{on}) is achieved in D1 and D2, showing a higher dependency of I_{on} on α whereas leakage current (I_{off}) degrades in D6 due to the lower value of β. More negative α in D1 and D2 enhances internal voltage amplification due to stronger polarization switching, which improves surface potential modulation in the channel, leading to better gate control and higher I_{on}. Lower β in D6 deteriorates the stability

Table 5.2: Landau coefficients for various dopant material considered for HfO_2 ferroelectric layer

Dopant material in HfO_2 doped FE layer	Configuration	α (cm/F)	β ($cm^5/F/C^2$)
Silicon	D1	-1.29×10^{11}	6.49×10^{20}
Gadolinium	D2	-1.13×10^{11}	1.42×10^{20}
Strontium	D3	-1.12×10^{11}	1.06×10^{20}
Aluminium	D4	-1.05×10^{11}	2.06×10^{20}
Zirconium	D5	-8.6×10^{10}	1.3×10^{20}
Lanthanum	D6	-3.46×10^{10}	8.55×10^{18}

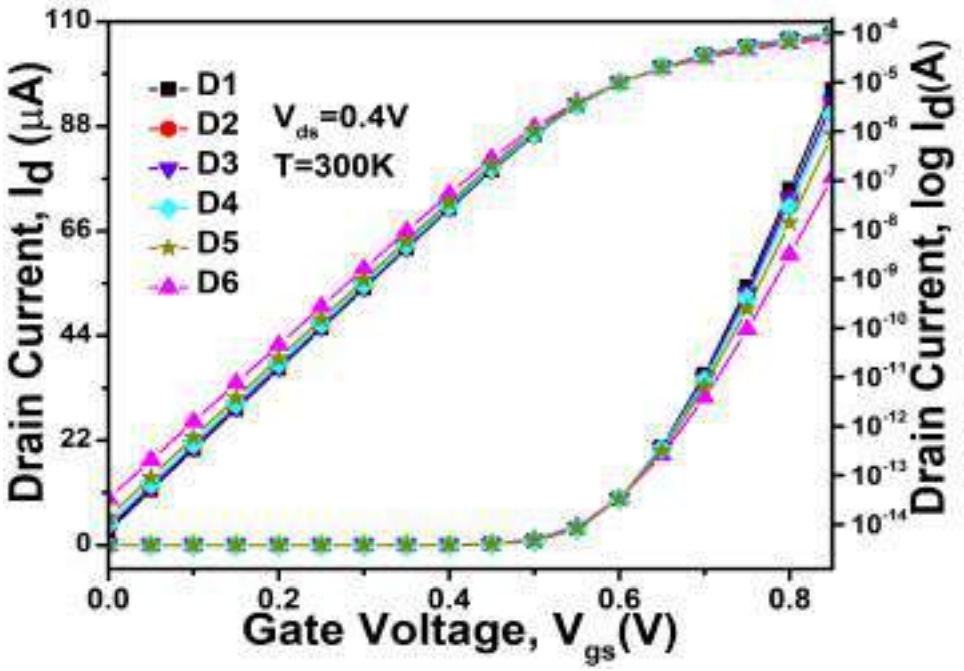

Figure 5.2: Impact of different dopant material on the transfer characteristics of HD-VS-FeFinFET linear and log scale

of the ferroelectric polarization states which results in less sharp polarization switching and poor subthreshold control along with unwanted leakage paths. Hence, I_{off} increases in D6. Following the above trend, D1 shows significantly improved g_m as compared to other dopants material used in HfO_2 owing to its more effective gate modulation of the channel potential, resulting in a higher transconductance (g_m) as shown in Figure 5.3(a) . Also, the transconductance generation factor (TGF), defined as the ratio of g_m to drain current (I_d), also shows its dependency on these landau coefficients. A more negative value of α not only increases g_m but also enhances the TGF, as the improvement in g_m is proportionally higher relative to I_d in D1 as showcased in Figure 5.3(b). So, the study supports that Si doped HfO_2 showcased better ferroelectric property with improved

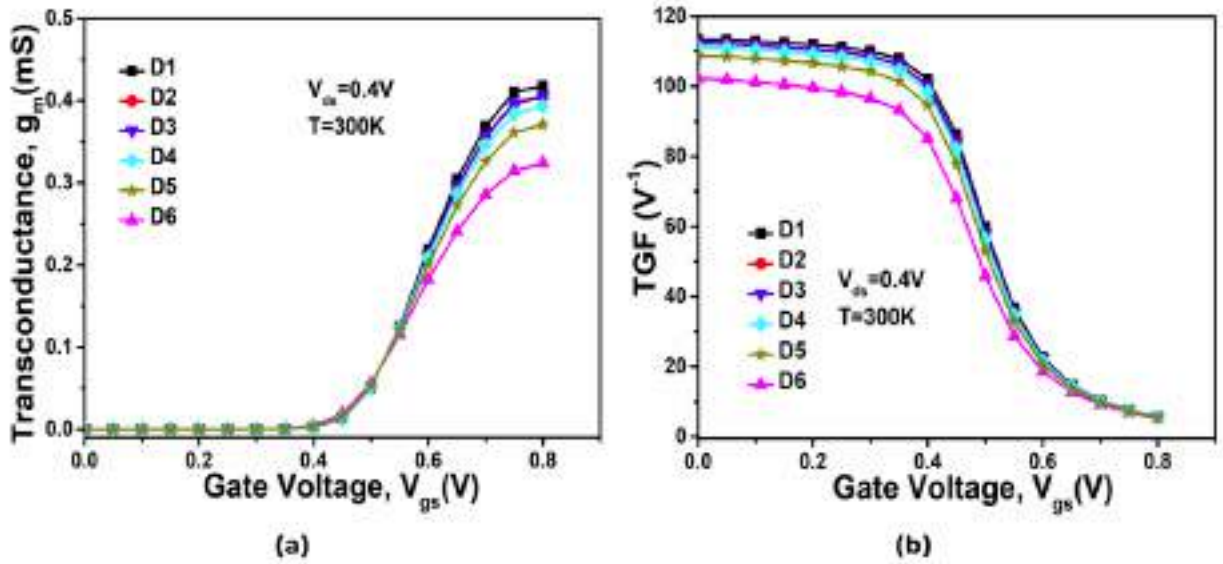

Figure 5.3: Impact of different dopant material on the transconductance and TGF of HD-VS-FeFinFET

device performance as compared to other material dopants. The parametric values of device characteristics for various dopant materials are tabulated in Table 5.3.

Table 5.3: Summary of performance parameters of HD-VS-FeFinFET for different ferroelectric dopants material at T=300K

Parameter	D1	D2	D3	D4	D5	D6
I_{on} (A)	9.57×10^{-5}	9.29×10^{-5}	9.32×10^{-5}	9.07×10^{-5}	8.63×10^{-5}	7.72×10^{-5}
I_{off} (A)	7.51×10^{-15}	8.88×10^{-15}	8.74×10^{-15}	1.03×10^{-14}	1.42×10^{-14}	3.32×10^{-14}
I_{on}/I_{off}	1.27×10^{10}	1.05×10^{10}	1.07×10^{10}	8.84×10^{9}	6.07×10^{9}	2.33×10^{9}
g_m (S)	4.18×10^{-4}	4.05×10^{-4}	4.06×10^{-4}	3.93×10^{-4}	2.67×10^{-2}	3.24×10^{-4}
TGF (V^{-1})	1.13×10^{2}	1.12×10^{2}	1.12×10^{2}	1.11×10^{2}	3.10×10^{2}	1.02×10^{2}

5.4.2 DFT studies on the electronic properties of HfO_2 doped ferroelectric material at atomic level

In this section, DFT analysis is done to study the electronic properties of HfO_2 as ferroelectric material doped with various dopant elements. This study investigates the pristine (undoped) HfO_2

structure as well as HfO_2 doped with gadolinium (Gd) and silicon (Si) atoms to understand the impact of doping on its electronic behavior. Specifically, four configurations have been analysed: pure HfO_2, Gd-doped HfO_2, singly Si-doped HfO_2, and doubly Si-doped HfO_2. For each of these configurations, various performance metrics such as band structure and projected density of states (PDOS) are studied to gain insights into their potential suitability as ferroelectric material.

5.4.2.1 Crystal Structure and Computational Methodology

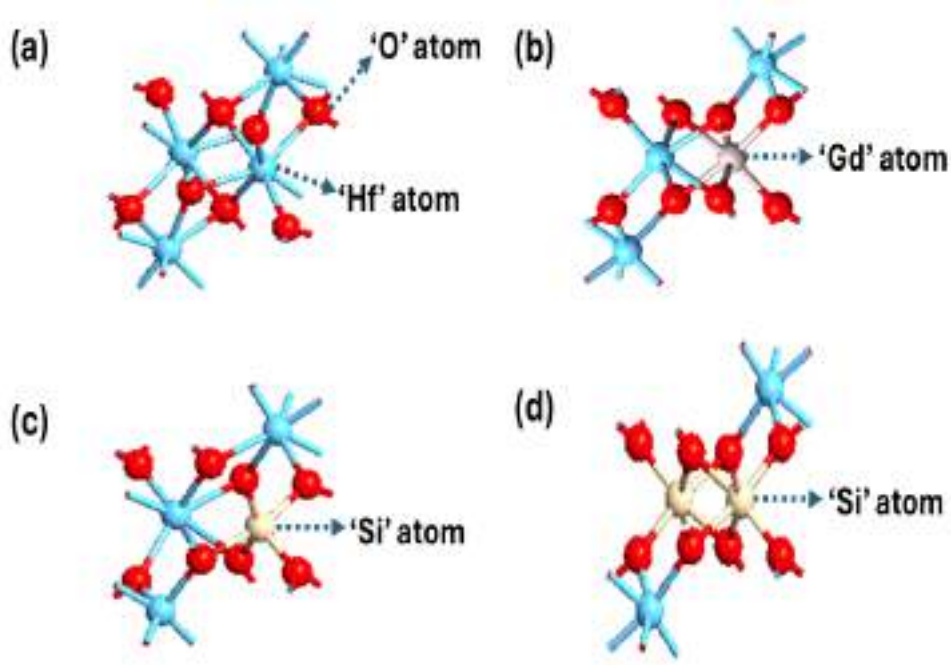

Figure 5.4: Atomic level structure considered for four different configurations (a) Undoped HfO_2 (b) gadolinium doped HfO_2 (c) singly Si–doped HfO_2 (d) doubly Si–doped HfO_2

In this study, the atomic structure of ferroelectric hafnium dioxide (HfO_2) was modeled in its orthorhombic crystalline phase, which is known to exhibit non-centrosymmetric distortion—a key characteristic for sustaining ferroelectric behavior. The primitive unit cell used for undoped HfO_2 consists of 4 hafnium (Hf) atoms and 8 oxygen (O) atoms, arranged in a lattice. The orthorhombic symmetry facilitates the formation of a polar phase, crucial for applications in ferroelectric field-effect transistors (FeFETs). To explore the influence of doping on the electronic properties, three doped variants of HfO_2 are considered along with undoped HfO_2 as showcased in Figure 5.4, such as (a) Undoped HfO_2 (b) Gadolinium doped HfO_2 (Gd–doped HfO_2) in which one Hf atom is replaced by an Gd atom, (c) Singly silicon doped HfO_2 (singly Si–doped HfO_2) in which one Hf atom is replaced by a Si atom, (d) Doubly silicon doped HfO_2 (doubly Si–doped HfO_2) in which two Hf

atoms are replaced by two Si atoms.

5.4.2.2 Method of Crystal

All structures are geometrically optimized using DFT as implemented in the Quantum ATK simulation package. The Perdew–Burke–Ernzerhof (PBE) exchange–correlation functional under the Generalized Gradient Approximation (GGA) is employed for all calculations. Ultrasoft pseudopotentials are used for the core electrons, and a plane-wave basis set with an energy cutoff suitable for transition-metal oxides is chosen to ensure convergence. Brillouin zone integrations are performed using a Monkhorst-Pack kkk-point mesh, optimized for energy convergence(DGMIB19; LSO+23; ZMDL24).

5.4.2.3 Performance Comparison

The comparative analysis of key electronic properties such as band structure and PDOS, enables us to assess how doping modifies the electronic properties of HfO_2, which is critical for optimizing its performance in next- generation ferroelectric FET devices.

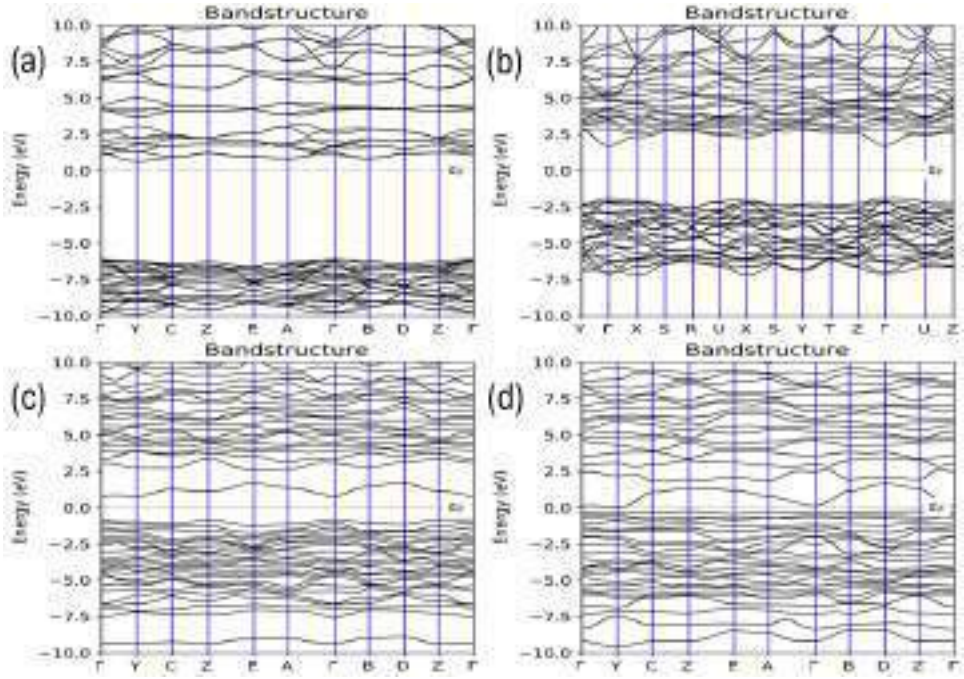

Figure 5.5: Variation in bandstructure of (a) Undoped HfO_2 (b) Gd–doped HfO_2 (c) singly Si–doped HfO_2 (d) doubly Si–doped HfO_2

Figure 5.5 reveals the band structure of all the four configurations. The electronic band struc-

tures for all configurations are computed to evaluate their relative band gaps and electronic transition characteristics. The doubly Si-doped HfO_2 crystal exhibited a lower band gap as compared to the undoped, Gd-doped, and singly Si-doped structures. The band gap narrowed notably in the doubly Si-doped HfO_2 structure. A reduced band gap implies enhanced carrier injection and improved switching behavior, both of which are desirable for FET applications. The additional Si atoms introduce localized states near the conduction band edge, which facilitate easier electron transitions.

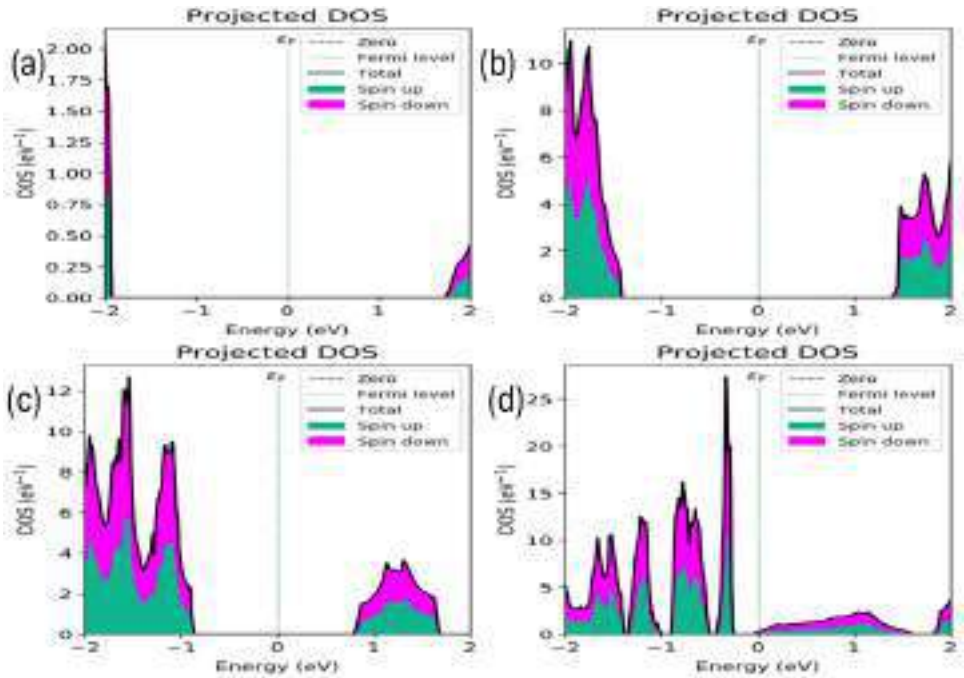

Figure 5.6: Variation in Projected Density of States (PDOS) (a) Undoped HfO_2 (b) Gd–doped HfO_2 (c) singly Si–doped HfO_2 (d) doubly Si–doped HfO_2

Figure 5.6 shows the PDOS for all the four configurations. The Projected Density of States (PDOS) profiles show a significantly higher peak near the Fermi level for the doubly Si-doped HfO_2 structure. Also, it shows the densest electronic states around the minimum of conduction band. A higher PDOS near the Fermi level enhances the material's ability to conduct charge and supports better ferroelectric polarization switching. This behavior suggests that doubly Si doping increases the availability of electronic states for conduction, making it more suitable for electronic and ferroelectric applications.

Among all the analysed configurations, the doubly Si-doped HfO_2 structure exhibits the most favorable characteristics for ferroelectric FET applications. The simultaneous enhancement in PDOS along with a reduced band gap, points towards a synergistic effect of dual-Si doping in promoting

desirable electronic properties required for FeFET applications.

5.4.3 Influence of Self Heating Effect on the performance of HD-VS-FeFinFET under varying biasing conditions and ambient temperatures

This section focuses on analysing the impact of self heating effect (SHE) on the performance of HD-VS-FeFinFET, comparing its crucial performance parameters with and without considering self heating. Additionally, the study investigates how this impact varies under varying biasing voltages and ambient temperatures. These insights are critical for designing thermally robust FeFinFET-based circuits, especially in applications where thermal management and reliability are of paramount importance.

As showcased in Figure 5.7, the transfer characteristics of the device shifts downwards exhibiting lower ON current as compared to ideal curve (without considering SHE). This reduction is attributed to channel temperature rise by self heating which leads to phonon scattering and ultimately mobility degradation. On the other hand, leakage current is observed to be almost same in case of with and without considering self heating effect. This is because SHE is mainly caused by the joule heating which depends significantly on the current flow during the ON state of the device. In the subthreshold region, the drain current is extremely low resulting in minimal channel heating thus SHE is practically inactive in this region.

Thereafter, as the V_{ds} is reduced, overall ON current reduces and this reduction is observed in both the cases of with and without considering SHE. Moreover SHE impact is less noticeable at lower V_{ds} as degradation in I_{on} is 24% at V_{ds}=0.2V as compared to degradation of 34.1% at V_{ds}=0.6V. This is because of the less localized self heating within the channel at lower V_{ds}. This is also observable in the contour profile showing the lattice temperature in the device at different biasing voltages in Figure 5.8 . As it is observed, as V_{ds} increases, the lattice temperature contour profile evolves from a nearly uniform distribution to a highly localized hot spot near the channel-drain region. The temperature peak shifts closer to the drain side, as maximum energy dissipation happens in this region due to higher electric field at the drain side. The contour profile shows pronounced hot spots, with the lattice temperature significantly elevated near the drain-end of the channel. Heat begins spreading laterally and vertically into the surrounding regions, but the core

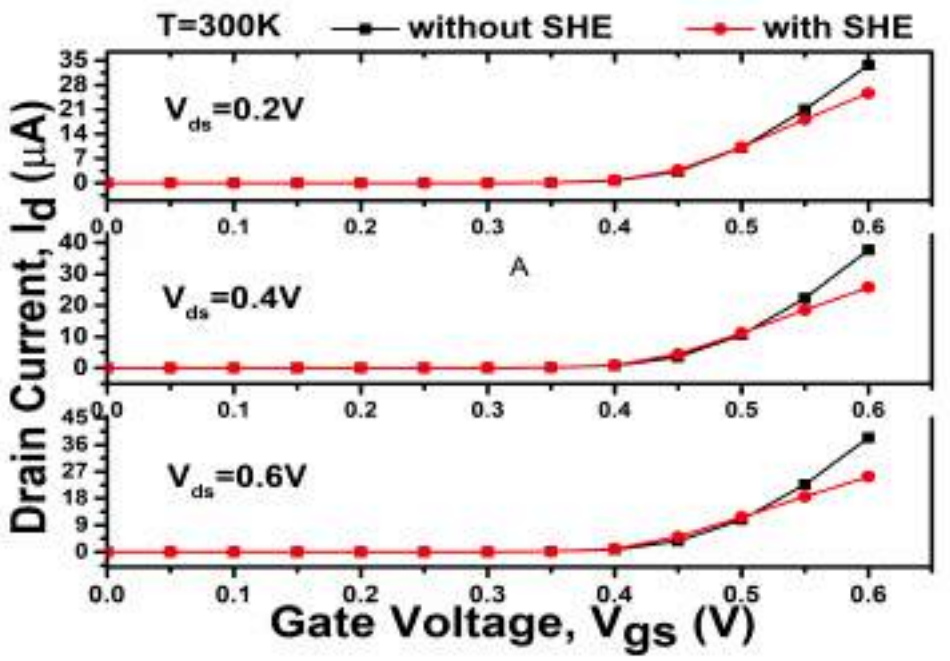

Figure 5.7: Influence of SHE on the transfer characteristics of HD-VS-FeFinFET at different biasing voltages

of the hot spot remains concentrated near the channel-drain interface.

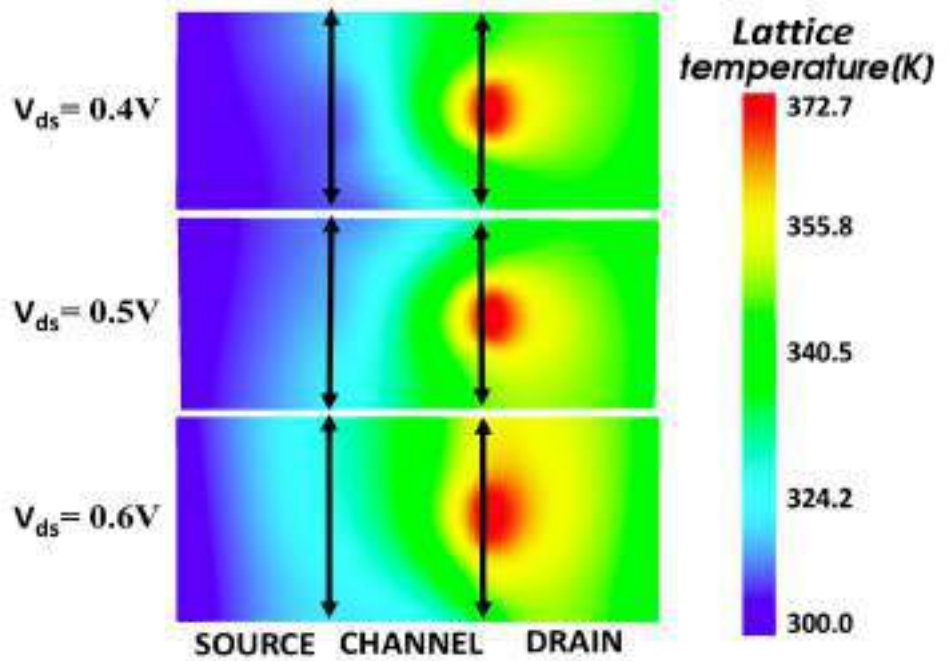

Figure 5.8: Contour profile of lattice temperature at different biasing voltages of HD-VS-FeFinFET under the influence of SHE

Figure 5.9(a) shows the variation in transconductance with variation in V_{gs} with and without considering SHE that too at varying biasing voltages. In absence of SHE, g_m rises steadily with V_{gs} and then saturates with maximum peak for higher V_{ds}. In contrast, in case of consideration of SHE,

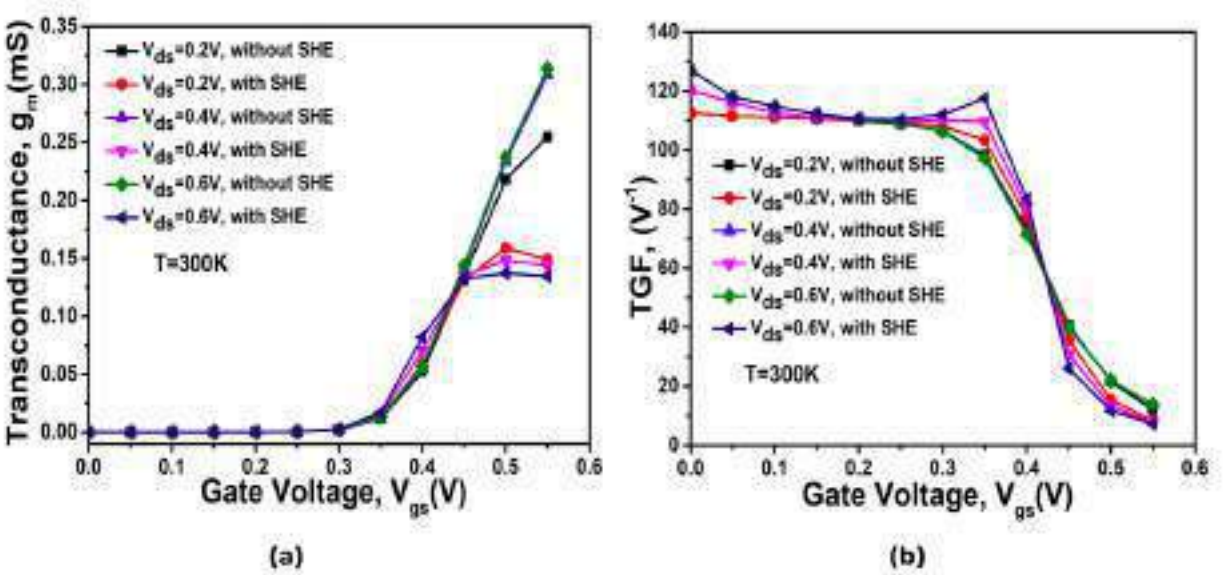

Figure 5.9: Influence of SHE on the (a) g_m (b) TGF for HD-VS-FeFinFET at different biasing voltages

for higher V_{ds}, weakened transconductance is observed due to significant localized channel heating. Moreover, g_m curve with SHE flattens earlier and stays below without SHE curve, indicating degraded gate control due to thermal effects. Figure 5.9(b) shows the variation of Transconductance Generation Factor at different biasing voltages and higher value of TGF implies the enhanced efficiency of the device at converting gate modulation into the drain current. As, it can be observed from the figure, TGF increases as the supply voltage is increasing due to enhanced inversion and better channel control. Also, SHE seems to have no impact on TGF in subthreshold region since the channel temperature does not rise significantly above the ambient temperature to generate contributable heat. While in the middle region, self heating begins to impact device performance but its impact on drain current is more severe then g_m which result in higher TGF with SHE as compared to without SHE. At higher V_{gs}, TGF with SHE decreases, reversing the trend observed in the middle region. This occurs because the device operates in strong inversion, with the channel fully formed, which leads to higher carrier densities and increased joule heating. The resulting temperature rise exacerbates mobility degradation and scattering effects, causing a larger reduction in g_m as compared to the drain current.

Figure 5.10 shows the impact of SHE on the output characteristics of the device for varying biasing voltages. The difference between the curves with and without SHE becomes more significant at higher gate bias, due to increased power dissipation in the channel. This elevates the local tempera-

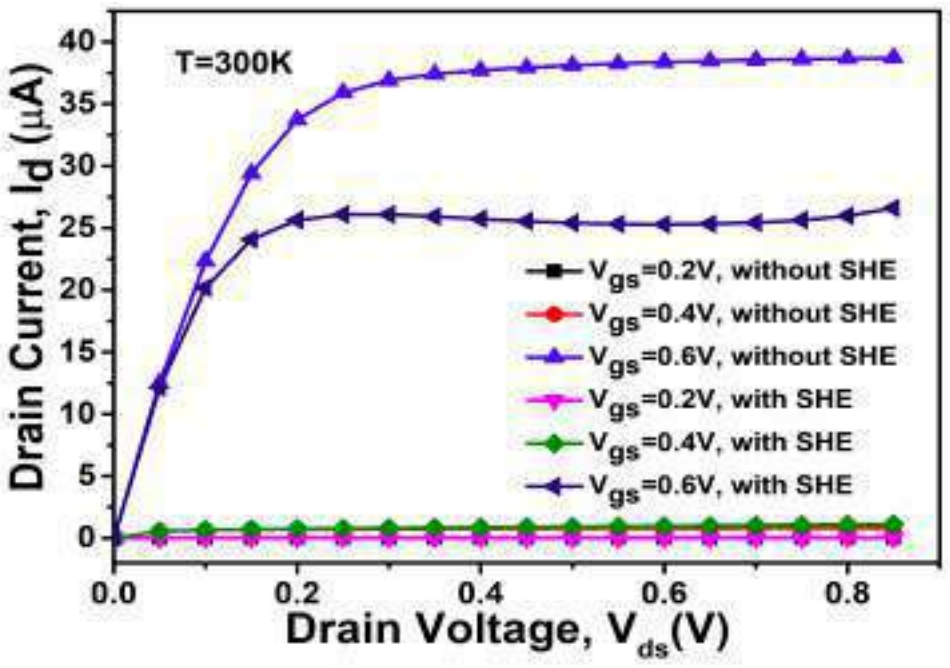

Figure 5.10: Influence of SHE on the output characteristics of HD-VS-FeFinFET at different biasing voltages

ture, reducing carrier mobility and enhancing scattering, which amplifies SHE-induced degradation at high V_{gs}. The parametric values of device characteristics under the influence of SHE at various biasing voltage are tabulated in Table 5.4.

Table 5.4: Summary of performance parameters at different biasing voltage considering SHE and without SHE

Parameter	without SHE			with SHE		
	V_{ds}=0.2V	V_{ds}=0.4V	V_{ds}=0.6V	V_{ds}=0.2V	V_{ds}=0.4V	V_{ds}=0.6V
I_{on} (A)	3.37×10^{-5}	3.77×10^{-5}	3.84×10^{-5}	2.56×10^{-5}	2.57×10^{-5}	2.53×10^{-5}
I_{off} (A)	2.45×10^{-13}	2.36×10^{-13}	2.25×10^{-13}	2.45×10^{-13}	2.36×10^{-13}	2.25×10^{-13}
I_{on}/I_{off}	1.38×10^{8}	1.60×10^{8}	1.70×10^{8}	1.05×10^{8}	1.09×10^{8}	1.12×10^{8}
g_m (S)	1.27×10^{-2}	1.54×10^{-2}	1.57×10^{-2}	7.93×10^{-3}	7.40×10^{-3}	3.75×10^{-3}
TGF (V^{-1})	5.62×10^{3}	6.01×10^{3}	6.3×10^{3}	5.63×10^{3}	6.01×10^{3}	1.48×10^{2}

Further, it is explored that how the temperature rise affect the influence of self heating on the device characteristics, which is critical for evaluating the thermal robustness of the device. Figure 5.11 presents the transfer characteristics of the device at various ambient temperatures, comparing performance with and without SHE. The drain current degrades with increasing temperature

because of carrier mobility degradation due to phonon scattering and SHE exacerbates this degradation further due to added localized heating in addition to ambient temperature rise as showcased in Figure 5.11. Also, in case of SHE, the drain current curves almost overlap at various ambient temperatures because the device's internal heating dominates its external ambient temperature variations, leading to similar channel temperatures and almost similar current degradation across varying ambient temperature.

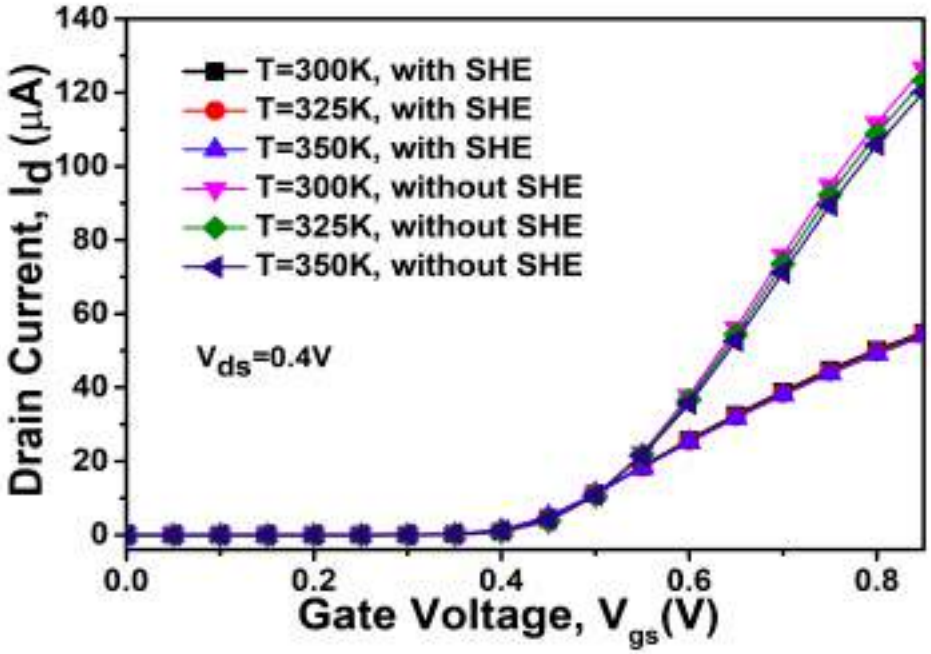

Figure 5.11: Influence of SHE on the transfer characteristics of HD-VS-FeFinFET at varying ambient temperatures

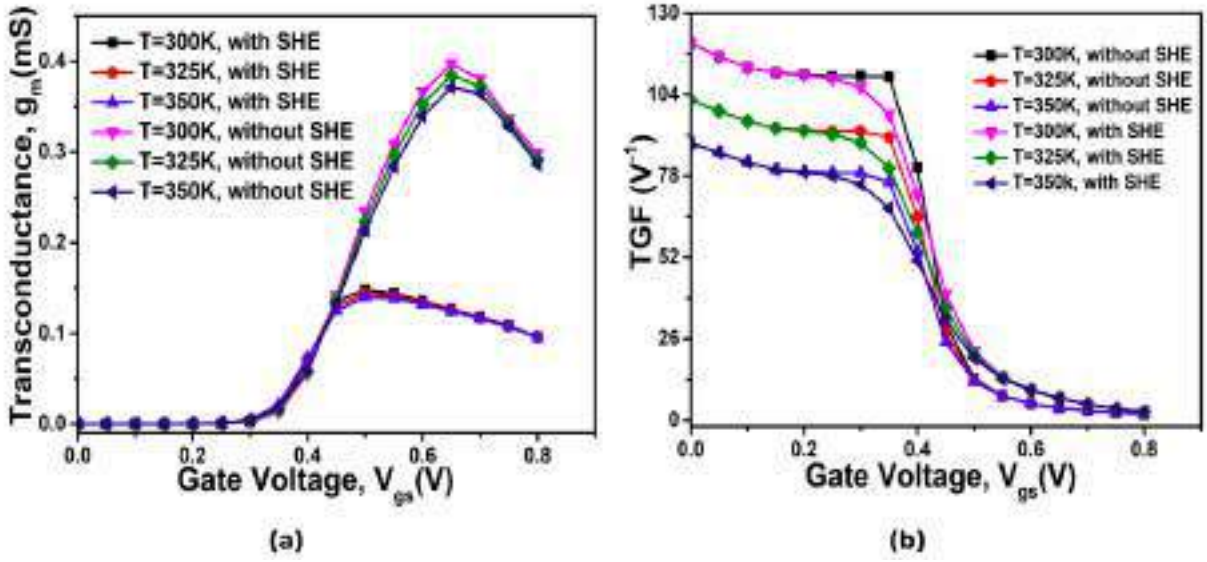

Figure 5.12: Influence of SHE on the (a) g_m (b) TGF for HD-VS-FeFinFET at varying ambient temperatures

Figure 5.12(a) shows the variation in transconductance at varying ambient temperature while comparing performance with and without SHE. With SHE, g_m is consistently lower as compared to g_m without SHE due to degrading carrier mobility with rise in local channel temperature. Moreover, the peak transconductance shifts towards lower V_{gs} under the influence of SHE because of early onset of strong inversion at lower V_{gs}. Further, at higher V_{gs}, self-heating becomes more pronounced due to higher power dissipation as a result of joule heating. This local heating causes thermal saturation effect where increased temperature leads to reduced mobility, but since the device is already thermally saturated, the impact of additional temperature rise becomes less significant. Figure 5.12(b) shows the influence of SHE on TGF at varying ambient temperatures. Firstly, it is observed that TGF is higher at lower temperature due to reduced phonon scattering and increased carrier mobility as compared to TGF at increasing temperature. Secondly, there is overlap of SHE and without SHE curve at lower V_{gs}. It is due to the fact that inversion layer in the channel is not strongly formed thus power dissipation is minimal, hence the effect of self heating. Similarly, the overlapping at higher V_{gs} occurs because local heating dominates and reaches thermal saturation, leading to similar mobility degradation across all conditions. In contrast, there is distinguishable difference between TGF curves with and without SHE in the middle region of V_{gs}, because the device transitions from weak to strong inversion, which activates SHE more prominently and significantly influences its performance. The parametric values of device characteristics under the influence of SHE at various ambient temperature are tabulated in Table 5.5.

Table 5.5: Summary of performance parameters at varying ambient temperatures considering SHE and without SHE

Parameter	with SHE			without SHE		
	T=300K	T=325K	T=350K	T=300K	T=325K	T=350K
I_{on} (A)	5.49×10^{-5}	5.44×10^{-5}	5.39×10^{-5}	1.27×10^{-4}	1.23×10^{-4}	1.20×10^{-5}
I_{off} (A)	2.36×10^{-13}	9.51×10^{-13}	3.15×10^{-12}	2.35×10^{-13}	9.50×10^{-13}	3.14×10^{-12}
I_{on}/I_{off}	2.33×10^{8}	5.72×10^{7}	1.71×10^{7}	5.38×10^{8}	1.30×10^{8}	3.82×10^{7}
g_m (S)	1.48×10^{-4}	1.44×10^{-4}	1.40×10^{-4}	3.97×10^{-4}	3.84×10^{-4}	2.60×10^{-2}
TGF (V^{-1})	1.20×10^{2}	1.02×10^{2}	8.85×10^{2}	1.20×10^{2}	1.02×10^{2}	2.17×10^{2}

While self-heating introduces performance challenges, the device still demonstrates strong operational stability at lower and higher gate biases. With its enhanced mobility benefits and manageable self-heating impact through optimized design and thermal strategies, this device structure

holds significant promise for reliable, high-performance applications across varying ambient temperatures.

5.4.4 Circuit Level Analysis of HD-VS-FeFinFET based CMOS inverter for the characteristics performance parameters under varying biasing voltages and ambient temperatures

In this section, the performance analysis is done for HD-VS-FeFinFET based CMOS inverter to understand its behavior under varying operational conditions, which is very crucial for modern low-power and high-speed circuit designing. Key performance parameters such as Voltage Transfer Characteristic (VTC), propagation delay, switching current, rise time, and fall time directly govern the inverter's reliability and efficiency for digital applications. This study focuses on evaluating these parameters at different ambient temperatures and various biasing voltages to assess thermal stability and voltage scalability for this CMOS inverter.

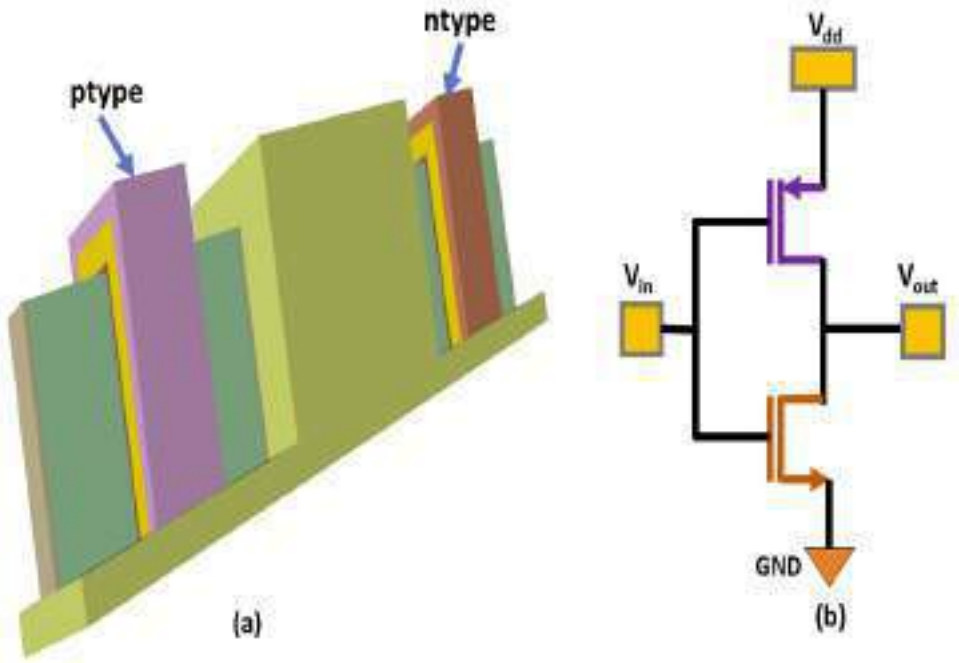

Figure 5.13: (a) 3D structure and (b) Schematic diagram of HD-VS-FeFinFET based CMOS inverter

For this, a required setup is designed with Cogenda Visual TCAD simulator with n-channel and p-channel HD-VS-FeFinFET isolated electrically with the help of 60 nm SiO_2 spacer. Figure 5.13(a) and Figure 5.13(b) respectively shows the 3D view and schematic of the CMOS inverter circuit

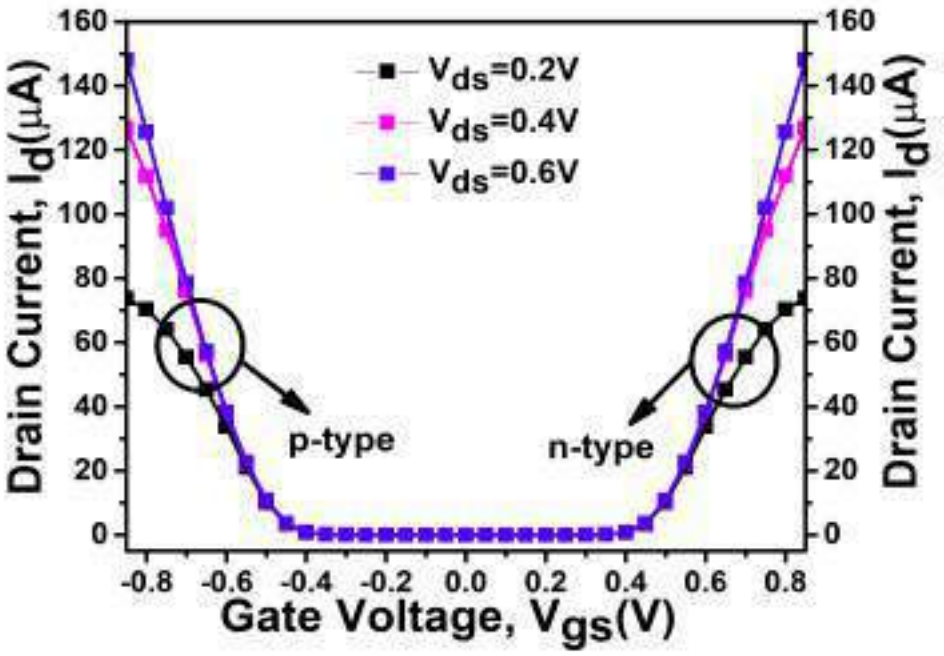

Figure 5.14: Influence of varying biasing voltage on threshold voltage matching curve for HD-VS-FeFinFET based CMOS inverter

where V_{dd}, V_{in}, and V_{out} are the supply voltage, input voltage and output voltage respectively. Initially threshold matching is done for both the n-channel and p-channel HD-VS-FeFinFET to make optimized device-based CMOS inverter as displayed in Figure 5.14 and Figure 5.15 for varying biasing voltage and varying ambient temperature respectively. The V_{gs} is varied from -0.85 V to 0.85 V with dual work function metal (DWFM) integration scheme, which employs two different gate metals with distinct work functions such that low for nMOS and high for pMOS, to independently tune their threshold voltages.

The variation in VTC curve with variation in biasing voltages is showcased in Figure 5.16(a). It is visible from the figure that as supply voltage decreases, the switching threshold voltage moves towards the lower input voltage because the available gate overdrive voltage for both the n-type device and p-type device reduces which causes both the transistors to switch more slowly and the point where their current equalize shifts towards to a lower voltage. Figure 5.16(b) showcases the trend of switching current for varying biasing voltage. It follows the same trend with peak of I_{sc} shifts leftward as the peak switching current occurs near the inverter's switching threshold voltage. Also with a lower supply voltage, the transistors operate in a more resistive region which limits the peak current in switching transitions as the curve almost flattens for V_{dd}=0.4V. This behavior indicates that the device can maintain controlled switching currents even at reduced supply voltages,

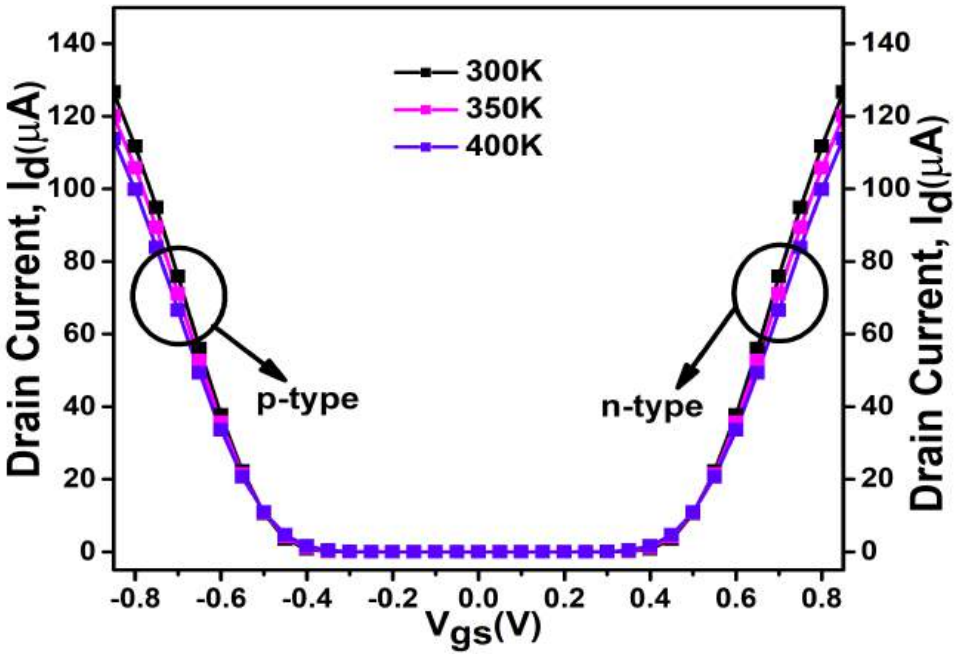

Figure 5.15: Influence of varying ambient temperature on threshold voltage matching curve for HD-VS-FeFinFET based CMOS inverter

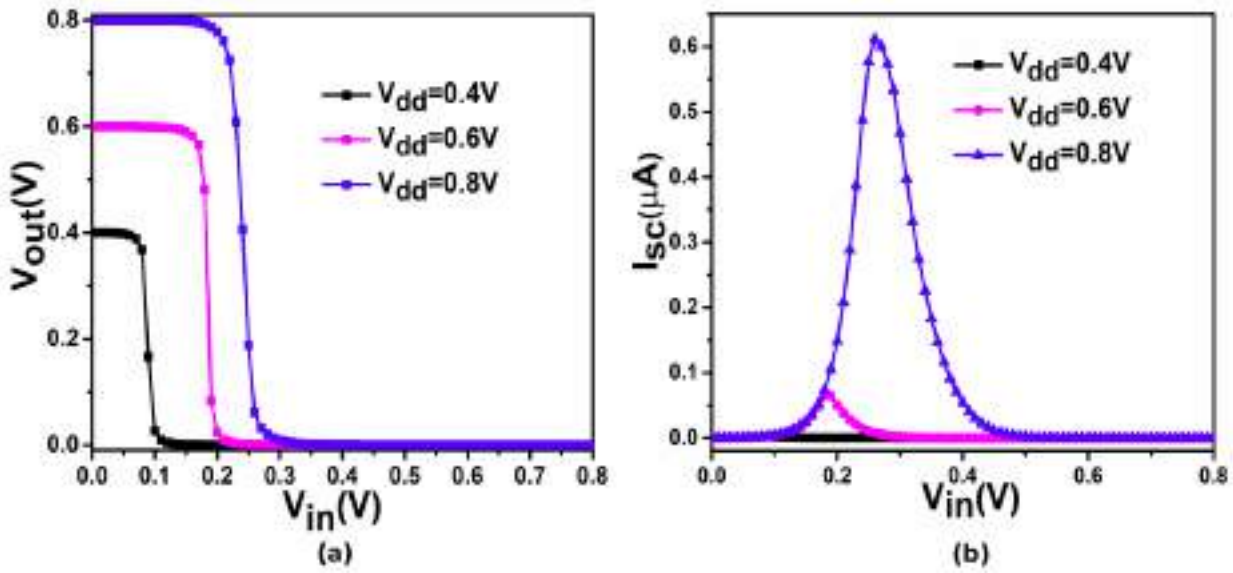

Figure 5.16: Impact of varying biasing voltage on (a) Voltage Transfer Characteristics and (b) Switching Current of HD-VS-FeFinFET based CMOS inverter

highlighting its potential for low-power, high-efficiency digital circuit applications.

Further, the variation in VTC curve with variation in ambient temperature is showcased in Figure 5.17(a) shows the rightward shift of approximately 34.627mV in switching threshold voltage of the inverter as the ambient temperature is increased from 300K to 400K. The rightward shift indicates that the inverter requires a slightly higher input voltage to switch at elevated temperatures,

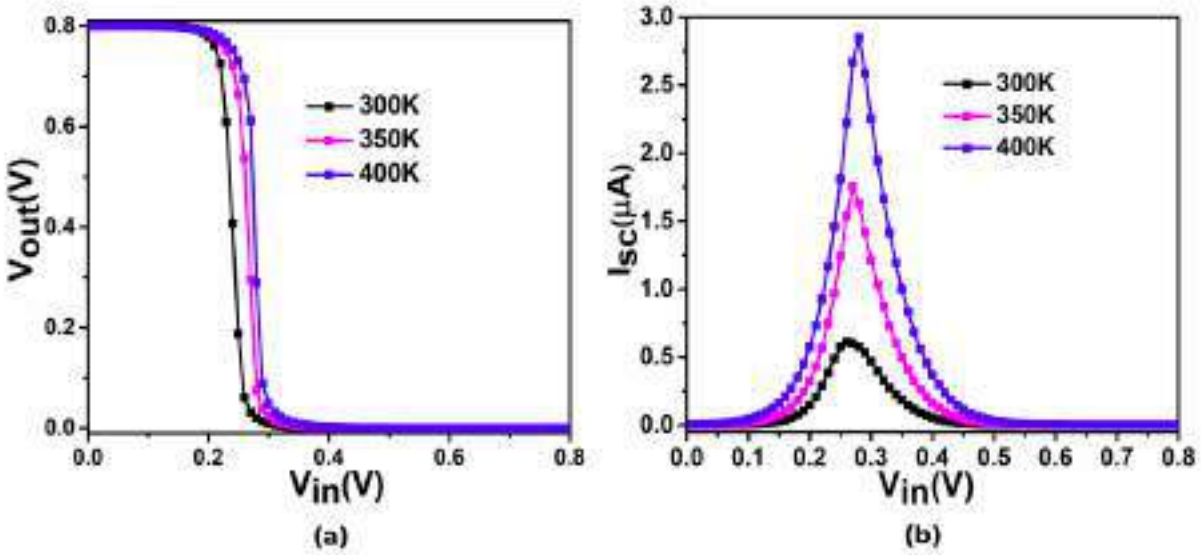

Figure 5.17: Impact of varying ambient temperature on (a) Voltage Transfer Characteristics and (b) Switching Current of HD-VS-FeFinFET based CMOS inverter

primarily due to reduced carrier mobility and altered threshold voltage of the transistors. Then, Figure 5.17(b) showcases the trend of switching current for varying ambient temperature. There is rightward shift in peak of switching current (I_{sc}) along with increase upto 4.66 times as the temperature is increased to 400K. This increase in switching current can be attributed to enhanced subthreshold leakage and thermally activated carriers, which contribute to higher current flow during the switching transition at elevated temperatures. Such behavior can be exploited in temperature-sensitive sensing applications or adaptive circuits, where a predictable increase in switching current with temperature can improve responsiveness and circuit functionality(SZV+13b; SSCS10).

Further, in case of FET based CMOS inverters, various non idealities comes into picture, one of them is parasitic capacitances. These intrinsic capacitances existing between the device terminals, introduce delay in voltage transition from low to high or from high to low, thus limiting the switching speed of the inverter(NLR02; MTS22; MTS22). Subsequent analysis cover how these non idealities impact the inverter's timing performance under varying ambient temperature. For this, a step voltage is applied at the input terminal of the inverter and resulting output waveform of this logic circuit is analysed as shown in Figure 5.18. Subsequently, propagation delay, which is defined as the time taken by the output to respond to an input change, is taken into account for studying the transient analysis as it affects the overall speed of logic circuits. Two propagation delay components namely high to low propagation delay (t_{pHL}) and low to high propagation delay (t_{pLH}) are analysed

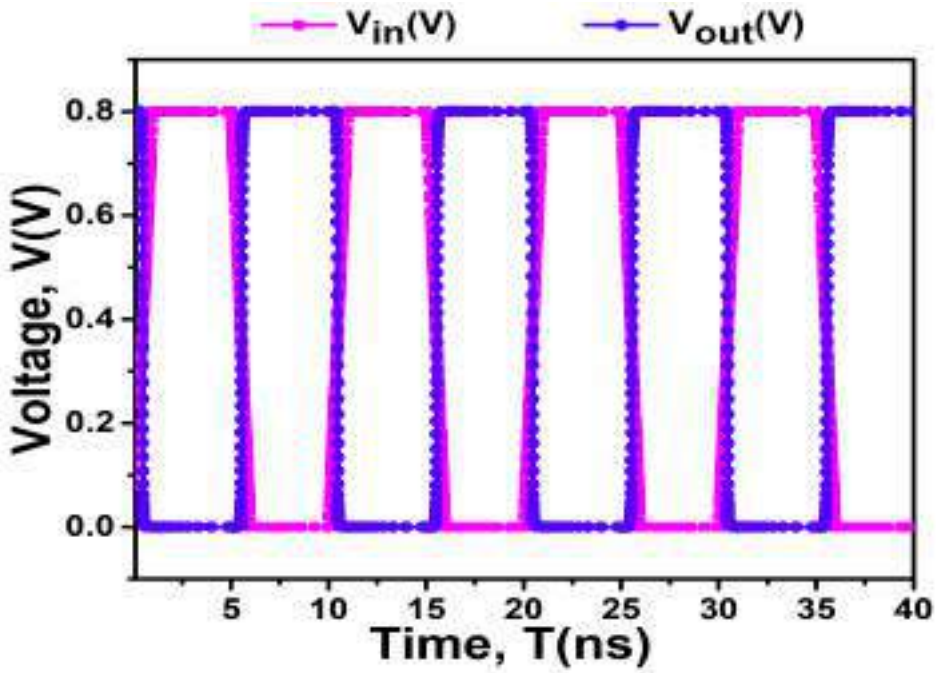

Figure 5.18: Output transition waveform of the HD-VS-FeFinFET based CMOS inverter

under varying ambient temperature, as showcased in Figure 5.19(a). t($_{pHL}$) and (t$_{pLH}$) represent the time taken by the output voltage to transit from V_{OH} (Output High Voltage) to (V_{OH} + V_{OL})/2, and from V_{OL} (Output Low Voltage) to (V_{OH} + V_{OL})/2, respectively(MTS22). It can be observed from the figure that as the temperature increasing, both the components of propagation delay are decreasing as shown in figure. This behavior is attributed to mobility degradation of charge carriers at elevated temperatures, which slows down the charging and discharging of parasitic capacitances. Additionally, increased threshold voltage shifts and enhanced leakage currents at higher temperatures further contribute to longer switching times.

Similarly, transition time factors such as rise and fall time of the inverter are also analysed to understand the response time and sharpness of the inverter. Rise time (t$_r$) is defined as the time interval during which the output signal rises from 10% to 90% of the voltage difference between V_{OH} and V_{OL}. Similarly, fall time (t$_f$) represents the time interval over which the output signal falls from 90% to 10% of the (V_{OH} - V_{OL}) voltage range(GGYE15). These parameters serve as key indicators of how quickly the inverter transitions between logic states. Figure 5.19(b) shows that as the temperature increases, there is increase in both t$_r$ and t$_f$. This is primarily due to enhanced phonon scattering which slows down the rate at which output node charges and discharges and thus requiring more time for the output voltage to make transition between logic levels. These

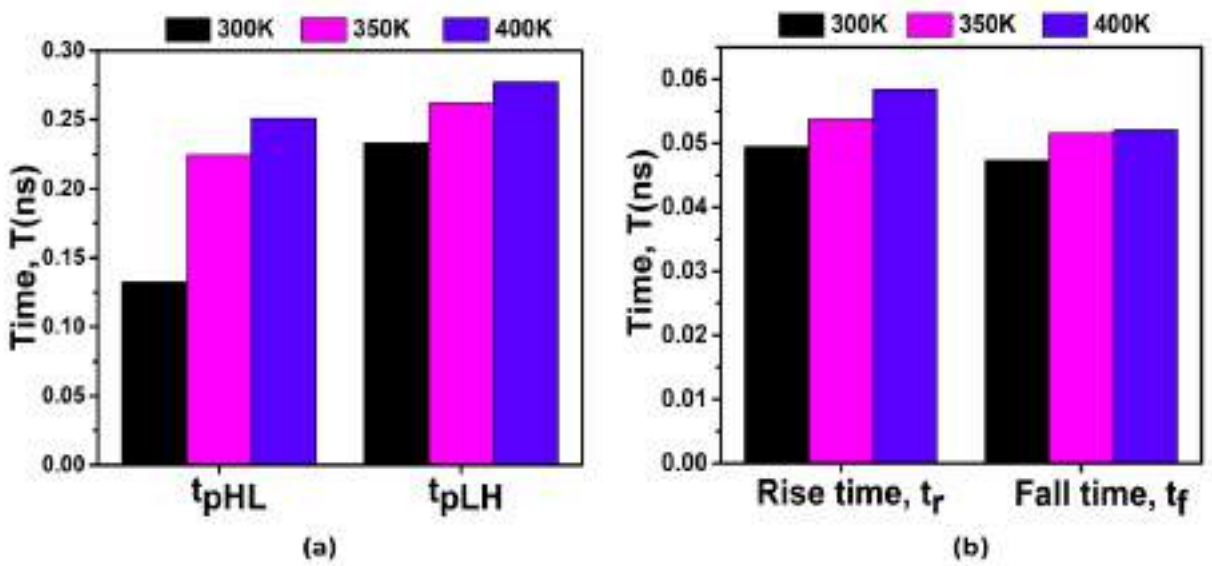

Figure 5.19: Influence of ambient temperature on (a) high to low propagation delay and low to high propagation delay (b) rise time and fall time of HD-VS-FeFinFET based CMOS inverter

slower transitions (increased t_r and t_f) observed at higher temperature can reduce the likelihood of signal glitches or false triggering due to high-frequency noise, thus enhancing the circuit reliability in noisy or thermally stressed environments.

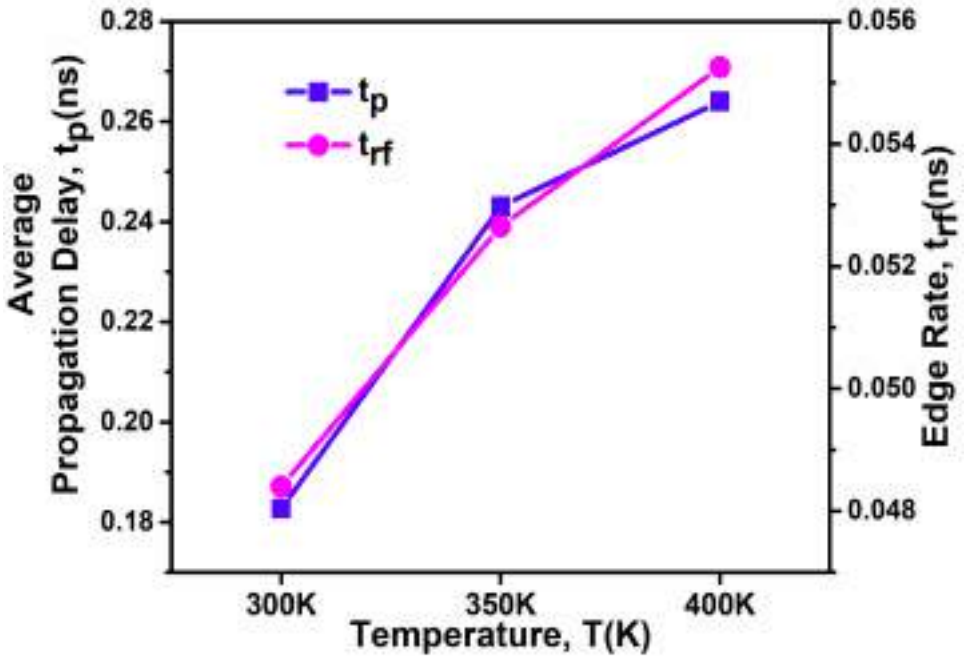

Figure 5.20: Imapact of ambient temperature on Propagation delay and Edge Rate of HD-VS-FeFinFET based CMOS inverter

Later, Figure 5.20 displays the variation in average propagation delay (t_p), calculated as the mean of t_{pHL} and t_{pLH}, along with the edge rate (t_{rf}) defined as the mean of t_r and t_f, across

different ambient temperatures(GGYE15; SSCS10). Both t_p and t_{rf} increase with rising temperature, reflecting a reduction in transition sharpness due to decreased carrier mobility and increased scattering in the channel. Despite this thermal effect, understanding the temperature dependence of propagation delay and edge rate is valuable for designing thermally robust circuits. Such insights can be exploited to optimize device performance for high-speed and reliable digital applications under varying operating temperatures. Performance parameters of HD-VS-FeFinFET based CMOS inverter under the influence of varying ambient temperature are also tabulated in Table 5.6.

Table 5.6: Performance parameters of HD-VS-FeFinFET based CMOS inverter under the influence of varying ambient temperature

Parameter	T=300K	T=350K	T=400K
t_{phl} (ns)	0.132	0.224	0.251
t_{plh} (ns)	0.233	0.262	0.277
t_p (ns)	0.183	0.243	0.264
t_r (ns)	0.049	0.053	0.058
t_f (ns)	0.047	0.051	0.052
t_{rf} (ns)	0.048	0.052	0.055

5.5 Summary

This study presents a comprehensive multiscale analysis connecting the impact of dopant material on ferroelectric HfO_2 at the atomic level with DFT calculation and at the device level. The analysis concludes that increasing negative value of ferroelectric landau parameter such as alpha and beta improves the performance characteristics of the device with 24% rise in I_{on} and 77.4 % reduction in leakage current in case of silicon dopant material (D1) over lanthanum dopant material (D6) due to enhanced surface potential modulation in the channel. Further, the two best dopant material structures Si doped HfO_2 and Gd doped HfO_2 found at device level, are analysed microscopically using DFT calculations with comparison in their band structure and PDOS. The impact of increasing dopant material concentration in Si doped HfO_2 is also studied which confirms that with less direct bandgap and dense projected density of states, doubly silicon doped HfO_2 have outperformed all the four considered structural configurations. Subsequently, considering the cruciality of thermal robustness, the present study also addresses the critical impact of self-

heating effects (SHE) at varying biasing voltages and ambient temperatures, particularly in the context of Si-doped HfO_2-based FeFinFETs. It is observed that there is significant impact of SHE on drain characteristics of the device but it is very much dependent on region of operation of the device such as g_m and TGF respectively show minimal degradation in subthreshold region as 4.11% and 3.33% at V_{ds}=0.4V but with the onset of inversion, significant degradation can be observed with 36.6% in g_m and 39.7% in TGF. Further, the exploration about how temperature rise, combined with self-heating, alters the device characteristics reveals that the peak g_m shifts towards lower V_{gs} along with flattening of TGF under the influence of SHE, due to the early onset of strong inversion at lower V_{gs}. Further, at higher V_{gs}, impact of additional temperature rise becomes less significant since the device is already thermally saturated as can be visible with the overlapping curves of TGF at different temperatures in contrast to variation of visible at lower V_{gs}. In continuation, HD-VS-FeFinFET based CMOS inverter is examined to understand the effect of biasing voltages and ambient temperature on key performance parameters such as voltage transfer characteristic, propagation delay, switching current, rise time, and fall time to govern the inverter's reliability and efficiency for digital applications. With improved transition time by 12.4% and reduced propagation delay by 30.8% at 300K, the inverter the demonstrates enhanced switching efficiency and faster signal propagation at lower temperature. Additionally, at reduced biasing voltages, the inverter maintains controlled switching currents, underscoring its suitability for low-power applications. Conversely, elevated temperatures induce a predictable shift in switching threshold and an increase in switching current, which can be leveraged for temperature-sensitive and adaptive circuit designs. Overall, the device exhibits promising potential for energy-efficient and environment-adaptive digital applications. Together, these characteristics suggest that, with appropriate voltage scaling and thermal management, the circuit can leverage temperature-driven switching behavior to achieve enhanced speed and performance in next-generation low-power, high performance logic circuit applications.

Furthermore, the next chapter serves as the culmination of the research done in the thesis and provides an outlook on potential future developments regarding the proposed solutions.

Chapter 6

Conclusion, Future Scope and Social Impact

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* This chapter provides a summary of the research conducted in this thesis. In addition, the conclusions generated from the results are highlighted briefly.
* Further, the chapter discusses about the potential future work that may be done to expand this research.
* Later, this chapter also discusses the social impact of the research and its potential benefits to society.

6.1 Summary

The rapid growth of technologies such as logic-in-memory computing, smart devices, and Internet of Things (IoT) has intensified the demand for low-power, high-performance electronics. While Complementary Metal-Oxide-Semiconductor (CMOS) scaling has driven progress, it now faces fundamental limits due to short channel effects (SCEs) like gate leakage, Drain-Induced Barrier Lowering, and dopant-induced variability. To address these challenges, several device architectures have been explored, among which the Ferroelectric FinFET (FeFinFET) stands out. By integrating ferroelectric materials with FinFETs, FeFinFETs combine strong electrostatic control with

electrically tunable polarization charges. This synergy not only mitigates SCEs but also enhances charge controllability and device performance, positioning FeFinFETs as a promising candidate for next-generation electronic devices.

In this thesis, a strained Vertically Stacked FeFinFET (VS-FeFinFET) architecture is extensively investigated, as it enables aggressive device scaling and enhanced performance. Moreover, to overcome various challenges faced by conventional FeFinFET, different engineering schemes have also been incorporated in VS-FeFinFET. The integration of Silicon-on-Insulator (SOI) technology (substrate engineering) with FeFinFET improves electrostatic control, suppresses parasitic capacitance, and enhances energy efficiency. To further mitigate SCEs, advanced channel materials such as strained Si/SiGe (strain engineering/channel engineering) have been explored, combinedly forming heterostructure on insulator, resulting in Vertically Stacked Heterostructure on Insulator Ferroelectric based FinFET (VS-HOI-FeFinFET) as developed in **Chapter 2**, which demonstrates superior performance over conventional FeFinFETs. In this regard, initially in **Chapter 2**, performance of FeFinFET and VS-HOI-FeFinFET is compared for different performance parameters and it is found that VS-HOI-FeFinFET performed better in comparison to FeFinFET on all examined parameters. Later, **Chapter 2** discusses the extensive analysis done to optimize VS-HOI-FeFinFET for achieving high performance analog and RF applications. As continued scaling introduces challenges like increased gate tunneling current and leakage due to thinner oxides, which high-k dielectrics can address, but direct implementation of high-k dielectric over semiconductor layer creates the issues of interface quality and instability. Thus, a gate stack (GS) approach, incorporating a thin low-k interfacial layer between silicon and the high-k dielectric, is used to alleviate these limitations (gate engineering). Considering these factors, the proposed VS-HOI-GS-FeFinFET with a strained tri-layered heterostructure channel has been developed as a robust solution, combining ferroelectric integration, SOI isolation, strain engineering, and GS architecture for enhanced performance and scalability. Thus, VS-HOI-FeFinFET is further analysed for gate stacked configuration for different gate stacked dielectric materials. The combinations taken for gate oxide stacking in different configurations are C1(SiO_2+Al_2O_3), C2(SiO_2+HfO_2), C3(Al_2O_3), and C4(Al_2O_3+HfO_2). In subsequent parts, this chapter presents the study of VS-HOI-GS-FeFinFET to optimize the gate stack material for upgraded static, analog, and RF performance. The C4 configuration exhibits the most enhanced performance as compared to other three configurations. In comparison to C1, C4 shows

an increase in I_{on} by 26.91% and reduction in I_{off} by 78.4% thus results in significant increment in switching ratio. Further, an increment in peak transconductance by 50.42% is observed in C4 over C1 along with improved subthreshold swing with reduction by 6.86%. As compared to C1, device efficiency (TGF) and V_{th} are also enhanced in C4 configuration by 17.58% and 7.69%. Other analog parameters such as A_V, V_{EA} and R_{out} also shows remarkable improvement in C4 with increment by 308.23%, 105.64% and 204.45% respectively as compared to C1. Also, performance optimization of VS-HOI-GS-FeFinFET with variation in mole fraction of germanium, geometric dimensions of Fin, thickness of ferroelectric layer and oxide layer is also explored for various analog metrics. Further, RF parameters like GFP also gets enhanced by 233.33% and GTFP by 279.80% for C4 over C1 configuration. Along with these parameters, improved ability of C4 for enhanced amplification with minimum distortion is depicted by increased gate capacitance and reduced unity gain cut off frequency by 138.21% and 16.33% respectively over C1, makes the device suitable for high performance analog and RF applications.

The results of this multi-faceted optimization highlight the potential of the VS-FeFinFET as a high-performance, energy-efficient device architecture that successfully addresses several limitations of conventional CMOS scaling. However, while these enhancements highlight the potential of the device under ideal conditions, a comprehensive evaluation also requires addressing its reliability under practical operating scenarios. In particular, the role of interfacial trap charges (ITCs) at the semiconductor–oxide boundary becomes critical, as these traps are unavoidable in real devices and can influence threshold stability, switching behavior, and long-term performance. Thus, having established its optimized static and dynamic performance, it becomes imperative to investigate the reliability of the device under ITC-induced effects, ensuring its robustness for future applications in advanced electronic systems. By incorporating gate engineering and developing hetero dielectric vertically stacked ferroelectric based FinFET (HD-VS-FeFinFET), the study not only mitigates the adverse effects of ITCs but also demonstrates significant improvements in analog, linearity, and circuit-level performance. This transition from geometry-driven optimization to reliability-centric design completes the continuum of work, establishing a holistic framework that ensures both high performance and robust functionality of the device. Thus, **Chapter 3** presented a comprehensive assessment from device to circuit level showing the influence of ITCs on various analog, linearity, and distortion parameters of HD-VS-FeFinFET. The strained channel system and

gate engineering modify the band structure and increase the carrier mobility thus improving the transistor's performance and making it more desirable for many electronic applications. The process improves the device performance in terms of various metrics such as I_{on}, I_{off}, V_{th}, g_m, VIP2, VIP3, IIP3, IMD3, 1-dB compression point, and harmonic distortion parameters. At the device level, HD-VS-FeFinFET outperforms VS-FeFinFET with improvement in various analog parameters like A_v by 27 times, V_{EA} by 7.5 times, and R_{out} by 23 times along with minimal average variations of 11.15%, 3.03% and 11.39% respectively in contrast to 45.73%, 14.24% and 42.48% for VS-FeFinFET under the influence of ITCs. Thus, the heterogeneous dielectric engineering approach effectively strengthens device immunity against ITCs, leading to enhanced performance and reliability for advanced nanoelectronic applications. Further, circuit level comparison has also been made for CMOS inverter and it is found that HD-VS-FeFinFET based inverter offers improved performance in terms of noise margin, I_{sc}, and transition range along with more tolerance against ITCs. With the comprehensive analysis done on the intricacies of ITCs from device to circuit level, this work provides insights into the development of HD-VS-FeFinFET with enhanced functionality, reliability, and performance, poised to shape the landscape of modern electronics.

The investigations clearly established that the proposed HD-VS-FeFinFET exhibits remarkable improvements in device and circuit performance under the influence of ITCs. Despite these encouraging outcomes, the analysis in **Chapter 3** was limited to nominal operating conditions and assumed ITCs to be static. In reality, ITCs exhibit temperature-sensitive dynamics due to thermally activated carrier capture and emission processes. Additionally, ITC's density and polarity strongly affect device reliability, leading to threshold voltage shifts, variations in transconductance, and distortions in device performance. Therefore, a realistic evaluation of device robustness requires an in-depth investigation of ITCs under different temperatures, densities, and polarities. Thus, **Chapter 4** presented a comprehensive analysis from device to circuit level to encompass the reliability of HD-VS-FeFinFET in terms of : 1) temperature affectability on impact of ITCs to understand their effect at various operating temperatures, 2) impact of ITCs density with different polarity, over various figure of merits. Results demonstrate that HD-VS-FeFinFET has better immunity against ITCs with minimun variation at all considered operating temperatures such as average variation of 0.6% in I_{on} at 300K and 0.64% in I_{on} at 400K in contrast to variation shown by VS-FeFinFET like 3.5% in I_{on} at 300K and 4% in I_{on} at 400K. Further, the study done to analyze the impact of ITCs

density and polarity reveals that device performance alters significantly with rising density of ITCs for both PITC(NITC) but this deviation is very much less in HD-VS-FeFinFET with 4.3%(5.45%) in I_{on}, and 6.56% (5.46%) in V_{th} for PITC(NITC) in comparison to 21.3%(38.7%) in I_{on} and 59.69% (56.65%) in V_{th} for VS-FeFinFET. Further, the extensive performance analysis done at circuit level for HD-VS-FeFinFET based CMOS inverter under the influence of ITCs at various operating temperatures confirmed its improved immunity towards ITCs and makes it an ideal choice for advanced digital circuits and low-power electronic applications. Thus, this study highlights how HD-VS-FeFinFET maintains high reliability and performance under coupled thermal and trap dynamics, establishing it as a robust and efficient candidate for CMOS inverter applications in increasingly demanding and dynamic environments of the future.

While these analyses provided an in-depth exploration of the reliability of HD-VS-FeFinFETs under the coupled influence of temperature variations, ITCs and their polarity/density effects, a critical gap remains since the evaluation does not sufficiently account for the fact that device performance and reliability are not solely governed by interface phenomena but are equally dependent on the intrinsic material properties of the ferroelectric layer. Since the ferroelectric HfO_2 layer forms the core of polarization charges and switching, its structural, electronic, and thermal characteristics directly dictate the overall efficiency and stability of the device. Hence, to establish a more fundamental and holistic understanding, it becomes essential to extend the investigation from interface-related reliability concerns to the intrinsic material-level properties and their translation into device and circuit performance. Therefore, **Chapter 5** shifts the focus towards a comprehensive investigation of ferroelectric HfO_2-based devices, incorporating both atomic-level (through DFT-based analysis of dopants and structural modifications) and device-level (through performance characterization under varying conditions) perspectives. This transition allows for a deeper understanding of how dopant engineering, thermal effects, and self-heating mechanisms influence the electrical behavior of HD-VS-FeFinFETs and their circuit-level applications. By bridging the gap between interface-driven reliability issues and intrinsic material-driven performance modulation, this chapter builds a coherent pathway towards the optimized design of robust, energy-efficient, and scalable ferroelectric devices for next-generation electronic systems. This study presents a comprehensive multiscale analysis connecting the impact of dopant material on ferroelectric HfO_2 at the atomic level with DFT calculation and at the device level. The analysis concludes that

increasing negative value of ferroelectric landau parameter such as alpha and beta improves the performance characteristics of the device with 24% rise in I_{on} and 77.4% reduction in leakage current in case of silicon dopant material (D1) over lanthanum dopant material (D6) due to enhanced surface potential modulation in the channel. Further, the two best dopant material structures Si doped HfO_2 and Gd doped HfO_2 found at device level, are analysed microscopically using DFT calculations with comparison in their band structure and PDOS. The impact of increasing dopant material concentration in Si doped HfO_2 is also studied which confirms that with less direct bandgap and dense projected density of states, doubly silicon doped HfO_2 have outperformed all the four considered structural configurations. Subsequently, considering the cruciality of thermal robustness, the present study also addresses the critical impact of self-heating effects (SHE) at varying biasing voltages and ambient temperatures, particularly in the context of Si-doped HfO_2-based FeFinFETs. It is observed that there is significant impact of SHE on drain characteristics of the device but it is very much dependent on region of operation of the device such as g_m and TGF respectively show minimal degradation in subthreshold region as 4.11% and 3.33% at V_{ds}=0.4V but with the onset of inversion, significant degradation can be observed with 36.6% in g_m and 39.7% in TGF. Further, the exploration about how temperature rise, combined with self-heating, alters the device characteristics reveals that the peak g_m shifts towards lower V_{gs} along with flattening of TGF under the influence of SHE, due to the early onset of strong inversion at lower V_{gs}. Further, at higher V_{gs}, impact of additional temperature rise becomes less significant since the device is already thermally saturated as can be visible with the overlapping curves of TGF at different temperatures in contrast to variation of visible at lower V_{gs}. In continuation, HD-VS-FeFinFET based CMOS inverter is examined to understand the effect of biasing voltages and ambient temperature on key performance parameters such as voltage transfer characteristic, propagation delay, switching current, rise time, and fall time to govern the inverter's reliability and efficiency for digital applications. With improved transition time by 12.4% and reduced propagation delay by 30.8% at 300K, the inverter the demonstrates enhanced switching efficiency and faster signal propagation at lower temperature. Additionally, at reduced biasing voltages, the inverter maintains controlled switching currents, underscoring its suitability for low-power applications. Conversely, elevated temperatures induce a predictable shift in switching threshold and an increase in switching current, which can be leveraged for temperature-sensitive and adaptive circuit designs. Overall, the

device exhibits promising potential for energy-efficient and environment-adaptive digital applications. Together, these characteristics suggest that, with appropriate voltage scaling and thermal management, the circuit can leverage temperature-driven switching behavior to achieve enhanced speed and performance in next-generation low-power, high performance logic circuit applications.

Ultimately, this work paves the way for an optimized ferroelectric device design by uniting interface reliability and material-driven performance modulation, delivering robust, scalable, and energy-efficient solutions for high-performance analog and circuit applications.

6.2 Future Work

The main goal of this thesis is to create a Si/SiGe strained VS-FeFinFET device that can overcome the constraints of conventional FETs. Yet all goals are largely achieved through the use of sophisticated Technology Computer-Aided Design (TCAD) and simulations. Nevertheless, given the existing work, it may be worthwhile to explore and refine the following aspects as future directions.

1. The circuit behavior of the VS-FeFinFET can be explored to make the proposed device suitable for other digital circuit applications such as DRAM, SRAM, and other gated logic designs.

2. This study can be extended to model process-induced variability in VS-Fe-FinFETs, particularly focusing on the influence of sidewall spacers and the effect of random dopant fluctuations (RDF) on device performance.

3. Furthermore, exploring 2D materials as alternative channel materials is promising because of their high carrier mobility. Such advancements can enhance the suitability of the proposed device for high-speed applications, including next-generation high-frequency communication systems.

4. Various environmental based sensors such as hydrogen, oxygen and various gas sensor may also be made with VS-FeFinFET to measure and identify potentially dangerous substances floating in the environment.

5. Moreover, a biosensor may also be designed with VS-FeFinFET to effectively identify and measure viruses such as influenza, HIV, and SARS-CoV-2.

6.3 Social Impact

The proposed research carries significant social impact by enabling the development of energy efficient and reliable device, with a particular focus on analog and circuit applications that form the foundation of modern electronic systems. The strained VS-FeFinFET device reduces power dissipation while maintaining high switching speeds, supporting high-performance, low-power operation that is critical for VLSI and next-generation electronic applications. These improvements contribute to sustainable and environmentally responsible technology, helping to lower the overall carbon footprint of electronic systems. Reliability is further enhanced through material and device-level engineering that mitigates ITCs effects, ensuring stable and predictable device operation under practical conditions. This robustness benefits analog, RF, and digital systems, which form the backbone of communication, computation, and emerging smart technologies. The low-power characteristics of the VS-FeFinFET make it particularly suitable for energy-constrained applications, including IoT devices, wearable electronics, and healthcare systems, where long device lifetimes and minimal maintenance are essential. By integrating ferroelectric HfO_2-based materials with scalable FinFET structures, the work bridges fundamental device-level innovations with practical circuit-level benefits, fostering technological advancement that is both sustainable and socially impactful. Overall, the research paves the way for eco-friendly, high-performance electronics, promoting inclusivity, societal progress, and climate-conscious technological growth.

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PAPER

Optimization and analysis of Si/SiGe strained vertically stacked heterostructure on insulator FeFinFET for high performance analog and RF applications

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Abstract

As semiconductor technology advances, the exploration of novel materials and device architectures becomes imperative to meet the growing demands of integrated circuits for analog and radio-frequency (RF) applications. In this paper, various advanced technologies have been amalgamated such as integration of ferroelectric layer in multigate FinFET along with the adaptation of SOI technology. Further strain technology is also used which employs a tri-layered strained-silicon channel system with the help of SiGe to form Vertically Stacked Heterostructure on Insulator Ferroelectric based FinFET (VS-HOI-FeFinFET) and on comparison with baseline FeFinFET, it is found to show remarkable improvements in terms of various measured parameters such as drain current, switching ratio, threshold voltage and subthreshold swing. Subsequently, gate stacking architecture is incorporated in VS-HOI-FeFinFET to further optimize the device performance. The four different configurations C1 to C4 are taken in terms of four different combinations of gate stack materials considered for gate oxide such as C1(SiO_2+Al_2O_3), C2(SiO_2+HfO_2), C3(Al_2O_3), and C4(Al_2O_3+HfO_2). It is found that the static and analog performance of VS-HOI-GS-FeFinFET enhance sequentially from configuration C1 to C4 such as switching ratio is enhanced upto around 5 times, DIBL and quality factor are improved by around 41% and 58% respectively along with significant improvement in device efficiency, early voltage, intrinsic gain, output conductance and output resistance. Subsequently performance optimization of VS-HOI-GS-FeFinFET with variation in mole fraction of germanium is also explored for various analog metrics. Further, several RF parameters are also explored and it is observed that the gain frequency product (GFP) and gain transconductance frequency product (GTFP) are augmented by around three times in magnitude along with 16% reduction in the unity gain cut off frequency in C4 configuration, exhibiting its ability of high frequency amplification with minimized noise distortion thus makes the device suitable for various high performance Analog and RF applications.

1. Introduction

Advancement in technology such as logic in memory (LiM) computing, mobile smart devices and Internet of things have led to increasing demand for low power and high-performance electronic devices [1]. To meet the growing demands, Devices under CMOS technology are being aggressively scaled down and are reaching their fundamental limits. At submicron dimensions, short channel effects (SCEs) such as gate leakage current, drain induced barrier lowering (DIBL), and fluctuation of device characteristics due to random channel dopant, start dominating and deteriorates the device performance [2]. To overcome these limitations, different device designs and engineering schemes are reported in literature such as Dual Gate, Trigate FinFET, Recessed channel, FeFETs etc [3, 4].

Among these structures, FeFinFET is considered as a promising contender for ultimate CMOS device structure because the device has robustness against short channel effect (SCE) and improved overall transistor performance [5]. The concept to tune the conductivity of surface of semiconductor by adopting the ferroelectric material was showcased for the first time in 1957. The n-channel FeFET was successfully demonstrated at Research laboratory by Shu-Yau We *et al* for the first time in Pittsburgh in 1974 with Bismuth Titanate ($Bi_4Ti_3OI_2$) ferroelectric film [6]. The Ferroelectric FinFET represents a paradigm shift in the realm of electronic devices, blending the advantages of FinFET technology with the unique properties of ferroelectric materials [7]. Traditional FinFETs have long been the backbone of modern semiconductor manufacturing, delivering superior control over electronic channels [8]. However, the introduction of ferroelectricity introduces an additional dimension, allowing for non-volatile memory capabilities and unprecedented control over the transistor's state [9, 10]. When combined with the advantages of Silicon-on-Insulator (SOI) technology, which involves placing a thin layer of insulating material beneath the transistor channel, the resulting SOI FeFinFET mitigates the adverse effects of parasitic capacitance and reduces the susceptibility to various short-channel effects [11, 12]. This isolation enhances the transistor's electrostatic control, enabling more efficient switching and reducing power consumption which is a critical requirement in the era of energy-efficient computing [12, 13].

To further improve the performance of SOI FeFinFET and to minimize the short channel effects, there is need to go beyond silicon channel materials such as SiGe, GaAs, and group III-IV materials [14]. The performance of Vertically Stacked Ferroelectric based FinFET using a compound semiconductor material (SiGe) with a strained-silicon channel system has been analysed in previous work and it is found that the device, Vertically Stacked Ferroelectric based FinFET shows improved SCEs and can be further scaled down compared to FeFinFET [15]. Strained silicon is a form of silicon where the silicon atoms are stretched or compressed out of their natural lattice positions. This is usually achieved by placing a layer of silicon along with another material with a slightly different lattice constant, such as silicon-germanium (SiGe). The mismatch between the lattice constants causes the silicon atoms to either stretch or compress, depending on another material. To develop strain in the channel region in VS-HOI-FeFinFET, a SiGe layer is sandwiched between two silicon layers. Straining the silicon changes the energy band structure, which reduces the effective mass of the charge carriers (electrons and holes). This allows them to move faster, increasing the mobility of the carriers. Higher mobility leads to faster switching speeds in transistors and lower power consumption [16, 17]. Unstrained silicon is silicon in its natural state, where the atoms are in their regular, unmodified lattice positions. There is no external stress applied to the silicon crystal structure . In unstrained silicon, the charge carriers (electrons and holes) move at their normal speeds, which is slower compared to strained silicon. While it works well for standard electronic applications, it doesn't provide the performance enhancements that strained silicon does [18]. With the development of strained tri-layered channel in the device, its performance is significantly improved as compare to unstrained one. This is attributed mainly to two following phenomenon: energy band shifting and degenerate splitting of electronic states. These two effects collectively improve the carrier's mobility and led significant enhancement in drive current [16, 18].

Even though the on current is improved with a strained-silicon channel still another major concern in the continued scaling is the increment of gate direct tunneling current with decreasing gate oxide thickness, thus resulting in enhanced off-state leakage current [19]. The most technological solution is the use of high-k dielectric materials. However, there are certain drawbacks of direct deposition of high-k dielectrics on Silicon such as maintaining the interface's quality between Silicon and high-k dielectric, mobility degradation with threshold voltage instability [20, 21]. The implementation of the Gate Stack (GS) configuration tackles the problem. GS architecture consists of a thin low-k dielectric layer between the high-k dielectrics and Silicon [22]. Thus, taking all these considerations into account, we propose a Vertically Stacked Heterostructure on Insulator Gate Stacked Ferroelectric based FinFET (VS-HOI-GS-FeFinFET) with strained tri-layered heterostructure channel system. It is formed with the amalgamation of several advanced technologies such as integration of ferroelectric layer in multigate FinFET along with the adaptation of SOI technology. Further strain engineering is incorporated in doing the vertical stacking of strained tri-layered channel forming heterostructure channel system with the help of Si/SiGe. Subsequently gate stack engineering is also employed in the structure with the help of materials of different dielectric constants for gate oxide. Thus, the resulting VS-HOI-GS-FeFinFET is further optimized in this research work in the subsequent sections to make the device suitable for various high performance Analog and RF applications.

The detailed optimization of the device is considered and analysed with a initial fair comparison between conventional FeFinFET and proposed VS-HOI-FeFinFET followed by the optimization of VS-HOI-GS-FeFinFET with gate stacking consisting high-k/low-k dielectric for the enhanced analog/RF performance. This work is divided into five sections: section II includes all the device's specifications and fabrication flowchart; section III explains the simulation framework and physical models; section IV provides the results and discussion; and section V concludes the paper.

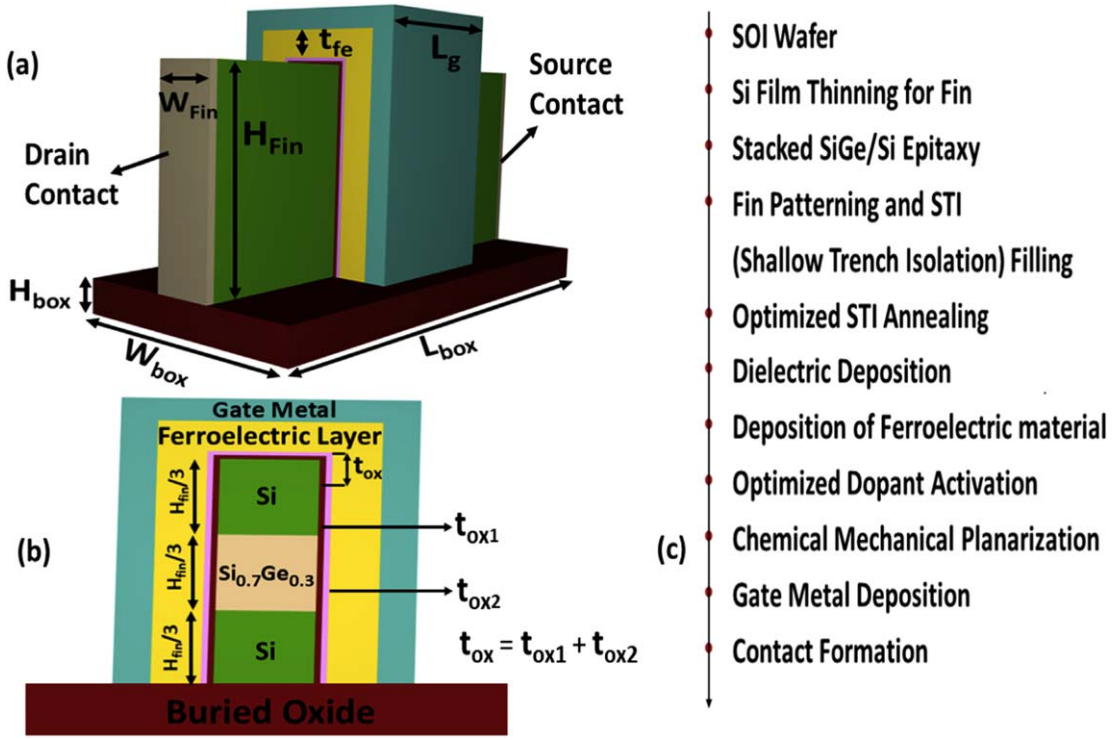

Figure 1. (a) 3D schematic view of VS-HOI-GS-FeFinFET (b) inset of vertical cross-sectional view of VS-HOI-GS-FeFinFET (c) Fabrication process flowchart.

2. Device structure

The Vertically Stacked Heterostructure on Insulator Gate Stacked Ferroelectric based FinFET (VS-HOI-GS-FeFinFET) 3-dimensional structure is shown in figure 1 (a) and vertical 2-dimensional view of FeFinFET slit through the fin of the device is illustrated in figure 1(b). Further figure 1(c) displays the step by step fabrication process flowchart for VS-HOI-GS-FeFinFET. As the starting material SOI wafer is used with a thick buried oxide layer and thick silicon film followed by silicon film thinning for fin. Afterwards stacked SiGe/Si tri-layer were epitaxially grown by reduced-pressure chemical vapor epitaxial deposition. Thereafter, fin patterning is done using the self-aligned quadruple patterning (SAQP) method followed by shallow trench isolation (STI) filling and an optimized STI densification annealing which is performed with a rapid thermal annealing (RTA) at an optimized temperature. The gate dielectric is deposited on the silicon interfacial layer by atomic layer deposition (ALD) followed by ferroelectric layer deposition over the gate oxide using atomic layer deposition (ALD) or chemical vapor deposition (CVD). The drain and source regions are implanted, and the dopants of these regions are activated using spike annealing followed by chemical mechanical planarization for smoothening the surface. Metal gate is deposited using electron beam evaporation at room temperature on the top of the ferroelectric layer. The source/drain metal contacts are deposited by electron beam evaporation followed by lift-off process. The VS-HOI-GS-FeFinFET is formed and continues processing [14, 23, 24]. The gate length considered for the device is fixed at 20nm where the gate stack consists of silicon doped hafnium oxide (HfO_2FE) as the ferroelectric material with thickness fixed at 4 nm and different combinations of high-k/low-k gate dielectric materials are used as gate oxide material with total physical thickness fixed at 1 nm. The height and width of the fin are taken as 30 nm and 8 nm respectively. A tri-layered strained-silicon channel system is formed with the help of SiGe as channel is stacked with silicon germanium sandwiched between two silicon layers as Si-$Si_{0.7}Ge_{0.3}$-Si (where $Si_{0.7}Ge_{0.3}$ represents that the mole fraction of Si and Ge is taken as 0.7 and 0.3 respectively) with each stacked layer having the same height of 10 nm. The doping concentration of source/drain is taken as 1×10^{20} cm^{-3} with donor type and that of channel is 1×10^{16} cm^{-3} with acceptor type with uniform profile. The length of the source/drain regions is fixed at 20 nm. Besides that, to avoid any poly-depletion effect seen in polysilicon gates, metal gate with work function 4.53 eV is used in this device which is having high thermal stability and is also compatible with CMOS processing [25]. Further the entire heterostructure is built on an insulator SiO_2 box whose length, width and height are kept 62nm, 32 nm and 5 nm respectively to add the advantages of SOI technology such as improved subthreshold characteristics, minimum parasitic capacitances and suppressed threshold voltage (V_{th}) variations. Table 1 displays the different dielectric materials used for the simulations and

Table 1. Dielectric Materials.

Material and Properties	SiO_2	Al_2O_3	HfO_2
Dielectric Constant	3.9	9	22
Band gap [eV]	9	8.8	5.8
Conduction band offset [eV]	3.5	2.8	1.5

Table 2. Gate Stack Configurations.

Gate stack configuration of VS-HOI-GS-FeFinFET	Gate stack materials
C1	SiO_2+Al_2O_3
C2	SiO_2+HfO_2
C3	Al_2O_3
C4	Al_2O_3+HfO_2

their properties. Four Gate Stack Configuration C1 to C4 are considered in this study. Each configuration involves different combinations of interfacial layers, combinedly making gate oxide in between the ferroelectric layer and the semiconductor. Four different combinations C1 to C4 are taken in such a way that each subsequent combination improves the performance of the device in terms of various analog/RF parameters. The combinations taken for gate oxide in different configurations are C1(SiO_2+Al_2O_3), C2(SiO_2+HfO_2), C3(Al_2O_3), and C4(Al_2O_3+HfO_2), as also summarized in table 2.

3. Simulation framework and physical models

All the simulations are carried out by Genius 3D TCAD simulator by Cogenda. The gate to source voltage is varied from 0 to 1 V while drain to source voltage and temperature are fixed at 0.4 V and 300K respectively during the entire simulation. The simulation setup includes the drift-diffusion model level 1 (DDML1) to solve the set of partial differential equations coupled with Poisson's equation as given by equation (1) and continuity equations to govern the carrier transport phenomena for the electrons and the holes as given by equation (2) and (3) respectively,

$$\nabla.\epsilon\nabla\psi = -q(p - n + N_D^+ - N_A^-) \tag{1}$$

$$\frac{\partial n}{\partial t} = \nabla.(\mu_n n\vec{E}_n + \mu_n \frac{k_b T}{q}\nabla n - (U - G) \tag{2}$$

$$\frac{\partial p}{\partial t} = -\nabla.(\mu_p p\vec{E}_p + \mu_p \frac{k_b T}{q}\nabla p - (U - G) \tag{3}$$

where ψ is the electrostatic potential of the vacuum level, n and p are the electron and hole concentration, N_D^+ and N_A^- are the ionized impurity concentrations, q is the magnitude of the charge of an electron, E_n and E_p are the efective driving electrical feld for electrons and holes, μ_n and μ_p are mobilities of electrons and holes, U and G are the recombination and generation rates for both electrons and holes.

Also Shockley-Read-Hall (SRH) recombination model is used to incorporate generation and recombination of electrons and holes [15]. Further to consider the mobility degradation at silicon to oxide interface due to various factors, Lombardi mobility model is used for silicon which takes into account three components related to carrier mobility such as doping-dependent bulk mobility (μ_b) which mainly accounts for the ionized impurity scattering, the mobility degradation due to acoustic phonon scattering in the inversion layer (μ_{ac}) which also accounts quantum confinement in the potential well at the interface and the mobility degradation due to the surface roughness scattering (μ_{sr}) as given by equation (4), to collectively give the total mobility (μ_t). Similarly, Philips mobility model is used for SiGe that takes into account the distinct acceptor (A) and donor (D) scattering, carrier-carrier scattering and carrier screening effects (P) as given by equation (5), where $\mu_{0,n}$ is the total low field electron mobilities, $\mu_{lattice,n}$ is the electron mobilities due to lattice scattering [26].

$$\frac{1}{\mu_t} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \tag{4}$$

Table 3. Device parameters.

Device parameters	VS-HOI-GS-FeFinFET
Gate length (L_g)	20nm
Drain/Source ($L_{d/s}$)	20nm
Channel material	Si-$Si_{0.7}Ge_{0.3}$-Si
Oxide thickness (t_{ox})	1nm
Ferroelectric thickness (t_{fe})	4nm
Background dielectric constant of Ferroelectric layer	27
Width of fin (W_{Fin})	8nm
Height of fin (H_{Fin})	30nm
Height of box (H_{box})	5nm
Width of box (W_{box})	32nm
Length of box (L_{box})	62nm
Doping concentration of drain/source ($N_{d/s}$) (cm^{-3})	1×10^{20}
Doping concentration of channel (N_{ch}) (cm^{-3})	1×10^{16}
Gate work function (ϕ)	4.53 eV

$$\frac{1}{\mu_{0,n}} = \frac{1}{\mu_{lattice,n}} + \frac{1}{\mu_{D+A+P}} \tag{5}$$

The density gradient method is also used to consider quantum confinement phenomena along with Fermi–Dirac carrier statistics model [26, 27]. The physics of ferroelectric (FE) layer is modeled with time-dependent Landau-Khalatnikov (LK) equation for relating electric field used for the FE layer as a function of polarization (P) as given by equation (6),

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\left(\frac{\partial P}{\partial t}\right) \tag{6}$$

where α, β, and γ are the static Landau FE material-dependent coefficients taken as -1.23×10^{11} cm/F, 3.28×10^{20} cm^5/FC^2, 0.0 cm^9/FC^4 while g is dipole interaction coefficient and ρ is viscosity coefficient [26, 28]. The background dielectric constant of ferroelectric layer is fixed at 27 as mentioned in table 3. Also, the polarization parameters are adjusted as coercive field (E_c) equals to 1.29 MV/cm, and remnant polarization (P_r) equals to 13.69 $\mu C/cm^2$ [26]. Further Lucent model is used to capture the high-field mobility effects along with hot carrier models to consider the effect of hot carriers. The various device parameters considered for the simulation are displayed in tables 1 and 3.

4. Result and discussion

4.1. Performance comparison between FeFinFET and VS-HOI-FeFinFET

In this section, the performance of FeFinFET and VS-HOI-FeFinFET is compared for different parameters. The device dimensions of both the structures are kept same as discussed in section 2. Instead of gate oxide stack, only single layer of oxide is used as gate oxide for this comparison. Firstly, the VS-HOI-FeFinFET is compared with FeFinFET with SiO_2 as gate oxide and then simultaneously the performance of VS-HOI-FeFinFET is analysed with Al_2O_3 as gate oxide instead of SiO_2.

$$FOM = \frac{|PV\,(VS - HOI - FeFinFET\,(Al_2O_3)) - PV\,(FeFinFET\,(SiO_2))|}{|PV\,(FeFinFET\,(SiO_2))|} \times 100 \tag{7}$$

The I_d-V_{gs} characteristics of all configurations are depicted in figure 2 , which shows significant increment in ON current (I_{on}) for VS-HOI-FeFinFET(Al_2O_3) as compared to VS-HOI-FeFinFET(SiO_2) and FeFinFET(SiO_2). Further figure 3 shows 97.849% reduction in leakage current in VS-HOI-FeFinFET(Al_2O_3) due to enhanced control over the channel and reduced tunnelling current which results in 61.745 times increment in its switching ratio as compared to FeFinFET. Figure 4 depicts improved performance for VS-HOI-FeFinFET(Al_2O_3) in terms of threshold voltage and subthreshold swing with increment by 41.33% and decrement by 11.45% respectively as compared to FeFinFET due to better controllability over the channel and enhanced shielding of drain-side potential, thus resulting in improved subthreshold characteristics. Figure of merit (FOM) of VS-HOI-FeFinFET(Al_2O_3) over FeFinFET(SiO_2) is also shown in table 4, which is a performance metric and used to characterize the performance of a device relative to its alternatives. Here, it gives the improvement in the performance of VS-HOI-FeFinFET(Al_2O_3) over FeFinFET(SiO_2) in terms of various analysed parameters and it

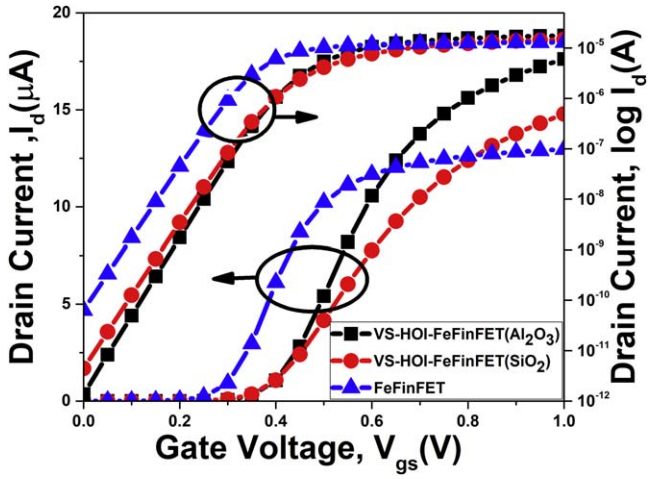

Figure 2. Variation in transfer characteristic of VS-HOI-FeFinFET and FeFinFET in linear and log scale.

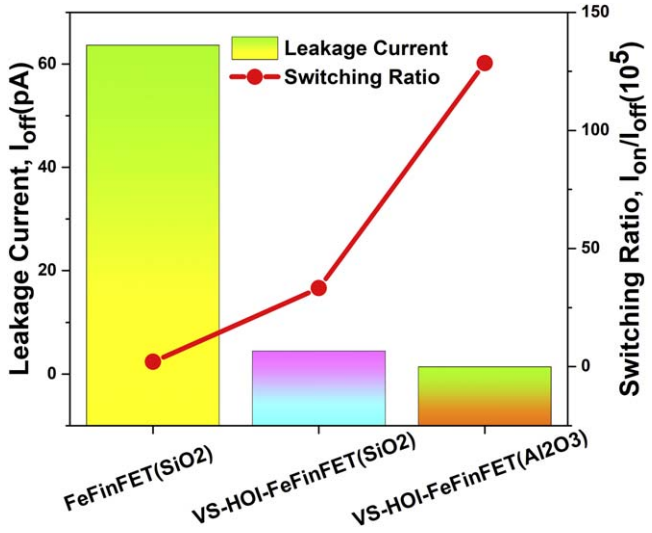

Figure 3. Comparison of Switching Ratio and Leakage Current.

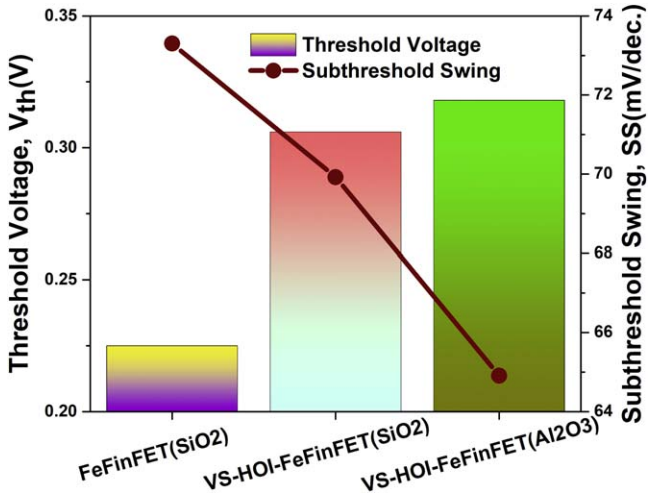

Figure 4. Comparison of Threshold Voltage and Subthreshold Swing.

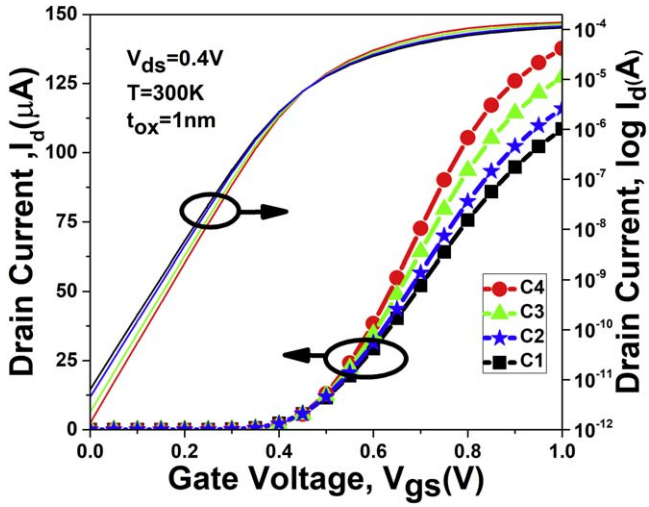

Figure 5. Variation in transfer characteristic of VS-HOI-GS-FeFinFET for different configurations in linear and log scale.

Table 4. Performance Comparison between FeFinFET and VS-HOI-FeFinFET.

Parameter	FeFinFET(SiO_2)	VS-HOI-FeFinFET(SiO_2)	VS-HOI-FeFinFET(Al_2O_3)	figure of Merit (FOM)
I_{on} (A)	1.295×10^{-5}	1.478×10^{-5}	1.761×10^{-5}	35.98%
I_{off}(A)	6.365×10^{-11}	4.446×10^{-12}	1.371×10^{-12}	97.84%
I_{on}/I_{off}	$2.034 \times 10^{+5}$	$3.324 \times 10^{+6}$	$1.284 \times 10^{+7}$	63.12 times
$V_{th}(V)$	0.225	0.306	0.318	41.33%
SS ($mV/dec.$)	73.301	69.922	64.910	11.44%

is calculated using equation (7) [29], where PV(VS-HOI-FeFinFET(Al_2O_3)) and PV(FeFinFET(SiO_2)) are the parametric values of the respective structures. On account of these advantages of VS-HOI-FeFinFET over FeFinFET, the impact of various gate dielectric materials in gate oxide stack configuration for VS-HOI-FeFinFET is analysed for static, analog and RF performance.

4.2. Gate stack optimization for static and analog performance

In this section, various vital static and analog parameters are examined to optimize the gate stack with different dielectric materials to further improve the performance of VS-HOI-GS-FeFinFET over VS-HOI-FeFinFET(Al_2O_3) which showed best performance for single oxide layer as discussed in section 4.1 and can also be observed from table 4. Figure 5 shows the comparison of I_d-V_{gs} characteristics in both linear and log scale for different configurations as discussed in table 2. It shows increase in ON current due to improved gate control over the channel with increased capacitance per unit area and decrease in leakage current due to reduction in gate leakage current with high-k materials when the gate stack configuration changes from C1 to C4. Improved gate control means the gate can more effectively modulate the flow of current through the channel, which is crucial in switching the transistor between the ON and OFF states. High-k materials have a higher dielectric constant compared to traditional SiO_2 which led to increase in the gate capacitance as related by equation (8), where k is the dielectric constant of the material, ϵ_0 is the permittivity of free space, A is the area of the gate, and d is the thickness of the dielectric layer [30].

$$C = \frac{k\epsilon_0 A}{d} \tag{8}$$

A higher capacitance means that for a given gate voltage, more charge is induced in the channel which results into stronger electric field. This stronger electric field more effectively controls the number of carriers in the channel. This leads higher carrier density in the channel, thereby increasing the ON-state current. Also, gate leakage current is the undesired current that flows through the gate dielectric when the transistor is in the OFF state. A higher dielectric constant allows for a larger capacitance. This is beneficial because it reduces gate leakage current while maintaining strong gate control over the channel. The reduction in gate leakage current directly lowers the overall leakage current in the transistor as shown in the figure 5.

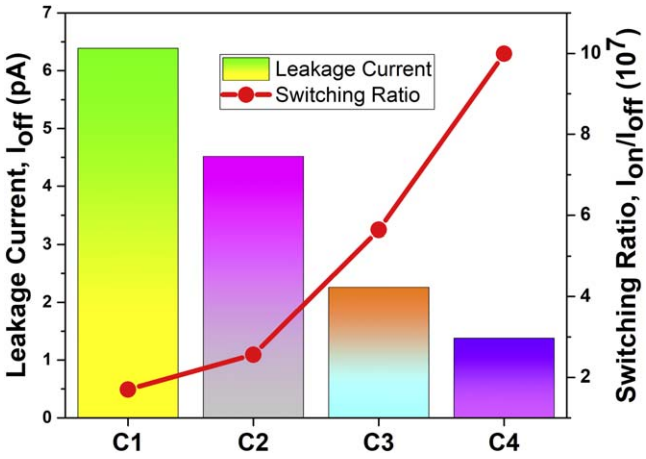

Figure 6. Comparison of Leakage Current and Switching Ratio for different configurations.

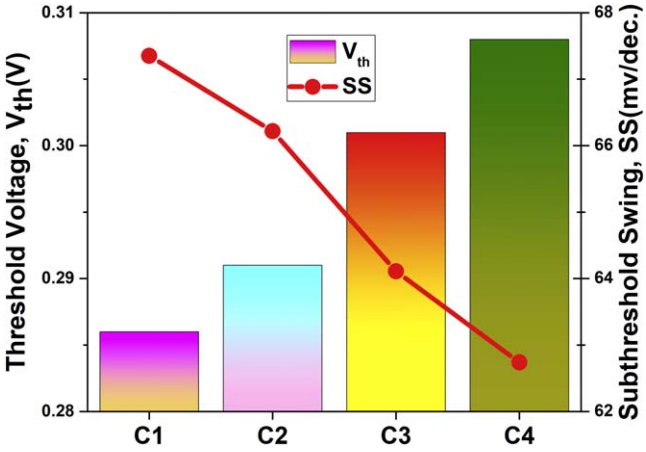

Figure 7. Comparison of Threshold Voltage and Subthreshold Swing for different configurations.

This results in increase in the switching ratio upto 5.879 times for C4 over C1 as shown in figure 6. Further, figure 7 displays the sequential increase in threshold voltage and improved subthreshold swing as the configuration changes from C1 to C4 thus enhancing the subthreshold device characteristics.

Transconductance (g_m), which is given by equation (9), measures the effectiveness of the FET device in converting variations in the gate-to-source voltage into changes in the drain current [31]. Figure 8 confirms that transconductance rises with rise in dielectric constant and shows maximum peak for C4 because of the enhanced drain current and lower electric field at the drain side thus exhibits better amplification capabilities over others. Further C4 also displays the improved device efficiency which is also known as Transconductance Generation Factor (TGF) [32]. It is an important parameter in the design of analog circuits and higher TGF shown by C4 depicts its enhanced efficiency of converting DC parameter (I_d) into AC parameters (g_m) as showcased in figure 8.

Quality factor (QF) is an indicator of the transistor's overall performance, as defined by equation (10), combining both the efficiency of switching (represented by g_m) and how quickly the device can switch from OFF to ON (represented by SS) [22]. In many FETs, there is a trade-off between achieving a high transconductance and a low subthreshold swing. The QF encapsulates this trade-off into a single parameter. Optimizing for a higher QF means balancing these two critical aspects to achieve a transistor that is both responsive and has efficient switching, making it an important parameter in the design and evaluation of advanced semiconductor devices [22]. The maximum value of g_m considered for the QF evaluation is obtained at $V_{gs} = 0.65$V. As shown in figure 9, C4 gives maximum quality factor which is 58.98% increment over C1. This improvement in the QF value with increasing dielectric constant is due to the enhanced transconductance and reduced subthreshold swing for C4. The DIBL is another vital subthreshold performance metric and minimum DIBL values are preferred for optimum device performance in advanced technology nodes thus figure 9 successfully depicts C4 a

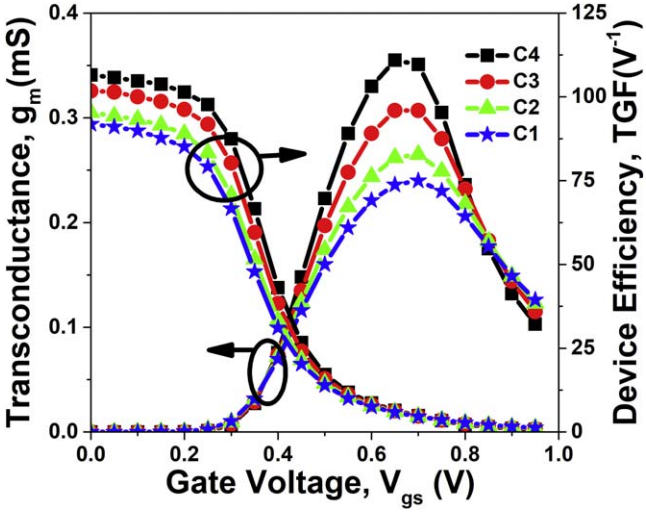

Figure 8. Variation in transconductance and device efficiency for different configurations.

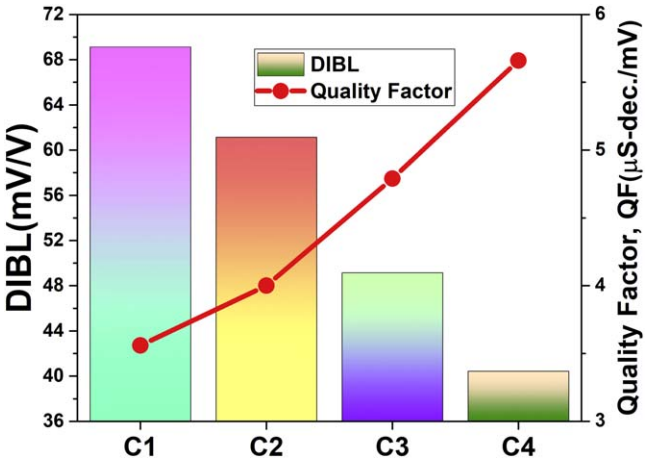

Figure 9. Comparison of DIBL and Quality factor for different configurations.

better configuration with smaller DIBL over other structures.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{9}$$

$$QF = \frac{g_m}{SS} \tag{10}$$

$$A_v = \frac{g_m}{g_d} \tag{11}$$

$$V_{EA} = \frac{I_d}{g_d} \tag{12}$$

The potential contours of all the four configurations considered for VS-HOI-GS-FeFinFET are displayed in figure 10(a). Further, the potential profile for silicon and SiGe is also presented in figures 10(b) and (c) which shows the variation of electric potential along the channel for all configurations. It shows that higher electric potential is acquired at the drain end as compared to the source end for all the four configurations which leads to an increased drain-source voltage and results in a stronger electric field in the channel. Thus, it makes the device to work with improved current control, faster switching, and better on-state performance. It also shows the improvement in potential significantly in the channel region for C4 configuration as compared to its counterparts due to the ability of high-k dielectrics in the gate oxide to improve the electrostatic control over the channel and the effect is more prominent in the strained layers of SiGe in the middle of channel due to higher

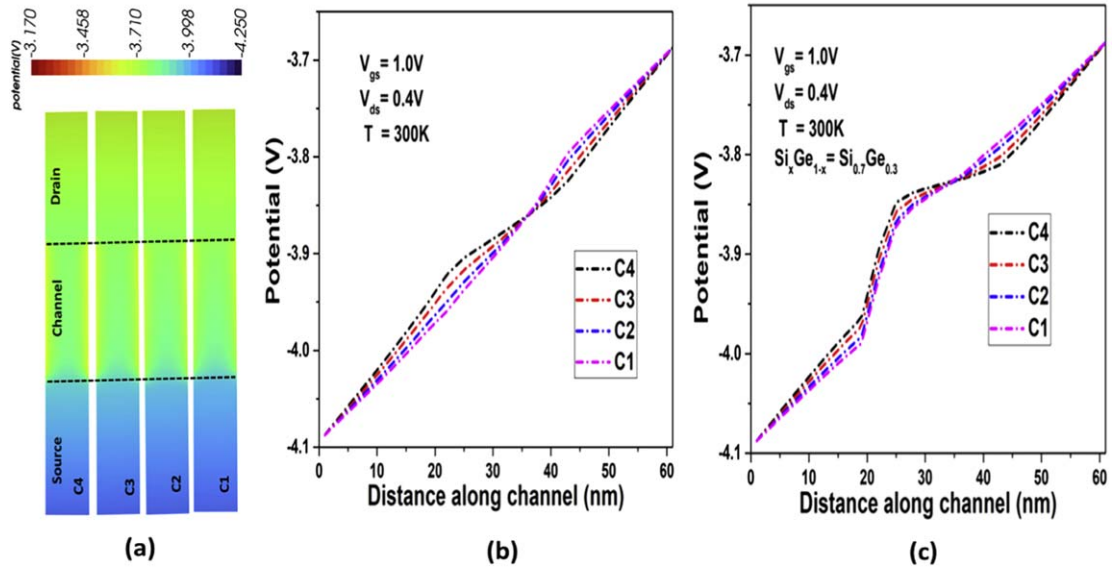

Figure 10. (a) Potential contour of all the four configurations (b) Potential profile variation in silicon with distance along the channel (c) Potential profile variation in SiGe with distance along the channel.

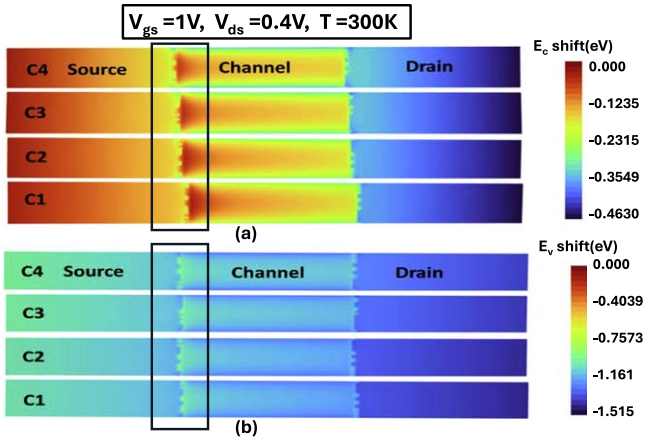

Figure 11. Contour of band energy shift for (a) Conduction band (b) Valence band for all the four configurations.

carrier mobility and narrower bandgap in SiGe as compared to silicon material [18]. Subsequently, there is decrease in potential in C4 configuration from channel-drain junction towards drain side as compared to other configurations. This is due to the reduction in DIBL in the C4 configuration as shown in figure 9, that reduces the flattening of the potential profile, resulting in a steeper potential drop between the channel-drain junction and the drain terminal. Thus, this configuration leads to better switching characteristics, lower leakage current, and improved threshold voltage control, making the device more efficient and reliable, particularly in low-power and high-speed applications [33]. Further figures 11(a) and (b) respectively shows the contour plot of shift in conduction band energy and valence band energy for all the configurations considered at $V_{gs} = 1V$, $V_{ds} = 0.4V$ and $T = 300K$. Due to the shift, the conduction band of C4 configuration is lower than the other configurations across the channel, which reveals the improved conductivity with more band bending, and enhanced band to band tunnelling rate of the carriers from valence band to conduction band for C4 configuration.

Understanding and controlling the output conductance is crucial in optimizing the performance of the device, especially in applications where precise control of the transistor behaviour is necessary, such as in high-frequency amplifiers or low-power designs. Figure 12 displays a combined plot showing variation in drain current and output conductance as a function of V_{ds} at constant $V_{gs} = 0.4V$. Initially, g_d is large while device is operating in linear region but it keeps on decaying with increase in drain to source voltage. In the saturation region, g_d maintains almost constant value. High-k dielectric materials have a higher dielectric constant

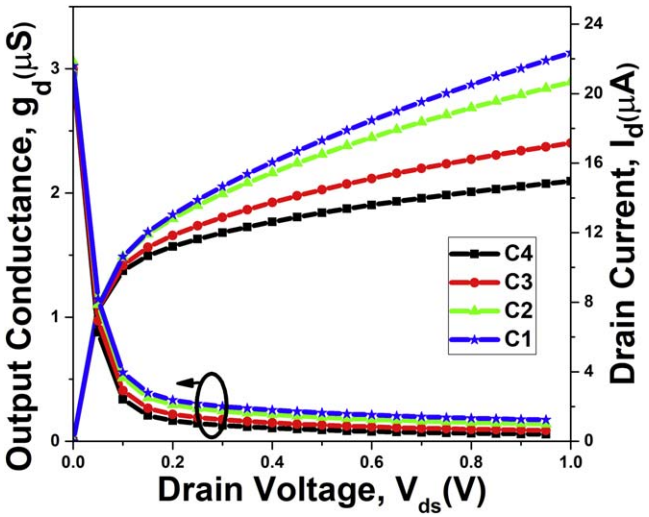

Figure 12. Variation in output characteristic and output conductance for different VS-HOI-GS-FeFinFET configurations.

compared to traditional SiO_2. This enhances the capacitance, which is critical for better control over the channel. Improved gate control helps in effectively modulating the channel, leading to better electrostatic control over the threshold voltage and carrier mobility. This improved gate control also helps in reducing leakage current due to reduced DIBL and preventing any threshold voltage roll-off. The suppression of these SCEs stabilizes the channel behavior, and this stabilization further minimizes the dependence of output conductance on the drain voltage, leading to lower g_d. Thus, due to improved gate controllability and suppressed SCEs, g_d is minimum for C4 configuration when compared to other counterparts. Also, channel length modulation (CLM) is a phenomenon that occurs when the effective channel length of a FET device changes with variations in the drain voltage, especially in short-channel devices. This effect causes the I_d to vary with the V_{ds}, even when the V_{gs} is constant, which leads to an increase in the output conductance (g_d). When g_d is low, it means that the drain current is less sensitive to changes in the drain voltage. This indicates that the effective channel length is not significantly modulated by the drain voltage, implying reduced channel length modulation. Reduced CLM helps in stabilizing the current output, ensuring that the FET device can provide a more constant current, which is essential for certain applications such as constant current sources [34]. Thus, lower g_d ensures reduced channel length modulation which is useful for driving constant current source applications.

Intrinsic gain and early voltage are evaluated using equations (11) and (12) respectively, and they must be as high as possible for enhanced analog performance of the device [34]. Figure 13 shows the variation of Intrinsic gain and early voltage against gate to source voltage for all the configurations. The Early voltage takes into account the Early effect and is vital for accurate small-signal analysis, particularly in the saturation region of transistor operation. The maximum value of early voltage and highest peak of intrinsic gain is achieved for C4 configuration thus making it suitable for high-speed analog and mixed-signal circuits, where the signal fidelity and linearity are critical [35].

Output resistance is a measure of how much a device's output voltage changes in response to variations in the load resistance. In electronic circuits, it plays a vital role in maintaining signal integrity and stability. High output resistance ensures better signal fidelity by minimizing voltage variations in response to changes in load resistance. The variation in Rout for different configurations is displayed in figure 14. The increment in R_{out} is very well observed in both the regions, but the rise in saturation region is significantly higher than the active region. Compared to the C1 configuration, the C4 configuration acquires high output resistance which contribute to improved noise performance by minimizing the impact of load-induced noise on the output signal and improve overall performance of the device [36].

4.2.1. Performance optimization for variation in mole fraction of the channel material

Compound materials are defined with mole fraction (x) that depicts the amount of composition present in the mixture. It influences the properties of the channel material and performance of the device, thus for an optimized device response, its impact needs to be analyzed. As C4 configuration has given the most improved performance out of four considered configurations in section 4, it is considered for the analysis in this section. Figure 15 displays the impact of germanium mole fraction in the form of turn on characteristics of VS-HOI-GS-FeFinFET by varying the Ge-mole fraction from 0.1 to 0.9. It is apparent from the figure 16 that as we increase the mole fraction, I_{on} starts decreasing but there is improvement in leakage current (I_{off}) which decreases from

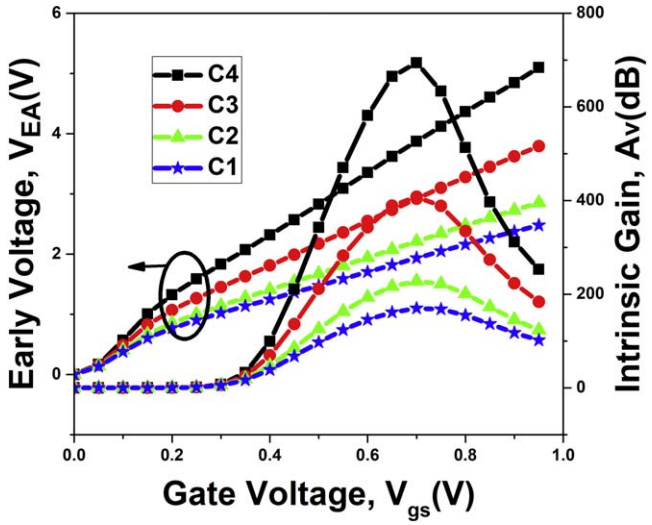

Figure 13. Variation in Early Voltage and Intrinsic Gain for different configurations.

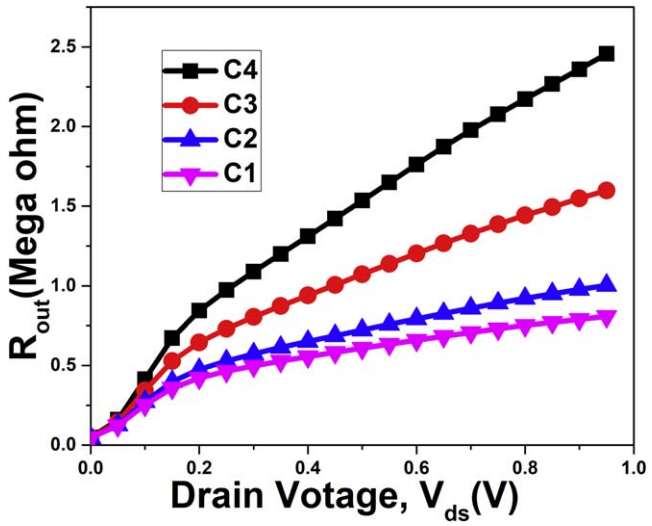

Figure 14. Variation in output resistance for different VS-HOI-GS-FeFinFET configurations.

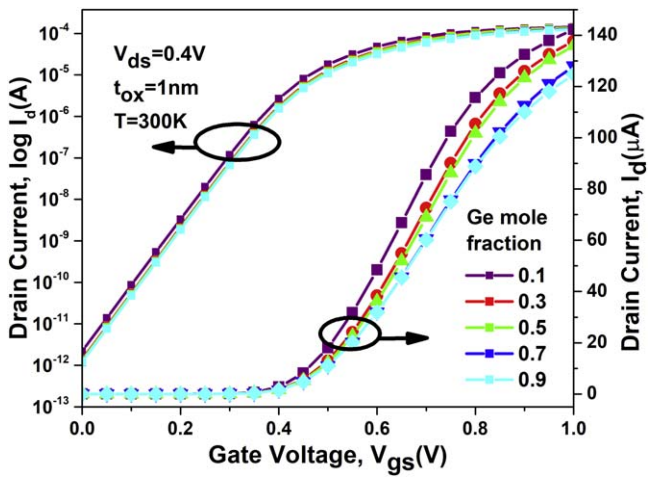

Figure 15. Turn on characteristics of VS-HOI-GS-FeFinFET for different Ge mole fraction in channel.

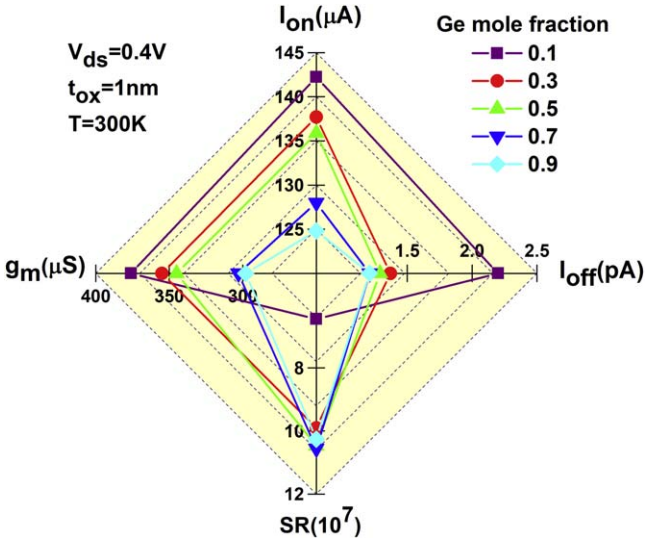

Figure 16. Variation in I_{on}, I_{off}, SR, g_m performance of VS-HOI-GS-FeFinFET for different Ge mole fraction.

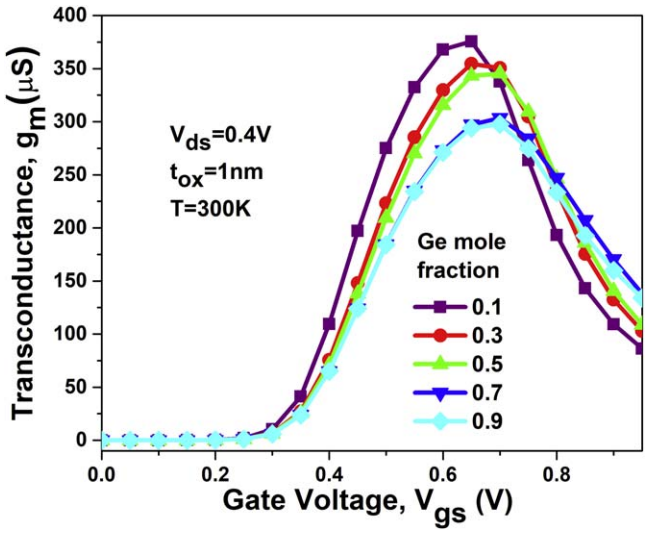

Figure 17. Variation in transconductance of VS-HOI-GS-FeFinFET with gate voltage for different Ge mole fraction.

2.20 pA at x = 0.1 to 1.22 pA at x = 0.9 that amounts to total decrement by 44.8%. On the other hand, switching ratio for the device is increased from 6.46×10^7 at x = 0.1 to 10.3×10^7 at x = 0.9 implies enhancement by 58.9%. It also shows the variation of peak transconductance with mole fraction which show better performance with 376 μS at low value of x = 0.1 as compared to 298 μS at high value of x = 0.9 for lower V_{gs}. But as the gate voltage is increasing, the g_m increases for large value of mole fraction as depicted in figure 17, indicating that the device can be optimized for variable mole fraction as per the design and application's requirements with balancing the trade offs between different performance metrics.

4.2.2. Performance optimization for variation in height and width of the Fin

Performance optimization of a FeFinFET with respect to variations in the height (H_{Fin}) and width (W_{Fin}) of the fin is a crucial aspect of device design. These geometrical parameters significantly influence the electrical characteristics of the FeFinFET, such as threshold voltage (V_{th}), leakage current (I_{off}), switching ratio etc., thus needs to be optimized for improving the performance of the device. As C4 configuration has given the most improved performance out of four considered configurations in section 4, it is considered for the analysis in this section. Figure 18 displays the variation in drain current with variation in gate voltage for different heights of the Fin of VS-HOI-GS-FeFinFET. As it is visible from the figure that the variation in transfer characteristics of VS-HOI-GS-FeFinFET is very less with variation in H_{Fin}. Several reasons are responsible for this such as, although

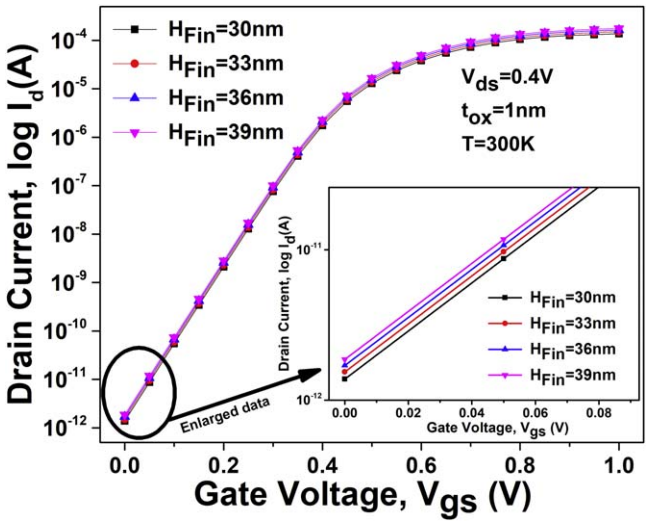

Figure 18. Variation in drain current with variation in gate voltage for different height of the Fin of VS-HOI-GS-FeFinFET with fixed width of Fin at 8nm.

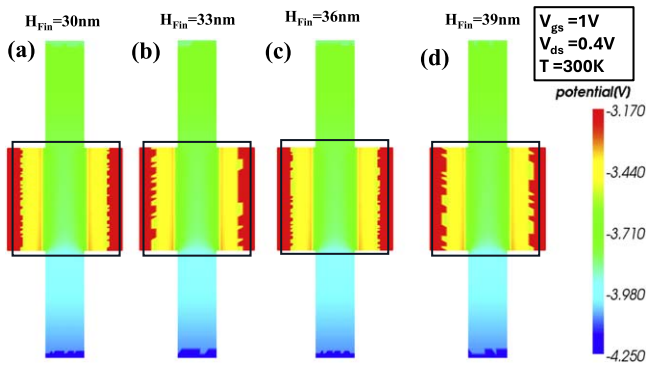

Figure 19. The contour plot of potential for (a) H_{Fin} = 30 nm (b) H_{Fin} = 33 nm (c) H_{Fin} = 36 (d) H_{Fin} = 39 nm for VS-HOI-GS-FeFinFET with W_{Fin} fixed at 8 nm.

H_{Fin} influences the effective channel area (thus affecting current-carrying capability of the device), it doesn't impact gate control as much as the width. The gate's ability to control the channel is more sensitive to lateral dimensions (W_{Fin}) rather than vertical dimension [37]. Also, the behavior of the ferroelectric material is sensitive to the electric field, which is influenced more by the gate-channel coupling. Since the coupling is strongly affected with changes in W_{Fin} in comparison to changes in H_{Fin}, the ferroelectric behavior is more affected by width variations. Therefore, as H_{Fin} doesn't influence the gate control as strongly as fin width, leading to a smaller overall impact on device performance when it is varied. It clearly shows that as height is reducing from 39nm to 30 nm, there is decrement in leakage current from 1.86 pA to 1.38 pA which is 25.8% reduction in I_{off}. It leads to increase in switching ratio from 9.47×10^7 to 9.98×10^7 and minimal increase in V_{th} from 0.30V to 0.31V due to better electrostatic control of gate over the carriers in the channel with decreasing H_{Fin} from 39 nm to 30 nm.

Figure 19 shows the contour plot of potential for VS-HOI-GS-FeFinFET at various fin heights such as (a) H_{Fin} = 30 nm (b) H_{Fin} = 33 nm (c) H_{Fin} = 36 nm and (d) H_{Fin} = 39 nm, at V_{gs} = 1V, V_{ds} = 0.4V and T = 300K. A reduction in fin height brings the entire fin closer to the gate, allowing the gate to exert stronger electrostatic control over the channel. This results in higher electric potential gradients near the top surface of the fin, with a more uniform and tightly controlled potential distribution across the channel, particularly near the source and drain regions, as visible in figure 19. Also, lowering the fin height also reduces the vertical distance that the gate potential must cover to control the channel. This leads to a more uniform potential drop from the gate towards the bottom of the fin as shown in the contour plot for H_{Fin} = 30 nm. Figure 19 also shows that higher electric potential is acquired at the drain end as compared to the source end which leads to an increased drain-source

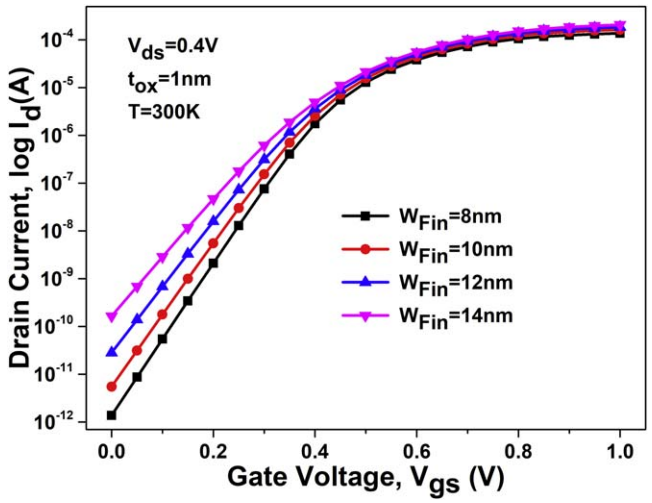

Figure 20. Variation in drain current with variation in gate voltage for different width of the Fin of VS-HOI-GS-FeFinFET with fixed height of Fin at 30 nm.

voltage and results in a stronger electric field in the channel. Thus, it makes the device to work with improved current control, faster switching, and better on-state performance.

Figure 20 displays the variation in drain current with variation in gate voltage for different width of the Fin of VS-HOI-GS-FeFinFET. It illustrates that as width is reducing from 14 nm to 8 nm, there is decrement in I_{off} from 1.64×10^{-10} A to 1.38×10^{-12} A, thus led to 99.15% reduction in leakage current, depicting suppressed SCEs by improving gate control over the channel. This also ensures substantial improvement in switching speed of the device with improvement in switching ratio from 1.26×10^{6} to 9.98×10^{7} and increment in V_{th} from 0.23V to 0.31V as the width of fin is decreased from 14 nm to 8 nm. Thus, combinedly, it can be summarized that the width and height of the fin as 8 nm and 30 nm respectively give the most improved performance for VS-HOI-GS-FeFinFET.

4.2.3. Impact of variation in ferroelectric layer on the device performance and its interdependance on the geometric variations of Fin and oxide layer

The performance of ferroelectric based devices is significantly influenced by the thickness of the ferroelectric layer. In a FeFinFET structure, the ferroelectric layer's behavior is intertwined with several key geometric parameters like fin height, fin width, and oxide thickness. In this section, a brief analysis has been done to understand the dependence of ferroelectric layer on the variations in geometric parameters of the fin and oxide layer. As C4 configuration has given the most improved performance out of four considered configurations in section 4, it is considered for the analysis in this section. Figure 21 shows the variation in transfer characteristics and subthreshold swing of VS-HOI-GS-FeFinFET with the variation in thickness of ferroelectric layer. It shows the improvement in subthreshold characteristics like reduction in I_{off} from 2.47×10^{-12} A to 3.39×10^{-14} A, improvement in SS from 63.97 mV/dec. to 55.1 mV/dec., and enhancement in V_{th} from 0.3 V to 0.36 V as t_{fe} is increased from 2 nm to 14 nm. This happens due to improved electrical field coupling between gate and channel with enhanced polarization on increasing t_{fe}. This improves the transition between the off and on states, ensuring a smoother turn-on behavior which is important in minimizing power loss and ensuring the device functions properly in low-power or high-reliability environments [27, 38].

Further, figures 22, 23 and 24 respectively shows the interdependent effect of variation in ferroelectric layer thickness with variation in fin height, fin width, and oxide thickness. The minimum effect of geometric variation on t_{fe} is displayed by the variation in H_{Fin} as shown in figure 22 while the variation in W_{Fin} shows significant effect on t_{fe} as shown in figure 23. The most improved performance is achieved at $H_{Fin} = 30$ nm, $W_{Fin} = 8$ nm, $t_{fe} = 6$ nm, and $t_{ox} = 1$ nm, with reduced leakage current and improved switching subthreshold characteristics based on several geometric variations of fin and oxide layer. Figure 23 also shows the variation in the transfer characteristics of the device for rising gate voltage (Forward Sweep) and falling gate voltage (Reverse Sweep) with t_{fe}=6 nm. It is seen that hysteresis loop is formed between the forward sweep and reverse sweep, which arises due to bistable polarization states of the ferroelectric material.

Figure 25(a) displays the variation in transfer characteristics of VS-HOI-GS-FeFinFET with variation of ferroelectric thickness. It shows that as thickness is increased from 2 nm to 6 nm, the device's performance improves in terms of ON current and leakage current due to better charge accumulation in the channel via

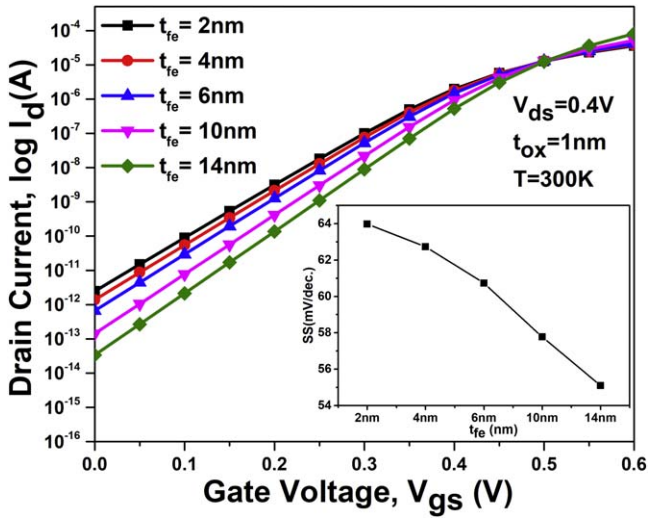

Figure 21. Variation in transfer characteristics and subthreshold swing of VS-HOI-GS-FeFinFET for different ferroelectric thickness at fixed height, width and oxide thickness.

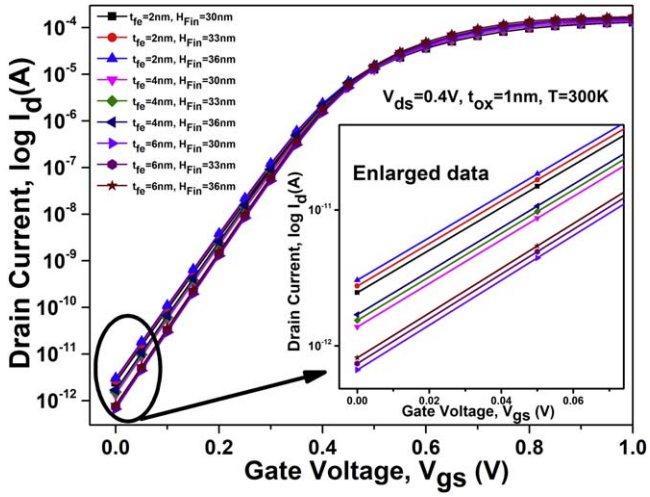

Figure 22. Variation in drain current with variation in gate voltage for different ferroelectric thickness and height of the fin in VS-HOI-GS-FeFinFET at fixed width and oxide thickness.

stronger coupling of the channel and the gate with enhanced polarization, leading to the enhancement of switching ratio from 5.27×10^7 at 2 nm to 2.19×10^8 at 6 nm. This also results in increment in g_m and TGF of the device with increase in t_{fe} from 2 nm to 6 nm as displayed by figure 26(a), indicating improved analog performance of the device with increase in ferroelectric thickness. Further, figure 26(b) shows the $g_{m2}(g_{m3})$ which is defined as second(third) order derivative of drain current with respect to V_{gs} at constant V_{ds} [39]. It confirms the improvement in linearity characteristics of the device with low values of g_{m2} and g_{m3} due to more uniform polarization switching as t_{fe} decreases from 6 nm to 2 nm.

Figure 25(b) also shows the variation in transfer characteristics of VS-HOI-GS-FeFinFET with variation in the thickness of oxide layer. It shows that as the oxide layer thickness decreases, the device performance improves with increment in ON current and reduction in leakage current due to better electrostatic control, thus leading enhancement in switching ratio from 7.29×10^7 at 1.2 nm to 1.35×10^8 at 0.8 nm. Further, figure 27(a) also displays the improving trend for g_m and TGF due to improved amplification effect of ferroelectric layer with decreasing t_{ox}. But figure 27(b) displays the opposite trend in the linearity performance of the device with degradation in g_{m2} and g_{m3} when t_{ox} decreases from 1.2 nm to 0.8 nm. As, it is observed that a noticeable analog performance is achieved at $t_{fe} = 4$ nm and and $t_{ox} = 1$ in VS-HOI-GS-FeFinFET without compromising linearity performance. Therefore, $t_{fe} = 4$ nm and $t_{ox} = 1$ nm are respectively considered as the optimum thickness of ferroelectric and oxide layer for VS-HOI-GS-FeFinFET.

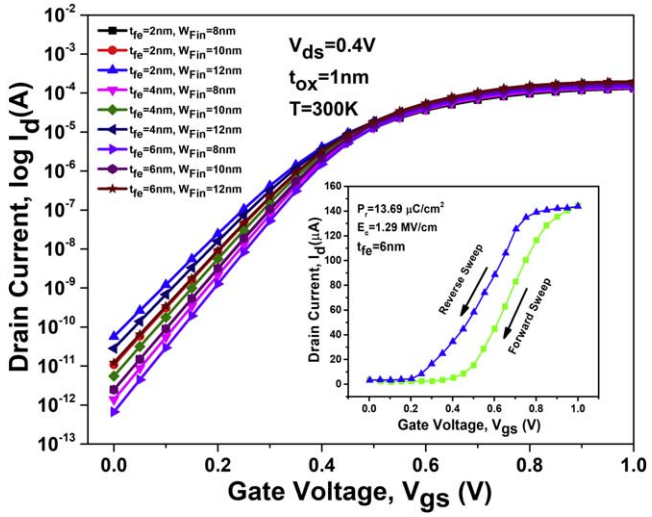

Figure 23. Variation in drain current with variation in gate voltage for different ferroelectric thickness and width of the fin in VS-HOI-GS-FeFinFET at fixed height and oxide thickness.

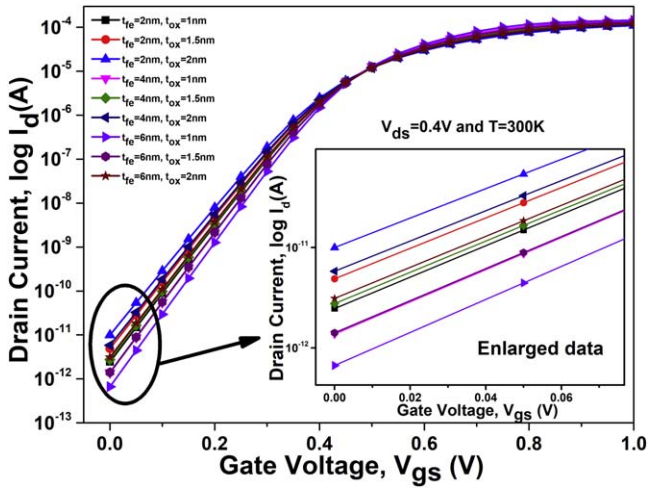

Figure 24. Variation in drain current with variation in gate voltage for different ferroelectric and oxide thickness in VS-HOI-GS-FeFinFET at fixed height and width of the fin.

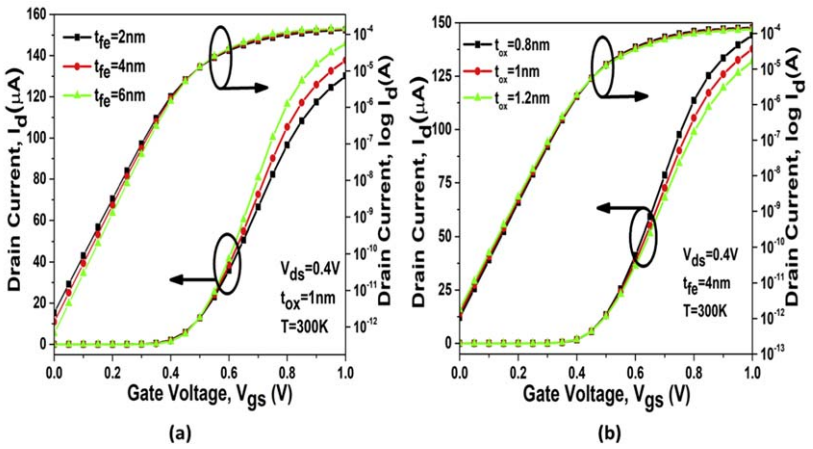

Figure 25. Variation in transfer characteristics of VS-HOI-GS-FeFinFET for different (a) ferroelectric layer thickness (b) oxide layer thickness.

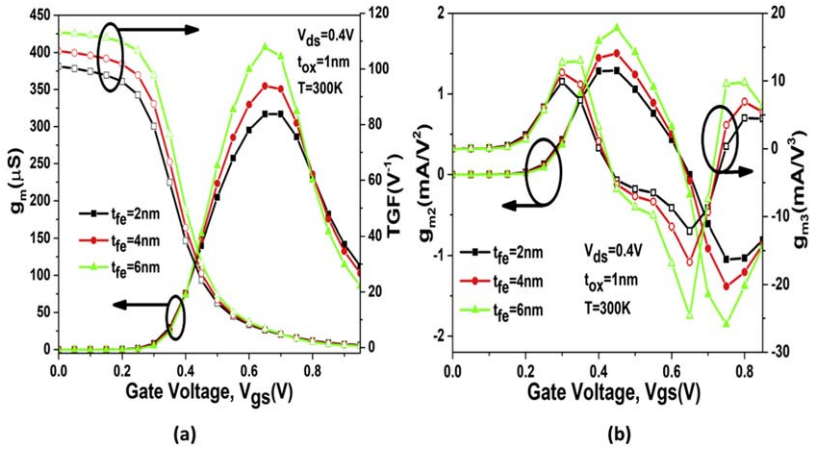

Figure 26. Variation in (a) transconductance and device efficiency (b) g_{m2} and g_{m3} of VS-HOI-GS-FeFinFET for various thickness of ferroelectric layer.

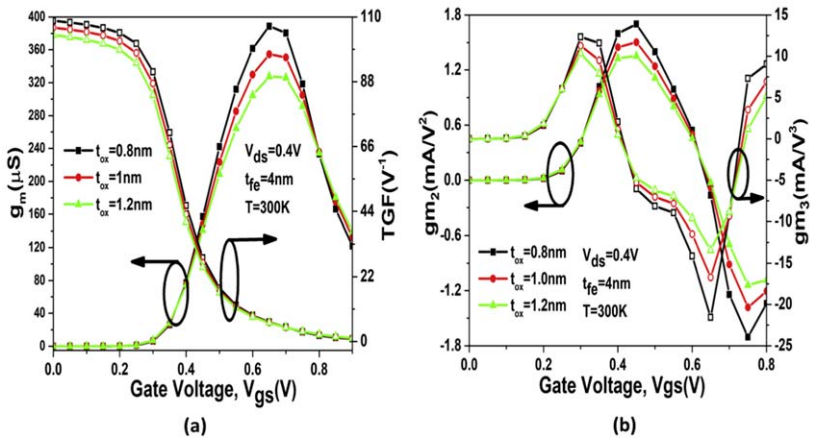

Figure 27. Variation in (a) transconductance and device efficiency (b) g_{m2} and g_{m3} of VS-HOI-GS-FeFinFET for various thickness of oxide layer.

4.3. Gate stack optimization for RF performance

Figure 28 shows combined plot of total gate capacitance (C_{gg}) and Unity gain cut-off frequency (f_T) as a function of gate to source voltage, V_{gs}. It is observed that C_{gg} increases very slowly with V_{gs} in the subthreshold region, but with further increase in V_{gs}, C_{gg} increases swiftly due to the enhanced lateral field, which enhances the movement of charge carriers from source to drain side. In saturation region, as expected, total gate capacitance become constant due to the non-contribution of V_{ds}. In radio frequency (RF) applications, high gate capacitance can be advantageous for achieving higher gain in RF amplifiers [31, 40]. So, figure 28 well confirms the C4 configuration's ability to amplify high-frequency signals effectively as compare to its other counter parts.

Unity gain cutoff frequency (UGCF) is a key parameter for understanding the bandwidth and frequency response characteristics of the system. In electronic systems, it is the point at which the gain of a device or circuit becomes 1 or 0 dB. Figure 28 shows that C4 showcase low UGCF as compared to other configurations which is generally preferred to minimize the impact of noise and distortion on the output signal [41].

The Gain Frequency Product (GFP), as given by equation (13) is a critical parameter characterizing the relationship between the gain and frequency response of a FET device and MOSFETs with a higher GFP are capable of amplifying signals across a broader range of frequencies [41, 42]. Figure 29 displays the peak values of GFP of all the four configurations considered for VS-HOI-GS-FeFinFET and attaining maximum peak value for C4 with 1.84 PHz as compared to 0.552 PHz for C1, makes C4 preferable for applications where a wide frequency range is crucial, such as in radio-frequency (RF) amplifiers and high-frequency communication systems [22, 35]. Transconductance Frequency Product (TFP), given by equation (14) also known as transit frequency represents the frequency at which the transconductance gain of the device starts to decrease [34], indicating its high-frequency performance limitations. Therefore, as shown in figure 29, devices with higher TFP

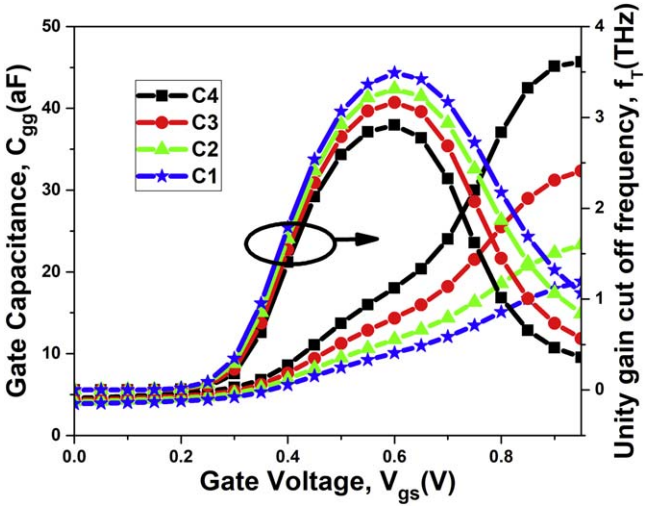

Figure 28. Variation in Gate Capacitance and Unity gain cut off frequency for different configurations.

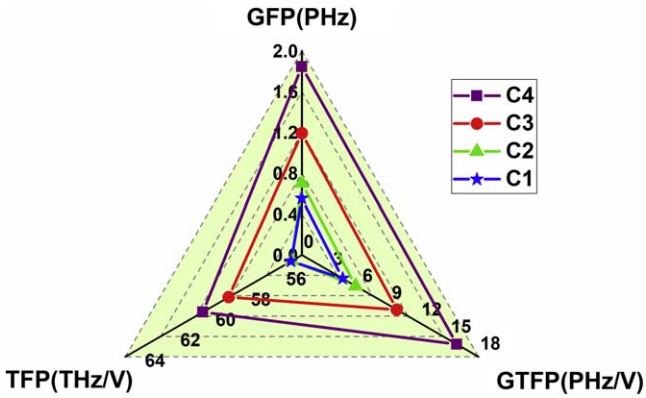

Figure 29. Variation in TFP, GFP and GTFP for different VS-HOI-GS-FeFinFET configurations.

as offered by C4 with 60.6 THz/V as compared to 55.6 THz/V by C1 configuration, are desirable for applications requiring high-speed signal processing and amplification such as in RF circuits and high-speed digital circuits [7, 34].

$$GFP = \frac{g_m}{g_d} \times f_T \tag{13}$$

$$TFP = \frac{g_m}{I_d} \times f_T \tag{14}$$

$$GTFP = \frac{g_m}{g_d} \times \frac{g_m}{I_d} \times f_T \tag{15}$$

Further, it also shows another important RF parameter, gain transconductance frequency product (GTFP) that combines the transconductance and the unity-gain frequency of a MOSFET as given by equation (15) [34]. Highest GTFP for C4 with 15.8 PHz/V as compared to 4.16PHz/V for C1 contributes to improved signal fidelity, ensuring that the amplified output faithfully replicates the input signal. Therefore, with high desired value of GFP, TFP and GTFP, C4 can be very well integrated in fields like wireless communication, radar systems, and other RF applications where rapid signal processing is essential [22, 43].The analog and RF performance metrics of all the four considered configurations are also summarized in table 5. In addition, the performance metrics obtained in this work have been compared with several different devices in existing literatures, as shown in table 6. It can be seen that the results obtained in this work stand out from the previously published work.

Table 5. Summary of different Analog and RF parameters for different configurations of VS-HOI-GS-FeFinFET.

Parameter	C1	C2	C3	C4	Figure of Merit (FOM)
I_{on} (A)	1.085×10^{-4}	1.159×10^{-4}	1.273×10^{-4}	1.377×10^{-4}	26.91%
I_{off} (A)	6.39×10^{-12}	4.52×10^{-12}	2.26×10^{-12}	1.38×10^{-12}	78.40%
I_{on}/I_{off}	$1.697 \times 10^{+7}$	$2.564 \times 10^{+7}$	$5.632 \times 10^{+7}$	$9.978 \times 10^{+7}$	487.97%
$V_{th}(V)$	0.286	0.291	0.301	0.308	7.69%
SS (mV/dec)	67.351	66.216	64.111	62.738	6.84%
DIBL (mV/V)	69.143	61.140	49.143	40.143	41.52%
QF ($uS - dec/mV$)	3.56	4.0	4.79	5.66	58.98%
g_m (S)	2.36×10^{-4}	2.62×10^{-4}	3.07×10^{-4}	3.55×10^{-4}	50.42%
TGF (V^{-1})	$0.91 \times 10^{+2}$	$0.95 \times 10^{+2}$	$1.02 \times 10^{+2}$	$1.07 \times 10^{+2}$	17.58%
A_v (dB)	$1.70 \times 10^{+2}$	$2.28 \times 10^{+2}$	$4.08 \times 10^{+2}$	$6.94 \times 10^{+2}$	308.23%
$V_{EA}(V)$	2.48	2.85	3.79	5.10	105.64%
R_{out} (ohm)	$0.808 \times 10^{+6}$	$1.0 \times 10^{+6}$	$1.60 \times 10^{+6}$	$2.46 \times 10^{+6}$	204.45%
C_{gg} (F)	1.91×10^{-17}	2.37×10^{-17}	3.27×10^{-17}	4.55×10^{-17}	138.21%
F_t (Hz)	$3.49 \times 10^{+12}$	$3.31 \times 10^{+12}$	$3.17 \times 10^{+12}$	$2.92 \times 10^{+12}$	16.33%
GFP (Hz)	$5.52 \times 10^{+14}$	$7.0 \times 10^{+14}$	$11.90 \times 10^{+14}$	$18.40 \times 10^{+14}$	233.33%
TFP (Hz/V)	$5.56 \times 10^{+13}$	$5.56 \times 10^{+13}$	$5.91 \times 10^{+13}$	$6.06 \times 10^{+13}$	8.99%
GTFP (Hz/V)	$4.16 \times 10^{+15}$	$5.47 \times 10^{+15}$	$9.68 \times 10^{+15}$	$15.80 \times 10^{+15}$	279.80%

Table 6. Comparison of the performance parameters of VS-HOI-GS-FeFinFET with the existing literature.

Reference	$V_{ds}(V)$	Device structure	$I_{off}(A)$	$I_{on}(A)$	t_{fe}(nm)
This work	0.4	VS-HOI-GS-FeFinFET	1.38×10^{-12}	1.37×10^{-4}	4
[44]	0.1	Fe-HZO-GeFinFET	0.88×10^{-10}	5.0×10^{-5}	—
[33]	1	NC-FinFET	1.43×10^{-12}	1.80×10^{-5}	1.7
[45]	—	Fe-FinFET	2.10×10^{-10}	3.30×10^{-6}	7
[46]	0.1	HZO Fe-FinFET	8.90×10^{-12}	1.0×10^{-6}	9
[47]	0.5	NC-FinFET	4.20×10^{-11}	3×10^{-5}	5

5. Conclusion

In this paper, initially, performance of FeFinFET and VS-HOI-FeFinFET is compared for different parameters and it is found that VS-HOI-FeFinFET with Al_2O_3 as gate oxide performed better in comparison to FeFinFET on all examined parameters such as 97.849% reduction in leakage current and 35.984% increment in drain current which consequently results the switching ratio to increase around 61 times. VS-HOI-FeFinFET(Al_2O_3) also displays significant improvement in threshold voltage and subthreshold swing. Thus VS-HOI-FeFinFET is further analysed for gate stacked configuration for different gate stacked dielectric materials. In subsequent parts, this paper presents the numerical study of VS-HOI-GS-FeFinFET over VS-HOI-FeFinFET(Al_2O_3) while optimizing the gate stack material for upgraded static, analog, and RF performance. The C4 configuration exhibits the most enhanced performance as compared to the other three configurations as shown in table 5 with stated figure of merit (FOM) of C4 over C1. In comparison to C1, C4 shows an increase in I_{on} by 26.912% and reduction in I_{off} by 78.403% thus results in significant increment in switching ratio. Further an increment in peak transconductance by 50.423% is observed in C4 over C1 along with improved subthreshold swing with reduction by 6.869%. As compared to C1, device efficiency (TGF) and V_{th} are also enhanced in C4 configuration by 17.582% and 7.692%. Other analog parameters such as A_V, V_{EA} and R_{out} also shows remarkable improvement in C4 with increment by 308.235%, 105.645% and 204.455% respectively as compare to C1. Also performance optimization of VS-HOI-GS-FeFinFET with variation in mole fraction of germanium is explored for various analog metrics. Further, RF parameters like GFP also gets enhanced by 233.33% with slight improvement in TFP and GTFP by 279.80% for C4 over C1 configuration. Along with these parameters, improved ability of C4 for enhanced amplification with minimum distortion is depicted by increased gate capacitance and reduced unity gain cut off frequency by 138.21% and 16.332% respectively over C1, makes the device suitable for various high performance Analog and RF applications.

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Data availability statement

The data cannot be made publicly available upon publication because the data can be misused by the third party. The data that support the findings of this study are available upon reasonable request from the authors.

Declarations

Funding statement

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Conflict of interests

The authors declare that they are not aware of any disagreement regarding personal ties or interests that might have impacted the work represented in this publication.

Availability of data & material

The authors mentioned above have all the relevant data associated with this research work and will be dedicated to sharing that they will be asked to do so in the future.

Authors' contribution

All authors contributed to the study's conception and design.

Compliance with ethical standard

The authors have seen all the Ethical Standards and will suppose to follow them in the future.

Consent to participate & for publication

Since the concerned research paper is based on the 'non-life science journal.' So, 'Not Applicable' here. However, the authors have gone through all journal policies and consented to the authorities for further processing.

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Unveiling the Impact of Interfacial Trap Charges on Strained VS-FeFinFETs for Improved Reliability:Device to Circuit Level Assessment

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***Abstract*—This paper focuses on the device to circuit level assessment of Si/SiGe strained vertically stacked ferroelectric based FinFETs (VS-FeFinFETs) for improved reliability under the influence of interfacial trap charges (ITCs) at the semiconductor/oxide interface. The device is designed with the amalgamation of several advanced technologies such as SOI, strained tri-layered silicon channel system along with the integration of ferroelectric material in superior gate controlled FinFET. Gate engineering has also been incorporated to further improve the device's reliability against ITCs, forming hetero dielectric vertically stacked ferroelectric based FinFET (HD-VS-FeFinFET) and it is found to possess superior analog, linearity, and harmonic distortion performance. It shows 91.48% reduction in leakage current resulting in 13 times increment in switching ratio along with improvement in quality factor by 46.01% , transconductance by 32.77% , and device efficiency by 26.54% with negligible variations due to ITCs as compared to VS-FeFinFET. Various linearity and harmonic parameters also improved and showed negligible average variations like 4.72% (177.15%) in VIP2 and 6.525% (25.3%) in 1-dB compression point for HD-VS-FeFinFET (VS-FeFinFET) against different ITCs polarity making it more reliable for low power microwave and distortion less wireless communication applications. Further logic circuit application of HD-VS-FeFinFET based CMOS inverter has been analysed and it shows improvement by 17.9% in transition range, 51.674% in voltage gain along with ITCs induced average variation of 3.66% (15.88%) in noise margin for HD-VS-FeFinFET(VS-FeFinFET) based circuit thus led to its development with enhanced functionality, reliability, and performance, poised to shape the landscape of modern electronics.**

***Index Terms*—FinFET, ferroelectric, strain, Si/SiGe, CMOS, HD-VS-FeFinFET, interfacial trap charges, reliability, inverter.**

I. Introduction

TECHNOLOGY advancements like Internet of Things, mobile smart devices, and logic in memory (LiM) computing have increased the demand for high-performance and low-power electronic devices [1]. To meet this increasing demand, devices using CMOS technology are being rapidly scaled down and they are approaching their fundamental limits now. In such a scenario, various short channel effects (SCEs) begin to predominate at submicron dimensions and degrade the device performance [2].

As documented in different works of literature, several engineering techniques and device designs, including dual gates, recessed channels, trenched gates, trigate FinFETs, FeFETs, etc., have been used to get around these restrictions [3]. Among these structures, FeFinFET(Ferroelectric based FinFET) is considered a viable contender for the ultimate CMOS device structure due to its resilience against SCEs and enhanced transistor performance. By blending the advantages of FinFET technology with the unique qualities of ferroelectric materials, the FeFinFET marks a burgeoning field within semiconductor technology [4]. Further to lessen the vulnerability to negative effects of parasitic capacitance, SOI (Silicon On Insulator) technology is adopted in the current structure to create the SOI FeFinFET. In the era of energy-efficient computing, this isolation improves the transistor's electrostatic control, enabling more effective switching and lowering the power consumption [5].

Silicon has been the cornerstone of the semiconductor industry for decades, but its limitations in meeting the demand of progressing technology make it necessary to look beyond silicon channel materials like SiGe, GaAs, group III-IV semiconductors, and alloy-based materials to further enhance the performance of SOI FeFinFET. In our previous work, we have analyzed the performance of vertically stacked ferroelectric-based FinFET involving a strained-silicon channel system using a compound semiconductor material (SiGe). The results showed that the device has showcased improved performance against SCEs and can be further scaled down as compared to FeFinFET [6].

At the heart of FeFinFETs lies the interface between oxide and semiconductor layers, where the dynamics of interfacial trap charges (ITCs) exert a profound influence on device performance and functionality. The complexity introduced by ITCs at the semiconductor-oxide (S/O) interface in FeFinFETs calls for careful research. The dynamics of these ITCs are affected by various elements such as material composition, processing techniques, and operational environment. The OFF-state performance deteriorates and the threshold voltage is shifted by these trap charges [7]. To maximize the performance of device and realize their full potential for a variety of applications, it is imperative to comprehend the behavior of ITCs. There are

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various factors responsible for occurrence of these ITCs. Firstly, the creation of dangling bonds due to disruption of atomic lattice at the S/O interface which leads to creation of energy states with in the bandgap of the semiconductor. Secondly, contamination of the surface with impurities can introduce localized states that trap charges [8]. Further, other factors may be thermal oxidation process during growth of oxide layer, high energy radiation during ion implantation, electrical stress during operation or testing, mechanical stress during deposition or thermal expansion can break bonds or introduce defects, ultimately creating ITCs. Controlling ITCs is crucial for enhancing the performance and reliability of semiconductor devices. Various potential methods can be incorporated in the devices to mitigate these ITCs such as passivation techniques, optimized thermal oxidation, surface cleaning before deposition, high-k dielectric materials, low-damage deposition techniques like atomic layer deposition (ALD), etc [9]. In this paper, gate stack engineering with heterogeneous gate dielectric (Al_2O_3+HfO_2) is incorporated in vertically stacked ferroelectric based FinFET to form HD-VS-FeFinFET, a novel combination of Si/SiGe strained tri-layered channel-engineered, heterostructure on insulator FeFinFET, and has been examined to minimize the effect of ITCs. The combination leverages the passivation properties of Al_2O_3 and the high-k benefits of HfO_2[10]. Al_2O_3 is used as an interfacial layer (t_{ox1}), which is known for high-quality interface with semiconductors leading to reduced dangling bonds and ITCs. Al_2O_3 has a high bandgap (∼9 eV), which minimizes creation of energy states, further reducing trap density at the interface [9]. Then, the high-k nature of HfO_2 reduces the electric field stress at the interface, thereby minimizing the generation of new traps. HfO_2 also exhibits good thermal stability, reducing defect formation during high-temperature processing. Thus, the stacked structure minimizes the density of trap charges at both the interface and within the dielectric layers. These dielectrics are also compatible with ALD processes, allowing precise thickness and composition control [11]. Thus, the combination of Al_2O_3 and HfO_2 uses their complementary properties, such as Al_2O_3's superior passivation and HfO_2's high-k dielectric performance, make them ideal for next-generation electronic devices requiring high efficiency and robust reliability [10].

In this article, the detailed analysis of static, analog, linearity, and harmonic distortion performance under the influence of ITCs is done for both the devices. Further, the work is extended to discuss the influence of ITCs at the circuit level by comparing the performance of HD-VS-FeFinFET based CMOS inverter with VS-FeFinFET based CMOS inverter for improved efficiency and reliability. This work is divided into five sections: Section II includes all the specifications regarding the device structure; Section III explains the simulation framework and fabrication feasibility; Section IV provides the results and discussion; and Section V concludes the paper.

II. Device Structure

Fig. 1(a) depicts the 3-dimensional structure of HD-VS-FeFinFET, while Fig. 1(b) and (c) respectively shows the device's vertical and lateral 2-dimensional view chopped through its fin. The gate length (L_g) considered for the device is fixed at 20 nm where silicon-doped hafnium oxide (HfO_2 FE) is used as the ferroelectric material with thickness (t_{fe}) fixed at 6 nm with total gate oxide dielectric thickness (t_{ox}) fixed at 1 nm. The total gate oxide is composed of a heterogeneous dielectric stack consisting of equal proportion of Al_2O_3 and HfO_2, each with a thickness of 0.5 nm. So, the combined thickness of ferroelectric layer and gate oxide dielectric is 7 nm. The height and width of the fin are taken as 30 nm and 8 nm respectively. A tri-layered strained-silicon channel system is formed with the help of SiGe sandwiched between two silicon layers as Si-$Si_{0.7}$ $Ge_{0.3}$-Si (where $Si_{0.7}$ $Ge_{0.3}$ represents that the mole fraction of Si and Ge is taken as 0.7 and 0.3 respectively). The doping concentration of source/drain is fixed as 1×10^{20} cm^{-3} with n-type and that of channel is 1×10^{16} cm^{-3} with p-type with uniform profile. The length of the source/drain electrodes ($L_{s/d}$) is fixed at 20 nm. In addition, a metal gate with a work function of 4.65 eV, which has excellent thermal stability and is compatible with CMOS processing, is utilized in this device to prevent any poly-depletion effect that is common in polysilicon gates. Further, to exploit the advantages of SOI technology, the entire heterostructure FeFinFET is built on an insulator SiO_2 box whose width, height, and length are kept 32 nm, 5 nm, and 62 nm respectively. To unveil the intricacies of ITCs on the device reliability and performance, ITCs with different polarity have been introduced at the S/O interface with trap charge density to be fixed at 10^{12} cm^{-2} based on formerly reported literature [7], [8], [9].

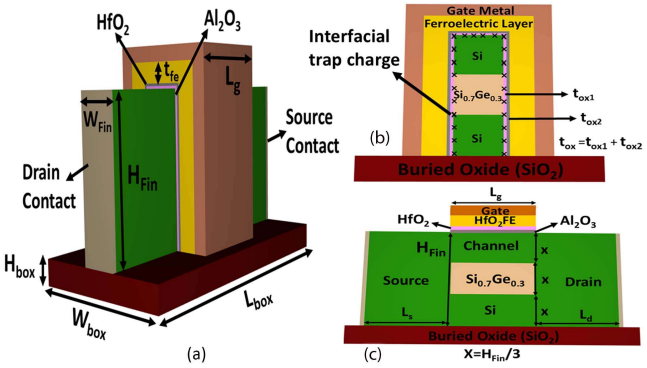

Fig. 1. (a) 3D schematic view of HD-VS-FeFinFET. (b) Vertical cross-sectional view of HD-VS-FeFinFET. (c) Lateral cross-sectional view of HD-VS-FeFinFET.

III. Simulation Framework and Fabrication Feasibility

All the simulations have been carried out using Genius 3D TCAD simulator by Cogenda. For the validation of the models used in the simulator tool, the TCAD simulation result for Silicon on Insulator (SOI) FinFET structure has been calibrated with experimental data [12], and a reasonably good agreement between the two results validates the various models used in the study as displayed by Fig. 2(a). The simulation setup includes the drift-diffusion model level 1 (DDML1) which keeps the lattice temperature constant throughout the solving procedure, coupled with consistent Poisson and continuity equations

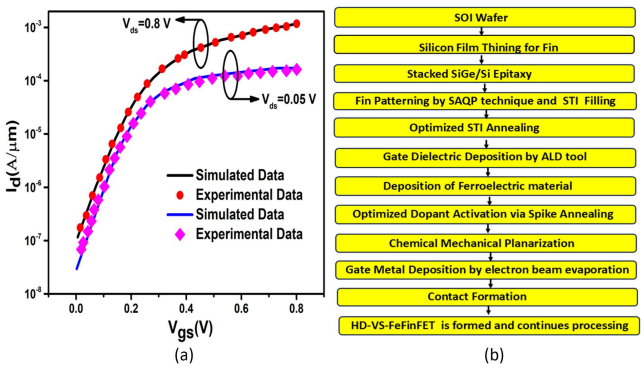

Fig. 2. (a) Experimental and simulated transfer characteristic for Silicon on Insulator (SOI) FinFET at $V_{ds} = 0.05$ V and $V_{ds} = 0.8$ V. (b) Fabrication process flow chart for HD-VS-FeFinFET, where SiGe is silicon-germanium, SAQP is self-aligned quadruple patterning, STI is shallow trench isolation, and ALD is atomic layer deposition technique.

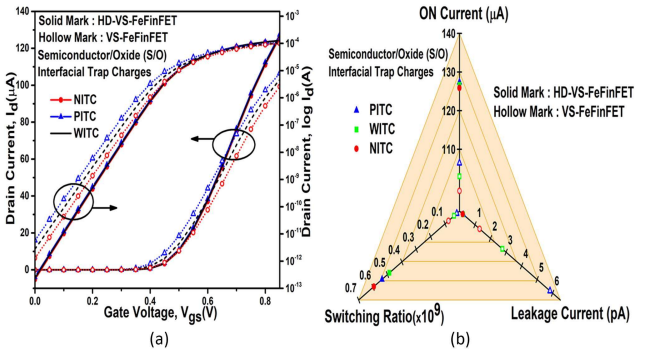

Fig. 3. Transfer characteristics of HD-VS-FeFinFET and VS-FeFinFET in (a) linear and log scale at $V_{ds} = 0.4$ V. (b) Comparison of different device characteristics such as ON current (I_{on}), leakage current (I_{off}) and switching ratio (I_{on}/I_{off}) in presence of different ITCs at $V_{ds} = 0.4$ V.

to govern the carrier transport phenomena for the holes and the electrons. The temperature and doping-dependent carrier recombination-generation phenomenon are accurately captured by Shockley-Read-Hall (SRH) recombination and Auger models [13]. Further, Lombardi mobility model for silicon and Philips mobility model for SiGe are used to consider the mobility degradation at the semiconductor-oxide interface [6]. Lucent model is used to consider the high-field mobility effects along with hot carrier models for capturing the effect of hot carriers. To check the velocity saturation and mobility of carriers, the velocity saturation model, and Esurface models are activated. The density gradient method is also used to incorporate quantum confinement phenomena along with the Fermi-Dirac carrier statistics model [14]. Further, the position and polarity of ITCs in the device are mentioned using the INTERFACE statement along with Trap models to capture the associated mechanisms [9], [14]. A few abbreviations are used in this paper such as PITC - positive interfacial trap charge, NITC - negative interfacial trap charge, WITC - without (neutral) interfacial trap charge.

Further, Fig. 2(b) displays the fabrication feasibility of the HD-VS-FeFinFET using a step-by-step fabrication process flowchart. As the starting material SOI wafer is used with a thick buried oxide layer and thick silicon film followed by silicon film thinning for fin. Afterwards stacked SiGe/Si tri-layer were epitaxially grown by reduced-pressure chemical vapor epitaxial deposition. Thereafter, fin patterning is done using the self-aligned quadruple patterning (SAQP) technique followed by shallow trench isolation (STI) filling and an optimized STI densification annealing which is performed with a rapid thermal annealing (RTA) at an optimized temperature. The gate dielectric is deposited on the silicon interfacial layer by ALD followed by ferroelectric layer deposition over the gate oxide using ALD technique. The drain and source regions are implanted, and the dopants of these regions are activated using spike annealing followed by chemical mechanical planarization for smoothening the surface. Metal gate is deposited using electron beam evaporation at room temperature on the top of the ferroelectric layer. The source/drain metal contacts are deposited by electron beam evaporation followed by lift-off process. This completes the process of manufacturing the HD-VS-FeFinFETs [15], [16].

IV. Result and Discussion

A. Influence of ITCs on Static and Analog Performance

In this section, the effect of ITCs polarity at the S/O interface is analysed to study the static and analog performance for both the devices (HD-VS-FeFinFET and VS-FeFinFET) at supply voltage $V_{ds} = 0.4$ V and at constant temperature 300 K. Fig. 3 displays the transfer characteristics of both the devices with different polarity. The presence of ITCs leads to altercation in flat band voltage (V_{fb}) as given by (1), where q is the electronic charge, N_{it} is the ITCs density and C_{ox} is gate oxide capacitance.

$$V_{\mathrm{fb}} = \frac{qN_{\mathrm{it}}}{C_{\mathrm{ox}}} \tag{1}$$

The changes in V_{fb} caused by PITC/NITC leads to modification in threshold voltage (V_{th}) as related by (2), where x_t is maximum space charge width and ψ_{fp} is built in potential.

$$V_{\mathrm{th}} = V_{\mathrm{fb}} + \psi_{\mathrm{fp}} + \frac{qN_{\mathrm{a}}x_{\mathrm{t}}}{C_{\mathrm{ox}}} \tag{2}$$

This modification in V_{th} leads to change in device characteristics thus change the ON current (I_{on}) and leakage current (I_{off}) of the device as shown in Fig. 3(a) [17]. The use of high-k dielectric led to reduced interface states and traps at the S/O interface which improves the carrier mobility within the channel region as can be very well observed in elevated I_{on} of HD-VS-FeFinFET. The PITC (NITC) increases (decreases) the ON current by 0.59% (0.62%) and 3.35% (3.64%) in HD-VS-FeFinFET and VS-FeFinFET respectively. I_{off} with NITC (PITC) decreases (increases) by 11.01% (10.02%) in HD-VS-FeFinFET in comparison to deviation in VS-FeFinFET in presence of PITC (NITC) by 111% (53.1%), as depicted in Fig. 3(b) which confirms that the transfer characteristics of HD-VS-FeFinFET are less affected by ITCs, proving it more reliable in contrast to VS-FeFinFET. Fig. 4(a) shows the variation of output characteristics with drain bias for different ITC polarity. Owing to the suppression of channel hot carrier injection with

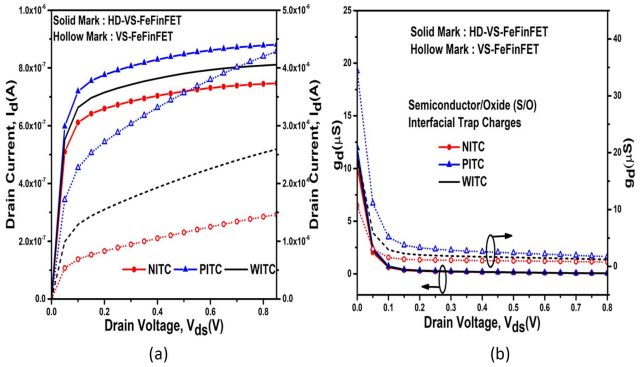

Fig. 4. Effect of ITCs on (a) drain current (I_d) and (b) output conductance (g_d) for HD-VS-FeFinFET and VS-FeFinFET at $V_{ds} = 0.4$ V.

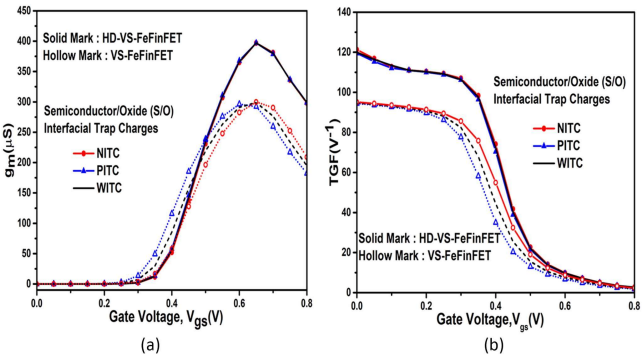

Fig. 5. Variation in (a) transconductance (g_m) and (b) device efficiency (TGF) in presence of different ITCs at $V_{ds} = 0.4$ V.

the incorporation of hetero dielectric gate engineering in HD-VS-FeFinFET, there is negligible impact on output conductance (g_d) due to ITCs as showcased in Fig. 4(b), thereby confirming its improved reliability.

Fig. 5(a) and (b) respectively shows the variation of transconductance (g_m) and device efficiency, also known as Transconductance Generation Factor (TGF) of both the devices for different ITC polarity. These are the important parameters in the design of analog circuits and Fig. 5 shows higher value of g_m and TGF for HD-VS-FeFinFET due to improved carrier mobility and better electrostatic control along with minimum variations in presence of ITCs thus depicts its enhanced efficiency and reliability of converting DC parameter (I_d) into AC parameters (g_m) as compared to its counterpart [18].

PITC(NITC) acts to decrease (increase) the threshold voltage (V_{th}) but the variation in V_{th} is minute in case of HD-VS-FeFinFET whereas the V_{th} for PITC(NITC) is decreased (increased) by 8.9% (9.3%) in VS-FeFinFET as displayed in Fig. 6(a) and Table I. ITCs introduce additional energy states within the bandgap of semiconductor material which can capture and release charge carriers leading to energy dissipation [17], [19]. This energy loss affects the overall Quality factor (QF) of the device as depicted in Fig. 6(b), as energy stored in the system is dissipated due to trap-assisted recombination and scattering mechanisms.

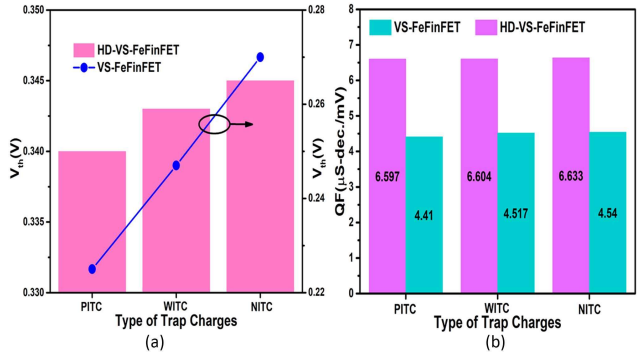

Fig. 6. Effect of ITCs on (a) threshold voltage (V_{th}) (b) quality factor (QF) of HD-VS-FeFinFET and VS-FeFinFET at $V_{ds} = 0.4$ V.

TABLE I
SUMMARY OF DIFFERENT ANALOG PARAMETERS FOR HD-VS-FEFINFET AND VS-FEFINFET UNDER THE INFLUENCE OF ITCS

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	1.06×10^{-4}	1.03×10^{-4}	9.92×10^{-4}	1.27×10^{-4}	1.26×10^{-4}	1.25×10^{-4}
I_{off} (A)	5.83×10^{-12}	2.77×10^{-12}	1.30×10^{-12}	2.62×10^{-13}	2.36×10^{-13}	2.12×10^{-13}
I_{on}/I_{off}	$1.83\times 10^{+7}$	$3.72\times 10^{+7}$	$7.65\times 10^{+7}$	$5.37\times 10^{+8}$	$4.86\times 10^{+8}$	$5.94\times 10^{+8}$
$V_{th}(V)$	0.225	0.247	0.270	0.340	0.343	0.345
QF ($\mu S - dec/mV$)	4.41	4.52	4.54	6.60	6.60	6.63
g_m (S)	2.92×10^{-4}	2.99×10^{-4}	3.0×10^{-4}	3.97×10^{-4}	3.97×10^{-4}	3.97×10^{-4}
TGF (V^{-1})	94.43	94.76	95.10	119.46	119.91	121.23
A_v (dB)	$1.42\times 10^{+2}$	$2.11\times 10^{+2}$	$3.35\times 10^{+2}$	$5.16\times 10^{+3}$	$5.78\times 10^{+3}$	$6.45\times 10^{+3}$
$V_{EA}(V)$	1.82	2.07	2.41	15.17	15.63	16.12
R_{out} (ohm)	$5.74\times 10^{+5}$	$8.19\times 10^{+5}$	$1.27\times 10^{+6}$	$1.72\times 10^{+7}$	$1.93\times 10^{+7}$	$2.16\times 10^{+7}$

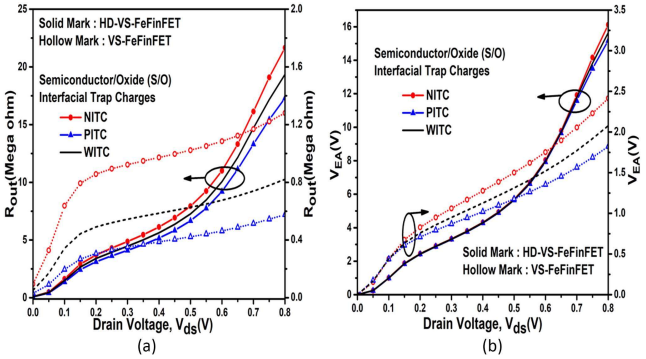

Fig. 7. Impact of ITCs on (a) output resistance (R_{out}) (b) early voltage (V_{EA}) of HD-VS-FeFinFET and VS-FeFinFET at $V_{ds} = 0.4$ V.

Fig. 7(a) shows the output resistance (R_{out}) for both the devices in presence of ITCs and higher R_{out} ensures better signal fidelity by suppressing voltage variations for changes in load resistance as shown by HD-VS-FeFinFET. High-k dielectric materials help in minimizing the variation in R_{out} caused by ITCs due to their ability to lower interface trap density and provide

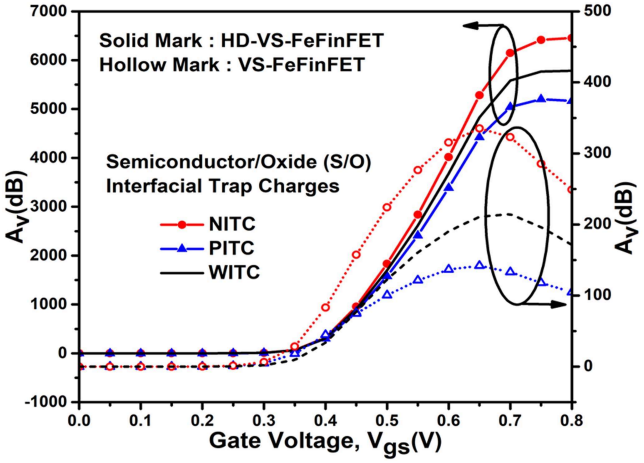

Fig. 8. Variation of intrinsic gain (A_v) for HD-VS-FeFinFET and VS-FeFinFET in presence of different ITCs at $V_{ds} = 0.4$ V.

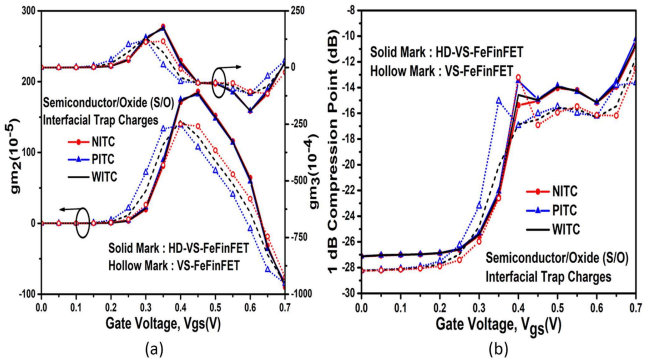

Fig. 9. Impact of ITCs on (a) higher order transconductance coefficient (g_{m2} and g_{m3}) (b) 1-dB Compression Point of HD-VS-FeFinFET and VS-FeFinFET at $V_{ds} = 0.4$ V.

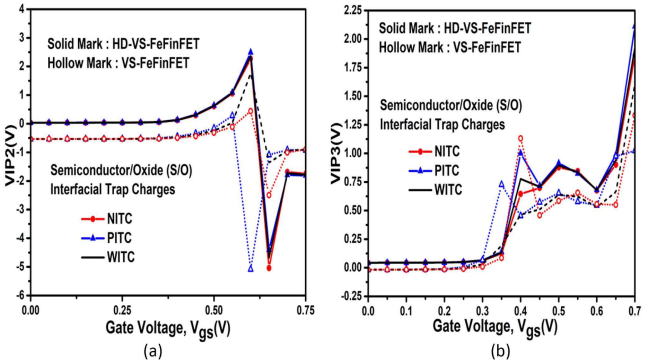

Fig. 10. Effect of ITCs on voltage intercept point (a) VIP2 (b) VIP3 of HD-VS-FeFinFET and VS-FeFinFET at $V_{ds} = 0.4$ V.

stronger electrostatic control over the channel [20], [21]. The peak value of R_{out} is increased (decreased) by 56% (29.9%) on introduction of NITC(PITC) at S/O interface of VS-FeFinFET as compared to increase (decrease) by 12% (10.6%) showing more immunity of HD-VS-FeFinFET towards ITCs.

Further, early voltage (V_{EA}) measures how quickly the output current increases in response to V_{ds} and trap charges in localized states within the semiconductor leading to deviations from ideal transistor behaviour. But owing to the implementation of heterogeneous dielectric in HD-VS-FeFinFET, there is only 3.09% (2.98%) increase (decrease) in presence of NITC (PITC) as compared to 12.3% (16.3%) increase(decrease) in its counterpart as shown in Fig. 7(b), making it more apt for high-speed analog and mixed-signal circuits [22]. Fig. 8 displays the comparison plots of intrinsic gain (A_v) for both the devices in presence of ITCs and it is found that with higher A_v along with less variability due to ITCs, HD-VS-FeFinFET is more immune and reliable for analog performance as compared to VS-FeFinFET that shows huge deviations of 45.4% (38.8%) increment (decrement) for NITC(PITC).

B. Influence of ITCs on Linearity, Harmonic and Intermodulation Distortion Performance

Designing modern circuits and communication systems requires improved linearity and minimal distortion of signals to ascertain desired output at the receiver end. To take into account the non linearity issue, the influence of ITCs at S/O is investigated on various linearity and distortion parameters such as g_{m2}, g_{m3}, VIP2, VIP3, 1 dB compression point, IMD3, IIP3, etc for both the devices, HD-VS-FeFinFET and VS-FeFinFET. The importance of these higher-order derivatives lies in their direct influence on circuit gain, distortion, linearity, wireless performance, and power consumption. Designers must precisely analyze and optimize these parameters to meet the particular requirements of the application, thereby guaranteeing the circuit's reliability and overall success [23].

The higher-order coefficients of transconductance provide an estimate about the non-linearity in a device. g_{m2} (g_{m3}) is the second (third) order transconductance coefficient that quantifies the second (third) order nonlinearity in a MOSFET, affecting even (odd) order distortion in circuits [24]. Fig. 9(a) displays that the incorporation of heterogeneous dielectric in HD-VS-FeFinFET results into negligible deviation in g_{m2} and g_{m3} due to ITCs as compared to increase (decrease) in peak value in VS-FeFinFET in presence of NITC (PITC). Fig. 9(b) shows another important parameter, 1 dB compression point which denotes the level of input power at which shifting of output power from linearity by 1 dB occurs [25]. The figure displays higher value of 1 dB compression point for HD-VS-FeFinFET due to enhanced g_m thus ensures reduced signal distortion. Also, there is negligible increase (decrease) of 7.57% (5.48%) in 1 dB compression point on existence of PITC(NITC) in HD-VS-FeFinFET as compared to 27% (23.6%) variation in VS-FeFinFET for PITC(NITC).

Voltage intercept point (VIP) is an important parameter used to describe the linearity of the device. VIP2 (VIP3) is the second (third) order voltage intercept point that depicts input voltage level at which the second (third) order harmonics equals the fundamental signal [22]. Higher VIP2 and VIP3 indicates better linearity and reduced distortion. Fig. 10(a) displays that along with higher value of VIP2, the influence of ITCs is negligible on HD-VS-FeFinFET due to hetero dielectric engineering. The

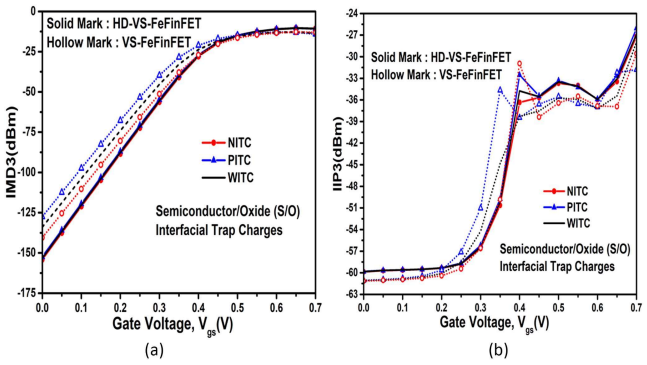

Fig. 11. Impact of ITCs on (a) third order intermodulation distortion power (IMD3) (b) third order intercept input power (IIP3) of HD-VS-FeFinFET and VS-FeFinFET at $V_{ds} = 0.4$ V.

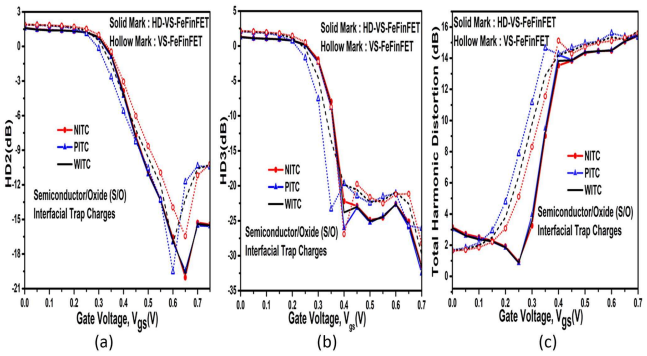

Fig. 12. Effect of ITCs on harmonics distortion (a) HD2 (b) HD3 (c) THD for HD-VS-FeFinFET and VS-FeFinFET at $V_{ds} = 0.4$ V.

presence of PITC(NITC) increases (decreases) the amplitude of VIP2 by 5.31% (4.14%) in case of HD-VS-FeFinFET. However, for VS-FeFinFET, the decrement in VIP2 is 57.3% (297%) in presence of NITC(PITC) in terms of WITC. Similar pattern is noticed in case of VIP3, its peak increases (decreases) only by 2.1% (2.03%) in presence of PITC(NITC) with respect to WITC whereas PITC(NITC) varies the VIP3 by 2.15% (7.57%) in VS-FeFinFET.

$$HD2 = \frac{1}{2} V_{\mathrm{a}} \frac{(\partial g_{\mathrm{m}}/\partial V_{\mathrm{gs}})}{2 g_{\mathrm{m}}} \tag{3}$$

$$HD3 = \frac{1}{4} V_{\mathrm{a}}^2 \frac{(\partial^2 g_{\mathrm{m}}/\partial V_{\mathrm{gs}}^2)}{6 g_{\mathrm{m}}} \tag{4}$$

$$THD = \sqrt{HD2^2 + HD3^2 + \cdots ..} \tag{5}$$

Third order intermodulation distortion power (IMD3) and third order intercept input power (IIP3) are other critical parameters of linearity in wireless applications. IMD3 refers to the distortion caused by third-order non linearities when two signals mix, producing undesired spectral components near the fundamental frequencies [24]. For better linearity, minimum value of IMD3 is desired as depicted by HD-VS-FeFinFET in Fig. 11(a). Further, the influence of ITCs on carrier mobility is less pronounced with high-k dielectrics which results in negligible influence on IMD3 in comparison to rise(fall) by 4.81% (4.89%) for PITC(NITC) in VS-FeFinFET. IIP3 is that extrapolated input power point where 1st and 3rd order harmonic power become equal. Higher IIP3 indicates better linearity [25]. Fig. 11(b) shows that IIP3 is nearly unaffected in presence of ITC for HD-VS-FeFinFET thus making it more reliable as compared to its counterpart. Furthermore, at low V_{gs}, IIP3 of HD-VS-FeFinFET is higher than the IMD3, which implies improved device power and performance by minimizing the hot carrier effect. In Fig. 11(b), at high V_{gs}, IIP3 of HD-VS-FeFinFET is lower than the IMD3, which is opposite to the trend at low V_{gs}. This occurs due to voltage-dependent non-linearities. Gate voltage significantly affects the channel's electrostatic potential, carrier mobility, and the non-linear terms in the device's transconductance. At low V_{gs}, the device operates in the subthreshold or near-threshold region, where second-order nonlinearities dominate due to weak inversion effects. These distortions influence IMD3 more strongly, making IIP3 appear relatively higher. On the other hand, at high V_{gs}, the device is in strong inversion, where third-order nonlinearities become more prominent. This increases the impact on IIP3, reducing its relative value compared to IMD3 [25], [26].

To evaluate the intricacies of ITCs on the harmonics distortion characteristics, 2nd order harmonics (HD2), 3rd order harmonics (HD3), and total harmonic distortion (THD) of both the devices are analyzed in presence of ITCs with different polarity as given by (3), (4), (5) respectively where amplitude of V_a is taken as 50 mV. HD2 (HD3) measures the second (third) order nonlinearities producing signals at twice (thrice) the input frequency. And the measure of all harmonic distortion components relative to fundamental frequency is accounted as THD. The values of these parameters should be as low as possible for lesser distortion in device operation [26]. Fig. 12 displays the impact of ITCs on HD2, HD3, and THD with change in V_{gs} and it is found that HD-VS-FeFinFET shows negligible variations due to ITCs as compared to increment(decrement) in harmonic distortions with rise in V_{gs} for VS-FeFinFET due to PITC(NITC). High-k materials tend to reduce the density of interface traps as compared to conventional dielectrics due to reduced dangling bonds at the interface. This reduction minimizes charge-trapping and de-trapping, leading to lower variations in harmonic distortions caused by PITC or NITC. Also, the high-k dielectric in HD-VS-FeFinFETs increases the gate capacitance, strengthening the gate's control over the channel potential. As a result, the channel becomes less sensitive to perturbations caused by ITCs. Thus, HD-VS-FeFinFET is proved to be more immune against any nonlinearity and distortion that arise from ITCs.

C. Circuit Level Analysis

To analyze the impact of ITCs of different polarity on HD-VS-FeFinFET based CMOS inverter, a required setup is designed on Cogenda Visual TCAD simulator with n-channel and p-channel HD-VS-FeFinFET isolated electrically with the help of 60 nm SiO_2 spacer and later its performance has been compared with VS-FeFinFET based CMOS inverter. Fig 13(a) shows the schematic of the CMOS inverter circuit where V_{dd}, V_{out} and

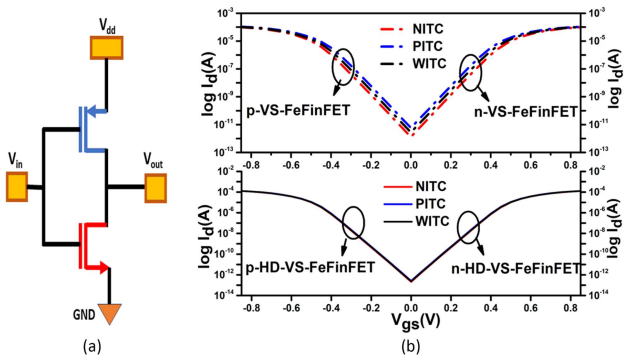

Fig. 13. (a) Schematic diagram of CMOS Inverter. (b) Threshold voltage matching curve for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs.

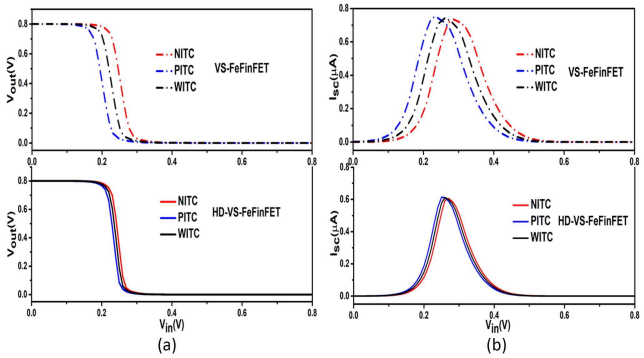

Fig. 14. Effect of ITCs on (a) Voltage transfer characteristics and (b) switching current of HD-VS-FeFinFET and VS-FeFinFET based inverter.

V_{in} are the supply voltage, output voltage, and input voltage respectively. Initially threshold matching of the n-channel and p-channel configuration is done for both the devices as displayed in Fig. 13(b) in presence of different ITCs. The V_{gs} is varied from −0.85 to 0.85 V with dual work function metal (DWFM) integration scheme.

It is very much required to examine the crucial parameters to estimate the performance of inverter and for this, voltage transfer characteristics (VTC) for both the inverters in presence of ITCs of different polarity is analyzed as shown in Fig. 14(a). It is visible that the transition range (TR) of HD-VS-FeFinFET based inverter is more sharper than the VS-FeFinFET based inverter due to improved electrostatic control and reduced SCEs, which ensures high speed switching [27], [28]. Further, the switching threshold voltage (V_{TH}) or the transition voltage, at which $V_{in} = V_{out}$ on the VTC curve, is examined and it is found to be 0.247 V for HD-VS-FeFinFET with minimal variation due to ITC's polarity as compared to 0.238 V for VS-FeFinFET in case of WITC.

ITCs can generate additional spurious signals that can interfere with the proper functioning of the inverter. Noise Margin (NM) is a crucial parameter to depict the noise immunity of the circuit and its value should be higher for better tolerance to undesirable variations with more reliable operation. The noise margin for low signal levels (NM_L) and the noise margin for high signal levels (NM_H) is defined by (6) and (7). Here, V_{OL} and V_{OH} are minimum and maximum output voltage when corresponding output levels are logic 0 and logic 1 respectively. V_{IL} and V_{IH} are maximum and minimum input voltage which can be interpreted as logic 0 and logic 1 respectively [29]. It is found as shown in Table II that with higher NM due to sharper switching characteristics along with negligible deviation under the influence of ITCs, HD-VS-FeFinFET is more reliable for digital circuits and applications.

TABLE II
PERFORMANCE COMPARISON BETWEEN HD-VS-FEFINFET AND VS-FEFINFET BASED INVERTER UNDER THE INFLUENCE OF ITCS WITH DIFFERENT POLARITY

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
V_{IL} (mV)	143.473	169.841	196.792	183.994	191.341	198.031
V_{IH} (mV)	270.794	285.762	297.713	267.452	274.142	280.174
V_{OL} (mV)	5.77×10^{-8}	1.39×10^{-7}	3.41×10^{-7}	3.60×10^{-8}	4.58×10^{-8}	3.35×10^{-8}
V_{OH} (mV)	799.99	800	800	800	800	800
NM_L (mV)	1.43×10^{2}	1.70×10^{2}	1.97×10^{2}	1.84×10^{2}	1.91×10^{2}	1.98×10^{2}
NM_H (mV)	529.196	514.238	502.287	532.548	525.858	519.826
TR (mV)	102.321	100.921	100.921	83.458	82.801	82.143

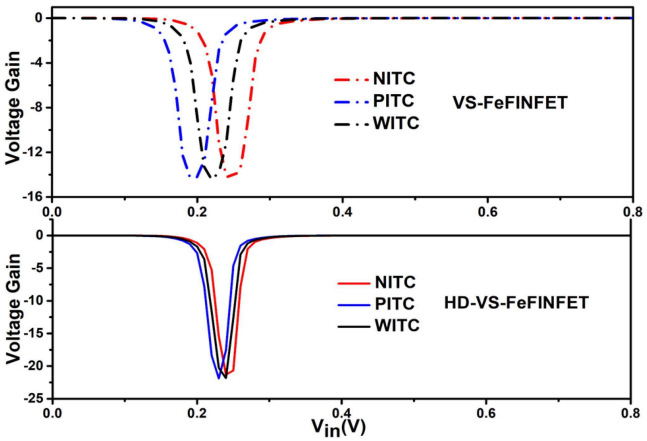

Fig. 15. Impact of ITCs polarity on Voltage Gain of HD-VS-FeFinFET and VS-FeFinFET based inverter.

$$NM_{\mathrm{L}} = V_{\mathrm{IL}} - V_{\mathrm{OL}} \tag{6}$$

$$NM_{\mathrm{H}} = V_{\mathrm{OH}} - V_{\mathrm{IH}} \tag{7}$$

Fig. 14(b) displays the switching current (I_{sc}) of both the logic circuits in presence of different ITCs. The static current (at $V_{in} = 0$ V, $V_{in} = V_{dd}$) is less than 1 pA, confirming significantly lower static power dissipation and improved energy efficiency for HD-VS-FeFinFET along with negligible variations under the influence of ITCs with different polarity [27]. The effect of ITCs on inverter gain for both the devices is shown in Fig. 15. An increase of 51.674% in gain due to higher g_m and R_{out} along with minimum deviations due to ITCs is observed in HD-VS-FeFinFET based inverter as compared to VS-FeFinFET based

inverter thus proved to be more desirable in various applications where signal fidelity and amplification are crucial.

V. Conclusion

This paper presented a comprehensive assessment from device to circuit level showing the influence of ITCs on various analog, linearity, and distortion parameters of hetero dielectric gate engineered Si/SiGe strained vertically stacked ferroelectric based FinFET (HD-VS-FeFinFET). The strained channel system and engineering modify the band structure and increase the carrier mobility thus improving the transistor's performance and making it more desirable for many electronic applications. The process improves the device performance in terms of I_{on}, I_{off}, V_{th}, g_m, VIP2, VIP3, IIP3, IMD3, 1-dB compression point, and harmonic distortion parameters. At the device level, HD-VS-FeFinFET outperforms VS-FeFinFET with improvement in various analog parameters like A_v by 27 times, V_{EA} by 7.5 times, and R_{out} by 23 times along with minimal average variations of 11.15% , 3.03% and 11.39% respectively in contrast to 45.73% , 14.24% and 42.48% for VS-FeFinFET under the influence of ITCs. Further, circuit level comparison has also been made for CMOS inverter and it is found that HD-VS-FeFinFET based inverter offers improved performance in terms of noise margin, I_{sc}, and transition range along with more tolerance against ITCs. With the comprehensive analysis done on the intricacies of ITCs from device to circuit level, this work provides insights into the development of HD-VS-FeFinFET with enhanced functionality, reliability, and performance, poised to shape the landscape of modern electronics.

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Research paper

Reliability analysis of the intricacies of interfacial trap charges in HD-VS-FeFinFET and its applicability as CMOS inverter

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Inverter

ABSTRACT

This paper investigates the impact of semiconductor-oxide interfacial trap charges (ITCs) on the performance of Si/SiGe strained hetero dielectric vertically stacked ferroelectric-based FinFET (HD-VS-FeFinFET), formed with the novel amalgamation of several advanced technologies. ITCs induced degradation is a major concern for device reliability, and this study examines the reliability of HD-VS-FeFinFET by analyzing: (1) temperature affectability on ITCs, (2) impact of varying ITC densities and polarities, and comparing the results with vertically stacked ferroelectric-based FinFET (VS-FeFinFET). Temperature affectability reveals that HD-VS-FeFinFET exhibits better reliability with less average variations against ITCs at all operating temperatures such as 10.65% in leakage current (I_{off}) and 11.39% in output resistance (R_{out}) at 300 K which further decreases to 8.13% in I_{off} and 7.76% in R_{out} at 400 K in contrast to huge variation shown by VS-FeFinFET like 82.05% in I_{off} and 43.10% in R_{out} at 300 K along with 59.35% in I_{off} and 29.86% in R_{out} at 400 K. Further, the analysis done at various ITCs densities and polarities reveals that, at higher donor trap charge density of 10^{13} cm^{-2}, the device performance alters significantly for VS-FeFinFET with degradation in I_{off} by 552 times in comparison to HD-VS-FeFinFET which degrades only by 2.52 times, thus making it more reliable under varying environmental conditions. Lastly, HD-VS-FeFinFET based CMOS inverter shows improved immunity towards ITCs with negligible variations at all operating temperatures, thus with reliable circuit-level operation, HD-VS-FeFinFET proves itself an ideal choice for advanced logic circuits and low-power electronic applications in dynamic environments.

1. Introduction

The growing demand for high-performance and low-power electronic devices can be attributed to technological breakthroughs such as logic in memory (LiM) computing, mobile smart gadgets, and the Internet of Things. In order to keep up with the rising demand, CMOS-based devices are being scaled down [1]. But as they are approaching their fundamental limits, various short channel effects (SCEs) begin to predominate at submicron dimensions and degrade the device performance [2,3].

Numerous engineering methods and device designs, such as dual gates, recessed channels, trenched gates, trigate FinFETs, FeFETs, etc., have been employed to circumvent these limitations, as reported in several literary works [4–6]. Among these structures, FeFinFET (Ferroelectric based FinFET) is considered a viable contender for the ultimate CMOS device structure due to its resilience against SCEs and enhanced transistor performance [7]. The FeFinFET, which uses ferroelectric materials to control charge distribution, is a developing area in semiconductor technology by combining the benefits of FinFET technology with the special properties of ferroelectric materials [8,9]. Further to lessen the vulnerability to negative effects of parasitic capacitance, SOI (Silicon on Insulator) technology is adopted in the current structure to create the SOI FeFinFET. This isolation enhances the transistor's electrostatic control, allowing for more efficient switching and reduced power usage in the era of energy-efficient computing [10,11].

For many years, silicon has been the mainstay of the semiconductor industry. However, due to its limitations in meeting the demands of advancing technology, group III-IV semiconductors, SiGe, GaAs, and alloy-based materials are alternatives that must be considered in order to further improve the performance of SOI FeFinFET [12]. In our earlier research, we used a compound semiconductor material (SiGe) to examine the performance of vertically stacked ferroelectric-based FinFETs incorporating strained-silicon channel system. The outcomes demonstrated that, in comparison to FeFinFET, the device has demonstrated enhanced performance against SCEs and can be further scaled down [13].

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Till now, mainly the device performance has been investigated for various novel device architectures and engineering of FeFinFET to enhance the performance, but to ensure the device reliability and applicability over dynamic environments, the temperature affectability as well as impact of ITCs needs to be analyzed. Moreover, it has been reported that the reliability of the device is more prominent problem due to limited adaptability of the devices in environmental variations [14,15].

The interface between oxide and semiconductor layers, which is central to FeFinFETs, is where the dynamics of ITCs have a significant impact on the functioning of the device. Careful investigation is necessary due to the complexity posed by ITCs at the semiconductor-oxide (S/O) interface in FeFinFETs. The dynamics of these trap charges depend on a number of factors, including the operational environment, processing methods, and material composition. They might originate from defects, impurities, radiation, and surface states [16,17]. Understanding the behavior of ITCs is essential for optimizing the performance of VS-FeFinFETs and realizing their full potential for a range of applications, including logic circuits and memory devices.

Also, the on-chip performance of the device is always subject to operating temperatures. The chip's working temperature rises dramatically as a result of the increased number of transistors, which enhanced the heat dissipation [18–20]. Furthermore, because the characteristics of semiconductors are temperature-dependent, it is necessary to examine the impact of temperature to ensure the stability of the device at various operating temperatures [21]. Therefore, understanding and mitigating the combined effects of temperature and interfacial trap charges on the device performance is not only crucial for current applications but also paves the way for the development of next-generation semiconductor devices that are more resilient, efficient, and adaptable towards dynamic environments.

To mitigate the effects of ITCs, a hetero dielectric gate engineered Vertically Stacked Ferroelectric based FinFET (HD-VS-FeFinFET), a novel combination of Si/SiGe strained tri-layered channel engineered, heterostructure on insulator FeFinFET has been examined in this work. The use of a heterogeneous gate dielectric has enhanced the device's immunity towards ITCs at varied temperatures. The device's performance is improved for the environmental variations by utilizing a stack of high-k dielectric and a low-k interfacial layer over the semiconductor. This type of gate stack (GS) engineering helps to counteract the effects of trap charges while maintaining the device's electrostatic integrity.

So, the main aim of this paper is to investigate the reliability of HD-VS-FeFinFET with extensive analysis from device to circuit level subjective to the impact of operating temperature and its affectability on the influence of ITCs. This is done by analyzing the influence of positive ITCs and negative ITCs on various static and analog performance parameters of HD-VS-FeFinFET compared to VS-FeFinFET at different operating temperatures. This gives the insights about how the various figures of merit of both the devices will be affected due to combined effect of temperature and ITCs. Further, the reliability of the both devices with fair comparison is also explored in terms of variation in several device characteristics at different densities along with different polarities of ITCs. Later, the work is extended to discuss the reliability at the circuit level by analyzing the performance of HD-VS-FeFinFET based CMOS inverter under the influence of ITCs at various operating temperatures and examined its capability to work under varying environmental conditions. Thus, the paper bridges both device-level physics and circuit-level implications, providing a holistic view of reliability across operational scenarios. The rest of the work is organized as Section 2 includes all the specifications regarding the device structure and fabrication feasibility of HD-VS-FeFinFET. Section 3 explains the simulation framework and physical models used in the study. Section 4 provides the results and discussion on the intricacies associated with ITCs and Section 5 concludes the paper.

2. Device structure and fabrication feasibility

Fig. 1(a) depicts the three-dimensional structure of HD-VS-FeFinFET, while Fig. 1(b) shows the device's vertical 2-dimensional view chopped through its fin. Further, Fig. 1(c) displays fabrication feasibility of the HD-VS-FeFinFET using a step-by-step fabrication process flowchart [22,23]. The gate length considered for the device is fixed at 20 nm where silicon-doped hafnium oxide (HfO_2FE) is used as the ferroelectric material with thickness fixed at 6 nm with total gate oxide thickness of 1 nm. The total gate oxide (t_{ox}) is composed of a heterogeneous dielectric stack consisting of equal proportion of Al_2O_3 (t_{ox1}) and HfO_2 (t_{ox2}), each with a thickness of 0.5 nm. The height and width of the fin are taken as 30 nm and 8 nm respectively. A tri-layered strained-silicon channel system is formed with the help of SiGe sandwiched between two silicon layers as Si-$Si_{0.7}$ $Ge_{0.3}$-Si (where $Si_{0.7}Ge_{0.3}$ represents that the mole fraction of Si and Ge is taken as 0.7 and 0.3 respectively). The doping concentration of source/drain is fixed as 1×10^{20} cm^{-3} with n-type and that of channel is 1×10^{16} cm^{-3} with p-type with uniform profile. The length of the source/drain regions is fixed at 20 nm. In addition, a metal gate with a work function of 4.65 eV, which has excellent thermal stability and is compatible with CMOS processing, is utilized in this device to prevent any poly-depletion effect that is common in polysilicon gates [24]. Further, to exploit the advantages of SOI technology such as improved subthreshold characteristics, suppressed threshold voltage (V_{th}) variations, and minimum parasitic capacitances in the considered structure, the entire heterostructure FeFinFET is built on an insulator SiO_2 box whose width, height, and length are kept 32 nm, 5 nm, and 62 nm respectively. To unveil the intricacies of ITCs on the device reliability and performance, ITCs with different polarity have been introduced at the S/O interface with trap charge density to be fixed at 1×10^{12} cm^{-2} based on formerly reported literature [25–28] in Sections 4.1 and 4.3. Further three different ITCs densities are considered with positive and negative polarities as N_{it1}, N_{it2}, and N_{it3} equals to 1×10^{11} cm^{-2}, 1×10^{12} cm^{-2} and 1×10^{13} cm^{-2} respectively to analyze their impact on both the devices in Section 4.2 (see Table 1).

3. Simulation framework and physical models

All the simulations have been carried out using Cogenda's Genius 3D TCAD simulator. The simulation setup includes the drift–diffusion model level 1 (DDML1) which maintains the lattice temperature constant throughout the solving procedure, coupled with consistent Poisson's equation as given by Eq. (1) [29], and continuity equations to govern the carrier transport phenomena for the electrons and the holes as given by Eqs. (2) and (3) respectively [29],

$$\nabla.\epsilon\nabla\psi = -q(p - n + N_D{}^{+} - N_A{}^{-}) \tag{1}$$

$$\frac{\partial n}{\partial t} = \nabla.(\mu_n n\vec{E}_n + \mu_n \frac{k_b T}{q}\nabla n) - (U - G) \tag{2}$$

$$\frac{\partial p}{\partial t} = -\nabla.(\mu_p p\vec{E}_p + \mu_p \frac{k_b T}{q}\nabla p) - (U - G) \tag{3}$$

where ψ is the electrostatic potential of the vacuum level, ϵ is the permittivity of material, $N_D{}^{+}$ and $N_A{}^{-}$ are the ionized impurity concentrations, n and p are the concentration for electron and hole respectively, q is the electric charge, μ_n and μ_p are mobilities of electrons and holes, E_n and E_p are the effective driving electrical field for electrons and holes, U and G are the recombination and generation rates considered for both electrons and holes.

The temperature and doping-dependent recombination-generation phenomenon for carriers are accurately captured by Shockley-Read-Hall (SRH) recombination and Auger models [13]. Further, Philips mobility model for SiGe and Lombardi mobility model for silicon are used to consider the mobility degradation at the semiconductor-oxide interface [30,31]. Lucent model is used to take into account the high-field mobility effects along with hot carrier models for capturing the

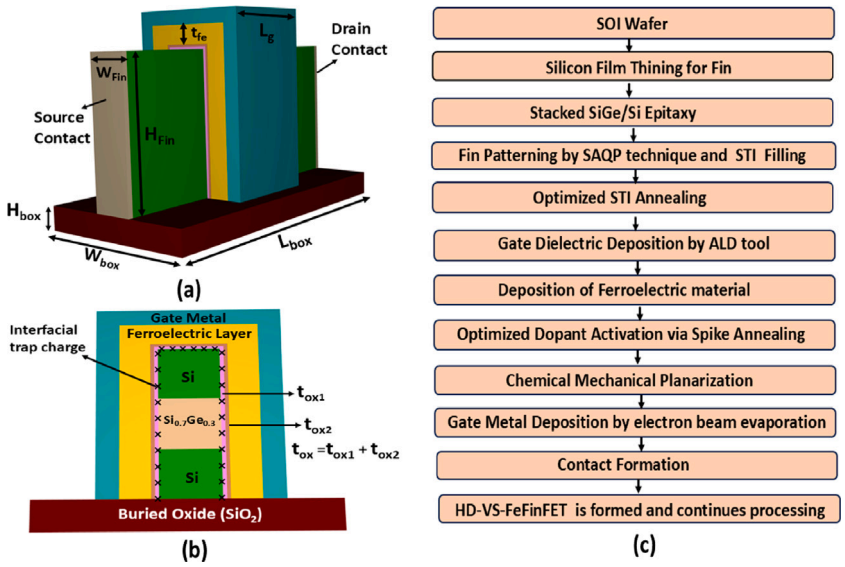

Fig. 1. (a) 3D schematic view of HD-VS-FeFinFET (b) inset of vertical cross-sectional view of HD-VS-FeFinFET (c) Fabrication process flowchart for HD-VS-FeFinFET.

Table 1
Device parameters.

Parameters	Dimension
Gate length (L_g)	20 nm
Drain/Source ($L_{d/s}$)	20 nm
Channel material	Si-$Si_{0.7}Ge_{0.3}$-Si
Oxide thickness (t_{ox})	1 nm
Ferroelectric thickness (t_{fe})	6 nm
Background dielectric constant of Ferroelectric layer	27
Landau coefficient (α)	-1.23×10^{11} cm/F
Landau coefficient (β)	3.28×10^{20} cm^5/FC^2
Landau coefficient (γ)	0.0 cm^9/FC^4
Dipole interaction coefficient (g)	1×10^{-4} cm^3/F
Viscosity coefficient (ρ)	2.25×10^4 Ω cm
Width of fin (W_{Fin})	8 nm
Height of fin (H_{Fin})	30 nm
Height of box (H_{box})	5 nm
Width of box (W_{box})	32 nm
Length of box (L_{box})	62 nm
Interfacial trap charge density	1×10^{11} (cm^{-2}) to 1×10^{13} (cm^{-2})
Doping concentration of drain/source ($N_{d/s}$)	1×10^{20} (cm^{-3})
Doping concentration of channel (N_{ch})	1×10^{16} (cm^{-3})
Gate work function (ϕ)	4.65 eV

effect of hot carriers. To check the velocity saturation and mobility of carriers, the velocity saturation model along with Esurface models are activated. The density gradient method is also used to incorporate quantum confinement phenomena along with the Fermi–Dirac carrier statistics model [29]. The physics of ferroelectric (FE) layer is modeled with the time-dependent Landau–Khalatnikov (LK) equation for relating electric field used for the FE layer as a function of polarization (P), which is given by equation (4) [26],

$$E_{FE} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\left(\frac{\partial P}{\partial t}\right) \quad (4)$$

where α, β, and γ are the static Landau FE material-dependent coefficients taken as -1.23×10^{11} cm/F, 3.28×10^{20} cm^5/FC^2, 0.0 cm^9/FC^4 while g as dipole interaction coefficient and ρ as viscosity coefficient are taken as 1×10^{-4} cm^3/F and 2.25×10^4 Ωcm respectively, from the tool manual [29].

Further, the position and polarity of ITCs in the device are mentioned using the INTERFACE statement along with Trap models to capture the associated phenomena [25,29]. A few abbreviations are used in this paper such as PITC — positive (donor) interfacial trap charge, NITC — negative (acceptor) interfacial trap charge, WITC — without (neutral) interfacial trap charge. The paper is focused on studying the combined effect of temperature, ITCs polarity and density at the S/O interface of HD-VS-FeFinFET and VS-FeinFET to see which one is more immune and reliable to ITCs, both at the device and circuit level.

4. Result and discussion

4.1. Impact of ITCs and temperature affectability

This subsection discusses the temperature affectability on both the devices under the influence of ITCs to analyze the reliability through various static and analog metrics. Characteristics of CMOS devices changes with change in temperature. Fig. 2(a) and (b) shows the transfer characteristics of both the devices (HD-VS-FeFinFET and VS-FeFinFET) at various operating temperatures. As temperature increases, the carrier mobility decreases as given by equation (5) [16,32],

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-n} \quad (5)$$

where $\mu(T_0)$ is carrier mobility at room temperature, $\mu(T)$ is carrier mobility at temperature T, n is the mobility temperature exponent, T_0 is room temperature.

It can be observed from Fig. 2(a) and (b) respectively that HD-VS-FeFinFET showcases more driving current (I_{on}) and less leakage current

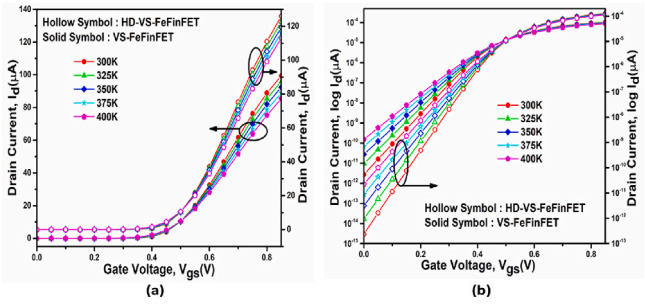

Fig. 2. Impact of temperature on transfer characteristics of HD-VS-FeFinFET and VS-FeFinFET in (a) linear and (b) log scale.

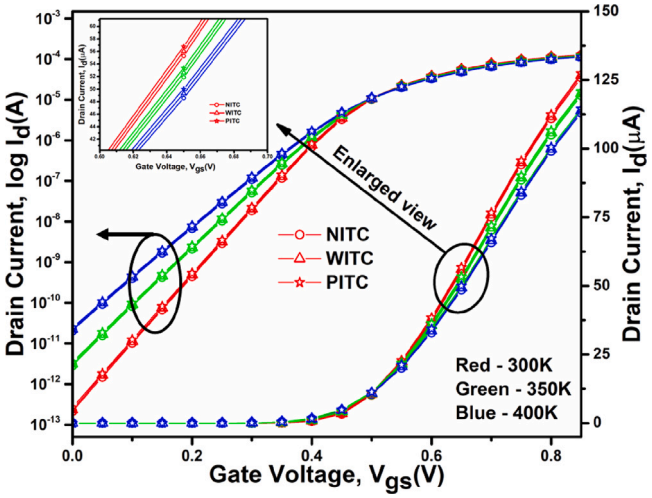

Fig. 3. Impact of ITCs on transfer characteristics of HD-VS-FeFinFET under different operating temperatures.

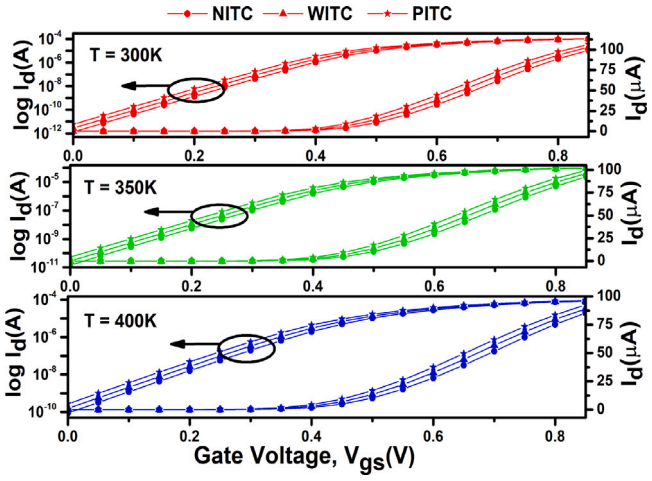

Fig. 4. Impact of ITCs on transfer characteristics of VS-FeFinFET under different operating temperatures.

(I_{off}) at various operating temperatures in comparison to VS-FeFinFET. Also both I_{on} and I_{off} are degrading with increasing temperature for both the devices due to decreasing mobility as related by Eq. (5).

Further, the presence of ITCs leads to altercation in flat band voltage (V_{fb}) as given by equation (6) [33], where q is the electronic charge, N_{it} is the ITCs density and C_{ox} is gate oxide capacitance.

$$V_{\mathrm{fb}} = \frac{qN_{\mathrm{it}}}{C_{\mathrm{ox}}} \tag{6}$$

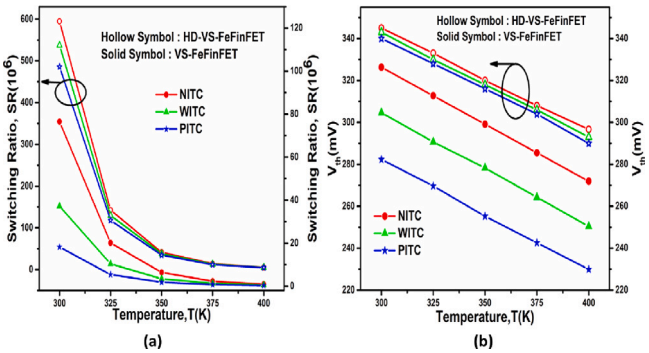

Fig. 5. Variation in (a) Switching ratio and (b) threshold voltage of both the devices under the influence of ITCs at different operating temperatures.

The changes in V_{fb} caused by PITC/NITC leads to modification in threshold voltage (V_{th}) as related by Eq. (7) [34], where x_t is maximum space charge width and ψ_{fp} is built in potential.

$$V_{\mathrm{th}} = V_{\mathrm{fb}} + \psi_{\mathrm{fp}} + \frac{qN_{\mathrm{a}}x_{\mathrm{t}}}{C_{\mathrm{ox}}} \tag{7}$$

This modification in V_{th} leads to change in device characteristics thus change the ON current (I_{on}) and leakage current (I_{off}) of the device [34].

Figs. 3 and 4 respectively shows the impact of ITCs with different polarity on HD-VS-FeFinFET and VS-FeFinFET at different operating temperatures in linear and log scale. It is inferred from Fig. 3 that the transfer performance of the device is minimally gets affected due to PITC and NITC with respect to WITC. The variation in I_{on} is 0.588% rise(0.615% fall) with increase (decrease) in leakage current by 11.2%(10.1%) in presence of PITC(NITC) at 300 K. With the rise in temperature to 400 K, there is only 0.628% rise(0.652% fall) in I_{on} along with increment(decrement) in leakage current by 8.47%(7.8%) under the influence of PITC (NITC).

So the tolerance in the HD-VS-FeFinFET towards different ITCs is almost consistent with variation in temperature from 300 K to 400 K in contrast to VS-FeFinFET which displays large variations with rise(fall) in I_{on} by 3.35%(3.64%) along with increase(decrease) in leakage current by 111%(53.1%) at 300 K and rise(fall) of 3.88%(4.22%) in I_{on} along with increment(decrement) of 75.2%(43.5%) at 400 K in presence of PITC(NITC) as showcased in Fig. 4, thus confirms HD-VS-FeFinFET to be more reliable in presence of ITCs even with increasing temperature.

Fig. 5(a) and (b) respectively displays the variation of switching ratio (SR) and threshold voltage (V_{th}) of both the devices under the influence of ITCs of different polarities at various range of temperature. Fig. 5(a) shows that HD-VS-FeFinFET exhibits higher SR with minimal deviations under the influence of ITCs in comparison to VS-FeFinFET. It also showcases that although there is decrease in SR with rise in temperature from 300 K to 400 K for both the devices but the variations due to ITCs also gets suppressed with increasing temperature thus favoring the switching performance of the device. Further the enhanced(reduced) effective gate voltage i.e. (V_{gs}-V_{fb}) due to presence of PITC(NITC) results in decrease(increase) in V_{th} of both the devices under consideration. Also the V_{th} is inversely proportional to temperature that led to its decrement by 14.57%(17.8%) for HD-VS-FeFinFET(VS-FeFinFET) with increase in temperature from 300 K to 400 K as displayed in Fig. 5(b).

Figs. 6 and 7 respectively shows the variation of transconductance (g_m) and device efficiency, also known as Transconductance Generation Factor (TGF) of HD-VS-FeFinFET and VS-FeFinFET for different ITCs polarity at various operating temperatures. These are the important parameters in the design of analog circuits and Fig. 6 shows that at high

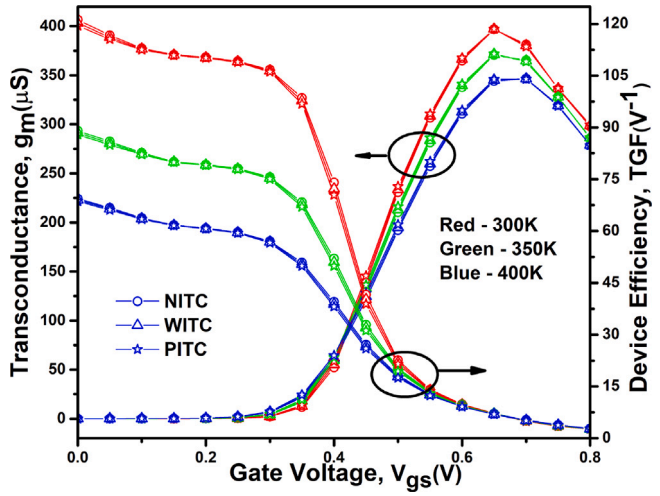

Fig. 6. Impact of ITCs on transconductance and device efficiency of HD-VS-FeFinFET under different operating temperatures.

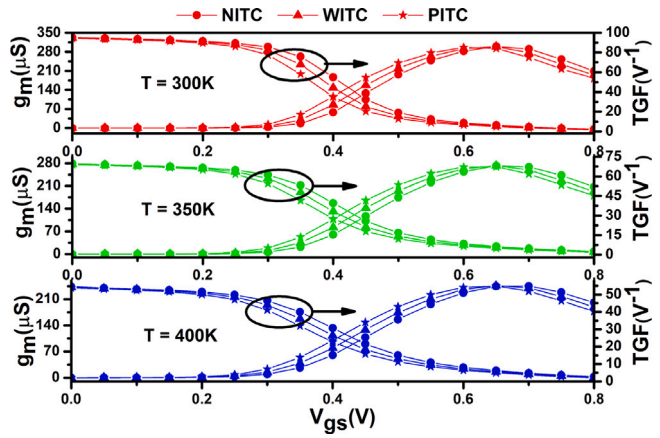

Fig. 7. Influence of ITCs on transconductance and device efficiency of VS-FeFinFET under different operating temperatures.

gate bias, g_m increases with decrease in temperature and an opposite behavior is observed at low gate bias. While analyzing the impact of temperature on TGF, it is found that at higher gate bias, temperature has negligible impact on TGF as compare to large variation at lower gate bias. As it is clearly visible from Fig. 6 that HD-VS-FeFinFET showcase higher g_m and TGF along with negligible variations due to ITCS at all temperature ranges in contrast to visible increase(decrease) caused by NITC(PITC) in VS-FeFinFET as depicted in Fig. 7.

Fig. 8 shows the variation of quality factor (QF) of both the devices with variation in temperature in presence of ITCs of different polarities. Dependence of QF on temperature is a critical consideration in the design and application of FETs in electronic circuits. It is inferred from the figure that there is reduction in QF by 33.16% and 38.1% for HD-VS-FeFinFET and VS-FeFinFET respectively due to reduced transconductance and enhanced SS at elevated temperature. Moreover the figure also confirms that presence of ITCs negligibly affects the quality factor of both the devices.

Fig. 9 illustrates the variation of output characteristics with drain voltage (V_{ds}) for both the devices at various operating temperatures at fixed negative trap charge density. The drain current increases with increase in temperature and it is analyzed that, at V_{ds} = 0.7 V, with a rise in temperature from 300 K to 400 K, the drain current increases

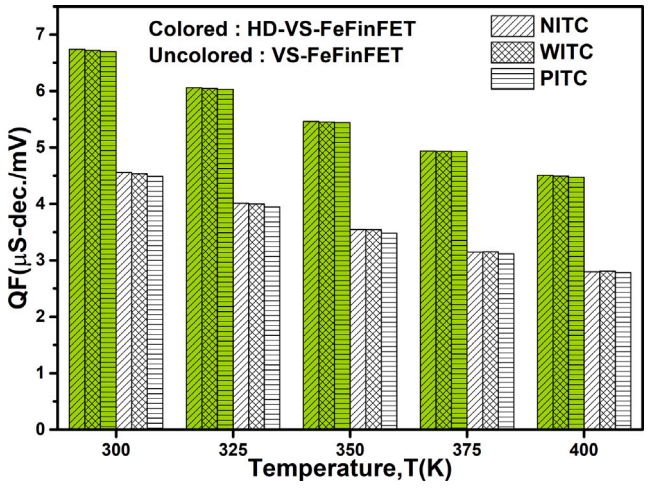

Fig. 8. Variation in Quality factor of both the devices under the influence of ITCs at different operating temperatures.

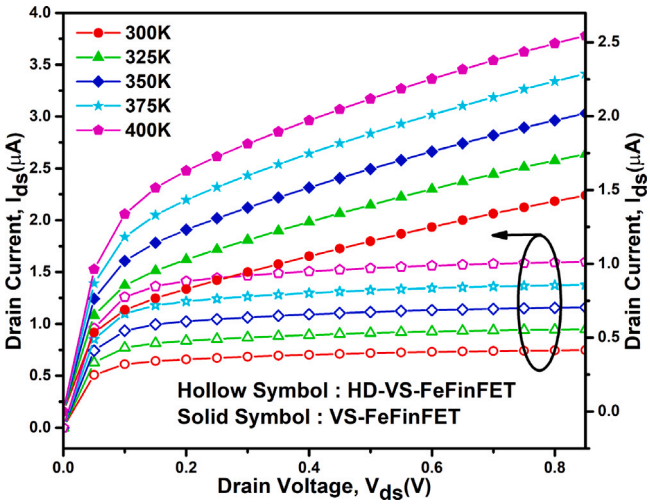

Fig. 9. Impact of temperature on output characteristics of HD-VS-FeFinFET and VS-FeFinFET.

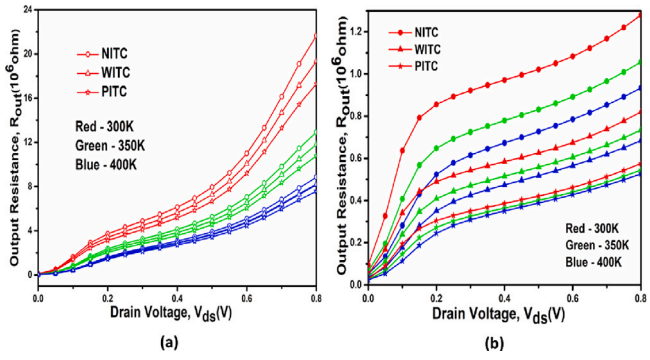

Fig. 10. Variation in output resistance of (a) HD-VS-FeFinFET and (b) VS-FeFinFET under the influence of ITCs at different operating temperatures.

by 2.14 times and 1.77 times for HD-VS-FeFinFET and VS-FeFinFET respectively.

Further, Fig. 10(a) and (b) displays the influence of ITCs of different polarities on the output resistance R_{out} of both the devices at different temperatures. Higher R_{out} ensures better signal fidelity by suppressing

Table 2
Summary of different static and analog parameters for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs at 300 K.

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	1.06×10^{-4}	1.03×10^{-4}	9.92×10^{-4}	1.27×10^{-4}	1.26×10^{-4}	1.26×10^{-4}
I_{off} (A)	5.83×10^{-12}	2.77×10^{-12}	1.30×10^{-12}	2.62×10^{-13}	2.36×10^{-13}	2.12×10^{-13}
I_{on}/I_{off}	$1.83 \times 10^{+7}$	$3.72 \times 10^{+7}$	$7.65 \times 10^{+7}$	$4.86 \times 10^{+8}$	$5.38 \times 10^{+8}$	$5.95 \times 10^{+8}$
V_{th} (V)	0.282	0.30	0.32	0.340	0.343	0.345
QF (uS-dec/mV)	4.49	4.53	4.56	6.70	6.60	6.74
g_m (S)	2.96×10^{-4}	2.99×10^{-4}	3.0×10^{-4}	3.97×10^{-4}	3.97×10^{-4}	3.97×10^{-4}
TGF (V^{-1})	94.42	94.75	95.10	119.43	120.29	121.21
R_{out} (ohm)	$5.74 \times 10^{+5}$	$8.19 \times 10^{+5}$	$1.28 \times 10^{+6}$	$1.73 \times 10^{+7}$	$1.93 \times 10^{+7}$	$2.17 \times 10^{+7}$

Table 3
Summary of different static and analog parameters for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs at 350 K.

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	9.95×10^{-5}	9.61×10^{-5}	9.23×10^{-5}	1.21×10^{-4}	1.20×10^{-4}	1.19×10^{-4}
I_{off} (A)	5.24×10^{-11}	2.76×10^{-11}	1.44×10^{-11}	3.46×10^{-12}	3.15×10^{-12}	2.87×10^{-12}
I_{on}/I_{off}	$1.90 \times 10^{+6}$	$3.47 \times 10^{+6}$	$6.40 \times 10^{+6}$	$3.49 \times 10^{+7}$	$3.81 \times 10^{+7}$	$4.16 \times 10^{+7}$
V_{th} (V)	0.25	0.27	0.29	0.31	0.32	0.32
QF (uS-dec/mV)	3.48	3.54	3.55	5.44	5.45	5.46
g_m (S)	2.69×10^{-4}	2.73×10^{-4}	2.72×10^{-4}	3.72×10^{-4}	3.71×10^{-4}	3.71×10^{-4}
TGF (V^{-1})	69	69.32	69.76	87.91	88.47	89.03
R_{out} (ohm)	$5.44 \times 10^{+5}$	$7.33 \times 10^{+5}$	$1.06 \times 10^{+6}$	$1.08 \times 10^{+7}$	$1.18 \times 10^{+7}$	$1.29 \times 10^{+7}$

Table 4
Summary of different static and analog parameters for HD-VS-FeFinFET and VS-FeFinFET under the influence of ITCs at 400 K.

Parameter	VS-FeFinFET			HD-VS-FeFinFET		
	PITC	WITC	NITC	PITC	WITC	NITC
I_{on} (A)	9.25×10^{-5}	8.91×10^{-5}	8.53×10^{-5}	1.14×10^{-4}	1.14×10^{-4}	1.13×10^{-4}
I_{off} (A)	2.70×10^{-10}	1.54×10^{-10}	8.71×10^{-11}	2.43×10^{-11}	2.24×10^{-11}	2.07×10^{-11}
I_{on}/I_{off}	$3.42 \times 10^{+5}$	$5.77\ 10^{+5}$	$9.79 \times 10^{+5}$	$4.70 \times 10^{+6}$	$5.07 \times 10^{+6}$	$5.46 \times 10^{+6}$
V_{th} (V)	0.22	0.25	0.27	0.29	0.29	0.29
QF (uS-dec/mV)	2.78	2.81	2.80	4.47	4.49	4.51
g_m (S)	2.42×10^{-4}	2.47×10^{-4}	2.45×10^{-4}	3.46×10^{-4}	3.45×10^{-4}	3.44×10^{-4}
TGF (V^{-1})	53.79	54.14	54.63	68.63	68.99	69.35
R_{out} (ohm)	$5.25 \times 10^{+5}$	$6.83 \times 10^{+5}$	$9.33 \times 10^{+5}$	$7.58 \times 10^{+6}$	$8.18 \times 10^{+6}$	$8.85 \times 10^{+6}$

Table 5
Summary of different performance parameters for VS-FeFinFET under the influence of ITCs with different density and different polarity.

Parameter	N_{it3}	N_{it2}	N_{it1}	WITC	$-N_{it1}$	$-N_{it2}$	$-N_{it3}$
I_{on} (A)	1.25×10^{-4}	1.06×10^{-4}	1.03×10^{-4}	1.03×10^{-4}	1.03×10^{-4}	9.92×10^{-5}	6.31×10^{-5}
I_{off} (A)	1.53×10^{-9}	5.83×10^{-12}	2.93×10^{-12}	2.77×10^{-12}	2.58×10^{-12}	1.30×10^{-12}	4.51×10^{-15}
I_{on}/I_{off}	$8.18 \times 10^{+4}$	$1.83\ 10^{+7}$	$3.53 \times 10^{+7}$	$3.72 \times 10^{+7}$	$3.98 \times 10^{+7}$	$7.63 \times 10^{+7}$	$1.40 \times 10^{+10}$
V_{th} (V)	0.122	0.283	0.303	0.304	0.306	0.326	0.477

Table 6
Summary of different performance parameters for HD-VS-FeFinFET under the influence of ITCs with different density and different polarity.

Parameter	N_{it3}	N_{it2}	N_{it1}	WITC	$-N_{it1}$	$-N_{it2}$	$-N_{it3}$
I_{on} (A)	1.32×10^{-4}	1.27×10^{-4}	1.27×10^{-4}	1.27×10^{-4}	1.27×10^{-4}	1.26×10^{-4}	1.20×10^{-4}
I_{off} (A)	6.09×10^{-13}	2.62×10^{-13}	2.37×10^{-13}	2.36×10^{-13}	2.33×10^{-13}	2.12×10^{-13}	1.02×10^{-13}
I_{on}/I_{off}	$2.17 \times 10^{+8}$	$4.86 \times 10^{+8}$	$5.35 \times 10^{+8}$	$5.38 \times 10^{+8}$	$5.43 \times 10^{+8}$	$5.94 \times 10^{+8}$	$1.17 \times 10^{+9}$
V_{th} (V)	0.320	0.340	0.342	0.343	0.343	0.345	0.361

voltage variations for changes in load resistance as shown by HD-VS-FeFinFET at all the considered temperatures along with behavior of negative temperature coefficient of resistance exhibited by both the devices. High-k dielectric materials help in minimizing the average variation in R_{out} caused by ITCs (i.e. 11.3%) due to their ability to lower interface trap density and provide stronger electrostatic control over the channel in comparison to VS-FeFinFET, that showcases wide variation of 43%. Further with rise in temperature, this average variation induced due to ITCs reduces to 7.78% and 29.8% for HD-VS-FeFinFET and VS-FeFinFET respectively, showing their improved immunity (see Tables 2–4).

4.2. Impact of ITCs with variation in density and polarity

In this section, the effect of variation in ITCs density and polarity on both the devices is investigated at constant temperature of 300 K. Fig. 11 shows the impact of ITCs density of different polarity on the transfer characteristics of VS-FeFinFET.

It is clearly visible from the figure that with an increase in PITC (NITC) density, I_{on} increases (decreases) with respect to the case of WITC. This increase(decrease) in I_{on} is attributed to the decrease (increase) in the flatband voltage (V_{fb}) caused by the PITC(NITC), as defined by Eq. (6).

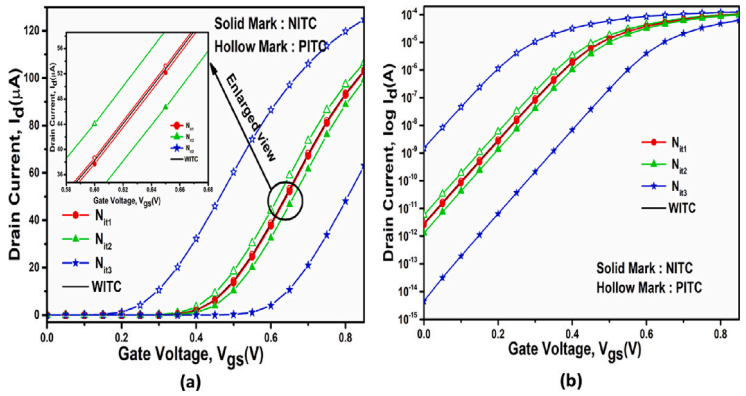

Fig. 11. Impact of ITC's density and polarity on transfer characteristics of VS-FeFinFET in (a) linear and (b) log scale.

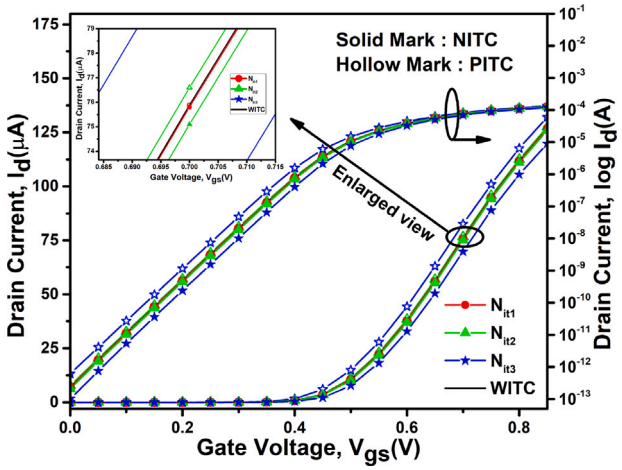

Fig. 12. Effect of ITC's density and polarity on transfer characteristics of HD-VS-FeFinFET.

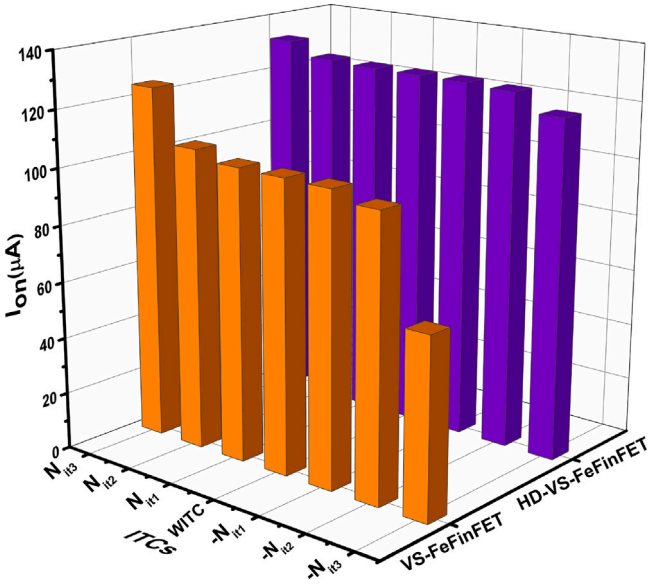

Fig. 13. Effect of ITC's density and polarity on the ON current of HD-VS-FeFinFET and VS-FeFinFET.

Moreover, PITC(NITC) decreases (increases) the V_{fb}, thereby, increases(decreases) the effective gate bias ($V_{eff} = V_{gs}$-V_{fb}) in proportionality to N_{it}, as evident by the increase(decrease) in I_{on} with increase in density for PITC(NITC) to N_{it1}, N_{it2}, and N_{it3} as depicted in Fig. 11(a). The degradation posed by the PITC is as hazardous for the device operated at low gate bias as at the high gate bias as shown in the figure. Furthermore, it is analyzed that with an increase in density for PITC to N_{it1}, N_{it2}, and N_{it3}, I_{off} degrades significantly by around 1.06 times, 2.11 times, and 552 times respectively with respect to WITC as displayed in Fig. 11(b).

Owing to the implementation of heterogeneous gate dielectric engineering in HD-VS-FeFinFET which not only helps in minimizing the variation caused by ITCs in device's characteristics due to their ability to lower interface trap density, but also provide stronger electrostatic control over the flow of carriers. The improvement in the performance of the device is clearly visible in Fig. 12, with negligible degradation in leakage current with increasing trap density such that with an increase in PITC's density to N_{it1}, N_{it2}, and N_{it3}, I_{off} degrades minimally by around 1.01 times, 1.11 times, and 2.58 times respectively with respect to WITC, thus confirming HD-VS-FeFinFET to be more immune and reliable towards ITCs in comparison to VS-FeFinFET.

The presence of PITC(NITC) decreases(increases) the V_{fb}, thereby, modify the effective gate bias in proportionality to N_{it}, as evident by the increase(decrease) in I_{on} by 0.26% (0.32%), 3.35%(3.69%) and 21.3%(38.7%) for VS-FeFinFET with increase in PITC(NITC) density to N_{it1}, N_{it2}, and N_{it3} respectively. However the increase(decrease) in I_{on} for HD-VS-FeFinFET is negligibly very less that is only by 0.04%(0.05%), 0.58%(0.61%) and 4.3%(5.45%) with increase in PITC (NITC) density to N_{it1}, N_{it2}, and N_{it3} respectively as shown in Fig. 13, thereby confirming its improved reliability.

The impact of ITC density and polarity on V_{th} for both the devices is presented in Fig. 14. It is obtained that the presence of PITC(NITC) decreases(increases) V_{th}. The reduced(enhanced) V_{th} for PITC(NITC) is the result of the increased(decreased) band bending caused by PITC(NITC) [35]. V_{th} reduces(enhances) by 59.69%(56.65%) at N_{it3}. This increase in trap charge density also cause variation in HD-VS-FeFinFET with decrease(increase) by 6.56%(5.46%) but that is very minimal in comparison to VS-FeFinFET thus making it more immune to any ITCs associated distortions in the performance (see Tables 5–6).

4.3. Impact of ITCs and temperature affectability: Circuit level analysis

Increasing density of transistors per unit area of chip with advancing technologies results into huge amount of heat dissipation, which seriously affects the transistor's performance and causes variations in device's parameters such as threshold voltage (V_{tn}, V_{tp}) and carrier mobility (μ_n, μ_p) [36].

The switching threshold voltage (V_{TH}) of a CMOS inverter can be explained by the well known Eqs. (8), (9), and (10) [37], as given

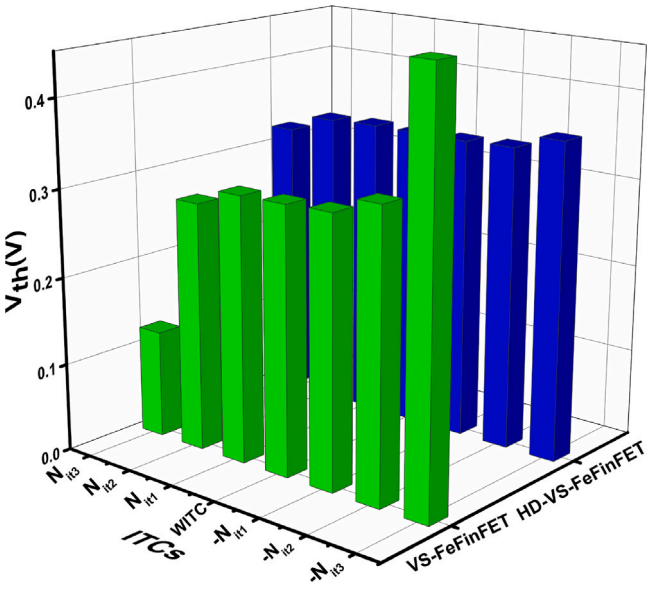

Fig. 14. Effect of ITC's density and polarity on threshold voltage of HD-VS-FeFinFET and VS-FeFinFET.

below,

$$V_{TH} = \frac{V_{dd} - |V_{tp}| + V_{tn}\sqrt{\frac{(W/L)_n \mu_n C_{ox}}{(W/L)_p \mu_p C_{ox}}}}{1 + \sqrt{\frac{(W/L)_n \mu_n C_{ox}}{(W/L)_p \mu_p C_{ox}}}} \quad (8)$$

$$\mu_{(n,p)} = \mu_0 \left(\frac{T_0 + \delta T}{T_0}\right)^{-m} \quad (9)$$

$$V_{t(p,n)} = V_{th0} - k(T_0 + \delta T) \quad (10)$$

where V_{tn} and V_{tp} respectively are the threshold voltages for n-channel and p-channel device, C_{ox} is the oxide capacitance, μ_n and μ_p are the electron and hole mobilities respectively, $(W/L)_n$ and $(W/L)_p$ are the aspect ratio of n-channel and p-channel device respectively, μ_0 is carrier mobility at room temperature, m is the mobility temperature exponent, T_0 is room temperature, dT is the temperature change from T_0, V_{th0} is the threshold voltage at absolute zero temperature, and k is the temperature coefficient of the threshold voltage.

The carrier mobilities and threshold voltages of n-type and p-type configurations are two major metrics which are strongly dependent on operating temperatures, thus the characteristics of inverter are also temperature dependent [37].

Also ITCs can generate additional spurious signals that can have a detrimental effect on the performance of CMOS inverters, influencing parameters like threshold voltage, mobility, leakage current, noise margin, and overall reliability of the circuits [26,38]. These effects are critical in advanced and scaled-down CMOS technologies, thus it is necessary to analyze the impact of ITCs of different polarity on HD-VS-FeFinFET based CMOS inverter at various operating temperatures.

For this, a required setup is designed on Cogenda Visual TCAD simulator with n-channel and p-channel HD-VS-FeFinFET isolated electrically with the help of 60 nm SiO_2 spacer. Fig. 15(a) and (b) respectively shows the 3D simulated structure and schematic of the CMOS inverter circuit where V_{dd}, V_{in}, and V_{out} are the supply voltage, input voltage and output voltage respectively. Initially threshold matching of both the n-channel and p-channel structure is done for HD-VS-FeFinFET based CMOS inverter as displayed in Fig. 16(a) and (b) at different operating temperatures and in presence of different ITCs respectively. The V_{gs} is varied from −0.85 to 0.85 V with dual work function metal

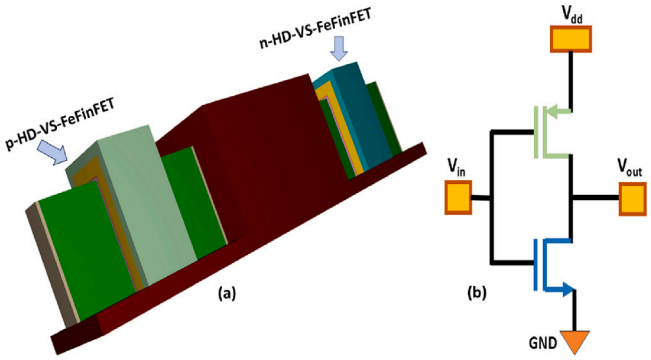

Fig. 15. (a) 3D structure and (b) Schematic diagram of HD-VS-FeFinFET based CMOS inverter.

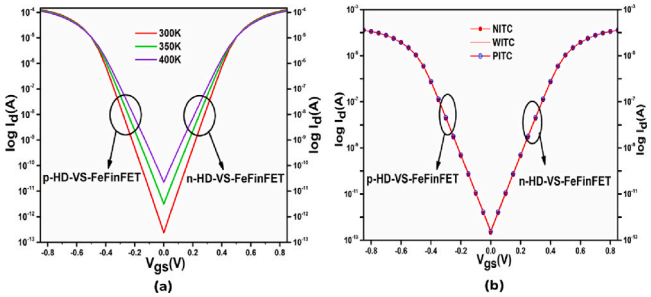

Fig. 16. Influence of (a) temperature and (b) ITCs on Threshold Voltage Matching Curve for HD-VS-FeFinFET based CMOS inverter.

(DWFM) integration scheme.

It is very much required to analyze the crucial FOMs to estimate the performance of the inverter and for this, voltage transfer characteristics (VTC) for HD-VS-FeFinFET based CMOS inverter at various temperatures and under the influence of ITCs with different polarities is analyzed as shown in Figs. 17 and 18 respectively. Simulation results give approximately 34.627 mV shift in the inverter switching threshold voltage (V_{TH}) for a temperature change from 300 K to 400 K . Also as we have very well discussed earlier the improved reliability of HD-VS-FeFinFET under the influence of ITCs in previous sections, this is very well maintained in device based inverter as confirmed from Fig. 18 which displays only negligible average variations of 1.45% for NITC(PITC) in V_{TH} at 300 K and that too decreases to 0.73% with increasing temperature to 400 K.

Further, Noise Margin (NM) is a crucial parameter to depict the noise immunity of the circuit and this value should be high enough for better tolerance to variations and more reliable operation [39]. Modification in threshold voltage of MOSFETs due to variation in temperature can cause the input and output levels to either rise or fall from their ideal state at room temperature, which leads to variation in noise margin. It is found as shown in Table 7 that with increase in temperature to 400 K, noise margin decreases by 6.8%. Also improved immunity of HD-VS-FeFinFET towards ITCs is very well confirmed in its CMOS inverter circuits with negligible variation in noise margin by 1.13%(1.26%) at 300 K, 1.29%(1.48%) at 350 K and 1.39%(1.32%) at 400 K under the influence of NITC(PITC), making it reliable for digital circuits and applications.

Fig. 17 also displays the variation of switching current (I_{sc}) with variation in temperature, which shows the increasing trend of I_{sc} with temperature such that peak I_{sc} increases up to 4.66 times along with rightward shift when temperature increases from 300 K to 400 K. Also Fig. 19 displays the influence of ITCs with different polarity at various operating temperatures. It shows that I_{sc} is little bit higher(lower) for NITC(PITC) before reaching its peak in contrast to trend in I_{sc} for later

Table 7
Performance comparison of HD-VS-FeFinFET based CMOS inverter under the influence of ITCs at various operating temperature.

T (K)	ITCs	V_{IL} (mV)	V_{IH} (mV)	V_{OL} (mV)	V_{OH} (mV)	NM_L (mV)	NM_H (mV)	V_{TH} (mV)	TR (mV)
300	PITC	183.77	267.27	4.33×10^{-7}	800	1.84×10^{2}	532.72	242.13	83.50
	WITC	191.06	273.898	5.51×10^{-7}	800	1.91×10^{2}	526.10	246.92	82.83
	NITC	197.68	279.863	7.04×10^{-7}	800	1.98×10^{2}	520.137	249.315	82.176
350	PITC	201.227	289.095	8.18×10^{-6}	800	2.01×10^{2}	510.905	265.93	87.86
	WITC	207.423	296.586	1.01×10^{-5}	800	2.07×10^{2}	503.414	271.825	89.16
	NITC	213.78	303.096	1.24×10^{-5}	800	2.14×10^{2}	496.904	270.424	89.31
400	PITC	213.38	303.19	7.70×10^{-5}	799.98	2.13×10^{2}	496.78	276.25	89.81
	WITC	220.511	309.674	9.25×10^{-5}	799.99	2.21×10^{2}	490.31	281.55	89.16
	NITC	226.721	316.532	1.11×10^{-4}	799.99	2.27×10^{2}	483.458	280.401	89.811

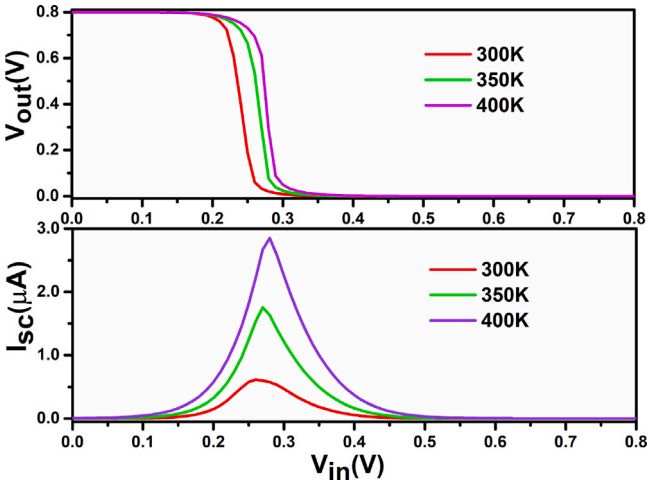

Fig. 17. Impact of temperature on (a) Voltage Transfer Characteristics and (b) Switching Current of HD-VS-FeFinFET based CMOS inverter.

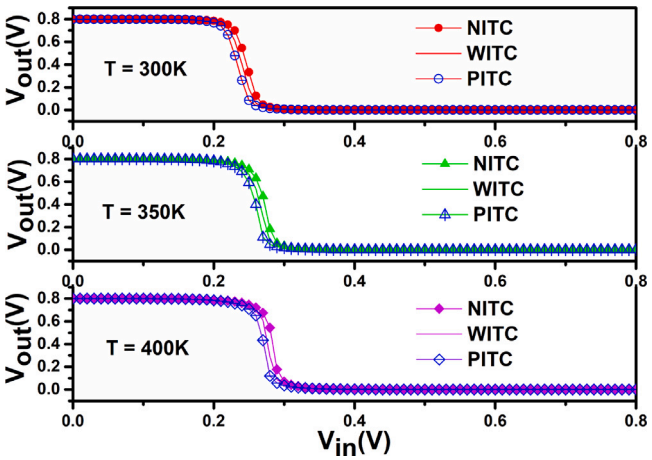

Fig. 18. Impact of ITCs polarity on Voltage Transfer Characteristics of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures.

values of V_{in} due to modifications in effective threshold voltage under the influence of ITCs. Also it confirms the improved reliability of HD-VS-FeFinFET based CMOS inverter with negligible variation in peak value I_{sc} from 0.99%(0.31%) at 300 K to 2.41%(0.81%) at 400 K in presence of NITC(PITC).

Further, Fig. 20(a) and (b) respectively displays the performance comparison of HD-VS-FeFinFET based CMOS inverter for its transition range and voltage gain at various temperatures. It exhibits sharper transition range and higher voltage gain at 300 K due to higher carrier mobility and reduced leakage currents.

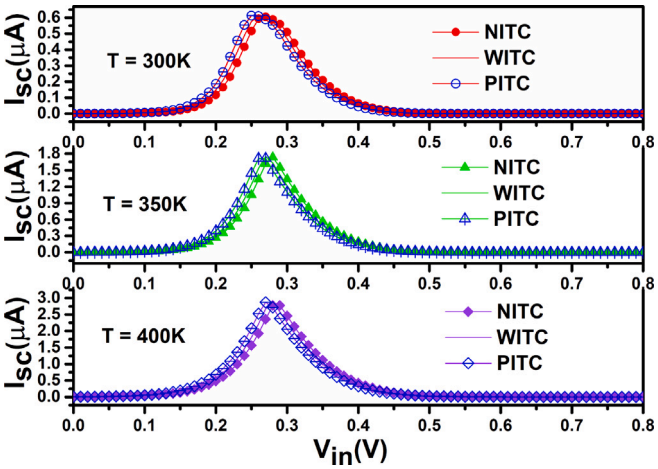

Fig. 19. Impact of ITCs polarity on switching current of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures.

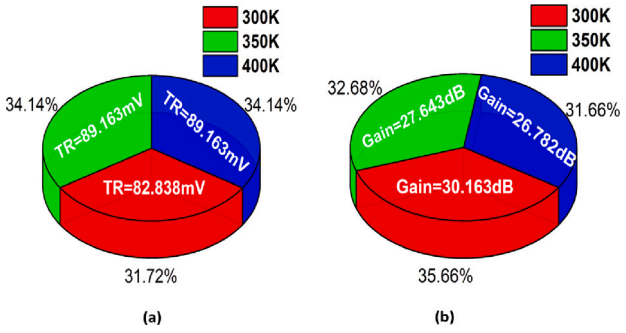

Fig. 20. Comparison chart of (a) transition region (b) voltage gain of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures.

Although dissipation of power was traditionally negligible in CMOS technology, it has become a significant factor in modern, scaled-down technologies due to increased leakage currents [38]. Fig. 21 displays the variation of power dissipation (P_d) in HD-VS-FeFinFET based CMOS inverter at various operating temperatures and under the influence of ITCs with different polarity. It is inferred from the figure that with increase in temperature from 300 K to 400 K, P_d increases up to 366% due to increasing leakage currents. Also the graph shows that NITC(PITC) minimally affects the power performance of the inverter with variations by 0.99%(0.31%) at 300 K to 2.41%(0.81%) at 400 K, thus confirming its reliability especially for applications that operate in variable temperature environments or where power efficiency is critical.

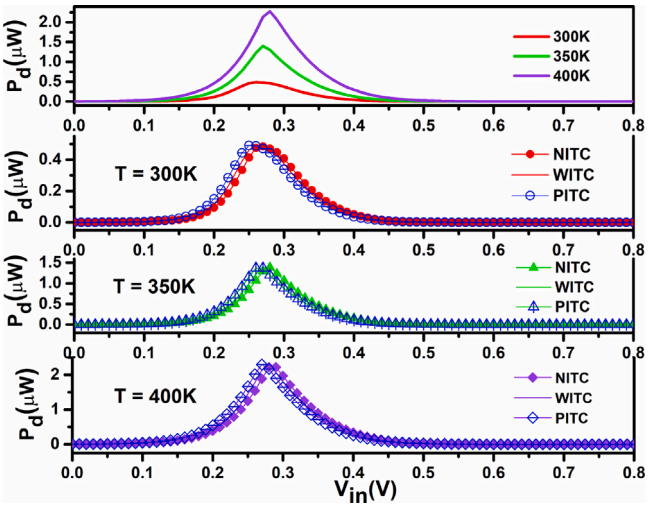

Fig. 21. Impact of ITCs polarity on power dissipation of HD-VS-FeFinFET based CMOS inverter at various opertaing temperatures.

5. Conclusion

Interface trap charges result from dangling bonds created by the abrupt end of the semiconductor surface, hence they are unavoidable. Since trap charges are always present in real devices and are never zero, it is crucial to understand and mitigate their effects for the design of reliable and efficient semiconductor devices, particularly in applications that demand high performance under varying environmental conditions. So, this paper presented a comprehensive analysis from device to circuit level to encompass the reliability of HD-VS-FeFinFET in terms of: (1) temperature affectability on impact of ITCs to understand their effect at various operating temperatures (2) impact of ITCs density with different polarity, over various figure of merits. Results demonstrate that HD-VS-FeFinFET has better immunity against ITCs with minimum variation at all considered operating temperatures in comparison to VS-FeFinFET. Further the study done to analyze the impact of ITCs density and polarity reveals that device performance alters significantly with rising density of ITCs for both PITC(NITC) but this deviation is very much less in HD-VS-FeFinFET with 4.3%(5.45%) in I_{on}, and 6.56% (5.46%) in V_{th} for PITC(NITC) in comparison to 21.3%(38.7%) and 59.69% (56.65%) respectively in VS-FeFinFET. Further, the performance analysis done at circuit level with HD-VS-FeFinFET based CMOS inverter at various operating temperatures confirmed its improved immunity towards ITCs and makes it an ideal choice for advanced logic circuits and low-power electronic applications. Thus, by shedding light on the intricacies of interfacial trap charges and temperature affectability studied with different polarity/density, this work paves the way for the development of HD-VS-FeFinFET as a more reliable, efficient, and adaptable device to the increasingly demanding and dynamic environments of the future.

CRediT authorship contribution statement

Kajal Verma: Conceptualization, Methodology, Software, Analysis, Data curation, Writing – original draft preparation. **Rishu Chaujar:** Conceptualization, Writing – review and editing at different stages, Supervision.

Consent to participate & for publication

Since the concerned research paper is based on the 'non-life science journal'. So, 'Not Applicable' here. However, the authors have gone through all journal policies and consented to the authorities for further processing.

Compliance with ethical standard

The authors have seen all the Ethical Standards and will suppose to follow them in the future

Funding statement

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

No data was used for the research described in the article.

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Investigating DFT and Device-Level Behavior in Doped Ferroelectric HfO_2-Based HD-VS-FeFinFET With Self-Heating and Logic Circuit Perspectives

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***Abstract*— In this work, a comprehensive investigation of ferroelectric hafnium oxide (HfO_2)-based devices is presented, encompassing both material- and device-level analyses. At the device level, the impact of various doped ferroelectric materials on the transfer characteristics of heterodielectric vertically stacked ferroelectric fin field effect transistor (HD-VS-FeFinFET) is studied, highlighting dopant-driven modulation of the performance parameters with enhancement in the drain current (I_{ON}) by 24%, transconductance (g_m) by 29%, and transconductance generation factor (TGF) by 10.8% for silicon-doped HfO_2 over lanthanum-doped HfO_2 as an ferroelectric layer. Subsequently, density functional theory (DFT) simulations are performed to examine the structural and electronic properties of undoped HfO_2 and its doped variants using gadolinium (Gd) and silicon (Si). Furthermore, self-heating effects (SHEs) are critically examined in the HD-VS-FeFinFET structure across varying biasing voltages and ambient temperatures. The analysis reveals influence on transconductance and its leftward peak shifts toward lower V_{gs}, along with lattice temperature contour evolution due to SHE, emphasizing its impact on device reliability. Also, the CMOS inverter with these advanced technologies exhibited stable switching and sharp transitions, showing only a moderate increase in propagation delay (15.88%) and edge rate (12.31%) over a 100 K temperature rise, confirming its stability and reliability under high-temperature operation. Thus, the integrated multiscale analysis provides a holistic understanding of material doping, thermal effects, and circuit performance, establishing a pathway for the optimized design of ferroelectric-based next-generation systems in advanced low-power, high-speed electronic applications.**

***Index Terms*— Density functional theory (DFT), dopants, ferroelectric, fin field effect transistor (FinFET), heterodielectric vertically stacked ferroelectric FinFET (HD-VS-FeFinFET), inverter, self-heating effect (SHE), Si/SiGe.**

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I. Introduction

THE growing demand for energy-efficient, compact, and high-performance electronic devices is mainly driven by progressions in areas such as logic-in-memory (LiM) architectures, cloud computing, mobile smart technologies, and the Internet of Things (IoT) [1], [2]. To address this demand, transistors are being continuously scaled down. However, as these devices reach their physical and operational limits, issues like short channel effects (SCEs) begin to occur [3]. To address these scaling-induced challenges, device architectures such as dual-gate FETs, trenched gates, trigate fin field effect transistors (FinFETs), recessed channel designs, ferroelectric field-effect transistors (FeFETs), and so on have shown their credibility in extending CMOS scalability. Among these, ferroelectric FinFETs (FeFinFETs) are emerging as potential candidates for next-generation CMOS technology, due to their superior control over SCEs and improved switching performance [4], [5], [6].

To further minimize parasitic effects in the device and enhance gate control over the channel, silicon-on-insulator (SOI) technology is integrated into FeFinFET designs, resulting in the SOI-based FeFinFET configuration. While silicon remains the primary semiconductor material for its use as channel material in transistors, its inherent limitations have encouraged the exploration of alternative materials such as group III–V compounds, SiGe alloys, and other compound semiconductors to further enhance device capabilities [7], [8]

In addition to channel material innovations, employing heterodielectric gate stacks comprising ferroelectric hafnium oxide (HfO_2) combined with interfacial oxides like SiO_2 or Al_2O_3 allows precise engineering of the gate dielectric properties, enabling a balance between ferroelectric functionality and minimized gate leakage [9].

In aggressively scaled devices, traditional perovskite-based ferroelectric materials are unsuitable due to their relatively large physical thickness, incompatibility with standard CMOS fabrication processes, and associated environmental concerns. To overcome these limitations, doped HfO_2 thin films are adopted as the ferroelectric layer, offering better integration with existing semiconductor manufacturing techniques [10].

In this work, a detailed study has been carried out by varying the Landau coefficients to capture the ferroelectric behavior of different doped HfO_2-based ferroelectric materials [11], [12]. This investigation provides a critical groundwork for optimizing dopant selection to augment FeFinFET performance.

Thereafter, this work presents a systematic density functional theory (DFT) study of the atomic and electronic properties of HfO_2 as a ferroelectric candidate layer in FET devices. We investigate the pristine (undoped) HfO_2 structure as well as HfO_2 doped with gadolinium (Gd) and silicon (Si) atoms to understand the impact of doping on its atomic and electronic behavior. The comparative analysis of these parameters enables us to assess how doping modifies the electronic properties of HfO_2, which is critical for optimizing its performance in next-generation FeFET devices.

In addition, the present study also addresses the critical impact of self-heating effects (SHEs), particularly in the context of Si-doped HfO_2-based FeFinFETs. As device scaling advances, SHE has become a major reliability concern due to restricted thermal dissipation pathways in nanoscale 3-D structures like FinFETs [13], [14].

Recognizing the significance of this issue, a detailed electrothermal analysis has been performed specifically for Si-doped HfO_2 FeFinFET structures within this work. This study integrates self-heating modeling with ferroelectric domain analysis to evaluate how temperature rise affects both electrical characteristics in Si-doped HfO_2 gate stacks. The combined dopant-dependent and electrothermal investigation provides a comprehensive understanding of Si-doped HfO_2-based FeFinFET performance, highlighting the necessity of addressing SHE for the development of thermally robust, high-performance ferroelectric transistors. Later, the work is also extended to circuit level, demonstrating the utility of heterodielectric vertically stacked FeFinFET (HD-VS-FeFinFET) as a CMOS inverter and NAND gate logic circuit.

This work is divided into five sections. Section II includes all the specifications regarding the device structure and fabrication process flowchart of HD-VS-FeFinFET. Section III explains the simulation framework and physical models. Section IV provides the results and discussion. Section V concludes the article.

II. Device Structure

Fig. 1(a) shows the 3-D structure of HD-VS-FeFinFET while Fig. 1(b) shows the 2-D structure of the device chopped vertically through its fin. The gate length is fixed at 20 nm, along the height and width of the fin are taken as 30 nm and 8 nm, respectively. Various ferroelectric materials are chosen for the simulation, with a thickness fixed at 6 nm with a total gate oxide thickness of 1 nm. Also, a trilayered strained silicon channel is formed with the stacking of silicon and silicon germanium having their mole fraction in the ratio of 0.7 and 0.3, respectively [15]. The doping concentration considered for the channel is 1×10^{16} cm^{-3} with p-type and that of source/drain is 1×10^{20} cm^{-3} with n-type, with a uniform profile. In addition, a metal gate with a work function set at 4.65 eV, having exceptional thermal stability and well-suited for CMOS processing, is used in this device to avert any poly-depletion effect

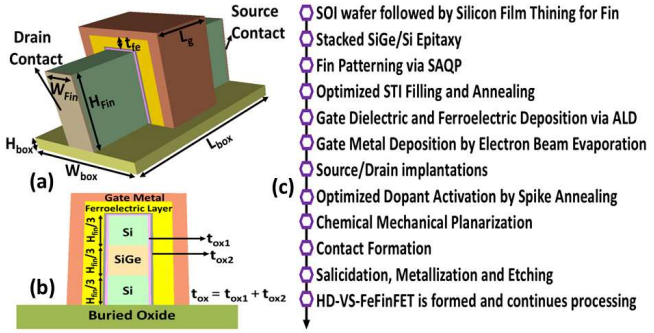

Fig. 1. (a) 3-D schematic view, (b) inset of vertical cross-sectional view, and (c) fabrication process flowchart for HD-VS-FeFinFET.

that usually occurs with polysilicon gates [24]. Furthermore, to exploit the benefits of SOI technology, the entire strained FeFinFET is built on an insulator box with a width, height, and length fixed at 32 nm, 5 nm, and 62 nm, respectively.

Fig. 1(c) illustrates the complete fabrication process flow of HD-VS-FeFinFET, demonstrating the feasibility of the proposed design. The process starts with an SOI wafer with a thick buried oxide and silicon layer, followed by controlled silicon thinning to define the fin. A SiGe/Si tri-layer is grown via reduced-pressure chemical vapor deposition (CVD), and fins are patterned using self-aligned quadruple patterning (SAQP). Shallow trench isolation (STI) is filled and densified by rapid thermal annealing (RTA). Gate dielectric and ferroelectric layers are deposited by atomic layer deposition (ALD), followed by metal gate formation via electron-beam evaporation. Source/drain implantation, spike annealing, and chemical mechanical planarization are performed, then metal contacts and interconnects are added, followed by backend steps. Finally, the HD-VS-FeFinFET is formed and undergoes testing with characterization to evaluate its electrical characteristics [16], [17].

III. Simulation Framework and Physical Models

All the simulations are done using Cogenda's Genius 3-D TCAD simulator. The simulation process includes the drift–diffusion model level 2 (DDML2) which considers the influence of lattice temperature by solving the extra thermal equation simultaneously with the electrical equations, coupled with consistent Poisson's equation as given by (1) [18], and continuity equations to govern the carrier transport phenomena for the electrons and the holes as given by (2) and (3), respectively [29]. This allows self-consistent coupling between carrier transport and lattice heating, enabling accurate evaluation of SHEs with thermodynamic models. So, on adding the thermal components, the final governing equations for DDML2 to consider the SHEs are summarized as follows:

$$\nabla.\epsilon\nabla\psi = -q\left(\mathrm{p} - \mathrm{n} + N_{\mathrm{D}}{}^{+} - N_{\mathrm{A}}{}^{-}\right) \tag{1}$$

$$\frac{\partial n}{\partial t} = \nabla.\left(\mu_{\mathrm{n}}\mathrm{n}\vec{E_{\mathrm{n}}} + \mu_{\mathrm{n}}\frac{k_{\mathrm{b}}T}{q}\nabla\mathrm{n} + \mu_{\mathrm{n}}\frac{k_{\mathrm{b}}\nabla T}{q}\mathrm{n}\right) - (U - G) \tag{2}$$

$$\frac{\partial \mathrm{p}}{\partial t} = -\nabla.\left(\mu_{\mathrm{p}}\mathrm{p}\vec{E_{\mathrm{p}}} - \mu_{\mathrm{p}}\frac{k_{\mathrm{b}}T}{q}\nabla\mathrm{p} - \mu_{\mathrm{p}}\frac{k_{\mathrm{b}}\nabla T}{q}\mathrm{p}\right) - (U - G) \tag{3}$$

$$\rho c_{\mathrm{p}} \frac{\partial T}{\partial t} = \nabla.\kappa \nabla T + \vec{J}.\vec{E} + \left(E_{\mathrm{g}} + 3k_{\mathrm{b}}T\right).(U - G) \tag{4}$$

where ψ is the electrostatic potential associated with the vacuum level, ϵ is the permittivity of the material, N^{D+} and N^{D-} are the concentrations for the ionized impurities, n and p are the concentration considered electron and hole, respectively, q is the electric charge, μ_{n} and μ_{p} are mobilities for electrons and holes, respectively, U and G are the recombination and generation rates associated for both electrons and holes, respectively, E_{n} and E_{p} are the effective driving electrical field for electrons and holes, respectively, ρ is the mass density of the semiconductor material considered, c_{p} is the heat capacity, κ is the thermal conductivity of the material, and $\vec{J}.\vec{E}$ Joule heating of the current [18].

Furthermore, the lattice heat flow model solves heat conduction, while Joule heating is included via the heat generation model. Bandgap variation with temperature is captured with the bandgap temperature dependence model to predict thermally induced leakage and parametric shifts. Thermal conductivity, dependent on lattice temperature, doping, layer thickness, and SiGe composition, is included for all layers in the physics modeling of TCAD. Also, Shockley–Read–Hall (SRH) recombination and Auger models accurately capture the temperature and doping-dependent recombination–generation phenomenon for carriers. Furthermore, the Philips mobility model for silicon germanium and the Lombardi mobility model for silicon are considered to take into account the mobility degradation at the semiconductor-oxide interface. The Lucent model is used to capture the high field mobility effects along with hot carrier models for considering the effect of hot carriers, and the Esurface models along with the velocity saturation model are activated [15]. The density gradient method is also used to consider quantum confinement phenomena along with the Fermi–Dirac carrier statistics model [18]. The simulation setup is validated against experimental data, keeping the device dimensions as L_g = 2 nm, H_{Fin} = 42 nm, and W_{Fin} = 8 nm with calibrated models [19]. Models parameters are tuned with low-field mobility and high-field saturation parameters (BETAN = 2 and BETAP = 1), acoustic phonon-limited velocities (4.75×10^7 cm/s for electrons and 9.93×10^6 cm/s for holes), contact resistivity ($2.4 \times 10^{-8}\Omega\cdot$cm^2), reference doping (NREFN = 1.1×10^{17} cm^{-3} and NREFP = 1.6×10^{17} cm^{-3}), and minimum mobilities (MUMINN = 56 cm^2/Vs and MUMINP = 46 cm^2/Vs). Phonon and surface roughness scattering coefficients (ALPHAN = 0.68, ALPHAP = 0.52, THETAN = 2.0, and THETAP = 1.6) ensured smooth low- to high-field transitions. Fig. 2(a) showcases the simulated transfer characteristics closely matching experimental data, thereby validating the model considerations of the simulation setup.

IV. Result and Discussion

A. Impact of Material-Specific Dopants in the HfO_2-Doped Ferroelectric Layer on the Device Performance

The physics of the ferroelectric layer is modeled with the time-dependent Landau–Khalatnikov (LK) framework for

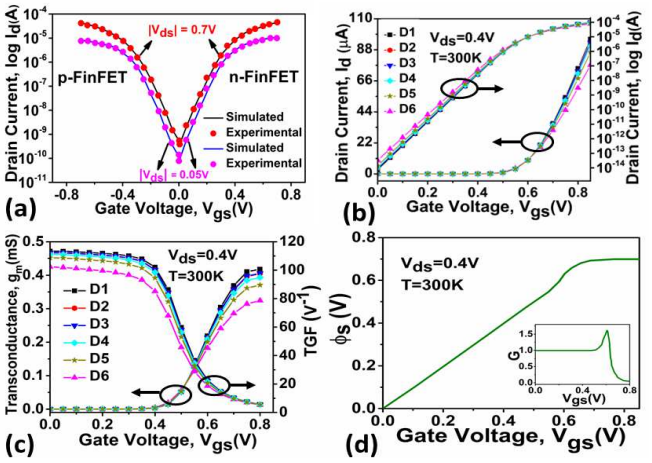

Fig. 2. (a) Calibration of the transfer characteristics (I_d–V_{gs}) of the FinFET device simulated against experimentally measured data at V_{ds} = 0.05 V and V_{ds} = 0.7 V. Impact of different dopant material on (b) transfer characteristics in the linear scale and semilogarithmic scale, (c) transconductance and TGF of HD-VS-FeFinFET, and (d) variation of surface potential with the gate voltage for silicon-doped HfO_2. The inset shows the gain versus gate voltage, showing voltage amplification.

TABLE I
Landau Coefficients for Various Dopant Material Considered for the HfO_2 Ferroelectric Layer

Dopant material	Configuration	α (cm/F)	β (cm^5/F/C^2)
Silicon	D1	-1.29×10^{11}	6.49×10^{20}
Gadolinium	D2	-1.13×10^{11}	1.42×10^{20}
Strontium	D3	-1.12×10^{11}	1.06×10^{20}
Aluminium	D4	-1.05×10^{11}	2.06×10^{20}
Zirconium	D5	-8.6×10^{10}	1.3×10^{20}
Lanthanum	D6	-3.46×10^{10}	8.55×10^{18}

associating the electric field used for the ferroelectric layer as a function of polarization (P), which is given by the following equation:

$$E_{\mathrm{FE}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - 2g\Delta P + \rho\left(\frac{\partial P}{\partial t}\right) \tag{5}$$

where α, β, and γ are the static Landau ferroelectric material-dependent coefficients, while g as the dipole interaction coefficient and ρ as the viscosity coefficient are taken as 1×10^{-4} cm^3/F and 2.25×10^4 $\Omega\cdot$cm, respectively, from the tool manual [18]. In this study, different material dopants are considered for HfO_2 and they are modeled with their associated values of α and β as summarized in Table I [6], [11], while keeping the value of γ as zero. Fig. 2(b) shows the impact of various dopants in the HfO_2 layer on the transfer characteristics of HD-VS-FeFinFET in the linear and log scales. The enhanced I_{ON} is achieved in $D1$ and $D2$, showing a higher dependency of I_{ON} on α, whereas the I_{OFF} degrades in $D6$ due to the lower value of β. More negative α in $D1$ and $D2$ augments the internal voltage amplification due to stronger polarization switching, which improves the surface potential modulation in the channel, better gate control, and higher drive current (I_{ON}) during the ON-state. Lower β in $D6$ deteriorates the stability of the ferroelectric polarization states, which results in less sharp polarization switching and

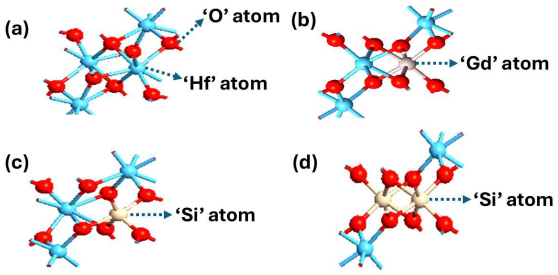

Fig. 3. Atomic-level structure considered for four different configurations (a) undoped HfO_2, (b) one gadolinium-doped HfO_2, (c) one silicon-doped HfO_2, and (d) two silicon-doped HfO_2.

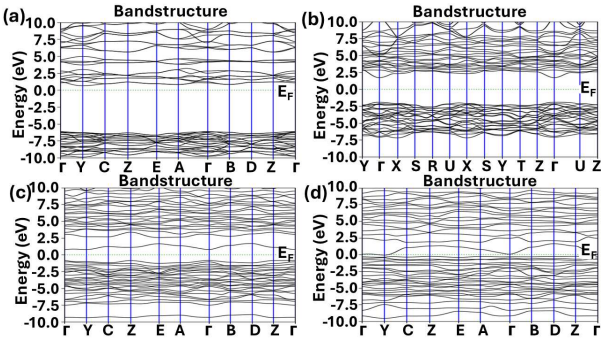

Fig. 4. Variation in the band structure of (a) undoped HfO_2, (b) one gadolinium-doped HfO_2, (c) one silicon-doped HfO_2, and (d) two silicon-doped HfO_2.

poor subthreshold control along with unwanted leakage paths. Hence, I_{OFF} (leakage current) increases in $D6$. Following the above trend, $D1$ shows significantly improved g_m when compared to other dopant materials used in HfO_2 due to the enhanced voltage amplification in $D1$, which sharpens the gate control over the channel, resulting in a higher transconductance (g_m) as shown in Fig. 2(c). Also, the transconductance generation factor (TGF), defined as the ratio of g_m to drain current (I_d), also shows its dependency on these Landau coefficients. A more negative value of α not only increases g_m but also enhances the TGF, as the improvement in g_m is proportionally higher relative to I_d in $D1$, as shown in Fig. 2(c). Conversely, $D6$ shows both the degraded trend for g_m and TGF due to weaker voltage amplification and resulting increased leakage current. So, the study supports that Si-doped HfO_2 showcased better ferroelectric property with improved device performance when compared to other material dopants. Fig. 2(d) depicts the variation of surface potential (ϕ_s) and voltage gain ($G = d\phi_s/dV_{gs}$) with gate voltage for silicon-doped HfO_2. A region of enhanced ϕ_s and a corresponding rise in gain indicate strong electrostatic coupling between the gate and channel, leading to evident voltage amplification.

B. DFT Studies on the Electronic Properties of HfO_2-Doped Ferroelectric Material at the Atomic Level

In the next section, DFT analysis is considered for studying the microscopic properties of these dopant materials. This work presents a systematic DFT study of the atomic and electronic properties of HfO_2 as a ferroelectric layer in an FET device. The comparative analysis of these parameters enables us to assess how doping modifies the electronic properties of HfO_2, which is critical for optimizing its performance in next-generation FeFET devices.

1) Crystal Structure and Computational Methodology: In this study, the atomic structure of ferroelectric HfO_2 was modeled in its orthorhombic crystalline phase, which is known to exhibit noncentrosymmetric distortion—a key characteristic for sustaining ferroelectric behavior. The primitive unit cell used for undoped HfO_2 consists of four hafnium (Hf) atoms and eight oxygen (O) atoms, arranged in a lattice defined by the parameters: lattice constants aaa, bbb, ccc, and angles α, β, and γ. The orthorhombic symmetry facilitates the formation of a polar phase, crucial for applications in FeFETs. To explore the influence of doping on the electronic properties, three doped variants of HfO_2 are considered along with undoped HfO_2 as showcased in Fig. 3: (a) undoped HfO_2, (b) gadolinium-doped HfO_2 (Gd-doped HfO_2): one Hf atom is replaced by a Gd atom, (c) single silicon-doped HfO_2 (1-Si-doped HfO_2): one Hf atom is replaced by a Si atom, (d) double silicon-doped HfO_2 (2-Si-doped HfO_2): two Hf atoms are replaced by two Si atoms.

2) Method of Crystal: All structures are geometrically optimized using DFT as implemented in the quantum ATK simulation package. The Perdew–Burke–Ernzerhof (PBE) exchange–correlation functional under the generalized gradient approximation (GGA) was employed for all calculations. Ultrasoft pseudopotentials were used for the core electrons, and a plane-wave basis set with an energy cutoff suitable for transition-metal oxides was chosen to ensure convergence. Brillouin zone integrations were performed using a Monkhorst–Pack kkk-point mesh, optimized for energy convergence [20], [21].

3) Performance Comparison: Fig. 4 reveals the band structure of four configuration. The electronic band structures for all four configurations were computed to evaluate their relative bandgaps and electronic transition characteristics. The double Si-doped HfO_2 crystal exhibited a lower bandgap when compared to the undoped, Gd-doped, and single Si-doped structures. A reduced bandgap implies enhanced carrier injection and improved switching behavior, both of which are desirable for FET applications.

Fig. 5 shows the projected density of state (PDOS) of four configurations. The PDOS profiles show a significantly higher peak near the Fermi level for the 2-Si-doped HfO_2 structure. A higher PDOS near the Fermi level enhances the material's ability to conduct charge and supports better ferroelectric polarization switching. This behavior suggests that 2-Si doping increases the availability of electronic states for conduction, making it more suitable for electronic and ferroelectric applications.

Fig. 6 shows the Hartree potential versus length for four configurations. The Hartree potential profile showed a pronounced peak in the 2-Si-doped HfO_2 structure when compared to other variants. Hartree potential gives insights into the internal electrostatic environment, which is critical for

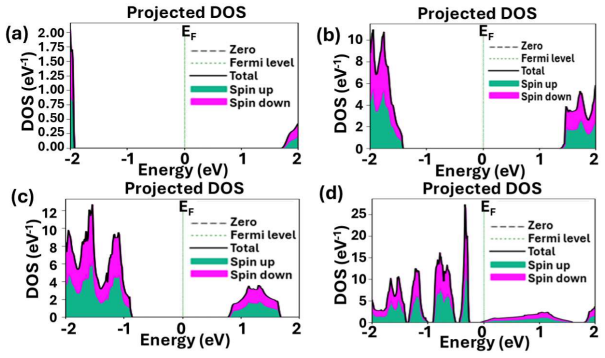

Fig. 5. Variation in PDOS of (a) undoped HfO_2, (b) one gadolinium-doped HfO_2, (c) one silicon-doped HfO_2, and (d) two silicon-doped HfO_2.

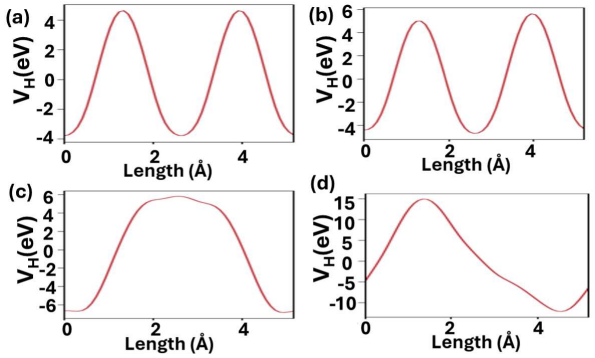

Fig. 6. Variation in Hartree potential of (a) undoped HfO_2, (b) one gadolinium-doped HfO_2, (c) one silicon-doped HfO_2, and (d) two silicon-doped HfO_2.

polarization stability in ferroelectric materials. The enhanced potential profile could support robust dipole alignment and retention, important for nonvolatile memory applications in FeFETs.

Among all studied configurations, the double Si-doped HfO_2 crystal exhibits the most favorable characteristics for FeFET applications. The simultaneous enhancement in PDOS, Hartree potential, along with a reduced bandgap, points to a synergistic effect of dual-Si doping in promoting desirable electronic and ferroelectric properties.

C. Influence of SHE on the Performance of HD-VS-FeFinFET Under Varying Biasing Conditions and Ambient Temperatures

This section focuses on analyzing the impact of SHEs on the performance of HD-VS-FeFinFET, comparing its crucial performance parameters with and without considering self-heating. Additionally, the study investigates how this impact varies under varying biasing voltages. These insights are critical for designing thermally robust and low-power FinFET-based circuits.

As showcased in Fig. 7(a), the transfer characteristics of the device shift downward, exhibiting lower ON current when compared to the ideal curve (without considering SHE). This reduction is attributed to channel temperature rise by self-heating, which is quite visible in the inversion region where

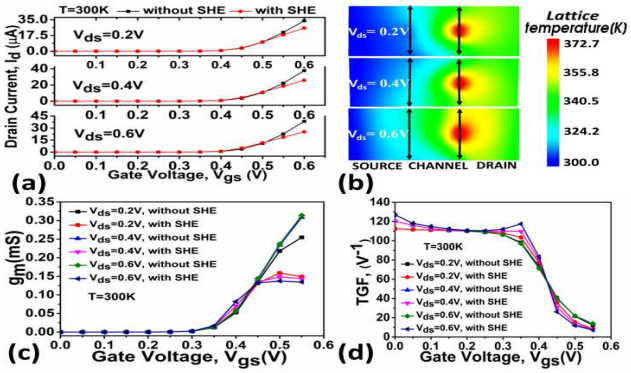

Fig. 7. Influence of SHE on (a) transfer characteristics, (b) contour profile of lattice temperature, (c) g_m, and (d) TGF of HD-VS-FeFinFET at different biasing voltages.

high drain current and power dissipation generate substantial heat in the channel. This results in channel temperature rise, which leads to phonon scattering and ultimately mobility degradation. On the other hand, the leakage current is observed to be almost the same in the case of with and without considering self-heating as the transistor's low subthreshold current generates minimal heat, causing negligible temperature rise and leaving drain characteristics almost unaffected in the subthreshold region. Thereafter, as V_{ds} is reduced, overall ON current reduces, and this reduction is observed in both cases with and without considering SHE. Moreover, SHE impact is less noticeable at lower V_{ds} as degradation in I_{ON} is 24% when compared to degradation of 34.1% at V_{ds} = 0.6 V. This is because of the less localized self-heating within the channel at lower V_{ds}. This is also observable in the contour profile showing the lattice temperature in the device at different supply voltages in Fig. 7(b). As it is observed, as V_{ds} increases, the lattice temperature contour profile evolves from a nearly uniform distribution to a highly localized hot spot near the channel-drain region. The temperature peak shifts closer to the drain side, as maximum energy dissipation happens in this region due to the higher electric field.

Fig. 7(c) shows the variation in transconductance with variation in V_{gs} with and without considering SHE, that too at varying drain supply. In the absence of SHE, g_m rises steadily with V_{gs} and then saturates with a maximum peak for higher V_{ds}. In contrast, in the case of consideration of SHE, for higher V_{ds}, weakened transconductance is observed at higher V_{ds} due to significant localized channel heating. Moreover, the g_m curve with SHE flattens earlier and stays below without SHE, indicating degraded gate control due to thermal effects. Fig. 7(d) shows the variation of TGF at different operational conditions, and as can be observed from the figure, TGF increases as the supply voltage increases due to enhanced inversion and better channel control. Also, the SHE seems to have no impact on TGF at the subthreshold region since the channel temperature does not rise significantly above the ambient temperature to generate contributory heat.

Furthermore, it is explored how the temperature rise, combined with self-heating, alters the device characteristics,

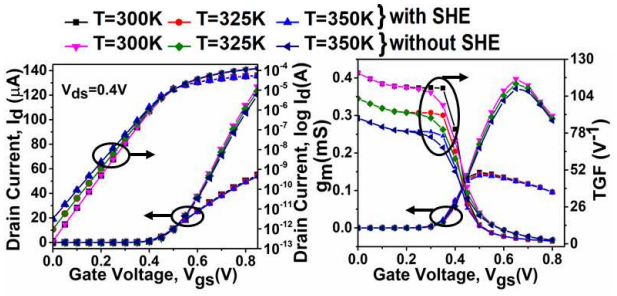

Fig. 8. Influence of SHE on (a) transfer characteristics in linear and semilogarithmic scale and (b) g_m and TGF of HD-VS-FeFinFET at different ambient temperature.

which is critical for evaluating the thermal robustness of the device. Fig. 8(a) shows the transfer characteristics of the device in linear and semilogarithmic scales at various ambient temperatures, along with comparing performance with SHE included. The drain current degraded with increasing temperature, both in the inversion and subthreshold regions, because of carrier mobility degradation due to phonon scattering. In addition, SHE exacerbates this degradation further in the inversion region due to added localized heating in addition to ambient temperature rise, as shown in Fig. 8(a). Furthermore, the semilogarithmic plot shows that in the subthreshold region, since current is very small, power dissipation and hence self-heating are minimal, leading to the overlap of "with SHE" and "without SHE" curves.

Fig. 8(b) shows the variation in transconductance with varying ambient temperature, along with the impact of SHE. With SHE, g_m is consistently lower when compared to g_m without SHE due to degrading carrier mobility with a rise in local channel temperature. Moreover, the peak transconductance shifts toward lower V_{gs} under the influence of SHE because of the early onset of strong inversion at lower V_{gs}. Furthermore, at higher V_{gs}, self-heating becomes more pronounced due to higher power dissipation as a result of Joule heating. Fig. 8(b) shows the influence of SHE on TGF at varying ambient temperatures. First, it is observed that TGF is higher at lower temperatures due to reduced phonon scattering and increased carrier mobility when compared to TGF at increasing temperatures. Second, there is an overlap of SHE and without the SHE curve at lower V_{gs}. It is due to the fact that the inversion layer in the channel is not strongly formed, thus, power dissipation is minimal, hence the effect of self-heating.

While self-heating introduces performance challenges, the device still demonstrates strong operational stability at lower and higher gate biases. With its enhanced mobility benefits and manageable self-heating impact through optimized design and thermal strategies, this device structure holds significant promise for reliable, high-performance applications across varying ambient temperatures.

D. Circuit-Level Analysis of HD-VS-FeFinFET-Based CMOS Inverter for the Characteristics Performance Parameters Under Varying Biasing Voltages and Ambient Temperatures

For this, a required setup is designed with Cogenda Visual TCAD simulator with n-channel and p-channel

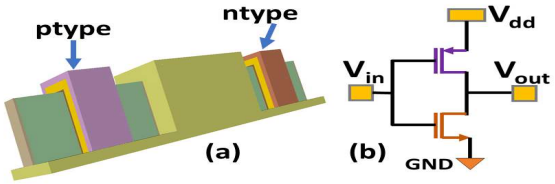

Fig. 9. (a) 3-D structure and (b) schematic of HD-VS-FeFinFET-based CMOS inverter.

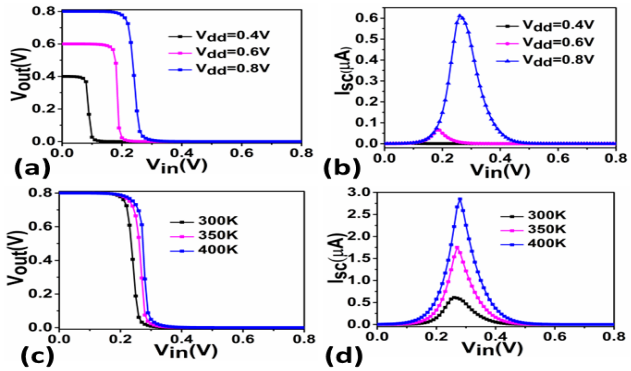

Fig. 10. Impact of varying biasing voltage on (a) VTCs and (b) switching current and impact of varying ambient temperature on (c) VTCs and (d) switching current of the HD-VS-FeFinFET-based CMOS inverter.

HD-VS-FeFinFET isolated electrically with the help of 60-nm SiO_2 spacer. Fig. 9(a) and (b), respectively, shows the 3-D view and schematic of the CMOS inverter circuit, where V_{dd}, V_{in}, and V_{out} are the supply voltage, input voltage, and output voltage, respectively. The performance analysis done for this device-based CMOS inverter is essential in understanding its behavior under varying operational conditions, which is very crucial for modern low-power and high-speed circuit designing. Key performance parameters such as the voltage transfer characteristic (VTC) curve, propagation delay, switching current, rise time, and fall time directly govern the inverter's reliability and efficiency for digital applications. This study focuses on evaluating these parameters at different ambient temperatures and various biasing voltages to assess thermal stability and voltage scalability for this CMOS inverter.

The variation in the VTC curve with variation in supply voltages is showcased in Fig. 10(a). It is visible from the figure that as the supply voltage decreases, the switching threshold voltage moves toward the lower input voltage because the available gate overdrive voltage for both the n-type device and p-type device reduces, which causes both the transistors to switch more slowly and the point where their current equalizes shifts toward a lower voltage. Fig. 10(b) showcases the trend of switching current for varying supply voltage. It follows the same trend with the peak of I_{sc} shifts leftward as the peak switching current occurs near the inverter's switching threshold voltage. Also, with a lower supply voltage, the transistors operate in a more resistive region, which limits the peak current in switching transitions.

Furthermore, Fig. 10(c) shows the shift of approximately 34.627 mV in switching threshold voltage of the inverter as the

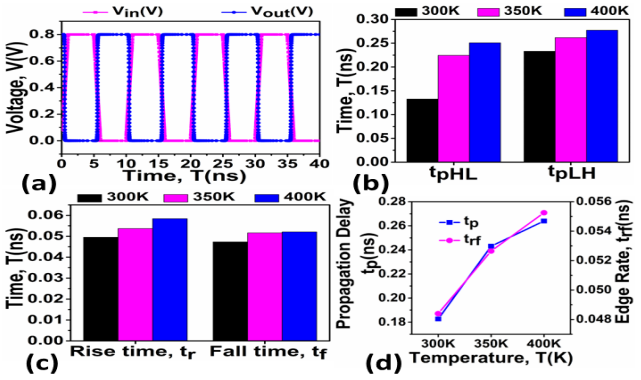

Fig. 11. Influence of ambient temperature on (a) transition time schematic, (b) components of propagation delay, (c) rise time and fall time, and (d) propagation delay and edge rate of HD-VS-FeFinFET-based CMOS inverter.

TABLE II
COMPARISON OF PERFORMANCE PARAMETERS OF THE HD-VS-FEFINFET-BASED CMOS INVERTER WITH OTHER PUBLISHED CMOS INVERTERS

Ref.	Inverter structure	t_{pHL} (ns)	t_{pLH} (ns)	t_p (ns)	t_r (ns)	t_f (ns)	t_{rf} (ns)
[23]	Strained Bulk FinFET Inverter	41	65	53	33	69	51
[24]	Modified NCFET inverter	0.52	0.255	0.387	0.068	0.064	0.066
[25]	Mosfet inverter	-	-	0.5	-	-	1.2
[23]	s-SOI FinFET inverter	43	59	51	27	61	44
This work	HD-VS-FeFinFET inverter	0.132	0.233	0.183	0.058	0.052	0.055

ambient temperature is varied from 300 to 400 K. The rightward shift indicates that the inverter requires a slightly higher input voltage to switch at elevated temperatures, primarily due to reduced carrier mobility and altered threshold voltage of the transistors. Fig. 10(d) also shows that there is rightward shift in peak of switching current (I_{sc}) along with increase up to 4.66 times as the temperature is increased to 400 K. This increase in switching current can be attributed to enhanced subthreshold leakage and thermally activated carriers, which contribute to higher current flow during the switching transition at elevated temperatures. Although there is slow switching at a lower supply voltage but this trend can also be exploited for low power designs, as reduced switching leads to lower power consumption, which is demanding on power delivery circuits [17].

In the case of FET-based CMOS inverters, various non-idealities come into the picture, one of which is parasitic capacitances. These intrinsic capacitances existing between the device terminals introduce delay in voltage transition from low to high or from high to low, thus limiting the switching speed of the inverter [22]. For this, a step voltage is applied at the input terminal of the inverter, and the resulting output waveform of this logic circuit is analyzed as shown in Fig. 11(a). Subsequently, two propagation delay components, namely high to low propagation delay and low to high propagation delay, are analyzed as showcased in Fig. 11(b). It showcased the variation in these components with varying ambient temperature. It can be observed that as the temperature increases, both components of the propagation delay decrease, as shown in the figure. This behavior is attributed to mobility degradation of charge carriers at elevated temperatures, which slows down the charging and discharging of parasitic capacitances.

Similarly, rise and fall times of the inverter are analyzed to understand the response time and sharpness of the inverter. These parameters serve as key indicators of how quickly the inverter transitions between logic states. Fig. 11(c) shows that as the temperature increases, there is an increase in both rise time and fall time. This is primarily due to enhanced phonon scattering, which slows down the rate at which output node charges and discharges, and thus requires more time for the output voltage to make a transition between logic levels.

Later, Fig. 11(d) shows the variation in propagation delay and edge rate, which also shows a similar trend due to less sharpness and gentler sloppiness during transition with a temperature rise. This controlled current flow can reduce peak dynamic power consumption, leading to potentially lower power dissipation peaks, especially during rapid switching sequences. Though increased rise/fall times and propagation delays typically suggest reduced speed, in FeFinFET-based CMOS inverters, these trends can be harnessed as indicators of thermal stability, noise resilience, and controlled dynamic behavior, which are critical for reliable and robust circuit designs in high-temperature or mission-critical applications. Table II highlights improved propagation delay and transition parameters, demonstrating the superior efficiency and reliability of the proposed HD-VS-FeFinFET CMOS inverter for circuit integration.

Furthermore, to evaluate the circuit-level applicability of the proposed device, a two-input NAND gate is implemented using HD-VS-FeFinFET. The circuit consists of two p-type HD-VS-FeFinFETs connected in parallel in the pull-up network and two n-type HD-VS-FeFinFETs connected in series in the pull-down network, forming a standard CMOS configuration. The schematic representation of the proposed HD-VS-FeFinFET-based NAND gate along with its corresponding truth table is illustrated in Fig. 12(a) and (b), respectively. The transient response of the circuit, shown in Fig. 12(c), validates the correct functionality of the NAND logic circuit, demonstrating accurate output transitions for all possible input combinations.

The results demonstrate consistent performance trends, providing valuable insights, though certain aspects offer opportunities for further exploration. This study examined the impact of SHE on the proposed device under varying bias and temperature conditions, revealing that SHE can degrade performance through mobility reduction and accelerated gate dielectric wear. While mitigating SHE requires careful CMOS

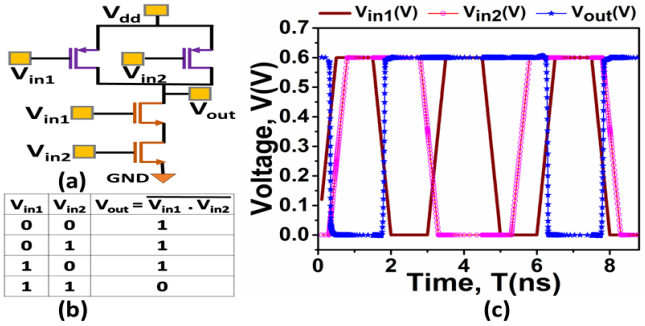

Fig. 12. (a) Schematic of the two-input NAND gate circuit, (b) its truth table, and (c) transient response of the NAND gate circuit.

design as given in these literatures [26], [27], it can also be exploited positively via electrothermal annealing (ETA) to rejuvenate aged dielectrics, particularly in nanoscale devices [28]. Future work could explore device configurations to harness SHE for self-recovery. Also, fabricated FeFinFETs may exhibit process-induced variations (channel length, doping, and oxide thickness) affecting switching behavior, and intrinsic material factors like interface traps and oxide quality can influence performance at elevated temperatures. Long-term reliability under repeated thermal cycling was not studied, and alternative channel materials or device geometries could be considered. Despite these limitations, the analysis provides a holistic understanding of the proposed ferroelectric-based device and offers guidance for optimized designs in low-power, high-speed electronics. Addressing these factors in future studies would enhance the reliability and generalizability of the findings.

V. Conclusion

This study presents a comprehensive multiscale analysis connecting the impact of material doping at the material level with DFT calculations and at the device level. The analysis of various dopant materials in HfO_2 concludes that increasing the negative value of the ferroelectric Landau parameter, such as alpha and beta, improves the performance characteristics of the device with 24% rise in I_{ON} and 77.4% reduction in leakage current in the case of silicon dopant ($D1$) over lanthanum dopant material ($D6$) due to enhanced surface potential modulation in the channel. Furthermore, the two best dopant material structures, Si-doped HfO_2 and Gd-doped HfO_2, are analyzed microscopically using DFT calculation with comparison in their band structure, PDOS, and Hartree potential. Subsequently, considering the cruciality of thermal robustness, the present study also addresses the critical impact of SHE at varying biasing voltages and ambient temperatures, particularly in the context of Si-doped HfO_2-based FeFinFETs. It is observed that there is significant impact of SHE on drain characteristics of the device but it is very much dependent on region of operation of the device such as the g_m and TGF show minimal degradation in subthreshold region as 4.11% and 3.33% at V_{ds} = 0.4 V but with the onset of inversion, significant degradation can be observed with 36.6% and 39.7%, respectively. Furthermore, the exploration of how the temperature rise combined with self-heating alters the device characteristics revealed that the peak g_m shifts toward lower V_{gs} along with smoothness in TGF under the influence of SHE because of the early onset of strong inversion at lower V_{gs}. In continuation, we have examined the device-based CMOS inverter to understand the effect of supply voltages and ambient temperature, with key performance parameters such as VTC curve, propagation delay, switching current, rise time, and fall time to govern the inverter's reliability and efficiency for digital applications. Together, these characteristics suggest that, with appropriate voltage scaling and thermal management, the circuit can leverage temperature-driven switching behavior to achieve enhanced speed and performance in next-generation low-power, high-performance electronic applications.

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