

DESIGN AND IMPLEMENTATION OF REVERSIBLE LOGIC GATES AND ITS APPLICATION IN EMERGING TECHNOLOGIES

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DIKSHA RUHELA

Univ. Roll No: 2k19/PhDCO/11

UNDER THE GUIDANCE OF

Prof. RAJNI JINDAL

(Professor)

Department of Computer Science & Engineering

Delhi Technological University, Delhi



DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(FORMERLY DELHI COLLEGE OF ENGINEERING)

DELHI-42

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DECLARATION

I, **Diksha Ruhela**, Roll No. **2k19/PhDCO/11**, Ph.D. Scholar in the **Department of Computer Science & Engineering**, hereby declare that this thesis entitled “*Design and Implementation of Reversible Logic Gates and Its Application in Emerging Technologies*”, submitted to **Delhi Technological University, Delhi**, is a record of the original work carried out by me under the guidance of **Prof. Rajni Jindal (Professor, Department of Computer Science & Engineering)**.

This thesis work is submitted in partial fulfilment of the requirements for the award of the degree of **Doctor of Philosophy (Ph.D.) in Computer Science & Engineering**.

I solemnly and sincerely affirm that all the particulars stated above are true and correct to the best of my knowledge and belief.

Place: Delhi

DIKSHA RUHELA

Date:

2K19/PHDCO/11

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This is to certify that the thesis entitled “*Design and Implementation of Reversible Logic Gates and Its Application in Emerging Technologies*” is a Bonafide work of **Diksha Ruhela** (University Roll No. 2k19/PhDCO/11), Ph.D. Scholar, **Delhi Technological University, Delhi**.

This research work was carried out under my direct supervision and guidance and forms a part of the **Doctor of Philosophy (Ph.D.) Programme in Computer Science & Engineering** at Delhi Technological University.

To the best of my knowledge, the matter embodied in this thesis has not been submitted to any other University or Institute for the award of any degree or diploma.

Date:

PROF. RAJNI JINDAL

(Supervisor)
Professor,
Department of Computer
Science & Engineering,
Delhi technological University

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ABSTRACT

The increasing demand for high-speed, low-power, and scalable computing architectures has driven significant interest in reversible logic and all-optical computation. Conventional irreversible electronic systems inherently dissipate energy due to information loss, while photonic technologies offer ultra-fast signal propagation and immunity to electromagnetic interference. Reversible logic, when combined with optical implementations, provides a promising pathway toward energy-aware, quantum-compatible, and high-throughput computing systems.

This thesis presents a comprehensive investigation into the design, modeling, and realization of reversible arithmetic and logic circuits for fixed-point unsigned integer data, with a primary focus on quantum and all-optical architectures.

The work begins with the design of a reversible 4×4 -bit Vedic multiplier based on the Urdhva–Tiryagbhyam (UT) algorithm, constructed using two proposed 2×2 Vedic multiplier modules and newly developed reversible ripple-carry adder (RCA) and carry-save adder (CSA) circuits. The proposed 4-bit Vedic multiplier is analytically compared with state-of-the-art reversible designs and is shown to be superior in terms of quantum cost (QC), gate count (GC), hardware complexity (HC), ancilla inputs (AI), and garbage outputs (GO). Logical correctness is verified using Xilinx Vivado, and an entropy-based analysis confirms the energy-saving benefits of reversibility by demonstrating reduced information loss.

Building on this optimized real multiplier, the architecture is extended to realize a reversible complex Vedic multiplier in the quantum domain, following a modular and scalable design methodology.

The thesis then explores all-optical N -bit Vedic multipliers based on MZI–SOA interferometric switches, constructed using existing optical adder architectures. These designs are analytically benchmarked against prior optical multipliers in terms of optical cost (OC) and optical delay (OD), and closed-form expressions for N -bit OC and OD are derived. The analysis reveals inherent scalability and stability limitations of interferometer-based designs due to phase sensitivity, interferometer duplication, and irreversibility.

To overcome these challenges, interferometer-free RSOA-based reversible optical architectures are proposed. A family of RSOA-based reversible logic gates and arithmetic blocks is developed using cross-gain modulation (XGM). Using these primitives, scalable N -

bit reversible Vedic multipliers are formulated analytically, and expressions for OC, OD, constant inputs (CI), and garbage outputs (GO) are derived.

A key contribution of the optical domain is the design of a parity-preserving 2×2 -bit reversible optical Vedic multiplier, implemented using RSOA-based logic gates. This multiplier is photonic-level simulated, and its performance is quantitatively evaluated using Extinction Ratio (ER), Q-factor, and Relative Eye Opening Percentage (REOP). Comparative analysis with existing optical multipliers demonstrates superior signal integrity and fault-awareness. This parity-preserving 2-bit building block is then extended analytically to construct an N-bit complex Vedic multiplier, with closed-form expressions derived for OC, OD, CI, and GO.

Additionally, the thesis introduces a novel universal reversible NAND–NOR gate (NTG) realized using a hybrid RSOA and MZI–SOA switching mechanism, capable of implementing all fundamental Boolean logic functions and serving as a universal primitive for reversible optical logic synthesis.

The final part of the thesis develops a reversible RSOA-based universal multiplexer framework, including 2×1 and 4×1 multiplexers, and demonstrates how these structures can realize all basic logic functions (AND, OR, NOT, XOR, XNOR, NAND, NOR) as well as half-adder and half-subtractor circuits. Performance evaluation based on Contrast Ratio (CR), Extinction Ratio (ER), and Relative Eye Opening Percentage (REOP) confirms the superior signal quality, robustness, and integration potential of the proposed RSOA–FRG architecture compared to existing photonic logic designs.

Overall, this thesis establishes a unified, modular, and scalable methodology for reversible arithmetic and logic circuit design across quantum and photonic domains. The proposed architectures demonstrate strong potential for energy-efficient, fault-tolerant, and high-speed computation, providing a solid foundation for future extensions toward floating-point arithmetic, sequential reversible circuits, and large-scale integrated optical and quantum computing systems.

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LIST OF ABBREVIATION

Abbreviation Full Form

ALU	Arithmetic Logic Unit
AND	Logical AND Operation
ASE	Amplified Spontaneous Emission
BDD	Binary Decision Diagram
BER	Bit Error Rate
BPF	Band-Pass Filter
BS	Beam Splitter
CCNOT	Controlled-Controlled NOT (Toffoli Gate)
CEA	Control Energy
CI	Constant Inputs
CMOS	Complementary Metal–Oxide–Semiconductor
CNOT	Controlled-NOT (Feynman Gate)
CR	Contrast Ratio
CSA	Carry-Save Adder
DFG	Double Feynman Gate
DSP	Digital Signal Processing
ER	Extinction Ratio
FG	Feynman Gate
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FRG	Fredkin Reversible Gate
GC	Gate Count
GO	Garbage Outputs
HC	Hardware Complexity
I/O	Input/Output
ISI	Inter-Symbol Interference
LUT	Lookup Table
MRR	Micro-Ring Resonator
MIG	Modified Islam Gate
MIM	Metal–Insulator–Metal Waveguide
MZI	Mach–Zehnder Interferometer
MZI–SOA	Mach–Zehnder Interferometer using Semiconductor Optical Amplifier
MUX	Multiplexer
NAND	NOT–AND
NCGM	Non-linear Cross-Gain Modulation
NOR	NOT–OR

Abbreviation Full Form

NTG	NAND–NOR Reversible Gate
OC	Optical Cost
OD	Optical Delay
OR	Logical OR
PBS	Polarizing Beam Splitter
PG	Peres Gate
PIC	Photonic Integrated Circuit
PPTG	Parity-Preserving Toffoli Gate
QF	Quality Factor
QC	Quantum Cost
QFT	Quantum Fourier Transform
QKD	Quantum Key Distribution
RCA	Ripple-Carry Adder
REOP	Relative Eye-Opening Percentage
RSOA	Reflective Semiconductor Optical Amplifier
SNR	Signal-to-Noise Ratio
SOA	Semiconductor Optical Amplifier
SPP	Surface Plasmon Polariton
SUB	Subtraction Output
TDM	Time-Division Multiplexing
TG	Toffoli Gate
UT	Urdhva Tiryagbhyam (Vedic Multiplication Sutra)
VOA	Variable Optical Attenuator
XGM	Cross-Gain Modulation
XOR	Exclusive-OR
XNOR	Exclusive-NOR

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Chapter 1: Introduction

1.1 Background and Motivation

The rapid expansion of computational demands in artificial intelligence, high-performance computing, signal processing, and cryptography has intensified the need for energy-efficient architectures. While transistor scaling has historically followed Moore's Law, further miniaturization of CMOS technology faces a fundamental barrier: the thermodynamic cost of irreversible computation. According to Landauer's principle (1961), each bit of information erased in an irreversible logic operation dissipates a minimum energy of $kT \ln 2$ joules, where k is Boltzmann's constant and T is the operating temperature. This intrinsic energy loss becomes increasingly significant in nanoscale technologies, leading to heat buildup, reduced reliability, and efficiency bottlenecks.

Bennett (1973) demonstrated that computation can be performed without this energy penalty if the process is logically reversible, meaning every output state uniquely maps back to an input state. Reversible computing thus emerges as a promising paradigm enabling ultra-low-power information processing. Moreover, reversibility is not merely advantageous—it is fundamental in quantum computing, where all transformations are unitary and inherently reversible. Similarly, optical computing leverages the physics of photons—massless, high-speed carriers unaffected by resistive losses—to perform computation with minimal energy dissipation [1, 2]. Optical devices such as Mach–Zehnder Interferometers (MZI–SOAs) and Reflective Semiconductor Optical Amplifiers (RSOAs) provide pathways for realizing ultrafast, high-bandwidth, and low-power all-optical circuits. Meanwhile, quantum computing inherently requires reversible arithmetic units due to its dependence on bijective transformations. Across both domains, multiplication is one of the most critical operations, forming the computational backbone of DSP algorithms, FFTs, convolution, filtering, modulation, image analysis, and machine learning. Efficient reversible multipliers are therefore essential for next-generation computing systems.

Despite extensive research, significant gaps remain in designing scalable, resource-efficient reversible circuits—particularly complex multipliers—in both quantum and optical domains. This thesis is motivated by addressing these gaps through novel architectures that integrate reversible logic principles with high-speed optical switching and quantum gate synthesis.

1.2 Fundamentals of Reversible Logic Design

Reversible logic is a computational paradigm in which a one-to-one correspondence exists between the input and output vectors of a logic function. This bijective mapping ensures that the original input values can be uniquely reconstructed from the outputs, thereby preventing the loss of information during computation. As a result, reversible computation theoretically avoids the fundamental energy dissipation associated with information erasure, as established by Landauer's principle.

The design of reversible circuits introduces a set of constraints and performance parameters that differ fundamentally from those of conventional irreversible logic. These include the presence of garbage outputs, which are auxiliary outputs required to preserve reversibility but do not contribute to the functional result, and constant inputs, which are ancillary lines initialized to fixed logical values to enable desired reversible transformations. In addition, quantum cost is widely used as a key metric to evaluate the hardware efficiency and resource requirements of reversible and quantum-compatible circuits.

Unlike irreversible logic, reversible systems prohibit direct fan-out and feedback, as these operations violate the bijective input–output relationship. Consequently, signal replication and conditional control must be achieved using specialized reversible gate structures. A set of fundamental reversible gates—including the Feynman, Toffoli, Fredkin, and Peres gates—serve as the primary building blocks for constructing reversible arithmetic and control circuits. These gates are extensively employed in both quantum computing architectures and optical logic implementations.

Reversible logic design thus provides a unified framework for developing energy-efficient arithmetic circuits compatible with emerging computing technologies. In quantum systems, reversibility is a strict requirement due to the unitary nature of quantum operations, while in optical computing, reversible logic supports low-power, high-speed signal processing by preserving information throughout the computation. The detailed structures, operating principles, and performance characteristics of reversible logic gates and arithmetic circuits are examined comprehensively in Chapter 2 [3-5].

1.3 Problem Statement

Although reversible logic promises energy-efficient computation, several challenges persist in both quantum and optical domains.

1. Quantum Circuit Design Bottlenecks

- Quantum reversible circuits for arithmetic operations frequently incur high quantum cost, excessive garbage outputs, and large circuit depth, significantly limiting scalability.
- There is a growing demand for compact, low-resource, and hardware-efficient reversible arithmetic units suitable for future quantum processors.
- No optimized reversible design for a complex multiplier has been reported in quantum literature, despite its importance in signal processing and communication systems.
- Existing designs often lack modularity and architectural uniformity, making integration into larger quantum systems difficult.

2. Optical Domain Challenges

- Optical reversible circuits reported in literature predominantly rely on MZI–SOA interferometric structures, which suffer from large footprint, thermal drift, polarization dependence, and strict alignment requirements.
- Although RSOA-based switching offers compact and interferometer-free operation, its potential for realizing reversible optical arithmetic circuits has not yet been fully exploited.
- The realization of reversible optical arithmetic circuits using RSOA-based switching remains a challenging and underexplored problem.
- The integration of MZI–SOA and RSOA devices within reversible optical logic gate design presents unresolved implementation challenges.
- Existing optical multipliers exhibit high optical delay and complexity, making them unsuitable for ultrahigh-speed computation.

These limitations collectively highlight the need for new reversible architectures in both quantum and optical domains, with enhanced scalability, reduced hardware complexity, and practical integration potential.

1.4 Objectives of the Thesis

The primary objectives of this research are as follows:

- To design quantum-compatible reversible real and complex multipliers optimized for low quantum cost and minimal garbage outputs.
- To develop compact, interferometer-free reversible optical logic gates and circuits using RSOA-based switching, enabling energy-efficient all-optical computation.
- To design scalable n-bit all-optical multipliers using MZI–SOA switching and to realize interferometer-free n-bit all-optical multipliers using RSOA-based switching for comparative evaluation.

- To implement parity-preserving reversible optical logic circuits using RSOA-based gates for enhanced fault tolerance and error detection.
- To design a universal RSOA-based reversible logic gate capable of generating NAND and NOR functions within a single gate structure, thereby enabling the realization of arbitrary Boolean logic.

1.5 Research Contributions

The thesis makes the following significant research contributions in the domains of reversible logic, optical computing, and quantum arithmetic:

- **Quantum Reversible Real and Complex Multipliers Based on Vedic Mathematics:** Reversible multiplier designs for both real and complex arithmetic are proposed in the quantum domain using Vedic mathematical principles. The architectures employ optimized reversible gates such as Toffoli, Fredkin, and Peres gates, achieving reductions in quantum cost and garbage outputs compared to existing reversible multiplier designs.
- **RSOA-Based Interferometer-Free 2×2 Reversible Optical Multiplier with State-of-the-Art Comparison:** An interferometer-free 2×2-bit reversible optical multiplier is designed using RSOA-based switching. The proposed design is quantitatively compared with state-of-the-art optical multiplier implementations in terms of Q-factor, received optical power (REOP), and extinction ratio (ER), demonstrating the advantages of RSOA-based reversible logic in terms of signal quality and optical performance.
- **RSOA-Based Scalable n-Bit Reversible Optical Multiplier with Comparative Analysis:** Scalable n-bit reversible optical multiplier is designed using RSOA-based switching. For comparison, an n-bit MZI-SOA-based optical multiplier is implemented and evaluated against existing interferometer-based multiplier designs reported in the literature, which are not fully reversible in nature. The RSOA-based reversible multiplier is then designed to highlight the benefits of interferometer-free operation, improved compactness, and enhanced suitability for scalable reversible optical arithmetic.
- **Parity-Preserving Reversible Optical Complex Multipliers:** A parity-preserving reversible optical complex multiplier is developed using RSOA-based logic gates. Initially, a 2-bit Vedic multiplier is designed and compared with state-of-the-art optical multiplier implementations in terms of extinction ratio (ER), received optical power (REOP), and Q-factor. The validated design is subsequently extended to realize an n-

bit reversible optical complex multiplier, with performance metrics derived and evaluated in terms of optical cost, optical delay, constant inputs, and constant outputs.

- **Parity-Preserving RSOA-Based Reversible Logic and Multiplexer Gates:** Novel parity-preserving reversible logic gates are designed using RSOA-based switching, including reversible multiplexer (MUX)-based logic gates. These gates serve as essential building blocks for constructing larger reversible optical arithmetic and control circuits.
- **Universal Reversible NAND–NOR Logic Gate Using Hybrid MZI–SOA and RSOA Switching:** A universal reversible logic gate capable of generating both NAND and NOR functions within a single gate structure is designed using a combined MZI–SOA and RSOA switching mechanism. Since NAND and NOR are universal Boolean functions, the proposed gate enables the realization of arbitrary Boolean logic within reversible optical computing systems.

1.6 Scope of the Work

This research focuses on the design, modelling, simulation, and evaluation of reversible arithmetic and logic circuits in both quantum and optical computing domains. The work is confined to gate-level and circuit-level reversible logic design, with particular emphasis on reversible multipliers, complex multipliers, and universal logic gates.

In the optical domain, reversible logic circuits are realized using RSOA-based switching mechanism. Optical circuit behaviour and performance are analyzed through Python-based numerical models and Opti System simulations. Key performance parameters include extinction ratio (ER), received optical power (REOP), Q-factor, optical cost, optical delay, and switching behaviour.

In the quantum domain, reversible and quantum-compatible arithmetic circuits are designed using standard reversible gate libraries. Functional validation of these designs is performed using VHDL simulations in the Vivado environment. Performance evaluation is carried out in terms of quantum cost, garbage outputs, constant inputs, and circuit complexity.

The scope of this work is limited to theoretical analysis and simulation-based validation. Practical fabrication, experimental prototyping, device-level noise modelling, and thermal characterization are beyond the present scope and are identified as potential directions for future research.

1.7 Research Methodology

The proposed research methodology follows a structured and systematic approach to the design, synthesis, simulation, and evaluation of reversible arithmetic and logic circuits in both quantum and optical domains. The methodology is organized into multiple stages to ensure correctness, scalability, and fair comparison with existing state-of-the-art designs.

1. **Gate-Level Reversible Logic Design:** Fundamental arithmetic and logic functions, including multiplication, complex multiplication, and universal logic operations, are first formulated using established reversible logic gates such as Toffoli, Fredkin, Peres, and Feynman gates. Parity-preserving reversible gates are employed where fault tolerance is required. These gate-level designs form the basis for both quantum-compatible and optical logic realizations.
2. **Optical Domain Mapping and Circuit Realization:** The reversible gate-level designs are mapped to the optical domain using RSOA-based and MZI-SOA-based switching mechanisms. RSOA-based logic is utilized to realize interferometer-free reversible gates and arithmetic circuits, while MZI-SOA-based designs are implemented to enable comparison with interferometer-based optical logic reported in the literature. Hybrid MZI-SOA and RSOA switching is employed selectively for the realization of universal reversible NAND-NOR logic gates.
3. **Optical Simulation and Performance Evaluation:** The optical circuits are simulated using Python-based numerical models and Opti-System. Key performance parameters—including extinction ratio (ER), received optical power (REOP), Q-factor, optical cost, optical delay, and switching behaviour—are evaluated to assess signal integrity, scalability, and overall optical performance.
4. **Quantum-Compatible Reversible Circuit Design and Verification:** Quantum-compatible reversible arithmetic circuits are synthesized using standard reversible gate libraries. Functional verification of these designs is performed using VHDL simulations in the Vivado environment to validate logical correctness and reversible behaviour. Performance is evaluated in terms of quantum cost, garbage outputs, constant inputs, and circuit complexity.
5. **Benchmarking and Comparative Analysis:** The proposed reversible optical and quantum designs are benchmarked against existing state-of-the-art implementations reported in the literature. Comparative evaluation is conducted to quantify improvements in hardware efficiency, optical performance, scalability, and reversibility.

1.8 Organization of the Thesis

The remainder of this thesis is organized as follows:

- **Chapter 1** introduces the background and motivation of the research, presents the problem statement, objectives, scope of the work, research methodology, and outlines the overall organization of the thesis.
- **Chapter 2** provides a comprehensive review of the literature related to reversible logic, reversible arithmetic circuits, optical computing technologies, quantum computing fundamentals, and Vedic mathematics–based multiplier designs, and identifies the key research gaps addressed in this work.
- **Chapter 3** presents the design and optimization of quantum-compatible reversible real and complex multipliers based on Vedic mathematics, along with performance evaluation in terms of quantum cost, garbage outputs, and constant inputs.
- **Chapter 4** discusses the design and simulation of an RSOA-based interferometer-free 2×2 reversible optical multiplier, including a detailed comparison with state-of-the-art designs in terms of extinction ratio, received optical power, and Q-factor.
- **Chapter 5** focuses on scalable n-bit optical multiplier designs, including an MZI–SOA-based optical multiplier developed for comparative analysis with existing interferometer-based implementations, and a fully reversible RSOA-based n-bit optical multiplier. This chapter also derives closed-form expressions for optical cost, optical delay, constant inputs, and constant outputs for the proposed RSOA-based n-bit multiplier.
- **Chapter 6** presents parity-preserving reversible optical complex multipliers, beginning with a validated 2-bit Vedic multiplier and extending to n-bit complex multipliers. This chapter also introduces a universal reversible NAND–NOR logic gate realized using a hybrid MZI–SOA and RSOA switching mechanism, enabling the synthesis of arbitrary Boolean logic.
- **Chapter 7** introduces parity-preserving RSOA-based reversible logic gates, including reversible multiplexer (MUX)-based logic gates that serve as fundamental building blocks for optical arithmetic and control circuits.
- **Chapter 8** concludes the thesis by summarizing the key findings, highlighting the major contributions, and outlining potential directions for future research.

Chapter 2: Literature Review

2.1 Introduction to Reversible Computing

Reversible computing has been extensively investigated as a promising paradigm for overcoming the fundamental energy dissipation limitations of conventional irreversible logic. Unlike irreversible circuits, in which multiple input combinations may map to the same output and lead to information loss, reversible circuits maintain a one-to-one correspondence between input and output vectors. This property enables information preservation throughout computation and forms the theoretical basis for low-power and energy-efficient computing systems.

Following the foundational work of Landauer and Bennett, reversible logic has attracted significant research interest across multiple domains, including low-power VLSI design, nanotechnology, optical computing, and quantum information processing. In particular, reversibility is an inherent requirement in quantum computing, where all operations are represented by unitary transformations. Similarly, in optical computing, reversible logic is well aligned with all-optical signal processing, where information can be preserved without frequent optical–electrical–optical conversions.

Over the years, a wide range of reversible logic gates, arithmetic circuits, and system-level designs have been proposed to reduce hardware complexity, energy dissipation, and error susceptibility. Research efforts have focused on optimizing key parameters such as quantum cost, garbage outputs, constant inputs, and scalability. Reversible adders and multipliers have received particular attention due to their central role in signal processing, communication systems, and cryptographic applications.

More recently, the scope of reversible computing has expanded beyond classical digital logic to include optical and quantum implementations. While substantial progress has been made in reversible gate synthesis and arithmetic circuit design, several challenges remain—particularly in achieving scalable, compact, and fully reversible multiplier architectures, as well as extending reversible computation to complex arithmetic and interferometer-free optical realizations.

This chapter reviews the existing literature on reversible logic gates, reversible arithmetic circuits, optical switching technologies, quantum reversible computation, and Vedic mathematics–based multiplier designs. The review highlights the strengths and limitations of prior work and identifies the research gaps that motivate the reversible optical and quantum multiplier architectures proposed in this thesis.

2.2 Reversible Logic Gates

Reversible logic gates serve as the fundamental building blocks for designing low-power, information-preserving computational systems. Unlike conventional irreversible gates, reversible gates establish a bijective (one-to-one and onto) relationship between input and output vectors. This bijection ensures that the original inputs can be uniquely reconstructed from the outputs, thereby eliminating information loss. Such a property is essential not only for achieving zero theoretical energy dissipation but also for enabling the physical realizability of quantum circuits, since all quantum transformations are inherently reversible due to their unitary nature [6-14].

A reversible logic gate is defined by two primary characteristics:

1. Equal number of inputs and outputs, and
2. Unique input-to-output mapping.

Additional parameters used to evaluate reversible gate performance include:

- **Quantum Cost (QC):** The number of primitive quantum operations required to implement the gate.
- **Garbage Outputs (GO):** Unused or auxiliary outputs necessary to preserve reversibility.
- **Constant Inputs (CI):** Inputs fixed at logic '0' or '1' to enable desired functionality.

These metrics are central to the design of efficient reversible arithmetic circuits and are independent of the underlying physical implementation. Implementation-specific performance parameters for optical realizations, such as optical cost and optical delay, are discussed in subsequent sections of this chapter.

2.2.1 Basic Reversible Gates

Basic reversible logic gates form the core building blocks for reversible arithmetic and control circuit design. These gates establish a bijective mapping between input and output vectors and are widely used in classical reversible logic synthesis as well as quantum circuit design.

The Feynman gate (CNOT) is a 2×2 reversible gate primarily used for signal replication and exclusive-OR (XOR) operations. Since direct fan-out is not permitted in reversible logic, the Feynman gate plays a crucial role in distributing signals within reversible circuits and has a quantum cost of one.

The Toffoli gate (CCNOT) is a 3×3 reversible gate that performs a controlled-controlled-NOT operation. It is a universal gate for classical reversible computation and is extensively employed in reversible arithmetic circuits such as adders and multipliers. Due to its ability to

efficiently implement conditional logic, the Toffoli gate is a fundamental component of reversible multiplier architectures.

The Peres gate (PG) is a compact 3×3 reversible gate that combines the functionality of the Feynman and Toffoli gates. Owing to its relatively low quantum cost and efficient realization of arithmetic functions, the Peres gate is widely adopted in reversible adder and multiplier designs reported in the literature.

These basic reversible gates are not inherently parity-preserving, but they provide essential functionality for constructing larger reversible arithmetic and control circuits in both quantum-compatible and optical reversible logic systems.

2.2.2 Advanced and Parity-Preserving Reversible Gates

Parity-preserving reversible logic gates maintain identical parity between their input and output vectors, making them particularly suitable for fault-tolerant and error-detectable reversible circuit design. Such gates are widely used in reversible arithmetic circuits where reliability and error detection are critical.

The Fredkin gate, also known as the Controlled-SWAP (CSWAP) gate, is a 3×3 parity-preserving reversible gate that conditionally swaps its target inputs based on the control input. Since the number of logical '1's is conserved between input and output, the Fredkin gate belongs to the class of conservative reversible logic gates. Variants of the Fredkin gate, commonly referred to as Fredkin–Rees gates (FRG), are frequently employed in reversible multiplexing, data routing, and parity-preserving arithmetic circuits.

The Feynman Double Gate (FDG) extends the functionality of the standard Feynman gate by enabling simultaneous signal replication and multiple XOR operations while maintaining parity. FDG-based designs help reduce additional gate requirements, thereby lowering garbage outputs and overall circuit complexity.

Several optimized parity-preserving reversible gates, such as the Modified IG (MIG) gate and ZPLG gate, have been proposed in the literature to minimize quantum cost and enhance fault tolerance. These gates are particularly effective in the synthesis of parity-preserving reversible adders and multipliers.

Parity-preserving reversible gates play a crucial role in the development of reliable reversible arithmetic circuits in both quantum and optical domains. Their ability to support error detection, reduce garbage outputs, and maintain reversibility makes them essential components in advanced reversible computing architectures.

2.2.3 Evaluation Metrics for Reversible Gate-Based Circuits

Reversible circuits are evaluated using a set of performance metrics that differ fundamentally from those employed in conventional irreversible logic. These metrics quantify the efficiency, scalability, and reversibility of gate-level designs and are independent of the underlying physical implementation technology.

The primary evaluation metrics used in reversible logic design include:

- **Gate Count:** The total number of reversible logic gates used to realize a circuit.
- **Quantum Cost (QC):** The number of primitive reversible or quantum operations required to implement the circuit, serving as a key indicator of resource efficiency in quantum-compatible designs.
- **Garbage Outputs (GO):** Additional outputs introduced to preserve reversibility that do not contribute to the intended computational result.
- **Constant Inputs (CI):** Input lines initialized to fixed logic values (0 or 1) to enable reversible transformations.
- **Hardware Complexity:** The total count of elementary logical operations such as XOR, AND, and NOT required to realize the reversible circuit.

These metrics form the basis for analyzing and comparing reversible logic circuits at the gate and algorithmic levels. Implementation-specific performance parameters for optical realizations—such as optical cost, optical delay, extinction ratio, and Q-factor—are dependent on the underlying device technology and are therefore discussed separately in the corresponding optical sections of this chapter.

2.2.4 Importance of Reversible Gates in This Research

The reversible logic gates reviewed in this section form the fundamental building blocks for reversible arithmetic and logic circuit design. Their characteristics—such as low quantum cost, reduced garbage outputs, and parity-preserving capability—directly influence the efficiency and scalability of reversible systems in both quantum and optical domains. These gates enable systematic synthesis of reversible adders, multipliers, and complex arithmetic circuits, and support direct mapping to optical switching elements such as RSOAs and MZI-SOAs. Consequently, careful selection and optimization of reversible gates play a critical role in achieving efficient reversible circuit implementations.

2.3 Review of Existing Reversible Arithmetic Circuits

Reversible arithmetic circuits have been extensively explored due to their relevance in low-power digital systems, nanotechnology, optical computing, and quantum information

processing. Over the years, researchers have proposed numerous reversible adders, multipliers, and arithmetic units optimized for fault tolerance, energy efficiency, and hardware scalability. This section consolidates prior research in both reversible digital and optical domains, providing a comprehensive overview of the advancements and identifying the major research gaps that motivate the present work.

2.3.1 Early Work on Fault-Tolerant Reversible Adders

The earliest systematic contributions in reversible arithmetic can be traced to the works of Islam and Begum (2008, 2009). Their research introduced the first fault-tolerant reversible carry-skip BCD adder and fault-tolerant reversible full adder, which demonstrated the feasibility of parity preservation in reversible arithmetic. These architectures ensured error-detectability but generated significant garbage outputs and constant inputs.

Subsequent improvements were proposed by Haghparast (2011), who designed a fault-tolerant reversible BCD adder; however, the design lacked support for processed fan-out, limiting scalability. Mitra and Chowdhury (2012) later introduced a minimal-cost fault-tolerant reversible full adder and Zhou et al. (2014) presented reversible BCD adders, though their architecture required a large number of gates, garbage bits, and high quantum cost, making them inefficient for quantum processors [15-19].

These initial contributions established the foundation for reversible arithmetic design but were restricted mainly to adders and small bit-width arithmetic units.

2.3.2 Evolution of Reversible Multipliers (2005–2014)

The first reversible multiplier architectures were designed by Thapliyal and Srinivas (2005), who implemented a 4×4 reversible Vedic multiplier using TG, NG, and FRG gates. In 2006, they further optimized the Vedic architecture by employing FRG gates for partial-product generation and TSG gates for full addition, resulting in improved hardware efficiency [20-22].

Growing interest in reversible multipliers led to several influential works:

- Shams et al. (2008) introduced a 4-bit multiplier using PG and MKG gates, reducing quantum cost and garbage [23].
- Akbar et al. (2011) proposed a reversible signed multiplier using Wallace-tree reduction with TG and PG gates, and an HNG-based summation network [24].
- Babazadeh and Haghparast (2012) developed a parity-preserving fault-tolerant multiplier using FRG and MIG gates [25].

- Qi et al. (2012) designed a 5-bit reversible Wallace multiplier using FRG, MNFT, F2G, and MIG gates with enhanced parity preservation [26].

These works demonstrate diverse approaches—array, Wallace-tree, and Vedic methods—yet suffer from high gate count, excessive garbage, and large circuit depth.

2.3.3 Reversible Vedic Multipliers and High-Performance Designs (2013–2017)

The integration of Vedic mathematics significantly improved the speed and regularity of reversible multipliers. Key developments include [27-35]:

- Saligram and Rakshith (2013) proposed a 4-bit parity-preserving Vedic multiplier employing PG, FG, BVPPG, and NFT gates for partial products, and HNG gates for summation.
- Haghparast and Shams (2013) introduced a nanometric parity-preserving Vedic multiplier using NFG, IG, FG, and IG-based full adders, optimized for nanoscale implementation.
- Panchal and Nayak (2014) presented a 4-bit reversible parallel multiplier using PG, TG, DPG, and PG gates, though without parity preservation.
- Srikanth et al. (2014) designed high-speed reversible Vedic multipliers and dividers using PG, FG, and FRG gates.
- Bhardwaj et al. (2014) demonstrated a reversible parallel Wallace multiplier using FRG for partial products and IG/PG for summation.
- Sahu and Sahu (2014–2015) developed scalable parity-preserving multipliers up to 64×64 bits, utilizing NFT, DFG, IG, and F2G gates.
- Valinataj (2017) designed a parity-preserving signed array multiplier using FRG, F2G, LMH gates for partial products and ZCG, F2G, ZPLG gates for summation.

Furthermore, Babu et al. (2017) introduced a reversible ALU employing a Vedic multiplier supported by TG, PG, and HNG gates.

These advancements improved scalability and fault tolerance. However, all designs are limited to real-valued multiplication, and none address complex multiplication—a critical requirement for DSP, FFT, modulation, and communication systems.

2.3.4 Reversible Multipliers for Emerging Technologies (2018–2024)

More recent research has focused on scalable and energy-efficient multiplier architectures:

- Ariaifar et al. (2019) proposed two reversible 2-bit and 4-bit Vedic multipliers, including a parity-preserving version using FRG, DFG, ZCG, PPTG, HNG, and PG gates [36-37].

- Zahra and Mosleh (2019) optimized reversible Vedic multipliers for large operand sizes [38].
- Barati (2022) introduced high-speed low-power reversible multipliers suitable for next-generation processors [39].
- Nandhini and Sambath (2023) implemented reversible multipliers in VLSI, demonstrating hardware feasibility [40].

In quantum research, Noorallahzadeh et al. (2021–2024) introduced advanced techniques for reversible multipliers using [41-45]:

- Multiple-control Toffoli gate synthesis
- Parity-preserving quantum multipliers
- Energy-efficient designs for nanoscale and IoT devices

Their recent works represent major advancements toward quantum-ready reversible multipliers but remain limited to scalar multiplication.

2.3.5 Reversible Multipliers in the Optical Computing Domain

Optical implementations of reversible logic are relatively recent. Literature includes:

- Programmable Logic Device (PLD) multipliers [46]
- Two-bit electro-optic multipliers [47]
- MZI-based reversible gates and adders, where ORG-I and ORG-II gates were introduced to realize reversible binary adders [48-49]
- MZI-based n -bit array and CSA multipliers, though suffering from high optical delay due to interferometric path imbalances [50]

Motivated by these developments, some recent works have implemented all-optical $n \times n$ Vedic multipliers using MZI-SOA structures, demonstrating various design trade-offs. However, the proposed architectures rely exclusively on MZI-SOA interferometers, which suffer from thermal instability, bulkiness, and challenges in alignment. It is important to note that several reported optical multiplier designs are not fully reversible in nature, as they rely on interferometric architectures without strict input–output bijection

Notably, no optical reversible multiplier has been reported using RSOA or interferometer-free switching mechanisms, leaving a significant gap in practical optical integration.

2.3.6 Identified Research Gaps

Based on the detailed literature survey presented above, several research gaps remain unaddressed in the domain of reversible arithmetic circuit design. To the best of the author’s knowledge, existing reversible multiplier designs are largely limited to real-valued arithmetic

and do not address complex multiplication, despite its critical importance in signal processing, communication systems, and image processing applications. Furthermore, reversible optical implementations reported in the literature predominantly rely on interferometer-based architectures, which impose limitations in terms of scalability, stability, and integration.

The major research gaps identified from the literature review are summarized as follows:

- To the best of the author's knowledge, reversible multiplier designs reported in the literature primarily support scalar (real-valued) multiplication, with no dedicated reversible architectures addressing complex-number arithmetic.
- Although Vedic multiplication techniques have been extensively employed to realize fast and regular reversible multipliers, their integration with complex arithmetic operations has not been adequately explored.
- Reversible optical multiplier implementations rely almost exclusively on MZI-SOA interferometric structures, while interferometer-free RSOA-based reversible logic realizations remain unexplored.
- Existing reversible multipliers often incur high quantum cost, excessive garbage outputs, and increased circuit depth, which limit their scalability and suitability for quantum and optical implementations.

These identified gaps collectively motivate the present research, which focuses on the development of scalable, parity-preserving, and interferometer-free reversible multiplier architectures. The work aims to advance reversible real and complex multiplier design using Vedic mathematics and optimized reversible logic, with realizations in both quantum and optical domains.

2.4 Optical Computing Fundamentals

Optical computing has emerged as a promising alternative to conventional electronic computation due to its inherent advantages in speed, bandwidth, and energy efficiency. Unlike electronic systems that rely on charge-based signal transport and are therefore subject to resistive losses and thermal constraints, optical systems manipulate photons, which propagate at the speed of light and are immune to electromagnetic interference. These characteristics make optical computing particularly attractive for high-speed communication, parallel signal processing, and energy-efficient arithmetic operations.

In optical logic systems, information can be encoded using various physical attributes of light, including intensity, phase, polarization, and wavelength. Logic operations are realized through optical nonlinearities such as cross-gain modulation (XGM), cross-phase modulation (XPM),

four-wave mixing (FWM), and gain saturation effects in semiconductor optical devices. These nonlinear phenomena enable all-optical switching, allowing logic functions to be performed without intermediate optical–electrical–optical (O–E–O) conversions, thereby reducing latency and power consumption [51-60].

Among the various platforms investigated for optical logic implementation, semiconductor optical amplifiers (SOAs) have played a central role due to their strong nonlinear response, compact size, and compatibility with photonic integrated circuits. SOA-based devices have been extensively employed to realize optical logic gates, adders, multiplexers, and arithmetic circuits. In particular, the Mach–Zehnder interferometer integrated with SOAs (MZI-SOA) has been widely reported as a versatile structure for implementing all-optical switching and logic operations, owing to its ability to exploit carrier-induced phase modulation and interference effects [61-65].

Despite their widespread use, interferometer-based optical architectures such as MZI-SOA structures exhibit several inherent limitations, including large physical footprint, sensitivity to temperature and polarization variations, stringent phase-matching requirements, and increased complexity when cascading multiple stages. These challenges pose significant constraints on the scalability and stability of large optical arithmetic circuits, especially for reversible logic applications that require strict input–output correspondence [65-70].

Beyond MZI-SOA architectures, a variety of alternative optical switching technologies have been explored in the literature, including terahertz optical asymmetric demultiplexers (TOADs), micro-ring resonators, photonic crystal devices, plasmonic logic elements, and hybrid electro-optic platforms [71-78]. While each of these approaches offers specific advantages—such as ultrafast switching or compact footprints—they also suffer from limitations related to fabrication complexity, thermal sensitivity, optical loss, synchronization requirements, or limited scalability [79-82].

Reflective Semiconductor Optical Amplifiers (RSOAs) have attracted increasing research interest as a compact and non-interferometric optical switching device. Owing to their reflective configuration and strong nonlinear behaviour, RSOAs have been widely employed in optical communication systems for signal modulation and wavelength remapping. However, their application to reversible optical logic and arithmetic circuit design has received limited attention in existing literature.

Table 2.1 summarizes the key characteristics of prominent optical switching technologies reported in the literature, highlighting their relative advantages, limitations, and integration potential. While interferometer-based devices continue to dominate optical logic

implementations, the exploration of interferometer-free optical switching mechanisms presents an important opportunity for improving scalability and robustness in optical computing systems.

Table 2.1: The key characteristics of prominent optical switching technologies

Technology	Device Type	Key Advantages	Key Limitations	Integration Potential	Typical Speed	Power Consumption	Scalability
Mach–Zehnder Interferometer (MZI)	Passive Interferometer	Simple structure, fast switching, mature	Large footprint, polarization sensitivity, complex biasing	Moderate	~ps	Low	Limited
TOAD	Nonlinear optical loop	Ultrafast response, good extinction	Requires delay lines, synchronization complexity	Low	~fs–ps	Moderate	Poor
Micro-ring Resonators	Resonant photonic device	Compact footprint, CMOS compatible	Thermal sensitivity, narrow bandwidth	High	~ps	Low	Good
Photonic Crystal-based Gates	Photonic bandgap structure	Sub-wavelength confinement, very compact	Fabrication complexity, slow tuning	Moderate	~ps–ns	Low	Moderate
Plasmonic Logic Gates	Metal-dielectric nanostructure	Ultra-compact, sub-wavelength operation	High optical loss, heat generation, poor CMOS compatibility	Low	~fs–ps	High	Poor
Hybrid Electro-optic Platforms	Silicon-organic hybrids	CMOS compatible, high-speed	Material instability, fabrication complexity	Moderate	~ps	Moderate	Moderate
RSOA-based Gates (this work)	Active optical amplifier (PI-RSOA in XGM mode)	Gain + switching, compact, low power, fast, polarization-independent	Requires bias current control	High	~ps	Very low	Excellent

In summary, optical computing provides a powerful foundation for high-speed and energy-efficient information processing. Although significant progress has been made in the development of optical logic and arithmetic circuits, existing implementations predominantly rely on interferometric structures that impose practical scalability constraints. These observations motivate further investigation into both interferometer-based and interferometer-free optical switching mechanisms for reversible logic and arithmetic circuit realization. Detailed structural and operational aspects of SOA–MZI and RSOA devices are discussed in the following sections.

2.5 Mach–Zehnder Interferometer with Semiconductor Optical Amplifiers (MZI–SOA)

The Mach–Zehnder Interferometer integrated with Semiconductor Optical Amplifiers (MZI–SOA) is a widely used platform for realizing all-optical switching and logic functions. Due to

its fast carrier dynamics, strong nonlinear response, and compatibility with photonic integrated circuits, the MZI–SOA has been extensively reported in the literature for implementing optical logic gates, multiplexers, adders, and arithmetic circuits [83-85].

2.5.1 Structural Overview

A typical MZI–SOA consists of an input coupler, two interferometer arms, and an output coupler. The input coupler splits an incoming optical signal into two coherent components that propagate through the interferometer arms. Each arm incorporates a semiconductor optical amplifier (SOA), which acts as an active nonlinear element. The output coupler recombines the optical signals from the two arms, producing two complementary outputs referred to as the bar port and the cross port.

Two optical input ports are considered:

- Port A receives the incoming or probe signal at wavelength λ_1 .
- Port B receives the control signal at wavelength λ_2 , where $\lambda_1 \neq \lambda_2$.

The wavelength separation enables nonlinear interaction inside the SOA without direct interference between the probe and control signals.

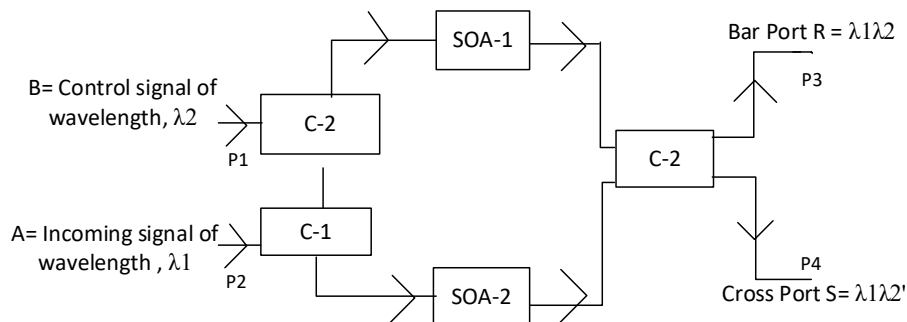


Figure 2.1: MZI-SOA switch

2.5.2 Operating Principle Based on Control–Probe Interaction

The operation of the MZI–SOA relies on carrier-induced gain saturation and refractive-index variation within the SOAs. When an optical control signal propagates through an SOA, it depletes the carrier density via stimulated emission. This carrier depletion modifies both the optical gain and the refractive index of the SOA, leading to a phase shift in the co-propagating probe signal.

The relative phase difference accumulated between the two interferometer arms determines the interference condition at the output coupler. Depending on the presence or absence of the control signal, constructive interference occurs at either the bar port or the cross port, while destructive interference occurs at the complementary port.

2.5.3 Switching Behaviour and Bar/Cross Port Outputs

In this work, the following convention is adopted, consistent with standard literature:

- Presence of optical signal $\rightarrow$ logic '1'
- Absence of optical signal $\rightarrow$ logic '0'
- P denotes the bar port output
- Q denotes the cross-port output

The switching behaviour of the MZI–SOA can be described as follows.

Case (i): Incoming signal present and control signal present ($A = 1, B = 1$)

When both the incoming signal at port A and the control signal at port B are present, the control signal induces carrier depletion in the SOA arm(s), resulting in a phase condition that favours constructive interference at the bar port. Consequently, light appears at the bar port, while the cross port remains dark.

- Bar port (P) = 1
- Cross port (Q) = 0

Case (ii): Incoming signal present and control signal absent ($A = 1, B = 0$)

In the absence of the control signal, the carrier densities in the SOAs remain unsaturated, leading to a different interference condition. In this case, constructive interference occurs at the cross port, while destructive interference occurs at the bar port.

- Bar port (P) = 0
- Cross port (Q) = 1

If the incoming signal A is absent ($A = 0$), no optical output is observed at either port, regardless of the control signal state.

2.5.4 Boolean Logic Mapping

Based on the above switching behaviour, the MZI-based all-optical switch realizes the following Boolean functions:

$$P = A \cdot B$$

$$Q = A \cdot \bar{B}$$

where:

- A represents the incoming (probe) signal,
- B represents the control signal,
- P and Q correspond to the bar and cross port outputs, respectively.

This deterministic input–output mapping enables the MZI–SOA to function as a controlled optical switch. By cascading such switches and appropriately assigning control signals, fundamental logic operations and arithmetic circuits can be synthesized.

2.5.5 Modes of Operation

MZI-SOA switches can operate in different regimes depending on the dominant nonlinear effect. In cross-phase modulation-based operation, the control signal primarily induces a phase shift in the probe signal. In gain-saturation-assisted operation, both phase and amplitude variations contribute to switching. Appropriate SOA biasing and control-signal power selection allow optimization of extinction ratio, switching speed, and crosstalk.

2.5.6 Optical Cost and Delay Model

For circuit-level analysis and comparison with existing literature, the optical cost of the MZI-based all-optical switch is considered to be unity, and the optical delay (Δ) associated with the switch is also assumed to be unity. These assumptions are commonly adopted in optical logic synthesis to simplify higher-level performance evaluation.

2.5.7 Role of MZI-SOA in the Present Research

In this thesis, MZI-SOA-based switches are employed primarily as baseline and comparative implementations. Scalable N-bit optical multipliers are designed using MZI-SOA switching to enable comparison with existing interferometer-based designs reported in the literature. These results serve as reference benchmarks for evaluating the advantages of interferometer-free, RSOA-based reversible optical circuits presented in subsequent sections

2.6 Reflective Semiconductor Optical Amplifier (RSOA):

Reflective Semiconductor Optical Amplifiers (RSOAs) are compact active photonic devices widely used in optical communication and signal processing systems. Unlike travelling-wave SOAs, an RSOA employs an asymmetric facet configuration consisting of a highly reflective (HR) coating on one facet and an anti-reflective (AR) coating on the opposite facet. This structure enables double-pass amplification and enhances nonlinear interaction within a short device length. Due to their compact footprint, polarization-insensitive operation, and strong nonlinear response, RSOAs have attracted increasing interest for all-optical switching and logic applications.

2.6.1 Structural Overview

An RSOA consists of three principal components:

- **Anti-Reflective (AR) Facet:** Allows efficient coupling of incoming optical signals into the device while minimizing unwanted reflections.
- **Active Gain Medium:** Electrically biased to maintain a high carrier density, enabling optical amplification and nonlinear interaction.

- **Highly Reflective (HR) Facet:** Reflects the optical signal back through the gain medium, resulting in double-pass propagation.

Unlike interferometer-based structures, the RSOA operates as a single-port device, where the same facet serves as both input and output. This interferometer-free configuration eliminates the need for phase matching or path-length balancing, making RSOAs inherently suitable for scalable optical circuit integration.

2.6.2 Operating Principle Based on Cross-Gain Modulation

The operation of an RSOA-based optical switch is primarily governed by cross-gain modulation (XGM). Consider two optical signals applied to the RSOA:

- Incoming (probe) signal A at wavelength λ_1
- Control signal B at wavelength λ_2 , where $\lambda_1 \neq \lambda_2$

Both signals interact within the same gain medium. When a strong control signal propagates through the RSOA, it depletes the carrier density through stimulated emission. This carrier depletion reduces the available gain experienced by the probe signal.

As a result:

- A high control signal power leads to low reflected probe power
- A low or absent control signal allows high reflected probe power

This complementary gain behaviour forms the basis of logic-level switching in RSOA-based circuits.

2.6.3 Switching Behaviour and Logic Interpretation

The switching behavior of the RSOA-based optical logic element can be described using the following convention:

- Presence of optical signal $\rightarrow$ logic '1'
- Absence of optical signal $\rightarrow$ logic '0'

Case (i): Incoming signal present and control signal absent ($A = 1, B = 0$)

When the incoming probe signal A is present and the control signal B is absent, the carrier density in the RSOA remains high. The probe signal experiences maximum gain during the double-pass propagation and is strongly reflected at the output.

- Output = 1 (high optical power)

Case (ii): Incoming signal present and control signal present ($A = 1, B = 1$)

When both the probe and control signals are present, the control signal depletes the carrier population through XGM. This reduces the gain available for the probe signal, resulting in a significantly attenuated reflected output.

- Output = 0 (low optical power)

If the incoming signal A is absent ($A = 0$), no output is observed regardless of the control signal state.

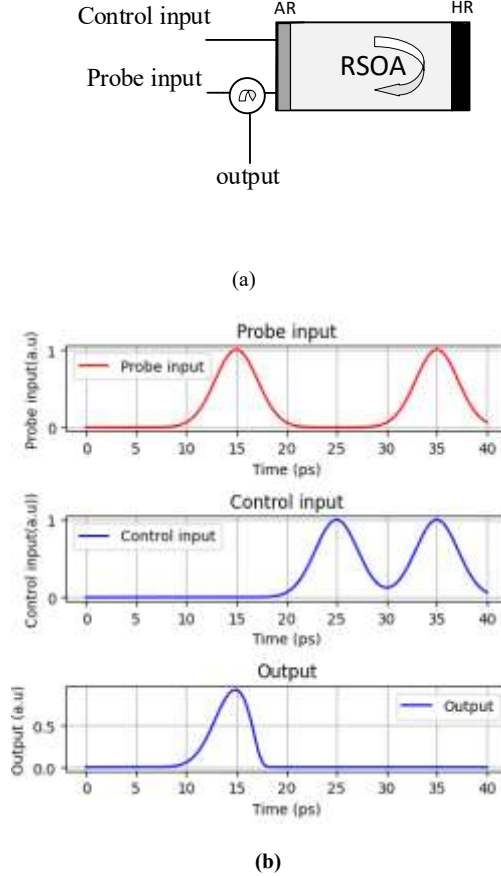


Figure 2.2: (a) Schematic diagram of the RSOA used in the switching configuration. (b) Simulated waveform showing logic levels based on control and probe signal inputs using cross-gain modulation (XGM).

2.6.4 Boolean Logic Mapping

Based on the above switching behaviour, the RSOA-based optical switch realizes the following Boolean function:

$$Y = A \cdot \bar{B}$$

where:

A is the incoming (probe) signal,

B is the control signal,

Y is the reflected output from the RSOA.

This Boolean relation shows that the RSOA inherently implements a controlled-inversion switching function. By appropriate cascading and signal routing, this primitive can be used to

construct universal logic functions such as NAND, NOR, multiplexers, and reversible logic gates.

2.6.5 Advantages of RSOA-Based Switching

RSOA-based logic offers several advantages over interferometer-based optical switches:

- Interferometer-free operation (no phase alignment required)
- Compact device footprint
- Polarization-insensitive behaviour
- Low power consumption
- High extinction ratio and contrast
- Stable cascading of multiple stages
- Suitability for dense photonic integration

These characteristics make RSOAs particularly attractive for implementing scalable and robust all-optical logic and arithmetic circuits [86].

2.6.6 Optical Cost and Delay Model

For circuit-level analysis, the optical cost of an RSOA-based switching element is considered unity, corresponding to a single active device. The optical delay is determined by the carrier recovery time and double-pass propagation, and is treated as a fixed unit delay for comparative performance evaluation in this work.

2.6.7 Role of RSOA in the Present Research

In this thesis, RSOA-based switching forms the core optical platform for implementing interferometer-free reversible logic circuits. RSOAs are employed to design reversible logic gates, universal NAND–NOR gates, multiplexing structures, and scalable optical arithmetic circuits. Their deterministic Boolean behaviour, compactness, and stable cascading capability enable the realization of energy-efficient and scalable optical computing architectures, which are evaluated and compared against interferometer-based implementations in later chapters.

2.7 Quantum Computing Background

Quantum computing represents a fundamentally new paradigm of information processing based on the principles of quantum mechanics. Unlike classical bits, which exist in a discrete state of either 0 or 1, quantum bits or qubits can exist in a linear superposition of both states simultaneously. A general qubit state is expressed as:

$$|\psi\rangle = \alpha |0\rangle + \beta |1\rangle,$$

where (α) and (β) are complex probability amplitudes satisfying $|\alpha|^2 + |\beta|^2 = 1$. This property enables quantum systems to explore multiple computational paths in parallel, providing exponential speedups for certain algorithms [88-90].

2.7.1 Multi-Qubit Systems and Entanglement

When multiple qubits are combined, their states are represented using the tensor product formalism. An (n) -qubit register spans a computational space of size 2^n , allowing highly complex correlations and computations.

A key quantum phenomenon in multi-qubit systems is entanglement, where qubit states become correlated such that the measurement of one instantaneously determines the state of another, irrespective of physical distance. Entanglement is a critical resource in quantum algorithms, cryptography, teleportation, and parallel computation.

2.7.2 Reversibility in Quantum Computation

All quantum operations are inherently reversible, represented by unitary matrices (U) satisfying:

$$U^\dagger U = I.$$

This reversible nature aligns quantum computing closely with reversible logic, making reversible circuit design fundamental for quantum architectures. Every quantum gate must preserve information, inject no energy loss due to bit erasure, and support bijective input–output mappings.

2.7.3 Quantum Reversible Gates

Quantum computation relies on a set of reversible gates that operate on one or more qubits. These gates form the building blocks for quantum logic and arithmetic circuits. Commonly used quantum reversible gates include:

- **Pauli Gates (X, Y, Z):** Single-qubit gates used for bit-flip and phase-flip operations.
- **Hadamard Gate (H):** Creates superposition states and enables quantum parallelism.
- **Phase and T Gates:** Introduce controlled phase rotations and are essential for universal quantum computation.
- **Controlled-NOT (CNOT) Gate:** A two-qubit gate that flips the target qubit when the control qubit is in state $|1\rangle$. It is the fundamental entangling gate.
- **Toffoli Gate (CCNOT):** A three-qubit gate that performs a controlled-controlled-NOT operation. It is universal for classical reversible computation and forms the backbone of quantum arithmetic circuits.

- **Fredkin Gate (CSWAP):** A parity-preserving reversible gate that conditionally swaps two qubits based on a control qubit.
- **Peres Gate (PG):** A composite reversible gate that efficiently combines CNOT and Toffoli operations, offering reduced quantum cost for arithmetic implementations.
- **V and $V^\dagger$ Gates:** Square-root-of-NOT gates used to decompose multi-controlled operations into elementary quantum gates.

These gates enable the realization of reversible arithmetic units such as adders, subtractors, and multipliers within quantum circuits [91-95].

2.7.4 Quantum Circuit Resource Metrics

Quantum reversible circuits are evaluated using a set of metrics that reflect both logical correctness and physical realizability. These parameters are essential for assessing the efficiency, scalability, and implementation feasibility of quantum arithmetic circuits.

- **Quantum Cost (QC):** The total number of elementary quantum operations required to implement a reversible circuit, serving as a measure of quantum resource consumption.
- **Garbage Outputs (GO):** Additional output qubits introduced solely to preserve reversibility. A higher number of garbage outputs increases circuit overhead and limits scalability.
- **Constant Inputs (CI):** Ancillary qubits initialized to fixed logical states ($|0\rangle$ or $|1\rangle$) to facilitate reversible computation.
- **Gate Count:** The total number of reversible gates used, providing an estimate of structural complexity.
- **Hardware Complexity (HC):** Hardware complexity provides a gate-level estimation of circuit implementation based on conventional logical operations. It is computed in terms of the number of basic logic operators required to realize the reversible circuit, expressed as:
 - $X \times \alpha$: X occurrences of 2-input XOR operations,
 - $Y \times \beta$: Y occurrences of 2-input AND operations,
 - $Z \times \delta$: Z occurrences of NOT operations.

Using these parameters, the hardware complexity is defined as:

$$HC = X\alpha + Y\beta + Z\delta,$$

where X , Y , and Z represent the total counts of XOR, AND, and NOT operations, respectively, in the circuit.

- **Total Evaluated Implementation Cost of the Reversible Circuit (TEICR):** TEICR is a composite metric used to assess the overall complexity and efficiency of a reversible circuit by collectively considering gate count (GC), constant inputs (CI), quantum cost (QC), and garbage outputs (GO). It provides a unified measure for comparative evaluation of reversible circuit implementations and is expressed as:

$$TEICR = \sum(GC, CI, QC, GO).$$

Minimizing quantum cost, garbage outputs, circuit depth, and hardware complexity is crucial for designing scalable and efficient quantum arithmetic circuits under practical hardware constraints.

2.7.5 Quantum Reversible Arithmetic Circuits

Quantum processors require reversible arithmetic circuits for applications in signal processing, cryptography, image processing, and scientific computation. As a result, significant research has focused on designing reversible adders, subtractors, and multipliers optimized for quantum environments.

Existing quantum reversible arithmetic designs include ripple-carry and carry-lookahead adders, Vedic and Wallace multipliers, and parity-preserving architectures [95-128]. However, many reported designs focus on real-valued arithmetic and often incur high quantum cost and excessive ancillary qubit usage, limiting scalability.

2.7.6 Relevance to the Present Research

A thorough understanding of quantum computation and reversible gate structures is essential for designing efficient quantum-compatible arithmetic circuits. In this thesis, reversible logic principles are employed to construct optimized quantum multipliers and complex arithmetic circuits using reversible gate libraries. The concepts introduced in this section provide the theoretical foundation for the quantum circuit synthesis, optimization, and performance evaluation presented in subsequent chapters.

2.8 Vedic Mathematics Background

Vedic Mathematics is an ancient Indian mathematical system derived from the Atharva Veda, consisting of sixteen Sutras (formulas) and thirteen Upa-sutras (sub-formulas). These sutras offer highly efficient strategies for numerical computation, especially multiplication, division, and algebraic simplification. Due to their regular structure, reduced computational complexity, and suitability for parallel implementation, Vedic mathematical techniques have been widely

adopted in modern digital arithmetic design, including reversible, optical, and quantum computing architectures [129].

Among the various sutras, the Urdhva–Tiryagbhyam (UT) Sutra—translated as “Vertically and Crosswise”—is particularly relevant for multiplier design. This sutra provides a method for computing partial products simultaneously through vertical and diagonal multiplication patterns. The algorithm naturally supports parallelism, resulting in lower latency and a regular hardware layout compared to conventional multiplication algorithms such as array, Wallace tree, or Booth multiplication.

2.8.1 Urdhva–Tiryagbhyam Sutra for Binary Multiplication

The Urdhva–Tiryagbhyam Sutra decomposes multiplication into three primary operations:

1. **Vertical products** (bit-by-bit multiplication of aligned bits)
2. **Crosswise products** (multiplication of diagonally aligned bits)
3. **Summation of partial products** in a structured and parallel manner

For two (n)-bit numbers A and B , the multiplication generates $2n - 1$ partial product terms. Unlike sequential algorithms, UT computes all these terms simultaneously, reducing overall propagation delay.

The architecture involves:

- Multiple vertical and crosswise multipliers (bitwise AND gates in binary logic)
- Adders arranged in a symmetric pattern
- Well-structured carry propagation paths

This inherent parallelism makes UT-based multipliers more efficient than traditional ripple or shift-and-add multipliers, especially for larger bit-widths.

2.8.2 Regularity and Scalability of Vedic Multipliers

A major advantage of Urdhva–Tiryagbhyam is its recursive and scalable structure. An n -bit Vedic multiplier can be constructed hierarchically using smaller Vedic blocks, for example:

- A 4×4 multiplier is built using four 2×2 Vedic multipliers
- An 8×8 multiplier is constructed from four 4×4 blocks
- This pattern continues for higher bit-widths

Such modularity greatly simplifies hardware implementation and makes UT-based multipliers highly suitable for:

- FPGA and ASIC design
- Optical logic circuits
- Quantum and reversible computing architectures

The regularity also reduces wiring complexity, routing overhead, and delay variation across the circuit.

2.8.3 Relevance to Reversible and Quantum Arithmetic Circuits

Vedic multipliers have gained significant attention in reversible and quantum computing due to:

(i) **Reduced Circuit Depth**

The parallel computation pattern minimizes sequential dependencies, lowering circuit depth—an essential requirement for quantum circuits with limited coherence time.

(ii) **Lower Garbage Outputs (GO) and Constant Inputs (CI)**

Compared to array and Wallace-tree designs, Vedic structures require fewer intermediate registers, allowing more efficient reversible circuit synthesis.

(iii) **Modular Reversible Implementation**

Hierarchical construction maps naturally to reversible building blocks such as Peres, Toffoli, Fredkin, and HNG gates.

(iv) **Compatibility with Optical Logic**

The partial-product generation and summation network can be realized using XGM-based and MZI-based switching elements, making UT widely applicable in optical reversible designs as well.

(v) **Support for Complex Multiplication**

The symmetric multiplication pattern allows easy extension to complex arithmetic by generating both real and imaginary partial products.

2.8.4 Why Vedic Multiplication Is Used in This Research

The motivation for incorporating the Urdhva–Tiryagbhyam Sutra in this thesis stems from its suitability for efficient reversible arithmetic design:

- It reduces optical cost, circuit depth, and gate count.
- When combined with optimized reversible gates, UT-based architectures can reduce ancillary bits, lowering overall reversible overhead.
- It is highly adaptable to RSOA-based and MZI-SOA-based optical circuits.
- It supports quantum circuit optimization by minimizing multi-controlled gate operations.
- It enables high-speed operation due to its inherently parallel structure.

These characteristics make UT-based multiplication particularly suitable for reversible arithmetic circuit design, motivating its use in the architectures presented in subsequent chapters.

2.9 Summary and Research Gaps

This chapter presented a comprehensive review of the theoretical foundations and prior research relevant to reversible logic, optical computing technologies, quantum computation, and Vedic mathematical approaches for arithmetic circuit design. The discussion began with an overview of reversible computing principles, emphasizing the importance of information preservation, energy efficiency, and bijective input–output mapping. Fundamental reversible logic gates and their evaluation metrics were reviewed to establish a basis for reversible circuit synthesis.

The literature survey highlighted significant progress in reversible arithmetic circuit design, particularly in the development of reversible adders, multipliers, and fault-tolerant architectures. Vedic multiplication techniques, especially the Urdhva–Tiryagbhyam Sutra, were identified as effective approaches for achieving parallelism, regularity, and scalability in multiplier architectures. These characteristics make Vedic multipliers attractive for implementation in reversible, optical, and quantum computing environments.

From an optical computing perspective, various all-optical switching technologies were examined, including MZI-SOA interferometers, TOADs, micro-ring resonators, photonic crystal devices, plasmonic structures, and hybrid electro-optic platforms. Among these, MZI-SOA-based architectures have dominated optical logic and arithmetic implementations reported in the literature. However, interferometer-based designs suffer from inherent limitations such as large physical footprint, thermal and polarization sensitivity, phase-matching constraints, and reduced scalability when multiple stages are cascaded. In contrast, Reflective Semiconductor Optical Amplifiers (RSOAs) offer compact, interferometer-free operation with strong nonlinear characteristics, yet their application to reversible optical logic and arithmetic circuits remains largely unexplored.

In the quantum domain, reversible logic forms the foundation of all quantum computation due to the unitary nature of quantum operations. Existing research has produced a wide range of reversible arithmetic circuits using Toffoli, Fredkin, Peres, and related gates. However, most reported quantum arithmetic designs focus on real-valued operations and often incur high quantum cost, excessive garbage outputs, and increased circuit depth, limiting their scalability on near-term quantum hardware.

Based on the critical analysis of the literature, several key research gaps are identified. Reversible multiplier architectures reported to date are predominantly limited to scalar arithmetic, with no dedicated focus on complex multiplication despite its importance in signal processing and communication systems. The integration of Vedic multiplication techniques with complex arithmetic in reversible logic has not been adequately explored. In the optical domain, reversible implementations rely almost exclusively on interferometer-based switching, while interferometer-free RSOA-based reversible logic circuits are absent from existing studies. Furthermore, resource-efficient reversible designs that simultaneously address quantum cost, garbage outputs, circuit depth, and hardware complexity remain limited. These observations indicate a clear need for scalable, low-overhead, and interferometer-free reversible arithmetic architectures in both quantum and optical domains. The subsequent chapters address these challenges by presenting optimized reversible multiplier and complex multiplier designs using Vedic mathematics and reversible logic principles, with implementations and comparative evaluations in quantum and all-optical platforms.

Chapter 3: Quantum Reversible Vedic Multiplier

3.1. Introduction

Efficient multiplier architectures play a central role in modern computational systems, particularly in applications such as digital signal processing, image reconstruction, wireless communication, and scientific computing. Complex multiplication, in particular, is a computationally intensive operation required in algorithms such as FFT, DFT, modulation schemes, and numerical solvers. As device technologies move toward nanometer-scale and quantum-compatible platforms, there is a growing need for arithmetic circuits that are not only fast and modular but also minimize resource overhead and information loss.

Reversible logic provides a natural framework for achieving such objectives, as it enables computation without losing input information, thereby supporting low-power operation and compatibility with quantum hardware. While several reversible arithmetic circuits have been proposed in the literature, most existing multipliers focus on real-valued operations or rely on architectures with high garbage outputs, excessive ancilla inputs, and elevated quantum cost. Moreover, reversible complex multipliers—essential components for quantum signal processing—have received limited attention, and existing designs do not fully exploit algorithmic optimizations such as those offered by Vedic mathematics.

The Urdhva–Tiryagbhyam (UT) Sutra from Vedic mathematics provides a highly parallelizable multiplication strategy that naturally suits reversible logic due to its regular structure, balanced dataflow, and modular decomposition. Leveraging these features, this chapter introduces a quantum-ready reversible architecture for a 4×4 -bit complex Vedic multiplier. The design employs a hierarchy of reversible modules, including a 4×4 Vedic multiplier, reversible carry-save adders, a ripple-carry adder, and an 8-bit unified adder–subtractor. These modules are constructed using optimized reversible gates such as Peres, HNG, and Feynman gates to minimize quantum cost, garbage generation, and ancilla requirements.

A detailed investigation of previous work forms the basis for identifying specific gaps: reversible complex multipliers remain scarce, most reported designs are not optimized for quantum cost, and none exploit the bidirectional or modular capabilities of Vedic multiplication within a reversible framework. The proposed architecture addresses these challenges by offering two variants of the reversible 4×4 Vedic multiplier (VM1 and VM2) and integrating them into a complete reversible complex multiplier (CVM1 and CVM2). This modularity allows systematic scalability to higher bit-width operations.

The designs are evaluated using widely accepted reversible design metrics—gate count, ancilla inputs/constant input, garbage outputs, quantum cost, hardware complexity, and TEICR. Entropy-based validation is additionally employed to confirm information preservation, reinforcing the reversible nature of the proposed circuits. Functional validation is carried out using Xilinx Vivado on the Artix-7 FPGA platform, ensuring correct logical behavior even though FPGA devices are inherently irreversible.

Overall, this chapter presents the complete design flow, analysis, and performance comparison of the proposed reversible multipliers, demonstrating its advantages over existing reversible multipliers and establishing its suitability for future quantum and low-power computing architectures.

3.2 Reversible Gates Utilized in the Proposed Architecture

The proposed 4×4-bit reversible Vedic multiplier and the associated complex multiplier architecture are realized using a carefully selected set of reversible and quantum-compatible logic gates. These gates serve as the fundamental computational primitives for constructing reversible arithmetic units while ensuring bijective input–output mapping, minimal information loss, and compatibility with quantum circuit synthesis.

The selection of gates is guided by three primary criteria:

- (i) suitability for arithmetic operations such as partial product generation and addition,
- (ii) low quantum cost and reduced hardware complexity, and
- (iii) efficient support for signal duplication and routing under reversible logic constraints.

The reversible gates employed in this work include the Feynman gate (FG), Toffoli gate (TG), Feynman Double Gate (F2G), Peres gate (PG), and Haghparast–Navi gate (HNG). Together, these gates enable the modular construction of reversible adders, carry-save adders, ripple-carry adders, unified adder–subtractors, and multiplier blocks used throughout the proposed architecture.

3.2.1 Feynman Gate (FG)

The Feynman Gate, also widely recognized as the Controlled-NOT (CNOT) Gate, is one of the simplest reversible logic gates. It operates on two inputs A, B and produces two outputs P, Q as:

$$P=A, Q=A\oplus B$$

In the proposed architecture, the FG is used exclusively for signal duplication and control preparation, enabling fan-out without violating reversibility.

- Quantum Cost (QC): 1
- Hardware Complexity (HC): 1α (one XOR operation)



Figure 3.1: (a) Schematic depiction of the FG gate; (b) The quantum structure of the FG gate

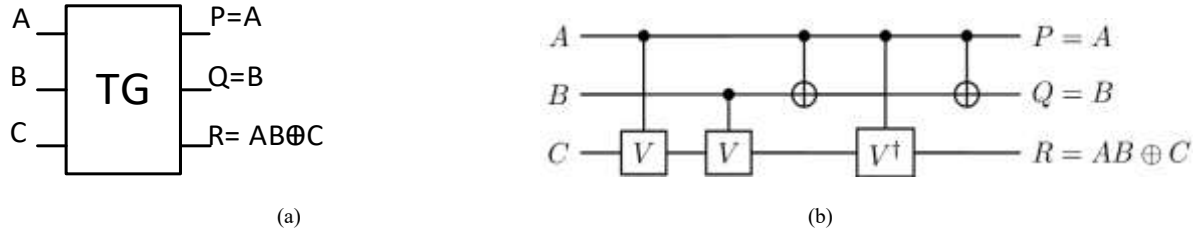


Figure 3.2: (a) TG gate schematic diagram; (b) The quantum framework of the TG gate

3.2.2 Toffoli Gate (TG)

The Toffoli Gate, also known as the Controlled-Controlled NOT (CCNOT) gate, is a fundamental 3×3 reversible logic gate that operates on inputs A, B, and C, producing outputs $P = A$, $Q = B$, and $R = (A \cdot B) \oplus C$. It provides controlled AND functionality and forms the basis for partial product generation in reversible multipliers.

- **Quantum Cost (QC):** 5
- **Hardware Complexity (HC):** $1\alpha + 1\beta$ (one XOR and one AND).

Representation:

- Figure 3.2(a): Block diagram of the Toffoli Gate.
- Figure 3.2(b): Quantum realization using a network of controlled gates implementing the CCNOT operation.

3.2.3 Feynman Double Gate (F2G/DFG)

The Feynman Double Gate (F2G), also known as the Double Feynman Gate (DFG), is a 3×3 reversible gate that extends the functionality of the basic Feynman gate to allow multiple signal duplications. It operates on three inputs A, B, C and produces three outputs P, Q, R as:

$$P=A, Q=A \oplus B, R=A \oplus C$$

- **Quantum Cost (QC):** 2
- **Hardware Complexity (HC):** 2α



Figure 3.3: (a) Schematic diagram of DFG gate; (b) The quantum logic synthesis of the DFG gate

3.2.4 Peres Gate (PG)

The Peres gate is a 3×3 reversible gate defined by $P = A$, $Q = A \oplus B$, $R = (A \cdot B) \oplus C$. When $C = 0$, the gate functions as a reversible half adder, making it highly efficient for arithmetic operations.

- Quantum Cost (QC): 4
- Hardware Complexity (HC): $2\alpha + 1\beta$

The PG gate is extensively used for partial product accumulation and intermediate addition stages in the proposed Vedic multiplier.

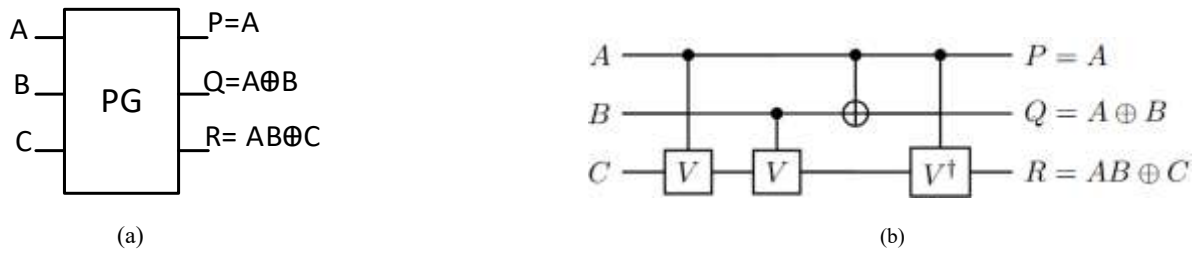


Figure 3.4: (a) PG gate schematic diagram; (b) Quantum gate modelling of the PG gate

3.2.5 Fredkin Gate (FRG)

The Fredkin Gate (FRG) is a 3×3 reversible and bidirectional quantum gate that can simultaneously function as a controlled swap gate and a multiplexer. It takes three inputs A, B, C and produces three outputs P, Q, R, where:

$$P=A, Q=A'B \oplus AC, R=A'C \oplus AB$$

Here, the control input A determines whether the target inputs B and C are swapped.

- If $A=0$, the outputs remain unchanged ($Q=B$, $R=C$).
- If $A=1$, the gate swaps the target signals ($Q=C$, $R=B$).

It performs a controlled swap operation and functions as a reversible multiplexer. Due to its parity-preserving nature, the FRG is particularly suitable for fault-tolerant signal routing and selection.

- Quantum Cost (QC): 5

- Hardware Complexity (HC): $2\alpha + 4\beta + 2\delta$ (two XOR, four AND, and two NOT operations)

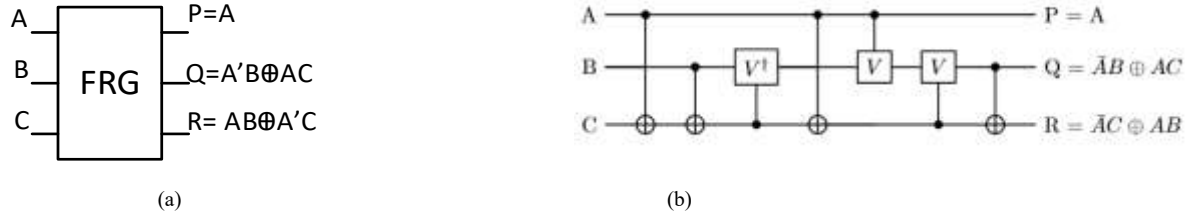


Figure 3.5: (a) Structural configuration of the FRG gate; (b) The quantum framework of FRG gate

3.2.6 Haghparast–Navi Gate (HNG)

The Haghparast–Navi gate is a 4×4 reversible gate designed specifically for arithmetic operations. It produces sum and carry outputs in a single structure and functions as a reversible full adder when the fourth input is set to zero.

The HNG gate is used to implement reversible full adders in carry-save adders, ripple-carry adders, and unified adder–subtractor blocks.

- Quantum Cost (QC): 6
- Hardware Complexity (HC): $5\alpha + 2\beta$

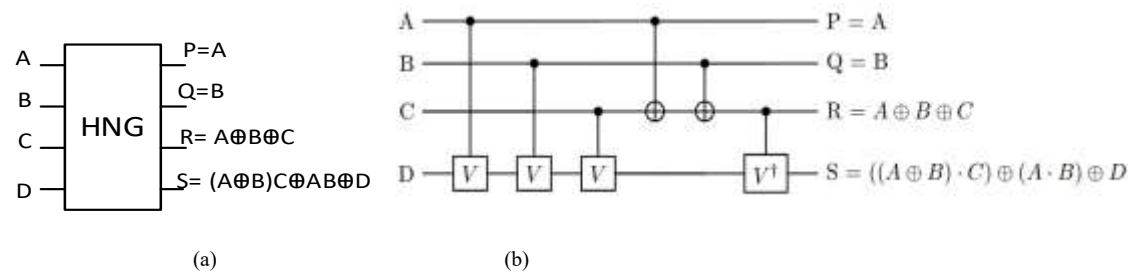


Figure 3.6: (a) Schematic layout of HNG gate; (b) The quantum gate representation of HNG gate

3.3 Urdhva–Tiryagbhyam Algorithm

The proposed reversible complex multiplier is based on the Urdhva–Tiryagbhyam (Vertical & Crosswise) Sutra, one of the sixteen fundamental techniques of Vedic mathematics. This Sutra provides a generalized multiplication theorem applicable to numbers of any size.

Unlike conventional shift-and-add multiplication, Urdhva–Tiryagbhyam (UT) performs partial product generation and addition in parallel, significantly reducing computational latency and making it highly suitable for hardware implementations, especially in low-power, quantum-compatible architectures.

Mathematical Formulation of the UT Algorithm for Binary Multiplication

Let two n -bit binary numbers A and B be represented as:

$A = A_{n-1}A_{n-2} \dots \dots A_1A_0$ and $B = B_{n-1}B_{n-2} \dots \dots B_1B_0$

where each bit $A_i, B_i \in \{0,1\}$

Multiplication of these numbers produces a $2n$ -bit binary product:

$$P = P_{2n-1}P_{2n-2} \dots \dots P_1P_0$$

Each product bit is computed as:

$$P_k = \sum_{i=0}^k A_i B_{k-i} + \text{carry for } 0 \leq k \leq 2n - 2$$

and the most significant product bit is:

$$P_{2n-1} = A_{n-1}B_{n-1}$$

The most significant product bit is obtained from the final carry and the highest-order partial product. This parallel generation of partial products avoids long carry-propagation chains, thus improving speed and energy efficiency.

Partitioning for Scalable Implementation

For practical hardware realization, the given n -bit numbers are partitioned to simplify computation.

1. Rounding to the nearest power of two:

$$k = \lceil \log_2(n) \rceil$$

$$N_{\text{new}} = 2^k$$

Example: For $n=7$,

$$k = \lceil \log_2(7) \rceil = \lceil 2.81 \rceil = 3$$

$$n_{\text{new}} = 2^3 = 8$$

2. Splitting into halves:

$$A = (A_L, A_H), B = (B_L, B_H)$$

where A_H, B_H are the higher $\left\lceil \frac{n}{2} \right\rceil$ -bit segments (MSB), and A_L, B_L are the lower $\left\lceil \frac{n}{2} \right\rceil$ -bit segments (LSB).

Partial Product Computation

Using this partitioning, the UT algorithm computes four intermediate products:

Vertical Multiplications: $P_0 = A_L \times B_L$; $P_3 = A_H \times B_H$

Cross Multiplications: $P_1 = (A_H \times B_L)$; $P_2 = (A_L \times B_H)$

Finally, the complete product is obtained as:

$$P = \sum \left[(P_3 \ll n), \left([P_1 + P_2] \ll \left(\frac{n}{2} \right) \right), P_0 \right], \text{ where “}\ll\text{” denotes left-bit shifting.}$$

Advantages of UT Algorithm

- **Parallelism:** Simultaneous generation of partial products and their summation.
- **Reduced latency:** Eliminates the need for sequential addition stages.
- **Hardware efficiency:** Suitable for modular and scalable hardware designs.
- **Energy saving:** Lower switching activity reduces power consumption.

This makes the UT Sutra ideal for high-performance computing, digital signal processing, cryptographic circuits, and quantum-compatible reversible multipliers [32].

3.4 Reversible Complex Vedic Multiplier

Complex multiplication forms the backbone of numerous digital signal processing (DSP) applications, including Fast Fourier Transform (FFT), Discrete Fourier Transform (DFT), modulation techniques, and image filtering. In mathematics and engineering, complex numbers are indispensable for solving polynomial equations lacking real solutions, modelling electromagnetic waves, and analyzing oscillatory systems.

In conventional hardware, complex multiplication is realized through a combination of real multiplications and add/subtract operations, which increases computational latency and energy consumption. To improve parallel processing capability and energy efficiency, researchers have investigated the use of Vedic multiplication algorithms in reversible circuits, when combined with optimized reversible gate structures, Vedic multiplication enables reduced garbage output and improved resource efficiency.

Mathematical Model of Complex Multiplication

Let two complex numbers be expressed as:

$Z_1 = a_{\text{real}} + ja_{\text{imaginary}}$ and $Z_2 = b_{\text{real}} + jb_{\text{imaginary}}$, where a_{real} , b_{real} are the real components and $a_{\text{imaginary}}$, $b_{\text{imaginary}}$ are the imaginary components.

The complex product Z_1 and Z_2 is given by:

$$Z_{\text{real}} = (a_{\text{real}} \cdot b_{\text{real}} - a_{\text{imaginary}} \cdot b_{\text{imaginary}}) \quad \text{Equation 3.1 ,}$$

$$Z_{\text{imaginary}} = (a_{\text{real}} \cdot b_{\text{imaginary}} + a_{\text{imaginary}} \cdot b_{\text{real}}) \quad \text{Equation 3.2}$$

Thus, four independent multiplications of the real and imaginary parts are required, followed by one addition and one subtraction to compute the final real and imaginary outputs.

Hardware Requirements for n-bit Complex Multiplication

For two n -bit complex numbers, the computation in Equation (3.1, 3.2) necessitates:

- **Four $n \times n$ -bit multipliers** (for partial products),
- **One $2n$ -bit adder** (for $a_{\text{real}} \cdot b_{\text{imaginary}} + a_{\text{imaginary}} \cdot b_{\text{real}}$), and
- **One $2n$ -bit subtractor** (for $a_{\text{real}} \cdot b_{\text{real}} - a_{\text{imaginary}} \cdot b_{\text{imaginary}}$)

This modular structure allows the design to scale efficiently for larger bit-widths. Figure 3.7 illustrates the modular architecture of an $n \times n$ -bit reversible complex Vedic multiplier, where each block corresponds to a reusable reversible arithmetic circuit.

Unsigned Data Representation for Simplified Design

The proposed architecture is optimized for unsigned magnitude representation, treating both the real and imaginary components as positive integers. This approach eliminates the overhead of signed arithmetic, such as:

- Sign extension,
- Handling of two's complement representation,
- Additional logic for overflow detection.

Instead, the design ensures controlled carry propagation and precise bit-shifting for all intermediate partial products, guaranteeing that no overflow occurs during the computation.

By restricting the computation to unsigned data, the architecture achieves simpler control logic, reduced quantum cost, and lower garbage output, making it well-suited for reversible logic implementations. Although the internal arithmetic treats operands as unsigned magnitudes for simplicity, subtraction results are represented in two's complement form when required, ensuring correct arithmetic behaviour without additional sign-handling logic.

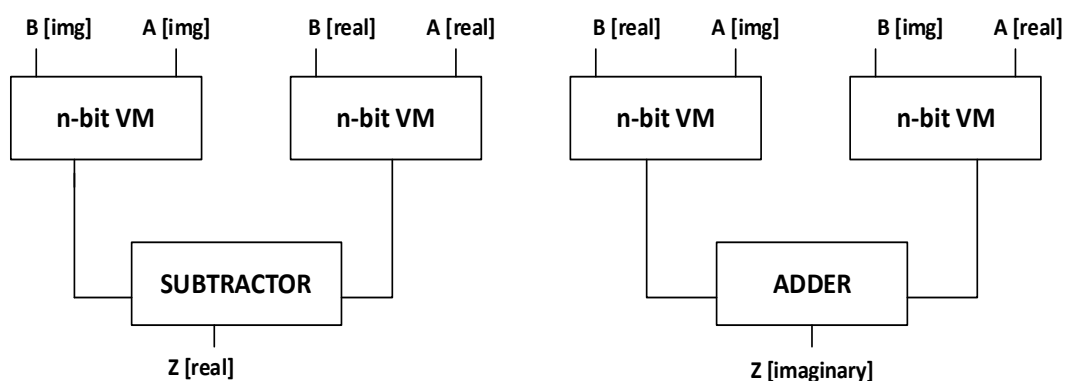


Figure 3.7: Modular designs of Complex Multiplier

Integration with Reversible Vedic Multiplier Units

Each required $n \times n$ -bit multiplication in Equation (3.1, 3.2) are realized using the Urdhva–Tiryagbhyam Vedic multiplier, which inherently supports parallel partial product generation. The intermediate results are then processed by reversible adders and subtractors, all constructed using optimized gate libraries such as PG and HNG gates.

This hierarchical composition of multipliers, adders, and subtractors forms the reversible complex Vedic multiplier, which exhibits:

- High modularity for scalable bit-widths,
- Lower ancilla input and garbage output,
- Improved energy efficiency compared to conventional irreversible implementations.

The detailed gate-level design and analysis of each multiplier block, unified adder–subtractor, and carry-save adder variants are presented in the subsequent sections.

3.4.1 4×4-bit Reversible Vedic Multiplier

The Urdhva–Tiryagbhyam (UT) algorithm for binary multiplication is inherently hierarchical. To compute an $n \times n$ -bit product, the algorithm recursively decomposes the operation into:

- Four $\left(\left\lceil \frac{n}{2} \right\rceil \times \left\lceil \frac{n}{2} \right\rceil\right)$ -bit multipliers for generating partial products, and
- Three n -bit adders for summing intermediate results.

Thus, implementing a 4×4-bit Vedic multiplier requires:

- Four 2×2-bit reversible Vedic multipliers,
- One 4-bit carry-save adder (CSA) to efficiently add lower and intermediate partial products $[P_0]$ and $[(P_1+P_2) \ll 2]$, and
- One 4-bit ripple carry adder (RCA) to add the higher-order partial product $[P_3 \ll 4]$.

This modular design reduces the critical path delay, minimizes garbage outputs, and ensures logical reversibility, making it suitable for quantum-ready arithmetic circuits.

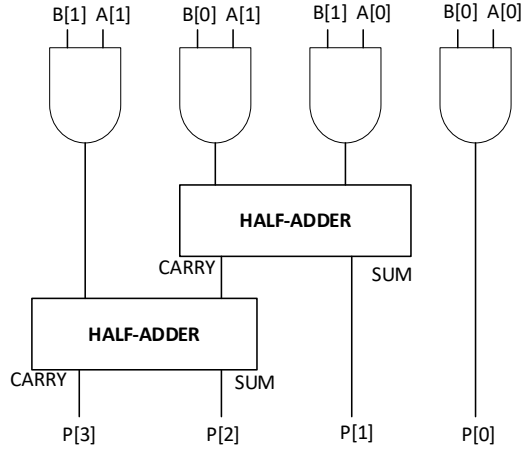
(a) 2×2-bit Reversible Vedic Multiplier

The 2×2-bit Vedic multiplier is the fundamental building block for higher-order multipliers. It operates on two 2-bit inputs and produces a 4-bit output using the UT algorithm with vertical and crosswise partial products.

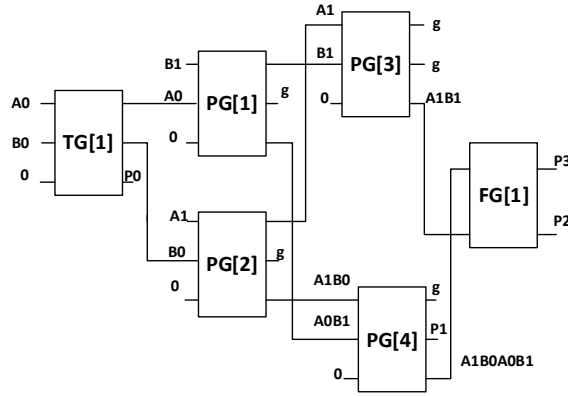
- Gate-level Implementation:
 - 1 Toffoli Gate (TG) for AND operations,
 - 1 Feynman Gate (FG) for XOR propagation, and
 - 4 Peres Gates (PG) for partial product accumulation.
- Performance Parameters:
 - Ancilla inputs: 5

- Garbage outputs: 5
- Quantum cost (QC): 22
- Hardware complexity (HC): $10\alpha+5\beta$

The structural schematic of the 2×2 -bit Vedic multiplier is shown in Figure 3.8(a), while its optimized hardware architecture is illustrated in Figure 3.8(b).



(a)



(b)

Figure 3.8: (a) 2×2 -bit multiplier: Gate-level circuit diagram, and (b) Hardware architecture for 2×2 -bit Vedic multiplier

(iii) 4-bit Carry-Save Adder (CSA)

A Carry-Save Adder (CSA) is an optimized arithmetic unit designed for multi-operand addition, which is a critical step in multiplication and other complex arithmetic operations. Unlike conventional adders, which propagate carry bits immediately at each stage, the CSA defers carry propagation, thereby allowing parallel computation of partial sums and carries. The final result requires a second stage—usually a Ripple Carry Adder (RCA)—to combine the saved carries with the partial sum. This reduces the overall critical path delay, making CSA highly effective for multi-operand summation in:

- Multiplication circuits

- Digital signal processing (DSP)
- Cryptographic and modular arithmetic

Modular CSA Designs for UT-Based Multiplication

In this work, two modular 4-bit CSA architectures are developed for summing lower and intermediate partial products generated during the Urdhva-Tiryagbhyam (UT) multiplication:

1. Conventional 4-bit CSA Design:

- The first stage consists of four reversible full adders, enabling parallel addition of P_0 and $(P_1 + P_2) \ll 2$.
- The second stage performs final summation using a 4-bit RCA.

2. Modified 4-bit CSA Design:

- The lower [2]-bits (LSB) are computed using full adders, while the upper [2]-bits (MSB) are computed using half adders, reducing quantum cost and hardware complexity.
- The second stage again uses a 4-bit RCA for final addition.

Both designs are illustrated in Figure 3.9, highlighting their structural differences and gate-level implementations.

Reversible Gate Composition:

The CSA is implemented using HNG and PG reversible logic gates:

- HNG gate $\rightarrow$ acts as a full adder (producing both sum and carry outputs).
- PG gate $\rightarrow$ acts as a half adder (producing a partial sum and carry).

Performance Metrics of 4-bit CSA:

The conventional 4-bit CSA (as shown in Figure 3.9(a)) comprises:

- 6 HNG gates (full adders: $R = \text{sum}$, $S = \text{carry}$)
- 1 PG gate (half adder: $Q = \text{sum}$, $R = \text{carry}$)

Its reversible computation metrics are:

- Ancilla inputs: 9
- Garbage outputs: 14
- Quantum cost (QC): 40
- Hardware complexity (HC): $32\alpha + 13\beta$

The modified 4-bit CSA, depicted in Figure 3.9(b), further optimizes the design by reducing unnecessary full adder stages, achieving lower QC and garbage output, making it more hardware-efficient for higher-order multipliers. The circuit has 7 ancilla inputs and 12 garbage

outputs. The quantum cost of the modified 4-bit CSA is 36, and the hardware complexity is $26\alpha + 11\beta$.

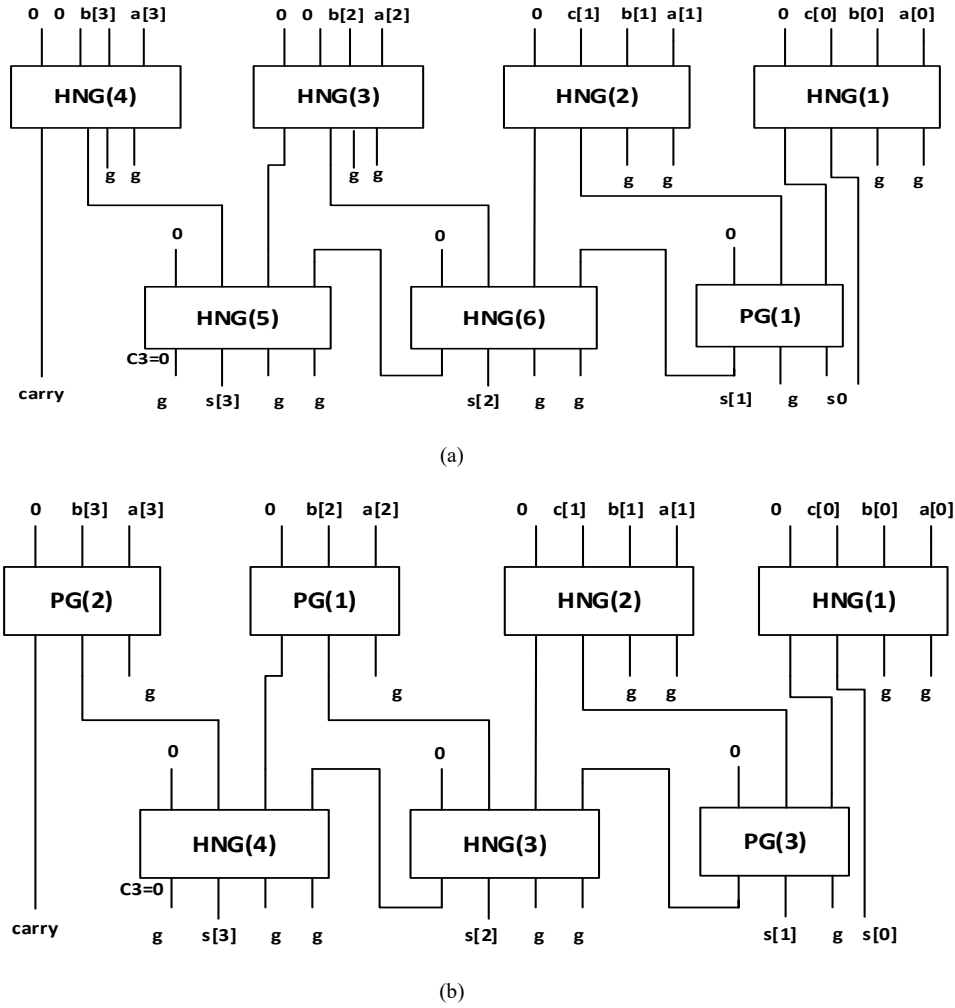


Figure 3.9: (a) Hardware implementation of 4-bit CSA, (b) Hardware implementation of modified 4-bit CSA.

*(c1 c0 = P0[3:2]; a[3:0] = P1[3:0] A_LB_H; b[3:0] = P2[3:0] A_HB)

(iv) 4-bit Ripple Carry Adder (RCA)

The Ripple Carry Adder (RCA) is one of the most fundamental reversible arithmetic units used for binary addition. It consists of a cascade of full adders, where the carry output of each stage serves as the carry input for the next stage, hence the term “ripple carry.”

Although the RCA is simple in design, the carry propagation introduces a linear delay proportional to the number of bits, making it slower than advanced adder architectures for large operand sizes. However, for small-bit-width designs, such as the 4-bit RCA, it offers a minimal and efficient structure that is highly suitable for modular arithmetic circuits like the proposed 4×4-bit Vedic multiplier.

The 4-bit RCA presented in this work (illustrated in Figure 3.10(a)) is implemented using:

- Three HNG gates → acting as full adders (producing both sum and carry outputs).

- One PG gate $\rightarrow$ acting as a half adder for the least significant bit (LSB) addition.

This combination ensures a fully reversible structure with no loss of information, making it suitable for quantum and low-power computing platforms.

Performance Metrics of 4-bit RCA:

For the 4-bit RCA, the reversible computation parameters are:

- Ancilla inputs: 5
- Garbage outputs: 8
- Quantum cost (QC): 22
- Hardware complexity (HC): $17\alpha + 7\beta$

Thus, the RCA provides a compact, low-overhead solution for final carry-propagation stages in modular reversible arithmetic circuits.

With both the Carry Save Adder (CSA) and the Ripple Carry Adder (RCA) in place, the 4×4 -bit Vedic multiplier achieves optimized partial product summation, minimizing delay, garbage outputs, and quantum cost [130].

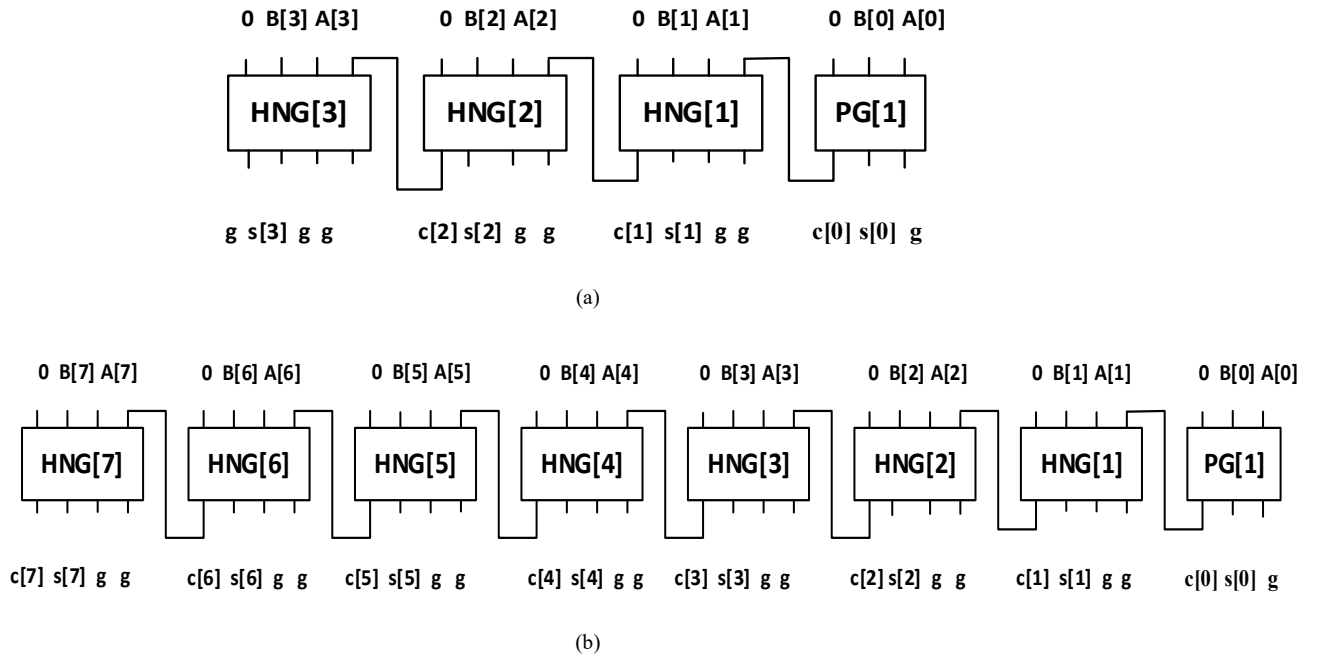


Figure 3.10: (a) Hardware implementation of 4-bit RCA*, and (b) Hardware architecture for 8-bit RCA.

* $(a[3:0] = [0, \text{carry}, s3, s2]; b[3:0] = P3[3:0])$

(v) Architecture of 4×4 -bit Vedic Multiplier

The 4×4 -bit Vedic multiplier is implemented using the Urdhva-Tiryakbhyam (UT) Sutra, which efficiently generates partial products and enables parallel summation to minimize delay.

Its internal architecture integrates:

- Four 2×2-bit Vedic multipliers for generating the lower, intermediate, and higher partial products.

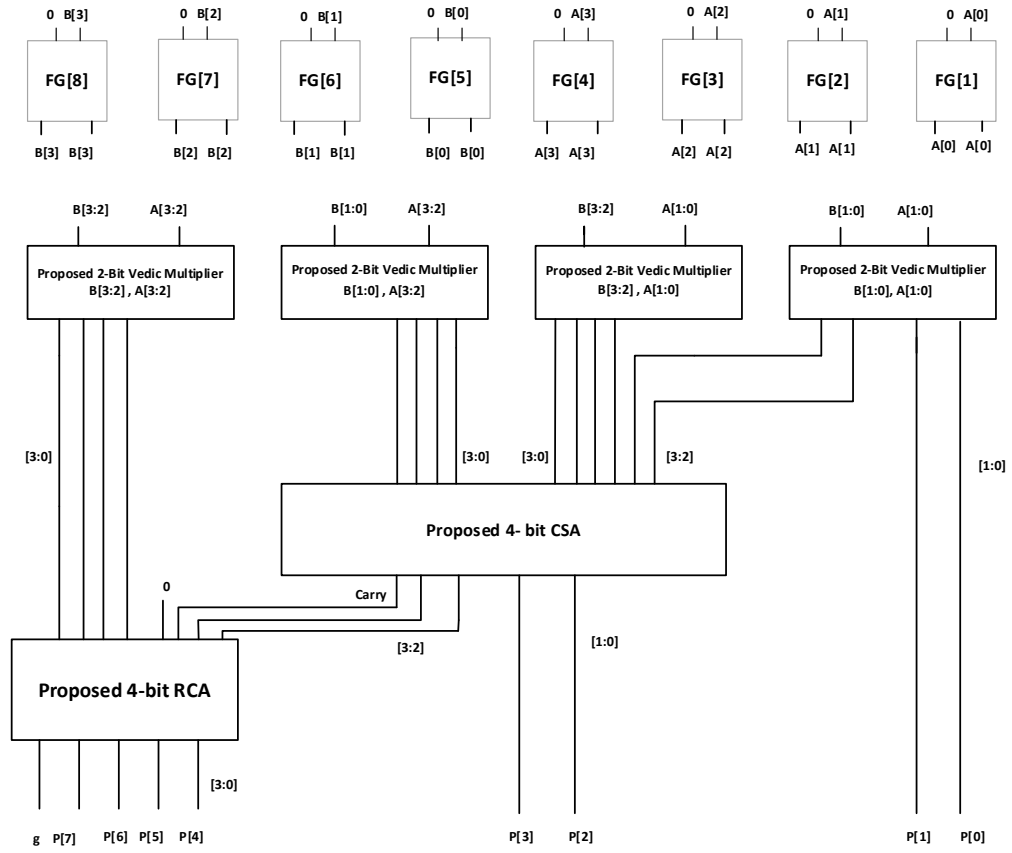


Figure 3.11: Hardware implementation of proposed 4x4-bit Vedic multiplier

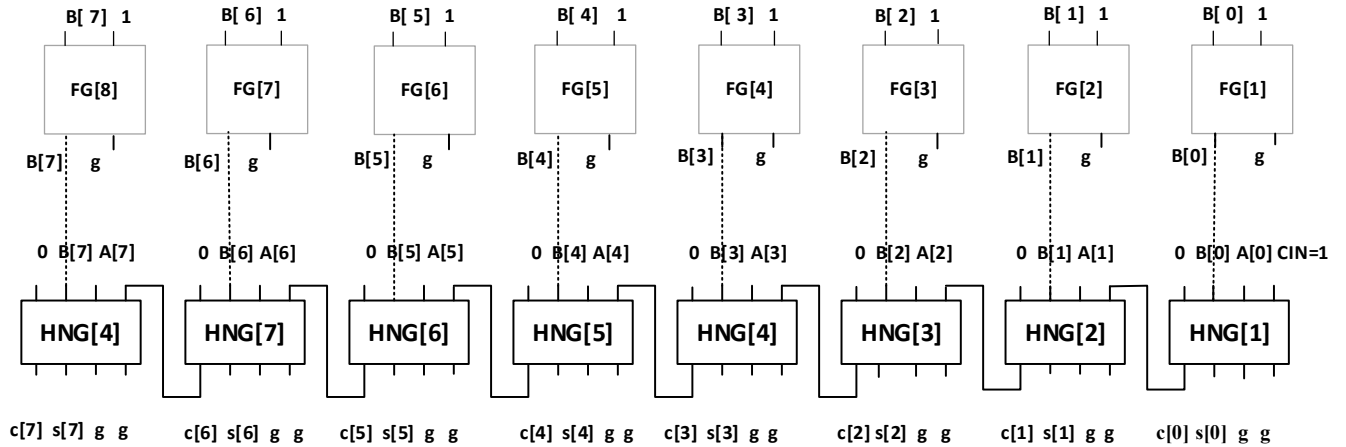


Figure 3.12: Hardware implementation of an 8-bit Unified Adder-Subtractor

- One 4-bit Carry Save Adder (CSA) for fast addition of the lower and intermediate partial products.
- One 4-bit Ripple Carry Adder (RCA) for final carry propagation and summation.

This modular approach supports optimized resource utilization, improving quantum cost (QC), ancilla inputs (CI), garbage outputs (GO), and hardware complexity (HC) compared to conventional ripple structures.

Two Modular Designs for the 4×4-bit Vedic Multiplier

Two variants of the 4×4-bit reversible Vedic multiplier were developed to analyze trade-offs between performance metrics:

Design 1 (VM1): Standard CSA-Based Architecture

- Utilizes the standard 4-bit CSA for intermediate summation.
- Performance metrics are calculated as:

$$QC (VM1)_{4 \times 4\text{-bit}} = 8QC_{FG} + 4QC_{2\text{-bit VM}} + QC_{4\text{-bit CSA}} + QC_{4\text{-bit RCA}} = 158$$

$$CI (VM1)_{4 \times 4\text{-bit}} = 8CI_{FG} + 4CI_{2\text{-bit VM}} + CI_{4\text{-bit CSA}} + CI_{4\text{-bit RCA}} = 42$$

$$GO (VM1)_{4 \times 4\text{-bit}} = 4GO_{2\text{-bit VM}} + GO_{4\text{-bit CSA}} + GO_{4\text{-bit RCA}} = 42$$

$$HC (VM1)_{4 \times 4\text{-bit}} = 8HC_{FG} + 4HC_{2\text{-bit VM}} + HC_{4\text{-bit CSA}} + HC_{4\text{-bit RCA}} = 97\alpha + 40\beta$$

This configuration prioritizes structural simplicity, making it highly suitable for modular integration in larger reversible multiplier architectures.

Design 2 (VM2): Modified CSA-Based Architecture

- Replaces the standard CSA with a modified CSA that uses mixed full-adder and half-adder stages, reducing quantum overhead and garbage generation.
- Performance metrics are calculated as:

$$QC (VM2)_{4 \times 4\text{-bit}} = 8QC_{FG} + 4QC_{2\text{-bit VM}} + QC_{4\text{-bit CSA}_{MODIFIED}} + QC_{4\text{-bit RCA}} = 154$$

$$CI (VM2)_{4 \times 4\text{-bit}} = 8CI_{FG} + 4CI_{2\text{-bit VM}} + CI_{4\text{-bit CSA}_{MODIFIED}} + CI_{4\text{-bit RCA}} = 40$$

$$GO (VM2)_{4 \times 4\text{-bit}} = 4GO_{2\text{-bit VM}} + GO_{4\text{-bit CSA}_{MODIFIED}} + GO_{4\text{-bit RCA}} = 40$$

$$HC (VM2)_{4 \times 4\text{-bit}} = 8HC_{FG} + 4HC_{2\text{-bit VM}} + HC_{4\text{-bit CSA}_{MODIFIED}} + HC_{4\text{-bit RCA}} = 91\alpha + 38\beta.$$

This variant reduces QC, CI, and GO while maintaining functional correctness, making it more optimized for quantum-ready implementations.

Comparative Analysis

From the above metrics:

- VM2 outperforms VM1 by achieving lower QC (154 vs. 158), reduced garbage outputs (40 vs. 42), and less hardware complexity ($91\alpha + 38\beta$ vs. $97\alpha + 40\beta$).

- Both designs maintain the same logical functionality, but VM2 is more resource-efficient, especially for quantum-compatible environments.

Thus, VM2 is the preferred design choice for implementing scalable, low-garbage, and energy-efficient reversible multipliers.

3.4.2 8-bit Unified Adder-Subtractor (UAS)

In the proposed architecture, the subtraction operation is performed using the two's complement technique, represented mathematically as:

$$A - B = A + (\text{Two's complement of } B)$$

Since the data representation is unsigned, the following conditions apply:

- If $A < B$, the result is negative and expressed in two's complement form, with the MSB carry-out (C_n) = 0, indicating a borrow.
- If $A \geq B$, no borrow occurs, and the MSB carry-out (C_n) = 1. In this case, the extra carry is discarded.

As shown in Figure 3.12, the 8-bit reversible Unified Adder-Subtractor (UAS) is implemented using:

- 8 Feynman gates (FG) for signal duplication and conditional bit inversion.
- 8 HNG gates acting as full adders for parallel addition/subtraction.

The UAS behaves as a subtractor when the FG gates are set with inputs $A = 1$ and the HNG gate's initial carry-in $C_0 = 1$. Otherwise, the circuit functions as a standard 8-bit reversible ripple carry adder.

Performance metrics:

- Ancilla inputs (CI): 17
- Garbage outputs (GO): 24
- Quantum cost (QC): 56
- Hardware complexity (HC): $48\alpha + 16\beta$

This unified approach eliminates the need for separate hardware for addition and subtraction, thereby reducing circuit complexity and resource overhead.

3.4.3 8-bit Ripple Carry Adder (RCA)

To compute the imaginary part of the complex multiplication,

$Z_{\text{imaginary}} = (a_{\text{real}} \cdot b_{\text{imaginary}} + a_{\text{imaginary}} \cdot b_{\text{real}})$, an 8-bit Ripple Carry Adder (RCA) is utilized to sum the two 8-bit partial products.

The reversible RCA is implemented using:

- 1 Peres Gate (PG) functioning as a half adder for the least significant bit (LSB) addition.
- 7 HNG gates functioning as full adders for the remaining bits.

The circuit is shown in Figure 3.10(b) and achieves the following metrics:

- Ancilla inputs (CI): 8
- Garbage outputs (GO): 15
- Quantum cost (QC): 46
- Hardware complexity (HC): $37\alpha + 15\beta$

This RCA architecture is chosen for its low hardware complexity and predictable propagation delay, which is acceptable for an 8-bit addition stage within the complex multiplier.

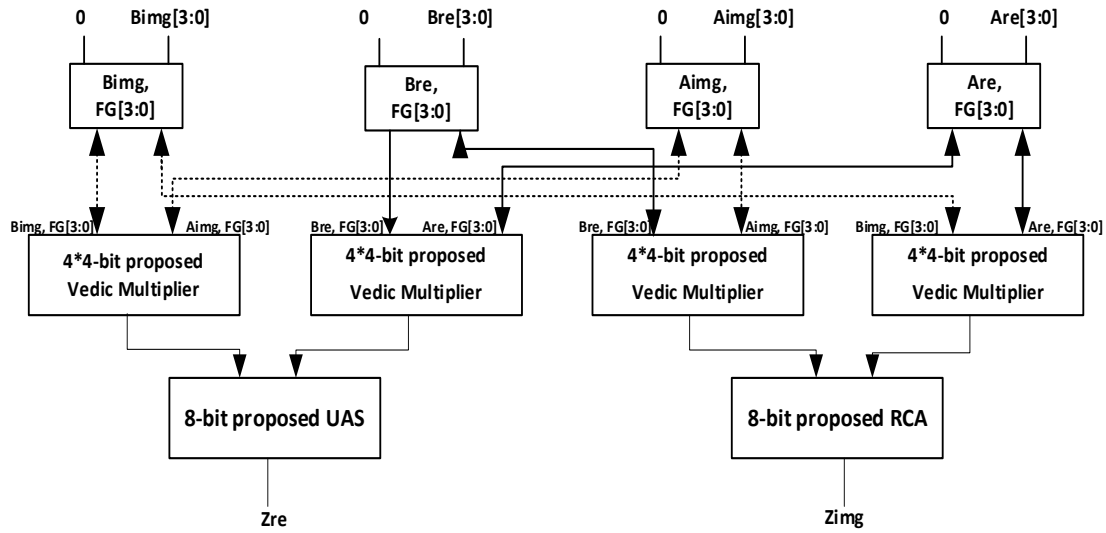


Figure 3.13: Hardware implementation of proposed 4x4-bit Complex Vedic multiplier

3.5 Architecture of 4×4-bit Complex Vedic Multiplier

The 4×4-bit Complex Vedic Multiplier is constructed using the modular building blocks discussed in the previous sections. Specifically, it integrates:

- Four 4×4-bit Vedic multipliers (either VM1 or VM2 depending on the chosen design) corresponding to the four real multiplications required in complex arithmetic,
- One 8-bit Unified Adder-Subtractor (UAS) for performing addition/subtraction of real partial products, and
- One 8-bit Ripple Carry Adder (RCA) for computing the imaginary partial products.

These modules collectively realize the complex multiplication defined in Equation (3.1 & 3.2). Since complex multiplication requires four independent Vedic multiplications along with two arithmetic stages (one addition and one subtraction), the performance metrics of the complete complex multiplier can be derived from the cumulative contributions of its submodules.

Design 1: 4×4-bit Complex Vedic Multiplier (CVM1)

In CVM1, the 4-bit Vedic multiplier module VM1 (using standard CSA design) is utilized. The cumulative performance parameters are:

- $QC(CVM1)_{4 \times 4\text{-bit}} = 16QC_{FG} + 4QC_{4\text{-bit VM1}} + QC_{8\text{-bit UAS}} + QC_{8\text{-bit RCA}} = 750$
- $CI(CVM1)_{4 \times 4\text{-bit}} = 16CI_{FG} + 4CI_{4\text{-bit VM1}} + CI_{8\text{-bit UAS}} + CI_{8\text{-bit RCA}} = 209$
- $GO(CVM1)_{4 \times 4\text{-bit}} = 4GO_{4\text{-bit VM1}} + GO_{8\text{-bit UAS}} + GO_{8\text{-bit RCA}} = 207$
- $HC(CVM1)_{4 \times 4\text{-bit}} = 16HC_{FG} + 4HC_{4\text{-bit VM1}} + HC_{8\text{-bit UAS}} + HC_{8\text{-bit RCA}} = 489\alpha + 191\beta$

This design is structured to prioritize modularity and is based on the standard CSA-based VM1, which introduces slightly higher quantum cost but ensures balanced hardware complexity.

Design 2: 4×4-bit Complex Vedic Multiplier (CVM2)

In CVM2, the optimized VM2 module is used, which employs a modified CSA architecture with reduced garbage outputs and ancilla lines. The resulting performance parameters are:

- $QC(CVM2)_{4 \times 4\text{-bit}} = 16QC_{FG} + 4QC_{4\text{-bit VM2}} + QC_{8\text{-bit UAS}} + QC_{8\text{-bit RCA}} = 734$
- $CI(CVM2)_{4 \times 4\text{-bit}} = 16CI_{FG} + 4CI_{4\text{-bit VM2}} + CI_{8\text{-bit UAS}} + CI_{8\text{-bit RCA}} = 201$
- $GO(CVM2)_{4 \times 4\text{-bit}} = 4GO_{4\text{-bit VM2}} + GO_{8\text{-bit UAS}} + GO_{8\text{-bit RCA}} = 199$
- $HC(CVM2)_{4 \times 4\text{-bit}} = 16HC_{FG} + 4HC_{4\text{-bit VM2}} + HC_{8\text{-bit UAS}} + HC_{8\text{-bit RCA}} = 465\alpha + 183\beta$

Compared to CVM1, this design achieves:

- Reduced quantum cost (QC)
- Lower ancilla inputs (CI) and garbage outputs (GO)
- Slightly reduced hardware complexity (HC)

This makes CVM2 more resource-efficient and suitable for scalable quantum-ready implementations.

Comparative Insight

The difference between CVM1 and CVM2 lies primarily in the type of CSA used in the 4×4 Vedic multiplier module, which directly impacts garbage outputs and ancillary requirements.

- CVM1 offers a baseline implementation, whereas
- CVM2 improves efficiency through a modified CSA approach, making it the preferred choice for low-power and resource-constrained environments.

3.6. Results and Discussion

This section presents a comprehensive evaluation of the proposed reversible arithmetic architectures, including the 4×4-bit Vedic multiplier (VM1 and VM2) and the 4×4-bit Complex

Vedic Multiplier (CVM1 and CVM2). The analysis encompasses theoretical performance, comparative benchmarking with existing reversible designs, HDL-based simulation, and entropy-based validation to assess the information-preserving nature of the circuits. Together, these results demonstrate the efficiency, scalability, and reversibility of the proposed quantum-compatible architectures.

3.6.1 Comparative Analysis with Existing Designs

Table 3.1 provides a detailed comparison of the proposed Vedic multipliers with existing reversible architectures reported in the literature. The comparison focuses on dominant parameters governing reversible design efficiency—namely garbage outputs (GO), ancilla inputs (CI), gate count (GC), quantum cost (QC), hardware complexity (HC) and total Evaluated Implementation Cost of the Reversible Circuit (TEICR).

The analysis highlights several key observations:

- VM2 achieves the lowest QC and GO among all compared designs, attributed to its optimized modified CSA.
- VM1 provides a balanced trade-off between hardware complexity and reversibility metrics but incurs slightly higher QC and GO than VM2.
- The proposed designs outperform many earlier works, where architectures often suffer from excessive garbage generation or high quantum overhead due to unoptimized partial product addition stages.

Figure 3.14 graphically illustrates the performance enhancement achieved by the proposed multipliers, confirming the suitability of VM2 for scalable reversible arithmetic applications. Overall, the comparative study validates that the architectural refinements introduced in VM2 lead to substantially improved resource efficiency without compromising functional correctness.

3.6.2 Performance Assessment of the Proposed Complex Multipliers

The cumulative performance of the complete 4×4-bit complex Vedic multipliers (CVM1 and CVM2) is summarized in Table 3.2. Since complex multiplication requires four Vedic multipliers along with additional add/subtract stages, the efficiency of the underlying 4-bit multiplier directly influences the total resource footprint.

Key findings include:

- CVM2 demonstrates a significant reduction in QC, CI, and GO compared to CVM1, reflecting the advantage of using the optimized VM2 module.
- Hardware complexity is consistently lower in CVM2, with reductions in both XOR (α) and AND (β) counts, indicating a more compact and energy-efficient structure.

- The improvements achieved at the submodule level propagate to the complex multiplier, evidencing the scalability of the modular Vedic architecture.

These results confirm that optimizing the partial-product addition stage at lower bit-widths leads to measurable benefits in higher-level composite designs

3.6.3 FPGA-Based Functional Verification

To validate logical correctness, both complex multiplier designs were implemented in Verilog HDL and synthesized using Xilinx Vivado 2019.2 targeting an Artix-7 FPGA. Figure 3.15 shows the RTL schematic of the proposed architecture, comprising interconnected 4×4 multipliers, an 8-bit Unified Adder–Subtractor (UAS), and an 8-bit Ripple Carry Adder (RCA). Simulation waveforms (Figure 3.16-3.17) confirm:

- Correct computation of both real and imaginary components
- Preservation of bijective input–output mapping
- Absence of undefined or redundant signals
- Functional consistency across all test vectors

Although FPGA platforms cannot measure quantum-specific metrics such as QC or ancilla usage, the hardware simulation ensures that the reversible logic behavior is functionally correct and suitable for modular expansion.

3.6.4 Entropy-Based Validation of Logical Reversibility

To quantify the information-preserving nature of the proposed designs, an entropy evaluation was conducted using Shannon’s information theory. For reversible systems, the input entropy $H(X)$ must equal the output entropy $H(Y)$, ensuring no information loss.

For an n -bit reversible system with equally probable inputs:

$$H(X) = H(Y) = n \text{ bits}$$

Example:

A 2-bit reversible gate has 4 input states, each with probability 0.25:

$$H(X) = -\sum 0.25 \log_2 0.25 = 2 \text{ bits}$$

Since each output maps uniquely back to an input:

$$H(Y) = 2 \text{ bits}$$

Table 3.3 contrasts the entropy behaviour of reversible and irreversible gates:

- Irreversible gates (AND, OR, XOR) exhibit entropy reduction due to state merging, violating reversibility and incurring energy dissipation as per Landauer’s limit.

- Reversible gates preserve entropy, implying theoretically zero information loss and minimal energy dissipation.

For the proposed multipliers, all evaluated modules satisfied:

$$H(X) = H(Y)$$

confirming full logical reversibility.

3.6.5 Energy Dissipation Estimation

While physical hardware implementation is not part of this work, theoretical energy dissipation can be estimated. The hardware complexity of CVM1 is:

$$HC = 489\alpha + 191\beta$$

If implemented using irreversible gates, the estimated minimum energy dissipation would be:

$$E_{\text{irrev}} \approx (489 + 191) k_B \ln 2$$

This equates to approximately:

$$680 k_B \ln 2 \approx 1.7544 \times 10^{-18} \text{ J}$$

In contrast, a logically reversible implementation theoretically avoids energy dissipation due to information erasure, although physical non-idealities may still contribute to practical energy loss.

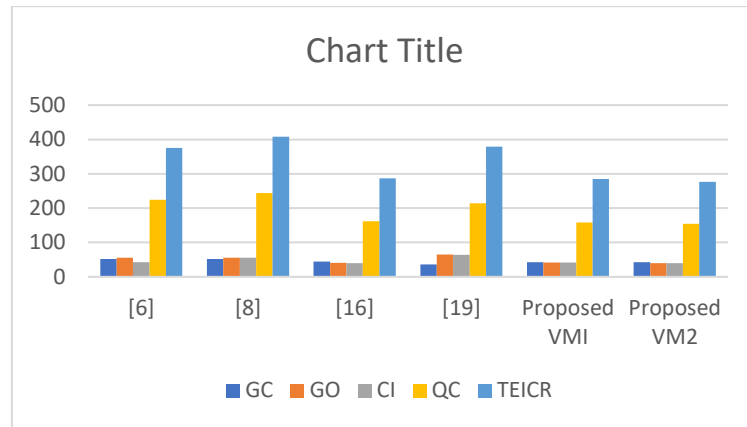


Figure 3.14: Graphical analysis of the presented 4×4-bit Vedic multiplier with previously reported studies in the literature.

3.6.6 Overall Discussion

The key insights from the presented evaluations are:

1. **Resource Efficiency:** CVM2 consistently reduces QC, GO, CI, and hardware complexity compared to CVM1, achieving a 10–15% improvement.
2. **Scalability:** The modular UT-based structure allows straightforward extension to higher bit-width multipliers.

3. **Energy Advantages:** The reversible design paradigm ensures minimal logical entropy loss, making the architecture suitable for quantum processors, nanotechnologies, and energy-limited systems.
4. **Practical Feasibility:** FPGA-based simulations verify correctness and confirm that the architecture can be synthesized using standard hardware description flows.

Overall, the proposed reversible Vedic multiplier architectures offer a high-performance, energy-efficient, and quantum-ready solution compared to existing reversible designs.

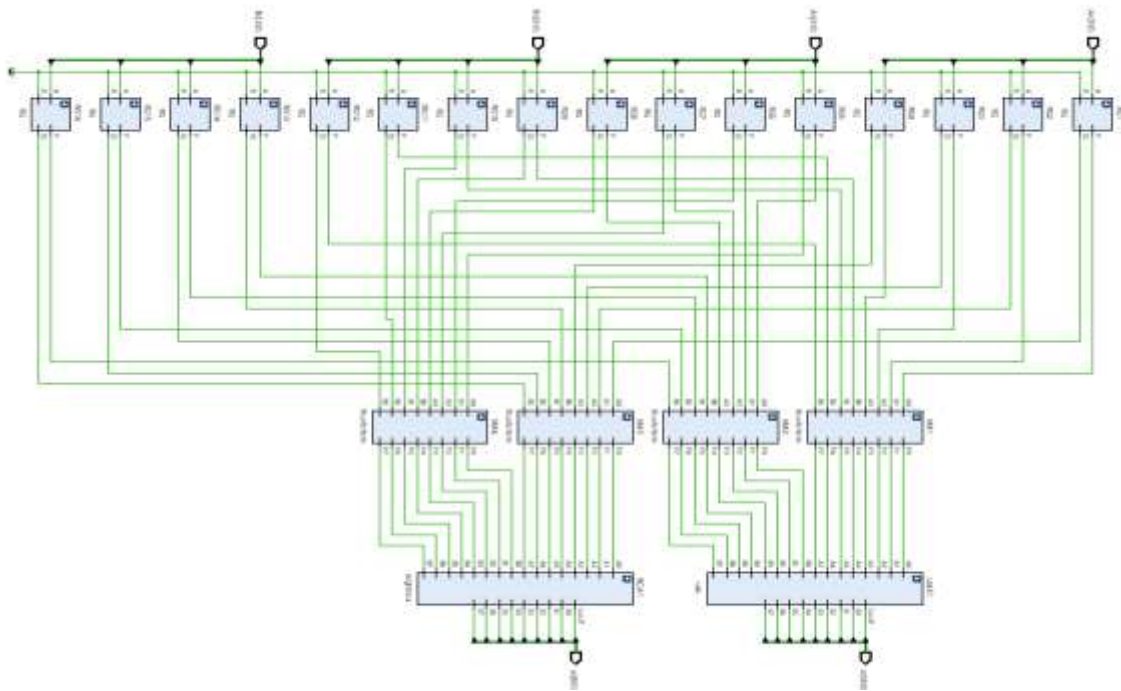


Figure 3.15: RTL view of 4×4 Complex Vedic Multiplier

Table 3.1: Comparison results of 4×4-bit Vedic multiplier

Design	GC	GO	CI	QC	TEICR	HC
Thapliyal. [20]	52	56	43	224	375	$92\alpha + 100\beta + 68\gamma$
Shams. [23]	52	56	56	244	408	$116\alpha + 52\beta + 36\gamma$
Zahra. [38]	44	41	40	162	287	$99\alpha + 41\beta$
Barati. [39]	36	65	64	214	379	$156\alpha + 94\beta + 35\gamma$
Proposed VMI	43	42	42	158	285	$97\alpha + 40\beta$
Proposed VM2	43	40	40	154	277	$91\alpha + 38\beta$

Table 3.2: Comparison results of proposed 4×4-bit Complex Vedic multiplier

Design	GC	CI	GO	QC	TEICR	HC
Complex Vedic multiplier (CVM1)	212	209	207	750	1378	$489\alpha + 191\beta$
Complex Vedic multiplier (CVM2)	212	201	199	734	1346	$465\alpha + 183\beta$

Table 3.3: Entropy Analysis of Irreversible vs Reversible Logic Gates

Logic Gate	Approach	H(X)	H(Y)	Entropy Loss (ΔH)
AND	Irreversible	2 bits	~ 0.811	1.189 bits
	Reversible	3 bits	3 bits	0 bit
XOR	Irreversible	2 bits	1 bit	1 bit
	Reversible	2 bits	2 bits	0 bit

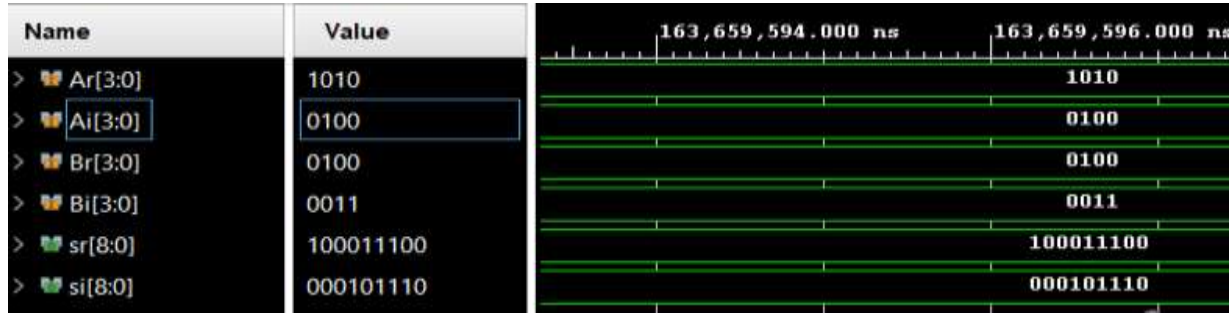


Figure 3.16: Simulation result of 4×4 Complex Vedic Multiplier (CVM1), where, $a = (1010 + j 0100)$ and $b = (0100 + i 0011)$. The output $Z_{re} = 1 00011100$ and $Z_{im} = 000101110$

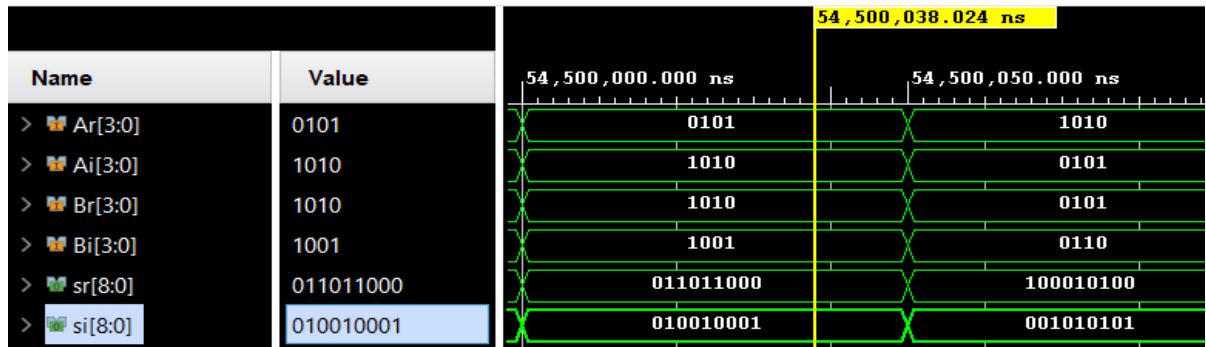


Figure 3.17: Simulation result of 4×4 Complex Vedic Multiplier (CVM2) where, $a = (0101 + j 1010)$ and $b = (1010 + i 1001)$. The output $Z_{re} = 0 11011000$ (2's complement) and $Z_{im} = 0 10010001$.

3.7 Summary

This chapter presented the complete design, modular realization, and performance evaluation of a reversible 4×4 -bit Complex Vedic Multiplier tailored for quantum-compatible and energy-efficient arithmetic computation. Building upon the reversible gate structures and Vedic multiplication framework introduced earlier, two variants of the 4×4 Vedic multiplier (VM1 and VM2) were developed, along with supporting reversible modules such as the 4-bit Carry-Save Adder, 4-bit Ripple Carry Adder, and the 8-bit Unified Adder–Subtractor.

The proposed architectures exploit the inherent parallelism of the Urdhva–Tiryagbhyam (UT) Sutra and utilize optimized reversible gate libraries—including Feynman, Toffoli, Peres, and HNG gates—to minimize quantum cost, garbage outputs, and constant inputs. The modular design methodology demonstrated how improvements at the sub-block level directly enhance

the overall complex multiplier. In particular, VM2, based on a modified CSA structure, achieved superior efficiency, offering lower QC, CI, GO, and hardware complexity compared to VM1 and previously reported reversible multipliers in the literature.

FPGA-based verification on the Xilinx Artix-7 platform confirmed the functional correctness of the proposed designs, validating the seamless integration of reversible modules within a hardware description environment. Although FPGA tools cannot evaluate true quantum parameters, they effectively verified bijective input-output behaviour and modular interconnections. Additionally, entropy-based analysis showed perfect preservation of Shannon information entropy $H(X) = H(Y)$, confirming logical reversibility and indicating zero information loss, in accordance with Landauer's principle.

Overall, the results demonstrate that the proposed complex Vedic multiplier architectures offer significant improvements in resource efficiency, modular scalability, and energy-awareness. These advantages make the designs well suited for integration into future quantum processors, nanophotonic arithmetic systems, low-power DSP architectures, and emerging reversible computing frameworks. The core contributions presented in this chapter have been peer-reviewed and published in the Journal of Computational Electronics (Springer), an SCIE-indexed journal. This publication validates the novelty, correctness, and research significance of the reversible arithmetic architectures developed in this chapter. The next chapter extends this work by transitioning from quantum-domain reversible logic to all-optical reversible arithmetic, beginning with the design of a compact RSOA-based 2×2 -bit multiplier.

Chapter 4: RSOA-based All-Optical 2×2-Bit Reversible Multiplier

4.1 Introduction

Multiplication is a core arithmetic operation in digital and photonic computing systems, forming the basis of numerous applications such as digital signal processing, image and video analysis, cryptographic primitives, wireless communication, and high-speed computation. As system complexity continues to grow, the demand for ultrafast, energy-efficient, and compact multiplier architectures has intensified. Conventional electronic multipliers suffer from limitations related to resistive losses, heat generation, and RC-related delays, making them unsuitable for emerging high-speed and low-power platforms.

All-optical computing has emerged as a promising alternative due to its inherent advantages—including picosecond-level switching speed, immunity to electromagnetic interference, high bandwidth, and low transmission loss. By relying entirely on photons for computation, optical systems significantly reduce capacitive loading and thermal dissipation typically associated with electronic circuits. Integrating reversible logic principles into optical designs further enhances energy efficiency by ensuring bijective input–output mappings, thereby avoiding information loss and adhering to Landauer’s principle.

This chapter presents the design and simulation of a 2×2-bit all-optical reversible multiplier constructed using RSOA-based Feynman (FG) and RSOA-based Peres (PG) gates. The Reflective Semiconductor Optical Amplifier (RSOA), operated in cross-gain modulation (XGM) mode, serves as the fundamental switching element enabling reversible XOR and AND operations required for multiplication. Unlike interferometer-based optical architectures such as MZI–SOA, RSOA-based gates do not rely on phase-sensitive interferometric paths, making them inherently more compact and less sensitive to alignment and thermal drift.

The proposed 2×2-bit reversible multiplier follows a modular structure comprising:

1. Reversible fan-out generation using FG gates
2. Partial product computation using PG gates
3. Reversible addition of partial products
4. Final product synthesis through shift-and-add logic

The optical design is evaluated using two key performance metrics:

- **Optical Cost (OC):** Total number of RSOA switching elements
- **Optical Delay (OD):** Number of cascaded RSOAs in the critical path

Additionally, signal integrity parameters—including Extinction Ratio (ER), Q-factor, and Relative Eye Opening (REOP)—are analyzed under varying RSOA injection currents to characterize the switching performance.

Simulation results confirm the correct operation of the reversible optical multiplier across all input combinations and reveal excellent optical performance characteristics suitable for high-speed photonic processors. The compactness and modularity of the design make it suitable as a foundational building block for larger reversible optical arithmetic circuits, as explored in subsequent chapters.

4.2 Theoretical Background

This section outlines the fundamental concepts supporting the design of the proposed all-optical reversible multiplier. It covers the principles of reversible optical logic, the operational characteristics of Reflective Semiconductor Optical Amplifiers (RSOAs), and the mechanism of cross-gain modulation (XGM) that enables reversible logic operations in the photonic domain.

4.2.1 Reversible Logic in Optical Domain

Reversible logic plays a crucial role in reducing energy dissipation by ensuring a bijective mapping between input and output vectors. When extended to the optical domain, reversible logic offers additional benefits such as ultrafast signal propagation, low latency, and high bandwidth, making it ideal for all-optical arithmetic and signal processing systems.

In reversible optical circuit design, several performance parameters directly influence computational efficiency:

- **Constant Inputs (CI):** Additional fixed logical inputs (typically set to 0 or 1) required to maintain reversibility without altering the primary computation.
- **Garbage Outputs (GO):** Extra outputs produced to preserve bijectivity. Although they do not contribute to the final result, they are essential to maintain information integrity.
- **Optical Cost (OC):** The number of RSOA-based switching elements used in the circuit. A lower OC implies reduced device footprint and improved integration feasibility.
- **Optical Delay (OD):** The total delay introduced by cascaded RSOAs in the critical path. Since optical switching occurs on the order of picoseconds, minimizing OD greatly enhances overall computational speed.

In reversible optical circuits, fan-out cannot be performed directly; instead, special reversible gates such as the Feynman Gate (FG) are used for signal duplication. Likewise, arithmetic

operations rely on reversible gates such as the Peres Gate (PG), which conveniently implements XOR and AND functions in a single reversible framework.

4.2.2 RSOA-Based Switching and the XGM Mechanism

The Reflective Semiconductor Optical Amplifier (RSOA) is the central photonic switching device used in the proposed architecture. Unlike conventional SOAs, an RSOA features a reflective facet, enabling bidirectional signal propagation and enhanced gain with relatively compact device dimensions. Its switching capability derives from cross-gain modulation (XGM), a nonlinear optical process in which the carrier density is modulated by a high-power control signal.

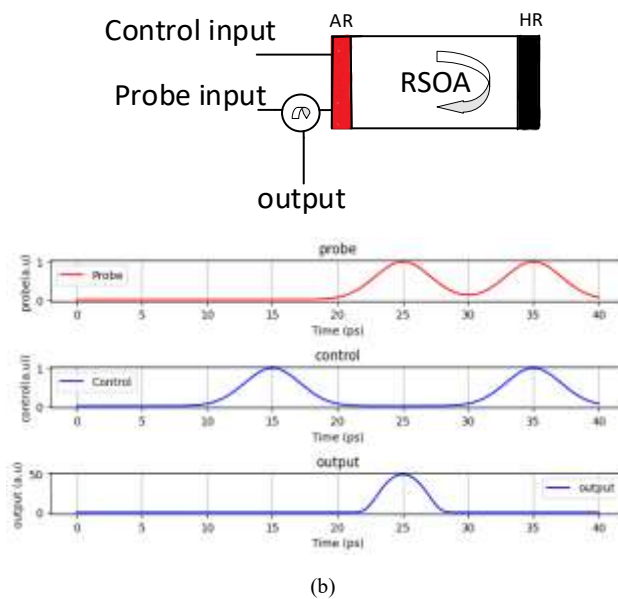


Figure 4.1: (a) Schematic diagram of the Reflective Semiconductor Optical Amplifier (RSOA) used in the switching configuration. (b) Simulated waveform showing logic levels based on control and probe signal inputs using cross-gain modulation (XGM).

The logic behaviour can be interpreted as follows: when the control signal is present (logic '1'), carrier depletion suppresses the probe gain, resulting in a low output level; when the control signal is absent (logic '0'), the probe experiences high gain, resulting in a high output level, subject to appropriate decision thresholds.

Cross-Gain Modulation Principle

When a strong control pulse enters the RSOA, it depletes the carrier density, reducing the gain available to an incoming probe signal. The resulting amplification or attenuation encodes a logical output based on the state of the control and probe signals.

The gain behavior under XGM can be expressed as:

$$G = \frac{G_0}{1 + \frac{P_c}{P_{sat}}}$$

where:

- G_0 = small-signal gain

- P_c = control signal power
- P_{sat} = saturation power of the RSOA

The output probe power is then given by:

$$P_{out} = P_p e^{(G-\alpha_D)L}$$

where:

- P_p = input probe power
- α_D = internal waveguide loss
- L = device length

These simplified expressions capture the dominant gain-saturation behaviour of the RSOA and are sufficient for logic-level modelling used in this work.

Additionally, amplified spontaneous emission (ASE) contributes noise, calculated as:

$$P_{ASE} = 2n_{sp}h\nu(G - 1)\Delta f$$

This nonlinear interaction forms the basis for implementing XOR, AND, and other logic operations using RSOA-based optical gates.

RSOA-Based Reversible Gate Operation

Both the FG and PG gates leverage XGM-induced switching to realize reversible logic functions. XOR operations are realized through complementary XGM-based gain suppression in parallel RSOA paths, followed by optical recombination, while AND operations are obtained by configuring control–probe interactions such that a high output occurs only when both input signals satisfy the required power conditions.

The RSOA's compact size, low switching energy, and compatibility with photonic integrated circuits (PICs) make it an excellent choice for creating scalable reversible optical logic blocks. Figure 4.1 illustrates the RSOA switching configuration and a representative XGM-based output waveform, validating correct logic-level operation.

These figures validate the feasibility of using XGM-driven RSOAs as the foundational switching elements for all-optical reversible arithmetic circuits [131].

4.3 All-Optical Reversible Gate and Multiplier Design

This section presents the design methodology for implementing reversible optical logic gates using RSOA-based switching elements and their integration into a complete 2×2-bit all-optical reversible multiplier. The approach relies on the inherent nonlinear gain characteristics of RSOAs under cross-gain modulation, enabling the realization of XOR, AND, and fan-out operations required for reversible arithmetic. The key reversible primitives—Feynman Gate

(FG) and Peres Gate (PG)—are first described in their optical form, followed by the system-level architecture of the proposed optical multiplier

4.3.1 Feynman Gate (FG)

The Feynman Gate (FG), also known as the Controlled-NOT (CNOT) gate, is a 2×2 reversible gate that produces the outputs:

$$P = A, Q = A \oplus B$$

This gate is essential in reversible computation because it enables fan-out (signal duplication), which is otherwise not permissible in reversible logic circuits.

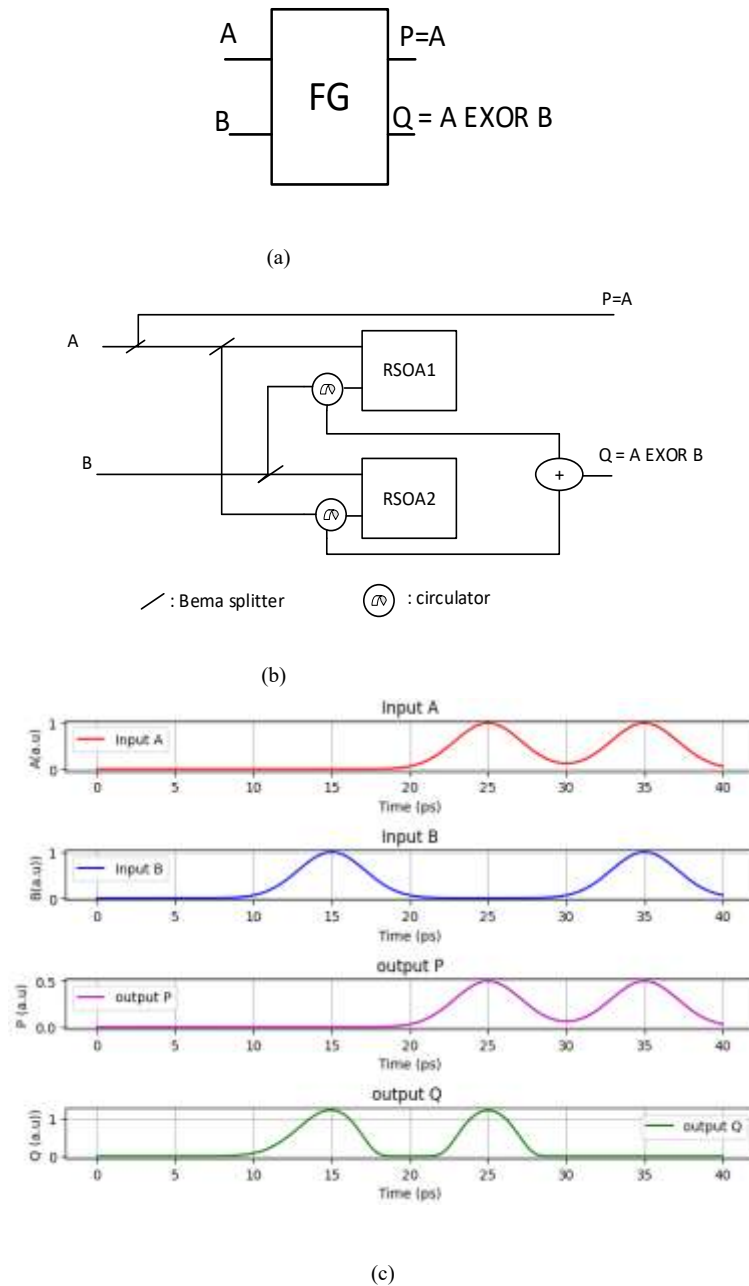


Figure 4.2: (a) Block diagram of FG gate, (b) RSOA implementation of FG gate, (c) Simulation waveform of FG gate [17].

Optical Realization Using RSOA Switching:

In the proposed optical implementation, two RSOA switches are configured to generate the XOR behaviour through XGM:

- RSOA1: Probe = B, Control = A $\rightarrow$ Output = $A'B$
- RSOA2: Probe = A, Control = B $\rightarrow$ Output = $B'A$

The optical recombination of these outputs yields:

$$Q = A'B + B'A = A \oplus B$$

The identity output $P = A$ is obtained by tapping the input signal A through a beam splitter, which preserves the input signal without violating reversibility.

Performance Metrics:

- Optical Cost (OC): 2 RSOAs
- Optical Delay (OD): 1Δ

Figure 4.2 illustrates the FG block diagram, RSOA switching model, and simulated waveform, all confirming correct XOR operation.

Table 4.1: RSOA based Logic Operation of FG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	'B'	'A'	' $\bar{A}B$ '
RSOA2	'A'	'B'	' $\bar{B}A$ '
$P = A$ $Q = \text{Output RSOA1} + \text{Output RSOA2} = A \oplus B$			

4.3.2 Peres Gate (PG)

The Peres Gate (PG) is a 3×3 reversible gate that simultaneously produces XOR and AND-based outputs:

$$P = A, Q = A \oplus B, R = AB \oplus C$$

Its ability to combine two logic operations makes it particularly suitable for reversible arithmetic such as half-adders, full-adders, and partial product computation in multipliers.

Optical Realization Using RSOA Switching

The optical PG gate employs six RSOA switches and seven beam splitters, forming a modular configuration capable of implementing both XOR and controlled-AND operations:

- RSOA1 & RSOA2: Generate $A \oplus B$
- RSOA3 & RSOA4: Generate $\bar{A}$ and intermediate terms required for AND logic
- RSOA5 & RSOA6: Implement $AB \oplus C$

When $C = 0$, the gate behaves as a reversible half-adder, producing sum and carry outputs.

Performance Metrics:

- Optical Cost (OC): 6 RSOAs

- Optical Delay (OD): 3Δ

Figure 4.3 presents the PG gate model and simulation waveform validating the expected logic outputs.

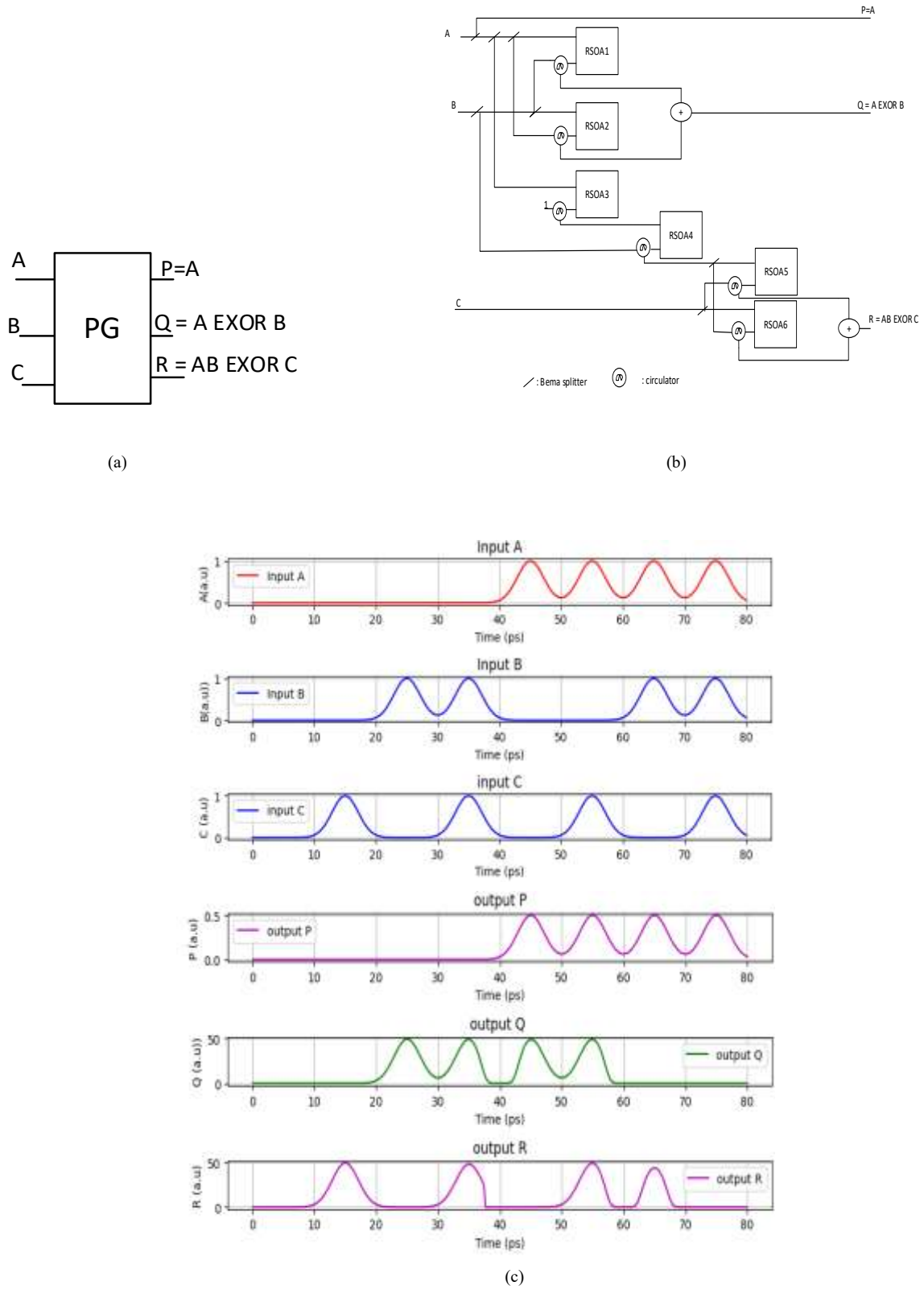


Figure 4.3: (a) Block diagram of PG gate, (b) RSOA implementation of PG gate, (c) Simulation waveform of PG gate.

Table 4.2: RSOA-Based Logic Operations of PG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	'B'	'A'	' $\bar{A}B$ '
RSOA2	'A'	'B'	' $\bar{B}A$ '
RSOA3	High state	'A'	' $\bar{A}$ '
RSOA4	'B'	' $\bar{A}$ '	' $\bar{\bar{A}}B$ '
RSOA5	'C'	'AB'	' $\bar{A}\bar{B}C$ '
RSOA6	'AB'	'C'	' $\bar{C}AB$ '
$P = A$ $Q = \text{RSOA1} + \text{RSOA2} = A \oplus B$ $R = \text{RSOA5} + \text{RSOA6} = AB \oplus C$			

4.3.3 Architecture of the All-Optical 2×2-Bit Reversible Multiplier

The proposed 2×2-bit reversible multiplier integrates RSOA-based FG and PG gates to realize binary multiplication in a fully reversible optical domain. The architecture consists of four main functional stages:

1. Fan-Out Generation Using FG Gates

Reversible logic does not allow direct replication of signals; therefore, four FG gates are used to generate duplicate copies of inputs:

- A_1, A_0
- B_1, B_0

Each FG gate receives a constant input (set to 0), ensuring that the original input bit is preserved while generating its copy.

This stage guarantees that the subsequent partial-product generators receive the required independent signal lines without violating reversibility.

2. Partial Product Generation Using PG Gates

Partial products for a 2×2-bit multiplication are computed as:

$$P_3 = A_1B_1, P_2 = A_1B_0, P_1 = A_0B_1, P_0 = A_0B_0$$

Each AND operations are implemented through the R-based output of a PG gate configured for AND functionality via XGM.

This step forms the foundational multiplicative components necessary for reconstructing the final 4-bit product.

3. Addition of Partial Products Using PG Gates as Half Adders

The intermediate partial products P_2 and P_1 are added using PG gates configured as reversible half adders perform:

$$\text{Sum} = P_2 \oplus P_1, \text{Carry} = P_2P_1$$

This reversible addition ensures a bijective mapping and avoids loss of information.

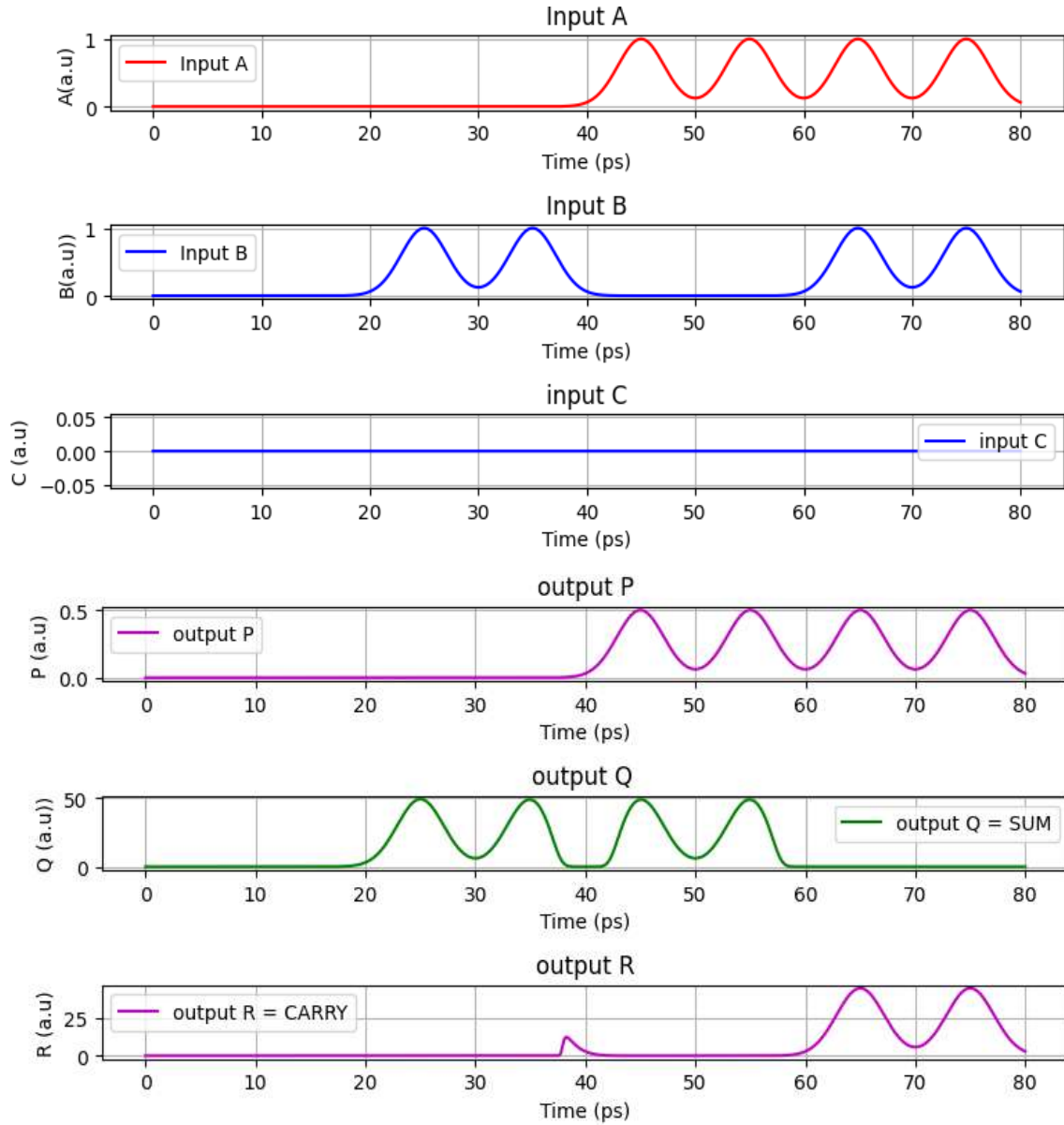


Figure 4.4: PG gate as a half adder

4. Final Product Synthesis

The final 4-bit product is obtained through reversible optical shift-and-add operations as:

$$P_{\text{out}} = [P_3 \ll 2] + [(P_2 + P_1) \ll 1] + P_0$$

where “ $\ll$ ” denotes binary left shift.

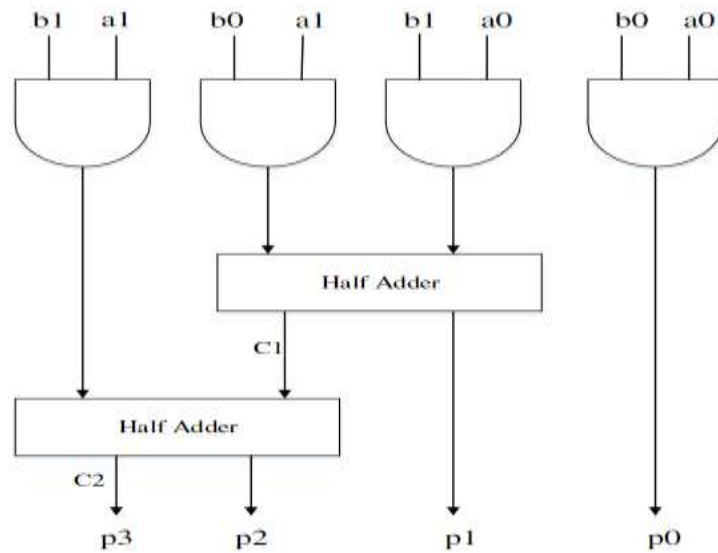
The resulting output bits (P_3, P_2, P_1, P_0) collectively represent the optical 2×2 -bit multiplication result.

Circuit Metrics and Characteristics

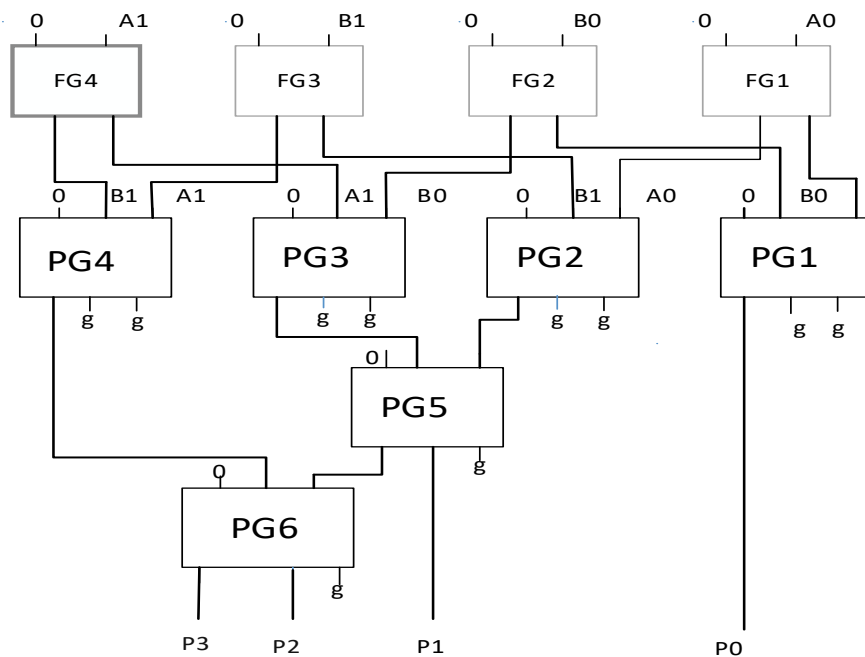
- Constant Inputs (CI): 10
- Garbage Outputs (GO): 10
- Optical Cost (OC): 44 RSOAs
- Optical Delay (OD): 10Δ

These values demonstrate that the proposed architecture maintains strict reversibility while achieving efficient optical computation.

Figures 4.4-4.7 provide the circuit diagrams, component-level layouts, and simulation waveforms confirming logical correctness.



(a)



(b)

Figure 4.5: (a) Block diagram of 2x2-bit multiplier, (b) Implementation of 2x2-bit multiplier using RSOA-FG and RSOA-PG logic gates.

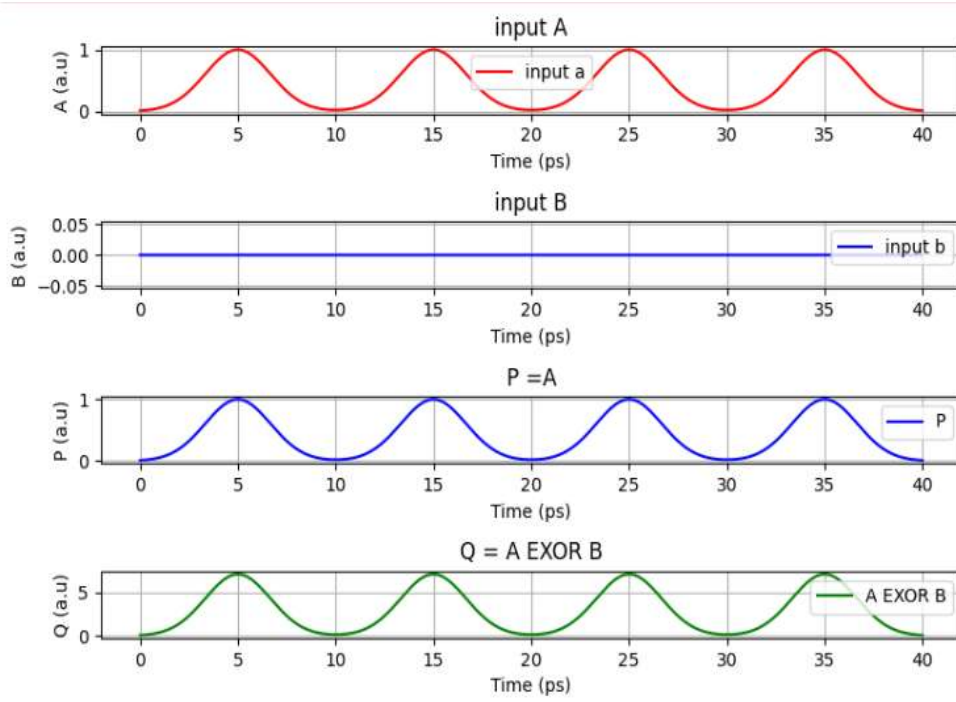


Figure 4.6: FG gate with inputs $A = [1,1,1,1]$, $B = [0,0,0,0]$ and outputs $P = A$ $[1,1,1,1]$, $Q = A$ $[1,1,1,1]$, generate copy of A.

4.4 Simulation and Results

This section presents the simulation methodology and performance evaluation of the proposed 2×2 -bit all-optical reversible multiplier implemented using RSOA-based Feynman (FG) and Peres (PG) gates. The simulations were conducted using a custom Python-based photonic modeling framework developed in a Jupyter Notebook environment. The framework emulates the nonlinear gain behaviour of RSOAs under cross-gain modulation (XGM), enabling accurate representation of the reversible optical logic operations required in the multiplier.

4.4.1 Functional Verification

The multiplier was simulated for all sixteen combinations of the 2×2 input operands (A_1A_0, B_1B_0). Figure 4.7 shows an example waveform illustrating the temporal evolution of the output signals for a representative input case. The outputs P_3, P_2, P_1, P_0 consistently matched the expected binary results produced by the mathematical model of the 2×2 -bit multiplication.

Table 4.5 presents the complete truth table for the proposed design. The simulated outputs were cross-verified with the theoretical results, demonstrating full functional correctness. No inconsistency was observed across any test cases, confirming that the reversible optical logic gates preserve bijective input–output mapping and do not merge computational states.

4.4.2 Simulation Parameters

The RSOA device parameters used in the simulation are summarized in Table 4.6. These values correspond to practical device specifications reported in recent photonic literature and ensure physically realistic performance modelling.

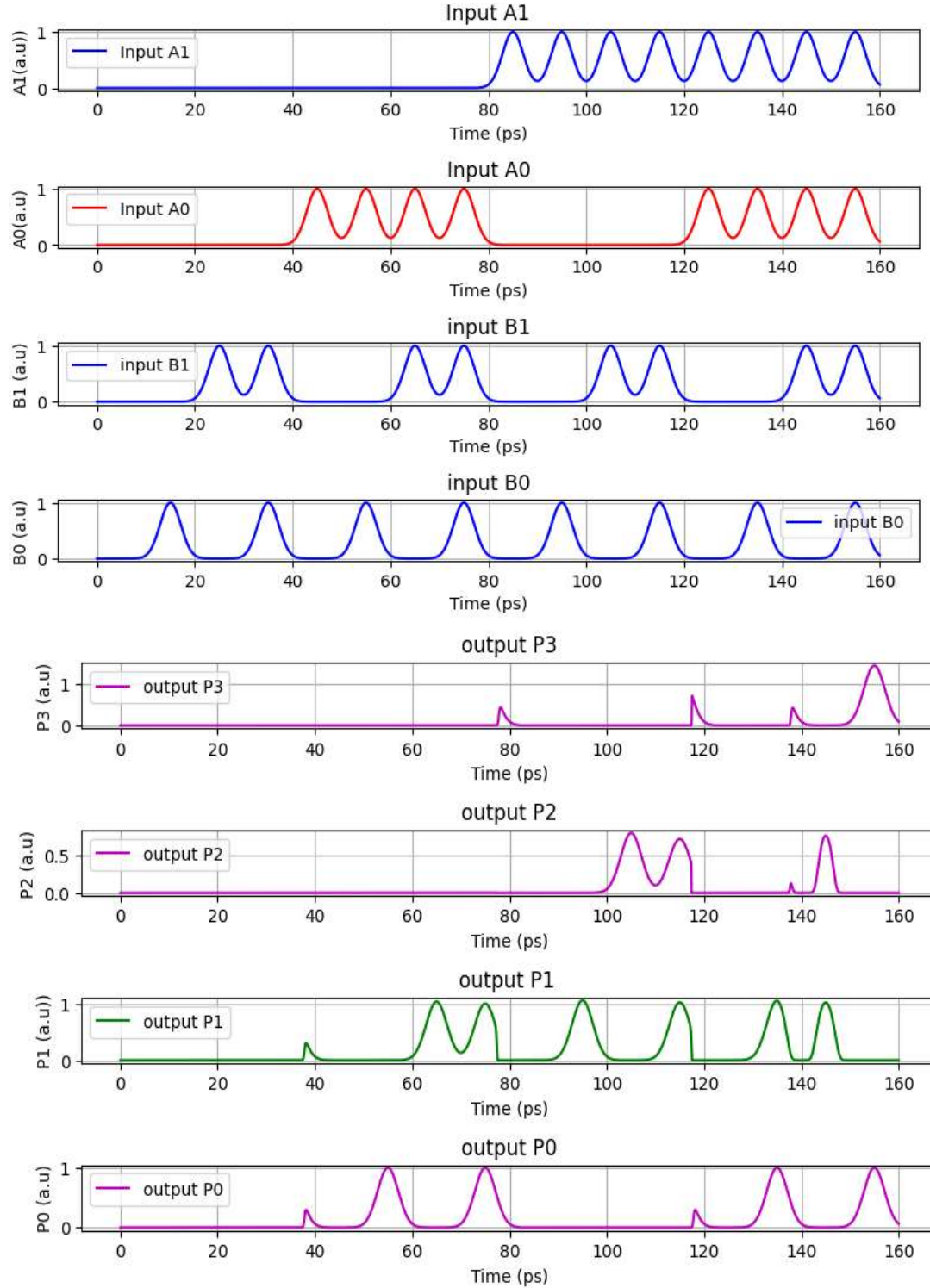


Figure 4.7: Simulation waveform of the 2x2-bit multiplier

Key parameters include:

- Confinement factor $\Gamma = 0.48$

- Injection current $I = 200 \text{ mA}$
- Internal waveguide loss $\alpha_D = 2700 \text{ m}^{-1}$
- Saturation energy $E_s = 25 \text{ fJ}$
- Operating wavelength $\lambda = 1550 \text{ nm}$
- Data rate $B = 100 \text{ Gbps}$

These device-level properties directly influence the gain compression, switching quality, and noise characteristics such as amplified spontaneous emission (ASE), which in turn affect the logic output fidelity. These parameters are selected to reflect representative device characteristics reported in the literature and are used here for comparative and architectural evaluation rather than absolute hardware prediction.

Table 4.3: Truth Table of 2x2- Multiplier

INPUTS				OUTPUTS			
A1	A0	B1	B0	P3	P2	P1	P0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

4.4.3 Signal Quality Metrics (ER, Q-Factor, and REOP)

To assess the quality of the optical signals generated by the multiplier, three widely used photonic performance metrics were evaluated:

• Extinction Ratio (ER)

ER quantifies the contrast between logical ‘1’ and ‘0’ power levels:

$$ER = 10 \log_{10} \left(\frac{P_1}{P_0} \right)$$

Higher ER values indicate stronger modulation and improved signal detectability.

• **Q-Factor**

Q-factor provides an estimate of the signal-to-noise margin at the decision threshold using:

$$Q = \frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}$$

where μ and σ are the mean and standard deviation of logical levels.

• **Relative Eye-Opening Percentage (REOP)**

$$REOP(\%) = \frac{P_{\max} - P_{\min}}{P_{\max}} \times 100$$

REOP reflects eye diagram clarity, indicating resilience to inter-symbol interference (ISI).

4.4.4 Impact of Control Energy and Injection Current

The influence of control pulse energy E_c and injection current I on circuit performance was analyzed for three biasing currents: 180 mA, 190 mA, and 200 mA.

Figures 4.8-4.10 illustrate how ER, Q-factor, and REOP vary with E_c for the outputs P_0, P_1, P_2, P_3 .

Table 4.4: Parameter used in simulation

Symbol	Parameter	Value
Γ	Confinement factor	0.48
c	Velocity of light	$3 \times 10^8 \text{ m/s}$
I	Injection current	200 mA
αN	Differential gain	$3.3 \times 10^{-20} \text{ m}^2$
N_t	Carrier density at transparency	$1 \times 10^{24} \text{ m}^{-3}$
w	Width of the active region	1.5 μm
d	Depth of the active region	250 nm
L	Active length	150 μm
α_D	Internal loss of the waveguide	2700 m^{-1}
λ	Wavelength of light	1550 nm
E_c	Control pulse energy	20 fJ
τ_{FWHM}	Full-width at half-maximum	5 ps
n_2	Nonlinear coefficient	$2.6 \times 10^{-20} \frac{\text{m}^2}{\text{W}}$
D	Dispersion constant	1 ps/(nm km)
A_{eff}	Fiber effective area	$5 \times 10^{-13} \text{ m}^2$
E_s	Saturation energy	25 fJ
b_0	Optical bandwidth	3 nm
n_{sp}	ASE factor	2
B	data rate	100 Gbps

Observations:

- Increasing injection current consistently enhances ER, Q-factor, and REOP.

- Higher control energy leads to mild degradation in these metrics due to gain saturation in the RSOA.
- Minor variations across different output bits arise from input-dependent nonlinearities inherent to XGM.

Overall, the outputs remain within high-performance operational bounds across the tested energy range.

4.4.5 Performance at 100 Gbps Operation

At the nominal bias $I = 200$ mA and control energy $E_c = 20$ fJ, the multiplier demonstrated excellent switching characteristics.

Measured performance for output bits P_0 – P_3 :

Output Bit	ER (dB)	Q-Factor	REOP (%)
P_0	22.48	12.4	99.46
P_1	25.45	13.0	99.76
P_2	25.75	13.1	99.74
P_3	25.18	13.0	99.65

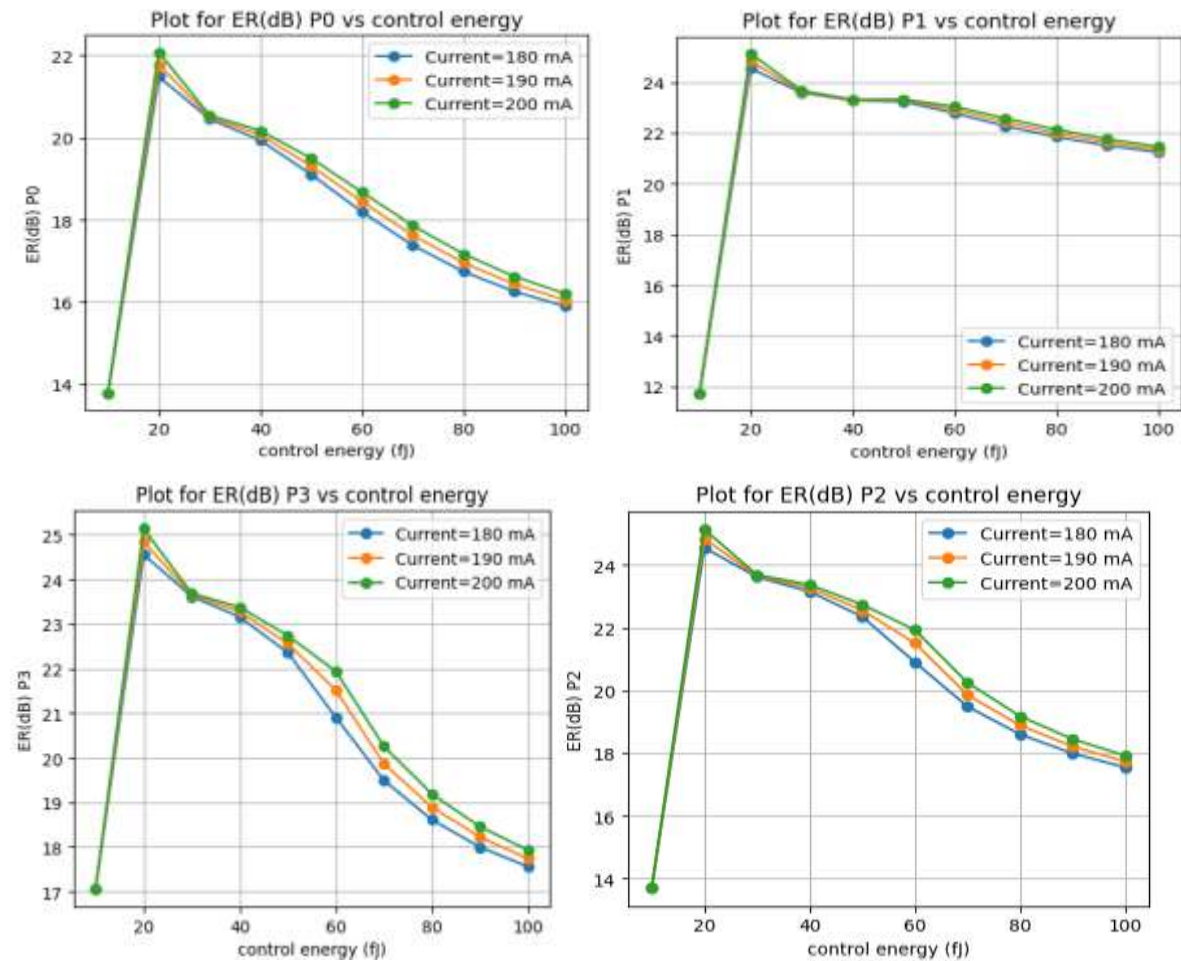


Figure 4.8: Plot of Extinction Ratio (ER) vs. Control Energy (E_c) for outputs P_0 , P_1 , P_2 , and P_3 .

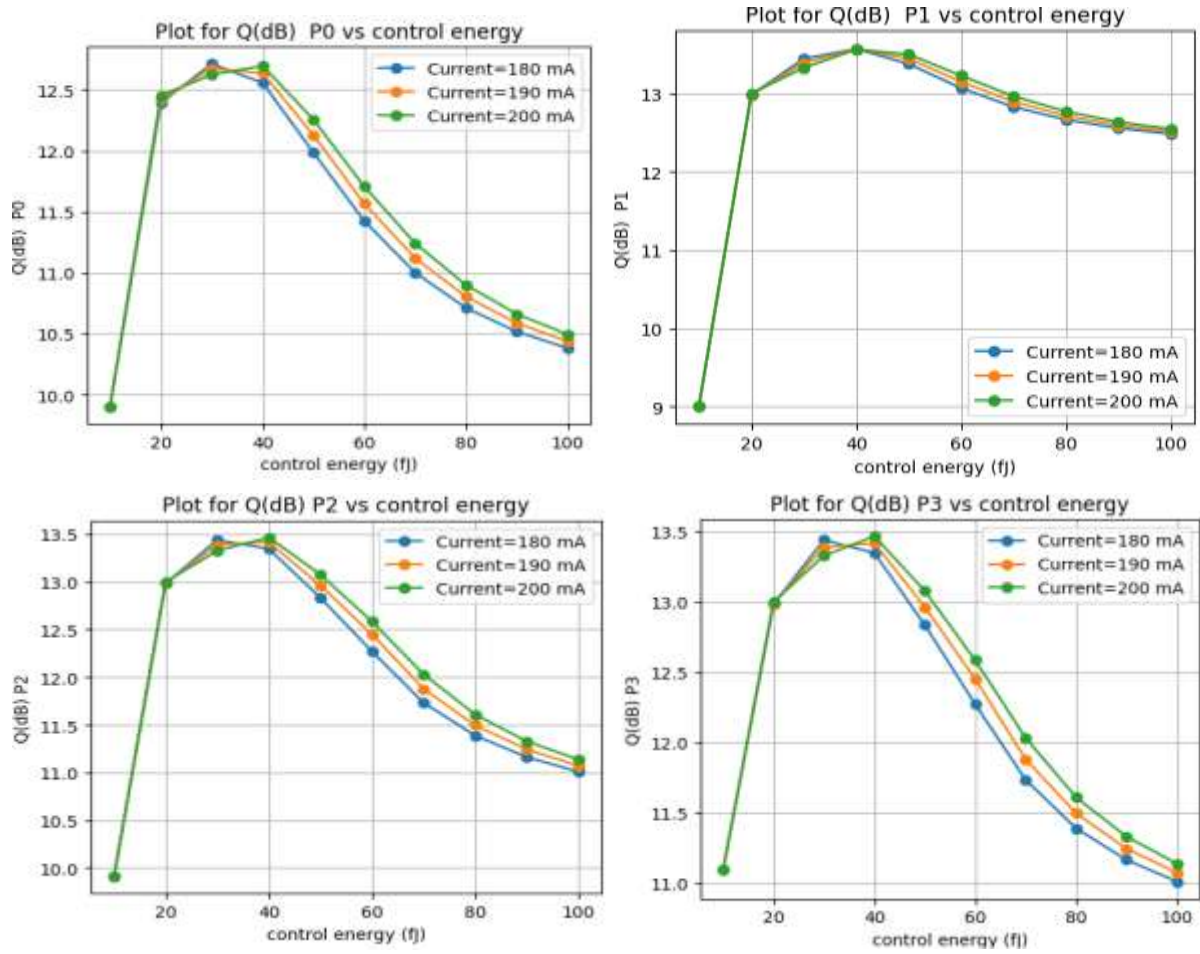


Figure 4.9: Plot of Q-factor (Q) vs. Control Energy (Ec) for outputs P0, P1, P2, and P3

These results confirm:

- High modulation depth ($ER > 22$ dB)
- Strong signal-to-noise ratio ($Q > 12$)
- Near-ideal eye openings ($> 99\%$)

These values indicate robust logic-level separation under the simulated operating conditions. Such performance validates the suitability of RSOA-based reversible gates for high-throughput photonic arithmetic

4.4.6 Comparison with Existing Optical Multipliers

Table 4.7 compares the proposed reversible optical multiplier with several all-optical multipliers reported in prior work.

Key Findings:

- Most existing designs do not support reversibility, leading to information loss and higher power dissipation.
- Many earlier architectures lack reported ER/Q-factor values, limiting their suitability for high-fidelity optical processing.

- The proposed RSOA-based design achieves:
 - Comparable or superior ER (≈ 25 dB)
 - High Q-factor (~ 13)
 - Excellent REOP ($\sim 99\%$)

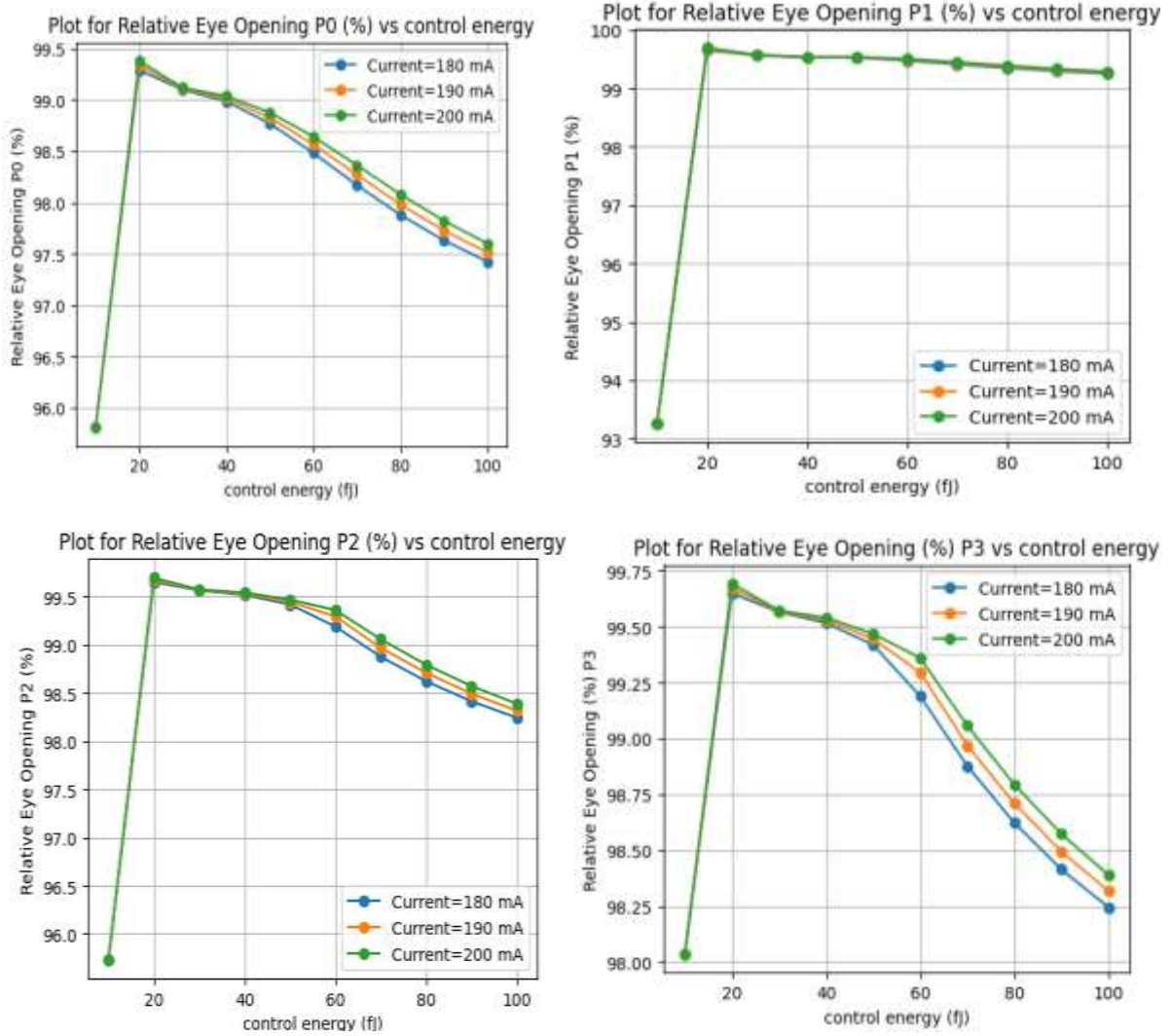


Figure 4.10: Plot of Relative Eye Opening (REOP) vs. Control Energy (E_c) for outputs P0, P1, P2, and P3.

Thus, the proposed architecture not only ensures reversibility but also demonstrates comparable or improved signal quality metrics while uniquely supporting reversible computation.

4.4.7 Overall Performance Assessment

The comprehensive simulation results demonstrate that:

- The proposed 2×2 -bit reversible optical multiplier produces correct outputs for all input combinations.
- The design exhibits excellent noise tolerance and high-speed switching capability.

- Control energy variations introduce minor performance degradation, consistent with RSOA gain dynamics.
- The architecture is structurally modular, allowing extension to higher-bit multipliers without fundamental redesign.

These findings highlight the robustness and feasibility of RSOA-based reversible logic for next-generation photonic computing and arithmetic processors.

Table 4.5: Comparison of proposed design with existing optical multiplier architectures.

Reference	Technology Used	ER (dB)	REOP (%)	Q(dB)	reversible
[66]	Semiconductor Optical Amplifier—assisted Sagnac Switch	25.16	Not calculated	Not calculated	no
[67]	Polarization Switch	Not calculated	Not calculated	Not calculated	no
[68]	Micro-ring resonator	12.9	Not calculated	Not calculated	no
[69]	Photonic Crystal Structure.	8.82	Not calculated	Not calculated	no
[70]	MIM Waveguides	Not calculated	Not calculated	31.31	no
[71]	SPP technology	Not calculated	Not calculated	Not calculated	no
Our work	Reflective Semiconductor Optical Amplifier	25.89	99 (approx.)	13.46	yes

4.5 Summary

This chapter presented the design, implementation, and performance evaluation of a 2×2 -bit all-optical reversible multiplier constructed using RSOA-based Feynman (FG) and Peres (PG) gates. The proposed architecture leverages the cross-gain modulation (XGM) mechanism of Reflective Semiconductor Optical Amplifiers to realize reversible XOR and AND functions, enabling a fully photonic computation framework that preserves information through bijective input–output mapping and supports energy-efficient operation.

The chapter began by outlining the motivation for all-optical reversible arithmetic circuits and introduced the fundamental switching behaviour of RSOAs. Detailed optical implementations of the FG and PG gates were then presented, along with their corresponding optical cost, optical delay, and signal-level behaviour, establishing them as suitable primitives for reversible optical computation within RSOA-based architectures.

A complete 2×2 -bit multiplier was designed using these reversible gates, comprising four functional stages: reversible fan-out generation, partial product computation, reversible addition, and final output synthesis. The design strictly adhered to the constraints of reversibility, resulting in 10 constant inputs, 10 garbage outputs, and a total optical cost of 44 devices with a critical path delay of 10Δ .

Simulation studies conducted using a Python-based numerical framework validated the correctness of the multiplier for all sixteen input combinations. The device-level photonic evaluation demonstrated excellent signal integrity, with high extinction ratio (ER), Q-factor, and relative eye opening (REOP) values at 100 Gbps operation. These results indicate strong modulation capability, high signal-to-noise margins, and robust noise tolerance under the simulated operating conditions.

Performance trends with respect to control energy and injection current indicated predictable and physically consistent behavior. While higher control energy induced mild degradation due to gain saturation, increasing injection current improved the overall signal quality, showcasing the tunability of RSOA-driven logic circuits. Comparative analysis further demonstrated that the proposed reversible multiplier achieves comparable or improved signal-quality metrics relative to several existing all-optical multiplier architectures, while uniquely supporting reversible computation. A substantial part of the work presented in this chapter has been peer-reviewed and published in the *Indian Journal of Pure & Applied Physics*.

Overall, this chapter establishes a foundational building block for larger reversible photonic arithmetic systems. The demonstrated functionality, signal fidelity, and modular design flexibility make the proposed approach well-suited for extending to higher-bit multipliers and integrating into next-generation all-optical processors and photonic computation platforms. The insights gained here lay a strong foundation for the more advanced all-optical multiplier architectures presented in the subsequent chapter.

Chapter 5: All-optical n-bit Multiplier

5.1 Introduction

The increasing demand for ultra-high-speed communication systems, photonic signal processors, and optical accelerators has intensified the need for arithmetic circuits capable of operating entirely in the optical domain. Among these, multipliers constitute a fundamental computational block in digital signal processing (DSP) tasks such as filtering, Fourier transforms, modulation, and correlation. As operating frequencies and data rates continue to rise, conventional electronic multipliers encounter inherent limitations due to resistive losses, thermal dissipation, and RC-delay constraints, motivating the exploration of all-optical arithmetic architectures.

Recent research has demonstrated several all-optical multiplier implementations, predominantly based on Semiconductor Optical Amplifiers (SOAs) integrated within Mach–Zehnder Interferometers (MZIs). While MZI–SOA-based multipliers offer high switching speeds, they are inherently irreversible, resulting in information loss during computation and unavoidable energy dissipation in accordance with Landauer’s principle. In addition, interferometer-based architectures suffer from phase-matching requirements, polarization sensitivity, amplified spontaneous emission (ASE) noise accumulation, and scalability challenges as the number of cascaded interferometric stages increases with bit-width.

In contrast, Reflective Semiconductor Optical Amplifiers (RSOAs) enable interferometer-free optical switching based on cross-gain modulation (XGM), offering compact device footprints, improved stability, and reduced sensitivity to phase and polarization variations. More importantly, RSOA devices support the realization of reversible optical logic gates, enabling information-preserving computation in the optical domain. The feasibility of RSOA-based reversible arithmetic was established in Chapter 4 through the design and simulation of a 2×2 -bit all-optical reversible multiplier, which served as a validated building block for scalable designs.

Building upon this foundation, the present chapter addresses the problem of scaling all-optical multiplication to arbitrary n-bit widths. To this end, the chapter adopts a structured two-part methodology. In the first part, n-bit all-optical Vedic multipliers are realized using MZI–SOA switching elements in conjunction with existing adder architectures reported in the literature. These designs are intentionally kept irreversible and are used solely as benchmark architectures to study optical cost–delay trade-offs, scalability behaviour, and the limitations inherent to interferometer-based multipliers. Analytical comparisons with state-of-the-art MZI–SOA

multipliers are carried out in terms of optical cost (OC), optical delay (OD), ancilla input (N_{AI}) and garbage output (N_{GO}).

In the second part, the focus shifts to the development of a fully reversible, interferometer-free all-optical n -bit Vedic multiplier using RSOA-based switching. Following the same design philosophy adopted in Chapter 4, a 2×2 -bit reversible Vedic multiplier is first employed as the fundamental building block. Reversible RSOA-based ripple-carry adders (RCA) and carry-save adders (CSA) are then designed and integrated to support scalable multiplication. Using the hierarchical Urdhva–Tiryagbhyam (UT) decomposition strategy, identical to that employed for the quantum-domain architecture in Chapter 3, the proposed reversible blocks are recursively combined to construct an n -bit all-optical reversible Vedic multiplier.

For the proposed n -bit designs, performance evaluation is carried out through closed-form analytical expressions for optical cost (OC), optical delay (OD), constant inputs (CI), and garbage outputs (GO). No signal-quality simulations are performed at higher bit-widths; instead, scalability and efficiency are assessed analytically based on the validated behaviour of the 2×2 reversible building block. This methodology enables a clear and fair comparison between irreversible interferometer-based multipliers and the proposed reversible RSOA-based architecture, highlighting the benefits of reversibility, interferometer-free operation, and structured scalability.

Overall, this chapter establishes a systematic framework for scalable all-optical reversible multiplication, bridging conventional interferometer-based designs and next-generation reversible photonic arithmetic units. The results presented here form a critical step toward energy-efficient optical ALUs and quantum-compatible photonic computing platforms.

5.2 Overview of the Proposed Methodology (Two-Phase Development Strategy)

The design of an all-optical n -bit multiplier in this research follows a two-phase development strategy. This staged approach allows the work to (i) first design and analytically benchmark interferometer-based all-optical multipliers using existing architectures reported in the literature, and (ii) subsequently develop a fully reversible, interferometer-free n -bit multiplier using RSOA-based switching. This methodology ensures a clear distinction between benchmarking studies and novel contributions while enabling a fair evaluation of scalability, optical cost, and delay characteristics.

5.2.1 Phase I: Development of SOA–MZI–Based N -Bit Vedic Multipliers

In the first phase of this work, an $n \times n$ all-optical Vedic multiplier was designed using Mach–Zehnder Interferometers (MZIs) configured with Semiconductor Optical Amplifiers (SOAs).

The Urdhva–Tiryagbhyam (UT) multiplication algorithm was employed due to its inherent parallelism and suitability for hierarchical optical realization.

Three multiplier architectures were developed by integrating the UT algorithm with existing adder architectures reported in the literature:

- **Design 1:** UT algorithm combined with existing Carry Look-Ahead (CLA) adders [73]
- **Design 2:** UT algorithm combined with existing Carry-Save Adder (CSA) structures using 2-bit basic blocks [74]
- **Design 3:** UT algorithm combined with existing Carry-Save Adder (CSA) structures using 4-bit basic blocks [74]

All three designs were constructed exclusively using MZI-SOA switching elements, and no new adder or logic structures were introduced in this phase. These architectures are irreversible by construction and are used solely as benchmark designs.

For each design, closed-form analytical expressions were derived for the following performance parameters:

- Optical Cost (OC)
- Optical Delay (OD)
- Constant Inputs (CI)
- Garbage Outputs (GO)

The derived expressions were compared with state-of-the-art MZI-SOA-based multipliers reported in the literature, including PLD-based, array-based, and CSA-based optical multipliers, in order to evaluate optical cost–delay trade-offs and scalability trends.

Key Findings from Phase I Analysis

- MZI-SOA-based multiplier architectures offer high switching speed but remain irreversible, resulting in information loss during computation.
- As the bit-width increases, the number of interferometric stages grows rapidly, leading to increased optical cost and optical delay, and significantly higher architectural complexity.
- The extensive use of interferometric structures introduces practical implementation challenges, including stringent phase-balancing requirements, sensitivity to fabrication tolerances, and increased control overhead for stable operation in large-scale circuits.
- Existing adder architectures (CLA, CSA) introduce distinct trade-offs between optical cost and optical delay when integrated within UT-based multiplier frameworks.
- None of the MZI-SOA-based multipliers preserve logical reversibility, making them unsuitable for thermodynamically efficient or quantum-inspired photonic computation.

This analytical benchmarking study establishes the structural and scalability limitations of interferometer-based all-optical multipliers and motivates the transition toward interferometer-free, reversible photonic architectures, which are addressed in Phase II.

5.2.2 Phase II: Development of RSOA-Based Reversible N-Bit Vedic Multipliers

Building upon the insights obtained from the Phase I benchmarking study, Phase II focuses on the development of a fully reversible, interferometer-free all-optical n-bit Vedic multiplier implemented using Reflective Semiconductor Optical Amplifiers (RSOAs). Unlike MZI-SOA-based architectures, RSOAs operate without interferometric paths and rely on cross-gain modulation (XGM) for intensity-based optical switching. This operating principle offers several practical advantages, including:

- Polarization-insensitive switching, eliminating polarization control requirements,
- Compact device footprint, facilitating dense photonic integration,
- Improved operational stability due to the absence of phase-sensitive interferometric structures,
- Elimination of phase control and path-balancing constraints, which simplifies large-scale implementation.

Most importantly, RSOA devices enable the realization of reversible optical logic gates, allowing bijective, information-preserving input–output mappings in the optical domain.

To realize scalable reversible multiplication, reversible adder architectures developed earlier in the thesis—specifically reversible ripple-carry adders (RCA) and reversible carry-save adders (CSA)—are mapped into the optical domain using RSOA-based switching behaviour. These reversible adders are integrated with RSOA-based reversible logic gates to construct a Vedic multiplier architecture based on the Urdhva–Tiryagbhyam (UT) algorithm.

Key Contributions of Phase II

- Development of a fully reversible all-optical n-bit Vedic multiplier using interferometer-free RSOA switching.
- Derivation of closed-form analytical expressions for optical cost (OC), optical delay (OD), constant inputs (CI), and garbage outputs (GO) for arbitrary n-bit designs.
- A modular and hierarchical architecture that enables systematic scalability from 2-bit building blocks to n-bit multipliers.
- Preservation of information through reversible computation, supporting thermodynamically efficient optical processing.
- Structural compatibility with quantum-inspired photonic computation and low-power optical arithmetic logic units (ALUs).

5.3 Proposed All-Optical n-Bit Multiplier Architecture

This section presents the complete framework for designing all-optical $n \times n$ Vedic multipliers investigated in this chapter. The development is carried out in two distinct and progressive stages to systematically transition from conventional interferometric optical arithmetic toward reversible and energy-efficient photonic computation.

In the first stage, an irreversible all-optical n -bit Vedic multiplier is realized using Mach–Zehnder Interferometer (MZI) structures integrated with Semiconductor Optical Amplifiers (SOAs). This stage exclusively employs existing adder architectures reported in the literature and serves as a benchmarking platform to analyze optical cost–delay trade-offs against state-of-the-art SOA–MZI-based multiplier designs.

In the second stage, a fully reversible and interferometer-free all-optical N -bit Vedic multiplier is developed using Reflective Semiconductor Optical Amplifiers (RSOAs). This architecture leverages reversible optical logic gates and proposed reversible adder blocks to preserve information and enable scalable, thermodynamically efficient photonic arithmetic.

Together, these two stages establish a comprehensive design pathway from conventional irreversible optical multipliers to reversible, quantum-compatible photonic arithmetic units.

5.3.1 MZI-SOA–Based n-Bit Vedic Multiplier

In the first stage of this work, an $n \times n$ all-optical Vedic multiplier is constructed using MZI-SOA interferometric switching elements. These switches exploit carrier-induced phase modulation within the MZI arms to implement fundamental optical logic operations such as AND and XOR. The multiplication process is governed by the Urdhva–Tiryagbhyam (UT) Vedic algorithm, which enables parallel generation of partial products and supports hierarchical expansion to higher bit widths.

To investigate the impact of different adder structures on optical cost and delay, three MZI-SOA-based multiplier architectures are developed. Each design uses only existing adder circuits reported in the literature, without introducing any new or reversible adder modifications.

Design 1: MZI-SOA Multiplier Using Existing Carry Look-Ahead (CLA) Adders

- Employs published CLA architectures for partial-product summation.
- Achieves reduced optical delay due to faster carry computation [73].
- Incurs increased optical cost because of additional interferometric switching stages.

Design 2: MZI-SOA Multiplier Using Existing 2-bit CSA Blocks

- Utilizes existing 2-bit Carry-Save Adder (CSA) modules [74].

- Reduces sequential carry propagation delay.
- Results in moderately higher optical cost compared to CLA-based design.
- Suitable for moderate n-bit multiplier sizes.

Design 3: MZI-SOA Multiplier Using Existing 4-bit CSA Blocks

- Employs larger 4-bit CSA building blocks to enhance block-level parallelism.
- Achieves the lowest optical delay among the three SOA–MZI designs.
- Involves higher optical cost due to increased adder complexity [74].

All three SOA–MZI-based multipliers are irreversible, reflecting the fundamental limitation of interferometric architectures. These designs primarily serve as reference models for evaluating optical cost–delay trade-offs and benchmarking the improvements achieved through the reversible RSOA-based architecture introduced in the next stage.

5.3.2 RSOA–Based Fully Reversible N-Bit Vedic Multiplier (Using Proposed Adders)

The second stage introduces the central contribution of this thesis: a fully reversible, interferometer-free all-optical n-bit Vedic multiplier implemented using Reflective Semiconductor Optical Amplifier (RSOA) switches.

Unlike MZI-SOA circuits, RSOA-based logic operates through cross-gain modulation (XGM), enabling stable intensity-based switching without requiring phase alignment or interferometric path balancing. This eliminates key limitations associated with MZI-based architectures, such as thermal drift, polarization sensitivity, and fabrication-induced phase mismatch.

The proposed RSOA-based multiplier architecture is constructed entirely from reversible optical logic gates and reversible adder blocks, ensuring a bijective input–output mapping and complete preservation of information.

Key features of the proposed RSOA-based architecture include:

- Use of RSOA-based reversible logic gates (Feynman, Peres, and Toffoli gates) for fan-out, XOR, and AND operations.
- Integration of proposed reversible optical adders:
 - 4-bit reversible Ripple Carry Adder (RCA),
 - 4-bit reversible Carry-Save Adder (CSA).
- Modular UT-based structure enabling recursive scalability from 2-bit to n-bit multipliers.
- Preservation of information, ensuring thermodynamically efficient computation in accordance with reversible logic principles.

- Interferometer-free operation, improving stability and suitability for photonic integration.

While the overall structural decomposition follows the same UT-based Vedic multiplication framework as the MZI-SOA design, the RSOA-based multiplier fundamentally differs by being fully reversible and by employing newly proposed reversible adder architectures. These design choices lead to structured and predictable growth in optical cost, optical delay, constant inputs, and garbage outputs, making the architecture well suited for scalable reversible photonic arithmetic.

5.4 Optical Cost and Delay Analysis of MZI-SOA-Based N-Bit Vedic Multipliers

The proposed MZI-SOA-based $n \times n$ -bits Vedic multipliers operate in two logical stages:

- Stage α (Partial Product Generation): All vertical and crosswise partial products are generated in parallel using MZI-SOA-based 2×2 -bit Vedic multiplier cells derived from the Urdhva–Tiryagbhyam (UT) sutra.
- Stage β (Partial Product Summation): The generated partial products are summed using different adder architectures, leading to three variants: Design 1 (CLA-based), Design 2 (CSA with 2-bit basic block), and Design 3 (CSA with 4-bit basic block).

For analytical evaluation, the complexity of these multipliers is quantified using four key parameters:

- Optical Cost (OC): total number of MZI-SOA switching elements used in the realization.
- Optical Delay (OD): number of cascaded MZI stages in the critical path, expressed in units of Δ (the delay of a single MZI-SOA stage).
- Ancilla Inputs (AI): number of constant inputs (if any).
- Garbage Outputs (GO): number of unused outputs required to preserve reversibility in designs where reversible gates are used.

Since the MZI-SOA-based multipliers are irreversible, AI is zero and GO is reported only as an effective output overhead arising from the UT structure rather than true reversible garbage outputs. In this chapter, for MZI-SOA-based multipliers, the beam splitters (BS) and beam combiners (BC) are assumed to have negligible cost, and only MZI switches are counted toward OC. Similarly, OD is obtained by multiplying Δ with the maximum number of MZIs in series along the critical computation path.

5.4.1 Stage α : Partial Product Generation

Let A and B be two n -bit binary operands:

- $A = A_{n-1} \dots A_1 A_0$
- $B = B_{n-1} \dots B_1 B_0$

Using the UT algorithm, partial products are generated by a regular array of MZI-SOA-based 2-bit Vedic multiplier units. As shown in Figure 5.1, OC of 2-bit MZ-SOA based VM is 8 and OD is 3Δ . For an $n \times n$ multiplier, the partial-product generation stage requires $2^{2\log_2 n + 1}$ MZI-SOA switching elements, yielding $OC(\alpha) = N_{MZI} = 2^{2\log_2 n + 1}$, while the optical delay remains constant at $OD(\alpha) = 3\Delta$

This stage is common to all three designs (Design 1–3), since each uses the same UT-based decomposition for partial product generation.

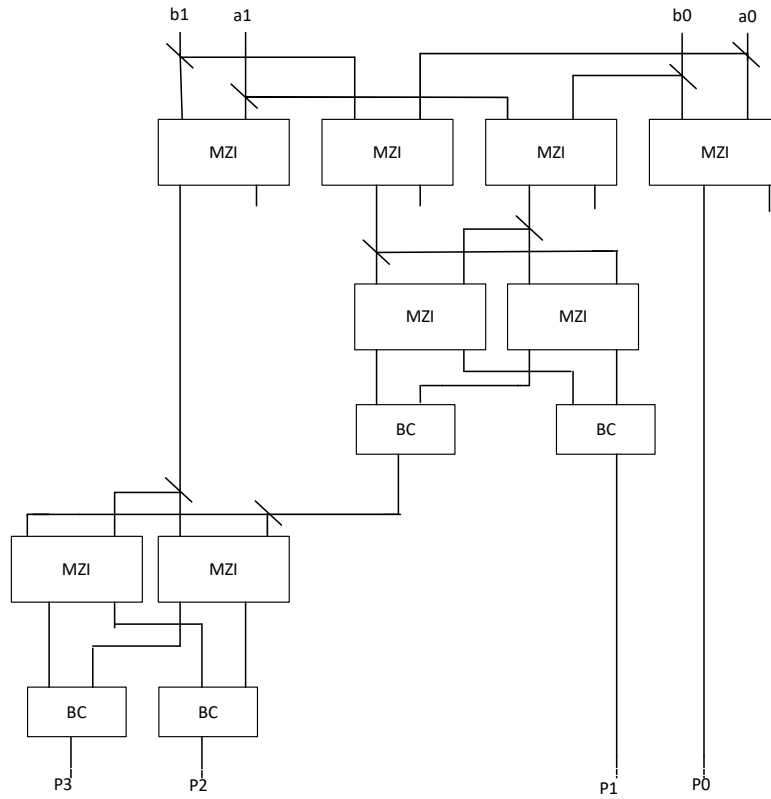


Figure 5.1: All-optical circuit of 2-bit VM [132].

5.4.2 Stage β : Partial Product Summation

In the second stage, the partial products from UT expansion are combined using different adder topologies:

- Design 1: n-bit Carry Look-Ahead Adder (CLA)
- Design 2: n-bit Carry-Save Adder (CSA) with 2-bit basic module
- Design 3: n-bit Carry-Save Adder (CSA) with 4-bit basic module

The UT-based architecture requires four $(\frac{n}{2} \times \frac{n}{2})$ Vedic multipliers and three n-bit adders to obtain the final 2n-bit product. The adder choice determines OC and OD of stage β .

Let $n = 2^k$, ($k \geq 2$) and $k = \log_2 n$. Using the hierarchical UT structure, the cost and delay of stage β can be written as follows.

(a) Design 1 – CLA-Based n-Bit Vedic Multiplier

In Design 1, three n-bit CLAs are used in the second stage. If the optical cost and delay of an n-bit CLA are $OC_{CLA} = 4n - 2$ and $OD_{CLA} = n\Delta$ respectively, the hierarchical UT decomposition leads to:

- Optical cost of stage β :

$$OC(\beta) = 3 \sum_{i=2}^k 4^{(k-i)} (4 \cdot 2^i - 2)$$

- Optical delay of stage β :

$$OD(\beta) = 3 \sum_{i=2}^k 2^i \Delta$$

- Total OC and OD for Design 1:

$$OC_{VM, D1} = OC(\alpha) + OC(\beta) = 2^{2 \log_2 n + 1} + 3 \sum_{i=2}^k 4^{(k-i)} (4 \cdot 2^i - 2)$$

$$OD_{VM, D1} = OD(\alpha) + OD(\beta) = 3 + 3 \sum_{i=2}^k 2^i \Delta$$

Since the adders are not designed in a reversible manner and the multiplier as a whole is not reversible, $AI = 0$, while $GO = n^2$ (due to UT structure) is used to report the effective output overhead in the proposed design family.

(b) Design 2 – CSA-Based n-Bit Multiplier (2-Bit Basic Block)

In Design 2, the partial products are summed using n-bit CSA constructed from 2-bit building blocks. For a single n-bit CSA of this type, the expressions are:

- Optical cost of n-bit CSA: $OC_{CSA2} = 5.5n - 5$
- Optical delay of n-bit CSA: $OD_{CSA2} = (0.5n + 2)\Delta$

Using the UT decomposition (four $\frac{n}{2}$ VMs + three n-bit CSAs), the accumulated cost and delay of stage β become:

- Optical cost of stage β :

$$OC(\beta) = 3 \sum_{i=2}^k 4^{(k-i)} (5.5 \cdot 2^i - 5)$$

- Optical delay of stage β :

$$OD(\beta) = 3 \sum_{i=2}^k (0.5 \cdot 2^i + 2) \Delta$$

- Total OC and OD for Design 2:

$$OC_{VM, D2} = 2^{2 \log_2 n + 1} + 3 \sum_{i=2}^k 4^{k-i} (5.5 \cdot 2^i - 5)$$

$$OD_{VM, D2} = 3 + 3 \sum_{i=2}^k (0.5 \cdot 2^i + 2) \Delta$$

Again, $AI = 0$, while $GO = n^2$ for the proposed UT-based architecture.

(c) Design 3 – CSA-Based n-Bit Multiplier (4-Bit Basic Block)

In Design 3, the summation network uses an n-bit CSA constructed from **4-bit basic modules**, which slightly increases local complexity but improves global delay.

For a single n-bit CSA using 4-bit blocks:

- Optical cost: $OC_{CSA4} = 7.25n - 9$
- Optical delay: $OD_{CSA4} = (0.25n + 3)\Delta$

Using UT decomposition, stage β parameters become:

- Optical cost of stage β :

$$OC(\beta) = 3 \sum_{i=2}^k 4^{(k-i)} (7.25 \cdot 2^i - 9)$$

- Optical delay of stage β :

$$OD(\beta) = 3 \sum_{i=2}^k (0.25 \cdot 2^i + 3) \Delta$$

- Total OC and OD for Design 3:

$$OC_{VM, D3} = 2^{2 \log_2 n + 1} + 3 \sum_{i=2}^k 4^{(k-i)} (7.25 \cdot 2^i - 9)$$

$$OD_{VM, D3} = 3 + 3 \sum_{i=2}^k (0.25 \cdot 2^i + 3) \Delta$$

As with the other designs, the structure remains irreversible; the analysis here focuses on OC and OD as the primary metrics for performance.

5.4.3 Summary of Design Trade-Offs

The analytical expressions derived above reveal a clear trade-off between optical cost and optical delay:

- **Design 1 (CLA-based)** – Lowest effective optical delay for smaller n , but adder complexity grows rapidly with bit-width. OD is moderate, OC is relatively lower than sophisticated CSA designs for small to medium N .
- **Design 2 (CSA, 2-bit block)** – Offers a balanced compromise between OC and OD. For moderate n (e.g., 8, 16, 32 bits), this design often gives the best joint optimization of delay and cost, as also observed in comparative plots.
- **Design 3 (CSA, 4-bit block)** – Achieves the lowest optical delay among the three, especially for larger n , at the expense of higher OC due to the more complex 4-bit CSA blocks.

The numerical evaluation of these expressions for $n = 2, 4, 8, 16, 32, 64$, and 128 —summarized in the comparison tables and plotted in logarithmic scale—confirms that Design 2 is generally the most favourable in terms of both OC and OD for practical bit-widths, while Design 3 becomes competitive for very large n where delay dominates the design criteria.

These analytical insights serve as the baseline for the next sections, where the proposed RSOA-based fully reversible n -bit multipliers are introduced and their OC/OD characteristics are compared with the MZI-SOA designs

Table 5.1: Design parameters of All-optical SOA-MZI based n -bit multipliers.

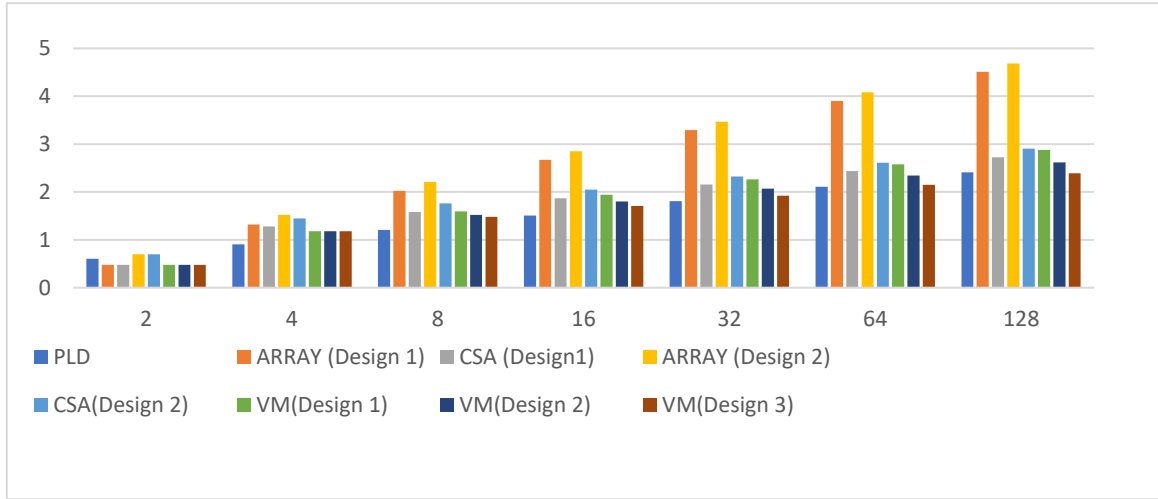
Parameter		N_{AI}	N_{GO}	$OC_{(N_{MZI})}$	$OD_{(\Delta)}$
PLD Multiplier [46]		0	0	$2^{2n} - 1$	$2n$
Array Multiplier [50]	Design1	0	$3n^2 - 4n$	$5n^2 - 6n$	$2n^2 - 3n + 1$
	Design2	$3n^2 - 4n$	$5n^2 - 7n$	$11n^2 - 16n$	$3n^2 - 4n + 1$
CSA Multiplier [50]	Design1	0	$n^2 + 2[(\frac{2}{3})^{\log_2(\frac{n}{2})} n^2] + 8n$	$n^2 + 8[(\frac{2}{3})^{\log_2(\frac{n}{2})} n^2] + 8n$	$4n + 2\log_3(\frac{n}{2}) + 1$
	Design2	$6[(\frac{2}{3})^{\log_2(\frac{n}{2})} n^2] + 6n$	$n^2 + 8[(\frac{2}{3})^{\log_2(\frac{n}{2})} n^2] + 8n$	$n^2 + 20[(\frac{2}{3})^{\log_2(\frac{n}{2})} n^2] + 20n$	$6n + 3\log_3(\frac{n}{2}) + 1$
MZI-SOA based n -bit Vedic Multiplier (proposed work) [132]	Design1	0	n^2	$2^{2\log_2 n + 1} + 3 \sum_{i=2}^k 4^{k-i} (4 * 2^i - 2)$	$3 + 3 \sum_{i=2}^k 2^i$
	Design2	0	n^2	$2^{2\log_2 n + 1} + 3 \sum_{i=2}^k 4^{k-i} (5.5 * 2^i - 5)$	$3 + 3 \sum_{i=2}^k (0.5 * 2^i + 2)$
	Design3	0	n^2	$2^{2\log_2 n + 1} + 3 \sum_{i=2}^k 4^{k-i} (7.25 * 2^i - 9)$	$3 + 3 \sum_{i=2}^k (0.25 * 2^i + 3)$

5.5 Design of RSOA-Based Fully Reversible N-Bit Vedic Multiplier

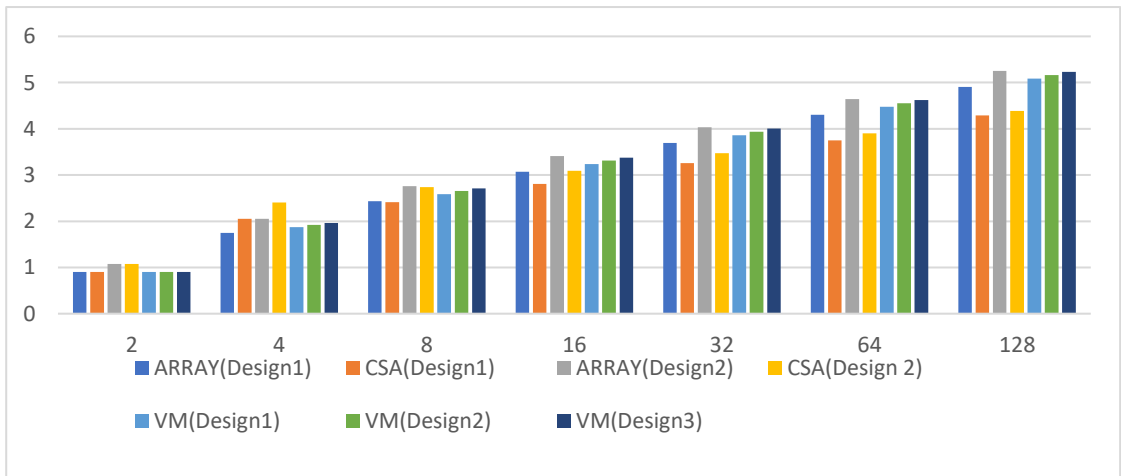
While the MZI-SOA-based n-bit Vedic multipliers discussed in Section 5.4 achieve high-speed all-optical multiplication, they remain irreversible and rely on interferometric structures that are sensitive to phase, polarization, and fabrication imperfections. To overcome these limitations and move towards information-preserving, interferometer-free photonic architectures, this section presents the design of an RSOA-based fully reversible $n \times n$ Vedic multiplier.

The proposed architecture has two main goals:

1. Eliminate interferometric paths by using only RSOA-based switching elements (no MZI arms), improving robustness and integration potential.
2. Ensure logical reversibility by constructing the multiplier entirely from reversible optical gates and reversible adder blocks, thereby preserving one-to-one input-output mapping and avoiding information loss.



(a) Optical Delay



(b) Optical Cost

Figure 5.2: Graphical comparison of (a) Optical Delay, and (b) Optical cost of all-optical n-bit multipliers in log10 scale.

Table 5.2: Comparative results of All-optical MZI-SOA based n-bit multipliers

	n-bit	2	4	8	16	32	64	128
OD	PLD [22]	4	8	16	32	64	128	256
	ARRAY (Design 1) [23]	3	21	105	465	1953	8001	32385
	CSA (Design1) [23]	3	19	38	74	143	273	532
	ARRAY (Design 2) [23]	5	33	161	705	2945	12033	48641
	CSA (Design 2) [23]	5	28	58	112	211	409	799
	VM (Design 1)	3	15	39	87	183	375	759
	VM (Design 2)	3	15	33	63	117	219	417
	VM (Design 3)	3	15	30	51	84	141	246
	n-bit	2	4	8	16	32	64	128
OC	PLD [22]	15	255	65535	4294967326	1.8×10^{19}	3.4×10^{38}	1.55×10^{77}
	ARRAY (Design 1) [23]	8	56	272	1184	4928	20096	81152
	CSA (Design 1) [23]	8	112	257	643	1801	5656	19514
	ARRAY (Design 2) [23]	12	112	576	2560	10752	44032	178176
	CSA (Design 2) [23]	12	256	547	1225	2968	7996	24210
	VM (Design 1)	8	74	386	1730	7298	29954	121346
	VM (Design 2)	8	83	449	2045	8693	35813	145349
	VM (Design 3)	8	92	515	2381	10193	42137	171305
	n-bit	2	4	8	16	32	64	128

The n-bit reversible multiplier is constructed hierarchically using the Urdhva–Tiryagbhyam (UT) Vedic multiplication algorithm, similar in structure to the quantum design of Chapter 3 but realized here in the optical domain using RSOA-based reversible gates, proposed reversible ripple-carry adders (RCA), and reversible carry-save adders (CSA).

5.5.1 Architectural Overview

The proposed RSOA-based $n \times n$ -bit reversible multiplier follows the same conceptual decomposition as the UT algorithm:

- At the lowest level, a 2×2 reversible Vedic multiplier is realized using RSOA-based Toffoli and Peres gates.
- Four 2×2 blocks are combined to obtain a 4×4 reversible Vedic multiplier.
- Higher-order $n \times n$ multipliers are obtained recursively by partitioning n-bit operands into $\frac{n}{2}$ -bit segments and reusing the lower-order blocks.

For an n-bit operand, where n is a power of two ($n \geq 4$), the UT algorithm yields a modular hierarchical structure.:

- Partial Product Stage (UT structure):
Four $\left(\frac{n}{2}\right) \times \left(\frac{n}{2}\right)$ reversible multipliers generate lower, intermediate, and higher partial products.
- Summation Stage (Adder Network):
Proposed RSOA-based reversible RCA and CSA blocks are used to sum these partial products in a parallel, reversible fashion.

This hierarchical structure is repeated over $\log_2 \left(\frac{n}{4} \right) + 1$ levels, starting from 4×4-bit up to the final n×n bit multiplier. At each level, both the number of building blocks and the number of adders increase in a regular, Vedic-friendly pattern, enabling closed-form expressions for optical cost, delay, and reversibility metrics.

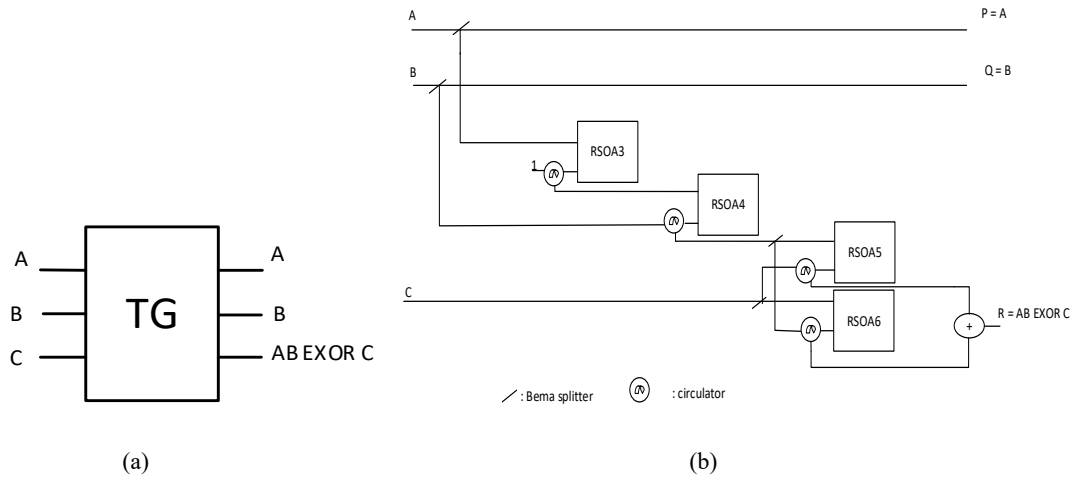


Figure 5.3: RSOA-based Toffoli (TG) gate realizing controlled AND and signal duplication (OC = 4, OD = 3Δ)

5.5.2 Reversible Optical Building Blocks

The RSOA-based n-bit multiplier is built entirely from reversible optical logic modules, ensuring strict bijective behaviour:

- **RSOA-based 2-bit multiplier using Toffoli (TG) and Peres (PG) gates**
 - Used for fan-out, XOR/AND generation, and 2×2 Vedic multiplication (Chapter 4).
 - Implemented via cross-gain modulation (XGM) in RSOAs, using probe/control signal configurations.
 - OC=28, OD=12Δ, CI and GO = 6

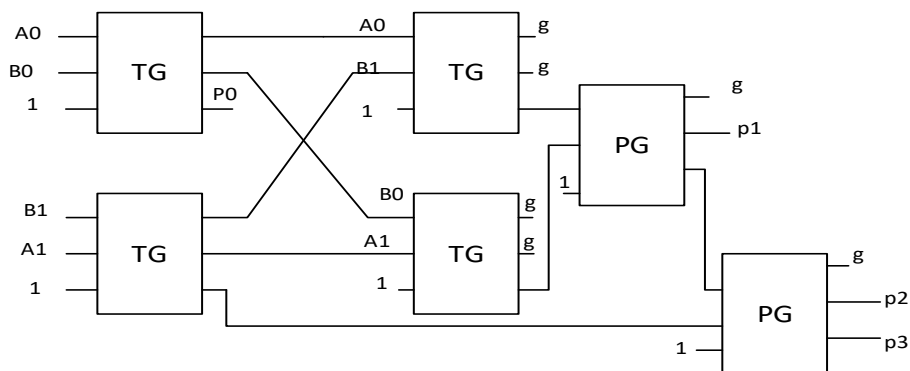


Figure 5.4: Block diagram of 2*2-bit reversible Vedic multiplier

- **Proposed RSOA-based Reversible Ripple-Carry Adder (RCA)**

- Realized using combinations of PG gates work as full adder.
- Performs reversible addition of partial products with minimal garbage outputs and constant inputs.

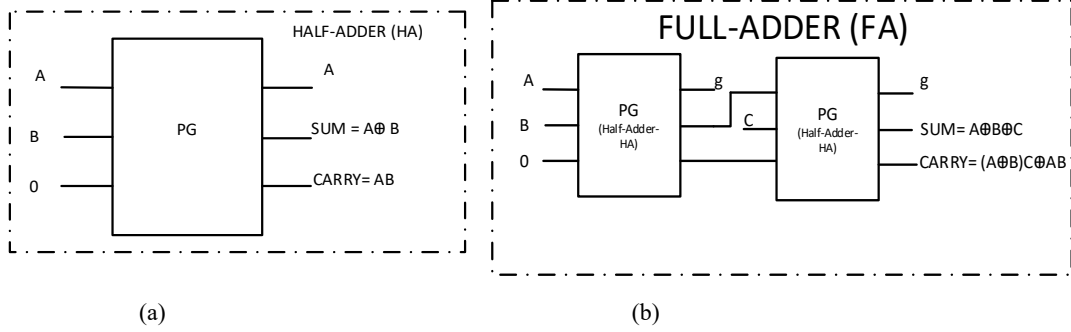


Figure 5.5: (a) Half-Adder (PG gate): - OC: 6, OD:3 Δ, CI:1, GO:1; (b) Full-Adder (2 PG gate): - OC: 12, OD:6 Δ, CI:1, GO:2

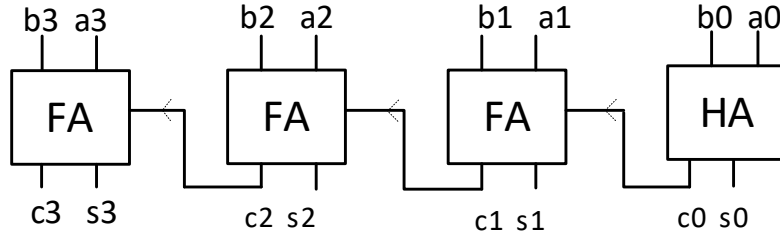


Figure 5.6: Block diagram of the 4-bit all-optical reversible ripple carry adder: OC:34, OD:17 Δ, CI:10, GO:13.

- Performance metrics for n-bit RCA:

$$\text{Optical Cost: } OC_{RCA} = OC_{HA} + (n - 1)OC_{FA} = 6 + 12(n - 1) = 12n - 6$$

$$\text{Optical Delay: } OD_{RCA} = OD_{HA} + (n - 1)OD_{FA} = 3 + 6(n - 1) = (6n - 3)$$

$$\text{Constant Inputs: } CI_{RCA} = CI_{HA} + (n - 1)CI_{FA} = 1 + (n - 1) = n$$

$$\text{Garbage Outputs: } GO_{RCA} = GO_{HA} + (n - 1)GO_{FA} = 1 + 2(n - 1) = 2n - 1$$

- **Proposed RSOA-based Reversible Carry-Save Adder (CSA)**

- Designed as a modular building block for multi-operand addition.
- Utilizes RSOA-based reversible full/half adders to generate sum and carry bits without information loss.
- Employed in intermediate UT levels to reduce delay while preserving reversibility.

- Performance metrics of n-bit CSA:

$$\text{Optical Cost: } OC_{CSA} = 2n \cdot OC_{FA} - OC_{HA} = 24n - 6$$

$$\text{Optical Delay: } OD_{CSA} = OD_{FA}^{(\text{stage1})} + OD_{FA}^{(\text{stage2})} + OD_{HA} = 6 + 6(n - 1) + 3 = (6n + 3)\Delta$$

$$\text{Constant Inputs: } CI_{CSA} = (2n - 1)CI_{FA} + CI_{HA} = 2n$$

$$\text{Garbage Outputs: } GO_{\text{CSA}} = (2n - 1)GO_{\text{FA}} + GO_{\text{HA}} = 4n - 1$$

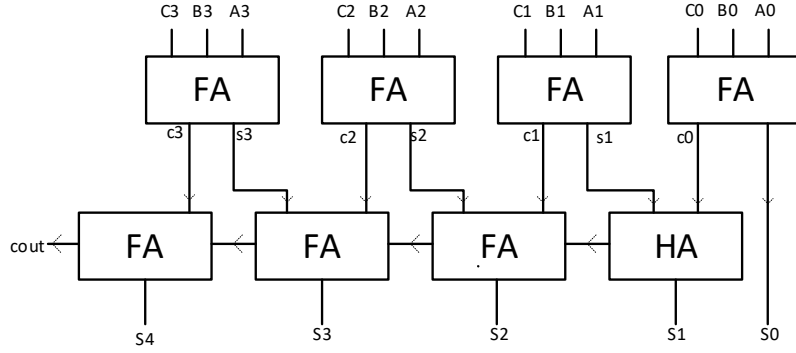


Figure 5.7: Block diagram of 4-bit CSA: OC:74, OD:22 Δ, CI:22, GO:29

Each of these modules is synthesized entirely from RSOA switches, beam splitters, and combiners, with no interferometric paths. As a consequence:

- The architecture is interferometer-free.
- All intermediate signals remain accessible, ensuring a fully reversible optical mapping.
- Garbage outputs (GO) and constant inputs (CI) arise only from reversible gate constraints, not from interferometric constraints.

5.5.3 UT-Based Reversible $n \times n$ Architecture Using RSOA

Let the two n -bit input operands be:

$$A = A_{n-1} \dots A_1 A_0, B = B_{n-1} \dots B_1 B_0,$$

with n chosen as a power of 2. The UT-based reversible architecture proceeds as:

1. Base Level (4×4 Reversible Vedic Multiplier):

- Built from four 2×2 -bit RSOA-based reversible multipliers (Chapter 4) and proposed RSOA-based reversible RCA/CSA blocks.
- This 4×4 unit forms the basic recursive block for constructing higher-order multipliers.

2. Recursive Expansion to N Bits:

- For each higher level, an $n \times n$ reversible multiplier is synthesized using four $\left(\frac{n}{2}\right) \times \left(\frac{n}{2}\right)$ reversible multipliers:

$$\text{— } P_0 = A_L \times B_L$$

$$\text{— } P_1 = A_H \times B_L$$

$$\text{— } P_2 = A_L \times B_H$$

$$\text{— } P_3 = A_H \times B_H$$

- where $A = (A_H, A_L)$ and $B = (B_H, B_L)$ are divided into high and low halves.

3. Reversible Partial Product Summation:

- Proposed RSOA-based reversible CSA blocks combine:
 - P_0 and shifted terms $(P_1 + P_2) \ll \left(\frac{n}{2}\right)$,
- Proposed RSOA-based reversible RCA blocks perform final carry propagation by adding:
 - $P_3 \ll n$ to the accumulated intermediate sum.
- All intermediate outputs are preserved as either:
 - primary outputs, or
 - garbage outputs required for reversibility (and can potentially be reused in larger systems).

Through this structure, every input bit pattern maps uniquely to an output bit pattern plus a well-defined set of garbage outputs, ensuring complete reversibility in the optical domain.

5.5.4 Complexity Analysis of RSOA-Based Reversible n-Bit Vedic Multiplier

To quantify the efficiency of the proposed RSOA-based reversible $n \times n$ multiplier, four metrics are evaluated:

- Optical Cost (OC): total number of RSOA switches used.
- Optical Delay (OD): maximum number of cascaded RSOA stages along the critical path (in units of Δ).
- Constant Inputs (CI): number of ancilla inputs fixed to logical '0' or '1'.
- Garbage Outputs (GO): number of auxiliary outputs preserved for reversibility but not used as primary outputs.

Let:

$$m = \log_2 \left(\frac{n}{4} \right),$$

so that the hierarchy progresses from 4×4 to $n \times n$ over $m + 1$ levels.

Using the recursive UT structure and the proposed RSOA-based RCA/CSA blocks, the design parameters of the n -bit reversible RSOA-based Vedic multiplier can be expressed as:

- Optical Cost (OC):

$$OC_{\text{RSOA}}(n) = 4^{(m+1)} \cdot 28 + 4n + \sum_{i=0}^m 4^i \left[36 \left(\frac{n}{2^i} \right) - 12 \right]$$

- Optical Delay (OD):

$$OD_{\text{RSOA}}(n) = \left\{ 12 + \sum_{i=0}^m 12 \left(\frac{n}{2^i} \right) \right\} \Delta$$

- Constant Inputs (CI):

$$CI_{\text{RSOA}}(n) = 4^{(m+1)} \cdot 6 + 2n + \sum_{i=0}^m 4^i \left[3 \left(\frac{n}{2^i} \right) \right]$$

- Garbage Outputs (GO):

$$GO_{\text{RSOA}}(n) = 4^{(m+1)} \cdot 6 + \sum_{i=0}^m 4^i \left[6 \left(\frac{n}{2^i} \right) - 2 \right]$$

These expressions capture:

- The $4^{(m+1)}$ terms, corresponding to the total number of 4×4 (and recursively smaller) Vedic multiplier blocks at all levels.
- The summation terms, which arise from the proposed RSOA-based reversible RCA and CSA networks used at each level to combine partial products.
- The linear dependence on n inside the summations, reflecting the width of adders at each level.

For small n (e.g., $n = 4, 8, 16$), these expressions reduce to manageable values and can be tabulated; for larger n , they provide insight into the asymptotic growth of cost, delay, and reversibility-related overhead.

5.5.5 Discussion

Compared to the SOA–MZI-based n -bit Vedic multipliers of Section 5.4, the proposed RSOA-based design exhibits several important qualitative differences:

- **Reversibility:** The RSOA-based architecture is fully reversible by construction, with explicitly bounded CI and GO. In contrast, the MZI-based designs are irreversible and do not preserve all intermediate information.
- **Interferometer-Free Operation:** By eliminating interferometric arms, the design avoids phase-matching, thermal drift, and polarization sensitivity issues inherent in MZI-based circuits, thereby improving robustness and fabrication tolerance.
- **Structured Resource Growth:** Although the RSOA-based multiplier incurs non-trivial OC, CI, and GO overhead due to reversibility, the growth follows a regular, hierarchical pattern determined by the UT algorithm and the recursive 4×4 building block. This makes the design amenable to optimization and mapping onto photonic integrated circuits.
- **Suitability for Quantum-Compatible Optical Systems:** Since the architecture is reversible and information-preserving, it aligns better with the requirements of

quantum-compatible optical computing and energy-aware photonic processors, where information erasure and associated Landauer dissipation must be minimized.

5.6 Comparative Evaluation of SOA–MZI and RSOA-Based n-Bit Multipliers

This section presents a comprehensive comparative analysis between the two multiplier architectures developed in this research:

- (1) MZI-SOA based all-optical n-bit Vedic multipliers (Designs 1–3), and
- (2) RSOA-based fully reversible n-bit Vedic multipliers.

The comparison is performed across key design parameters including optical cost (OC), optical delay (OD), constant inputs (CI), garbage outputs (GO), reversibility, scalability, and signal integrity. This evaluation highlights the practical advantages of the proposed RSOA-based architecture while also acknowledging trade-offs that emerge in the transition toward reversible photonic computing.

5.6.1 Comparison of Optical Delay (OD)

For the MZI-SOA multipliers, optical delay increases with the number of interferometric stages in the critical path.

- MZI-based Designs 1–3 show OD increases with n due to cascaded adder stages and hierarchical UT-based partial product generation.
- Design 3 (CSA–4-bit block) provides the smallest OD among MZI designs because of shallower addition depth.

In contrast, the RSOA-based multiplier exhibits delay growth primarily due to:

- the hierarchical recursive UT decomposition, and
- the number of RSOA gates in the longest path.

However, because RSOA switching is interferometer-free, OD growth is more predictable and structured with respect to UT recursion depth.

For example:

- 2-bit reversible multiplier: $OD = 12\Delta$
- Higher-bit multipliers: OD follows the expression:

$$OD = 12 + \sum_{i=0}^{\log_2\left(\frac{n}{4}\right)} 12\left(\frac{n}{2^i}\right)\Delta$$

Although OD is generally higher than MZI-based Design 3 for small n, it becomes more stable for large n because RSOA paths do not accumulate phase errors or interferometric drift.

Key Insight: MZI-based multipliers are faster for small n due to shallow interferometric stages, but RSOA-based multipliers become more reliable and scalable for large n .

5.6.2 Comparison of Optical Cost (OC)

The optical cost in MZI-based designs is dominated by:

- MZI count,
- beam splitters/combiners,
- additional stages required for adders (CLA/CSA).

Trends show:

- Design 1 (CLA): moderate OC
- Design 2 (CSA–2bit block): higher OC
- Design 3 (CSA–4bit block): highest OC but lowest OD

For large n , MZI count grows rapidly due to interferometer duplication, leading to rapid growth in optical cost.

The RSOA-based design has optical cost governed by the expression:

$$OC = 4^{\left(\log_2\left(\frac{n}{4}\right)+1\right)} \cdot 28 + 4n + \sum_{i=0}^{\log_2\left(\frac{n}{4}\right)} 4^i \left[36 \left(\frac{n}{2^i} \right) - 12 \right]$$

Although OC is comparatively high due to reversible gate structures, it remains more scalable and predictable because:

- No beam splitters/combiners are required,
- No interferometer duplication is involved,
- RSOA gates scale uniformly with UT hierarchy.

Key Insight: RSOA-based multipliers incur higher gate count but avoid the exponential OC growth associated with cascading interferometers.

5.6.3 Reversibility, CI, and GO Comparison

MZI-based multipliers lose information during addition and partial product generation, making them unsuitable for thermodynamically efficient or quantum-compatible computing.

RSOA-based multipliers use reversible RCA, and CSA designs, ensuring:

- bijective input–output mapping,
- structured and bounded garbage outputs compared to non-modular reversible architectures,
- compatibility with future optical–quantum co-processors.

Key Insight: Only the RSOA-based multiplier preserves information, making it suitable for reversible and quantum-inspired computing frameworks

5.6.4 Signal-Quality Performance (Qualitative Assessment)

Although this work does not explicitly compute optical parameters such as extinction ratio (ER), Q-factor, or return-to-zero output probability (REOP), a qualitative comparison can still be made based on the inherent physical behaviour of the switching mechanisms.

MZI-SOA based multipliers rely on interferometric configurations. Their output quality is governed by:

- differential phase shifts between the two arms,
- gain saturation behaviour of SOAs,
- accumulated amplified spontaneous emission (ASE) noise,
- polarization dependence,
- sensitivity to thermal and fabrication variations.

As a result, signal degradation (crosstalk, reduced contrast, amplitude drift) tends to increase with bit-width because more cascaded interferometers introduce compounding phase errors.

In contrast, the proposed RSOA-based architecture uses single-ended XGM switching, which inherently avoids interferometric imbalance. This leads to superior qualitative signal behaviour due to:

- absence of phase-sensitive components,
- reduced susceptibility to thermal drift,
- lower accumulation of ASE noise compared to dual-arm MZI structures,
- more stable on–off gating response,
- simpler optical path and depth.

Thus, even though quantitative metrics were not evaluated, the RSOA-based design is expected to exhibit better stability, less distortion, and more predictable switching behaviour than its MZI–SOA counterparts, particularly as multiplier size increases.

Key Insight: RSOA-based multipliers provide inherently cleaner and more stable optical switching because they eliminate interferometric effects, even though numerical optical performance parameters are not calculated in this work.

5.6.5 Scalability and Practical Integration

MZI-SOA multipliers

- employ UT-based hierarchical expansion but rely on interferometric MZI structures,
- scale poorly due to duplication of interferometers, leading to increased optical loss, thermal sensitivity, and phase instability at higher bit-widths,

- require precise phase and path-length control, making large-scale integration challenging,
- become less suitable for dense photonic integration beyond moderate complexity.

RSOA-based multipliers

- employ the same UT-based hierarchical structure, but realize it using interferometer-free, intensity-modulated RSOA switches,
- exhibit improved scalability due to the absence of alignment-sensitive interferometric arms,
- offer greater fabrication tolerance and operational robustness at larger bit-widths,
- are more compatible with monolithic photonic integration platforms and scalable optical ALUs.

Key Insight: Although both architectures utilize the UT algorithm for hierarchical multiplication, the interferometer-free nature of RSOA-based switching enables more robust, scalable, and integration-friendly implementations, making RSOA-based multipliers a more practical choice for large-bit photonic arithmetic systems.

5.6.6 Summary of Comparative Findings

The comparative study between MZI-SOA-based and RSOA-based all-optical n-bit multipliers leads to the following observations:

1. MZI-SOA-based multipliers can achieve lower optical delay for small bit-widths due to shallow interferometric stages; however, their scalability is limited by interferometer duplication, phase sensitivity, thermal drift, and inherent irreversibility.
2. RSOA-based multipliers enable fully reversible optical computation by construction, making them more suitable for energy-efficient and quantum-compatible photonic computing paradigms where information preservation is essential.
3. The interferometer-free nature of RSOA-based architectures eliminates critical issues associated with MZI structures, such as phase noise, path-length mismatch, and polarization sensitivity, thereby improving robustness and fabrication tolerance.
4. Although quantitative signal-quality metrics such as extinction ratio (ER), Q-factor, and relative eye-opening percentage (REOP) are not explicitly evaluated for the n-bit architectures in this chapter, the use of single-ended XGM-based RSOA switching is expected to provide more stable and predictable signal behaviour than interferometric MZI-SOA implementations, particularly as the multiplier size increases.

5.7 Summary of the Chapter

This chapter presented a comprehensive design and analytical evaluation of all-optical n -bit multipliers implemented using two distinct switching technologies: MZI-SOA interferometric switches and RSOA-based interferometer-free reversible switches. The work was structured in two phases to address both the limitations of existing optical multiplier architectures and the growing need for scalable, energy-efficient photonic computing solutions.

In Phase I, three MZI-SOA-based n -bit Vedic multipliers (Design 1, Design 2, and Design 3) were developed using existing carry look-ahead (CLA) and carry-save adder (CSA) architectures reported in the literature. These designs demonstrated clear trade-offs between optical cost and optical delay, which are characteristic of interferometer-based implementations. While functional correctness was ensured and significant variation in cost–delay behaviour was observed across different adder choices, all three designs remained irreversible, rendering them thermodynamically inefficient and unsuitable for lossless optical computing in accordance with Bennett’s reversibility principle. A portion of the work presented in Phase I, focusing on MZI-SOA-based n -bit Vedic multipliers and their optical cost–delay trade-offs, has been published in the IEEE International Conference on Emerging Technology (INCET).

In Phase II, a fully reversible all-optical N -bit Vedic multiplier based on RSOA switching was proposed. Unlike MZI-SOA architectures, the RSOA-based design operates without interferometers and leverages cross-gain modulation (XGM), resulting in a compact, stable, and interferometer-free realization that is less susceptible to phase errors, thermal drift, and alignment constraints. New reversible optical adder architectures, including reversible RCA and CSA variants, were developed and integrated with the Urdhva–Tiryagbhyam multiplication framework. Analytical evaluation demonstrated predictable scalability in optical cost, optical delay, constant inputs, and garbage outputs, confirming the suitability of the proposed architecture for large-bit photonic arithmetic implementations.

A comparative assessment of both phases revealed that:

- MZI-SOA-based multipliers can offer lower optical delay for certain bit-widths but suffer from irreversibility, increased optical cost, and scalability limitations due to interferometric dependencies.
- RSOA-based multipliers, although incurring higher optical cost due to reversible gate overhead, provide true logical reversibility, improved structural robustness, and enhanced suitability for scalable, low-energy, and quantum-compatible photonic computing systems.

Overall, this chapter established the inherent limitations of interferometer-based optical multipliers and highlighted the advantages of RSOA-driven reversible photonic architectures. The presented results provide a strong foundation for subsequent extensions toward higher-order arithmetic units and integrated reversible optical computing platforms.

Chapter 6: All-optical Complex Multiplier

6.1 Introduction

The design of high-performance arithmetic units in the optical domain has gained increasing relevance with the rapid emergence of photonic processors and energy-aware computing architectures. While the preceding chapters established reversible logic foundations and presented all-optical implementations of real-valued and N-bit multipliers, many practical signal-processing and communication systems require arithmetic operations on complex numbers. Applications such as FFT/DFT processing, adaptive filtering, MIMO communication, and advanced modulation schemes critically depend on efficient complex multiplication.

In Chapter 3, a reversible complex multiplier was developed in the quantum domain, demonstrating the feasibility of Vedic-mathematics-based complex arithmetic using reversible logic gates. Building on the same algorithmic structure and design philosophy, the present chapter extends this framework to the optical domain, where physical constraints such as optical cost, delay, and signal integrity must be explicitly considered.

In conventional electronic systems, complex multiplication is realized using multiple real multipliers along with several addition and subtraction operations. Translating this structure into an all-optical and reversible framework is non-trivial, as it requires careful coordination of arithmetic and logic operations while preserving reversibility and controlling circuit overhead in terms of optical resources.

Motivated by these challenges, this chapter presents an all-optical reversible complex multiplier architecture based on the Urdhva–Tiryagbhyam (UT) Vedic algorithm, implemented using RSOA-based reversible and parity-preserving logic gates where appropriate. In contrast to earlier chapters that focused on real-valued multiplication, this chapter specifically addresses the additional complexity introduced by complex arithmetic in the optical domain.

The scope of this chapter is threefold:

1. Design and simulation of a 2×2 -bit all-optical reversible Vedic multiplier using parity-preserving RSOA-based logic gates, which serves as the fundamental building block for complex multiplication. The proposed 2×2 design is simulated and compared with state-of-the-art optical multiplier implementations, and its signal quality is evaluated in terms of extinction ratio (ER), Q-factor, and relative eye-opening percentage (REOP) at each output.
2. Construction of a reversible optical complex multiplier architecture using the same structural methodology adopted in Chapter 3, but realized entirely in the optical domain

using RSOA-based switching. While the quantum design employed reversible (but not parity-preserving) gates, the optical realization emphasizes parity preservation to enhance fault tolerance.

3. Analytical derivation of n -bit performance expressions for the proposed complex Vedic multiplier, including optical cost (OC), optical delay (OD), garbage outputs (GO), and constant inputs (CI). The n -bit complex multiplier is not fully simulated optically; instead, closed-form expressions are derived to establish scalability and design trends.

The optical implementation primarily relies on RSOA-based cross-gain modulation (XGM), ensuring interferometer-free, compact, and stable operation. In addition, a universal reversible NAND–NOR logic gate, realized using a hybrid MZI–SOA and RSOA switching mechanism, is introduced as a supporting logic primitive. This gate is presented to demonstrate functional completeness and design flexibility but is not directly employed in the complex multiplier architectures developed in this chapter.

Through this approach, the chapter bridges the gap between reversible complex arithmetic in the quantum domain and its realization in practical all-optical systems, highlighting the feasibility, scalability, and signal-level performance of reversible optical complex multipliers for next-generation photonic computing.

6.2 Key Contributions

The core contributions of this research to **all-optical reversible complex arithmetic** are summarized as follows.

1. Universal Reversible NTG Gate

- A novel reversible universal logic gate (NTG) is introduced, capable of performing NAND and NOR operations within a single gate structure.
- The gate is optically realized using a hybrid MZI–SOA and RSOA switching mechanism, exploiting the complementary nonlinear characteristics of interferometric and XGM-based devices.
- Since NAND and NOR together constitute a functionally complete logical set, the proposed NTG gate provides a flexible foundation for constructing reversible optical logic circuits.
- Other Boolean functions such as AND, OR, XOR, and NOT can be derived through appropriate configurations of the NTG gate, demonstrating its versatility as a universal reversible logic primitive.

- The NTG gate is introduced as a supporting contribution to establish universality and design flexibility and is not directly employed in the complex multiplier architectures presented in this chapter.

2. Reversible Parity-Preserving 2-Bit Multiplier

- A 2×2-bit reversible multiplier that preserves input–output parity is introduced, enabling fault detection and enhanced reliability, which are critical for future photonic processors.
- The multiplier is constructed using parity-preserving RSOA-based reversible logic gates, including:
 - Double Feynman Gate (DFG) for controlled signal duplication and XOR generation,
 - Parity-Preserving Toffoli Gate (PPTG) for conditional partial product generation, and
 - Modified Islam Gate (MIG) as an efficient reversible adder building block.
- This 2×2 parity-preserving multiplier serves as the fundamental building block for the formulation of higher-order and complex multiplier architectures.

3. Reversible n-Bit Complex Vedic Multiplier Architecture

- A reversible complex multiplier architecture is formulated using the Urdhva–Tiryagbhyam (UT) Vedic algorithm, enabling parallel generation and accumulation of partial products.
- The complex multiplication:

$$(a + jb)(c + jd) = (ac - bd) + j(ad + bc)$$

is realized using:

- four reversible real multipliers,
 - one reversible adder, and
 - one reversible subtractor.
- While the 2×2 parity-preserving multiplier is implemented and simulated optically, the N-bit complex multiplier is developed analytically, and closed-form expressions are derived to evaluate optical cost (OC), optical delay (OD), constant inputs (CI), and garbage outputs (GO).
- This formulation establishes the scalability and feasibility of reversible complex arithmetic in the optical domain without incurring the computational overhead of full n-bit optical simulation.

4. Performance Evaluation

- A detailed performance evaluation is carried out for the 2×2-bit parity-preserving reversible multiplier, which forms the core arithmetic unit for complex multiplication.
- Optical signal integrity metrics, including extinction ratio (ER), Q-factor, and relative eye-opening percentage (REOP), are extracted using RSOA rate-equation-based simulation for each output.
- For higher-bit complex multipliers, performance assessment is conducted through analytical evaluation of OC, OD, CI, and GO, providing insight into scalability trends and architectural efficiency.

6.3 Proposed All-Optical Reversible Building Blocks

6.3.1 Universal Reversible NAND–NOR Gate (NTG)

Reversible logic literature lacks a single universal gate capable of generating both NAND and NOR functions within the same reversible framework. Since NAND and NOR operations form the foundation for realizing all classical Boolean functions, their reversible optical mappings are essential for building more flexible and compact logic processors. Motivated by this gap, we propose a new reversible universal gate—referred to as the NTG—capable of implementing NAND, NOR, and all derived Boolean functions such as AND, OR, XOR, and XNOR.

The NTG is constructed using a hybrid switching architecture combining MZI–SOA interferometric elements with RSOA-based XGM switches. This hybrid configuration enables the gate to achieve controlled gain modulation and phase-dependent switching necessary for realizing reversible optical NAND/NOR behaviour. [133].

Although this gate is not utilized in the final design of the proposed complex multiplier, its introduction serves an important conceptual purpose. The NTG establishes the feasibility of mapping traditionally irreversible universal Boolean operations into an all-optical reversible domain. Thus, it can be employed as a fundamental block in future designs of reversible optical ALUs, control circuits, and programmable logic networks. Figure 6.1 shows the optical mapping of the gate and Table 6.1 demonstrate the operation of the gate.

By proposing this gate, the work fills a notable literature gap and provides a reusable universal primitive for reversible photonic logic synthesis.

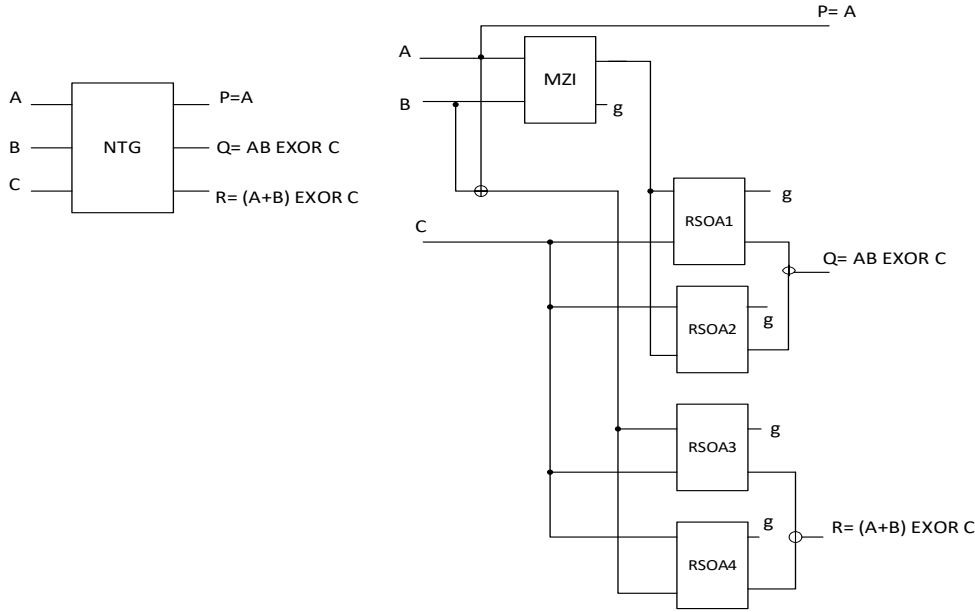


Figure 6.1:Block diagram of NTG and optical mapping of NTG with MZI-SOA switch and RSOA-switch

Table 6.1: Logical operation of NTG Gate

RSOA	Probe Signal Input	Control Signal Input	Output
MZI-SOA	'A'	'B'	'AB'
RSOA1	'C'	'AB'	' $\overline{A}BC$ '
RSOA2	'AB'	'C'	' $\overline{C}AB$ '
RSOA3	'C'	'A+B'	' $\overline{A} + \overline{B}C$ '
RSOA4	'A+B'	'C'	' $\overline{C}A + B$ '
OUTPUTS $P = A$ $Q = \text{RSOA1} + \text{RSOA2} = AB \oplus C$ $R = \text{RSOA3} + \text{RSOA4} = (A+B) \oplus C$			

6.4 Parity-Preserving 2×2-Bit Reversible Optical Vedic Multiplier

The design of the complex all-optical multiplier developed in this chapter relies on a compact, fault-tolerant 2×2-bit reversible multiplier as its fundamental building block. In contrast to the 2×2-bit RSOA-based multiplier of Chapter 4 (which focused on basic reversibility), the circuit considered here additionally enforces parity preservation, thereby enabling intrinsic error detection. This 2×2 cell is later used as the fundamental architectural building block within the proposed all-optical complex Vedic multiplier, together with the reversible unified adder–subtractor (UAS) and other arithmetic modules.

The architecture is implemented entirely in the optical domain using Reflective Semiconductor Optical Amplifier (RSOA) switches operating in the cross-gain modulation (XGM) regime. At the logical level, the multiplier is constructed from three parity-preserving reversible gates:

- **Double Feynman Gate (DFG)** – used for reversible fan-out and XOR generation,

- **Parity-Preserving Toffoli Gate (PPTG)** – used for partial product generation, and
- **Modified Islam Gate (MIG)** – used as a compact parity-preserving half-adder block.

Together, these gates realize a 2×2 Vedic-style multiplier that follows the Urdhva–Tiryagbhyam (UT) “vertical and crosswise” multiplication pattern while preserving both reversibility and parity at every stage.

6.4.1 Design Principles and Role in the Complex Multiplier

The 2×2 multiplier is designed with two complementary goals:

1. **Architectural suitability for Vedic scaling:** The internal structure follows the UT algorithm, where partial products are generated in parallel and then combined using simple adders. This makes the 2×2 cell directly reusable as a basic Vedic block when constructing higher bit-width multipliers and the n -bit complex Vedic multiplier.
2. **Parity preservation and fault awareness:** All constituent gates (DFG, PPTG, MIG) are parity-preserving. Hence, the overall 2×2 multiplier maintains the same parity at its outputs as at its inputs. This property allows an external parity checker to detect single-bit errors without modifying the internal multiplier architecture. When the 2×2 unit is replicated in the complex multiplier, this parity consistency propagates through the hierarchy, providing a natural layer of fault monitoring.

Within the complex multiplier proposed later in this chapter, this 2×2 block acts as the primitive multiplication cell, while the UAS and other reversible adders perform accumulation and subtraction of real and imaginary partial products.

6.4.2 Gate-Level Realization Using DFG, PPTG and MIG

The 2×2 parity-preserving multiplier uses a structured combination of DFG, PPTG and MIG gates, all mapped onto RSOA-based XGM switches.

- **Double Feynman Gate (DFG):** The DFG is a 3×3 parity-preserving gate with input vector (A, B, C) and output vector (P, Q, R) defined as:

$$P = A, Q = A \oplus B, R = A \oplus C.$$

In this work, the DFG is employed as a reversible fan-out element: the primary input bits A_1, A_0, B_1, B_0 are replicated and distributed to multiple subsequent gates without violating the no-fan-out constraint of reversible logic. When the auxiliary inputs are fixed to logic ‘0’, DFG effectively produces parity-preserving copies and XOR combinations required by the multiplier data path.

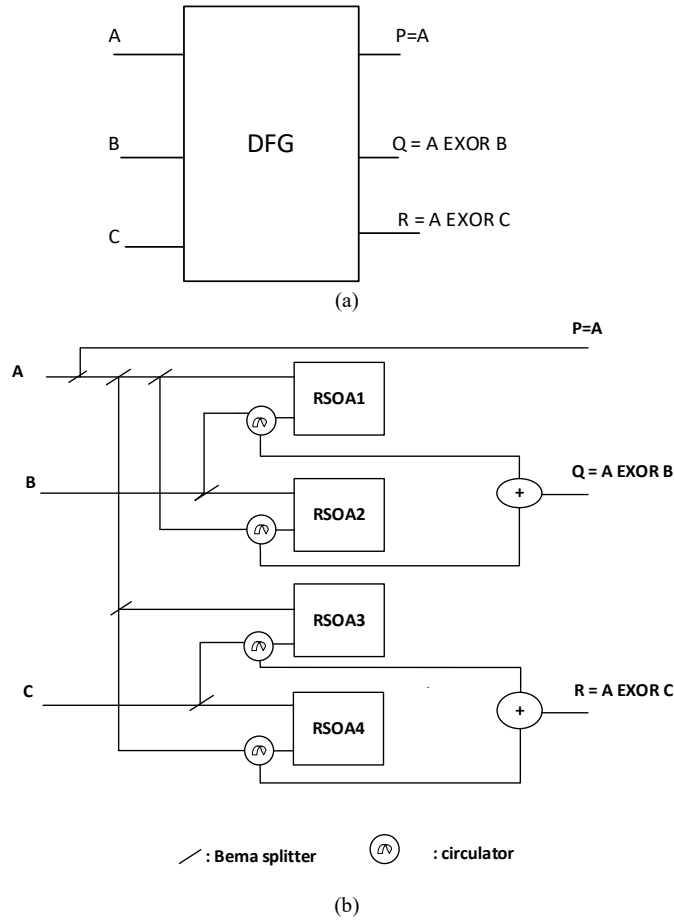


Figure 6.2: (a) Block diagram of DFG gate, (b) RSOA implementation of DFG gate [5]

Table 6.2: RSOA based Logic Operation of DFG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	'B'	'A'	' $\bar{A}B$ '
RSOA2	'A'	'B'	' $\bar{B}A$ '
RSOA3	'C'	'A'	' $\bar{A}C$ '
RSOA4	'A'	'C'	' $\bar{C}A$ '
OUTPUTS $P = A$ $Q = \text{RSOA1} + \text{RSOA2} = A \oplus B$ $R = \text{RSOA3} + \text{RSOA4} = A \oplus C$			

- **Parity-Preserving Toffoli Gate (PPTG):** The PPTG is a 4×4 gate with inputs A, B, C, D and outputs:

$$P = A, Q = B, \quad R = (A \cdot B) \oplus C, \quad S = (A \cdot B) \oplus D.$$

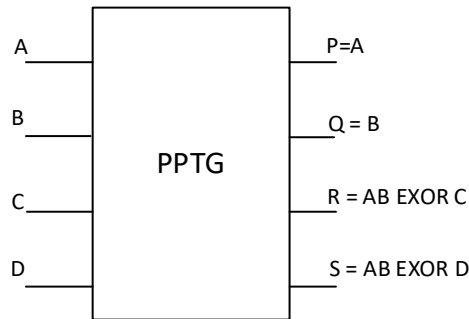
By fixing $C = 0$ and $D = 0$, the PPTG efficiently generates AND-style partial products:

$$R = A \cdot B, \quad S = A \cdot B.$$

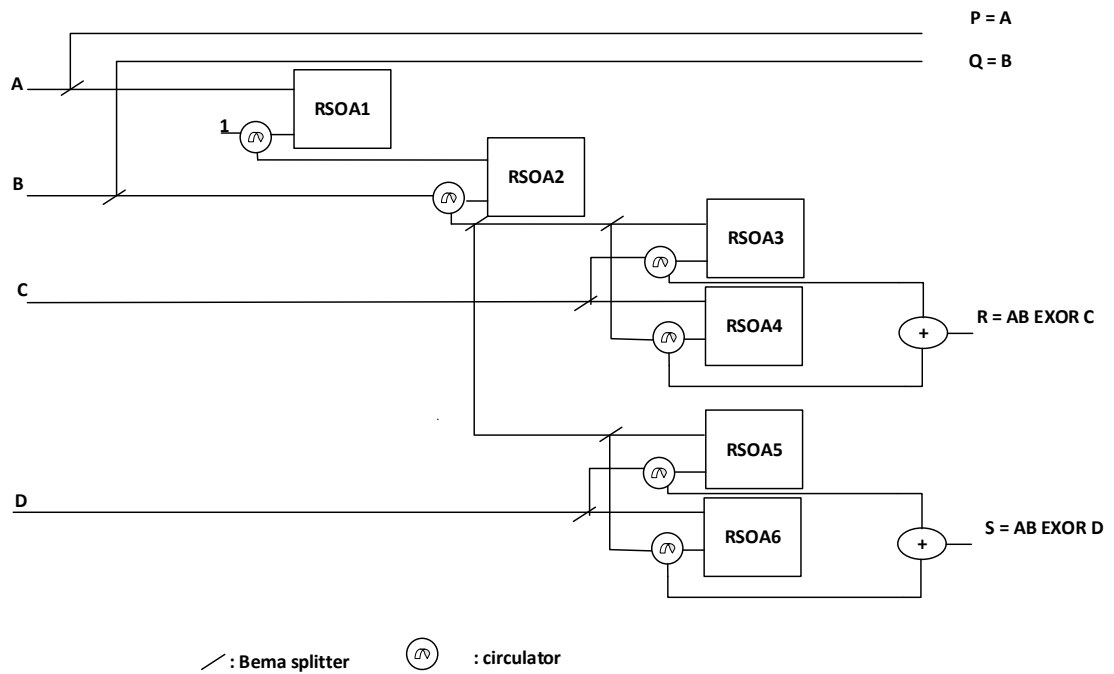
This feature is exploited to compute the four fundamental partial products of the 2×2 binary multiplication entirely in the optical domain, while still preserving parity.

Table 6.3: RSOA based Logic Operation of PPTG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	'High state'	'A'	' $\bar{A}$ '
RSOA2	'B'	' $\bar{A}$ '	'AB'
RSOA3	'C'	'AB'	' $\bar{A}BC$ '
RSOA4	'AB'	'C'	' $\bar{C}AB$ '
RSOA5	'D'	'AB'	' $\bar{A}BD$ '
RSOA6	'AB'	'D'	' $\bar{D}AB$ '
OUTPUTS $P = A$ $Q = B$ $R = \text{RSOA3} + \text{RSOA4} = AB \oplus C$ $S = \text{RSOA5} + \text{RSOA6} = AB \oplus D$			



(a)



(b)

Figure 6.3: (a) Block diagram of PPTG gate, (b) RSOA mapping of PPTG gate

- **Modified Islam Gate (MIG):** The MIG is a 4×4 parity-preserving gate defined as:

$$P = A, \quad Q = A \oplus B, \quad R = (A \cdot B) \oplus C, \quad S = (A \cdot B') \oplus D.$$

When configured with $C = 0$, the pair Q, R behaves as a reversible half-adder, generating the sum and carry of two input bits in a single gate. In the proposed multiplier, MIG gates are used to realize the addition of partial products in a compact, parity-preserving manner.

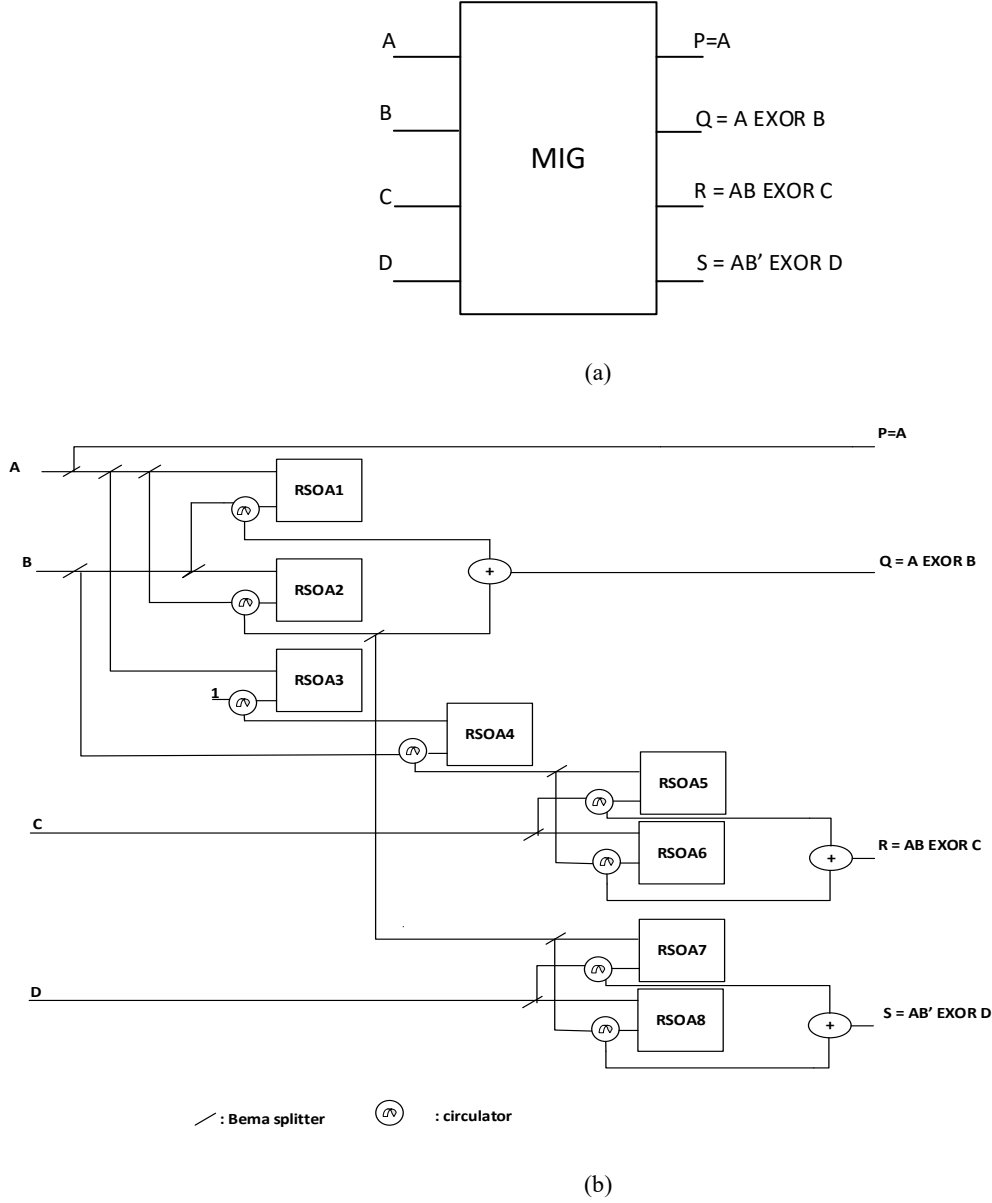


Figure 6.4: (a) Block diagram of MIG gate, (b) RSOA based implementation of MIG gate [15]

At the optical level, each gate is implemented using a specific arrangement of RSOA switches and passive elements (beam splitters and combiners). The RSOA count of each gate directly contributes to the optical cost (OC), while the number of cascaded RSOAs along the critical path defines the optical delay (OD). For the gates used here (Figure 6.2-6.4):

- DFG: OC = 4, OD = 1Δ

- PPTG: $OC = 6, OD = 3\Delta$
- MIG: $OC = 8, OD = 3\Delta$

where Δ denotes the unit delay associated with a single RSOA stage.

Table 6.4: RSOA based Logic Operation of MIG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	'B'	'A'	' $\overline{AB}$ '
RSOA2	'A'	'B'	' $\overline{BA}$ '
RSOA3	'High state'	'A'	' $\overline{A}$ '
RSOA4	'B'	' $\overline{A}$ '	'AB'
RSOA5	'C'	'AB'	' $\overline{ABC}$ '
RSOA6	'AB'	'C'	' $\overline{CAB}$ '
RSOA7	'D'	' $\overline{BA}$ '	' $\overline{BAD}$ '
RSOA8	' $\overline{BA}$ '	'D'	' $\overline{DBA}$ '
OUTPUTS $P = A$ $Q = RSOA1 + RSOA2 = A \oplus B$ $R = RSOA5 + RSOA6 = AB \oplus C$ $S = RSOA7 + RSOA8 = \overline{AB} \oplus D$			

6.4.3 2×2 Vedic Multiplier Architecture and Operation

Let the two 2-bit input operands be:

$$A = A_1A_0, B = B_1B_0,$$

and the 4-bit product be:

$$Z = Z_3Z_2Z_1Z_0.$$

Following the Urdhva–Tiryagbhyam (“vertical and crosswise”) rule, the binary multiplication is decomposed into:

- Vertical products

$$G_0 = A_0B_0, G_3 = A_1B_1$$

- Crosswise products

$$G_1 = A_0B_1, G_2 = A_1B_0$$

These terms are combined as:

$$Z_0 = G_0, Z_1 = G_1 + G_2, Z_2, Z_3 = G_3 + \text{carry from crosswise sum}.$$

The optical realization proceeds in four logical stages:

1. **Reversible fan-out using DFG gates:** Since direct copying of signals is not allowed in reversible logic, DFG gates are first used to generate the necessary copies of A_1, A_0, B_1, B_0 . By driving the auxiliary inputs of DFG with constants, we obtain multiple parity-preserving replicas of each operand bit to be routed toward partial product and adder blocks.

2. **Partial product generation using PPTG gates:** Multiple PPTG instances are then configured with $C = D = 0$ to realize:

$$G_0 = A_0B_0, G_1 = A_0B_1, G_2 = A_1B_0, G_3 = A_1B_1.$$

Because PPTG is parity-preserving and reversible, the generation of these products does not lose information or disturb the overall parity.

3. **Summation of partial products using MIG gates:** The crosswise terms G_1 and G_2 are added using MIG gates configured as half adders (with $C = 0$):

- The sum of G_1 and G_2 contributes to bit Z_1 ,
- The carry from this addition contributes to bit Z_2 along with G_3 in a subsequent MIG stage.

In this way, MIG realizes the complete “crosswise summation” required by the UT algorithm using a minimal number of parity-preserving reversible gates.

4. **Final product formation:** Collecting all contributions, the 4-bit product is formed as:

$$Z_0 = G_0, Z_1 = \text{sum}(G_1, G_2), Z_2, Z_3 = \text{carry}(G_1, G_2) \oplus G_3.$$

The complete architecture can be viewed as an all-optical, parity-preserving realization of the 2×2 -bit Vedic multiplier, with DFG acting as a copy generator, PPTG as a partial product generator, and MIG as a half-adder, exactly as illustrated in the corresponding gate-level diagrams and simulation waveforms.

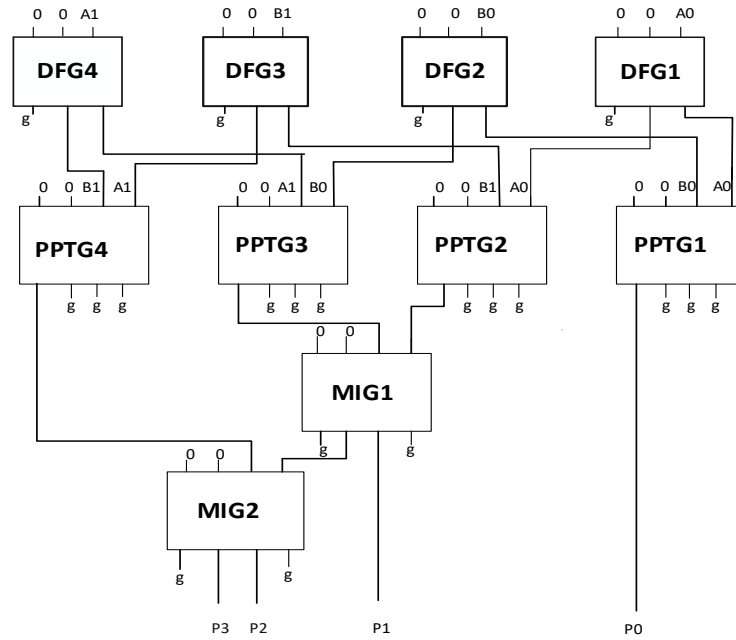


Figure 6.5: Parity preserving 2×2 -bit Vedic multiplier

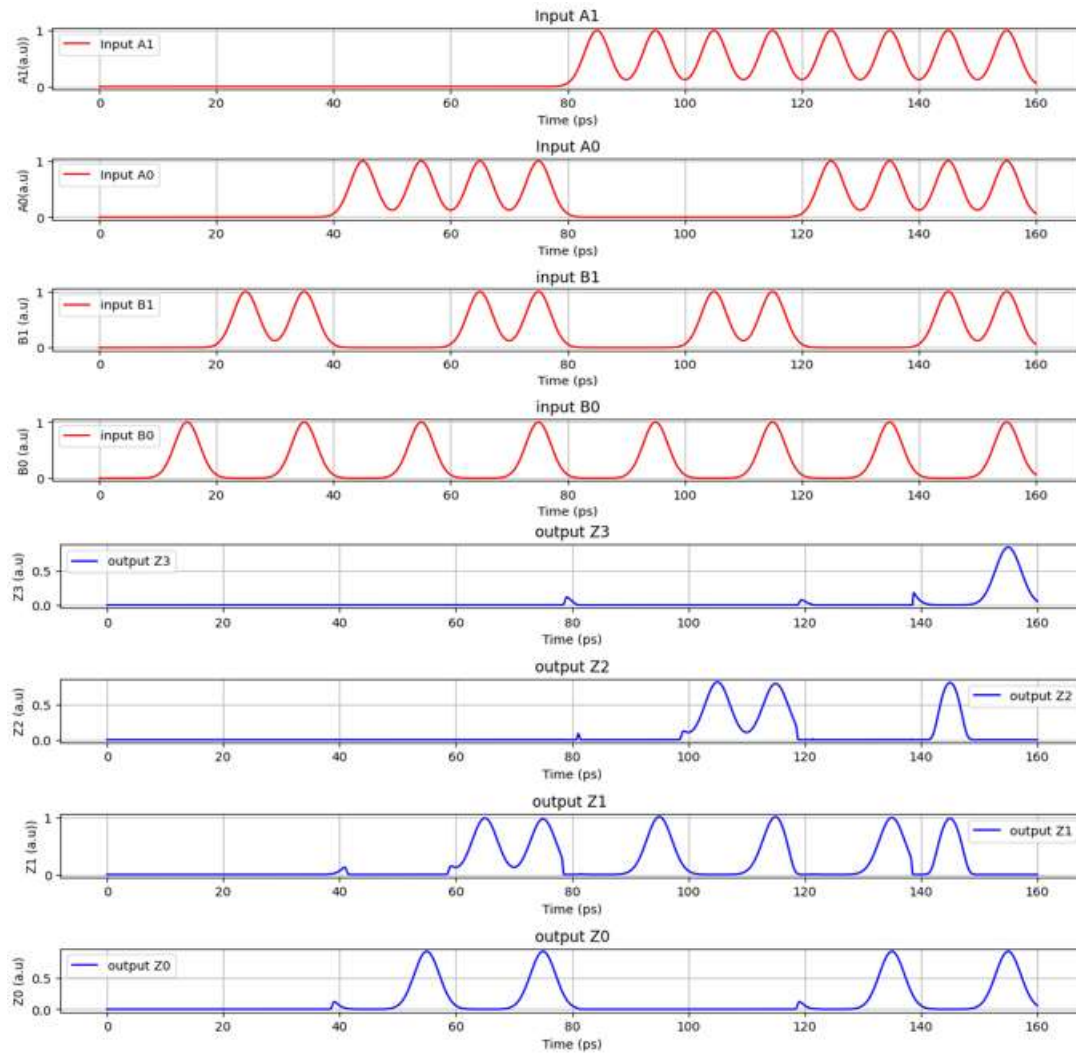


Figure 6.6: waveform of the 2x2-bit multiplier

Table 6.5: Truth Table of 2x2- Multiplier

INPUTS				OUTPUTS			
A[1]	A[0]	B[1]	B[0]	Z[3]	Z[2]	Z[1]	Z[0]
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

6.4.4 Reversibility, Parity Preservation and Resource Metrics

Because each gate in the design (DFG, PPTG, MIG) is individually reversible and parity-preserving, the overall 2×2 multiplier satisfies two key properties:

- **Reversibility:** There is a one-to-one mapping between the set of input vectors and the set of output vectors. No logical information is erased; any output pattern uniquely determines its corresponding input pattern.
- **Parity preservation:** The parity (even/odd sum of bit values) of the input set equals the parity of the output set. This allows a simple external parity checker to detect single-bit errors: any mismatch between input parity and output parity immediately flags a fault in the optical path or device behaviour.

From a resource perspective, the complete 2×2 parity-preserving multiplier exhibits:

- **Constant Inputs (CI):** 20 (Fixed ancilla lines required for configuring DFG, PPTG and MIG in specific roles.)
- **Garbage Outputs (GO):** 20 (Additional outputs necessary to maintain reversibility, not part of the functional product word.)
- **Optical Cost (OC):** 56 (Total number of RSOA switches used across all DFG, PPTG and MIG instances.)
- **Optical Delay (OD):** 10Δ (Determined by the maximum number of RSOA stages in the critical signal path.)

Although the CI and GO overhead is non-negligible at the 2-bit level, this design offers two decisive advantages for the higher-level complex multiplier:

1. It is fully reversible and parity-preserving, enabling inherent fault detection when cascaded into larger architectures; and
2. Its Vedic structure aligns naturally with the UT-based n -bit complex multiplier discussed later in this chapter, simplifying hierarchical composition with the proposed reversible UAS and other adder blocks.

Thus, the parity-preserving 2×2 -bit reversible optical Vedic multiplier presented in this section forms the core multiplication primitive used in the design and analysis of the all-optical complex multiplier developed in the subsequent sections.

6.5 Design of the All-Optical Reversible Complex Multiplier

The reversible all-optical complex multiplier proposed in this chapter is realized using RSOA-based parity-preserving logic gates and the Urdhva–Tiryagbhyam (UT) Vedic multiplication algorithm. The overall architecture extends the complex multiplier formulation introduced in

Chapter 3 (quantum domain) to the optical domain, while additionally enforcing parity preservation to enable fault detection. Unlike the quantum design of Chapter 3, which employed reversible but non-parity-preserving gates, the present optical realization strictly maintains parity at every computational stage.

The complex multiplier is constructed from the following reversible optical submodules:

- Four parity-preserving reversible Vedic multipliers (Section 6.4),
- One reversible unified adder–subtractor (UAS),
- One reversible ripple-carry adder (RCA),

all implemented using RSOA-based cross-gain modulation (XGM) switching. This modular approach ensures full reversibility, parity preservation, and interferometer-free optical operation.

Given two complex numbers,

$$X = a + jb, Y = c + jd,$$

their product is expressed as:

$$X \cdot Y = (ac - bd) + j(ad + bc).$$

The proposed architecture maps each arithmetic operation in this expression to a dedicated reversible optical subcircuit.

6.5.1 Architectural Overview

The Figure 6.7 illustrates the block-level architecture of the proposed all-optical reversible complex multiplier. The design consists of:

- Four parity-preserving reversible Vedic multipliers, generating:

$$P_1 = ac, P_2 = bd, P_3 = ad, P_4 = bc,$$

- A 2n-bit reversible unified adder–subtractor (UAS) to compute the real part:

$$Z_R = ac - bd,$$

- A 2n-bit reversible ripple-carry adder (RCA) to compute the imaginary part:

$$Z_I = ad + bc.$$

All intermediate signals propagate through reversible and parity-preserving paths, ensuring one-to-one input–output mapping and enabling inherent fault detection. Each subcircuit is implemented using MIG, PPTG, and DFG-based optical cells described previously.

6.5.2 Reversible Partial Product Generation

The complex multiplication operation decomposes naturally into four independent real-valued multiplications, each realized using a parity-preserving reversible Vedic multiplier.

In this work, the 2×2-bit parity-preserving Vedic multiplier discussed in Section 6.4 is hierarchically extended to an n-bit Vedic multiplier, following the same UT-based recursive

methodology used in Chapters 3 and 5. However, unlike Chapter 5, carry-save adders (CSAs) are not used here. Instead:

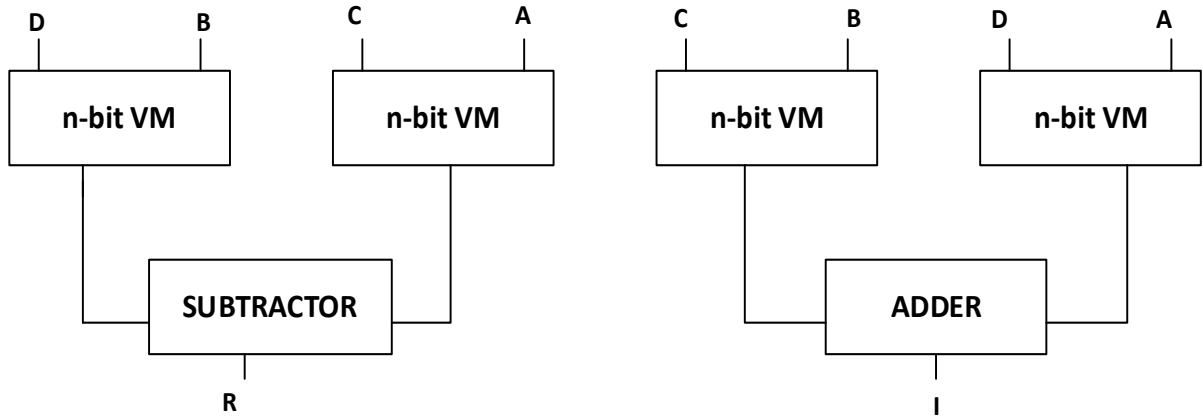


Figure 6.7: Modular designs of Complex Multiplier

- Three reversible ripple-carry adders (RCAs) are employed for summation of lower, intermediate, and higher-order partial products,
- DFG gates are explicitly used at the inputs to generate reversible fan-out, satisfying the no-fan-out constraint of reversible logic.

Thus, the n -bit Vedic multiplication is computed as:

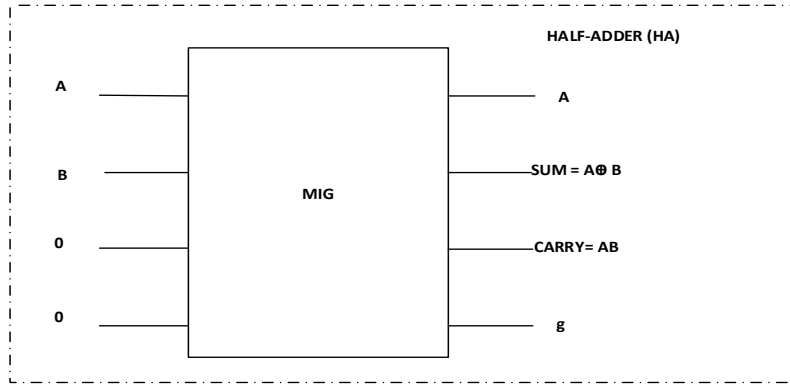
$$Z = (Z_3 \ll n) + ((Z_1 + Z_2) \ll (n/2)) + Z_0,$$

where all additions are performed using reversible RCA blocks.

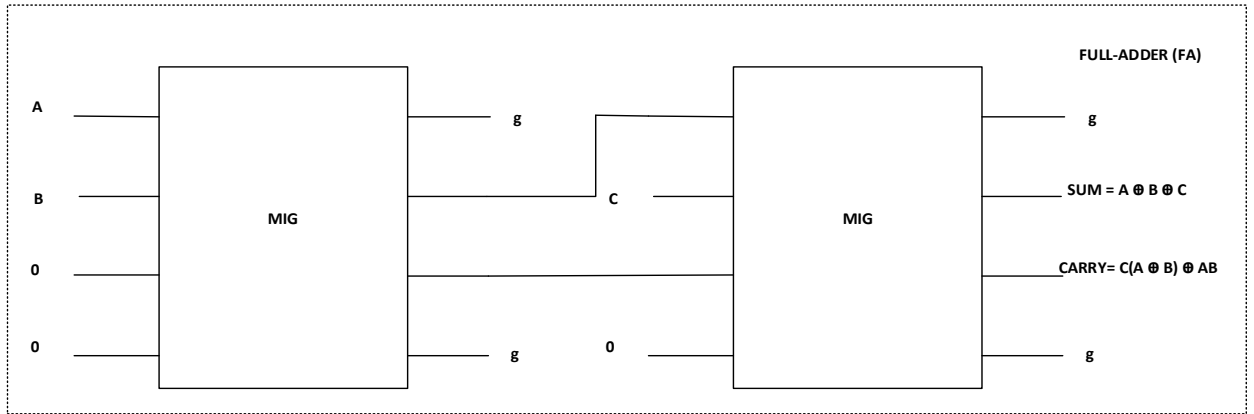
Note: The step-wise derivation of the optical cost (OC), optical delay (OD), constant inputs (CI), and garbage outputs (GO) for the n -bit reversible Vedic multiplier is not repeated here, since the analytical formulation and UT-based hierarchical expansion are identical to those presented in Chapter 5. Only the final closed-form expressions are reported.

The cumulative optical metrics for the n -bit parity-preserving Vedic multiplier are:

$$\begin{aligned} OC_{VM}(n) &= 4^{\left(\left(\log_2 \frac{n}{4}\right)+1\right)} * 56 + 8n + \sum_{i=0}^{\log_2 \frac{n}{4}} 4^i \left[48 \left(\frac{n}{2^i} \right) - 24 \right] \\ OD_{VM}(n) &= \left\{ 11 + \sum_{i=0}^{\log_2 \frac{n}{4}} \left[18 \left(\frac{n}{2^i} \right) - 9 \right] \right\} \Delta \\ CI_{VM}(n) &= 4^{\left(\left(\log_2 \frac{n}{4}\right)+1\right)} * 20 + 4n + \sum_{i=0}^{\log_2 \frac{n}{4}} 4^i \left[9 \left(\frac{n}{2^i} \right) - 3 \right] \\ GO_{VM}(n) &= 4^{\left(\left(\log_2 \frac{n}{4}\right)+1\right)} * 20 + 2n + \sum_{i=0}^{\log_2 \frac{n}{4}} 4^i \left[12 \left(\frac{n}{2^i} \right) - 6 \right] \end{aligned}$$



(a)



(b)

Figure 6.8: (a) Half-Adder (MIG gate): - OC: 8, OD:3, CI:2, GO:2; (b) Full-Adder (2 MIG gate) - OC: 16, OD:6, CI:3, GO:4

6.5.3 Reversible Real-Part Computation ($ac - bd$)

The real component of the complex product is computed using a $2n$ -bit reversible unified adder–subtractor (UAS).

- When the control signal $\text{Ctrl} = 1$, the circuit operates as a subtractor:

$$Z_R = ac - bd,$$

- When $\text{Ctrl} = 0$, the same circuit operates as an adder.

The subtraction result is generated in two's-complement form, exactly following the methodology established in Chapter 3. The UAS is realized using MIG-based reversible full adders and DFG-based controlled inversion, ensuring both reversibility and parity preservation.

The optical metrics of the $2n$ -bit UAS are:

$$\begin{aligned} \text{OC}_{\text{UAS}}(n) &= 40n, \\ \text{OD}_{\text{UAS}}(n) &= (12n + 1)\Delta, \\ \text{CI}_{\text{UAS}}(n) &= 10n, \\ \text{GO}_{\text{UAS}}(n) &= 12n. \end{aligned}$$

6.5.4 Reversible Imaginary-Part Computation ($ad + bc$)

The imaginary component is obtained using a $2n$ -bit reversible ripple-carry adder (RCA):

$$Z_I = ad + bc.$$

The RCA is constructed entirely from MIG-based reversible half- and full-adder cells, preserving parity throughout the carry-propagation process.

The optical parameters of the $2n$ -bit RCA are:

$$\begin{aligned} OC_{RCA}(n) &= 32n - 8, \\ OD_{RCA}(n) &= (12n - 3)\Delta, \\ CI_{RCA}(n) &= 6n - 1, \\ GO_{RCA}(n) &= 8n - 2. \end{aligned}$$

6.5.5 Combined Complex Multiplier Output

The final complex output is:

$$Z = (Z_R, Z_I) = (ac - bd, ad + bc).$$

By combining four n -bit Vedic multipliers, one $2n$ -bit UAS, one $2n$ -bit RCA, and DFG-based fan-out networks, the optical metrics of the n -bit complex Vedic multiplier are derived as:

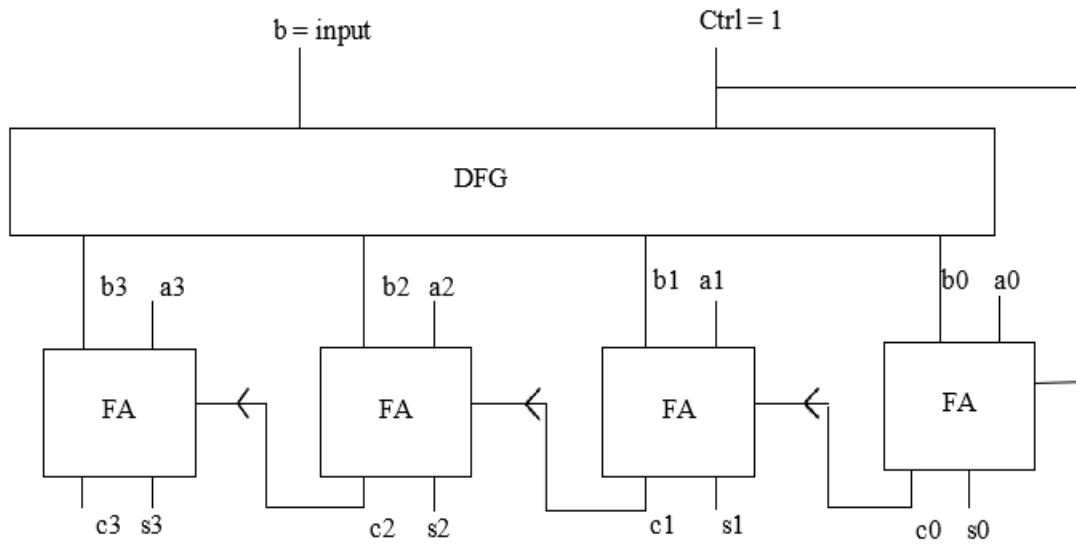


Figure 6.9: Block diagram of 4-bit UAS: OC:80, OD:25, CI:20, GO:24

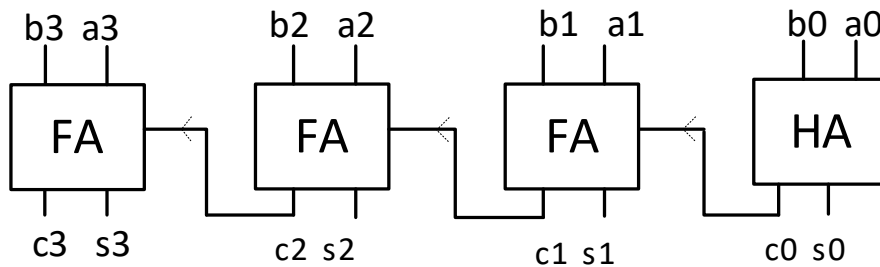


Figure 6.10: Block diagram of the 4-bit all-optical reversible ripple carry adder: OC:56, OD:21, CI:11, GO:14.

$$\begin{aligned}
OC_{CVM}(n) &= 4^{\left(\log_2\left(\frac{n}{4}\right)+1\right)} \cdot 56 + \sum_{i=0}^{\log_2\left(\frac{n}{4}\right)} 4^i \left[48 \left(\frac{n}{2^i} \right) - 24 \right] + 96n - 8, \\
OD_{CVM}(n) &= \left\{ 13 + \sum_{i=0}^{\log_2\left(\frac{n}{4}\right)} \left[18(n/2^i) - 9 \right] + 12n \right\} \Delta, \\
GO_{CVM}(n) &= 4^{\left(\log_2\left(\frac{n}{4}\right)+1\right)} \cdot 20 + \sum_{i=0}^{\log_2\left(\frac{n}{4}\right)} 4^i \left[12 \left(\frac{n}{2^i} \right) - 6 \right] + 24n - 2, \\
CI_{CVM}(n) &= 4^{\left(\log_2\left(\frac{n}{4}\right)+1\right)} \cdot 20 + \sum_{i=0}^{\log_2\left(\frac{n}{4}\right)} 4^i \left[9 \left(\frac{n}{2^i} \right) - 3 \right] + 28n - 1.
\end{aligned}$$

6.5.6 Reversibility, Parity, and Gate-Level Characteristics

The proposed all-optical complex multiplier satisfies the following properties:

- Reversibility: Every sub-module ensures bijective input–output mapping.
- Parity preservation: All gates (DFG, PPTG, MIG) preserve parity, enabling single-bit error detection.
- Scalability: UT-based hierarchy ensures logarithmic–linear growth of resources.
- Interferometer-free operation: Entirely RSOA-based, eliminating phase sensitivity.

These properties make the proposed design highly suitable for fault-tolerant photonic signal processing, optical DSP blocks, and quantum-compatible optical arithmetic units.

6.6 Performance Evaluation

This section presents the photonic performance evaluation of the proposed 2×2-bit parity-preserving reversible optical Vedic multiplier realized using RSOA-based XGM switching. Since the n-bit complex multiplier architecture in this chapter is derived analytically using hierarchical composition, time-domain optical simulations are restricted to the fundamental 2×2-bit Vedic multiplier block. The performance of this block serves as a representative indicator of the signal quality and feasibility of the larger architecture.

The evaluation focuses on key optical performance metrics—Extinction Ratio (ER), Q-factor, and Relative Eye-Opening Percentage (REOP)—which are widely accepted indicators of signal integrity in high-speed optical logic circuits.

6.6.1 Simulation Setup and Device Parameters

The proposed 2×2-bit reversible optical multiplier was simulated using Python in a Jupyter Notebook environment. The optical switching behaviour of the RSOA devices was modelled

numerically using a rate-equation-based formulation, capturing carrier density dynamics, gain saturation, and nonlinear cross-gain modulation (XGM).

The RSOA model parameters were adopted from established literature and are summarized in Table 6.6. These parameters reflect realistic device characteristics suitable for high-speed optical logic operation at 1550 nm wavelength.

Table 6.6: Parameter used in simulation

Symbol	Parameter	Value
Γ	Confinement factor	0.48
c	Velocity of light	3×10^{-8} m/s
I	Injection current	200 mA
αN	Differential gain	3.3×10^{-20} m ²
N_t	Carrier density at transparency	1024 m ⁻³
w	Width of the active region	1.5 μ m
d	Depth of the active region	250 nm
L	Active length	150 μ m
α_D	Internal loss of the waveguide	2700 m ⁻¹
λ	Wavelength of light	1550 nm
E_c	Control pulse energy	25 fJ
τ_{FWHM}	Full-width at half-maximum	5 ps
n_2	Nonlinear coefficient	2.6×10^{-20} m ² /W
D	Dispersion constant	1 ps/(nm km)
A_{eff}	Fiber effective area	5×10^{-13} m ²
E_s	Saturation energy	30 fJ
b_0	Optical bandwidth	88 GHz, .7 nm
n_{sp}	ASE factor	2
B	data rate	100 Gbps

Key simulation conditions:

- Gaussian-shaped optical pulses were generated analytically to represent data signals at 100 Gbps.
- Carrier density evolution was solved using a fourth-order Runge–Kutta (RK4) numerical integration scheme, ensuring accurate modelling of fast carrier dynamics.
- Amplified spontaneous emission (ASE) effects were incorporated into the model to reflect realistic noise behaviour.
- Simulation resolution was selected to accurately capture pulse-level dynamics and RSOA recovery effects.

This modelling framework provides a reliable balance between numerical accuracy and computational efficiency for evaluating high-speed RSOA-based optical circuits.

6.6.2 Functional Verification

The simulated input–output waveforms of the 2×2-bit multiplier confirms correct realization of the Vedic multiplication logic. The circuit produces the expected 4-bit product outputs for all possible input combinations, validating functional correctness in the optical domain.

The corresponding truth table confirms accurate mapping between binary inputs and outputs, demonstrating that the proposed architecture performs purely optical multiplication without any electrical conversion, thereby minimizing latency and energy overhead.

6.6.3 Optical Performance Metrics

In optical computing systems, signal quality is primarily assessed using the following metrics:

- **Extinction Ratio (ER):** ER quantifies the contrast between logic ‘1’ and logic ‘0’ levels and is defined as:

$$ER = 10\log_{10}\left(\frac{P_{min}}{P_{max}}\right)$$

Higher ER values indicate improved logic-level discrimination and reduced bit error probability.

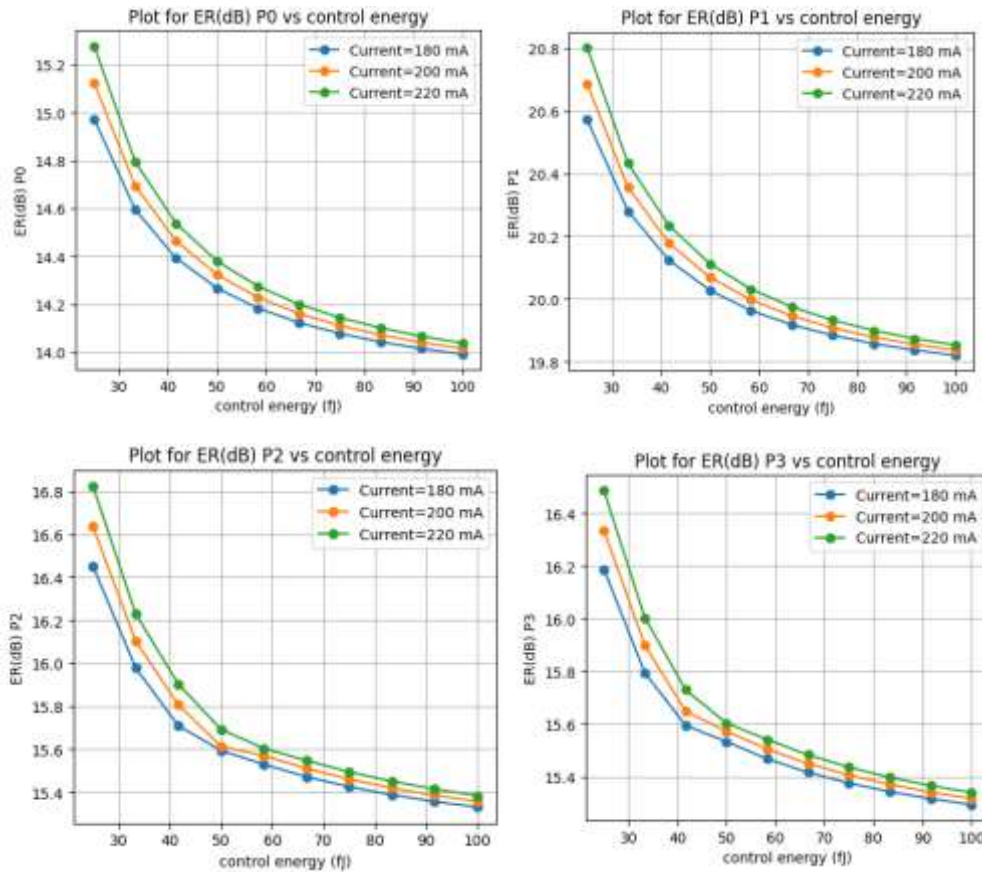


Figure 6.11: Plot of Extinction Ratio (ER) vs. Control Energy (Ec) for outputs P0, P1, P2, and P3.

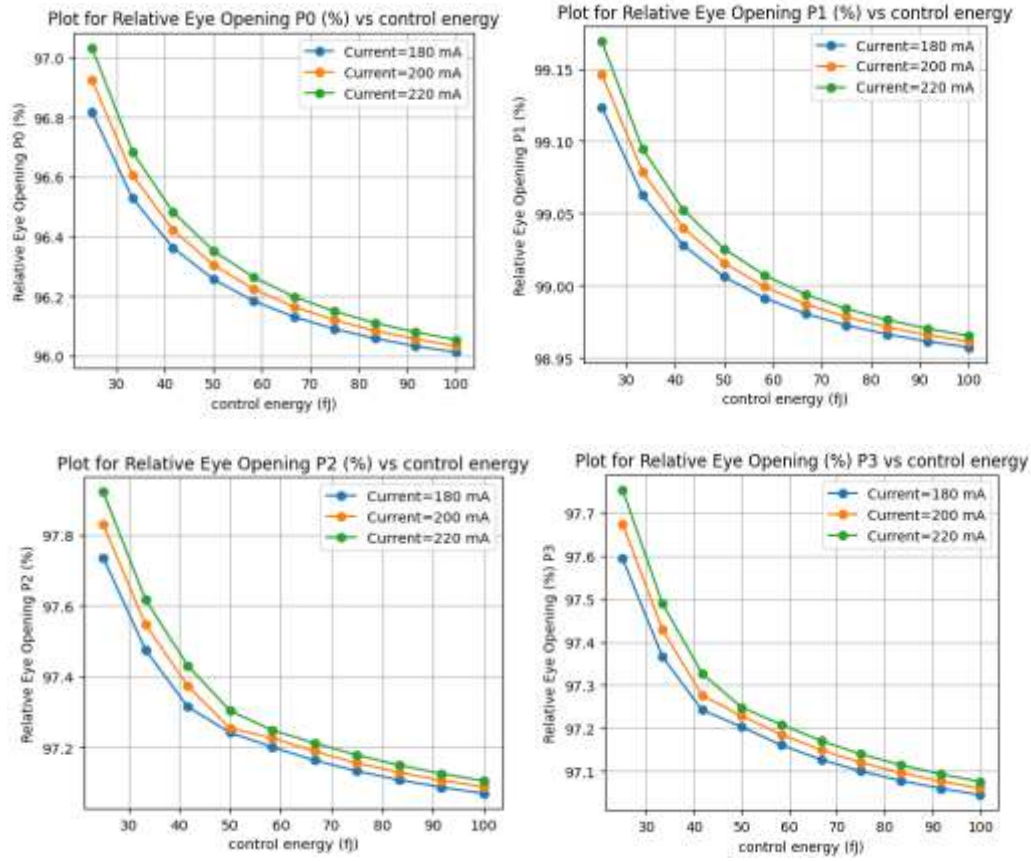


Figure 6.12: Plot of Relative Eye Opening (REOP) vs. Control Energy (E_c) for outputs P0, P1, P2, and P3.

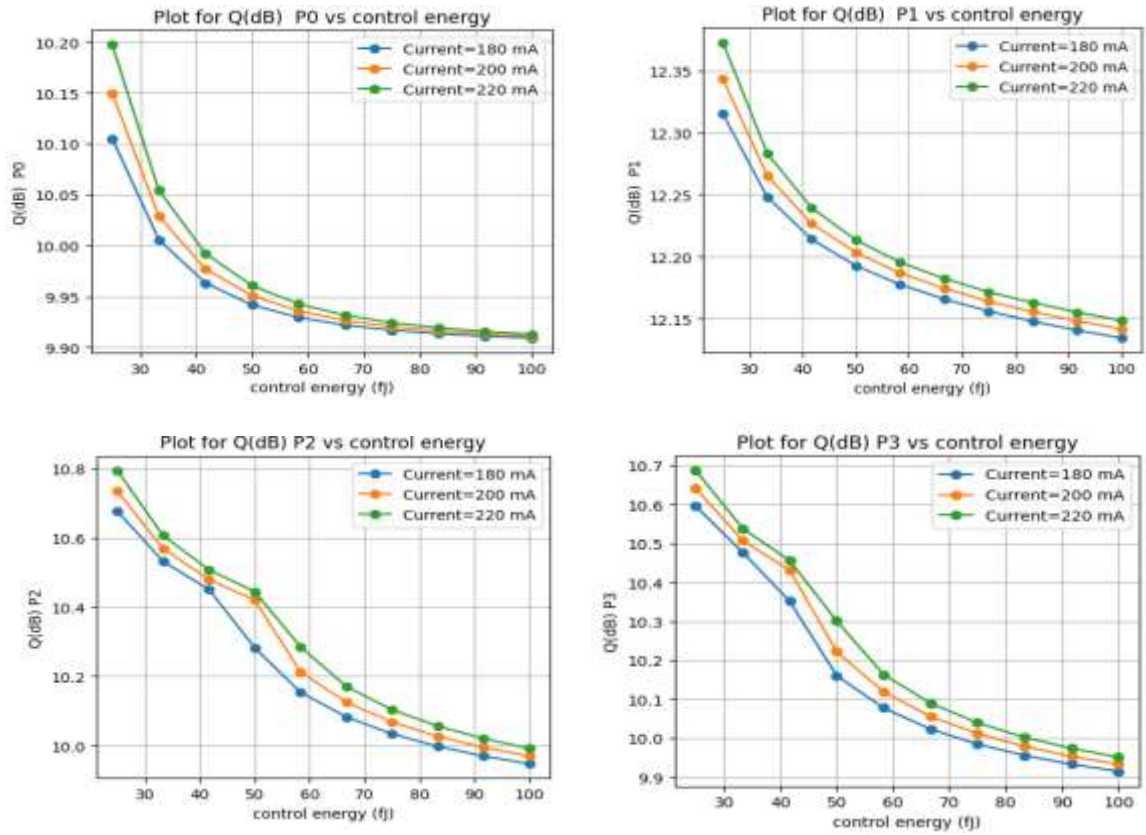


Figure 6.13: Plot of Q-factor (Q) vs. Control Energy (E_c) for outputs P0, P1, P2, and P3.

- **Q-Factor:** The Q-factor provides a statistical measure of signal integrity and noise margin:

$$Q = \frac{\mu_1 - \mu_0}{\sigma_1 + \sigma_0}$$

A higher Q-factor corresponds to lower bit error rates (BER) and better robustness against noise.

- **Relative Eye-Opening Percentage (REOP):** REOP quantifies the usable eye opening derived from eye-diagram analysis:

$$REOP(\%) = \frac{P_{min} - P_{max}}{P_{min}} \times 100$$

Larger REOP values indicate lower inter-symbol interference (ISI) and higher detection reliability.

6.6.4 Impact of Injection Current on Performance

To study the effect of operating conditions, simulations were performed for three injection current levels: 180 mA, 200 mA, and 220 mA, representing typical operating ranges for RSOA-based logic circuits.

Across all cases, increasing injection current resulted in:

- Improved ER due to enhanced gain contrast,
- Higher Q-factor indicating stronger noise immunity,
- Wider eye openings (higher REOP), reflecting reduced ISI.

These trends demonstrate that RSOA bias current provides an effective tuning knob for optimizing optical logic performance.

6.6.5 Performance at Optimal Operating Conditions

At a data rate of 100 Gbps, injection current $I = 220$ mA, and control pulse energy $E_C = 25$ fJ, the following performance metrics were achieved at the four multiplier outputs:

Output	ER (dB)	Q-Factor (dB)	REOP (%)
P₀	15.32	10.19	97.05
P₁	20.80	12.33	99.18
P₂	16.81	10.79	97.92
P₃	16.52	10.69	97.75

These results indicate:

- High extinction ratios, ensuring clear logic-level separation,
- Excellent Q-factors, corresponding to low BER operation,
- REOP values exceeding 97%, confirming robust eye openings and minimal distortion.

A slight degradation in performance is observed when control energy exceeds the optimal range, attributable to RSOA gain saturation, which is an inherent nonlinear characteristic of semiconductor optical amplifiers.

6.6.6 Comparison with Existing Optical Multipliers

Table 6.7 compares the proposed design with recent optical multipliers and basic logic blocks reported in the literature. While many prior works do not evaluate ER, Q-factor, or REOP comprehensively, the proposed multiplier demonstrates:

- Competitive or superior signal quality,
- Full reversibility, unlike most existing designs,
- Parity preservation, enabling inherent fault detection—absent in all compared works.

This combination of signal integrity, reversibility, and parity preservation distinguishes the proposed design from existing optical multipliers.

6.6.7 Discussion and Implications for n-Bit Complex Multipliers

Although detailed optical simulations are limited to the 2×2 -bit multiplier, the n-bit complex multiplier presented in Section 6.5 is constructed hierarchically using the same building blocks.

Therefore:

- The observed signal quality trends are expected to extend to larger architectures,
- Interferometer-free RSOA-based switching ensures scalability without phase sensitivity,
- Parity preservation provides a strong foundation for fault-tolerant photonic arithmetic.

6.6.8 Discussion of Results and Design Implications

The performance evaluation confirms that the proposed 2×2 -bit parity-preserving reversible optical Vedic multiplier achieves:

- High-speed operation at 100 Gbps,
- Strong signal integrity with high ER, Q-factor, and REOP,
- Stable performance across realistic RSOA operating conditions.

These results validate the feasibility of the proposed building block for integration into larger n-bit and complex optical multipliers, supporting future fault-tolerant, energy-efficient photonic computing systems.

6.7 Summary

This chapter presented the design, implementation, and performance evaluation of an all-optical reversible complex multiplier based on RSOA-driven parity-preserving logic gates. Extending the reversible arithmetic frameworks developed in earlier chapters, the work addressed complex-number computation in the optical domain, which is a fundamental requirement for photonic signal processing, communication systems, and emerging optical computing platforms.

Table 6.7: Comparison of proposed work with state-of-art

Reference	Technology used	ER (dB)	REOP (%)	Q (dB)	Reversible	Parity preserving
[67]	Polarization switch	Not Evaluated	Not Evaluated	Not Evaluated	No	No
[70]	MIM waveguides	Not Evaluated	Not Evaluated	31.31	No	No
[71]	SPP technology	Not Evaluated	Not Evaluated	Not Evaluated	No	No
[134]	Micro ring resonator (MRR)	15.9	97.4	57.6	Yes	No
[135]	Electro-optic Mach–Zehnder interferometer	26	96	Not Evaluated	No	No
[136]	Coherent perfect absorption	6.1	Not Evaluated	Not Evaluated	No	No
[137]	2D photonic crystal slab	18	Not Evaluated	Not Evaluated	No	No
Our work	Reflective semiconductor optical amplifier	16.8	97.8 (approx.)	10.46	Yes	Yes

Building on the reversible multiplier methodologies introduced in Chapter 3 (quantum domain) and Chapters 4 and 5 (real-valued optical domain), this chapter demonstrated how the same hierarchical and Vedic design philosophy can be systematically extended to complex arithmetic. Unlike the quantum-domain design, the optical architecture presented here emphasizes parity preservation in addition to reversibility, thereby enabling intrinsic fault-detection capability alongside energy-efficient computation.

A universal reversible NAND–NOR gate (NTG) was first introduced as a conceptual contribution. The NTG demonstrates the feasibility of mapping functionally complete Boolean logic into a reversible all-optical framework using a hybrid MZI–SOA and RSOA-based switching architecture. Although the NTG was not employed in the final complex multiplier design, it establishes a reusable universal primitive for future reversible optical arithmetic logic units (ALUs), control circuits, and programmable photonic logic fabrics. This part of the work, related to the NTG design and its optical realization, has been published in the IEEE 8th International Conference on Signal Processing and Communication (ICSC 2022), which is SCOPUS indexed.

The core arithmetic building block of the proposed architecture is a parity-preserving 2×2 -bit reversible optical Vedic multiplier, realized using DFG, PPTG, and MIG gates mapped onto RSOA-based cross-gain modulation (XGM) switches. This multiplier strictly maintains bijective input–output mapping and parity consistency, making it suitable for fault-aware photonic computation. Detailed gate-level realization, functional operation, and analytical

resource evaluation in terms of optical cost (OC), optical delay (OD), constant inputs (CI), and garbage outputs (GO) confirmed its suitability as a scalable primitive.

Using this 2×2-bit unit, a complete all-optical reversible complex multiplier was constructed following the classical complex multiplication expression $(a + jb)(c + jd) = (ac - bd) + j(ad + bc)$.

The architecture integrates four parity-preserving Vedic multipliers, a 2n-bit reversible unified adder–subtractor (UAS) for real-part computation, and a 2n-bit reversible ripple-carry adder (RCA) for imaginary-part computation. The design follows the same recursive and modular methodology adopted in Chapters 3 and 5, while deliberately avoiding CSA-based accumulation and instead using RCA-based summation to preserve parity and simplify analytical modelling. Closed-form expressions for OC, OD, CI, and GO were derived for the N-bit complex multiplier, demonstrating predictable and scalable growth.

Photonic performance evaluation was carried out for the 2×2-bit parity-preserving Vedic multiplier using a Python-based numerical simulation framework incorporating RSOA rate-equation modelling, ASE noise, and gain saturation effects. Signal-quality metrics such as Extinction Ratio (ER), Q-factor, and Relative Eye-Opening Percentage (REOP) were extracted at 100 Gbps operation, confirming high modulation depth, strong noise immunity, and minimal inter-symbol interference. These results validate the feasibility of the proposed design for high-speed, low-error optical computing. The remaining portions of this chapter, including the parity-preserving reversible multiplier and the complex multiplier architecture, have been communicated for journal publication.

Overall, this chapter establishes a unified methodology for designing reversible arithmetic circuits using RSOA-based optical switches, with particular emphasis on parity preservation, scalability, and signal integrity in complex-number computation. The design principles, gate-level abstractions, and analytical modelling techniques developed here form a foundational layer for future research toward all-optical arithmetic logic units (ALUs), reversible digital signal processing (DSP) blocks, photonic neuromorphic processors, and quantum-compatible reversible computing architectures.

Building upon these results, the next chapter extends the scope of reversible optical design beyond arithmetic circuits by integrating the proposed reversible gates into larger and more versatile switching structures. In particular, it focuses on the design and realization of an RSOA-based reversible universal multiplexer, which serves as a critical interconnection and control element for scalable photonic computing systems.

Chapter 7: RSOA-Based Reversible Universal Multiplexer

7.1 Introduction

With the growing demand for ultrafast, compact, and energy-efficient computing platforms, photonic logic circuits are emerging as strong candidates to complement or even replace conventional electronic logic. In particular, all-optical designs based on reversible logic are attractive because they simultaneously exploit the high-speed nature of photons and the information-preserving characteristics of reversible computation, thereby addressing both performance and energy-efficiency requirements.

Building upon the reversible arithmetic architectures developed in Chapters 4–6, this chapter presents a complete family of all-optical combinational logic blocks realized using parity-preserving reversible logic. The circuits are constructed using Reflective Semiconductor Optical Amplifier (RSOA)-based switching elements operating in the cross-gain modulation (XGM) regime, ensuring interferometer-free, stable, and scalable photonic implementation.

The central idea of this chapter is to employ the parity-preserving Fredkin Reversible Gate (FRG) as a universal optical building block. The Fredkin gate inherently satisfies the reversibility constraint and preserves input–output parity, making it particularly suitable for fault-tolerant and error-aware photonic computing systems. By realizing the FRG optically using RSOA-based XGM switching, it is configured to function as a 2×1 reversible multiplexer (MUX), which then serves as the fundamental primitive for constructing a wide range of optical logic and arithmetic circuits.

Once the parity-preserving FRG-based MUX is established, it is systematically reconfigured to implement:

- Basic logic gates: NOT, AND, OR, NAND, NOR, XOR, and XNOR
- A 4×1 reversible multiplexer
- A half-adder and a half-subtractor, all realized without violating reversibility or parity constraints

All circuits are evaluated under realistic photonic operating conditions by accounting for RSOA gain saturation, nonlinear carrier dynamics, and optical propagation effects. Key signal-integrity metrics—Extinction Ratio (ER), Contrast Ratio (CR), and Relative Eye-Opening Percentage (REOP)—are employed to quantify switching robustness, logic-level discrimination, and high-speed operational reliability.

Specifically, this chapter focuses on:

1. RSOA-based optical realization of the parity-preserving Fredkin Reversible Gate (FRG) and its configuration as a 2×1 reversible multiplexer.
2. Systematic synthesis of basic logic gates using FRG–MUX configurations guided by Binary Decision Diagram (BDD)–based logic decomposition.
3. Construction of higher-level combinational circuits, including a 4×1 MUX, half-adder, and half-subtractor, using the same parity-preserving primitive.
4. Comprehensive performance evaluation and comparison with existing all-optical logic implementations reported in the literature.

Wherever required, the underlying concepts of reversible logic and RSOA-based XGM switching are only briefly recalled, as they have been thoroughly discussed in the preceding chapters. This ensures conceptual continuity while clearly positioning the present chapter as a natural extension from reversible arithmetic units to universal optical control and switching structures.

7.2 FRG Gate and RSOA-Based 2×1 Multiplexer

7.2.1 Fredkin Reversible Gate (FRG)

The Fredkin Reversible Gate (FRG), also known as the controlled-swap gate, is a 3×3 reversible logic gate widely used in low-power and conservative logic design. Let the input vector be (A, B, C) , where A is the control input and B, C are data inputs. The output vector (P, Q, R) is defined by:

$$\begin{aligned} P &= A \\ Q &= \bar{A}B + AC \\ R &= \bar{A}C + AB \end{aligned}$$

Thus:

For $A = 0$: $Q = B, R = C$ (no swap)

For $A = 1$: $Q = C, R = B$ (swap)

The corresponding truth table is shown in Table 7.1, and the logical structure is depicted in Figure 7.1(a).

Optical implementation: The FRG is realized using five RSOA-based optical switches and six beam splitters, as shown in Figure 7.1(b). The operational mapping of probe and control signals for each RSOA is summarized in Table 7.2. The outputs are obtained as:

$$P = A, Q = \text{RSOA}_1 + \text{RSOA}_5 = \bar{A}B + AC, R = \text{RSOA}_2 + \text{RSOA}_4 = \bar{A}C + AB$$

For design comparison, the following metrics are used:

- Optical Cost (OC): number of RSOA switches = 5

- Optical Delay (OD): number of RSOAs in critical path = 2Δ

The simulated waveform in Figure 7.1(c) confirms correct reversible operation.

Table 7.1: Truth Table of FRG gate

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

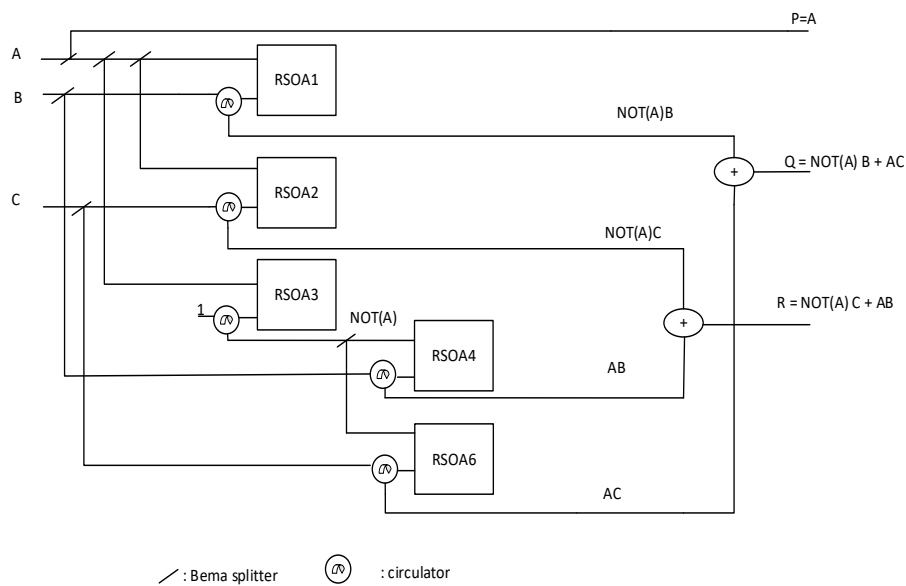
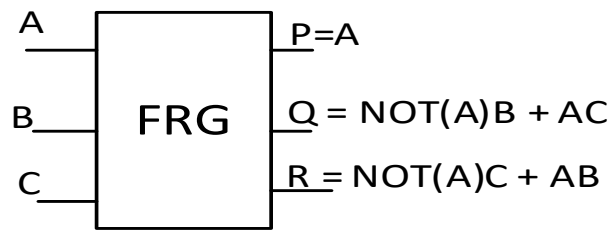
7.2.2 FRG-Based 2×1 Multiplexer Realization

The output Q of the FRG can be interpreted directly as a 2×1 MUX function:

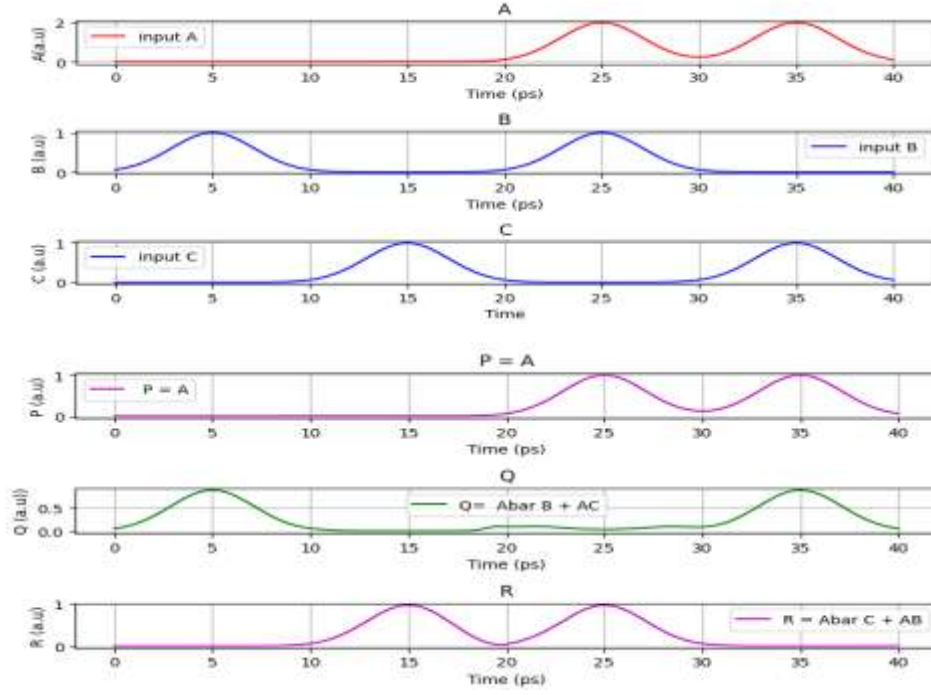
$$Q = \bar{A}B + AC$$

where:

A acts as the select line,



⧵ : Bema splitter Ⓢ : circulator



(c)

Figure 7.1: (a) Block diagram of FRG gate, (b) RSOA implementation of FRG gate, (c) Simulation waveform of FRG gate.

B and C act as data inputs I_0 and I_1 , respectively.

This is identical to the standard 2×1 MUX expression:

$$f = \bar{S}I_0 + SI_1$$

The equivalence between the FRG output and the MUX structure is illustrated in Figure 7.2, and the truth table for a 2×1 MUX is listed in Table 7.3.

A Variable Optical Attenuator (VOA) is placed at the input of the FRG–MUX to normalize input power and maintain the RSOA in an optimal gain region, ensuring clean switching behavior under XGM operation.

Table 7.2: Operational table of RSOA-Based FRG gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	B	A	$\bar{A}B$
RSOA2	C	A	$\bar{A}C$
RSOA3	‘high’	A	$\bar{A}$
RSOA4	B	$\bar{A}$	AB
RSOA5	C	$\bar{A}$	AC
$P = A$ $Q = \text{RSOA1} + \text{RSOA5} = \bar{A}B + AC$ $R = \text{RSOA2} + \text{RSOA4} = \bar{A}C + AB$			

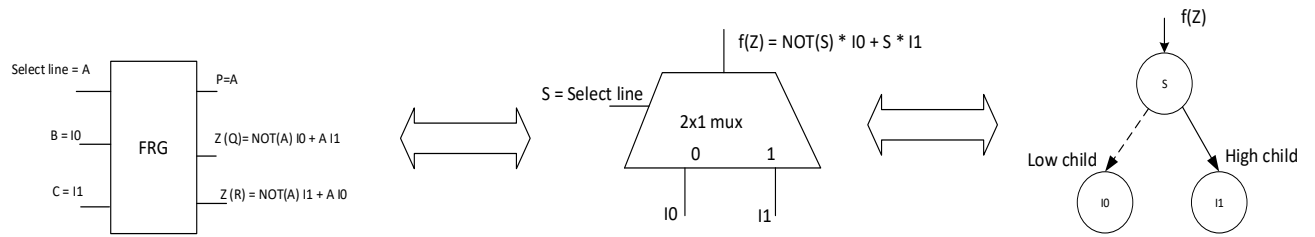


Figure 7.2: (a) Block diagram of FRG gate, (b) 2X1 MUX mapping of FRG gate, (c) BDD diagram of 2X1 MUX

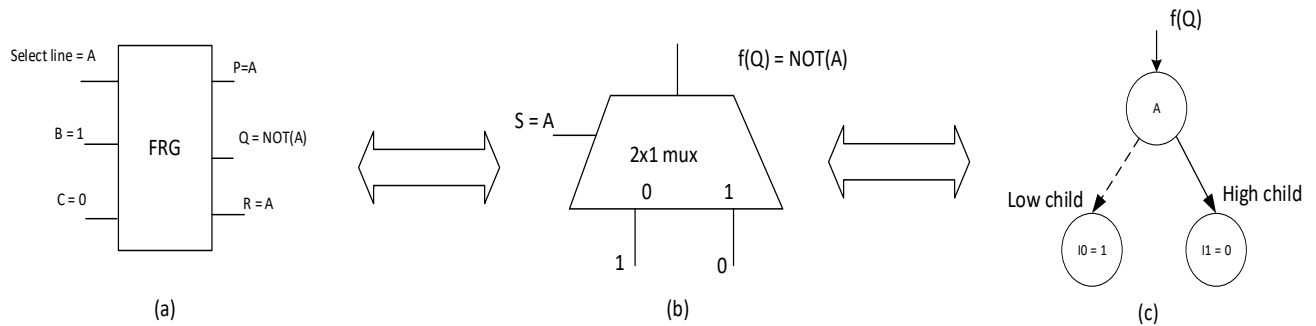


Figure 7.3: (a) FRG gate as NOT gate, (b) 2X1 MUX -NOT gate, (c) BDD diagram of NOT gate.

Table 7.3: Truth Table 2X1 MUX

SELECT LINE S	I0	I1	f(Z)
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

7.3 Logic Function Realization Using 2×1 MUX

To systematically derive logic functions from the FRG-based 2×1 MUX, two theoretical tools are employed:

1. **Shannon Decomposition Theorem (SDT):** Any Boolean function $f(A)$ can be expressed as:

$$f = \bar{A}I_0 + AI_1$$

where I_0 and I_1 are suitable subfunctions/constants. This matches exactly the functionality of a 2×1 MUX.

2. **Binary Decision Diagrams (BDDs) and Reduced BDDs (RBDDs):** These graphical representations are used to obtain compact, optimized MUX-based realizations of Boolean functions, minimizing logic redundancy and thus the number of RSOA switches.

Using these principles, the FRG-based MUX is configured to implement the standard logic gates as described below. Operational tables (RSOA mapping), BDD/RBDD diagrams, and waveforms are shown in the referenced figures and tables.

7.3.1 NOT Gate Using 2×1 MUX

A fundamental logic operation—the logical NOT—can be efficiently realized using a 2×1 multiplexer by fixing its data inputs to logical constants and configuring the select line as the variable input. Specifically, the MUX inputs are assigned as $I_0 = 1$ and $I_1 = 0$, while the select line A serves as the input variable. The resulting logic is governed by the expression:

$$\text{Output} = A' \cdot 1 + A \cdot 0 = A'$$

Thus, the output corresponds to the logical complement of the input A. The functional behavior is summarized as follows:

- When A = 0: Output = 1
- When A = 1: Output = 0

This configuration effectively inverts the input signal using the optical characteristics of the RSOA-based switch. The optical MUX circuit toggles the output based on the presence or absence of a control pulse at input A, exploiting the cross-gain modulation (XGM) property of the RSOA to modulate signal intensity in response to the control input.

Table 7.4: Operational table of RSOA-Based 2x1 MUX -NOT gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	1	A	$\bar{A}$
RSOA2	0	A	0
RSOA3	‘high’	A	$\bar{A}$
RSOA4	1	$\bar{A}$	A
RSOA5	0	$\bar{A}$	0
$P = A$ $Q = \text{RSOA1} + \text{RSOA5} = \bar{A}$ $R = \text{RSOA2} + \text{RSOA4} = A$			

Table 7.5: Truth Table NOT gate

INPUTS: A	OUTPUT: Y
0	1
1	0

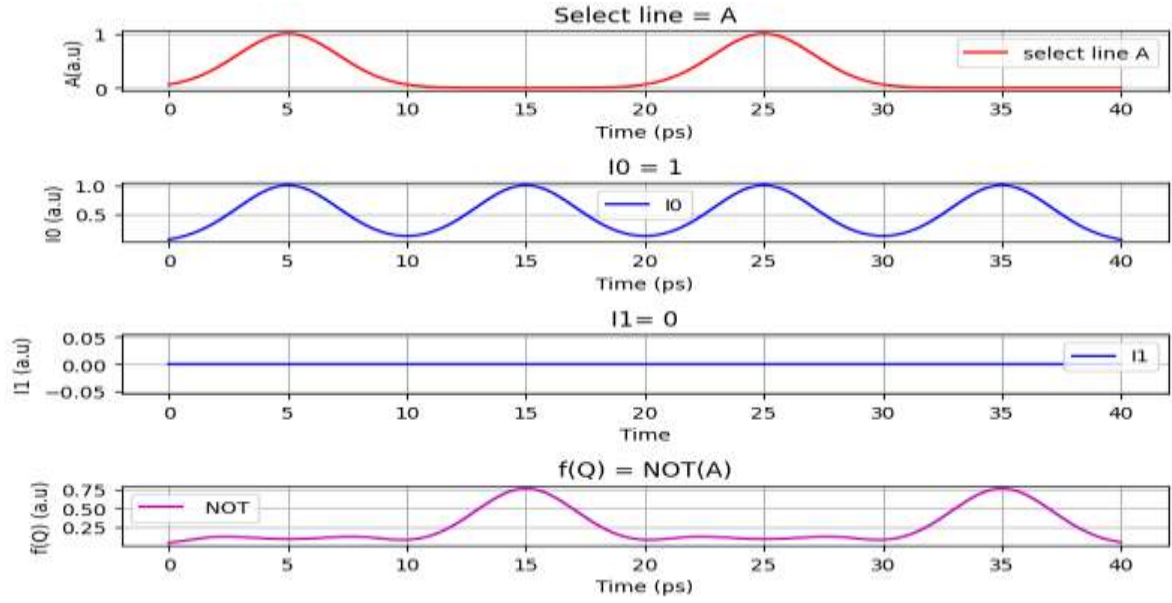


Figure 7.4: Simulation waveform of 2X1 MUX-NOT gate

The operational table of the RSOA-based NOT gate using the 2×1 MUX is provided in Table 7.4, while the simulation waveform, shown in Figure 7.4, illustrates the temporal dynamics of the gate under varying input conditions. Table 7.5 presents the conventional truth table of the NOT operation, reaffirming that the proposed design correctly replicates the logical inversion with optical signal integrity preserved.

7.3.2 AND Gate Using 2×1 MUX

The 2×1 multiplexer (MUX) can be configured to realize the logical AND function by strategically assigning one of the inputs to a constant logic value and the other to a variable signal. In this case:

- The select line is assigned to the input variable A.
- The MUX data inputs are fixed as $I_0 = 0$ and $I_1 = B$.

Under this configuration, the output behaviour follows the expression:

$$\text{Output} = A' \cdot 0 + A \cdot B = A \cdot B$$

Hence, the output corresponds precisely to the Boolean AND operation between A and B.

The operational logic is as follows:

- When $A = 0$: Output = 0
- When $A = 1$: Output = B

Table 7.6 outlines the functional mapping of the AND gate using the 2×1 MUX configuration, while Figure 7.6 presents the corresponding simulated waveforms demonstrating correct optical operation. The traditional truth table of the AND function is provided in Table 7.7,

confirming the logical integrity of the implementation. The design remains logically reversible, in line with the overarching principles of reversible computing discussed earlier.

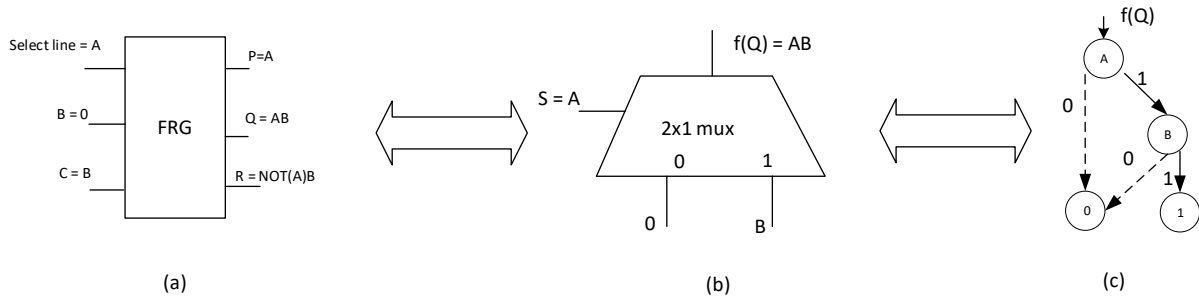


Figure 7.5: (a) FRG gate as AND gate, (b) 2X1 MUX -AND gate, (c) RBDD diagram of AND gate.

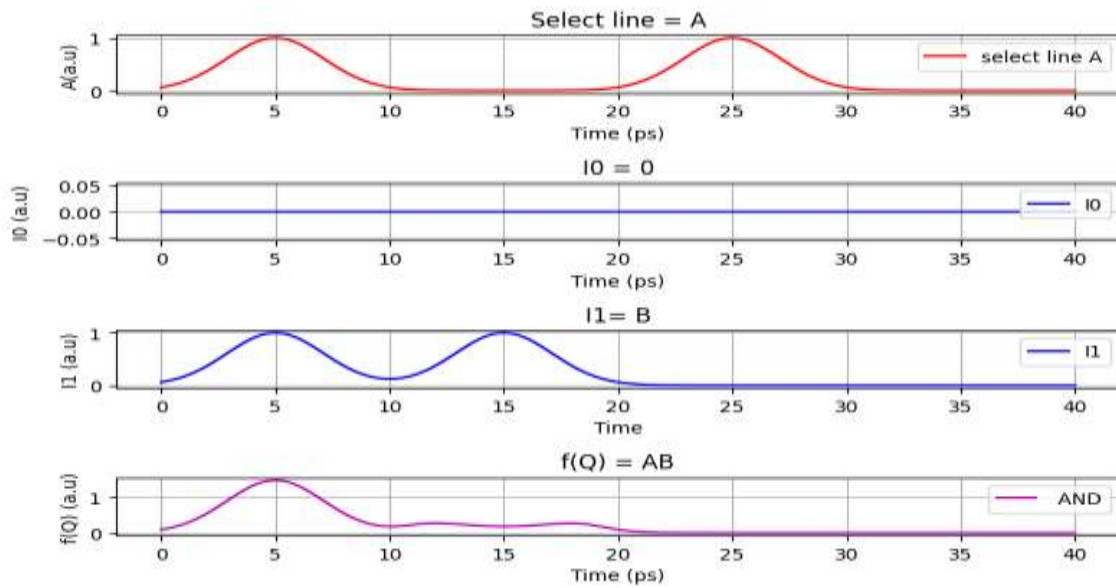


Figure 7.6: Fig. 8 Simulation waveform of 2X1 MUX-AND gate

Table 7.6: Operational table of RSOA-Based FRG 2X1- MUX AND gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	0	A	0
RSOA2	B	A	$\bar{A}B$
RSOA3	'high'	A	$\bar{A}$
RSOA4	0	$\bar{A}$	0
RSOA5	B	$\bar{A}$	AB
$P = A$ $Q = \text{RSOA1} + \text{RSOA5} = AB$ $R = \text{RSOA2} + \text{RSOA4} = \bar{A}B$			

Table 7.7: Truth Table AND gate

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	0
1	0	0
1	1	1

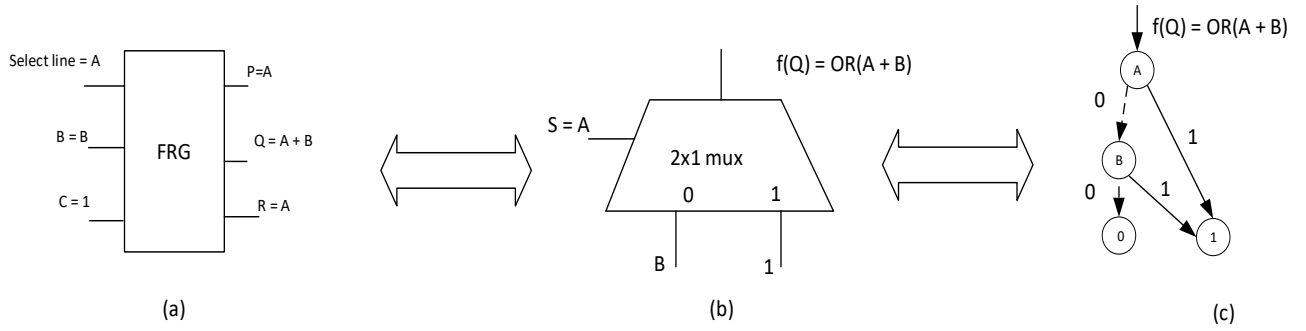


Figure 7.7: (a) FRG gate as OR gate, (b) 2X1 MUX -OR gate, (c) RBDD diagram of OR gate.

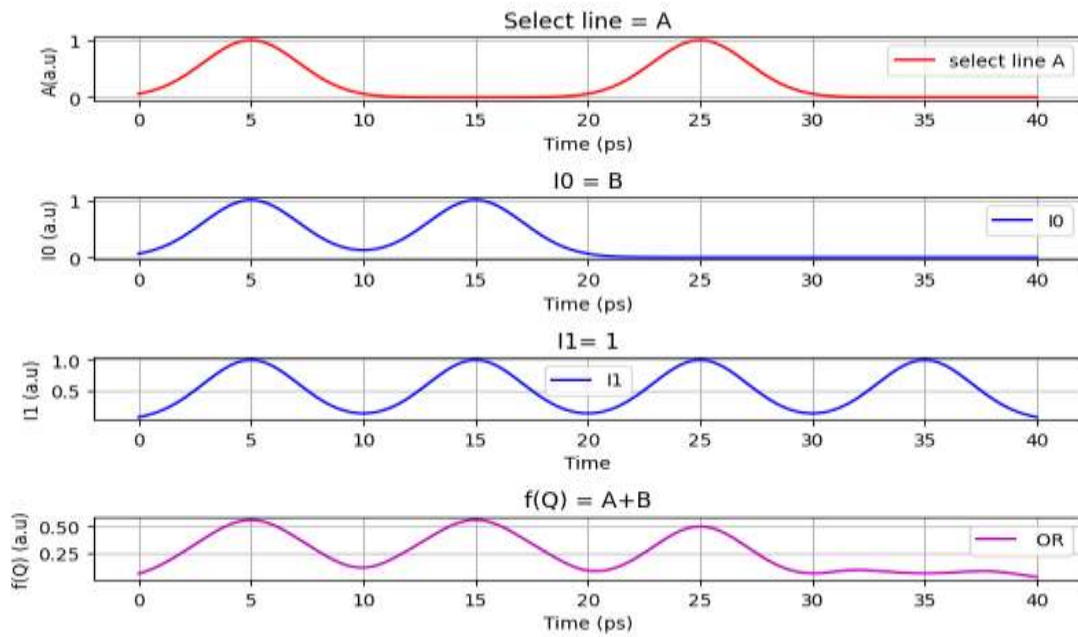


Figure 7.8: Simulation waveform of 2X1 MUX-OR gate

7.3.3 OR Gate Using 2×1 MUX

Similarly, the logical OR function can be synthesized using a 2×1 MUX by assigning the following data input configuration:

- The select line is connected to input A.
- The MUX data inputs are set as $I_0 = B$ and $I_1 = 1$.

This configuration realizes the logic:

$$\text{Output} = A' \cdot B + A \cdot 1 = A + B$$

Effectively, the output corresponds to the Boolean OR of A and B.

The operational sequence is as follows:

- When $A = 0$: Output = B
- When $A = 1$: Output = 1

In this design, the RSOA-based multiplexer performs the logical selection based on the control input A, directing either the signal B or a logical '1' to the output.

The operation behaviour of the OR gate is captured in Table 7.8, and the simulated waveform response under varying inputs is shown in Figure 7.8. The corresponding truth table for the OR logic is presented in Table 7.9, validating the functional accuracy and completeness of the implementation.

Table 7.8: Operational table of RSOA-Based FRG 2X1 MUX- OR gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	B	A	$\overline{A}B$
RSOA2	1	A	$\overline{A}$
RSOA3	'high'	A	$\overline{A}$
RSOA4	B	$\overline{A}$	AB
RSOA5	1	$\overline{A}$	A
$P = A$ $Q = \text{RSOA1} + \text{RSOA5} = \overline{A}B + A = A + B$ $R = \text{RSOA2} + \text{RSOA4} = \overline{A} + AB = \overline{A} + B$			

Table 7.9: Truth Table OR gate

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	1
1	0	1
1	1	1

7.3.4 NAND Gate Using 2×1 MUX

The implementation of a NAND logic function—one of the universal gates—can be effectively realized using a 2×1 multiplexer structure by carefully assigning its select and input lines to

Table 7.10: Operational table of RSOA-Based FRG 2X1 MUX – NAND gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	1	A	$\overline{A}$
RSOA2	$\overline{B}$	A	$\overline{A}\overline{B}$
RSOA3	'high'	A	$\overline{A}$
RSOA4	1	$\overline{A}$	A
RSOA5	$\overline{B}$	$\overline{A}$	$A\overline{B}$
$P = A$ $Q = \text{RSOA1} + \text{RSOA5} = \overline{A} + A\overline{B} = \overline{A}\overline{B}$ $R = \text{RSOA2} + \text{RSOA4} = \overline{A}\overline{B} + A = A + \overline{B}$			

emulate the desired logical behaviour. The configuration adopted for this realization is as follows:

- The select line is connected to input A.
- The multiplexer data inputs are set as $I_0 = 1$ and $I_1 = \overline{B}$.

Under this configuration, the output logic can be formally expressed as:

$$\text{Output} = A' 1 + AB' = (AB)'$$

Thus, the circuit accurately replicates the Boolean NAND function.

Table 7.11: Truth Table NAND gate

INPUT A	INPUT B	OUTPUT Y
0	0	1
0	1	1
1	0	1
1	1	0

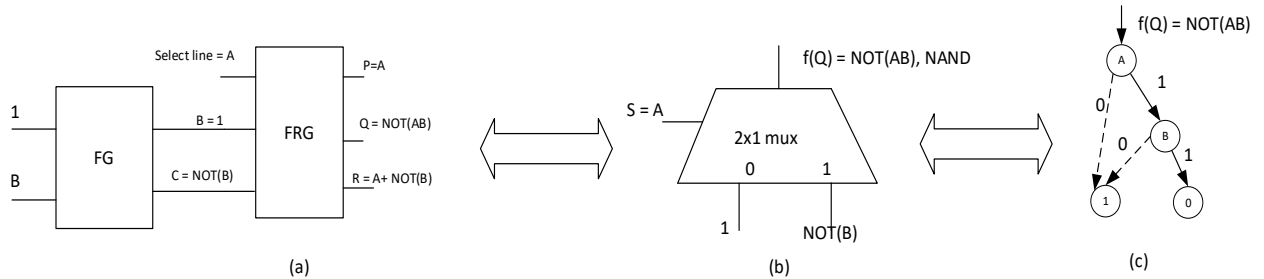


Figure 7.9: (a) FRG gate as NAND gate, (b) 2X1 Mux -NAND gate, (c) RBDD diagram of NAND gate.

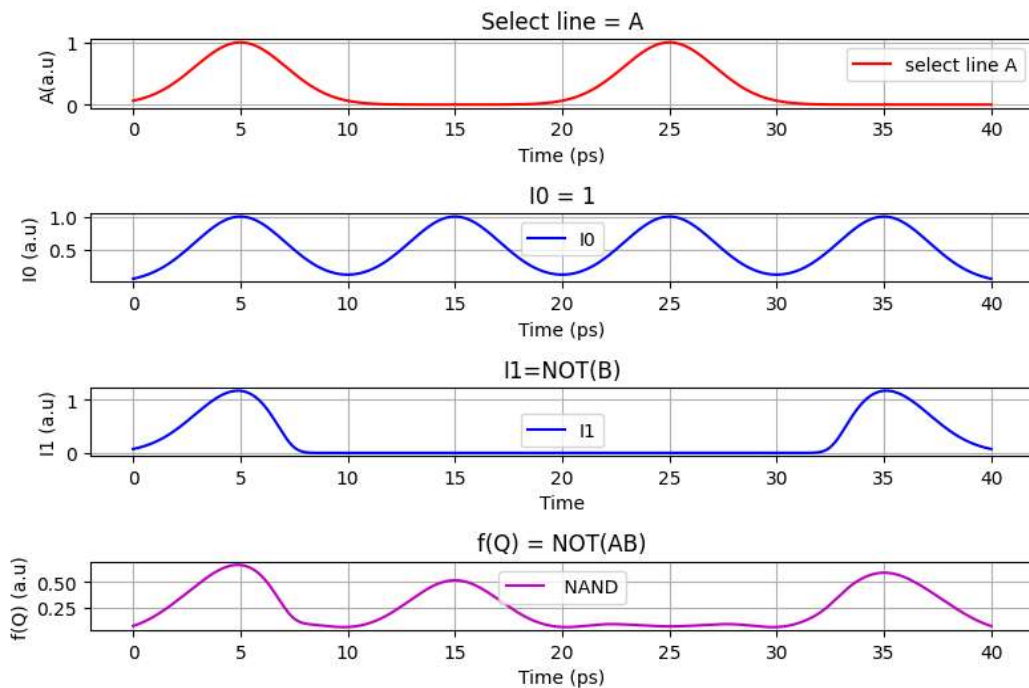


Figure 7.10: Simulation waveform of 2X1 MUX-NAND gate

The functional dynamics of the gate are summarized as:

- When $A = 0$: Output = 1
- When $A = 1$: Output = B'

To generate the complemented signal $\bar{B}$ within the all-optical reversible domain, a Feynman Gate (FG) is employed. In this auxiliary configuration, the control input A of the FG is fixed at logic '1', while B is applied to the second input. Owing to the reversible XOR operation of the

FG, the corresponding output produces the complement B' , which can then be used as a valid logical input for the subsequent multiplexer stage.

This hybrid realization leverages both parity-preserving Fredkin Reversible Gate (FRG) and FG-based reversible structures. The RSOA-based multiplexer dynamically selects between the probe inputs—logic '1' and B' —under the control of input A. As a result, the correct NAND function is realized entirely in the optical domain while strictly preserving reversibility and avoiding information loss.

The operational behaviour of this gate is summarized in Table 7.10, while the simulated optical waveforms confirming its correct functionality are shown in Figure 7.10. The corresponding logical truth table for the NAND function is provided in Table 7.11, reinforcing the accurate logical mapping of the proposed circuit.

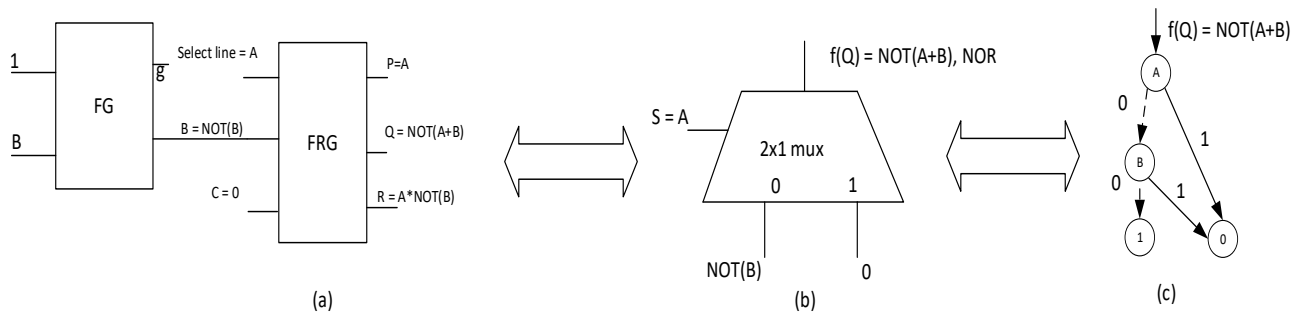


Figure 7.11: (a) FRG gate as NOR gate, (b) 2X1 MUX -NOR gate, (c) RBDD diagram of NOR gate.

7.3.5 NOR Gate Using 2×1 MUX (FRG-Based Implementation)

The logical NOR function—another universal gate—can be synthesized within a reversible optical framework using a 2×1 multiplexer by appropriately configuring the select and data input lines. The adopted configuration is as follows:

- The select line is connected to input A.
- The MUX data inputs are set as $I_0 = B'$ and $I_1 = 0$.

Under this configuration, the logical operation is governed by:

$$\text{Output} = A' B' + A 0 = (A + B)'$$

This directly corresponds to the NOR function, confirming the correctness of the optical mapping.

The functional behaviour of the gate is summarized as:

- When $A = 0$: Output = B'
- When $A = 1$: Output = 0

To generate the complemented signal B' , the design incorporates an FG (Feynman Gate), which is a 2×2 reversible logic gate. In this configuration, the control input of the FG gate is

held at logical ‘1’, and B is provided as the second input. This configuration yields the output B’, which is then used as a data input for the multiplexer.

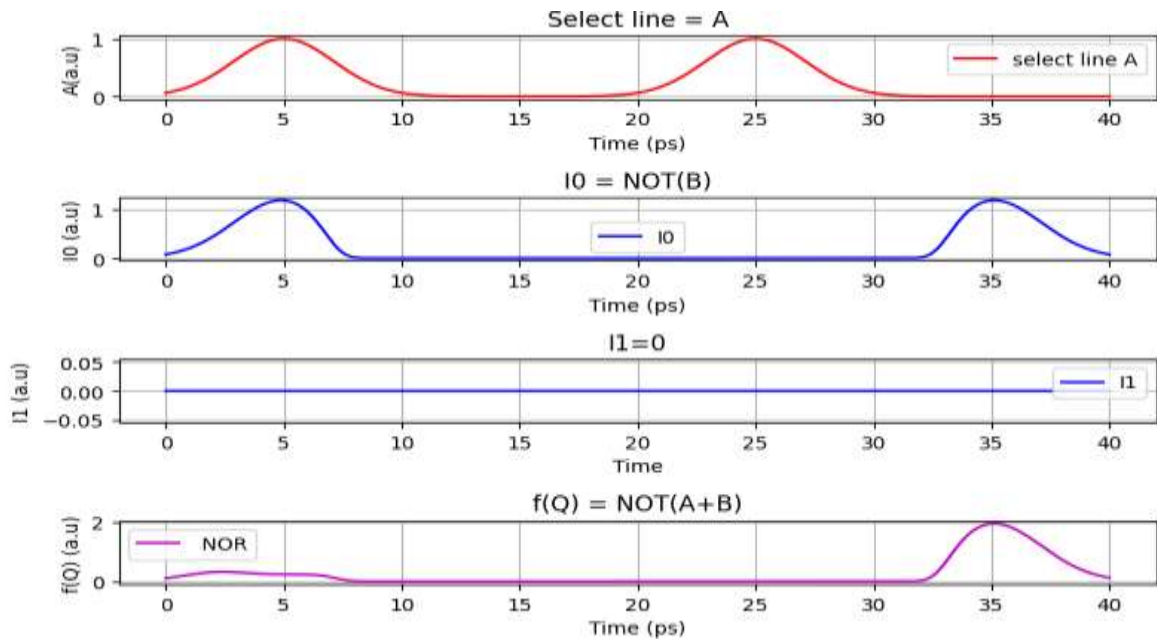


Figure 7.12: Simulation waveform of 2X1 MUX-NOR gate

Table 7.12: Operational table of RSOA-Based FRG 2X1 MUX-NOR gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	$\bar{B}$	A	$\bar{A}\bar{B}$
RSOA2	0	A	0
RSOA3	‘high’	A	$\bar{A}$
RSOA4	$\bar{B}$	$\bar{A}$	$A\bar{B}$
RSOA5	0	$\bar{A}$	0
Output $P = A$ $Q = \text{RSOA1} + \text{RSOA5} = \bar{A}\bar{B} = \overline{A + B}$ $R = \text{RSOA2} + \text{RSOA4} = \bar{A}\bar{B}$			

Table 7.13: Truth Table NOR gate

INPUT A	INPUT B	OUTPUT Y
0	0	1
0	1	0
1	0	0
1	1	0

The RSOA-based 2×1 MUX, structured using the Fredkin Reversible Gate (FRG), dynamically selects between B’ and logic ‘0’ depending on the value of the control input A.

The detailed operational behaviour is outlined in Table 7.12, while the simulated waveform confirming NOR gate operation is presented in Figure 7.12. The truth table validating the logical function is provided in Table 7.13, establishing the functional accuracy of the design in alignment with expected Boolean behaviour.

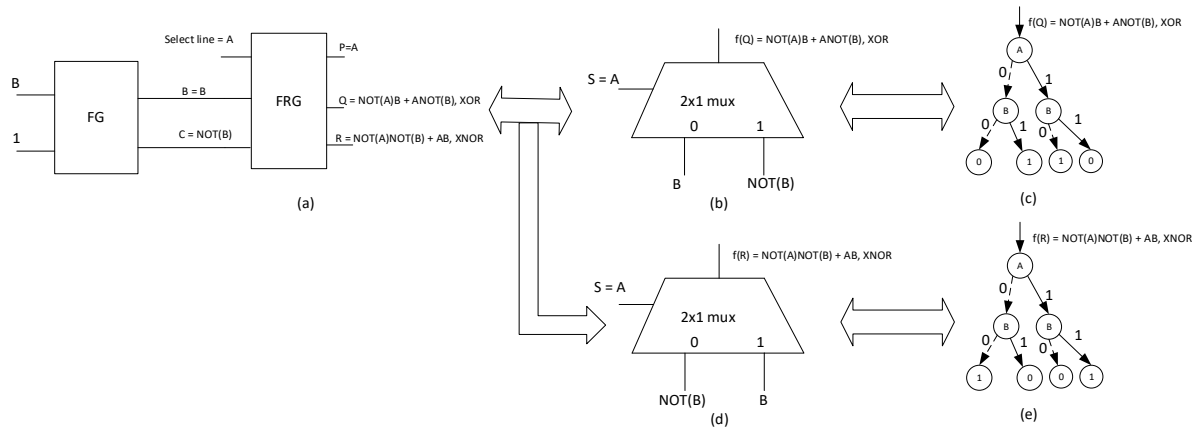
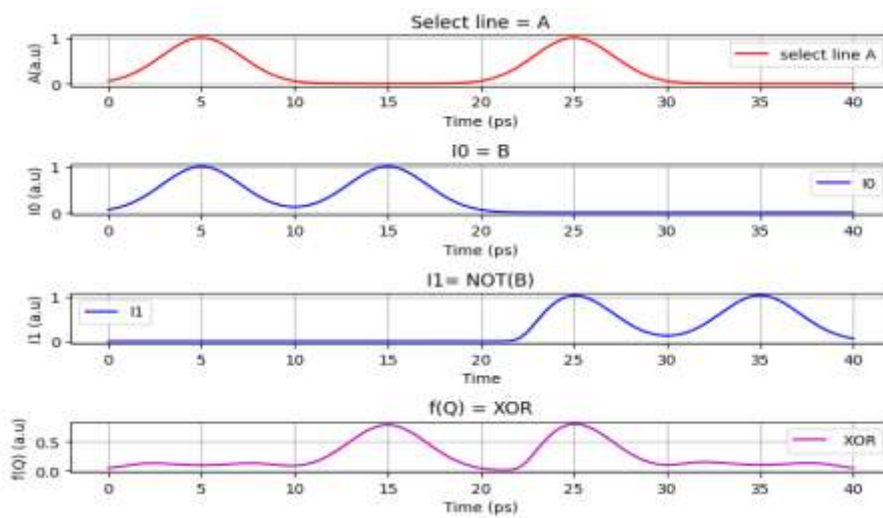
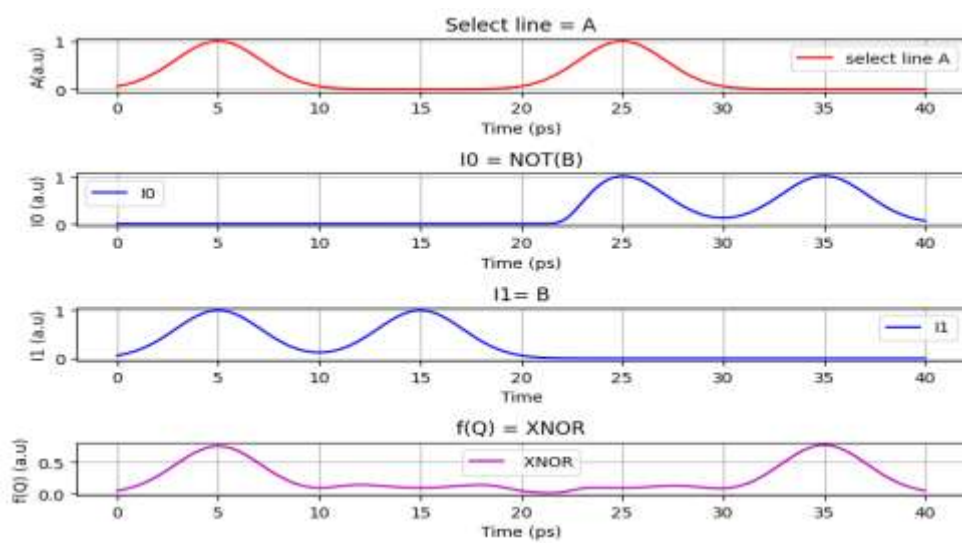


Figure 7.13: (a) FRG gate as XOR and XNOR gate, (b) 2X1 MUX -XOR gate, (c) BDD diagram of XOR gate, (d) 2X1 Mux -XNOR gate, (e) BDD diagram of XNOR gate.



(a)



(b)

Figure 7.14: Simulation waveform of (a) 2X1 MUX-XOR and (b) 2X1 MUX-XNOR gate

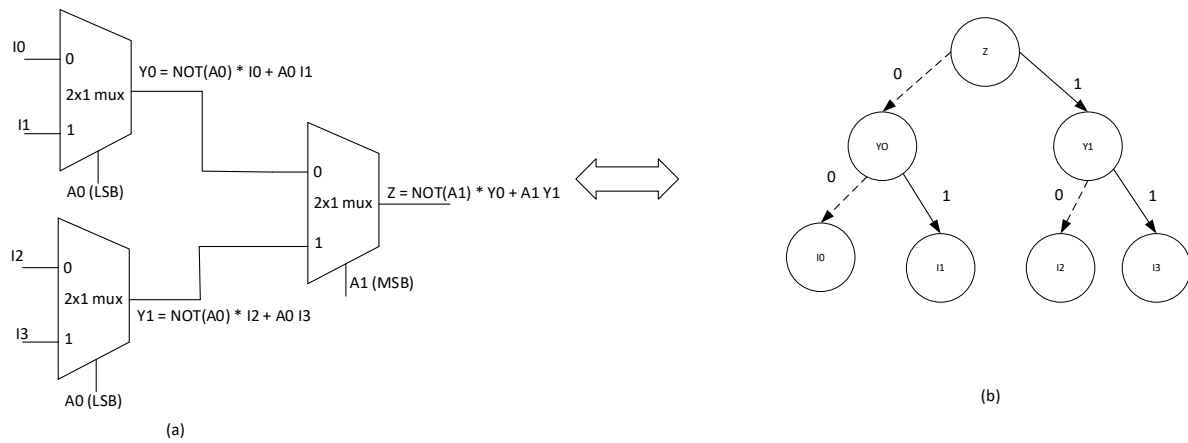


Figure 7.15: (a) 4 X 1 MUX realization using 2X1 MUX, (b) BDD diagram of 4X1 MUX.

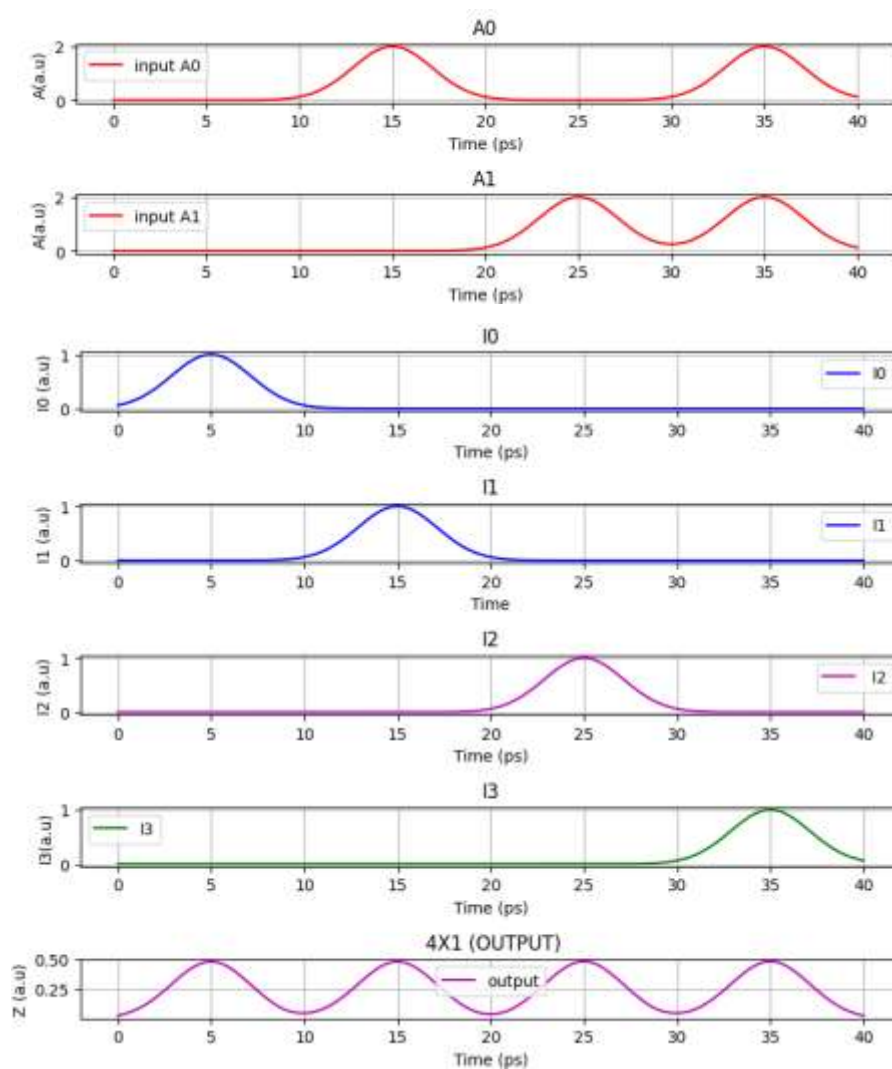


Figure 7.16: Simulation waveform of 4X1 MUX

Table 7.14: Operational table of RSOA-Based 2X1-MUX FRG- XOR/ XNOR gate

RSOA	Probe Signal Input	Control Signal Input	Output
RSOA1	B	A	$\bar{A}B$
RSOA2	$\bar{B}$	A	$A\bar{B}$
RSOA3	‘high’	A	$\bar{A}$
RSOA4	B	$\bar{A}$	AB
RSOA5	$\bar{B}$	$\bar{A}$	$A\bar{B}$
$P = A$ $Q = \text{RSOA1} + \text{RSOA5} = \bar{A}B + A\bar{B}$ $R = \text{RSOA2} + \text{RSOA4} = \bar{A}B + AB$			

Table 7.15: Truth Table XOR gate

INPUT A	INPUT B	OUTPUT Y
0	0	0
0	1	1
1	0	1
1	1	0

Table 7.16: Truth Table XNOR gate

INPUT A	INPUT B	OUTPUT Y
0	0	1
0	1	0
1	0	0
1	1	1

7.3.6 FRG-XOR and FRG-XNOR Gates Using 2×1 MUX

The Fredkin Reversible Gate (FRG) can be strategically configured to realize XOR and XNOR logic operations through the manipulation of a 2×1 multiplexer (MUX) structure, utilizing Reflective Semiconductor Optical Amplifiers (RSOAs) as switching elements. This approach preserves logical reversibility while achieving functionally complete and energy-efficient computation in the optical domain.

FRG-XOR Gate Configuration

- Select Line: A (Control Input)
- MUX Data Inputs: B and B’

The operational logic is described as:

- When A = 0: Output = B
- When A = 1: Output = B’

This configuration yields the Boolean expression:

$$Q = A \oplus B$$

Functionally, this design behaves as an exclusive-OR gate, where the RSOA-based MUX toggles between the true and complemented values of input B depending on the control signal A. The optical inversion B' is generated using a FG (Feynman Gate).

FRG-XNOR Gate Configuration

- Select Line: A (Control Input)
- MUX Data Inputs: B' and B

The output behaviour follows:

- When A = 0: Output = B'
- When A = 1: Output = B

This yields the Boolean expression:

$$Q = A \odot B$$

This setup realizes the exclusive-NOR (XNOR) operation, preserving the reversible characteristics of the FRG-based structure. Again, the FG gate is utilized to generate B', ensuring that the inputs to the MUX remain optically driven and reversible.

The operational mappings of both gates are summarized in Table 7.14, with the truth tables provided in Tables 7.15 and 7.16, respectively. The simulated optical waveforms confirming correct logical operation and all-optical signal modulation are depicted in Figure 7.14. These implementations highlight the feasibility of compact, reversible logic designs for high-speed optical computing using MUX-based architectures.

7.3.7 4×1 Multiplexer (MUX) Using Three 2×1 MUXes

A 4×1 multiplexer (MUX) is a fundamental building block in optical logic systems, capable of routing one of four input signals to a single output based on two binary select lines. This functionality can be efficiently realized through the hierarchical composition of three 2×1 MUXes, leveraging modular design principles and scalable architecture.

Design Configuration:

Let the four data inputs be: I_0, I_1, I_2, I_3

Let the select lines be:

A0 (LSB), A1 (MSB)

The cascade structure is as follows:

- MUX1: Select line = A₀, inputs = I_0 and I_1 → Output = Y_0
- MUX2: Select line = A₀, inputs = I_2 and I_3 → Output = Y_1
- MUX3: Select line = A₁, inputs = Y_0 and Y_1 → Output = Z (Final Output)

Functional Behaviour:

- If $A_1A_0 = 00 \rightarrow \text{Output } Z = I_0$
- If $A_1A_0 = 01 \rightarrow \text{Output } Z = I_1$
- If $A_1A_0 = 10 \rightarrow \text{Output } Z = I_2$
- If $A_1A_0 = 11 \rightarrow \text{Output } Z = I_3$

The block diagram is shown in Figure 7.15, and the truth table in Table 7.17. Since each 2×1 MUX is FRG-based and reversible, the composite 4×1 MUX also preserves reversibility.

Table 7.17: Truth Table 4X1 MUX

SELECT LINE A1	SELECT LINE A0	OUTPUT Z
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

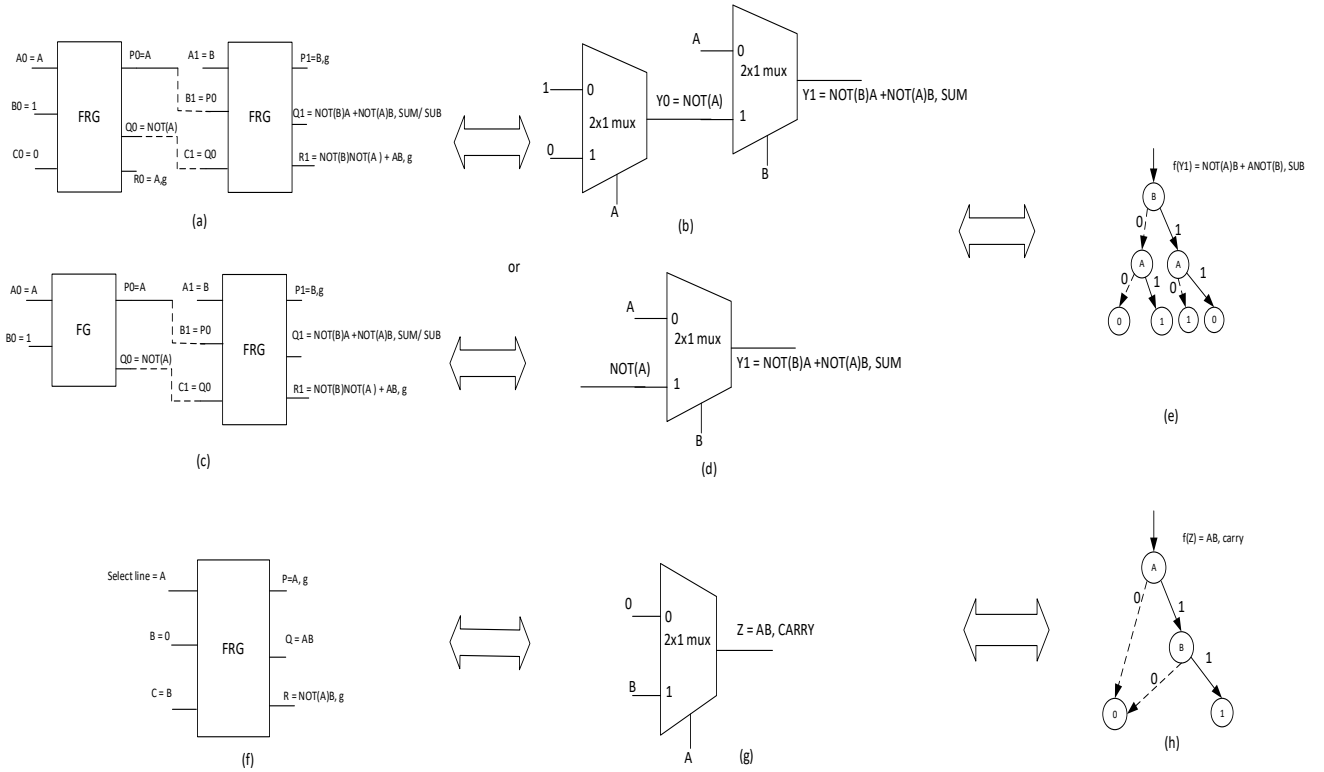


Figure 7.17: (a) FRG-XOR (SUM) gate, (b) 2X1-MUX-XOR (SUM) gate, (c) BDD diagram of XOR(SUM), (d) FG-FRG-XOR (SUM) gate, (e) 2X1 MUX XOR (SUM) gate, (f) FRG-AND (CARRY) gate, (g) 2X1-MUX AND (CARRY) gate, (h) BDD diagram of AND (CARRY).

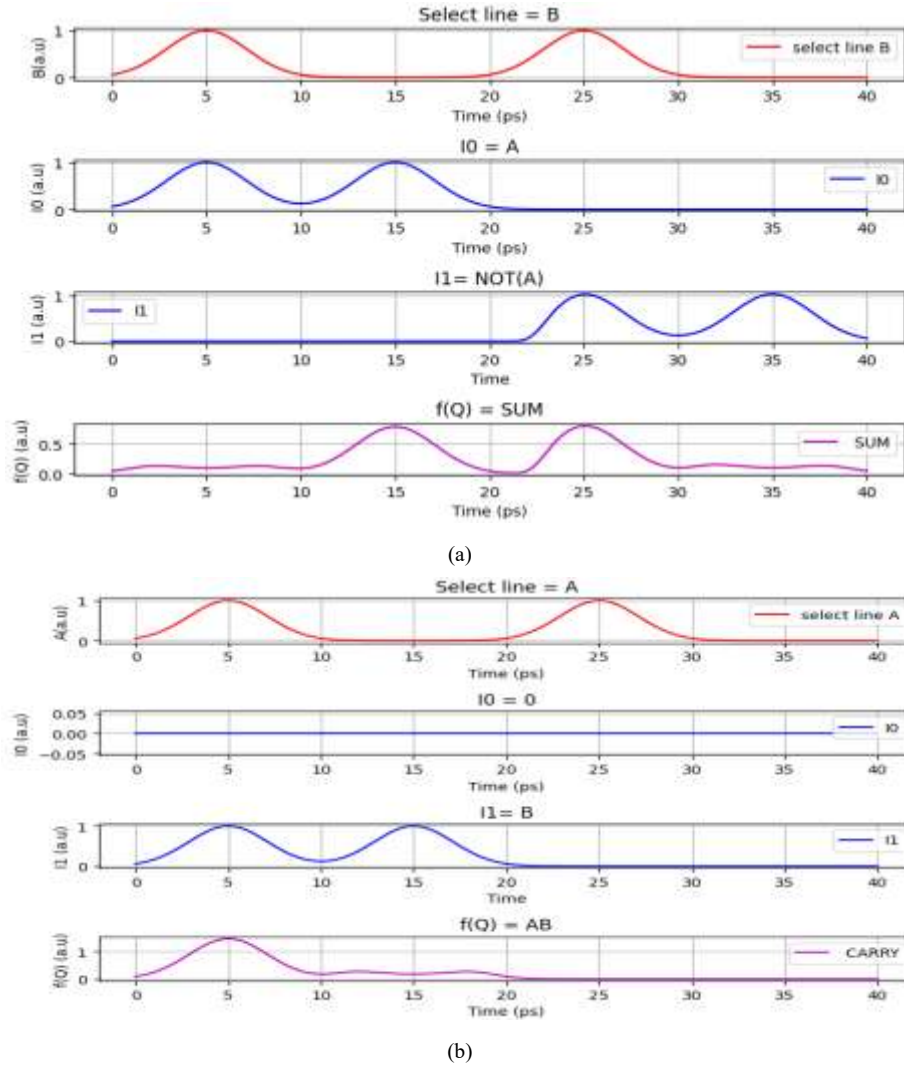


Figure 7.18: Simulation waveform of 2X1 MUX-half adder: (a) SUM, (b) CARRY

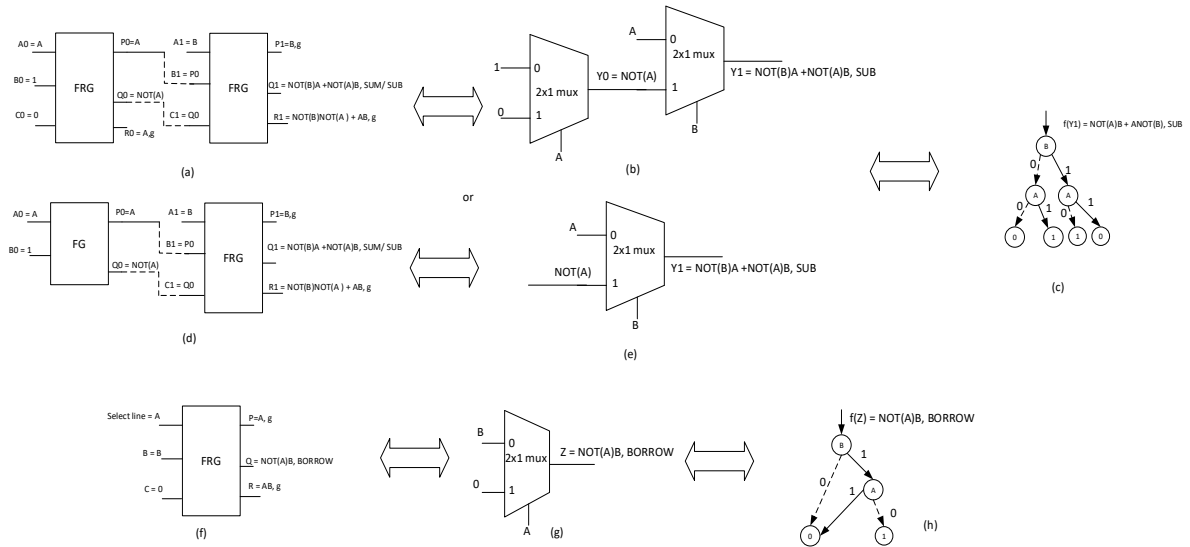
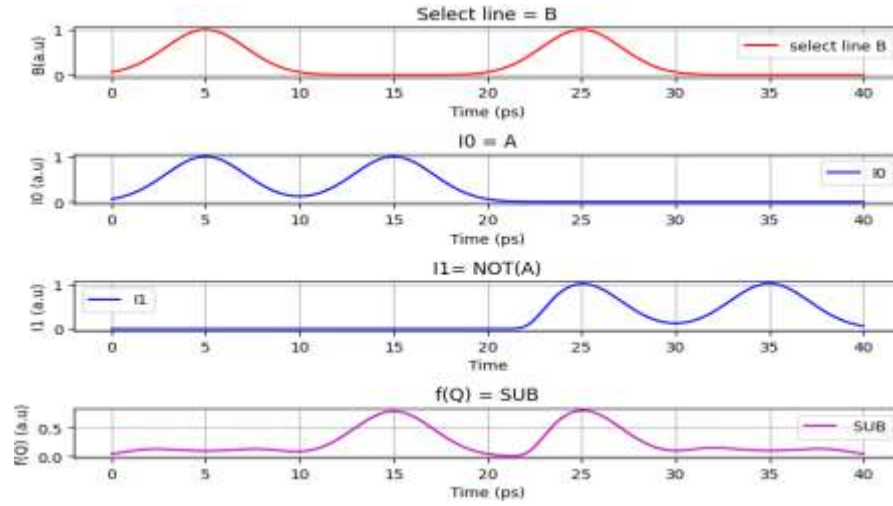
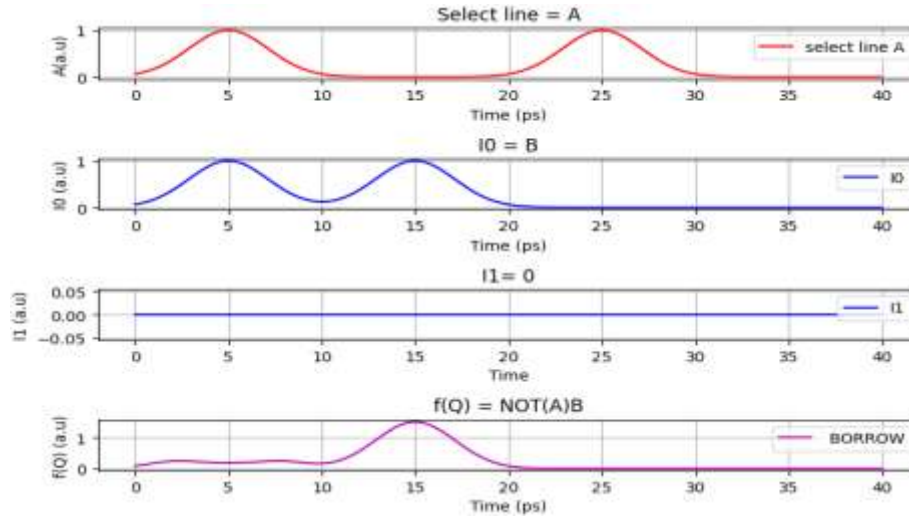


Figure 7.19: (a) FRG –XOR (SUB) gate, (b) 2X1- MUX-XOR (SUB) gate, (c) BDD diagram of XOR(SUB), (d) FG-FRG-XOR (SUB) gate, (e) 2X1 MUX XOR (SUB) gate, (f) FRG-AND (BORROW) gate, (g) 2X1-MUX AND (BORROW) gate, (h) RBDD diagram of AND (BORROW).



(a)



(b)

Figure 7.20: Simulation waveform of 2X1 MUX-half subtractor: (a) SUB, (b) BORROW

7.3.8 2×1 Multiplexer as a Half Adder

A 2×1 multiplexer (MUX) can be strategically configured to realize the functionality of a half adder, which computes the sum ($A \oplus B$) and carry ($A \cdot B$) outputs for a pair of binary inputs A and B. This implementation leverages the modular and reversible nature of MUX-based logic using Reflective Semiconductor Optical Amplifiers (RSOAs), facilitating an all-optical, low-complexity arithmetic circuit suitable for ultrafast photonic computing systems.

Sum Generation ($A \oplus B$):

The sum output of a half adder corresponds to the exclusive-OR operation between inputs A and B, i.e., $SUM = A \oplus B$. This operation is implemented using a single 2×1 MUX configured as follows:

- Select Line: B

- MUX Inputs: $I_0=A$, $I_1=A'$

The functional behaviour is defined by:

- When $B = 0$: Output = A
- When $B = 1$: Output = A'

This configuration realizes the XOR function $A \oplus B$, with the input complement A' generated using a Feynman (FG) gate or a secondary MUX, depending on the design constraints. Two equivalent circuit arrangements for obtaining A' are shown in Figure 7.17, offering flexibility in optical hardware synthesis.

Carry Generation ($A \cdot B$)

The carry output of the half adder corresponds to the logical AND of inputs A and B , i.e., $CARRY=A \cdot B$. This is realized using a second 2×1 MUX configured as:

- Select Line: A
- MUX Inputs: $I_0=0$, $I_1= B$

This yields:

- When $A = 0$: Output = 0
- When $A = 1$: Output = B

$$\text{Output}=A \cdot B$$

The use of RSOA-based MUXes in both sum and carry circuits ensures dynamic gain-controlled switching and low optical delay, preserving the reversibility and energy efficiency of the circuit.

Table 7.18: Truth Table HALF-ADDER

INPUT A	INPUT B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Design Summary:

By cascading these two MUX-based subsystems, the complete half adder is constructed entirely in the optical domain, eliminating the need for intermediate electrical conversion or external logic stages.

The logical operation of the half adder is detailed in Table 7.18, while the corresponding simulated waveforms validating the functionality are depicted in Figure 7.18. These results confirm the accurate all-optical realization of the half adder using FRG-based 2×1 MUX configurations, reinforcing the viability of RSOA-enabled multiplexers in constructing fundamental arithmetic units for next-generation optical processors.

7.3.9 2×1 Multiplexer as a Half Subtractor

The 2×1 multiplexer (MUX) can be effectively adapted to implement a 1-bit half subtractor, which computes both the difference (SUB) and borrow for two binary inputs, A and B, using an all-optical configuration based on Reflective Semiconductor Optical Amplifier (RSOA)-based switching. The compact and modular nature of the MUX-based design makes it highly suitable for high-speed, energy-efficient arithmetic operations within integrated photonic circuits.

Difference Generation ($A \oplus B$):

The difference output of a half subtractor is defined by the XOR of inputs A and B:

$$\text{DIFF} = A \oplus B$$

This operation is realized using a single 2×1 MUX, configured as follows:

- Select Line: B
- MUX Inputs: $I_0=A$, $I_1=A'$

The operational logic is:

- If B = 0: Output = A
- If B = 1: Output = A'

This configuration mirrors the XOR implementation used in the half adder. The complementary signal A' is generated via a Feynman Gate (FG) or using an auxiliary MUX-based inverter circuit, as illustrated in Figure 7.19. Either realization method can be employed depending on architectural constraints or optimization goals such as footprint or power consumption.

Borrow Generation ($A' \cdot B$):

The borrow output is defined by the logical expression:

$$\text{Borrow} = A' \cdot B$$

This can be implemented using an additional 2×1 MUX configured with the input A as the select line. The configuration is as follows:

- Select Line: A
- MUX Inputs: $I_0=B$, $I_1=0$

Functional operation:

- If A = 0: Output = B
- If A = 1: Output = 0

$$\text{Output} = A' \cdot B$$

The combination of these two MUX-based blocks yields a complete half subtractor, realized entirely in the optical domain using RSOA-based gain switching.

Performance and Validation:

The truth table detailing the correct logic operation of the half subtractor is presented in Table 7.19, while the simulated optical waveforms validating the difference and borrow outputs are depicted in Figure 7.20. These results demonstrate the circuit’s functional correctness, signal integrity, and feasibility within an RSOA-enabled MUX architecture.

Table 7.19: Truth Table HALF-SUBTRACTOR

INPUT A	INPUT B	SUB	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

7.4. Results

This chapter presents the simulation outcomes and performance analysis of the proposed all-optical logic circuits, realized using the Fredkin Reversible Gate (FRG) architecture integrated with Reflective Semiconductor Optical Amplifiers (RSOAs). All designs were evaluated under small-signal gain conditions, with a peak gain of approximately 20 dB, using Gaussian-shaped input pulses to emulate realistic optical transmission scenarios. The logical correctness and functional robustness of each circuit—including NOT, AND, OR, NAND, NOR, XOR, XNOR, Half-Adder, Half-Subtractor, and a 4×1 MUX—were validated using a Python-based simulation environment.

7.4.1 Performance Evaluation Metrics

The FRG-MUX-based circuits were assessed using three key optical performance parameters: Extinction Ratio (ER), Contrast Ratio (CR), and Relative Eye-Opening Percentage (REOP), which are critical indicators of optical signal integrity and system viability in photonic logic environments:

- Contrast Ratio (CR) quantifies the ratio of mean optical power in the logical high and low states:

$$CR = 10 \log_{10} \left(\frac{P_1}{P_0} \right)$$

where P1 and P0 denote the mean optical power levels corresponding to logic ‘1’ and logic ‘0’, respectively.

- Extinction Ratio (ER) measures the optical separation between logic levels by comparing the minimum power of logic ‘1’ with the maximum power of logic ‘0’:

$$ER = 10 \log_{10} \left(\frac{P_{\min}}{P_{\max}} \right)$$

- Relative Eye Opening (REOP) provides a normalized measure of signal clarity, defined as:

$$\text{REOP}(\%) = \left(\frac{P_{\min} - P_{\max}}{P_{\max}} \right) \times 100$$

These metrics collectively serve as quantitative indicators of the circuit's ability to distinguish between logical states, manage signal distortion, and operate reliably under variable optical input conditions.

7.4.2 Simulation Results and Analysis

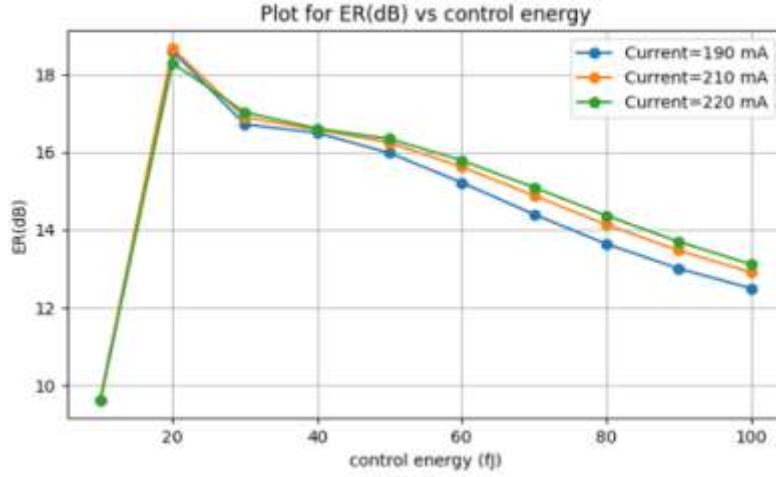
Under a bias current of 220 mA and control energy of 20 fJ, the RSOA-based FRG multiplexer achieved an ER of approximately 18 dB, a CR of 22 dB, and a REOP exceeding 99%, as shown in Figure 7.21. These values affirm excellent signal contrast and minimal inter-symbol interference, underscoring the design's effectiveness in supporting high-fidelity photonic computation.

To assess the robustness and scalability of the proposed circuits, a comparative performance evaluation was conducted against established designs, including hybrid plasmonic waveguide MUXes, electro-optic Mach–Zehnder interferometers (MZIs), and photonic crystal ring-resonator-based multiplexers. As summarized in Table 7.20, the RSOA–FRG-based approach delivers higher CR and ER, along with lower structural complexity and improved integration potential, establishing it as a superior alternative for all-optical signal routing and logic synthesis.

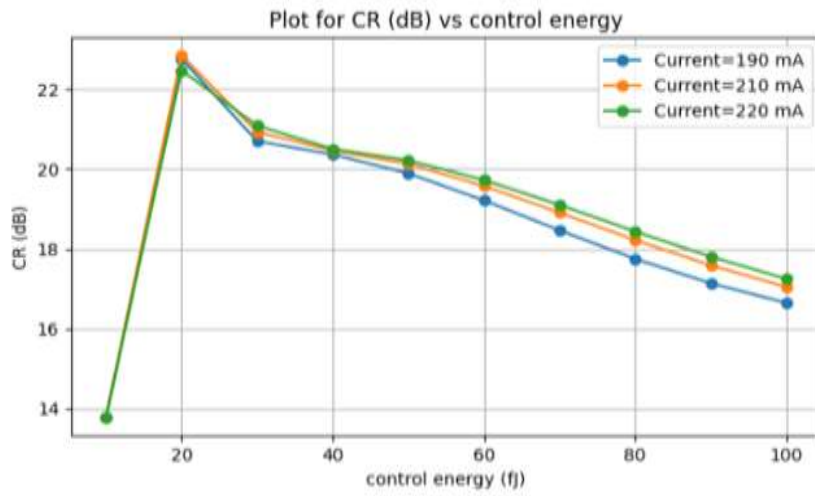
7.4.3 Effect of Bias Current and Control Energy

To evaluate the effect of varying bias current (I) and control energy (E_c) on the optical switching performance, simulations were performed across three bias levels: 190 mA, 210 mA, and 220 mA, while the control energy ranged from 10 fJ to 100 fJ. The results, depicted in Figure 7.21, reveal the following trends:

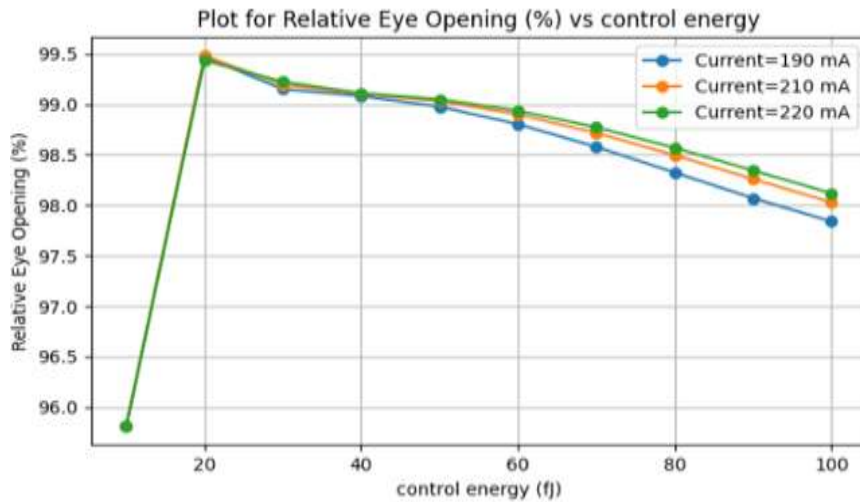
- Increasing bias current enhances ER, CR, and REOP, owing to stronger carrier population modulation and improved gain dynamics within the RSOA medium.
- Beyond 40 fJ, a saturation point emerges, where further increases in control energy lead to marginal decrease in performance, attributed to gain compression, carrier heating, and nonlinear distortion effects in the RSOA.
- The optimum operating point lies in the 20–40 fJ control energy range at ≥ 210 mA bias, balancing performance and power efficiency.



(a)



(b)



(c)

Figure 7.21: Performance analysis of the proposed RSOA-FRG-based 2×1 multiplexer under varying control energy and injection currents using cross-gain modulation (XGM). (a) Extinction Ratio (ER in dB), (b) Contrast Ratio (CR in dB), and (c) Relative Eye opening (%) versus control energy for injection currents of 190 mA, 210 mA, and 220 mA.

These plots correspond to the FRG output Q, which functions as the primary output of the 2×1 multiplexer. The results clearly indicate improved optical performance with increasing bias current, with performance saturation observed beyond 30 pJ due to gain compression and carrier heating effects.

Table 7.19: Performance parameter of proposed work

GATE	CI	GC	GO	OC	OD
FRG-2X1 MUX	0	5	1	3	2
NOT	2	5	2	3	2
AND	1	5	2	3	2
OR	1	5	2	3	2
NAND	1	7	2	5	3
NOR	2	7	3	5	3
XOR	1	7	2	5	3
XNOR	1	7	2	5	3
4X1 MUX	0	15	6	9	4

Table 7.20: Comparison table of proposed work with the other optical devices

Reference	ER (dB)	CR (dB)	REOP (%)	reversible
[138]	Not calculated	10.84	Not calculated	no
[139]	8.71	11.67	Not calculated	no
[140]	21.61	31.61	Not calculated	no
[141]	Not calculated	21.22	Not calculated	no
[142]	Not calculated	Not calculated	Not calculated	no
[50]	18.6	17.3	85.33	no
[63]	26	26.95	96	no
Our work	18.21	22.18	99.45	yes

These observations reinforce the need for precise bias-current tuning and energy-aware input optimization to maintain system stability and minimize energy losses, particularly for densely integrated photonic logic architectures. The simulation results decisively establish that the proposed FRG–RSOA–XGM framework enables scalable, ultrafast, and reliable optical logic circuits with superior extinction and contrast properties. The low insertion loss, fast carrier recovery of RSOAs, and reversibility of the Fredkin gate collectively contribute to a high-performance platform for implementing advanced optical computing primitives. The design is readily adaptable to large-scale Photonic Integrated Circuits (PICs) and Wavelength-Division Multiplexed (WDM) systems, offering a robust pathway toward future all-optical processors

7.5 Summary

This chapter presented the design and realization of an RSOA-based reversible universal multiplexer using the parity-preserving Fredkin Reversible Gate (FRG) as the fundamental optical switching primitive. By exploiting the controlled-swap functionality of the FRG and its inherent parity-preserving property, a 2×1 all-optical reversible multiplexer was implemented and further configured to realize a range of combinational logic circuits, including basic logic gates, a 4×1 multiplexer, and elementary arithmetic units such as a half-adder and a half-subtractor.

For generating complementary inputs required in certain logic realizations (e.g., NAND operation), a Feynman Gate (FG) was employed to obtain the inverted signal within the reversible optical domain. While this approach enables straightforward complement generation, it is noted that the FG is not parity-preserving, and therefore strict parity preservation is not maintained across all stages of the presented logic realizations. However, complete parity preservation can be achieved by replacing the FG-based inversion with parity-preserving alternatives such as the Double Feynman Gate (DFG) or the Fredkin Reversible Gate (FRG) configured for signal complementation. This observation highlights a clear design option for achieving fully parity-preserving realizations when required, without altering the overall multiplexer-based logic framework.

The proposed RSOA-based reversible multiplexer and derived logic circuits were evaluated under realistic photonic operating conditions. Performance evaluation showed an extinction ratio (ER) of approximately 18 dB, a contrast ratio (CR) of about 22 dB, and a relative eye-opening percentage (REOP) close to 99 %, confirming excellent signal quality, low distortion, and robust switching behaviour at high data rates. These results validate the suitability of the FRG-based optical multiplexer for reliable all-optical logic processing.

A qualitative comparative analysis further demonstrated that the proposed reversible RSOA–FRG design offers superior signal quality and improved integration potential compared to several existing non-reversible optical logic implementations, particularly due to its interferometer-free operation, reversible signal flow, and compatibility with photonic integrated circuit platforms.

Overall, this chapter establishes a flexible and modular methodology for constructing reversible and parity-aware all-optical combinational logic circuits using RSOA-based switching elements. The approaches developed here form a foundational layer for future research toward all-optical ALUs, reversible DSP blocks, photonic neuromorphic processors, and quantum-compatible reversible architectures. The work presented in this chapter is currently under peer review in an SCIE-indexed journal.

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Chapter 8: Conclusion and Future Work

8.1 Conclusion

This thesis presented a comprehensive investigation into the design, modelling, and realization of reversible arithmetic and logic circuits for fixed-point unsigned integer arithmetic, with a primary focus on all-optical and quantum-compatible computing architectures. Motivated by the growing demand for energy-efficient, high-speed, and scalable computation, the work systematically addressed the fundamental limitations of conventional irreversible electronic and interferometer-based optical systems by leveraging reversible logic principles and photonic switching technologies.

The research began by establishing a strong theoretical foundation in reversible computation, optical logic, and quantum arithmetic. Classical limitations related to information loss, heat dissipation, and scalability, as dictated by Landauer's principle, were identified as key challenges motivating the shift toward reversible and all-optical computation. A detailed literature survey revealed critical research gaps, particularly the absence of reversible complex multipliers, interferometer-free optical multiplier architectures, and parity-preserving reversible optical arithmetic units—gaps that directly shaped the objectives of this thesis.

In the quantum computing domain, a reversible 4x4-bit complex Vedic multiplier was developed using reversible (but not parity-preserving) quantum gates. The design followed the Urdhva–Tiryagbhyam (UT) sutra, enabling modular, hierarchical construction with analytically derived expressions for quantum cost, garbage outputs, constant inputs, and circuit depth. This work demonstrated that Vedic arithmetic can be efficiently mapped onto reversible and quantum-friendly architectures while maintaining scalability and structural regularity.

Transitioning to the optical domain, the thesis introduced an RSOA-based all-optical 2×2-bit reversible multiplier, realized using Feynman and Peres gates under cross-gain modulation (XGM). Unlike traditional MZI–SOA designs, the proposed architecture was interferometer-free, compact, and thermally stable. Extensive simulation results validated functional correctness and demonstrated excellent signal quality at 100 Gbps, with high extinction ratio (ER), Q-factor, and relative eye-opening percentage (REOP). This work established RSOA-based reversible gates as viable building blocks for high-speed photonic arithmetic.

Building upon this foundation, a scalable all-optical n-bit Vedic multiplier framework was developed in two phases. In Phase I, MZI–SOA-based n-bit Vedic multipliers were constructed using existing adder architectures and analytically compared with state-of-the-art designs to highlight optical cost–delay trade-offs and scalability limitations inherent to interferometric

systems. In Phase II, these limitations were addressed by proposing the first fully reversible, interferometer-free, RSOA-based n -bit Vedic multiplier, incorporating newly designed reversible ripple-carry and carry-save adders. Closed-form analytical expressions for optical cost, optical delay, constant inputs, and garbage outputs were derived, demonstrating predictable scalability and suitability for large-bit photonic arithmetic units.

A major contribution of this thesis is the first all-optical reversible complex multiplier, realized using RSOA-based parity-preserving logic gates. A compact parity-preserving 2×2 -bit reversible Vedic multiplier was designed using Double Feynman, parity-preserving Toffoli, and Modified Islam gates, enabling inherent fault detection through parity conservation. This unit was hierarchically extended to an n -bit complex Vedic multiplier, following the same methodological framework used in earlier quantum and optical designs. While photonic simulation was carried out for the 2×2 -bit parity-preserving reversible Vedic multiplier, which serves as the fundamental building block of the complex multiplier, the n -bit all-optical complex Vedic multiplier was constructed hierarchically using this validated unit. Based on this construction, closed-form analytical expressions for optical cost, optical delay, constant inputs, and garbage outputs were derived directly for the n -bit complex multiplier, thereby establishing scalability without requiring exhaustive photonic simulation at higher bit-widths.. To further enhance functional completeness, the thesis introduced a universal reversible NAND–NOR gate (NTG) using a hybrid MZI–SOA and RSOA configuration. Although not integrated into the final complex multiplier, the NTG establishes a reusable universal primitive for reversible optical logic synthesis and programmable photonic architectures.

Finally, the thesis presented an RSOA-based reversible universal multiplexer using the parity-preserving Fredkin Reversible Gate (FRG) as the core building block. The proposed multiplexer was systematically configured to realize basic logic gates, higher-order multiplexers, and arithmetic blocks. Performance evaluation confirmed high signal integrity, with $ER \approx 18$ dB, $CR \approx 22$ dB, and $REOP \approx 99\%$. While a non-parity-preserving Feynman gate was used to generate complementary inputs in selected configurations, the work clearly demonstrated that fully parity-preserving realizations are achievable using DFG or FRG alternatives, providing a clear design pathway for fault-tolerant optical logic.

In the optical realization of reversible logic gates and arithmetic circuits presented across Chapters 4 to 7, a variable optical attenuator (VOA) was consistently employed to normalize the input optical power levels. This normalization ensured that the probe and control signals operated within the optimal gain region of the RSOA, thereby preventing excessive gain saturation and maintaining stable cross-gain modulation (XGM) behaviour. The use of VOAs

was essential for achieving reliable switching performance, uniform logic-level contrast, and accurate evaluation of signal quality metrics such as extinction ratio, Q-factor, and relative eye opening. This practical consideration further strengthens the feasibility of the proposed RSOA-based reversible architectures for realistic photonic implementations.

Overall, this thesis establishes a unified, modular, and scalable framework for reversible arithmetic and logic design across quantum and optical domains, demonstrating that RSOA-based interferometer-free photonic architectures can effectively support reversible, parity-aware, and high-speed computation. Several parts of this work have been published in SCI/SCIE journals and international conferences, while others are currently under peer review, reflecting the originality and relevance of the research.

8.2 Limitations

While the results presented in this thesis are promising, several limitations must be acknowledged:

- **Physical fabrication and integration:** This work is primarily focused on logical-level design and numerical simulation. Practical aspects such as photonic integrated circuit (PIC) fabrication tolerances, packaging constraints, thermal crosstalk, and long-term device stability were not experimentally demonstrated and remain beyond the scope of this thesis.
- **Scaling overhead in reversible architectures:** Fully reversible optical designs inherently introduce increased optical cost (number of switching elements) and garbage outputs when compared to irreversible architectures. Although these overheads are analytically quantified in this work, further device-level and architectural optimization will be required to ensure practical scalability for large-bit-width systems.
- **Dynamic device non-idealities:** Effects such as amplified spontaneous emission (ASE), carrier recovery dynamics, polarization dependence, and component variability were considered at the modelling level. While polarization effects were mitigated using PI-RSOA assumptions in simulation, real-world implementations may exhibit additional non-idealities that require experimental calibration and compensation.
- **Thermodynamic and quantum-level validation:** Although logical reversibility theoretically minimizes information loss, a complete demonstration of thermodynamic benefits—such as approaching the $kT \ln 2$ energy limit per irreversible operation—requires device-level energy measurements, cryogenic operation, or quantum hardware platforms. Such experimental validation lies outside the scope of the present study.

8.3 Future Work

The work presented in this thesis establishes a comprehensive foundation for reversible combinational arithmetic circuit design in both quantum and all-optical domains. Building upon the proposed architectures, several important research directions remain open for future investigation:

1. **Extension from Fixed-Point Integer to Floating-Point Architectures:** The reversible arithmetic circuits developed in this thesis operate on fixed-point binary representations, supporting unsigned integer arithmetic. A natural extension of this work is the development of reversible floating-point arithmetic architectures, including floating-point adders, multipliers, and complex arithmetic units. Such designs will involve exponent alignment, mantissa normalization, rounding mechanisms, and exception handling, significantly broadening applicability to scientific computing, signal processing, and machine learning workloads.
2. **Floating-Point Realization in Quantum and Optical Domains:** Future research will explore floating-point reversible architectures in both quantum and optical computing paradigms.
 - In the quantum domain, this includes the design of low-quantum-cost floating-point circuits compatible with fault-tolerant quantum computing models.
 - In the optical domain, RSOA-based reversible logic can be extended to floating-point computation by incorporating optical normalization, exponent control, and power-balanced signal routing techniques.
3. **Quantum Circuit Simulation and Hardware Execution:** The quantum circuits proposed in this thesis were analytically evaluated using standard reversible and quantum cost metrics. Future work will involve simulation on real quantum simulators and experimental execution on available quantum hardware, enabling performance evaluation under realistic noise, decoherence, and hardware constraints. This step will bridge the gap between theoretical circuit design and practical quantum implementation.
4. **Extension from Combinational to Sequential Reversible Circuits:** This thesis primarily focuses on reversible combinational circuit design, including logic gates, adders, multipliers, and complex arithmetic units. An important future direction is the development of reversible sequential circuits, such as latches, flip-flops, registers, counters, and memory elements, in both quantum and optical domains. These components are essential for realizing complete reversible processors and control units.

5. **System-Level Integration of Reversible Computing Architectures:** Future research may focus on system-level integration of the proposed reversible arithmetic blocks into larger computing structures, such as reversible arithmetic logic units (ALUs), data-paths, and optical processing cores. Such integration will enable the development of fully reversible, energy-efficient, and quantum-compatible computing platforms suitable for next-generation photonic and hybrid quantum–optical systems.

8.4 Societal and Ethical Impact

The research presented in this thesis contributes to the long-term evolution of computing technologies by exploring reversible and all-optical circuit architectures aimed at improving energy efficiency, scalability, and computational sustainability. Although the work is primarily theoretical and simulation-based, its implications extend beyond technical innovation and intersect with broader societal and ethical considerations.

- **Energy Efficiency and Environmental Sustainability:** Modern digital infrastructure—data centers, communication networks, and high-performance computing platforms—accounts for a rapidly growing share of global energy consumption and carbon emissions. By investigating reversible logic and all-optical computation, this thesis addresses a fundamental limitation of conventional irreversible computing: unavoidable information loss and associated heat dissipation. Architectures based on reversible computation have the potential to significantly reduce energy consumption per operation, thereby contributing to environmentally sustainable computing paradigms. In the long term, such advances may help mitigate the ecological footprint of large-scale digital systems.
- **Societal Benefits of High-Speed and Low-Power Computing:** The development of ultrafast and energy-efficient photonic arithmetic units can enable future applications in communication systems, signal processing, scientific computing, and data analytics. Improved computational efficiency may enhance access to advanced technologies in areas such as healthcare diagnostics, climate modelling, and secure communications. By reducing power requirements, reversible photonic systems can also support deployment in resource-constrained environments, promoting broader technological inclusion.
- **Ethical Use of Emerging Computing Technologies:** As with any advanced computing technology, reversible and photonic processors may eventually be applied in systems that process sensitive data or influence decision-making processes. While

this thesis does not directly address applications involving personal data, artificial intelligence, or autonomous systems, the ethical deployment of future implementations must consider issues of transparency, accountability, and responsible use. Energy-efficient hardware alone does not guarantee ethical outcomes; it must be complemented by appropriate governance, regulation, and design practices at the system and application levels.

- **Alignment with Quantum-Compatible and Future Computing Paradigms:** The reversible architectures explored in this work align conceptually with quantum-compatible computation, which raises additional ethical considerations related to cryptography, data security, and computational power asymmetry. By focusing on foundational circuit-level design rather than application-specific exploitation, this thesis contributes responsibly to the knowledge base without enabling immediate misuse. Ethical challenges associated with quantum and photonic computing—such as cryptographic disruption—require coordinated responses from researchers, policymakers, and society at large.
- **Research Responsibility and Limitations:** This work remains at the modelling and simulation level and does not involve experimental deployment, human subjects, or real-world data. Consequently, immediate ethical risks are minimal. Nevertheless, the research emphasizes transparent reporting of assumptions, limitations, and performance metrics to avoid misleading conclusions. Acknowledging the gap between theoretical efficiency and practical deployment is essential for responsible scientific communication.

8.5 Concluding Remarks

Overall, the societal and ethical impact of this research lies in its contribution to sustainable, energy-aware computing and its alignment with responsible development of next-generation technologies. By advancing reversible and all-optical arithmetic at a fundamental level, this thesis supports long-term societal goals of environmental sustainability, technological efficiency, and ethical innovation, while recognizing that broader ethical implications will emerge as these technologies transition from theory to practice.

List of publication

Conference paper

- R. Jindal, D. Ruhela, “All-Optical N-bit Multiplier Design using Mach-Zehnder Interferometer”, IEEE International Conference for Emerging Technology (INCET), 2021. (SCOPUS INDEX).
- D. Ruhela, R. Jindal, “All-Optical N-Bit Reversible Complex Multiplier”, IEEE 8th International Conference on Signal Processing and Communication (ICSC), 2022. (SCOPUS INDEX)

Journal paper (SCI/SCIE index)

- Ruhela, D., Jindal, R.: “Design and simulation of all-optical 2×2-bit reversible multiplier using RSOA-based switches”, Indian Journal of Pure & Applied Physics Vol. 63, July 2025, pp. 626-637 DOI: 10.56042/ijpap.v63i7.18507. Impact Factor: .8
- Ruhela, Diksha, and Rajni Jindal. "Low-power computing with reversible logic: A modular approach to Vedic multiplication", *Journal of Computational Electronics*, vol. 24, no. 1, 2025, p. 155. Springer, <https://doi.org/10.1007/s10825-025-02396-1>. Impact factor: 2.5
- R. Jindal, D. Ruhela, “RSOA-Based Reversible Logic Design: A Scalable Approach for Optical Gates and Multiplexers Using FRG Architecture” (SCIE INDEX JOURNAL, Accepted)

Communicated paper

- Ruhela, D., Jindal, R. “Design and Simulation of a Parity-Preserving Reversible Optical Multiplier Realized with RSOA-Based XGM Switching” (SCIE INDEX JOURNAL)
- D. Ruhela, R. Jindal, “All-Optical Implementation of Reversible n-Bit Multiplier”, (SCOPUS INDEX CONFERENCE)

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