DESIGN AND ANALYSIS OF SYNCHRONIZATION TECHNIQUES FOR CONTROL OF POWER ELECTRONIC CONVERTERS

A Thesis Submitted in Partial Fulfilment of the Requirement

for the Degree of

DOCTOR OF PHILOSOPHY

by

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v_s	grid voltage supply (volt)
V_A	amplitude of the input voltage (volt)
K_{PD}	gain of phase detector
K_p	proportional gain of PI controller of single phase SRF PLL
K_I	integral gain of PI controller of single phase SRF PLL
$\frac{T}{4}$	90º time delay (º)
T	time period of supply voltage (s)
v_α	α component of supply voltage signal in stationary reference frame (αβ) (Volt)
v_β	β component of supply voltages signal in stationary reference frame (αβ) (Volt)
ω_{nf}	nominal angular frequency of SRF PLL (rad/s)
ω_{cf}	control angular frequency (rad/s)
ω_O	estimated frequency (rad/s)
ω_{est}	estimated frequency (rad/s)
θ_{in}	input signal phase angle (º)
θ_{est}	estimated phase angle (º)
θ_{err}	phase error (º)
v_d	the d-axis component of input voltage (Volt)
v_q	quadrature- axis component of input voltage (Volt)
${}_aD_T^{rl}$	Fractional Calculus's Basic Operator
ω_{ff}	nominal frequency of MSRF PLL (rad/s)
θ_{input}	phase angle of input voltage of MSRF PLL
θ_{error}	phase error of MSRF PLL (º)
θ_{out}	estimated signal's phase angle of MSRF PLL (º)
$v_{s\alpha}$	α component of supply voltage signal in stationary reference frame (αβ) of MSRF PLL (Volt)
v_{sq}	β component of supply voltages signal in stationary reference frame (αβ) of MSRF PLL (Volt)
K_{PD}	damping factor (Ns/m)
s^a, s^b	Fractional exponent operator
ω_{pc}	phase crossover frequencies (rad/s)
ω_{gc}	gain crossover frequencies (rad/s)
T_{LF}	transfer function of Loop Filter
Tf_{VCO}	transfer function of VCO
$T_{1-\emptyset SRF}$	Open Loop Transfer Function of single Phase SRF PLL
$H_{1-\varphi SRF}$	Closed Loop Transfer Function of single phase SRF PLL
T_Q	closed loop transfer function of quadrature component of phase signal of single phase SOGI PLL
T_E	transfer function of error signal of phase signal of single phase SOGI PLL
x*(k)	reference input signal of LMS PLL (V)
$W(k+1)$	weight updation
T_{LMS}	open loop transfer function of single LMS
T_{clLMS}	closed loop transfer function of LMS
e_{ser}	error signal of LMS PLL (V)
$\xi(k)$	cost function
v(k)	estimated output of the LMS PLL (V)

Tf_{FO-PD}	transfer function of phase detector
$\mathrm{Tf_{FO-LP}}$	transfer functions of fractional low pass filter
$\mathrm{Tf_{FO-PI}}$	transfer function of fractional-order proportional plus integral
θ_{in}	phase angle of input voltage of three phase SRF PLL (°)
$T_{3-\varphi SRF}$	open loop transfer function of the 3-phase SRF PLL
$T_{cl3-\varphi SRF}$	closed loop transfer function of the 3-phase SRF PLL
$\mathrm{e_{ser}}$	error signal of 3-phase LMF PLL (Volt)
u(k)	reference input signal of 3-phase LMF PLL (Volt)
v (k)	estimated output signal of 3-phase LMF PLL (Volt)
V_{ter}	terminal voltage of 3-phase LMF PLL (Volt)
V_m	amplitude of the terminal voltage of 3-phase LMF PLL (Volt)
μ_d	adaptive constant
e_{serda}	adaptive active component error of phase 'a' (Volt)
PM	Phase margin (radian)
GM	Gain margin (dB)
ω_{pc}	phase cross over frequency (rad/s)
ω_{gc}	gain cross over frequency (rad/s)
T_ω	window length of MAF (s)
V_{dc}^*	Reference voltage (Volts)
i_d^*	d-axis reference current (Ampere)
i_q	q-axis reference current (Ampere)
ω_s	Stator angular frequencies (rad/s)
ω_r	Rotor angular frequencies (rad/s)
C_p	power coefficients
C_t	torque coefficient
R_s	stator resistance (ohm)
R_r	rotor resistance (ohm)
n_s	synchronous speed (rpm)
ω_{slip}	slip frequency (rad/s)
ω_m	mechanical speed of rotor (rad/s)
$\mathrm{L_{ls}}$, $\mathrm{L_{lr}}$	stator and rotor leakage inductance (H)
T_e	electromechanically torque (N/m)
ψ_s, ψ_r	stator flux, rotor flux (Wb)
$\mathrm{L_m}$	magnetising inductance
θ_{slip}	slip angle (°)
P_g	Active power (Watt)
Q_g	Reactive power (VAR)

LIST OF ABBREVIATIONS

PLL	Phase-Locked Loop
LF	Loop filter
PD	Phase Detector
PI	Proportional Plus Integral
VCO	Voltage-Controlled Oscillator
SRF	Synchronous Reference Frame
SOGI	Second-Order Generalized Integrator
EPLL	Enhanced Phase Locked Loop
ZCD	Zero-Crossing Detection-Based Methods
FLL	Frequency-Locked Loop
DVR	Dynamic Voltage Restorer
D-STATCOM	Distribution Static Compensator
FACTS	Flexible AC Transmission Systems
STATCOM	Static Synchronous Compensator
SVC	Static VAR Compensator
SSSC	Static Synchronous Series Compensator
UPFC	Unified Power Flow Controller
DERs	Distributed Energy Resources
DDSRF	Decoupled Double Synchronous Reference Frame
MSRF	Modified Synchronization Frame
FO-LP MSRF	Fractional Order Low Pass Modified Synchronization Frame
FO-LPFO-PI MSRF	Fractional Order Low Pass Filter and Loop Filter Modified Synchronous Reference Frame Phase Locked Loop
H-LMS-SOGI	Hybrid Least Mean Square Second Order Generalized Integral CLMS Cascaded Least Mean Square
CSOGI	Cascaded Second Order Generalised Integrator
DG	Distributed Generation
KF	Kalman Filter
MAF	Moving Average Filter
DFT	Discrete Fourier Transform

ANF	Adaptive Notch Filter
LPF	Low Pass Filter
SVF	Space Vector Filter
EKF	Extended Kalman Filter
WLSE	Weighted Least Squares Estimation
ADALINE	Adaptive Linear Neuron
MSOGI	Multiple-Second Order Generalized Integral
HCDFT	Half-Cycle Discrete Fourier Transform
THD	Total Harmonic Distortion
RBFNN	Radial-Basis-Function Networks
SOGI-FLL	Second-Order Generalized Integrator- Frequency-Locked Loop DSOGI Dual Second Order Generalised Integrator
PV	Photovoltaic
APU	Auxiliary Power Unit
MCCF	Multiple-Complex Coefficient-Filter-Based
FXLMS	Filtered-X Least Mean Square
FXLMF	Filtered-X Least Mean Fourth
LFXLMF	Leaky Filtered-X Least Mean Fourth
DDSRF	Decoupled Double Synchronous Reference Frame
DFIG	Doubly-Fed Induction Generator
FONF	Fractional-Order Notch Filter
FOC	Fractional-Order Controller
FA-EPLL	Frequency-Adaptive Enhanced PLL
ALC	Adaptive Linear Combiner
FAC	Frequency-Adaptive Compensation
LMS	Least Mean Square
LMF	Least-Mean Fourth
FOMCON	Fractional-Order Modelling and Control
FOTF	Fractional Order Transfer Function
OPAL-RT	OPAL Real Time Simulator
DFIG	Doubly Fed Induction Generator

WT	Wind turbine
WECS	Wind Energy Conversion System
GSC	Grid side converter
RSC	Rotor side converter
V_{dc}	DC link voltage
PWM	Pulse width modulation
DC	direct current
MPPT	Maximum power point tracking
K_{PD}	Gain of Phase Detector of MSRF PLL
DSO	Digital Signal Oscilloscope
HIL	hardware-in-the-loop
T_D	closed loop transfer function of in-phase component of phase signal of single phase SOGI PLL
K_p	proportional gain of PI controller of MSRF PLL
K_i	integral gain of PI controller of MSRF PLL
Tf_{LGMSRF}	open loop transfer function of MSRF PLL
Tf_{clMSRF}	closed loop transfer function of MSRF PLL

ABSTRACT

The increasing integration of renewable energy sources into electrical power systems has necessitated advanced synchronization techniques for power electronics converters. This thesis investigates synchronization methods, with particular emphasis on Phase-Locked Loop (PLL) technologies, to address challenges in grid-integrated systems under various disturbances. The primary objective is to develop and validate enhanced synchronization algorithms that overcome limitations of conventional PLLs in applications including photovoltaic systems, doubly fed induction generator (DFIG) wind energy converters, and electric vehicles.

A comprehensive methodology combining mathematical modelling, stability analysis, extensive MATLAB Simulink simulations, and experimental validation using OPAL-RT real-time simulator was employed. Multiple PLL architectures were evaluated under abnormal grid conditions including voltage sags/swells, frequency jumps, DC offsets, and harmonic distortions. The research examined single-phase and three-phase PLLs, including Synchronous Reference Frame (SRF), Second-Order Generalized Integrator (SOGI), Least Mean Square (LMS), Least Mean Fourth (LMF), Modified Synchronous Reference Frame (MSRF), and fractional-order PLLs.

Key findings demonstrate that the LMF PLL outperforms SRF PLL under phase shift and frequency change disturbances, while Type III Enhanced PLL exhibits superior frequency response with polluted grid voltage and DC offset. The proposed fractional-order FO-LPFO-PI MSRF-PLL with optimized parameters shows enhanced stability during grid abnormalities. Additionally, the novel H-LMS-SOGI PLL architecture provides exceptional dynamic responses, surpassing conventional structures under all adverse grid conditions tested. Experimental validation of DFIG systems with LMF-PLL confirms satisfactory performance under variable wind speeds and grid disturbances.

This research significantly contributes to grid stability and renewable energy integration by providing validated solutions for maintaining reliable power system operation with high penetration of distributed energy resources. The dual validation approach ensures practical applicability, offering a comprehensive framework for

designing robust power electronics-based systems capable of handling complex grid disturbances in modern power networks.

Chapter: 1

INTRODUCTION

1.1 State of the Art of Synchronization Techniques

Synchronization is a fundamental requirement in modern electrical power systems. Nowadays there is increased global shift towards sustainable energy due to alarming global warming caused by greenhouse gases and need to meet the increasing energy demand using power electronic–based converters in modern distribution systems. Conventionally, synchronization in power systems was achieved inherently through synchronous generators, which naturally align their voltage magnitude, frequency, and phase angle with the grid. However, the transition from conventional generation to power electronics converter-interfaced generation has necessitated advanced synchronization techniques.

State-of-the-art of synchronization techniques mainly rely on signal processing and control algorithms. Phase angle, voltage frequency, and voltage magnitude at the PCC of the utility grid are the important parameters which are used for grid synchronization as well as operational control, dynamic analysis and protection. Among various methods commonly employed Phase-Locked Loop (PLL) based techniques are the most widely adopted due to their simplicity, robustness, and ease of implementation. Several enhanced PLL structures, such as Synchronous Reference Frame PLL (SRF-PLL), Second-Order Generalized Integrator PLL (SOGI-PLL), and Enhanced PLL (EPLL) have been developed to improve performance under distorted and unbalanced grid conditions.

Different alternative synchronization techniques in the literature can be broadly divided into the following categories like (a) zero-crossing detection-based methods (ZCD), (b) frequency-locked loop (FLL), (c) phase-locked loop (PLL), and (d) filtering based methods (including Fourier transform, Kalman, moving average, and notch filters). In recent years, development of FLL, enhanced PLL (EPLL) aim to overcome the limitations of conventional PLLs, especially in abnormal circumstances

like voltage sag/swell, frequency jumps, dc offset, harmonic content, phase jump etc. The SRF PLL is the most commonly used technique because of its simple implementation and superior dynamic performance over the other techniques The state of the art thus reflects a transition from purely grid-following synchronization techniques toward more resilient and adaptive synchronization strategies.

1.2 Role of Synchronization in Electrical Power Systems

In order to reduce the deterioration in power quality due to integration of renewable energy sources to the conventional grid system, several power electronic devices are connected to the distribution system. In power distribution systems, Custom Power Devices like Dynamic Voltage Restorer (DVR), Distribution Static Compensator (D-STATCOM) and FACTS (Flexible AC Transmission Systems) devices, like: Static Synchronous Compensator (STATCOM), Static VAR Compensator (SVC), Static Synchronous Series Compensator (SSSC), Unified Power Flow Controller (UPFC) etc are used to improve the power quality. Synchronization plays a very important role in ensuring the stable and reliable operation of electrical power systems. These grid-connected devices have to be precisely synchronized with grid voltage. Therefore, accurate phase angle information, magnitude and frequency of grid voltage is indispensable for proper operation of every grid-connected power converter. It ensures that multiple generators or distributed energy resources (DERs) operate coherently with the grid by matching their voltage magnitude, frequency, and phase angle. Proper synchronization is essential before connecting any generation unit to the grid to prevent large transient currents, voltage disturbances, or system instability.

In power electronic–based systems, synchronization enables accurate control of active and reactive power exchange between the converter and the grid. It also supports essential grid services such as voltage regulation, frequency support, and power quality improvement. Inaccurate or delayed synchronization can lead to control errors, power oscillations, and even system collapse in extreme cases.

With the increasing integration of renewable energy sources such as wind and solar power, synchronization has become even more crucial. These sources lack inherent

rotational inertia and depend entirely on control algorithms for grid interaction. Therefore, effective synchronization techniques are vital for maintaining system stability, especially under dynamic operating conditions.

1.3 Issues in Synchronization of Integrated Systems

Integrated power systems combining conventional generation, renewable energy

sources, energy storage systems, and loads, present several synchronization challenges. One major issue arises from grid disturbances such as voltage sags and swell, harmonics, phase angle change, frequency deviations, and presence of DC-offset as unbalanced conditions. These disturbances can degrade the accuracy of synchronization techniques and affect converter performance.

Another issue is the increasing presence of weak grids, characterized by low short-circuit ratios and high grid impedance. In such systems, conventional synchronization techniques may experience slow response, oscillations, or instability. Additionally, interactions between multiple converters operating with similar synchronization mechanisms can lead to adverse coupling effects.

The variability and intermittency of renewable energy sources further complicate synchronization uses as frequent changes in operating conditions demand fast and robust tracking of grid parameters. There are several important aspects to be considered in renewable energy based integrated systems; (i) variability and intermittency of renewable energy sources like fluctuation of solar generation with daily/seasonal cycles and weather conditions and rapid power fluctuations from wind power output caused by fluctuation in wind speed. (ii) voltage and frequency stability issues due to insufficient reactive power support, and frequency deviations. (iii) bidirectional power flow and grid infrastructure limitations as traditional grids were designed for unidirectional power flow so it creates challenges as the existing infrastructure require bidirectional flows from distributed generation, due to the connection of RES and power electronic converters. (iv) synchronization of distributed energy resources (DERs); the proliferation of DERs introduces synchronization

complexities and can introduce frequency/voltage fluctuations. (v) protection and control system challenges; fault currents from power electronic devices create interface problems and need advanced control strategies to manage variability. (vi) power quality issues; renewable integration introduces several power qualities concerns like harmonic distortion from power electronic converters, voltage sags/swells during synchronization, flicker from rapid power variations, need for harmonic filtering and reactive power compensation hence Grid Codes must address these power quality aspects. (vii) Grid Codes and Regulatory Challenges; standards like Grid Codes must address fault ride-through, reactive power regulation and this requires implementation of grid codes. (viii) cybersecurity threats; digitalization causes smart grids to face hardware attacks, ransomware, traffic overloads, hence inefficient synchronization systems could destabilize the grid.

1.4 Classification of Synchronization Techniques

Synchronization techniques in electrical power systems can be broadly classified as single phase and three phase synchronization techniques based on the types of phase connections. They are further divided into open loop and closed loop synchronisation techniques. While closed loop systems update the predicted value of phase using a feedback loop mechanism, open-loop approaches directly estimate the magnitude, phase, and frequency of the input signals. The estimated value of the signal is locked to its actual value by this loop.

A. Single phase open loop synchronous techniques

B. Single phase closed loop synchronous techniques

C. Three phase open loop synchronous techniques

D. Three phase closed loop synchronous techniques

PLL-Based Synchronization Techniques estimate the grid phase angle and frequency using feedback control loops. Examples include SRF-PLL, SOGI-PLL, and EPLL. They are widely used in grid-following converters.

1. **FLL-Based Synchronization Techniques**

   Frequency-locked loops focus on frequency estimation and are often combined with PLLs to improve performance under frequency variations.

2. **Grid-Following Synchronization**

   In this approach, converters rely on the grid voltage as a reference and synchronize accordingly. PLL-based methods dominate this category.

3. **Grid-Forming Synchronization**

   Grid-forming converters establish their own voltage and frequency references, enabling operation in weak or islanded grids. Virtual synchronous machines and droop control
   fall under this category.

4. **Hybrid Synchronization Techniques**

   These methods combine grid-following and grid-forming features to enhance system
   flexibility and robustness.

1.5 Challenges and Solutions in Synchronization of Integrated Systems

The synchronization of integrated power systems faces several technical challenges due to the complex interaction between multiple generation units and varying grid conditions. Addressing these challenges requires both advanced control strategies and improved synchronization algorithms.

1.5.1 Challenges of Grid Synchronization Using PLL

Despite their widespread use, PLL-based synchronization techniques face several limitations:

- **Sensitivity to Grid Disturbances:** PLLs are highly sensitive to voltage harmonics, unbalance, and noise, which can lead to inaccurate phase estimation.
- **Poor Performance in Weak Grids:** In weak grid conditions, PLLs may introduce instability and slow dynamic response.
- **Frequency and Phase Oscillations:** Rapid grid changes can cause oscillations in estimated frequency and phase angle.
- **Coupling with Control Loops:** Interaction between PLL dynamics and converter control loops can degrade overall system stability.
- **Limited Robustness under Fault Conditions:** Voltage sags and faults can cause PLL loss of synchronization.

1.5.2 Solutions to the Challenges of Grid Synchronization Using PLL

To overcome the challenges associated with PLL-based synchronization, several solutions have been proposed:

- **Advanced PLL Structures:** Techniques such as SOGI-PLL and decoupled double synchronous reference frame PLL (DDSRF-PLL) improve performance under unbalanced and distorted conditions.
- **Adaptive Control Techniques:** Adaptive bandwidth and gain tuning enhance PLL robustness under varying grid strengths.
- **Filtering and Signal Conditioning:** Improved filtering techniques reduce the impact of harmonics and noise on PLL operation.
- **Hybrid Synchronization Approaches:** Combining PLL-based methods with grid-

  forming or virtual inertia techniques enhances stability in weak grids.

- **Fault-Tolerant Control Strategies:** Designing PLLs capable of maintaining synchronization during grid faults improves system reliability.

1.6 Thesis structure

The content of the thesis work is organised into the following chapters.

CHAPTER 1: This chapter deals with introduction, state of art of synchronization techniques, role of synchronization in electrical power system, issues faced in synchronization of integrated system, classification of synchronization techniques, challenges and solutions in synchronization of integrated system.

CHAPTER 2: This chapter deals with the extensive literature review based on classification of single-phase open loop and closed loop synchronization techniques, three phase open loop and closed loop synchronization techniques, single and three phase Phase-Locked Loop (PLL) dealing with both conventional and advanced algorithms.

CHAPTER 3: This chapter discuss the design and mathematical modelling, and analysis of single phase PLLs like SRF, MSRF, SOGI, LMS and three phase PLLs like SRF and LMF PLL. Performance analysis of these PLLs under grid abnormalities like voltage sag, swell, frequency change, polluted grid voltage, phase shift, DC offset through MATLAB Simulink is also validated by using laboratory hardware set up.

CHAPTER 4: This chapter deals design of different Types and orders of a typical PLL. Design of Types I, Type II and Type III PLLs is carried out in this chapter. It also discusses the stability analysis of Type I, Type II and Type III PLLs through bode diagrams. Dynamic performance analysis under grid abnormalities like voltage sag, swell, frequency change, polluted grid voltage, phase shift, DC offset using MATLAB Simulink are validated experimentally. The comparison between different types is carried out to observe their suitability under grid abnormalities.

CHAPTER 5: This chapter discuss the mathematical modelling for the design of fractional order PLLs like fractional order low pass modified synchronization frame phase locked loop (FO-LP MSRF-PLL) with only one fractional order parameter ‘a’ and fractional order low pass filter and loop filter modified synchronous reference frame phase locked loop (FO-LPFO-PI MSRF-PLL) with two fractional order parameters like ‘a’ and ‘b’. Steady state stability analysis is carried out using bode

diagram. Dynamic performance analysis under grid abnormalities like voltage sag and swell, frequency change, polluted grid voltage, phase shift, DC offset is verified using Simulation and experimental studies also.

CHAPTER 6: This chapter discuss the mathematical modelling for the design of a hybrid phase locked loops (H-LMS-SOGI). Modelling of cascaded LMS and cascaded SOGI PLL and H-LMS-PLL is carried out. Simulation and experimental studies are analyzed under grid abnormalities like voltage sag, swell, frequency change, polluted grid voltage, phase shift, DC offset is also included in this Chapter.

CHAPTER 7: This chapter discuss the modelling of LMF PLL for application to a DFIG -grid integrated system to analyse the performance under grid abnormalities like voltage sag, swell, frequency change, polluted grid voltage, phase shift, DC offset using MATLAB Simulink results are validated by OPAL-RT real-time simulator. The performance analysis is done under varying wind speed and constant wind speed conditions.

Chapter 8: This chapter deals with the summary of the conventional single phase, three phase PLLs like SRF, SOGI, LMS, MSRF and advanced versions like cascaded LMS (CLMS), cascaded SOGI (CSOGI), cascaded hybrid LMS-SOGI (H-LMS-SOGI) PLLs, and application of LMF PLL in DFIG wind energy converter system.

In the last section of the chapter a future scope of work is presented.

Chapter: 2

LITERATURE SURVEY

2.1 General

The previous chapter provides a detailed introduction to the synchronization techniques, role of synchronization in electrical power system, related issues in synchronization of integrated system, the classification of synchronization techniques, challenges and solutions in synchronization of integrated system, challenges of grid synchronisation using PLL and the solutions to the challenges of Grid Synchronisation using PLL. In the previous chapter the various classification of synchronization techniques based on both conventional and advanced methods has been mentioned and discussed.

In this chapter an extensive literature survey on several classification of grid synchronization techniques for resources based on power electronic converters is discussed for tracking the phase and frequency of the system. The literature survey of the synchronization techniques is broadly classified into single phase and three phase synchronizations based on the control system. These classifications are subdivided into open loop and closed loop synchronization techniques based on the absence or presence of feedback system and it focuses on various alternative techniques for estimating the phase and frequency of the system. The literature survey tries to cover both the conventional and advanced synchronization techniques of the single phase and three phase for the open loop and closed loop system.

2.1.1 Literature Survey on Single Phase Open Loop Synchronization Techniques

Synchronization techniques perform a vital role in controlling the single-phase power electronic converters as they are responsible for ensuring a smooth connection of the grid tied inverters and monitoring utility issues. An innovative open-loop synchronization approach for single-phase grid systems has been introduced that eliminate the feedback loop inherent in PLL systems, ensuring unconditional stability, estimate grid phase and frequency directly from filtered signals and achieve high

harmonic rejection and robustness under distorted grid voltages. This open-loop methods provide inherently stable, fast, and computationally efficient synchronization, though frequency adaptability remains challenging under grid variations [1]-[3]. Numerous synchronization techniques have been proposed in literature due to rapid expansion of distributed generation (DG) in power grid [4]. A multistage filtering approach to eliminate false crossings caused by notches and DC offsets during zero-crossing detection in thyristor converters is introduced providing phase accuracy without signal distortion [5]. The frequency-dependent properties of the filters used in open loop synchronization techniques cause inaccuracies in amplitude and phase estimates so using a parallel frequency detector to adjust the prefiltering step in response to frequency fluctuation is mentioned in literature [6]-[10]. The grid voltage fundamental frequency of the positive sequence component is extracted using various operators in [11]-[17]. Thus, the synchronization in zero crossing Detection approach relies on estimating phase by detecting the zero crossing of a reference signal and frequency [18]. The use of the Kalman Filter (KF) is mentioned as another method of synchronization technique. For linear Kalman filters, an additional frequency estimation block (PLL/FLL) is required [19,20]. The Nonlinear Kalman filter uses an expanded state-space model to convert the parameter estimation issue into a state estimation problem, taking into account the unknown frequency as an additional variable. The nonlinear Kalman filter is computationally expensive and very sensitive to initial conditions and noise parameter tuning [21Constant zero serves as the quadrature signal in the anti-conjugate harmonic decomposition and cascaded delayed signal cancellation open loop synchronization technique, which is entirely open-loop [22]. The actual grid frequency is not compulsory for phase error compensation while using the moving average filter (MAF)-prefilter method in grid synchronization technique [23]. Modified Discrete Fourier Transform (DFT) has been applied in order to remove the decaying DC components more successfully and mentioned in [24]-[25]. For estimating the frequency of a pure sinusoidal signal, an adaptive notch filter (ANF) with global convergence property and a modified ANF structure that can determine the fundamental frequency of any periodic signal, including pure sinusoidal signals has been mentioned in [26]. An efficient harmonic detection technique based on a radial-basis-function neural network is developed to enhance power quality. It is

perceived as an advanced form of open loop synchronization technique. [27] requires less sampled data points for harmonic assessment and delivers higher accuracy in calculating harmonic amplitudes when compared to various other popular conventional methods [27,28]. An improved four-sample technique for grid frequency estimation is mentioned in [29] which corrects amplitude and phase errors brought on by frequency drift while maintaining accuracy under frequency fluctuations and disturbances. This technique is resistant to DC offsets in the grid voltage has quick dynamic response, and efficiently suppresses harmonics [29]. Low pass filter (LPF) method, Space vector filter (SVF) based method, extended Kalman filter (EKF) based method and weighted least squares estimation (WLSE) based method of open loop synchronisation techniques has also been mentioned in [30,31] which calculate phase angle of the voltage which is based on $\alpha\beta$- frame signals. Compared to Kalman filters, ANN-based methods based on the adaptive linear combiner (Adaline) produce estimates that are faster and more accurate [32]. Another new adaptive neural phase-locked loop (AN-PLL) is present in literature for grid-connected converter synchronization that is based on an adaptive linear neuron (ADALINE) [33,34].

2.1.2 Literature Survey on Three Phase Open Loop Synchronization Techniques

Three-phase grid-tied systems are more popular for high-power applications over single-phase systems because they provide practically continuous power flow and can minimize excessive asymmetry in utility grid current. A high-efficiency three-phase grid-connected inverter system is designed for increasing the efficiency while preserving low current total harmonic distortion (THD), which is essential for renewable energy applications [35]. The three-phase open loop synchronization techniques also analysed the grid parameters directly and are typically based on filtering units like low pass filtering (LPF), Kalman filter (KF), space vector filter (SVF), weighted least square estimation (WLSE). Three phase open loop synchronization techniques with LPF provide effective filtering at lower cut-off frequencies but show slow response at steady frequencies and are sensitive to grid voltage imbalance and phase variations. KF based open loop synchronization techniques can work both in imbalanced and distorted grid conditions, on phase shift, and is frequency adaptable [36]. However, it has high computational workload,

difficulty in covariance matrices measurement, and has prolonged convergence time. The SVF synchronization algorithm [30] can operate sufficiently under harmonics distortion and phase shift however it introduces phase shift under grid frequency variations. WLSE filter based open loop synchronization techniques has fast detection of phase angle. It can calculate negative and positive sequence components individually and with frequency variation. They are sensitive to noise and harmonics and have high level of computational complexity [37, 38].

2.1.3 Literature Survey on Single Phase Closed Loop Synchronization Techniques

Single-phase closed-loop synchronization techniques are essential both in power and energy systems for accurate estimation of grid phase, frequency, and amplitude, especially during non-ideal grid conditions such as frequency change, harmonics, dc offsets, phase and voltage changes. Closed-loop synchronization uses feedback, which provides better robustness and dynamic performance than open-loop techniques [1]-[3]. Single-phase closed-loop synchronization techniques are widely used in grid-connected power electronic systems, particularly in single-phase photovoltaic (PV) inverters, to accurately estimate grid phase angle and frequency. Unlike open-loop methods, closed-loop techniques employ feedback mechanisms to continuously minimize synchronization errors, making them more robust under grid disturbances such as voltage sags, harmonics, noise, and frequency variations. In single phase closed loop synchronization techniques a loop mechanism is used to continuously update the phase estimation for locking the estimated phase value to its actual value [39]. The two main types of closed-loop synchronization are frequency-locked loops (FLLs) and phase-locked loops (PLLs). Single-phase FLLs are implemented in the stationary reference frame, which makes them especially appropriate for single-phase systems, whereas PLLs function in the synchronous reference frame [40]. Second-order generalized integrators (SOGI), adaptive notch filters, and enhanced PLLs (EPLL). SOGI-PLL, EPLL DC-rejection SOGI-FLLs for mitigating dc offsets, Multiple-SOGI FLLs (MSOGI-FLLs) have been used for selective harmonic rejection and SOGI-FLLs with prefilters or in-loop filters for improved harmonic and inter harmonic attenuation etc have been developed recently

as closed loop synchronization techniques [41]- [45]. An enhanced half-cycle discrete Fourier transform (HCDFT) algorithm is discussed in [46] to estimate phasors in numerical relays quickly. By employing an alternating-sample decimation methodology, the strategy reduced the impact of decaying DC components produced during fault transients. This improvement makes a compromise between computational simplicity and transient response, offering half-cycle DFT performance without sacrificing full-cycle computation accuracy [47,48]. A recursive estimating technique that used a least-error-square approach to adaptively track fading DC components in power signals was presented. Relay performance during fault initiation and clearance was enhanced by the algorithm's real-time determination of exponential decay constants. [49,50]. In order to improve harmonic rejection and transient tracking, a new design that incorporates a Kalman estimator as a prefilter within the PLL loop is presented [51]. This method produced cleaner αβ components, improving phase estimation reliability in distorted single-phase situations [52]. Radial-basis-function networks (RBFNN) are used in a neural network technique for harmonic detection. Under nonlinear situations, the RBFNN outperformed the FFT and ADALINE algorithms in terms of accuracy and convergence speed. The paper demonstrated how AI was initially included into power quality analysis [27]. A fundamental method for single-phase synchronization called the second-order generalized integrator-based frequency-locked loop (SOGI-FLL) has been introduced in [45]. For αβ transformations, the SOGI structure produced orthogonal components, while the FLL tracked grid frequency adaptively. The stability, harmonic immunity, and ease of use of this technique on digital controllers has led to its widespread application [53]-[55].

2.1.4 Literature Survey on Three Phase Closed Loop Synchronization Techniques

Grid-connected power converters frequently employ three-phase closed-loop synchronization algorithms to precisely predict the grid voltage phase angle and frequency under real-world circumstances including harmonics in grid voltage, unbalance, and frequency fluctuations. Closed-loop techniques provide better dynamic performance and robustness than open-loop systems because they continuously correct the estimated phase via feedback. For medium- and high-power applications, grid-tied

photovoltaic (PV) and converter-based systems frequently use three-phase closed-loop synchronization techniques. The most popular closed-loop synchronization technique for three-phase systems is the SRF-PLL [56]- [60]. Enhanced PLL-based synchronization technique uses a nonlinear dynamical system that provides robust resistance to noise, harmonics, frequency fluctuations, and imbalanced circumstances [61]. Two modifications of the single-phase enhanced phase locked loop (EPLL) for three-phase systems are seen in literature [61]-[70]. For variable-frequency airplane electrical systems, a hybrid DFT-PLL algorithm is discussed in [71].

Unlike PLLs, ANF-based synchronization techniques are frequency-adaptive and independent of a voltage-controlled oscillator (VCO). Because it has excellent harmonic rejection, accurate tracking of frequency variations, and robust operation under distorted and unbalanced grid conditions, three-phase ANF structures use either multiple single-phase ANFs or a single three-phase ANF to estimate grid frequency and phase. However, it has drawbacks such as increased design complexity and a bandwidth trade-off between speed and harmonic suppression [72,73]. Certain closed-loop systems use FLLs, such DSOGI-FLL, which prioritize frequency estimates before deriving phase information due to its benefits, such as robust frequency tracking, in comparison to PLLs, showing slower phase convergence but good disturbance rejection [74,75]. The development of sensor less synchronous motor drive for aircraft auxiliary power units (APUs) is discussed in [76]. An improved synchronization and load correction in PV systems by incorporating variable learning rates into the adaptive linear neuron (Adaline) approach has been suggested in [77] where the upgraded Adaline exhibited quicker convergence, higher accuracy, and decreased error during power quality compensation. In order to suppress sinusoidal or periodic interference in signals, a novel idea of adaptive noise cancelling (ANC) was presented that would subsequently serve as the foundation for numerous adaptive filtering and synchronization techniques. The paper discussed a system built an adaptive notch filter that tracked and removed time-varying sinusoidal interferences without the need for explicit frequency measurement by iteratively adjusting filter weights using a least-mean-square (LMS) method [78,79]. For spectrum factorization and cepstral analysis, a two-dimensional recursive filtering framework is created, providing a

computationally effective way to carry out multidimensional filtering operations. The recursive filtering principle of the study established the foundation for effective real-time spectrum and harmonic decomposition algorithms that were later modified for use in PLL-based systems and digital control [80]. Kalman filter-based synchronization techniques (KF-PLL) produced synchronization signals resistant to grid distortions by directly incorporating harmonics, voltage imbalance, noise, and transient disturbances into the filter's state-space formulation, in contrast to classical PLLs [81]-[84]. For grid-connected converters, a model predictive control-based harmonic correction method is suggested in paper [85]. In order to predict future voltage harmonics and modify inverter modulation appropriately, the system used a predictive algorithm [86,87].

2.1.5 Single Phase and Three Phase Phase-Locked-Loop

Paper [88] has offered a fundamental review of phase-locked loop theory emphasising on loop filter design, phase error modelling, and control system dynamics. Synchronous reference frame PLL (SRF-PLL) is the conventional PLL and it is mathematically identical to a first-order adaptive complex band-pass filter. Explicit transfer function derivations were presented providing fresh perspectives on PLL system design and tuning [89]. Quadrature-signal-generation-based and power-based techniques are the two main categories into which a thorough analysis of single-phase PLL structures is divided as discussed in [54]. Further this paper emphasises the benefits of SOGI-FLL and EPLL methods for real-time applications because of their quick dynamic response, simplicity, and immunity to noise [90]. Literature survey of an improved synchronous reference frame PLL (SRF-PLL) for operation under unbalanced voltage situations by adopting twin synchronous reference frames to separate positive- and negative-sequence components is discussed in [38]. The improvement eliminated oscillations caused by negative-sequence voltages while maintaining synchronization precision, offering a strong basis for contemporary SRF-PLL systems [91,92]. A detailed modelling and tuning guide are developed for SRF-PLLs and their advanced forms, such as DSOGI-PLL and Multiple-Complex Coefficient-Filter-Based PLL MCCF-PLL which focused on analytical methods for loop bandwidth and damping optimization, offering a cohesive framework for design

trade-offs [68]. For three-phase synchronization in unbalanced and harmonic-distorted situations, a decoupled double synchronous reference frame PLL (DDSRF-PLL) is presented where two SRF-PLL loops are used that were tuned to positive and negative sequence components, enabling quick transient response and efficient decoupling and DDSRF-PLL outperformed conventional SRF-PLLs in accuracy making it perfect for weak-grid applications [93]. Literature survey also discusses a modified synchronous reference frame PLL (SRF-PLL) for better phase and frequency tracking that incorporates a low-pass notch filter. Under distorted single-phase grid conditions, this adjustment greatly improved harmonic suppression and decreased phase delay. The method in [50] performed better in terms of accuracy and response time than traditional SRF-PLLs. An adaptive SRF-PLL with variable notch filtering for contaminated utility grids is mentioned in literature [94]. By adjusting its rejection frequency in response to harmonic content, the adaptive notch filter ensured precise synchronization even in the face of extreme distortion. The study showed faster dynamic recovery and a notable reduction in THD [95]. A thorough classification of three-phase PLL algorithms, including SRF-PLL, EPLL, DSOGI-PLL, and MAF-PLL variants has been provided in [64] in an extensive survey which examined frequency adaption strategies, stability standards, and structural variations among various designs According to paper [40] the conventional SRF-PLL is still the basis for comparison and benchmarking, although adaptive and hybrid PLLs greatly improve synchronization accuracy under distorted and unbalanced grid situations [96,97]. The effectiveness of several PLL algorithms, such as SRF-PLL, EPLL, DSOGI-PLL, and MAF-PLL, is compared in renewable energy systems [58] with unbalanced voltages and harmonic distortion showing that the optimal trade-off between dynamic speed and noise immunity was provided by EPLL and DSOGI-PLL. It also offered crucial performance standards for choosing suitable PLL architectures in wind and photovoltaic (PV) systems [98]-[108]. A hybrid adaptive PLL is described in [79] that incorporates nonlinear gain control and disturbance compensation circuits. The hybrid technique outperformed conventional SRF-PLL structures in terms of convergence speed and harmonic rejection, as demonstrated by simulation and hardware implementation [98]. An extensive literature survey of PLL-based synchronization techniques used in wind and PV systems is conducted [99]-[108], classifying PLLs by

structure (SRF, EPLL, SOGI, MAF, and hybrid) and evaluating their performance under weak-grid, imbalance, and noise situations. Paper [79] concluded that the most promising future paths for strong renewable integration are hybrid and adaptive PLLs. Paper [109] concluded that among various adaptive PLL structures intended for harmonic mitigation in distributed generation applications, techniques using multi-stage SRF loops and adaptive notch filters provided better accuracy under nonlinear loads and leads to practical design strategies for inverter-based synchronization [110]-[113]. In paper [20] it is found that Kalman filter-based synchronizers have been formed and achieve the optimal trade-off between dynamic response and noise immunity, while conventional SRF-PLLs offer simplicity and low computational cost during comparative study analysis between PLL, FLL, EPLL and KF-PLL [114]. The study in paper [112] also included implementation efficiency and experimental validation settings, establishing it as a fundamental component of contemporary synchronization algorithms intended for fault-tolerant distributed generation control system [115]. To enhance harmonic rejection under grid distortions, a single-phase PLL with an adjustable notch filter is mentioned in [26]. By adaptively adjusting its bandwidth in response to grid conditions, the filter reduced the impact of low-order harmonics while preserving synchronization accuracy. When compared to conventional SRF-PLL techniques, this adaptive notch-PLL hybrid showed better performance, especially in contaminated grids [116,117]. In order to preserve stability in weak and distorted grids, a hybrid adaptive SRF-PLL is suggested in [118]. In order to improve transient behavior and synchronization robustness, the algorithm employed dynamic gain scheduling to modify bandwidth in response to fluctuations in grid impedance. Because of its hybrid design, it achieved good accuracy in low-stiffness grid circumstances by combining adaptive filtering with traditional PLL control [119,120]. The impact of PLL dynamics on the transient response of doubly-fed induction generator (DFIG)-based wind turbines during voltage phase jumps was examined in [101]. Instead of using phase error to compute grid frequency, a digital PLL alternative is suggested in [42] that uses instantaneous angular velocity. These changes improved convergence speed and accuracy under frequency drifts and harmonics when used in single-phase solar inverters [121]. A comprehensive study of the literature on synchronization methods for grid-tied photovoltaic systems is

mentioned in [122]. They various synchronization techniques, highlighting the growing popularity of hybrid approaches that combine DFT, PLL systems, and adaptive filtering for speed and resilience [123]. In order to improve dynamic response and lower steady-state phase error, this review paper [124] introduced a nonlinear gain control framework within a three-phase PLL. The suggested approach produced better harmonic rejection and quicker locking times by adaptively modifying the loop gain according to phase error magnitude. The method served as a standard for advancements in adaptive PLL in power electronics synchronization. The dual SOGI-PLL (DSOGI-PLL) mentioned in [125] has been developed by adding parallel SOGI blocks to the SOGI structure in order to generate orthogonal signals. Improved detection of both positive- and negative-sequence components in single-phase applications was made possible by this approach. Additionally, a comparison of SOGI-PLL and dual-SOGI-PLL (DSOGI-PLL) structures was carried out in [126] and the results showed that DSOGI-PLL achieved better harmonic immunity and a faster transient response at the cost of a slightly higher computational effort. Another improvement in the dual second-order generalized integrator frequency-locked loop (DSOGI-FLL) was mentioned in survey in [127] that reduced the overshoot and enhanced settling time by improving the frequency adaptation and including a damping term in the FLL loop. This technique established DSOGI-FLL as a dependable synchronization tool for distributed energy converters by offering more consistent frequency estimate during voltage fluctuations. To accommodate real-time frequency drifts, an improved SOGI-FLL (eSOGI-FLL) with a configurable FLL gain coefficient was designed in [128]. Again, another literature study highlights the relevance of adaptive filtering in improving PLL stability under grid disturbances and provides an extensive review of three-phase PLL synchronization methods, including dqPLL, DSOGI-PLL, and MRF-PLL techniques [65]. Analytical models for amplitude normalization and harmonic rejection for SOGI-based frequency estimation in single- and three-phase systems has been mentioned in [90] in literature that are used in distributed generation control and microgrid synchronization [129]-[131]. Numerous orthogonal-signal-generator-based PLLs [96] have been assessed under various distortions, including delay-based, derivative, SOGI, and CCF-based methods. The authors in [34] have mentioned that SOGI-PLL was found to be the most balanced in

terms of durability, accuracy, and performance. A modified adaptive notch filter (ANF) with dynamic bandwidth control has been developed in [132] for better transient performance. The suggested design was especially effective for grid frequency monitoring and renewable power synchronization because it offered quicker harmonic rejection and decreased sensitivity to phase noise. Two new adaptive filtering algorithms for active noise control applications like the Filtered-X Least Mean Fourth (FXLMF) and its leaky variant (LFXLMF) are mentioned in [133]. These algorithms extend the conventional Filtered-X Least Mean Square (FXLMS) technique by adding a fourth-order error power criterion to improve convergence under low signal-to-noise ratios (SNR). By adding a leakage term to the adaptation process, the LFXLMF variation addressed overflow and instability issues typical of LMS algorithms and enhanced numerical stability. The enhanced tracking and robustness of the suggested filters over FXLMS and MFXLMS were confirmed by simulation findings, especially in nonlinear acoustic settings [134]. A basis for expanding higher-order adaptive filters in real-time noise and vibration control systems was established by the paper's mathematical formulation and stochastic analysis [135]. For low-frequency distortion correction, high-order PLL topologies incorporating higher-order filters and nonlinear compensation terms has been discussed in [136]. The technique supported weak and unbalanced grid applications by lowering phase latency and enabling reliable operation across a broad frequency range [120]. This work introduced a hybrid PLL combining adaptive low-pass filtering and dynamic loop gain control for enhanced synchronization in heavily distorted grid environments. The structure improved phase tracking accuracy and harmonic immunity without significantly increasing computational complexity, demonstrating the synergy between adaptive filtering and PLL control [137]. Paper [117] presented a modified low-pass filter integrated into the PLL loop to enhance the dynamic response of synchronization systems under harmonic distortion. The design-maintained phase linearity while improving the filter’s cut off dynamics, achieving faster convergence and superior harmonic attenuation. This practical modification was verified through MATLAB/Simulink and experimental results [44]. An adaptive starting technique that improves phase tracking and reduces overshoot for single-phase enhanced PLLs (EPLLs) by utilizing improved initial conditions and dynamic gain

adjustment. to guarantee smooth convergence and get rid of oscillations is developed in [62,138]. An extensive review [99] highlighted the increasing integration of PLL-based control systems in contemporary wind farms by identifying control and synchronization as the most active areas. Additionally, the analysis highlighted machine learning and data-driven approaches as potential areas for future research [108]. In survey it is also found that PLL dynamics influence the electromechanical reactions of DFIG-based wind turbine generators during voltage sags and phase jumps. The investigation found that the PLL bandwidth has a significant impact on system damping and stability margins [115]. The Least Mean Fourth (LMF) adaptive filtering technique was developed as a higher-order variant of the Least Mean Squares (LMS) method. The LMF increased its convergence and robustness in impulsive noise situations by reducing the mean fourth power of the error. The study established the theoretical basis for various adaptive control systems and signal estimating approaches [139]. In order to enhance power quality in grid-connected PV inverters, a fractional-order notch filter (FONF) is implemented in [80]. The filter significantly reduced total harmonic distortion (THD) by correctly extracting fundamental current while attenuating harmonics. Flexible control over phase and frequency responses was made possible by fractional-order tuning [140]-[145]. An introduction to fractional-order calculus and its applications in control engineering was given in literature. Numerical realization techniques, stability criteria, and fractional differentiation and integration operators were all covered in detail. This work contributed to the widespread use of fractional-order controllers (FOCs) as instruments for enhancing response flexibility, capturing memory, damping effects and resilience and A fractional-order model was created to examine power system oscillations and synchronization behaviour [146]-[155]. In [156] an analysis has been on adaptive harmonic rejection filters incorporated into PLL structures to enhance harmonic immunity and dynamic response. In order to maintain stable phase locking, the authors created a self-tuning harmonic compensator that automatically modified its rejection bands based on grid distortion levels. Significant reduction in total harmonic distortion was confirmed by experimental validation as mentioned in [157]-[160]. A more advanced version of PLL is discussed in [92] which is a generalized impedance-based PLL model that was developed using Maclaurin expansion. By capturing nonlinear behaviour in PLL dynamics, the model

improved controller tuning and stability prediction in converter-based systems [161]. Another adaptive PLL was designed that responded to grid distortions and frequency disruptions common to renewable energy systems by dynamically adjusting its loop bandwidth. The system greatly improved transient response and reduced overshoot by implementing an online error-based gain scheduling technique. A grid-connected PV inverter was used to validate the suggested PLL, which showed better synchronization during sharp voltage swings [110]. A dual-stage enhanced PLL (EPLL) that combines secondary harmonic mitigation loops and primary frequency estimation was presented. While lowering phase jitter, the two-stage construction increased tracking accuracy during brief disruptions. Without sacrificing steady-state accuracy, this architecture produced sub-cycle synchronization times [162]-[167]. A PLL with a proportional-integral (PI) controller and an adaptive linear combiner (ALC) was presented as an advanced form in [32]. In comparison to conventional PLLs, this arrangement achieved faster settling times by improving accuracy and tracking under harmonic distortion and phase jump disturbances [64]. By creating a frequency-adaptive improved PLL (FA-EPLL) intended for single-phase systems under frequency fluctuations and harmonic distortion, the EPLL concept is expanded. The suggested technique used adaptive frequency estimation to automatically modify its loop parameters, allowing accurate phase tracking even during grid transients. The FA-EPLL showed better harmonic rejection, less overshoot, and quicker adaptability than static EPLL structures. Its robustness for grid-connected renewable systems and active power filters was confirmed by its performance in non-sinusoidal and unbalanced voltage situations [51]. In order to solve harmonic and frequency offset problems in weak-grid situations, an improved PLL with frequency-adaptive compensation (FAC-PLL) is designed in [73]. A redesigned adaptive gain structure that dynamically adjusted the loop filter bandwidth based on grid conditions was introduced in this paper. Without sacrificing stability, this self-tuning feature produced excellent harmonic suppression and rapid frequency convergence. Its efficacy in low-voltage distributed generation systems was confirmed by experimental installation [6]. The literature presents a novel analytical methodology for assessing the steady-state performance and convergence behavior of the Least-Mean Fourth (LMF) adaptive filtering algorithm. In contrast to conventional stochastic gradient analysis, an

eigenvalue-based determinant technique is used to propose novel adequate criteria for mean-square convergence. The development of generalized necessary conditions for convergence, which expand on previous work by Walach and Widrow (1984), was a significant contribution. Additionally, the study yielded a more generic expression for the extra steady-state error term, demonstrating its dependency on step-size restrictions and higher-order noise moments. In situations when traditional LMS algorithms behave less than optimally, this approach enhanced theoretical knowledge of higher-order adaptive filters and offered design insights for robust adaptive control and noise suppression systems [139].

2.2 Research gap

The following research gaps are highlighted after thorough literature survey.

1. Effective synchronisation techniques are required for control of frequency deviation and effective phase angle detection for best dynamic performance under severe grid
   voltage and harmonic pollution.
2. More focus on integrating artificial intelligence and machine learning techniques with traditional approaches for grid-tied power converters is needed.
3. The synchronization techniques based on grid frequency and voltage detection deserve greater attention under weak grid conditions.
4. Testing of the developed synchronization techniques for grid integration.

2.3 Objective of Research work

1. Design and performance analysis of conventional and advanced PLLs for single and three phase system.
2. Performance study of synchronization techniques with grid-tied renewable energy sources (RES) based distribution systems.

3. Simulation analysis of PLLs for evaluating dynamic performance including stability and transient analysis.

4. Experimental testing of PLLs under grid voltage variations.

2.4 Conclusion

This chapter includes an extensive literature survey that includes the classification of synchronization techniques in electrical power system. The techniques are classified into various types depending on the type of connection like single phase and three phase, presence or absence of the feedback mechanism like open loop and closed loop synchronization techniques. It includes an extensive survey covering the conventional and advanced techniques of PLL and FLL and other forms which are used as synchronization techniques to improve the dynamic performance of grid integrated system. Several papers have also listed the applications of their designed techniques in Photovoltaic (PV) system, doubly fed induction generator (DFIG) wind energy converter system and electric vehicles (EV) based systems.

Chapter: 3

DESIGN AND PERFORMANCE ANALYSIS OF CONVENTIONAL PHASE LOCKED LOOPS

This chapter presents the design and performance analysis of conventional phase locked loops (PLLs) for single phase power distribution system and covers the following PLLs (i) Synchronous Reference Frame (SRF) PLL, (ii) Second Order Generalised Integrator (SOGI) PLL, (iii) Least Mean Square (LMS) PLL. It also discusses the three phase PLLS viz (i) Synchronous Reference Frame (SRF) PLL (ii) Least Mean Fourth (LMF) PLL. The chapter focuses on the key design components, operating principle, and dynamic behaviour of these PLLs. It also discusses the mathematical modelling of the PLLs for developing their transfer function derivations and stability analysis. The simulation and experimental results are presented to validate the theoretical analysis under abnormal grid conditions. The grid disturbances considered are taken as (i) 30% voltage sag, (ii) 35% voltage swell, (iii) polluted grid voltage, (iv) 30o phase shift, (v) +5 Hz frequency change and (vi) 20% dc offset in all the chapters of the Thesis.

3.1 Design and Performance Analysis of Single Phase Conventional PLL

The design of single-phase conventional phase locked loops (PLLs) like (i) Synchronous Reference Frame (SRF) PLL, (ii) Second Order Generalised Integrator (SOGI) PLL, (iii) Least Mean Square (LMS) PLL has been presented to analyse the dynamic performance when the PLLs are exposed to grid abnormalities. Every PLL system considered consists mainly of three fundamental components viz. (i) Phase Detector (PD), (ii) Loop Filter (PI controller), (iii) Voltage-Controlled Oscillator (VCO) and functions as a negative feedback system. A grid voltage supply of v_s (V) with a nominal angular frequency, ω_{nf} is fed as an input. V_A is the amplitude of the input voltage, and is calculated as $V_A = \sqrt{2} * V_{rms}$. PD gives relation between input and output phases of the voltage signal. K_{PD} denotes the gain of PD. It is equal to amplitude / (2*pi rad), so its unit is volt per rad. PD gives a nonlinear response but is

linear in a range within 1cycle or 2 cycles. The loop filter (LP) normally taken in all the models of PLLs is a Proportional Plus Integral (PI) controller. The gains associated with PI controller are K_p and K_I and these are proportional and integral gains respectively. The output of the LF, (ω_{cf}), is added to the nominal angular frequency (ω_{nf}) and sent to the voltage-controlled oscillator (VCO) as (ω_{est}). The output of the VCO is the estimated frequency denoted by θ_{est}. The PD output can be considered as a voltage proportional to the phase error and its output signal contains both DC and high frequency components**.** The loop filter removes the high frequency component leaving the lower frequency component unchanged. When the frequency of the input signal is equal to the frequency of the VCO then we say that the loop is locked, i.e. $\theta_{in} = \theta_{est}$ where θ_{in} is the phase angle of the input signal.

3.1.1 Synchronous Reference Frame (SRF) PLL

The structural block diagram of a single phase SRF PLL is shown in Fig. 3.1. The supply voltage, ' v_s' is transformed into into two quadrature voltage signals, i.e. α and β voltage components. The α component (v_α) is same as original supply voltage (v_s) while the β component (v_β) is created by introducing a phase shift of 90° which is a quarter-cycle, $\frac{T}{4}$, time delay as T is the time period of the supply voltage.

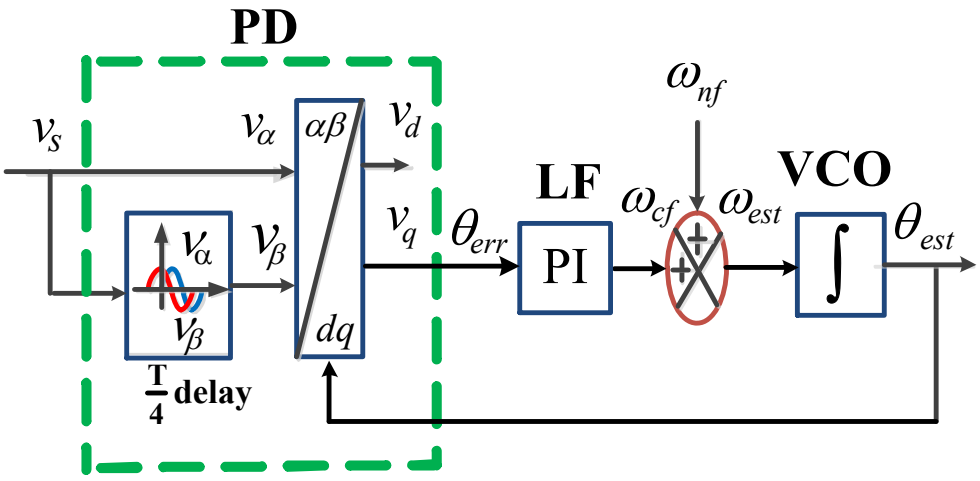


Fig. 3.1 Structural block diagram of single phase SRF PLL

The supply voltage,v_s and its orthogonal signals in time domain, can be expressed as

$$v_s(t) = v_\alpha(t) = V_A \sin(\omega t + \emptyset) \tag{3.1}$$

$$v_\beta(t) = v_\alpha\left(t - \frac{T}{4}\right) = V_A \sin\left(\omega t + \emptyset - \frac{\omega T}{4}\right) \tag{3.2}$$

$$v_\beta(t) = V_A \sin\left(\theta_{in} - \frac{\omega T}{4}\right) = -V_A \cos\left(\theta_{in} - \omega_{cf}\frac{T}{4}\right) \tag{3.3}$$

where V_A is the amplitude of the supply voltage, θ_{in} is phase angle of supply voltage and ω_{cf} is the lower angular frequency component obtained as output of the loop filter (LF). The stationary frame voltage components, v_α and v_β are transformed into rotating frame of voltage components, v_d and v_q, using Park's transformation The converted αβ-voltage components are transformed into dq-voltages by the equation given below

$$\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \begin{bmatrix} \sin\theta_{est} & -\cos\theta_{est} \\ \cos\theta_{est} & \sin\theta_{est} \end{bmatrix} \begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} \tag{3.4}$$

$$v_d(t) = v_\alpha(t)\sin\theta_{est} - v_\beta(t)\cos\theta_{est} \tag{3.5}$$

$$v_q(t) = v_\alpha(t)\cos\theta_{est} + v_\beta(t)\sin\theta_{est} \tag{3.6}$$

The phase error measured by PD is expressed as

$$\theta_{err} = \theta_{in} - \theta_{est} \tag{3.7}$$

where θ_{err} is the phase error of input and output voltage signals, θ_{in} is the phase angle input signal and θ_{est} is the output phase obtained from VCO.

As shown in Fig.3.1, the phase error is passed through a PI controller which is used as a loop filter (LF) and its output is known as angular frequency error (ω_{cf}). The angular frequency error is added with the nominal angular frequency (ω_{nf}) providing an estimated angular frequency (ω_{est}). The estimated frequency is fed to VCO which gives a phase angle (θ_{est}) which can be expressed as

$$\theta_{est} = tan^{-1}\frac{\bar{v}_q}{\bar{v}_d} \tag{3.8}$$

The error voltage from PD is processed by LF and is responsible for the dynamic response of the PLL. With proper tuning of the PI controller, the d-axis aligns with the

virtual input voltage, while the quadrature component (q-axis) carries the phase error signal. As a result, in steady state, the q-axis voltage $v_q = 0$. The transfer function of LF in Laplace transformation is expressed as

$$T_{LF}(s) = \frac{K_p s + K_i}{s} \tag{3.9}$$

where K_p and K_i are the gains of the PI controller.

The transfer function of VCO having a gain of K_{VCO} in Laplace transformation can be expressed as

$$T_{VCO}(s) = \frac{K_{VCO}}{s} \tag{3.10}$$

The open loop transfer function of the single phase SRF can be expressed as

$$\mathrm{T_{1-\emptyset SRF}(s)} = \frac{\theta_{est}(s)}{\theta_{err}(s)} = \mathrm{T_{PD}(s) * T_{LF}(s) * T_{VCO}(s)} \tag{3.11}$$

$$\mathrm{T_{1-\emptyset SRF}(s)} = \mathrm{K_{PD}} * \frac{\mathrm{K_p s + K_i}}{\mathrm{s}} * \frac{\mathrm{K_{VCO}}}{\mathrm{s}} = \frac{\mathrm{K_p s + K_i}}{\mathrm{s^2}} \tag{3.12}$$

The closed loop transfer function of the SRF-PLL is

$$\mathrm{H_{1-\varphi SRF}(s)} = \frac{\mathrm{T_{1-\varphi SRF}(s)}}{1+\mathrm{T_{1-\varphi SRF}(s)}} = \frac{\mathrm{K_p s + K_i}}{\mathrm{s^2 + K_p s + K_i}} \tag{3.13}$$

3.1.2 Second Order Generalised Integrator (SOGI) PLL

The structural block diagram of the single phase second order generalised integrator (SOGI) PLL is shown in Fig. 3.2. It consists of a SOGI structure which is a second order filter used in phase detector, loop filter (LF) and a VCO. The grid supply voltage, v_s with nominal angular frequency as ω_{nf} is applied to SOGI and it creates the in-phase and quadrature signals of the supply grid voltage (v_α and v_β). These orthogonal voltages signals, v_α and v_β in the stationary reference frame (αβ), are converted into rotatory reference frame (d-q-o) voltages, v_d and v_q by Park's transformation. The d-component of voltage, v_d has the details of amplitude and q-component v_q gives details of phase error (θ_{err}) of supply voltage. This phase error,

θ_{err}, signal is fed to PI controller to regulate the control angular frequency ω_{cf}. The resultant angular frequency ω_{cf} is added with the nominal grid angular frequency ω_{nf}

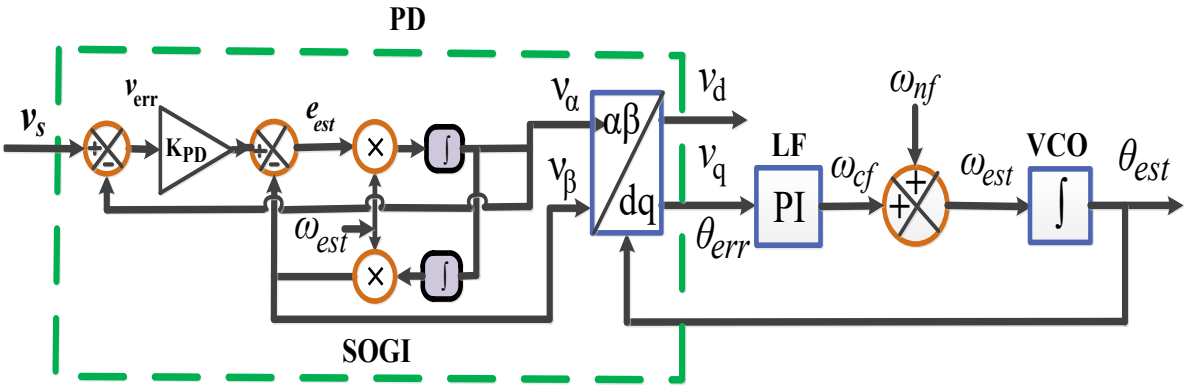


Fig. 3.2 Structural block diagram of single phase SOGI PLL

and produces the estimated angular frequency ω_{est}. The estimated frequency is integrated through VCO to obtain the estimated phase angle (θ_{est}). Under steady state condition when v_q is controlled to zero through PI controller and VCO, the estimated phase angle θ_{est} is equal to input phase angle. Hence the grid supply voltage of the single phase SOGI is also equal to its direct or alpha component and it can be expressed as

$$v_s(t) = v_\alpha(t) = V_A \sin(\omega t + \emptyset) \tag{3.14}$$

The quadrature component of the grid voltage signal can be expressed as

$$v_\beta(t) = v_\alpha\left(t - \frac{T}{4}\right) = V_A \sin\left(\omega t + \emptyset - \frac{\omega T}{4}\right) \tag{3.15}$$

$$v_\beta(t) = V_A \sin\left(\theta_{in} - \frac{\omega T}{4}\right) = -V_A \cos\left(\theta_{in} - \omega_{cf}\frac{T}{4}\right) \tag{3.16}$$

The error signal v_{err} is expressed as

$$v_{err}(t) = v_s(t) - v_\alpha(t) \tag{3.17}$$

$$v_\beta(t) = \omega_{est} \int v_\alpha(t)\, dt \tag{3.18}$$

The Laplace transform of Eq. (3.18) is expressed as

$$v_\beta(s) = \frac{\omega_{est} v_\alpha(s)}{s} \tag{3.19}$$

$$v_\alpha(t) = \int e_{est}(t)\omega_{est} dt \tag{3.20}$$

The estimated error is given as

$$e_{est}(t) = K_{PD} v_{err}(t) - v_\beta(t) \tag{3.21}$$

Substituting the value of '$e_{est}(t)$' from Eq. (3.21) in Eq. (3.20), we obtain

$$v_\alpha(t) = \int \omega_{est} K_{PD} v_{err}(t) dt - \int \omega_{est} v_\beta(t)) dt \tag{3.22}$$

The Laplace transform of Eq. (3.22) is expressed as

$$v_\alpha(s) = \omega_{est} K_{PD} \left[\frac{v_s(s)}{s} - \frac{v_\alpha(s)}{s}\right] - \omega_{est} \frac{v_\beta(s)}{s} \tag{3.23}$$

$$v_\alpha(s) = \omega_{est} K_{PD} \left[\frac{v_s(s)}{s} - \frac{v_\alpha(s)}{s}\right] - \omega_{est}^2 \frac{v_\alpha(s)}{s^2} \tag{3.24}$$

By rearranging the above Eq. (3.24), the closed loop transfer function of in-phase signal with damping factor '$K_{PD} = \sqrt{2}$' can be expressed as

$$T_D(s) = \frac{v_\alpha(s)}{v_s(s)} = \frac{K_{PD}\omega_{est} s}{s^2 + K_{PD}\omega_{est} s + \omega_{est}^2} \tag{3.25}$$

The closed loop transfer function of quadrature component of phase signal can be expressed as

$$T_Q(s) = \frac{v_\beta(s)}{v_s(s)} = \frac{K_{PD}\omega_{est}^2}{s^2 + K_{PD}\omega_{est} s + \omega_{est}^2} \tag{3.26}$$

Thus, the open loop transfer function of linearized SOGI PLL can be expressed as

$$T_{1-\emptyset SOGI}(s) = \frac{\theta_{est}(s)}{\theta_{err}(s)} = \frac{K_p s + K_i}{s^2} \tag{3.27}$$

Transfer function of error signal $v_{err}(s)$ w.r.t supply voltage $v_s(s)$ is expressed as

$$T_E(s) = \frac{v_{err}(s)}{v_s(s)} = \frac{s^2 + \omega_{est}^2}{s^2 + K_{PD}\omega_{est} s + \omega_{est}^2} \tag{3.28}$$

3.1.3 Least Mean Square (LMS) PLL

Least Mean-Squares (LMS) is a very popular stochastic gradient based adaptive filter showing a low to medium computational complexity. It is used to find the coefficients of the filter to minimise the square error. The derivation of the conventional LMS algorithm is done using the Steepest Descent Approach. The diagram of weight updating algorithm of LMS filter and the block diagram of the structure of single phase LMS PLL are shown in Fig. 3.3 and Fig. 3.4. The reference input signal is denoted by x*(k) where 'k' denotes the number of iterations, $v_s(k)$ is the input signal and the estimated output signal is denoted by v(k). It is the output obtained from the LMS filter. The error signal, $e_{ser}(k)$ is another output signal obtained by taking the difference between the output and input signals. The reactive voltage component from LMS is fed to the PI controller of the LMS PLL and the output of VCO is the estimated phase angle/frequency. The steady state error signal is expressed as

$$e_{ser}(k) = v_s(k) - v(k) \tag{3.29}$$

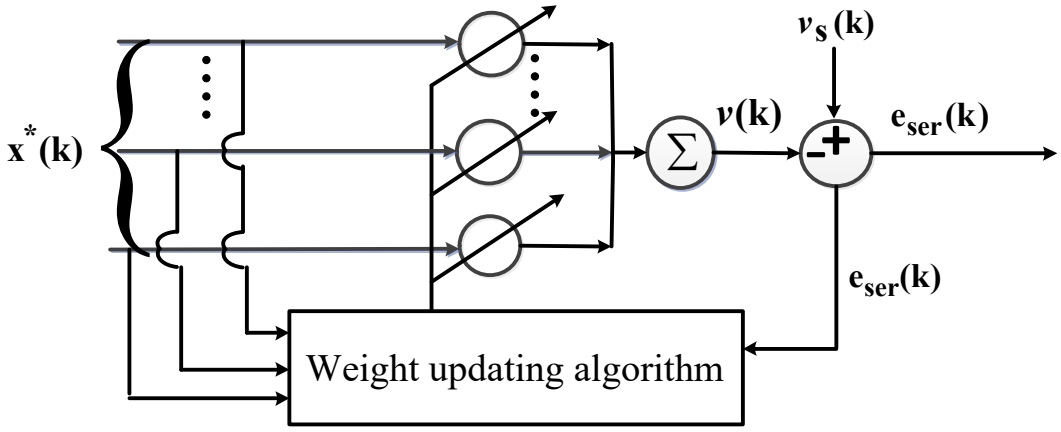


Fig. 3.3 Weight updating diagram of the algorithm of LMS filter

The cost function ($\xi(k)$), is defined by the error signal and it is expressed as

$$\xi(k) = E[e_{ser}^2(k)] = E[(v_s(k) - v(k))^2] \tag{3.30}$$

The input coefficient matrix for N samples is represented as

$$\overrightarrow{x^*}(k) = [x^*(k)x^*(k-1)x^*(k-2)\ x^*(k-3) \ldots\ldots\ldots x^*(k-N+1)]^T$$

$$= [sin\theta_{est}\ cos\theta_{est}\quad \sin(N-1)\theta_{est}\quad \cos(N-1)\theta_{est}\quad sinN\theta_{est}\quad cosN\theta_{est}]^T \tag{3.31}$$

The phase angle ' θ_{est}' is obtained as output from VCO of LMS PLL after modulating it. The weight coefficient in matrix form at time 'k' is expressed as

$$\overrightarrow{W^{T}}(k) = [W_0(k)W_1(k) \dots \dots \dots \dots \dots W_{N-1}(k)] \quad (3.32)$$

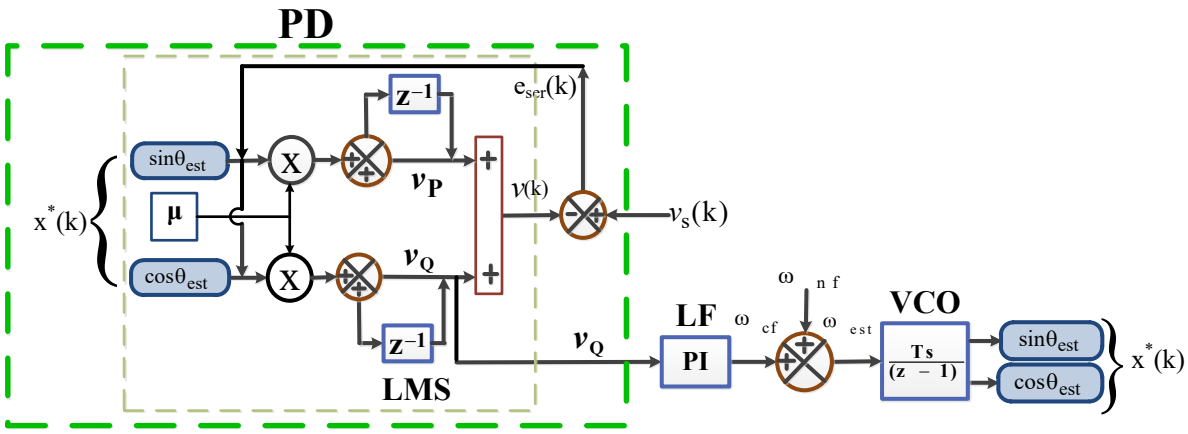


Fig. 3.4 Block diagram of the structure of single phase Least Mean Square (LMS) PLL

The estimated output of the LMS in the matrix form is expressed as

$$v(k) = W^{T}(k)\overrightarrow{X^*}(k) \quad (3.33)$$

$$v(k) = \sum_{i=0}^{N-1} V_{Ai}\sin(i\omega kT_s + \varphi_i) \quad (3.34)$$

$$= \sum_{i=0}^{N-1}(V_{Ai}\cos\varphi_i \sin i\omega kT_s + V_{Ai}\sin\varphi_i \cos i\omega kT_s) \quad (3.35)$$

$$= \sum_{i=0}^{N-1}(v_{Pi}\sin i\omega kT_s + v_{Qi}\cos i\omega kT_s) \quad (3.36)$$

Here in the above equations ' V_{Ai}' is the amplitude of the i^{th} voltage signal with $(\omega kT_s + \varphi_i)$ as its phase angle. The active and reactive voltage components can be written as $v_{Pi} = (V_{Ai}\cos\varphi_i)$ and $v_{Qi} = (V_{Ai}\sin\varphi_i)$ respectively. The amplitude of the voltage signal considering dq-axis component is expressed as

$$V_{PQA}(k) = \sqrt{(v_{Pi})^2 + (v_{Qi})^2} \quad (3.37)$$

Weight updating of the LMS can be modelled using the Steepest Descent Approach as

$$W(k+1) = W(k) + \mu e_{ser}(k)X^*(k) \quad (3.38)$$

The active and reactive component of the voltage while updating the weight from equation (3.38) can be expressed in equations (3.39) and (3.40)

$$W_P(k+1) = W_P(k) + \mu e_{ser}(k) \sin\theta_{est} \tag{3.39}$$

$$W_Q(k+1) = W_Q(k) + \mu e_{ser}(k) \cos\theta_{est} \tag{3.40}$$

The learning rate or the convergence factor of an LMS filter is represented by ' μ' and ' T_s' is the sampling time considered for k=1,2,3, 4,……N samples. The reactive component of the voltage is passed to the proportional plus integrator (PI) controller which is used as loop filter (LF). The output from PI is the controlled voltage given by ω_{cf}. The estimated phase angle, θ_{est} , and estimated frequency ω_{est} is obtained by adding fundamental frequency, ω_{nf} to ω_{cf}. After modulating the outcome from voltage-controlled oscilloscope (VCO) the estimated phase angle is obtained. The reference input signals are obtained by multiplying it with sine and cosine functions. The estimated frequency and phase angle with T_s as the sampling time can be expressed as

$$\omega_{est} = \omega_{cf} + \omega_{nf} \tag{3.41}$$

$$\theta_{est} = \frac{T_s}{z-1}\omega_{est} \tag{3.42}$$

The open loop transfer function of single LMS in z transform with T_s as the sampling time is expressed as [69]

$$T_{LMS}(z) = \frac{output}{error} \tag{3.43}$$

$$= \frac{\mu(z\cos\omega_{est}T_s - 1)}{z^2 - 2z\cos\omega_{est}T_s + 1} \tag{3.44}$$

The closed loop transfer function of LMS with T_s as the sampling time is expressed as [69]

$$T_{clLMS}(z) = \frac{output}{input} \tag{3.45}$$

$$= \frac{T_{LMS}(z)}{1 + T_{LMS}(z)} \tag{3.46}$$

$$= \frac{\mu(z\cos\omega_{est}T_s - 1)}{z^2 - 2z\cos\omega_{est}T_s + 1} * \frac{1}{1 + [\mu(z\cos\omega_{est}T_s - 1)/z^2 - 2z\cos\omega_{est}T_s + 1]} \tag{3.47}$$

$$= \frac{[\mu(z\cos\omega_{est}T_s - 1)]}{[z^2 - 2z\cos\omega_{est}T_s + 1] + [\mu(z\cos\omega_{est}T_s - 1)]} \tag{3.48}$$

$$= \frac{[\mu(z\cos\omega_{est}T_s - 1)]}{z^2 - 2(1-\mu/2)\, z\cos(\omega_{est}T_s) + (1-\mu)} \quad (3.49)$$

3.2 Design and Performance Analysis of Three Phase Conventional PLLs

This section of the chapter presents the design and performance analysis of three-phase conventional phase locked loops (PLLs). For a balanced grid, the three phase PLLs generally offers superior noise rejection than single phase PLLs. The three phase grid supply voltages use both the Clarke and the Park transformations for converting the three phase supply voltages (v_{abc}) to dq-rotating reference frame where the system locked to its nominal frequency when $v_q = 0$. It discusses three phase SRF-PLL and another three phase PLL called Least Mean Fourth, (LMF) PLL. They are tested under grid abnormalities like 30% voltage sag, 35% voltage swell, polluted, 30° phase shift, +5 Hz frequency change and 20% dc offset. The performance analysis has been done through the simulation results and it is validated by hardware results.

3.2.1 Three-phase SRF- PLL

The schematic diagram of a three phase SRF PLL is shown in Fig. 3.5 and it has the three sections of conventional PLL i.e. (i) phase detector (PD), (ii) loop filter (LF) and (ii) voltage-controlled oscilloscope (VCO) and is a negative feedback system. The three-phase voltages (v_a, v_b, v_c) having an amplitude of ' V_A' (peak value) representing the grid voltages are fed to the PD section. These voltages at the stationary reference frame are converted into another orthogonal stationary reference frame αβ (v_α, v_β) by Clarke transformation. The αβ -dq voltage transformation (stationary to rotating frame) is performed by Park transformation. The input PCC voltage has a nominal angular frequency ' $\omega_{nf} = 2\pi f$', phase angle, ' θ_{in}' with frequency as f=50 Hz. The three phase input grid voltages of SRF PLL, (v_a, v_b, v_c), are symmetrical and are 120° apart can be expressed as

$$v_a = \mathrm{V}_A sin\omega_{nf}t = \mathrm{V}_A sin\theta_{in} \quad (3.50)$$

$$v_b = \mathrm{V}_A sin(\omega_{nf}t - \tfrac{2\pi}{3}) = \mathrm{V}_A sin(\theta_{in} - \tfrac{2\pi}{3}) \quad (3.51)$$

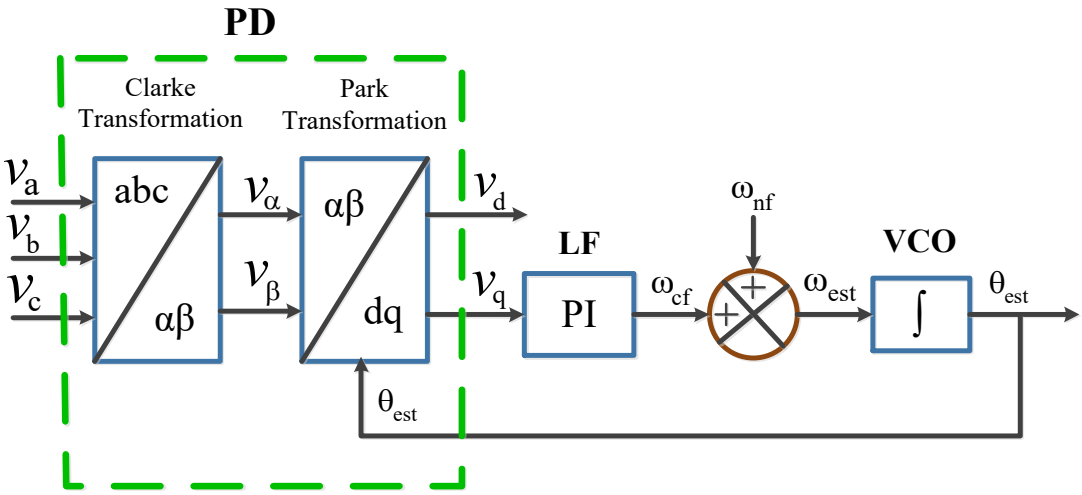


Fig. 3.5 The schematic diagram of a three phase SRF PLL

$$v_c = V_A sin(\omega_{nf} t + \frac{2\pi}{3}) = V_A sin(\theta_{in} + \frac{2\pi}{3}) \tag{3.52}$$

where V_A is the peak voltage and is expressed as

$$V_A = \sqrt{2} V_{rms} = \frac{\sqrt{2(v_a^2 + v_b^2 + v_c^2)}}{3} \tag{3.53}$$

The Clarke transformation equations in the matrix form can be written as

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.54}$$

Hence, the two orthogonal voltages (v_α, v_β) obtained from three phase grid voltage by Clarke transformation can be expressed as

$$v_\alpha = \frac{3}{2} sin\ \omega_{nf} t = \frac{3}{2} sin\theta_{\ in} \tag{3.55}$$

$$v_\beta = \frac{3}{2} \cos \omega_{nf} t = \frac{3}{2} cos\theta_{\ in} \tag{3.56}$$

The Park transformation (αβ to dq) can be written as

$$\begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} = \begin{bmatrix} \cos\theta_{est} & \sin\theta_{est} & 0 \\ -\sin\theta_{est} & \cos\theta_{est} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} \tag{3.57}$$

The instantaneous voltages, 'v_q' and 'v_d' from dq-reference frame as an output of PD can be expressed as

$$v_d = \frac{3}{2}\sin(\theta_{in} - \theta_{est}) = \frac{3}{2}\sin\theta_{err} \tag{3.58}$$

$$v_q = \frac{3}{2}\cos(\theta_{in} - \theta_{est}) = \frac{3}{2}\cos\theta_{err} \tag{3.59}$$

where the input phase angle is denoted as θ_{in}, ' θ_{est}' is the estimated angular frequency, ' θ_{err}' is the phase angle error and it is the difference of phases θ_{in} and θ_{est} obtained as an output from PD. It is expressed as

$$\theta_{err} = \theta_{in} - \theta_{est} \tag{3.60}$$

The estimated angular frequency, 'ω_{est}' is the output from PI controller and obtained by combining nominal frequency, 'ω_{nf}' and control angular frequency, 'ω_{cf}' from PI controller (which is the LF). It is expressed as

$$\omega_{est} = \omega_{nf} + \omega_{nf} \tag{3.61}$$

The estimated phase angle, ' θ_{est}' is obtained by integrating and modulating the estimated frequency ω_{est}' from VCO as its output. Thus, under the steady balanced condition, the estimated phase angle is equal to the inherent phase angle of the grid voltage ($\theta_{est} = \theta_{in}$), $v_q = 0$ and v_d is equal to magnitude of the input grid voltage. The open loop transfer function of the 3-phase SRF PLL can be expressed as

$$T_{3-\varphi SRF}(s) = \frac{output}{error} = \frac{\theta_{est}(s)}{\theta_{in}(s)} \tag{3.62}$$

$$T_{3-\varphi SRF}(s) = \frac{V_A(K_p s + K_i)}{s^2} \tag{3.63}$$

The closed loop transfer function of the 3-phase SRF PLL is expressed as

$$T_{cl3-\varphi SRF}(s) = \frac{output}{input} = \frac{T_{3-\varphi SRF}(s)}{1 + T_{3-\varphi SRF}(s)} \tag{3.64}$$

$$T_{cl3-\varphi SRF}(s) = \frac{V_A(k_p s + k_i)}{s^2 + V_A k_p s + k_i} \tag{3.65}$$

3.2.2 Least Mean Fourth (LMF) PLL

The least mean fourth (LMF) PLL algorithm is based on steepest gradient structure and was first introduced by E. Walach and B. Widrow in 1984 as part of a family of adaptive algorithms that minimize higher-order error criteria [139]. The LMF minimizes the error in mean fourth form and gives better performance in the uniform non-Gaussian noise environment. Fig. 3.6 shows the block diagram of LMF algorithm where the reference input signal is denoted by u(k) and 'k' is the number of iterations, $v_s(k)$ is the input signal and the estimated output signal is denoted by v (k). It is the output obtained from the LMF filter. The error signal, $e_{ser}(k)$ is another output signal obtained by taking the difference between the output and input signals. Fig. 3.7 shows the schematic block diagram of 3-Φ LMF PLL.

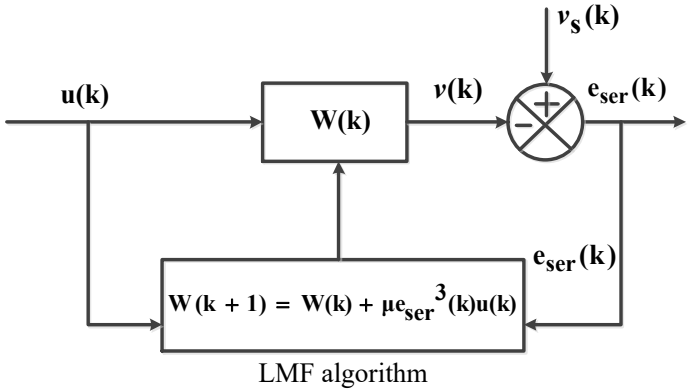


Fig.3.6 Block diagram of LMF algorithm

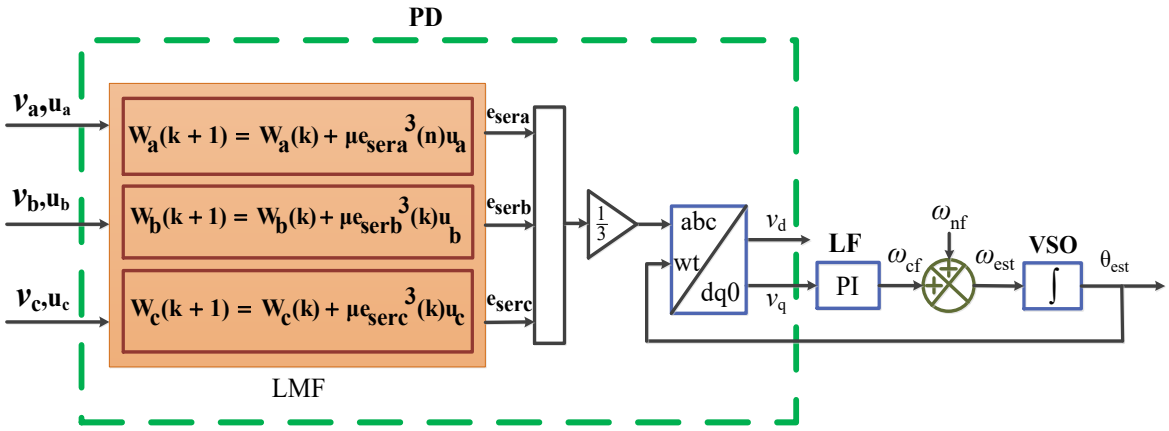


Fig. 3.7 The schematic block diagram of 3-Φ LMF PLL

The three phase voltages from the line voltages at the point of common coupling fed to the phase detector (PD) of the LMF PLL can be expressed as

Phase A voltage, $v_a = \frac{2v_{ab}+v_{bc}}{3}$ (3.66)

Phase B voltage, $v_b = \frac{-v_{ab}+v_{bc}}{3}$ (3.67)

Phase C voltage, $v_c = \frac{-v_{ab}-2v_{bc}}{3}$ (3.68)

where v_{ab} and v_{bc} are the line voltages

The amplitude, V_m of the terminal voltage, V_{ter} can be estimated as

$$V_m = \sqrt{\frac{2}{3}(v_a^2 + v_b^2 + v_c^2)} \quad (3.69)$$

The unit templates which are in-phase with phase voltages are expressed as

$$u_{da} = \frac{v_a}{V_m},\ u_{db} = \frac{v_b}{V_m},\ u_{db} = \frac{v_b}{V_m} \quad (3.70)$$

The orthogonal unit templates are expressed as

$$u_{qa} = \frac{u_{dc}-u_{db}}{\sqrt{3}},\ u_{qb} = \frac{\sqrt{3u_{da}}}{2} + \frac{u_{db}+u_{dc}}{2\sqrt{3}},\quad u_{qc} = \frac{-\sqrt{3}u_{da}}{2} + \frac{u_{dc}-u_{db}}{2\sqrt{3}} \quad (3.71)$$

The error voltage, $e_{ser}(k)$ at the instant k is given as

$$e_{ser}(k) = v_s(k) - v(k) \quad (3.72)$$

The cost function ($\xi(k)$) of LMF scheme is defined as

$$\xi(k) = E[e_{ser}^4(k)] \quad (3.73)$$

$$= E[(v_s(k) - v(k))^4] \quad (3.74)$$

The input coefficient matrix for N number of samples at instant k is expressed as

$$\vec{u}(k) = [u(k),\ u(k-1), u(k-2), \ldots\ldots\ldots u(k-N+1)]^T$$

$$= [\sin\theta_{est}\ \ \cos\theta_{est}\ \ldots\ldots \sin(N-1)\theta_{est}\ \ \cos(N-1)\theta_{est}\ \sin\ N\theta_{est}\ \cos N\theta_{est}]^T \quad (3.75)$$

where phase angle ' θ_{est}' is outputs from VCO of LMF PLL after modulating it

The weight adaptation for 'k' samples is expressed as

$$W^T(k) = [W_0(k), W_1(k), \dots\dots\dots W_{N-1}(k)] \tag{3.76}$$

Weight updating equation is expressed as [139]

$$W\ (k+1) = W(k) + \mu e_{ser}^3(k)u(k) \tag{3.77}$$

The weight updating coefficient rule can be expressed as

$$\vec{W}\ (k+1) = \vec{W}(k) + \mu e_{ser}^3(k)u(k) \tag{3.78}$$

The active component of the weight updation for phase 'a' can be

$$W_{da}(k+1) = W_{da}(k) + \mu_d u_{da}(k) e_{serda}^3(k) \tag{3.79}$$

where μ_d is the adaptive constant and $e_{serda}(k)$ is adaptive active component error of phase 'a' and is derived and written as

$$e_{serda}(k) = V_{tera}(k) - u_{da}(k) W_{da}(k) \tag{3.80}$$

Similarly, the active components of weights for phase B and C can be obtained. The reactive component of weight and error of phase A can be estimated as

$$W_{qa}(k+1) = W_{qa}(k) + \mu_q u_{qa}(k) e_{serqa}^3(k) \tag{3.81}$$

$$e_{serqa}(k) = V_{tera}(k) - u_{qa}(k) W_{qa}(k) \tag{3.82}$$

The mean value of the reactive component of the reactive voltages of the three phases can be expressed as

$$W_{Mq} = \frac{W_{qa} + W_{qb} + W_{qc}}{3} \tag{3.83}$$

This mean reactive component of voltage is passed through PI controller which is a loop filter of PLL. The supply phase 'a' voltage is taken as $v_a\,(k) = V_m \sin(\omega k T_s) + \varphi)$ where V_m is the amplitude of the voltage signal, ω is the angular frequency, $\theta = ((\omega k T_s) + \varphi)$ is the phase angle with noise. $\omega = 2\pi f = 100\pi$ rad/sec. Considering phase, 'a', the reactive supply voltage signal can be expressed as

$$u_{qa}(k) = \cos\ (\theta k) \tag{3.84}$$

The estimated output voltage is expressed as

$$v_a(k) = u_{qa}(k)\, W_{qa}(k) \tag{3.85}$$

Linearisation of LMF PLL with γ_e^2 taken as the linearisation constant is done for transfer function calculation. Hence $E[e^3(k)] \approx 3\gamma_e^2\ e(k)$.

Now new weight update becomes of phase 'a'

$$W_{qa}(k+1) \approx W_{qa}(k) + 3\mu_q \sigma_e^2 u_{qa}(k) e_{serqa}^3(k) \tag{3.86}$$

Taking $\mu_{fl} = 3\mu_q\sigma_e^2$ as the effective linear step size of LMF PLL.

The open loop transfer function of LMF PLL in z domain after considering equation (3.86) of LMS can be expressed as

$$T_{LMF}\ (z) = \mu_{fl}(z\cos(\omega_{nf}T_s) - 1 \tag{3.87}$$

Similarly, the closed-loop transfer function of LMF PLL is estimated as []

$$T_{clLMF}(z) = \frac{T_{LMF}\ (z)}{1+T_{LMF}\ (z)} \tag{3.88}$$

$$= \frac{\mu_{fl}(z\cos(\omega_{nf}T_s)-1}{z^2-2\left(1-\frac{\mu_{fl}}{2}\right)z\cos(\omega_{nf}T_s)+(1-\mu_{fl})} \tag{3.89}$$

3.3 Stability Analysis of Conventional PLLs

In the event of grid disruptions, steady-state (static) stability analysis of PLL guarantees dependable frequency, phase locking and capacity in stabilising. Inadequate tuning can lead to instability and asynchronization. An increased bandwidth of PLL decreases stability margins but enhances its dynamic response. Thus, stability analysis helps in choosing parameters to obtain the efficient relationship between robustness and speed which is done mostly by analysing the roots of the PLL's characteristic equation. The stability, marginal stability, and instability of the system are predicted by the position of the poles and zeros. Nyquist diagrams, Routh-Hurwitz, bode plots, and pole-zero analysis are common techniques applied for finding the stability.

In this section of the chapter the stability analysis of the PLLs is performed by the Nyquist diagram, calculation of phase margin with its crossover frequency. The Nyquist plot is a variant of the polar plots which is used for determining the stability of the closed loop control system by varying the frequency, 'ω' from 180^o to -180^o. It is the frequency response obtained from the open loop transfer function. The Nyquist stability criterion for a linear system in 's' plane is generally expressed by the following equation as

$$N=Z-P \tag{3.90}$$

where 'N' is the number of encirclements of critical point (-1, 0j), 'Z' is the number of poles of the unstable closed loop and 'P' is the number of poles of the unstable open loop transfer functions. It states that if a system is without any unstable open-loop poles, the closed-loop system must be stable if the point −1 on the complex plane is not surrounded by the Nyquist plot (NG(jω) as ω_{est} ranges from −∞ to +∞).

The stability of the system can be narrated with the following relationships

- The control scheme is stable if the phase margin, PM is positive and the gain margin

  GM is greater than one with the phase cross over frequency 'ω_{pc}' is greater than gain

  cross over frequency ' ω_{gc}'.
- The control scheme is marginally stable if the phase margin, PM = 0^o and the gain margin, GM =1 with $\omega_{pc} = \omega_{gc}$.
- The control scheme is unstable if the phase margin PM is absolutely negative and $\omega_{pc} < \omega_{gc}$.

3.3.1 Synchronous Reference Frame (SRF) PLL

The stability analysis of SRF PLL is done from the open loop transfer function obtained in equation (3.12) through the Nyquist diagram is shown in Fig. 3.8. The open loop curve in the anticlockwise direction does not encircle the critical points (-1,0j) in the s-plane. Hence the closed loop system of SRF PLL is stable. The phase margin (PM) is 45.1^o with crossover frequency ω_{pc} of 11rad/s.

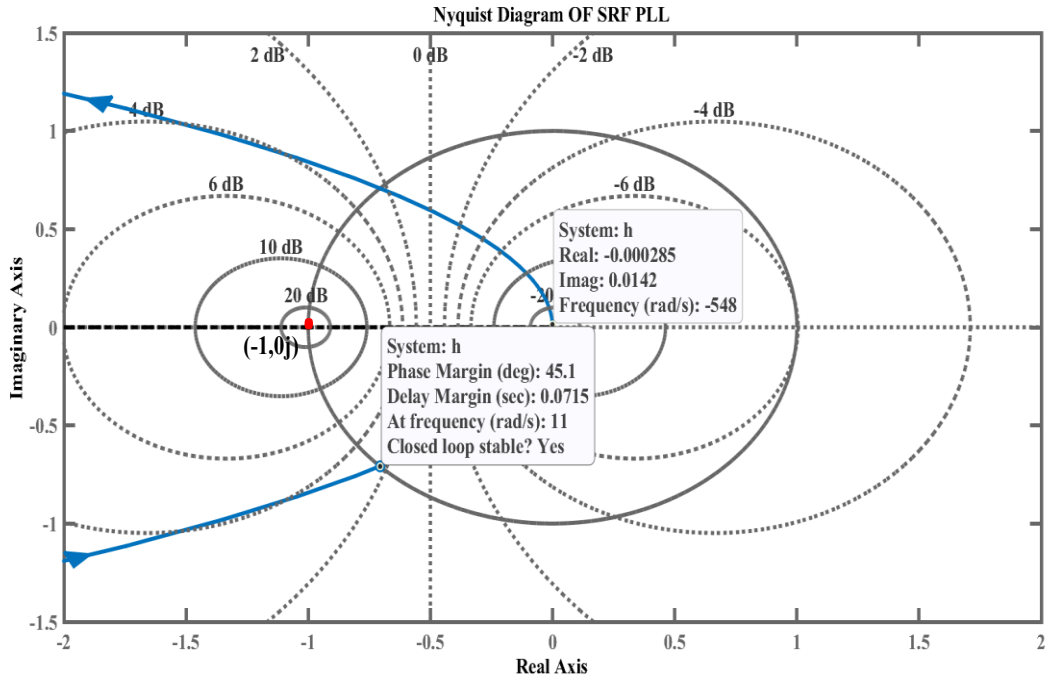


Fig. 3.8 Nyquist diagram of SRF PLL

3.3.2 Second Order Generalized Integral (SOGI) PLL

The stability analysis of SOGI PLL is performed from the open loop transfer function obtained in equation (3.27) with the Nyquist diagram as shown in Fig. 3.9. The diagram shows that the critical point (-1,0j) is not encircled by the Nyquist curve

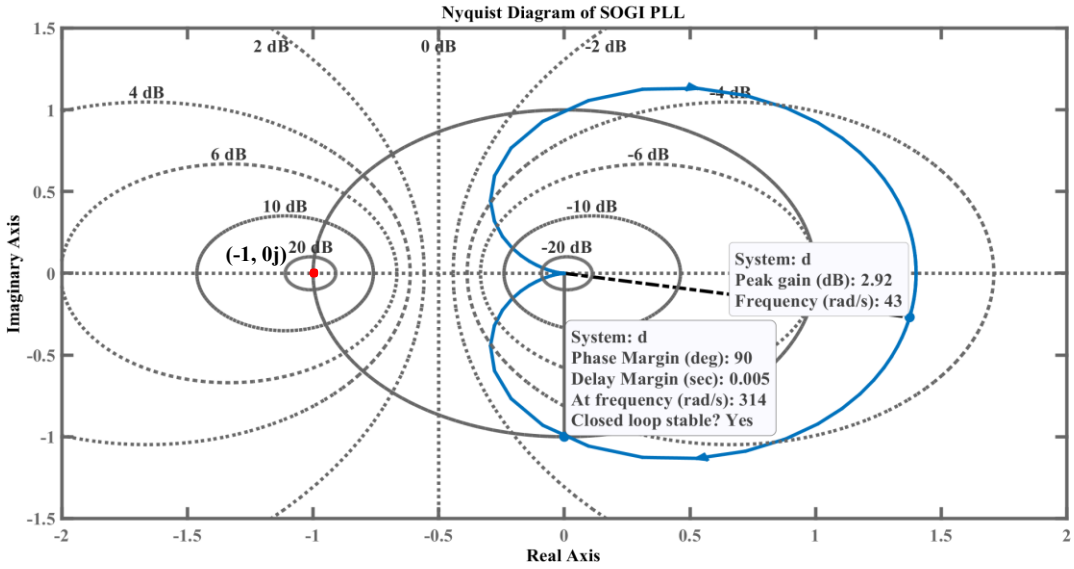


Fig. 3.9 Nyquist diagram of SOGI PLL

plotted in clockwise direction. Hence the closed loop system of SOGI PLL is stable. The plot shows a phase margin, PM of 90° with crossover frequency,ω_{pc} of 314 rad/s.

3.3.3 Least Mean Square (LMS) PLL

The diagram shown in Fig. 3.10 depicts the stability analysis of LMS PLL by Nyquist stability criterion using the transfer function given in equation 3.50. The diagram shows that the open loop plot does not encircle the critical point, (-1,0j) of the s-plane. Therefore, it is concluded that the closed loop of the system is stable. The phase margin (PM) is found to be 178° at crossover frequency ω_{pc} =511 rad/s. whereas the gain margin (GM) is 46dB at 3.14e+06 rad/s.

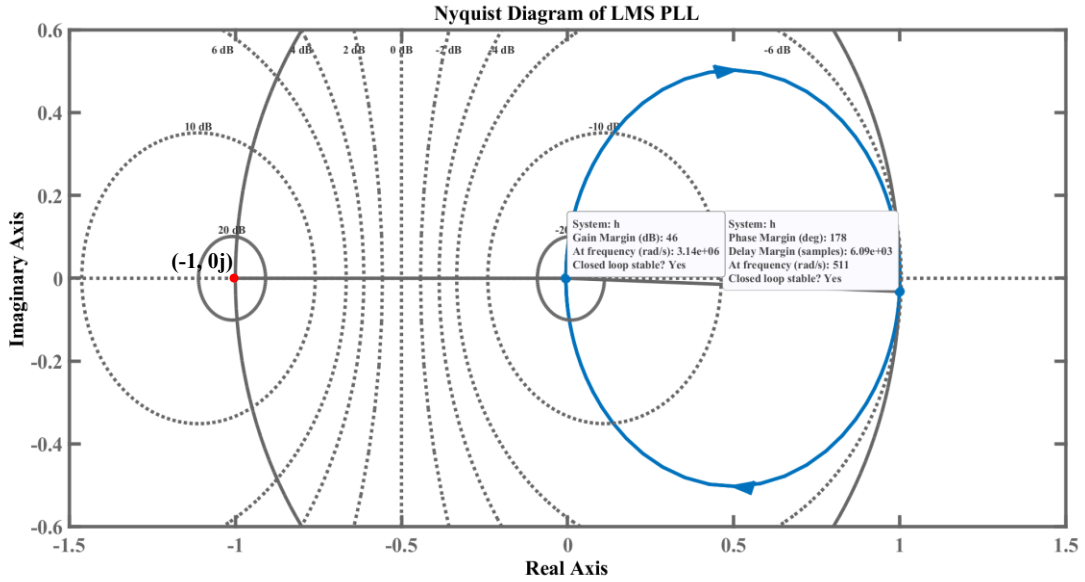


Fig. 3.10 Nyquist diagram of LMS PLL

3.3.4 Least Mean Fourth (LMF) PLL

The steady state stability analysis of LMF PLL performed with Nyquist stability criterion using the open loop transfer function is performed using equation (3.95). The Nyquist diagram shown in Fig. 3.11 does not encircle the critical point, (-1,0j) on the right-hand side of the s-plane. Hence, it is concluded that the closed loop system is stable. The phase margin (PM) is found to be 180° at 314 rad/s whereas the gain margin (GM) is 176 dB at 6.28e+04 rad/s.

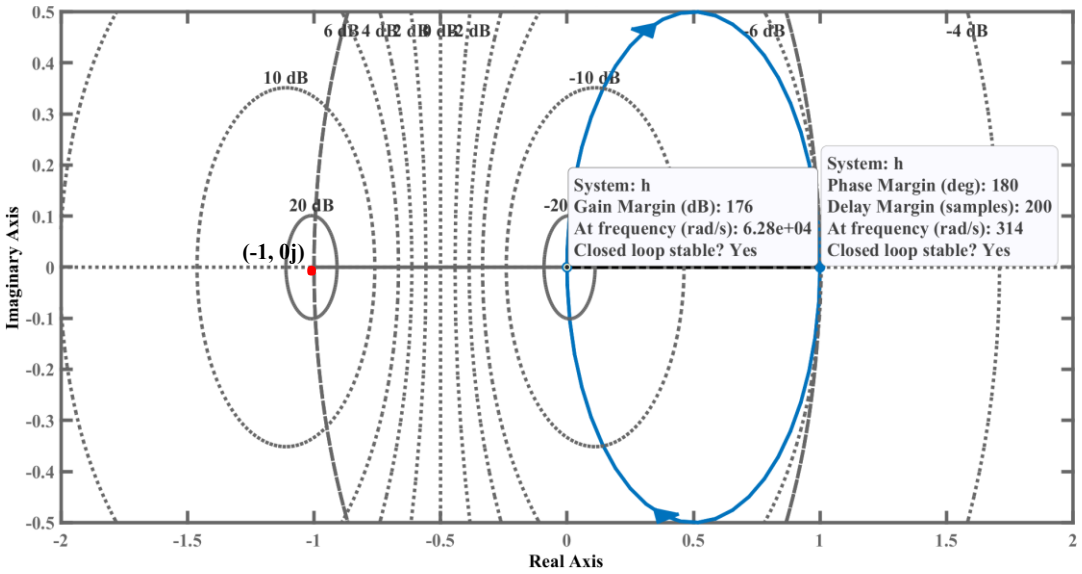


Fig. 3.11 Nyquist diagram of LMF PLL

Table 3.1: Comparison of SRF, SOGI, LMS and LMF PLLs on Nyquist stability criterion

PLL	Encirclement at (-1, 0j)	PM in (°)	ωpc in rad/s	Interpretation
SRF	No	45.1	11	Stable
SOGI	No	90	314	Stable
LMS	No	178	511	Stable
LMF	**No**	**180**	**314**	**Stable**

Table 3.1 depicts the summary of the Nyquist diagrams of SRF, SOGI, LMS and LMF PLLs for stability analysis of different PLLs. The results of the PMs are seen to be improving increasing with the improvement of the PLLs (from SRF PLL to LMF PLL). Among the conventional PLLs, LMS is seem to be more stable then SRF and SOGI PLLs in as it has more PM (178°).

3.4 Performance Analysis of Various PLLs through Simulation and Hardware Results

The dynamic performances of the various PLLs considered in this chapter (SRF, SOGI, LMS and LMF PLLs) are evaluated under different grid abnormalities like (i) 30% voltage sag (ii) 35% voltage swell (iii) polluted grid voltage, (iv) 30° phase

shift (v) +5Hz frequency change and (vi) 20% DC offset. The simulation results are obtained using MATLAB Simulink environment and experimental hardware set-ups

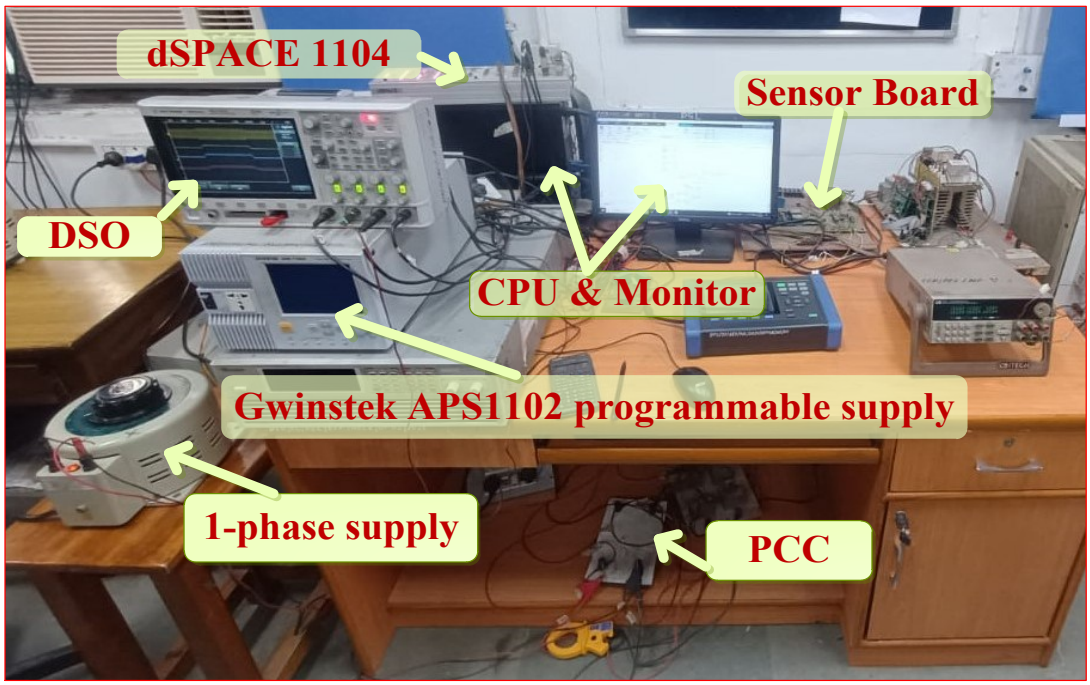


Fig. 3.12 Hardware setup for analysing the dynamic performances of different PLLs

are done in the laboratory which is shown in Fig. 3.12 for single phase and three phase to obtain the experimental results. A sinusoidal grid peak voltage of v_s=325 V and fundamental grid frequency of f=50Hz is taken as input for all the PLLs considered. The simulation is run with a sampling time of Ts=50e-6s. The hardware results of PLLs like (i) single phase SRF PLL (ii) single phase SOGI PLL (iii) single phase LMS PLL are obtained using a single-phase programmable supply of GwinSTEK model (APS-1102A) to generate different types of voltage signal waveforms like simple sinusoidal waveform, 10% of the 3rd and 5th harmonics are considered. 3rd and 5th harmonic induced waveform under polluted environment and other dynamics in the voltage. The input grid voltage has been sensed using a Hall effect voltage sensor and is passed to the dSpace 1104 controller for processing the algorithms through the Analog to Digital Converter (ADC) channel of dSpace. The estimated signals from Digital to Analog Converter (DAC) channels through mixed signal oscilloscope/digital storage oscilloscope (MSO/DSO) are analysed for different cases of non-ideal grid conditions. The values of the parameters chosen for obtaining hardware results are

v_s=100V and f =50Hz.

3.4.1 Single phase Synchronous Reference Frame (SRF) PLL

The software and hardware results of the single phase SRF PLL obtained under various abnormal grid conditions are shown in Fig. 3.14 and Fig. 3.15 respectively.

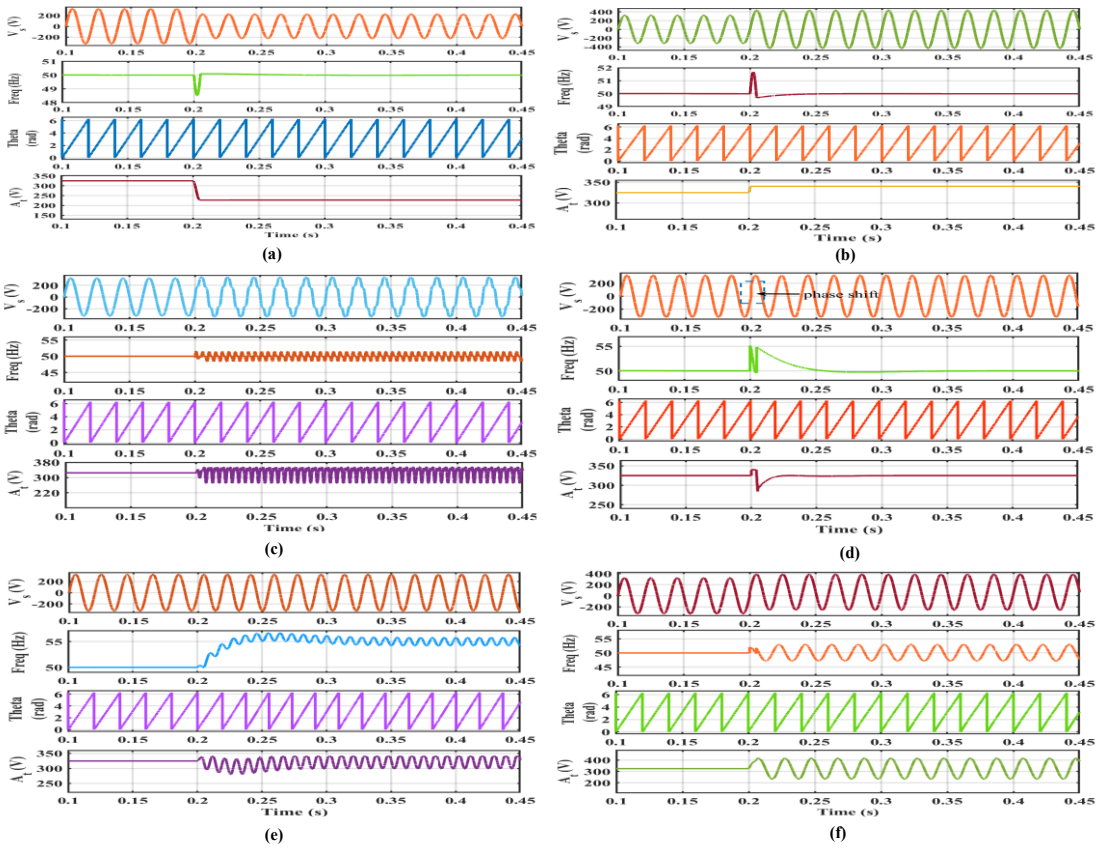


Fig. 3.13 Simulated results of single phase SRF PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

The disturbance is introduced at 0.2s instant. The plots Fig.3.13 and Fig. 3.14 of the single phase PLLs depicts the response of the source voltage v_s in volts, estimated frequency of PLL in Hz, estimated angle theta of PLL in radians and the amplitude of the source voltage. Fig. 3.14 (a) shows the simulated results of single phase SRF PLL under 30% grid voltage sag. In this plot a sharp drop of frequency is observed at (0.2s) instant of disturbance and returns to its original position within one cycle (0.022s). Fig. 3.14 (b) shows the simulated results under 35% grid voltage swell. From the plot it is observed that there is a sharp shooting of (51.67Hz) frequency but it settles down quickly within one cycle (0.02s). Fig. 3.14 (c) shows the plot when the SRF PLL is

exposed to a grid polluted voltage which contains 3rd and 5th harmonics. The frequency is affected and continuous oscillations (51.25Hz) are observed under this disturbance. The distortion in the source grid voltage due to presence of harmonic pollution can be observed here. Fig. 3.14 (d) shows the plots of the responses under 30° phase shift. At the instant, 0.2s, when the disturbance is initiated, an oscillation (55.14Hz) in the frequency response is observed but it comes to its normalcy under 3 cycles (0.056s). Fig. 3.14 (e) shows the plot of the responses of SRF PLL under +5 Hz step frequency

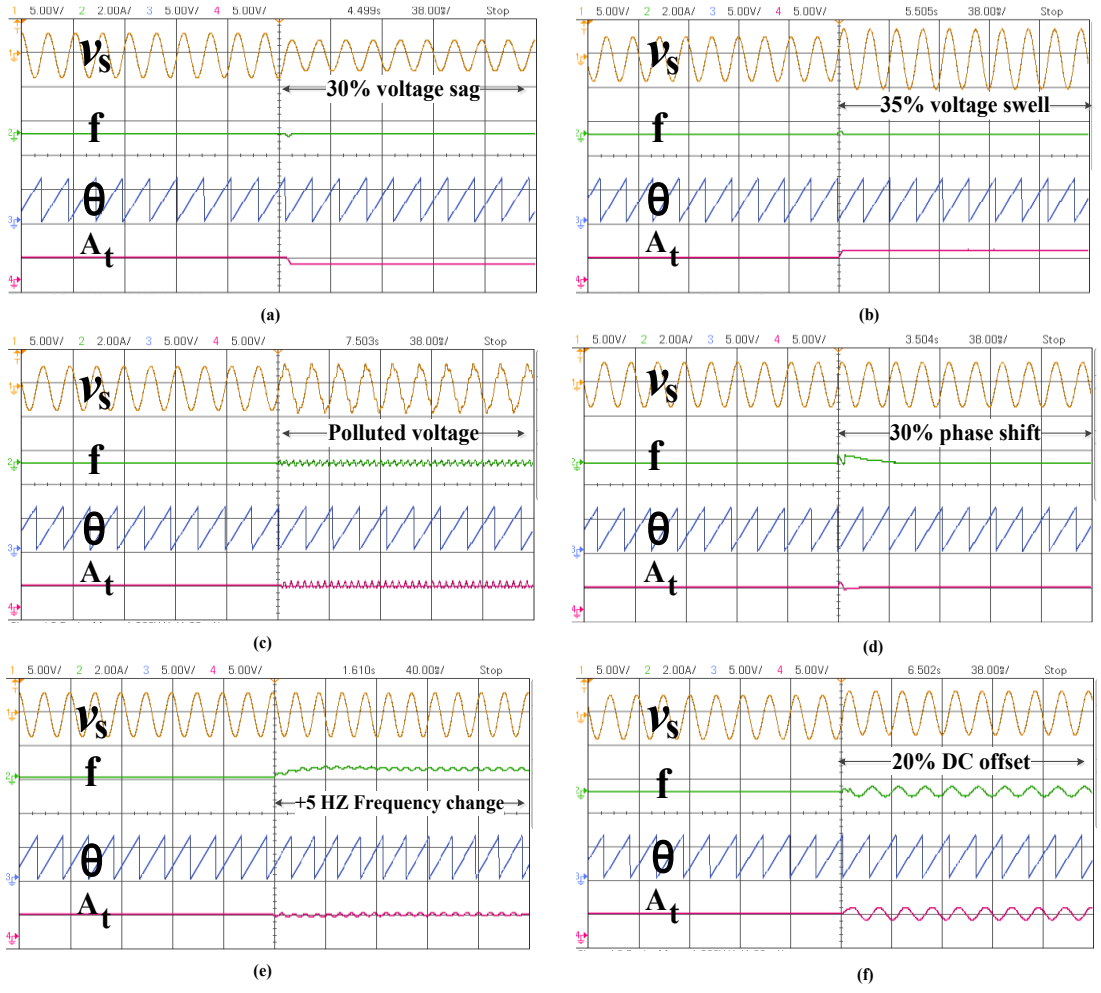


Fig. 3.14 Experimental results of single phase SRF PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

change. But during disturbance a small oscillation is seen in the amplitude of grid voltage can be observed. It shows an overshoot of 56.67Hz.Fig. 3.13 (f) shows the plot under 20% DC offset in the grid voltage. The plot shows oscillatory responses both in the frequency and the magnitude of the grid voltage.

The disturbance in the supply grid voltage is introduced for a period of 0.2s (0.2s-0.4s) for obtaining the experimental results. The hardware results of single phase SRF PLL under 30% grid voltage sag is shown in Fig. 3.14 (a). The frequency response shows that there is a drop in frequency at the time of disturbance feed. This validates the simulation result shown in Fig. 3.13(a). Fig. 3.14 (b) shows the responses under 35% grid voltage swell. The frequency response shows an oscillation and amplitude also shows the rise in response which validates the simulated results in Fig. 3.13 (b). Fig. 3.14 (c) shows the hardware results under polluted grid voltage. The frequency response shows oscillatory response during the disturbed period which validates the simulated results in Fig. 3.13(c). Fig. 3.14(d) gives the results under 30^{o} phase shift disturbance. The frequency response shows an oscillation which comes to its normalcy at three cycles and it validates the simulation results. Fig.3.14 (e) shows the response of the PLL at +5Hz frequency step change. The frequency response shows the desired change validating its simulated result of Fig.3.13 (e). Fig. 3.14 (f) shows the experimental result under presence of 20% DC offset in grid voltage. The frequency and magnitude plots show oscillatory response validating the simulation results in Fig. 3.13 (f).

Therefore from Fig. 3.13 and Fig. 3.14 it is seen that the simulation and experimental responses validate each other.

3.4.2 Single phase Second Order Generalized Integrator (SOGI) PLL

The simulated results of SOGI PLL showing the plots of the response of grid voltage, v_s in volts, frequency in Hz, phase angle in rad and amplitude of the grid voltage in volts under various grid abnormalities are shown in Fig. 3.15. Fig. 3.15 (a) shows the plot of SOGI PLL under 30% grid voltage sag abnormality. The frequency response shows a peak oscillation (52.13Hz) but it settles down within 3 cycles (0.047s). The simulation results under 35% grid voltage swell abnormalities are shown in Fig. 3.15 (b). The frequency response shows overshoot (53.38Hz) and it dies down to its normal condition under 3 cycles (0.059s). Fig 3.15 (c) shows response under polluted grid voltage. The frequency and magnitude plot show oscillatory responses during the entire disturbed period. Fig. 3.15 (d) shows the plot of the responses of

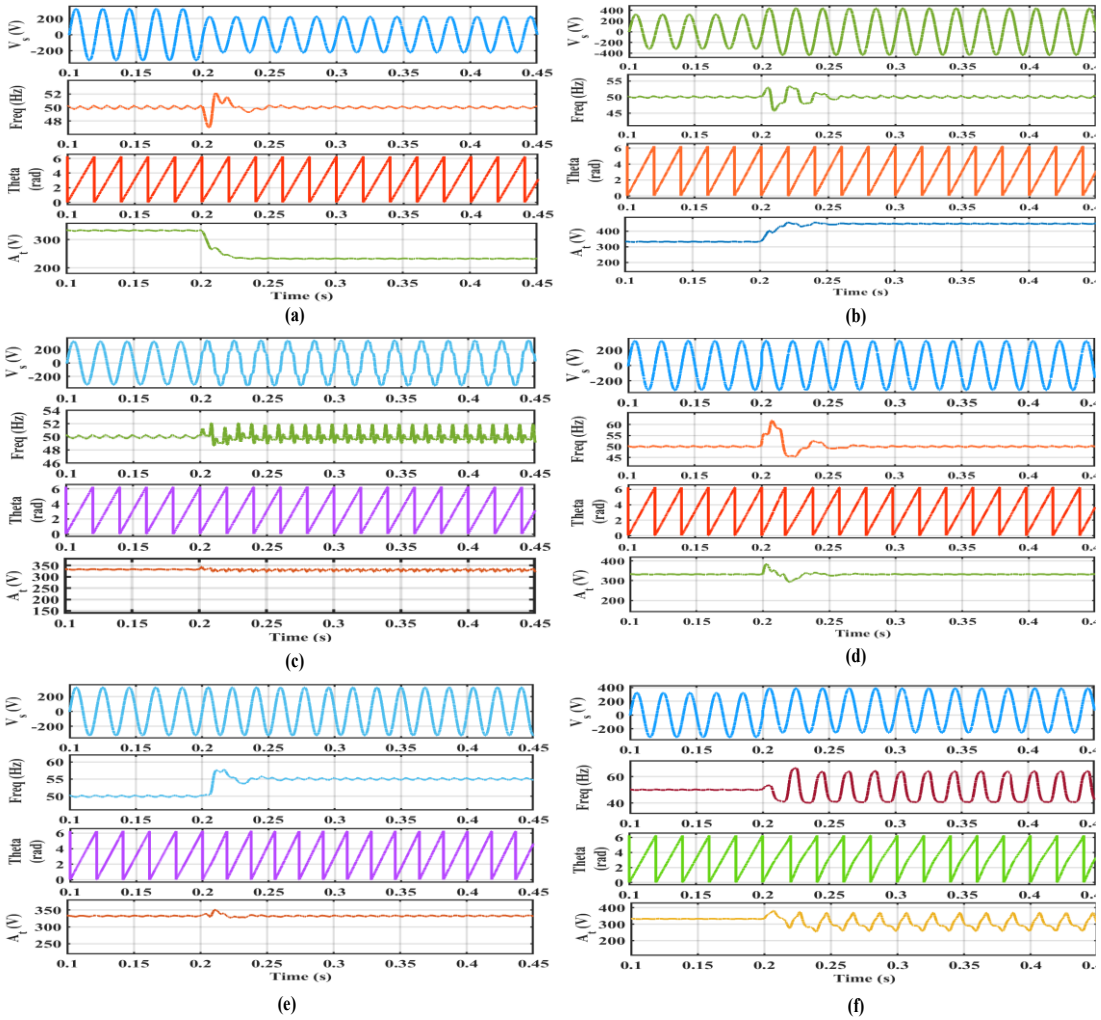


Fig. 3.15 Simulated results of single phase SOGI PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

SOGI PLL under 30° phase shift. The frequency plot shows a peak oscillation (61.5 Hz) which settles down within 4 cycles (0.065s). Fig. 3.15 (e) shows the response under +5Hz frequency change. The frequency plot shows a peak oscillation (57.79 Hz) that dies down within 2 cycles (0.036s). Fig. 3.15 (f) shows simulation results of single phase SOGI PLL under 20% DC offset. Plots of frequency and magnitude show oscillatory response during disturbed period.

The hardware results of single phase SOGI PLL under 30% grid voltage sag is shown in Fig. 3.16 (a). The experimental results show that frequency response has oscillations but settles down within 3 cycles. The grid voltage source shows the occurrence of 30% voltage sag validating the simulated result of Fig. 3.15 (a). Fig. 3.16 (b) shows the plot of SOGI PLL under 35% grid voltage swell disturbance. The

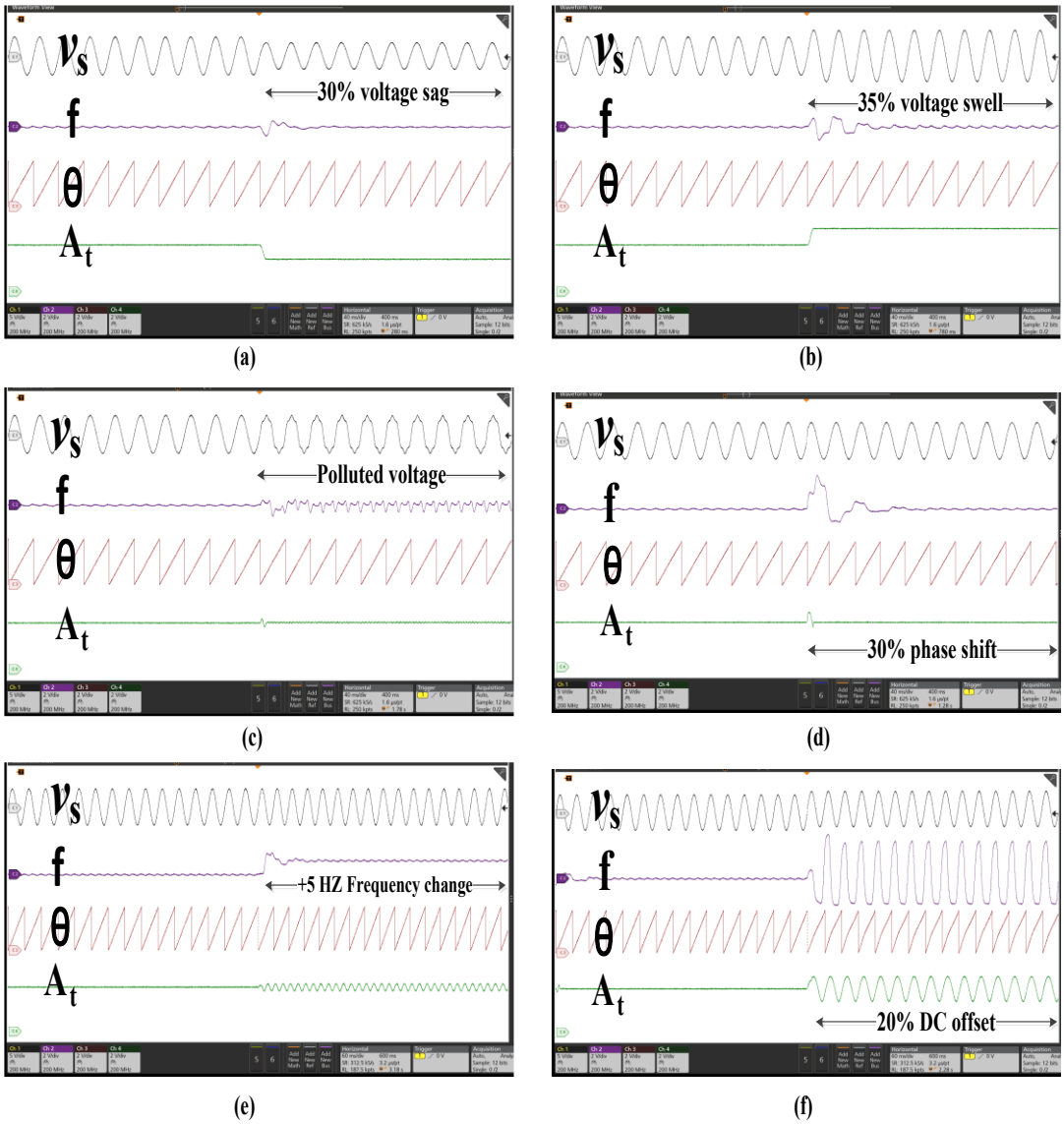


Fig. 3.16 Experimental results of single phase SOGI PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

swell in voltage is observed in grid voltage plot. The frequency response shows oscillation which dies down within three cycles validating the simulated results of Fig. 3.15 (b). Fig. 3.16 (c) shows the hardware results under polluted grid voltage. The frequency response shows oscillation during the disturbed period. The phase angle remains unaffected validating its simulated results in Fig. 3.15 (c). Fig. 3.16 (d) gives the response of single phase SOGI PLL under 30° phase shift disturbance. The frequency response shows overshoot that settles down within four cycles. The voltage magnitude response also shows a small overshoot. Fig.3.16 (e) shows the response of the PLL at +5 Hz frequency change. Fig. 3.16(f) shows the experimental response

under 20% DC offset in grid voltage. The frequency and voltage magnitude responses show oscillatory responses during entire disturbance.

Therefore from Fig. 3.15 and Fig. 3.16 it is seen that the simulation and experimental responses validate each other.

3.4.3 Single Phase Least Mean Square (LMS) PLL

The simulation and experimental results of LMS-PLL are plotted with responses of the grid voltages, frequency (Hz), phase angle in radian, and magnitude of grid voltage in volts. The plots of the simulation results are shown in Fig. 3.17. Fig. 3.17 (a) shows the simulated results of LMS PLL under 30% grid voltage sag. Its frequency response plot shows a peak overshoot (51.3Hz) but it dies down and comes to normalcy within three cycles (0.053s). Fig. 3.17 (b) shows simulated results under 35% grid voltage swell disturbance. The frequency response shows a peak oscillation (52.62Hz) which settles within 4 cycles (0.08s). Fig. 3.17 (c) shows the plots when the PLL is exposed to a grid polluted voltage containing the 3^{rd} and 5^{th} harmonics of magnitude 10%. The frequency response is affected and shows oscillatory response during disturbance. Fig. 3.17 (d) shows the plots of the responses under 30^{o} phase shift and the frequency response shows a peak oscillation (52.87Hz) which comes to normalcy under 2 cycles (0.038s). Fig. 3.17 (e) shows the plot of LMS PLL under +5 Hz step frequency change and step frequency shift is seen in frequency response. The new frequency of 55Hz is tracked with larger settling time greater than 5 cycles. Fig. 3.17 (f) shows the plot of PLL responses under 20% DC offset in the grid voltage. The presence of the disturbance causes oscillated frequency response and the magnitude of the estimated grid voltage is also affected.

The hardware results of single phase LMS PLL under 30% grid voltage sag is shown in Fig. 3.18 (a). The experimental frequency shows ripples in response but it settles down within three cycles of time interval. The grid voltage source and its magnitude show the presence of 30% voltage sag in its waveforms validating the simulated results. Fig. 3.18 (b) shows the plot of LMS PLL under 35% grid voltage swell disturbance. The swell in voltage is observed in grid voltage and its magnitude response. The frequency response shows fluctuation which settles down within four

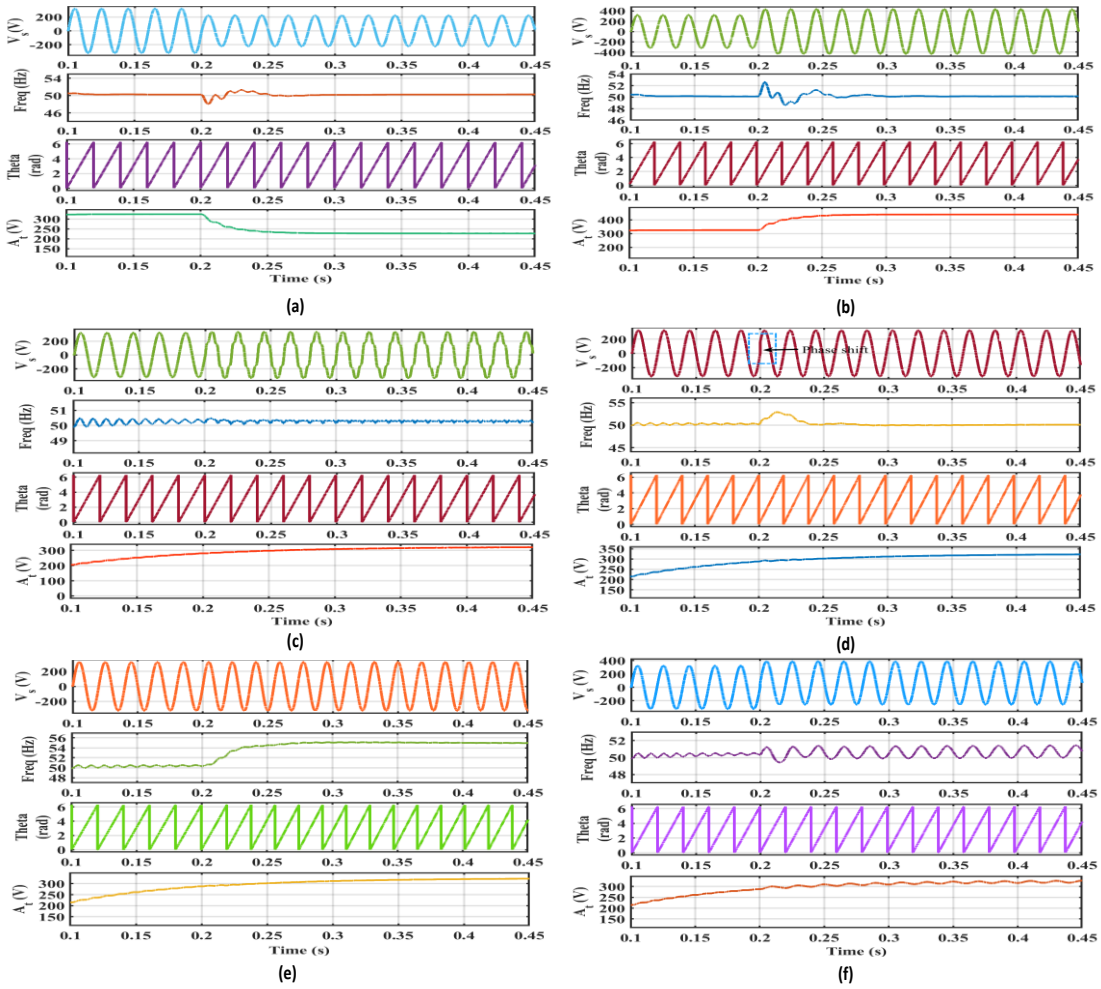


Fig. 3.17 Simulation results of single phase LMS PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

cycles validating the simulation shown in Fig. 3.17 (b). Fig. 3.18 (c) shows the hardware results under polluted grid voltage. A small peak overshoot is seen in magnitude response at the instance of harmonic introduction. Fig. 3.18 (d) gives the response of single phase SRF PLL under 30° phase shift disturbance. The frequency response shows oscillation in its response which is takes longer time than five cycles to settle validating simulation response. Fig. 3.18 (e) shows the response of the PLL at +5Hz frequency step change and the frequency response show prominent oscillations which settles down within more than 5 cycles validating its simulation results shown in Fig.3.18 8 (e). Fig. 3.18 (f) shows the experimental results under 20% DC offset in grid voltage. The frequency response shows oscillatory. The grid voltage magnitude also shows oscillatory response during the disturbance period which validates the simulation results obtained as in Fig. 3.17 (f).

Therefore from Fig. 3.17 and Fig. 3.18 it is seen that the simulation and experimental responses validate each other.

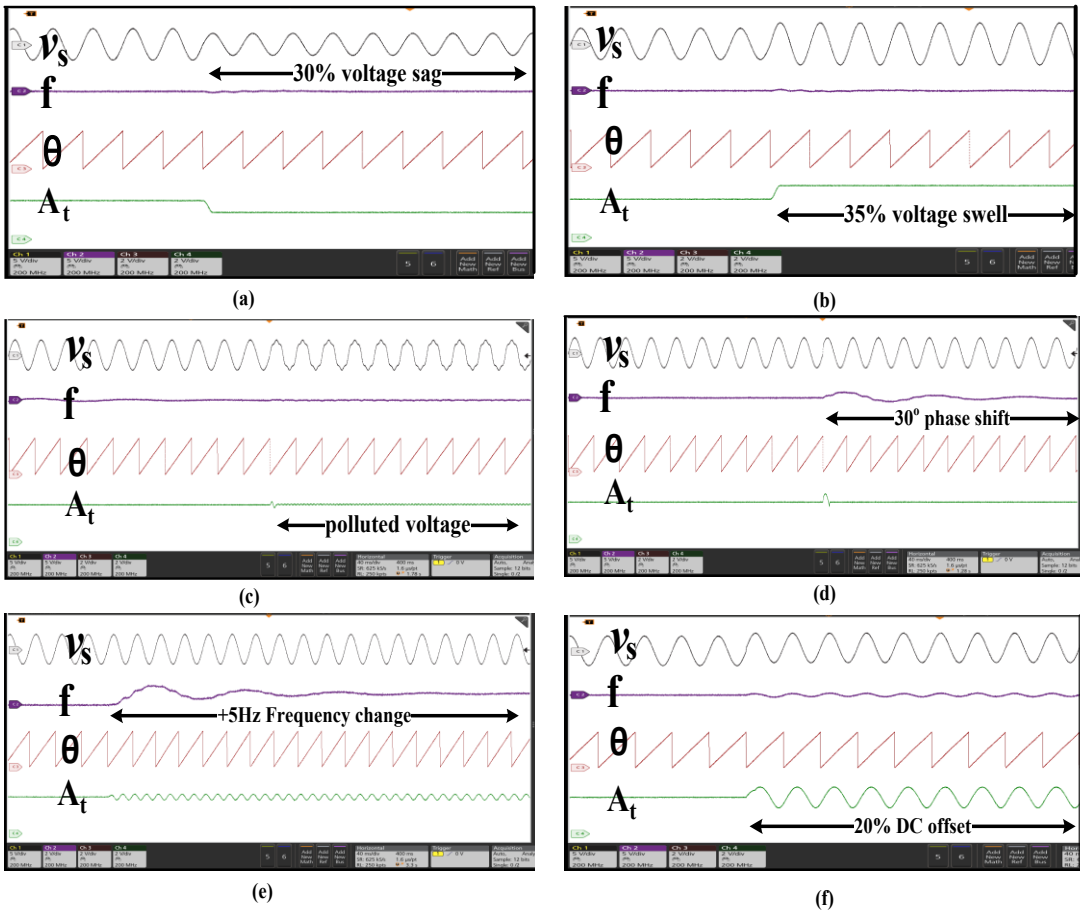


Fig. 3.18 Experimental results of single phase LMS PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

Table 3.2 shows the comparative dynamic performance analysis of single phase SRF, SOGI and LMS PLLs based on parameters like overshoot and settling time obtained from the simulation results. It is observed that under 30% grid voltage sag disturbance SRF PLL shows smallest overshoot with fastest settling time while LMS PLL shows moderate overshoot response with slowest settling response (0.053s). Under 35% grid voltage swell LMS PLL shows the best response with least overshoot (51.63Hz) and moderate settling time. SOGI PLL shows the 53.36Hz overshoot and fastest settling time. It is observed from Table 3.2 that under polluted voltage all the three PLLs shows oscillating frequency response. It is observed that under 30° phase shift LMS gives the best response with least overshoot (52.85Hz) and fastest settling

time. The dynamic response under +5Hz frequency change SRF PLL gives the best overshoot response (56.72 Hz) though the settling time is the largest (0.1s). while LMS PLL gives negative response (54.13 Hz) at the time of disturbance. The response under 20% dc offset shows that LMF has least overshoot.

Table 3.2: Comparative performance analysis of single phase SRF, SOGI and LMS PLLs based on overshoot and settling time

Grid condition tested	**Parameter considered**	**SRF PLL**	**SOGI PLL**	**LMS PLL**
30% voltage sag	**Overshoot**	50.25Hz	52.16Hz	51.32Hz
	Settling time	0.04s	0.048s	0.053s
35% voltage swell	**Overshoot**	51.69 Hz	53.36 Hz	51.63Hz
	Settling time	0.069s	0.059s	0.061s
Polluted grid voltage	**Overshoot**	51.4 Hz	52 Hz	50.4 Hz
	Settling time	distorted	oscillating	oscillating
30^{o} phase shift	**Overshoot**	55.14 Hz	61.72 Hz	52.85Hz
	Settling time	0.058s	0.065s	0.04s
+5 Hz frequency shift	**Overshoot**	56.72 Hz	57.7 Hz	54.13Hz
	Settling time	0.1s	0.037s	0.07s
20% dc offset	**Overshoot**	53Hz	66.49 Hz	51.38Hz
	Settling time	distorted	distorted	distorted

3.4.4 Three-phase Synchronous Reference Frame (SRF) PLL

The simulation results of three phase SRF PLL are shown in Fig. 3.19 considering the responses of phase 'a' grid voltage, v_a in volts, sine theta, frequency in Hz and phase angle in radians of PLL. The simulation is run for a time interval of 0.35s to 0.65s. Fig. 3.19 (a) shows the plot of three phase SRF PLL response under 30% grid voltage sag of grid abnormality. The grid voltage and sin theta response of

phase ‘a’ are in the same phase. The frequency and phase angle response are shown, the tracked frequency is 50Hz. Fig. 3.19 (b) shows the plot of responses under 35%

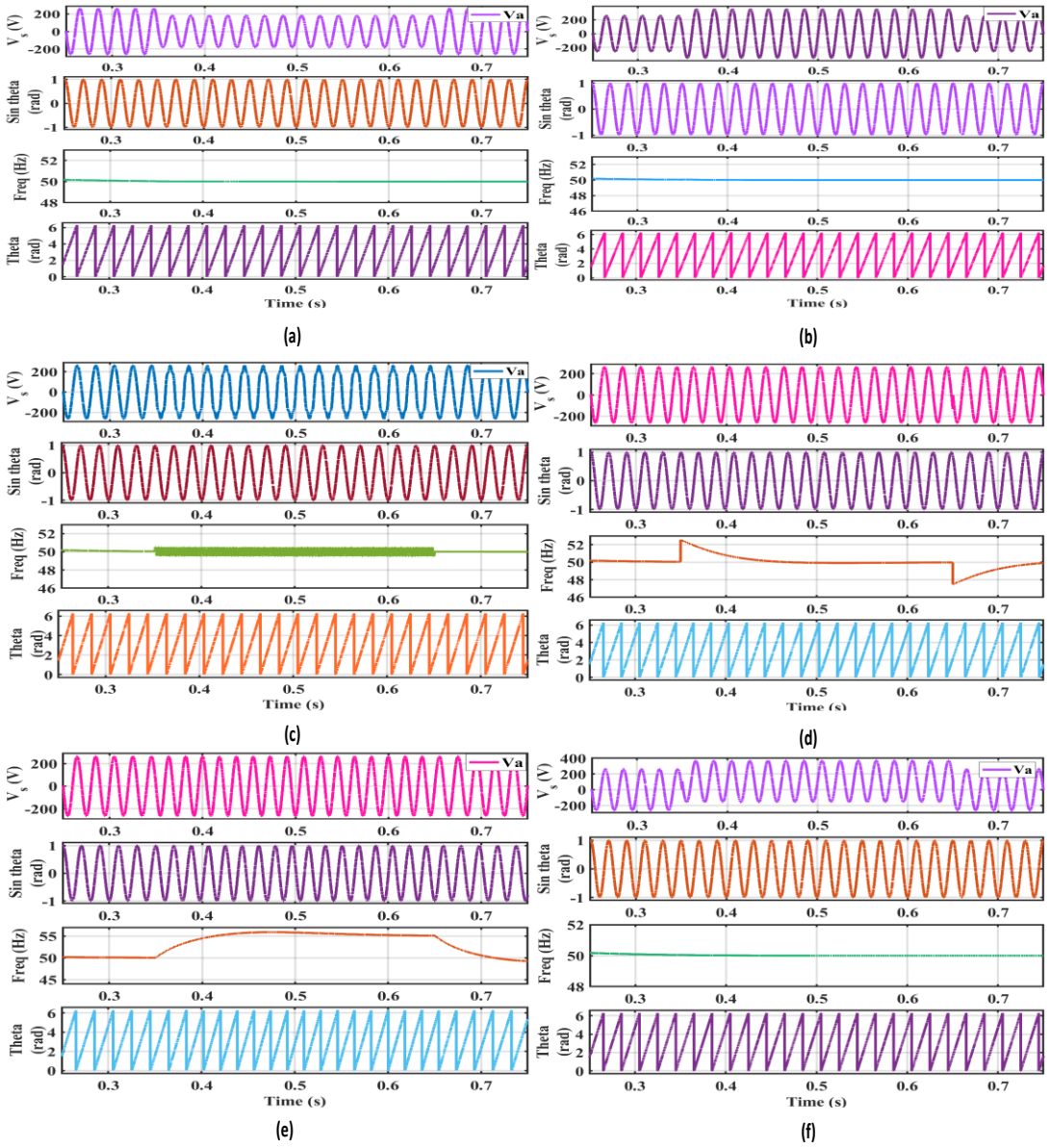


Fig. 3.19 Simulation results of three phase SRF PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

grid voltage swell. The grid voltage response shows voltage swell and is in phase with the obtained in-phase template or sine theta signal. The frequency and phase angle response remains unaffected. Fig 3.19 (c) shows the response under polluted grid voltage. The frequency response shows oscillatory response during the entire disturbance period. There is no change in the phase angle response but prominent

oscillation is observed in frequency response from during the disturbance. Fig. 3.19 (d) shows the plot of responses of three phase SRF PLL under 30º phase shift. The frequency response shows a peak oscillation 53 Hz and is settles down within five cycles. Fig. 3.19 (e) shows the plot of PLL under +5Hz frequency change. Frequency response does not able to settles down within the disturbance. Fig. 3.19 (f) shows the result under 20% DC offset. The frequency, voltage magnitude, does not show prominent changes though voltage response does show the presence of 20% DC offset.

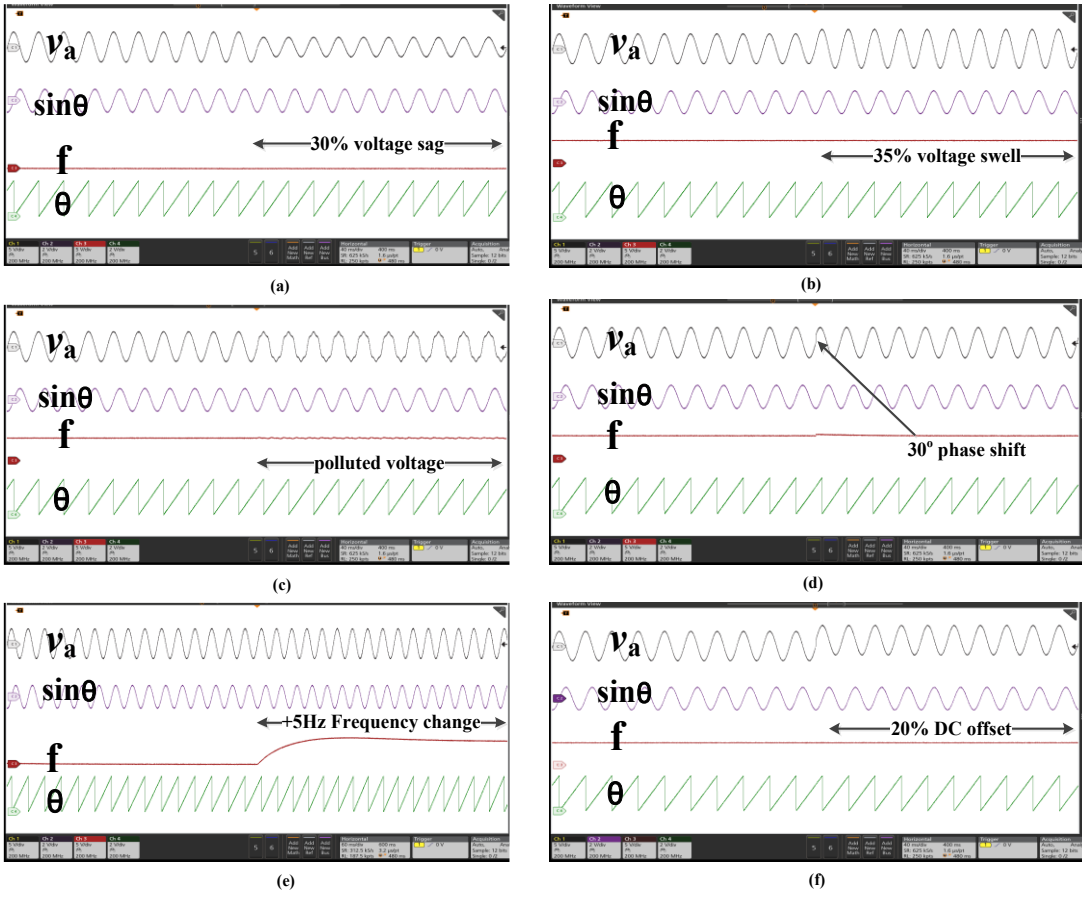


Fig. 3.20 Experimental results of three phase SRF PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30º phase shift (e) +5Hz frequency change and (f) 20% DC offset

Fig. 3.20 discusses the experimental results of three phase SRF PLL under grid abnormalities like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30º phase shift (e) +5 Hz frequency change (f) 20% DC offset are shown in Fig. 3.21. The experimental results are taken considering responses of grid voltage in volt, sin theta of phase angle, frequency in Hz and theta of phase angle. Fig. 3.20 (a) and Fig. 3.20 (b) show the experimental results of three phase SRF PLL under 30% and

35% grid voltage sag and swell. The frequency responses do not reflect prominent changes under these disturbances. Fig. 3.20 (c) shows the experimental results under polluted environment. Under this grid disturbance the frequency shows oscillatory response during the period of disturbance while the phase angle does not show prominent change during the disturbance. Fig. 3.20 (d) show the experimental result under 30^o phase shift. Under this disturbance overshoot in frequency response is seen which takes around 5 cycles to settle down validating the experimental results. Fig. 3.20 (e) shows the experimental results under +5 Hz frequency change. Under this disturbance +5 Hz frequency change is seen in frequency response while grid voltage, phase angle responses do not show any prominent change validating the simulation angle shown in Fig. 3.19 (e). Fig. 3.20 (f) shows the experimental results under 20% DC offset. The grid voltage response shows the presence of 20% DC offset while the frequency and phase angle responses do not show significant changes validating the simulation results shown in Fig. 3.19 (f).

Therefore from Fig. 3.19 and Fig. 3.20 it is seen that the simulation and experimental responses validate each other.

3.4.5 Three Phase Least Mean Fourth (LMF) PLL

The simulation results of three phase LMF PLL is shown in Fig. 3.21 and the plots of phase 'a' grid voltage, v_a in volts, sine theta, frequency in Hz and phase angle in radians of PLL are shown. The simulation is run for a time interval of 0.35s to 0.65s. Fig. 3.21 (a) and Fig. 3.21 (b) shows simulation results under 30% grid voltage sag and 35% grid voltage swell. The grid voltage and sin theta responses are in phase with one another indicating the PLL correctly computes the phase angle. The frequency is close to 50Hz and is not affected. Fig 3.21 (c) shows the response under polluted grid voltage. It is shows that the frequency response remained unaffected even with polluted voltage containing 3rd and 5th harmonics. Fig. 3.21 (d) shows the results of the responses under 30^o phase shift. The frequency response shows a peak oscillation 53 Hz and settles down within 6 cycles. Fig. 3.21 (e) shows the results under +5Hz frequency change. The grid voltage 'v_a', is observed to be in-phase with sin theta signal. The frequency response of +5Hz step change is seen. Fig. 3.21 (f) shows plot

of response under 20% DC offset. Frequency and phase angle show no prominent response under this disturbance.

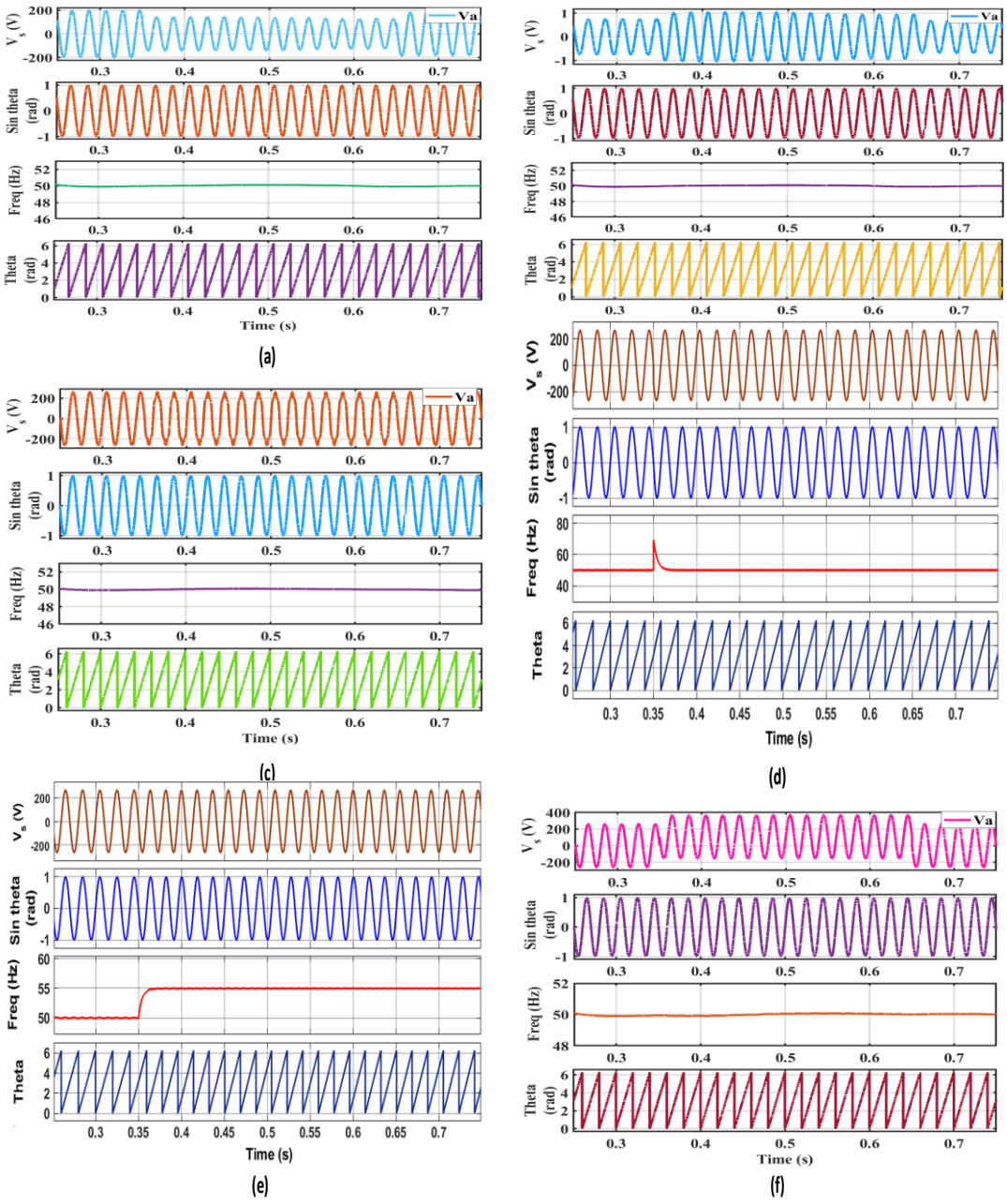


Fig. 3.21 Simulation results of three phase LMF PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

The hardware results of three phase LMF PLL are shown in Fig. 3.22 considering the responses of grid voltage, v_a in volts, sine theta, frequency in Hz and phase angle in radians of PLL.Fig. 3.22 (a) and Fig. 3.22 (b) show the plots of three phase LMF PLL responses under 30% grid voltage sag and 35% grid voltage swell

abnormalities respectively. The grid voltage and sin theta responses are observed to be in phase with one another. The grid voltage signals show the drop and swell in the responses. The frequency response and the phase angle response do not show

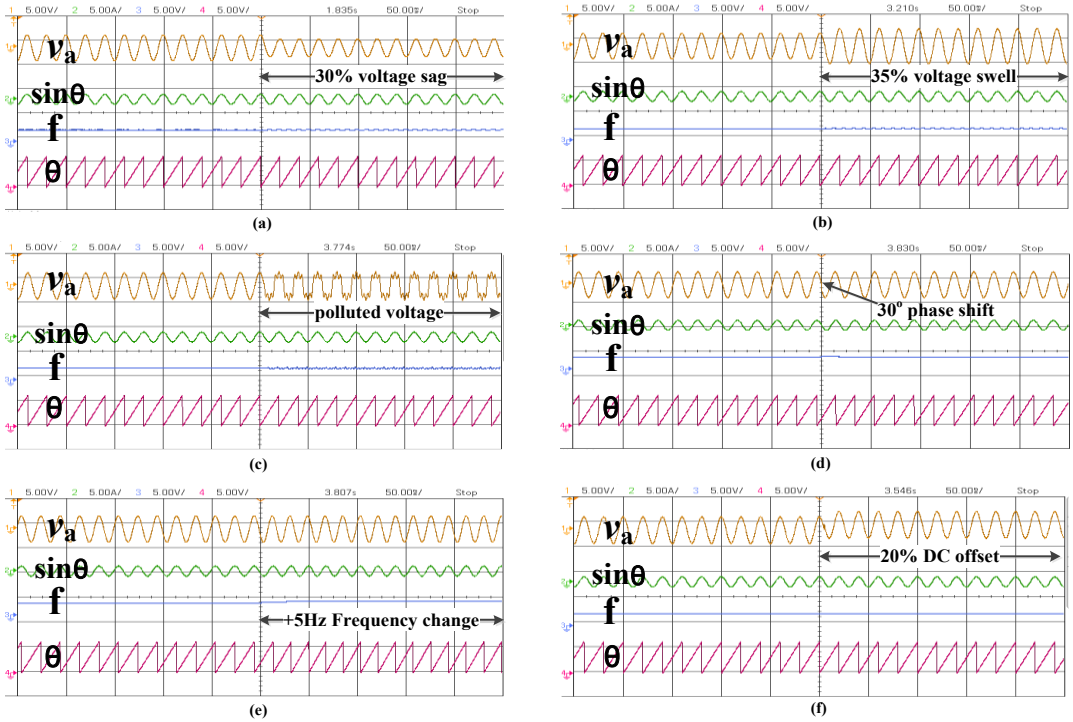


Fig. 3.22 Experimental results of three phase LMF PLL at (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30° phase shift (e) +5Hz frequency change and (f) 20% DC offset

prominent changes during these disturbances. Fig 3.22 (c) shows the response of three phase LMF PLL under polluted grid voltage. It is shows that the frequency response shows very small oscillations during the disturbed interval. The voltage signal response is distorted due to the presence of 3rd and 5th harmonics in grid voltage. The phase angle does not show prominent visible change. Fig. 3.22 (d) shows the experimental result under 30° phase shift. The frequency response shows change overshoot which settles down within two cycles. Fig. 3.22 (e) shows the plot of the PLL under +5Hz frequency change. The grid voltage 'v_a', shows no change and is in-phase with sin theta signal while frequency response show +5Hz change. Fig. 3.22 (f) shows plot of responses under 20% DC offset. The voltage signal response shows the presence of DC offset while frequency, phase angle does not show prominent changes.

Therefore from Fig. 3.21 and Fig. 3.22 it is seen that the simulation and experimental responses validate each other.

3.4.6 Comparative Analysis of the PLLs

The comparative performance analysis of the single phase PLLs like (i) SRF (ii) SOGI (iii) LMS is tabulated in Table 3.3 considering the parameters like overshoot and settling time under the grid abnormalities considered. The results are tabulated using simulation responses. Table 3.3 shows comparative analysis of the dynamic performance of single SRF, SOGI and LMS that under 30% voltage sag SRF PLL has the lowest overshoot (50.25Hz) and fastest settling time (0.04s) than SOGI and LMS PLLs. Under the 35% voltage swell the LMS PLL is showing better performance than the other SRF and SOGI PLLs depicting an overshoot of 51.63 Hz and moderate settling time of 0.06s. With polluted grid voltage it is observed that all the three PLLs (SRF, SOGI and LMS) show oscillations in frequency during the disturbed time interval but LMS gives the least overshoot (50.4 Hz) than SRF (51.4Hz) and SOGI (52 Hz) PLLs. Under the disturbance of +5Hz frequency change, again LMS PLL shows best performance with least overshoot (54.13Hz) and moderate settling time (0.07s) than SRF and SOGI PLL. SOGI PLL gives better performance under +5 Hz frequency change with least settling time but with highest overshoot (57.7Hz). The dynamic performance under the presence of 20% DC offset showed that LMS PLL gives better performance with least overshoot (51.38 Hz). Thus overall, comparatively best performance is observed with LMS PLL under all disturbances (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30^{o} phase shift (e) +5Hz frequency change and (f) 20% DC offset.

Table 3.4 is also shown to depict the comparative dynamic performance analysis of three phase SRF PLL and LMF PLL. The simulation and hardware results are presented in Fig. 3.20 to Fig. 3.22 of the three phase SRF and SOGI PLLs shows affects in the frequency response during the 30^{o} phase shift and +5 Hz frequency changes. Therefore, only these parameters are tabulated in Table 3.3 for comparative analysis. Under 30^{o} phase shift, LMF shows least overshoot (51.29Hz) but slower response (1.1s) while during +5 Hz frequency shift the LMF and SRF gives nearly same overshoot (56 Hz) but SRF PLL shows the sluggish performance than LMF PLL. Hence, LMF PLL shows better dynamic performance than SRF PLL.

Table 3.3: Comparative performance analysis single phase SRF, SOGI and LMS PLLs

	Parameter considered	SRF PLL	SOGI PLL	LMS PLL
30% voltage sag	**Overshoot**	Lowest (50.25Hz)	Highest (52.16Hz),	Moderate (51.32Hz)
	Settling time	Fast response (~ 2 cycles) 0.04s	slower response (~3 cycles) 0.048s	slowest response (~3 cycles) 0.053s
35% voltage swell	**Overshoot**	Moderate (51.69 Hz)	Highest (53.36 Hz)	Least (51.63Hz)
	Settling time	Sluggish (more than 3 cycles) 0.069s	Fast (~ 3cycle) 0.059s	Moderate (~2cycles) 0.061s
Polluted grid voltage	**Overshoot**	Moderate (51.4 Hz)	Highest (52 Hz)	Lesser (50.4 Hz)
	Settling time	distorted (entire disturbed interval)	oscillating (entire disturbed interval)	oscillating (entire disturbed interval)
30^{o} phase shift	**Overshoot**	Moderate (55.14 Hz)	Highest (61.72 Hz)	Lesser (52.85Hz)
	Settling time	sluggish (~ 3 cycles) 0.058s	Slow (more than 3 cycles) 0.065s	Fast (2 cycles) 0.04s
+5 Hz frequency shift	**Overshoot**	Moderate (56.72 Hz)	Highest (57.7 Hz)	54.13 Hz
	Settling time	Sluggish response (~ 5 cycles) 0.1s	Fast response (~ 2 cycles) 0.037s	Moderate (~ 4 cycles) 0.07s
20% dc offset	**Overshoot**	Moderate (53Hz)	Largest (66.49 Hz)	Lowest (51.38Hz)
	Settling time	distorted (entire disturbed interval)	distorted (entire disturbed interval)	distorted (entire disturbed interval)

Table 3.4 Comparative performance analysis of three phase SRF, and LMF PLLs

Grid condition tested	**Parameter considered**	**SRF PLL**	**LMF PLL**
30% voltage sag	**Overshoot** **Settling time**	50.03Hz (+ve) 0.135s	49.8Hz (-ve) Fast 0.025s
35% voltage swell	**Overshoot** **Settling time**	50.06Hz 0.086s	49.8 Hz Fast 0.014s
Polluted voltage	**Overshoot**	Oscillatory	oscillatory
30^{o} phase shift	**Overshoot** **Settling time**	High (52.51 Hz) Slow response 0.07s	Least (51.29 Hz) Fast response 0.02s
+5 Hz frequency shift	**Overshoot** **Settling time**	Less (55.89 Hz) Resumes more tunning effort	Less (55.07 Hz) Fast response
20% DC offset	**Overshoot** **Settling time**	50.04Hz 0.1s	49.94Hz Slower 0.12s

3.5 Conclusion

The mathematical modelling for the design of the conventional single phase PLL like SRF, SOGI and LMS are done and their transfer functions are estimated. Similarly, three phase PLLs such as SRF and LMF PLL are also modelled and their transfer functions have been developed. The developed transfer functions of the single phase PLLs (SRF, SOGI, LMS) and three phase PLLs (SRF, LMF) are used to study the steady state stability with Nyquist plots. All the PLLs are found to be stable although PM of LMF PLL is obtained to be the highest. The simulated and the experimental results are obtained under grid disturbances like (i) 30% voltage sag (ii) 35% voltage swell (iii) polluted grid voltage, (iv) 30^{o} phase shift (v) +5Hz frequency change and (vi) 20% DC offset. The experimental results validate the simulation results of suitable comparison tables have been prepared to validate the performance of PLLs. For three phase PLLs, the conventional SRF PLL and LMF PLL are modelled and their respective transfer functions are estimated. Their state dynamic performance is studied with simulated and experimental results. The experimental results are found to be validating the simulated results. From the results it is observed that the frequency response under 30%voltage sag, 35% voltage swell, polluted grid voltage and DC-

offset seen to remain almost unaffected. However, the performance of LMF PLL is better than SRF PLL under 30^{o} phase shift and +5Hz frequency change grid disturbances.

Chapter: 4

MODELLING AND PERFORMANCE ANALYSIS OF DIFFERENT TYPES OF PLLs

4.1 Introduction

Phase lock loops (PLLs) are used as synchronization technique for numerous kinds of grid systems. The major function of a PLL is detecting the frequency and phase angle of grid voltage. Proper utility grid synchronization is essential for controlling the power converters connected at the point of common coupling (PCC) for obtaining maximum efficiency. PLL is a closed-loop feedback control system and it synchronizes the frequency and phase angle of the output signal with the reference input signals. A fundamental PLL always has three fundamental parts which consist of a (i) phase error detector (PD), (ii) loop filter (LF) and(iii) voltage-controlled oscillator (VCO). The general block diagram showing structure of a fundamental PLL is shown in Fig. 4.1. Every part of this PLL structure plays a specific role to perform its function satisfactorily. The modelling and performance analysis of different types

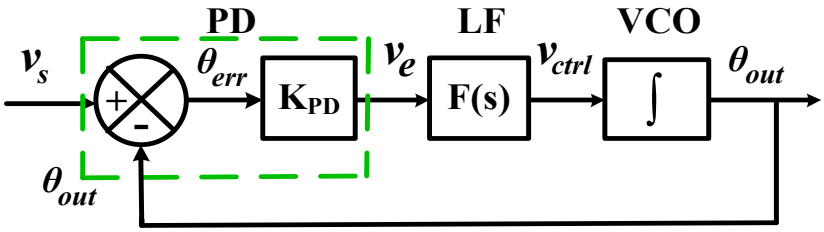


Fig. 4.1 General block diagram of a PLL structure

of phase locked loops (PLLs) focus on its key fundamental components, operating principles, dynamic behaviour and steady state stability analysis. The transfer function each type of PLL is calculated after mathematical modelling. The steady state stability analysis helps to compute stability using the obtained transfer functions. This chapter presents the design modelling and performance analysis of single-phase Type I, Type II and Type III PLLs. The comparison of different types of PLLs is also carried out at

the end of this chapter. The simulation and experimental results of the three types of PLLs are presented to validate the theoretical analysis under abnormal grid conditions like 30% voltage sag, 35% voltage swell, polluted, 30° phase shift, +5 Hz frequency change and 20% DC offset.

4.2 General Approach for the Design of Types and Orders of a PLL

The types and orders of any PLL are the two main characteristics of that PLL. Types and orders of a PLL are defined by the presence of different designs of loop filter in PLL. The order of a PLL is the highest degree of the characteristic polynomial of transfer function of the PLL. The degree indicates the number of poles in the open loop transfer function of that PLL. The type of a PLL is indicated by the number of the integrators in the loop which also gives the number of poles at origin (s=0). The loop filter (LF) determines the types and order of the PLL.

The general design approach for any type and order of a PLL is shown in Fig. 4.2. The general approach for designing a PLL includes defining its core components, a frequency/phase detector (F/PD) which detects the voltage signal's frequency or phase error between output voltage and reference grid voltage, loop filter (LF) which is usually a low- pass filter used to eliminate the error, and a voltage-controlled oscillator (VCO) which gives the estimated output voltage signal and then iteratively modifying them to achieve the desired performance. Here 'K_{PD}', 'K_{VCO}', LF_1, LF_2 and LF_3 represent the gain of the frequency/ phase detector (F/PD), VCO and loop filter of loop1 (LF_1), loop2 (LF_2) and loop3 (LF_3). Considering a loop filter LF_1

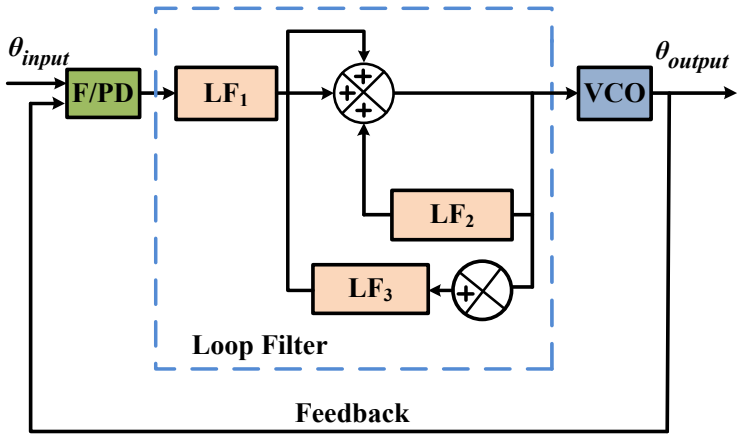


Fig. 4.2 Block diagram of the general approach for design of Types of PLL

with 'τ' as the time constant the transfer function of LF_1 can be expressed as

$$Tf_{LF1}(s) = \frac{1}{1+s\tau} \tag{4.1}$$

The transfer function of the VCO is expressed as

$$Tf_{VCO}(s) = \frac{K_{VCO}}{s} \tag{4.2}$$

The open loop transfer function of a PLL (PLL_1) having LF_1 as loop filter can be expressed as

$$Tf_{PLL_1}(s) = (K_{PD})\,(Tf_{LF1})$$

$$= (K_{PD})\left(\frac{1}{1+s\tau}\right)\left(\frac{K_{VCO}}{s}\right)$$

$$= \frac{(K_{PD})\,(K_{VCO})}{s(1+s\tau)} \tag{4.3}$$

The equation (4.3) gives two poles, one pole at s=0 and another pole at $s = -\frac{1}{\tau}$. The pole at s=0 indicates the presence of one integer in the PLL structure. The highest degree of the characteristic polynomial, $s(1+s\tau) = s^2\tau + s$, is two. Hence, the order of such PLL having LF_1, is two and therefore such PLL is of Type I and order 2.

Consider another PLL_2 with a loop filter, (LF_2) having a transfer function as

$$Tf_{LF2}(s) = \left[\frac{1}{(1+s\tau_1)}\right]\left[\frac{1}{(1+s\tau_2)}\right] \tag{4.4}$$

Then the open loop transfer function of PLL_2 with LF_2 having T.F shown in Eq. 4.4 can be expressed as

$$Tf_{PLL_2}(s) = (\mathrm{K}_{PD})\,(\mathrm{Tf}_{LF2})\,(Tf_{VCO})$$

$$= (\mathrm{K}_{PD})\left[\frac{1}{(1+s\tau_1)}\right]\left[\frac{1}{(1+s\tau_2)}\right]\left(\frac{K_{VCO}}{s}\right)$$

$$= \frac{(\mathrm{K}_{PD})\,(K_{VCO})}{[s^3\tau_1\tau_2 + s^2(\tau_1+\tau_2)+s]} \tag{4.5}$$

The transfer function of PLL_2 with LF_2 given in equation (4.5) shows that the PLL_2 has three poles. These poles are at s=0, $s = -\frac{1}{\tau_1}$, $s = -\frac{1}{\tau_2}$. The pole at s=0 indicates

that one integrator is present in the loop filter showing that the PLL_2 is of a Type I PLL due to the presence of one

integrator or a pole at origin. The highest degree of the characteristic polynomial of the PLL_2 is three, so such PLL is of order 3. Therefore, PLL_2 is a Type I and of order 3 PLL. Again, consider a third PLL, (PLL_3) with a loop filter, LF_3. The loop filter LF_3 has both zeros ($s\tau_{z1}$) and poles ($s\tau_3$) with transfer function of LF_3 expressed as

$$\mathrm{Tf}_{LF3}(s) = \frac{1+s\tau_{z1}}{s\tau_3} \tag{4.6}$$

The open loop transfer function of PLL_3 can be expressed as

$$\mathrm{Tf}_{PLL_3} = (\mathrm{K}_{PD})\,(\mathrm{Tf}_{LF3})\,(Tf_{VCO})$$

$$= (\mathrm{K}_{PD})\left(\frac{1+s\tau_{z1}}{s\tau_3}\right)\left(\frac{K_{VCO}}{s}\right) \tag{4.7}$$

Equation (4.7) gives two poles at s=0, and the highest degree of the characteristic polynomial is two. Thus, PLL_3 is a Type II PLL having order 2. Therefore, each of the two poles is from VCO and loop filter, LF_3. Select another loop filter, LF_4 having a transfer function expressed as

$$\mathrm{Tf}_{LF4}(s) = \left(\frac{1+s\tau_{z2}}{s\tau_4}\right)\left(\frac{1}{1+s\,\tau_5}\right) = \frac{1+s\tau_{z2}}{s\tau_4+s^2\,\tau_4\tau_5} \tag{4.8}$$

The transfer function of another PLL (PLL_4) having loop filter, LF_4 can be expressed as

$$\mathrm{TF}_{PLL_4}(s) = (K_{PD})\left(\frac{1+s\tau_{z3}}{s\tau_4+s^2\,\tau_4\tau_5}\right)\left(\frac{K_{VCO}}{s}\right) \tag{4.9}$$

Equation (4.9) shows that PLL_4 has two poles at s=0 and highest degree of the characteristic equation is three. Such PLL_4 is of Type II and order 3. Likewise, another PLL (PLL_5) of Type III and of order 3 must have three integrators in the loop of the system i.e., three poles at origin (s=0) and the highest degree of the characteristic polynomial such PLL must be three. For this we have to consider a loop filter (LF_5) having transfer function expressed as

$$Tf_{LF5}(s) = \frac{(1+s\tau_{z4})(1+s\tau_{z5})}{s^2\tau_6\tau_7} \tag{4.10}$$

where $s\tau_{z4}$ and $s\tau_{z5}$, are the zeroes and $s\tau_6$ and $s\tau_7$ are the poles of LF_5. The open loop transfer function of such PLL_5 with LF_5 is expressed as

$$\mathrm{Tf}_{PLL_5}(s) = (K_{PD})\left[\frac{(1+s\tau_{z4})(1+s\tau_{z5})}{s^2\tau_6\tau_7}\right]\left(\frac{K_{VCO}}{s}\right) \tag{4.11}$$

Hence, the design approach for different Types and orders of a PLL considers the number of poles at origin, (s=0) or the total number of integrators in the control loop of a PLL which determines the Type of PLL. Moreover, the highest degree of the characteristic polynomial from the transfer function of PLL gives the order of the PLL and the general approach of any conventional PLL model can be designed using this design. Such approach creates a general model of any PLL and is shown in Fig. 4.2, where LF_1, LF_2, LF_3 are the loop filter (LF) of Type I, Type II and Type III respectively. Table 4.1 shows the five different PLLs considered according to the choice of the transfer function of the loop filter indicating the types and orders of the PLLs.

Table 4.1: Table showing the types and orders of PLLs considered along with their transfer function

PLLs	Transfer function of LFs	Transfer function of PLLs	Type	Order
PLL_1	$Tf_{LF1}(s) = \frac{1}{1+s\tau}$	$Tf_{PLL_1}(s) = \frac{(K_{PD})\,(K_{VCO})}{s(1+s\tau)}$	**I**	**2**
PLL_2	$Tf_{LF2}(s) = \left[\frac{1}{(1+s\tau_1)}\right]\left[\frac{1}{(1+s\tau_2)}\right]$	$Tf_{PLL_2}(s) = \frac{(\mathrm{K}_{PD})\,(K_{VCO})}{[s^3\tau_1\tau_2 + s^2(\tau_1+\tau_2)+s]}$	**I**	**3**
PLL_3	$\mathrm{Tf}_{LF3}(s) = \frac{1+s\tau_{z1}}{s\tau_3}$	$\mathrm{Tf}_{PLL_3} = (\mathrm{K}_{PD})\left(\frac{1+s\tau_{z1}}{s\tau_3}\right)\left(\frac{K_{VCO}}{s}\right)$	**II**	**2**
PLL_4	$\mathrm{Tf}_{LF4}(s) = \frac{1+\mathrm{s}\tau_{z2}}{\mathrm{s}\tau_4 + \mathrm{s}^2\tau_4\tau_5}$	$\mathrm{TF}_{PLL_4}(s) = (K_{PD})\left(\frac{1+\mathrm{s}\tau_{z3}}{\mathrm{s}\tau_4 + \mathrm{s}^2\tau_4\tau_5}\right)\left(\frac{K_{VCO}}{s}\right)$	**II**	**3**
PLL_5	$Tf_{LF5}(s) = \frac{(1+s\tau_{z4})(1+s\tau_{z5})}{s^2\tau_6\tau_7}$	$\mathrm{Tf}_{PLL_5}(s) = (K_{PD})\left[\frac{(1+s\tau_{z4})(1+s\tau_{z5})}{s^2\tau_6\tau_7}\right]\left(\frac{K_{VCO}}{s}\right)$	**III**	**3**

4.3 Modelling Analysis of Various Types of PLLs

The modelling for the design of three types of PLLs like (i) Type I, (ii) Type

II and (iii) Types III will be discussed in this section of the chapter. The transfer functions of each component and the open loop transfer function of the designed PLL have been developed to observe the number of poles at origin in the loop filter for defining the type of it.

4.3.1 Modelling Analysis of Type I PLL

The structural block diagram of a conventional Type I PLL is shown in Fig.4.3 (a) where the nominal frequency, calculated frequency and calculated phase angle from VCO are represented as 'ω_{nf}', 'ω_{est}' and 'θ_{est}' respectively. The calculated frequency $\omega_{est} = \omega_{nf} + \omega_{cf}$. The calculated phase angle $\theta_{est} = \omega_{nf}t + \Delta\theta_{cf}$, where '$\Delta\theta_{cf}$' is the controlled frequency. The conventional Type I PLL is characterized by the presence of only one integrator in the control loop of the system and with highest stability margin. However, during frequency alteration such PLL cannot obtain the zero average steady state phase error. Thus, in order to overcome this problem a quasi-Type I PLL which actually contains one integrator along with a low pass filter used as a loop filter (LF) with gain K_{dc} is considered as shown in Fig. 4.3 (b) [28]. A Moving Average Filter (MAF) has an exceptional filtering capacity thus, it has been used as a linear low pass filter having a dc gain K_{dc} in this chapter in the design approach. Under low frequency, MAF acts like an integrator. Under the nominal grid voltage conditions, quasi-Type I PLL uses a basic phase angle detector (PD) so that it will act as Type I PLL.

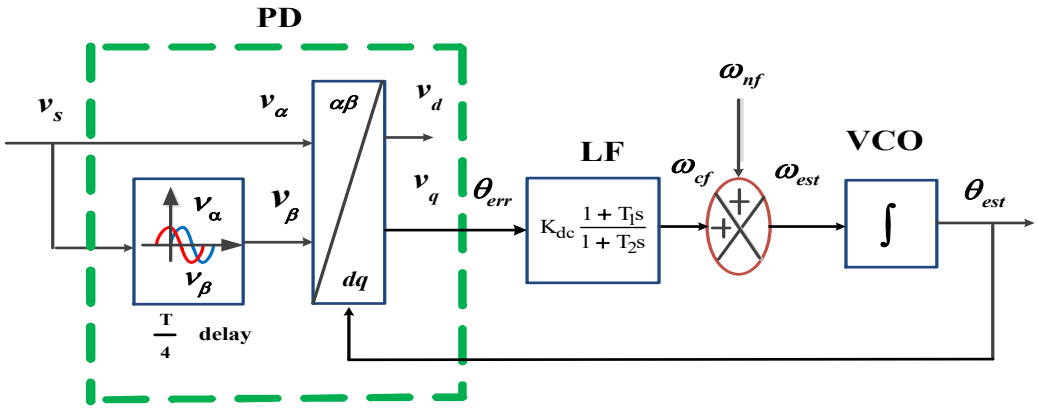


Fig. 4.3 (a) Structural block diagram of conventional Type I PLL

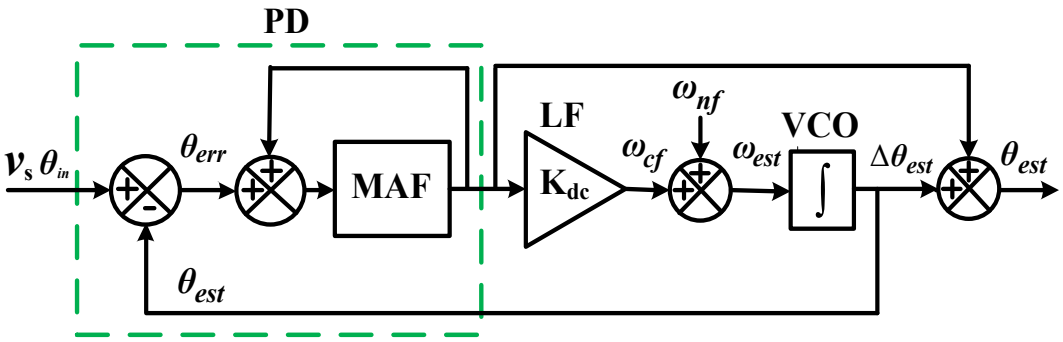


Fig. 4.3 (b) Structural block diagram of Type I PLL [41]

The grid input voltage can be expressed as

$$v_s = V_{ms} \sin \omega_{in} t = V_{ms} \sin \theta_{in} \tag{4.12}$$

The output voltage from VCO is expressed as

$$v_{out} = V_{out} \sin \omega_{out}\, t = V_{out}\ \sin \theta_{out} \tag{4.13}$$

The input and output phases will respectively have the following expression

$$\theta_{in} = \omega_f t + \int \Delta\omega_{in}(0)\, dt = \Delta\, \theta_{in} \tag{4.14}$$

$$\theta_{out} = \omega_f t + \int \Delta\, \omega_{out} dt\ = \Delta\theta_{out} \tag{4.15}$$

where ω_f, $\Delta\omega_{in}$ and $\Delta\omega_{out}$ are respectively the free running frequency of VCO, input frequency deviation and output frequency deviation with $\int \Delta\, \omega_{in}(0)dt = \Delta\, \theta_{in}$, and $\int \Delta\, \omega_{out} dt\ = \Delta\, \theta_{out}$. Under steady state condition when the phase error, θ_{err} is constant i.e., nearly zero the phase angle is locked and the input frequency is equal to the output frequency, and $\omega_{in} = \omega_{out}$. $\theta_{err} = \theta_{nf} - \theta_{est} = 0$; $\omega_{nf} = \omega_{est}$. Hence for a typical Type I PLL for a step change in phase angle and frequency, the phase error can be achieved respectively as

$$\theta_{err,s} = 0 \tag{4.16}$$

$$\theta_{err,s} = \left(\frac{\Delta\, \omega_{in}}{K_{PD} K_{VCO}}\right) \tag{4.17}$$

where K_{PD} and K_{VCO} are the proportional gains of phase detector and VCO respectively. The transfer function of MAF, a low pass filter which is used to improve the control system can be expressed in the Laplace transformation as

$$\mathrm{Tf}_{MAF}(s) = \frac{1-e^{-T_\omega s}}{T_\omega s} \tag{4.18}$$

Here 'T_ω' is the window length of MAF. By applying the first-order Pade Approximation method to the time delay, $e^{-T_\omega s}$, its transformation into Laplace domain can be expressed as

$$e^{-T_\omega s} = \frac{e^{-T_\omega \frac{s}{2}}}{e^{+T_\omega \frac{s}{2}}} \approx \frac{1-T_\omega \frac{s}{2}}{1+T_\omega \frac{s}{2}} \tag{4.19}$$

Substituting the equation (4.19) into (4.18) transfer function of MAF can be rewritten as

$$\mathrm{Tf}_{MAF} s \approx \frac{1}{\left(\frac{T_\omega}{2}s+1\right)} \tag{4.20}$$

From equation (4.20) the transfer function of MAF, can be approximated by a low pass filter which has time constant, $\frac{T_\omega}{2}$ and the behaviour of the transfer function of MAF can be modelled. The steady state phase error in such Type I PLL is linearly proportional to input frequency deviation, $\Delta\omega_{in}$. The open loop transfer function of the Type I PLL in Laplace domain can be expressed as follows [28]

$$Tf_{LGTypeI}(\mathrm{s}) = \frac{output}{error} = \frac{\theta_{est}(s)}{\theta_{in}(s)-\theta_{est}(s)} \tag{4.21}$$

$$= \left[\frac{Tf_{MAF}(s)}{1-Tf_{MAF}(s)}\right]\left[\frac{s+K_{dc}}{s}\right] \tag{4.22}$$

Putting equation (4.20) into equation (4.22) we get

$$= \left(\frac{\frac{1}{\frac{T_\omega}{2}s+1}}{1-\frac{1}{\frac{T_\omega}{2}s+1}}\right) * \left(\frac{s+K_{dc}}{\mathrm{s}}\right) = \frac{\frac{2}{T_\omega}(s+K_{dc})}{s^2} \tag{4.23}$$

Thus, equation (4.23) shows that the quasi-Type I PLL has two poles at origin as the characteristic polynomial has s^2, i.e., two roots at s=zero. Hence it is a Type II PLL by control but the structure consideration shows that it is Type I PLL. The gain K_{dc} is selected in such a way that it gives a sufficient stability margin.

4.3.2 Modelling Analysis for Type II PLL

The design and modelling of Type II PLL are characterized by the presence of two integrators in the control loop structure of the system and has two poles at origin. The structural block diagram of Type II PLL is shown in Fig. 4.4. It also represents the structure of the most commonly used conventional PLL known as Synchronous Reference Frame (SRF) PLL. The SRF PLL normally consists of a (i) phase detector (PD), (ii) proportional integral (PI) controller as the loop filter (LF) and (iii) voltage-controlled oscillator (VCO) in its structure.

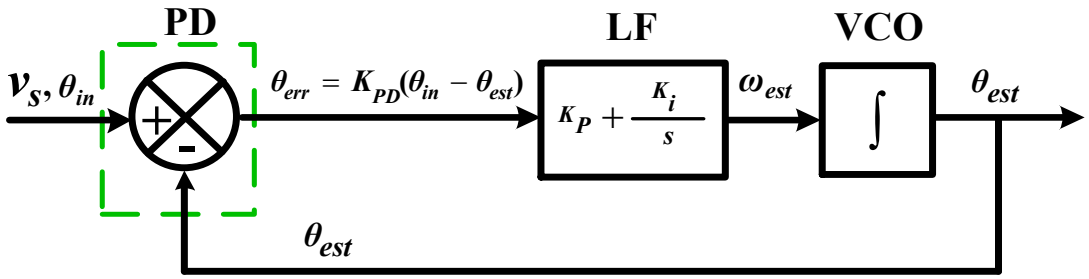


Fig. 4.4 Structural Block Diagram of Type II PLL

It is a closed-loop feedback system which is used to estimate its accurate frequency and phase angle. In the structure of SRF PLL, two integrators are present, one integrator in VCO and another integrator in the PI controller. Under balanced grid voltages, such PLL can achieve fast and accurate estimation of frequency and phase by employing a high bandwidth design. The transfer functions of the PD consist of only a gain, K_{PD}. The transfer functions of LF and VCO in the s-domain can be expressed respectively as

$$\mathrm{Tf}_{LF}(s) = \frac{K_P s + K_i}{s} \tag{4.24}$$

$$\mathrm{Tf}_{VCO}(s) = \frac{K_{VCO}}{s} \tag{4.25}$$

The open loop transfer function of Type II PLL (SRF PLL) system can be expressed as

$$\mathrm{Tf}_{LG\ Type\ II}(s) = [Tf_{PD}(s)] * [Tf_{LF}(s)] * [Tf_{VCO}(s)]$$

$$= (\mathrm{K}_{PD}) * \left(\frac{K_{p_T} s + K_i}{s}\right) * \left(\frac{K_{VCO}}{s}\right)$$

$$= \frac{(K_{PD})*(K_p s+K_i)*(K_{VCO})}{s^2} \quad (4.26)$$

Equation (4.26) shows the presence of two poles at origin (s=0) which indicates that there are two integrators in the control loop. This verifies that the SRF PLL considered is a Type II PLL both by the structure and control.

4.3.3 Modelling Analysis for Type III PLL

For modelling the design of a Type III PLL, three integrators must be considered in the loop structure of the PLL. The structural block diagram of Enhanced PLL (EPLL) is shown in Fig. 4.5. An illustrative example for the modelling analysis of design of Type III PLL is enhanced phase locked loop (EPLL) which has three loop integrators and it consists of two main loops, one for the estimation of magnitude of the grid input voltage and the other loop is the phase estimation loop which is actually a phase locked loop.

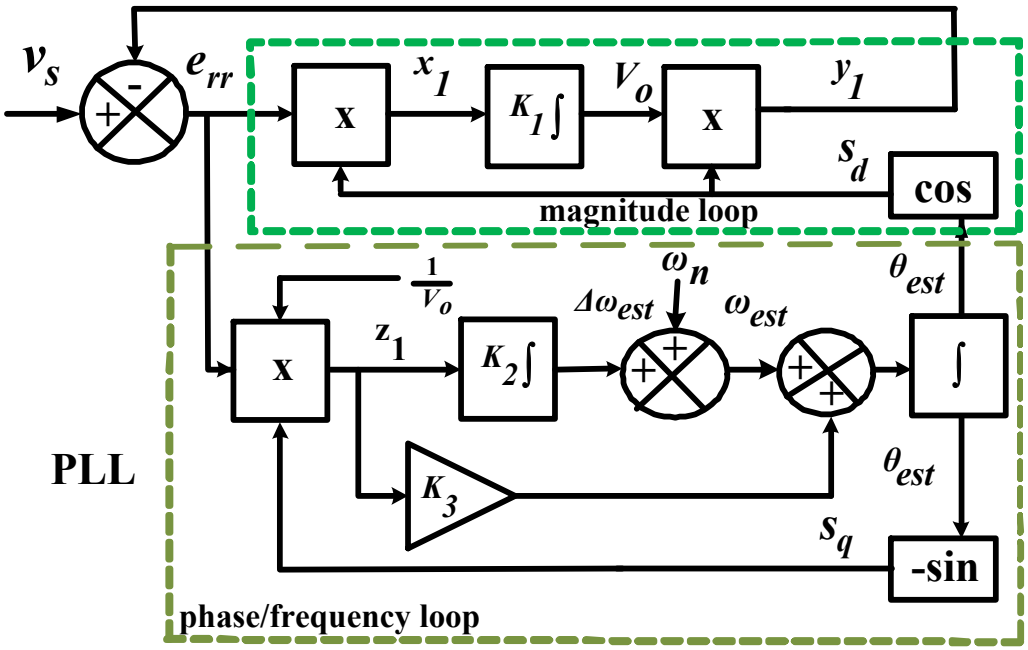


Fig. 4.5 The structural block diagram of Type III PLL (EPLL)

The voltage v_s is the grid input signal voltage which is sinusoidal in nature. 'V_o' is the estimated magnitude of input voltage. 's_d' and 's_q' are the direct and quadrature signal

in dq reference frame. The error between the reference grid input voltage signal, v_s and estimated output voltage signal, y_1 is expressed as

$$e_{rr} = v_s - y_1 \tag{4.27}$$

The estimated frequency of z_1 signal is expressed as

$$\omega_{est} = \omega_{nf} + \Delta\omega_{est} \tag{4.28}$$

where ω_{nf} is the nominal angular frequency (314rad/s) and $\Delta\omega_{est}$ is the controlled angular frequency obtained from the output of the PI controller. The output of the VCO is the estimated phase angle represented by θ_{est}. Type III PLL (EPLL), can be mathematically described by three differential equations as

$$\dot{V_o} = K_1\, e_{rr} cos\, \theta_{est} \tag{4.29}$$

$$\dot{\omega_{est}} = K_2 e_{rr}\, cos\, \theta_{est} \tag{4.30}$$

$$\dot{\theta_{est}} = \omega_n + \Delta\omega_{est} + K_3\, e_{rr}\, sin\, \theta_{est} \tag{4.31}$$

The gains in the loop system like K_1, K_2, and K_3 are the positive value parameters which directly affect the performance of EPLL. The values of these parameters are selected [112] as $K_1 = K_3 = K = \mu\omega_n$ and $K_2 = \frac{K^2}{8}$ and this is obtained by taking damping ratio of unity for their transfer function. K is selected as K=$\sqrt{2}$ within the recommended range $0.5 \leq K \leq 1.5$ The output of the PD with a simple proportional gain and the output of LF acting as PI controller are summed up. Hence the open loop transfer function of EPLL can be expressed as

$$Tf_{LG}(s) = \frac{\theta_{est}}{\theta_{err}} = \frac{y_1}{e_{rr}} \tag{4.32}$$

$$= Tf_{PD}(s) * Tf_{PLL}(s) \tag{4.33}$$

$$= \frac{(K_1+K_3)s^2+(K_2+K_3K_1)s+K_1K_2}{s^3} \tag{4.34}$$

The equation (4.34) indicates that the open loop transfer function of EPLL has three poles at $s = 0$, at the characteristic polynomial. This shows that the illustrative PLL (EPLL) is a Type III PLL as it has three integrators in the system loop.

4.4 Stability Analysis of PLLs

Stability is a very important factor in design of any system. Hence in a PLL design, the stability analysis also plays an important role in ensuring that the PLL acquires smooth locking and it remains locked despite the presence of noise and

disturbances in the input. Stability is analyzed for a linear steady state model and transfer functions like open loop, closed loop and error transfer functions are developed from it. Stability analysis in PLL design is conducted using open-loop characteristics, although the manifestation of stability is evident in the structural properties of the closed-loop response. The stability of Type I, Type II, Type III PLLs is analyzed through Bode plots which is the most common and intuitive method for stability analysis. It displays the magnitude (in dB) and phase (in degrees) versus frequency of the open

loop transfer functions for the respective PLL. A positive Gain Margin (GM) and Phase Margin (PM) are essential for stability of a system. GM and PM are calculated by examining the interaction between the gain and phase plots at their phase crossover frequency (where the phase is -180°) and gain crossover frequency (where the gain is 0 dB). A feedback control system is stable if both PM and GM are positive and unstable if negative at their respective cross over frequencies.

Table 4.2: Interpretation of stability for different values of PM

Sl. No.	**Range of PM value**	**Interpretation**
1.	PM > 45°	Good stability, well-damped response
2.	PM ≈ 0°	Marginally stable
3.	PM < 0°	Unstable system

Table 4.2 shows the interpretation of the stability ~~at~~ for different values of PM. The phase response of open loop in Laplace domain (s-domain) remains unaffected by variations in the phase detector or voltage-controlled oscillator gains. The phase margin (PM, $\emptyset_{\mathrm{M}}$) in radians with ω_{gc} as the phase crossover frequency and the gain margin (GM) in dB with ω_{π} as the gain crossover frequency of the open loop system can be expressed respectively as

$$\text{Phase margin, PM}, \emptyset_{\mathrm{M}} = \mathrm{Arg}\left[\mathrm{Tf}_{LG}\left(\mathrm{j}\omega_{\mathrm{gc}}\right)\right] + 180^{0} \tag{4.35}$$

$$\text{Gain margin, GM}, \mathrm{gm} = -20\log|\mathrm{LG}(\mathrm{j}\omega_{\pi})| \tag{4.36}$$

The phase margin in a PLL is not only used for analyzing the stability of the system but also for suggesting modification in the design of the PLL. The stability of Type I, Type II and Type III PLLs is analyzed by considering the open loop transfer function given in equations (4.23), (4.26) and (4.34) and deciding the optimized parameters.

4.4.1 Stability Analysis of Type I PLL

The Bode plot of Type I PLL is plotted which is shown in Fig. 4.6, by considering the optimized gain and window length as $K_p = 92.34$ and $T_w = 0.01$ms [52]. It gives a GM of 37.8 dB with a frequency crossover of 594 rad/s and a PM of 45^0 at 206 rad/s. Since both GM and PM are positive at their respective crossover frequencies Type I PLL is stable.

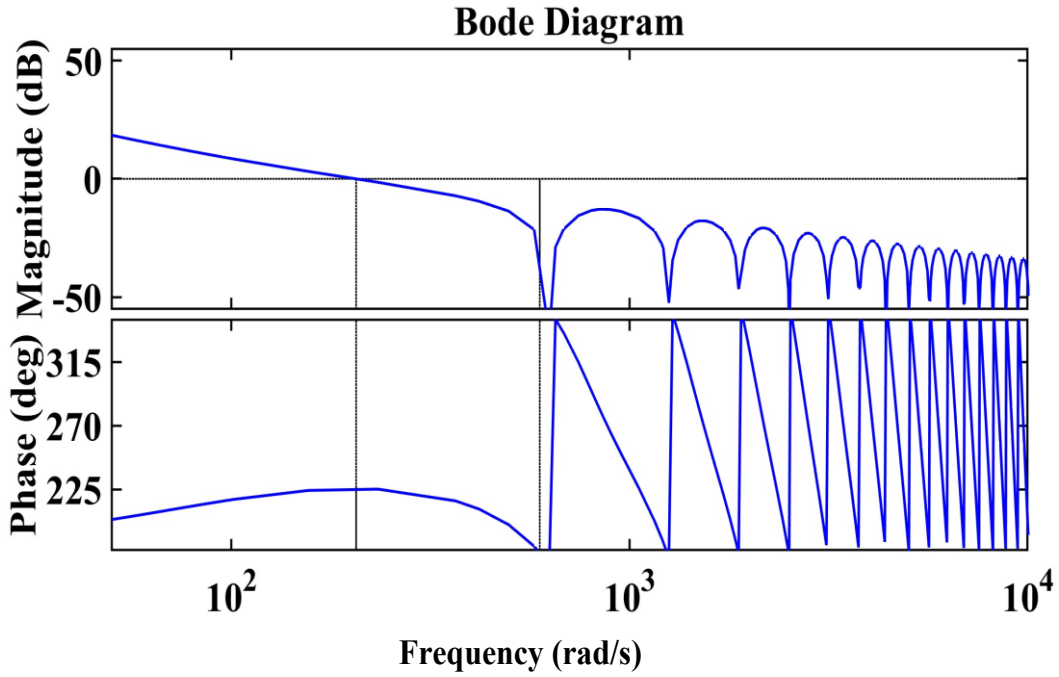


Fig. 4.6 Bode plot of open loop transfer function of Type I PLL

4.4.2 Stability Analysis of Type II PLL

The Bode plot of Type II is drawn as shown in Fig. 4.7 by considering the optimized parameter values $K_p = 7.8$, $K_i = 85.05$ and damping ratio= 0.707. It shows a gain margin (GM) of infinity at zero rad/s and the phase margin (PM) of 45.2° with a cross-over frequency of 11 rad/s. Therefore, it depicts that the considered Type II PLL design is stable.

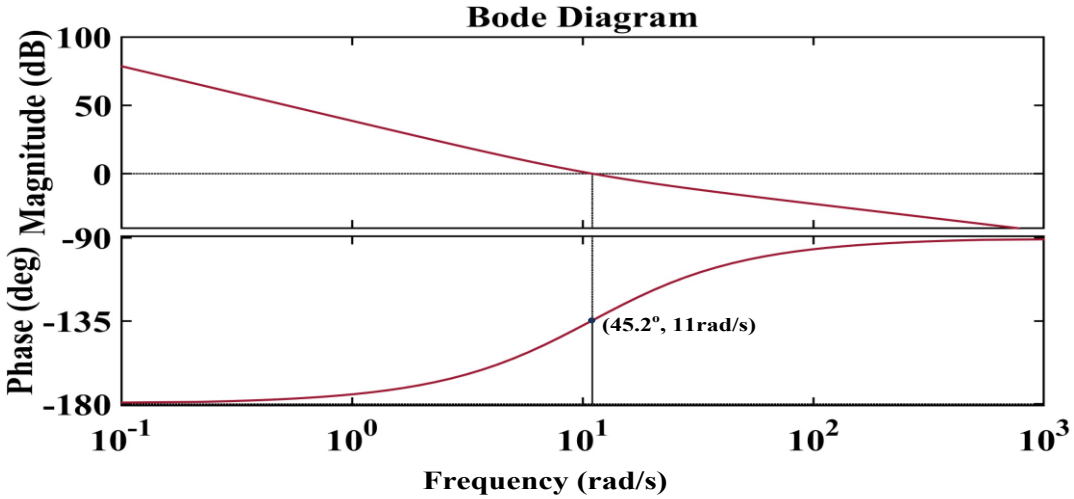


Fig. 4.7 Bode plot of the open loop transfer function of Type II PLL

4.4.3 Stability Analysis of Type III PLL

Similarly, the Bode plot of Type III PLL is plotted as shown in Fig. 4.8 considering the optimised parameters like K_1=K_3 = K, $K_2 = \frac{K^2}{8}$ and K is selected as K=$\sqrt{2}$ within the recommended range of $0.5 \leq K \leq 1.5$. K_1=K_2 = K_3. The bode plot shown in Fig. 4.8 depicts that the gain margin is infinite dB at zero rad/s and phase margin is 74.4^0 at 2.89 rad/s indicating that Type III PLL modelled is stable.

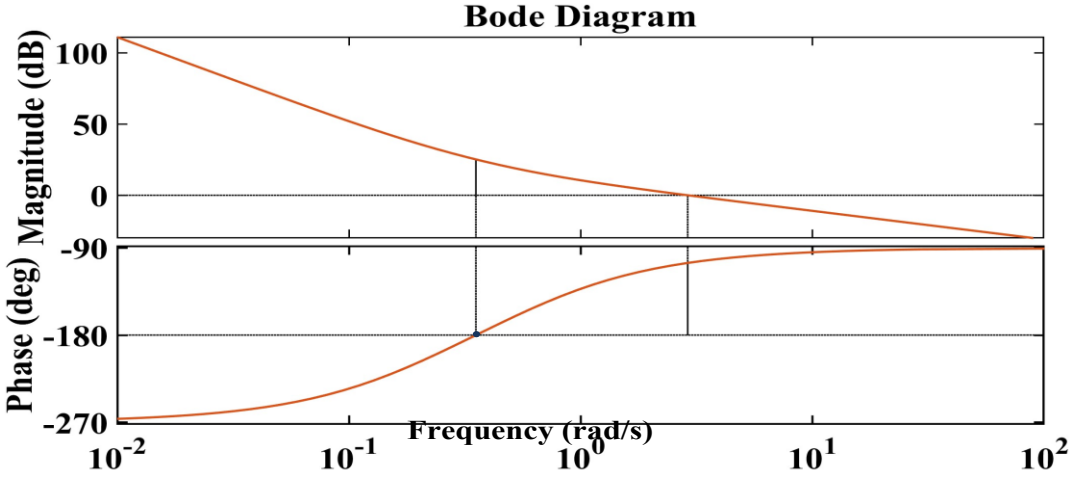


Fig. 4.8 Bode plot of the open loop transfer function of Type III PLL

4.4.4 Interpretation of the Stability Analysis of three Types of PLLs

Table 4.3 depicts the summary showing the optimized parameters that are chosen for the three types of PLLs and the calculated GM and PM from their respective Bode

Plots along with the interpretation of the results. It is observed that the values of the GMs and PMs of Type I PLL (GM=37.8 dB, PM=45°), Type II PLL (GM= infinite dB, PM= 45.2°) and Type III PLL (GM= infinite dB, PM=74.4°) are positive at their respective cross over frequencies. This shows that the three types of PLLs are all stable under dynamic steady state conditions. Moreover, the gain margin of Type II and Type III PLLs is found to be infinite interpreting that these systems have absolute stability. Therefore, the three types of PLLs are stable under dynamic conditions considered and the optimized parameters taken from literature.

Table 4.3 Interpretation of the three types of the PLLs

Sl. No.	**PLL type**	**Parameters**	**GM (in dB)**	**PM (in rad/s)**	**Interpretation**
1.	Type I PLL	$K_p = 92.34, T_w = 0.01$	GM=37.8 dB at crossover frequency of 594 rad/s	PM=45° at cross over frequency of 206 rad/s	Stable
2.	Type II PLL (SRF PLL)	$K_p = 7.8, K_i = 85.05$, damping ratio= 0.707	GM= infinity at cross over frequency of zero rad/s	PM= 45.2° with a cross-over frequency of 11 rad/s	Absolutely stable
3.	Type III PLL (EPLL)	$K_1=K_3 = K$, $K_2 = \frac{K^2}{8}$, K=0.5	GM= infinite dB at crossover frequency of zero rad/s	PM=74.4° at crossover frequency of 2.89 rad/s	Absolutely stable

4.5 Performance Analysis of Different Types of PLLs

The dynamic performance analysis of Type I, Type II and Type III PLLs under various grid abnormal conditions like (i) 30% voltage sag (ii) 35% voltage swell, (iii) polluted grid, (iv) +5Hz frequency jump, (v) 30° phase shift and (vi) 20% dc -offset is performed through simulation results and verified by hardware results. The simulation is done in MATLAB Simulink environment. The disturbance due to grid abnormalities

is injected from time duration of 0.2s-0.4s. The sampling time is considered as Ts=50e-6s with run time of 1s.-The parameters selected for simulation results are mentioned in the Table 4.4.

Table 4.4 Values of the parameters chosen for the three PLLs

Sl. No.	Types of PLL	parameters selected
1.	All Types	V_{RMS} = 230 V, V_{peak} = 325V f = 50Hz
3.	Type I	$K_p = 92.34, T_w = 0.01$
4.	Type II	$K_p = 7.8, K_i = 85.05,$ damping ratio= 0.707
5.	Type III	K_1=K_3 = K, $K_2 = \frac{K^2}{8}$, K=0.5

The hardware results showing performance of the three Types of PLLs p are obtained by setting up a laboratory prototype environment as shown in Fig. 4.9 to validate the simulation results under various cases. A single-phase programmable supply of GwinSTEK model (APS-1102A) is used for generating different types of voltage signal waveforms like ~~simple~~ pure sinusoidal waveform, waveform with 10% of the 3rd and 5th harmonics induced to simulate the polluted environment and other dynamics in the voltage.

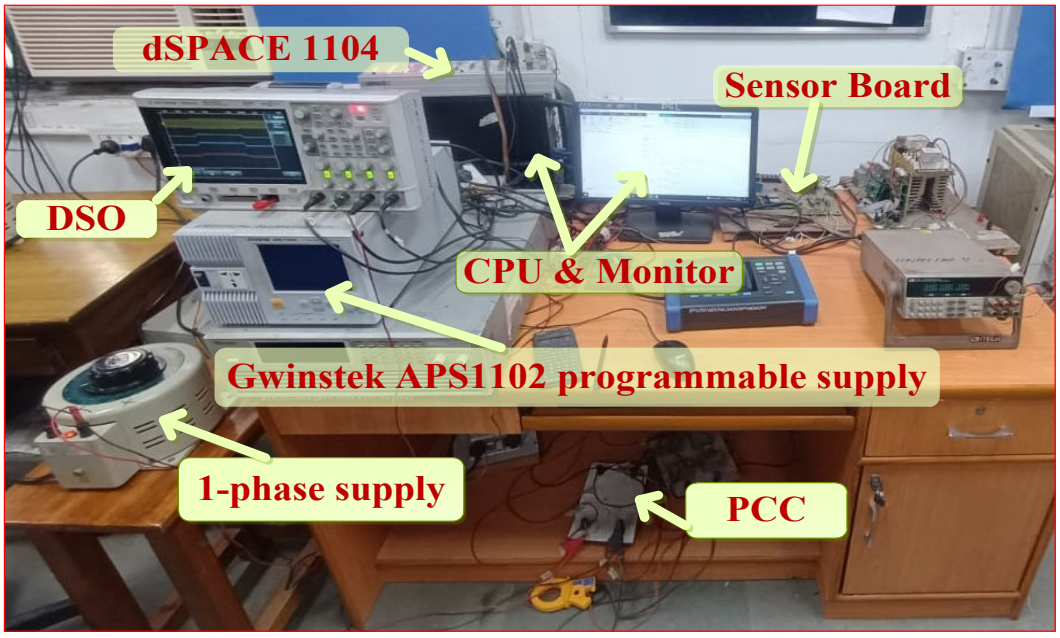


Fig. 4.9 Photograph of the hardware setup for analysing the dynamic performance of different PLLs

The input grid voltage has been sensed using a Hall effect voltage sensor and this signal is passed to the dSpace 1104 controller for processing the algorithm through the Analog to Digital Converter (ADC) channel of dSpace. The estimated signals (frequency, theta etc) from Digital to Analog Converter (DAC) channels through DSO are analyzed under different cases of non-ideal grid conditions. The sampling time is taken as Ts=100e-6s and the input voltage, v_s is taken as 100V with fundamental frequency as 50Hz.

4.5.1 Simulation and Experimental Analysis of Type I PLL under Grid Abnormalities

The simulation results depicting the signal response of source voltage v_s (volts), fundamental frequency of PLL (Hz), estimated phase angle (radians) and the amplitude of the source voltage (volts) of the dynamic performance of Type I PLL under various

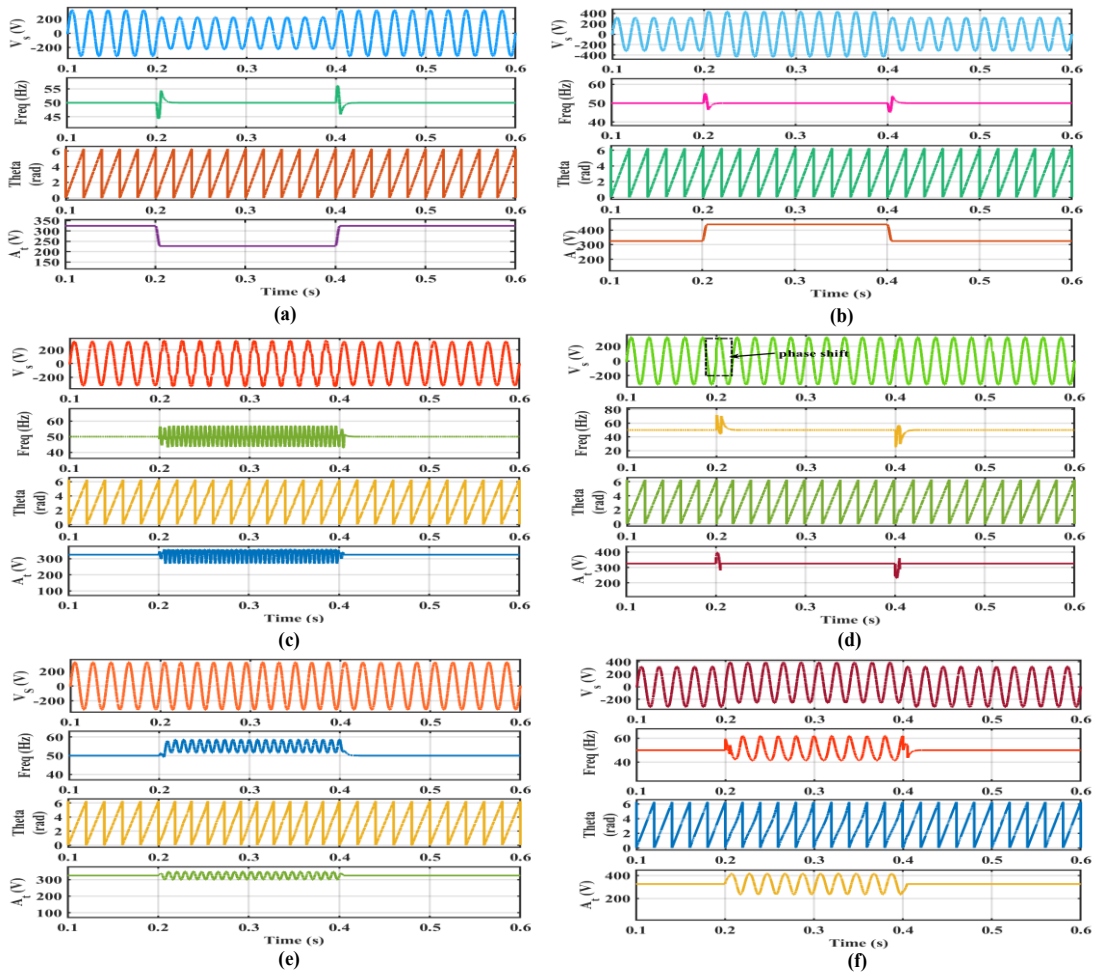


Fig. 4.10 Simulation results of Type I PLL under grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30° phase shift, (e) +5Hz frequency change, (f) 20% dc-offset

abnormal grid conditions like (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30° phase shift, (e) +5Hz frequency change, (f) 20% dc-offset are shown in Fig. 4.10. The grid abnormalities are simulated for time period of 0.2s-0.4s.

Fig. 4.10 (a) shows response under 30% grid voltage sag of Type I PLL. The response shows simulated 30% voltage drop from 0.2s to 0.4s in v_s and A_t plots. The frequency response shows peak overshoot of 54.11 Hz when the sag is initiated. The estimated frequency settles down to 50Hz within 2 cycles. Fig. 4.10 (b) shows the response under 35% swell in grid voltage. The frequency response depicts an overshoot of 55.2Hz which settles down within 1 cycle. Fig. 4.10 (c) shows the polluted grid voltage and frequency response shows oscillations during 0.2s to 0.4s with a peak of 56.81Hz. Moreover, amplitude response of voltage source also shows oscillation during disturbance period. The 30° phase shift response is simulated as shown in Fig. 4.10 (d) and it shows an overshoot of 70.7 Hz frequency response which settles down within 2 cycles. Distortion is also seen in phase angle, and amplitude of the source voltage. Fig. 4.10 (e) shows response of +5 Hz step frequency change which is oscillating with a peak of 58.61 Hz. The voltage magnitude A_t is also observed to be oscillating during the 0.2s to 0.4s. Fig. 4.10 (f) shows response under 20% DC offset in grid voltage. The frequency and amplitude of source voltage responses show oscillations during interval 0.2s to 0.4s.

Fig. 4.11 shows the experimental results of the dynamic performance of a single-phase Type I PLL under various abnormal grid conditions. The experimental plot depicts the signal response of source voltage v_s (volts), frequency of PLL (Hz), estimated phase angle (radians) and the amplitude of the source voltage (volts). Fig. 4.11 (a) shows response under 30% grid voltage sag and it depicts a sudden rise in estimated frequency response which recovers to its normal position in around 2cycles validating the simulated results of Fig.4.10 (a). Fig. 4.11 (b) shows the simulated results of the PLL under 35% swell in grid voltage. It shows an overshoot in frequency response but it settles down quickly under 1 cycle; this also validates the simulated results of Fig. 4.10(b). Fig. 4.11(c) shows responses under polluted grid voltage disturbances. The

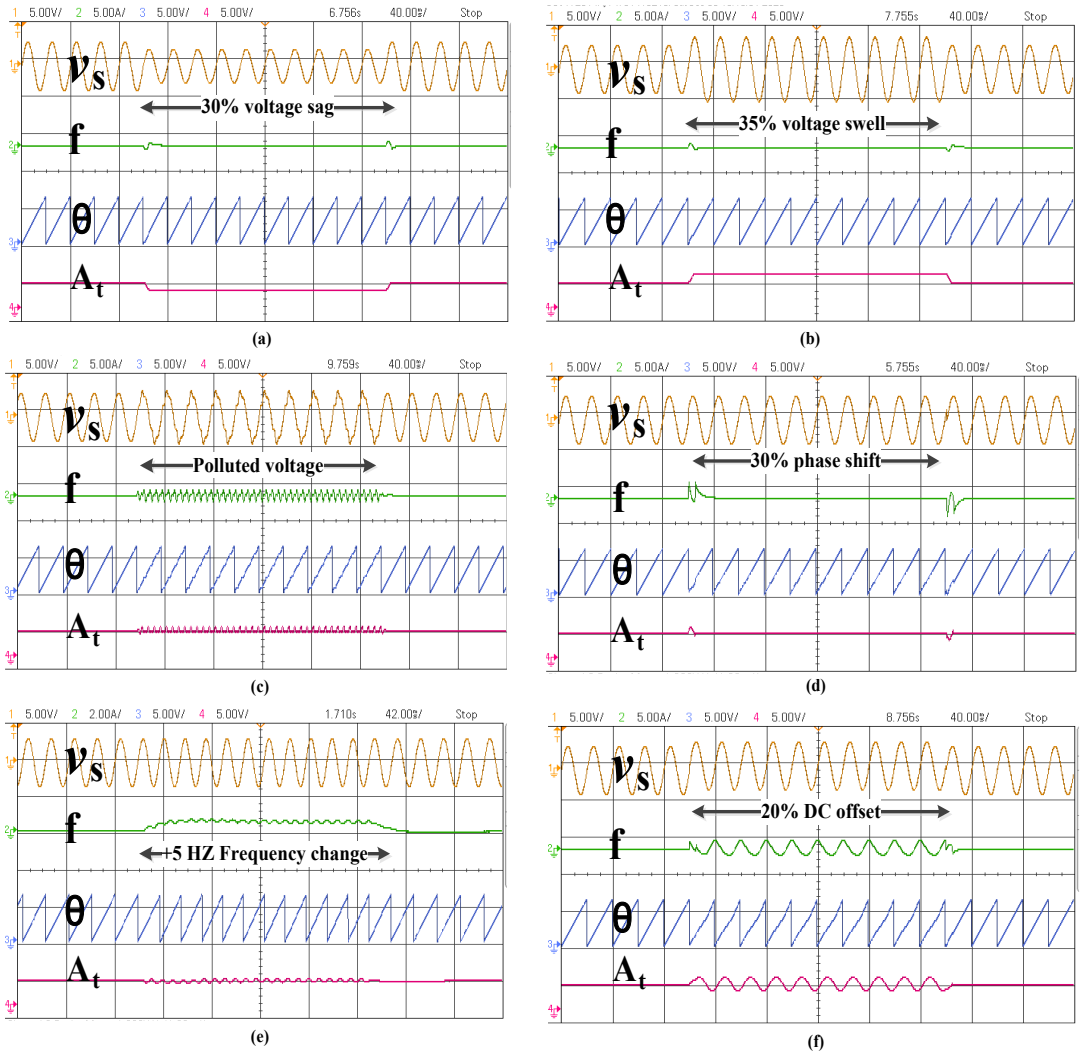


Fig. 4.11 Experimental results of Type I PLL at grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30o phase shift, (e) +5Hz frequency change, (f) 20% dc-offset

frequency and magnitude responses show oscillations during the entire disturbance period which validates the simulated results of Fig. 4.10 (c). The responses under 30° phase shift are shown in Fig. 4.11 (d). Frequency response depicts an oscillation which settles down within 2 cycles. Fig. 4.11 (e) shows response under +5 Hz frequency step change. The frequency and magnitude of source voltage responses show small oscillations during the disturbance period. The phase angle and source voltages remain unchanged and these responses validate the simulated responses of Fig. 4.10 (e). The presence of 20% DC offset in grid voltage is shown in Fig. 4.11 (f). The tracked frequency and amplitude of source voltage remains oscillating during the disturbance interval validating its simulation responses in Fig. 4.10 (f).

4.5.2 Simulation and Experimental Analysis of Type II PLL under Grid Abnormalities

The simulation results for the dynamic performance of a single-phase Type II PLL under various abnormal grid conditions are shown in Fig. 4.12. The grid disturbances are fed for time duration of 0.2s-0.4s with sampling time, Ts=50µs. The

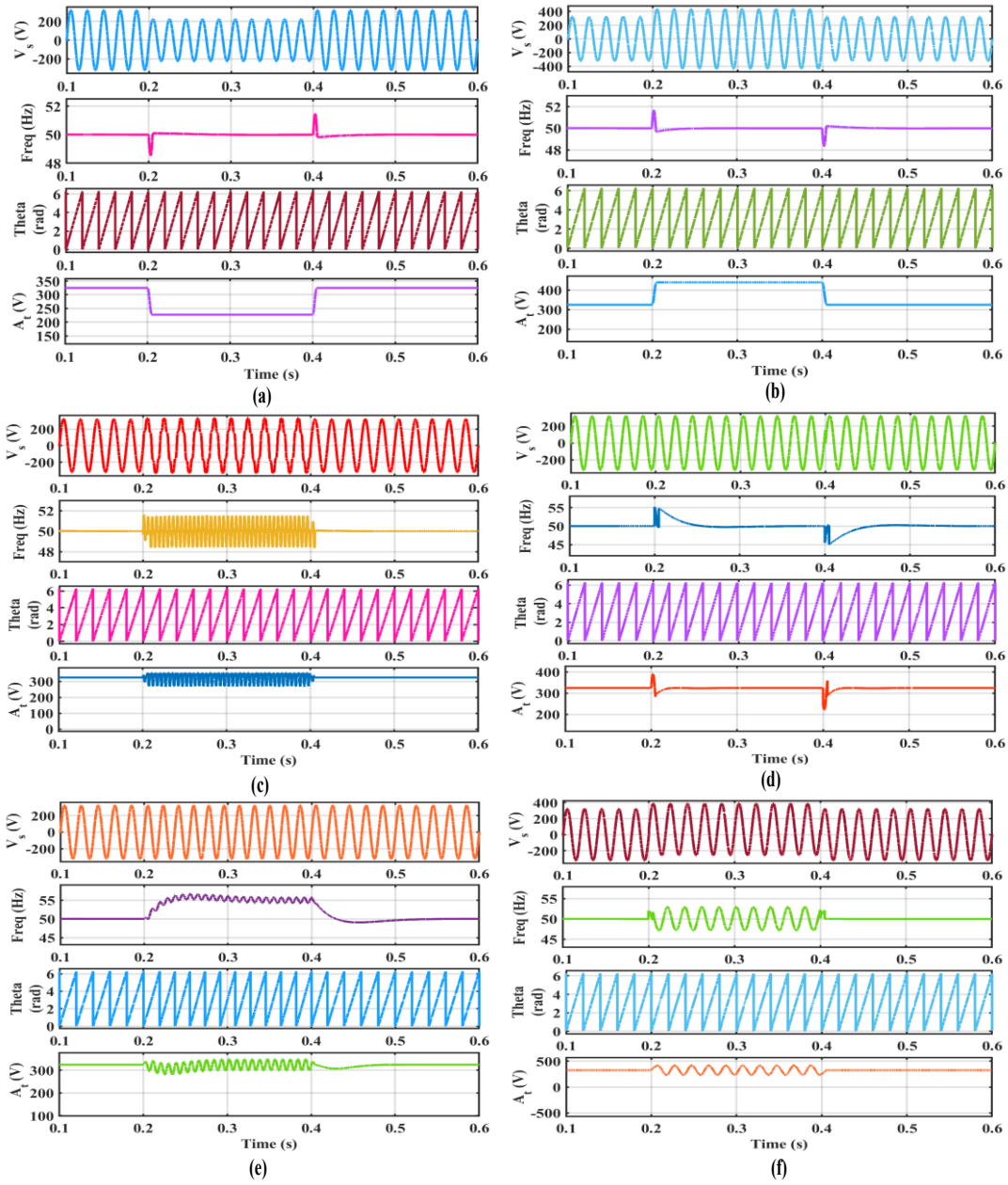


Fig. 4.12 Simulation results of Type II PLL at grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30° phase shift, (e) +5Hz frequency change, (f) 20% dc-offset

simulation plots contain the information of source voltage v_s (volts), fundamental frequency of PLL (Hz), estimated phase angle (radians) and the amplitude of the source voltage (volts). Fig. 4.12 (a) shows the simulation response under 30% grid voltage sag. The frequency response depicts a drop in voltage of 48.52Hz at the instant voltage sag is introduced. However, it recovers to its normal position within two cycles. Fig. 4.12 (b) shows the simulated results of the PLL under 35% grid voltage swell. Frequency response shows peak overshoot of 51.65Hz and it comes to normal 50Hz within two cycle. Fig. 4.12 (c) depicts the result test under polluted grid voltage. The frequency response shows continuous oscillations having a peak of about 51.41Hz during the disturbance period (0.2s to 0.4s). During the disturbance period, oscillations in the amplitude of the source voltage are also noticed. The performance of Type II PLL under 30^o phase shift is shown in Fig. 4.12 (d). It shows an overshoot of 55.03 Hz frequency response and settles down within 4 cycles. An overshoot in amplitude of the source voltage is also observed which settles to normalcy under 3 cycles after disturbance. Fig. 4.12 (e) shows responses under +5 Hz frequency step change but is oscillating giving a peak of 56.65 Hz. The oscillating source voltage magnitude is seen during the disturbed time interval. The phase angle and source voltages remain unchanged. The presence of 20% DC offset in grid voltage is shown in Fig. 4.12 (f). The frequency and amplitude of source voltage remains oscillating during the disturbance time interval. The peak of the estimated frequency is 52.99Hz. The estimated phase angle under this disturbance remains unchanged.

Fig. 4.13 shows the experimental results of the dynamic performance of a single-phase Type II PLL under various abnormal grid conditions. The experimental plot depicts the signal response of source voltage v_s (volts), frequency of PLL (Hz), estimated phase angle (radians) and the amplitude of the source voltage (volts). Fig. 4.13 (a) shows the experimental results under 30% grid voltage sag. It depicts a drop in frequency response. However, it recovers to its normal position after two cycles validating the simulated results obtained in Fig.4.12 (a). Fig. 4.13 (b) shows the experimental results of the Type II PLL under 35% swell in grid voltage. At the instant of disturbance, it shows overshoot in frequency response but it settles down after sometime very quickly in two cycles; This also validates the simulated results of Fig.

4.12 (b). Fig. 4.13 (c) shows the experimental responses under polluted grid voltage disturbance. The frequency response and the magnitude responses show oscillations during the entire disturbance period validating the simulated results in Fig.4.12 (c). Fig. 4.13 (d) shows the experimental responses under 30° phase shift. The frequency and source voltage magnitude response depicts overshoots. The overshoot in frequency response comes to normalcy after four cycles. Fig. 4.13 (e) shows responses under +5 Hz frequency step change; The frequency and the magnitude of source voltage show oscillation during disturbance period. The phase angle and source voltages remain unchanged and these responses validate the simulated responses of

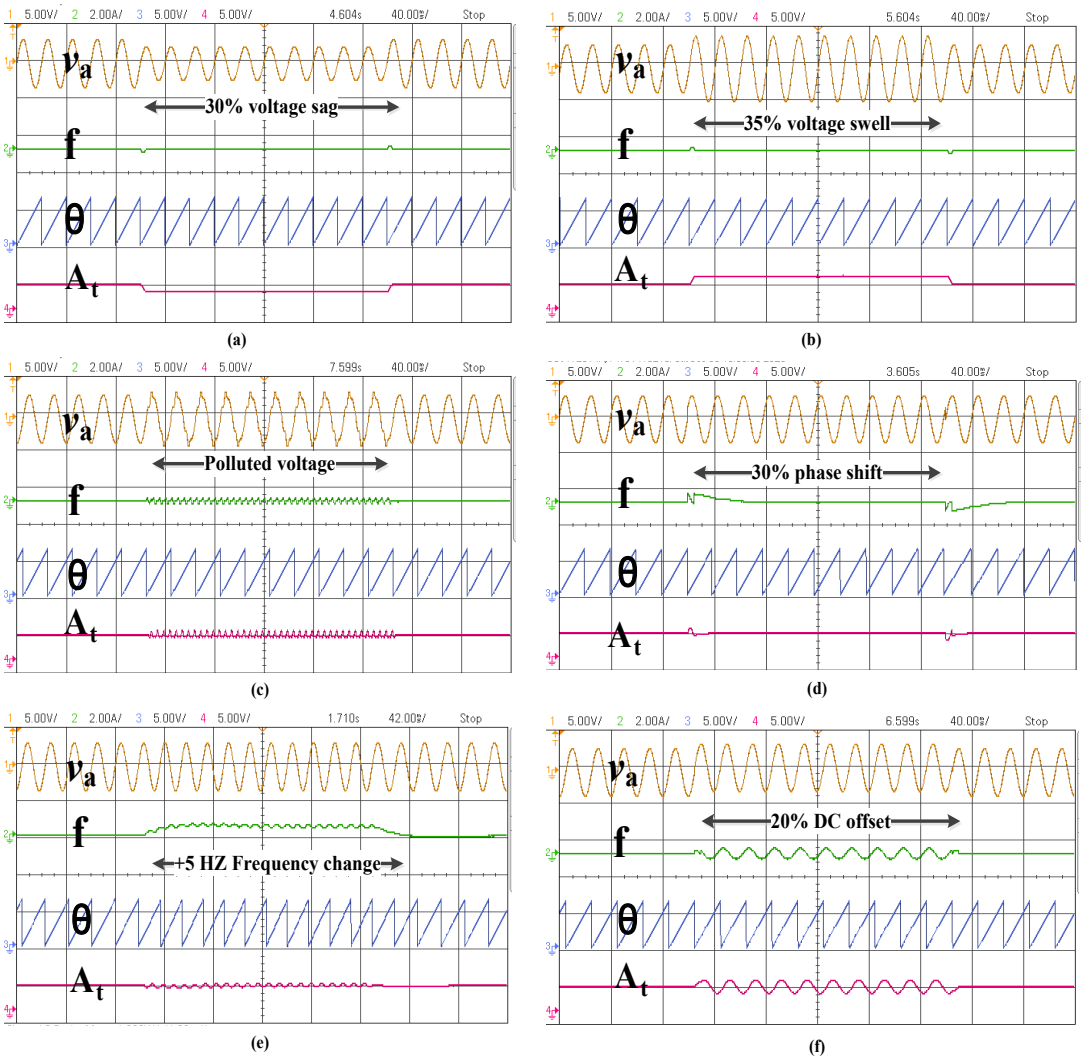


Fig. 4.13 Experimental results of Type II PLL at grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30° phase shift, (e) +5Hz frequency change, (f) 20% dc-offset

Fig. 4.12 (e). The presence of 20% DC offset disturbance in grid voltage is shown in Fig. 4.13 (f). The frequency and the magnitude of voltage source responses show oscillating response during the disturbed interval validating the simulated results of Fig. 4.12 (f).

4.5.3 Simulation and Experimental Analysis of Type III PLL under Grid Abnormalities

Fig. 4.14 shows the simulation results of dynamic performance of a single-phase Type III PLL under various abnormal grid conditions. The simulation responses give the information of source voltage v_s (volts), fundamental frequency of PLL (Hz), estimated phase angle (radians) and the amplitude of the source voltage (volts). Fig. 4.14 (a) shows the simulation. results under 30% sag in grid voltage. The voltage source and its magnitude show 30% voltage dip. The frequency response does not show any significant change, only minor oscillations. Fig. 4.14 (b) shows the simulation response of the Type III PLL under 35% grid voltage swell frequency response does not show significant change and remains almost 50Hz. The voltage and its magnitude depict the swell in their responses. Fig. 4.14 (c) is the simulation responses under polluted grid voltage disturbance. The frequency response is oscillating but of very small magnitude. The magnitude of the voltage source is oscillating during disturbance period. Type III PLL under 30^o phase shift is shown in Fig. 4.14 (d). It shows an overshoot of 51.72 Hz in frequency response but settles down within 5 cycles. Overshoot in the amplitude of the source voltage is also seen which dies down within 1 cycle. Fig. 4.14 (e) shows the response of +5 Hz frequency step change. The magnitude of source voltage is also oscillating during the disturbed time interval. The phase angle and source voltages remain unchanged. The presence of 20% DC offset in grid voltage is seen in Fig. 4.14 (f). The frequency response shows tracked distortion and computed amplitude of source voltage remains oscillating during the disturbance.

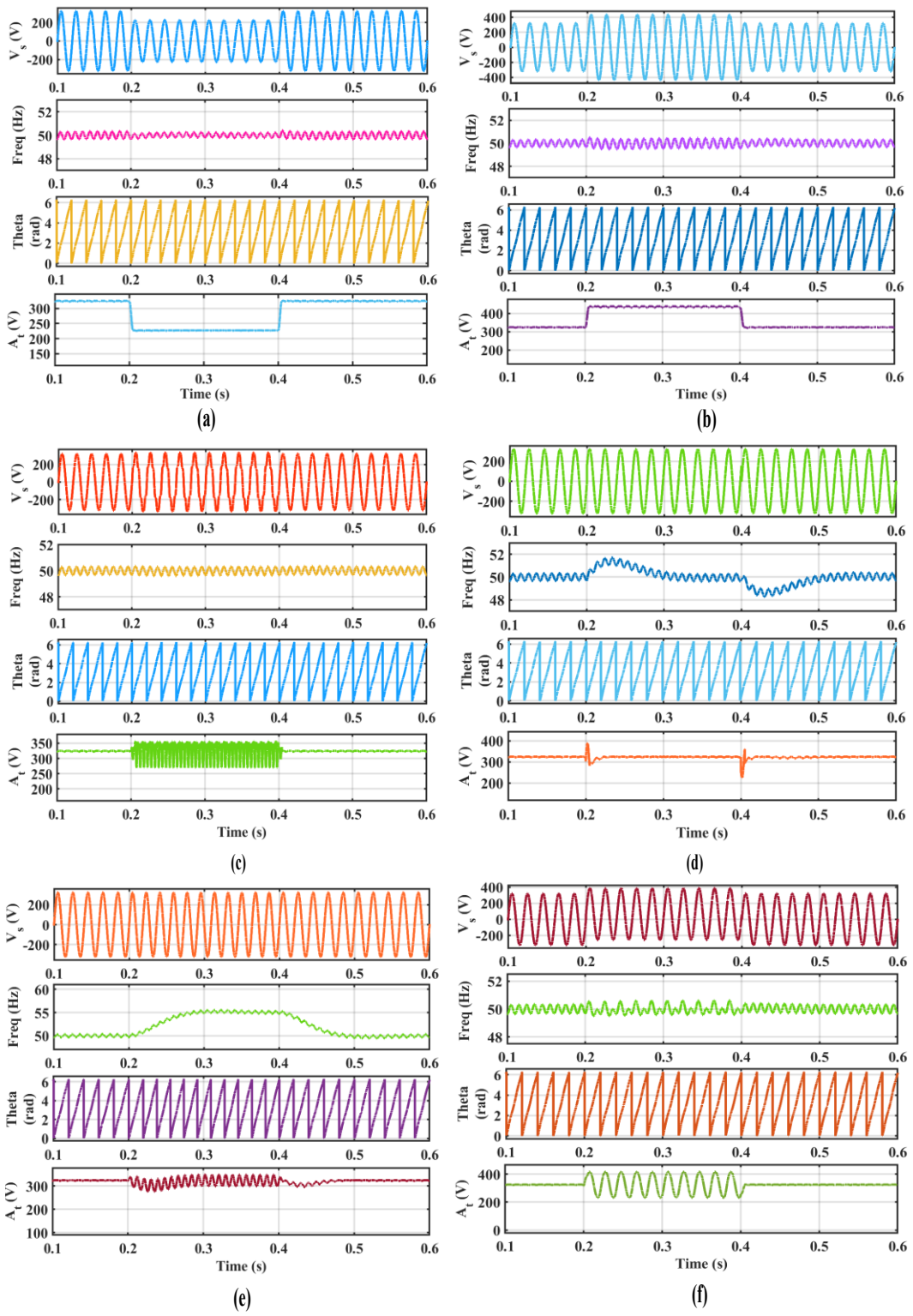


Fig. 4.14 Simulation results of Type III PLL at grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30° phase shift, (e) +5Hz frequency change, (f) 20% dc-offset

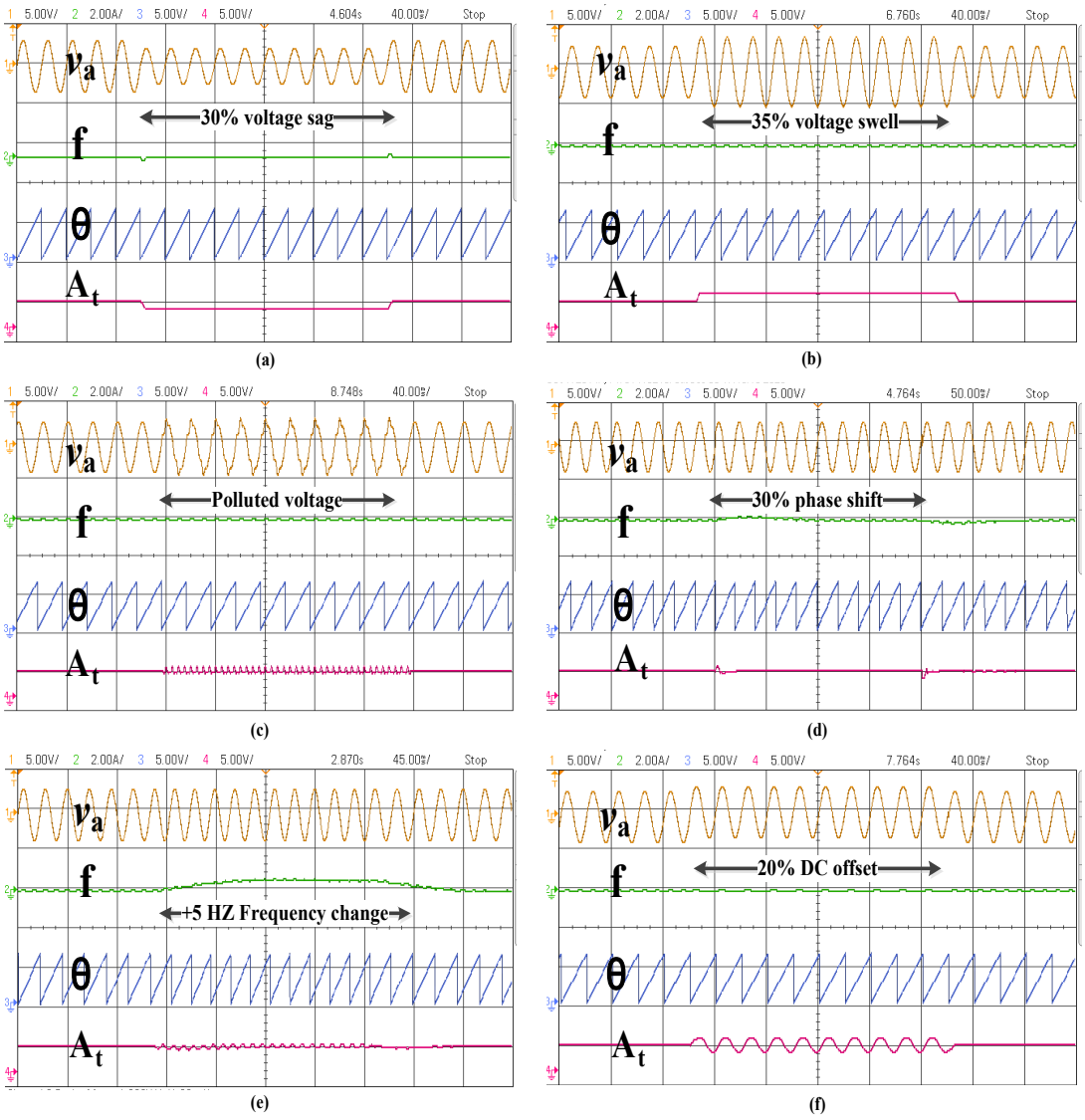


Fig. 4.15 Experimental results of Type III PLL at grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30o phase shift, (e) +5Hz frequency change, (f) 20% dc-offset

Fig. 4.15 shows the experimental results of the dynamic performance of a single-phase Type III PLL under various abnormal grid conditions. For experimental testing a peak voltage of $v_s = 325\text{V}$ peak is taken as source voltage. The experimental plot depicts the signal response of source voltage v_s (volts), frequency of PLL (Hz), estimated phase angle (radians) and the amplitude of the source voltage (volts). Fig. 4.15 (a) shows that the experimental results under 30% grid voltage sag. It depicts that at 30% voltage drop introduction the frequency response shows negligible change. Fig. 4.15 (b) shows the experimental results of the Type III PLL under 35% grid voltage swell. The frequency response remains same at 50Hz with slight oscillation; This validates

the simulated results of Fig. 4.14 (b). Fig. 4.15 (c) is the result of simulation under polluted grid voltage disturbance. The frequency response show +5Hz change while the magnitude of the estimated source voltage shows oscillations during disturbed interval validating its simulated results of Fig.4.14 (c). Performance of Type III PLL under 30^{o} phase shift is shown in Fig. 4.15 (d). It shows overshoot in frequency response but settles down in sufficient time. Fig. 4.13 (e) shows that experimental results under +5 Hz step frequency change; the frequency response shows +5 Hz change and magnitude of source voltage is distorted during 0.2s to 0.4s. The phase angle and source voltages remain unchanged validating the simulated responses. The presence of 20% DC offset in grid voltage is shown in Fig. 4.15 (f). The estimated frequency and magnitude of voltage source show oscillations during the disturbed interval time and it validates the simulated results of Fig. 4.14 (f).

4.5.4 Comparative Performance Analysis of Different Types of PLLs under Grid Abnormalities

The comparative analysis of the dynamic performance of Type I, Type II, Type III PLL is analyzed through simulation and experimental responses obtained under various grid abnormalities like (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30^{o} phase shift, (e) +5Hz frequency change, (f) 20% dc-offset are shown in Fig. 4.16 and Fig. 4.17 respectively. Fig. 4.16 (a) shows the comparative simulation analysis of Type I, II and III PLLs under 30% grid voltage sag disturbances. Type I PLL shows an overshoot of 54.22 Hz while Type III PLL shows almost no undershoot or overshoot in frequency response. For Type II PLL, the frequency response shows a drop after of 30% voltage sag disturbance. Fig. 4.16 (b) shows the comparative simulation analysis of Type I, II and III PLLs under 35% grid voltage swell disturbances. It shows that Type I PLL shows an overshoot of 55.2 Hz, Type II has an overshoot of 51.68 Hz, while Type III PLL remains constant at 50Hz with minor oscillatory nature and not significant change in frequency response. Fig. 4.16 (c) shows the comparative simulation analysis of Type I, II and III PLLs under polluted grid voltage sag disturbances. Type I PLL shows the oscillatory frequency response with overshoot of 56.56 Hz, Type II shows overshoot of 51.94 Hz while Type

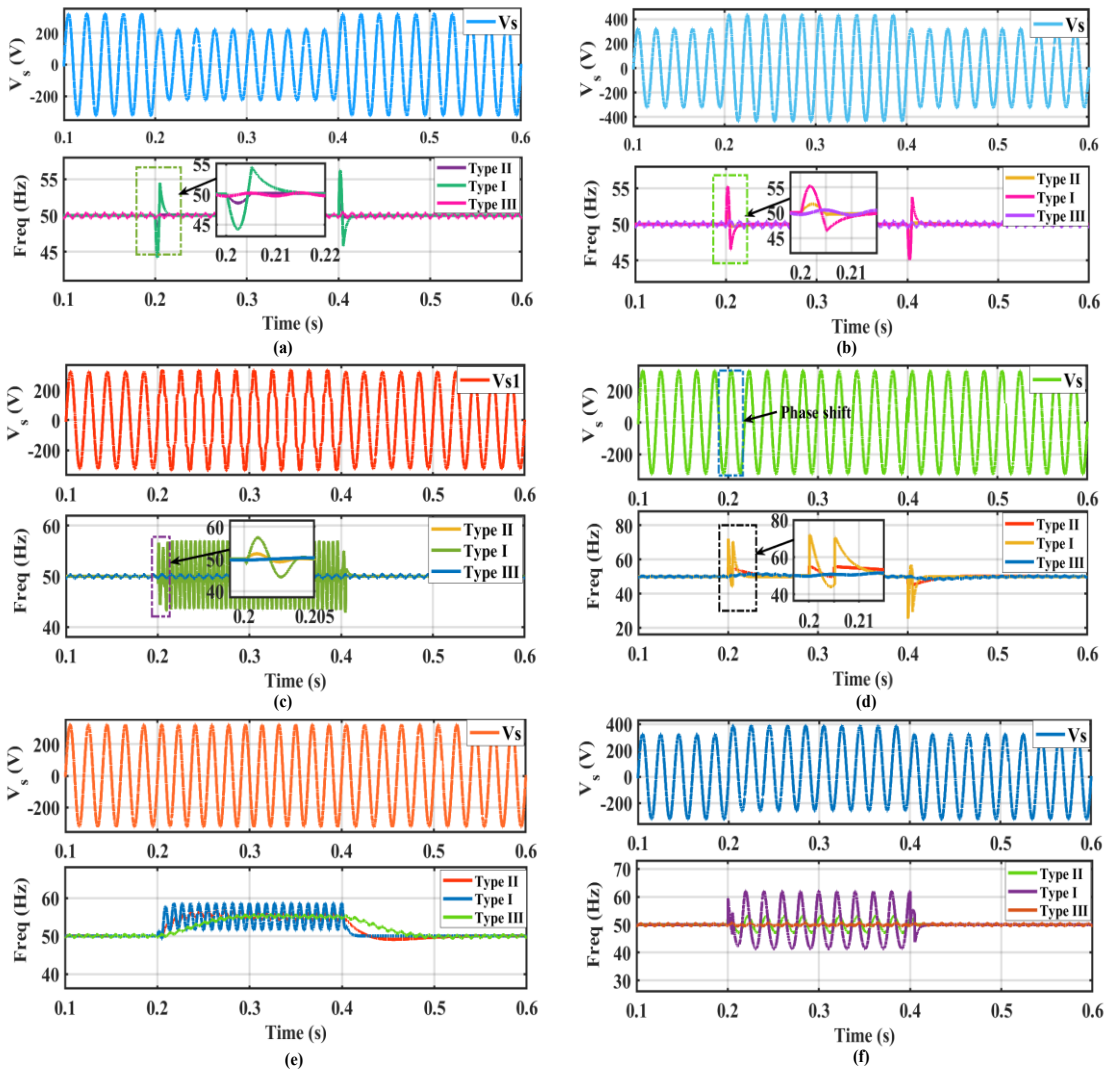


Fig. 4.16 Comparative simulation results of Type I, Type II and Type III PLL at grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30° phase shift, (e) +5Hz frequency change, (f) 20% dc-offset.

III PLL shows almost no change in Fig. 4.16 (d) shows the comparative simulation analysis of Type I, II and III PLLs under 30° phase shift disturbances. Type I PLL shows the overshoot of 71.92Hz in frequency response, Type II shows overshoot of 54.56 Hz while Type III PLL shows a slight rise of 51.72Hz. Type III takes longer settling time around 5 cycles while other two types of PLL takes around 3 cycles to come settle down to normal condition. Fig. 4.16 (e) shows the comparative simulation analysis of Type I, II and III PLLs under +5Hz frequency step change. Type I PLL shows the oscillatory frequency response of 58.58 Hz with settling time of 1 cycle after 0.4s. Type II also shows oscillatory signal of 55.61 Hz with 5 cycles as settling time

after 0.4s while Type III PLL shows overshoot of 55.02Hz frequency response and settles at around 4 cycles after 0.4s. Fig. 4.16 (f) shows the comparative simulation analysis of Type I, II and III PLLs under the presence of 20% DC offset in grid voltage. Type I PLL shows the oscillatory frequency response with overshoot of 61.67 Hz, Type II also shows oscillatory overshoot of 52.91 Hz while Type III PLL shows response of 50Hz during the entire disturbance interval.

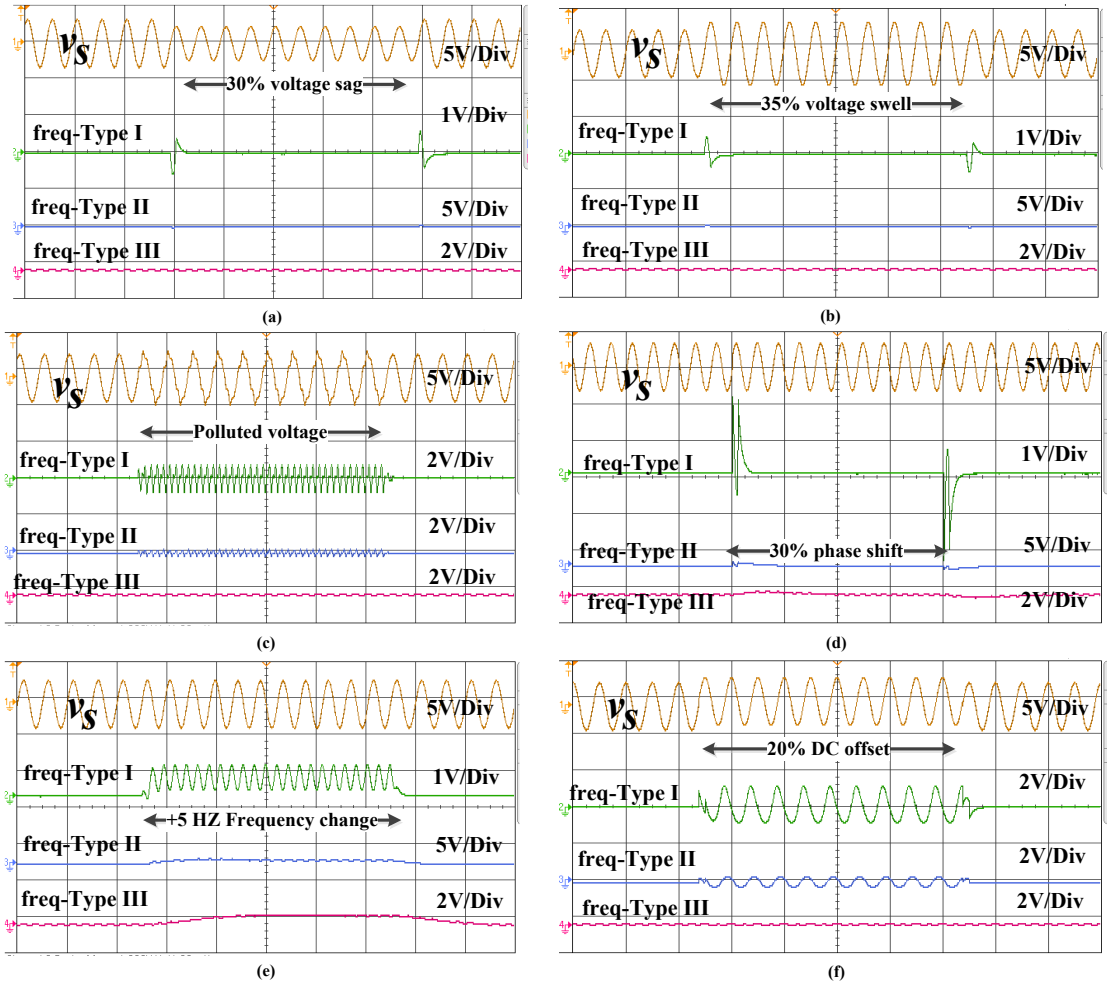


Fig. 4.17 Comparative experimental results of Type I, Type II and Type III PLL at grid abnormalities (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30° phase shift, (e) +5Hz frequency change, (f) 20% dc-offset.

The experimental comparative frequency response of the Type I, II and III PLLs under various grid voltage abnormalities is shown in Fig. 4.17. Fig.4.17 (a) shows the comparative response under 30% voltage sag. Type I shows overshoot, Type II shows slight drop and Type III shows almost no change during the disturbance period which validates the simulation results shown in Fig. 4.16 (a). Fig. 4.17 (b) shows the

comparative response under 35% grid voltage swell. Type I and Type II PLLs show overshoot in frequency response but Type III shows no change during the disturbance which validates the simulation results shown in Fig. 4.16 (b). Fig. 4.17 (c) shows the comparative response under polluted grid voltage disturbance. Type I shows large oscillatory response while Type II shows smaller oscillatory frequency response but Type III shows no change during the disturbance which validates the simulation results shown in Fig. 4.16 (c). Fig. 4.17 (d) shows the comparative response under 30^{o} phase shift. Type I PLL shows a very high overshoot and Type II PLL shows a smaller overshoot in frequency response and Type III PLL also shows very small rise in frequency response during the disturbance; it validates the simulation results shown in Fig. 4.16 (d). Fig. 4.17 (e) shows the comparative response under +5 Hz frequency change. Type I, Type II and Type III PLLs show +5Hz frequency response. Type I shows large oscillating response while Type III shows no oscillating response during the disturbance and validates the simulation results shown in Fig. 4.16 (e). Fig. 4.17 (f) shows the comparative response under the presence of 20% DC offset in grid voltage. Type I and Type II PLLs show oscillating frequency response but Type III shows no change during the disturbance which validates the simulation results shown in Fig. 4.16 (f).

The comparative results of the dynamic performance of Type I, II and III PLLs are tabulated in Table 4.5. The tabulation for the comparison is done by considering the parameters like overshoot and settling time of the frequency response in various grid abnormalities. During 30% sag in grid voltage, the frequency response of Type I PLL shows the highest overshoot with a settling time of two cycles and Type III PLL gives the least overshoot of 50.16Hz with fastest settling time among the three types of PLLs making it the best PLL during 30% voltage sag disturbance. During 35% grid voltage swell the frequency response of Type I gives the highest overshoot of 55.2Hz but it shows the fastest settling time of 1 cycle. Type II PLL give moderate overshoot but the slowest settling time of 3 cycles and Type III gives the least overshoot with moderate settling time. So, Type III PLL can be considered to be the best PLL under voltage swell considering overall dynamic performance regarding its robustness and stability. When a grid voltage is polluted with 3^{rd} and 5^{th} harmonics the frequency

tracked using Type I PLL gives the highest overshoot of 56.8Hz and whereas Type III PLL gives the least overshoot frequency response of 50.32 Hz. During this disturbance interval all the three types of PLLs show oscillations and among them Type III PLL gives the best dynamic performance. Under 30^{o} phase shift Type II PLL gives the moderate frequency overshoot of 54.56Hz and a slow dynamic response. Type III gives least overshoot but is very sluggish in nature. Type I PLL gives the highest frequency overshoot with fast settling time. Under +5 Hz frequency change the best dynamic performance is seen in Type III which has least overshoot of 55.02Hz and moderate settling time whereas Type II gives moderate frequency overshoot response with sluggish dynamic response. When 20% DC offset is present in grid voltage source the frequency tracked using Type III PLL shows least overshoot and least distortion which indicates that DC offset does not affect its dynamic performance. Type I PLL is highly affected with highest frequency overshoot and largest oscillating response during the entire disturbance period (0.2s-0.4s).

4.6 Conclusion

In this chapter modelling of three types of PLLs is carried out starting from general approach of modelling different types and orders of a PLL. Type I PLL considered for modelling is quasi-Type I PLL where MAF is used as controller with only proportional gain as loop filter. The presence of VCO as a basic component in the structure of PLL make this quasi type PLL as Type I PLL by structure but Type II by control. A pure Type I PLL which contains only one integrator as VCO does not perform well under grid disturbances. Type II PLL considered is SRF PLL as it contains two integrator one each from PI controller used as loop filter and integrator from VCO structure. The Type III PLL considered is Enhanced PLL having presence of three integrators for better performance. The stability aspects of all three Types of PLL have been investigated using Bode plots. Results have shown that although all three Types of PLL are stable, yet Type II and III PLLs have absolute stability. The various grid abnormalities like (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30^{o} phase shift, (e) +5Hz frequency change, (f) 20% dc-offset validate each other. Table 4.5 gives the summary of the dynamic performance analysis of the three types of PLLs under various grid abnormalities. Results have

Table 4.5: Comparative dynamic performance analysis of single-phase Type I, Type II and Type III PLLs

Grid condition tested	Parameter considered	Type I	Type II	Type III
30% voltage sag	**Overshoot**	Highest (54.22 Hz)	Medium moderate (48.53Hz)	Small (50.16Hz)
	Settling time	Moderate response (~ 2 cycles) 0.033s	Slower response (~3 cycles) 0.05s	Fast (1 cycles) 0.01s
35% voltage swell	**Overshoot**	Highest (55.2Hz)	Moderate (51.68 Hz)	Least (50.53Hz)
	Settling time	Fast response (1cycle) 0.012s	Slow response (~ 3cycles) 0.059s	Moderate (2 cycles) 0.03s
Polluted grid voltage	**Overshoot**	Highest (56.8 Hz)	Moderate (51.94 Hz)	Least (50.32Hz)
	Settling time	Oscillating (entire disturbed interval)	Oscillating (entire disturbed interval)	Oscillating (entire disturbed interval)
30^{o} phase shift	**Overshoot**	Highest (71.92 Hz)	Moderate (54.56 Hz)	Least (51.72Hz)
	Settling time	Fast response (~ 3 cycles) 0.05s	Slow response (3 cycles) 0.059s	Sluggish (~5 cycles) 0.09s
+5 Hz frequency shift	**Overshoot**	Highest (58.58 Hz)	Moderate (55.61 Hz)	Least (55.02Hz)
	Settling time	Fastest response (1cycle) 0.015s	Sluggish response (~ 5 cycles) 0.1s	Moderate response (~ 4 cycles) 0.079s
20% dc offset	**Overshoot**	Largest (61.67Hz)	moderate (52.91 Hz)	Lowest (50.02Hz)
	Settling time	Largest distortion (entire disturbed interval)	Small distortion (entire disturbed interval)	Least distortion (entire disturbed interval)

shown that Type III PLL gives the best overall frequency response even in the presence of polluted grid voltage and DC offset disturbance. Among the three types of PLLs, Type I PLL is the most severely affected PLL under all grid disturbances. The dynamic performance of Type II PLLs is better than Type I but worse than Type III PLLs.

Chapter 5

DESIGN AND PERFORMANCE ANALYSIS OF FRACTIONAL ORDER MODIFIED SRF PLL UNDER GRID ABNORMALITIES

5.1 Introduction

Three phase Synchronous Reference Frame PLL (SRF-PLL) is a very popular method for achieving synchronization in grid-connected power electronic converters. Single phase SRF-PLL is also popular and gives rapid and precise phase detection and a fairly satisfactory dynamic response under ideal grid circumstances. However, its efficiency significantly deteriorates in the presence of grid abnormalities like voltage amplitude change, frequency change and harmonic contents etc. Therefore, to improve its performance SRF-PLL is modified by adding an integral order low pass filter to the control loop and decrease the bandwidth of the SRF PLL at the expense of dynamic performance [68]. The traditional calculus based on integer order differentiation and integration is popular and convenient due to the absence of suitable and appropriate solution methods for fractional differential equations [142]. Thus, an interest in integrating fractional-order calculus into the Modified Synchronous Reference Frame PLL (MSRF-PLL) structure is developed in this work [78].

This chapter introduces and evaluates two novel fractional-order algorithms for a single phase MSRF PLL, analysing their effectiveness during various grid disturbances like (i) 30% voltage sags, (ii) 35% voltage swells, (iii) harmonic pollution, (iv) +5Hz frequency jump, (v) 30^{o}phase shifts, and (vi) 20% DC offset. The two novel designs are as follows

(i) design by incorporating a fractional-order element solely into a first-order low-pass filter (FO-LP) and it is named as Fractional Order Low Pass Modified Synchronous Reference Frame Phase Locked Loop (FO-LPMSRFPLL)

(ii) design by incorporating fractional-order control to both the first-order low-pass filter (FO-LP) and loop filter which is the proportional-integral (PI) controller (FO-PI) and termed it as Fractional Order Low Pass filter and Loop Filter (FO-PI) Modified Synchronous Reference Frame Phase Locked Loop (FO-LP FO-PI) MSRFPLL.

The parameter of the fractional orders 'α' and 'b' for the newly designed novel controllers are defined within the range of 0 to 2. Analysis of the dynamic performance of the two novel FO algorithms of MSRF PLL has been program using a typical toolbox like the Fractional-Order Modelling and Control (FOMCON) toolbox for the MATLAB/SIMULINK. FOMCON is a new type of toolbox in MATLAB for fractional order modelling and control. It offers fractional system analysis in the time and frequency domains and the verification of the system stability. The fractional order transfer function (FOTF) in the toolbox provides fractional-order systems. The experimental results are taken through OPAL-RT setup in the laboratory. The steady state stability of both fractional order algorithms (FO-LP MSRFPLL and FO-LPFO-PI MSRFPLL) are tested through the Bode Plot.

5.2 Design and Mathematical modelling of the system

The mathematics which deals with the study of integrals and derivatives of any order, including fractions, is known as fractional calculus. Leibniz and L'Hopital were the first to propose its concept in 1695. Fractional calculus is based on a number of fundamental definitions, such as those provided by Riemann–Liouville, Caputo, Grünwald–Letnikov, and the Cauchy integral formula. This calculus's basic operator ${}_{a}D_{T}^{rl}$ unifies these operations for any real order and is a continuous integro-differential operator with bounds a and T. The continuous integral-differential operator is defined as

$$ {}_{a}D_{T}^{rl} = \begin{cases} d^{rl}/d^{rl} & R(rl) > 0 \\ 1 & R(rl) = 0 \\ \int_{0}^{T} d\tau^{-rl} & R(rl) < 0 \end{cases} \qquad (5.1) $$

The order of the operation is 'rl' and it belongs to real number (rl∈ R), but this order of operation can also be a complex number [140]. The most popularly used definition of fractional-order calculus are defined by Grunwald-Letnikov and Riemann-Liouville [141]. The fractional order definition given by Grunwald-Letnikov is expressed as

$$ {}_{a}\mathbf{D}_{\mathbf{T}}^{\mathbf{rl}}\mathbf{f(t)} = \lim_{h \to 0} \mathbf{h}^{-\mathbf{rl}} \sum_{\mathbf{j}=0}^{\frac{\mathbf{T}-\mathbf{a}}{\mathbf{h}}} (-1)^{\mathbf{j}} \binom{\mathbf{rl}}{\mathbf{j}} \mathbf{f(T - jh)} $$

(5.2) Equation (5.2) describes a fractional calculus operator (D) that can perform both differentiation and integration. The value of 'rl' (which is a non-integer) determines the differential and integral operation: a positive value means differentiation; a negative value means integration. The binomial coefficients $\binom{rl}{j}$ are part of the operator's definition, and the limits of integration is specified by the subscripts on operator 'D'. The fractional-order integral according to Riemann-Liouville(Haubold & Mathai, 2017) is expressed as

$$ {}_{a}D_{T}^{-rl}f(t) = \frac{1}{\Gamma(rl)} \int_{a}^{T} (t - \tau)^{rl-1} f(t) d\tau \tag{5.3} $$

The initial value is given by 'a' and $0 < rl < 0$. When 'a' = 0, the integral form is simply denoted by $ {}_{a}\mathbf{D}_{\mathbf{t}}^{-\mathbf{rl}}\mathbf{f(t).}$ The Laplace transformation of fractional-order differentiation defined by Riemann-Liouville is expressed as

$$ \int_{0}^{\infty} e^{-st} {}_{0}D_{T}^{rl} f(t) dt = s^{rl} F(s) - \sum_{k=0}^{n-1} s^{k} {}_{0}D_{t}^{rl-k-1} f(t)\Big|_{T=0} \tag{5.4} $$

where$(n - 1 < rl \leq n)$. Similarly, the Laplace transformation of the fractional-order differentiation defined by Riemann-Liouville is expressed as

$$ \int_{0}^{\infty} e^{-st} {}_{0}D_{t}^{r'} f(t) dt = s^{r'} F(s) - \sum_{k=0}^{n-1} s^{k} {}_{0}D_{t}^{r'-k-1} f(t)\Big|_{t=0} \tag{5.5} $$

The fractional calculus is able to create accurate models that closely resemble real objects and for this reason recently numerous developments is seen in technical and physical system.

5.2.1 Mathematical modelling of Integer-order MSRF PLL

MSRF PLL is developed by adding a first order low pass filter to eliminate the noise associated with the input voltage signal, (v_s) and it is shown in Fig. 5.1. The components of the MSRF PLL like phase detector (PD), loop filter (LF) which is normally a proportional integral (PI) controller and the voltage-controlled oscillator (VCO) are of integer order. A simple first-order low-pass filter is used in the PD section of the PLL. It produces the orthogonal voltage signal ($v_{s\beta}$) by precisely delaying the primary input voltage signal ($v_{s\alpha}$) by a quarter of a cycle (i.e., by 90° phase delay). A Park's transformation block is used to transform these two signals ($v_\alpha$and v_β) from a stationary to a rotating coordinate system (dq-frame). The q-frame voltage on the quadrature axis (v_q) is actively forced to zero by the system's control loop when the phase error between input reference grid voltage equals the output phase angle (θ_{out}) from VCO. The reactive voltage component 'v_{sq}' provides phase calculation error while 'v_{sq1}' provides the phase calculation error after the removal of disturbances by the first order low pass filter (LPF). The estimated grid frequency (ω_O)

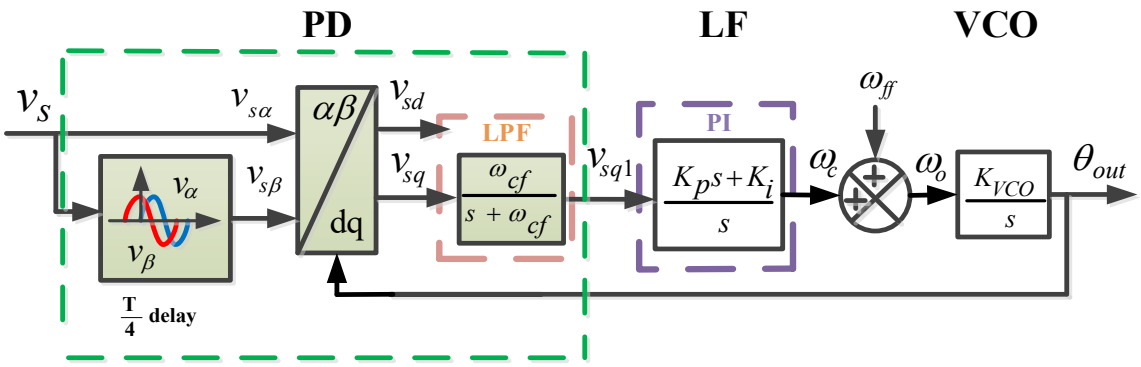


Fig. 5.1: Block diagram of MSRF PLL having integer order LPF and PI controller

is generated by combining the output from loop filter (ω_c) with the nominal frequency ($\omega_{ff} = 100\pi\ rad/s$) of the system and the estimated frequency is expressed as $\omega_o = \omega_c + \omega_{ff}$. This estimated frequency (ω_O) is then integrated by a VCO to determine the estimated signal's phase angle (θ_{out}). Integer-order transfer functions are used to model the whole control system of MSRF-PLL. A sinusoidal input signal v_s (V) having magnitude of V_s (V), nominal frequency ω_{ff} (Hz) is modelled as grid supply

voltage and the output of the PLL is the phase angle θ_{out} (°). The grid supply voltage is given as

$$\left.\begin{array}{c} v_s = V_s sin\omega_o t = V_s sin\theta_{out} \\ \sin\left(\omega_o t + \frac{t}{4}\right) = \cos\omega_o\, t = \cos\theta_{out} \\ v_{s\alpha} = V_s \sin\theta_{out} \\ v_{s\beta} = V_s \sin\left(\omega_o t + \frac{T}{4}\right) = V_s\, cos\,\theta_{out} \end{array}\right\} \quad (5.6)$$

The following equations are obtained after Park transformation of $v_{s\alpha}$ and $v_{s\beta}$

$$\begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} = \begin{bmatrix} sin\,\theta_{out} & -\cos\theta_{out} \\ \cos\theta_{out} & \sin\theta_{out} \end{bmatrix} \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \quad (5.7)$$

$$\left.\begin{array}{l} v_{sd} = V_{s\alpha} \sin\theta_{out} - V_{s\beta} \cos\theta_{out} \\ v_{sq} = V_{s\alpha} \cos\theta_{out} + V_{s\beta} \sin\theta_{out} \end{array}\right\} \quad (5.8)$$

The magnitude of 'v_s' is calculated as $V_s = \sqrt{\left({v_{sd}}^2 + {v_{sq}}^2\right)}$. The phase angle-error of grid voltage 'v_s' is computed from 'v_{sq}' at PCC of grid utility converters and it is passed through a low pass filter (LPF) of first order to exclude high amplitude steady state oscillations in the calculated phase and frequency and the output of the LPF is denoted by 'v_{sq1}'. The transfer function of the first order low pass filter (LPF) with a cut-off frequency 'ω_{cf}' having integral order of 's' can be expressed as

$$\mathrm{Tf_{LPF}(s)} = \frac{\omega_{cf}}{s + \omega_{cf}} \quad (5.9)$$

The transfer function of the phase detector (PD) section consists of a gain K_{PD} and the first order low pass filter can be expressed as

$$\mathrm{Tf_{PD}(s)} = K_{PD} \frac{\omega_{cf}}{s + \omega_{cf}} \quad (5.10)$$

The phase error from PD 'v_{sq1}' is passed through the loop filter (LF) which is a proportional and integral (PI) controller. It is designed for control by using an integral order capacitive impedance with a proportional gain and integral gain denoted as K_p andK_i respectively. The transfer function of this PI controller is given as

$$\mathrm{Tf_{LF}(s)} = \frac{K_p\, s + K_i}{s} \quad (5.11)$$

The transfer function of VCO with a gain 'K_{VCO}' is given by

$$\mathrm{Tf_{VCO}(s)} = \frac{K_{VCO}}{s} \tag{5.12}$$

The output obtained after integration from the VCO is the estimated phase angle which is denoted by θ_{output}.

The transfer function of the open-loop system, '$\mathrm{Tf_{LG}}$' of integral order MSRF PLL can be expressed as

$$\mathrm{Tf_{LGMSRF}(s)} = [\mathrm{Tf_{PD}\ (s)}] * [\mathrm{Tf_{LF}(s)}] * [\mathrm{Tf_{VCO}\ (s)}]$$

$$= \left[\frac{K_{PD}\omega_{cf}}{s+\omega_{cf}}\right] * \left[\frac{K_p s+K_i}{s}\right] * \left[\frac{K_{VCO}}{s}\right]$$

$$= \left[\frac{K_{PD}K_pK_{VCO}\,\omega_{cf}\,s+\,K_{PD}K_iK_{VCO}\omega_{cf}}{s^3+\omega_{cf}s^2}\right]$$

$$= \left[\frac{Ks+K^{/}}{s^3+s^2\omega_{cf}}\right] \tag{5.13}$$

where 'K' and '$K^{/}$' are the constant, whose values are represented by $K = K_{PD}K_{VCO}K_p\omega_{cf}$ and $K^{/} = K_{PD}K_{VCO}K_i\omega_{cf}$. The closed-loop transfer function for integer order MSRF-PLL is given by

$$\mathrm{Tf_{clMSRF}(s)} = \frac{\theta_{output}}{\theta_{input}} = \frac{\mathrm{Tf_{LGMSRF}\ (s)}}{1+\mathrm{Tf_{LGMSRF}(s)}}$$

$$= \left[\frac{(K_{PD}\omega_{cf})*(K_p\,s+\,K_i)*(K_{VCO})}{(s^3+\,s^2\omega_{cf})+(K_{PD}\omega_{cf})*(K_p\,s+\,+K_i)*(K_{VCO})}\right]$$

$$= \left[\frac{K_{PD}K_pK_{VCO}\omega_{cf}\,s\,+\,K_{PD}K_{VCO}K_pK_i\omega_{cf}}{s^3+\,\omega_{cf}s^2+\,K_{PD}K_pK_{VCO}\omega_{cf}\,s+\,K_{PD}K_iK_{VCO}\omega_{cf}}\right]$$

$$= \frac{Ks+K^{/}}{s^3+\omega_{cf}\,s^2+Ks+K^{/}} \tag{5.14}$$

The transfer function of error response for integral order MSRF-PLL is expressed as

$$\mathrm{E_{MSRF}(s)} = \frac{1}{1+Tf_{LG}(s)}$$

$$= \frac{1}{1+\left(\frac{Ks+\,K^{/}}{s^3+\,\omega_{cf}s^2}\right)}$$

$$= \frac{s^3+\,\omega_{cf}\,s^2}{s^3+\,\omega_{cf}\,s^2+\,Ks+\,K^{/}} \tag{5.15}$$

The phase angle of input, error and output signals are denoted as θ_{input}, θ_{error}, and θ_{out}. The phase error of the integral order MSRF PLL is given by $\theta_{error} = \theta_{input} - \theta_{out}$ and it is obtained with negative feedback of the output signal.

5.3 Mathematical Modelling of Fractional-order MSRF-PLL

The conventional electronic filters designing is described by the generalised transfer function as $H(s) = \frac{N(s)}{D(s)}$ which is actually a polynomial function with Laplacian operator 's'.

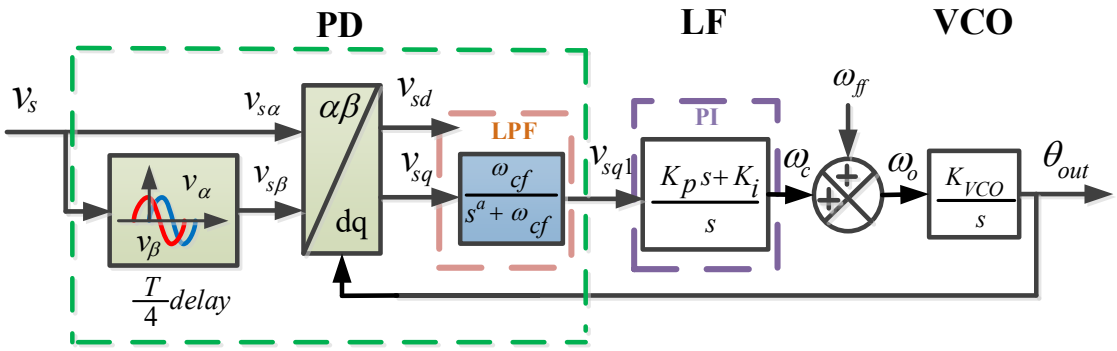


Fig. 5.2: Block diagram of MSRF-PLL with fractional-order low pass filter (FO-LP)

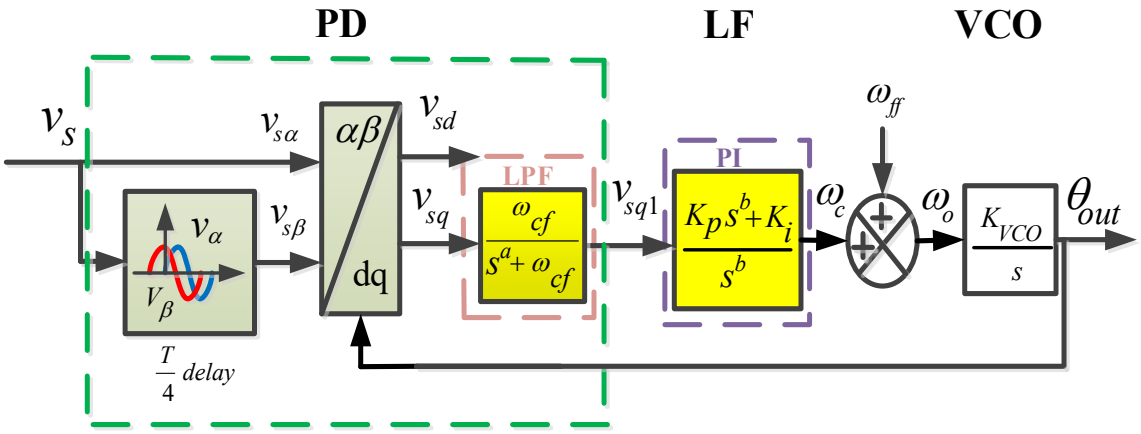


Fig. 5.3: Schematic block diagram of MSRF-PLL with fractional-order of both low pass filter and PI controller (FO-LPFO-PI)

Thus, with fractional exponent of operator 's' like 's^a', 's^b' where 0<a<2 and 0<b<2. Two fractional-order models of MSRF-PLL are designed and they are shown in Fig. 5.2 and Fig. 5.3. Fig. 5.2 shows the configuration of fractional-order model of MSRF-PLL (FO-LP MSRF-PLL) where the first order low pass filter (passive RC filter) is made fractional using an order 'a'. However, the second fractional-order algorithm is shown in Fig. 5.3 and it is designed by making fractional first order low pass filter (FO-LP) of order 'a' and fractional order proportional plus integral (PI) controller (FO-PI) with fractional order 'b' respectively.

The transfer functions of fractional low pass filter (FO-LP) having fractional-order 'a' and fractional-order proportional plus integral (FO-PI) controller having

fractional- order 'b' (0 < b < 2) can be expressed as:

$$\mathrm{Tf}_{\mathrm{FO-LP}}(\mathrm{s}) = \frac{\omega_{cf}}{s^a+\omega_{cf}} \tag{5.16}$$

$$\mathrm{Tf}_{\mathrm{FO-PI}}(\mathrm{s}) = K_p + \frac{K_i}{s^b} \tag{5.17}$$

The transfer function of the PD section of MSRF-PLL which has a gain as $K_p$and fractional order first order low pass filter in Laplace domain is now expressed as

$$Tf_{FO-PD}(s) = K_{PD}[Tf_{FO-LP}(s)] = \frac{K_p\omega_{cf}}{s^a+\omega_{cf}} \tag{5.18}$$

The transfer impedance of the VCO block is considered integral order in both the fractional order models (FO-LP MSRFPLL and FO-LPFO-PI MSRF PLL) developed and its transfer function is expressed as $\mathrm{Tf}_{\mathrm{VCO}}(\mathrm{s}) = \frac{K_{VCO}}{s}$ which is the same as that is given in equation (5.12).

5.3.1 Mathematical Model FO-LP MSRF-PLL

The mathematical model of transfer-functions for open-loop, closed-loop and error response of fractional-order MSRF-PLL which has only fractional order low pass filter (FO-LP) are developed in this Section. The transfer function for open-loop gains FO-LP MSRF-PLL using equations (5.11), (5.12) and (5.18) can be expressed as

$$\mathrm{Tf}_{\mathrm{LG\ FOLP}}(\mathrm{s}) = [\mathrm{Tf}_{\mathrm{FO-PD}}(\mathrm{s})] * [\mathrm{Tf}_{PI}(\mathrm{s})] * [\mathrm{Tf}_{\mathrm{VCO}}(\mathrm{s})]$$

$$= \mathrm{K}_{\mathrm{PD}}[\mathrm{Tf}_{\mathrm{FO-LP}}(\mathrm{s})] * [\mathrm{Tf}_{\mathrm{LF}}(\mathrm{s})] * [\mathrm{Tf}_{\mathrm{VCO}}(\mathrm{s})]$$

$$= \left[\frac{K_{PD}\omega_{cf}}{s^a+\omega_{cf}}\right] * \left[\frac{K_p s+K_i}{s}\right] * \left[\frac{K_{VCO}}{s}\right]$$

$$= \left[\frac{K_{PD}\,K_p\,K_{VCO}\,\omega_{cf}s+K_{PD}\,K_i\,K_{VCO}\,\omega_{cf}}{s^{2+a}+\omega_{cf}s^2}\right]$$

$$= \left[\frac{Ks+K'}{s^{2+a}+\omega_{cf}\,s^2}\right] \tag{5.19}$$

where$K = K_{PD}K_{VCO}K_p\omega_{cf}$and $K' = K_{PD}K_{VCO}K_i\,\omega_{cf}$.

The closed-loop transfer function of FO-LP MSRF-PLL is expressed as

$$\mathrm{H_{FO-LP}(s)} = \frac{\theta_{\mathrm{output}}}{\theta_{\mathrm{input}}} = \left[\frac{\mathrm{Tf_{LG\ FO-LP}(s)}}{1+\mathrm{Tf_{LG\ FO-LP}(s)}}\right]$$

$$= \left[\frac{K_{PD}\,K_{VCO}K_P\omega_{cf}s + K_{PD}K_{VCO}K_i\omega_{cf}}{s^{2+a} + \omega_{cf}s^2 + K_{PD}K_{VCO}K_p\omega_{cf}s + K_{PD}K_{VCO}K_i\omega_{cf}}\right]$$

$$= \left[\frac{Ks+K^{/}}{s^{2+a}+\omega_{cf}s^2+Ks+K^{/}}\right] \tag{5.20}$$

where$K = K_{PD}K_{VCO}K_P\omega_{cf}$ and$K^{/} = K_{PD}K_{VCO}K_i\omega_{cf}$.

Moreover, the error response transfer function of the FO-LPF MSRF-PLL can be expressed as

$$\mathrm{E_{FO-LP}(s)} = \left[\frac{\theta_{error}}{\theta_{input}}\right] = \left[\frac{1}{1+\mathrm{Tf_{LGFO-LP}(s)}}\right]$$

$$E_{FO-LP}(s) = \left[\frac{\theta_{error}}{\theta_{input}}\right] = \left[\frac{1}{1+Tf_{LGFO-LP}(s)}\right] \tag{5.21}$$

where$K = K_{PD}K_{VCO}K_P\omega_{cf}$, $K^{/} = K_{PD}K_{VCO}K_i\omega_{cf}$. The θ_{input}, θ_{error} and θ_{output} are the Laplace transformation for phase angle of input signal, error signal and output signal respectively.

5.3.2 Mathematical Model of FO-LPFO-PI MSRF PLL

The fractional order FO-LPFO-PI MSRF-PLL has been modelled by considering both fractional first order low pass filter (FO-LP) and fractional loop filter, which is a PI controller (FO-PI). The open-loop gain transfer function of FO-LPFO-PI MSRF-PLL is expressed as

$$\mathrm{Tf_{LGFOLPFOPI}(s)} = [\mathrm{Tf_{PD}}] * [\mathrm{Tf_{FO-PI}}] * [\mathrm{Tf_{VCO}}]$$

$$= K_{PD} * [\mathrm{Tf_{FO-LP}}] * [\mathrm{Tf_{FO-PI}}] * [\mathrm{Tf_{VCO}}]$$

$$= \left[\frac{K_{PD}\omega_{cf}}{s^a+\omega_{cf}}\right] * \left[\frac{K_p s^b + K_i}{s^b}\right] * \left[\frac{K_{VCO}}{s}\right]$$

$$= \left[\frac{K_{PD}K_pK_{VCO}\omega_{cf}s^b + K_{PD}K_{VCO}K_i\omega_{cf}}{s^{(1+a+b)}+\omega_{cf}s^{(1+b)}}\right]$$

$$= \left[\frac{Ks^b + K'}{s^{(1+a+b)} + \omega_{cf} s^{(1+b)}}\right] \quad (5.22)$$

where$K = K_{PD}K_{VCO}K_p\omega_{cf}$and $K' = K_{PD}K_{VCO}K_i\omega_{cf}$

The closed-loop transfer function of FO-LPFO-PI MSRF-PLL is expressed as

$$\mathrm{H_{FOLPFOPI}(s)} = \left[\frac{\theta_{output}}{\theta_{input}}\right] = \left[\frac{\mathrm{Tf_{LGFOLPFOPI}(s)}}{1+\mathrm{Tf_{LGFOLPFOPI}(s)}}\right]$$

$$= \frac{K_{PD}K_pK_{VCO}\omega_{cf}s^b + K_{PD}K_iK_{VCO}\omega_{cf}}{s^{(1+a+b)} + \omega_{cf}s^{(1+b)} + K_{PD}K_pK_{VCO}\omega_{cf}s^b + K_{PD}K_iK_{VCO}\omega_{cf}}$$

$$= \left[\frac{Ks^b + K'}{s^{(1+a+b)} + \omega_{cf}s^{(1+b)} + Ks^b + K'}\right] \quad (5.23)$$

where$K = K_{PD}K_pK_{VCO}\omega_{cf}$and $K' = K_{PD}K_iK_{CVO}\omega_{cf}$

The transfer function for error response of FO-LPFO-PI MSRF-PLL is expressed as

$$\mathrm{E_{FOLPFOPI}(s)} = \left[\frac{\theta_{error}}{\theta_{input}}\right] = \left[\frac{1}{1+\mathrm{Tf_{LGFOLPFOPI}(s)}}\right]$$

$$= \left[\frac{s^{(1+a+b)} + \omega_{cf}s^{(1+b)}}{s^{(1+a+b)} + \omega_{cf}s^{(1+b)} + K_{PD}K_pK_{VCO}\omega_{cf}s^b + K_{PD}K_iK_{VCO}\omega_{cf}}\right]$$

$$= \left[\frac{s^{(1+a+b)} + \omega_{cf}s^{(1+b)}}{s^{(1+a+b)} + \omega_{cf}s^{(1+b)} + Ks^b + K'}\right] \quad (.24)$$

where$K = K_{PD}K_pK_{VCO}\omega_{cf}$,$K' = K_{PD}K_iK_{VCO}\omega_{cf}$. The phase angles such as $\theta_{input,}$ θ_{error}, and $\theta_{output}$are respectively the phase angle of input, error and output signals.

5.4 Steady State Stability Analysis of Fractional-Order MSRF-PLLs

Stability analysis is an essential feature and crucial component of any PLL system as represents the capacity of a PLL to sustain a steady state (locked) relationship with the input signal even under grid disturbances. Hence, the study of the steady state stability of fractional order MSRF-PLL is very important and can be analysed by using frequency response obtained through the bode plots method. For stability analysis the linearization of the system is performed.

The phase margin and gain margin play a crucial role in predicting the stability and robustness of the PLL. The poles of the open loop system which are also the roots of the characteristic equation given by $[1 + Tf_{LG}(s) = 0]$ of a FO-MSRF PLL determine the stability condition of the fractional order PLLs. All the poles must have negative real part for the system to be stable. Bode plot is a technique used to examine a linear system's frequency response therefore, it is utilized to ascertain the phase margin for stability studies. Literature review suggests that a system with a low or negative phase margin (PM) may oscillate or be unstable and the one with a positive phase margin (PM) is stable under steady-state conditions and it will settle after a disturbance. The reciprocal of the frequency response amplitude in which the phase angle is -180° at crossover frequency (ω_{pc}) is the gain margin (GM). The gain margin (GM) of the open-loop system of fractional order MSRF-PLL having transfer function as $Tf_{LG}(j\omega_{\pi})$ is measured in dB and expressed as

$$GM = -20log|Tf_{LG}(j\omega_{\pi})|\text{dB}. \tag{5.25}$$

The frequency where either of the two ±180° axis crosses the open-loop locus is called as the phase crossover frequency (ω_{pc}). The phase margin (PM) is defined as the difference in phase between 180° and gain crossover and is measured in (°). It is expressed as

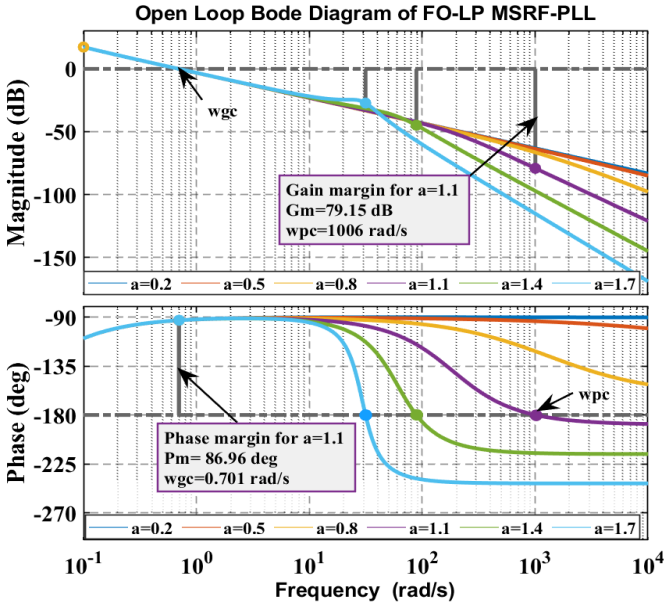
$$PM = arg\,[Tf_{LG}(j\omega_{\pi})] + \pi \tag{5.26}$$

The crossover frequency of the open-loop plot along 0-dB axis is termed as the gain crossover frequency (ω_{gc}).

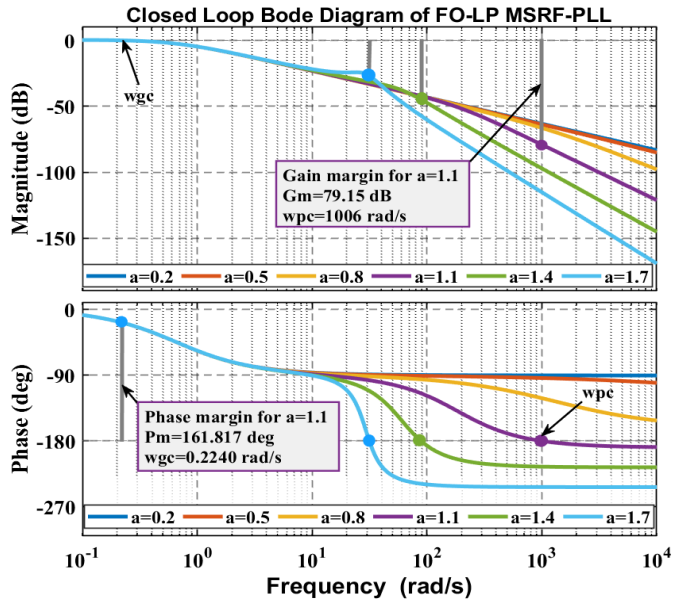
5.4.1 Stability Analysis of FO-LP MSRF-PLL with Fractional Order 'a'

Frequency response plots based on the open loop and closed loop transfer functions of FO-LP MSRF-PLL modelled in equations (5.19), (5.20) are shown. The stability criterion for any system including fractional order system will be considered stable if the phase margin (PM) and gain margin (GM) are both positive. Similarly, the fractional-order systems, FO-LP and FO-LPFO-PI MSRF PLLs are considered stable if phase margin (PM) and gain margin (GM) are positive at their respective cross over frequencies. Fig. 5.4: (a) and (b) show the frequency response of the open-loop

and closed-loop transfer function of FO-LP MSRF-PLL for various values of 'a' ranging between 0.2≤a≤1.7. Different values of fractional order 'a' are considered by making a step change of +0.3 points. Table 5.1 is prepared which includes all the calculated values of the gain margin (GM) and phase margin (PM) along with their respective crossover frequencies. The Bode diagrams shown in Fig. 5.4: (a) and (b)along with Table 5.1 are used for analysing the optimum value of the fractional order parameter 'a' for a stable FO-LP MSRF-PLL system.



(a)



(b)

Fig. 5.4: (a), (b) Bode diagrams of open loop and closed loop transfer functions of FO-LP MSRF-PLL

Table 5.1: Values of gain margin, phase margin and cross over frequencies for different values of 'a' for FO-LP MSRF-PLL

Value of 'a'	Value of 'GM' in dB		Value of 'ω_{pc}' in rad/s		Value of 'PM' in (°)		Value of 'ω_{gc}' in rad/s	
	Open-loop	Closed-loop	**Open-loop**	Closed-loop	**Open-loop**	Closed-loop	**Open-loop**	Closed-loop
a=0.2	-179.9	Infinite	5.0192e-06	undefined	87.0225	161.789	0.6989	0.2238
a=0.5	-184.9	Infinite	3.7692e-06	undefined	86.9699	161.780	0.6996	0.2242
a=0.8	-185.1	Infinite	3.7221e-06	undefined	86.9505	161.796	0.7004	0.2242
a=1.1	**79.16**	**79.15**	**1005.8**	**1006**	**86.9620**	**161.817**	**0.7011**	**0.2240**
a=1.4	44.84	44.79	88.7913	88.7913	86.9963	161.836	0.7017	0.2238
a=1.7	27.21	26.82	31.4975	31.4978	87.0420	161.847	0.7020	0.2237

Table 5.1 gives the values of gain margins (GM) in dB with its corresponding phase crossover frequencies (ω_{pc}) in rad/s and phase margins (PM) in (°) with its corresponding gain crossover frequencies (ω_{gc}) in rad/s for open-loop and closed-loop transfer functions of FO-LP MSRF-PLL for different values of 'a'. From Table 5.1, it is evident that the phase margin is positive and almost constant for 'a'= 0.2 to 1.7 for both open-loop and closed-loop system of FO-LP MSRF-PLL. However, for fractional order a=0.2 to 0.8, the system is unstable as GM is negative for open-loop of FO-LP MSRF-PLL. The closed-loop fractional order MSRF-PLL response with a= 1.1 to 1.7 with a step difference of 0.3 is analysed and it is observed that the values of GM happen to be positive however their values decrease for both the open-loop and closed-loop systems of FO-LP MSRF-PLL. From Table 5.1 and Fig. 5.4 (a) and (b) of the designed FO-LP MSRF-PLL it is observed that at 'a'=1.1, the value of GM is 79.16 dB with $\omega_{pc} = 1005.8$ rad/s for the open loop system and GM is 79.15 dB with $\omega_{pc} = 1006$ rad/s for closed loop system of FO-LP MSRF-PLL.

Again at 'a'= 1.1 the value of PM is 86.9620 dB with $\omega_{gc} = 0.7011$ rad/s for open loop system and PM is 161.817 dB with $\omega_{gc} = 0.2240$ rad/s for closed loop system

of FO-LP MSRF-PLL. Moreover, these are the highest positive values among the GM and PM obtained. Hence it can be concluded from Table 5.1 and Fig. 5.4 (a) and (b) that the designed FO-LP MSRF-PLL gives its best performance when the value of fractional order 'a' is optimized as 1.1.

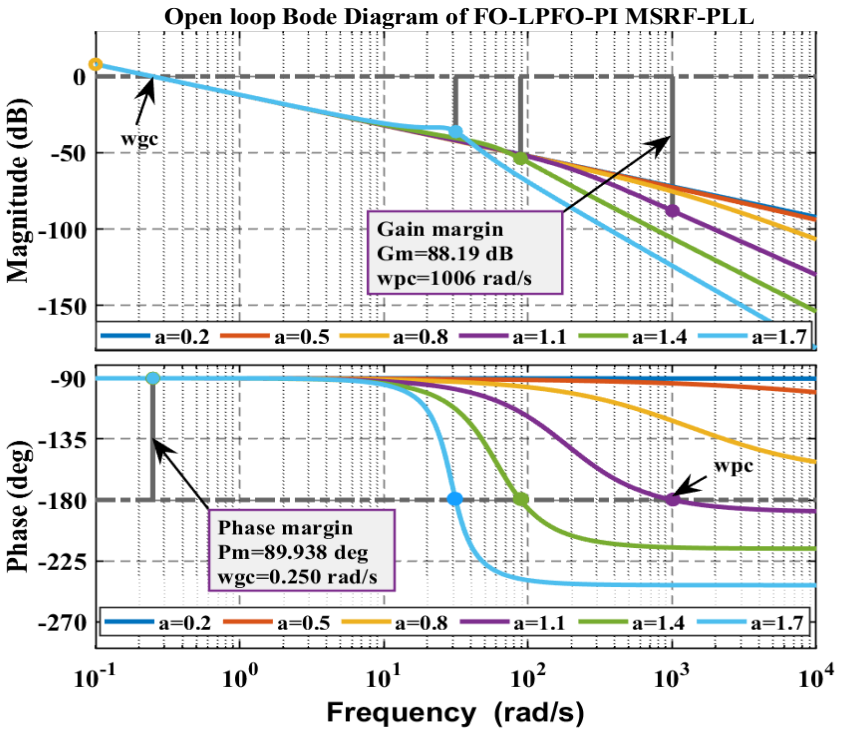
5.4.2 Stability Analysis of FO-LPFO-PI MSRF-PLL with Fractional Orders 'a' and 'b'

The second fractional order PLL design viz FO-LPFO-PI MSRF-PLL has been modelled with two fractional order components (fractional order low pass filter with fractional order parameter 'a' and fractional order proportional plus integral controller having fractional parameter 'b'). Since two varying fractional order parameters 'a' and 'b' are involved which need to be optimised therefore, two cases are considered for analysing the stability of FO-LPFO-PI MSRF-PLL through Bode Diagrams.

The optimized value of 'a' and 'b' are obtained by first keeping 'b' as fixed and varying 'a' and secondly by keeping the fractional order 'a' fixed and varying the second fractional order 'b'. With the two cases considered for stability analysis of the PLL, bode diagrams are plotted using the open loop and closed loop transfer functions as given in equations (5.22) and (5.23).

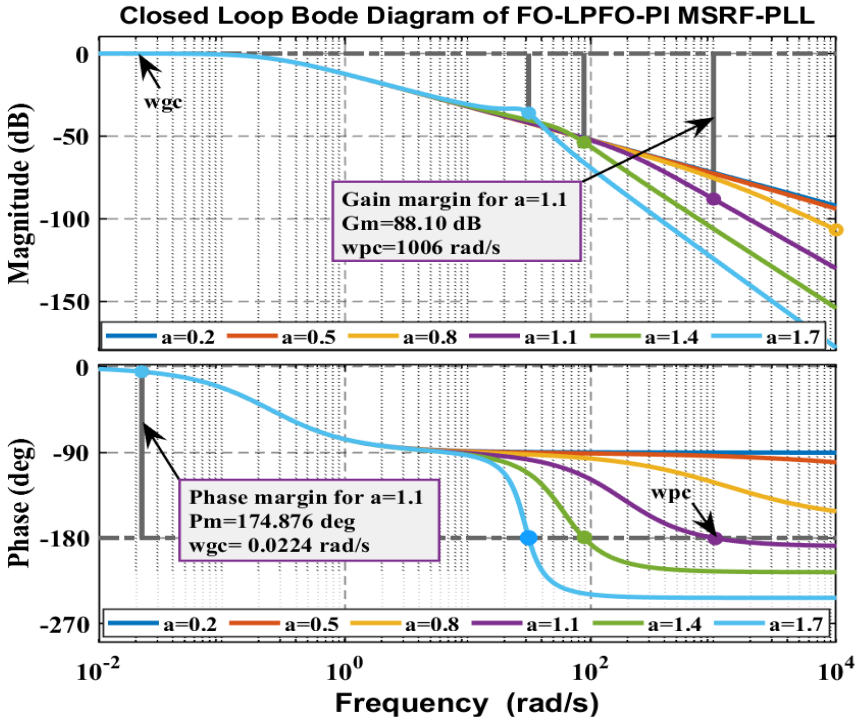
5.4.3 Stability analysis of FO-LPFO-PI MSRF-PLL with fixed 'b' and variable 'a'

The frequency response of FO-LPFO-PI MSRF-PLL is obtained by varying the fractional order 'a' and keeping the second fractional order 'b' fixed at 1. The fractional order 'a' is varied by keeping a uniform difference of 0.3 between each consecutive values. The values of 'a' chosen lies between 0.2 and 1.7 ($0.2 \leq a \leq 1.7$). Table 5.2 is drawn to obtain the optimized values of the fractional order parameter 'a' with 'b' being fixed for FO-LPFO-PI MSRF-PLL system. It gives information of the values of gain margin (GM) in dB with corresponding phase crossover frequencies (ω_{pc}) in rad/s and phase margins (PM) in (^{o}) with corresponding gain crossover frequencies ω_{gc} in rad/s. Table 5.2 shows that for the fractional integer 'a' lying in range of $0.2 \leq a \leq 0.8$, with a step difference of 0.3 the gain margin (GM) is found to be negative for open-loop and infinite for closed-loop system of FO-LPFO-PI MSRF-



(a)

Fig. 5.5: (a) Bode diagram for open loop transfer function of FO-LPFO-PI MSRF-PLL for fixed 'b' =1 and different values of 'a'



(b)

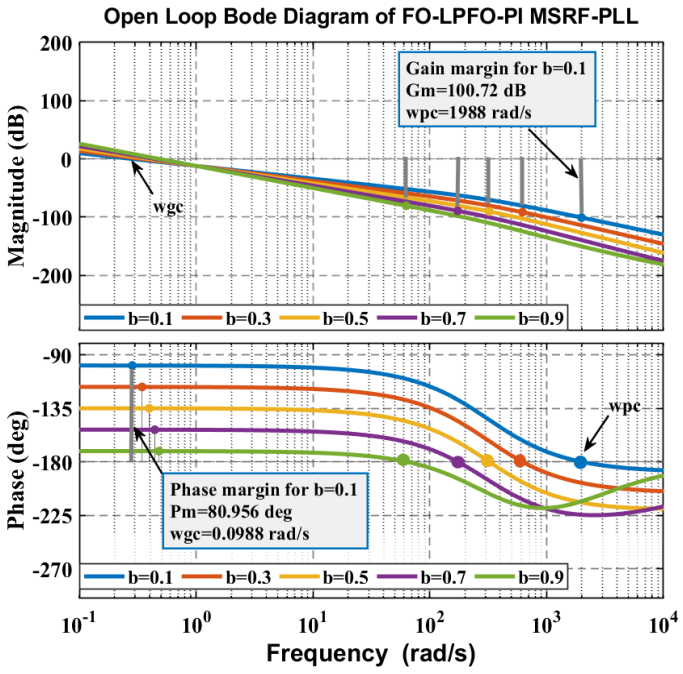
Fig. 5.5: (b) Bode diagram for closed loop transfer function of FO-LPFO-PI MSRF-PLL at fixed 'b' =1 and different values of 'a'

Table 5.2 and Bode diagrams shown in Fig. 5.5 (a) and (b), depict that for 'a'=1.1 to 1.7, the gain margin (GM) decreases with increase in fractional order 'a' but it is found that there is a minimal increment in phase margin (PM). Hence it is inferred from Table 5.2 that for 'a'=1.1 the system remains stable showing the highest positive value of gain margin, GM= 88.19 dB with $\omega_{pc} = 1006$ rad/s and phase margin, PM= 174.876 dB with $\omega_{gc} = 0.250$ rad/s open loop system FO-LPFO-PI MSRF-PLL. The values of closed loop are also positive for GM and PM with positive values of their respective cross over frequencies. Thus, the value of the fractional order parameter 'a'=1.1 is selected as the optimised value. Hence it can be inferred from Table 5.2 that for 'a'=1.1 the system remains stable showing highest positive value of GM and PM and this is the optimized choice for fractional parameter 'a' as 'b' is kept fixed.

Table 5.2: Gain margin, phase margin and cross over frequencies for different values of 'a' with fixed 'b' as 1 for FO-LPFO-PI MSRF-PLL

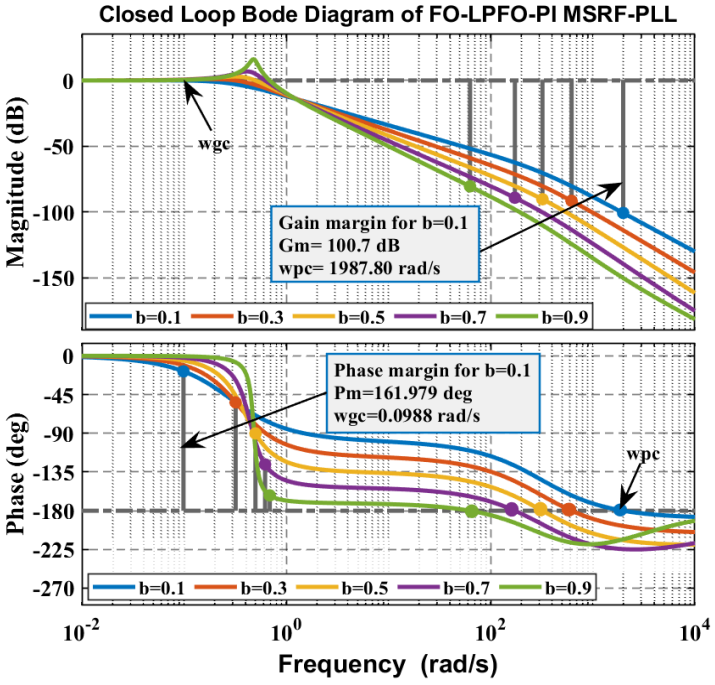
Value of 'a'	Value of 'GM' in dB		Value of phase crossover frequency 'ω_{pc}' in rad/s		Value of 'PM' in (°)		Value of gain crossover frequency 'ω_{gc}' in rad/s	
	Open-loop	Closed - loop	**Open-loop**	Closed-loop	**Open-loop**	Closed-loop	**Open-loop**	Closed-loop
a=0.2	-125.00	Infinite	3.6989e-06	undefined	89.934	174.849	0.249	0.0225
a=0.5	-125.20	Infinite	3.6962e-06	undefined	89.913	174.859	0.250	0.0224
a=0.8	-125.21	Infinite	3.6960e-06	undefined	89.920	174.871	0.250	0.0224
a=1.1	**88.19**	**88.10**	**1006**	**1006**	**89.938**	**174.876**	**0.250**	**0.0224**
a=1.4	83.79	53.77	88.8267	88.8258	89.956	174.878	0.250	0.0224
a=1.7	36.16	36.02	31.5083	31.5082	89.969	174.879	0.250	0.0224

5.4.4 Stability analysis of FO-LPFO-PI MSRF-PLL with Fixed 'a' and Variable 'b'



(a)

Fig. 5.6: (a) Bode diagram for open loop transfer function of FO-LP-PI MSRF-PLL at fixed 'a' = 1 with different values of 'b'



(b)

Fig. 5.6: (b) Bode diagram for closed loop transfer function of FO-LP-PI MSRF-PLL at fixed 'a' = 1 with different values of 'b'

In this case the fractional order parameter 'a' is kept fixed at 'a'=1 and fractional order parameter 'b' is varied from 0.1 to 0.9 with a step difference of 0.2 points between consecutive values. Figures5.6 (a) and (b) show Bode diagrams of the open-loop and closed-loop transfer functions of FO-LPFO-PI MSRF-PLL for fixed 'a' and variable 'b' ($0.1 \leq b \leq 0.9$). The gain margins (GM) and phase margins (PM) obtained with different values of 'b' are tabulated in Table 5.3. Table 5.3 shows different values of gain margin (GM) in dB with corresponding phase crossover frequencies (ω_{pc})in rad/s and phase margin (PM) with corresponding gain crossover frequencies (ω_{gc}) in rad/s. For both the open-loop and closed-loop system of the PLL, it is observed that both GM and PM decreases when value of fractional order 'b' increases and lies between $0.1 \leq b \leq 0.9$. At 'b'=0.1 and 'a' =1, the value of gain margin is positive and 100.718 dB with $\omega_{pc} = 1987.8$ rad/s while phase margin is also positive and 80.956° with $\omega_{gc} = 0.2838$ rad/s for open loop FO-LPFO-PI MSRF-PLL.

Table 5.3: Values of gain margin, phase margin and cross over frequencies for different values of 'b' and 'a' =1 for FO-LPFO-PI MSRF-PLL

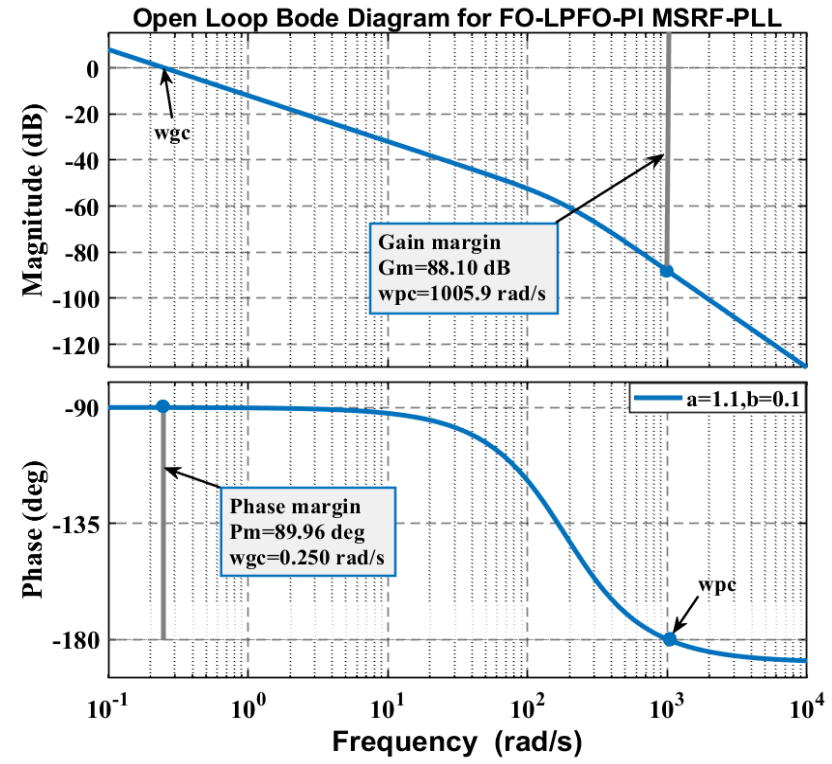
Value 'b'	Value of 'GM' in dB		Value of 'ω_{pc}' in rad/s		Value of 'PM' in (°)		Value of 'ω_{gc}' in rad/s	
	Open-loop	Closed-loop	**Open-loop**	Closed-loop	**Open-loop**	Closed-loop	**Open-loop**	Closed-loop
b=0.1	**100.718**	**100.72**	**1987.8**	**1987.80**	**80.956**	**161.979**	**0.2838**	**0.0988**
b=0.3	91.528	91.53	621.362	621.362	62.956	125.923	0.3444	0.3201
b=0.5	90.292	90.29	322.134	322.134	44.953	89.892	0.3970	0.5005
b=0.7	89.143	89.14	173.073	173.073	26.948	53.854	0.4425	0.6219
b=0.9	80.522	80.52	62.9963	62.996	8.941	17.8374	0.4821	0.6900

The gain margin, GM= 100.72 dB and PM= 161.979^{o} for closed loop FO-LPFO-PI MSRF-PLL. As these values of GM and PM are the largest positive value among all others calculated with different values of 'b'. Hence Fig. 5.6 (a), (b) and Table 5.3 it is observed that FO-LPFO-PIMSRF-PLL system is most stable for 'b'=0.1 when 'a' is kept fixed at 1. Thus, the optimized values for FO-LPFO-PI MSRF-PLL system are selected as 'a'=1 and 'b'=0.1 respectively.

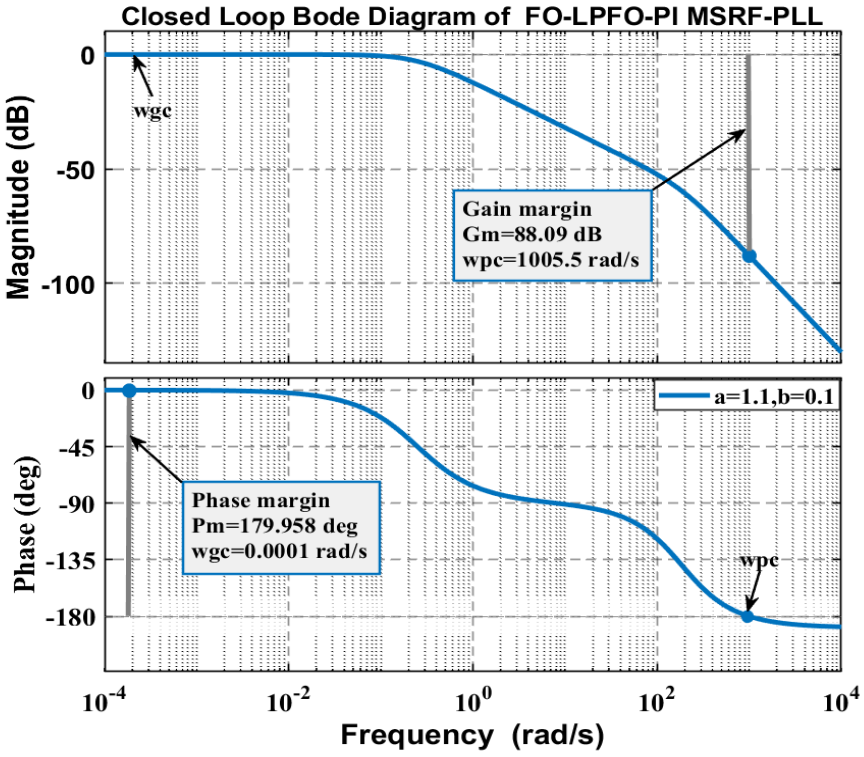
5.4.5 Stability Analysis of FO-LPFO-PI MSRF-PLL with optimized 'a' and 'b'

It is important to test the stability of FO-LPFO-PI MSRF-PLL with the selected optimised value of variables 'a' as a=1.1 and 'b' as b=0.1 in the previous sections. Therefore, Fig. 5.7: (a) and (b) show the Bode diagrams for the open-loop and closed-loop transfer functions for FO-LPFO-PI MSRF-PLL corresponding to the selected optimized values of 'a'=1.1 and 'b'=0.1. The open-loop gives a gain margin, GM= 88.10dB with phase crossover frequency (ω_{pc}) at 1005.9 rad/s and phase margin (PM) obtained is PM = 89.96^{o} with gain crossover frequency (ω_{gc}) at 0.25 rad/s. The closed-loop analysis from the frequency response plot shows that the gain margin, GM = 88.09 dB with phase crossover frequency (ω_{pc}) at 1005.5 rad/sand phase margin, PM =179.958^{o}. Thus, the values of GM and PM for both the open loop and closed loop FO-LPFO-PI MSRF- PLL are positive at their respective cross over frequencies. Hence FO-LPFO-PI MSRF-PLL is found stable for the selected and optimised values of 'a' and 'b'.

The findings of the frequency response plots of fractional order PLLs like FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL for both open loop and closed loop functions are tabulated in Table 5.4.



(a)



(b)

Fig. 5.7: (a) Open-loop and (b) Closed-loop transfer function of FO-LP-PIMSRF-PLL for 'a'=1.1 and 'b'=0.1

Table 5.4: Summarized results for FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL

Types of MSRF-PLL		Open-loop transfer function	Closed-loop transfer function
FO-LP MSRF-PLL		$\mathrm{Tf}_{\mathrm{LG\ FOLP}}(\mathrm{s}) = [\mathrm{Tf}_{\mathrm{FO-PD}}(\mathrm{s})] * [\mathrm{Tf}_{PI}(\mathrm{s})] * [\mathrm{Tf}_{\mathrm{VCO}}(\mathrm{s})] = \left[\frac{Ks+K'}{s^{2+a}+\omega_{cf}s^2}\right]$	$\mathrm{H}_{\mathrm{FO-LP}}(\mathrm{s}) = \left[\frac{\mathrm{Tf}_{\mathrm{LG\ FO-LP}}(\mathrm{s})}{1+\mathrm{Tf}_{\mathrm{LG\ FO-LP}}(\mathrm{s})}\right] = \left[\frac{Ks+K'}{s^{2+a}+\omega_{cf}s^2+Ks+K'}\right]$
	At optimized value of 'a'= 1.1 GM' in dB PM' in (°)	 **79.16 dB** **86.9620** °	 **79.15 dB** **161.817** °
FO-LPFO-PI MSRF-PLL		$\mathrm{Tf}_{\mathrm{LGFOLPFOPI}}(\mathrm{s}) = [\mathrm{Tf}_{\mathrm{PD}}] * [\mathrm{Tf}_{\mathrm{FO-PI}}] * [\mathrm{Tf}_{\mathrm{VCO}}] = \left[\frac{Ks^b+K'}{s^{(1+a+b)}+\omega_{cf}s^{(1+b)}}\right]$	$\mathrm{H}_{\mathrm{FOLPFOPI}}(\mathrm{s}) = \left[\frac{\mathrm{Tf}_{\mathrm{LGFOLPFOPI}}(\mathrm{s})}{1+\mathrm{Tf}_{\mathrm{LGFOLPFOPI}}(\mathrm{s})}\right] = \left[\frac{Ks^b+K'}{s^{(1+a+b)}+\omega_{cf}s^{(1+b)}+Ks^b+K'}\right]$
	At optimised value of 'a'= 1.1 and 'b'=0.1 'GM' in dB 'PM' in (°)	 **88.10 dB** **89.96°**	 **88.09 dB** **179.958°**

Table 5.4 discusses the summary of gain margin and phase margin results of the open-loop and closed-loop transfer functions of FO-LP MSRF-PLL that have been derived using equations (5.19) and (5.20) with optimized fractional parameter 'a' where the relevant Bode diagrams are presented in Fig. 5.4. FO-LPFO-PI MSRF-PLL has been designed with two two fractional parameters 'a' and 'b'. The open and closed loop

frequency responses are plotted using equations (5.22) and (5.23) respectively. The Bode diagrams for FO-LPFO-PI MSRF-PLL are plotted in Fig. 5.5-5.6 and it shows how two fractional varying parameters 'a' and 'b' are optimized by fixing 'a' while varying 'b' and vice versa. Fig. 5.5 shows the Bode plots for FO-LPFO-PI MSRF-PLL with variable 'a' and fixed 'b'=1. Fig. 5.6 shows the Bode plot for variable 'b' with fixed 'a'=1. The final optimised values of 'a' (a=1.1) and 'b' (b=0.1) for the open-loop and closed-loop transfer functions for FO-LPFO-PI MSRF-PLL is verified by the GM and PM obtained from Fig. 5.7: (a) and (b).

5.5 Dynamic Performance Analysis of MSRF-PLLs

The performance of the designed fractional order PLLs is studied for (i) integer order MSRF-PLL, (ii) FO-LP MSRF-PLL and (iii) FO-LPFO-PI MSRF-PLL. They are tested through simulation and experimental results using MATLAB/Simulink environment and fractional-order modelling and control (FOMCON) toolbox of MATLAB/Simulink respectively and a single-phase programmable grid voltage supply. A grid voltage supply is selected with peak of 325V, fundamental reference frequency of 50Hz and the parameters used for the FO-LPMSRF-PLL are cut off frequency, ω_{cf}= 2*π*36.72, gains of PI controller are K_p= 0.7, K_i = 0.025, a=1.1 and those for FO-LPFO-PI MSRF-PLL are cut off frequency, ω_{cf} = 2*π*36.72, gains of PI controller are, $K_p = 0.025$, $K_i = 0.000025$, and optimized fractional order values are 'a' =1.1 and'b' = 0.1, sampling time, Ts = 50e-6s under various grid abnormalities.

Test results include performance studied under (i) 30% grid voltage sag, (ii) 35% grid voltage swell, (iii) polluted environment (iv) 30^o phase shift (v) +5 Hz frequency change and (vi) 20% DC- offset. These disturbances are introduced from a time interval from 0.2s to 0.4s. The experimental results of the three PLL models are obtained from the laboratory set up consisting of a Digital Signal Oscilloscope (DSO) (Infinite Vision DSO-X-2014A), personal computer (PC) and REAL-TIMESIMULATOR (OPAL-RT OP4312) as shown in Fig. 5.8.

The dynamic performance of (i) integral order MSRF PLL, (ii) FO-LP MSRF-PLL and (iii) FO-LPFO-PI MSRF-PLL are tested using single phase programmable grid voltage supply. When there is grid disturbance, change in load, malfunctioning of

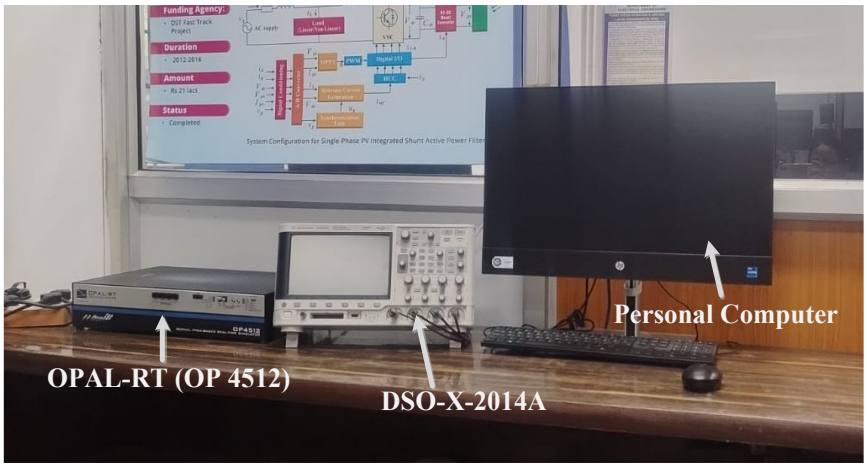


Fig. 5.8: Real Time Simulator lab set-up using OPAL-RT (OP4512) for experimental results.

relay or transformer tap change then such grid abnormalities may lead to voltage sag and swell conditions causing voltage amplitude variations in power system. A polluted supply is due to presence of nonlinear loads at the consumer end such as power electronic devices. The dynamic performance analysis of the proposed FO-LPMSRF-PLL and FO-LPFO-PIMSRF-PLL is carried out by analysing the grid parameters like input voltage supply in volts, estimated frequency of the system in (Hz), phase angle in (^{o}) and the amplitude of source voltage (V) at the point of common coupling of the systemin.

5.5.1 Simulation and Experimental Analysis of Integral Order MSRF-PLL

The simulated and experimental results of for integral order MSRF-PLL is shown in Fig. 5.9 and Fig. 5.10 respectively under various grid abnormalities like (a) 30% grid voltage sag (b) 35% grid voltage swell (c) polluted voltage supply (d) 30^o phase shift (e) +5Hz frequency change and (f) 20% DC-offset. The simulation results of integral order MSRF-PLL for analyzing the dynamic performance show the plots considering source voltage in volts (V), frequency in Hz, phase angle in (rad) and amplitude of voltage, (V) in volts (V) when the grid voltage undergoes 30% voltage sag are shown in Fig. 5.9: (a). The disturbance occurs for a duration of 0.2s i.e. from 0.2s-0.4s and after 0.4s the normalcy of the system is restored. In the voltage source amplitude, a drop of 30% sag of supply voltage is observed during disturbance from 0.2s to 0.4s. It is also observed that there is no change in the phase angle of such grid

voltage. However, the magnitude of the source voltage decreases during voltage sag conditions and is correctly estimated in simulation results.

Fig. 5.10: (a) shows the experimental result 30% voltage sag. The grid supply and its magnitude response depicts the voltage drop in plot validating the simulation results. Fig. 5.9: (b) and Fig. 5.10: (b) depicts the simulated dynamic performance under 35% grid voltage swell. A small variation in magnitude of the estimated frequency is observed in both the simulated and experimental results. There is no change in the estimated phase angle. The voltage amplitude also shows the 35% grid voltage swell in both the simulated and experimental results. Hence, experimental results of 35% voltage swell validates its simulation results. Fig. 5.9: (c) and Fig 5.10: (c) shows the simulated and experimental results analysis under polluted grid voltage respectively when 3^{rd} and 5^{th} harmonics are added to the input sinusoidal signal for time interval of 0.2s to 0.4s. The sinusoidal supply voltage becomes distorted during the disturbed interval due to the harmonic content. The frequency response of simulation results show a peak overshoot of 53.42 Hz at 0.202s which dies down within three cycles (0.06s). However, though there is change in experimental frequency response shown in Fig. 5.10: (c) though it is not clearly visible. The oscillatory response in voltage magnitude is seen in simulation results. The Fig. 5.9: (d) gives the dynamic performance under 30^{o} phase shift. The estimated frequency signal shows a peak overshoot of 59.71Hz at 0.21s. The overshoot settles down at 0.26s after a delay of 0.06s (within three cycles). The experimental frequency response also shows peak overshoot which dies down within three cycles. The voltage magnitude shows a peak overshoot of 397.4 V at 0.2s and dies down within three cycles (0.048s). The experimental result shown in Fig. 5.10: (d) also show the peak overshoot which dies down within three cycles. Fig. 5.9: (e) and Fig. 5.10: (e) present the simulated and experimental dynamic performance under +5 Hz step change in frequency. The frequency change leads to a peak oscillation of 59.2 Hz at 0.22s which settles down at 0.25s with a delay of 0.05s (within three cycles) in simulated result. An overshoot is also observed in the experimental frequency response. The voltage magnitude is distorted during the entire disturbed period in both the simulation and experimental results. Fig. 5.9: (f) of MSRF PLL presents the simulated dynamic performance under 20% DC-offset for time interval of 0.2s to 0.4s. The presence of this offset is predicted

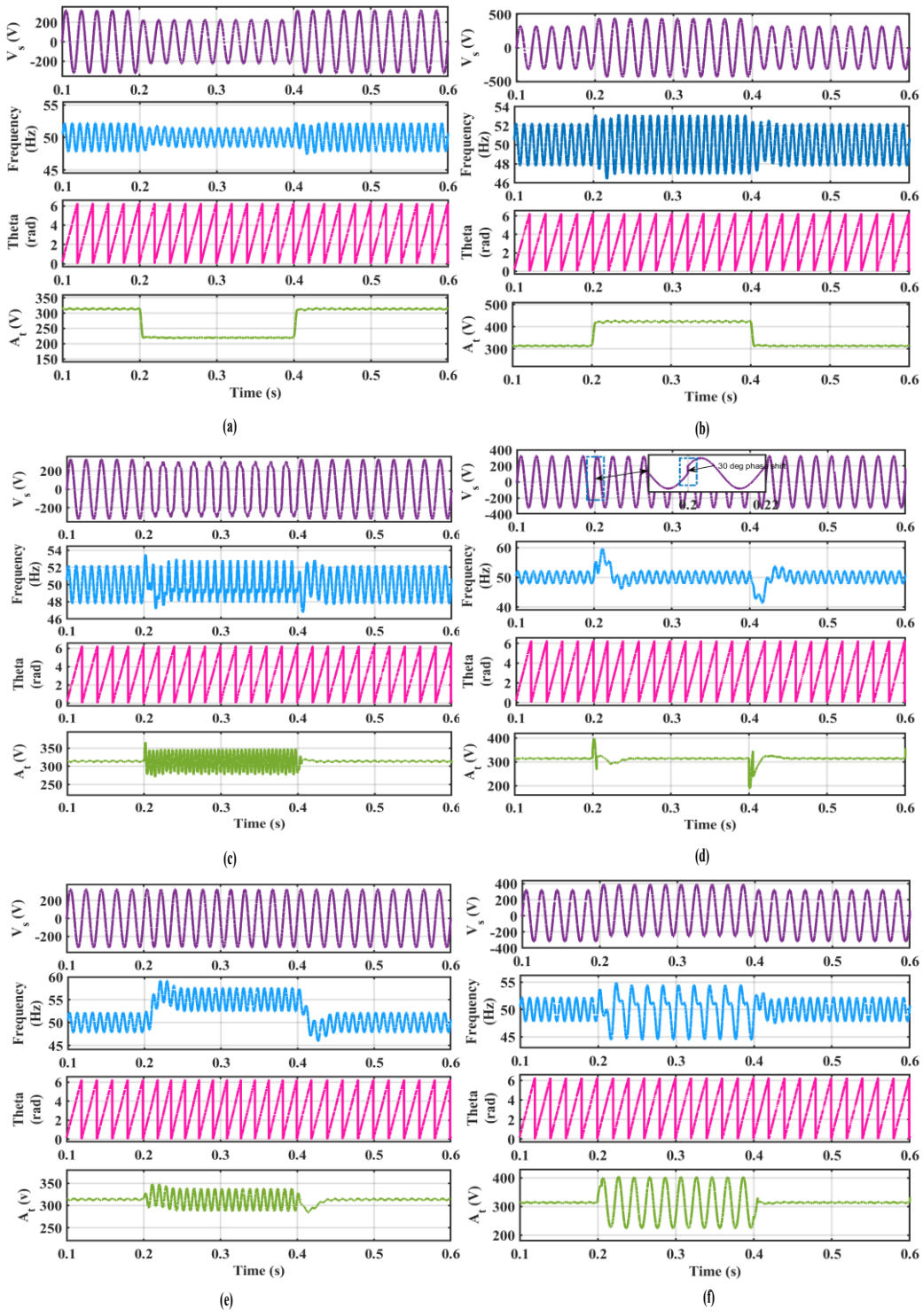


Fig. 5.9: Simulation results of MSRF PLL at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset

in source voltage and its magnitude during the disturbed interval. The frequency response is distorted during 0.2s-0.4s time interval in the simulated results. Fig. 5.10: (f) shows the experimental results under 20% DC offset in grid voltage. The supply

voltage depicts presence of DC offset led to distorted frequency signal response validating the simulated results. Therefore, from Fig. 5.9 and Fig. 5.10 it is observed that the simulated and the experimental responses validate each other.

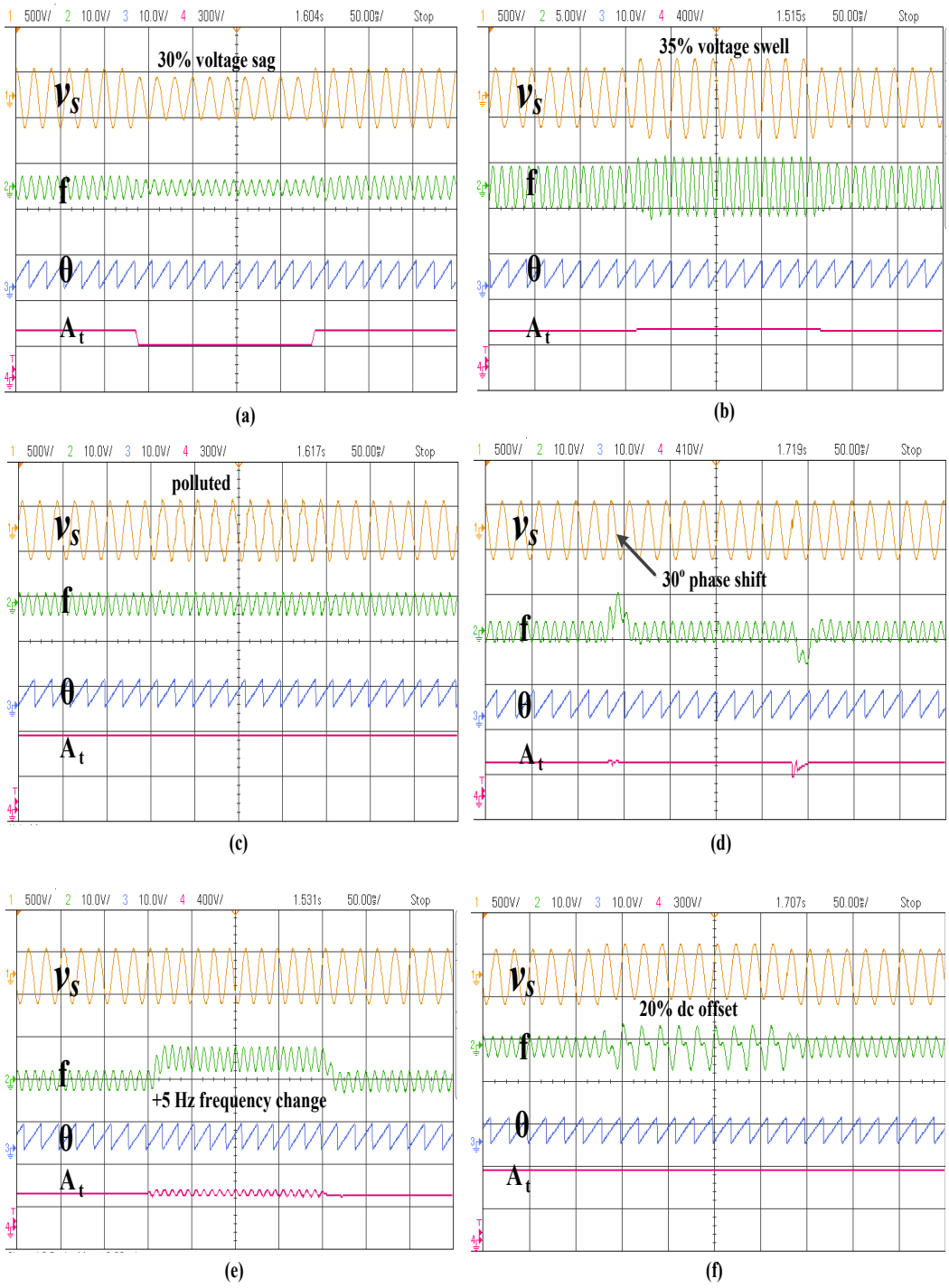


Fig. 5.10: Experimental results of MSRF PLL at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset

5.5.2 Simulation and Experimental Analysis of FO-LP MSRF-PLL

The simulated and experimental results are shown in Fig. 5.11 and Fig. 5.12 under grid abnormalities like (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30^{o} phase shift (e) +5 Hz frequency change and (f) 20% DC-offset for analysing the dynamic performance of the fractional order MSRF PLL (FO-LP MSRF PLL). These two figures give the information about supply voltage, in volts, fundamental frequency in Hz, phase angle in rad and amplitude of supply voltage in volts. Fig. 5.11: (a) and Fig. 5.12: (a) give the simulated and experimental dynamic performance under 30% voltage sag. It is observed that there is no prominent change in the phase angle although the supply voltage and amplitude of the voltage source show a dip in voltage by 30% of supply voltage in both the simulation and experimental results. There is slight dip in the frequency response during the disturbance. Similarly, Fig. 5.11: (b) and Fig. 5.12: (b) show the simulated and experimental dynamic performance under 35% voltage swell. Again, under this disturbance it is observed that no change in phase angle takes place under this disturbance. There is slight swell in the frequency response during the disturbance. The supply voltage and its magnitude show swell in their signal response. Fig. 5.11: (c) and Fig. 5.12: (c) give the simulated and experimental dynamic performance under polluted voltage supply. The frequency response shows peak fluctuation of 52.34Hz at 0.203s and attains a normal value of 50Hz after 0.233s in the simulated result while the experimental result shows smoother response. The simulated results shown in Fig. 5.11: (d) gives the dynamic performance under 30^{o} phase shift in grid voltage supply. It shows frequency fluctuation during disturbance time period and the frequency raised to a peak of 57.56Hz at 0.211s which attains its normal condition after 0.26s. These simulation results are validated by the experimental results shown in Fig. 5.12: (d). The dynamic performance analysis when the grid voltage supply undergoes a disturbance of +5Hz frequency change is shown in Fig. 5.11: (e) and Fig. 5.12: (e). It is observed that the peak of frequency overshoot is 57.34Hz at 0.22s and dies down at 0.24s in simulated results shown in Fig. 5.10: (e) and this result is validated by the experimental results shown in Fig. 5.12: (e). Fig. 5.11: (f) shows the simulation results when the grid voltage is exposed to 20% DC-offset. During the time period of 0.2s-0.4s the estimated frequency shows fluctuations

and they are validated by the experimental results shown in Fig. 5.12: (f). Therefore simulation and experimental results shown in Fig. 5.11 and Fig. 5.12 respectively validate each other.

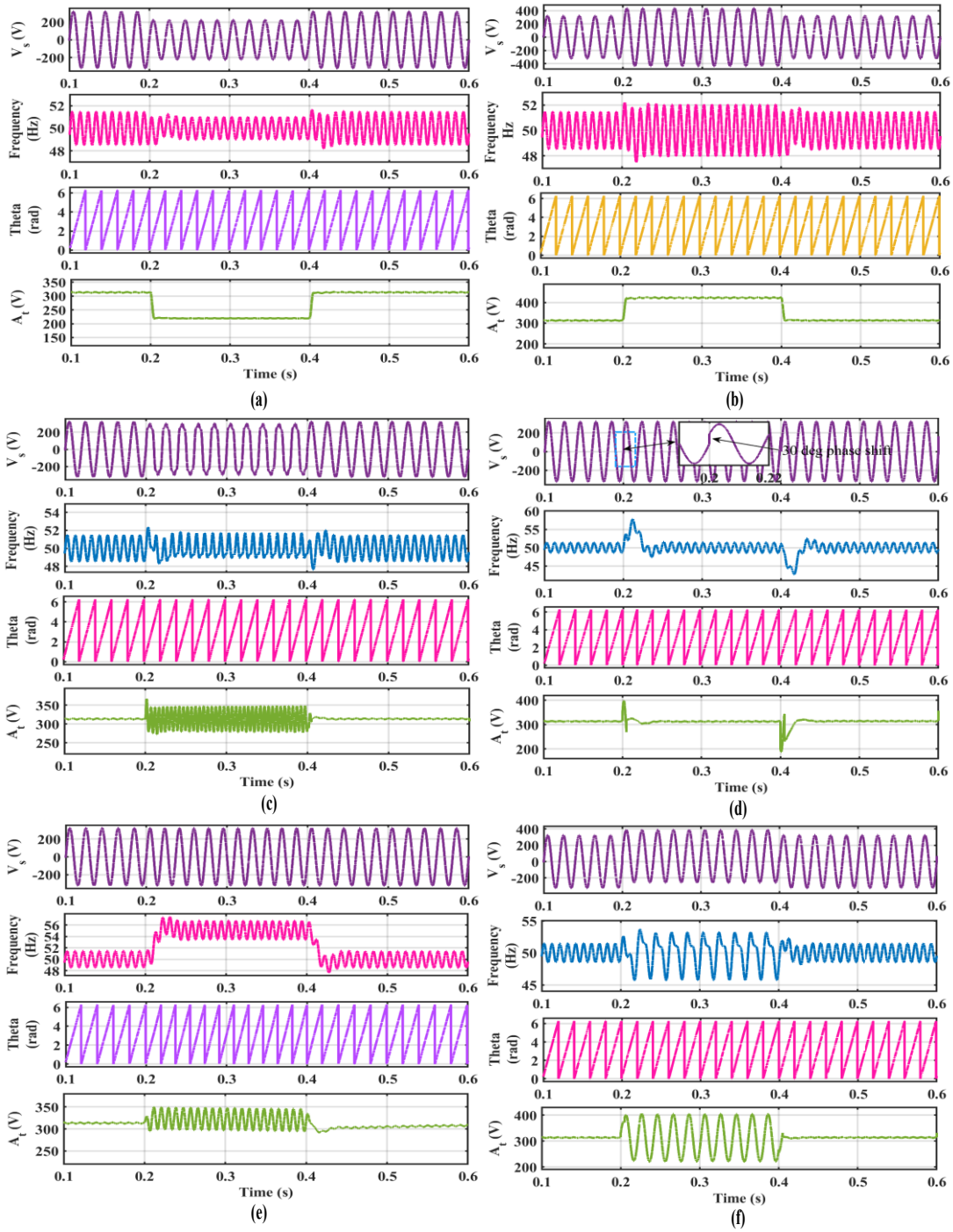


Fig. 5.11: Simulation results of FO-LP MSRF PLL at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset

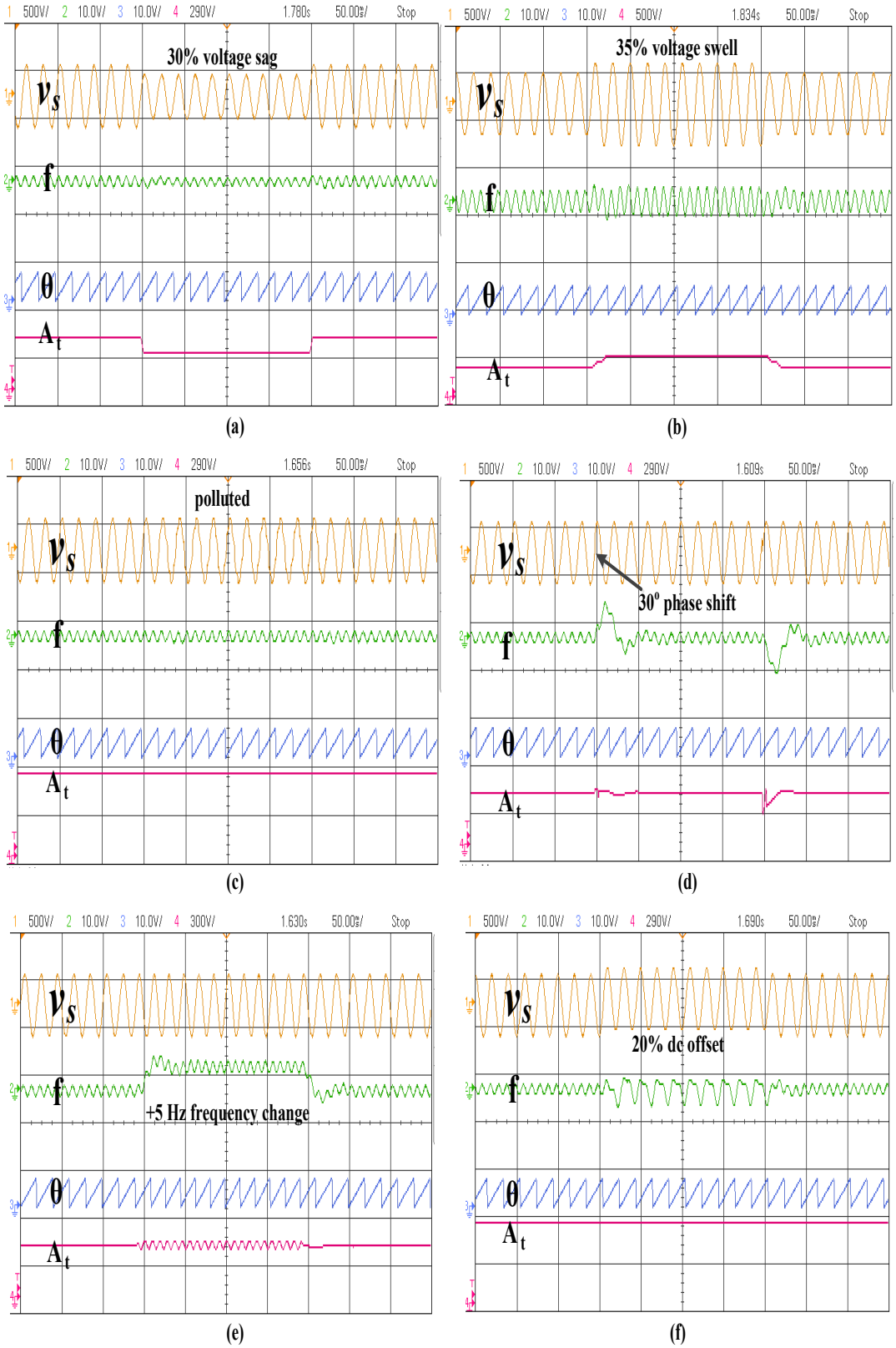


Fig. 5.12: Experimental results of FO-LP MSRF PLL at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset

5.2.3 Simulation and Experimental Analysis of FO-LPFO-PI MSRF-PLL

The simulation and experimental results for analysing the dynamic performance of fractional order first order low pass filter and loop filter MSRF-PLL (FO-LPFO-PI MSRF- PLL) for different grid abnormal conditions like (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30^{o} phase shift (e) +5 Hz frequency change and (f) 20% DC-offset are shown in Fig. 5.13 and Fig. 5.14. The dynamic performance analysis is done by considering supply voltage in volts (V), estimated frequency in hertz (Hz), phase angle in rad and voltage amplitude, in volts (V). Fig. 5.13: (a) shows the simulated performance analysis under 30% input voltage sag during time interval of 0.2s to 0.4s, while Fig. 5.14: (a) validate the performance analysis experimentally. The estimated frequency and phase angle remain unaffected though amplitude of grid input voltage is dropped by 30% during disturbed time interval. Fig. 5. 13: (b) gives the simulated dynamic performance under 35% input grid voltage swell during disturbed interval. The frequency is well tracked while the input voltage amplitude shows an increased by 35% of the input supply voltage during disturbance period. There is no change in the estimated phase angle and Fig. 5.14: (b) validates this result experimentally. Fig. 5.13: (c) gives the simulated dynamic performance under polluted input grid voltage supply. The supply voltage is non-sinusoidal during the disturbed time period of 0.2s–0.4s owing to the harmonics content. The computed input voltage amplitude shows some oscillations while frequency and phase angle remain unaffected. Fig. 5.14: (c) validates the simulated results experimentally. Fig. 5.13: (d) gives the simulated dynamic performance under 30^{o} phase shift. The estimated frequency shows a peak overshoot of 53.65Hz at 0.213s. The overshoot settles down at 0.26s. Fig. 5.14: (d) validate simulation results experimentally. Fig. 5.13: (e) gives the simulated dynamic performance under +5 Hz frequency change. The frequency response shows +5Hz frequency change and no prominent change in phase angle. Fig.5.14: (e) shows the experimental results under +5Hz frequency change. Under this disturbance the frequency response also shows +5hz change with no prominent change in phase angle validating its simulated results in Fig. 5.13: (e). Fig. 5.12: (f) gives the simulated dynamic performance under 20% DC-offset during time interval of 0.2sto 0.4s. The presence of DC offset is seen in grid

supply voltage and its amplitude responses. Moreover, distortion in frequency signal response is observed though the phase angle does not show any prominent change. Fig. 5.14: (f) shows the experimental results under 20% DC offset grid disturbance. The supply voltage response shows the presence of DC offset which leads to distortion in the frequency response. No prominent change in phase angle is seen, validating the simulated result in Fig. 5.13: (f).

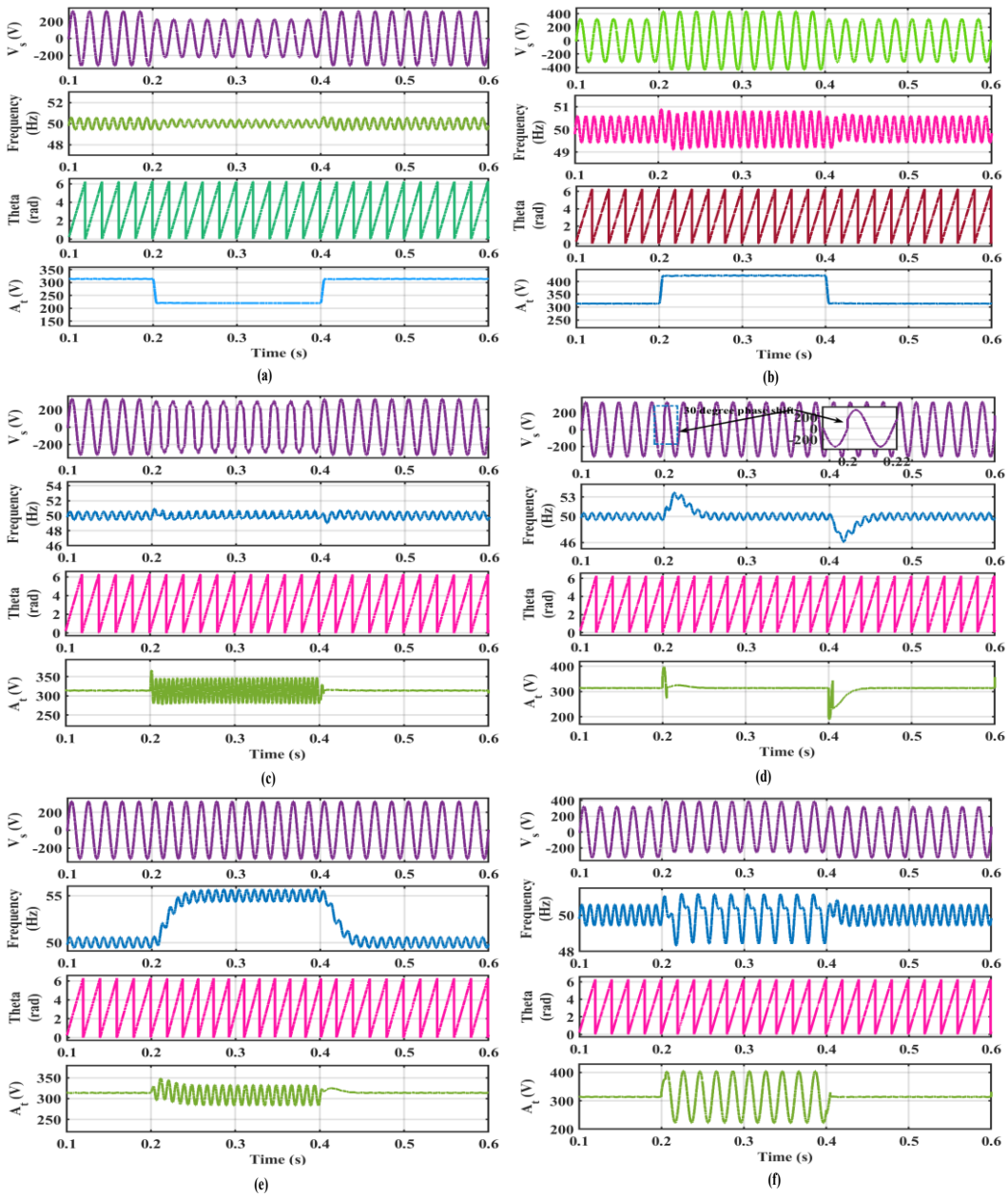


Fig. 5.13: Simulation results of FO-LPFO-PI MSRF PLL at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset

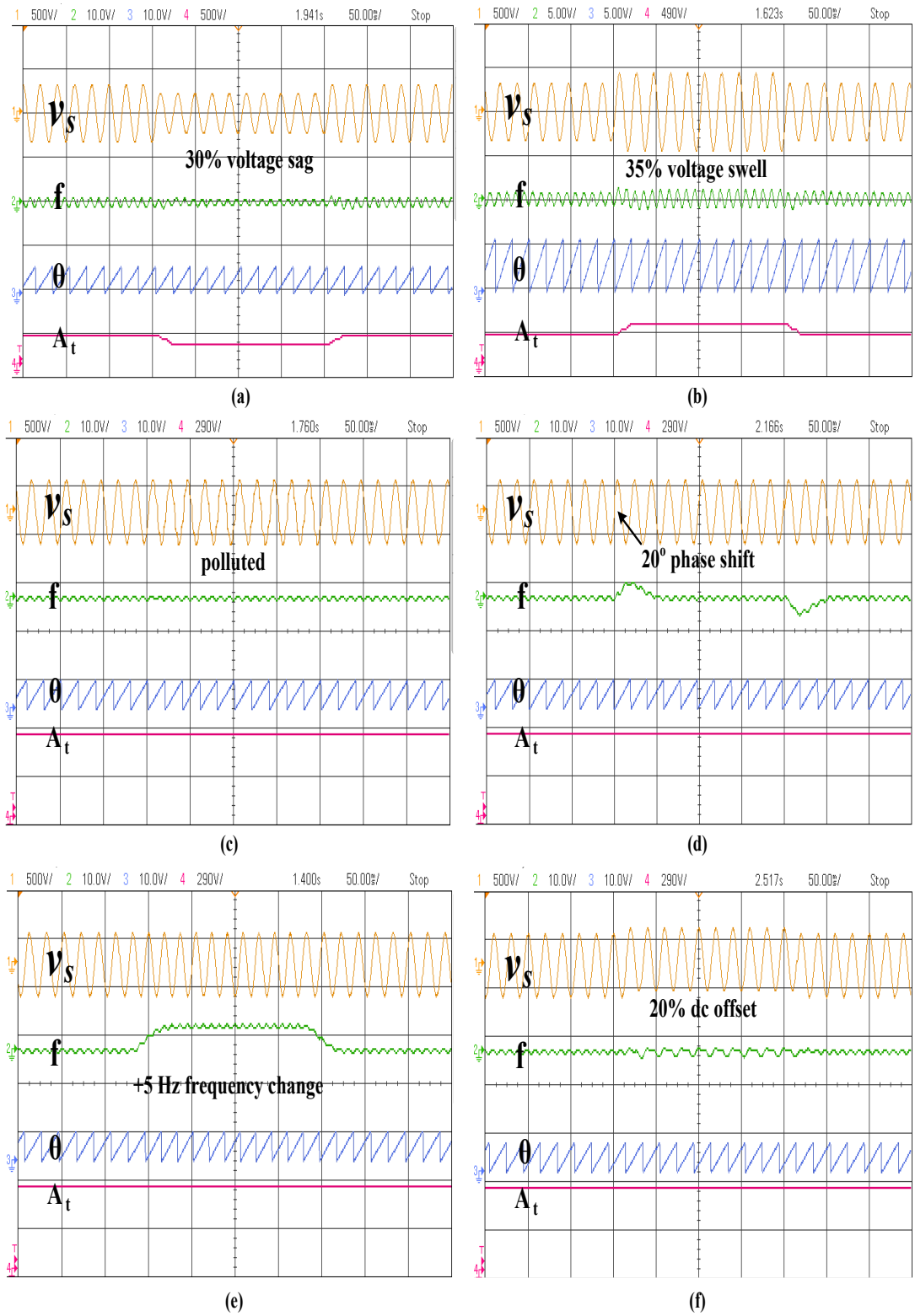


Fig. 5.14: Experimental results of FO-LPFO-PI MSRF PLL at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% dc offset

5.5.4 Comparative Performance Analysis of Simulation and Experimental Results

A fair comparison of the simulated and experimental dynamic performance analysis of the three PLLs under grid abnormalities like (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30^{o} phase shift (e) +5 Hz frequency change and (f) 20% DC-offset are discussed in Fig. 5.15: (i) and (ii) respectively. The comparisons of MSRF-PLL, FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL are performed during 0.2s-0.4s. Fig. 5.15: (i) (a) gives the comparison of the estimated frequencies of simulation for the three PLLs (MSRF-PLL, FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL) when the input grid voltage undergoes 30% voltage sag during the time interval of 0.2s-0.4s. MSRF-PLL shows peak overshoot of 51.82 Hz at 0.22s and settles down at 0.24s, FO-LP MSRF-PLL gives a frequency overshoot of 51.25Hz at 0.22s while FO-LPFO-PI MSRF-PLL gives smallest frequency overshoot of 50.45Hz at 0.22s. Hence the best dynamic performance is seen in FO-LPFO-PI MSRF-PLL in terms of frequency overshoot. Fig. 5.15: (i) (b) gives the dynamic performance comparison of the estimated frequencies when grid voltage undergoes 35% voltage swell during 0.2s to 0.4s. MSRF-PLL shows the highest frequency overshoot of 53.21 Hz at 0.232s and settles down at 0.25s, FO-LP MSRF-PLL 52.14 Hz at 0.23s while FO-LPFO-PI MSRF-PLL gives smallest frequency overshoot of 50.9 Hz at 0.203s and its settling time is 0.22s.Thus, it is observed that the performance of FO-LPFO-PI MSRF-PLL surpasses that of integral and fractional order MSRF-PLL and FO-LP MSRF-PLL under grid voltage swell condition respectively. This analysis is validated by the experimental results shown in Fig. 5.15: (ii) (b). Fig. 5.15: (i) (c) shows the comparison of frequency responses under polluted grid voltage supply during 0.2s to 0.4s. MSRF-PLL shows largest oscillation in the tracked frequency among the three PLLs due to the presence of the harmonics. The FO-LPFO-PI MSRF-PLL shows better performance with lowest oscillations (50.9Hz at 0.203s) than FO-LP MSRF-PLL (52.34Hz at 0.203s) and MSRF-PLL (53.51Hz at 0.202s) under polluted grid voltage supply. Settling time of the MSRF-PLLs is about 0.25s, FO-LP MSRF- PLL is 0.23s and FO-LPFO-PI MSRF-PLL is 0.213s. These simulation results under the polluted grid voltage are validated experimentally in Figure 5.15: (ii) (c). Fig. 5.15: (i) (d) and

Fig. 5.15: (ii) (d) shows the comparative frequency responses for dynamic performance analysis of MSRF-PLL, FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL when the grid supply voltage undergoes 30^{o} phase shift during 0.2s to 0.4s. MSRF-PLL shows the highest frequency overshoot of 59.71 Hz at 0.211s which settles at 0.27s while FO-LPFO-PI MSRF-PLL gives smallest frequency overshoot of 53.6 Hz at 0.211s and the settling time is 0.25s. FO-LP MSRF-PLL shows a frequency overshoot of 57.56Hz at 0.211s which settles at 0.26s and shows moderate performance. Fig. 5.15: (ii) (d) validates the simulation results showing that FO-LPFO-PI MSRF-PLL has the lowest oscillation and fastest selling time.

Fig. 5.15: (i) (e) shows the comparison under +5 Hz step frequency shift in input voltage at 0.2s. MSRF-PLL shows the highest frequency overshoot of 59.2Hz at 0.22s which settles at 0.25s while FO-LPFO-PI MSRF-PLL gives smallest frequency overshoot of 55.6 Hz at 0.25s and it settles down at 0.26s. FO-LP MSRF-PLL shows moderate frequency overshoot of 57.34 Hz at 0.222s and it settle downs at 0.24s. This dynamic performance is validated by Fig. 5.15: (ii) (e) showing that FO-LPFO-PI MSRF-PLL gives the best performance.

Fig. 5.15: (i) (f) shows the comparison of frequency response of the integral order MSRF-PLL with fractional orders PLLs (FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL) when the grid voltage is exposed to abnormality of 20% DC-offset. MRSF PLL shows the highest frequency oscillation of 54.9Hz at 0.22s while FO-LPFO-PI MSRF-PLL shows the smallest frequency oscillation of 51.16Hz at 0.22s. FO-LP MSRF-PLL shows moderate frequency overshoot of 53.6 Hz at 0.22s. The three PLLs settles at 0.24s. These results are validated by the experimental results of frequency responses of MSRF-PLL, FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL. Hence, from all the grid abnormal conditions given in Fig. 5.15 (a) to (f) it is observed that the FO-LPFO-PI MSRF-PLL with two fractional order parameters shows minimum frequency overshoot response which is lower than that obtained with single fractional order parameter FO-LP MSRF-PLL and integer order MSRF-PLL. FO-LPFO-PI MSRF-PLL shows better settling time than the other two PLLs.

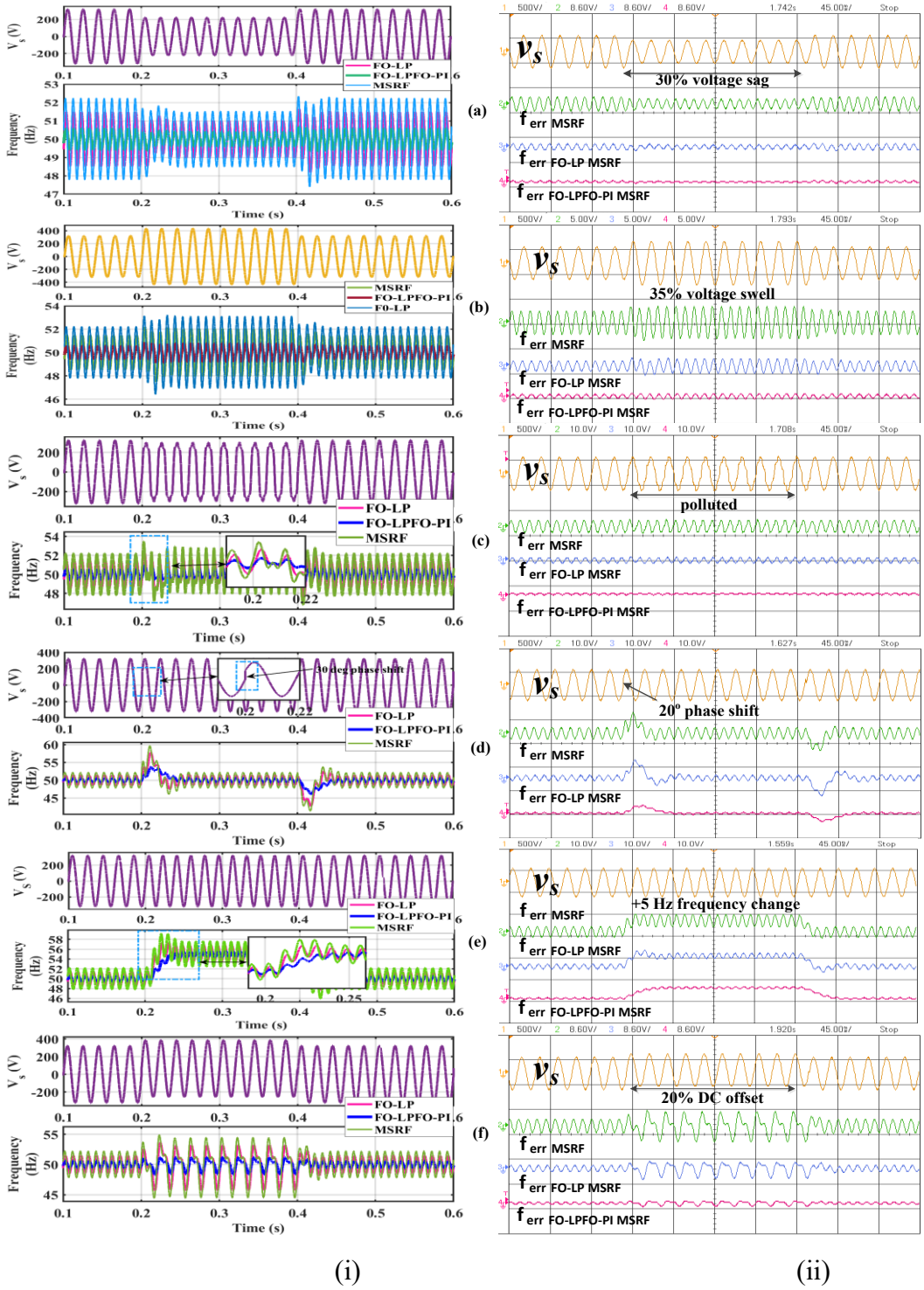


Fig. 5.15: (i) and (ii) Comparative dynamic performance analysis of simulation and experimental results of frequency response of FO-LP MSRF-PLL, FO-LPFO-PI MSRF PLL with integral order MSRF-PLL at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted voltage, (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset respectively.

A conclusive comparative performance analysis of the three PLLs is shown in Table 5.5. In this table, the frequency overshoot and settling time for integer order PLL

Table 5.5. Comparative performance analysis of MSRF-PLL, FO-LP MSRF-PLL and FO-PLFO-PI MSRF-PLL

Testing Conditions	**MSRF-PLL**	**FO-LP MSRF-PLL**	**FO-LPFO-PI MSRF-PLL**
30% grid voltage sag			
Frequency over shoot	Larger peak overshoot of 51.81 Hz	Smaller peak overshoot of 51.29 Hz	Least peak overshoot of 50.45Hz
Settling time (s)	0.05s, Slower response (within three cycles)	0.043s, Slow response (within three cycles)	0.03s, Fastest response (within two cycles)
35% voltage swell			
Frequency over shoot	Larger peak overshoot of 53.1Hz	Smaller peak overshoot of 52.14Hz	Smallest peak overshoot of 50.9 Hz
Settling time (s)	0.05s, Slow (within three cycles)	0.053s, Sluggish (within three cycles)	0.02s, Faster (within one cycle)
Polluted grid voltage			
Frequency over shoot	Largest peak overshoot of 53.5Hz	Smaller peak overshoot of 52.34Hz	Smallest peak overshoot of 50.9 Hz
Settling time (s)	0.052s, Sluggish (within three cycles)	0.033s, Slower (within two cycles)	0.013s, faster (within one cycle)
30^{o}phase angle shift			
Frequency over shoot	Largest peak overshoot of 59.71 Hz	Smaller peak overshoot of 57.6 Hz	Smallest peak overshoot of 53.61 Hz
Settling time (s)	0.07s, Sluggish (within four cycles)	0.06s, Slow (within three cycles)	0.05s, faster (within three cycles)
+5Hz Frequency shift			
Frequency over shoot	Largest peak oscillation of 59.2Hz	Smaller peak overshoot of 57.34Hz	Smallest peak overshoot of 55.6Hz
Settling time (s)	0.05s, Slower (within three cycles)	0.04s, fastest (within two cycles)	0.06s, Slowest (within three cycles)
Presence of DC-offset			
Response in frequency	Large oscillations	Small oscillations	Minimum oscillations

and the fractional-order PLLs are estimated under the considered six abnormal grid conditions. Under the testing condition30% grid voltage sag from Table 5.5, it is observed that the integral order MSRF-PLL shows the largest peak frequency overshoot and slowest settling time while FO-LP MSRF-PLL shows medium dynamic

performance and FO-LPFO-PI MSRF-PLL gives the best performance. Under 35% grid voltage swell FO-LP MSRF-PLL shows sluggish response than MSRF-PLL while FO-LPFO-PI MSRF-PLL gives the best performance. Under polluted grid, 30% phase shift and 20% DC-offset FO-LPFO-PI MSRF-PLL performs the best than the other two PLLs. FO-LPFO-PI MSRF-PLL under +5 Hz frequency change gives smallest peak overshoot but sluggish response than the other two PLLs.

5. 6 Conclusion

In this chapter, the mathematical modeling of three PLLs viz. (i) integral order MSRF-PLL, (ii) FO-LP MSRF-PLL with one fractional-order 'a' and (iii) FO-LPFO-PI MSRF-PLL with two fractional-order 'a' and 'b' coefficients is performed. The three PLLs are designed and their open-loop, closed-loop and error-loop transfer functions are mathematically developed. The open-loop and closed-loop Bode diagrams of FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL are plotted to predict optimum values of 'a' and 'b' considering PLL stability. As FO-LPFO-PI MSRF-PLL has two fractional order parameters 'a' and 'b', the Bode diagrams of FO-LPFO-PI MSRF-PLL are plotted for various values of 'a' with fixed 'b' as 1 in one case and in another case with various values of 'b' for fixed 'a' as 1. The Bode diagrams helped to optimize the fractional parameters 'a' and 'b'. The selected optimized values of fractional-order coefficients are 'a'=1.1 and 'b'=0.1 which are finally selected for the FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL.

The dynamic performance analysis for the conventional integral order MSRF-PLL and fractional-order FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL is performed under different grid abnormalities like 30% grid voltage sag and 35% grid voltage swell, 3^{rd} and 5^{th} harmonics polluted voltage, 30% phase shift, +5Hz frequency change and 20% Dc-offset voltage supply. Both the simulated and experimental comparative analysis is performed rigorously. The comparative results predict that among the integral order and fractional order PLLs, FO-LPFO-PI MSRF-PLL with two fractional-order parameters 'a' and 'b' gives the best performance results during the grid abnormalities. Moreover, this PLL is more stable as compared to FO-LP MSRF-PLL after optimizing the values of 'a' and 'b' parameters.

Chapter 6

DESIGN AND PERFORMANCE ANALYSIS OF HYBRID PHASE LOCKED LOOPS

6.1 General Introduction

Grid-connected power electronic converters must be synchronized with the power grid in order to provide reliable operation, precise control, and grid code compliance. Phase-locked loop (PLL) techniques are frequently used to estimate the grid voltage phase, frequency, and amplitude under different operating situations. Conventional PLL like Synchronous Reference Frame (SRF), Second Order Generalised Integrator (SOGI), Least Mean Square LMS PLLs function well under optimal grid circumstances. However, under harmonics, voltage imbalances, frequency drifting, presence of noise and depending on the type and complexity of the PLLs used, the performance in tracking voltage amplitude, phase angle and frequency deteriorates. The estimated phase angle, frequency, and amplitude shows oscillations leading to enhanced power quality issues and these problems cannot be solved by a conventional PLL. Hence, modified PLL approaches like SOGI PLL and adaptive systems based on LMS algorithms have been developed to overcome these restrictions. Therefore, it is important to design such synchronizing techniques that must be able to eliminate DC-offset as well as harmonic content in supply grid voltage for efficient operation of power system. Pre-filtering with an adaptive filter based on Least Mean Square (LMS) technique and use of orthogonal signal generator such as SOGI techniques to improve PLL response under abnormal grid conditions is reported in [35]. With optimized gain settings, LMS shows benefits over SOGI involving a frequency-independent bandwidth, low or moderate computational requirements, and ease of application [135]. The two LMS filters cascaded together greatly enhance the attenuation of harmonics better than cascaded- SOGI [45], despite having an overall slower dynamic response. A novel cascaded hybrid PLL comprising LMS and SOGI PLLs has been developed in this chapter for analysing the dynamic performance under grid abnormalities.

This chapter discusses the design and modelling of modified phase locked loop like cascaded Least Mean Square (CLMS), cascaded Second Order Generalised Integrator (CSOGI) and a novel cascaded hybrid Least Mean Square and Second Order Generalised Integrator (H-LMS-SOGI) phase locked loop as an adequate filter structures and precise synchronization technique for interfacing converters to the grid to monitor the phase, amplitude, and frequency of the supply voltage. These PLLs are studied for testing the dynamic performance under adverse grid conditions like 30% voltage sag and 35% swell, +5 Hz frequency change, 30^{o} phase shift, 20% dc-offset and polluted environment. It also discusses the stability analysis of the H-LMS-SOGI PLLw.r.t CLMS PLL, and CSOGI PLL through the bode plots and pole-zero map.

6.2 Design and Mathematical Modelling of Cascaded PLLs

Design and mathematical modelling of the algorithms of three cascaded PLLs (i) Cascaded Least Mean Square (CLMS) PLL (ii) Cascaded Second Order Generalised Integrator (CSOGI) PLL and (iii) Cascaded hybrid Least Mean Square and Second Order Generalised Integrator (H-LMS-SOGI) PLL are discussed in detail and their transfer function are developed for further analysis of the steady state stability.

6.2.1 Cascaded Least Mean square (CLMS) based PLL

A cascaded least mean square (CLMS) PLL is formed by combining two identical single LMS algorithms in cascaded form to provide the harmonic attenuation of the grid voltage and extract the fundamental grid frequency and phase angle. The block diagram shown in Figure 6.1 represent Cascaded Least Mean Square (CLMS) PLL. The learning mechanism of LMS is based on stochastic gradient and it exhibits adaptive qualities by continuously updating the weights to minimize the estimated steady state error [160]. Fig. 6.1 (a) and (b) shows the schematic block diagram of a single LMS structure and block diagram of cascaded LMS (CLMS). For LMS structure the reference input signal is denoted by x*(k) where ‘k’ denotes the number of iterations, $v_s(k)$ is the desired input signal and the estimated output signal is denoted by v(k) which is obtained from the LMS filter. The error signal, $e_{ser}(k)$ is another output signal obtained by taking the difference between the estimated output and

desired input signals. In the CLMS PLL the error signal, '$e_{ser}(k)$' of the first LMS (LMS1) is given as the desired input signal of the second LMS (LMS2). The estimated output of LMS2 is denoted by '$v_1(k)$'. The error signal from LMS2 is denoted as $e_{ser1}(k)$. The reactive voltage component from LMS2 is fed to the PI controller of the CLMS PLL and the output of VCO is the estimated phase angle/frequency.

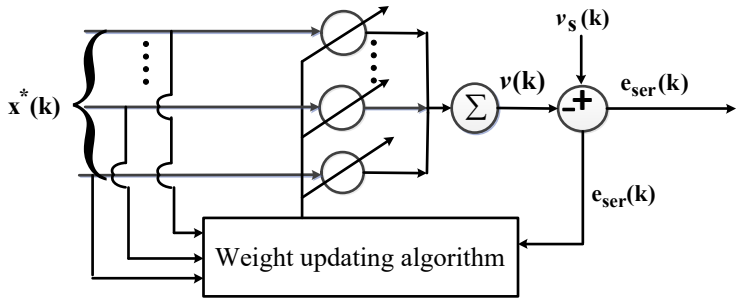


Fig. 6.1 (a): Weight updating diagram of LMS filter

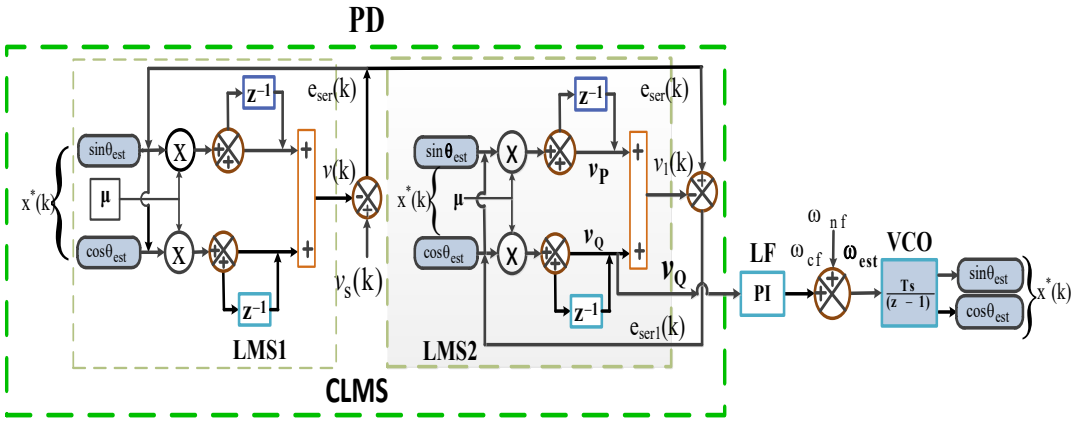


Fig. 6.1 (b): Block diagram of cascaded LMS (CLMS) PLL

The steady state error signal of LMS2 is expressed as

$$e_{ser1}(k) = v_1(k) - e_{ser}(k) \tag{6.1}$$

The cost function ($\xi(k)$), is defined by the error signal and it is expressed as

$$\xi(k) = E[e_{ser1}^2(k)] = E[(v_1(k) - e_{ser}(k))^2] \tag{6.2}$$

The input coefficient matrix for N samples is represented as

$$\overrightarrow{x^*}(k) = [x^*(k)x^*(k-1)x^*(k-2)\ x^*(k-3) \dots\dots\dots x^*(k-N+1)]^T$$

$$= [sin\theta_{est}\ cos\theta_{est} \quad \sin(N-1)\theta_{est}\ \cos(N-1)\theta_{est} \quad sinN\theta_{est}\ cosN\theta_{est}\ ]^T \tag{6.3}$$

The phase angle ' θ_{est}' is obtained as outputs from VCO of LMS PLL after modulating it. The weight coefficient in matrix form at time 'k' is expressed as

$$\overrightarrow{\mathrm{W}}^{\mathrm{T}}(\mathrm{k}) = [\mathrm{W}_0(\mathrm{k})\mathrm{W}_1(\mathrm{k}) \ldots\ldots\ldots\ldots\ldots \mathrm{W}_{\mathrm{N}-1}(\mathrm{k})] \tag{6.4}$$

The estimated output of the LMS in the matrix form is expressed as

$$v_1(\mathrm{k}) = \mathrm{W}^{\mathrm{T}}(\mathrm{k})\overrightarrow{\mathrm{X}^*}(\mathrm{k}) \tag{6.5}$$

$$v_1(k) = \sum_{i=0}^{N-1} V_{Ai}\sin(\omega k T_s + \varphi_i) \tag{6.6}$$

$$= \sum_{i=0}^{N-1}(V_{Ai}\cos\varphi_i \sin\omega k T_s + V_{Ai}\sin\varphi_i \cos\omega k T_s) \tag{6.7}$$

$$= \sum_{i=0}^{N-1}(v_{Pi}\sin i\omega k T_s + v_{Qi}\cos i\omega k T_s) \tag{6.8}$$

Here in the above equations ' V_{Ai}' is the amplitude of the i[th] voltage signal with $(\omega k T_s + \varphi_i)$ as its phase angle. The active and reactive voltage components can be written as $v_{Pi} = (V_{Ai}\cos\varphi_i)$ and $v_{Qi} = (V_{Ai}\sin\varphi_i)$ respectively. The amplitude of the voltage signal considering dq-axis component is expressed as

$$V_{PQA}(k) = \sqrt{(v_{Pi})^2 + (v_{Qi})^2} \tag{6.9}$$

Weight updating of the LMS2 can be modelled using the Steepest Descent Approach as

$$W(k+1) = W(k) + \mu e_{ser1}(k)X^*(k) \tag{6.10}$$

The active and reactive component of the voltage while updating the weight from equation (6.10) can be expressed in equations (6.11) and (6.12)

$$W_P(k+1) = W_P(k) + \mu e_{ser1}(k)\sin\theta_{est} \tag{6.11}$$

$$W_Q(k+1) = W_Q(k) + \mu e_{ser1}(k)\cos\theta_{est} \tag{6.12}$$

The learning rate or the convergence factor of an LMS filter is represented by ' μ' and ' T_s' is the sampling time considered for k=1,2,3, 4,……N samples. The reactive

component of the voltage is passed to the proportional plus integrator (PI) controller which is used as loop filter (LF). The output from PI is the controlled voltage given by ω_{cf}. The estimated phase angle, θ_{est} , and estimated frequency ω_{est} is obtained by adding fundamental frequency, ω_{nf} to ω_{cf}. After modulating the outcome from voltage-controlled oscilloscope (VCO) the estimated phase angle is obtained. The reference input signals are obtained by multiplying it with sine and cosine functions. The estimated frequency and phase angle with T_s as the sampling time can be expressed as

$$\omega_{est} = \omega_{cf} + \omega_{nf} \tag{6.13}$$

$$\theta_{\mathrm{est}} = \frac{\mathrm{T_s}}{\mathrm{z-1}}\omega_{est} \tag{6.14}$$

The open loop transfer function of single LMS in z transform with 'T_s' as the sampling time is

expressed as from (3.44) and (3.45)

$$T_{LMS}(z) = \frac{output}{error} \tag{6.15}$$

$$= \frac{\mu(z\cos\omega_{est}T_s-1)}{z^2-2z\cos\omega_{est}T_s+1} \tag{6.16}$$

The closed loop transfer function of LMS with T_s as the sampling time is expressed as [69]

$$T_{clLMS}(z) = \frac{output}{input} \tag{6.17}$$

$$= \frac{T_{LMS}(z)}{1+T_{LMS}(z)} \tag{6.18}$$

$$= \frac{\mu(z\cos\omega_{est}T_s-1)}{z^2-2z\cos\omega_{est}T_s+1} * \frac{1}{1+[\mu(z\cos\omega_{est}T_s-1)/z^2-2z\cos\omega_{est}T_s+1]} \tag{6.19}$$

$$= \frac{[\mu(z\cos\omega_{est}T_s-1)]}{[z^2-2z\cos\omega_{est}T_s+1]+[\mu(z\cos\omega_{est}T_s-1)]} \tag{6.20}$$

$$= \frac{[\mu(z\cos\omega_{est}T_s-1)]}{z^2-2(1-\mu/2)\,z\cos(\omega_{est}T_s)+(1-\mu)} \tag{6.21}$$

Hence the open loop transfer function of the cascaded LMS (CLMS) structure can be expressed as

$$T_{CLMS}(z) = [T_{LMS}]^2 = \left[\frac{\mu(z\cos\omega_{est}\,T_s - 1)}{z^2 - 2z\cos\,\omega_{est}\,T_s + 1}\right]^2 \tag{6.22}$$

The closed loop transfer function of the cascaded LMS (CLMS) structure considering the active component of the input voltage source in the z transform is obtained as

$$T_{clCLMS}(z) = \frac{T_{CLMS}(z)}{1 + T_{CLMS}(z)} = \left[\frac{\mu(z\cos\omega_{est}T_s - 1)}{z^2 - 2\left(1 - \frac{\mu}{2}\right)z\cos(\omega_{est}T_s) + (1 - \mu)}\right]^2 \tag{6.23}$$

6.2.2 Design of Cascaded Second Order Generalised Integrator (CSOGI) based PLL

The block diagrams of the single second order generalised integral (SOGI) structure and cascaded second order generalised integral (CSOGI) PLL are shown in Fig. 6.2 and Fig. 6.3 respectively. Fig. 6.2 structure of SOGI orthogonal signal generator (OSG) has 'k', as the gain of phase detector. SOGI OSG generates both in phase voltage signal 'v_α' and out of phase voltage signal 'v_β' signals from the supply voltage ' v_s'. The two orthogonal signals are converted in dq reference frame voltage components by Park's transformation. The cascaded SOGI (CSOGI) PLL consists of two identical blocks of single SOGI structure in cascaded form. CSOGI structure represents the phase detector part of the PLL. The grid supply voltage, v_s is fed to the first SOGI block and its output $v_\propto$,is fed as the input to the second SOGI block. The orthogonal outputs $v_\propto$ and v_β from the second SOGI structure are fed to the embedded synchronous reference frame structure of the PLL to obtain the estimated frequency and phase angle, θ of the PLL. In CSOGI PLL, $\omega_e^{/}$ is the estimated resonant angular frequency of the cascaded SOGI (CSOGI) PLL which is fed back to the first SOGI structure.

The angular fundamental grid frequency is marked as $\omega_{ff} = 2\pi f$ with f = 50Hz and this frequency is also the resonant frequency. The CSOGI structure is used

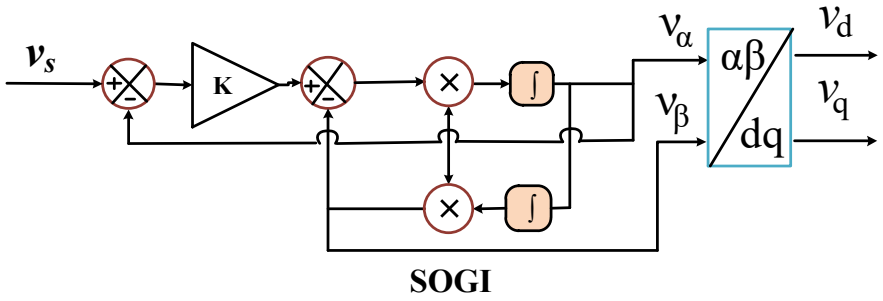


Fig. 6.2 schematic diagram of single SOGI structure

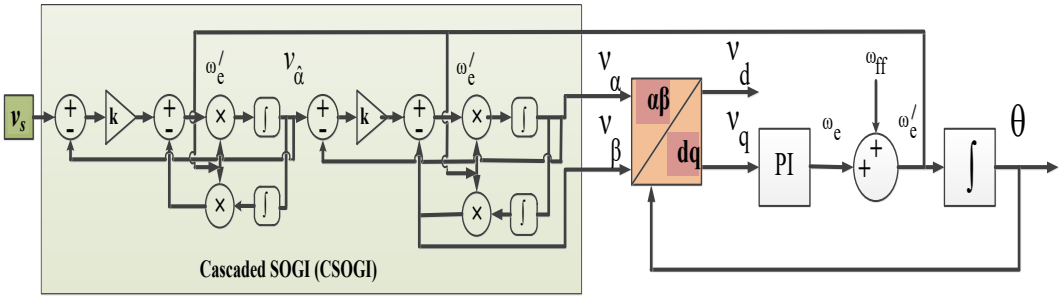


Fig. 6.3 (b) Block diagram of cascaded SOGI (CSOGI) PLL

as phase detector (PD) of the PLL. The in-phase and quadrature signals from the second SOGI structure undergo Park transformation to obtain dq-axis components, 'v_d' and 'v_q'. The reactive component, v_q is further fed to PI controller of the embedded PLL to obtain the required phase angle and frequency of the CSOGI PLL. For simplifying the mathematical modelling, a single SOGI PLL is initially considered and then cascaded combination is discussed. The conventional single phase single SOGI is an orthogonal signal generator structure which generates two signals, '$v_\propto$' and 'v_β' which are orthogonal to one another. The closed loop transfer functions of a single SOGI structure are represented as

$$H_{\alpha SOGI}(s) = \frac{k\omega_e' s}{s^2 + k\omega_e' s + \omega_e'^2} \tag{6.24}$$

$$H_{\beta SOGI}(s) = \frac{k\omega_e'}{s^2 + k\omega_e' s + \omega_e'^2} \tag{6.25}$$

The closed loop transfer functions of the CSOGI structure can be expressed as

$$H_{\alpha SOGI}(s) = \left[\frac{k\omega_e^{/}s}{s^2+k\omega_e^{/}s+\omega_e^{/2}}\right]^2 \tag{6.26}$$

$$H_{\beta SOGI}(s) = \frac{k(\omega_e^{/})^3 s}{(s^2+k\omega_e^{/}s+\omega_e^{/2})^2} \tag{6.27}$$

The closed loop transfer function given by equation (6.24) represents a band pass filter (BPF) which has zero phase shift and the transfer function given by equation (6.25) represents a low pass filter with a phase difference of 90° under unity gain at resonant frequency of single SOGI. The equations (6.26) represent the band pass filter (BPF) and (6.27) represents low pass filter of cascaded SOGI (CSOGI). The bandwidth of (6.24) and (6.26) is decided by the damping factor 'k' so its correct value plays an important role in performance of SOGI structure. Moreover, the resonant frequency is determined by the value of 'k', which must be kept low to get a greater filtering effect. Similarly, a lower value of 'k' provides a stronger efficient filtering effect can be seen as in (6.25) but with longer reaction time. The value of 'k' is adjusted to enhance the transient response of CSOGI PLL. In CSOGI structure increase in k gives improved filter bandwidth which enables quick response at the expense of filtering ability. The continuous operation of SOGI structure when used for digital hardware implementation needs to be discretized. The most popular method of obtaining discretization is the Euler method where the discrete lime integrator of '$\frac{1}{s}$' is approximated as $T_s \frac{z^{-1}}{1-z^{-1}}$ by Forward Euler method and as $T_s \frac{1}{1-z^{-1}}$ by Backward Euler method where T_s is the sampling time. For a fixed 'T_s' at nominal frequency 50 Hz the Forward and Backward Euler methods are not able to create a phase shift of $\frac{\pi}{2}$ °. Therefore, the advanced method, like Trapezoidal method for discretization is used where the integrator or '$\frac{1}{s}$' is approximated by $\frac{T_s\,(1+z^{-1})}{2\,(1-z^{-1})}$. Here T_s is the sampling time and after discretizing equations (6.24) and (6.25) by Trapezoidal method can be expressed as

$$H_{\alpha CSOGI}(z)|_{s=\frac{2(z-1)}{T_s(z-1)}} = \frac{k\omega_e^{/}2(z-1)/T_s(z+1)}{\{2(z-1)/T_s(z+1)\}^2+\frac{kk\omega_e^{/}2(z-1)}{T_s(z+1)}+\omega_e^{/2}} \tag{6.28}$$

$$H_{\beta CSOGI}(z)\big|_{s=\frac{2(z-1)}{T_s(z-1)}} = \frac{k\omega_e'^2}{\{2(z-1)/T_s(z+1)\}^2+\frac{kk\omega_e'^{2(z-1)}}{T_s(z+1)}+\omega_e'^2} \tag{6.29}$$

Discretizing CSOGI PLL, equations (6.28) and (6.29) can be re-expressed as (6.30) and (6.31) respectively.

$$H_{\alpha SOGI}(z)\big|_{s=\frac{2(z-1)}{T_s(z-1)}} = \left[\frac{k\omega_e'^{2(z-1)/T_s(z+1)}}{\{2(z-1)/T_s(z+1)\}^2+\frac{kk\omega_e'^{2(z-1)}}{T_s(z+1)}+\omega_e'^2}\right]^2 \tag{6.30}$$

$$H_{\beta SOGI}(z)\big|_{s=\frac{2(z-1)}{T_s(z-1)}} = \frac{k\omega_e'^{2(z-1)/T_s(z+1)}}{\left(\{2(z-1)/T_s(z+1)\}^2+\frac{kk\omega_e'^{2(z-1)}}{T_s(z+1)}+\omega_e'^2\right)^2} \tag{6.31}$$

The transfer functions shown in (6.30) and (6.31) represent a band pass filter (BPF) with zero phase delay and low pass filter with phase difference of 90^o under unity gain of CSOGI PLL in discretized form.

6.2.3 Design of Cascaded hybrid Least Mean Square Second Order Generalised Integrator (H-LMS-SOGI) based PLL

The cascaded hybrid least mean square second order generalised integrator (H-LMS-SOGI) PLL is formed by cascading a single LMS and a SOGI structure which is then combined with normal typical SRF PLL to obtain the estimated phase angle and frequency of a grid voltage. The block diagram of the cascaded H-LMS-SOGI PLL is shown in Fig. 6.3. The estimated output voltage containing the minimised mean error from the LMS structure is passed as an input to the SOGI structure which then creates two orthogonal voltage signals. These in phase and out of phase voltage signals are transformed into the rotating dq-reference frame voltage signal by Parks' transformation. The reactive voltage components 'v_q' is passed to the PI controller which is a loop filter in the PLL. The output from VCO is the estimated phase angle or frequency. The cascaded H-LMS-SOGI PLL is said to be locked when the estimated frequency is equal to the input frequency. In Fig. 6.3, let 'v_s' be the grid voltage signal containing disturbances like dc offset, 'v_{dcoff}' and the harmonics 'v_h'. Let '$v(k)$' be the estimated output grid voltage signal and 'e_{ser}' be the estimated steady state error of LMS; '$W(k)$' be the weight coefficient matrix and '$x(k)$' be the unit input

coefficient matrix of the reference input signal. The steady state error signal of the LMS is expressed as

$$e_{ser}(k) = v_s(k) - v(k) \tag{6.32}$$

The unit input coefficient matrix for N samples is represented as

$$\vec{x}(\mathrm{k}) = [\mathrm{x(k)x(k-1)x(k-2)\ x(k-3)} \ldots\ldots\ldots \mathrm{x(k-N+1)}]^{\mathrm{T}}$$

$$= [sin\theta \quad cos\theta \quad \ldots \quad \sin(N-1)\theta \quad \cos(N-1)\theta \quad \sin N\theta \quad cosN\theta\ ]^{T} \tag{6.33}$$

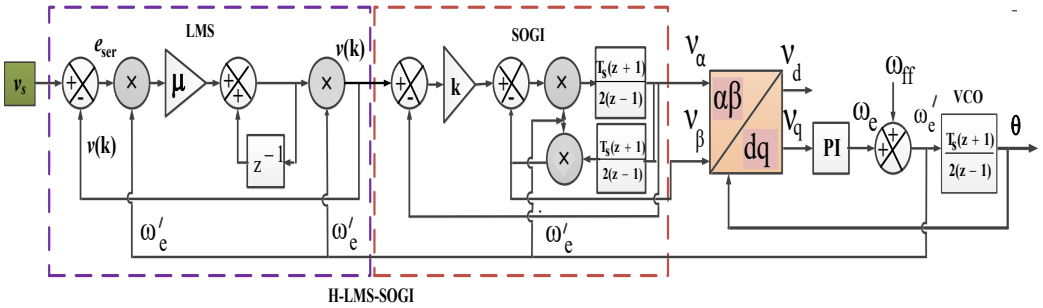


Fig. 6.4: Block diagram of H-LMS-SOGI PLL

The weight coefficient in matrix form at instant 'k' is expressed as

$$\overrightarrow{\mathrm{W}}^{\mathrm{T}}(\mathrm{k}) = [\mathrm{W_0(k)W_1(k)} \ldots\ldots\ldots\ldots \mathrm{W_{N-1}(k)}] \tag{6.34}$$

angle Weight updating of the LMS can be expressed as

$$W(k+1) = W(k) + \mu e_{ser}(k)x(k) \tag{6.35}$$

where 'μ' is the learning rate or the convergence factor of an LMS filter structure.

The estimated output of the LMS in the matrix form is expressed as

$$v(\mathrm{k}) = \mathrm{W^T(k)}\overrightarrow{\mathrm{X^*}}(\mathrm{k}) \tag{6.36}$$

$$v(k) = \sum_{i=0}^{N-1} V_{Ai}\sin(i\omega kT_s + \varphi_i) \tag{6.37}$$

where 'V_{Ai}' is the amplitude of the ith voltage signal with $(\omega kT_s + \varphi_i)$ as its phase.

The open loop transfer function of H-LMS-SOGI PLL can be obtained as

$$\mathrm{G_{olH-LMS-SOGI}(z) = G_{olLMS}(z) * G_{olSOGI}(z)}$$

$$= \left(\frac{\mu\,(\mathrm{z}\cos\omega_e'\,T_s - 1)}{\mathrm{z^2 - 2z}\cos\omega_e'\,T_s + 1}\right)\left(\frac{x(\mathrm{z^2} - 1)}{4(\mathrm{z}-1)^2 + \mathrm{y(z}+1)^2}\right)$$

$$= \left(\frac{\mu x\left((\cos\omega_e' T_s) z^2 - (1 + \cos\omega_e' T_s) z + 1 \right)}{Mz^3 + BMz^2 + BMz + M^2} \right) \tag{6.38}$$

where $x = 2kT_s\omega_e'$, $y = (\omega_e' T_s)^2$, $M = 4 + y$ and $B = 1 - 2\cos\omega_e' T_s$

The closed loop transfer function of H-LMS-SOGI PLL from (6.28) can be expressed as

$$H_{clH\text{-}LMS\text{-}SOGI}(z) = \frac{G_{olH - LMS - SOGI}(z)}{1 + G_{olH - LMS - SOGI}(z)}$$

$$= \left(\frac{\mu(z\cos\omega_e' T_s - 1)}{z^2 - 2(1 - \mu/2) z\cos\omega_e' T_s + (1 - \mu)} \right) \left(\frac{ky(z + 1)^2}{(4 + x + y)z^2 - 2(y + 4)z + (y - x)} \right) \tag{6.39}$$

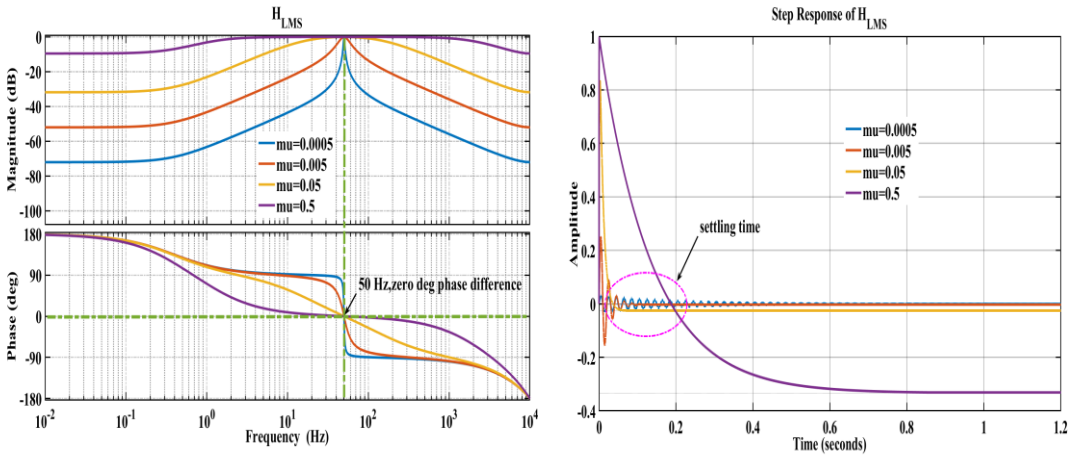
where $x = 2kT_s\omega_e'$, $y = (\omega_e' T_s)^2$

6.3 Stability Analysis of the System

This section discusses the stability analysis based on frequency response obtained through Bode plots and pole-zero plot of the individual SOGI PLL, LMS PLL and the novel H-LMS-SOGI PLL for finding out the optimized values of the control parameters like damping factor 'k' in SOGI and 'mu (μ)' which is the learning rate of LMS algorithms. A comparative steady state stability of the three PLLs structures (CLMS, CSOGI and H-LMS-SOGI) is also done based on the frequency response of Bode plots.

6.3.1 Stability Analysis of individual SOGI and LMS PLLs

The value of the control parameters like mu and k are selected from the Bode plots and step responses of drawn with the help of closed loop transfer functions given in equations (6.21) of single LMS PLL, (6.26) and (6.27) of single SOGI PLL. Fig. 6.5: (a) and (b) show the frequency response and the step response of the closed loop single LMS respectively for different values of 'μ' like mu= 0.5, mu=0.05, mu=0.005 and mu=0.0005. It is observed from the bode plot as shown in Fig. 6.5: (a) that with the increase in value of 'μ' the bandwidth increases and the harmonic attenuation decreases. Step response as shown in Fig. 6.5: (b), it is observed that the by considering settling time and oscillation the response gives best result for mu=0.005. However,



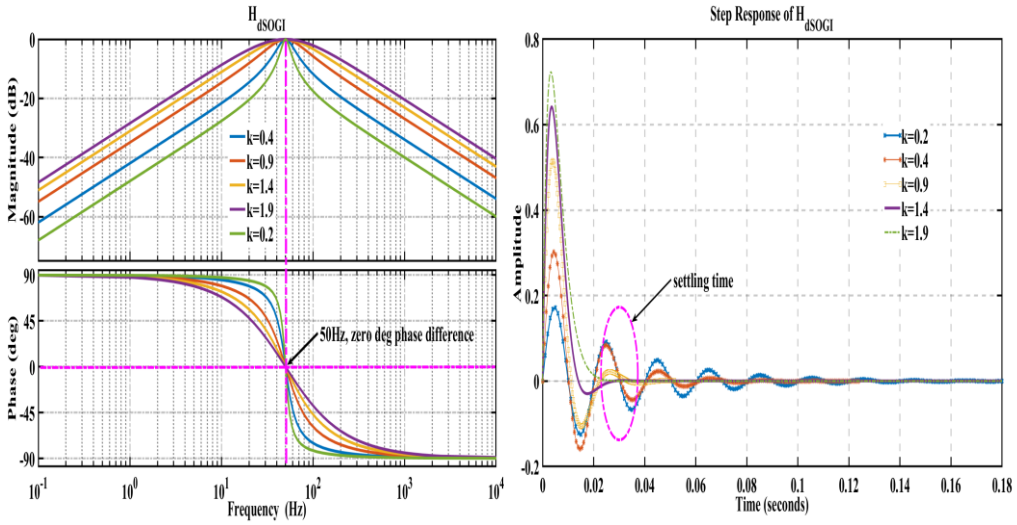
(a) (b)

Fig. 6.5: (a) Bode plot of LMS at different values of μ and (b) step response of LMS at different values of μ

larger value of 'μ' (mu=0.0005) leads to larger settling time, unstable dynamic performance and smaller value of 'μ' shows very large overshoot, Hence, from the response analysis the value of $\mu = 0.005$ is chosen for single LMS structure which gives better harmonic attenuation due to steeper bandwidth and faster settling time (<0.1s) with lesser damping oscillation when compared to other values.

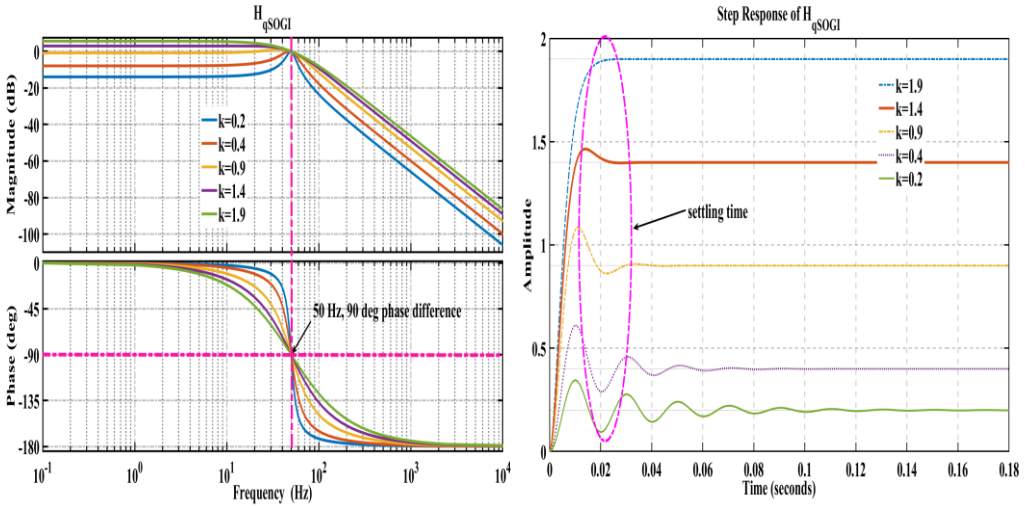
The two orthogonal signals of SOGI which are '$v_\propto$' and 'v_β are denoted as (dSOGI=$H_{\alpha SOGI}$) and (qSOGI=$H_{\beta SOGI}$) respectively in the bode and step response plots of SOGI. The frequency and step responses of dSOGI for various values of 'k' like k=0.2, k=0.4, k=0.9, k=1.4 and k=1.9 are shown in Fig. 6.6: (a) and (b), and that of qSOGI are shown in Fig. 6.7: (a) and (b) respectively. Fig. 6.6: (a) and (b) depicts the frequency response and the step response of the closed loop transfer function of active component of SOGI (H_{dSOGI}) for different values of 'k'. Fig. 6.7: (a) and 6.7: (b) are the frequency response and the step response of the closed loop transfer function of reactive component of SOGI (H_{qSOGI}) for different values of k. The bode plot and the step response of dSOGI and qSOGI as shown in the Fig. 6.6: (a) and (b), Fig. 6.7: (a) and (b) interpret that with decrease in the values of 'k' leads to better attenuation but with decayed dynamic response. Hence k=1.4 is chosen for the system analysis which yields better response after comparing the frequency response from the

bode plot and settling time (<0.035s) from the step responses of both dSOGI and qSOGI.



(a) (b)

Fig. 6.6: (a) Bode plot of dSOGI at different values of k and (b) step response of dSOGI at different values of k



(a) (b)

Fig. 6.7: Bode plot of qSOGI at different values of k and (b) step response of qSOGI at different values of k.

6.3.2 Stability Analysis of H-LMS-SOGI PLL

The hybrid LMS SOGI PLL needs proper tuning of the control parameters like learning rate 'μ' of LMS and gain 'k' of SOGI as these control parameters influence

the operation of H-LMS-SOGI PLL as a synchronization technique. Determination of optimum values of these two control parameters of H-LMS-SOGI PLL is done through the Bode plots and pole-zero map. Using the open loop transfer function given in equation (6.38), and closed loop transfer function in equation (6.39) of the hybrid PLL relevant bode plots and pole-zero maps are drawn by fixing one parameter and varying the other parameter at one time and again by varying both 'k' and 'μ'. The fixed values of k=1.4 and mu=0.005 from single SOGI and LMS PLLs as observed in previous sub sections are chosen as optimised values to observe their effect and validity in analysing the stability of H-LMS-SOGI PLL. Therefore, three cases are considered viz. case I: Fixed 'k' and varying 'μ', case II: Fixed 'μ'and varying 'k' and case III: Varying both k and 'μ'for finding the optimised value of 'k' and 'μ'.

Case I: Fixed 'k' and varying 'μ'

Fig. 6.8 shows the Bode diagram of H-LMS-SOGI PLL with fixed damping ratio, k=1.4 of SOGI and varying the learning rate (mu) 'μ' like μ=1.2, 0.1, 0.5, 0.05, 0.005, 0.0005 of LMS. The bode plot shows that for decreased values of 'μ', at the response becomes more narrow interpreting that the bandwidth decreases and hence the harmonic attenuation increases in the process. This gives a slower dynamic response. Therefore, the response of H-LMS-SOGI with μ = 0.005, 0.0005 shows better performance than other values. Further, choice of the optimised value out of these two (μ = 0.005,0.0005) is done by analysing the pole-zero plot. Fig. 6.9: shows the pole-zero plot and the zoomed portion of the pole-zero plot of transfer function as given in equation (6.39) in z-plane. The z-plane pole-zero plot predicts that the H-LMS-SOGI system is stable as all its poles and zeros lie within the unit circle. The poles closer to unit circle show slower settling. The pole-zero plots in Fig. 6.9 shows that the poles of the system with $\mu = 0.0005$ are nearest to the unit circle and that with $\mu = 0.005$ is farther away from it. Hence, the system with $\mu = 0.005$ gives distinct non overlapping conjugates poles. Therefore, this value of $\mu = 0.005$ is found to be the best choice for better harmonic attenuation and faster settling time while considering the responses from both bode and zero-pole plots with different values of μ.

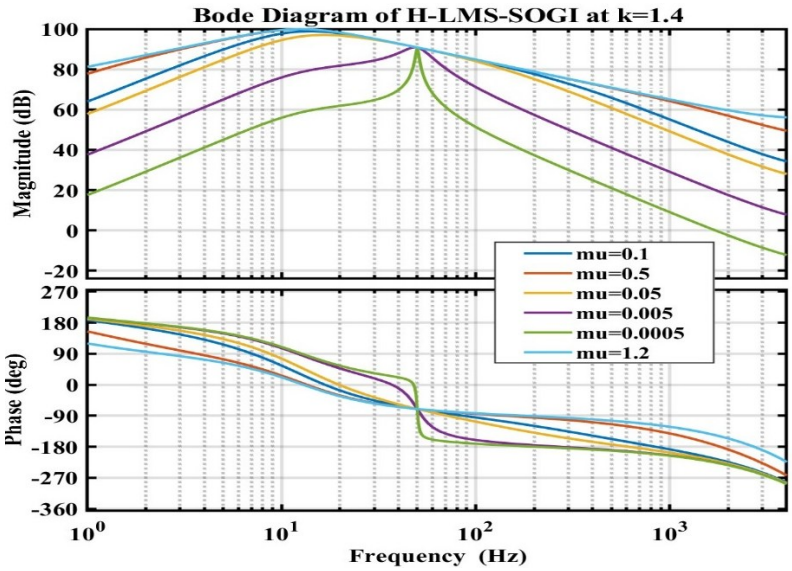


Fig. 6.8: Bode plot at constant k=1.4 and varying μ

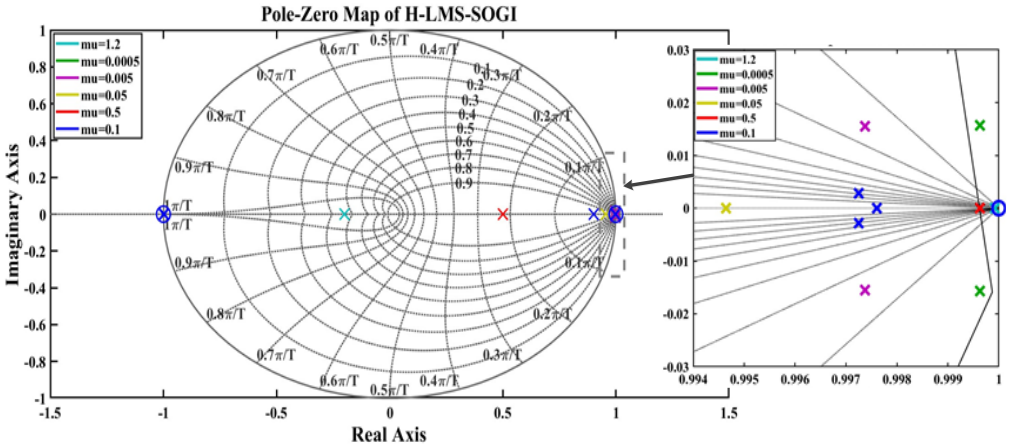


Fig. 6.9: pole-zero maps of H-LMS-SOGI and enlarged section for constant k=1.4 and varying μ

Case II: Varying 'k' and fixed 'μ'

Fig. 6.10 shows the bode diagram of H-LMS-SOGI structure with fixed 'μ=0.005' which is the optimised value of learning rate of single LMS structure as obtained from previous section and varying 'k'. Different values of 'k' parameter are selected randomly like k= 0.1, 0.8, 1.4, 2, 2.6, 3 for plotting the bode diagram. The plot shows that with decreased values of k, the slope becomes narrower indicating decrease in the bandwidth and increased harmonic attenuation. The values of k=0.1, 0.8 and 1.4 show better performance than other values considered. The pole-zero plots shown in Fig. 6.11 is plotted by using the closed loop transfer function given in

equation (6.39) in z-plane. It predicts that the H-LMS-SOGI system is stable as all its poles and zeros lie within the unit circles.

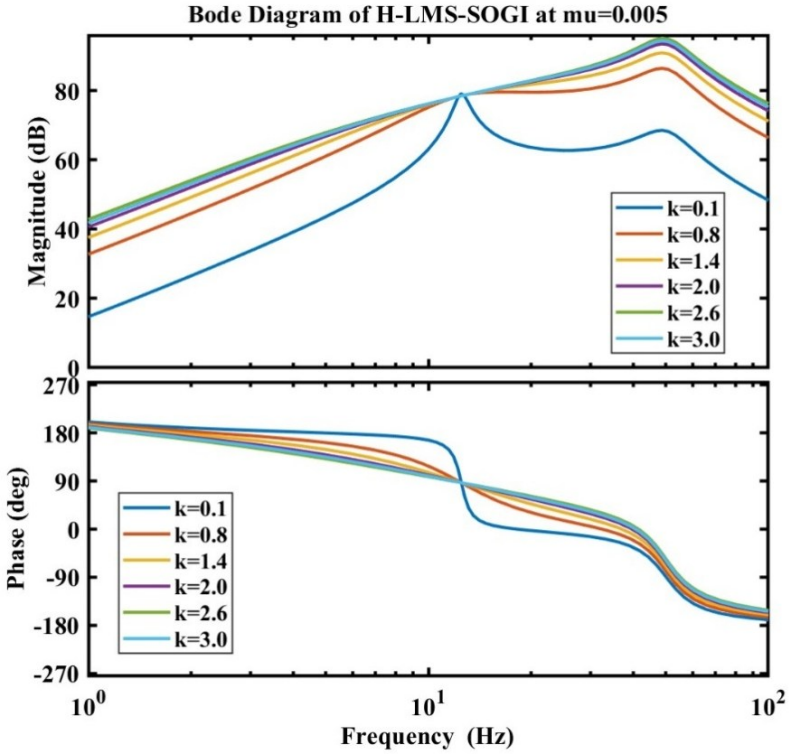


Fig. 6.10: Bode diagram of H-LMS-SOGI at constant mu=0.005 and varying k.

The extended zoomed portion of pole-zero plot of Fig. 6.11 depicts the positions of poles various k, with values of k=0.1, 0.8 and 1.4 considered, the poles of the system with k=0.8 are nearer to the unit circle. The poles with k=1.4 are farther away from it

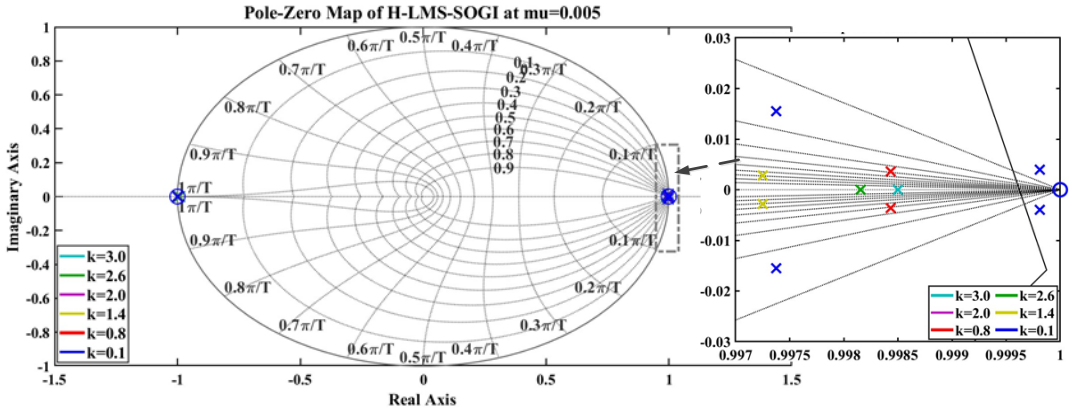


Fig. 6.11 pole-zero map of H-LMS-SOGI and its enlarged section at constant μ=0.005 and varying k

and unit circle. The poles with k=1.4 are farther away from it and show distinct conjugate poles without overlapping. Hence, the system with k= 1.4 is found to be the best choice with better harmonic attenuation and faster settling time after considering both bode plot and zero-pole map.

Case III: Varying both k and μ

In the analysis of this case, suitable value combinations of 'k' and 'μ' are selected and studied for obtaining the optimum performance of the system. Six values combinations are chosen like k=0.8 and $\mu = 0.005$; k=0.8 and $\mu = 0.0005$; k=1.4 and $\mu = 0.005$; k=1.4 and $\mu = 0.0005$; k=2.0 and $\mu = 0.005$; and lastly k=2.0 and $\mu = 0.0005$ for plotting both bode and pole-zero map. Fig. 6.12 presents the bode diagram of H-LMS-SOGI structure by varying both control parameters, 'k' and 'μ'. This diagram shows that three choices with k=0.8 and $\mu = 0.005$; k=1.4 and $\mu = 0.0005$; k=0.8 and $\mu = 0.0005$ have narrower plots than other values.

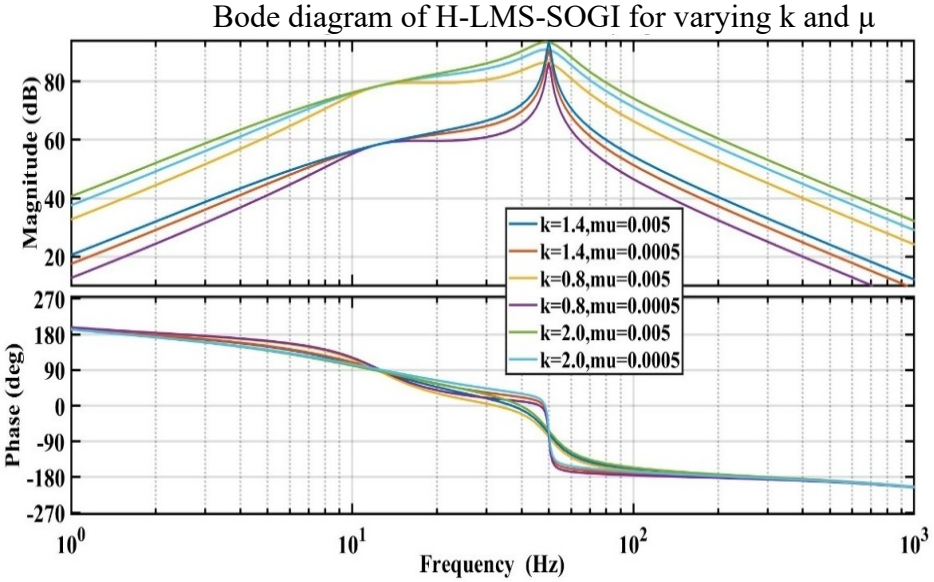


Fig. 6.12: Bode diagram of H-LMS-SOGI for varying k and μ

Fig. 6.13 show the pole-zero map of H-LMS-SOGI PLL under varying k and μ with k=0.8 and μ =0.005; k=0.8 and μ =0.0005; k=1.4 and μ=0.005; k=1.4 and μ =0.0005; k=2.0 and μ=0.005; and lastly k=2.0 and μ=0.0005. It predicts that the system is stable as all the poles and zeros lie within the unit circle and also settling nature of proposed hybrid structure for various combinations of k and μ. This map shows that

out of the three combinations, response for k=1.4 and $\mu = 0.005$ is farther away from unit circle and are non-overlapping than those with k=0.8 and $\mu = 0.005$, k=1.4 and $\mu = 0.0005$. The poles with k= 2 and $\mu = 0.005$ are the farthest away from unit circle but these poles are overlapping. Hence the best suitable combination considering steady state and faster setting time turn out to be k=1.4 and $\mu = 0.005$. Hence, the choice of parameters k=1.4 and $\mu = 0.005$ of H-LMS-SOGI as the optimised values shows the best performance when observed from steady state and settling time response from bode diagram, step response as well as pole-zero map from Fig. 6.8-6.13.

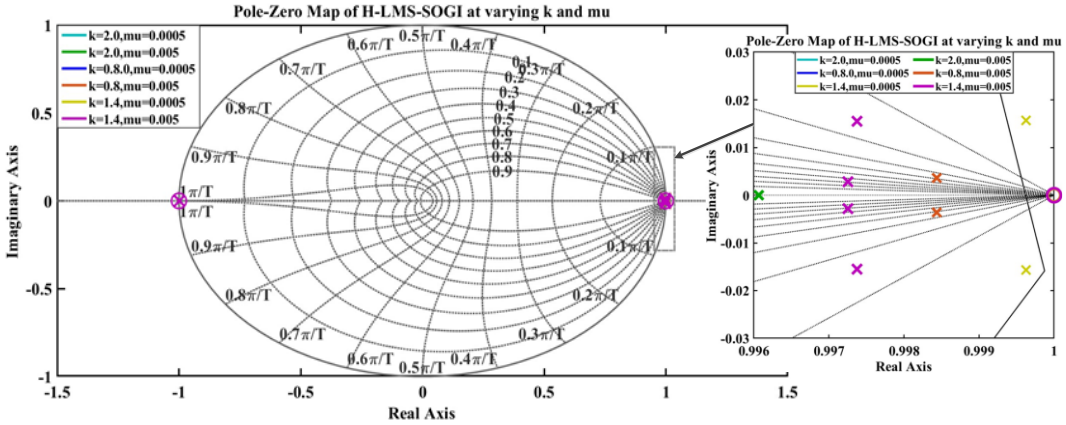


Fig. 6.13: Pole-zero map of H-LMS-SOGI and its enlarged section for varying k and μ

6.3.3 Comparative Stability Analysis of CLMS, CSOGI and H-LMS-SOGI PLLs

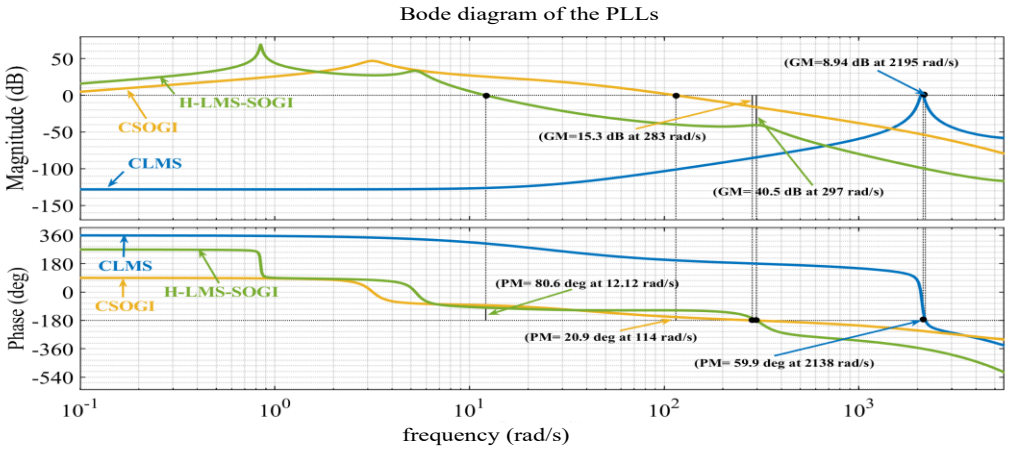


Fig. 6.14: Bode plot of CLMS, CSOGI, H-LMS-SOGI PLLs

The closed loop transfer functions of CLMS PLL, CSOGI PLL and H-LMS-SOGI PLL given in equations (6.23), (6.31) and (6.39) are used to plot the frequency response diagram shown in Fig. 6.14. It gives the comparative steady state stability analysis of the cascaded and hybrid PLLs through the values of gain margin (GM) with phase cross over frequency and phase margin (PM) with gain cross over frequency.

Table 6.1: Gain margin and phase margin with their crossover frequencies of the three PLLs

Types of PLL	GM in dB	Cross over frequency (rad/sec)	PM in (°)	Cross over frequency (rad/sec)
CLMS PLL	8.94	2195	59.9	2138
CSOGI PLL	15.3	283	20.9	114
H-LMS-SOGI PLL	**40.5**	297	**80.6**	12.12

Table 6.1 gives the values of the gain margin and phase margin with the respective crossover frequencies (rad/sec) of the three PLLs. The stability of these three PLLs are compared considering the sign and magnitude of the gain margin and phase margin values obtained from the Bode diagram. It shows that all the three PLLs give positive gain margin (GM) in dB and positive phase margin (PM) in (°), depicting that all the three PLLs are stable. The values of the gain margin and phase margin are compared to determine the most stable among the three PLLs.

Table 6.1 depicts that the proposed H-LMS-SOGI PLL has the largest positive values of gain margin (GM= 40.5dB) and phase margin (PM=80.6°) then followed by CLMS and CSOGI PLLs. Therefore, it can be concluded that the proposed H-LMS-SOGI PLL is highly stable than the other two combination PLLs.

6.4 Performance Analysis of Different PLLs

A sinusoidal grid voltage of v_s=325 V (peak value) and fundamental grid frequency of f=50Hz are given as input voltage to all the three PLLs. The proportional, integral gains of the PI controller, damping factor and learning rate of the PLLs are chosen carefully to obtain best results. The optimised gain parameters values taken

for CSOGI PLL, CLMS PLL and H-LMS-SOGI PLL are considered for simulation. The simulation results are tested under adverse grid conditions like (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30° phase jump, (e) +5Hz frequency change, and (f) 20% dc offset are discussed using MATLAB Simulink toolbox. During simulation, disturbances are given within a time period of 0.2s to 0.4s.

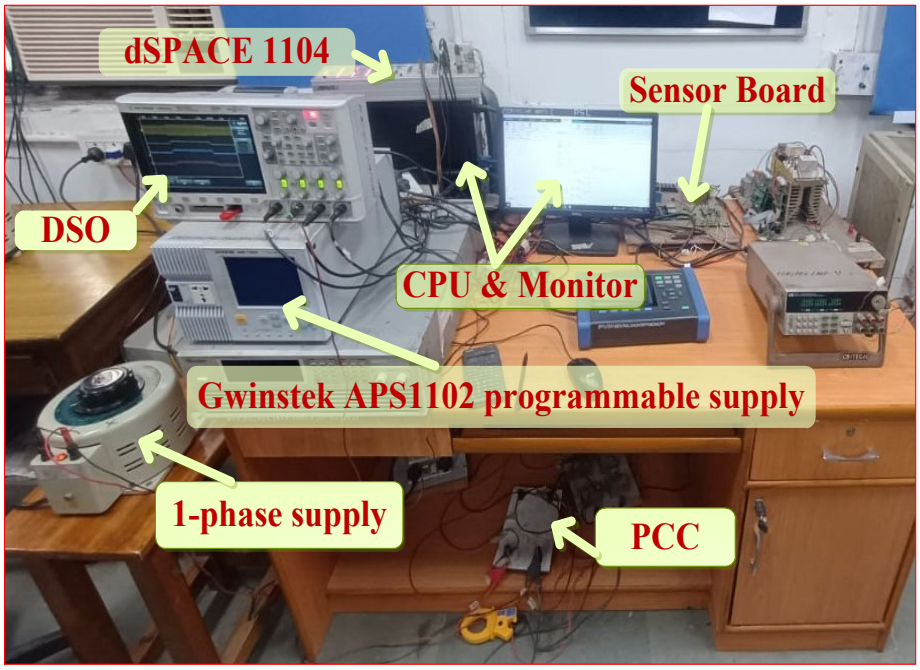


Fig. 6.15: Photograph of hardware setup for analysing the dynamic performances of different PLLs

The hardware results of the PLLs performances are obtained by setting up a laboratory prototype environment as shown in Fig. 6.15 to validate the simulation results under various cases. A single-phase programmable supply of GwinSTEK model (APS-1102A) is used for generating different types of voltage signal waveforms like simple sinusoidal waveform, 10% of the 3rd and 5th harmonics are considered.3rd and 5th harmonic induced waveform under polluted environment and other dynamics in the voltage. The input grid voltage has been sensed using a Hall effect voltage sensor and is passed to the dSpace 1104 controller for processing the algorithms through the Analog to Digital Converter (ADC) channel of dSpace. The estimated signals from Digital to Analog Converter (DAC) channels through DSO are analysed under different cases of non-ideal grid conditions.

6.4.1 Simulation and Experimental Results Analysis of CLMS PLL

The simulation results of cascaded LMS (CLMS) PLL are shown in Fig. 6.16. These results are analysed to observe the performance characteristics under various grid abnormal conditions in terms of the settling time and oscillation.

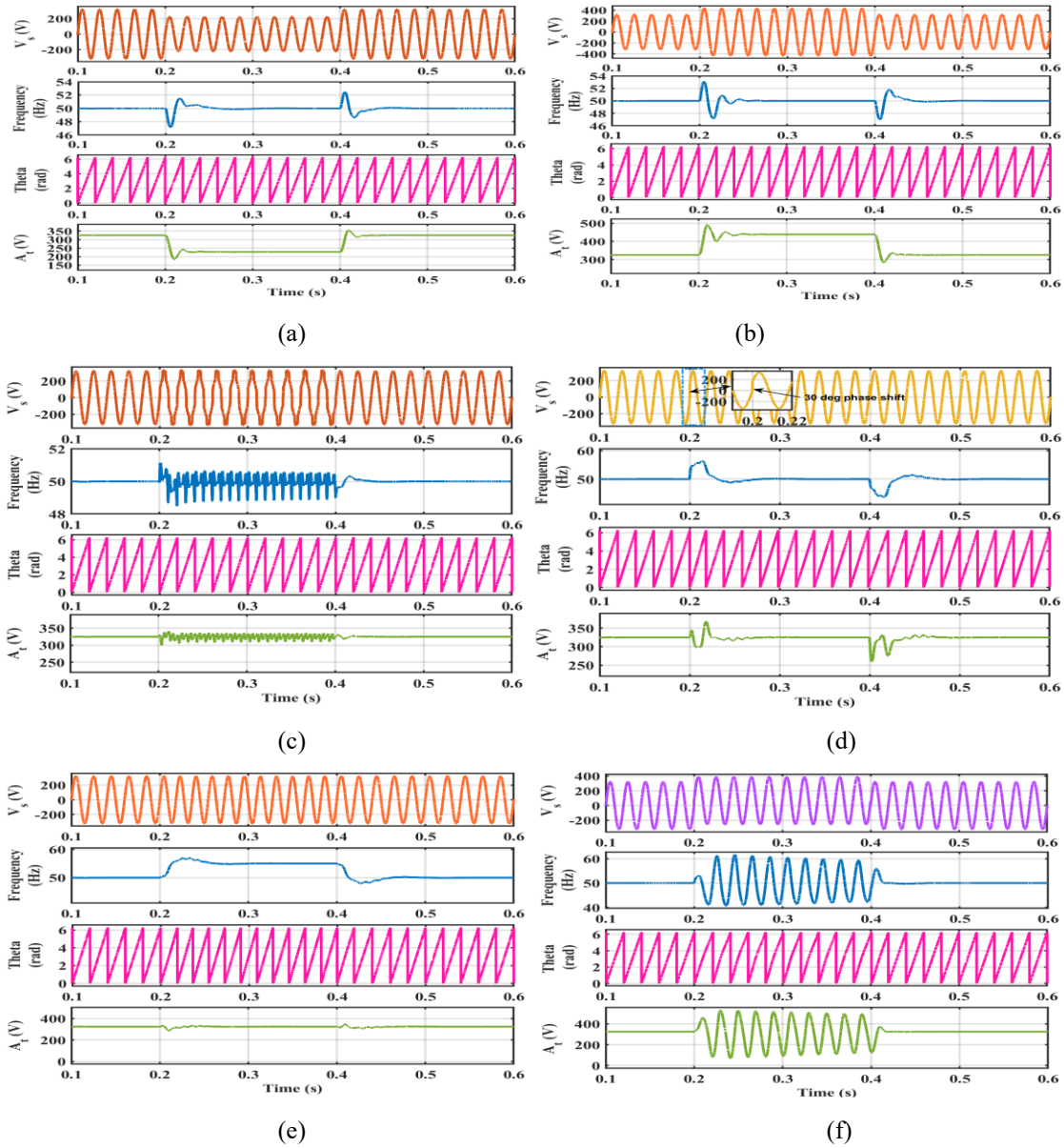


Fig. 6.16: Simulation results of dynamic performances of CLMS PLL under adverse grid conditions under (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30° phase jump, (e) +5Hz frequency change, and (f) 20 % dc offset

The plots consist of input source voltage, v_s in volts (V), frequency, in Hz, phase angle in theta, and voltage magnitude in volts (V). Fig. 6.16 (a) depicts the simulation results of 30% grid voltage sag of grid abnormalities. The plot shows

deviation in frequency response and a peak overshoot of 51.5 Hz at 0.217s. Moreover, this oscillation dies down after two cycles (0.04s). Fig. 6.16 (b) shows performance under 35% voltage swell and it shows a peak overshoot of 53.14 Hz at 0.205s but dies down within two and half cycles giving settling time as 0.043s. Fig. 6.16 (c) shows the performance plot of CLMS PLL when the grid is exposed to polluted environment i.e., when the grid voltage contains harmonics. The estimated frequency shows oscillatory response during the polluted environment. At the time of disturbance, a spike of 51.06 Hz in frequency response at 0.2s is observed which settles down at 0.22s depicting a settling time of 0.02s. Fig. 6.16: (d) gives the plot of CLMS PLL at grid abnormalities of 30^{o} phase shift. The frequency response shows a peak overshoot of 51.5 Hz at 0.216s and its settles within three cycles (0.06s). Fig. 6.16: (e) gives the performance plot at +5Hz frequency change. Its peak overshoot due to frequency change is 56.89 Hz and occurs at 0.23s and it dies down at 0.243s which gives a settling time of two and half cycles (0.043s). Fig. 6.16: (f) shows the performance of the CLMS under 20% DC-offset grid abnormalities. The frequency response shows oscillation throughout the disturbance period (0.2s-0.4s). The voltage magnitude shows an oscillatory response during the entire disturbance time period.

Fig. 6.17 gives the experimental results of CLMS PLL to validate its simulation results under adverse grid conditions. Fig. 6.17 (a) gives the experimental results of CLMS PLL under 30% voltage sag. The frequency response shows spike in oscillation which settles down within two cycles. Fig. 6.17 (b) shows the experimental results of CLMS PLL under 35% voltage swell. The frequency response shows a peak overshoot which settles down within three cycles. The voltage and magnitude responses also show the presence of 35% swell in grid voltage. Fig. 6.17: (c) shows experimental results under polluted grid voltage. The frequency response shows oscillatory response during the disturbed time period. Fig.6.17: (d) shows the experimental results under 30^{o} phase jump. The frequency response shows peak response which settles down within three cycles. Fig. 6.17: (e) shows the experimental results under +5Hz frequency change grid abnormality. The frequency response shows of +5 Hz and Fig. 6.17: (f) shows the experimental results of CLMS PLL under 20 % dc offset. The frequency and voltage magnitude responses show oscillatory response during the entire disturbance time period.

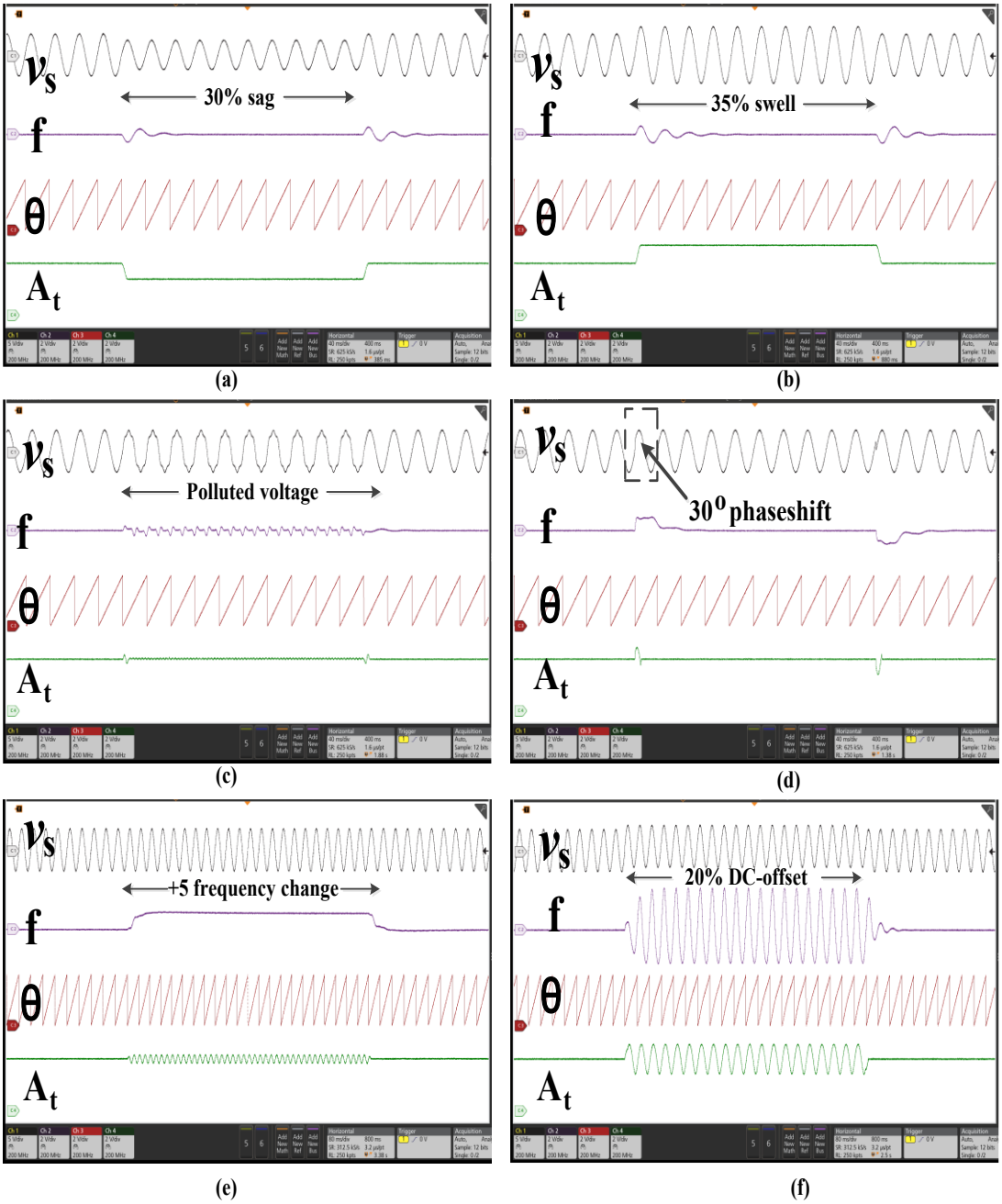


Fig. 6.17: Experimental results of dynamic performances of CLMS PLL under adverse grid conditions under (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30^o phase jump, (e) +5Hz frequency change, and (f) 20 % dc offset.

Therefore, the simulated and experimental results validate each other in all the adverse conditions.

6.4.2 Simulation and Experimental Results Analysis of CSOGI PLL

Fig. 6.18 shows the simulation results of cascaded SOGI (CSOGI) PLL under various grid abnormal conditions. The plots consist of input source voltage, v_s in volts (V), frequency, in Hz, phase angle theta in radian, and voltage magnitude in volts (V). Fig. 6.18: (a) depicts the simulation results of 30% grid voltage sag and it gives an oscillation peak of 51.67 Hz at 0.2055s in the frequency response where it dies down within four cycles (0.07s). Fig. 6.18: (b) depicts 35% grid voltage swell obtained under grid abnormalities. It shows an oscillation peak in frequency response of 51.7 Hz at 0.205s. It dies down within four cycles (0.071s). Fig. 6.18 (c) shows the performance plot when the grid is exposed to polluted environment (grid voltage containing harmonics). The voltage source in the plot shows its affect from 0.2s to 0.4s. The frequency plot also responded accordingly to the polluted environment. During the disturbance an oscillation of 50.69 Hz at 0.202s is observed and it settles down around four cycles (0.069s) depicting a settling time of 0.069s. Fig. 6.18: (d) gives the result plot of 30^o phase shift grid abnormalities. It shows frequency oscillation peak of 57.33 Hz at 0.214s and its settling time is 0.05s. Fig. 6.18: (e) gives the result of CSOGI PLL with +5Hz frequency change. Its peak overshoot is 57.63 Hz and occurs at 0.224s. It dies down within three cycles giving a settling time of about 0.046s. Fig. 6.18: (f) shows the simulated results of the CSOGI at 20% DC-offset grid abnormalities. The frequency response gives peak overshoot of 51.99 Hz at 0.205s. The peak of oscillation is 57.63 Hz and occurs at 0.224s. However, it dies down within three cycles giving a settling time of about 0.046s.

Fig. 6.19 gives the experimental results of CSOGI PLL under grid abnormalities to validate the simulation results. Fig. 6.19: (a) shows the experimental results under 30% voltage sag. The frequency response shows peak overshoot which settles down four cycles. Fig. 6.19: (b) shows the experimental results under 35% voltage swell. Its frequency response shows peak overshoot that dies down four cycles. Fig. 6.19: (c) experimental results under polluted grid voltage abnormality. Its frequency peak overshoot response dies down within four cycles. Fig. 6.19 (d) shows the experimental results under 30^o phase jump grid abnormality. The peak overshoot result of frequency response settles down within three cycles. Fig. 6.19: (e) shows the

experimental results of CSOGI PLL under +5Hz frequency change. The frequency response shows peak overshoot which settles down within three cycles.

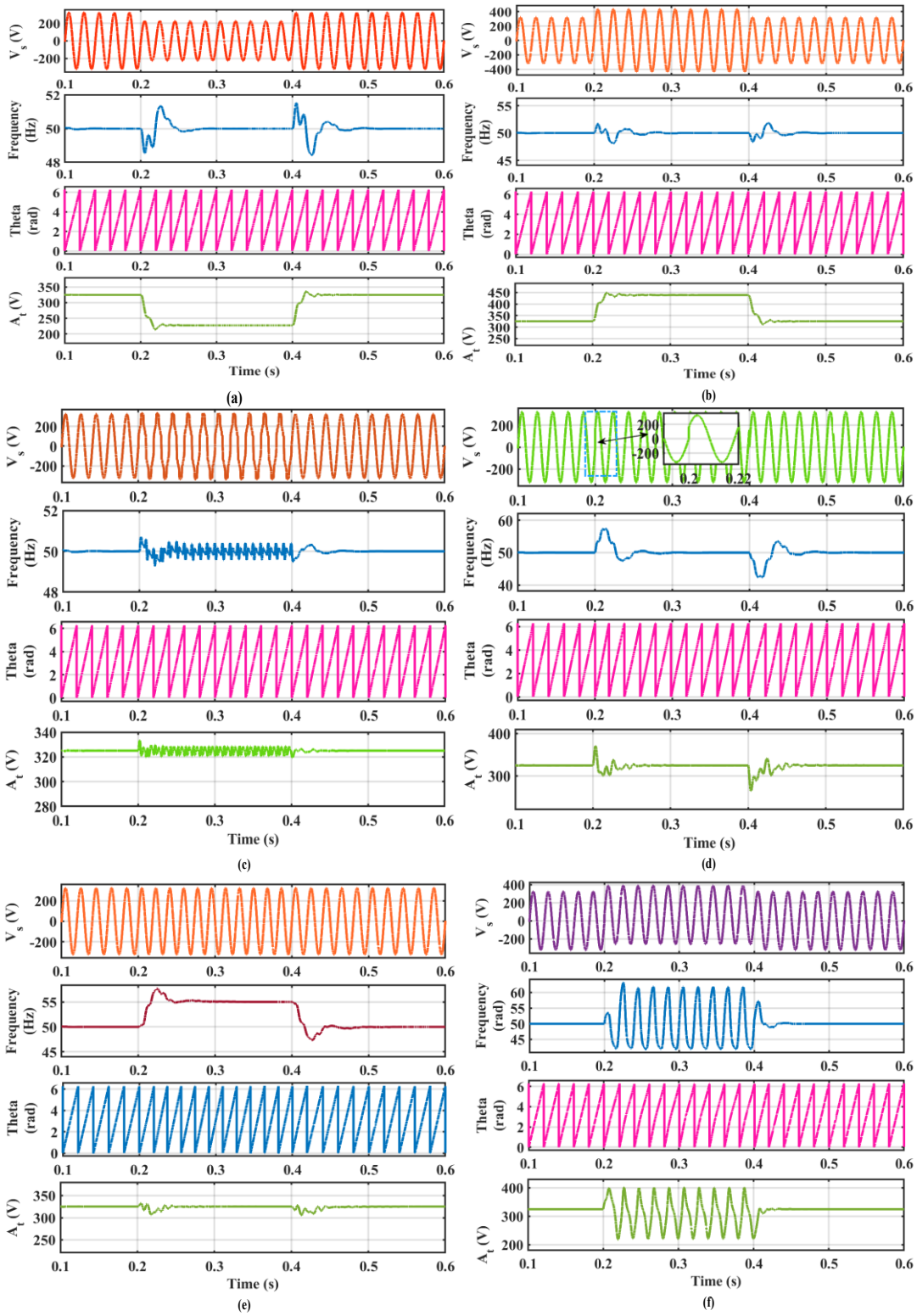


Fig. 6.18: Simulation results of dynamic performances of CSOGI PLL under adverse grid conditions under (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30° phase jump, (e) +5Hz frequency change, and (f) 20 % dc offset.

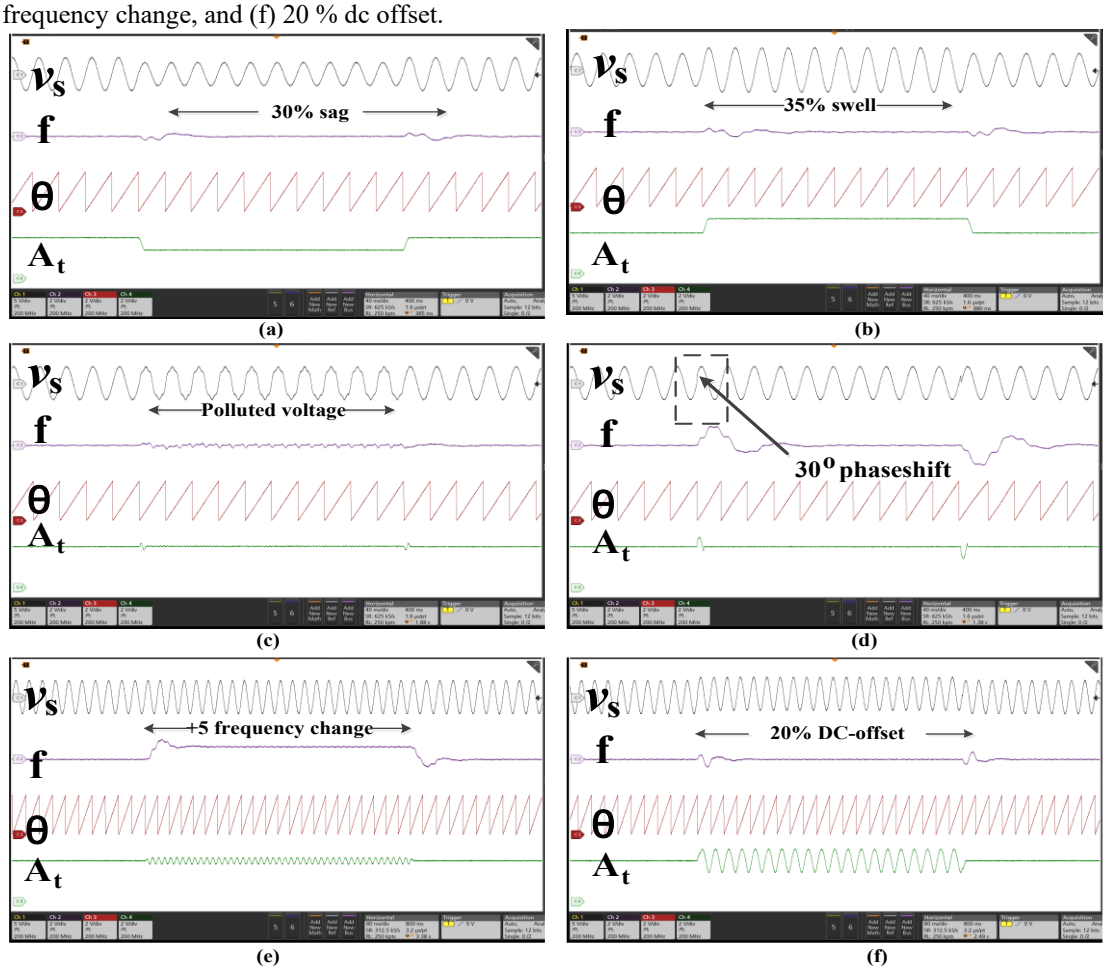


Fig. 6.19: Experimental results of dynamic performances of CSOGI PLL under adverse grid conditions at (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30° phase jump, (e) +5Hz frequency change, and (f) 20 % dc offset.

Fig. 6.19: (f) shows experimental results under 20 % DC offset grid content. The frequency response shows peak overshoot and it dies down within three cycles.

6.4.3 Simulation and Experimental Results Analysis of H-LMS-SOGI PLL

Fig. 6.20 and Fig. 6.21 show the simulation and the hardware results for the dynamic performance analysis of the cascaded hybrid least mean square and second order generalised integrator PLL (H-LMS-SOGI PLL) under various adverse grid conditions like (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30° phase jump, (e) +5Hz frequency change and (f) 20 % DC-offset. Fig. 6.20: (a) and (b) depict the simulated dynamic performances of under 30% sag and 35% swell

of grid voltages. It is observed that there is no variation in estimated phase angle. The overshoot of the frequency response under 30% voltage sag is of 51.28Hz and peak overshoot of frequency response under 35% voltage swell is 53.6 Hz. The estimated frequencies settle down within two cycles under both the sag and swell voltage deviations. Fig. 6.20: (c) predicts the simulated performances under polluted grid voltage. Oscillations in the estimated frequency are observed during the disturbed period. It is observed that the overshoot with ripples the settle down faster within one cycle. Fig. 6.20: (d) predict the simulated results under 30^{o} phase jump. The disturbances observed in the estimated frequency has an overshoot of 52.38 Hz and grid voltage amplitude settle down within three cycles. Fig. 6.20: (e) predict the simulated results under +5Hz frequency jump respectively. There are changes in the estimated frequency response. The frequency response shows an overshoot of 57.2Hz. and voltage amplitude settles down in three cycles. Fig. 6.20: (f) predicts the simulated performances under 20% DC-offset. Frequency response shows oscillatory response during disturbed time period.

Fig. 6.21 shows the experimental dynamic performance of H-LMS-SOGI PLL under grid abnormalities. Fig. 6.21: (a) shows the experimental results under 30% voltage sag. The frequency response the voltage amplitude response shows the voltage drop of 30%. Fig. 6.21: (b) shows the experimental result under 35% voltage swell. The voltage amplitude response shows 35% voltage rise. Fig. 6.21: (c) shows the experimental result under polluted grid voltage. The ripples in the frequency and amplitude responses during the disturbance period are seen. Fig. 6.21: (d) shows the experimental result of cascaded hybrid PLL under 30^{o} phase jump. The frequency response shows peak overshoot which dies down within three cycles. Fig. 6.21: (e) shows the experimental results under +5Hz frequency change. The peak overshoot observed in frequency response settles down within three cycles and also shows the +5 Hz change in frequency. Fig. 6.21: (f) shows the experimental result under 20 % DC-offset. The frequency and voltage amplitude shows oscillatory response during disturbance.

Therefore, during adverse grid conditions it can be concluded that the performance of novel H-LMS-SOGI PLL is satisfactory. Both the simulated and

experimental dynamic performance analysis considering the overshoot and settling time response which is shown in Fig. 6.20 and Fig. 6.21 validates each other.

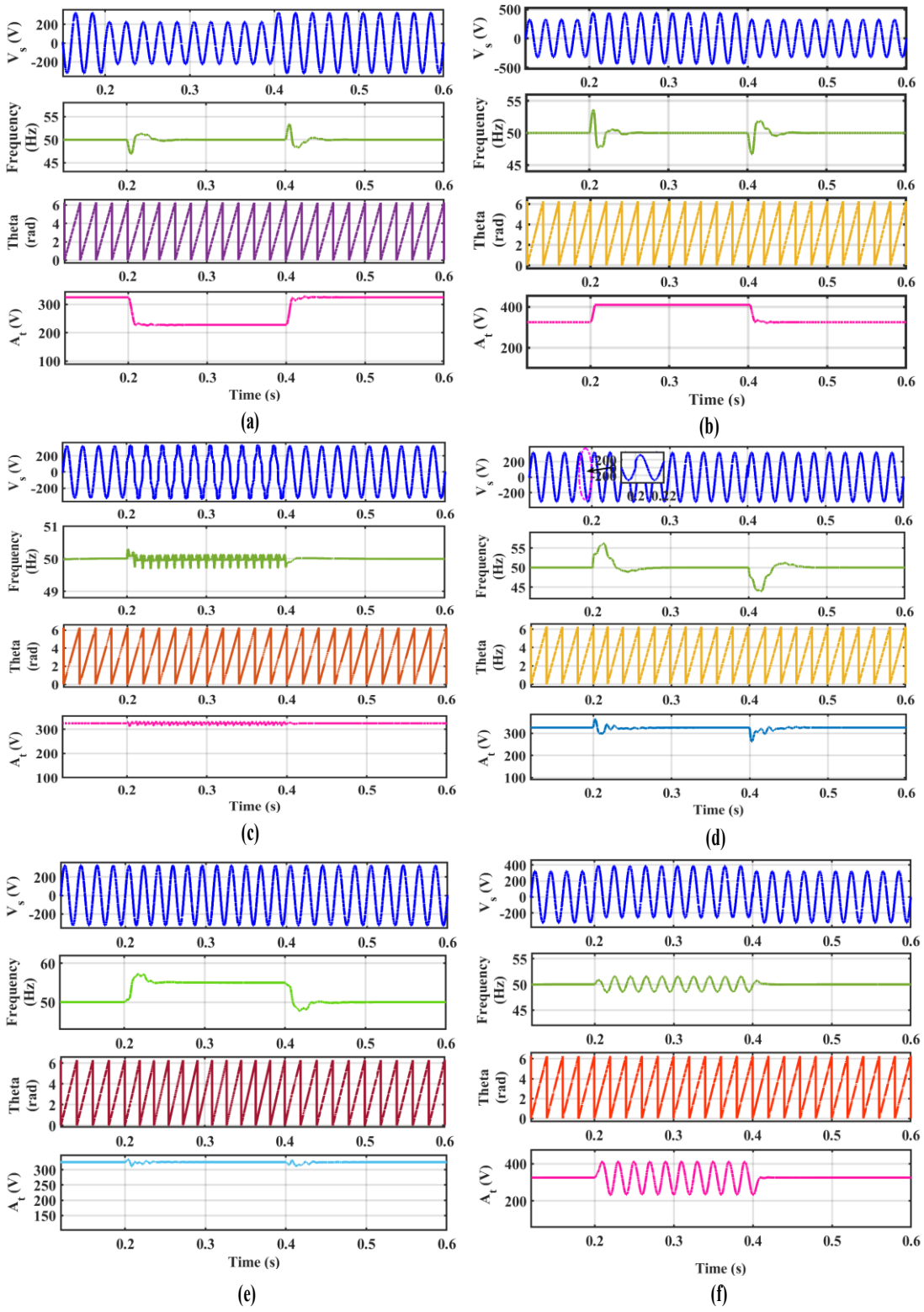


Fig. 6.20: Simulation results of dynamic performances of H-LMS-SOGI PLL for adverse grid conditions under (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30° phase jump, (e) +5Hz frequency change, and (f) 20 % dc offset.

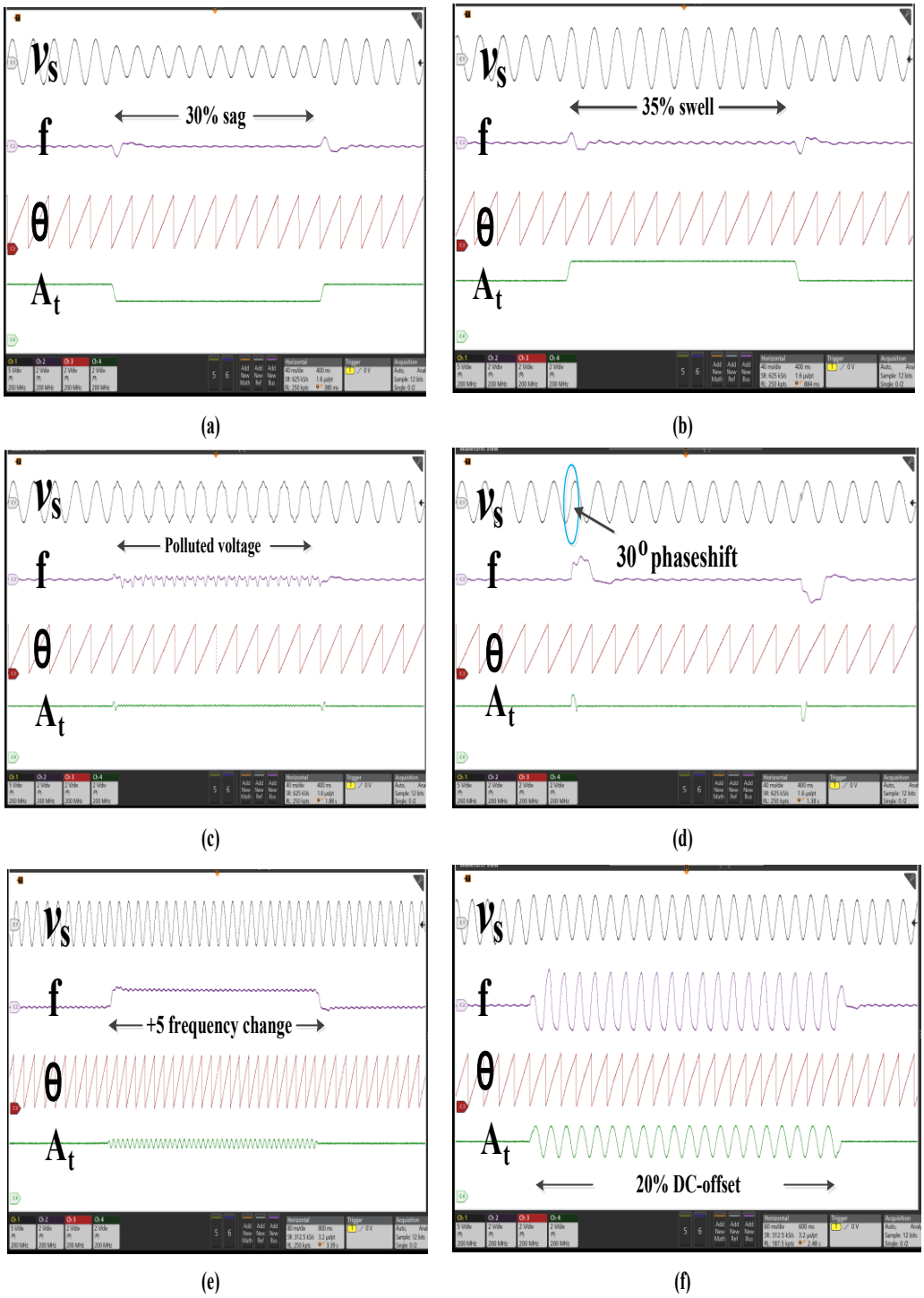


Fig. 6.21: Experimental results of dynamic performances of H-LMS-SOGI PLL for adverse grid conditions under (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30° phase jump, (e) +5Hz frequency change, and (f) 20 % dc offset.

6.4.4 Comparative Performance Analysis of Different PLLs

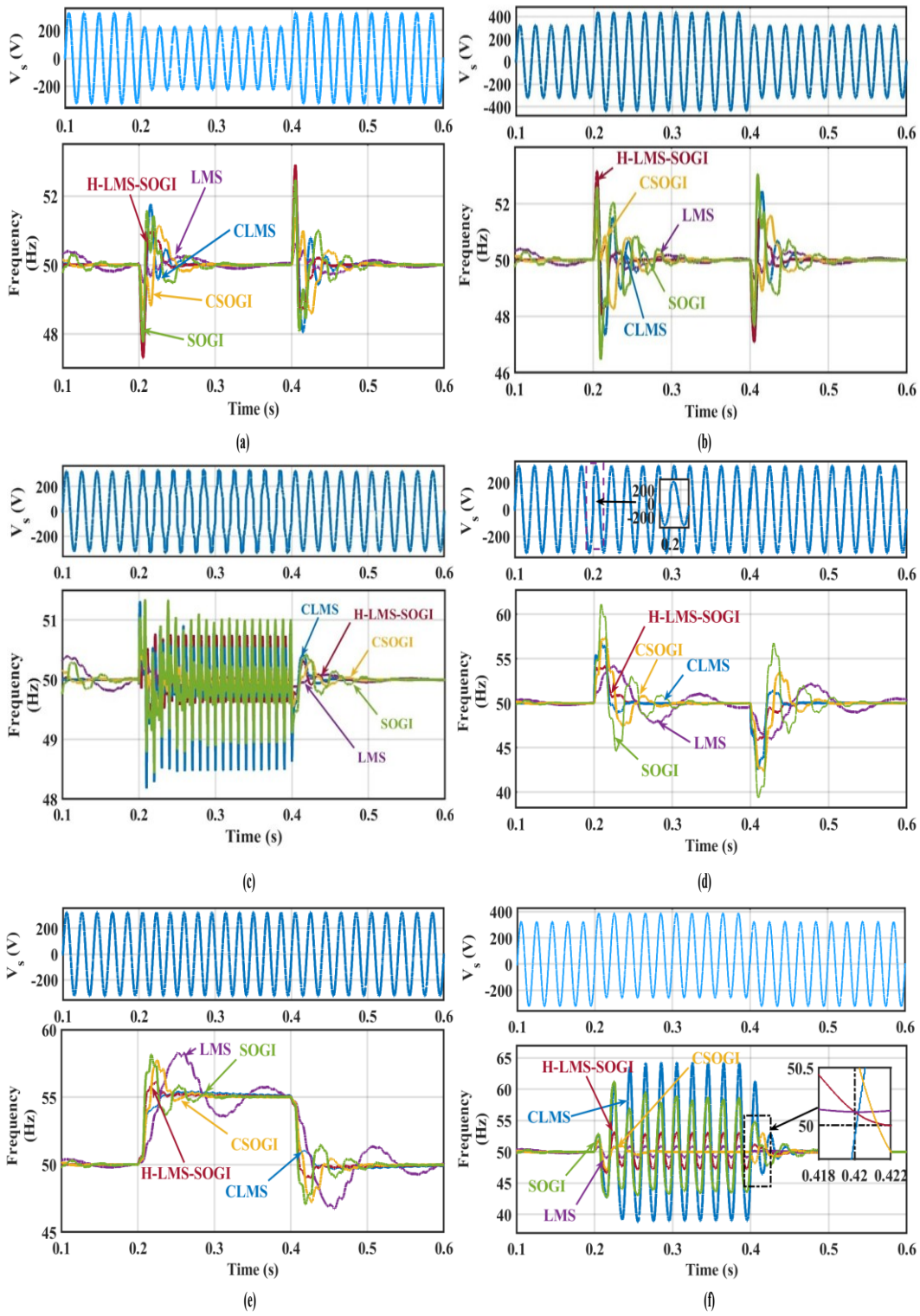


Fig. 6.22: Simulated comparative dynamic performance analyses of H-LMS-SOGI, CLMS, CSOGI, LMS, SOGI PLLs under adverse grid voltage under (d) 30^o phase jump (e) under +5 frequency jump(f) 20% dc offset.

The dynamic response of different PLLs like single SOGI, single LMS, cascaded SOGI (CSOGI), cascaded LMS (CLMS) and hybrid LMS-SOGI (H-LMS-SOGI) PLL are considered for the comparative frequency response when the grid voltage is exposed under the adverse conditions. The adverse conditions considered are (a) 30% voltage sag, (b) 35% voltage swell, (c) polluted grid voltage (d) 30^o phase jump, (e) +5Hz frequency change, and (f) 20 % dc offset. Both the simulated frequency response and experimental response of the PLLs are considered for the performance analysis. Fig. 6.22 shows the comparative analysis of single LMS, and SOGI, H-LMS-SOGI, CLMS CSOGI PLLs under non ideal grid conditions. Fig. 6.22 (a) shows the comparative frequency response under 30% voltage sag. It is observed that H-LMS-SOGI PLL shows lower overshoot with fastest settling response then the remaining four other PLLs considered. has least overshoot but with oscillatory response. Fig. 6.22 (b) shows the comparative frequency response analysis under 35% voltage swell. It shows that H-LMS-SOGI PLL shows the highest frequency overshot response but least settling time than the other four PLLs. In Fig. 6.22 (c) under polluted grid voltage H-LMS-SOGI PLL shows moderate settling response than CSOGI, single SOGI and single LMS based PLL. The overshoot of proposed hybrid PLL is also quite less. In Fig. 6.22 (d) under 30^o phase shift H-LMS-SOGI PLL shows very low overshoot than CLMS, CSOGI and single SOGI and single LMS. The highest overshoot is observed under SOGI PLL. The LMS PLL shows the worst settling time under 30 ^{o} phase shift. In Fig. 6.22 (e) under +5 frequency change H-LMS-SOGI PLL shows lowest overshoot than CSOGI, single SOGI and single LMS. H-LMS-SOGI also shows fastest settling response than without any oscillations. LMS PLL shows oscillatory response, while CLMS PLL shows more sluggish response. In Fig. 6.22 (f) under 20% dc offset H-LMS-SOGI PLL shows lower overshoot than CLMS and single SOGI. However, CSOGI PLL shows almost no oscillation under dc offset effect after 0.04s.

The comparative experimental result of the SOGI, CSOGI, LMS, CLMS and H-LMS-SOGI PLLs under various grid abnormalities are shown in Fig. 6.23. Fig.

6.23: (a) shows the comparative experimental results under 30% grid voltage sag grid abnormality. The frequency response of all the PLLs is considered for analysing their performance. The input voltage response 'v_s' depicts 30% grid voltage drop. The frequency responses of all the PLLs shows peak overshoots and among them single SOGI PLL and single LMS PLL show larger peak overshoot and large settling time. CLMS PLL shows least overshoot but show larger settling time. H-LMS-SOGI PLL gives the best performance due to least overshoot and fastest response with least settling time. Fig. 6.23: (b) shows the comparative experimental result under 35% grid voltage swell. The supply voltage response 'v_s' depicts 35% grid voltage swell. The frequency response of single SOGI PLL and single LMS PLL show the largest overshoot among all the PLLs and larger settling time. The CSOGI gives better response than CLMS in case of setting time but the overshoot of CSOGI is larger than CLMS. The best performance is shown by H-LMS-SOGI as it depicts fastest settling time and least overshoot. Fig. 6.23: (c) shows the comparative experimental results under polluted grid voltage. The single SOGI and LMS give larger overshoot and more settling time than CSOGI, CLMS and H-LMS-SOGI. Overshoot is not seen CLMS and H-LMS-SOGI however, CLMS shows sluggish response than H-LMS-SOGI. Fig. 6.23: (d) shows comparative experimental result under 30^o phase shift. The frequency response of CSOGI depicts better performance than CLMS, single SOGI, single LMS in case of settling time (lesser settling time). The overshoot of CLMS is smaller than SOGI, LMS and CSOGI. The best dynamic performance is shown by H-LMS-SOGI in terms of overshoot and settling time. Fig. 6.23: (e) shows the comparative experimental results under +5Hz frequency change. Least overshoot is seen in CLMS but it has larger settling time than CSOGI but lesser than SOGI and LMS. The performance of H-LMS-SOGI is best as it gives moderate response in both overshoot and settling time. Fig. 6.23: (f) shows the comparative experimental results under 20 % dc offset. The effect of DC offset is not seen in CSOGI. However, SOGI, LMS, CLMS and H-LMS-SOGI PLLs show ripples in the response during the entire disturbance period. CLMS depicts least overshoot but is sluggish in nature. SOGI and LMS show larger overshoot and larger settling time. Hence H-LMS-SOGI shows smaller overshoot but fastest settling time.

Moreover, Table 6.2 has been prepared for observing the overshoot and settling time of each PLL under each grid abnormal condition and from Table 6.2 it is observed that the H-LMS-SOGI PLL gives best dynamic performance under 30% voltage sag, 30° phase shift and +5 Hz frequency change as compared to others PLL techniques. Moreover, its performance is also satisfactory under polluted grid condition as well as 20% dc offset condition. Hence this PLL is a good synchronization technique which is a hybrid combination of LMS and SOGI PLL.

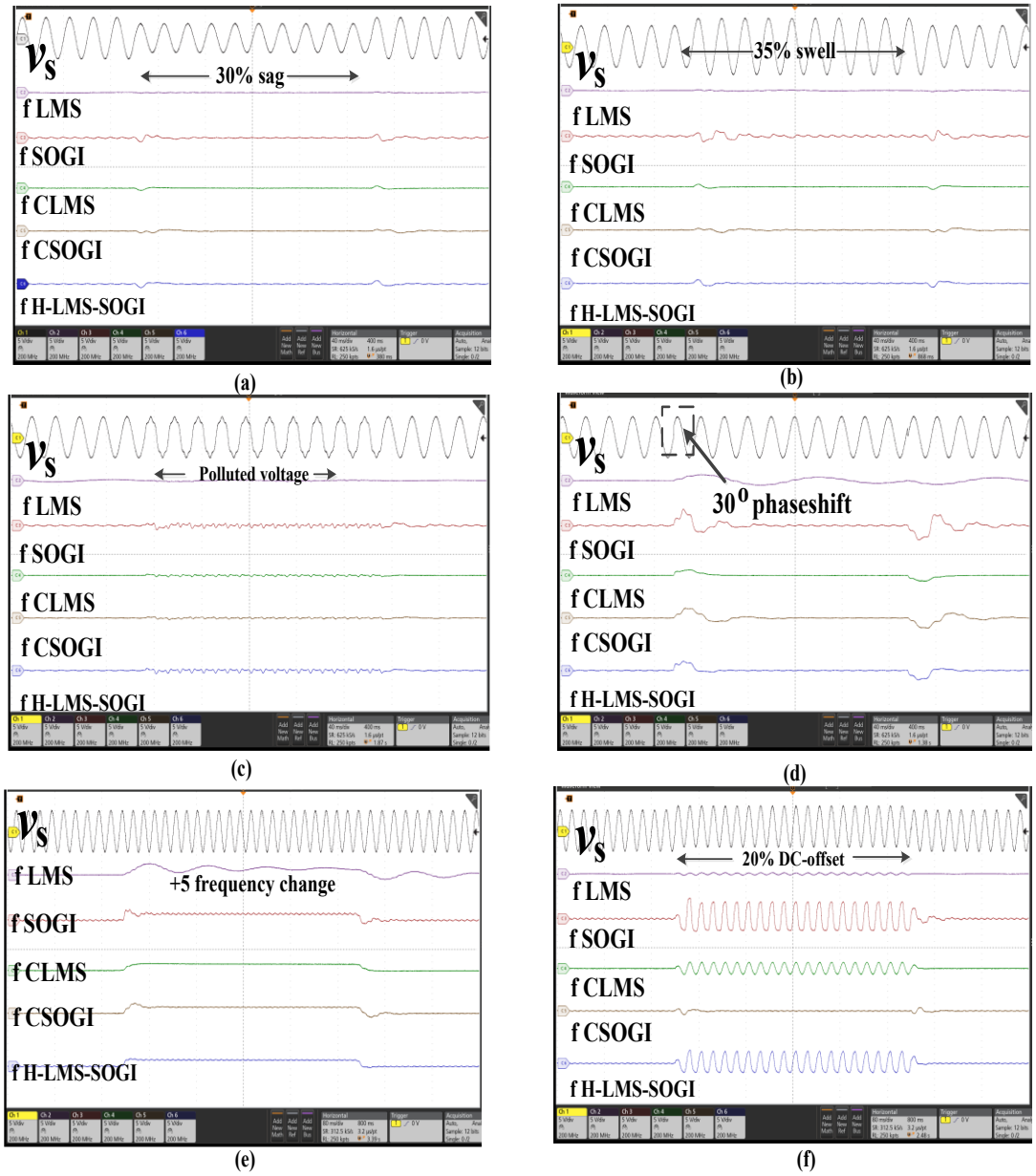


Fig.6.23: Experimental comparative dynamic performance analyses of H-LMS-SOGI, CLMS, CSOGI, LMS, SOGI PLLs under adverse grid voltage under (a) 30% grid voltage sag (b) 35% grid voltage swell (c) polluted grid voltage(d) 30° phase jump (e) under +5 frequency jump(f) 20% dc offset

Table6.2: Comparative performance analysis of LMS, CLMS, SOGI, CSOGI and H-LMS-SOGI PLLs

Grid condition tested	Parameter considered	LMS	SOGI	CLMS	CSOGI	H-LMS-SOGI
30% voltage sag	**Overshoot**	Lowest (50.24 Hz) but oscillatory	Moderate (51.56 Hz)	Highest (51.74Hz)	High (51.73 Hz)	Lower (50.9 Hz) and no oscillation
	Settling time	Sluggish (~ 3 cycles)	Slower response (nearly 3 cycles)	Moderate response (more than 2 cycles)	Moderate response (more than 2 cycles)	Fastest response (less than 2 cycles
35% voltage swell	**Overshoot**	50.7Hz at 0.205s	52.4 at 0.204	52.6 Hz at 0.2036s	51.48Hz at 0.205s	Highest 53.1Hz at 0.204s
	Settling time	Sluggish (0.307s	Sluggish (nearly 6 cycle) 0.32s	Moderate (nearly 3 cycles)	Moderate (more than 3 cycle) 0.29s	Fastest (~ 1 cycle)
Polluted grid voltage	**Overshoot**	Least (50.28 Hz)	Highest (51.33 Hz)	High (50.77 Hz	moderate (50.63 Hz)	Lower (50.3 Hz)
	Settling time	Slower response (within two cycles))	Moderate response (within two cycles)	Least response (within two cycles	Sluggish response (within two cycles)	Moderate response (within two cycles)
30° phase shift	**Overshoot**	Lesser (54.17 Hz)	Highest (61.12 Hz)	moderate (56.8Hz)	largest (57.32Hz)	least (52.38 Hz)
	Settling time	sluggish (~ 5 cycles)	slow response (~ 3 cycles)	Moderate response (~ 2 cycles)	Moderate response (~ 2cycles)	Fastest response (~ 1 cycle)
+5 Hz frequency shift	**Overshoot**	high (58.29 Hz)	Moderate (58.11 Hz)	54.2Hz (undershoot)	high(58.7Hz)	least (56.12Hz)
	Settling time	Sluggish response and oscillatory	~ 2 cycles	~ 2 cycles	~ 3 cycles	~ 2 cycles and fastest response
20% dc offset	**Overshoot**	largest (61.04 Hz)	Least (50.82 Hz)	High (55.16Hz)	Low (53.1 Hz)	Moderate (51.25 Hz)
	Settling time	~ 6 cycles	~ 3 cycles	~ 6 cycles	~ 4 cycles	~ 2 cycles

6.5 Application of proposed H-LMS-SOGI PLL for Inverter Control

Under this Section, an application of the proposed hybrid PLL for inverter control has been investigated. The proposed H-LMS-SOGI based controller for inverter control for a single-phase grid connected system. Fig. 6.24 shows the block diagram where the proposed H-LMS-SOGI has been used as controller for compensating the non-linear load current drawn by the no linear load. The system block diagram shows a single-phase grid connected system feeding non-linear load modelled as a R-L branch connected at the ends of a diode rectifier.

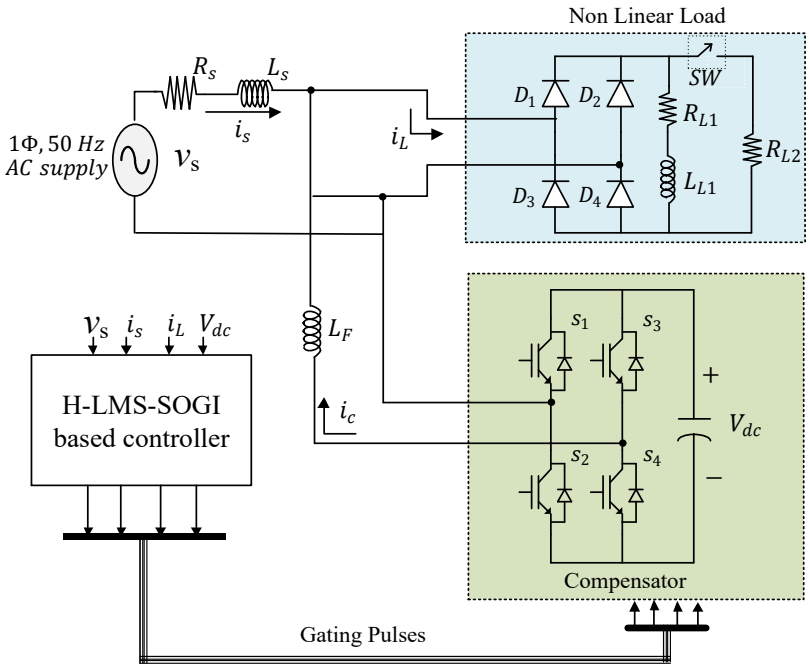


Fig. 6.24: **B**lock diagram of inverter connection with H-LMS-SOGI PLL based controller

Further, the proposed H-LMS-SOGI technique is now used as a technique for fundamental current estimation and not as a PLL. The H-LMS-SOGI controller block estimates the fundamental load current component in the system and computes the reference supply current. The actual supply current and the reference supply currents are compared using the pulse width modulation technique to generate the gating pulses for the compensator. Fig. 6.25 shows the simulation results of the inverter connection with H-LMS-SOGI based controller. The load current is non-linear and increased after 0.5s. It is observed that the supply current is sinusoidal and in phase with the grid voltage. Thus, power correction is close to unity. Moreover, the dc link voltage of the

inverter (Vdc) is maintained to its reference value of 150V by PI controller action. The fundamental current component extracted using the proposed H-LMS-SOGI technique is constant and varied only when the load current changes at t=0.5s. Thereafter it again becomes steady as shown in the Fig. 6.25. Thus, Fig. 6.25 clearly shows that the proposed Hybrid PLL can also be used as H-LMS-SOGI based controller.

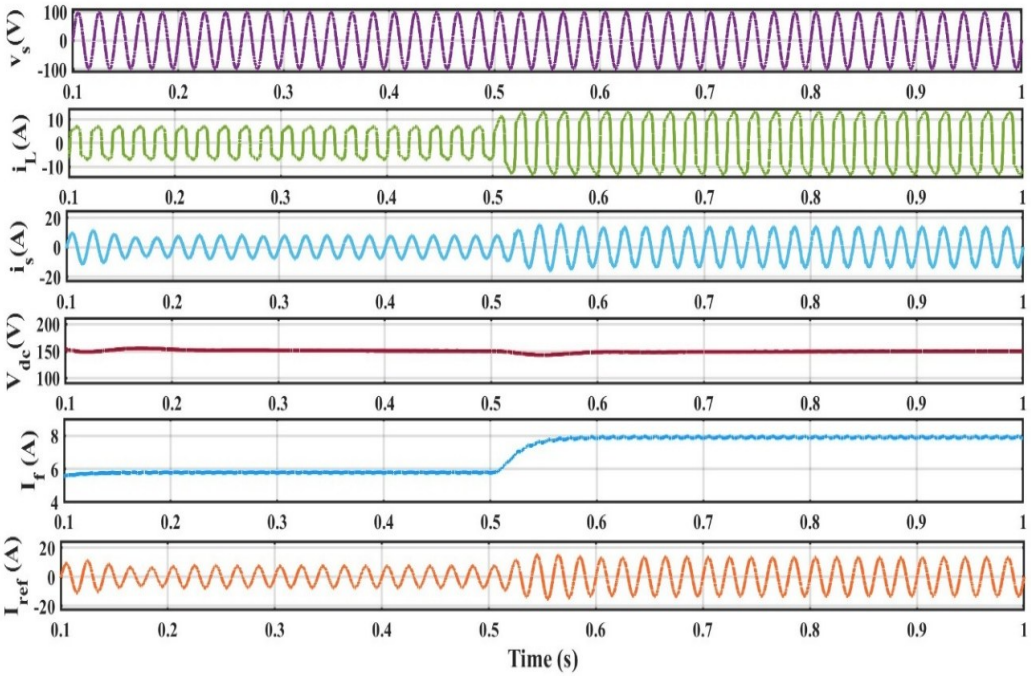


Fig. 6.25: Simulation result of proposed H-LMS-SOGI based controller showing reference current, I_{ref} (A), fundamental current, I_f (A), dc voltage V_{dc} (V), source current, i_s (A), load current, i_L(A) and source voltage, v_s (V)

6.6 Conclusion

In this chapter, the design and modelling of H-LMS-SOGI PLL is investigated and analysed in detail. The performances of the five PLLs viz. SOGI, LMS and three cascaded PLLs under adverse grid conditions is analysed through simulation using MATLAB Simulink toolbox (2020A). The designed mathematical modelling of the three PLLs is discussed and the selection of the control parameters 'μ'of LMS and 'k' of SOGI is done through Bode plot and pole-zero plots. The simulated results are validated through hardware results by setting up a laboratory prototype using a $1-\emptyset$ programmable supply of GwinSTEK model (APS-1102A). The stability of the three PLLs are analysed through of the gain margin (GM) in dB and phase margin (PM) in degree. The enhanced stability of the novel H-LMS-SOGI PLL is further validated by

the pole-zero plot in complex plane and H-LMS-SOGI PLL is more stable than the other two cascaded PLLs due to larger values of positive GM and PM. The dynamic performance under steady state analysis of H-LMS-SOGI PLL, CLMS PLL, and CSOGI PLL is performed under adverse grid conditions considering six test conditions viz. (a) Grid voltage deviation with 30% sag (b)Grid voltage deviation with 35% swell, (c) Under polluted grid voltage, (d) Grid voltage under 30^{o}phase jump, (e): Grid voltage under +5 Hz frequency jump, (f): Grid voltage under 20% dc offset. The experimental frequency response of these three PLLs are also analysed for validating the simulation results under same considered grid abnormal conditions. The comparative analysis of the five PLLs is also performed considering six test cases of non-ideal grid conditions viz. (a): Grid voltage change of 30% sag, (b): Grid voltage change of 35% swell, (c) Grid voltage under polluted environment, (d): Grid voltage under 30^{o}phase jump, (e): Grid voltage under +5 frequency jump, (f): Grid voltage under 20% dc offset. Under 30% voltage sag H-LMS-SOGI PLL gives a lower overshoot and fastest settling time though LMS PLL gives the lowest overshoot but performs sluggishly. Under 35% Grid voltage swell H-LMS-SOGI PLL gives the highest overshoot than the other four PLLs but the fastest settling time period. With 30^{o} phase shift, H-LMS-SOGI PLL gives the least overshoot with moderate settling time of five cycles. The proposed H-LMS-SOGI PLL also shows least overshoot and fastest dynamic response under polluted grid voltage and +5Hz step frequency change. Moreover, the novel H-LMS-SOGI PLL gives satisfactory response under 20%dc offset. Further, the designed H-LMS-SOGI technique is validated for inverter control in a single-phase grid connected system. Hence it can be concluded that the novel H-LMS-SOGI PLL gives satisfactory dynamic response under all the adverse grid conditions considered and the technique can also be used for load compensation satisfactorily.

Chapter 7

PERFORMANCE ANALYSIS OF DFIG INTEGRATED THREE PHASE SYSTEM

7.1 General Introduction

Recently grid connected wind energy conversion systems (WECS) are highly in demand due to the growing need for environmentally acceptable and sustainable energy sources. The properties of wind energy like its versatility and low environmental impact have rendered it as one of the most promising renewable energy sources. Thus, wind power generation has become very popular and a crucial component of today's power systems. However, the performance of WECS is highly dependent on wind characteristics, which are inherently intermittent and non-uniform in nature. These fluctuations cause uncertainty in the mechanical input power supplied to the wind turbine which will also vary the electrical power output of the wind energy system. These power fluctuations provide voltage instability, frequency variations, power quality issues, and increased strain on power electronic converters connected to grid. Hence, modern grid-connected WECS use advanced control algorithms, maximum power point tracking (MPPT) methods, and energy management systems to overcome these obstacles and maximize wind output while adhering to grid codes. This chapter discusses the modelling analysis and control of grid connected WECS. The emphasis is placed on understanding the impact of wind speed fluctuation on system performance. The modelling of three phase Least Mean Fourth (LMF) phase locked loop (PLL) is also done. This LMF PLL is used in Doubly Fed Induction Generator (DFIG) system for controlling the voltage angle calculation and detection of the output frequency which helps in fast and easy synchronization of the phase and frequency of the output frequency with that of grid voltage. The performance analysis of DFIG WECS grid integrated system is investigated under constant wind speed and dynamic performance analysis of LMF PLL are investigated under grid abnormalities like (i) 30% voltage sag (ii) 35% voltage swell, (iii) polluted grid, (iv) +5Hz frequency

jump, (v) 30^{o} phase shift and (vi) 20% dc -offset is done through simulation results. The simulation results and verified hardware results using OPAL RT simulator under variable wind speed is also discussed.

7.2 Modelling of DFIG system and LMF PLL

Dynamic performance analysis of a wind energy conversion system requires the modelling of the Doubly Fed Induction Generator (DFIG) wind turbine, it's rotor side and stator side control systems. Wind turbine (WT) is connected to the induction generator by a gearbox while DFIG's rotor windings are connected to the grid via back-to-back converters and the stator windings are directly connected to the power grid.

DFIG has certain benefits over permanent magnet synchronous generator (PMSG) in large scale wind turbine applications because of its robust and affordable partial scale power electronics converter topology [105]. DFIG uses low-cost power converter has lower losses and lower cooling requirements as these converters require 20-30% of rated power of the generator while PMSG are full-scale power converters so they are costly. DFIG provides decoupled control of both active and reactive power by using rotor-side converter control. This renders a flexible grid support including reactive power compensation and voltage regulations without the need for extra external equipment [115].

7.2.1 Modelling of DFIG Grid Integrated System

The simplified structural block diagram of DFIG WECS is shown in Fig. 7.1. It shows a wind turbine, gear box, DFIG and power electronics converter (PEC). It uses an LMF PLL in control algorithm for accurate tracking of phase angle and frequency for proper synchronization, control and operation within the electrical grid. DFIG used in this system is a wound rotor induction asynchronous machine. The stator windings are directly connected to the grid and the rotor windings are connected through back-to-back voltage source converters. The mathematical modelling of DFIG

mainly consists of two parts (i) mechanical system modelling and (ii) electrical system modelling.

A. Modelling of Wind Turbine and DFIG

Under mechanical modelling, the conversion of wind energy fed to the turbine through rotor blades into mechanical power, P_{mec} and mechanical torque, T_{mec} is given by

$$P_{mec} = \frac{1}{2}\rho A v_w^3 C_p \tag{7.1}$$

$$T_{mec} = \frac{1}{2}\rho A R v_w^2 C_t \tag{7.2}$$

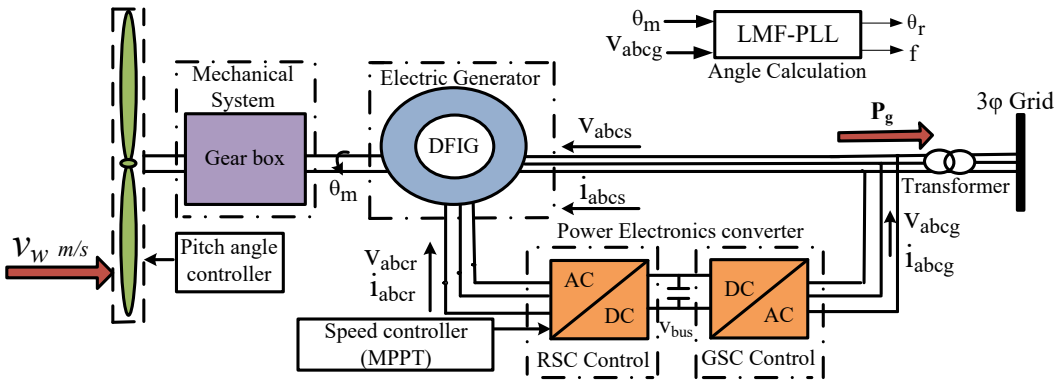


Fig. 7. 1 Structural block diagram of DFIG integrated with LMF PLL WECS

where A is the surface area of the turbine blade given in m^2 as $A = \pi R^2$ is the radius of turbine rotor, v_w is wind speed in m/s, ρ is the air density in kg/m^3. The power coefficients and torque coefficient are represented respectively as C_p and C_t. C_p represents the function of tip speed ratio λ and pitch angle β. The power coefficient, C_p is related to torque coefficient,C_t as

$$C_p = \lambda C_t \tag{7.3}$$

tip speed ratio is written as $\lambda = \frac{R\omega_t}{v_w}$ (7.4)

Here ω_t is the rotational speed of the turbine and R is the length of the turbine blade. The electrical modelling of DFIG due to the asynchronous wound-rotor induction machine starts by relating the stator and the rotor phase voltages ($\overline{v_s}$, $\overline{v_r}$) with currents

($\overline{\imath_s}$, $\overline{\imath_r}$), resistances (R_s and R_r) and fluxes in vector form and are expressed as [105]

$$\overline{v_s} = \overline{\imath_s}\, R_s + \frac{d\overline{\psi_s}}{dt} \tag{7.5}$$

$$\overline{v_r} = \overline{\imath_r}\, R_r + \frac{d\overline{\psi_r}}{dt} \tag{7.6}$$

When a balanced three phase voltage of frequency 'f' in Hz is provided to the three stator windings of DFIG, flux 'ψ_s' is induced in stator. It moves with a synchronous speed, ' n_s' which is expressed as

$$n_s = \frac{120*f}{p}\ rpm \tag{7.7}$$

where n_s is the synchronous speed in rpm and the number of poles is p. Thus, a DFIG turbine which has 4 poles and 50 Hz frequency will have a synchronous speed, $n_s = \frac{120*50}{4} = 1500\ rpm.$

The stator flux remains constant during stable condition. DFIG's stator flux ($\overline{\psi_s}$) and rotor flux ($\overline{\psi_r}$) in vector form can be expressed as

$$\overline{\psi_s} = L_s\overline{\imath_s} + L_m\overline{\imath_r} \tag{7.8}$$

$$\overline{\psi_r} = L_r\overline{\imath_r} + L_m\overline{\imath_s} \tag{7.9}$$

Here, L_s is the stator inductance which is expressed as

$$L_s = L_{ls} + L_m \tag{7.10}$$

L_r is rotor inductance which is given by

$$L_r = L_{ir} + L_m \tag{7.11}$$

where L_m is magnetising inductance, L_{ls} and L_{lr} are the leakage inductances of stator and rotor respectively. In DFIG, the slip speed which is the difference between stator and the rotor speed, gives the relative motion between the rotating magnetic field of the stator and rotor conductors. This relative motion induces rotor voltage which drives the rotor current. The slip frequency is given by

$$\omega_{slip} = \omega_s - \omega_r \tag{7.12}$$

The rotor angular speed of DFIG having 'p' poles and mechanical speed of rotor 'ω_m' in rad/s can be expressed as

$$\omega_r = p\omega_m \tag{7.13}$$

Substituting equation (7.13) to equation (7.12) we get equation (7.14)

$$\omega_{slip} = \omega_s - p\omega_m \tag{7.14}$$

Here ω_r is the rotor winding's angular speed in rad/s; ω_s is angular speed of stator windings in rad/s, ω_{slip} is the slip speed of rotor (rad/s). The rotor current is synchronized with the slip angle, θ_{slip} to control the rotor speed. Hence, the rotor currents can be controlled by aligning the control with the slip speed allowing both sub and super synchronous operation of DFIG. The slip angle is defined by the relationship

$$\theta_{slip}(t) = \theta_s(t) - \theta_r(t) \tag{7.15}$$

The stator angle, 'θ_s' is calculated using a PLL on the grid voltage and θ_r is the rotor mechanical angle.

B. Modelling of Grid Side Converter (GSC)

The grid side converter (GSC) of a DFIG wind turbine is connected between the rotor side converter (RSC) and grid through a DC-link. The GSC control method is shown in Fig. 4.2. It uses a decoupled dq current control with PI controllers and has two control loops (i) outer control loops and (ii) inner (current) control loops. The outer (voltage) control loops have a DC-link voltage controller which regulates DC link voltage (V_{dc}) to reference voltage (V_{dc}^*) reference. The PI controller output is a d-axis reference current, i_d^*. The outer loop control is also a power control loop and it also fixes the grid reactive power at unity power factor and an output q-axis reference current is obtained, (i_q). In the loops the current controllers are operating in dq synchronous frame.

GSC helps in keeping a constant DC-link voltage regardless of the rotor power fluctuations. The control of GSC is done in the dq reference frame which is aligned

with grid voltage. The relation between the stator and rotor voltage differential equations and current vectors of Doubly Fed Induction Generator at dq coordinates

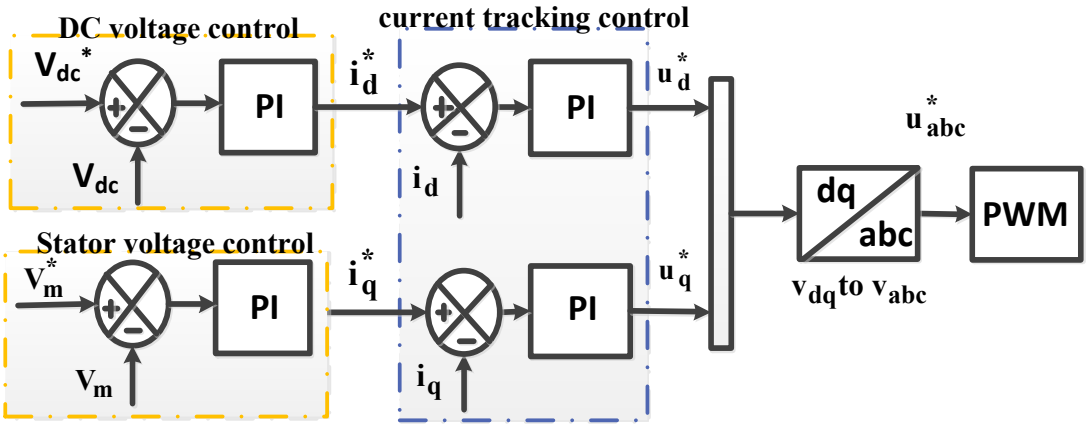


Fig. 7.2 Block diagram of control of GSC

can be written as [104]

$$\bar{v}_{sdq} = \bar{\imath}_{sdq}R_s + \frac{d\bar{\psi}_{sdq}}{dt} + j\omega_s\bar{\psi}_{sdq} \tag{7.16}$$

$$\bar{v}_{rdq} = \bar{\imath}_{rdq}R_r + \frac{d\bar{\psi}_{rdq}}{dt} + j(\omega_s - \omega_r)\bar{\psi}_{rdq} \tag{7.17}$$

where ω_s and ω_r are the stator and rotor angular frequencies.

The active and reactive powers at GSC can be expressed as

$$P_g = \frac{3}{2}(u_d i_{gd} + u_q i_{gq}) \tag{7.18}$$

$$Q_g = \frac{3}{2}(u_q i_{gd} - u_d i_{gq}) \tag{7.19}$$

where u_d and u_q, i_{gd} and i_{gq} are the dq components of grid voltage and currents respectively.

Since the q-component of voltage is zero i.e., $u_q = 0$ and $V_m = u_d$ as the voltage at d-axis the active and reactive power from (7.18) and (7.19) can be rewritten as

$$P_g = \frac{3}{2}(u_d i_{gd})$$

$$= \frac{3}{2}(V_m i_{gd}) \tag{7.20}$$

$$Q_g = \frac{3}{2}(u_d i_{gq})$$

$$= \frac{3}{2}(V_m i_{gq}) \quad (7.21)$$

GSC also regulates bidirectional active power flow to keep constant DC voltage; during the sub-synchronous operation the rotor absorbs power making GSC to deliver power to grid and at super-synchronous operation the rotor delivers power where GSC has to transfer power to grid. Finally, these reference voltages are converted into switching signals using sinusoidal PWM.

C. Modelling of Rotor Side Converter (RSC)

Fig.7.3 demonstrates controls of RSC through stator-flux-oriented dq reference frame. The dq transformation angle on the machine side correlates to the induction machine flux. The q-axis rotor current controller controls the electromagnetic torque which produce active power. The d-axis controls the reactive power or the stator voltage. The converter regulates the electrical power in the machine through q-axis current control. There are two current control loops, (i) the outer current control loop and (ii) inner current control loop. The outer loop consists of the torque and the reactive power control loop of RSC. The MPPT provides the outer loop reference and it is used to extract the wind's maximum power. The inner loop generates the q-axis voltage reference to follow the q-axis current reference generated by the outer loop. The current in dq axes restricts the current reference. The converter voltages are controlled by inner loop control allowing to follow the reference of the outer loop. RSC impose rotor voltages in dq-axes by PWM. Fig. 7.4 depicts the angle calculation of slip, rotor and stator where the LMF-PLL has been used to obtain the synchronized frequency the phase angle of the grid.

The RSC circuit independently controls the active and reactive powers to maximize the available power. In RSC, the Stator Flux Orientation (SFO) scheme is chosen for DFIG power regulation and it can also be decoupled. Proportional integrator (PI) controllers are tuned for controlling the converter currents which controls both active and reactive powers.

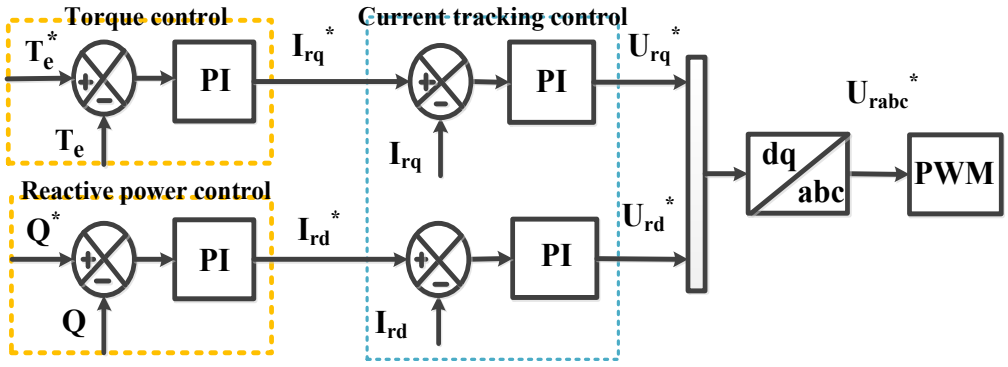


Fig. 7.3 Block diagram of RSC of DFIG integrated system [99]

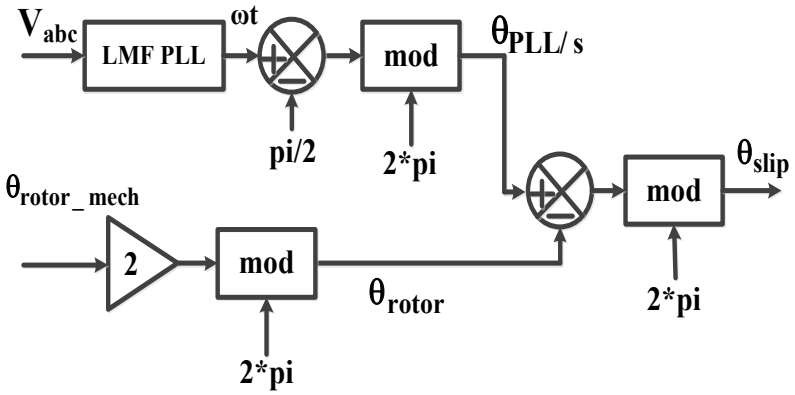


Fig. 7.4 Block diagram for angle calculation

7.2.2 Design of Least Mean Fourth Phase Locked Loop (LMF-PLL)

The least mean fourth (LMF) algorithm is a popular adaptive method recognised for its quick convergence and minimal steady state. The general block structure of the weight updation of LMF system and 3-phase LMF diagram are shown in Fig. 7.5 and Fig. 7.6.

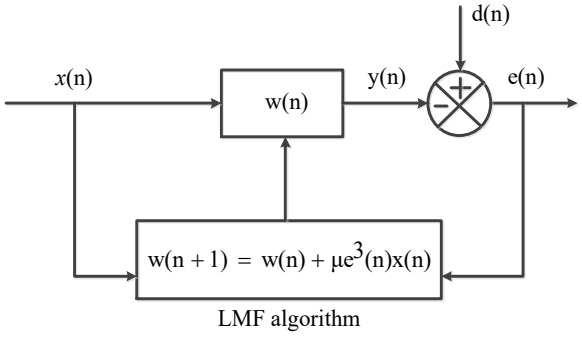


Fig. 7.5 Block structure for the weight of LMF system

The three phase grid input voltages fed to the phase detector (PD) of the LMF PLL

can be expressed as

$$v_a = V_m sin(\omega_{nf} t + \emptyset) = V_m sin\theta_{in} \tag{7.22}$$

$$v_b = V_m \sin[(\omega_{nf} t + \emptyset) - \frac{2\pi}{3}] = V_m sin(\theta_{in} - \frac{2\pi}{3}) \tag{7.23}$$

$$v_c = V_m \sin[(\omega_{nf} t + \emptyset) + \frac{2\pi}{3}] = V_m sin(\theta_{in} + \frac{2\pi}{3}) \tag{7.24}$$

The cost function of LMF scheme [139] is defined as

$$J(n) = E[e_{rr}^4(n)] \tag{7.25}$$

The error at the nth instant is given by

$$e_{err}(n) = d(n) - y(n) \tag{7.26}$$

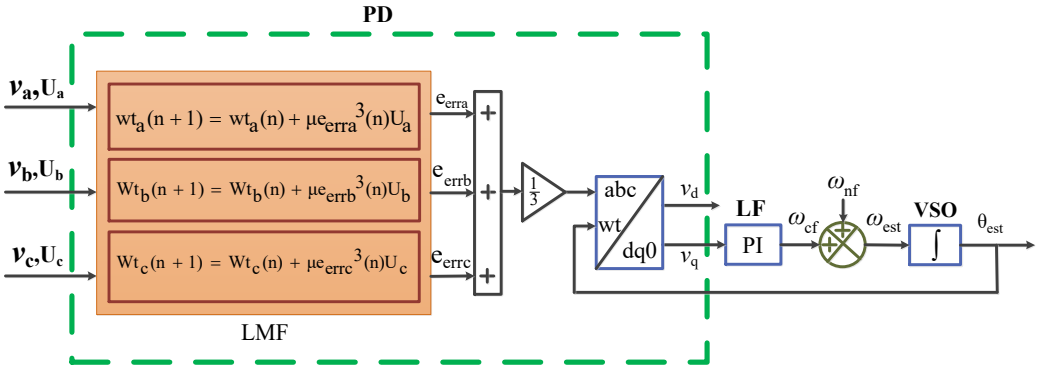


Fig. 7.6 The schematic block diagram of 3-Φ LMF PLL

The output of the system is expressed as

$$y(n) = Wt(n)^3\, u(n) \tag{7.27}$$

The vector form of the input signal having k samples

$$u_n^T = [u_n, u_{n-1}, \ldots\ldots\ldots u_{n-k+1}] \tag{7.28}$$

The weight adaptation for k samples is expressed as

$$Wt(n)^2 = [Wt_{1n}, Wt_{2n}, \ldots\ldots\ldots Wt_{nk}] \tag{7.29}$$

The gradient of (7.25) given by Widrow-Hoff rule is expressed as

$$\nabla(e_{err}^4(n)) = -4\mu e_{err}^3(n)u(n) \tag{7.30}$$

The weight updating equation of the LMF can be written as

$$Wt_{n+1} = Wt_n + 4\mu e_{err}^3(n)u(n) \quad (7.31)$$

Here u(n) is the input signal of 'n' interval and 'μ' is a constant which regulates the stability and convergence rate of the LMF PLL.

7.3 Performance Analysis of DFIG WECS with LMF PLL

The dynamic performance analysis of DFIG WECS with LMF PLL is observed in two cases, firstly under Case I. variable wind speed and secondly under Case II. constant wind speed but under adverse grid conditions like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage, (d) 30^o phase shift (e) +5Hz frequency change and (f) 20% DC offset. These disturbances are introduced during a time interval from 0.35s to 0.65s. The simulation results are obtained using MATLAB Simulink environment and experimental hardware set-ups are performed in the laboratory for three phase system to obtain the experimental results. The experimental results of the three phase DFIG WEC and LMF PLL models are obtained from the laboratory set up consisting of a Digital Signal Oscilloscope (DSO) (Infinite Vision DSO-X-2014A), host personal computer (PC) and Real-Time Simulator (OPAL-RT OP4312) as shown in Fig. 7.7.

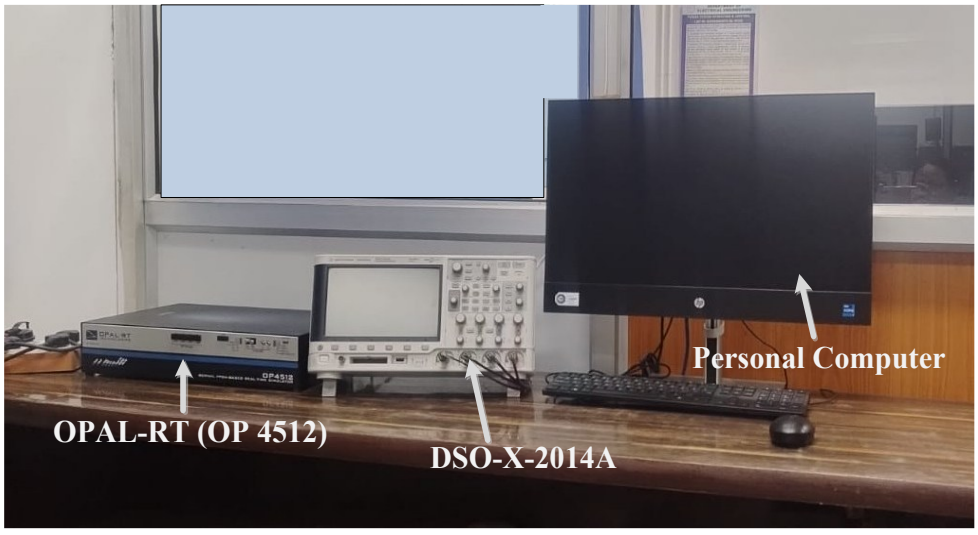


Fig. 7.7 Experimental set-up using OPAL-RT (OP4512) for validating the simulations results of DFIG model.

A DFIG wind energy conversion system (WECS) is selected as a asynchronous wound rotor machine having a nominal power of 1KVA, 320V (Vrms), and 50 Hz frequency wind turbine. It is integrated with LMF-PLL to synchronize the phase angle and frequency of the system. Table 7.1 gives the parameters of the WECS system. The simulation and the experimental results of dynamic performance of DFIG WECS is analysed under variable wind speed to observe the three stages of operation of rotor speed (i) sub synchronous speed (ii) synchronous speed and (iii) super synchronous speed. The dynamic performance of DFIG and LMF PLL under grid abnormalities is analysed with a constant wind speed (8m/s).

Table 7.1: Specifications and Parameters of DFIG

Name of the parameter	Value	No. of poles	4
Stator frequency (Hz)	50	Stator resistance (ohm)	9.7 Ω
Rated stator power (VA)	P=1KVA	Leakage inductance of stator(H)	0.0489
Synchronous speed (rpm)	1500	Rotor resistance referred to stator (ohm)	10.7 Ω
Rated stator voltage (Vs)(Vrms)	400V	Leakage inductance of rotor(H)	0.0903
Air gap flux (Wb)	0.588	Magnetizing inductance (H)	0.705

7.3.1 Simulation Results under Variable Speed

The simulation results of DFIG under variable wind speed for the dynamic performance is shown in Fig. 7.8. This figure shows the responses of DFIG WECS like response of rotor speed in rpm, three phase rotor current (A), three phase stator current (A), slip angle (rad/s), electrical angle of rotor (rad/s), frequency of the system (Hz), wind speed (m/s), electromechanically torque (N/m), rotor flux (Wb), active and reactive power of rotor, rotor voltage (V), active and reactive power (kW) and three phase voltages of the stator(V). Fig. 7.8 shows that the rotor speed varying from 1132

rpm to 2010 rpm while wind speed varies from 7.5m/s to 13.4m/s. The synchronous speed of the rotor is 1500 rpm which is obtained at 10m/s wind speed. The RSC feeds the three-phase ac current, i_{abc} into rotor winding with rotor frequency (f_r). As rotor current depends on the slip, s, ($f_r = sf$). As a result, in rotor current and rotor slip response the three modes of operations can be seen. Hence, the rotor current, slip angle responses of the DFIG during the variable wind speed operation show the phase sequence alterations of sub synchronous, synchronous and super synchronous mode of operations. The electrical angle of LMF PLL is not affected with variation in speed. The stator frequency attains 50 Hz and remain constant throughout. The three phase stator voltages remain unchanged. During sub synchronous speed ($\omega_r < \omega_s$) the power flows into the rotor from the grid by back-to-back converters of DFIG. Hence,

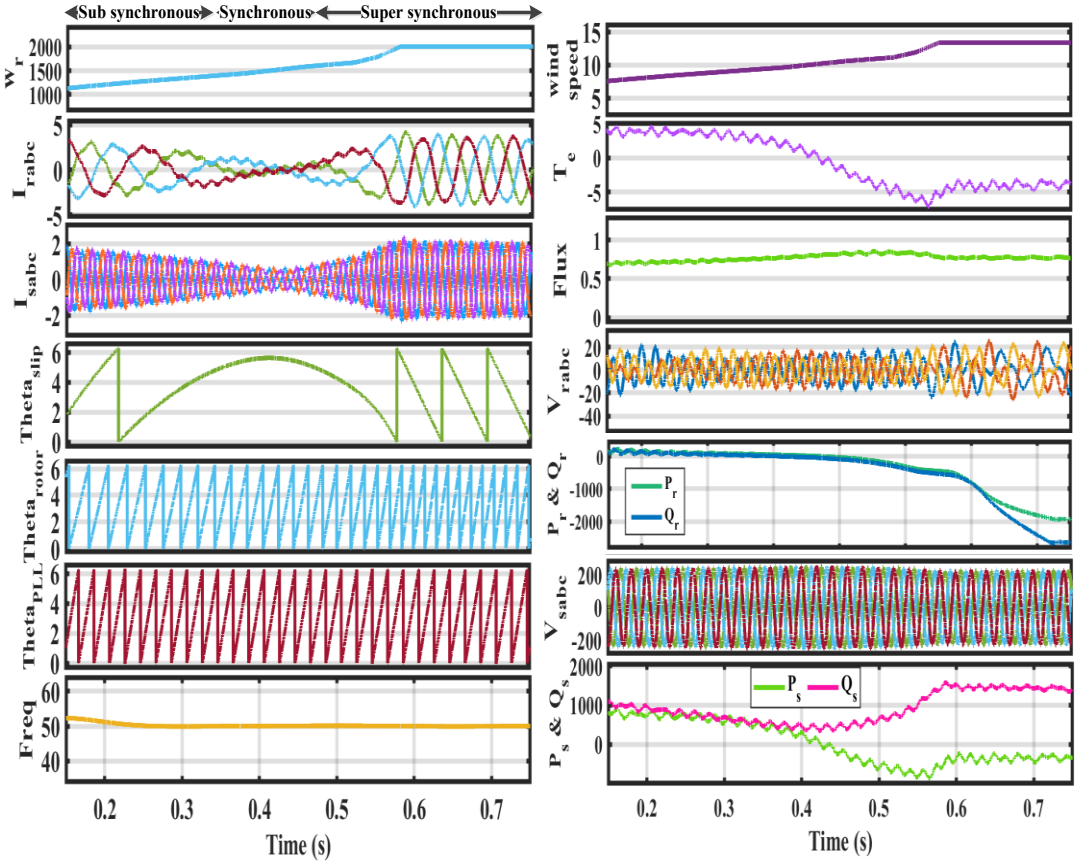


Fig.7.8 Simulated results of DFIG wind turbine under variable wind speed

extra electromechanical torque, T_e is required and RSC acts as an inverter and GSC acts as rectifier by drawing power from grid to feed dc-link. During synchronous speed, ($\omega_r = \omega_s$), active power is delivered through the stator and RSC is used only

for excitation by providing controlled DC current to the rotor and it does not generate any power. Minimal torque is produced in this region. During the super synchronous speed, the electromagnetic torque decreases and goes negative. The rotor flux in this super synchronous speed increases slightly due to higher slip frequency. The stator power is more negative making DFIG to act as generator delivering power to grid. The rotor power becomes more negative supplying more power to the grid along with stator power.

7.3.2 Simulation Results under Adverse Grid Abnormalities under Constant Speed

The simulation results are taken under abnormal conditions of grid like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset. The disturbance has been injected for a duration of 0.35s-0.65s. The dynamic performance of DFIG under 30% sag of grid

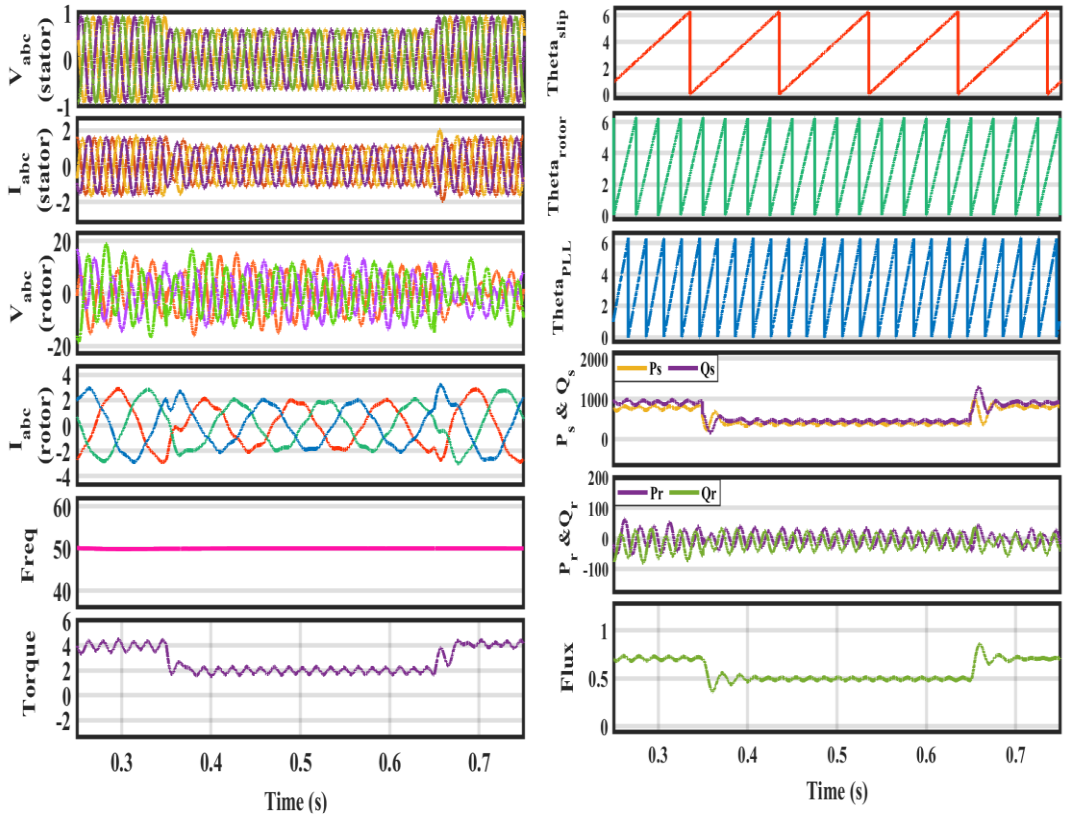


Fig.7.9 Simulated results of dynamic performance of DFIG wind turbine under 30% grid voltage sag

voltage is shown in Fig. 7.9. It shows the stator voltage and current dip in the response of stator voltage (p.u) and current (p.u), rotor voltage (p.u) and current (p.u), frequency of the system in Hz, torque, phase angle of slip, rotor and PLL, the active and reactive powers of stator and rotor, the stator flux. The stator voltage shows 30% dip in magnitude. The rotor voltage and current are distorted during the transient period. The magnitude of electromagnetic torque falls during the disturbed period. The active and reactive power of stator show fall in magnitude. The flux also falls during the transient period. The torque, power and flux observed some ripples which settles down within two cycles.

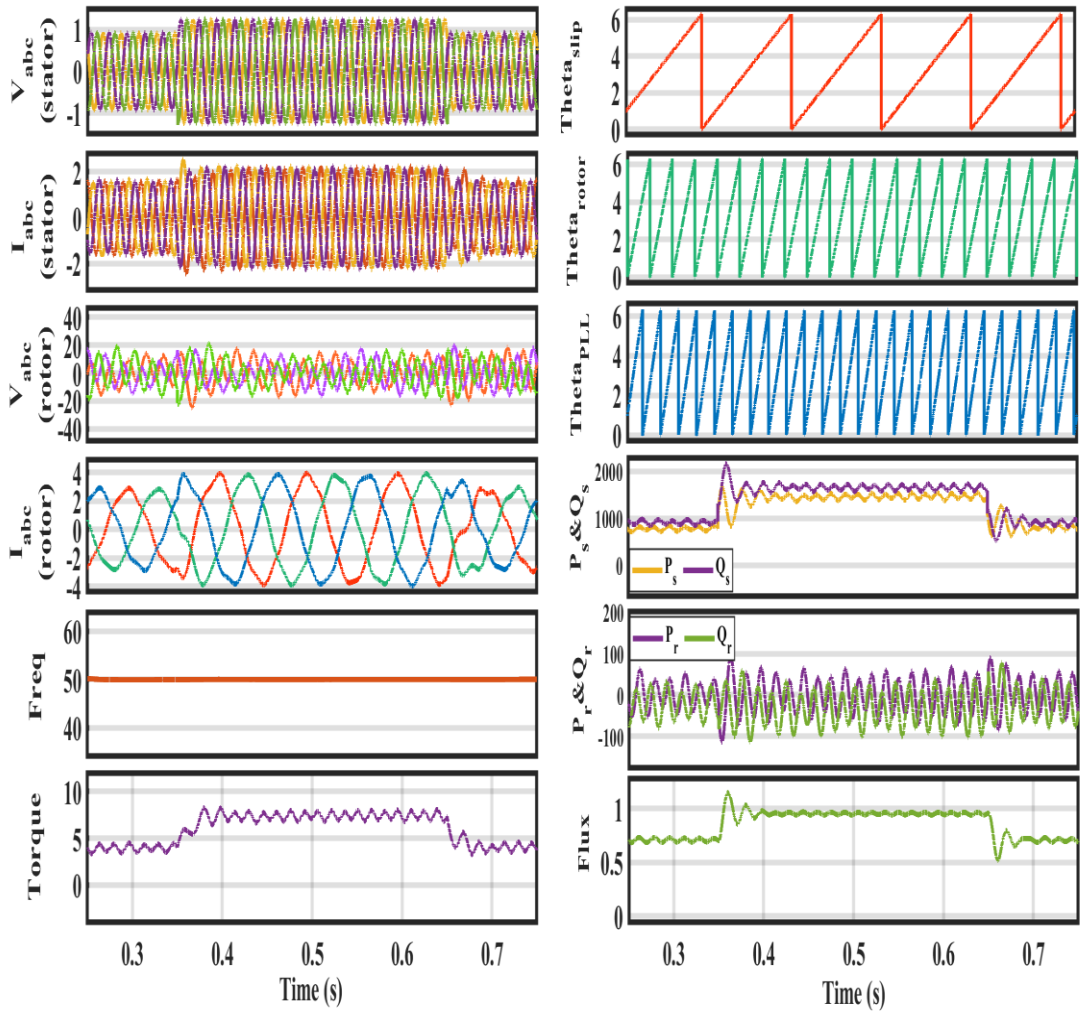


Fig.7.10 Simulated results of dynamic performance of DFIG wind turbine under 35% grid voltage swell

The simulation results of dynamic performance of DFIG wind turbine under 35% grid voltage swell is shown in Fig. 7.10. The stator voltage and current show

swell in their magnitude. The rotor current is also increased during disturbance. The frequency remains unchanged. The electromagnetic torque is increased. The phase angle of slip, rotor and LMF PLL does not show any distortion. There is overshoot and increased magnitude in the active power of the stator which dies down within two cycles while its reactive power shows very small overshoot but with increased magnitude. The active and reactive power of rotor do not show significant change. The stator flux is increased observing an overshoot which dies down within 2 cycles.

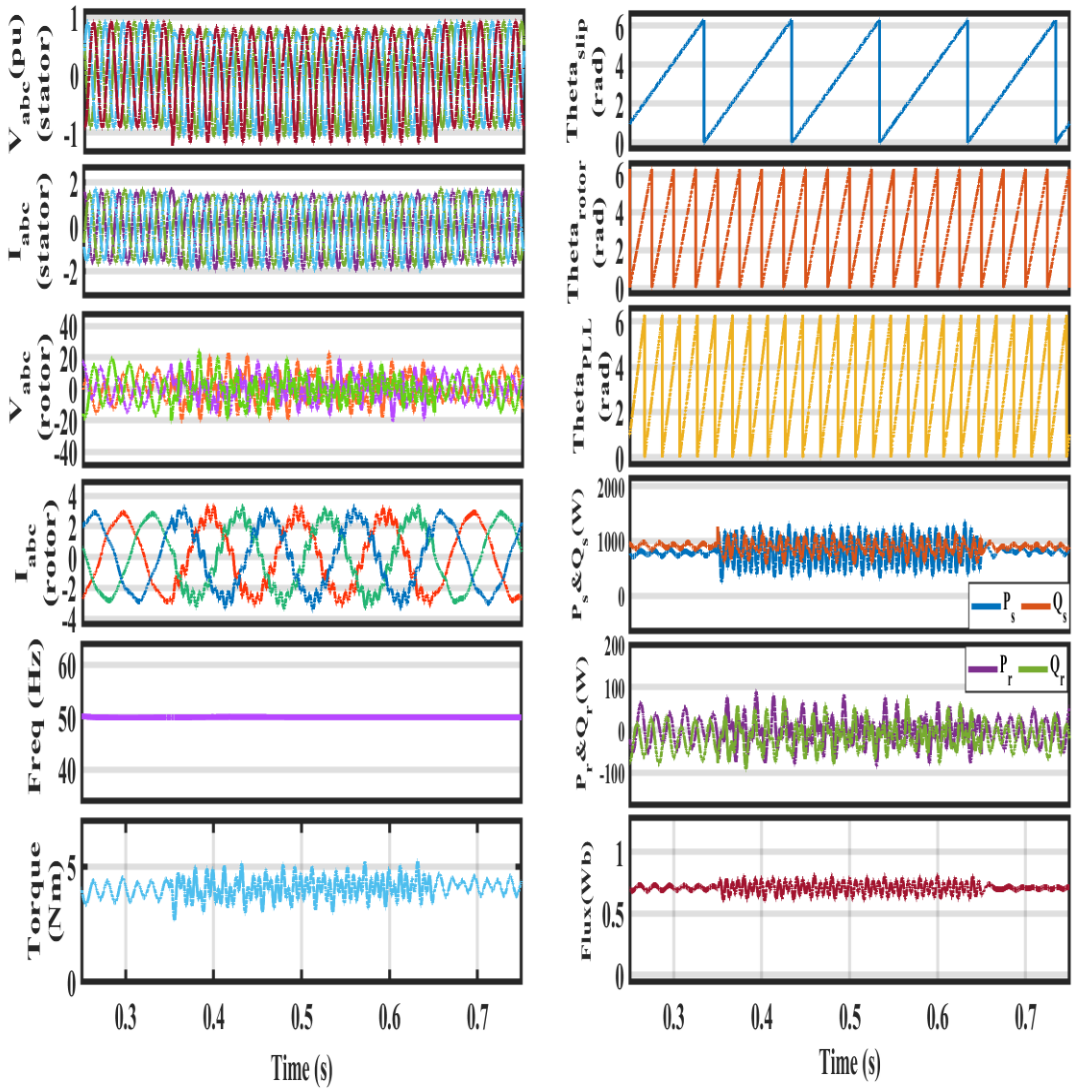


Fig.7.11 Simulated results of dynamic performance of DFIG wind turbine under polluted grid voltage

The simulated results of dynamic performance of DFIG wind turbine under polluted grid voltage is shown in Fig. 7.11. Distorted signals of stator voltage and

current, rotor voltage and current are observed due to harmonics in grid voltage. The electromagnetic torque, the stator power and flux show oscillatory response to this disturbance. The rotor powers are also distorted. The frequency response does not show any change.

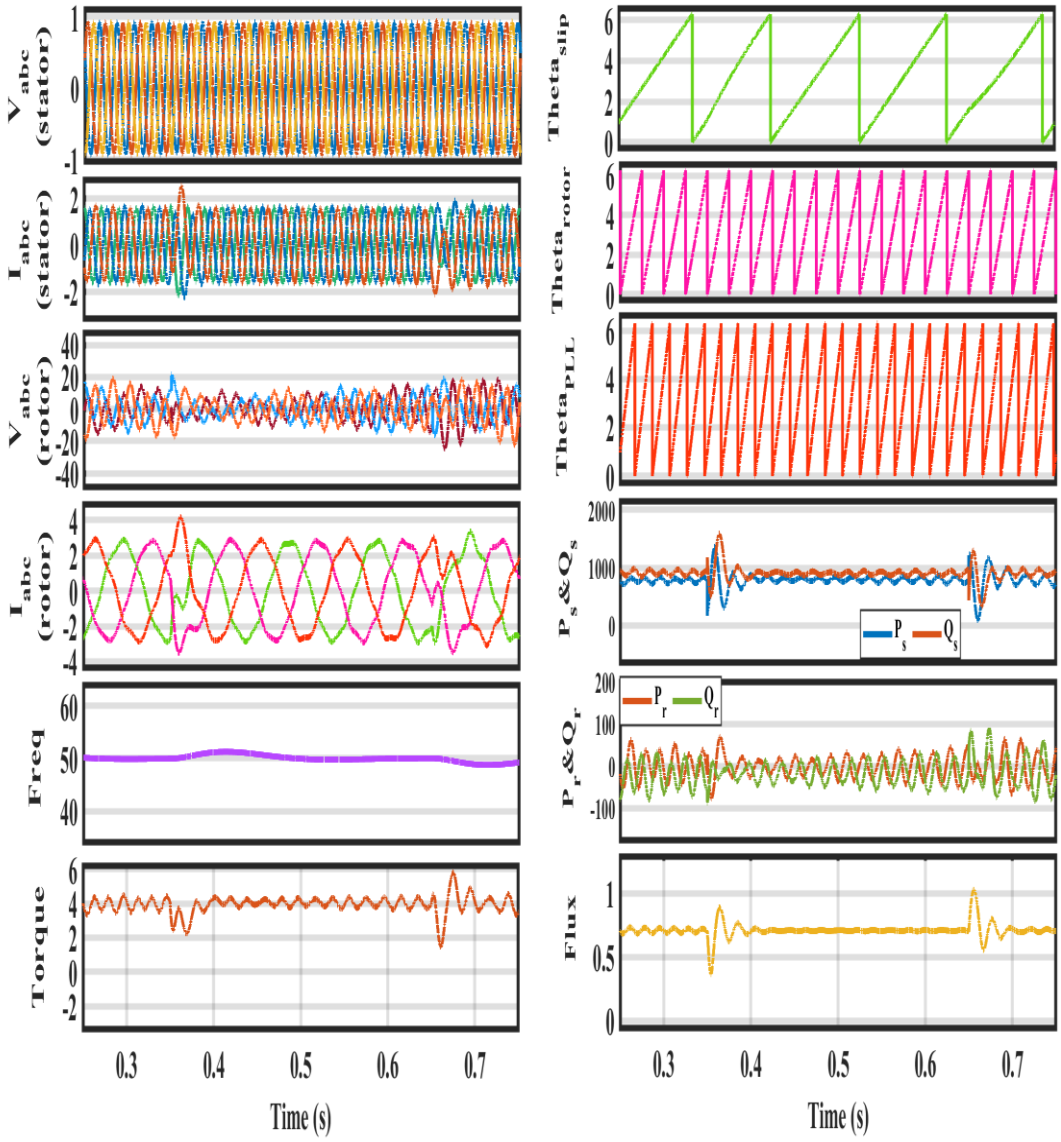


Fig.7.12 Simulated results of dynamic performance of DFIG wind turbine under 30° phase shift

The simulated results of dynamic performance of DFIG wind turbine under 30° phase shift is shown in Fig. 7.12. During phase shift overshoot in stator and rotor current which dies down within one cycle is seen in dynamic response analysis. The torque also shows the spike but in inversed form. The phase angles remain unchanged.

The frequency response shows slight overshoot. It is also observed that the overshoot in torques, stator and rotor current, rotor voltage, flux, stator and rotor power responses settle down fast.

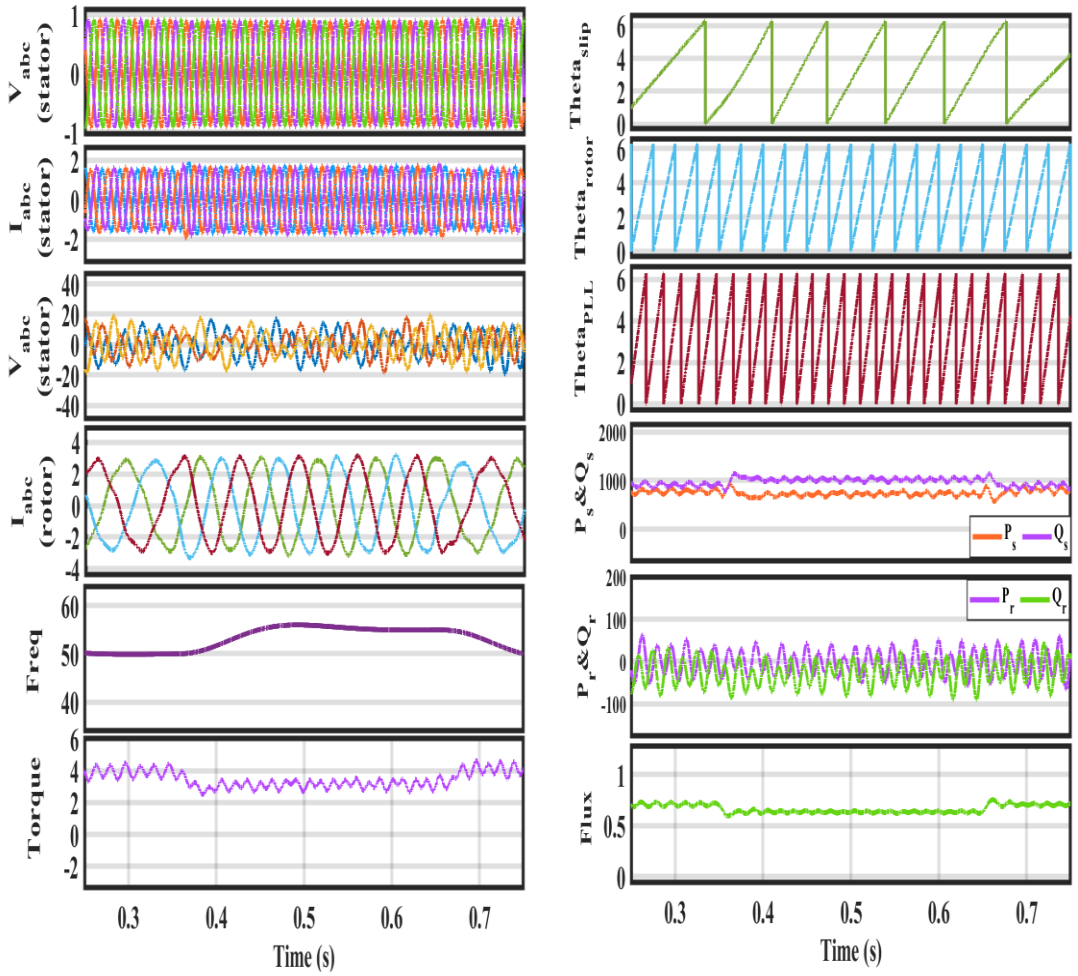


Fig.7.13 Simulated results of dynamic performance of DFIG wind turbine under +5Hz frequency shift

The simulation results of the dynamic performance of DFIG wind turbine under +5Hz frequency shift is shown in Fig. 7.13. During this disturbance the electromechanical torque and stator flux has decreased magnitude. The active and the reactive power of the stator are decoupling.

Fig. 7.14 shows the dynamic response under the presence of 20% DC offset in grid voltage. The presence of DC offset is seen in stator voltage. The rotor current waveform is seen to be distorted. The rotor voltage magnitude is reduced. The reactive

power is greater than the active power. The frequency response remains unchanged. The torque gives negative response. The flux shows positive response.

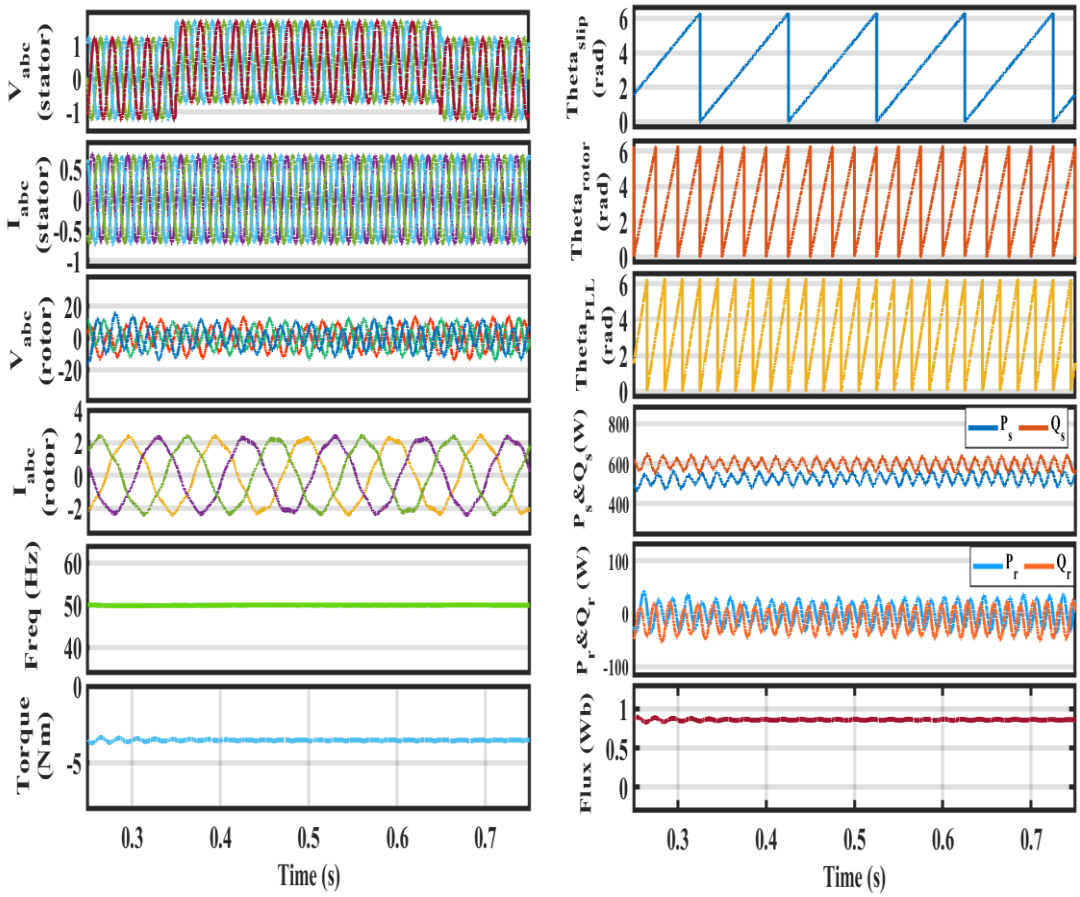


Fig.7.14 Simulated results of dynamic performance of DFIG wind turbine under 20% DC-offset.

7.3.3 Experimental Results of DFIG WECS under Variable Speed

An experimental set up with a real-time hardware-in-the-loop (HIL) system is created in the laboratory to validate the simulation results obtained in Matlab SIMULINK. The experimental set up consists of a Digital Signal Oscilloscope (DSO) (Infinite Vision DSO-X-2014A), personal computer (PC) and the real-time HIL system consists of an OPAL-RT real-time digital simulator (OPAL-RT OP4312). The experimental results for analysing the dynamic performance of DFIG wind turbine under variable speed are given in Fig.7.15, 7.16, 7.17, 7.18 and 7.19. The responses of the variable rotor speed in rpm and that of the three phase rotor currents are shown in Fig. 7.15. The results depict the three modes of operations of rotor speed. With sub-

synchronous speed the of rotor the currents have positive sequence frequency letting sequence and the power flow into the rotor. The rotor current is zero at synchronous speed, behaving like a synchronous generator and at super synchronous speed it has negative sequence hence power flows out from the rotor. Fig. 7.16 shows the response of stator flux, and slip angle, rotor angle and angle of LMF-PLL. The flux remains constant due to continuous voltage and current injection into the rotor by RSC. The slip angle is changed in all the three modes of speed operations. It changes from positive at sub synchronous speed to negative or reverse in super synchronous speed.

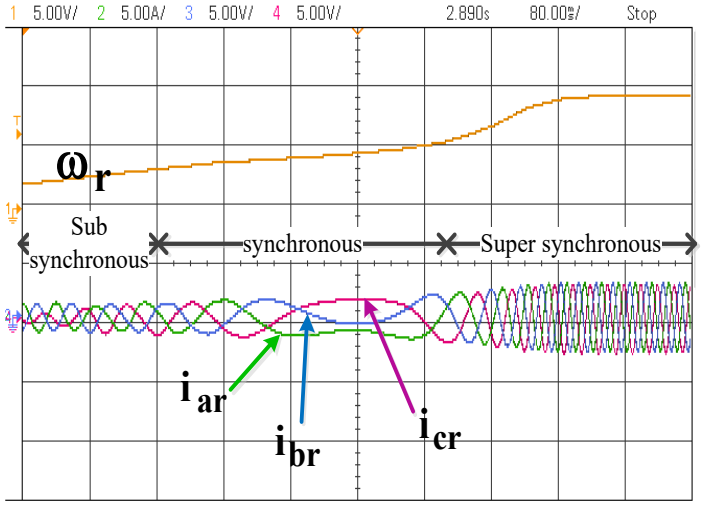


Fig.7.15 Experimental results of dynamic performance of DFIG wind turbine under variable wind speed showing rotor currents and variable rotor speed

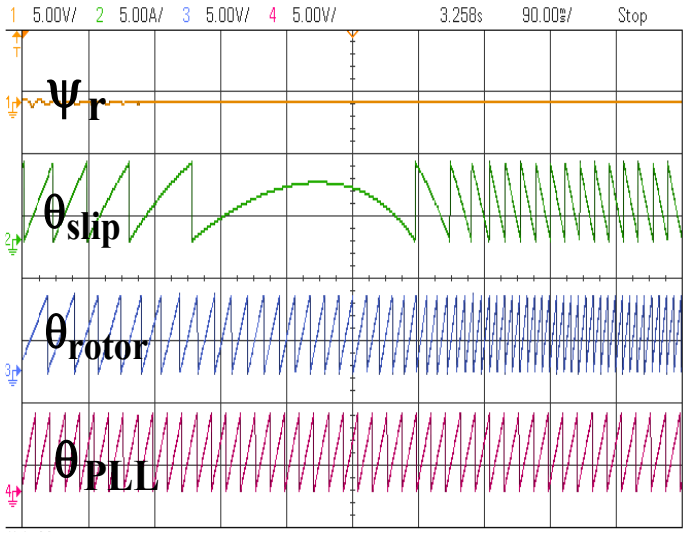


Fig.7.16 Experimental results of dynamic performance of DFIG wind turbine under variable wind speed showing the flux, phase angles of slip, rotor and LMF-PLL

The rotor angle and LMF-PLL appears to move slower during sub-synchronous speed while in super synchronous speed it moves faster in positive direction. Similarly, the phase angle of LMF-PLL shows positive behaviour during the entire modes of operation. Fig. 7.17 shows the experimental results of the active and reactive powers of the dynamic performance of DFIG wind turbine under variable speed.

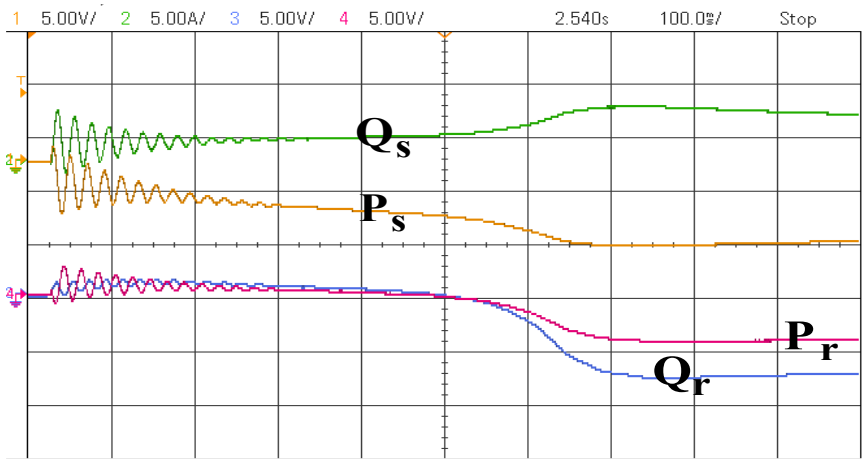


Fig.7.17 Experimental results of dynamic performance of DFIG wind turbine under variable wind speed showing the active and reactive powers of the stator and rotor

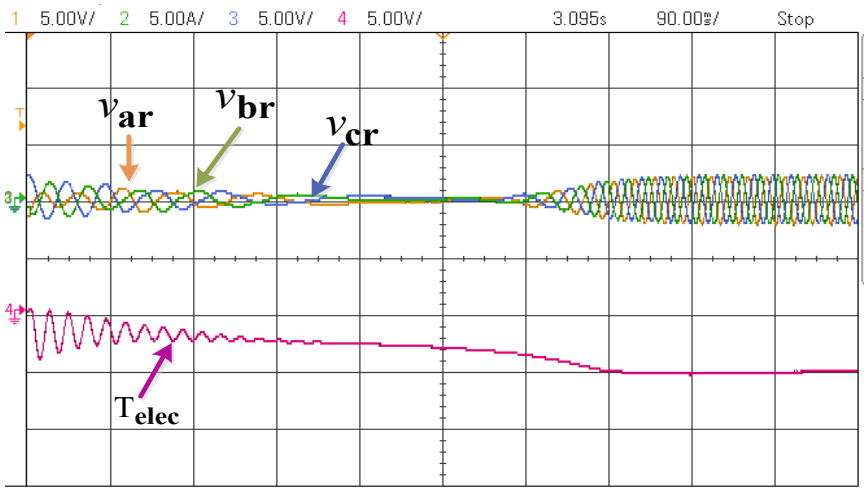


Fig.7.18 Experimental results of dynamic performance of DFIG wind turbine under variable wind speed showing three phase rotor voltages and electromechanical torque

The experimental results of the dynamic performance of DFIG wind turbine showing the three phase rotor voltages and electromagnetic torque are shown in Fig. 7.18. Rotor voltages show increased magnitude in sub-synchronous speed and during the synchronous speed the three phase voltages magnitude becomes zero and during

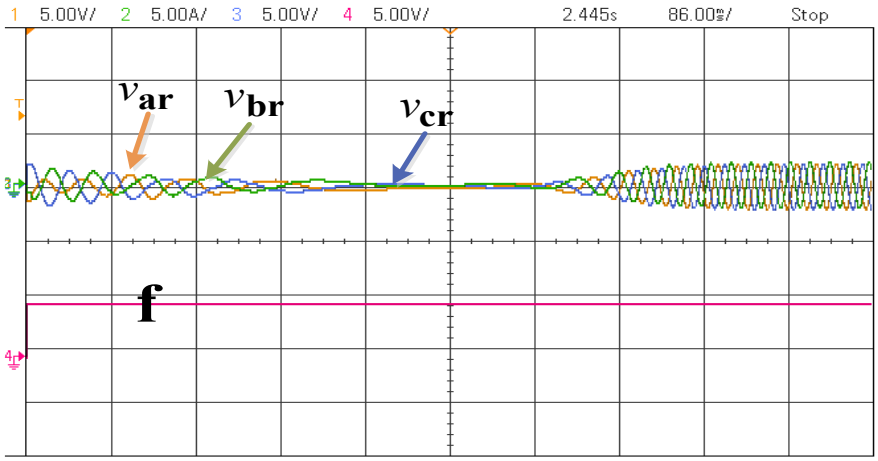


Fig.7.19 Experimental results of dynamic performance of DFIG wind turbine under variable wind speed showing three phase rotor voltages and frequency

the synchronous speed the three phase voltages magnitude becomes zero and during the super-synchronous speed the magnitude of the voltages are increased but in reverse phase sequence increased. Similarly, the electromagnetic torque during sub-synchronous speed is positive which is a generating torque and during synchronous speed the torques is reduced and further reduced during super synchronous speed. Fig. 7.19 shows the experimental results of dynamic performance of DFIG wind turbine under variable wind speed showing three phase rotor voltages and frequency. This plot shows that the voltages changes during the three modes of speed operation but the fundamental frequency of the system remains unchanged during the three modes of speed operation.

7.4 Performance Analysis of LMF-PLL under Adverse Grid Conditions under Constant Speed

The dynamic performance of LMF-PLL under adverse grid conditions like like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset. The disturbance has been injected for a duration of 0.35s-0.65s and tested under Matlab SIMULINK environment. The analysis of dynamic performance of LMF-PLL has been plotted considering phase 'a' of the stator voltage, v_a (V), sin theta (rad), frequency in Hz and angle of PLL, theta in rad. The performance analysis is shown in 7.20.(a) under 30% voltage sag and (b)

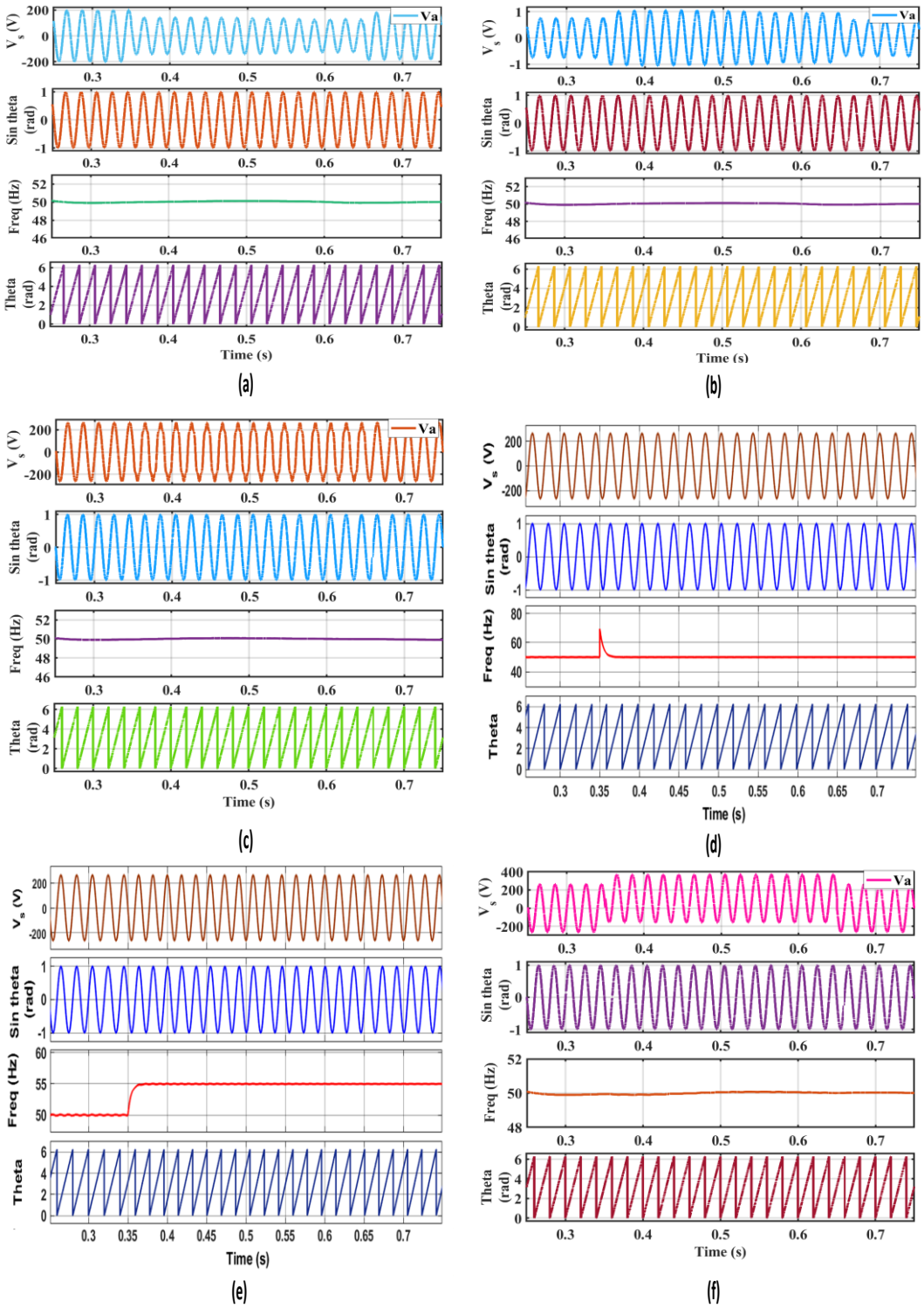


Fig.7.20 Simulation results of the dynamic performance of LMF PLL under constant speed under grid abnormalities like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset.

35% swell in the grid voltage, the stator voltage only shows changes in its magnitude.

Fig. 7.20 (c) shows the simulation under polluted grid environment. The voltage source

shows the presence of harmonics in the voltage signal. Fig. 7.20 (d) shows the simulation results under 30° phase shift. The frequency response shows an overshoot which dies down within one cycle. The grid voltage response also shows the presence of 30° phase shift. Fig. 7.20 (e) shows the simulation result under +5 Hz frequency change. The frequency response shifts +5 Hz. The supply voltage and phase angle theta do not show changes. Fig. 7.20 (f) shows the simulation results under 20% DC offset. The supply voltage shows the presence of DC component in this experimental result in Fig. 20 (f). The sin theta response and the supply voltage response of phase a are in phase with each other. The phase angle theta shows no significant change. The is a very slight change in the frequency response.

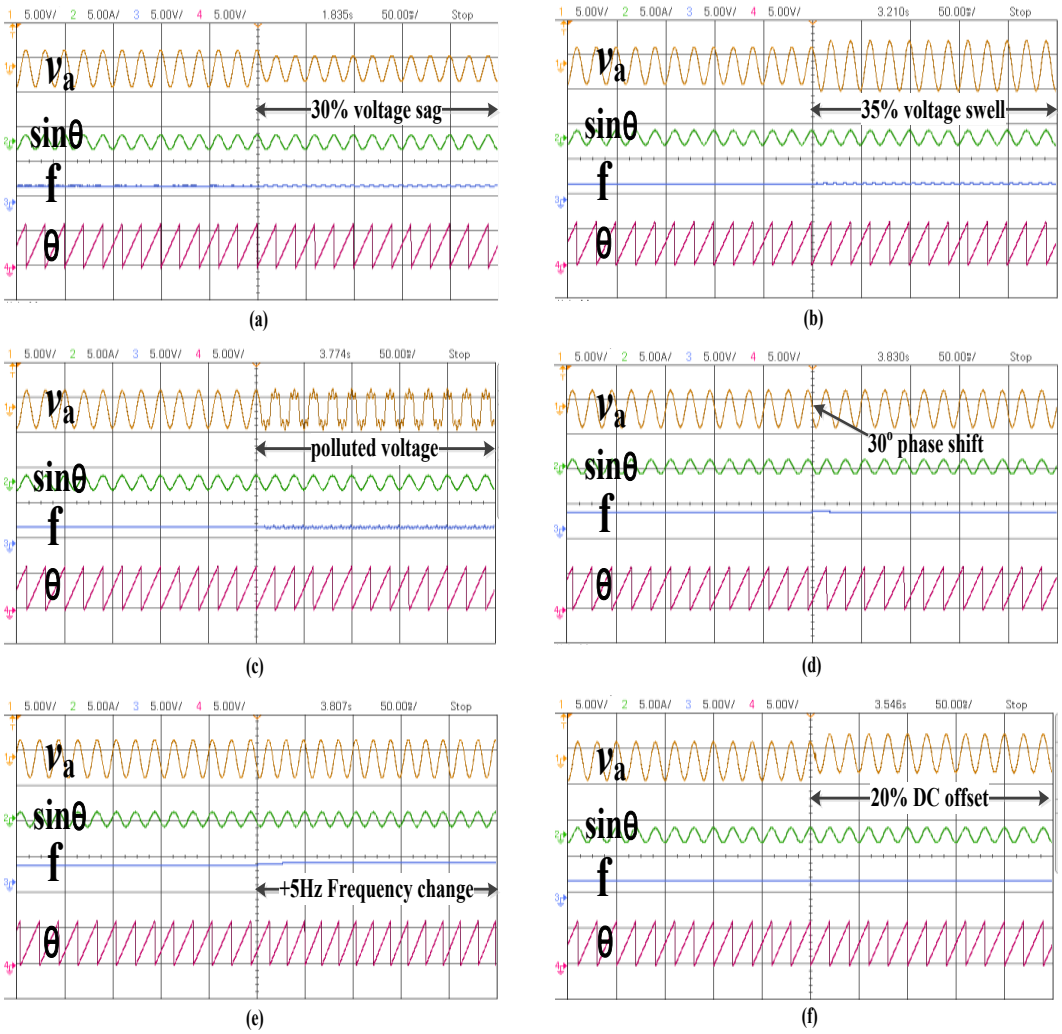


Fig.7.21 Experimental results of the dynamic performance of LMF PLL under constant speed under grid abnormalities like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30° phase shift (e) +5 Hz frequency change and (f) 20% DC-offset.

The hardware results of LMF PLL are shown in Fig. 7.21 considering the responses of grid voltage, v_a in volts, sine theta, frequency in Hz and phase angle in radians of PLL. The hardware results are taken under constant speed of 8m/s considering the grid abnormalities like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30^o phase shift (e) +5 Hz frequency change and (f) 20% DC-offset. Fig. 7.21 (a) and Fig. 7.21 (b) show the plots of three phase LMF PLL responses under 30% grid voltage sag and 35% grid voltage swell abnormalities respectively. The grid voltage signals show 30% voltage drop and 35% voltage swell in the responses. The frequency response and the phase angle response do not show prominent changes during these disturbances. Fig. 7.21 (c) shows the response of LMF PLL under polluted grid voltage. The frequency response does not show significant change. The phase angle also does not show prominent visible change. Fig. 7.21 (d) shows the experimental result under 30^o phase shift. The frequency response shows overshoot which settles down within one cycle. Fig. 7.21 (e) shows the frequency response under +5Hz frequency change. Fig. 7.21 (f) shows plot of responses under 20% DC offset. The voltage signal response shows the presence of DC offset while frequency, phase angle does not show prominent changes.

7.5 Conclusions

In this chapter the mathematical model of three phase DFIG WEC with LMF-PLL has been discussed. The modelling of RSC and GSC has been discussed in this chapter. A new LMF PLL's mathematical modelling has also been done. This LMF - PLL is used for rotor angle calculation, the dynamic performance of DFIG has been studied under both (a) variable wind speed and (b) constant wind speed. Under variable wind speed study, the three modes of speed operation are observed in DFIG dynamic performance. The simulation and experimental results using Matlab SIMULINK environment and experimental results using OPAL RT lab setup and it is found that the results are validating each other. Under constant wind speed the dynamic behavior of DFIG system is studied under various grid abnormalities like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30^o phase shift (e) +5 Hz frequency change and (f) 20% DC-offset when the disturbance has been injected for a duration

of 0.35s-0.65s. the performance is found to be satisfactory under these grid abnormalities. Moreover, the dynamic performance of the LMF-PLL is also tested under grid abnormalities and the performance is found satisfactory.

Chapter 8

CONCLUSION AND FUTURE SCOPE

8.1 Conclusions

Chapter 1 discusses the introduction to synchronization techniques for control of power electronics converters in electrical power system, role of synchronization techniques, issues involved in synchronization of integrated systems, classification of synchronization techniques and some challenges and solutions in the synchronization of integrated systems.

Chapter 2 discusses an extensive literature survey that includes the classification of synchronization techniques in electrical power system. The techniques are classified into various types depending on the type of connection like single phase and three phase, presence or absence of the feedback mechanism like open loop and closed loop synchronization techniques. It includes an extensive survey covering the conventional and advanced techniques of PLL and FLL and other forms which are used as synchronization techniques to improve the dynamic performance of grid integrated system. Several papers have also listed the applications of their designed techniques in Photovoltaic (PV) system, doubly fed induction generator (DFIG) wind energy converter system and electric vehicles (EV) based systems.

Chapter 3 The mathematical modelling for the design of the conventional single phase PLL like SRF, SOGI and LMS are done and their transfer functions are estimated. Similarly, two three phase PLLs such as SRF and LMF PLL are also modelled and developed their transfer functions. The developed transfer functions of the single phase PLLs (SRF, SOGI, LMS) and three phase PLLs (SRF, LMF) are used to study the steady state stability with Nyquist plot method. All the PLLs are found to be stable. The simulated and the experimental results are obtained under grid disturbances like (i) 30% voltage sag (ii) 35% voltage swell (iii) polluted grid voltage, (iv) 30^{o} phase shift (v) +5Hz frequency change and (vi) 20% DC offset. The experimental results validate the simulation results. For three phase PLLs, the conventional SRF PLL and

LMF PLL are modelled and their respective transfer functions are estimated. The steady state dynamic performances are studied with simulated and experimental results. The experimental results are found to be validating the simulated results. From the results it is seen that the frequency response under 30%voltage sag, 35% voltage swell, polluted grid voltage and DC-offset seen to remain almost unaffected. Hence, the comparative analysis of three phase SRF and LMF PLLs are tabulated considering 30^{o} phase shift and +5Hz frequency change grid disturbances. LMF PLL is found to be better PLL than SRF.

Chapter 4 discusses the modelling of three types of PLLs is performed starting from general approach of modelling for different types and orders of a PLL. Type I PLL considered for modelling is quasi-Type I PLL where MAF is used as controller with only proportional gain as loop filter. The presence of VCO as a basic component in the structure of PLL make this quasi type PLL as Type I PLL by structure but Type II by control. A pure Type I PLL which contains only one integrator as VCO does not perform well under grid disturbances. Type II PLL considered is SRF PLL as it contains two integrator each from PI controller used as loop filter and integrator from VCO structure. The Type III PLL considered is Enhanced PLL with presence for three integrators for better performance. From the stability through Bode plot of all the three PLLs considered indicate their dynamic stability although Type II and Type III indicate absolute stability. The simulated and experimental responses under various grid abnormalities like (a) 30% grid voltage sag (b) 35% grid voltage swell, (c) polluted environment (d) 30^{o} phase shift, (e) +5Hz frequency change, (f) 20% dc-offset validate each other. Table 4.4 gives the summary of the dynamic performance analysis of the three types of PLLs under various grid abnormalities. Type III PLL gives the best overall frequency response even in the the presence of polluted grid voltage and DC offset disturbance. Among the three types of PLLs, Type I PLL is the most badly affected PLL under all grid disturbances. The dynamic performance of Type II PLLs is better than Type I but worse than Type III PLLs.

Chapter 5 discusses the mathematical modeling of three PLLs viz. (i) integral order MSRF-PLL, (ii) FO-LP MSRF-PLL with one fractional-order ‘a’ and (iii) FO-LPFO-PI MSRF-PLL with two fractional-order ‘a’ and ‘b’ coefficients is performed. The

three PLLs are designed and their open-loop, closed-loop and error-loop transfer functions are mathematically developed. The open-loop and closed-loop Bode diagrams of FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL are plotted to predict optimum values of 'a' and 'b' considering PLL stability. As FO-LPFO-PI MSRF-PLL has two fractional order parameters 'a' and 'b', the Bode diagrams of FO-LPFO-PI MSRF-PLL are plotted for various values of 'a' with fixed 'b' as 1 in one case and in another case with various values of 'b' for fixed 'a' as 1. The Bode diagrams helped to optimize the fractional parameters 'a' and 'b'. The selected optimized values of fractional-order coefficients are 'a'=1.1 and 'b'=0.1 which are finally selected for the FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL.

The dynamic performance analysis for the conventional integral order MSRF-PLL and fractional-order FO-LP MSRF-PLL and FO-LPFO-PI MSRF-PLL is performed under different grid abnormalities like 30% grid voltage sag and 35% grid voltage swell, 3rd and 5th harmonics polluted voltage, 30% phase shift, +5Hz frequency change and 20% Dc-offset voltage supply. Both the simulated and experimental comparative analysis is performed rigorously. The comparative results predict that among the integral order and fractional order PLLs, FO-LPFO-PI MSRF-PLL with two fractional-order parameters 'a' and 'b' gives the best performance results during the grid abnormalities. Moreover, this PLL is more stable as compared to FO-LP MSRF-PLL after optimizing the values of 'a' and 'b' parameters.

Chapter 6 discusses the design and modelling of H-LMS-SOGI PLL is investigated and analysed in detail. The performances of the five PLLs viz. SOGI, LMS and three cascaded PLLs under adverse grid conditions is analysed through simulation using MATLAB Simulink toolbox (2020A). The designed mathematical modelling of the three PLLs is discussed and the selection of the control parameters 'μ'of LMS and 'k' of SOGI is done through Bode plot and pole-zero plots. The simulated results are validated through hardware results by setting up a laboratory prototype using a $1-\emptyset$ programmable supply of GwinSTEK model (APS-1102A). The stability of the three PLLs are analysed through of the gain margin (GM) in dB and phase margin (PM) in degree. The enhanced stability of the novel H-LMS-SOGI PLL is further validated by the pole-zero plot in complex plane and H-LMS-SOGI PLL is more stable than the

other two cascaded PLLs due to larger values of positive GM and PM. The dynamic performance under steady state analysis of H-LMS-SOGI PLL, CLMS PLL, and CSOGI PLL is performed under adverse grid conditions considering six test conditions viz. (a) Grid voltage deviation with 30% sag (b)Grid voltage deviation with 35% swell, (c) Under polluted grid voltage, (d) Grid voltage under 30^{o}phase jump, (e): Grid voltage under +5 Hz frequency jump, (f): Grid voltage under 20% dc offset. The experimental frequency response of these three PLLs are also analysed for validating the simulation results under same considered grid abnormal conditions. The comparative analysis of the five PLLs is also performed considering six test cases of non-ideal grid conditions viz. (a): Grid voltage change of 30% sag, (b): Grid voltage change of 35% swell, (c) Grid voltage under polluted environment, (d): Grid voltage under 30^{o}phase jump, (e): Grid voltage under +5 frequency jump, (f): Grid voltage under 20% dc offset. Under 30% voltage sag H-LMS-SOGI PLL gives a lower overshoot and fastest settling time though LMS PLL gives the lowest overshoot but performs sluggishly. Under 35% Grid voltage swell H-LMS-SOGI PLL gives the highest overshoot than the other four PLLs but the fastest settling time period. With 30^{o} phase shift, H-LMS-SOGI PLL gives the least overshoot with moderate settling time of five cycles. The proposed H-LMS-SOGI PLL also shows least overshoot and fastest dynamic response under polluted grid voltage and +5Hz step frequency change. Moreover, the novel H-LMS-SOGI PLL gives satisfactory response under 20%dc offset. Further, the designed H-LMS-SOGI technique is validated for inverter control in a single-phase grid connected system. Hence it can be concluded that the novel H-LMS-SOGI PLL gives satisfactory dynamic response under all the adverse grid conditions considered and the technique can also be used for load compensation satisfactorily.

Chapter 7 discusses the mathematical model of three phase DFIG WEC with LMF-PLL has been discussed. THE modelling of RSC and GSC has been discussed in this chapter. A new LMF PLL's mathematical modelling has also been done. This LMF - PLL is used for rotor angle calculation, the dynamic performance of DFIG has been studied under both (a) variable wind speed and (b) constant wind speed. Under variable wind speed study, the three modes of speed operation are observed in DFIG dynamic

performance. The simulation and experimental results using Matlab SIMULINK environment and experimental results using OPAL RT lab setup and it is found that the results are validating each other. Under constant wind speed the dynamic behavior of DFIG system is studied under various grid abnormalities like (a) 30% voltage sag (b) 35% voltage swell (c) polluted grid voltage (d) 30^{o} phase shift (e) +5 Hz frequency change and (f) 20% DC-offset when the disturbance has been injected for a duration of 0.35s-0.65s. the performance is found to be satisfactory under these grid abnormalities. Moreover, the dynamic performance of the LMF-PLL is also tested under grid abnormalities and the performance is found satisfactory.

8.2 Future Scope

Synchronization Techniques for Control of Power Electronics Converters shows highly promising future research scope, particularly in light of the integration of renewable energy, smart grids, and systems dominated by power electronics. Future work in this area needs to address:

- Switch from grid-following converters based on PLL to grid-forming converters.
- Focus on developing Neural-network-based PLL, artificial intelligence (AI) assisted PLL and its tuning for Grid-connected PV, wind, EV charging system.
- For sturdy PLL performance in the face of grid faults (LVRT/HVRT), frequency variations, DC offset, and pollution or combination of these may be studied.
- Synchronization techniques for offshore wind farms, remote microgrids, virtual impedance-assisted synchronization, and impedance-based modelling of synchronization loops need to be investigated.
- There is a need to focus on effective FPGA/DSP-based real-time implementation techniques to develop event-triggered synchronization so that hardware and synchronization algorithms are co-designed, and ultra-fast synchronization for high-frequency converters can be tested.
- Synchronization techniques in microgrids with hybrid AC/DC need to be studied in detail where Cross-domain synchronization (electrical +

communication time), interaction with energy storage and EVs will play an important role.

- More focus on studying PLL behavior during asymmetrical faults, cyber-resilient synchronization and recovery dynamics following islanding incidents.

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APPENDIX A

Parameters for MSRF-PLL:

Input voltage supply, v_s=235V, fundamental frequency =50Hz, Kp =0.7, Ki = 3

Parameters for FO-LP MSRF-PLL:

Input voltage supply, v_s=235V, fundamental frequency = 50Hz, ω_{cf} = 2*π*36.72, Kp= 0.7, Ki = 0.025, a=1.1

Parameters for FO-LPFO-PI MSRF-PLL:

Input voltage supply, v_s=235V, fundamental frequency = 50Hz, ω_{cf} = 2*π*36.72, Kp= 0.025, Ki = 0.000025, a=1.1, b= 0.1

APPENDIX B

a. H-LMS-SOGI PLL
   v_s=325 V,f=50Hz, K_p=0.5, K_i=21.5, k=1.414, μ =0.005
b. For CLMS PLL
   v_s=325 V, f=50Hz, K_p=0.15, K_i=12, μ =0.05
c. For CSOGI PLL
   v_s=325 V, f=50Hz, K_p=0.4, K_i=10, k=1.8

Publications

List of publications in SCI/SCIE journals (Published)

1. Oinam Lotika Devi and A. Singh, “Performance analysis of fractional-order modified SRF PLL under grid abnormalities,” International Journal of Circuit Theory and Applications, vol. 53, no. 3, pp. 1491–1511, Jul. 2024, doi: 10.1002/cta.4161
2. Oinam Lotika Devi & A. Singh. (2025). Design of hybrid LMS-SOGI-based phase-locked loop tested under adverse grid conditions. Electrical Engineering. 1-18. 10.1007/s00202-025-03200-w

List of Publications in National and International Conferences

1. Oinam Lotika Devi and A. Singh, "Design Approach and Performance Analysis of Type I, Type II, and Type III PLL," 2023 7th International Conference on Computer Applications in Electrical Engineering-Recent Advances (CERA), Roorkee, India, 2023, pp. 1-6, doi: 10.1109/CERA59325.2023.10455725
2. Oinam Lotika Devi and A. Singh, "Modelling and Performance Analysis of DFIG Integrated with LMF-PLL under Grid Abnormalities," 2025 International Conference on Power Electronics Converters for Transportation and Energy Applications (PECTEA), Jatni, India, 2025, pp. 1-6, doi: 10.1109/PECTEA61788.2025.11076272