# ANALYSIS AND DESIGN OF A ZERO VOLTAGE TRANSITION DC-DC BOOST CONVERTER FOR PHOTOVOLTAIC (PV) ENERGY SYSTEM

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# ANALYSIS AND DESIGN OF A ZERO VOLTAGE TRANSITION DC-DC BOOST CONVERTER FOR PHOTOVOLTAIC (PV) ENERGY SYSTEM

A DISSERTATION
SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
CONTROL & INSTRUMENTATION


Submitted by:

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# CHAPTER-1

# INTRODUCTION

## 1.1 GENERAL

Energy is a vital component for human economic development and growth. With the increase in population, people's require for energy is also growing. Fossil energy holds are draining and won't have the capacity to address the issues of social advancement in the future. Additionally, broad utilization of non-renewable power sources has harmed our living condition. Therefore, the world has turned its regard for sustainable power sources. Among them, sun based energy(Solar Energy) has pulled in individuals' consideration since it has high calibre of Energy, is safe and reliable, and does not bring about contaminating outflows.

Besides, sun energy can nearly be discovered all around, and isn't limited to particular land territories. Because of their diminishing expenses and adaptable arrangements, photovoltaic frameworks will without a doubt turn into a promising environmentally friendly power energy innovation to accomplish economic advancement. Universal patterns unmistakably show an expanding job of renewable energy sources in covering current and future interest on electric energy. Since the year 2004, Poland has been an individual from the European Union. One of the principle commitments of the EU individuals is to diminish their effect on the common habitat by expanding RES share in the energy blend. Clean energy framework depends on residential non-renewable energy sources, especially hard and earthy colored coal, which empower Poland to produce over 83% of its electric energy. Explicitness of hard and earthy colored coal filled power plants inclined them to be enormous base load power plants which have a constrained capacity to quickly slope yield or decrease power age.

Therefore, the world has turned its regard for sustainable power sources. Among them, sun based energy(Solar Energy) has pulled in individuals' consideration since it is having high caliber of Energy, is reliable & safe, and doesn’t bring about contaminating outflows. Besides, sun energy can nearly be discovered all around, and isn't limited to particular land territories

Because of their diminishing expenses and adaptable arrangements, photovoltaic frameworks will without a doubt turn into a promising environmentally friendly power energy innovation to accomplish economic advancement because of the significant situation of industrialized fuel that comprise gas-oil & others, the improvement of non conventional source of energy is constantly improving. that is why non conventional source has turn into more essential these days.

Fundamental boost converter topography is most mainstream topology utilized in power factor correction circuits. The productivity and execution of the boost converter relies upon the switching recurrence influencing the switching misfortune. This paper presents a delicate switching support converter that used to convert photovoltaic boards yield level. The converter is reasonable for variable boosting component and high effectiveness applications, because of the delicate switching cell adjusted to the converter. So as to confirm its viability, trial verification is applied on a 120-watt converter. The DSP based PI controller used to produce 50kHz signs. The outcomes from the converter working with hard-switching and delicate switching are looked at. Hypothetical examination, operation standard and geography subtleties are likewise introduced and considered. The strategy can be effectively embraced by savvy lattice applications like microgrids and where exact and cleverly overseeing power flexibly is required.

## 1.2 LITERATURE REVIEW

## 1.3 OBJECTIVES

The objective of this thesis is to learn & examine function of converter & design the converter. The objectives of the thesis are as follows

To design converters that has

(a) compact switching losses

(b) Less EMI

(c) compact conduction losses

1. Traditional converters work with a sinusoidal current through the power switches, which brings about high pinnacle and rms currents for the power transistors and high voltage weights on the rectifier diodes.
2. When the line voltage or burden current shifts over a wide range, Semi Resonant Converters are adjusted with a wide switching recurrence extend, making the circuit structure hard to enhance.
3. As a tradeoff between the PWM and resonant methods, different delicate switching PWM converter strategies proposed to target joining alluring highlights of both the conventional PWM and Semi Resonant procedures without a critical increment in the flowing energy.

# CHAPTER-2

# SWITCHING TECHNIQUES

Hard switching is use for simple switch, motor drive inverter, and switched-mode power supply application. In compare, soft switching use an LC resonant circuit to turn on and trun off a apparatus at zero current or voltage.Soft switching means there is no loss linked with switching. It can occur either during turn on or off or during both.

## 2.1 PHOTOVOLTIC ENERGY SYSTEM USING BOOST CONVERTER

The concerns for atmosphere due the always escalating use of fossil fuel and hasty depletion of this resource have lead to the growth of different source of energy for instance solar energy. Propose that how to boost the effectiveness of a solar PV energy system via the advancement in conventional DC to DC Boost converter.

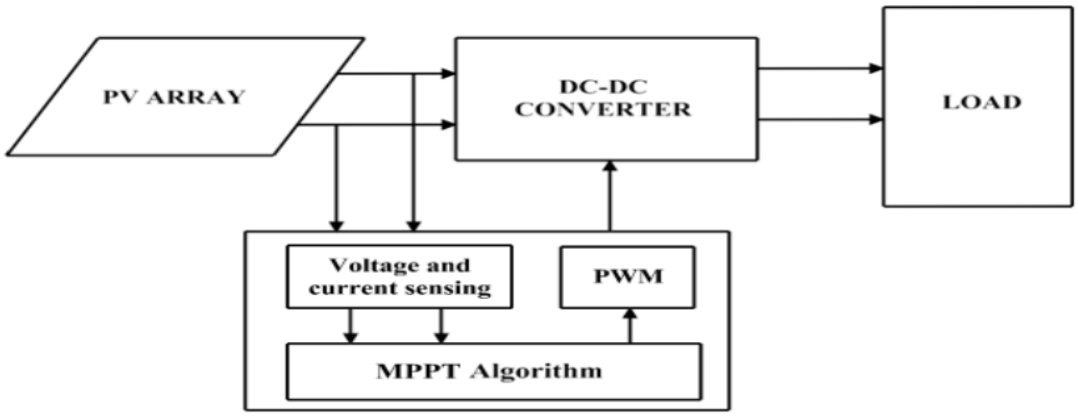


Fig: 2.1: Figure of DC-DC converter Photovoltaic system

Above Figure illustration a diagram presentation to utilize of a converter for Photovoltic system. When Switching MOSFETs establish then circuit is prohibited by a MPPT calculation which track that working purpose of the PV exhibit that meet the DC load line.

## 2.2 POWER LOSSES IN CONVERTERS (HARD-SWITCHING)

Hard-Switching has various notable downsides, the biggest of which is the presentation of switching losses. Power converters utilizing Hard-Switching (once more, basically every one of them), have to adjust the longing for higher switching frequencies with the requirement for worthy system losses to meet the ideal system efficiencies.Practically speaking this implies system requiring high efficiencies are intended to switch gradually to pick up effectiveness.

The proficiency picks up from decreasing the total measure of switching cycles (and henceforth aggregate switching losses) of every transistor in the transformation procedure. The downside of this methodology is that originators must expand the size of different segments in the system required to hold the power for a more drawn out timespan between the transistor's more extended switching cycles.

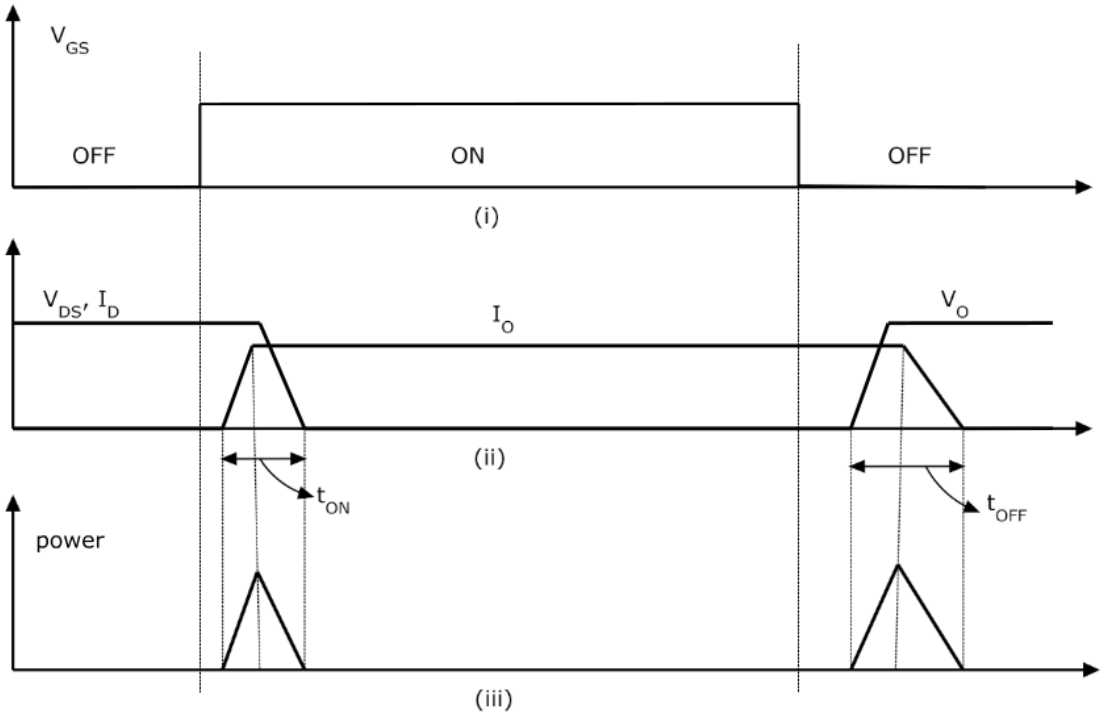


Fig 2.2: hard switching converters losses

There is another disadvantage to decreasing a transistor's switching frequency so as to pick up proficiency. By more slow switching frequencies produce more harmonic distortion & yield swell. Twists and wave for the most part should be separated to make the power usable. power designers commonly take care of this issue by including bigger yield channels - which again includes cost, size and weight.

The equation for switching losses for first cycle can be written as

$$P_{sw} = V_s I_s F_s \left[\frac{T_{on} T_{off}}{2}\right] \qquad (2.1)$$

By the above given situation of switching losses for each semiconductor gadget contrast straightly through switching frequency & delay times. In this manner like as hard switching converters cann't be use as high recurrence switching application. Regardless of whether utilization of detached snubbers over the switch decline voltage focuses onstresses, the adequacy cann't be improved brought about by high switching losses.

From the switching losses equation , it can be study that the switching losses can be reduced in two methods

1. By reducing the delay times during turn ON/OFF, by using faster and more competent switches in converter.
2. By making the voltage across or current through the switch is zero before turning it ON or OFF, the concept of soft switching converters.

## 2.3 SOFT SWITCHING TECHNIQUES

There are two basic ways to attain soft switching, zero current switching and zero voltage switching ,based on the constraint that is made zero, either the voltage or current through the device.

### 2.3.1 ZERO CURRENT SWITCHING

A switch operating by ZCS has a blocking diode and an inductor in series with it. The switch turns ON under ZCS as the rate of increase of current later than voltage become zero is controlled by the inductor. Because the inductor doesn't allow rapid change in current, it rises linearly from zero.

When a negative voltage is made to appear across the amalgamation of inductor and switch with a resonant circuit, the current flowing throughout the switch is as expected reduced to zero which outcome in the turn OFF of the switch below zero current switching.

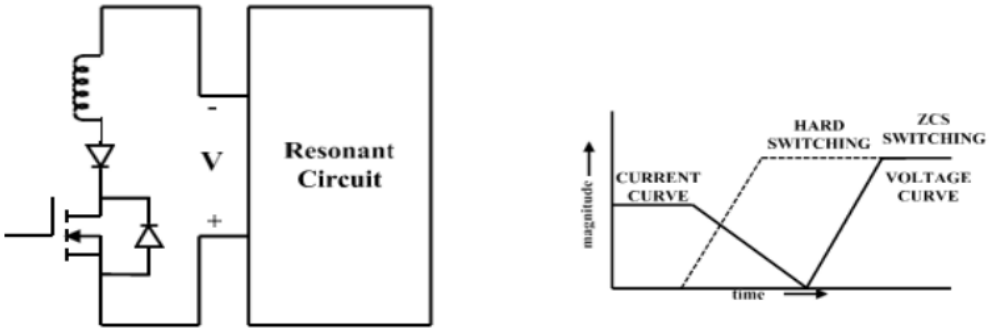


Figure 2.3: (a) ZCS turn OFF using negative voltage

(b) Switching waveforms of hard switching and ZCS during turn OFF

### 2.3.2 ZERO VOLTAGE SWITCHIING

A switch working with ZVS has a capacitor & an anti-parallel diode across it. During turn OFF as the current reduces to zero, the rate of voltage increases that takes place across the switch is controlled by the capacitor. As the capacitor does not allow rapid change in voltage, it increases linearly from zero.

The turn OFF characteristics of the switch is controlled with a capacitor allied across it. This capacitor reduce the voltage increase rate as current flow reduces to zero.

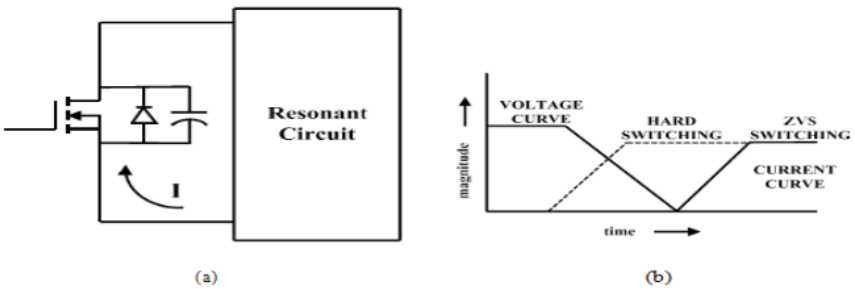


Figure 2.4: (a) ZVS turn ON using negative current

(a) Switching waveforms of hard switching and soft switching

## 2.4 ZERO VOLTAGE TRANSITION CONVERTERS

The ZVT converters achieve zero voltage switching through both turn-ON & turn-OFF transitions of the primary and boost switch.

The zero voltage transition in zero voltage switching converters is accomplished by turning OFF the switch which has capacitor and a diode connected in parallel with it. while the flow of current by the switch falls to zero, the capacitor maintains zero voltage across the switch. Where as in zero voltage transition, at the same time as the switch turns OFF, the current in the switch is transfer to the capacitor associated in parallel to it.

The turn ON transition in zero voltage switching is accomplished when discharging the capacitor connected in parallel by making use of the energy stored in a magnetic circuit Component like a transformer winding or an inductor coil. The switch is turned ON following the parallel diode enter into the state of conduction. This ensure a zero voltage across the switch through transition.There are various zero voltage switching techniques. Each one differs from other in the techniques used to control and adjust to manage regulation and as well in the mechanism of storing energy to get zero voltage turn ON.

# CHAPTER-3

# ZERO VOLTAGE TRANSITION DC-DC BOOST CONVERTER

DC-DC convertor is associate electric circuit whose main application is to transform a dc voltage from one level to a different level. it's almost like a transformer in AC source, it will ready to step the voltage level up or down. The variable dc voltage level may be regulated by controlling the duty ratio (on-off time of a switch) of the converter.

## 3.1 CONVERTERS

There are numerous forms of dc-dc converters[19] that may be used to transform the amount of the voltage as per accessibility|the provision} availability and load demand. a number of them are mentioned below

1. Buck converter
2. Boost converter
3. Buck-Boost converter

Each of them is explained below.

### 3.1.1 Buck converter:

The practicality of a buck converter is to cut back the voltage level. The circuit diagram of the buck converter is manifested in figure 3.1.

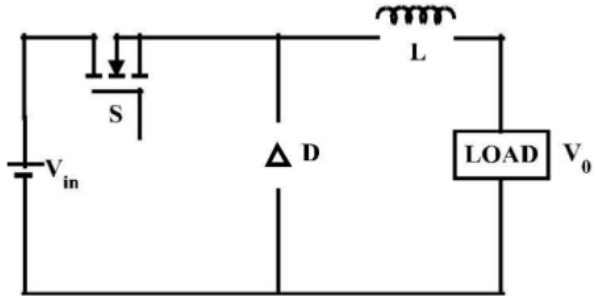


Fig. 3.1 circuit diagram of buck converter

When the switching component is in state of conduction the voltage showing across the load is Vin and also the current is equipped from source to load. Once the switch is off the load voltage is zero and also the direction of current remains the same. Because the power flows from source side to load side, the load side voltage remains less than the source side voltage. The output voltage is set as a perform of source voltage using the duty ratio of the gate pulse given to the switch. it's the product of the duty ratio and also the input voltage.

### 3.1.2 Boost converter:

The practicality of boost converter is to extend the voltage level. The circuit configuration of the boost converter is manifested in figure 3.2.

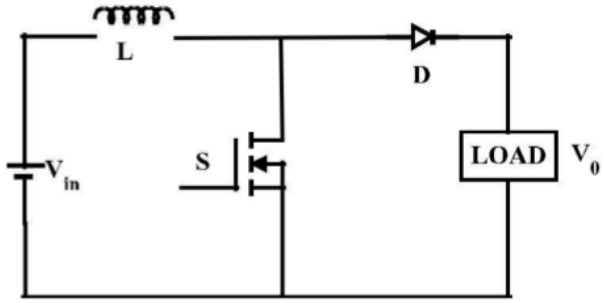


Fig. 3.2 circuit diagram of boost converter

The current carried by the inductance starts rising and it stores energy throughout ON time of the switching component. The circuit is said to be in charging state. throughout OFF condition, the reserve energy of the inductance starts dissipating into the load in conjunction with the supply. The output voltage level exceeds that of the input voltage and depends on the inductance time constant. The load side voltage is that the ratio of source side voltage and also the duty ratio of the switching device.

### 3.1.3 Buck-Boost converter:

The practicality of a buck-boost converter is to set the amount of load side voltage to either bigger than or less than that of the source side voltage. The circuit configuration of the buck-boost converter is manifested in figure 3.3.

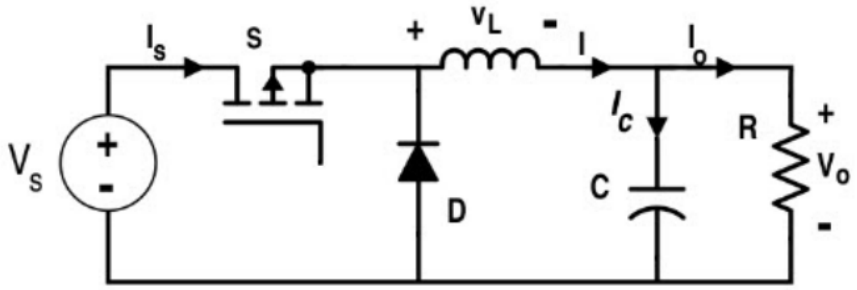


Fig. 3.3 circuit diagram of buck-boost converter

When the switches are within the state of conduction, the current carried by the inductance starts rising and it stores energy. The circuit is said to be in charging state. whereas the switches are within the OFF state, this stored energy of the inductance is dissipated to the load through the diodes. The output voltage may be varied supported the On-time of the switches.

The buck-boost converter acts as each buck and boost converters depending on the duty cycle of the switches. For the duty ratio but five hundredth it acts as a buck converter and for the duty ratio exceeds than five hundredth it acts as boost converter. As the voltage may be stepped each up and down, we have a tendency to use buck-boost converter for our convenience in our work.

## 3.2 CIRCUIT DESCRIPTIONAND ITS NOVELTY

The diagram of the ZV transition DC-DC boost converter is shown in below Figure3.1.

It is a usual boost converter with a diode $D_1$, input boost inductor $L_{in}$, main switch $S_1$ and an output capacitor $C_0$ across a load $R_{load.}$ In addition to the boost circuit, it also constitute of an additional circuit that resonates, consisting of an inductor $L_r$, a capacitor $C_r$, diodes $D_2$-$D_5$ and a capacitor $C_b$ to feed the resonant energy to the load.The capacitance Cs given away across the main switch $S_1$ is its parasitic capacitance.

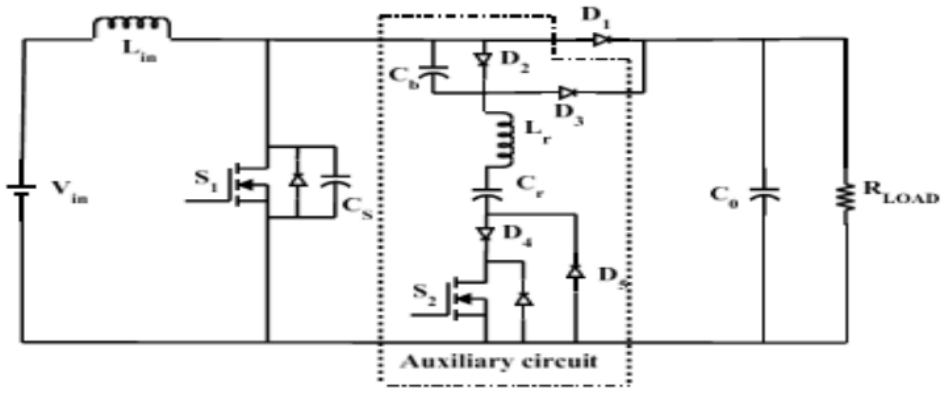


Figure 3.4: Schematic diagram of the ZVT dc-dc boost converter

The basic theory of Zero Voltage Transitions is to facilitate the auxiliary circuit carry a current higher than that of the input supply current, for a little portion of the complete switching phase in order to accomplish soft switching of the switching element present in the converter. Therefore Zero Voltage Transition converters have higher ohmic losses than that of those converters that work under hard-switching. other than the efficiency of the converters that run under soft switching is inflated distinct the hard switching converters on account of diminish switching losses.

## 3.3 CIRCUIT FUNCTION

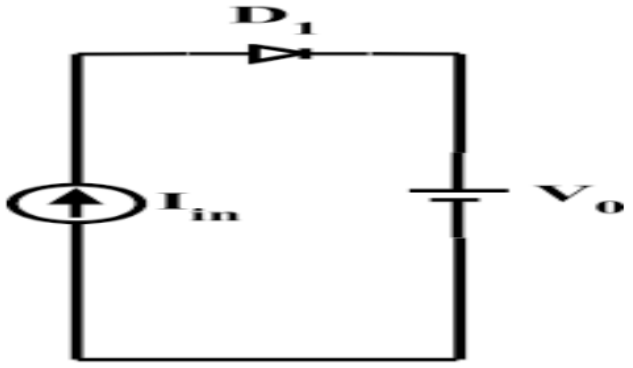


Fig: 3.4(a) converter circuit [$t<t_0$]

The given figure explain total switching cycle those are separated in 7 parts every of these belongings is explain with the given circuit for time interval. At first the diode $D_1$ store the output current and that act as simple PWM boost converter.[20] A circuit has shown this situation in fig 3.2.

**[$t_0$-$t_1$] Mode 1:**

When time t0 switch S2 is turned ON with ZVT because of the presence of supplementary resonant inductor sequentially related to it. The current step by step begins to redirect through diode D1 and the piece of circuit can be supplement the core circuit, those at last begin resonate. that inductor hinder the switched OFF current percentage entirely through D1 in order to switched OFF underneath ZCS by means of finish of this recess.[21] At that point auxiliary current moving via boost inductor equivalent the initial current which is given at the time of input. The same circuit of this span is show in diagram 3.3.

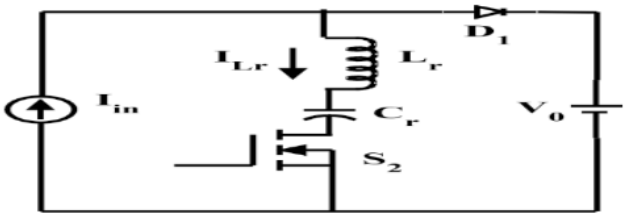


Fig 3.5 : CircuitInterval[$t_0$-$t_1$]

**[$t_1$-$t_2$] Mode 2:**

The current in auxiliary circuit continues rising throughout the entire intervals. In any case, the information current provided is thought to be consistent because of tremendous inductance which doesn't permit fast change in current. in this way parasitic capacitance(Cs) of key switch(S1) begin releasing into supplementary circuit in organize bring expanded part supplementary current. Before finish this period capacitance releases totally. Relating circuit of that span is showed in diagram 3.4.

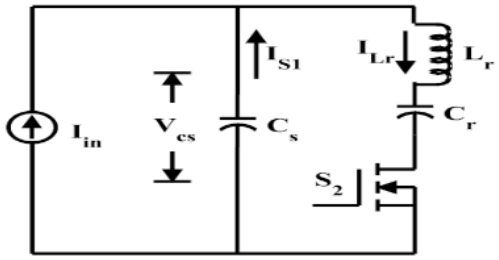


Fig: 3.6 : CircuitInterval[$t_1$-$t_2$]

**[$t_2$-$t_3$] Mode 3:**

After the instant $t_2$ the diode internally present in the main switch associated anti parallel to it starts conducting, which cause the voltage blocked by the main switch $S_1$ to be zero. This is the Zero Voltage interval during which the switch $S_1$ must be supplied with the trigger. [22] By the end of this interval the current carried by the auxiliary circuit equals the input supply current and the main switch is in a condition of about to start conduction. The equivalent circuit of the converter for this mode is manifest in fig:3.5.

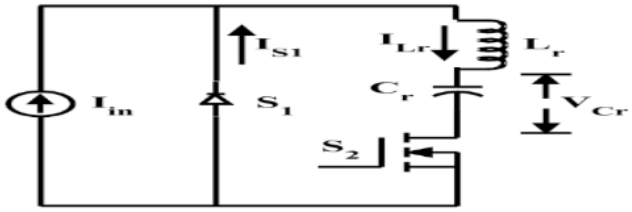


Fig: 3.7: CircuitInterval[$t_2$-$t_3$]

**[$t_3$-$t_4$] Mode 4:**

Supply current of input is decreased by supplementary current & the remainder of the info current later than supply with the supplementary current beginning flow by the switch(S1). At the Finish of that Intervals the progression of current in the supplementary circuit become 0. The comparing circuit of converter of that mode is illustrate in diagram 3.6 .

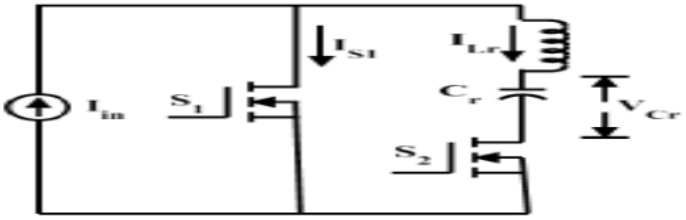


Fig: 3.8: CircuitInterval[$t_3$-$t_4$]

**[$t_4$-$t_5$]Mode 5 :**

The comparable circuit of this span is showed in diagram 3.7.

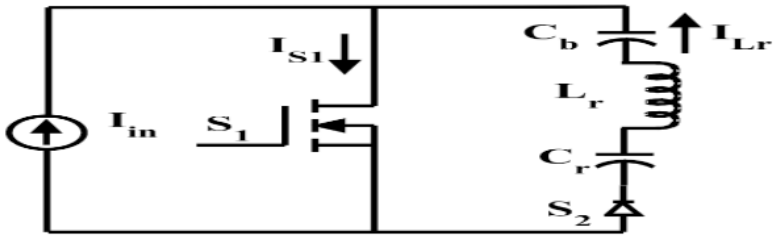


Fig: 3.9 : CircuitInterval[$t_4$-$t_5$]

**[$t_5$-$t_6$] Mode 6:**

As this mode beginning at moment t5, the supplementary current becomes 0 .The contrasting circuit of converter in span is appear in fig: 3.8 .

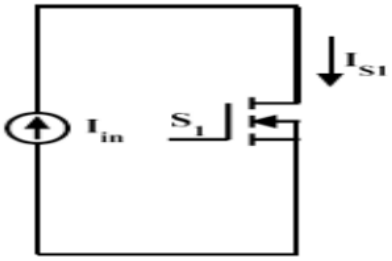


Fig 3.10: CircuitInterval[$t_5$-$t_6$]

**[$t_6$-$t_7$] Mode 7:**

The relating circuit of this converter on the side of this interval is showed up in diagram 3.9 .

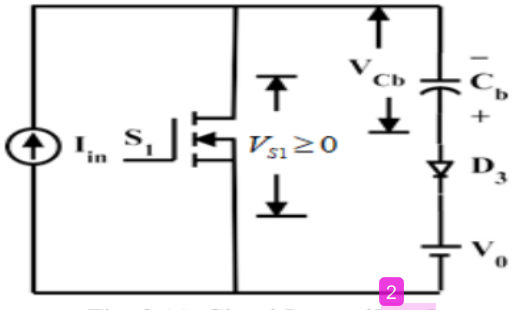


Fig: 3.11: CircuitInterval[$t_6$-$t_7$]

## 3.4 NOTIONAL WAVEFORMS

Diagram 3.10 show hypothetical waveforms for activity of converter demonstrating every stretch in whole switching cycle. That varieties of thunderous circuit current & capacitor sequencly, voltages(V) & current(I) (fundamental and suplimentary),feed forward capacitor voltage in every span is indicated plainly.

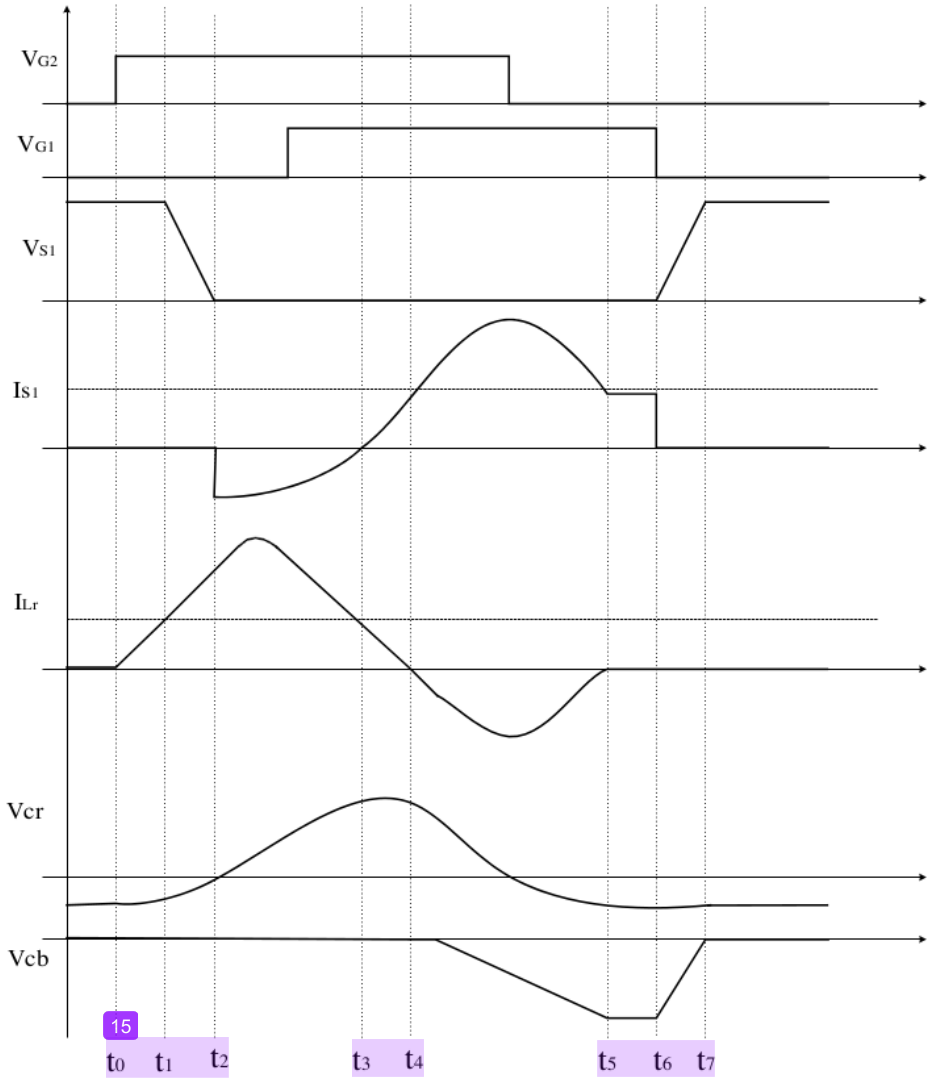


Fig: 3.12 : Notional Waveform

For extra specifying in ZVS turnON S1, total waveforms is collected on ordinary time rotate & showed up. diagram 3.11 show zero(0) voltage range throughout that essential switch must be switchedON. The current waveforms passed on resonant inductor , voltage(v) blocked via resonant capacitor(c),voltage obstructed with FFC(feed forward capacitor) & t major switch voltage is secured with basic cognizance.

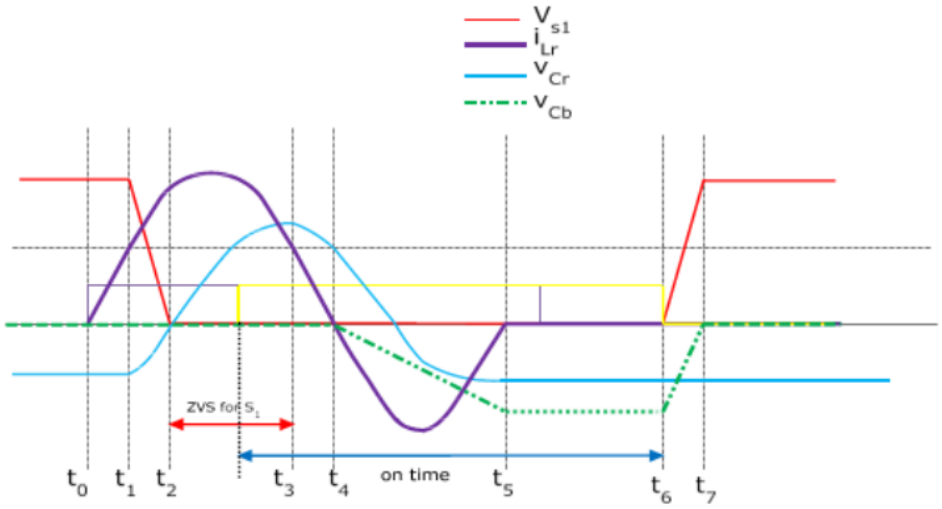


Fig: 3.13 : ZVSInterval of Switch($S_1$)

## 3.5 CONVERTER DESIGN

### Design objectives:

This manual gives tips to structuring the circuits of DC/DC converters. The most effective method to structure DC/DC converter circuits that fulfill the necessary particulars under an assortment of imperatives is depicted by utilizing solid models however much as could be expected.

- To examine the activity of buck converter.
- To examine the activity of step down PWM methods.

- Recreation buck converter, to control circuit & force circuit by utilizing PSpice, MATLAB software's ,Protel DXP 2004.
- Reenactment buck converter recurrence reaction utilizing software of PSpice programming.
- Propose buck converter circuit(power stage).
- Propose controller & compensator circuit.
- Testing & adjustment of finished buckConverter to affirm genuine reaction with hypothetical forecasts.
- Perception of waveforms as of diverse experiment purpose of the converter.

The design particular depends on low force application. Circuit is mimicked via utilizing Spice programming to acquire ideal yield voltage to providing fix input esteem.

## Design specifications :

The particulars for structure of converter is given in diagram(3.1) .Details incorporate converter yield input voltage,powerRating, & voltage, reasonable wave/rate in current & voltage and so on.

| Sl.No. | Parameter | Specification | Value |
|---|---|---|---|
| 1 | Output voltage | $V_{0ut}$ | 400V |
| 2 | Output power | $P_{0ut}$ | 250W |
| 3 | Input voltage | $V_{in}$ | 90-265V |
| 4 | Switching frequency | $F_{sw}$ | 120kHz |
| 5 | Input current peak ripple | $\Delta I_{rpp}$ | 20% |
| 6 | Output voltage ripple | $V_{rp}$ | 1% |

Table 3.1 Converter specifications

### 3.5.1 Design of Power Circuit

Power circuit comprises of input inductor, boost diode, principle switch & yield capacitor. Estimation every circuit component esteems is indicated plainly.

**Input inductor $L_{in}$ :**

The geometric evaluation of information inductor(Lin) , have to chosen primary since this worth set apex input current that the converter switch need to resist & consequently that current is significant to choose rating of other force circuit segments. Most extreme current not including ripple is

$$I_{in-pk} = \frac{\frac{P_{out}\sqrt{2}}{n}}{V_{in}} = \frac{\frac{250\sqrt{2}}{0.95}}{90} = 4.135A \qquad (3.1)$$

The peak-peak ripple (maximum) current is

$$\Delta I_{rpp} = I_{rp\_max}\Delta I = 4.135 * 20\% = 0.827A \qquad (3.2)$$

so the peak input(maximum)current with ripple

$$I_{rpk\_max} = I_{rp\_max} + \frac{\Delta I_{rpp}}{2} = 4.135 + \frac{0.827}{2} = 4.55A \qquad (3.3)$$

The duty ratio of converter (maximum current occurs)

$$D_{pk} = 1 - \sqrt{2}\frac{V_{in-min}}{V_o} = 1 - \frac{\sqrt{2} * 90}{400} = 0.682 \qquad (3.4)$$

The input inductor value is calculate as given below

$$I_{in} = \frac{\sqrt{2}V_{in-min}D_{pk}}{\Delta I_{rpp}F_{sw}} = \frac{\sqrt{2} * 90 * 0.682}{0.827 * 100kHZ} \qquad (3.5)$$

## Output Capacitor :

The output capacitor goes about as a vitality stockpiling component. The peak charge current of the capacitor is

$$I_{Chg-pk} = \frac{P_{out}}{V_{out}} = \frac{250}{400} = 0.625a \qquad (3.6)$$

The ripple voltage across$C_0$ is give by

$$V_{chg\_pk} = \frac{I_{chg-pk}}{2\pi F_r r_{chg\_pk}} = \frac{0.625}{2\pi * 120Hz(0.01 * 400)} = 207\mu F \qquad (3.7)$$

Where;

$$V_{chg\_pk} = \frac{I_{chg\_pk}}{2\pi F_r C_o}$$

## Boost diode:

The most extreme voltage over boost diode may be output voltage 400=V0 that shows up over diode as primary switch stays at directing circumstance. The pinnacle current,courses via diode is top with wave of current moving all the way via boost inductor given by

$I_{rpk\_max} = 4.55A$ That is normal current coursing via diode is

$$I_{D1\_avg} = \frac{P_o}{V_o} = \frac{250}{400} = 0.625A \qquad (3.8)$$

Peak current rating of boost support switch relies on supplementary circuit. Subsequently that is planned later than the supplementary circuit.

### 3.5.2 Design Of The Main Switch And Auxillary Circuit

**Base Values :**

The base voltage Vb is defined as:

$$V_b = V_o = 400V \tag{3.9}$$

The base current Ib is defined as:

$$I_b = I_{pk-max} - \frac{\Delta I_{rpp}}{2} = 4.135 - \frac{0.827}{2} = 3.7221 \tag{3.10}$$

So the base impedance is define as

$$Z_{rb} = \frac{V_b}{I_b} = \frac{400}{3.722} = 107.48\Omega \tag{3.11}$$

The base time is defined as the natural resonant cycle of the auxiliary circuit and is given as:

$$T_r = 2\pi\sqrt{L_r}\sqrt{C_r} \tag{3.12}$$

The most horrible condition is the place the ZVS span will be littlest which happens when the info help current is at its greatest pinnacle. At this estimation of pinnacle current the impedance Zrb will be one.

**Resonant Inductor $L_r$:**

Lr can be calculated as follows :

$$L_r = \frac{3t_{rr}V_{s2\_pk}}{I_B} = 5.8\mu H \tag{3.13}$$

### Resonant Capacitor $C_r$ :

The value of resonant capacitor $C_r$ is chosen from the graph of ZVS interval vs. resonant impedance $Z_r$. We have to opt $C_r$ that will give enough ZVS turn-on interval as well as fine turn-off. For correct design we choose the curve K=3 and $Z_r$=0.21 pu [1] and value of $C_r$ can be dogged as follows

$$Z_r = \sqrt{\frac{L_r}{C_r}} => C_r = \frac{L_r}{Z_r^2}$$

$$Z_R = \left(Z_{r\_pu} Z_{rb}\right) = (0.21 \times 107.469) = 22.568\Omega \quad (3.14)$$

## Auxiliary capacitor ($C_b$):

ZVS at turn-off is provided by capacitor $C_b$. the selection of this capacitor is simple and is the same as follows

$$K = \frac{C_r}{C_b} = 3$$

$$C_b = \frac{C_r}{V} = 3.66nf \quad (3.1)$$

## Rating of auxiliary switch:

From the values of K and $Z_r$ chosen it is found that the peak voltage blocked by auxiliary switch $V_{s2\_pk}$ is

$$V_{S2\_pk} = 0.64 * 400V = 256V \quad (3.16)$$

The peak current of the switch is

$$I_{s_2-pk} = 1.61pu * 3.722 = 5.99A \quad (3.17)$$

The rms current is found to be

$$I_{s2\_rms} = \left(I_{ss2\_rms}, pu\right) I_b \sqrt{T_r F_{sw}} = (0.53) 3.722 \sqrt{1.58\mu s \times 100KHz} = 0.786A \quad (3.18)$$

## Rating of the auxiliary circuit diodes:

The auxiliary circuit diodes contain a similar voltage rating equivalent to that of lift diode. The 2 arrangement diodes D2 and D4 will do a similar pinnacle current as auxiliary switch S2. The pinnacle current passed by diode D5 is additionally somewhat same as the abovementioned. The pinnacle current passed by diode D3 is the pinnacle current with swell Irpk_max that stream in the converter was seen as 4.55A. The normal current is seen as through diode D2.

$$I_{D2_{avg}} = \left(I_{D2_{avg}}, pu\right) I_b T_r F_{sw} = (0.21pu) 722A * 1.587\mu s * 100KHz = 0.12A \quad (3.19)$$

## Rating of the main switch:

Most extreme voltage that this switch must have the option to hold is the output voltage V0 with swell. The wave present in the output voltage can be found as

$$V_{chg\_pk} = 0.01 * 400 = 4V \quad (3.20)$$

Thus switch $S_1$ have to handle 404 volts

The peak current of main switch given by $2.27\ pu \times 3.722 = 8.448$ (3.21)

The maximum RMS current used for the switch is establish to be

$$I_{s1\_rms} = I_{pk\_max}\sqrt{\frac{1}{2} - \frac{4V_{in\_min}\sqrt{2}}{3\pi V_o}} = 3.722\sqrt{\frac{1}{2} - \frac{4*90*\sqrt{2}}{3\pi*400}} = 2.55A \quad (3.22)$$

The voltage over the capacitor Cb for K=3 and Zr=0.21 is - 0.87 pu. This implies the voltage obstructed by switch S1 during turn-off is 0.13 pu. accordingly voltage hindered by switch S1 is seen as be

$0.13pu \times 400 = 52V$

Therefore the turn-off losses are also significantly reduced.

## 3.6 SIMULATION VALUES OF THE CONVERTER

The converter circuit shown in fig-1 is simulated in MATLAB simulation environment by taking the element values showing in table 3.2.

| Sl. no. | Circuit component | Symbol | specification |
|---|---|---|---|
| 1 | Resonant inductor | $L_r$ | 7μH |
| 2 | Resonant capacitor | $C_r$ | 16Nf |
| 3 | Feed-forward capacitor | $C_b$ | 3.5Nf |
| 4 | Boost inductor | $L_{in}$ | 1060μH |
| 5 | Output capacitor | $C_0$ | 480μF |
| 6 | Input voltage | $V_{in}$ | 275V |
| 7 | Switching frequency | $F_{sw}$ | 100kHz |

Table 3.2 Component disclaimer for simulation

# CHAPTER-4

# MODELLING OF PHOTO VOLTAIC ARRAY

## 4.1 INTRODUCTION

Solar modules or panels are used for converting solar energy to electrical energy in a photovoltaic system. The fundamental element of a PV array is a PV cell.

### 4.1.1 PHOTOVOLTAIC CELL

This function analogous to basic P-N junction devices., When sunlight falls on the face of the PV cell, the photons are captivated by the atoms in the semiconductor material and electrons are released from the negative layer, [17] When PV cell is coupled through an external circuit to the load, the free electrons discover a path to get in touch with the positive layer. The current production process is shown in figure 4.1.

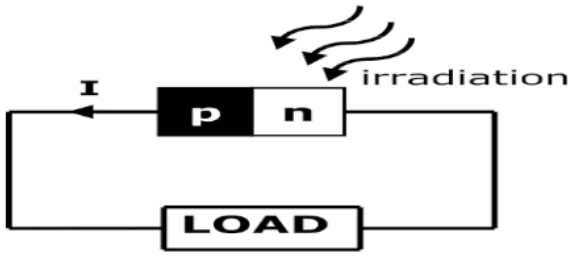


Fig 4.1 photocurrent generation

### Detailed construction and working of a PV Cell:

Various types of semiconductor materials are used for manufacturing PV cell using various processes. Now a days, the monocrystalline and polycrystalline are typically used. Si cells have a Si coating that is attached to terminals of other devices. To turn up a P-N junction one side of the sheet undergoes a process of accumulation of impurities, usually called doping . A very thin grid (metallic) is placed on the crest of the PV cell which faces the sun.

An electric current is originated when the light is incident on the face of the cell, charge carriers are produced, when the cell becomes a component of a loop or is associated to a load. As the energy of the incident photon becomes adequate to break the covalent bond charge carriers are produced due to detachment of the electrons of the semiconductor .No voltage is produced by the photons that have lesser energies than the energy gap of PV cell and are not of any use. Whereas Photons that have energy higher then the band gap can generate electricity, but the energy related with the band gap is only made use of. The residual energy will be degenerated in the form of heat [10].

### 4.1.2 PHOTOVOLTAIC MODULE

A very low voltage of around 0.5 volts is generated. So in order to achieve desired output a numeral of cells should be connected in series and parallel . In case of partial shading. diodes may be desired in order to evade reverse current in the array.

### 4.1.3 PHOTOVOLTAIC ARRAY

As the power generated by the module is not sufficient enough for operating any power appliances that's why various other arrangements are made in order to reach the demand. The PV array are connected in either series or parallel to meet the demand. They are connected in series if high voltage rating is required otherwise connected in parallel for high current rating..The connection are made according to requirements.[18]

## 4.2 MODELING OF PV SYSTEM

### 4.2.1 PV CELL MODELING

The solitary diode circuit of a single PV cell is shown in the figure 4.2. It includes a current source, a diode parallelly connected to the current source which represents the photocurrent, a series resistance $R_s$ and a parallel resistance $R_{sh}$.

An exact single diode model is depicted in the above figure. Equation 3.1 represents the current produced from the cell

$$I = I_{PV} - I_O \left[ exp \left\{ \frac{V+IR_S}{\alpha V_T} \right\} - 1 \right] - \left[ \frac{V+IR_S}{R_p} \right] \quad (4.1)$$

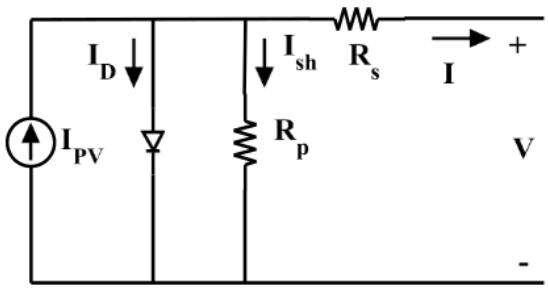


Fig: 4.2 Analytical circuit of a practical PV cell

Here

$I_0$ is the diode's reverse saturation current

$V_T$ is the diode's thermal voltage

$a$ is the ideality factor of the diode

The equation of a PV current affiliated of varying environmental conditions, the temperature and irradiance can be written as

$$I_{PV} = (I_{PV-STC} + K_I \Delta T) \frac{G}{G_{STC}} \quad (4.2)$$

Where

$I_{PV\_STC}$ is the photocurrent under Standard Test Conditions (STC)

$\Delta T = T - T_{STC}$ (in Kelvin) and $T_{STC}$=25°C

$G$ is the irradiance on the surface of the cell

$G_{STC}$ is the irradiance under STC (1000W/m²)

$K_I$ is the short circuit current coefficient (generally provided by the manufacturer)

Saturation current(I) of diode is given by

$$I_0 = I_{0-STC}\left(\frac{T_{STC}}{T}\right)^3 exp\left[\frac{qE_g}{ak}\left(\frac{1}{T_{STC}} - \frac{1}{T}\right)\right] \quad (4.3)$$

Where

$E_g$ is the energy gap of the semiconductor

$I_{0\_STC}$ is the nominal saturation current

The reverse saturation current equation can be further improved as a function of temperature as follows

$$I_o = \frac{I_{sc\_stc} - K_1\Delta T}{\exp\left[V_{oc\_stc} + K_V\Delta T\right]/\alpha V_T} \quad (4.4)$$

### 4.2.2 PV ARRAY MODELING

All the above conditions are suitable for a solitary PV cell. In any case, in a great establishment of a PV power station ,so as to remunerate the flexibly request hole PV modules are utilized in which arrangement and equal associated PV cells are utilized . Arrangement blend of the cells helps in expanding the voltage and the equal plan of the cells helps in raising the current of the whole module

$$I = I_{PV}N_P - I_O N_P\left[exp\left\{\frac{V + IR_S\frac{N_S}{N_P}}{\alpha V_T N_S}\right\} - \frac{V + IR_S\frac{N_S}{N_P}}{R_P\frac{N_S}{N_P}}\right] \quad (4.5)$$

The arrangement of modules in a series parallel structure is shown in figure 4.3.

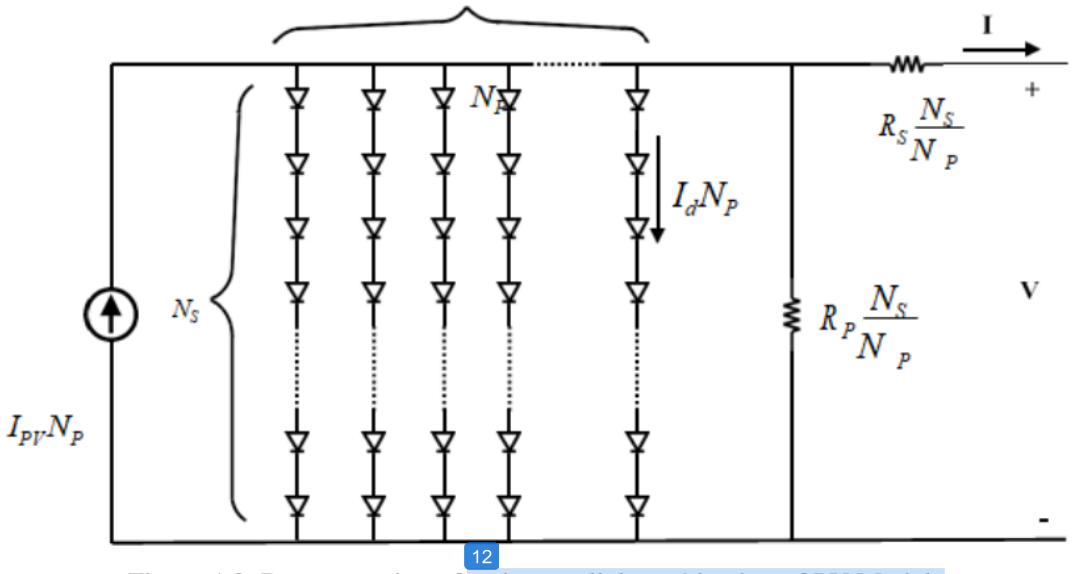


Figure 4.3: Demonstration of series parallel combination of PV Module

The standard qualities of a PV energy system is appeared in the figures beneath. The current voltage (I-V) qualities & the power Voltage (P-V) attributes are separate photovoltaic qualities. The standard bends of these attributes are appeared. The point P maximum in the I-V bend shows where greatest power can be created. It speaks to the voltage at the most extreme power point from the bend. This most extreme power point is followed from the P-V bend utilizing different following strategies

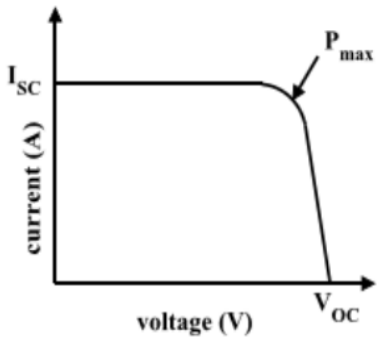


Figure 4.4: Typical I-V curve

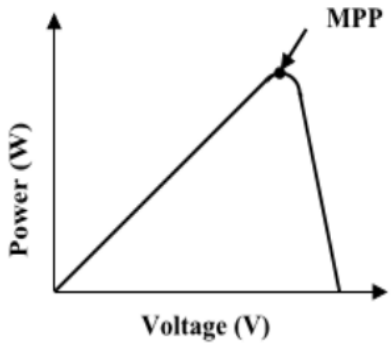


Figure 4.5: Typical P-V curve

The maximum power purpose of a PV cell is the peakpoint of the P-V bend. For various cells, this point will be diverse . Be that as it may, the maximum power point following framework recognize the MPP of the total framework , for example all the cells associated. As of late examination is continuing reenacting MPP tracking beacons for every cell.

## 4.3 SIMULATION OF PV ARRAY

The PV module model is simulated in MATLAB simulink using the above equations. The parameters designed for simulating the PV module are as shown in the table 4.1

| Serial No. | PARAMETER | SYMBOL | VALUE |
|---|---|---|---|
| 1. | Voltage at maximum power | $V_{max.p}$ | 26.29 V |
| 2. | Current at maximum power | $I_{max.p}$ | 7.59A |
| 3. | Open circuit voltage | $Vo._{c.}$ | 32.89 V |
| 4. | Maximum power | $P_{max.}$ | 200.139 W |
| 5. | Short circuit current | $I_{s.c.}$ | 8.19A |
| 6. | Temperature coefficient of I | $K._i$ | 0.0031 A/K |
| 7. | Temperature coefficient of V | $K._v$ | -0.1229 V/K |

Table 4.1 Parameters of the simulated PV module

At the point when a specific module is simulated, the open circuit voltage of the module is seen as around 30 volts. Be that as it may, this voltage is seen not as close by inside the information voltage scope of the thought about converter. This voltage can't be taken care of to the converter to confirm its activity in the PV condition. So 6 modules of same kind are associated in arrangement so the output voltage increments. At the point when 6 modules are arrangement associated, at that point the output voltage of the array is expanded to right around 180 volts. This voltage of 180 volts is inside the information scope of the considered Zero Voltage Transition DC-DC help converter which is 90-265 volts.

# CHAPTER-5

# MAXIMUM POWER POINT TRACKING

## 5.1 INTRODUCTION

Due to non linear qualities of voltage and current in PV board and so as to recover the effectiveness of the PV framework we need mppt calculation to find the working point to MPP of the trademark bend.[23] The PV boards, the converter and the MPP tracker are the main 3 significant instrument of the PV energy framework . The proficiency advancement of the converter and PV boards should be possible effectively as it relies on the innovation utilized and include packet of currency. So as to regain the proficiency in a economically ability way we use MPPT calculations [10].

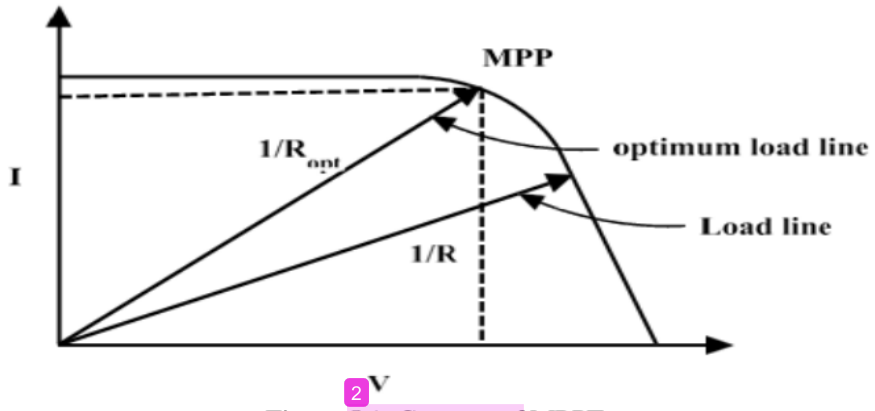


Figure 5.1: Concept of MPPT

Maximum power point (MPP) is an bias potential at which the solar cell outputs the maximum total power. It is a point present either on I-V or P-V characteristics curve of the PV panel. It helps in yielding the maximum power output. [27] In MPPT theorem by keeping constant the load and varying the duty cycle of load (which indirectly vary the load) help in yielding the maximum system output power from the PV energy system. By varying the slope of the load line and changing the operating point and setting up at the MPP, maximum power can be achieved from the PV array. The perception of maximum power point tracking is shown in figure 5.1

## 5.2 TYPES OF MPPT TECHNIQUES/ALGORITHMS

In earlier years, numerous calculations have been acquainted with trail maximum power point.[29] They change from each other in viewpoints like unpredictability, proficiency and cost. Some of them are

1. Neural networks
2. Perturb and observe
3. Fuzzy logic control
4. Incremental conductance
5. Fractional short circuit current
6. Maximum power point current and voltage computation
7. State based MPP tracking technique

From all the mentioned techniques, we use Perturb and observe algorithm for effortlessness..

## 5.3 PETURB AND OBSERVE

In this method we have a tendency to announce a perturbation within the operative voltage of the panel. Perturbation in voltage is often done by fluctuating value of duty-cycle of dc-dc convertor.[28]

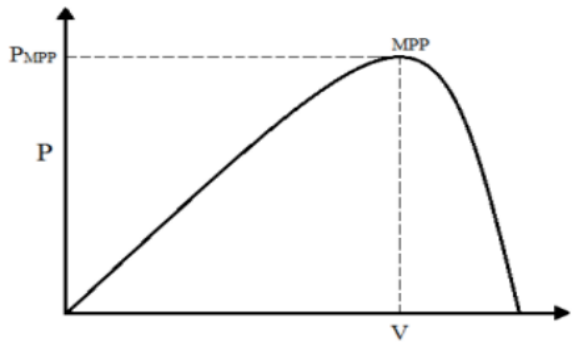


Fig. 5.2 P-V characteristics (basic idea of P&O algorithm)

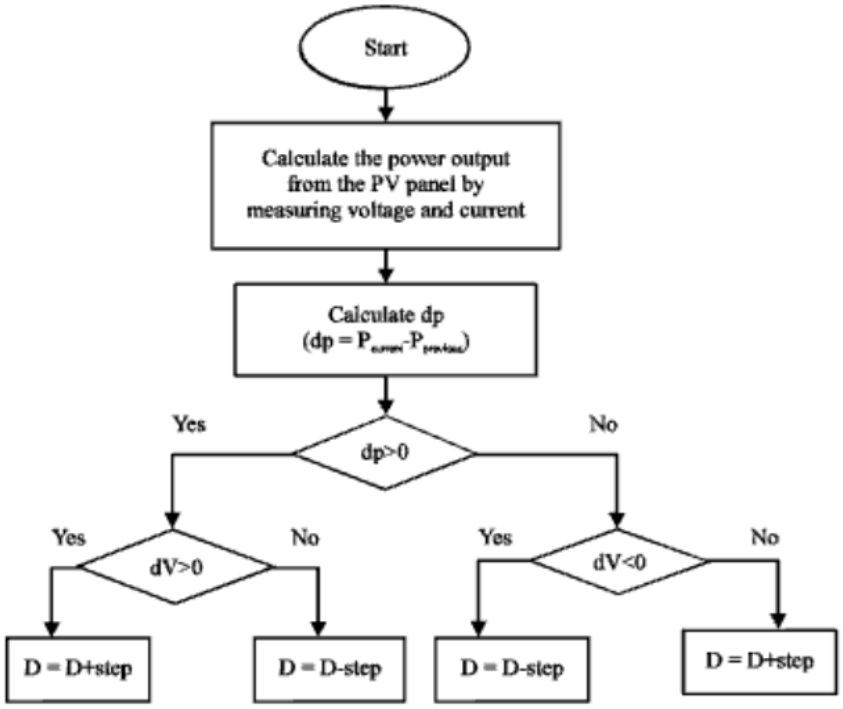


Fig.5.3 Flowchart of Perturb

Fig 5.2 show the p-v characteristics of a photovoltaic system, by analyzing the p-v characteristics we are able to see that on right facet of MPP because the voltage decreases the power will increase however on left facet of MPP increasing voltage will increase power.[25] this can be the most plan we've utilized in the P&O algorithmic program to track the MPP [11]. The flow chart of P&O algorithmic program is manifested in figure 5.3.

As we are able to see from the flow chart 1st of all we have a tendency to extent voltage & current, by use these ideals we have a tendency to analyse power, calculated power is equated with earlier one and consequently we have a tendency to increase or decrease voltage to find the maximum power by fluctuating the duty cycle of convertor.[26]

# CHAPTER-6

# SIMULATION AND RESULT

## 6.1 SIMULATION AND RESULTS OF CONVERTER

The simulation model of proposed zero voltage transition converter is as shown below

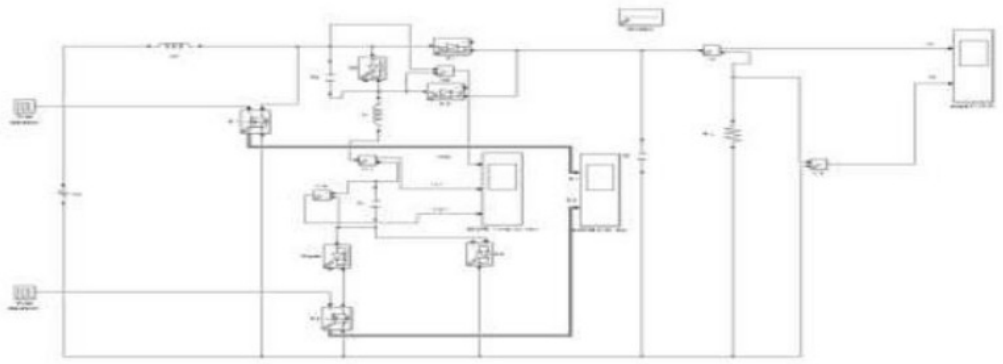

Fig 6.1: Simulation model of proposed converter

The waveforms of the auxiliary circuit elements for a resonant cycle & the main switch current and voltage waveforms subsequent to the confirmation of the converter operation for single switching cycle are given below.

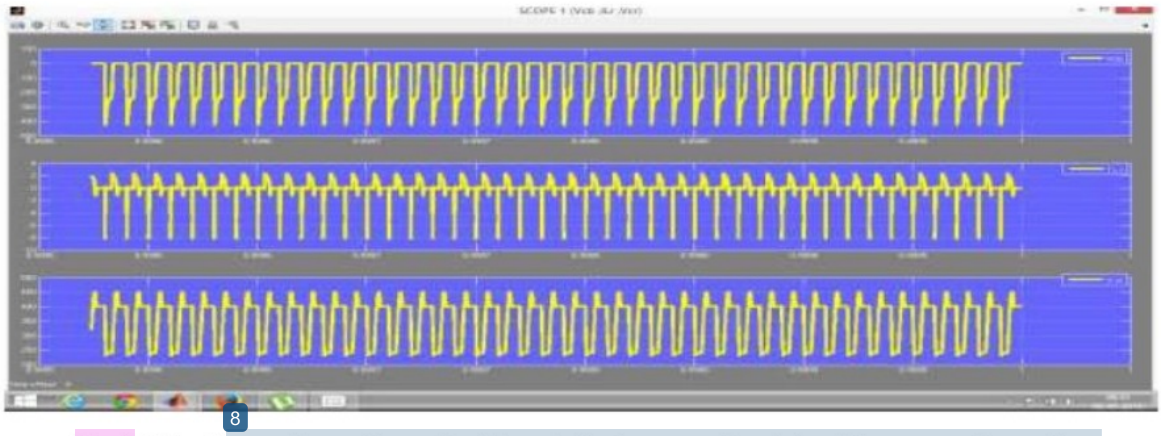

Fig 6.2:Feed capacitor voltage, Auxiliary inductor current and Auxiliary capacitor voltage

Figures 6.2 illustrate the resonating circuit waveforms for one resonant cycle which is a element of the switching cycle. These waveforms are compared with the systematic waveforms shown in the figure 3.10. This shows the variation in feed forward capacitor voltage waveform.

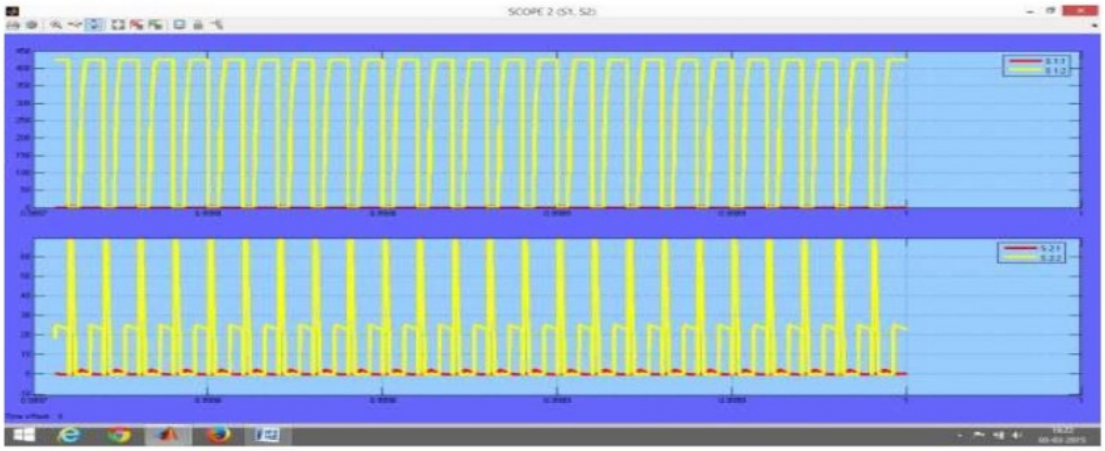

Fig 6.3:Main switch current and voltage and Auxiliary switch curret and voltage

Figure 6.3 shows the main switch voltage waveform and the manifest the main switch current waveform. Superimposing one on the other, the zero voltage turn ON of the main switch is shown in figure and the decreased voltage turn-off of the main switch is shown in the figure. The voltage during turn-OFF is calculated to be 80 volts.

The waveform of current and voltage across load is as shown

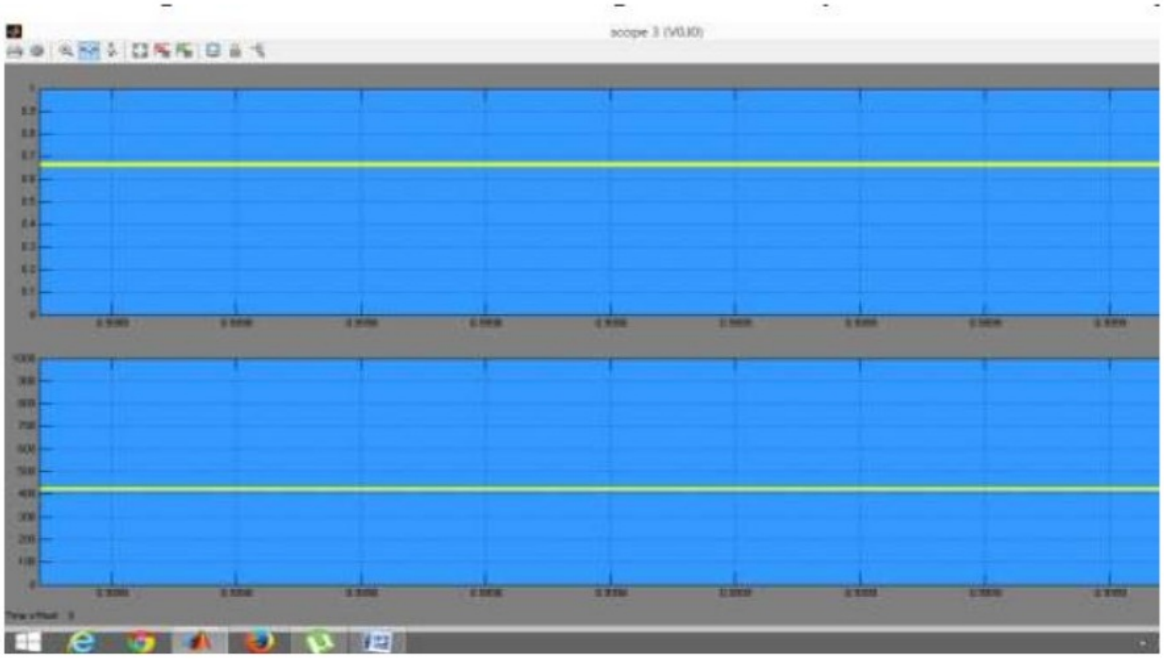

Fig 6.4 : Current and voltage across load

The circuit is running beneath different input conditions with input voltage ranging from 100- 270V and the circuit is establish to provide an output voltage of 400V for unlike values of duty cycles ranging from 35-81.2% and is shown in table 6.1.

| Input voltage $V_{in}$(V) | Duty cycle δ (%) | Input voltage $V_{in}$(V) | Duty cycle δ (%) |
|---|---|---|---|
| 270 | 34.00 | 184 | 55.45 |
| 265 | 35.25 | 179 | 56.80 |
| 260 | 36.60 | 174 | 58.25 |
| 255 | 37.90 | 169 | 59.70 |
| 250 | 39.20 | 164 | 61.10 |
| 245 | 40.60 | 159 | 62.60 |
| 240 | 41.85 | 154 | 64.10 |
| 235 | 43.20 | 149 | 65.54 |
| 230 | 44.56 | 144 | 67.10 |
| 225 | 45.90 | 139 | 68.70 |
| 220 | 47.30 | 134 | 70.3 |
| 215 | 48.60 | 129 | 72 |
| 210 | 50.00 | 124 | 73.7 |
| 205 | 51.30 | 119 | 75.6 |
| 200 | 52.70 | 114 | 77.65 |
| 195 | 54.00 | 109 | 80.2 |

Table 6.1 Duty cycle for input voltage of 400V output

Also the RMS current flowing through the auxiliary switch is calculated for different standards of input voltage and is tabulated below in table 04

| Input voltage (volts) | Duty cycle (%) | Rms current of switch-2(Amps) |
|---|---|---|
| 270 | 34.99 | 0.134 |
| 210 | 52.29 | 0.242 |
| 160 | 66.56 | 0.413 |
| 120 | 81.19 | 0.633 |

Table 6.2 Auxiliary switch RMS current

## 6.2 LOSS CALCULATION AND COMPARATIVE STUDY

A conventional hard switching converter is considered for the same specifications in order to hold out the comparative study. A boost converter with the component values given in table 6.1 is simulated and the losses of respective converters are compared.

| Sl.No. | Component | Symbol | Value |
|---|---|---|---|
| 1 | Boost inductor | $L_{ind}$ | 5.57mH |
| 2 | Output capacitor | $C_{out}$ | 1.23$\mu$F |

Table 6.3 Conventional hard switching converter components

The switching losses of any switch is calculated using the following formula

$$P_{sw} = V_O I_O F_{sw} [\frac{T_{on}+T_{off}}{2}] \quad (6.1)$$

## 6.3 LOSSES STUDIED IN THE SOFT SWITCHING CONVERTER

The main switch's turn ON alteration takes place beneath zero voltage. Therefore from the above formula the switching losses of the main switch during turn ON are zero.

$$P_{sw1on} = 0W$$

The main switch's turn OFF transition takes place at decreased voltage and the voltage during turn OFF is calculated and is calculated to be 80V and the peak current that is passed by this switch is calculated to be 4A.

The switching losses during turn OFF time is considered as follows

$$P_{sw1off} = 80 * 4 * 10^5 \left(\frac{0 + 100 * 10^{-9}}{2}\right) = 1.6W$$

The auxiliary switch's turn ON transition takes place under ZCS and its turn OFF transition takes place under ZVS. Therefore the switching losses of $S_2$ are zero.

$$P_{sw2on} = P_{sw2off} = 0\text{W}$$

The total switching losses are

$$P_{sw} = P_{sw1} + P_{sw2} = 1.6 + 0 = 1.6W$$

The conduction losses of the switches are measured using the formula

$$P_{sw\_cond} = 1.8 * I_{s-rms}^2 * R_{on} \qquad (6.2)$$

The rms current of the main switch is calculated to be 2.3481Amperes and the conduction losses are measured as follows

$$P_{cond\_s1} = 1.8 * 2.3481^2 * 0.85 = 8.435W$$

The rms current of the auxiliary switch is calculated to be 0.786 Amperes and the conduction losses are measured as follows

$$P_{cond\_s2} = 1.8 * 786^2 * 0.85 = 0.947W$$

The overall conduction losses of the switches are

$$P_{cond\_s} = 8.4357 + 0.947 = 0.93827W$$

The conduction losses of the diode are multiple of the forward voltage drop across the diode and the standard current flowing through it. The forward voltage drop is calculated to be 0.8027 Volts and the current flowing during this is the load current which is 0.625 Amperes. So the conduction losses of the diode are measured as follows.

$$P_{d\_cond} = V_f I_{D\_avg} = 0.827 * 0.625 = 0.502W$$

The total losses in the converter are

$$P_{losses} = P_{sw} + P_{cond} + P_D = 0.827 * 0.625 = 0.502W$$

The efficiency of the converter is calculated as follows

$$\eta = \left(\frac{P_0}{P_0 + P_{losses}}\right) * 100 = \left(\frac{250}{250 + 11.480}\right) * 100$$

## 6.4 LOSSES IN CONVENTIONAL HARD SWITCHING CONVERTER

The single switch in this converter is hard switched and the switching losses are measured using the equation 6.1. The voltage across the switch throughout ON and OFF conditions is 400V and the peak current is calculated to be 4.6A. The switching losses of the switch in conventional boost converter are

$$P_{sw} = 400 * 4.6 * 10^5 \left(\frac{100 * 10^{-9} + 100 * 10^{-9}}{2}\right) = 18.4W$$

The conduction losses in the hard switching converter are measured using the formula mentioned in equation 6.2. The rms current flowing throughout the switch is calculated to be 2.2632A. The conduction losses are measured as

$$P_{sw\_cond} = 1.8 * 2.2632^2 * 0.85 = 7.836W$$

The conduction losses of the diode stay equivalent as that of the soft switching converter.

$$P_{D\_cond} = V_f I_{D\_avg} = 18.4 * 0.625 = 0.502W$$

The total losses in the converter are

$$P_{losses} = P_{sw} + P_{cond} + P_{D\_cond} = 18.4 + 7.386 + 0.502 = 26.288W$$

The efficiency of the converter is calculated as follows

$$\eta = \left(\frac{P_0}{P_0 + P_{losses}}\right) * 100 = \left(\frac{250}{250 + 26.288}\right) * 100 = 90.4\%$$

All the results obtained from the comparative study are tabulated and shown in table 6.2

| Serial No. | Parameters | Hard switching converter | Soft switching converter |
|---|---|---|---|
| 1. | $P_{sw}$ | 18.39 | 1.59 |
| 2. | $P_{cond}$ | 7.387 | 9.383 |
| 3. | $P_D$ | 0.519 | 0.519 |
| 4. | %η | 90.39 | 95.59 |

Table 6.4 P Comparison of soft switching and hard switching topology

## 6.5 SIMULATION AND RESULT OF PV ARRAY

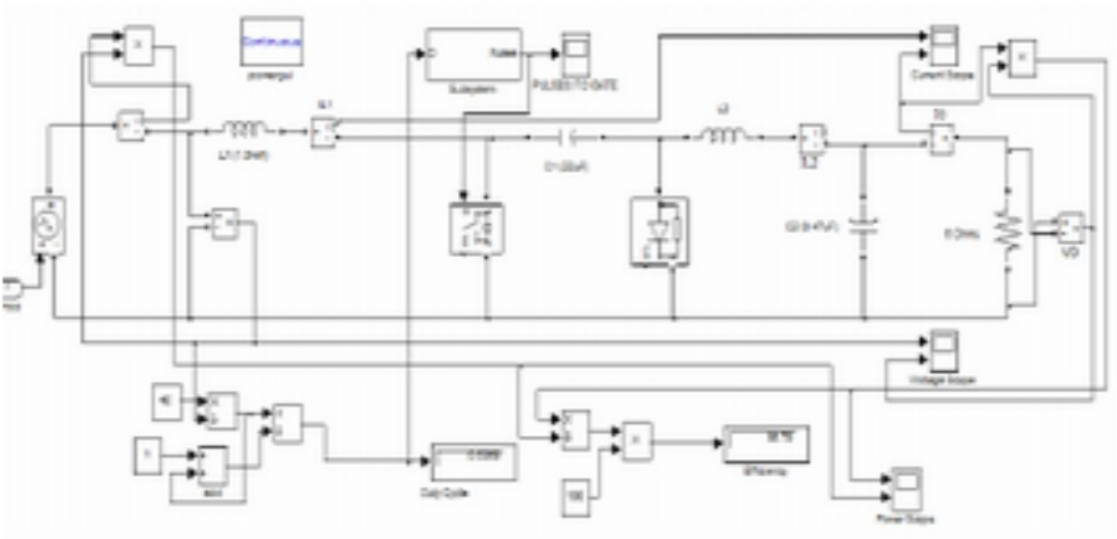

Fig 6.5: Simulation of MPPT using P&O Algorithm[24]

The simulation results of the PV array are shown below. The I-V characteristics and P-V characteristics are in figures 6.6 and 6.7 respectively. The open circuit voltage of the simulated PV array is 180 volts and the short circuit current is 2.25 amperes.

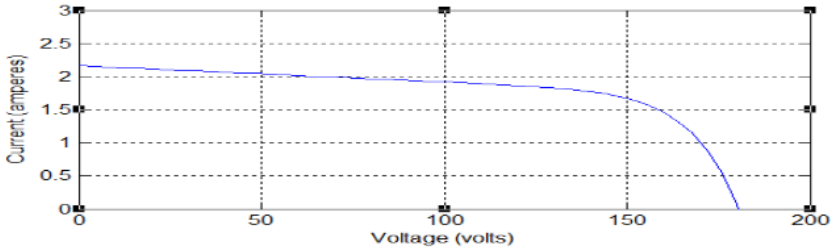


Fig 6.6: The PV array current-voltage characteristics

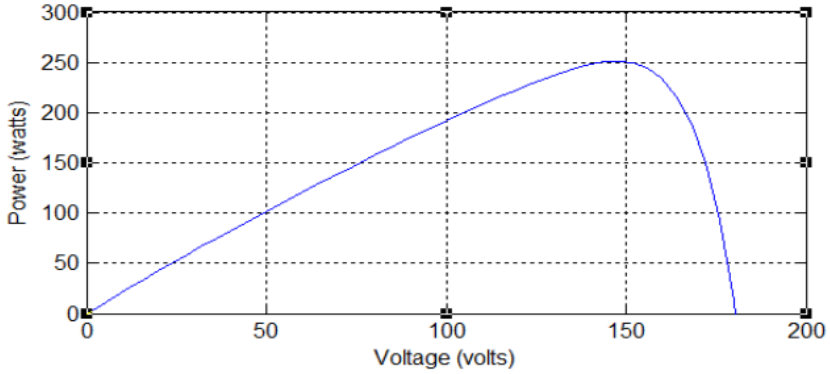


Fig 6.7: The PV array Power-Voltage characteristics

The tracked operating point at which maximum power can be obtained using an MPPT algorithm as indicated below in figure 6.8

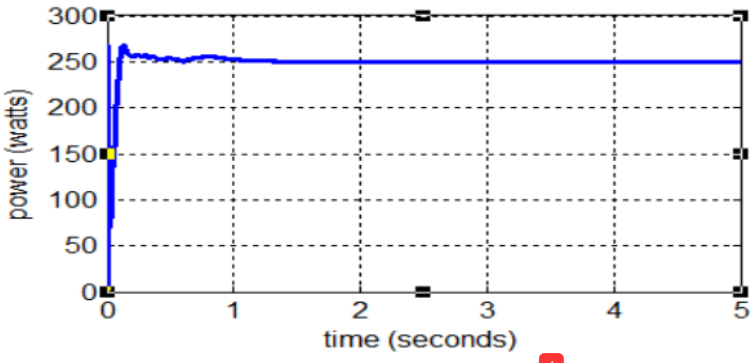


Fig 6.8: The PV array Output Power after MPPT

## 6.6 CONCLUSIONS

- The soft switch losses of conventional converter are much less than those of the hard- switched converter.
- The auxiliary switch losses are 0 in both converters since no auxiliary switch in conventional converter and in the new converter it's soft switched
- The losses occurred during diode conduction remain equal in both the cases
- By varying the RMS current carried through the switches the conduction losses can be varied. As the auxiliary circuit losses are summed up to conduction losses it is found to be more in gentle switched converter .

But the switching loss contribution of the hard switching converter dominates in the calculation of total losses and hence the soft-switched converter is found to be more efficient than the conventional hard-switched converters.

## 6.7 FUTURE SCOPE

Work can be executed on similarly reducing the voltage during turn-off transition of the main switch or making it zero without growing the circuit complexity.

# REFERENCES

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