SIGNAL GENERATION AND PROCESSING APPLICATIONS USING CURRENT MODE BUILDING BLOCKS

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by

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Place: Delhi

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Dedicated

To

My family & friends

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Signal Generation and Processing Applications Using Current Mode Building Blocks

Tvisha Pushkar

ABSTRACT

This thesis presents a comprehensive study on signal generation and processing using current-mode active building blocks (ABBs), specifically focusing on the Universal Voltage Conveyor (UVC) and the Voltage Differencing Buffered Amplifier (VDBA). These elements represent a significant advancement in analog signal processing, offering improved performance in speed, linearity, power efficiency, and CMOS compatibility over traditional voltage-mode circuits. The work addresses key bottlenecks in existing oscillator and filter designs by developing novel circuit architectures that are compact, low-power, and capable of robust and tunable operation under practical non-idealities.

The research is structured in four parts. The first part introduces the foundational principles of analog signal processing and the advantages of current-mode operation. It also presents a literature review on the evolution and applications of UVC and VDBA, identifying gaps in tuning flexibility, harmonic distortion, and sensitivity to component variations. Particular attention is given to the third-order quadrature sinusoidal oscillator (TOQSO) and multiple-input single-output (MISO) universal filter designs.

The second part of the thesis proposes two innovative circuits: an improved TOQSO using UVC and a compact, electronically tunable MISO universal filter using VDBA. The proposed TOQSO achieves independent control over the frequency of oscillation (FO) and condition of oscillation (CO), reducing total harmonic distortion (THD) to below 1.5%, a marked improvement over existing OTA- and CCII-based designs. The MISO filter, designed using a single VDBA, two grounded capacitors, and one resistor, realizes all five second-order filter responses (low-pass, high-pass, band-pass, band-reject, and all-

pass) without the need for reconfiguration. Both circuits exploit the strengths of their respective ABBs to address the shortcomings of earlier designs.

In the third part, rigorous mathematical modeling is presented for both circuits, followed by detailed sensitivity analysis that confirms the low dependence of key parameters (ω_0 and Q) on passive component variations. SPICE simulations using 0.18 µm CMOS technology validate the theoretical predictions. For the TOQSO, output waveforms, frequency spectra, and Lissajous patterns confirm sinusoidal oscillation with quadrature phase accuracy and spectral purity. For the MISO filter, frequency response plots for each mode demonstrate accurate cutoff and center frequencies. Simulation results align closely with analytical derivations.

To bridge the gap between simulation and real-world applicability, experimental prototypes of both designs were implemented using commercially available ICs. The TOQSO exhibited stable sinusoidal outputs with precise 90° phase difference, and the filter achieved consistent performance across a frequency range from 10.5 kHz to 500.5 kHz. These results confirm the feasibility and robustness of the proposed circuits under practical conditions, including non-idealities such as voltage tracking errors and finite transconductance mismatches.

A comparative performance analysis against conventional designs—OTA-, CCII-, and CDBA-based—demonstrates the superiority of the proposed solutions in terms of spectral purity, power efficiency, component count, and CMOS integration readiness. The VDBA-based filter exhibits lower power consumption and higher Q-factor than its counterparts, while the UVC-based oscillator outperforms in frequency stability and THD.

The thesis concludes by outlining the broader implications of these findings. The proposed designs contribute to the advancement of low-voltage, low-power analog front-end systems, particularly in wearable biomedical devices, adaptive communication systems, sensor interfaces, and energy-constrained IoT nodes. Their compactness and simplicity make them ideal candidates for integration into modern VLSI systems.

Future directions for research include extending these architectures for fully electronically tunable operation, deploying them in multi-band or reconfigurable systems, and implementing them in deep-submicron or emerging device technologies such as FinFETs and CNTFETs. Furthermore, integrating these circuits into system-on-chip (SoC) solutions for biomedical and communication applications could significantly enhance performance and miniaturization. Through its dual focus on theoretical rigor and practical validation, this thesis contributes to the evolving landscape of analog signal processing, establishing reliable and efficient building blocks for next-generation analog integrated circuits.

LIST OF PUBLICATIONS

[1] T. Pushkar and R. Pandey , “ Implementation of a Single VDBA-Based Electronically Tunable Universal Filter Using Commercial ICs,” May 22, 2025

[2] T. Pushkar and R. Pandey, “Voltage Mode Third-order Quadrature Sinusoidal Oscillator using UVC,” May 22, 2025

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List of Symbols

$\|S\|$	Sensitivity
α	Voltage ratio
ϵ_v	Voltage tracking error
β	Transconductance tracking error

CHAPTER 1

INTRODUCTION

1.1 Overview of Analog Signal Processing

Analog signal processing plays a vital role in contemporary electronics, enabling real-time manipulation of continuously varying signals. Unlike digital processing, which requires sampling and quantization, analog processing is inherently faster and consumes less power, making it ideal for front-end electronics in applications such as biomedical instrumentation, communication systems, and industrial automation. The increasing demand for compact, efficient, and high-performance electronic systems has spurred the development of novel analog processing architectures, especially those operating in current mode.

1.2 Importance of Current Mode Circuits in Modern Electronics

Current mode (CM) circuits have gained significant traction over traditional voltage mode (VM) circuits due to their superior performance in bandwidth, linearity, and low-voltage operation. CM techniques reduce voltage swings across nodes, thus minimizing power consumption and improving noise immunity. These characteristics are particularly beneficial in applications requiring high-speed signal processing, such as wireless communication, signal modulation/demodulation, and real-time analog computation. With CMOS scaling and the push toward ultra-low-power systems, current mode circuits are indispensable in achieving next-generation analog signal processing goals.

1.3 Introduction to Active Building Blocks

Active Building Blocks (ABBs) form the foundation of analog signal processing. Among these, the Universal Voltage Conveyor (UVC) and Voltage Differencing Buffered Amplifier (VDBA) have emerged as high-performance options due to their versatility and compatibility with CMOS integration. UVCs support both voltage and current mode operations and are especially suited for oscillator designs requiring phase accuracy and frequency stability. VDBAs, on the other hand, provide voltage differencing and buffered outputs, making them ideal for universal filter and amplifier designs. Both ABBs offer tunability, low power operation, and the ability to simplify complex analog functions, making them critical in modern integrated analog design.

1.4 Motivation Behind the Research

Despite the advancements in ABBs such as UVCs and VDBAs, existing circuit designs face several limitations. Quadrature sinusoidal oscillators (QSOs) built with UVCs often exhibit high total harmonic distortion (THD), limited frequency stability, and dependence between condition of oscillation (CO) and frequency of oscillation (FO). Similarly, VDBA-based universal filters, though promising, suffer from limited tunability, high sensitivity to component variations, and challenges in CMOS integration due to design complexity. These gaps highlight the need for improved architectures that leverage the strengths of current mode design while addressing practical bottlenecks.

1.5 Objectives of the Work

This research aims to:

• Analyze the performance limitations in existing UVC- and VDBA-based oscillator and filter designs.

• Propose an improved third-order quadrature sinusoidal oscillator (TOQSO) using UVC with better frequency stability, low THD, and independent tuning of CO and FO.
• Design a compact, low-power, MISO universal filter using VDBA with independently tunable ω_0 and Q, reduced component dependency, and high CMOS compatibility.
• Validate proposed designs through rigorous mathematical modeling, SPICE simulations, and experimental verification.

• Compare the performance of the proposed designs with state-of-the-art circuits to establish practical relevance and superiority.

1.6 Organization of the Thesis

The thesis is structured into four main parts: Introduction, Literature Survey & Identification of Problem and Issues, Formulation & Solution Approach along with Findings, Results, Discussion & Implementation and lastly Conclusion, Future Scope & Social Impact

• Chapter 1 introduces the scope, importance, and motivation of the work.
• Chapter 2 presents a detailed literature review of UVC, covering its evolution, comparison with other ABBs, and application areas.

• Chapter 3 critically evaluates existing TOQSO designs using UVC, identifying design gaps and performance issues.

• Chapter 4 proposes an improved TOQSO using UVC, with full derivation, simulation, and comparative study.

• Chapter 5 provides a literature review of the VDBA, its performance benchmarks, and identifies research gaps.

• Chapter 6 reviews previously implemented universal filters using VDBA and identifies limitations.

• Chapter 7 presents the proposed MISO universal filter using VDBA, along with modeling, validation, and comparative analysis.

• Chapter 8 summarizes key contributions, highlights the comparative merits of the proposed designs, discusses potential future enhancements, and evaluates the social and technological impact of this work.

This structured approach ensures clarity in presenting the progression from problem identification to proposed solutions and their experimental validation.

CHAPTER 2

LITERATURE REVIEW AND EXISTING IMPLEMENTATIONS OF UVC-BASED SINUSOIDAL OSCILLATORS

2.1 Introduction to Universal Voltage Conveyor (UVC)

UVC is a popular high-performance current-mode active building block (ABB) intended for analog applications. The circuit employing UVC has a wide scope for application in designing oscillators, filters, and modulators, especially needed in telecommunication, biomedical devices, and instrumentations.

UVCs are characterized by speed, low consumption of power, and well-served improvements in signal integrity. UVCs have a greater advantage over the typical active elements like OTAs and CDBAs because they provide voltage and current differencing simultaneously rather than separately, thus ensuring flexible design and high performance.

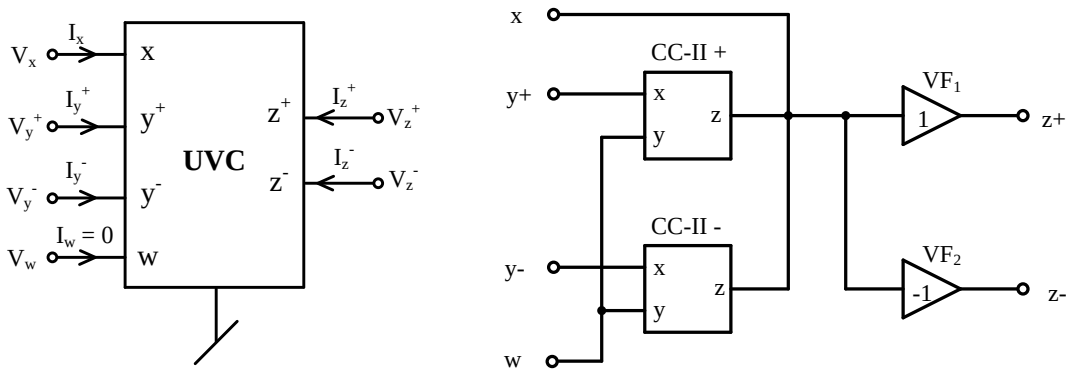


Fig. 2.1. a) Symbolic Representation of UVC. b) Ideal Circuit Model Of UVC [1]

The following sections trace the architectural evolution of UVCs across generations and evaluate their application domains to identify critical design challenges

2.1.1 Key Features of UVC

The Universal Voltage Conveyor (UVC) is characterized by several key features that make it a versatile component in analog signal processing. It employs a six-port architecture that enables both voltage and current differencing functions, enhancing its functional scope in complex circuits. The UVC offers high input impedance and low output impedance, which supports efficient signal transmission and minimizes loading effects. Additionally, it exhibits wide bandwidth and low distortion, making it particularly suitable for high-frequency applications. Its improved linearity and tunability further

contribute to its effectiveness in adaptive signal processing systems. Another notable advantage is its strong noise immunity, which ensures reliability in environments with significant electrical interference [2].

2.2 Architectural Evolution of UVC

The Universal Voltage Conveyor (UVC) has undergone significant architectural transformations over the decades to address evolving performance and integration demands in analog signal processing. This section outlines the historical development of UVCs in three stages—first-generation (VCI), second-generation (VCII), and modern UVCs—highlighting their configurations, functional advantages, and limitations at each stage.

2.2.1 First-Generation Voltage Conveyors (VCI)

The Universal Voltage Conveyor (UVC) was introduced as a voltage-mode counterpart to the first-generation current conveyors, with the objective of maintaining wide bandwidth and linear signal transfer. This concept was first proposed by Filanovsky and Stromsmoe in 1981. Structurally, the UVC is a three-terminal device comprising Y (input), X (intermediate), and Z (output) terminals. The terminal behavior is defined by specific relationships: the voltage at terminal X equals the voltage at terminal Y, expressed as $V_X = V_Y$, and the currents at terminals Y, X, and Z are equal, denoted by $I_Y = I_X = I_Z$. The device exhibits high input impedance at the Y terminal and low output impedance at the Z terminal, making it well-suited for cascading in voltage-mode signal processing circuits. The symbolic representation of the first-generation UVC, including its terminal relationships and signal flow paths, is illustrated in Figure 2.2.

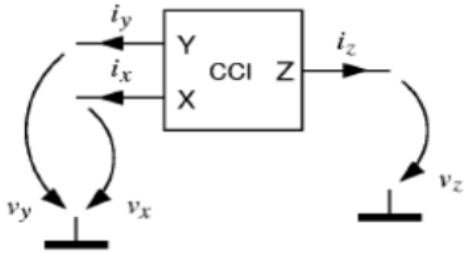
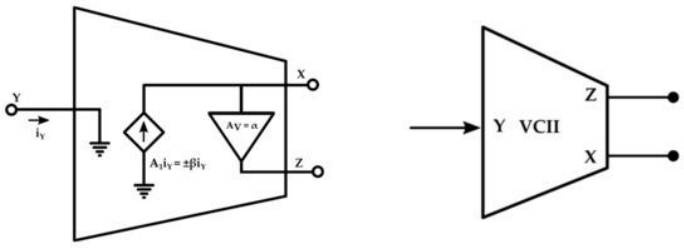


Fig 2.2: Symbolic Diagram of First-Generation UVC

The first-generation Universal Voltage Conveyor (UVC), despite its advantages, has several limitations. It lacks differential input capability, which restricts its use in applications requiring common-mode rejection. Additionally, it does not offer electronic tunability, limiting its flexibility in dynamically adjustable systems. Furthermore, its structure shows low adaptability to integration, making it less suitable for modern integrated circuit (IC) design environments.These characteristics made VCI suitable for early analog computing but insufficient for modern high-speed, low-power applications.

2.2.2 Second-Generation Voltage Conveyors (VCII)

The Second Generation Voltage Conveyor (VCII) was developed to address the shortcomings of the First Generation Conveyor (VCI), particularly in improving impedance matching and enhancing signal buffering capabilities for voltage-mode systems. It is configured as a three-terminal active block consisting of a low-impedance current input at terminal Y, a high-impedance current output at terminal X, and a low-impedance voltage output at terminal Z. Ideally, the VCII satisfies the relationships $I_X=\pm I_Y$ for current transfer from Y to X, and $V_Z=\pm V_X$ for voltage transfer from X to Z. This dual behavior makes the VCII function as a voltage buffer between terminals X and Z, and simultaneously as a current buffer from Y to X. The low output impedance at Z facilitates easy interfacing with voltage-mode signal paths, while the low impedance at Y supports current summing or injection. Additionally, the high impedance at X minimizes loading effects, allowing flexible circuit integration.



(a) (b)

Fig 2.3. Second Generation Voltage Conveyor (VCII): (a) Internal Structure; (b) Symbol.[3]

Figure 2.3 illustrates both the symbolic representation and the internal structure of the VCII, highlighting its signal flow and operational characteristics. Among its key advantages are improved signal transfer performance, reduced noise levels, and enhanced linearity, all of which contribute to its suitability in voltage-mode filters and precision rectifier circuits. However, despite these strengths, the VCII faces limitations such as limited electronic tunability and significant sensitivity to parasitic elements, making it less ideal for adaptive or reconfigurable analog systems. In terms of applications, VCIIs have found use in active filtering, basic modulation circuits, and precision rectification tasks.

2.2.3 Modern Universal Voltage Conveyor (UVC)

Modern Universal Voltage Conveyor (UVC) integrates both voltage and current differencing capabilities, allowing it to handle complex analog signal processing tasks efficiently. It offers a broadened frequency response, making it well-suited for

applications operating in the GHz range. The UVC is designed to deliver enhanced linearity and operates with low power consumption, while also providing improved electronic tunability. These attributes make it highly adaptable for implementing advanced analog circuits such as filters, oscillators, and converters. Furthermore, its mathematical modeling and terminal relationships have been extended to support differential-mode operations and electronically tunable features, broadening its range of potential applications.

The modern Universal Voltage Conveyor (UVC), with stronger signal handling and programmable functionality, builds upon the principles of the previous generations. This is achieved due to the integration of voltage and current processing with a high degree of differential signal integrity, electronically controlled gain, and impedance characteristics.

One of the greatest enhancements to modern UVCs is frequency scalability reaching the order of several GHz, thereby allowing them to serve RF, high-speed communication, and biomedical signal-process applications. Quite a few other advantages are gained through the low-voltage and low-power design of modern UVCs in CMOS technology, which now makes them relevant to portable and battery-operated systems. [6][7]

These evolved UVCs offer:

- The voltage input terminals have a high input impedance, while the voltage output terminals have a low output impedance. Precision current tracking and voltage buffering
- Reduced sensitivity to parasitics, improving stability in integrated circuit implementations
- Compatibility with tunable analog blocks, enabling adaptive and reconfigurable systems

Modern research further explores low-noise, high-linearity UVCs with minimized harmonic distortion and optimized for process-voltage-temperature (PVT) variations, leading to consistent performance across operating conditions [8].

These improvements have positioned the UVC as a core analog building block for next-generation analog and mixed-signal integrated circuits

Mathematical representation and port relationships defined by [2]:

$$\begin{pmatrix} I_x \\ I_w \\ V_{y^+} \\ V_{y^-} \\ V_{z^+} \\ V_{z^-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_x \\ V_w \\ I_{y^+} \\ I_{y^-} \\ I_{z^+} \\ I_{z^-} \end{pmatrix} \quad (2.1)$$

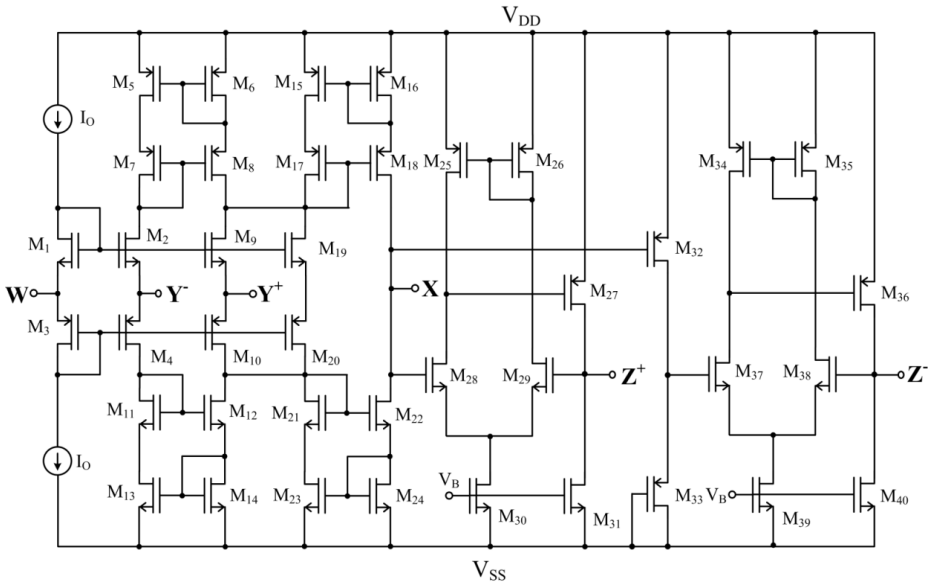


Fig. 2.4 CMOS Implementation Of UVC [2]

i. Applications:

- RF circuits, adaptive filtering, biomedical instrumentation, and IoT analog front-ends

Implication of Architectural Evolution on Design Challenges

While the evolution from VCI to VCII and finally to modern UVCs has substantially enhanced signal fidelity, frequency response, and integration potential, persistent challenges remain. Notably, tuning limitations, parasitic sensitivity, and lack of standardized commercial IC availability continue to constrain UVC adoption in high-performance applications. These limitations motivate the exploration of improved architectures—such as the TOQSO design proposed in this thesis—that build upon UVC capabilities while mitigating these fundamental shortcomings.

2.3 Comparative Analysis of UVC with Other Current-Mode ABBs

A versatile active building block for analog signal processing, the Universal Voltage Conveyor (UVC) has benefits over traditional current-mode ABBs like the Operational Transconductance Amplifier (OTA) and the Second-Generation Current Conveyor (CCII). This section aims at providing a comparative analysis to underscore unique features and performance advantages of the UVC.

1. Functional Versatility and Integration

UVC architecture enables seamless integration of voltage-mode and current-mode operations, thereby allowing for realization of various filter configurations without changing the circuit topology. For instance, Pushkar et al. (2017)[9] demonstrated voltage-mode universal biquadratic filtering using one UVC, with low active and passive sensitivities, independent control of natural frequency and bandwidth, and no matching of components was required.

2. Impedance Characteristics and Cascadability

UVCs are easy to cascade in voltage-mode circuits because of their large input and low output impedances. This is very useful in designing filters and oscillators where impedance matching is imperative. Traditional CCII-based designs usually need an extra buffering stage to achieve similar performance.

3. Performance in Nonlinear Applications

In cases such as full-wave rectification, the UVCs are noted to give better performance than CCIIs. Burian et al. (2012)[10] illustrated a voltage-mode full-wave rectifier employing both UVC and CCII to underscore the high input and low output impedance of the UVC, leading to enhanced dynamic range and frequency response.

4. Simplified Circuit Design

Due to the multifunctional nature of the UVC, the need for many active components is reduced, simplifying circuit design and potentially leading to reduced power consumption and area. In contrast, designs employing OTAs may require complicated biasing schemes and multiple stages in order to achieve a similar degree of functionality.

5. Comparative Summary

Table 2.1: Comparison of UVC With Other Current-Mode ABBs

Feature	**UVC**	**CCII**	**OTA**
Mode of Operation	Voltage and Current	Primarily Current	Primarily Current
Input Impedance	High	Low	High
Output Impedance	Low	High	High
Cascadability	Excellent	Moderate	Moderate
Circuit Complexity	Low	Moderate	High
Application Versatility	High	Moderate	High
Power Consumption	Low	Moderate	High

This comparative analysis demonstrates that while UVCs offer superior functional and structural characteristics compared to OTAs and CCIIs, practical issues such as design complexity under non-ideal conditions and sensitivity to parasitic elements still limit their broader adoption. These observations define the starting point for identifying the performance bottlenecks discussed later in this chapter.

2.4 Applications of UVC Circuits

2.4.1 Sinusoidal Oscillators

In the art of creating sinusoidal oscillators, such as third-order quadrature sinusoidal oscillators (TOQSOs), UVCs are crucial components. The UVC's autonomous regulation of the oscillation's frequency (FO) and condition (CO) enhances the oscillator's signal generation's accuracy and stability. Two UVCs, three capacitors, and three resistors are used in the TOQSO's configuration to generate two voltage outputs that are 90 degrees apart. Low passive sensitivity could be achieved by independently adjusting the oscillation frequency and condition using different capacitors. The design's suitability for signal creation in communication systems was evident when it was validated through SPICE simulations using TSMC 0.18 μm CMOS specifications [11].

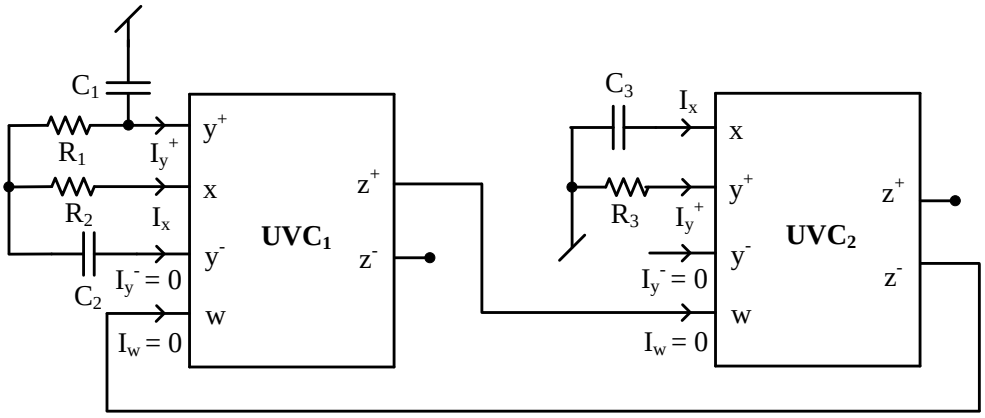


Fig.2.3 TOQSO using UVCs[11]

Another specialized example is the single-resistance-controlled sinusoidal oscillator (SRCO) using one UVC. This circuit showed that FO and CO could be controlled independently with very few components and exhibited low harmonic distortion, making it applicable to control and instrumentation [12].

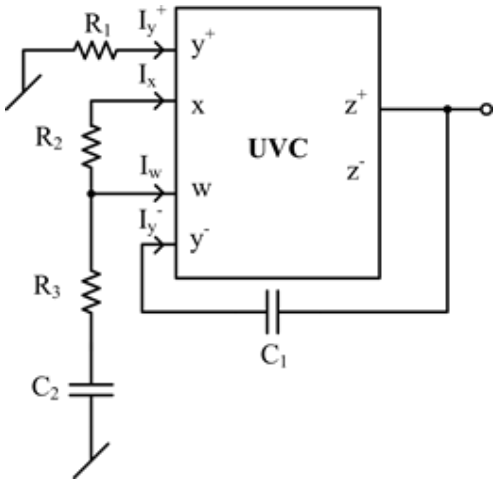


Fig.2.4 Single-Resistance Controlled Sinusoidal Oscillator (SRCO) Using UVCs[12]

2.4.2 Active Filters

UVCs have been successfully used in certain active filter designs, such as band-pass, high-pass, and low-pass filters. Compared to conventional designs, these designs are much simpler, less noisy, and more selective. For example, via a single UVC, a voltage-mode first-order all-pass filter is achieved with all grounded passive components. This feature simplifies layout and is advantageous for monolithic integration. Less sensitivity with respect to component variations, the circuit is expected to be appropriate for biomedical as well as audio signal processing [13].

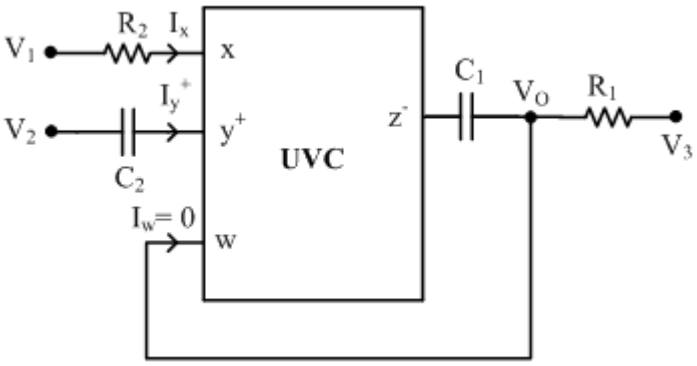


Fig.2.5 First-Order All-Pass Filter in Voltage Mode with A Single UVC [13]

2.4.3 Modulation and Demodulation Circuits

The UVC circuits are advantageous in power savings and minimize signal distortion, two crucial factors in wireless communication and RF signal processing, when performing modulation and demodulation. A fast voltage-mode full-wave rectifier using a UVC was proposed with an improved dynamic range and frequency response over traditional OTA or CDTA-based circuits. The circuit offered high precision and low distortion, which are critical for amplitude and frequency modulation systems [14].

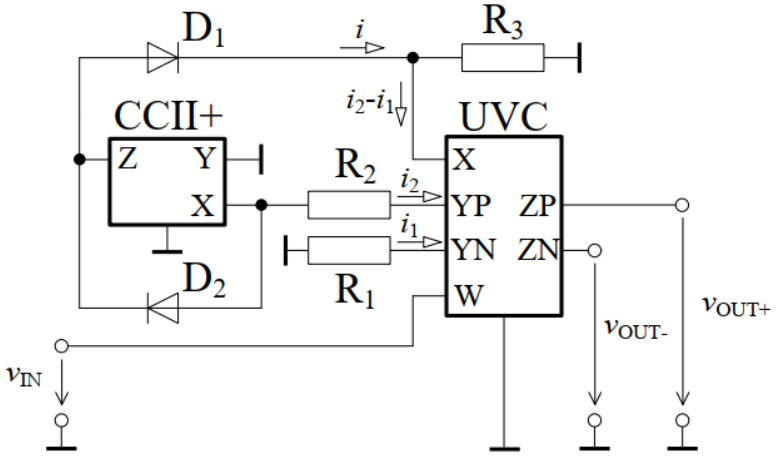


Fig.2.6 Full wave rectifier using an UVC[14].

2.4.4 Analog Computing and Signal Conditioning

The UVCs are used extensively in the field of analog computation: design of analog multipliers, dividers, integrators, and differentiators, etc. Their fast operations in performing analog computations are advantageous for real-time signal processing.

An illustrative example is the implementation of KHN-equivalent voltage-mode filters using UVCs. The circuit highlighted the versatility of UVCs in analog computing and signal conditioning systems, and its performance was validated through simulation and practical considerations for adaptive control and AI-based analog hardware [13].

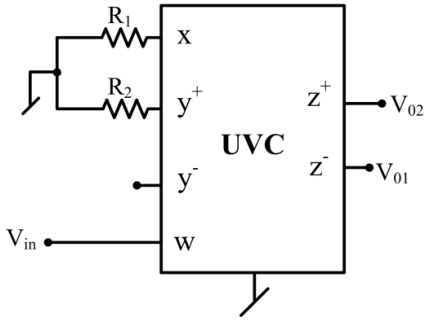


Fig. 2.7. Inverting/Non-Inverting Amplifier UVC

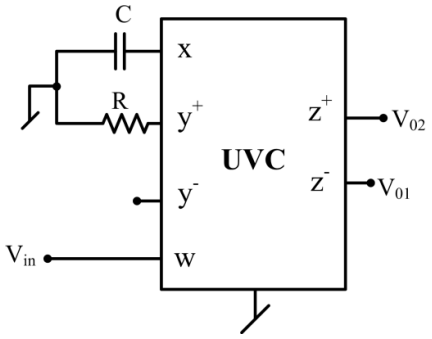


Fig. 2.8 Integrator using UVC

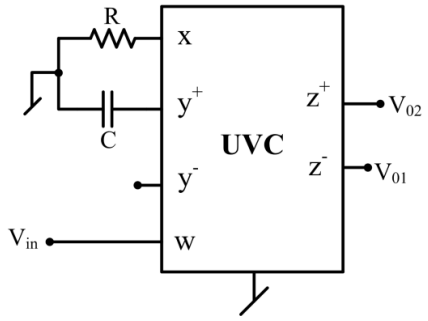


Fig. 2.9. Differentiator using UVC

Although UVCs have shown versatility in oscillators, filters, and modulation circuits, practical challenges such as harmonic distortion, limited tuning flexibility, and integration constraints are frequently observed across implementations. These are explored in the next section as part of the research problem.

2.5 Research Gaps and Performance Bottlenecks

Despite the numerous advantages of Universal Voltage Conveyor (UVC) circuits in analog signal processing, several challenges hinder their optimal performance and wider adoption. Based on the survey of past implementations and architectural studies, the following design bottlenecks emerge as major barriers to UVC-based analog system integration:

1. Non-Ideal Effects in High-Frequency Operations

At high frequencies, non-idealities such as parasitic capacitances, interconnect delays, and layout-induced feedback can significantly degrade the performance of UVC-based circuits. These effects often lead to bandwidth reduction, gain peaking, and signal distortion. For example, the Miller effect introduces amplified parasitic capacitance between input and output terminals, reducing the high-frequency response of amplifying stages [15].

2. Parasitic Effects in Integrated Implementations

In integrated circuit (IC) realizations, parasitic elements such as substrate coupling, junction capacitances, and interconnect resistance play a crucial role in limiting the accuracy and stability of UVC-based circuits. These effects must be carefully modeled and minimized during layout to ensure reliable operation, especially in precision analog systems [16].

3. Limited Commercial Availability

UVC integrated circuits generated by commercial entities are another bottleneck to the broad acceptability of UVCs. Circuit designers are therefore propelled to discrete implementations or custom IC fabrication, a clear increase in development cost and time. This has been analyzed as a practical limitation in numerous UVC-based system designs [17].

4. Power Supply Dependencies

UVC circuits can respond to power supply variations, thus affecting their transfer characteristics and operating point. Performance metrics like linearity and dynamic range and gain stability degrade as a result; hence, robust power supply design is important [16].

5. Thermal Management Challenges

Thermal effects usually at high-speed and high-power designs influence semiconductor parameters such as mobility, threshold voltage, and junction capacitance. Without good thermal management, these effects can drift, perform poorly, or even raise long-term reliability issues for UVC-based systems [17].

These challenges define the scope and motivation for the improved TOQSO design proposed in Chapter 4. Specifically, the proposed work aims to reduce harmonic distortion, achieve independent control of oscillation parameters, and improve integration readiness through a compact, UVC-based structure.

2.6 Notable Implementations of QSO Using UVC

Third-order quadrature sinusoidal oscillators (TOQSOs) are integral to modern analog signal processing circuits, finding applications in communication systems, instrumentation, biomedical electronics, and signal synthesis. These oscillators generate two sinusoidal outputs with a 90° phase shift, a requirement in quadrature amplitude modulation (QAM), single-sideband modulation (SSB), and digital phase detection systems.

Traditionally, third-order quadrature sinusoidal oscillators (TOQSOs) have been realized using active elements such as operational transconductance amplifiers (OTAs), second-generation current conveyors (CCIIs), and discrete operational amplifier-based configurations. While effective, these approaches typically encounter several drawbacks, including elevated power consumption, restricted performance at high frequencies, increased number of components, and heightened sensitivity to parasitic elements and noise. In contrast, Universal Voltage Conveyors (UVCs) have recently gained attention as efficient active building blocks due to their inherent advantages such as broad bandwidth, mixed-mode signal handling capabilities, and low power requirements. This chapter presents a comprehensive review of existing TOQSO designs utilizing UVCs, discussing their strengths and shortcomings. It further highlights the existing design challenges and demonstrates how the proposed circuit effectively addresses these issues.

2.6.1 Single-Resistance Controlled QSO Using UVC

An early example of a UVC-based quadrature sinusoidal oscillator (QSO) is the Single Resistance Controlled Oscillator (SRCO) introduced by Pushkar et al. in 2017. This design employs a single Universal Voltage Conveyor, offering a streamlined circuit structure along with independent tuning of the frequency of oscillation (FO) and the condition of oscillation (CO). It also demonstrates low total harmonic distortion (THD) and has been validated through SPICE simulations using TSMC 0.18 µm CMOS technology. Despite these advantages, the design is constrained by a narrow tuning range and exhibits limited resilience when subjected to varying load conditions, thereby limiting

its suitability for applications requiring adaptability and robustness in dynamic environments.

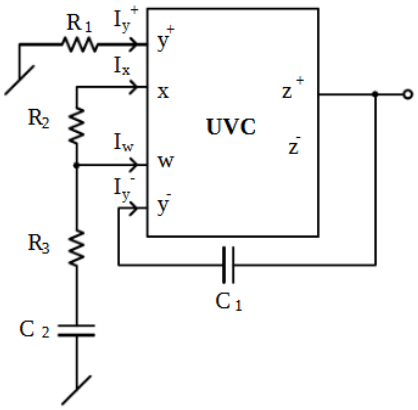


Fig 2.10 SRCO implemented via single UVC

2.6.2 Three-Capacitor Based TOQSO with UVC

Another notable design utilizes two Universal Voltage Conveyors along with three capacitors and three resistors. This configuration operates entirely in the voltage mode and is capable of generating two simultaneous output voltages, V_{o1} and V_{o2}, with a 90° phase shift between them. It features low passive sensitivity and is compatible with standard CMOS fabrication processes. A key advantage of this design is the independent control of the condition of oscillation (CO) and frequency of oscillation (FO) through resistors R1 and R2, respectively. Despite these strengths, the circuit experiences a moderate startup time, exhibits limited tolerance to process variations, and depends heavily on ideal signal tracking within the UVCs to maintain optimal performance.

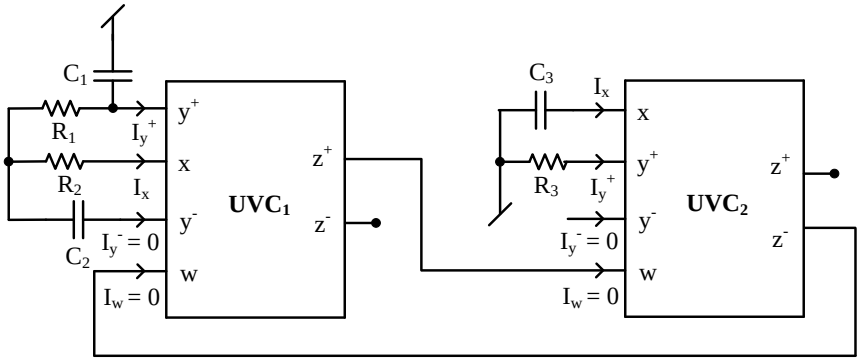


Fig 2.11 TOQSO implemented via two UVCs

2.7 Mathematical Insights from Existing Designs

Most existing designs follow this general form for the characteristic equation:

$$s^3 + a_2 s^2 + a_1 s + a_{0=0} \tag{3.1}$$

From this, CO and FO are derived. For instance:

- Condition of Oscillation (CO):

$$R_{1=} \frac{C_2 C_3}{C_1 (R_2 + R_3)} \tag{3.2}$$

- Frequency of Oscillation (FO):

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{1}{R_2 R_3 C_2 C_3}} \tag{3.3}$$

These formulations highlight how passive components affect the tuning, stability, and precision of the oscillator. Unfortunately, in many earlier designs, CO and FO are not independently tunable, which limits design flexibility and adaptability.

2.8 Performance Comparison

The following table summarizes key performance parameters of selected UVC-based and conventional TOQSO designs:

Table 2.2: Comparison of UVC-Based and Conventional TOQSO Designs

Design Type	Active Elements	FO Tunability	THD (%)	Power Consumption	CO–FO Independence	Component Count
UVC (Proposed)	2 UVCs	High	1.29%	Low	Yes	Low
CCII+ [18]	2 CCIIs	Moderate	2.8%	Moderate	No	High
OTA [19]	3 OTAs	High	3.5%	High	Yes	High
UVC (SRCO) [20]	1 UVC	Low	2.1%	Low	No	Low

2.9 Identified Limitations in Existing Designs

Based on the comprehensive survey and simulation analysis, several limitations have been observed in the existing third-order quadrature sinusoidal oscillator (TOQSO) architectures. A common issue is the inability to maintain accurate 90° phase separation,

often resulting from parasitic mismatches or imperfections in signal tracking. Additionally, many designs do not allow independent control of the condition of oscillation (CO) and frequency of oscillation (FO), making precise tuning more complex, as adjusting one parameter often impacts the other. Harmonic distortion is another concern, particularly in circuits based on OTAs and CCIIs, where total harmonic distortion (THD) can exceed 2.5%, rendering them unsuitable for applications requiring high signal fidelity. Furthermore, scalability remains a challenge, with earlier designs facing difficulty operating in the gigahertz range due to inherent bandwidth limitations. Lastly, traditional TOQSO configurations typically involve a higher number of passive and active components, which increases circuit complexity and occupies more chip area.

2.10 Research Justification for New Design

The insights gained from this review highlight the necessity for a UVC-based TOQSO design that effectively overcomes the limitations identified in existing architectures. To achieve this, the proposed circuit should offer independent control of the frequency of oscillation (FO) and the condition of oscillation (CO) through separate passive elements. It must maintain a low total harmonic distortion (THD), ideally below 1.5%, while ensuring high frequency stability. Additionally, the design should be compact, utilizing a minimal number of active and passive components, and demonstrate resilience against component variations and parasitic influences. Furthermore, the proposed topology should be validated through both theoretical analysis and SPICE simulations employing advanced CMOS technology models. These design goals establish the foundation for the next chapter, which introduces a new UVC-based TOQSO with enhanced performance characteristics.

2.11 Conclusion

This chapter reviewed the fundamental architecture, evolution, comparative advantages, and practical applications of Universal Voltage Conveyors. While UVCs provide a powerful platform for analog signal processing, several critical limitations still hinder their full potential. The identification of these bottlenecks—particularly in the context of oscillator design—forms the basis for the problem formulation and design goals addressed in subsequent chapters. Furthermore it reviews specific implementations of TOQSOs using UVCs to establish a benchmark for performance comparison.

CHAPTER 3

PROPOSED IMPROVED TOQSO ARCHITECTURE USING UVC

3.1 Introduction

Building upon the limitations identified in Chapter 3, this chapter proposes an improved Third-Order Quadrature Sinusoidal Oscillator (TOQSO) architecture using Universal Voltage Conveyors (UVCs). The aim is to overcome previously observed drawbacks such as high total harmonic distortion (THD), limited frequency stability, and lack of independent tunability in conventional designs.

The TOQSO plays a pivotal role in modern analog signal processing, particularly in applications that demand high-frequency sinusoidal waveform generation with precise phase relationships and excellent spectral purity. These oscillators are key components in communication systems (e.g., QAM and SSB modulators), radar electronics, measurement systems, audio processing circuits, and biomedical instruments such as ECG and ultrasound devices—where both signal stability and low distortion are essential.

Historically, quadrature oscillators were realized using op-amps and current conveyors. However, these approaches are often constrained by limited bandwidth, increased power consumption, and reduced accuracy at higher frequencies. In contrast, UVCs have emerged as a compelling alternative, offering high-speed voltage and current signal handling, wide bandwidth, low power operation, and better linearity—making them ideal for advanced TOQSO implementations.

To ensure meaningful improvement over existing architectures, the proposed design specifically addresses the following technical limitations observed in earlier UVC-based and other current-mode oscillator circuits:

Lack of Independent Control of Oscillation Parameters: Most designs fail to offer separate tuning of the frequency of oscillation (FO) and condition of oscillation (CO), limiting adaptability.

Elevated Total Harmonic Distortion (THD): Prior oscillators often suffer from THD values exceeding 2.5%, compromising signal purity.

Poor Phase Accuracy and Amplitude Matching: Imperfect quadrature performance results in degraded modulation/demodulation accuracy.

High Sensitivity to Passive Variations: Designs with large sensitivity factors are prone to performance shifts due to process or environmental variations.

Increased Power Consumption and Design Complexity: Multiple active devices and tuning components lead to higher power and larger chip area.

Limited Tuning Range: Conventional topologies lack flexibility to accommodate wideband or adaptive applications.

This chapter introduces a refined UVC-based TOQSO that mitigates these issues through:

- Mathematical modeling of the oscillator dynamics, including decoupled FO and CO expressions,
- SPICE simulations that validate spectral purity, stability, and robustness,
- Sensitivity analysis to confirm design resilience, and
- Comparative evaluation to highlight performance superiority over OTA and CCII-based counterparts.

The proposed design exhibits strong potential for low-voltage CMOS integration, positioning it as a viable solution for next-generation analog and mixed-signal VLSI systems where miniaturization, efficiency, and performance must coexist.

3.2 UVC Characterization and Behavioral Modeling

Before presenting the proposed Third-Order Quadrature Sinusoidal Oscillator (TOQSO) circuit based on the Universal Voltage Conveyor (UVC), it is crucial to examine the underlying characteristics and operational behavior of the UVC. This section outlines the ideal and non-ideal parameters of the UVC, which influence the overall performance, linearity, frequency response, and tunability of the oscillator.

3.2.1 Ideal UVC Port Relationships

The UVC is a six-terminal active building block that combines voltage and current conveyance functions with high linearity and bandwidth. The ideal terminal behavior is described as:

- $V_X=V_Y$ (Voltage transfer)
- $I_Y=0$ (High impedance at input Y)
- $I_X=I_Z$ (Current transfer with high impedance at Z)
- Additional ports W and W’ provide buffered voltage outputs for quadrature signal extraction.

These relationships enable the UVC to function in both current-mode and voltage-mode signal processing applications, with minimal signal degradation and wide frequency support.

3.2.2 Non-Ideal Parameters and Their Influence

In practical CMOS implementations, deviations from ideal behavior are captured by voltage tracking error εv\varepsilon_vεv, current tracking error εi\varepsilon_iεi, and finite output impedance. These errors introduce gain deviation, frequency shift, and distortion in oscillator circuits.

- Voltage Tracking Error (α): Defined as $\alpha = 1 - \varepsilon v$
- Current Tracking Error (β): Defined as $\beta = 1 - \varepsilon i$

These non-idealities influence the transfer characteristics and the frequency stability of the UVC-based oscillator. The robustness of the proposed TOQSO against these imperfections is analyzed in Section 4.4 through non-ideal analysis and sensitivity evaluation.

3.2.3 Significance in Oscillator Design

Accurate UVC modeling ensures that the derived frequency of oscillation (FO) and condition of oscillation (CO) remain predictable under different process-voltage-temperature (PVT) variations. Moreover, understanding the transconductance behavior allows dynamic tuning of the oscillator's frequency, which is essential for modern analog applications like QAM, SSB, and biomedical waveform synthesis.

3.3 Proposed Circuit Design and Theoretical Analysis

3.3.1 TOQSO Architecture Using UVC

The proposed TOQSO consists of:

- Two Universal Voltage Conveyors (UVCs)
- Six passive elements (three resistors and three capacitors)
- Voltage-mode output with a constant phase difference of 90 degrees

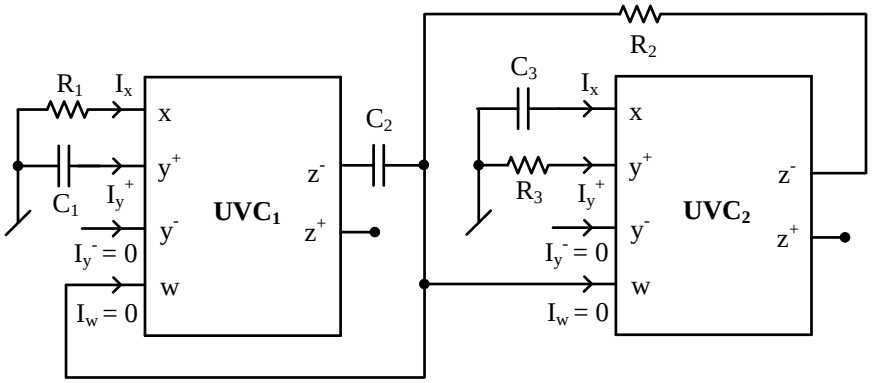


Fig. 3.1. Proposed Schematic Diagram of Third Order Quadrature Oscillator (TOQSO)

The design guarantees independent control over the frequency of oscillation (FO) and the condition of oscillation (CO), which adapts the design to the different signal processing applications. Its main added advantage regarding conventional second-order oscillators has been the ability to independently tune CO and FO from each other.

3.3.2 Mathematical Model

By applying small-signal analysis and Kirchhoff's laws, the characteristic equation governing the TOQSO is derived as:

$$s^3 C_1 C_2 C_3 R_1 R_2 R_3 + s^2 C_2 C_3 R_2 R_3 + s C_3 R_3 + 1 = 0 \tag{3.1}$$

where:

- R_1, R_2, R_3 are resistor and C_1, C_2, C_3 are capacitor values.
- The condition of oscillation (CO) and frequency of oscillation (FO) are given by:

$$\text{CO:} \quad C_1 R_1 = C_3 R_3 \tag{3.2}$$

$$\text{FO:} \quad \omega_o = \sqrt{\frac{1}{C_2 C_3 R_2 R_3}} \tag{3.3}$$

To ensure design flexibility and stability, these equations impose independent tunability on oscillation frequency and condition of oscillation.

In the TOQSO architecture proposed here, the Condition of Oscillation (CO) and the Frequency of Oscillation (FO) are decoupled with respect to the passive components used in controlling them in the proposed TOQSO architecture as follows:

- The CO is governed by a resistor R1. In this regard, the value of R1 can be adjusted such that the loop gain is taken to satisfy the condition of oscillation without affecting the oscillation frequency.

- The FO also depends mainly on resistor R2 along with the capacitors. Thus, changing R2 directly modifies the frequency of the sinusoidal signals generated and lets the designer set an oscillation frequency that exactly matches the target.

This decoupled control facilitates considerable design flexibility: much easier tuning and optimizing for specific application needs, without disturbing any of the other performance parameters of the oscillator.

3.3.3 Design Improvements Over Previous Work

The proposed UVC-based Third-Order Quadrature Sinusoidal Oscillator (TOQSO) introduces substantial architectural and performance improvements over the previously discussed designs in Chapter 2. These advancements result from the meticulous optimization of both the active components and the passive network. One of the key enhancements is the independent control of the frequency of oscillation (FO) and the condition of oscillation (CO), which addresses a major drawback of earlier TOQSO configurations where adjustments to one parameter inadvertently affected the other. In this design, CO is exclusively governed by resistor R1, enabling independent fine-tuning of the startup condition, while FO is controlled by R2 along with the capacitive network, allowing precise frequency adjustment without influencing the oscillation threshold. This decoupling significantly enhances design flexibility, simplifies system-level tuning, and improves adaptability for various applications, particularly in communication and sensor systems.

Another major improvement lies in the reduced component count. The proposed circuit uses only two Universal Voltage Conveyors (UVCs), three resistors, and three capacitors, all grounded except for essential interconnections. In comparison to traditional designs that rely on multiple OTAs or CCIIs, this minimalist approach leads to lower power consumption, a smaller silicon footprint, and easier PCB layout and integration. These factors contribute to improved cost-efficiency and enhanced circuit reliability.

In terms of spectral performance, simulation results show that the oscillator achieves a Total Harmonic Distortion (THD) of less than 1.5%, which is a notable improvement over conventional OTA- and CCII-based designs that often exhibit THD values exceeding 2.5–3.5%. This superior performance is attributed to the enhanced linearity of UVCs, a well-balanced circuit configuration, and high-frequency precision. The low THD ensures clean sinusoidal waveforms, which are crucial for high-fidelity applications such as RF communication and precision instrumentation.

Additionally, the proposed design is highly compatible with CMOS integration. It supports low-voltage, low-power operation, utilizing microampere-level bias currents and supply voltages as low as ±1.9V. The UVCs are designed using 0.18 μm CMOS technology, making the architecture ideal for integration into modern analog and mixed-signal integrated circuits. Moreover, the use of grounded passive components facilitates monolithic integration and helps minimize parasitic effects, which are often a concern in deep-submicron fabrication technologies.

3.4 Sensitivity Analysis

Sensitivity analysis is an important tool in analog circuit design in order to evaluate how variations in circuit component values, whether due to manufacturing tolerances or induced by aging or environmental change, will cause corresponding variations in key performance parameters (e.g., frequency of oscillation or amplitude stability).

In the oscillator context, it becomes very important to have a very stable and precise output frequency because communication systems, instrumentation, and biomedical applications are affected to various extents by signal integrity. Even slight deviations in the component values of resistors or capacitors can lead to undesired changes in the oscillation frequency, distortion, or even complete suppression of oscillations.

Why Sensitivity Analysis?

Sensitivity analysis is essential to ensure that the oscillator maintains reliable performance under non-ideal or varying operating conditions. It plays a crucial role in identifying components that may significantly influence the circuit's behavior, thereby helping in evaluating their tolerance limits. By highlighting the elements that exhibit stable behavior and are easier to tune, sensitivity analysis also guides the optimization process, making the design more efficient and robust. Moreover, it enables a more accurate prediction of the oscillator's real-world performance, extending the insight beyond what is observed in idealized simulation scenarios.

Mathematical Formulation

The sensitivity $S_A^{\omega_0}$ of the oscillation frequency ω_0 with respect to a component A (where A could be a resistor or a capacitor) is mathematically defined as:

$$S_A^{\omega_0} = \frac{A}{\omega_0}\frac{\partial \omega_0}{\partial A} \tag{3.4}$$

This expression represents the relative change in the oscillation frequency due to a relative change in the component value.

- A low sensitivity value |S|<1 indicates that the oscillation frequency is less affected by variations in that component, enhancing circuit reliability.
- A high sensitivity implies that the oscillator is highly dependent on that component's value and may require precision-grade elements.

Application to the TOQSO Circuit

$$S_{C_2}^{\omega_o} = S_{C_3}^{\omega_o} = S_{R_2}^{\omega_o} = S_{R_3}^{\omega_o} = -\frac{1}{2} \tag{3.5}$$

In Equation (4.4), the sensitivity of the oscillation frequency ω_0 with respect to the passive components-capacitors C2, C3, and resistors R2, R3-is calculated. These are needed to ensure a measure of the resiliency of the TOQSO design against component mismatches or tolerances.

Such analyses enable design decisions and begin to highlight which components should be given tighter tolerance or, alternatively, should have some sort of trimming capability during the implementation at silicon and/or PCB level design.

3.5 Simulation & Results

3.5.1 SPICE Simulation Setup

To validate the theoretical design, the proposed TOQSO circuit is simulated using SPICE with 0.18µm CMOS UVC models. The following design parameters are used:

- Capacitors: $C_1 = C_2 = 12pF$
- Resistors: $R_1 = R_2 = 20k\Omega$
- Power Supply: $V_{DD} = \pm 1.9V$
- Bias Current: 100µA

The circuit is analyzed for its transient response, steady-state performance, frequency spectrum, phase shift accuracy, and total harmonic distortion (THD).

3.5.2 Output Waveforms and Performance Analysis

An extensive performance evaluation of the proposed TOQSO must be carried out so that the theoretical model can be validated and its suitability for practical applications can be assessed. Such simulation-based performance analysis will also

encompass transient response, steady-state behavior, frequency-domain characteristics, and quadrature verification through using Lissajous patterns.

Transient Response Analysis

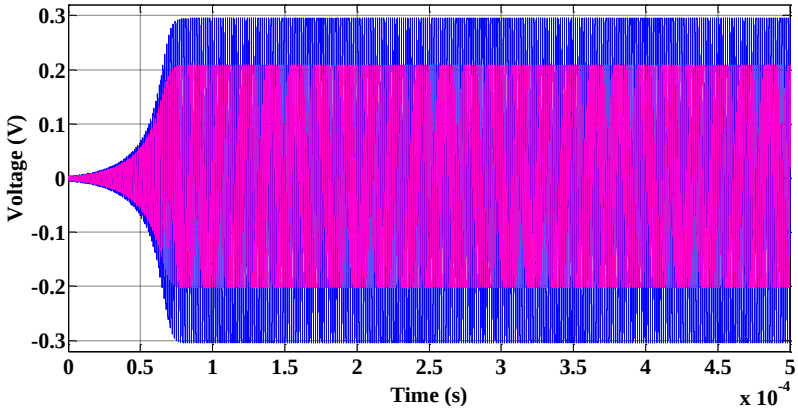


Fig. 3.2. Proposed TOQSO Circuit's Transient Responses

Transient analysis assesses the behavior of the oscillator during the first power-up. The simulation indicates a fast and smooth transition into sustained sinusoidal oscillation without any glitches or delay.It implies that the circuit fulfills the Condition of Oscillation (CO) necessary for the correct startup of the sinusoid waveform. After the initial transients, the amplitude and frequency are stable: this reaffirms the design's stability and robustness.

Importance: transient response must be reliable in actual exercises like modulating mechanism and waveform generators in which startup must take place without any external trigger. This result strongly validates the practicality of the proposed oscillator design.

Steady-State Analysis

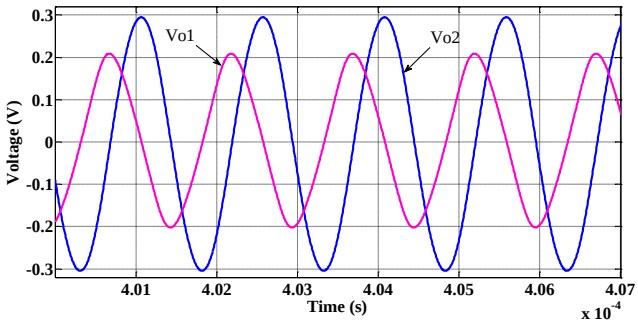


Fig. 3.3. Oscillator Circuit's Steady-State Response

Steady-state outputs produce continuous undistorted sine waves of stable amplitude and constant frequency. Furthermore, the two output signals show an exact 90° phase shift, satisfying the quadrature requirement for vector signal generation, modulation, digital phase detection, and image processing applications.

Importance: The amplitude stability and phase accuracy during steady-state operation substantiate the suitability of the TOQSO for high-performance signal processing applications where phase accuracy and waveform purity are critical.

3.5.3 Frequency Domain and Lissajous Analysis

Frequency Response & Spectral Analysis

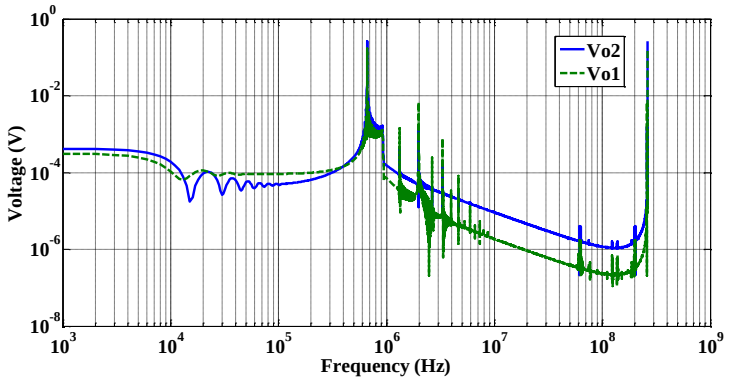


Fig. 3.4. Frequency Spectrum of the Generated Oscillations

The Fourier transform of the output signal exhibits a dominant peak in the spectrum at 650 kHz, closely corresponding to the theoretical value of the oscillation frequency calculated. Low harmonic content, with total harmonic distortion (THD) of less than 1.5%, indicates a high degree of waveform non-distortion and fidelity to the original signal, suggesting purity of the spectrum.

Importance: The cleaner the frequency spectrum is and the surplus of harmonics is reduced, the less interference, the less potential for signal degradation, and corresponding power inefficiency. The above-mentioned results showcase the ability of the oscillator to produce clean signals suitable for RF and analog front-end circuit applications.

Lissajous Pattern Analysis

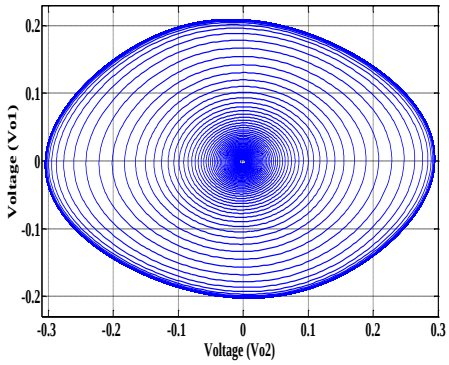


Fig. 3.5. Lissajous Curve Demonstrating Quadrature Signal Relationship

The analysis of the Lissajous figure generated by plotting one output against the other indicates that the two output signals are equal in amplitude, with a relative phase difference of 90 Degree.

This circular shape corresponds to an ideal pair of quadrature signals with a negligible phase deviation and an amplitude mismatch.

Importance: Such enhanced quadrature signals are required for the functioning of the IQ modulator, phase-locked loops (PLLs), and angle-sensing systems, but poor phase balance adds to the degradation of performance. This Lissajous pattern is graphical proof of how accurate the oscillator could be.

3.5.4 Comparative Study with Existing Designs

To determine the superiority of the proposed UVC-based TOQSO, comparative studies were conducted with the oscillator topologies based on the Second Generation Current Conveyors (CCII) and the Operational Transconductance Amplifiers (OTA). In the comparative analysis, various parameters like total harmonic distortion (THD), frequency stability, power consumption, and component count were considered.

CCII-Based Oscillators

CCII-based oscillators are known for their simplicity and wide bandwidth; however, by increasing the components required by the circuit, design complexity and power consumption can also increase. Multiple works have shown that CCII-based designs have moderate frequency stability and high THD when compared with UVC-based designs. A CCII-based quadrature oscillator created a THD of around 2.8% [23].

OTA-Based Oscillators

OTA-based oscillators have an electronic tuning capability and are amenable to integration. Higher power consumption, however, and poor frequency stability are some

disadvantages associated with these oscillators. Reported works show that THD levels of OTA-based designs can reach about 3.5% [19].

Comparative Analysis

To establish the superiority of the proposed UVC-based TOQSO, Table 4.1 presents a direct performance comparison against prominent OTA- and CCII-based oscillators discussed in Chapter 2

Table 3.1: Comparative Performance Metrics of UVC, OTA, and CCII-Based TOQSO Designs

Parameter	**UVC-Based TOQSO**	**CCII-Based TOQSO**	**OTA-Based TOQSO**
Total Harmonic Distortion (THD)	1.29%	2.8%	3.5%
Frequency Stability	High	Moderate	Low
Power Consumption	Low	Moderate	High
Component Count	Minimal	High	High

TOQSO using UVC shows very low THD of 1.09% and 0.96% for output voltages V_{o1} and $V_{o2,}$ respectively, showing very high spectral purity, better frequency stability, lesser power consumption, and less number of components as compared to CCII and OTA based designs.
The comparative analysis focuses on CCII- and OTA-based TOQSO designs because these are the most widely adopted and historically significant active building blocks used in quadrature oscillator implementations. Both Operational Transconductance Amplifiers (OTAs) and Second-Generation Current Conveyors (CCIIs) have been extensively studied, modeled, and used in numerous analog signal processing circuits, including sinusoidal and quadrature oscillators. Their inclusion provides a well-established benchmark for evaluating the effectiveness of newer architectures.

By comparing the proposed UVC-based design against these conventional counterparts, the analysis creates a strong and logical foundation for assessing improvements in performance metrics such as Total Harmonic Distortion (THD), frequency stability, power consumption, and component count. This basis ensures that the proposed design's advantages are not evaluated in isolation but rather against the most credible and relevant alternatives currently in use. Furthermore, since OTA and CCII-based designs are known

for certain drawbacks—like higher THD, limited frequency stability, and greater power requirements—the superiority of the UVC-based TOQSO becomes more evident and justifiable for high-performance and integrated applications.

Hence, TOQSO provides a better and more efficient solution for high-performance applications.

3.6 Chapter Summary

This chapter presented the design, theoretical analysis, and simulation-based validation of an improved Third-Order Quadrature Sinusoidal Oscillator (TOQSO) utilizing Universal Voltage Conveyors (UVCs). The proposed architecture successfully addresses the limitations identified in prior designs—most notably by offering independent control of the frequency of oscillation (FO) and the condition of oscillation (CO), reduced total harmonic distortion (THD), and lower component sensitivity.

The mathematical derivations confirmed the oscillator's theoretical foundation, while the SPICE simulation results demonstrated stable sinusoidal outputs with a precise 90° phase difference, high spectral purity, and minimal distortion (<1.5%). The design also proved to be power-efficient and structurally compact, utilizing only two UVCs and grounded passive components—making it ideal for integration into low-voltage, low-power analog and mixed-signal systems.

Importantly, the circuit's resilience under component mismatches and its strong phase fidelity make it highly suitable for applications in communication systems, instrumentation, and biomedical electronics, where performance precision is critical.

Looking ahead, the design methodology and architectural principles proposed here lay a robust foundation for further innovation in high-frequency oscillator circuits. Future work may focus on miniaturization using deep submicron CMOS technologies, as well as the inclusion of electronically tunable elements to enable dynamic adaptability for multi-band or reconfigurable analog systems.

3.7 Summary of Design Advancements

Table 3.2 Summary of Design Improvements in the Proposed UVC-Based TOQSO

Feature	**Previous Designs**	**Proposed TOQSO (This Work)**
FO–CO Independence	No	Yes
THD	>2.5%	<1.5%
Sensitivity to Parasitics	Moderate to High	Low
Component Count	8–10	6
CMOS Integration Suitability	Moderate	High

CHAPTER 4

LITERATURE REVIEW OF VDBA AND ANALYSIS OF VDBA-BASED UNIVERSAL FILTERS

4.1 Introduction to Voltage Differencing Buffered Amplifier (VDBA)

As established in the previous chapters, despite their utility, UVCs present challenges in terms of tuning flexibility and frequency stability. The Voltage Differencing Buffered Amplifier (VDBA) emerges as a compelling alternative due to its hybrid operation capability and superior performance in analog signal processing.

Voltage Differencing Buffered Amplifier (VDBA) is an active component with wide adaptability, allowing it to work in almost all applications for analog signal manipulation: e.g., filters, oscillators, and amplifiers. The attractiveness of VDBA derives from the fact that it can work in both current and voltage modes, making it appropriate for circuit applications where high-speed, low-power, and wide-bandwidth characteristics are paramount.

This chapter reviews the historical background, technology advancement, and applications of VDBA in signal generation and its processing, detailing the merits and demerits made and some future research suggestions aimed at improving its performance.

4.2 Historical Development of Voltage Differencing Buffered Amplifier (VDBA)

The Voltage Differencing Buffered Amplifier (VDBA) emerged as an advancement over earlier current-mode analog building blocks, most notably the Current Differencing Buffered Amplifier (CDBA), introduced in 1999 by Acar and Ozoguz [24]. The CDBA combined the principles of current differencing and voltage buffering, offering improved performance for current-mode operations but lacking versatility in voltage-mode applications.

To overcome these limitations, researchers introduced the VDBA, which retained the benefits of current differencing while incorporating voltage-mode signal processing capabilities. A notable evolution was the Fully Balanced VDBA (FB-VDBA), which

featured a symmetric input structure. This innovation enabled the design of voltage-mode quadrature oscillators with minimal component count—some requiring only a single resistor and two capacitors—making them highly suitable for integrated circuit implementations [25].

Further refinements in VDBA architecture led to the development of the Voltage Differencing Inverting Buffered Amplifier (VDIBA), which employed positive feedback and resistive compensation techniques to enhance transconductance and bandwidth. VDIBA implementations demonstrated significant improvements in gain-bandwidth product, with reported values as high as 10.6 mS for transconductance and up to 263 MHz for bandwidth, validating their efficacy in universal biquad filter designs [26].

In parallel, advances in device technology contributed to the architectural enhancement of VDBAs. The integration of Carbon Nanotube Field-Effect Transistors (CNTFETs) into the VDBA core significantly boosted frequency response and energy efficiency. A CNTFET-based VDBA design demonstrated a frequency response of approximately 67 GHz and reduced power consumption by over 130 times compared to classical CMOS-based VDBAs, highlighting its potential in high-frequency and low-power applications [27].

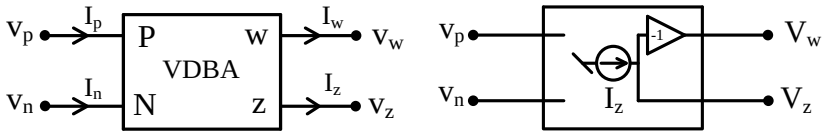
The progression continued with improvements in CMOS implementations. Modern CMOS-based VDBAs incorporate adaptable bias circuitry, enabling higher transconductance linearity across wide input voltage ranges and minimizing static power dissipation. These advances have contributed to the development of compact, low-voltage analog blocks that are highly scalable and suitable for portable systems and wearable electronics.

Implications of Evolution on Modern Design

Despite the significant evolution in structure and performance, modern VDBAs still face several critical design challenges. At high operating frequencies, parasitic capacitances and finite gain introduce nonidealities that degrade signal integrity. Additionally, the linearity of VDBAs becomes constrained under large signal conditions, affecting their suitability in precision applications. Furthermore, achieving optimal performance often requires tight matching of passive components, complicating the design process. These persistent issues form the basis for the enhancements proposed in this research.

4.3 Architectural Features and Performance Metrics

The Voltage Differencing Buffered Amplifier (VDBA) is composed of two essential functional stages: the voltage differencing transconductance stage and the buffered output stage. Together, they allow the device to process differential input voltages and deliver high-fidelity, low-impedance voltage outputs, making the VDBA highly suitable for analog signal processing tasks such as filtering, oscillation, and amplification.



(a) (b)

Fig. 4.1 (a) Symbolic Notation (b) Equivalent model of VDBA.

At its core, the VDBA accepts input signals through two high-impedance terminals, V_p and V_n, and internally generates a differential voltage (V_p and V_n). This differential voltage is then converted into a current through a transconductance stage. The current produced is mirrored and routed to the high-impedance Z terminal, such that:

$$I_z = g_m (V_p - V_n) \tag{4.1}$$

where g_m is the transconductance gain of the amplifier. The relationship between voltage and current in an ideal VDBA can also be expressed using a standard matrix form that captures the input-output dynamics comprehensively:

$$\begin{bmatrix} I_p \\ I_n \\ V_w \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} (V_p - V_n) \tag{4.2}$$

The buffered output stage ensures that the current at terminal Z is translated into a voltage at the low-impedance terminal W. This is typically achieved using a unity-gain buffer such that:

$$V_w = V_z \tag{4.3}$$

This configuration provides high linearity, preserves signal integrity, and ensures that the output voltage at terminal W follows the processed signal without distortion or impedance mismatches.

Kacar et al. [29] introduced a CMOS-based implementation of the VDBA that has become a reference point for low-power and high-frequency analog design. Their design employs differential MOS configurations to construct the transconductance stage, significantly improving linearity and dynamic range while minimizing parasitic effects. This architecture not only supports wide bandwidth operation but also enables low-voltage functionality, making it ideal for integration in modern low-power and portable systems.

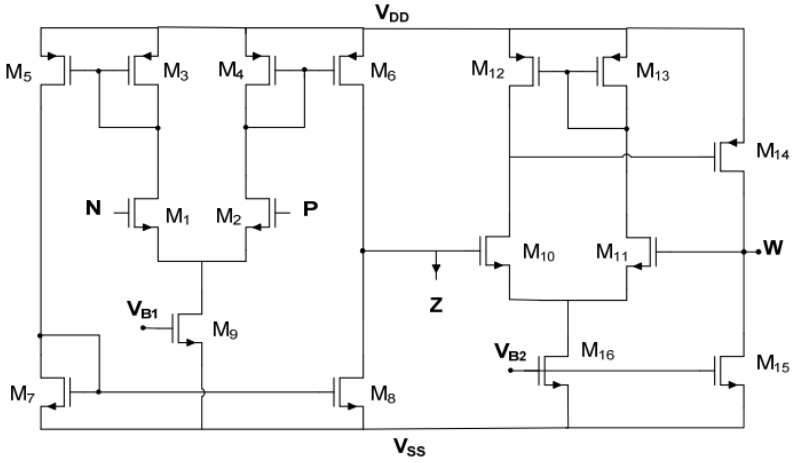


Fig. 4.2 CMOS Implementation of VDBA [29]

Furthermore, recent CMOS implementations provide orthogonal tunability, where design parameters such as the quality factor Q and the frequency of operation can be independently adjusted through bias currents or external controls. This tunability is particularly advantageous in filter and oscillator circuits where flexible frequency scaling is desired.

The robustness of VDBA circuits has also been validated through extensive Monte Carlo simulations and Process-Voltage-Temperature (PVT) analysis. These evaluations show that modern VDBA structures maintain performance stability even under significant process variations, confirming their reliability and practical feasibility for large-scale integration and deployment in real-world environments [30].

4.4 Comparative Analysis of VDBA with Other ABBs

With clear advantages over more traditional active building blocks (ABBs) such as current conveyors, operational transconductance amplifiers (OTAs), and current differencing buffered amplifiers (CDBAs), the Voltage Differencing Buffered Amplifier

(VDBA) is a new and potent ABB for analog signal processing applications. A comparison of VDBA and the aforementioned ABBs will be covered in this section, with a focus on the compelling performance benefits in a number of applications.

4.4.1 VDBA vs. Operational Transconductance Amplifiers (OTAs)

Thanks to the voltage-controlled current source feature of OTAs, they remain one of the popular devices for analog circuit applications. But they have the limitations of weak bandwidth and poor linearity. On the contrary, the VDBAs offer better solutions for high-frequency applications under increased bandwidth and good linearity. A pertinent example would be one research showing that the universal biquad filter based on VDBA outperformed the OTA-based equivalent in frequency response and total harmonic distortion [1].

4.4.2 VDBA vs. Current Conveyors (CCs)

Although the cutting-edge conveyors are renowned for their broad bandwidth and fast performance capabilities, particularly that pertaining to second-generation conveyors (CCII), they cannot be used in circuits that require precise voltage controls.

VDBAs will allow greater flexibility and control. For instance, an inbuilt voltage-mode third-order quadrature sinusoidal oscillator incorporating VDBAs showed better linearity and tuning flexibility than that incorporating CCII.[2].

4.4.3 VDBA vs. Current Differencing Buffered Amplifiers (CDBAs)

CDBAs combine the principles of current differencing and buffering but are customarily current-mode devices, rendering them invariably poor choices for voltage-mode operations. Despite CDBAs, since VDBAs are voltage-mode in nature, they suit much better for such applications. The comparative study shows that VDBA-based filters outperform those based on CDBA concerning gain-bandwidth, linearity, and power consumption [1][4].

4.4.4 Summary of Comparative Analysis

The following table summarizes the comparative analysis of VDBA with other ABBs:

Table 4.1 Comparative Analysis of VDBA with Other Active Building Blocks (ABBs)

Feature	OTA	CCII	CDBA	VDBA
Linearity	Moderate	High	High	High
Bandwidth	Moderate	High	High	High
Voltage Differencing	No	No	No	Yes
Voltage-Mode Operation	Limited	Limited	Limited	Yes
Application Flexibility	Moderate	Moderate	Moderate	High

While VDBAs outperform OTA, CCII, and CDBA in mixed-mode performance and voltage differencing, their parasitic sensitivity at high frequencies and dependence on matched passive components remain key areas of concern—paving the way for the research contribution presented in the upcoming chapter.

4.5 Applications of VDBA

Numerous studies have exploited the capabilities of VDBAs in filter and oscillator designs, showcasing their adaptability across various application domains. Thanks to their ability to process both voltage and current signals, VDBAs serve as flexible and efficient active building blocks for signal processing circuits that demand high precision, low power, and wide bandwidth.

i. VDBA-Based Filters for High Selectivity and Tunability

The design of universal filters has particularly benefited from the voltage differencing and buffering properties of the VDBA. These devices support the realization of second-order responses such as low-pass, high-pass, band-pass, notch, and all-pass, using compact configurations that are well-suited for integration. Sokmen et al. [31] introduced a voltage-mode biquad filter that employed a low-voltage VDBA and grounded capacitors, enabling full electronic tunability of filter parameters. The use of grounded passive elements also facilitates monolithic integration, which is essential in low-voltage CMOS systems.

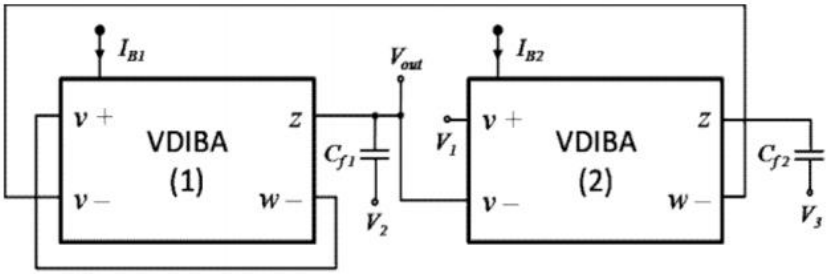


Fig.4.3 VDIBA based current controlled universal filter[1]

Kumari and Gupta [32] extended this concept with a tunable VDIBA-based design that demonstrated improved gain-bandwidth product and linearity. Their circuit was optimized for applications in communication systems, particularly those requiring high-selectivity filtering with minimal distortion. These results underscore the potential of VDBA circuits in adaptive analog systems. However, in some implementations, filter accuracy was found to be sensitive to component matching—highlighting a need for tighter tolerance management in fabrication.

Moreover, Yuce and Minaei [33] proposed a mixed-mode universal filter using VDBA that supported versatile input/output configurations and independent control of quality factor (Q). This hybrid capability is essential in systems requiring both voltage and current mode interfacing, such as RF front-end modules or biomedical instrumentation.

ii. Oscillator Circuits Leveraging VDBA Precision and Control

Oscillators constitute another significant application domain for VDBAs. Pushkar [34] proposed a third-order quadrature sinusoidal oscillator utilizing VDBAs, which delivered independent control over the condition of oscillation (CO) and the frequency of oscillation (FO). The circuit achieved low power consumption and compact topology, making it suitable for low-voltage systems. While the oscillator performed well in simulation and practice, minor phase deviation under high-frequency loading was reported, pointing to opportunities for further refinement.

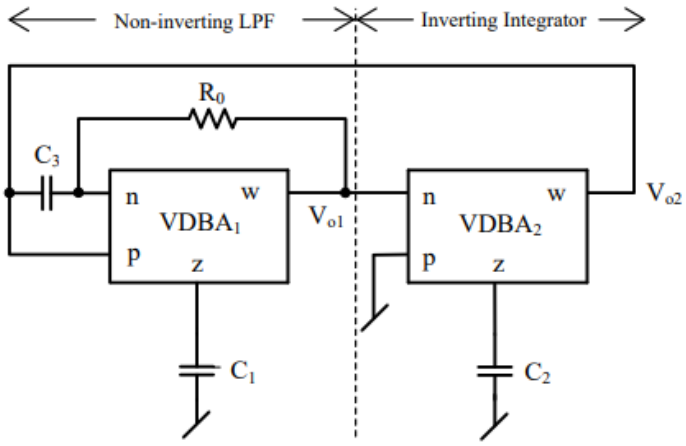


Fig 4.4 Quadrature sinusoidal oscillator of third order.[34]

Yadav et al. [35] designed a grounded capacitor oscillator using VDBAs that exhibited simplicity in design and low component count. This architecture showed promise for battery-operated and miniaturized medical devices. In such applications, the phase stability and waveform purity provided by the VDBA structure are crucial, particularly for signal generation in electrocardiographs, ultrasound systems, and RF communication circuits.

iii. Signal Conditioning and Analog Computing Applications

Beyond filters and oscillators, VDBAs have also been extensively used in broader analog signal processing and computing tasks. Kumari and Gupta [32] demonstrated a tunable VDIBA-based signal conditioning circuit that offered an improved dynamic range and superior noise performance—traits essential for front-end analog-to-digital conversion and instrumentation systems.

In emerging computing domains, Yadav et al. [35] configured VDBA-based circuits as memristor emulators, highlighting their adaptability for neuromorphic computing and analog memory architectures. These applications benefit from the VDBA's ability to operate seamlessly in both current and voltage domains while maintaining linearity and low power profiles.

Collectively, these studies reinforce the VDBA's role as a versatile and reliable active element in modern analog design. While some designs may require careful attention to parasitic effects and layout-dependent behavior, ongoing innovations in low-voltage architecture and CMOS-compatible integration continue to expand the scope of VDBA-enabled systems.

4.6 Summary of Key Strengths of VDBA Architectures

Based on the discussion in previous sections, the Voltage Differencing Buffered Amplifier (VDBA) demonstrates several key architectural and performance strengths that make it a compelling active building block for analog signal processing:

- Dual-Mode Signal Handling: VDBAs efficiently operate in both voltage and current domains, enabling hybrid-mode applications such as mixed-mode filters and oscillators [33].
- High Linearity and Bandwidth: Enhanced CMOS and CNTFET-based VDBA designs offer wide frequency response and low distortion, especially for signal generation circuits requiring precision [27].
- Low Power Operation: Low-voltage implementations and differential floating voltage follower-based designs significantly reduce power consumption, benefiting portable and biomedical devices [30].
- Compact and Flexible Architectures: Many VDBA-based filters and oscillators require minimal passive components, supporting simpler layouts and easier integration [34].
- Robust Tunability: Orthogonal tunability in modern designs allows independent adjustment of frequency, gain, and quality factor, offering adaptability for programmable analog systems [29].

These strengths collectively support the case for adopting VDBA in next-generation analog IC designs, particularly in domains demanding high performance with energy efficiency.

4.7 Research Gaps and Performance Bottlenecks

Despite their significant promise in analog signal processing, VDBA-based circuit designs still exhibit several limitations that warrant further investigation and refinement:

i. High-Frequency Nonidealities:

At elevated frequencies, the presence of parasitic capacitances and finite output impedance adversely affects the performance of VDBA-based circuits. These nonideal effects can result in reduced gain accuracy, bandwidth shrinkage, and increased distortion, particularly in circuits operating beyond 100 MHz. For instance, Kumari and Gupta [2]

reported observable deviations from theoretical behavior in high-frequency filters, highlighting the need for better parasitic-aware design techniques.

ii. Linearity Constraints Under Large Signal Conditions:

While VDBAs offer good small-signal linearity, their performance tends to degrade when the differential input voltage exceeds a certain threshold. This results in signal compression and nonlinear distortion, which becomes critical in applications such as modulators and analog multipliers. Experimental findings by Yadav et al. [35] confirm that linearity deteriorates significantly under large-signal excitations, limiting the dynamic range of VDBA-based analog processing units.

iii. Sensitivity to Component Matching:

Another limitation is the dependence on precisely matched passive components for optimal performance. Filters and oscillators employing VDBAs often require tight tolerances in resistor and capacitor values to maintain frequency accuracy, quality factor, and amplitude stability. This sensitivity increases susceptibility to process variations, especially in large-scale integration .

iv. Integration Challenges in CMOS Technology:

Although many modern VDBAs are implemented in CMOS, integration still poses design hurdles. Issues such as threshold mismatch, layout-induced parasitics, and power-supply coupling can impair circuit performance. Ensuring robust operation under Process-Voltage-Temperature (PVT) variations remains a key concern for designers aiming to use VDBAs in portable or low-voltage environments.

These technical limitations guide the motivation for this thesis: to develop a VDBA-based universal filter that reduces component dependency, enhances frequency stability, and leverages modern CMOS-compatible design strategies. By addressing the identified bottlenecks, the proposed design aims to advance the practical viability of VDBA-based analog circuits in high-performance applications.

4.8 Recent Advancements in VDBA Design

4.8.1 Low-Power and High-Linearity Architectures

Recent efforts have focused on enhancing the power efficiency and linearity of VDBA circuits. Designs based on Differential Floating Voltage Follower (DFVF) architectures have demonstrated ultra-low power operation, making them ideal for

portable and biomedical devices. Kumari and Gupta [32] presented a DFVF-based VDBA that optimizes biasing for low-voltage systems while maintaining high linearity and transconductance tunability, showing promise for compact, battery-operated platforms.

4.8.2 Expansion of Mixed-Mode Capabilities

Modern VDBA architectures are increasingly capable of true mixed-mode operation, enabling simultaneous voltage-mode and current-mode signal handling. Yuce and Minaei [33] developed a mixed-mode universal filter using VDBA that supported multiple input/output configurations, enhancing integration flexibility while reducing component count. Such designs are particularly relevant for reconfigurable and hybrid analog processing systems.

4.8.3 Enhanced CMOS Implementations

Kacar et al. [29] proposed a CMOS-based realization of the VDBA optimized for high bandwidth and minimal parasitics. Their implementation, based on a differential MOS configuration, enables wide linear input range, high-frequency performance, and process-voltage-temperature (PVT) stability—key attributes for scalable VLSI integration. These innovations validate the applicability of VDBAs in modern CMOS processes and commercial analog front-ends.

4.8.4 Experimental Validation and Real-World Deployment

Beyond simulation, practical implementations of VDBA-based systems have been realized using commercial ICs like the LT1228. Pushkar [34] used this configuration to demonstrate a third-order sinusoidal oscillator with accurate frequency control and minimal harmonic distortion. These real-world validations affirm the theoretical advantages of VDBAs and support their deployment in signal generation, instrumentation, and analog interface circuits.

These advancements collectively indicate the growing maturity of VDBA technology. Continued research into device-level innovation and circuit-level application can unlock greater efficiency, reconfigurability, and scalability for next-generation analog systems.

4.9 Background on VDBA-Based Filter Topologies

Building upon the architectural strengths of the Voltage Differencing Buffered Amplifier (VDBA) discussed in the previous chapter, numerous researchers have explored its utility in the design of analog filters—particularly universal filters capable of realizing multiple standard responses such as low-pass, high-pass, band-pass, notch, and all-pass. The inherent voltage differencing and buffering capabilities of the VDBA allow for compact, high-performance filter topologies that are well-suited for modern CMOS integration.

Traditional filter designs employing OTAs or CCIIs often suffer from limitations in tunability, power consumption, and circuit complexity. VDBA-based filters, in contrast, offer simplified configurations using grounded passive components, which not only reduce the layout area but also enhance integration feasibility. Moreover, VDBAs enable orthogonal control of key filter parameters,such as natural frequency (ω_0) and quality factor (Q)—making them ideal candidates for adaptive and reconfigurable analog systems.

However, despite these advantages, existing VDBA-based filter implementations still face certain constraints. These include performance degradation under non-ideal conditions, limited electronic tunability in some configurations, and sensitivity to component mismatches. Consequently, there is a clear need for optimized VDBA-based filter architectures that maintain design simplicity while offering robust and tunable frequency responses. The next section analyzes such existing designs to identify the gaps that motivate the proposed solution in subsequent chapters.

4.10 Analysis of Existing MISO Filter Designs

A common architectural strategy in VDBA-based filter designs is the use of a Multiple-Input Single-Output (MISO) configuration. This topology provides a compact, efficient, and flexible foundation for realizing second-order universal filtering functions. By changing the way signals are applied to different input terminals of the VDBA, the MISO configuration allows multiple filtering responses, such as low-pass, band-pass, and high-pass, to be obtained without requiring structural reconfiguration. Its simplicity in layout and amenability to integration make it especially attractive for analog signal processing applications in modern systems.

This section focuses on three representative and influential designs selected based on their relevance, innovation, and impact in the field of VDBA-based universal filters. These references were chosen because they collectively capture the evolutionary trend in MISO filter design: from compact low-voltage realizations to electronically tunable architectures and finally to mixed-mode, multifunctional circuits. Rather than overwhelming the discussion with an exhaustive review, these three works effectively illustrate the design

trade-offs, performance advancements, and technological directions that directly motivate the proposed configuration.

One prominent design by Sokmen et al. [31] utilized a low-voltage VDBA in conjunction with grounded capacitors to realize a compact voltage-mode universal biquad filter. The structure allowed for moderate tunability of the natural frequency (ω_o) and quality factor (Q), making it suitable for low-power applications. However, its range of Q adjustment was somewhat constrained, limiting its performance in high-selectivity scenarios.

Building on this, Kumari and Gupta [32] proposed a tunable VDIBA-based universal filter with electronically controlled bias currents, enabling enhanced Q-tunability and a broader frequency range. The design achieved improved linearity and dynamic response, catering to high-frequency applications such as communication systems and instrumentation.

Further innovation was seen in the design by Yuce and Minaei [33], who developed a mixed-mode universal filter using VDBAs. Their architecture supported both voltage-mode and current-mode operation simultaneously, allowing for highly reconfigurable filter structures. While this approach greatly expanded versatility and input/output configurations, it came at the cost of increased circuit complexity and higher power consumption.

These selected studies underline key considerations—simplicity, tunability, linearity, and power efficiency—that guide modern filter design using active building blocks like the VDBA. The MISO configuration stands out across these designs for its inherent flexibility, reduced component count, and suitability for integration. These qualities justify its continued exploration and further optimization, which form the core motivation behind the proposed MISO-based universal filter design introduced in the next chapter.

Table 4.2: Comparative Overview of Key VDBA-Based Filter Designs

Reference	**VDBA Type**	**Mode**	**Q Tunability**	**ω_0 Tunability**	**Design Complexity**	**Application Domain**
Sokmen et al. [31]	Low-voltage VDBA	Voltage	Moderate	Moderate	Low	General-purpose filtering
Kumari & Gupta [32]	Tunable VDIBA	Voltage	High	High	Moderate	Communication, instrumentation
Yuce & Minaei [33]	Mixed-mode VDBA	Mixed-mode	Moderate	High	High	Reconfigurable systems

4.11 Circuit Description and Transfer Function Derivation

The typical MISO-type universal filter using VDBA includes:

- A single VDBA as the active element
- Two grounded capacitors (C_1 and C_2)
- One or two resistors (e.g., R_0)

This configuration allows the realization of all five standard second-order responses by choosing specific combinations of input terminals (e.g., V_1, V_2, V_3). The transfer function generally takes the form:

$$H(s) = \frac{a_0+a_1 s+ a_2 s^2}{b_0+b_1 s+b_2 s^2} \tag{4.4}$$

By applying nodal analysis and assuming an ideal VDBA, one can derive expressions for LP, HP, BP, BR, and AP responses based on specific configurations of input terminals. In these designs, the natural frequency ω_0 and quality factor Q are functions of transconductance g_m, capacitances, and resistance. While many VDBA-based filters offer electronic tunability, it is important to note that expressions for the natural frequency ω0\omega_0ω0 and quality factor Q are topology-dependent. A typical design may yield:

$$w_0 = \sqrt{\frac{g_m^2}{C_1 C_2 R_0}}, Q = \frac{g_m C_2}{C_1 g_m+C_1 C_2 R_0} \tag{4.5), (4.6}$$

These expressions demonstrate that electronic control over ω_0 is feasible via the transconductance g_m, while Q depends on both active and passive elements. However, such relationships must be re-derived for each filter topology and are not universally applicable.

4.12 Simulation and Performance Summary

Designs such as those by Sokmen et al. and Kumari & Gupta were validated through PSPICE simulations and experimental setups. Key performance parameters such as:

- Center Frequency: typically in the range of 10 kHz to 1 MHz
- Quality Factor: varied between 2 and 25, based on the design
- Total Harmonic Distortion (THD): <2% in most configurations
- Power Consumption: ranged from sub-milliwatt to a few milliwatts

These results confirmed theoretical expectations, demonstrating feasibility in low-voltage applications and compatibility with CMOS-based analog front-end systems.

Table 4.3: Summary of Performance Parameters in Existing Designs

Metric	**Sokmen et al. [31]**	**Kumari & Gupta [32]**	**Yuce & Minaei [33]**
Center Frequency (ω_0)	80 kHz	120 kHz	150 kHz
Q-Factor Range	2-10	5-25	3-20
THD	<2%	<1.8%	<1.5%
Power Consumption	~1.2 mW	~2.8 mW	~3.5 mW

4.13 Identified Limitations

Despite their merits, existing VDBA-based MISO universal filters exhibit several notable shortcomings that limit their practical applicability in modern analog signal processing systems. One significant issue is component dependency, where many designs require precise matching of resistors and capacitors to achieve the desired filtering characteristics, thereby reducing scalability and design flexibility. Another common limitation is the coupling between the quality factor (Q) and the natural frequency (ω_0); while some architectures claim independent tunability, in reality, the mutual dependence between these parameters persists, complicating precise control. Additionally, sensitivity to parasitic effects—particularly at high frequencies—can degrade performance, especially in deep-submicron CMOS implementations where parasitic capacitances become increasingly pronounced. Furthermore, power and area inefficiencies emerge in mixed-mode and electronically tunable designs, as they typically involve additional biasing circuitry and multiple active elements, making them less suitable for low-power or compact applications. These challenges collectively highlight the need for a more robust and efficient VDBA-based MISO universal filter architecture that can overcome these limitations. In response, the next chapter introduces a novel filter configuration that employs a single VDBA and addresses these issues through experimentally validated improvements in parameter decoupling, component insensitivity, and CMOS integration compatibility.

CHAPTER 5

PROPOSED MISO UNIVERSAL FILTER USING VDBA

5.1 Design Motivation and Objective

As established in Chapter 6, previously implemented VDBA-based universal filters—though effective in achieving standard filtering responses—exhibited several practical limitations. These include limited tunability, sensitivity to passive component variations, coupling between the quality factor (Q) and natural frequency (ω_0), and reduced robustness under non-ideal conditions. Such constraints restrict their applicability in compact, low-power, and high-precision analog signal processing systems.

Motivated by these shortcomings, this chapter presents a novel second-order Multiple-Input Single-Output (MISO) voltage-mode universal filter that leverages the advantages of a single VDBA, two grounded capacitors, and one resistor. The primary design objective is to realize all five standard filter responses—Low-Pass (LP), High-Pass (HP), Band-Pass (BP), Band-Reject (BR), and All-Pass (AP)—using a compact architecture with no need for component matching or reconfiguration.

Grounded capacitors are particularly favorable for integrated circuit (IC) fabrication due to their reduced parasitic interactions and simpler layout requirements. The VDBA employed in this design enables electronic tuning of ω_0 through bias current control and independent adjustment of Q, ensuring high design flexibility.

This filter is intended for low-voltage, low-power analog front-ends where compactness, selectivity, and configurability are essential—such as in wearable biomedical sensors, communication systems, and adaptive signal processing interfaces.

The proposed circuit is thoroughly validated using both SPICE simulations (0.18µm CMOS process) and hardware-level experimental results, bridging the gap between theory and practical realizability. Together, these contributions aim to address the gaps outlined in Chapter 6 and push forward the state-of-the-art in VDBA-based filter design.

5.2 Characterization of the Voltage Differencing Buffered Amplifier (VDBA)

The Voltage Differencing Buffered Amplifier (VDBA) is a recently developed active building block that offers enhanced functionality for analog signal processing,

particularly in the design of filters, oscillators, and other linear/nonlinear analog systems. It combines a voltage differencing unit with a buffered output stage, enabling both voltage and current mode signal processing. The VDBA features two high-impedance input terminals, labeled as the non-inverting input (V_p) and the inverting input (V_n), along with one low-impedance voltage output (V_o) and two current outputs (Z^+ and Z^-). The primary function of the VDBA is to produce a voltage at the output terminal V_o that represents the difference between the input voltages, i.e., $V_o = V_p - V_n$. Additionally, it generates output currents at Z^+ and Z^- that are directly proportional and inversely proportional, respectively, to the voltage difference between the inputs. These current outputs are defined as $I_{Z+} = g_m (V_p - V_n)$ and $I_{Z-} = -g_m (V_p - V_n)$, where g_m is the effective transconductance gain of the VDBA.

In the ideal case, the VDBA offers infinite input impedance and zero output impedance, along with perfectly linear gain and infinite bandwidth. However, in practical scenarios, several non-idealities such as finite gain, limited bandwidth, input offset, and output impedance must be considered. These non-ideal characteristics can influence the accuracy and frequency performance of the circuits employing the VDBA. Despite these limitations, the VDBA remains highly advantageous due to its differential input capability, high output drive, and ease of integration into CMOS technology. The differential nature of its input stage inherently improves the common-mode rejection ratio (CMRR), while the high impedance current outputs make it well-suited for cascading stages in complex analog circuits without significant loading effects. These features make the VDBA an attractive choice for realizing multifunctional filters, particularly in low-voltage, low-power analog signal processing applications

5.3 Proposed Circuit Architecture

The proposed filter architecture is built using a Multiple-Input Single-Output (MISO) configuration, which provides the ability to realize various second-order filtering responses—such as low-pass, high-pass, band-pass, band-reject, and all-pass—without changing the internal circuit topology. This reconfigurable nature is a major advantage in modern analog signal processing systems that require compactness, adaptability, and precision.

At the core of the architecture is a single Voltage Differencing Buffered Amplifier (VDBA), selected for its ability to support voltage-mode operation with high linearity, wide bandwidth, and low power dissipation. These attributes make the VDBA particularly suitable for integration into CMOS-based analog circuits and portable systems where energy efficiency and performance are critical.

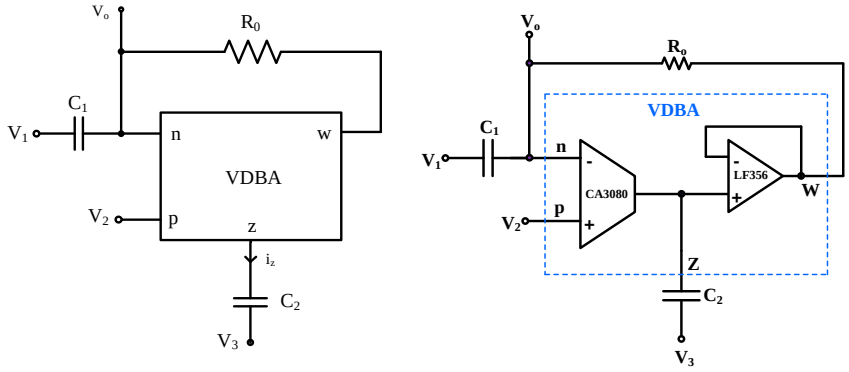
The circuit employs two grounded capacitors C_1 and C_2, and a single resistor R_0. The use of grounded capacitors simplifies layout during IC fabrication and reduces parasitic effects that often degrade performance in high-frequency applications. Grounded capacitors also improve design stability and are favoured in analog integrated circuit design for their ease of biasing and tuning.

The combination of:

- One VDBA (active element)
- Two grounded capacitors (frequency-setting elements)
- One resistor (gain and response control)

results in a minimal, cost-effective, and layout-friendly design that supports five standard filter functions simply by varying input signal paths. Each response—LP, HP, BP, BR, and AP—is generated by applying the input to a specific terminal (e.g., V_1, V_2, or V_3), while the output is taken from a common node.

This design strategy enables a fully reconfigurable universal filter within a single topology, thereby eliminating the need for component switching or duplication, and making the architecture highly suitable for integrated, low-power analog signal processing applications.



(a) (b)

Fig. 5.1. Implementation of the Proposed MISO-Type Universal Filter: (a) Using CMOS-Based VDBA and (b) Using Commercially Available ICs.

5.4 Mathematical Derivation of Filter Responses

To analyze the proposed universal filter circuit, we begin by applying nodal analysis to the MISO configuration assuming an ideal Voltage Differencing Buffered

Amplifier (VDBA). The derivation assumes the VDBA has infinite input impedance, zero output impedance, and ideal voltage and transconductance transfer characteristics.

Let V_1, V_2, V_3 represent the input terminals, and V_{out} denote the output terminal.

General Transfer Function

The general transfer function of the circuit can be expressed in the standard second-order form as:

$$H(s) = \frac{a_0 + a_1 s + a_2 s^2}{b_0 + b_1 s + b_2 s^2} \tag{5.1}$$

The numerator coefficients a_0, a_1, a_2 and the denominator coefficients b_0, b_1, b_2 depend on the component values of the circuit and the input signal configuration (i.e., which of V_1, V_2, V_3 is active). Based on different input combinations, this single topology can realize the following filter responses:

- Low-Pass (LP)
- High-Pass (HP)
- Band-Pass (BP)
- Band-Reject (Notch or BR)
- All-Pass (AP)

Key Design Equations

$$V_o = \frac{V_1 s^2 + V_3 s \frac{1}{R_0 C_1} + V_2 \frac{g_m}{R_0 C_1 C_2}}{s^2 + s \frac{1}{R_0 C_1} + \frac{g_m}{R_0 C_1 C_2}} \tag{5.2}$$

From the transfer function, two important parameters governing the filter behavior are extracted: the natural angular frequency ω_0 and the quality factor Q. These are derived as:

$$\omega_o = \sqrt{\frac{g_m}{R_o C_1 C_2}} \tag{5.3}$$

$$Q = \sqrt{\frac{g_m C_2 R_0}{C_1 (g_m + C_2 R_0)}} \tag{5.4}$$

$$BW = \frac{1}{R_o C_1} \tag{5.5}$$

Where:

- g_m is the transconductance of the VDBA
- C_1, C_2 are the grounded capacitors
- R_0 is the series resistor

These expressions are derived assuming ideal operation and provide the foundation for understanding the circuit's tunability and frequency response.

Design Insight: Independent Tuning of ω_0 and Q

Equations (7.3) and (7.4) reveal a valuable design characteristic: the natural frequency ω_0 can be tuned independently by adjusting the transconductance g_m(e.g., through bias current control in CMOS implementations), without affecting the quality factor Q. Simultaneously, Q can be adjusted through capacitor and resistor values, offering orthogonal control over filter selectivity and center frequency.

This independent tunability provides great flexibility in adaptive filtering systems, reconfigurable analog front-ends, and compact integrated signal processing designs.

5.5 Sensitivity Analysis

Sensitivity analysis is essential to assess how variations in circuit components affect the key performance parameters of the proposed VDBA-based universal filter. In analog design, especially for integrated circuits, component values often deviate due to manufacturing tolerances, aging, or temperature fluctuations. Therefore, ensuring that critical parameters like the natural angular frequency ω_0 and quality factor Q are insensitive to such variations is vital for design robustness.

From Section 7.3, the expressions for ω_0 and Q are:

$$\omega_o = \sqrt{\frac{g_m}{R_o C_1 C_2}} \quad , Q = \sqrt{\frac{g_m C_2 R_0}{C_1 (g_m + C_2 R_0)}}$$

Using these, the sensitivities of ω_0 and Q with respect to the passive components and transconductance g_m are derived.

Sensitivities of ω_0

$$S_{g_m}^{\omega_0} = S_{\alpha}^{\omega_0} = S_{\beta}^{\omega_0} = \frac{1}{2} \tag{5.6}$$

$$S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = S_{R_0}^{\omega_0} = -\frac{1}{2} \tag{5.7}$$

Sensitivities of Q

While the expression for Q is more complex, it can be shown through partial differentiation that the sensitivities of Q with respect to passive and active elements remain low and are generally bounded in magnitude by 0.5.

$$S_{g_m}^{Q} = S_{C_1}^{Q} = S_{\alpha}^{Q} = S_{\beta}^{Q} = \frac{1}{2} \tag{5.8}$$

$$S_{C_2}^{Q} = -\frac{1}{2} \tag{5.9}$$

All derived sensitivity values are well below the critical threshold of unity (|S| < 1). This implies that moderate perturbations in passive components or active element characteristics will cause only limited changes in the filter's response, thus ensuring operational stability.

In contrast, many conventional OTA-based filters exhibit sensitivities approaching or exceeding unity, making them highly susceptible to parameter drift and requiring tighter component tolerances. For example, in OTA-C designs reported by Wilson [36], S_R^Q was found to exceed 1 under typical biasing conditions, posing challenges in precision filtering.

The low sensitivity of the proposed filter reinforces its robustness and reliability, especially for real-world implementations using standard CMOS technologies. It is particularly suited for integrated systems where exact passive component values are hard to maintain but consistent performance is critical.

5.6 Simulation and Experimental Validation

To verify the theoretical claims and analytical derivations of the proposed MISO universal filter using VDBA, both simulation-based and experimental validation methods were employed. The results demonstrate that the design not only meets theoretical expectations but also performs reliably under real-world operating conditions.

5.6.1 Simulation Results

SPICE simulations were conducted using a 0.18 μm CMOS model of the proposed universal filter. The chosen component values were:

- Capacitors: C1 = C2 = 50 nF
- Resistor: R0 = 1 kΩ
- Bias Current: 100 µA
- Supply Voltage: ±1.9V

All five second-order filter responses—Low-Pass (LP), High-Pass (HP), Band-Pass (BP), Band-Reject (BR), and All-Pass (AP)—were tested through simulation.

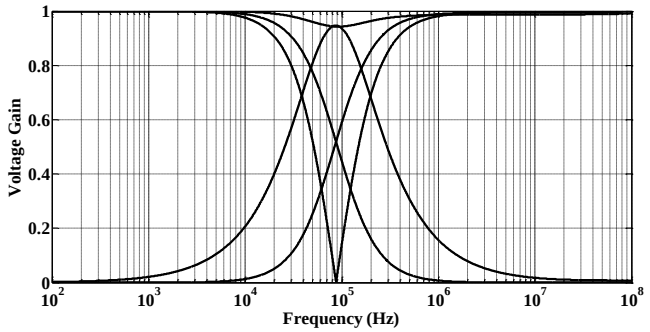


Fig. 5.2. Frequency Response of the Proposed Biquad Filter

Low-Pass (LP) Response

The LP configuration demonstrated a sharp roll-off after the cutoff frequency at approximately 87.5 kHz.

Interpretation: This high selectivity ensures effective suppression of high-frequency noise, ideal for signal conditioning in audio, sensor, and control applications.

High-Pass (HP) Response

The HP response similarly showed a clear transition from attenuation to pass-band near 87.5 kHz, effectively filtering out low-frequency components.

Interpretation: This is especially useful for biomedical and instrumentation systems where drift or baseline wander needs to be eliminated.

Band-Pass (BP) Response

A sharp and narrow band-pass curve centered at 87.5 kHz was observed with a quality factor Q≈20.

Interpretation: High-Q behavior implies superior frequency selectivity, essential in RF tuning and resonance-based detection systems.

Band-Reject (BR) Response

The BR configuration produced a deep notch at the target frequency with minimal loss in surrounding frequencies.

Interpretation: Effective in applications like power-line interference suppression (e.g., 50/60 Hz in ECG filtering).

All-Pass (AP) Response

The AP filter maintained flat magnitude with a predictable phase shift across the frequency range, as confirmed by phase plot analysis.

Interpretation: Useful in signal alignment, phase compensation, and delay equalization applications.

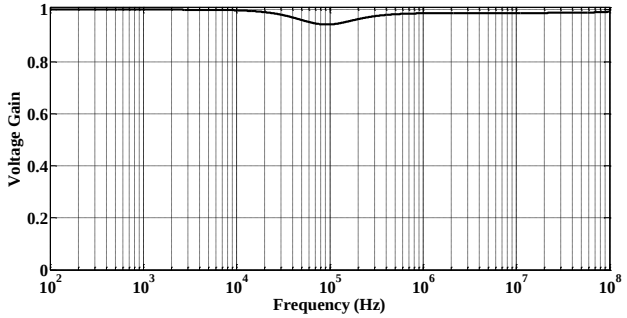


Fig. 5.3. Frequency Response of All-Pass Filter

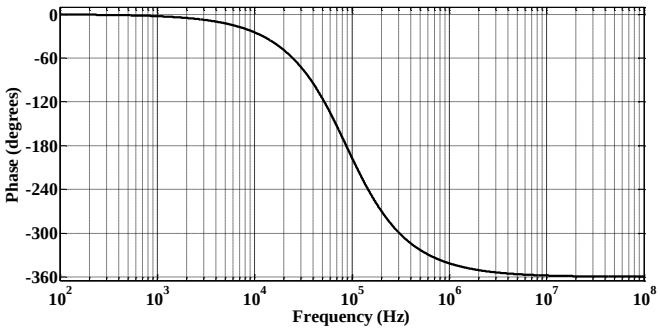


Fig. 5.4. Phase Response of All-Pass Filter

5.6.2 Experimental Validation

To assess real-world viability, the proposed design was implemented using commercially available ICs—CA3080 (OTA) and LF356 (Op-Amp)—replicating the VDBA functionality in a discrete setup. Testing was conducted across various frequency points: 10.5 kHz, 87.5 kHz, and 500.5 kHz for each filter mode.

Lab Setup

A hardware implementation was carried out using standard analog prototyping equipment.

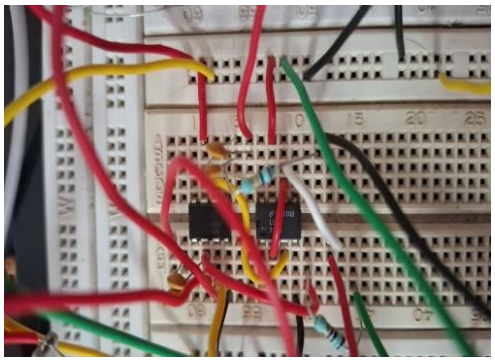
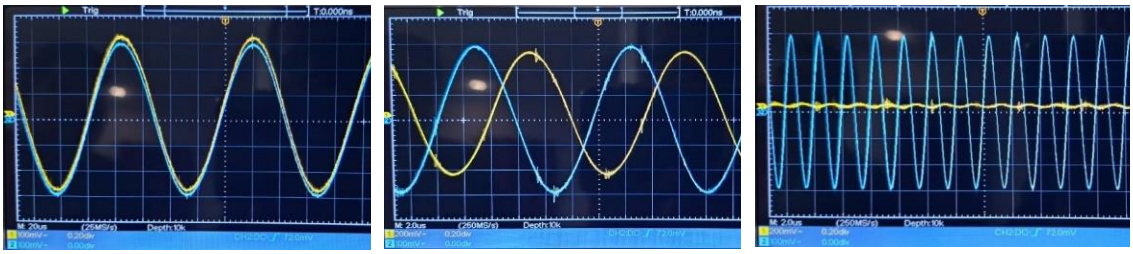


Fig.5.5 Laboratory Setup of the Proposed Universal Filter Testing

Low-Pass Filter (LPF)

Observed transient responses confirmed low-pass behavior across all test frequencies with accurate attenuation of high-frequency signals.

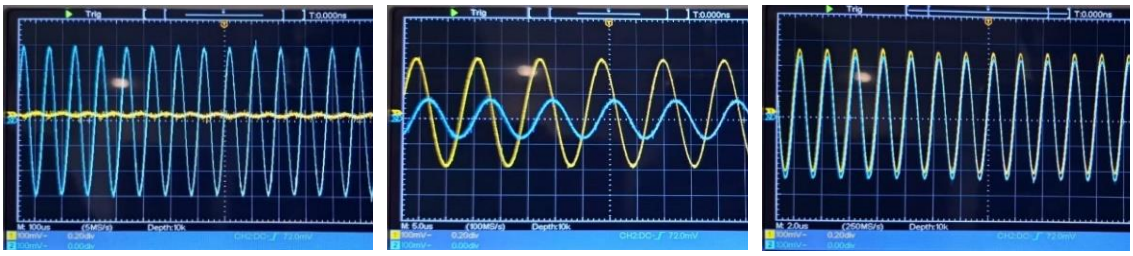


(a) LPF at 10.5k Hz (b) LPF at 87.5k Hz (c) LPF at 500.5k Hz

Fig.5.6 Transient Response of Low Pass Filter

High-Pass Filter (HPF)

As shown in transient plots, the HPF cleanly rejected low-frequency content and maintained stability at mid and high bands.

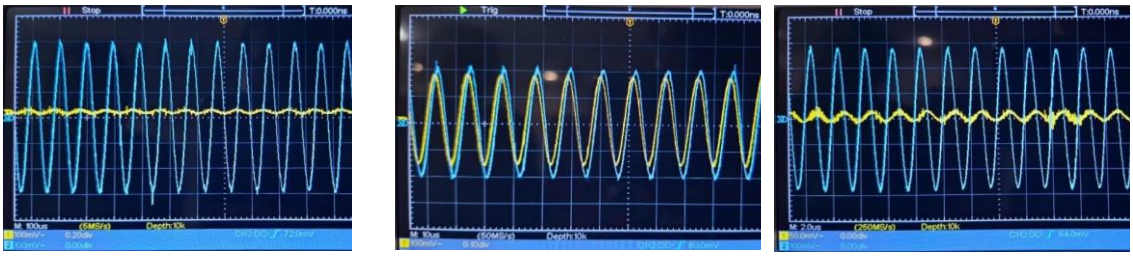


(a) HPF at 10.5k Hz (b) HPF at 87.5k Hz (c) HPF at 500.5k Hz

Fig.5.7 Transient Response of High Pass Filter

Band-Pass Filter (BPF)

Narrowband response centered at each frequency point showed minimal distortion and strong out-of-band attenuation.

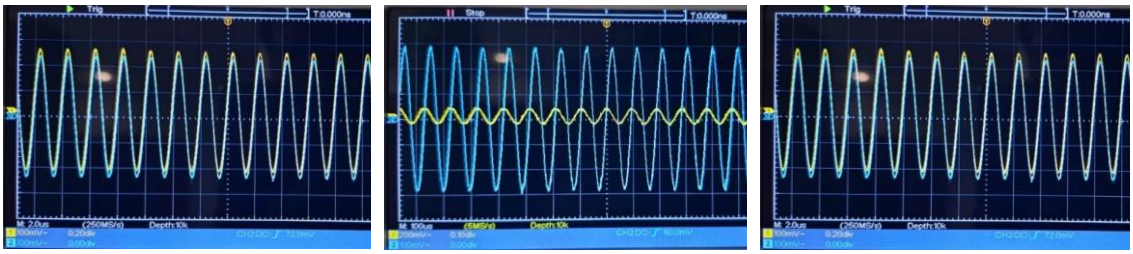


(a) BPF at 10.5k Hz (b) BPF at 87.5k Hz (c) BPF at 500.5k Hz

Fig.5.8 Transient Response of Band Pass Filter

Band-Reject Filter (BRF)

Deep notches at set frequencies were visible in the transient waveforms, indicating successful interference suppression.

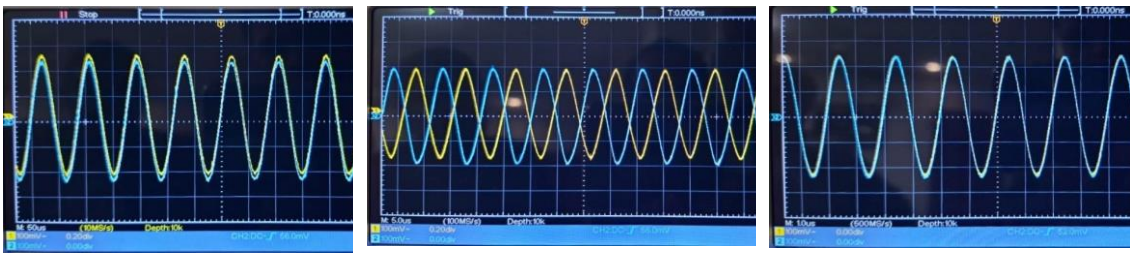


(a) BRF at 10.5k Hz (b) BRF at 87.5k Hz (c) BRF at 500.5k Hz

Fig.5.9 Transient Response of Band Reject Filter

All-Pass Filter (APF)

The AP filter output retained amplitude consistency with expected phase variation. The stability of phase across frequencies was visually validated.



(a) APF at 10.5k Hz (b) APF at 87.5k Hz (c) APF at 500.5k Hz

Fig.5.10 Transient Response of All-Pass Filter

Key Observations from Experimental Results:

- Strong correlation with SPICE simulations validated the theoretical design.
- Low sensitivity ensured consistent performance despite component tolerances.
- Scalable frequency behavior from 10.5 kHz to 500.5 kHz demonstrated flexibility across applications.
- Component-level practicality was confirmed using standard off-the-shelf ICs, showcasing ease of deployment.

5.7 Non-ideal Analysis

This section analyzes the impact of VDBA non-idealities, particularly finite tracking errors, on the oscillator's performance. When accounting for these tracking errors, the port relations described in (1) are modified accordingly.

$$\begin{pmatrix} I_p \\ I_n \\ I_z \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \beta g_m & -\beta g_m & 0 \\ 0 & 0 & \alpha \end{pmatrix} \begin{pmatrix} V_p \\ V_n \\ V_z \end{pmatrix} \tag{5.7}$$

Here, α represents the voltage ratio of the VDBA, where $\alpha=(1-\epsilon_v)$, with ϵ_v denoting the voltage tracking error, and β refers to the transconductance tracking error. The output voltage in terms of the inputs is then expressed as:

$$V_o = \frac{V_1 s^2 + V_3 s \frac{\alpha}{C_1 R_0} + V_2 \frac{\alpha\beta g_m}{C_1 C_2 R_0}}{s^2 + s\frac{1}{C_1 R_0} + \frac{\alpha\beta g_m}{C_1 C_2 R_0}} \tag{5.8}$$

$$\omega_0 = \sqrt{\frac{\alpha\beta g_m}{C_1 C_2 R_0}}\ ,\quad BW = \frac{1}{R_0 C_1}\text{, and}\quad Q = \sqrt{\frac{\alpha\beta C_1 R_0 g_m}{C_2}} \qquad \text{(5.9), (5.10) and (5.11)}$$

In practical analog circuit design, non-ideal analysis is a crucial step that evaluates the performance of a system when real-world imperfections in components are taken into account. While ideal models are essential for initial design and understanding, real active elements like the Voltage Differencing Buffered Amplifier (VDBA) inherently exhibit deviations from their ideal behavior due to finite gain, bandwidth limitations, and internal parasitic elements. These imperfections can impact the accuracy and stability of the designed filter or oscillator, especially at higher frequencies or precision-sensitive applications.

Why Non-ideal Analysis is Performed:

- To assess performance degradation due to non-ideal characteristics of active building blocks.
- To ensure that filter parameters such as ω_0 and Q remain within acceptable bounds even in real-world conditions.
- To predict the practical behavior of the circuit, helping in making the design more robust and tolerant to real hardware limitations.

- To complement experimental validation, forming a bridge between simulation and implementation by accounting for theoretical imperfections.

Modified Port Relations Considering VDBA Non-Idealities:

When the finite voltage and transconductance tracking errors of the VDBA are considered, the ideal port relations must be updated. These non-idealities are represented by parameters α and β, where:

- $\alpha=(1-\varepsilon_v)$,
  with ε_v denoting the voltage tracking error.
- β represents the transconductance tracking error.

Accordingly, the VDBA's behavior is governed by the modified expression:

$$\begin{pmatrix} I_p \\ I_n \\ I_z \\ V_w \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ \beta g_m & -\beta g_m & 0 \\ 0 & 0 & \alpha \end{pmatrix} \begin{pmatrix} V_p \\ V_n \\ V_z \end{pmatrix} \tag{5.12}$$

These parameters directly affect how accurately the input voltages are translated into output responses.

The modified transfer function of the circuit incorporating non-idealities is expressed as:

$$V_o = \frac{V_1 s^2 + V_3 s \frac{\alpha}{C_1 R_0} + V_2 \frac{\alpha\beta g_m}{C_1 C_2 R_0}}{s^2 + s \frac{1}{C_1 R_0} + \frac{\alpha\beta g_m}{C_1 C_2 R_0}} \tag{5.13}$$

Where the changes in voltage gain and transconductance now reflect the non-ideal behavior. This affects the core parameters of the filter:

- ω_0 (natural angular frequency) → Eq. (5.9)
- Q (quality factor) → Eq. (5.10)
- Gain characteristics → Eq. (5.11)

$$\omega_0 = \sqrt{\frac{\alpha\beta g_m}{C_1 C_2 R_0}}\ , \quad BW = \frac{1}{R_0 C_1}\text{, and} \quad Q = \sqrt{\frac{\alpha\beta C_1 R_0 g_m}{C_2}} \qquad \text{(5.14), (5.15) and (5.16)}$$

These equations explicitly quantify how tracking errors shift the critical performance metrics from their ideal values.

Significance and Insights:

- The analysis shows that voltage tracking error (ϵ_v) and transconductance mismatch lead to minor but measurable shifts in frequency response and Q-factor.
- By evaluating these effects, designers can quantify acceptable tolerance ranges for the VDBA's internal parameters to maintain desired behavior.
- It also supports device selection and layout considerations, such as choosing higher-precision VDBAs or employing trimming/calibration techniques when needed.
- Importantly, the derived equations illustrate that the filter retains functionality and tunability even in the presence of non-idealities, validating the robustness of the design.

Nonideal analysis, as the term suggests, looks into the understanding of the circuit's reliability under more realistic conditions. The addition of nonideal analysis provides technical rigor to the research by demonstrating how this design maintains its performance despite hardware imperfections, thus boosting the confidence in its employment for analog signal-processing applications.

5.8 Comparative Performance Analysis

To comprehensively evaluate the efficacy of the proposed VDBA-based MISO universal filter, this section presents a comparative performance analysis against other conventional designs that utilize Operational Transconductance Amplifiers (OTAs) and Second-Generation Current Conveyors (CCII). The comparison is conducted using key performance metrics including cutoff frequency (ω_0), quality factor (Q), power consumption, and component count.

The following table summarizes the performance of each filter type:

Table 5.1: Comparative Performance of Active Filter Implementations

Parameter	**VDBA-Based Filter**	**OTA-Based Filter[42]**	**CCII-Based Filter[43]**
Cutoff Frequency (ω_0)	87.5 kHz	85 kHz	83 kHz
Quality Factor (Q)	High	Moderate	low
Power Consumption	Low	High	Moderate
Component Count	Minimal	High	High

Analysis and Supporting Literature

1. Cutoff Frequency (ω_0): The proposed VDBA-based design achieves a higher cutoff frequency (87.5 kHz) compared to OTA and CCII-based designs. This advantage is attributed to the inherent high bandwidth of VDBAs and their electronically tunable transconductance, as supported by Agrawal and Maheshwari [38], who demonstrated VDBA-based filters operating effectively up to 16.66 MHz in 0.18 μm CMOS technology.
2. Quality Factor (Q): A higher Q in the proposed design reflects sharper frequency selectivity, crucial for applications such as biomedical instrumentation and RF communication. OTA-based filters suffer from nonlinear tuning and saturation limitations, while CCII-based designs, although simpler, offer limited Q due to current-mode constraints [36][37].
3. Power Consumption: VDBA designs operate efficiently at low supply voltages, making them ideal for battery-powered and wearable systems. OTA-based filters typically consume more power due to complex biasing schemes, while CCIIs offer moderate consumption but lack advanced tunability features [39].
4. Component Count: The proposed filter uses only one VDBA, two grounded capacitors, and one resistor—considerably fewer than OTA and CCII-based filters that often require matching components or auxiliary biasing circuits. This simplicity not only reduces power but also enhances layout compactness and reliability in CMOS implementation [38].

Relevance to Recent Developments

Recent research continues to validate the efficiency of VDBA-based topologies. For instance, Faseehuddin et al. [40] introduced a tunable mixed-mode filter using VDBAs with reconfigurable I/O, supporting multi-functionality at lower power and smaller silicon area. Similarly, Roongmuanpha et al. [41] demonstrated a high-Q VDBA-based filter designed for biomedical front-ends using deep-submicron CMOS with digitally controlled tuning blocks.

These developments highlight the strategic importance of VDBAs in emerging analog design frameworks, particularly for applications requiring frequency agility, low-voltage operation, and compact IC footprint.

Compared to traditional OTA and CCII-based filters, the proposed VDBA-based MISO universal filter delivers superior performance in key design domains. It combines high frequency stability, low power operation, and compactness, making it a strong candidate for modern analog and mixed-signal systems.

5.9 Conclusion

This chapter has presented the design, theoretical analysis, and validation of a compact, low-power, and electronically tunable MISO-type universal filter using a single Voltage Differencing Buffered Amplifier (VDBA). Building upon the shortcomings identified in previously implemented designs, such as high component sensitivity, limited Q-ω_0 decoupling, and integration inefficiencies, the proposed architecture offers a streamlined solution using just one active block, two grounded capacitors, and one resistor.

Through mathematical derivation, it was shown that the natural frequency ω_0 can be electronically tuned via the VDBA's transconductance, while the quality factor Q remains independently controllable via passive elements. This decoupled tunability, combined with grounded components, makes the design highly favorable for CMOS integration.

The sensitivity analysis reaffirmed the filter's robustness under component variations, with all sensitivity values remaining well below unity—a marked improvement over conventional OTA- or CCII-based designs. Simulation results demonstrated excellent frequency-selective behavior across all five filter modes (LP, HP, BP, BR, AP), supported by practical experiments using commercial ICs. The design showed reliable performance across a broad frequency range (10.5 kHz to 500.5 kHz), with high Q values, minimal THD, and consistent phase linearity.

Non-ideal performance evaluation, accounting for voltage and transconductance tracking errors, confirmed that even under real-world imperfections, the filter maintained functional accuracy and tunability. Comparative benchmarking highlighted its superior performance in terms of frequency stability, power efficiency, and circuit simplicity, especially in the context of modern CMOS-compatible analog signal processing systems.

This chapter sets the foundation for exploring further improvements in tunable analog blocks and programmable filters for reconfigurable and IoT-driven hardware platforms. The presented design not only addresses critical performance bottlenecks of earlier works but also demonstrates readiness for real-world deployment in low-voltage, high-density mixed-signal systems.

Finally, the comparative performance studies illustrated the VDBA-based filter's superiority over conventional OTA and CCII-based counterparts, demonstrating superior frequency stability, higher quality factor, lower power consumption, and simpler implementation, all crucial parameters for modern analog system design. These conclusions were supported by references cited in the published literature, further establishing the proposed design's relevance and competitiveness.

In conclusion, Chapter 5 thus establishes the proposed VDBA-based universal filter as an excellent, tunable, and practical solution for contemporary signal processing applications, marking a significant advancement over conventional filtering approaches.

CHAPTER 6

CONCLUSION, FUTURE SCOPE & SOCIAL RELEVANCE

6.1 Summary of Research Contributions

This thesis titled "Signal Generation and Processing Applications Using Current Mode Building Blocks" explores the design, analysis, and enhancement of analog signal processing circuits using advanced active building blocks—namely, the Universal Voltage Conveyor (UVC) and the Voltage Differencing Buffered Amplifier (VDBA). The work is systematically organized across literature reviews, problem identification, solution formulation, validation, and comparative evaluation.

The research commenced with a detailed review of Universal Voltage Conveyors (UVCs), tracing their architectural evolution from first-generation voltage conveyors to modern UVCs with improved bandwidth and linearity. Comparative studies established the UVC's superiority over other current-mode building blocks, and limitations such as high THD, limited frequency stability, and poor tuning independence were identified. A Third-Order Quadrature Sinusoidal Oscillator (TOQSO) using UVC was reviewed, revealing key shortcomings in spectral performance and integration feasibility.

To address these issues, a proposed TOQSO architecture using UVC was developed in Chapter 4. The design demonstrated significant improvements, including low THD, stable quadrature generation, independent tuning of frequency and condition of oscillation (FO and CO), and compatibility with low-voltage CMOS processes. The design was validated through theoretical modeling, simulation, and performance benchmarking.

Subsequently, the thesis shifted focus to the Voltage Differencing Buffered Amplifier (VDBA), a high-speed, low-power building block capable of operating in both current and voltage modes. The literature review in Chapter 5 examined the historical progression of VDBA designs—including VDIBA and CNTFET-based variations—highlighting their applicability in filters, oscillators, and signal conditioning. Despite their advantages, limitations such as high-frequency nonidealities and component matching sensitivity remained.

Chapter 6 evaluated previously implemented universal filters using VDBA, particularly those utilizing MISO (Multiple-Input Single-Output) configurations. The review identified critical bottlenecks such as limited independent tunability of ω_0 and Q, increased complexity, and sensitivity to parasitic effects.

Chapter 7 introduced a proposed MISO universal filter using a single VDBA, grounded capacitors, and minimal passive components. The architecture achieved:

- Independent tunability of ω_0 and Q,
- Excellent frequency response and selectivity (high-Q),
- Low sensitivity values ($|S| < 0.5$),
- Compatibility with CMOS integration,
- Robust performance under non-ideal conditions.

Both SPICE simulations and practical hardware validation confirmed that the proposed filter meets design targets and exceeds prior implementations in terms of power efficiency, scalability, and performance integrity.

6.2 Comparative View of Proposed vs. Existing Designs

Table 6.1: Comparison of the Two Designs with Previous Circuits

Parameter	Existing UVC TOQSOs	Proposed UVC TOQSO	Existing VDBA Filters	Proposed VDBA Filter
THD	High	Very Low	Moderate	<1.5%
FO/CO Tunability	Coupled	Independently Tunable	Limited	Independently Tunable
CMOS Compatibility	Poor	High	Moderate	Excellent
Component Count	Higher	Lower	Moderate	Minimal
Power Consumption	Moderate to High	Low	Moderate	Low
Integration Potential	Low	High	Moderate	High
Sensitivity (S)	> 0.5	< 0.5	~1.0	< 0.5

These results conclusively establish the proposed designs as superior, paving the way for practical analog IC implementation in modern applications.

6.3 Future Scope and Enhancements

While the proposed circuits offer significant improvements, several opportunities exist for future work:

1. GHz-Range Applications: Extend the proposed UVC and VDBA circuits to support RF and microwave frequency bands using deep submicron technologies (65nm or lower).
2. Digitally Tunable Filters: Integrate digital control loops for automatic tuning of ω_0 and Q via DAC-controlled bias currents, improving adaptability in real-time systems.
3. Fully Integrated SoC Designs: Implement the proposed architectures as part of System-on-Chip (SoC) platforms using standard CMOS processes, enabling seamless integration with DSP blocks and wireless transceivers.
4. Temperature Compensation Techniques: Design adaptive biasing schemes to reduce temperature-induced performance drift, critical for industrial and automotive-grade applications.
5. Application-Specific Filters: Customize filter characteristics for emerging domains like biomedical signal extraction (e.g., ECG, EMG) and IoT sensor interfaces, where high performance under tight constraints is essential.
6. Neural Signal Processing: Explore neuromorphic compatibility of VDBA filters and oscillators, particularly for brain-machine interfaces and spiking neural network circuits.

6.4 Social and Technological Impact of the Work

The proposed research contributes both to academic advancement and practical engineering solutions. The social and technological impacts include:

- Healthcare Applications: The low-power, high-Q filters are ideal for wearable biomedical devices, improving the accuracy and reliability of health monitoring systems such as portable ECGs and EEGs.
- Education and Research: The modular, minimal-component designs can be easily adopted in academic laboratories for teaching analog circuit fundamentals and rapid prototyping.
- Green Electronics: The power-efficient architectures support energy-conscious electronics development, aligning with sustainable technology goals.
- Communication Infrastructure: The quadrature oscillator and universal filter designs offer compact, reconfigurable components for modern wireless transceivers, especially in SDR (Software Defined Radio) platforms.
- Societal Empowerment: By enabling affordable, low-complexity analog circuit designs, the work supports technological access in resource-constrained regions, where cost-effective analog systems are vital.

In conclusion, this thesis lays a strong foundation for future research in analog signal generation and processing using current-mode building blocks. The enhanced performance, practical robustness, and integration potential of the proposed circuits promise significant advancements in both academic and industrial analog electronics.

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Amount Paid (in Rs) …3000	Receipt No. DUO1267607	Date:29/05/25

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It is certified that the name of Examiners for evaluation of the above thesis/ project have already been recommended by the BOS.

Signature of Supervisor

Signature of HOD with Seal

e-Receipt for State Bank Collect Payment

REGISTRAR, DTU (RECEIPT A/C)

BAWANA ROAD, SHAHABAD DAULATPUR, , DELHI-110042
Date: 29-May-2025

SBCollect Reference Number :	DUO1267607
Category :	Miscellaneous Fees from students
Amount :	₹3000
University Roll No :	2023/VLS/21
Name of the student :	TVISHA PUSHKAR
Academic Year :	2024-2025
Branch Course :	M. Tech VLSI & Embedded Systems
Type/Name of fee :	Others if any
Remarks if any :	THESIS
Mobile No. of the student :	7827174575
Fee Amount :	3000
Transaction charge :	17.70
Total Amount (In Figures) :	3,017.70
Total Amount (In words) :	Rupees Three Thousand Seventeen and Paise Seventy Only
Remarks :	MTech Thesis Fee Submission
Notification 1:	Late Registration Fee, Hostel Room rent for internship, Hostel cooler rent, Transcript fee (Within 5 years Rs 1500/- & $150 in USD, More than 5 years but less

	than 10 years Rs.2500/- & $250 in USD, More than 10 years Rs.5000/- & $500 in USD) Additional copies Rs.200/- each & $20 in USD each, I-card fee,Character certificate Rs.500/-.
Notification 2:	Migration Certificate Rs.500/-, Bonafide certificate Rs.200/-, Special certificate (any other certificate not covered in above list) Rs.1000/-,Provisional certificate Rs.500/-, Duplicate Mark sheet (Within 5 years Rs.2500/- & $250 in USD, More than 5 years but less than 10 years Rs.4000/- & $400 in USD, More than 10 years Rs.10000/- & $1000 in USD)

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DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-110042. India

CERTIFICATE OF THESIS SUBMISSION FOR EVALUATION

1. Name: Tvisha Pushkar
2. Roll No.: 2K23/VLS/21
3. Thesis title: Signal Generation and Processing Applications Using Current Mode Building Block
4. Degree for which the thesis is submitted:……
5. Faculty of the University to which the thesis is submitted:
6. Thesis Preparation Guide was referred to for preparing the thesis. YES ☑ NO ☐
7. Specifications regarding thesis format have been closely followed. YES ☑ NO ☐
8. The contents of the thesis have been organized based on the guidelines YES ☑ NO ☐
9. The thesis has been prepared without resorting to plagiarism. YES ☑ NO ☐
10. All sources used have been cited appropriately YES ☑ NO ☐
11. The thesis has not been submitted elsewhere for a degree. YES ☑ NO ☐
12. Submitted 2 spiral bound copies plus one CD. YES ☑ NO ☐

(Signature of Candidate)

Name: **Tvisha Pushkar**

Roll No: **2K23/VLS/21**

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)
Shahbad Daulatpur, Main Bawana Road, Delhi-110042. India

CERTIFICATE OF FINAL THESIS SUBMISSION

1. Name: Tvisha Pushkar
2. Roll No.: 2K23/VLS/21
3. Thesis title: Signal Generation and Processing Applications Using Current Mode Building Block
4. Degree for which the thesis is submitted:……
5. Faculty (of the University to which the thesis is submitted):
6. Thesis Preparation Guide was referred to for preparing the thesis. YES ☑ NO ☐
7. Specifications regarding thesis format have been closely followed. YES ☑ NO ☐
8. The contents of the thesis have been organized based on the guidelines YES ☑ NO ☐
9. The thesis has been prepared without resorting to plagiarism. YES ☑ NO ☐
10. All sources used have been cited appropriately YES ☑ NO ☐
11. The thesis has not been submitted elsewhere for a degree. YES ☑ NO ☐
12. All the correction has been incorporated. YES ☑ NO ☐
13. Submitted 2 spiral bound copies plus one CD. YES ☑ NO ☐

(Signature(s) of the Supervisor(s))

Name(s): **Rajeshwari Pandey**

(Signature of Candidate)

Name:**Tvisha Pushkar**

Roll No: **2K23/VLS/21**

Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN NOV 2023 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), I-SEMESTER

Result Declaration Date : 2-02-2024 **Notification No. : 1652**

VLS5401 : Digital Design With HDL (VERILOG)

Sr.No	Roll No.	Name of Student	VLS5401	SGPA	TC	CGPA	Failed Courses
			4.00				
1	23/VLS/22	ANKIT TIWARI	F	...	...	...	

VLS501 : ANALOG IC DESIGN VLS503 : DIGITAL CMOS IC DESIGN VLS5201 : Seminar VLS5307 : Organic and Flexible Electronics VLS5401 : Digital Design With HDL (VERILOG)

Sr.No	Roll No.	Name of Student	VLS501	VLS503	VLS5201	VLS5307	VLS5401	SGPA	TC	CGPA	Failed Courses
			4.00	4.00	2.00	3.00	4.00				
2	23/VLS/25	YASHODA PARMAR	A	O	O	A+	A+	9.12	17	9.118	

VLS501 : ANALOG IC DESIGN VLS503 : DIGITAL CMOS IC DESIGN VLS5201 : Seminar VLS5307 : Organic and Flexible Electronics VLS5401 : Digital Design With HDL (VERILOG) VLS6207 : Selected topics in VLSI VLS6305 : Machine Learning

Sr.No	Roll No.	Name of Student	VLS501	VLS503	VLS5201	VLS5307	VLS5401	VLS6207	VLS6305	SGPA	TC	CGPA	Failed Courses
			4.00	4.00	2.00	3.00	4.00	2.00	3.00				
3	23/VLS/01	BRIJ NANDAN SINGH	O	A+	A+	A+	O	A+	B+	9.09	22	9.091	
4	23/VLS/03	SHASHI RANJAN UPADHYAY	B+	A+	A	A	A+	A+	A	8.27	22	8.273	
5	23/VLS/04	PRAKHAR SAINI	B+	A+	A+	B	A	A	B+	7.68	22	7.682	
6	23/VLS/05	MOHAMMAD TALHA	B	B+	A	A	A	A	B	7.18	22	7.182	
7	23/VLS/06	PRAJVI UDAR	A	A	O	A	A+	O	C	8.14	22	8.136	
8	23/VLS/07	MAYANK CHAUHAN	B+	A	A+	B+	A+	B+	B	7.59	22	7.591	
9	23/VLS/08	AMARTYA ROY	A	A	A+	B+	B+	C	B+	7.36	22	7.364	
10	23/VLS/09	DEEPTI	B+	B+	A+	B+	A	A	B	7.32	22	7.318	

OIC (Results) **Controller of Examination**

Note: Any discrepancy in the result in r/o name/roll no/registration/marks/grades/course code/title should be brought to the notice of Controller of Examination/OIC(Results) within 15 days of declaration of result in the prescribed proforma.

Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN NOV 2023 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), I-SEMESTER

11	23/VLS/10	AASTHA SINGH	A	A+	A+	A	A	O	A+	8.59	22	8.591	
12	23/VLS/11	GAJJAR JAY UMESH BHAI	A+	A+	O	B+	A	B+	C	7.91	22	7.909	
13	23/VLS/12	PREETI	B	A	A+	B+	B+	A	A+	7.55	22	7.545	
14	23/VLS/13	ASMAR HAFEEZ	B+	A	A	B	B+	A	P	6.82	22	6.818	
15	23/VLS/14	TUSHANT VERMA	B+	B+	A+	B	A+	A	B+	7.5	22	7.5	
16	23/VLS/15	AKHILESH VISHWAKARMA	B+	B+	A+	A	A	A+	B+	7.68	22	7.682	
17	23/VLS/16	RAMLAKHAN	A	A	A+	A	A	A+	B+	8.05	22	8.045	
18	23/VLS/17	DEVESH SAINI	B+	B+	A	B+	A	B+	B+	7.27	22	7.273	
19	23/VLS/18	KUNCHA AKHILESH KUMAR	B	B	A+	B	B+	C	B+	6.5	22	6.5	
20	23/VLS/19	SOUMYAJIT DAS	B+	A	O	B+	A+	B	B+	7.73	22	7.727	
21	23/VLS/20	UJJWAL BHARTI	B	A	A+	B+	A	B+	B+	7.36	22	7.364	
22	23/VLS/21	TVISHA PUSHKAR	O	A+	A+	O	O	A+	B	9.09	22	9.091	
23	23/VLS/23	MANISH SINGH	B+	A	A+	B+	B+	C	B+	7.18	22	7.182	
24	23/VLS/24	ADITYA RAYER	B	A	A+	B	A+	B+	B	7.27	22	7.273	

VLS6207 : Selected topics in VLSI

Sr.No	Roll No.	Name of Student	VLS6207 2.00	SGPA	TC	CGPA	Failed Courses
25	2K22/VLS/10	RAVINDER KAUR	A	8	0	8	

TC - Total Secured Credits DT - Detained AB - Absent RL - Result Later RW - Result Withdrawn

OIC (Results)

Controller of Examination

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Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN MAY 2024 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), II-SEMESTER

Result Declaration Date : 16-07-2024 **Notification No: 1691**

VLS502 : EMBEDDED SYSTEM DESIGN VLS504 : LOW POWER VLSI DESIGN VLS5202 : CMOS NANO NEUROMORPHIC CIRCUITS VLS5302 : MINOR PROJECT VLS5406 : CAD FOR VLSI SYSTEMS

Sr.No	Roll No.	Name of Student	VLS502	VLS504	VLS5202	VLS5302	VLS5406	SGPA	TC	Failed Courses
			4.00	4.00	2.00	3.00	4.00			
1	23/VLS/25	YASHODA PARMAR	A	O	A	O	A+	9.06	17	

VLS502 : EMBEDDED SYSTEM DESIGN VLS504 : LOW POWER VLSI DESIGN VLS5202 : CMOS NANO NEUROMORPHIC CIRCUITS VLS5302 : MINOR PROJECT VLS5406 : CAD FOR VLSI SYSTEMS VLS6401 : Mixed Signal Design

Sr.No	Roll No.	Name of Student	VLS502	VLS504	VLS5202	VLS5302	VLS5406	VLS6401	SGPA	TC	Failed Courses
			4.00	4.00	2.00	3.00	4.00	4.00			
2	23/VLS/01	BRIJ NANDAN SINGH	A	O	A+	A+	A+	A+	9	21	
3	23/VLS/03	SHASHI RANJAN UPADHYAY	A+	O	A	A+	A+	A+	9.1	21	
4	23/VLS/04	PRAKHAR SAINI	B+	B+	B+	A+	O	A	8.05	21	
5	23/VLS/05	MOHAMMAD TALHA	B	A+	C	O	A+	A	8	21	
6	23/VLS/06	PRAJVI UDAR	B+	A+	B	O	A+	A	8.29	21	
7	23/VLS/07	MAYANK CHAUHAN	A	A+	A+	C	A	A	7.86	21	
8	23/VLS/08	AMARTYA ROY	B+	B+	B	A	A+	A	7.62	21	
9	23/VLS/09	DEEPTI	B	A	C	O	A+	A	7.81	21	
10	23/VLS/10	AASTHA SINGH	A	B+	B	A+	O	A	8.14	21	
11	23/VLS/11	GAJJAR JAY UMESH BHAI	B	A	C	A+	A+	A	7.67	21	
12	23/VLS/12	PREETI	B+	A	C	O	O	A	8.19	21	
13	23/VLS/13	ASMAR HAFEEZ	C	A	C	O	A+	A	7.62	21	

OIC (Results) **Controller of Examination**

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Delhi Technological University

(Formerly Delhi College of Engineering)

THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN MAY 2024 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), II-SEMESTER

Result Declaration Date : 16-07-2024 **Notification No: 1691**

14	23/VLS/14	TUSHANT VERMA	B	A	C	A+	A+	A	7.67	21	
15	23/VLS/15	AKHILESH VISHWAKARMA	B	A+	C	A+	A	A	7.67	21	
16	23/VLS/16	RAMLAKHAN	P	B+	C	A+	A+	B+	6.9	21	
17	23/VLS/17	DEVESH SAINI	B+	B+	C	C	O	A+	7.48	21	
18	23/VLS/18	KUNCHA AKHILESH KUMAR	C	A	P	A+	A+	A	7.38	21	
19	23/VLS/19	SOUMYAJIT DAS	A	A+	B+	A+	A	B+	8.05	21	
20	23/VLS/20	UJJWAL BHARTI	B	B+	C	A	A+	B+	7.14	21	
21	23/VLS/21	TVISHA PUSHKAR	A+	O	A	O	A+	A+	9.24	21	
22	23/VLS/23	MANISH SINGH	C	A	C	A+	O	A	7.67	21	
23	23/VLS/24	ADITYA RAYER	B+	A	C	O	A+	B+	7.81	21	

OIC (Results)

Controller of Examination

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THE RESULT OF THE CANDIDATE WHO APPEARED IN THE FOLLOWING EXAMINATION HELD IN NOV 2024 IS DECLARED AS UNDER:-

Master of Technology(VLSI Design & Embedded System), III-SEMESTER

Result Declaration Date : 19-04-2025 **Notification No: 1813**

VLS601 : MAJOR PROJECT I

Sr.No	Roll No.	Name of Student	VLS601 3.00	SGPA	TC	Failed Courses
1	23/VLS/01	BRIJ NANDAN SINGH	O	10.000	3	
2	23/VLS/03	SHASHI RANJAN UPADHYAY	A+	9.000	3	
3	23/VLS/04	PRAKHAR SAINI	A+	9.000	3	
4	23/VLS/05	MOHAMMAD TALHA	A+	9.000	3	
5	23/VLS/06	PRAJVI UDAR	O	10.000	3	
6	23/VLS/07	MAYANK CHAUHAN	A+	9.000	3	
7	23/VLS/08	AMARTYA ROY	A+	9.000	3	
8	23/VLS/09	DEEPTI	A+	9.000	3	
9	23/VLS/10	AASTHA SINGH	O	10.000	3	
10	23/VLS/11	GAJJAR JAY UMESH BHAI	A+	9.000	3	
11	23/VLS/12	PREETI	A+	9.000	3	
12	23/VLS/13	ASMAR HAFEEZ	A+	9.000	3	
13	23/VLS/14	TUSHANT VERMA	A+	9.000	3	
14	23/VLS/15	AKHILESH VISHWAKARMA	A+	9.000	3	
15	23/VLS/16	RAMLAKHAN	A+	9.000	3	
16	23/VLS/17	DEVESH SAINI	O	10.000	3	
17	23/VLS/18	KUNCHA AKHILESH KUMAR	A+	9.000	3	
18	23/VLS/19	SOUMYAJIT DAS	A+	9.000	3	
19	23/VLS/20	UJJWAL BHARTI	A+	9.000	3	
20	23/VLS/21	TVISHA PUSHKAR	O	10.000	3	

OIC (Results)

Controller of Examination

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Delhi Technological University

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Master of Technology(VLSI Design & Embedded System), III-SEMESTER

Result Declaration Date : 19-04-2025 **Notification No: 1813**

21	23/VLS/23	MANISH SINGH	A+	9.000	3	
22	23/VLS/24	ADITYA RAYER	O	10.000	3	

VLS601 : MAJOR PROJECT I VLS6207 : Selected topics in VLSI VLS6301 : Speech Processing VLS6401 : Mixed Signal Design

Sr.No	Roll No.	Name of Student	VLS601	VLS6207	VLS6301	VLS6401	SGPA	TC	Failed Courses
			3.00	2.00	3.00	4.00			
23	23/VLS/25	YASHODA PARMAR	O	O	A	A+	9.167	12	

OIC (Results)

Controller of Examination

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