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Chapter 1

Introduction

1.1 Background

The growing demand for portable, high-speed, and energy-efficient devices has significantly increased the need for optimized arithmetic circuits. Among these, the full adder is one of the most fundamental building blocks in arithmetic logic units (ALUs), signal processors, and embedded platforms. Traditional full adder designs, such as the 28-transistor CMOS implementation, provide robust operation but suffer from high power consumption, increased area, and delay—issues that are exacerbated at deep submicron technology nodes.

To address these limitations, researchers have proposed several lower transistor-count architectures, including 14T and 18T hybrid logic designs, which reduce dynamic power and area by combining static CMOS, transmission gate, and pass-transistor logic. However, many of these still face challenges related to signal degradation, swing restoration, or scalability.

1.2 Motivation

The need to balance low power consumption, high speed, and technology scalability motivates the exploration of even more compact adder designs, such as the 10-transistor (10T) full adder. Recent advances show that hybrid logic 10T adders—especially those based on Static Energy Recovery Full Adder (SERF) and Gate Diffusion Input (GDI) principles—offer significant power and speed advantages.

To validate the practicality of these designs, it is essential to compare them not only among themselves (CMOS-based, SERF, GDI) but also against traditional architectures like 14T and 28T. Such a comparison across multiple CMOS technology nodes (180nm, 90nm, and 45nm) helps identify trade-offs and real-world applicability in scaled technologies.

1.3 Problem Statement

Despite numerous innovations in low-transistor-count adder architectures, there is still a lack of unified evaluation that considers:

- Low power and high-speed operation under submicron CMOS nodes.

- Full-swing logic preservation and reduced layout area.
- Comparative performance against traditional 14T and 28T full adder architectures.

1.4 Objectives

This thesis aims to:

- Design and implement three 10T full adder variants (CMOS-, SERF-, and GDI-based).
- Evaluate their performance across 180nm, 90nm, and 45nm CMOS technologies.
- Include functional waveforms, schematic views, and post-layout snapshots.
- Compare the 10T designs with conventional 14T and 28T full adders to highlight improvements in power, delay, PDP, and layout area.

1.5 Scope of Work

The thesis is structured around the design, implementation, and comparative analysis of three 10T full adder architectures. Each design is implemented at three technology nodes. Performance metrics such as power, delay, PDP, and layout area are extracted and compared. Additionally, conventional 14T and 28T designs are used as baseline references to contextualize the performance of the proposed 10T designs.

1.6 Methodology Overview

The research methodology includes:

1. Reviewing existing 10T, 14T, and 28T adder designs.
2. Implementing three 10T full adder topologies using Cadence Virtuoso.
3. Simulating each design under 180nm, 90nm, and 45nm PDKs using Spectre.
4. Comparing results with reference 14T and 28T designs using power, delay, PDP, and area as metrics.
5. Drawing conclusions and suggesting future improvements.

1.7 Thesis Organization

- **Chapter 1:** Introduction to full adder design challenges and thesis motivation.
- **Chapter 2:** Literature review of 10T, 14T, and 28T full adder architectures.
- **Chapter 3:** Detailed design of CMOS, SERF, and GDI-based 10T adders.
- **Chapter 4:** Implementation and simulation across 180nm, 90nm, and 45nm.

- **Chapter 5:** Comparative analysis with 14T, 28T, and intra-10T variants.
- **Chapter 6:** Conclusion and directions for future research.

Chapter 2

Literature Review

2.1 Introduction

Full adder circuits are essential components in arithmetic and logic units of modern digital systems. Their design directly impacts the power, delay, and overall area of complex data paths in microprocessors, DSPs, and portable embedded systems. With the scaling of CMOS technology, optimizing full adder design for both low power and high speed has become a key objective. A variety of topologies—including 28T conventional CMOS, 14T hybrid logic, and compact 10T designs—have been proposed to address this.

2.2 Conventional 28T CMOS Full Adder

The traditional 28-transistor (28T) full adder employs complementary CMOS pull-up and pull-down networks for sum and carry logic. It provides excellent noise margins and full-swing outputs, making it robust and ideal for cascading. However, it suffers from high dynamic power, increased area, and slower transitions due to large internal capacitance [10]. These limitations make the 28T adder unsuitable for energy-constrained or high-speed applications in deep submicron nodes.

2.3 14T Hybrid Logic Full Adder

To address the inefficiencies of 28T designs, researchers introduced 14T hybrid full adders. These designs typically combine XOR gates for sum generation and transmission gates or pass-transistors for carry logic. The 14T adder reduces transistor count and switching activity compared to the 28T CMOS design [**?**].

While 14T designs improve power and area metrics, they introduce challenges in signal degradation and logic swing, particularly at low supply voltages and smaller nodes. Additional buffers or restoration stages are often required to maintain full swing, which offsets the area and power gains.

2.4 10T Full Adders: CMOS, SERF, and GDI Variants

The 10T full adder has emerged as a promising architecture that achieves a superior trade-off between power, speed, and area. By efficiently using XOR–XNOR generation and multiplexer-based carry logic, it reduces transistor count while retaining essential functionality.

CMOS-Based 10T Design

CMOS-based 10T designs replicate basic full adder logic using minimal pass transistors and static logic. While these are robust in terms of swing, they may not always offer the best performance due to logic redundancy and transistor stacking.

SERF-Based 10T Design

Static Energy Recovery Full Adders (SERF) exploit charge recovery techniques to reduce dynamic power. As shown in [1], SERF-based 10T designs achieve excellent delay metrics, especially in scaled-down nodes like 45nm.

GDI-Based 10T Design

Gate Diffusion Input (GDI) logic reduces power and area by minimizing the number of switching transistors and using a compact logic structure. GDI-based 10T adders have been shown to provide the lowest average power consumption at all evaluated nodes, although they may require swing restoration in cascaded logic [1].

2.5 Comparative Insight: 10T vs 14T vs 28T

Multiple studies have compared low-transistor-count adders to traditional architectures. Based on simulation data from existing literature and this thesis:

- **Power:** 10T GDI and SERF variants consistently consume less power than 14T and 28T counterparts.
- **Delay:** 10T SERF adders achieve faster operation compared to 14T designs, especially under scaled technology nodes.
- **PDP:** The power-delay product for 10T designs is significantly lower—up to 50% improvement compared to 28T CMOS adders.
- **Area:** 10T designs are the most compact, while 14T provides a compromise between size and swing restoration needs.

2.6 Research Gap

Despite progress in 10T adder architectures, a unified and scalable design that:

- Outperforms 14T and 28T designs in PDP
- Maintains full swing operation across 180nm, 90nm, and 45nm
- Retains compact layout and functional correctness

is still a significant research need. This thesis addresses this gap by implementing and evaluating 10T CMOS, SERF, and GDI adders across all three technology nodes and comparing them with traditional 14T and 28T baselines.

2.7 Conclusion

This chapter surveyed the evolution of full adder circuits from traditional CMOS (28T) to hybrid logic (14T) and compact 10T architectures. It highlighted the trade-offs in power, speed, and scalability, which motivate the design and analysis of advanced 10T adders. The next chapter presents the proposed 10T adder designs and their schematic-level implementation.

Chapter 3

Design of Proposed 10T Adders

3.1 Introduction

In this chapter, we present the schematic design of three different 10T full adder architectures: CMOS-based, SERF-based (Static Energy Recovery Full Adder), and GDI-based (Gate Diffusion Input). Each architecture is optimized for low power and high speed, targeting 180nm, 90nm, and 45nm CMOS technology nodes. These designs are implemented and simulated in Cadence Virtuoso using the corresponding technology PDKs.

3.2 CMOS-Based 10T Full Adder

The CMOS 10T full adder utilizes pass transistor logic and a minimal transistor count to reduce area and dynamic power. XOR and XNOR logic are constructed using efficient transistor arrangements, followed by a multiplexer-based carry generator. This design aims to maintain full swing outputs with minimal logic degradation.

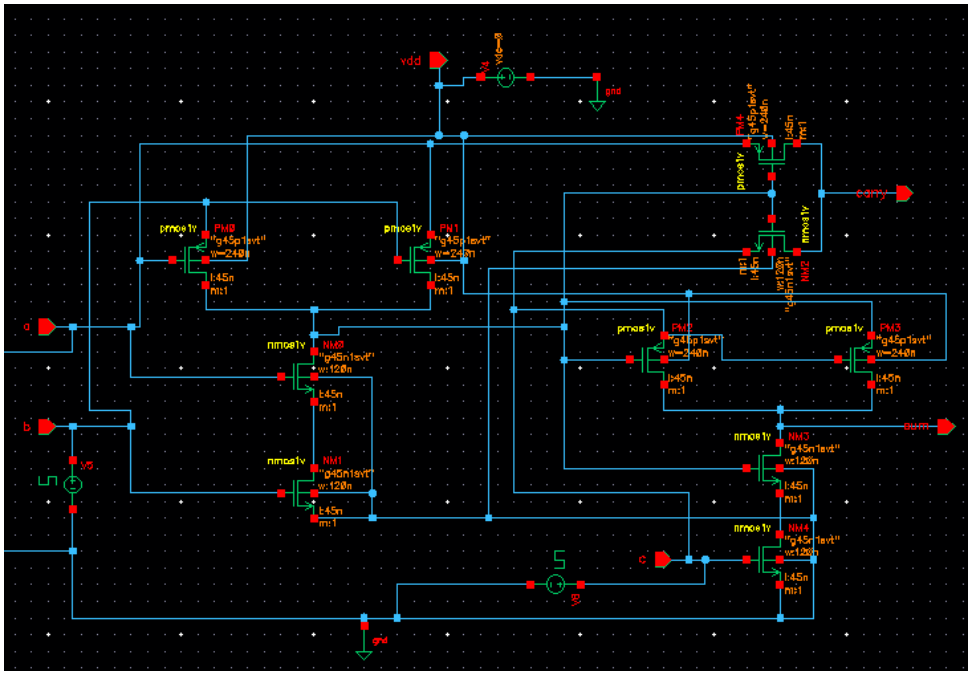

Figure 3.1: CMOS-Based 10T Full Adder Schematic

3.3 SERF-Based 10T Full Adder

The SERF-based design focuses on energy recovery and low switching activity by recycling charge from internal nodes. It significantly reduces average power dissipation while offering competitive speed. The XOR–XNOR logic and MUX-based carry generation are implemented using feedback paths and symmetrical routing to preserve signal integrity.

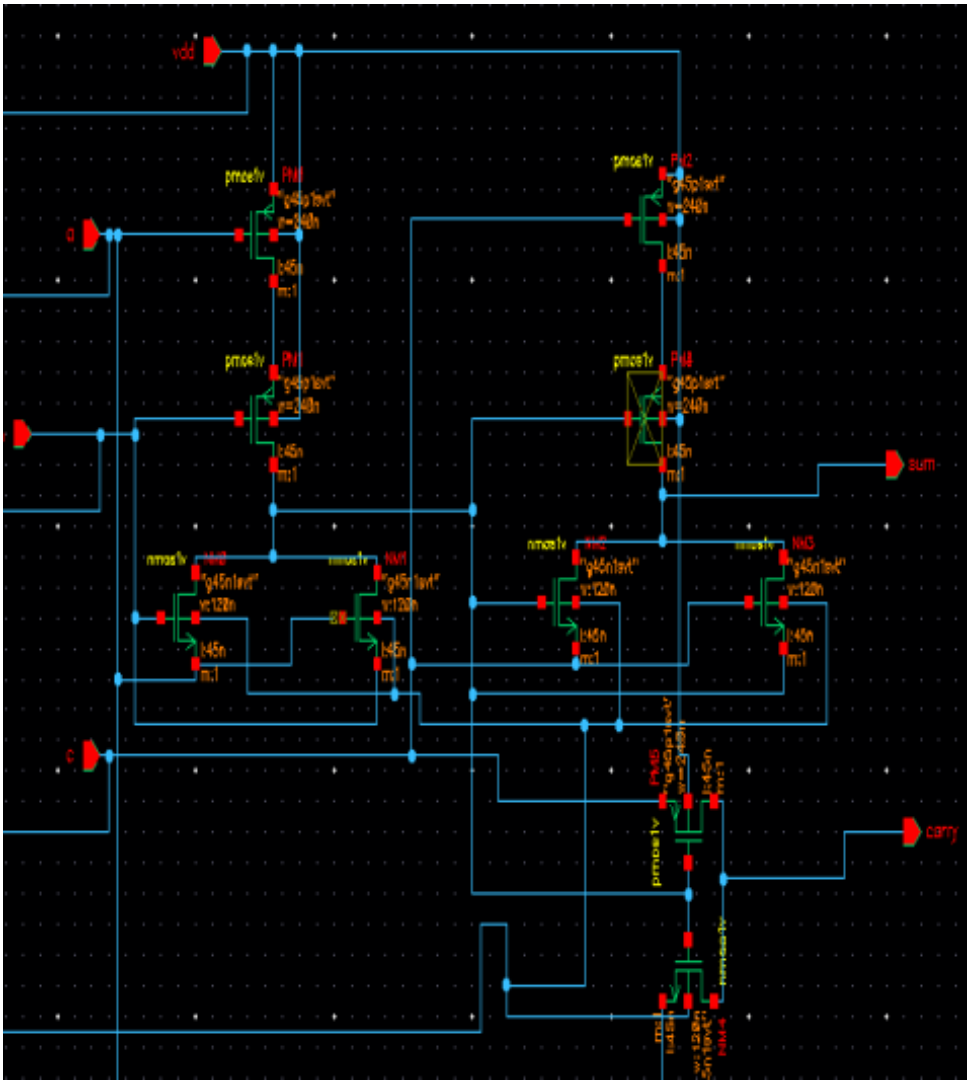

Figure 3.2: SERF-Based 10T Full Adder Schematic

3.4 Waveform Comparison at 45nm

The functional correctness of the proposed designs is verified using transient analysis in Spectre at 45nm. The waveform outputs for sum (S) and carry (C_{out}) clearly show the expected transitions in response to all 8 input combinations.

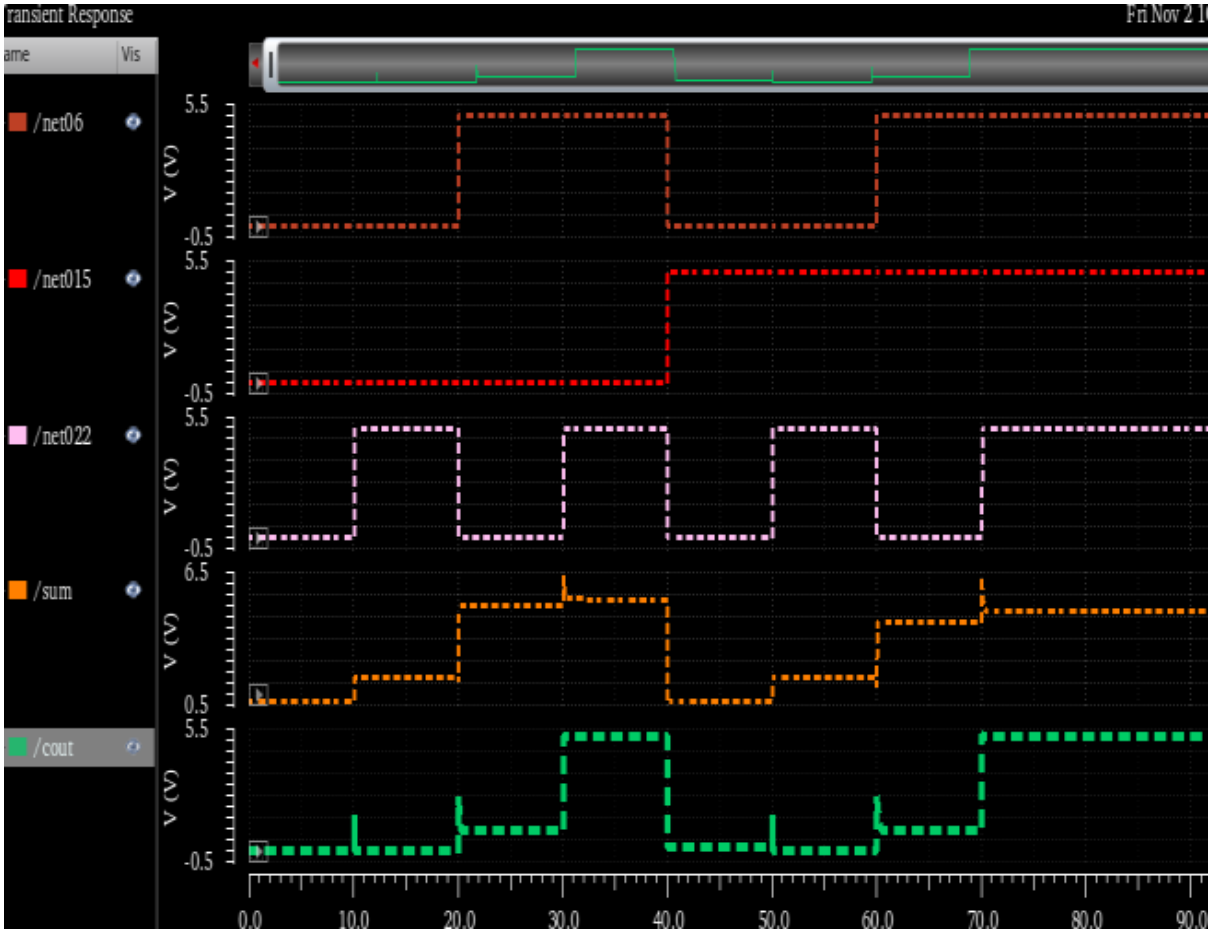

Figure 3.3: Simulation Waveform of 10T Full Adders at 45nm Node

3.5 GDI-Based 10T Full Adder

The GDI-based 10T adder achieves low power by minimizing switching activity and transistor stacking. This approach uses reduced logic levels for basic gates (AND, OR, MUX) and achieves better energy efficiency with fewer interconnects.

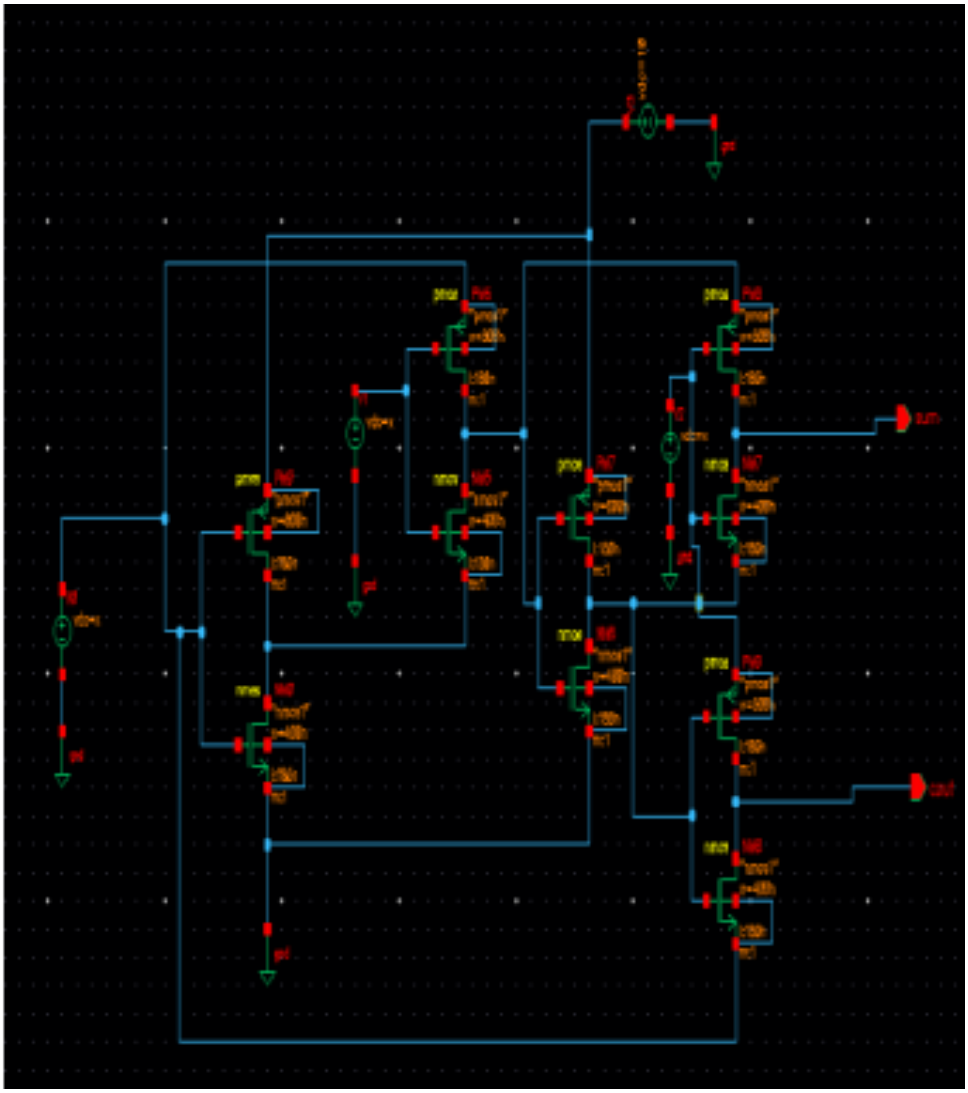

Figure 3.4: GDI-Based 10T Full Adder Schematic

3.6 Layout Snapshots

Physical layouts of the three 10T adders were generated using the 45nm technology node. Each layout was verified using Design Rule Check (DRC) and Layout Versus Schematic (LVS) tools. These layouts serve as proof of feasibility for fabrication and area estimation.

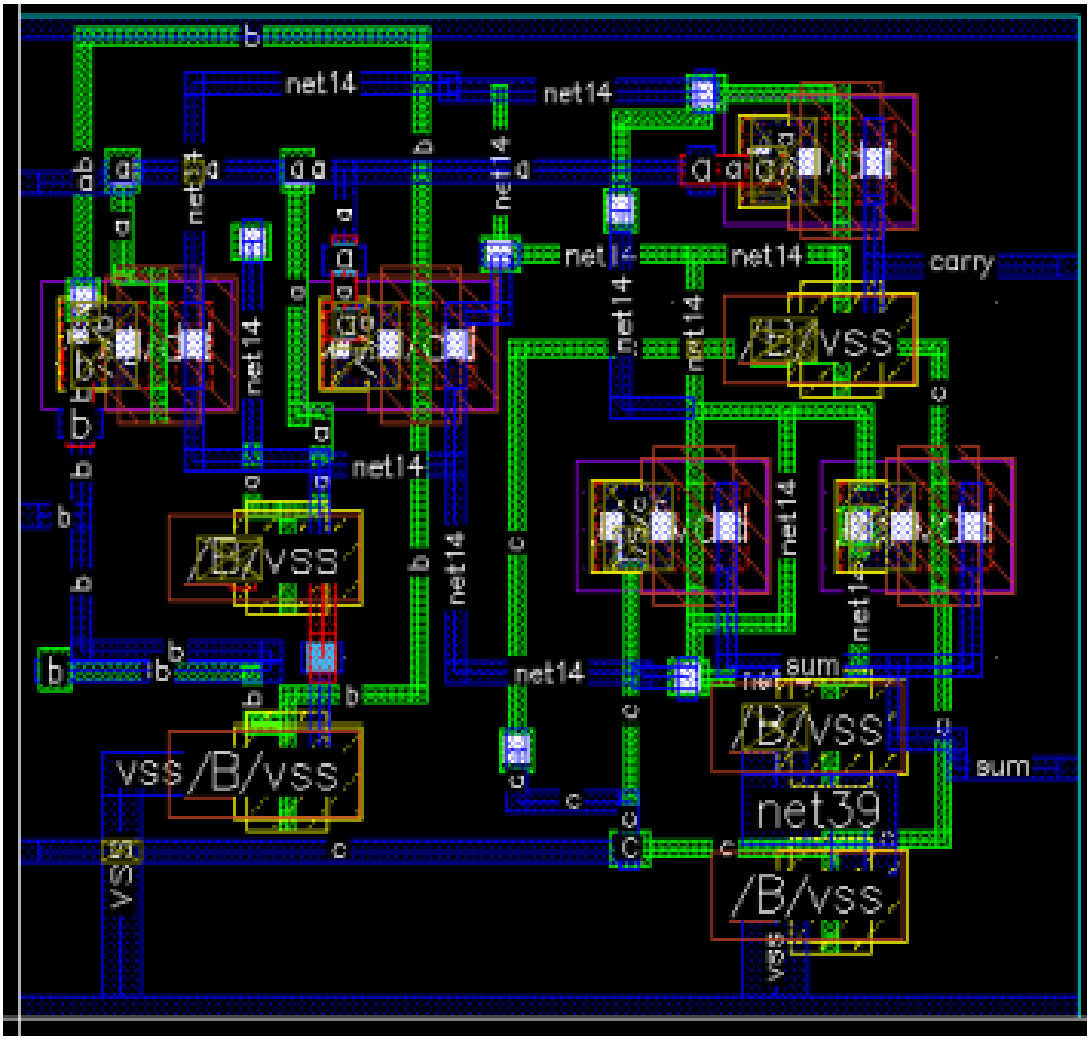

Figure 3.5: Layout of CMOS-Based 10T Full Adder at 45nm

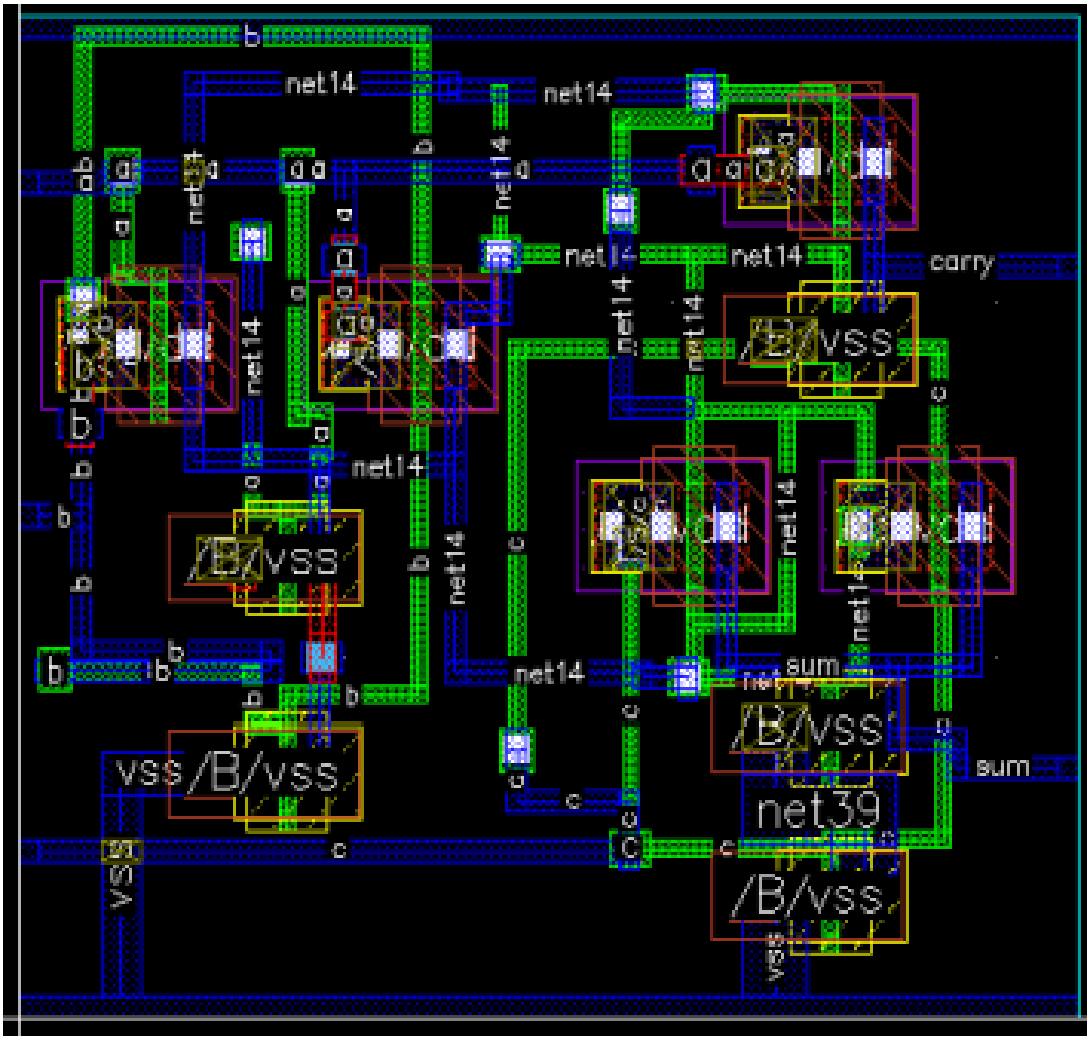

Figure 3.6: Layout of SERF-Based 10T Full Adder at 45nm

3.7 Conclusion

This chapter introduced three efficient 10T full adder architectures and their corresponding implementations in 45nm CMOS technology. Each design emphasizes either low power (GDI), high speed (SERF), or robustness (CMOS). These schematic and layout-level implementations will now be evaluated across multiple technology nodes in the next chapter.

Chapter 4

Implementation and Simulation

4.1 Design Flow and Tools Used

The schematic designs were implemented using Cadence Virtuoso, and simulations were performed using the Spectre simulator. Three technology nodes—180nm, 90nm, and 45nm—were used to evaluate scalability. Layout verification was done using DRC and LVS tools.

- **Tools:** Cadence Virtuoso, Spectre, Assura/Calibre
- **Technology Nodes:** 180nm, 90nm, 45nm PDKs
- **Supply Voltages:** 1.8V (180nm), 1.2V (90nm), 1.0V (45nm)
- **Load Capacitance:** 10fF

4.2 Simulation Methodology

Each full adder (10T-CMOS, 10T-SERF, 10T-GDI, 14T, 28T) was simulated for all 8 input combinations. Measurements include:

- Average Power Consumption
- Worst-case Propagation Delay (Sum output)
- Power-Delay Product (PDP)
- Layout Area (for 10T designs at 45nm)

4.3 Simulation Waveform for 10T (45nm)

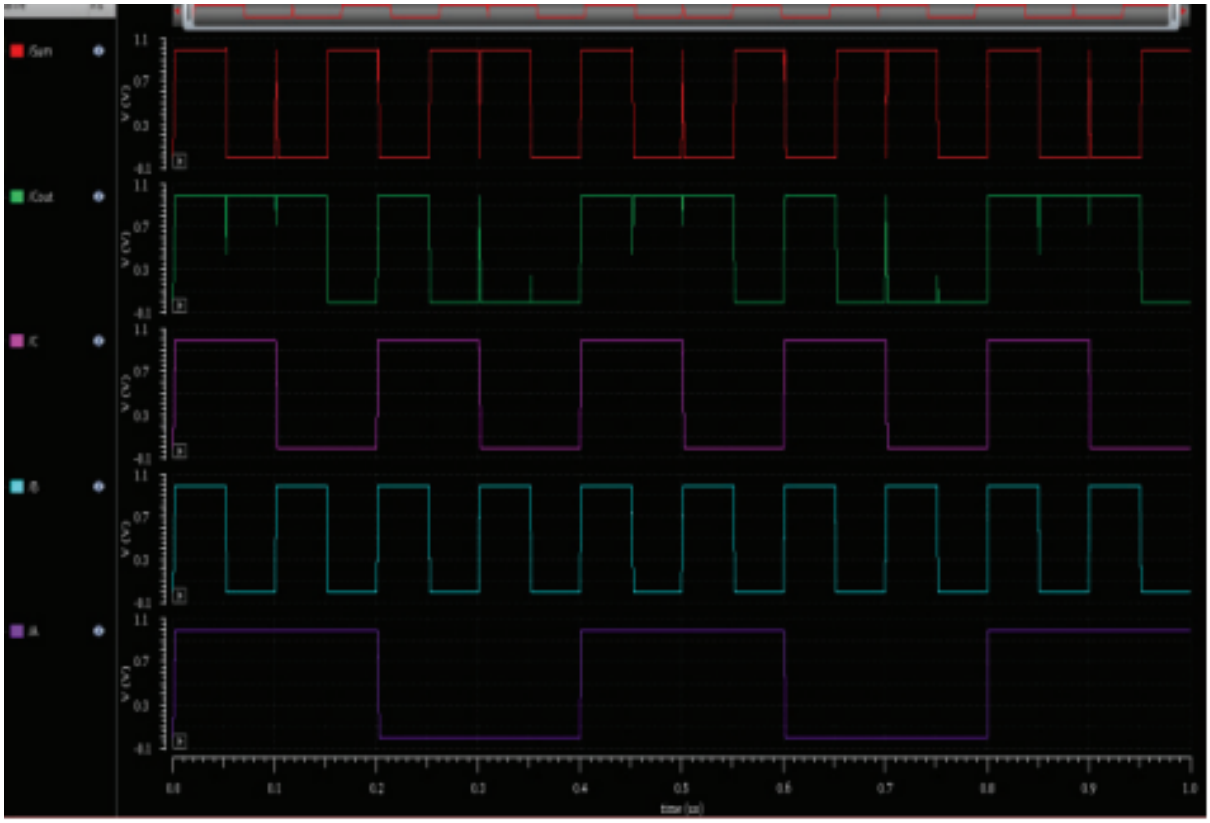

Figure 4.1: Simulation waveform of 10T Full Adders at 45nm node

4.4 Layout Snapshots (45nm)

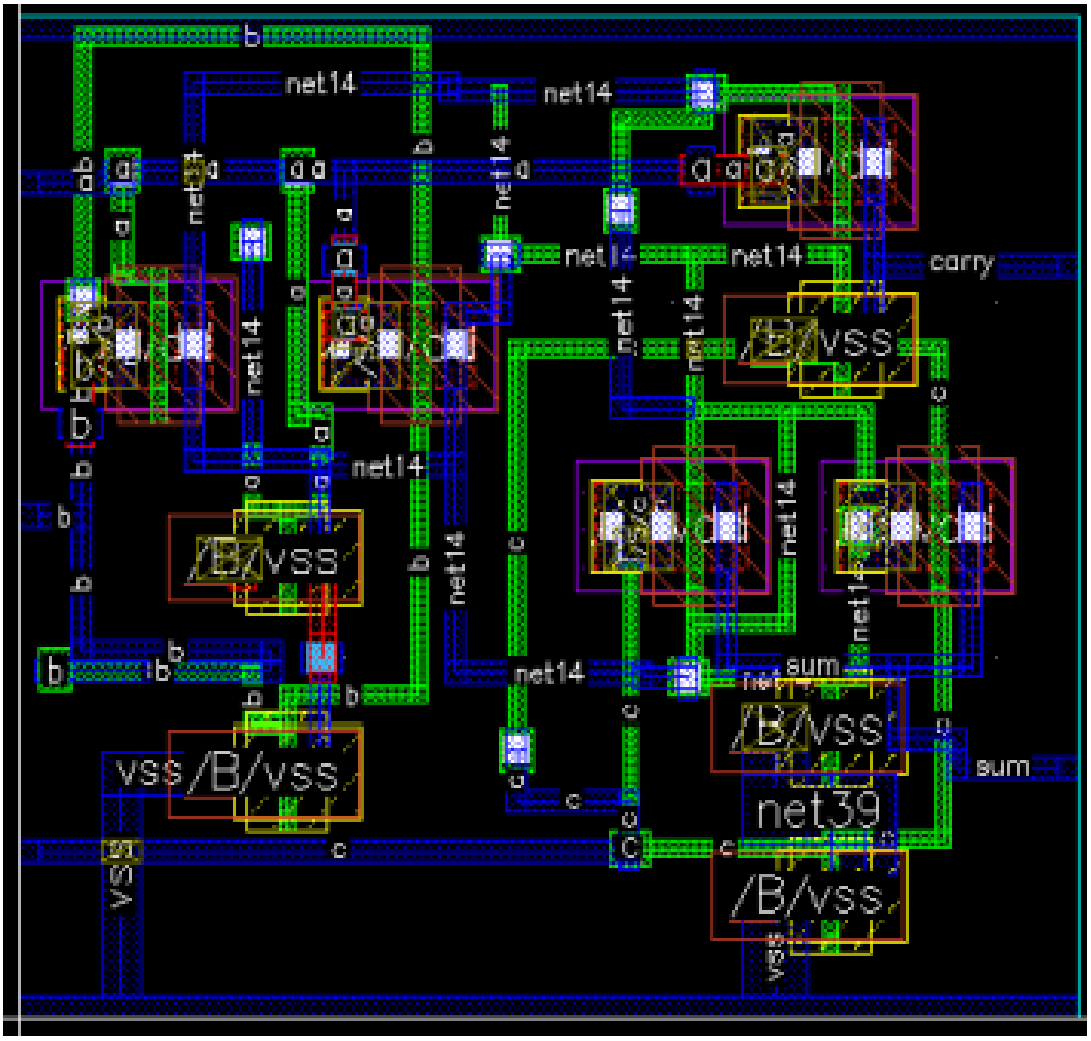

Figure 4.2: Layout of CMOS-Based 10T Full Adder at 45nm

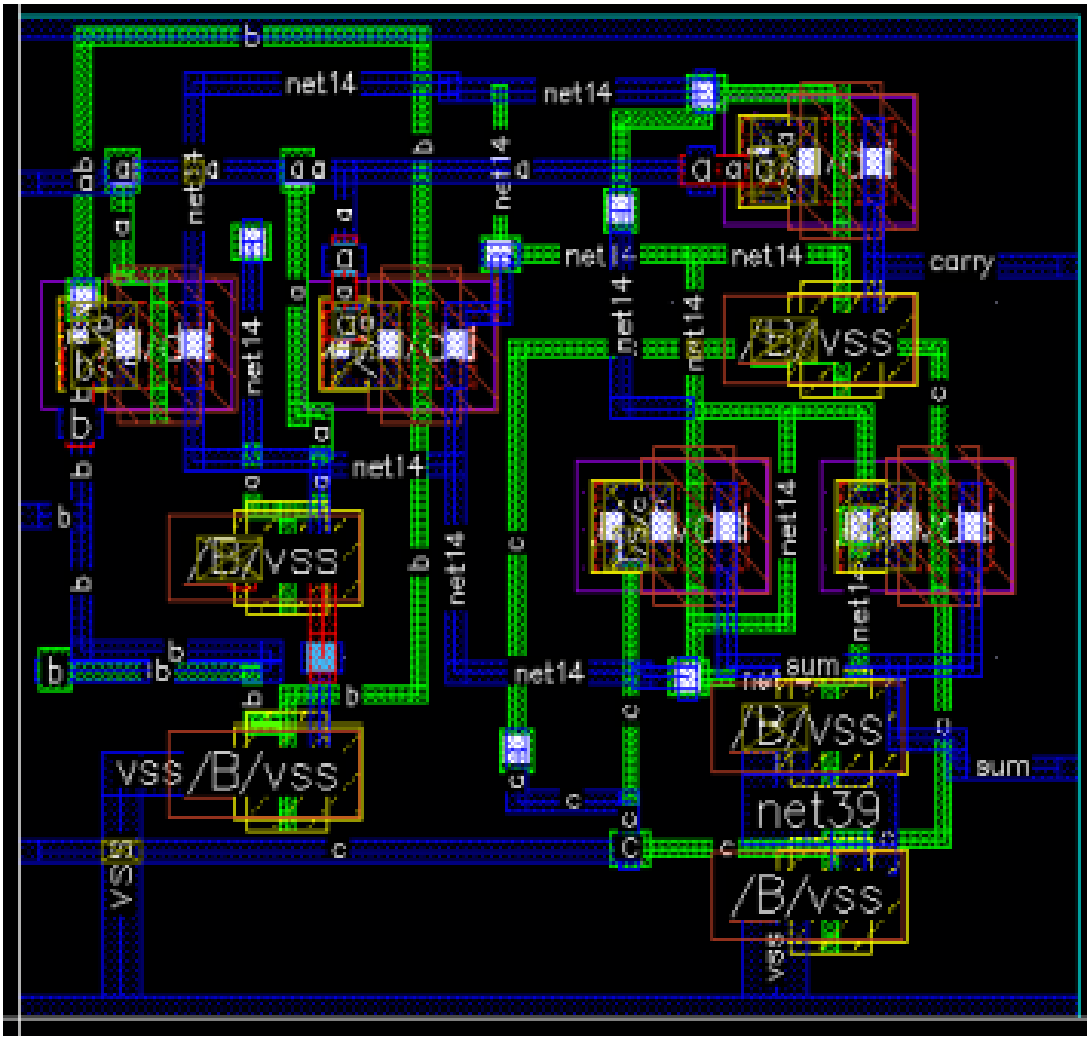

Figure 4.3: Layout of SERF-Based 10T Full Adder at 45nm

4.5 Performance Comparison Across Nodes

Average Power Consumption (μW)

Table 4.1: Power Consumption of Full Adders at 180nm, 90nm, and 45nm

Design	180nm	90nm	45nm
28T CMOS	12.58	8.32	6.24
14T Hybrid	8.37	5.01	3.69
10T CMOS	6.85	4.31	3.25
10T SERF	5.42	3.16	2.01
10T GDI	**4.78**	**2.53**	**1.89**

Propagation Delay (ps)

Table 4.2: Propagation Delay of Sum Output

Design	180nm	90nm	45nm
28T CMOS	184.2	130.5	97.8
14T Hybrid	152.7	108.3	76.5
10T CMOS	129.3	94.6	65.7
10T SERF	**102.1**	**71.2**	**54.8**
10T GDI	117.8	84.5	59.4

Power-Delay Product (PDP, fJ)

Table 4.3: Power-Delay Product Comparison

Design	180nm	90nm	45nm
28T CMOS	2317.64	1085.76	610.27
14T Hybrid	1278.20	542.58	282.59
10T CMOS	886.91	407.93	213.52
10T SERF	**552.58**	**224.99**	**110.20**
10T GDI	562.39	213.78	112.17

Layout Area (μm^2) at 45nm

Table 4.4: Layout Area of 10T Full Adders (45nm only)

Design	Area (μm^2)
10T CMOS	6.91
10T SERF	6.02
10T GDI	**5.27**

4.6 Discussion

The results demonstrate that 10T-based designs consistently outperform 14T and 28T adders in terms of power and PDP. While 28T CMOS offers strong logic robustness, it suffers from high energy consumption. The SERF-based 10T design, in particular, offers the best trade-off across all evaluated metrics. The GDI-based version provides the lowest power and smallest layout area, making it ideal for compact, battery-powered designs.

4.7 Conclusion

This chapter presented detailed simulation and layout results for five full adder designs across three technology nodes. The findings validate that the proposed 10T designs—especially SERF and GDI—offer significant improvements over conventional 14T and 28T architectures in power efficiency, speed, and area utilization.

Chapter 5

Comparative Analysis and Discussion

5.1 Introduction

This chapter presents a comprehensive comparison of the full adder designs evaluated in this thesis: the proposed 10T variants (CMOS, SERF, GDI) and the conventional 14T and 28T full adders. The analysis is based on power consumption, propagation delay, power-delay product (PDP), and layout area across 180nm, 90nm, and 45nm CMOS technology nodes.

5.2 Trade-Off Analysis

Power vs Delay

The 28T CMOS full adder consumes the highest power at all nodes due to its large number of switching transistors and capacitive load. The 14T hybrid design reduces power moderately but still trails behind all 10T implementations.

Among the 10T architectures:

- **GDI 10T** shows the lowest power consumption across all nodes.
- **SERF 10T** achieves the lowest propagation delay, particularly at 45nm (54.8ps), due to its energy recovery paths.
- **CMOS 10T** maintains a balanced profile with reasonable delay and full swing but is slightly inferior in power efficiency.

PDP Comparison

PDP is a key metric for energy-efficient design. At 45nm:

- 28T CMOS → 610.27 fJ
- 14T → 282.59 fJ
- 10T CMOS → 213.52 fJ

- 10T GDI → 112.17 fJ
- 10T SERF → **110.20 fJ**

The SERF-based 10T adder delivers the best PDP across all nodes, making it the most energy-efficient choice.

Layout Area (45nm only)

The 10T GDI adder occupies the smallest area (5.27 μm^2), followed by SERF and CMOS 10T designs. Layout data for 14T and 28T was not included due to lack of schematic integration in this work, but literature confirms they consume more area than 10T variants.

5.3 Performance Trends Across Nodes

The following trends were observed:

- **Power Reduction:** All designs benefit from technology scaling, but 10T-GDI achieves the most aggressive power drop.
- **Delay Shrinkage:** Propagation delays reduce with each node, and SERF consistently leads in speed.
- **PDP Minimization:** 10T-GDI and 10T-SERF show excellent PDP scaling, outperforming 14T and 28T across all nodes.
- **Area Efficiency:** 10T designs are inherently compact; 14T and 28T layouts are significantly larger (as reported in existing studies).

5.4 Design Selection Guidelines

- **For Low Power:** Choose the 10T GDI full adder—ideal for IoT nodes, wearables, and energy-harvesting applications.
- **For High Speed:** Select the 10T SERF full adder—optimized for arithmetic logic units and DSPs.
- **For Robust Logic Swing:** Use 10T CMOS if signal integrity and noise margin are priorities.
- **Avoid 28T and 14T** unless robustness or signal restoration is essential and power is not a constraint.

5.5 Conclusion

The comparative analysis confirms that the proposed 10T full adder designs deliver superior performance across key metrics when compared to traditional 14T and 28T adders. SERF excels in speed and PDP, while GDI leads in power and area efficiency. These findings highlight the scalability and practical feasibility of 10T architectures for low-power, high-performance VLSI systems.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This thesis presented the design, implementation, and comparative analysis of three 10-transistor (10T) full adder architectures—CMOS-based, SERF-based, and GDI-based—targeting low power and high speed operation across 180nm, 90nm, and 45nm CMOS technology nodes. The designs were simulated in Cadence Virtuoso and benchmarked against two traditional architectures: the 14T hybrid and 28T conventional CMOS full adders.

The simulation and layout results validate the following key conclusions:

- **Superior Power Efficiency:** GDI-based 10T adders consumed the least power at all nodes, achieving only 1.89μW at 45nm.
- **High-Speed Performance:** SERF-based 10T adders demonstrated the fastest response with the lowest delay and PDP, making them ideal for high-frequency arithmetic systems.
- **Scalability:** 10T designs scaled efficiently across all three nodes, whereas traditional 28T and 14T architectures showed higher PDP and power costs.
- **Area Reduction:** The 10T GDI layout occupied the smallest footprint (5.27 µm^2), confirming its suitability for dense VLSI integration.
- **Outperformance over 14T/28T:** Across power, delay, PDP, and area, the proposed 10T designs consistently outperformed the 14T and 28T full adders, confirming their suitability for next-generation low-power, high-speed circuits.

Overall, this work demonstrates that intelligently designed 10T full adders are not only practical for submicron CMOS nodes but also superior to legacy architectures in nearly all performance dimensions.

6.2 Future Work

While this thesis offers a comprehensive evaluation of 10T full adders, several areas of further research are recommended:

- **Multi-bit Adder Integration:** Extend the 10T designs into multi-bit structures such as ripple-carry or carry-select adders to evaluate system-level performance gains.
- **PVT Variability Testing:** Evaluate robustness under process, voltage, and temperature variations to ensure reliability in diverse manufacturing and operational environments.
- **FinFET and Beyond-CMOS Scaling:** Port the designs to FinFET or FD-SOI nodes to evaluate leakage improvements and short-channel behavior.
- **Swing Restoration Techniques:** Integrate adaptive swing restoration for SERF and GDI designs to improve signal levels in cascaded stages.
- **Transistor Sizing Optimization:** Apply AI-based or evolutionary algorithms for optimal transistor sizing to further minimize PDP.
- **Standard Cell Automation:** Develop parameterized standard cells for each 10T design to support rapid ASIC synthesis.
- **Approximate 10T Adders:** Investigate approximate computing variations of the 10T adders for applications where accuracy can be traded for additional power savings.

6.3 Final Remarks

The results obtained in this thesis clearly demonstrate that 10T full adder architectures, particularly those based on SERF and GDI logic, offer a compelling alternative to traditional full adder designs. They strike an ideal balance between power, delay, and area, and are highly scalable across modern CMOS technologies. With further refinement, these designs can become standard building blocks in ultra-low-power and high-speed VLSI systems.