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Design of Gate Diffusion Input based energy efficient CNTFET circuits

A MAJOR PROJECT-II REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE AWARD OF THE DEGREE

Of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN AND EMBEDDED SYSTEM

Submitted BY

YASHODA PARMAR (23/VLS/25)

Under the supervisor of

PROF. NEETA PANDEY

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly DELHI COLLGE of Engineering)

Bawana Road, Delhi-110042

May, 2025

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

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CANDIDATE'S DECLARATION

I, Y**ashoda Parmar**, roll no: **2k23/vls/25** students of M.Tech VLSI design and Embedded system, hereby declare that the major project-II "**Design of Gate Diffusion Input based energy efficient CNTFET circuits**" which is submitted by me to the department of electronics and communication, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of master of technology, is original and not copied from any source without proper citation. this work has not previously formed the basis for the award of any degree, diploma associateship, fellowship or other similar title or recognition.

Place: Delhi YASHODA PARMAR

Date: May 2025

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

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Bawana Road, Delhi-110042

CERTIFICATE

This is to certify that the Major Project-II **"Design of Gate Diffusion Input based energy efficient CNTFET circuits"** which is submitted by **YASHODA PARMAR**, Roll No: **2K23/VLS/25** Department of Electronics and Communication Engineering, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date: May 2025

Dr. NEETA PANDEY

PROFESSOR (ECE)

Delhi Technological University

ABSTRACT

An extensive examination of low-power digital circuit design utilizing Gate Diffusion Input (GDI) and its dynamic extensions—DGDI, DTGDI, and DMGDI cells—is presented in this major project-II report. A transient simulation of the XOR logic gate, full adders, ripple carry adder (RCA), and 2×2 multiplier is conducted using the Gate Diffusion Input (GDI) technique and its variations, namely DGDI, DTGDI, and DMGDI.

The DGDI which is a merger of basic GDI cell and novel dynamic logic block. It was investigated because of the drawbacks of GDI, such as insufficient output swing and excessive delay in intricate circuits. DGDI improves performance by enhancing swing characteristics. When GDI- and DGDI- based full adders are compared, it is shown that the former significantly reduces latency while the latter increases power consumption because of its greater transistor count. However, the lower output swing at the input of dynamic block leads to lower driving capability of the transistor and hence results in higher delay.

To resolve the issue in DGDI cell, the DTGDI cell is suggested. This cell Improved latency and power efficiency, which make them competitive substitutes for intricate arithmetic processes like ripple carry multipliers and adders. Comprehensive simulations using Cadence Virtuoso based on a 32nm node evaluated the performance parameters of DGDI and DTGDI cells utilizing quantitative measurements of delay, power consumption, and power-delay product (PDP) for different circuit topologies. The DTGDI-based XOR gate was shown to be 23.6% quicker than DGDI. DGDI and DTGDI have typical power consumptions of 1.62 µW and 1.54 µW, respectively. The findings confirm the advantages of integrating dynamic logic into GDI-based designs, paving the way for more efficient, low-power digital systems.

Furthermore, three transistors are used to implement XOR logic in a static logic-based MGDI cell. Compared to a GDI cell, it employs one fewer transistor since the MGDI cell implementation does not use the inverting input. As a result, the dynamic cell that is produced using MGDI, known as DMGDI, also has improved performance metrics.

Acknowledgement

First and foremost, I am indebted to GOD almighty for allowing me to excel in my effort to complete this major project on time. I am extremely grateful to express my gratitude and thankfulness to my respected guide Dr. Neeta Pandey for encouraging me to always work hard and pursue the task at hand with utmost diligence and for giving invaluable help, guidance, and motivation during the Major Project-II.

Yashoda Parmar

(23/VLS/25)

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LIST OF SYMBOL, ABBREVIATION AND NOMENCLATURE

Symbols

- ⊕- XOR Logic
- Θ- XNOR logic
- µ- Micro

Abbreviations

- GDI- Gate Diffusion Input
- DGDI- Dynamic Gate Diffusion Input
- DTGDI- Dynamic Transmission Gate Diffusion Input
- DMGDI- Dynamic modified Gate Diffusion Input
- TGDI- Transmission Gate Diffusion Input
- PDP- Product of delay and power consumption
- RCA- Ripple Carry Adder

Nomenclature

- Logic Gate
- Full adder
- RCA (Ripple carry adder)
- Multiplier

Chapter 1: Introduction

Low-power the explosion of associated activity in the engineering and scientific community indicates that VLSI design has garnered attention in recent years. Until the market shifts to portable consumer gadgets, low power has mostly been ignored. Subsequently, the mass-market digital design presents low-power issues. In addition to the need for mobility, per-chip power consumption has been steadily rising as a result of advancements in semiconductor process technology. According to Moore's Law, an integrated circuits (IC) transistor counts doubles roughly every two years. As a result, a VLSI chip's power consumption is anticipated to increase above its existing level. Additionally, the low power requirements on the techno-political front are a result of environmental concerns regarding the energy use of workplace computer equipment.

The power dissipation issue cannot be resolved in every application area by a single method. Furthermore, power efficiency cannot be attained without compromising the design's other metrics of merit. Power, latency, and transistor count must all be traded off in order to optimize power. To design in accordance with the intended standards, the extensive effects on every area must be examined.

Leakage power may be minimized in a variety of methods. These include the sleepy stack strategy, leaky feedback approach, sleepy keeper approach, sleep mode approach, and stack approach [1]. We can maximize the power in digital circuits by adjusting a number of factors. Switching voltage, capacitance, switching frequency, and leakage current may all be decreased to lower the power [2]. Other methods for designing low-power [3] VLSIs other than Gate Diffusion Input (GDI) cells exist.

1.1 Low Power Techniques

1.1.1 Clock Gating

15

By optimizing enable flops into a clock gating structure during logic synthesis, this strategy often saves mux space and lowers the clock net's total switching activity (Fig. 1.1). In terms of the power equation, the objective is to lower activity factors and capacitive load (by reducing area), which lowers the dynamic power's switching power component. This is a very easy and accessible method of cutting area and power. To carry out this optimization, it does, however, depend on the logic synthesis tool. Thankfully, the majority of tools and processes support this well-known method.

1.1.2 Multiple Voltage Thresholds (Multi-Vt)

This method divides a chip's functionalities according to its performance attributes. As seen in Fig. 1.2, it is possible that one block has a high performance while the remainder of the chip has a lesser performance. While a lower voltage can be utilized to conserve electricity on the lesser-performance blocks, a greater voltage is usually needed to meet the objectives for the high-performance block. This replaces the simpler but more power-intensive design of the whole block at the higher voltage. Every static and dynamic power component in the power equation reduces as the voltage is decreased.

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The challenge of designing in distinct voltage islands with multi-voltage designs is that voltage crosses between islands may necessitate "level shifter" (LS) cells, which must implement and analysis the blocks at their different voltage characteristics

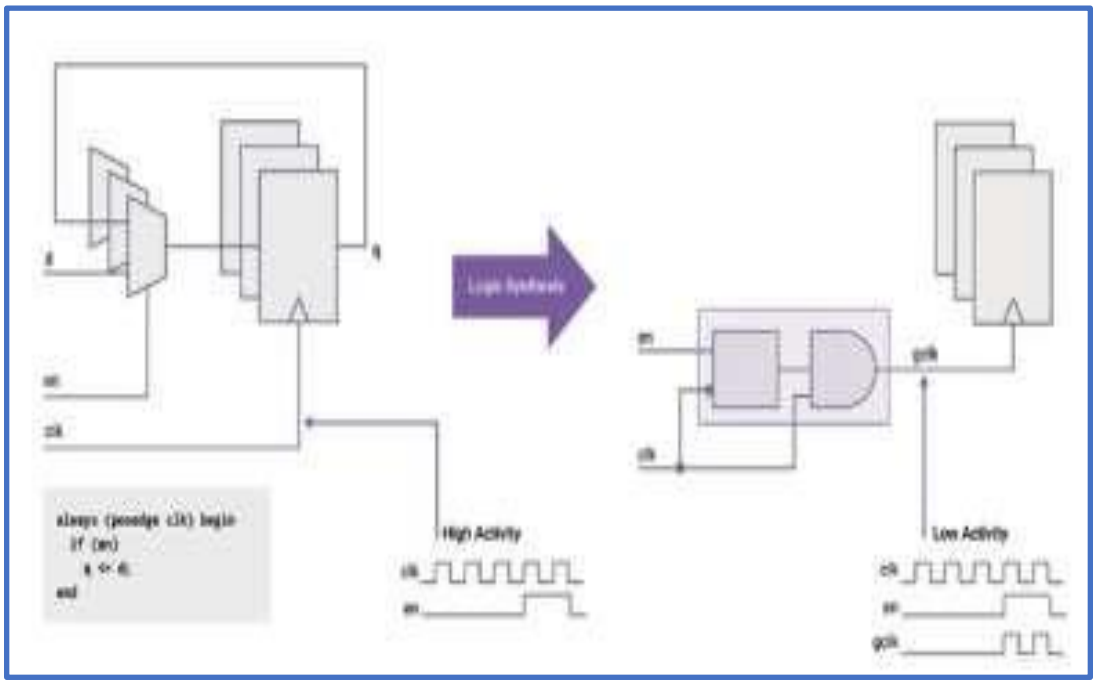


Fig. 1.1: Clock Grating

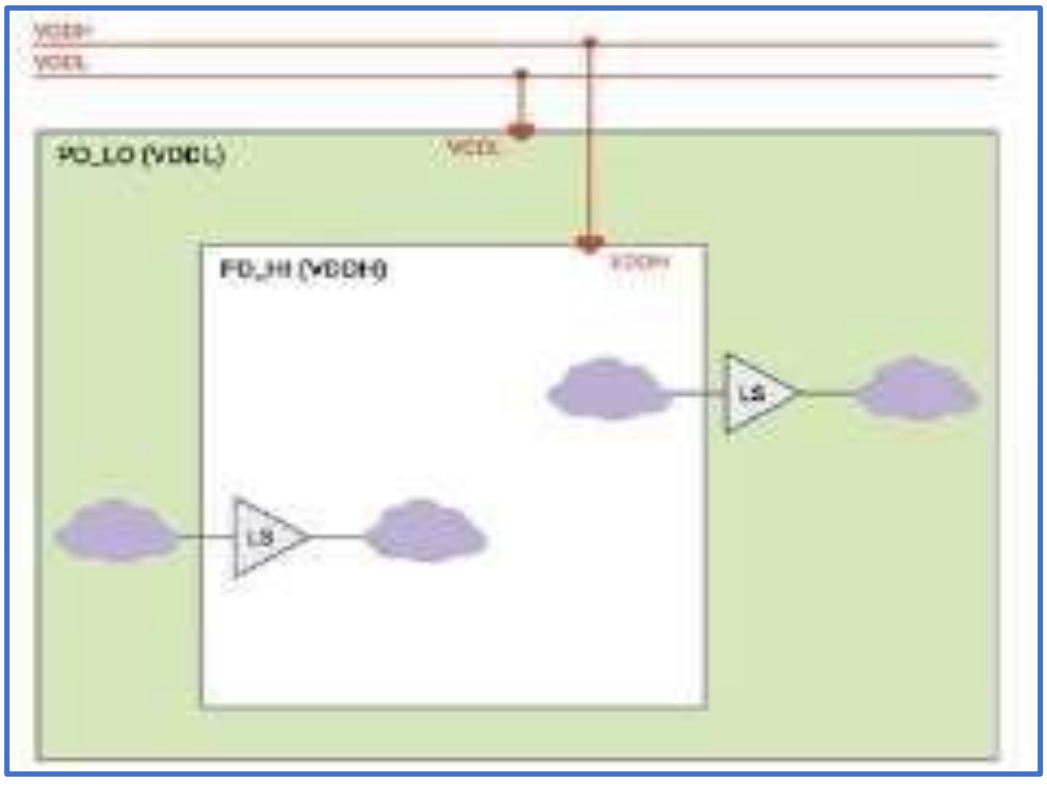


Fig 1.2: Multiple Voltage Threshold

1.1.3 Dynamic Voltage and Frequency Scaling (DVFS)

This method saves power by dynamically adjusting the voltage and frequency according to the computing needs, as seen in Fig.1. 3. In order to maximize power savings when such resources are not required and optimize resource allocation for jobs, dynamic voltage and frequency scaling, or DVFS, modifies the power and speed settings on a computer device's multiple CPUs, controller chips, and peripheral devices.

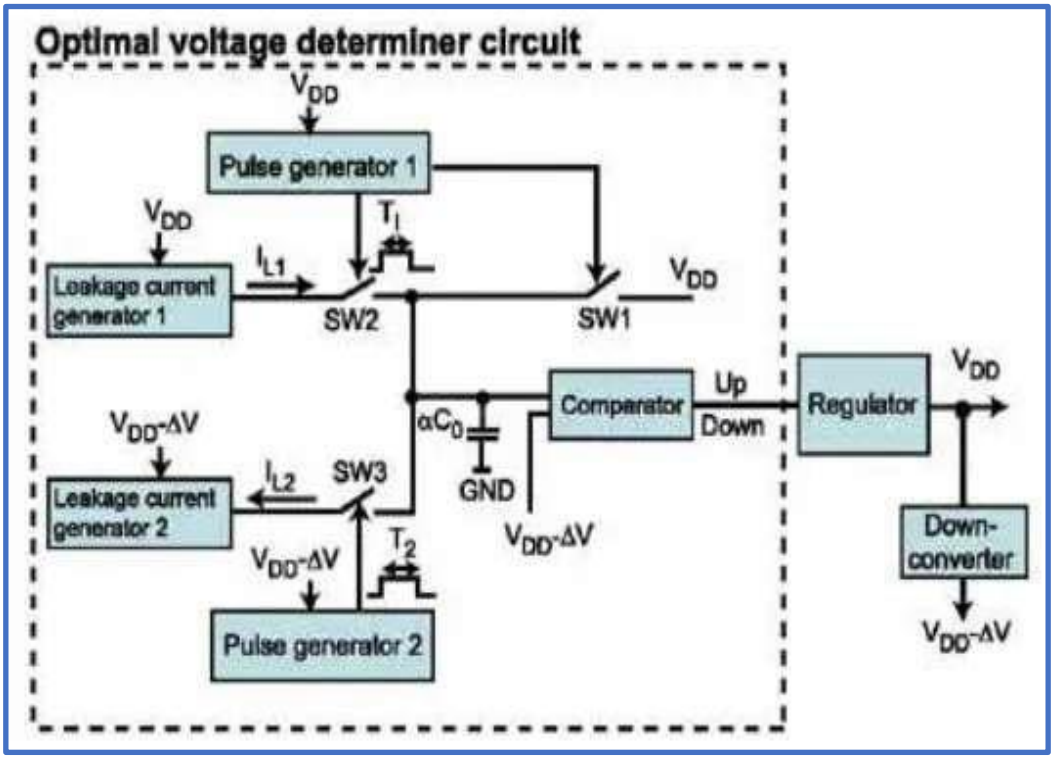


Fig. 1.3: Dynamic Voltage Frequency Scaling

1.1.4 Adaptive Voltage and Frequency Scaling (AVFS):

Like DVFS, AVFS similarly modifies the voltage and frequency, but it does so in response to changes in the process and operating circumstances. Many processors employ a technique called Adaptive Voltage and Frequency Scaling (AVFS) to modify power and performance in accordance with the demands of the job at hand. The voltage levels of the targeted power domains are scaled in defined discrete voltage steps in this modification of DVFS. The voltage-scaling power supply and the delay-sensing performance monitor on the SoC are connected via a closed-loop feedback mechanism in AVFS. In addition to seeing the actual voltage provided on-chip, the on-chip performance monitor can determine if the silicon is slow, normal, or quick, as well as the impact of the surrounding silicon's temperature.

1.1.5 Power Gating

This method divides an IC's functions similarly to multi-voltage, however in this case, power switches are used to link the power supply for the power domains, as seen in Fig. 1.4. For a block, power gating basically cuts off all power. This eliminates power and zeroes out the voltage in the power equation, saving both static and dynamic energy during the block's off-time. It is optimal to shut down as many domains as possible, as frequently as possible, while preserving functioning, as power gating usually provides the most aggressive power reductions. To accomplish this power savings through power gating, the design must have power switches, which calls for isolation gates that clamp the boundaries of the power domain to known values when off.

Consideration must be given to the design's power states and the combination of ON and OFF states for the specified voltages. Finally, it is necessary to create a power management unit (PMU) that regulates the isolation enable signals and power switch. For the values during shutdown to be clamped to the appropriate values at the appropriate moment, the sequence of these signals during power down and power up must be precise.

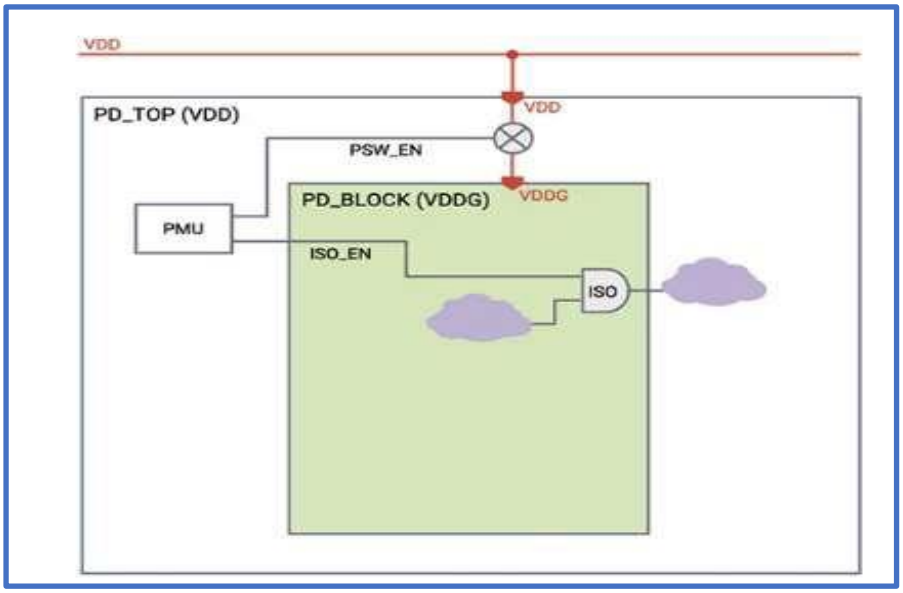


Fig. 1.4: Power Grating

a. **Use of Specialized Low Power Library Cells:** These are special cells designed with low power consumption in mind.
b. **Algorithmic-Level Power Reduction:** This involves optimizing the algorithm used in the design to reduce power consumption.
c. **Technology Mapping:** The objective of this decomposition is to minimize the total power dissipation by reducing the total switching activity.
d. **Glitching Power Reduction:** A design with more balanced delay paths has

fewer glitches, and thus has less power dissipation.

1.2 Motivation

Power consumption becomes a crucial factor in the design of CMOS VLSI circuits as technology advances to submicron processes. The need for fast speed, small implementation, and low power consumption has led to a lot of research efforts due to technological advancements and the quick growth of portable digital applications [4], [5]. To maximize different factors, other design approaches like PTL and CMOS [6] are recommended. Several design strategies are offered to improve power dissipation [7]–[9].

GDI is one such method. GDI makes it possible to implement circuits with fewer transistors, which reduces size, delay, and ultimately power consumption. Power dissipation in any circuit is dependent on two fundamental elements. The first is known as static power dissipation, which mostly results from leakage current or from the current continuously drawn from the power source. The second is known as dynamic power dissipation, which results from switching transients, or the charging and discharging of the load capacitances.

In terms of low power, low current, excellent linearity, and minimal leakage, the GDI cell with CNFET implementations offer even greater advantages. In contrast to the conventional MOSFET construction, which uses bulk silicon as the channel material, a carbon nanotube field-effect transistor (CNTFET) uses a single carbon nanotube (CNT) or an array of CNTs. Since CNTFETs were originally exhibited in 2008, significant advancements have been made [10][11].

Moore's law states that every two years, the size of the individual components in an integrated circuit has shrunk by a factor of around two. Since the late 20th century, technical advancements have been propelled by this gadget downsizing. However, when the essential size decreased to the sub-22 nm region, further scaling down has encountered significant limitations pertaining to fabrication technique and device performance, as the ITRS 2009 edition points out. Limits include short channel effects, passive power dissipation, leakage currents, electron tunnelling via thin insulator coatings and short channels, and changes in doping and device construction. Changing the channel material in the conventional bulk MOSFET structure with a single carbon nanotube or an array of carbon nanotubes can partially eliminate these limitations and enable further device size reduction.

The bandgap of a carbon nanotube is directly related to its diameter and chiral angle. If such properties could be controlled, carbon nanotubes (CNTs) would be a good choice for next-generation nanoscale transistor devices. In CNT–metal contacts, which are composed of metals such as silver, titanium, palladium, and aluminium, the distinct work functions of the metal and the CNT provide a Schottky barrier at the source and drain. Quantum mechanical tunnelling via the Schottky barrier dominates the carrier transport through the metal-CNT interface, despite the fact that, like Schottky barrier diodes, the

barriers would have limited the kind of carrier that this FET could have transported. A significant current contribution may be obtained by tunnelling via CNTFETs, which are readily thinned by the gate field.

Because CNTFETs (Fig.1.5) are ambipolar, it is possible to inject either electrons or hol es, or both at once. Because of this, the Schottky barrier's thickness is crucial.

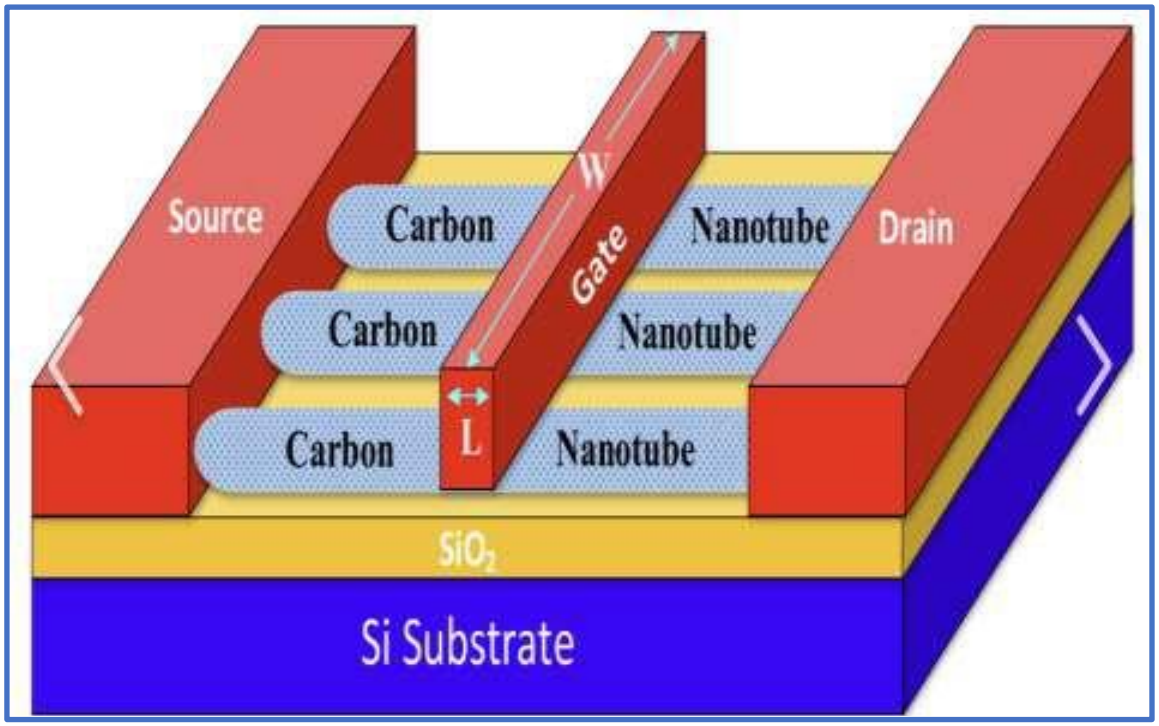


Fig. 1.5: CNTFET Device

The drain current of CNTFETs rises as the applied gate voltage grows in magnitude, conducting electrons when a positive bias is supplied to the gate and holes when a negative bias is applied. Due to the equal contributions of electrons and holes, the current reaches its lowest at Vg = Vds/2. The drain current rises as the drain bias rises, just like with other FETs, unless the applied gate voltage falls below the threshold value.

A FET with a shorter channel length provides a larger saturation current in planar CNTFETs with different design parameters, while a FET with a smaller diameter but the same length also produces a higher saturation drain current. Because a CNT is surrounded by an oxide layer, which is subsequently surrounded by a metal contact that serves as the gate terminal, it is clear that cylindrical CNTFETs drive a higher drain current than planar CNTFETs.

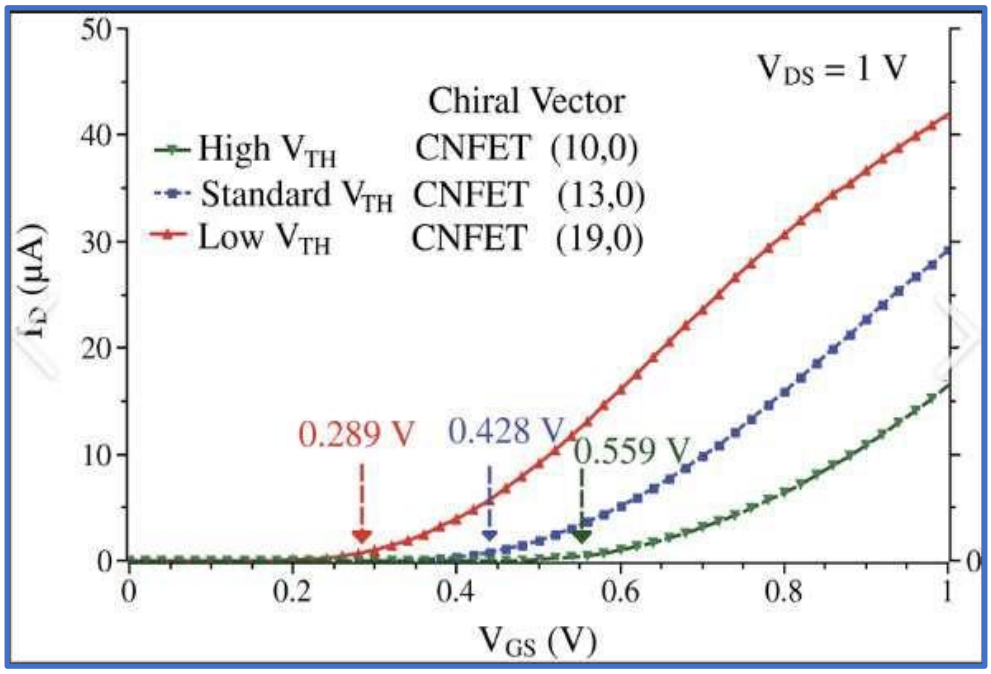


Fig. 1.6: I-V Characteristic of CNTFET

1.3 Objective

The C-GDI cell is a low-power circuit design described in this paper that uses dynamic gate diffusion input (GDI) technology in carbon nanotube field-effect transistor (CNTFET) technology. With fewer transistors and a simpler circuit, the GDI approach provides low power, whereas CNTFET technology provides minimal short channel effect (SCE). The GDI approach is used to build a full adder based on XOR gates, and performance analysis is performed for a number of metrics, including power consumption, latency, and power delay product (PDP). In comparison to traditional CMOS-based NAND gate circuits, the results demonstrate that XOR-based circuits based on dynamic GDI, which were utilized to create the entire adder circuit, have low power and short latency.

Additionally, because GDI's output swing is insufficient, several methods such as D-GDI, D-TGDI, and D-MGDI will be examined in the upcoming chapters to address this issue. The implementation of all the approaches began with XOR logic gates and progressed to **full** adders, ripple carry adders, and multiplier circuits. Every circuit's performance metrics, including latency, power consumption, and PDP, were assessed and contrasted. Additionally, the impact of supply voltage fluctuation and load capacitance was examined to make sure The DGDI cell's process variation analysis was also completed for this report; observe how changes in Vdc and capacitance affect the output.

1.4 Project Organizations

There were five chapters in the report. Chapter 1 introduces the project's purpose, motivation, and low-power methodology.

Chapter 2, Combinational circuitry based on GDI-Based Circuit, introduces the GDI cell. We looked at the transient behavior of the circuit and found that it is working. The transient nature of the GDI cell demonstrated and to evaluate the reliability of the GDI, a number of circuits based on it have been simulated. Logic such as AND, OR, and the p-equivalent of the AND gate are constructed using three CNFET-based devices. All of the successfully imitated logic's transient behavior is reported in this chapter. Furthermore, a simulation of the GDI-based full adder was conducted.

The DGDI cell was examined in Chapter 3 as well, and it was used to validate the XOR gate's logic. The entire swing is now in the DGDI cell. The DGDI cell is also developing a full adder circuit as a result of its advantage over the GDI cell. The full adder circuit's power consumption and latency are examined in comparison to the full adder based on the GDI cell. Moreover, multiplier circuits and the RCA are implemented using the DGDI cell.

In Chapter 4, the DTGDI cell was also examined, and it was used to validate the XOR gate's logic. Since the DTGDI cell has achieved full swing even at the intermittent node, DTGDI has a lower latency than DGDI. DTGDI is much better than DGDI because of this benefit. Additionally, the DGDI-based circuitry is compared to the XOR logic gate, full adder circuit, RCA, and multiplier to examine their power consumption and latency.

In Chapter 5, DMGDI cell also analyzed and all the logic of XOR gate were verified through the DMGDI cell. DMGDI cell has obtained the full swing. Because of this advantage of DMGDI over the GDI cell, full adder circuit is being also developed by the DMGDI cell. Delay and power consumption of the full adder circuit is analyzed as compared to the full adder based on the GDI cell. Further, DGDI cell is used to implement the RCA as well as multiplier circuitry.

In chapter 6, all of the techniques were compared. It was shown that DTGDI cells are better, as same can be configurable and also have superior performance parameters than DGDI and GDI. Although the performance of the DMGDI cell is likewise superior, but this cell is not programmable.

Chapter 2: Combinational circuitry based on the GDI

C-GDI is a GDI cell that is based on the CNFET. In the Cadence Virtuoso, the cell has been simulated. First, examine the simulation's simple GDI cell, which consists of just two CNFET devices. The identical circuit's power use and delay were simulated. Results of the investigation showed that the basic GDI cell has limits with regard to complete swing and latency.

A well-known low-power design approach that drastically lowers the number of transistors required for logic gates is the Gate Diffusion Input (GDI) technique. This characteristic makes GDI particularly appropriate for uses like high-performance CPUs and portable devices where power economy is crucial. Applications such as microprocessors and Digital Signal Processor (DSP) designs depend heavily on full adders. High-throughput, low-power, and compact designs are required because to the increasing need for portable applications, which frequently have restricted power availability. Such advancements are very beneficial to addition, a basic and widely used arithmetic operation in digital circuit design.

The different fundamental cell-like AND, OR, and AND operations of Abar.B and AND operations of A.Bbar are likewise implemented using GDI methods. This report examines their transient behavior and analyzes its delay parameter. Through the circuit's transient response, full adders based on GDI approaches were also examined.

2.1 The GDI Cell

The GDI cell as shown in Fig. 2.1. With certain modifications, this cell is similar to a CMOS inverter. X (common gate of pMOS and nMOS transistors), Z (input to the source of the nMOS), Y (input to the source of pMOS transistor), and F_1 Out (common diffusion node for both transistors) are the four terminals of a GDI cell. Numerous logical statements and functions that a GDI cell may be used to implement. With GDI, same functionalities may be implemented with just two transistors, but with CMOS technology, they may require six to twelve transistors. Consequently, this lowers the circuitry's size, latency, and power consumption.

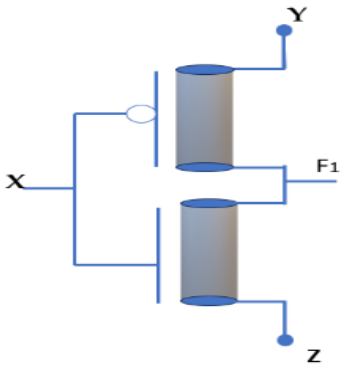


Fig 2.1: GDI Cell

The GDI is a novel technique [12] for designing low-power, area-efficient, and high-speed static combinational circuits. Additionally, the GDI technique helps in reducing circuit complexity and adds reconfigurability to the design. The schematic of the basic GDI cell is shown in Fig. 2.1. It is a three-input device, G, P and N. It explored only two devices to implement XOR and XNOR logic. Upon applying various input combinations enlisted in Table 2.1, different logic functions can be realized.

Table 2.1: Function Realizations using GDI with various combinations of inputs

X	Y	Z	OUT	Function	Issue of full swing	Logic confronts Inadequate Swing
X	Y	'1'	X+Y	OR	Present	00,10,11
X	Y'	'0'	X'Y'	NOR	Present	11
X	'0'	Z	XZ	AND	Present	00,01,11
X	'1'	Y'	(XY)'	NAND	Present	10
X	Y	Z	X'Y+XZ	MUX	Present	00,10
X	Y	Y'	X'Y+XY'	XOR	Present	00,10
X'	Y	Y'	X'Y'+XY	XNOR	Present	11, 01

2.1.1 Advantage of GDI technique

When designing digital integrated circuits, the Gate Diffusion Input (GDI) approach effectively minimizes both the layout space and power consumption. The CNEFT was used in the design and development of GDI cells because of its many benefits, which are listed below:

a. Reduced Delay: The GDI approach is appropriate for high-speed applications because to its reduced propagation delay. A quick circuit is necessary for a rapid arithmetic operation, and compact circuits reduce the delay effects of wires. These fast circuits can be implemented as part of a larger single-chip system to minimize input/output delays, and their small size indicates a single-chip implementation to minimize wire layers.

b. Reduced Transistor Count: With GDI, a large number of intricate logic operations may be implemented with just two transistors. As a consequence, there are fewer transistors than with conventional CMOS design and current Pass Transistor Logic (PTL) methods.

c. Decreased Area of Circuits: Due to the reduced transistor count, the area of digital circuits is also decreased.

d. Low Complexity of Designing: GDI technique makes the system design less complex.

e. High Performance: Low-power integrated circuits with high performance and great power density may be made with CNFETs. Their near-ballistic transport

characteristics and high carrier velocity make them ideal for FET devices.

f. Lower Power Consumption: Carbon nanotubes (CNTs) are used in CFETs to connect a MOSFET structure's source and drain. As a result, CNFETs can offer a greater driving current density due to increased current carrier mobility.

g. Improved control over channel formation: The diameter and chiral angle of a carbon nanotube directly impact its bandgap. CNFETs would be an excellent option for upcoming nanoscale transistor devices if these characteristics could be managed. Considerations for CNT Material: Control over channel creation may also be impacted by the CNT's material selection. For example, carbon nanotubes are chemically inert and capable of carrying high electric currents because to the strong covalent carbon–carbon bonding in the sp2 configuration.

h. Potential for Ultra-thin electronics: CNFETs have the potential for ultra-thin electronics because of their extremely tiny diameter (1-3 nm).

Better threshold voltage: Improving the threshold voltage in Carbon Nanotube Field-Effect Transistors (CNFETs) can be achieved through several methods:

a. Control of Chiral Angle and Diameter: A carbon nanotube's chiral angle and diameter influence its bandgap, which has a direct impact on the threshold voltage. Consequently, the threshold voltage may be raised by regulating these characteristics.

b. Adjusting the Diameter of Carbon Nanotubes (CNTs): The threshold voltage can be improved by adjusting the diameter of the CNTs in the CNFETs. Changing the Flat-Band Voltage of CNFET: Another method for adjusting the threshold voltages is changing the flat-band voltage of CNFET.

c. Low-Temperature Annealing: This airborne annealing process can efficiently enhance on-state current, boost mobility, and lower subthreshold swing and device threshold voltage.

d. High Linearity: One of the main characteristics of carbon nanotube field-effect transistors (CNFETs) that makes them appropriate for a range of applications is their high linearity. The high linearity of CNFETs is caused by ballistic Transport. Electrons are carried via the nanotubes in CNFETs without scattering after being injected from the source to the drain. Ballistic transport makes the nanotubes an ideal conductor for electrons, allowing for the lossless passage of all of the electrons' quantum information, including momentum, energy, and spin. Based on a 3D device simulation of both CNTs and contacts, many basic designs for the gate contact arrangement are taken into consideration. This aids in reaching high linearity and maximum speed. A large frequency response range and a very linear, wide, continuous tuning range are maintained using a novel high-performance OTA based on 32 nm CNFET devices.3. Better linearity is produced by a low-power, stable-frequency hybrid VS-CNTFET-CMOS VCO ring oscillator than by a traditional CMOS design.

e. Compatibility with High-K Dielectric Material: CNFETs are compatible with high-K dielectric material offering high ON currents.

f. Very Small Leakage Currents: CNFETs have very small leakage currents.

Cadence Virtuoso version 6.1.7 implements GDI cells on 64 bits. An effective tool for designing bespoke and analog integrated circuits (ICs) is Cadence Virtuoso. This Cadence application makes use of 30 years of industry expertise and competence in custom/analog design. It offers more comprehensive support for a range of systems, such as advanced heterogeneous designs, photonics, mixed-signal, and radio frequency.

A key component of the Virtuoso Studio platform, the Virtuoso ADE Suite is the industry's top tool for analyzing, verifying, and exploring analog, mixed-signal, and radio frequency designs. It tackles the performance issue of greatly for complete design, a higher simulation throughput is required.

In order to implement the circuits, a specific process must be followed in the cadence. The Virtuoso schematic editor is first used by designers to build schematics. This entails setting up parts, joining nets, and establishing the circuit. Next, mark the circuitry's input, output, and power supply. The user then configures simulations (such as transient, DC, and AC) to examine the behavior of the circuit. Transient studies were performed on every circuit in our investigation. Following the application of a pulse of varying length, the duty cycle and pulse width are provided. Following schematic verification, designers go on to layout design, where they construct actual circuit layouts. Consistency between the schematic and layout is ensured via parasitic extraction and layout vs. schematic (LVS) tests. To ensure layout conformity, DRC (design rule check) and LVS (layout vs. schematic) conducted physical verification. The tape-out step is the final step. The design is now prepared for production.

Despite the benefits of using the Gate Diffusion Input (GDI) approach to reduce the number of transistors in logic circuits, one notable disadvantage is that it does not give accomplish output signal swing. The intrinsic characteristics of P-type and N-type transistors are the cause of this restriction. For example, when a P-type transistor is used, the low logic level "0" at the circuit's output is restricted to |Vthp|, whereas the high logic level "1" through the N-type transistor is limited to Vdd - Vthn. The Table 2.2 displays the |Vthp| and |Vdd-Vthn| values.

This problem occurs because, similar to P-type transistors' inability to successfully transfer the "0" logic level, N-type transistors are unable to entirely communicate the "1" logic level. Consequently, the limited signal swing has a detrimental effect on the succeeding circuit stages' ability to function properly. A number of research projects [13] [14] suggest adding more P-type and N-type transistors to the traditional GDI gate arrangement in order to get around this problem. These additional transistors improve circuit functioning and provide a more thorough transfer of logic levels. Fig. 2.2 shows a comprehensive schematic of a GDI cell created in Cadence, providing a visual depiction of the suggested improvements.

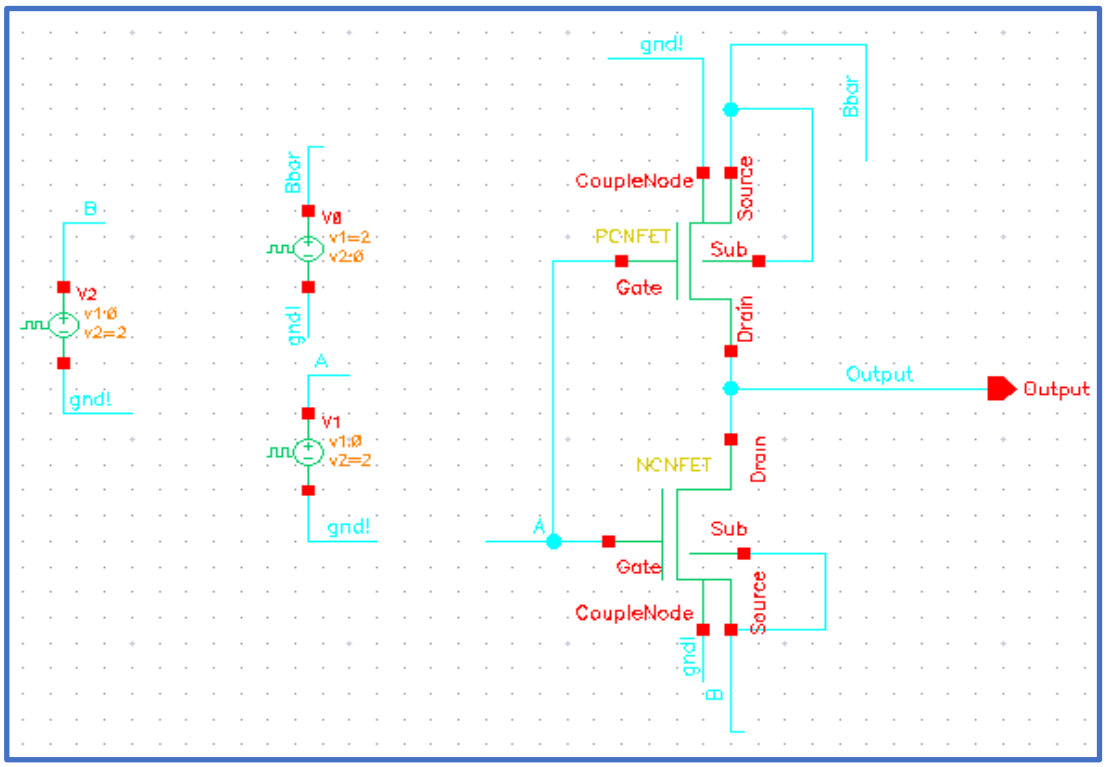


Fig. 2.2: Basic GDI Schematic in Cadence

Table 2.2: GDI Cell Output

G	N	P	Output at Node X
0	0	1	1.998V (Vdd)
0	1	0	173mV (Vtp)
1	0	1	0
1	1	0	1.84 V (Vdd-Vtp)

The Virtuoso cadence was used to demonstrate the GDI cell's transient nature. Both the signal at A and the signal at B have clock pulses with periods of 46ns and 23ns, respectively. The duty cycle of both signals is 50%. Both signals' pulse widths were maintained at 1.8V, with load capacitance of 10f F

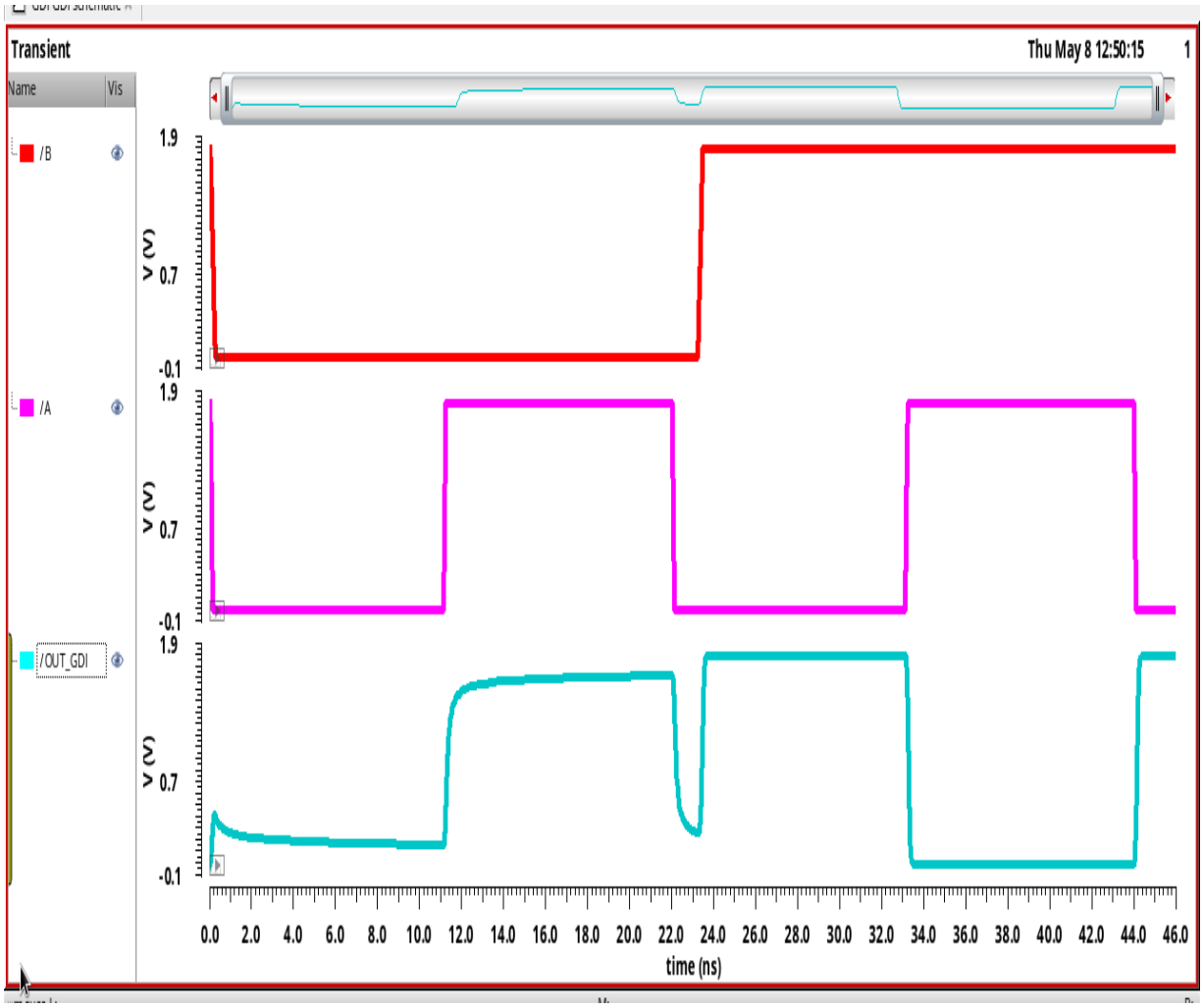


Fig. 2.3.a: Transient Response of GDI Cell

In Fig. 2.3.a, the transitory behaviour is shown. It guarantees that the XOR gate and GDI cell are implemented successfully. The zoom is shown in Fig. 2.3.b at 30-ns intervals, where signal A stays at A and signal B shifts from 1 to 0. The output value in this case settles after 133.1 ns when B changes its value, requiring 700 nW of electricity.

Different gate implementation using a GDI cell

The several circuits of based on GDI to realized different logic are created in Fig. 2.4 using GDI techniques. Logics like AND A.B, OR A+B, AND $\bar{A}$.B and AND A.$\bar{B}$ shown in Fig. 2.4.a, 2.4.b, 2.4.c, and 2.4.d respectively, was simulated in the cadence. Virtuoso. In this simulation, inputs A and B have durations of 10 and 15 ns, respectively, with a pulse width of 1.8 V and a 50% duty cycle.

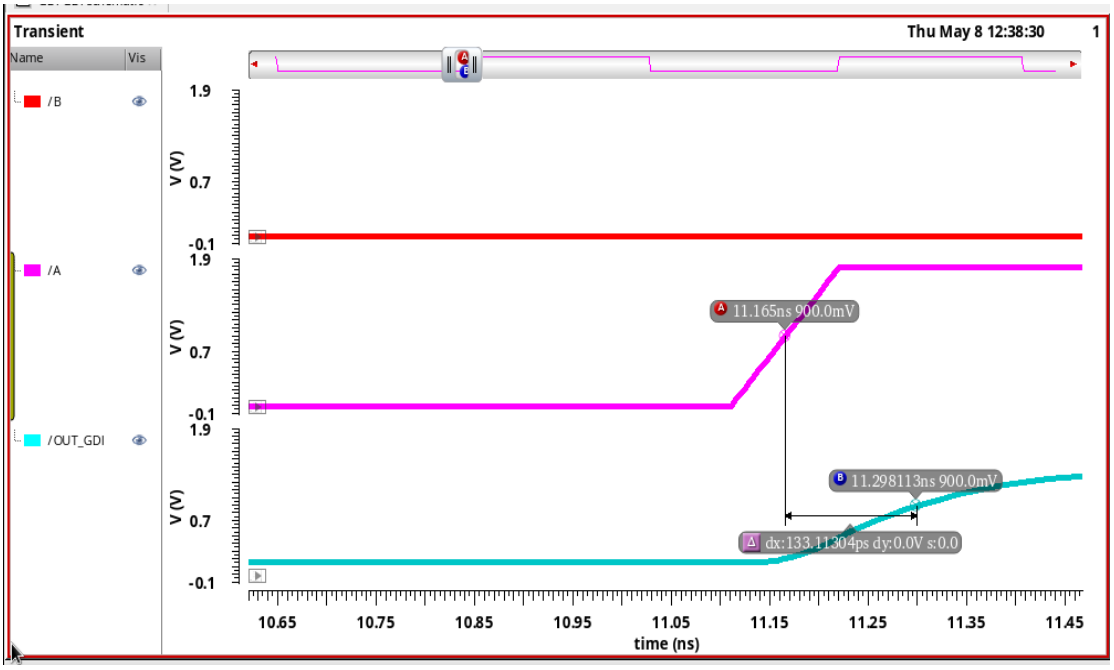


Fig. 2.3.b: Transient Response of GDI Cell for Delay Calculations

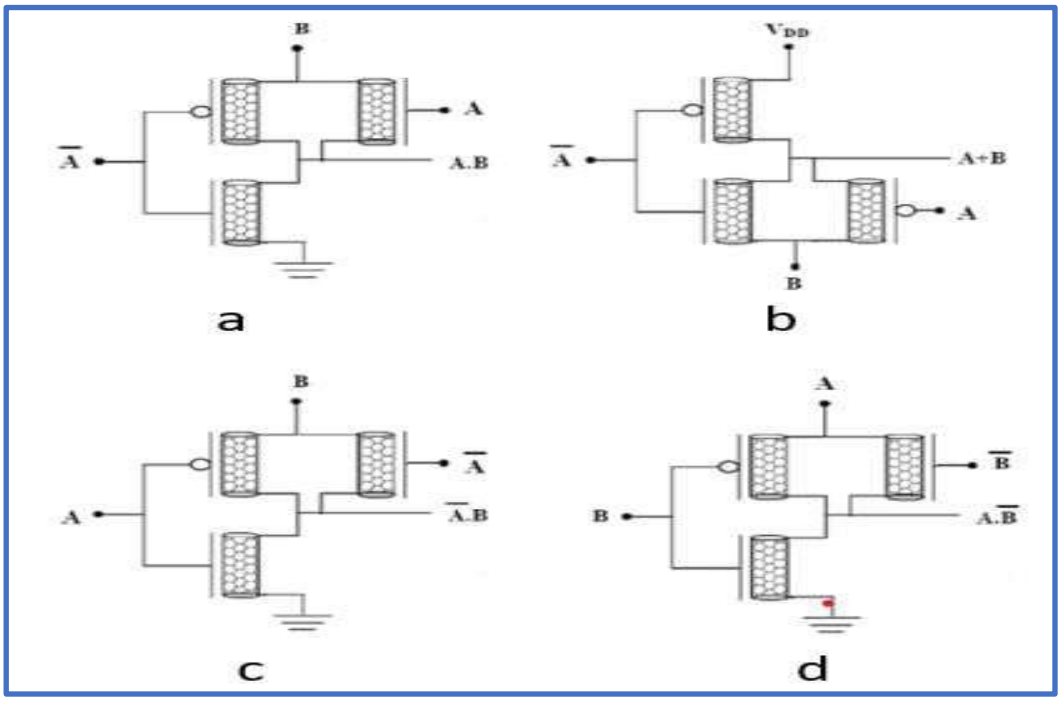


Fig. 2.4: Different Gate implementation using GDI cell [16]

a.i Implementations of AND gate

Fig. 2.5, shows the schematic of the AND gate based on the GDI cell.

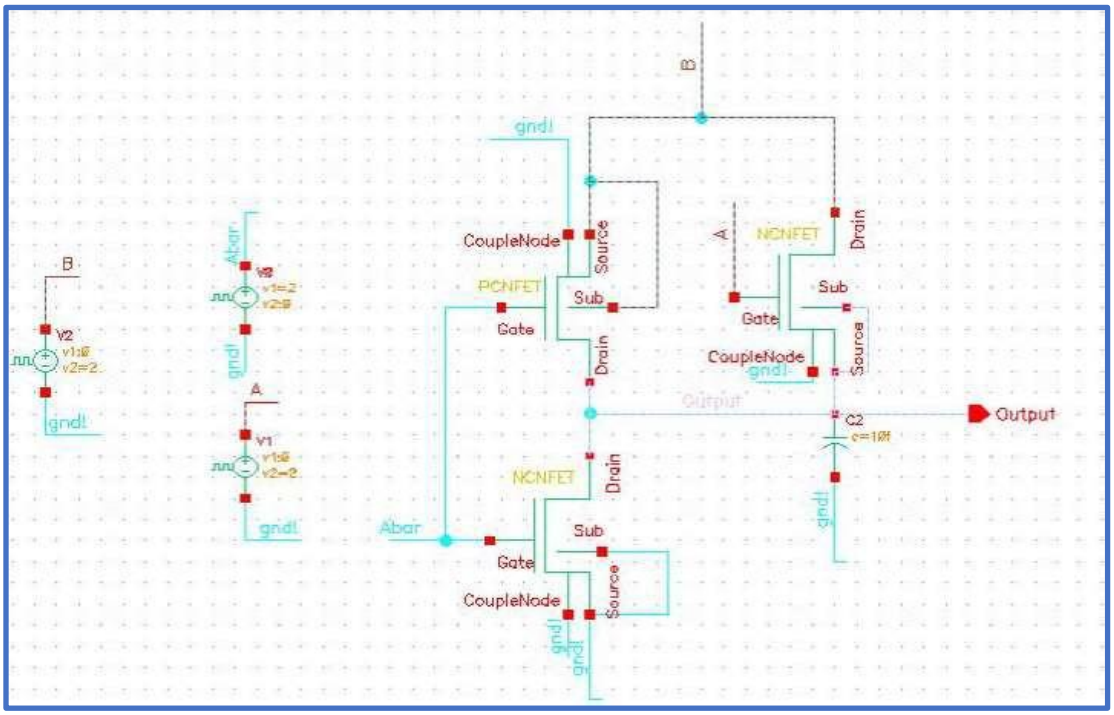


Fig 2.5: AND Gate using GDI cell

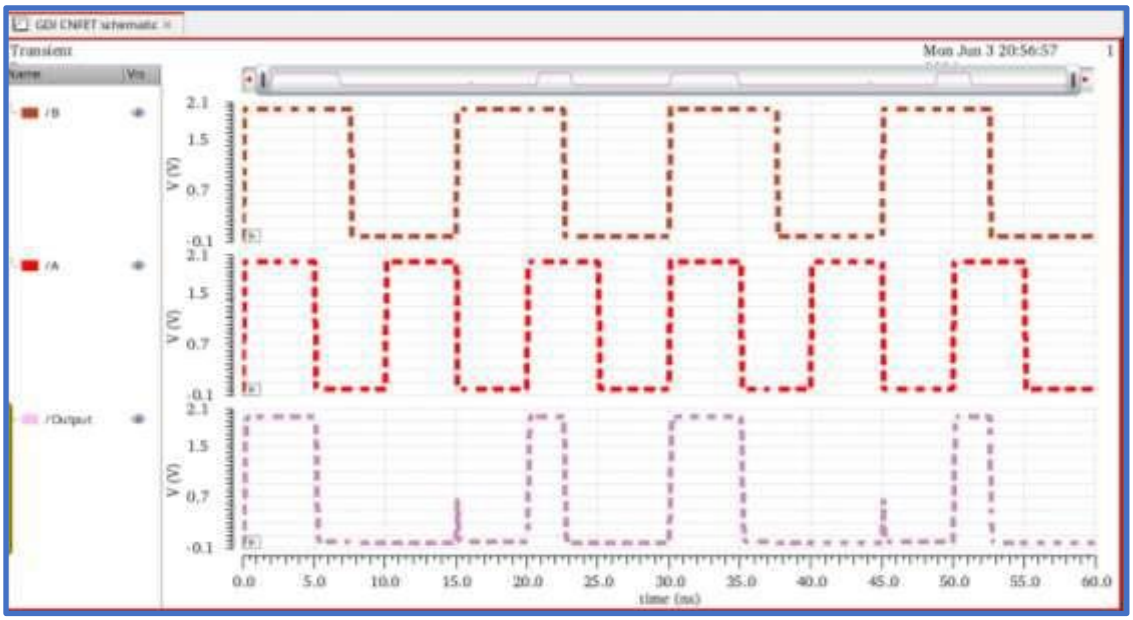


Fig 2.6.a: Transient Response of the AND gate

The circuitry is properly established, all of the AND gate's logic outputs have been confirmed,

and the delay of the same circuitry is examined and displayed in Fig.2.6.b. by maintaining the value of signal B at 1 while signal A transitions from 1 to 0.The delay was measured at about 83 ns.

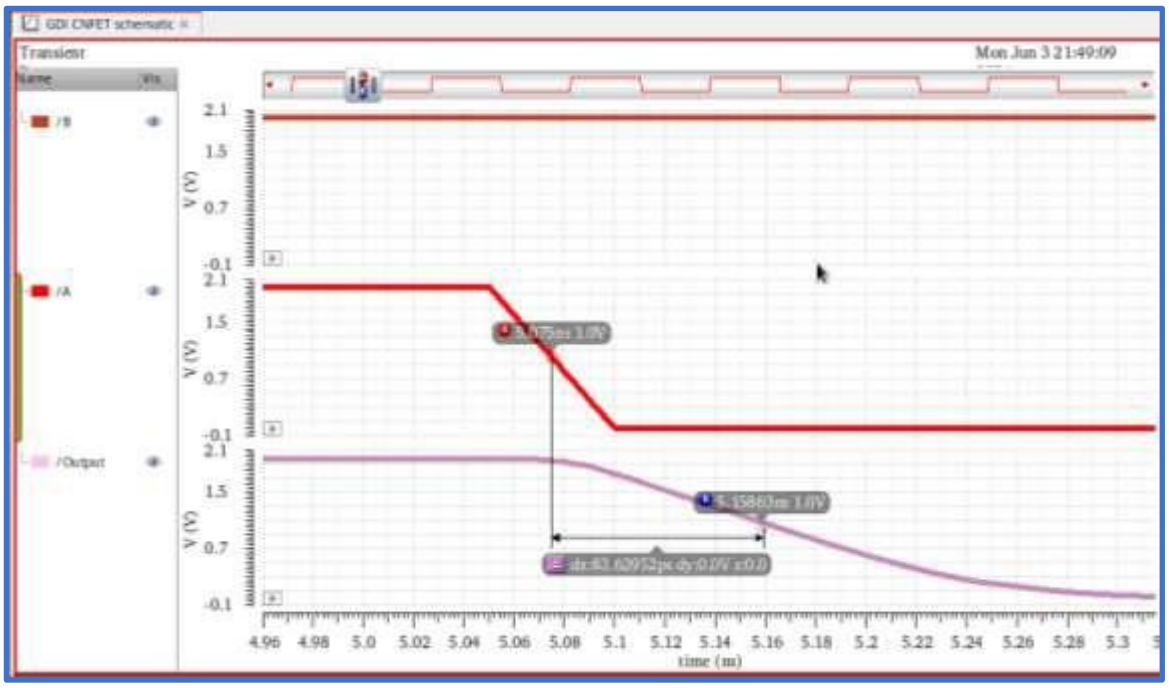


Fig 2.6.b: Transient Response of the AND gate for Delay calculation

a.ii Implementations of AND operation of Abar and B

Fig. 2.7, shows the schematic of the AND operation of Abar and B based on the GDI cell.

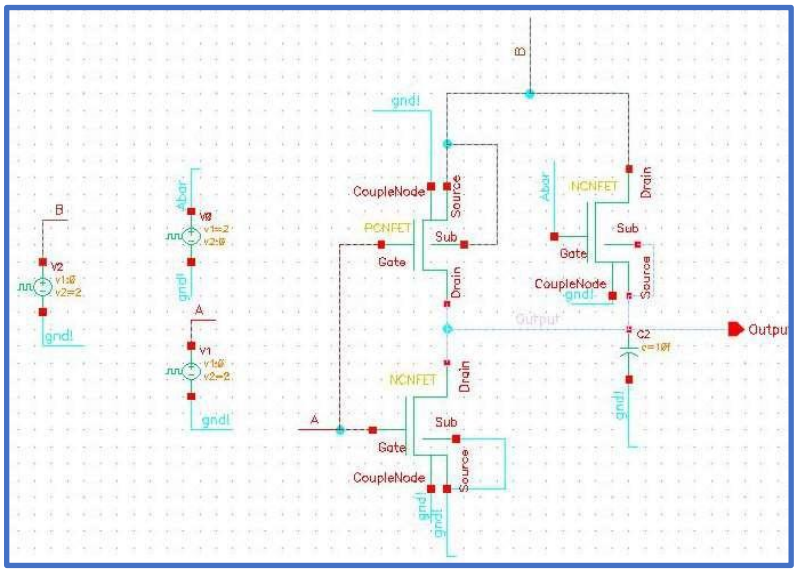


Fig 2.7: AND Gate of Abar and B using GDI cell

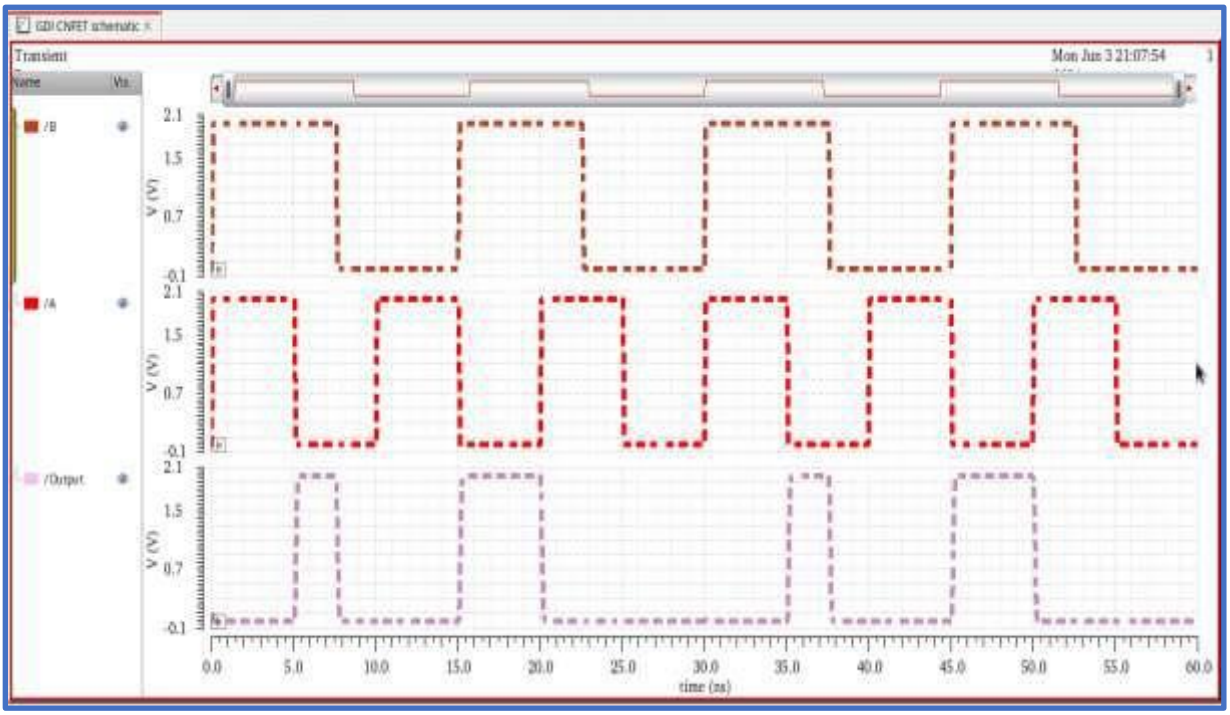


Fig 2.8.a: Transient Response of the AND gate of Abar and B

For this circuit, all the logic output of the gate has been verified and circuitry is successfully implemented and delay of the same circuitry analyzed and shown in Fig. 2.8.b by keeping the signal value of B at 1 and signal A makes an transition from 1 to 0. Delay obtained at around 58ns.

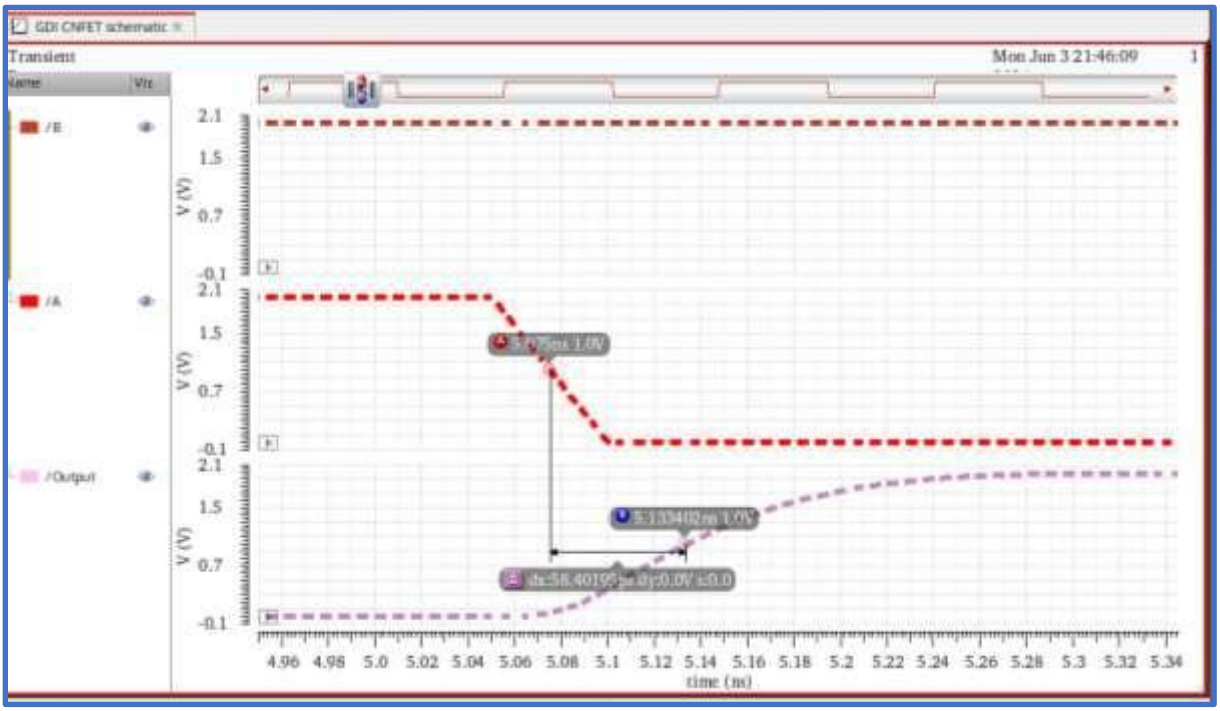


Fig 2.8.b: Transient Response of the AND gate of Abar and B for delay calculation

a.iii Implementations of AND operation of A and B bar

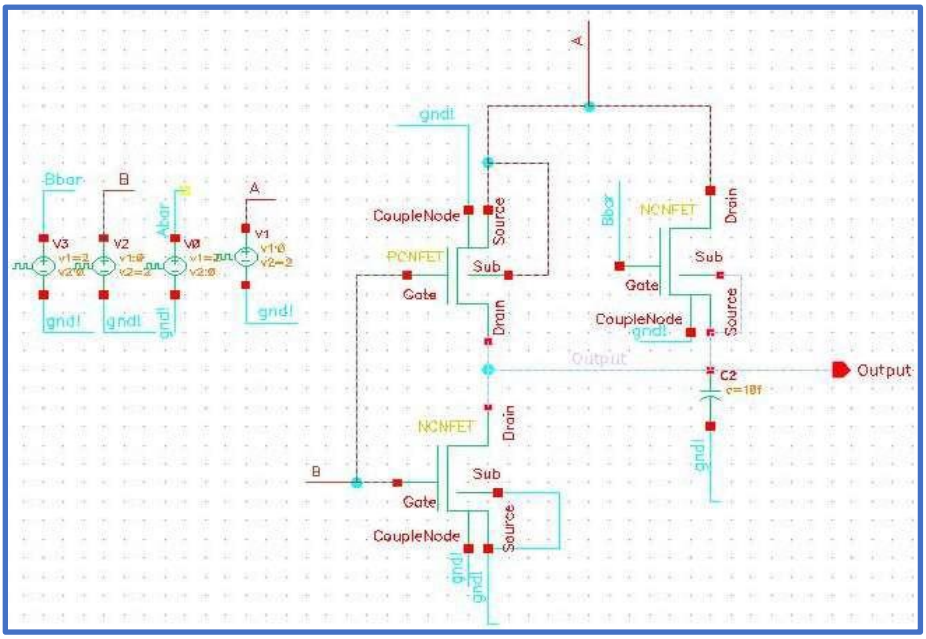


Fig 2.9: AND Gate of A and Bbar using GDI cell

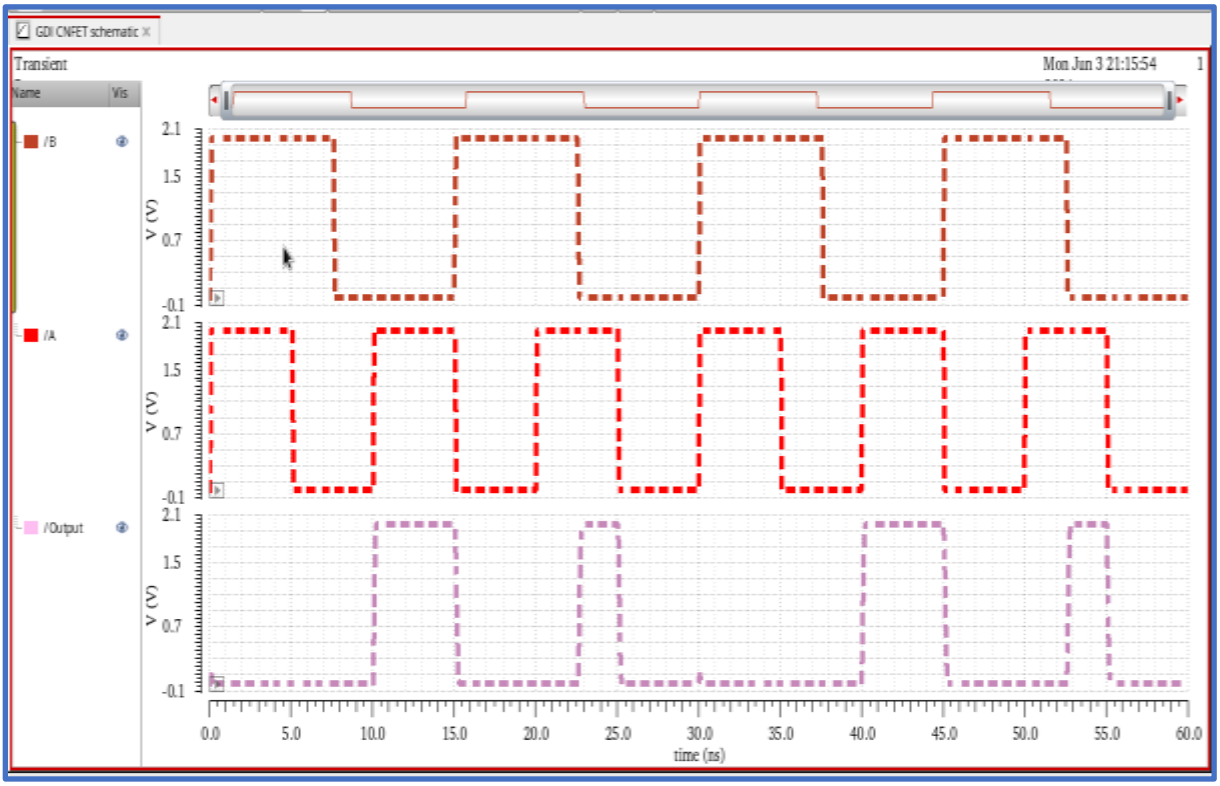


Fig 2.10.a: Transient Response of the AND gate of A and Bbar

For this circuit, all the logic output of the gate has been verified and circuitry is successfully implemented and delay of the same circuitry analyzed and shown in Fig. 2.10.b by keeping the

signal value of B at 0 and signal A makes an transition from 0 to 1. Delay obtained at around 46ns.

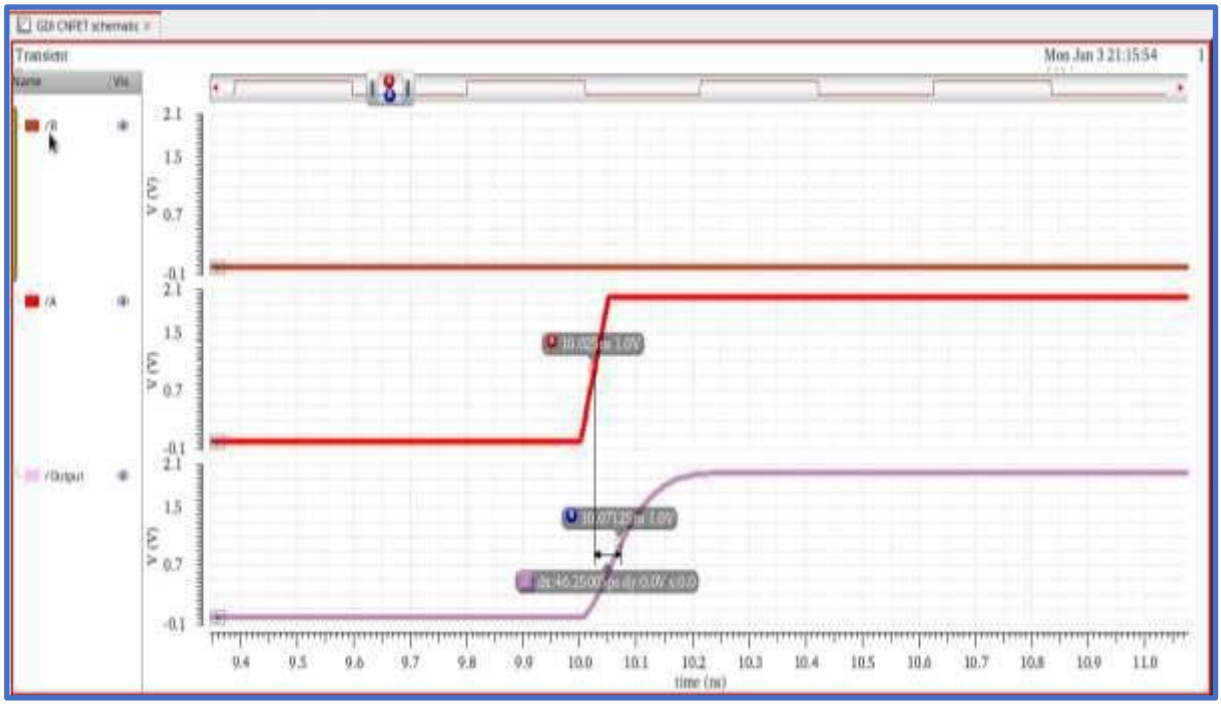


Fig. 2.10.b: Transient Response of the AND gate of A and Bbar for delay calculations

a.iv Implementations of OR gate

Fig. 17, shows the schematic of the OR gate based on the GDI cell.

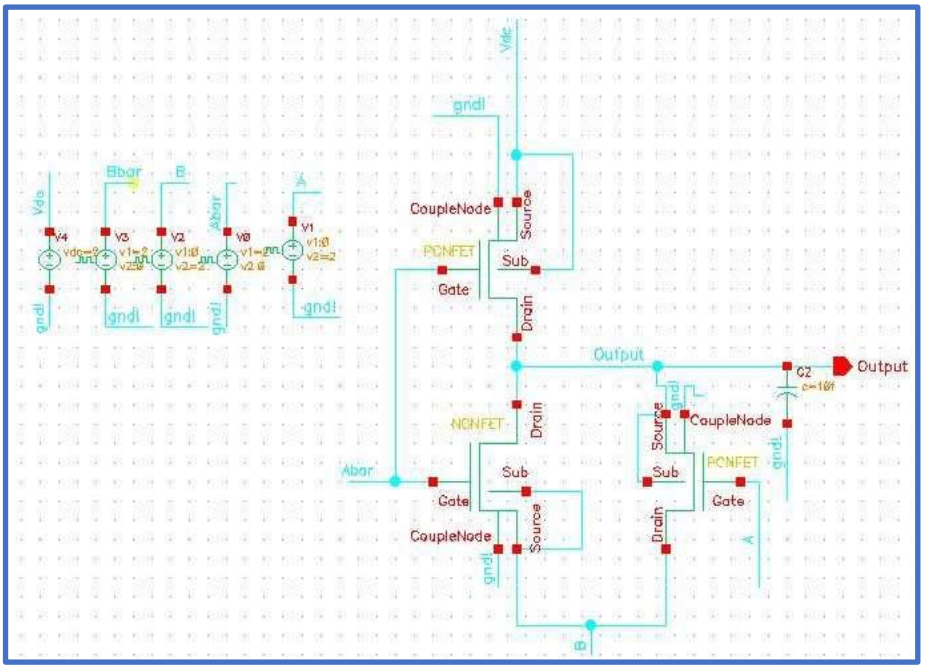


Fig. 2.11: OR Gate using GDI cell

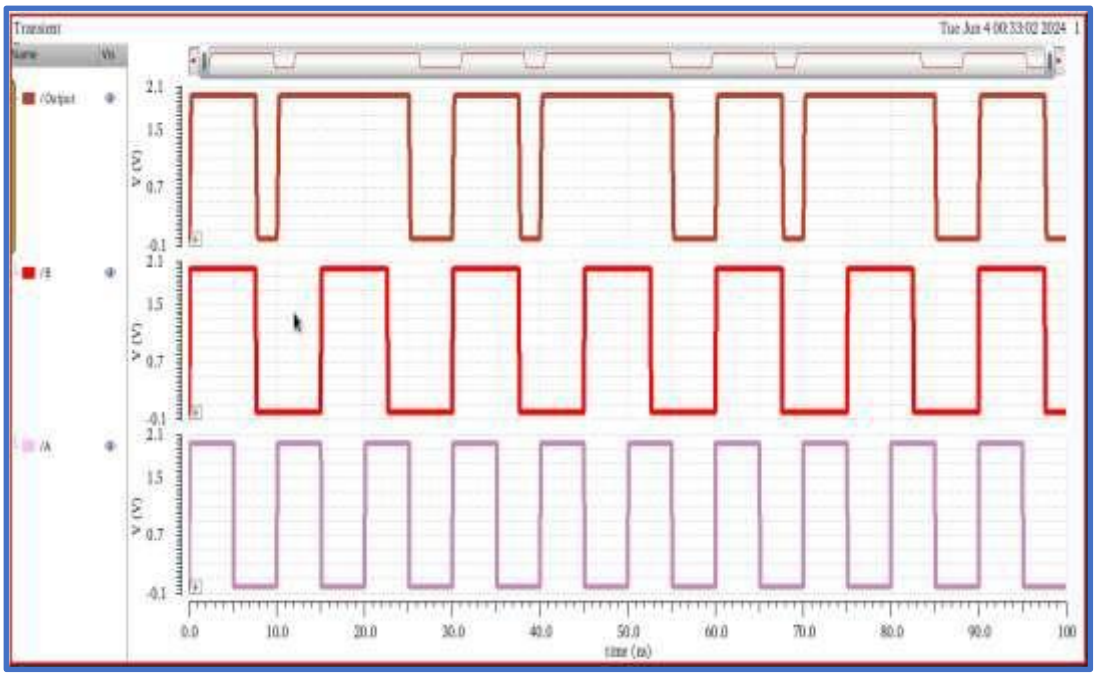


Fig. 2.12.a: Transient Response of the OR gate

The circuitry is properly established, all of the OR gate's logic outputs have been confirmed, and the delay of the same circuitry is examined and displayed in Fig. 2.11.b. by maintaining the value of signal A at o while signal B transitions from 0 to 1. The delay was measured at about 91 pS.

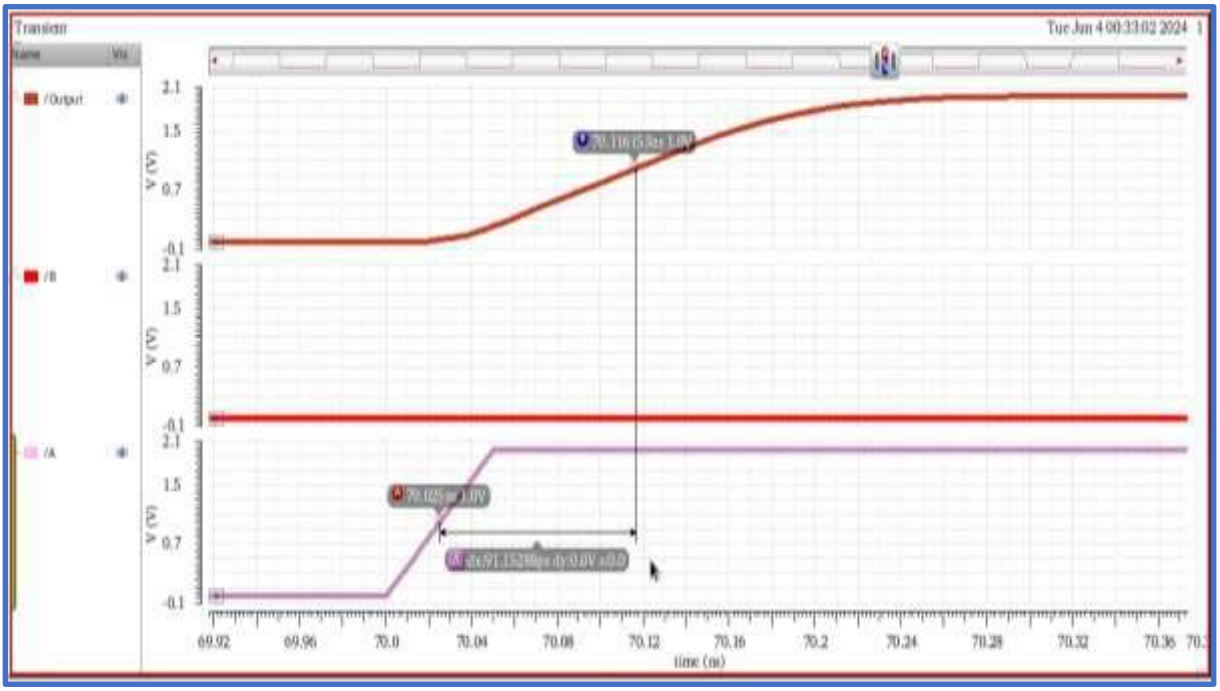


Fig. 2.12.b: Transient Response of the OR gate for delay calculations

2.3 Effect of load variation and Power supply

The power supply and load capacitance have a big impact on circuit performance. Higher load capacitance lengthens charging and discharging times, lowering the circuit's switching speed and diminishing its overall frequency responsiveness. Longer charging cycles also result in increased dynamic power usage. The circuit's power usage and signal amplitude are influenced by the power supply voltage. While a lower voltage conserves electricity but may jeopardize circuit speed and reliability, a higher supply voltage causes greater power dissipation and a stronger signal. To maximize performance, power efficiency, and signal integrity in electronic circuits, load capacitance and power supply voltage must be properly balanced.

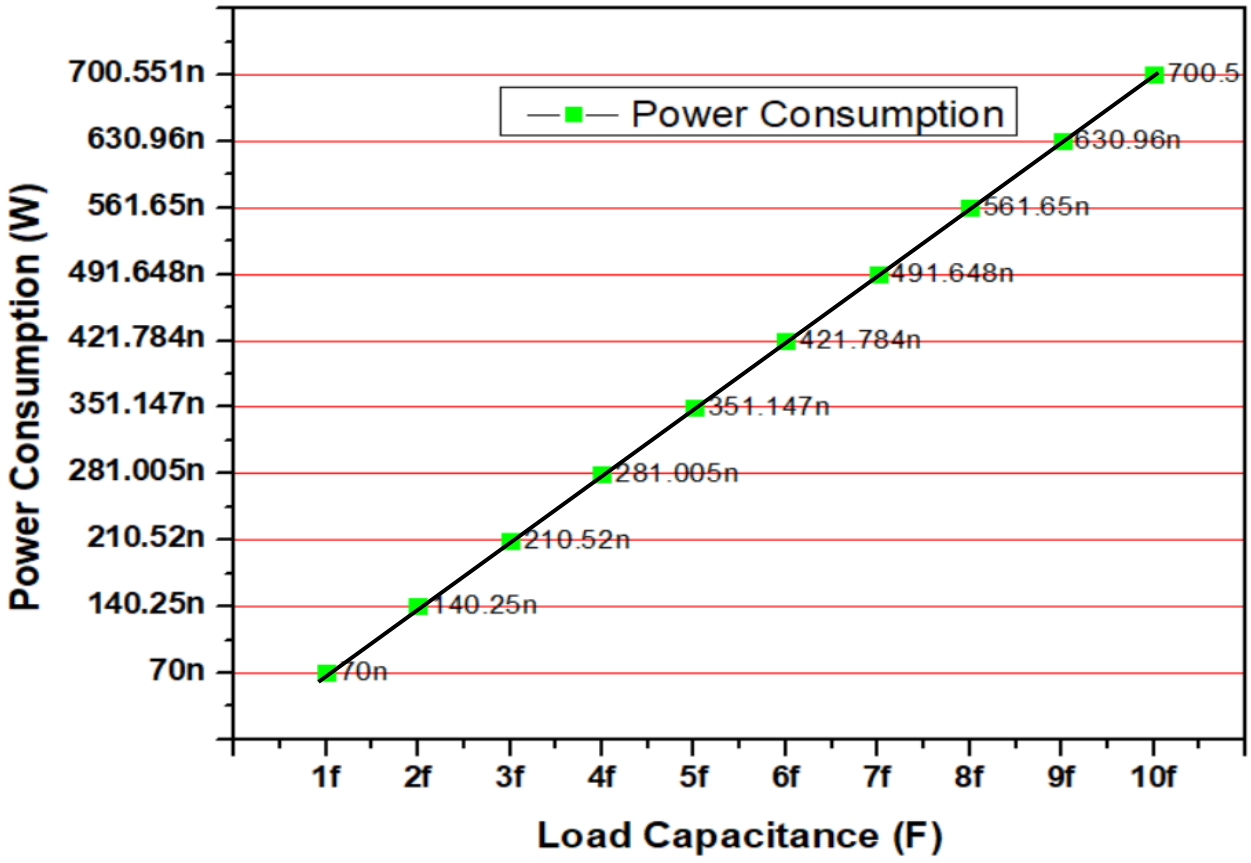


Fig. 2.13: Effect of the load variation on the power consumption

The load capacitance of the GDI circuit as depicted in Fig. 1.2 varies its ranges from 1 fF to 10 fF. Fig. 2.13 and 2.14 illustrate this. It was found that both delay and power usage rise with the load. The impact of load variation on transient behaviour is seen in Fig. 2.15. The power supply also fluctuates between 0.7 and 1.8 volts. As shown in Figures 2.16 and 2.17, it was found that power consumption rises linearly with power supply and delay decreases with power supply. The impact of power supply variation on transient behaviour is seen in Fig. 2.18.

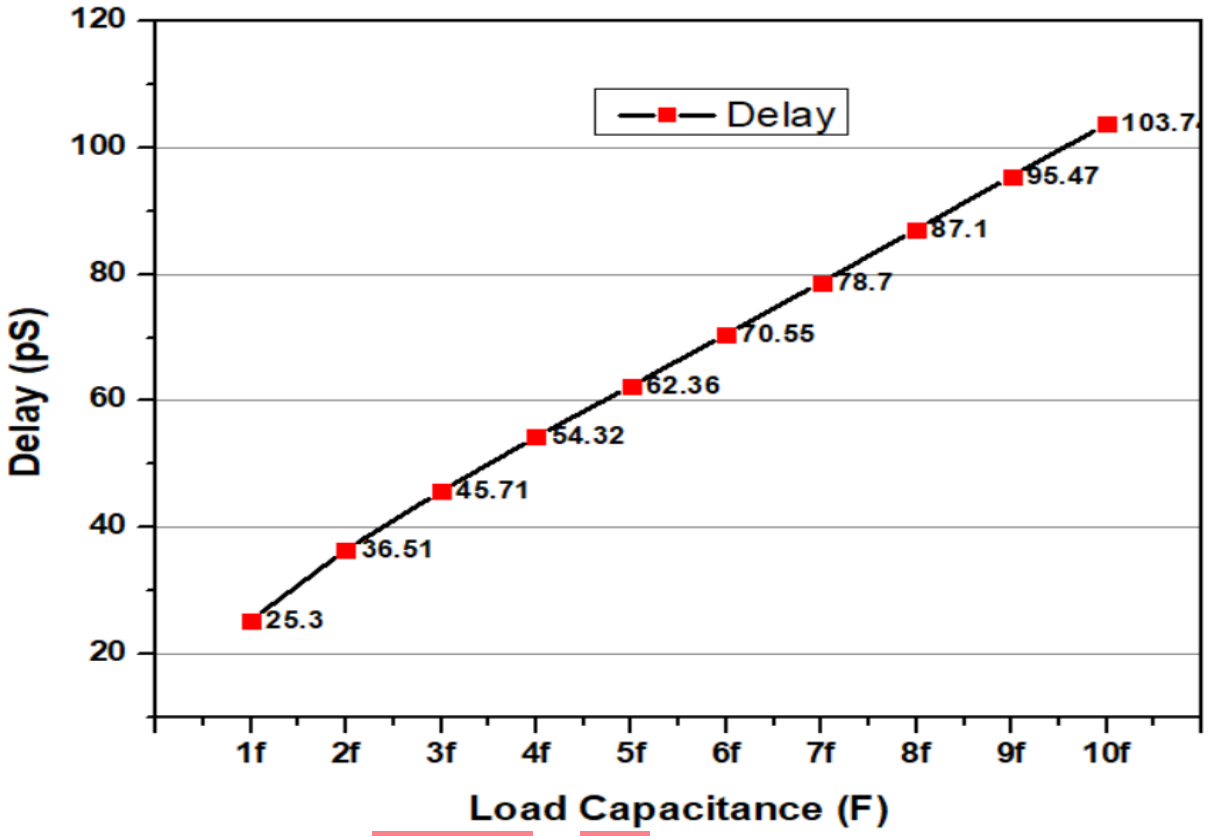


Fig. 2.14: Effect of the load variation on the delay

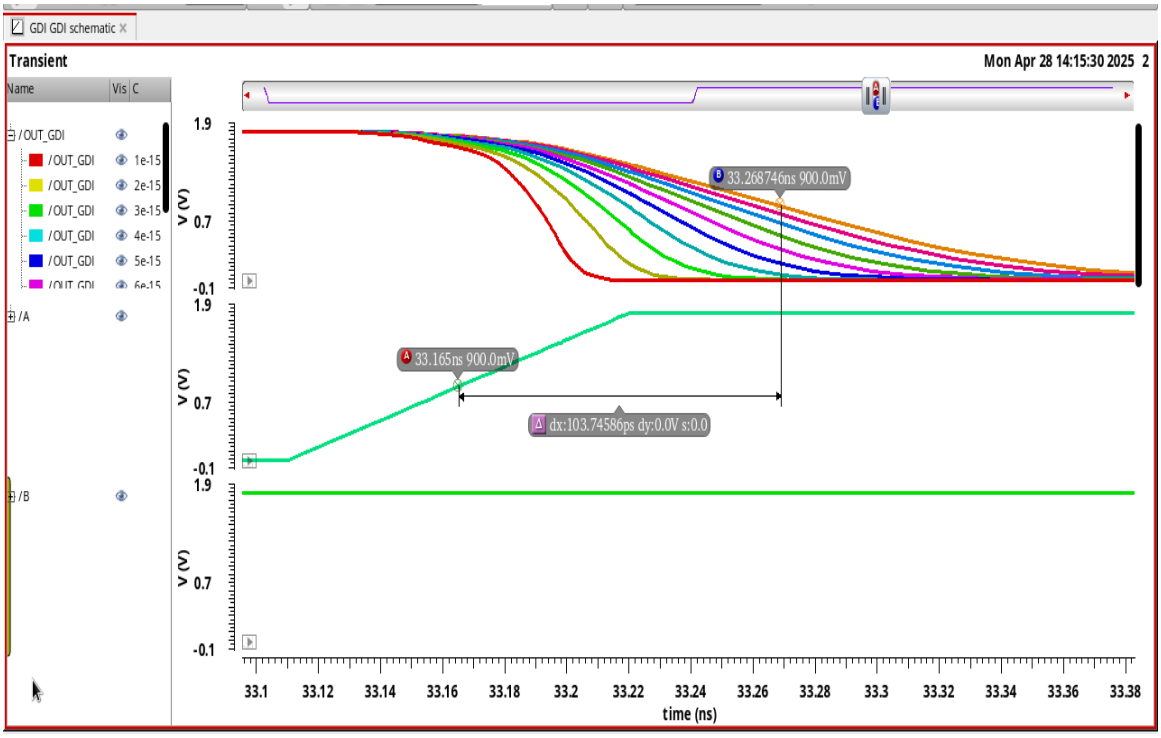


Fig. 2.15: Effect of the load variation on the transient behaviour

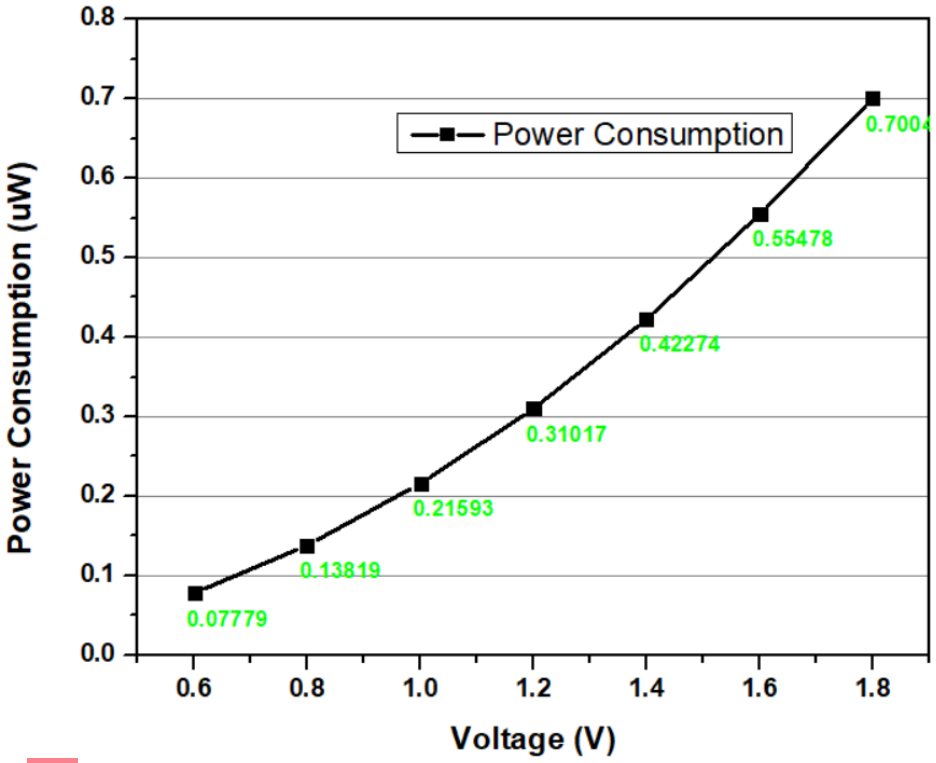


Fig. 2.16: Effect of voltage variation on the power consumption

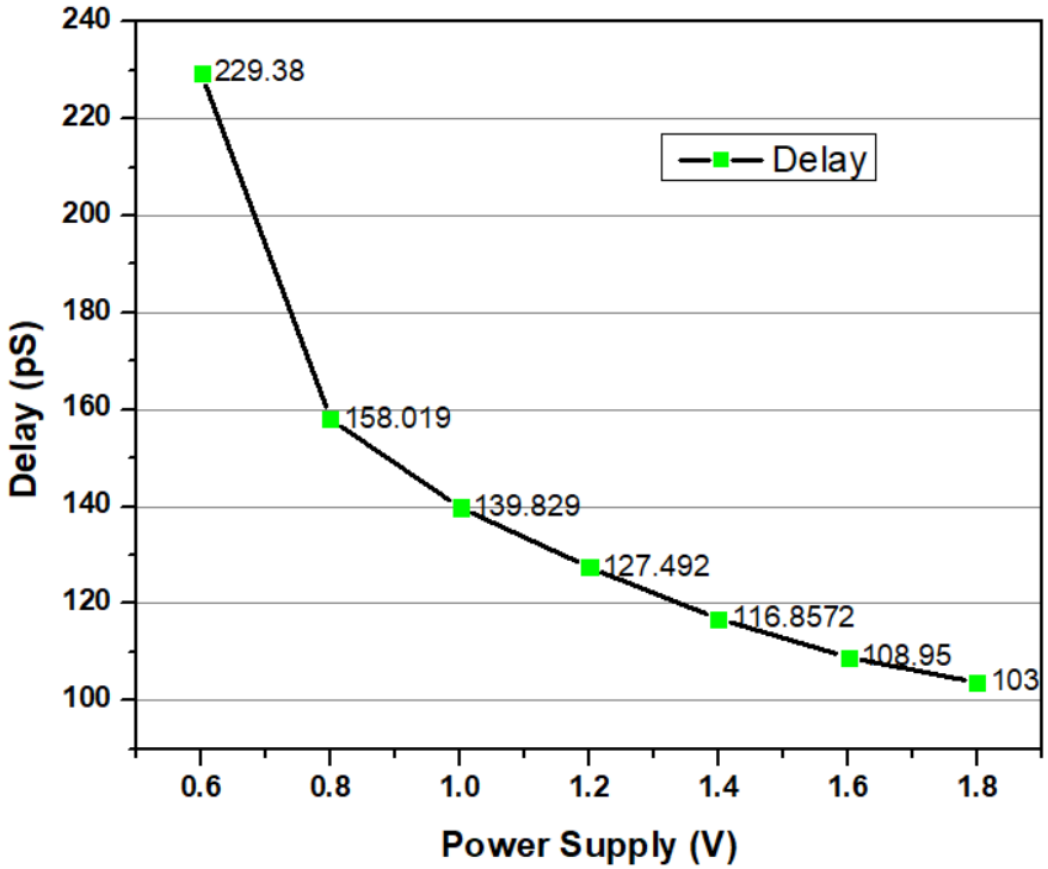


Fig. 2.17: Effect of voltage variation on the Delay

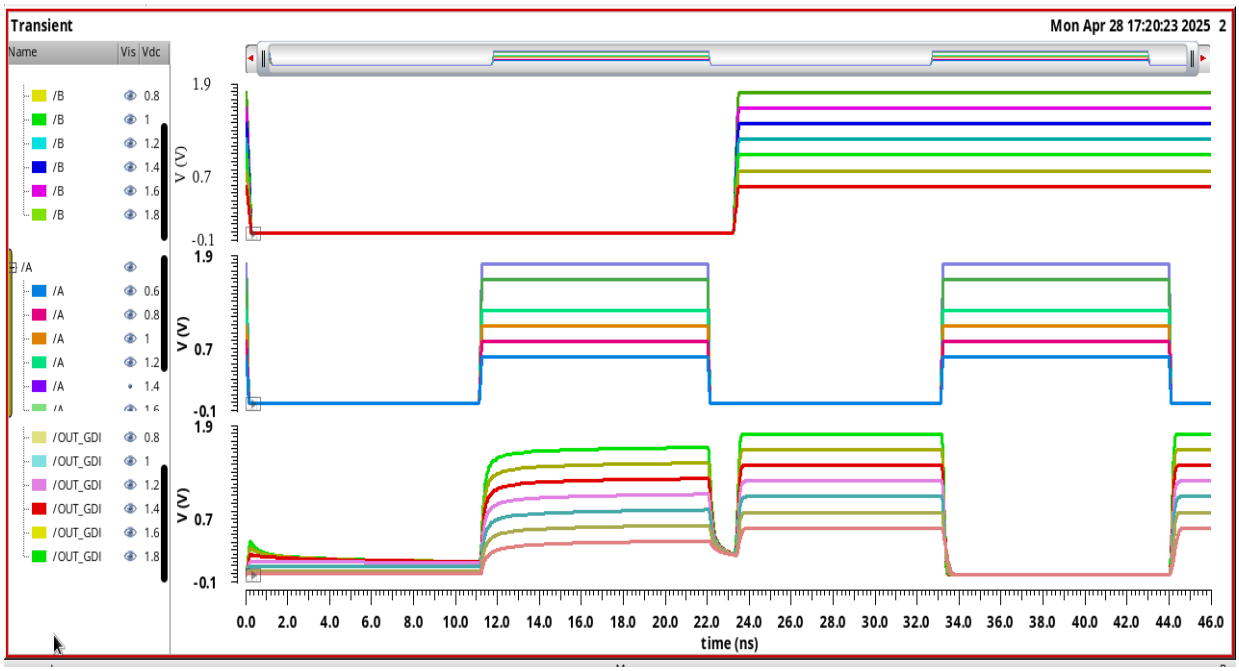


Fig. 2.18: Transient response for Power supply variations

To maximize a circuit's performance and dependability, it is essential to test how the power supply and load capacitance affect it. It guarantees that the circuit runs effectively without consuming too much power or distorting the signal. You can find possible bottlenecks influencing dynamic power consumption or switching speed by assessing load capacitance. Evaluating the effect of power supply voltage aids in striking a balance between circuit reliability, signal strength, and power efficiency. This is particularly crucial in contemporary electronic gadgets where high-speed operations and energy-saving features are essential. Thorough testing ensures that circuits full-fill design requirements and operate as intended in practical settings.

2.4 Full adder using the GDI cell

A full adder based on the XNOR GDI cell is a simulated successfully in a cadence virtuoso based on 32nm technology node. A 1-bit full adder has been created using the methods recommended in [15] to demonstrate the potential implementation of full adder based on GDI cell. Truth table of the full-adder is depicted in Table 2.3.

$$COUT = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC = BC + A(B\overline{C} + \overline{B}C) \quad \text{----------1}$$

$$COUT = C(B\overline{C} + \overline{B}C) + A(B\overline{C} + \overline{B}C) = C(B \odot C) + A(B \oplus C) \quad \text{--------2}$$

$$SUM = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC = A(B \odot C) + A(B \oplus C) \quad \text{--------3}$$

Table 2.3: Truth Table of the full adder

A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

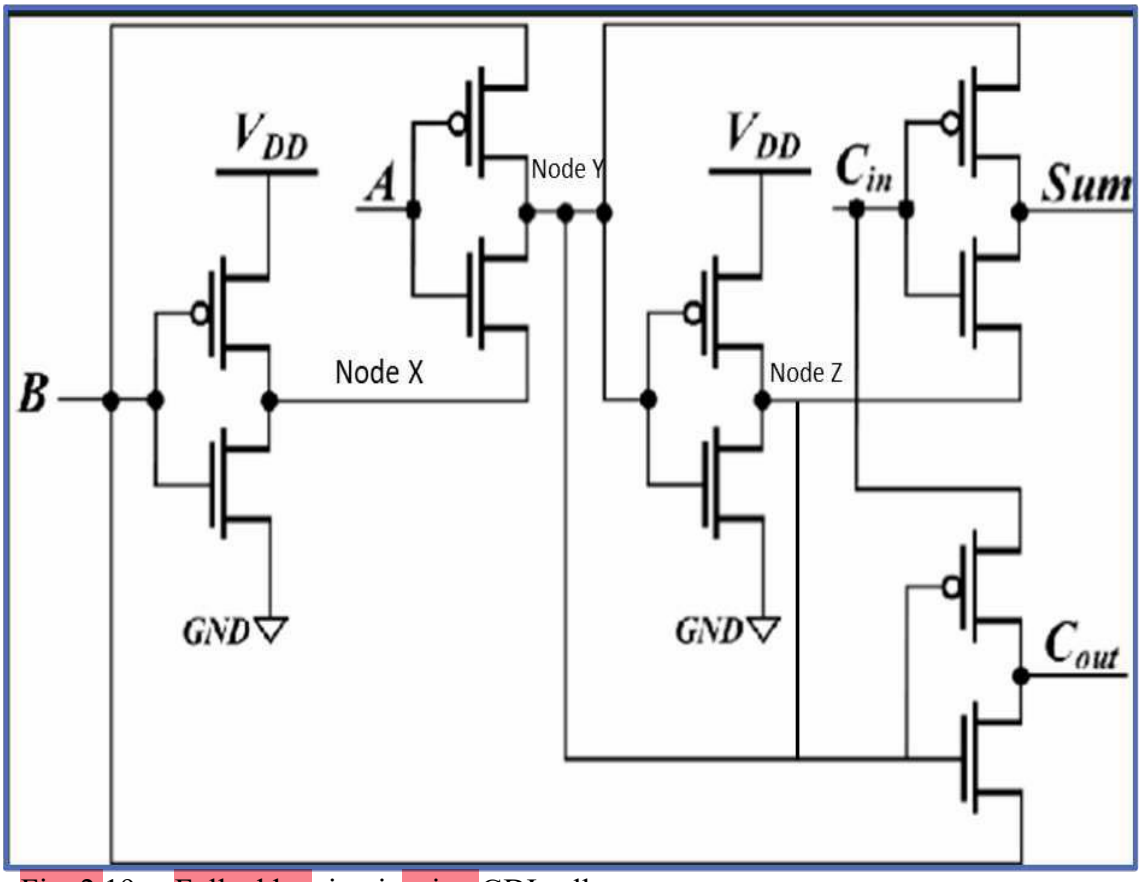


Fig. 2.19.a: Full adder circuit using GDI cell

The inverted logic B value was acquired at node X in the first step, and the inverted signal B was then applied to the following stage. XOR logic has been obtained at node Y. The XOR signal is sent to a GDI-based inverter in the next step to construct XNOR logic at node z. following the acquisition of the XOR and XNOR logic. The adder's last step is to generate the SUM and carry. To properly implement, the XNOR–XOR are cascaded to transport the desired signal to the output port. The GDI-based network's outputs are the Cout and Sum.

Signals A, B, and Cin each have a period set at 80 ns, 40 ns, and 20 ns in order to get the SUM and Carry output as seen in Fig. 2.19.a. Every input has a 50% duty cycle, a 0.8 V pulse width, and a 1 fF load capacitance. The transient figure shows that every logic based on input combination has been confirmed.

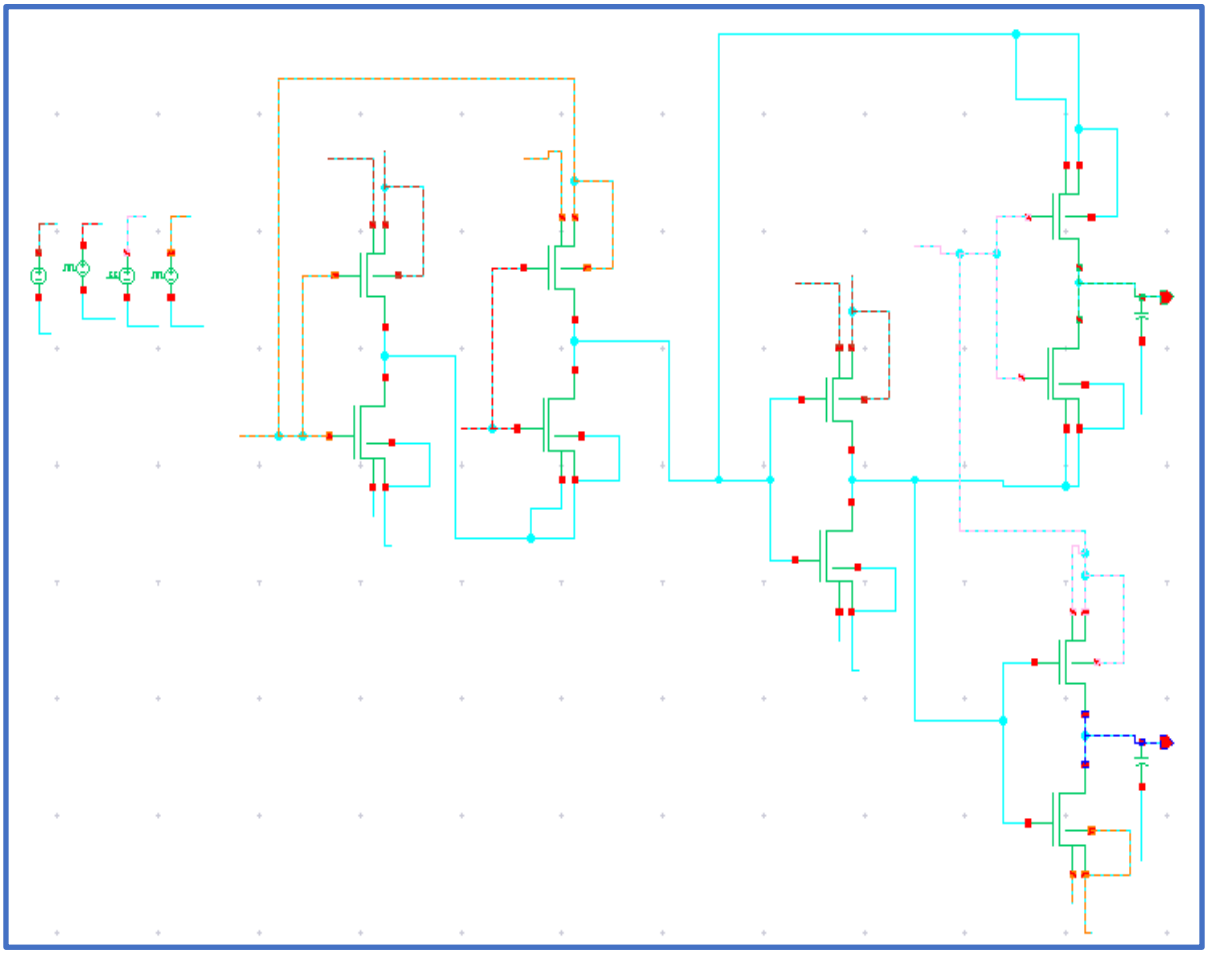


Fig. 2.19.b Schematic of Full adder using GDI

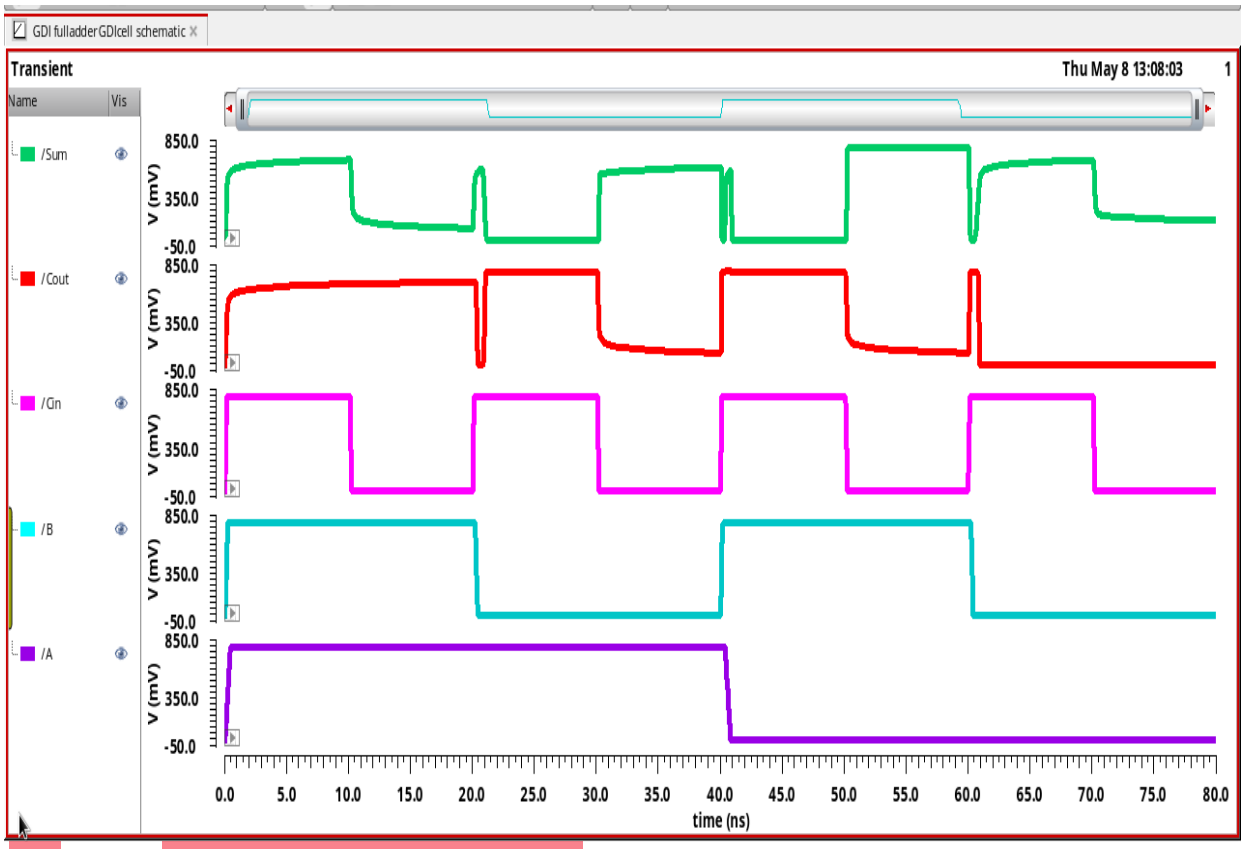


Fig. 2.20.a: Transient Response of Full adder

The delay of the GDI cell has been calculated while signals A and B are at logic 1 and signal Cin is changing from logic 1 to logic 0. The output signal, SUM, will oscillate between logic 1 and 0. The delay in this instance was around 58 ps. Throughout the whole transition period, 184 nW of electricity will be consumed. Fig. 2.20.b and Fig. 2.21 showed these delay and power findings.

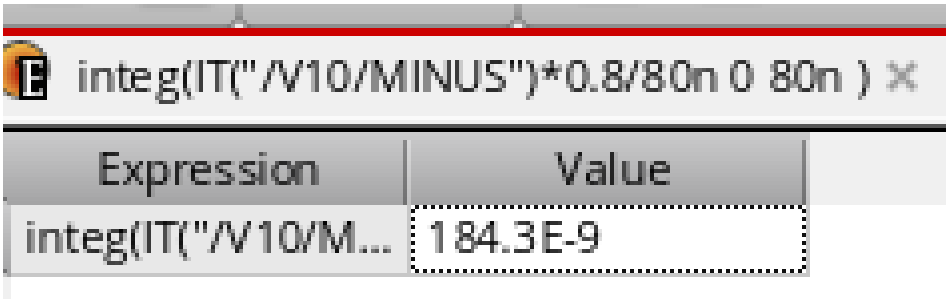


Fig. 2.21 Power Consumed by full adder based on GDI

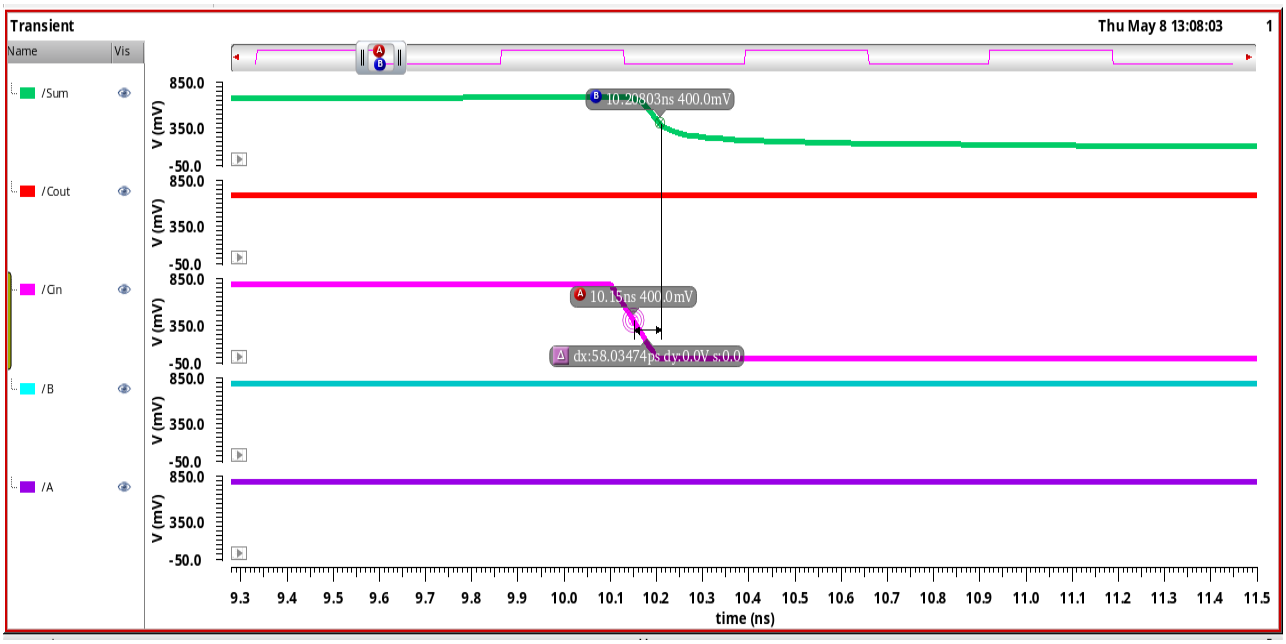


Fig. 2.20.b Transient Response of full adder for delay calculations

2.5 Ripple Carry Adder

An essential digital circuit for adding multi-bit binary integers is a ripple adder, also referred to as a ripple-carry adder (RCA). Each full adder processes a pair of input bits and a carry input from the stage before it. The fundamental structure is made up of a succession of full adders. As the carry moves through the circuit, the carry output from each full adder is sent to the subsequent full adder in the sequence, producing a "ripple" effect.

Function and Organization:

➢ Logic Circuit for Combination:

- A combinational logic circuit called the RCA is made to add two n-bit binary values.
- It processes multiple bits at once by cascading n complete adders in sequence, thus its other name, an n-bit parallel adder.

➢ Carry Propagation:

- For the next full adder stage, the carry input is the carry output from each full adder.
- The cumulative delay caused by this sequential carry prop, also referred to as the propagation delay, rises as the number of input bits increases.

4-Bit Ripple Carry Adder:

- **Dynamic Gate Diffusion Input (GDI) Logic:**
  - A 4-bit RCA based on DGDI logic demonstrates the suitability of this approach for designing adders with higher bit lengths.
  - GDI is a low-power design technique that reduces the number of transistors required for logic gates, enhancing power efficiency and performance.

- **Design Simplicity and Delay:**
  - The RCA's simple structure is one of its key advantages, making it easy to design and implement.
  - However, the delay increases with the number of input bits, which can be a limitation in real-time applications.

Implementation Details:

- **4-Bit Example:**
  - In a 4-bit RCA, four full adders are connected in series, each responsible for adding corresponding bits of two binary numbers (A0-A3 and B0-B3).
  - The least significant bits (LSBs) A0 and B0 are input to the first full adder (FA0), which generates the sum bit (SUM0) and the carry bit (COUT0).
  - This carry bit (COUT0) is fed into the second full adder (FA1) along with the next bits A1 and B1, producing SUM1 and COUT1.
  - The process continues with FA2 and FA3, where the carry output from each stage feeds into the next, ultimately generating the final sum bits and the carry-out signal.

Because of its simplicity, the architecture is perfect for low-power devices, educational settings, and situations where speed needs are subordinated to design simplicity. Fig. 2.22 shows the ripple adder's construction, and Table 4 offers the truth table that goes with it. The RCA's functioning and operation are further explained by these tables and pictures, which further illustrate the device's usefulness and performance traits in digital circuit design.

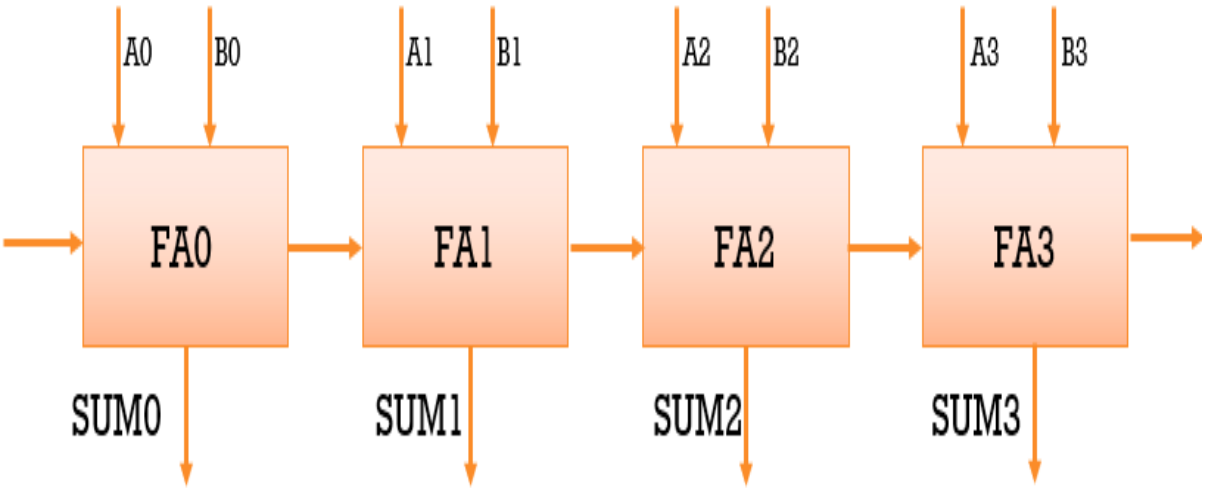


Fig. 2.22 Architecture of the Ripple carry Adder

Table 2. 4: Truth Table of RCA (4 Bits)

Cin	A				B				Sum				Carry
0	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
	0	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	1	0	0	0	1	0
	0	0	1	0	0	0	1	0	0	0	1	0	0
	0	0	1	1	0	0	1	1	0	0	1	1	0
	0	1	0	0	0	1	0	0	0	1	0	0	0
	0	1	0	1	0	1	0	1	0	1	0	1	0
	0	1	1	0	0	1	1	0	0	1	1	0	0
	0	1	1	1	0	1	1	1	0	1	1	1	0
	1	0	0	0	1	0	0	0	1	0	0	0	1
	1	0	0	1	1	0	0	1	1	0	0	1	1
	1	0	1	0	1	0	1	0	1	0	1	0	1
	1	0	1	1	1	0	1	1	1	0	1	1	1
	1	1	0	0	1	1	0	0	1	1	0	0	1
	1	1	0	1	1	1	0	1	1	1	0	1	1
	1	1	1	0	1	1	1	0	1	1	1	0	1
	1	1	1	1	1	1	1	1	1	1	1	1	1
	1	1	1	1	1	1	1	1	1	1	1	1	1

RCA Simulations in a Cadence Virtuoso and Results

To develop a Ripple Carry Adder (RCA) using a GDI (Differential Gate Diffusion Input) block, follow these steps:

1. **Design the Full Adder Circuit:** Start by implementing the full adder circuit based on DGDI, as illustrated in Fig. 2.19b.
2. **Construct Four Full Adders:** Create four full adders, each with unique input names or pin configurations.
3. **Create Symbols:** Generate symbols for each full adder (FA0, FA1, FA2, and FA3) by using the cell-view option in Cadence.
4. **Generate the Circuitry:** Open a new window and build the overall circuitry as shown in Fig. 2.22, which depicts the schematic of the RCA based on DGDI.

Operation of the RCA: The RCA performs binary addition of inputs A (A0, A1, A2, A3) and B (B0, B1, B2, B3). Here's the step-by-step process:

- **FA0 (First Full Adder):** Feed the least significant bits (LSBs), A0 and B0, into FA0. This adder generates SUM0 and the carry-out bit, COUT0.
- **FA1 (Second Full Adder):** Pass COUT0 along with the next bits, A1 and B1, into FA1. This generates SUM1 and COUT1.
- **FA2 (Third Full Adder):** Feed COUT1 along with inputs A2 and B2 into FA2, producing

SUM2 and COUT2.

- **FA3 (Fourth Full Adder):** Finally, provide the most significant bits (MSBs), A3 and B3, along with COUT2, to FA3. This produces the final SUM and carry-out signal.

The schematic of the RCA unit block (FA1) is shown in Fig. 2.23. This method ensures accurate binary addition by leveraging the DGDI block for high performance and low power consumption in digital circuits.

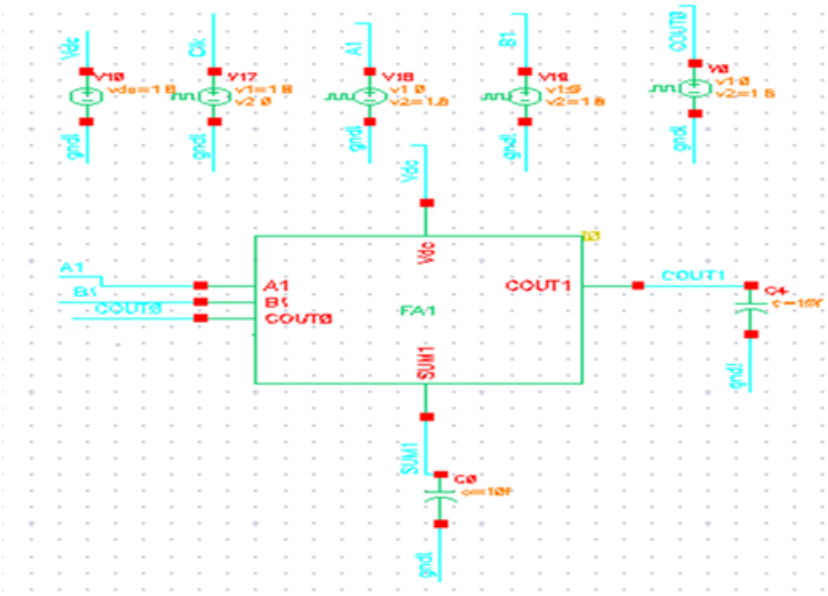


Fig. 2.23: Schematic of unit block of RCA

The Ripple Carry Adder (RCA) based on Dynamic Gate Diffusion Input (GDI) was simulated in Cadence Virtuoso. During the simulation, the input values were set as follows:

- Period of A0, A1, A2 and A3 setup at: 80 nm
- Period of B0, B1, B2 and B3 setup at: 40 nm
- Period of C0, C1, C2 and C3 setup at: 20 nm with a duty cycle of 50%
- Voltage range of the input voltage: 0.8V

The power consumption would be around 419nW as shown in Fig. 2.24 with the delay of 263pS for ripple carry adder circuitry, same depicted in Fig 2.25.b.

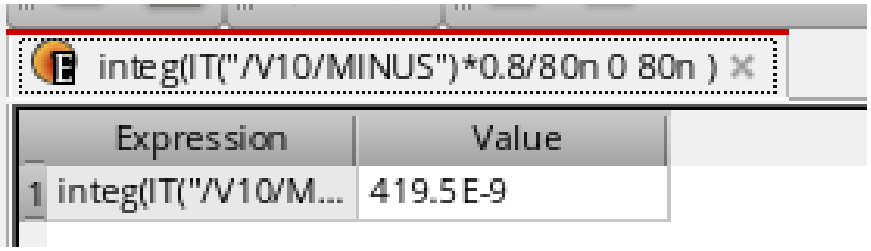


Fig. 2.24 Power consumed by GDI based RCA circuitry

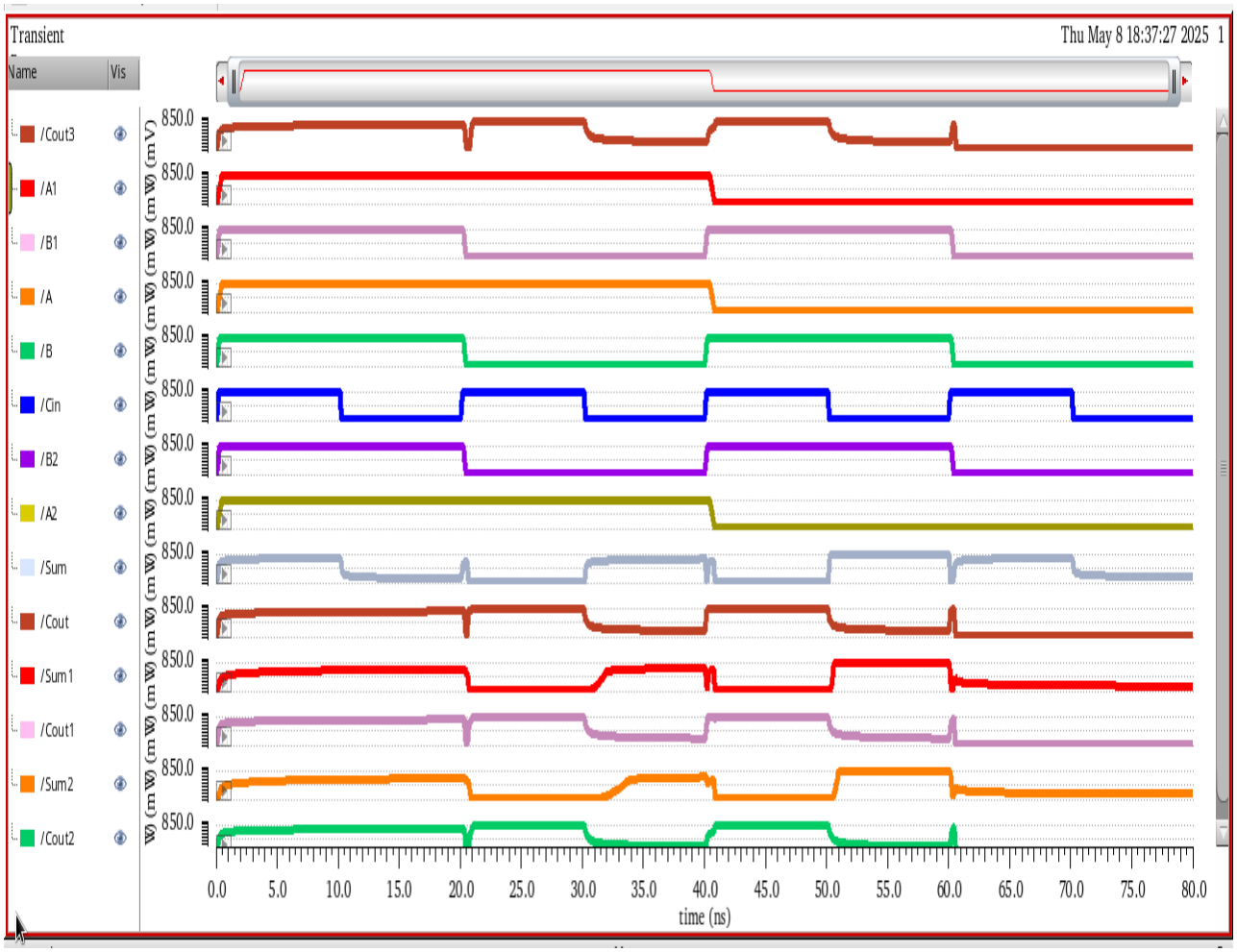


Fig. 2.25.a Transient response of the 4-bit Ripple bit carry adder

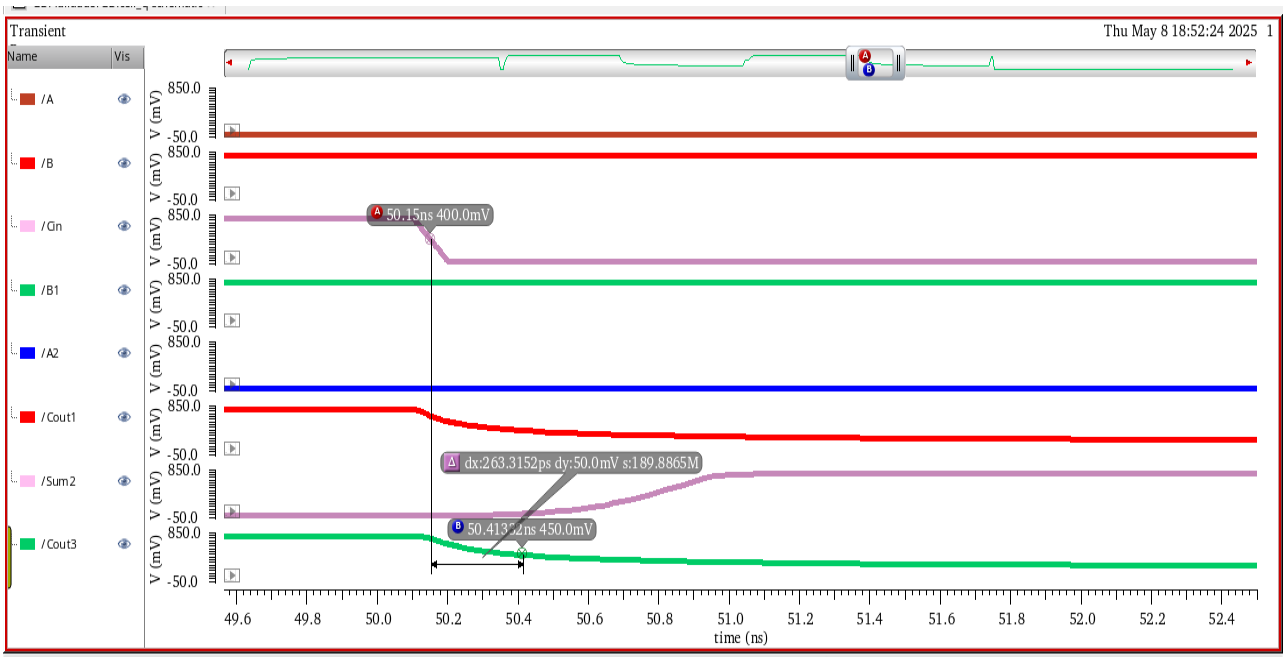


Fig. 2.25.b Delay plot for RCA based on GDI technique

2.6 Multiplier

33

A circuit for a 2x2 multiplier that takes two 2-bit binary values (X1 X0) and Y1 Y0 as inputs and outputs a 4-bit binary output (S3 S2 S1 S0) that shows the product of those two values. To calculate the multiplication, two half-adder operations and AND gates are employed. The 2x2 multiplier's implementation block diagram is displayed in Fig. 2.26.

The original circuitry had four outputs: X0Y0, X1Y0, X0Y1, and X1Y1. The least significant bit (LSB) of the multiplier output (B), S0, is produced by the product X0Y0. The S1 bit is created by combining X1Y0 and X0Y1 using a half adder (HA1). The S2 bit is created by adding the carry output from the first half adder (HA1) to X1Y1. The S3 bit performs this second half adder (HA2). The delay graphs for the 2x2 multiplier and the simulated waveforms for each input and output are shown in Fig. 2.27 and 2.28 respectively. Furthermore, the MSB of the multiplier output was obtained by measuring the delay of approximately 49.92 ps. The same circuitry uses 129 nW of electricity on average.

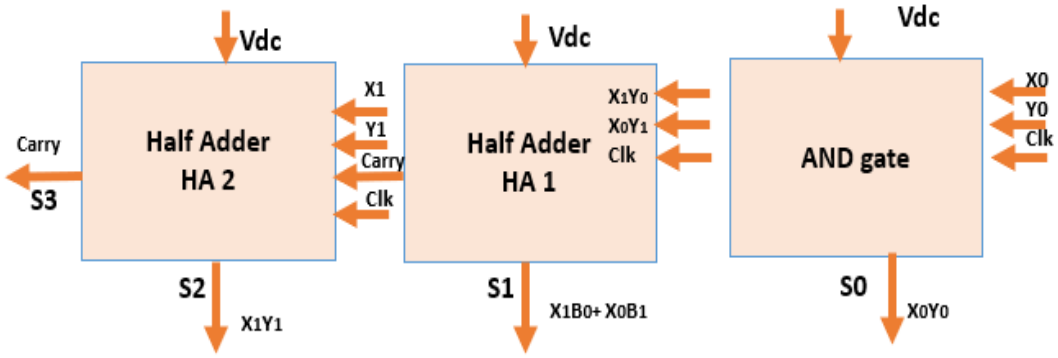


Fig. 2.26 Schematic for 2x2 multiplier based on DMGDI

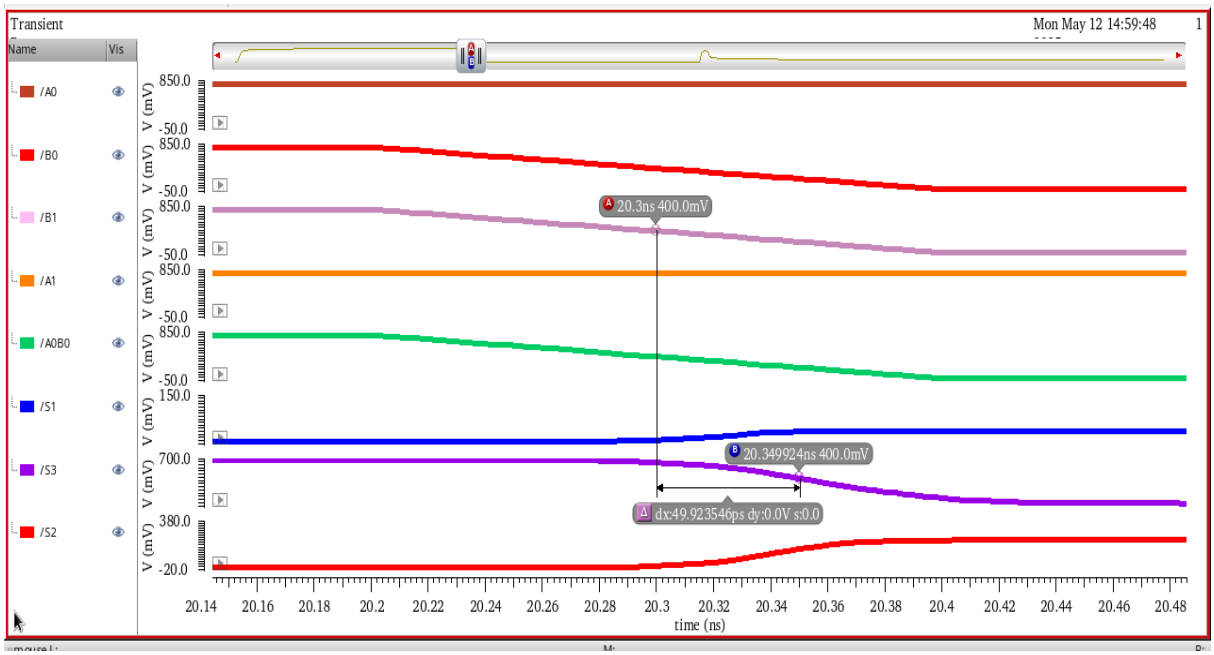


Fig. 2.27: Delay plot for 2x2 multiplier based on GDI technique

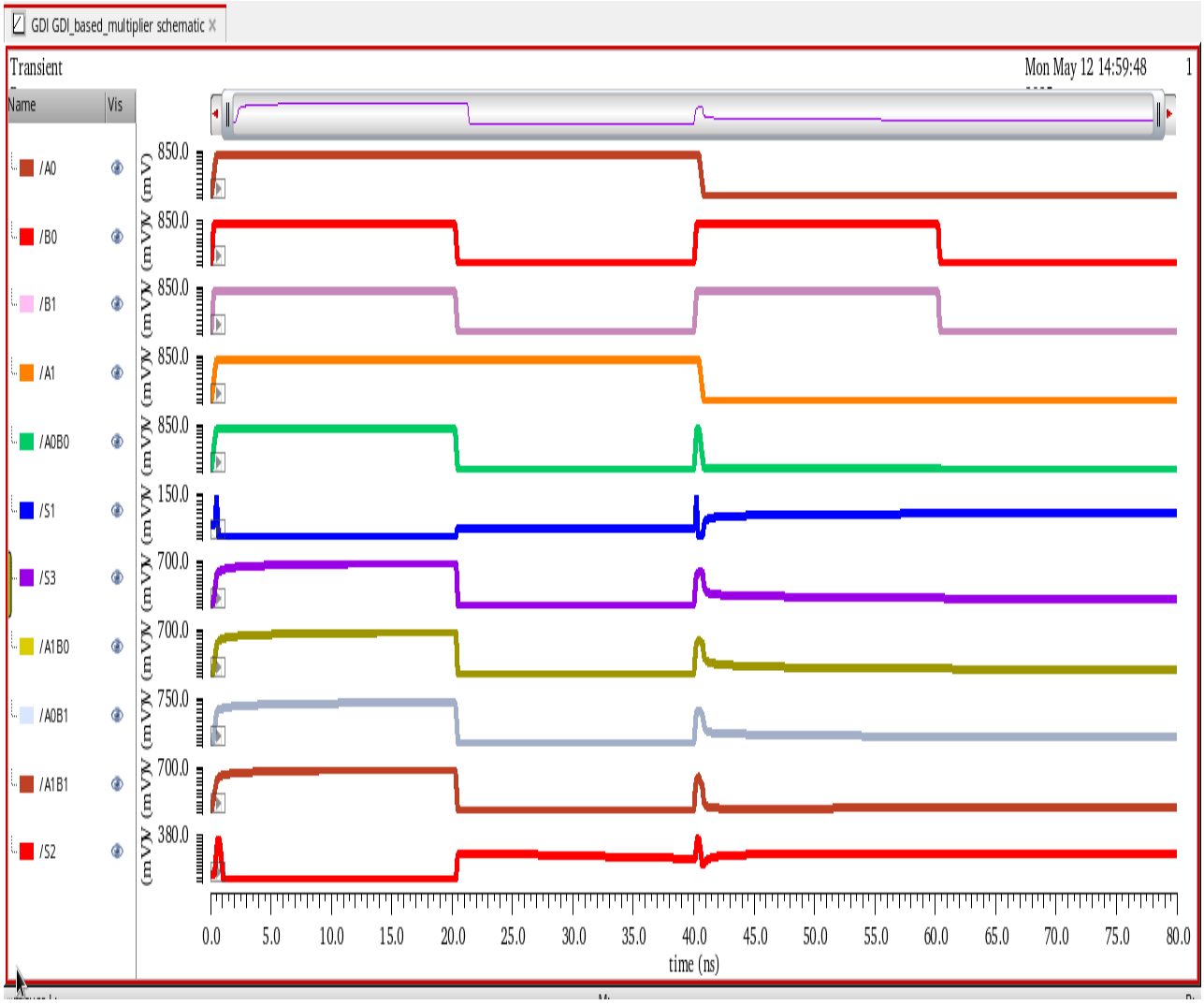


Fig. 2.28 Transient response of the 2x2 multiplier based on GDI technique

2.7 Summary

The Cadence Virtuoso effectively emulated GDI cells, then full adders, RCA and multiplier based on GDI cells, and different logic implemented utilizing GDI cells. GDI cells are used to construct XNOR, AND, and OR gates. Every gate's temporal response (transient analysis) was completed, and every logic input's output was confirmed. Every circuit's delay was also measured. There are 75.89 ns, 83 ns, 58 ns, 46 ns, and 91 ns delays for the GDI cell based on AND gate, AND operation of Abar.B, AND operation of A.Bbar, and OR gate, respectively.

Using GDI, the circuit was successfully XORed. For the XOR gate, transient analysis and output verification of every logical input were also confirmed. In contrast to GDI, which limits the complete swing at logical input (GPN) 001 and 101, output has full swing. An XOR gate based on a GDI cell would need 700 nW of power and have a delay of about 133

ps. A load capacitance of 10f F and 1.8 V were used for this simulation.

A simple GDI cell is used to construct a full adder. The circuitry is being simulated at 1f F and a voltage of 0.8 V for a fair comparison with other cutting-edge technology. The output of the entire adder (SUM and Carry) was examined in transient response following the successful implementation of the design in Cadence. The GDI-based full adder has successfully validated all of the full adder's logic. For the GDI cell, the reported delay and power consumption would be 58.03 ps and 0.184.3µW, respectively. Performance parameter of different combinational circuitry based on GDI is tabulated in Table 2.5.

Table 2.5: Different circuitry based on GDI Cell

Logic Gate	Delay (pS)	Power Consumptions (nW)	PDP Parameter (E-18)
XOR Gate (1.8V)	133.1	700	93.170
Full Adder (0.8)	58.03	184.3	10.694
RCA (0.8)	263.31	419.5	110.458
Multiplier (0.8)	49.92	129	6.439

Chapter 3: Combinational circuit based on Dynamic Gate Diffusion Input based (DGDI)

The GDI is a novel technique for designing low-power, area efficient and high-speed static combinational circuit. Additionally, GDI technique helps in reducing circuit complexity and adds reconfigurability to the design. But as seen in last chapter, that the output may display weak '0' or weak '1' states for particular input combinations, depending on the specific function that the GDI circuit is intended to perform. To rectify the same, dynamic logic block included after GDI cell, called as Dynamic Gate Diffusion Input (DGDI) [16] cell.

3.1 The DGDI Cell

Fig. 3.1 depicts a typical DGDI cell. The total number of CNFET devices is four, which is twice as many as the GDI. As can be observed, dynamic logic is used at the output stage, where the clock is applied to the PCNFET gate and the clock bar is applied to the NCNFET source. As was previously said, the DGDI has an advantage in terms of complete swing achievable at the output, whereas the GDI is unable to achieve full swing. It will facilitate the easy realization of the intricate circuit. The dynamic circuit theory of the DGDI circuit means that the output node will be pre-charged to Vdd while the clock is at logic 0 and the PCNFET is ON. Depending on the value G, P, and Clock at logic 1

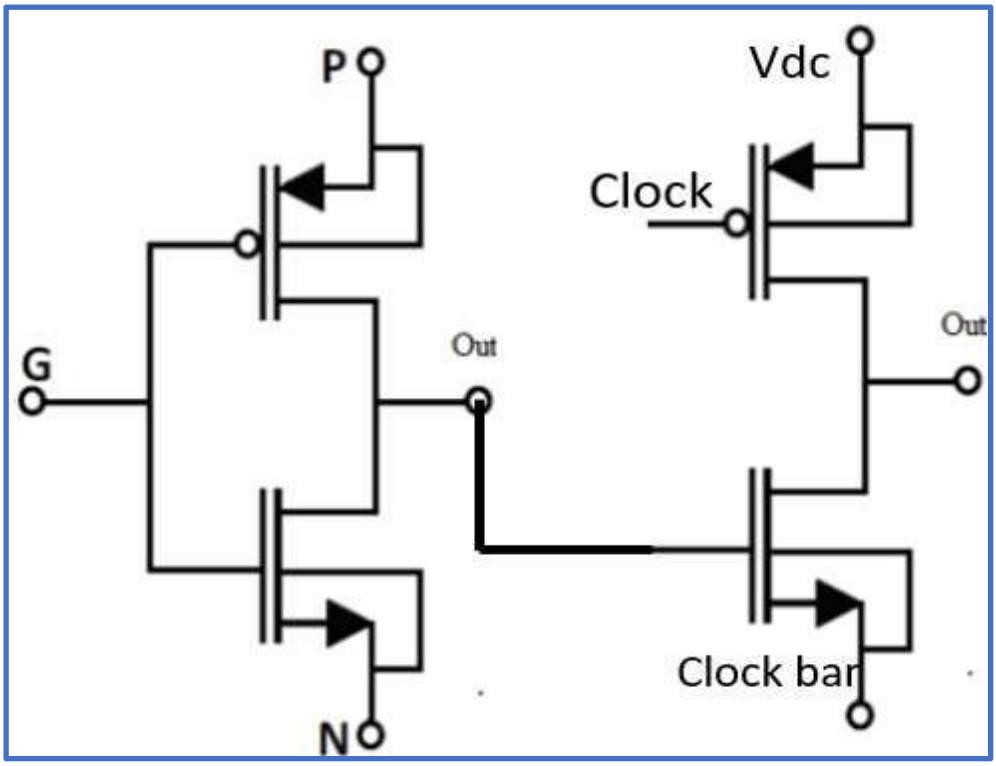


Fig. 3.1: DGDI Cell

3.2 XOR gate based on the DGDI cell

The GDI cell applies Ybar at the P node and Y at the N node to aid in the development of the XNOR gate. XNOR of G and B will be present in the Out. The dynamic stage will work as an inverter; therefore, resultant output would be XOR. The XOR configure DGDI cell is depicted in Fig. 3.2. The GDI circuit's output equals | VDD-Vthn| when both the X and Y inputs are set to "1". Similarly, in the case when X = 0 and Y = 1, the GDI cell's output would be |Vtp|. Consequently, out of GDI has inadequate swing with these input combinations.

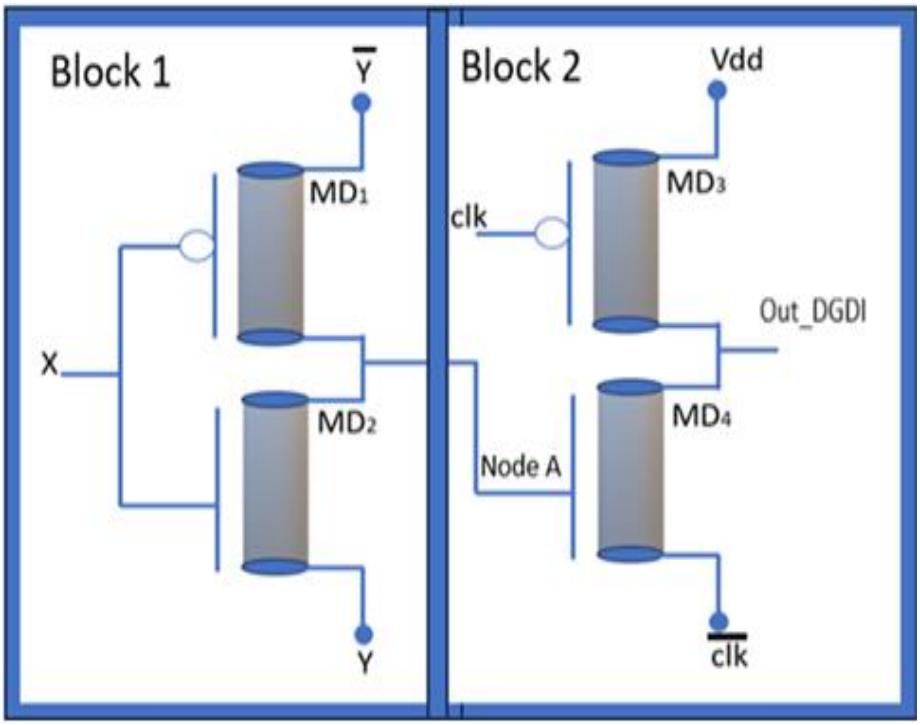


Fig. 3.2: XOR configured DGDI cell

This problem is increasingly common, particularly with circuits that have three inputs. However, Fig. 3.3 illustrates the suggested DGDI XOR. In compared to a traditional GDI XNOR circuit, the circuit enhances the output swing, allowing the suggested design to achieve a rail-to-rail swing because of the applied dynamic circuit structure [17]. Furthermore, a GDI circuit's power consumption is further reduced by applying a CLK signal in a dynamic circuit layout.
Dynamic logic gates work by temporarily storing electric charges at the nodes connected to the internal parasitic capacitances. Clock signals are necessary for the dynamic logic type digital circuits to update the internal node voltages. This problem makes it possible to create basic sequential circuits, which have the well-known advantages of using less space and power than alternative static or traditional CMOS logic types.

The DGDI circuit functions in the following manner: The M2 transistor charges the load capacitor to the VDD level when the CLK signal is "0." However, because transistor M1 uses a CLK signal, when the CLK signal is "1" and the logic levels of the A and B inputs differ, the M1 transistor cuts off, and the output signal equals the voltage that was previously stored in the load capacitor—

the same value as the pre-charged state (VDD). Lower delay and dynamic power consumption numbers are the outcome of this problem. Figs. 3.4.a and 3.4.b depict the transient behaviour of the dynamic gate diffusion input with various combinations of the A and B inputs. Table 3.1 displays the DGDI truth table

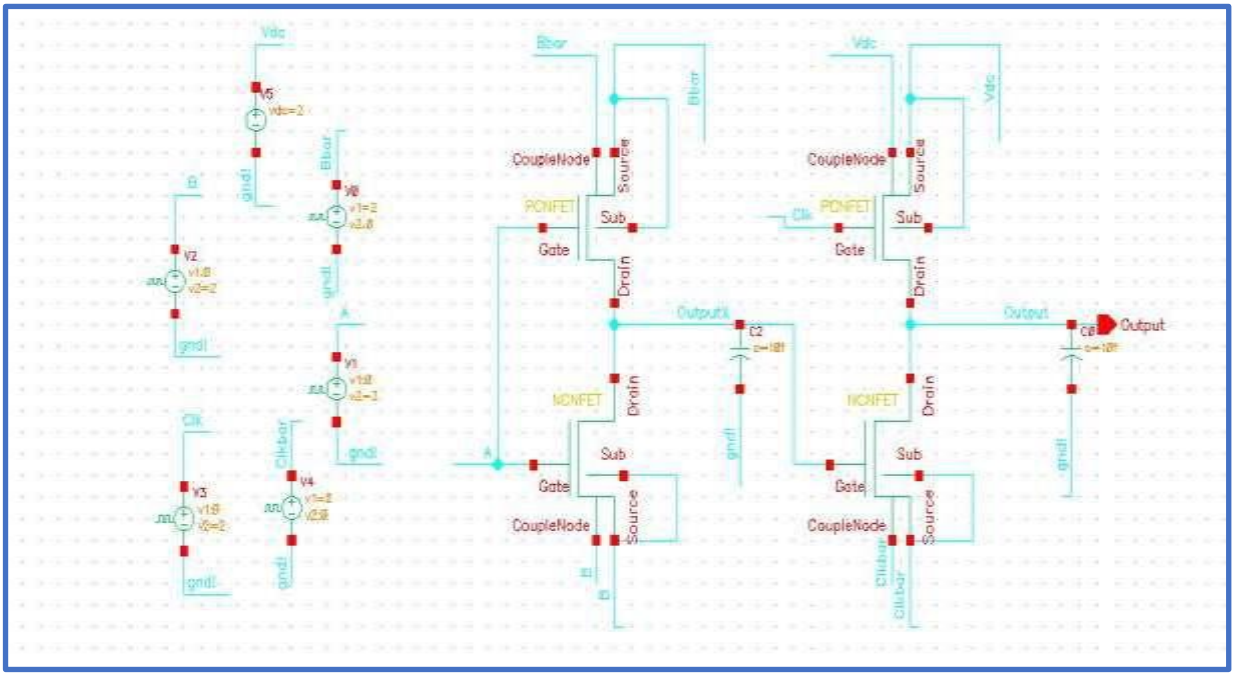


Fig. 3.3 Dynamic GDI Circuit Schematic in Candence

As demonstrated by the transient response, the XOR gate has been properly validated and produced the intended output for all input values. Additionally, it was noted that all input combinations yielded full swing. Delay calculation done by keeping X=1 & does the transition in Y 1 to 0. Delay value obtained 122.7 ps as shown in Fig. 3.4.b. Power Consumption for DGDI observed at 1.62µW and same is shown in the Fig. 3.5.

Table 3.1: DGDI Cell Output

G	P	N	GDI Cell (Node X of DGDI) XNOR	Dynamic GDI (XOR)
0	**1**	**0**	**1.998V (Vdd)**	**0**
0	**0**	**1**	**173mV (Vtp)**	**Vdd**
1	**1**	**0**	**0**	**Vdd**
1	**0**	**1**	**1.84 V (Vdd-Vtp)**	**0**

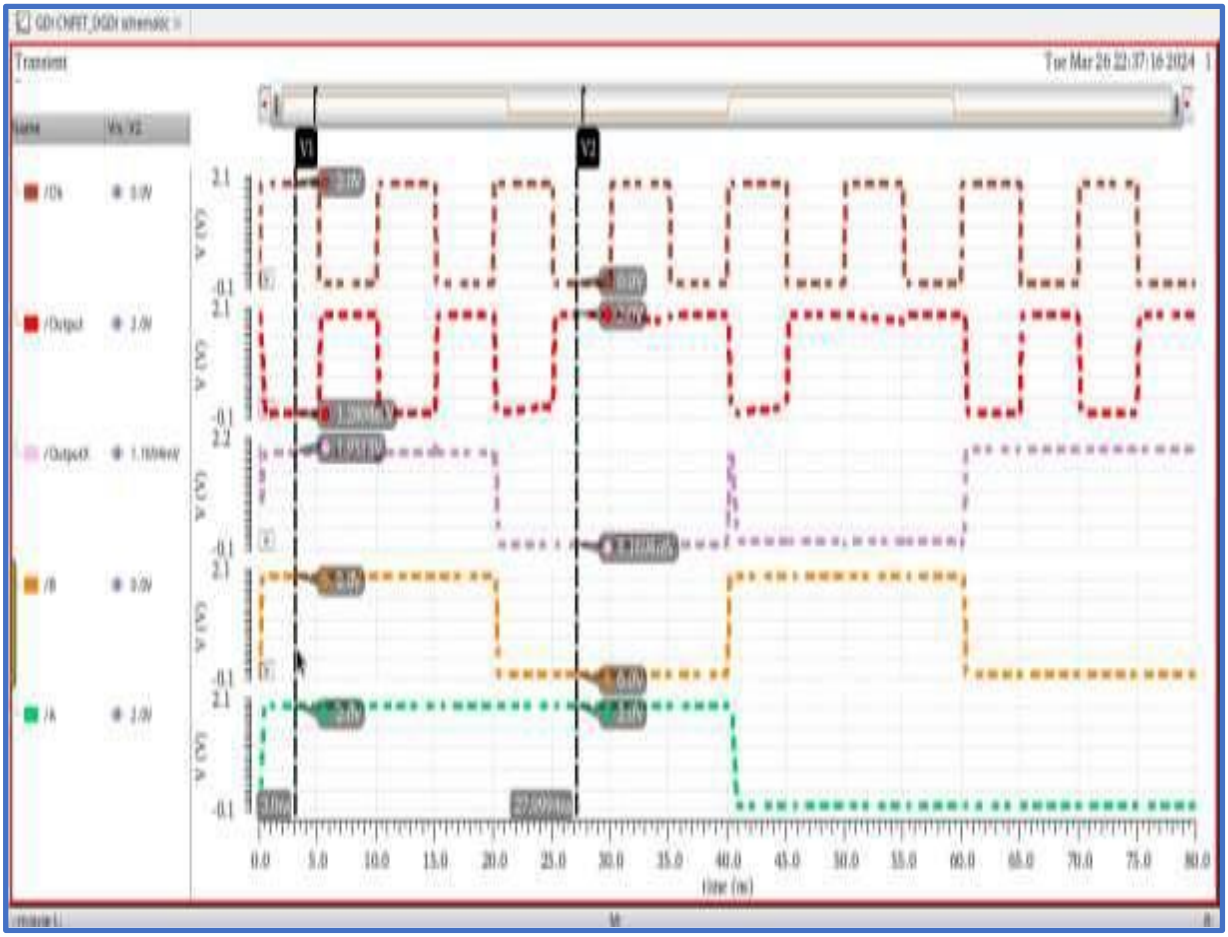


Fig. 3.4.a. Transient Response of the XOR logic based on Dynamic GDI cell

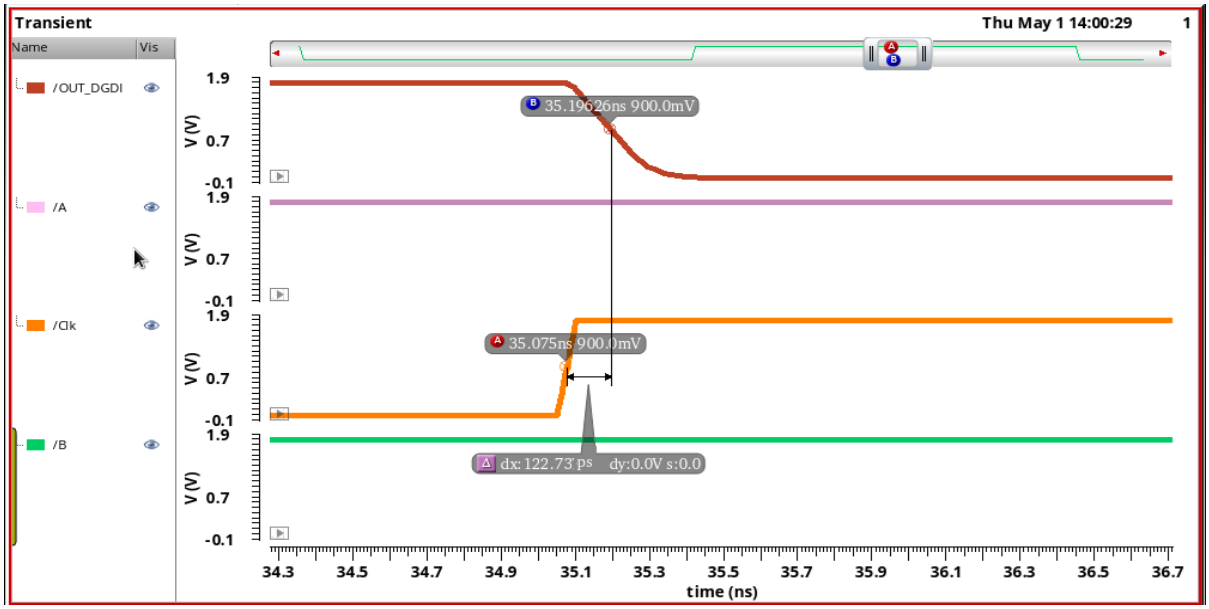


Fig. 3.4.b Transient Response of the Dynamic GDI cell for delay calculation Average

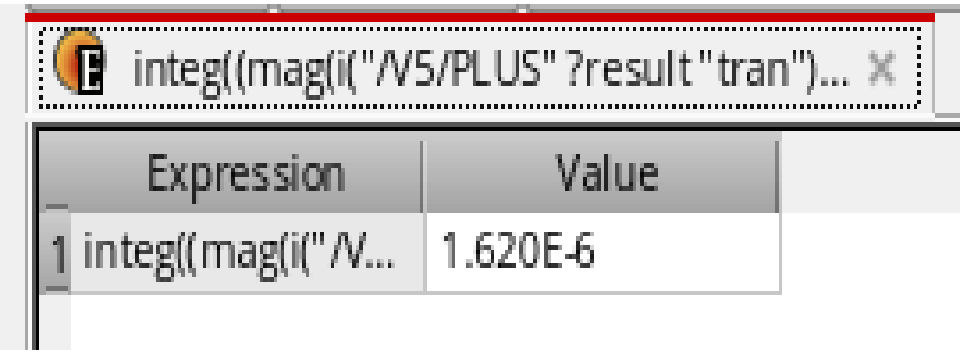


Fig. 3.5. Power Consumption for DGDI based XOR Cell

Inaccurate lithography and uneven CNT development might result in irregularities in pitch variations, changes in nanotube diameter, flaws, and misalignment. It results in changes to the process and might affect the circuit's performance. A 3σ Gaussian distribution is used to account for the ±5% pitch variance. To evaluate the effect of process modifications on the delay and power consumption of XOR gates based on the current DGDI, Monte Carlo simulation was performed for 500 samples. Figs. 3.6 (a), 3.6 (b), show the charts for the delay and power consumption of DGDI. It can be seen that the highest standard deviation is very less.

Fig. 3.7 depicts the layouts of XOR logic based existing DGDI drawn in the Electric VLSI Design System 9.07 [18]. The layout area is found to be 3192 nm2

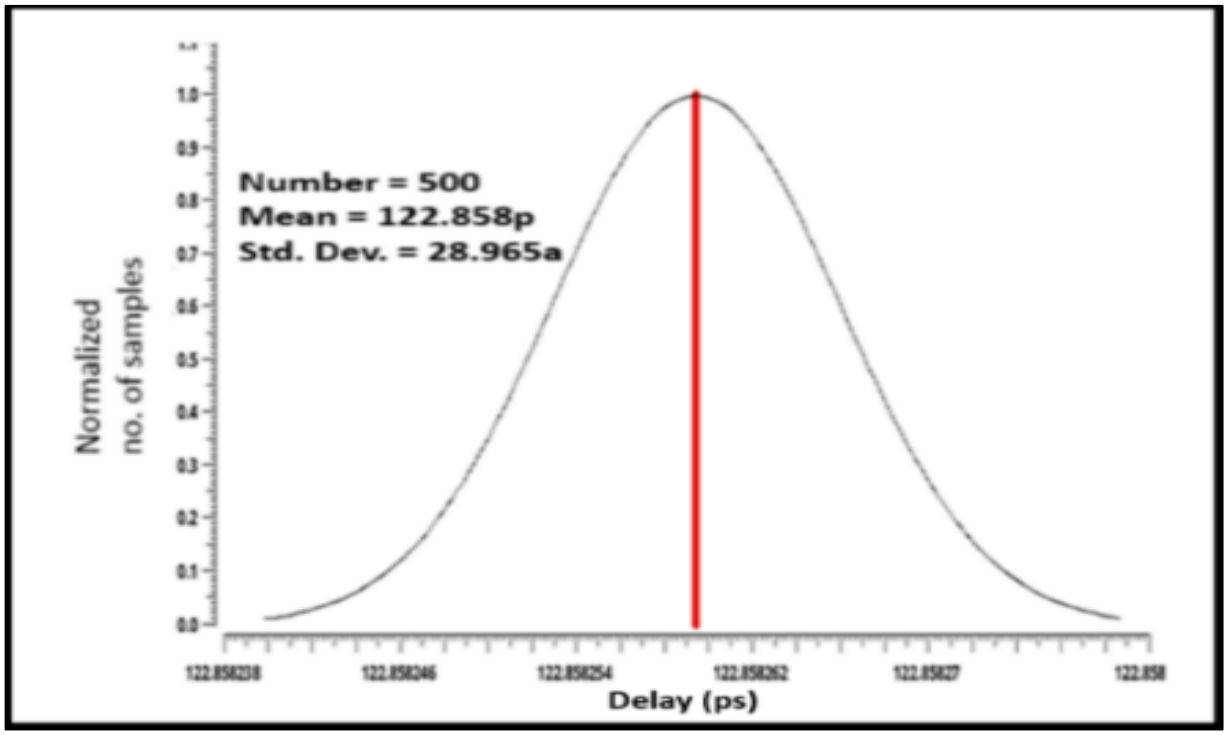


Fig. 3.6.a Monte-Carlo Simulation for delay by varying pitch 5% DGDI

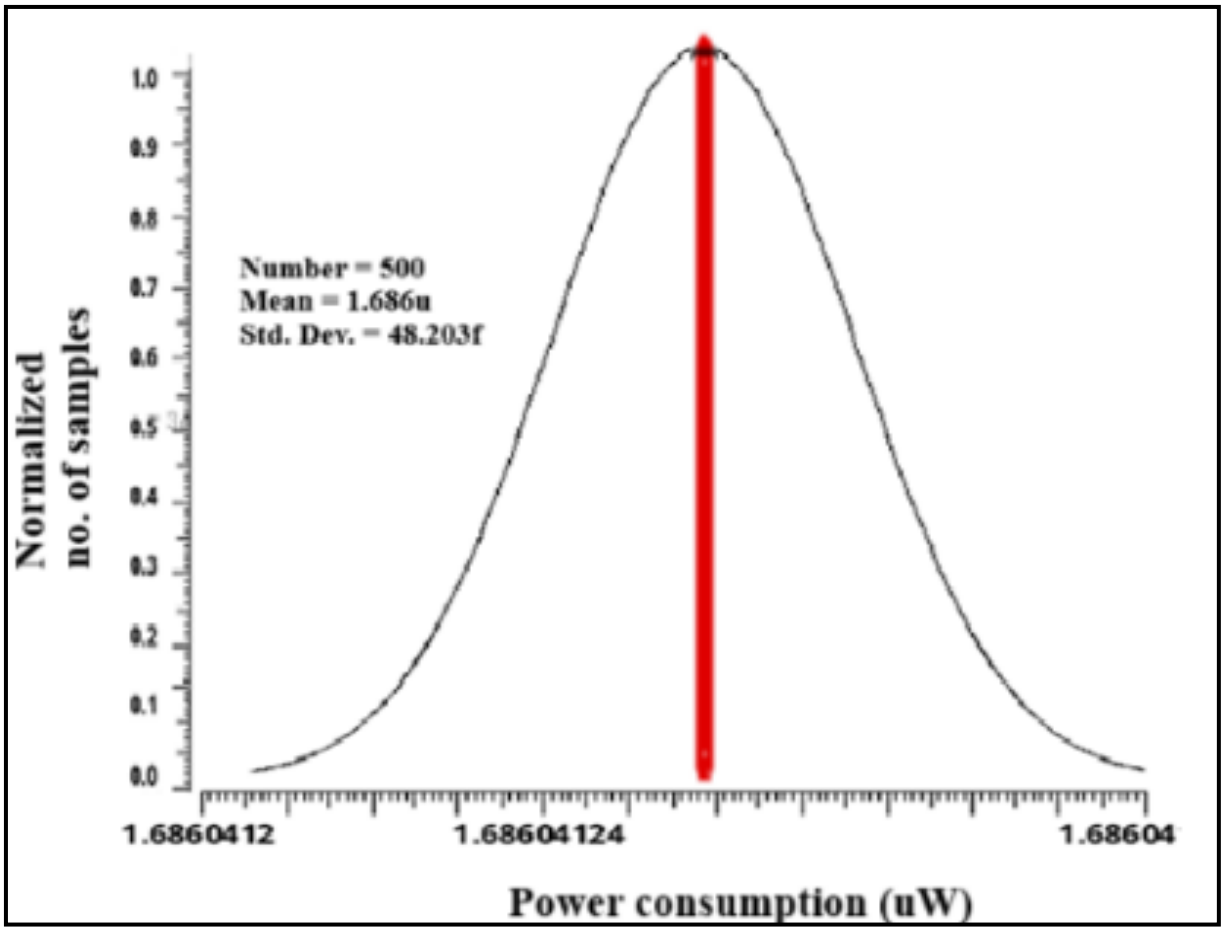


Fig. 3.6.b: Monte-Carlo Simulation for power consumptions by varying pitch 5% DGDI

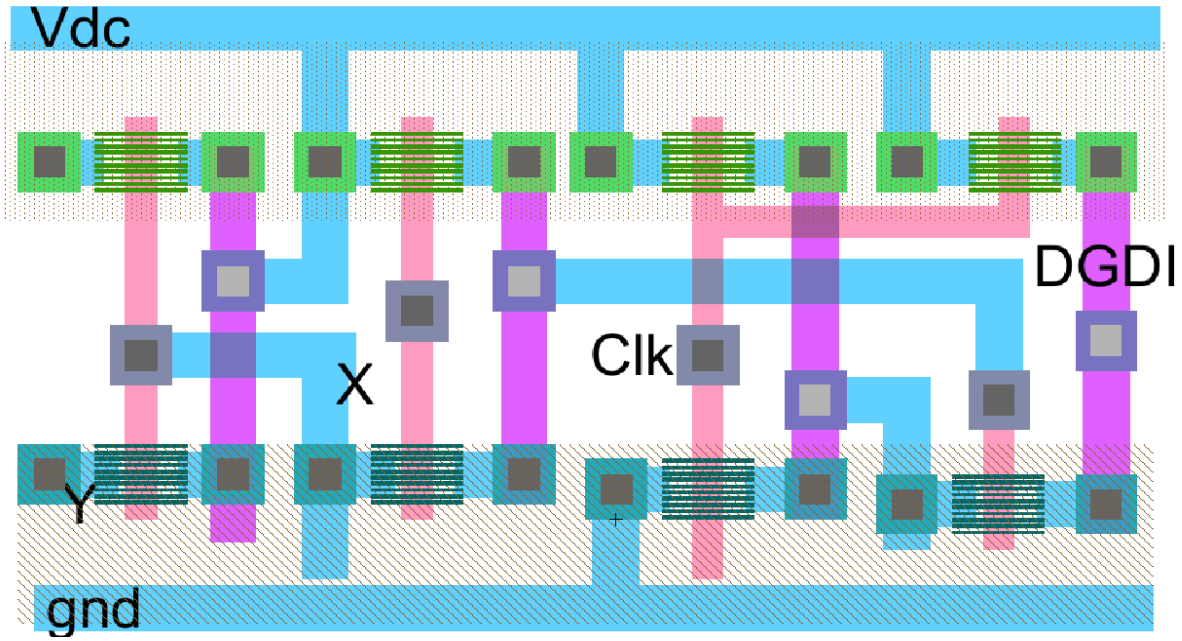


Fig. 3.7: Layouts of XOR based on DGDI cells

3.3 Effect of Load Variation and supply variation

Effect of load variation for DGDI cell, where load capacitance increase from 1f F to 10f F with the step size of 1f F were also studied for this cell. As predicted, delay and power expenditure both rises with load capacitance. Since with increase in the load capacitance, circuitry will take more time in charging and discharging, and hence delay as well power consumption increase, same is depicted in the Figs. 3.8 and 3.9.

Also, Power supply variation can impact the circuit delay. With a reduced supply voltage lessens the gate drive strength, thereby increasing the gate delay. The same has been observed and shown in the Fig. 3.10 and 3.11. To do the transient analysis for the circuit with varying VDC, value of the VDC varies 10% from the typical value of 0.8V as shown in Table 3.2.

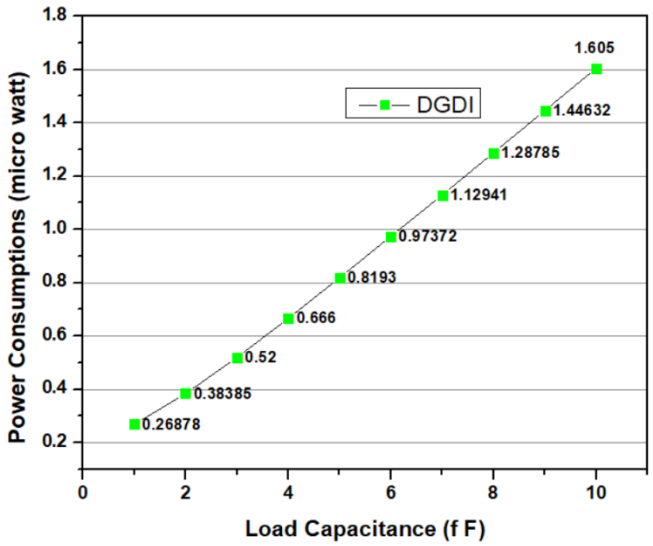


Fig. 3.8: Impact of the load Capacitance variations on the power consumptions

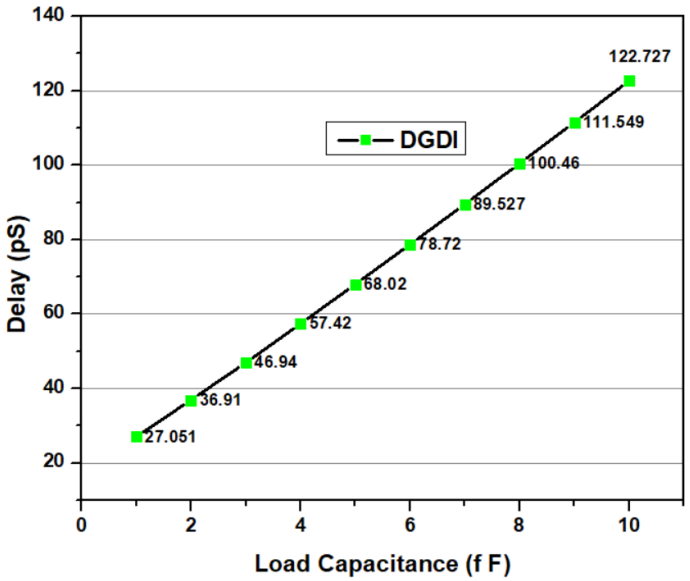


Fig. 3.9: Impact of the load Capacitance variations on the delay

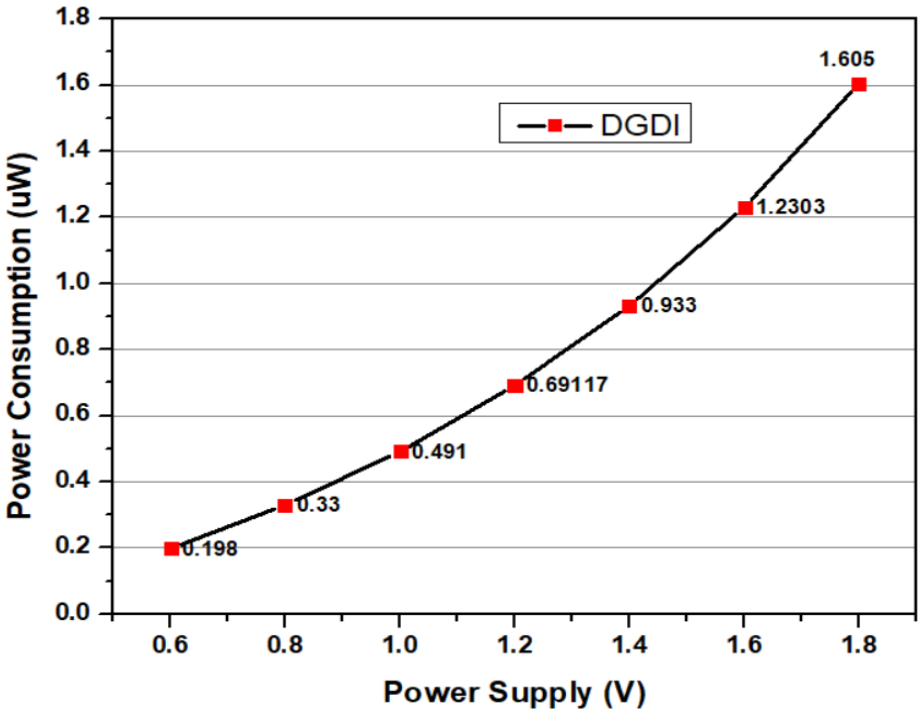


Fig. 3.10: Effect of Power supply variations on the power consumptions

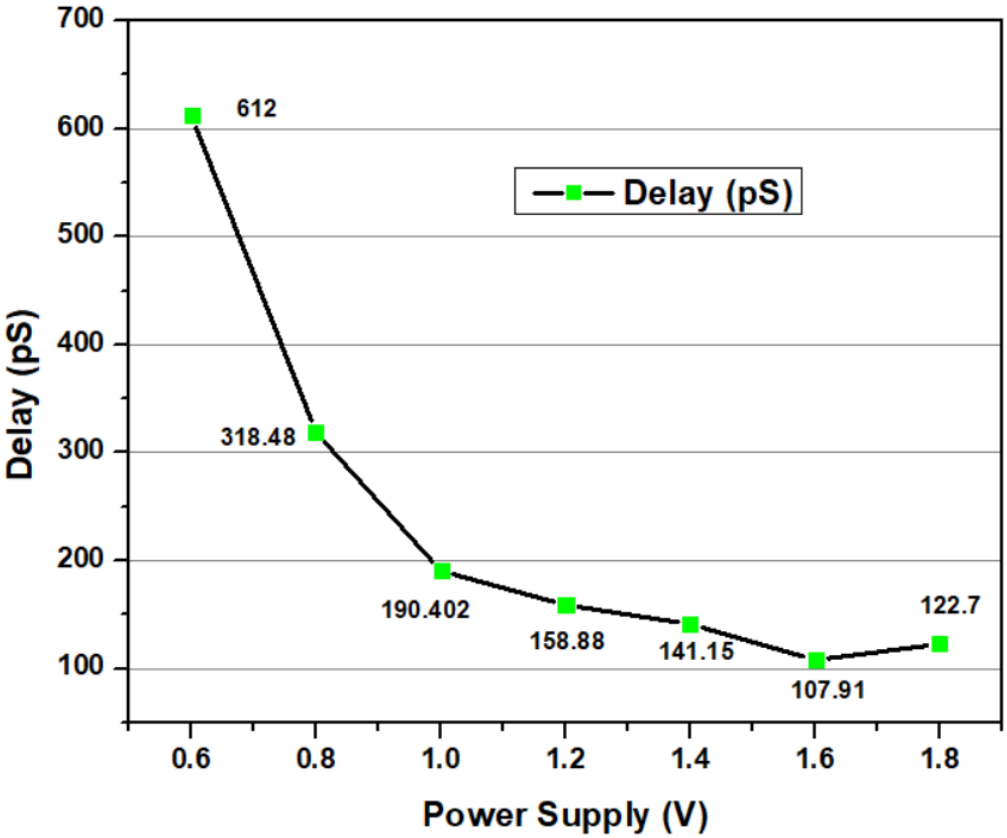


Fig. 3.11: Effect of Power supply variations on Delay

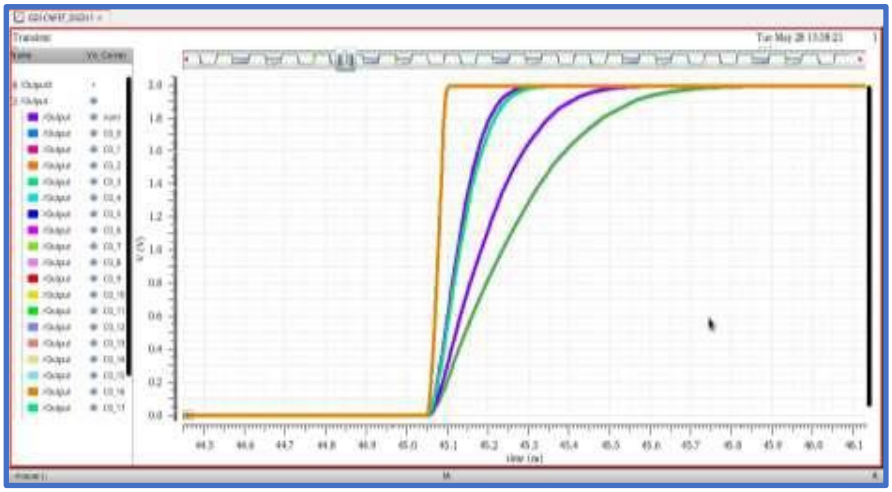


Fig. 3.12.a Rise Time Varies with Load capacitance

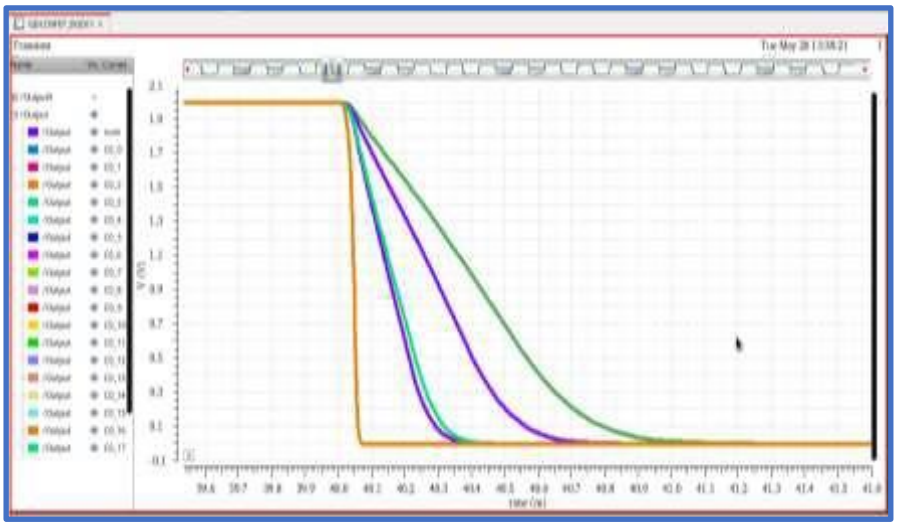


Fig. 3.12.b Fall Time Varies with Load capacitance

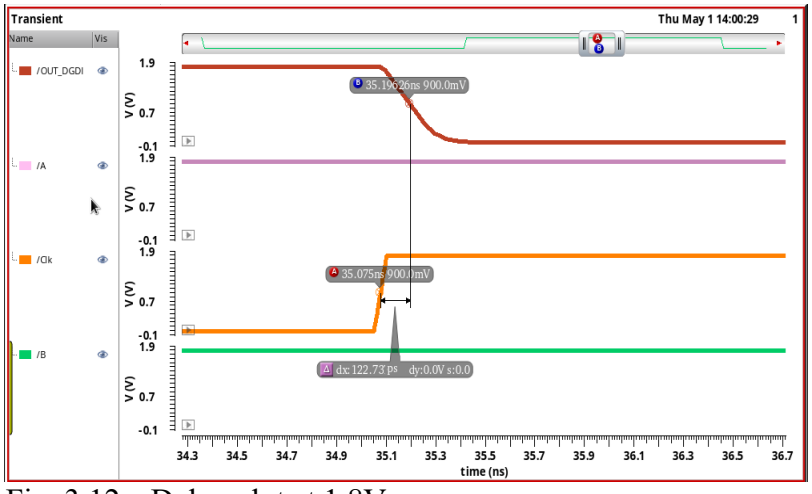


Fig. 3.12.c Delay plot at 1.8V

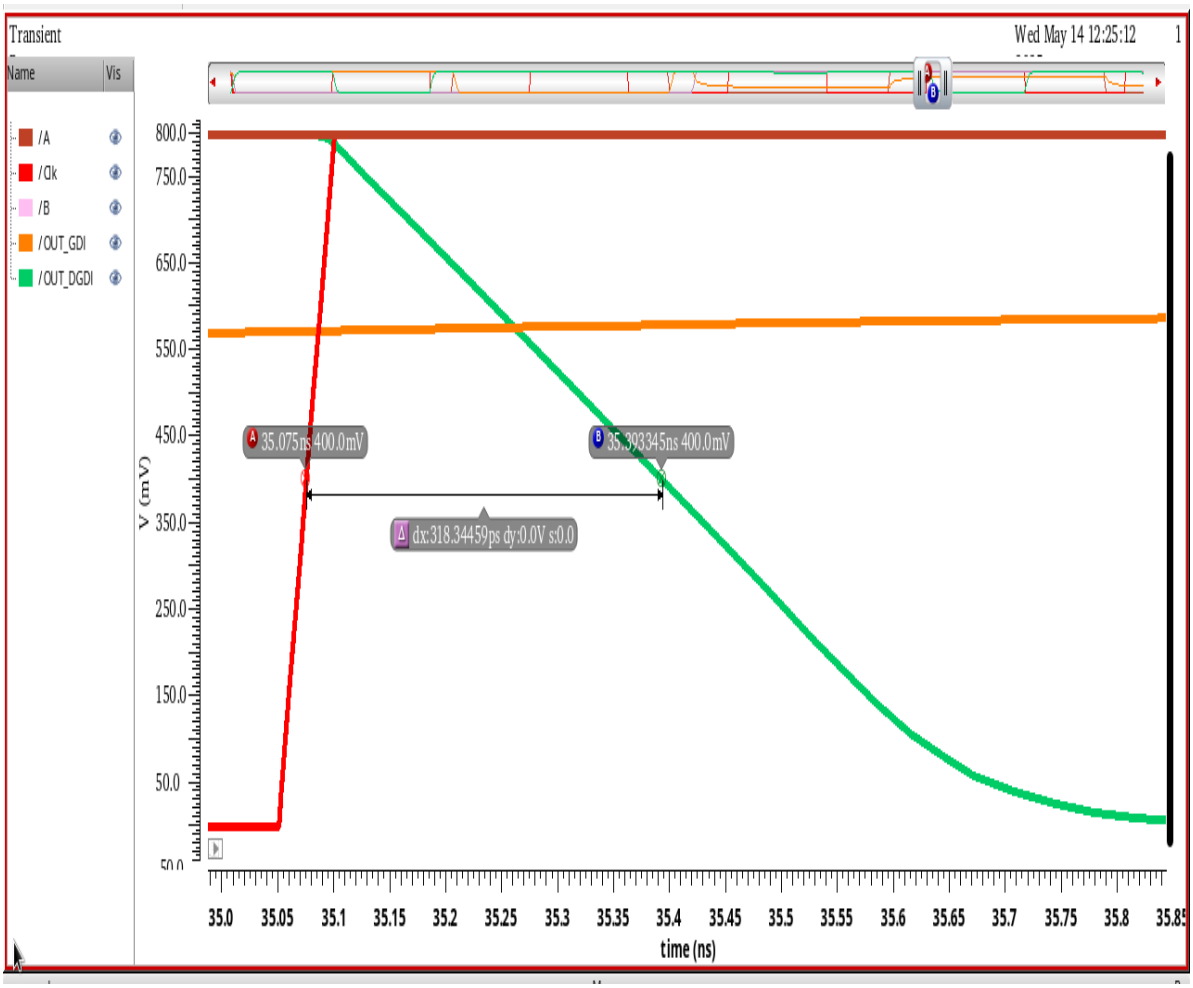


Fig. 3.13: Delay plot at 0.8V

Table 3.2: Delay varies with Supply Variation

Vdc	Delay (pS)	Power consumption
0.6	612	0.198
0.8	318.48	0.33
1.0	190.4	0.491
1.2	158.88	0.691
1.4	141.15	0.933
1.6	107.91	1.23
1.8	122.7	1.605

3.4 Full adder using the DGDI logic

As the primary component of full adder circuits, the XOR gate is extremely important. The total efficiency of the full adder may be considerably increased by improving the design using carefully chosen circuit characteristics. Simplifying logic equations as much as feasible is crucial to creating the perfect logic circuit in terms of speed and chip size. Faster processing and less space are guaranteed with a simplified design. Additionally, circuit speed is improved by reducing the number and size of transistors, and power consumption is reduced by lowering the supply voltage, albeit at the expense of greater delay.

Designers should concentrate on circuit topologies that are optimal for PDP, latency, and power consumption in light of these factors. Consequently, a complete adder circuit is used in the suggested design, which is based on the equation (1), (2) and (3).

The "B⊕C" factors in both the SUM and COUT outputs reduce the number of transistors needed, according to the provided calculations. To further reduce the number of transistors, the suggested design also uses the GDI approach. The dynamic technology is smoothly combined with the traditional GDI approach to maximize efficiency, hence lowering chip area and power consumption.

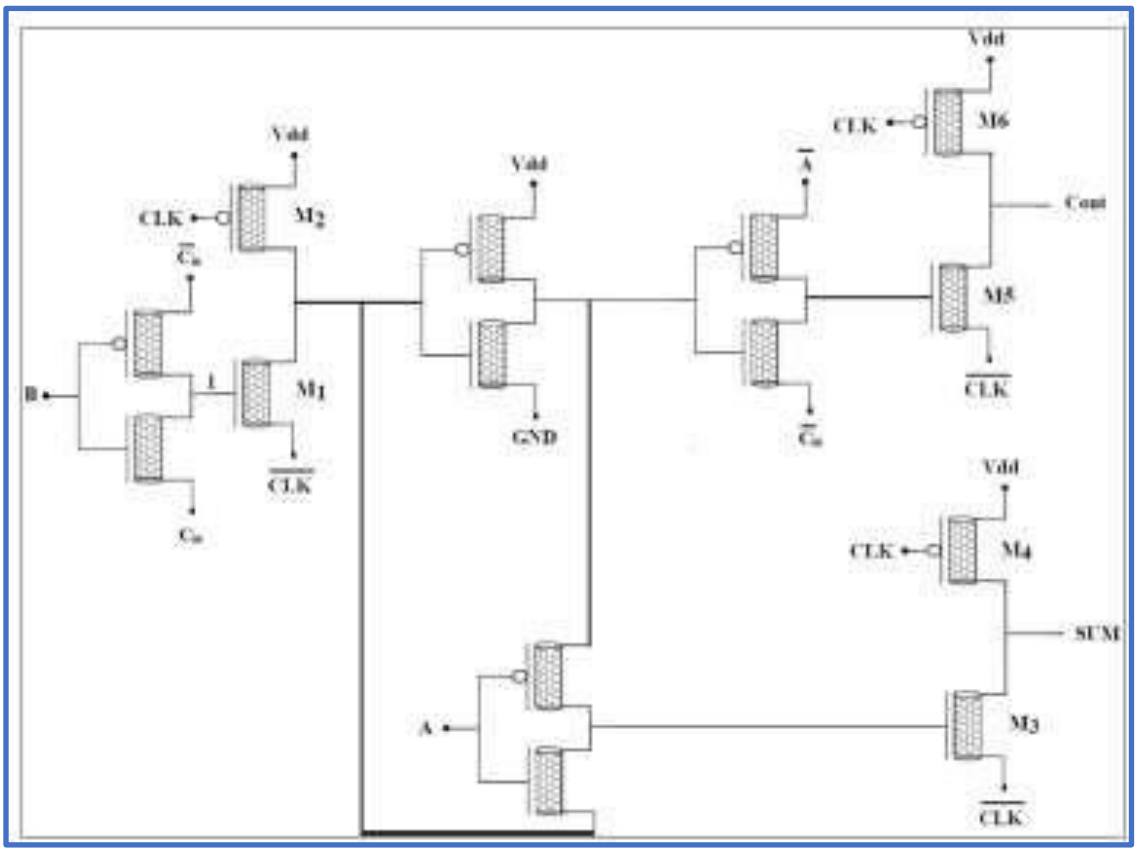


Fig 3.14.a: Full Adder circuit using DGDI [16]

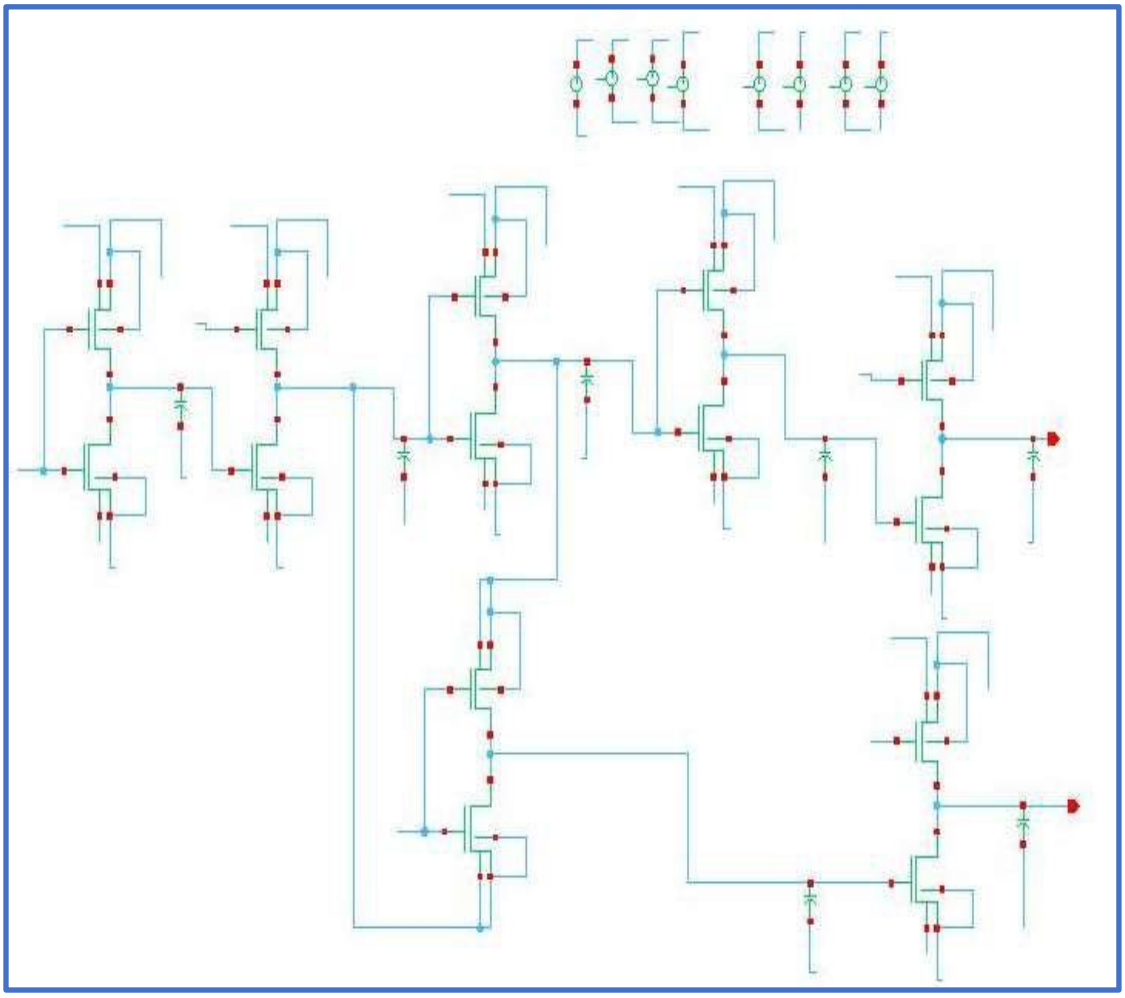


Fig. 3.14.b: Full Adder using DGDI in Cadence

The T1, T3, and T5 transistors are "OFF" when the CLK is set to "0," allowing the CL capacitor to be charged to the VDD level (pre-charge phase). The T2, T4, and T6 transistors, however, turn "OFF" when the CLK signal is "1." In contrast, as shown in Figure 29.a, the load capacitor CL discharges to ground if the GDI block output is higher than the threshold voltage of the T1, T3, and T5 transistors; otherwise, it maintains its previous logic level. Therefore, the suggested combination of GDI and dynamic circuit approaches is realized by using the CLK input signal at the source terminal of the T1, T3, and T5 transistors.

Full adder implements with basic DGDI cell. After successfully, save and check the full adder as shown in Fig. 3.14.b. The output of the full adder SUM and Carry were analysed. Since the circuit based on the dynamic logic, when clock is at logic 0, output pre-charged, therefore SUM And carry output has logic 1 as output. Whenever clock goes to the logic 0, based on the input of the adder, SUM and carry logic can be realized. When Both input are 00, sum and carry shows the logic 0. When One input transit to 1, SUM output goes to logic 1 and carry stays at previous logic i.e. logic 0.

When both the input is high, SUM shows logic 0 and Carry shows logic 1 as a output.

To obtained the SUM and Carry output as shown in Fig. 3.14.c, Signal X, Y and Z has a period set at value of 80ns, 40ns and 20ns respectively. Clock signal has a period of 10ns. All input has a duty cycle of 50% and pulse width of 0.8 V. As can be seen in the figure, all the logic based on input combination has been verified. Fig. 3.14.d depict the delay plot for full adder based on the DGDI cell.

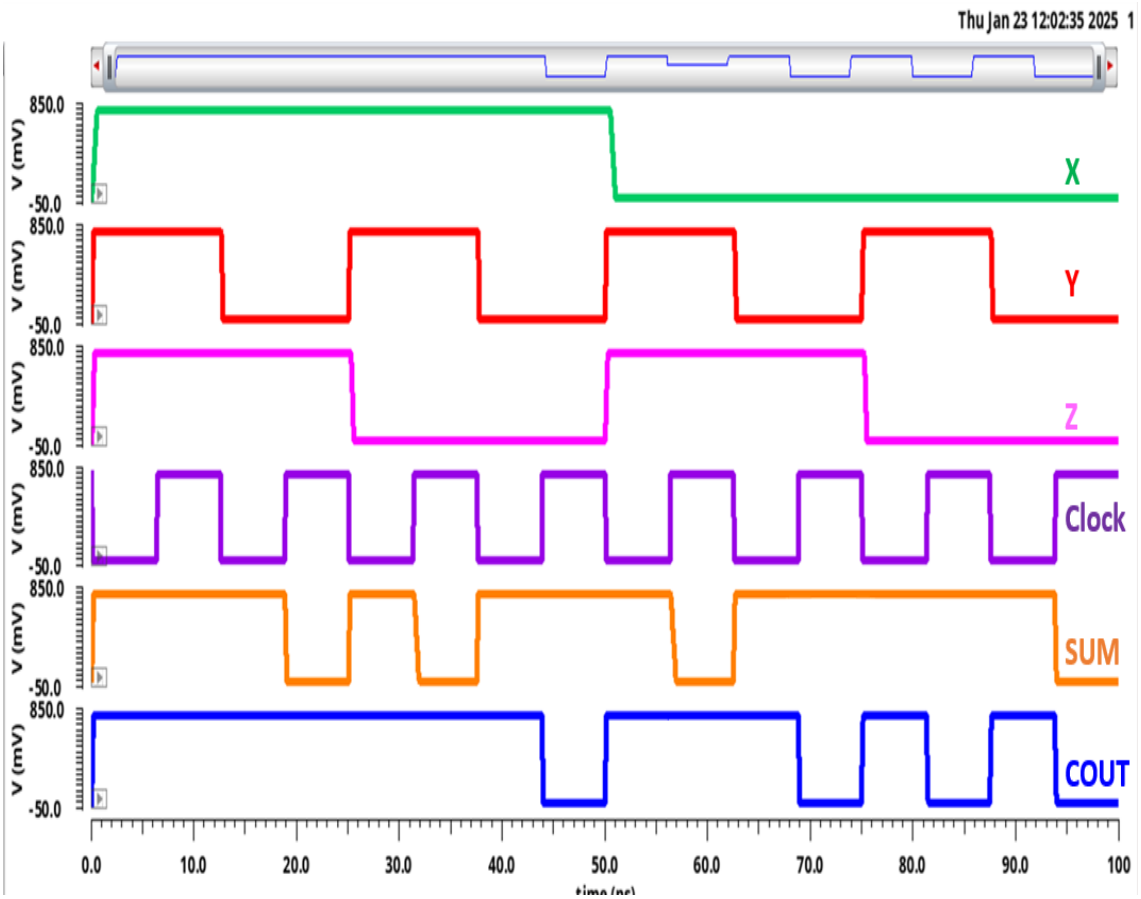


Fig. 3.14.c Transient Response of Full Adder

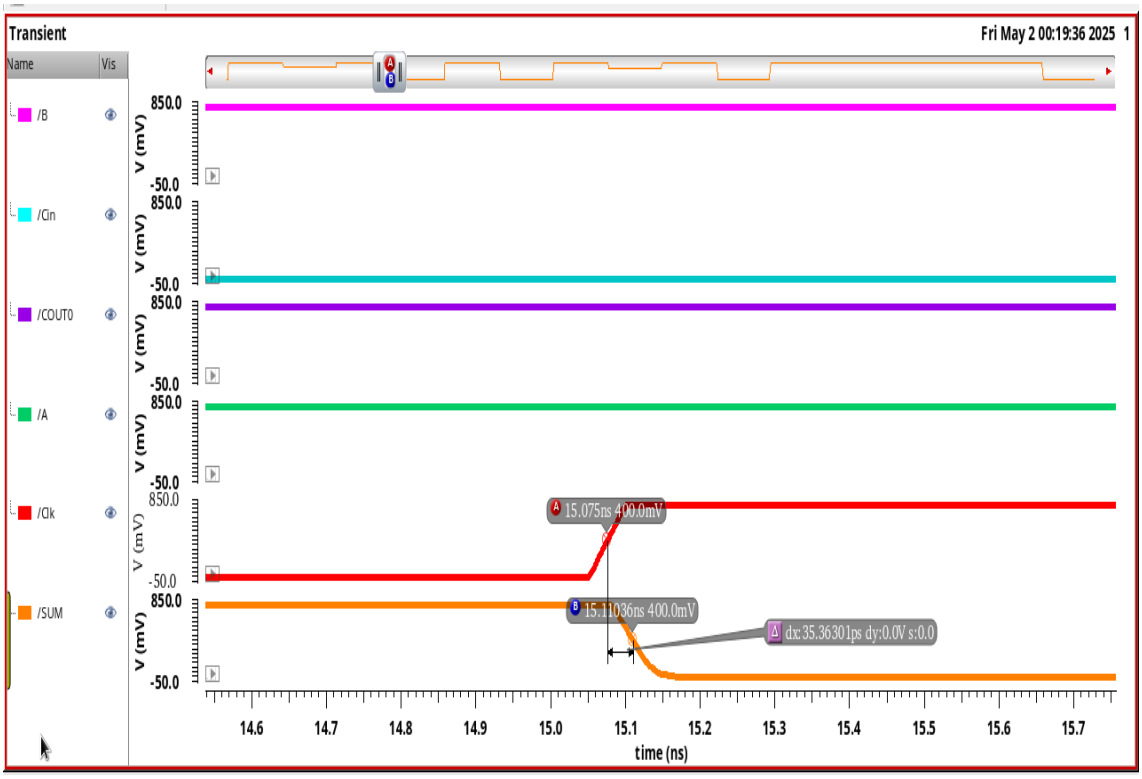


Fig. 3.14.d Transient Response of Full Adder for delay calculations

3.5 Ripple Carry Adder

The ripple carry adder based on the dynamic gate diffusion input was also designed in accordance with the RCA architecture, as illustrated in Fig. 2.22,. Cadence Virtuoso was used to imitate the Ripple Carry Adder (RCA), which is based on Dynamic Gate Diffusion Input (GDI). The following input values were used throughout the simulation:

- Period of A: 120 nm
- Period of B: 60 nm
- Period of C: 30 nm with a duty cycle of 50%
- Voltage range of the input voltage: 0-0.8V
- Vdc: 0.8V

RCA's transient response is depicted in the Fig. 3.16.a and 3.16.b. Additionally, a simulation was conducted for the 4-bit array. The initial carry-in (Cin) was set to 0, while Signal A and Signal B were set to 0001 and 0000, respectively. The output obtained matched the values listed in the truth table. As a result, the Sum was 0001, and the carry-out (Cout) was 0000. The circuit was also tested with Signal A and Signal B both set to 1111. Under these conditions, the resulting Sum was 1110 and the Carry-Out (Cout) was 1111. The schematic of the Ripple Carry Adder is shown in the truth table.

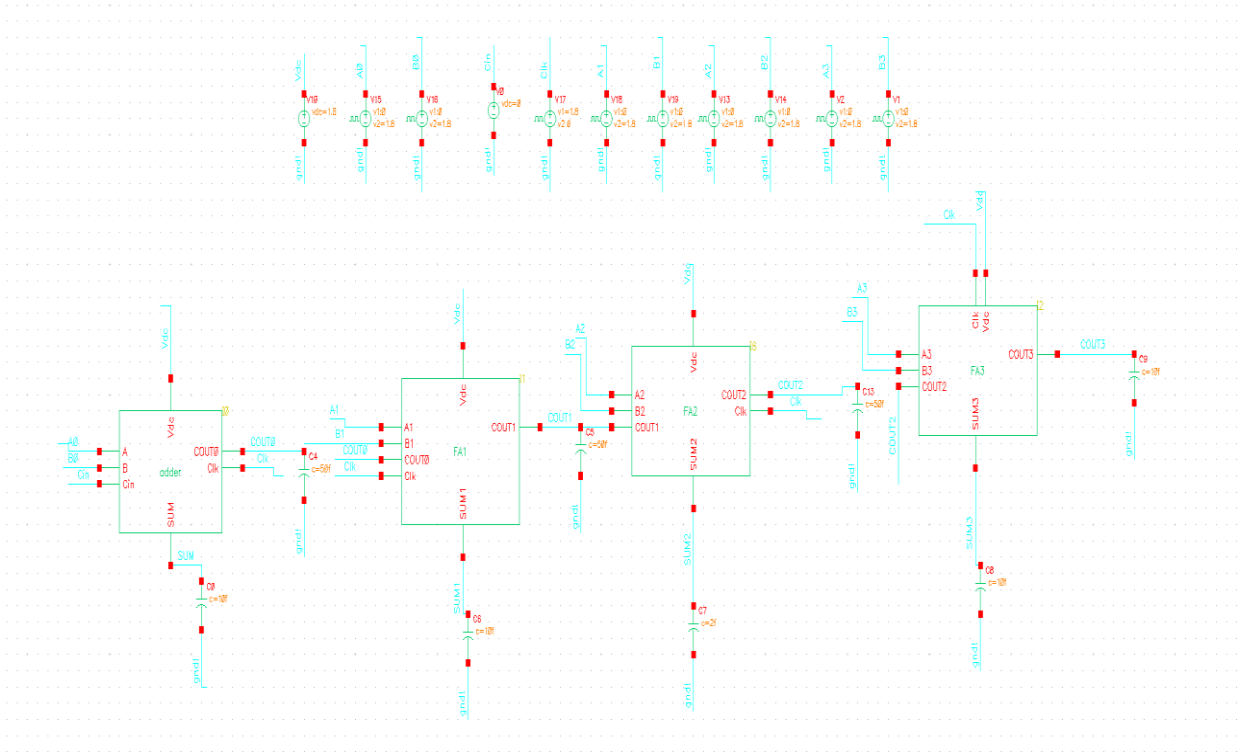


Fig.3.15: Architectural Layout of the RCA

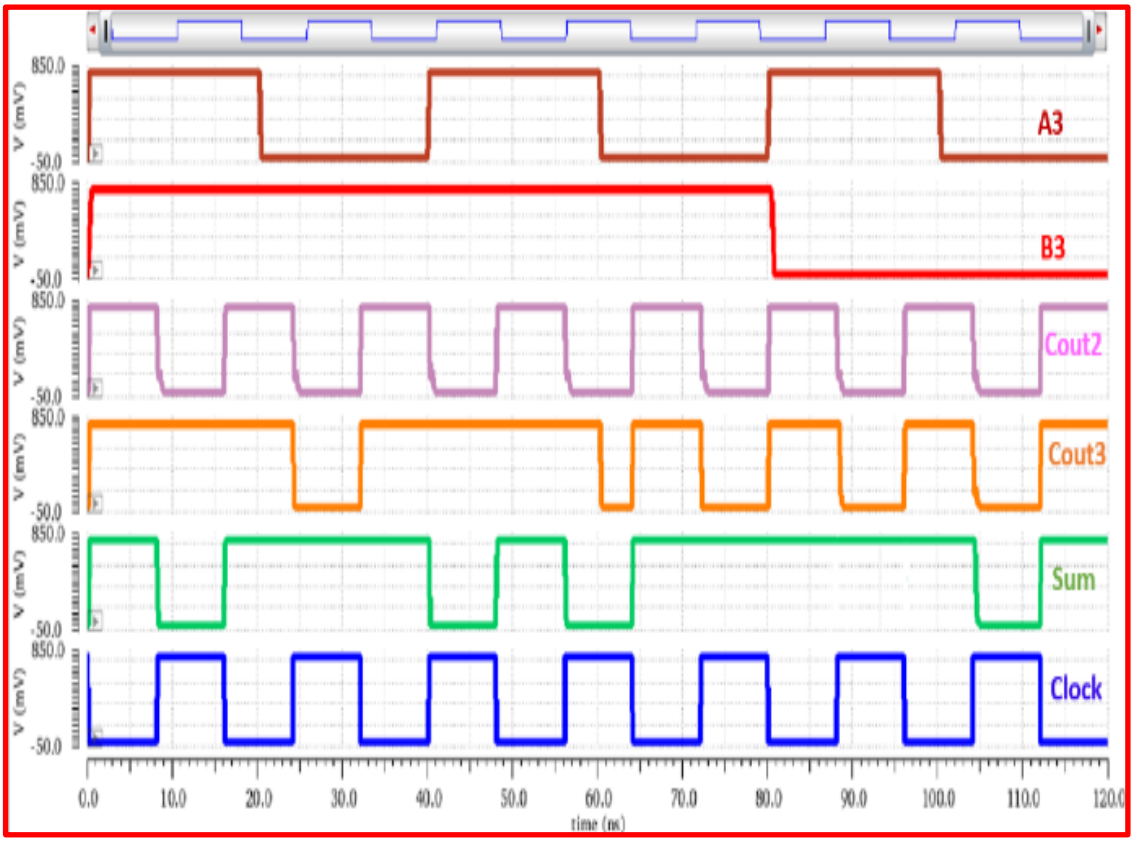


Fig. 3.16.a: Transient Behavior of 4 bit- RCA based on DGDI cell

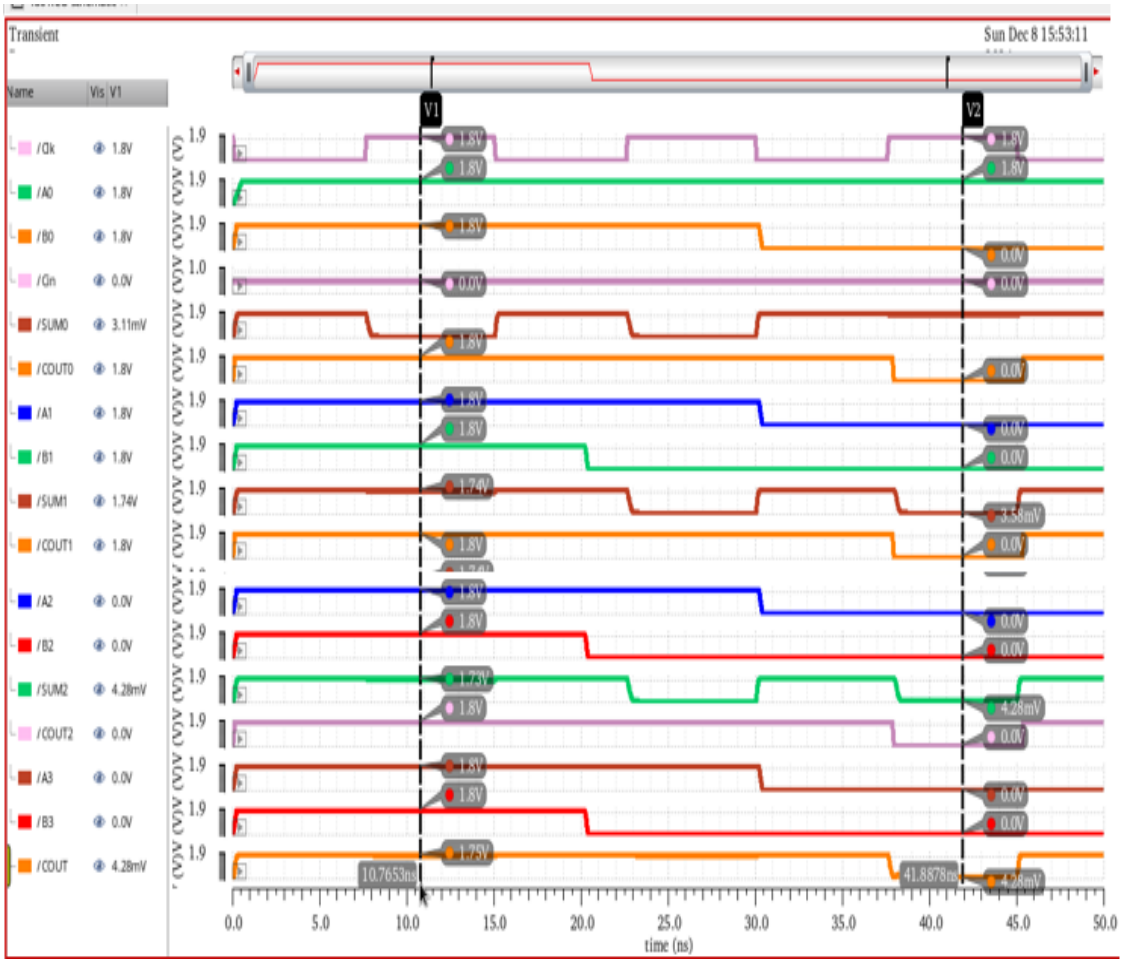


Fig. 3.16.b Transient behaviour of 4-bit RCA based on DGDI cell

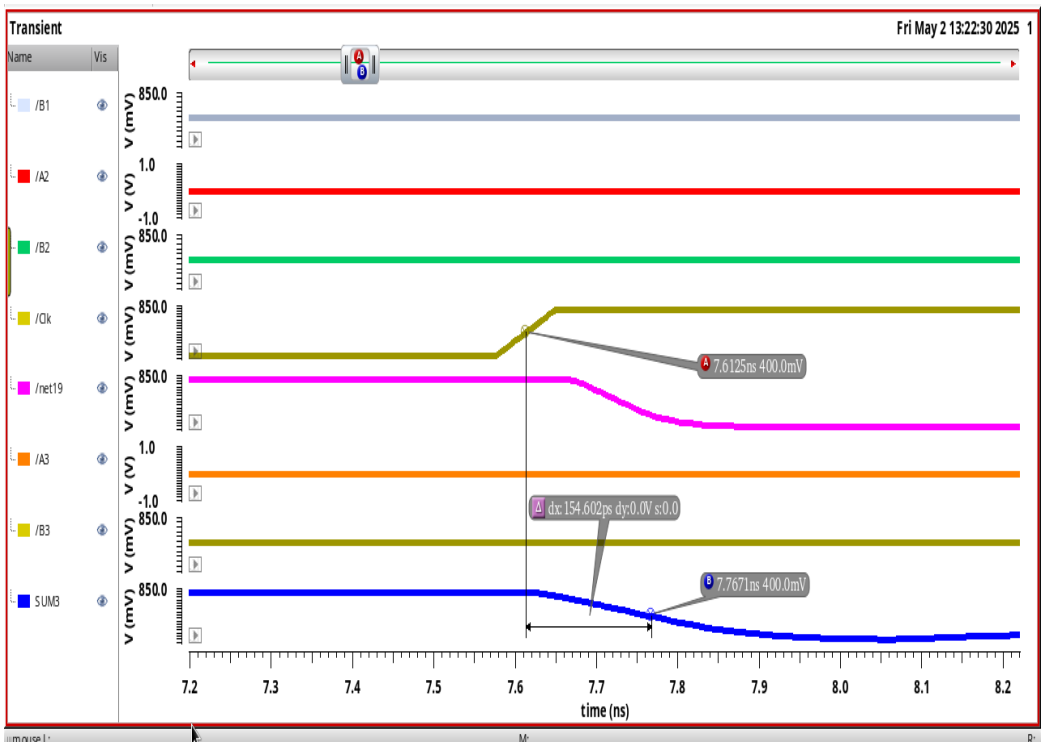


Fig. 3.17: Transient Response of Ripple Carry Adder for delay calculations

3.6 Multiplier (2x2)

A 2x2 multiplier circuit that produces a 4-bit binary output (S3 S2 S1 S0) that indicates the product of two 2-bit binary values (X1 X0) and (Y1 Y0) as input. The multiplication is calculated using two half-adder operations and AND gates. The block diagram used to create the 2x2 multiplier is seen in section 2.6.

Four outputs are obtained from the initial circuitry: X0Y0, X1Y0, X0Y1, and X1Y1. The product of X0Y0 results in S0, which is the least significant bit (LSB) of the multiplier output (B). X1Y0 and X0Y1 are added using a half adder (HA1) to produce the S1 bit. The first half adder's (HA1) carry output and X1Y1 are added to form the S2 bit. The second half adder (HA2) is carried out by the S3 bit. Fig. 3.18 displays the simulated waveforms for each input and output, while Fig. 3.19 displays the delay graphs for the 2x2 multiplier. In addition, a delay of around 69.4 ps was recorded in order to get the multiplier output's MSB. About 0.5207 µW of power is used by the same circuitry.

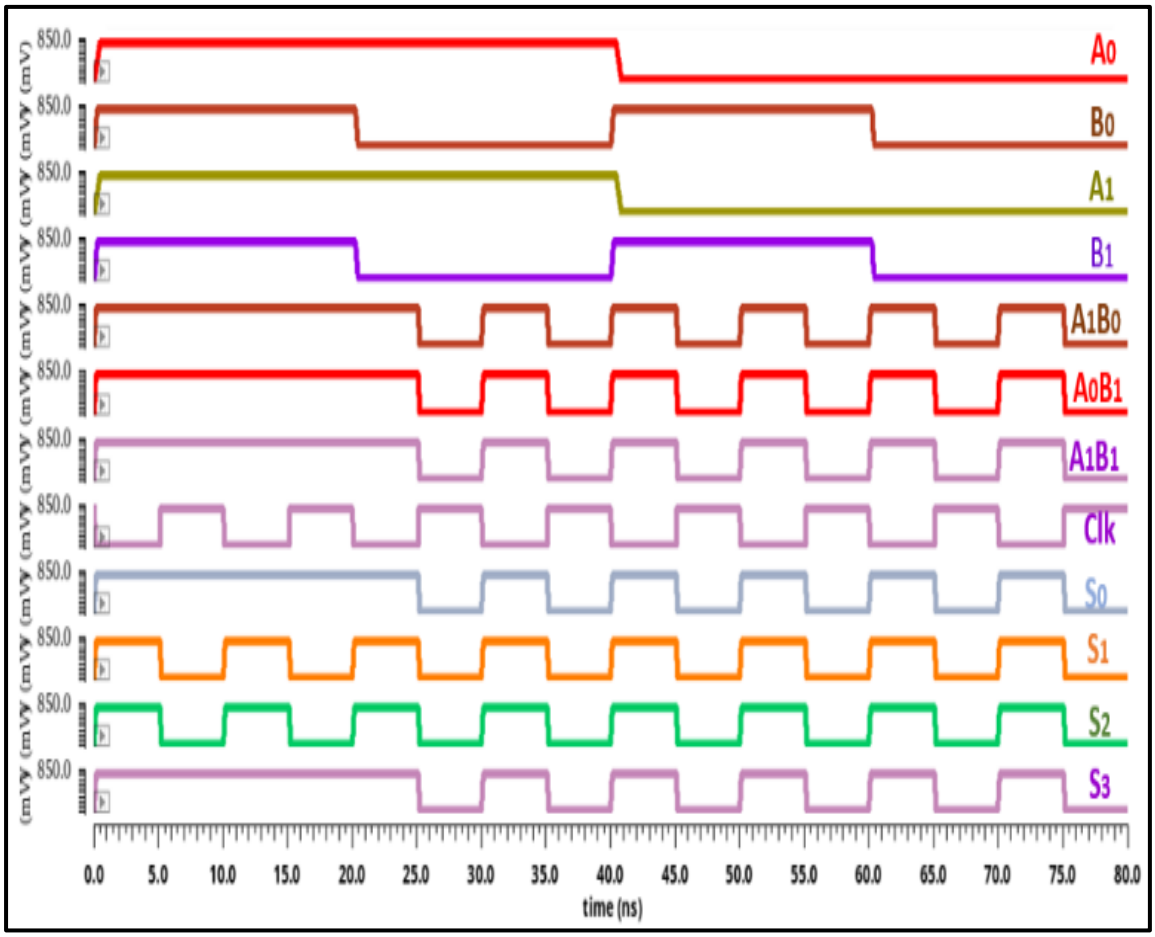


Fig. 3.18: Transient response of the 2x2 multiplier based on DGDI cell

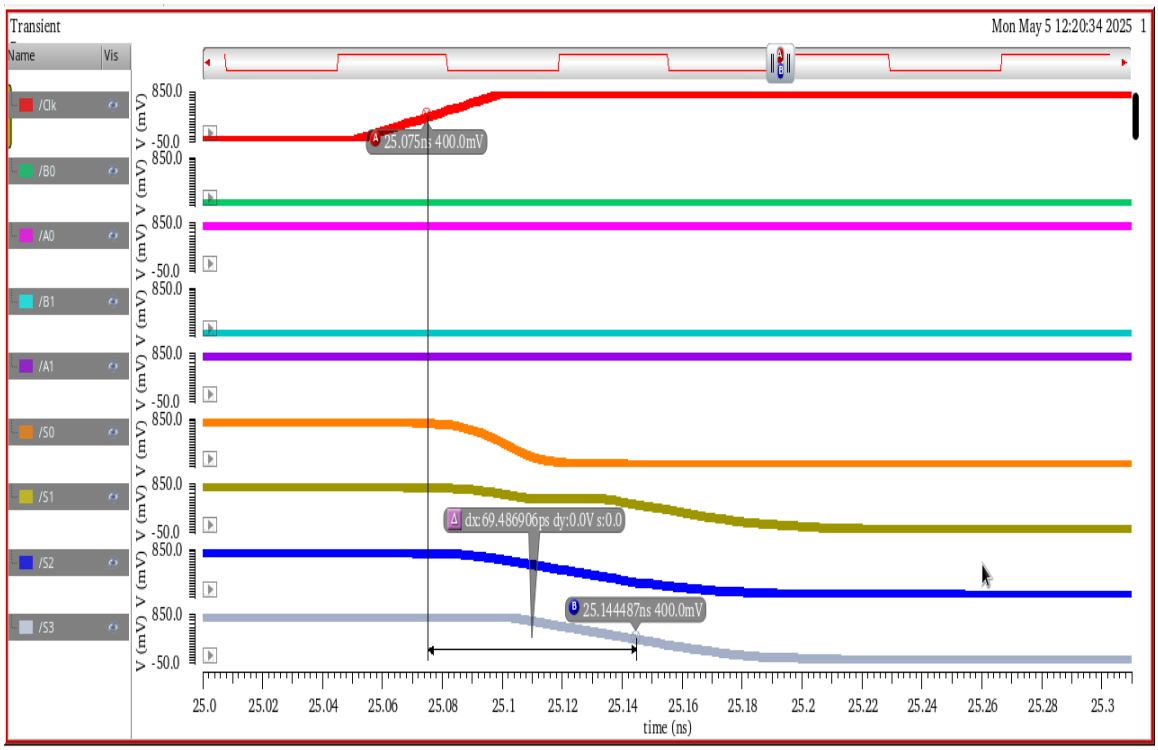


Fig. 3.19: Delay plot for 2x2 multiplier based on DGDI

3.7 Summary

Upon examining the GDI, it was discovered that, in contrast to CMOS-based technology, XOR, full adder, RCA, and multiplier all had lower power usage. Yet, more complicated circuitry cannot be investigated because of the GDI cell's output's inadequate swing, which also results in increased delay. In order to overcome the similar issue, the DGDI cell was investigated in 2020. The DGDI cells were investigated in this chapter.

After investigating the XOR logic using the DGDI cell, a full adder was built using this logic gate. Following that, a 4-bit ripple carry adder was also put into use. Additionally, the 2x2 multiplier circuitry was designed and implemented using the DGDI cell. All of the circuitry's DGDI-based performance metrics, including latency, power consumption, and PDP, parameters are summarized in the Table 3.3.

Table 3.3: Different Circuitry based on DGDI Cell

Logic Gate	Delay (pS)	Power Consumptions (µW)	PDP (E-18)
XOR Gate (1.8V)	127	1.6	203.2
Full Adder (0.8)	35.36	0.127	4.49
RCA (0.8)	154.6	0.41	63.38
Multiplier (0.8)	69.4	0.5207	36.13

Chapter 4: Combinational circuit based on Dynamic Transmission Gate Diffusion Input based Circuit

4.1 The DTGDI Cell

The GDI design strategy is effectively used as a low-power solution, benefiting from the low transistor count and circuit complexity, as XOR logic is implemented with only four transistors [19]. But in GDI-based logic implementations such as XOR/XNOR, the threshold voltage drop limits the output swing. In battery-operated devices, the combination of the GDI and a static circuit may result in large leakage current in static mode. Additionally, the transistors in the next static circuit will have a low current drive, which will increase the delay. Eventually, GDI technology was also included into CNTFET technology [20].

Further, The DGDI based XOR gate (Fig. 3.3) uses 6 transistors and the output swing issue is resolved in DGDI, but there is full swing problem at intermittent node (input of dynamic block) which leads to lower driving capability of evaluate transistor and causes increased delay and power consumption, as discussed in chapter 3. In order to achieve full swing in the CNTFET based GDI logic, the dynamic transmission logic gate has been explored. Since, with this design, the direct connection is never established between the power supply and the ground in dynamic circuits, therefore short circuit power consumption does not exist.

As discussed in chapter 2, about GDI cell. Output may display weak ‘0’ or weak ‘1’ states for particular input combinations, depending on the specific function that the GDI circuit is intended to perform. It is advised to use an extra PCNTFET in parallel with the NCNTFET or vice versa in order to obtain full swing in CNTFET-based GDI logic (FS-GDI) [21]. Because the FS-GDI XOR gate needs 13 transistors, its design is more complicated and uses more power. It should be noted that static logic is the foundation of several implementations [22], [23], and [24]. However, because dynamic logic has fewer parasitic capacitances and no output glitches, it is frequently preferred over static logic [25]. Dynamic circuits avoid short-circuit power dissipation because they do not create a direct connection between the power source and ground. Dynamic GDI (DGDI) [16], which combines a conventional GDI cell with a novel dynamic block, was created to overcome full swing issues and reduce transistor count. Comparing the DGDI XOR gate to FS-GDI, the former employs a substantially a smaller number of transistors—just six. At the intermittent node (the input of the dynamic block), DGDI poses a complete swing challenge even though it fixes the output swing problem. The driving capacity of the evaluation transistor is weakened as a result, increasing delay and power consumption.

Further, CNTFET based TGDI is suggested in research paper [26] and the schematic of the basic TGDI cell based on CNTFET is depicted in Fig. 4.1.a. This cell ensures

full swing output, as it uses NCNTFET and PCNTFET in parallel which are controlled by complementary signals. Table 4.1 shows the logic functions that can be realized with a full swing. The XNOR configured TGDI cell is shown in Fig. 54.b. By keeping in mind to improve GDI logic techniques to address the voltage swing issue and meet the low-power and high-efficiency requirements of portable electronic devices. In this context, authors propose: Dynamic Transmission Gate Diffusion Input circuit (DTGDI), which is an amalgamation of Transmission Gate Diffusion Input (TGDI) and a dynamic block.

The proposed DTGDI combines Block 2 of the current DGDI with the TGDI idea. Fig. 4.2, shows the schematic of the XOR gate based on DTGDI. As can be seen, node A achieves XNOR capability, to which the transistors MT5 and MT6 contribute dynamic functionality. The problems mentioned in DGDI are resolved since node A has the entire voltage swing

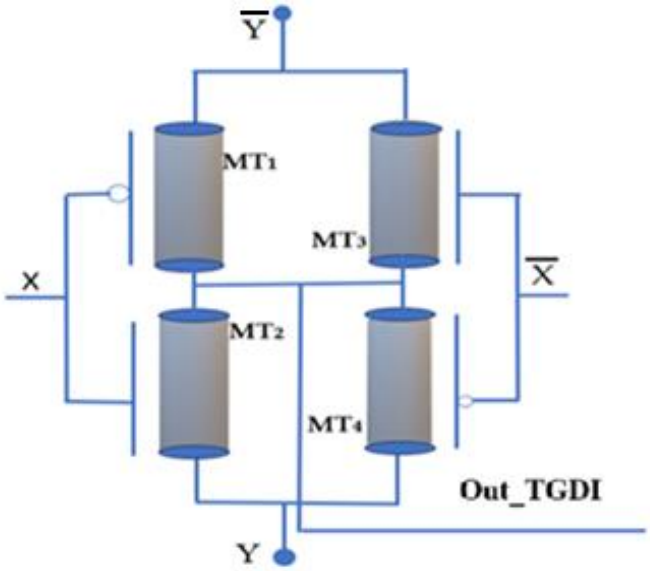


Fig. 4.1.a: Basic TGDI cell based on CNTFET .

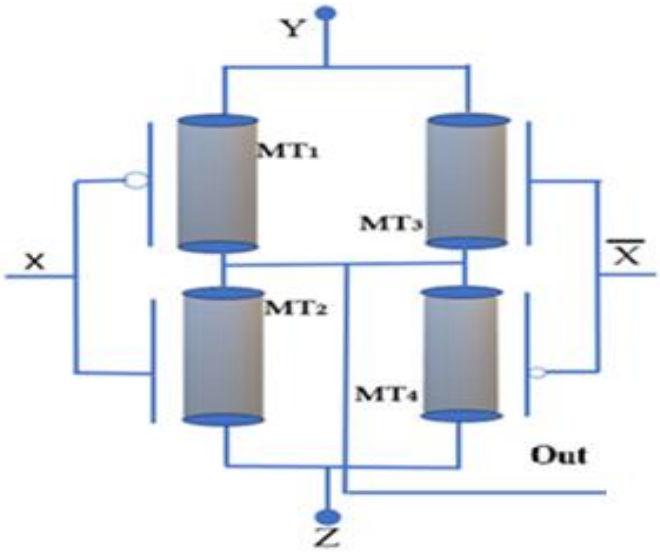


Fig. 4.1.b: XNOR configured TGDI cell

Table 4.1: Function Realizations using TGDI with various combinations of inputs

X	Y	Z	OUT	Function	Issue of full swing resolved
X	Y	'1'	X+Y	OR	✓
X	Y'	'0'	X'Y'	NOR	✓
X	'0'	Z	XZ	AND	✓
X	'1'	Y'	(XY)'	NAND	✓
X	Y	Z	X'Y+XZ	MUX	✓
X	Y	Y'	X'Y+XY'	XOR	✓
X'	Y	Y'	X'Y'+XY	XNOR	✓

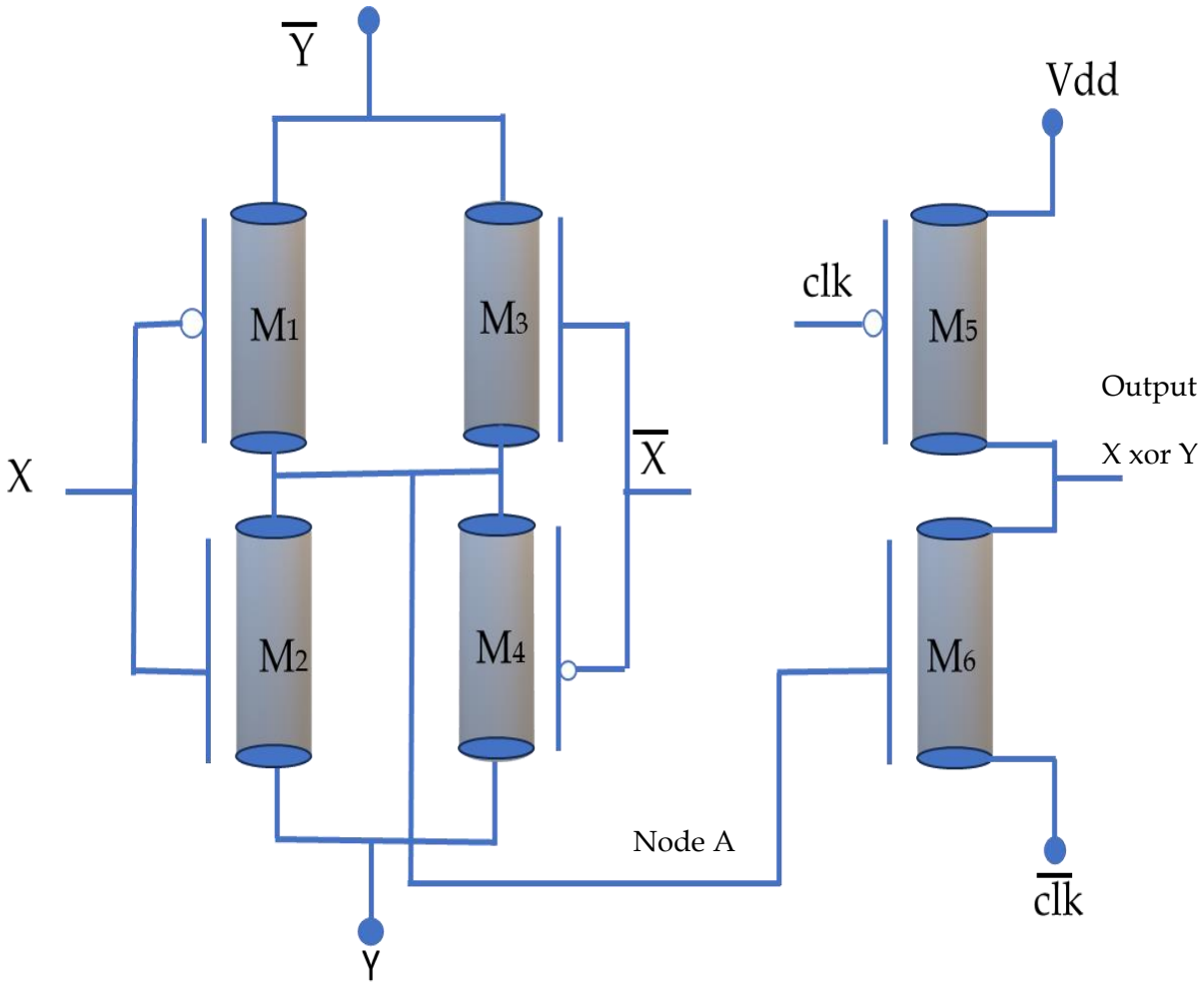


Fig. 4.2: XOR configured Proposed Dynamic Transmission gate diffusion input based on CNTFET

4.1.2 Mathematical Modelling of the DTGDI cell

A key factor in increasing the intended circuit's speed is the interconnection delay. Create effective and analytical delay models for the complex interconnection networks in this part to properly evaluate and handle this problem in the XOR-based proposed circuit DTGDI cell and the current DGDI cell [27]. The delay is computed by capturing the short time gap between the output's falling edge at 50% transition value of Vdd and the clock's rising edge at 50% of Vdd. In both DTGDI, the intermittent node attains Vdd as shown in Table 4.2. Furthermore, we solely compare τphl for analysis because both circuits are dynamic circuits. Fig. 4.3 illustrates the rise in clock signal and decay in the output of the dynamic block.

The evaluation transistor starts operating in saturation region and subsequently enters and works in linear region for output values between Vdd-Vtn to 50% of Vdd. The propagation delay is sum of time t_1, where the device is operating in saturation (Vdd to Vdd-Vtn), and t_2, where operating mode is linear (Vdd-Vtn to 50% Vdd). Assuming the resistance of evaluation transistor in saturation and linear region is R1 and R2, the propagation delay is given by sum of time intervals t_1 and t_2 is given by (5) and (6).

$$\tau_{PHL\_fullswing} = t_1 + t_2 \quad (4)$$

Using the capacitor discharge relation, t_1 and t_2 are computed as:

$$t_1 = R_1 C \ ln \frac{V_{dd}}{V_{dd} - V_{tn}} \quad (5)$$

$$t_2 = R_2 C \ ln \left(\frac{2(V_{dd} - V_{tn})}{V_{dd}} \right) \quad (6)$$

It is to be noted that the value of $R_1 >> R_2$.

To compare the $\tau_{PHL\_fullswing}$ with propagation delay of DGDI, similar calculations are done. For DGDI, the evaluation transistor starts operating in saturation region and subsequently enters and works in linear region for output values between Vdd-2Vtn to 50% of Vdd. The difference lies in the fact that gate voltage of evaluate transistor will be Vdd-Vtn and corresponding resistance of evaluation transistor in saturation (R3) and linear region (R4) will be much higher than DTGDI and DFSGDI counterparts. The propagation delay is sum of time t_3, where the device is operating in saturation (Vdd to Vdd-2Vtn), and t_4, where operating mode is linear (Vdd-2Vtn to 50% Vdd). The propagation delay for DGDI is given by

$$\tau_{PHL\_DGDI} = t_3 + t_4 \quad (7)$$

Using the capacitor discharge relation, t_3 and t_4 are computed as:

$$t_3 = R_3 C \ ln \frac{V_{dd}}{V_{dd} - 2V_{tn}} \quad (8)$$

$$t_4 = R_4 C \ ln\left(\frac{2(V_{dd}-2V_{tn})}{V_{dd}}\right) \quad (9)$$

Below shows the derivation for the equation (5), (6), (8) and (9)

$$V_{out} = V_{ini}\left(e^{-\frac{t_1}{R_1 C}}\right) \rightarrow \quad V_{dd} - 2V_{tn} = V_{dd}\left(e^{-\frac{t_1}{R_1 c}}\right) \quad \rightarrow \quad \frac{V_{dd}-2V_{tn}}{V_{dd}} = e^{-\frac{t_1}{R_1 c}}$$

$$e^{\frac{t_1}{R_1 c}} = \frac{V_{dd}}{V_{dd-2V_{tn}}} \rightarrow \quad \frac{t_1}{R_1 c} = ln\frac{V_{dd}}{V_{dd-2V_{tn}}} \quad \rightarrow \quad \boldsymbol{t_1 = R_1 C \ ln\frac{V_{dd}}{V_{dd-2V_{tn}}}}$$

$$\frac{V_{dd}}{2} = (V_{dd} - 2V_{tn})\left(e^{-\frac{t_2}{R_2 C}}\right) \rightarrow \quad \frac{V_{dd}}{2(V_{dd}-2V_{tn})} = e^{-\frac{t_2}{R_2 C}} \rightarrow \quad e^{\frac{t_2}{R_2 C}} = \frac{2(V_{dd}-2V_{tn})}{V_{dd}}$$

$$\boldsymbol{t_2 = R_2 C \ ln\left(\frac{2(V_{dd}-2V_{tn})}{V_{dd}}\right)}$$

$$\frac{V_{dd}}{2} = (V_{dd} - V_{tn})\left(e^{-\frac{t_4}{R_4 C}}\right) \quad \frac{V_{dd}}{2(V_{dd}-V_{tn})} = e^{-\frac{t_4}{R_4 C}} \quad e^{\frac{t_4}{R_4 C}} = \frac{2(V_{dd}-V_{tn})}{V_{dd}}$$

$$\boldsymbol{t_4 = R_4 C \ ln\left(\frac{2(V_{dd}-V_{tn})}{V_{dd}}\right)}$$

Upon comparing the durations of t_1 and t_3 of the DGDI and TGDI saturation regions, it can be inferred that t_3 is shorter. Since the device is operating at saturation during this time, its resistance would be larger. Thus, R_1 would be 21MΩ, and R_3 would be around 3.6KΩ. This will further increase the time period t_1. Additionally, time t_4 is longer than t_3, but the device operates in the linear zone during this time, devices resistance R_4 relative to R_3 both will be lesser. Therefore, according to the above delay model, in DGDI, a transistor with a lower driving capability is produced by a lower output swing at the dynamic block's input, which increases the delay. Proposed DTGDI will helps to addressed this issue and further enhance the performance parameter.

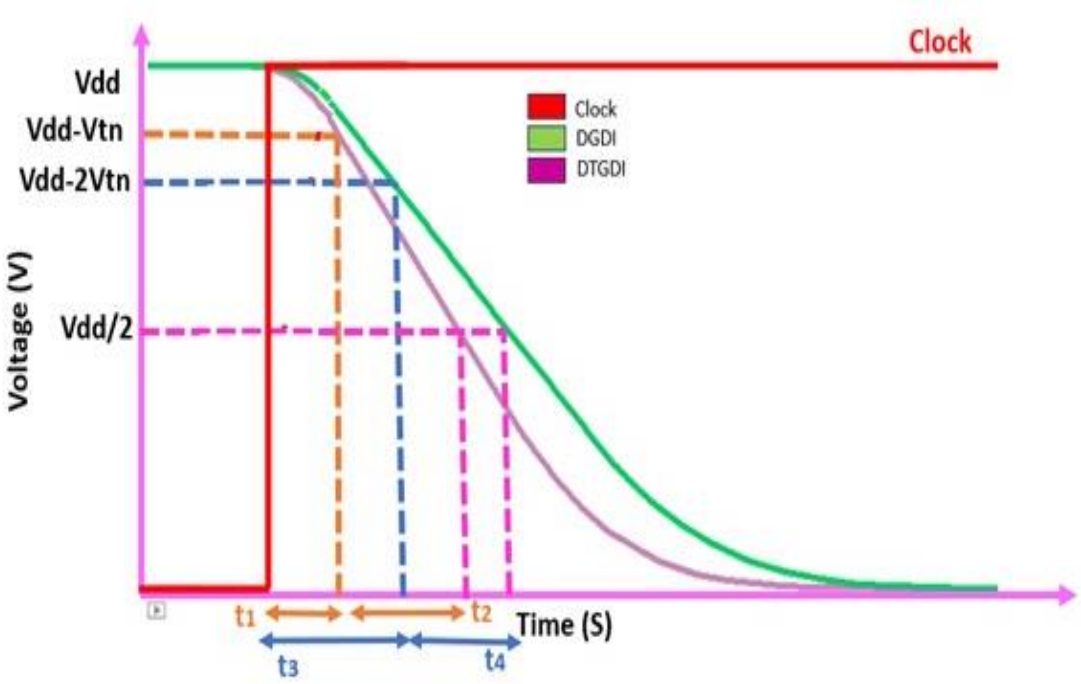


Fig. 4.3: Output response of DGDI and DTGDI with clock rise

4.2 XOR gate based on the DTGDI cell

The TGDI cell applies X and Xbar at the both the diffused gate, Y and Ybar applies at PCNTFET M_1 source and NCNTFET M_2 source respectively. This configuration to aid in the development of the XNOR gate at node A. The dynamic stage will work as an inverter; therefore, resultant output would be XOR. The XOR configure DTGDI cell is depicted in Fig. 4.2. Truth table for TGDI based cell is shown below in Table 4.2.

Table 4.2: Truth Table for DTGDI cell

A	B	Output at Node A	Output of DTGDI
0	0	Vdd	0
0	1	o	Vdd
1	0	0	Vdd
1	1	Vdd	0

53 The simulations are carried out using 32 nm technology node in Cadence Virtuoso. Fig. 4.6 show the simulated timing waveforms for XOR gate based on DTGDI. It may be observed that output is pre-charged to Vdd when clk = '0' for all the three circuits. When clk eventually becomes '1', the output remains at logic '1' when both inputs differ from each other and evaluated to '0' when both inputs are same. Thus, the circuits adhere to XOR gate functionality.

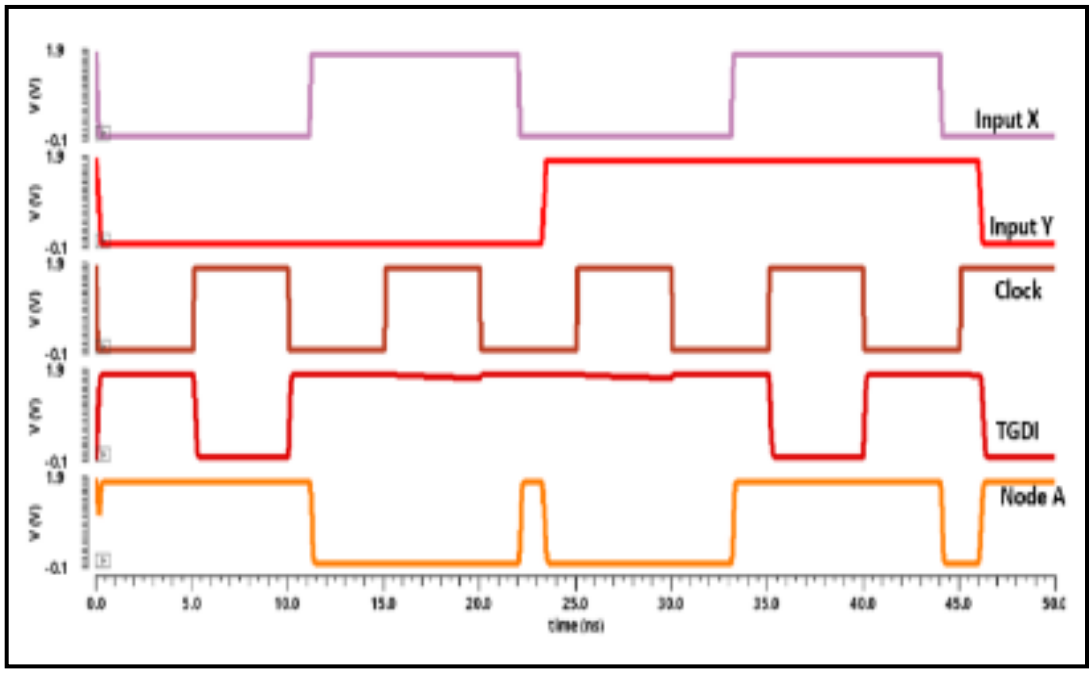


Fig. 4.4: Simulated Timing waveform of the XOR gate based on DTGDI

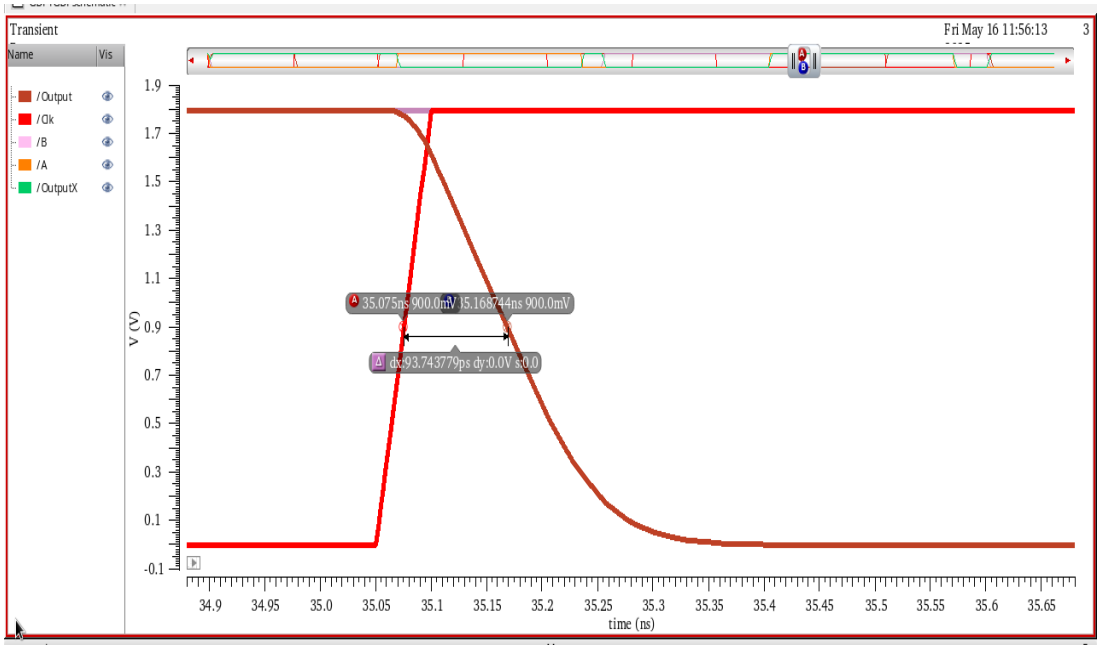


Fig. 4.5: Delay plot for XOR gate based on DTGDI

To perform this assessment, transient analysis done by taking load capacitance of 10fF and clock frequency of 100MHz. The analysis done for the case when the inputs are applied such that the logic is evaluated at node 'A' prior to clk = '1' or the circuit enters in the evaluation phase. The delay calculated, by capturing the brief interval of time between the clock's rising edge at 50% of Vdd (0.9 V) and the output's falling edge at 50% transition value of Vdd (0.9). The delay of the XOR gated based on DTGDI, is thoroughly examined. The delay is measured, when inputs XY is maintained at logic "11," clock transits from logic '0' to '1', the circuit is evaluated, the output is acquired at the output node of dynamic logic (Block-2) of the proposed circuit (I and II) and DGDI, which switches from logic '1' to logic '0'. Delay measured to be around 93.47pS and power consumption is in the range 1.54µW.

Pitch variations, changes in nanotube diameter, defects, and misalignment can all be caused by inaccurate lithography and uneven CNT growth. It alters the procedure and may have an impact on the circuit's functionality. The ±5% pitch variation is taken into consideration using a 3σ Gaussian distribution. Monte Carlo simulation was carried out for 500 samples in order to assess how process changes affected the XOR gates' latency and power consumption based on the present DTGDI. The DTGDI delay and power usage charts are displayed in Figs. 59(a) and 59(b). As may be shown, the maximum standard deviation is quite low. The existing DTGDI layouts based on XOR logic are shown in Fig. 4.7 and were created using the Electric VLSI Design System 9.07 [18]. The area for layout is found to be around 4780nm^2.

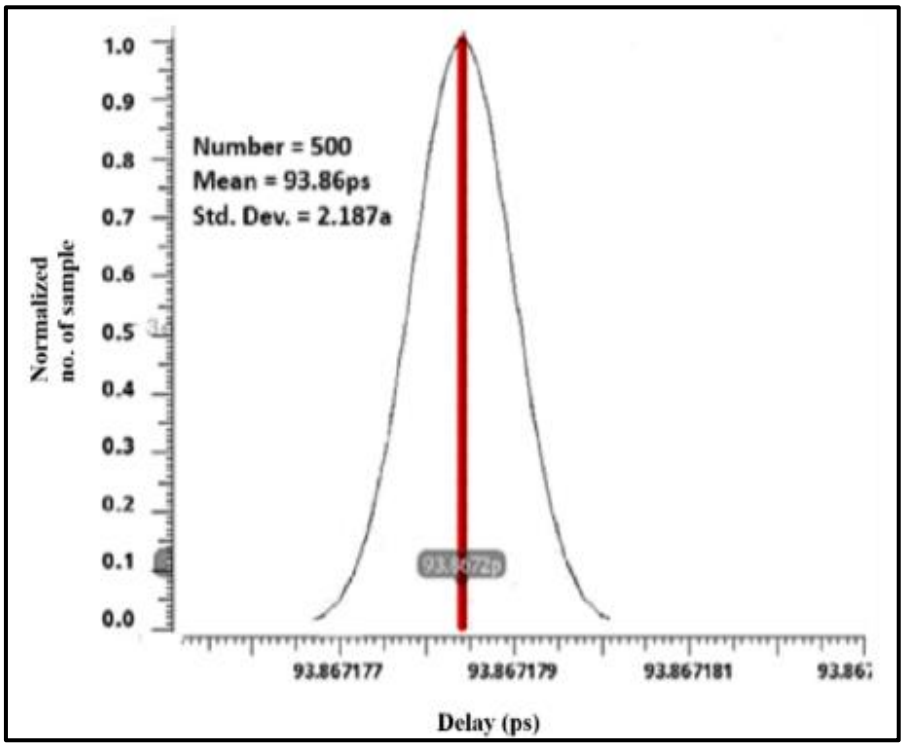


Fig. 4.6.a Monte-Carlo Simulation for delay by varying pitch 5% DGDI

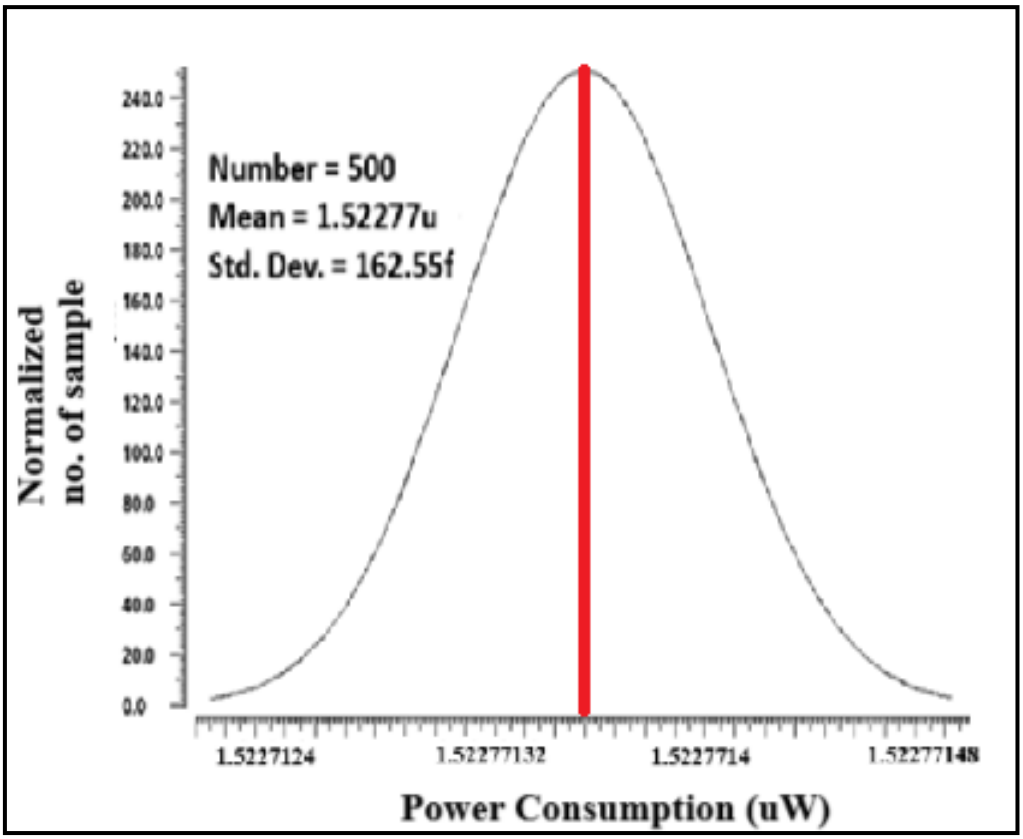


Fig. 4.6.b Monte-Carlo Simulation for power-consumptions by varying pitch 5% DGDI

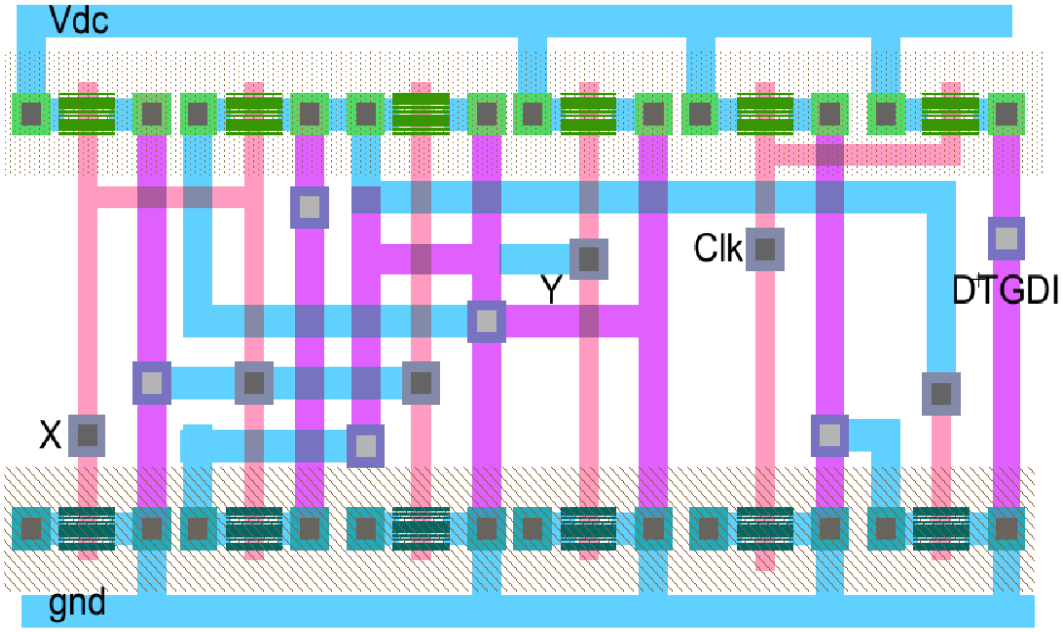


Fig. 4.7: Layout of XOR based DTGDI cell

4.3 Effect of Load Variation and supply variation

Effect of load variation for DTGDI cell (Fig. 4.8 and 4.9), where load capacitance increase from 1f F to 10f F with the step size of 1f F were also studied for this cell. As predicted, delay and power expenditure both rises with load capacitance. Since with increase in the load capacitance, circuitry will take more time in charging and discharging, and hence delay as well power consumption increase.

Also, Power supply variation can impact the circuit delay. With a reduced supply voltage lessens the gate drive strength, thereby increasing the gate delay. To do the transient analysis for the circuit with varying VDC, value of the VDC varies 10% from the typical value of 1.8V. The same has been observed and shown in the Fig. 4.10 and Fig. 4.11.

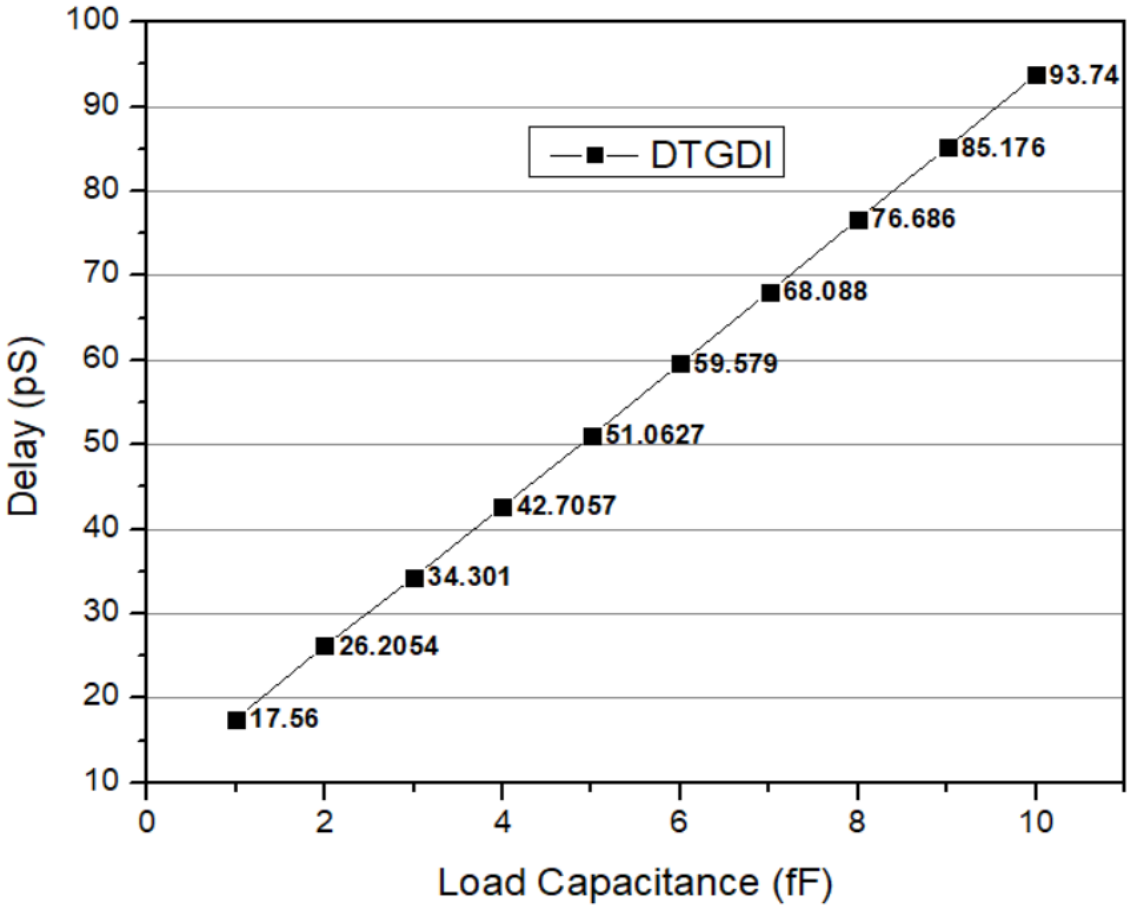


Fig. 4.8: Effect of the load variation on the delay

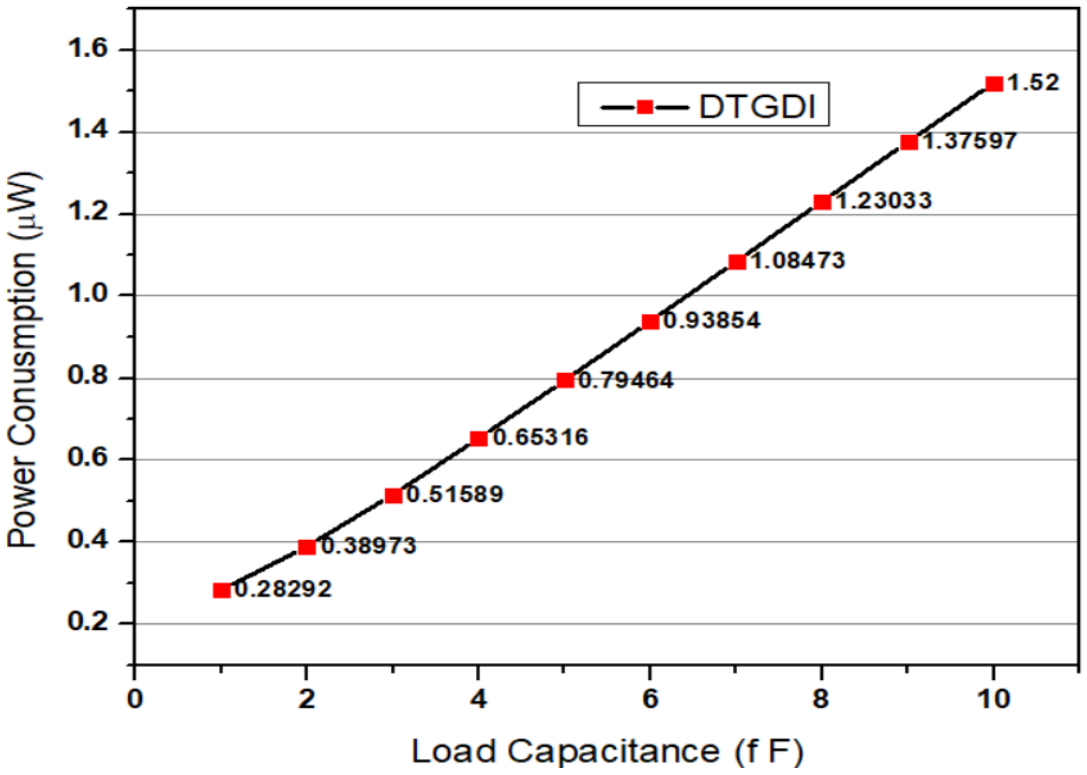


Fig. 4.9: Effect of the load variation on the power consumption

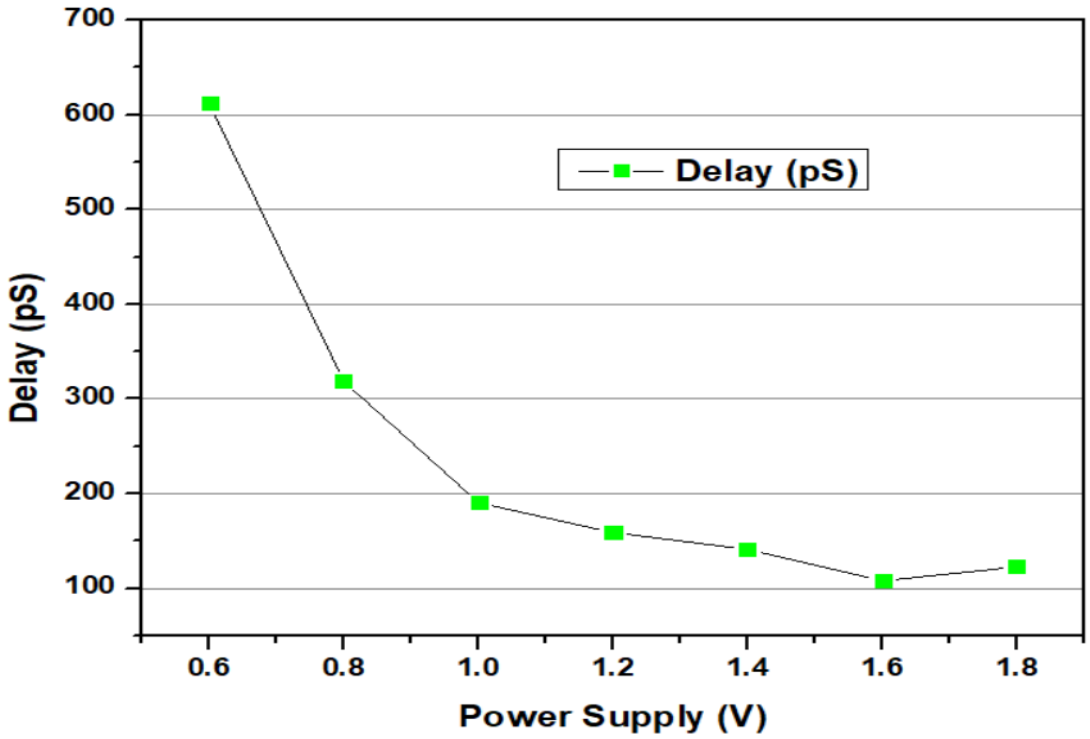


Fig. 4.10 Effect of the change in the supply voltage on the delay

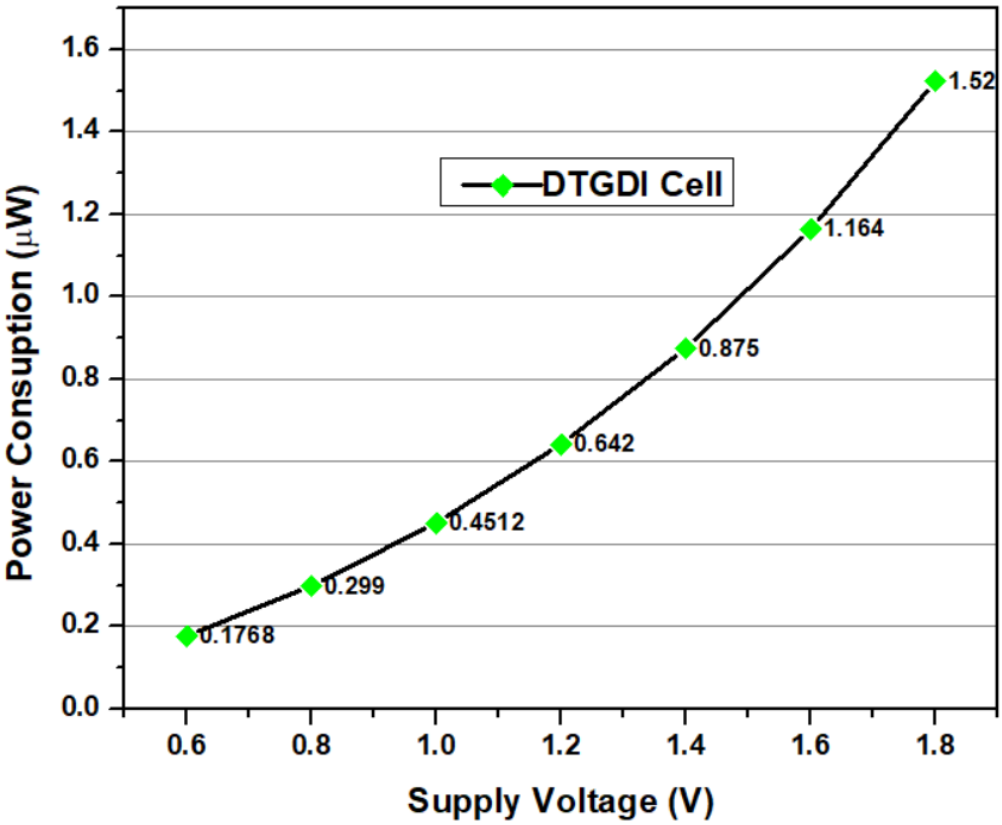


Fig. 4.11 Effect of the change in the supply voltage on the power consumption

4.4 Full adder using the DTGDI logic

The full adder's design architecture is based on the DTGDI, which optimizes the PDP, latency, and power consumption factors. The following simplified equations serve as the foundation for the implementation of the full adder circuit in the suggested design [15]:

$$Sum = X \oplus Y \oplus Z$$

$$COUT = Z(X \odot Z) + X(Y \oplus Z)$$

$$SUM = X(Y \odot Z) + X(Y \oplus Z)$$

Taking into account the aforementioned formulae, the "Y⊕Z" components that are included in both the SUM and COUT outputs result in less transistors. Fig. 4.12 displays the circuitry of the complete adder based on the DTGDI cell.

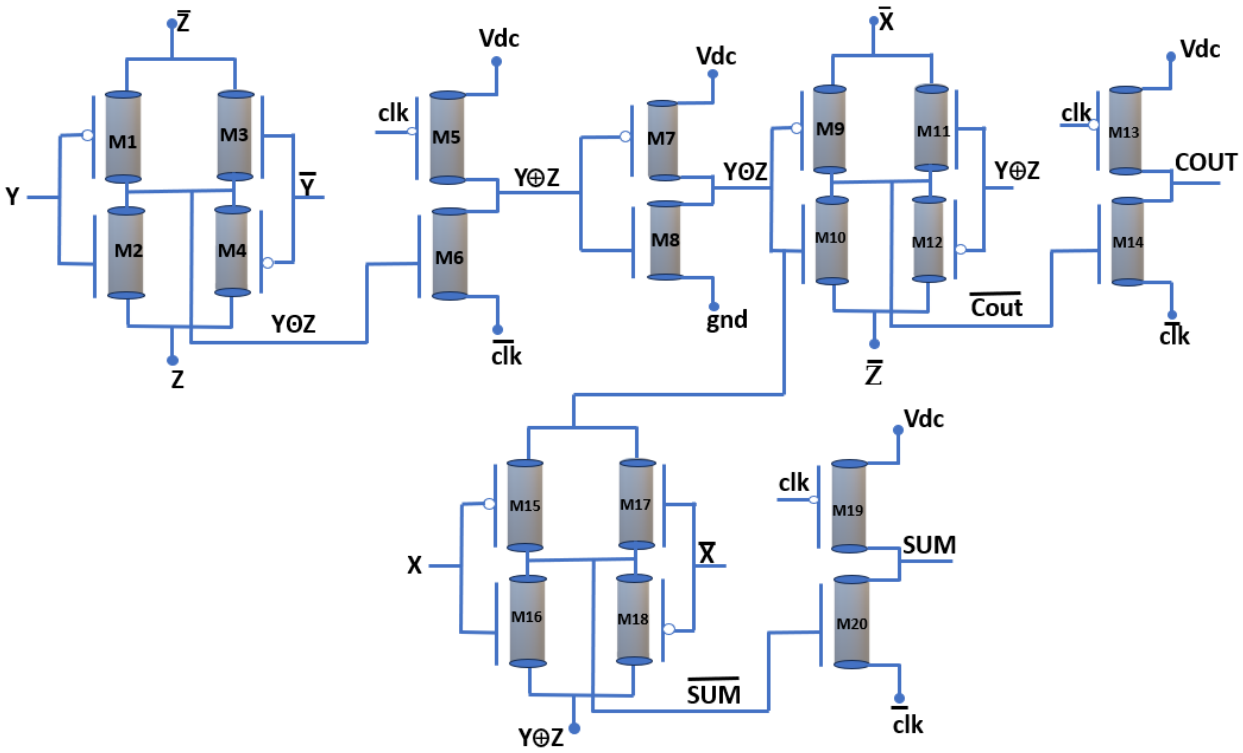


Fig. 4.12 Schematic for DTGDI based full adder

A TGDI cell, which is made up of the transistors M1, M2, M3, and M4, is responsible of producing the XNOR logic. The dynamic block then flips the logic such that XOR functionality may be derived. Efficient logic processing is ensured by applying the XOR logic of inputs Y and Z to the gate terminals of transistors M9 and M10 and feeding the XNOR logic to the gate terminals of transistors M11 and M12 in order to compute the carry output bar. The carry signal will ultimately be obtained by applying this input to the dynamic block once again.

Sum bar logic will be obtained by generating XOR Y and Z with signal X from the transistor M15, M16, M17 and M18. The Sum signal then can be obtained by applying the Sum bar as an input to the dynamic logic block.

Analysis was done on the full adder's SUM and Carry output. Because the circuit uses dynamic logic, the output is pre-charged while the clock is at logic 0, hence the SUM and carry output has logic 1 as its output. Depending on the adder's input, SUM and carry logic can be implemented whenever the clock reaches logic 0. The sum and carry function display the logic 0 when both inputs are 0. One input transiting to 1 causes the SUM output to travel to logic 1 while the carry remains at logic 0, the prior logic. Carry displays logic 1 as the output while SUM displays logic 0 when both inputs are high.

To obtained the SUM and Carry output as shown in Fig. 4.13, Signal A, B and Cin has a period set at value of 80ns, 40ns and 20ns respectively. Clock signal has a period of 10ns. All input has a duty cycle of 50% and pulse width of 0.8 V. As can be seen in the figure, all the logic based on input combination has been verified. Fig. 4.14 shows the delay curve, with a delay value of 23.11 pS. Fig, 4.15 shows the power consumption by full adder based on DTGDI cell.

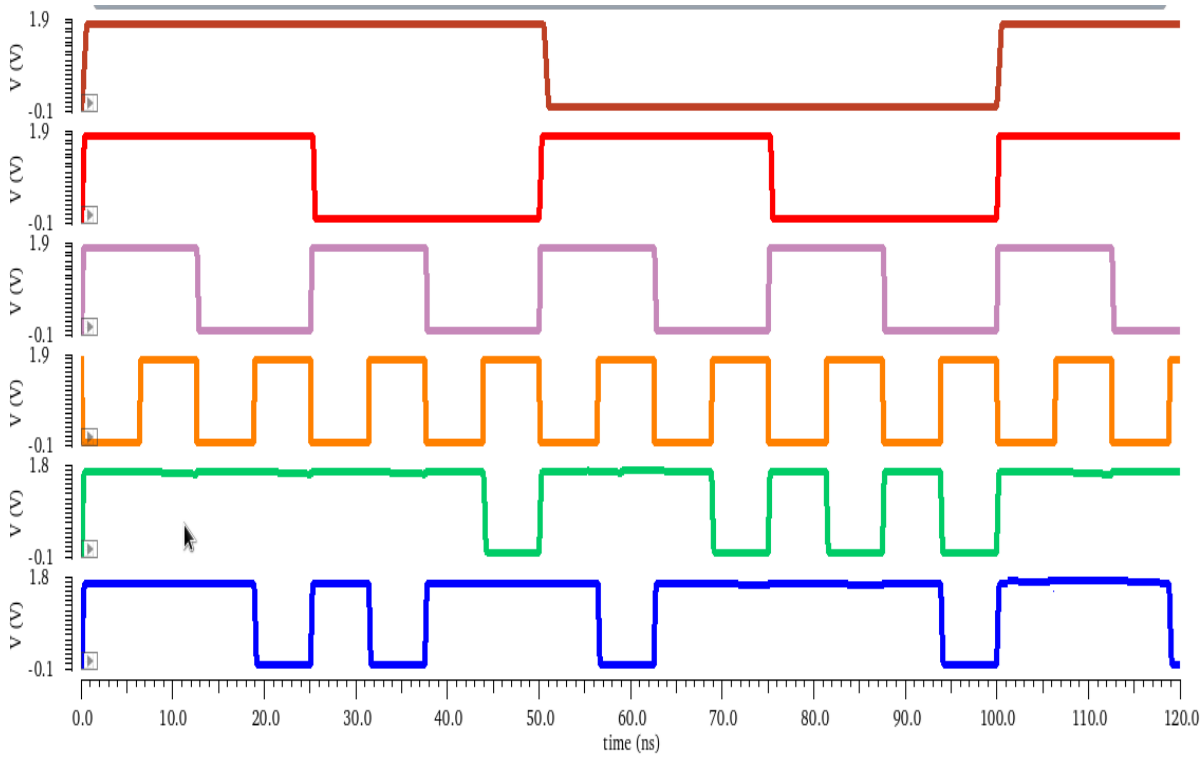


Fig. 4.13: Transient response of the full adder based on DTGDI cell

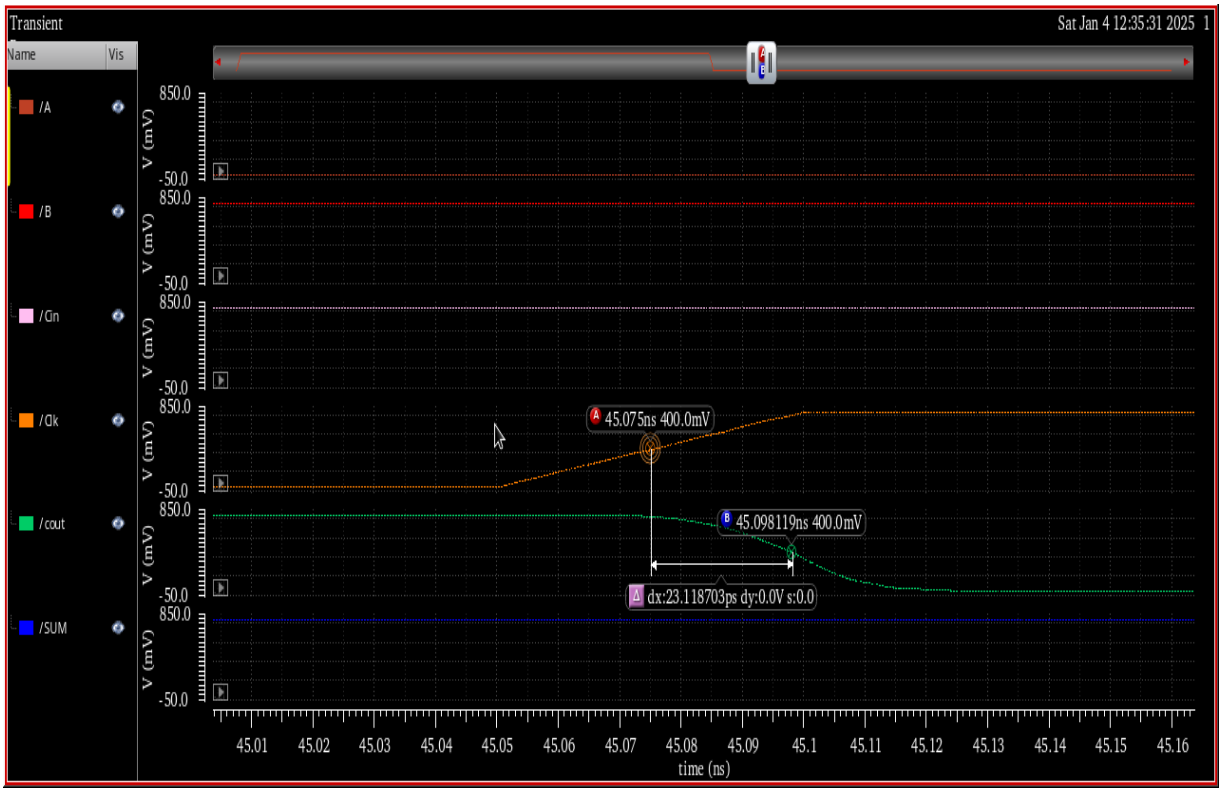


Fig. 4.14: Delay plot for the full adder based on the DTGDI cell

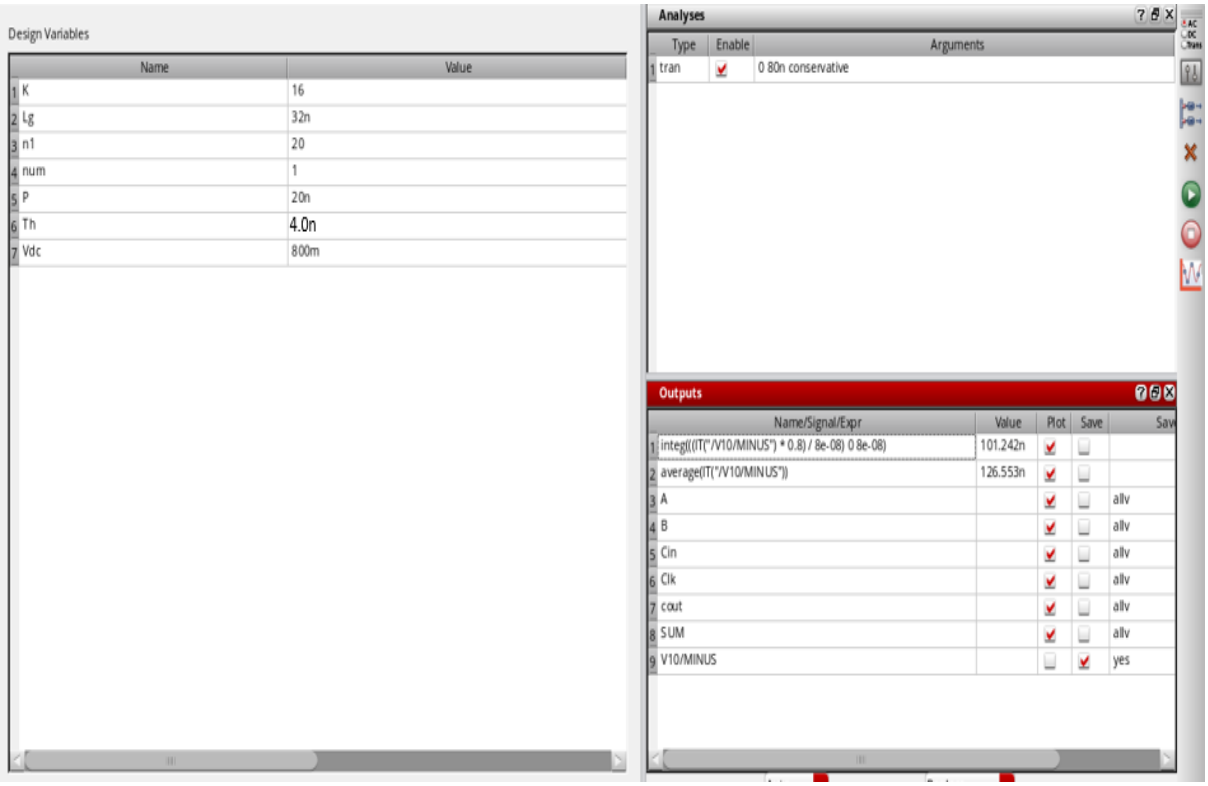


Fig. 4.15: Power-consumption for the full adder based on DTGDI cell

Additionally, a power supply experiment was conducted on the full adder; Figs. 4.16, 4.17 and 4.18 show the plots of this experiment. When the power supply is changed, performance metrics that delay consumption and PDP are noted. Because a rise in voltage causes power consumption to rise and delay to decrease. Examine the supply voltage's optimal value with this experiment.

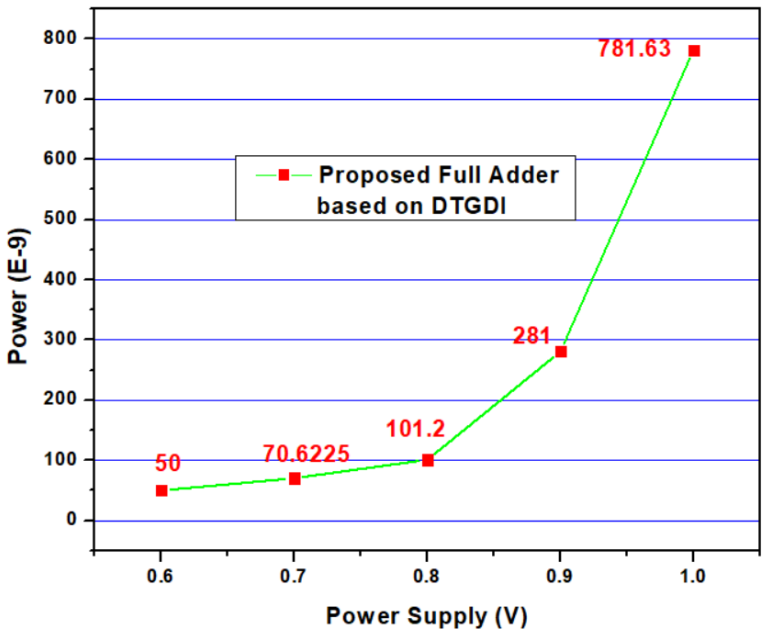


Fig. 4.16: Power consumption variation with change in supply voltage in full adder

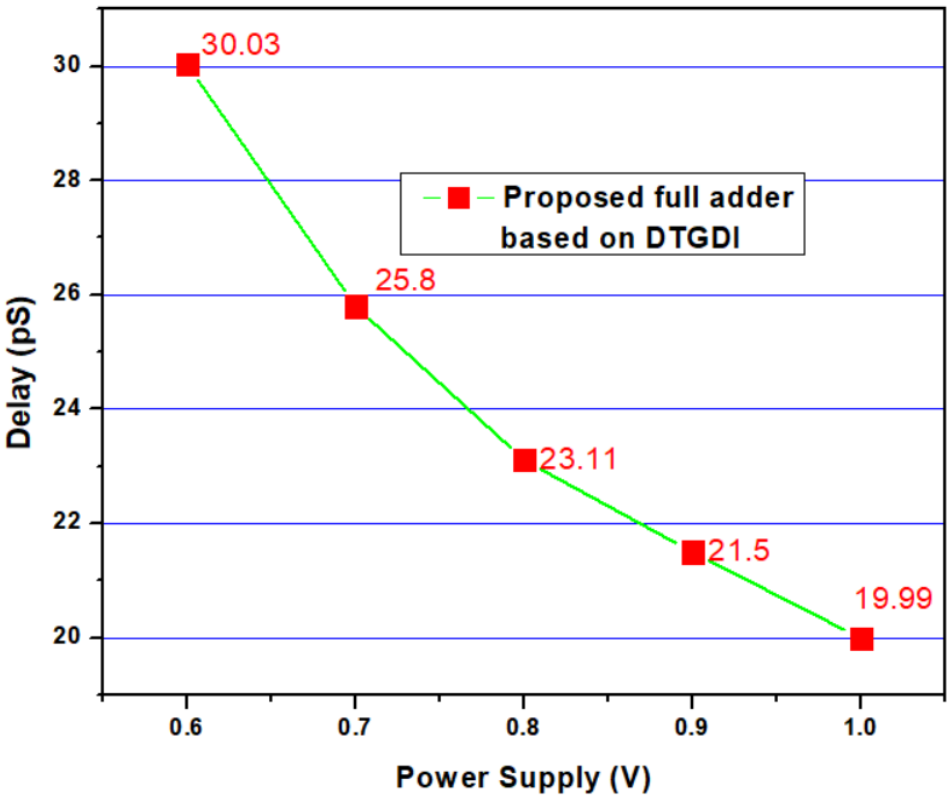


Fig. 4.17: Delay variation with change in supply voltage in full adder

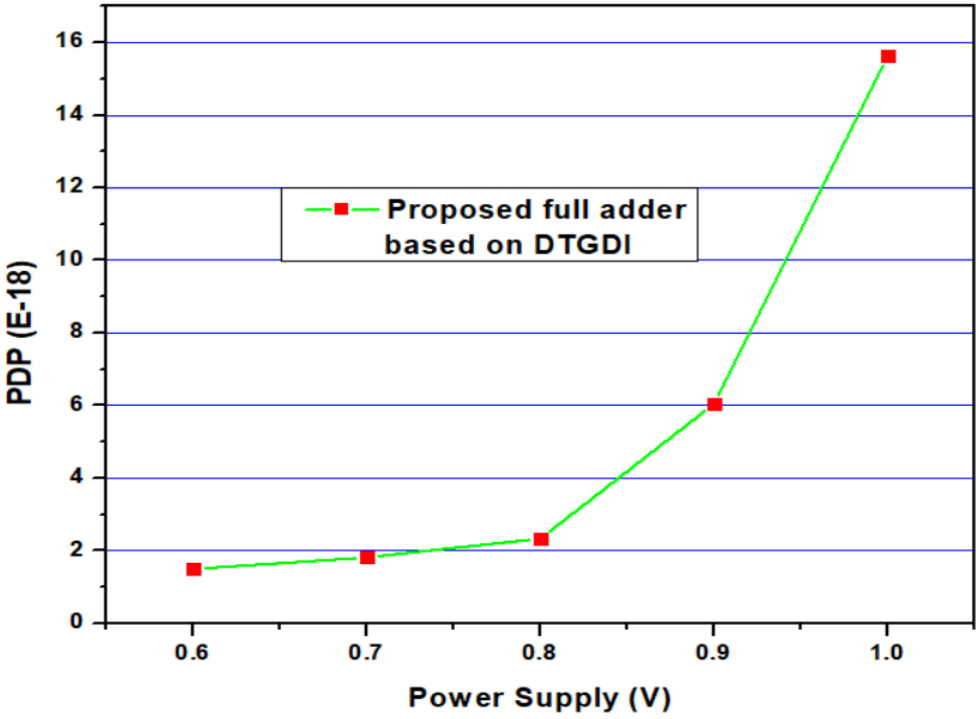


Fig. 4.18: PDP variation with change in full adder

4.5 Ripple carry adder based on DTGDI

Ripple carry adder based on the dynamic gate diffusion input also developed as per the architecture of the RCA as shown in Fig. 2.22. The transient response of the RCA based on DGDI is shown in the Fig. 4.19. Its implemented by connection 4 full adder in a serial manner. Delay to generate the SUM by last full adder measured to be around 88pS as shown in Fig. 4.20. The power consumption would be around 0.377µW.

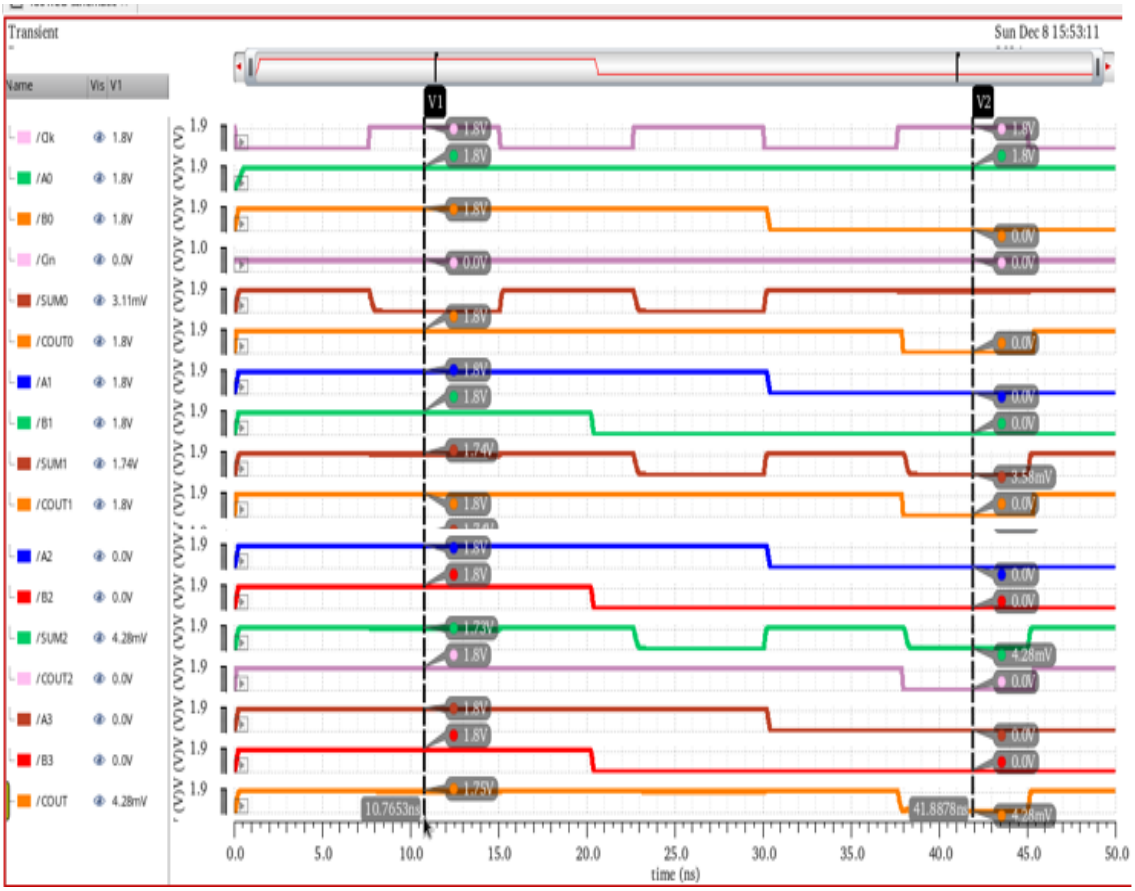


Fig. 4.19: Transient Response of the 4-bit RCA based on DTGDI cell

4.6 Multiplier based on the DTGDI Cell

To further studied the DTGDI cell in detail, 2x2 multiplier circuitry also designed. The schematic for the same is shown in the Fig.4.21. Circuitry developed as per the block diagram shown in Fig. 2.26. The simulated waveforms for each input and output are shown in Fig. 4.22, and the delay graphs for the 2x2 multiplier are shown in Fig. 4.23. Additionally, a delay of about 61.4 ps was measured to obtain the MSB of the multiplier output. Approximately 0.49 µW of electricity is used by the same circuit.

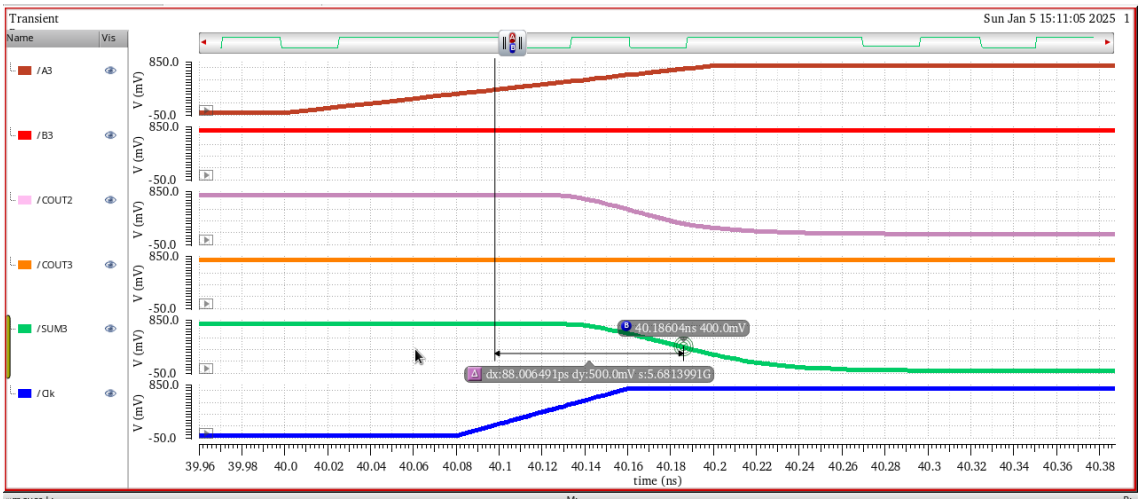


Fig. 4.20: Delay Plot for RCA based on DTGDI cell

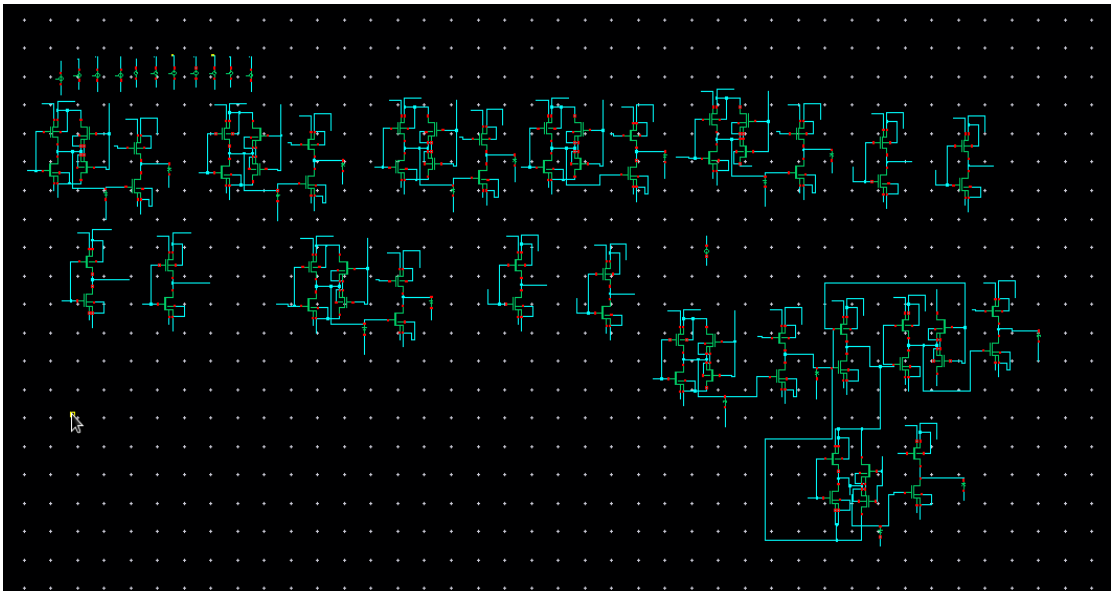


Fig. 4.21 Schematic of 2x2 multiplier

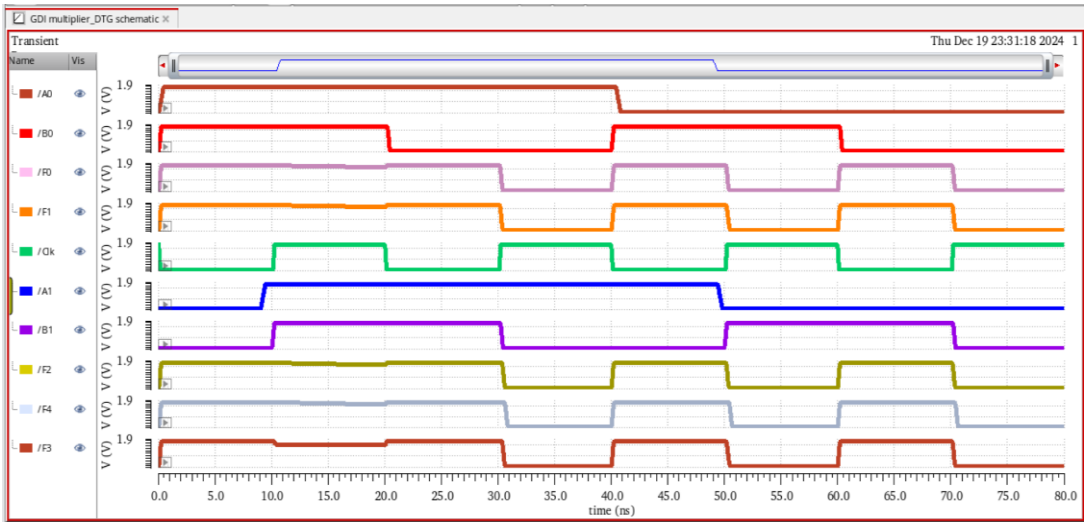


Fig. 4.22: Transient Response of the 2x2 multiplier based on the DTGDI cell

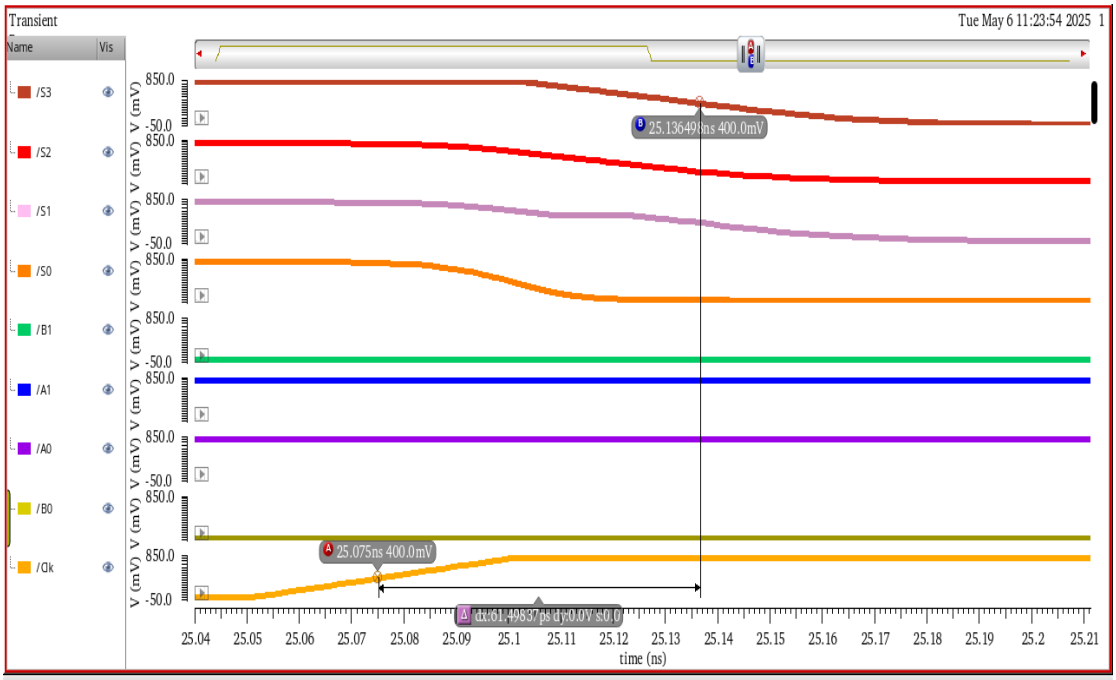


Fig. 4.23: Delay Plot for multiplier based on DTGDI

4.7 Summary

This chapter studied DTGDI cells, which implement the XOR or XNOR logic by merging the Transmission Gate Diffusion Input (TGDI) and Dynamic logic block (DLB). This cell is also configurable, means by changing the input value, different logics can be realized, same seen in section 4.1.

The XOR logic was studied using the DTGDI cell, a fundamental part of complex circuitry. Afterwards, a full adder, RCA, and 2x2 multiplier were subsequently built using this cell. An overview of the characteristics is given in Table 4.3. All of the circuitry is constructed utilizing DTGDI-based performance requirements, including PDP, power consumption, and latency. The results showed that the present DGDI cells were not as effective as the DMGDI-based combination circuits.

Table 4.3: Different Circuitry based on DTGDI Cell

Logic Gate	Delay (pS)	Power Consumptions (μW)	PDP (E-18)
XOR Gate (1.8V)	93.7	1.52	142.424
Full Adder (0.8)	23.11	0.102	2.35
RCA (0.8)	88	0.377	33.176
Multiplier (0.8)	61.4	0.49	30.086

Chapter 5: Implementation of Dynamic Modified Gate Diffusion Input based (three terminal) Circuit

5.1 The MGDI cell

A GDI cell's basic configuration consists of nMOS and pMOS transistors with four terminals: the pMOS transistor's outer diffusion node (P), the nMOS transistor's outer diffusion node (N), the shared gate input (G), and the common diffusion node (D). This research compared customized GDI logic gates with conventional GDI and CMOS logic after they were constructed using 32nm technology. Basic modified GDI gates, including AND, OR, NOR, NAND, XOR, XNOR, and MUX, are constructed as shown in Fig. 5.1 [16]. For example, the AND gate has the source of the nMOS linked to input 'B.' and the drain of the pMOS transistor connected to input A. 'A.' is connected to gate terminal G.. While nMOS is switched off, pMOS will function linearly when both inputs are zero. PMOS is in cutoff and NMOS is in linear when A = '1' and B = '0'. In the same way, if A='0' and B='1', the result will be 1 [28].

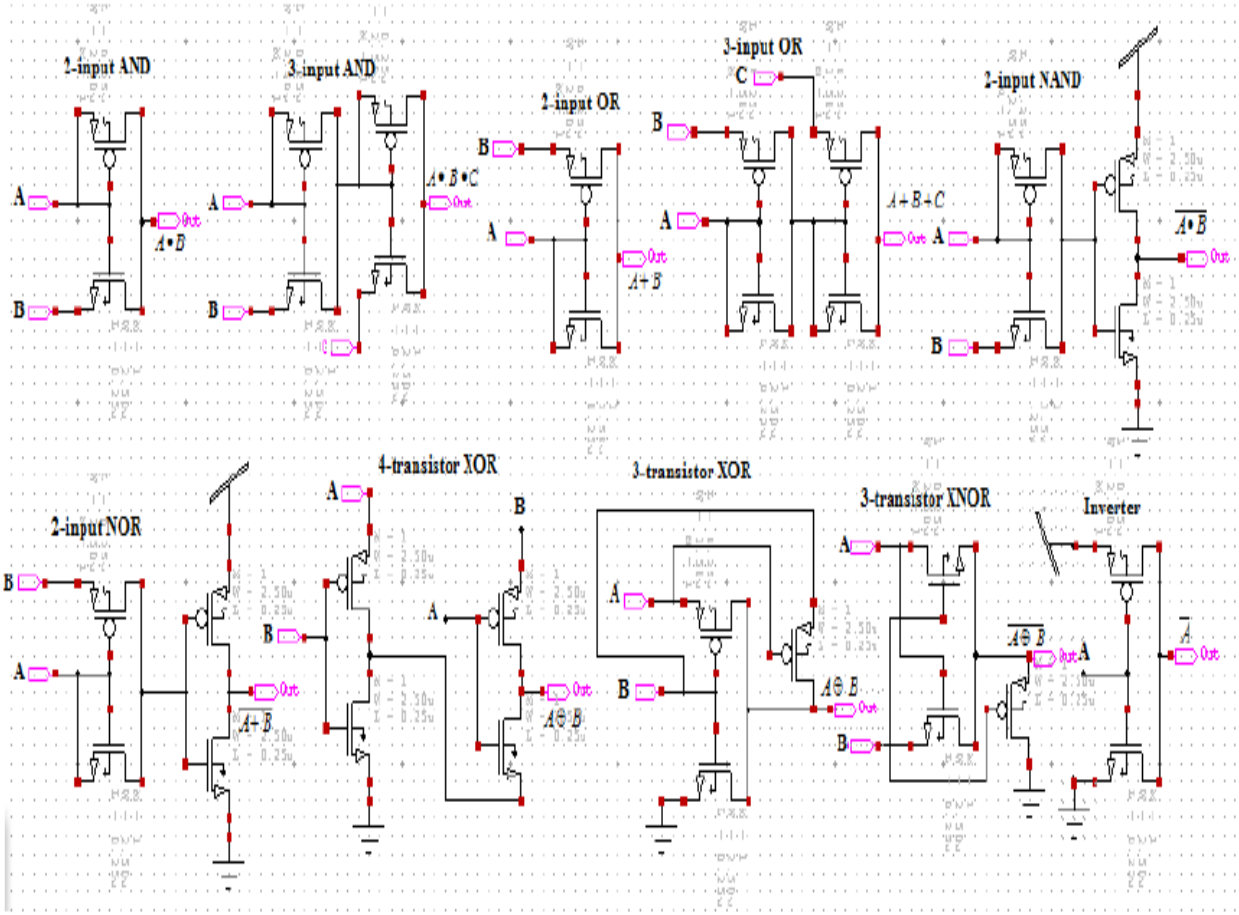


Fig. 5.1 [28]: Modified Primitive GDI Logic gates

5.2 XOR logic based on DMGDI

MGDI, it can be realized to get an XOR logic with only three transistors. The swing issue remains the same as that in GDI. The XOR logic implementation from MGDI is depicted in Fig. 5.2. For the logic input 'XY' set at '00', transistors MT1 and MT3 turn ON, and MT2 turns off. Since PCNTFET passed weak '0' or |Vtp|. Likewise, for the input '01', MT1 turns OFF, MT2 and MTF3 turn ON, and the obtained ratioed output. For the other two combinations, '10' and '11', the output is strong '1' and strong '0' respectively; the same is summarized in Table 5.1. The dynamic logic utilizes with the concept of pre-charging and evaluation by employing a clock signal. The pre-charged phase is the mode of operation in which the output node is temporarily charged to the Vdd when the clock (clk) = '0'. Additionally, it enters the evaluation phase at clock (clk) = '1', where input combinations determine the intended output. of two transitor MD4 and MD5, it works as an inverter and helps to obtained the full swing.

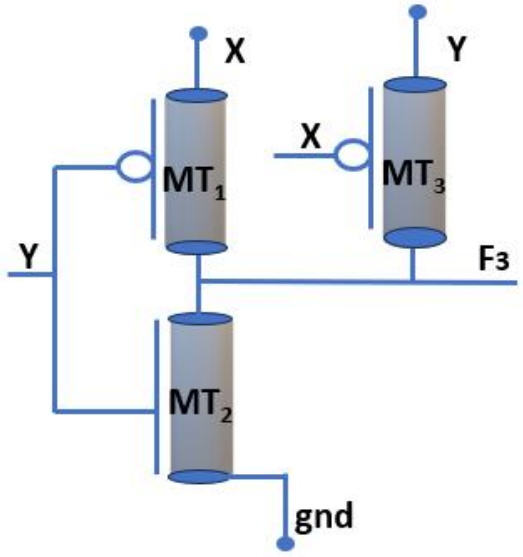


Fig. 5.2 MGDI cell

Table 5.1: Functionality of XOR gate for MGDI cell

X	Y	Transistor State of the Devices			Output
		MT1	MT2	MT3	
0	0	ON	OFF	ON	|Vtp|
0	1	OFF	ON	ON	Ratioed
1	0	ON	OFF	OFF	Strong Logic '1'
1	1	OFF	ON	OFF	Strong Logic '0'

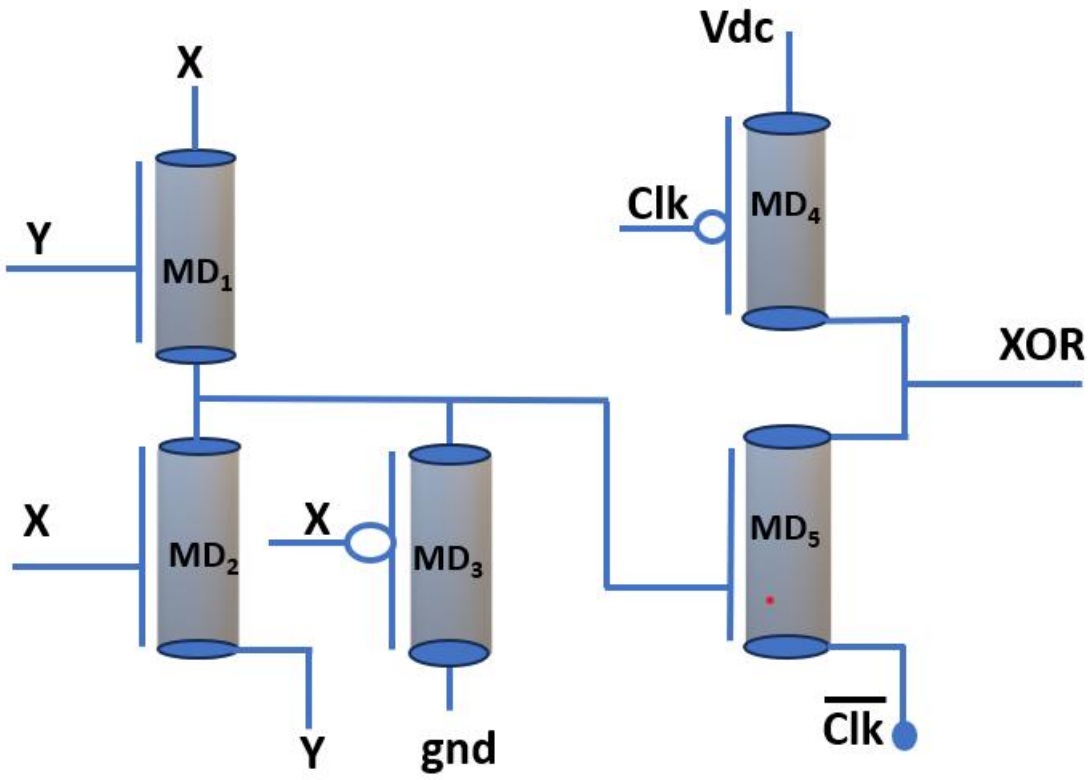


Fig. 5.3 XOR logic gate based on DMGDI Cell

5.3 Effect of varying load capacitance and supply voltage

Effect of load variation for DGDI cell (Fig. 5.4 and Fig. 5.5), where load capacitance increase from 1f F to 10f F with the step size of 1f F were also studied for this cell. As predicted, delay and power expenditure both rises with load capacitance. Since with increase in the load capacitance, circuitry will take more time in charging and discharging, and hence delay as well power consumption increase.

The transient analysis for the circuit with varying VDC also performed by varying the value of the VDC varies 10% from the typical value of 0.8V. Power supply variation can impact the circuit delay. With a reduced supply voltage lessens the gate drive strength, thereby increasing the gate delay. The same has been observed and shown in the Fig. 5.6. At the same time, with increase in power supply leads to increase in power-consumption, same depicted in Fig. 5.7.

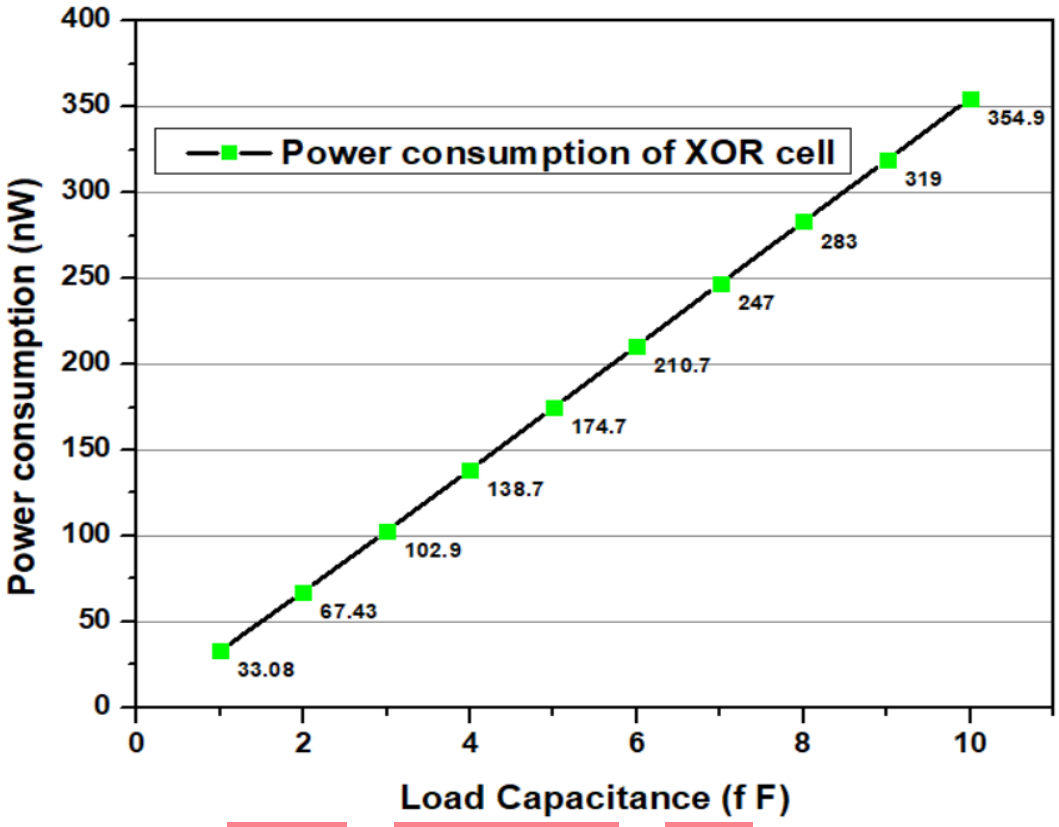


Fig. 5.4: Effect of the load variation on the power consumptions

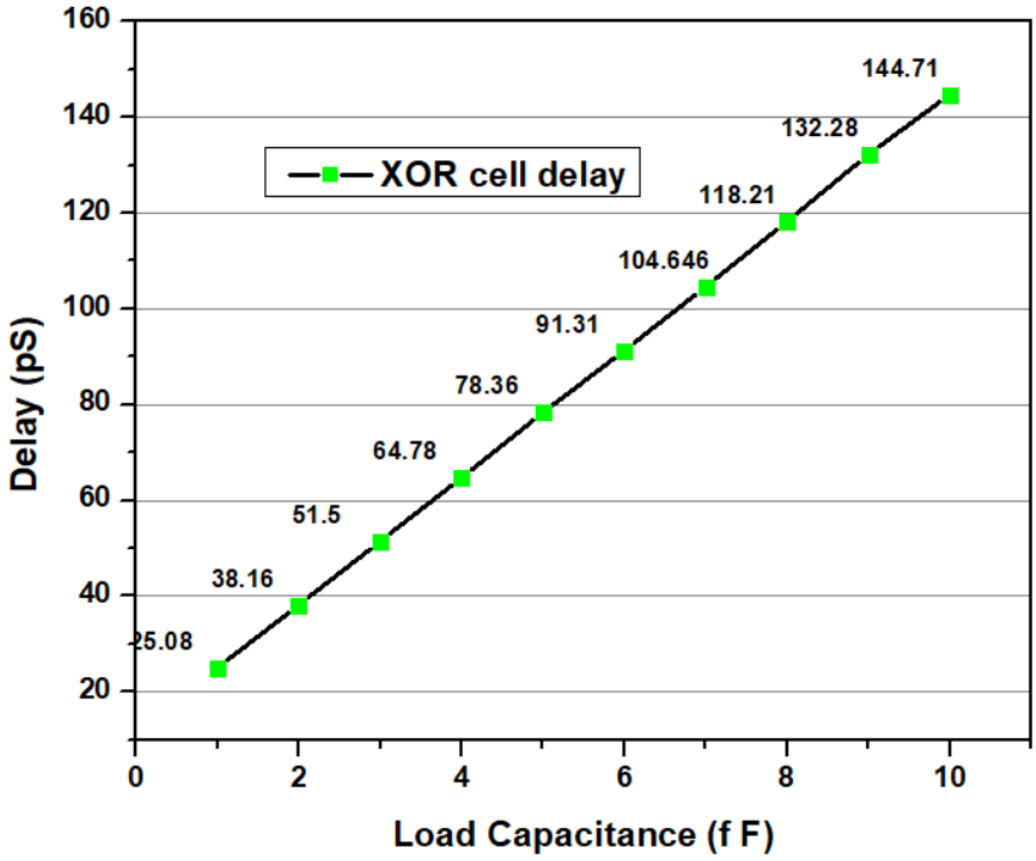


Fig. 5.5: Effect of the load variation on the delay

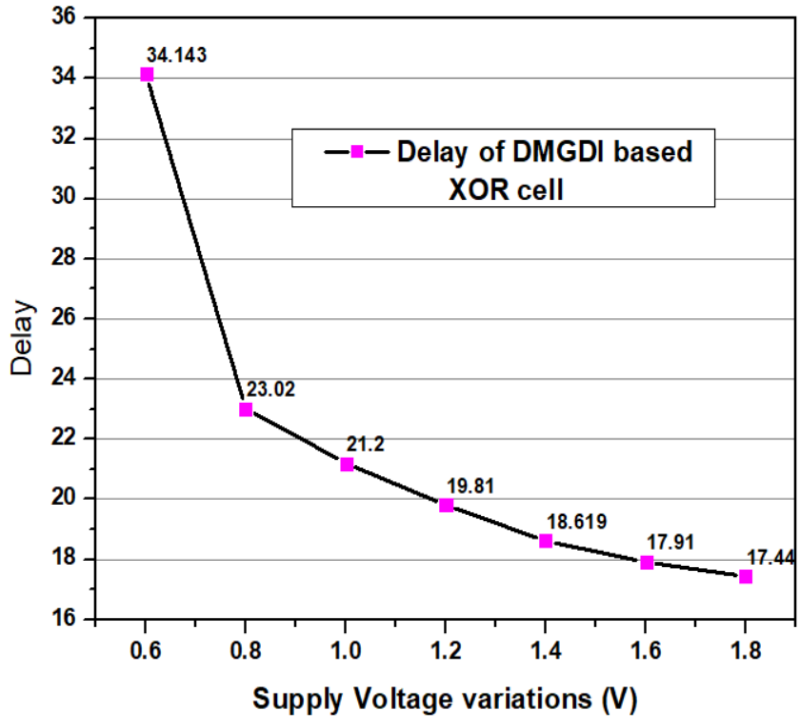


Fig. 5.6: Effect of the supply voltage variation on the delay

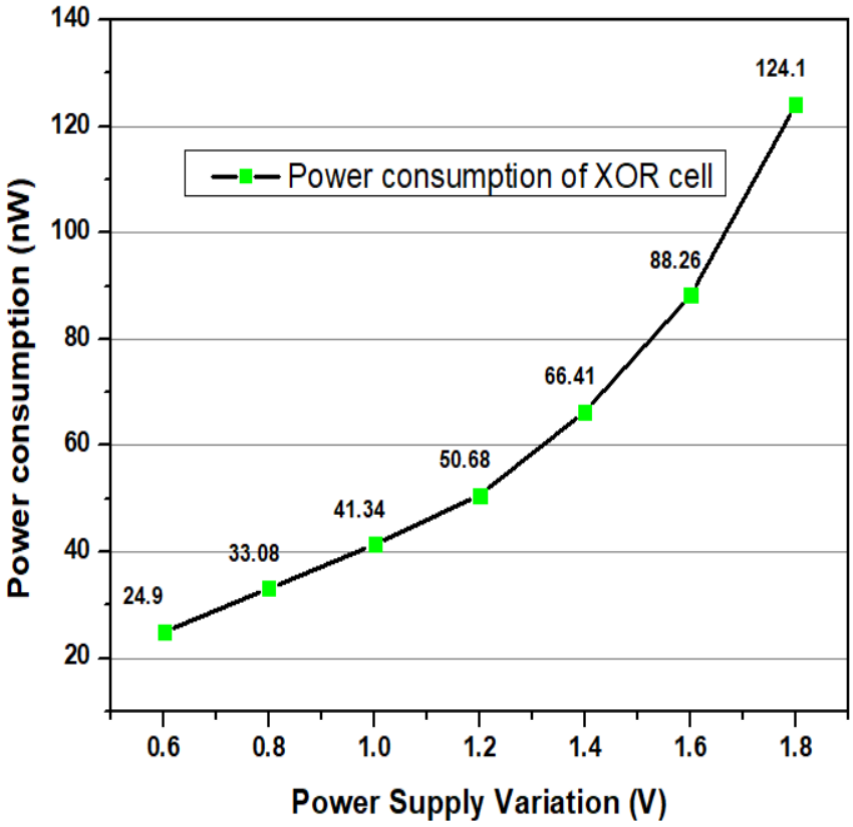


Fig. 5.7: Effect of the supply voltage variation on the power consumption

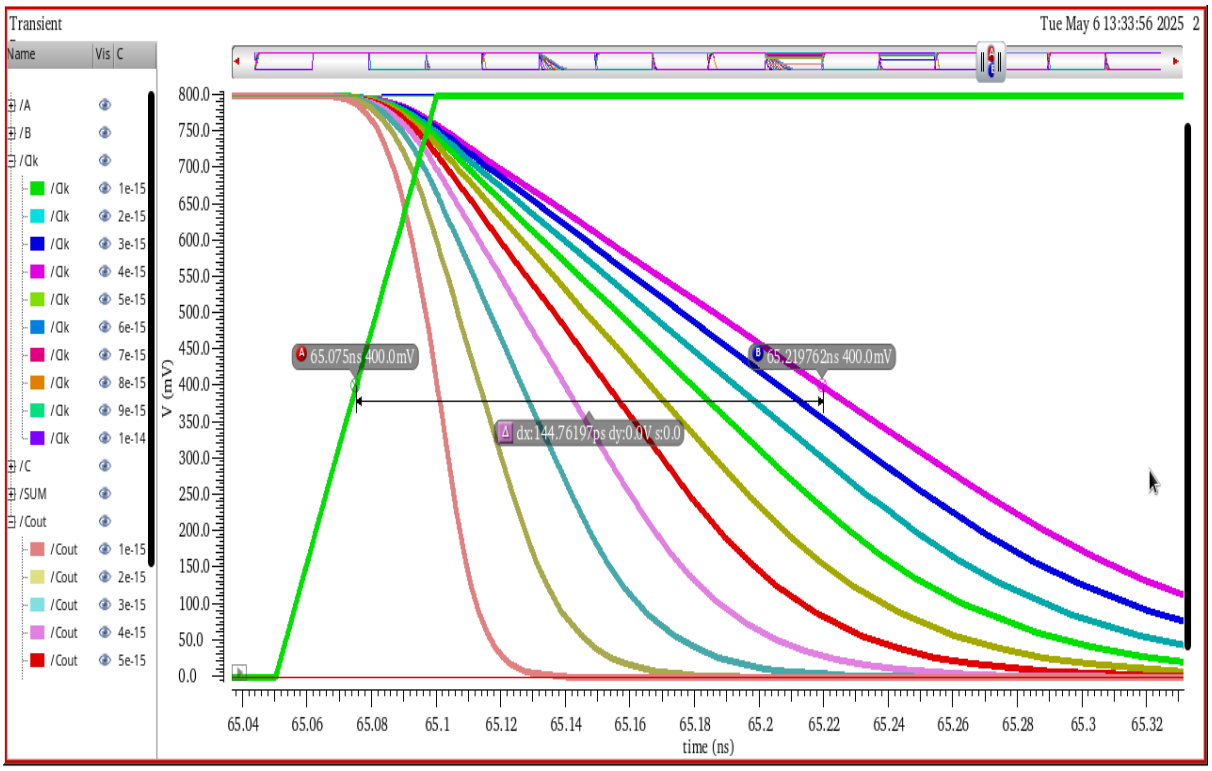


Fig. 5.8 Transient response showing delay varies with load capacitance

5.4 Full adder based on the DMGDI

In a microprocessor, an arithmetic unit requires a full adder, it is a digital circuit used to add three binary number. It generates two outputs, sum and output carry (cout), from three inputs, X, Y and Z. The logics for the SUM bar and Carry bar [19] is summarized in the equation 3 and 4.

$$\overline{SUM} = \overline{XYZ} + \bar{X}YZ + XY\bar{Z} + X\bar{Y}Z = \bar{Z}\,(YX + \overline{YX}) + Z\,(\bar{Y}X + Y\,\overline{X}) \quad (3)$$

$$\overline{COUT} = \overline{XYZ} + \bar{X}Y\bar{Z} + X\overline{YZ} + \overline{XY}Z = (\bar{Z})\,(\overline{XY} + XY) + \bar{X}(\bar{Y}X + Y\bar{X}) \quad (4)$$

In Fig. 5.9, the schematic of a 1-bit full adder is displayed. M_1, M_2, and M_3 give the XOR logic for inputs X and Y; the DLB then receives the XNOR logic for X and Y (M_4 and M_5). Furthermore, the XOR of XΘY with Z will be produced by the M_6, M_7, and M_8. Additionally, DLB (M_9 and M_{10}) generates SUM. Cout gets generated by providing the XΘY as a control signal to the GDI MUX block, with input of Z to PCNTFET of M_{11} and X to PCNTFET of M_{12}. The inverter and DLB are linked in series to obtain COUT in order to achieve a full swing.

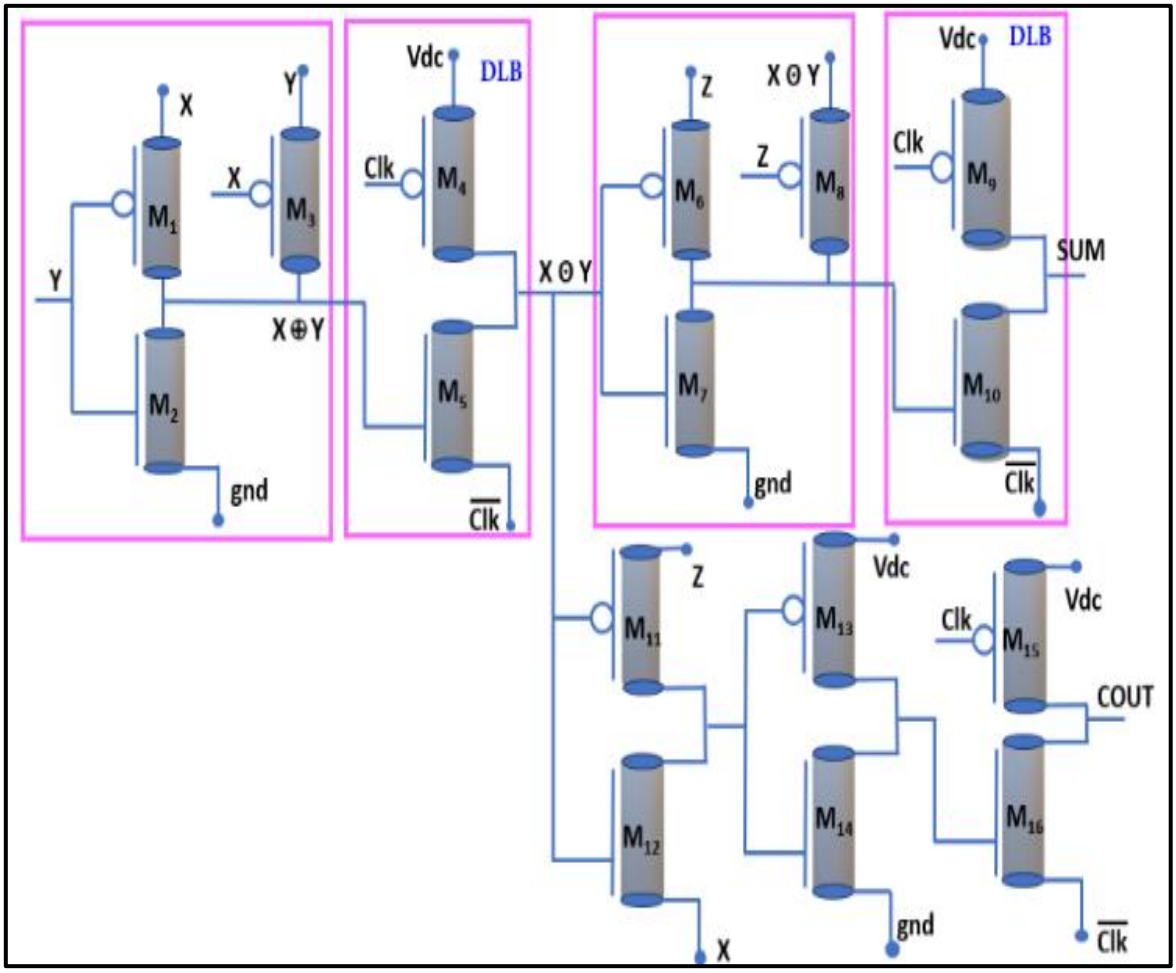


Fig. 5.9: Schematic of the full adder (1-bit) as per Dynamic Modified Gate Diffusion Input (DMGDI)

Transient analysis is performed using a 100 MHz clock frequency and 1 fF load capacitance with 0.8 V Vdc. The inputs X, Y, and Z were set at frequencies of 12.5MHz, 25MHz, and 50MHz, respectively. To take into consideration every transition in accordance with the truth table, transient analysis was carried out at 80 nm. It may be observed that output is pre-charged to Vdd when clk = '0'. When clk eventually becomes '1', the SUM is at logic '0' when two inputs out of three are at logic '1', and evaluated to '1' when one input out of three is set at '1'. Similarly, the COUT is at logic '1' when two inputs out of three are at logic '1', and evaluated to '0' when one input out of three is set at '1'. When all inputs 'XYZ' are set to '000', COUT and SUM will be obtained as '000' respectively. Thus, all the logic of SUM and COUT is realized successfully. Fig. 5.10 shows a full adder simulated timing waveforms based on the proposed design.

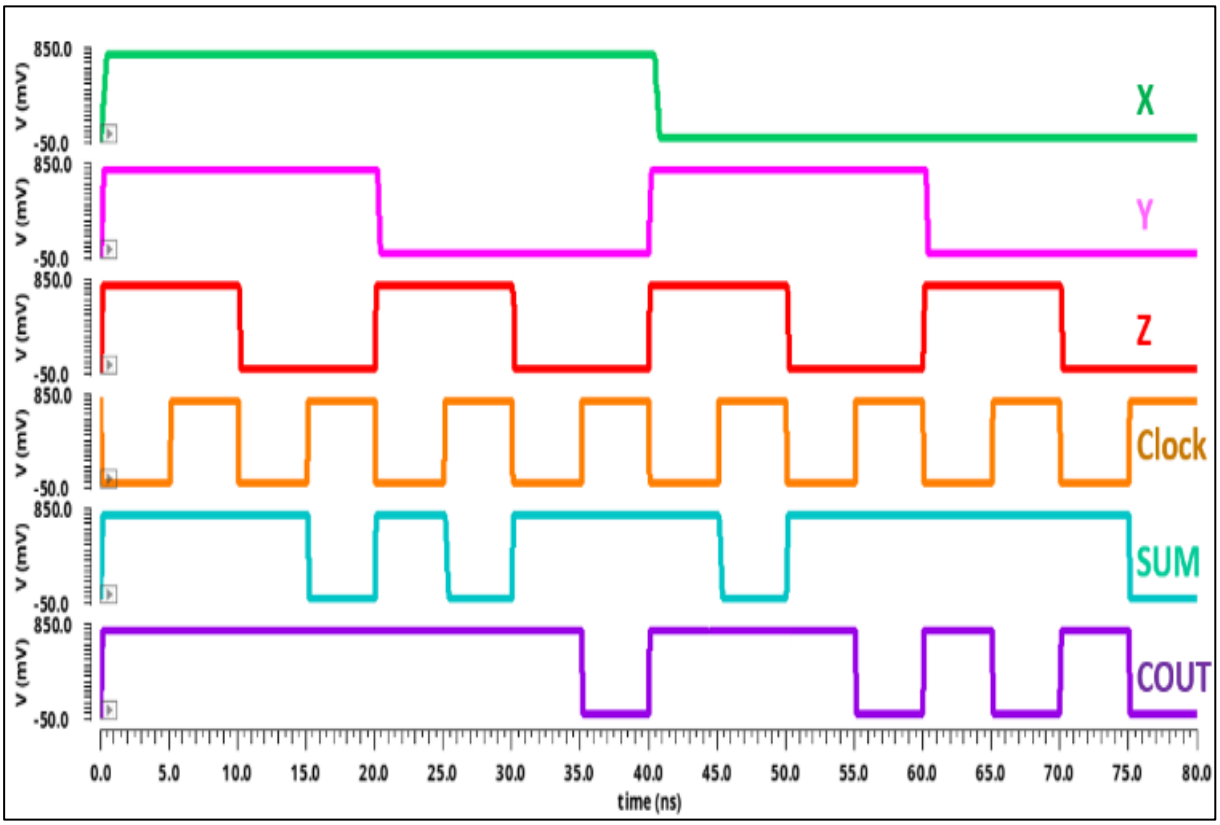


Fig. 5.10 Simulation result of the1-bit full adder DMGDI based

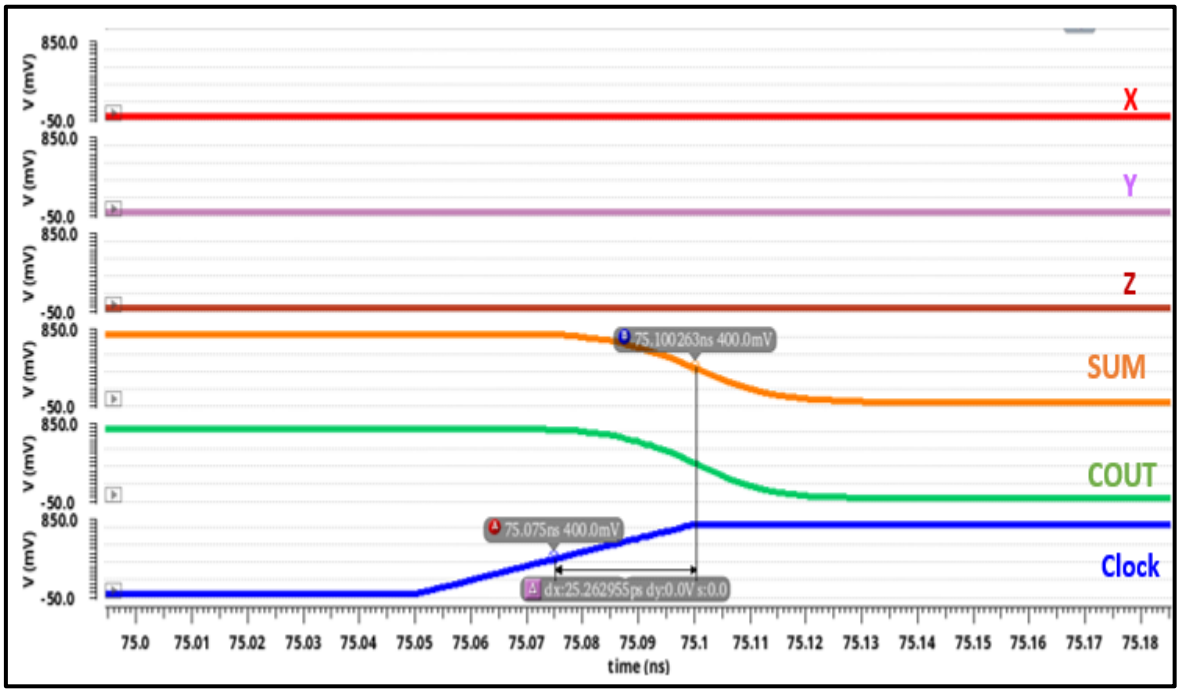
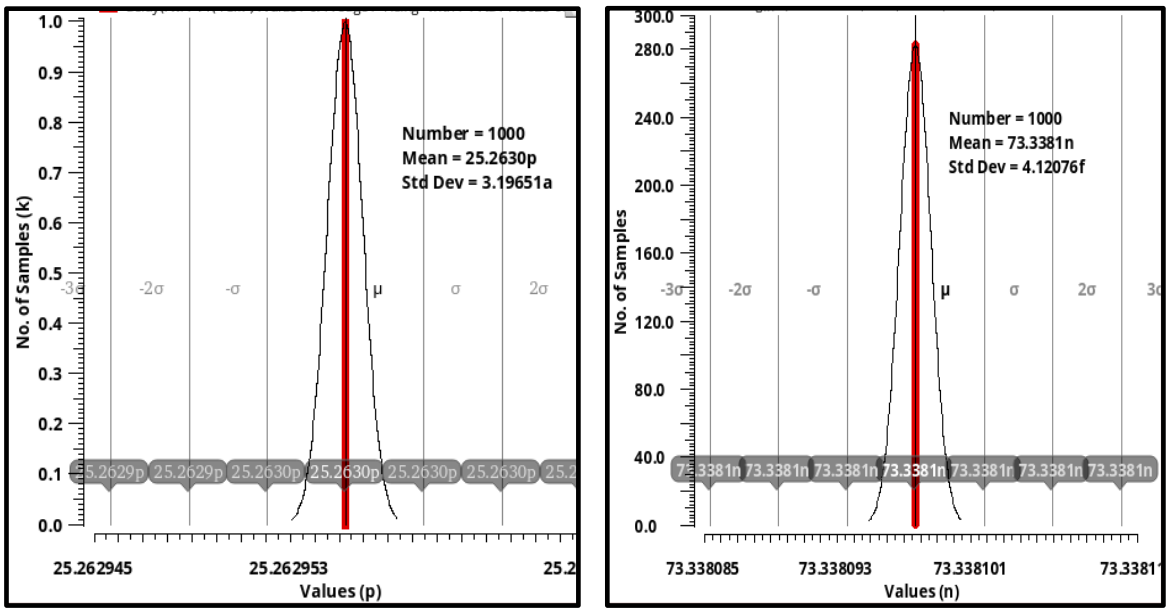


Fig. 5.11 Delay plot of the1-bit full adder DMGDI based

The delay is measured when the clock transits from logic ‘0’ to '1'; SUM and COUT go from logic ‘1’ to ‘0’. Delay calculated by acquiring the concise interval of time between the clock’s rising edge at 50% of Vdd (0.4V) and the output's falling edge at 50% transition value of Vdd (0.4). The delay plot is shown in Fig. 5.11. The simulation of the aforementioned circuit revealed that the delay value for COUT and SUM was around 25.26 ps. The measured power usage was around 73.3 nW.

To evaluate the impact of process variation on the delay and power consumption of the DMGDI-based 2x2, a Monte Carlo simulation involving 1000 samples was conducted. The Monte Carlo simulation power consumption and delay plot for the full adder, with a 15% pitch variation, is displayed in Fig. 5.12. As may be shown, the power consumption and delay standard deviations are 16.6f and 22.7a, respectively. As a result, the circuit exhibits resistance to changes in process.



(a) (b)

Fig. 5.12: Monte Carlo plot for full adder based on DMGDI (a) delay (b) Power consumption

5.5 4-bit Ripple Carry Adder based on DMGDI

Ripple carry adder based on the dynamic gate diffusion input also developed as per the architecture of the RCA as shown in Fig. 2.22. The transient response of the RCA is shown in the Fig. 5.13. The Ripple Carry Adder (RCA) based on Dynamic Gate Diffusion Input (GDI) was simulated in Cadence Virtuoso. During the simulation, the input values were set as follows:

- Period of A: 120 nm
- Period of B: 60 nm
- Period of C: 30 nm with a duty cycle of 50%

- Voltage range of the input voltage: 0-0.8V
- Vdc: 0.8V

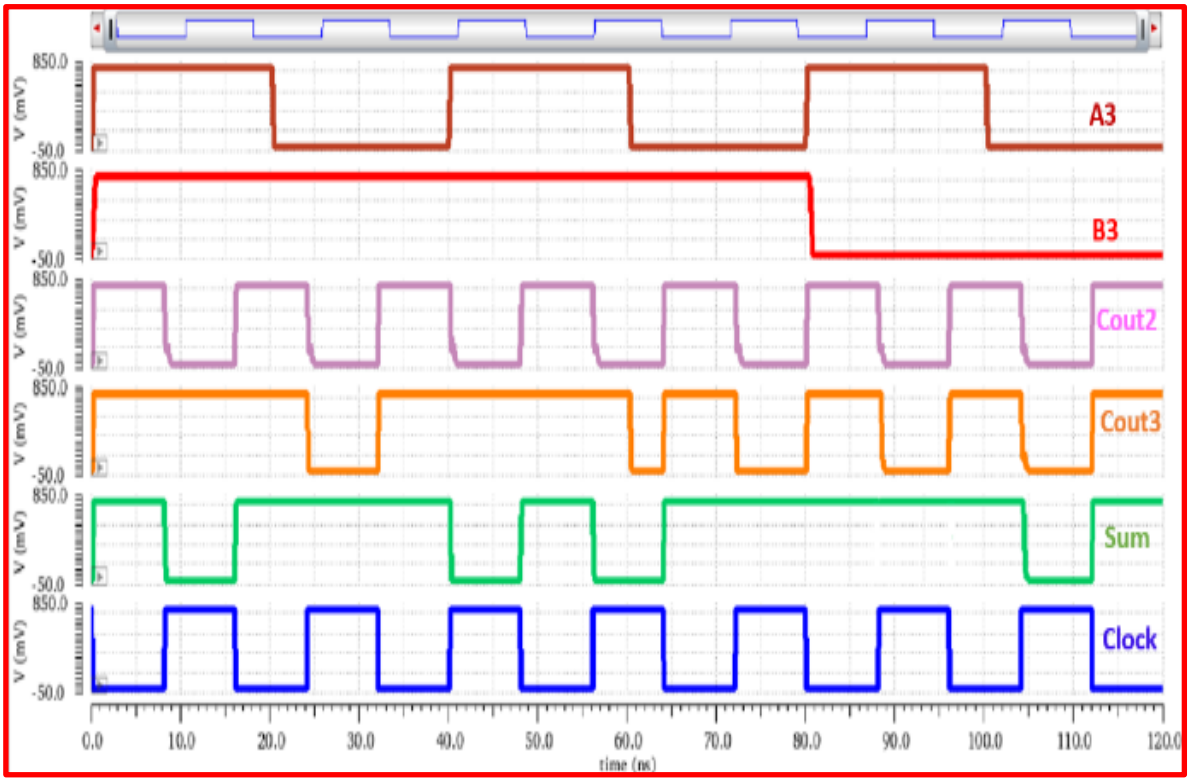


Fig. 5.13: Simulation result of the 4-bit RCA DMGDI based

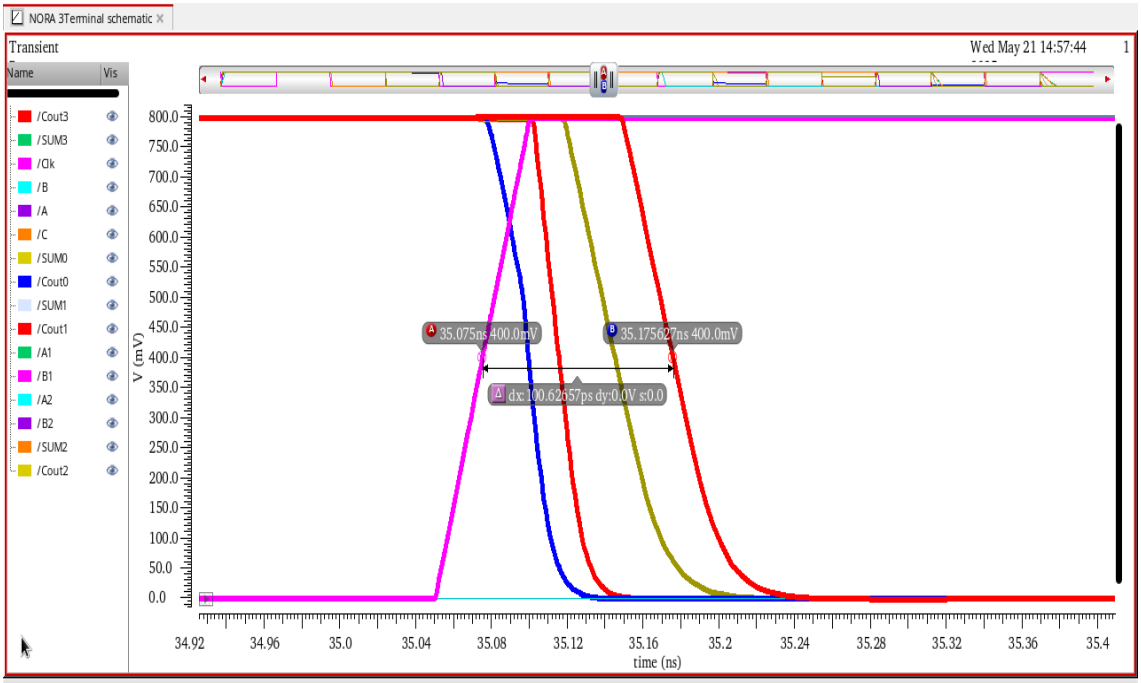


Fig. 5.14: Delay plot of the 4-bit RCA DMGDI based

5.6 Multiplier based on DMGDI

A 2x2 multiplier circuitry that accepts two 2-bit binary value (X_1 X_0) and (Y_1 Y_0) as input and yields a 4-bit binary output (S_3 S_2 S_1 S_0) indicating their product. AND gates and two half adder processes are used to compute the multiplication. Fig. 2.26 shows the block diagram used to implement the 2x2 multiplier. Initial circuitry yields four outputs: X_0Y_0, X_1Y_0, X_0Y_1, and X_1Y_1. The product X_0Y_0 yields S_0, the multiplier output's (B) least significant bit (LSB). The S_1 bit is obtained by adding X_1Y_0 and X_0Y_1 using a half adder (HA_1). The S_2 bit is created by adding X_1Y_1 and the carry output from the first half adder (HA_1). The S_3 bit is the carry-out of the second half adder (HA_2). The simulated waveforms for each input and output are shown in Fig. 5.15, and the delay graphs for the 2x2 multiplier are shown in Fig. 5.16. Furthermore, the delay measured for obtaining the MSB of the multiplier output is approximately 41.52 pS. The same circuitry uses about 483.5 nW of power.

After investigating the XOR logic using the DMGDI cell, a full adder, RCA and 2x2 multiplier was built using this cell. All of the circuitry's based on DMGDI-based performance metrics, including latency, power consumption, and PDP, parameters are summarized in the Table 5.2..

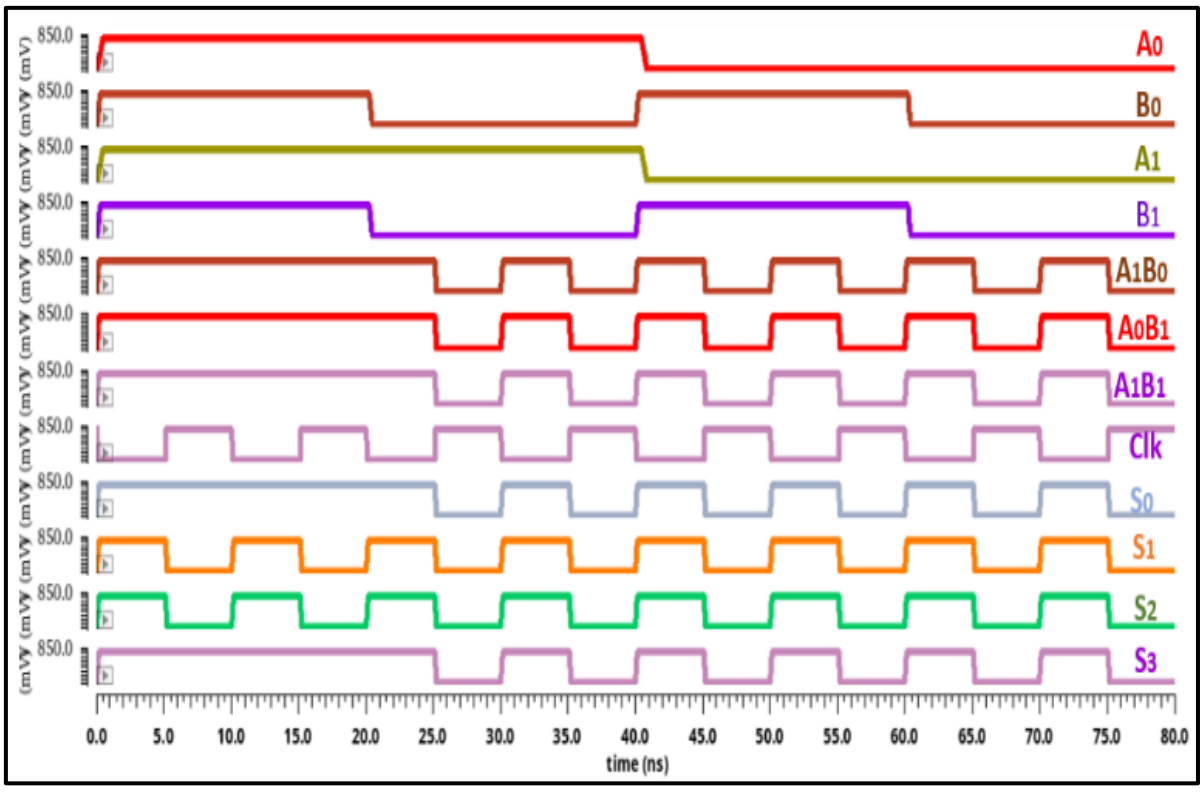


Fig. 5.15: Transient response of 2x2 multiplier

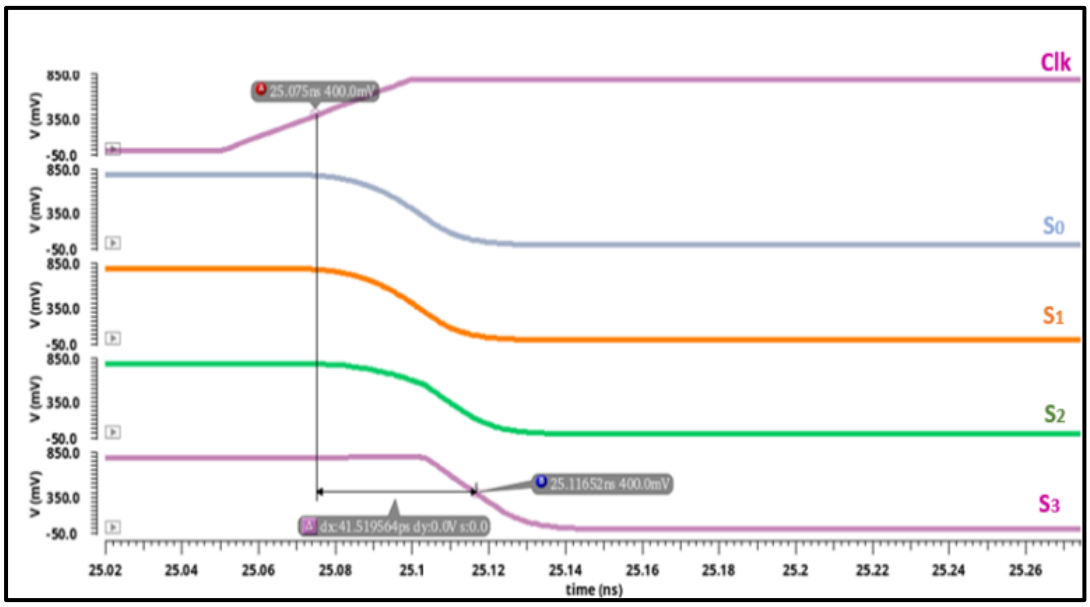


Fig. 5.16: Delay plot for multiplier based on DMGDI cell

5.7 Summary

This chapter studied DMGDI cells, which implement the XOR or XNOR logic by reducing the transistor from six to five.

After employing the DMGDI cell, a basic component of intricate circuitry, to study the XOR logic. This cell was then used to construct a 2x2 multiplier, RCA, and complete adder. All of the circuitry is built using DMGDI-based performance criteria, such as PDP, power consumption, and latency; Table 5.2 provides a summary of the parameters. The DMGDI-based combination circuitry outperformed the current DGDI cells, according to the findings.

Table 5.2: Different circuitry based on DMGDI Cell

Logic Gate	Delay (pS)	Power Consumptions(nW)	PDP (E-18)
XOR Gate (1.8V)	144.71	354.9	51.35
Full Adder (0.8)	25.26	73.3	1.851
RCA (0.8)	94pS	328.5	30.879
Multiplier (0.8)	41.52	283.5	11.770

Chapter 6: Conclusion and Future Scope

A successful approach for creating low-power digital combinational circuits is the Gate Diffusion Input (GDI) methodology. Nonetheless, more developments in GDI technology have been prompted by restrictions in voltage swing for specific logic combinations. To solve this, dynamic variants such as the dynamic GDI cell, dynamic transmission input gate, and dynamic modified GDI have been investigated. To demonstrate its potential, this technology was originally used to create the XOR logic, a fundamental building block; it was then extended to complicated circuits such as complete adders, RCAs, and multipliers. The basic GDI cell and its dynamic variant's delay, power consumption and PDP's were investigated for this research.

All of the circuitry analyzed is implemented with CNFETs due to their low leakage current and compatibility with high-K dielectric materials. This standard aids in the development of a low-power GDI cell without sacrificing speed.

With the basic GDI cell, the output will not have the full swing, this problem addressed by adding dynamic logic block. This cell called as DGDI cell. Since node before dynamic block not has a full swing, therefore, the delay and power-consumption occurred more. To resolve these, two new approaches used in this report: DTGDI and DMGDI. Its performance parameter for different combinational circuitry summarized in the Table 6.1 (a), 6.1 (b), 6.1 (c) and 6.1 (d).

Table 6.1: Comparison between existing DGDI and suggested techniques DTGDI and DMGDI

(a) Comparison among dynamic-GDI families for XOR logic

Dynamic Technique	Delay (ps)	Power consumption (µW)	PDP (E-18)
DGDI	127	1.62	205.7
DTGDI	93.7	1.52	142.424
DMGDI	93.8	1.6	150.08

(b) Comparison among dynamic-GDI families for full adder

Dynamic Technique	Delay (ps)	Power consumption (µW)	PDP (E-18)
DGDI	35.36	0.127	4.49
DTGDI	23.11	0.102	2.35
DMGDI	25.26	0.073	1.84

(c) Comparison among dynamic-GDI families for RCA

Dynamic Technique	Delay (ps)	Power consumption (µW)	PDP (E-18)
DGDI	154.6	0.41	63.38
DTGDI	88	0.377	33.176
DMGDI	94	328.5	30.87

(d) Comparison among dynamic-GDI families for multiplier

Dynamic Technique	Delay (ps)	Power consumption (µW)	PDP (E-18)
DGDI	69.4	0.5207	36.13
DTGDI	61.4	0.49	30.08
DMGDI	41.51	0.483	20.04

The combination of TGDI and dynamic block is called DTGDI. Full swing at the dynamic node's input node has been handled when the transmission model has been used. Therefore, delay and consumption are both reduced in DTGDI as compared to DGDI. Further, a combination of MGDI and dynamic block, DMGDI improves PDP by limiting the input signal to the original signal (not using the complementary input) and lowering the number of transistors. This also led to less PDP as compared to the DGDI cell.

XOR logic: The PDP of DTGDI was found to be 30.4% lower than that of DGDI. In the same way, DMGDI's PDP is 27.03% lower than DGDI's. Even though DTGDI and DMGDI have about the same delay value, MGDI uses power that is comparable to that of the DGDI cell because it also fails to possess a significant swing before the dynamic.

Full-adder: DTGDI and DMGDI-based full adders perform 34.64% and 28.56% faster, respectively, than DGDI. The power consumption of DTGDI and DMGDI is 8.048% and % lower, respectively, than that of DGDI. As a result, DTGDI's PDP was discovered to be 47.66% lower than DGDI's. Similarly, DMGDI's PDP is 59% the lower than DGDI's.

RCA: RCAs based on DTGDI and DMGDI have lower delays than DGDI by 43.07% and 39.19%, respectively. Compared to DGDI, the power consumption of DTGDI and DMGDI is 5.8% and 19.87% lower, respectively. Consequently, it was found that DTGDI's PDP was 47.65% lower than DGDI's. Likewise, the PDP of DMGDI is 51.29% lower than that of DGDI.

Multiplier: The PDP of DTGDI was found to be 47.66% lower than that of DGDI. In the same way, DMGDI's PDP is 59% lower than DGDI's.

From the above result it was conclude that DTGDI and DMGDI based combinational circuitry perform better than existing DGDI cell in term of both delay and power consumptions.

The Gate Diffusion Input (GDI) technique is gaining popularity in low-power digital circuit design due to its ability to reduce power consumption, propagation delay, and transistor count when compared to traditional CMOS circuits.

Future scope of the static GDI and dynamic GDI is listed below:

1. Low-Power VLSI Design: GDI-based circuits will become increasingly important in battery-powered devices such as smartphones and Internet of Things sensors as the need for energy-efficient electronics increases. [29], [30] [31] and [32].

2. High-Speed Computing: By reducing latency, GDI cells can increase processing speed in digital signal processors and microprocessors.[33] and [34]

3. Nano-Scale Integration: GDI approaches will be enhanced for sub-45nm technology nodes, increasing performance and decreasing chip space, thanks to developments in nanoelectronics. [35].

4. AI & Machine Learning Hardware: For effective data processing, GDI-based circuits might be included into AI accelerators and neuromorphic computers [36].

5. Biomedical Applications [37]: Wearable health monitoring and implanted medical devices may make advantage of low-power GDI circuits.

List of Publications

1. GDI and Dynamic Logic: A synergy behind the modern electronics, published in 3rd International Conference on "Device Intelligence, computing and communication technologies, DICCT-2025"

2. Energy Efficient dynamic logic based on TGDI cell for portable electronics, published in 8th Internationational on trends in Electronics and Informatics (ICOEI-2025)

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3rd IEEE International Conference on — Device Intelligence, Computing & Communication Technologies 21-22 March, 2025

DICCT 2025

Certificate of Participation

This is to certify that

yashoda Yashoda

have successfully presented the paper entitled

GDI and Dynamic Logic: A synergy behind the modern electronics

at the 3rd IEEE International Conference on Device Intelligence, Computing, and Communication Technologies (DICCT-2025) organised by the Department of Electronics and Communication Engineering, Graphic Era (Deemed to be University), Dehradun, India held on 21-22 March, 2025.

Dr. Abhay Sharma
Convener

Prof. (Dr.) Md. Irfanul Hasan
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Energy Efficient Dynamic Logic based on TGDI Cell for Portable Electronics

at the 8th International Conference on Trends in Electronics and Informatics (ICOEI-2025) held from 24th-26th,April 2025 at SCAD College of Engineering and Technology, Tirunelveli, Tamil Nadu, India.

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