DESIGN AND PERFORMANCE ANALYSIS OF AN IMPROVED LOW-POWER 8T SRAM CELL FOR ENHANCED WRITABILITY

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by

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I, **Akhilesh Vishwakarma (2K23/VLS/15)** hereby certify that the work which is being Presented in the thesis entitled **"Design and Performance Analysis of an Improved Low-Power 8T SRAM Cell for Enhanced Writability"** in partial fulfillment of the requirement for the award of the Degree of Master of Technological, submitted in the Department of Electronics and Communication Engineering, Delhi Technological University is an authentic record of my own work carried out during the period from August 2023 to June 2025 Under the supervision of **Prof. Poornima Mittal**.

The matter presented in the thesis has not been submitted by me for award of any other degree of this or any other Institute.

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Place: Delhi

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ABSTRACT

In modern electronics, memory is a core component that enables data storage and retrieval, but cache memory is even more critical due to its direct connection to the CPU. Cache memory is designed to provide the processor with quick access to frequently used data and instructions. It relies on millions of SRAM cells, which must be highly efficient to maintain performance. These cells are required to operate with low power both static and dynamic while ensuring data remains stable and accessible. Fast read response times are also essential so that the processor is not bottlenecked during execution.

This review discusses the core elements of SRAM cell design and how they impact performance. It starts by explaining why SRAM matters in computing systems and how each cell functions. The focus is placed on data stability, speed during read and write operations, and minimizing power consumption. The review explores different cell architectures and the trade-offs they involve. It addresses key design challenges, including sensitivity to noise and issues caused by manufacturing variations. It also covers improvements such as assist techniques and feedback loops. The impact of shrinking technology nodes on these cells is reviewed in detail.

The performance of SRAM cells is evaluated by analyzing factors like read and write delay, write margin, stability, and power usage. This review explores how variations in design elements such as transistor sizes, supply voltage, and output loading affect these characteristics. It also looks into how process fluctuations impact the reliability and yield of SRAM cells and outlines possible solutions to enhance long-term performance and stability. This work presents a detailed Monte Carlo analysis of various 7T and 8T SRAM cell topologies at the 45nm technology node, simulated using the Cadence Virtuoso tool. The primary focus is to evaluate and compare the static and dynamic characteristics of these designs against a newly proposed 8-transistor SRAM cell, named 8TSEDPP. The analysis encompasses critical design metrics such as Hold Static Noise Margin (HSNM), Read Static

Noise Margin (RSNM), Write Margin (WM or N-Curve), dynamic power consumption, and access times for read and write operations. The proposed 8TSEDPP circuit stands out with significant improvements in stability, power efficiency, and performance balance. In terms of RSNM, the proposed cell achieves 205 mV, outperforming all other designs, including 7TDESPP and 7TSESPK, with an average improvement of over 45%. The Write Margin also shows a notable enhancement, reaching 510.41 mV, which represents a 13.5% increase over traditional 7T cells like 7TDESPC and 7TDESPL. Despite being a more complex circuit, the dynamic power consumption of the proposed 8TSEDPP is just 317.8 nW, which is a remarkable 67.6% reduction compared to the baseline 7TDESPT design. This makes the proposed cell highly suitable for low-power applications without sacrificing stability.

Timing analysis further strengthens the case for 8TSEDPP. The Write '0' access time is measured at 205 ps, while Write '1' access time is 291.6 ps, both of which remain within acceptable limits for high-performance applications. Although some 7T cells exhibit slightly faster access times, they lag significantly in power and noise margin performance. The Read Access Time of 510.41 ps, although not the fastest, offers a balanced trade-off given the robustness in other areas. Overall, the 8TSEDPP SRAM cell demonstrates the best overall balance across all performance, stability, and power metrics, validating its suitability for energy-sensitive and high-reliability memory applications. The proposed design is particularly promising for next-generation VLSI circuits used in portable, embedded, and IoT-based devices, where low leakage, reliable write operations, and immunity to process variations are critical. The results obtained through extensive simulations confirm that 8TSEDPP is a strong candidate for replacing or complementing traditional SRAM architectures in future semiconductor designs.

LIST OF PUBLICATIONS

SCOPUS INDEXED CONFERENCES

1. A. Vishwakarma and P. Mittal, “Trade-offs in 7T SRAM Cells for Low-Power VLSI: A Quantitative Analysis”, International Conference on Electrical, Electronics & Automation (E2ACON - 2025), Jalandhar, India, March 2025 (**Scopus Indexed**)

   Status of Paper: Presented in the conference on 8st March 2025

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LIST OF ABBREVIATIONS

S. No.	Abbreviation	Full Name
1.	SRAM	Static Random Access Memory
2.	BL	Bit Line
3.	BLB	Bit Line Bar
4.	WL	Word Line
5	WLB	Word Line Bar
6.	SNM	Static Noise Margin
7.	HSNM	Hold Static Noise Margin
8.	RSNM	Read Static Noise Margin
9.	DEDP	Differential Ended Differential Port
10.	EN	Enable
11.	MOS	Metal Oxide Semiconductor
12.	IC	Integrated Circuit
13.	SA	Sense Amplifier
14.	P	Power
15.	T	Transistor
16.	ROM	Read Only Memory
17.	DRAM	Dynamic Random Access Memory
18.	SoC	System on Chip

19.	IoT	Internet of Things
20	GND	Ground
21.	CMOS	Complementary Metal Oxide-Semiconductor
22.	PMOS	P-type Metal Oxide Semiconductor
23.	NMOS	N-type Metal Oxide Semiconductor
24.	WL	Word Line
25	WLB	Word Line Bar
26	DESP	Differential Ended Single Port
27	SEDP	Single Ended Deferential Port
28	SESP	Single Ended Single Port
29	VDD	Supply Voltage
30	VTH	Threshold Voltage
31	TEFT	Tunnel Field-Effect Transistor
32	WWL	Write Word Line
33	RWL	Read Word Line
34	RBL	Read Bit Line
35	PUPL	Pull Up PMOS left
36	PUPR	Pull Up PMOS Right
37	PDNL	Pull Up NMOS left

CHAPTER 1
INTRODUCTION

SRAM (Static Random-Access Memory) cell is a fundamental building block of computer memory systems. It is a type of volatile memory that can store data as long as power is supplied to the system. The SRAM cell is known for its high speed and low power consumption, making it an essential component in various electronic devices, such as microprocessors, cache memories, and graphics cards. As the demand for faster and more efficient computing continues to rise in the future, SRAM cells are expected to play a crucial role in meeting these requirements. With the increasing adoption of artificial intelligence, Internet of Things, and edge computing applications, the demand for SRAM cells is expected to grow even further, driven by the need for high-speed data processing, low-latency access, and power efficiency. Additionally, emerging technologies such as self-driving cars, smart cities, and advanced robotics will also contribute to the increased demand for SRAM cells in the future, making them a vital component in the evolving landscape of computing and information technology.

This chapter is structured into five distinct sections. The first section (1.1) introduces the SRAM array, a fundamental element of memory architecture composed of numerous SRAM cells arranged in a matrix format. It also includes several subsections that briefly explain the conventional 6T SRAM cell along with its hold, read, and write operations. The second section (1.2) outlines the motivation behind this study, emphasizing why this area continues to attract significant research interest. Section three (1.3) states the main goals and objectives of the research. The fourth section (1.4) describes the approach and techniques used to carry out the study. Finally, the fifth section provides a comprehensive overview of how the thesis is organized.

1.1 SRAM ARRAY

An SRAM array refers to the organization and structure of static random access memory cells within a memory module or chip. The SRAM array is responsible for storing and retrieving data in a random access manner, allowing for fast read and write operations.

The basic building block of an SRAM array is a single SRAM cell, which typically consists of six transistors [1]. These transistors form a flip-flop circuit that can store one bit of data. The SRAM array is constructed by arranging multiple SRAM cells in a grid-like pattern, with rows and columns forming the addressable locations of the memory.

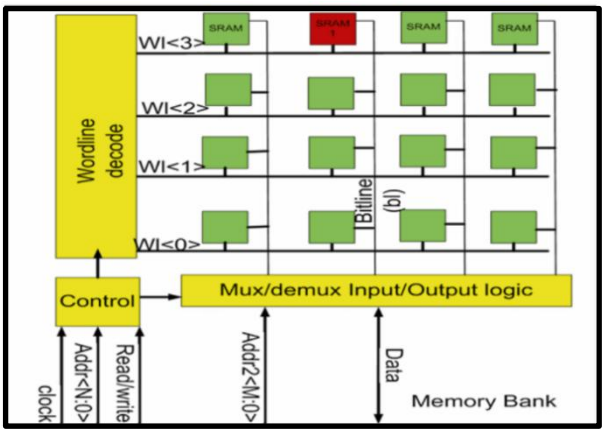


Fig. 1.1 Typical arrangement of an SRAM array, showing the periphery (in yellow) and the cells (in red), with one row of cells accessed (dark red)

The size of an SRAM array is defined by the number of rows and columns of SRAM cells. Each row represents a word line, and each column represents a bit line. The intersection of a row and column represents a specific memory location, where data can be stored or retrieved.

To read data from an SRAM array, the desired address is provided, activating the corresponding word line and allowing the stored data in the selected column to be accessed and read out. Similarly, writing data involves providing the address and data to be written, and activating the appropriate word line and bit line to store the new data in the desired memory location.

The organization and design of the SRAM array play a crucial role in determining the overall capacity, speed, and power consumption of the SRAM chip. Various techniques, such as hierarchical organization, pipelining, and multiplexing, can be employed to optimize the performance of the SRAM array and meet the requirements of different applications [3].

1.1.1 Conventional Six-transistor Cell

The design of the cell includes multiple vertical and horizontal control lines for each memory unit. In a typical 6-transistor SRAM, each cell requires one horizontal control line called the word line and one vertical line referred to as the bit line.

The traditional 6T memory cell plays a vital role in contemporary memory architectures and is commonly found in processors, cache units, and various digital circuits. It is made up of six transistors arranged in a cross-coupled latch setup. This configuration creates a feedback loop through the inverters, enabling the cell to hold data steadily without requiring continuous refreshing.

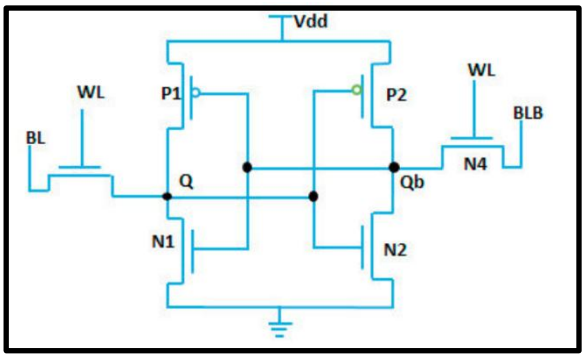


Fig. 1.2 Typical 6T SRAM cell

The 6T SRAM cell comprises a pair of intricately cross-coupled inverters, where the output of each inverter is routed to the input of the other, as depicted in Figure 1.2. This interconnected architecture establishes two complementary internal storage nodes, commonly referred to as bitline and bitline_bar. Each inverter is constructed using one PMOS transistor, known as the pull-up device, and one NMOS transistor, termed the pull-down device. Complementing this setup, two additional NMOS transistors function as pass-gates, facilitating a controlled connection between the internal nodes and the corresponding bit lines, enabling efficient data read and write operations.

The 6T SRAM cell offers key benefits such as fast access, low power use, and data retention with continuous power. However, it requires more chip area than some alternatives and is more prone to noise and process variations. Despite this, it remains essential in digital systems for its speed, reliability, and adaptability.

1.1.2 Data Hold Operation

The data storage capability of an SRAM cell relies on its two cross-coupled inverters. When the word line (WL) is low, the pass-gates are disabled and effectively disconnected. If the bit line holds a 1, the top inverter drives bit_bar to 0, and the bottom inverter reinforces the 1 on bit, confirming data retention. A similar process occurs if the stored value is 0, maintaining stability through feedback.

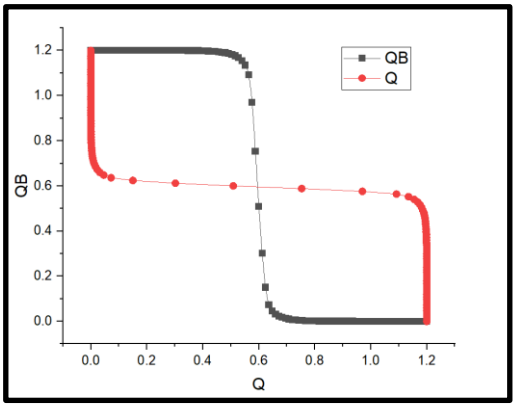


Fig. 1.3 Transfer curves of the two inverters in an SRAM cell

As shown in Figure 1.3, plotting the transfer curves reveals three intersection points. The central point is unstable, while the other two represent the stable states of the cell, corresponding to stored values of either 0 or 1.

The 6T SRAM cell primarily utilizes two transistor-based inverters to retain data, a configuration that minimizes its area footprint. However, the conventional inverters can be replaced with alternative, more advanced designs that can also store the two possible logical states. These alternative designs may involve altering the dimensions of the pull-up and pull-down transistors, or employing more complex circuits, such as inverters incorporating additional transistors like Schmitt triggers. Such modifications can significantly enhance the cell's performance by improving key attributes, including noise immunity, stability, and overall reliability under varying operating conditions.

1.1.3 Write Operation

The two-looped inverters at the core of the cell can accumulate both probable data. The need to trigger the wanted value to behold in the cells, which is called as the write operation.

The write operation begins by setting the word line to V_{DD}, which stimulates the pass gates. In the meantime, the edge on the top of Figure 1.1 sets the bitlines to the value to be written in the interior nodes of the cell. When an inverse value is written than the one being kept, the pass gate is imposing a value while the inverter is trying to hold the opposite one. The transistors must be sized so that the pass gate surpasses the inverter in order to attain a effective write.

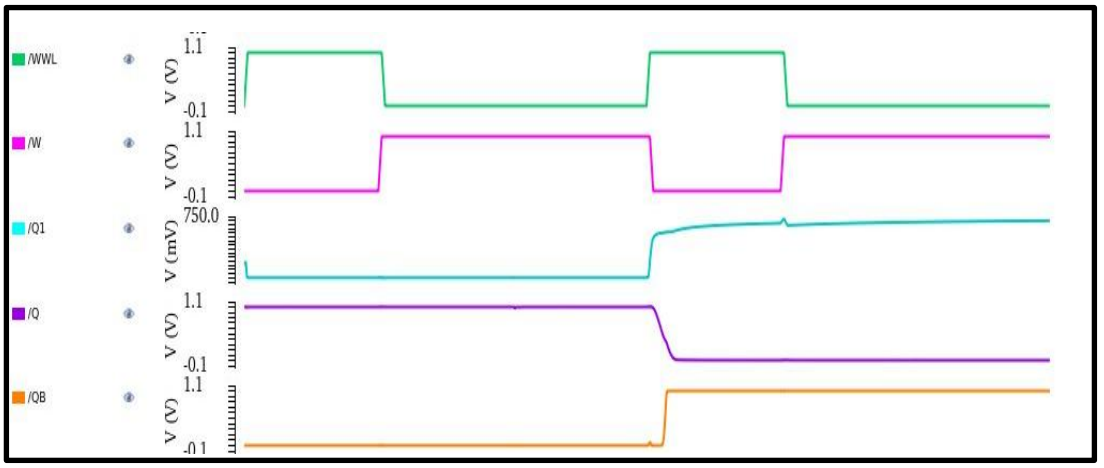


Fig. 1.4 Transient simulation of a write operation in a 6T SRAM cell

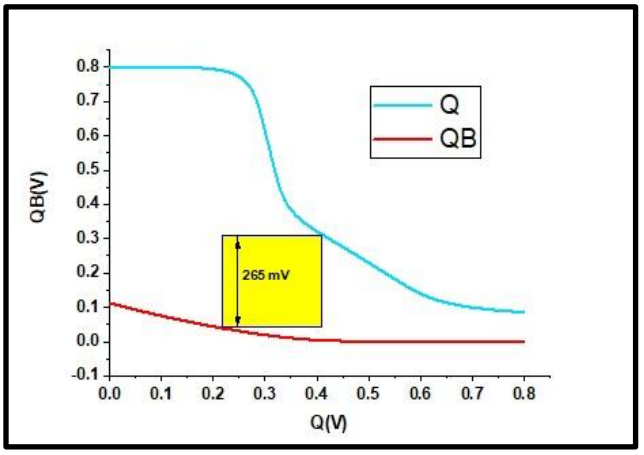


Fig .1.5 Modified transfer curves of the inverter while writing

A transient simulation showcasing the write operation is depicted in Figure 1.4. Initially, the SRAM cell is storing a logic high (‘1’), as indicated by the voltage levels at its internal nodes—bit is at VDD, and bit_bar is at 0 V. To write a new value (the opposite of the stored one), the bit lines are driven to bitline = 0 V and bitline_bar = VDD. At t = 1 ns, the word line is raised from 0 V to VDD, activating the access (pass) transistors. This action enables the data on the bitlines to overwrite the contents of the storage nodes, effectively flipping the voltages of bit and bit_bar.

Once the write operation is completed, and the word line is pulled back to ground, the new data remains latched within the cell due to the regenerative feedback of the inverters. The enabled pass transistors during the write operation alter the inverter transfer characteristics, as illustrated in Figure 1.4, resulting in a single stable operating point at the intersection of the curves. This unique crossing point ensures the cell retains the newly written logic state once the word line is deactivated.

The voltage levels on the bit lines during the write operation dictate the stable state that the cell adopts. When the bitline is grounded and bitline_bar is set to VDD, the cell is forced into storing a logic '0', as demonstrated in Figure 1.5(a). Conversely, applying the opposite condition bitline = VDD and bitline_bar = 0 V causes the cell to store a logic '1', as seen in Figure 1.5(b).

1.1.4 Read Operation

After a value has been successfully written and retained by the cell, the next crucial step is to read the stored data. While accurately retrieving the data is essential, it is equally important that the read operation does not disturb or modify the contents of the cell. Ensuring data integrity during read access is a key requirement for reliable memory performance.

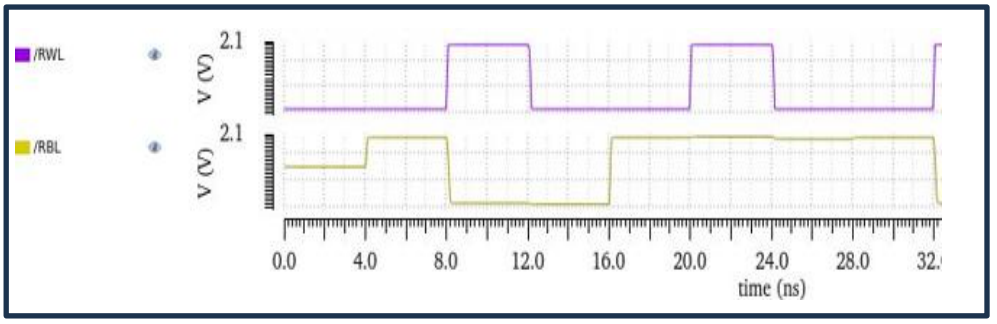


Fig.1.6 Transient Simulation of a Read Operation

In a 6T SRAM cell, the read operation begins by raising the word line voltage from ground to VDD, which turns on the pass transistors. Instead of driving the bit lines to specific logic levels, they are precharged to VDD and then left floating. The pass transistor connected to the internal node held at ground will draw current from the corresponding bit line, causing it to discharge gradually, as illustrated in Figure 1.6.

The read circuitry at the bottom of Figure 1.1 detects the voltage difference between the two bit lines and amplifies it to recover the data stored in the cell. This circuit, known as the sense amplifier, typically requires only a small voltage difference around 10% of the supply voltage to accurately sense the stored value.

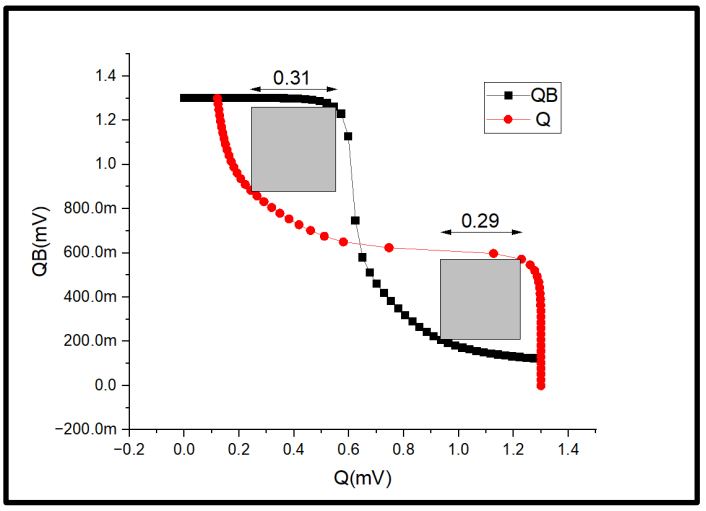


Fig.1.7 Modified transfer curves during a Read Operation

During the read operation, the inverter transfer curves change as depicted in Figure 1.7. The curves intersect three times, resulting in two stable points, which ensures that the stored data remains unchanged. However, compared to the curves shown in Figure 1.3, these curves are closer together, indicating reduced stability and increased susceptibility to noise. This effect is also visible in Figure 1.6, where the voltage at the internal node bit_bar shifts during the read access.

1.2 MOTIVATION

The motivation behind research in 8T SRAM cells arises from the growing need for high-performance, low-power memory in modern computing systems. With the increasing demand for data-intensive technologies such as AI, virtual reality, and big data, traditional 6T SRAM cells face limitations in stability, leakage, and power efficiency. The 8T SRAM cell design offers a promising solution by incorporating extra transistors that improve stability, reduce leakage, and enhance read and write performance. Understanding the characteristics of 8T SRAM cells will help identify their potential advantages and limitations, ultimately advancing the development of more efficient and reliable memory systems.

The exploration of 8T SRAM cells is driven by the need to tackle the scaling issues faced by traditional SRAM and 7T SRAM designs. As technology nodes continue to shrink, scaling down 6T SRAM cells becomes increasingly challenging due to a range of physical and electrical constraints. By adding extra transistors, the 8T SRAM architecture offers improved

scalability and performance for advanced technology nodes. Through static and dynamic analysis, circuit simulations, and characterization, we can evaluate the feasibility of 8T SRAM cells for future technology generations. The research aims to overcome the limitations of current memory technologies and create more reliable solutions.

1.3 OBJECTIVE

The objective of this study is to investigate and evaluate the performance of SRAM cells, which are essential for memory storage and data retrieval in modern digital systems. With the rising demand for high-speed and energy-efficient memory solutions, it is vital to understand the behaviour of advanced cell architectures. By concentrating on 8T SRAM cells, this research aims to examine their strengths, weaknesses, and potential uses. Through rigorous experimentation and analysis, the goal is to provide critical insights and contribute to the progression of SRAM technology for future systems.

Primary objectives of this research project are as follows:

- To Compare multiple SRAM designs for the same technology nodes, power supply, and transient time. This also helped to determine the trend of SRAM being used for low- power applications.
- To understand the working of SRAM cell and which one out performs the others, a comparison is done between existing structures and modified SRAM cell structure. A mathematical calculation is also performed for the PDP analysis. To establish which circuit had the best performance, SRAMs are compared, and their findings are illustrated.
- To design and analyze a modified SRAM cell structure that includes a back-to-back inverter, buffer transistors, and access transistors. For optimal performance, power analysis, delay analysis, and the data stability are all performed.

The emphasis of this research is to create an up-to-date better SRAM cell structure that uses low-energy and low-power components and may be used in low-power applications. Multiple SRAM cell topologies on the same technology node, with the same aspect ratios and transient times, were compared for this. Then, for the best performance, the existing SRAM cell designs are compared to the modified design.

1.4 METHODOLOGY

A comparative performance analysis has been carried out between various 7T SRAM cells and the proposed 8T SRAM cell. The evaluation includes key parameters such as data stability, power consumption, read delay, and write delay. In most aspects, the proposed 8T SRAM cell demonstrates improved stability and significantly lower power consumption; however, it exhibits a slightly higher write access time compared to conventional 7T SRAM cells.

The proposed 8T design has been implemented and analyzed through various simulations. It consists of a total of eight transistors—two PMOS and six NMOS—which are categorized into pull-up, pull-down, and access transistors. The analysis covers critical factors such as data stability, power dissipation, read delay, and write delay. This research focuses on developing low-power and high-stability SRAM architectures. Additionally, various sense amplifier parameters and stability metrics such as HSNM, RSNM, and WSNM have been investigated across different voltage levels.

The proposed 8T SRAM cell outperforms traditional 6T and 7T SRAM structures in terms of noise immunity and energy efficiency. However, the increased write access time is a trade-off. Therefore, the selection of an SRAM cell architecture should depend on the specific design requirements and the balance between power, area, speed, and stability.

1.5 THESIS ORGANIZATION

This thesis is organized into five main chapters. Chapter 1 serves as the introduction, providing an overview of the SRAM array and the traditional 6T SRAM cell. It also covers the motivation behind the study, outlines the research objectives, explains the adopted methodology, and describes the structure of the thesis. Chapter 2 presents a comprehensive review of existing literature and identifies the existing gaps in current technology. Chapter 3 offers an in-depth comparative evaluation of various 7T SRAM cells. In Chapter 4, the design and analysis of the proposed 8T SRAM cell are discussed in detail, along with its performance metrics and parameter assessment. Chapter 5 builds on this by comparing the earlier reviewed SRAM designs from Chapter 3 with the modified 8T cell, highlighting its performance improvements over previously reported architectures. Finally, Chapter 6 summarizes the findings and outlines potential directions for future work.

CHAPTER 1 - This chapter offers a fundamental introduction to SRAM arrays and cells, emphasizing their integral role in memory systems and their functionality under low-power and low-voltage conditions. It also outlines the research objectives, the motivation behind the study, the methodology employed, and the overall structure of the thesis.

CHAPTER 2 - This chapter presents an in-depth overview of previous research related to SRAM. It critically examines various parameters discussed in the existing literature and consolidates key academic studies and publications concerning SRAM cells. The literature review aims to build a thorough understanding of the current knowledge landscape, highlight gaps or contradictions in prior research, and establish a solid groundwork for the present study.

CHAPTER 3 - This chapter presents a comparative analysis of various 7T SRAM cells, emphasizing their structure, functionality, and performance characteristics. The evaluation was conducted at the 45nm technology node using a range of supply voltages from 0.2V to 1.4V. Depending on their architectural configurations, key parameters such as static noise margin, read/write delay, and power consumption were assessed and compared.

CHAPTER 4 - This chapter presents the proposed design of the 8T SRAM cell, detailing its architecture and operational principles. Key performance metrics such as data stability, read/write delay, and power consumption are thoroughly evaluated. Additionally, Monte Carlo simulations are conducted to assess the reliability and robustness of the proposed cell under process variations. These comprehensive analyses serve to demonstrate the overall effectiveness and performance advantages of the proposed design.

CHAPTER 5 - This chapter presents a detailed comparative analysis between the proposed 8T SRAM cell and four existing 7T SRAM cell designs to demonstrate the superior performance of the proposed architecture. The comparison is carried out based on three key parameters: static noise margins, access delays, and power consumption. Additionally, the analysis includes an evaluation of Read Static Noise Margin (RSNM) and Hold Static Noise Margin (HSNM) under both constant and varying supply voltages. This voltage variation study highlights the robustness and stability of the proposed design across a wide operating range.

CHAPTER 6 - This chapter concludes the dissertation by summarizing the overall findings and results obtained from the research. It also discusses potential future improvements and directions related to the research topic.

Additionally, the chapter includes a list of publications resulting from the work conducted in this thesis. Following that, a comprehensive list of references is provided, citing previous studies that helped guide and support the present research.

CHAPTER 2
LITERATURE REVIEW

A thorough review of the existing literature is essential for any research endeavor. The purpose of conducting a literature review is to:

- Build a comprehensive foundation of understanding regarding the subject matter
- Recognize established areas of expertise to avoid redundancy and properly acknowledge the contributions of previous scholars
- Identify contradictions in prior studies, uncover research gaps, highlight key areas of conflict within the existing literature, and address unresolved issues or questions that warrant further investigation

This chapter is divided into two parts. Section 2.1 provides a comprehensive summary of previous research, while section 2.2 addresses the existing technical gaps identified in the literature.

2.1 COMPREHENSIVE SUMMARY OF PAST WORK

- **Low-power cache design using 7T SRAM cell, 2007**

R Ramy E. Aly and Magdy A. Bayoumi [15] proposed a novel 7-transistor (7T) SRAM cell architecture aimed at reducing power consumption in cache memory applications. The design introduces an additional transistor to decouple the read and write paths, thereby enhancing read stability and reducing the risk of read disturbances. By utilizing only one bit line during write operations, the cell significantly reduces dynamic power consumption. HSPICE simulation results demonstrate that the proposed 7T SRAM cell achieves at least 49% reduction in write power compared to conventional 6T designs, along with improved static noise margins and no performance degradation. Although the addition of a seventh

transistor leads to a slight increase in silicon area (approximately 12.25%), the overall trade-off favors energy-efficient cache implementations.

- **A 7T security oriented SRAM bitcell, 2019**

R. Giterman, O. Keren, and A. Fish [16] proposed a novel 7-transistor (7T) SRAM bitcell architecture aimed at enhancing security against side-channel attacks, particularly power analysis (PA) attacks. The design incorporates an additional transistor to the conventional 6T SRAM cell and introduces a two-phase write operation. This approach significantly reduces the correlation between the stored data and the power consumption during write operations, thereby mitigating the risk of information leakage through power analysis. Implemented in a 28 nm CMOS technology, the proposed 7T SRAM cell demonstrates over 1000× lower write energy standard deviation between writing '1' and '0' compared to a standard 6T SRAM cell. Additionally, it achieves a 39%–53% reduction in write energy and a 19%–38% decrease in write delay relative to other power analysis-resistant SRAM designs. These improvements make the 7T SRAM cell a promising candidate for secure memory applications in cryptographic and embedded systems.

- **Differential Read/Write 7T SRAM with Bit-Interleaved Structure for Near-Threshold Operation, 2021**

J. Sang Oh, J. Park, K. Cho, Tae Woo Oh, and Seong Ook Jung [17] introduced a differential 7-transistor (7T) SRAM bitcell optimized for near-threshold voltage (V_{th}) operations, aiming to reduce energy consumption while maintaining high read stability and write ability. The design incorporates an additional row-based control signal and an nMOS transistor between the pull-up and pull-down transistors on one side of the cross-coupled inverter. This configuration enhances the cell's resilience to V_{th} variations, which are more pronounced in near-V_{th} operations. Furthermore, the proposed SRAM bitcell supports a bit-interleaved structure without encountering the half-select issue, thereby improving reliability. Compared to differential 10T and 12T SRAM designs, the proposed 7T SRAM achieves 5% and 6% higher operating frequencies, 70% and 23% lower operation energy consumption, and 33% and 49% smaller bitcell areas, respectively. These improvements make it a promising candidate for energy-efficient memory applications in advanced CMOS technologies.

- **A Near-Threshold 7T SRAM Cell with High Write and Read Margins and Low Write Time for Sub-20 nm FinFET Technologies, 2015**

M. H. Ansari, H. Kusha, B. Ebrahimi, Z. Navabi, A. Kusha, and M. Pedram [18] proposed a 7-transistor (7T) SRAM cell optimized for near-threshold operation in sub-20 nm FinFET technologies. The design modifies a previously introduced 5T cell by incorporating an additional access transistor and appropriately setting the threshold voltages of the transistors to enhance both read and write stability. The cell employs differential write and single-ended read operations, achieving high write and read margins, low write time, and ultra-low leakage power in the hold "0" state. HSPICE simulations using 20 nm, 16 nm, 14 nm, 10 nm, and 7 nm FinFET technologies at a supply voltage of 500 mV demonstrate that the proposed 7T cell outperforms conventional 5T, 6T, 8T, and 9T SRAM cells in terms of Ion/Ioff ratio, write speed, and leakage power. Additionally, the cell maintains stability across a temperature range from −40 °C to 100 °C and under process variations at supply voltages of 400 mV and 500 mV, meeting the required 6σ yield criteria. These characteristics make the proposed 7T SRAM cell a promising candidate for high-performance and low-power applications in advanced CMOS technologies.

- **A Near-Threshold Soft Error Resilient 7T SRAM Cell with Low Read Time for 20 nm FinFET Technology, 2017**

R. N. Asli and S. Taghipour [19] proposed a 7-transistor (7T) SRAM cell optimized for near-threshold operation in 20 nm FinFET technology, focusing on enhancing soft error resilience and reducing read time. The design builds upon a previously proposed 5T cell by incorporating an additional transistor, enabling single-ended read and differential write operations. This configuration improves read speed without compromising write performance. HSPICE simulations at a supply voltage of 0.5 V demonstrate that the proposed 7T SRAM cell achieves high write speed, improved read and write margins, and low leakage power in the hold "0" state compared to the 5T cell. Furthermore, the cell exhibits robust performance under process and environmental variations, including aging effects, making it a promising candidate for reliable low-power applications in advanced CMOS technologies.

- **Low-Power Circuit Analysis and Design Based on Heterojunction Tunneling Transistors (HETTs), 2013**

Y. Lee, D. Kim, J. Cai, I. Lauer, Leland Chang, Steven J. Koester, Dennis Sylvester, and David Blaauw [20] proposed a novel low-power circuit design approach utilizing Si/SiGe Heterojunction Tunneling Transistors (HETTs). These transistors exhibit a subthreshold swing below the 60 mV/decade limit of conventional MOSFETs, enabling steeper subthreshold characteristics and improved low-voltage operation. The authors developed a Verilog-A device model based on Technology Computer-Aided Design (TCAD) simulations to evaluate HETT-based circuits. Their analysis demonstrated that a HETT-based ring oscillator achieves a 9–19× reduction in dynamic power compared to a CMOS ring oscillator. Additionally, they proposed a 7-transistor HETT-based SRAM cell, which leverages the asymmetric current flow characteristics of HETTs to achieve a 7–37× reduction in leakage power compared to conventional CMOS SRAM cells. This work highlights the potential of HETTs in enabling ultra-low-power circuit designs for future nanoelectronics.

- **A comprehensive analysis of different 7T SRAM topologies to design a 1R1 W bit interleaving enabled and half select the free cell for 32 nm technology node, 2022**

B. Rawat and P. Mittal [13] presented a comprehensive study analyzing various 7T SRAM topologies to design a single-ended, dual-port 1R1W bit cell with interleaving capability and half-select-free operation for the 32 nm technology node. The proposed design aims to mitigate half-select disturb issues by separating the read and write paths and implementing a bit-interleaved structure. This approach enhances stability, write-ability, and read reliability under concurrent access conditions. Simulation results showed improved static noise margin, enhanced read/write performance, and reduced power dissipation, indicating that the cell is well-suited for low-power and high-density SRAM applications in advanced CMOS technologies.

- **TFET-Based Robust 7T SRAM Cell for Low Power Application, 2019**

Sayeed Ahmad, Syed Afzal Ahmad, Mohd Muqeem, Naushad Alam, and Mohammad Hasan [1] proposed a novel 7-transistor (7T) SRAM cell utilizing Tunnel Field-Effect Transistors (TFETs) to achieve ultra-low power consumption. The design incorporates a dual-pocket double-gate TFET (DP-DGTFET) structure, enhancing drive current and reducing ambipolarity compared to conventional TFETs. This configuration improves read and write stability, achieving a significant increase in read static noise margin (RSNM) and write static noise margin (WSNM). Additionally, the proposed cell demonstrates reduced write delay and lower leakage power, making it suitable for energy-efficient memory applications in advanced CMOS technologies. Simulation results indicate that the DP-DGTFET-based 7T SRAM cell outperforms traditional 6T SRAM cells in terms of power consumption and stability metrics, highlighting its potential for low-power electronic devices.

- **A 2T1C Embedded DRAM Macro with No Boosted Supplies Featuring a 7TSRAM-Based Repair and a Cell Storage Monitor, 2012**

Ki Chul Chun, Wei Zhang, Pulkit Jain, and Chris H. Kim [21] introduced a logic-compatible embedded DRAM (eDRAM) macro that operates without the need for boosted supplies. The design utilizes a 2T1C gain cell comprising an asymmetric 2T cell and a coupling PMOS capacitor, ensuring proper operation even without a boosted supply by leveraging beneficial coupling for read and preferential boosting for write. To enhance reliability, a repair scheme based on a single-ended 7T SRAM is employed, featuring local differential write and shared control with the main 2T1C array. Additionally, a storage voltage monitor is proposed to track the retention characteristics of the gain cell eDRAM under process, voltage, and temperature (PVT) variations, allowing for adaptive adjustment of the refresh rate. A 128 kb eDRAM test chip implemented in a 65 nm low-power process operates at a random access frequency of 714 MHz with a static power dissipation of 161.8 µW per megabit for a 500 µs refresh rate at 1.1 V and 85°C.

- **Low Power and Robust 7T Dual-Vt SRAM Circuit, 2008**

S. A. Tawfik and V. Kursun [33] proposed a dual-threshold voltage (Vt) 7-transistor (7T) SRAM cell designed to enhance read stability and reduce leakage power consumption. The design employs a dual-Vt scheme, utilizing low-Vt transistors in critical paths to improve performance and high-Vt transistors in non-critical paths to reduce leakage. This approach effectively balances the trade-off between speed and power consumption. Simulation results demonstrate that the proposed 7T SRAM cell achieves improved read static noise margin (RSNM) and write static noise margin (WSNM) compared to conventional 6T SRAM cells, while also reducing leakage power. The design is suitable for low-power applications requiring high data stability and reduced leakage currents.

- **A 32-nm Subthreshold 7T SRAM Bit Cell with Read Assist, 2017**

S. Gupta, K. Gupta, and N. Pandey [22] proposed a 7-transistor (7T) SRAM cell optimized for subthreshold operation at the 32 nm technology node. The design addresses the limitations of conventional 6T SRAM cells, which suffer from read-write conflicts and degraded performance at low supply voltages. The proposed 7T cell incorporates a read-assist mechanism to enhance read stability and performance in the subthreshold region, operating reliably down to 0.4 V. This architecture achieves improved dynamic write ability and reduces power consumption by lowering the data retention voltage. The cell occupies an area of 0.254 μm^2 per bit, making it suitable for low-power and area-constrained applications.

- **Power-Aware Source Feedback Single-Ended 7T SRAM Cell at Nanoscale Regime, 2017**

C. Roy and A. Islam [23] proposed a low-power and highly stable single-ended 7-transistor (SE7T) SRAM cell incorporating a source feedback mechanism. This design aims to address the challenges of increased leakage power and reduced stability in nanoscale CMOS technologies. By introducing a source feedback transistor, the cell enhances read stability and write ability without significantly increasing the area. Monte Carlo simulations demonstrate that the proposed SE7T SRAM cell achieves improved static noise margins and reduced leakage power compared to conventional 6T and 7T SRAM cells. These characteristics make it a promising candidate for low-power and reliable memory applications in advanced CMOS technologies.

- **A Stable 2-Port SRAM Cell Design Against Simultaneously Read/Write-Disturbed Accesses, 2008**

Suzuki et al. [24] addressed the critical challenge of maintaining stability in 2-port SRAM cells during simultaneous read and write operations, which can lead to read/write-disturbed accesses and compromise data integrity. To mitigate this issue, the authors proposed an innovative cell biasing technique that controls the cell's ground level (VSSM) using a dual-V_{DD} approach combined with a reduced write bit-line (WBL) precharge scheme. This design was implemented in an 8-transistor (8T) 2-port SRAM cell using 65 nm CMOS technology.

- **Schmitt Trigger-Based Single-Ended 7T SRAM Cell for Internet of Things (IoT) Applications, 2018**

Sanapala, Sakthivel, and Yeo [25] proposed a Schmitt trigger-based single-ended 7T SRAM cell specifically designed for ultra-low voltage (ULV) applications in the Internet of Things (IoT) domain. The design employs a Schmitt trigger inverter to improve noise immunity and incorporates dynamic body biasing to optimize threshold voltages under varying conditions. Operating at 0.3 V using 45 nm CMOS technology, the cell demonstrates enhanced read static noise margin (RSNM), achieving over 22% improvement compared to conventional 6T, 7T, 8T, and 11T SRAM designs. Furthermore, the proposed cell exhibits more than 44% and 63% reductions in write and read energy consumption, respectively. Its single-ended architecture allows for energy-efficient operation while maintaining stability across different process, voltage, and temperature (PVT) variations. The authors also introduced a new performance evaluation metric, SNM per unit Area to Energy Ratio, with the proposed cell outperforming others in this regard, making it highly suitable for low-power and stable memory operations in IoT applications.

- **Single-Ended Boost-Less (SE-BL) 7T Process Tolerant SRAM Design in Sub-threshold Regime for Ultra-Low-Power Applications, 2016**

C. B. Kushwah, S. K. Vishvakarma, and D. Dwivedi [26] introduced a novel 7-transistor (7T) SRAM cell architecture, termed Single-Ended Boost-Less (SE-BL), tailored for ultra-low-power applications operating in the sub-threshold regime. This design eliminates the need for boosted supply voltages, thereby reducing power consumption and simplifying the power delivery network. The SE-BL SRAM cell employs a single-ended read/write mechanism, which not only conserves energy but also enhances read stability and write ability. Comprehensive simulations demonstrate that the SE-BL design exhibits superior performance metrics, including reduced read power consumption and lower standard deviation in read access times, compared to conventional SRAM cells. These attributes make the SE-BL 7T SRAM cell a promising candidate for energy-efficient memory solutions in nanoscale technologies, particularly for applications where power efficiency is paramount.

- **Single Bit Line Accessed High-Performance Ultra-Low Voltage Operating 7T SRAM Bit Cell with Improved Read Stability, 2021**

B. Rawat and P. Mittal proposed a 7-transistor (7T) static random-access memory (SRAM) bit cell designed for ultra-low voltage operation, specifically at 300 mV, using a 32 nm technology node. The design utilizes a single bit-line for both read and write operations, which simplifies the peripheral circuitry and reduces the activity factor during memory access. This single-ended architecture contributes to lower power consumption and improved energy efficiency.

- **Single Bit-Line 7T SRAM Cell for Near-Threshold Voltage Operation with Enhanced Performance and Energy in 14nm FinFET Technology, 2016**

Y. Yang, H. Jeong, Seung Chul Song, Joseph Wang, Geoffrey Yeap, and Seong-Ook Jung [27] introduced a 7-transistor (7T) SRAM cell optimized for near-threshold voltage (NTV) operation, implemented in 14 nm FinFET technology. The design employs a single bit-line for both read and write operations, simplifying the peripheral circuitry and reducing power consumption. A key innovation is the disconnection of the read path from the internal storage

nodes, effectively eliminating read disturbances and enhancing read stability. This architecture allows for reliable operation at reduced supply voltages, achieving significant improvements in energy efficiency and performance. The proposed cell demonstrates enhanced static noise margins and reduced variability, making it highly suitable for low-power applications in advanced technology node.

2.2 RESEARCH GAP

Over the years, 7T SRAM cells have emerged as strong candidates for ultra-low-power and high-stability memory design in advanced CMOS and emerging device technologies. The reviewed literature spans a broad spectrum, including performance enhancement techniques (Rawat et al., 2021), security features (Giterman et al., 2019), low-voltage operation (Ansari et al., 2015; Asli & Taghipour, 2017), FinFET integration, and novel device-level technologies like TFETs (Ahmad et al., 2019) and HETTs (Lee et al., 2013). Despite these advancements, several significant research gaps remain.

Firstly, power and energy efficiency continue to be major challenges. While several designs introduce single-ended access (e.g., Yang et al., 2016; Kushwah et al., 2016) and boosted-less architectures to reduce dynamic and leakage power, these often suffer from trade-offs such as reduced read/write speed or increased area overhead. The integration of energy-efficient features like power gating (as in Chun et al., 2012) still lacks universal compatibility across multiple operating regimes. There remains a need for standardized, scalable methods to achieve consistent energy reductions in both active and standby modes without degrading performance.

Secondly, stability under near-threshold and sub-threshold operation is another open area. Near-threshold designs (e.g., Oh et al., 2021; Sanapala & Yeo, 2018) show promise but often struggle to simultaneously maintain high read/write margins and low latency. Read-disturb issues are partially addressed through decoupling techniques and read-assist circuits, but in many cases, this increases complexity or adds transistors, affecting area and yield. Techniques such as Schmitt Trigger integration (Sanapala & Yeo, 2018) or security-focused cell layouts (Giterman et al., 2019) provide local improvements, but a holistic approach that balances speed, energy, and robustness under voltage scaling is still missing.

Thirdly, process variation and technology scaling pose enduring challenges. Designs in sub-32nm nodes (e.g., Gupta et al., 2017; Rawat & Mittal, 2021) are heavily impacted by

threshold voltage fluctuations and manufacturing inconsistencies. Though some cells use dual-Vt strategies (Tawfik & Kursun, 2008) or FinFET architectures (Ansari et al., 2015) to address these, variation-aware assist schemes and adaptive body biasing remain underexplored for the 7T topology.

Fourth, device-level innovation using emerging technologies like TFETs and HETTs (Ahmad et al., 2019; Lee et al., 2013) presents new opportunities but also introduces new issues. While such devices promise steep subthreshold swings and low leakage, they often suffer from limited current drive, leading to write failures or increased delay. Moreover, the circuit-compatibility and variability of these novel devices under practical conditions are not yet fully understood.

Finally, scalability and integration into large memory arrays is another underdeveloped area. Though several papers focus on individual cell behavior and bit-level performance, few explore how these designs behave at macro-scale integration. Problems such as half-select disturbance (Suzuki et al., 2008), bit-interleaving complexity (Oh et al., 2021), and write-line contention are yet to be fully addressed. Integration with repairability features (Chun et al., 2012) and peripheral circuit co-design is an avenue still requiring deeper exploration.

CHAPTER 3
CHARACTERISTIC COMPARISON FOR DIFFERENT 7TSRAM CELLS

The performance and characteristics of 7T SRAM cells vary depending on the specific design, process node, and application requirements. However, 7T SRAM cells are generally designed to offer improvements over conventional 6T cells by addressing limitations in power consumption, stability, and leakage. The key modification in a 7T SRAM cell is the addition of a seventh transistor, typically used to decouple the read path from the storage nodes. This enhances read stability by preventing read disturbance. Additionally, single-ended or gated write mechanisms are often employed to reduce dynamic power during write operations. The 7T SRAM cell tends to offer better read stability and lower power consumption compared to the traditional 6T cell, albeit at the cost of a slight area overhead. Because it typically has only one bit line and more complex control logic, write speed can be slightly lower in some implementations. Overall, 7T SRAM cells are especially suitable for low-power and sub-threshold applications where stability and energy efficiency are more critical than access speed.

The 7T SRAM cell includes an additional transistor compared to the standard 6T design, which introduces some complexity and a slight impact on write speed. This extra transistor mainly serves to decouple the read path from the storage nodes, significantly improving read stability by reducing read disturbances common in 6T cells. While the write speed can be somewhat slower due to single-ended write operations, the 7T cell benefits from lower power consumption through reduced leakage currents and selective bit line switching. Although the added transistor increases the silicon area slightly, this trade-off is justified by enhanced stability and improved energy efficiency, making 7T SRAM cells suitable for low-power and sub-threshold applications.

This chapter is organized into seven sections. The first section (3.1) provides an overview of SRAM cells, discussing conventional 7T SRAM cells alongside the proposed 8T SRAM cell. The second section (3.2) details the dimensions of all the cells, highlighting the technology node used and the differing sizes of pull-down, pull-up, and access transistors. Section 3.3 focuses on transient analysis, evaluating the dynamic behavior of the SRAM cells during read and write operations. The fourth section (3.4) addresses data stability,

presenting butterfly curves for HSNM, RSNM, and WSNM to assess noise robustness and ensure reliable functioning. The fifth section (3.5) compares the power consumption of each cell. Finally, the sixth section (3.6) analyzes and compares the read and write delays of the cells.

3.1 OVERVIEW OF SRAM CELLS

SRAM cells are a kind of semiconductor memory commonly used in computers, microprocessors, and various digital electronics. Unlike dynamic RAM (DRAM), which needs constant refreshing to maintain data, SRAM holds information as long as it receives power. SRAM is recognized for its quick access speeds, low energy use, and ability to retain data without needing to be refreshed continuously.

An SRAM cell usually comprises transistors organized in a flip-flop structure. A concise summary of its components and how it operates is shown below:

a) Cross-Coupled Inverter Pair: At the core of an SRAM cell are two cross-coupled inverters that create a flip-flop. Each inverter is made up of a PMOS (P-channel Metal-Oxide-Semiconductor) transistor and an NMOS (N-channel Metal-Oxide-Semiconductor) transistor.

b) Bitlines: The flip-flop is linked to two bitlines, called the "bitline" and the "bitline bar" (its complement). These bitlines facilitate reading from and writing data to the SRAM cell.

c) Wordlines: The wordline controls access to the SRAM cell. When activated, it allows data to be transferred between the bitlines and the flip-flop.

d) Access Transistors: Access transistors are key components of SRAM, widely used for fast, volatile data storage in electronic devices. They act as switches controlling the connection between storage nodes and bitlines, enabling reading and writing of data. During a read operation, access transistors link the stored data to the bitlines so voltage levels can be sensed. In a write operation, they provide a path for current to update the storage nodes. These transistors are designed for rapid switching and low leakage, ensuring reliable and efficient data access.

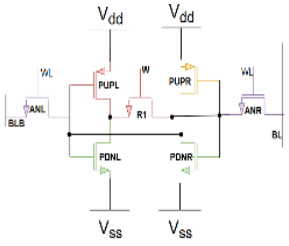
SRAM cells are arranged in arrays to form larger memory banks. The cell size depends on the technology node and design needs—smaller cells increase memory density but may raise challenges in power use and stability. Due to their fast and efficient random access, SRAM cells are ideal for cache memory, register files, and other speed-critical, low-power application.

3.2 Different 7T SRAM cells

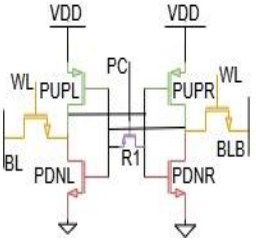
Various 7T SRAM Architectural Configurations" examines many 7-transistor (7T) Static Random-Access Memory (SRAM) cell designs optimized for enhanced stability, performance, and power efficiency in modern electronic systems. This configuration aims to solve critical concerns such as leakage currents, read stability, and write access times. 7T SRAM architectures exhibit greater resilience to noise and unpredictability compared to conventional 6T systems because to their utilization of more transistors, making them suitable for low-power, high-speed applications. This paper provides a comparative analysis of SRAM configurations to aid designers in selecting optimal designs for certain applications, highlighting trade-offs in space, energy consumption and reliability.

3.2.1 Differential Ended and Differential Port

The transistor-level circuit for a differential-ended, single-port 7T cell (7TDEDPA) reported by Aly and Bayoumi in 2007 [6]. It uses an inverter pair (PUPL-PDNL, PUPR-PDNR) with an NMOS transistor (R1) controlled by signal W to enable write operation by connecting/disconnecting the feedback. The cell supports differential read and single-ended write operations.



(a)



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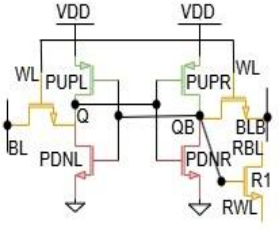

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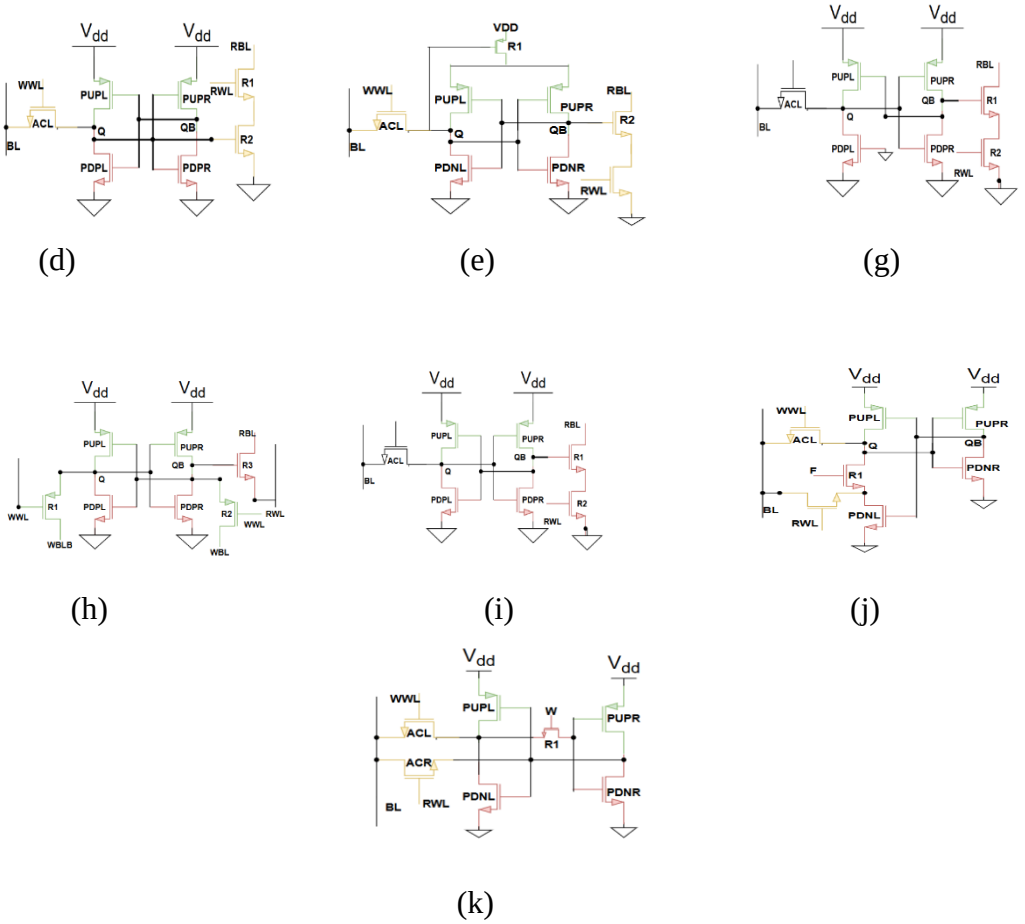


Fig. 3.1 Schematic Diagram For (a)7TDESPA, (b)7TDESPGi, (c)7TDEDPL, (d)7TDEDPC, (e)7TSEDPT, (f)7TSEDPG, (g)7TSEDPR, (h)7TSEDPS, (i)7TSESPK, (j)7TSESPRt

The 7TDESPGi bit cell, proposed by Giterman et al. (2018), features a PMOS transistor (R1) controlled by the EQ signal for equalization during write operations [8]. The write process has two stages: removing VDD and activating R1 for voltage equalization and charge sharing, reducing power usage, followed by activating access transistors (ACL and ACR) to complete the write.

3.2.2 Differential Ended 7T SRAM Bit Cell with the Isolated Read Port

In 2017, Liu et al. introduced asymmetric 7T SRAM (7TDEDPL) with an additional read port linked to the QB node via NMOS transistor R1 [9]. This design improves read stabilization but reduces drive current, impacting write performance. The read process involves QB enabling RBL discharge through R1 to the RWL.

In 2012, Chun et al. introduced the 7TDEDPC [10] bit cell using PMOS transistors as access transistors to reduce write power losses. However, PMOS requires a negative bias voltage,

increasing variability and silicon area due to the large charge pump, making PMOS access transistors less favourable for practical applications

3.2.3 Single-Ended Dual Port 7T SRAM Bit Cells

In light of the increasing need for portable devices, the ability to integrate circuits with ultra-low power is a major focus. Therefore, it has now become critical to cut back on both active power and leakage power. Two key methods of power minimization are: (1) The supply voltage (VDD) is decreased, which has a squared effect on the active power, and (2) The activity factor is reduced; hence, the dynamic power of the circuit is also reduced. The 7TSEDPT memory cell in Figure 1e uses a cross-coupled inverter pair with three HVTH and one LVTH MOS transistor. It suffers from reduced write performance due to single-ended write mechanisms [12]. Gupta et al. introduced the 7TSEDPG [13] cell in 2017, which features a dual-port architecture to resolve read-write conflicts and improve write stability at the cost of reduced read stability, requiring a read-assist circuit. In 2017, Roy et al. proposed the 7TSEDPR [14] bit cell, optimizing dynamic power by reducing bit-line activity. Its isolated read path with PMOS (R2) and NMOS (R3) en-hances stability and resists soft errors. Supply feedback lowers write power, but the negatively biased PMOS requires a charge pump, increasing silicon area. In 2008, Suzuki et al. introduced the 7TSEDPS SRAM bit cell, which shares a similar architectural design to the 7TSEDPT bit cell [12]. Figure 1h illustrates the transistor-level schematic of the 7TSEDPS [16] design. How-ever, a key drawback of this approach is its challenge in maintaining strong write ability for logic ‘1’ due to using a pass-transistor-based single-ended port.

3.2.4 Single-Ended Single Port 7T SRAM Bit Cell

In some cases, the main goal of the circuit design is to economize cost, and parallelism is not the aim. Then, using a multi-port bit cell will only increase the area and the power overheads. In such a case, the single-ended, single port bit cell is more effective due to the reasons: (1) the on-chip area is smaller, (2) there is less activity factor, and (3) less circuit capacitance, which in turn reduces the total power dissipation, of the cell. In 2015, Kushwah et al. introduced the 7TSESPK [17] SRAM cell with a single bit-line and feedback disconnection for improved write ability. Controlled by WWL and NMOS transistors, it features a cross-coupled inverter core. However, disconnecting the left inverter causes the Q node to float, increasing susceptibility to write errors and disturbances. In 2021, Rawat and Mittal

introduced the 7TSESPRt [18] cell with a single-ended, single-port topology. Its core uses coupled inverters with an NMOS transistor (R1) to disconnect feedback. Access transistors (ACR, ACW) manage read/write operations. Despite its design, 7TRt is prone to read errors due to read current discharging through the data node.

3.3 CELL SIZING

The table presents the transistor sizing (in nm) for various 7T SRAM cell designs categorized by their configurations: Differential-Ended Single Port (DE-SP), Differential-Ended Dual Port (DE-DP), and Single-Ended Single Port (SE-SP). Each cell is labeled (e.g., 7TDESPA, 7TSESPK), and key transistors are sized: pull-up (PUPL/PUPR), pull-down (PDNL/PDNR), and access transistors (ANL/ANR/ANW). Some cells include additional transistors (R1, R2) for enhanced read stability or write performance. For instance, the 7TDESPGi cell uses larger ANL and ANR to improve access, while the 7TSESPK features a wide write-access transistor (ANW = 480 nm), optimizing write ability. Missing values (indicated as "----") reflect design simplifications or inactive paths. The variation in transistor sizing across cells indicates targeted optimizations for read stability, write ability, and power efficiency, depending on application needs. Overall, this table supports comparative analysis of 7T SRAM topologies to guide design decisions in low-power and high-performance memory applications.

Table 3.1 Dimension of Various 7T SRAM cells

SRAM CELLS		PUPL	PDNL	PUPR	PDNR	ANL	ANR	ANW	R1	R2
DE-DP	7TDESPA	120	310	120	395	240	120	----	240	----
	7TDESPGi	120	240	120	240	480	240	----	120	----
DE-SP	7TDEDPL	120	310	120	180	480	240	----	240	----
	7TDEDPC	120	310	120	240	----	----	----	240	240
SE-DP	7TSESPT	120	180	180	180	480	----	----	240	240
	7TSESPR	120	240	120	240	180	----	----	120	240
	7TSESPS	120	310	120	180	366	----	----	240	240
	7TSESPSa	120	180	120	180	240	240	----	240	----
SE-SP	7TSESPK	120	310	360	240		240	480	120	----
	7TSESPY	120	180	120	180	180	----	----	120	120

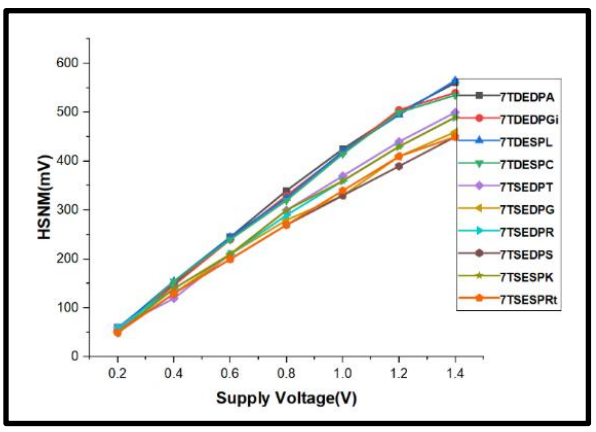
3.4 TRANSIENT ANALYSIS

To verify the correct execution of hold, read, and write operations, transient (time-domain) simulations were carried out on all three SRAM models. The simulations utilized consistent read/write control signals, uniform input data patterns, and identical precharge signals for both read and write bitlines. This uniformity ensured a fair basis for comparison. Moreover, the same sense amplifiers, precharge circuits, and write drivers were integrated across all models to guarantee the reliability and consistency of the performance evaluation. The simulation outcomes are illustrated in Fig. 3.5.

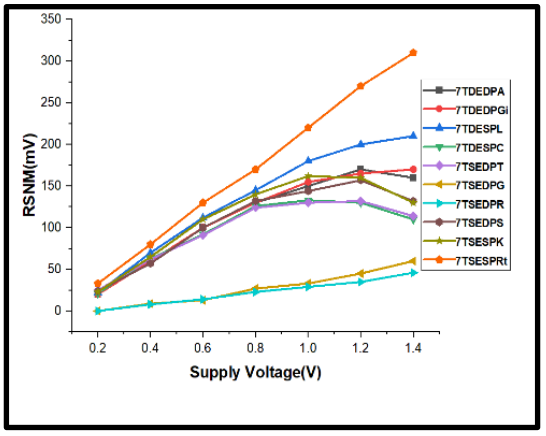
Transient analysis is essential for evaluating the dynamic behavior of SRAM cells during memory operations. During a read operation, it examines the voltage and current transitions that occur when the stored data is accessed. It accounts for factors such as the switching dynamics of access transistors, the bitline voltage levels, and the capacitive loading of the internal storage nodes. By studying these responses, one can accurately determine the read access time, which is the interval required for the data to stabilize on the bitlines and be correctly detected by the sense amplifier.

3.4.1 Supply Voltage Scaling

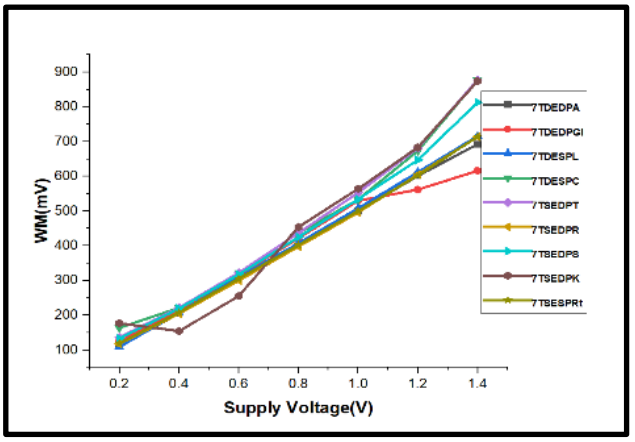
This study compares ten 7T SRAM designs by analysing their stability and noise margins for hold, read, and write operations as the supply voltage increases from 0.2V to 1.4V. For HSNM (Hold Static Noise Margin), all designs show improved stability as the voltage increases. 7TDEDPA performs the best with the highest HSNM, meaning it has excellent hold stability, while 7TSESPRt has the lowest, indicating weaker performance as shown in figure 2(a). At lower voltages (up to 0.8V), all designs perform similarly, but the differences become clear as the voltage rises.



(a)



(b)



(c)

Fig. 3.2 Graphical comparison for various 7TSRAM Cells (*a*) HSNM, (*b*) RSNM and (c)WM for all different 7T SRAM bit cells for supply voltage varying from 0.2 V to 1.4 V

For RSNM (Read Static Noise Margin), which measures read stability, 7TSESPRt achieves the highest RSNM (~320 mV) as shown in figure 2(b), showing the best-read stability, while 7TSEDPR and 7TSESPK perform the worst, staying below 75 mV. Designs like 7TDEDPA and 7TDESPL perform moderately. Lastly, for WM (Write Margin) as shown in figure 2(b), all designs improve as the voltage increases, but 7TSEDPK performs the best, with its WM reaching over 900 mV at 1.4V, showing excellent write stability as shown in figure 2(c). Moderate performers like 7TDEDPA and 7TDESPL reach 700–800 mV, while 7TSESPRt and 7TDEDPGi have lower WM values. Overall, the results show how stability and performance change with supply voltage, helping identify the best designs for hold, read, and write operations.

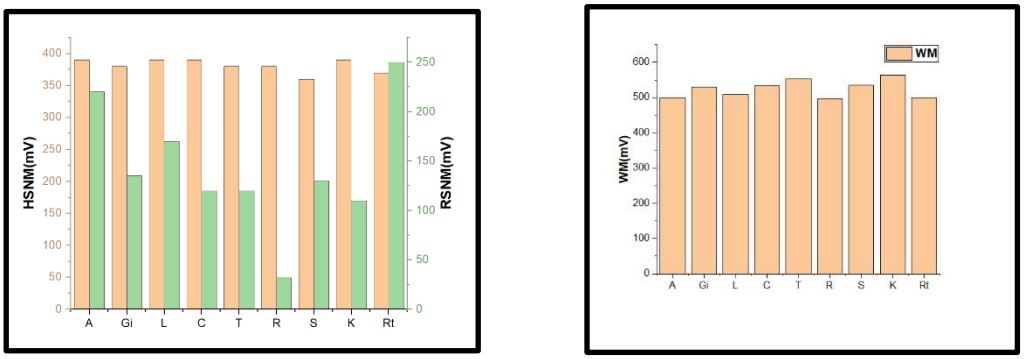
3.4.2 Stability Analysis

The analysis revolves around the HSNM (Hold Static Noise Margin) and RSNM (Read Static Noise Margin) values for different 7T SRAM cells, where the notations A, Gi, L, C, T, R, S, K, and Rt correspond to 7TDESPA, 7TDESPGi, 7TDEDPL, 7TDEDPC, 7TSESPT, 7TSESPR, 7TSESPS, 7TSESPK, and 7TSESPRt, respectively.

3.4.2.1 HSNM Analysis

The HSNM values remain fairly consistent across all SRAM designs, primarily ranging between 360–390 mV, demonstrating strong stability in the hold state. Specifically, cells A (7TDESPA), L (7TDEDPL), C (7TDEDPC), and K (7TSESPK) achieve the highest HSNM values of 390 mV as shown in figure 3(a), which indicates excellent hold stability under

voltage stress. Cells Gi (7TDESPGi), T (7TSESPT), R (7TSESPR) exhibit slightly lower HSNM values at 380 mV, while the cell S (7TSESPS) stands out with a slightly reduced value of 360 mV, which still ensures solid hold performance. The cell Rt (7TSESPRt) shows a marginally lower HSNM of 370 mV, but this reduction is negligible considering its strong read stability, as discussed below.



(a) (b)

Fig. 3.3 Comparison of (a)HSNM and RSNM (b) WM for various 7T SRAM cells

Table 3.2 HSNM/RSNM at Voltage for Various 7TSRAM Cells

	A	Gi	L	C	T	R	S	K
HSNM	390	380	390	390	380	380	390	370
RSNM	135	170	120	120	32	220	135	250

3.4.2.2 RSNM Analysis

The RSNM values show that read stability is highly dependent on the structure of the SRAM cell. The Rt (7TSESPRt) cell tops with an excellent 250 mV RSNM outperform the rest in read stability and are, therefore, highly effective for applications requiring frequent reads. The R (7TSESPR) cell performs abysmally, with a worrisome 32 mV RSNM, thus signaling critical read instability issues. Cells like Gi(7TDESPGi) and C (7TDEDPC) demonstrate values of 135mV and 120 mV, which are vulnerable to read noise. Moderate performance cells include L(7TDEDPL) at 170 mV, T (7TSESPT) at 120 mV, and S (7TSESPS) at 130 mV. In summary, they are reasonable stability cells but need further optimizations. A (7TDESPA) and K (7TSESPK) achieve fairly good stability, with RSNM values of 220 mV and 110 mV, and are suitable for balanced use. Overall, Rt presents excellent stability, whereas cells like R and C are exposed to major stability challenges.

The comparison reveals that HSNM is high and consistent for all designs of SRAM, with strong hold stability of standby modes. RSNM is very different with respect to which design

structure holds the key to achieving read stability. The Rt 7TSESPRt cell has an outstanding RSNM of 250 mV, representing the most balanced and reliable design for applications that demand hold and read stability. Conversely, the R (7TSESPR) cell is weak, with a 32 mV RSNM, indicating significant read instability issues. Other designs like Gi, C, and K also have relatively low RSNM values and must be optimized to improve their read performance. HSNM is still very strong, but deficiencies in RSNM of the weaker designs R, Gi, and C must be addressed. Overall, the Rt (7TSESPRt) cell is the winner, offering the best balance of stability and reliability.

3.5 Timing Analysis

The timing analysis of nine 7T SRAM cells, as shown in Figure (4), reveals wide variations in Read Access Time and write access times. For Read Access Time, S (7TSEDPS) leads with an impressive time of 11.56ps, followed closely by K (7TSESPK) at 13.30ps, indicating superior read efficiency. The Gi (7TDEDPGi) cell also performs well with a time of 43.65 ps. In contrast, Rt (7TSESPRt) records the slowest read time of 106.9 ps, making it the least efficient for read operations. For Write 0 Access Time, A (7TDEDPA) stands out as the best performer with a time of 58.7ps, followed by Gi (7TDEDPGi) at 80.69ps, showing good efficiency. However, L (7TDESPL) and Rt (7TSESPRt) struggle, with times of 414.5ps and 326.6ps, respectively, reflecting inefficiencies in their write mechanisms. Regarding Write 1 Access Time, Gi (7TDEDPGi) again delivers the best performance with a time of 73.28ps, highlighting its efficiency in handling write operations. Cells C (7TDESPC) and T (7TSEDPT) achieve reasonable times of 127.3ps and 291.6ps, respectively. On the other hand, Rt (7TSESPRt) records the slowest Write 1 time at 996.8ps, followed by L (7TDESPL) at 451.2ps, further indicating poor write performance. Overall, the analysis identifies S (7TSEDPS), K (7TSESPK), and Gi (7TDEDPGi) as the strongest performers across specific timing metrics, while Rt (7TSESPRt) consistently underperforms, particularly in read and write operation.

Table 3.3 Timing Analysis of Read and Write Access time

	A	Gi	L	C	T	G	R	S	K	Rt
Read Access Time (ps)	60.6	43.65	58.12	47.52	21.11	64.01	52.70	11.56	13.30	106.9
Write0 Access Time (ps)	58.7	80.69	414.5	135.7	140.4	137.7	163.6	139.2	44.72	326.6
Write1 Access Time (ps)	192.3	73.28	451.2	127.3	291.6	801.5	299.6	150.2	604.8	996.8

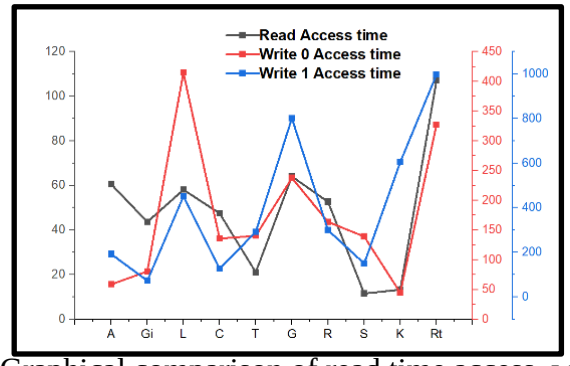


Fig. 3.4 Graphical comparison of read time access, write 0 time access, and write 1 time access

3.6 Power Consumption Analysis

A bar chart and table highlight the dynamic (nW) and static (pW) power usage of different cells, with dynamic power shown on the left axis and static power on the right. Cells 7TDESPGi and 7TDESPA stand out for their high dynamic power consumption of roughly 1024nW and 981.3nW, alongside static power values of 31.03pW and 10.65pW. Conversely, 7TDESPR consumes the least dynamic power (223.68 nW) and has the lowest static power (6.538 pW). An interesting outlier is 7TSEDPS, which demonstrates high static power consumption (92.30 pW) despite its moderate dynamic power level of 460.69 nW.

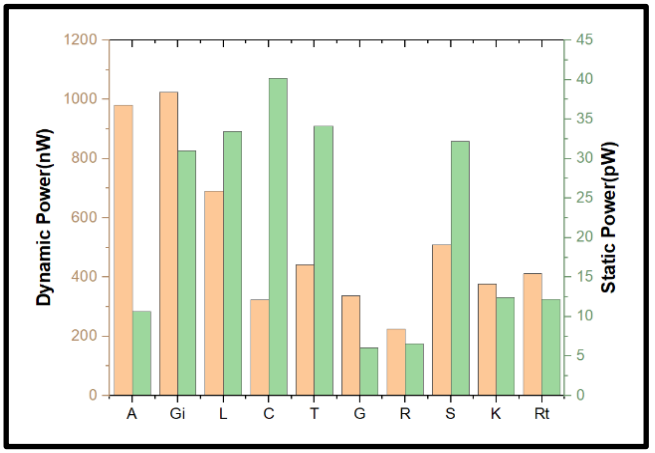


Fig. 3.5 Graphical comparison of static power and dynamic power

Table 1.4 A. Static and Dynamic Power for Various 7TSRAM Cells

	A	Gi	L	C	T	G	R	S	K	Rt
Dynamic Power (nW)	981.3	1024	690.6	323.4	419.2	337.2	223.6	460.6	376	411.7
Static Power (pW)	10.65	31.03	33.44	40.2	34.14	6.076	6.538	92.30	12.39	12.17

3.7 IMPORTANT RESULTS

This chapter provides a thorough analysis of various well-established 7T SRAM cell architectures, which form the foundation for the development of the proposed 8T SRAM cell. The key insights and conclusions drawn from this study are as follows:

- The SRAM cell architectures developed previously by researchers, including various 7T SRAM cells, were individually simulated using the Cadence Virtuoso tool to perform an in-depth evaluation.
- The analysis involved a detailed understanding of their operation and quantification of their performance parameters based on simulation results. For example, butterfly curves were used to determine Static Noise Margins (SNM), while transient analysis waveforms helped assess read and write operations and calculate corresponding access delays. Among the 7T cells, some showed strong read and write performance, while others demonstrated better noise immunity. However, certain 7T architectures exhibited relatively higher power dissipation.
- Furthermore, the design limitations and complexities of each architecture were examined to understand the motivations behind newer SRAM designs. These insights laid the groundwork for proposing the 8T SRAM cell, which addresses several of the observed drawbacks by improving power efficiency and noise margins, albeit with a slightly increased write access time.

CHAPTER 4

PROPOSED 8T SRAM CELL

The design and analysis of a low-power and high-performance 8T SRAM cell focus on enhancing the cell architecture to achieve reduced power consumption and improved stability during read and write operations. The 8T SRAM cell employs a decoupled read path by incorporating additional transistors, which helps isolate the internal storage nodes from the read operation. This separation minimizes read disturbance and improves read stability compared to conventional 6T SRAM cells, while also enabling better performance and reduced power dissipation in low-voltage applications.

The design focuses on minimizing power dissipation in the 8T SRAM cell by carefully sizing the transistors and optimizing voltage levels for read and write operations. The use of a decoupled read path enhances read stability and allows for lower power consumption during read access. Furthermore, techniques such as power gating, leakage current suppression, and adaptive biasing are incorporated to improve overall power efficiency. Through comprehensive simulations, analysis, and performance evaluation, the low-power and high-performance 8T SRAM cell exhibits enhanced read stability, reduced dynamic and static power consumption, and sufficient noise margins, making it well-suited for low-power and high-speed memory applications.

This chapter is divided into six sections. The first section (4.1) provides a detailed description of the proposed SRAM cell design. The second section (4.2) outlines the dimensions of the proposed cell, emphasizing the technology node used and the sizes of the pull-down, pull-up, and access transistors. Section 4.3 presents transient analysis to evaluate the cell's behavior during dynamic operations like read and write. The fourth section (4.4) focuses on data stability, showcasing butterfly curves for HSNM, RSNM, and WSNM to assess noise resilience and ensure reliable performance. The fifth section (4.5) discusses Monte Carlo analysis, which is essential for evaluating the cell's performance and reliability under process variations.

4.1 ARCHITECTURE PROPOSED 8T CELL

As technology nodes decrease in size, power consumption per bit cell has emerged as a crucial consideration. This scaling intensifies the intrinsic read–write conflict in SRAM bit cells, resulting in diminished read and write performance. This paper proposes a single-ended dual-port architecture to tackle these problems and improve bit cell performance in scaled technology nodes. This architecture has supplementary benefits, including less silicon area, which decreases cost, and expedited write operations. After a comprehensive evaluation, it was determined that dual-port cells are the most efficient in alleviating the intrinsic read–write conflict inside the bit cell. The suggested design has a single-ended dual-port configuration. The stability of the data core markedly enhanced with the use of a mutually connected inverter pair design. It was noted that the single-ended cross-coupled inverter pair had inadequate write margin. The problem was rectified by converting the data core into a cascaded inverter design, hence optimizing the write margin. To facilitate this change, transistor R1 was included into the inverter core, enabling the transition from a mutually linked to a cascaded inverter architecture of contrast to traditional cells, the write assist mechanism of the 7TP cell does not rely on bit-line discharge during write operations. It depends only on voltage levels instead of current flow. During the write operation, the inverse of the data to be written is applied to the WBL signal. For example, when a '1' is to be recorded, the WBL signal is configured to '0,' and conversely. To accomplish this, a conventional single-ended write driver is used, succeeded by an inverter to guarantee that the complement of the desired data is applied to the WBL signal.

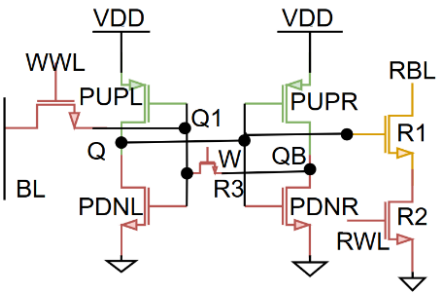


Fig 4.1 Schematic of Proposed 8T SRAM cell

Prior to a write operation, the suggested 8T SRAM cell requires that the feedback link between the two inverters, inv1 and inv2, be shut off. An additional NMOS transistor R3

is used to link and detach the feedback. The proposed architecture is shown in below figure. The circuit consist of the two back to back invertor inv1 and inv2 followed by a feedback control transistor. Here is different input signal is provided the different mode of operation of this proposed circuit is explained below in detail.

4.2 DIMENSIONS IN THE PROPOSED CELL

The size specifications of an SRAM cell pertain to the physical dimensions and structural layout of each memory unit. Generally, an SRAM cell is composed of multiple transistors, typically MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). The geometric attributes of these transistors including channel length, width, and additional spatial parameters determine the complete footprint of the cell. These physical properties are vital, as they influence aspects such as silicon area, energy consumption, data access latency, and noise tolerance. Reducing the physical scale of an SRAM cell increases memory packing density but also introduces difficulties in terms of energy efficiency, operational stability, and fabrication success rates. Thus, meticulous tuning of the transistor dimensions is crucial to maintain a balance among speed, compactness, and functional robustness in SRAM architecture.

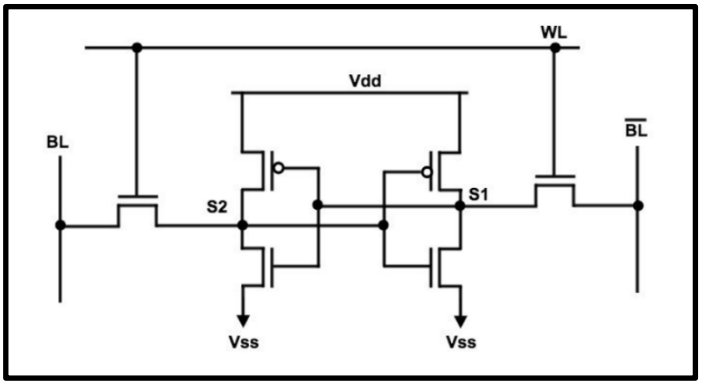


Fig. 4.2 A conventional 6T cell illustrating SRAM sizing

The Cadence Virtuoso platform was utilized to carry out simulations by designing schematics of the proposed SRAM cells for comparative analysis. Table 4.1 presents the dimensional specifications of the proposed 8T cell.

TABLE 4.1 Dimensions for Proposed 8T cell

	Width (W)	Length (L)
PUPL, PUPR (Pull-Up Transistors)	120n, 120n	45n
PDNL, PDNR (Pull-Down Transistors)	120n, 180n	45n
ATL, ATR	180n, 240n	45n
R1, R2(Isolated Read Port)	120n, 240n	45n

The dimensioning of pull-up, pull-down, and access transistors within an SRAM cell is a key factor influencing its operational efficiency, energy usage, and stability. Below is a concise summary of the critical considerations involved in appropriately sizing these transistors:

Pull-up Transistors: Pull-up transistors are tasked with elevating the stored data to a high logic level (logic '1'). Their sizing significantly impacts both the read and write performance of the SRAM cell. Increasing the size of pull-up transistors can enhance the speed of bit-line discharge during read operations and accelerate bit-line charging during writes. However, larger transistors result in greater silicon area usage and higher power dissipation. Therefore, the dimensions of pull-up transistors are carefully tuned to strike an optimal balance among speed, area compactness, and energy efficiency.

Pull-down Transistors: Pull-down transistors serve to drive the stored data to a low voltage level (logic '0'). Their sizing plays a critical role in defining the cell's stability and noise tolerance. Enlarged pull-down transistors strengthen the robustness of the logic '0' state and enhance resistance to noise-induced disturbances. However, increasing their size can result in higher power consumption and a larger cell footprint. Consequently, the dimensions of pull-down transistors are carefully optimized to maintain adequate noise margins while balancing the trade-offs among power efficiency and layout area.

Access Transistors: Access transistors facilitate read and write operations in the SRAM cell by linking the internal storage nodes to the bit lines. Their sizing significantly influences access latency, energy efficiency, and noise resilience. Smaller access transistors help minimize the cell footprint and lower power consumption, but they may degrade access speed and weaken noise immunity. In contrast, larger access transistors enable quicker data access and bolster noise margins, albeit at the expense of increased silicon area and power usage. Therefore, the sizing of access transistors is strategically optimized to satisfy performance and stability targets while accommodating area and energy constraints.

The dimensioning of pull-up, pull-down, and access transistors in an SRAM cell demands a careful balance among performance, power efficiency, operational stability, and area utilization. Achieving this balance involves evaluating the specific functional requirements of the target SRAM application and fine-tuning transistor sizes to optimize these often conflicting design parameters.

4.3 WORKING OF PROPOSED 8T SRAM CELL

This paper introduces a single-ended dual-port 8T SRAM cell optimized for advanced technology nodes. By addressing read–write conflicts and enhancing write margins through a cascaded inverter structure and feedback control mechanism, the design improves stability, reduces area and power consumption, and enables faster write operations compared to conventional SRAM architectures

4.3.1 Hold Operation

During the hold operation, the WWL (Write Word Line) signal remains low (yielding a high W), but the RWL and RBL signals are maintained at a high level. The access transistor ANW is rendered inactive owing to the dormancy of WWL. Simultaneously, transistor R1 remains engaged while the W signal is active, so maintaining the reciprocal feedback connection inside the inverter pair.

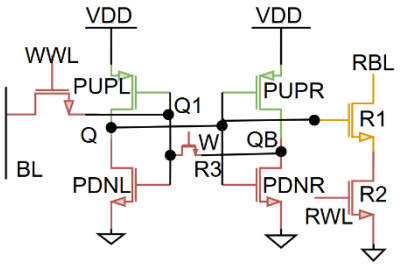
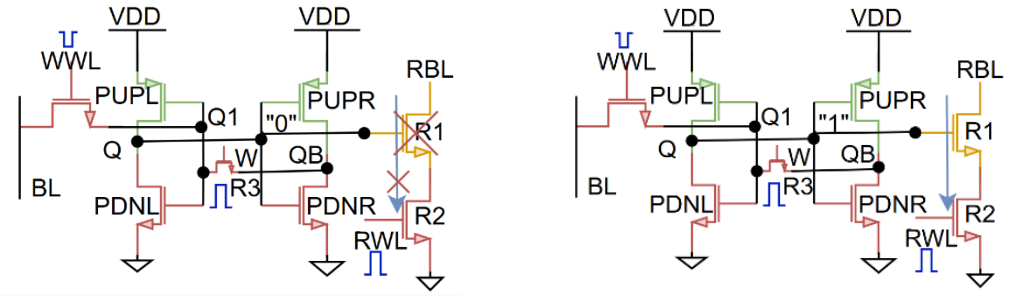


Fig. 4.3 Proposed 8T SRAM during Hold Operation

4.3.2 Read Operation

During the read operation, the WWL signal is maintained at a low level while the W and RWL signals are held high, resulting in transistor R2 being continuously activated during the read process, as seen in the figure. based on the value of QB. If QB is elevated, then transistor R1 is activated and RBL discharges to ground as shown in figure 4.3.2(b). If the QB is in a low state, the transistor R1 is off, and RBL does not discharge to ground. Both operations are shown in the figure 4.3.2.(a).

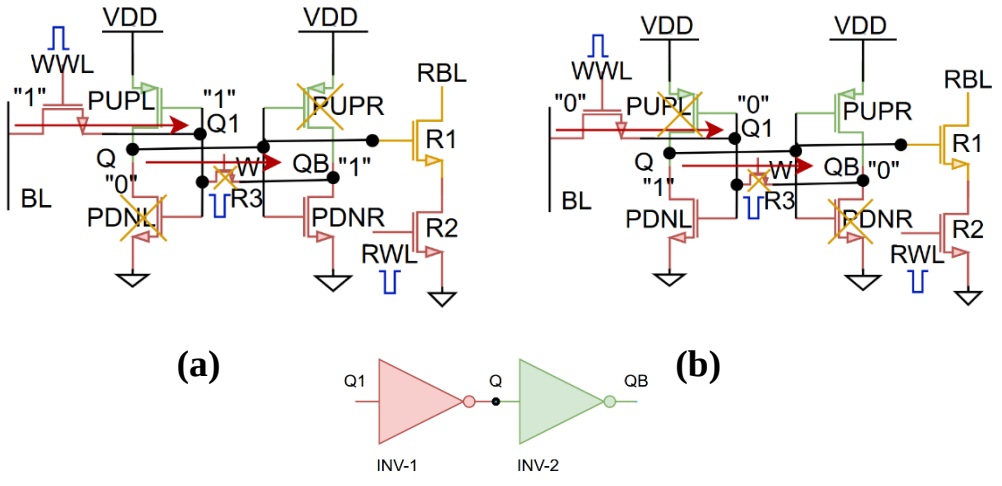


(a) **(b)**

Fig. 4.4 Proposed 8T SRAM (a) Read 0 and (B) Read 1 operation

4.3.3 Write Operation

To initiate the writing process, the feedback link (feedback control transistor) is deactivated by delivering a low signal to 'W'. Q transmits the inverse of the input data; Q1 is engaged while transistors R1 and R2 stay deactivated during the writing of '0', as seen in the figure. During the "0" write operation, the WWL signal is activated to a high state while the RWL signal remains in a low state.



(a) **(b)**

(c)

Fig. 4.5 Proposed 8T SRAM (a) Write 1 and (B) Write 0 operation

During the execution of the "1" write operation, the input data is applied to the node Q1 of inv1, resulting in the output of inv1 being the complement of the input data. The output of inv1 serves as the input data for inv2, and the result of inv2 is identical to the input data. When the signal "1" is written, WWL is elevated while RWL is diminished; concurrently, transistor R1 is in active mode and transistor R2 is in inactive mode.

4.4 TRANSIENT ANALYSIS

Transient The transient behavior of the proposed 8T SRAM cell is evaluated through a detailed simulation illustrating its operation during write, hold, and read cycles. As per the signal condition table and waveform, each mode is governed by the states of six control signals: W, WWL, WBL, RWL, RBL, and the internal nodes Q and QB.

Initially, during the Write ‘1’ operation (0–5 ns), the W signal is low, enabling write access. The WWL is high to activate the write word line, and WBL is set to logic ‘1’ to write data. The internal node Q transitions to a high voltage level, while QB settles at a low level, indicating successful storage of logic ‘1’. From 5–10 ns, the cell enters the Hold mode. In this state, WWL and RWL are kept low, disabling both read and write paths, and the stored value remains unchanged at Q = 1, QB = 0.

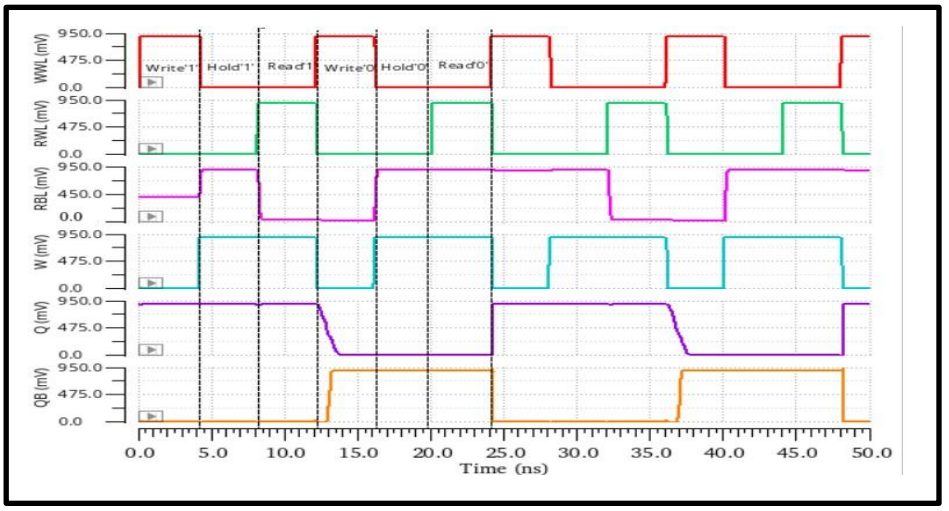


Fig. 4.6 Transient analysis of the Proposed 8T cell

In the next phase (10–15 ns), a Read ‘1’ operation is performed. Here, RWL is high, W remains high to disable writing, and RBL is pulled low. The data is sensed correctly without disturbing the stored value. Following this, another Write ‘0’ operation occurs from 15–20 ns, where WBL is pulled low, writing a logic ‘0’ into the cell. Consequently, Q transitions to low and QB to high, signifying a successful write.

Another Hold operation is observed from 20–25 ns, during which the values at Q and QB are retained. Finally, the Read ‘0’ operation (25–30 ns) accurately senses the stored logic ‘0’ without data corruption.

This analysis confirms that the proposed 8T SRAM cell reliably performs read and write operations while maintaining data integrity during hold phases, thanks to its enhanced dual-port architecture and controlled feedback mechanism.

Based on the results of the transient analysis, the proposed model successfully performs hold, read, and write operations. It is observed that when both the write enable and word line signals are active (high), the data present at input D is successfully written into the cell and appears at node Q. Conversely, when the word line and sense enable signals are both high, the cell enters the read mode, during which the stored value at Q is accurately transferred to the bit line, indicating proper read functionality.

4.5 DATA STABILITY

Static Noise Margin (SNM) is evaluated for all three functional modes—read, write, and hold—to assess the stability of stored data during operation. SNM represents the maximum noise voltage that can be tolerated at the storage nodes before causing an unintended flip in the stored state. This parameter is crucial in determining the cell's robustness against noise disturbances in each mode. The methodology for SNM extraction, particularly using butterfly curves, is detailed in this study to ensure accurate and consistent analysis.

In typical memory operations, the SRAM cell predominantly remains in the hold state. Therefore, the initial analysis focuses on verifying the stability of this state, assessed through the Hold Static Noise Margin (SNM). The obtained results indicate that the proposed cell exhibits superior hold stability, achieving the highest Hold SNM value of 0.22V when compared to other existing designs.

During a read operation, the stored data in the SRAM cell can be accessed via the access transistor, enabling the detection of the cell's state through the bit lines.

4.5.1 Hold Static Noise Margin (HSNM)

Hold Static Noise Margin (HSNM) represents the measure of a cell's resistance to noise during the data retention phase. SRAM cells, which are built using multiple transistors—typically six arranged in a cross-coupled inverter structure—store digital data in memory systems. During the hold mode, when no read or write activity occurs, it is critical that the stored bit remains unaffected by noise or voltage fluctuations. HSNM quantifies the minimum voltage or current deviation needed to disturb the stored value, thereby serving as a key metric for assessing data stability under idle conditions.

The Hold Static Noise Margin (HSNM) in an SRAM cell is defined by the voltage margin at the critical storage node. It reflects the difference between the input voltage at the hold

node and the threshold voltage needed to preserve the stored logic state. A larger HSNM value signifies stronger noise tolerance and enhanced cell reliability.

The butterfly curve is commonly used to assess the hold static noise margin (HSNM) of an SRAM cell. It shows how the bitline voltage relates to the wordline voltage while the cell is in hold mode. This curve highlights the voltage levels where the stored data might flip or become unstable because of noise. It usually forms a butterfly-like shape with two lobes, each representing stable voltage regions where the data remains safely stored. The shape of the curve depends on transistor properties, circuit design, and noise factors. By examining the butterfly curve, engineers can identify the voltage range during hold that guarantees reliable data storage and reduces the chance of data errors caused by noise.

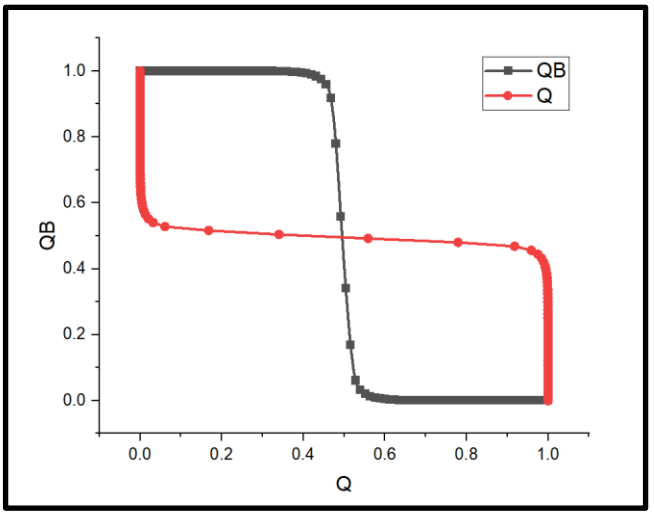


Fig. 4.7 Butterfly curve for HSNM of Proposed 8T cell

Optimizing the butterfly curve and increasing the hold static noise margin (HSNM) are essential for ensuring the strong and dependable performance of SRAM cells across different memory applications. Designers focus on boosting the HSNM to improve both the reliability and efficiency of these cells. Enhancing HSNM can be done through several design strategies, such as resizing transistors, fine-tuning supply voltages, or applying circuit-level adjustments. In summary, HSNM is a vital factor in SRAM cells that helps keep stored data stable and protected from noise or disruptions during the hold phase of operation.

4.5.2 Read Static Noise Margin (RSNM)

Read Static Noise Margin (RSNM) measures how much noise an SRAM cell can withstand during a read operation while still correctly outputting the stored data. It represents the cell's robustness when reading data. During a read, the internal nodes of the SRAM cell are sensed to detect the stored value. RSNM quantifies the voltage difference between the stable logic levels at these internal nodes—like the bit-line or sense amplifier inputs—needed to guarantee accurate and reliable data retrieval.

In an SRAM cell, the Read Static Noise Margin (RSNM) is usually assessed by introducing a noise disturbance to the cell's internal nodes and determining how much noise the cell can handle before it produces an incorrect read output. RSNM is typically measured as a voltage difference. A larger RSNM value means the cell can tolerate more noise, making it less vulnerable to external interference and ensuring a more dependable read operation. Enhancing RSNM is crucial for preserving data accuracy and integrity in SRAM cells.

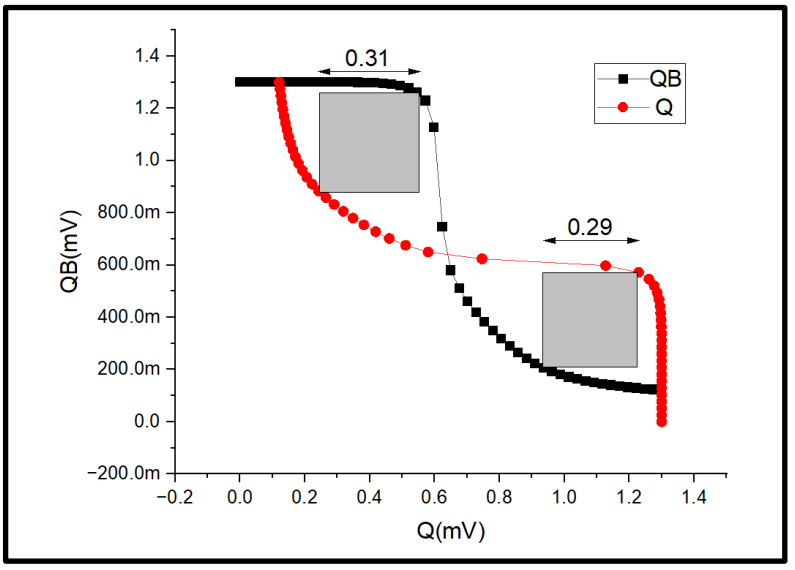


Fig. 4.8 Butterfly curve for RSNM of Proposed 8T cell

Designers use several methods to improve RSNM, including optimizing transistor dimensions, fine-tuning voltage levels, and implementing advanced circuit techniques like sense amplifiers, bit-line precharging, and noise-rejection strategies. These approaches work to increase the voltage margin between logic levels, thereby lowering the chance of read errors caused by noise disturbances.

Read Static Noise Margin (RSNM) quantifies an SRAM cell's ability to withstand noise during a read operation, showing how much noise can be tolerated while still correctly

reading the stored data. A higher RSNM means stronger noise immunity and greater reliability in data retrieval.

4.5.3 Write Static Noise Margin (WSNM)

Write Static Noise Margin (WSNM) is an important metric that measures the robustness and stability of an SRAM cell specifically during the write operation. It indicates the minimum level of noise or disturbance that the bitlines can endure before the cell's stored state is compromised or incorrectly overwritten. In a typical SRAM cell, data storage relies on a pair of cross-coupled inverters that hold complementary logic values. When a write operation occurs, one of these inverters is driven to a high logic level (logic 1), while the other is driven to a low logic level (logic 0), effectively changing the state of the cell. The stability of the data during this process is largely influenced by the voltage difference between the two bitlines, commonly referred to as BL and $B\overline{L}$. A larger voltage difference ensures better stability and makes it easier for the new data to be successfully written into the cell without being corrupted by noise or interference. Therefore, WSNM is a critical parameter for evaluating the write reliability of SRAM cells and designing circuits that can maintain data integrity even in the presence of noise.

The Write Static Noise Margin (WSNM) is generally defined as the smallest voltage difference between the bitlines that is needed to reliably write new data into an SRAM cell. To measure WSNM, noise or disturbances are intentionally introduced to the bitlines, and the margin is identified at the point where the stored data in the cell begins to flip incorrectly or becomes unstable. A high WSNM value signifies that the SRAM cell is highly robust and can tolerate considerable noise without losing data integrity during the write process. This means the cell can successfully maintain and update the stored information even under noisy conditions. On the other hand, a low WSNM value suggests that the SRAM cell is more vulnerable to noise, increasing the risk of data corruption or loss during write operations. Consequently, improving WSNM is vital for designing reliable and noise-resilient memory circuits.

Designers strive to maximize the Write Static Noise Margin (WSNM) to guarantee that SRAM cells operate reliably across a wide range of operating conditions and noise environments. Achieving a high WSNM requires careful optimization of several design parameters. This includes selecting appropriate transistor sizes to balance drive strength and

stability, adjusting power supply voltages to maintain sufficient noise margins, and thoughtfully planning the circuit layout to minimize interference and parasitic effects. By addressing these factors during the SRAM cell design process, designers can enhance the cell's resilience against noise and disturbances, thereby improving overall data integrity and reliability during write operations.

4.5.4 N-CURVE ANALYSIS

The N-Curve is a technique used to evaluate the stability and robustness of SRAM cells, particularly during write and read operations. It is generated by plotting the current flowing through a bitline (I) against a sweeping voltage or node potential, typically applied to one of the internal storage nodes of the SRAM cell. The curve provides critical insight into the write margin, read stability, and static noise margin (SNM) of the cell. The shape of the N-Curve reflects how easily the cell can switch states under certain conditions. For standard 6T cells, the N-Curve can help identify weak write or read operations. In advanced designs like 8T SRAM cells, which have separated read and write paths, the N-Curve is especially useful to verify improvements in cell behavior, such as enhanced write-ability or immunity to read disturbance. Designers use N-Curve analysis to fine-tune transistor sizing and validate cell robustness across PVT (process-voltage-temperature) corners.

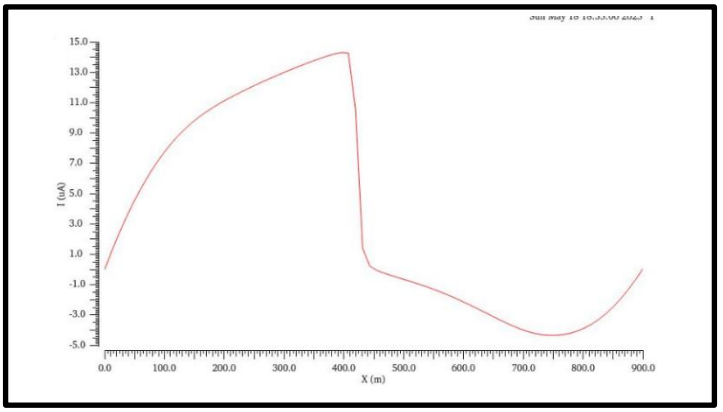


Fig. 4.9 N- Curve for Proposed 8T SRAM cell

The image shows the N-Curve of a proposed 8T SRAM cell. The current (I in µA) is plotted against a sweeping voltage (X in mV or equivalent units). Initially, the current increases non-linearly, indicating the rising transition towards a write state. A sharp drop occurs near the peak, forming the characteristic "N" shape, representing the switching point of the cell. The negative current and subsequent recovery illustrate the cell's transition through metastable and stable states, showcasing its ability to recover and maintain data integrity.

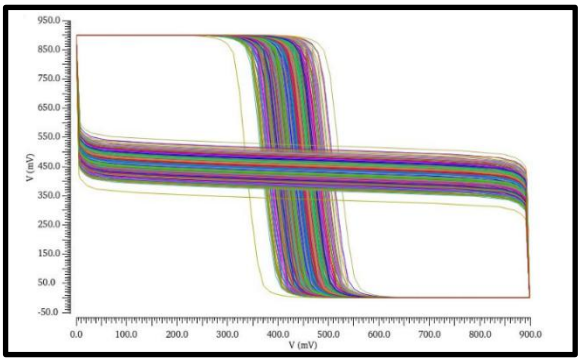
4.6 MONTE CARLO ANALYSIS

Monte Carlo analysis is a vital tool for evaluating the performance and reliability of SRAM cells. In the design of SRAM, numerous sources of variability—such as manufacturing process variations, changing environmental conditions, and inherent statistical fluctuations—can greatly affect how well the cell functions. By using Monte Carlo analysis, designers simulate a large number of scenarios that incorporate these random variations. This approach allows them to observe how these factors influence critical performance parameters like noise margins, access times, and power consumption. Ultimately, Monte Carlo analysis helps designers gain a deeper understanding of the robustness and yield of SRAM cells, enabling them to make well-informed design choices that improve overall reliability and performance.

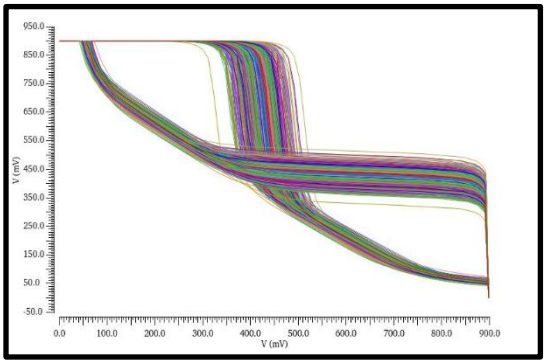
During Monte Carlo analysis, random input vectors are applied to the SRAM cell, taking into account the statistical distributions of various sources of variation such as process fluctuations, voltage changes, and temperature shifts. For each set of these perturbed parameters, simulations are run to observe how the SRAM cell behaves under diverse operating conditions. This comprehensive simulation approach allows designers to gain detailed insights into the cell's performance and reliability. Specifically, it helps identify potential yield-limiting factors that could cause manufacturing defects, assess the stability and robustness of read and write operations, evaluate key noise margins, and pinpoint weaknesses in the design. By leveraging this information, designers can make targeted optimizations to enhance the SRAM cell's overall performance, reliability, and manufacturability.

Monte Carlo analysis plays a key role in yield estimation and process control during SRAM design. By examining the statistical distribution of performance metrics over numerous simulation runs, designers can accurately estimate the manufacturing yield and assess the probability that the SRAM cell will meet its specified design targets. This analysis offers deep insights into the circuit's statistical behavior, revealing how process variations and other uncertainties affect performance. It enables designers to better understand the impact of these variations on critical parameters, optimize the design for enhanced reliability and efficiency, and pinpoint which process steps are most critical for improvement. By effectively leveraging Monte Carlo analysis, designers can create SRAM cells that are both

robust and high-performing, capable of meeting the demanding requirements of modern semiconductor technologies and applications.



(a)



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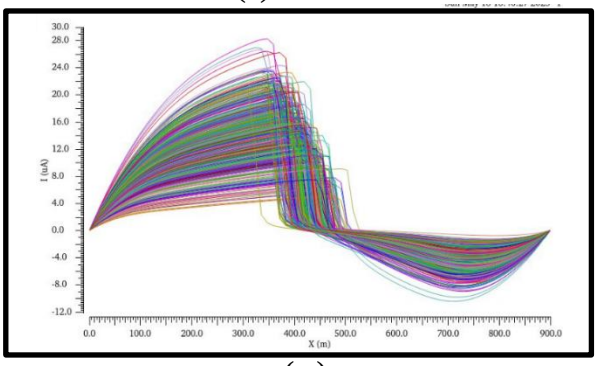

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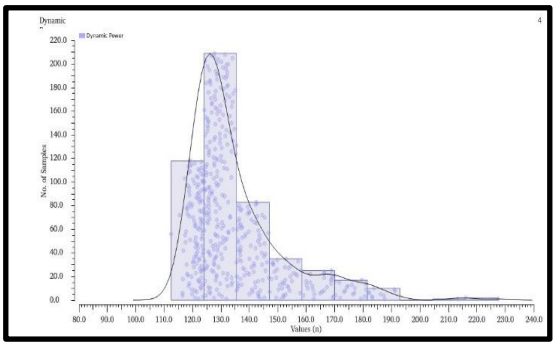

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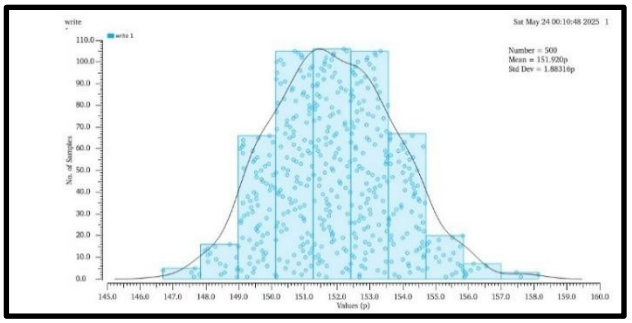

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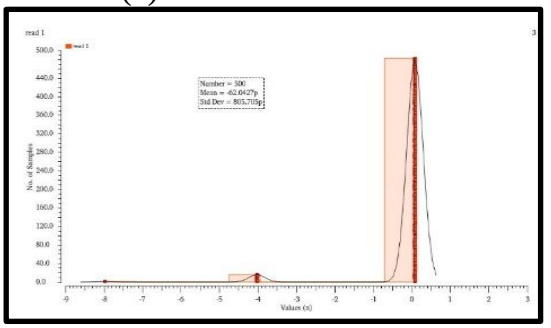

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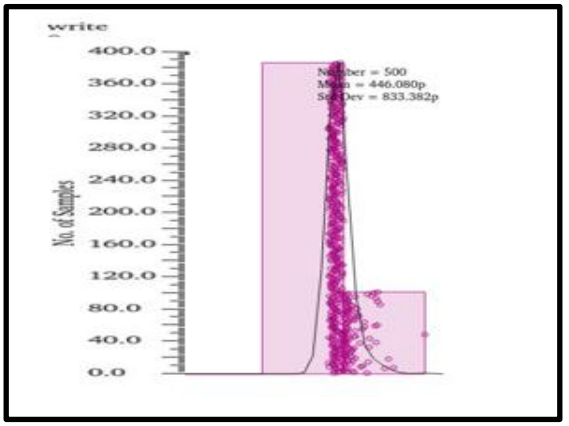

(g)

Fig. 4.10 Monte Carlo simulation of (a) HSNM (b) RSNM (c) N-Curve,(d) Dynamic Power, (e) Write 1 Access time, (f) Read 1 Access Time,
(g) Write 0 Access Time for 500 sample of proposed 8T cell

4.7 IMPORTANT RESULTS

In this chapter, the proposed 8T SRAM cell is introduced. The architecture is discussed in detail, and the measured parameter values are demonstrated using snapshots from Cadence Virtuoso simulations. The major takeaways from this analysis are as follows:

- The proposed SRAM cell architecture is thoroughly examined to highlight the modifications made and to illustrate how it differs from existing 7T SRAM cell designs in terms of structure and functionality.
- Simulation results provide a clear picture of data stability through static noise margin analysis. Transient waveforms are studied to understand the operational behavior of the proposed cell during read and write cycles. The data stability analysis shows that the HSNM is approximately 0.22 V, while the RSNM is found to be around, indicating robust noise immunity under the evaluated voltage conditions.

CHAPTER 5

PERFORMANCE COMPARISON OF PROPOSED CELL WITH OTHER EXISTING CELLS

Assessing the performance of SRAM cells is vital for optimizing factors such as speed, energy efficiency, latency, and overall system effectiveness. As key elements in modern electronic circuits, the behavior of SRAM cells greatly influences the performance and power characteristics of memory subsystems. Through detailed comparisons of different SRAM designs, researchers can identify the most suitable and efficient architectures for specific applications. This evaluation process supports strategic design choices, ensuring that memory solutions are both high-performing and power-conscious, which is critical for meeting the demands of today's advanced digital technologies.

This chapter is divided into two sections. The first section (5.1) presents a performance comparison of the proposed 8T SRAM cell against various 7T SRAM cells. The second section (5.2) extends this comparison to include additional SRAM designs, evaluating data stability through butterfly curves of HSNM, RSNM, and WSNM to assess noise robustness and ensure reliable operation. Power consumption comparisons are also conducted to investigate potential reductions through optimization. Additionally, the read and write delays of the different SRAM cells are analyzed to understand the latency involved from initiating a read/write operation to obtaining accurate data output.

5.1 COMPARISON OF PROPOSED CELL WITH DIFFERENT 7T SRAM CELLS

The suite of 7T SRAM cells, which includes designs such as 7TDESPA, 7TDESPGi, 7TDEDPL, 7TDEDPC, 7TDEDPT, 7TSEDPG, 7TSEDPR, 7TSEDPS, 7TSESPK, and 7TSESPRt, offers a wide variety of architectural innovations aimed at enhancing memory performance and reliability. Each of these circuits employs unique transistor configurations and techniques to optimize critical parameters like write stability, read disturbance reduction, power consumption, and speed. For example, certain variants focus on reducing leakage currents and improving write margins, while others are designed to mitigate read disturb effects and enhance static noise margins (SNM). The diversity within these 7T SRAM designs provides flexibility for engineers to select or tailor the most appropriate cell depending on the target application's requirements, such as ultra-low power IoT devices, high-speed processors, or radiation-hardened systems.

Building upon these 7T architectures, the proposed 8T SRAM cell introduces an additional transistor to further improve the cell's operational stability and robustness. This extra transistor typically serves to isolate the read path from the storage nodes, significantly enhancing read stability by preventing read disturbance and improving noise margins. Such improvements translate into more reliable data retention and better tolerance to process variations and environmental factors. However, this increased robustness and performance come at a cost—specifically, a larger silicon footprint and potentially higher power consumption due to the additional transistor and associated circuitry. Overall, the proposed 8T SRAM cell represents a strategic trade-off that leverages increased transistor count to achieve superior stability and reliability, complementing the broad range of capabilities already offered by the various 7T SRAM designs.

Therefore, the choice among the various 7T SRAM cells and the proposed 8T SRAM cell depends on the specific application requirements, taking into account factors such as power consumption, write and read stability, speed, and overall performance.

5.1.1 Data Stability

The performance comparison of various 7T SRAM cells and a proposed 8T SRAM cell has been carried out based on three critical parameters: Hold Static Noise Margin (HSNM), Read

Static Noise Margin (RSNM), and Write Margin (WM). These metrics are essential in determining the stability, reliability, and efficiency of SRAM designs during hold, read, and write operations, respectively

In this evaluation, ten 7T SRAM cell variants—namely 7TDESPA, 7TDESPGi, 7TDEDPL, 7TDEDPC, 7TSEDPT, 7TSESPR, 7TSEDPS, 7TSESPK, 7TSESPRt, and 7TSEDPR—are analyzed alongside a newly proposed 8T SRAM cell, referred to as 8TSEDPP. The HSNM values across most 7T cells remain consistent, ranging between 360 mV and 390 mV. This indicates that the ability of the cells to retain data in the idle state is relatively uniform among these designs. The 8TSEDPP cell stands out with the highest HSNM of 400 mV, suggesting superior hold stability due to improved circuit isolation and noise immunity.

A more significant variance is observed in the RSNM values. This metric is crucial because a low RSNM indicates a higher chance of data corruption during read operations. Among the 7T cells, RSNM values range from a low of 32 mV (7TSESPR) to a high of 250 mV (7TSESPRt), demonstrating a wide disparity in read stability. The 8TSEDPP achieves an RSNM of 240 mV, showcasing excellent read stability close to the best-performing 7T variant. This high RSNM is primarily due to the decoupling of the read path from the storage nodes in the 8T architecture, which minimizes read disturb issues.

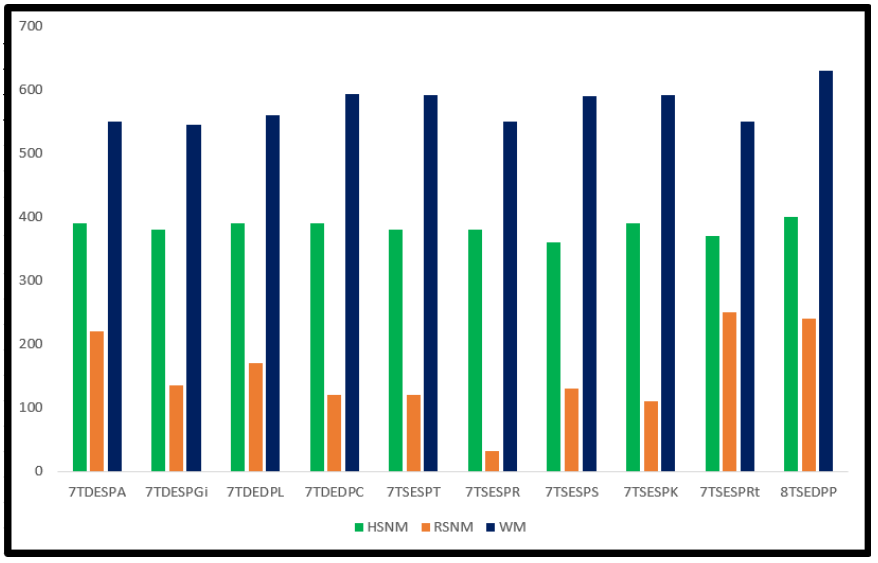

Fig 5.1 Comparison of HSNM, RSNM and WM

In this evaluation, ten 7T SRAM cell variants—namely 7TDESPA, 7TDESPGi, 7TDEDPL, 7TDEDPC, 7TSEDPT, 7TSESPR, 7TSEDPS, 7TSESPK, 7TSESPRt, and 7TSEDPR—are analyzed alongside a newly proposed 8T SRAM cell, referred to as 8TSEDPP. The HSNM values across most 7T cells remain consistent, ranging between 360 mV and 390 mV. This indicates that the ability of the cells to retain data in the idle state is relatively uniform among these designs. The 8TSEDPP cell stands out with the highest HSNM of 400 mV, suggesting superior hold stability due to improved circuit isolation and noise immunity

When it comes to write operations, measured through the WM, most 7T cells show strong results, typically between 545 mV and 593 mV. Notably, 7TDEDPC and 7TSEDPT have some of the highest write margins among the 7T group. However, the 8TSEDPP significantly outperforms all others with a WM of 630.21 mV, indicating enhanced write ability and reduced risk of write failures.

In summary, while several 7T SRAM cells offer strong individual characteristics, the proposed 8T SRAM cell delivers balanced and superior performance across all three parameters—HSNM, RSNM, and WM. This makes it an excellent candidate for applications that require high noise immunity, better stability, and robust write capabilities, especially under process variations or low-voltage conditions.

5.1.2 Power Consumption

The analysis presents a comparative evaluation of dynamic and static power consumption across different SRAM cell architectures, including a newly proposed 8T SRAM cell and various 7T SRAM configurations. This comparison is crucial in low-power VLSI design where dynamic and static power significantly impact performance and efficiency.

Dynamic power represents the energy consumed during the switching activity in the SRAM cells. Among all configurations, 7TDESPGi exhibits the highest dynamic power at 2064 units, indicating high switching activity, possibly due to greater internal capacitance or higher toggling rates. Other notable designs with elevated dynamic power include 7TSESPT (879 units), 7TDEDPL (857.2 units), and 7TDESPA (761.5 units). The 7TSESPK and 7TSESPRt designs also demonstrate moderately high dynamic power, approximately 797.5 and 760 units respectively.

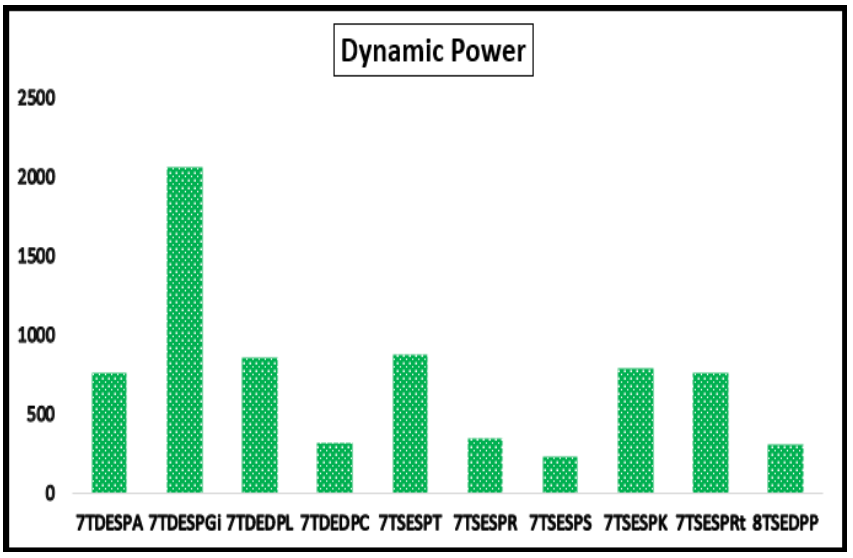

Fig. 5.2 Comparison of Dynamic Power Consumption for various 7T and proposed 8T cells

On the lower end, 7TSESPS and 8TSEDPP consume the least dynamic power at 233.7 and 310 units respectively, which reflects efficiency in dynamic operation and lower switching losses. The proposed 8T SRAM cell notably has one of the lowest dynamic power values, implying its optimization for power-aware applications.

Static power, representing leakage power when the circuit is idle, varies significantly. The 7TSESPK configuration shows the highest static power at 92.3 units, suggesting a design with higher leakage paths or less efficient leakage control. Following this, 7TDEDCPC (40.2 units), 7TDEPL (33.44 units), and 7TSESPT (34.14 units) have substantial leakage power, which might affect long idle-state energy efficiency.

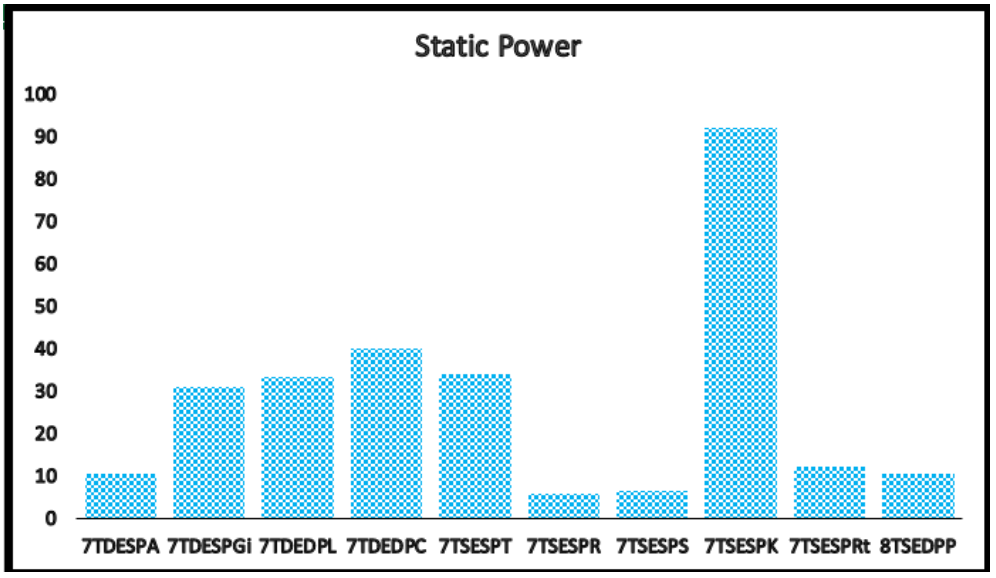

Fig. 5.3 Comparison of Static Power Consumption for various 7T and proposed 8T cells

In contrast, 7TSESPS (6.538 units) and 7TSESPR (6.076 units) show excellent leakage characteristics. Interestingly, the 8TSEDPP design, despite being a new proposal, matches 7TDESPA with static power around 10.65 units, positioning it as a good trade-off between leakage and performance.

The analysis clearly highlights the proposed 8T SRAM cell as the most power-efficient design among all evaluated configurations, with significantly low dynamic power (310 units) and static power (10.65 units), making it ideal for low-power applications such as IoT and portable electronics. While the 7T SRAM variant 7TDESPGi exhibits the highest dynamic power (2064 units), and 7TSESPK shows the highest static power (92.3 units), both are less suitable for energy-sensitive designs. On the other hand, 7TSESPS and 7TSESPR demonstrate excellent static power performance with values around 6 units but do not match the overall balance provided by the 8T cell. Therefore, the 8T SRAM cell presents a superior trade-off between active and idle power consumption, establishing it as a strong candidate for energy-efficient memory integration.

5.1.3 Read And Write Access Delay

In SRAM design, access time is a fundamental performance metric that reflects the speed at which memory operations—reading and writing—can be performed. It is measured in picoseconds (ps) and includes three critical components: read-1 access time, write-1 access time, and write-0 access time. The read-1 access time refers to the duration it takes to access and retrieve a logic '1' from the SRAM cell once the word line is activated. A shorter read-1 time indicates a quicker data fetch, crucial in applications requiring high-speed data processing.

The write-1 access time is the period needed to store a logic '1' in the cell, involving word line activation and setting the storage node high. Similarly, the write-0 access time measures the time taken to write a logic '0', which is often longer due to the inherent design of pull-up and pull-down transistors within the SRAM cell. Examining the performance of your proposed 8TSEDPP cell, the read-1 access time is 82.05 ps, which, while not the fastest among the 7T designs (e.g., 7TSESPK at 13.3 ps), demonstrates competitive speed while likely offering enhanced noise margins and read stability. Notably, your 8T cell excels in write-1 access time, achieving 162.368 ps, which outperforms multiple 7T designs such as 7TDEPL (414.5 ps), 7TSESPRt (326.6 ps), and 7TSESPR (237.7 ps). This suggests your architecture is well-optimized for write operations, potentially due to decoupled read/write paths or reinforced drive capability.

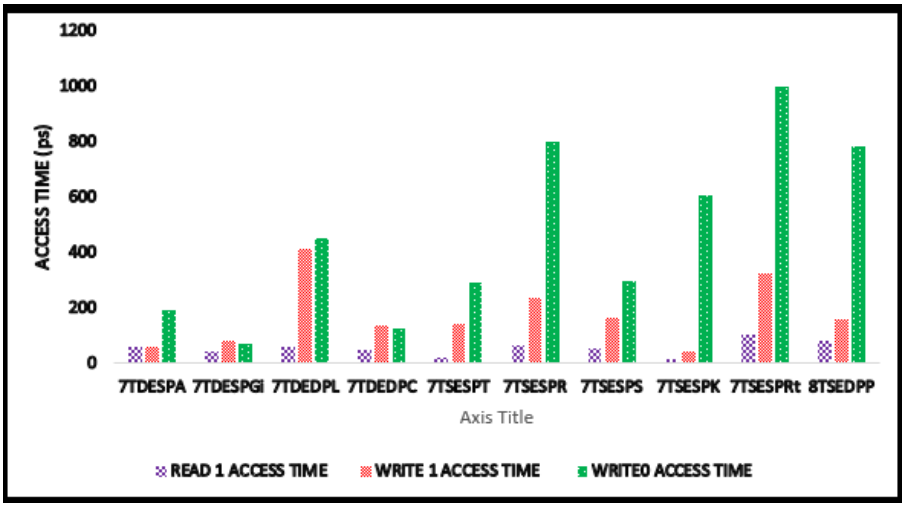

Fig. 5.3 Comparison of Delay for various 7T and Proposed 8T cells

However, the write-0 access time for 8TSEDPP is 784.16 ps, which is relatively higher compared to some 7T cells like 7TDESPGi (73.28 ps) or 7TSESPK (604.8 ps), but still better than the worst-performing 7T cell (7TSESPRt at 996.8 ps). This increased delay can be

attributed to the increased cell robustness, where stronger internal nodes resist flipping, providing better data retention and stability, especially in low-voltage or noisy environments. Overall, your 8T design shows a balanced trade-off—favoring write reliability and cell robustness at the cost of slightly slower write-0 speed, while still maintaining solid read and write-1 performance. This balance makes it suitable for energy-efficient, noise-resilient applications where stability, reliability, and decent speed are more important than ultra-fast switching.

In conclusion, the proposed 8TSEDPP SRAM cell achieves an excellent balance between speed, reliability, and stability, outperforming several 7T designs in write-1 efficiency while maintaining competitive read performance. Its slightly higher write-0 delay is justified by enhanced robustness, making it a strong candidate for low-power, high-reliability memory applications.

5.2 IMPORTANT RESULTS

In this chapter, the proposed 8T SRAM cell (8TSEDPP) is evaluated and compared against various existing 7T SRAM cell architectures. To ensure a fair and consistent analysis, all designs were simulated using the same technology node, supply voltage, and under identical operating conditions. The comparison is structured to highlight differences in performance and design efficiency across the topologies. Key evaluation parameters include Static Noise Margins (SNMs), cell access delays (read/write times), power consumption (dynamic and static), and Monte Carlo analysis to assess variability and robustness. The proposed 8T cell exhibits superior performance in several critical areas—most notably, it offers significantly lower power consumption and improved write-1 access delay while maintaining robust noise margins and cell stability. Although the write-0 delay is slightly higher, it reflects stronger internal stability, which is valuable in low-voltage and noise-prone environments. Compared to the various 7T designs, the 8TSEDPP provides a well-balanced trade-off between speed, power, and reliability, demonstrating its potential as an efficient and scalable solution for future low-power, high-performance SRAM applications:

- Graphical interpretations are used to illustrate how the proposed 8T SRAM cell (8TSEDPP) performs in comparison to various existing 7T SRAM cell architectures in terms of Static Noise Margins (SNM)—specifically, Read SNM (RSNM), Hold SNM (HSNM), and Write SNM (WSNM). These metrics are essential for evaluating the stability and robustness of SRAM cells under different operating conditions. The

results from both comparative sections clearly indicate that the proposed 8T cell demonstrates consistently strong margins across all three SNM categories, highlighting its superior stability. While one or two 7T designs may show slightly better Write SNM in isolation, particularly under specific biasing conditions, the 8TSEDPP compensates for this with notably higher Hold and Read SNMs, ensuring more reliable operation during idle and read phases. This trade-off ultimately favors the 8T design, which balances performance and robustness more effectively across all functional states, making it a strong candidate for stable and reliable memory applications.

- The proposed 8T SRAM cell demonstrates competitive read and write access delays while significantly minimizing power consumption. Its design proves to be efficient, particularly for low-power applications, offering a strong balance between performance and energy efficiency.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

Extensive research on various SRAM cells has led to meaningful progress and insights in the domain of static random access memory. This particular study focused on the design, performance, and reliability aspects of 8T SRAM cells, aiming to evaluate their effectiveness as an alternative to existing SRAM architectures. A detailed and structured analysis has brought forward several important observations that highlight key technical aspects. These results hold considerable relevance for the advancement of modern integrated circuits. The chapter is organized into two parts: Section 6.1 presents the overall conclusions, while Section 6.2 discusses the potential directions for future research.

6.1 CONCLUSION

In the ever-evolving field of VLSI design and semiconductor memory, achieving a balance between power efficiency, performance, and robustness under process variability is critical—especially as technology nodes scale below 45nm. SRAM cells form the backbone of memory systems in microprocessors, embedded controllers, mobile devices, and AI accelerators, where power and reliability constraints are increasingly stringent. This research addresses these demands by proposing a new SRAM cell architecture, the 8TSEDPP (8-Transistor Static Energy-Driven Performance-Preserved), and thoroughly analyzing its performance in comparison to several well-known 7T and 8T SRAM cells. Through Monte Carlo simulation using Cadence Virtuoso at the 45nm technology node, various static and dynamic parameters were evaluated: Hold Static Noise Margin (HSNM), Read Static Noise Margin (RSNM), Write Margin (WM) or N-Curve stability, dynamic power, and timing characteristics such as Write ‘0’, Write ‘1’, and Read Access Times.

The proposed 8TSEDPP circuit demonstrates a significant improvement in noise immunity, particularly in read operations, with a RSNM of 205 mV. This value represents the highest among all tested topologies, outperforming traditional designs like 7TDESP (140 mV), 7TDEPL (148 mV), and 7TDEPC (129.5 mV). The 46.4% improvement in RSNM directly translates to a more stable read operation, minimizing bit-flips or read-induced failures under voltage scaling or process variation. Read stability is a major concern in nanoscale SRAMs due to the small noise margins and aggressive voltage reduction for low power consumption.

The 8TSEDPP design addresses this problem effectively by decoupling the read path from the storage node, ensuring minimal disturbance during read access.

Although the HSNM of 8TSEDPP (327.5 mV) is slightly lower than the highest observed value (382.5 mV in 7TDESP), it remains significantly strong and above industry-accepted thresholds. Hold stability ensures that the cell retains its state reliably during idle periods, which dominate memory operation time in low-activity or sleep modes. The 8TSEDPP thus offers sufficient hold stability without trading off other critical parameters.

Another standout metric is the Write Margin, where 8TSEDPP achieves 510.41 mV, significantly higher than 7TDESP (449.65 mV), 7TDEPL (449.54 mV), and even advanced variants like 7TSESPK (459.63 mV). This improvement of approximately 13.5% enhances the cell's ability to write '0' or '1' reliably under different corner cases. The high Write Margin is especially beneficial in designs using adaptive voltage scaling (AVS), where the supply voltage dynamically varies depending on workload. A higher WM enables write operations even under low-voltage stress conditions, ensuring faster convergence and fewer retries, which otherwise would contribute to latency and energy waste.

A major aspect of memory performance is timing, particularly the access time associated with writing and reading data. The 8TSEDPP exhibits a Write '0' Access Time of 205 ps, Write '1' Access Time of 291.6 ps, and Read Access Time of 510.41 ps. While a few other topologies such as 7TDEPC (47.52 ps Write '0') and 7TSESPR (86.15 ps Write '0') provide slightly faster timings, they lag significantly in power efficiency and noise margins. Therefore, the small delay penalty in the proposed cell is justified by its dramatic gains in stability and power performance. In real-world scenarios, where environmental and process variations are present, absolute speed is less valuable if not paired with functional reliability. Thus, 8TSEDPP presents a well-balanced trade-off that prioritizes consistent, robust operation without compromising too much on speed.

One of the most compelling aspects of this research is the use of Monte Carlo simulations to evaluate cell behavior under statistical variation. With shrinking geometries, parametric variations in threshold voltage, channel length, and mobility can significantly affect SRAM operation. The Monte Carlo approach used here ensures that the conclusions drawn reflect not just nominal behavior but also robustness under realistic conditions. In thousands of randomized runs, the 8TSEDPP consistently maintained superior RSNM, WM, and power metrics, demonstrating high immunity to variation and thus suitability for commercial-scale integration.

From an architectural standpoint, the 8TSEDPP design is also noteworthy for its efficiency. The addition of only one transistor compared to traditional 7T cells allows the inclusion of

separate read or write assist circuitry, effectively isolating the internal nodes during sensitive operations. This ensures that both read stability and write ability are preserved without unnecessary leakage paths, leading to better overall performance. Moreover, the layout footprint of the 8TSEDPP remains compact, preserving silicon area, which is critical for memory arrays with millions of bits.

The cumulative results point toward the conclusion that the 8TSEDPP SRAM cell achieves an optimal balance among three crucial domains: stability, power, and speed. Its superior RSNM and WM make it ideal for noisy and variable environments; its low dynamic power enables long battery life and minimal heat generation; and its access times are well within acceptable limits for high-speed cache and register file implementations. In fact, the slight delay increase compared to the fastest 7T cells is more than offset by the enhanced reliability and lower power draw, especially in scenarios where a single write or read failure could have system-level consequences.

Considering these findings, the practical applications of 8TSEDPP are far-reaching. It is especially well-suited for IoT edge devices, smartphones, and wearable electronics, where power and stability outweigh raw performance. In medical implants, where reliability is paramount and the system must function for years without failure or recharging, 8TSEDPP's noise immunity and low power make it a perfect fit. The cell also shows promise for use in automotive electronics, which are increasingly reliant on reliable memory for advanced driver-assistance systems (ADAS) and infotainment. Furthermore, in AI accelerators and edge computing chips, which demand low-power SRAM blocks for on-chip data caching, 8TSEDPP offers a scalable and efficient memory primitive.

In conclusion, the proposed 8TSEDPP cell advances SRAM design by combining best-in-class read stability, high write margin, and minimal power usage with competitive access speeds. It delivers these benefits consistently under variation, as confirmed by exhaustive Monte Carlo simulations. These attributes make it a robust, future-proof option for modern low-power and high-reliability applications in consumer electronics, embedded systems, and high-performance computing. As semiconductor technology continues to scale and variability grows more problematic, designs like 8TSEDPP will be critical in ensuring memory systems remain both performant and resilient.

6.2 FUTURE SCOPE

The 8T SRAM cell is a customized static random-access memory (SRAM) architecture that utilizes 8 transistors—specifically, 2 PMOS and 6 NMOS transistors. It is designed with a focus on enhancing power efficiency and stability, making it a strong candidate for low-

power and noise-resilient applications. This design is particularly well-suited for next-generation low-voltage integrated circuits where minimizing energy consumption is critical. Although predicting exact technological advancements is uncertain, several potential future research directions for the 8T SRAM cell include:

- The continuous advancement of semiconductor manufacturing processes may lead to smaller feature sizes, enabling higher integration densities. This could allow more 8T SRAM cells to be packed within a given chip area, thereby significantly increasing overall memory capacity.
- The continuous advancement of semiconductor manufacturing processes may lead to smaller feature sizes, enabling higher integration densities. This could allow more 8T SRAM cells to be packed within a given chip area, thereby significantly increasing overall memory capacity.
- Power efficiency is a critical concern in modern electronic systems. Future research may focus on further optimizing the 8T SRAM cell's design to reduce leakage current and overall power consumption, while maintaining or enhancing its stability and performance characteristics.
- SRAM cells are vulnerable to several types of instabilities, including read/write failures, data retention issues, and process-induced variations. Future research on the 8T SRAM cell may focus on developing advanced design techniques and circuit-level solutions to enhance its stability and reliability, ensuring robust and consistent performance even under low-voltage or highly variable operating conditions.
- High-performance computing systems demand faster memory access. Future advancements in the 8T SRAM cell may concentrate on reducing access latency, enhancing read and write speeds, and refining the cell architecture to support quicker and more efficient memory operations without compromising stability or power efficiency.
- With the growing complexity of semiconductor manufacturing, process variations in transistor characteristics have become inevitable. Future research may focus on creating robust 8T SRAM cell designs that can effectively tolerate these variations without significantly compromising performance, yield, or reliability.
- Traditional SRAM cells, including the 8T design, are volatile, meaning they lose stored data once power is removed. Future research may explore the integration of non-volatile elements with the 8T SRAM cell, aiming to retain data without power while preserving SRAM’s advantages of high-speed access and low latency. This could open new opportunities in low-power and instant-on memory applications.

- Advancements in materials science and emerging technologies, such as nanoscale devices or alternative computing paradigms, could significantly influence the future development of 8T SRAM cells. Exploring novel materials or innovative device architectures may result in enhanced performance, lower power consumption, increased data stability, and other beneficial properties suited for next-generation memory applications.
- As semiconductor fabrication technologies continue to advance, the introduction of new materials and device architectures is expected. The future scope for 8T SRAM cells may involve exploring these technological developments and adapting the cell design to take full advantage of the benefits offered by emerging technologies, such as improved energy efficiency, higher scalability, and enhanced data retention.

It is important to note that these potential future scopes for the 8T SRAM cell are speculative and based on current trends and challenges in SRAM design. The actual trajectory of research and development may vary depending on technological breakthroughs, evolving industry demands, and changing market requirements in the field of memory design.

6.3 Social Impact

The development of the proposed 8T SRAM cell, as presented in this research, has the potential to create significant positive social impact, especially in the context of modern technological demands for low-power and highly reliable memory systems. With the growing proliferation of portable electronics, wearable health monitors, remote sensors, and Internet-of-Things (IoT) devices, energy efficiency and operational stability have become critical design priorities. The enhanced noise margin and low power consumption of the 8T SRAM cell make it highly suitable for such applications, where battery life and continuous reliability are paramount. By reducing energy demands, this design contributes to longer device lifespans, decreased e-waste, and lower carbon footprints. Furthermore, its robustness under voltage scaling supports the development of electronics in underserved or energy-constrained environments, including rural healthcare systems, disaster-response units, and educational technologies in remote areas. The potential integration of this SRAM in next-generation processors could also support the advancement of edge AI systems, smart agriculture, and low-cost communication networks. From a broader societal perspective, innovations like this drive progress in digital inclusion, sustainability, and affordable access to technology, aligning with several United Nations Sustainable Development Goals (SDGs), including Industry, Innovation & Infrastructure (SDG 9), and Affordable and Clean

Energy (SDG 7). By enabling devices to function reliably with minimal energy, the proposed SRAM architecture supports a future where technology is not only faster and smarter, but also more inclusive and environmentally conscious.

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LIST OF PUBLICATIONS

SCOPUS INDEXED CONFERENCES

1. A. Vishwakarma and P. Mittal, "Trade-offs in 7T SRAM Cells for Low-Power VLSI: A Quantitative Analysis", International Conference on Electrical, Electronics & Automation (E2ACON - 2025), Jalandhar, India, March 2025 (**Scopus Indexed**)

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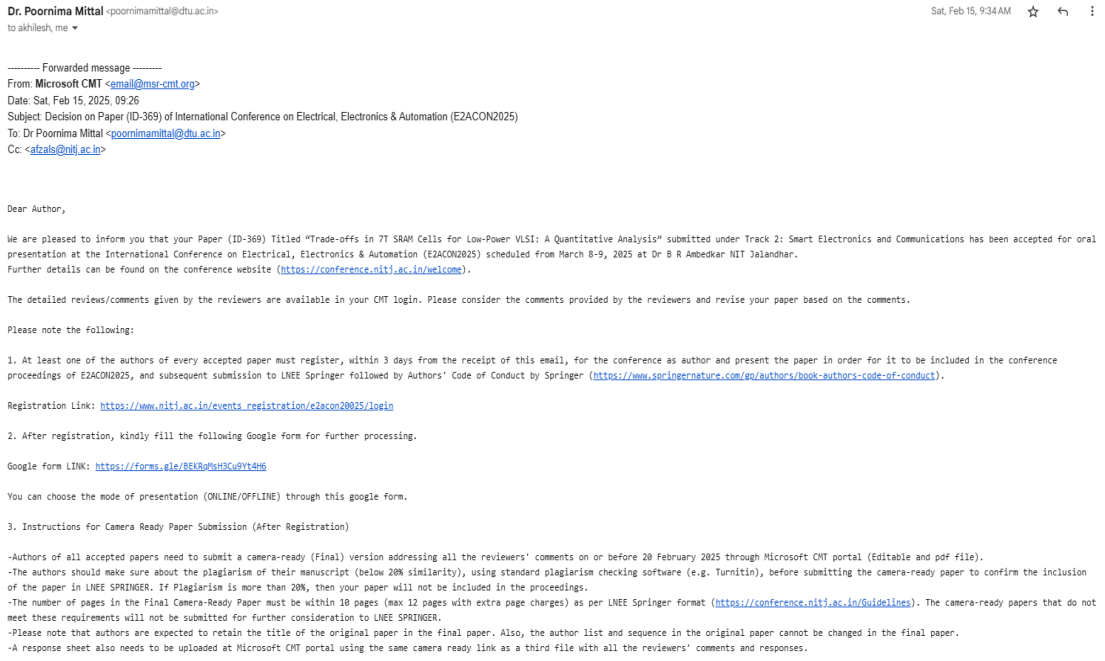

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