GRID SYNCHRONIZATION AND OPERATION OF PARALLEL INVERTERS

DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

DOCTOR OF PHILOSOPHY

Submitted by:

Aditya Narula

(Roll no. 2K16/PhD/EE/07)

Under the supervision of

Prof. Vishal Verma

DEPARTMENT OF ELECTRICAL ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
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DECLARATION

I, ADITYA NARULA (2K16/PhD/EE/07) hereby declare that the work, which is being presented in the project report entitled, **"GRID SYNCHRONIZATION AND OPERATION OF PARALLEL INVERTERS"** submitted for partial fulfillment of the requirements for the award of the degree of Doctor of Philosophy is an authentic record of my own work carried out under the able guidance of Dr. VISHAL VERMA, Professor, EED, DTU. The matter embodied in the dissertation work has not been plagiarized from anywhere and the same has not been submitted for the award of any other degree or diploma in full or in part.

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(Formerly Delhi College of Engineering)

CERTIFICATE

This is to certify that the thesis entitled, "**GRID SYNCHRONIZATION AND OPERATION OF PARALLEL INVERTERS**", submitted by Mr. **ADITYA NARULA**, Roll No. 2K16/PhD/EE/07, student of Doctor of Philosophy in Electrical Engineering Department from Delhi Technological University (Formerly Delhi College of Engineering), is a dissertation work carried out by him under my guidance during session 2016-2024 towards the partial fulfillment of the requirements for the award of degree of Doctor of Philosophy.

The uniqueness of the thesis pertains to the incorporation of impedance on the DC link of the inverter to limit the circulating current among the inverters, additionally the synchronization and resynchronization algorithm with superior dynamic performance, which has not been reported elsewhere. I wish him all the best in his endeavors.

(Dr. VISHAL VERMA)

Professor, EED, DTU

SUPERVISOR

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Above all, I thank God for everything.

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Mr. Aditya Narula
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GRID SYNCHRONIZATION AND OPERATION OF PARALLEL INVERTERS

ABSTRACT

With rapid industrialization in developing nations, the power demand from the end consumer has exponentially grown. To support the conventional power generation sources (based on fossil fuels) in meeting the rising power demand, power generation based on Distributed Energy Resources (DER's) enacting as small power sources are gaining popularity. The microgrid architecture with local energy generating sources like photovoltaic, wind, battery systems have opened the pathway for small scale smart distribution grids interfacing the sustainable and clean energy sources with the grid through a voltage / current controlled voltage source inverter. Interfacing a voltage sourced inverter with the grid additionally allows the inverter to support the power quality of grid during grid sag and swell condition. Further based on the power demand at the consumer end the number of interfacing inverters can be added or reduced allowing a scale up or scale down approach in the connected network. The response and dynamics of the microgrid are governed by three major factors – 1) The dynamics of the renewable energy source at the DC side, 2) the synchronization dynamics of the interfaced inverter, 3) Control technique of the interfacing inverter and 4) Effect of high penetration of the low inertial inverters with high switching frequency.

The interfacing voltage source inverter is vulnerable to disturbance from both grid side and the renewable energy source or input side, with common intermittencies like partial shading of the photovoltaic panel, different wind speeds, low battery voltages etc. The disturbances at the grid side can be controlled through the control technique of the interfacing inverter or a synchronization algorithm with fast tracking capability. On the DC side the conventional practice is to use a non-isolated boost or buck converter based upon the series parallel combination of the installed solar panels. Conventional converters like buck converter or boost converter struggle with the operating duty requirement at time of partial shading, with the operating duty reaching the nonlinear region, thereby compromising on the operating efficiency. Also, addition of the natural output impedance network through the interfacing

converter will help in mitigating the spike and transients in the DC link and the control signals during intermittencies at either grid side or input side. This would result in smooth running of the inverter.

A VSI interfaced with the renewable energy source typically has low inertia due to lack of moving parts unlike a synchronous generator. As a result, the system remains sensitive towards grid frequency variations. With multiple injection of VSI in the system, the inertia of the system would not increase making the system vulnerable unless and until a fast control on frequency change is not incorporated or virtual inertia is embedded, even though such arrangement provides better reliability. With paralleled VSI having different situations on the connected nodes the response to the change of voltage or frequency often lead to issues of circulating current and large variations during transients due to lack of inertia or damping system. For parallel combination of inverters aligned with the stringent grid codes, synchronization algorithm plays a crucial role. Noncompliance of the code would result in outage of the inverter. The stability of synchronization algorithm dictates the capability dictates the capability of the parallel operation of the inverter especially during off grid mode of operation in master slave configuration. The synchronization algorithms like zero crossing detection (ZCD), voltage unit template-based algorithms and SRF – PLL provide the requisite tracking but suffer immensely during grid disturbances. SOGI adaptive filter based PLL with filtering capability has a superior tracking and filtering capability when compared to conventional PLL. Moreover, the capability of the SOGI filter to generate orthogonal signals eliminates the requirement of Clarke's transformation reducing the complexity and computation of the algorithm.

The work proposes impedance based continuous input current converters for photovoltaic and battery charging applications. The same have been modelled; simulated and experimentally validated under various test conditions. The impedance network allows auxiliary boost supporting the system under severe conditions like partial shading, irradiance change and battery deep discharge. Additionally, the impedance network installed at the input side of the inverter limits the flow of circulating current within the system.

Synchronization algorithm based on Second Order Generalized Integrator (SOGI) resonating at 100Hz is proposed and experimentally validated for severe grid disturbances. The synchronization algorithm enhances the fault bearing capability of the inverter allowing it to remain synchronized with the grid with minimum transients. A resynchronization algorithm embedded in the Second Order Generalized Integrator Phase Locked Loop (SOGI – PLL) is proposed in the work working with adaptive droop filter. The resynchronization algorithm seamlessly transfers the inverter from grid forming mode to grid connected mode and vice versa while limiting the circulating current among the inverters. The resynchronization algorithm limits the transitional spikes besides administering fast dynamics with prominent signal filtering.

The development of algorithm and hardware including development of various control and interface cards have been indigenously done. The simulation and hardware results are presented which show good agreement with the theoretical modeling and analysis.

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ABBREVIATIONS

Abbreviations	Full-Form
PV	Photovoltaic
AC	Alternating Current
DC	Direct Current
P&O	Perturb And Observe
InC	Incremental Conductance
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
I_{SC}	Short-Circuit Current
V_{OC}	Open-Circuit Voltage
V_{DC}	Dc Link Voltage
VSI	Voltage Source Inverter
MIC	Module Integrated Converter
THD	Total Harmonic Distortion
CMC	Current Mode Control
EMI	Electromagnetic Interference
STATCOM	Static Compensator
PWM	Pulse Width Modulation
d-q	Direct-Quadrature
G2V	Grid To Vehicle
V2G	Vehicle To Grid
SoC	State Of Charge
EVs	Electric Vehicles
LVRT	Low Voltage Ride Through
HF	High Frequency
VSC	Voltage Source Converter
SPWM	Sinusoidal PWM
BESS	Battery Energy Storage System
SRF	Synchronous Reference Frame
SOGI	Second Order Generalized Integrator
PLL	Phase Locked Loop
PCC	Point Of Common Coupling

PI	Proportional Integral
PQ	Power Quality
THD	Total Harmonic Distortion
V/F	Voltage/Frequency
kHz	Kilo Hertz
DSO	Digital Storage Oscilloscope
I/O	Input / Output
ADC	Analog to Digital Converter

Chapter I

INTRODUCTION

1.1. General

With rapid industrialization in developing nations the power demand from the end consumer is growing exponentially increasing the stress over the fuel reserves. With the limitations imposed because of environmental concerns and depleting fuel reserves the generation from conventional power sources based on fossil fuels, has been slowly migrating towards renewable energy sources for sustainable growth. In contrast to centralized generation system, the distributed generation system includes many generating and storage units, facilitating energy efficiency due to vicinity with the load centers, reduction in the pollution due to the use of renewable sources and good power quality due to quick response and more reliability [1-2]. Further energy efficient devices, different converter configurations have facilitated extraction of maximum power from the renewable energy sources like photovoltaic and wind and reduce the burden on the grid. High efficiency power electronics converters have helped boost the efficient power generation from renewable sources. Among all the renewable energy sources photovoltaic energy source has seen growth at much faster rate due to drop in capital costs. To support this high penetration of Distributed Energy Sources (DER's) the governing bodies are coming up with stringent grid codes to improve the grid stability.

The power electronic converter interfacing with the renewable energy source and the grid should be reliable, efficient, and configurable for which multiple control techniques, topologies or converter configurations must be explored to extract the maximum power. Also, the interface converter must be capable of bidirectional energy transaction as and when required. Many configurations interfacing the distributed energy sources to the grid with different control techniques are possible with the system operation in either, grid connected mode or off grid mode.

In this thesis the study is done to investigate the means and methods for enhance the dynamic performance of the grid interfacing inverters along with studying the influence of connected DC – DC converter on DC bus of the inverters for the transient dynamics, and issues of synchronization / resynchronization of inverters to grid and interventions of DC side converters and adaptive control to offer effective parallel operation of inverters.

The following sections and sub sections gives an insight of the state-of-the-art photovoltaic converter interfaced with the grid through a converter / inverter topology. In addition, the issues of synchronization and resynchronization of the inverter with the grid are presented. Further the dynamic performance of grid connected parallel inverters is also investigated.

1.2. Solar Photovoltaic System : Issues and Opportunities

The photovoltaic energy source is abundantly available clean source of energy; however, the panels have very low efficiency when it comes to the conversion of solar energy to electrical energy. It is essential to extract the maximum possible power from the solar panel using an MPPT charge controller using algorithms like Perturb & Observe (P&O) and Incremental Conductance (InC) algorithm.

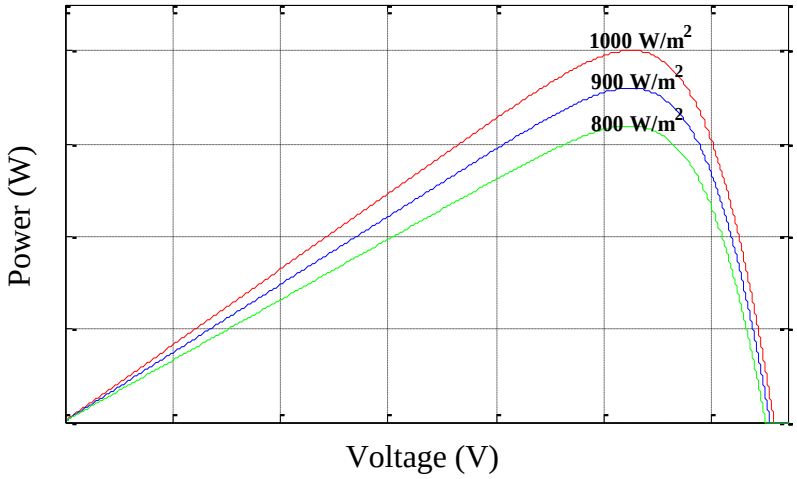


Fig. 1.1 PV Characteristics of Photovoltaic Panel with variation of irradiance

A few topologies have been studied upon and published over the years, be it isolated or non – isolated with focus on cost, efficiency, and reliability of operation. Isolated

converters offer galvanic isolation with capabilities of high gain through interfacing transformer but at an additional component count and cost. The conventional non isolated converters on the other hand lack the isolation and high gain capability but are less complex and easy to execute. For effective use the developed power is further inverted from DC to feed power into the AC load, the microgrid, the distribution network, and or to the entire fed through the national grid connected, islanded mode operation in off grid configurations as shown in Fig. 1.1 and Fig. 1.2.

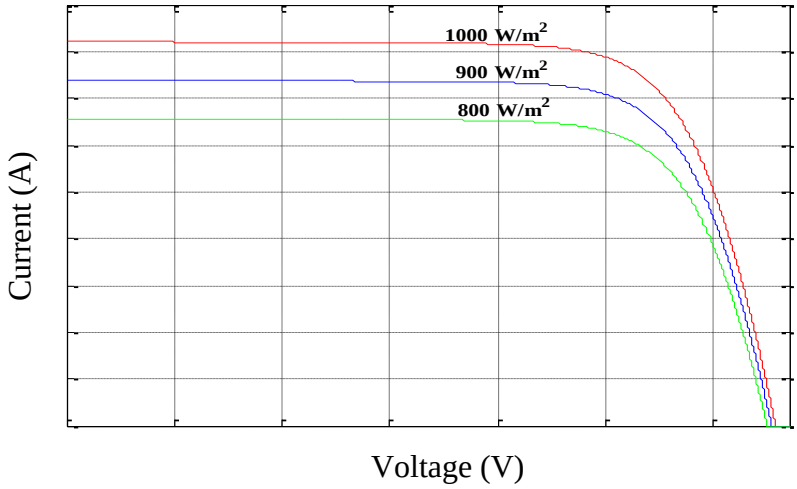


Fig. 1.2 IV Characteristics of Photovoltaic Panel

The following sections deals with challenges encountered, configurations they are connected and added to provide requisite DC voltage to enable the inverters for grid coupling at an appropriate voltage.

1.3. PV String and Array : Challenges

PV panels exhibits a typical non-linear I-V and P-V characteristics as shown in Fig.1.1 and Fig. 1.2 respectively. With the output power varying with variation in irradiance and temperature conditions, the output current of the panel being dependent on the irradiance varies and the output voltage being dependent on the panel temperature varies, a typical variation as shown in Fig. 1.3 and Fig. 1.4. The PV panel being comprised of many single solar cells units connected in series and in parallel to offer power at requisite voltage and

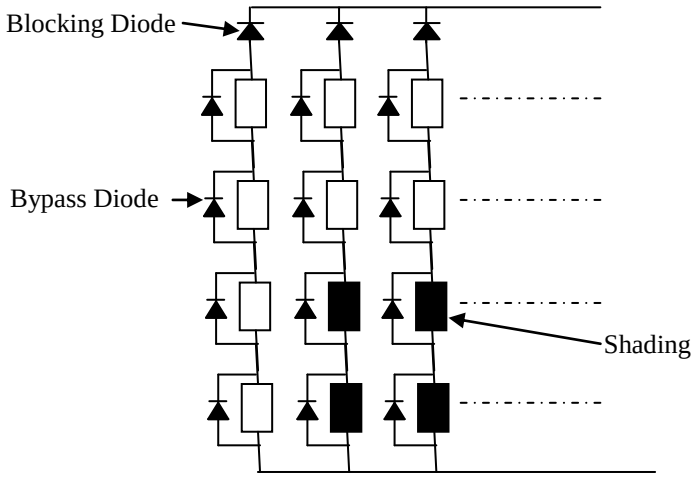


Fig. 1.3 Photovoltaic Panel Configuration and Partial Shading

current levels, thereby panels are made by connecting these cells in series and parallel. And to match the upfront connected power electronic converters and inverters PV panels are connected in series and parallel to form an array to offer adequate DC voltage and current. If number of panels is increased in series, it leads to increase in open circuit voltage and when paralleled it increases the short circuit current of the PV arrays. For extracting maximum power and maximize the utilization of the solar panels, various global MPPT (GMPPT) are advocated in literature for operation at GMPPT under partial shading and shading of PV panels in strings since the power generated by the string under shading of panel / partial shading of the panel a voltage drop is witnessed at the terminals of string / parallel, appropriate voltage gain of the string MPPT controller would be a requisite to avoid knocking out of string from the PV array.

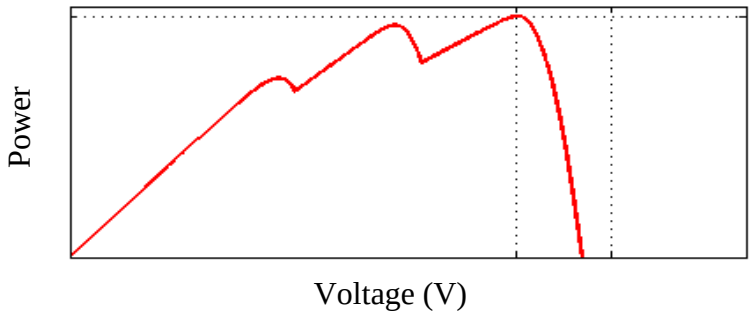


Fig. 1.4 PV Characteristic during Partial Shading

1.4. Converter/Inverter Configurations for the PV System

Power Electronic converter and inverters are the enablers for transacting PV power into the grid. The conventional grid integration is based on centralized inverters which interfaces many PV modules placed in the form of an array to form a DC link appropriate for directly coupling to the grid through inverter acting in current control mode and voltage control mode respectively in single stage or two stage configurations as shown in Fig. 1.5 or 1.6 [3]. Parallel strings of PV panels are connected to generate sufficiently high voltage to avoid the requirement of amplification by converters in single stage configuration. But the main problems associated with these centralized single stage inverters lies with high-voltage dc cables between the PV modules and the inverter, power losses due to a centralized MPPT, mismatch losses between the PV modules and losses in the string diodes, partial shading / shading of panels in the string.

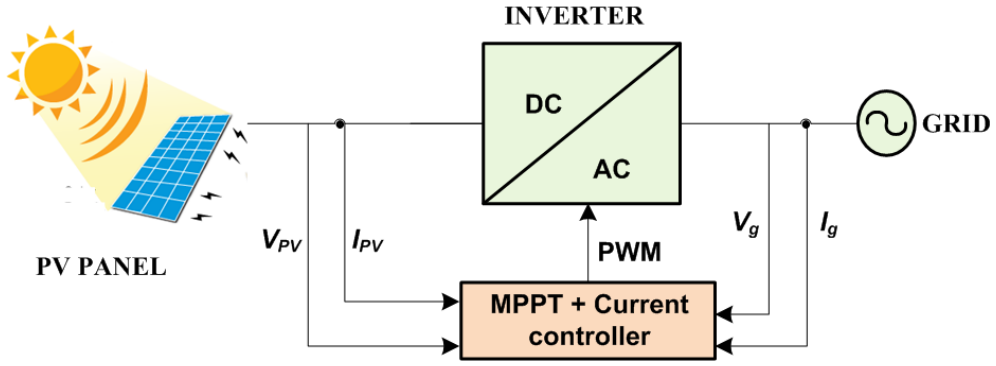


Fig. 1.5 Single Stage Configuration interfacing DER to Grid

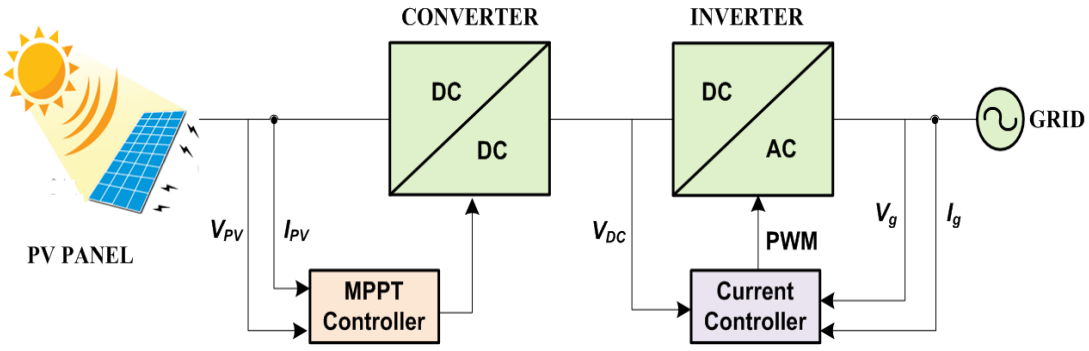


Fig. 1.6 Double Stage Configuration interfacing DER to Grid

Sometimes in the absence of sufficient number of panels and or deliberately for increasing the reliability against shading / partial shading the requisite voltage, is built up through DC-DC boost type converters between the sub sections of string of PV panels with separate MPPT controllers and the inverter making them operate in the two-stage configuration while all such modified string connected to grid in parallel as shown in Fig. 1.6. In double stage mainly isolated or non-isolated DC-DC converters are used in conjunction with voltage source inverter (VSI). Isolated topology though enhances the overall cost of the system, but provides an additional advantage in terms of isolation, which avoids leakage current, preventing occurrence of hazardous situations. For the low wattage off grid PV systems, low-cost non-isolated converters are often preferred.

Recently module integrated converters (MIC) have gained popularity, where in the generated power is transformed to grid coupling compatible, thereby making them capable of avoiding the mismatch losses between PV modules in the string since there is only one PV module to which it caters to, and it also facilitates the individual MPPT, thus enhancing the efficiency and reliability. However, MIC for single PV module is being used; it requires high amplification to match the grid voltage making it a slightly costly proposition.

2 – Level / 3 - Level multi-string / single string inverters are popularly deployed in the field. The topology for multistring inverter consists of several PV strings, each connected with separate DC – DC converters to a common DC – AC inverter [4 – 5]. This topology features several advantages such as the independent tracking of the MPP of each string and the possibility to scale the system by plugging more strings to the existing plant. But the power output suffers a lot under partial shading condition. Further the losses and stresses on switches are quite high due to the high voltage condition prevailing on single DC link capacitor. Due to the heavy power transaction across common capacitor, its capacitance is generally kept being at very high value which due to large stress deteriorates early causing lessening life of the PV system. The classical two-level VSIs is mainly limited to low- or medium power level applications due to the limits of the power-semiconductor switches used in the configuration.

1.5. DC – DC Converter

The interfacing DC – DC converter plays a vital role in extracting the power from the photovoltaic panels and feeding it to the DC bus of the inverter, which in turn feeds it to the distribution grid. A simple and cost-effective converter mostly interfaced with a PV system is boost converter, however the conventional boost converter may witness more than the allowable stress under partial shading conditions leading to failure or breach of design [6-7].

To improve the efficiency of the converter and reducing the stress over the components interleaving of converters have been reported, while for high gain requirement, incorporation of multiplier cells or cascading of converter topologies are proposed. Such modifications enhance the operating band of the converter. Isolated topologies provide an alternative for with boosting capabilities by altering the turns ration of the isolating transformer. Non isolated boost converters based on impedance converters have also been investigated with the capability to operate during shoot through and providing auxiliary boost [8].

1.6. Voltage Sourced Inverter

The output power generated from the PV panel is low voltage DC in nature, which is scaled up to maintained at the required level of voltage and power by appropriately connecting them in parallel / series. The inverter in the single stage configuration can be interfaced with the distribution grid directly [9], while in two stage configurations through an interface converter. In single stage application the DC bus voltage level need to be maintained at a higher value by PV string, and the inverter in turn to performs the maximum power tracking and power transfer to the distribution grid by appropriately controlling the current drawn from the PV string as shown in Fig. 1.7. Though single stage configuration eliminates the need for extra DC – DC converter, but during voltage sag condition the instantaneous increase in the PV system current momentarily decrease in the DC link voltage and thereby shifts the operating point towards I_{SC}, leading to collapse of power generation from the string, unless and until DC link is provided with adequate hold up capacitor / STATCOM connection at the PCC.

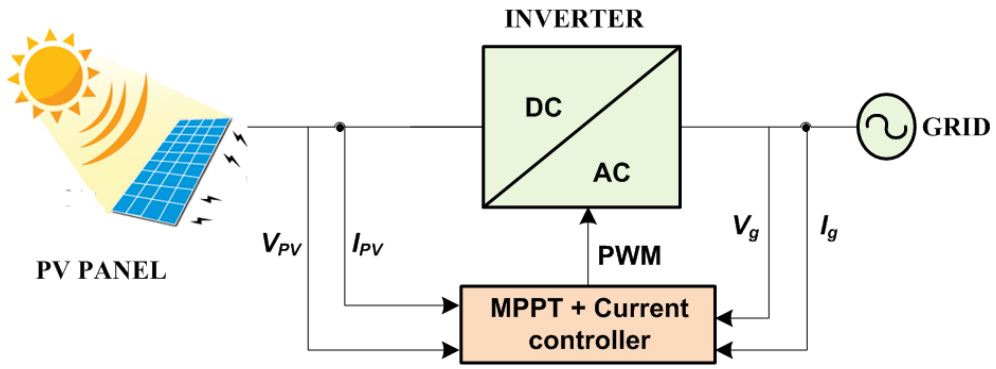


Fig. 1.7 Single Stage Configuration

In two stage configurations as shown in Fig. 1.8, the photovoltaic voltage is either stepped up or stepped down through the interfacing DC – DC charge controller as per the requirement of the system [10-11]. The DC power is converted into AC using an inverter interfacing the DC output of the charge controller with the grid. The interfacing inverter pushes the power generated from PV panel / PV string to the AC distribution grid and in turn to the connected loads.

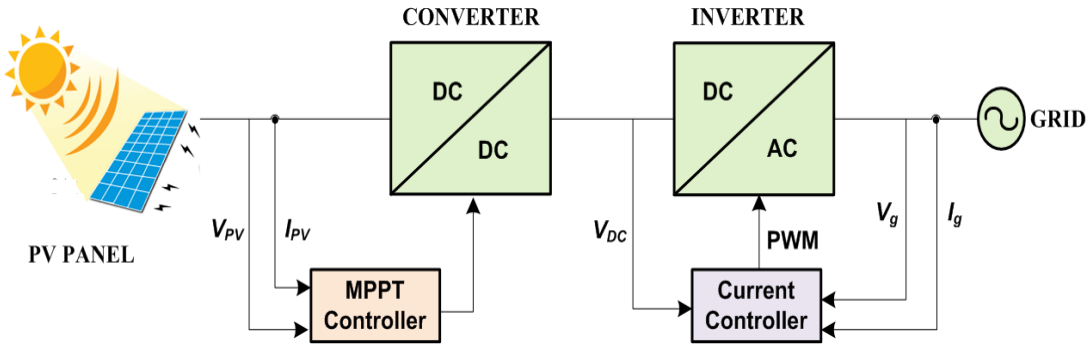


Fig. 1.8 Dual Stage Configuration

In addition to power transfer from DC link to AC distribution grid the interfacing inverter is often entrusted for multitasking. Some of the additional tasks carried out are [12–13] -

i. Active Filtering –it can act as an active filter injecting a specific current at the PCC for mitigation of harmonics and thereby improving the power quality of the complete system working on the remaining capacity of hardware.

ii. Power Conditioning – The inverter helps in a controlled exchange of energy between two electrical units. The control of the inverter switching sequence is to ensure that

parameters like voltage magnitude, frequency, current magnitude, power factor and Total Harmonic Distortion (THD) are maintained as per the requisite specifications and standards.

iii. Compensator – the voltage source inverter acting as a power compensator helps increase the power transfer capability, efficiency of power transfer, efficiency of power transfer in distribution grid. The inverters can be used series compensators or Static Synchronous Compensator (STATCOM).

Inverter interfacing unit converting the DC to AC helps in increasing the depth of penetration of renewable distributed energy sources in an efficient and reliable way with the existing power infrastructure.

1.6.1. Voltage Sourced Inverter - Configurations

The basic inverter configuration is the half bridge inverter as shown in Fig. 1.9, consisting of an upper and lower switch with an antiparallel diode and interfacing inverter for connection to the grid. The DC voltage is maintained by the DC link capacitors at the input side which is in turn fed from the MPPT charge controller, energy storage system (ESS). The fundamental component of the output voltage of the inverter is controlled by the switching sequence of the inverter. However, such configuration is mainly used for coupling it with the grid, since it requires very high voltage to be maintained at the DC link, and possibilities of injection of DC components to the grid.

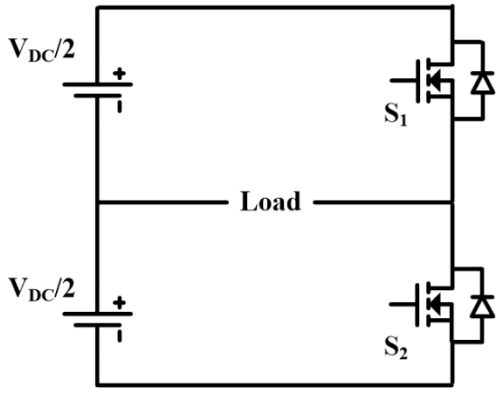


Fig. 1.9 Half Bridge Inverter Configuration

Two half bridges connected in parallel at the input DC side constitutes the full bridge configuration of inverter, also known as full bridge / H bridge inverter having two legs. An extension of H – bridge inverter with 3rd leg is presented for 3φ systems and is shown in Fig. 1.10. The three-phase voltage sourced inverter interfaces the input DC link to the 3-phase grid through interfacing inductors. If the configuration required is that of a 4-wire system, the neutral wire is attached to the midpoint of the series side capacitor on the input side.

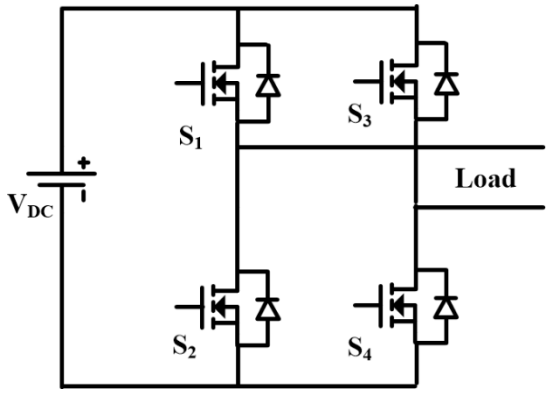


Fig. 1.10 3 Phase Full Bridge Inverter Configuration

1.6.2. Control Techniques of the Voltage Sourced Inverter

The interfacing voltage source inverter (VSI) can operate in either grid connected mode or off grid mode. In off grid mode the inverter output is not connected to the grid, and thus need to operate in voltage control mode to control the voltage and frequency fed to the load.

While. in the grid connected mode, the configuration can be master slave mode where the distribution grid acts as master and governs the voltage and frequency at the Point of Common Coupling (PCC) while the VSI injects the current, or in all master mode, where the VSI also acts as a voltage source and transfer by altering the lead angle with respect to voltage at PCC. Generally, the inverter is employed as current controlled VSI, thereby pushing current equivalent to the power generated by the photovoltaic panels or while witnessing near constant voltage at AC side. The most common control technique for switching of VSI in grid connected mode are Hysteresis Current Control (HCC) in master

slave mode and Sinusoidal Pulse Width Modulation (SPWM) for connection of VSI as voltage controlled VSI [14].

1.6.2.1. Hysteresis Current Control (HCC)

The hysteresis current control compares the reference sinusoidal current with a tolerance band having an upper and lower limit as shown in Fig. 1.11, the switch transitions from ON state to OFF state and vice versa based upon the current waveform reaching the upper and lower thresholds. The switches in a leg of VSI are turned ON and OFF based on the corresponding current threshold. The operating state is reversed when the actual current reaches the other threshold. The control algorithm is simple to implement with very less computation required. However, the transition of the switches from ON state to OFF state is dependent on the slope change of slope of current transition and threshold limits set, thus resulting in operation of the inverter at a switching frequency which may vary with change of the slope if current in sinusoidal and / or parametric variations.

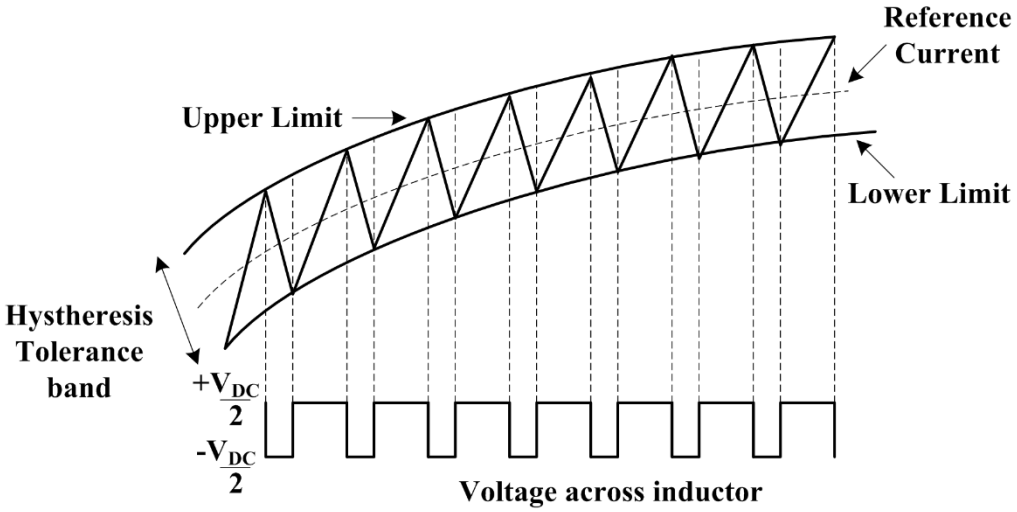


Fig. 1.11 Hysteresis Current Control (HCC) Technique

1.6.2.2. Pulse Width Modulated Control –

Pulse width modulation technique employ control on the modulation index to control the output magnitude of voltage and phase level by a corresponding modulating signal as given by (1).

$$v_t = mV_{DC} \quad (1)$$

The sinusoidal waveform acts as the modulating signal and is compared with the high frequency carrier signal. The reference current is compared to the actual current and the error is compensated using a PI controller. The reference current for the control is governed by the power generated from the distributed energy source at the DC side. The compensator output after decoupling is converted to switching pulses as per desired modulation index based on (1). The feed forward component also helps in establishing robust response of the control loop. The control technique maintains the switching frequency equivalent to the carrier frequency but suffers from the control complexity and computation requirement as shown in Fig. 1.12 and Fig.1.13.

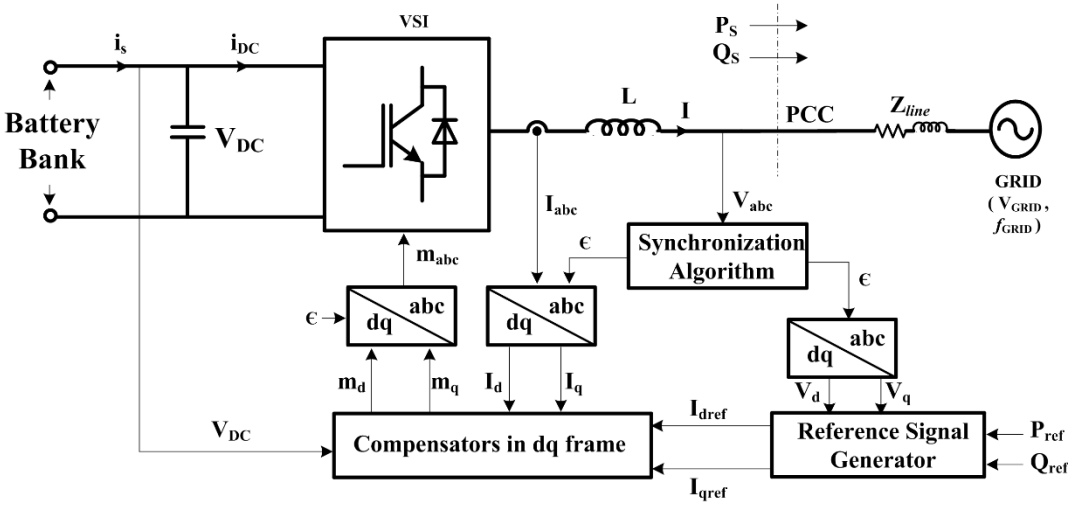


Fig. 1.12 SPWM Control of VSI

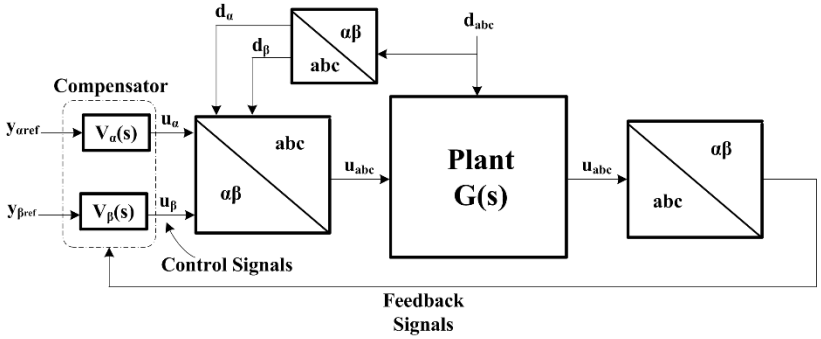


Fig. 1.13 SPWM Control Technique

1.7. Parallel Operation of Inverters

To meet the increasing load demand with aim to reduce the carbon footprint, power generated based on DER's is gaining importance. To meet the load demand, parallel operation of inverters in a microgrid is essential. The parallel operation of the inverters can be investigated separately into operation during off grid mode or grid connected mode.

During off grid mode the voltage and frequency at the connected loads are maintained by the interfacing inverter, with the master inverter operating in voltage control mode maintaining the voltage and frequency at Point of Common Coupling (PCC). Other interfacing inverters are synchronized with the master inverter and are attached to the PCC as current controlled sources behaving as slaves following the frequency and voltage set by the master. The most critical component for interfacing of multiple inverters in parallel is the robust synchronization of the inverters. It is requisite that all the parallel operating

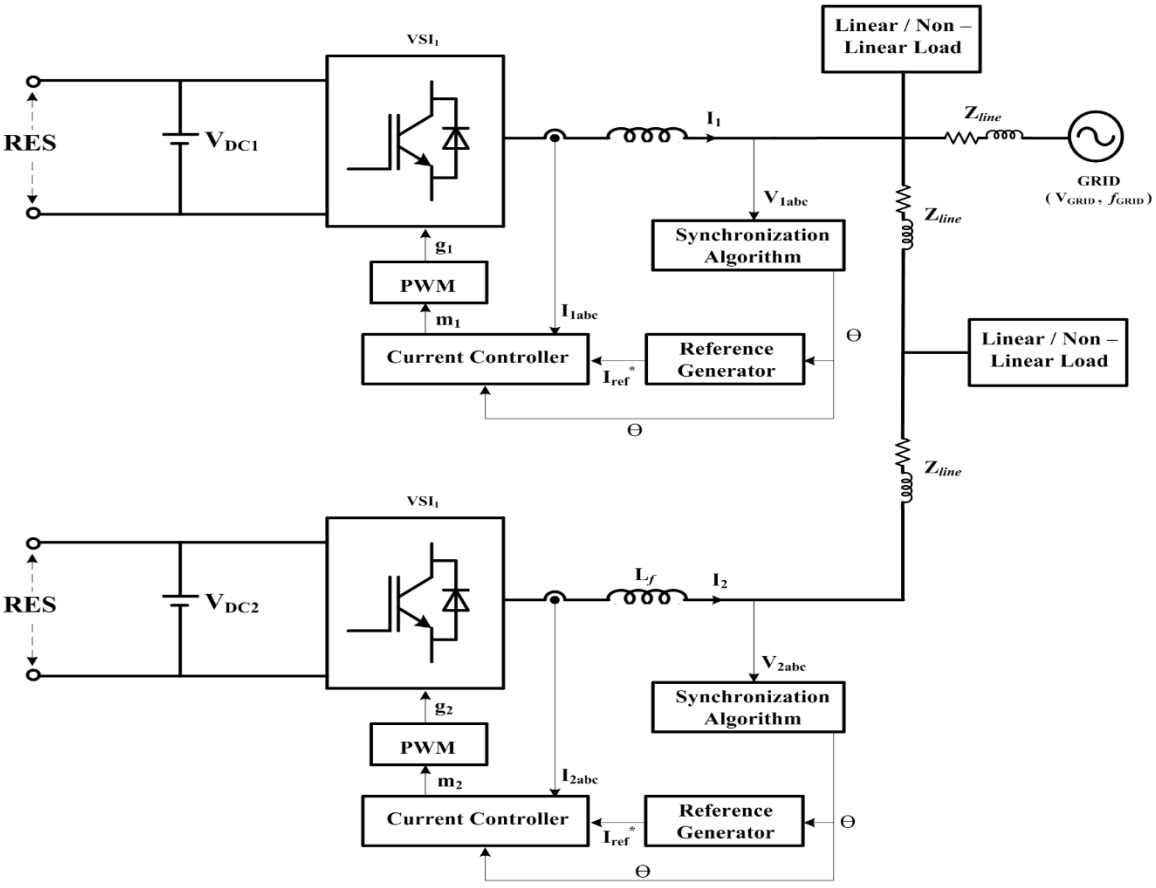


Fig. 1.14 Parallel Operation of Inverters

inverters should operate in synchronization, maintaining the output parameters within the required standards. Parallel operation of inverters during off grid mode may experience

circulating currents among themselves due to differences in the response of PLL, hardware parameters and / or the switching sequences.

In grid connected mode, all the connected multiple inverters generally operate in slave mode, pushing the power generated at their input sides to the connected grid in terms of equivalent current where the grid is acting as master and maintaining the voltage and frequency at their respective PCC's as shown in Fig. 1.14. However, during disturbances either at the grid side or at the DC input side, high transients and circulating current flows amongst the inverter bridges. This high di/dt and high dv/dt transients damage the switching devices of the inverters leading to collapse of the system. High circulating current can also be experienced if one of the inverters goes out of synchronization, leading to its failure.

An investigation is therefore due for impedance source based MPPT charge controller at the DC side which can act as an impedance network, which can enhance the transient performance of the system. In addition to limiting the flow of circulating current by imposing an additional impedance at the DC link.

1.8. Synchronization and Resynchronization

The phase locked loop ensures precise synchronization of the interfaced inverter with the grid along with providing ride through capability, and accordingly plentiful attention is requisite for investigation into synchronization algorithms. Unit template-based synchronization algorithm determines the sine and cosine synchronizing signals for balanced grid conditions. However, under perturbations the grid voltage and frequency change, making loss of synchronization among inverters is found inevitable and thereby compromising the current references and the control algorithm of the concerned inverter. Conventional synchronization algorithms like Synchronous Reference Frame Phase Locked Loop (SRF – PLL) based on inverse park transformation show fast synchronization response only under balance conditions. To improve the dynamic performance of SRF – PLL, Amplitude Normalization Scheme (ANS) is integrated in the algorithm while to improve the filtering capability by modifying the integrator of low pass filter (PI controller). While, to improve the filtering capability of the PLL, Moving Average Filter

(MAF) is also investigated in the algorithm. Second Order Generalized Integrator (SOGI) acting as a Quadrature Signal Generator (QSG) in addition to its capability of providing infinite gain at a particular frequency with robust performance put the algorithm, in a class apart.

It is important that that the synchronization algorithm should be capable of detecting and adapting to curbing the intermittent conditions on the grid in least possible time, besides exhibiting the capability of accurate transient tracking i.e., the response of the synchronization algorithm should match the fast dynamics of the low inertia inverter assuring the ride through capability in addition to complying with the grid codes. Furthermore, the frequency adaptive algorithms should also allow co – operative synchronization of inverters having different dynamics (due to type of hardware/type of controllers), generating distortion free reference, and nullifying the circulating current flow between the inverter modules.

A microgrid with multiple inverters faces several bottlenecks when it comes to mode transition from grid forming to grid connected mode and vice versa. The level of uncertainty varies with the number of generators at the instance of grid outage and grid return and can lead to a mismatch in the power generation vis a vis power demanded. In case the grid goes out with ‘n’ inverters in generating mode and returns with ‘n+i’ connected inverters meeting the load demand, then the incoming inverters ‘i’ are not required to operate at its maximum capacity. Moreover, while resynchronizing with the grid at PCC, it is mandatory that the incoming inverters has to have a slight leading phase angle if inserted in voltage mode, such that it can feed the necessary power to the grid and avoid becoming a load to the grid. In addition to grid synchronization problems, the problem of transient currents during mode transition is also a major concern. In grid forming mode, where the inverter is tasked to maintain the grid voltage at the nominal frequency, inter converter circulating current is another deterrent. Inverters operating at different dynamics like phase/frequency and having different physical parameters can cause interaction of inverters in the microgrid.

A synchronization and resynchronization algorithm enhancing the dynamic performance of a grid interfaced inverters and for limiting the flow of circulating current among the inverters during the transition from grid connected mode to off grid mode and vice versa is requisite for deep investigation.

1.9. Scope of the work

It has been noticed that for cordial operation of the parallel connected inverters, especially during grid fluctuations multiple factors play a crucial role. Perturbations in the irradiance, partial shading of the panels require high gain resulting in reduced operating efficiency of conventional MPPT interface converters like boost converter. Also lack of thevenin equivalent output impedance in boost converter limits the elimination of the spikes / transients become inevitable on the DC link and thus reflects on reference control parameters of the inverter. A converter based on LC impedance network with auxiliary boost technique should be envisaged as a befitting solution, which can damp the disturbances arising from the input side amicably. In addition, the impedance network can also pose impedance in the path of the circulating currents if at all these are arising due to mismatch in the operation of parallel connected inverters. Secondly, a synchronization algorithm with fast dynamics and robust response reduces the impact of disturbances observed in the inverter control parameters arising from the grid / microgrid side. Further, the fast and robust synchronization and resynchronization algorithm helps in smooth transition of the inverter from grid connected mode to islanded mode and vice versa. The prime focus of the study is to work on the above points resulting a robust grid connected system with fast dynamics both in grid connected and off grid mode of operation. Based on the above points the key challenges taken into consideration for operation of PV fed parallel inverters in a microgrid are –

1. Incorporation of impedance through interfacing DC – DC converter to curb the spikes observed at the DC link and circulating currents in parallel operating inverters.

2. Synchronization algorithm with fast dynamics
3. Resynchronization algorithm with fast transition capability from on grid mode to off grid mode and vice versa.

1.9.1. Wide Operating Impedance Converter for Photovoltaic Application

A DC – DC converter based on the T Source impedance network is investigated. The investigated impedance converter is a non-isolated converter operating with incremental conductance (InC) maximum power point tracking algorithm, realized through a low cost 16-bit dsPIC33F micro-controller. The proposed converter based on a half bridge topology allows operation in shoot through mode (upper and lower switch ON) providing an auxiliary boost capability at higher gain conditions. The auxiliary boost significantly reduces the operating stress on the switching MOSFET's during low input voltage conditions (partial shading / discharged battery) also reducing the voltage stress on the switches. The developed converter provides floating ground at the output eliminating the path for the ground currents. The proposed converter being a continuous input current converter unlike the conventional T source and Z source impedance converter allows superior tracking of the maximum power point for the power extraction of the PV panel(s).

1.9.2. Bidirectional Impedance Source Converter for ESS

While investigation on the impedance source converter for MPPT applications, a bidirectional DC – DC impedance source converter is also investigated. Such bidirectional impedance converter holds the advantage of operating in shoot conditions, through similar to the wide operating range impedance source converter, providing an auxiliary boost, in turn reducing the stress across the converter during discharge conditions. Moreover, the bidirectional impedance source converter being multiport it allows installation of multiple battery packs for the charging / discharging cycle with the capability of charging / discharging at different rates.

1.9.3. Interfacing impedance converter with the distribution grid and impact of impedance converter on the grid disturbances

The series connection of the impedance source converters is managing the DC link voltage of the voltage source inverter (VSI) is interfaced with the central grid operating in current controlled mode. The dynamic capability of the series connected impedance source converters is validated through simulation under the perturbations of irradiation change and sectional partial shading on its input side. The impedance source converter string efficiently feeds the DC link under these extreme perturbations, even under presence of bypassed panels due to partial shading.

1.9.4. Fast tracking synchronization algorithm for grid synchronization

Synchronization algorithm based on Second Order Generalized Integrator (SOGI) based adaptive filter, resonating at second harmonic frequency i.e., 100 Hz is developed. The double frequency adaptive filter ensures the improved phase and amplitude gains at greater nominal frequency, expanding the stable operating region. The adaptive filter resonating at 100 Hz reduces the system settling and damping time, along with limiting the transient overshoots and undershoots, hence improving the transient tracking capability of the system. Taking 2^{nd} harmonic frequency of 100 Hz as the resonating frequency curbs the low harmonic resonance observed under perturbations and weak grid conditions. The synchronization algorithm is investigated for various grid perturbations resembling a weak grid condition. Its comparison with conventional SOGI – PLL is also investigated.

1.9.5. Resynchronization Algorithm

A synchronization algorithm-based control for seamless transition to/fro between grid connected mode and grid forming mode using an adaptive droop controller in islanded mode, and through PI compensator operating on circuit in grid connected mode is

developed. Besides limiting the transient current and voltage spikes, the algorithm is additionally investigated for providing stringent control over the power flow among inverters. The synchronization algorithm utilizes SOGI QSG resonating at the reference frequency obtained from the adaptive power frequency droop in grid forming mode. The reference frequency in conjunction with the power sensed at the inverter output terminal, restricts any inflow of circulating current. Moreover, the algorithm retains the last phase value when transitioning from grid connected mode to grid forming mode, enhancing the dynamics of the transient response. On resynchronization with the utility grid, frequency and phase deviations experienced are investigated for regulation through the compensator in the phased locked loop.

1.10. Organization of Thesis

Following this introductory chapter, the work in this thesis is organized as follows:

Chapter-II: In this chapter a brief literature review of state-of-the-art DC – DC converters for photovoltaic applications is presented. Further it also includes the review of various control techniques used for parallel operation of inverters, the synchronization and resynchronization algorithms proposed over the years.

Chapter-III: In this chapter a study on the wide range photovoltaic interface converter based on continuous current T impedance network is presented. The proposed converter based on a half bridge topology allows operation during shoot through mode (upper and lower switch ON) providing an auxiliary boost capability to offer higher gain conditions. The study also shows the advantage of auxiliary boost in significantly reducing the operating stress on the switching MOSFET's during low input voltage conditions (partial shading / discharged battery) besides reducing the voltage stress on the switches. Based on the developed impedance converter, a study on bidirectional DC – DC impedance source converter is also developed. Such bidirectional converter being multiport allows installation of multiple battery packs for the charging / discharging cycle with the capability of charging / discharging at different rates.

Chapter-IV: In this chapter a synchronization algorithm based on the Second Order Generalized Integrator (SOGI) adaptive filter resonating at double frequency is presented. The double frequency adaptive filter ensures the improved phase and amplitude gains at greater nominal frequency expanding the stable operating region. The adaptive filter resonating at 100 Hz reduces the system settling and damping time, along with limiting the transient overshoots and undershoots, hence improving the transient tracking capability of the system

Chapter V and Chapter VI: In this chapter a synchronization algorithm-based control for seamless transition to/fro between grid connected mode and grid forming mode using an adaptive droop controller in islanded mode, and PI compensator in grid connected mode with protection against circulating current is presented.

Chapter-VII**:** In this chapter the impedance converter is interfaced with the DC link of voltage source inverter (VSI) which in turn is interfaced with the distribution grid. The developed MPPT charge controller at the DC side acting as an impedance network enhances the transient performance of the system during perturbations observed at the DC side like irradiation change or partial shading. In addition, the efficacy of thevenin equivalent impedance of the proposed impedance converter is shown to limit the flow of circulating current within the system.

Chapter II

LITERATURE SURVEY

2.1. General

The increasing power demand has posed a huge burden on the existing distribution grid infrastructure. The residential loads have become a major consumer of the available power. To meet the growing energy demand local photovoltaic generation and consumption is encouraged by using power electronics interface for higher efficiency and adequate control. The PV and balance of the system for efficient power extraction in on grid/off-grid mode requires, various topologies of voltage converter, remediation of the issues related to PV system and the same have been envisioned as scope of the work. In this chapter a brief on the advancement of PV technology, an insight view of state – of – the – art technologies for various converters suitable for PV system is presented to pinpoint the objectives of the research.

The interfacing voltage source inverter is vulnerable to disturbance both from grid side and from the renewable energy source (input) side, having intermittent solar influx, partial shading of the photovoltaic panel, different wind speeds, low battery voltages etc. The disturbances at the grid side can be mitigated through the reactive power-based control of the interfacing inverter and appropriate synchronization algorithm with fast tracking capability. However, as per the scope of thesis work, the literature is explored corresponding to PV fed inertia and their operational issues while they operate in parallel connected to the low voltage grid / microgrid.

2.2. Survey of the Literature for PV Fed System

The literature review for PV including system interfacing DC – DC converters, grid interfaced converters; control of parallel inverters and synchronization algorithm are

discussed and through extensive survey of literature as per the research objectives are drawn in previous chapter.

2.2.1. Solar PV Balance of System

Solar photovoltaic (PV) power is one of the most widely used green and clean renewable sources for generation of electric power to fulfill the ever - increasing demand of the utility [15]. Major challenge for harnessing the energy rests with generation cost/wattage, availability of source, reliability compared with other power sources based on fossil fuels. With exponential growth in semiconductor technology cost of PV module and its balance of the system (BoS) have gone down steeply, and the trend is continuing, hence it makes PV based generation, a prospective future for system [16].

The PV cell follow non-linear I-V and P-V characteristics, which also vary with insolation and temperature change. The characteristics get more complicated if the entire array does not receive uniform insolation, as in partially cloudy (shaded) conditions, resulting in multiple peaks [17-18]. The experimental validation of the effect of shading is shown through I-V and P-V characteristics. Numerical algorithm to study the effect of mismatch of varying insolation on individual PV panel cells is also reported in literature [19]. Few authors have investigated the effect of shading of the PV plant on grid and concluded that it may have financial implication and may also lead to instability of the utility [20] [21]. The estimation of the power output at different operating conditions, viz, insolation change and temperature change, which often is not feasible in real time practical PV panels. To cope up with such problem, many researchers have proposed mathematical modeling of the PV panels in MATLAB to closely approximate with the actual PV panel characteristics [22].

2.2.2. MPPT Techniques for PV System

With rise in temperature, the conversion efficiency of PV modules goes down drastically, whereas generated power changes with change in insolation conditions. The generated power, if not evacuated but allowed to free wheel inside the PV module, would

unnecessarily heat the panel and adversely affects its generation efficiency [23]. Moreover, the cost of PV modules is quite high so there is need for maximum power point tracking (MPPT) and invoke complete evacuation of power from PV modules for maximizing the system efficiency. Various MPPT techniques are reported in literatures wherein, perturb and observe (P&O) method is most widely used due to simplicity of algorithm and its easy implementation [24 – 25]. Though the MPPT technique based on the P&O algorithm is widely used, its performance is very ordinary due to the following problems: (i) its dependence on the step size: a small step size restricts the system with slow dynamics, while a long step size cause low efficiency; (ii) oscillations around the MPP in both transient and steady-state operations; (iii) local minima tracking (LMT); and others [26]. Amidst varying insolation conditions, the Incremental conductance (INC) method is reportedly performed to effective tracking of the MPP [27 – 28]. The INC MPPT algorithm usually has a fixed iteration step size determined by the requirements of the accuracy at steady state and the quickness of the response of the MPPT. For fast tracking and efficient control fuzzy logic base MPPT controller is also reported [29]. In [30], neural network algorithm is utilized for MPPT in which thorough proper training with data, optimal MPP is reached.

Due to the availability of multiple local and global peaks, the conventional algorithm fails to track MPP under partial shading condition [31]. In [32] algorithm for partial shading works well with multicell high voltage application, but fails to extract power from individual cells, and the tracking speed has not been reported fast. Others have also proposed a tracking algorithm based on power estimation for both under grid and off-grid modes [33]. Some of the reported algorithms employ metaheuristic optimization methods such as particle swarm optimization (PSO) [34]. But most of the algorithms are quite complicated and needs multiple iterations along with scanning.

2.2.3. MPPT Charge Controllers

A simple and cost – effective converter mostly interfaced with PV system is boost converter. For cases like shading of a portion of panel, the global maxima may be found at

lower voltages thereby, pushing the converter to its operating limits. With increasing duty, cycle stress, the converter may lead to conditions that may surpass the rating leading to failure/breach of design.

To improve the efficiency of converter and distributing the stress, interleaving of converter is adopted [35]. Interleaving of channel enhances the efficiency but doesn't significantly improve the operating region of the converter. The use of high gain topologies, incorporating multiplier cells [36-37] or cascading topologies [38-39] improves the operating band at the cost of increase in component count and converter size. On the other hand, isolated converter topologies also provide an alternative, where the boosting ratio is chiefly governed by transformer ratio. With the benefit of isolation between input and output, isolated converter may also suffer from the requirement of high turns ratio while witnessing lower voltage which increases the design considerations and converter size.

Non isolated converters incorporating input impedance network having the ability to incorporate auxiliary boost in voltage, holds the key to improve the operating bandwidth on the I/V characteristics of the PV panel. Nominal topology of Z source network suffers from discontinuous input current operation, making it unsuitable for PV applications [40]. However, boosting in voltage with such impedance networks could alternatively be achieved using coupled inductors, as T-type converters [41-42-43] devising power dense solution with higher throughput of energy along with flexibility of auxiliary boost. However, these too extract discontinuous input current from PV panels. Γ- Source [44] and Y – Source [45] based converters rely on magnetically coupled inductors for auxiliary boosting but suffer from discontinuity in input current during shoot through state. The Y – Source impedance converters with three inductors and a capacitor establishes a degree of freedom which allows the enhancement of the gain for both increase and decrease of the operating duty. However, the increased number of inductors in Y – Source converter affects its power density. On the other hand, Quasi-Z source [46], Quasi-T type network and quasi-Y Source [47] rectifies the problem of input side current discontinuity through bypassing the input side diode during shoot through state. However, the introduction of bypass capacitor affects the characteristic of panel hence these topologies do not form a befitting

solution for PV applications. Moreover, all the above discussed impedance converters suffer from high voltage stress on the switches used in different topologies.

2.2.4. Bi – Directional Converter

Bidirectional converters utilizing buck boost converter topologies are used to provide a modular and low-cost approach. However, under high step up / step down demands, they experience significant drop in efficiency, besides causing faster deterioration of battery life due to discontinuous current with high current ripple. Several non – isolated bi – directional converters with significant buck boost capabilities have been reported [48-50], these configurations however have increased switch counts and capacitors which significantly complicate the system. In [49], the authors have proposed a bidirectional converter with the control being executed through a complicated and costly fuzzy controller. Moreover, cascading, and multilevel architectures for obtaining wide operating range, affects the system efficiency besides complex control design. Bi-directional converter topologies based on galvanic isolation provided by the transformer, like Dual Active Bridge (DAB) and resonant converters like CLLC having high gain capabilities. circumvent the drawback of discontinuous input current and limited operating range [51-53]. However, these topologies are costly, complex, and bulky solutions. Moreover, bidirectional operation of converter is hindered by low impedance seen by on the current when flowing from high voltage to low voltage side resulting in peaky current across the transformer, possibly saturating the transformer core.

Under practical case where batteries with different SoC's are stacked together, the battery with lower SoC tends to load the healthy batteries, thus requires additional equalizer/ balancer circuits which increases the cost and complexity of converter. Multiport topologies [54], allow battery stacking based upon the number of inputs on a single converter with simpler solution. In [55 – 57], the authors have presented multiport topologies for electric vehicle and photovoltaic applications, the multiport converters fail on optimizing the power utilization from individual input source with limited operating band. Also, under different SoC conditions or input conditions, converters discussed, both

non-isolated and isolated are incapable to charge the batteries stacks at different rates. The magnetically coupled inductors utilized in impedance source converters capable of providing additional boosting during intermittent operation provide wide operating range without deteriorating the efficiency [58-60]. The architecture using coupled inductors for energy storage and transfer allows power dense and modular solution. T-source network and Z-source network suffer from discontinuous operation and lack bi-directional operation capability, while Quasi Z- network, provides a continuous input current but remains unidirectional in operation. Thereby, auxiliary boosting capability of the impedance converter together with the possibility of bi – directional operation and fast dynamics is yet to be explored.

2.3. Grid Connected Voltage Source Inverters

The literature reveals that primarily two types, namely grid "grid forming" and "grid following" inverters are used for grid coupling. Voltage controlled grid forming inverters are generally proposed for large power plant and are coupled to higher voltage levels feeding comprehensively to loads connected through downstream feeders, whereas current controlled grid following inverters are suitable for coupling to relatively lower voltage levels and are very widely used. The major issues related to grid coupling of inverters hovers around synchronization / re – synchronization and circulating currents while in parallel operation.

2.3.1. Synchronization Algorithm

Unit template – based synchronization algorithm work towards determination of the sine and cosine synchronizing signals only for balanced grid conditions. However, under perturbations the grid voltage and frequency change, making loss of synchronization among inverter inevitable and thus compromising the current references and the control algorithm of the inverter. Conventional synchronization algorithms like Synchronous Reference Frame Phase Locked Loop (SRF – PLL) and Decoupled Double SRF (DSRF –

PLL) [61] based on inverse park transformation show fast synchronization response only under balance conditions. In presence of harmonics in the system, the operating bandwidth of the system is curtailed owing to harmonics elimination in the measurement loop thereby, leading to unacceptable performance of the synchronization algorithm. The interest of researchers towards synchronization algorithms are in majority targeted on achieving three goals i) to improve the dynamics of synchronization algorithm ii) provide better immunity towards grid disturbances and iii) reducing the steady state error during grid disturbance. To improve the dynamic performance of SRF – PLL, Amplitude Normalization Scheme (ANS) is integrated in the algorithm to improve the filtering capability besides, changes in integrator of low pass filter (PI controller) is proposed in [62-63]. These additions escalate the computation time of processor, leading to costly proposition. To improve the filtering capability of the PLL, Moving Average Filter (MAF) as proposed in [64-65] is integrated in the algorithm. The MAF ensures cancellation of specific frequencies, with a drawback of slow dynamic response and complex design considerations. SRF – PLL algorithms along with Enhanced Phase Locked Loop (EPLL) [66-67], based on adaptive frequency improves the synchronization capability using adaptive notch filtering. The algorithm suffers from increased complexity and computational burden resulting in unsatisfactory performance under disturbance/harmonic conditions.

Second Order Generalized Integrator (SOGI) acting as a Quadrature Signal Generator (QSG), additionally having the capability of providing infinite gain at a particular frequency with robust performance put the algorithm, in a class apart. The ability of SOGI adaptive filter to resonate at a particular frequency demonstrate its operation like notch filter by not only ensuring compensation of harmonics present in the system, but also increasing the robustness of tuning [68-69]. The SOGI QSG in comparison to previously reported QSG's like transport delay, Hilbert transformation and inverse park transformation is less frequency dependent, simple with prominent harmonic and noise filtering capabilities. However, these algorithms suffer from second harmonic distortion and high computational burden. In addition to the PLL algorithms, significant research has been done over nonlinear frequency locked loop concept (FLL) with negative feedback

wherein the phase locked loop is negotiated [70-71]. FLL operating in αβ domain requires prominent tuning of filters in addition to the complicated analysis and design procedures.

2.3.2. Resynchronization Algorithm

Significant literature has been reported for seamless transition from one mode to other, based on islanding detection algorithms and algorithms meant for control of power, voltage, and frequency. In [72] authors use both current and voltage modes of operation throughout, i.e., grid connected (grid following inverter) and islanded mode respectively (grid forming inverter). The proposed method negotiates the need of mode transfer but significantly increases computational requirement and the complexity of the control algorithm. A control algorithm is presented for transitioning from grid connected to islanded mode and vice versa through correct estimation of grid angle [73]. The involved control strategy limits the current transient at the cost of increased calculations. The algorithm is based on changes in scalar quantities during mode transition while neglecting the effect of phase angle [74]. A droop power based seamless transition algorithm is proposed in [75-76], wherein both the voltage and the frequency vary, resulting in oscillatory response and significant voltage distortion. A PLL based seamless transfer control is also proposed riding on the estimation of positive and negative sequence currents [77]. The method significantly reduces the computation in comparison to the previously proposed methods but experience slow transient dynamics. Under stringent grid norms adopted the grid codes across the world it is of importance that the system response should be as instantaneous as possible. Thereby, it is essential that synchronization algorithm has to have fast dynamics to restrict the overshoot and attain steady state quickly.

Popular synchronization techniques like unit template and Synchronous Reference Frame Phase Locked Loop (SRF-PLL) perform seamlessly under balanced conditions however, under unbalanced distorted voltage conditions or while transitioning from one operating mode to the other, these algorithms exhibit slow dynamics making the system unacceptable for establishing compliance with the stringent grid codes. Amplitude normalization scheme reported in enhances the dynamic response of the SRF-PLL at the cost of increased

computation and complexity. On the other hand, enhanced phased locked loop (EPLL) exhibits better transient response owing to its adaptive frequency notch filtering at the cost of large computational load. Phase locked loops and frequency locked loops with second order adaptive filter (SOGI) offer improved dynamic response taking advantage of adaptive filter based on band pass filter resonating at nominal frequency with optimum filtering of the input signal. Moreover, the ability of the SOGI adaptive filter to generate Quadrature signal generators (QSG) like Hilbert transformer, transport delay and inverse park transformation puts it aside with others. The improved dynamics of SOGI-PLL in addition to low computational requirement, makes it the fit algorithm for the synchronization/resynchronization requirement.

2.3.3. Two / Single Stage Grid Connected PV Inverters and their Parallel Operations

Grid-connected PV systems usually employs two stages: The first stage is a dc-dc boost converter for boosting the PV voltage, and achieving MPPT; and the second stage is a inverter stage for injection of the power by coupling with the grid employing synchronization. However, such systems have drawbacks on the count of higher part count, lower efficiency, lower reliability, higher cost, and larger size. In double stage topology, isolated or non-isolated dc-dc converters are used in conjunction with voltage source converter (VSC). For the low wattage, low – cost PV system non-isolated converters are preferred. To further reduce the operation cost the single stage grid connected PV systems are advocated [28].

Several PV inverter configurations have been presented in literatures to harvest the energy efficiently and cost effectively [29-34]. The technology based on centralized inverters that interfaced a large array of PV modules to the grid is very old and is operated for lower efficiency and limited duty periods. The technology involving multiple string inverters, where multiple strings of PV modules are connected in parallel instead of an array is more popular now-a-days [10-11]. The multi-string inverter system involves several strings are interfaced with their own dc–dc converter and parallel operating inverters or can have a

common centralized inverter. The ac module or module integrated inverter involves one or zero combination of one PV panels with a grid-connected inverter connected in dual-stage mode with an embedded HF transformer. Review of ac module inverters is given in [12]. In literature voltage source converter (VSC) based PV grid coupling is also considered with limited power conditioning to utilize the capacity of VSC at the maximum capacity to solve the Grid power quality issues like unbalance current, harmonics etc. [12-14].

With development of microgrid architecture based on clean and sustainable energy sources, role of power electronic converter especially voltage source inverter is very important. VSI can be employed for active filtering, compensation, and power conditioning. To enable large penetration of RES in the grid efficiently, the injection of these RES has to be uniformly distributed to enable consumption of power closest to the connected load. And this calls for paralleling of large number of such small DER to make up the demand in an environmentally friendly way. Such paralleling of VSI put large number of challenges in terms of their control and co-operative operation in the grid. A VSI interfaced with the renewable energy source typically has low inertia due to lack of moving parts unlike a synchronous generator. As a result, the system remains sensitive towards grid frequency variations. With multiple injection of VSI in the system, the inertia of the system would not increase making the system vulnerable unless and until a fast control on frequency change is not incorporated or virtual inertia is embedded. With paralleled VSI having different situations on the connected nodes, the response to the change of voltage or frequency often lead to issues of circulating currents and large variations during transients due to lack of inertia or damping system. For parallel combination of inverters aligned with the stringent grid codes, synchronization algorithm plays a crucial role. Noncompliance of the code would result in outage of the inverter. The stability of synchronization algorithm dictates the capability during parallel operation of the inverters especially during off grid mode of operation in master slave configuration.

2.4. Research Gap

Through the literature survey following research gaps are identified. Based on these the objectives of the thesis are identified as:

4. Incorporation of impedance through interfacing DC – DC converter to curb the spikes observed at the DC link.
5. Synchronization algorithm with fast dynamics
6. Resynchronization algorithm with fast transition capability from on grid mode to off grid mode and vice versa.

Chapter III

WIDE OPERATING RANGE DC – DC IMPEDANCE BASED CONVERTER FOR PHOTOVOLTAIC APPLICATION

3.1. Problem formulation

The power generated through PV panels is heavily dependent on the environmental conditions. For intermittent condition of irradiation change the output current of the panel is largely affected with small variation in the voltage at maximum point (V_{MPP}). With small variations in the input voltage, interfacing converters like conventional boost converter efficiently operate through the intermittency in irradiation with quick response to the changing conditions. However, for conditions like partial shading wide variations in input voltage are observed depending on the operating point corresponding to global maxima. Fig. 3.1.1, Shows the I – V characteristics corresponding to the shading on two portions corresponding to 2/3rd of the panel. Considering the cumulative power generated corresponding to the three operating points A', B' and C' is lesser than that corresponding to operating point C, the shaded portion gets bypassed, thereby pushes the MPPT controller to operate at V_{MPPC}. For such a low input voltage, a high operating duty is requisite for boost converter, which reduces the efficiency of conventional boost converter.

At the instance when the shading gets reduced to 1/3rd portion of the panel as shown in Fig. 3.1.2, the operating point swiftly moves from point C to point B'' and gradually settles at corresponding maximum power point B. During such transient a sudden rise in operating current can be observed which diminishes with gradual increase in output voltage. The voltage still being significantly low, therefore requires higher operating duty.

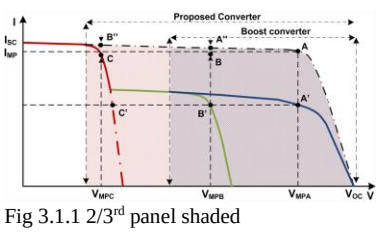


Fig 3.1.1 2/3rd panel shaded

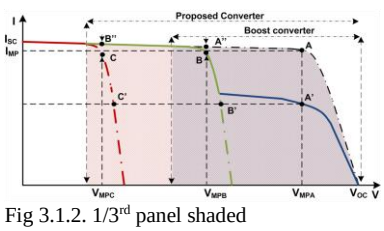


Fig 3.1.2. 1/3rd panel shaded

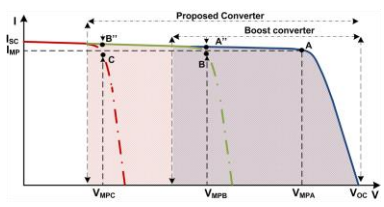


Fig 3.1.3. Normal Operation

3.2. Proposed Wide Operating Range Continuous Input Current Impedance Network Converter

The chapter proposes a new diode bypassed T – type network – based converter with continuous input current exhibiting wide operating range and offering modular structure for PV applications as shown in Fig. 3.2. The bypassing diode allows auxiliary boost using the storage of charge in shunt branch of T – network without affecting the characteristic of interfaced PV panel. The coupled inductor in T – network branch provides versatile boosting ability and adequate degree of freedom along with low ripple content. On the output side, the half-bridge topology with floating ground reduces the voltage stress on the switches to half, thereby, reducing the losses and heat sink size besides reduction on common mode currents. The operating duty of the switches are governed and alternating shared equally in accordance with the incremental conductance (InC) algorithm, extracting maximum power from the panel. The PV system utilizing the proposed converter is simulated under MATLAB Simulink environment and is experimentally tested using DSP microcontroller operating on a developed prototype for different conditions of incident on the PV panel.

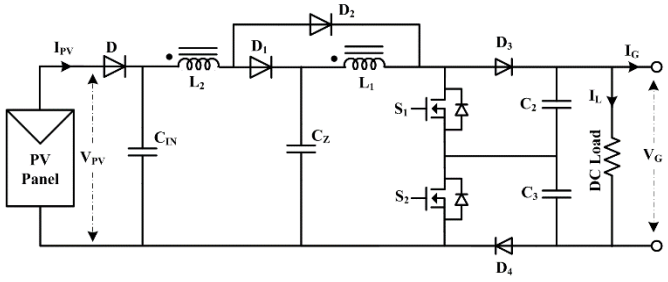


Fig 3.2 Continuous Input Current Impedance Converter

3.3. Operating Modes

The circuit configuration and operation of proposed continuous input current T converter (CIC – TC) is proposed in Fig.3.3 and Fig.3.4, where the operating modes are elaborated on the basis of operating duty, i) Operating Duty < 0.5 ii) Operating Duty > 0.5

3.3.1. Operating Duty < 0.5

The operating mode is analysed based on three possible gating sequence; only S_1 ON; only S_2 ON and both S_1 and S_2 are OFF shown in Fig.3.3. When only one switch S_1 or S_2 is ON, diode D_1 is reverse biased (previously charged capacitor C_Z with voltage greater than V_{IN}), while input current flows through inductor L_2 and diode D_2 ($V_{IN} > V_O/2$). Shunt capacitor discharges through inductor L_1 while the load/grid current is supported by discharging capacitor C_1 for S_1 ON and C_2 for S_2 ON. For the time corresponding to both S_1 and S_2 OFF with the duty d_O, shunt capacitor C_Z charges through the difference of current flowing through L_2 and L_1. Diode D_2 is reverse biased as the output voltage V_O is presented to it. Charging of capacitor C_Z to a voltage greater than V_{IN} depends on the duty d_O, which provides an additional auxiliary gain which in turn alleviates the switching stress further. Current across coupled inductor along with voltages across impedance capacitor and output capacitor is shown in Fig 3.5.

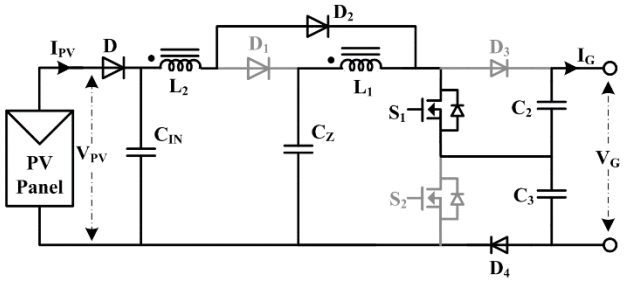


Fig. 3.3.1 Only S_1 ON (Duty < 0.5)

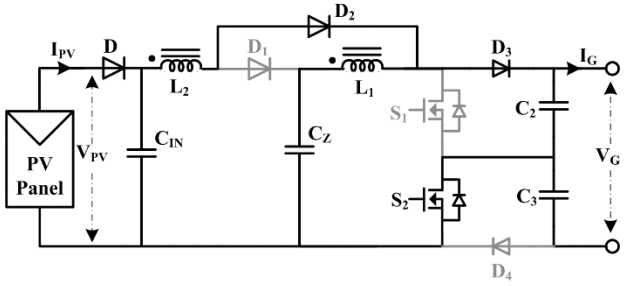


Fig. 3.3.2 Only S_2 ON (Duty < 0.5)

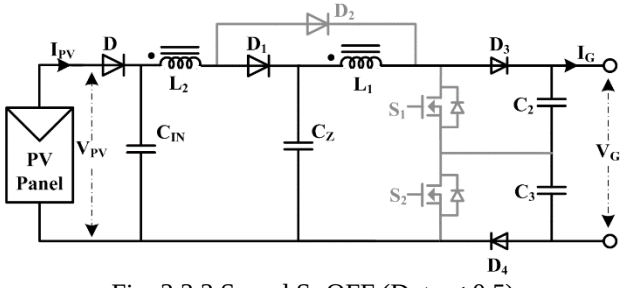


Fig. 3.3.3 S_1 and S_2 OFF (Duty < 0.5)

3.3.2. Operating Duty > 0.5

With operating duty of greater than 50%, the input impedance network gets enabled for the operation of the converter. Shoot through operation is essential for wide operating band and can be analysed under three switching states; only S_1 ON alone; only S_2 ON and both S_1 and S_2 ON as shown in Fig. 3.4. For only S_1 alone ON or S_2 alone ON, shunt capacitor C_Z now charges through the difference of the current flowing through inductor L_2 and L_1 since D_1 remains ON and D_2 becomes reverse biased as $V_{IN} < V_O/2$. The load is supported by output capacitor C_1 for S_1 ON and C_2 for S_2 ON. When both S_1 and S_2 both are ON for a duty cycle of *ds*, diode D_1 becomes reverse biased as voltage across capacitor C_Z is greater than V_{IN}, while diode D_2 gets forward biased, providing continuous input current during shoot through operation while the load is supported alternatively and cumulatively by capacitors C_1 and C_2.

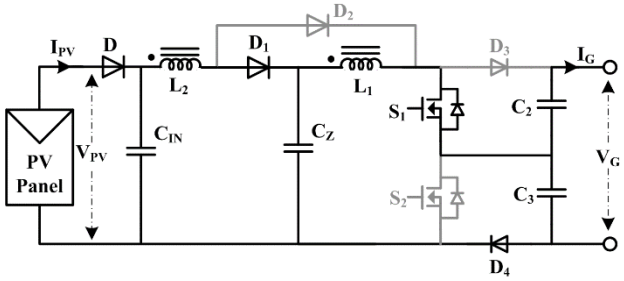


Fig. 3.4.1 Only S_1 ON (Duty > 0.5)

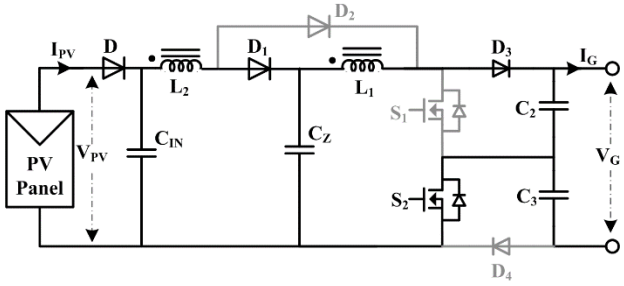


Fig. 3.4.2 Only S_2 ON (Duty > 0.5)

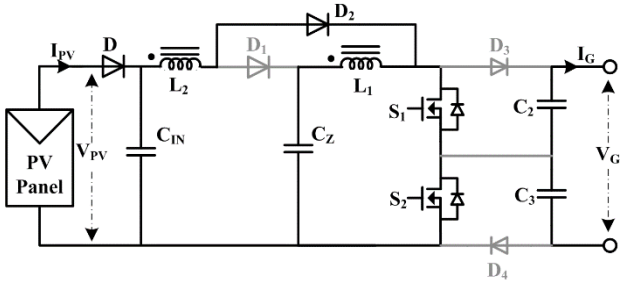


Fig. 3.4.3 S_1 and S_2 ON (Duty > 0.5)

The current and voltages across coupled inductor, impedance capacitor and output capacitors respectively during shoot through operation is shown in Fig. 3.6

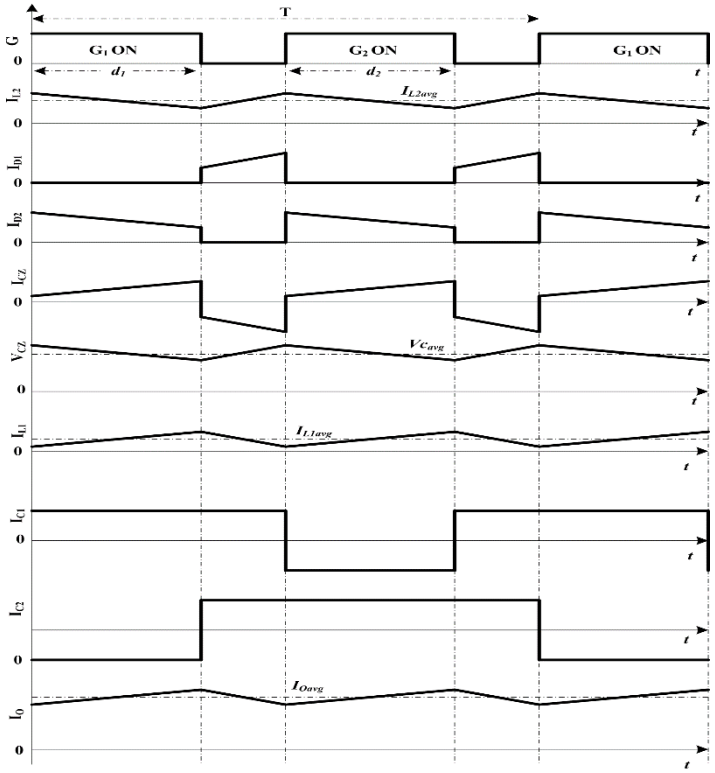


Fig. 3.5 Inductor currents and voltages during normal operating condition

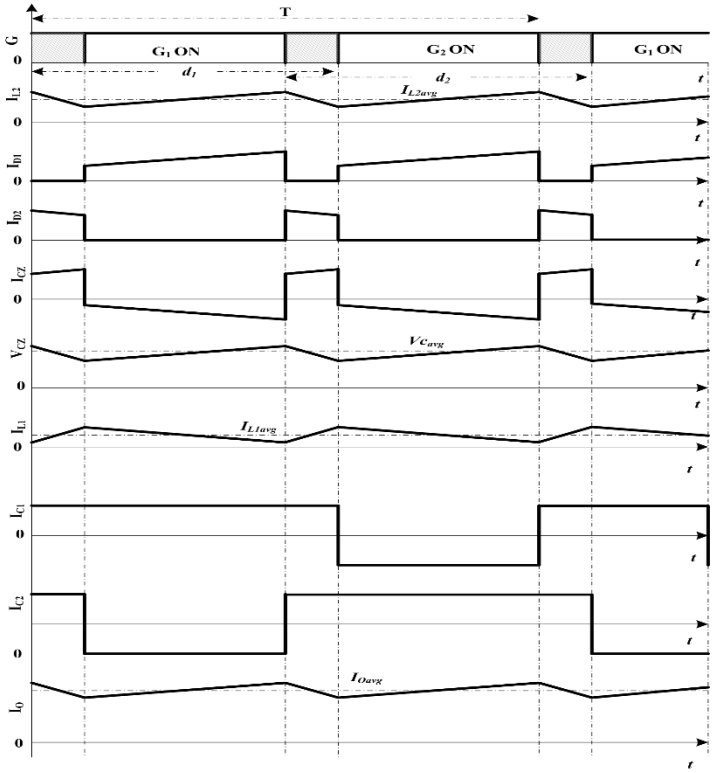


Fig. 3.6 Inductor currents and voltages during shoot through condition

3.4. Converter Analysis – Voltage Mode and Current Mode

3.4.1. Converter Analysis for Voltage Mode

The steady state converter analysis for voltage mode under normal operating conditions and shoot through conditions are presented using voltage second balance equations. '*n*' represents turns ratio of the coupled inductor and d_1, d_2 represents the duty of switches S_1 and S_2 the duty cycle d_0 and *ds* are defined as either the deficit of the sum d_1+d_2 from one and excess to one respectively, where, do correspond to duty where both switches S_1 and S_2 are off and d_S is the overlapping duty of d_1 and d_2 during shoot through mode.

For normal operating conditions as shown in Fig 3.3, the voltage across the coupled inductor during the time when only S_1 is on, are given by (1); Since

$V_{L2} = n\,V_{L1};\ V_{L2} = V_{in} - V_{C3}$, therefore

$$V_{L1} = \frac{V_{in}-V_{C2}}{n} \tag{1}$$

For the switching duration when only S_2 is on, the inductor voltages are given by (2);

$$V_{L2} = V_{in} - V_{C2}, \text{ therefore } V_{L1} = \frac{V_{in}-V_{C1}}{n} \tag{2}$$

For both S_1 and S_2 are off the inductor voltages are given by (3); where n is the turns ratio of coupled inductors. $V_{L2} = \left(\frac{V_{in}-V_o}{n+1}\right)n$ therefore

$$V_{L1} = \frac{V_{in}-V_o}{n+1} \tag{3}$$

The voltage second balance equation for inductor L_2 can be as given by (4)

$$(V_{in} - V_{C3})d_1T + (V_{in} - V_{C2})d_2T + \frac{(V_{in}-V_o)n}{n+1}d_oT = 0 \tag{4}$$

Taking $d_1 = d_2 = d$, and solving (4) and substituting $V_{C1} + V_{C2} = V_o$ we get

$$(2V_{in} - V_o)d = \frac{(V_{in}-V_o)n}{n+1}d_o \tag{5}$$

Substituting $d_0 = 2(0.5 - d)$ it gives the expression for gain as (6)

$$\frac{V_o}{V_{in}} = \frac{(n+2d)}{n(1-d)+d} \quad (6)$$

During shoot through mode as shown in Fig. 3.4, the corresponding inductor voltages for the only S_1 on with operating duty d_1 is given by (7).

$$V_{L2} = \left(\frac{V_{in}-V_{C2}}{n+1}\right)n \; ; V_{L1} = \frac{V_{in}-V_{C2}}{n+1} \quad (7)$$

For the switching duration where only S_2 is on, it corresponds to the duty of d_2; the inductor voltages are given by (8);

$$V_{L2} = \left(\frac{V_{in}-V_{C1}}{n+1}\right)n \; ; V_{L1} = \frac{V_{in}-V_{C1}}{n+1} \quad (8)$$

Similarly, when both S_1 & S_2 are on, it corresponds to duty of d_S; the inductor voltages are given by (9);

$$V_{L2} = V_{in} \; ; V_{L1} = \frac{V_{in}}{n} \quad (9)$$

Voltage second balance equation for inductor L_2 is given by (10)

$$\frac{(V_{in}-V_{C2})}{n+1} n d_1 T + \frac{(V_{in}-V_{C1})}{n+1} n d_2 T + V_{in} d_s T = 0 \quad (10)$$

Substituting $d_S = 2(d - 0.5)$, it gives the expression for gain as

$$\frac{V_o}{V_{in}} = \frac{2d(2n+1)-(1+n)}{nd} \quad (11)$$

3.4.2. Converter Analysis for Current Mode

The steady state converter analysis for current mode under normal operating conditions and shoot through conditions are presented using current second balance equations across capacitor. During normal operating conditions as shown in Fig 3.3, the currents across the capacitors when S_1 alone is ON are given by (12);

$$I_{CZ} = I_{L1} \; ; I_{C2} = I_O \; ; I_{L2} = I_{PV} \; ; I_{C3} = -I_{L1} - I_{L2} + I_o \quad (12)$$

Similarly, when S_2 alone is ON, with corresponding duty d_2 the currents are given by (13);

$$I_{CZ} = I_{L1} \; ; I_{C2} = -I_{L1} - I_{L2} + I_o \; ; I_{L2} = I_{PV} ; I_{C3} = I_o \quad (13)$$

when both S_1 and S_2 are off with duty d_0, the currents are given by (14);

$$I_{CZ} = -I_{L2} + I_{L1}\ ; I_{C2} = -I_{L1} + I_O; I_{C3} = I_{L1} - I_o \quad (14)$$

Current second balance equation for capacitor C_Z is given by (15)

$$I_{L1}d_1T + I_{L1}d_2T + (-I_{L2} + I_{L1})d_oT = 0 \quad (15)$$

Taking $d_1 = d_2 = d$, and $d_0 = 2(0.5 - d)$, (15) can be solved to;

$$I_{L1} = (I_{L2})(1 - 2d) \quad (16)$$

$$\frac{I_{L2}}{I_{L1}} = \frac{1}{(1-2d)} \quad (17)$$

The current second balance for capacitor C_2;

$$I_o d_1 T + (-I_{L2} - I_{L1} + I_o)d_2T + (-I_{L1} + I_o)d_oT = 0 \quad (18)$$

Taking $d1 = d2 = d$ and $d_0 = (2d - 1)$ and solving;

$$(I_o) = (I_{L2}d) + (1 - d)I_{L1} \quad (19)$$

$$(I_o) = (I_{L2}d) + (1 - d)(1 - 2d)I_{L2} \quad (20)$$

The transfer function for output current with respect to input current is given as (21)

$$\frac{I_o}{I_{L2}} = \frac{I_o}{I_{PV}} = d + (1 - d)(1 - 2d) \quad (21)$$

For shoot through operating conditions as shown in Fig. 3.4, currents across the capacitors for the switching state when alone S_1 is conducting with duty d_1 is given by (22);

$$I_{CZ} = I_{L1} - I_{L2}\ ; I_{C2} = I_O; I_{C3} = -I_{L1} + I_o; I_{L2} = I_{PV} \quad (22)$$

Similarly, when alone S_2 is on with duty of d_2 the currents are given by (23);

$$I_{CZ} = I_{L1} - I_{L2}\ ; I_{C2} = -I_{L1} + I_O; I_{C3} = I_o; I_{L2} = I_{PV} \quad (23)$$

When both S_1 and S_2 are ON with duty d_S the currents are given by (24);

$$I_{CZ} = I_{L1}\ ; I_{C2} = I_O; I_{C3} = I_o \quad (24)$$

Current second balance equation for capacitor C_Z is given by

$$(-I_{L2} + I_{L1})d_1T + (-I_{L2} + I_{L1})d_2T + I_{L1}d_ST = 0 \quad (25)$$

Taking $d_1 = d_2 = d$, and $d_S = 2(d - 0.5)$ and solving;

$$(-2I_{L2} + 2I_{L1})d + (I_{L1})(2d - 1) = 0 \quad (26)$$

$$\frac{I_{L2}}{I_{L1}} = \frac{(4d-1)}{(2d)} \quad (27)$$

Similarly current second balance for capacitor C_2;

$$I_o d_1 T + (-I_{L1} + I_o)d_2 T + (I_o)d_S T = 0 \quad (28)$$

$$(I_{L1})d = (I_o)(4d - 1) \quad (29)$$

The relation between input current and output current during shoot through operation can be given by (30)

$$\frac{I_o}{I_{L2}} = \frac{I_o}{I_{PV}} = \frac{2d^2}{(4d-1)(4d-1)} \quad (30)$$

3.4.3. Efficiency Analysis

The efficiency is analyzed accounting the internal resistances of both inductors L_1 and L_2 as r_l, internal turn ON resistance of both the switches S_1 and S_2 as r_s and voltage drop V_d across the diodes. During normal operation, the voltage across inductor L_2 for the gating sequence S_1 alone ON, S_2 alone ON and S_1 and S_2 OFF are given by (31-33) respectively.

$$V_{L2} = V_{in} - I_{L2}(r_l + r_s) - 2V_d - \frac{V_o}{2} \quad (31)$$

$$V_{L2} = V_{in} - I_{L2}(r_l + r_s) - 2V_d - \frac{V_o}{2} \quad (32)$$

$$V_{L2} = (V_{in} - 2I_{L2}(r_l) - 3V_d - V_o)k \quad (33)$$

Where $k = \frac{n}{n+1}$; Using voltage second balance across inductor L_2, the input voltage V_{IN} is given by (34), the input current (I_{PV}) of the converter from (21), can be given by (35)

$$V_{in} = \frac{\left[V_o\left[(d(1-2k)+k)+\frac{(r_l(2d(1-2k))+2k)+2dr_S}{R(d+(1-d)(1-2d))}\right]+V_d(3k(1-2d)+4d)\right]}{(2d(1-k)+k)} \quad (34)$$

$$I_{PV} = I_{L2} = \frac{I_o}{d+(1-d)(1-2d)} = \frac{V_o}{R(d+(1-d)(1-2d))} \quad (35)$$

The input power (P_{in}) is given as $P_{in} = V_{in} * I_{PV}$, and the output power (P_O) is given as $P_o = V_o * I_o = \frac{V_o^2}{R}$. Therefore, the efficiency (η) of converter can be given by (36).

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o^2}{\left[\frac{V_o}{(d+(1-d)(1-2d))}\right]\frac{\left[V_o\left[(d(1-2k)+k)+\frac{(r_l(2d(1-2k))+2k)+2dr_s}{R(d+(1-d)(1-2d))}\right]+V_d(3k(1-2d)+4d)\right]}{(2d(1-k)+k)}} \quad (35)$$

Similarly, for shoot through mode, the voltage across inductor L_2, incorporating the drops across inductor, switches and diodes for the gating sequence S_1 alone ON, S_2 alone ON and S_1 & S_2 both ON are given by (37-39).

$$V_{L2} = \left(V_{in} - 2I_{L2}(r_l) - I_{L2}(r_s) - 2V_d - \frac{V_o}{2}\right)k \quad (37)$$

$$V_{L2} = \left(V_{in} - 2I_{L2}(r_l) - I_{L2}(r_s) - 2V_d - \frac{V_o}{2}\right)k \quad (38)$$

$$V_{L2} = V_{in} - I_{L2}(r_l) - 2I_{L2}(r_s) - V_d \quad (39)$$

From voltage second balance of inductor L_2, the input voltage (V_{IN}) is given in (40). And from (30), the input current (I_{PV}) during shoot through given by (41)

$$V_{in} = \frac{\left[V_o\left[kd+\frac{(4d-1)^2}{2Rd^2}\left(r_l(2d(2k+1)-1)+r_s(2d(k+2)-2)\right)\right]+V_d(2d(2k+1)-1)\right]}{(2d(k+1)-1)} \quad (40)$$

$$I_{PV} = I_{L2} = I_o\frac{(4d-1)^2}{2d^2} = \frac{V_o(4d-1)^2}{2Rd^2} \quad (41)$$

With the input power $P_{in} = V_{in} * I_{PV}$ and output power $P_o = V_o * I_o = \frac{V_o^2}{R}$, the efficiency of the converter during shoot through mode is given by (42).

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o^2}{\left[\frac{(4d-1)^2}{2Rd^2}\right]\frac{\left[V_o\left[kd+\frac{(4d-1)^2}{2Rd^2}\left(r_l(2d(2k+1)-1)+r_s(2d(k+2)-2)\right)\right]+V_d(2d(2k+1)-1)\right]}{(2d(k+1)-1)}} \quad (42)$$

3.5. MATLAB Based Simulation of Impedance Converter

The proposed impedance converter interfaced with photovoltaic energy source and a DC bus of 48V is designed and simulated in MATLAB Simulink environment. The photovoltaic panels are modeled to the configuration of TSE210PV photovoltaic panel

from NEOSOL rated at 206W with maximum voltage (V_{MP}) and maximum current (I_{MP}) of 27.2V and 7.6A respectively. For a panel of 54 cells, a bypass diode is considered across 18 solar cells. The modeled configuration of the converter is specified in TABLE I.

TABLE I
SIMULATION PARAMETERS

Name	Quantity/Value
Power	206 W
DC Grid Voltage	48 V
Open Circuit Voltage of PV Panel (V_{OC})	33.62 V
Short Circuit Current of PV Panel (I_{SC})	8.35 A
Inductor (L_1), Turns Ratio	100 µH, 2
Impedance Capacitor (C_Z)	200 µF
Output Capacitor (C_2 & C_3)	47 µF
Switching Frequency (f_s)	50 kHz

The dynamic performance of the converter is verified for the disturbance conditions as shown in Fig. 3.7.

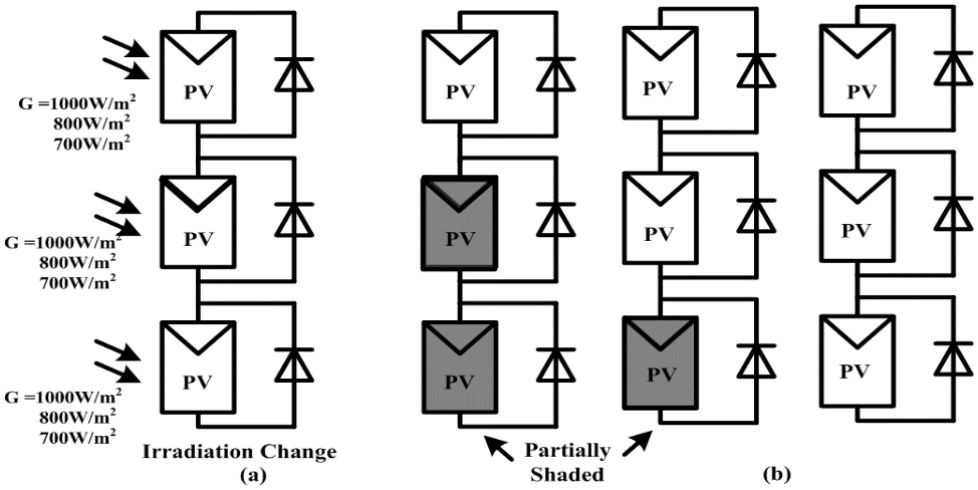


Fig. 3.7 Intermittencies in Photovoltaic Panel a) Irradiance Change b) Partial Shading

3.5.1. Performance During Irradiance Change

Response of the converter for intermittency of uniform irradiation change across the panel is as shown in Fig. 3.8.1 and Fig. 3.8.2. Fig. 3.8.1 represents irradiation (G), maximum extracted power, voltage across input terminals (V_{IN}) and impedance capacitor (V_Z) along with input current (I_{IN}) to the converter. The grid voltage (V_{GRID}) along with load current, grid current and output of the converter (I_{OUT}) is shown in Fig 3.8.2. Initially, irradiation across the panel is at its nominal value of 1000 W/m^2. The MPPT algorithm of InC extracts maximum power of 206W feeding the impedance converter at 27.2V, 7.6A. With operating

duty close to 50%, impedance capacitor is charged to a voltage of 28V. The converter feeds 4A, 3.25A to the connected local load and 0.75A is supplied to the grid. The irradiation across the solar panel reduces to 800W/m^2 uniformly across the panel at t = 0.15s. The maximum power extracted from the panel reduces to 165W, with input current reducing to 6.2A at 26.6V. To push the generated power through to the DC grid, the operating duty of the converter increases. As a result, the voltage across impedance capacitor is boosted to

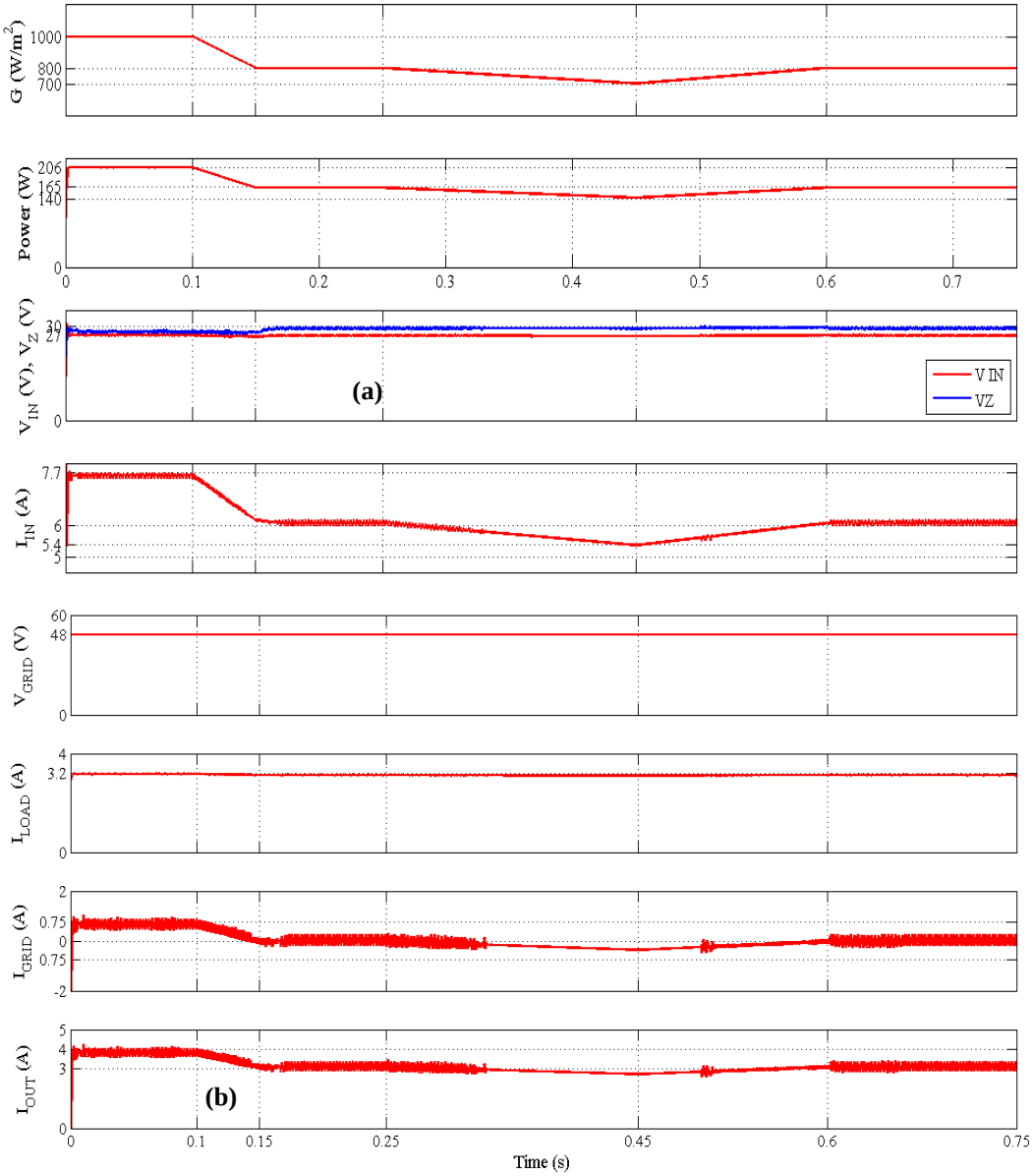


Fig 3.8.1 a) i) Maximum Power ii) Input Voltage (V_{IN}), iii) Capacitor Voltage (V_Z) iv) Input Current (I_{IN})
Fig. 3.8.2 b) i) Grid Voltage ii) Load Current iii) Grid Current iv) Output Current under irradiation change

30V with converter output current reducing to 3.3A, wherein 0.1A is fed to the grid. At t = 0.25s, the irradiation across the panel is further reduced to 700W/m^2 at t = 0.45s. With the input current further reducing to 5.4A and input voltage of 25.9V, the extracted power from the panel drops to 140W. With small change in the operating duty, impedance capacitor voltage is at 30V.The converter feeds 2.7A with the grid supporting load demand by feeding 0.75A. At t= 0.45s, irradiation across the panel is gradually restored to 800W/m^2 with the converter response same as previously discussed.

3.5.2. Performance during Partial Shading

Dynamics of the proposed converter for intermittency of partial shading is shown in Fig. 3.9.1 and Fig. 3.9.2. The condition of partial shading is taken in accordance to the test condition shown in Fig. 3.7. Initially 68W is extracted from the panel at 9V,7.6A, representing 2/3rd of the panel being shaded. As the converter operates in shoot through

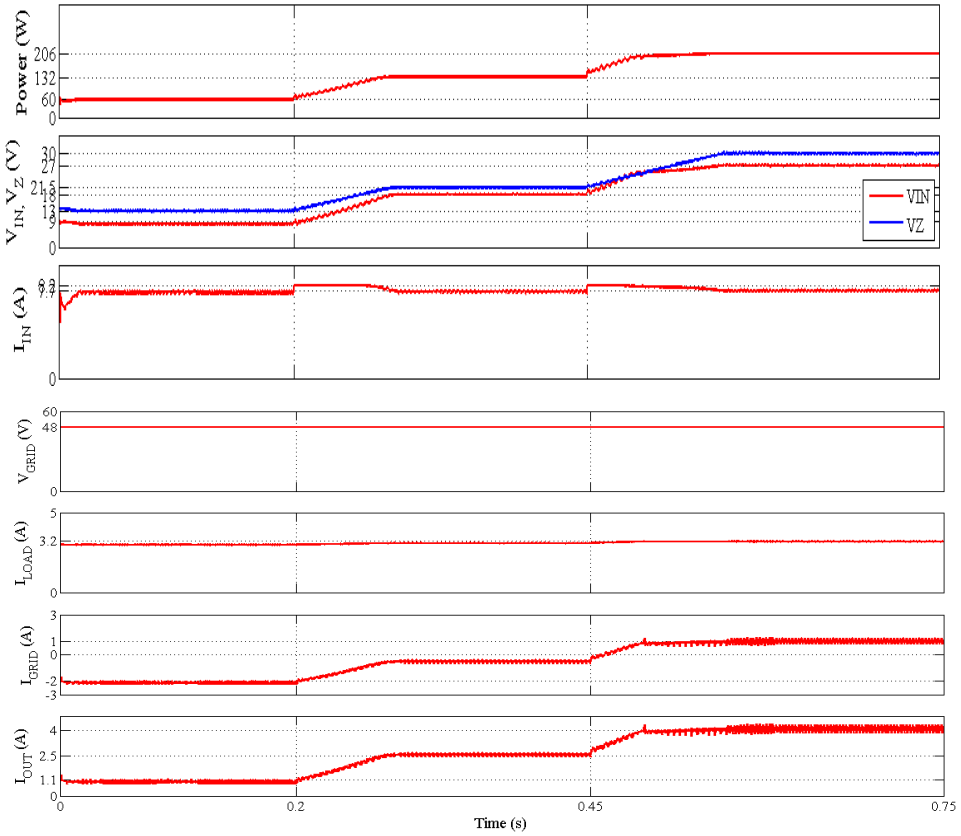


Fig 3.9.1 a) i) Maximum Power ii) Input Voltage (V_{IN}), iii) Capacitor Voltage (V_Z) iv) Input Current (I_{IN})

Fig. 3.9.2 b) i) Grid Voltage ii) Load Current iii) Grid Current iv) Output Current under partial shading

mode, an auxiliary boost is provided through the impedance capacitor with its voltage boosted at 13V. The load demand of 3.2A is supported by 1.1A from the converter and 2.1A from grid. At t = 0.2s, the shading is reduced to 1/3rd of the panel. The extracted power from the panel rises to 137, with the input voltage increasing to 18V and input current maintained at 7.6A. The voltage across the impedance capacitor is at 21.5V, with the operating duty reducing, the auxiliary boost provided by the impedance network reduces. The converter feeds 2.5A to the load, with the remainder demand of 0.7A fed by the grid. At t = 0.45s, the panel operation is restored to its nominal value i.e. maximum power of 206W. The response of the converter is same as discussed earlier.

3.6. Experimental Analysis of Impedance Converter

The prototype of the proposed converter as shown in Fig 3.10, is designed and experimentally verified for the intermittent conditions of irradiance change and partial shading as discussed above. The characteristic of PV panel is emulated through PV simulator AMETEK TDS 600/8. The InC algorithm is implemented of dsPIC33FJ16GS502. The hardware parameters are as shown in TABLE II.

TABLE II
HARDWARE PARAMETERS

Name	Quantity/Value
Power	78W
DC Grid Voltage	48V
Max Power Voltage of PV Panel (V_{MP})	27V
Max Power Current of PV Panel (I_{MP})	2.9 A
Inductor (L_1) , Turns Ratio, Core	100µH, 2, EE/25(EPCOS)
Impedance Capacitor (C_Z)	220µF
Output Capacitor (C_2 & C_3)	47µF
Switching Frequency (f_s)	50kHz
MOSFET	TI NexFET CSD19535KCS
Gate Driver	ADUM4223
Sampling Frequency of dsPIC (MPPT)	1kHz

3.6.1. Experimental Performance during Irradiance Change and Partial Shading

Fig. 3.11.1 shows the voltage extracted from the panel (V_{IN}), Grid voltage (V_{GRID}) and the voltage across the impedance capacitor (V_Z), while Fig. 3.11.2 depicts the converter output

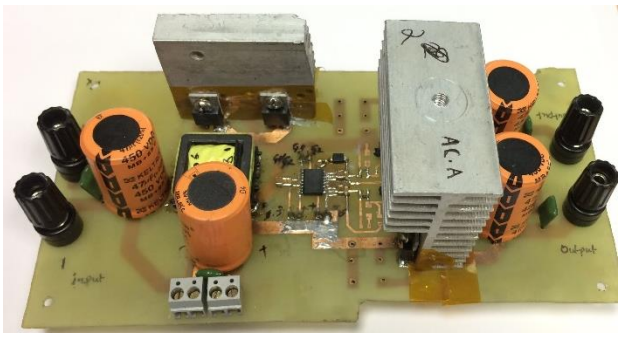


Fig 3.10 Hardware Prototype of Proposed Impedance Converter

current (I_{OUT}), load current (I_{LOAD}), Grid current (I_{GRID}) and converter input current. Initially under nominal irradiation condition of 1000W/m^2 and the grid voltage maintained at 50.8V (i.e., charged battery / strong grid), the input voltage of the converter is 27V. The impedance converter voltage is at 26.3V. For an input current of 2.9A, the converter feeds 1.1A i.e., 610mA to the connected load and 500mA to the grid. At t = 4.5s, irradiation across the panel is dwelled to 800W/m2. The input current drops to 2.5A with low variation

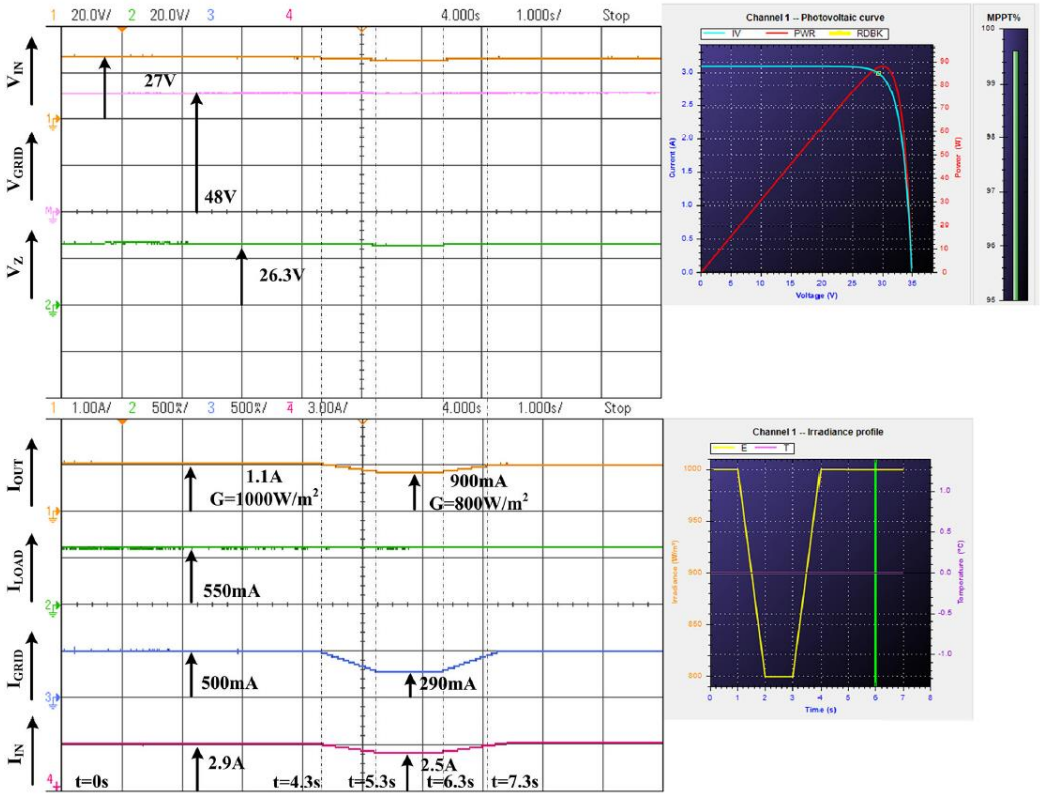


Fig 3.11 a) i) Input Voltage (V_{IN}) ii) Grid Voltage (V_G) iii) Capacitor Voltage (V_Z) b) i) Output Current (I_{OUT}) ii) Load Current iii) Grid Current iv) Input Current (I_{IN}) for irradiation change (strong grid)

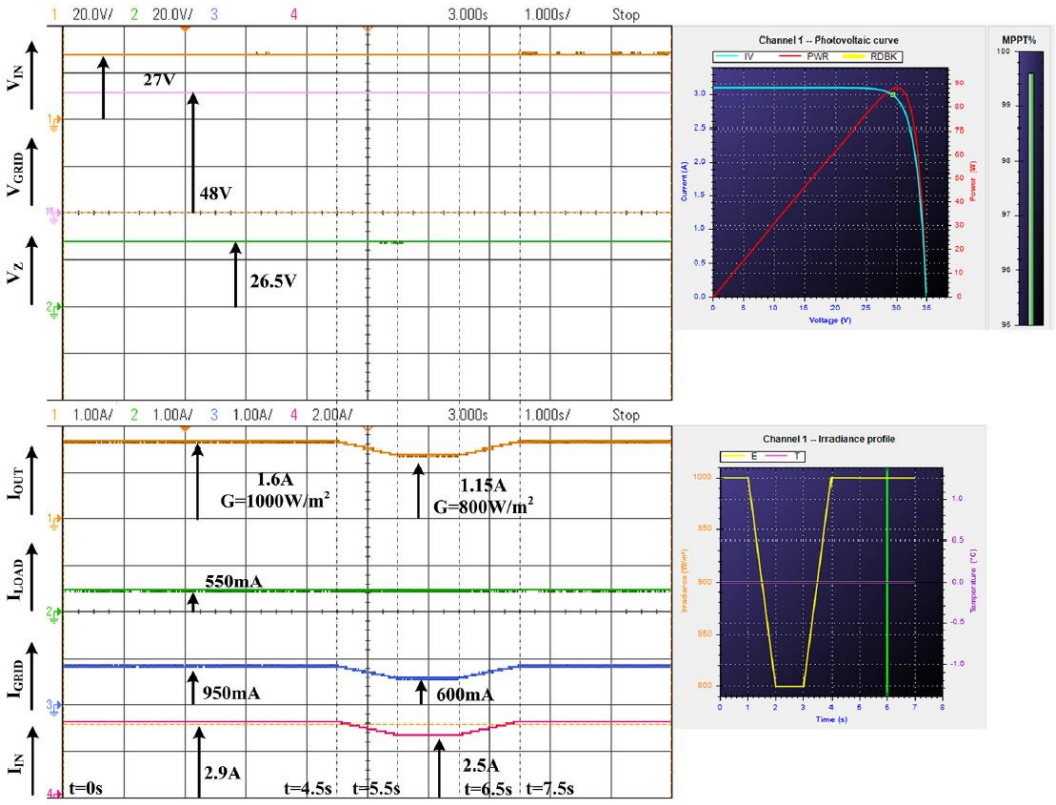


Fig 3.12 a) i) Input Voltage (V_{IN}) ii) Grid Voltage (V_G) iii) Capacitor Voltage (V_Z) b) i) Output Current (I_{OUT}) ii) Load Current iii) Grid Current iv) Input Current (I_{IN}) for irradiation change (Weak grid)

in input voltage and the voltage across the impedance capacitor. The output current of the converter reduces to 900mA with the grid feeding 290mA. At t =6.3s, the irradiation is restored to its nominal value of 1000W/m^2 as converter response is same as discussed above. The response of the converter for grid voltage of 48V (i.e., discharged battery/weak grid) is shown in Fig. 3.12.1 and Fig. 3.12.2. For the same operating conditions as discussed above for strong grid, the converter feeds 1.6A to the load and grid at 1000W/m^2, while for 800W/m^2, the converter output reduces to 1.15A.

Fig. 3.13 and Fig. 3.14 show the response of converter under partial shading conditions. Fig. 3.13 shows the dynamic response of converter with 1/3rd of the panel shaded. Initially, the panel response is same as initial condition as discussed for strong grid under irradiation of 1000W/m^2. At t = 2.7s, 1/3rd of the panel is shaded with input voltage dropping to 17.25V. With the converter operating in shoot through mode, impedance capacitor voltage is boosted to 20.3V. At the instance of partial shading the input current momentarily rises towards ISC and gradually settles at I_{MP} value of 2.9A. The converter output current

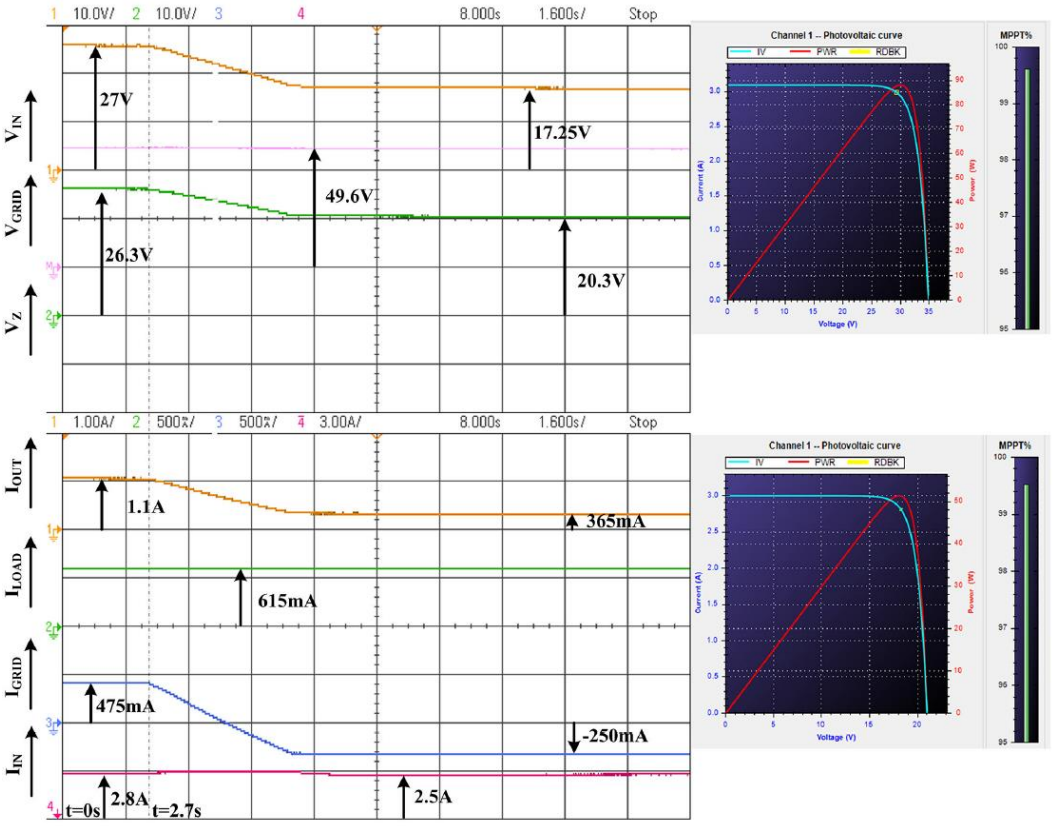


Fig 3.13. a) i) Input Voltage (V_{IN}) ii) Grid Voltage (V_G) iii) Capacitor Voltage (V_Z) b) i) Output Current (I_{OUT}) ii) Load Current iii) Grid Current iv) Input Current (I_{IN}) for partial shading (27V to 18V)

reduces from 1.1A to 365mA, with the grid feeding 250mA to cater the load demand of 615mA. The panel is further shaded such that only 1/3rd panel is operational as shown in Fig. 3.14. At t= 3s, the shading of panel increases for 1/3rd of panel to 2/3rd of panel. Input voltage drops to 8V, and impedance capacitor voltage is boosted to 9.6V. The converter output current drops to 280mA and the grid supports the load demand, feeding 606mA.

3.7. Performance Analysis

A comparison is drawn for the operating duty with the varying input voltage in respect of the proposed converter, comparing conventional boost converter, continuous input Quasi Z source and Quasi Y source converters as shown in Fig.3.15. A comparison is drawn between the converters based on the operating duty of the converters for the varying input voltage as shown in TABLE III. For an intermittent condition of irradiation change, the

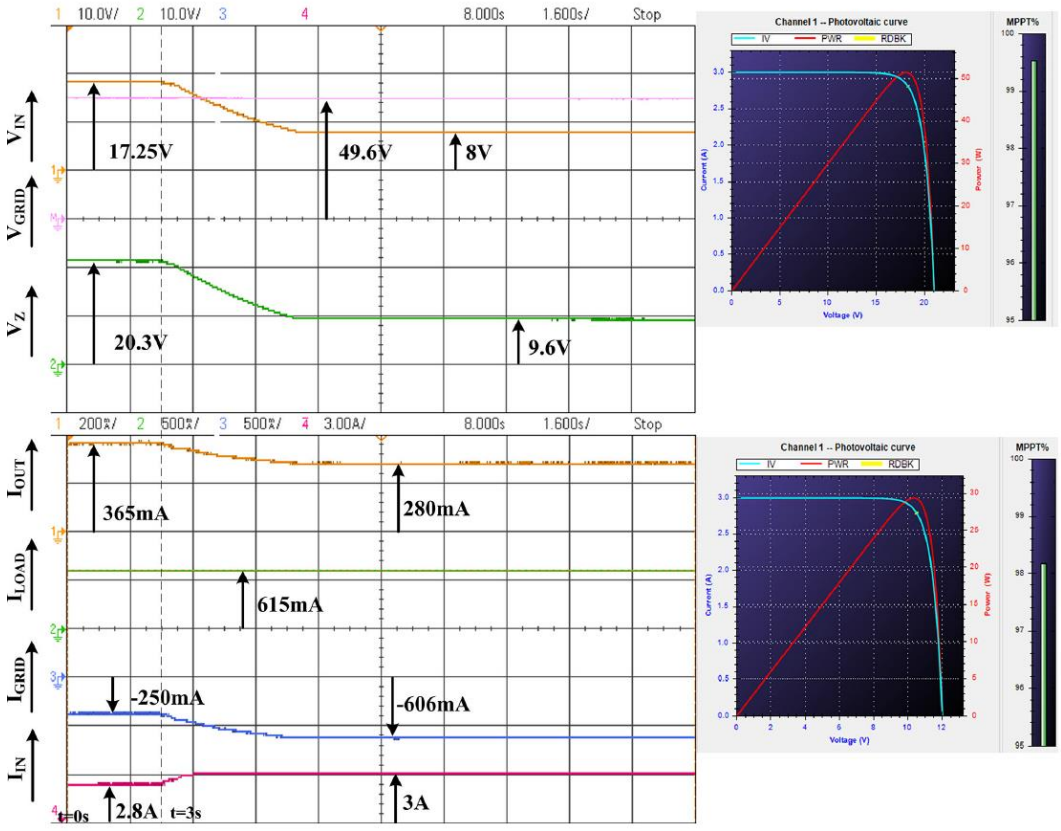


Fig 3.14. a) i) Input Voltage (V_{IN}) ii) Grid Voltage (V_G) iii) Capacitor Voltage (V_Z) b) i) Output Current (I_{OUT}) ii) Load Current iii) Grid Current iv) Input Current (I_{IN}) for partial shading (18V to 9V)

operating duty for the rated conditions, the converter is operated around 0.45 duty and lesser. In this range of duty, the proposed converter provides rated output power at the lowest duty in comparison to conventional boost and other impedance converters, offering higher efficiency. Under partial shading conditions where the input voltage drops considerably, the operating duty increases in order to push the maximum power to the LVDC µG. For the operating duty range of 0.45 to 0.55, the boost converter operates with

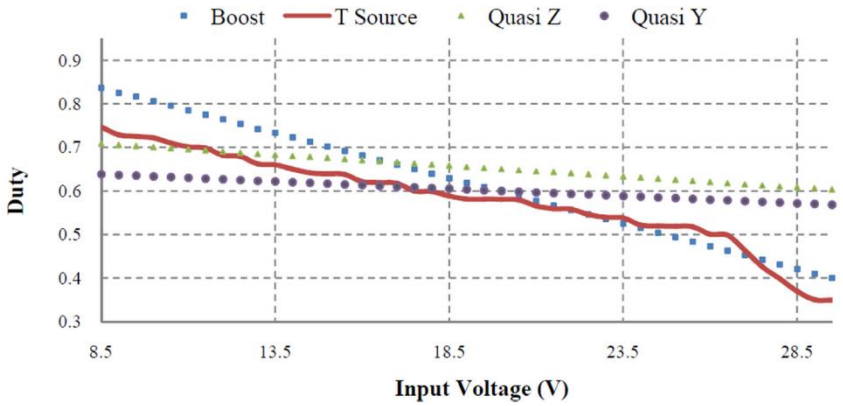


Fig 3.15. Performance Comparison of Impedance Converter

only slightly lower duty compared to the proposed converter. While, Quasi Z (with additional capacitor) and Quasi Y (with additional inductor) converters operate at higher duties. For duty range of 0.55 to 0.625, where the lower voltage conditions are observed under partial shading, the proposed converter operates at minimum duty. Even at higher duties where the voltage gain requirement is 3 or beyond i.e., operating duty of around 0.7 the proposed converter performs only second to the Quasi Y converter, and that too marginally, indicating higher efficiency throughout the operation.

TABLE III PERFORMANCE ANALYSIS

Duty / Converter	Less than 0.45	0.45 to 0.55	0.55 to 0.625	0.625 to 0.7	0.7 and above
Boost Converter	II	I (Best)	II	IV	IV
Proposed T Source	I (Best)	II	I (Best)	II	III
Quasi Z Source	IV	IV	IV	III	II
Quasi Y Source	III	III	II	I (Best)	I (Best)
	Region of Irradiance change		Region of partial shading		

3.8. Conclusion

The observed results affirm the capability of the proposed impedance source converter for photovoltaic applications. The results demonstrate the converters capability to operate under intermittent PV conditions, feeding the generated power to the grid at reduced duty and voltage stress in both normal and shoot through operating condition as compared to conventional converters ensures efficient wide operating band. Moreover, the modular and power dense architecture allows the converter to be interfaced directly with the photovoltaic panel.

Chapter IV

BI – DIRECTIONAL WIDE OPERATING MULTIPORT IMPEDANCE CONVERTER

4.1. Problem formulation

Energy storage system is interfaced at the output of the DC -DC MPPT charge controller and input of the grid interfacing inverter. For meeting the voltage required stacking of the batteries is done in series parallel combination. Under practical case where batteries with different SoC's are stacked together, the battery with lower SoC tends to load the healthy batteries, thus requires additional equalizer/ balancer circuits which increases the cost and complexity of converter. Multiport topologies, allow battery stacking based upon the number of inputs on a single converter with simpler solution. Multiport topologies for electric vehicle and photovoltaic applications are presented where the multiport converters fail in optimizing the power utilization from individual input source with limited operating band. Also, under different SoC conditions or input conditions, above discussed converters, both non-isolated and isolated are incapable to charge the batteries stacks at different rates. Different SoC and SoH conditions of individual battery in the battery stack significantly hinders the efficiency of the system, thus demanding battery equalizer circuit.

4.2. Proposed Bi – Directional Multiport Impedance Network

This chapter proposes a bi-directional impedance converter for power transaction as shown in Fig. 4.1. The presented converter provides auxiliary boost capabilities by operating under shoot through operations, ensuring efficient operations during intermittent conditions. Moreover, multi-input architecture allows stacking of batteries, to operate even with batteries of different characteristics, by adequately regulating the battery charging/dis-charging current through control switches. The converter provides continuous charging and discharging current profile at low ripple with low voltage/ duty stress across the switches. The converter for bidirectional operation is simulated in MATLAB Simulink environment

and the same is experimentally validated with control implemented on the 16-bit fixed point DSP micro-controller (μC). The control algorithm of the proposed converter is capable to individually control the charging/discharging rates of the battery stack.

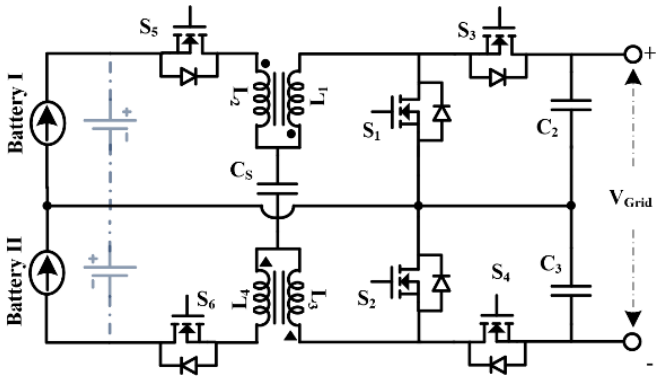


Fig 4.1 Bidirectional Multiport Impedance Converter

4.3. Operating Modes

The operation of the proposed converter can be classified under two operating modes 1) Discharging mode (batteries to DC Link); 2) Charging mode (DC Link to batteries).

4.3.1. Discharging Mode

Under discharging mode, switches S_1 and S_2 control the discharging rate of the battery stacks. Switches S_3, S_4, S_5 and S_6 are turned off, with the body diodes of the switches providing the conducting paths.

Discharging mode shown in Fig 4.2, is further subdivided, based on the switching states; 1) Switches S_1 or S_2 alone ON; 2) Switch S_1 and S_2 are both OFF; 3) Switches S_1 and S_2 are both ON. When one switch S_1 is in conduction state, the impedance capacitor (C_S) is charging through differential current of input current and current through inductor L_2. Body diode of switch S_3 is off while body diode of switch S_4 provides the returning path for the current. Current is supported by discharging capacitor C_2. For the time cycle where only S_2 is conducting the DC Link side current is supported by the capacitor C_3. When both the switches are off, input inductor L_2 charges rapidly while the energy stored in inductor L_1 is fed to the grid. The shoot through state allowing auxiliary boost capability is observed

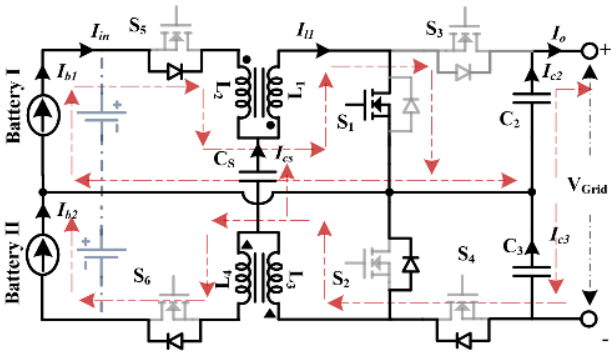


Fig 4.2.1 Discharging Mode – Only S_1 ON

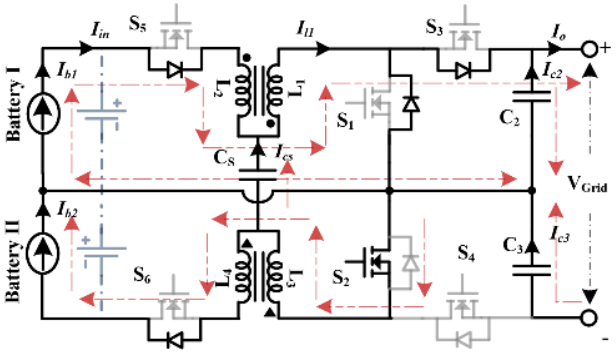


Fig 4.2.2 Discharging Mode – Only S_2 ON

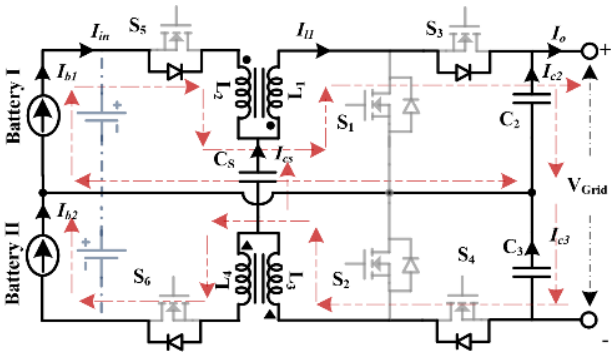


Fig 4.2.3 Discharging Mode – S_1 and S_2 OFF

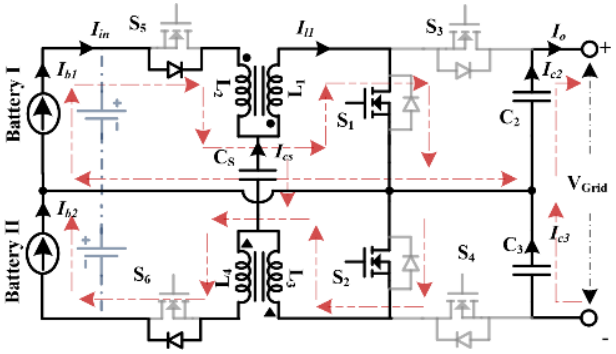


Fig 4.2.4 Discharging Mode – S_1 and S_2 ON

under simultaneous switching of S_1 and S_2, wherein capacitors C_2 and C_3 feed the load demand.

4.3.2. Charging Mode

The charging mode of operation as shown in Fig. 4.3, is governed by the switches S_3 and S_4, while switches S_1 and S_2 are turned OFF. Switches S_5 and S_6 are completely ON for this operating mode to provide continuous charging current.

The operating duty of the switches S_3 and S_4 is maintained over 50% to provide continuous charging current to the battery. Charging states can be classified under 1) Only S_3 or S_4 ON 2) Both S_3 and S_4 ON. When either S_3 or S_4 are turned on, the converter operates in buck mode. Inductor L_1/L_4 charges while inductor L_2 discharges through the battery. The body diodes of switches S_1/S_2 provide the return path for the current. A distinct advantage of the proposed converter is that the impedance capacitor acts as a pseudo source where the capacitor charges to a voltage equal to battery voltage, it discharges supporting inductor L_1/ L_3, leveling the current from the DC grid. When both switch S_3 and S_4 are ON, inductor L_1/L_3 discharges, charging inductor L_2/L_4 respectively. Capacitor C_S charges during this interval. The current across the coupled inductor and the capacitors both for the charging and discharging modes and shown in Fig. 4.4.

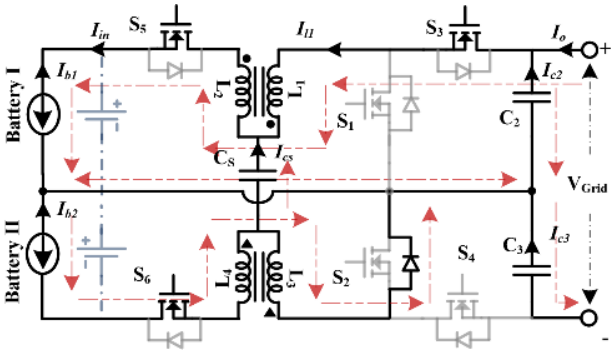


Fig 4.3.1 Charging Mode – S_3 ON

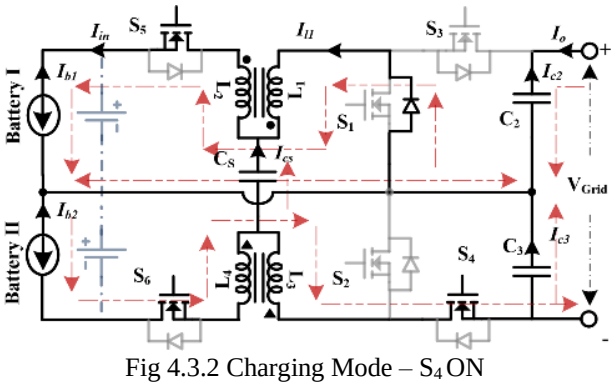


Fig 4.3.2 Charging Mode – S_4 ON

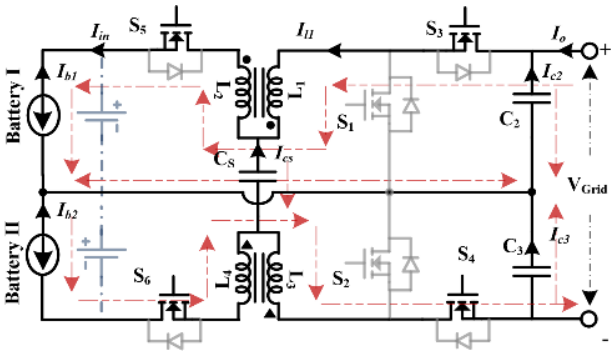


Fig 4.3.3 Charging Mode – S_3 and S_4 ON

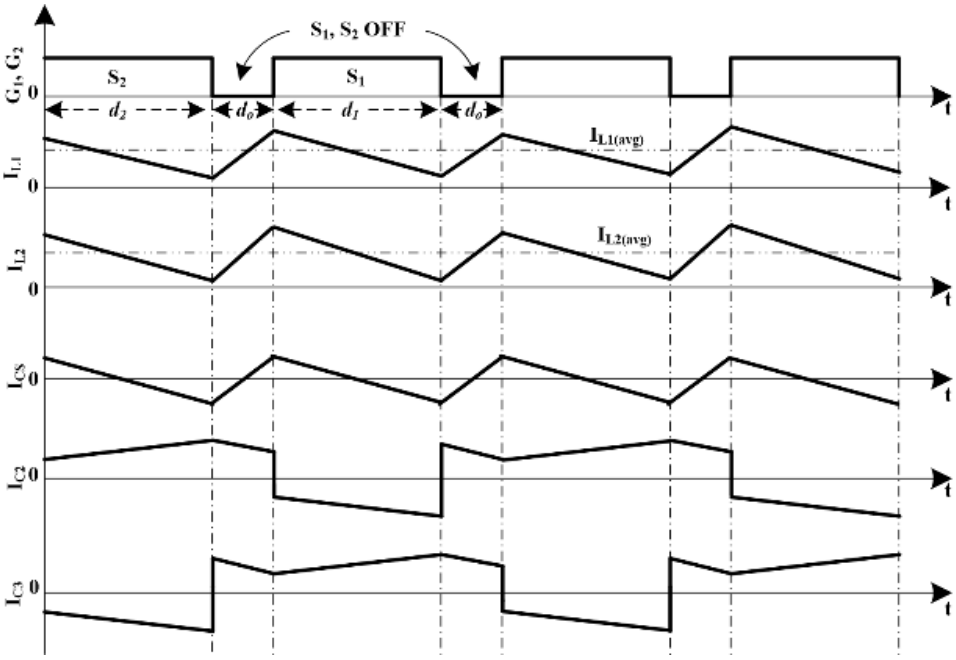


Fig 4.4.1 Discharging Mode with Operating Duty < 0.5

4.4. Converter Analysis: Current Mode and Voltage Mode

4.4.1. Converter Analysis: Current Mode

4.4.1.1. Discharging Mode

During discharging mode, the converter is capable of operating both in normal mode with operating duty less than 50% and shoot through mode with operating duty more than 50%. With reference to Fig. 4.2, the converter analysis based on the switching states for discharging mode can be subdivided into 1) S_1 and S_2 alone ON (1-2) 2) S_1 and S_2 both OFF (2) i.e., normal operating mode 3) S_1 and S_2 both ON i.e., shoot through mode (4). The capacitors C_S, C_2 and C_3 are given as below, where IC is the circulating current.

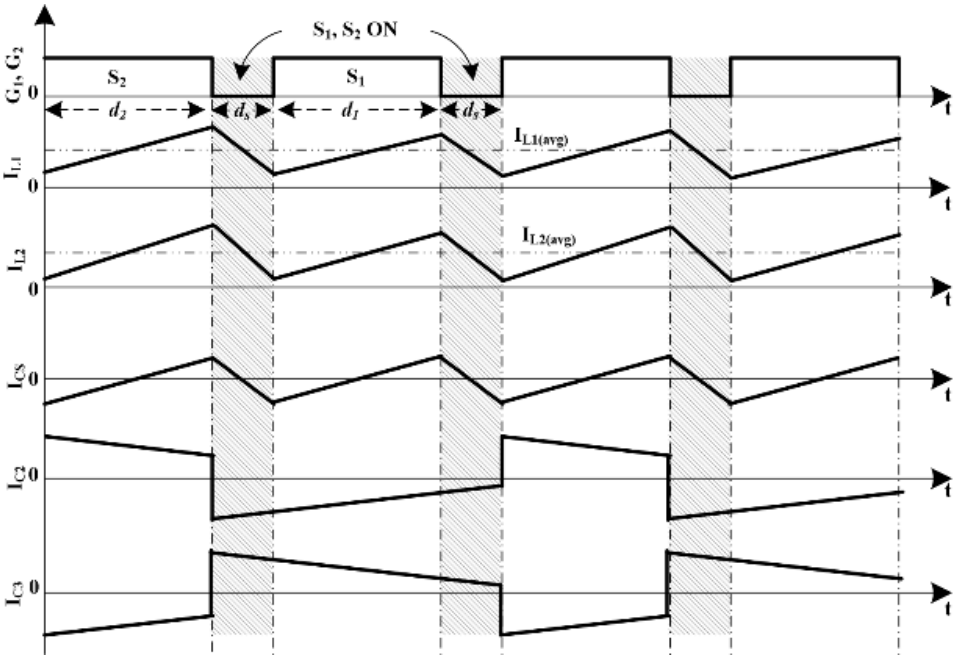


Fig 4.4.2 Discharging Mode with Operating Duty > 0.5

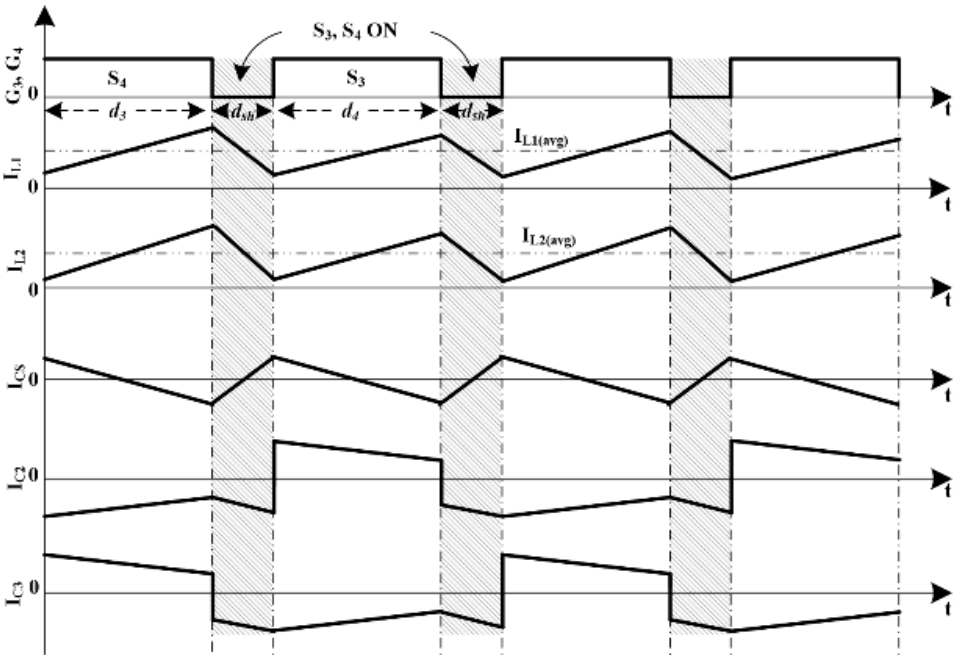


Fig 4.4.3 Charging Mode

$$I_{CS} = I_{L1} - I_{in};\ I_{C2} = I_O;\ I_{C3} = I_O + I_C - I_{L1} \quad (1)$$

$$I_{CS} = I_{L1} - I_{in};\ I_{C2} = I_O - I_{L1};\ I_{C3} = I_O \quad (2)$$

$$I_{CS} = I_{L1} - I_{in};\ I_{C2} = I_O - I_{L1};\ I_{C3} = I_C + I_{C2} \quad (3)$$

$$I_{CS} = I_{L1} - I_{in};\ I_{C2} = I_O;\ I_{C3} = I_O \quad (4)$$

Solving (1-3), we get $I_{in} = I_{L1}$ and $I_o = (1-d)I_{L1}$, Thus, relation between input and output current of the converter under normal operation is given by

$$I_o = (1-d)I_{in} \tag{5}$$

Similarly, from (1,2&4), we get $I_{in} = I_{L1}$ and $I_O = \frac{d}{(4d-1)} I_{L1}$, the transfer function for input and output current for shoot through operation is given by

$$I_O = \frac{d}{(4d-1)} I_{in} \tag{6}$$

4.4.1.2. Charging Mode

The capacitor currents for the switching states of S_3 alone ON, S_4 alone ON and S_3 and S_4 simultaneously ON is are given by (7-9) respectively.

$$I_{CS} = I_{L2} - I_{L1};\ I_{C2} = I_{L1} - I_O;\ I_{C3} = I_C + I_{C2} \tag{7}$$

$$I_{CS} = I_{L2} - I_{L1};\ I_{C2} = -I_O;\ I_{C3} = I_C + I_{C2} + I_{L1} \tag{8}$$

$$I_{CS} = I_{L2} - I_{L1};\ I_{C2} = I_{L1} - I_O \tag{9}$$

Solving (7-9), we have $I_O = \frac{(3d-1)}{(4d-1)} I_{L1}$ and $I_{in} = I_{L1}$ the transfer function for grid current and charging current during charging mode is given by

$$I_O = \frac{(3d-1)}{(4d-1)} I_{in} \tag{10}$$

Based upon the analysis under discharging mode under normal condition, the inductors and capacitors are designed,

$$L_1 = \frac{V_{B1}d}{(n+1)f\Delta I_{L1}}, L_2 = \frac{nV_{B1}d}{(n+1)f\Delta I_{L1}}, L_3 = \frac{V_{B2}d}{(n+1)f\Delta I_{L3}}, L_4 = \frac{nV_{B2}d}{(n+1)f\Delta I_{L3}} \tag{11}$$

$$C_2 = \frac{V_O d}{R\Delta V_{C2} f}\ C_3 = \frac{V_O d}{R\Delta V_{C3} f} \tag{12}$$

4.4.2. Converter Analysis: Voltage Mode

4.4.2.1. Discharging Mode

With reference to Fig. 2, the converter analysis based on the switching states for discharging mode can be subdivided into 1) S_1 and S_2 alone ON (13) and (14) 2) S_1 and S_2 both OFF (15) 3) S_1 and S2 both ON (16).

$$V_{L2} + V_{L1} - V_{L3} - V_{L4} = V_{B1} + V_{B2} - \frac{V_O}{2}; V_{L2} = nV_{L1}; V_{L4} = nV_{L3} \quad (13)$$

$$V_{L2} + V_{L1} - V_{L3} - V_{L4} = V_{B1} + V_{B2} - \frac{V_O}{2}; V_{L2} = nV_{L1}; V_{L4} = nV_{L3} \quad (14)$$

$$V_{L2} + V_{L1} - V_{L3} - V_{L4} = V_{B1} + V_{B2} - V_O; V_{L2} = nV_{L1}; V_{L4} = nV_{L3} \quad (15)$$

$$V_{L2} + V_{L1} - V_{L3} - V_{L4} = V_{B1} + V_{B2}; V_{L2} = nV_{L1}; V_{L4} = nV_{L3} \quad (16)$$

Taking voltage second balance for normal operation mode the input output transfer function can be given as (17)

$$V_O = \frac{1}{(1-d)}(V_{B1} + V_{B2}) \quad (17)$$

Where $d_1=d_2=d$ and $d_O=2(0.5-d)$. The transfer function for shoot through mode is given as (18)

$$V_O = \frac{(4d-1)}{d}(V_{B1} + V_{B2}) \quad (18)$$

Where $d_1=d_2=d$ and $d_S=2(d-0.5)$

4.4.2.2. Charging Mode

For charging operation, switches S_3 and S_4 are the governing switches controlling the charging rate. Switches S_5 and S_6 are turned ON for the complete cycle. For continuous charging of the battery stacks the operating duty of switches S_3 and S_4 is above 50%. Therefore, the steady state analysis during charging mode can be analyzed for 1) S_3 and S_4 alone ON (19) - (20) 2) S_3 and S_4 both ON (21).

$$V_{L3} + V_{L4} - V_{L2} - V_{L1} = V_{B1} + V_{B2} - \frac{V_O}{2}; V_{L2} = nV_{L1}; V_{L4} = nV_{L3} \quad (19)$$

$$V_{L3} + V_{L4} - V_{L2} - V_{L1} = V_{B1} + V_{B2} - \frac{V_O}{2}; V_{L2} = nV_{L1}; V_{L4} = nV_{L3} \quad (20)$$

$$V_{L3} + V_{L4} - V_{L2} - V_{L1} = V_{B1} + V_{B2} - V_O; V_{L2} = nV_{L1}; V_{L4} = nV_{L3} \quad (21)$$

The transfer function can be given as (22)

$$(V_{B1} + V_{B2}) = \frac{(3d-1)}{(4d-1)} V_O \tag{22}$$

Where $d_3=d_4=d$ and $d_{sh}=2(d-0.5)$.

4.5. Control Algorithm

The control algorithm for the proposed converter during charging and discharging mode is shown in Fig. 4.5 and Fig. 4.6 respectively. During power transaction from the battery stacks installed to the DC grid i.e. discharging mode, the control algorithm governs the gating of the switches S_1 and S_2. Switches S_3, S_4, S_5 and S_6 are in off state. The discharging current reference for the battery is compared to the actual current and the error is passed through PI controller. The controller is based on feed forward of steady state duty cycle to make the controller robust to variations. Under different battery SoC states, the control logic enables secondary control loop governing the operating duty of the switches depending upon the difference of the battery SoC's. The secondary control loop results in different operating duties of the switches, allowing independent discharging rates for the batteries.

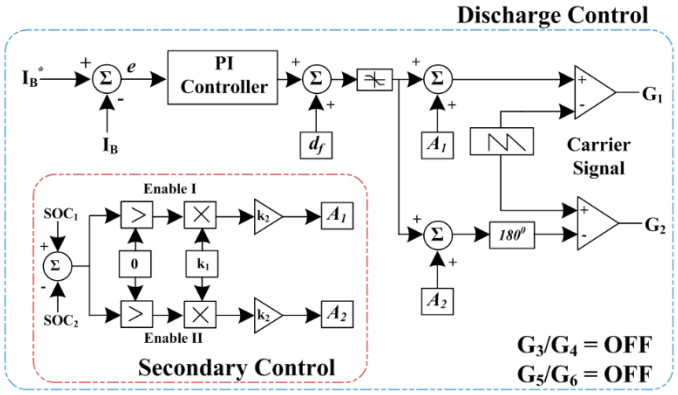


Fig 4.5 Control algorithm for Discharging Mode

During charging mode, the control parameters remain same as observed for discharging mode. The charging rate of the battery stacks can be controlled based upon the present battery SoC conditions, similar to discharging mode. The charging rate is governed by switches S_3 and S_4, while switch S_1 and S_2 are in off state. Moreover, switches S_5 and S_6 remain in conducting state during charging mode. The operating duty of the switches is

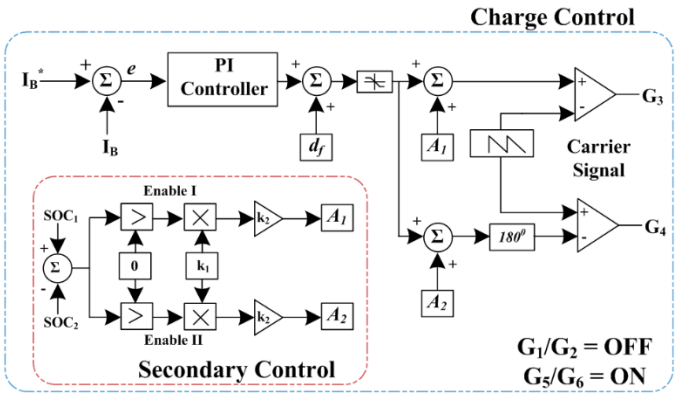


Fig 4.6 Control algorithm for Charging Mode

governed such that the battery with lower SoC charges at a faster rate. With different charging rates, as the SoC's of two batteries equalize, the batteries charge at similar rates. For continuous charging of the batteries, the operating duty of switches S_3 and S_4 is maintained above 50%.

4.6. Stability Analysis of Impedance Converter

The state space analysis for the proposed converter under both modes is formulated below for balanced conditions with L_1=L_3, L_2=L_4 and C_2=C_3. Under balance conditions circulating current (I_C) is taken 0. For discharging mode with operating duty less than 0.5, the state space matrices for the switching states based on the KVL and KCL equations for S_1 and S_2 conducting alone (23 – 24), S_1 and S_2 OFF (25);

$$A_{ON1} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{2L_1(n+1)} \\ 0 & 0 & \frac{-1}{2L_2} & \frac{-n}{2L_2(n+1)} \\ \frac{1}{C_s} & \frac{-1}{C_s} & 0 & 0 \\ \frac{-1}{C_2} & 0 & 0 & \frac{2}{RC_2} \end{bmatrix}; B_{ON1} = \begin{bmatrix} \frac{1}{L_1(n+1)} \\ \frac{n}{L_2(n+1)} \\ 0 \\ 0 \end{bmatrix} \quad (23)$$

$$A_{ON2} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{2L_1(n+1)} \\ 0 & 0 & \frac{-1}{2L_2} & \frac{-n}{2L_2(n+1)} \\ \frac{1}{C_s} & \frac{-1}{C_s} & 0 & 0 \\ \frac{-1}{C_2} & 0 & 0 & \frac{2}{RC_2} \end{bmatrix}; B_{ON2} = \begin{bmatrix} \frac{1}{L_1(n+1)} \\ \frac{n}{L_2(n+1)} \\ 0 \\ 0 \end{bmatrix} \quad (24)$$

$$A_{OFF} = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1(n+1)} \\ 0 & 0 & \frac{-1}{2L_2} & \frac{-n}{L_2(n+1)} \\ \frac{1}{C_s} & \frac{-1}{C_s} & 0 & 0 \\ \frac{-1}{C_2} & 0 & 0 & \frac{2}{RC_2} \end{bmatrix}; B_{OFF} = \begin{bmatrix} \frac{1}{L_1(n+1)} \\ \frac{n}{L_2(n+1)} \\ 0 \\ 0 \end{bmatrix} \quad (25)$$

With the state space variables $X = [I_{L1} \quad I_{L2} \quad V_{CS} \quad V_{C2}]^T$ and $Y = [V_{B1}]$. The state space averaging for the converter is computed based upon $X' = AX + Fd$, with $A=D[A_{ON1}]+D[A_{ON2}]+(1-2D)[A_{OFF}]$ and $F=[A_{ON1}+A_{ON2}-2A_{OFF}]X + [B_{ON1}+B_{ON2}-2B_{OFF}]Y$

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{d-1}{L_1(n+1)} \\ 0 & 0 & \frac{-1}{2L_2} & \frac{n(d-1)}{L_2(n+1)} \\ \frac{1}{C_s} & \frac{-1}{C_s} & 0 & 0 \\ \frac{-1}{C_2} & 0 & 0 & \frac{2}{RC_2} \end{bmatrix} \text{ and } F = \begin{bmatrix} \frac{V_{C2}}{L_1(n+1)} \\ \frac{nV_{C2}}{L_2(n+1)} \\ 0 \\ 0 \end{bmatrix} \quad (26)$$

The transfer function for small variation in current $\widehat{I_{L1}}$ and duty $\hat{d}$ respectively is computed using $\frac{\hat{x}}{\hat{d}} = [SI - A]^{-1}$ (27).

$$\frac{\widehat{I_{L1}}}{\hat{d}} = \frac{\left(s-\frac{2}{RC_2}\right)\left(\frac{1}{L_1(1+n)}\right)\left(s^2-\frac{1}{2C_sL_2}\right)V_2}{-\frac{\left(\frac{(1-d)}{L_1(1+n)}\right)\left(s^2-\frac{1}{2C_sL_2}\right)}{C_2}+\left(s-\frac{2}{RC_2}\right)\left(s^3-\frac{s}{2C_sL_2}\right)} \quad (27)$$

For shoot through, state space matrices for S_1 ON, S_2 ON remain the same as A_{ON1}, B_{ON1} and A_{ON2}, B_{ON2} (23) and (24) respectively, for the space matrix is given by (28).

$$A_{SH} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{2L_2} & 0 \\ \frac{1}{C_s} & \frac{-1}{C_s} & 0 & 0 \\ 0 & 0 & 0 & \frac{2}{RC_2} \end{bmatrix}; B_{SH} = \begin{bmatrix} \frac{1}{L_1(n+1)} \\ \frac{n}{L_2(n+1)} \\ 0 \\ 0 \end{bmatrix} \quad (28)$$

The averaging of the state space matrices is based on the relation $A=D[A_{ON1}]+D[A_{ON2}]+(2D-1)[A_{SH}]$ and $F= [A_{ON1}+A_{ON2}+2A_{SH}]X + [B_{ON1}+B_{ON2}+2B_{SH}]Y$, given by (29)

$$A=\begin{bmatrix} 0 & 0 & 0 & \frac{-D}{L_1(n+1)} \\ 0 & 0 & \frac{1-4D}{2L_2} & \frac{-Dn}{L_2(n+1)} \\ \frac{-1+4D}{C_S} & \frac{1-4D}{C_S} & 0 & 0 \\ \frac{-2D}{C_2} & 0 & 0 & \frac{-2+8D}{RC_2} \end{bmatrix} \text{ and } F=\begin{bmatrix} \frac{-V_{C2}+4V_{B1}}{L_1(n+1)} \\ \frac{-nV_{C2}+4nV_{B1}}{L_2(n+1)} - \frac{2V_S}{L_2} \\ \frac{4(I_{L1}-I_{L2})}{C_s} \\ \frac{-2I_{L1}}{C_2} + \frac{8V_{C2}}{RC_2} \end{bmatrix} \quad (29)$$

The transfer function of current $\widehat{I_{L1}}$ and duty $\hat{d}$ is (30).

$$\frac{\widehat{I_{L1}}}{\hat{d}} = \frac{\left(s^2-\frac{(16d^2-8d+1)}{2C_SL_2}\right)}{\left(\frac{-4d^2\left(s^2-\frac{1-8d+16d^2}{2C_SL_2}\right)}{2C_2L_1(1+n)}+\left(s+\frac{2-8d}{RC_2}\right)\left(s^3-\frac{s(16d^2-8d+1)}{2C_SL_2}\right)\right)}\left(\frac{\frac{4d}{C_2}\left(-I_{L1}+4\frac{V_2}{R}\right)}{2L_1(1+n)}+\frac{\left(s+\frac{2(1-4d)}{RC_2}\right)\left(\frac{-V_2+4V_{B1}}{L_1(1+n)}\right)}{1}\right) \quad (30)$$

State space matrices for charging mode with variables $X = [I_{L1} \quad I_{L2} \quad V_{CS}]^T$ and $Y = [V_{C2}]$ for the switching state S_3 and S_4 alone ON (31)-(32), S_3 and S_4 alone ON (33) is

$$A_{CON1} = \begin{bmatrix} 0 & 0 & \frac{1}{2L_1(n+1)} \\ 0 & 0 & \frac{n}{2L_2(n+1)} \\ \frac{-1}{C_s} & \frac{1}{C_s} & 0 \end{bmatrix}; B_{CON1} = \begin{bmatrix} \frac{1}{2L_1(n+1)} \\ \frac{n}{2L_2(n+1)} \\ 0 \end{bmatrix} \quad (31)$$

$$A_{CON2} = \begin{bmatrix} 0 & 0 & \frac{1}{2L_1(n+1)} \\ 0 & 0 & \frac{n}{2L_2(n+1)} \\ \frac{-1}{C_s} & \frac{1}{C_s} & 0 \end{bmatrix}; B_{CON2} = \begin{bmatrix} \frac{1}{2L_1(n+1)} \\ \frac{n}{2L_2(n+1)} \\ 0 \end{bmatrix} \quad (32)$$

$$A_{CSH} = \begin{bmatrix} 0 & 0 & \frac{1}{2L_1(n+1)} \\ 0 & 0 & \frac{n}{2L_2(n+1)} \\ \frac{-1}{C_s} & \frac{1}{C_s} & 0 \end{bmatrix}; B_{CSH} = \begin{bmatrix} \frac{-1}{2L_1(n+1)} \\ \frac{-n}{2L_1(n+1)} \\ 0 \end{bmatrix} \quad (33)$$

State space averaging is based on $A=D[A_{CON1}]+D[A_{CON2}]+(2D-1)[A_{CSH}]$ and $F=[A_{CON1}+A_{CON2}+2A_{CSH}]X + [B_{CON1}+B_{CON2}+2B_{CSH}]Y$, and is given by (34).

$$A=\begin{bmatrix} 0 & 0 & \frac{4d-1}{2L_2(n+1)} \\ 0 & 0 & \frac{n(4d-1)}{2L_1(n+1)} \\ \frac{1-4d}{C_s} & \frac{-(1-4d)}{C_s} & 0 \end{bmatrix} \text{ and } F=\begin{bmatrix} \frac{2V_S}{L_1(n+1)} \\ \frac{2nV_S}{L_1(n+1)} \\ \frac{-4(I_{L1}-I_{L2})}{C_s} \end{bmatrix} \quad (34)$$

The transfer function in reference to small variation in parameter I_{L1} and d is given by (35).

$$\frac{\widehat{I_{L1}}}{\widehat{d}} = \left(\frac{1}{s^3+\frac{s(16d^2-8d+1)}{2C_S}\left(\frac{1}{L_1(1+n)}-\frac{2}{L_2(1+n)}\right)}\right)\left(\frac{\frac{4s(I_{L2}-I_{L1})(4d-1)}{2C_SL_1(1+n)}+\frac{4n(16d^2-8d+1)V_S}{2C_SL_1(1+n)}}{2L_2(1+n)}+\frac{4V_s\left(s^2-\frac{n(16d^2-8d+1)V_S}{2C_SL_2(1+n)}\right)}{2L_1(1+n)}\right) \quad (35)$$

The bode pot for discharging and charging state is as shown in Fig. 4.7.1 and Fig. 4.7.2 respectively. From the plot, the cross over frequency of the converter is 39kHz with positive phase margin and infinite gain margin, thereby confirming stable operation of the converter in charging and discharging mode. The stability is further verified via Nyquist stability criteria for both the discharging and charging mode of operation as shown in Fig. 4.8. An ideal system is considered with the system parameters as specified in TABLE I. The Nyquist contour encircles the right half of s plane for all the operating modes as shown in Fig. 8, thereby affirming the controller's stability under both the operating mode.

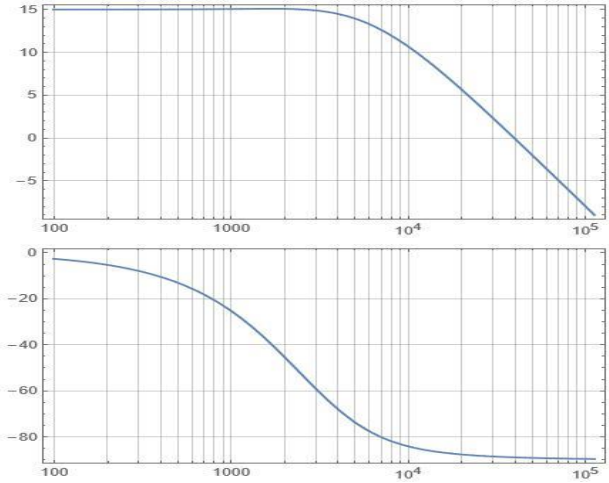


Fig 4.7.1 Stability Plot – Discharging Mode

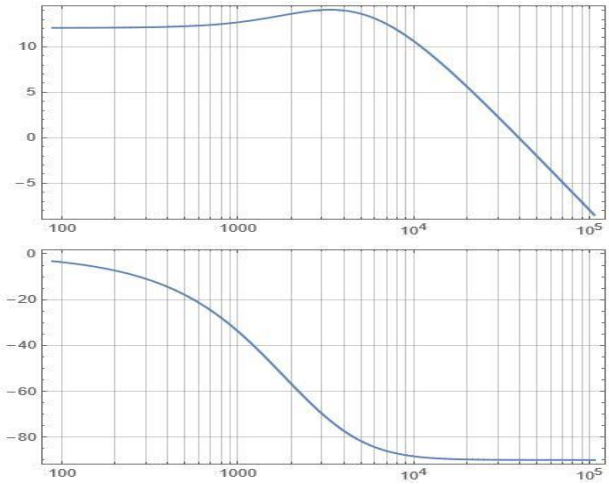


Fig 4.7.2 Stability Plot – Charging Mode

4.7. MATLAB Based Simulation of Bi – Directional Multiport Impedance Converter

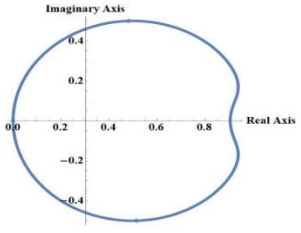
The presented grid interfaced bidirectional converter is designed and simulated in MATLAB Simulink. Two 12V/17Ah lead acid batteries representing battery stacks and multi – input supply of the impedance converter interfaced with 48V LVDC grid. The converter parameters are shown in TABLE IV.

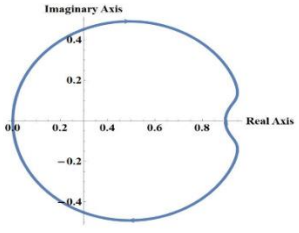
TABLE IV SIMULATION PARAMETER

Quantity	Value
Battery Specification	12V/17Ah
DC Grid Voltage	48V
Inductor (L_1)	170µH
Inductor (L_2)	680µH
Turns Ratio	2
Impedance Capacitor (C_S)	220µF
Output Capacitor (C_2 & C_3)	47µF
Switching Frequency (f_s)	50kHz

4.7.1. Transition from Discharging to Charging State

The dynamic response of converter under transition from discharging to charging state is shown in Fig.4.9. Fig.4.9.1. shows the dynamics of input side i.e., input voltage (V_{IN}), impedance capacitor voltage (V_S), battery stacks current (I_{B1} & I_{B2}) and SoC of the batteries (SoC_1/SoC_2). The grid voltage (V_G) and grid current (I_O) along with the common mode current (I_C) is shown in Fig.4.9.2. Initially, both the batteries with same SoC of 80%, discharge at a constant rate of 3.4A. The cumulative battery voltage at the input and the impedance capacitor is maintained at 24.2V. The LVDC grid maintained at 48V is fed by continuous current of 1.65A. At t = 0.5s, the controller transits from discharging to charging mode. The voltage across the capacitor now governed by the grid rises to 25.3V.





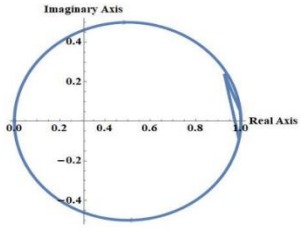


Fig 4.8.1 Discharging Mode (Normal Operation); Fig 4.8.2 Discharging Mode (Shoot Through); Fig 4.8.3 Charging Mode

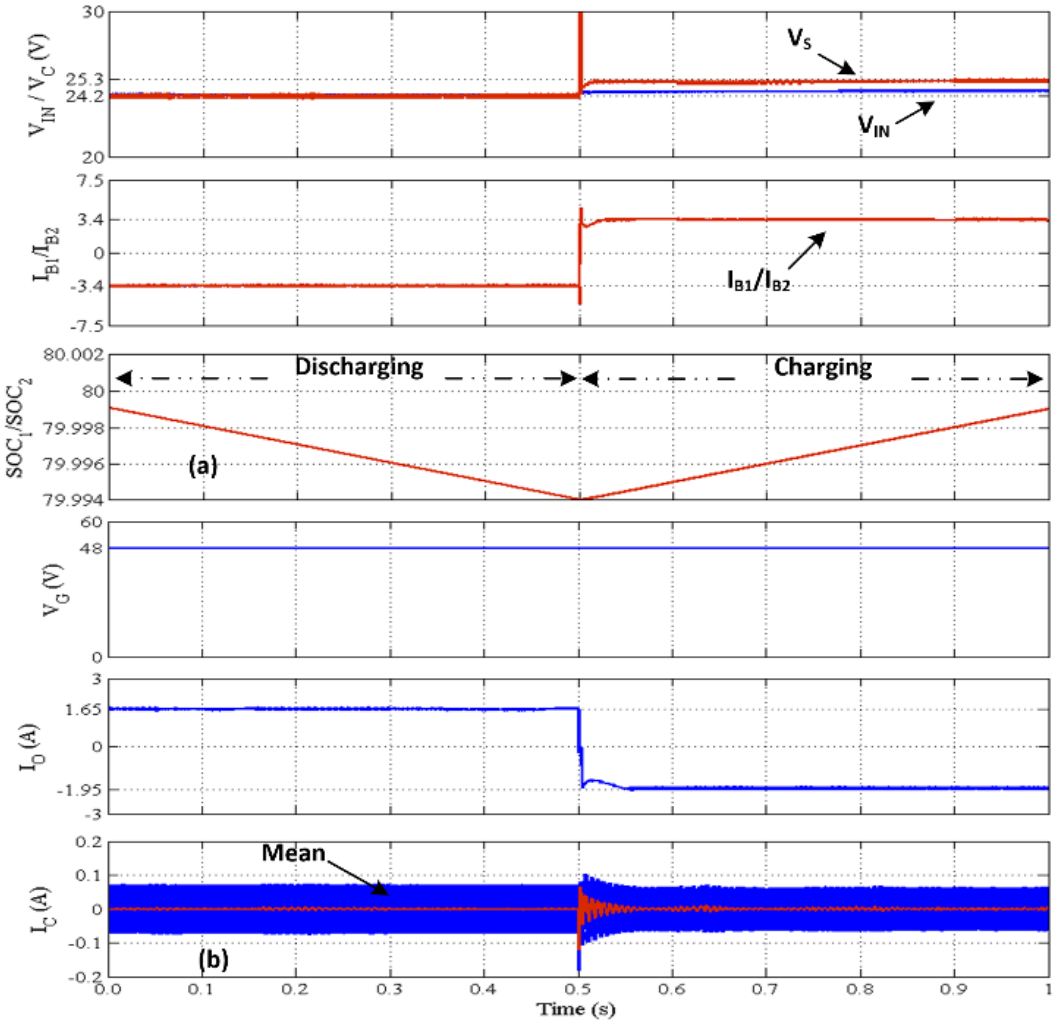


Fig. 4.9 Discharge to charge mode – a) i)Input & capacitor voltage (V_{IN} & V_C) ii) Battery currents(I_{B1} & I_{B2}) iii)SoC (SoC_1 & SoC_2) b) iv) Grid Voltage (V_G) v) Grid Curr (I_G) vi) Converter current (I_C)

The battery is charged at a fixed rate equivalent to C/5 i.e., 3.4A. The charger draws 1.95A from the grid. The initial SoC's of the batteries is considered equal hence the common mode current is averaged 0 as shown in Fig. 9b. The zoomed profile of the converter dynamics during both discharging and charging state is shown in Fig 4.10 and Fig. 4.11 respectively. The current ripple across the battery in discharging state is 0.4A. While the ripple in grid current and common mode current is 0.1A and 0.2A respectively. During charging mode, ripple of 0.4A is maintained across the battery stacks with ripple of 0.1A and 0.2A in I_G and I_C respectively.

4.7.2. Charging Discharging at Different SoC

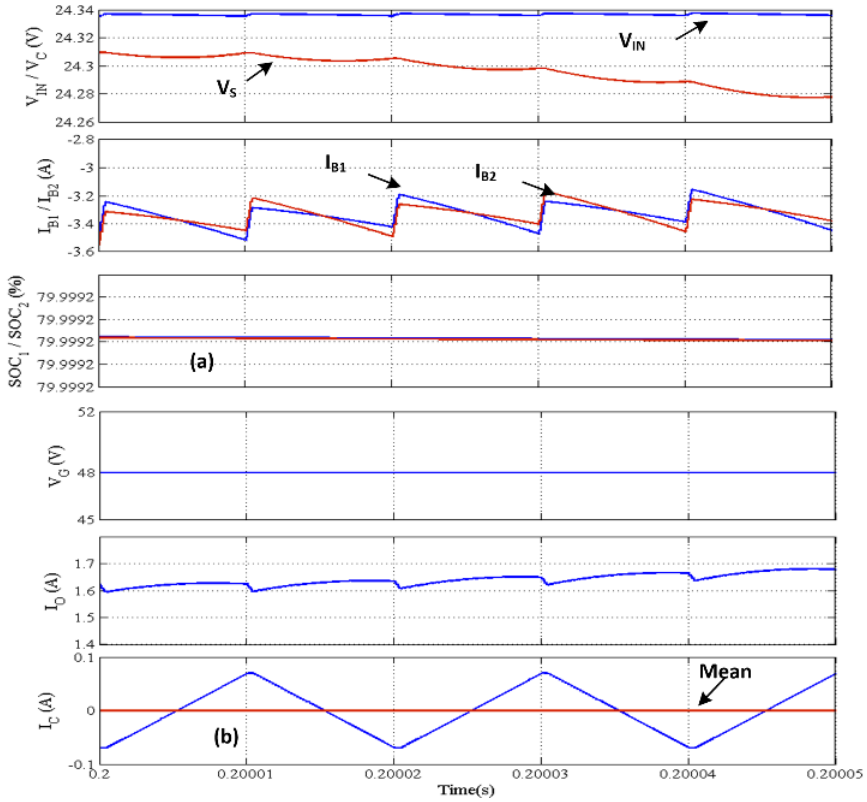


Fig. 4.10 Dynamics – Discharging Mode

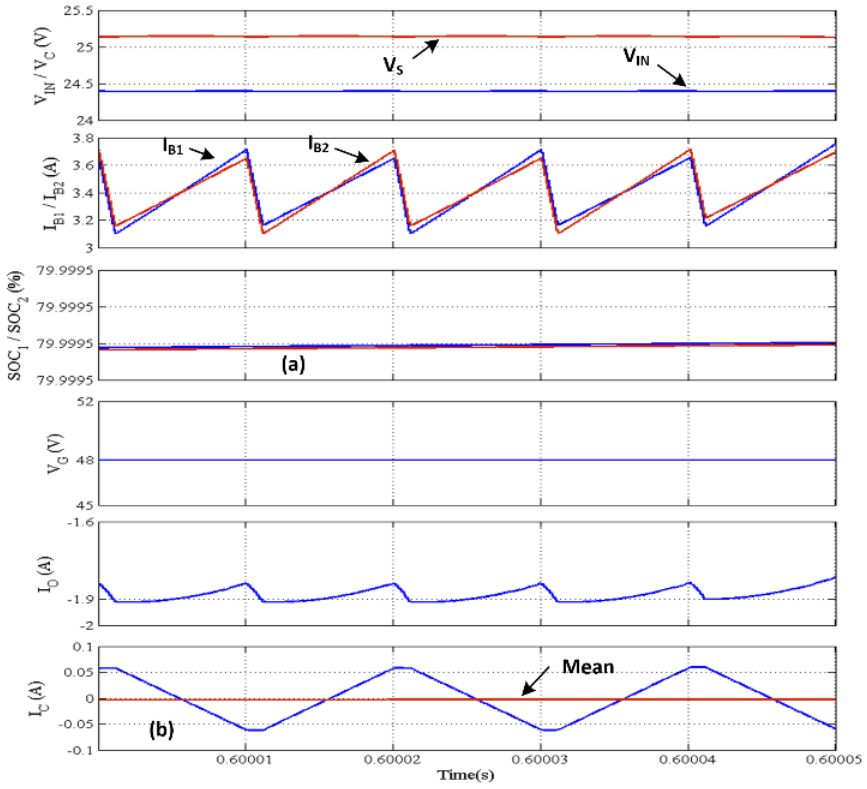


Fig. 4.11 Dynamics – Charging Mode

The response of converter with the batteries at different SoC's charging at a different rate is shown in Fig. 4.12. The initial SoC of the two batteries is maintained at 80% for battery 1 and 79.5% for battery 2. The battery with SoC at 79.5% initially charges at a constant current of 3.5A, such that a balance among the batteries can be achieved, while the second

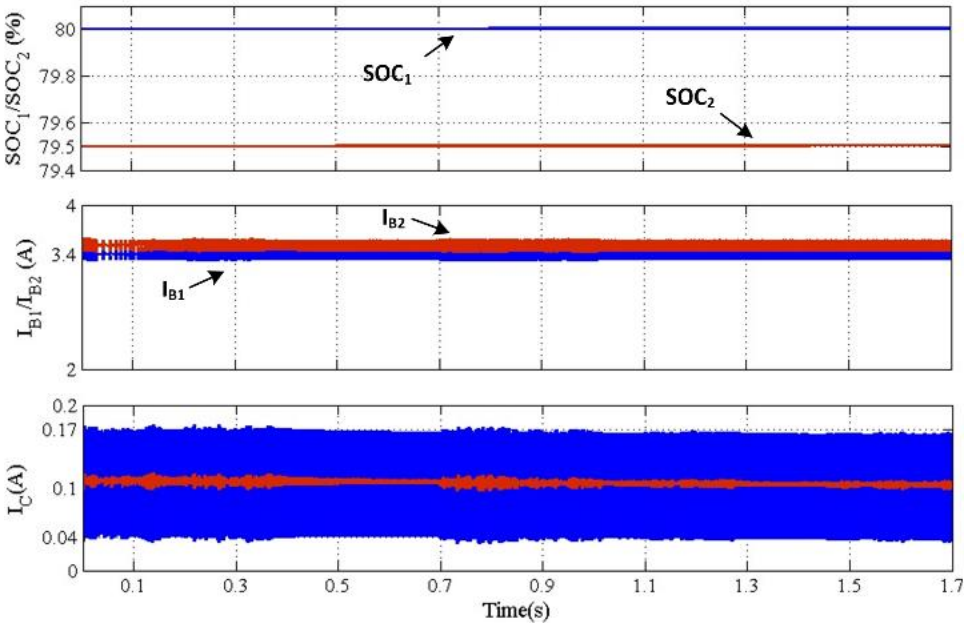


Fig. 4.12 Charging at different SoC i) SoC (SoC_1 & SoC_2) ii) Battery current (I_{B1} & I_{B2}) iii) Conv. current

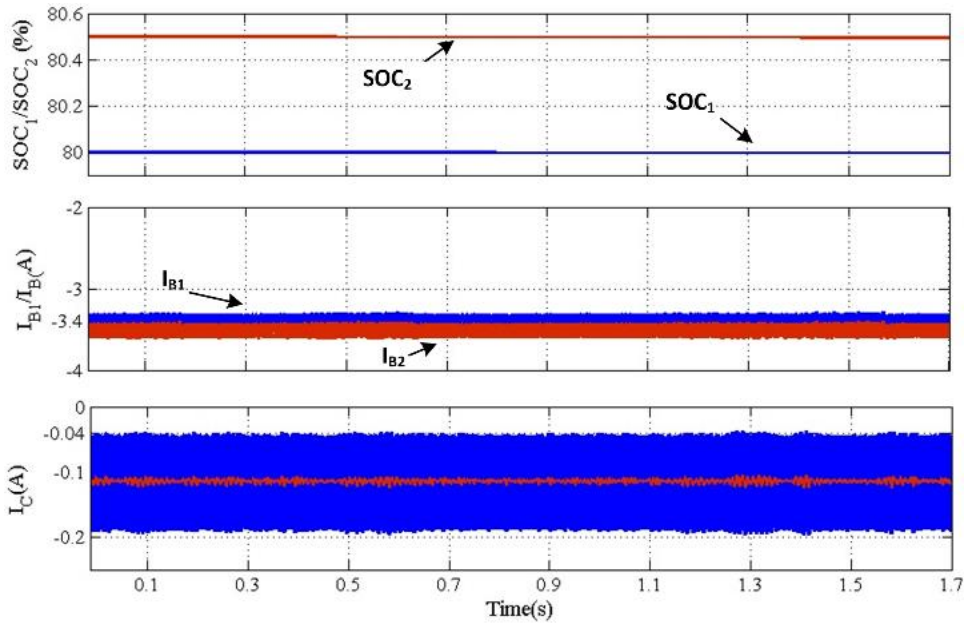
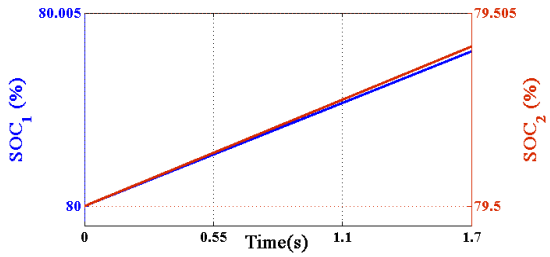


Fig. 4.13 Discharging at different SoC i) SoC (SoC_1 & SoC_2) ii) Battery current (I_{B1} & I_{B2}) iii) Conv. current

battery with SoC at 80% charges at a current of 3.4A. As the gradient in SoC of the two batteries reduces, the charging current of battery 2 reduces. The capacitor 1.9A from LVDC



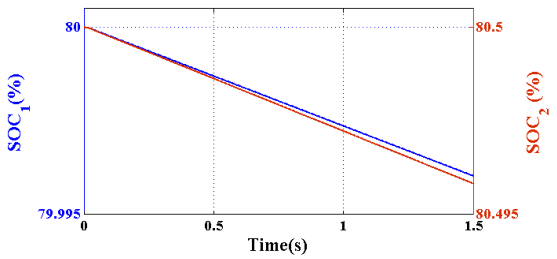


Fig. 4.14.1 Charging at Different Rates; Fig. 4.14.2 Discharging at Different Rates;

grid to charge the batteries. As the t wo batteries have different SoC, an average common mode current of 0.1A is observed. The dynamic response of the converter for batteries with different SoC's discharging at different rates is shown in Fig 4.13. The initial SoC of battery 1 and battery 2 is considered at 80% and 80.5% respectively. Battery 2 being healthier discharges at 3.5A and battery 1 discharges at 3.4A. The grid is fed by constant current of 1.6A. The impedance capacitor voltage is maintained equal to input voltage of 24.5V. The common mode current is observed to be -0.1A. As the difference in the SoC's is reduced, the discharging current of battery 2 reduces. The difference in charging and discharging rates of the batteries with respect to SoC is given in Fig 4.14.

4.8. Experimental Analysis of Bi – Directional Multiport Impedance Converter

A prototype of the proposed bidirectional impedance source converter is experimentally validated. 12V/7Ah batteries are taken at the input side of the converter, representing the battery stacks, 48V grid is maintained through 4, 12V/17Ah batteries. The control is embedded in 16-bit DSP microcontroller dsPIC33FJ16GS502 ensuring low cost. The analog sampling is at 600Hz triggered through the timer module. The PI controller works on the principle of repeated error correction.

4.8.1. Experimental Response – Discharging to Charging

The dynamic response of the developed prototype for transition from V2G to G2V is shown in Fig. 4.15. The voltage parameters corresponding to the converter i.e., grid voltage (V_G), impedance capacitor voltage (V_S) and the battery voltages (V_{B1} & V_{B2}) are shown in Fig. 4.15.1. The converter output current (I_{OUT}) and battery currents (I_{B1} & I_{B2}) are shown in

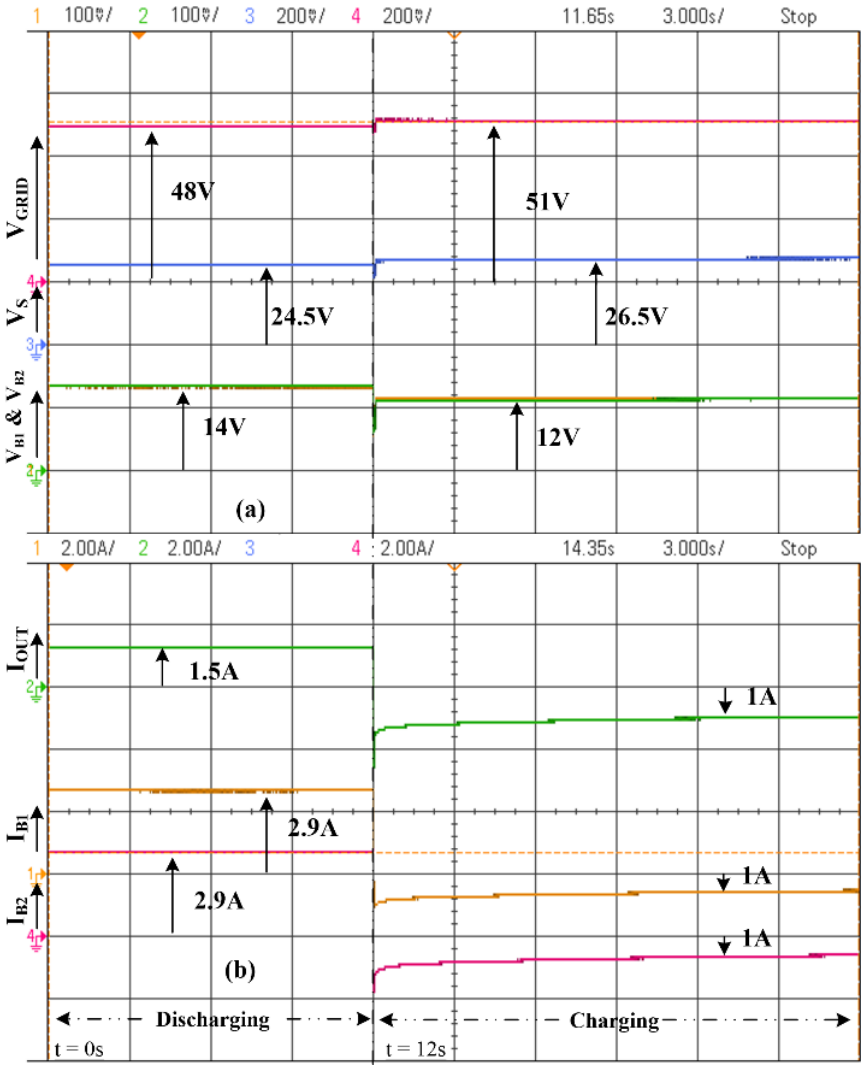


Fig. 4.15 Discharge to charge – i) Grid Voltage (V_G) ii) capacitor voltage (V_S) iii) Battery Voltage (V_{B1}) iv) Battery Voltage (V_{B2}) v) Converter current (I_O) vi) Battery currents (I_{B1}) vii) Battery currents (I_{B2})

Fig. 4.15.2. Initially, both the batteries discharge at 2.9A. The terminal voltage of both the batteries is maintained at 14V and the grid voltage is at 48V. The voltage across the impedance capacitor is 24.5V, and the converter feeds 1.5A to the LVDC µG. At t=12s, the converter transits from discharging mode to charging mode, with grid voltage rising to 51V (battery stack) feeding 1A to the converter. The converter charges the battery at a current of 1A, with the battery voltages at 12V respectively. The impedance capacitor voltage rises to 26.5V due to reverse power flow.

4.8.2. Experimental Response – Different SoC

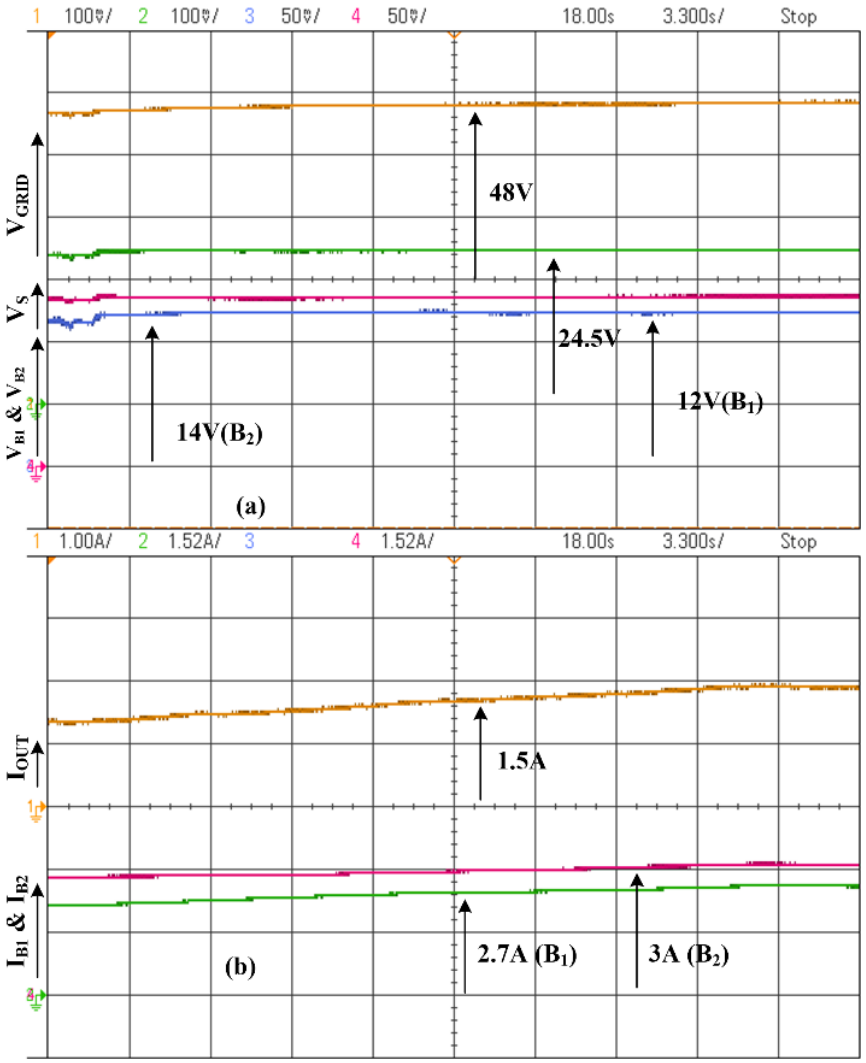


Fig. 4.16 Discharge at different SoC – i) Grid Voltage (V_G) ii) capacitor voltage (V_S) iii) Battery Voltage (V_{B1}) iv) Battery Voltage (V_{B2}) v) Converter current (I_O) vi) Battery currents (I_{B1}) vii) Battery currents (I_{B2})

Fig 4.16 exhibits the converter response for input side batteries discharging at different SoC, the voltages across batteries 1 & 2 are at 12V and 14V respectively. The LVDC grid and impedance capacitor voltage is maintained at 48V and 24.5V respectively. Battery 2 at higher SoC discharges at a higher rate of 3A while battery 1 discharges at 2.7A. It may be observed that the slope of the discharging current of battery 2 gradually decreases as the difference in voltage reduces. To affirm the capability of the converter, the response with the batteries charging at different SoC's is shown in Fig 4.17. The battery voltages of battery 1 and 2 are kept at 12.5V and 12V respectively. Battery 2 being at lower SoC, charges at a current of 1.1A while battery 1 charges at 900mA. The grid and the impedance capacitor voltage is maintained at 48V and 25.5V respectively.

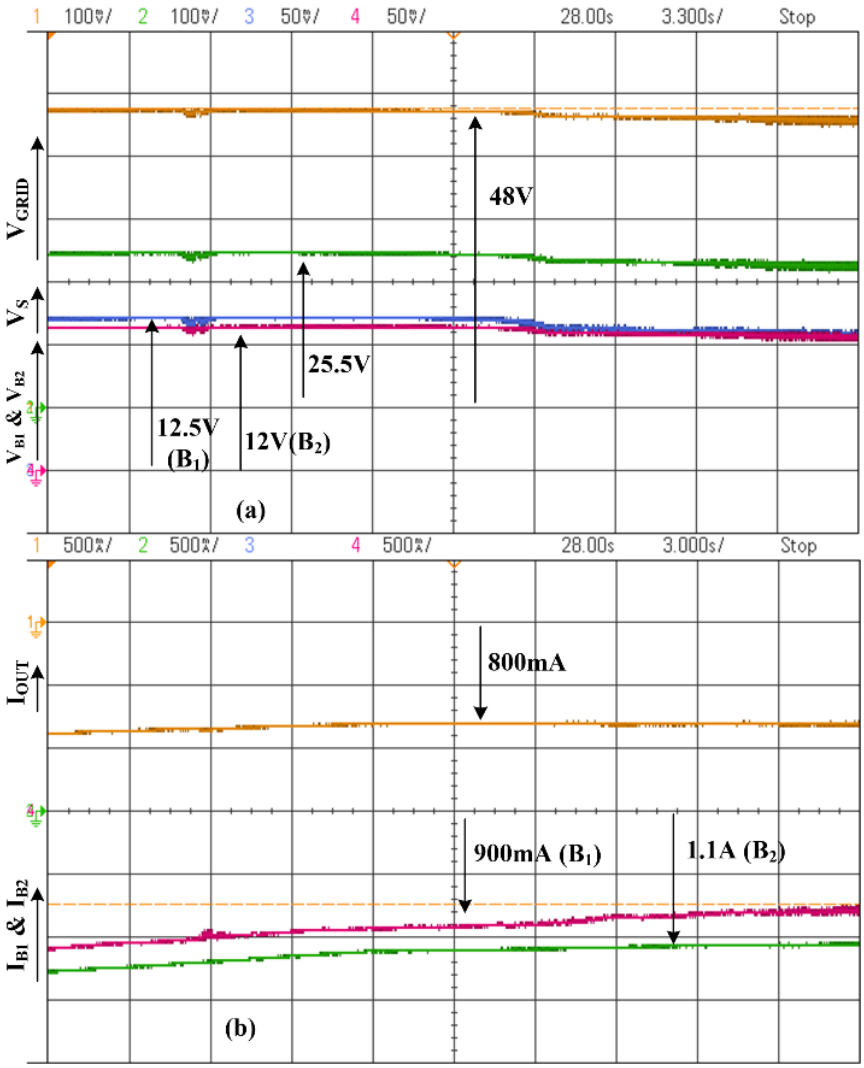


Fig. 4.17 Charge at different SoC – i) Grid Voltage (V_G) ii) capacitor voltage (V_S) iii) Battery Voltage (V_{B1}) iv) Battery Voltage (V_{B2}) v) Converter current (I_O) vi) Battery currents (I_{B1}) vii) Battery currents (I_{B2})

4.9. Performance Analysis

A comparison is drawn between the conventional bidirectional buck boost converter and the proposed impedance converter as shown in Fig. 4.18. For a low input voltage of 18.5V representing the deep discharge condition, the operating duty for the proposed impedance converter is significantly less than conventional buck boost converter. With higher battery voltage, the impedance converter for an output of 48V, operates at a duty significantly less than buck boost converter, reducing the loss and stress across the converter. Fig. 4.19.1 and

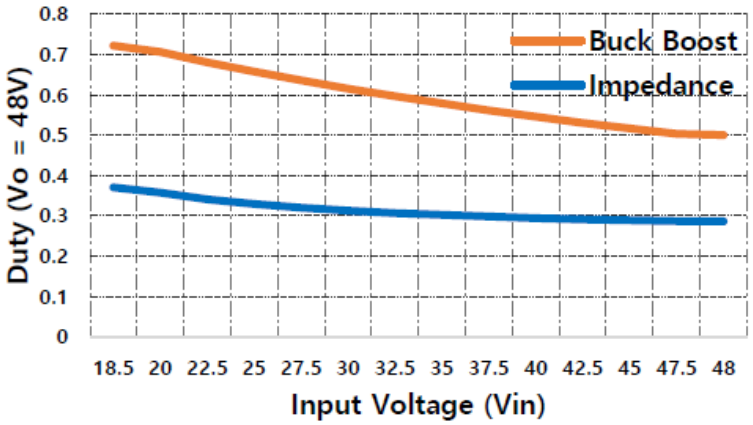


Fig. 4.18 Performance comparison conventional buck boost converter and impedance converter

Fig. 4.19.2 depicts the gain curves of the proposed converter (taking $V_{B1} = V_{B2}$) for both boost and buck operation respectively in comparison to conventional low – cost converter as TABLE V.

TABLE V COMPARATIVE ANALYSIS

Converter	Boost	Buck
Impedance (Orange)	$\frac{2}{(1-d)}, \frac{2*(4d-1)}{d}$	$\frac{2*(3d-1)}{(4d-1)}$
Buck Boost (Red)	$\frac{d}{(1-d)}$	$\frac{(1-d)}{d}$
Coupled Ind Bidirectional (Blue)	$\frac{(1+d)}{(1-d)}$	$\frac{d}{(2-d)}$
Cascaded Bidirectional (Aqua)	$\frac{1}{(1-d)}$	d
Inter. Charge Pump (Green)	$\frac{2}{(1-d)}$	$\frac{d}{2}$

Fig 4.19.1 and Fig. 4.19.2 affirms superior buck and boost curves of the proposed converter in comparison to conventional non isolated bidirectional converters. For duty greater than 0.5 in boost mode, the gain of the proposed converter is linear as duty increases, while the remaining converters enter unstable operating region. The comparison maintains the superior and wide operating range of the impedance converter over the conventional bidirectional converters by virtue of the impedance network providing auxiliary boost.

4.10. Conclusion

The simulation and hardware results affirm bidirectional and wide operating capability of the proposed impedance converter. The results demonstrate the proposed multiport

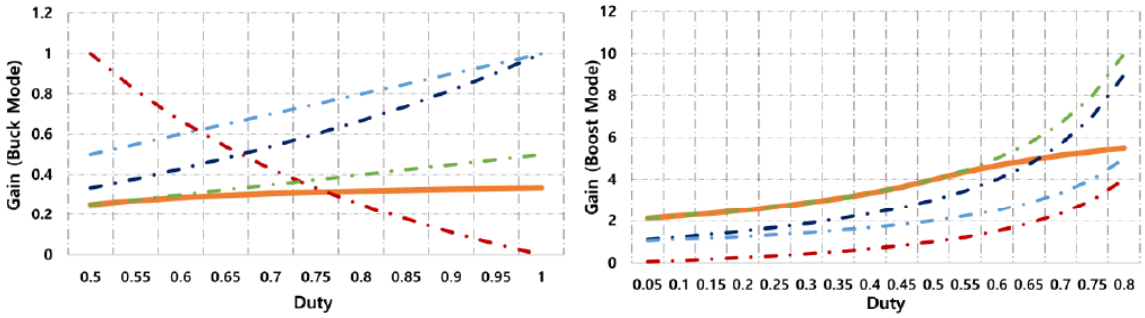


Fig. 4.19.1 Gain Curve (Buck Mode); Fig. 4.19.2 Gain Curve (Boost Mode)

converters capability of configurable charging & discharging of the connected battery stacks based upon the state of charge (SoC) of the individual batteries, significantly reducing the battery degradation. Control over individual battery from a simple control algorithm allows flexibility in control of the modular, power dense and low ripple converter, allowing direct coupling of converter with DC grid.

Chapter V

DOUBLE FREQUENCY PHASE LOCKED LOOP FOR GRID CONNECTED INVERTER

5.1. Problem formulation

To inject clean real and reactive power into the grid it is essential to determine the phase and frequency of the grid, thereby requiring a phase locked loop (PLL). Under weak grid conditions, the interaction between the control algorithm and the grid conditions result in harmonic resonance within the system. The phase locked loop ensures precise synchronization of the interfaced inverter with the grid along with providing ride through capability.

It is important that that the synchronization algorithm should be capable of detecting and adapting to the intermittent conditions on the grid in least possible time, besides exhibiting the capability of accurate transient tracking i.e., the response of the synchronization algorithm should match the fast dynamics of the low inertia inverter assuring the ride through capability, complying with the grid codes. Furthermore, the frequency adaptive algorithm should also allow co – operative synchronization of inverters having different dynamics (due to type of hardware/type of controllers) generating distortion free reference and nullifying the circulating current flow between the inverter modules. With the impedance of the phase locked loop acting as a parallel admittance to the inverters output admittance significantly influences the systems stability. A PLL algorithm with wide bandwidth along with the dynamics of Quadrature Signal Generator (QSG) may result in grid instability under weak grid conditions or grid perturbations. Moreover, when the frequency exceeds the nominal frequency (f_O) i.e., $f > f_O$ a phase shift is observed in the phase frequency curve, the stability of the system decreases with the decrease in the amplitude and phase angle of both the grid and PLL admittance.

5.2. Proposed Double Frequency Phase Locked Loop

This chapter proposes a synchronization algorithm based on Second Order Generalized Integrator (SOGI) adaptive filter resonating at second harmonic frequency i.e., 100 Hz as shown in Fig. 5.1. The double frequency adaptive filter ensures the improved phase and amplitude gains at greater nominal frequency expanding the stable operating region. The adaptive filter resonating at 100 Hz reduces the system settling and damping time, along with limiting the transient overshoots and undershoots, hence improving the transient tracking capability of the system. Taking 2nd harmonic frequency of 100 Hz as the resonating frequency curbs the low harmonic resonance observed under perturbations and weak grid conditions. The synchronization algorithm is validated for various grid perturbations resembling a weak grid condition. The response of the algorithm is analyzed in respect to the response of conventional SOGI – PLL

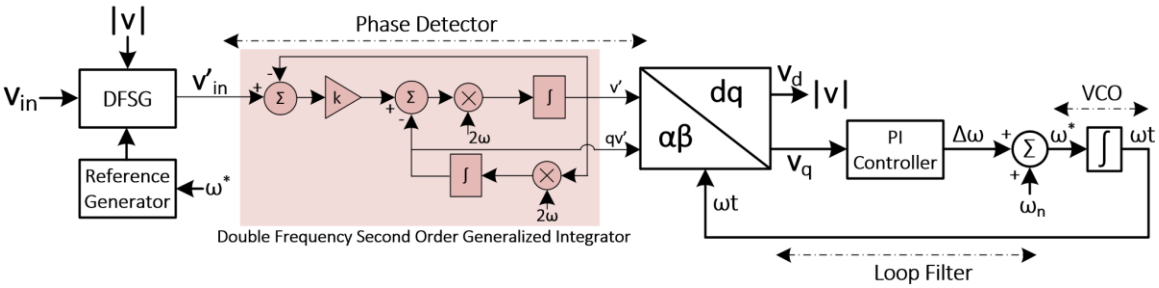


Fig. 5.1 Proposed Double Frequency Synchronization Algorithm

5.2.1. Control

The synchronization algorithm utilizes the benefits of the second order generalized integrator (SOGI) resonating at double of fundamental frequency. The algorithm focuses on the dynamic performance of the synchronization algorithm under grid disturbances. The algorithm is based upon the phase detector (PD), loop filter (LF) and voltage-controlled oscillator (VCO). Operation at double frequency allows dynamic transient tracking, allowing the systems to be compliant with the stringent grid codes making it a vital characteristic for low inertial power converters. The algorithm is based on SOGI adaptive filter resonating at *2ω* and generating quadrature signals v'' and qv''. The input to the SOGI adaptive filter is converted to double frequency using a double frequency signal generator (DFSG) and reference generator (RG). The quadrature signal generated through SOGI are converted into direct and quadrature signals v_d and v_q using parks transformation, with v_q

determining the phase error and v_d giving the magnitude of the grid voltage. The phase error identified through v_q is compensated through a proportional integral controller. The voltage-controlled oscillator generates the sine and cosine signals both at double frequency (2ω) and fundamental frequency (ω) for controller reference generation.

5.3. Analysis of Double Frequency Synchronization Algorithm

For an input voltage signal $v_{in} = v_m sin\ (\omega t + \varphi)$ where v_m, ω and φ is the peak voltage, frequency and phase of the grid voltage, the double frequency input for the SOGI adaptive filter is generated through reference generator using (1),

$$v'_{in} = v_m(1 - [2 * sin\ (\omega t + \varphi)^2]) = v_m \cos 2(\omega t + \varphi) \qquad (1)$$

DFSOGI adaptive filter resonating at 2ω generates the in phase and quadrature signals v' and qv' eliminating the requirement of Clarke transformation. In addition, the DFSOGI adaptive filter signals v' and qv' acts as band pass and low pass filter as shown in Fig. 5.2.

The transfer functions $G'_{\alpha}(s)$ and $G'_{\beta}(s)$for are given by (2) and (3) respectively.

$$G'_{\alpha}(s) = \frac{v'(s)}{v'_{in}(s)} = \frac{2k\omega s}{s^2+2k\omega s+4\omega^2} \qquad (2)$$

$$G'_{\beta}(s) = \frac{qv'(s)}{v'_{in}(s)} = \frac{4k\omega^2}{s^2+2k\omega s+4\omega^2} \qquad (3)$$

The time response of (2) and (3) for input of $v_m \cos 2(\omega t + \varphi)$ is given by (4) and (5) respectively, where v' is the in-phase signal and qv' is the quadrature signal with peak magnitude v_m.

$$v'(t) = \frac{v_m*(\cos 2(\varphi+\omega t)*\sqrt{k^2-4})+2\sin h(\omega t\sqrt{k^2-4})*\sin 2\varphi*e^{-kt\omega}+k\cos(2\varphi)*\sin h(\omega t\sqrt{k^2-4})*e^{-kt\omega}-\cos h(\omega t\sqrt{k^2-4})*\cos 2\varphi*e^{-kt\omega}))}{\sqrt{k^2-4}} \quad (4)$$

$$qv'(t) = \frac{-v_m*(\cos(2\varphi)*\sin h(\omega t\sqrt{k^2-4})*e^{-kt\omega}-\sin 2(\varphi+\omega t)*\sqrt{k^2-4})+k\sin h(\omega t\sqrt{k^2-4})*\sin 2\varphi*e^{-kt\omega}+\cos h(\omega t\sqrt{k^2-4})*\sin 2\varphi*e^{-kt\omega}\sqrt{k^2-4}))}{\sqrt{k^2-4}} \quad (5)$$

The parks transformation of the signals v' and qv' gives the signal v_d and v_q, where v_d represents the peak grid voltage and v_q gives the phase error which damps with time constant $\frac{1}{k\omega}$. At instance where $\omega = \omega_n$ (nominal frequency) i.e., $v_q = 0$, phase error is zero and the sinusoidal reference signal is generated.

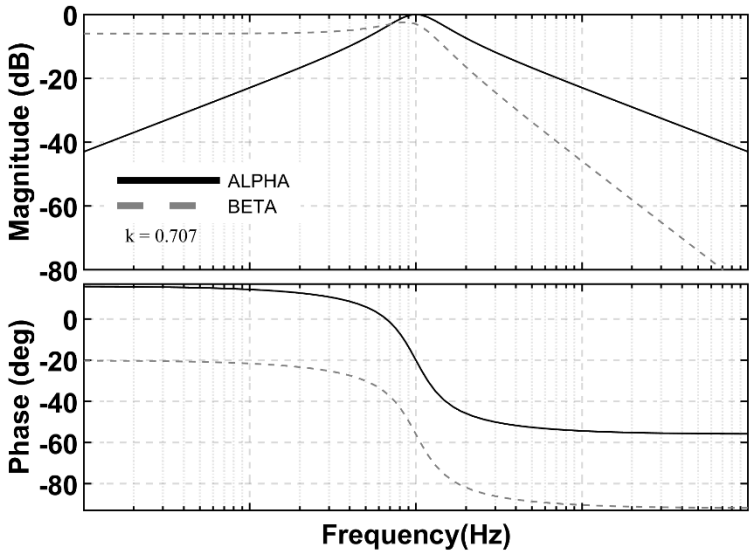


Fig. 5.2 Frequency response of v' and qv' of DFSOGI – PLL

5.3.1. Stability Analysis

The linear model of the DFSOGI – PLL as shown in Fig. 5.3, is derived based on the following consideration; for a small phase difference $(\varphi - \hat{\varphi}), \sin(\varphi - \hat{\varphi}) = (\varphi - \hat{\varphi})$ and $\cos(\varphi - \hat{\varphi}) = 1$ and the frequency $\omega = \omega_n$. $D'(s)$ corresponds to the disturbance in the grid. Taking into account the above assumptions the step response for (7) is given by (8)

$$v_q(s) = \frac{Vk\omega}{2+k\omega}(\varphi - \hat{\varphi}) \tag{8}$$

From the linear model taking into consideration $D'(s) = 0$,the open loop transfer function of the model is given by (9) and the corresponding phase margin (PM) is given by (10).

$$G_1(s) = \frac{\varphi(s)}{\varphi_e(s)} = \frac{k_i(\tau_1 s+1)}{s^2(\tau_2 s+1)} \tag{9}$$

$$PM = \tan^{-1}(\tau_1\omega) - \tan^{-1}(\tau_2\omega) \tag{10}$$

With factor τ_1 dependent on the proportional and integral coefficient of the PI controller k_p and k_i, and factor τ_2 being the damping factor for the phase detector. In equations (9) and (10), $\tau_1 = \frac{k_p}{k_i}$ for both DFSOGI – PLL and SOGI – PLL, while $\tau_2 = \frac{1}{k\omega}$ for DFSOGI – PLL

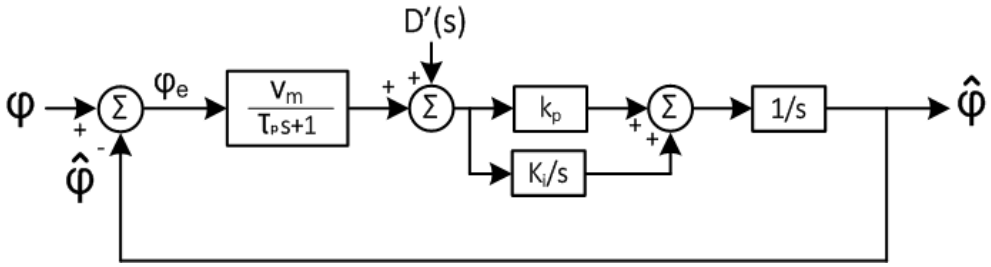


Fig. 5.3 Linear model of DFSOGI – PLL

and $\tau_2 = \frac{2}{k\omega}$ for SOGI – PLL. Phase margin for transfer function can be given as (11)

$$PM = \tan^{-1}\left(\frac{b^2-1}{2b}\right) \tag{11}$$

with $b = \sqrt{\frac{\tau_1}{\tau_2}}$. For conventional SOGI – PLL $b = \sqrt{\frac{k_p}{k_i} * \frac{k\omega}{2}}$ while for proposed DFSOGI – PLL $= \sqrt{\frac{k_p}{k_i} * k\omega}$. Based on (10) and (11) the phase margin for both SOGI – PLL and DFSOGI – PLL is as shown in Fig.3, the phase margin for DFSOGI – PLL is 0.888 radians for $b = 2\sqrt{2}$, while the phase margin for SOGI – PLL is 0.643 radians for $b = 2$. Therefore, DFSOGI – PLL algorithm with more phase margin is more stable.

5.3.2. Transient Response

The open loop transfer function given by (6) can be rewritten as (10)

$$G_1(s) = \frac{\varphi(s)}{\varphi_e(s)} = \frac{k_i\left(\frac{sb}{\omega_c}+1\right)}{s^2\left(\frac{s}{b\omega_c}+1\right)} \tag{9}$$

$$G_1(s) = \frac{\varphi(s)}{\varphi_e(s)} = \frac{sb\omega_c^2+\omega_c^3}{s^2(s+b\omega_c)} \tag{10}$$

The closed loop transfer response for $G_1$is given by (11)

$$G_2(s) = \frac{1}{1+G_1(s)} \tag{11}$$

G_2 can be rewritten as (12) and (13) in the form of second order equation.

$$G_2(s) = \frac{s^2(s+b\omega_c)}{(s+\omega_c)(s^2+(b-1)\omega_c s+\omega_c^2)} \quad (12)$$

$$G_2(s) = \frac{s^2(s+(2\varepsilon+1)\omega_n)}{(s+\omega_n)(s^2+2\varepsilon\omega_n s+\omega_n^2)} \quad (13)$$

Where $\omega_n = \omega_c$ and $\varepsilon = \frac{(b-1)}{2}$.

Based on (13), the normalized settling time for the proposed converter and SOGI – PLL is shown in Fig. 5.4. Damping factor ε is proportional to the factor b, which in itself is dependent on the nominal frequency ω_n. The settling time for the proposed converter as seen from Fig. 5.4 is significantly less compared to SOGI – PLL.

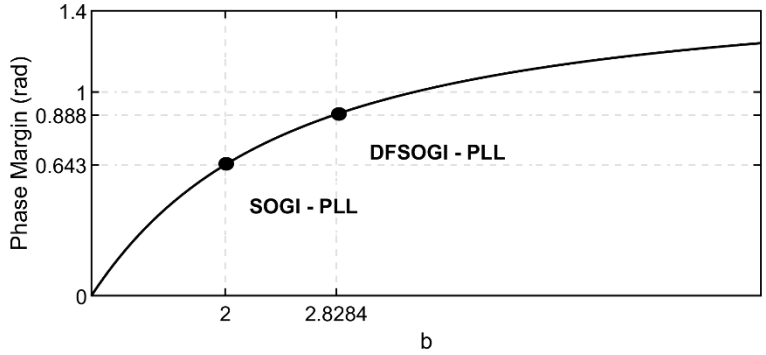


Fig. 5.4 Phase margin vs b for DFSOGI – PLL and SOGI – PLL

Based on (3) and (4), the bode plot and step response of DFSOGI – PLL and SOGI – PLL are shown in Fig.5.5 and Fig. 5.6 respectively. As seen from the bode plot in Fig. 5.5, the crossover frequency for DFSOGI – PLL is 628.318 Hz while for SOGI – PLL is 314.159 Hz. The step response as shown in Fig. 5.7 supports the superior transient performance of DFSOGI – PLL. A comparative based upon the dynamic performance of DFSOGI – PLL and SOGI – PLL is drawn in Table I for a step response.

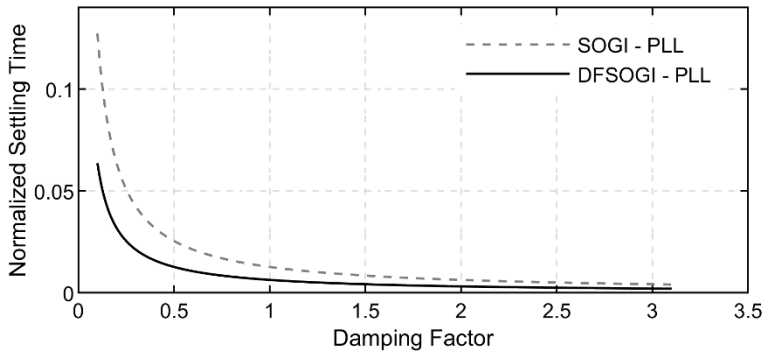


Fig. 5.5 Normalized settling time of DFSOGI – PLL and SOGI - PLL

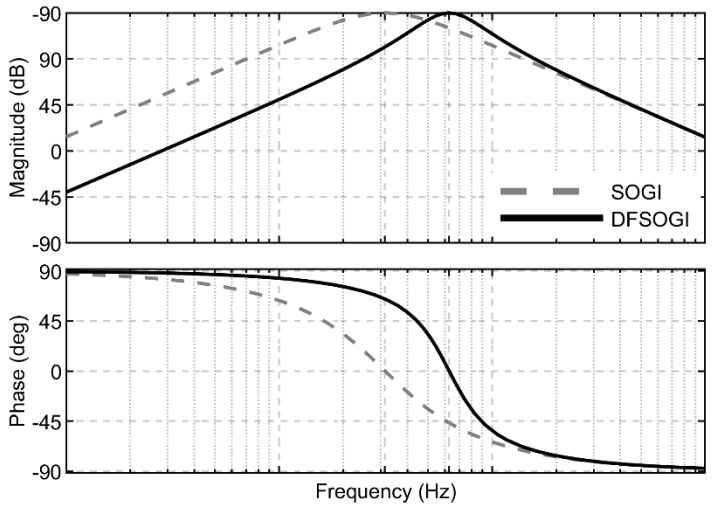


Fig. 5.6 Bode Plot of DFSOGI – PLL and SOGI - PLL

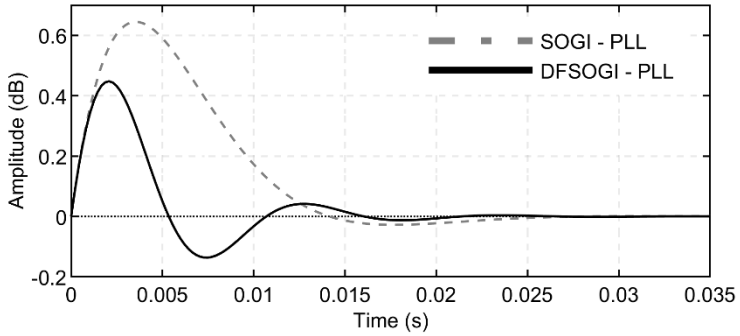


Fig. 5.7 Bode Plot of DFSOGI – PLL and SOGI – PLL

TABLE I TRANSIENT RESPONSE FOR STEP INPUT

Parameter	DFSOGI – PLL	SOGI – PLL
Phase Margin	0.888 rad	0.643 rad
Peak to Peak Variation	0.4476 dB	0.6448 dB
Maximum Overshoot	0.4476 dB	0.6448 dB
Minimum Undershoot	0.1364 dB	0.0279 dB
Settling Time	0.0195 sec	0.0225 sec
Peak Time	0.0021 sec	0.0035 sec
Crossover Frequency	628.3 Hz	314.1 Hz

5.4. Experimental Analysis of Proposed Synchronization Algorithm

5.4.1. Grid Perturbation – Step Frequency change of 5 Hz

The voltage at point of common coupling (PCC) is taken at a nominal voltage of 100 (pk-pk), 50Hz, 0^0 as shown in Fig. 5.8.1 with the quadrature signal v_α and v_β generated at 100Hz with peak amplitude of 100 Hz and reference sine signal at 50Hz. Fig 5.8.2, shows the reference sine and cosine signals for the proposed algorithm at 100Hz and the phase response. The direct and quadrature voltages v_d and v_q along with the frequency response is shown in Fig.5.8.3. Initially voltages v_d and v_q settle at 100V and 0V, with the frequency settling at 50Hz. At t=0.5s, the grid frequency steps down to 45Hz, the frequency settles to 45Hz in 129ms with an undershoot of 1.35Hz as shown in Fig. 5.9 and Fig. 5.10. The direct axis voltage v_d restores to 100Vwith v_q settling at 0V reducing the phase shift to 0 as seen in the phase response. The sine and cosine reference generated for parks transformation at both 50Hz and 100Hz is shown in Fig 5.8.1 and Fig.5.8.2. At t = 1.5s, the grid frequency restores to 50Hz in a step response, with the frequency experiencing an overshoot of 1.35Hz and the voltages v_d and v_q restoring to 100V and 0V.

5.4.2. Grid Perturbation – Step Phase change of $+30^0$

Fig.11 shows the dynamic response of DFSOGI – PLL for a step change of $+30^0$ in grid phase. At t=0.5s, the grid phase shifts from 0^0 to $+30^0$, with the frequency experiencing a peak – to – peak variation of 5.1Hz, 4.7 Hz overshoot and 0.4Hz undershoot. Voltages v_d and v_q settle at 100V and 0V respectively in 125msec representing the algorithm locking phase to grid phase of $+30^0$. Clean reference sine and cosine signals at 50Hz and 100Hz are generated as depicted in Fig 5.11.1. At t=1.5s, the grid phase restores back to 0^0 with voltages v_d and v_q restoring to 100V and 0V respectively.

5.4.3. Grid Perturbation – Step Voltage Sag of 80%

The dynamic response of DFSOGI – PLL algorithm for voltage sag of 80% is shown in Fig. 5.14 with same initial conditions as above. At t=0.5s, the PCC voltage dips from 100V

to 20V, direct and quadrature voltages v_d and v_q respectively settle at 20V and 0V respectively in 30ms as shown in Fig. 5.15 and Fig. 5.16. The frequency experiences a peak – to – peak variation of 2.2Hz. The phase response along with sine and cosine reference signals is also shown in Fig.14.1. at t=1.5s, the grid voltage restores to 100V, with v_d and v_q restoring to 100V and 0V respectively. The frequency response experiences a peak – to – peak variation of 2.2Hz.

5.4.4. Response for Pulsed Voltage Signal

The response of DFSOGI – PLL is further validated for pulsed voltage representing a worst case scenario with maximum distorted voltage at PCC is shown in Fig.17. The synchronization algorithm generates sine and cosine signals at 100Hz and 50Hz. The phase locked loop algorithm tracks the fundamental frequency of 50Hz as shown in Fig.17.1 and the same is validated through the FFT plot shown. Direct and quadrature voltages v_d and v_q respectively settle at 77.2V and 0V.

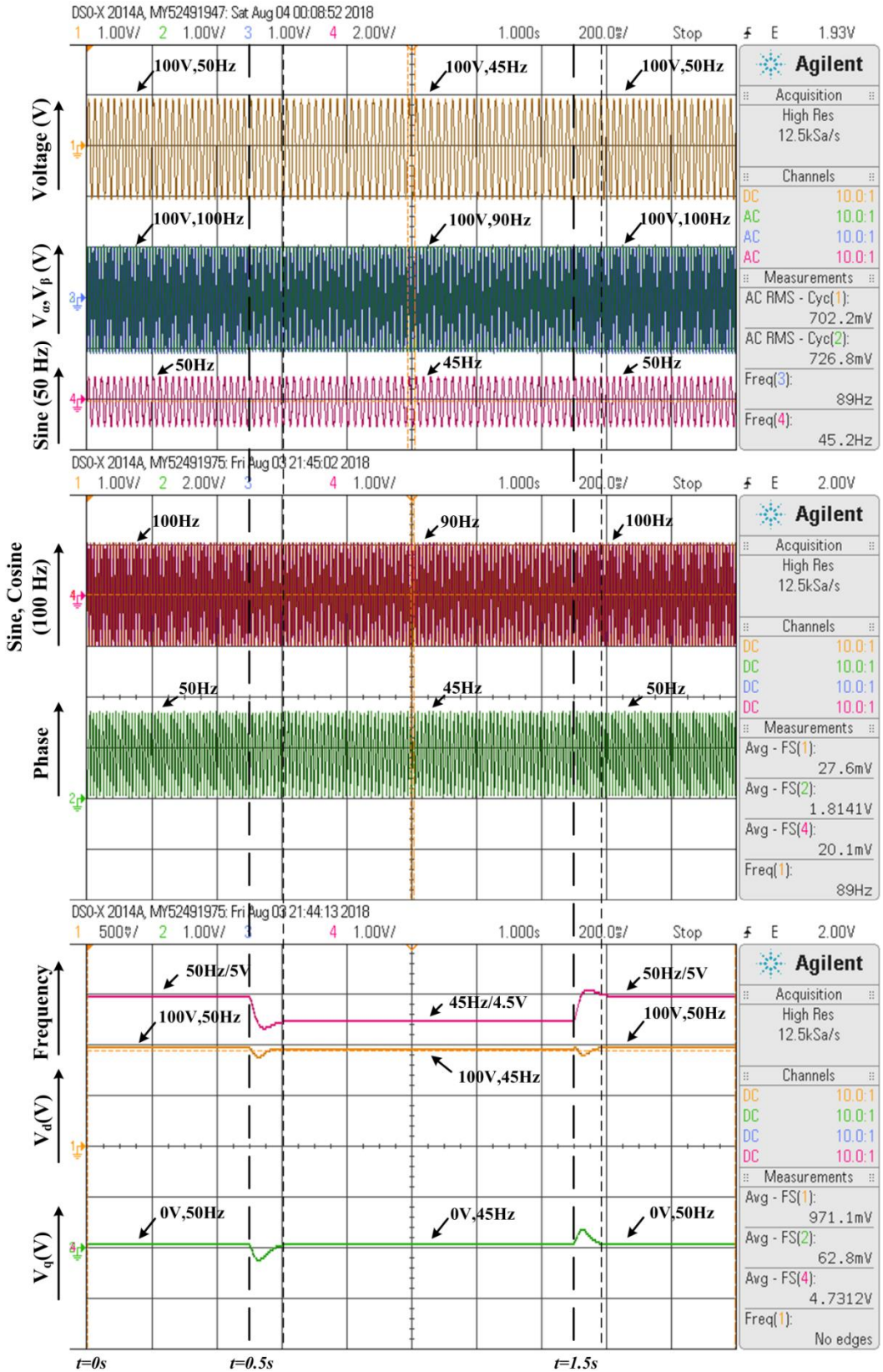


Fig. 5.8 Response – Frequency change a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

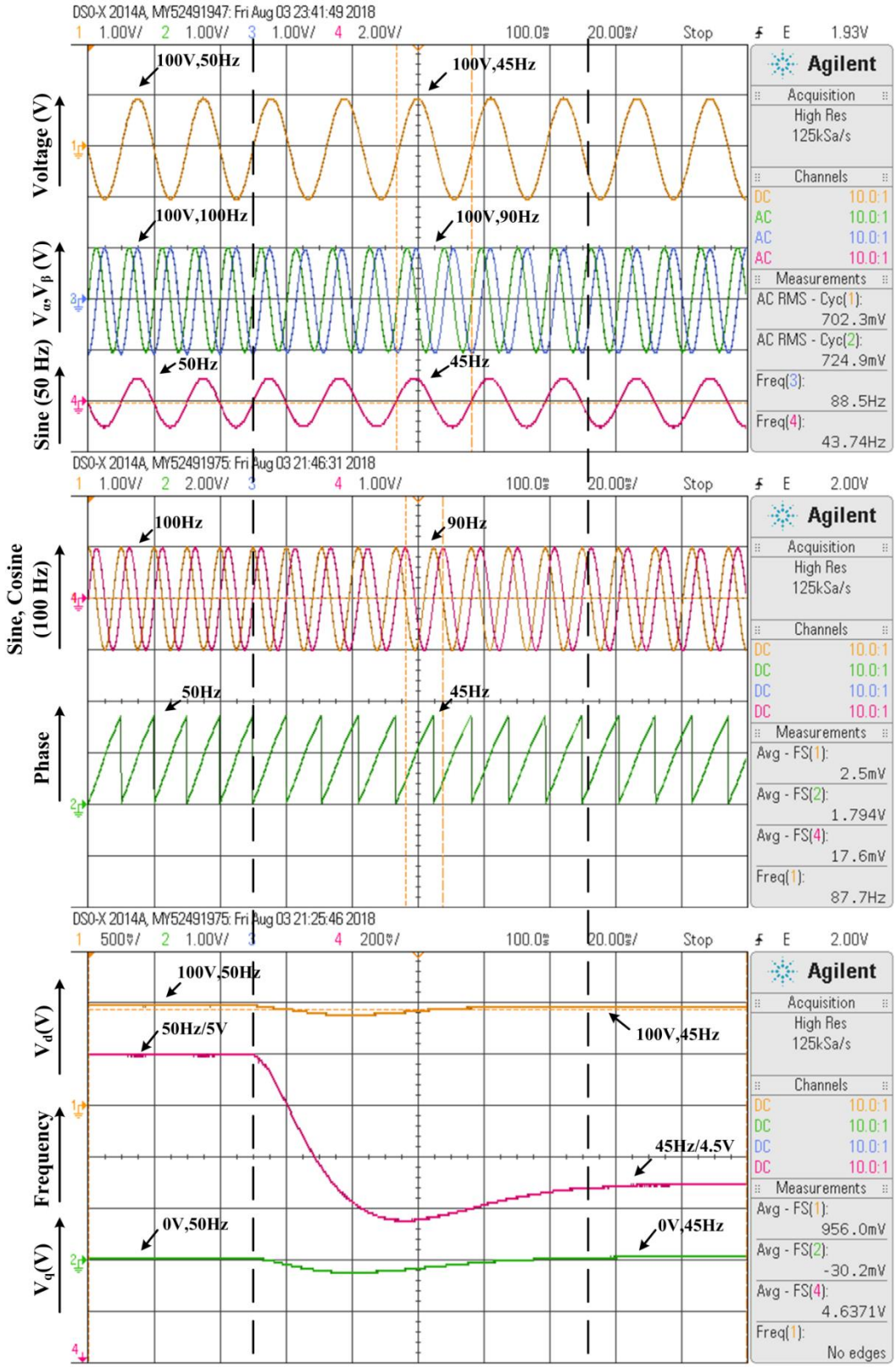


Fig. 5.9 Zoomed (t = 0.5s) - Response – Frequency change a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

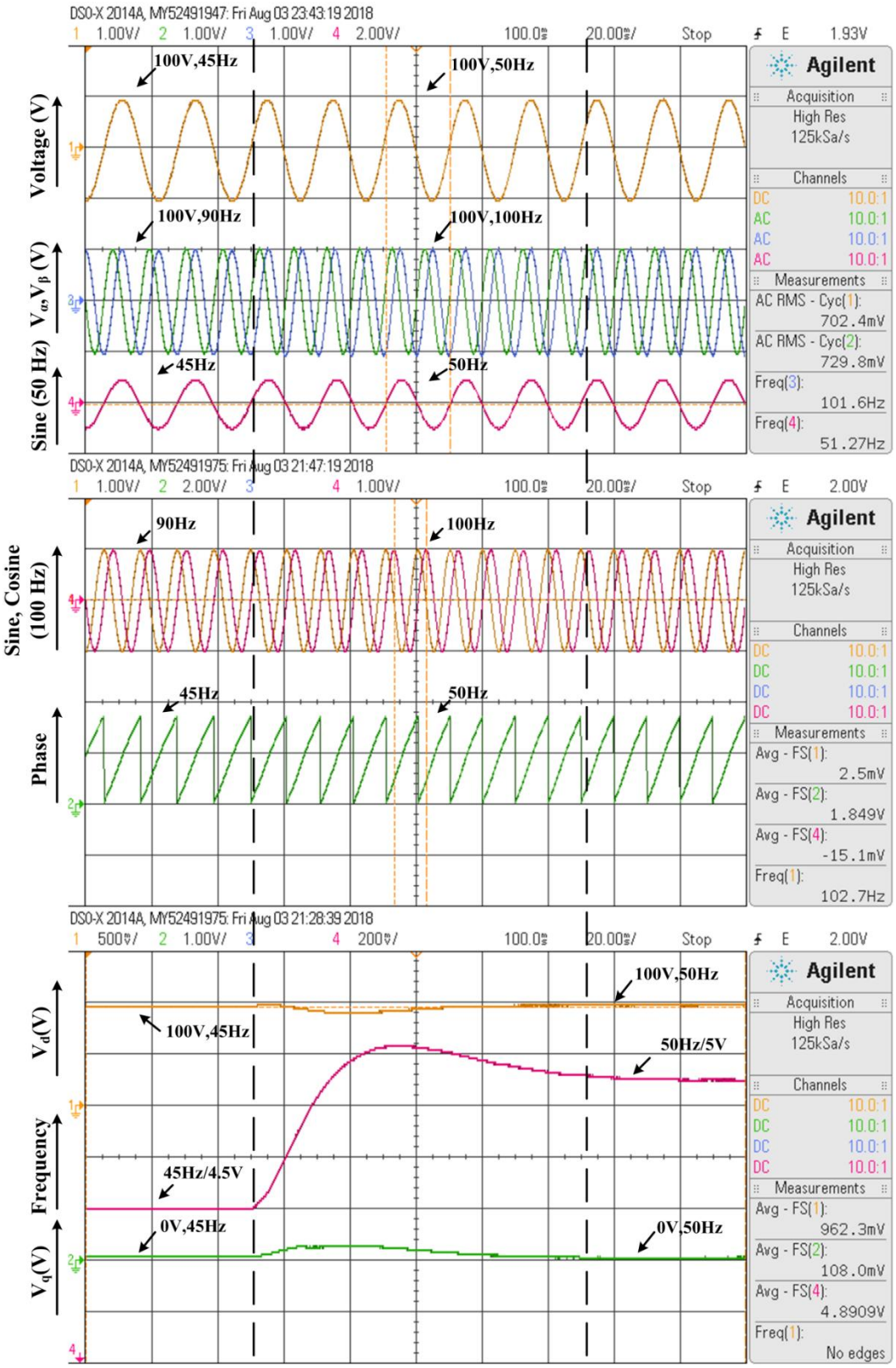


Fig. 5.10 Zoomed (t = 1.5s) - Response – Frequency change a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

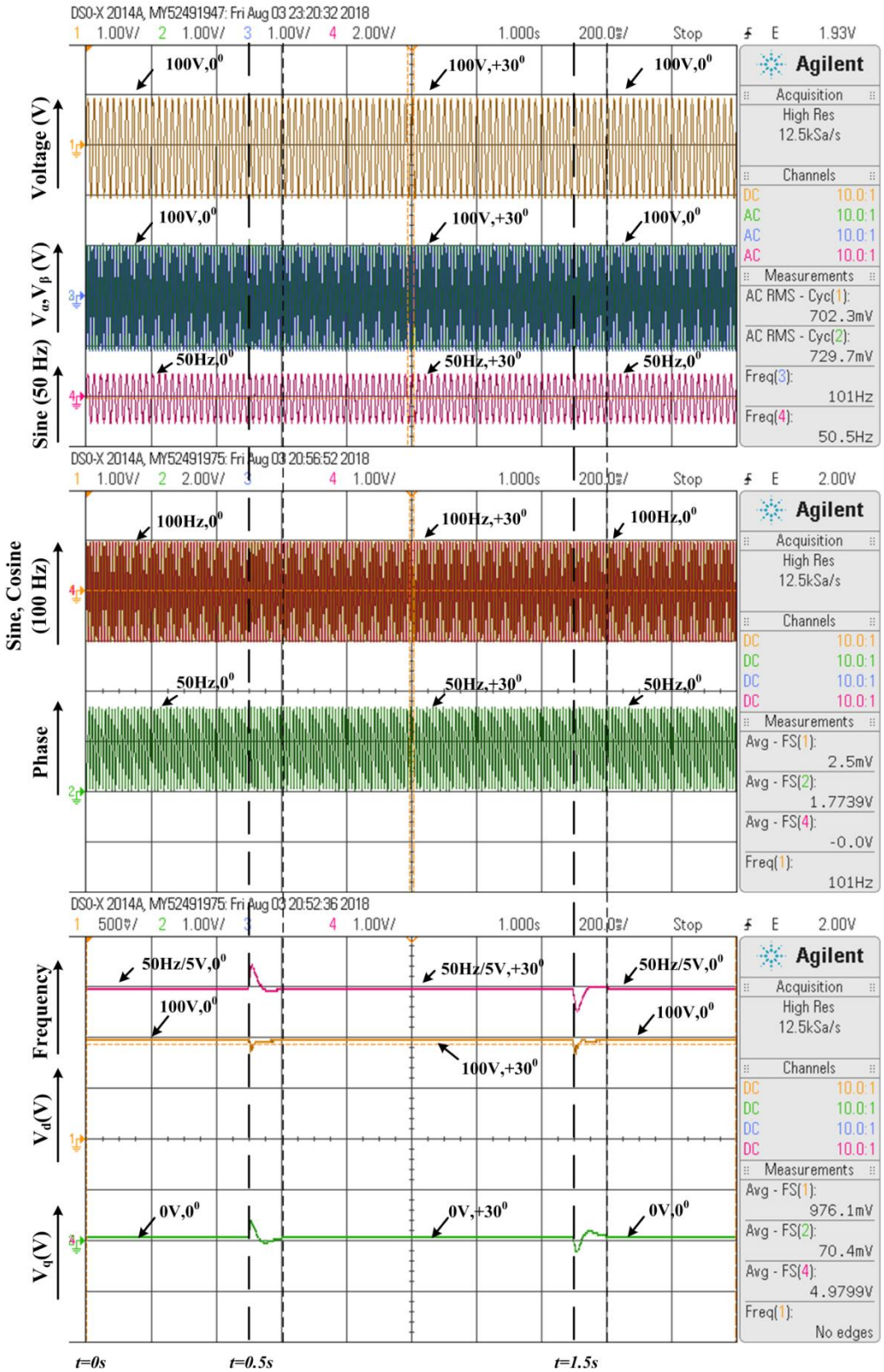


Fig. 5.11 Response – Phase Change a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

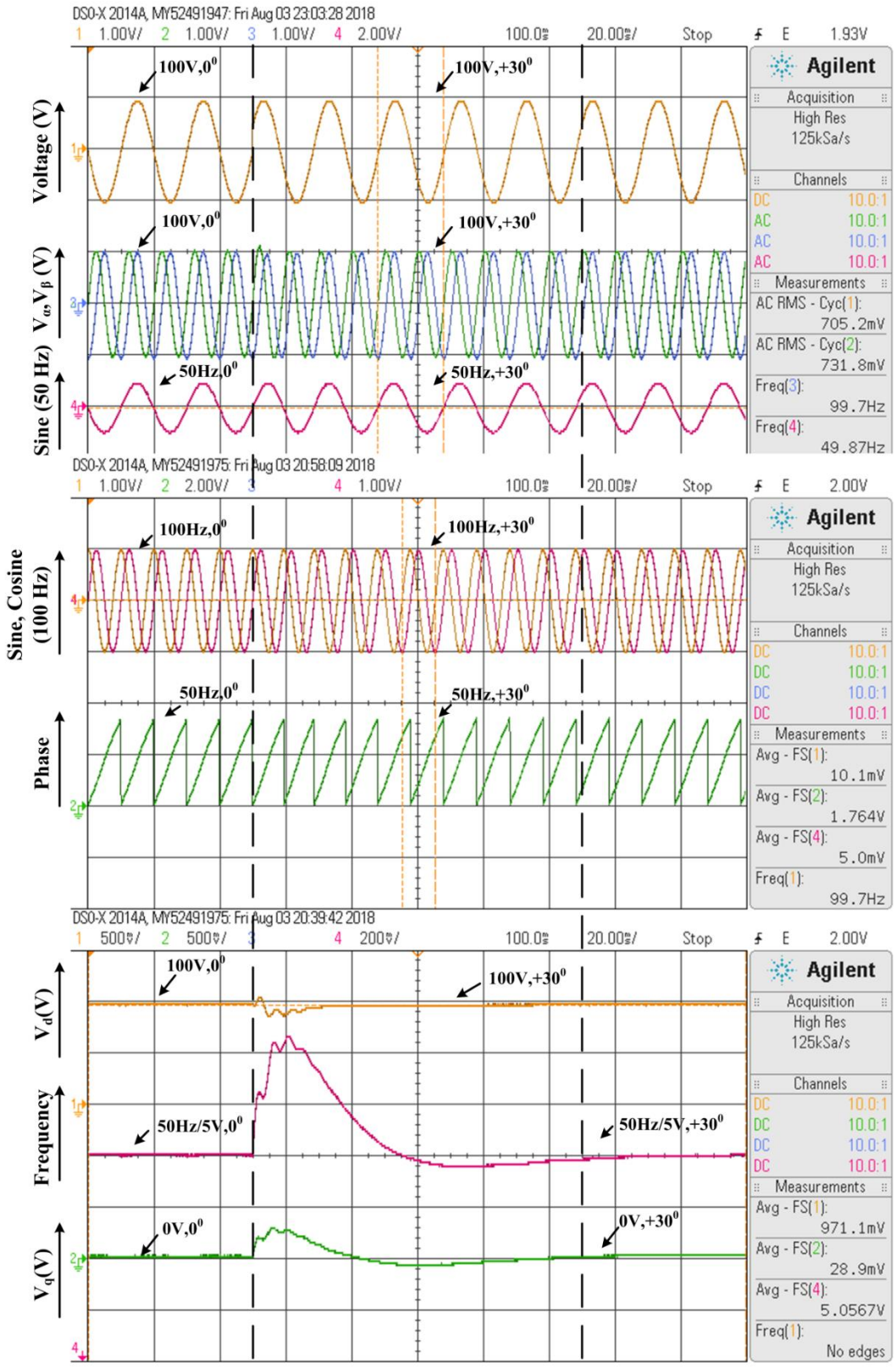


Fig. 5.12 Zoomed (t = 0.5s) – Response – Phase Change a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

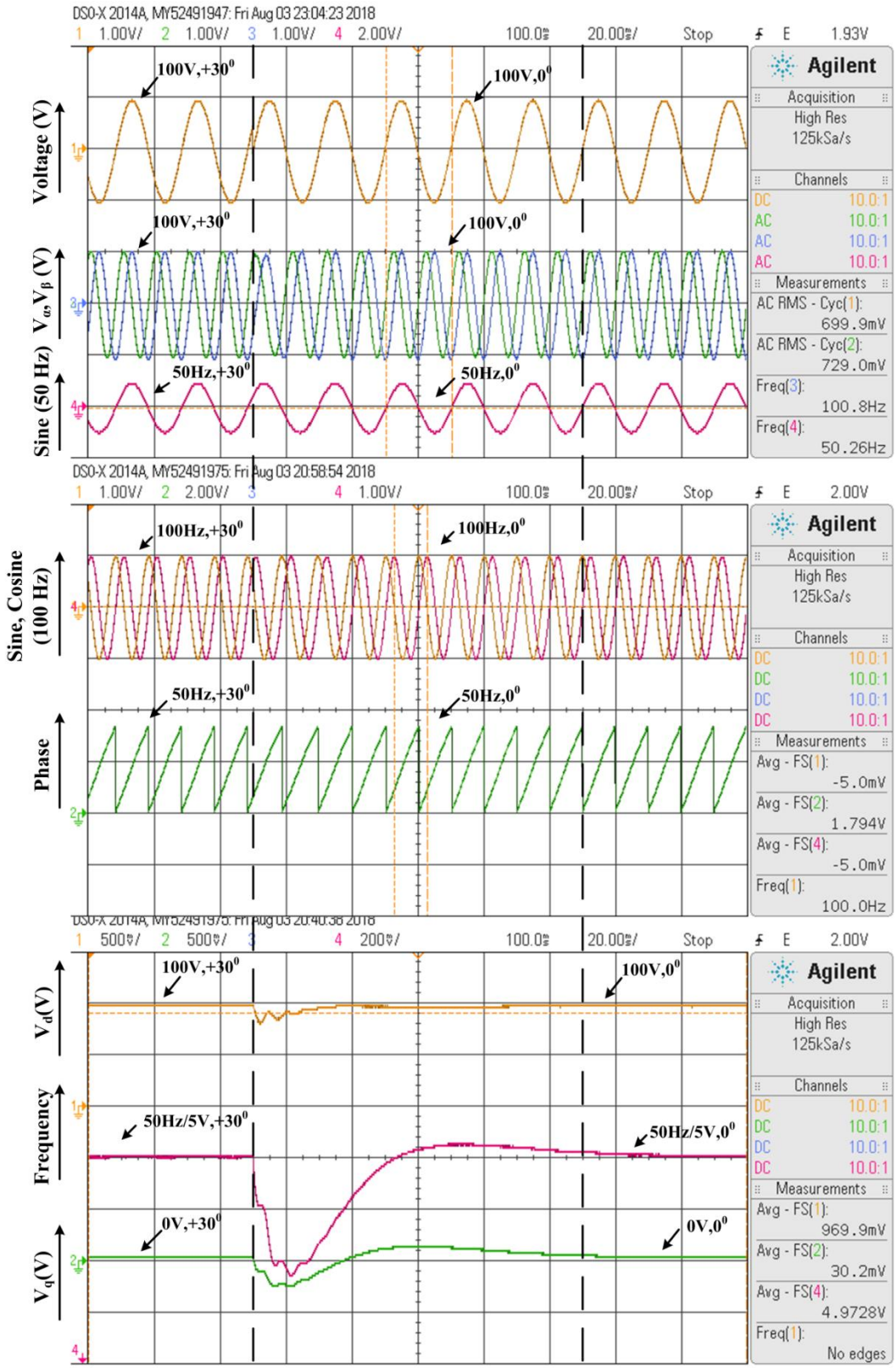


Fig. 5.13 Zoomed (t = 1.5s) – Response – Phase Change a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

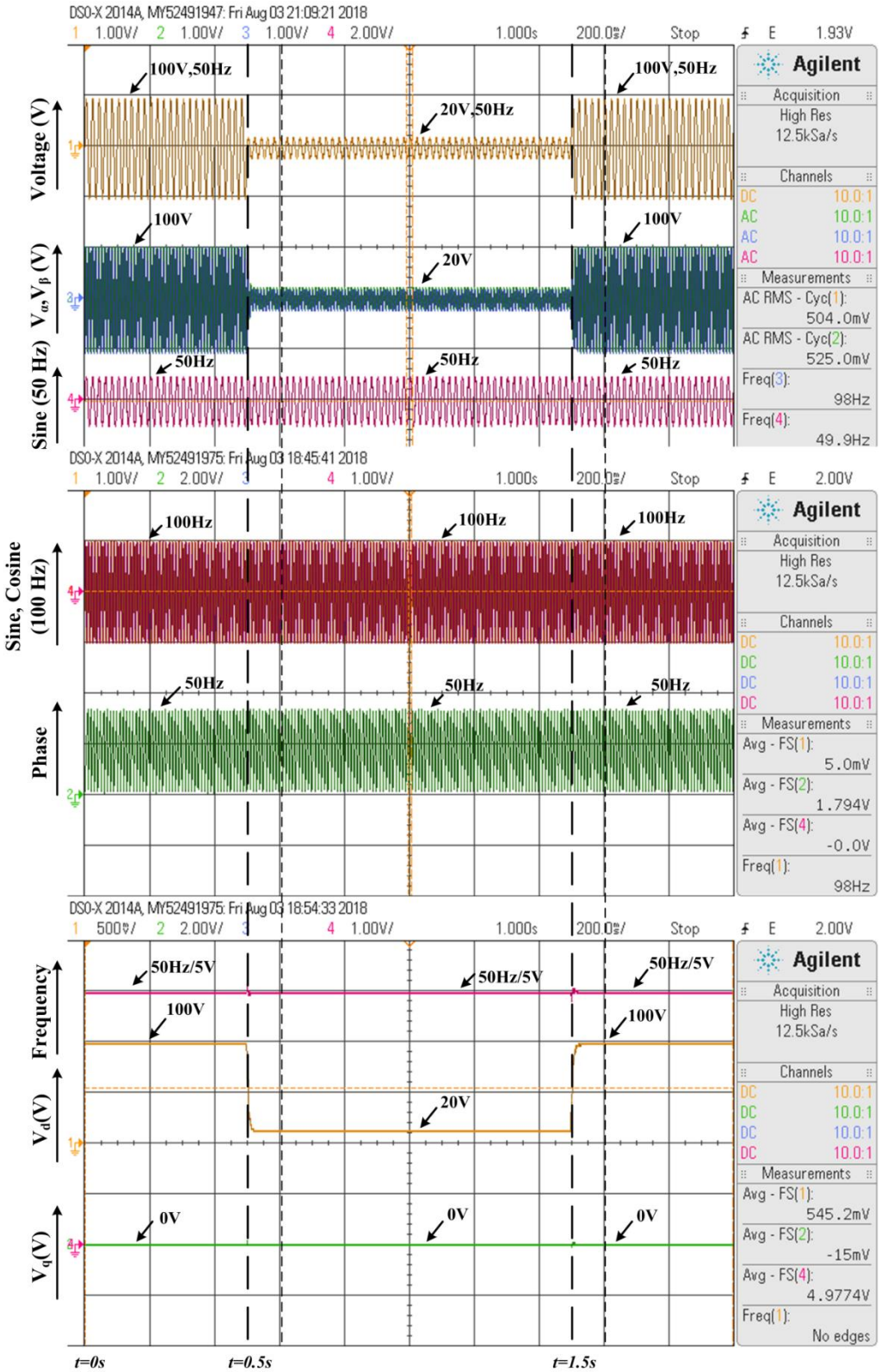


Fig. 5.14 Response – Voltage sag a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

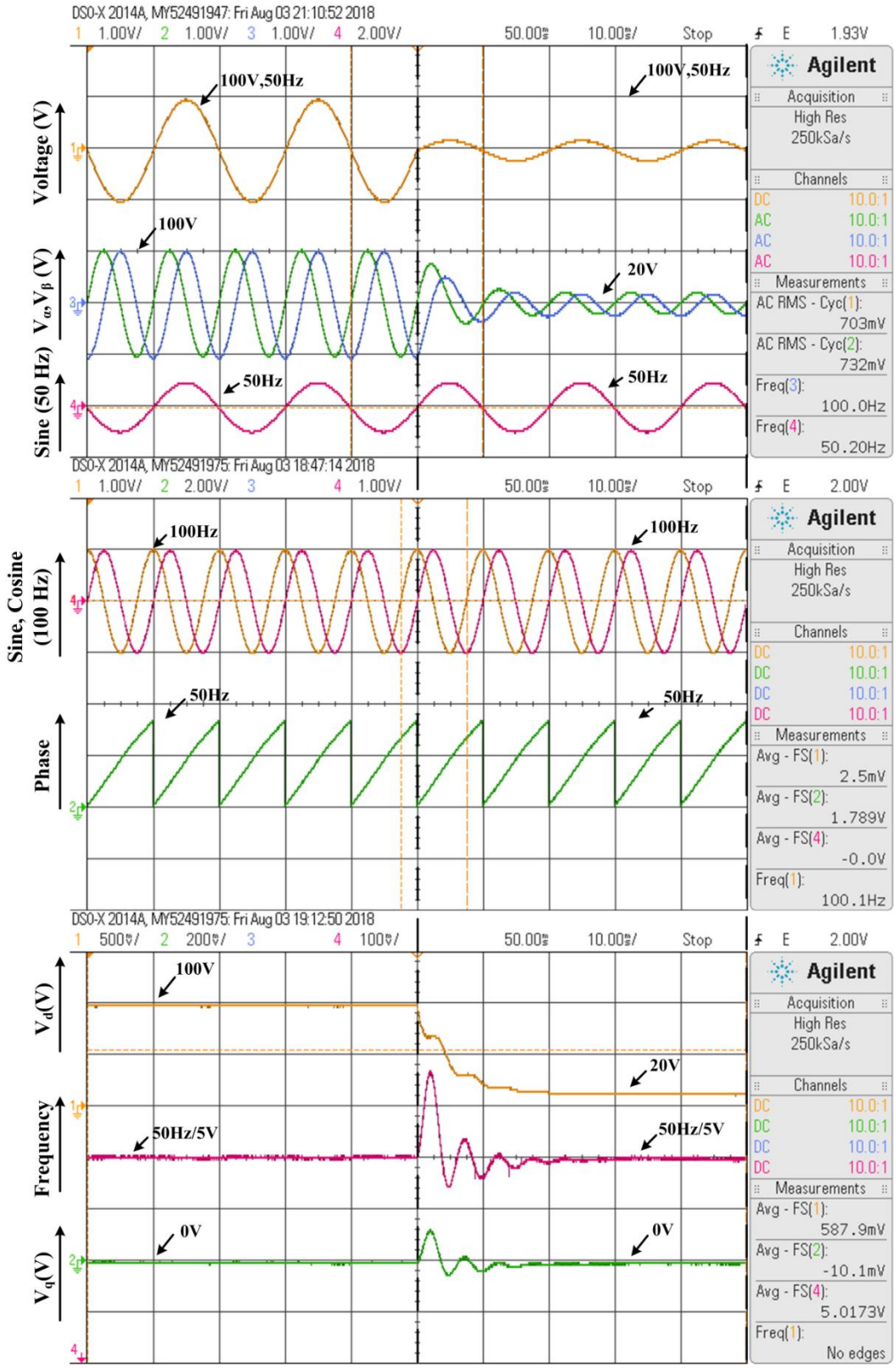


Fig. 5.15 Zoomed (t= 0.5s) – Response – Voltage sag a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

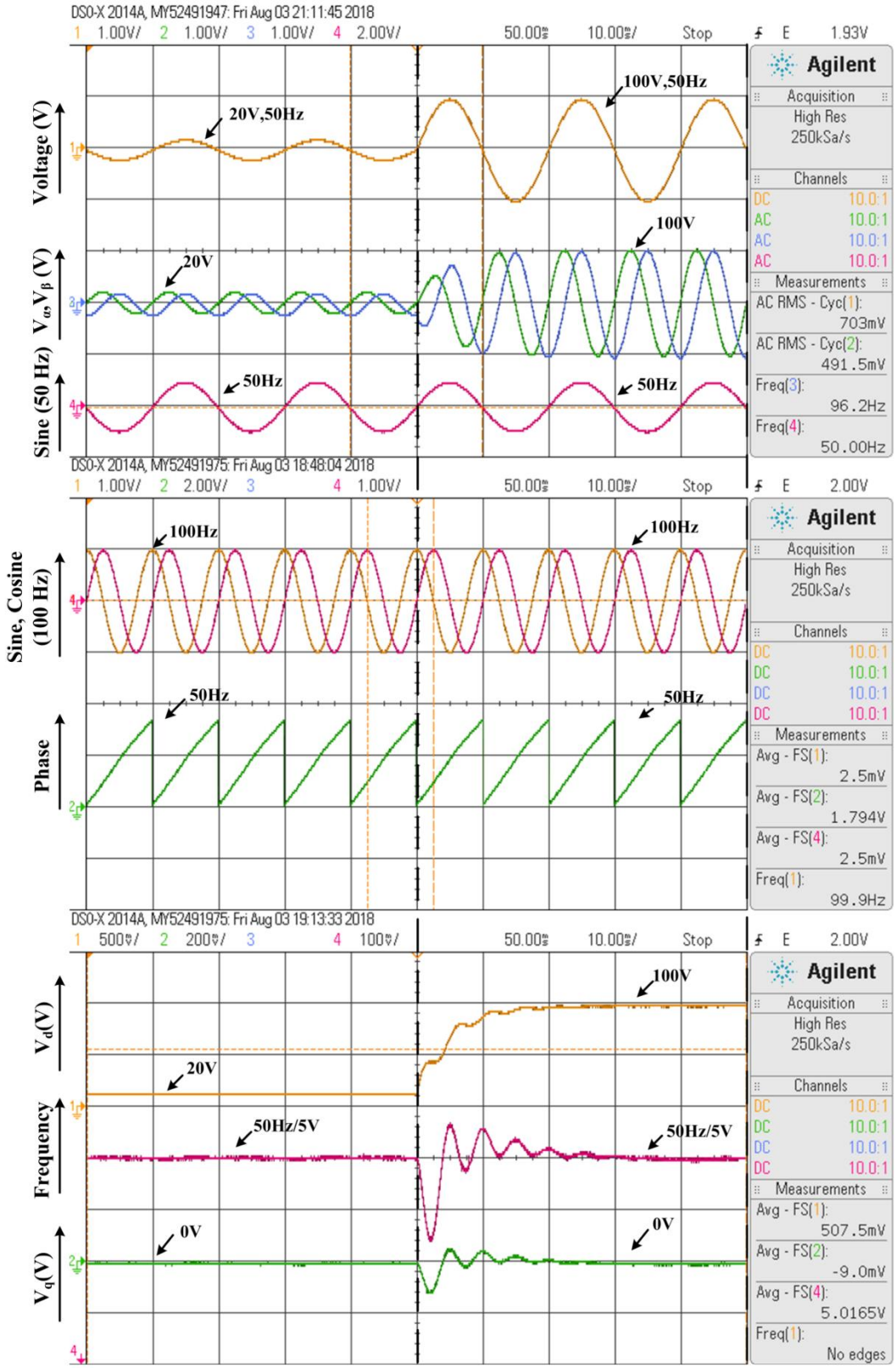


Fig. 5.16 Zoomed (t= 1.5s) – Response – Voltage sag a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

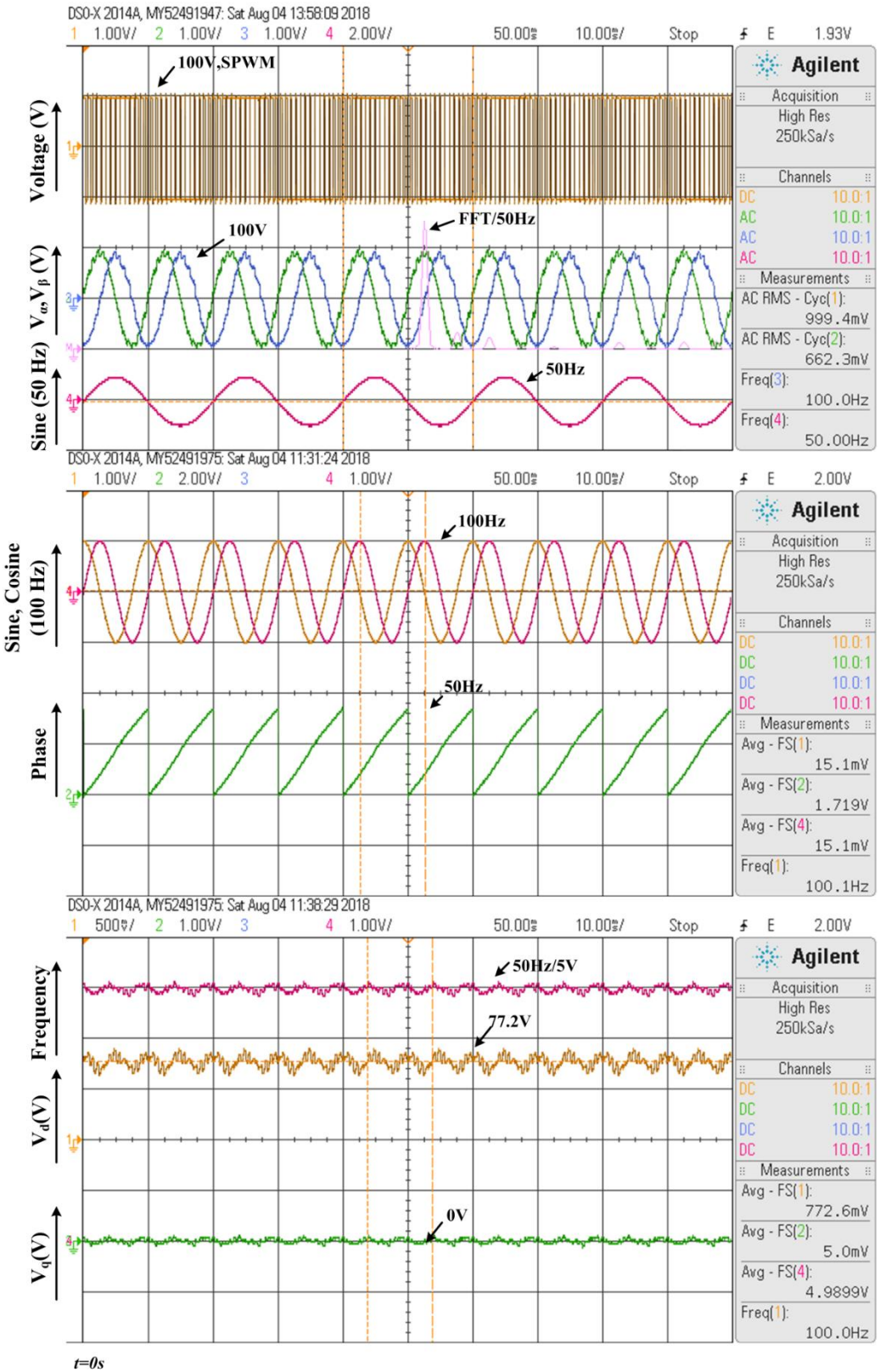


Fig. 5.17 Response – Pulsed input voltage a) i) input voltage (V_{IN}) ii) v_α and v_β iii) sine reference (50 Hz) b) i) sine and cosine reference (100Hz) ii) phase c) i) frequency iv) v_d v) v_q

5.5. Performance Analysis

The dynamic performance of proposed DFSOGI – PLL is compared with conventional SOGI – PLL for the above discussed grid disturbances as shown from Fig.5.18. to Fig. 5.20. A comparative for a peak – to – peak variation in frequency for the above discussed perturbations is drawn between DFSOGI – PLL and SOGI – PLL as depicted by Table II.

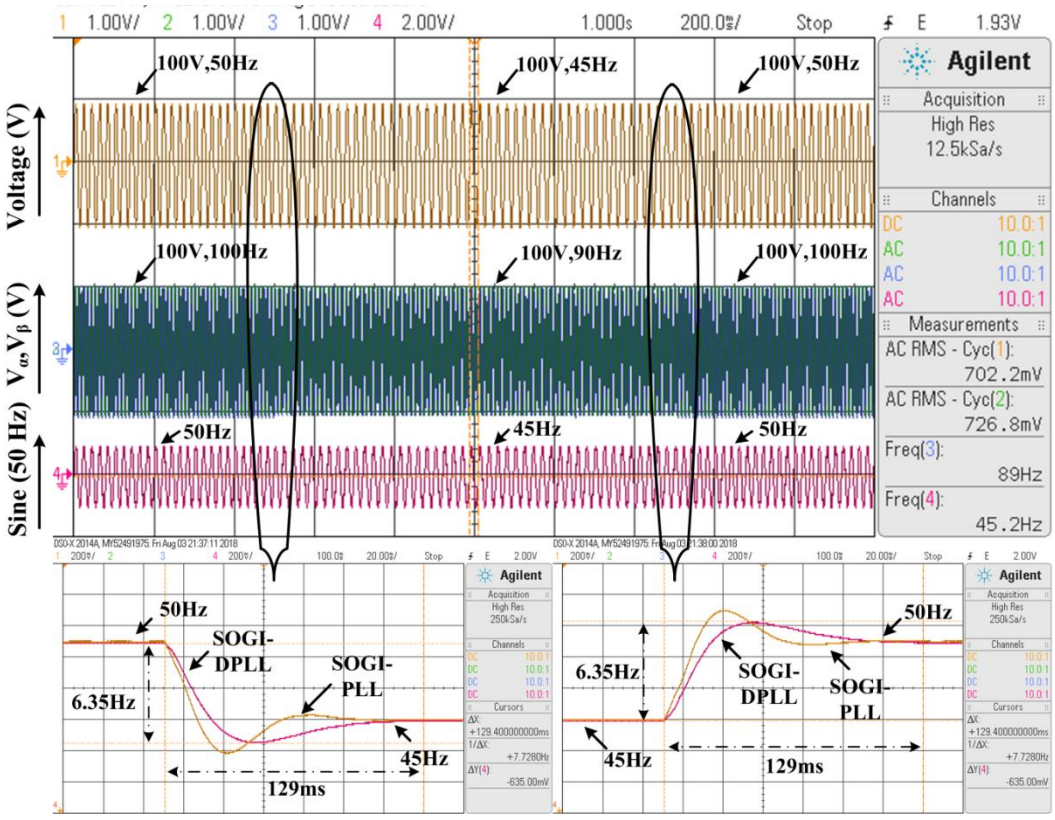


Fig. 5.18 Comparison of DFGOSI – PLL and SOGI – PLL for step frequency change of 5Hz

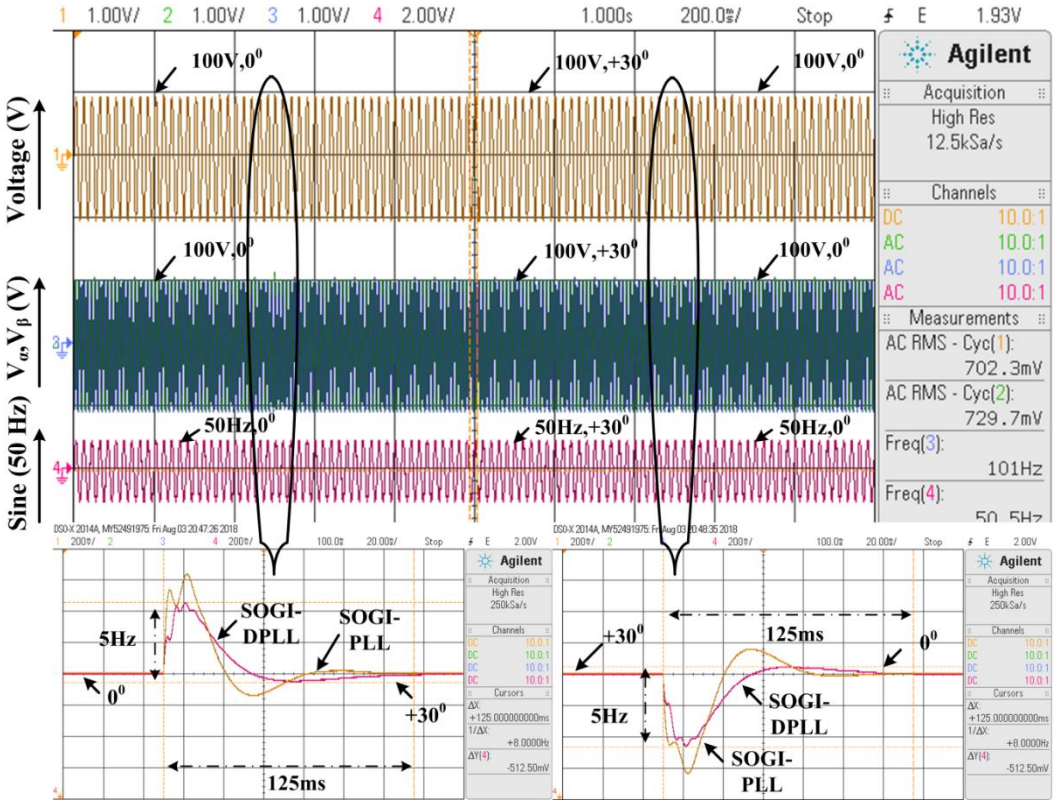


Fig. 5.19 Comparison of DFGOSI – PLL and SOGI – PLL for step phase change of 30^0

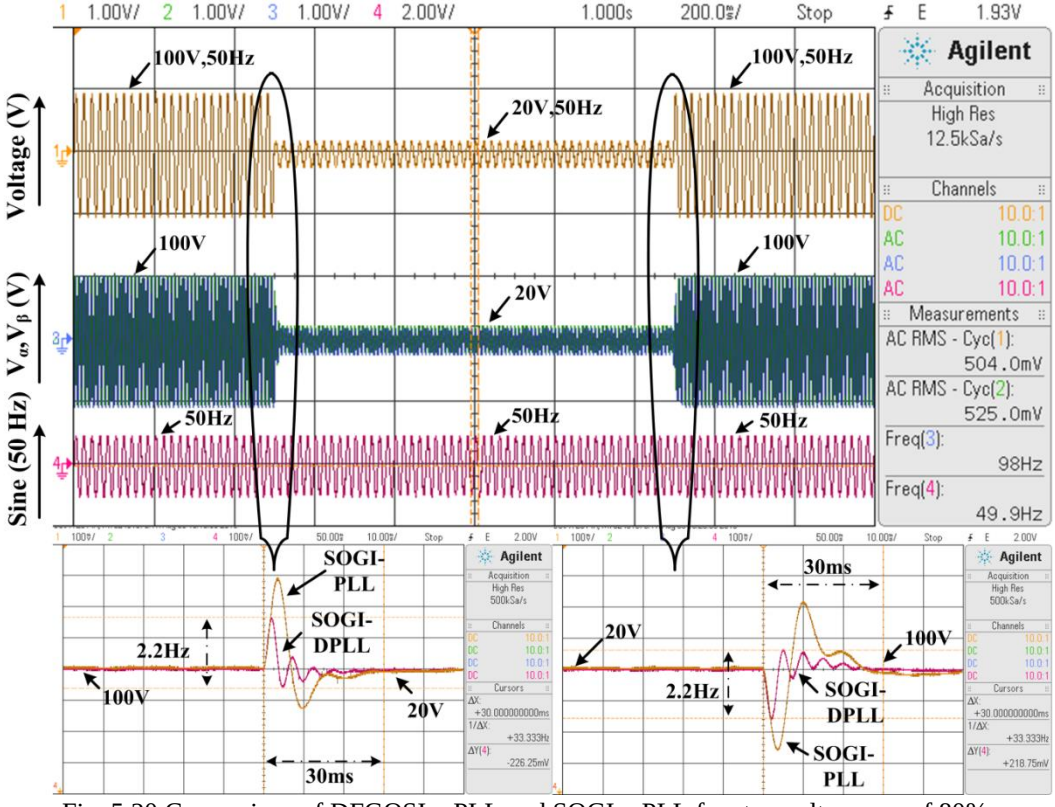


Fig. 5.20 Comparison of DFGOSI – PLL and SOGI – PLL for step voltage sag of 80%

TABLE II RESPONSE OF DFSOGI – PLL AND SOGI – PLL

Parameters		SOGI – PLL			DFSOGI - PLL		
		Overshoot	**Undershoot**	**Pk – pk**	**Overshoot**	**Undershoot**	**Pk – pk**
Frequency Jump of 5Hz	45Hz to 50Hz	0.4Hz	2Hz	2.4Hz	0Hz	1.35Hz	1.35Hz
	45Hz to 50Hz	2Hz	0.4Hz	2.4Hz	1.35Hz	0Hz	1.35Hz
Phase Jump of $+30^0$	0^0 to $+30^0$	6.3Hz	1.2Hz	7.5Hz	4.7Hz	0.4Hz	5.1Hz
	$+30^0$ to 0^0	1.2Hz	6.3Hz	7.5Hz	0.4Hz	4.7Hz	5.1Hz
Voltage Dip of 80%	100V to 20V	2.9Hz	1.2Hz	4.1Hz	1.6Hz	0.6Hz	2.2Hz
	20V to 100V	1.2Hz	2.9Hz	4.1Hz	0.6Hz	1.6Hz	2.2Hz

5.6. Conclusion

The hardware results affirm the superior tracking and transient performance of the proposed Double Frequency Second Order Generalized Integrator Phase Locked Loop (DFSOGI – PLL). The proposed synchronization algorithm limits the transient overshoots and undershoots during major grid disturbances hence increasing the performance and robustness of the control algorithm for the grid interfaced inverter.

Chapter VI

ADAPTIVE DROOP BASED RESYNCHRONIZATION ALGORITHM MITIGATING TRANSIENTS AND CIRCULATING CURRENT FOR GRID CONNECTED INVERTER

6.1. Problem formulation

A microgrid with multiple inverters faces a number of bottlenecks when it comes to mode transition from grid forming to grid connected mode and vice versa. The level of uncertainty varies with the number of generators at the instance of grid outage and grid return and can lead to a mismatch in the power generation vis a vis power demanded. In case the grid goes out with 'n' inverters in generating mode and returns with 'n+i' connected inverters meeting the load demand, then the incoming inverter is not required to operate at its maximum capacity. Moreover, while resynchronizing with the grid at PCC, it is mandatory that the incoming inverter has to have a slight leading phase angle if inserted in voltage mode, such that it can feed the necessary power to the grid and avoid becoming a load to the grid. In addition to grid synchronization problems, the problem of transient currents during mode transition is also a major concern. In grid forming mode, where the inverter is tasked to maintain the grid voltage at the nominal frequency, inter converter circulating current is another deterrent. Inverters operating at different dynamics like phase/frequency and having different physical parameters can cause interaction of inverters in the microgrid. This unwanted power is greater than maximum capacity of the inverter and can damage the inverter, while the inverter acting as a load.

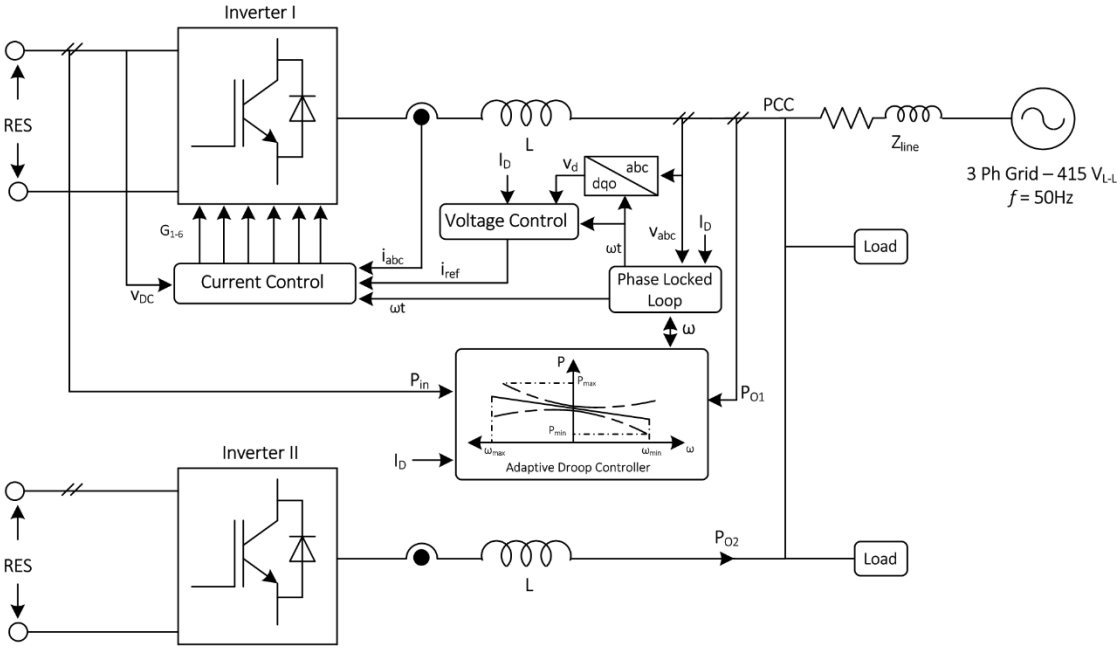
Significant literature has been reported for seamless transition from one mode to other, based on islanding detection algorithms and algorithms meant for control of power voltage and frequency. In [72] authors use both current and voltage modes of operation throughout, i.e., grid connected and islanded mode respectively. The proposed method negotiates the need of mode transfer but significantly increases computational requirement and the complexity of the control algorithm. A control algorithm is

presented for transitioning from grid connected to islanded mode and vice versa through estimation of grid angle [73]. The involved control strategy limits the current transient at the cost of increased calculations. The algorithm is based on changes in scalar quantities during mode transition while neglecting the affect of phase angle [74]. A droop power based seamless transition algorithm is proposed in [75-76], wherein both the voltage and the frequency vary, resulting in oscillatory response and significant voltage distortion. A PLL based seamless transfer control is also proposed riding on the positive and negative sequence estimation [77]. The method significantly reduces the computation in comparison to the previously proposed methods but experience slow transient dynamics. Under stringent grid norms across variety of grid codes it is of importance that the system response should be as instantaneous as possible. Thereby, it is essential that synchronization algorithm has to have fast dynamics to restrict the overshoot and attain steady state quickly.

Popular synchronization techniques like unit template and Synchronous Reference Frame Phase Locked Loop (SRF-PLL) perform seamlessly under balanced conditions however, under unbalanced distorted voltage conditions or while transitioning from one operating mode to the other, these algorithms exhibit slow dynamics making the system unacceptable for complying with the stringent grid codes. Amplitude normalization scheme reported in [66-67] enhances the dynamic response of the SRF-PLL at the cost of increased computation and complexity. On the other hand, enhanced phased locked loop (EPLL) reported in [67] exhibits better transient response owing to its adaptive frequency notch filtering at the cost of large computational load. Phase locked loops and frequency locked loops with second order adaptive filter (SOGI) reported in [68-69] offer improved dynamic response taking advantage of adaptive filter based on band pass filter resonating at nominal frequency for optimum filtering of the input signal. Moreover, the ability of the SOGI adaptive filter to generate Quadrature signal generators (QSG) like Hilbert transformer, transport delay and inverse park transformation puts it aside others. The improved dynamics of SOGI-PLL in addition to low computational requirement make it the fit algorithm for the synchronization/resynchronization requirement.

6.2. Proposed Adaptive Droop Control Re – Synchronization Algorithm for Grid Connected Inverter

A grid connected inverter operating in compliance with the grid norms requires operating under grid connected mode and islanded mode should seamlessly transit between the two modes. When operating in grid connected mode the inverter operates in current control mode with the grid as the master, while in islanded mode, the inverter operates in voltage mode, maintaining the voltage and frequency at PCC for connected loads. Depending upon the islanding signal, inverter control transits from either grid connected mode to islanded mode or vice versa resulting in transitional current and voltage spikes along with circulating currents among the inverters due to parametric mismatch in islanded mode. With the control for seamless transfer embedded in the main inverter control, the complexity and computational requirements of the system increases. A synchronization algorithm with embedded control for seamless mode transfer provides an independent solution to negotiate the transient spikes and circulating current during mode transfer increases the system reliability with reduced computational burden. Proposed adaptive power frequency droop based seamless control algorithm embedded in the synchronization algorithm is shown in Fig. 6.1. The proposed adaptive droop curves limit the current and voltage transitional spikes based upon an adaptive



control band besides administering fast dynamics with

Fig. 6.1 System Configuration

prominent signal filtering capability invoked by the SOGI adaptive filter thereby, limits the inverter operation below its maximum capacity at all instances. The reference frequency in conjunction with the power is sensed at the inverter output terminal,

restricting any inflow of circulating current. The algorithm retains the last phase value when transitioning from grid connected mode to grid forming mode, enhancing the dynamics of the transient response. On resynchronization with the utility grid, frequency and phase deviations experienced are regulated through the compensator in the phased locked loop.

6.2.1. Control Algorithm

The control algorithm based on adaptive droop embedded in the synchronization algorithm is shown in Fig. 3. The controller dynamics can be categorized under two transitions i) grid connected mode to islanded mode with the islanding detection signal (ID) changing from 0 to 1 ii) islanded mode to grid connected mode with the islanding detection signal (ID) changing from 1 to 0.

6.2.1.1. Grid Connected to Islanded Mode

While transitioning from grid connected to islanded mode, the inverter transits from current control mode to voltage mode with the inverter becoming the master, controlling the voltage magnitude and frequency at PCC. While transitioning to islanded mode, the inverter is prone to both the transitional spikes and flow of circulating currents among the inverters due to parametric mismatch. At time of transition, if the circulating current or the transitional spike exceeds the absolute maximum capacity of inverter then there may be a possible inverter failure leading to added stress on the other connected inverters.

The control algorithm presented in Fig. 6.2 caters to reduction in both the transitional spikes and circulating current. The PLL locks the phase reference for islanded mode with the last sampled phase under grid connected mode damping any phase transitional overshoot. While the resonating frequency of SOGI adaptive filter is brought to the nominal frequency based upon the adaptive droop curve and the sensed output power of the inverter in accordance to the droop coefficient shown in (1).

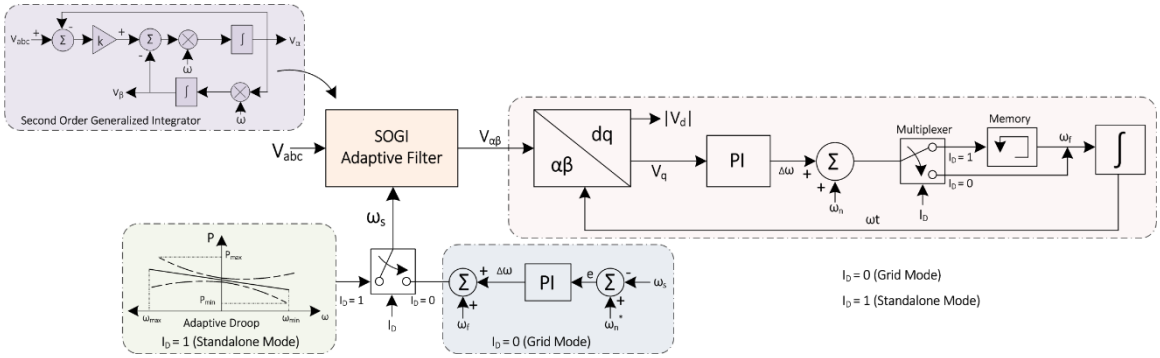


Fig. 6.2 Proposed Adaptive Re – Synchronization Algorithm

$$\omega = \omega' - G_P(s)(P - P^*) \tag{1}$$

An exponentially adaptive power band based upon the maximum capacity of the inverter restricts the power exceeding the maximum capacity of the inverter based on (2).

$$y = P_m e^{\frac{|f - f_n|}{c}} \tag{2}$$

Where, 'Pm' is the maximum power, 'f' is the frequency, 'f_n' is the nominal frequency and 'c' is the scaling factor. The operation of adaptive droop controller under islanded mode can be described under four conditions for transition to islanded mode as shown in Fig. 6.3.

6.2.1.1.1. Heavy loading condition with no circulating current

Initially at operating point O, controller transits to islanded mode, with the heavy loading pushing the operating point of the inverter to the absolute maximum capacity of inverter (P_{max} i.e. pt A) limited by the adaptive curve. To protect the inverter from any possible damage it is essential the droop controller reduces the frequency based upon (1) thereby reducing the inverter output power switching the operation from pt A to pt A′. The frequency is further reduced keeping the inverter output point below the maximum allowable capacity corresponding to the system frequency. On reaching the pt A″, the inverter operates at its rated capacity 'P_{m1}' meeting the heavy load demands.

6.2.1.1.2. Light loading condition with no circulating current

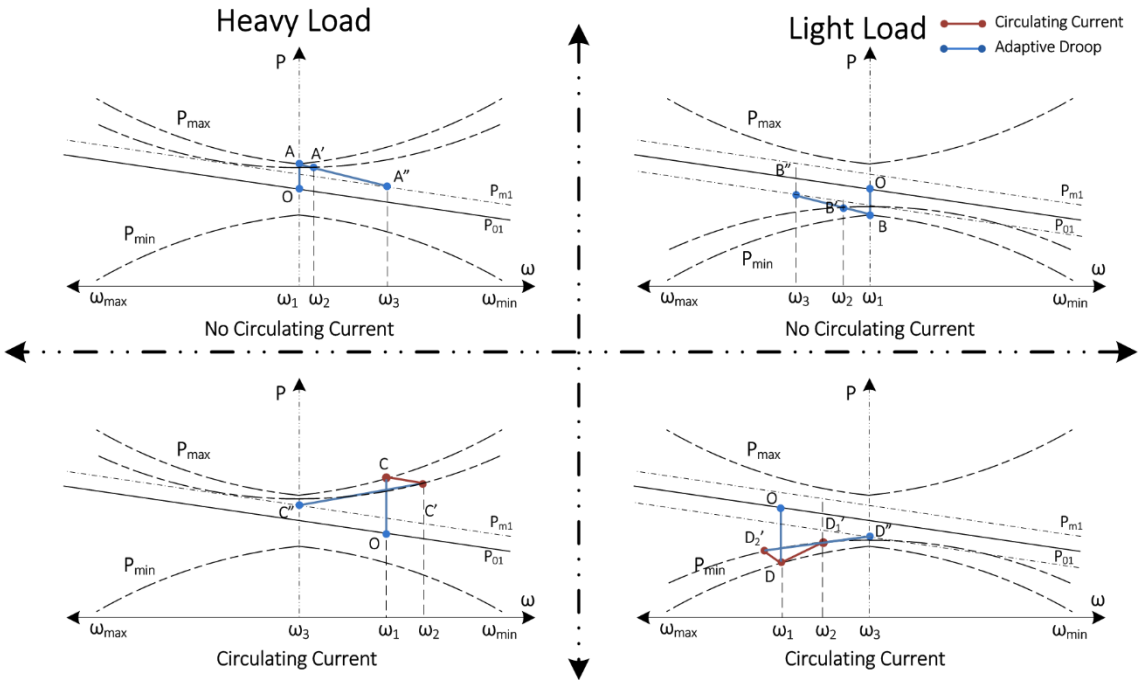


Fig. 6.3 Adaptive Droop Control

Under light load condition, at the outage of grid the output power of inverter reduces due to low power demand i.e. switching from pt O to pt B. the output power reaching the minimum operating capacity limited by the adaptive curve is increased by increasing the operating frequency from pt B to pt B′ and subsequently pt B″ in accordance to (1).

6.2.1.1.3. Heavy loading condition in presence of circulating current

Initially it is taken that the operating frequency of the inverter (pt O) is less than 50 Hz pertaining to heavy load condition. At outage of grid, the operating point of inverter moves to pt C with the maximum power limited by the adaptive curve. The presence of circulating current at the time of transition increases the power at the output terminal of the inverter, increasing the danger of failure. To protect the inverter from failure the frequency is drooped (pt C′) to limit the output power of the inverter until circulating current is present. As the circulating current is reduced to 0, the frequency is gradually increased based on (1) to increase the output power of inverter such that it meets the required load demand and the inverter settles at pt C″ i.e. the nominal.

6.2.1.1.4. Light loading condition in presence of circulating current

At the instance of grid return, the control of the inverter switches to current control mode with the grid being the master determining the voltage and the frequency. On return of the grid, the dynamics are dependent over the phase and frequency deviation of the incoming grid. To reduce the transitional overshoot, the control algorithm shown in Fig. 2 uses independent PI controllers. First PI controller embedded in the phase locked loop compensates the phase error of the incoming grid, while the second PI compensator atones any error in the frequency at which the SOGI adaptive filter resonates. Use of two PI controllers allows enhanced control over the system dynamics.

6.2.1.2. Islanded to Grid Connected Mode

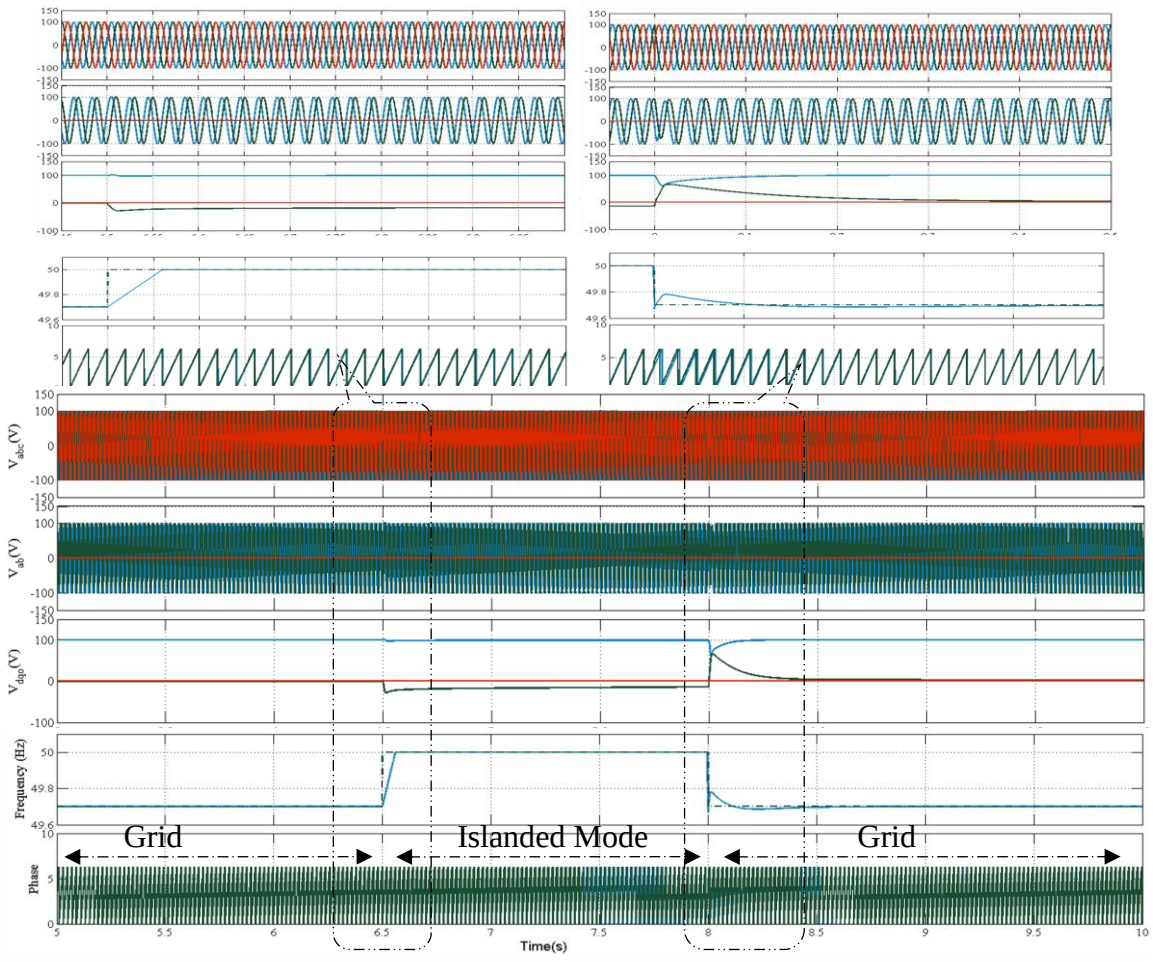
At the instance of grid return, the control of the inverter switches to current control mode with the grid being the master determining the voltage and the frequency. On return of the grid, the dynamics are dependent over the phase and frequency deviation of the incoming grid. To reduce the transitional overshoot, the control algorithm shown in Fig. 6.2 uses independent PI controllers. First PI controller embedded in the phase locked loop compensates the phase error of the incoming grid, while the second PI compensator atones any error in the frequency at which the SOGI adaptive filter resonates. Use of two PI controllers allows enhanced control over the system dynamics

6.2.2. Performance Analysis

The proposed adaptive droop – based synchronization / resynchronization algorithm for seamless transition from grid connected to islanded mode and vice versa is designed and simulated under MATLAB Simulink environment. The grid voltage is taken as 100V (pk-pk) at 49.7 Hz, while the nominal frequency for islanded operation is taken to be 50 Hz.

6.2.2.1. Dynamic Response without Circulating Current

The dynamic response of the controller under no circulating current is shown in Fig. 6.4. Initially, the algorithm operates in grid connected mode with peak grid voltage V_d of 100V at a grid frequency of 49.7 Hz. At t = 6.5s, the system transits from grid connected mode to islanded mode and the control algorithm switches to adaptive droop controller. The resonating frequency of the SOGI adaptive filter is mastered by the droop controller and gradually increases depending upon the droop coefficient. The phase sequence is locked at the last sampled phase in grid connected mode thereby eliminating the phase transients. The frequency gradually increases to nominal frequency of 50 Hz at t = 6.56s. V_d is maintained at 100V while V_q is maintained at -12V. At t = 8s, the grid operation is restored with the PI compensator of PLL compensating the phase error in respect of the



incoming grid. The PI

Fig. 6.4 Transition with no circulating current i) Vabc ii) $V_{\alpha\beta}$ iii) V_{dq} iv) Frequency v) Phase

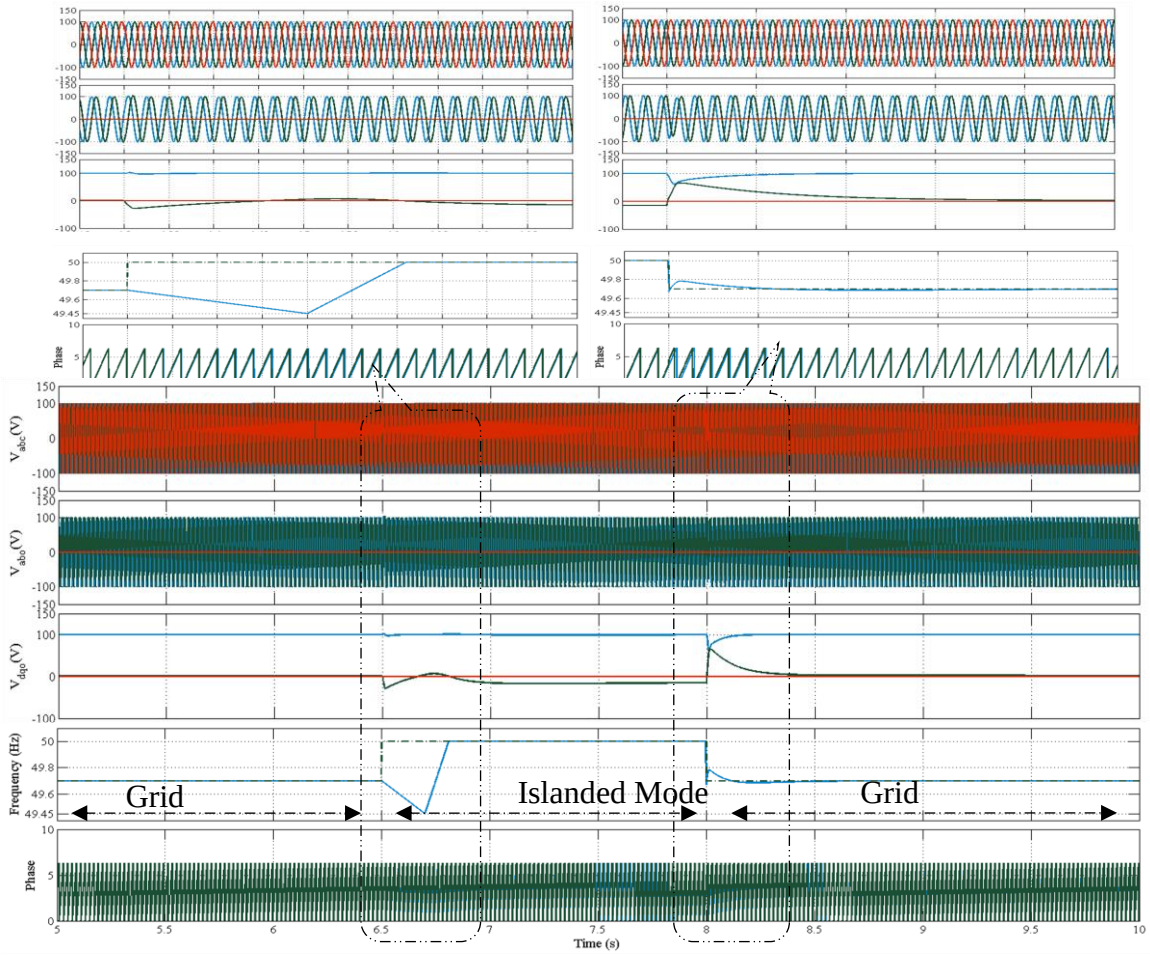


Fig. 6.5 Transition with circulating current i) Vabc ii) $V_{\alpha\beta}$ iii) V_{dq} iv) Frequency v) Phase

compensator for the SOGI adaptive filter damps the frequency error transients between the limits of ±0.2 Hz resonating the SOGI adaptive filter at grid frequency of 49.7 Hz. The magnitude V_d is maintained at 100V with V_q reducing to 0V.

6.2.2.2. Dynamic Response with Circulating Current

The dynamics of the proposed controller is further verified under presence of circulating current as shown in Fig. 6.5. The initial dynamics remain the same as discussed above. At t = 6.5s, as discussed above, in presence of circulating current at the instance of transition, the controller transits from grid connected mode to islanded mode and decreases the frequency to limit the output power of the inverter and maintains the inverter output power

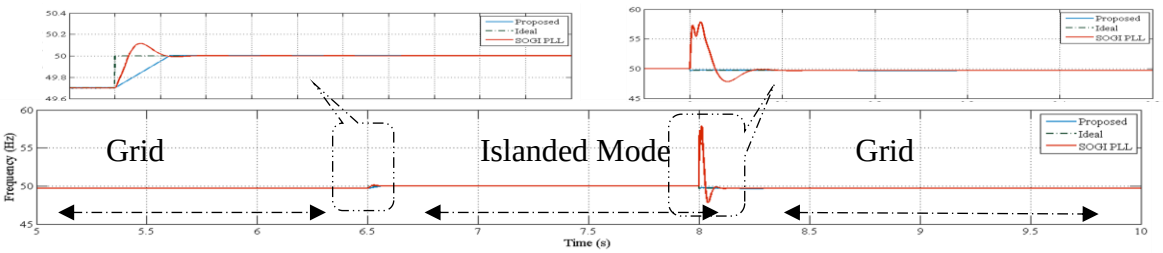


Fig. 6.6 Comparison with conventional SOGI – PLL

below the maximum capacity. At t = 6.7s, as the circulating current reduces to 0, the system frequency again rises in accordance of the droop coefficient and reaches the nominal frequency of 50 Hz at t = 6.81s. At t = 8s, the controller transits to grid connected mode with the system dynamics the same as discussed above. To validate the effectiveness of the control algorithm, the response of adaptive droop controller is compared to that of conventional SOGI – PLL for the transitions of grid connected to islanded mode and vice versa as shown in Fig. 6.6. It can be observed that the proposed control algorithm transits with minimal overshoots

6.3. Conclusion

The results affirm the proposed control algorithm under transitions from grid connected mode to islanded mode and vice versa. The results depict the capability of the proposed adaptive droop controller to restrict the transitional spikes and regulate the operating point of the inverter such that the output power of the inverter never exceeds the maximum inverter capacity. Moreover, with the seamless synchronization / resynchronization algorithm embedded within the synchronization algorithm, the computational burden is significantly less.

Chapter VII

SIMULATION AND EXPERIMENTAL VALIDATION OF GRID TIED INVERTER

7.1. Introduction

In this chapter the proposed continuous input current series cascaded impedance converter to power the DC link bus is coupled with the grid through a conventional H – bridge inverter. This chapter discusses the simulation of the practical implementation of the synchronization and resynchronization algorithms as proposed in chapter 5 and chapter 6 respectively. The experimental results establish the seamless transition of the inverter from grid forming mode (off grid mode) to grid tied mode (on grid mode) of operation and vice versa. The series architecture ensures integration of multiple PV modules interfaced through modular converter governing individual MPPT algorithm. The individual unit of impedance converter uses auxiliary diode ensuring continuous input current throughout the switching state. The shunt impedance capacitor charges to a higher voltage both for normal operating conditions and shoot through conditions unlike conventional impedance networks. The architecture of the proposed cascaded impedance fed grid connected inverter is shown in Fig. 7.1.

7.2. Impedance Based Converter Fed Grid Connected Inverter

The architecture supports distributed generation with modular approach ensuring plug and play operation especially in hostile terrains. Photovoltaic modules rated at 300W (72 cells) with V_{MP} and I_{MP} of 37V and 8A respectively are connected to impedance

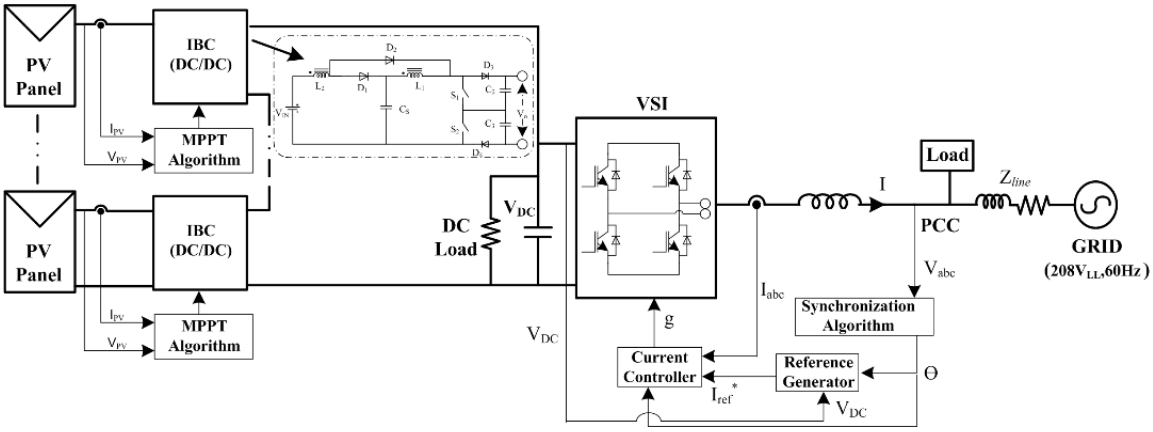


Fig. 7.1 System Architecture

converter. The cascaded impedance converters, commutatively push the generated power across DC link capacitor to the grid. Each impedance converter is controlled to enact current sources, with gating of switches governed by MPPT algorithm using Incremental Conductance (InC) method. Individual control of each module ensures most efficient utilization of PV panels under intermittent conditions, particularly partial shaded conditions.

The PV panels and impedance converters are interfaced to the grid through VSI operating in current controlled mode. The nominal grid voltage is taken as $208V_{L-L}$ at 60Hz with the DC link maintained at 380V to push the generated power to the grid all the time except extreme conditions to the connected loads. The VSI is synchronized with the grid through Double Frequency Second Order Generalized Integrator Phase Locked Loop (DFSOGI – PLL). The current reference drawn out as per SRF theory controls the switching of VSI after passing through error compensator.

7.3. Control Technique

The output of photovoltaic module extensively depends on the environment and surrounding conditions making it essential to always harvest maximum power through the panel to elongate the life of the panel and to justify cost involved in the generation. The control of the proposed solution can be seen in two distinct parts, one deals with PV based generation and its accumulation on DC bus and the other for evaluation of power from DC bus for feeding into AC grid. Accordingly, in the first part, impedance converter treats the PV panel as a current source and extracts maximum available power

through InC algorithm. The algorithm provides the requisite operating duty for the converter for gating sequence of switch S_1 at 25kHz, while the gating sequence of switch S_2 is phase shifted by 180^0. The control realizes the extraction of maximum power through impedance converter as current source at DC bus. It is therefore the onward control mandated for VSI must look forward to maintenance of DC bus and thereby pushing the appropriate current for transaction of real power to the grid. The control scheme for grid connected GCI is realized in current control mode for feeding the generated power to the grid at PCC. VSI is synchronized through DFSOGI – PLL, which acts as band pass filter resonating at double the nominal frequency fed from the phase locked loop and generates quadrature signals. The quadrature signals are directly fed to PLL compensating frequency variations and generating sine/cosine signals for Parks transformation. The DC bus voltage is regulated through PI controller responsible for generating the magnitude of the current reference which in tandem after error compensation provides switching for GCI.

7.4. MATLAB Based Simulation and Control

The proposed cascaded impedance converter is designed and simulated under MATLAB Simulink environment. Five PV panels rated at 300W, are connected as sources impedance converter, in turn feeding DC bus of GCI, considered operating at a nominal V_{L-L} of 208V,60 Hz distribution grid. Each converter is individually controlled by InC algorithm for extracting maximum power from the panel at all instances. The performance of converter is observed under intermittent conditions, viz, complete shading and partial shading. System parameters are shown in TABLE VIII.

Fig. 7.2 shows the response of the impedance converter and GCI during complete outage of one panel through shading. Fig. 7.2.a. shows the response of DC side in terms of output voltage at PV panel terminals (V_{PV}); PV current (I_{PV}); Maximum Power extracted from PV panel (P_{MPP}); output voltage of impedance converter (V_{CONV}) and voltage of C_S (V_S). Fig. 7.2.b shows the common DC bus voltage (V_{DC}), cascaded impedance converter output current (I_{CONV}) and d axis component of reference current of GCI (I_d). Fig. 7.2.c depicts the PCC voltage (V_{PCC}); source side current referenced

TABLE VIII
SIMULATION PARAMETERS

Name	Quantity/Value
PCC Voltage	$208V_{L-L}$
Photovoltaic Panel Max Power (P_{MPP})	300W
Max Voltage and Current (V_{MP}, I_{MP})	37V, 8A
DC Link Voltage	380V
Switching Frequency	25kHz
Impedance Capacitor (C_S)	100 μF
Output Capacitor (C_2 & C_3)	47 μF
Inductor L_1, Turns Ratio	300μH, 2

from PCC (I_{GRID}); load current (I_{LOAD}) and GCI output current (I_{INV}). The initial transients of the system are ignored as the same can be taken care by soft starting procedures. During the initial phases the cascaded impedance converters are considered disconnected from the GCI and of 38V at an operating duty of 52%. At t=0.4s, the impedance converter is interfaced to the DC bus with the grid pulling up 3.5A across the DC bus capacitor. The GCI supports the grid on source side with 3A (pk-pk) and connected load at the PCC with peak-to-peak current of 3.5A, with a net injection of 6A (pk to pk) with little reactive power support. At t=0.55s, one panel is completely bypassed on account of shading, resulting in complete outage of one unit of impedance converter as shown in Fig.7.2, the operating point for the unshaded panel shifts towards V_{OC} during transient but gradually settles back to MPP condition sharing the stress equally. Output of each unshaded impedance converter other than the one which is fully black rises to 95V with C_S of each unshaded units charged to 45V. The cascaded units thus accumulate a voltage of 380V aggregated at the DC bus. The 2.7A of current contributed at 380V feeds GCI caters to the load and curtails the source side current to 0.2A.

The response of the system is further investigated for the condition of partial shading as shown in Fig 7.3. The response during unshaded remains the same as the status quo is maintained at the PV side. At t=0.55s, one panel is partially shaded by half allowing the bypass diodes to operate, the voltage of the partially shaded panel drops to 18V, while the operating point temporarily of unshaded panels temporarily shifting towards V_{OC} (Refer Fig 6a). The maximum power output of the converter pertaining to shaded panel reduces to 140W with the shunt capacitor charged to 19V and output voltage reducing to 35V. The stress is equally shared by the healthy converters with their output voltage rising to 85V and shunt capacitor getting charged to 42V. The output current of

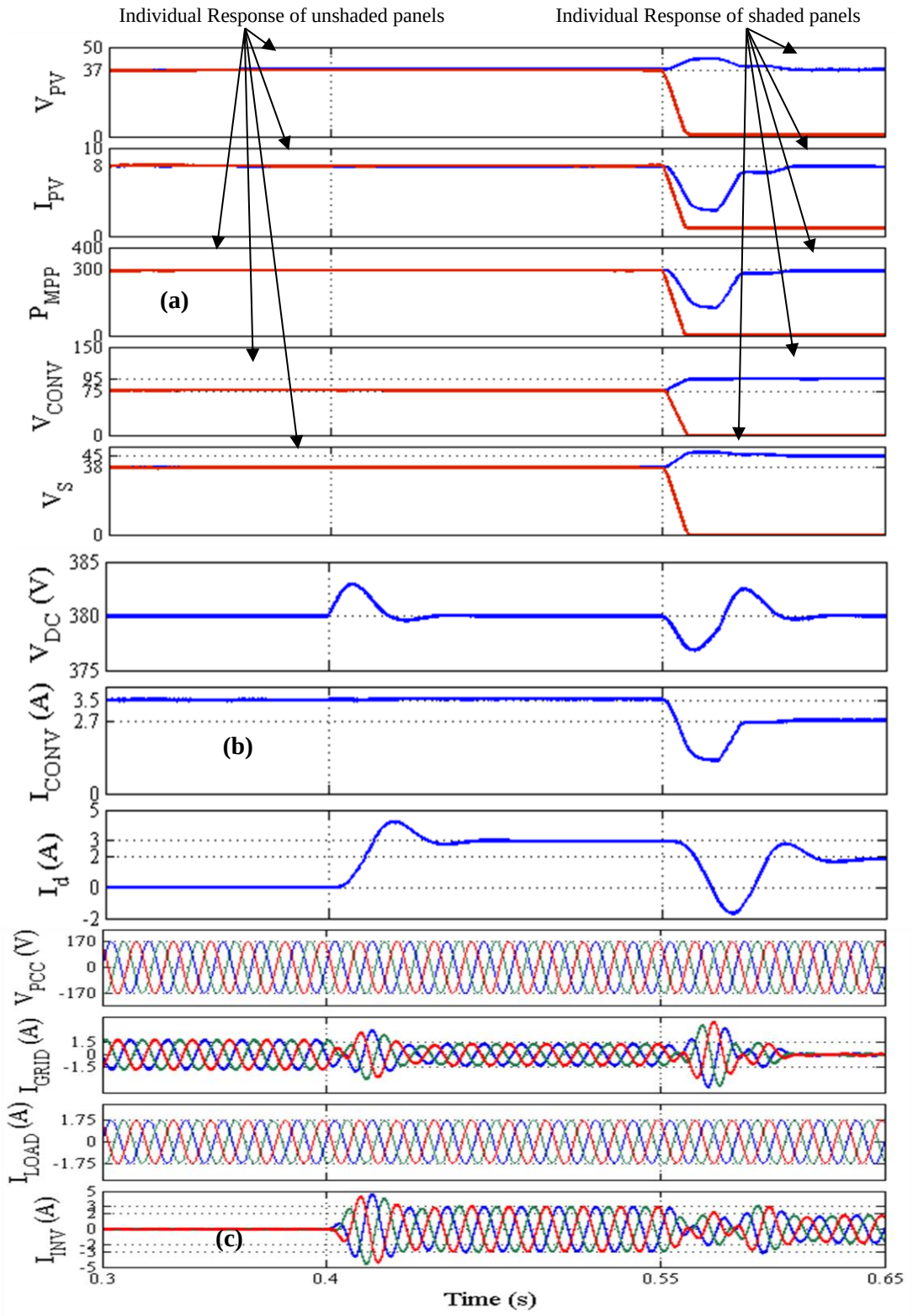


Fig 7.2. a) i) Input Voltage ii) Input Current iii) Input Power iv) Output Voltage v) Shunt capacitor voltage b) i) DC link voltage ii) Converter output current iii) I_d c) i) V_{PCC} ii) Grid Current iii) Load Current iv) Inverter current under outage of one panel

the string reduces to 3A from 3.5A (unshaded condition) while inverter output current reducing to 4.8A (pk- pk) as shown in Fig 7.3.b and Fig 7.3.c respectively and is shown capable of pushing 1.2A (pk-pk) under partially shaded conditions. Thus, converter

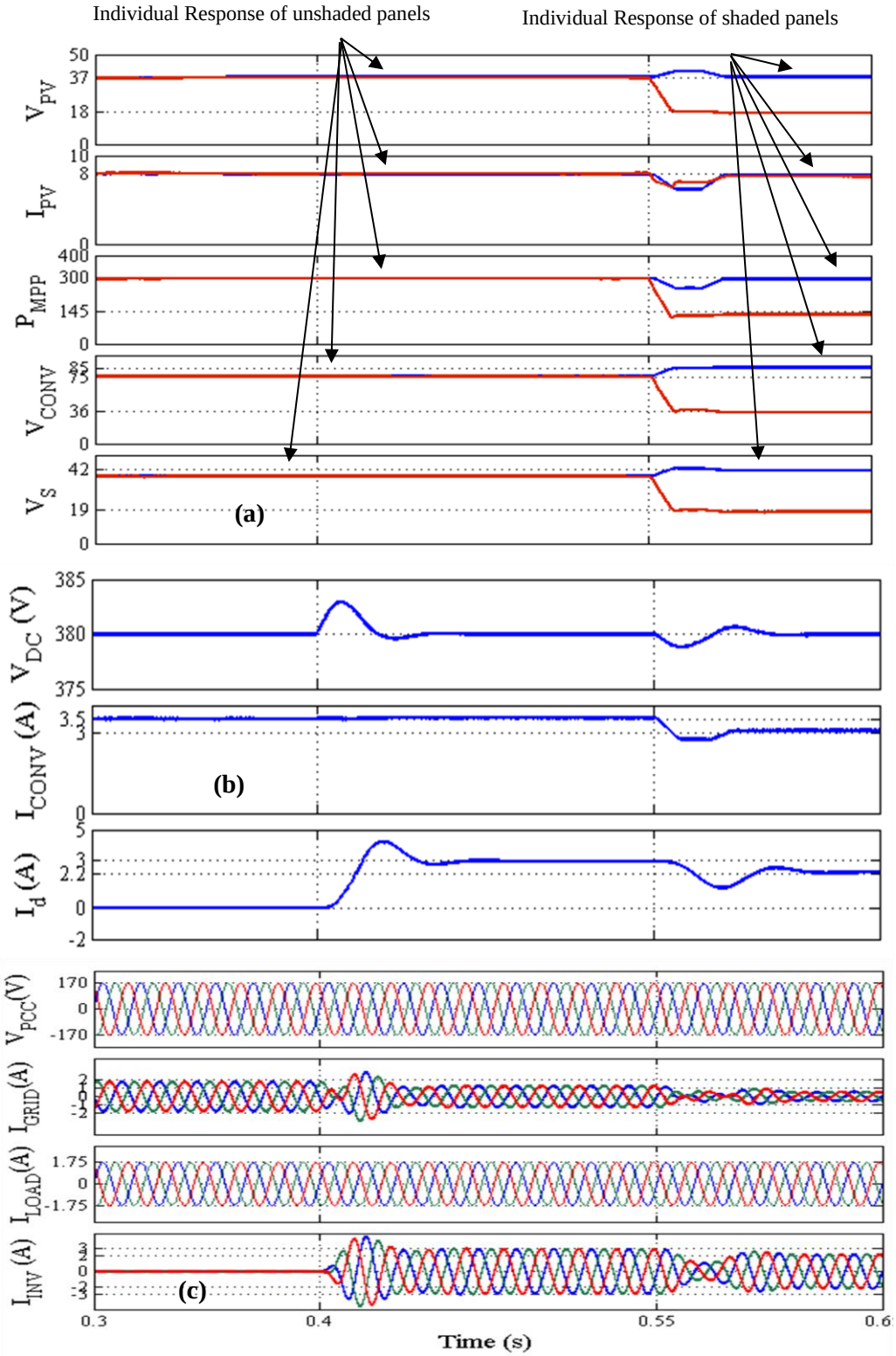


Fig 7.3. a) i) PV Voltage ii) PV Current iii) Max. Power iv) Output Voltage v) Shunt capacitor voltage b) i) DC bus voltage ii) MT - IBC output current iii) I_d c) i) V_{PCC} ii) Grid Current iii) Load Current iv) Inverter current under partial shading condition

demonstrates the uninterrupted support to the grid under wide variations at input side, making the system reliable and robust.

7.5. Prototype – Grid Connected Inverter

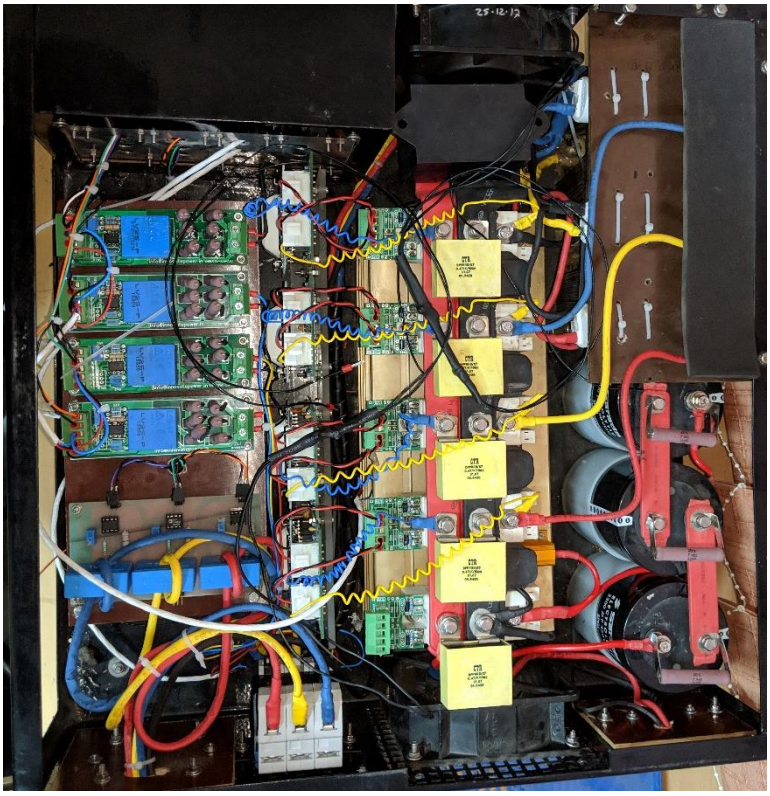


Fig. 7.4 Experimental Setup of Grid Tied Inverter

Fig.7.4 shows the experimental setup for the grid tied inverter with the IGBT stacks from Semikron, representing the individual half bridge leg of the inverter. The voltage and current sensing are achieved through isolated voltage and current sensors LV25P and LA25P rated for 1000V and 25A respectively. The gate drive for the IGBT modules is given through gate drive module SKYPER 32 PRO. An additional IGBT stack is used for over voltage protection of the DC link as shown in the over voltage protection section in Fig. 7.1. For practical realization two IGBT modules are used, working as 1φ inverter, an additional IGBT stack is used as over voltage protection . An interfacing inductor of 3mH with filter capacitor of 4.7MFD is used in the experimental setup.

TABLE VIII
EXPERIMENTAL SETUP

Name	Quantity/Value
TOPOLOGY	H BRIDGE
IGBT	SEMIKRON 75GB12T4
IGBT DRIVER	SKYPER 32 PRO
VOLTAGE SENSOR	LV25P
CURRENT SENSOR	LA25P
DC LINK CAPACITOR	1.1 MFD
INPUT GRID VOLTAGE	$230V_{RMS}$
INTERFACING INDUCTOR	3mH
FILTER CAPACITOR	4.7MFD
CONTROLLER	dSPACE 1104

The hardware details of the experimental setup are as given in TABLE VII –

The gate for the IGBT stack is as per the hybrid modulation technique where in one leg of the inverter is drived at fundamental frequency of 50Hz. The other IGBT leg is drived by sinusoidal pulse width modulation technique as shown in Fig.7.5.

Fig. 7.5 Sinusoidal Pulse Width Modulation of Voltage Source Inverter

Fig.7.6 confirms the grid tied operation of the inverter with the inverter feeding the grid maintained at rms voltage of 228.46V. The inverter feeds are rms current of 17.40A

thereby feeding 4kW in the utility grid. The inverter feeds current in phase with the grid voltage maintaining the phase locking and synchronization.

The peak current and voltage being fed to the grid is 22.18A and 316.4V respectively as depicted in Fig.7.7. Fig.7.8 depicts the off-grid operation of the inverter. The inverter feeds the connected load of 380W, maintaining a rms grid voltage of 219.43V. The inverter feeds a bulb load of 380W with rms output current of 1.73A. The current maintains power factor close to unity with respect to the grid voltage.

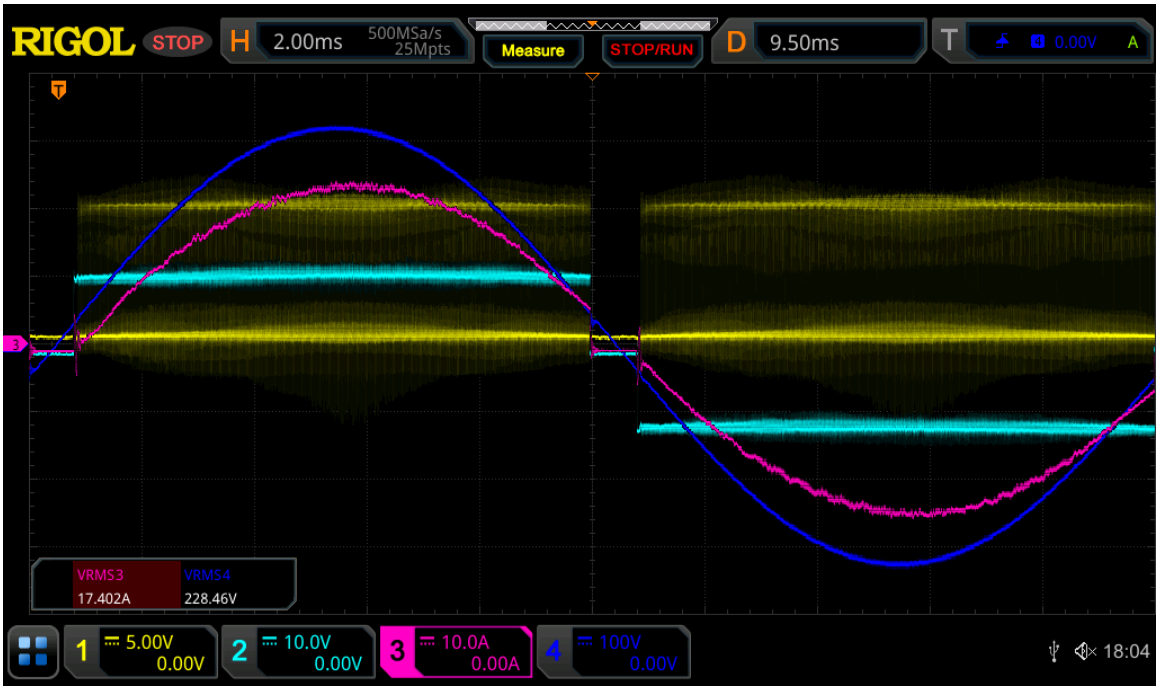


Fig. 7.6 Grid Voltage; Grid Current and Pulse Width Modulation of Voltage Source Inverter (Grid Tied Operation)

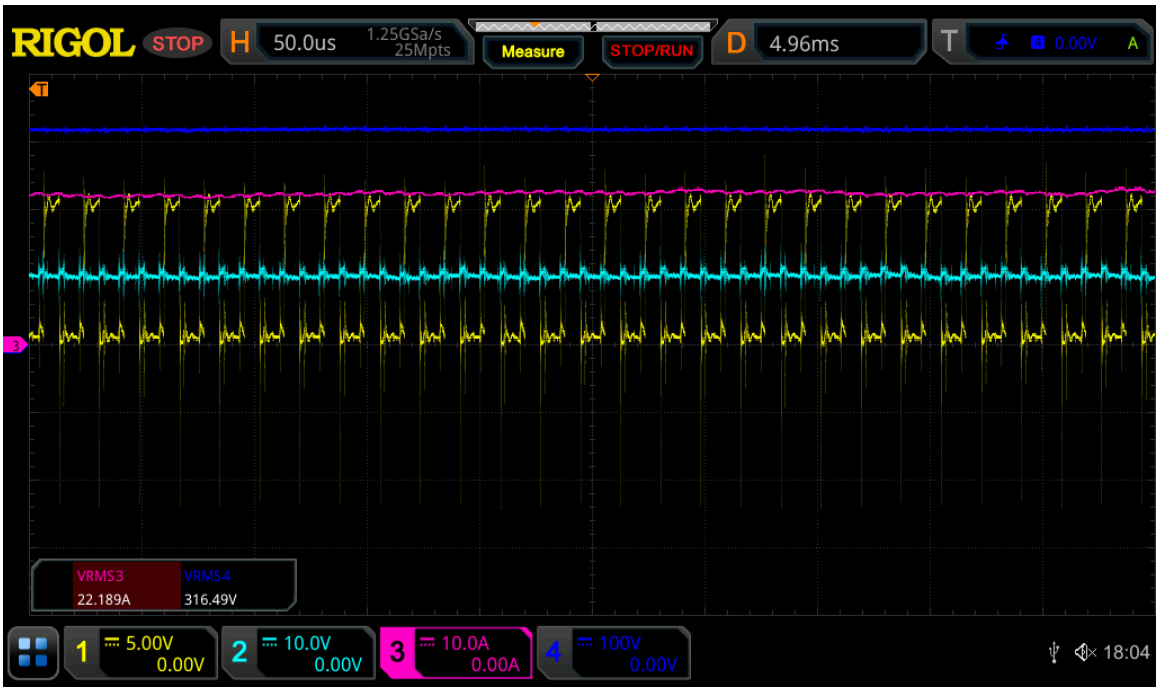


Fig. 7.7 Peak value of Grid Voltage and Grid Current

Fig. 7.8 Grid Voltage; Grid Current and Pulse Width Modulation of Voltage Source Inverter (Off Grid Operation)

Fig. 7.9 Transition from Grid Connected Mode to Off Grid Mode of Operation

Fig.7.9 shows the mode transition of the inverter from grid connected mode of operation to off grid mode of operation. The grid supply is interrupted resulting in the inverter being disconnected from the grid with the help of the islanding detection algorithm as

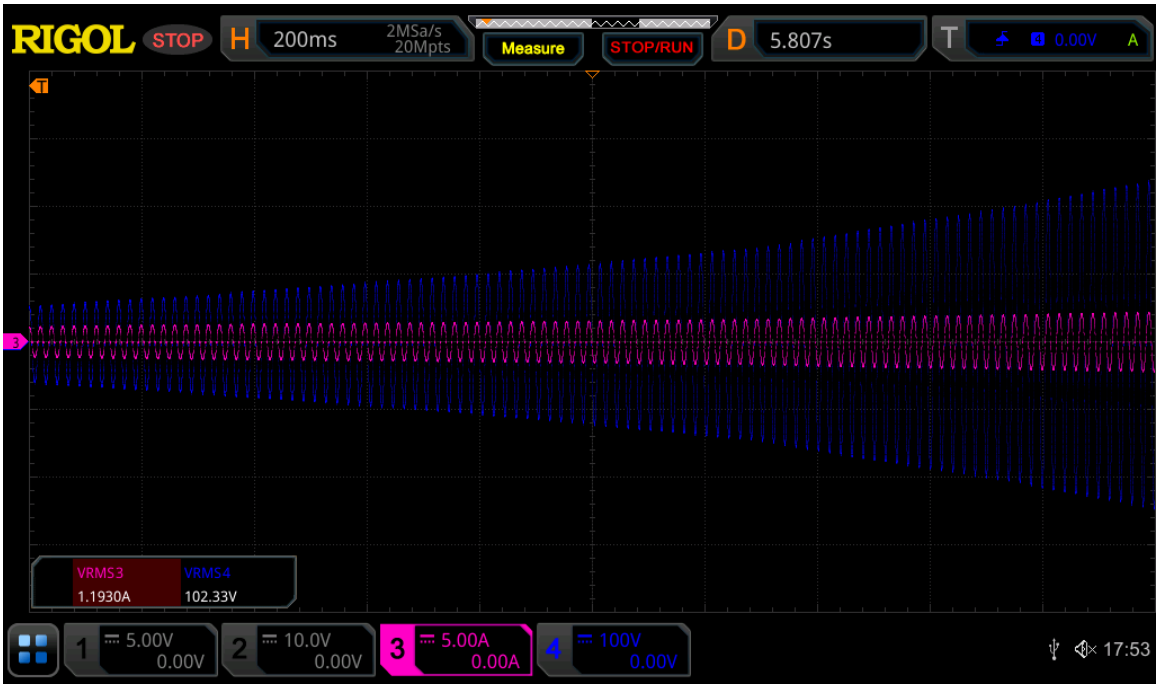


Fig. 7.10 Soft Start (Off Grid Mode) – Zoom 1

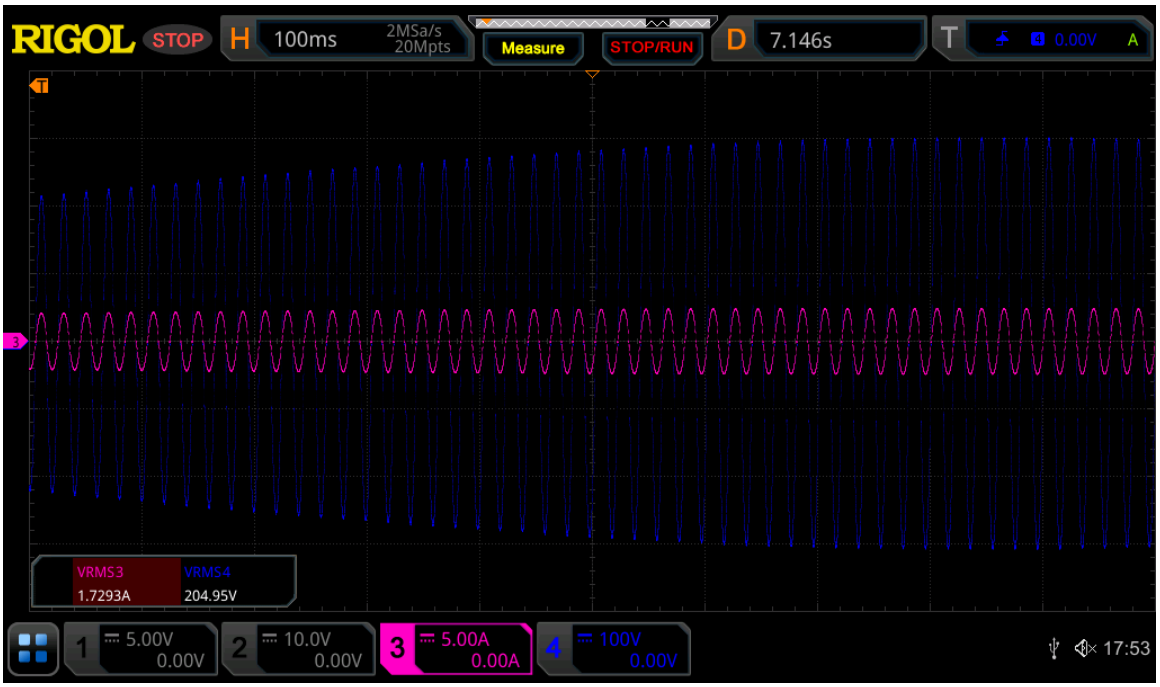


Fig. 7.11 Soft Start (Off Grid Mode) – Zoom 2

proposed in previous chapter. A small leakage voltage of 60V is observed between the phases of the inverter. The inverter initiates the soft startup sequence with the inverter slowly increasing the voltage across the load to a rms voltage of 220V. The soft start

sequence reduces the voltage spike across the load as observed in Fig.7.10 and Fig.7.11 respectively.

Fig.7.12 depicts the transition of the inverter from off grid mode of operation to grid tied mode of operation. The islanding algorithm detects the grid presence and initiates the transition from off grid mode of operation to on grid mode of operation. Common mode voltage of 60V is observed during the changeover sequence and the inverter transits is synchronized with the utility grid and transits into grid connected mode of operation. The control algorithm initiates the soft start sequence where the current inverter output current gradually increases to the steady state value as shown in Fig.7.12.

The performance of the developed hardware prototype for the grid connected inverter is validated along with the performance of the previously proposed synchronization and resynchronization algorithms. The developed hardware solution incorporates on board current and voltage sensing, over current and over voltage protection.

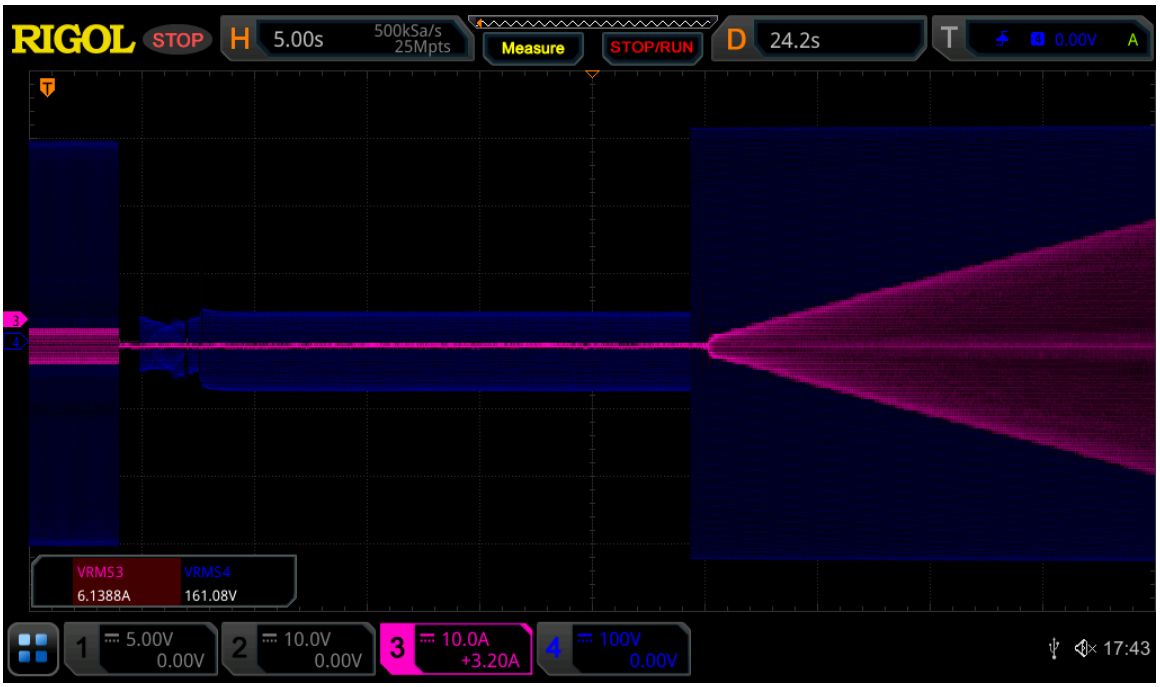


Fig. 7.12 Transition from Off Grid Mode to Grid Connected Mode of Operation

Chapter VIII

MAIN CONCLUSION AND FUTURE WORK

8.1. Main Conclusion

The work presented in the thesis has meticulously figured out the challenges and research gaps for seamless integration and synchronization of voltage sourced inverter with the grid and identified befitting converter topologies, synchronization and re – synchronization algorithms best suited for grid connected inverters under present grid norms. The work presents implementation of impedance network on the DC side of the inverter restricting the flow of the circulating currents among the inverter units. Unlike the conventional T source converter, the proposed impedance converter has continuous input current providing better MPPT tracking efficiency and the auxiliary boost capability allows wide operating range for the converter. The impedance converter is modeled and simulated in MATLAB simulation environment and a small-scale prototype of the same is developed. The developed prototype is experimentally validated for severe dynamics like partial shading and irradiation change, validating the theoretical calculations and superior performance of the converter.

Based on the same principal a bidirectional impedance converter is modeled and designed for grid to vehicle and vehicle to grid charging applications. The bidirectional impedance converter is a multiport topology allowing stacking of batteries at the input terminal. The multiport architecture along with an easy and robust control algorithm allows charging and discharging of the batteries at different rates based upon their present state of charge. The experimental results of the bidirectional impedance converter demonstrate the capability of the converter for the application of grid to vehicle and vehicle to grid application.

After establishing strong foundation on the DC side, a synchronization and resynchronization algorithm is developed based on Second Order Generalized Integrator adaptive filter. The synchronization algorithm resonates at double the fundamental

frequency i.e. 100Hz. The synchronization algorithm resonating at 100Hz significantly improves the dynamic performance of the system by limiting the transient overshoots and undershoots and reducing the settling and damping time. Additionally, operation at 2nd harmonic frequency curbs the low harmonic resonance as observed. The performance of the algorithm is analyzed with respect to the conventional SOGI – PLL algorithm, and the results demonstrate the superior performance of the proposed algorithm.

An adaptive droop-based resynchronization algorithm embedded in the phase locked loop is modeled and simulated. The resynchronization algorithm incorporates protection against any circulating current observed among inverters. The resynchronization algorithm based on the Second Order Generalized Integrator based Phase Locked Loop negotiates the transient spikes during mode transfer besides administering fast dynamics.

A prototype of an industrial grid tied inverter is also developed as presented in the work and interfaced with the grid. The developed prototype validates the synchronization and resynchronization algorithms as developed.

8.2. Future Scope of the Work

Since research and development over new ideas, innovations, technology and techniques is a never ending process, there are many more avenues that may be worked upon and explored over the coming years. Further scope of work as per the author is as below for future study –

1. Incorporation of faster dynamics MPPT algorithm with the capability to track local and global maximum power point which would enhance the overall system performance.
2. Multiple inverters may be integrated together developing a microgrid and study may be done over further issues observed.
3. Wide band gap devices may be explored for power dense solution; with silicon carbide (SiC) for the inverters and gallium nitride (GaN) devices for the DC – DC converters.

4. Lithium-Ion battery bank may be explored for battery energy storage system.
5. Common mode analysis of the inverter is required for understanding the dynamic performance of the inverter.

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