DESIGN AND ANALYSIS OF SRAM CELLS UNDER STABILITY, POWER AND SPEED CONSTRAINTS

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by

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CANDIDATE'S DECLARATION

I, **Ram Murti Rawat** (**Roll No. 2K19/PHDCO/13)** student of Ph.D., hereby declare that the Dissertation titled "**Design and Analysis of SRAM Cells under Stability, Power and Speed Constraints**" which is submitted by me to the Department of Computer Science and Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of **Doctor of Philosophy**, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma, Associateship, Fellowship, or other similar title or recognition.

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Certified that **Ram Murti Rawat** **(2K19/PHDCO/13**) has carried out their research work presented in this thesis entitled **"Design and Analysis of SRAM Cells under Stability, Power and Speed Constraints"** for the award of **Doctor of Philosophy** from Delhi Technological University, Delhi, under my supervision. The thesis embodies results of original work, and studies are carried out by the student himself, and the contents of the thesis do not form the basis for the award of any other degree to the candidate or to anybody else from this or any other University/Institution.

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ABSTRACT

Memory plays a vital role in most of the electronic devices used in embedded systems. The increasing processing workload has led to a growing demand for low-power, high-performance SRAM cells. The memories are formed by an array of SRAM cells for data storage and their peripheral circuits. The peripheral circuit comprises row-column decoders and pre-charge circuitry. The 6T SRAM cell was the industry standard, but with decreasing technology node and V_{DD} scaling, the performance of the 6T SRAM cell was deteriorating. This has motivated researchers to design other SRAM cells. SRAM cells play a crucial role in the design of system-on-chips (SoCs), constituting a substantial portion of the die area and thereby contributing to increased power consumption. Despite significant advancements in SRAM performance in finer technologies, concerns persist regarding cell stability in the deep sub-micron domain.

This thesis introduces an innovative approach to address these issues by proposing a low-power SRAM cell based on swing restoration inverter (SRI). The swing restoration inverter (SRI) addresses the challenge of swing voltages in finer technologies by integrating two additional transistors to act as swing-restored elements. This innovation results in an impressive 67% reduction in leakage power at 27°C for the 90 nm technology. To evaluate the effectiveness of the proposed SRI-based SRAM cell, performance metrics such as delay and power delay product are calculated. In the context of a 6T SRAM cell in the 90 nm technology, the conventional inverters are replaced with the swing restoration inverter (SRI). The implementation of SRI in the proposed 8T SRAM cell leads to a substantial 86% reduction in leakage power at 108°C and an impressive 91.22% reduction at 27°C compared to the conventional 6T SRAM cell. The SRI technique proves instrumental in enhancing stability, resulting in the proposed 8T SRAM cell outperforming its 6T SRAM counterpart. However, it's important to note that the heightened performance of the proposed 8T SRAM cell comes at the expense of two additional transistors. Simulations are conducted using the 90 nm technology and the Cadence Virtuoso simulator to validate the effectiveness of the swing restoration inverter (SRI) technique in leakage power consumption and enhancing stability in SRAM cells.

This thesis examines the factors that affect the Static Noise Margin (SNM) of Static random-access memories. Find the equivalent time, improve hold, read, and write operation of the low power 8T SRAM cell, which is better than 6T SRAM and standard

8T SRAM cells using swing restoration dual node voltages for hold, read, and write operation, and improve stability analysis. This circuit or architecture-level SRAM technique is required to improve hold, read, and write SNM. This thesis, comparative analysis of 6T SRAM, standard 8T SRAM, and low power 8T SRAM cells with improved read and write noise margin, is completed for nanometer technology.

The typical memory for very large-scale integrated (VLSI) circuits has traditionally been static random-access memory (SRAM) because it has offered faster speeds compared to other alternatives. However, SRAM has been associated with a high-power consumption rate. Researchers have recognized the importance of lowering the power consumption of SRAM cells due to their critical role in memory architecture. This literature review has aimed to provide innovative and effective strategies for designing low-power SRAM cells. Several circuit topologies and methodologies have been introduced to compute stability, leakage current, delay, and power, and novel techniques for designing SRAM cells based on eight transistors (8T) have been proposed. SRAM has frequently been chosen over dynamic random-access memory (DRAM) because it has demonstrated faster speeds and lower power consumption. It has been named "static" because no modification or action, such as refreshing, has been required to maintain data intact. However, leakage current in SRAM has often increased and impaired its performance as technology nodes have been scaled down. Voltage scaling has been adopted as a solution to this issue, although it has also affected the stability and latency of SRAM. A separate (isolated) read port has been employed to enhance read stability, while a negative bit-line (NBL) write-aid circuit has been implemented to improve write ability. The proposed design has been evaluated against cutting-edge approaches based on criteria such as write static noise margin (WSNM), write stability, read static noise margin (RSNM), and other performance metrics. Future research has been directed toward exploring novel circuit topologies and methodologies to further enhance stability, reduce leakage current, and minimize delay and power consumption. Researchers have also investigated the performance of SRAM cells at smaller technology nodes to develop new techniques for maintaining stability and performance at these scales. Additional efforts have been made to explore new approaches to voltage scaling and to develop methods that improve the read and write stabilities of SRAM cells.

In this thesis, we introduce a proposed 8T SRAM cell that incorporates an isolated read path to enhance read stability compared to the conventional 6T SRAM cell. To address leakage power, two PMOS transistors are integrated into the read and write circuitry, effectively minimizing leakage current induced by stacking effects. The proposed 8T SRAM cell design demonstrates a substantial reduction in leakage current, exhibiting a decrease of 61.11% compared to the 6T SRAM cells, respectively. Moreover, the read operation for the newly proposed 8T SRAM cell is significantly improved, showcasing a 53.08% improvement compared to the 6T SRAM cell, respectively. The results also indicate noteworthy speed enhancements during write operations, boasting a 66.66% improvement compared to the 6T and 8T SRAM cells, respectively. The Read Static Noise Margin (RSNM) and write trip point (WTP) of the proposed cell measure at 12 mV and 360 mV, respectively, signifying an improvement over the conventional 6T SRAM cell measures at 6.37 mV and 240 mV. The effectiveness of the proposed cell is validated through comprehensive simulation analyses conducted in the Cadence Virtuoso environment at the 90 nm technology node.

All the proposed cells are of a double-ended nature owing to their better performance at lower power and high speed. This growing demand for double-ended cells has also generated the need for a swing restoration inverter (SRI) and negative bit line (NBL) circuits that are compatible with the array of double-ended SRAM cells. Conventionally, sense amplifiers were designed with differential SRAM cells. These SRAM cells are usually voltage-based in nature, owing to their low power and high speed with low operational V_{DD}. Thus, this generates a need for double-ended SRAM cells that have low power consumption.

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List of Symbols and Abbreviations

Symbol/Abbreviation	Full Form
IC	Integrated Circuit
VLSI	Very large-scale integration
PMOS	P-type metal-oxide semiconductor
NMOS	N-type metal-oxide semiconductor
CMOS	Complementary metal-oxide semiconductor
RAM	Random Access Memory
ROM	Read Only Memory
SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory
RWM	Read Write Memory
VTC	Voltage Transfer Characteristic
BL	Bit line
BLB	Bit line Bar
INV	Inverter
SRI	Swing Restoration Inverter
NBL	Negative Bit-line
DSA	Domain-specific architecture
Vds	Drain-to-source voltage
Vgs	Gate-to-source voltage
C_L	Load Capacitance
HSNM	Hold Static Noise Margin
RSNM	Read Static Noise Margin
WSNM	Write Static Noise Margin
WTP	Write-trip-point
IoT	Internet of Things
Kt	Thermal Noise = 26 mV

W	Width
L	Length
W/L	Width-to-length ratio
PVT	Process, Voltage, and Temperature
Q	Data Node
QB	Data Node Bar
RWL	Read word line
RBL	Read Bitline
SA	Sense Amplifier
PD	Proposed Design
Vt	Threshold Voltage
SNM	Static Noise Margin
SoC	System on Chip
V_{DD}	Supply Voltage
GND	Ground Voltage
V_{OH}	High Level of Output Voltage
V_{OL}	Low Level of Output Voltage
V_{th}	Threshold Voltage
D_{in}	Data input
D_{inb}	Data input bar
WL	Word line
WM	Write Margin
WWL	Write Word line
μ	Mean
σ	Standard deviation
n	Number of Rows
m	Number of Columns
C_{ox}	Oxide Capacitance

CHAPTER 1

INTRODUCTION AND MOTIVATION

The growing depends of civilization on digital devices has opened up a new world of processing and data. This plethora of data and its processing are dependent on various types of powerful digital devices. These devices comprise a microprocessor or a group of microprocessors. An essential component of these microprocessors is the memory circuits that enable their fast operation. In this chapter, a detailed introduction to the memory and its building blocks is presented. It is essential to understand the classification of CMOS memories so as to identify the different aspects that can be worked upon to improve their performance.

This chapter is divided into six different sections, including an introduction to semiconductor process, Section 1.1. It is followed by section 1.2, which is an introduction to memory. Based on the brief introduction of the classification of CMOS memories in section 1.3. Thereafter, in section 1.4, Memory organization. The motivations are used to achieve each desired objective in section 1.5. Finally, in section 1.6, the thesis organization is summarized.

1.1. INTRODUCTION TO SEMICONDUCTOR PROCESS

Semiconductor process technology has been scaling for over four decades. Process technology advancements are the driving force behind the semiconductor industry's growth. In response to increasing consumer demand for improved performance and functionality at a lower cost, the semiconductor industry has developed a new process technology generation every two to three years over the last four decades [1]. Memory is widely employed in all electrical systems, including mainframe computers, microcomputers, and cellular phones. Energy-efficient processors are becoming increasingly important as the need for portable battery-powered computers grows. These gadgets' performance is restricted by their size, weight, and battery life. Serious reliability issues, increased design costs, and battery-operated applications prompted the IC design community to seek out new approaches and methodologies that produce more power-efficient designs, resulting in significant power consumption reductions for the same level

of performance. Memory circuits, such as dynamic RAMs, static RAMs, Ferroelectric RAMs, ROMs, or Flash memories, are an essential component of any system architecture and contribute significantly to system power consumption. Reducing power dissipation in memories can enhance the system's power efficiency, performance, reliability, and total costs. RAMs have been fast growth in low-power, low-voltage memory design in recent years, owing to rising demand for notebooks, laptops, handheld communication devices, and IC memory cards. Various techniques are employed to reduce power dissipation, including power supply voltage scaling through circuit design, power gating, and the use of sleepy systems. Reducing the power supply voltage lowers dynamic power consumption quadratically, but it also increases leakage power exponentially. However, scaling down the supply voltage also decreases the noise margin. Many SRAM arrays are designed to minimize active capacitance and reduce voltage swing. In technologies below 100 nm, leakage currents mainly stem from gate leakage and sub-threshold leakage. Gate leakage can be mitigated with high-k (high dielectric constant) gate materials, while sub-threshold leakage is reduced through methods like forward body biasing and dual-threshold voltage (dual-Vt) designs. In sub-threshold SRAMs, the supply voltage (V_{DD}) is lower than the threshold voltage (Vt) of the transistors, making sub-threshold leakage the dominant operating current [2].

1.2. INTRODUCTION TO MEMORY

Computer data storage, often called storage or memory, refers to computer components and recording media that retain digital data used for computing for some interval of time. The main purpose of storage is that without a significant amount of memory, a computer would merely be able to perform fixed operations and immediately output the result [3]. It has to be reconfigured every time an operation needs to be performed. The hierarchy of storage is as shown in Figure 1.1.

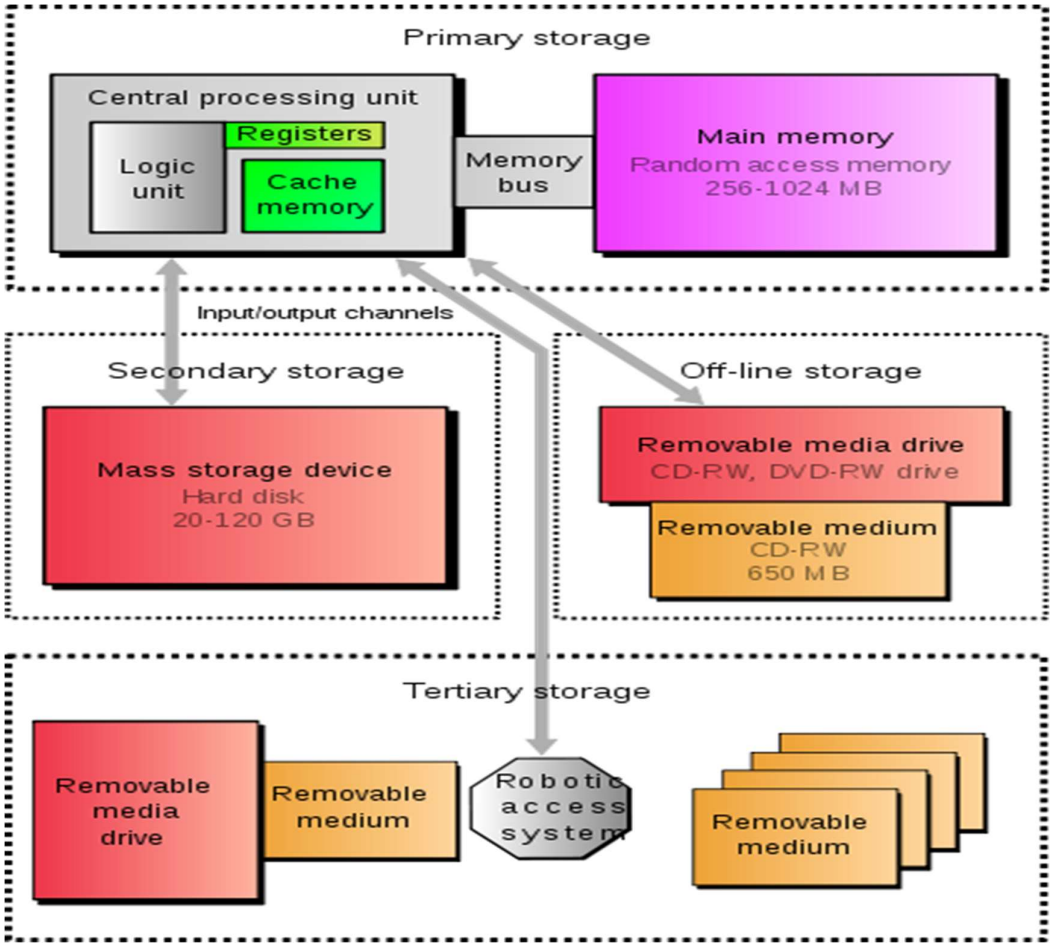


Figure 1.1. Types of Computer data storage [3].

1.2.1 Primary Storage

Primary storage (or main memory or internal memory), often referred to simply as memory, is the only one directly accessible to the CPU. The CPU continuously reads instructions stored there and executes them as required. Any data actively operated on is also stored there in uniform manner.

1.2.2 Secondary Storage

Unlike primary storage, secondary storage (also known as external memory) is not directly accessible by the CPU. The computer typically transmits the needed data via an intermediate area in primary storage and accesses secondary storage through its input/output channels. Since secondary storage is non-volatile, data is not lost when the device is turned off. Additionally, the cost per unit is usually two orders of magnitude lower than that of primary storage. As a result, secondary storage is usually two orders of magnitude larger than primary storage in current computer systems, and data is stored there for extended periods of time.

1.2.3 Tertiary Storage

Tertiary storage or tertiary memory provides a third level of storage. Typically, it involves a robotic mechanism that will mount (insert) and dismount (removable) mass storage media into a storage device according to the system's demands; this data is often copied to secondary storage before use.

1.2.4 Offline Storage

Offline storage is used to transfer information, since the detached medium can be easily physically transported. Additionally, in case a disaster, for example a fire, destroys the original data, a medium in a remote location will probably be unaffected, enabling disaster recovery. Offline storage increases general information security.

1.3. CLASSIFICATION OF CMOS MEMORIES

This section explains the different types of CMOS memories and the given figure 1.2 explains the memory can be classified as volatile and non-volatile memories [4].

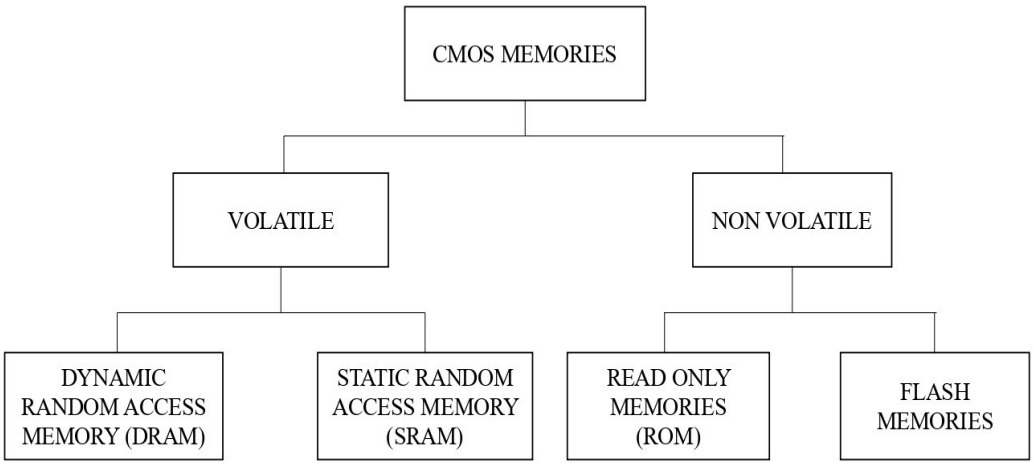


Figure 1.2. Classification of CMOS memories.

1.3.1 Volatile memories

Power is necessary for this memory to preserve the data they contain. Computer data can be stored in random access memory (RAM). It takes the shape of integrated circuits, which provide arbitrary order access to stored data. The concept of randomness states that every item of data, regardless of its physical location or relationship to the preceding piece of data, can be returned in a fixed amount of time.

1.3.1.1 Dynamic Random Access Memory

One kind of random-access memory that keeps each bit of information in a different capacitor inside an integrated circuit is called dynamic random-access memory (DRAM).

The information gradually fades unless the capacitor charge is routinely updated, since real capacitors leak charge. Unlike SRAM and other static memories, it is a dynamic memory because of this refresh requirement. DRAM's structural simplicity is a benefit over SRAM, which requires six transistors per bit, whereas DRAM just requires one transistor and a capacitor.

1.3.1.2 Static Random Access Memory

Because it stores each bit using bistable latching circuitry, static random-access memory (SRAM), a form of semiconductor memory, does not require periodic refreshes like dynamic random-access memory (DRAM). Although SRAM may recall data, it is nevertheless volatile in the traditional sense that when the memory is not powered on, data eventually disappears.

1.3.2 Non-Volatile memories

Non-volatile memory, NVM, or non-volatile storage, is computer memory that can retain the stored information even when not powered. Examples of non-volatile memory include read-only memory, flash memory, and most types of magnetic computer storage devices.

1.3.2.1 Read-Only Memory

ROM is a class of storage that is fabricated with desired data permanently fixed in it, thus it cannot be modified.

1.3.2.2 FLASH Memory

FLASH is a non-volatile computer storage technology that can be electrically erased and reprogrammed. Since flash memory is non-volatile, no power is needed to maintain the information stored in the chip.

1.4. MEMORY ORGANIZATION

Figure 1.3 illustrates how a memory system is organized. Random-access architecture is the name given to this structure. The ability to access memory addresses in constant time and in a random order, regardless of the actual location for reading or writing, is the source of the name. In the storage array or core, the basic cell circuits are arranged so that they share connections in horizontal rows and columns. Word lines are the horizontal lines that are only driven from the external storage array, whereas bit lines are the vertical lines that carry data as it enters and exits the cells. A cell's specifically chosen row and column can be read or written to. Either "0" or "1" can be stored in each cell. Depending on the operation, memories can simultaneously select 4, 8, 16, 32, or 64 columns per row. The specific rows and columns are identified by decoding the dual address data [5].

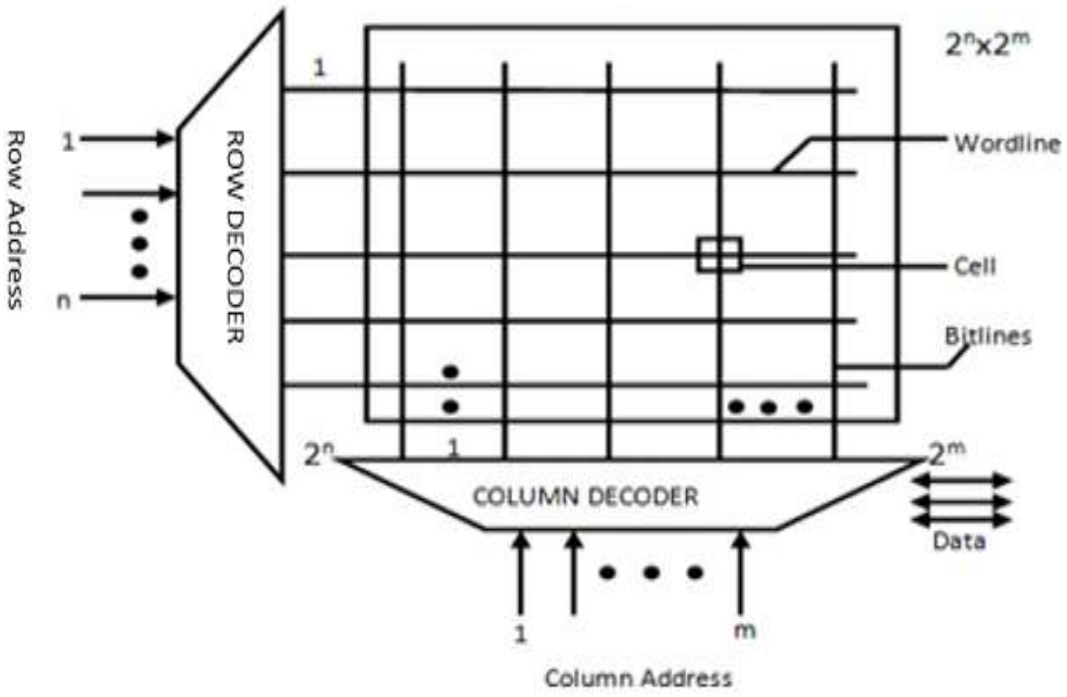


Figure 1.3. Organization of memory system [5].

Read-Write Random-Access Memory (RAM) is the term for the data that is stored in flip-flop circuits or, more simply, as charge on capacitors. Due to its volatility, the reading or writing data experiences roughly the same latency. Because read-write memories store data in an active circuit, they lose their stored data in the event of a power failure. Because Read-Write Random-Access Memory is often referred to as RAM, it would make sense for Read-Write Memory to be abbreviated as RWM. The two most popular kinds of RAMs are dynamic RAM (DRAM) and static RAM (SRAM). The static RAM stores the stored value in flip-flop circuits when the power is on. SRAMs are typically high-speed memory for clock cycles between 5 and 50 ns. The values on the capacitor are stored in dynamic RAM. Compared to SRAMs, they are slower and more susceptible to leakage and noise issues. While SRAMs have roughly a quarter of the density of DRAM in a given technology generation, DRAMs can pack significantly more memory into the same area. This arrangement is also used by ROMs, which have read speeds similar to those of read-write memories (see figure 1.3). Although each ROM writes data in a unique way, they are all non-volatile. Since the most basic type of ROM is programmed during manufacturing by creating physical patterns on the chip, it is difficult to make modifications to the stored data later

on with mask-programmed ROMs. In order to demonstrate the distinction, programmable read-only memory (PROM) is constructed with a data channel between each row and column that stores "1" in each data location. Storage cells are primarily switched to the "0" state when manufacture is complete, and "0" cannot be written as "1" once it has been programmed or blown, thanks to the provision of suitable electrical pulses that selectively open the row-column data channels. Similar to PROMs, Erasable Programmable Read-Only Memories (EPROMs) are electrically programmed, but exposure to ultraviolet (UV) light has the potential to erase all of the data. All of their bits are initially in a single binary state. To allow UV light to reach the packages, these parts feature a clear window over the chip. The most sophisticated and costly types of PROMs are Electrically Erasable Programmable Read-Only Memories (EEPROMs). Electrical methods can also be used to write and erase them. In contrast to EPROMs, E^2PROMs can be overwritten to alter even a single bit and can be completely or selectively deleted. Since all PROMs are able to keep data even when the power is turned off, they are referred to as non-volatile. The processes of writing and erasing data for all types require time intervals that can range from microseconds to milliseconds. The more modern version of EPROM and E^2PROM is called flash memory. The memory blocks in flash memory can be wiped out all at once. The hot electron effect, which is produced by applying a strong field in the channel region, is used to write data in the EPROM form's flash memory. These electrons then penetrate the oxide region and boost the device's threshold voltage. In contrast, the data in E^2PROM flash is written using Fowler Nordheim (FN) tunnelling, where a device with a higher threshold voltage represents a stored "1" while one with a lower threshold voltage signifies a stored "0" This storage mechanism involves electron tunneling through a thin insulating layer such as a gate-connected thin oxide allowing current to pass by overcoming the energy barrier. Memories like FRAM (or FeRAM) utilize ferroelectric materials and can retain data even after power is removed. These memory cells are built using perovskite crystals, which can be polarized in either direction to store information. This creates a non-volatile memory structure, as the polarization remains intact without power. Despite the availability of alternative memory technologies, semiconductor memories remain the preferred choice in VLSI design, offering superior performance in terms of cost, speed, energy efficiency, and compactness.

1.5. MOTIVATION AND OBJECTIVES

1.5.1 Low-power and High-speed SRAM Cell

Their research introduced an effective, stable cell selection method to identify SRAM cells that exhibit strong bias, resistance to circuit noise, and resilience to voltage, temperature fluctuations, and aging. Despite these advancements, the study concluded that additional endeavors are required to achieve more promising outcomes.

1. To solve the issue of SRAM stability and delay, a novel Swing Restoration Inverter (SRI) circuit is developed and implemented utilizing the proposed 8T SRAM cell.
2. A Swing restoration Inverter (SRI) is used to improve the cell's stability during read and write operations.
3. By adding two more transistors, the leakage power is minimized by increasing the node voltages and decreasing the threshold voltages.
4. As a result of the recommended enhancement, SRAM's stability and latency have improved.

1.5.2 Improved Stability of SRAM Cell

There were a number of approaches because early electronic systems were extremely slow due to memory speed not being proportional to CPU performance. Therefore, the cache memory is employed to increase the system's overall speed. At the moment, static random-access memory (SRAM) serves as the foundation for the cache memory. However, the technique's reduction in cell supply voltage disrupts the stored node voltage, which causes data loss during read, write, and hold operations. By raising the word-line voltage in the enhanced word-line write assist technique [18], access transistors' gate to source voltage rises as well, increasing static power dissipation. As a result, low-voltage operation is likewise not appropriate for this approach. Furthermore, S. Kamineni and B. H. Calhoun [21] introduced techniques aimed at minimizing static power dissipation and enhancing the efficiency of read/write operations.

1. To improve the stability of the SRAM cell for low power and high speed.
2. To design an 8T SRAM cell for improved read and write margins.
3. Analyze the proposed 8T SRAM cell and validate it against the conventional 6T SRAM cell.

1.5.3 Low-leakage and High-stability of SRAM Cell

The world's technology has been rapidly moving toward the nano regime as consumers' demands for improved electronic device performance are also growing. Consumers want affordable, high-performing gadgets. On-chip circuits have become essential in all areas

of technology, including wireless sensors, the internet, and portable handheld gadgets [22]. On-chip memories play a crucial role in high-performance applications, as the superior speed of SRAM renders it particularly well-suited for such purposes [23]. SRAM memory faces significant challenges, including high leakage power and operational instability, which have been exacerbated by the continued downscaling of process technology [24]. However, to decrease power consumption, the supply voltage was lowered, which in turn caused a proportional decrease in the threshold voltage of the devices. However, this lower threshold voltage results in an exponential rise in subthreshold leakage current. Since the SRAM cell must be able to store its data in all read and hold scenarios, stability is the most crucial design criterion [25]. Data loss could occur if the SRAM cell is not stable. The lowest noise voltage values that can potentially push the cell into an undesirable state during a hold or a read operation, respectively, are known as these static noise margins [26]. By taking into account the static voltage transfer characteristics (VTCs) of the two inverters that comprise the cross-coupled pair, it is possible to examine the stability of the SRAM cell during a hold operation [27]. However, the results obtained are not promising.

1. To address stability and delay difficulties in SRAM, a unique negative bit-line (NBL) circuit is proposed, then put into action using an 8T SRAM cell.
2. In the recommended architecture, one of the bit lines produces a negative voltage during the write operation (due to the NBL circuit), which enhances the access transistors' driving capacity and, as a result, the writing ability.
3. To increase the cell's stability during read operation, a separate or isolated read port is employed.
4. As a consequence, the suggested improvement has improved SRAM's stability and decreased its latency.

Objectives

The growing demand for low-power and high-speed memory with low leakage the need for re-designing memory and its peripheral components for performance enhancement. Also, the cumulative aftermath of a reduction in technology node, scaling V_{DD}, and increased process variation may result in augmented memory failure. Thus, the following three objectives were formulated to improve the performance of SRAM.

Objective 1: To design SRAM Cell for low power and High speed.

Objective 2: To develop an improved stability of low power SRAM cell.

Objective 3: To develop a low-leakage SRAM cell.

1.6. THESIS ORGANIZATION

The organization of the thesis is presented in this section, which comprises seven chapters listed below:

Chapter 1 is **Introduction and Motivation:** The simplest and most crucial component for memory is the SRAM cell. The 6T SRAM cell was the industry standard for a very long duration, but its performance deteriorates with the decreasing technology node and scaling V_{DD}. The literature review has helped identify the proposed 8T SRAM cell as a potential successor, as it has low power and high speed.

Chapter 2 Literature Review: The literature survey forms a key part of this review, providing detailed insights into current techniques and research developments. In particular, the review of SRAM cells focuses on three critical aspects: stability, energy efficiency, and power constraints.

Chapter 3 deals with the **Low power SRAM Cell using Swing Restoration Inverter (SRI)** for low-power applications. In this chapter, proposed 8T SRAM cell is proposed, and its performance is analyzed. The proposed cell is based on a swing restoration inverter (SRI), dual-port in nature. This particular configuration is chosen for its low power and high speed.

Chapter 4 details the **Improved stability of low power SRAM cell.** The cell stability analysis of the sensitivity of the memory cell using Low Power VLSI. The stability of a Static Random access memory cell in the presence of DC noise is measured by the static noise margin (SNM). Static Noise Margin is the amount of voltage noise required at the output nodes to flip the state of the cell. This can be obtained using the voltage transfer characteristic (VTC) of the two cross-coupled inverters of the SRAM cell.

Chapter 5 In this chapter the **Low-leakage, High-stability SRAM cell for IoT Applications.** The design and characterization of a low-leakage, high-stability SRAM cell for IoT applications is crucial for the development of portable electronic devices. This study proposes a negative bit-line (NBL) write assist circuit and a separate (isolated) read port to improve the write and read stability of the SRAM cell, respectively. The proposed design has been compared to previous state-of-the-art work, and it has been shown that the WSNM has improved significantly, while the write latency has decreased and faster operation.

Chapter 6 In this chapter the **Energy Efficient SRAM Cell.** An energy efficient 8T SRAM cell is also proposed to ensure easy integration for the components of SRAM. Therefore, for performance energy efficient SRAM cell configuration is also proposed mechanisms to lower power consumption and high speed. While ensuring that the designed proposed 8T SRAM cell for low leakage.

Finally, **Chapter 7 Conclusions and future scope**: SRAM is an essential component for microprocessors. The decreasing technology node and increasing demand for portable devices with longer battery life has generated the need for re-designing SRAM for performance enhancement. Thus, in this thesis double ended, dual port bit cell designs are proposed, that have the ability to achieve the same. Also, a new concept for a dual mode operational cell and its functioning is also explained. Thereafter, for performance energy efficient SRAM cell configuration is also proposed.

The chapters are followed by the references and list of publications. All the books and papers that were referred to during the study to form the basis for this work are listed in the reference section. While all the papers published for the completion of this work are listed in – List of Publications.

CHAPTER 2

LITERATURE REVIEW

Memory has been the center of attention for performance enhancement for a very long time. Researchers have proposed various techniques and designs for improving the performance of single or multiple components of memory. SRAM cells are designed to have received special attention from researchers, as the bit cell is the heart of SRAM. Attempts have also been made to modify sense amplifier designs for better compatibility. While array configuration optimization is a fairly recent domain. Thus, a detailed review of pre-existing designs, configurations, and topologies is essential to understand the different challenges that need to be overcome while designing a new proposed and improved cell, sense amplifier, and array for performance enhancement. Thus, in this chapter, a detailed review of the different memory cells, technology, and a summary and observations are presented.

"Literature review on SRAM cells under Stability, Energy, and Power Constraints."

The chapter is divided into six different sections, starting with an introduction to the processor, Section 2.1. It is followed by section 2.2, literature survey. This section helps identify the definition of research questions and conduct a search. Thus, the next section 2.3 reviews of different SRAM cell designs, their characterization based on technique and technology, and performance analysis. Further in section 2.4, a summary of the research review based on the literature review, and their performance is commented upon. While in section 2.5, research gaps based on different approaches for array implementations are explained. Finally, based on the research gaps, the identified research objectives are elaborated upon in Section 2.6.

2.1. INTRODUCTION TO THE PROCESSOR

The key feature of a microprocessor is its multi-core architecture and fast operation. The optimal functioning of a processor is reliant on the performance of the internal memory. This internal memory for the processor is formed by a matrix of SRAM cells. Consequently, improving the performance metric for an SRAM cell improves the performance of the memory array. The overall power consumption for a cell is the sum

of its static and dynamic power components; the charging and discharging event accounts for 60% of the latter component. Therefore, limiting the charging/discharging event for a cell reduces its dynamic power consumption. Consequently, to reduce switching power consumption, double-ended cell topologies are gaining popularity. Various other researchers have also reported other SRAM cell configurations to rectify the abovementioned problems. Therefore, in this chapter, a detailed review of different SRAM cells, technologies, and a summary and observations are presented to understand the different topologies and techniques reported over time to improve the performance of each SRAM cell. It is essential to develop a deep understanding of the different techniques to design and develop new proposed SRAM cells to improve performance.

2.2. LITERATURE SURVEY

The literature survey is one of the main focuses of the literature review. It also provides detailed information about current area techniques. The survey is divided into the following sections.

2.2.1 Definition of the Research Questions

In this step, this study formulates the Research Questions (RQs) that will guide our work.

RQ1: What are the various designs for stability analysis of low-power SRAM cells?

RQ2: What are the different low-power SRAM architectures?

RQ3: What are the various designs for energy and power-efficient SRAM cells?

RQ4: What are the various parameters for SRAM cell analysis?

2.2.2 Conduct Search

The objective of searching is to find the journal and conference papers that investigated the low-power SRAM cells. The search is normally based on some keywords. The keywords used in this study to search for research articles are listed below: Low power SRAM, static noise margin (SNM), swing restoration inverter (SRI), leakage power, energy-efficient, and power consumption

2.2.3 Screening of Papers

To ensure that all the papers included in the review were clearly related to the research questions, detailed inclusion and exclusion criteria were defined. Table 2.1 describes the inclusion and exclusion criteria chosen for our research.

Table 2.1: Inclusion and Exclusion Criteria

Criteria for Inclusion	Criteria for Exclusion
Studies that focus on the improved stability of SRAM cells	Studies not in English
Studies focusing on various approaches for energy-efficient, leakage power, and stability analysis	Studies not related to any of the research questions
Studies that conduct High-performance SRAM Cell analysis of their research	Studies whose findings are unclear and ambiguous

2.3. REVIEW OF DIFFERENT SRAM CELLS DESIGNS

Several methods have been proposed for improved stability and energy efficiency for SRAMs in the present low-power analysis. Below is a summary of the work done on SRAMs that are more stable and energy-efficient. Noted that traditional static random-access memory (SRAM) cells often experience internal data instability because the read operations involve direct access to the data storage nodes. Memory cell noise margins in scaled CMOS technologies decrease with increasing power supply voltage and variability. This work presents memory architectures featuring six, seven, eight, and nine transistors, and evaluates them based on key parameters such as area, data stability, write voltage margin, access speed, active power usage, idle leakage current, and minimum operating voltage. To compare these memory cells, a comprehensive electrical performance metric is employed, which considers both manufacturing variations and supply voltage fluctuations. Triple-threshold-voltage 8T and 9T SRAM cells demonstrate up to 2.5 times lower data stability but offer 765.9 times better overall electrical performance than conventional 6T SRAM cells when implemented using TSMC 65 nm CMOS technology [28].

This study proposes a gated ground SRAM design based on a seven-transistor (7T) bit-cell. Under varying process, voltage, and temperature (PVT) conditions, the proposed cell shows superior data stability and yield in comparison to the conventional 6T cell. A single-ended sensing amplifier is also presented for reading from the proposed cell, and a novel write mechanism is employed to reduce write power to less than half that of the 6T cell. The proposed cell is designed and simulated to use a similar silicon area and

leakage power to the 6T cell using a commercial 65 nm CMOS technology. Ground gating is achieved by selectively controlling the column virtual ground (CVG) of consecutively accessed words. By adopting multiple words per row and significantly reducing leakage power consumption, the design minimizes multi-bit data upsets caused by radiation-induced single-event disturbances or soft errors. Additionally, because of its intrinsic 30% greater soft error critical charge, the recommended cell's soft error rate (SER) is less than half that of the 6T cell [29]. According to [30], speed, power consumption, and area are among the key considerations in modern memory design, especially as this study advances toward deep sub-micron technologies; the problems of leakage current, noise, and cell stability caused by changes in physical characteristics become more apparent. In this work, an 8T read-decoupled dual-port SRAM cell with dual threshold voltage was built, and its leakage current, data retention voltage, read-write delay, and read-write noise margins were all assessed. Through read decoupling, dual-Vt transistors are used to boost the read noise margin and decrease static power dissipation. The results show the benefit of the proposed design in comparison to existing 6T, 8T, and 9T SRAM Cells. The cell in TSPICE is designed and simulated using 90 nm CMOS technology. The reduction of leakage current and data retention are two of the primary problems with modern CMOS technology. In this study, 6T, 8T, and 9T SRAM cells' read and write latency, read and write margins, data retention voltage (DRV), layout, and parasitic capacitance are compared. Through statistical simulation of the noise margin and corner analysis, the effects of intrinsic parameter modifications have been investigated. When compared to 6T SRAM cells, 8T and 9T SRAM cells have a greater read noise margin (about four times the RSNM). The 9T SRAM cell offers greater write stability despite being around 1.35 times larger than the 8T SRAM cell. The 8T SRAM cell's write stability is significantly impacted by single-ended bit line sensing. The write '1' noise margin of the 8T SRAM cell is nearly three times lower than that of the 9T SRAM cell. The data retention voltages for the 8T, 9T, and 6T SRAM cells are 93.64 mV, 84.5 mV, and 252.3 mV, respectively. In terms of read delay, the 9T SRAM cell shows a delay of 98.85 ps, compared to 72.82 ps for the 6T cell and 77.72 ps for the 8T cell. The higher read delay is caused by dual threshold voltage technology, which was employed in the 9T SRAM cell to reduce the leakage current. The write delay was 10 ps for 9T SRAM cells, 45.47 ps for 8T SRAM cells, and 8.97 ps for 6T SRAM cells. The simulation was conducted at 90 nm with CMOS technology [31]. Leakage power constitutes a significant portion of the total active power, particularly in scaled-down

CMOS technologies. It is estimated that 20–50% of the average power loss during normal operation is caused by leakage. This issue is even more critical for mobile devices, where battery life and precise timing are essential. This study introduces a low-leakage SRAM cell and array architecture aimed at delivering high performance with low power consumption for embedded memory applications. Compared to the traditional 6-transistor (6T) SRAM cell, the proposed revolutionary 7-transistor (7T) based memory offers 50% less leakage power and 30% faster access time. Additionally, its area is 20% greater than that of the small 6T cell. All comparisons are based on low-power process technologies from 28 nm foundries [32]. This study provides a low-power SRAM design with a quiet-bit line architecture by integrating two important methodologies. First, to prevent excessive full-swing charging of the bit lines, the authors initially use a single-ended driving approach for the write operation. Second, to maintain constant low voltages for all bit lines, they employ a pre-charge free pulling method for the read operation. An important 84.4% power reduction over a self-designed baseline low-power SRAM macro can result from such an architecture, according to SPICE simulation on a 2K-bit SRAM macro [33]. In order to overcome the inherent read stability and write margin trade-off and scaling functional restrictions, large-scale 6T SRAM beyond 65 nm will increasingly rely on assist technologies. Improved read or write margin has been the main goal of circuit assistance techniques, with little consideration paid to performance issues. In this study, they demonstrate the direct effects on voltage-sensitive yield and present margin sensitivity and delay analysis tools for evaluating the functional efficiency of bias-based assist approaches. A margin and delay analysis demonstrates how bias-based circuit assistance techniques influence functionality, stability, and performance characteristics. A framework is established to evaluate these assistance methods, providing a basic understanding of their underlying mechanisms. The study covers four generations of low-power technologies to illustrate trends and assess the long-term effectiveness of circuit assistance strategies in future low-power bulk technologies [34].

This study proposes a low-power write technique based on charge-sharing. By minimizing the voltage swing on the bit lines, the dynamic power consumption of the bit lines is effectively reduced. The static noise margin (SNM) of the memory cell concept is discussed in order to illustrate its viability. According to simulation data, this SRAM saves more than 20% dynamic power during the write cycle when compared to traditional SRAM [35]. A significant portion of the entire chip is occupied by on-chip cache, which is predicted to grow in advanced technologies. A significant amount of the power used

during a write operation is represented by the capacitance of charging and discharging bit lines. This study provides a brand-new write mechanism that can execute a write operation using just one of the two-bit lines. Consequently, to execute a write operation, the suggested 7T SRAM cell lowers the activity factor of discharging the bit line pair. The write power saving is at least 49%, according to experimental results using the HSPICE simulation. After the cell transistors are precisely sized, both the read delay and the static noise margin are preserved [36]. The proposed design improves gate leakage power consumption while increasing subthreshold leakage compared to the 6T SRAM cell. The recommended 8T SRAM cell has the greater advantage of an improved write margin as compared to the standard 8T SRAM cell [37]. It was also shown that the circuit operates as a two-port SRAM bit cell without changing the basic topology. The proposed bit cell will be used to create a test chip with a functional array in the future [38].

This work proposes a differential 8T SRAM cell that is robust, low-power, and extremely noise-tolerant. Process and voltage variations are examined in connection with read current, hold power, read stability, access delay, and other attributes. Most of the measures show improvements when compared to the other cells. As a result, the proposed cell is a good choice for low-power, high noise tolerance SRAM cells in scaled technology [39]. The majority of the power consumption of today's high-performance chips is now attributed to leakage power dissipation. Leakage power dissipation has emerged as the most challenging issue in VLSI circuits and systems. It also rationally classifies the different leakage minimization techniques. Furthermore, the effect of technology nodes on speed and leakage has been thoroughly investigated using the SPICE tool and a basic complementary metal-oxide-semiconductor (CMOS) gate. It also looks for reliability issues when the process, voltage, and temperature vary. This comprehensive study and the experimental results can be used to determine the most effective way to minimize leakage [40].

A new 8-transistor (8T) static random access memory cell is constructed to improve data stability in subthreshold operation. The proposed single-ended 8T static RAM (SRAM) cell with dynamic feedback management enhances the static noise margin (SNM) for the ultralow power supply. 8T SRAM Cells can be utilized in ultralow power applications because of these features [41]. For most of these devices, memory is an essential component, and the device's size decreases as it gets smaller. Fast and low-power memory architecture is therefore a major consideration. Another critical aspect is the stability of cells in static random-access memory (SRAM). This research integrates multi-threshold

and fingering techniques to present a modified 6T SRAM cell that offers higher speed, enhanced stability, and reduced leakage current during the standby mode of the memory cell [42].

This work suggests a new power-efficient dual-port 8T SRAM bit cell layout. The proposed cell shows a significant improvement in RSNM, HSNM, WSNM, and leakage power compared to the existing designs. The proposed memory cell could be useful for Internet of Things applications that need low voltage and low power [43]. Optimization of SRAM yield using dynamic stability techniques has been evaluated in the past to ensure the continuous scaling of bit cell size and supply voltage at future technology nodes. Despite the release of several dynamic stability metrics, they have not been used in real-world failure analysis or compared to conventional static margins. This work contrasts static and dynamic measurements to identify predicted relationships. The causes of variability and their impact on SRAM stability are identified using a dynamic stability characterization architecture using pulsed word-lines in 45 nm CMOS [44]. As technology develops, leakage power consumption becomes more significant and is now comparable to the dynamic component in high-performance Systems-on-Chip. These developments are significantly more noticeable for memory devices for two main reasons. First, because performance has historically been the primary criterion for memory architectures, they are by nature non-power-efficient. Second, a large amount of time is spent without access to the great majority of memory cells because memories are accessed in brief bursts. This study provides an overview of the approaches proposed in academia and industry to minimize the subthreshold component of leakage power in SRAMs. The choices reviewed include cell-level approaches and architectural solutions suitable for system-level design [45].

This study calculates the average power dissipation for SRAM cell design approaches. Subthreshold operation is used to make SRAM cells suitable for low-power applications by achieving reduced power dissipation. The sleep transistor technique has been determined to have the lowest power dissipation when compared to the conventional 6T-SRAM cell and stack transistor approach. In comparison to the conventional 6T-SRAM and sleep transistor strategies, the stack transistor technique is determined to provide the least amount of delay when it comes to delay measurement. Using the benefits of the minimum average latency of the stack transistor technique and the lowest power consumption of the sleep transistor technique, a new SRAM circuit technology will be devised in the future to enhance overall performance [46]. A fast statistical method is

proposed to analyze the Read SNM in the near/subthreshold region of a 6T SRAM cell. The method is based on the nonlinear behaviour of the cell. Considering DIBL and body effects, a precise closed-form solution for the near/subthreshold SRAM cell's Read Static Noise Margin (SNM) is obtained. This method uses the state space equation to calculate the Read SNM of the cell as a function of the threshold voltage of the cell transistors. This function shows how variations in temperature, size, and threshold voltage impact the Read SNM. It provides a small reliability analysis for a specific cell array size and supply voltage. It also calculates the exact failure probability of the cell using 45 nm for Monte-Carlo simulations. Analytical results are validated using Predictive Technology Models [47]. Since minimal-area SRAM bit-cells are achieved with a cell ratio and pull-up ratio of 1, this study investigates the feasibility of reducing the cell ratio from the standard range of 1.5–2.5:1. Among the various design metrics, read stability is the most significantly affected by a reduction in cell ratio, as shown through an analysis of its impact on area, power, performance, and overall stability. Nevertheless, this effect can be alleviated by employing specific read-aid circuits recommended in the literature [48]. The subthreshold region of SRAM write stability is examined in these studies. The semi-analytical model of write static noise margin (WSNM) for 6T SRAM (subthreshold region) is presented in this work. The write stability of the SRAM is also investigated in the presence of varying size ratios and supply voltage. To verify the write stability of the SRAM cell, process corner analyses are also performed using the model at the worst process corners. This model is the first to evaluate the WSNM using the traditional butterfly static noise margin technique. The model is accurate for all technology nodes, including those at 45 nm, 65 nm, and 130 nm. In addition to 6T SRAM cells, the model is also valid for 8T and 10T SRAM systems [49]. This study proposes two static random-access memory (SRAM) cells that effectively reduce static power dissipation resulting from gate and subthreshold leakage currents. The NMOS pass transistors' gate voltages are lowered by the first cell structure, which also lowers the gate leakage current. By raising the ground level while in the idle (inactive) mode, it lowers the subthreshold leakage current. PMOS pass transistors are used in the second cell configuration to reduce the gate leakage current. Furthermore, this design employs dual-threshold voltage technology combined with forward body biasing to reduce subthreshold leakage while maintaining performance [50]. Increasing the noise margin is one of the main challenges in any cutting-edge SRAM design. Achieving a high yield in low-voltage SRAM requires stable bit cell operation due to process factors, including supply voltage changes and

threshold voltage variations in scaled technologies. The proposed architecture improves read stability through a softened read technique that isolates the SRAM cell nodes from the bit-line. It also enhances write capability by dynamically disabling the feedback loop of the inverter pair. The introduced 8T SRAM cell employs a single bit-line for both read and write operations, achieving a 50% reduction in power consumption during bit-line pre-charging and discharging relative to a conventional 6T SRAM cell [51]. An 8T SRAM cell with a dynamic column-based power supply is shown in this work. It makes several comparisons between the proposed SRAM cell and the conventional 6T SRAM cell. To validate the read stability and write ability investigation, this study uses the N-curve measure. The proposed 8T SRAM cell performed better than the conventional 6T SRAM in terms of read stability, read current, and leakage current in 45 nm technology, according to simulation findings using the Cadence Virtuoso tool [52]. In this study, this study analyzes the read stability is analyzed using the N-curve metric and compared with the well-known Static Noise Margin (SNM) introduced by Seevinck. Additionally, new write-ability metrics derived from the same N-curve are evaluated against the conventional write trip point definition. Analytical models have been developed for each of these parameters. It is demonstrated that the new measures provide more up-to-date information, making it possible to build a cell that is more durable and stable. With this additional insight, scaling is no longer seen as a limiting factor for the cell's read stability. Ultimately, these metrics are used to examine the effect of intra-die variability on cell stability through a statistically-aware circuit optimization method, and the outcomes are compared with those from traditional worst-case or corner-based design approaches [53]. The stability of resistor-load (R-load) and full-CMOS SRAM cells is investigated using both analytical and simulation techniques. An explicit analytical expression for the static-noise margin (SNM) as a function of supply voltage and device parameters is provided. Moreover, full-CMOS cells are substantially more stable than R-load cells at low supply voltage [54]. This work suggests a pre-charged local bit-line sharing (PCLBS) static random-access memory (SRAM) for near-threshold operation. In earlier local bit-line sharing SRAM designs, such as conventional 8T and full-swing local bit-line (FSLB) SRAMs, multiple bit-cells share a local bit-line pair with moderate capacitance to ensure high read stability. However, the conventional 8T SRAM experiences significant latency because the local bit-line cannot be fully developed. Although the FSLB SRAM reduces the delay, it requires a temporal constraint of control signals to achieve a sufficient read sensing margin. The proposed PCLBS SRAM achieves a high read speed by fully

developing the local bit-line pair without any temporal limits. Furthermore, the proposed PCLBS SRAM enhances read stability and write capability by using transmission gates in write routes and a pre-charged local bit-line scheme, respectively [55]. The largest power user in an SRAM array is pre-charging or voltage switching on bit-lines during read or write operations. In the study, a bit-line charge cycling-based read-and-write assist circuit for static random-access memory is demonstrated. With the help of the assist circuit, the BL charges that are wasted in a conventional design are recycled for BLs' pre-charging in the subsequent period [56].

This article proposes the use of a cross-coupled bit line (BL) biasing technique to preserve the fast access speed of SRAM without excessively increasing the size of the SRAM cell and to minimize read-access failures in the presence of Vt variation. This study has shown that the proposed method reduces the cell area by 6.5% compared to the conventional BL biasing solutions previously investigated in this study using 22 nm predictive CMOS models and extensive Monte Carlo simulations [57]. The previously proposed average-8T static random-access memory (SRAM) has a competitive area and does not require a write-back mechanism. In the case of an average-8T SRAM architecture, a full-swing local bit line (BL) connected to the gate of the read buffer can be created using a boosted word line (WL) voltage. However, in the case of an average-8T SRAM based on current technology, such as a 22 nm FinFET technology, where the threshold voltage varies substantially, the higher WL voltage cannot be used because it decreases the read stability of the SRAM. The inability to drive the read buffer's gate with the full supply voltage (VDD) and the inability to generate a full-swing local BL lead to a considerable read delay. To overcome the aforementioned limitation, this study suggests a differential SRAM design with a full-swing local BL. By employing cross-coupled PMOS to guarantee full swing of the local BL and a full VDD to drive the read buffer's gate, the proposed SRAM architecture does away with the need for the boosted WL voltage. For various configurations of the proposed SRAM architecture, which stores multiple bits, the lowest working voltage and area per bit are investigated. The proposed SRAM that stores four bits in a single block can achieve a minimum voltage of 0.42 V and a read delay that is 62.6 times lower than the average-8T SRAM based on the 22-nm FinFET technology [58].

This study describes the design of a new low-power 11T SRAM cell. This proposed solution employs two voltage sources, one connected to the bit line and the other to the bit bar line, to prevent the swing voltage at the output nodes of the bit and bit bar lines.

When the SRAM cell is operational, the dynamic power dissipation is reduced by reducing the swing voltage. The self-controllable voltage level method reduces leakage current when the transistors transition from sleep to active and vice versa by employing NMOS transistors as resistors coupled in series with PMOS transistors acting as switches. A reduction in leakage current results in a decrease in static power dissipation. To avoid problems with data retention, the circuit receives a reduced voltage in the standby state and its maximum voltage in the active mode. The Synopsys EDA tool in 30 nm CMOS technology has been used to simulate the power dissipation, latency, transistor utilization, power delay product, and energy-delay product of the proposed 11T SRAM cell and other current models of SRAM cells [59].

In this study, the authors create a novel static random-access memory (SRAM) based on the adiabatic logic principle. To reduce energy dissipation, the proposed adiabatic SRAM is driven by two trapezoidal-wave pulses. The cell construction of the proposed SRAM consists of two high-value resistors based on a p-type NMOS transistor, a cross-coupled n-type metal-oxide-semiconductor (NMOS) pair, and an NMOS switch to reduce the short-circuit current. The addition of a transmission gate controlled by a write word line signal allows the proposed circuit to operate as an adiabatic SRAM during data writing. Simulation findings show that the proposed SRAM uses less energy than a conventional adiabatic SRAM [60]. To maximize the read and write performance of 8T SRAM cells, which are better than 6T SRAM cells, swing restoration dual node voltage is the main focus of static random-access memory (SRAM) design and study. the amount of time spent writing and reading, and improve stability. A PMOS transistor with a smaller width uses less power. This research uses the Cadence Virtuoso schematics tool to compare 6T and 8T SRAM cells for 180 nm technology [61].

The following discussion makes it evident that extensive research has been conducted and continues in the field of low-power SRAMs. Besides reducing power dissipation, it is essential to maintain acceptable performance metrics. In light of this, a literature review has been performed to identify a memory cell design that is both simple and power-efficient while delivering satisfactory performance.

2.4. SUMMARY OF RESEARCH REVIEW

Based on the literature review, a summary of all research articles is given below in Table 2.2. It includes the name of the technique, technology, summary, and observation.

Table 2.2: Summary of Research Review

TITLE AND AUTHORS	PUBLISHER AND YEARS	TECHNOLOGY	SUMMARY AND OBSERVATION
8T-SRAM Cell with Improved Read and Write Margins in 65 nm CMOS Technology, F. Moradi et al. [37].	IFIP International Federation for Information Processing, 2015	65 nm CMOS TSMC technology	Enhances subthreshold leakage while reducing gate leakage power consumption compared to the 6T-SRAM cell. Compared to the conventional 8T-SRAM cell, the suggested 8T-SRAM cell offers the superior benefit of an enhanced write margin. **Limitation:** The finding of this study increases the sub-threshold leakage.
A 40-nm Sub-Threshold 5T SRAM Bit Cell with Improved Read and Write Stability, A. Teman, and A. Fish et al. [38].	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, 2012	40 nm commercial CMOS process	The 5T bit cell was demonstrated to function asymmetrically, providing a low-leakage state that was 5 times superior to a typical implementation at the same operating voltage. Without altering the fundamental topology, it was also demonstrated that the circuit functions as a two-port SRAM bit cell. **Limitation:** There may be some possible SRAM Cell Symmetric operation.
Variation Tolerant Differential 8T SRAM Cell for Ultralow Power Applications, S. Pal, and A. Islam [39].	IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015	16 nm technology	This study proposes a differential 8T SRAM cell that is robust, low-power, and extremely noise-tolerant. an analysis of the effects of process and voltage variations on many metrics, including access delay, read current, hold power, and read stability. Most of the measures show improvements when compared to the other cells. Thus, the suggested cell is a good option for high noise tolerance, low

			power SRAM cells in scaled technology. **Limitation:** This research finds the Tail Transistor of the stacking effect on hold operation.
Review of Circuit Level Leakage Minimization Techniques in CMOS VLSI Circuits, R. Lorenzo & S. Chaudhury [40].	IETE Technical Review, 2016	NA	The majority of the power consumption of today's high-performance chips is now attributed to leaky power dissipation. Leakage power dissipation has emerged as the most challenging issue in VLSI circuits and systems. It also rationally classifies the different leakage minimization techniques. It also looks for reliability issues when the process, voltage, and temperature vary. With the help of this comprehensive analysis and the testing results, the most effective strategy for minimizing leakage may be chosen. **Limitation:** There may be possible Increases in circuit delay, data retention problems, and the need for extra transistors.
A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell, C. B. Kushwaha and S. K. Vishvakarma, [41].	IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2015	NA	A new 8-transistor (8T) static random access memory cell is constructed to improve data stability in subthreshold operation. The proposed single-ended 8T static RAM (SRAM) cell with dynamic feedback management enhances the static noise margin (SNM) for ultralow power supply. **Limitation**: The chip area is increased, and these features enable ultralow power applications of 8T

			SRAM Cell.
A Novel Approach to Design SRAM Cells for Low Leakage and Improved Stability, T. Tripathi, D. S. Chauhan, and S. K. Singh [42].	MDPI, 2018	UMC 55 nm technology	For most of these devices, memory is an essential component, and the device's size decreases as it gets smaller. Fast and low-power memory architecture is therefore a major consideration. This work recommends a modified 6T SRAM cell with high speed, better stability, and reduced leakage current in the memory cell's standby state by integrating multi-threshold and fingering techniques. **Limitation:** The leakage power in stand-by mode becomes a critical concern for researchers.
Low Leakage SRAM Cell with Improved Stability for IoT Applications, C. Duari, S. Birla [43].	Elsevier, 2020	32 nm technology	This study suggests a new power-efficient dual-port 8T SRAM bit cell layout. The proposed cell shows a significant improvement in RSNM, HSNM, WSNM, and leakage power compared to the existing designs. The proposed memory cell may be useful for Internet of Things applications that need low voltage and low power. **Limitation:** As with the majority of studies Read-disturb problem occurs in the SRAM Cell.
Characterization of Dynamic SRAM Stability in 45 nm CMOS,	IEEE JOURNAL OF SOLID-STATE CIRCUITS,	45 nm CMOS	This study, the continuous scaling of bit cell size and supply voltage at upcoming technology nodes, and optimization of SRAM yield utilizing dynamic stability measures, has

S. O. Toh, Z. Guo, and Borivoje [44].	NOVEMBER 2011		previously been assessed. Although a number of dynamic stability metrics have been put out, they have not been compared to traditional static margins or utilized in real-world failure analysis. **Limitation:** There may be occur Critical write ability that magnifies the impact of process-induced and temporal variability in transistor characteristics, compared to static write margins.
Design Techniques and Architectures for Low-Leakage SRAMs, A. Calimera, A. Macii, E. Macii, and M. Poncino [45].	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, 2012	65 nm or 90 nm	Leakage power consumption is now on par with the dynamic component in high-performance Systems-on-Chip, and its importance grows as technology advances. First, memories have traditionally been designed prioritizing performance, making them inherently inefficient in terms of power. Second, memories are accessed in small portions, leaving the majority of memory cells unused for most of the time. **Limitation:** It is subject to more power consumption in SRAM Cell design.
Analysis of SRAM Cell Designs for Low-Power Applications, C. K. Sharma, R. Chandel [46].	International Conference for Convergence of Technology, 2014	90 nm, 45 nm, and 32 nm technology	This study calculates the average power dissipation for SRAM cell design approaches. Subthreshold operation is used to make SRAM cells suitable for low-power applications by achieving reduced power dissipation. **Limitation:** Due to the smallest

			average delay, of stack transistor technique shall be used to design a new SRAM circuit technique to enhance the overall performance.
Statistical Analysis of Read Static Noise Margin for Near/Sub-Threshold SRAM Cell, R. Saeidi, M. Sharifkhani, and K. Hajsadeghi [47].	IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, DECEMBER 2014	45 nm Technology	A fast statistical method is proposed to analyze the Read SNM in the near/subthreshold region of a 6T SRAM cell. Considering DIBL and body effects, a precise closed-form solution for the near/subthreshold SRAM cell's Read Static Noise Margin (SNM) is obtained. It provides a small reliability analysis for a specific cell array size and supply voltage. It also calculates the exact failure probability of the cell. **Limitation:** The study focused on the failure probability of the SRAM cell.
A 65-nm Reliable 6T CMOS SRAM Cell with Minimum Size Transistors G. Torrens et al. [48].	IEEE Transactions on Emerging Topics in Computing, 2017	65 nm CMOS technology	Since minimum area SRAM bit-cells are achieved with a cell ratio and pull-up ratio of 1, this study investigates the possibility of lowering the cell ratio from the usual values, which vary from 1.5 to 2.5:1. Read stability is the parameter most affected by this choice, according to an analysis of its effects on area, power performance, and stability. However, this impact can be mitigated through the implementation of specific read-aid circuits proposed in the literature Limitation: A failure to write occurs when the pass transistor is not strong enough to overcome the cell pull-up PMOS transistor.

Compact Analytical Model to Extract Write Static Noise Margin (WSNM) for SRAM Cell at 45-nm and 65-nm Nodes, Ruchi and S. Dasgupta [49].	IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, FEBRUARY 2018	UMC 130 nm technology	This work presents the semi-analytical model of write static noise margin (WSNM) for 6T SRAM (subthreshold region). Additionally, the write stability of the SRAM is examined when different size ratios and supply voltages are present. Using the model at the worst process corners, process corner analyses are also carried out to confirm the write stability of the SRAM cell. This model is the first to use the conventional butterfly static noise margin approach to evaluate the WSNM. **Limitations:** This study could be addressed in the Process Corner analysis of the SRAM Cell.
Design and Analysis of Two Low-Power SRAM Cell Structures, G. Razavipour, A. A. Kusha, and M. Pedram [50].	IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS, OCTOBER 2009	45 nm technology	This study presents two static random-access memory (SRAM) cells that reduce static power dissipation from gate and subthreshold leakage currents. The first cell shape lowers the gate leakage current and lowers the gate voltages of the NMOS pass transistors. The second cell arrangement lowers the gate leakage current by using PMOS pass transistors. Additionally, this structure minimizes subthreshold leakage without compromising performance by utilizing dual threshold voltage technology with forward body biasing.

			Limitation: There may be some possible symmetric SRAM cells.
A Novel Single-Ended 8T SRAM with Improved Noise Margins and Stability, J. Narayan, R. K. Sharma [51].	Proceedings of 2014 RAECS UIET Panjab University Chandigarh, March 2014	Cadence GPDK 90 nm technology	One of the major obstacles in any state-of-the-art SRAM design is increasing the noise margin. Stable bit cell operation is essential to achieving a high yield in low-voltage SRAM because of process variables such as supply voltage variations and threshold voltage variations in scaled technologies. The write and read operations of the proposed 8T SRAM cell are carried out using a single bit-line technique. Comparing this to a traditional 6T SRAM cell, the power dissipation during pre-charging or discharging the bit-line is cut in half. **Limitation:** Reduction in power consumption may be possible in 8T SRAM cells.
CELL STABILITY ANALYSIS OF CONVENTIONAL 6T DYNAMIC 8T SRAM CELL IN 45 nm TECHNOLOGY, K. Dhanumjaya, et al. [52].	International Journal of VLSI Design & Communication Systems (VLSICS), April 2012	45 nm TECHNOLOGY	An 8T SRAM cell with a dynamic column-based power supply is shown in this work. It makes several comparisons between the proposed SRAM cell and the conventional 6T SRAM cell. To validate the read stability and write ability investigation, this study uses the N-curve measure. The proposed 8T SRAM cell performed better than the conventional 6T SRAM in terms of read stability, read current, and leakage current in 45nm technology, according to simulation findings using the Cadence Virtuoso tool.

			Limitation: It may be possible to reduce the Leakage current in a dynamic 8T SRAM cell.
Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies, E. Grossar, et al. [53].	IEEE JOURNAL OF SOLID-STATE CIRCUITS, NOVEMBER 2006	130 nm and 65 nm technology	In this study examine the read stability using the N-curve metric and compare it with the widely used Static Noise Margin (SNM) introduced by Seevinck. Additionally, new write-ability metrics derived from the same N-curve are evaluated against the conventional write trip point definition. Analytical models have been formulated for each of these parameters. **Limitation:** This research, however, is subject to several increasing over-design and hard-to-meet design criteria, making the statistically-aware circuit optimization very promising for SRAM cell designs in future technology nodes.
Static-Noise Margin Analysis of MOS SRAM Cells, E. SEEVINCK, FRANS, J. LIST, AND J. LOHSTROH [54].	IEEE JOURNAL OF SOLID-STATE CIRCUITS, OCTOBER, 1987	NA	The stability of resistor-load (R-load) and full-CMOS SRAM cells is investigated using both analytical and simulation techniques. An explicit analytical expression for the static-noise margin (SNM) as a function of supply voltage and device parameters is provided. Limitation: To maintain reasonable SNM values at a reduced supply voltage.
Pre-Charged Local Bit-Line Sharing SRAM Architecture for	IEEE TRANSACTIONS ON CIRCUITS	22 nm FinFET technology	For near-threshold operation, this study introduces a static random-access memory (SRAM) architecture utilizing pre-charged local bit-line

Near-Threshold Operation, T. W. Oh, H. Jeong, J. Park, and S. Jung, [55].	AND SYSTEMS, OCTOBER 2017		sharing (PCLBS). In earlier SRAM designs with local bit-line sharing, such as conventional 8T and full-swing local bit-line (FSLB) SRAMs, multiple bit-cells share a local bit-line pair with moderate capacitance to maintain good read stability. However, the conventional 8T SRAM suffers from significantly higher latency due to the incomplete development of the local bit-line. It's important to interpret the results of this study within the context of a more complex architectural design.
A low-power SRAM with a charge cycling-based read and write assist scheme H. Zhang, et al. [56].	2020, IEEE	14 nm FinFET	The largest power consumer in an SRAM array is pre-charging or voltage switching on bit-lines during read or write operations. In the study, a bit-line charge cycling-based read-and-write assist circuit for static random-access memory is demonstrated. With the help of the assist circuit, the BL charges that are wasted in a conventional design are recycled for BL pre-charging in the subsequent period. **Limitation:** The NBL Circuit is used to write assist circuits to reduce delay and good writing ability.
Cross-coupled Bit-Line Biasing for 22-nm SRAM, D. Halupka and A. Sheikholeslami	2009, IEEE	22 nm CMOS Technology	In order to reduce read-access failures in the presence of Vt variation and maintain SRAM's rapid access speed without unduly expanding the size of the SRAM cell, this article suggests using a cross-coupled bit line (BL) biasing technique.

[57].			**Limitation:** The combined worst-case BL leakage current is sufficient to trigger the cross-coupled PMOS transistors between PRE-BAR deactivation and WL activation. i.e., Effect on SRAM cell leakage current.
Full-Swing Local Bitline SRAM Architecture Based on the 22-nm FinFET Technology for Low-Voltage Operation, K. Kang, et al. [58].	2015, IEEE	22 nm FinFET Technology	In the case of an average-8T SRAM architecture, a full-swing local bit line (BL) connected to the gate of the read buffer can be created using a boosted word line (WL) voltage. The inability to drive the read buffer's gate with the full supply voltage (V_{DD}) and the inability to generate a full-swing local BL lead to a considerable read delay. By employing cross-coupled pMOSs to guarantee full swing of the local BL and a full V_{DD} to drive the read buffer's gate, the proposed SRAM architecture does away with the need for the boosted WL voltage. **Limitation:** There may be resulting in a considerable read delay in the SRAM Cell.
Low-power self-controllable voltage level and low swing logic-based 11T SRAM cell for high-speed CMOS circuits, K. Gavaskar, U. S. Ragupathy [59].	Analog Integrated Circuits and Signal Processing (2019)	30 nm CMOS technology	This work describes the design of a new low-power 11T SRAM cell. This proposed solution employs two voltage sources, one connected to the bit line and the other to the bit bar line, to prevent the swing voltage at the output nodes of the bit and bit bar lines. When the SRAM cell is operational, the dynamic power dissipation is reduced by reducing the swing voltage. The self-controllable voltage level method reduces leakage

			current when the transistors transition from sleep to active and vice versa by employing NMOS transistors as resistors coupled in series with PMOS transistors acting as switches. A reduction in leakage current is the reason for the fall. **Limitation:** Maybe more transistors are used in SRAM cells, then the area will be increased.
Low-power adiabatic 9T static random-access memory, Y. Takahashi, et al. [60].	The Journal of Engineering, 2014	0.18 µm CMOS process technology	To reduce energy dissipation, the cell construction of the proposed SRAM consists of two high-value resistors based on a p-type NMOS transistor, a cross-coupled n-type metal-oxide-semiconductor (NMOS) pair, and an NMOS switch to reduce the short-circuit current. **Limitation:** This study will attempt to expand the noise margin of the proposed circuit.
A Novel Low Power and Swing Restoration SRAM Logic Circuit Technique, R. M. Rawat [61].	International Journal of Engineering Research & Technology (IJERT), 2018	180 nm Technology	Design and study of SRAM with a focus on optimizing Restoration Swing 8T SRAM cells can read and write data more efficiently than 6T SRAM cells. Less power is used by a PMOS transistor with a narrower width. This study presents a comparative analysis of 6T and 8T SRAM cells. **Limitation:** Analysis of more parameters, like power consumption.

From the following discussion, it is evident that extensive research has been conducted and continues in the field of low-power SRAMs. A key design challenge in SRAM cells is balancing read and write stability. For reliable read operations, a high cell ratio is

required. However, this weakens the access transistors, increasing write access time and reducing write ability. Conversely, lowering the pull-up ratio improves write ability but negatively affects read performance. Another key drawback of previously reported SRAM cells is that they often focus on the improvement of the three hold, read, and write operations. Generally, this improvement in one parameter is attained at the low leakage power of the other.

Based on the detailed review of the different SRAM cells, their configurations, technologies, and array design, the following research gaps are identified. These research gaps form the basis of the research work proposed in this thesis.

2.5. RESEARCH GAPS

1. During the read and write operation in the 6T SRAM cell, there is poor read stability and write ability because of a voltage drop occur at the node voltages. [53], [55-56], [58-59], [61-64].
2. During the write operation in the SRAM cell, the conventional 6T SRAM cell provides a poor write ability because of disturbance in the node voltage that is present at the down-scaled cell supply voltage. [6-12], [42], [61-64].
3. The read disturb problems that SRAM memory has been facing are high leakage power consumption and instability due to continuous downscaling of the process technology. [22-24], [43], [45], [61-64].
4. The memory array is responsible for the consumption of a major amount of power consumed by the chip. [41], [56], [58-64].

2.6. RESEARCH OBJECTIVES

The following are the research objectives

1. To design SRAM Cell for low power and High speed.
2. To develop an improved stability of low power SRAM cell.
3. To develop a low-leakage SRAM cell.

CHAPTER 3

LOW POWER SRAM CELL USING SWING RESTORATION INVERTER (SRI)

The simplest and most crucial component for memory is the SRAM cell. The 6T SRAM cell was the industry standard for a very long duration, but its performance is deteriorating with the decreasing technology node and scaling of V_{DD}. The literature review has helped identify the proposed 8T SRAM cell as a potential successor, as it has low power and high speed. The following objective is framed to accommodate the aforementioned need.

"Design and Analysis of SRAM cell using Swing Restoration Inverter for Low Power Applications."

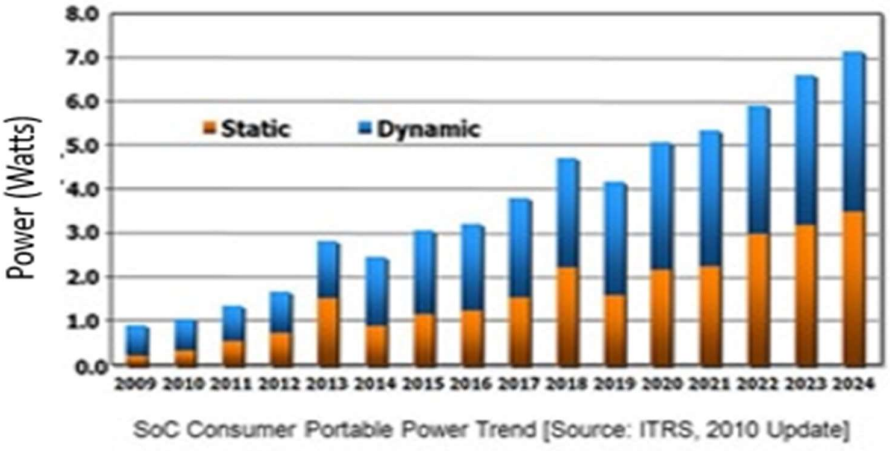
Methodology used to achieve the desired objective in the chapter is as follows –

- To solve the issue of SRAM stability and delay, a novel Swing Restoration Inverter (SRI) circuit is developed and implemented utilizing the proposed 8T SRAM cell.
- A Swing restoration Inverter (SRI) is used to improve the cell's stability during read and write operations.
- By adding two more transistors, the leakage power is minimized by increasing the node voltages and decreasing the threshold voltages.
- As a result of the recommended enhancement, SRAM's stability and latency have improved.

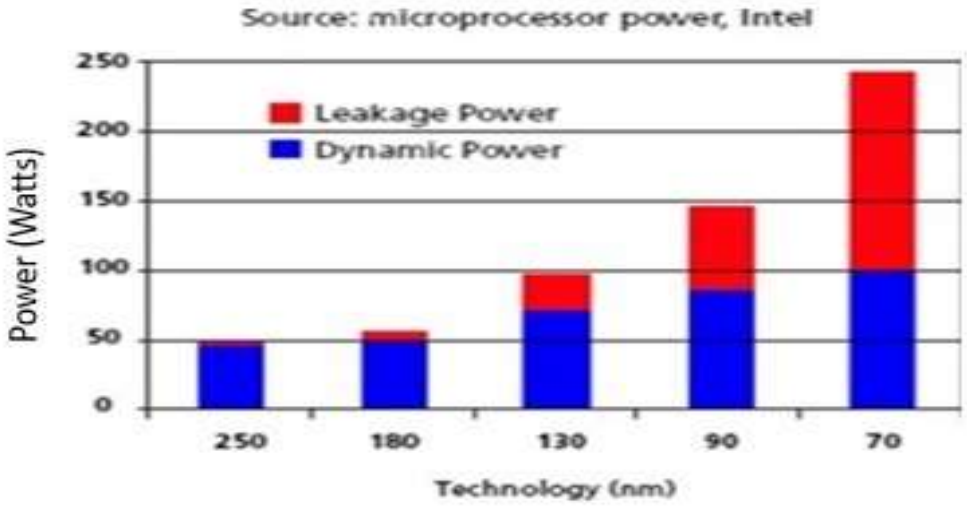
In this chapter, an 8T SRAM cell is proposed, and its performance is analyzed. The proposed cell is based on a swing restoration inverter (SRI), dual-port in nature. This particular configuration is chosen for its low power and high speed. The chapter is organized into the following sections. The first section is dedicated to an introduction to system on chip (SoC), section 3.1. In section 3.2, the swing restoration inverter (SRI) is explained, and its performance is elaborated upon. Thereafter, in section 3.3, the conventional 6T SRAM cell versus the proposed 8T SRAM cell design is compared to identify the best-performing SRAM cell. In section 3.4, the proposed 8T SRAM cell's mode of operation. Whereas, in section 3.5, the improved stability of the best performing proposed 8T SRAM cell is compared against the 6T SRAM cell topologies. In this section 3.6, Results and discussions. Finally, the important findings of the chapter are summarized in section 3.7.

3.1. INTRODUCTION TO SYSTEM ON CHIP (SoC)

In portable and battery-operated devices, System-on-Chip (SoC) technology is often used [65-67]. As functionality, circuit complexity, and density demands rise, a shift to lower technology nodes enables the requisite functionality scaling. Faster and higher-performing gadgets are made possible by technology scaling, but as technology scales down, power efficiency tends to decline [68]. Figure 3.1(a) depicts the power dissipation of a SoC chip in consumer electronics throughout the years (source ITRS). The overall power dissipation of an Intel microprocessor shows a discernible increase, but the growth in static and dynamic power contributions is not directly proportional, as depicted in Figure 3.1(b). The increase in dynamic power consumption is closely tied to the expanding functionality, whereas static power relies on the technology node and circuit layout. Notably, at lower nodes, power distribution is predominantly influenced by static power dissipation. Conversely, at higher nodes, dynamic power dissipation emerges as a substantial element of the overall power dissipation. Static Random Access Memory (SRAM) dominates the chip's physical space in System-on-Chip (SoC) designs, occupying a significant share of the chip area. For example, in a video decoder chip, it encompasses more than 65% of the total space [88], and contributes to over 30% of the overall power consumption in mobile devices [65-67], [68-70]. The use of SRAM in mobile devices introduces increased leakage power due to extended idle periods. The excess leakage power adversely affects battery life, raises cooling and packaging costs, and gives rise to reliability concerns in memory devices. Despite significant advancements in SRAM performance achieved through finer technologies, challenges persist in terms of cell stability and leakage power dissipation, especially in the deep sub-micron regime [69].



(a) Power trend in SoC.



(b) Power consumption in various technology.

Figure 3.1. Evolution of leakage power for (a) Power trend in SoC and (b) Power consumption in various technology [65-70].

Minimizing power dissipation caused by leakage and enhancing the stability of SRAM cells are vital objectives, particularly as semiconductor technology advances into the nanoscale realm. Traditional methods for reducing power consumption in CMOS circuits, such as adjusting supply voltage and scaling devices, have proven effective. It's important to highlight that voltage levels are currently trending towards the 1.0-0.9 V range. This suggests that upcoming progress might not necessarily translate into substantial power reductions. On the other hand, the continual scaling down of MOS transistor dimensions has led to a significant increase in leakage current, posing challenges to maintaining SRAM data stability. Therefore, developing an SRAM cell with minimal leakage and robust stability in the nanoscale domain is a formidable challenge. Various strategies have been proposed in the literature to mitigate leakage power and enhance SRAM cell stability [71-73]. At the circuit level, a multi-threshold CMOS approach [74] introduces two additional transistors, termed sleep transistors, to reduce leakage power in SRAM designs [75-76]. However, it is crucial to note that this method results in increased dynamic power. The super cutoff CMOS technology, designed to limit leakage current in SRAM, requires an additional control circuit [77]. Another technique, transistor stacking, involves replacing a single transistor with two transistors, a practice known as forced stacking [78]. Nevertheless, the introduction of extra latency into the circuits is an inevitable consequence. The LECTOR (LEakage Control TransistOR) system addresses this issue by incorporating two self-controlled leakage control transistors in a line from the supply to ground. This

configuration increases resistance and reduces leakage current without necessitating additional control circuitry [79]. It is crucial to emphasize that the size of the sleep transistor in LECTOR is a critical factor to consider [80]. Recently, there has been a notable advancement in swing restoration techniques, involving the incorporation of two transistors to augment the source voltage. This source biasing strategy has demonstrated superior power efficiency compared to the LECTOR technique across various logic circuits at the 100 nm scale [81]. Importantly, swing restoration has proven effective without necessitating a control circuit. It is imperative to further investigate the applicability of swing restoration methods for larger circuits, such as SRAM, and to explore the impact on dynamic power and method efficiency in deep sub-micron technologies. Reducing leakage power while ensuring optimal stability is crucial for SRAMs. Supportive techniques, particularly when operating at reduced supply voltage, can enhance static noise margin (SNM), specifically read static noise margin (read-stability) and write static noise margin (write-ability) [82]. Established techniques in the literature include cell voltage adjustment [83], modulation of word line voltage [84-85], dual-rail supply schemes [86], negative bit-line schemes [87-88], and gate biasing utilizing FinFET technology [89]. In conclusion, the development of energy-efficient and stable SRAM cells requires a careful examination of various strategies, each with its own trade-offs and inherent challenges. A comprehensive understanding of these approaches is essential for advancing the field and achieving the delicate balance between power efficiency and stability in SRAM design. V_{DD} boosting emerges as a highly effective method for enhancing stability; however, it comes at the cost of increased leakage power. This study outlines a recommended design for a low-power 8T SRAM cell, employing two PMOS transistors. Two connections are established, one to the node voltage Q and the other to Qbar, to eliminate the swing voltage in the bit and bit bar wires. As the cell operates, the swing voltage decreases, leading to reduced dynamic power dissipation. The pre-charge voltage level technique utilizes an NMOS transistor as a resistor and a PMOS transistor as a switch, causing a series of drops in leakage current as the transistors transition between inactive and active states. Comparative analyses demonstrate the consistent outperformance of the proposed 8T SRAM cell over the traditional 6T SRAM cell in read, write, and hold modes. This superiority arises from the increased static noise margins, which ensure improved bit-cell write ability [90], as well as from additional design strategies that reduce static power dissipation while enhancing read and write performance. In [91], a stability analysis based on leakage current is suggested. It

introduces metrics like read current noise margin (RINM) and write current noise margin (WINM) to assess the stability of subthreshold SRAMs. This study introduces a novel 8T compute SRAM (CSRAM) designed for reliable and high-speed in-memory searching and compound logic-in-memory computations [92]. This CSRAM incorporates a pair of pMOS access transistors and split WLs dedicated to computer access. This study presents an approach that eliminates the need for additional margins related to BL voltage swing [93], traditionally required to ensure tolerances against simulation errors and inaccurate estimation of SA offset voltage. This work compares cell stability, noise margins, performance, and power across various dual-V_T design options for a large on-chip cache featuring single-ended, full-swing sensing in a 0.13-µm technology node [94]. It also proposes a method aimed at optimizing a single-bit conventional static random-access memory (SRAM) cell to achieve high stability with low power usage and a significantly reduced Power-Delay Product (PDP) by adjusting the operating frequency within the MHz range. This study introduced a novel differential SRAM architecture featuring a full-swing local bitline (BL) [96]. This was achieved by ensuring a complete swing of the local BL through cross-coupled p-type metal-oxide-semiconductor (pMOS) transistors. Additionally, the gate of the read buffer was driven with a full supply voltage (V_{DD}), eliminating the need for boosted wordline (WL) voltage. In the work by [97], a compensation scheme was presented to address threshold voltage mismatch in sense amplifier (SA) transistors. The accomplishment in question was realized through the digital and iterative adjustment of the body bias voltage. In their study [103], Mani and the research team proposed a design approach that emphasizes low power consumption across writing, reading, and retention modes. Their strategy focused on maintaining robust static noise margins across all operations while minimizing read access time. A prior study [98] investigated power inefficiencies in low-voltage SRAM operating near the threshold voltage. They identified issues such as excessive bit line swing arising from random transistor variation and dynamic power consumption linked to the bit line swing in non-selected columns. In [99], a 10T SRAM cell was introduced, specifically designed for energy-efficient operation, offering high noise margins and radiation-hardened characteristics. Meanwhile, [100] investigated the influence of power supply ramp rate during power-up on SRAM power-up states. They addressed instability concerns leading to inconsistent responses from SRAM Physical Unclonable Functions (PUFs). The study proposed an effective, stable cell selection method to identify SRAM cells that demonstrate a strong startup bias, robustness against circuit noise, and resilience to variations in voltage, temperature, and device aging. Despite these

advancements, the study concluded that additional endeavors are required to achieve more promising outcomes.

1. To solve the issue of SRAM stability and delay, a novel Swing Restoration Inverter (SRI) circuit is developed and implemented utilizing the proposed 8T SRAM cell.
2. A Swing restoration Inverter (SRI) is used to improve the cell's stability during read and write operations.
3. By adding two more transistors, the leakage power is minimized by increasing the node voltages and decreasing the threshold voltages.
4. As a result of the recommended enhancement, SRAM's stability and latency have improved.

This research aims to develop an energy-efficient SRAM cell with minimal leakage by integrating a Swing Restoration Inverter (SRI). A thorough analysis of SRI performance is carried out using both DC and transient analyses, focusing on critical parameters such as leakage power, dynamic power, delays, and power delay product (PDP). In order to achieve a configuration with low leakage in the 8T SRAM, the conventional inverters in the 6T SRAM architecture are replaced with Swing Restoration Inverters (SRIs). The stability of the proposed low-leakage 8T SRAM is assessed based on read and write margins. To improve the stability of the suggested SRAM, appropriate assist techniques are integrated, and the results are compared with those of the conventional 6T SRAM design.

3.2. SWING RESTORATION INVERTER (SRI)

The sub-threshold leakage current outperforms other leakage currents in MOS devices, such as the reverse bias source/drain junction leakage current and Gate Induced Drain Leakage (GIDL) current. Equations (1) and (2) illustrate the sub-threshold leakage current.

$$I_{Subleakage} = I_0 \, e^{(V_{gs} - V_T)/nV_{th}} \, (1 - e^{-V_{ds}/V_{th}}) \qquad (1)$$

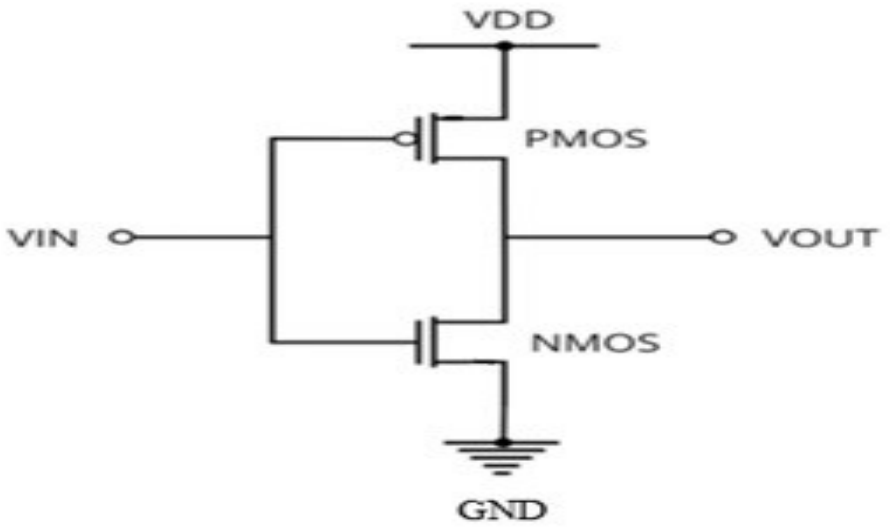
and

$$I_0 = \mu_0 \, C_{ox} \, (W/L) \, V_{th}^2 \qquad (2)$$

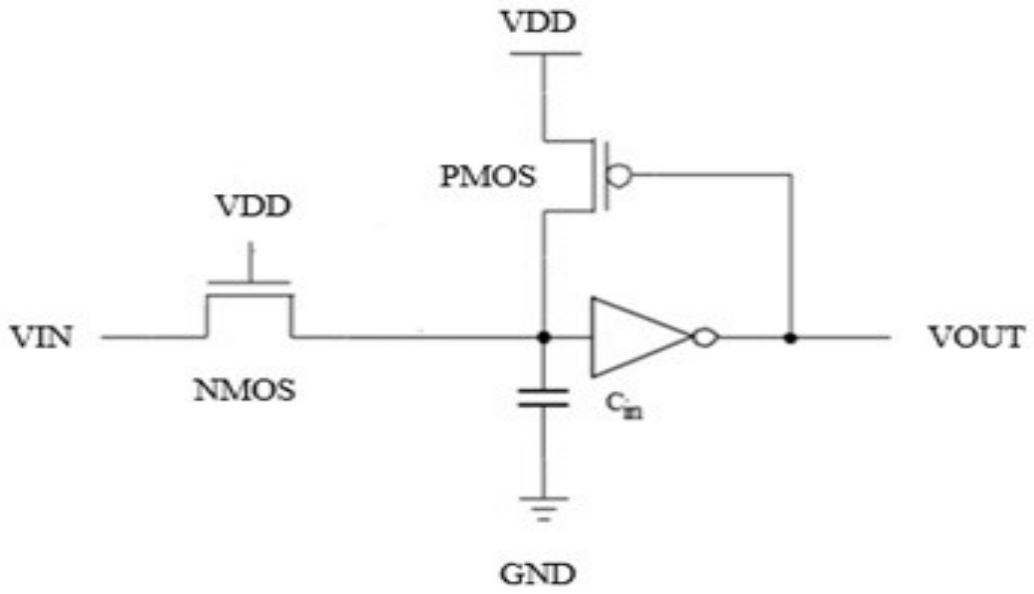
Equation (1) indicates that at smaller technology nodes, the drain-to-source voltage (V_{ds}) and threshold voltage (V_{th}) of the device decrease. However, Equation (1) also reveals that the sub-threshold current exhibits exponential growth as the threshold voltage (V_{th}) decreases. Furthermore, an increase in drain-source voltage (V_{ds}) results in a reduction in the threshold voltage (V_{th}) of the MOS device [81]. To overcome these challenges, swing

restoration emerges as a promising technique to raise the voltages at the node terminals of a MOS transistor, effectively minimizing leakage current. Figures 3.2(a) and 3.2(b) illustrate the standard and swing restoration inverter (SRI) circuits, respectively, with the W/L ratios of transistors specified for the 90 nm technology. The unit sizes are expressed in nanometers. The swing restoration inverter (SRI) circuit in Figure 3.2(b) consists of two main components: a pass-transistor logic output comprising CMOS inverters and a CMOS inverter output. Additionally, there is a swing-restoring node composed of a single CMOS inverter connected to the gate input of PMOS logic. Two types of circuit inputs are present: pass variables linked to the logic transistor's drain and control variables connected to the transistor's gate. The SRI demonstrates the ability to enhance static noise margins in both read and write operations [90].

Node dependency is illustrated in Figure 3.3, showcasing the impact of Q voltage on the width of M6. As the voltage at Q increases, the width of M6 also increases, ensuring that Q is charged by M6. This exclusive charging maintains Vgs more negative. The choice of M6 width is crucial, ranging between 50% and 135% of M2, to prevent the leakage path from shifting to M6, M2, GND, and to ensure optimal performance (preventing Q from exceeding $V_{dd}/2$ and ensuring a full swing output voltage). While widening M6 can further reduce leakage, it is essential to keep Q at a lower potential than the output node. For all simulations in this study, the Cadence simulator and 90 nm technology were employed. The simulations were conducted at 27°C for the 90 nm technology. The supply voltage utilized is 1 V for 90 nm technology and 0.9 V for 16 nm.



(a) Conventional Inverter [102].



(b) Swing Restoration Inverter (SRI).

Figure 3.2. Circuit schematics (W/L is in nanometers).

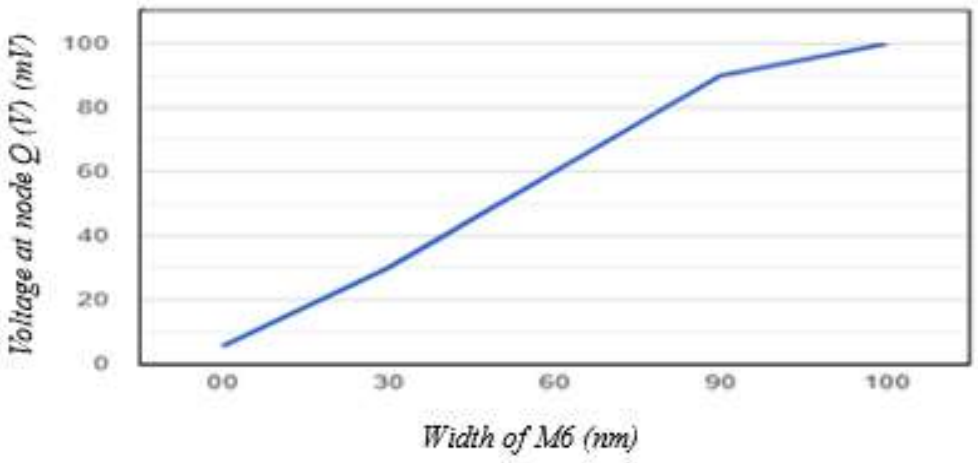


Figure 3.3. Dependency of node (Q) voltage on the width of M6 (nm).

3.2.1 Transfer characteristics

To examine the transfer characteristics of the two inverters, a DC analysis is performed at a temperature of 27 °C. As depicted in Figure 3.4, the transfer characteristics of swing restoration inverters (SRI) and conventional inverters (INV) for a 90 nm technology are illustrated. The circuit of the swing restoration inverter (SRI) is analogous to the conventional inverter but exhibits robust voltage transfer characteristics.

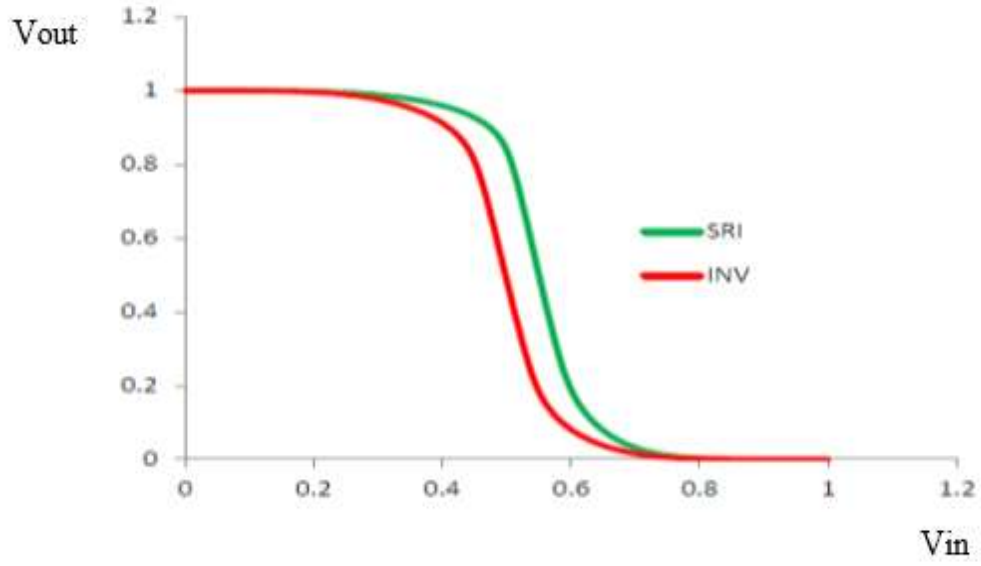


Figure 3.4. Inverter characteristics.

3.2.2 Leakage power

The power consumed by a circuit in a standby state is commonly referred to as leakage power. To assess leakage power, the inverter's input is set to logic '1' or logic '0'. The current flowing through the capacitive load (C_L) is then measured, and the leakage power is calculated using Equation (3). In this study, the specified value for C_L is 0.01 pF.

$$P_{leakage} = I_{leakage} \times V_{DD} \quad (3)$$

When a logic '0' is applied to the input of the two inverters, the analysis of leakage power indicates values of 25.37 pW for the standard inverter and 9.30 pW for the Swing Restoration Inverter (SRI) in the 90 nm technology. The exploration of leakage power trends highlights that Swing Restoration Inverters (SRI) demonstrate lower leakage power compared to traditional inverters in the 90 nm technology. Specifically, at the 90 nm technology, the Swing Restoration Inverter (SRI) achieves a 67% reduction in leakage power.

3.2.3 Dynamic power

The power consumed by the circuit during its operational state is known as dynamic power. The measurement of dynamic power for the inverters becomes significant as different strategies for reducing leakage power can impact dynamic power. The calculation of dynamic power is performed using Equation (4).

$$P_{dynamic} = V_{DD}^2 \times f_{in} \times C_L \quad (4)$$

The frequency of the input signal is represented by fin. In this scenario, the Swing Restoration Inverter (SRI) is evaluated by measuring the current passing through C_L. The circuit is supplied with a 1 MHz input signal and a capacitive load (C_L) of 0.1 pF. Table 3.1 presents the identified dynamic power. Comparative analysis with a conventional inverter reveals that the Swing Restoration Inverter (SRI) effectively lowers dynamic power.

3.2.4 Power delay product (PDP)

The Power-Delay Product (PDP) serves as a crucial metric for assessing the power efficiency of a CMOS circuit. It is computed by multiplying the average power dissipation by the propagation delay. In the context of low-power design, the objective is to minimize the Power-Delay Product (PDP). Figure 3.5 visually represents the time domain response of two inverters designed for the 90 nm technology. Meanwhile, Table 3.2 provides a concise summary of various time domain characteristics observed. Table 3.3 furnishes data on delay, average power dissipation, and PDP for both inverters at 27°C across different technology nodes. It is worth noting that the Swing Restoration Inverter (SRI) exhibits a longer delay compared to a traditional inverter. However, the average power dissipation of the Swing Restoration Inverter (SRI) is lower than that of the conventional inverter. Consequently, this leads to a reduced Power-Delay Product (PDP) for the Swing Restoration Inverter (SRI).

3.3. CONVENTIONAL 6T SRAM CELL VERSUS PROPOSED 8T SRAM CELL DESIGN

In a conventional 6T SRAM cell, the data storage nodes are directly accessed through the bit-line access transistors during read operations, as shown in Figure 3.6. While reading, the storage node voltages are disturbed between the cross-coupled inverter pair and bit lines. The BL and BLB are the bit lines, and WL is the word line. The access transistors are controlled by WL (word line) to perform the operation of read and write operations. In an SRAM cell, the bit lines are used as both input and output nodes. During a read operation, bit lines transfer the data from SRAM cells to a sense amplifier. Based on the technology, the minimum length of the transistors is 90 nm.

The swing restoration technique emerges as a promising strategy to mitigate leakage power in CMOS circuits, offering a potential alternative to the traditional use of inverters in SRAM cells. In this investigation, we assess leakage power by substituting the inverter in

a 6T SRAM cell with a swing restoration inverter (SRI). To enhance the stability of the SRAM cell, a comprehensive analysis of the cell's stability is conducted, incorporating appropriate assist techniques. Figure 3.7 illustrates a typical 6T SRAM cell, consisting of two inverters (M1, M5, M2, M6) and access transistors (M3, M4). Dimensions are specified in nanometers, and transistor sizes are denoted based on 90 nm technology. During the active mode of operation, two access transistors (M3, M4) are turned ON. The M7 and M8 transistors reduce the swing voltages and function as swing-restored transistors. In standby mode, these transistors are switched OFF by reducing the word line (WL) voltage to zero. Setting the WL lines to zero facilitates the identification of the sub-threshold leakage current component in the 6T SRAM.

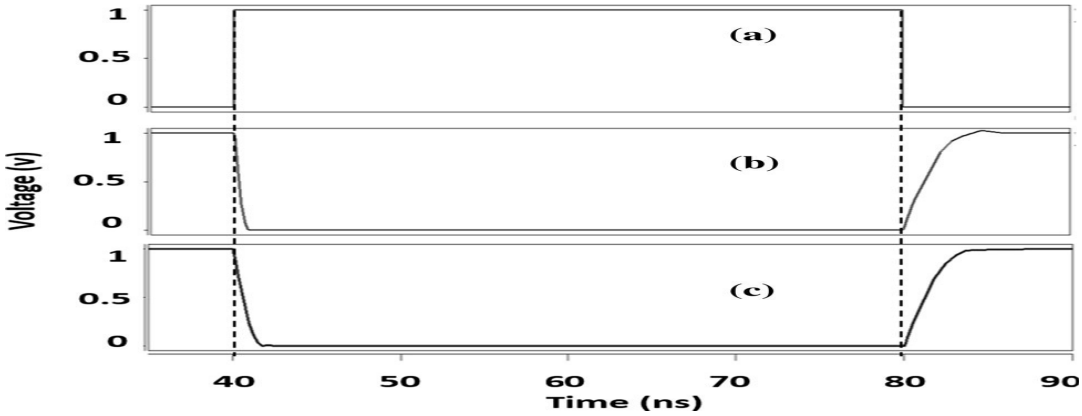


Figure 3.5. Time domain responses at 90 nm technology. (a) Inverter input. (b) Output of a conventional inverter. (c) Output of swing restoration inverter (SRI).

Figure 3.8 depicts a novel SRAM design integrating swing restoration inverters (SRI) with the goal of minimizing leakage. Instead of the two inverters found in conventional 6T SRAMs, swing restoration inverters are utilized, resulting in a proposed 8T SRAM configuration. To mitigate sub-threshold current in inverter-1, the source voltage of NMOS transistor M3 is elevated, primarily determined by the leakage current supplied by transistor M1. In inverter-2, the reduction in sub-threshold current depends on the source voltage of PMOS transistor M6, influenced by the leakage current from NMOS transistor M2. For a successful write operation, we should have M4 greater than M6. When setting the word lines (WL) to zero, the sub-threshold leakage current component in both conventional and proposed SRAMs can be identified. Cadence simulation is employed to compare the leakage power of the 90 nm technology. Figure 3.8 illustrates the temperature-dependent leakage power of the SRAM cell, demonstrating an increase in leakage power

with rising temperature. Notably, the leakage power of a proposed 8T SRAM cell is lower than that of a 6T SRAM cell. Specifically, at 27°C, the maximum leakage power of the 6T SRAM cell is 12.2 nW, whereas that of the proposed 8T SRAM cell is 1.07 nW. This results in leakage power savings of 91.22% at 27°C and 86% at 108°C for the 8T SRAM cell, as shown in Table 3.4.

Table 3.1: Comparison of dynamic Power

Technology (nm)	**Dynamic power (nW)**	
	Conventional inverter	**Swing Restoration inverter**
32	27.17	11.30
90	25.37	9.30

Table 3.2: Time domain response

Time domain response	**Rise time (t_r) (ns)**	**Fall time (t_f) (ns)**	**Propagation delay Low-high (t_{plh}) (ns)**	**Propagation delay High-low (t_{phl}) (ns)**
Conventional inverter	1.177	0.250	0.737	0.1561
Swing restoration inverter	1.58	0.503	0.732	0.1592

Table 3.3: Comparison of delay and power delay product (PDP)

Tech. (nm)	**Conventional inverter**			**Swing restoration inverter (SRI)**		
	Delay (ns)	**P (average) (W)**	**PDP (J)**	**Delay (ns)**	**P (average) (W)**	**PDP (J)**
32	0.7715	2.766 e^{-11}	213.39 e^{-22}	0.9167	0.9065 e-11	83.09 e^{-22}
90	0.6161	8.001 e^{-11}	600.1 e^{-22}	0.9211	0.9121 e^{-11}	84.03 e^{-22}

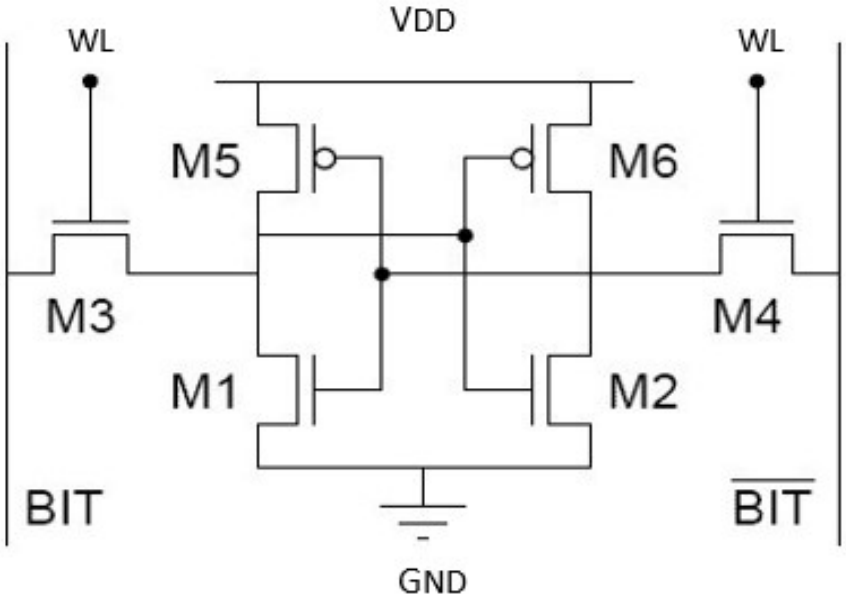


Figure 3.6. Conventional 6T SRAM cell (W/L is in nanometers).

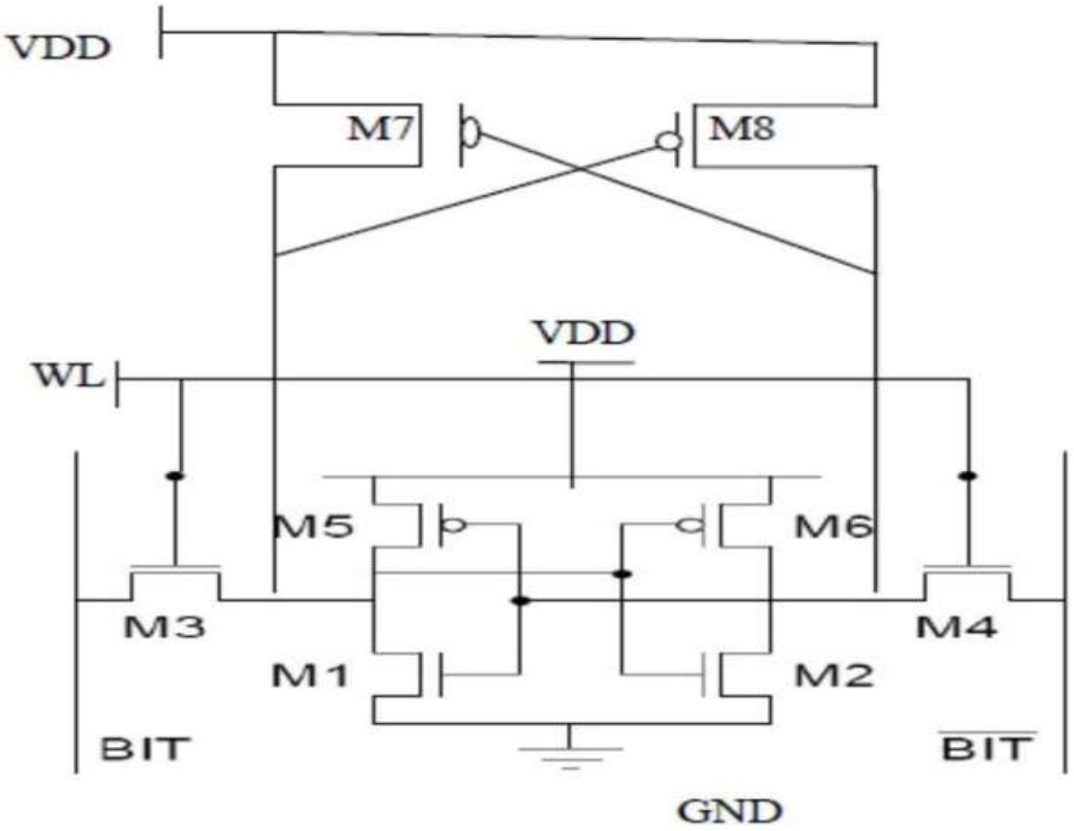


Figure 3.7. Proposed 8T SRAM cell (W/L is in nanometers).

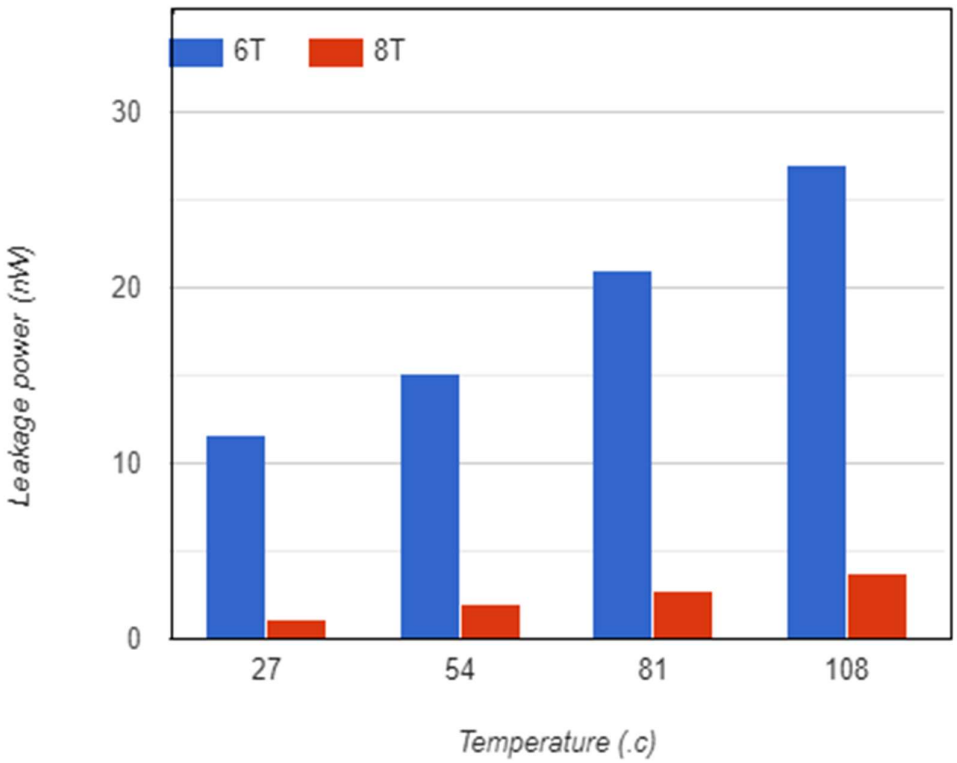


Figure 3.8. Temperature dependency of leakage power.

Table 3.4: Comparison of Conventional 6T SRAM and Proposed 8T SRAM Leakage Power

Temperature (°C)	**Conventional 6T SRAM** Leakage power (nW)	**Proposed 8T SRAM** Leakage power (nW)
27	12.2	1.07
54	15.08	1.999
81	21.05	2.766
108	27.01	3.799

Table 3.4, Comparison of conventional 6T and proposed 8T SRAM Leakage power (nW) with respect to Figure 3.8, variation of leakage power with temperature.

3.4. PROPOSED 8T SRAM CELL MODE OF OPERATIONS

This is a proposed SRAM, dual-node voltage with swing restoration logic. Perform node voltage in hold, read, and write operations, and other parameters like delay, stability, are used in Figure 3.7. Comparison between Low-power 6T SRAM and proposed 8T SRAM Cells in Table 3.5. The comparison results reveal that read, write, and hold mode operation for an 8T SRAM cell is better than 6T SRAM cell. This is because a higher noise margin is obtained, which ensures good write ability for the bit-cell.

3.5. IMPROVED STABILITY

Read assist methods aim to enhance the stability of reading operations, while write assist approaches focus on stabilizing write operations. In this study, we employ techniques like boosting the voltage of write word lines and lowering the voltage of read word lines to improve the ability of writing (WSNM) and the stability of reading (RSNM), respectively. Our investigation into stability enhancement encompasses both conventional SRAM and the proposed 8T SRAM cell in the 90 nm technology, Table 3.6 and Table 3.7.

3.5.1 Read Stability

The Read stability is measured by the read static noise margin (RSNM) in the SRAM Cell. In the proposed 8T SRAM cell, due to storing nodes isolation, we get better RSNM comparable to the conventional 6T SRAM Cell. Figure 3.9 (a) and Figure 3.10 (a) represent the read stability of 6T and proposed 8T SRAM Cells, respectively.

3.5.2 Write Stability

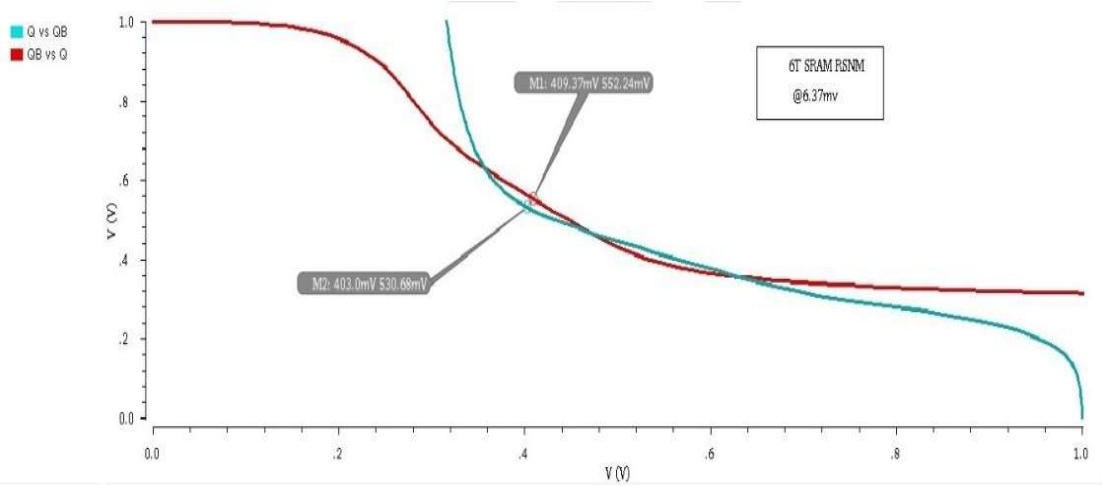
The write stability is measured by write static noise margin (WSNM). In the proposed 8T SRAM cell, due to storing nodes isolation, we get better WSNM comparable to the conventional 6T SRAM Cell. Figure 3.9 (b) and Figure 3.10 (b) represent the write stability of 6T SRAM and proposed 8T SRAM cells, respectively. Write trip point is the measure of the write ability of the cell. It shows how difficult it is for the storing nodes of the cell. The bit-line voltage is swept from 0 to V_{DD}, and the flipping of the cell, when Q and QB flip their content, is captured. The value of bit-line voltage at the crossing point of internal storage nodes Q and QB represents the write trip point.

3.5.3 Hold Stability

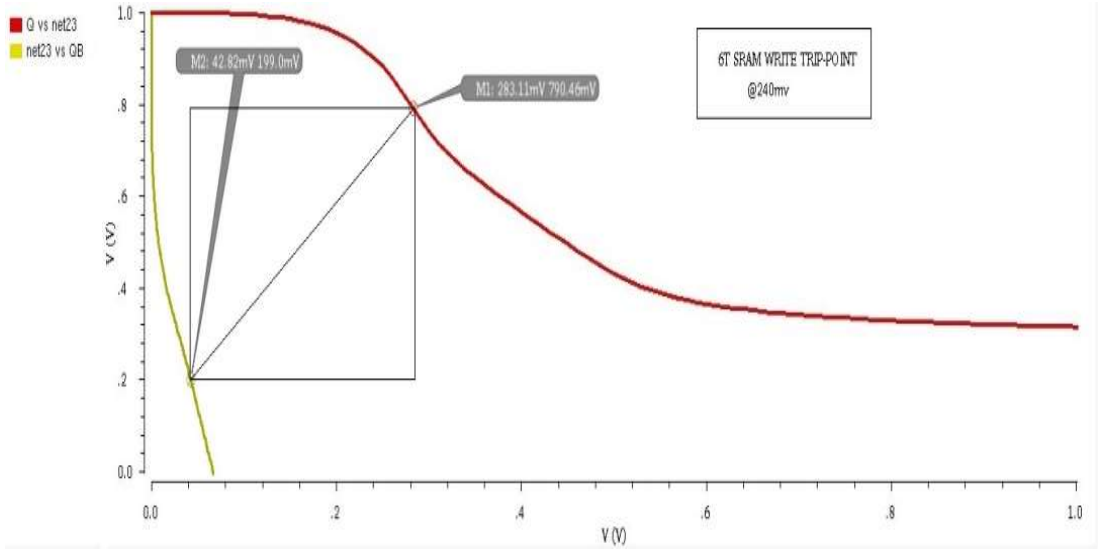
Static noise margin (SNM) is the most common approach to measure the hold stability of the cell. Hold stability is calculated when the SRAM cell is in the hold state. In the hold state, the word lines are off, so the cell is totally disconnected from the bit lines. SNM defines the largest noise that can be imposed on the storage nodes before flipping the content of the Cell.

3.6. RESULTS AND DISCUSSIONS

The Simulations were conducted using the Cadence Virtuoso tool with the 90 nm technology. Throughout the process, the supply voltage was set at 1V, and PTM models were utilized while maintaining a temperature of 27 °C. The margin of swing restoration inverter (SRI) exhibited a significant increase for both SRAM configurations, for the traditional 6T SRAM and 8T SRAM cells. The proposed method demonstrates its effectively in reducing power leakage in deep sub-micron technologies. An examination of the swing restoration inverter through DC analysis highlights its advantageous voltage transfer characteristics (VTCs).

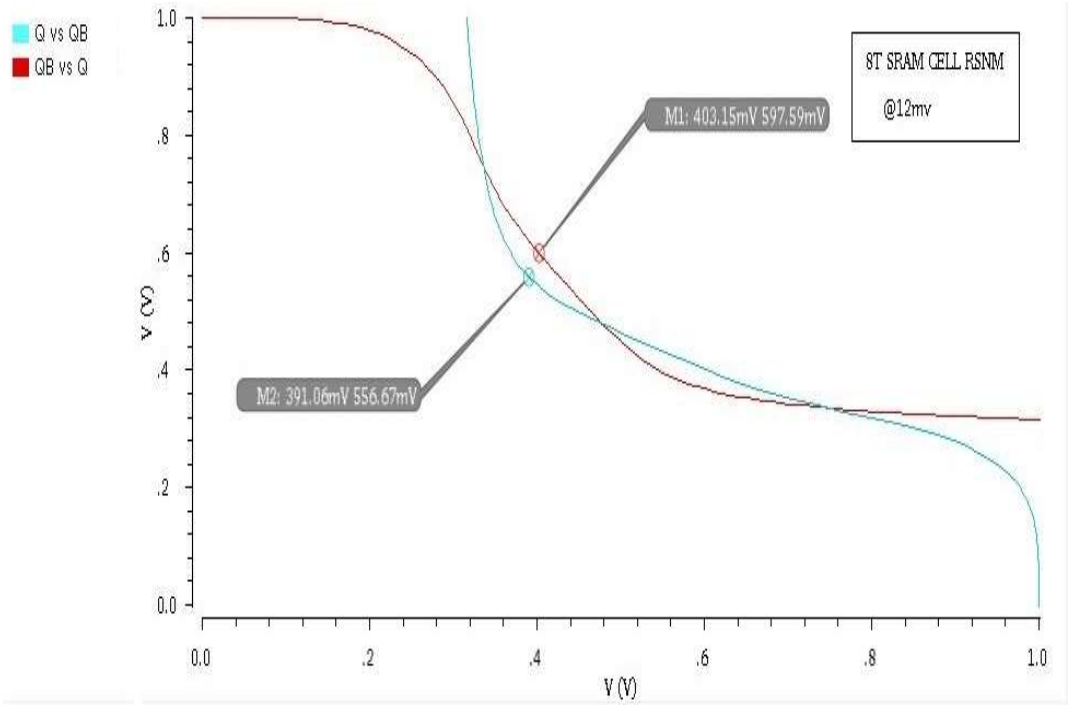


(a) RSNM

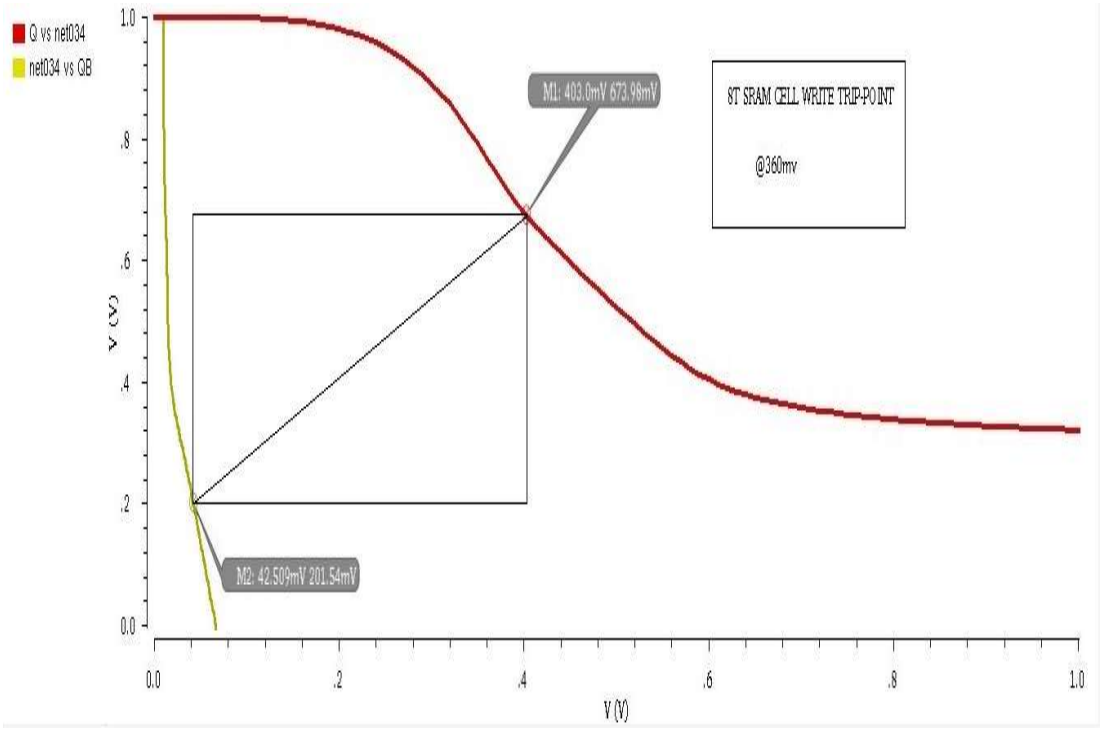


(b) WSNM

Figure 3.9. Characterisation of conventional 6T SRAM cell.



(a) RSNM



(b) WSNM

Figure 3.10. Characterisation of proposed 8T SRAM cell.

Table 3.5: Characterization of SRAM cells

Conventional 6T SRAM Cell		Proposed 8T SRAM Cell	
RSNM (mV)	**WSNM (mV)**	**RSNM (mV)**	**WSNM (mV)**
6.37	240	12	360

Table 3.6: Read operation word line voltage drop

Word line voltage (V)	Conventional 6T SRAM Cell		Proposed 8T SRAM Cell	
	RSNM (mV)	**% Improvement**	**RSNM (mV)**	**% Improvement**
1	6.37	--	12	--
0.8	11.9	55	74	62
0.6	91.2	85	94	82
0.4	104	97	103	91

Table 3.7: Write operation word line voltage boost

Word line voltage (V)	Conventional 6T SRAM Cell		Proposed 8T SRAM Cell	
	WSNM (mV)	**% Improvement**	**WSNM (mV)**	**% Improvement**
1	240	--	360	--
1.1	300	30	420	30
1.2	302	31	424	32
1.4	304	32	428	34

The provided information highlights the effectiveness of Swing Restoration Inverters (SRIs) in mitigating leakage power consumption, presenting distinct advantages over standard inverters. At 90 nm technology and 27°C, SRIs exhibit a significant 67% reduction in leakage power, which decreases to 39% at 22 nm and 35% at 16 nm with advancements in technology. Additionally, the swing restoration approach plays a crucial role in minimizing dynamic power usage, consistently resulting in a lower Power-Delay Product (PDP) compared to conventional inverters. Figure 3.7, An innovative application of SRIs involves their integration into the Conventional 6T SRAM cell, transforming it into a Proposed 8T SRAM cell with minimal leakage because dual node voltage is stored through transistors M7 and M8 are swing restoration inverters (SRIs).

Table 3.8 explores various strategies for minimizing leakage power in SRAM cells, accounting for differences in researchers' methodologies, simulation parameters, and technology variations. Notably, with 90 nm technology, the proposed approach achieves the lowest power consumption at 1.07 nW and 3.799 nW at 27°C and 108°C, respectively, demonstrating substantial savings of 91.22 % and 86% in leakage power. The versatility of the swing restoration approach extends to different conventional SRAM cells utilizing cross-coupled inverters. Comparative analysis of Read Static Noise Margin (RSNM) and Write Static Noise Margin (WSNM) values between Conventional 6T SRAM and Proposed 8T SRAM cells reveals their similarity. To evaluate stability enhancement, both types of SRAM cells undergo write and read stability mode operations. The Proposed 8T SRAM cell consistently outperforms the Conventional 6T SRAM cell in terms of stability.

Table 3.8: Comparison of various SRAM cells design techniques

Paper	Tech (nm)	SRAM cell	Technique	Temp (°C)	Leakage power (nW)	Leakage power savings (%)	Tool
Kavitha & Govindaraj [101].	32	6T	Low-power multimodal switchpower gating	–	23.00	91.00	HSPICE
Venkatareddy et al. [76].	28	10T	Dual power supply-based design	25	–	85.00	Measurement results
Krishna & Duraiswamy [102].	32	10T	Source biasing technique	25	1.06	90.88	HSPICE
Prasad & Anand [71].	90	8T	Supply voltage scaling	27	44.85	40.40	Cadence
Sharma et al. [72].	32	9T	FinFET based design	25	16.90	53.21	HSPICE
Venkatareddy et al. [76].	60	7T	Super cut-off word line	–	21.85	26.00	–
Mani et al. [103].	90	Conventional 6T SRAM Cell	Conventional inverter	27	5.62	45.44	Cadence
Proposed work	90	Proposed 8T SRAM Cell	Swing restoration inverter	27	1.07	91.22	Cadence

3.7. SUMMARY

In this chapter, in the context of designing SRAMs for deep sub-micron technologies, a novel low-leakage inverter based on a swing restoration approach is introduced. This innovative design incorporates two additional transistors used to node restoration to minimize leakage power. The presence of these additional transistors elevates node voltages while concurrently reducing threshold voltages (V_{th}). The resulting swing restoration inverter (SRI) exhibits lower leakage power compared to Conventional inverters. At a temperature of 27°C, the SRI achieves significant leakage power savings, amounting to 67% for the 90 nm technology and 57% for the 32 nm technology, respectively. However, it is noted that as technology nodes decrease, the leakage power savings of the suggested inverter diminish. Furthermore, it is demonstrated that the dynamic power consumption is reduced in both 90 nm and 32 nm technologies when utilizing the swing restoration inverter (SRI). The implementation of SRIs in place of standard inverters in a 6T SRAM design, with the low-leakage inverter employed for SRAM design, showcases noteworthy results. Comparing the resulting proposed 8T SRAM cell to a conventional 6T SRAM at 90 nm technology, there is a substantial reduction in leakage power 86% at 108°C and 91.22% at 27°C, respectively. Importantly, the proposed 8T SRAM cell maintains low leakage while being equivalent to the 6T SRAM cell in terms of stability. Moreover, the Proposed 8T SRAM cell, when incorporating swing restoration techniques, demonstrates enhanced stability compared to Conventional designs. It is important to note that the Proposed 8T SRAM cell integrates two additional transistors compared to the Conventional 6T SRAM cell, a trade-off made to effectively reduce leakage power and enhance stability. In conclusion, while working at 90 nm technology node has its limitations, it was a relevant choice for the research given its widespread adoption at the time. However, it is essential to acknowledge these limitations and to consider how to extend and adapt the proposed techniques to newer technology nodes in future work.

CHAPTER 4
IMPROVED STABILITY OF LOW POWER SRAM CELL

The cell stability analysis of the sensitivity of the memory cell using low-power VLSI. The stability of a Static Random access memory cell in the presence of DC noise is measured by the static noise margin (SNM). Static Noise Margin is the amount of voltage noise required at the output nodes to flip the state of the cell. This can be obtained using the voltage transfer characteristic (VTC) of the two cross-coupled inverters of the SRAM cell. Thus, the following objective is framed to accommodate the aforementioned need –

"A Comparative Analysis of 6T and 8T SRAM Cells for Improved Read and Write Margins."

Methodology used to achieve the desired objective in the chapter is as follows -

- To improve the stability of the 8T SRAM cell for low power and high- speed.
- Design an 8T SRAM bit cell for the improved read and write margin.
- Analyze the performance of the proposed 8T SRAM cell and validate it against the conventional 6T SRAM cell.

The concept for a proposed 8T SRAM cell is presented here in further context. To improve the stability of 8T SRAM cell for low power and high-speed. Analyze the performance of the proposed 8T SRAM cell and compare the performance with the 6T SRAM and Standard 8T SRAM cells.

This chapter is categorized into seven sections, including the introduction to low-power SRAM in VLSI chips, Section 4.1. Further in section 4.2, the six-transistor SRAM cell is explained. In section 4.3, explain the standard 8T-SRAM cell. Thereafter, the Evaluation of various performance parameters is explained in section 4.4. While the proposed 8T SRAM cell is explained in section 4.5, its results and discussions are presented in section 4.6. Finally, the important results for the chapter are summarized in section 4.7.

4.1. INTRODUCTION TO LOW-POWER SRAM IN VLSI CHIPS

Low-power Static Random-Access memories have become a critical component of many VLSI chips [118]. This is a special consideration for microprocessors where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processors and the main memory [118-119]. One of the major issues in the design of an SRAM cell is stability. The cell stability determines the sensitivity of the memory to process tolerances and operating conditions [113-114].

The stability of the Static Random access memory cell in the presence of DC noise is measured by the static noise margin (SNM). Static Noise Margin is the amount of voltage noise required at the output nodes to flip the state of the cell. This can be obtained using the voltage transfer characteristic (VTC) of the two cross-coupled inverters of the SRAM cell [105-109]. Figure 4.1 illustrates the schematic of a 6-transistor SRAM cell for simulating the static noise margin. The voltage sources (V_N) are the noise sources at the state nodes of the cell [109].

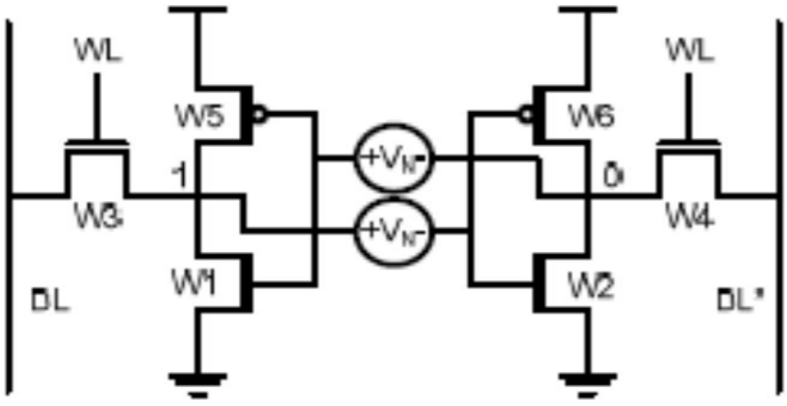


Figure 4.1. Schematic of a 6T SRAM bit cell with noise voltage sources for measuring SNM [109].

The cross-coupled inverters maintain a bistable state, and their output nodes retain the data stored in the cell. However, as the noise V_N increases, the stability of the cell degrades because of the fluctuations at the node voltages. The Static Noise Margin quantifies the allowed levels of these noise voltages and thus the ability of these inverters to retain their state in the presence of noise. The SNM of the SRAM Cell is used when in standby or retain mode, for read operations, and write operations. The SNM of the SRAM cell is obtained by plotting the VTCs of the two cross-coupled inverters. The VTC of one of the inverters is flipped with respect to the line y = x in order to form a “butterfly curve”. The SNM is the side of the smaller square that can be fitted inside the “eye” of the graph, as shown in Figure 4.2 [109].

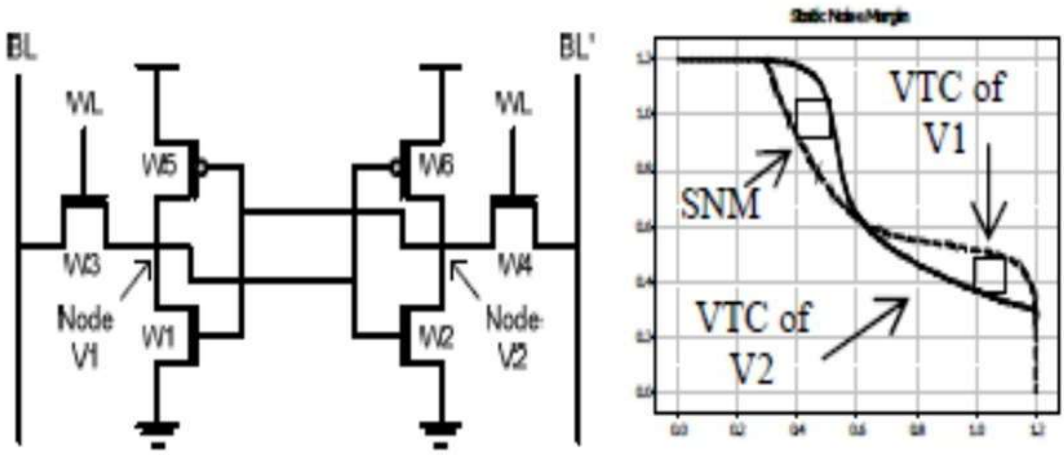


Figure 4.2. Schematic of a 6T SRAM bit cell and a sample of the side of The largest square fitted inside the graph [109].

Literature review of existing systems using and improving the performance parameters of SRAM cells using 130 nm CMOS Technology. define Performance Parameters of SRAM Cells [112], [117].

Read delay: Read delay refers to the time taken for the bit lines to discharge by approximately 10% of their maximum value, or the interval between the activation of the word line (WL) signal and the response time of the sense amplifier [115].

Write delays: Write delay is the time between the activation of the word line (WL) signal and the moment when the data is successfully written into the cell [115].

Leakage power: Leakage power is the energy consumed by a device that is not associated with state transitions. Also known as static power, it is present during both idle and switching conditions, but is particularly concerning during the inactive state, where all power consumed is essentially wasted [116].

Static Noise Margin: SNM quantifies the maximum noise voltage that can be introduced at the inputs of two cross-coupled inverters before the cell either loses its current stable state (during hold or read operations) or unintentionally switches to another stable state (during write operations) [54].

4.2. SIX-TRANSISTOR SRAM CELL

In a conventional 6T SRAM cell, the data storage nodes are directly accessed through the bit-line access transistors during read operations, as shown in Figure 4.3. While reading, the storage node voltages are disturbed between the cross-coupled inverter pair and bit lines. The BL and BLB are the bit lines, and WL is the word line. The access transistors

are controlled by WL (word line) to perform the operation of read and write operations. Bit lines act as input and output nodes. During a read operation, bit lines transfer the data from SRAM cells to a sense amplifier. Based on the technology, the minimum length of the transistors is 130 nm [26], [120].

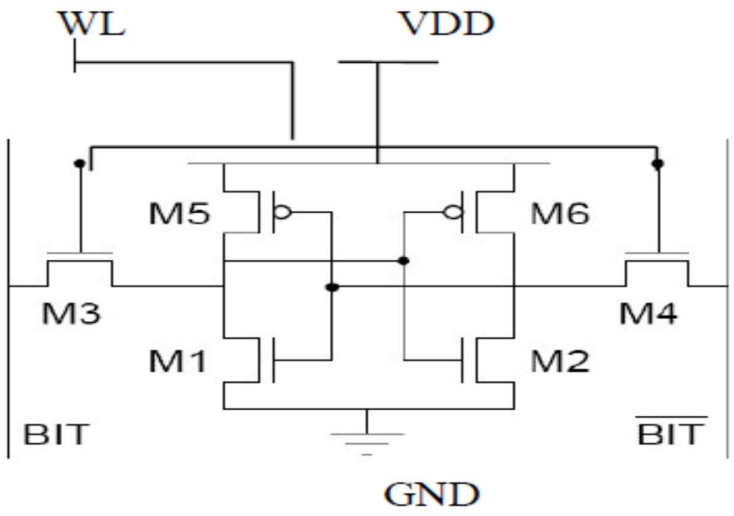


Figure 4.3. Conventional 6T SRAM cell [26].

4.3. STANDARD 8T SRAM CELL

The standard 8T-SRAM Cell is shown in Figure 4.4 as it is seen, that read and write cycles use different word lines and bit lines. Note that the standard 8T SRAM cell uses a single-ended read scheme which reduces the swing of bit lines. The 8T-SRAM cell provides significantly improved RSNM (similar to the Hold Static Noise Margin (HSNM) of the standard 6T-SRAM cell) with similar access time, write time, and write margin [110-111].

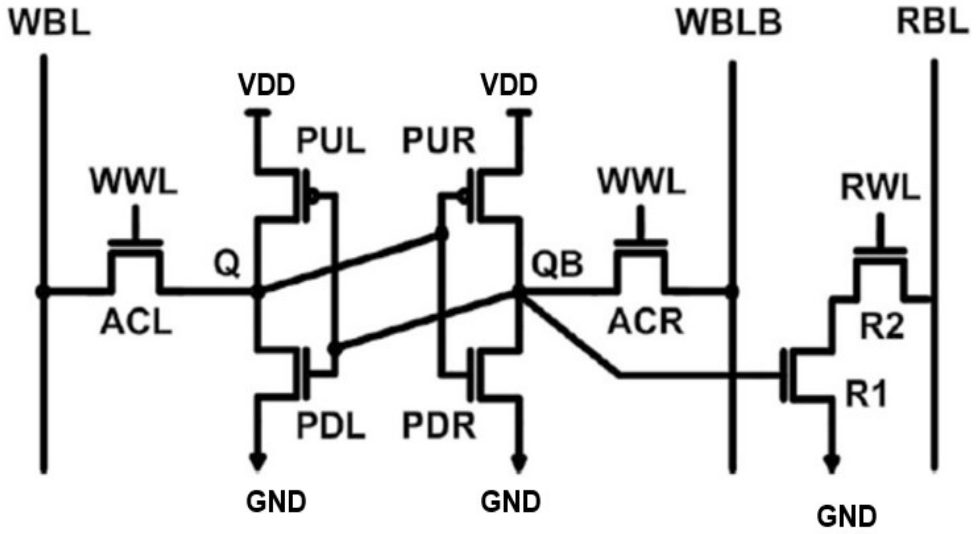


Figure 4.4. Standard 8T-SRAM cell [110-111].

The standard 8T-SRAM Cell is shown in Fig.4.4 as it is seen, read, and write cycles use different word lines and bit lines. Note that the standard 8T SRAM cell uses a single-ended read scheme, which reduces the swing of bit lines [111].

4.4. EVALUATION OF VARIOUS PERFORMANCE PARAMETERS

In this section, the performance of the proposed SRAM cell is evaluated and compared with various existing SRAM cell topologies. To ensure a comprehensive analysis, different designs are considered, including the conventional 6T SRAM, the standard 8T SRAM, and the proposed 8T SRAM cell.

Stability: Stability refers to the cell's ability to resist noise or unintended flipping caused by external disturbances during read, write, or hold operations. Across all these modes, stability is commonly measured using Static Noise Margin (SNM) techniques, typically visualized through butterfly curves [54]. In this study, stability is assessed during read, write, and hold states using RSNM (Read SNM), Write Trip Point (WTP), and Hold SNM (HSNM), respectively.

Read static noise margin (RSNM): RSNM measures the read stability of an SRAM cell. The butterfly curve method is used here, where the largest embedded square that fits into the lower lobe of the butterfly plot defines the RSNM [54], [62]. A higher RSNM value indicates better stability while reading data stored at internal nodes. During this analysis, the word line (WL) remains active to generate the butterfly curve for the read operation.

The proposed 8T SRAM cell demonstrates superior RSNM compared to both the traditional 6T and standard 8T SRAM cells. This improvement stems from the fact that, during the read operation, the bit-lines are completely isolated from the internal storage nodes Q and Qb, thus eliminating read disturbances. In contrast, the 6T SRAM's RSNM is significantly impacted by voltage division between the access and pull-down transistors, which introduces noise and can lead to unintentional flipping of the cell's state. In the proposed design, this issue is mitigated by incorporating PMOS cross-coupled transistors (M7 and M8), which increase the reverse bias and introduce a high-resistance path. This suppresses leakage current through the cell, thereby reducing noise at the storage nodes and enhancing read stability.

Write margin (WM): Write margin indicates the ease and efficiency with which data can be written to the cell's internal nodes Q and Qb. Write capability is typically assessed using either the write trip point (WTP) or the butterfly curve approach [63]. In the butterfly method, the largest square that can fit inside the lower lobe during a write operation is considered. To plot this curve, the word line (WL) is activated [64]. In this study, the write

margin is determined using the write trip point method, which provides a clear metric for evaluating how effectively the proposed SRAM cell can be written to.

4.5. LOW POWER 8T SRAM CELL

The low-power 8T SRAM cell is illustrated in Figure 4.5. In the low-power 8T SRAM cell, two PMOS transistors, M7 and M8, are connected to the cross-coupled node voltages Q and Qb, respectively. Directly switch the PMOS transistors ON and OFF during read and write operations. At the Stability analysis proposed 8T SRAM cell, the pre-charge voltage level reduces the swing voltage during read and write operation [108]. This reduction in swing voltage reduces the dynamic power dissipation. The comparison results revels that read, write, and hold mode operation for a low power 8T SRAM cell is better than 6T SRAM cell. This is because higher static noise margins are obtained, which ensure good write ability for the bit cell.

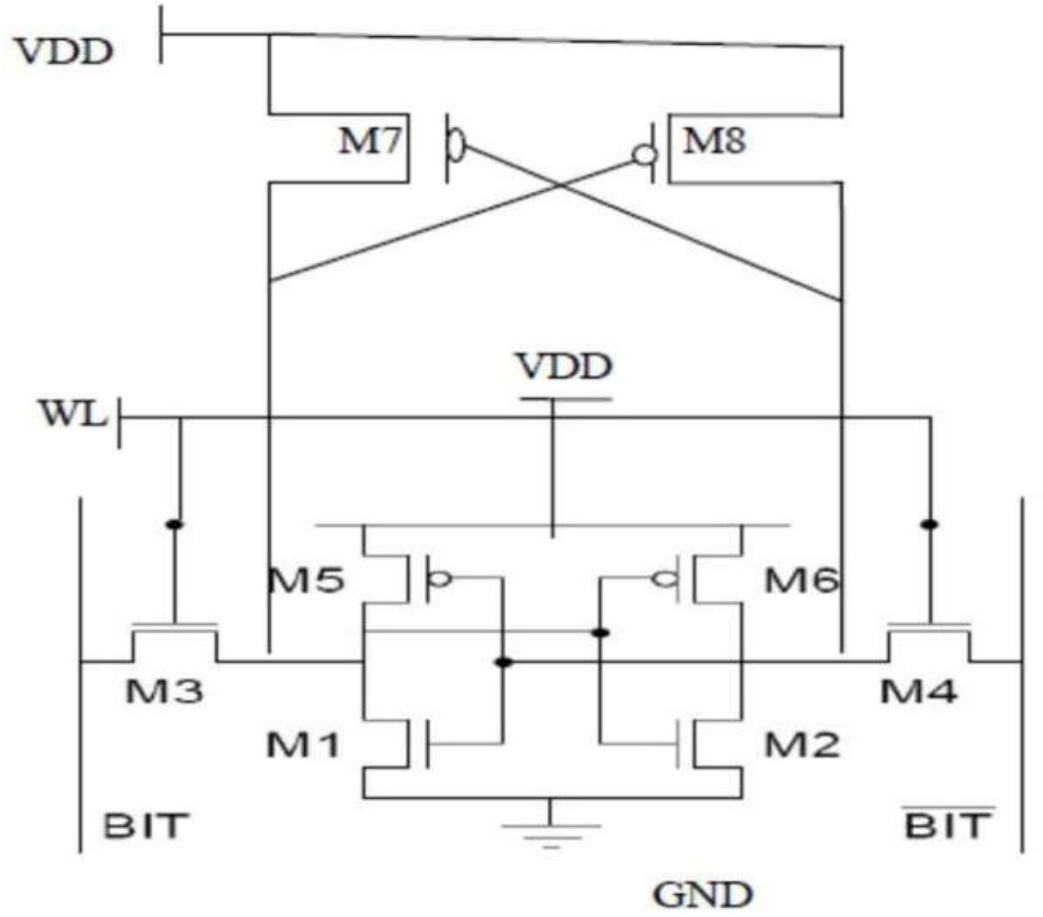


Figure 4.5. Low power 8T SRAM Cell [108].

4.6. RESULTS AND DISCUSSIONS

The simulation is carried out in SymicaDE software at 130 nm technology. Analysis of the low power 8T SRAM cell in terms of write ability, read stability, and hold static noise margin has been carried out in this section. These results are compared with standard 6T SRAM and 8T SRAM cells, Table 4.1 and Table 4.2. The circuit is characterized by using the 130 nm Technology with the supply voltage of 1.2V.

4.6.1 Hold Stability

Static noise margin (SNM) is the most common approach to measure the hold stability of the cell. Hold stability is calculated when the SRAM cell is in the hold state. In the hold state, the word lines are off, so the cell is totally disconnected from the bit lines. SNM defines the largest noise that can be imposed on the storage nodes before flipping the content of the cell. Figures 4.6, 4.7, and 4.8 show the hold static noise margin of 6T SRAM, standard 8T SRAM, and Low power 8T SRAM cells, respectively.

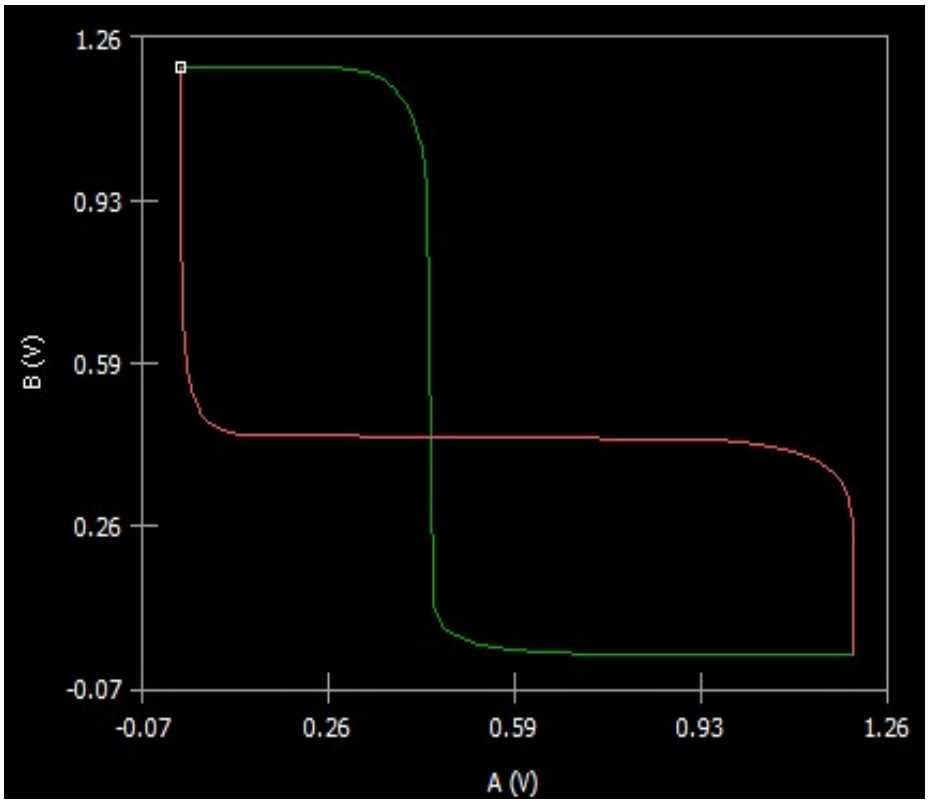


Figure 4.6. HSNM 6T SRAM Cell**.**

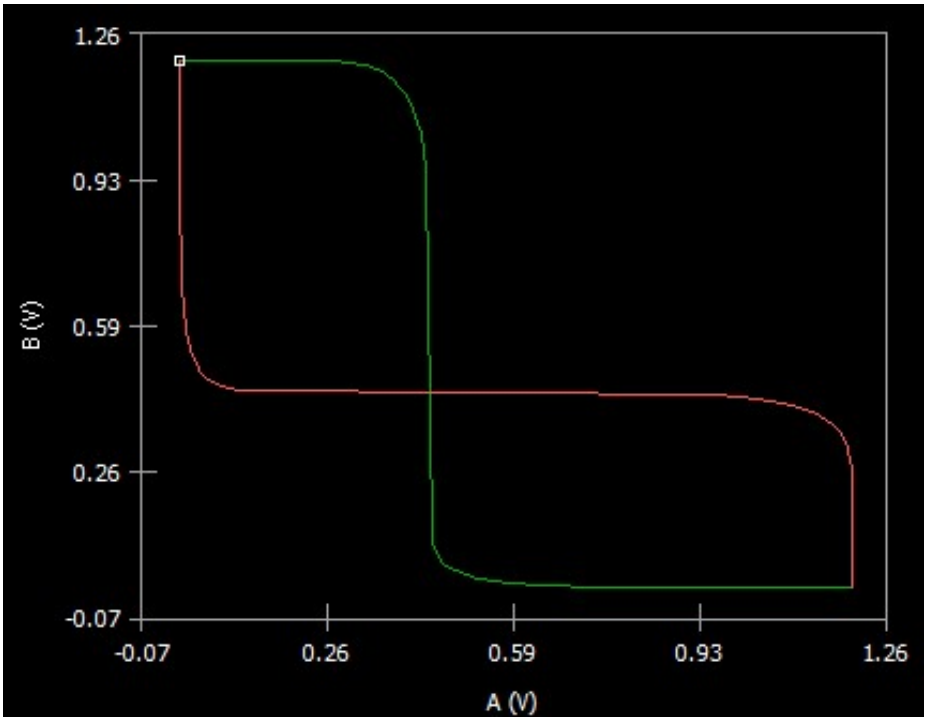


Figure 4.7. HSNM standard 8T SRAM cell**.**

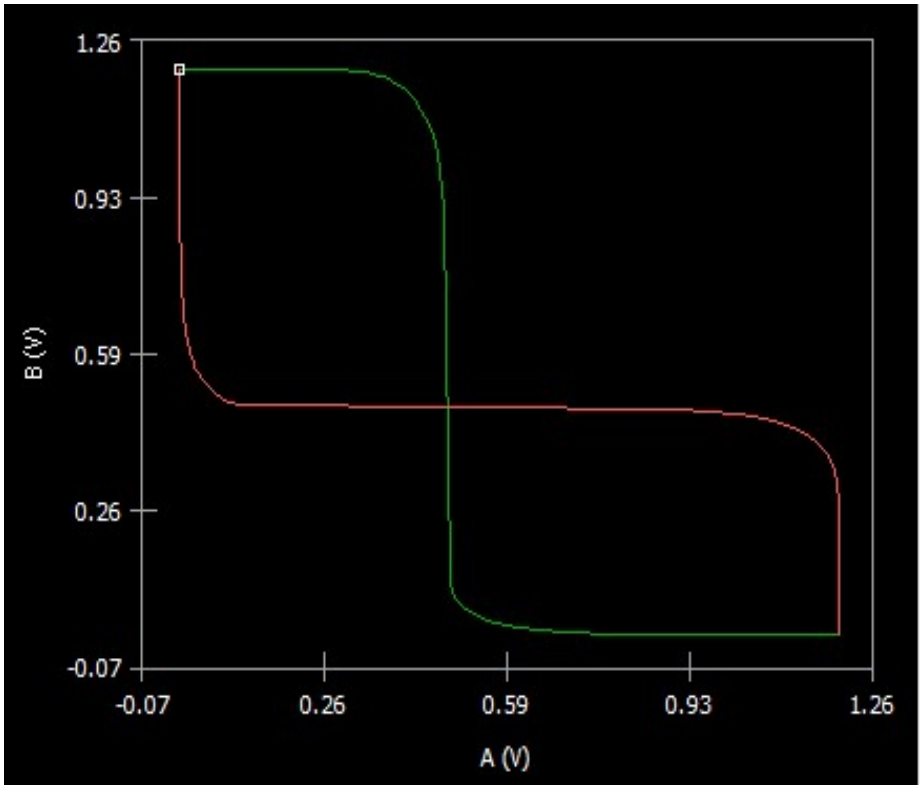


Figure 4.8. HSNM low power 8T SRAM cell.

4.6.2 Read Stability

The Read stability is measured by the read static noise margin (RSNM) in the SRAM Cell. In the low power 8T SRAM cell, due to storing nodes isolation, we get better RSNM comparable to conventional 6T SRAM and standard 8T SRAM cells. Figures 4.9, 4.10, and 4.11 represent the read stability of 6T SRAM, standard 8T SRAM, and low power 8T SRAM cells, respectively.

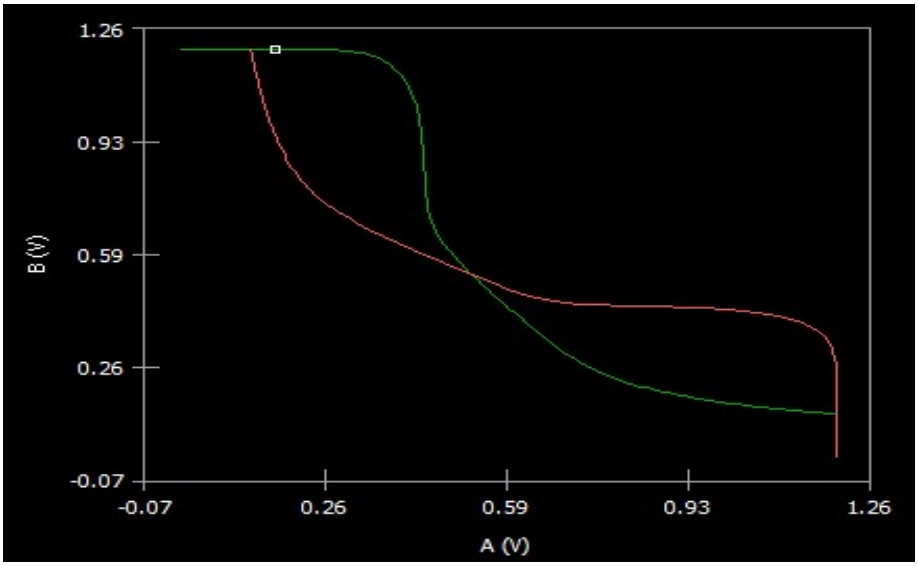


Figure 4.9. RSNM 6T SRAM cell.

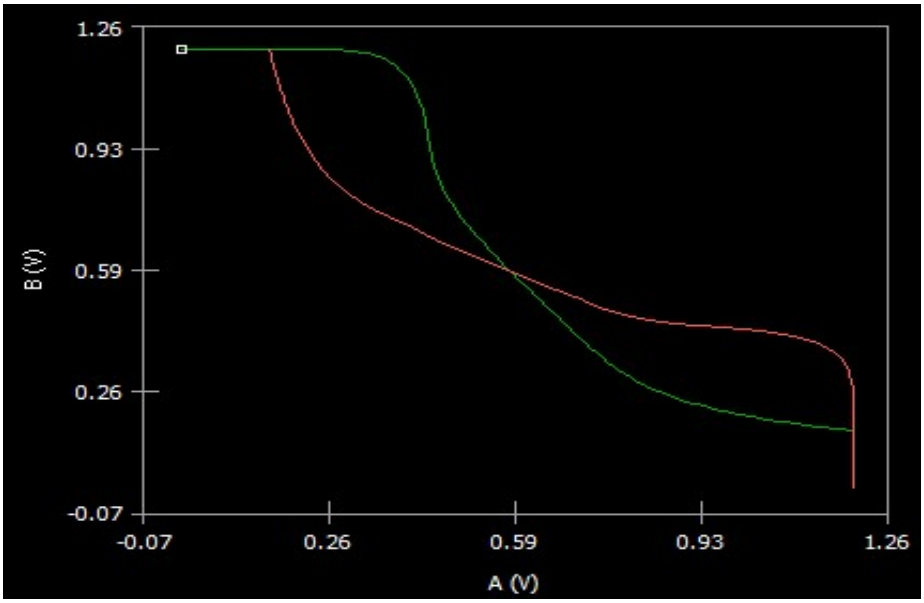


Figure 4.10. RSNM standard 8T SRAM cell.

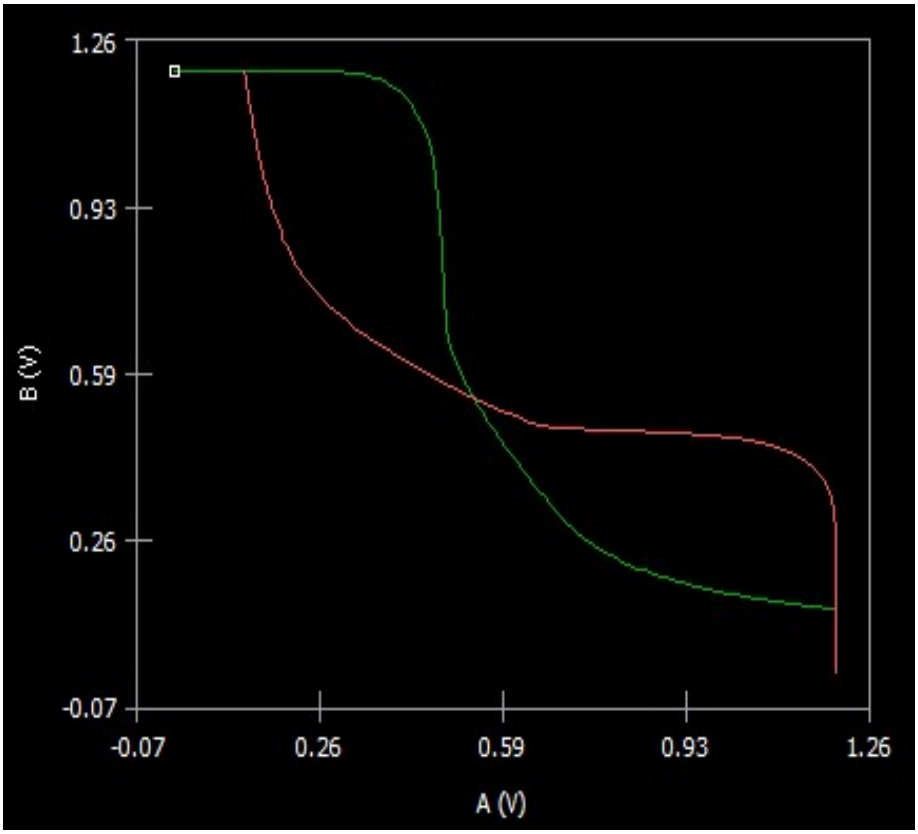


Figure 4.11. RSNM low power 8T SRAM cell.

Table 4.1 shows the hold static noise margin (HSNM) of 6T SRAM, standard 8T SRAM, and low power 8T SRAM cells, and the read static noise margin (RSNM) of 6T SRAM, standard 8T SRAM and low power 8T SRAM cells respectively.

Table 4.1: Comparison of Read SNM (RSNM) and Hold SNM (HSNM)

Cells	**RSNM** (in milli volts)	**HSNM** (in milli volts)
6T SRAM	71.1 mV	125 mV
Standard 8T SRAM	99.9 mV	125 mV
Low power 8T SRAM	100.0 mV	125 mV

4.6.3 Write Stability

The write stability is measured by write static noise margin (WSNM). In the low power 8T SRAM cell, due to storing nodes isolation, we get better WSNM comparable to conventional 6T SRAM and standard 8T SRAM cells. Figures 4.12, 4.13, and 4.14 represent the write stability of 6T SRAM, standard 8T SRAM, and low power 8T SRAM cells, respectively. Write trip point (WTP) is the measure of the write ability of the cell. It shows how difficult it is to the storing nodes of the cell. The bit-line voltage is swept from 0 to Vdd, and the flipping of the cell, when Q and Qbar flip their content, is captured. The value of bitline voltage at the crossing point of internal storage nodes Q and Qbar represents write trip point.

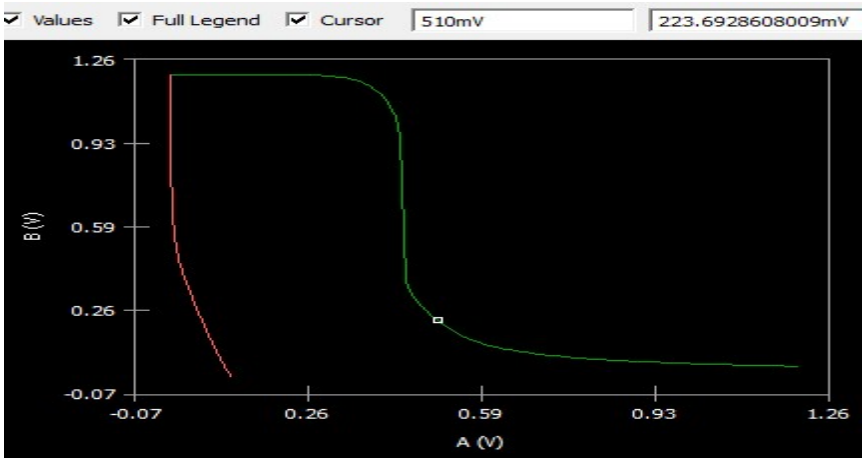


Figure 4.12. 6T SRAM write trip point (WTP).

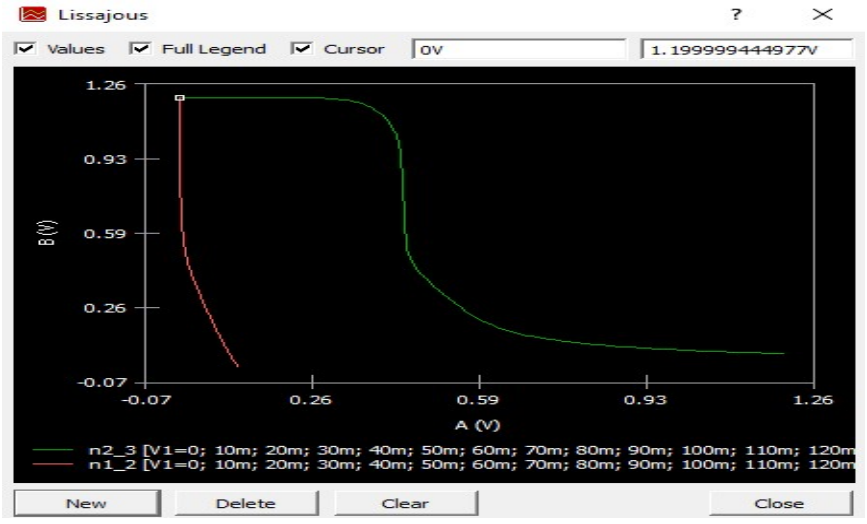


Figure 4.13. Standard 8T SRAM write trip point (WTP).

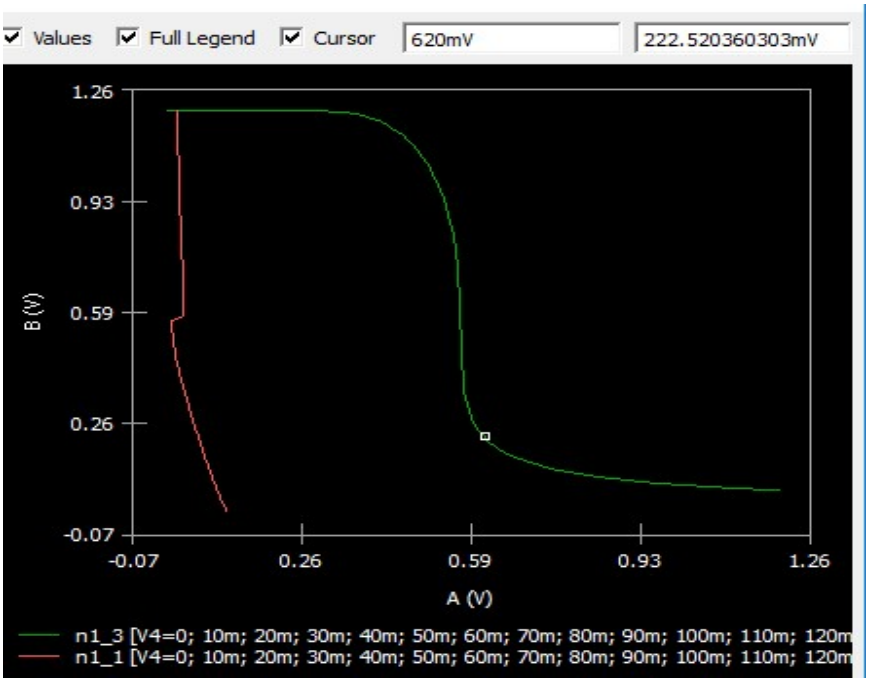


Figure 4.14. Low power 8T SRAM write trip point (WTP).

Table 4.2 The write stability is measured by write static noise margin (WSNM). In the low power 8T SRAM cell, due to storing nodes isolation, we get better Write trip point (WTP) comparable to conventional 6T SRAM and standard 8T SRAM cells. Table 4.2. represents the write stability of 6T SRAM, standard 8T SRAM, and low power 8T SRAM cells, respectively.

Table 4.2: Comparison for write trip point (WTP) of 6T SRAM and standard 8T SRAM, and low power 8T SRAM cells

Cells	**Write trip point (WTP)** (in milli volts)
6T SRAM	675 mV
Standard 8T SRAM	726 mV
Low power 8T SRAM	900 mV

4.7. SUMMARY

In this chapter, a low-power SRAM cell and swing node voltages are restored in the circuits. Static Random Access memory circuit techniques are presented in this study. This work is a comparative study analysis of 6T SRAM, standard 8T SRAM, and low power 8T SRAM cells in 130 nm Technology is also presented. This is the low power 8T SRAM cell and dual node voltage with swing restoration circuits, are perform stability analysis. hold, read, and write operations are good noise margin of the low power 8T SRAM cell is better than 6T SRAM and standard 8T SRAM cells. This conclusion is good because the power consumption is low for the SRAM cell. The low power 8T SRAM cell write mode operation, is power analysis, is better than 6T SRAM and standard 8T SRAM cells. Then the speed is higher for the low power 8T SRAM cell.

CHAPTER 5

LOW-LEAKAGE, HIGH-STABILITY SRAM CELL FOR IoT APPLICATIONS

The utility of a bit cell in SRAM is to store information, while its read and write operations are facilitated by the peripheral circuits. the design and characterization of a low-leakage, high-stability SRAM cell for IoT applications is crucial for the development of portable electronic devices. This study proposes a negative bit-line (NBL) write assist circuit and a separate (isolated) read port to improve the write and read stability of the SRAM cell, respectively. The proposed design has been compared to previous state-of-the-art work, and it has been shown that the WSNM has improved significantly, while the write latency has decreased, and faster operation. Thus, the following objective is framed to accommodate the aforementioned need –

"Design and Characterization of a Low-Leakage, High-Stability SRAM Cell for IoT Applications."

Methodology used to achieve the desired objective in the chapter is as follows -

- To address stability and delay difficulties in SRAM, a unique negative bit-line (NBL) circuit is proposed then put into action using an 8T SRAM cell.
- In the recommended architecture, one of the bit lines produces a negative voltage during the write operation (due to the NBL circuit), which enhances the access transistors' driving capacity and, as a result, the writing ability.
- To increase the cell's stability during read operation, a separate or isolated read port is employed.
- As a consequence, the suggested improvement has improved SRAM's stability and decreased its latency.

In this chapter, a low-leakage, high-stability SRAM cell for IoT Applications. This chapter is organized into ten sections, including an introduction to the Internet of Things (IoT), Section 5.1. In section 5.2, describe related work. Then section 5.3, proposed work. Further, the proposed design (NBL circuit with 8T SRAM cell) is presented in Section 5.4. In section 5.5, results and discussion. In section 5.6, static power dissipation. In section 5.7, write delay, section 5.8, read delay, and section 5.9, dynamic power dissipation. In section 5.10, the findings of the chapter are summarized.

5.1. INTRODUCTION TO THE INTERNET OF THINGS (IoT)

The rapid development of Internet of Things (IoT) technologies has significantly impacted various sectors, including healthcare. IoT-enabled biomedical devices hold tremendous potential to transform patient care by enabling real-time monitoring, diagnostics, and personalized treatment. A key factor in advancing these devices is optimizing memory systems, particularly Static Random Access Memory (SRAM), to meet the stringent requirements of low power consumption, high efficiency, and reliable operation [121]. Over the past five decades, the semiconductor industry has been driven by advancements in process technology, which have introduced new technologies every two to three years to meet the growing demand for better performance and functionality at lower costs [1]. All electronic systems, from mainframes to mobile phones, rely heavily on memory. Energy-efficient CPUs are becoming essential due to the increasing demand for battery-powered portable systems, with limitations in size, weight, and battery life affecting their performance. The integrated circuit (IC) design community is actively exploring new approaches to create power-efficient designs, leading to significant reductions in power consumption while maintaining the same level of performance, driven by reliability concerns, rising design costs, and the need for battery-operated systems. Memory circuits, which are integral to all system designs, contribute substantially to system-level power consumption, especially when using Dynamic RAM, SRAM, Ferroelectric RAM, ROM, or Flash memories. Reducing the power dissipation of memory systems can greatly enhance system performance, reliability, and cost. As the popularity of devices like laptops, mobile communication devices, and memory cards has risen, there has been significant progress in developing low-power, low-voltage memory designs for SRAM. Several strategies, including power gating, sleep mode, and voltage scaling, are employed to reduce power dissipation. Lowering the supply voltage (V_{DD}) reduces dynamic and leakage power, although it also lowers the noise margin. SRAM arrays are typically designed to minimize voltage swing and active capacitance, with gate leakage and sub-threshold leakage currents being the primary sources of leakage in sub-100 nm technologies. High dielectric constant gate technology helps reduce gate leakage, while binary threshold voltage (V_t) approaches and forward body biasing help minimize sub-threshold leakage. In sub-threshold SRAMs, the functional current is the sub-threshold leakage current, as the V_{DD} is lower than the transistor's threshold voltage (V_t) [2]. Memory, or storage, refers to the components and media that retain digital data used for

computation. Without sufficient memory, a computer would only be able to perform fixed operations and immediately produce results [3]. There are two main types of memory: volatile and non-volatile. Memory cells are organized in rows and columns within an array, with word lines as vertical connections driven externally and bit lines for data transfer. In read-write random-access memory (RW RAM), data is stored in flip-flop circuits or as charges on capacitors. This type of memory is volatile, meaning data is lost when the power is turned off. This study proposes a new SRAM cell with distinct write and single-ended read capabilities for IoT applications [121]. The proposed design uses a transmission gate as an access transistor to improve stability and voltage swing. The analysis of leakage power and stability for V_{DD} ranging from 0.9 V to 0.5 V shows superior performance compared to the current 5T and 6T SRAM cells at 32 nm technology. By separating the read line from the read disturbance problem, stability is improved [121]. The paper introduces an 8T SRAM cell design that features reduced swing voltage and decreased dynamic power dissipation, employing a pre-charge voltage technique with NMOS and PMOS transistors. The results show that the 8T SRAM cell outperforms the 6T SRAM in read, write, and hold modes, with increased static noise margins ensuring better write capability [90]. SRAM design inherently involves trade-offs between area cost, power consumption, and performance. The proposed design integrates a Negative Bit-Line (NBL) circuit with an 8T SRAM cell, resulting in specific trade-offs. While the NBL circuit enhances write stability and reduces quiescence, it adds extra transistors, increasing the overall area by 20% compared to conventional 6T SRAM cells. However, this area increase is offset by significant performance improvements, such as a 48% increase in Write Static Noise Margin (WSNM) and a 33% reduction in write delay. While the NBL circuit increases dynamic power during write operations, this trade-off is justified in applications where write stability and speed are crucial, such as low-voltage IoT devices. The proposed SRAM design addresses the key requirements of IoT applications, including ultra-low power consumption, wide temperature range operation, and high reliability. The integration of the NBL circuit with the 8T SRAM cell achieves significant power savings, with read power of 6.4 μW, lower than conventional SRAM designs, which is critical for extending battery life in IoT devices. Additionally, the proposed design demonstrates strong performance across a wide temperature range from -40°C to 120°C, maintaining stable noise margins essential for reliable data storage in varying environmental conditions.

5.2. PREVIOUS WORKS

Various strategies have been proposed to improve the stability and energy efficiency of SRAMs in modern low-power applications. The following discusses efforts to enhance both stability and energy efficiency in SRAMs. In the early days of electronics, systems were quite slow because memory speeds did not match the processor speeds. To address this, cache memory was introduced to boost the overall system speed. Today, cache memory is built on static random-access memory (SRAM). The number of SRAM cells on a single chip for a domain-specific architecture (DSA) is reaching hundreds of megabits. This creates two main challenges. The first challenge lies in the growing inefficiency of SRAM array utilization with the scaling of modern CMOS technologies. The second challenge is the static power dissipation caused by various leakage currents that flow from the higher V_{DD} through the SRAM cell to the lower V_{DD} [6]. These challenges highlight the need to design SRAM with minimal leakage, as this significantly reduces static power dissipation.

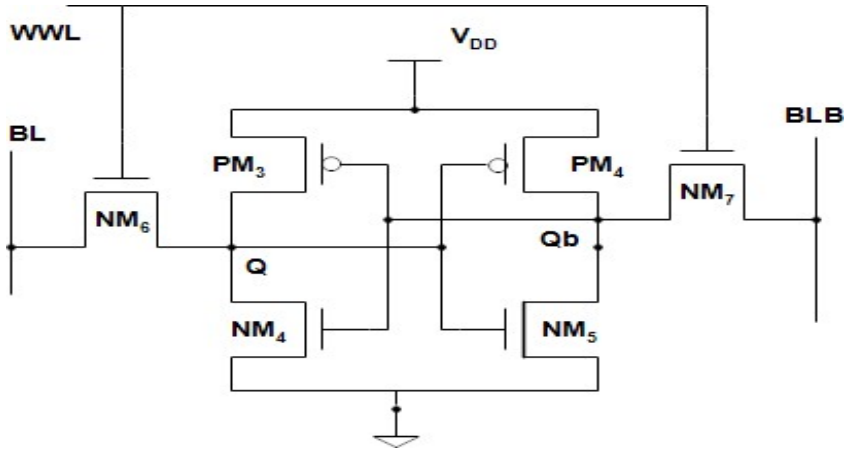


Figure 5.1. Basic 6T SRAM cell [11].

One proposed solution to the power issue is voltage scaling. The goal is to reduce the V_{DD}, but this introduces another challenge related to the reliability of the SRAM cell. Additionally, factors like data stability, delay, and high sensitivity to process variation also impact the overall performance of SRAM [7-12]. Figure 5.1 illustrates the basic 6T SRAM cell, which consists of four NMOS transistors (NM4, NM5, NM6, and NM7) and two PMOS transistors (PM3 and PM4). At the specified cell V_{DD}, the 6T SRAM cell faces several challenges, such as stability, delay, and high sensitivity to process variation [11]. The stability of the SRAM cell is mainly affected by the strength of the transistors that

form the internal latch and access transistors. To maintain writing capability, a weak pull-up transistor in the internal latch and a strong access transistor are required. For read stability, a strong pull-down transistor in the internal latch and a weak access transistor are needed [11]. During the write operation in the SRAM cell, the basic 6T SRAM cell experiences poor write capability due to disturbances in the node voltage when the cell V_{DD} is reduced [13]. Several write-assist techniques are used to improve the write capabilities of SRAM cells. Among the popular methods are negative bit-line, V_{DD} collapse, boosted V_{SS}, and word-line boosting [14-18]. The negative bit-line write assist technique, proposed by Y.H. Chen et al. [16] involve using a negative voltage on the bit lines instead of ground. This increases the gate-to-source voltage (V_{GS}) of the access transistors, which enhances their driving capacity without affecting the external latch. However, this approach also increases the bit-line capacitance through a boosted capacitor, which ultimately leads to an increase in access time [16].

In contrast, the V_{DD} collapse method, proposed by E. Karl et al. [17], involves reducing the internal latch voltage during a write operation to improve the write capability. However, this reduction in cell V_{DD} disturbs the stored node voltage, which can lead to data loss during read or hold operations. In the boosted word-line write assist method [18], the word-line voltage is increased, which raises the gate-to-source voltage of the access transistors and consequently increases static power dissipation. This makes it unsuitable for low-voltage operations. Furthermore, B. Wang et al. [19] and other researchers have proposed ultra-low voltage 9T SRAM cells to reduce static power dissipation and enhance read/write operations [20]. To enable SRAM to operate stably under low voltage (V_{DD}) [21], under-driven word-line (WL) read assist circuits and negative bit-line (NBL) write assist circuits are typically used.

However, NBL consumes significant energy, and the slow read assist function of WL impacts performance. Voltage-boosted fail-detection circuits for selective write assist (VBFD-SWA) and selective cell current boosting (VBFD-SCCB) have been proposed for high-performance, low-power FinFET SRAMs. VBFD-SWA detects the bit-line state and triggers NBL only when a write failure is detected, reducing energy consumption during write operations. VBFD-SCCB detects slow bit cells and selectively activates cell current boosting to improve read performance. This study introduces a reconfigurable negative bit-line collapsed force (RNBLCS) write driver circuit for the 9T Schmitt detector-grounded SRAM cell (9T-ST), significantly improving write performance for real-time memory

operations. In deep sub-micron technology, increasing device parameter variations significantly reduces SRAM cell write capability. The proposed Low V_{th} UDVS SRAM cell, demonstrated with low-threshold voltage transistors and ultra-dynamic voltage scaling circuits in 16 nm low-leakage CMOS technology, offers a wide operating voltage range through optimized circuits for both subthreshold and above-threshold ranges. This write assist method enables write capability at very low voltage levels while minimizing power consumption. Simulation results show that with 16 nm technology, write capability improves by 33% at 0.9V operating voltage.

1. To address stability and delay challenges in SRAM, a novel negative bit-line (NBL) circuit is proposed and implemented using an 8T SRAM cell.
2. In this design, one bit line generates a negative voltage during the write operation, enhancing the access transistors' driving capacity, thereby improving write capability.
3. Increase stability during the read operation; a separate, isolated read port is employed.
4. As a result, the proposed enhancement improves cell stability and reduces leakage power.

5.3. NEGATIVE BIT-LINE GENERATOR CIRCUIT (NBL)

The negative voltage is applied to one of the bit lines (BL or BLB) of the SRAM cell, thereby influencing the gate-source voltage (V_{GS}) of the access transistor. The primary function of the NBL circuit is to provide a negative voltage to the BL/BLB of the SRAM cell instead of 0V, depending on the operating conditions. Figure 5.2(a) illustrates the proposed NBL creator circuit, which includes four NMOS transistors, three PMOS transistors, and two NOR gates. In the NBL circuit, the signals Din, Dinb, and W_R serve as inputs to the NOR gate, and the output of the NOR gate is connected to the inputs of the NMOS and PMOS transistors [127].

The NBL circuit operates as follows:

Case I: The NBL circuit is in write mode when a "1" signal is applied. When "1" and "0" are applied to the Din and Dinb signals, respectively, and "0" is applied to W_R in a write "1" operation, the NOR gate's output will always reflect the inverted Din and Dinb signals. Consequently, NOR1 and NOR2 output "0" and "1" respectively. This causes transistor NM1 to turn off, while NM2 turns on. Additionally, PM1 turns on, and PM2 turns off. As a result, the bit-line (BL) will be set to a high voltage (V_{DD}), while the bit-line bar (BLB) state will depend on the statuses of the W_E and W_{EN} signals.

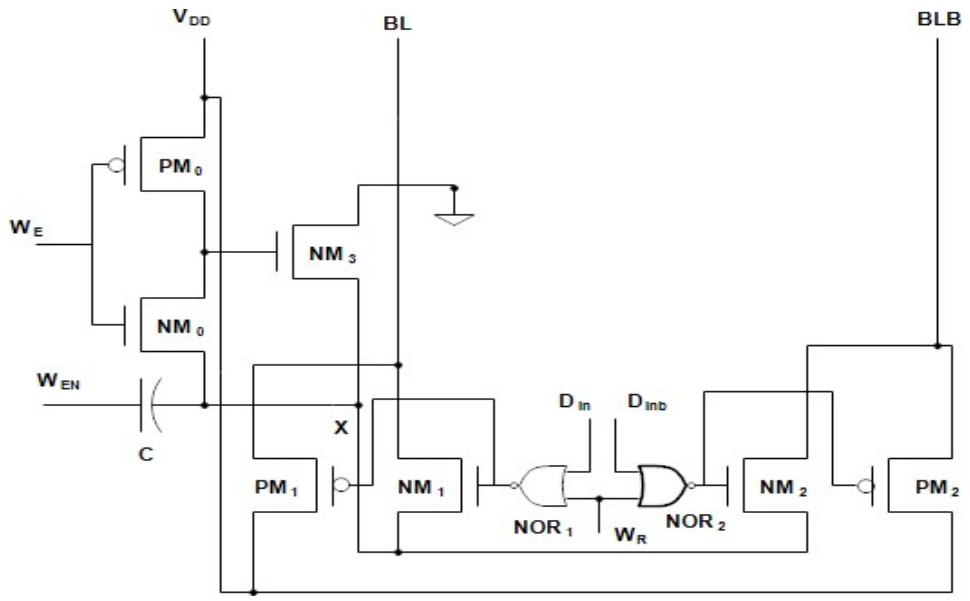


Figure 5.2(a). Circuit of negative bit line generator [127].

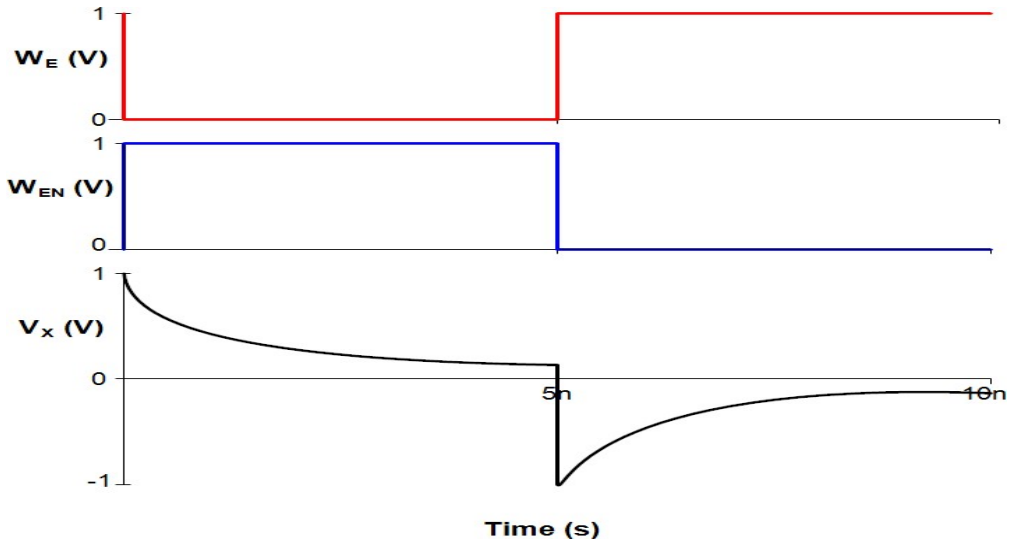


Figure 5.2(b). Output voltage at node X [127].

Case A: When the W_{EN} signal is at "1" and the W_E signal is at " 0", as shown in Figure 5.2(b) [127], the transistor NM0 is turned off, and PM0 is turned on. This also activates transistor NM3. The ON transistor NM3 operates in the triode region, providing resistance across it. The RC network consists of a capacitor (C) and the resistance (R_{ON}) of transistor NM3, and the circuit functions as an RC differentiator. Since the W_{EN} signal initially rises steeply at the positive edge, the capacitor behaves like a short circuit, making the input

voltage (W_{EN} signal voltage) and the voltage at knot X across (R_{ON} or V_X) equal. After the positive edge, when the W_{EN} signal reaches "1" the capacitor begins charging through R_{ON}. As the capacitor charges, the voltage at knot X (V_X) rapidly decreases as shown in Figure 5.2(b) [127], with the charging speed determined by the time constant $R_{ON}C$. In this case, the voltages at BLB and V_X are the same.

Case B: When the W_{EN} signal is at "0" and the W_E signal is at "1", the transistor PM0 is turned off by the W_E signal, and transistors NM0 and NM3 are turned on. The capacitor, which prevents sudden voltage changes, keeps the gate of NM3 connected to knot X through NM0. This creates an RC network, similar to Case A. The negative edge of the WEN signal, which drops steeply, causes the capacitor to not respond well to fast changes, resulting in a negative spike. As the W_{EN} signal reaches "0" after the negative edge, the capacitor discharges. As it discharges, the voltage at knot X (V_X) increases exponentially as seen in Figure 5.2(b) [127], with the discharging speed dependent on the time constant $R_{ON}C$. Therefore, in this case, the voltage at BLB becomes negative or equal to V_X.

Case II: When performing a write "0" operation, the Din and Dinb signals are at "0" and "1" respectively, while "0" is applied to W_R. The outputs of NOR1 and NOR2 gates are "1" and "0" respectively. As a result, transistor NM1 turns on, and NM2 turns off. Meanwhile, transistors PM1 and PM2 turn on and off, respectively. Consequently, BLB switches to "high" (V_{DD}), and the state of the bit-line (BL) depends on the W_E and W_{EN} signal conditions, similar to Cases A and B mentioned for Case I. When W_{EN} is at "0" the bit-line (BL) will receive a negative voltage.

Case III: During a read-and-hold operation, the NOR gate consistently outputs a zero, which turns on the PMOS transistors (PM1 and PM2) and turns off the NMOS transistors (NM1 and NM2). The W_R signal remains at "1" during read-and-hold operations, causing the NOR gate to output zero regardless of the Din and Dinb values. PMOS transistors (PM1 and PM2) connect the BL or BLB to V_{DD}. The previous Cases A and B do not affect the read-and-hold operation, as the NMOS transistors (NM1 and NM2) are off and knot X is disconnected from the bit-lines (BL/BLB). Since the bit-lines (BL/BLB) are switched to V_{DD} during the read-and-hold operation, the proposed NBL circuit applies a negative voltage to one of the bit-lines (BL/BLB) only during the write operation [122].

5.4. PROPOSED DESIGN (NBL CIRCUIT WITH 8T SRAM CELL)

The proposed design, which incorporates an NBL circuit with an 8T SRAM cell, is illustrated in Figure 5.3. An 8T SRAM cell consists of eight transistors. The SRAM's internal latch, responsible for storing data, is created using transistors NM4, NM5, PM3, and PM4. The separate read path, used for retrieving data from the SRAM cell, is formed by transistors NM8 and NM9. The data storage nodes of the SRAM cell are referred to as node Q and node Qb. Transistor NM9 acts as the access transistor during a read operation, triggered by the read word line (RWL) signal, while transistors NM6 and NM7 serve as write access transistors. The read bit line (RBL) functions as both an input and output line during read operations, while the bit lines (BL/BLB) are used as inputs during write operations.

The following explains the different operations of the proposed design.

5.4.1 Write Operation

Figure 5.4(a) illustrates the circuit behavior during write operations (with a dashed line representing an OFF transistor). The WWL signal is set to "1" for the write operation, activating the access transistors NM6 and NM7. For the write "1" operation at node Q, the states at Qb and Q are initially set to "1" and "0" respectively.

1. Initially, nodes Q and Qb store "1" and "0" independently.
2. The bit lines, BL and BLB, are set to "1" and "0" respectively.

In the proposed design, the NBL circuit is connected to the bit lines. The WR signal is at "0" for the write operation in the NBL circuit, while the Din and Dinb signals are at "1" and "0" independently. As a result, BLB is driven to a negative voltage, while BL is driven to VDD (as discussed in Section 5.3.1).

The negative voltage at BLB increases the gate-to-source voltage (VGS) of the access transistor NM7, which boosts NM7 driving capability. As a result, node Qb quickly discharges and reaches 0V because transistor NM7 operates faster than transistor NM6, as shown in Figure 5.4(a). This causes transistor PM3 to turn on and transistor NM4 to turn off. Consequently, transistor PM3 connects the storage node Q to VDD, where it stores the "1" value.

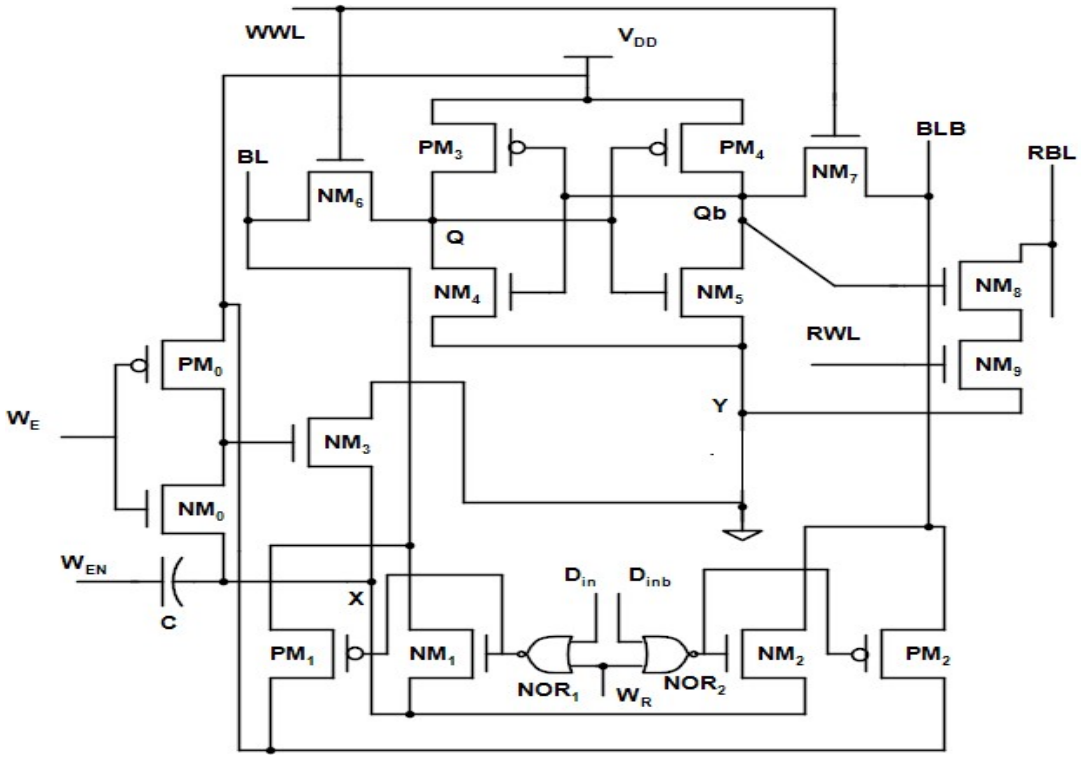


Figure 5.3. Proposed Design.

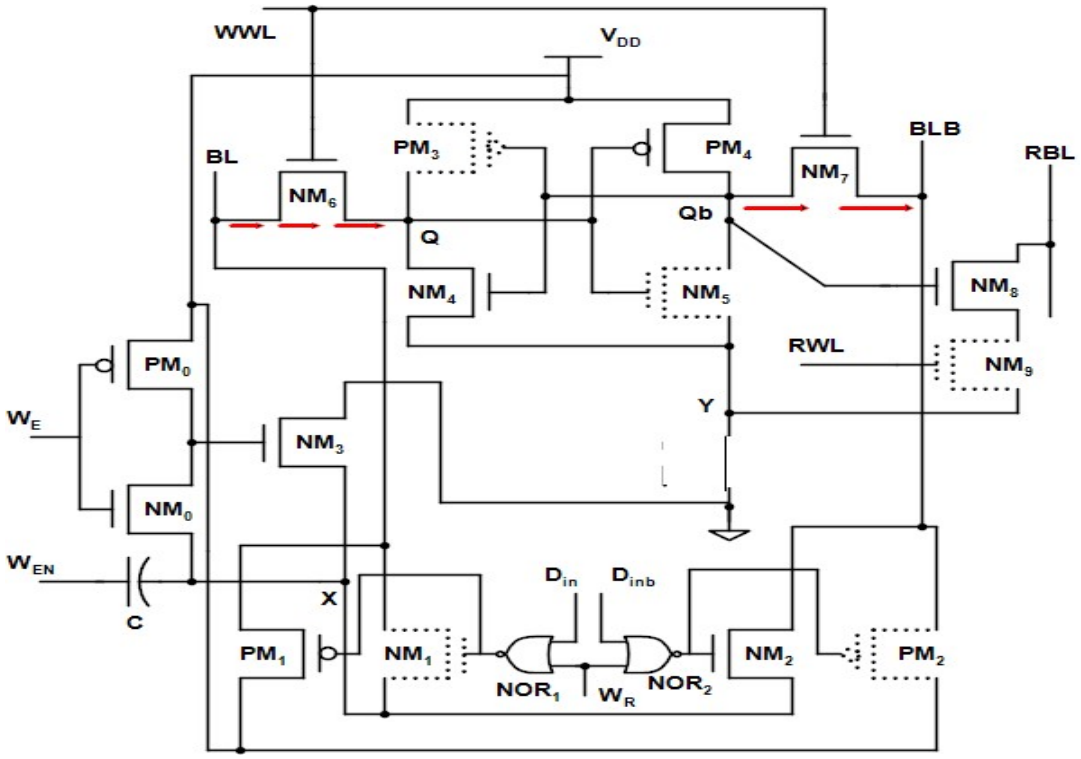


Figure 5.4(a). Proposed design during write operation.

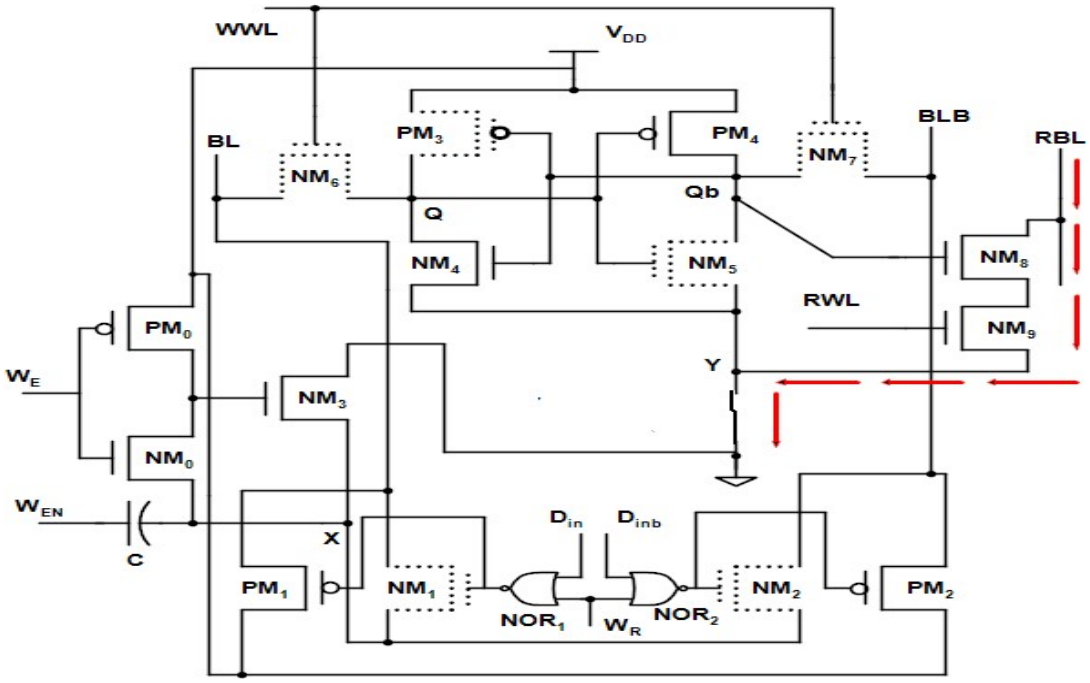


Figure 5.4(b). Proposed design during read operation.

5.4.2 Read Operation

Figure 5.4(b), illustrates the circuit behaviour of the proposed design during a read operation (with OFF transistors indicated by a dotted line). The output of the NOR gate is always at a low voltage, activating the PMOS transistors because the W_R signal must always be at "1" for reading data from the SRAM cell. As a result, the bit lines (BL or BLB) are consistently set to "1". During a read operation, RBL is pre-charged to "1", with the WWL signal at "0" and the RWL signal at "1", and so on. Initially, nodes Q and Qb store "0" and "1" for a read "0" operation. Transistor NM8 is activated due to the "1" stored at node Qb, which is connected to the gate of NM8 as shown in Figure 5.4(b). Together with transistors NM8 and NM9, a path (represented by an arrow) is created between RBL and ground, discharging RBL to 0V. This completes the read "0" operation.

5.4.3 Hold Operation

During the hold operation, the access transistors NM6, NM7, and NM9 are turned off because the RWL and WWL signals are kept at "0". The bit lines (BL, BLB) and RBL remain at "1" as the W_R signal in the NBL circuit stays at "1". The internal latch of the SRAM cell is disconnected from the bit lines in the hold mode, preserving the data. However, a significant amount of static power is lost during this mode due to leakage currents, particularly sub-threshold leakage currents, since most of the transistors remain in the OFF state. To address this, the proposed design minimizes static power dissipation.

The NM9 transistor generates a voltage drop, which reduces the drain-to-source voltage (V_{DS}) of the OFF transistors (NM5 and NM9). The gate-to-source voltage (V_{GS}) of these transistors effectively becomes zero due to NM9 being in the OFF state. As a result, the threshold voltage of NM5 increases, while the threshold voltage of NM9 remains unchanged.

5.5. RESULTS AND DISCUSSION

The performance of the proposed design has been evaluated using the Cadence Virtuoso tool for circuit design, operating at a 1V supply voltage and simulating the UMC 28nm CMOS technology node. The area of the proposed 8T SRAM design and the Negative Bit-Line (NBL) generator circuit were estimated using Virtuoso layout tools. The proposed SRAM cell occupies roughly 20% more area compared to the conventional 6T SRAM due to the additional transistors and separate read path configuration. The NBL generator circuit, which consists of multiple PMOS and NMOS transistors along with sense gates, adds another 15% area when integrated with the SRAM array. As a result, the total area of the proposed design is approximately 35% larger than that of the standard 6T SRAM cell. This increase in area is justified by significant improvements in write stability, reduced quiescence, and enhanced noise margins, though it may present limitations in area-constrained applications.

The following are the simulation results for various performance parameters of the proposed design:

5.5.1 Write ability

The stability of the SRAM cell is defined by the maximum noise voltage that cannot flip the state of the storage node in the SRAM cell. Write Static Noise Margin (WSNM) is used to define the write capability of the SRAM. This method involves sweeping the voltage at one node (Q) from 0V to V_{DD} and plotting it against the corresponding voltage at the other node (Qb) to create the Voltage Transfer Characteristic (VTC) curve. The process is then repeated by sweeping the voltage at node Qb from 0V to V_{DD} and generating a similar VTC at node Q. The two VTC curves are combined into a visual known as a butterfly plot. The WSNM [123-124] value is determined by the largest perpendicular distance from the plot's curve to the origin, where the widest region represents the WSNM. Figure 5.5 shows the butterfly plot for calculating the write-functional WSNM value of the proposed design at a 1V supply voltage and 27°C temperature with TT corner. When compared to an 8T SRAM cell without the NBL circuit, the proposed design achieves a WSNM of 490 mV.

The 8T SRAM cell with the NBL circuit improves the WSNM by 1.53 times over the SRAM cell without the NBL circuit, making it beneficial to include this feature.

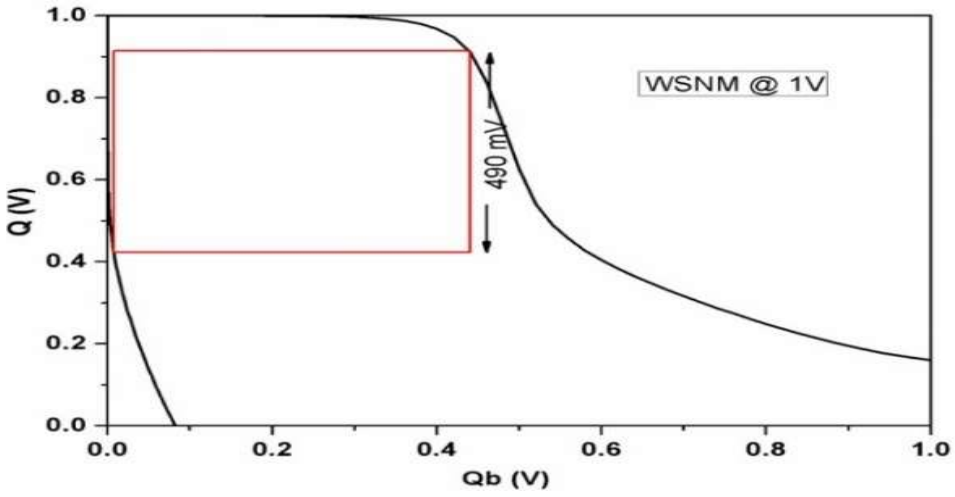


Figure 5.5. Butterfly curve for write stability.

Figure 5.6 presents a comparison of the proposed design with the standard 6T SRAM cell, the V_{DD} collapse write assist technique, the NBL write assist method, and the 9T UV SRAM cell at various cell VDDs. Due to the higher likelihood of data flipping in SRAM cells at lower V_{DD}s, it is observed that WSNM increases with V_{DD}.

Therefore, the cell is more stable at higher V_{DD}s than at lower ones. At a 1V operating voltage using the same technology node, the WSNM of the proposed design is improved by 48%, 11%, 19%, and 32.4% compared to the standard 6T SRAM cell [11], NBL [16], V_{DD} collapse [17], and 9T UV SRAM [19], respectively. This improvement is attributed to the ability of the negative bit-line to enhance the gate-to-source voltage (V_{GS}) of the access transistor. Figure 5.7 shows the WSNM of the proposed design at different temperatures. As the temperature increases from -40°C to 120°C at 1V, the WSNM of the proposed design decreases from 580 mV to 430 mV, due to the reduction in threshold voltage with increasing temperature.

The proposed SRAM design introduces a novel approach by strategically integrating the Negative Bit-Line (NBL) circuit with an 8T SRAM topology, optimized for low-power and high-stability operations. Unlike traditional designs, the NBL circuit in this configuration improves the gate-to-source voltage during write operations, significantly enhancing write stability without sacrificing read stability.

Additionally, the isolated read path design minimizes read disturbances, resulting in better read noise margins compared to conventional 6T and 9T SRAM cells. This design specifically addresses challenges such as voltage scaling and leakage currents, which degrade performance in sub-28 nm technology nodes. The impact of this innovation is validated through extensive simulations, demonstrating a 48% improvement in write static noise margin (WSNM) and a 33% reduction in write latency compared to state-of-the-art designs.

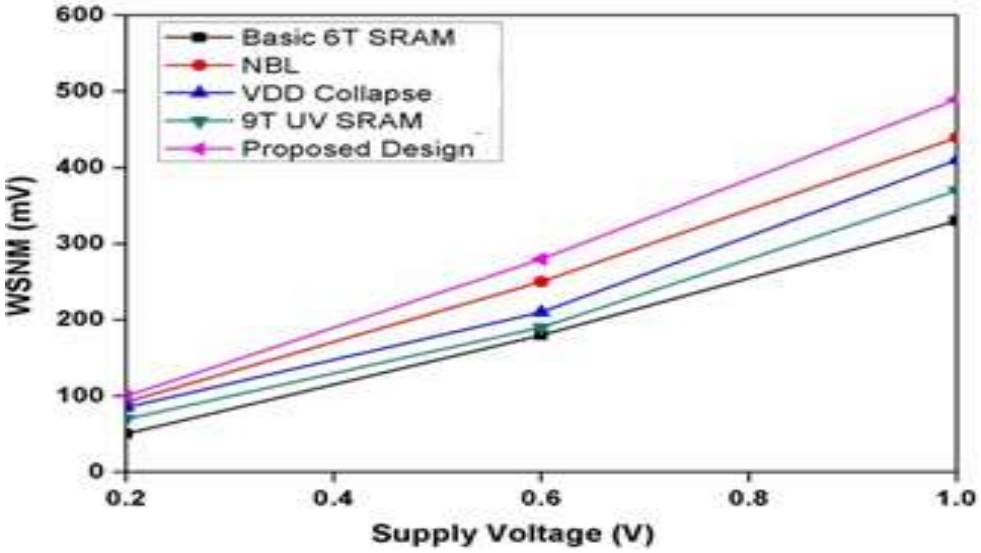


Figure 5.6. Variation in WSNM vs supply voltage.

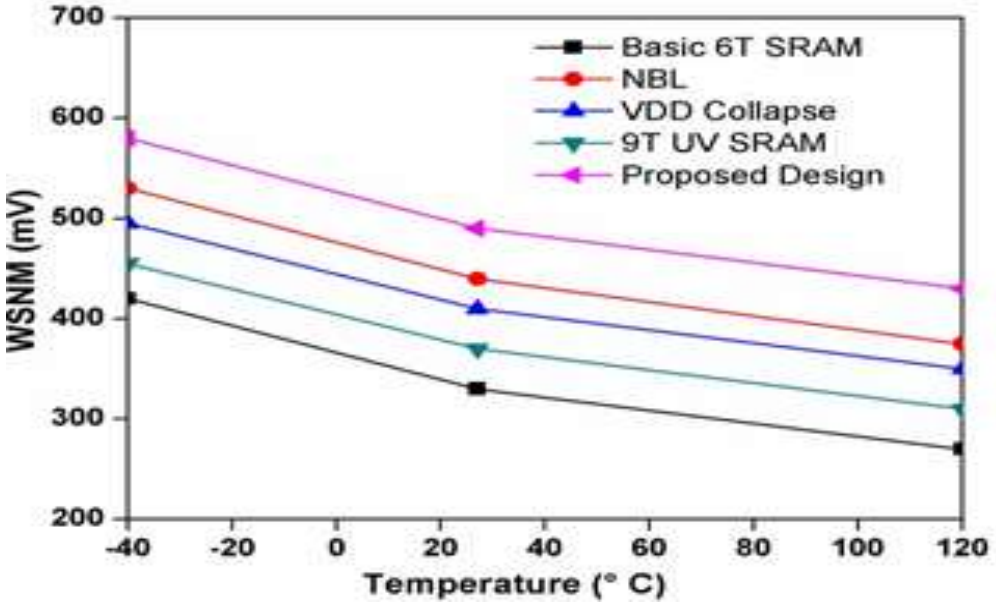


Figure 5.7. Variation of WSNM vs temperature.

As a result, the data values in the SRAM cell degrade, making the cell less stable at higher temperatures. However, when comparing the proposed design to the standard 6T and other current designs, as shown in Figure 5.7, the proposed design maintains stable WSNM performance even with increasing temperature.

To evaluate the yield of the proposed design, a Monte Carlo simulation was used to assess the effects of process variation and mismatch. The simulations were performed with a 10% variation in transistor length (L) and width (W), and a ±50 mV variation in threshold voltage (V_{th}), reflecting typical manufacturing variations in 28 nm CMOS technology. The conditions for the simulations included a 1V supply voltage and a temperature range from -40°C to 120°C. A total of 200 Monte Carlo runs were performed to balance statistical accuracy and computational efficiency, as further runs beyond 200 did not significantly affect the results. The simulation showed that the proposed design is less sensitive to process variations and mismatches, with a standard deviation (σ) of 0.09V for the Write Static Noise Margin (WSNM) and a mean value (μ) of 490 mV, resulting in a variability ratio (σ/μ) of 0.18, confirming the robustness of the design, as shown in Figure 5.8.

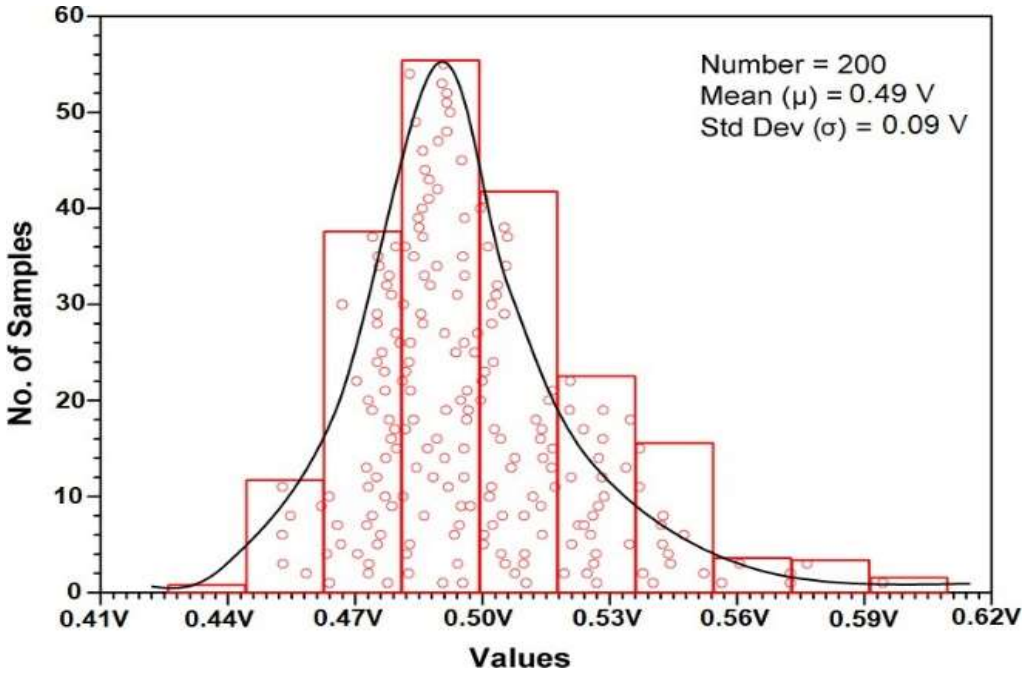


Figure 5.8. Monte Carlo of WSNM for proposed design.

5.5.2 Read Stability

The proposed SRAM design exhibits an improved Read Static Noise Margin (RSNM) compared to the Hold Static Noise Margin (HSNM), owing to the specific configuration

and functional characteristics of the circuit. The isolated read storage utilized in the design effectively separates the read operation from the storage elements, minimizing the impact of read-induced noise and improving the RSNM. In contrast, during the hold mode, the SRAM cell depends on internal feedback mechanisms that are more susceptible to noise and leakage currents, particularly at lower voltages and higher temperatures.

Additionally, the Negative Bit-Line (NBL) circuit enhances write stability but does not directly affect hold stability, further explaining the observed difference. While this design choice improves overall read stability, it results in a slightly lower HSNM due to the inherent vulnerabilities of the hold state. The read stability of the SRAM cell is characterized by the RSNM, which is measured using the butterfly plot [125]. The butterfly plot for read stability during the read operation is shown in Figure 5.9. The side length of the square formed within the lower lobe of the butterfly plot is used to estimate the RSNM value for the proposed design. It should be noted that the RSNM value for the proposed design is 400 mV at 1V for the cell.

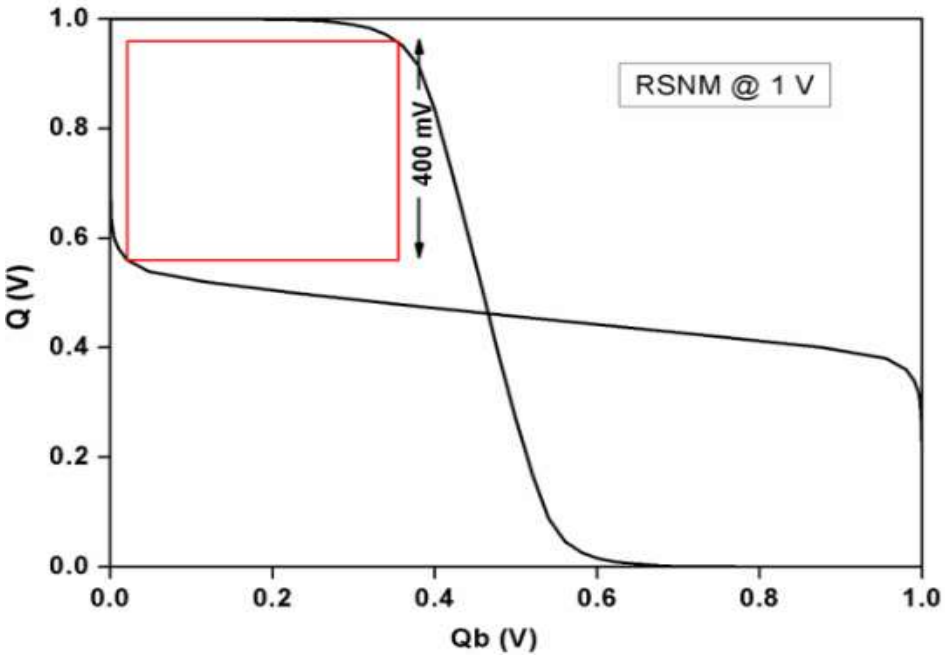


Figure 5.9. Butterfly curve for the read stability.

Figure 5.10 illustrates the change in RSNM values for the proposed design and previous published studies across various cell VDDs. At lower VDD, the RSNM is very low, but it increases as the voltage rises. Notably, the proposed design shows an improvement in RSNM by 81, 42, and 29 compared to the initial 6T SRAM cell [11], NBL [16], and VDD

collapse [17], respectively. However, it shows a decrease of 4.8 compared to the 9T UV SRAM [19] when designed at 1V using the same technology node.

The proposed design achieves this RSNM improvement through the use of a dedicated or isolated read storage. During the read operation, the WWL signal is set to "0", effectively isolating the storage elements from the bit lines (BL/BLB). This ensures that there is no disturbance or degradation of the data held in the storage nodes (Q/Qb), resulting in stable read performance. The RSNM values of the proposed design are shown in Figure 5.11, across various temperatures. As temperature increases, the lower threshold voltage of the transistors causes the RSNM value to decrease. Furthermore, Figure 5.11, compares the proposed design with other SRAM designs, showing that it delivers the best results for read operations at a specific temperature.

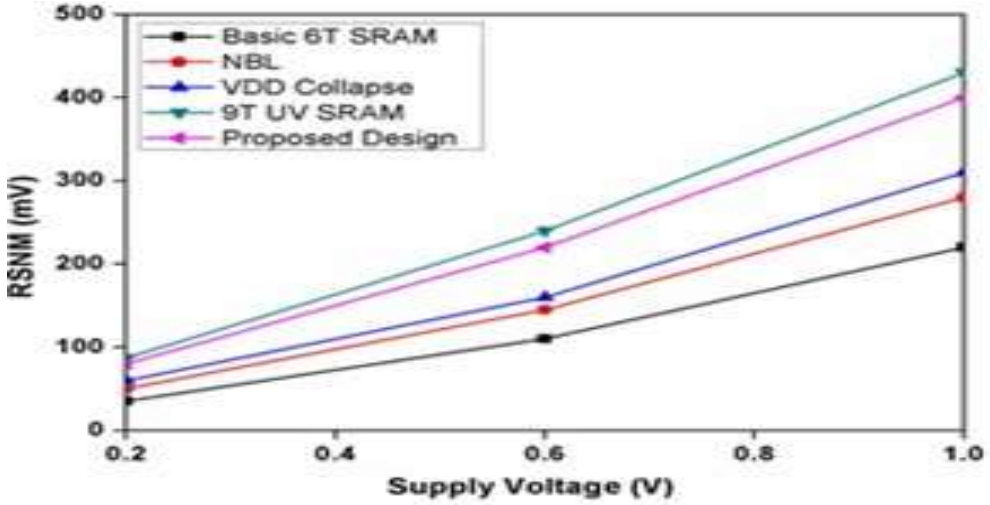


Figure 5.10. Variation of RSNM vs supply voltage.

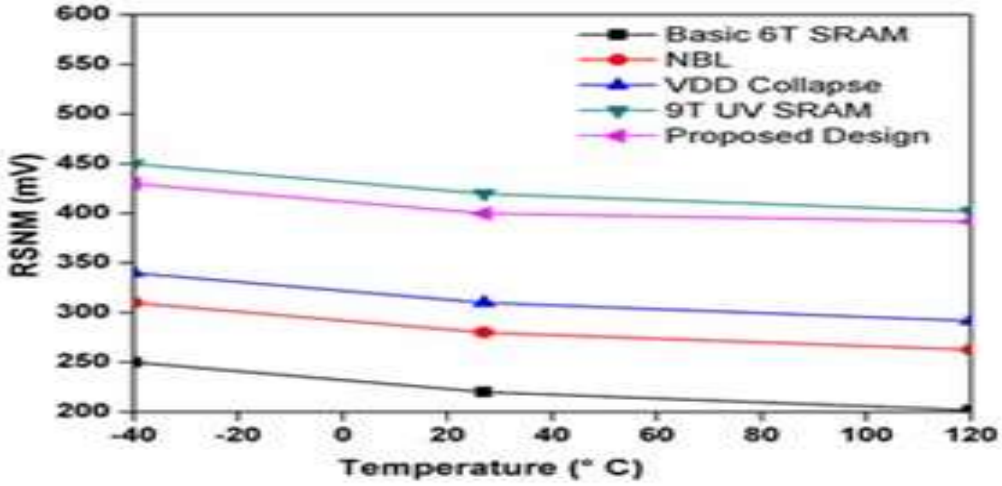


Figure 5.11. Variation of RSNM vs temperature.

5.5.3 Hold Stability

The Hold Static Noise Margin (HSNM) is used to evaluate the stability of the SRAM cell in hold mode. This is measured using the butterfly plot, as shown in Figure 5.12. The HSNM value for the proposed design is noted to be 350 mV at 1V for the cell.

Figure 5.13 compares the HSNM values of the proposed design with those of other existing designs across various cell V_{DD}s. In the hold mode of the proposed design, the internal latch is isolated from the bit lines, preventing data loss and enhancing the stability of the SRAM cell in hold mode. The proposed design shows improvements in HSNM of 28, 13, 40, and 8.5 compared to the initial 6T SRAM cell [11], NBL [16], VDD collapse [17], and 9T UV SRAM [19], respectively, when designed at 1V using the same technology node. Figure 5.14 shows the HSNM of the proposed design across different temperatures. It has been observed that the HSNM value decreases as the temperature increases from -40°C to 120°C at 1V. A comparison between the proposed design, the initial 6T SRAM cell, and other cutting-edge designs is also presented, indicating that the proposed design outperforms other designs in terms of HSNM across a range of temperatures.

The proposed SRAM design incorporates transistor mounding to significantly reduce leakage currents compared to traditional 6T and 8T SRAM cells. This technique increases the effective threshold voltage and minimizes sub-threshold leakage, particularly in low-power conditions. To provide leakage current measurements for the proposed design and other SRAM configurations, showing a leakage reduction of 44.4% compared to the standard 6T cell and 26.7% compared to the proposed 8T cell with NBL circuits. These results validate the effectiveness of the mounding approach, making the proposed design highly suitable for IoT applications, where minimizing leakage is crucial for extending battery life and preserving data integrity.

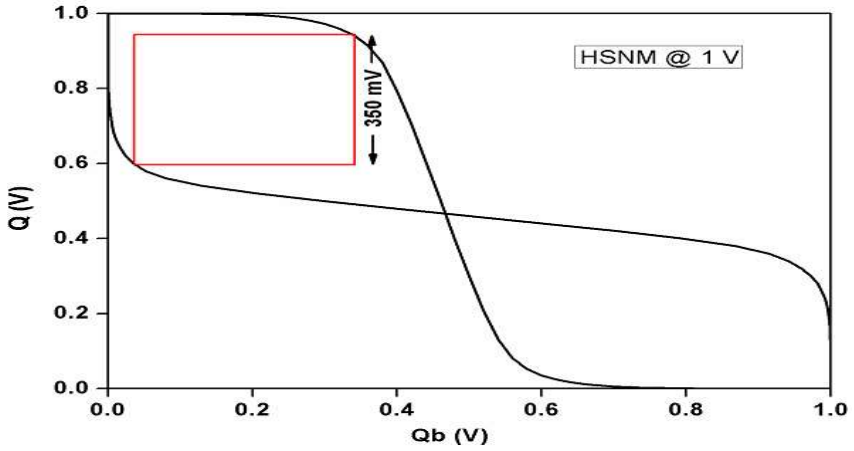


Figure 5.12. HSNM of proposed design.

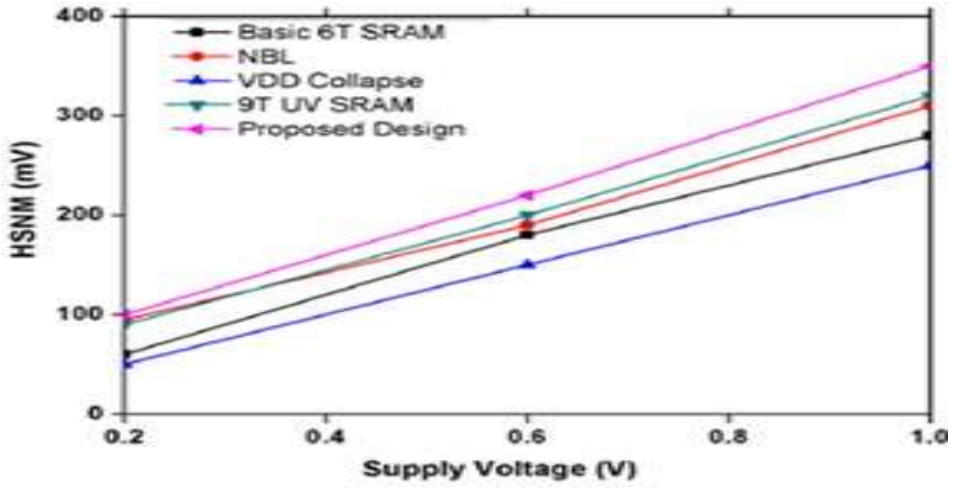


Figure 5.13. Variation of HSNM vs supply voltage.

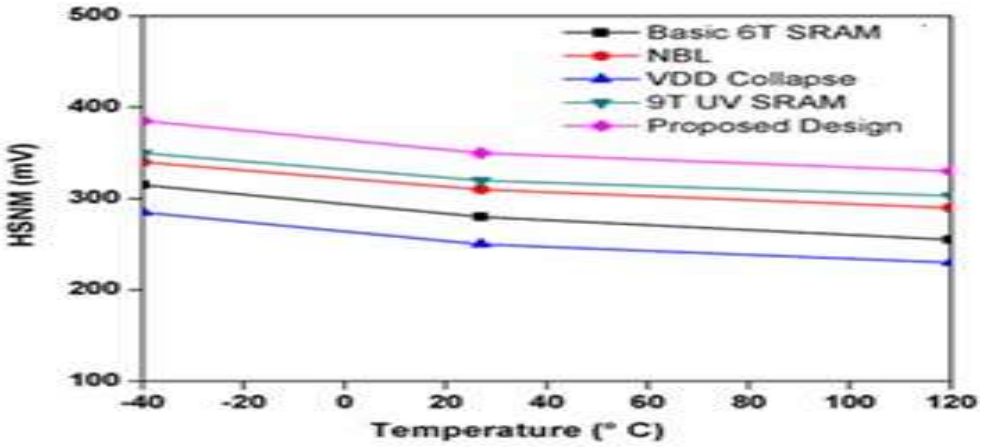


Figure 5.14. Variation of HSNM vs temperature.

5.6. STATIC POWER DISSIPATION

At smaller technology nodes, SRAM cells encounter the issue of static power dissipation, primarily caused by various leakage currents within the circuit. These leakage currents include sub-threshold leakage, junction leakage, and gate leakage, among others [126].

Figure 5.15 illustrates the static power dissipation of the proposed design at different V_{DDs}. Static power dissipation increases as the V_{DD} of the cell is raised. The proposed design's static power dissipation is 430 pW at a cell V_{DD} of 1V, compared to 190 pW for an 8T SRAM cell and 240 pW for an NBL circuit. The proposed design is also compared to other advanced designs and a simple 6T SRAM cell. It is observed that the proposed design consumes 30%, 11%, and 20% more power than the initial 6T SRAM cell [11], V_{DD} collapse [17], and 9T UV SRAM [19], respectively, while consuming 17% less power than the NBL [16] at 1V. The slightly higher static power dissipation in the proposed design is

due to the operation of a single NBL circuit. However, combining one NBL circuit with multiple SRAM cells can reduce static power dissipation.

Figure 5.16, shows the variation in static power dissipation at different temperatures. Since sub-threshold leakage current exponentially depends on temperature and threshold voltage, the proposed design experiences increased power loss as temperature rises. As the temperature increases, the threshold voltage decreases, which in turn increases sub-threshold leakage current. Consequently, the proposed design experiences higher static power dissipation at elevated temperatures.

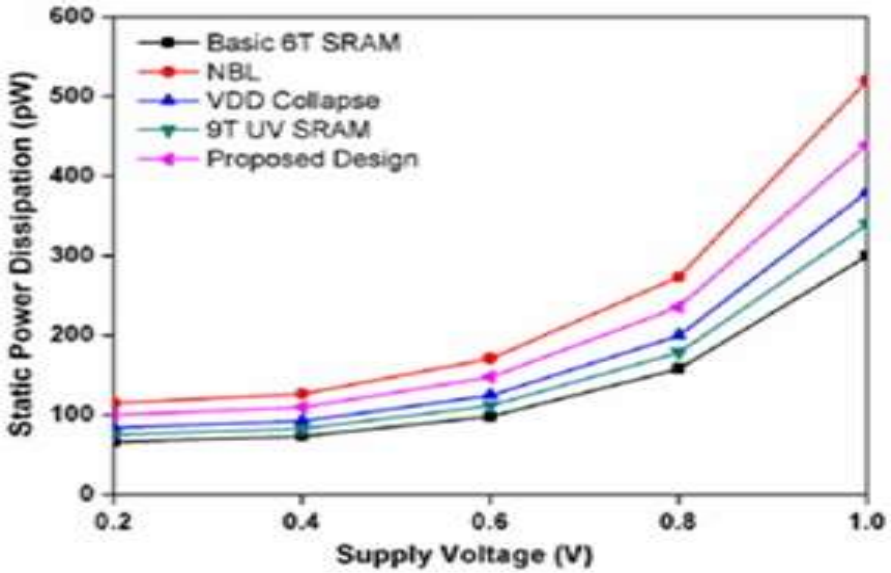


Figure 5.15. Static power dissipation at various VDD.

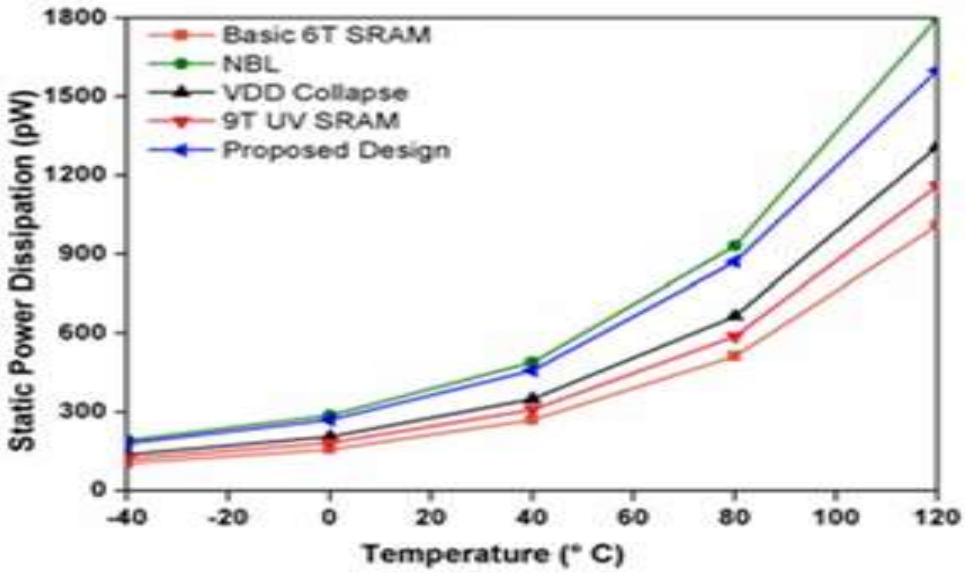


Figure 5.16. Variation of Static power dissipation vs temperature.

5.7. WRITE DELAY

The time required to write data to the storage nodes (Q/Qb) is defined as the time interval starting when the WWL signal reaches 50% of its maximum value during the write operation. At a 1V cell V_{DD}, the proposed design has a write latency of 140 ps.

Figure 5.17 shows the write latency of the proposed design at various VDDs, along with comparisons to other existing SRAMs. It is evident that the write latency of the proposed design is reduced by 33%, 39%, 48%, and 22% compared to the initial 6T SRAM cell [11], NBL [16], V_{DD} collapse [17], and 9T UV SRAM [19], respectively, at 1V.

The reduced write latency is due to the access transistor's source being at a negative voltage during the write operation, which enhances the driving capabilities of the access transistor. The cross-coupled inverter state is flipped quickly as the node storing the "1" discharges rapidly, facilitating quick data transfer to the storage nodes. Additionally, a Monte Carlo simulation was conducted to analyze the write latency of the proposed design, as shown in Figure 5.18. For 200 samples, the standard deviation and average write latency values were 32.2 ps and 140 ps, respectively, with a variability of 0.26%.

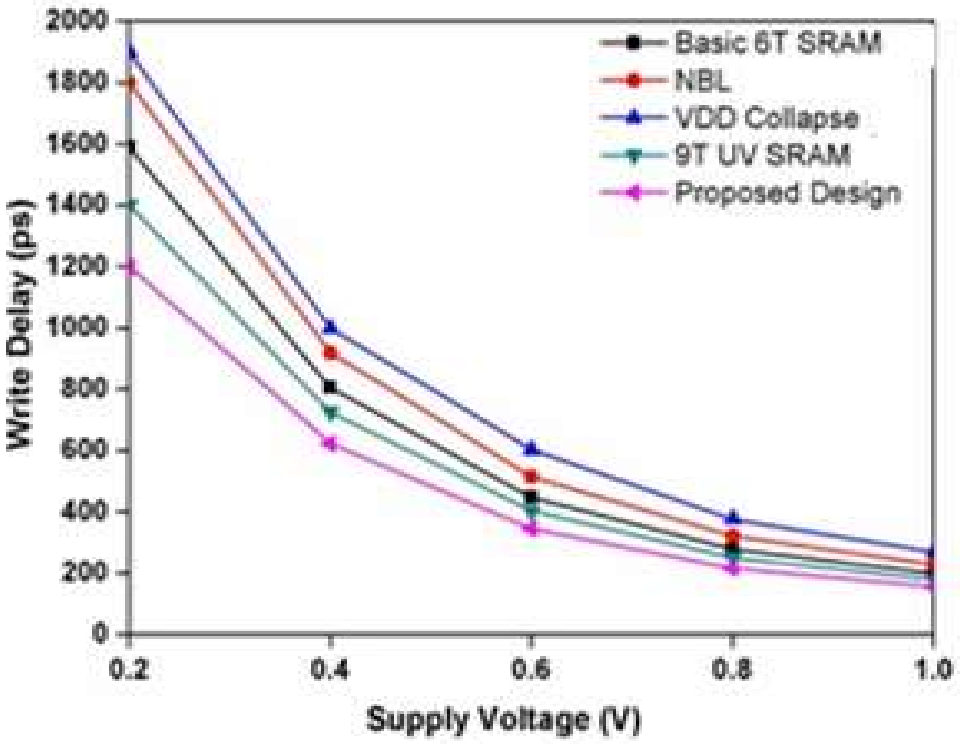


Figure 5.17. Variation of write delay vs supply voltage.

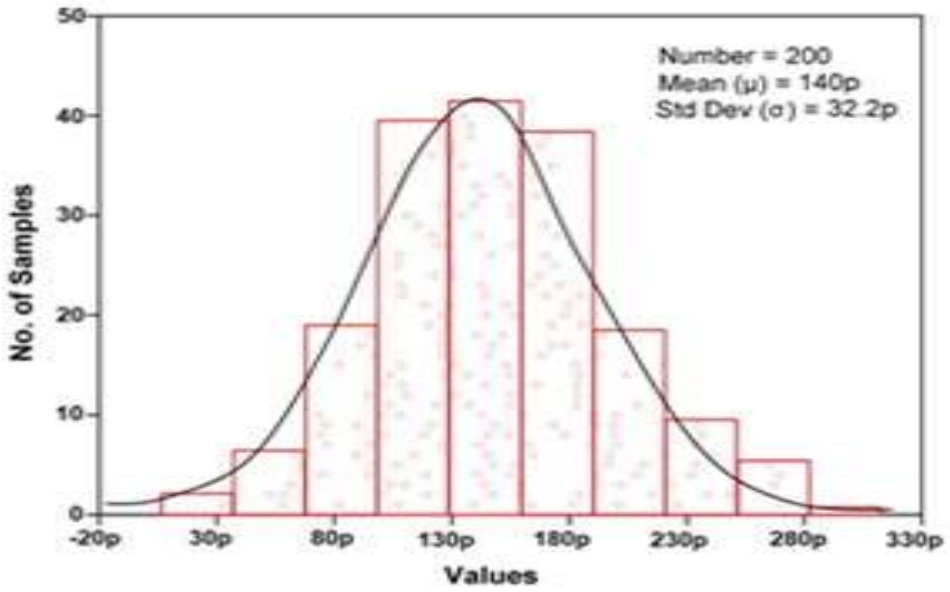


Figure 5.18. Monte Carlo of write delay for a proposed design.

5.8. READ DELAY

The time interval between the activation of the RWL signal and the RBL signal discharging to 50% of its maximum value is referred to as the read latency. At a 1V cell power supply, the proposed design has a read latency of 80 ps. Figure 5.19 shows the read latency of the proposed design at various voltages. It is observed that the read latency of the proposed design is reduced by 52%, 33%, and 38%, while it increases by 18% when compared to the initial 6T SRAM cell [11], NBL [16], V_{DD} collapse [17], and 9T UV SRAM [19], respectively. The use of an isolated read storage during the read operation contributes to the reduction in read time.

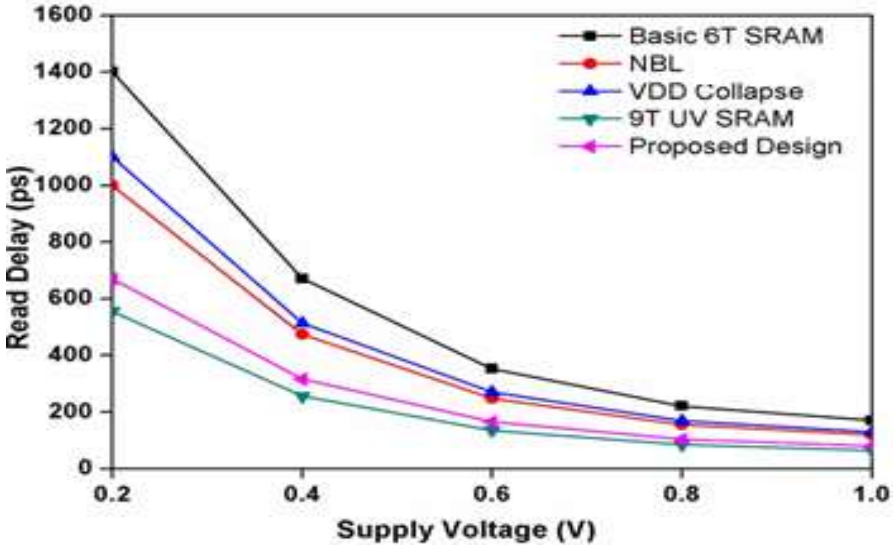


Figure 5.19. Variation of read delay vs supply voltage.

Table 5.1, presents a comparison between the proposed design and other leading state-of-the-art designs. It can be concluded that the proposed design offers superior stability and latency, although it consumes more static power than other advanced designs. This is primarily due to the incorporation of NBL circuits in the proposed design. Additionally, the proposed design enhances the write margin, which improves the write capability of the SRAM cell and reduces the write latency.

Table 5.1: Comparison of the proposed design with other state of the art work.

Parameters	**6T SRAM [6]**	**NBL [11]**	**V_{DD} Collapse [12]**	**9T UV SRAM [14]**	**8T SRAM [27]**	**10T SRAM [5]**	**Proposed Design (8T SRAM)**
Technology (nm)	28	28	28	28	28	28	28
Supply Voltage (V)	1	1	1	1	1	1	1
WSNM (mV)	330	440	410	370	350	360	490
RSNM (mV)	220	280	310	420	270	290	400
HSNM (mV)	280	310	250	320	300	310	350
Static Power Dissipation (pW)	300	520	380	340	310	370	430
Write Delay (ps)	210	230	270	180	144	138	140
Read Delay (ps)	168	120	131	64	60	419	80

5.9. DYNAMIC POWER DISSIPATION

The dynamic power dissipation of the SRAM cell can be measured during both write and read modes. The write power of the proposed design increases due to the NBL circuit's rise in the gate-to-source voltage, which leads to higher currents in the access and pull-down transistors. However, the read power of the proposed design remains minimal. Table 5.2 shows the dynamic power dissipation of the proposed design, including parasitic components, during read and write operations at various V_{DD} levels.

Dynamic power consumption during read and write operations is a key factor in evaluating SRAM performance, especially for power-sensitive applications like IoT. The dynamic power was measured through simulation, with conditions set at a 1V supply voltage, a frequency of 1 GHz, and a typical operating temperature of 27°C.

Table 5.3 compares the read and write dynamic power consumption of the proposed design with other relevant SRAM designs. The proposed design shows higher write power due to the NBL circuit's effect on the gate-to-source voltage, which increases the access transistor current. However, the read power remains competitive due to the use of an isolated read storage configuration. Dynamic power values were not included in Table 5.1, as that table focuses on static parameters, while dynamic power varies significantly with operating conditions and requires separate, detailed analysis.

Table 5.2: Read and Write Power at Different Supply Voltages

Supply Voltage (V)	Read Power	Write Power
0.2	59.00 nW	278.00 nW
0.4	505.00 nW	1.39 uW
0.6	2.20 nW	4.22 uW
0.8	6.40 uW	11.82 uW
1.0	12.50 uW	26.30 uW

Table 5.3: Dynamic Power Consumption Comparison

Design	Read Power	Write Power
6T SRAM [6]	8.5 µW	18.4 µW
NBL [11]	10.2 µW	22.6 µW
VDD Collapse [12]	9.3 µW	21.5 µW
9T UV SRAM [14]	7.8 µW	20.2 µW
8T SRAM [27]	7.0 µW	19.0 µW
Proposed Design	6.4 µW	26.3 µW

5.10. SUMMARY

In this chapter, since low-power integrated circuits are widely used in portable electronic devices, their necessity is well understood. Static Random Access Memory (SRAM) on the SoC (System on Chip) controls both the speed and power consumption of the device. Therefore, having low-power SRAMs is crucial. We have been reducing the size of CMOS devices for more than 50 years in order to make them portable, small, and to achieve superior performance in terms of access time, power consumption, latency, etc. As a result, there is a greater need for memory that is small and low-powered. Working on low supply voltage and energy leakage has become a top priority since there is a lot of room for power consumption reduction. Lower operating voltage will reduce the SRAM cell's stability, resulting in a lower static noise margin value. Certain essential factors, including static noise margin, read and write latency, static power dissipation, etc., regulate the SRAM cell. Designing an SRAM cell that performs better while taking into account all of the aforementioned characteristics at once is difficult. The designers have always had to make concessions in order to improve certain criteria at the expense of others. The necessity and application of the SRAM will determine which characteristics must be increased and which parameters can be compromised. This study offers a negative bit-line (NBL) write assist circuit for increasing the write stability of SRAM cells and a separate (isolated) read port for improving the read stability in order to increase stability and speed. In terms of write static noise margin (WSNM), write latency, read static noise margin (RSNM), and other factors, the suggested design has been compared to previous state-of-the-art work. When designed with a 1 V cell supply voltage, it has been shown that the WSNM has improved by 48%, 11%, 19%, and 32.4%, while the write latency has decreased by 33%, 39%, 48%, and 22% when compared to standard 6T SRAM cell, NBL, V_{DD} collapse, and 9T UV SRAM, respectively. In conclusion, the design and characterization of a low-leakage, high-stability SRAM cell for IoT applications is crucial for the development of portable electronic devices. This study proposes a negative bit-line (NBL) write assist circuit and a separate (isolated) read port to improve the write and read stability of the SRAM cell, respectively. The suggested design has been compared to previous state-of-the-art work, and it has been shown that the WSNM has improved significantly, while the write latency has decreased. The future scope of this study includes further optimization of the proposed design to achieve even better results in terms of power consumption, stability, and performance.

CHAPTER 6

ENERGY EFFICIENT SRAM CELL

SRAM is an essential component for computing devices. The decreasing technology node and increasing demand for portable devices with longer battery life have generated the need for re-designing SRAM for performance enhancement. Thus, in this thesis, double-ended, dual-port bit cell designs are proposed that have the ability to achieve the same. Also, a new concept for the proposed 8T SRAM cell and its functioning is explained. An energy-efficient 8T SRAM cell is also proposed to ensure easy integration of the components of SRAM. Therefore, for performance, an energy-efficient SRAM cell configuration is also proposed to lower power consumption and achieve high speed. While ensuring that the designed proposed 8T SRAM cell for low leakage. Thus, the following objective is framed to accommodate the aforementioned need –

"Energy Efficient 8T SRAM Cell for Enhancing Read/Write Assist Performances with Stability."

Methodology used to achieve the desired objective in the chapter is as follows -

- Analyze the performance of the energy-efficient SRAM cells.
- Proposed SRAM cell with voltage deviate-domino logic.
- Analyze the proposed SRAM cell for improved stability.
- Evaluate the proposed SRAM cell for leakage power consumption.

In this chapter, an overview of energy energy-efficient SRAM cell is presented, and a proposed SRAM with voltage deviate-domino logic. The chapter is divided into seven sections, including section 6.1, Low power energy efficient 8T SRAM cell, and 6.2, 8T SRAM with voltage deviate domino logic. In sections 6.3, 6T SRAM cell versus proposed 8T SRAM cell. Further, in section 6.4, Evaluation of various performance parameters. It is followed by section 6.5, Power consumption. Further, section 6.6, leakage power consumption results are analyzed. Finally, the findings of the chapter are concisely summarized in section 6.7.

6.1. LOW POWER ENERGY EFFICIENT 8T SRAM CELL

Radix-two is a prevalent choice in digital logic systems, employing a binary representation with two symbols to denote logic levels. Conversely, when the radix exceeds 2, the system is denoted as a multi-valued logic system [128-132]. Ternary logic, for example, utilizes three symbols or logic states-zero, one, and two. In the ternary system, $\log_3(2^n)$ bits are necessary to represent a binary number of n bits. Addressing pin-out issues becomes particularly challenging in VLSI circuits when dealing with multi-valued logic. The static random-access memory (SRAM) cell functions as a latch, utilizing back-to-back connected inverters to store data. It consists of a Bit Line (BL) and a select line. When the select line is active, the BL of the SRAM cell holds either read or write data [133]. Introducing ternary inverters in place of the inverters within a binary SRAM cell allows for the design of a ternary static random-access memory (TSRAM) cell [134-138]. The SRAM cell designed for ternary logic aims to facilitate the creation of larger memory arrays by utilizing ternary logic circuits [139]. In a conventional ternary SRAM cell, a traditional ternary inverter is typically employed. However, this design faces challenges in storing values effectively, leading to a notable voltage drop that directly impacts the read/write information in the SRAM cells. To overcome this issue, there is a need for the development of a ternary inverter cell capable of consistently providing the correct output voltage level for each of the three states in ternary logic [140-141]. In modern times, Carbon Nanotube Field-Effect Transistors (CNTFETs) have introduced complexity and stability challenges to SRAM design. In response to these challenges, a technology known as Enhanced Gate Diffusion Input based Ballistic Wrap Gate CNTFET (EGDI-BWGCNTFET) has been proposed. This technology is integrated with ternary static random-access memory (T-SRAM) to offer improved stability, reduced standby power consumption, minimized voltage drop, and the ability to precisely store read/write values in SRAM cells [142].

This section reviews recent literature on 8T SRAM. In 2020, Roy C. and team [143] introduced an innovative 8T SRAM cell designed for ultralow-power applications, employing a differential TG-based design. The primary goal is to minimize power consumption by integrating a single pair of transmission gates as access switches. Choosing transmission gates over pass gate access transistors results in a shorter write access time (TWA) for the proposed cell. The observed low power consumption is attributed to the stacking effect. The paper conducts a comparative analysis of design

metrics between the proposed cell and conventional 6T (CON6T) and ZIGZAG 8T (ZG8T) SRAM cells. Notably, the suggested 8T SRAM cell demonstrates a 1.159/1.179 improvement in TWA compared to CON6T and ZG8T, albeit with a 2.659 and 29 trade-off in read access time (TRA). The proposed cell shows a significant reduction in hold power consumption, marking 3.229 units lower compared to both CON6T and ZG8T SRAM cells. Furthermore, the write power consumption of the proposed cell is notably diminished, exhibiting a decrease of 4.419 and 4.449 compared to CON6T and ZG8T SRAM cells. In terms of chip area, our newly proposed cell occupies 1.379 times less space than the ZG8T cell, although it does require 1.499 times more area compared to the CON6T SRAM cell. Moreover, the suggested cell demonstrates 1.59 and 39 greater stability during write operations compared to CON6T and ZG8T SRAM cells, respectively. Although the read static margin of the proposed cell aligns with CON6T, it is 3.29 lower than that of the ZG8T SRAM cell. Noteworthy is the fact that the proposed cell not only provides improved speed but also reduces delay. In 2022, Chen J., et al. [144], introduced a dependable 8T SRAM tailored for high-speed searching and logic-in-memory operations. In this context, we introduce a groundbreaking 8T Compute SRAM (CSRAM) designed for robust and high-speed in-memory searching and intricate logic-in-memory computations. Our 8T CSRAM integrates a pair of pMOS access transistors and split Word Lines (WLs) dedicated specifically to compute access. A comprehensive circuit-level analysis highlights the pivotal role of the pMOS-based compute access port in significantly mitigating read disturbance. Furthermore, we propose an innovative elevated pre-charge voltage scheme and a sensing amplifier based on low-skewed inverters to enhance sensing speed. The effectiveness of our proposed 8T CSRAM design has been validated within a 16 Kb array utilizing 28-nm CMOS technology. Unlike the prevailing 8T CSRAM in the current landscape, our innovation not only underscores its reliability but also attains an impressive 3.1-fold increase in performance, achieving a peak operating frequency of 2.44 GHz. It excels in reduced delay and superior speed. In a 2022 study by Aura S. R. et al. [145], a novel High-Speed Dual Port 8T SRAM Cell with Simultaneous and Parallel READ-WRITE features was introduced. The proposed architecture was implemented using LTspice software in the 16nm Predictive Technology Model (PTM). The investigation involved a thorough analysis and comparison with traditional 6T, 8T, 9T, and 10T SRAM cells, considering read and write operation delays, power consumption, and power-delay product (PDP). Simulation outcomes indicate that our design outperforms its counterparts, particularly excelling in read operation speed

and overall PDP optimization. Furthermore, the design demonstrates enhanced noise margins compared to existing 6T and 9T topologies. Lastly, a comparison of the figure of merit (FoM) underscores the superior efficiency of our proposed design, achieving lower delay, albeit with higher power consumption. In a distinct development in 2021, Kim and colleagues (Kim, Y., et al. [146] introduced an innovative design for ultra-low power 8T SRAM-based Compute-in-Memory (CIM) specifically tailored for binary neural networks. The stack structure of the read unit has been cleverly devised to effectively separate read and write operations, minimizing power consumption due to leakage. Furthermore, the proposed bit cell structure enhances the stability of both read and write processes by isolating the respective paths and incorporating a higher pull-up ratio. In contrast to the prevailing SRAM-CIM technology, our proposed SRAM-CIM distinguishes itself by eliminating the requirement for additional transistors in Compute-in-Memory (CIM) vector-matrix multiplication. The implementation utilized a 16k (128 × 128) bit cell array for computing 128 neurons, employing 64 binary inputs (0 or 1) and 64 × 128 binary weight values (-1 or +1) for binary neural networks (BNNs). Each row in the bit cell array, representing a single neuron, comprises a total of 128 cells. Among these, 64 cells are specifically allocated for dot-product, while an additional 64 replica cells serve as Analog-to-Digital Converter (ADC) references. The 64 replica cells are further divided into 32 cells for ADC reference and 32 cells for offset calibration. For the quantized outputs of each neuron, a row-by-row Analog-to-Digital Converter (ADC) is employed, supporting 1–7 bits of output for each neuron. The ADC utilizes the sweeping method with 32 duplicate-bit cells, and the sweep cycle is set to 2^{N-1}, where N represents the number of output bits. In a study conducted in 2022 by Nii K. and colleagues [147], a novel strategy was introduced to address lower power consumption and increased delay. This approach focuses on Disturbance Aware Dynamic Power Reduction in Synchronous 2RW Dual-Port 8T SRAM. It involves the implementation of a self-adjusting wordline (WL) pulse timing control circuit for read/write operations. During each cycle, the row address inputs for Port A and Port B are compared to identify whether access is directed to the same row. In instances of simultaneous row access from both ports, potentially causing disturbances, the 2RW DP 8T SRAM incorporates an inherent mechanism. To mitigate disturbances and ensure sufficient margins for read/write operations, the width of the Word Line (WL) pulse is extended. Conversely, in scenarios of different row access where disturbances are not anticipated, the WL pulse width is reduced. This reduction minimizes excessive power consumption attributed to bitline discharge. To validate the

effectiveness of this proposed approach, test chips containing integrated 2RW DP SRAM macros were designed and manufactured. These chips utilized 40 nm, 28 nm, and 7 nm Fin-FET technologies. The collected data demonstrates a notable reduction in both read and write power, ranging from 6% to 13% and 13% to 28%, respectively, with the incorporation of the recommended circuits. Crucially, there is no discernible decline in speed when compared to traditional designs, and the supplementary area requirements are determined to be less than 1%. Despite achieving lower latency, this setup results in higher power consumption. In a research study conducted in 2021 by Tripathi M. R. et al. [148], the investigation focused on the influence of gate-oxide stacking on the performance of 8T SRAMs designed with source-pocket engineered (SPE) GaSb/Si heterojunction (HJ) vertical Tunnel Field Effect Transistors (VTFETs). The 8T SRAM circuits were crafted using SPE-HJ-VTFETs featuring three distinct gate-oxide engineered structures: laterally stacked HfO2/Al2O3 gate-oxide, vertically stacked Al2O3/HfO2 gate-oxide, and exclusively Al2O3 as gate-oxide. The study compared various aspects, including surface potential, electric field, transfer characteristics, drain characteristics, and intrinsic capacitances of the three types of VTFETs. Performance metrics of the SRAMs, encompassing read static noise margin (RSNM), write margin (WM), read delay, and write delay, were scrutinized for the three variants of SPE GaSb/Si HJ-VTFET structures. The investigation reveals that intrinsic capacitances arising from diverse stacking-based gate-oxide structures significantly impact SRAM performance. Notably, the 8T SRAM designed with laterally stacked gate-oxide-based SPE-HJ-VTFETs exhibits a considerably higher read delay compared to the other two 8T SRAM configurations. The evaluation of VTFETs' electrical performance utilized the commercially available SILVACO ATLAS TCAD tool, while the analysis of 8T SRAMs employed the CADENCE Virtuoso tool, utilizing Verilog-A code. Despite achieving reduced power consumption, this configuration does so at the expense of increased delay.

6.1.1 Proposed Methodology

Designing an 8T (8-transistor) static random-access memory (SRAM) cell involves creating a stable memory element using transistors. The 8T SRAM cell is a common design choice for on-chip memory due to its low leakage and good read and write characteristics.

6.1.1.1 Problem statement

In the existing work, the power consumption of the conventional 6T and 5T CNTFET

SRAM cells for all write and read operations is very high [143-148].

6.1.1.2 Rationale for Undertaking this Research Work

To overcome these challenges, finding solutions that can successfully address the issues at hand is crucial. The current SRAM architecture based on the 5T design exhibits significant drawbacks, including elevated leakage power, inefficient power utilization, and a lack of precise stability [143-148]. These shortcomings serve as the driving force behind our research endeavors.

6.1.1.3 Our Research Contribution

The main contributions of this research work are as follows:

1. In this research work, an 8T SRAM design utilizing Electrostatic Doped-Gate All-around CNTFETs is proposed for enhancing read/write assist performances with stability.
2. Electrostatic Doped-Gate All-around CNTFETs (EDGA-CNTFET) based 8T SRAM Cell design saves the data properly in the read and write signals.
3. In the pull-down network, two Electrostatic Doped-Gate All-around CNTFETs (N5 and N6) are interconnected in a Darlington configuration. The storage cell of the proposed structure comprises EDGA-CNTFETs (N1, N2, P1, P2, N5, and N6). Additionally, EDGA-CNTFETs N3 and N4 serve as access transistors, controlled by the word line. This configuration results in storage nodes Q and QB. The bit lines BL and BLB are utilized as pathways for write and read operations.
4. The presence of Darlington Electrostatic Doped-Gate All around CNTFETs in the pull-down network of the SRAM cell improves the power performance of the memory cell during the write and read conditions [143].
5. Then, the proposed Electrostatic Doped-Gate All around CNTFETs (EDGA-CNTFET) based 8T SRAM Cell design is simulated in HSPICE simulation tools.
6. Then the efficiency of the proposed Electrostatic Doped-Gate All-around CNTFETs (EDGA-CNTFET) based 8T SRAM Cell design is measured in terms of Read SNM, Write SNM, Read Delay, Write Delay, Average write power consumption, Average read power consumption, and Write and Read access time are measured.
7. Then the proposed Electrostatic Doped-Gate All-around CNTFETs (EDGA-CNTFET) based 8T SRAM Cell design is compared with the existing method-like Design of differential TG based 8T SRAM cell for ultralow-power applications [143], reliable 8T SRAM for High-Speed Searching and Logic-in-Memory Operations [144], respectively.

6.2. 8T SRAM WITH VOLTAGE DEVIATE-DOMINO LOGIC

Dynamic logic gates are an advantageous choice for applications demanding expansive memory and high speed, particularly when positioned in proximity to conventional Complementary Metal-Oxide-Semiconductor (CMOS) logical gates [149-151]. Domino logic circuits excel in achieving high speed due to their low-noise edges compared to standard CMOS logic. This low noise margin signifies increased sensitivity in domino logic circuits, contributing to enhanced noise immunity. Domino logic circuits are designed to enhance noise immunity, prioritizing signal integrity even at the cost of aggressive technology scaling. This careful design approach makes them particularly well-suited for high-performance and mission-critical applications. However, there's a trade-off in power consumption, as lowering the supply voltage to reduce power utilization can lead to increased delays in the circuit [152-154]. To counteract this delay, a primary voltage change is introduced alongside voltage scaling. Reducing the primary voltage results in an acceleration of the domino logic circuit speed [155-158]. The reduction in gate oxide thickness in scaling technology contributes to increased leakage, impacting the overall scaling of technology transformation. This leakage becomes evident in current domino circuits. Consequently, the efficiency of domino logic circuits is compromised in high voltage leakage scenarios and low-threshold noise sources. The transistor's threshold increases rapidly during transistor leakage, leading to decreased noise immunity and increased information noise in the domino circuit [159]. One critical challenge for domino OR gate frameworks is noise immunity. The pull-down network (PDN), a parallel combination of transistors in domino OR gate structures [160-162], faces issues in wide fan-outs. The dynamic nodes in these scenarios result in logic circuit failures. To address the issue of charge leaking, a weak P-channel Metal Oxide Semiconductor (PMOS) keeper transistor M2 is employed to safeguard the node. In gatekeeper mode, transistor M2 enhances noise immunity and mitigates load leakage in the dynamic node [163].

In the study by Chen et al. [164], a thorough analysis was conducted on an 8T Static Random-Access Memory (SRAM) macro specifically designed for bit-parallel searching and computing in memory (CIM). The 8T SRAM bit cell utilized in their research incorporates decoupled read and write ports, effectively eliminating read disturbance during search and CIM operations. The proposed BP-SCIM system exhibits versatility by supporting both in-memory Boolean logic and arithmetic operations.

The study introduces innovative CIM-friendly algorithms and peripheral circuits aimed at reducing the latency associated with complex arithmetic operations such as multiplication and division. In a distinct investigation, Wang et al. [165] focused on optimizing the overall area of the SRAM array while facilitating 1-bit multiplication without encountering read-disturbance issues. Their approach involved the application of an interleaving adder tree and a dual supply voltage strategy to further minimize the area and power consumption of computational circuits. Additionally, a result combination circuit was designed to enhance bit-precision flexibility. The techniques developed by the research team were implemented in a 16Kb SRAM CIM macro using 40 nm CMOS technology. In the study by Chen et al. [164], a thorough analysis was conducted on an 8T Static Random-Access Memory (SRAM) macro specifically designed for bit-parallel searching and in-memory computing (CIM). The 8T SRAM bit-cell utilized in their research incorporates decoupled read and write ports, effectively eliminating read disturbance during search and CIM operations. The proposed BP-SCIM system exhibits versatility by supporting both in-memory Boolean logic and arithmetic operations.

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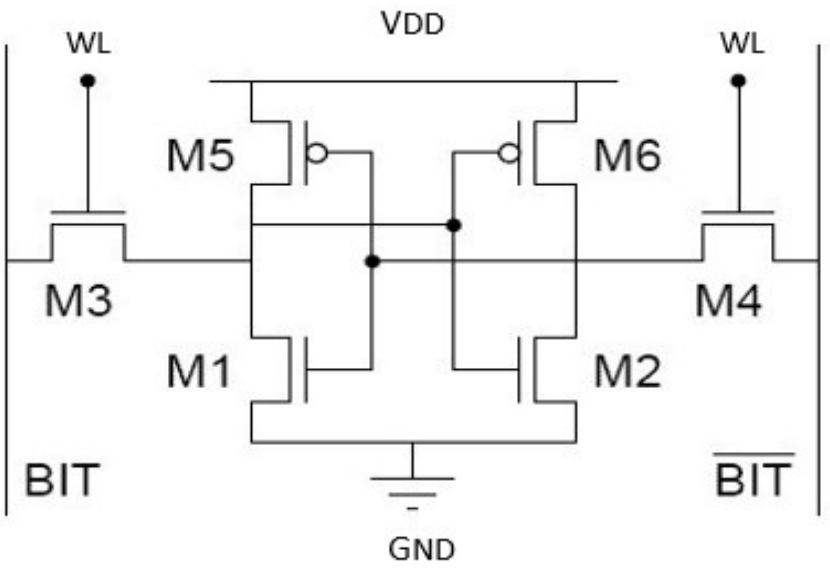
assist performances with stability. V_{DDL} [167] is a logic style designed to improve energy efficiency in memory cells like 8T SRAM. In a read operation of an 8T SRAM cell with V_{DDL}, the bit lines are pre-charged to a reference voltage. Activation of the word line (WL) connected to the access transistor enables data flow between the cell and bit lines. If the cell stores a logic "1", one of the inverters discharges the corresponding bit line, causing a voltage drop. Conversely, if the cell stores a logic "0", there is no significant voltage drop on the bit lines [166]. In a write operation, the bit lines are set to the desired values based on the data to be written. Activation of the word line allows the cross-coupled inverters to adjust their states accordingly [166]. Subsequently, the proposed Voltage Deviate-Domino Logic (V_{DDL}) Circuit-based 8T SRAM cell design undergoes simulation using HSPICE simulation tools. The efficiency of the V_{DDL}-8T SRAM-CMOS is then assessed in terms of Read SNM, Write SNM, Read Delay, Write Delay, Average Write Power Consumption, Average Read Power Consumption, Write Access Time, and Read Access Time. The performance metrics of the proposed V_{DDL}-8T SRAM-CMOS design are compared with existing methods, such as Reconfigurable 8T SRAM Macro for Bit-Parallel Searching and Computing (8T SRAM-BPSC) [164] and 8T SRAM-Based Digital Compute-In-Memory (CIM) Macro for Multiply-And-Accumulate Acceleration (8T SRAM-MAA) [165].

To sort out the complications discussed above, the proposed work offers the following benefits:

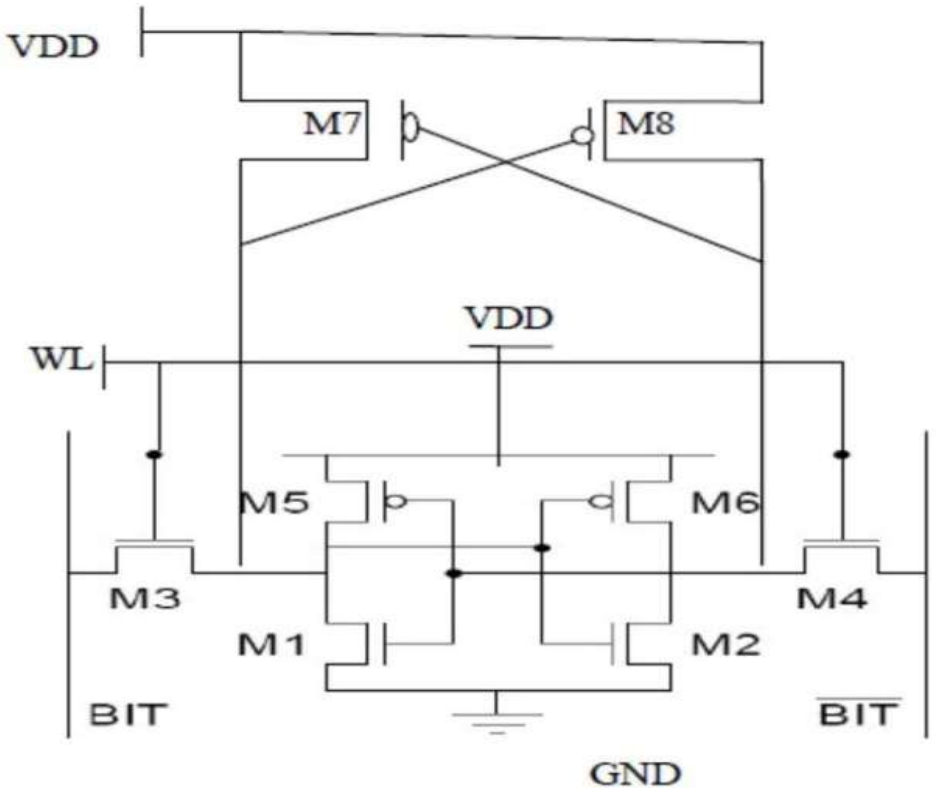
1. The suggested cell employs dual bit lines (BLs), and the selected width-to-length (W/L) ratio for the proposed cell topology significantly boosts its speed. As a result, the target bits are stored at the storage nodes in a considerably shorter amount of time.
2. Creating an 8T (8-transistor) static random-access memory (SRAM) cell entails constructing a robust memory element utilizing transistors. The 8T SRAM cell stands out as a prevalent design preference for on-chip memory owing to its minimal leakage and commendable read and write characteristics.
3. To address the challenges at hand, it is imperative to propose solutions for rectifying the existing problems. The current 6T SRAM architecture exhibits drawbacks such as elevated leakage power, suboptimal power utilization, and a lack of precise stability [164-167]. These issues have served as the driving force behind our research endeavors.

6.3. 6T SRAM CELL VERSUS PROPOSED 8T SRAM CELL

The schematic designs of the 6T SRAM and the proposed 8T SRAM cells are illustrated in Fig. 6.1 (a) and Fig. 6.1 (b), respectively. Both the 6T SRAM and proposed 8T SRAM cells feature double-ended read and write circuitry. The proposed 8T SRAM cell is specifically built on the concept of Swing Restoration Inverter (SRI). The core structure of the cell comprises two cross-connected inverters (M1, M5 and M2, M6) arranged in a back-to-back configuration. Additionally, two pass-transistors (M3 and M4) connect the drains, which serve as outputs of the inverters, while their sources are connected to the bit line (BL) and bit line bar (BLB). Two additional PMOS transistors (M7 and M8) are strategically configured to form a swing restoration inverter (SRI). In the SRI circuit, the sources of two PMOS transistors are connected to nodes Q and Qbar, and their drains are linked to the supply voltage (V_{DD}) within the topology. In the proposed 8T SRAM Cell topology, an extra pair of transistors, M7 and M8, is introduced to the cross-coupled inverters, rendering both inverters symmetrical in their configuration. The inclusion of additional transistors, M7 and M8, serves to inhibit positive feedback between the inverters, enhancing the stability of the cell. Moreover, the incorporation of these two transistors is deliberate to enforce reduced leakage, consequently leading to lower power consumption due to reduced leakage currents. The cell architecture integrates two access transistors, M3 and M4, dedicated to reading and writing desired bits into the internal storage nodes Q and Qbar. These access transistors are controlled by the word line (WL). Importantly, the 6T SRAM Cell is enhanced by the incorporation of extra transistors, M7 and M8. In this cell topology, a read and write structure is introduced, playing a key role in minimizing leakage. The read and write circuits consist of two PMOS transistors (M7 and M8). These PMOS devices, M7 and M8, function swing restoration inverter (SRI), controlled by nodes Q and Qbar. The transistors M7 and M8 are connected to the storing nodes Q and Qbar. The proposed read and write circuitry provides read and write operations while simultaneously enhancing the read and write stability of the cells. Hence, the proposed configuration effectively balances the reliability of reading and the efficiency of writing in the cell. To enhance the writing efficiency while maintaining high-speed performance, we set the width-to-length (W/L) ratio of the NMOS access transistor to the NMOS driver transistor at 1.5. Additionally, the dimensions of the PMOS load transistors are tuned to be double those of the NMOS driver transistors [26].



(a) 6T SRAM cell.



(b) Proposed 8T SRAM cell.

Figure 6.1. Static random-access memory (a) 6T SRAM cell and (b) Proposed 8T SRAM cell.

6.4. EVALUATION OF VARIOUS PERFORMANCE PARAMETERS

In this section, all simulations were performed utilizing the Cadence Virtuoso environment at the 90 nm technology node. To conduct an exhaustive exploration, we integrated several established topologies, encompassing the 6T SRAM, and the recently introduced 8T SRAM cell. This comparative investigation delves into various performance parameters, delivering an in-depth analysis of the different cell configurations.

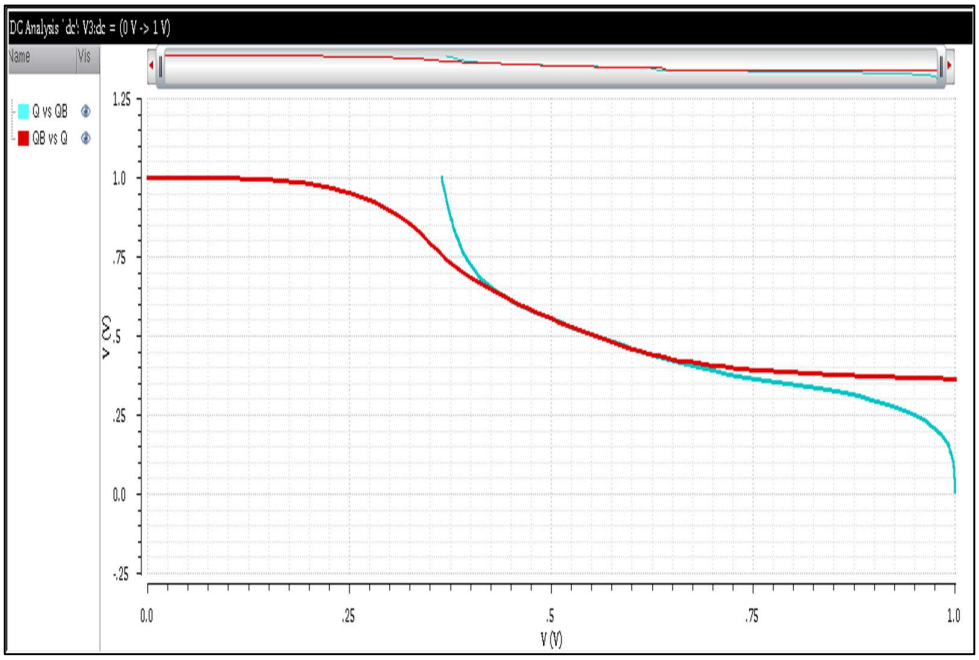
6.4.1 Stability

The SRAM cells to assess stability in various modes, static noise margin techniques are employed, and butterfly curves are plotted accordingly [63]. Stability in read, write, and hold states is determined through the analysis of read static noise margin (RSNM), write trip point (WTP), and hold static noise margin (HSNM) as elaborated in the following section.

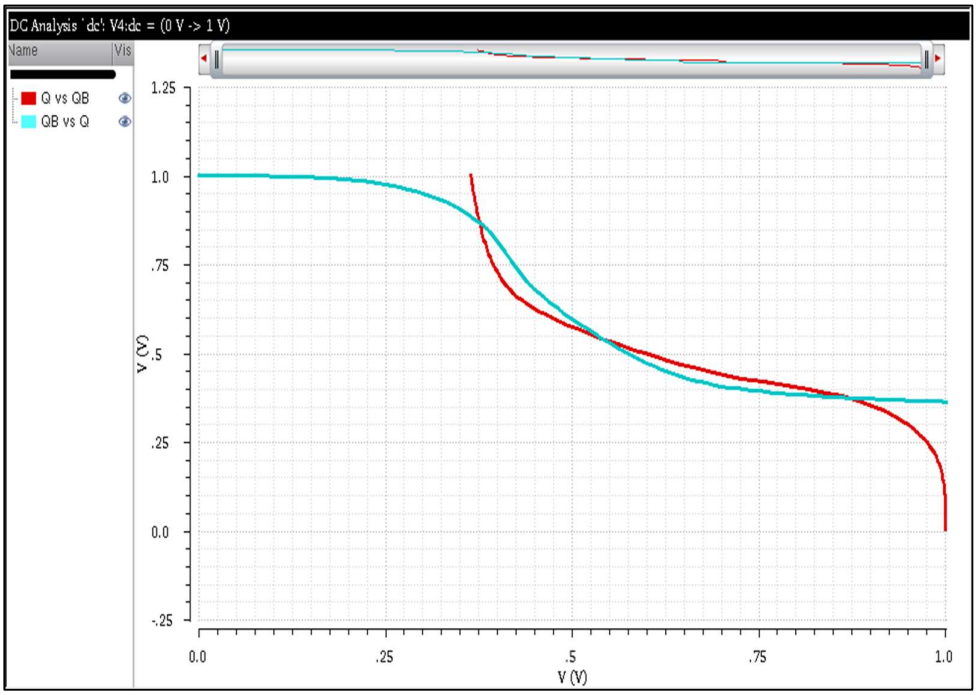
6.4.1.1 Read static noise margin (RSNM)

The Read Static Noise Margin (RSNM) serves as a critical measure for evaluating the read stability of the SRAM cell. The assessment of the read stability of the SRAM cell is known as Read Static Noise Margin (RSNM). To determine RSNM, the Butterfly Curve method is employed, where the RSNM is defined by the largest embedded square within the smaller lobe of the butterfly curve [64], [168]. A higher Read Static Noise Margin (RSNM) value indicates increased robustness during the reading process at the internal storage nodes. When performing the read operation, the butterfly curve is generated with the word-line (WL) activated. The newly introduced 8T SRAM cell demonstrates enhanced RSNM compared to the conventional 6T SRAM cell. The improved read stability of the proposed cell is attributed to the isolation of bitlines (BLs) from the internal storing nodes Q and Qbar during content reading, effectively preventing read disturbance. In contrast, the RSNM of the conventional 6T SRAM cell is often affected by the formation of a voltage divider network between the access transistor and pull-down transistor, introducing unwanted noise that can potentially alter the cell state. To address this issue, the proposed cell incorporates cross coupled-connected transistors M7 and M8. These transistors enhance node voltage, reducing the threshold voltage that minimizes leakage current through the cell. This reduction in leakage current directly contributes to the attenuation of noise at the storing nodes of the proposed SRAM cell. The read static noise margin of different SRAM cells has been analyzed, as shown in Fig. 6.2. (a) and Fig.

6.2 (b). the RSNM of the proposed cell is 12 mV, with an improvement of 53.08% as compared to the 6T SRAM cell, respectively.



(a) 6T SRAM cell.

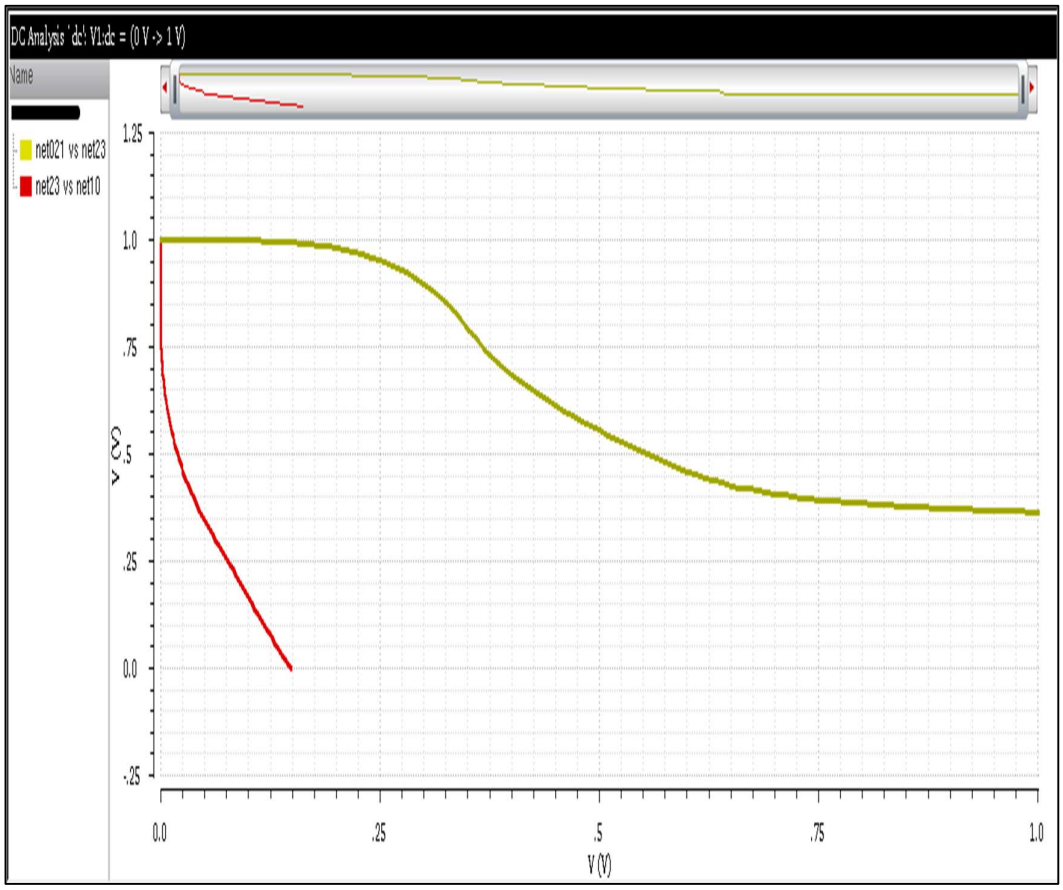


(b) Proposed 8T SRAM cell.

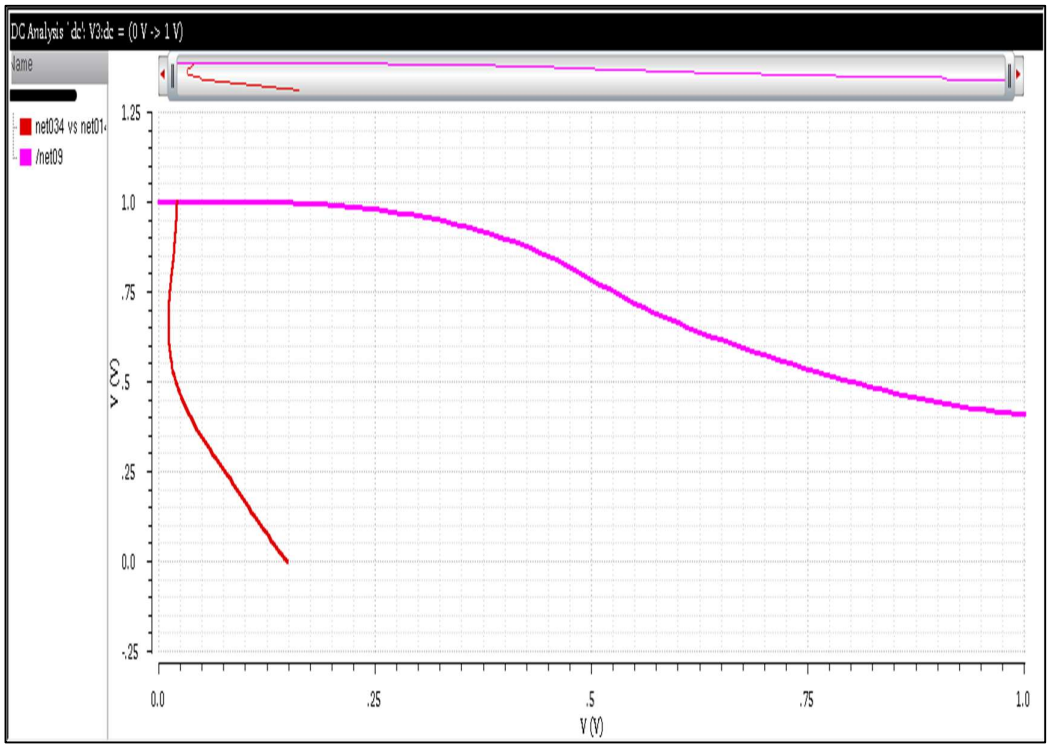
Figure 6.2. Read Static Noise Margin (RSNM) of the SRAM cells (a) 6T SRAM cell and (b) Proposed 8T SRAM cell.

6.4.1.2 Write margin (WM)

The term "write margin" refers to a cell's effectiveness in carrying out writing operations, indicating how efficiently it can write to its internal storage nodes Q and Qbar. Two commonly employed methods for assessing write ability are the write trip point (WTP) and the butterfly curve [169]. In the butterfly approach, the focus is on the largest square that can fit inside the smaller lobe of the butterfly curve. To illustrate the butterfly curve for a write operation, WL is activated. This study adopts the WTP method to determine the write margin [62]. To establish the WTP, one of the bit-lines undergoes sweeping from GND to VDD, producing a plot of Q versus Qbar. The WTP is identified as the point at which both storing nodes switch their content. Fig. 6.3. (a) and Fig. 6.3. (b) visually represent the write trip point for the 6T SRAM and the proposed 8T SRAM cell, respectively. The write trip point for the proposed SRAM cell is measured at 360 mV, which is comparable to the 6T SRAM cell. However, it is 66.66% lower than the conventional 6T and proposed 8T SRAM cells, respectively.



(a) 6T SRAM cell.



(b) Proposed 8T SRAM cell.

Figure 6.3. Write trip point (WTP) of the SRAM cells (a) 6T SRAM cell and (b) Proposed 8T SRAM cell.

6.4.1.3 Hold static noise margin (HSNM)

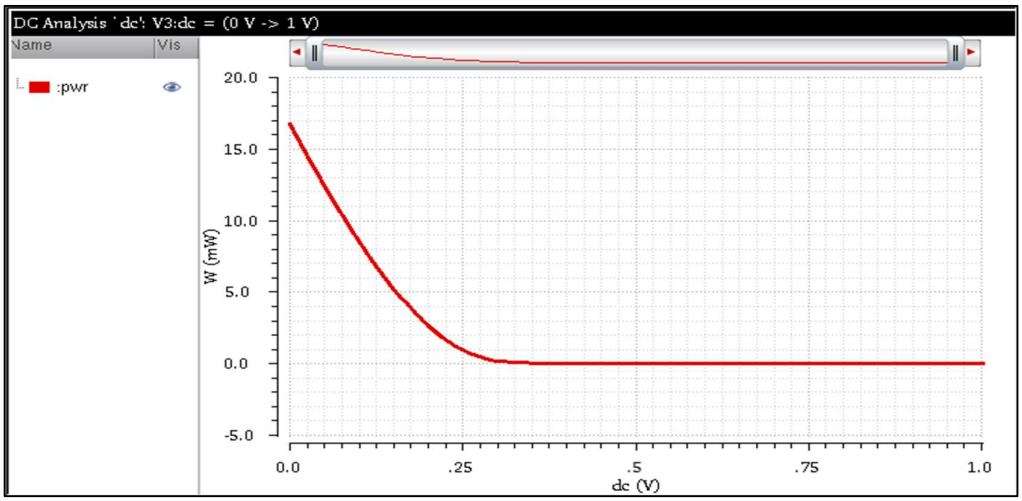
The Hold Static Noise Margin (HSNM) serves as an indicator of a cell's capacity to retain its data undisturbed in standby mode [170-171]. The Hold Static Noise Margin (HSNM) is a measure of a cell's capacity to maintain its data integrity without disruption or interference while in standby mode. During the hold operation, both word lines (WL) remain inactive. This analysis evaluates the HSNM (Hold Static Noise Margin) by employing the butterfly curve when the system is in standby mode. To improve the ability to retain data, it is essential to segregate the internal storage nodes Q and Qbar onto bit lines (BLs). This can be achieved by deactivating the word lines.

6.5. POWER CONSUMPTION

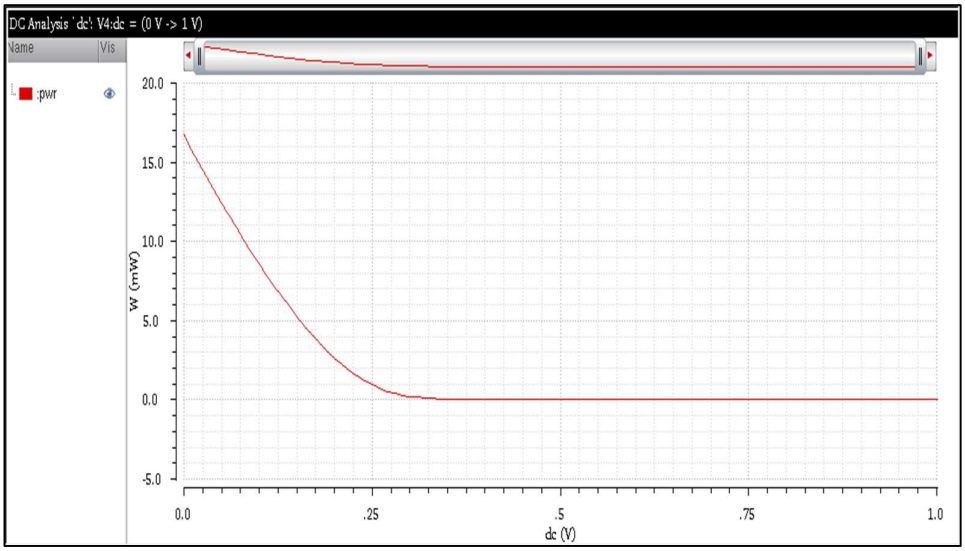
The access power refers to the energy consumed by the SRAM cell during read or write operations. It specifically measures the energy required for storing data in the internal storage nodes (Q and Qbar) during a write, and for retrieving that data from these nodes during a read. This includes both the power used in the write operation (write power) and the power used in the read operation (read power).

6.5.1. Read power consumption

In a read operation, data is accessed from the SRAM cell without altering the state of the storage nodes (Q and Qbar). However, power is still consumed by the sense amplifiers, word line drivers, and bit line pre-charge circuits involved in detecting and retrieving the stored data. The 8T SRAM cell proposed in this study shows a significant reduction in read operation power, as shown in Fig. 6.4. (a) and Fig. 6.4. (b). The proposed 8T SRAM cell as Compared to the 6T SRAM cell, the proposed 8T SRAM cell power consumed 34.0 mW and the 6T SRAM cell power consumed 34.5 mW, respectively.



(a) 6T SRAM cell.

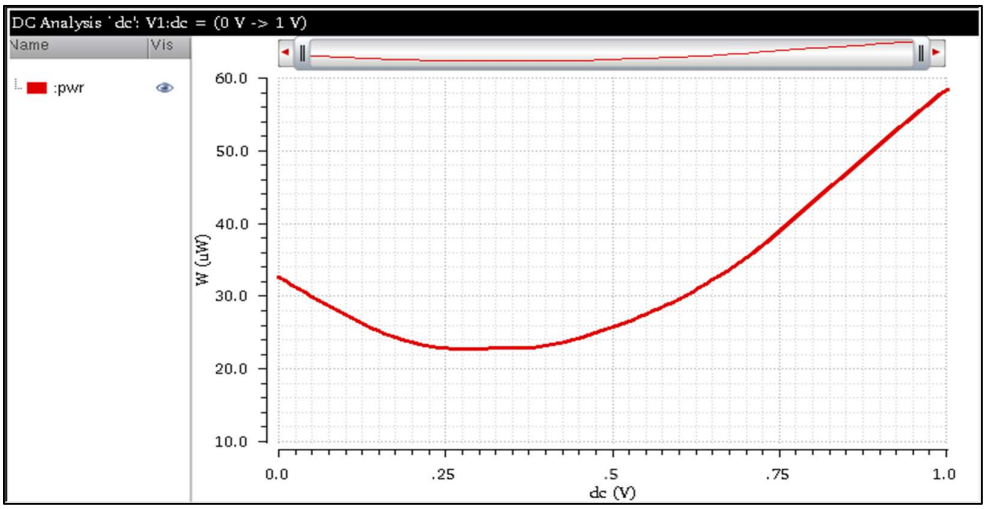


(b) Proposed 8T SRAM cell.

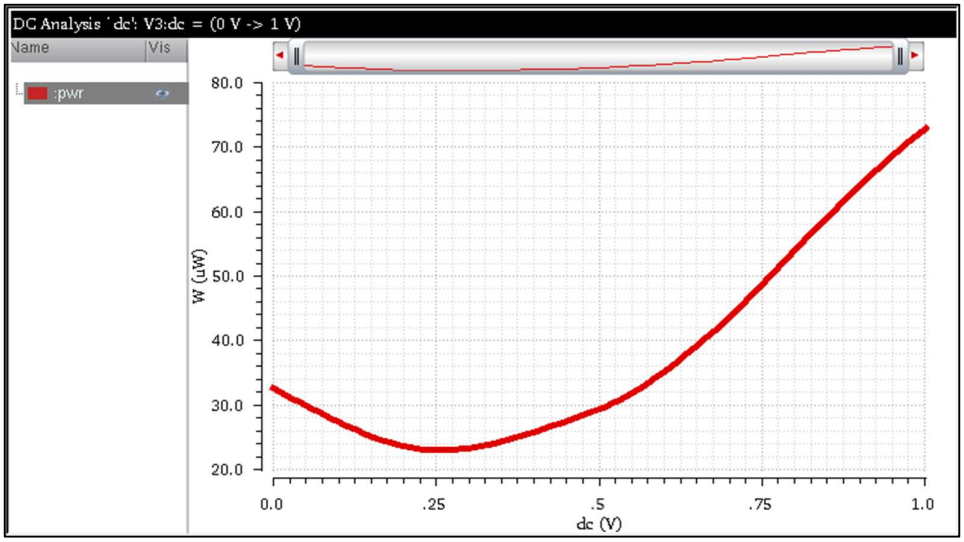
Figure 6.4. Read power consumption of the SRAM cells (a) 6T SRAM cell and (b) Proposed 8T SRAM cell.

6.5.2. Write power consumption

The writing data to the SRAM cell involves altering the state of the storage nodes (Q and Qbar), which requires charging and discharging the internal transistors, thus consuming power. This operation typically uses more power than a read, as it actively changes the cell's state. Fig. 6.5. (a) and Fig. 6.5. (b), highlight a notable reduction in write operation power for the 8T SRAM cell discussed in this study. Specifically, the proposed 8T SRAM cell reduces power consumption by 13.0 µW compared to the 6T SRAM cell, where the power consumption is 23.0 µW.



(a) 6T SRAM cell.

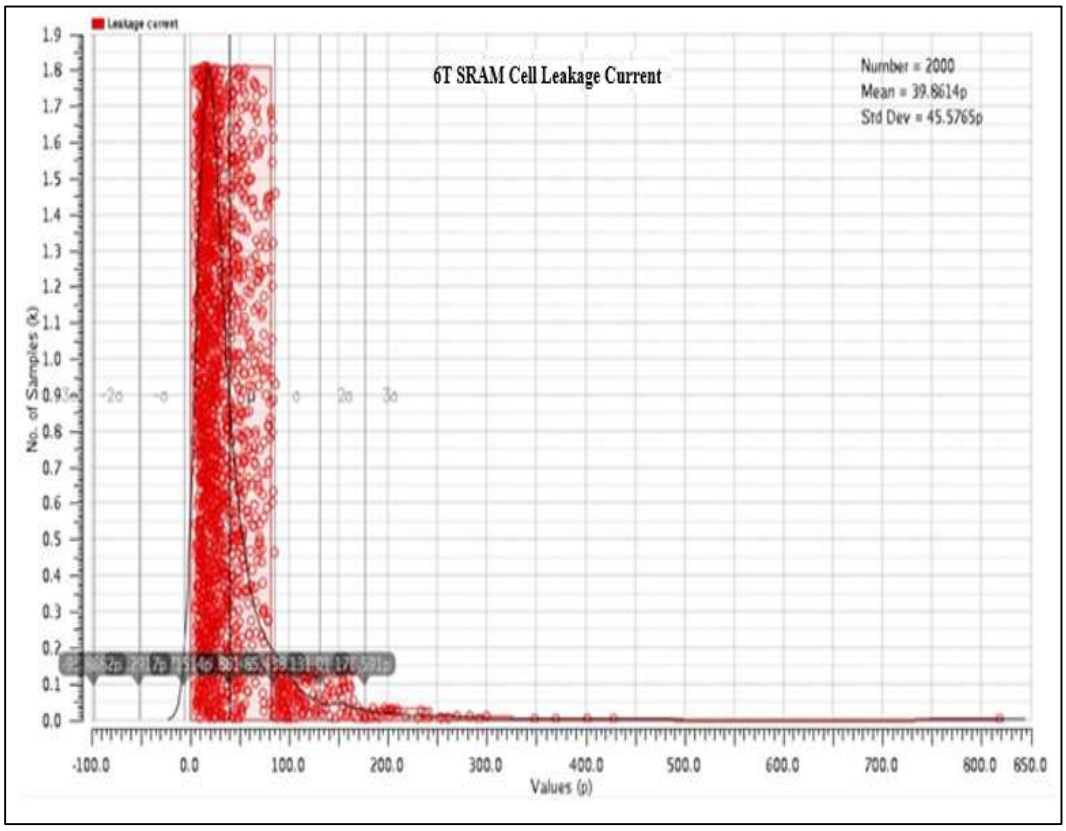


(b) Proposed 8T SRAM cell.

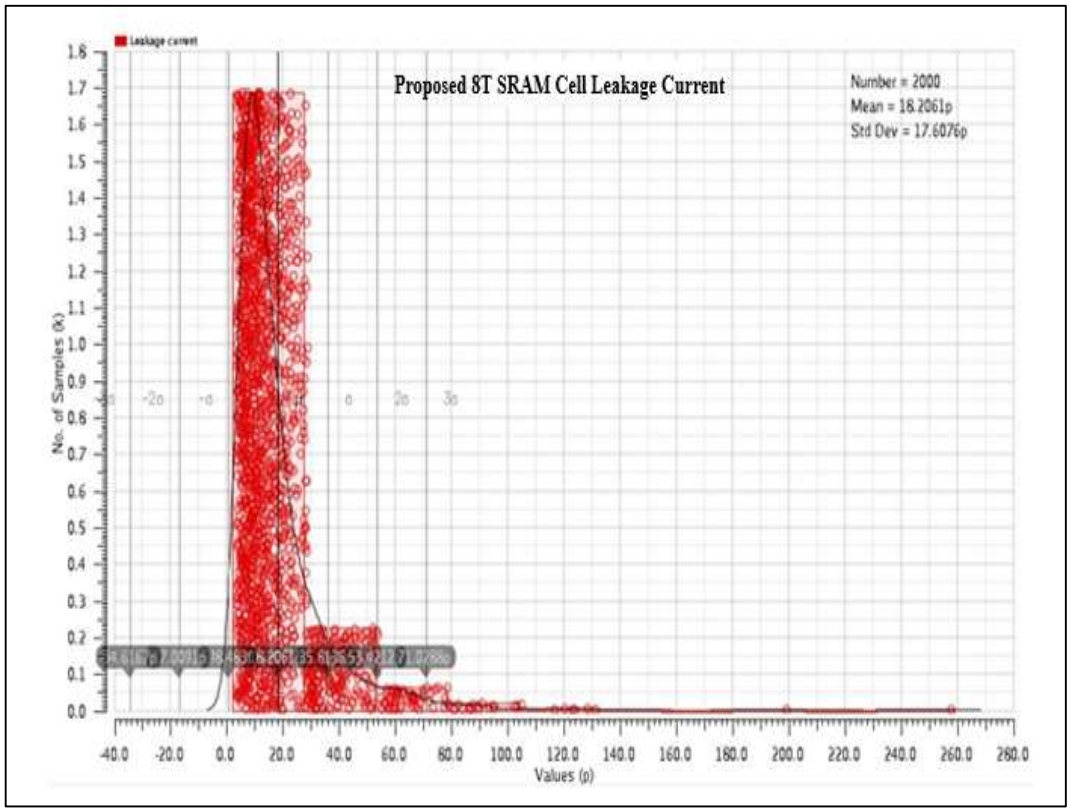
Figure 6.5. Write power consumption of the SRAM cells (a) 6T SRAM Cell and (b) Proposed 8T SRAM Cell.

6.6. LEAKAGE POWER CONSUMPTION

Leakage current becomes an issue within a circuit when a device is in cut-off mode, posing a more significant challenge in circuits with multiple devices. Technology advancements have exacerbated the problem of leakage current, particularly in circuits that remain inactive for extended periods, such as those in battery-operated devices, laptops, medical instruments, and wireless sensor networks. Although scaling the supply voltage is an effective method to reduce leakage current, it introduces a risk to cell stability. Decreasing V_{DD} levels can lead to reduced signal levels, making it more challenging to maintain cell stability [172]. The proposed 8T SRAM cell effectively addresses temperature effects compared to other considered cells. To assess the impact of process variations on SRAM cells, we performed 2000 Monte Carlo simulations for both the 6T SRAM cell and the proposed 8T SRAM cell, as depicted in Fig. 6.6. (a) and Fig. 6.6. (b), respectively. The results indicate that the 8T SRAM cell demonstrates a lower standard deviation and mean leakage current compared to the 6T SRAM cell. Table 6.1, provides a comprehensive comparison of various performance parameters for the SRAM cells.



(a) 6T SRAM cell.



(b) Proposed 8T SRAM cell.

Figure 6.6. 2000 Monte Carlo simulations for leakage current distribution of (a) 6T SRAM cell, and (b) proposed 8T SRAM cell.

Table 6.1: Comparison of various performance parameters of the SRAM cells.

Performance Parameters	**SRAM Cells**	
	6T	**Proposed 8T**
RSNM (mV)	6.37	12
WSNM (mV)	240	360
Read power consumption (mV)	34.5	34
Write power consumption (uW)	23	13
Leakage current (pA)	18.58	11.58

6.7. SUMMARY

This chapter presented a novel 8T SRAM cell design that incorporates both differential bit lines and word lines. The main goal of this architecture is to reduce leakage current, rendering it particularly suitable for applications demanding minimal power consumption. Furthermore, the proposed cell demonstrates superior speed compared to alternative topologies. In the context of the write operation, the proposed 8T SRAM cell exhibits a 66.66% performance improvement over the 6T SRAM cell, underscoring its enhanced speed. Moreover, the read operation of the proposed 8T SRAM cell is significantly improved by 53.08% compared to the 6T SRAM cell. This not only highlights its faster read performance but also emphasizes improved read stability. The comprehensive performance analysis indicates that the proposed 8T SRAM cell outperforms other considered 6T SRAM cells. This underscores its potential applicability in high-performance, power-efficient, and reliable circuit applications.

CHAPTER 7

CONCLUSIONS AND FUTURE SCOPE

SRAM is an essential component for processors. The decreasing technology node and increasing demand for portable devices with longer battery life have generated the need for re-designing SRAM for performance enhancement. Thus, in this thesis, double-ended, dual-port SRAM cell designs are proposed that can achieve the same. Also, a new concept for a swing restoration inverter (SRI) and a negative bit line (NBL) based SRAM cell, and its functioning is explained. Thereafter, for a performance energy efficient SRAM cell configuration is also proposed. Thus, in this chapter, the key findings of all chapters are summarized in section 7.1, and further in section 7.2, the future scope for the work is elaborated.

7.1 . CONCLUSIONS

SRAM is an essential component of computing devices and system-on-chip (SoCs). It is also preferred for memory implementation. The memory is formed by an array of SRAM cells for data storage and its peripheral circuits. The peripheral circuit comprises row-column decoders and pre-charge circuitry. The 6T SRAM cell was the industry standard, but with decreasing technology node and V_{DD} scaling, the performance of the 6T SRAM cell is deteriorating. This has motivated researchers to design other SRAM cells with different transistor counts and technologies to improve performance.

In this thesis, various existing SRAM cell topologies, categorized based on transistor count, technologies, and summary and observations, are reviewed to identify a viable successor for the conventional 6T SRAM cell. To improve performance for the SRAM cell in terms of stability, timing, variation analysis, and leakage power, researchers have increased the transistor count to achieve different targets, but it is observed that as the transistor count increases beyond eight, the area and cost for the cell become extremely large, making it an unfeasible alternative. Based on the performance analysis of the cells, the 8T bit cell is identified as the most reliable for the conventional 6T SRAM cell.

Thereafter, in the context of designing SRAMs for deep sub-micron technologies, a novel low-leakage inverter based on a swing restoration approach is introduced. This innovative design incorporates two additional transistors used for node restoration to minimize leakage power. The presence of these additional transistors elevates node voltages while concurrently reducing threshold voltages (V_{th}). The resulting swing restoration inverter (SRI) exhibits lower leakage power compared to Conventional inverters. At a temperature of 27°C, the SRI achieves significant leakage power savings, amounting to 67% for the 90 nm technology and 57% for the 32 nm technology, respectively. However, it is noted that as technology nodes decrease, the leakage power savings of the suggested inverter diminish. Furthermore, it is demonstrated that the dynamic power consumption is reduced in both 90 nm and 32 nm technologies when utilizing the swing restoration inverter (SRI). The implementation of SRIs in place of standard inverters in a 6T SRAM design, with the swing restoration inverter employed for SRAM design, showcases noteworthy results. Comparing the resulting proposed 8T SRAM cell to a conventional 6T SRAM at 90 nm technology, there is a substantial reduction in leakage power 86% at 108°C and 91.22% at 27°C, respectively. Importantly, the proposed 8T SRAM cell maintains low leakage while being equivalent to the 6T SRAM cell in terms of stability. Moreover, the proposed 8T SRAM cell, when incorporating swing restoration techniques, demonstrates enhanced stability compared to conventional designs. It is important to note that the proposed 8T SRAM cell integrates two additional transistors compared to the conventional 6T SRAM cell, a trade-off made to effectively reduce leakage power and enhance stability.

A low-power SRAM cell and swing node voltages are restoration circuits. Static Random Access memory circuit techniques are presented in this thesis. This thesis is a comparative study analysis of 6T SRAM, standard 8T SRAM, and low power 8T SRAM cells in 130 nm technology is also presented. This is the low power 8T SRAM cell and dual node voltage with swing restoration circuits, are perform stability analysis. hold, read, and write operations are good noise margin of the low power 8T SRAM cell is better than 6T SRAM and standard 8T SRAM cells. This conclusion is good because the power consumption is low for the SRAM cell. The low power 8T SRAM cell write mode operation, is power analysis, is better than 6T SRAM and standard 8T SRAM cells. Then the speed is higher for the low power 8T SRAM cell.

Thus, since low-power integrated circuits are widely used in portable electronic devices, their necessity is well understood. Static Random Access Memory (SRAM) on the SoC

(System on Chip) controls both the speed and power consumption of the device. Therefore, having low-power SRAMs is crucial. We have been reducing the size of CMOS devices for more than 50 years in order to make them portable, small, and to achieve superior performance in terms of access time, power consumption, latency, etc. As a result, there is a greater need for memory that is small and low-powered. Working on low supply voltage and energy leakage has become a top priority since there is a lot of room for power consumption reduction. The oxide thickness and operating voltage continue to drop as IC manufacturing technology scales. Lower operating voltage will reduce the SRAM cell's stability, resulting in a lower static noise margin value. Certain essential factors, including static noise margin, read and write latency, static power dissipation, of the SRAM cell. Designing an SRAM cell that performs better while taking into account all of the aforementioned characteristics at once is difficult. The designers have always had to make concessions in order to improve certain criteria at the expense of others. The necessity and application of the SRAM will determine which characteristics must be increased and which parameters can be compromised. This study offers a negative bit-line (NBL) write assist circuit for increasing the write stability of SRAM cells and a separate (isolated) read port for improving the read stability in order to increase stability and speed. In terms of write static noise margin (WSNM), write latency, read static noise margin (RSNM), and other factors, the suggested design has been compared to previous state-of-the-art work. When designed with a 1 V cell supply voltage, it has been shown that the WSNM has improved by 48%, 11%, 19%, and 32.4%, while the write latency has decreased by 33%, 39%, 48%, and 22% when compared to standard 6T SRAM cell, NBL, V_{DD} collapse, and 9T UV SRAM, respectively. In conclusion, the design and characterization of a low-leakage, high-stability SRAM cell for IoT applications is crucial for the development of portable electronic devices. This study proposes a negative bit-line (NBL) write assist circuit and a separate (isolated) read port to improve the write and read stability of the SRAM cell, respectively. The suggested design has been compared to previous state-of-the-art work, and it has been shown that the WSNM has improved significantly, while the write latency has decreased.

A novel 8T SRAM cell design that incorporates both differential bit lines and word lines. The main goal of this architecture is to reduce leakage current, rendering it particularly suitable for applications demanding minimal power consumption. Furthermore, the proposed cell demonstrates superior speed compared to alternative topologies. In the context of the write operation, the proposed 8T SRAM cell exhibits a 66.66%

performance improvement over the 6T SRAM cell, underscoring its enhanced speed. Moreover, the read operation of the proposed 8T SRAM cell is significantly improved by 53.08% compared to the 6T SRAM cell. This not only highlights its faster read performance but also emphasizes improved read stability. The comprehensive performance analysis indicates that the proposed 8T SRAM cell outperforms other considered 6T SRAM cells. This underscores its potential applicability in high-performance, power-efficient, and reliable circuit applications.

7.2 . FUTURE SCOPE

Based on the research carried out in this thesis and the reported results, the following future scope is suggested.

A SRAM cell is the key component for memory. It is the key focus of researchers for improving memory performance. But most researchers predominantly focus on the design of the SRAM cell, its transistor count, and the control signal. But when the transistor count goes beyond eight, the increase in area and cost for the cell outweighs all its performance merits. Presently, for low power applications, promising results are obtained for memory cells designed using swing restoration inverter (SRI) and negative bit line circuits (NBL). The SRI and NBL circuits are used to alter the memory core for the cells. The major highlight of SRI and NBL-based memory cells is that it can be designed using only eight transistors. Thereby significantly lowering its transistor count, area, and V_{DD}. Therefore, it is essential for researchers to explore this technique and propose cells with similar techniques that are unique and focus on modifying the latch-based memory core for performance improvement for the bit cell.

Along with the conventional 6T SRAM cell design, the concept of 8T SRAM cell can also be explored as a potential for IoT applications. Presently, in this thesis, the idea for the proposed 8T SRAM cell and its performance are presented. The concept, as well as the cell design, can be further extended and modified for application-specific requirements. Also, it is to be used as a foundational unit for memory design; array analysis can be performed and optimized for the modes of operation cell as well. Additionally, there is the possibility of designing an SRAM operation SA for easy integration with the SRAM cells. In conclusion, while working at the 90 nm technology node has its limitations, it was a relevant choice for the research given its widespread adoption at the time. However, it is essential to acknowledge these limitations and to consider how to extend and adapt the

proposed techniques to newer technology nodes in future work. The future scope of this study includes further optimization of the proposed design to achieve even better results in terms of power consumption, stability, and performance. As the SRAM cell for the memory is altered, it mandates re-designing its corresponding SA topology as well. Present-day SAs are efficient but still face a major bottleneck in terms of V_{DD} lowering. This also hampers lowering the operational V_{DD} for the cell, as the two have to work in conjunction. Thus, it is essential to come up with design techniques and circuit modifications that enable V_{DD} lowering of the memory. In addition to lowering the voltage, it is also essential to check if the concepts of SRI and NBL are applicable to SAs. To check if there is a possibility to alter the latch-based voltage mode SAs to be designed with a different core. This will open a new dimension for designing memory.

The array analysis is another essential parameter for memory. It has the capability to analyze the performance of the memory. For arrays, most research revolves around cell stability, leakage power, read-write timing analysis, and array size optimization. But parameters such as bit-interleaving, sub-bank sizing, and divided word line architecture for memory are fields that have potential for array performance optimization. These are areas that are purely array-centric and do not rely on modifying and improving the performance of the cell. These array analysis factors have not received as much attention, but hold immense potential for performance enhancement for memory.

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LIST OF PUBLICATIONS

Papers Published in National/International Journals

1. Ram Murti Rawat and Vinod Kumar, **"Design and analysis of SRAM cell using swing restoration inverter for low power applications",** International Journal of Electronics, vol. 1, pp. 1–19, 2025. doi: 10.1080/00207217.2025.2450733. **(SCIE, IF: 1.1) (Published).**

2. Ram Murti Rawat, Vinod Kumar, **"Design and Characterization of a Low-Leakage, High-Stability SRAM Cell for IoT Applications",** Indian Journal of Engineering and Materials Sciences (IJEMS), Vol. 31 No.5, pp. 627-640, 2024. https://doi.org/10.56042/ijems.v31i5.6683. **(SCIE, IF: 0.9) (Published).**

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